1983

INTERFACE
BIPOLAR LSI
BIPOLAR MEMORY
PROGRAMMABLE LOGIC

DATABOOK

National Semiconductor

INTERFACE
BIPOLAR LSI
BIPOLAR MEMORY
PROGRAMMABLE LOGIC
DATABOOK

NATIONAL
SEMICONDUCTOR
CORPORATION

INTERFACE
BIPOLAR LSI
BIPOLAR MEMORY
PROGRAMMABLE LOGIC
DATABOOK

All physical dimensions appear at the end of the databook.

Introduction

The 1983 edition of the National Semiconductor Interface / Bipolar LSI / Bipolar Memory / Programmable Logic Databook is the most comprehensive available. It contains complete specifications on these high technology products, as well as applications information, product selection and cross reference guides.

Quality and Reliability

As electronic systems become more and more complex, the need for consistently high quality integrated circuits becomes increasingly important. Having recognized this need as far back as the 1970s, National Semiconductor initiated a unique, company-wide Quality Improvement Program. The results have been dramatic and, we believe, unmatched in this industry. Over the years, National has regularly been named by many major customers as "Quality Manufacturer of the Year." We are proud of our success, which sets a standard for others to achieve. And yet our quest for perfection is ongoing, so that customers can continue to rely on National Semiconductor integrated circuits and products in their system designs.

Einführung

Die 1983er Ausgabe des National Semiconductor Interface/Bipolar LSI/Bipolar Memory/Programmable Logic Datenbuches ist die umfassendste Ausgabe die jemals zur verfügung stand. Sie beinhaltet komplette Spezifikationen dieser hochtechnologischen Produkte so wie Angaben über Anwendungsmöglichkeiten, Produktselektion und Referenzlisten.

Qualität und Zuverlässigkeit

Mit der zunehmenden Komplexität der elektronischen Systeme wird die Notwendigkeit integriete Schaltungen mit hoher Qualität immer wichtiger. Dies bereits in den 70iger Jahren erkannt, entwickelte National Semiconductor ein einmaliges, firmenweites "Qualitätsverbesserungsprogramm". Die damit von National Semiconductor erreichten Ergebnisse sind bis heute—wie wir glauben—unerreicht. Während der letzten Jahre wurde National Semiconductor regelmässig als "Qualitätshersteller Nr 1" bewertet. Auf diesen Erfolg sind wir stolz. Er setzt neue Mass-Stäbe für die Industrie. Und doch gehen unsere Austrengungen zu immer höheren Perfektion weiter, so dass sich unsere Kunden auch in Zukunft auf National Semiconductor's integriete Schaltungen und Produkte in ihren Systemen absolut verlassen können.

Introduction

L'edition 1983 du catalogue National Semiconductor Interface/Bipolar LSI/Bipolar Memory/Programmable Logic est le plus accessible des catalogues disponibles. Le contenu de cette édition spécifie complétement ces produits à technologie de pointe et décrit des examples d'application, plus une selection de produits avec une liste de correspondance.

Qualité et Fiabilité

La complexité croissante des systèmes electroniques demande des circuits intégrés de plus en plus haute qualité. Conscient de ce besoin dès les années '70 National Semiconductor fut à l'origine d'un programme unique accentuant la qualité de tous ses produits. Les résultats furent spectaculaires et inégalés. Depuis National Semiconductor a reçu la distinction pour la qualité de ses produits de la part de ses clients. Nous sommes fiers de ce succès qui force les autres à suivre nos standarts. Notre recherche de la perfection se poursuit apportant la confiance pour nos clients en nos produits et leur utilisation pour leurs systèmes.

TRADEMARKS

Following is the most current list of National Semiconductor Corporation's trademarks and registered trademarks.

Abuseable™
Anadig™
Auto-Chem Deflasher™
BI-FET™
BLC/BLX™
CIM™
CIMBUS™
CIM-BD™
CIM-XXX™
COPS™ microcontrollers
DIB™
DIGITALKER™
DISCERN™
DNR™
DPVM™
E-Z-LINK™
HEX 3000™
ISE™
Integral ISE™
Intelisplay™
ISE-16™
M²CMOS™
Macrocomponent™
Microbus™ data bus (adjective)
microCMOS™
MICROWIRE™
MICRO-DAC™
MST™
Nitride Plus™
Nitride Plus Oxide™
NSC800™
NS16000™
NSX-16™
NURAM™
OXISS™
P²CMOS™
Perfect Watch™
Polycraft™
POSitalker™
QUAD3000™
RAT™
Shelf-Chek™
SERIES/800™
SPIRE™
Starlink™
STARPLEX™
STARPLEX II™
SuperChip™
SYS-16™
TAPE-PAK™
Trapezoidal™
TRI-CODE™
TRI-POLY™
TRI-SAFE™
XMOS™
XPU™
Z STAR™
883B/RETS™
883S/RETS™
The National Anthem®
Datachecker®
Maxi-ROM®
TRI-STATE®

PAL® and PALASM® are registered trademarks of Monolithic Memories, Inc.
VAX® is a registered trademark of Digital Equipment Corp.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation 2900 Semiconductor Drive Santa Clara, California 95051 Tel: (408) 721-5000 TWX: (910) 339-9240

Table of Contents

Section 1—Transmission Line Drivers/Receivers

Table of Contents (Continued)

Section 2—Bus Transceivers

Section 3—Peripheral/Power Drivers

Section 4—Level Translators/Buffers

Table of Contents (Continued)

Section 5—Display Controllers/Drivers

Table of Contents (Continued)

Section 6—Memory Support

Section 7—Dynamic Memory Support

Table of Contents (Continued)

Section 8—Microprocessor Support

Section 9—Data Communications Support

Section 10—Disk Support

Section 11—Frequency Synthesis

Section 12—Interface Appendices

Sections 13 thru 20 for future expansion in supplement books

Table of Contents (Continued)

Section 21—Bipolar PROMs

Table of Contents (Continued)

Section 22—Bipolar and ECL RAMs

Section 23—2900 Family/Bipolar Microprocessor

Table of Contents (Continued)

Section 24—Programmable Logic

Alpha-Numerical Index

Alpha-Numerical Index (Continued)

Alpha-Numerical Index (Continued)

Alpha-Numerical Index (Continued)

Alpha-Numerical Index (Continued)

Alpha-Numerical Index (Continued)

Alpha-Numerical Index (Continued)

Alpha-Numerical Index (Continued)

Alpha-Numerical Index (Continued)

Alpha-Numerical Index (Continued)

Section 1
Transmission Line Drivers/Receivers

1

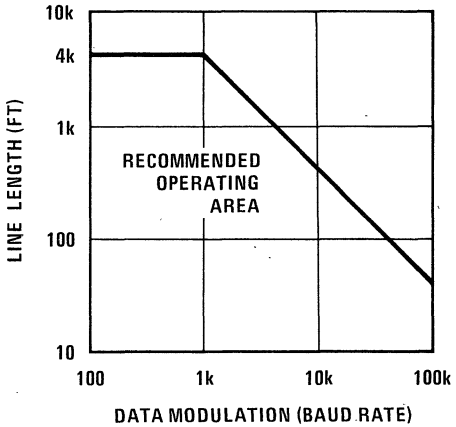
TEMPERATURE RANGE		DESCRIPTION	PAGE NUMBER
−55°C to +125°C	0°C to +70°C		
—	DS1488	Quad Line Driver	1-7
—	DS1489	Quad Line Receiver	1-10
—	DS1489A	Quad Line Receiver	1-10
*DS26LS31M	DS26LS31C	Quad Differential Line Driver	1-12
*DS26LS32M	DS26LS32C	Quad Differential Line Receiver	1-15
—	DS26LS32AC	Quad Differential Line Receiver	1-15
*DS26LS33M	DS26LS33C	Quad Differential Line Receiver	1-15
—	DS26LS33AC	Quad Differential Line Receiver	1-15
—	DS3486	Quad RS-422, RS-423 Line Receiver	1-18
DS3587	DS3487	Quad TRI-STATE Line Driver	1-22
*DS1603	DS3603	Dual TRI-STATE Line Receiver	1-25
*DS1650	DS3650	Quad Differential Line Receiver	1-31
*DS1652	DS3652	Quad Differential Line Receiver	1-31
*DS1691A	DS3691	RS422-RS423 Line Drivers	1-37
*DS1692	DS3692	TRI-STATE Differential Line Driver	1-42
—	DS3695	Differential TRI-STATE Bus/Line Transceiver	1-47
—	DS3696	Differential TRI-STATE Bus/Line Transceiver	1-47
—	DS3697	Differential TRI-STATE Bus/Line Transceiver/ Repeater	1-47
—	DS3698	Differential TRI-STATE Bus/Line Transceiver/ Repeater	1-47
*DS55107	DS75107	Dual Line Receiver	1-25
—	DS75207	Dual Line Receiver	1-25
*DS55108	DS75108	Dual Line Receiver	1-25
—	DS75208	Dual Line Receiver	1-25
*DS55113	DS75113	Dual TRI-STATE Differential Line Driver	1-52
*DS55114	DS75114	Dual Differential Line Driver	1-57
*DS55115	DS75115	Dual Differential Line Receiver	1-61
DS55121	DS75121	Dual Line Driver	1-66
*DS55122	DS75122	Triple Line Receiver	1-68
—	DS75123	Dual Line Driver	1-71
—	DS75124	Triple Line Receiver	1-73
—	DS75125	Seven-Channel Line Receiver	1-76
—	DS75127	Seven-Channel Line Receiver	1-76
—	DS75128	Eight-Channel Line Receiver	1-80
—	DS75129	Eight-Channel Line Receiver	1-80
—	DS75150	Dual Line Driver	1-84
—	DS75154	Dual Line Receiver	1-87
DS7820	DS8820	Dual Line Receiver	1-91
*DS7820A	DS8820A	Dual Line Receiver	1-94
*DS78C20	DS88C20	Dual CMOS Compatible Differential Line Receiver	1-98
*DS7830	DS8830	Dual Differential Line Driver	1-101
*DS7831	DS8831	Dual TRI-STATE Line Driver	1-104
*DS7832	DS8832	Dual TRI-STATE Line Driver	1-104
*DS78C120	DS88C120	Dual CMOS Compatible Line Receiver	1-109
*DS78LS120	DS88LS120	Dual Differential Line Receiver	1-116
MM78C29	MM88C29	Quad Single-Ended Line Driver	CMOS
MM78C30	MM88C30	Dual Differential Line Driver	CMOS
—	AN-22	Integrated Circuits for Digital Data Transmission	1-123
—	AN-108	Transmission Line Characteristics	1-139
—	AN-214	Transmission Line Drivers and Receivers for EIA Standards RS-422 and RS-423	1-145
—	AN-216	Summary of Electrical Characteristics of Some Well Known Digital Interface Standards	1-155

*Also available screened in accordance with MIL-STD-883 Class B. Refer to National Semiconductor's "The Reliability Handbook".

UNBALANCED (COMMON-MODE) TRANSMISSION DRIVERS AND RECEIVERS

Unbalanced data transmission isn't recommended for long lines or fast data rates. Unbalanced line receivers are sensitive to common-mode noise, such as ground IR noise and induced reactive noise. Unbalanced line drivers should employ slew rate control to prevent near end crosstalk to other wires in the cable. Receivers should employ response control and hysteresis. Unbalanced data transmission was preferred because the cabling requires only one wire/signal plus ground and the circuits were lower cost. New lower cost circuits available today negate the last argument. Many old interfaces such as RS-232 will continue to exist for many years, and so will the application for unbalanced circuits.

Line length is a function of data rate (baud) and slew rate. The recommended safe operating area (line length vs baud rate is shown below for 24 AWG wire. It assumes that a differential line receiver is used which is referenced at the driver ground. Also, it assumes that the driver slew rate is between 0.1 to 0.3 times the reciprocal of the baud rate (minimum unit interval). Otherwise, line lengths greater than 50 feet are not recommended. The exception to line length is the 360 I/O coaxial interface. The coaxial provides improved grounding and eliminates crosstalk.



UNBALANCED DRIVERS

Propagation Delay (ns)	Output Voltage (V)	Output Current (mA)	Slew Rate Control	Party-Line Application	Open-Collector or Open Emitter	Power Supplies (V)	Standard	Circuits/ Package	Device Number		Comment	Page No.
									Commercial 0°C to +70°C	Military −55°C to +125°C		
200	±6 or ±9	±6	I_{OS}/C			±9 or ±15	RS-232	4	DS1488			1-7
60	±5	±10	I_{OS}/C			±12	RS-232	2	DS75150			1-84
200	±2	±20	C_{EXT}	Yes	TRI-STATE®	5 or ±5	RS-423	4	DS3691	DS1691A		1-37
200	±2	±20	C_{EXT}	Yes	TRI-STATE	5 or ±5	MIL 188-114	4	DS3692	DS1692	±10V common-mode range	1-42
10	2.4	−100		Yes	Emitter	5	360 I/O	2	DS75121	DS55121	50Ω coax. driver	1-66
10	2.4	−100		Yes	Emitter	5	360 I/O	2	DS75123		50Ω coax. driver (IBM)	1-71
20	0.7	300		Yes	Emitter and Collector	5		2	DS75450			3-51
18	0.7	300		Yes	Collector	5		2	DS75451	DS55451		3-51
26	0.7	300		Yes	Collector	5		2	DS75452	DS55452		3-51
18	0.7	300		Yes	Collector	5		2	DS75453	DS55453		3-51
27	0.7	300		Yes	Collector	5		2	DS75454	DS55454		3-51

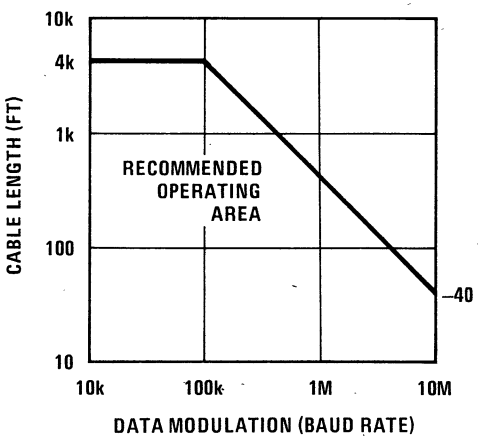
UNBALANCED RECEIVERS

Propagation Delay (ns)	Threshold Sensitivity (V)	Input Range (V)	Hysteresis (mV)	Response Control	Strobed or TRI-STATE®	Power Supplies (V)	Standard	Circuits/ Package	Device Number		Comments	Page No.
									Commercial 0°C to +70°C	Military −55°C to +125°C		
30	3	±25	250	C_{EXT}		5	RS-232	4	DS1489			1-10
30	3	±25	1150	C_{EXT}		5	RS-232	4	DS1489A		Preferential in applications to DS1489	1-10
22	3	±25	800	C_{EXT}		5 or 15	RS-232	4	DS75154			1-87
50	±0.2	±25	50	C_{EXT}	Strobed	5	RS-423	2	DS88LS120	DS78LS120	Fail-safe	1-116
50	±0.2	±25	50	C_{EXT}	Strobed	5 to 15	RS-423	2	DS88C120	DS78C120	Fail-safe	1-109
17	±0.2	±7	100		TRI-STATE	5	RS-423	4	DS26LS32C	DS26LS32M		1-15
23	±0.2	±7	100		TRI-STATE	5	RS-423	4	DS26LS32AC		Fail-safe	1-15
17	±0.5	±15	200		TRI-STATE	5	RS-423	4	DS26LS33C	DS26LS33M		1-15
23	±0.5	±15	200		TRI-STATE	5	RS-423	4	DS26LS33AC		Fail-safe	1-15
25	±0.1	±15	100		TRI-STATE	5	RS-423	4	DS3486			1-18
20	0.8 to 2	7	600		Strobed	5	360 I/O	3	DS75122	DS55122	50Ω coax. receiver	1-68
20	0.8 to 2	7	400		Strobed	5	360 I/O	3	DS75124	DS55124	50Ω coax. receiver (IBM)	1-73
16	0.7 to 1.7	−2/7				5	360 I/O	7	DS75125		IBM coax. receiver	1-76
16	0.7 to 1.7	−2/7				5	360 I/O	7	DS75127		IBM coax. receiver	1-76
16	0.7 to 1.7	−2/7				5	360 I/O	8	DS75128		IBM coax. receiver	1-80
16	0.7 to 1.7	−2/7				5	360 I/O	8	DS75129		IBM coax. receiver	1-80

BALANCED (DIFFERENTIAL) TRANSMISSION LINE DRIVERS AND RECEIVERS

Balanced data transmission is applicable for long lines in the presence of high common-mode noise. Balanced circuits don't generate much noise and are also not susceptible to common-mode noise, and therefore work well in long lines when cabled with other signals.

Line length is a function of data rate (baud) and the combination of IR drop and skin effect. Refer to AN-108 and AN-22. The recommended safe operating area (line length vs baud rate) is shown for 24 AWG wire.



BALANCED DRIVERS

Propagation Delay (ns)	V_{OL} (V)/ I_{OL} (mA)	V_{OH} (V)/ I_{OH} (mA)	Party Line Application	TRI-STATE®	Open-Collector	Power Supplies (V)	Standard	Circuits/ Package	Device Number		Comments	Page No.
									Commercial 0°C to +70°C	Military −55°C to +125°C		
10	0.5/40	1.8/−40				5		2	DS8830	DS7830		1-101
100	0.4/11	2.9/−57				5 or 15		2	MM88C30	MM78C30	CMOS comparator	CMOS
100	0.4/11	2.9/−57				5 or 15		2	MM88C29	MM78C29	Non-inverting MM88C30	CMOS
10	0.5/40	1.8/−40	Yes	TRI-STATE		5		2	DS8831	DS7831		1-104
10	0.5/40	1.8/−40	Yes	TRI-STATE		5		2	DS8832	DS7832	DS8831 without V_{CC} clamp diode	1-104
13	0.4/40	2/−40	Yes	TRI-STATE	Optional	5		2	DS75113	DS55113		1-52
15	0.4/40	2/−40			Optional	5		2	DS75114	DS55114		1-57
200	−2/20	2/−20	Yes	TRI-STATE		5 or ±5	RS-422	2	DS3691	DS1691A		1-37
200	−2/20	2/−20	Yes	TRI-STATE		5 or ±5		2	DS3692	DS1692	±10V TRI-STATE common-mode range	1-42
15			Yes	TRI-STATE		5	RS-485	1	DS3695		RS-485 Transceiver	1-47
15			Yes	TRI-STATE		5	RS-485	1	DS3696		RS-485 Transceiver	1-47
15			Yes	TRI-STATE		5	RS-485	1	DS3697		RS-485 Transceiver	1-47
15			Yes	TRI-STATE		5	RS-485	1	DS3698		RS-485 Transceiver	1-47
12	0.5/40	2.5/−20	Yes	TRI-STATE		5	RS-422	4	DS26LS31C	DS26LS31M		1-12
15	0.5/48	2/−50	Yes	TRI-STATE		5	RS-422	4	DS3487	DS3587		1-22

BALANCED RECEIVERS

Propagation Delay (ns)	Threshold Sensitivity (mV)	Common-Mode Range (V)	Hysteresis (mV)	Response Control	Strobed or TRI-STATE®	Power Supplies (V)	Standard	Circuits/ Package	Device Number Commercial 0°C to +70°C	Device Number Military −55°C to +125°C	Comments	Page No.
40	±1000	±15		Yes	Strobed	5		2	DS8820	DS7820		1-91
30	±1000	±15		Yes	Strobed	5		2	DS8820A	DS7820A		1-94
60	±200	±10	50	Yes	Strobed	5 to 15	RS-422	2	DS88C20	DS78C20	CMOS compatible	1-98
60	±200	±10	50	Yes	Strobed	5 to 15	RS-422	2	DS88C120	DS78C120	Fail-safe, CMOS compatible	1-109
50	±200	±10	50	Yes	Strobed	5	RS-422	2	DS88LS120	DS78LS120	Fail-safe	1-116
20	±500	±15		Yes	Strobed	5		2	DS75115	DS55115		1-61
17	±200	±7	100		TRI-STATE	5	RS-422	4	DS26LS32C	DS26LS32M		1-15
17	±200	±7	100		TRI-STATE	5	RS-422	4	DS26LS32AC		Fail-Safe	1-15
17	±500	±15	200		TRI-STATE	5	RS-422	4	DS26LS33C	DS26LS33M		1-15
17	±500	±15	200		TRI-STATE	5	RS-422	4	DS26LS33AC		Fail-Safe	1-15
25	±200	±10	80		TRI-STATE	5	RS-422	4	DS3486			1-18
10	±25	±3			TRI-STATE	±5		4	DS3650	DS1650		1-31
10	±25	±3			Strobed	±5		4	DS3652	DS1652		1-31
22	±200	+12, −7	70		TRI-STATE	5	RS-485	1	DS3695		RS-485 Transceiver	1-47
22	±200	+12, −7	70		TRI-STATE	5	RS-485	1	DS3696		RS-485 Transceiver	1-47
22	±200	+12, −7	70		TRI-STATE	5	RS-485	1	DS3697		RS-485 Transceiver	1-47
22	±200	+12, −7	70		TRI-STATE	5	RS-485	1	DS3698		RS-485 Transceiver	1-47
17	±25	±3			Strobed	±5		2	DS75107	DS55107		1-25
17	±10	±3			Strobed	±5		2	DS75207			1-25
17	±25	±3			Strobed	±5		2	DS75108	DS55108		1-25
17	±10	±3			Strobed	±5		2	DS75208			1-25
17	±25	±3			TRI-STATE	±5		2	DS3603	DS1603		1-25

Note. Voltage comparators (such as the LM710) have good threshold sensitivity and good common-mode range and, in turn, also make good line receivers. These comparators generally use 2 power supplies (±15V), which may not be available in some digital systems.

National Semiconductor

Transmission Line Drivers/Receivers

DS1488 Quad Line Driver

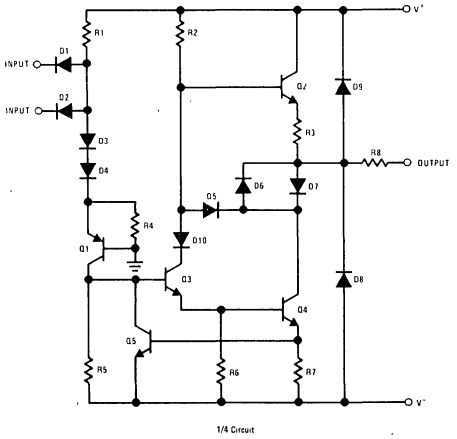
General Description

The DS1488 is a quad line driver which converts standard TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V. 24.

Features

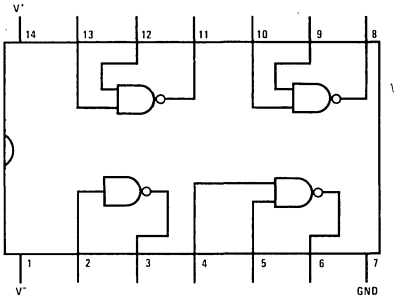
- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are TTL/LS compatible

Schematic and Connection Diagrams



1/4 Circuit

Dual-In-Line Package

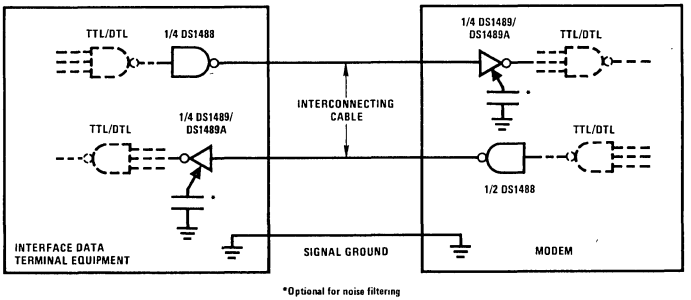


TOP VIEW

Order Number DS1488J or DS1488N
See NS Package J14A or N14A

Typical Applications

RS232C Data Transmission



*Optional for noise filtering

Absolute Maximum Ratings (Note 1)

Supply Voltage	
V^+	+15V
V^-	−15V
Input Voltage (V_{IN})	$-15V \leq V_{IN} \leq 7.0V$
Output Voltage	±15V
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1364 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 10 sec)	300°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3) $V_{CC}+ = 9V$, $V_{CC}- = -9V$ unless otherwise specified

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Logical "0" Input Current	$V_{IN} = 0V$			−1.0	−1.3	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = +5.0V$			0.005	10.0	μA
V_{OH}	High Level Output Voltage	$R_L = 3.0\ k\Omega$,	$V^+ = 9.0V$, $V^- = -9.0V$	6.0	7.0		V
		$V_{IN} = 0.8V$	$V^+ = 13.2V$, $V^- = -13.2V$	9.0	10.5		V
V_{OL}	Low Level Output Voltage	$R_L = 3.0\ k\Omega$,	$V^+ = 9.0V$, $V^- = -9.0V$		−6.8	−6.0	V
		$V_{IN} = 1.9V$	$V^+ = 13.2V$, $V^- = -13.2V$		−10.5	−9.0	V
I_{OS}^+	High Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 0.8V$		−6.0	−10.0	−12.0	mA
I_{OS}^-	Low Level Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{IN} = 1.9V$		6.0	10.0	12.0	mA
R_{OUT}	Output Resistance	$V^+ = V^- = 0V$, $V_{OUT} = \pm 2V$		300			Ω
I_{CC}^+	Positive Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V$, $V^- = -9.0V$		15.0	20.0	mA
			$V^+ = 12V$, $V^- = -12V$		19.0	25.0	mA
			$V^+ = 15V$, $V^- = -15V$		25.0	34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V$, $V^- = -9.0V$		4.5	6.0	mA
			$V^+ = 12V$, $V^- = -12V$		5.5	7.0	mA
			$V^+ = 15V$, $V^- = -15V$		8.0	12.0	mA
I_{CC}^-	Negative Supply Current (Output Open)	$V_{IN} = 1.9V$	$V^+ = 9.0V$, $V^- = -9.0V$		−13.0	−17.0	mA
			$V^+ = 12V$, $V^- = -12V$		−18.0	−23.0	mA
			$V^+ = 15V$, $V^- = -15V$		−25.0	−34.0	mA
		$V_{IN} = 0.8V$	$V^+ = 9.0V$, $V^- = -9.0V$		−0.001	−0.015	mA
			$V^+ = 12V$, $V^- = -12V$		−0.001	−0.015	mA
			$V^+ = 15V$, $V^- = -15V$		−0.01	−2.5	mA
P_d	Power Dissipation	$V^+ = 9.0V$, $V^- = -9.0V$			252	333	mW
		$V^+ = 12V$, $V^- = -12V$			444	576	mW

Switching Characteristics ($V_{CC} = 9V$, $V_{EE} = -9V$, $T_A = 25°C$)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay to a Logical "1"	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		230	350	ns
t_{pd0}	Propagation Delay to a Logical "0"	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		70	175	ns
t_r	Rise Time	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		75	100	ns
t_f	Fall Time	$R_L = 3.0\ k\Omega$, $C_L = 15\ pF$, $T_A = 25°C$		40	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1488.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Applications

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the DS1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

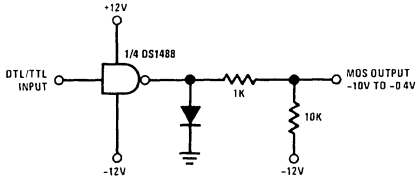
$$C = I_{SC} (\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

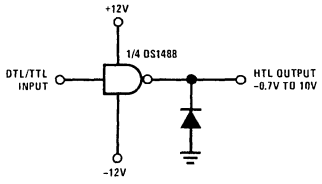
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

Typical Applications (Continued)

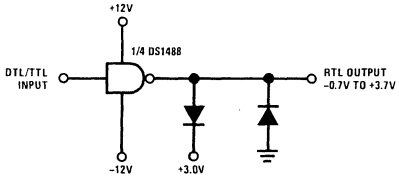
DTL/TTL-to-MOS Translator



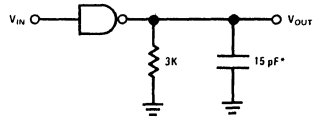
DTL/TTL-to-HTL Translator



DTL/TTL-to-RTL Translator

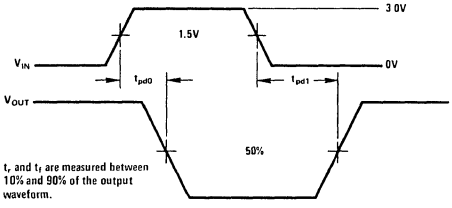


AC Load Circuit



*C_L includes probe and jig capacitance.

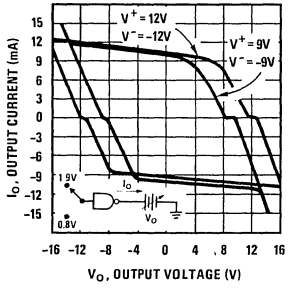
Switching Time Waveforms



t_r and t_f are measured between 10% and 90% of the output waveform.

Typical Performance Characteristics

Output Voltage and Current-Limiting Characteristics



National Semiconductor

Transmission Line Drivers/Receivers

DS1489/DS1489A Quad Line Receiver

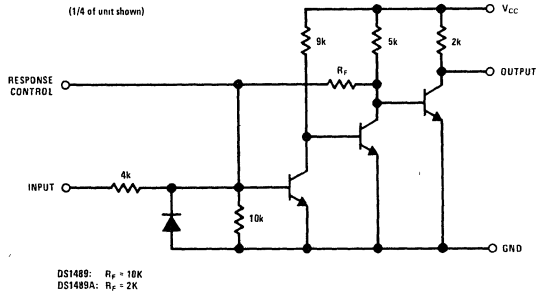
General Description

The DS1489/DS1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C. The DS1489/DS1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements.

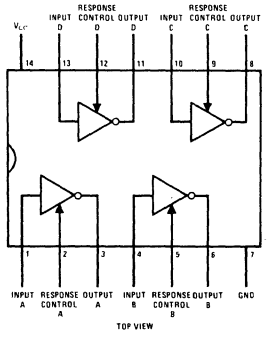
Features

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

Schematic and Connection Diagrams

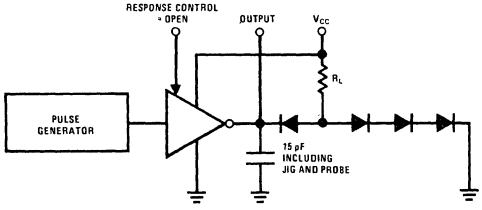


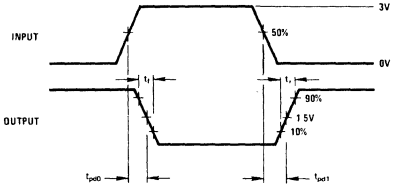
Dual-In-Line Package



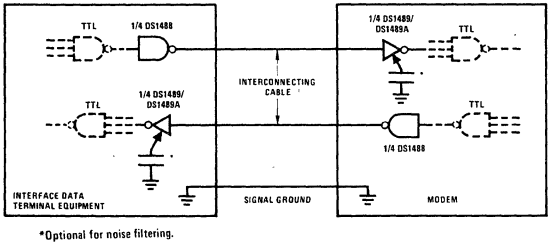
Order Number DS1489J, DS1489AJ, DS1489N or DS1489AN
See NS Package J14A or N14A

AC Test Circuit and Voltage Waveforms

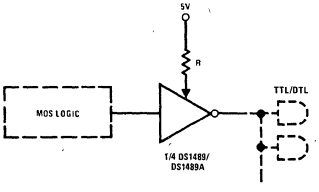




Typical Applications



RS232C Data Transmission



MOS to TTL/LS Translator

Absolute Maximum Ratings (Note 1)

The following apply for $T_A = 25°C$ unless otherwise specified.

Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20 mA
Power Dissipation (Note 2)	1W
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	-65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Electrical Characteristics (Notes 2, 3 and 4)

DS1489/DS1489A: The following apply for $V_{CC} = 5.0V \pm 1\%$, $0°C \leq T_A \leq +75°C$ unless otherwise specified.

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Input High Threshold Voltage	$V_{OUT} \leq 0.45V$, $I_{OUT} = 10$ mA	DS1489	$T_A = 25°C$	1.0	1.25	1.5	V
					0.9		1.6	V
			DS1489A	$T_A = 25°C$	1.75	2.00	2.25	V
					1.55		2.40	V
V_{TL}	Input Low Threshold Voltage	$V_{OUT} \geq 2.5V$, $I_{OUT} = -0.5$ mA		$T_A = 25°C$	0.75	1.00	1.25	V
					0.65		1.35	V
I_{IN}	Input Current	$V_{IN} = +25V$			+3.6	+5.6	+8.3	mA
		$V_{IN} = -25V$			-3.6	-5.6	-8.3	mA
		$V_{IN} = +3V$			+0.43	+0.53		mA
		$V_{IN} = -3V$			-0.43	-0.53		mA
V_{OH}	Output High Voltage	$I_{OUT} = -0.5$ mA	$V_{IN} = 0.75V$		2.6	3.8	5.0	V
			Input = Open		2.6	3.8	5.0	V
V_{OL}	Output Low Voltage	$V_{IN} = 3.0V$, $I_{OUT} = 10$ mA				0.33	0.45	V
I_{SC}	Output Short Circuit Current	$V_{IN} = 0.75V$				3.0		mA
I_{CC}	Supply Current	$V_{IN} = 5.0V$				14	26	mA
P_d	Power Dissipation	$V_{IN} = 5.0V$				70	130	mW

Switching Characteristics ($V_{CC} = 5V$, $T_A = 25°C$)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Input to Output "High" Propagation Delay	$R_L = 3.9k$, *(Figure 1)* (ac Test Circuit)		28	85	ns
t_{pd0}	Input to Output "Low" Propagation Delay	$R_L = 390\Omega$, *(Figure 1)* (ac Test Circuit)		20	50	ns
t_r	Output Rise Time	$R_L = 3.9k$, *(Figure 1)* (ac Test Circuit)		110	175	ns
t_f	Output Fall Time	$R_L = 390\Omega$, *(Figure 1)* (ac Test Circuit)		9	20	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1489 and DS1489A.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: These specifications apply for response control pin = open.

National Semiconductor

Transmission Line Drivers/Receivers

DS26LS31C/DS26LS31M Quad High Speed Differential Line Driver

General Description

The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

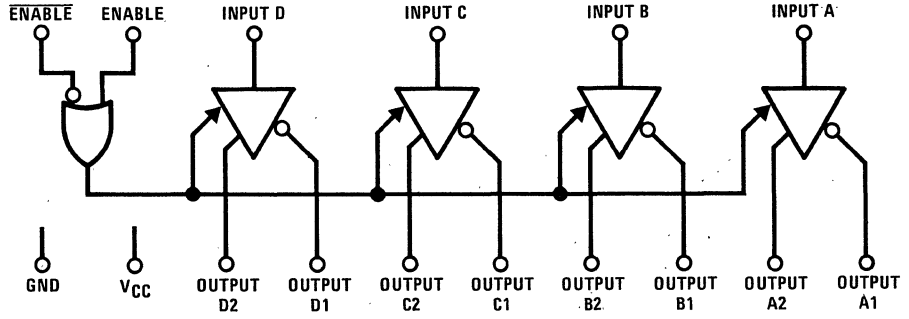
The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE® outputs and logically ANDed complementary outputs. The inputs are all LS compatible and are all one unit load.

The DS26LS31 features a power up/down protection circuit which TRI-STATEs the outputs during power up or down preventing erroneous glitches on the transmission lines.

Features

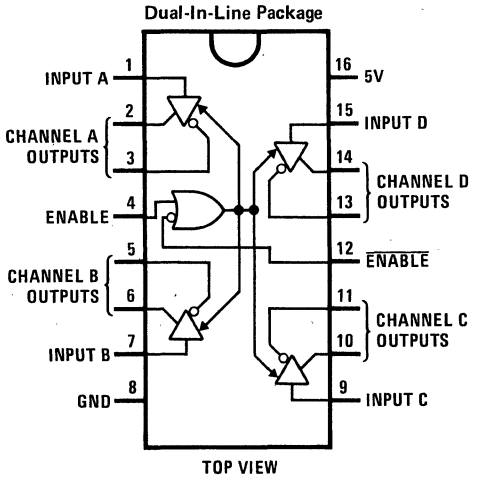
- Output skew — 2.0 ns typical
- Input to output delay — 10 ns
- Operation from single 5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when $V_{CC} = 0$
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA Standard RS-422
- Pin compatible with AM26LS31
- Available in military and commercial temperature range
- Glitch free power up/down

Logic Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS26LS31CJ, DS26LS31CN or DS26LS31MJ
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	5V
Output Voltage (Power OFF)	−0.25V to 6V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS26LS31M	4.5	5.5	V
DS26LS31	4.75	5.25	V
Temperature, T_A			
DS26LS31M	−55	+125	°C
DS26LS31	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	Output High Voltage	I_{OH} = −20 mA		2.5			V
V_{OL}	Output Low Voltage	I_{OL} = 20 mA				0.5	V
V_{IH}	Input High Voltage			2.0			V
V_{IL}	Input Low Voltage					0.8	V
I_{IL}	Input Low Current	V_{IN} = 0.4V			−40	−200	μA
I_{IH}	Input High Current	V_{IN} = 2.7V				20	μA
I_I	Input Reverse Current	V_{IN} = 7V				0.1	mA
I_O	TRI-STATE Output Current		V_O = 2.5V			20	μA
			V_O = 0.5V			−20	μA
V_{CL}	Input Clamp Voltage	I_{IN} = −18 mA				−1.5	V
I_{SC}	Output Short-Circuit Current			−30		−150	mA
I_{CC}	Power Supply Current	All Outputs Disabled or Active			35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Input to Output	C_L = 30 pF		10	15	ns
t_{PHL}	Input to Output	C_L = 30 pF		10	15	ns
Skew	Output to Output	C_L = 30 pF		2.0	6.0	ns
t_{LZ}	Enable to Output	C_L = 10 pF, S2 Open		15	35	ns
t_{HZ}	Enable to Output	C_L = 10 pF, S1 Open		15	25	ns
t_{ZL}	Enable to Output	C_L = 30 pF, S2 Open		20	30	ns
t_{ZH}	Enable to Output	C_L = 30 pF, S1 Open		20	30	ns

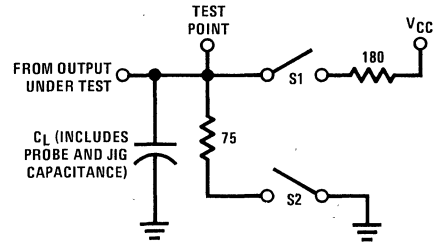
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS26LS31M and across the 0°C to +70°C range for the DS26LS31. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

AC Test Circuit and Switching Time Waveforms



Note. S1 and S2 of load circuit are closed except where shown.

FIGURE 1. AC Test Circuit

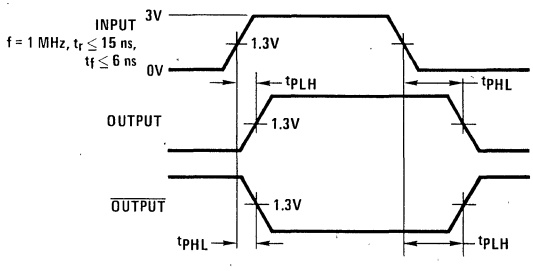


FIGURE 2. Propagation Delays

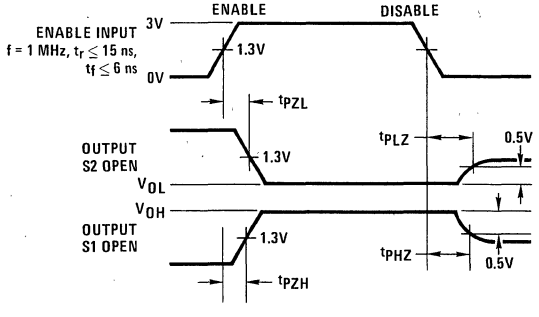
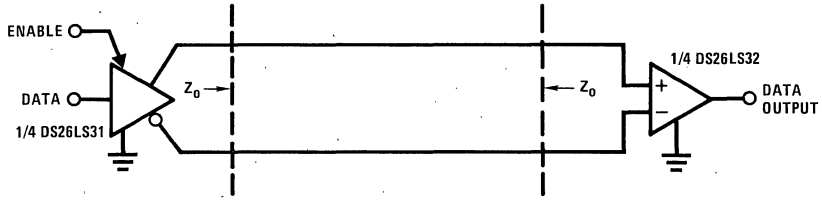


FIGURE 3. Enable and Disable Times

Typical Applications

Two-Wire Balanced System, RS-422



National Semiconductor

Transmission Line Drivers/Receivers

DS26LS32C/DS26LS32M, DS26LS32AC, DS26LS33C/DS26LS33M, DS26LS33AC Quad Differential Line Receivers

General Description

The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have an input sensitivity of 200 mV over the input voltage range of ±7V and the DS26LS33 and DS26LS33A have an input sensitivity of 500 mV over the input voltage range of ±15V.

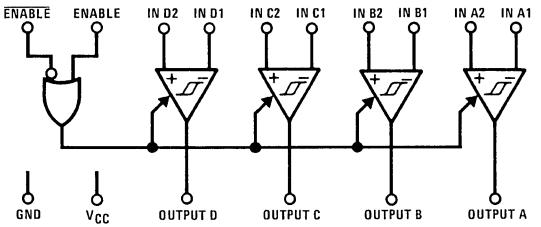
Both the DS26LS32A and DS26LS33A differ in function from the popular DS26LS32 and DS26LS33 in that input fail-safe circuitry is provided for each receiver, which causes the outputs to go to a logic "1" state when the inputs are open.

Each version provides an enable and disable function common to all four receivers and features TRI-STATE® outputs with 8 mA sink capability. Constructed using low power Schottky processing, these devices are available over the full military and commercial operating temperature ranges.

Features

- High differential or common-mode input voltage ranges of ±7V on the DS26LS32 and DS26LS32A and ±15V on the DS26LS33 and DS26LS33A
- ±0.2V sensitivity over the input voltage range on the DS26LS32 and DS26LS32A, ±0.5V sensitivity on the DS26LS33 and DS26LS33A
- Input fail-safe circuitry on the DS26LS32A and DS26LS33A
- DS26LS32 and DS26LS32A meet all requirements of RS-422 and RS-423
- 6k minimum input impedance
- 100 mV input hysteresis on the DS26LS32 and DS26LS32A, 200 mV on the DS26LS33 and DS26LS33A
- Operation from a single 5V supply
- TRI-STATE drive, with choice of complementary output enables for receiving directly onto a data bus
- Pin replacement for Advanced Micro Devices AM26LS32

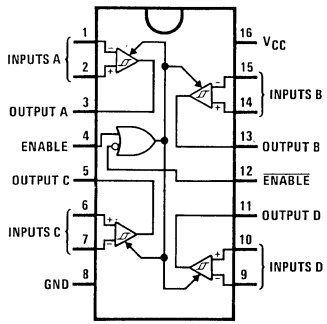
Logic Diagram



TL/F/5255-1

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5255-2

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
0	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0
		Open	1*

Hi-Z = TRI-STATE

* DS26LS32A and DS26LS33A only

Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

Order Number DS26LS32MJ, DS26LS32CJ, DS26LS32CN, DS26LS32ACJ, DS26LS32ACN, DS26LS33MJ, DS26LS33CJ, DS26LS33CN, DS26LS33ACJ or DS26LS33ACN
See NS Package J16A or N16A

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Common-Mode Range	±25V
Differential Input Voltage	±25V
Enable Voltage	7V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Storage Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DS26LS32M, DS26LS33M (MIL)	4.5	5.5	V
DS26LS32C, DS26LS33C DS26LS32AC, DS26LS33AC (COML)	4.75	5.25	V
Temperature (T_A)			
DS26LS32M, DS26LS33M (MIL)	−55	+125	°C
DS26LS32C, DS26LS33C DS26LS32AC, DS26LS33AC (COML)	0	+70	°C

Electrical Characteristics over the operating temperature range unless otherwise specified (Notes 2, 3 and 4)

	Parameter	Conditions		Min	Typ	Max	Units
V_{TH}	Differential Input Voltage	$V_{OUT} = V_{OH}$ or V_{OL}	DS26LS32, DS26LS32A, $-7V \le V_{CM} \le +7V$	−0.2	±0.07	0.2	V
			DS26LS33, DS26LS33A, $-15V \le V_{CM} \le +15V$	−0.5	±0.14	0.5	V
R_{IN}	Input Resistance	$-15V \le V_{CM} \le +15V$ (One Input AC GND)		6.0	8.5		kΩ
I_{IN}	Input Current (Under Test)	$V_{IN} = 15V$, Other Input $-15V \le V_{IN} \le +15V$				2.3	mA
		$V_{IN} = -15V$, Other Input $-15V \le V_{IN} \le +15V$				−2.8	mA
V_{OH}	Output High Voltage	V_{CC} = Min, $\Delta V_{IN} = 1V$, $V_{\overline{ENABLE}} = 0.8V$, $I_{OH} = -440\ \mu A$	Commercial	2.7	4.2		V
			Military	2.5	4.2		V
V_{OL}	Output Low Voltage	V_{CC} = Min, $\Delta V_{IN} = -1V$, $V_{\overline{ENABLE}} = 0.8V$	$I_{OL} = 4$ mA			0.4	V
			$I_{OL} = 8$ mA			0.45	V
V_{IL}	Enable Low Voltage					0.8	V
V_{IH}	Enable High Voltage			2.0			V
V_I	Enable Clamp Voltage	V_{CC} = Min, $I_{IN} = -18$ mA				−1.5	V
I_O	OFF-State (High Impedance) Output Current	V_{CC} = Max	$V_O = 2.4V$			20	μA
			$V_O = 0.4V$			−20	μA
I_{IL}	Enable Low Current	$V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Enable High Current	$V_{IN} = 2.7V$				20	μA
I_{SC}	Output Short-Circuit Current	$V_O = 0V$, V_{CC} = Max, $\Delta V_{IN} = 1V$		−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = Max, All V_{IN} = GND, Outputs Disabled	DS26LS32, DS26LS32A		52	70	mA
			DS26LS33, DS26LS33A		57	80	mA
I_I	Input High Current	$V_{IN} = 5.5V$				100	μA
V_{HYST}	Input Hysteresis	$T_A = 25°C$, $V_{CC} = 5V$, $V_{CM} = 0V$	DS26LS32, DS26LS32A		100		mV
			DS26LS33, DS26LS33A		200		mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 3: All typical values are $V_{CC} = 5V$, $T_A = 25°C$.

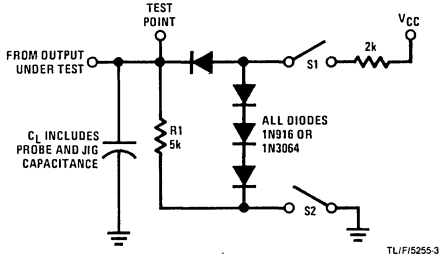
Note 4: Only one output at a time should be shorted.

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

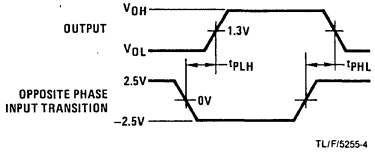
Parameter		Conditions	DS26LS32/DS26LS33			DS26LS32A/DS26LS33A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Input to Output	$C_L = 15$ pF		17	25		23	35	ns
t_{PHL}				17	25		23	35	ns
t_{LZ}	ENABLE to Output	$C_L = 5$ pF		20	30		15	22	ns
t_{HZ}				15	22		20	25	ns
t_{ZL}	ENABLE to Output	$C_L = 15$ pF		15	22		14	22	ns
t_{ZH}				15	22		15	22	ns

AC Test Circuit and Switching Time Waveforms

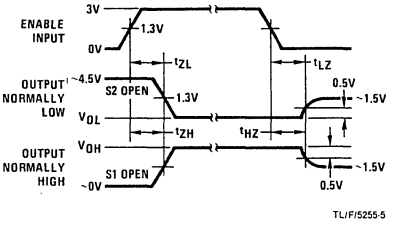
Load Test Circuit for TRI-STATE Outputs



Propagation Delay (Notes 1 and 3)



Enable and Disable Times (Notes 2 and 3)



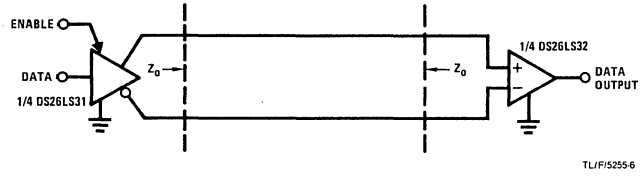
Note 1: Diagram shown for $\overline{\text{ENABLE}}$ low.

Note 2: S1 and S2 of load circuit are closed except where shown.

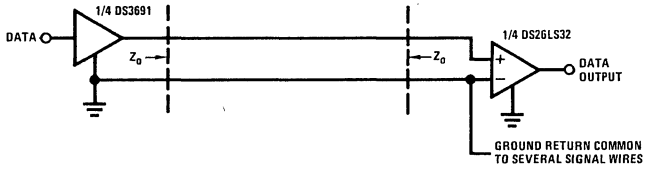
Note 3: Pulse generator for all pulses: Rate ≤ 1.0 MHz; $Z_O = 50\Omega$; $t_r \leq 15$ ns; $t_f \leq 6.0$ ns.

Typical Applications

Two-Wire Balanced Systems, RS-422



Single Wire with Common Ground Unbalanced Systems, RS-423



National Semiconductor

Transmission Line Drivers/Receivers

DS3486 Quad RS-422, RS-423 Line Receiver

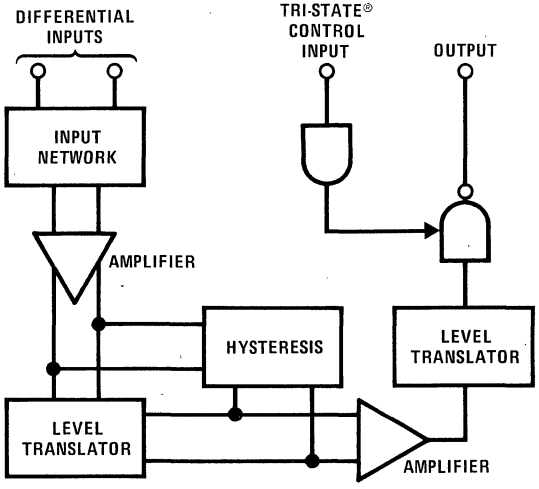
General Description

National's quad RS-422, RS-423 receiver features four independent receiver chains which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible, TRI-STATE® structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver chain has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

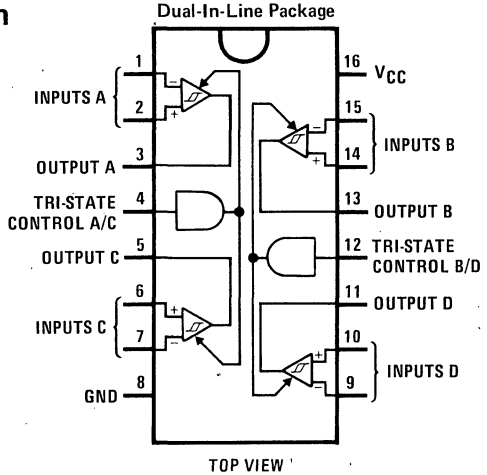
Features

- Four independent receiver chains
- TRI-STATE outputs
- High impedance output control inputs (PIA compatible)
- Internal hysteresis — 140 mV (typ)
- Fast propagation times — 18 ns (typ)
- TTL compatible
- Single 5V supply voltage
- Pin compatible and interchangeable with MC3486

Block Diagram



Connection Diagram



TOP VIEW

Order Number DS3486J or DS3486N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Power Supply Voltage, V_{CC}	8 V
Input Common-Mode Voltage, V_{ICM}	±25 V
Input Differential Voltage, V_{ID}	±25 V
TRI-STATE Control Input Voltage, V_I	8 V
Output Sink Current, I_O	50 mA
Storage Temperature, T_{STG}	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Power Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A	0	70	°C
Input Common-Mode Voltage Range, V_{ICR}	−7.0	7.0	V

Electrical Characteristics

(Unless otherwise noted, minimum and maximum limits apply over recommended temperature and power supply voltage ranges. Typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{IC} = 0V$. See Note 2.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Input Voltage — High Logic State (TRI-STATE Control)		2.0			V
V_{IL}	Input Voltage — Low Logic State (TRI-STATE Control)				0.8	V
$V_{TH(D)}$	Differential Input Threshold Voltage	$-7V \leq V_{IC} \leq 7V$, V_{IH} TRI-STATE = 2V				
		$I_O = 0.4$ mA, $V_{OH} \geq 2.7V$		0.070	0.2	V
		$I_O = 8$ mA, $V_{OL} \geq 0.5V$		0.070	−0.2	V
$I_{IB(D)}$	Input Bias Current	$V_{CC} = 0V$ or 5.25V, Other Inputs at 0V				
		$V_I = -10V$			−3.25	mA
		$V_I = -3V$			−1.50	mA
		$V_I = 3V$			1.50	mA
		$V_I = 10V$			3.25	mA
	Input Balance	$-7V \leq V_{IC} \leq 7V$, $V_{IH(3C)} = 2V$, (Note 4)				
		$I_O = 0.4$ mA, $V_{ID} = 0.4V$	2.7			V
		$I_O = 8$ mA, $V_{ID} = -0.4V$			0.5	V
I_{OZ}	Output TRI-STATE Leakage Current	$V_{I(D)} = 3V$, $V_{IL} = 0.8V$, $V_{OL} = 0.5V$			−40	μA
		$V_{I(D)} = -3V$, $V_{IL} = 0.8V$, $V_{OH} = 2.7V$			40	μA
I_{OS}	Output Short-Circuit Current	$V_{I(D)} = 3V$, V_{IH} TRI-STATE = 2V, $V_O \approx 0$, (Note 3)	−15		−100	mA
I_{IL}	Input Current — Low Logic State (TRI-STATE Control)	$V_{IL} = 0.5V$			−100	μA
I_{IH}	Input Current — High Logic State (TRI-STATE Control)	$V_{IH} = 2.7V$			20	μA
		$V_{IL} = 5.25V$			100	μA
V_{IC}	Input Clamp Diode Voltage (TRI-STATE Control)	$I_{IN} = -10$ mA			−1.5	V
I_{CC}	Power Supply Current	All Inputs $V_{IL} = 0V$			85	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, out of device pins are negative. All voltages referenced to ground unless otherwise noted.

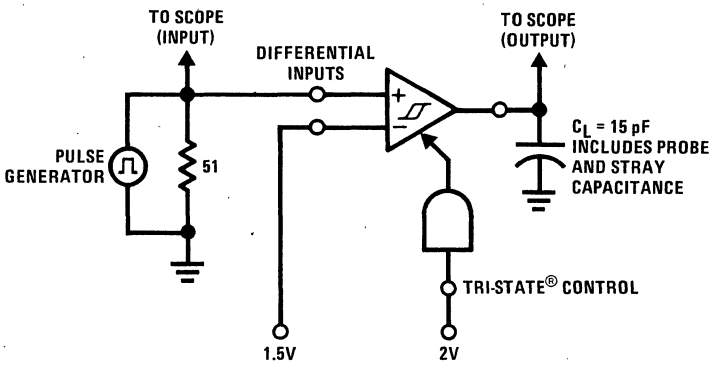
Note 3: Only one output at a time should be shorted.

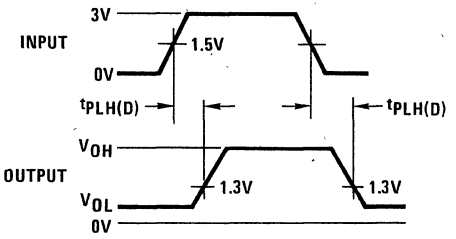
Note 4: Refer to EIA RS-422/3 for exact conditions.

Switching Characteristics (Unless otherwise noted, V_{CC} = 5V and T_A = 25°C.)

	PARAMETER	MIN	TYP	MAX	UNITS
	Propagation Delay Time — Differential Inputs to Output				
$t_{PHL(D)}$	Output High to Low		19	35	ns
$t_{PLH(D)}$	Output Low to High		19	30	ns
	Propagation Delay Time — TRI-STATE Control to Output				
t_{PLZ}	Output Low to TRI-STATE		23	35	ns
t_{PHZ}	Output High to TRI-STATE		25	35	ns
t_{PZH}	Output TRI-STATE to High		18	30	ns
t_{PZL}	Output TRI-STATE to Low		20	30	ns

AC Test Circuits and Switching Time Waveforms

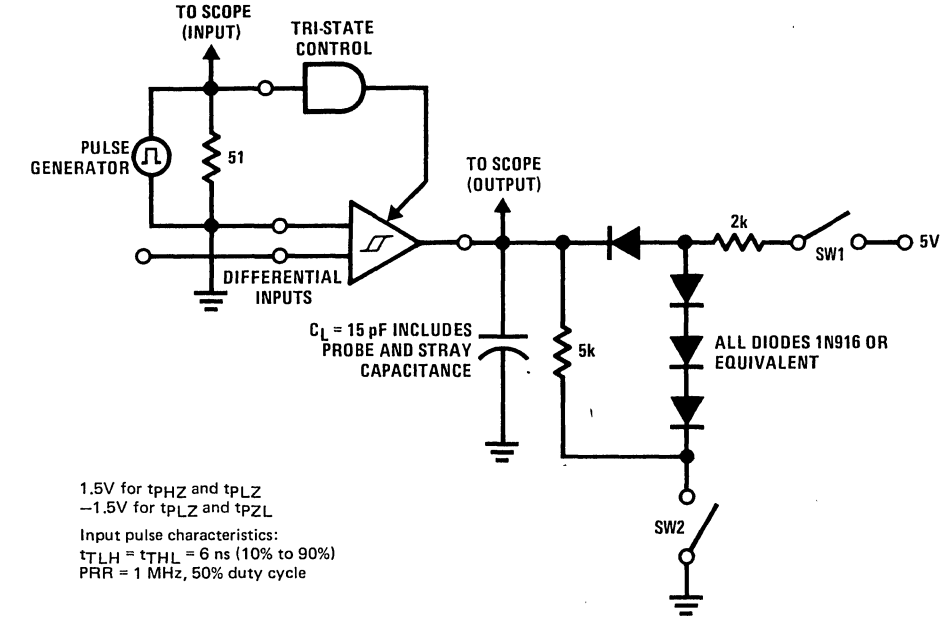




Input pulse characteristics:
$t_{TLH} = t_{THL}$ = 6 ns (10% to 90%)
PRR = 1 MHz, 50% duty cycle

FIGURE 1. Propagation Delay Differential Input to Output

AC Test Circuits and Switching Time Waveforms (Continued)



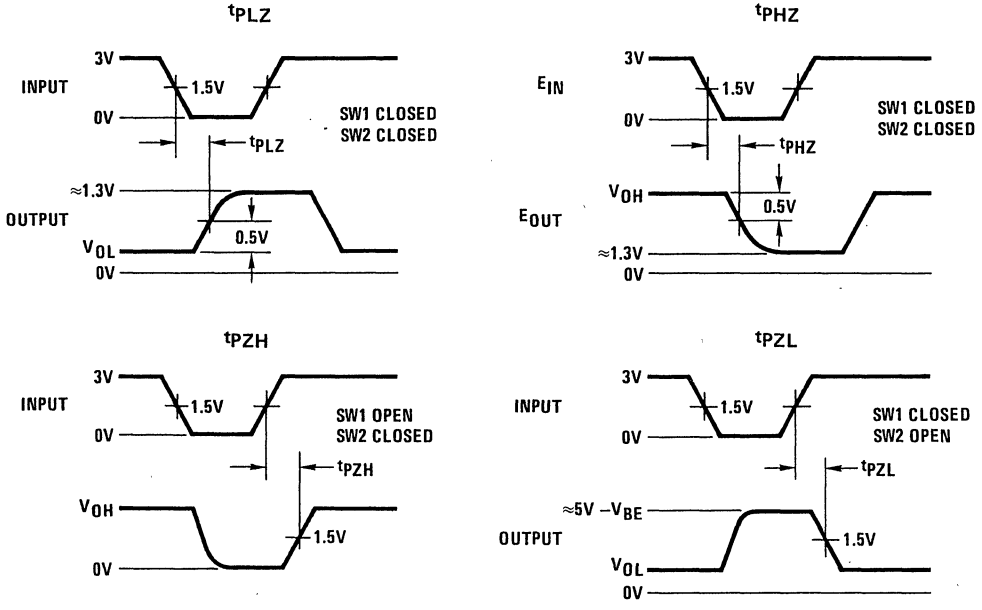


FIGURE 2. Propagation Delay TRI-STATE Control Input to Output

National Semiconductor

Transmission Line Drivers/Receivers

DS3587/DS3487 Quad TRI-STATE® Line Driver

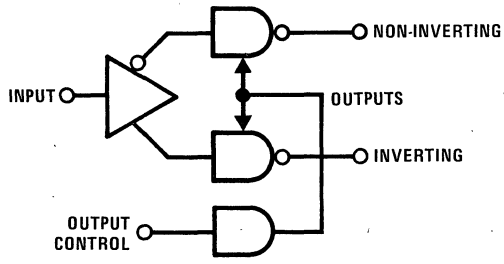
General Description

National's quad RS-422 driver features four independent driver chains which comply with EIA Standards for the electrical characteristics of balanced voltage digital interface circuits. The outputs are TRI-STATE® structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs. In addition, internal circuitry assures a high impedance output state during the transition between power up and power down.

Features

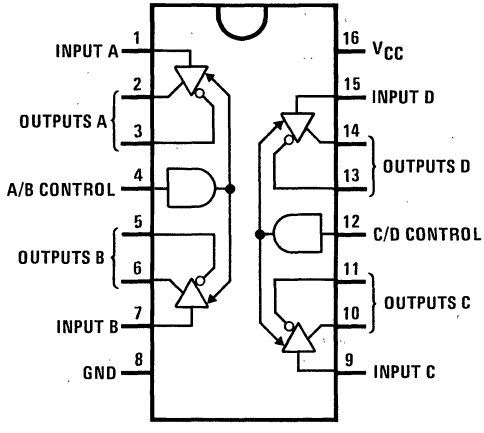
- Four independent driver chains
- TRI-STATE outputs
- PNP high impedance inputs (PIA compatible)
- Power up/down protection
- Fast propagation times (typ 10 ns)
- TTL compatible
- Single 5V supply voltage
- Output rise and fall times less than 20 ns (typ 10 ns)
- Pin compatible with MC3487
- Output skew – 2 ns typ

Block Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS3587J, DS3487J or DS3487N
See NS Package J16A or N16A

Truth Table

INPUT	CONTROL INPUT	NON-INVERTER OUTPUT	INVERTER OUTPUT
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high impedance)

Absolute Maximum Ratings (Note 1)

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS3587	4.5	5.5	V
DS3487	4.75	5.25	V
Temperature (T_A)			
DS3587	−55	+125	°C
DS3487	0	70	°C

Electrical Characteristics (Notes 2, 3, 4 and 5)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage					0.8	V
V_{IH}	Input High Voltage			2.0			V
I_{IL}	Input Low Current	V_{IL} = 0.5V				−200	μA
I_{IH}	Input High Current		V_{IH} = 2.7V			50	μA
			V_{IH} = 5.5V			100	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA				−1.5	V
V_{OL}	Output Low Voltage	I_{OL} = 48 mA				0.5	V
V_{OH}	Output High Voltage	I_{OH} = −20 mA		2.5			V
I_{OS}	Output Short-Circuit Current			−40		−140	mA
I_{OZ}	Output Leakage Current (TRI-STATE)		V_O = 0.5V			−100	μA
			V_O = 5.5V			100	μA
I_{OFF}	Output Leakage Current Power OFF	V_{CC} = 0	V_O = 6V			100	μA
			V_O = −0.25V			−100	μA
$\lvert V_{OS} - \bar{V}_{OS} \rvert$	Difference in Output Offset Voltage					0.4	V
V_T	Differential Output Voltage			2.0			V
$\lvert V_T \rvert - \lvert \bar{V}_T \rvert$	Difference in Differential Output Voltage					0.4	V
I_{CC}	Power Supply Current		Active		50	80	mA
			TRI-STATE		35	60	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Input to Output			10	15	ns
t_{PLH}	Input to Output			10	15	ns
t_{THL}	Differential Fall Time			10	15	ns
t_{TLH}	Differential Rise Time			10	15	ns
t_{PHZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		17	25	ns
t_{PLZ}	Enable to Output	R_L = 200Ω, C_L = 50 pF		15	25	ns
t_{PZH}	Enable to Output	R_L = ∞, C_L = 50 pF, S1 Open		11	25	ns
t_{PZL}	Enable to Output	R_L = 200Ω, C_L = 50 pF, S2 Open		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

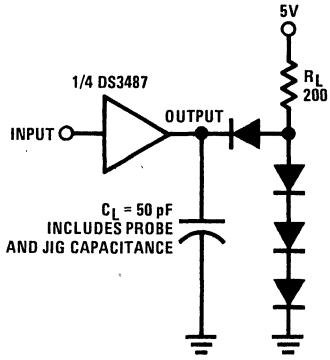
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS3487. All typicals are given for V_{CC} = 5V and T_A = 25°C.

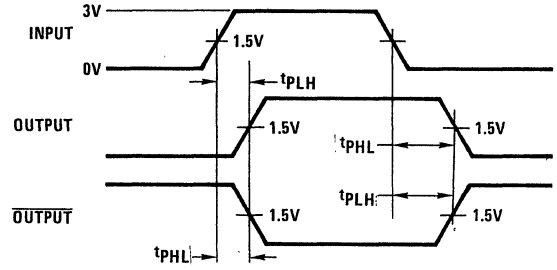
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422, where applicable.

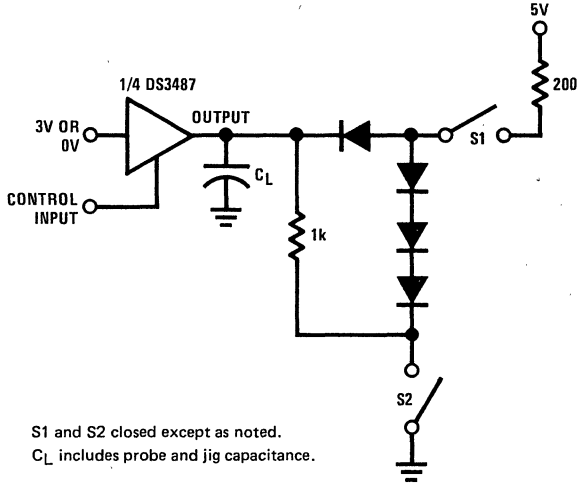
AC Test Circuits and Switching Time Waveforms



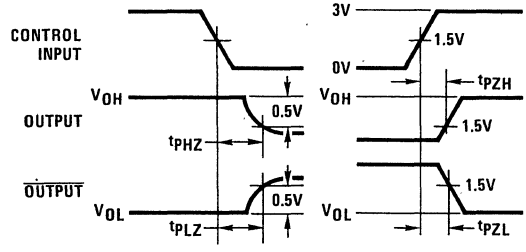


Input pulse: f = 1 MHz, 50%; $t_r = t_f \leq 15$ ns.

FIGURE 1. Propagation Delays



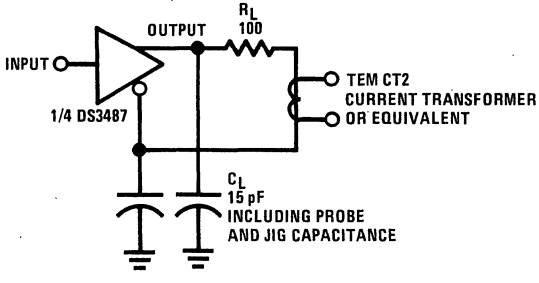
S1 and S2 closed except as noted.
C_L includes probe and jig capacitance.

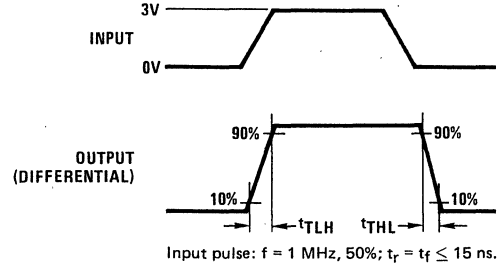


Input pulse: f = 1 MHz, 50%; $t_r = t_f \leq 15$ ns.

S1 = open for t_{PZH}
S2 = open for t_{PZL}

FIGURE 2. TRI-STATE Enable and Disable Delays





Input pulse: f = 1 MHz, 50%; $t_r = t_f \leq 15$ ns.

FIGURE 3. Differential Rise and Fall Times

National Semiconductor

Transmission Line Drivers/Receivers

DS1603/DS3603, DS55107/DS75107, DS55108/DS75108, DS75207, DS75208 Dual Line Receivers

General Description

The eight products described herein are TTL compatible dual high speed circuits intended for sensing in a broad range of system applications. While the primary usage will be for line receivers or MOS sensing, any of the products may effectively be used as voltage comparators, level translators, window detectors, transducer preamplifiers, and in other sensing applications. As digital line receivers the products are applicable with the SN55109/SN75109 and SN55110/SN75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems. The improved input sensitivity and delay specifications of the DS75207 and DS75208 make them ideal for sensing high performance MOS memories as well as high sensitivity line receivers and voltage comparators. TRI-STATE® products enhance bused organizations.

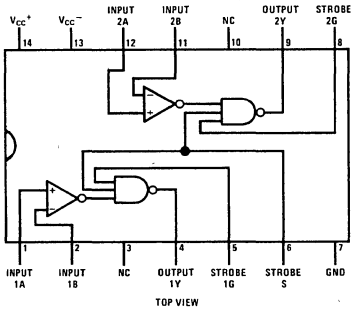
Input protection diodes are incorporated in series with the collectors of the differential input stage. These diodes are useful in certain applications that have multiple $V_{CC}+$ supplies or $V_{CC}+$ supplies that are turned off.

Features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±10 mV or ±25 mV input sensitivity
- ±3V input common-mode range
- High input impedance with normal V_{CC}, or $V_{CC} = 0V$
- Strobes for channel selection
- TRI-STATE outputs for high speed buses
- Dual circuits
- Sensitivity gntd. over full common-mode range
- Logic input clamp diodes—meets both "A" and "B" version specifications
- ±5V standard supply voltages

Connection Diagrams

Dual-In-Line Package

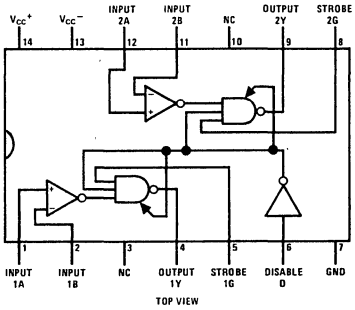


TOP VIEW

Order Number DS55107J, DS75107J, DS55108J, DS75108J, DS75207J or DS75208J
See NS Package J14A

Order Number DS75107N, DS75108N, DS75207N or DS75208N
See NS Package N14A

Dual-In-Line Package



TOP VIEW

Order Number DS1603J or DS3603J
See NS Package J14A

Order Number DS3603N
See NS Package N14A

Product Selection Guide

TEMPERATURE→ / PACKAGE→	−55°C ≤ T_A ≤ +125°C CAVITY DIP	0°C ≤ T_A ≤ +70°C CAVITY OR MOLDED DIP	
INPUT SENSITIVITY→ / OUTPUT LOGIC↓	±25 mV	±25 mV	±10 mV
TTL Active Pull-up	DS55107	DS75107	DS75207
TTL Open Collector	DS55108	DS75108	DS75208
TTL TRI-STATE	DS1603	DS3603	DS3604

Absolute Maximum Ratings (Notes 1, 2 and 3)

Supply Voltage, V_{CC}^+	7V
Supply Voltage, V_{CC}^-	−7V
Differential Input Voltage	±6V
Common Mode Input Voltage	±5V
Strobe Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C

Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 10 sec)	300°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	DS55107, DS55108, DS1603			DS75107, DS75207 DS75108, DS75208 DS3603		
	MIN	NOM	MAX	MIN	NOM	MAX
Supply Voltage V_{CC}^+	4.5V	5V	5.5V	4.75V	5V	5.25V
Supply Voltage V_{CC}^-	−4.5V	−5V	−5.5V	−4.75V	−5V	−5.25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

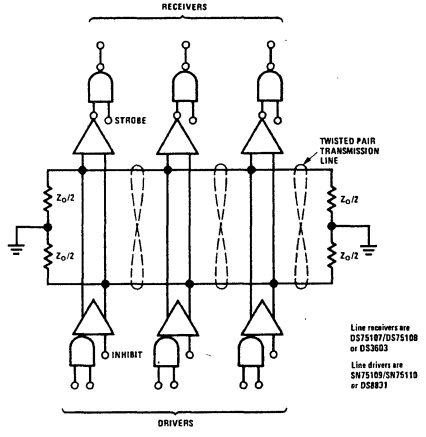
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1603, DS55107 and DS55108 and across the 0°C to +70°C range for the DS3603, DS75107, DS75108. All typical values are for T_A = 25°C and V_{CC} = 5V.

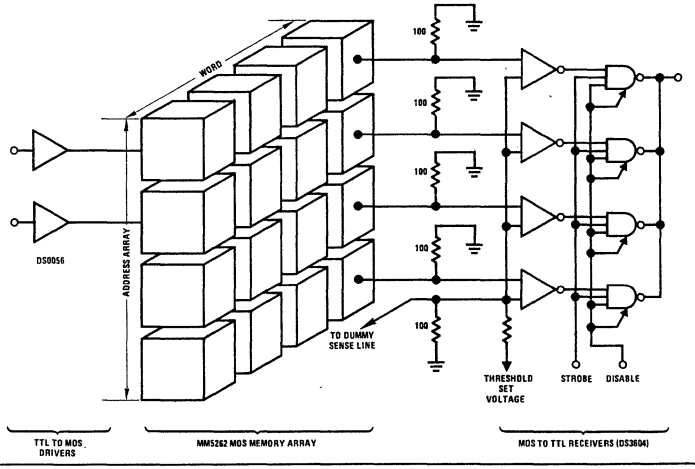
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Applications

Line Receiver Used in a Party-Line or Data-Bus System

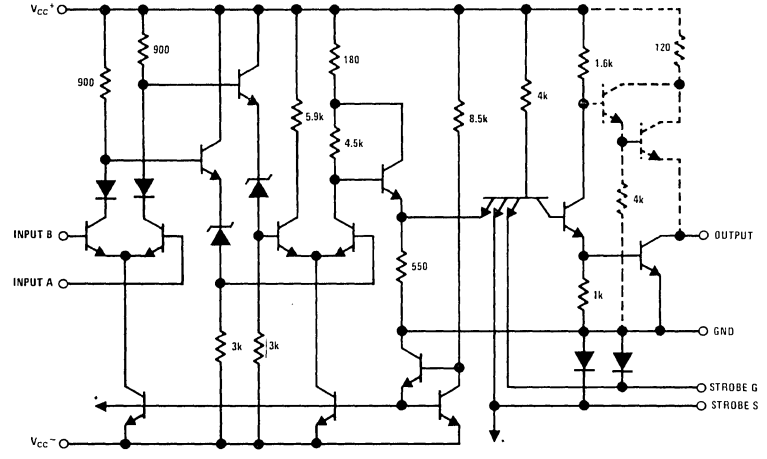


Line Receiver Used in MOS Memory System



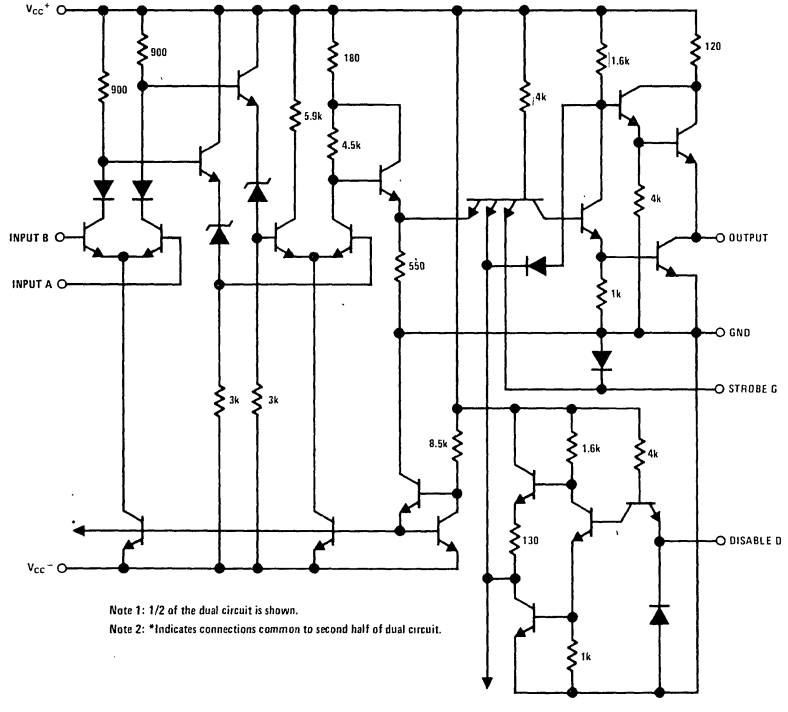
Schematic Diagrams

DS55107/DS75107, DS75207
DS55108/DS75108, DS75208



Note 1: 1/2 of the dual circuit is shown.
Note 2: *Indicates connections common to second half of dual circuit.
Note 3: Components shown with dash lines are applicable to the DS55107, DS75107 and DS75207 only.

DS1603/DS3603



Note 1: 1/2 of the dual circuit is shown.
Note 2: *Indicates connections common to second half of dual circuit.

DS55107/DS75107, DS55108/DS75108

Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			80	μA
			$V_{IH(S)}$ = Max V_{CC+}			2	mA
I_{IL}	Low Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −400μA, V_{ID} = 25 mV, V_{IC} = −3V to 3V, (Note 3)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	V_{CC+} = Min, V_{CC-} = Min V_{OH} = Max V_{CC+}, (Note 4)				250	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, V_{CC-} = Max, (Notes 2 and 3)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			18	30	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output	R_L = 390Ω, C_L = 50 pF	(Note 3)		10	15	ns
			(Note 4)		13	20	ns
$t_{PHL(S)}$	Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output	R_L = 390Ω, C_L = 50 pF	(Note 3)		8	15	ns
			(Note 4)		13	20	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.
Note 2: Only one output at a time should be shorted.
Note 3: DS55107/DS75107 only.
Note 4: DS55108/DS75108 only.

DS75207, DS75208

Electrical Characteristics ($0°C \leq T_A \leq +70°C$)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1 or G2	V_{CC+} = Max,	$V_{IH(S)}$ = 2.4V			40	μA
		V_{CC-} = Max	$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current Into S	V_{CC+} = Max,	$V_{IH(S)}$ = 2.4V			80	μA
		V_{CC-} = Max	$V_{IH(S)}$ = Max V_{CC+}			2	mA
I_{IL}	Low Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −400μA, V_{ID} = 10 mV, V_{IC} = −3V to 3V, (Note 3)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	V_{CC+} = Min, V_{CC-} = Min, V_{OH} = Max V_{CC+}, (Note 4)				250	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, V_{CC-} = Max (Notes 2, 3 and 4)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			18	30	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			35	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			20	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, From Strobe Input G or S to Output	R_L = 470Ω, C_L = 15 pF			17	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, From Strobe Input G or S to Output	R_L = 470Ω, C_L = 15 pF			17	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.
Note 2: Only one output at a time should be shorted.
Note 3: DS75207 only.
Note 4: DS75208 only.

DS1603/DS3603

Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1, G2 or D	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into D	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(D)}$ = 0.4V				−1.6	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(G)}$ = 0.4V	$V_{IH(D)}$ = 2V			−40	μA
			$V_{IL(D)}$ = 0.8V			−1.6	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −2 mA, V_{ID} = 25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V				0.4	V
I_{OD}	Output Disable Current	V_{CC+} = Max, V_{CC-} = Max, $V_{IH(D)}$ = 2V	V_{OUT} = 2.4V			40	μA
			V_{OUT} = 0.4V			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, $V_{IL(D)}$ = 0.8V, V_{CC-} = Max, (Note 2)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC+}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			28	40	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC-}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or D	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

Switching Characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)		17	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)		17	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, From Strobe Input G to Output	R_L = 390Ω, C_L = 50 pF		10	15	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, From Strobe Input G to Output	R_L = 390Ω, C_L = 50 pF		8	15	ns
t_{1H}	Disable Low-to-High to Output High to Off	R_L = 390Ω, C_L = 5 pF			20	ns
t_{0H}	Disable Low-to-High to Output Low to Off	R_L = 390Ω, C_L = 5 pF			30	ns
t_{H1}	Disable High-to-Low to Output Off to High	R_L = 1k to 0V, C_L = 50 pF			25	ns
t_{H0}	Disable High-to-Low to Output Off to Low	R_L = 390Ω, C_L = 50 pF			25	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.

Note 2: Only one output at a time should be shorted.

National Semiconductor

Transmission Line Drivers/Receivers

DS1650/DS3650, DS1652/DS3652 Quad Differential Line Receivers

General Description

The DS1650/DS3650 and DS1652/DS3652 are TTL compatible quad high speed circuits intended primarily for line receiver applications. Switching speeds have been enhanced over conventional line receivers by the use of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bussed organizations.

The DS1650/DS3650 has active pull-up outputs and offers a TRI-STATE strobe, while the DS1652/DS3652 offers open collector outputs providing implied "AND" operation.

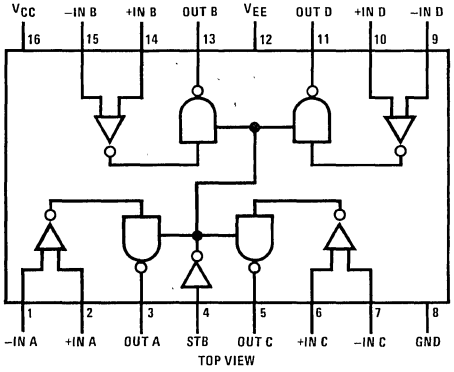
The DS1652/DS3652 can be used for address decoding as illustrated below. All outputs of the DS1652/DS3652 are tied together through a common resistor to 5V. In this configuration the DS1652/DS3652 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

Features

- High speed
- TTL compatible
- Input sensitivity ±25 mV
- TRI-STATE outputs for high speed busses
- Standard supply voltages ±5V
- Pin and function compatible with MC3450 and MC3452

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS1650J, DS1652J, DS3650J, DS3652J, DS3650N or DS3652N
See NS Package J16A or N16A

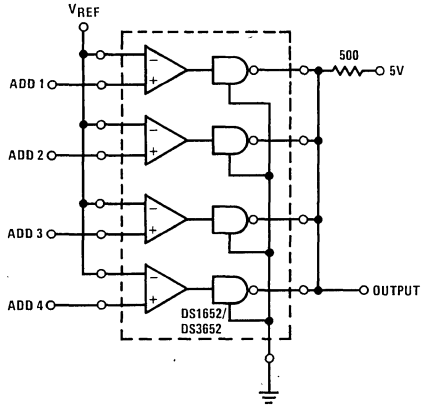
Truth Table

INPUT	STROBE	OUTPUT DS1650/ DS3650	OUTPUT DS1652/ DS3652
$V_{ID} \geq 25$ mV	L	H	Open
	H	Open	Open
-25 mV $\leq V_{ID} \leq 25$ mV	L	X	X
	H	Open	Open
$V_{ID} \leq -25$ mV	L	L	L
	H	Open	Open

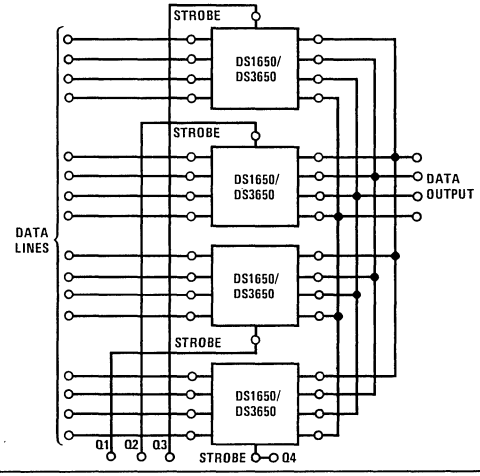
L = Low Logic State Open = TRI-STATE
H = High Logic State X = Indeterminate State

Typical Applications

Implied "AND" Gating



Wired "OR" Data Selecting Using TRI-STATE Logic



Absolute Maximum Ratings (Note 1)

Power Supply Voltages	
V_{CC}	+7.0 V_{DC}
V_{EE}	−7.0 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6.0 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5.0 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1650, DS1652	4.5	5.5	V_{DC}
DS3650, DS3652	4.75	5.25	V_{DC}
Supply Voltage, V_{EE}			
DS1650, DS1652	−4.5	−5.5	V_{DC}
DS3650, DS3652	−4.75	−5.25	V_{DC}
Operating Temperature, T_A			
DS1650, DS1652	−55	+125	°C
DS3650, DS3652	0	+70	°C
Output Load Current, I_{OL}		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	−5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	−3.0	+3.0	V_{DC}
Input Voltage Range (Any Input to GND), V_{IR}	−5.0	+3.0	V_{DC}

Electrical Characteristics

(V_{CC} = 5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted) (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range = −3V ≤ V_{IN} ≤ 3V)	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max				±25.0	mV
$I_{IH(I)}$	High Level Input Current to Receiver Input	*(Figure 5)*				75	µA
$I_{IL(I)}$	Low Level Input Current to Receiver Input	*(Figure 6)*				−10	µA
$I_{IH(S)}$	High Level Input Current to Strobe Input	*(Figure 3)*	$V_{IH(S)}$ = 2.4V, DS1650, DS1652			100	µA
			$V_{IH(S)}$ = 2.4V, DS3650, DS3652			40	µA
			$V_{IH(S)}$ = V_{CC}			1	mA
$I_{IL(S)}$	Low Level Input Current to Strobe Input		$V_{IH(S)}$ = 0.4V			−1.6	mA
V_{OH}	High Level Output Voltage	*(Figure 1)*	DS1650, DS3650	2.4			V_{DC}
I_{CEX}	High Level Output Leakage Current		DS1652, DS3652			250	µA
V_{OL}	Low Level Output Voltage	*(Figure 1)*	DS3650, DS3652			0.45	V_{DC}
			DS1650, DS1652			0.50	
I_{OS}	Short-Circuit Output Current (Note 4)	*(Figure 4)*	DS1650/DS3650	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	*(Figure 7)*	DS1650			100	µA
			DS3650			40	µA
I_{CCH}	High Logic Level Supply Current from V_{CC}	*(Figure 2)*			45	60	mA
I_{EEH}	High Logic Level Supply Current from V_{EE}	*(Figure 2)*			−17	−30	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS3650, DS3652 and the −55°C to +125°C range for the DS1650, DS1652. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{EE} = −5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

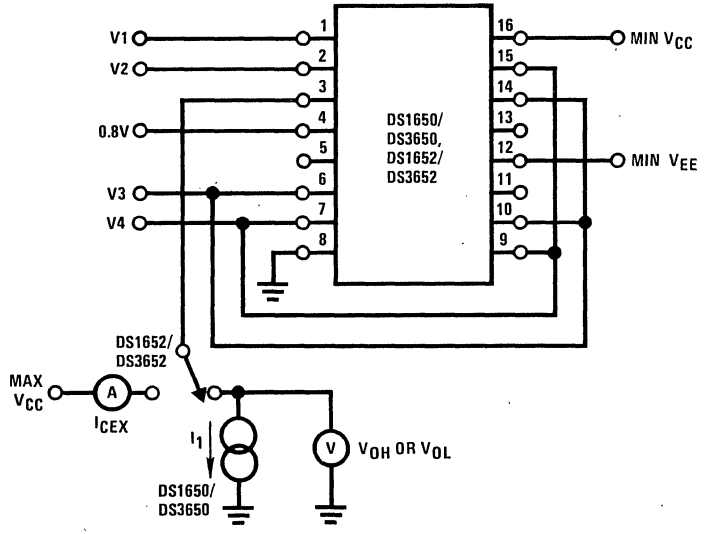
Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with line receivers is, what is the minimum differential input voltage required as the receiver input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1650, DS1652 and the DS3650, DS3652 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

Switching Characteristics (V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, T_A = 25°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	*(Figure 8)*	DS1650/DS3650		21	25	ns
			DS1652/DS3652		20	25	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)		DS1650/DS3650		20	25	ns
			DS1652/DS3652		22	25	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	*(Figure 9)*	DS1650/DS3650		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS1650/DS3650		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)		DS1650/DS3650		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS1650/DS3650		14	29	ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	*(Figure 10)*	DS1652/DS3652		16	25	ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)		DS1652/DS3652		13	25	ns

Electrical Characteristic Test Circuits



	V1		V2		V3		V4		I_1
	DS1650/ DS3650	DS1652/ DS3652	DS1650/ DS3650	DS1652/ DS1652	DS1650/ DS1650	DS1652/ DS1652	DS1650/ DS1650	DS1652/ DS1652	
V_{OH}	+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V		+0.4 mA +0.4 mA
I_{CEX}		+2.975V −3.0V		+3.0V −2.975V		+3.0V GND		GND −3.0V	
V_{OL}	+3.0V −2.975V	+3.0V −2.975V	+2.975V −3.0V	+2.975V −3.0V	GND −3.0V	GND −3.0V	+3.0V GND	+3.0V GND	−16 mA −16 mA

Channel A shown under test. Other channels are tested similarly.

FIGURE 1. I_{CEX}, V_{OH} and V_{OL}

Electrical Characteristic Test Circuits (Continued)

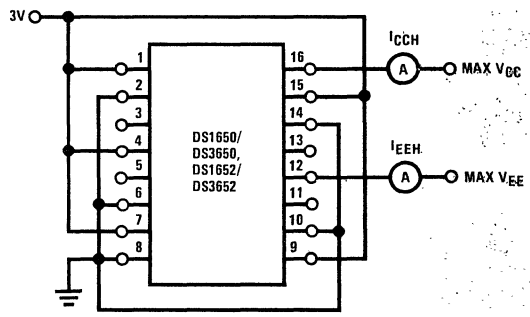


FIGURE 2. I_{CCH} and I_{EEH}

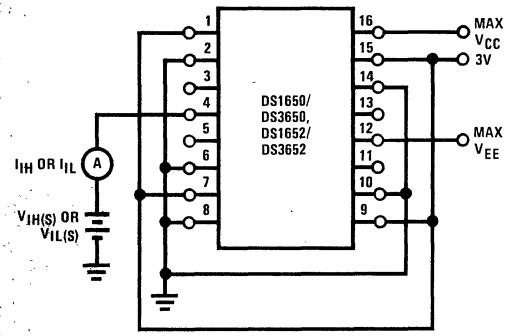
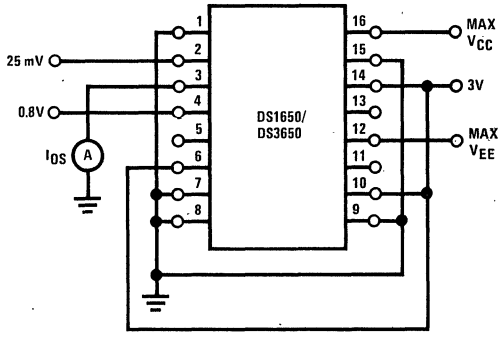
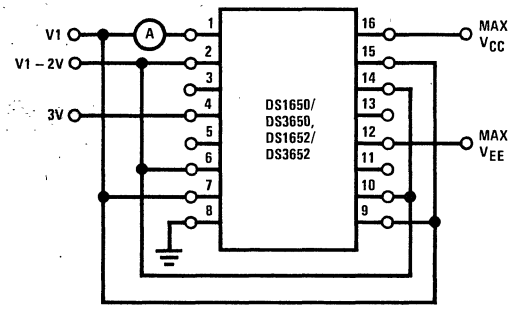


FIGURE 3. $I_{IH(S)}$ and $I_{IL(S)}$



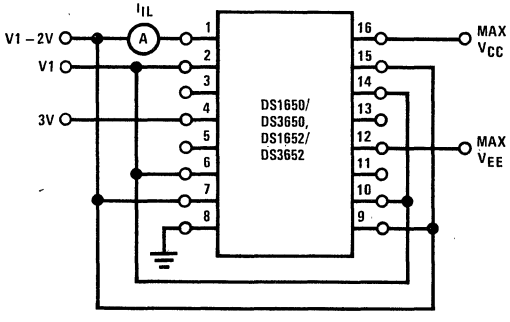
Note. Channel A shown under test, other channels are tested similarly. Only one output shorted at a time.

FIGURE 4. I_{OS}



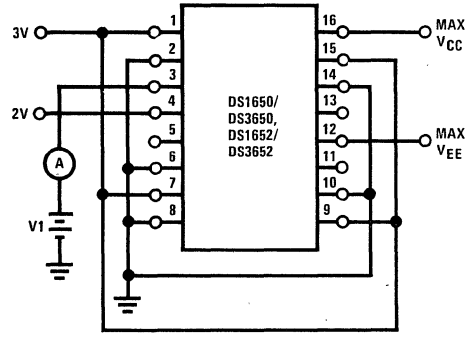
Note. Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to –3V.

FIGURE 5. I_{IH}



Note. Channel A(–) shown under test, other channels are tested similarly. Devices are tested with V1 from 3V to –3V.

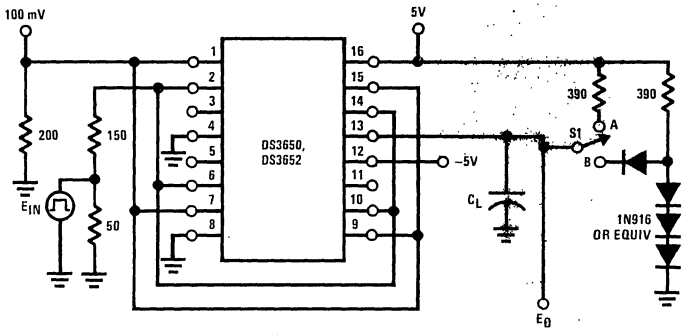
FIGURE 6. I_{IL}

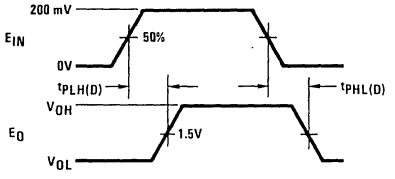


Note. Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4V and 2.4V.

FIGURE 7. I_{OFF}

AC Test Circuits and Switching Time Waveforms

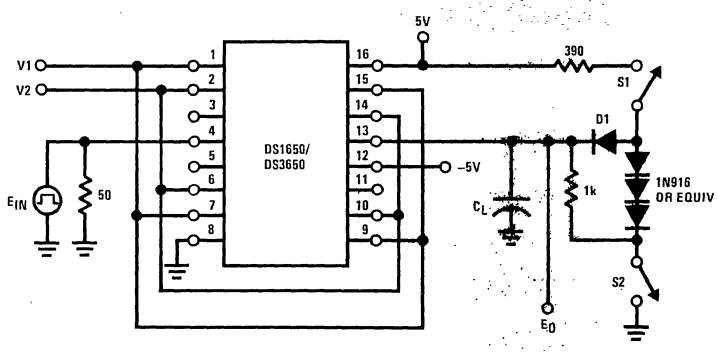




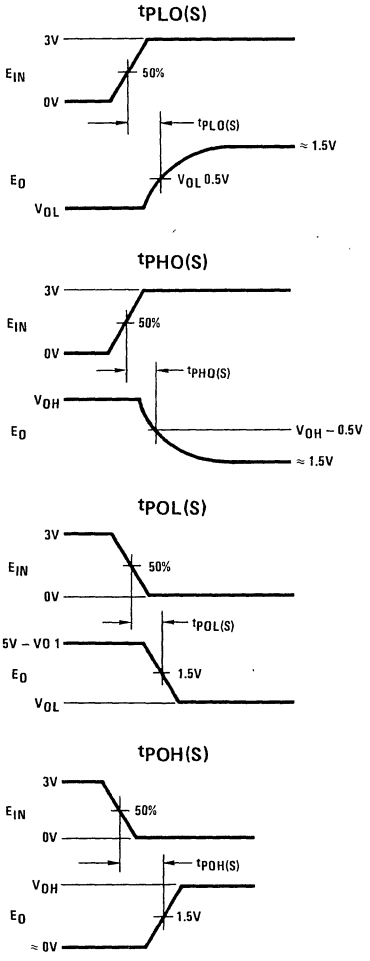
Note. Output of Channel B shown under test, other channels are tested similarly.
S1 at "A" for DS1652/DS3652
S1 at "B" for DS1650/DS3650
C_L = 15 pF total for DS1652/DS3652
C_L = 50 pF total for DS1650/DS3650

E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty Cycle = 500 ns

FIGURE 8. Receiver Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$



Note. Output of Channel B shown under test, other channels are tested similarly.

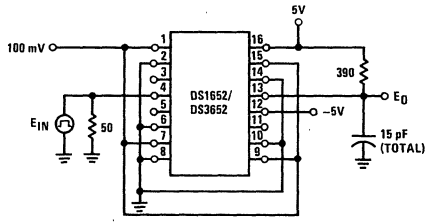


	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

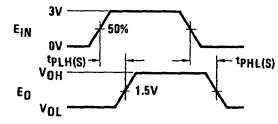
C_L includes jig and probe capacitance.
E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty Cycle = 50%

FIGURE 9. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHO(S)}$ and $t_{POH(S)}$

AC Test Circuits and Switching Time Waveforms (Continued)



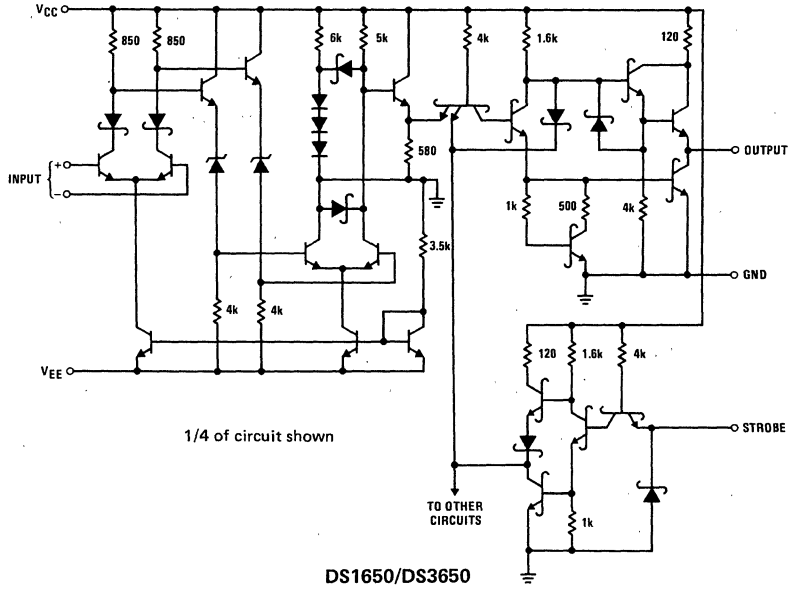
Note. Output of Channel B shown under test, other channels are tested similarly.



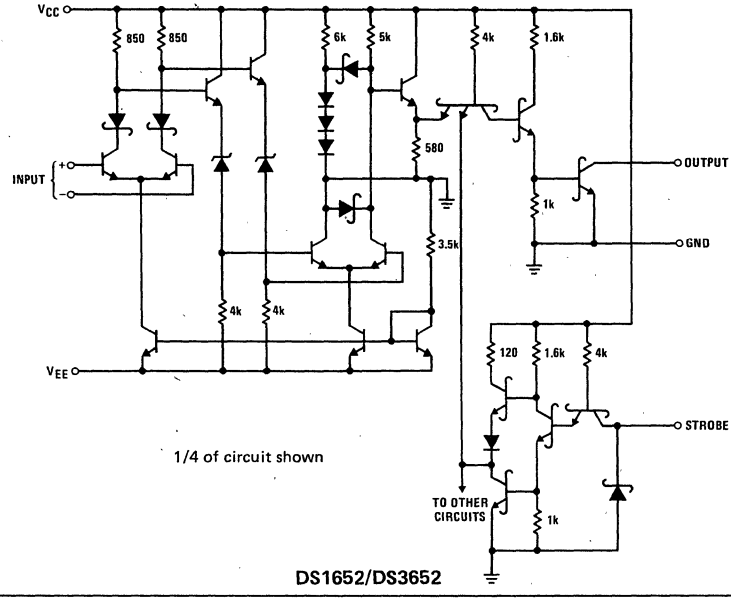
Note. E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty Cycle = 500 ns

FIGURE 10. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

Schematic Diagrams



DS1650/DS3650



DS1652/DS3652

National Semiconductor

Transmission Line Drivers/Receivers

DS1691A/DS3691 (RS-422/RS-423) Line Drivers with TRI-STATE®

General Description

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the requirements of EIA standards RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 independent line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to reduce rise time for suppression of near end crosstalk to other receivers in the cable.

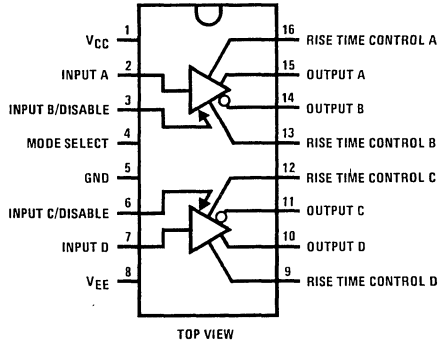
With the mode select pin low, the DS1691A/DS3691 are dual differential line drivers with TRI-STATE outputs. They feature ± 10V output common-mode range in TRI-STATE and 0V output unbalance when operated with ± 5V supply.

Features

- Dual RS-422 line driver with mode pin low, or quad RS-423 line driver with mode pin high
- Individually TRI-STATEable differential drivers in differential mode
- Short circuit protection for both source and sink outputs
- Outputs will not clamp line with power off or in TRI-STATE
- Individual rise time control for each output
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption
  - RS-422 35 mW/driver typ
  - RS-423 26 mW/driver typ
- Low current PNP inputs compatible with TTL, MOS and CMOS

Connection Diagram

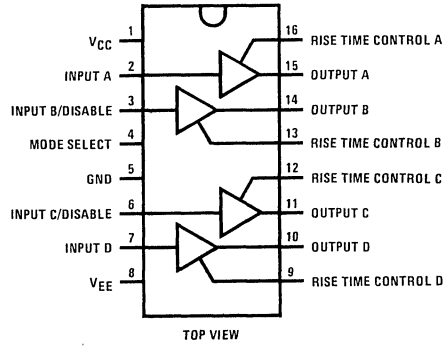
With Mode Select LOW (RS-422 Connection)



TOP VIEW

Connection Diagram

With Mode Select HIGH (RS-423 Connection)



TOP VIEW

Truth Table

Operation	Inputs			Outputs	
	Mode	A (D)	B (C)	A (D)	B (C)
RS-422	0	0	0	0	1
	0	0	1	TRI-STATE	TRI-STATE
	0	1	0	1	0
	0	1	1	TRI-STATE	TRI-STATE
RS-423	1	0	0	0	0
	1	0	1	0	1
	1	1	0	1	0
	1	1	1	1	1

Order Number DS1691AJ, DS3691J or DS3691N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	
V_{CC}	7V
V_{EE}	−7V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Input Voltage	15V
Output Voltage (Power OFF)	±15V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
DS1691A			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3691			
V_{CC}	4.75	5.25	V
V_{EE}	−4.75	−5.25	V
Temperature (T_A)			
DS1691A	−55	+125	°C
DS3691	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Parameter		Conditions		Min	Typ	Max	Units
RS-422 CONNECTION, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12$ mA				−1.5	V
V_O	Differential Output Voltage $V_{A,B}$	$R_L = \infty$	$V_{IN} = 2V$		3.6	6.0	V
$\overline{V_O}$			$V_{IN} = 0.8V$		−3.6	−6.0	V
V_T	Differential Output Voltage $V_{A,B}$	$R_L = 100\Omega$, $V_{CC} \geq 4.75V$	$V_{IN} = 2V$	2	2.4		V
$\overline{V_T}$			$V_{IN} = 0.8V$	−2	−2.4		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	$R_L = 100\Omega$			2.5	3	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	$R_L = 100\Omega$			0.05	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common-Mode Offset Voltage	$R_L = 100\Omega$			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	$R_L = 100\Omega$, $V_{CC} \geq 4.75V$		4.0	4.8		V
V_{CMR}	Output Voltage Common-Mode Range	$V_{DISABLE} = 2.4V$		±10			V
I_{XA}	Output Leakage Current Power OFF	$V_{CC} = 0V$	$V_{CMR} = 10V$			100	μA
I_{XB}			$V_{CMR} = -10V$			−100	μA
I_{OX}	TRI-STATE Output Current	$V_{CC} = Max$	$V_{CMR} \leq 10V$			100	μA
			$V_{CMR} \geq -10V$			−100	μA
I_{SA}	Output Short Circuit Current	$V_{IN} = 2.4V$	$V_{OA} = 6V$		80	150	mA
			$V_{OB} = 0V$		−80	−150	mA
I_{SB}	Output Short Circuit Current	$V_{IN} = 0.4V$	$V_{OA} = 0V$		−80	−150	mA
			$V_{OB} = 6V$		80	150	mA
I_{CC}	Supply Current				18	30	mA

AC Electrical Characteristics $T_A = 25°C$ (Note 5)

Parameter		Conditions	Min	Typ	Max	Units
RS-422 CONNECTION, $V_{CC} = 5V$, MODE SELECT = 0.8V						
t_r	Output Rise Time	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 1*)		120	200	ns
t_f	Output Fall Time	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 1*)		120	200	ns
t_{PDH}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 1*)		120	200	ns
t_{PDL}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 1*)		120	200	ns
t_{PZL}	TRI-STATE Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ pF (*Figure 4*)		250	350	ns
t_{PZH}	TRI-STATE Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ pF (*Figure 4*)		180	300	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ pF (*Figure 4*)		180	300	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ pF (*Figure 4*)		250	350	ns

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

Parameter		Conditions		Min	Typ	Max	Units
RS-423 CONNECTION, $\lvert V_{CC}\rvert = \lvert V_{EE}\rvert$, MODE SELECT ≥ 2V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12$ mA				−1.5	V
V_O	Output Voltage	$R_L = \infty$, (Note 6) $V_{CC} \geq 4.75V$	$V_{IN} = 2V$	4.0	4.4	6.0	V
$\overline{V_O}$			$V_{IN} = 0.4V$	−4.0	−4.4	−6.0	V
V_T	Output Voltage	$R_L = 450\Omega$, $V_{CC} \geq 4.75V$	$V_{IN} = 2.4V$	3.6	4.1		V
$\overline{V_T}$			$V_{IN} = 0.4V$	−3.6	−4.1		V
$\lvert V_T\rvert - \lvert\overline{V_T}\rvert$	Output Unbalance	$\lvert V_{CC}\rvert = \lvert V_{EE}\rvert = 4.75V$, $R_L = 450\Omega$			0.02	0.4	V
I_X^+	Output Leakage Power OFF	$V_{CC} = V_{EE} = 0V$	$V_O = 6V$		2	100	μA
I_X^-	Output Leakage Power OFF	$V_{CC} = V_{EE} = 0V$	$V_O = -6V$		−2	−100	μA
I_S^+	Output Short Circuit Current	$V_O = 0V$	$V_{IN} = 2.4V$		−80	−150	mA
I_S^-	Output Short Circuit Current	$V_O = 0V$	$V_{IN} = 0.4V$		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	$V_{IN} = 0.4V$, $R_L = \infty$			−10	−22	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1691A and across the 0°C to +70°C range for the DS3691. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Note 5: Symbols and definitions correspond to EIA RS-422 and/or RS-423 where applicable.

Note 6: At −55°C, the output voltage is +3.9V minimum and −3.9V minimum.

AC Electrical Characteristics $T_A = 25°C$ (Note 5)

Parameter		Conditions	Min	Typ	Max	Units
RS-423 CONNECTION, $V_{CC} = 5V$, $V_{EE} - 5V$, MODE SELECT = 2.4V						
t_r	Rise Time	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ (*Figure 2*)		120	300	ns
t_f	Fall Time	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ (*Figure 2*)		120	300	ns
t_r	Rise Time	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 50$ pF (*Figure 3*)		3.0		μs
t_f	Fall Time	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 50$ pF (*Figure 3*)		3.0		μs
t_{rc}	Rise Time Coefficient	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 50$ pF (*Figure 3*)		0.06		μs/pF
t_{PDH}	Output Propagation Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ (*Figure 2*)		180	300	ns
t_{PDL}	Output Propagation Delay	$R_L = 450\Omega$, $C_L = 500$ pF, $C_C = 0$ (*Figure 2*)		180	300	ns

AC Test Circuits and Switching Time Waveforms

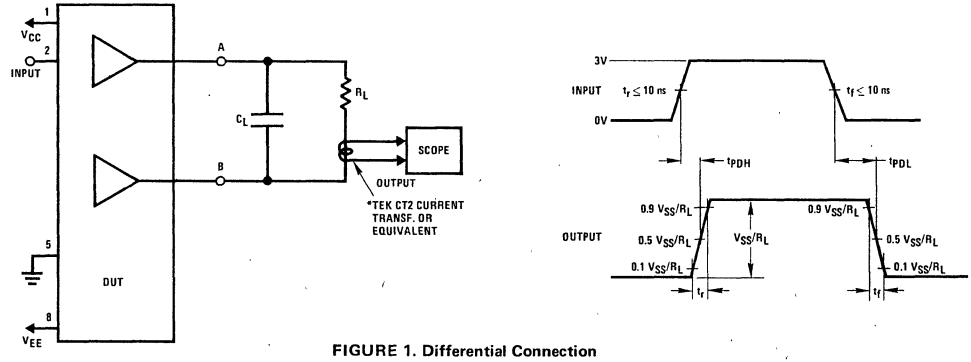


FIGURE 1. Differential Connection

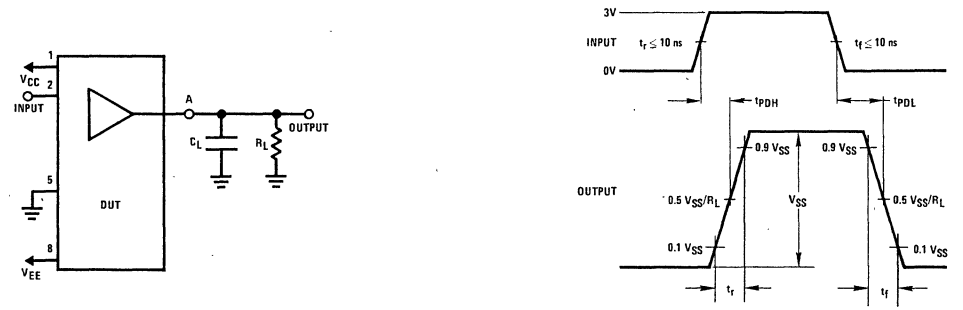


FIGURE 2. RS-423 Connection

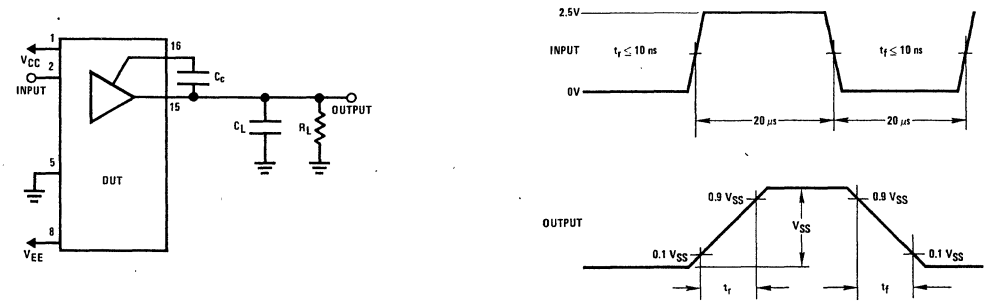


FIGURE 3. Rise Time Control for RS-423

AC Test Circuits and Switching Time Waveforms (Continued)

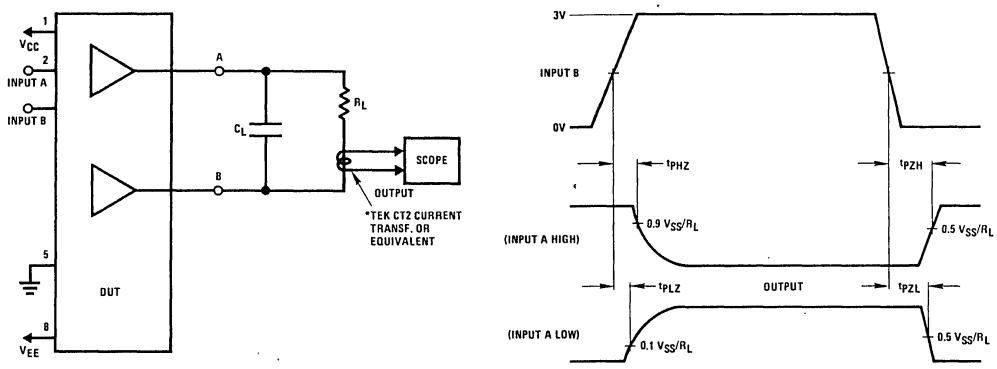
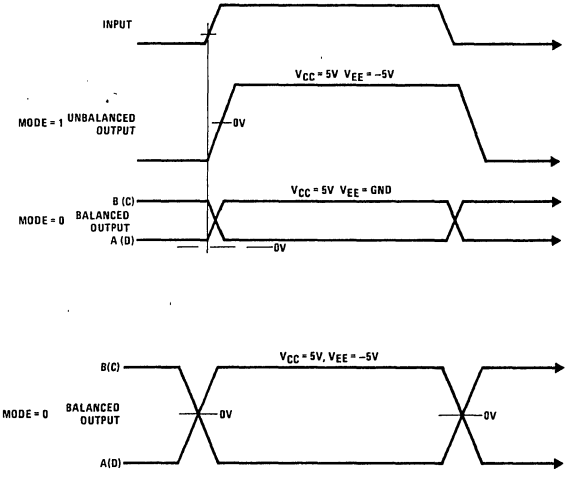


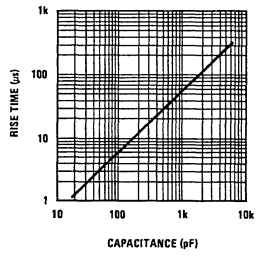
FIGURE 4. TRI-STATE® Delays

Switching Waveforms



Typical Rise Time Control Characteristics

Rise Time vs External Capacitor



National Semiconductor

Transmission Line Drivers/Receivers

DS1692/DS3692 TRI-STATE® Differential Line Drivers

General Description

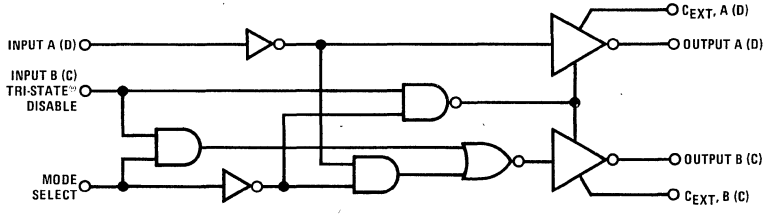
The DS1692/DS3692 are low power Schottky TTL line drivers electrically similar to the DS1691A/DS3691 but tested to meet the requirements of MIL-STD-188-114. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 independent line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to reduce rise time for suppression of near end crosstalk to other receivers in the cable.

With the mode select pin low, the DS1692/DS3692 are dual differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE and 0V output unbalance when operated with ±5V supply.

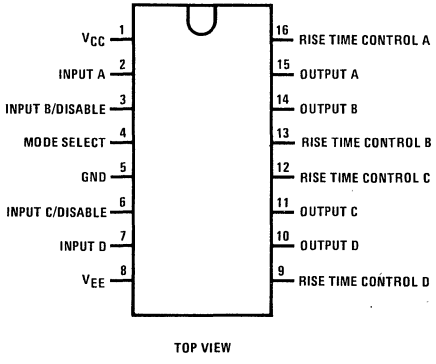
Features

- Dual differential line driver or quad single-ended line driver
- Individually TRI-STATEable differential drivers meet MIL-STD-188-114
- Short circuit protection for both source and sink outputs
- Individual rise time control for each output
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption
  - Differential mode 35 mW/driver typ
  - Single-ended mode 26 mW/driver typ
- Low current PNP inputs compatible with TTL, MOS and CMOS

Logic Diagram (1/2 Circuit Shown)



Connection Diagram



TOP VIEW

Order Number DS1692J, DS3692J or DS3692N
See NS Package J16A or N16A

Truth Table

Inputs			Outputs	
Mode	A (D)	B (C)	A (D)	B (C)
0	0	0	0	1
0	0	1	TRI-STATE	TRI-STATE
0	1	0	1	0
0	1	1	TRI-STATE	TRI-STATE
1	0	0	0	0
1	0	1	0	1
1	1	0	1	0
1	1	1	1	1

Absolute Maximum Ratings (Note 1)

Supply Voltage
- V_{CC} 7V
- V_{EE} −7V

Maximum Power Dissipation* at 25°C
- Cavity Package 1509 mW
- Molded Package 1476 mW

Input Voltage 15V

Output Voltage (Power OFF) ±15V

Storage Temperature −65°C to +150°C

Lead Temperature (Soldering, 10 seconds) 300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage			
DS1692			
V_{CC}	4.5	5.5	V
V_{EE}	−4.5	−5.5	V
DS3692			
V_{CC}	4.75	5.25	V
V_{EE}	−4.75	−5.25	V
Temperature (T_A)			
DS1692	−55	+125	°C
DS3692	0	+70	°C

Electrical Characteristics DS1692/DS3692 (Notes 2, 3 and 4)

Parameter		Conditions		Min	Typ	Max	Units
DS1692, V_{CC} = 5V ± 10%, DS3692, V_{CC} = 5V ± 5%, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_O	Differential Output Voltage	$R_L = \infty$	V_{IN} = 2V	2.5	3.6		V
$\overline{V_O}$	$V_{A,B}$		V_{IN} = 0.8V	−2.5	−3.6		V
V_T	Differential Output Voltage	$R_L = 100\Omega$	V_{IN} = 2V	2	2.6		V
$\overline{V_T}$	$V_{A,B}$	$V_{CC} \geq 4.75V$	V_{IN} = 0.8V	−2	−2.6		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	$R_L = 100\Omega$			2.5	3	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	$R_L = 100\Omega$			0.05	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common-Mode Offset Voltage	$R_L = 100\Omega$			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	$R_L = 100\Omega$, $V_{CC} \geq 4.75V$		4.0	4.8		V
I_{OX}	TRI-STATE Output Current	$V_O \leq -10V$			−0.002	−0.15	mA
		$V_O \geq 15V$			0.002	0.15	mA
I_{SA}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 6V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
I_{SB}	Output Short Circuit Current	V_{IN} = 0.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6V		80	150	mA
I_{CC}	Supply Current				18	30	mA
DS1692, V_{CC} = 5V ± 10%, V_{EE} = −5V ± 10%, DS3692, V_{CC} = 5V ± 5%, V_{EE} = −5 ± 5%, MODE SELECT ≤ 0.8V							
V_O	Differential Output Voltage	$R_L = \infty$	V_{IN} = 2.4V	7	8.5		V
$\overline{V_O}$	$V_{A,B}$		V_{IN} = 0.4V	−7	−8.5		V
V_T	Differential Output Voltage	$R_L = 200\Omega$	V_{IN} = 2.4V	6	7.3		V
$\overline{V_T}$	$V_{A,B}$		V_{IN} = 0.4V	−6	−7.3		V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Output Unbalance	$\lvert V_{CC} \rvert = \lvert V_{EE} \rvert$, $R_L = 200\Omega$			0.02	0.4	V
I_{OX}	TRI-STATE Output Current		V_O = 10V		0.002	0.15	mA
			V_O = −10V		−0.002	−0.15	mA
I_S^+	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		−80	−150	mA
I_S^-			V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		μA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, $R_L = \infty$			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, $R_L = \infty$			−10	−22	mA

Electrical Characteristics (Notes 2 and 3) $V_{EE} \leq 0V$

Parameter		Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.4V$			1	40	μA
		$V_{IN} \leq 15V$			10	100	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$			−30	−200	μA
V_I	Input Clamp Voltage	$I_{IN} = -12$ mA				−1.5	V
I_{XA} I_{XB}	Output Leakage Current Power OFF	$V_{CC} = V_{EE} = 0$	$V_O = 15V$		0.01	0.15	mA
			$V_O = -15V$		−0.01	−0.15	mA

Switching Characteristics $T_A = 25°C$

Parameter		Conditions	Min	Typ	Max	Units
$V_{CC} = 5V$, MODE SELECT = 0.8V						
t_r	Differential Output Rise Time	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 1*)		120	200	ns
t_f	Differential Output Fall Time	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 1*)		120	200	ns
t_{PDH}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 1*)		120	200	ns
t_{PDL}	Output Propagation Delay	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 1*)		120	200	ns
t_{PZL}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 2*)		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 2*)		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 2*)		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 100\Omega$, $C_L = 500$ pF (*Figure 2*)		80	150	ns
$V_{CC} = 5V$, $V_{EE} = -5V$, MODE SELECT = 0.8V						
t_r	Differential Output Rise Time	$R_L = 200\Omega$, $C_L = 500$ pF (*Figure 1*)		190	300	ns
t_f	Differential Output Fall Time	$R_L = 200\Omega$, $C_L = 500$ pF (*Figure 1*)		190	300	ns
t_{PDL}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF (*Figure 1*)		190	300	ns
t_{PDH}	Output Propagation Delay	$R_L = 200\Omega$, $C_L = 500$ pF (*Figure 1*)		190	300	ns
t_{PZL}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF (*Figure 2*)		180	250	ns
t_{PZH}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF (*Figure 2*)		180	250	ns
t_{PLZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF (*Figure 2*)		80	150	ns
t_{PHZ}	TRI-STATE Delay	$R_L = 200\Omega$, $C_L = 500$ pF (*Figure 2*)		80	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1692 and across the 0°C to +70°C range for the DS3692. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$. V_{CC} and V_{EE} as listed in operating conditions.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

AC Test Circuits and Switching Time Waveforms

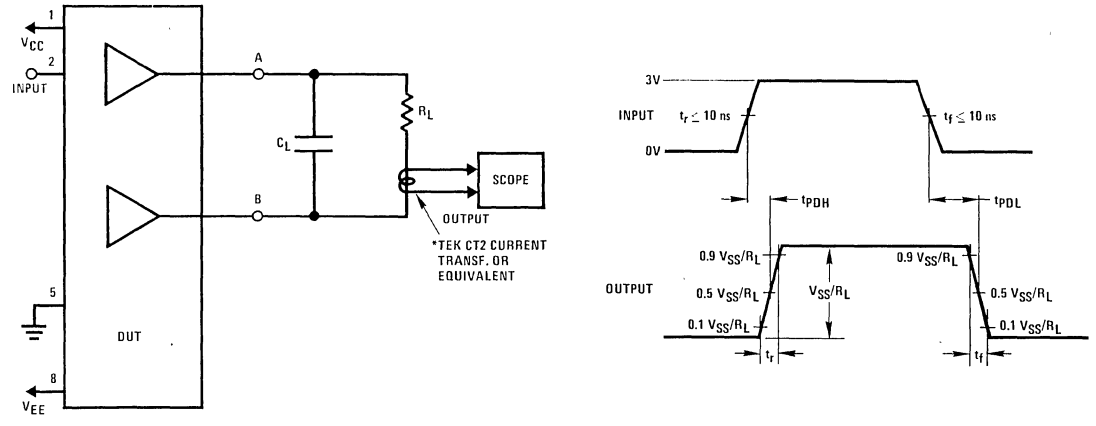


FIGURE 1. Differential Connection

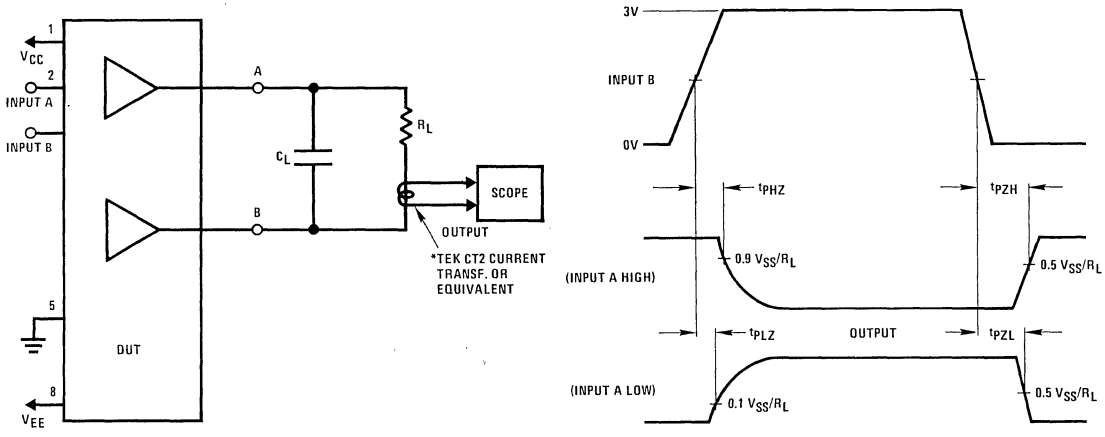
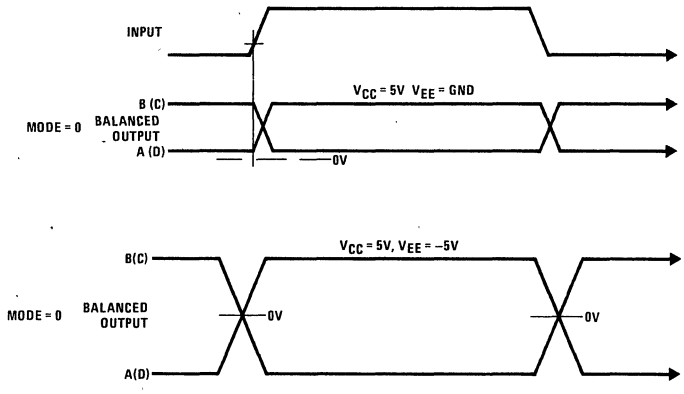
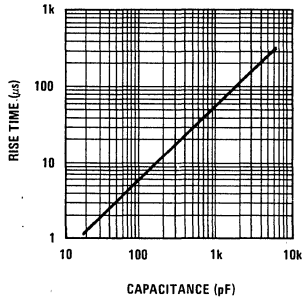


FIGURE 2. TRI-STATE Delays for DS1692/DS3692

Switching Waveforms



Typical Rise Time Control Characteristics



National Semiconductor

Transmission Line Drivers/Receivers
PRELIMINARY

DS3695/DS3696/DS3697/DS3698 Differential TRI-STATE® Bus/Line Transceivers/Repeaters

General Description

The DS3695, DS3696, DS3697 and DS3698 are high speed differential TRI-STATE bus/line transceivers/repeaters designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission.

The driver and receiver outputs feature TRI-STATE capability, for the driver outputs over the entire common mode range of +12V to −7V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state. The DS3696 and DS3698 provide an output pin which reports the occurrence of a line fault causing thermal shutdown of the device. This is an "open collector" pin with an internal 10 kΩ pull-up resistor. This allows the line fault outputs of several devices to be wire OR-ed.

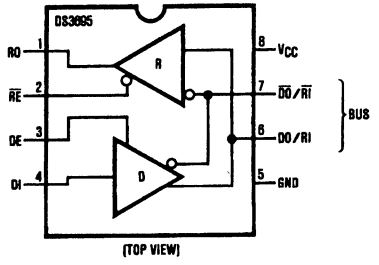
Both AC and DC specifications are guaranteed over the 0 to 70°C temperature and 4.75V to 5.25V supply voltage range.

TRI-STATE® is a registered trademark of National Semiconductor Corp.

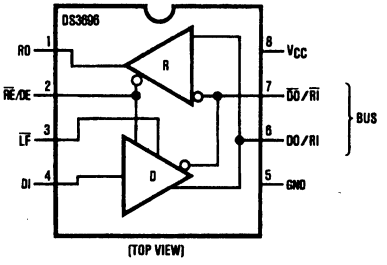
Features

- Meets new EIA standard RS485 (PN1488), for multipoint bus transmission.
- 15 ns driver propagation delays with 2 ns skew (typical).
- Single channel per package isolates faulty channels (from shutting down good channels).
- Single +5V supply.
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- Thermal shutdown protection.
- Power-up down glitch-free driver outputs permit live insertion or removal of transceivers.
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down.
- Line fault reporting capability on DS3696 and DS3698 allows automated fault location and re-routing under processor control.
- 12 kΩ Minimum receiver input impedance.
- 70 mV typical receiver hysteresis.

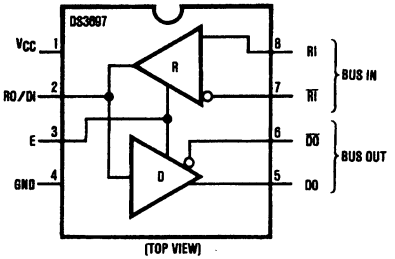
Connection and Logic Diagrams



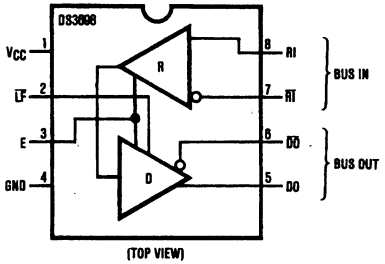
TL/F/5272–1



TL/F/5272–2



TL/F/5272–3



TL/F/5272–4

Order Number DS3695N, DS3696N, DS3697N or DS3698N
See NS Package N08E

Absolute Maximum Ratings (Note 1)

Supply voltage, V_{CC}	7V
Control input voltages	7V
Driver input voltage	7V
Driver output voltages	+15V/−10V
Receiver input voltages (DS3695, DS3696)	+15V/−10V
Receiver common mode voltage (DS3697, DS3698)	±25V
Receiver output voltage	5.5V
Continuous power dissipation @70°C	780 mW
Storage temperature range	−65°C to +150°C
Lead temperature (Soldering 10 seconds)	300°C

Recommended Operating Conditions

	Min	Max	Units
Supply voltage, V_{CC}	4.75	5.25	V
Bus voltage	−7	+12	V
Operating free air temperature T_A	0	70	°C

Electrical Characteristics (Notes 2 and 3) – (0°C ≤ T_A ≤ 70°C, 4.75V < V_{CC} < 5.25V unless otherwise specified)

Symbol	Parameter		Conditions		Min	Typ	Max	Units
V_{OD1}	Differential Driver Output Voltage (Unloaded)		$I_O = 0$				5	V
V_{OD2}	Differential Driver Output Voltage (with Load)		(Figure 1)		1.5			V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage For Complementary Output States		(Figure 1)				0.2	V
V_{OC}	Driver Common Mode Output Voltage		(Figure 1)				3.0	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common Mode Output Voltage For Complementary Output States		(Figure 1)				0.2	V
V_{IH}	Input High Voltage	DI, DE, $\overline{RE}$, E			2			V
V_{IL}	Input Low Voltage	DI, DE, $\overline{RE}$, E					0.8	V
V_{CL}	Input Clamp Voltage	DI, DE, $\overline{RE}$, E	$I_{IN} = -18$ mA				−1.5	V
I_{IL}	Input Low Current	DI, DE, $\overline{RE}$, E	$V_{IL} = 0.4V$				−360	μA
I_{IH}	Input High Current	DI, DE, $\overline{RE}$, E	$V_{IH} = 2.4V$				20	μA
I_{OZD}	TRI-STATE OUTPUT Current for Driver		$V_{CC} = 0V$ or V_{CC} = Max	$V_O = 12V$			+1	mA
				$V_O = -7V$			−0.8	mA
V_{TH}	Differential Input Threshold Voltage for Receiver		$V_{OUT} = V_{OL}$ or V_{OH} $-7V \le V_{CM} \le +12V$		−0.2		+0.2	V
ΔV_{TH}	Receiver Input Hysteresis		$V_{CM} = 0V$			70		mV
V_{OH}	Receiver Output High Voltage		$I_{OH} = -400$ μA		2.4			V
V_{OL}	Output Low Voltage	RO	$I_{OL} = 16$ mA				0.5	V
		$\overline{LF}$	$I_{OL} = 8$ mA				0.45	
I_{OZR}	OFF-State (High Impedance) Output Current at Receiver		V_{CC} = Max $0.4V \le V_O \le 2.4V$				±20	μA
R_{IN}	Receiver Input Resistance		$-7V \le V_{CM} \le +12V$		12			kΩ
I_{CC}	Supply current (total package)		No Load	Driver outputs enabled		40		mA
				Driver outputs disabled		23		mA
I_{OSD}	Driver Short-circuit Output current		Output voltage = −7V				−250	mA
			Output voltage = +12V				−250	mA
I_{OSR}	Receiver short-circuit Output current		$V_O = 0V$,		−15		−85	mA

Note 1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

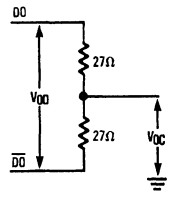
Note 2. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

Switching Characteristics ($4.75V \le V_{CC} \le 5.25V$; $0°C < T_A < 70°C$)

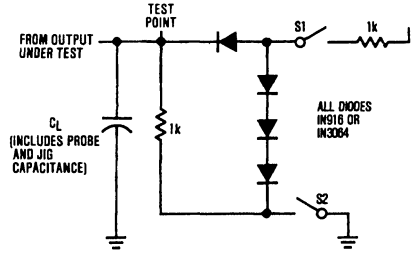
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Driver Input to Output	$R_{L_{DIFF}} = 60\Omega$		15		ns
t_{PHL}	Driver Input to Output	$C_{L1} = C_{L2} = 100$ pF		15		ns
Skew	Driver Output to Output	(Figures 3 and 5)		2		ns
t_{ZH}	Driver Enable to Output High	$C_L = 100$ pF (Figures 4 and 6) S1 open		33		ns
t_{ZL}	Driver Enable to Output Low	$C_L = 100$ pF (Figures 4 and 6) S2 open		33		ns
t_{LZ}	Driver Disable Time from Low	$C_L = 15$ pF (Figures 4 and 6) S2 Open		33		ns
t_{HZ}	Driver Disable Time from High	$C_L = 15$ pF (Figures 4 and 6) S1 Open		33		ns
t_{PLH}	Receiver Input to Output	$C_L = 15$ pF (Figures 2 and 7)		22		ns
t_{PHL}	Receiver Input to Output	S1 and S2 Closed		22		ns
t_{ZL}	Receiver Enable to Output Low	$C_L = 15$ pF (Figures 2 and 8) S2 Open		15		ns
t_{ZH}	Receiver Enable to Output High	$C_L = 15$ pF (Figures 2 and 8) S1 Open		15		ns
t_{LZ}	Receiver Disable from Low	$C_L = 15$ pF (Figures 2 and 8) S2 Open		12		ns
t_{HZ}	Receiver Disable from High	$C_L = 15$ pF (Figures 2 and 8) S1 Open		12		ns

AC Test Circuits



TL/F/5272-5

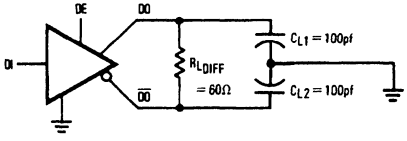
FIGURE 1.



TL/F/5272-6

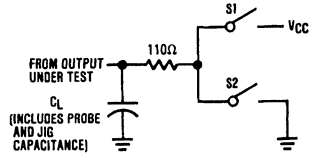
Note: S1 and S2 of load circuit are closed except as otherwise mentioned.

FIGURE 2.



TL/F/5272-7

FIGURE 3.



TL/F/5272-8

Note: Unless otherwise specified the switches are closed.

FIGURE 4.

Switching Time Waveforms

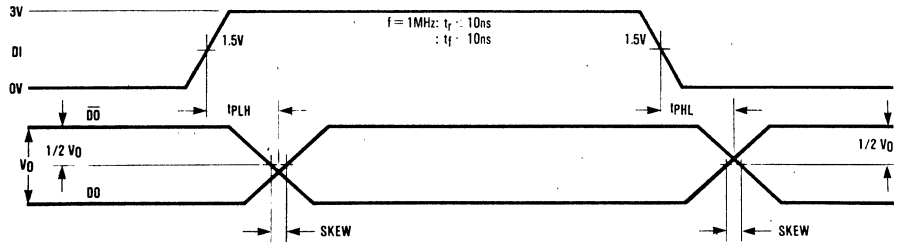


FIGURE 5. Driver Propagation Delays TL/F/5272-9

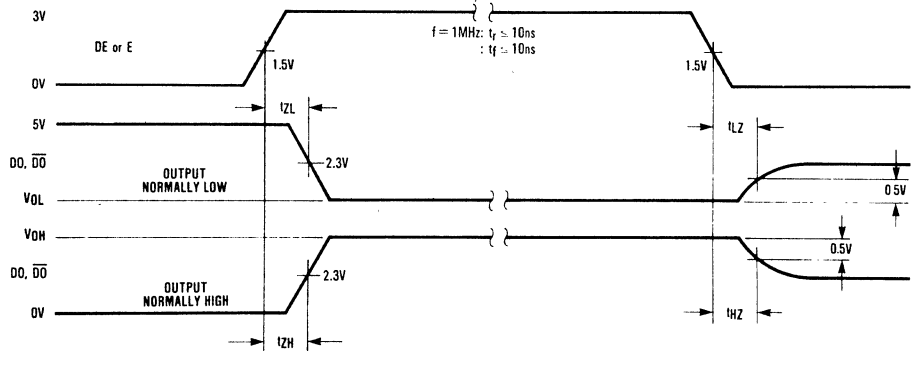
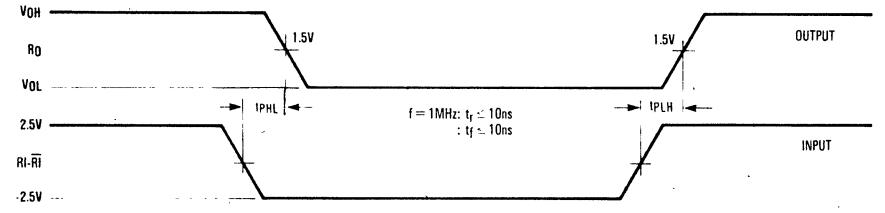


FIGURE 6. Driver Enable and Disable Times TL/F/5272-10



Note: Differential input voltage may be realized by grounding $\overline{RI}$ and pulsing RI between +2.5V and −2.5V

FIGURE 7. Receiver Propagation Delays TL/F/5272-11

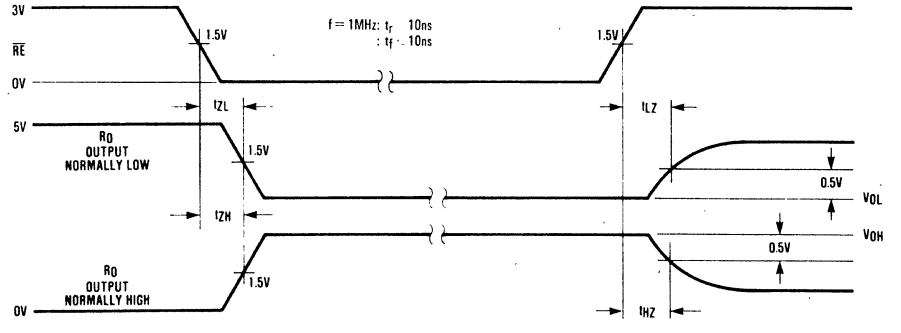


FIGURE 8. Receiver Enable and Disable Times TL/F/5272-12

Function Tables

DS3695/DS3696 Transmitting

Inputs			Line Condition	Outputs		
$\overline{RE}$	DE	DI		$\overline{DO}$	DO	$\overline{LF}$* (DS3696 Only)
X	1	1	No Fault	0	1	H
X	1	0	No Fault	1	0	H
X	0	X	X	Z	Z	H
X	1	X	Fault	Z	Z	L

DS3695/DS3696 Receiving

Inputs			Outputs	
$\overline{RE}$	DE	RI−$\overline{RI}$	RO	$\overline{LF}$* (DS3696 Only)
0	0	≥ +0.2V	1	H
0	0	≤ −0.2V	0	H
0	0	Inputs Open	1	H
1	0	X	Z	H

DS3697/DS3698

Inputs		Line Condition	Outputs			
E	RI−$\overline{RI}$		$\overline{DO}$	DO	RO/DI (DS3697 Only)	$\overline{LF}$* (DS3698 Only)
1	≥ +0.2V	No Fault	0	1	1	H
1	≤ −0.2V	No Fault	1	0	0	H
0	X	X	Z	Z	Z	H
1	≥ +0.2V	Fault	Z	Z	1	L
1	≤ −0.2V	Fault	Z	Z	0	L

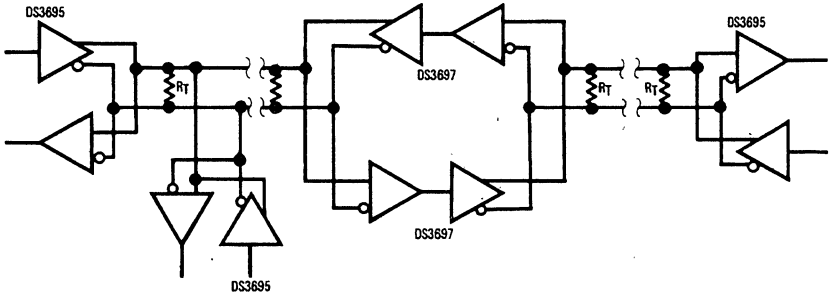
X — Don't care condition

Z — High impedance state

Fault — Improper line conditions causing excessive power dissipation in the driver, such as shorts or bus contention situations

*$\overline{LF}$ is an "open collector" output with an on-chip 10 kΩ pull-up resistor

Typical Application



TL/F/5272–13

National Semiconductor

Transmission Line Drivers/Receivers

DS55113/DS75113 Dual TRI-STATE® Differential Line Driver

General Description

The DS55113/DS75113 dual differential line drivers with TRI-STATE outputs are designed to provide all the features of the DS55114/DS75114 line drivers with the added feature of driver output controls. There are individual controls for each output pair, as well as a common control for both output pairs. When an output control is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

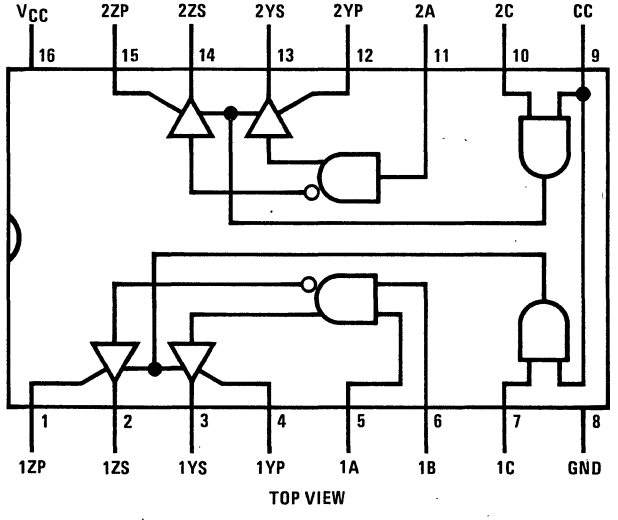
The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins.

Features

- Each circuit offers choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/LS compatibility
- High-impedance output state for party-line applications
- Short-circuit protection
- High current outputs
- Single-ended or differential AND/NAND outputs
- Common and individual output controls
- Clamp diodes at inputs
- Easily adaptable to DS55114/DS75114 applications

Connection Diagram

Dual-In-Line Package



TOP VIEW

Positive logic: $Y = \overline{AB}$, $Z = \overline{AB}$

Output is OFF when C or CC is low

Order Number DS55113J, DS75113J, or DS75113N
See NS Package J16A or N16A

Truth Table

INPUTS				OUTPUTS	
OUTPUT CONTROL		DATA		AND	NAND
C	CC	A	B*	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

H = high level
L = low level
X = irrelevant
Z = high impedance (OFF)
*B input and 4th line of truth table applicable only to driver number 1

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC}) (Note 1)	7V
Input Voltage	5.5V
OFF-State Voltage Applied to Open-Collector Outputs	12V
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Free-Air Temperature Range	
DS55113	−55°C to +125°C
DS75113	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 60 seconds): J Package	300°C
Lead Temperature (1/16" from case for 10 seconds): N Package	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C (Note 2).

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS55113	4.5	5.5	V
DS75113	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS55113	−55	125	°C
DS75113	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			CONDITIONS (Note 3)			DS55113 MIN	DS55113 TYP (Note 4)	DS55113 MAX	DS75113 MIN	DS75113 TYP (Note 4)	DS75113 MAX	UNITS
V_{IH}	High Level Input Voltage					2			2			V
V_{IL}	Low Level Input Voltage							0.8			0.8	V
V_{IK}	Input Clamp Voltage		V_{CC} = Min, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V		I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low Level Output Voltage		V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.23	0.4		0.23	0.4	V
V_{OK}	Output Clamp Voltage		V_{CC} = Max, I_O = −40 mA				−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	OFF-State Open-Collector Output Current		V_{CC} = Max	V_{OH} = 12V	T_A = 25°C		1	10				μA
					T_A = 125°C			200				
				V_{OH} = 5.25V	T_A = 25°C					1	10	
					T_A = 70°C						20	
I_{OZ}	OFF-State (High-Impedance-State) Output Current		V_{CC} = Max, Output Controls at 0.8V	T_A = 25°C, V_O = 0 to V_{CC}				±10			±10	μA
				T_A = Max	V_O = 0			−150			−20	
					V_O = 0.4V			±80			±20	
					V_O = 2.4V			±80			±20	
					V_O = V_{CC}			80			20	
I_I	Input Current at Maximum Input Voltage	A, B, C	V_{CC} = Max, V_I = 5.5V					1			1	mA
		CC						2			2	
I_{IH}	High Level Input Current	A, B, C	V_{CC} = Max, V_I = 2.4V					40			40	μA
		CC						80			80	
I_{IL}	Low Level Input Current	A, B, C	V_{CC} = Max, V_I = 0.4V					−1.6			−1.6	mA
		CC						−3.2			−3.2	
I_{OS}	Short-Circuit Output Current (Note 5)		V_{CC} = Max, V_O = 0			−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)		All Inputs at 0V, No Load, T_A = 25°C		V_{CC} = Max		47	65		47	65	mA
					V_{CC} = 7V		65	85		65	85	

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal information section.

Note 3: All parameters with the exception of OFF-state open-collector output current are measured with the active pull-up connected to the sink output.

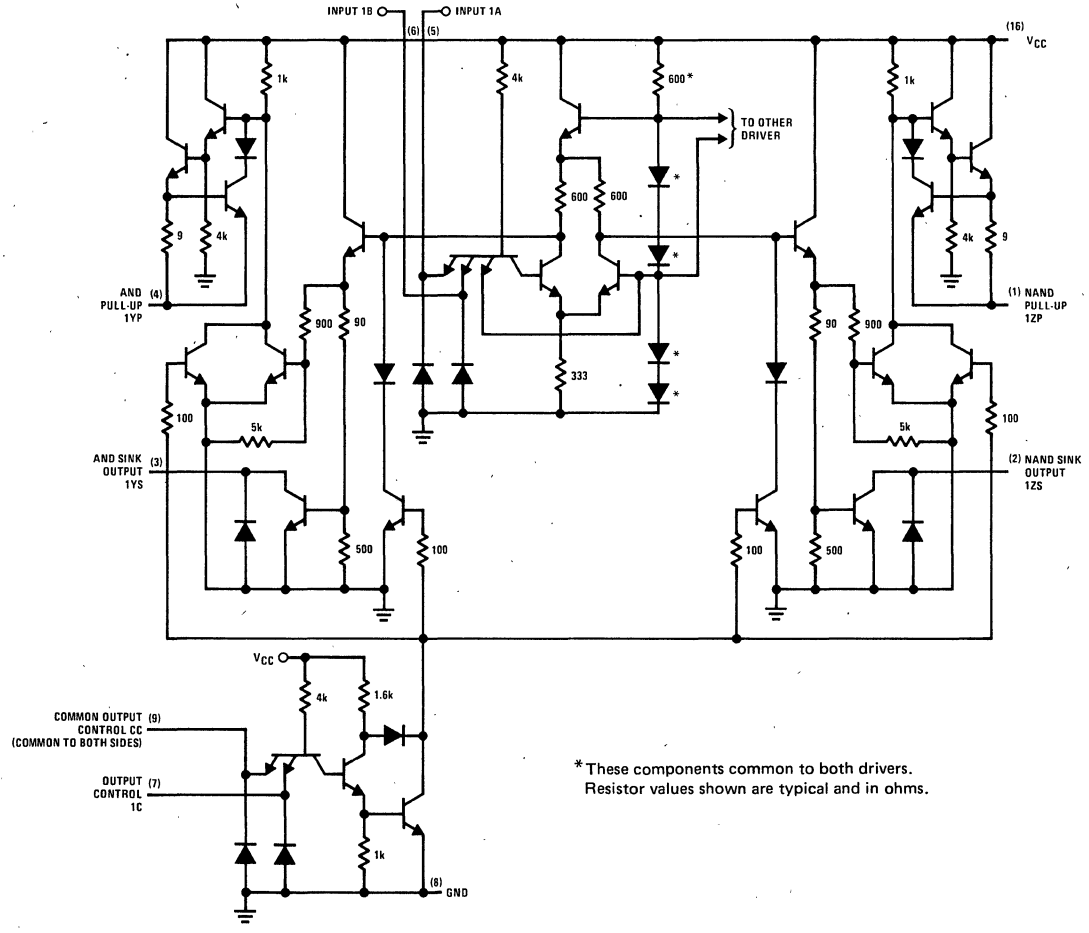
Note 4: All typical values are at T_A = 25°C and V_{CC} = 5V, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, C_L = 30 pF, T_A = 25°C

PARAMETER		CONDITIONS	DS55113			DS75113			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	*(Figure 1)*		13	20		13	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			12	20		12	30	ns
t_{PZH}	Output Enable Time to High Level	R_L = 180Ω, *(Figure 2)*		7	15		7	20	ns
t_{PZL}	Output Enable Time to Low Level	R_L = 250Ω, *(Figure 3)*		14	30		14	40	ns
t_{PHZ}	Output Disable Time from High Level	R_L = 180Ω, *(Figure 2)*		10	20		10	30	ns
t_{PLZ}	Output Disable Time from Low Level	R_L = 250Ω, *(Figure 3)*		17	35		17	35	ns

Schematic Diagram (One side shown only)



*These components common to both drivers.
Resistor values shown are typical and in ohms.

AC Test Circuits and Switching Time Waveforms

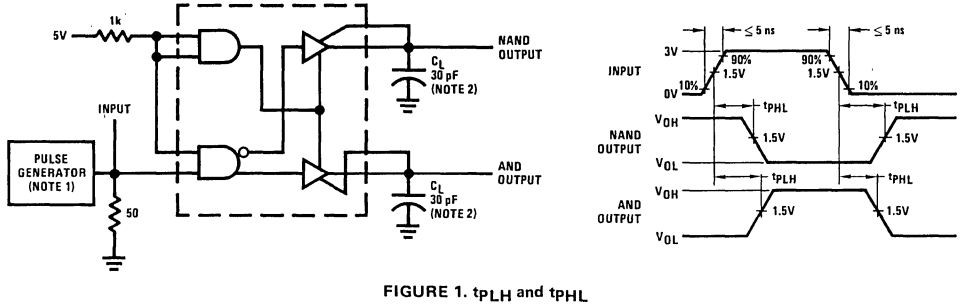


FIGURE 1. t_{PLH} and t_{PHL}

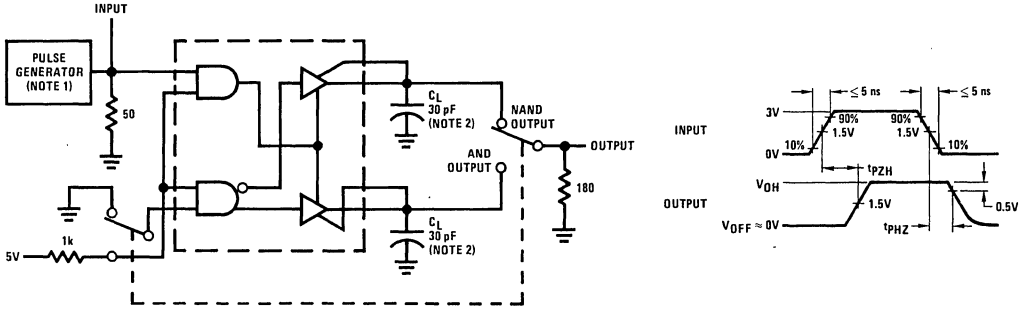


FIGURE 2. t_{PZH} and t_{PHZ}

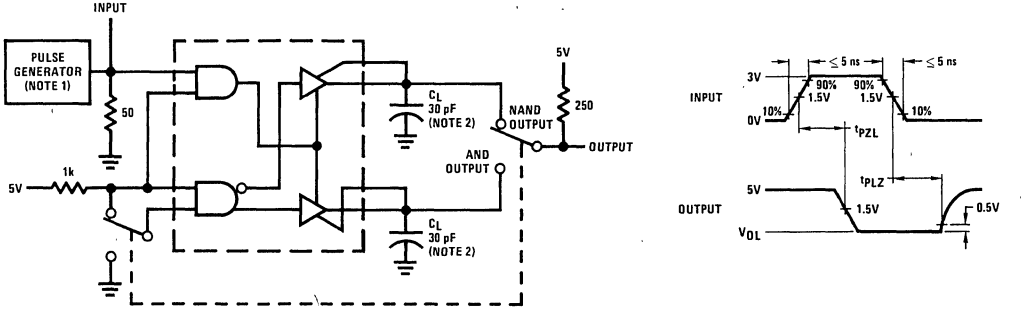


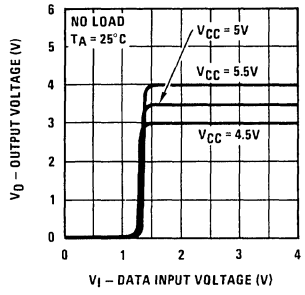
FIGURE 3. t_{PZL} and t_{PLZ}

Note 1: The pulse generator has the following characteristics: $Z_{OUT} = 50\Omega$, PRR = 500 kHz, $t_W \approx 100$ ns.

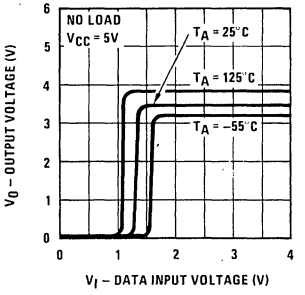
Note 2: C_L includes probe and jig capacitance.

Typical Performance Characteristics *

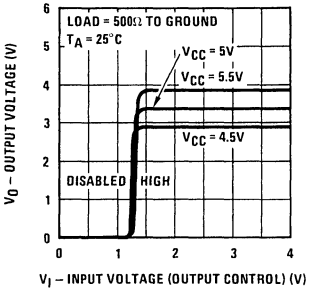
Output Voltage vs Data Input Voltage



Output Voltage vs Data Input Voltage



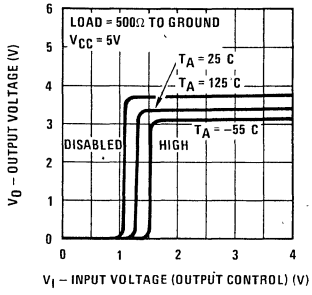
Output Voltage vs Output Control Voltage



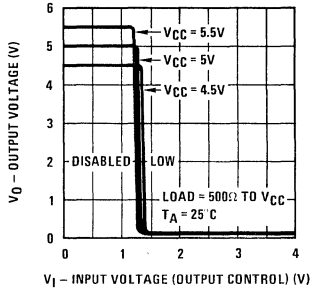
*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

Typical Performance Characteristics* (Continued)

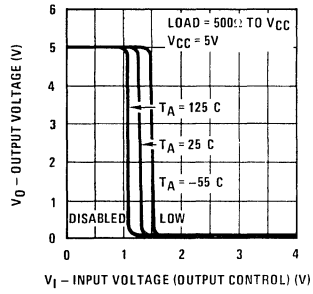
Output Voltage vs Output Control Voltage



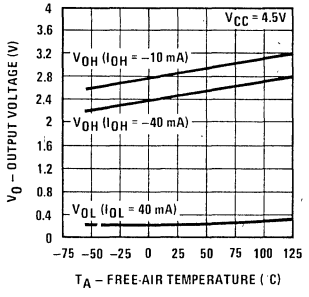
Output Voltage vs Output Control Voltage



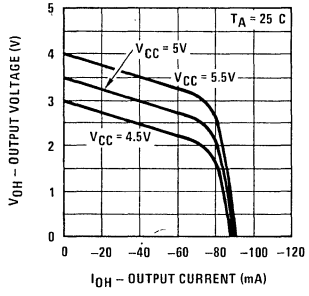
Output Voltage vs Output Control Voltage



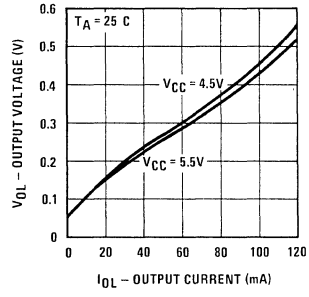
Output Voltage vs Free-Air Temperature



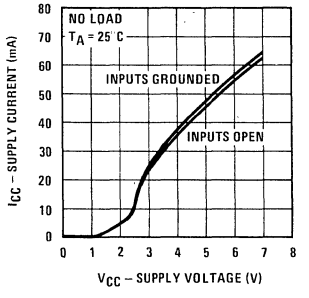
High Level Output Voltage vs Output Current



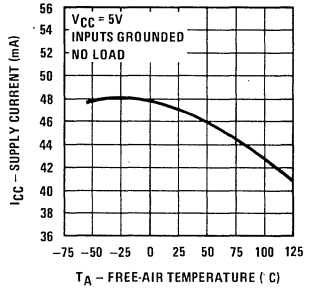
Low Level Output Voltage vs Output Current



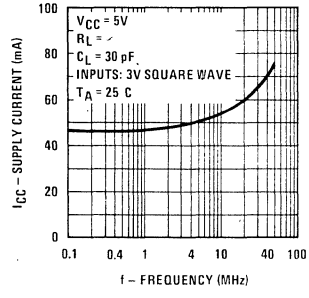
Supply Current (Both Drivers) vs Supply Voltage



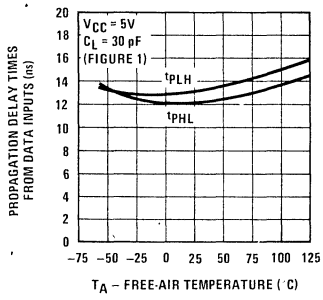
Supply Current (Both Drivers) vs Free-Air Temperature



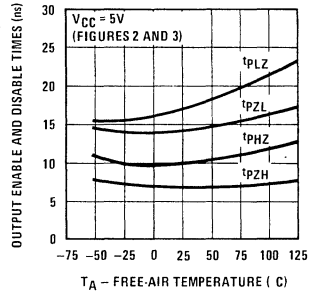
Supply Current (Both Drivers) vs Frequency



Propagation Delay Times from Data Inputs vs Free-Air Temperature



Output Enable and Disable Times vs Free-Air Temperature



*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

National Semiconductor

Transmission Line Drivers/Receivers

DS55114/DS75114 Dual Differential Line Drivers

General Description

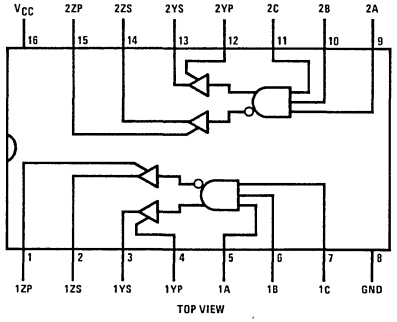
The DS55114/DS75114 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted pair at normal line impedances, without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL compatible output levels, these devices may also be used as TTL expanders or phase splitters.

Features

- Each circuit offers choice of open-collector or active pull-up (totem-pole) outputs
- Single 5V supply
- Differential line operation
- Dual channels
- TTL/LS compatibility
- Design to be interchangeable with Fairchild 9614 line drivers
- Short-circuit protection of outputs
- High current outputs
- Clamp diodes at inputs and outputs to terminate line transients
- Single-ended or differential AND/NAND outputs
- Triple inputs

Connection Diagram

Dual-In-Line Package



Positive logic: $Y = \overline{ABC}$
$Z = \overline{ABC}$

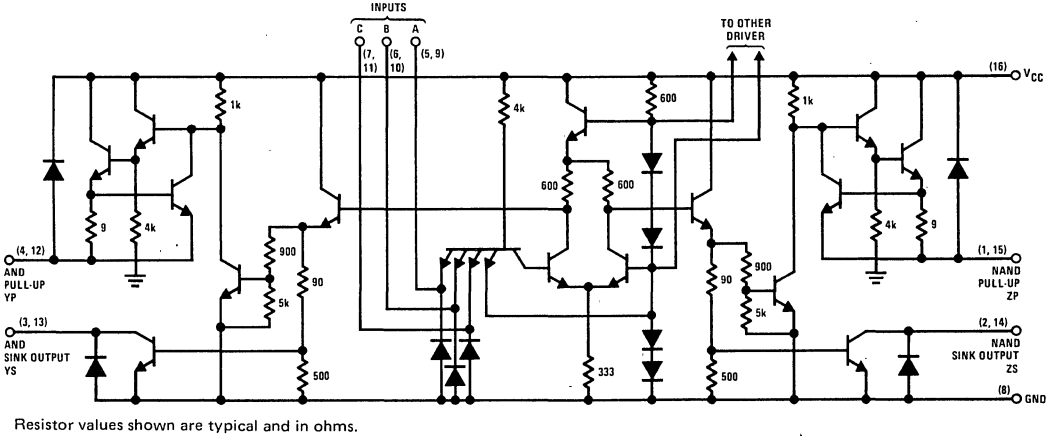
Order Number DS55114J, DS75114J, or DS75114N
See NS Package J16A or N16A

Truth Table

INPUTS			OUTPUTS	
A	B	C	Y	Z
H	H	H	H	L
All Other Input Combinations			L	H

H = high level
L = low level

Schematic Diagram (Each Driver)



Resistor values shown are typical and in ohms.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	7V
Input Voltage	5.5V
OFF-State Voltage Applied to Open-Collector Outputs	12V
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Free-Air Temperature Range	
DS55114	−55°C to +125°C
DS75114	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16" from case for 60 seconds): J Package	300°C
Lead Temperature (1/16" from case for 10 seconds): N Package	260°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C (Note 2).

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS55114	4.5	5.5	V
DS75114	4.75	5.25	V
High Level Output Current (I_{OH})		−40	mA
Low Level Output Current (I_{OL})		40	mA
Operating Free-Air Temperature (T_A)			
DS55114	−55	125	°C
DS75114	0	70	°C

Electrical Characteristics Over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS (Note 3)			DS55114 MIN	DS55114 TYP (Note 4)	DS55114 MAX	DS75114 MIN	DS75114 TYP (Note 4)	DS75114 MAX	UNITS
V_{IH}	High Level Input Voltage				2			2			V
V_{IL}	Low Level Input Voltage						0.8			0.8	V
V_{IK}	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V,	I_{OH} = −10 mA		2.4	3.4		2.4	3.4		V
		V_{IL} = 0.8V	I_{OH} = −40 mA		2	3.0		2	3.0		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 40 mA				0.2	0.4		0.2	0.45	V
V_{OK}	Output Clamp Voltage	V_{CC} = 5V, I_O = 40 mA, T_A = 25°C				6.1	6.5		6.1	6.5	V
		V_{CC} = Max, I_O = −40 mA, T_A = 25°C				−1.1	−1.5		−1.1	−1.5	
$I_{O(off)}$	OFF-State Open-Collector Output Current	V_{CC} = Max	V_{OH} = 12V	T_A = 25°C		1	100				μA
				T_A = 125°C			200				
			V_{OH} = 5.25V	T_A = 25°C					1	100	
				T_A = 70°C						200	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V					1			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V					40			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.1	−1.6		−1.1	−1.6	mA
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC} = Max, V_O = 0			−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply Current (Both Drivers)	Inputs Grounded, No Load, T_A = 25°C	V_{CC} = Max			37	50		37	50	mA
			V_{CC} = 7V			47	65		47	70	

Note 1: All voltage values are with respect to network ground terminal.

Note 2: For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section.

Note 3: All parameters, with the exception of OFF-state open-collector output current, are measured with the active pull-up connected to the sink output.

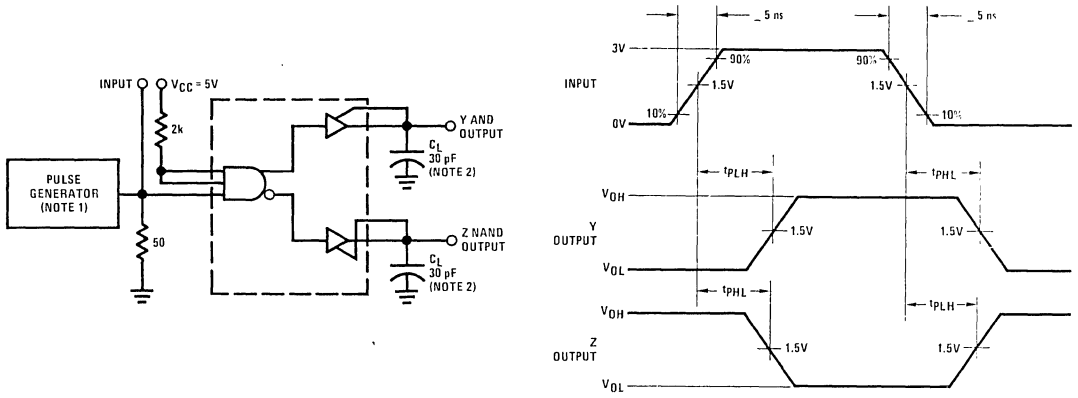
Note 4: All typical values are at T_A = 25°C and V_{CC} = 5V, with the exception of I_{CC} at 7V.

Note 5: Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	DS55114 MIN	DS55114 TYP	DS55114 MAX	DS75114 MIN	DS75114 TYP	DS75114 MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 30 pF, *(Figure 1)*		15	20		15	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			11	20		11	30	ns

AC Test Circuit and Switching Time Waveforms



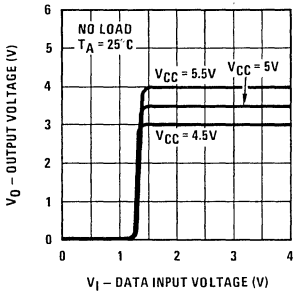
Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, t_w = 100 ns, PRR = 500 kHz..

Note 2: C_L includes probe and jig capacitance.

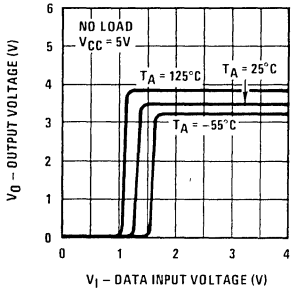
FIGURE 1

Typical Performance Characteristics

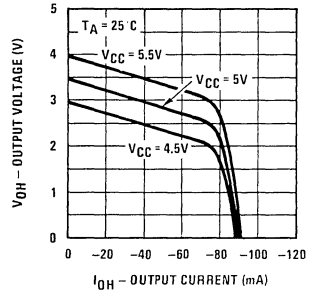
Output Voltage vs Data Input Voltage



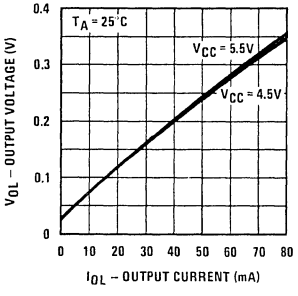
Output Voltage vs Data Input Voltage



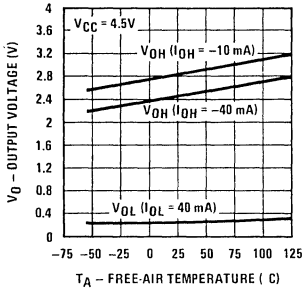
High Level Output Voltage vs Output Current



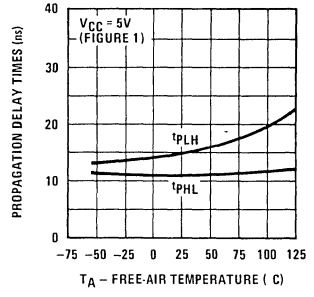
Low Level Output Voltage vs Output Current



Output Voltage vs Free-Air Temperature



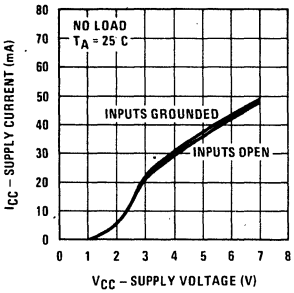
Propagation Delay Times vs Free-Air Temperature



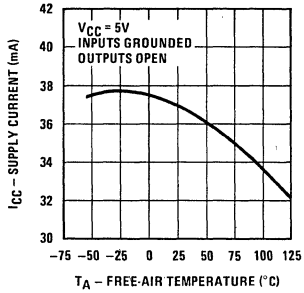
*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

Typical Performance Characteristics* (Continued)

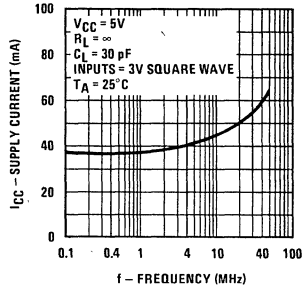
Supply Current (Both Drivers) vs Supply Voltage



Supply Current (Both Drivers) vs Free-Air Temperature



Supply Current (Both Drivers) vs Frequency



*Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75V and above 5.25V are applicable to DS55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

DS55115/DS75115 Dual Differential Line Receiver

General Description

The DS55115/DS75115 is a dual differential line receiver designed to sense differential signals from data transmission lines. Designed for operation over military and commercial temperature ranges, the DS55115/DS75115 can typically receive ±500 mV differential data with ±15V common-mode noise. Outputs are open-collector and give TTL compatible signals which are a function of the polarity of the differential input signal. Active output pull-ups are also available, offering the option of an active TTL pull-up through an external connection.

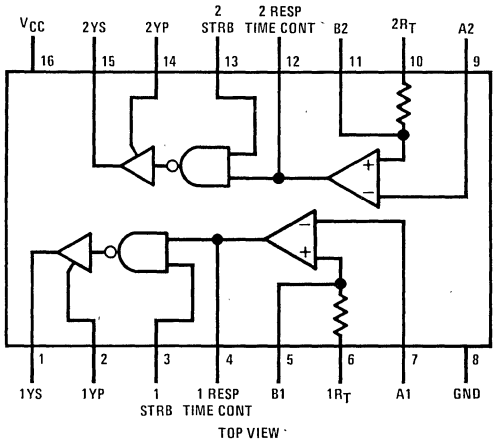
Response time may be controlled with the use of an external capacitor. Each channel may be independently controlled and optional input termination resistors are also available.

Features

- Single 5V supply
- High common-mode voltage range
- Each channel individually strobed
- Independent response time control
- Uncommitted collector or active pull-up option
- TTL compatible output
- Optional 130Ω termination resistors
- Direct replacement for 9615

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS55115J, DS75115J or DS75115N
See NS Package J16A or N16A

Function Table

STROBE	DIFF. INPUT	OUTPUT
L	X	H
H	L	H
H	H	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max

L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max

X = irrelevant

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC} (Note 1)	7V
Input Voltage at A, B and R_T Inputs	±25V
Input Voltage at Strobe Input	5.5V
Off-State Voltage Applied to Open-Collector Outputs	14V
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Free-Air Temperature Range	
DS55115	−55°C to +125°C
DS75115	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (1/16 inch from case for 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, (V_{CC})			
DS55115	4.5	5.5	V
DS75115	4.75	5.25	V
High Level Output Current, (I_{OH})		−5	mA
Low Level Output Current, (I_{OL})		15	mA
Operating Temperature, (T_A)			
DS55115	−55	125	°C
DS75115	0	70	°C

Electrical Characteristics (Notes 2, 3 and 5)

PARAMETER		CONDITIONS		DS55115			DS75115			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{TH}	Differential Input High-Threshold Voltage	V_O = 0.4V, I_{OL} = 15 mA, V_{IC} = 0			200	500		200	500	mV
V_{TL}	Differential Input Low-Threshold Voltage	V_O = 2.4V, I_{OH} = −5 mA, V_{IC} = 0			−200	−500		−200	−500	mV
V_{ICR}	Common-Mode Input Voltage Range	V_{ID} = ±1V		15 to −15	24 to −19		15 to −15	24 to −19		V
$V_{IH(STROBE)}$	High-Level Strobe Input Voltage			2.4			2.4			V
$V_{IL(STROBE)}$	Low-Level Strobe Input Voltage					0.4			0.4	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{ID} = −0.5V, I_{OH} = −5 mA	T_A = Min	2.2			2.4			V
			T_A = 25°C	2.4	3.4		2.4	3.4		
			T_A = Max	2.4			2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{ID} = 0.5V, I_{OL} = 15 mA			0.22	0.4		0.22	0.45	V
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, Other Input at 5.5V	T_A = Min			−0.9			−0.9	mA
			T_A = 25°C		−0.5	−0.7		−0.5	−0.7	
			T_A = Max			−0.7			−0.7	
I_{SH}	High Level Strobe Current	V_{CC} = Min, V_{ID} = −0.5V, V_{STROBE} = 4.5V	T_A = 25°C		0.5	2		0.5	5	µA
			T_A = Max			5			10	
I_{SL}	Low Level Strobe Current	V_{CC} = Max, V_{ID} = 0.5V, V_{STROBE} = 0.4V	T_A = 25°C		−1.15	−2.4		−1.15	−2.4	mA
I_4, I_{12}	Response Time Control Current (Pin 4 or Pin 12)	V_{CC} = Max, V_{ID} = 0.5V, V_{RC} = 0	T_A = 25°C	−1.2	−3.4		−1.2	−3.4		mA
$I_{O(OFF)}$	Off-State Open-Collector Output Current	V_{CC} = Min, V_{OH} = 12V, V_{ID} = −4.5V	T_A = 25°C			100				µA
			T_A = Max			200				
		V_{CC} = Min, V_{OH} = 5.25V, V_{ID} = −4.75V	T_A = 25°C						100	
			T_A = Max						200	
R_T	Line Terminating Resistance	V_{CC} = 5V	T_A = 25°C	77	130	167	74	130	179	Ω
I_{OS}	Short-Circuit Output Current	V_{CC} = Max, V_O = 0V, V_{ID} = −0.5V, (Note 4)	T_A = 25°C	−15	−40	−80	−14	−40	−100	mA
I_{CC}	Supply Current (Both Receivers)	V_{CC} = Max, V_{ID} = 0.5V, V_{IC} = 0V	T_A = 25°C		32	50		32	50	mA

Note 1: "Absolute Maximum Ratings' are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55115 and across the 0°C to +70°C range for the DS75115. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

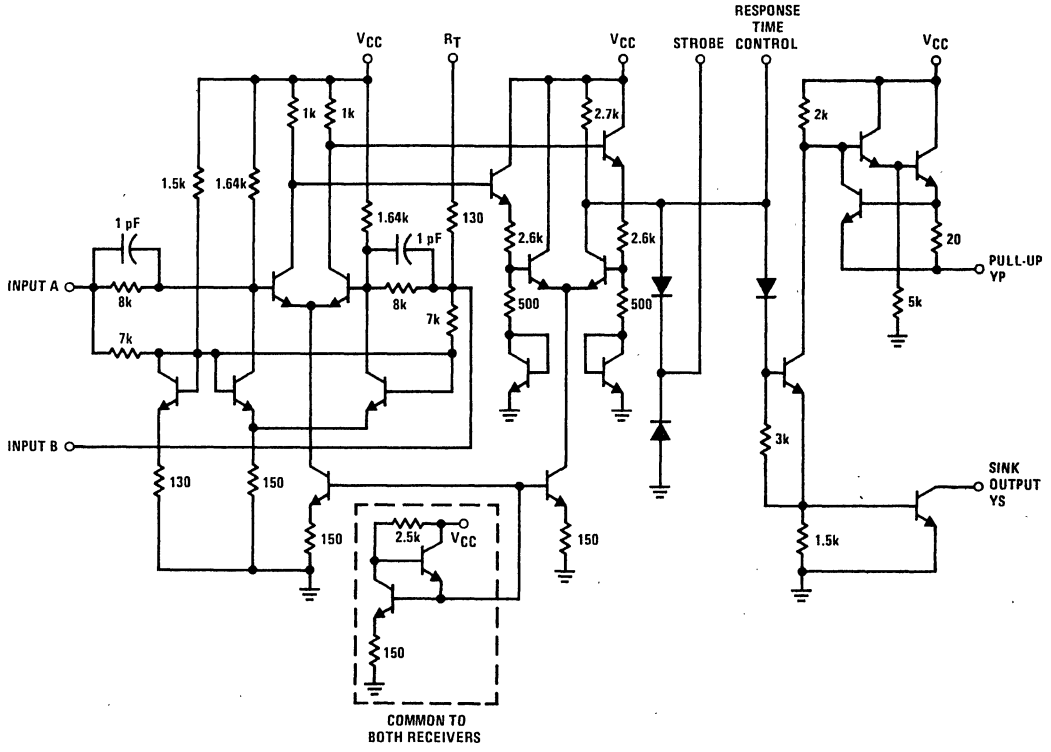
Note 4. Only one output at a time should be shorted.

Note 5: Unless otherwise noted, V_{STROBE} = 2.4V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.

Switching Characteristics V_{CC} = 5V, C_L = 30 pF, T_A = 25°C

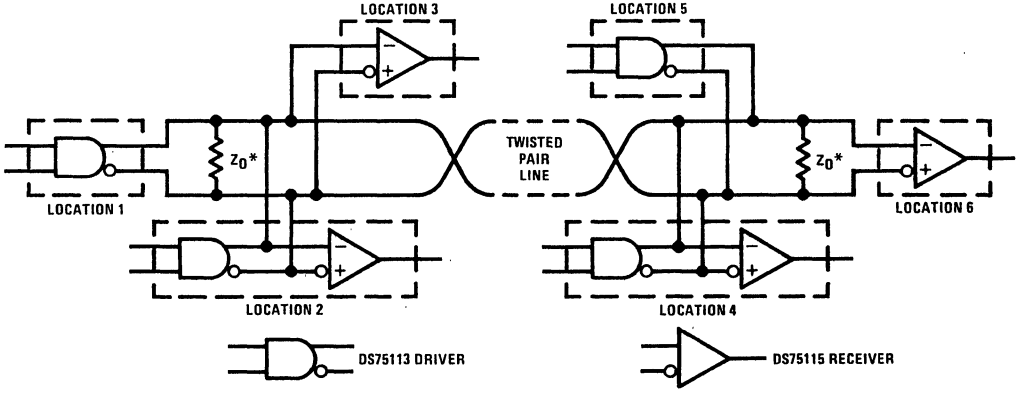
PARAMETER		CONDITIONS	DS55115			DS75115			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 3.9 kΩ, *(Figure 1)*		18	50		18	75	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 390Ω, *(Figure 1)*		20	50		20	75	ns

Schematic Diagram



Typical Application

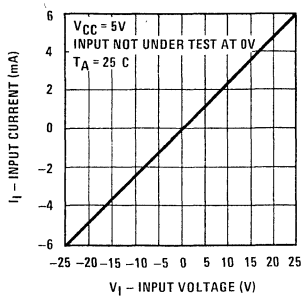
Basic Party-Line or Data-Bus Differential Data Transmission



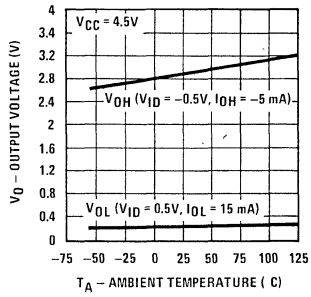
*Z_O is internal to the DS55115/DS75115
A capacitor may be connected in series with Z_O to reduce power dissipation.

Typical Performance Characteristics (Note 3)

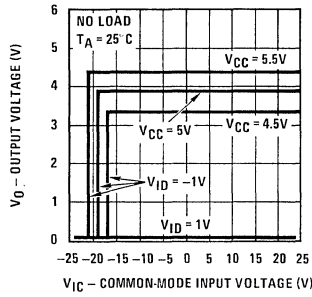
Input Current vs Input Voltage



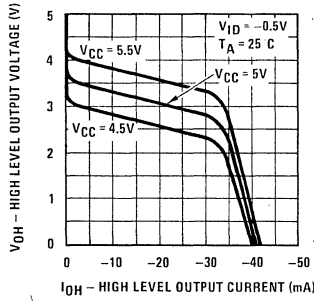
Output Voltage vs Temperature



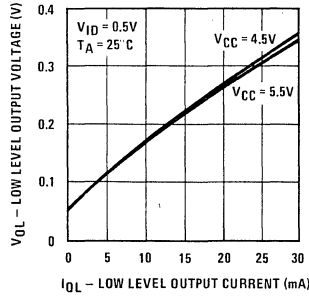
Output Voltage vs Common-Mode Input Voltage



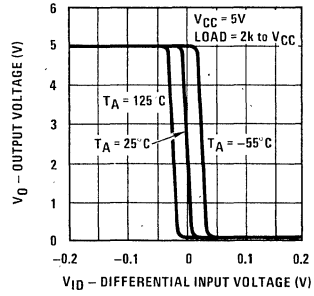
High Level Output Voltage vs Output Current



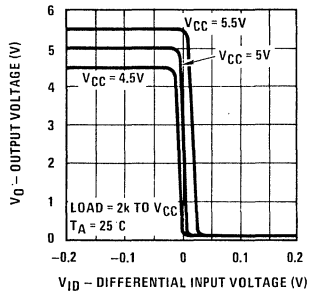
Low Level Output Voltage vs Output Current



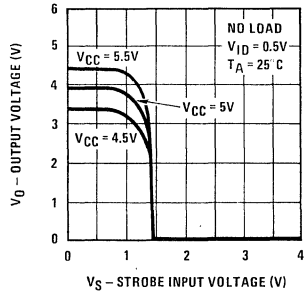
Output Voltage vs Differential Input Voltage



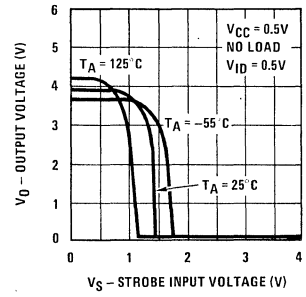
Output Voltage vs Differential Input Voltage



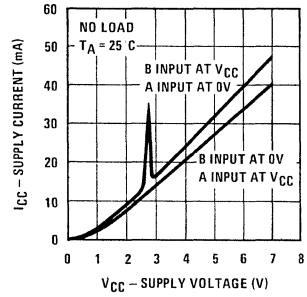
Output Voltage vs Strobe Input Voltage



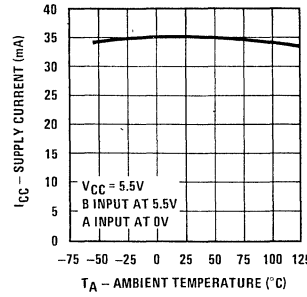
Output Voltage vs Strobe Input Voltage



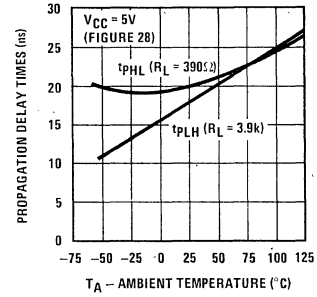
Supply Current (Both Receivers) vs Supply Voltage



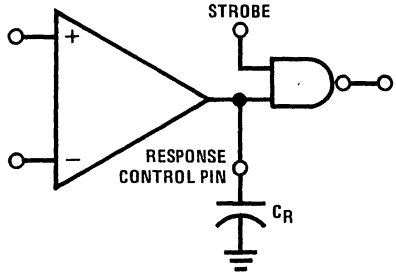
Supply Current (Both Receivers) vs Temperature



Propagation Delay Times vs Temperature

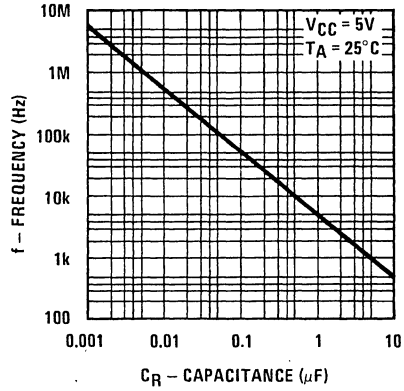


Frequency Response Control

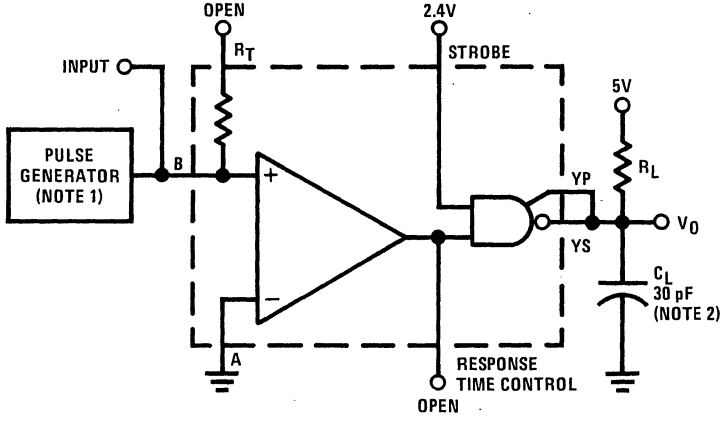


Note. C_R (response control) > 0.01 μF may cause slowing of rise and fall times of the output.

Frequency Response as a Function of Capacitance



AC Test Circuit and Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 500 kHz/t_w = 100 ns.
Note 2: C_L includes probe and test fixture capacitance.

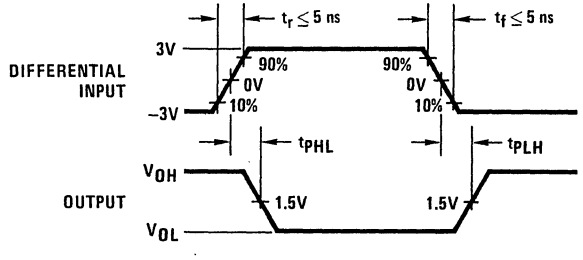


FIGURE 1. Propagation Delay Times

National Semiconductor

Transmission Line Drivers/Receivers

DS55121/DS75121 Dual Line Drivers

General Description

The DS55121/DS75121 are monolithic dual line drivers designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines having impedances from 50 to 500 ohms. Both are compatible with standard TTL logic and supply voltage levels.

The DS55121/DS75121 will drive terminated low impedance lines due to the low-impedance emitter-follower outputs. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

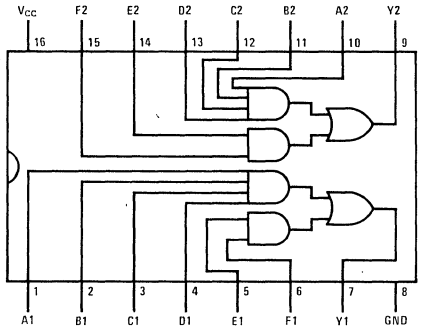
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Designed for digital data transmission over 50 to 500 ohms coaxial cable, strip line, or twisted pair transmission lines
- TTL compatible
- Open emitter-follower output structure for party-line operation
- Short-circuit protection
- AND-OR logic configuration
- High speed (max propagation delay time 20 ns)
- Plug-in replacement for the SN55121/SN75121 and the 8T13

Connection Diagram

Dual-In-Line Package

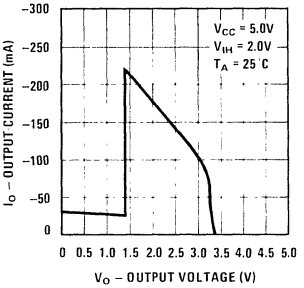


TOP VIEW

Order Number DS55121J, DS75121J or DS75121N
See NS Package J16A or N16A

Typical Performance Characteristics

Output Current vs Output Voltage

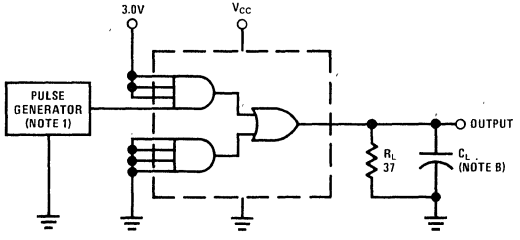


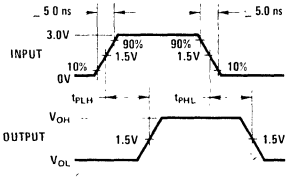
Truth Table

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = high level, L = low level, X = irrelevant

AC Test Circuit and Switching Time Waveforms





Note 1: The pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%, $t_r = t_f = 5.0$ ns.
Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	6.0V
Input Voltage	6.0V
Output Voltage	6.0V
Output Current	−75 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A			
DS55121	−55	+125	°C
DS75121	0	+75	°C

Electrical Characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA			−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
V_{OH}	High Level Output Voltage	V_{IH} = 2.0V, I_{OH} = −75 mA (Note 4)	2.4			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.75V, V_{OH} = 2.0V, T_A = 25°C (Note 4)	−100		−250	mA
I_{OL}	Low Level Output Current	V_{IL} = 0.8V, V_{OL} = 0.4V (Note 4)			−800	μA
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0V, V_O = 3.0V			500	μA
I_{IH}	High Level Input Current	V_I = 4.5V			40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V	−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C			−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open			28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open			60	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 37Ω, (See ac Test Circuit and Switching Time Waveforms)	C_L = 15 pF		11	20	ns
			C_L = 1000 pF		22	50	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 37Ω, (See ac Test Circuit and Switching Time Waveforms)	C_L = 15 pF		8.0	20	ns
			C_L = 1000 pF		20	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55121 and across the 0°C to +70°C range for the DS75121. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor

Transmission Line Drivers/Receivers

DS55122/DS75122 Triple Line Receivers

General Description

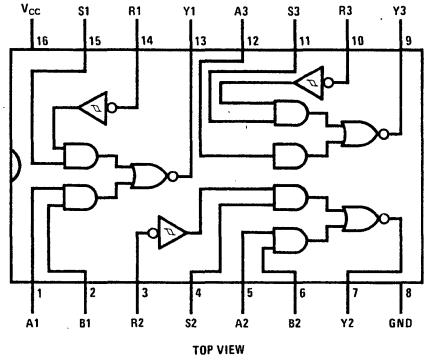
The DS55122/DS75122 are triple line receivers designed for digital data transmission with line impedances from 50Ω to 500Ω. Each receiver has one input with built-in hysteresis which provides a large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS55122/DS75122 are compatible with standard TTL logic and supply voltage levels.

Features

- Built-in input threshold hysteresis
- High speed . . . typical propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Fanout to 10 series 54/74 standard loads
- Plug-in replacement for the SN55122/SN75122 and the 8T14

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS55122J, DS75122J or DS75122N
See NS Package J16A or N16A

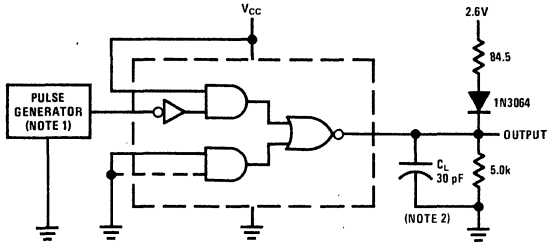
Truth Table

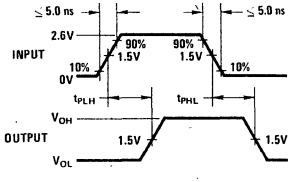
INPUTS A	INPUTS B†	INPUTS R	INPUTS S	OUTPUT Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant

†B input and last two lines of the truth table are applicable to receivers 1 and 2 only.

AC Test Circuit and Switching Time Waveforms





Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%, $t_r = t_f = 5.0$ ns.

Note 2: C_L includes probe and jig capacitance.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	6.0V
Input Voltage	
R Input	6.0V
A, B, or S Input	5.5V
Output Voltage	6.0V
Output Current	±100 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A			
DS55122	−55	+125	°C
DS75122	0	+75	°C
High Level Output Current, I_{OH}		−500	μA
Low Level Output Current, I_{OL}		16	mA

Electrical Characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	A, B, R, or S		2.0			V
V_{IL}	Low Level Input Voltage	A, B, R, or S				0.8	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC} = 5.0V, T_A = 25°C, R, (Note 6)		0.3	0.6		V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA, A, B, or S				−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V, A, B, or S				1.0	mA
V_{OH}	High Level Output Voltage	I_{OH} = −500μA	V_{IH} = 2V, V_{IL} = 0.8V, (Note 4)	2.6			V
			$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(R)}$ = 1.45V, $V_{I(S)}$ = 2.0V, (Note 7)	2.6			V
V_{OL}	Low Level Output Voltage	I_{OL} = 16 mA	V_{IH} = 2.0V, V_{IL} = 0.8V, (Note 4)			0.4	V
			$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(R)}$ = 1.45V, $V_{I(S)}$ = 2.0V, (Note 8)			0.4	V
I_{IH}	High Level Input Current	V_I = 4.5V, A, B, or S				40	μA
		V_I = 3.8V, R				170	μA
I_{IL}	Low Level Input Current	V_I = 0.4V, A, B, or S		0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C, (Note 5)		−50		−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V				72	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125 °C for DS55122 and 0°C to +75°C for DS75122, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

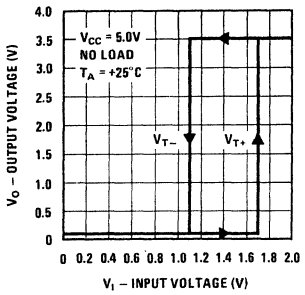
Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 7: Receiver input was at a high level immediately before being reduced to 1.45V.

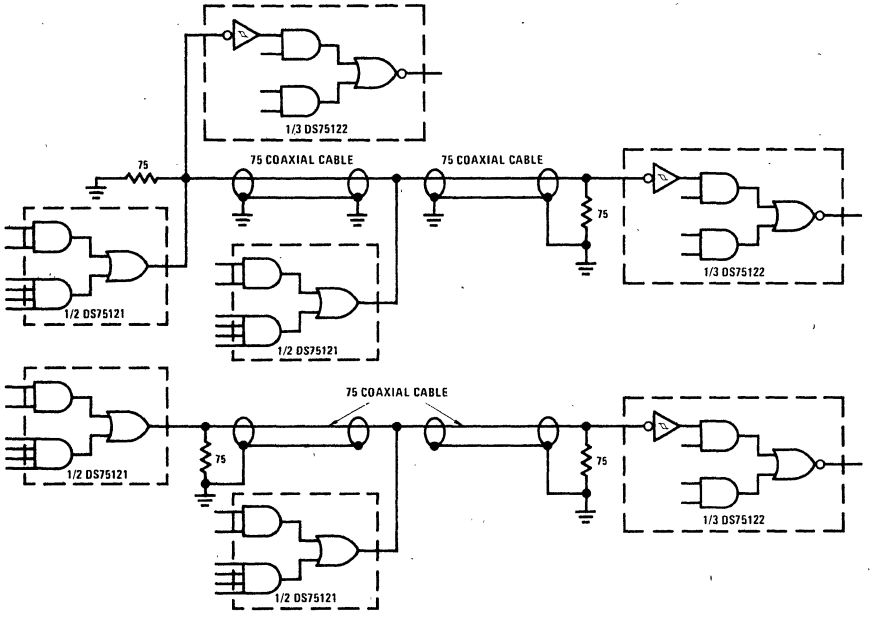
Note 8: Receiver input was at a low level immediately before being raised to 1.45V.

Typical Performance Characteristics

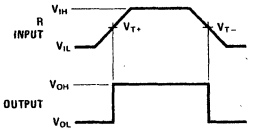
Output Voltage vs Receiver Input Voltage



Typical Applications



Single-Ended Party Line Circuits



The high gain and built-in hysteresis of the DS55122/DS75122 line receivers enable them to be used as Schmitt triggers in squaring up pulses.

Pulse Squaring

National Semiconductor

Transmission Line Drivers/Receivers

DS75123 Dual Line Driver

General Description

The DS75123 is a monolithic dual line driver designed specifically to meet the I/O interface specifications for IBM System 360. It is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the DS75123 enable driving terminated low impedance lines. In addition the outputs are uncommited allowing two or more drivers to drive the same line.

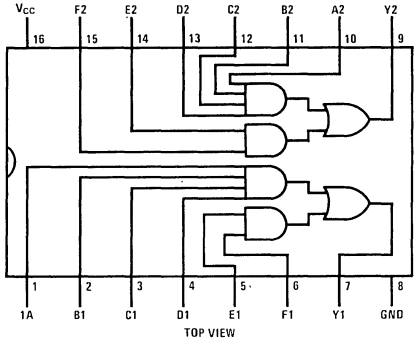
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

Features

- Meet IBM System 360 I/O interface specifications for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or terminated pair transmission lines
- TTL compatible with single 5.0V supply
- 3.11V output at I_{OH} = −59.3 mA
- Open emitter-follower output structure for party-line operation
- Short circuit protection
- AND-OR logic configuration
- Plug-in replacement for the SN75123 and the 8T23

Connection Diagram

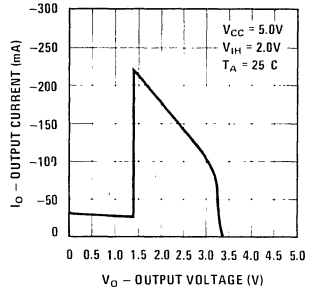
Dual-In-Line Package



Order Number DS75123J or DS75123N
See NS Package J16A or N16A

Typical Performance Characteristics

Output Current vs Output Voltage

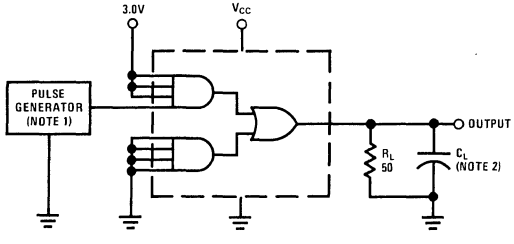


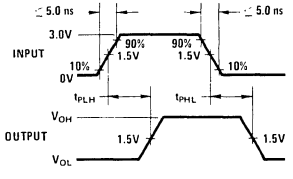
Truth Table

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = high level, L = low level, X = irrelevant

AC Test Circuit and Switching Time Waveforms





Note 1: THE PULSE GENERATORS HAVE THE FOLLOWING CHARACTERISTICS: Z_{OUT} = 50Ω, t_W = 200 ns, DUTY CYCLE = 50%.

Note 2: C_L INCLUDES PROBE AND JIG CAPACITANCE.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	7.0V
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Operating Free-Air Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−100	mA
Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA				−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V				1	mA
V_{OH}	High Level Output Voltage	V_{CC} = 5.0V, V_{IH} = 2.0V, I_{OH} = −59.3 mA, (Note 4)	T_A = 25°C	3.11			V
			T_A = 0°C to +75°C	2.9			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.5V, T_A = 25°C, V_{OH} = 2.0V, (Note 4)		−100		−250	mA
V_{OL}	Low Level Output Voltage	V_{IL} = 0.8V, I_{OL} = −240μA, (Note 4)				0.15	V
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0, V_O = 3.0V				40	μA
I_{IH}	High Level Input Current	V_I = 4.5V				40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C				−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open				28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open				60	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 50Ω, (See ac Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 50Ω, (See ac Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75123, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

National Semiconductor

Transmission Line Drivers/Receivers

DS75124 Triple Line Receiver

General Description

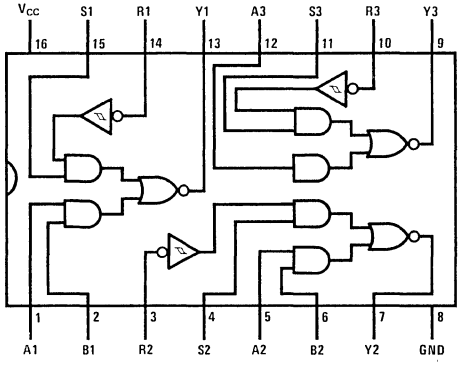
The DS75124 is designed to meet the input/output interface specifications for IBM System 360. It has built-in hysteresis on one input on each of the three receivers to provide large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS75124 is compatible with standard TTL logic and supply voltage levels.

Features

- Built-in input threshold hysteresis
- High speed . . typ propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Plug-in replacement for the SN75124 and the 8T24

Connection Diagram and Truth Table

Dual-In-Line Package



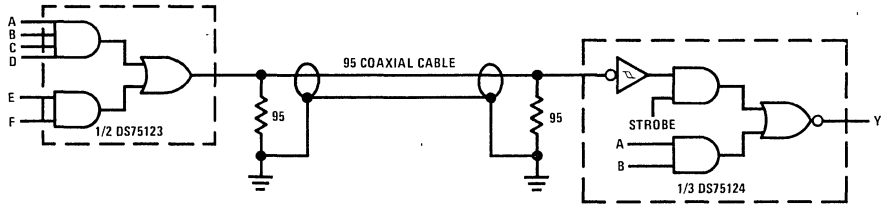
TOP VIEW

Order Number DS75124J or DS75124N
See NS Package J16A or N16A

INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant
†B input and last two lines of the truth table are applicable to receivers 1 and 2 only.

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	
R Input with V_{CC} Applied	7.0V
R Input with V_{CC} not Applied	6.0V
A, B, or S Input	5.5V
Output Voltage	7.0V
Output Current	±100 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−800	μA
Low Level Output Current, I_{OL}		16	mA
Operating Temperature, T_A	0	+75	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	A, B, or S		2.0			V
		R		1.7			V
V_{IL}	Low Level Input Voltage	A, B, or S				0.8	V
		R				0.7	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC} = 5.0V, T_A = 25°C, R, (Note 6)		0.2	0.4		V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA, A, B, or S				−1.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V, A, B, or S				1	mA
		R	V_I = 7.0V			5.0	mA
			V_I = 6.0V, V_{CC} = 0			5.0	mA
V_{OH}	High Level Output Voltage	V_{IH} = V_{IHMIN}, V_{IL} = V_{ILMAX}, I_{OH} = −800μA, (Note 4)		2.6			V
V_{OL}	Low Level Output Voltage	V_{IH} = V_{INMIN}, V_{IL} = V_{ILMAX}, I_{OL} = 16 mA, (Note 4)				0.4	V
I_{IH}	High Level Input Current	V_I = 4.5V, A, B, or S				40	μA
		V_I = 3.11V, R				170	μA
I_{IL}	Low Level Input Current	V_I = 0.4V, A, B, or S		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C, (Note 5)		−50		−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V				72	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

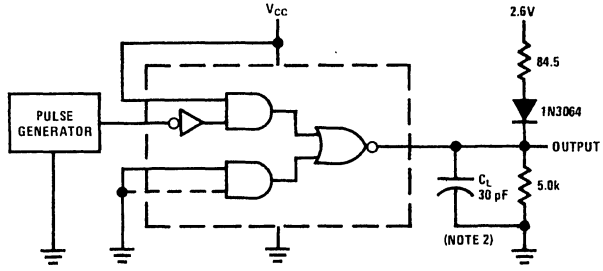
Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75124, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

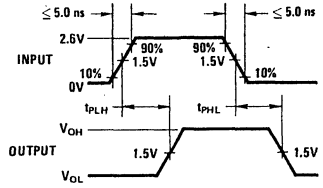
Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

AC Test Circuit and Switching Time Waveforms

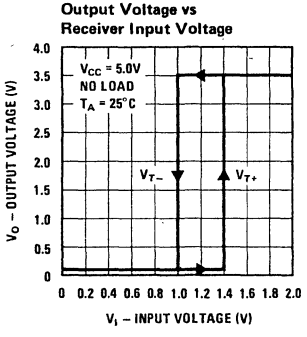


Note 1: THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, DUTY CYCLE = 50%.

Note 2: C_L INCLUDES PROBE AND JIG CAPACITANCE.



Typical Performance Characteristics



National Semiconductor

Transmission Line Drivers/Receivers

DS75125, DS75127 Seven-Channel Line Receivers

General Description

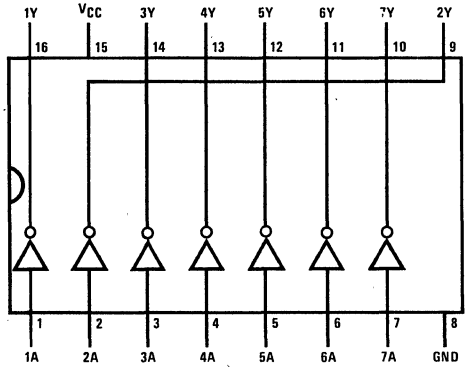
The DS75125 and DS75127 are monolithic seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 input/output interface specifications. Special low-power design and Schottky clamped transistors allow for low supply current requirements while maintaining fast switching speeds and high current TTL outputs. The DS75125 and DS75127 are characterized for operation from 0 °C to 70 °C.

Features

- Meets IBM 360/370 I/O specification
- Input resistance—7 kΩ to 20 kΩ
- Output compatible with TTL
- Schottky-clamped transistors
- Operates from single 5V supply
- High speed—low propagation delay
- Ratio specification for propagation delay time, low-to-high/high-to-low
- Seven channels in one 16-pin package
- Standard V_{CC} and ground positioning on DS75127

Connection Diagrams

DS75125
Dual-In-Line Package

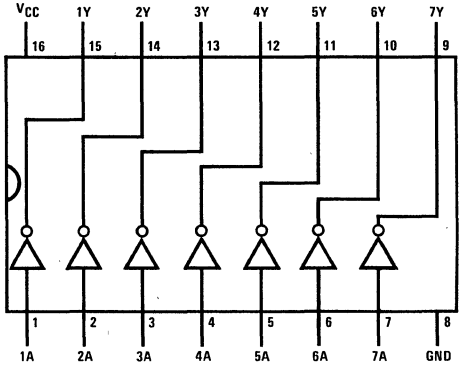


TOP VIEW

logic: $Y = \bar{A}$

Order Number DS75125J or DS75125N
See NS Package J16A or N16A

DS75127
Dual-In-Line Package



TOP VIEW

logic: $Y = \bar{A}$

Order Number DS75127J or DS75127N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC} (Note 1)	7V
Input Voltage Range	
DS75125	−0.15V to 7V
DS75127	−2V to 7V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.9 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	4.5	5	5.5	V
High-Level Output Current, I_{OH}			−0.4	mA
Low-Level Output Current, I_{OL}			16	mA
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (Note 3)

Parameter	Conditions	Min	Typ (Note 5)	Max	Units
V_{IH} High-Level Input Voltage		1.7			V
V_{IL} Low-Level Input Voltage				0.7	V
V_{OH} High-Level Output Voltage	$V_{CC}=4.5V$, $V_{IL}=0.7V$, $I_{OH}=-0.4$ mA	2.4	3.1		V
V_{OL} Low-Level Output Voltage	$V_{CC}=4.5V$, $V_{IH}=1.7V$, $I_{OL}=16$ mA		0.4	0.5	V
I_{IH} High-Level Input Current	$V_{CC}=5.5V$, $V_I=3.11V$		0.3	0.42	mA
I_{IL} Low-Level Input Current	$V_{CC}=5.5V$, $V_I=0.15V$			−0.24	mA
I_{OS} Short-Circuit Output Current (Note 4)	$V_{CC}=5.5V$, $V_O=0$	−18		−60	mA
r_I Input Resistance	$V_{CC}=4.5V$, 0V, or Open, $\Delta V_I=0.15V$ to 4.15V	7		20	kΩ
I_{CC} Supply Current	$V_{CC}=5.5V$, $I_{OH}=-0.4$ mA, All Inputs at 0.7V		15	25	mA
	$V_{CC}=5.5V$, $I_{OL}=16$ mA, All Inputs at 4V		28	47	mA

Switching Characteristics $V_{CC}=5V$, $T_A=25°C$

Parameter	Conditions	Min	Typ	Max	Units
t_{PLH} Propagation Delay Time, Low-to-High-Level Output	$R_L=400\Omega$, $C_L=50$ pF, See *Figure 1*	7	14	25	ns
t_{PHL} Propagation Delay Time, High-to-Low-Level Output		10	18	30	ns
$\frac{t_{PLH}}{t_{PHL}}$ Ratio of Propagation Delay Times		0.5	0.8	1.3	ns
t_{TLH} Transition Time, Low-to-High-Level Output		1	7	12	ns
t_{THL} Transition Time, High-to-Low-Level Output		1	3	12	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

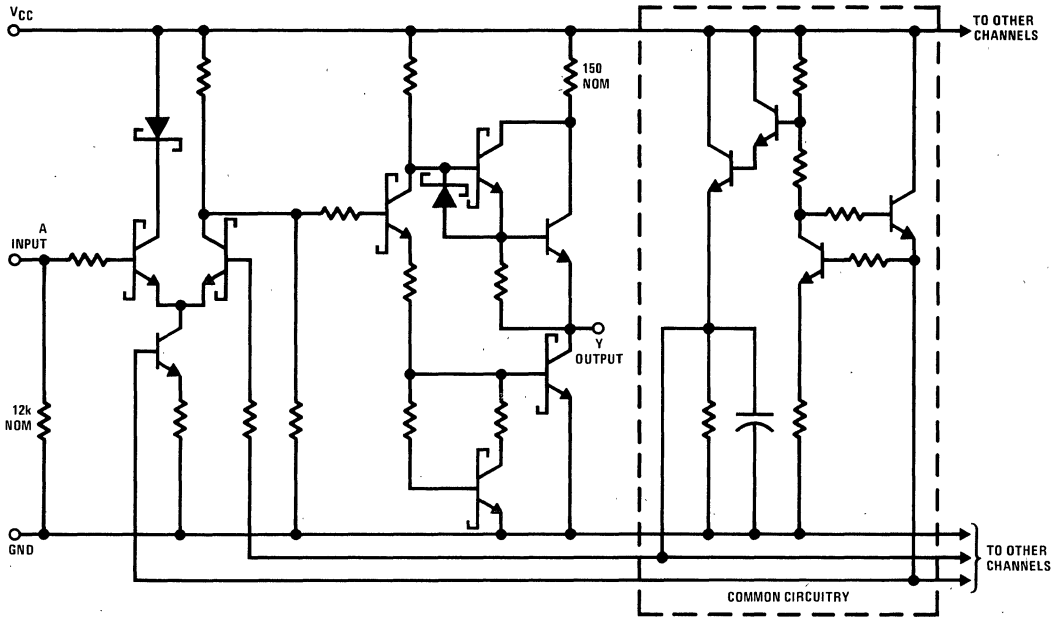
Note 2: For operation above 25°C free-air temperature, refer to Thermal Ratings for ICs in Section 12 of Interface Databook.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

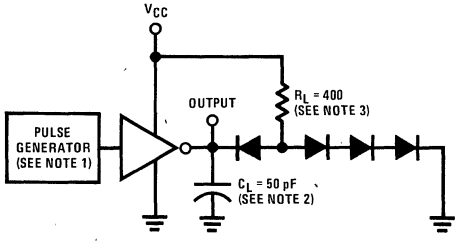
Note 4: Only one output should be shorted at a time.

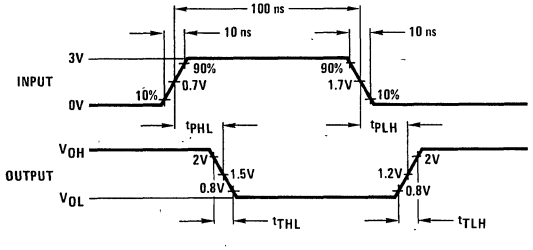
Note 5: All typical values are at $V_{CC}=5V$, $T_A=25°C$.

Schematic (each receiver)



AC Test Circuit and Switching Time Waveforms



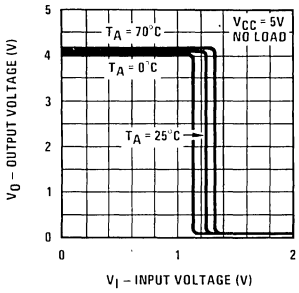


Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, PRR = 5 MHz.
Note 2: C_L includes probe and jig capacitance.
Note 3: All diodes are 1N3064 or equivalent.

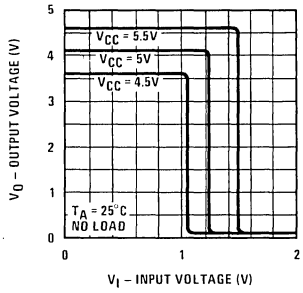
FIGURE 1

Typical Performance Characteristics

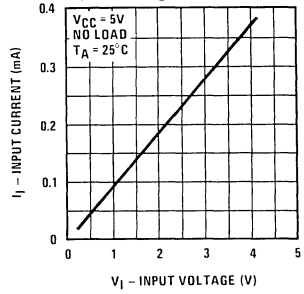
Voltage Transfer Characteristics



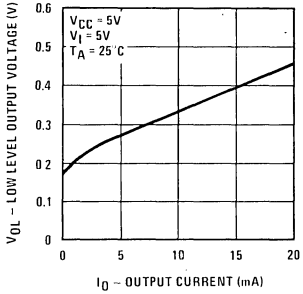
Voltage Transfer Characteristics



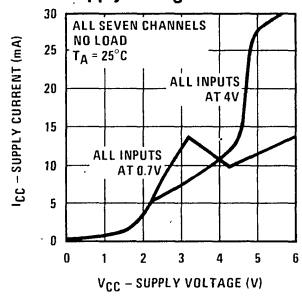
Input Current vs Input Voltage



Low-Level Output Voltage vs Output Current



Supply Current vs Supply Voltage



National Semiconductor

DS75128, DS75129 Eight-Channel Line Receivers

General Description

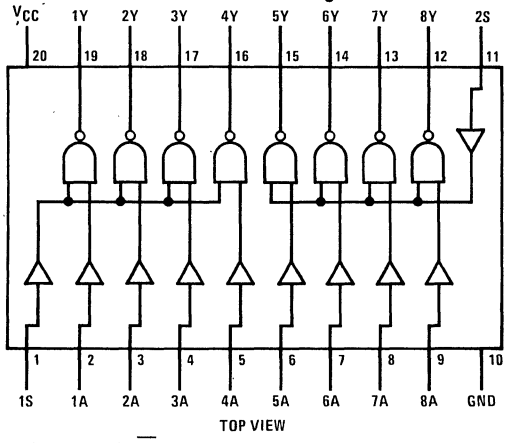
The DS75128 and DS75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four receivers. The DS75128 has an active-high strobe; the DS75129 has an active-low strobe. Special low-power design and Schottky-diode-clamped transistors allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The DS75128 and DS75129 are characterized for operation from 0 °C to 70 °C.

Features

- Meets IBM 360/370 I/O specification
- Input resistance — 7 kΩ to 20 kΩ
- Output compatible with TTL
- Schottky-clamped transistors
- Operates from a single 5V supply
- High speed — low propagation delay
- Ratio specification — t_{PLH}/t_{PHL}
- Common strobe for each group of four receivers
- DS75128 strobe — active-high
  DS75129 strobe — active-low

Connection Diagrams

DS75128
Dual-In-Line Package

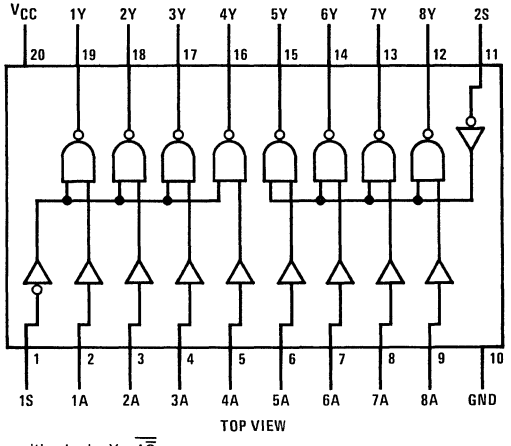


TOP VIEW

positive logic: $Y = \overline{AS}$

Order Number DS75128J or DS75128N
See NS Package J20A or N20A

DS75129
Dual-In-Line Package



TOP VIEW

positive logic: $Y = \overline{AS}$

Order Number DS75129J or DS75129N
See NS Package J20A or N20A

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (Note 1)	7V
A Input Voltage Range	−0.15V to 7V
Strobe Input Voltage	7V
Maximum Power Dissipation* at 25°C	
Cavity Package	1564 mW
Molded Package	1687 mW
Operating Free-Air Temperature Range	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature 1/16 inch from Case for 60 Seconds: J Package	300°C
Lead Temperature 1/16 inch from Case for 10 Seconds: N Package	260°C

*Derate cavity package 10.4 mW/°C above 25°C; derate molded package 13.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{CC}	4.5	5.0	5.5	V
High-Level Output Current, I_{OH}			−0.4	mA
Low-Level Output Current, I_{OL}			16	mA
Operating Free-Air Temperature, T_A	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (Note 3)

Parameter			Conditions	Min	Typ (Note 5)	Max	Units
V_{IH} High-Level Input Voltage		A		1.7			V
		S		2			
V_{IL} Low-Level Input Voltage		A				0.7	V
		S				0.7	
V_{OH} High-Level Output Voltage			V_{CC} = 4.5V, V_{IL} = 0.7V, I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL} Low-Level Output Voltage			V_{CC} = 4.5V, V_{IH} = 1.7V, I_{OL} = 16 mA		0.4	0.5	V
V_I Input Clamp Voltage		S	V_{CC} = 4.5V, I_I = −18 mA			−1.5	V
I_{IH} High-Level Input Current		A	V_{CC} = 5.5V, V_I = 3.11V		0.3	0.42	mA
		S	V_{CC} = 5.5V, V_I = 2.7V			20	μA
I_{IL} Low-Level Input Current		A	V_{CC} = 5.5V, V_I = 0.15V			−0.24	mA
		S	V_{CC} = 5.5V, V_I = 0.4V			−0.4	
I_{OS} Short-Circuit Output Current (Note 4)			V_{CC} = 5.5V, V_O = 0	−18		−60	mA
r_I Input Resistance			V_{CC} = 4.5V, 0V, or Open, ΔV_I = 0.15V to 4.15V	7		20	kΩ
I_{CC} Supply Current	DS75128		V_{CC} = 5.5V, Strobe at 2.4V, All A Inputs at 0.7V		19	31	mA
	DS75129		V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 0.7V		19	31	
	DS75128		V_{CC} = 5.5V, Strobe at 2.4V, All A Inputs at 4V		32	53	
	DS75129		V_{CC} = 5.5V, Strobe at 0.4V, All A Inputs at 4V		32	53	

Switching Characteristics V_{CC} = 5V, T_A = 25°C

Parameter			Conditions	DS75128 Min	DS75128 Typ	DS75128 Max	DS75129 Min	DS75129 Typ	DS75129 Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	A	R_L = 400Ω, C_L = 50 pF, See *Figure 1*	7	14	25	7	14	25	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output	A		10	18	30	10	18	30	ns
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	S			26	40		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output	S			22	35		16	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of Propagation Delay Times	A		0.5	0.8	1.3	0.5	0.8	1.3	
t_{TLH}	Transition Time, Low-to-High-Level Output			1	7	12	1	7	12	ns
t_{THL}	Transition Time, High-to-Low-Level output			1	3	12	1	3	12	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

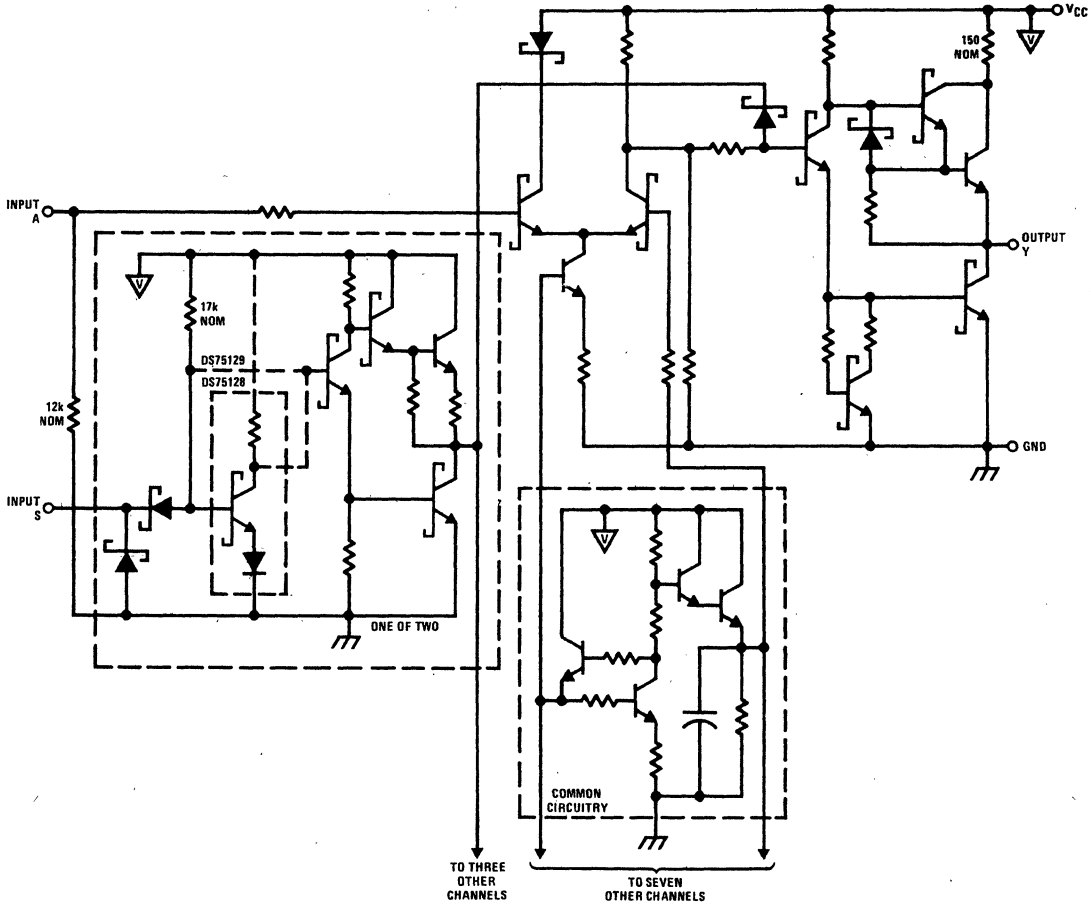
Note 2: For operation above 25°C free-air temperature, refer to Thermal Ratings for ICs, Section 12, Interface Databook.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

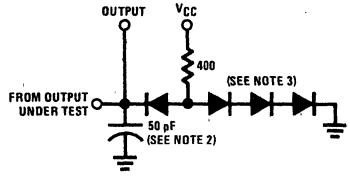
Note 4: Only one output should be shorted at a time.

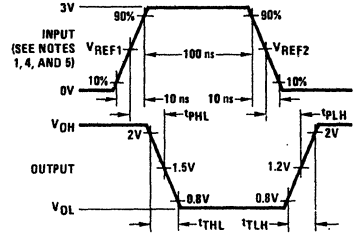
Note 5: All typical values are at V_{CC} = 5V, T_A = 25°C.

Schematic Diagram (each receiver)



AC Test Circuit and Switching Time Waveforms





Note 1: Input pulses are supplied by a generator having the following characteristics: $Z_O = 50\Omega$, PRR = 5 MHz.

Note 2: Includes probe and jig capacitance.

Note 3: All diodes are 1N3064 or equivalent.

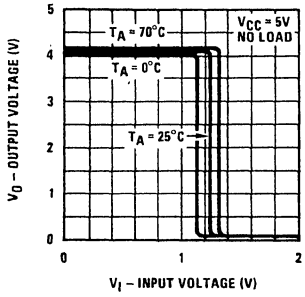
Note 4: The strobe inputs of DS75129 are in-phase with the output.

Note 5: $V_{REF1} = 0.7V$ and $V_{REF2} = 1.7V$ for testing data (A) inputs, $V_{REF1} = V_{REF2} = 1.3V$ for strobe inputs.

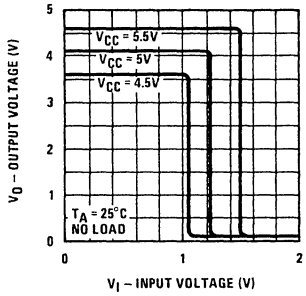
FIGURE 1

Typical Characteristics

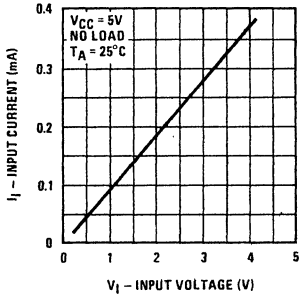
Voltage Transfer Characteristics From A Inputs



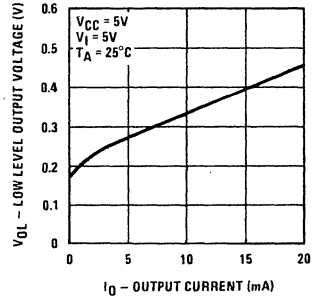
Voltage Transfer Characteristics From A Inputs



Input Current vs Input Voltage, A Inputs



Low-Level Output Voltage vs Output Current



National Semiconductor

Transmission Line Drivers/Receivers

DS75150 Dual Line Driver

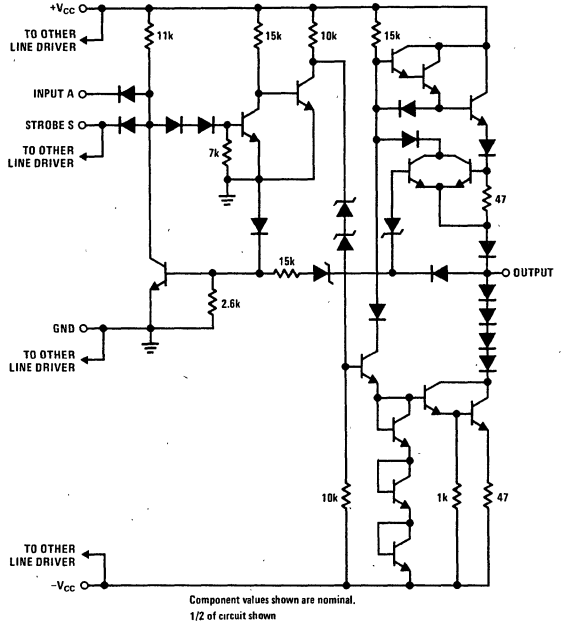
General Description

The DS75150 is a dual monolithic line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and LS families. Operation is from −12V and +12V power supplies.

Features

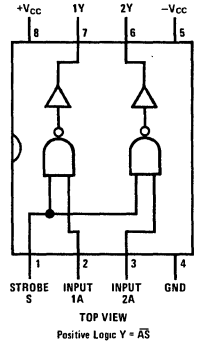
- Withstands sustained output short-circuit to any low impedance voltage between −25V and +25V
- 2μs max transition time through the −3V to +3V transition region under full 2500 pF load
- Inputs compatible with most TTL and LS families
- Common strobe input
- Inverting output
- Slew rate can be controlled with an external capacitor at the output
- Standard supply voltages ±12V

Schematic and Connection Diagrams



Component values shown are nominal.
1/2 of circuit shown

Dual-In-Line Package



TOP VIEW

Positive Logic $Y = \overline{AS}$

Order Number DS75150J-8 or DS75150N
See NS Package J08A or N08A

Absolute Maximum Ratings (Note 1)

Supply Voltage $+V_{CC}$	15V
Supply Voltage $-V_{CC}$	−15V
Input Voltage	15V
Applied Output Voltage	±25V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage ($+V_{CC}$)	10.8	13.2	V
Supply Voltage ($-V_{CC}$)	−10.8	−13.2	V
Input Voltage (V_I)	0	+5.5	V
Output Voltage (V_O)		±15	V
Operating Ambient Temperature Range (T_A)	0	+70	°C

DC Electrical Characteristics (Notes 2, 3, 4 and 5)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low-Level Input Voltage	*(Figure 2)*				0.8	V
V_{OH}	High-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −13.2V, V_{IL} = 0.8V, R_L = 3 kΩ to 7 kΩ, *(Figure 2)*		5	8		V
V_{OL}	Low-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −10.8V, V_{IH} = 2V, R_L = 3 kΩ to 7 kΩ, *(Figure 1)*			−8	−5	V
I_{IH}	High-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, Data Input V_I = 2.4V, *(Figure 3)*			1	10	μA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, Strobe Input V_I = 2.4V, *(Figure 3)*			2	20	μA
I_{IL}	Low-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, Data Input V_I = 0.4V, *(Figure 3)*			−1	−1.6	mA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, Strobe Input V_I = 0.4V, *(Figure 3)*			−2	−3.2	mA
I_{OS}	Short-Circuit Output Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, *(Figure 4)*, Note 4	V_O = 25V		2	5	mA
			V_O = −25V		−3	−6	mA
			V_O = 0V, V_I = 3V		15	30	mA
			V_O = 0V, V_I = 0V		−15	−30	mA
$+I_{CCH}$	Supply Current From $+V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			10	22	mA
$-I_{CCH}$	Supply Current From $-V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−1	−10	mA
$+I_{CCL}$	Supply Current From $+V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			8	17	mA
$-I_{CCL}$	Supply Current From $-V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−9	−20	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75150. All typical values are for T_A = 25°C and $+V_{CC}$ = 12V, $-V_{CC}$ = −12V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5V is the maximum, the typical value is a more-negative voltage.

AC Electrical Characteristics ($+V_{CC}$ = 12V, $-V_{CC}$ = −12V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.4	2	μs
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.5	2	μs
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		40		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		20		ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		60		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		45		ns

DC Test Circuits

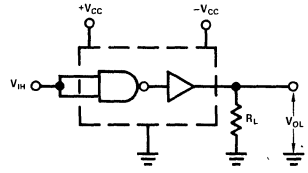
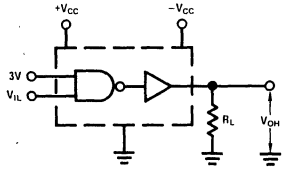
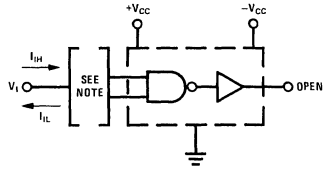


FIGURE 1. V_{IH}, V_{OL}



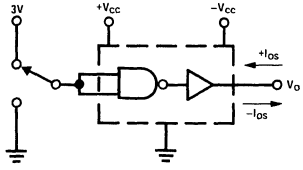
Each input is tested separately.

FIGURE 2. V_{IL}, V_{OH}



Note: When testing I_{IH}, the other input is at 3V; when testing I_{IL}, the other input is open.

FIGURE 3. I_{IH}, I_{IL}



I_{OS} is tested for both input conditions at each of the specified output conditions.

FIGURE 4. I_{OS}

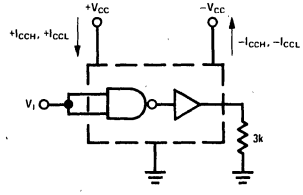
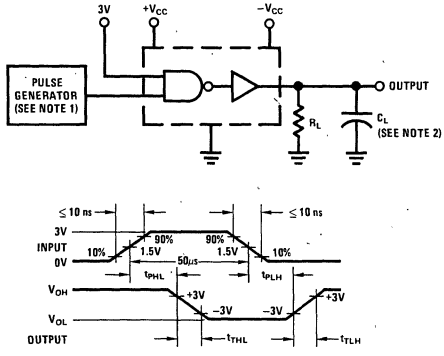


FIGURE 5. I_{CCH+}, I_{CCH-}, I_{CCL+}, I_{CCL-}

AC Test Circuit and Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 6.

Typical Performance Characteristics

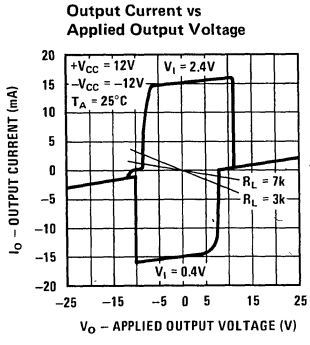


FIGURE 7.

DS75154 Quad Line Receiver

General Description

The DS75154 is a quad monolithic line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are in relatively short, single-line, point-to-point data transmission systems and for level translators. Operation is normally from a single 5V supply; however, a built-in option allows operation from a 12V supply without the use of additional components. The output is compatible with most TTL and LS circuits when either supply voltage is used.

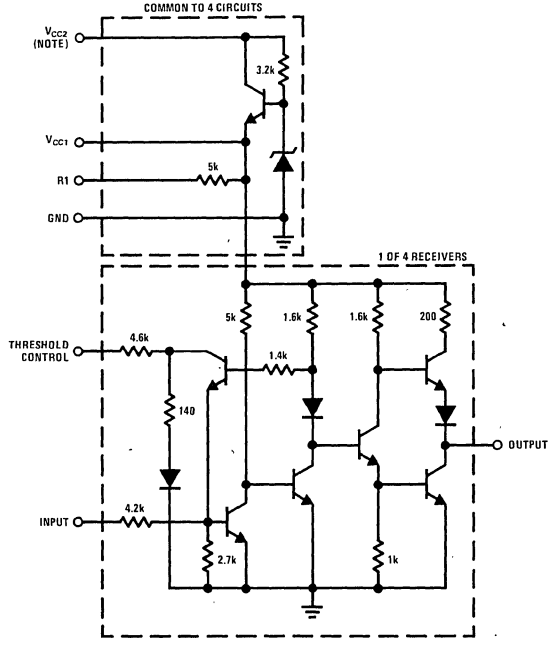
In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

Features

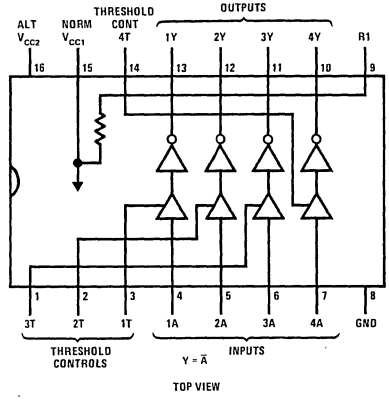
- Input resistance, 3 kΩ to 7 kΩ over full RS-232C voltage range
- Input threshold adjustable to meet "fail-safe" requirements without using external components
- Inverting output compatible with TTL or LS
- Built-in hysteresis for increased noise immunity
- Output with active pull-up for symmetrical switching speeds
- Standard supply voltage—5V or 12V

Schematic and Connection Diagrams



Note: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

Dual-In-Line Package



TOP VIEW

Order Number DS75154J or DS75154N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Normal Supply Voltage (Pin 15),(V_{CC1})	7V
Alternate Supply Voltage (Pin 16),(V_{CC2})	14V
Input Voltage	±25V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (Pin 15),(V_{CC1})	4.5	5.5	V
Alternate Supply Voltage (Pin 16) (V_{CC2})	10.8	13.2	V
Input Voltage		±15	V
Temperature, (T_A)	0	+70	°C

Electrical Characteristics (Notes 2, 3 and 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage	*(Figure 1)*		3			V
V_{IL}	Low-Level Input Voltage	*(Figure 1)*				−3	V
V_{T+}	Positive-Going Threshold Voltage	*(Figure 1)*	Normal Operation	0.8	2.2	3	V
			Fail-Safe Operation	0.8	2.2	3	V
V_{T-}	Negative-Going Threshold Voltage	*(Figure 1)*	Normal Operation	−3	−1.1	0	V
			Fail-Safe Operation	0.8	1.4	3	V
$V_{T+}-V_{T-}$	Hysteresis	*(Figure 1)*	Normal Operation	0.8	3.3	6	V
			Fail-Safe Operation	0	0.8	2.2	V
V_{OH}	High-Level Output Voltage	I_{OH} = −400μA, *(Figure 1)*		2.4	3.5		V
V_{OL}	Low-Level Output Voltage	I_{OL} = 16 mA, *(Figure 1)*			0.23	0.4	V
r_I	Input Resistance	*(Figure 2)*	ΔV_I = −25V to −14V	3	5	7	kΩ
			ΔV_I = −14V to −3V	3	5	7	kΩ
			ΔV_I = −3V to +3V	3	6		kΩ
			ΔV_I = 3V to 14V	3	5	7	kΩ
			ΔV_I = 14V to 25V	3	5	7	kΩ
$V_{I(OPEN)}$	Open-Circuit Input Voltage	I_I = 0, *(Figure 3)*		0	0.2	2	V
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC1} = 5.5V, V_I = −5V, *(Figure 4)*		−10	−20	−40	mA
I_{CC1}	Supply Current From V_{CC1}	V_{CC1} = 5.5V, T_A = 25°C, *(Figure 5)*			20	35	mA
I_{CC2}	Supply Current From V_{CC2}	V_{CC2} = 13.2V, T_A = 25°C, *(Figure 5)*			23	40	mA

Switching Characteristics (V_{CC1} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF, R_L = 390Ω, *(Figure 6)*		22		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 50 pF, R_L = 390Ω, *(Figure 6)*		20		ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 50 pF, R_L = 390Ω *(Figure 6)*		9		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 50 pF, R_L = 390Ω, *(Figure 6)*		6		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

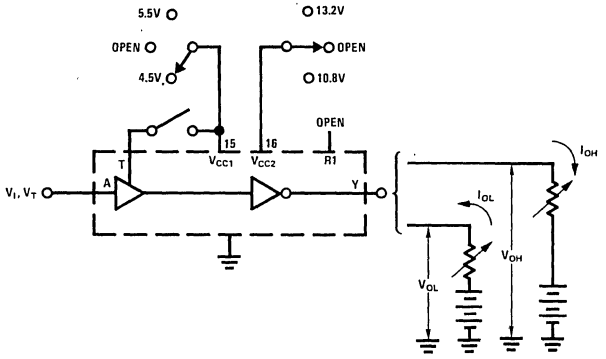
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75154. All typical values are for T_A = 25°C and V_{CC1} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3V is the maximum, the minimum limit is a more-negative voltage.

Note 5: Only one output at a time should be shorted.

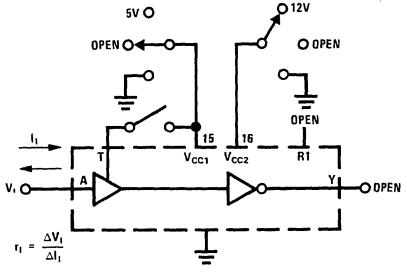
DC Test Circuits and Truth Tables



TEST	MEASURE	A	T	Y	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open-Circuit Input (fail-safe)	V_{OH} V_{OH}	Open Open	Open Open	I_{OH} I_{OH}	4.5V Open	Open 10.8V
V_{T+} min, V_{T-} (fail-safe)	V_{OH} V_{OH}	0.8V 0.8V	Open Open	I_{OH} I_{OH}	5.5V Open	Open 13.2V
V_{T+} min (Normal)	V_{OH} V_{OH}	Note 1 Note 1	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IL} max, V_{T-} min (Normal)	V_{OH} V_{OH}	−3V −3V	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IH} min, V_{T+} max, V_{T-} max (fail-safe)	V_{OL} V_{OL}	3V 3V	Open Open	I_{OL} I_{OL}	4.5V Open	Open 10.8V
V_{IH} min, V_{T+} max (Normal)	V_{OL} V_{OL}	3V 3V	Pin 15 Pin 15	I_{OL} I_{OL}	4.5V and T T	Open 10.8V
V_{T-} max (Normal)	V_{OL} V_{OL}	Note 2 Note 2	Pin 15 Pin 15	I_{OL} I_{OL}	5.5V and T T	Open 13.2V

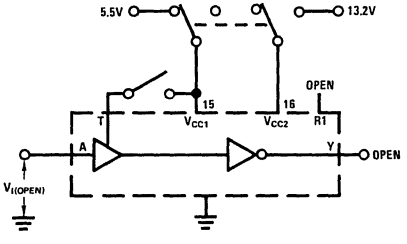
Note 1: Momentarily apply −5V, then 0.8V.
Note 2: Momentarily apply 5V, then ground.

FIGURE 1. V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}



T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5V	Open
Open	Gnd	Open
Open	Open	Open
Pin 15	T and 5V	Open
Gnd	Gnd	Open
Open	Open	12V
Open	Open	Gnd
Pin 15	T	12V
Pin 15	T	Gnd
Pin 15	T	Open

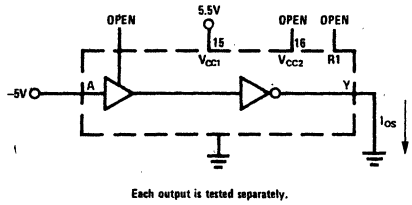
FIGURE 2. r_I



T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5.5V	Open
Pin 15	5.5V	Open
Open	Open	13.2V
Pin 15	T	13.2V

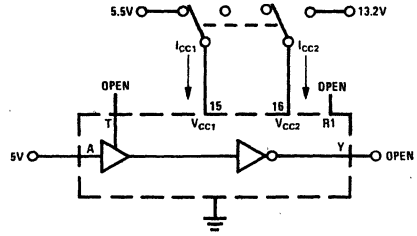
FIGURE 3. $V_{I(OPEN)}$

DC Test Circuits (Continued)



Each output is tested separately.

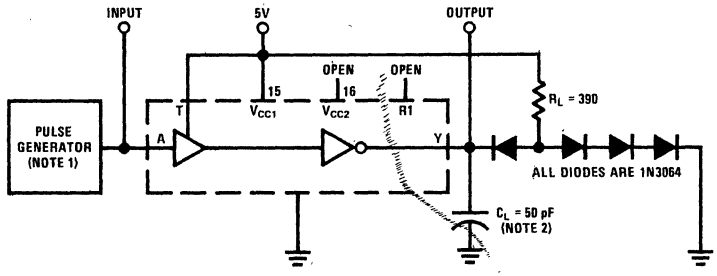
FIGURE 4. I_{OS}

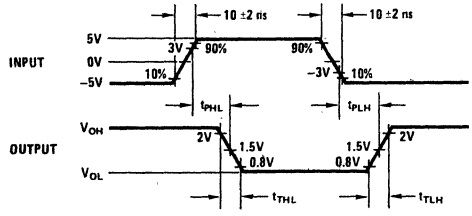


All four line receivers are tested simultaneously.

FIGURE 5. I_{CC}

AC Test Circuit and Switching Time Waveforms

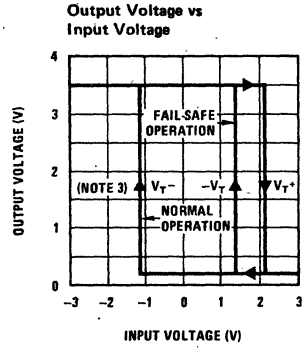




Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, t_W = 200 ns, duty cycle ≤ 20%.
Note 2: C_L includes probe and jig capacitance

FIGURE 6.

Typical Performance Characteristics



National Semiconductor

Transmission Line Drivers/Receivers

DS7820/DS8820 Dual Line Receiver

General Description

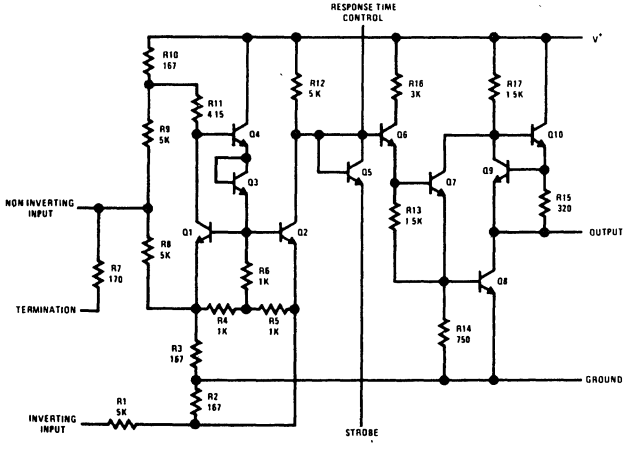
The DS7820, specified from −55°C to +125°C, and the DS8820, specified from 0°C to +70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with TTL or LS integrated circuits.

Features

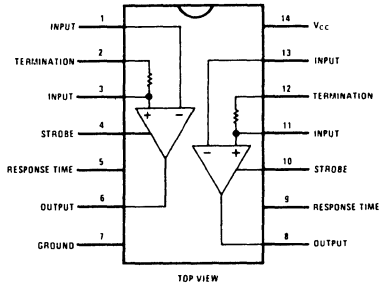
- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Each channel can be strobed independently
- High input resistance
- Fan out of two with TTL integrated circuits

The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

Schematic and Connection Diagrams

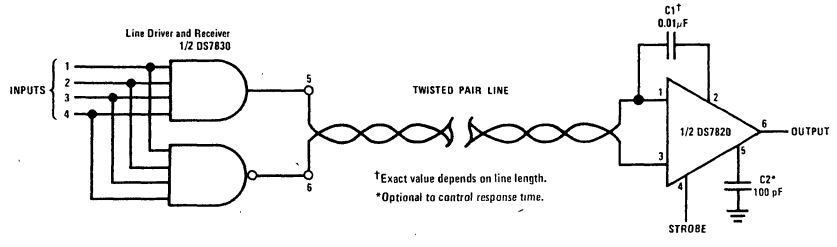


Dual-In-Line Package



Order Number DS7820J, DS8820J or DS8820N
See NS Package J14A or N14A

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage	8.0V
Input Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	25 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7820	4.5	5.5	V
DS8820	4.75	5.25	V
Temperature (T_A)			
DS7820	−55	+125	°C
DS8820	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{TH}	Input Threshold Voltage	$V_{CM} = 0$	−0.5	0	0.5	V
		$-15V \leq V_{CM} \leq 15V$	−1.0	0	1.0	V
V_{OH}	High Output Level	$I_{OUT} \leq 0.2$ mA	2.5		5.5	V
V_{OL}	Low Output Level	$I_{SINK} \leq 3.5$ mA	0		0.4	V
R_I^-	Inverting Input Resistance		3.6	5.0		kΩ
R_I^+	Non-Inverting Input Resistance		1.8	2.5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$	120	170	250	Ω
t_r	Response Time	$C_{DELAY} = 0$		40		ns
		$C_{DELAY} = 100$ pF		150		ns
I_{ST}	Strobe Current	$V_{STROBE} = 0.4V$		−1.0	−1.4	mA
		$V_{STROBE} = 5.5V$			5.0	μA
I_{CC}	Power Supply Current	$V_{IN} = 15V$		3.2	6.0	mA
		$V_{IN} = 0$		5.8	10.2	mA
		$V_{IN} = -15V$		8.3	15.0	mA
I_{IN}^+	Non-Inverting Input Current	$V_{IN} = 15V$		5.0	7.0	mA
		$V_{IN} = 0$	−1.6	−1.0		mA
		$V_{IN} = -15V$	−9.8	−7.0		mA
I_{IN}^-	Inverting Input Current	$V_{IN} = 15V$		3.0	4.2	mA
		$V_{IN} = 0$		0	−0.5	mA
		$V_{IN} = -15V$	−4.2	−3.0		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

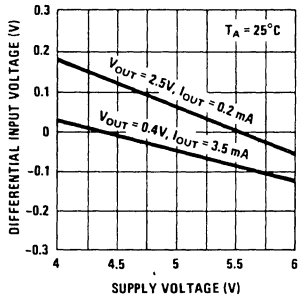
Note 2: These specifications apply for $4.5V \leq V_{CC} \leq 5.5V$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq +125°C$ for the DS7820 or $0°C \leq T_A \leq +70°C$ for the DS8820 unless otherwise specified; typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0$ unless stated differently.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

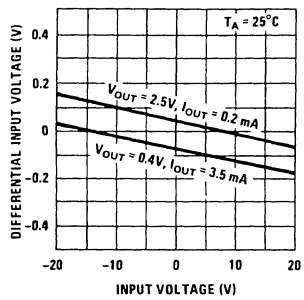
Note 4: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

Typical Performance Characteristics (Note 3)

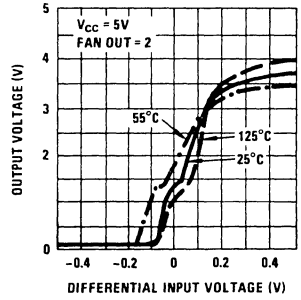
Supply Voltage Sensitivity



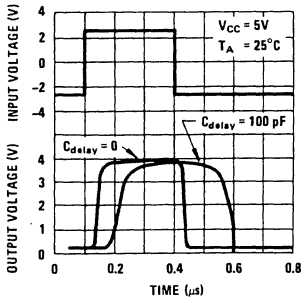
Common Mode Rejection



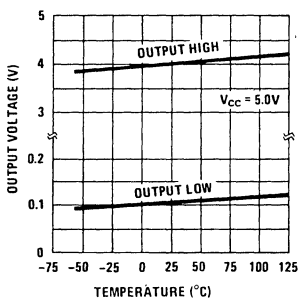
Transfer Function



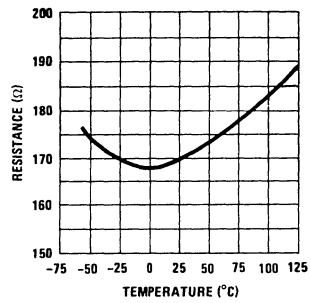
Response Time



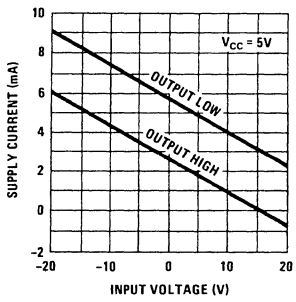
Output Voltage Levels



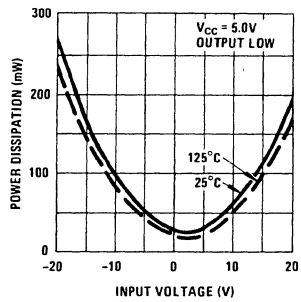
Termination Resistance



Positive Supply Current



Internal Power Dissipation



National Semiconductor

Transmission Line Drivers/Receivers

DS7820A/DS8820A Dual Line Receiver

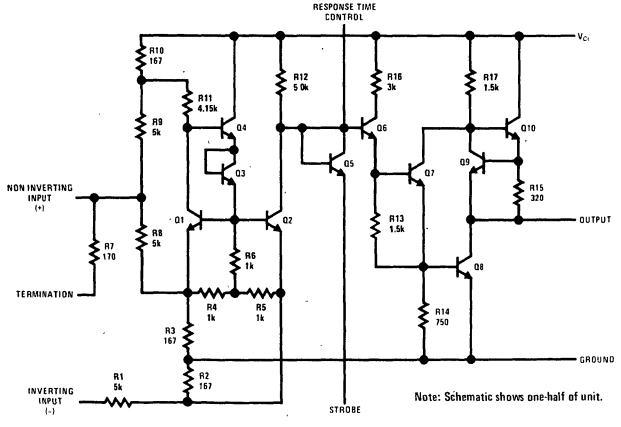
General Description

The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with TTL or LS integrated circuits. Some important design features include:

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

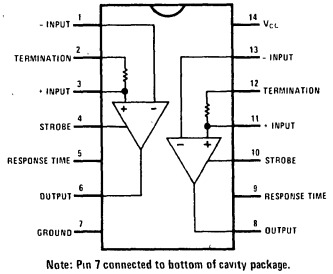
The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (−55°C to 125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

Schematic and Connection Diagrams



Note: Schematic shows one-half of unit.

Dual-In-Line Package



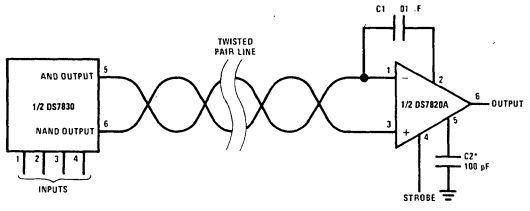
Note: Pin 7 connected to bottom of cavity package.

TOP VIEW

Order Number DS7820AJ, DS8820AJ or DS8820AN
See NS Package J14A or N14A

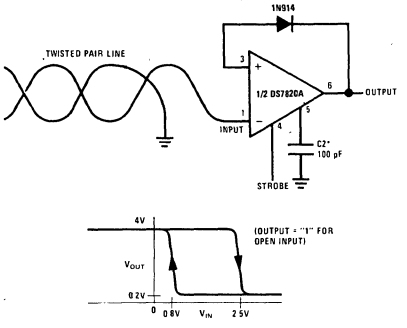
Typical Applications

Differential Line Driver and Receiver



*Optional to control response time.

Single Ended (EIA-RS232C) Receiver with Hysteresis



Absolute Maximum Ratings (Note 1)

Supply Voltage	8.0V
Common-Mode Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Storage Temperature Range	−65°C to 150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 10 sec)	300°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7820A	4.5	5.5	V
DS8820A	4.75	5.25	V
Temperature (T_A)			
DS7820A	−55	+125	°C
DS8820A	0	+70	°C

Electrical Characteristics (Notes 2, 3, and 4)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	I_{OUT} = −400μA, $V_{OUT} \geq 2.5V$	$-3V \leq V_{CM} \leq +3V$			0.06	0.5	V
			$-15V \leq V_{CM} \leq +15V$			0.06	1.0	V
		I_{OUT} = +16 mA, $V_{OUT} \leq 0.4V$	$-3V \leq V_{CM} \leq +3V$			−0.08	−0.5	V
			$-15V \leq V_{CM} \leq +15V$			−0.08	−1.0	V
R_I^-	Inverting Input Resistance	$-15V \leq V_{CM} \leq +15V$			3.6	5		kΩ
R_I^+	Non-Inverting Input Resistance	$-15V \leq V_{CM} \leq +15V$			1.8	2.5		kΩ
R_T	Line Termination Resistance	T_A = 25°C			120	170	250	Ω
I_I^-	Inverting Input Current	V_{CM} = 15V				3.0	4.2	mA
		V_{CM} = 0V				0	−0.5	mA
		V_{CM} = −15V				−3.0	−4.2	mA
I_I^+	Non-Inverting Input Current	V_{CM} = 15V				5.0	7.0	mA
		V_{CM} = 0V				−1.0	−1.6	mA
		V_{CM} = −15V				−7.0	−9.8	mA
I_{CC}	Power Supply Current One Side Only	I_{OUT} = Logical "0"	V_{DIFF} = −1V	V_{CM} = 15V		3.9	6.0	mA
				V_{CM} = −15V		9.2	14.0	mA
			V_{DIFF} = −0.5V,	V_{CM} = 0V		6.5	10.2	mA
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −400μA, V_{DIFF} = 1V			2.5	4.0	5.5	V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = +16 mA, V_{DIFF} = −1V			0	0.22	0.4	V
V_{SH}	Logical "1" Strobe Input Voltage	I_{OUT} = +16 mA, $V_{OUT} \leq 0.4V$, V_{DIFF} = −3V			2.1			V
V_{SL}	Logical "0" Strobe Input Voltage	I_{OUT} = −400μA, $V_{OUT} \geq 2.5V$, V_{DIFF} = −3V					0.9	V
I_{SH}	Logical "1" Strobe Input Current	V_{STROBE} = 5.5V, V_{DIFF} = 3V				0.01	5.0	μA
I_{SL}	Logical "0" Strobe Input Current	V_{STROBE} = 0.4V, V_{DIFF} = −3V				−1.0	−1.4	mA
I_{SC}	Output Short Circuit Current	I_{OUT} = 0V, V_{CC} = 5.5V, V_{STROBE} = 0V			−2.8	−4.5	−6.7	mA

Switching Characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay, Differential Input to "0" Output	R_L = 400Ω, C_L = 15 pF, see *Figure 1*		30	45	ns
t_{pd1}	Propagation Delay, Differential Input to "1" Output			27	40	ns
t_{pd0}	Propagation Delay, Strobe Input to "0" Output			16	25	ns
t_{pd1}	Propagation Delay, Strobe Input to "1" Output			18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

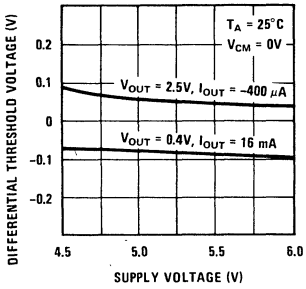
Note 2: These specifications apply for $4.5V \leq V_{CC} \leq 5.5V$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq +125°C$ for the DS7820A or $4.75V \leq V_{CC} \leq 5.25V$, $0°C \leq T_A \leq +70°C$ for the DS8820A unless otherwise specified. Typical values given are for V_{CC} = 5.0V, T_A = 25°C and V_{CM} = 0V unless stated differently.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

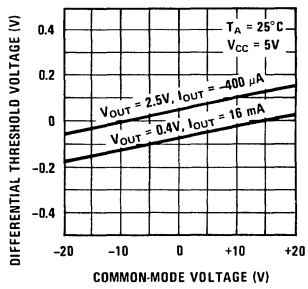
Note 4: Only one output at a time should be shorted.

Typical Performance Characteristics (Note 3)

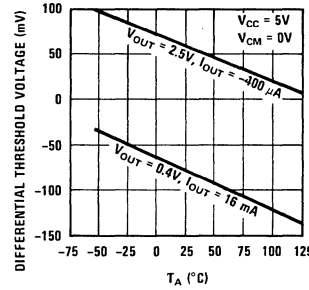
Supply Voltage Sensitivity



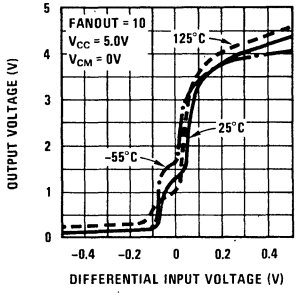
Common-Mode Voltage Sensitivity



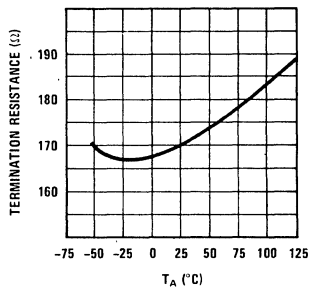
Temperature Sensitivity



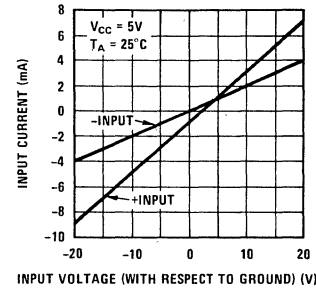
Transfer Function



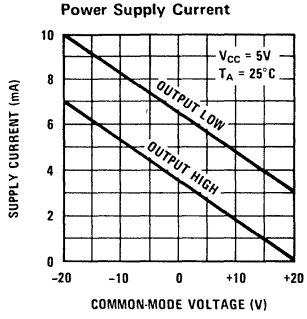
Termination Resistance



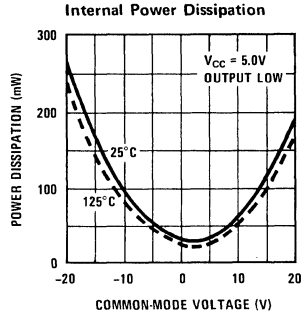
Input Characteristics



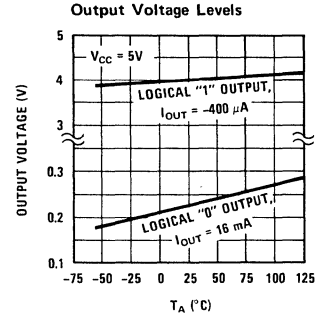
Power Supply Current



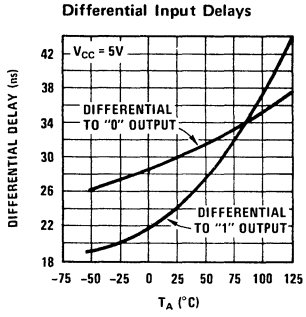
Internal Power Dissipation



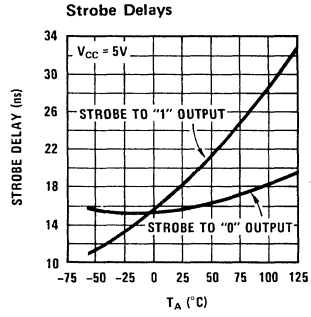
Output Voltage Levels



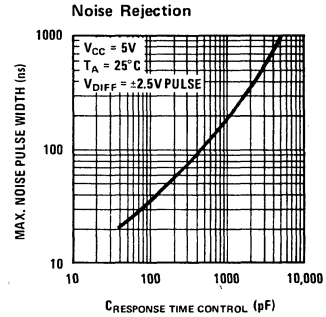
Differential Input Delays



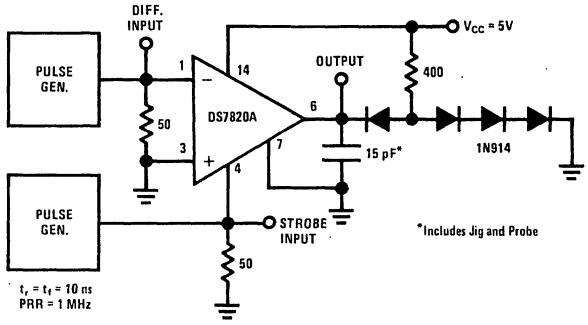
Strobe Delays

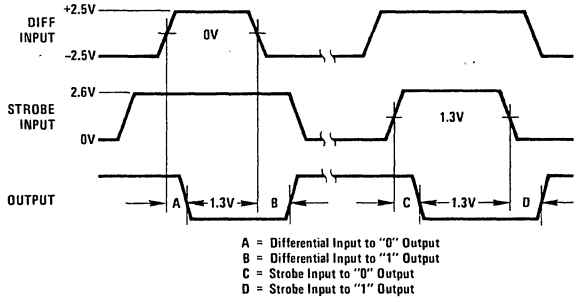


Noise Rejection



AC Test Circuit and Waveforms





A = Differential Input to "0" Output
B = Differential Input to "1" Output
C = Strobe Input to "0" Output
D = Strobe Input to "1" Output

FIGURE 1

National Semiconductor

Transmission Line Drivers/Receivers

DS78C20/DS88C20 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C20 and DS88C20 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA and Federal Standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver, and the pinout is identical.

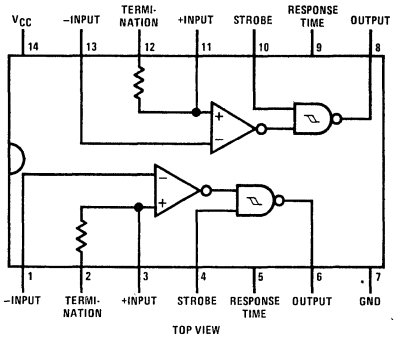
A response pin is provided for controlling sensitivity to input noise spikes with an external capacitor. Each receiver includes a 180Ω terminating resistor, which may be used optionally on twisted pair lines. The DS78C20 is specified over a −55°C to +125°C operating temperature range, and the DS88C20 over a 0°C to +70°C range.

Features

- Meets requirements of EIA Standards RS-232-C RS-422 and RS-423, and Federal Standards 1020 and 1030
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 1/2 V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- DS7830/DS8830 or MM78C30/MM88C30 recommended driver

Connection Diagram

Dual-In-Line Package

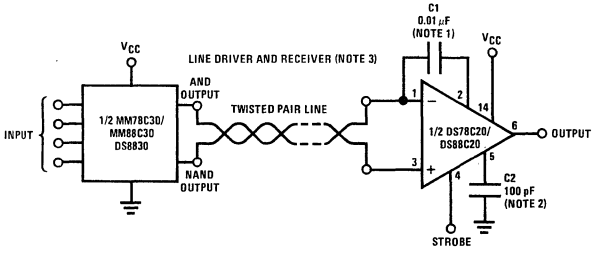


TOP VIEW

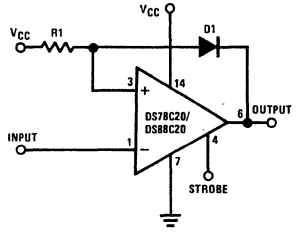
Order Number DS78C20J, DS88C20J or DS88C20N
See NS Package J14A or N14A

Typical Applications

RS-422/RS-423 Application



RS-232-C Application with Hysteresis



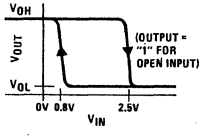
Note 1: (Optional internal termination resistor).
a) Capacitor in series with internal line termination resistor, terminates the line and saves termination power. Exact value depends on line length.
b) Pin 1 connected to pin 2; terminates the line.
c) Pin 2 open; no internal line termination.
d) Transmission line may be terminated elsewhere or not at all.

Note 2: Optional to control response time.

Note 3: V_{CC} 4.5V to 15V for the DS78C20. For further information on line drivers and line receivers, refer to application notes AN-22, AN-83 and AN-108.

For signals which require fail-safe or have slow rise and fall times, use R1 and D1 as shown above. Otherwise, the positive input (pin 3 or 11) may be connected to ground.

V_{CC}	R1 ±5%
5V	4.3 kΩ
10V	15 kΩ
15V	24 kΩ



Absolute Maximum Ratings (Note 1)

Supply Voltage	18V
Common-Mode Voltage	±25V
Differential Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1364 mW
Molded Package	1280 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C20	−55	+125	°C
DS88C20	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$	$-10V \leq V_{CM} \leq 10V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
		$I_{OUT} = 1.6$ mA, $V_{OUT} \leq 0.5V$	$-10V \leq V_{CM} \leq 10V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V$			5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
I_{IND}	Data Input Current (Unterminated)	$V_{CM} = 10V$			2	3.1	mA
		$V_{CM} = 0V$			0	−0.5	mA
		$V_{CM} = -10V$			−2	−3.1	mA
V_{THB}	Input Balance	$I_{OUT} = 200\ \mu A$, $V_{OUT} \geq V_{CC} - 1.2V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		0.1	0.4	V
		$I_{OUT} = 1.6$ mA, $V_{OUT} \leq 0.5V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -200\ \mu A$, $V_{DIFF} = 1V$		$V_{CC}-1.2$	$V_{CC}-0.75$		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 1.6$ mA, $V_{DIFF} = -1V$			0.25	0.5	V
I_{CC}	Power Supply Current	$15V \leq V_{CM} \leq -15V$, $V_{DIFF} = -0.5V$ (Both Receivers)	$V_{CC} = 5.5V$		8	15	mA
			$V_{CC} = 15V$		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 15V$, $V_{DIFF} = 3V$			15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$			−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	$I_{OUT} = 1.6$ mA, $V_{OL} \leq 0.5V$	$V_{CC} = 5V$	3.5	2.5		V
			$V_{CC} = 10V$	8.0	5.0		V
			$V_{CC} = 15V$	12.5	7.5		V
V_{IL}	Logical "0" Strobe Input Voltage	$I_{OUT} = -200\ \mu A$, $V_{OH} = V_{CC} - 1.2V$	$V_{CC} = 5V$		2.5	1.5	V
			$V_{CC} = 10V$		5.0	2.0	V
			$V_{CC} = 15V$		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{CC} = 15V$, $V_{STROBE} = 0V$, (Note 4)		−5	−20	−40	mA

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd0(D)}$	Differential Input to "0" Output	$C_L = 50$ pF		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	$C_L = 50$ pF		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	$C_L = 50$ pF		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	$C_L = 50$ pF		100	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

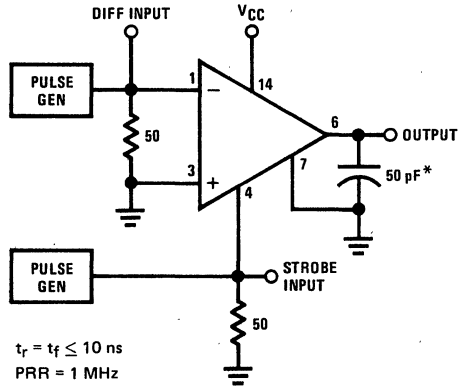
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C20 and across the 0°C to +70°C range for the DS88C20. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

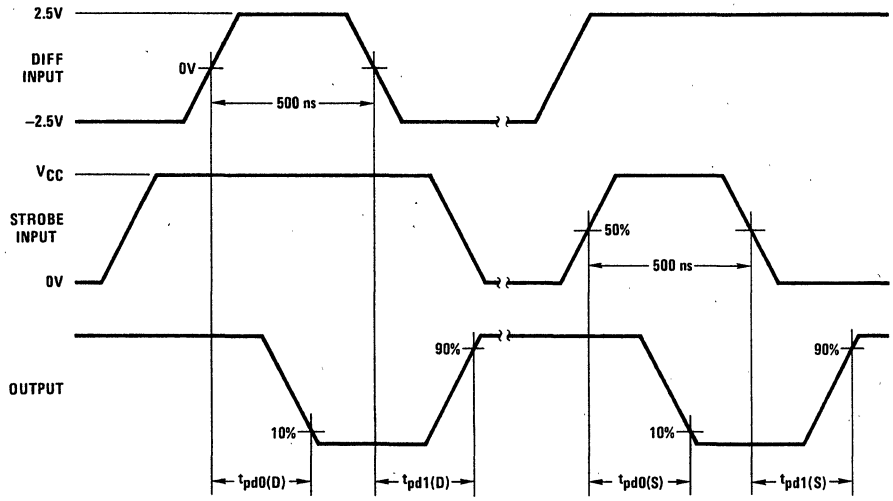
Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA-RS-422 for exact conditions.

AC Test Circuit and Switching Time Waveforms



*Includes probe and jig capacitance



National Semiconductor

Transmission Line Drivers/Receivers

DS7830/DS8830 Dual Differential Line Driver

General Description

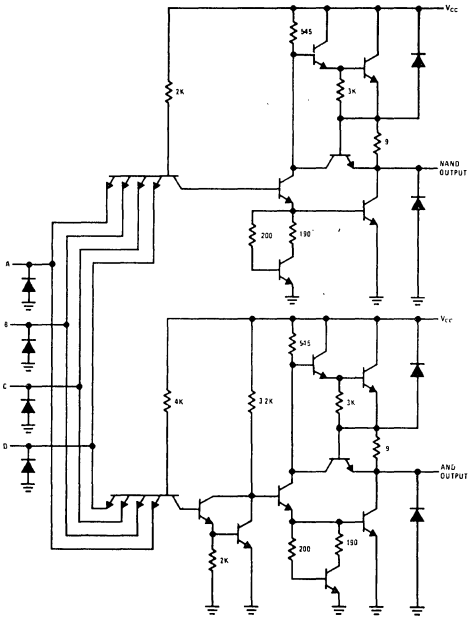
The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

Features

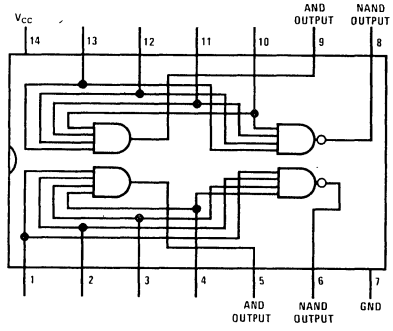
- Single 5 volt power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High speed
- Short circuit protection

Schematic* and Connection Diagrams



*2 PER PACKAGE.

Dual-In-Line and Flat Package

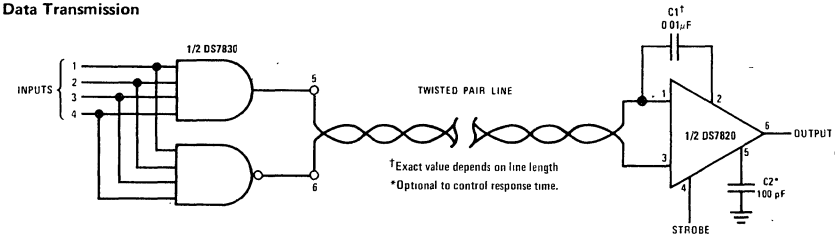


TOP VIEW

Order Number DS7830J, DS8830J or DS8830N
See NS Package J14A or N14A

Typical Application

Digital Data Transmission



Absolute Maximum Ratings (Note 1)

V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Output Short Circuit Duration (125°C)	1 second
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7830	4.5	5.5	V
DS8830	4.75	5.25	V
Temperature (T_A)			
DS7830	−55	+125	°C
DS8830	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V	I_{OUT} = −0.8 mA	2.4			V
			I_{OUT} = 40 mA	1.8	3.3		V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 2.0V	I_{OUT} = 32 mA		0.2	0.4	V
			I_{OUT} = 40 mA		0.22	0.5	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				120	μA
		V_{IN} = 5.5V				2	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−4.8	mA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0V, T_A = 125°C, (Note 4)		−40	−100	−120	mA
I_{CC}	Supply Current	V_{IN} = 5.0V, (Each Driver)			11	18	mA
V_I	Input Clamp	V_{CC} = Min, I_{IN} = −12 mA			−1.0	−1.5	V

Switching Characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay AND Gate	R_L = 400Ω, C_L = 15 pF		8	12	ns
t_{pd0}		*(Figure 1)*		11	18	ns
t_{pd1}	Propagation Delay NAND Gate	R_L = 400Ω, C_L = 15 pF		8	12	ns
t_{pd0}		*(Figure 1)*		5	8	ns
t_1	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns
t_2	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7830 and across the 0°C to +70°C range for the DS8830. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

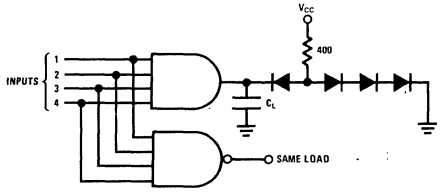


FIGURE 1.

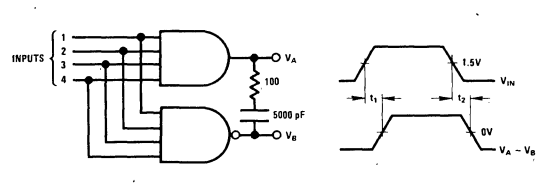
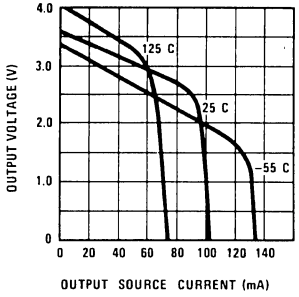


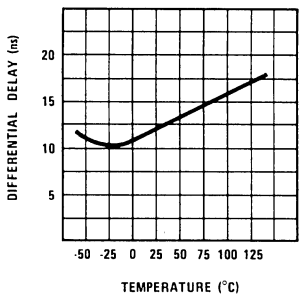
FIGURE 2.

Typical Performance Characteristics

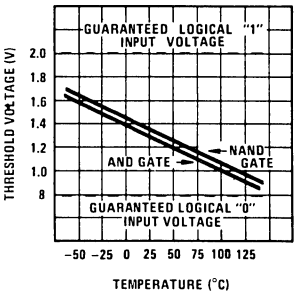
Output High Voltage (Logical "1") Vs Output Current



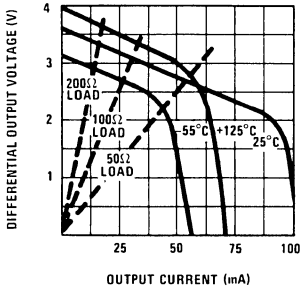
Differential Delay Vs Temperature



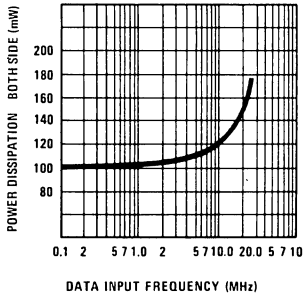
Threshold Voltage Vs Temperature



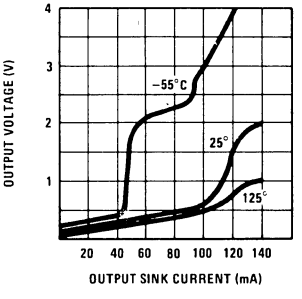
Differential Output Voltage ($|V_{AND} - V_{NAND}|$) Vs Differential Output Current



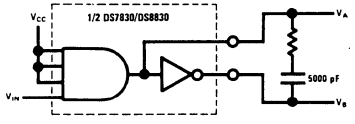
Power Dissipation (No Load) Vs Data Input Frequency



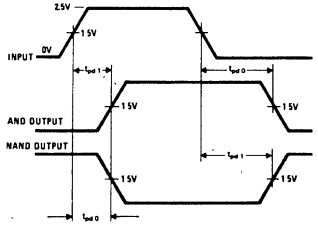
Output Low Voltage (Logical "0") Vs Output Current

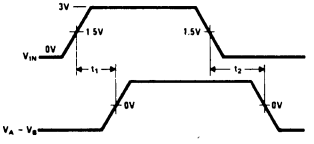


AC Test Circuit



Switching Time Waveforms





f = 1 MHz

$t_r = t_f \leq 10$ ns (10% to 90%)

Duty cycle = 50%

National Semiconductor

Transmission Line Drivers/Receivers

DS7831/DS8831, DS7832/DS8832 Dual TRI-STATE® Line Driver

General Description

Through simple logic control, the DS7831/DS8831, DS7832/DS8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DS7832/DS8832 does not have the V_{CC} clamp diodes found on the DS7831/DS8831.

The DS7831 and DS7832 are specified for operation over the −55°C to +125°C military temperature range. The DS8831 and DS8832 are specified for operation over the 0°C to +70°C temperature range.

Features

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line.

Mode of Operation

To operate as a quad single-ended line driver apply logical "0"s to the Output Disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"'s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs. The inputs to the A channels should be connected together and the inputs to the B channels should be connected together.

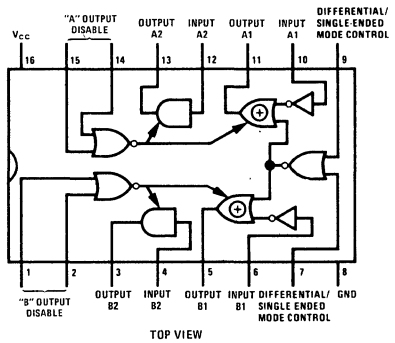
In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

When operating in a bus-organized system with outputs tied directly to outputs of other

(continued)

Connection and Logic Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS7831J, DS8831J, DS7832J, DS8832J, DS8831N or DS8832N
See NS Package J16A or N16A

Truth Table (Shown for A Channels Only)

"A" OUTPUT DISABLE		DIFFERENTIAL/ SINGLE-ENDED MODE CONTROL		INPUT A1	OUTPUT A1	INPUT A2	OUTPUT A2
0	0	0	0	Logical "1" or Logical "0"	Same as Input A1	Logical "1" or Logical "0"	Same as Input A2
0	0	X 1	1 X	Logical "1" or Logical "0"	Opposite of Input A1	Logical "1" or Logical "0"	Same as Input A2
1 X	X 1	X	X	X	High impedance state	X	High impedance state

X = Don't Care

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Time that 2 bus-connected devices may be in opposite low impedance states simultaneously	∞
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 sec.)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7831, DS7832	4.5	5.5	V
DS8831, DS8832	4.75	5.25	V
Temperature (T_A)			
DS7831, DS7832	−55	+125	°C
DS8831, DS8832	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min					0.8	V
V_{OH}	Logical "1" Output Voltage	DS7831, DS7832	V_{CC} = Min	I_O = −40 mA	1.8	2.3		V
				I_O = −2 mA	2.4	2.7		V
		DS8831, DS8832		I_O = −40 mA	1.8	2.5		V
				I_O = −5.2 mA	2.4	2.9		V
V_{OL}	Logical "0" Output Voltage	DS7831, DS7832	V_{CC} = Min	I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
		DS8831, DS8832		I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	DS7831, DS7832, V_{IN} = 5.5V				1	mA
			DS8831, DS8832, V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{OD}	Output Disable Current	V_{CC} = Max, V_O = 2.4V or 0.4V			−40		40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−100	−120	mA
I_{CC}	Supply Current	V_{CC} = Max in TRI-STATE				65	90	mA
V_{CLI}	Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA					−1.5	V
V_{CLO}	Output Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C	I_{OUT} = −12 mA	DS7831/DS8831 DS7832/DS8832			−1.5	V
			I_{OUT} = 12 mA	DS7831/DS8831			V_{CC}+1.5	V

Switching Characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs	R_L = 400Ω, C_L = 15 pF *See Figures 4 and 5*		13	25	ns
t_{pd1}	Propagation Delay to a Logical "1" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs			13	25	ns
t_{1H}	Delay from Disable Inputs to High Impedance State (from Logical "1" Level)			6	12	ns
t_{0H}	Delay from Disable Inputs to High Impedance State (from Logical "0" Level)			14	22	ns
t_{H1}	Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State)			14	22	ns
t_{H0}	Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State)			18	27	ns

Notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7831 and DS7832 and across the 0°C to +70°C range for the DS8831 and DS8832. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies for $T_A = 125°C$ only. Only one output should be shorted at a time.

Mode of Operation (Continued)

DS7831/DS8831's, DS7832/DS8832's *(Figure 1)*, all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DS7831/DS8831's, DS7832/DS8832's *(Figure 2)*.

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 μA), the output is easily able to supply that leakage current for several hundred other DS7831/DS8831's, DS7832/DS8832's and still have available drive for the bus line *(Figure 3)*.

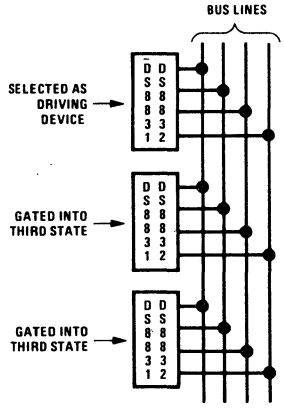


Figure 1

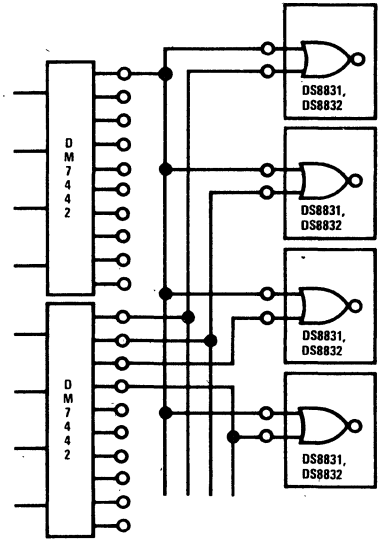


Figure 2

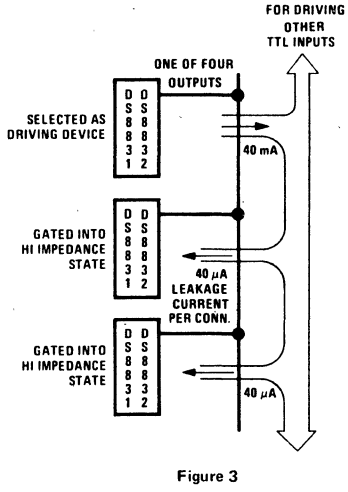
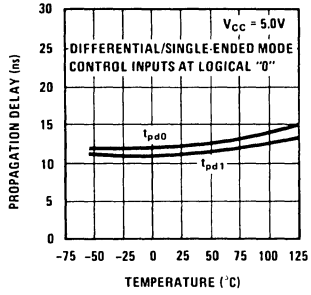


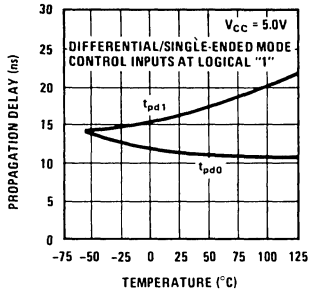
Figure 3

Typical Performance Characteristics

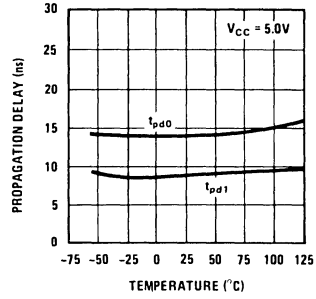
Propagation Delay from Input to Output (Channel 1)



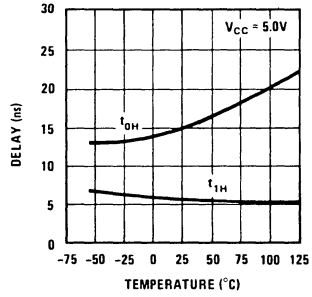
Propagation Delay from Input to Output (Channel 1)



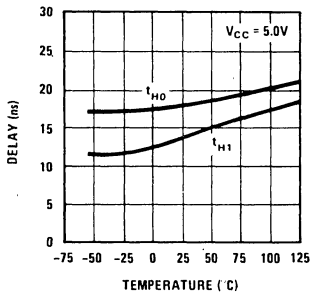
Propagation Delay from Input to Output (Channel 2)



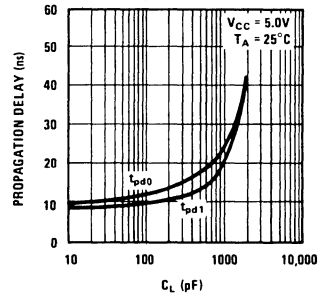
Delay from Disable to High Impedance State



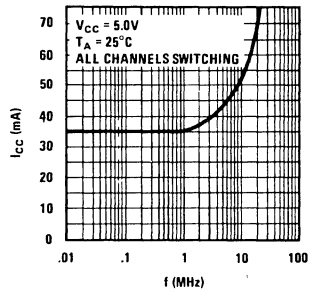
Delay from Disable to Low Impedance State



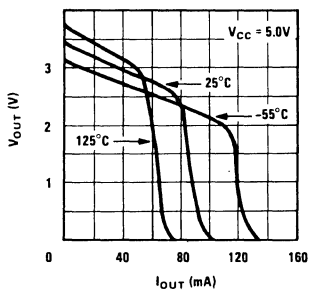
Propagation Delay vs Load Capacitance



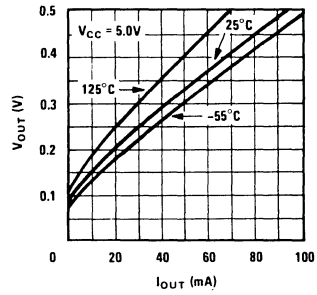
Total Supply Current vs Frequency



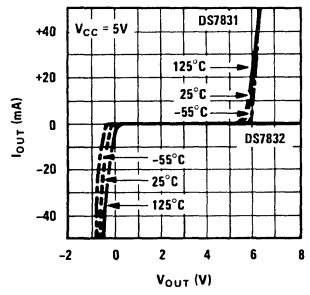
Logical "1" Output Voltage vs Source Current



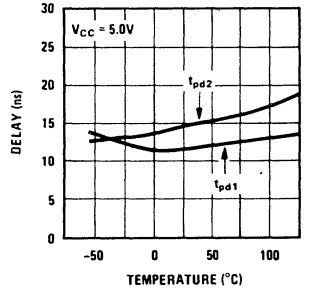
Logical "0" Output Voltage vs Sink Current

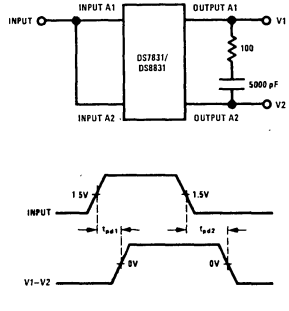


I_{OUT} vs V_{OUT} High Impedance Output State



Propagation Delay in Differential Mode





Switching Time Waveforms

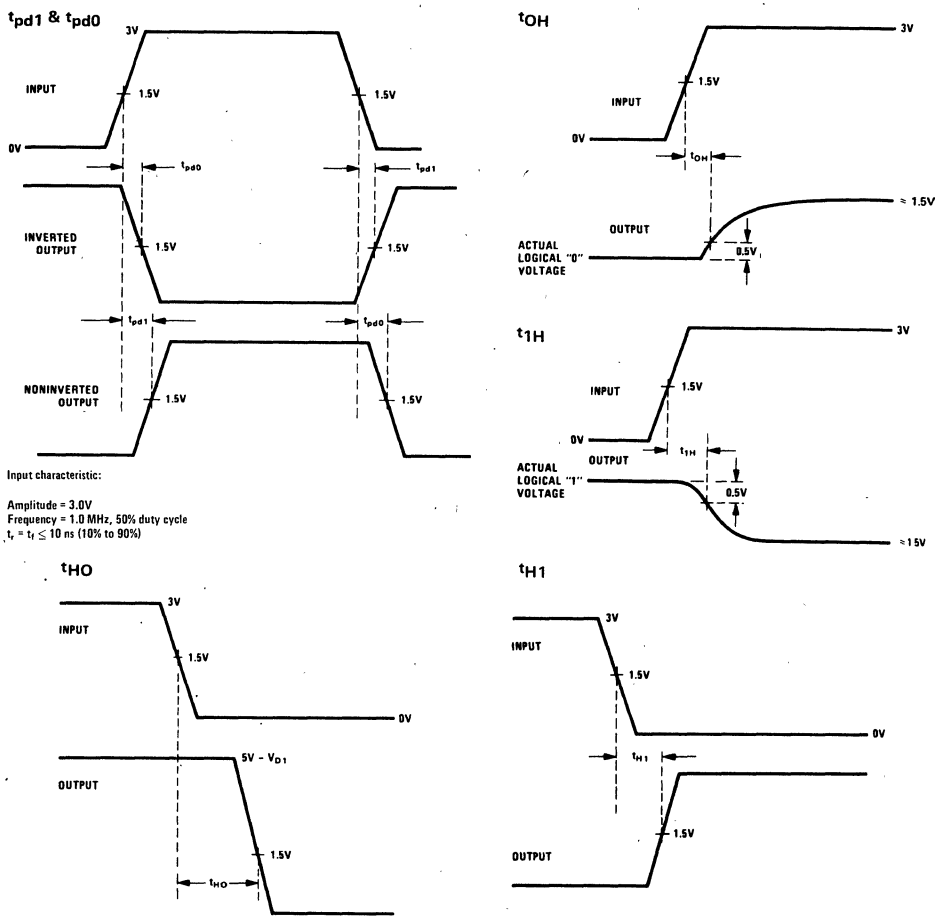
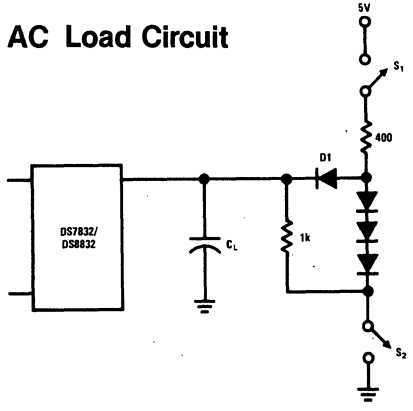


FIGURE 4

AC Load Circuit



	Switch S1	Switch S2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{OH}	closed	closed	* 5 pF
t_{1H}	closed	closed	* 5 pF
t_{HO}	closed	open	50 pF
t_{H1}	open	closed	50 pF

*Jig capacitance.

FIGURE 5

National Semiconductor

Transmission Line Drivers/Receivers

DS78C120/DS88C120 Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C120 and DS88C120 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

Features

- Full compatibility with EIA Standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 1/2 V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- Separate fail-safe mode

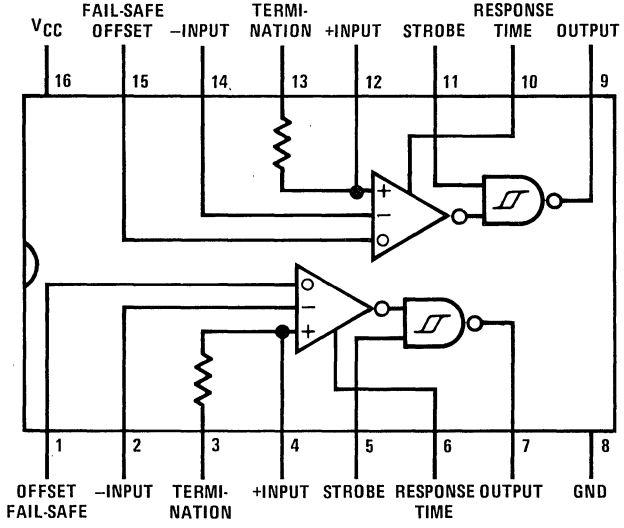
Functional Description

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes a 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78C120 is specified over a −55°C to +125°C temperature range and the DS88C120 from 0°C to +70°C.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS78C120J, DS88C120J or DS88C120N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	18V
Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C120	−55	+125	°C
DS88C120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	I_{OUT} = −200 μA, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
V_{TL}	Differential Threshold Voltage	I_{OUT} = 1.6 mA, $V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
V_{TH}	Differential Threshold Voltage	I_{OUT} = −200 μA, $V_{OUT} \geq V_{CC} - 1.2V$	$-7V \leq V_{CM} \leq 7V$		0.47	0.7	V
V_{TL}	Fail-Safe Offset = 5V	I_{OUT} = 1.6 mA, $V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$	0.2	0.42		V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V$, $0V \leq V_{CC} \leq 15V$		4	5		kΩ
R_T	Line Termination Resistance	T_A = 25°C		100	180	300	Ω
R_O	Offset Control Resistance	T_A = 25°C			56		kΩ
I_{IND}	Data Input Current (Unterminated)	$0V \leq V_{CC} \leq 15V$	V_{CM} = 10V		2	3.1	mA
			V_{CM} = 0V		0	−0.5	mA
			V_{CM} = −10V		−2	−3.1	mA
V_{THB}	Input Balance	I_{OUT} = 200 μA, $V_{OUT} \geq V_{CC} - 1.2V$, R_S = 500Ω, (Note 5)	$-7V \leq V_{CM} \leq 7V$		0.1	0.4	V
		I_{OUT} = 1.6 mA, $V_{OUT} \leq 0.5V$, R_S = 500Ω, (Note 5)	$-7V \leq V_{CM} \leq 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −200 μA, V_{DIFF} = 1V		V_{CC}−1.2	V_{CC}−0.75		V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 1.6 mA, V_{DIFF} = −1V			0.25	0.5	V
I_{CC}	Power Supply Current	$15V \leq V_{CM} \leq -15V$, V_{DIFF} = −0.5V (Both Receivers)	V_{CC} = 5.5V		8	15	mA
			V_{CC} = 15V		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	V_{STROBE} = 15V, V_{DIFF} = 3V			15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	V_{STROBE} = 0V, V_{DIFF} = −3V			−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	$V_{OL} \leq 0.5V$, I_{OUT} = 1.6 mA	V_{CC} = 5V	3.5	2.5		V
			V_{CC} = 10V	8.0	5.0		V
			V_{CC} = 15V	12.5	7.5		V
V_{IL}	Logical "0" Strobe Input Voltage	$V_{OH} = V_{CC} - 1.2V$, I_{OUT} = −200 μA	V_{CC} = 5V		2.5	1.5	V
			V_{CC} = 10V		5.0	2.0	V
			V_{CC} = 15V		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 15V, V_{STROBE} = 0V, (Note 4)		−5	−20	−40	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd0(D)}$	Differential Input to "0" Output	C_L = 50 pF		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	C_L = 50 pF		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	C_L = 50 pF		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	C_L = 50 pF		100	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

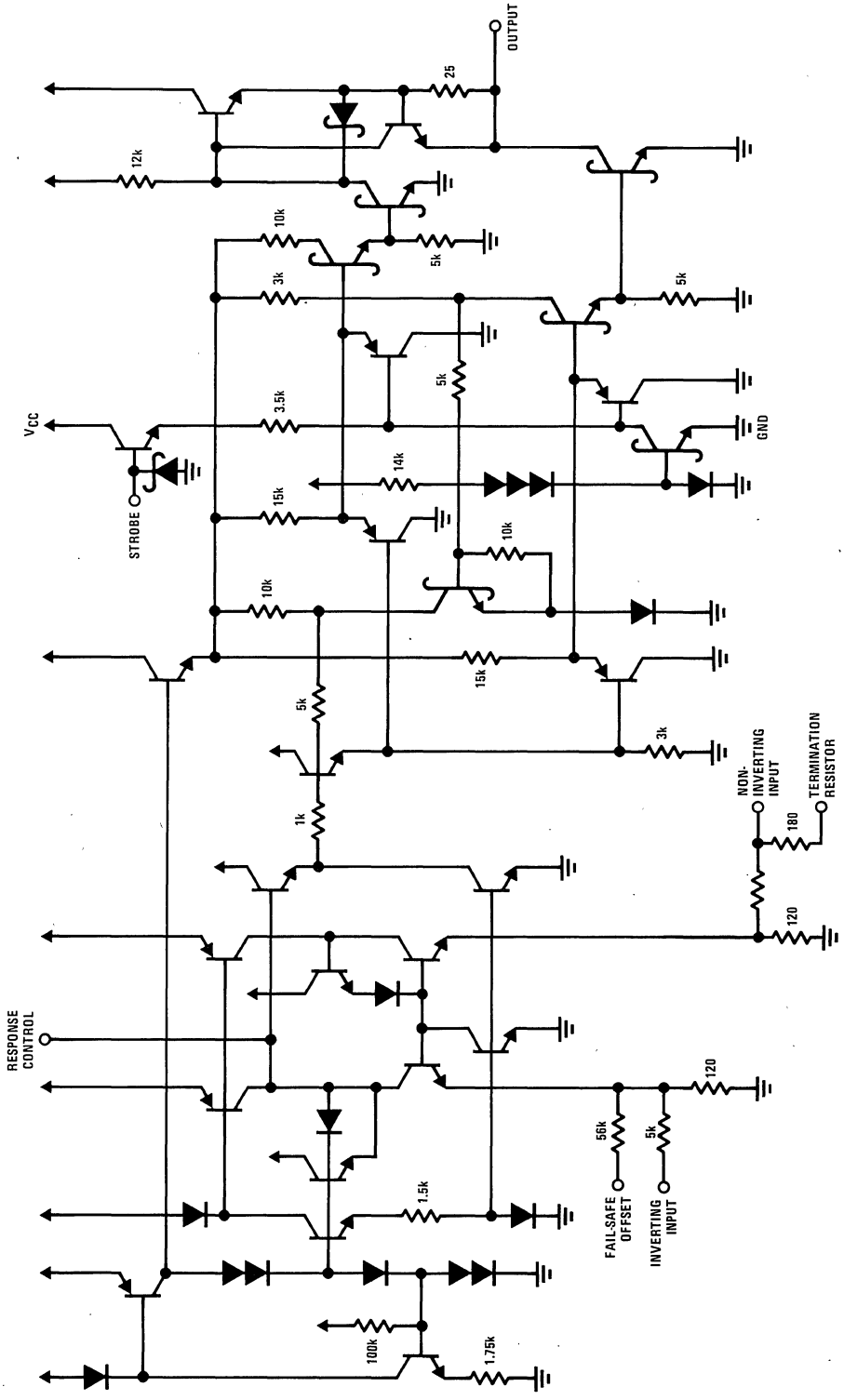
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C120 and across the 0°C to +70°C range for the DS88C120. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

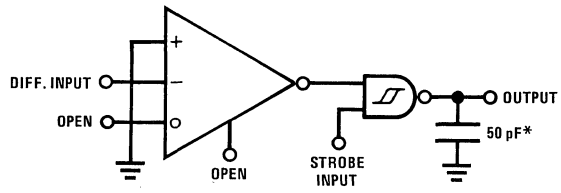
Note 5: Refer to EIA-RS422 for exact conditions.

Schematic Diagram (1/2 Circuit Shown)

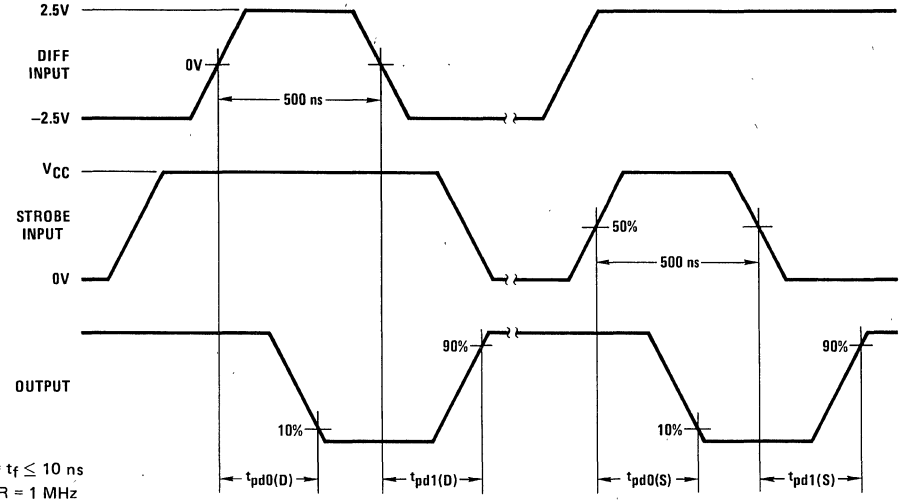


AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal



*Includes probe and test fixture capacitance

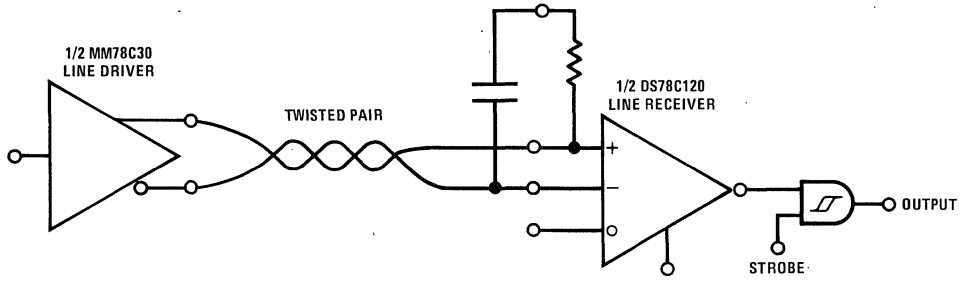


$t_r = t_f \leq 10$ ns
PRR = 1 MHz

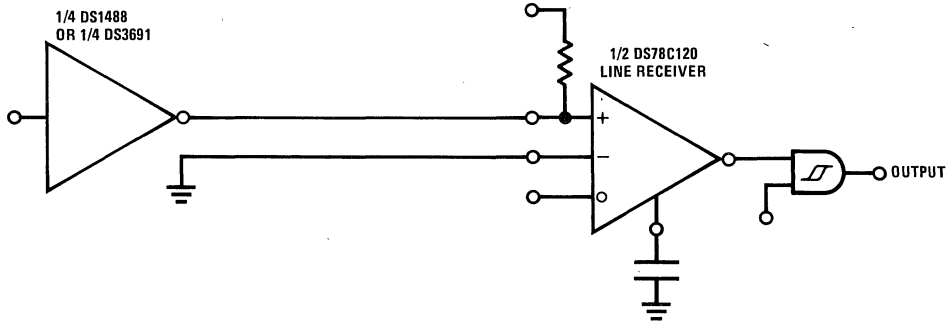
Note. Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection).

Application Hints

Balanced Data Transmission

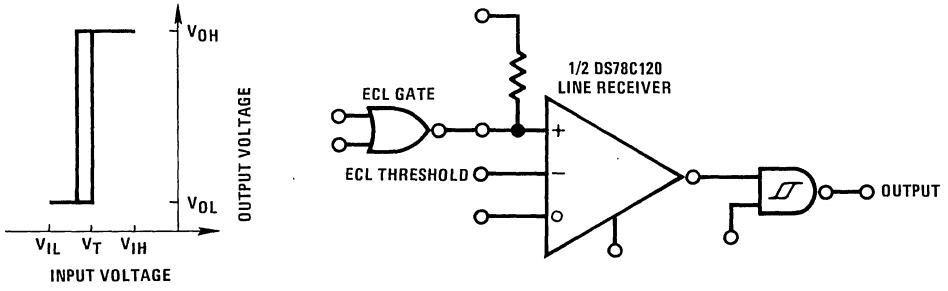


Unbalanced Data Transmission



Application Hints (Continued)

Logic Level Translator



The DS78C120/DS88C120 may be used as a level translator to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to 1/2 the voltage of the input signal, and the other input to the driving gate.

LINE DRIVERS

Line drivers which will interface with the DS78C120/DS88C120 are listed below.

Balanced Drivers

DS26LS31	Quad RS422 Line Driver
MM87C30, MM88C30	Dual CMOS
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE® TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691, DS3691	Quad RS423/Dual RS422 TTL
DS1692, DS3692	Quad RS423/Dual TRI-STATE RS422 TTL
DS3587, DS3487	Quad TRI-STATE RS422

Unbalanced Drivers

DS1488	Quad RS232
DS75150	Dual RS232

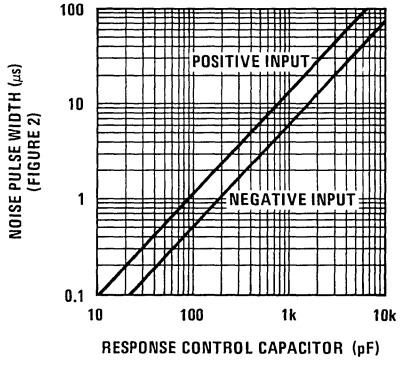


FIGURE 1. Noise Pulse Width vs Response Control Capacitor

RESPONSE CONTROL AND HYSTERESIS

In unbalanced (RS232/RS423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78C120/DS88C120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78C120/DS88C120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1 and 2*. This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.

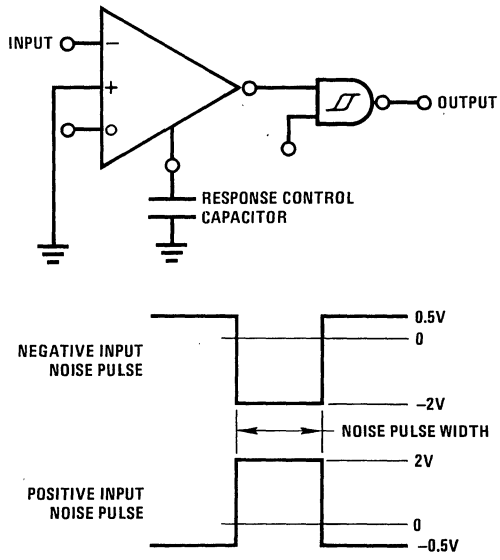


FIGURE 2

Application Hints (Continued)

TRANSMISSION LINE TERMINATION

On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/cross-talk. A 180Ω termination resistor is provided in the DS78C120/DS88C120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns) the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108 in the National Semiconductor Interface Data Book.

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78C120/DS88C120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

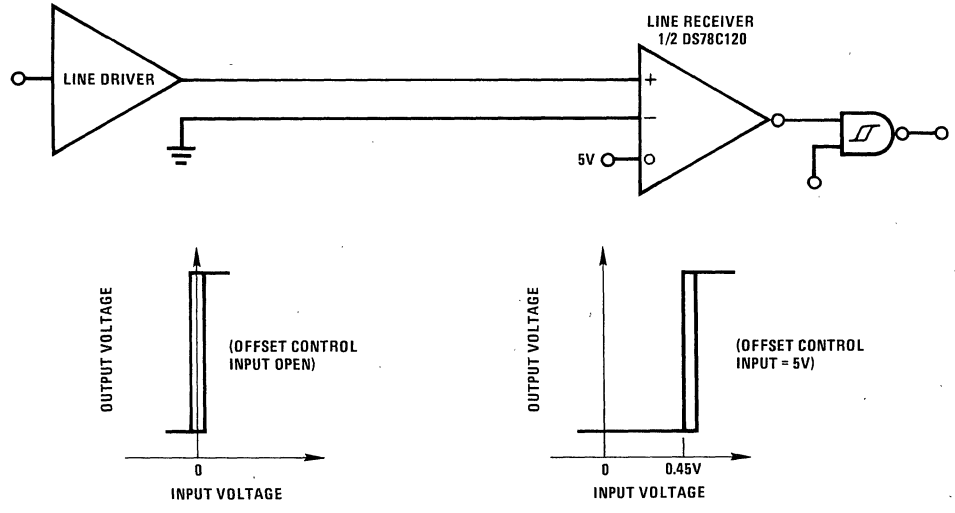
The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ + 0.45V or $V_{IN(INVERTING)}$ + 0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS423) or for balanced interface (RS422) operation.

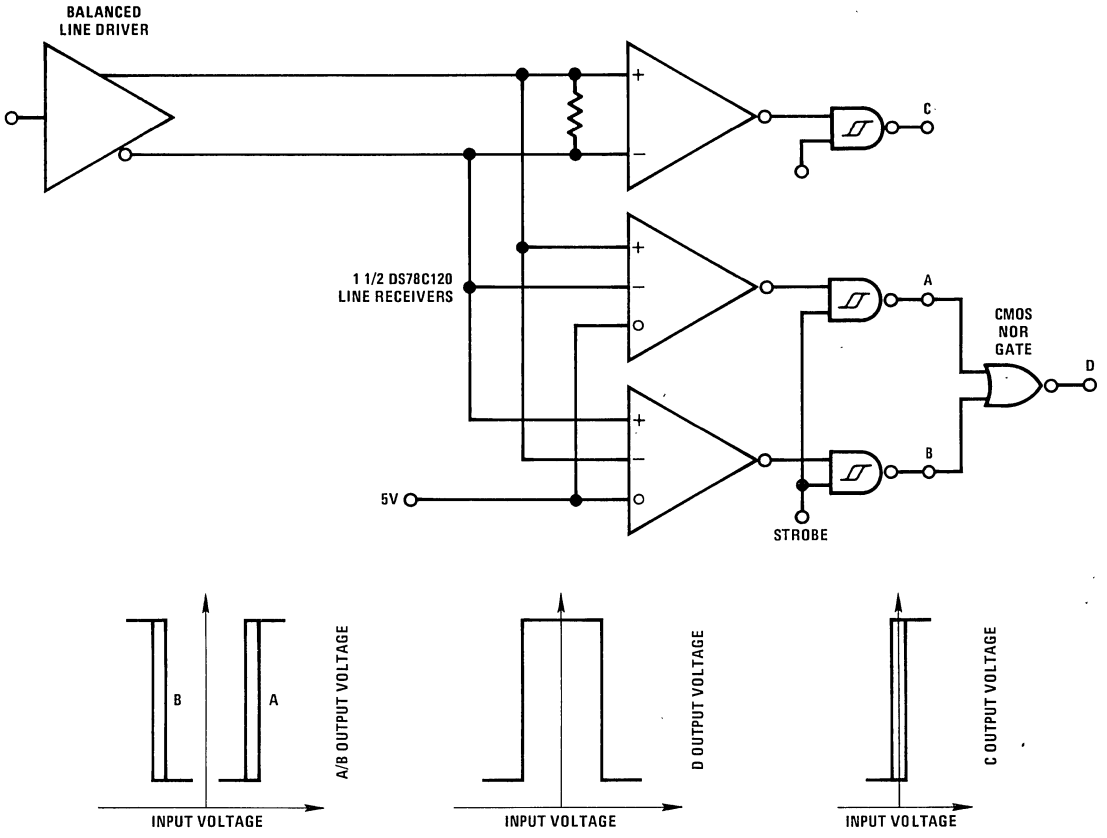
For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to 5V offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

Unbalanced RS423 and RS232 Fail-Safe



Application Hints (Continued)

Balanced RS422 Fail-Safe



For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of the NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

In a communications system, only the control signals are required to detect input fault conditions. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3 Long line lengths

Truth Table (For Balanced Fail-Safe)

INPUT	STROBE	A-OUT	B-OUT	C-OUT	D-OUT
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

National Semiconductor

DS78LS120/DS88LS120 Dual Differential Line Receiver (Noise Filtering and Fail-Safe)

General Description

The DS78LS120 and DS88LS120 are high performance, dual differential, TTL compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes an optional 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78LS120 is specified over a −55°C to +125°C temperature range and the DS88LS120 from 0°C to +70°C.

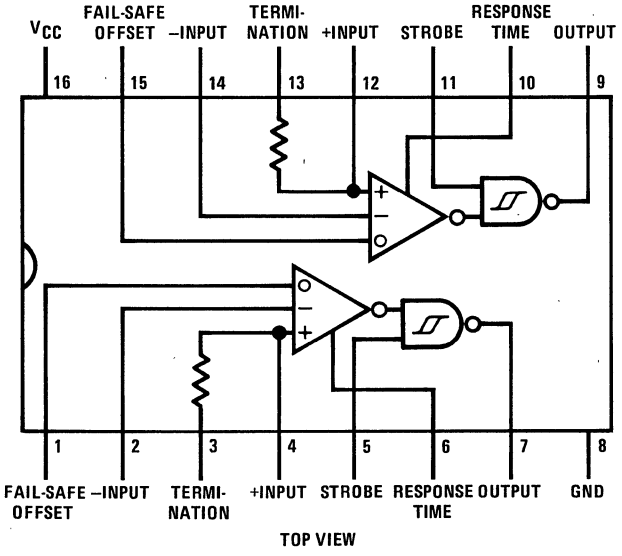
Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

Features

- Meets EIA Standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 5k typical input impedance
- Optional 180Ω termination resistor
- 50 mV input hysteresis
- 200 mV input threshold
- Separate fail-safe mode

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS78LS120J, DS88LS120J or DS88LS120N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	±25V
Strobe Voltage	7V
Output Sink Current	50 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS78LS120	−55	+125	°C
DS88LS120	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -400\,\mu A$, $V_{OUT} \geq 2.5V$	$-7V \leq V_{CM} \leq 7V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
V_{TL}	Differential Threshold Voltage	$I_{OUT} = 4$ mA, $V_{OUT} \leq 0.5V$	$-7V \leq V_{CM} \leq 7V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -400\,\mu A$, $V_{OUT} \geq 2.5V$	$-7V \leq V_{CM} \leq 7V$		0.47	0.7	V
V_{TL}	With Fail Safe Offset = 5V	$I_{OUT} = 4$ mA, $V_{OUT} \leq 0.5$	$-7V \leq V_{CM} \leq 7V$	−0.2	−0.42		V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V$, $0V \leq V_{CC} \leq 7V$		4	5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$		100	180	300	Ω
R_O	Offset Control Resistance	$T_A = 25°C$		42	56	70	kΩ
I_{IND}	Data Input Current (Unterminated)	$V_{CM} = 10V$	$0V \leq V_{CC} \leq 7V$		2	3.1	mA
		$V_{CM} = 0V$			0	−0.5	mA
		$V_{CM} = -10V$			−2	−3.1	mA
V_{THB}	Input Balance	$I_{OUT} = -400\,\mu A$, $V_{OUT} \geq 2.5V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		0.1	0.4	V
		$I_{OUT} = 4$ mA, $V_{OUT} \leq 0.5V$, $R_S = 500\Omega$, (Note 5)	$-7V \leq V_{CM} \leq 7V$		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -400\,\mu A$, $V_{DIFF} = 1V$, $V_{CC} = 4.5V$		2.5	3		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 4$ mA, $V_{DIFF} = -1V$, $V_{CC} = 4.5V$			0.35	0.5	V
I_{CC}	Power Supply Current	$V_{CC} = 5.5V$, $V_{DIFF} = -0.5V$, (Both Receivers)	$V_{CM} = 15V$		9	12	mA
			$V_{CM} = -15V$		10	16	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 5.5V$, $V_{DIFF} = 3V$			1	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$			−290	−400	μA
V_{IH}	Logical "1" Strobe Input Voltage	$V_{OL} \leq 0.5$, $I_{OUT} = 4$ mA		2.0	1.12		V
V_{IL}	Logical "0" Strobe Input Voltage	$V_{OH} \geq 2.5V$, $I_{OUT} = -400\,\mu A$			1.12	0.8	V
I_{OS}	Output Short-Circuit Current	$V_{OUT} = 0V$, $V_{CC} = 5.5V$, $V_{STROBE} = 0V$, (Note 4)		−30	−100	−170	mA

Switching Characteristics $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd0(D)}$	Differential Input to "0" Output	Response Pin Open, $C_L = 15$ pF, $R_L = 2$ kΩ		38	60	ns
$t_{pd1(D)}$	Differential Input to "1" Output			38	60	ns
$t_{pd0(S)}$	Strobe Input to "0" Output			16	25	ns
$t_{pd1(S)}$	Strobe Input to "1" Output			12	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

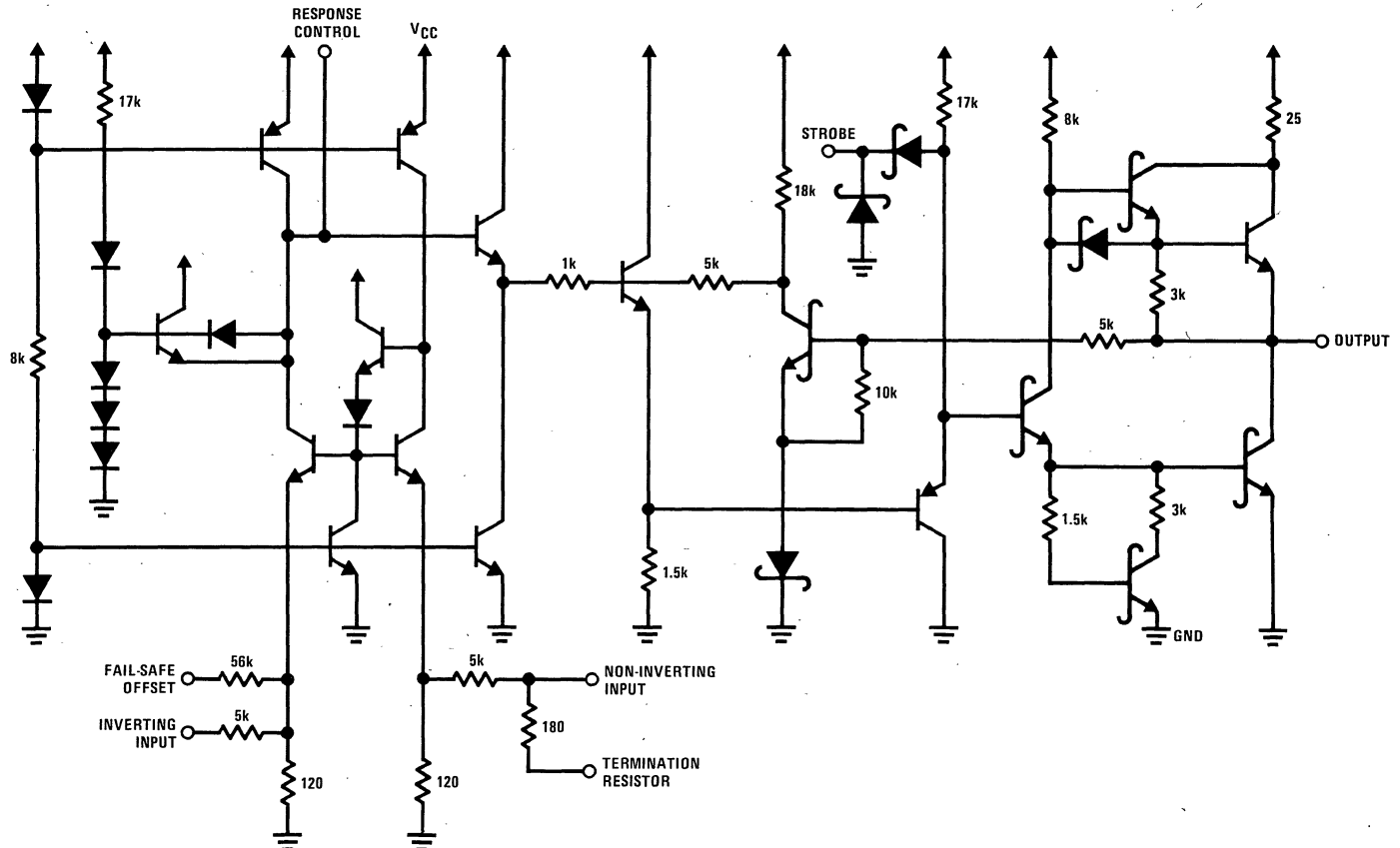
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78LS120 and across the 0°C to +70°C for the DS88LS120. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

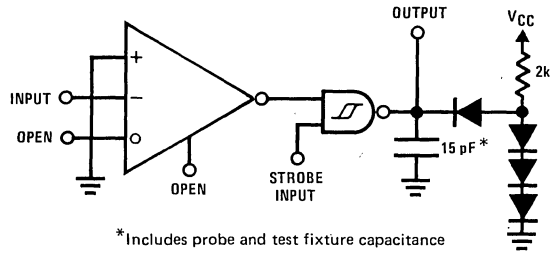
Note 5: Refer to EIA-RS422 for exact conditions.

Schematic Diagram

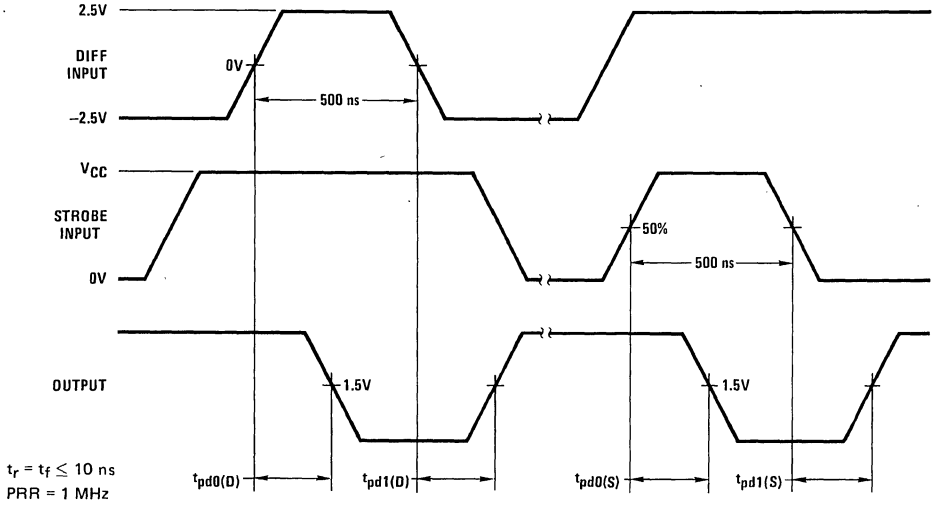


AC Test Circuit and Switching Time Waveforms

Differential and Strobe Input Signal



*Includes probe and test fixture capacitance

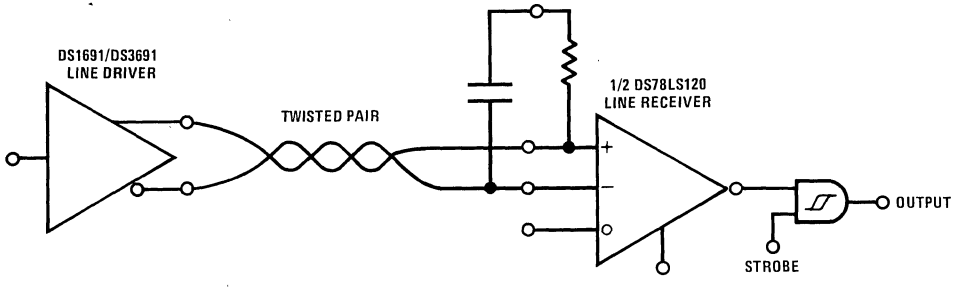


$t_r = t_f \leq 10$ ns
PRR = 1 MHz

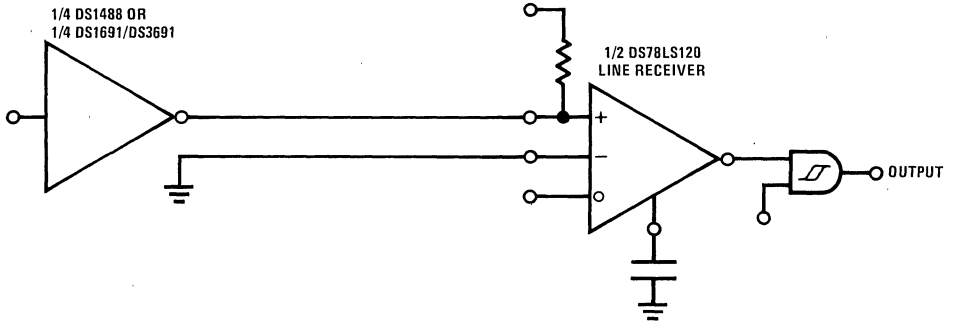
Note. Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection).

Application Hints

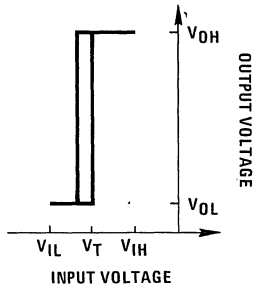
Balanced Data Transmission

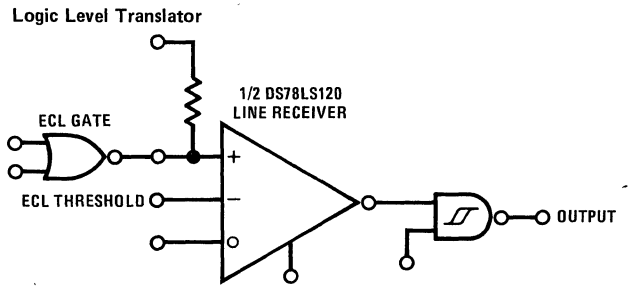


Unbalanced Data Transmission



Application Hints (Continued)





The DS78LS120/DS88LS120 may be used as a level translator to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to 1/2 the voltage of the input signal, and the other input to the driving gate.

LINE DRIVERS

Line drivers which will interface with the DS78LS120/ DS88LS120 are listed below.

Balanced Drivers

DS26LS31	Quad RS422 Line Driver
MM87C30, MM88C30	Dual CMOS
DS7830, DS8830	Dual TTL
DS7831, DS8831	Dual TRI-STATE® TTL
DS7832, DS8832	Dual TRI-STATE TTL
DS1691, DS3691	Quad RS423/Dual RS422 TTL
DS1692, DS3692	Quad RS423/Dual TRI-STATE RS422 TTL
DS3487	Quad TRI-STATE RS422

Unbalanced Drivers

DS1488	Quad RS232
DS75150	Dual RS232

RESPONSE CONTROL AND HYSTERESIS

In unbalanced (RS232/RS423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78LS120/ DS88LS120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78LS120/DS88LS120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmission line. Noise pulse width rejection vs the value of the response control capacitor is shown in *Figures 1 and 2*. This combination of filters followed by hysteresis will optimize performance in a worse case noise environment.

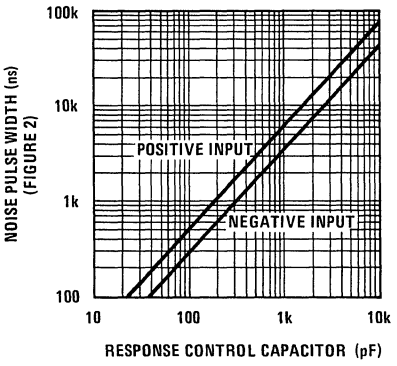


FIGURE 1. Noise Pulse Width vs Response Control Capacitor

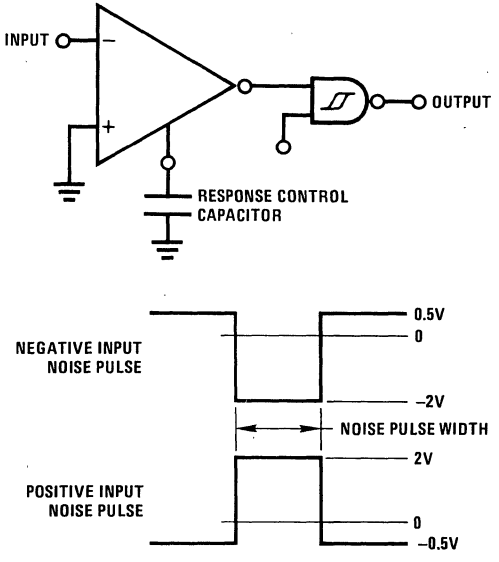


FIGURE 2

Application Hints (Continued)

TRANSMISSION LINE TERMINATION

On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/cross-talk. A 180Ω termination resistor is provided in the DS78LS120/DS88LS120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns), and the termination resistor value is 180Ω, the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108 in the National Semiconductor Interface Data Book.

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to V_{CC} = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or short, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

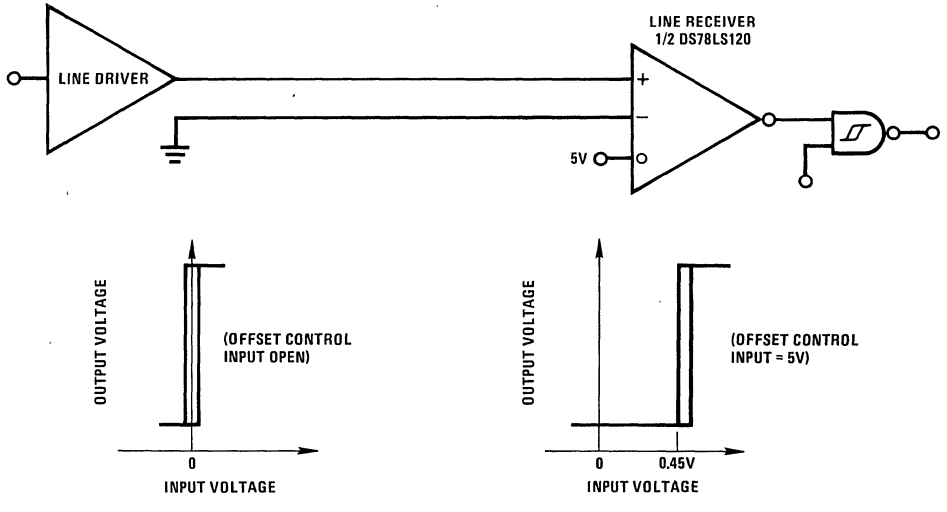
The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ + 0.45V or $V_{IN(INVERTING)}$ + 0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS423) or for balanced interface (RS422) operation.

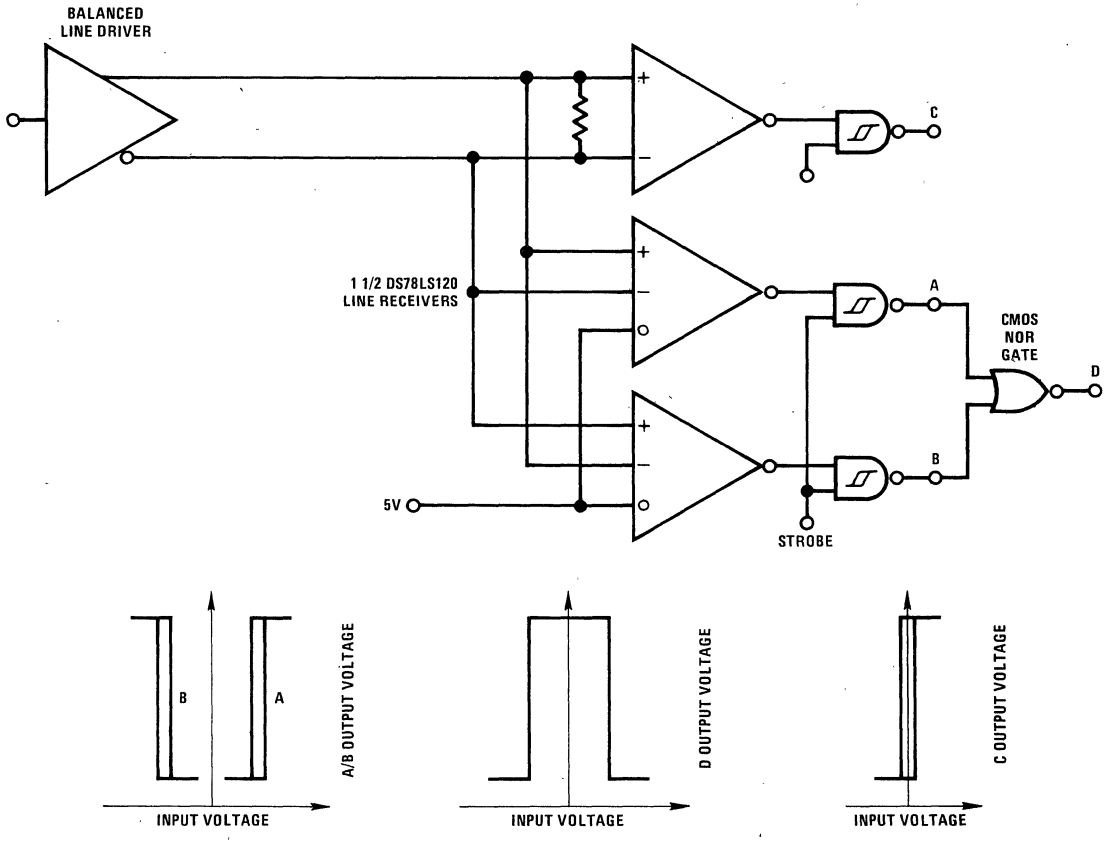
For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to 5V offsets the receiver threshold 0.45V. The output is forced to a logic zero state if the input is open or short.

Unbalanced RS423 and RS232 Fail-Safe



Application Hints (Continued)

Balanced RS422 Fail-Safe



For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of the NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

In a communications system, only the control signals are required to detect input fault conditions. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3 Long line lengths

Truth Table (For Balanced Fail-Safe)

INPUT	STROBE	A-OUT	B-OUT	C-OUT	D-OUT
0	1	0	1	0	0
1	1	1	0	1	0
X	1	0	0	X	1
0	0	1	1	0	0
1	0	1	1	0	0
X	0	1	1	0	0

Integrated Circuits for Digital Data Transmission

INTRODUCTION

It is frequently necessary to transmit digital data in a high-noise environment where ordinary integrated logic circuits cannot be used because they do not have sufficient noise immunity. One solution to this problem, of course, is to use high-noise-immunity logic. In many cases, this approach would require worst case logic swings of 30V, requiring high power-supply voltages. Further, considerable power would be needed to transmit these voltage levels at high speed. This is especially true if the lines must be terminated to eliminate reflections, since practical transmission lines have a low characteristic impedance.

A much better solution is to convert the ground referred digital data at the transmission end into a differential signal and transmit this down a balanced, twisted-pair line. At the receiving end, any induced noise, or voltage due to ground-loop currents, appears equally on both ends of the twisted-pair line. Hence, a receiver which responds only to the differential signal from the line will reject the undesired signals even with moderate voltage swings from the transmitter.

Figure 1 illustrates this situation more clearly. When ground is used as a signal return as in Figure 1a, the voltage seen at the receiving end will be the output voltage of the transmitter plus any noise voltage induced in the signal line. Hence, the noise immunity of the transmitter-receiver combination must be equal to the maximum expected noise from both sources.

The differential transmission scheme diagrammed in Figure 1b solves this problem. Any ground noise or voltage induced on the transmission lines will appear equally on both inputs of the receiver. The receiver responds only to the differential signal coming out of the twisted-pair line and delivers a single-ended output signal referred to the ground

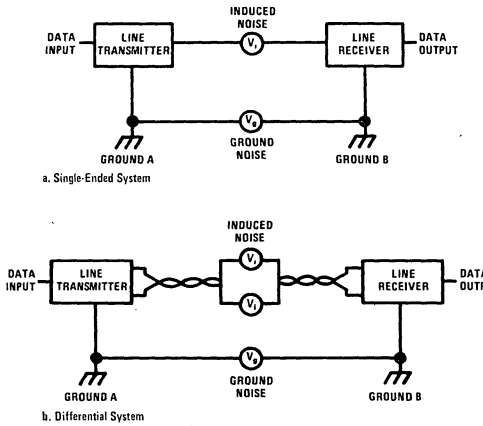


FIGURE 1. Comparing Differential and Single-Ended Data Transmission

at the receiving end. Therefore, extremely high noise immunities are not needed; and the transmitter and receiver can be operated from the same supplies as standard integrated logic circuits.

This article describes the operation and use of a line driver and line receiver for transmission systems using twisted-pair lines. The transmitter provides a buffered differential output from a DTL or TTL input signal. A four-input gate is included on the input so that the circuit can also perform logic. The receiver detects a zero crossing in the differential input voltage and can directly drive DTL or TTL integrated circuits at the receiving end. It also has strobe capability to blank out unwanted input signals. Both the transmitter and the receiver incorporate two independent units on a single silicon chip.

LINE DRIVER

Figure 2 shows a schematic diagram of the line transmitter. The circuit has a marked resemblance to a standard TTL buffer. In fact, it is possible to use a standard dual buffer as a transmitter. However, the DS7830 incorporates additional features. For one, the output is current limited to protect the driver from accidental shorts in the transmission lines. Secondly, diodes on the output clamp severe voltage transients that may be induced into the transmission lines. Finally, the circuit has internal inversion to produce a differential output signal, reducing the skew between the outputs and making the output state independent of loading.

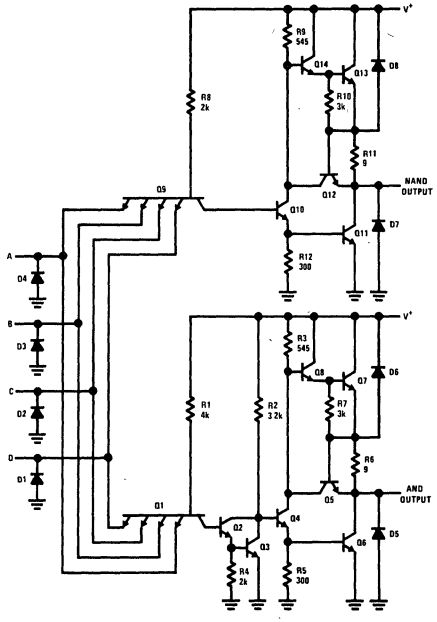


FIGURE 2. Schematic Diagram of the DS7830 Line Driver

As can be seen from the upper half of Figure 2, a quadruple-emitter input transistor, Q9, provides four logic inputs to the transmitter. This transistor drives the inverter stage formed by Q10 and Q11 to give a NAND output. A low state logic input on any of the emitters of Q9 will cause the base drive to be removed from Q10, since Q9 will be saturated by current from R8, holding the base of Q10 near ground. Hence, Q10 and Q11 will be turned off; and the output will be in a high state. When all the emitters of Q9 are at a one logic level, Q10 receives base drive from R8 through the forward biased collector-base junction of Q9. This saturates Q10 and also Q11, giving a low output state. The input voltage at which the transition occurs is equal to the sum of the emitter-base turn on voltages of Q10 and Q11 minus the saturation voltage of Q9. This is about 1.4V at 25°C.

A standard "totem-pole" arrangement is used on the output stage. When the output is switched to the high state, with Q10 and Q11 cut off, current is supplied to the load by Q13 and Q14 which are connected in a modified Darlington configuration. Because of the high compound current gain of these transistors, the output resistance is quite low and a large load current can be supplied. R10 is included across the emitter-base junction of Q13 both to drain off any collector-base leakage current in Q13 and to discharge the collector-base capacitance of Q13 when the output is switched to the low state. In the high state, the output level is approximately two diode drops below the positive supply, or roughly 3.6V at 25°C with a 5.0V supply.

With the output switched into the low state, Q10 saturates, holding the base of Q14 about one diode drop above ground. This cuts off Q13. Further, both the base current and the collector current of Q10 are driven into the base of Q11 saturating it and giving a low-state output of about 0.1V. The circuit is designed so that the base of Q11 is supplied 6 mA, so the collector can drive considerable load current before it is pulled out of saturation.

The primary purpose of R12 is to provide current to remove the stored charge in Q11 and charge its collector-base capacitance when the circuit is switched to the high state. Its value is also made enough less than R9 to prevent supply current transients which might otherwise occur* when the power supply is coming up to voltage.

*J. Kalb, "Design Considerations for a TTL Gate, "*National Semiconductor* TP-6, May, 1968.

The lower half of the transmitter in Figure 2 is identical to the upper, except that an inverter stage has been added. This is needed so that an input signal which drives the output of the upper half positive will drive the lower half negative, and vice versa, producing a differential output signal. Transistors Q2 and Q3 produce the inversion. Even though the current gain is not necessarily needed, the modified Darlington connection is used to produce the proper logic transition voltage on the input of the transmitter. Because of the low load capacitance that the inverter sees when it is completely within the integrated circuit, it is extremely fast, with a typical delay of 3 ns. This minimizes the skew between the outputs.

One of the schemes used when dual buffers are employed as a differential line driver is to obtain the NAND output in the normal fashion and provide the AND output by connecting the input of the second buffer to the NAND output. Using an internal inverter has some distinct advantages over this: for one, capacitive loads which slow down the response of the NAND output will not introduce a time skew between the two outputs; secondly, line transients on the NAND output will not cause an unwanted change of state on the AND output.

Clamp diodes, D1 through D4, are added on all inputs to clamp undershoot. This undershoot and ringing can occur in TTL systems because the rise and fall times are extremely short.

Output-current limiting is provided by adding a resistor and transistor to each of the complementary outputs. Referring again to Figure 2, when the current on the NAND output increases to a value where the voltage drop across R11 is sufficient to turn on Q12, the short circuit protection comes into effect. This happens because further increases in output current flow into the base of Q12 causing it to remove base drive from Q14 and, therefore, Q13. Any substantial increase in output current will then cause the output voltage to collapse to zero. Since the magnitude of the short circuit depends on the emitter base turn-on voltage of Q12, this current has a negative temperature coefficient. As the chip temperature increases from power dissipation, the available short circuit current is reduced. The current limiting also serves to control the current transient that occurs when the output is going through a transition with both Q11 and Q13 turned on.

The AND output is similarly protected by R6 and Q5, which limit the maximum output current to about 100 mA, preventing damage to the circuit from shorts between the outputs and ground.

The current limiting transistors also serve to increase the low state output current capability under severe transient conditions. For example, when the current into the NAND output becomes so high as to pull Q11 out of saturation, the output voltage will rise to two diode drops above ground. At this voltage, the collector-base junction of Q12 becomes forward biased and supplies additional base drive to Q11 through Q10 which is saturated. This minimizes any further increase in output voltage.

When either of the outputs are in the high state, they can drive a large current towards ground without a significant change in output voltage. However, noise induced on the transmission line which tries to drive the output positive will cut it off since it cannot sink current in this state. For this reason, D6 and D8 are included to clamp the output and keep it from being driven much above the supply voltage, as this could damage the circuit.

When the output is in a low state, it can sink a lot of current to clamp positive-going induced voltages on the transmission line. However, it cannot source enough current to eliminate negative-going transients so D5 and D7 are included to clamp those voltages to ground.

It is interesting to note that the voltage swing produced on one of the outputs when the clamp diodes go into conduction actually increases the diffferential noise immunity. For example with no induced common mode current, the low-state output will be a saturation voltage above ground while the high output will be two diode drops below the positive supply voltage. With positive-going common mode noise on the line, the low output remains in saturation; and the high output is clamped at a diode drop above the positive supply. Hence, in this case, the common mode noise increases the differential swing by three diode drops.

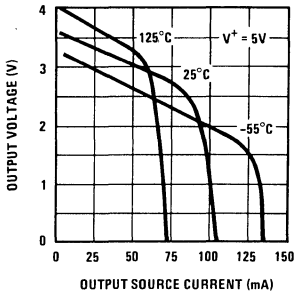


FIGURE 3. High State Output Voltage as a Function of Output Current

Having explained the operation of the line driver, it is appropriate to look at the performance in more detail. Figure 3 shows the high-state output characteristics under load. Over the normal range of output currents, the output resistance is about 10Ω. With higher output currents, the short circuit protection is activated, causing the output voltage to drop to zero. As can be seen from the figure, the short-circuit current decreases at higher temperatures to minimize the possibility of overheating the integrated circuit.

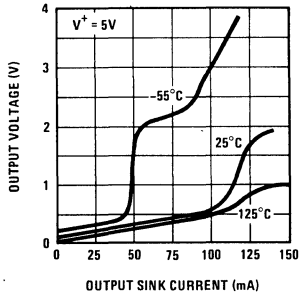


FIGURE 4. Low-State Output Current as a Function of Output Current

Figure 4 is a similar graph of the low-state output characteristics. Here, the output resistance is about 5Ω with normal values of output current. With larger currents, the output transistor is pulled out of saturation; and the output voltage increases. This is most pronounced at −55°C where the transistor current gain is the lowest. However, when the output voltage rises about two diode drops above ground, the collector-base junction of the current-limit transistor becomes forward biased, providing additional base drive for the output transistor. This roughly doubles the current available for clamping positive common-mode transients on the twisted-pair line. It is interesting to note that even though the output level increases to about 2V under this condition, the differential noise immunity does not suffer because the high-state output also increases by about 3V with positive going common-mode transients.

It is clear from the figure that the low state output current is not effectively limited. Therefore, the device can be damaged by shorts between the output and the 5V supply. However, protection against shorts between outputs or from the outputs to ground is provided by limiting the high-state current.

The curves in Figures 3 and 4 demonstrate the performance of the line driver with large, capacitively-coupled common-mode transients, or under

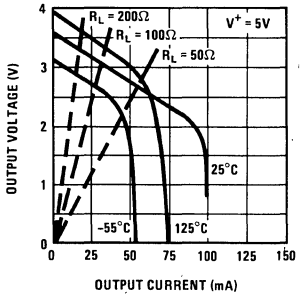


FIGURE 5. Differential Output Voltage as a Function of Differential Output Current

gross overload conditions. Figure 5 shows the ability of the circuit to drive a differential load: that is, the transmission line. It can be seen that for output currents less than 35 mA, the output resistance is approximately 15Ω. At both temperature extremes, the output falls off at high currents. At high temperatures, this is caused by current limiting of the high output state. At low temperatures, the falloff of current gain in the low-state output transistor produces this result.

Load lines have been included on the figure to show the differential output with various load resistances. The output swing can be read off from the intersection of the output characteristic with the load line. The figure shows that the driver can easily handle load resistances greater than 100Ω.

This is more than adequate for practical, twisted-pair lines.

Figure 6 shows the no load power dissipation, for one-half of the dual line driver, as a function of frequency. This information is important for two reasons. First, the increase in power dissipation at high frequencies must be added to the excess power dissipation caused by the load to determine the total package dissipation. Second, and more important, it is a measure of the "glitch" current which flows from the positive supply to ground through the output transistors when the circuit is going through a transition. If the output stage is

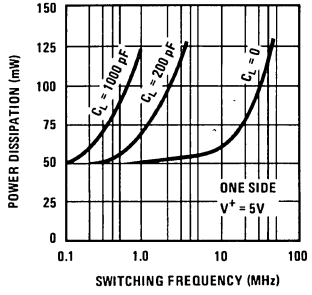


FIGURE 6. Power Dissipation as a Function of Switching Frequency

not properly designed, the current spikes in the power supplies can become quite large; and the power dissipation can increase by as much as a factor of five between 100 KHz and 10 MHz. The figure shows that, with no capacitive loading, the power increase with frequencies as high as 10 MHz is almost negligible. However, with large capacitive loads, more power is required.

The line receiver is designed to detect a zero crossing in the differential output of the line driver. Therefore, the propagation time of the driver is measured as the time difference between the application of a step input and the point where the differential output voltage crosses zero. A plot of the propagation time over temperature is shown in Figure 7. This delay is added directly to the propagation time of the transmission line and the delay of the line receiver to determine the total data-propagation time. However, in most cases, the delay of the driver is small, even by comparison to the uncertainties in the other delays.

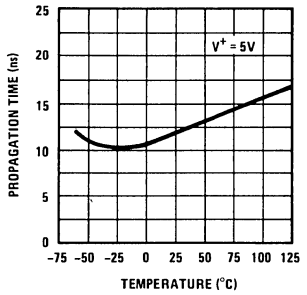


FIGURE 7. Propagation Time as a Function of Temperature

To summarize the characteristics of the DS7830 line driver, the input interfaces directly with standard TTL circuits. It presents a load which is equivalent to a fan out of 3 to the circuit driving it, and it operates from the 5.0V, ±10% logic supplies. The output can drive low impedance lines down to 50Ω and capacitive loads up to 5000 pF. The time skew between the outputs is minimized to reduce radiation from the twisted-pair lines, and the circuit is designed to clamp common mode transients coupled into the line. Short circuit protection is also provided. The integrated circuit consists of two independent drivers fabricated on a 41 x 53 mil-square die using the standard TTL process. A photomicrograph of the chip is shown in Figure 8.

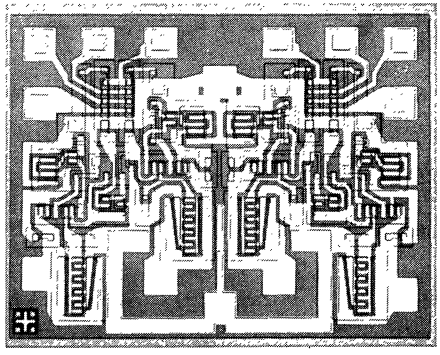


FIGURE 8. Photomicrograph of the DS7830 Dual Line Driver

LINE RECEIVER

As mentioned previously, the function of the line receiver is to convert the differential output signal of the line driver into a single ended, ground-referred signal to drive standard digital circuits on the receiving end. At the same time it must reject the common mode and induced noise on the transmission line.

Normally this would not be too difficult a task because of the large signal swings involved. However, it was considered important that the receiver operate from the +5V logic supply without requiring additional supply voltages, as do most other line receiver designs. This complicates the situation because the receiver must operate with ±15V input signals which are considerably greater than the operating supply voltage.

The large common mode range over which the circuit must work can be reduced with an attenuator on the input of the receiver. In this design, the input signal is attenuated by a factor of 30. Hence, the ±15V common mode voltage is reduced to ±0.5V, which can be handled easily by circuitry operating from a 5V supply. However, the differential input signal, which can go down as low as ±2.4V in the worst case, is also reduced to ±80 mV. Hence, it is necessary to employ a fairly accurate zero crossing detector in the receiver.

System requirements dictated that the threshold inaccuracy introduced by the zero crossing detector be less than 17 mV. In principle, this accuracy requirement should not pose insurmountable problems because it is a simple matter to make well matched parts in an integrated circuit.

Figure 9 shows a simplified schematic diagram of the circuit configuration used for the line receiver. The input signal is attenuated by the resistive dividers R1-R2 and R8-R3. This attenuated signal is fed into a balanced dc amplifier, operating in the common base configuration. This input amplifier, consisting of Q1 and Q2, removes the common mode component of the input signal. Further, it delivers an output signal at the collector of Q2, which is nearly equal in amplitude to the original differential input signal. This output signal is buffered by Q6 and drives an output amplifier, Q8. The output stage drives the logic load directly.

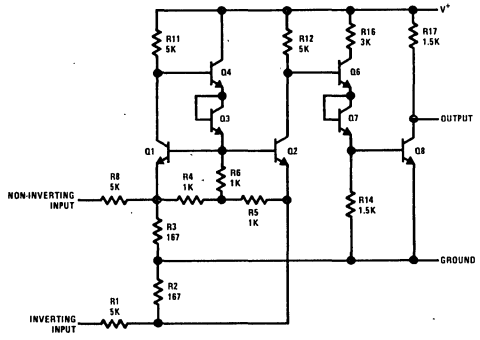


FIGURE 9. Simplified Schematic of the Line Receiver

An understanding of the circuit can be obtained by first considering the input stage. Assuming high current gains and neglecting the voltage drop across R3, the collector current of Q1 will be:

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R11}. \qquad (1)$$

With equal emitter-base voltages for all transistors, this becomes:

$$I_{C1} = \frac{V^+ - 3V_{BE}}{R11} \qquad (2)$$

The output voltage at the collector of Q2 will be:

$$V_{C2} = V^+ - I_{C2}R12. \qquad (3)$$

When the differential input voltage to the receiver is zero, the voltages presented to the emitters of Q1 and Q2 will be equal. If Q1 and Q2 are matched devices, which is easy to arrange when they are fabricated close together on a single silicon chip, their collector currents will be equal with zero input voltage. Hence, the output voltage from Q2 can be determined by substituting (2) into (3):

$$V_{C2} = V^+ - \frac{R12}{R11}(V^+ - 3V_{BE}). \qquad (4)$$

For R11 = R12, this becomes:

$$V_{C2} = 3V_{BE}.$$

The voltage on the base of Q6 will likewise be $3V_{BE}$ when the output is on the verge of switching from a zero to a one state. A differential input signal which causes Q2 to conduct more heavily will then make the output go high, while an input signal in the opposite direction will cause the output to saturate.

It should be noted that the balance of the circuit is not affected by absolute values of components—only by how well they match. Nor is it affected by variations in the positive supply voltage, so it will perform well with standard logic supply voltages between 4.5V and 5.5V. In addition, component values are chosen so that the collector currents of Q4 and Q6 are equal. As a result, the base currents of Q4 and Q6 do not upset the balance of the input stage. This means that circuit performance is not greatly affected by production or temperature variations in transistor current gain.

A complete schematic of the line receiver, shown in Figure 10, shows several refinements of the basic circuit which are needed to secure proper operation under all conditions. For one, the explanation of the simplified circuit ignores the fact that the collector current of Q1 will be affected by common mode voltage developed across R3. This can give a 0.5V threshold error at the extremes of the ±15V common mode range. To compensate for this, a separate divider, R9 and R10, is used to maintain a constant collector current in Q1 with varying common mode signals. With an increasing common mode voltage on the non-inverting input, the voltage on the emitter of Q1 will increase. Normally, this would cause the voltage across R11 to decrease, reducing the collector current of Q1. However, the increasing common mode signal also drives the top end of R11 through R9 and R10 so as to hold the voltage drop across R11 constant.

In addition to improving the common mode rejection, R9 also forces the output of the receiver into the high state when nothing is connected to the input lines. This means that the output will be in a pre-determined state when the transmission cables are disconnected.

A diode connected transistor, Q5, is also added in the complete circuit to provide strobe capability. With a logic zero on the strobe terminal, the out-

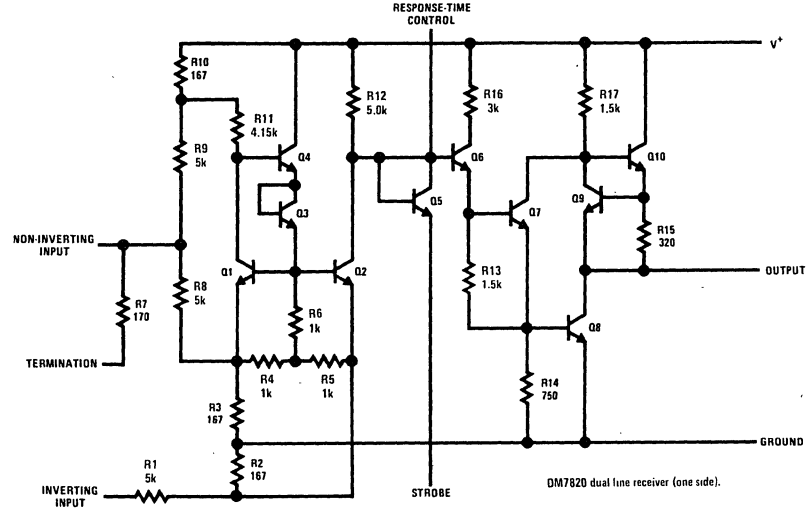


FIGURE 10. Complete Schematic of One Half of the DS7820 Line Receiver

put will be high no matter what the input signal is. With the strobe, the receiver can be made immune to any noise signals during intervals where no digital information is expected. The output state with the strobe on is also the same as the output state with the input terminals open.

The collector of Q2 is brought out so that an external capacitor can be used to slow down the receiver to where it will not respond to fast noise spikes. This capacitor, which is connected between the response-time-control terminal and ground, does not give exactly-symmetrical delays. The delay for input signals which produce a positive-going output will be less than for input signals of opposite polarity. This happens because the impedance on the collector of Q2 drops as Q6 goes into saturation, reducing the effectiveness of the capacitor.

Another difference in the complete circuit is that the output stage is improved both to provide more gain and to reduce the output resistance in the high output state. This was accomplished by adding Q9 and Q10. When the output stage is operating in the linear region, that is, on the verge of switching to either the high or the low state, Q9 and Q10 form sort of an active collector load for Q8. The current through R15 is constant at approximately 2 mA as the output voltage changes through the active region. Hence, the percentage change in the collector current of Q8 due to the voltage change across R17 is made smaller by this pre-bias current; and the effective stage gain is increased.

With the output in the high state (Q8 cut off), the output resistance is equal to R15, as long as the load current is less than 2 mA. When the load current goes above this value, Q9 turns on; and the output resistance increases to 1.5K, the value of R17.

This particular output configuration gives a higher gain than either a standard DTL or TTL output stage. It can also drive enough current in the high state to make it compatible with TTL, yet outputs can be wire OR'ed as with DTL.

Remaining details of the circuit are that Q7 is connected as an emitter follower to make the circuit even less sensitive to transistor current gains. R16 limits the base drive to Q7 with the output saturated, while R17 limits the base drive to the output transistor, Q8. A resistor, R7, which can be used to terminate the twisted-pair line is also included on the chip. It is not connected directly across the inputs. Instead, one end is left open so that a capacitor can be inserted in series with the resistor. The capacitor significantly reduces the power dissipation in both the line transmitter and receiver, especially in low-duty-cycle applications, by terminating the line at high frequencies but blocking steady-state current flow in the terminating resistor.

Since line receivers are generally used repetitively in a system, the DS7820 has been designed with two independent receivers on a single silicon chip. The device is fabricated on a 41 x 49 mil-square die using the standard six mask planar-epitaxial process. The processing employed is identical to that used on TTL circuits, and the design does not impose any unusual demands on the processing. It is only required that various parts within the circuit match well, but this is easily accomplished in a monolithic integrated circuit without any special effort in manufacturing. A photomicrograph of the integrated circuit chip is shown in Figure 11.

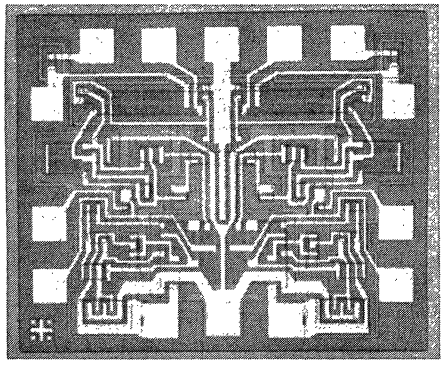


FIGURE 11. Photomicrograph of the DS7820 Dual Line Receiver

The only components in the circuit which see voltages higher than standard logic circuits are the resistors used to attenuate the input signal. These resistors, R1, R7, R8 and R9, are diffused into a separate, floating, N-type isolation tub, so that the higher voltage is not seen by any of the transistors. For a ±15V input voltage range, the breakdown voltages required for the collector-isolation and collector-base diodes are only 15V and 19V, respectively. These breakdown voltages can be achieved readily with standard digital processing.

The purpose of the foregoing was to provide some insight into circuit operation. A more exact mathematical analysis of the device is developed in Appendix A.

RECEIVER PERFORMANCE

The characteristics of the line receiver are described graphically in Figures 12 through 18. Figure 12 illustrates the effect of supply voltage variations on the threshold accuracy. The upper curve gives the differential input voltage required to hold the output at 2.5V while it is supplying 200 μA to the digital load. The lower curve shows the differential input needed to hold the output at 0.4V while it sinks 3.5 mA from the digital load. This load corresponds to a worst case fanout of 2 with either DTL or TTL integrated circuits. The data shows that the threshold accuracy is only affected by ±60 mV for a ±10% change in supply voltage. Proper operation can be secured over a wider range of supply voltages, although the error becomes excessive at voltages below 4V.

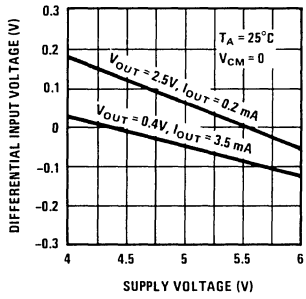


FIGURE 12. Differential Input Voltage Required for High or Low Output as a Function of Supply Voltage

Figure 13 is a similar plot for varying common mode input voltage. Again the differential input voltages are given for high and low states on the output with a worst case fanout of 2. With precisely matched components within the integrated circuit, the threshold voltage will not change with common mode voltage. The mismatches typically encountered give a threshold voltage change of ±100 mV over a ±20V common mode range. This change can have either a positive slope or a negative slope.

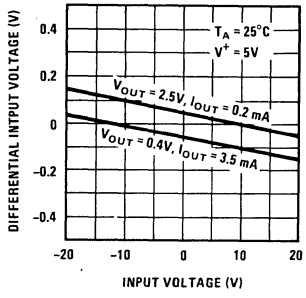


FIGURE 13. Differential Input Voltage Required for High or Low Output as a Function of Common Mode Voltage

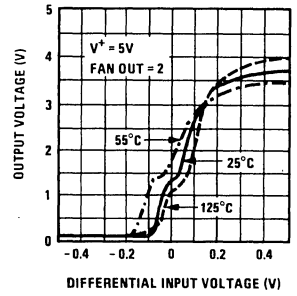


FIGURE 14. Voltage Transfer Function

The transfer function of the circuit is given in Figure 14. The loading is for a worst case fanout of 2. The digital load is not linear, and this is reflected as a non-linearity in the transfer function which occurs with the output around 1.5V. These transfer characteristics show that the only significant effect of temperature is a reduction in the positive swing at –55°C. However, the voltage available remains well above the 2.5V required by digital logic.

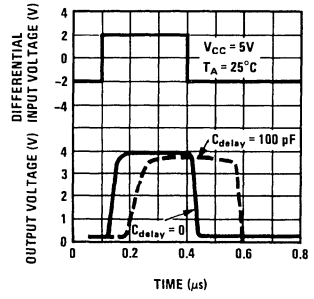


FIGURE 15. Response Time With and Without an External Delay Capacitor

Figure 15 gives the response time, or propagation delay, of the receiver. Normally, the delay through the circuit is about 40 ns. As shown, the delay can be increased, by the addition of a capacitor between the response-time terminal and ground, to make the device immune to fast noise spikes on the input. The delay will generally be longer for negative going outputs than for positive going outputs.

Under normal conditions, the power dissipated in the receiver is relatively low. However, with large common mode input voltages, dissipation increases markedly, as shown in Figure 16. This is of little consequence with common mode transients, but the increased dissipation must be taken into account when there is a dc difference between the grounds of the transmitter and the receiver. It is important to note that Figure 16 gives the dissipation for one half the dual receiver. The total package dissipation will be twice the values given when both sides are operated under identical conditions.

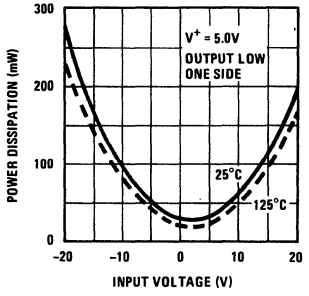


FIGURE 16. Internal Power Dissipation as a Function of Common Mode Input Voltage

Figure 17 shows that the power supply current also changes with common mode input voltage due to the current drawn out of or fed into the supply through R9. The supply current reaches a maximum with negative input voltages and can actually reverse with large positive input voltages. The figure also shows that the supply current with the output switched into the low state is about 3 mA higher than with a high output.

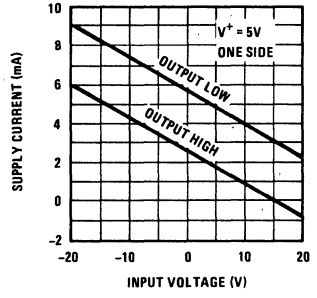


FIGURE 17. Power Supply Current as a Function of Common Mode Input Voltage

The variation of the internal termination resistance with temperature is illustrated in Figure 18.Taking into account the initial tolerance as well as the change with temperature, the termination resistance is by no means precise. Fortunately, in most cases, the termination resistance can vary appreciably without greatly affecting the characteristics of the transmission line. If the resistor tolerance is a problem, however, an external resistor can be used in place of the one provided within the integrated circuit.

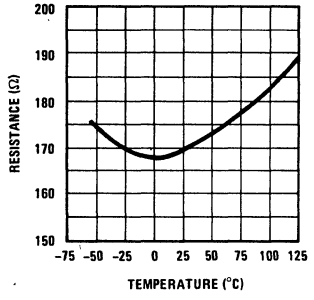


FIGURE 18. Variation of Termination Resistance With Temperature

DATA TRANSMISSION

The interconnection of the DS7830 line driver with the DS7820 line receiver is shown in Figure 19. With the exception of the transmission line, the design is rather straightforward. Connections on the input of the driver and the output or strobe of the receiver follow standard design rules for DTL or TTL integrated logic circuits. The load presented by the driver inputs is equal to 3 standard digital loads, while the receiver can drive a worst-case fanout of 2. The load presented by the receiver strobe is equal to one standard load.

The purpose of C1 on the receiver is to provide dc isolation of the termination resistor for the transmission line. This capacitor can both increase the differential noise immunity, by reducing attenuation on the line, and reduce power dissipation in both the transmitter and receiver. In some applications, C1 can be replaced with a short between Pins 1 and 2, which connects the internal termination resistor of the DS7820 directly across the line. C2 may be included, if necessary, to control the response time of the receiver, making it immune to noise spikes that may be coupled differentially into the transmission lines.

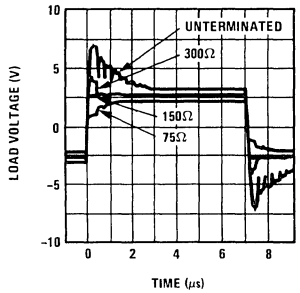


FIGURE 20. Transmission Line Response With Various Termination Resistances

The effect of termination mismatches on the transmission line is shown in Figure 20. The line was constructed of a twisted pair of No. 22 copper conductors with a characteristic impedance of approximately 170Ω. The line length was about 150 ns and it was driven directly from a DS7830 line driver. The data shows that termination resistances which are a factor of two off the nominal value do not cause significant reflections on the line. The lower termination resistors do, however, increase the attenuation.

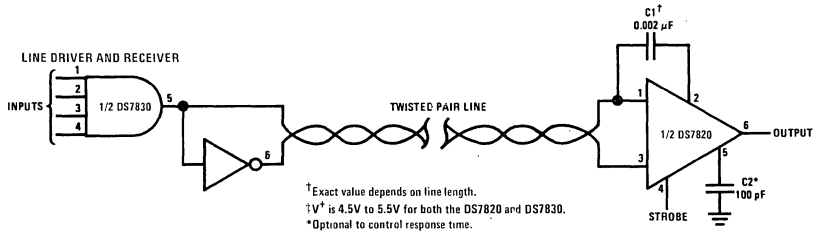


FIGURE 19. Interconnection of the Line Driver and Line Receiver

Figure 21 gives the line-transmission characteristics with various termination resistances when a dc isolation capacitor is used. The line is identical to that used in the previous example. It can be seen that the transient response is nearly the same as a dc terminated line. The attenuation, on the other hand, is considerably lower, being the same as an unterminated line. An added advantage of using the isolation capacitor is that the dc signal current is blocked from the termination resistor which reduces the average power drain of the driver and the power dissipation in both the driver and receiver.

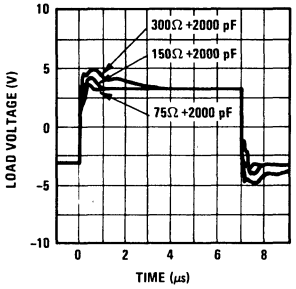


FIGURE 21. Line Response for Various Termination Resistances With a DC Isolation Capacitor

The effect of different values of dc isolation capacitors is illustrated in Figure 22. This shows that the RC time constant of the termination resistor/isolation capacitor combination should be 2 to 3 times the line delay. As before, this data was taken for a 150 ns long line.

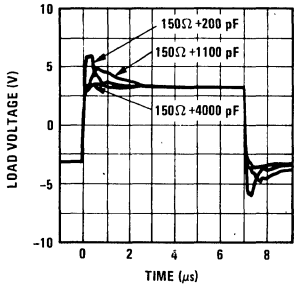
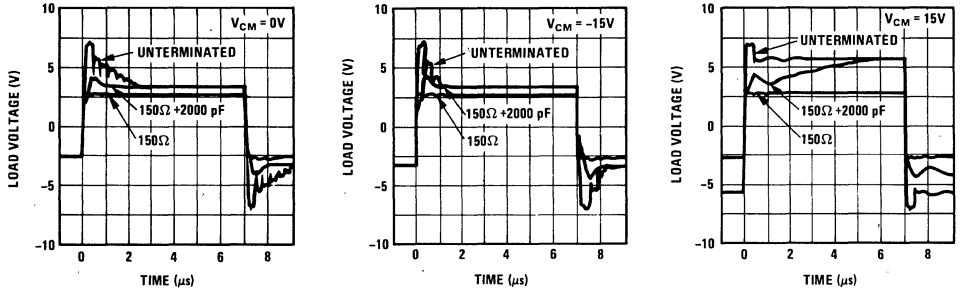


FIGURE 22. Response of Terminated Line With Different DC Isolation Capacitors

In Figure 23, the influence of a varying ground voltage between the transmitter and the receiver is shown. The difference in the characteristics arises because the source resistance of the driver is not constant under all conditions. The high output of



a. V_{CM} = 0V b. V_{CM} = −15V c. V_{CM} = 15V

FIGURE 23. Line Response With Different Terminations and Common Mode Input Voltages

the transmitter looks like an open circuit to voltages reflected from the receiving end of the transmission line which try to drive it higher than its normal dc state. This condition exists until the voltage at the transmitting end becomes high enough to forward bias the clamp diode on the 5V supply. Much of the phenomena which does not follow simple transmission-line theory is caused by this. For example, with an unterminated line, the overshoot comes from the reflected signal charging the line capacitance to where the clamp diodes are forward biased. The overshoot then decays at a rate determined by the total line capacitance and the input resistance of the receiver.

When the ground on the receiver is 15V more negative than the ground at the transmitting end, the decay with an unterminated line is faster, as shown in Figure 23b. This occurs because there is more current from the input resistor of the receiver to discharge the line capacitance. With a terminated line, however, the transmission characteristics are the same as for equal ground voltages because the terminating resistor keeps the line from getting charged.

Figure 23c gives the transmission characteristics when the receiver ground is 15V more positive than the transmitter ground. When the line is not terminated, the differential voltage swing is increased because the high output of the driver will be pulled against the clamp diodes by the common mode input current of the receiver. With a dc isolation capacitor, the differential swing will reach this same value with a time constant determined by the isolation capacitor and the input resistance of the receiver. With a dc coupled termination, the characteristics are unchanged because the differential load current is large by comparison to the common mode current so that the output transistors of the driver are always conducting.

The low output of the driver can also be pulled below ground to where the lower clamp diode conducts, giving effects which are similar to those described for the high output. However, a current of about 9 mA is required to do this, so it does not happen under normal operating conditions.

To summarize, the best termination is an RC combination with a time constant approximately equal to 3 times the transmission-line delay. Even though its value is not precisely determined, the internal termination resistor of the integrated circuit can be used because the line characteristics are not greatly affected by the termination resistor.

The only place that an RC termination can cause problems is when the data transmission rate approaches the line delay and the attenuation down the line (terminated) is greater than 3 dB. This would correspond to more than 1000 ft. of twisted-pair cable with No. 22 copper conductors. Under these conditions, the noise margin can disappear with low-duty-cycle signals. If this is the case, it is best to operate the twisted-pair line without a termination to minimize transmission losses. Reflections should not be a problem as they will be absorbed by the line losses.

CONCLUSION

A method of transmitting digital information in high-noise environments has been described. The technique is a much more attractive solution than high-noise-immunity logic as it has lower power consumption, provides more noise rejection, operates from standard 5V supplies, and is fully compatible with almost all integrated logic circuits. An additional advantage is that the circuits can be fabricated with integrated circuit processes used for standard logic circuits.

APPENDIX A

LINE RECEIVER

Design Analysis

The purpose of this appendix is to derive mathematical expressions describing the operation of the line receiver. It will be shown that the performance of the circuit is not greatly affected by the absolute value of the components within the integrated circuit or by the supply voltage. Instead, it depends mostly on how well the various parts match.

The analysis will assume that all the resistors are well matched in ratio and that the transistors are likewise matched, since this is easily accomplished over a broad temperature range with monolithic construction. However, the effects of component mismatching will be discussed where important. Further, large transistor current gains will be assumed, but it will be pointed out later that this is valid for current gains greater than about 10.

A schematic diagram of the DS7820 line receiver is shown in Figure A-1. Referring to this circuit, the collector current of the input transistor is given by

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} - \frac{\frac{R3}{R4 + 2R6 + R3} V_{BE1} - \frac{R3 \,//\, R11}{R8 + R3 \,//\, R1} V_{IN}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} + \frac{(V_{IN} - V^+) \frac{R10 \,//\, R11}{R9 + R10 \,//\, R11}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} \quad \text{(A. 1)}$$

where V_{IN} is the common mode input voltage and $R_a//R_b$ denotes the parallel connection of the two resistors. In Equation (A. 1), R8 = R9, R3 = R10, R10 << R11, R9 >> R10, R3 << R11, R8 >> R3

and $\frac{R3}{R4 + 2R6 + R3}$ <<3 so it can be reduced to

$$I_{C1} = \frac{V^+ - 3V_{BE} - \frac{R10}{R9} V^+}{R10 + R11 + R3} \quad \text{(A. 2)}$$

which shows that the collector current of Q1 is not affected by the common mode voltage.

The output voltage on the collector of Q2 is

$$V_{C2} = V^+ - I_{C2} R12 \quad \text{(A. 3)}$$

For zero differential input voltage, the collector currents of Q1 and Q2 will be equal so Equation (A. 3) becomes

$$V_{C2} = V^+ - \frac{R12 \left(V^+ - 3V_{BE} - \frac{R10}{R9} V^+\right)}{R10 + R11 + R3} \quad \text{(A. 4)}$$

It is desired that this voltage be $3V_{BE}$ so that the output stage is just on the verge of switching with zero input. Forcing this condition and solving for R12 yields

$$R12 = (R10 + R11 + R3) \frac{V^+ - 3V_{BE}}{V^+ - 3V_{BE} - \frac{R10}{R9} V^+} \quad \text{(A. 5)}$$

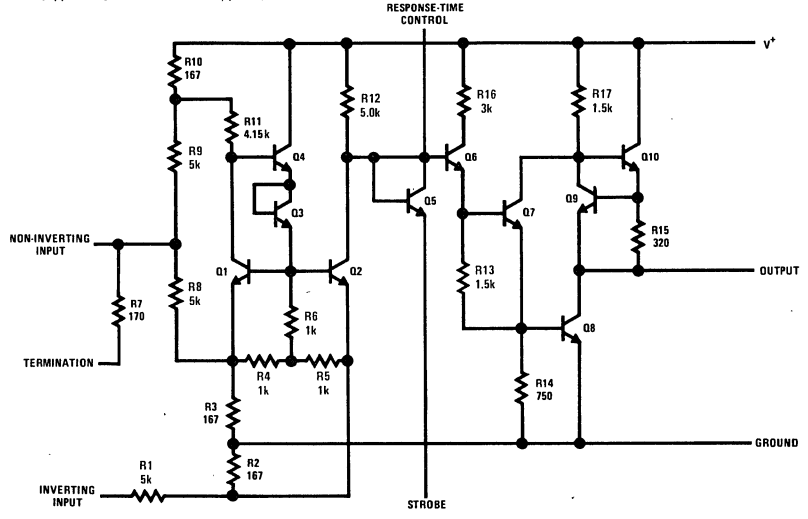


FIGURE A-1. Schematic Diagram of One Half of the DS7820 Line Receiver

This shows that the optimum value of R12 is dependent on supply voltage. For a 5V supply it has a value of 4.7 kΩ. Substituting this and the other component values into (A. 4),

$$V_{C2} = 2.83V_{BE} + 0.081V^{+}, \qquad \text{(A. 6)}$$

which shows that the voltage on the collector of Q2 will vary by about 80 mV for a 1V change in supply voltage.

The next step in the analysis is to obtain an expression for the voltage gain of the input stage.

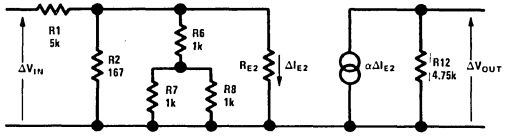


FIGURE A-2. Equivalent Circuit Used to Calculate Input Stage Gain

An equivalent circuit of the input stage is given in Figure A-2. Noting that R6 = R7 = R8 and R2 ≅ 0.1 (R6 + R7//R8), the change in the emitter current of Q1 for a change in input voltage is

$$\Delta I_{E2} = \frac{0.9\ R2}{R1\ (0.9\ R2 + R_{E2})}\ \Delta V_{IN}\ . \qquad \text{(A. 7)}$$

Hence, the change in output voltage will be

$$\Delta V_{OUT} = \alpha I_{E2} R12$$

$$= \frac{0.9\ \alpha\ R2\ R12}{R1\ (0.9\ R2 + R_{E2})}\ \Delta V_{IN}\ . \qquad \text{(A. 8)}$$

Since $\alpha \cong 1$, the voltage gain is

$$A_{V1} = \frac{0.9\ R2\ R12}{R1\ (0.9\ R2 + R_{E2})} \qquad \text{(A. 9)}$$

The emitter resistance of Q2 is given by

$$R_{E2} = \frac{kT}{qI_{C2}}, \qquad \text{(A. 10)}$$

where

$$I_{C2} = \frac{V^{+} - 3V_{BE}}{R12} \qquad \text{(A. 11)}$$

so

$$R_{E2} = \frac{kT\ R12}{q\ (V^{+} - 3V_{BE})} \qquad \text{(A. 12)}$$

Therefore, at 25°C where V_{BE} = 670 mV and kT/q = 26 mV, the computed value for gain is 0.745. The gain is not greatly affected by temperature as the gain at −55°C where V_{BE} = 810 mV and kT/q = 18 mV is 0.774, and the gain at 125°C where V_{BE} = 480 mV and kT/q = 34 mV is 0.730.

With a voltage gain of 0.75, the results of Equation (A. 6) show that the input referred threshold voltage will change by 0.11V for a 1V change in supply voltage. With the standard ±10-percent supplies used for logic circuits, this means that the threshold voltage will change by less than ±60 mV.

Finally, the threshold error due to finite gain in the output stage can be considered. The collector current of Q7 from the bleeder resistor R14, is large by comparison to the base current of Q8, if Q8 has a reasonable current gain. Hence, the collector current of Q7 does not change appreciably when the output switches from a logic one to a logic zero. This is even more true for Q6, an emitter follower which drives Q7. Therefore, it is safe to presume that Q6 does not load the output of the first-stage amplifier, because of the compounded current gain of the three transistors, and that Q8 is driven from a low resistance source.

It follows that the gain of the output stage can be determined from the change in the emitter-base voltage of Q8 required to swing the output from a logic one state to a logic zero state. The expression

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \qquad \text{(A. 13)}$$

describes the change in emitter-base voltage required to vary the collector current from one value, I_{C1}, to a second, I_{C2}. With the output of the receiver in the low state, the collector current of Q8 is

$$I_{OL} = \frac{V^{+} - V_{OL} - V_{BE9} - V_{BE10}}{R17}$$

$$+ \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} + I_{SINK}\ , \qquad \text{(A. 14)}$$

where V_{OL} is the low state output voltage and I_{SINK} is the current load from the logic that the receiver is driving. Noting that R13 = 2R14 and figuring that all the emitter-base voltages are the same, this becomes

$$I_{OL} = \frac{V^{+} - V_{OL} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15}$$

$$- \frac{V_{BE}}{2R14} + I_{SINK}\ . \qquad \text{(A. 15)}$$

Similarly, with the output in the high state, the collector current of Q8 is

$$I_{OH} = \frac{V^{+} - V_{OH} - V_{BE9} - V_{BE10}}{R17}$$

$$+ \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14}$$

$$+ \frac{V_{BE7}}{R13} - I_{SOURCE}\ , \qquad \text{(A. 16)}$$

where V_{OH} is the high-level output voltage and I_{SOURCE} is the current needed to supply the input leakage of the digital circuits loading the comparator.

With the same conditions used in arriving at (A. 15), this becomes

$$I_{OH} = \frac{V^+ - V_{OH} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15}$$

$$- \frac{V_{BE}}{2R14} - I_{SOURCE} \cdot \qquad \text{(A. 17)}$$

From (A. 13) the change in the emitter-base voltage of Q8 in going from the high output level to the low output level is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{OL}}{I_{OH}} \qquad \text{(A. 18)}$$

providing that Q8 is not quite in saturation, although it may be on the verge of saturation.

The change of input threshold voltage is then

$$\Delta V_{TH} = \frac{kT}{qA_{V1}} \log_e \frac{I_{OL}}{I_{OH}} \qquad \text{(A. 19)}$$

where A_{V1} is the input stage gain. With a worst case fanout of 2, where V_{OH} = 2.5V, V_{OL} = 0.4V, I_{SOURCE} = 40 μA and I_{SINK} = 3.2 mA, the calculated change in threshold is 37 mV at 25°C, 24 mV at -55°C and 52 mV at 125°C.

The measured values of overall gain differ by about a factor of two from the calculated gain. This is not too surprising because a number of assumptions were made which introduce small errors, and all these errors lower the gain. It is also not too important because the gain is high enough where another factor of two reduction would not cause the circuit to stop working.

The main contributors to this discrepancy are the non-ideal behavior of the emitter-base voltage of Q8 due to current crowding under the emitter and the variation in the emitter base voltage of Q7 and Q8 with changes in collector-emitter voltage (h_{RE}).

Although these parameters can vary considerably with different manufacturing methods, they are relatively fixed for a given process. The ΔV_{BE} errors introduced by these quantities, if known, can be added directly into Equation (A. 18) to give a more accurate gain expression.

The most stringent matching requirement in the receiver is the matching of the input stage divider resistors: R1 with R8 and R2 with R3. As little as 1% mismatch in one of these pairs can cause a threshold shift of 150 mV at the extremes of the ±15V common mode range. Because of this, it is necessary to make the resistors absolutely identical and locate them close together. In addition, since R1 and R8 do dissipate a reasonable amount of power, they have to be located to minimize the thermal gradient between them. To do this, R9 was located between R1 and R8 so that it would heat both of these resistors equally. There are not serious heating problems with R2 and R3; however, because of their low resistance value, it was necessary even to match the lengths of the aluminum interconnects, as the resistance of the aluminum is high enough to cause intolerable mismatches. Of secondary importance is the matching of Q1 and Q2 and the matching of ratios between R11 and R12. A 1 mV difference in the emitter-base voltages of Q1 and Q2 causes a 30 mV input offset voltage as does a 1% mismatch in the ratio of R11 to R12.

The circuit is indeed insensitive to transistor current gains as long as they are above 10. The collector currents of Q4 and Q6 are made equal so that their base currents load the collectors of Q1 and Q2 equally. Hence, the input threshold voltage is affected only by how well the current gains match. Low current gain in the output transistor, Q8, can cause a reduction in gain. But even with a current gain of 10, the error produced in the input threshold voltage is less than 50 mV.

Transmission Line Characteristics

National Semiconductor
Bill Fowler
May 1974

INTRODUCTION

Digital systems generally require the transmission of digital signals to and from other elements of the system. The component wavelengths of the digital signals will usually be shorter than the electrical length of the cable used to connect the subsystems together and, therefore, the cables should be treated as a transmissions line. In addition, the digital signal is usually exposed to hostile electrical noise source which will require more noise immunity then required in the individual subsystems environment.

The requirements for transmission line techniques and noise immunity are recognized by the designers of subsystems and systems, but the solution used vary considerably. Two widely used example methods of the solution are shown in *Figure 1*. The two methods

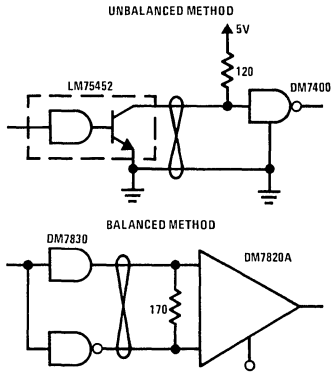


FIGURE 1.

illustrated use unbalanced and balanced circuit techniques. This application note will delineate the characteristics of digital signals in transmission lines and characteristics of the line that effect the quality, and will compare the unbalanced and balanced circuits performance in digital systems.

NOISE

The cables used to transmit digital signals external to a subsystem and in route between the subsystem, are exposed to external electromagnetic noise caused by switching transients from actuating devices of neighboring control systems. Also external to a specific subsystem, another subsystem may have a ground problem which will induce noise on the system, as indicated in *Figure 2*.

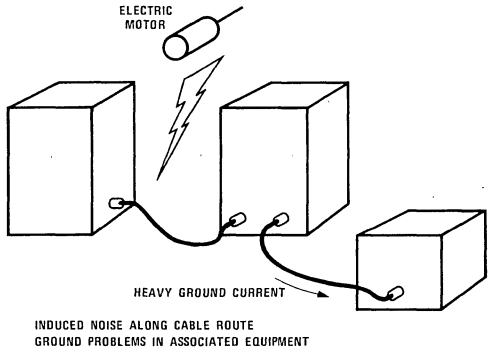


FIGURE 2. External Noise Sources

The signals in adjacent wires inside a cable may induce electromagnetic noise on other wires in the cable. The induced electromagnetic noise is worse when a line terminated at one end of the cable is near to a driver at the same end, as shown in *Figure 3*. Some noise may be

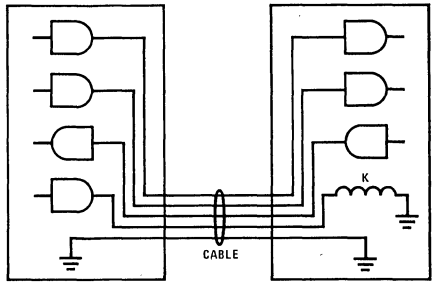


FIGURE 3. Internal Noise Sources

induced from relay circuits which have very large transient voltage swings compared to the digital signals in the same cable. Another source of induced noise is current in the common ground wire or wires in the cable.

DISTORTION

The objective is the transmission and recovery of digital intelligence between subsystems, and to this end, the characteristics of the data recovered must resemble the data transmitted. In *Figure 4* there is a difference in the pulse width of the data and timing signal transmitted, and the corresponding signal received. In addition there is a further difference in the signal when the data is "AND"ed with the timing signal. The distortion of the signal occurred in the transmission line and in the line driver and receiver.

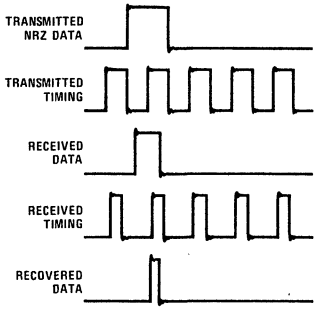


FIGURE 4. Effect of Distortion

A primary cause of distortion is the effect the transmission line has on the rise time of the transmitted data. *Figure 5* shows what happens to a voltage step from the driver as it travels down the line. The rise time of the signal increases as the signal travels down the line. This effect will tend to affect the timing of the recovered signal.

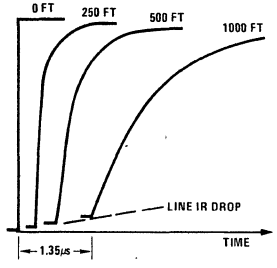


FIGURE 5. Signal Response at Receiver

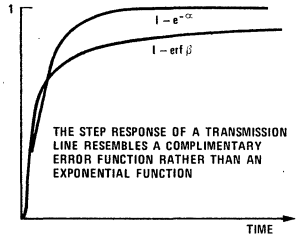


FIGURE 6. Signal Rise Time

The rise time in a transmission line is not an exponential function but a complementary error function. The high frequency components of the step input are attenuated and delayed more than the low frequency components. This attenuation is inversely proportional to the frequency. Notice in *Figure 6* particularly that the signal takes much longer to reach its final dc value. This effect is more significant for fast risetimes.

The Duty Cycle of the transmitted signal also causes distortion. The effect is related to the signal rise time as shown in *Figure 7*. The signal doesn't reach one logic level before the signal changes to another level. If the signal has a 1/2 (50%) Duty Cycle and the threshold of the receiver is halfway between the logic levels, the distortion is small. But if the Duty Cycle is 1/8 as shown in the second case the signal is considerably distorted. In some cases, the signal may not reach the receiver threshold at all.

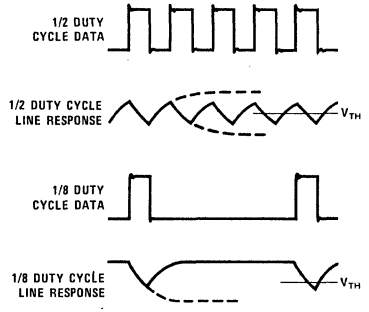


FIGURE 7. Signal Distortion Due to Duty Cycle

In the previous example, it was assumed that the threshold of the receiver was halfway between the ONE and ZERO logic levels. If the receiver threshold isn't halfway the receiver will contribute to the distortion of the recovered signal. As shown in *Figure 8*, the pulse time is lengthened or shortened, depending on the polarity of the signal at the receiver. This is due to the offset of the receiver threshold.

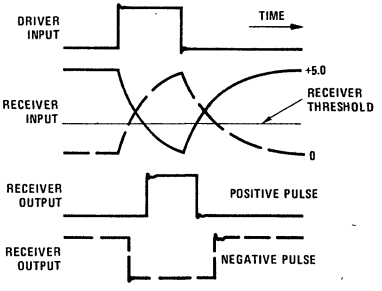


FIGURE 8. Slicing Level Distortion

UNBALANCED METHOD

Another source of distortion is caused by the IR losses in the wire. *Figure 9* shows the IR losses that occur in a thousand feet of no. 22 AWG wire. Notice in this

example that the losses reduce the signal below the threshold of the receiver in the unbalanced method. Also that part of the IR drop in the ground wire is common to other circuits—this ground signal will appear as a source of noise to the other unbalanced line receivers in the system.

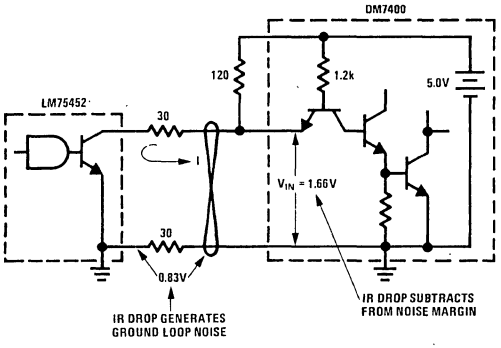


FIGURE 9. Unbalanced Method

Transmission lines don't necessarily have to be perfectly terminated at both ends, (as will be shown later) but the termination used in the unbalanced method will cause additional distortion. *Figure 10* shows the signal on the transmission line at the driver and at the receiver. In this case the receiver was terminated in 120Ω, but the characteristic impedance of the line is much less. Notice that the wave forms have significant steps due to the incorrect termination of the line. The signal is subject to misinterpretation by the line receiver during the period of this signal transient because of the distortion caused by Duty Cycle and attenuation. In addition, the noise margin of the signal is reduced.

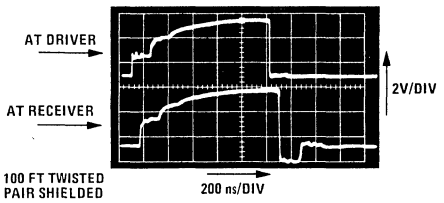


FIGURE 10. LM75451, DM7400 Line Voltage Waveforms

The signal waveforms on the transmission line can be estimated before hand by a reflection diagram. *Figure 11* shows the reflection diagram of the rise time wave forms. The voltage versus current plot on left is used to predict the transient rise time of the signal shown on the right. The initial condition on the transmission line is an IR drop across the line termination. The first transient on the line traverses from this initial point to zero current. The path it follows corresponds to the characteristic impedance of the line. The second transient on the diagram is at the line termination. As shown, the signal reflects back and forth until it reaches its final dc value.

Figure 12 shows the reflection diagram of the fall time. Again the signal reflects back and forth between the line termination until it reaches its final dc value. In both the rise and fall time diagrams, there are transient voltage and current signals that subtract from the particular signal and add to the system noise.

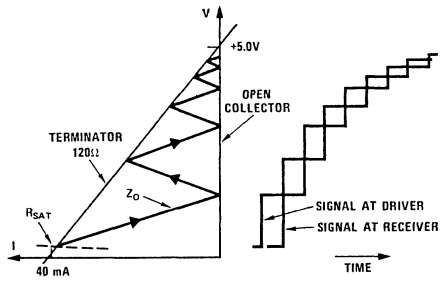


FIGURE 11. Line Reflection Diagram of Rise Time

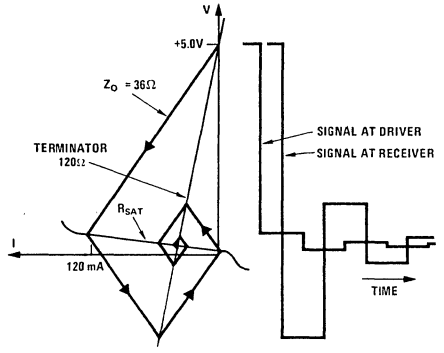
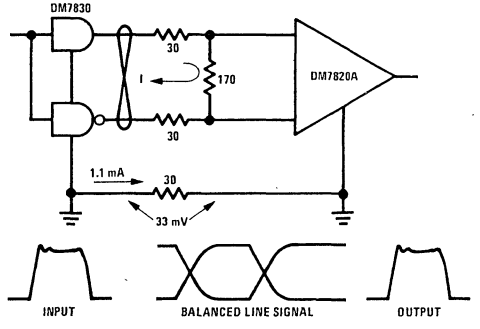


FIGURE 12. Line Reflection Diagram of Fall Time

BALANCED METHOD

In the balanced method shown in *Figure 13*, the transient voltages and currents on the line are equal and



THE GROUND LOOP CURRENT IS MUCH LESS THAN SIGNAL CURRENT

FIGURE 13. Cross Talk of Signals

opposite and cancel each others noise. Also unlike the unbalanced method, they generate very little ground noise. As a result, the balanced circuit doesn't contribute to the noise pollution of its environment.

The circuit used for a line receiver in the balanced method is a differential amplifier. Figure 14 shows a noise transient induced equally on line A and line B from line C. Because the signals on line A and B are equal, the signals are ignored by the differential line receiver.

Likewise for the same reason, the differential signals on line A and B from the driver will not induce transients on line C. Thus, the balanced method doesn't generate noise and also isn't susceptible to noise. On the other hand the unbalanced method is more sensitive to noise and also generates more noise.

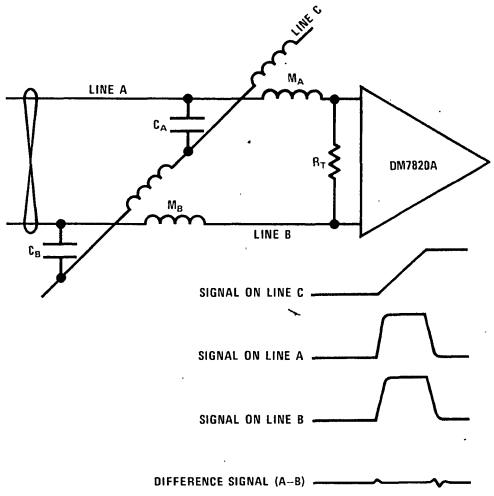


FIGURE 14. Cross Talk of Signals

The characteristic impedance of the unbalanced transmission line is less than the impedance of the balanced transmission line. In the unbalanced method there is more capacitance and less inductance than in the balanced method. In the balance method the Reactance to adjacent wires is almost cancelled (see *Figure 15*). As a result a transmission line may have a 60Ω unbalanced impedance and a 90Ω balanced impedance. This means that the unbalanced method, which is more susceptible to IR drop, must use a smaller value termination, which will further increase the IR drop in the line.

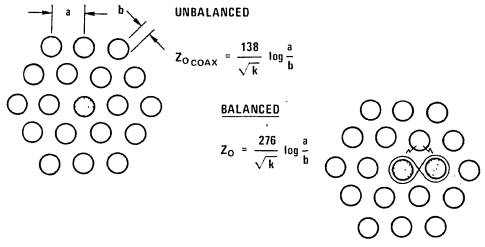


FIGURE 15. Z_O Unbalanced < Z_O Balanced

The impedance measurement of an unbalance and balance line must be made differently. The balanced impedance must be measured with a balanced signal. If there is any unbalance in the signal on the balanced line, there will be an unbalance reflection at the terminator. Therefore, the lines should also be terminated for unbalanced signals. *Figure 16* shows the perfect termination configuration of a balanced transmission line. This termination method is primarily required for accurate impedance measurements.

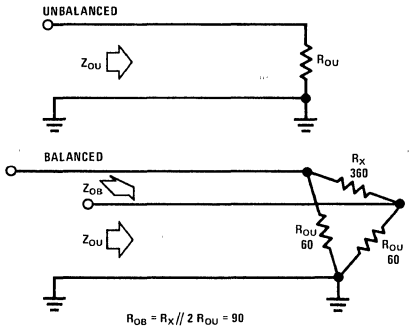


FIGURE 16. Impedance Measurement

MEASURED PERFORMANCE

The unbalanced method circuit used in this application note up to this point is the unbalanced circuit shown in *Figure 1*. The termination of its transmission line was greater than the characteristic impedance of the unbalanced line and the circuit had considerable threshold offset. The measured performance of the unbalanced circuit wasn't comparable to the balanced method. Therefore, for the following comparison of unbalanced and balanced circuits, an improved termination shown in *Figure 17* will be used. This circuit terminates the line in 60Ω and minimized the receiver threshold offset.

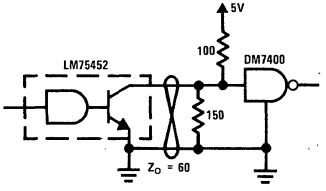


FIGURE 17. Improved Unbalanced Method

A plot of the Absolute Maximum Data Rate versus cable type is shown in *Figure 18*. The graph shows the different performances of the DM7820A line receiver and

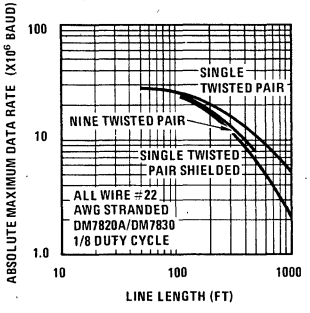


FIGURE 18. Data Rate vs Cable Type

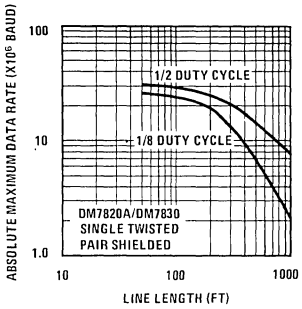


FIGURE 19. Data Rate vs Duty Cycle

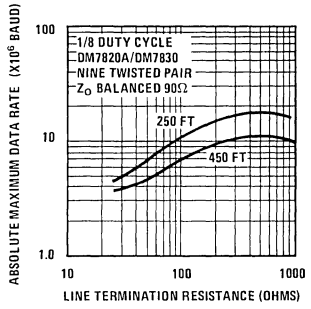


FIGURE 20. Data Rate vs Line Termination

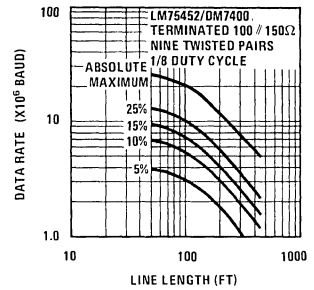


FIGURE 21. Data Rate vs Distorion of LM75452, DM7400

the DM7830 line driver circuits with a worse case 1/8 Duty Cycle in no. 22 AWG stranded wire cables. In a single twisted pair cable there is less reactance than in a cable having nine twisted pairs and in turn this cable has less reactance than shielded pairs. The line length is reduced in proportion to the increased line attenuation which is proportional to the line reactance. The plot shows that the reactance and attenuation has a significant effect on the cable length. Absolute Maximum Data Rate is defined as the Data Rate at which the output of the line receiver is starting to be degraded. The roll off of the performance above 20 mega baud is due to the circuit switching response limitation.

Figure 19 shows the reduction in Data Rate caused by Duty Cycle. It can be observed that the Absolute Maximum Duty Rate of 1/8 Duty Cycle is less than 1/2 Duty Cycle. The following performance curves will use 1/8 Duty Cycle since it is the worst case.

Absolute Maximum Duty Rate versus the Line Termination Resistance for two different lengths of cable is shown in *Figure 20*. It can be seen from the figure that the termination doesn't have to be perfect in the case of balanced circuits. It is better to have a termination resistor to minimize the extra transient signal reflecting between the ends of the line. The reason the Data Rate increases with increased Termination Resistance is that there is less IR drop in the cable.

The graphs in *Figure 21* shows the Data Rate versus the Line Length for various percentage of timing distortion using the unbalanced LM75452 and DM7400 circuits shown in *Figure 17*. The definition of Timing Distortion is the percentage difference in the pulse width of the data sent versus the data received.

Data Rate versus the Line Length for various percentage of timing distorition using the balanced DM7820A and DM7830 circuit is shown in *Figure 22*. The distortion of this method is improved over the unbalanced method, as was previously theorized.

The Absolute Maximum Data Rate versus Line Lengths shown in the previous two figures didn't include any induced signal noise. *Figure 23* shows the test configuration of the unbalanced circuits which was used to measure near end cross talk noise. In this configuration there are eight line drivers and one receiver at one end of the cable. The performance of the receiver measured in the presence of the driver noise is shown in *Figure 24*.

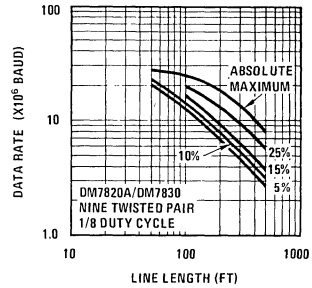


FIGURE 22. Data Rate vs Distorion of DM7820A, DM7830

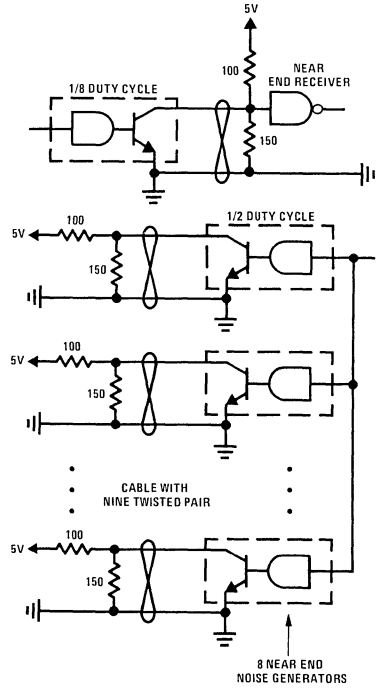


FIGURE 23. Signal Cross Talk Experiment Using DM75452, DM7400

Figure 24 shows the Absolute Maximum Duty Rate of the unbalanced method versus line length and versus the number of line drivers corresponding to the test configuration delineated in *Figure 23.* In the noise measurement set-up there was a ground return for each signal wire. If there is only one ground return in the cable the performance is worse. The graph shows that the effective line length is drastically reduced as additional Near End Drivers are added. When this performance is compounded by timing distortion the performance is further reduced.

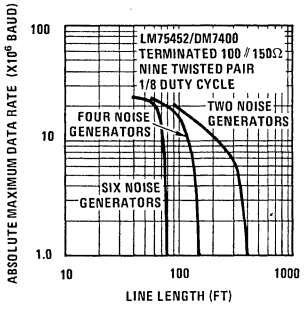


FIGURE 24. Data Rate vs Signal Cross Talk of LM75452, DM7400

Figure 25 shows the test configuration of the balanced circuit used to generate worst case Near End cross talk

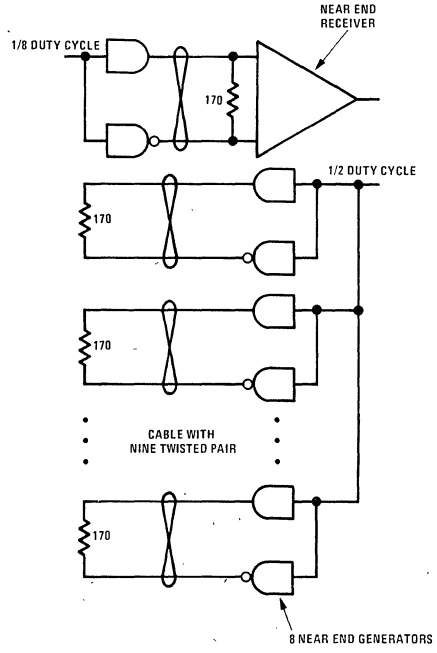


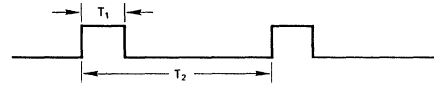
FIGURE 25. Signal Cross Talk Experiment Using DM7830, DM7820A

noise similar to the unbalance performance shown in the previous figure. Unlike the unbalanced case, there was no measurable degradation of the circuits Data Rate or distortion.

CONCLUSION

National has a full line of both Balanced and Unbalanced Line Drivers and Receivers. Both circuit types work well when used within their limitations. This application note shows that the balanced method is preferable for long lines in noisy electrical evironments. On the other hand the unbalanced circuit works perfectly well with shorter lines and reduced data rates. It should be kept in mind that when you are spending $500,000 for a CPU and $75,000 for peripherals, it pays to investigate the best way to transmit data between them.

DEFINITION OF BAUD RATE



$$\text{BIT RATE} = \frac{1}{\text{INTERVAL PER BIT}} = \frac{1}{T_2}$$

$$\text{BAUD RATE} = \frac{1}{\text{MINIMUM UNIT INTERVAL}} = \frac{1}{T_1}$$

The data in this note was plotted versus Baud Rate. The minimum unit interval reflected the worse case conditions and also normalized the diagrams so that the diagrams were independent of duty cycle. If the duty cycle is 50% then the Baud Rate is twice the Bit Rate.

REFERENCES

IC's for Digital Data Transmission , Widlar and Kubinec, *National Semiconductor Application Note AN-22.*

Data Bus and Differential Line Drivers and Receivers, Richard Percival, *National Semiconductor Application Note AN-83.*

RADC TR73-309, Experimental Analysis of the Transmission of Digital Signals over Twisted Pair Cable, Hendrickson and Evanowski, *Digital Communication Section Communications and Navigation Division,* Rome Air Development Center, Griffis Air Force Base, New York.

Fast Pulse Techniques, Thad Dreher, E-H Research Laboratories, Inc., *The Electronic Engineer,* Aug. 1969.

Transient Analysis of Coaxial Cables, Considering Skin Effects, Wigingtom and Nahmaj, *Proceedings of the IRE,* Feb. 1957.

Reflection and Crosstalk in Logic, Circuit Interconnections, John DeFalco, Honeywell, Inc., *IEEE Spectrum,* July 1970.

Transmission Line Drivers and Receivers for EIA Standards RS-422 and RS-423

National Semiconductor
Application Note 214
John Abbott
October 1978

With the advent of the microprocessor, logic designs have become both sophisticated and modular in concept. Frequently the modules making up the system are very closely coupled on a single printed circuit board or cardfile. In a majority of these cases a standard bus transceiver will be adequate. However because of the distributed intelligence ability of the microprocessor, it is becoming common practice for the peripheral circuits to be physically separated from the host processor with data communications being handled over cables (e.g. plant environmental control or security system). And often these cables are measured in hundreds or thousands of feet as opposed to inches on a backplane. At this point the component wavelengths of the digital signals may become shorter than the electrical length of the cable and consequently must be treated as transmission lines. Further, these signals are exposed to electrical noise sources which may require greater noise immunity than the single chassis system.

It is the object of this application note to underscore the more important design requirements for balanced and unbalanced transmission lines, and to show that National's DS1691 driver and DS78LS120 receiver meet or exceed all of those requirements.

THE REQUIREMENTS

The requirements for transmission lines and noise immunity have been adequately recognized by National Semiconductor's application note AN-108 and E.I.A. standards RS-422 (balanced) and RS-423 (unbalanced). A summary review of these notes will show that the controlling factors in a voltage digital interface are:

1) The cable length

2) The modulation rate

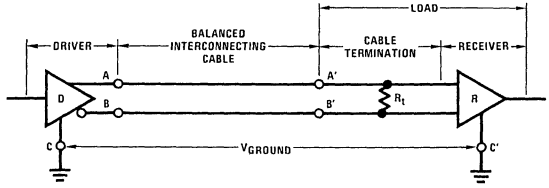
3) The characteristic of the interconnection cable

4) The rise time of the signal

RS-422 and RS-423 contain several useful guidelines relative to the choice of balanced circuits versus unbalanced circuits. *Figures 1a and 1b* are the digital interface for balanced *(1a)* and unbalanced *(1b)* circuits.

Even though the unbalanced interface circuit is intended for use at lower modulation rates than the balanced circuit, its use is not recommended where the following conditions exist:

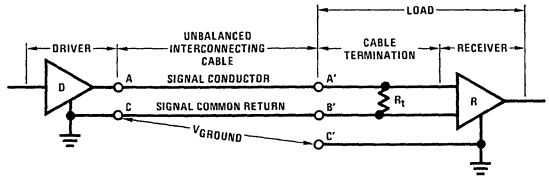
1) The interconnecting cable is exposed to noise sources which may cause a voltage sufficient to indicate a change of binary state at the load.
2) It is necessary to minimize interference with other signals, such as data versus clock.
3) The interconnecting cable is too long electrically for unbalanced operation *(Figure 2)*



Legend:

R_t = Optional cable termination resistance/receiver input impedance.
V_{GROUND} = Ground potential difference
A, B = Driver interface
A', B' = Load interface
C = Driver circuit ground
C' = Load circuit ground

FIGURE 1a. RS-422 Balanced Digital Interface Circuit



Legend:

R_t = Transmission line termination and/or receiver input impedance
V_{GROUND} = Ground potential difference
A, C = Driver interface
A', B' = Load interface
C = Driver circuit ground
C' = Load circuit ground

FIGURE 1b. RS-423 Unbalanced Digital Interface Circuit

CABLE LENGTH

While there is no maximum cable length specified, guidelines are given with respect to conservative operating distances as a function of modulation rate. *Figure 2* is a composite of the guidelines provided by RS-422 and RS-423 for data modulation versus cable length. The data is for 24 AWG twisted pair cable terminated for worst case (due to IR drop) in a 100 Ohm load, with rise and fall times equal to or less than one half unit interval at the applied modulation rate.

The maximum cable length between driver and load is a function of the baud rate. But it is influenced by:

1) A maximum common noise range of ±7 volts
   A) The amount of common-mode noise
      Difference of driver and receiver ground potential plus driver offset voltage and coupled peak random noise.
   B) Ground potential differences between driver and load.
   C) Cable balance
      Differential noise caused by imbalance between the signal conductor and the common return (ground)
2) Cable termination
   At rates above 200 kilobaud or where the rise time is 4 times the one way propagation delay time of the cable (RS-422 Sec 7.1.2)
3) Tolerable signal distortion

MODULATION RATE

Section 3 of RS-422 and RS-423 states that the unbalanced voltage interface will normally be utilized on data, timing or control circuits where the modulation rate on these circuits is below 100 kilobauds, and balanced voltage digital interface on circuits up to 10 megabauds. The voltage digital interface devices meeting the electrical characteristics of this standard need not meet the entire modulation range specified. They may be designed to operate over narrower ranges to more economically satisfy specific applications, particularly at the lower modulation rates.

As pointed out in AN-108, the duty cycle of the transmitted signal contributes to the distortion. The effect is the result of rise time. Due to delay and attenuation caused by the cable, it is possible due to AC averaging of the signal, to be unable to reach one binary level before it is changed to another. If the duty cycle is 1/2 (50%) and the receiver threshold is midway between logic levels, the distortion is small. However if the duty cycle were 1/8 (12.5%) the signal would be considerably distorted.

CHARACTERISTICS

Driver Unbalanced (RS-423)

The unbalanced driver characteristics as specified by RS-423 Sec 4.1 are as follows:

1) A driver circuit should be a low impedance (50 Ohms or less) unbalanced voltage source that will produce a voltage applied to the interconnecting cable in the range of 4 volts to 6 volts.
2) With a test load of 450 Ohms connected between the driver output terminal and the driver circuit ground, the magnitude of the voltage (VT) measured between the driver output and the driver circuit ground shall not be less than 90% of the magnitude for either binary state.
3) During transitions of the driver output between alternating binary states, the signal measured across a 450 Ohm test load connected between the driver output and circuit ground should be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS}. Thereafter, the signal shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT and $\overline{VT}$ exceed 6 volts, nor be less than 4 volts. V_{SS} is defined as the voltage difference between the 2 steady state values of the driver output.

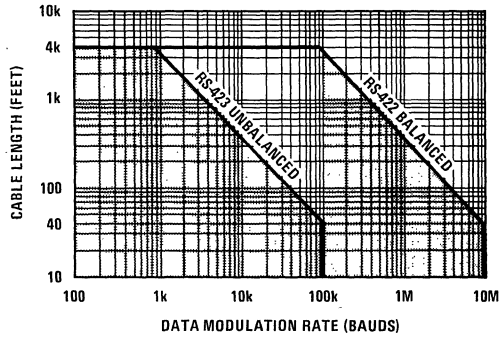
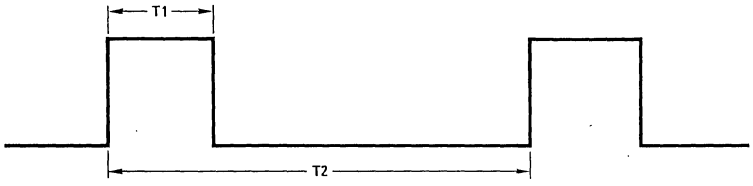


FIGURE 2. Data Modulation Rate vs Cable Length



$$\text{Bit Rate} = \frac{1}{\text{Interval Per Bit}} = \frac{1}{T2}$$

$$\text{Baud Rate} = \frac{1}{\text{Minimum Unit Interval}} = \frac{1}{T1}$$

FIGURE 3a. Definition of Baud Rate

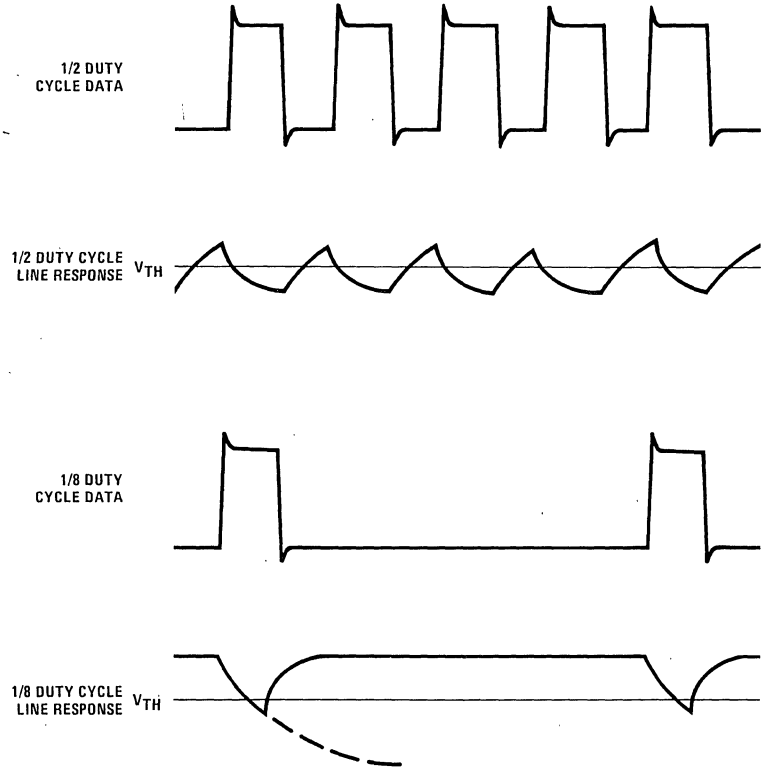
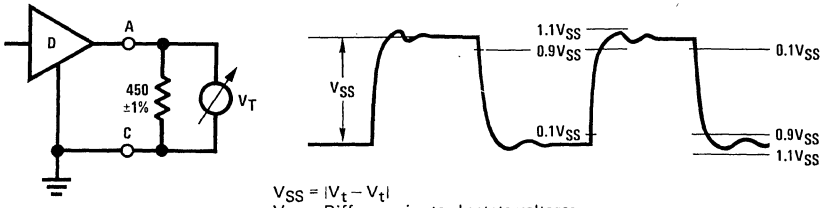


FIGURE 3b. Signal Distortion Due to Duty Cycle



$V_{SS} = |V_t - V_t|$
V_{SS} = Difference in steady state voltages.

FIGURE 4. Unbalanced Driver Output Signal Waveform

Driver Balanced (RS-422)

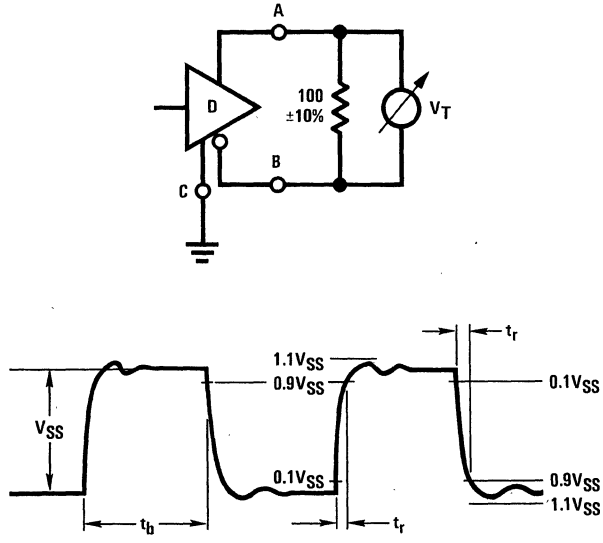
The balanced driver characteristics as specified by RS-422 Sec 4.1 are as follows:

1) A driver circuit should result in a low impedance (100 Ohms or less) balanced voltage source that will produce a differential voltage applied to the interconnecting cable in the range of 2 volts to 6 volts.
2) With a test load of 2 resistors, 50 Ohms each, connected in series between the driver output terminals, the magnitude of the differential voltage (VT) measured between the 2 output terminals shall not be less than either 2.0 volts or 50% of the magnitude of V_O, whichever is greater. For the opposite binary state the polarity of VT shall be reversed ($\overline{VT}$). The magnitude of the difference in the magnitude of VT and $\overline{VT}$ shall be less than 0.4 volts. The magnitude of the driver offset voltage (V_{OS}) measured between the center point of the test load and driver circuit ground shall not be greater than 3.0 volts. The magnitude of the difference in the magnitude of V_{OS} for one binary state and $\overline{V_{OS}}$ for the opposing binary state shall be less than 0.4 volts.
3) During transitions of the driver output between alternating binary states, the differential signal measured across a 100 Ohm test load connected between the driver output terminals shall be such that the voltage monotonically changes between 0.1 and 0.9 of V_{SS} within 0.1 of the unit interval or 20 nanoseconds, whichever is greater. Thereafter the signal voltage shall not vary more than 10% of V_{SS} from the steady state value, until the next binary transition occurs, and at no time shall the instantaneous magnitude of VT or $\overline{VT}$ exceed 6 volts, nor less than 2 volts.

Interconnecting Cable

The characteristics of the interconnecting cable should result in a transmission line with a characteristic impedance in the general range of 100 Ohms to frequencies greater than 100 kilohertz, and a DC series loop resistance not exceeding 240 Ohms. The cable may be composed of twisted or untwisted pair (flat cable) possessing the characteristics specified in RS-422 Sec 4.3 as follows:

1) Conductor size of the 2 wires shall be 24 AWG or larger with wire resistance not to exceed 30 Ohms per 1000 feet per conductor
2) Mutual pair capacitance between 1 wire in the pair to the other shall not exceed 20 pF per foot.
3) Stray capacitance between 1 wire in the pair with all other wires connected to ground, shall not exceed 40 pF per foot.



t_b = Time duration of the unit interval at the applicable modulation rate.
$t_r \leq 0.1\ t_b$ when $t_b \geq 200$ ns
$t_r \leq 20$ ns when $t_b < 200$ ns
V_{SS} = Difference in steady state voltages
$V_{SS} = |V_t - V_t|$

FIGURE 5. Balanced Driver Output Signal Waveform

Receiver

The load characteristics are identical for both balanced (RS-422) and unbalanced (RS-423) circuits. Each consists of a receiver and optional termination resistance as shown in *Figure 1*. The electrical characteristics single receiver without termination or optional fail-safe provisions are specified in RS-422/423 Sec 4.2 as follows:

1) Over an entire common-mode voltage range of −7 to +7 volts, the receiver shall not require a differential input voltage or more than 200 millivolts to correctly assume the intended binary state. The common-mode voltage (V_{CM}) is defined as the algebraic mean of the 2 voltages appearing at the receiver input terminals with respect to the receiver circuit ground. Reversing the polarity of VT shall cause the receiver to assume the opposite binary state. This allows for operations where there are ground differences caused by IR drop and noise of up to ±7 volts.
2) To maintain correct operation for differential input signal voltages ranging between 200 millivolts and 6 volts in magnitude.
3) The maximum voltage present between either receiver input terminal and receiver circuit ground shall not exceed 10 volts (3 volt signal plus 7 volts common-mode) in magnitude nor cause the receiver to operationally fail. Additionally, the receiver shall tolerate a maximum differential signal of 12 volts applied across its input terminals without being damaged.
4) The total load including up to 10 receivers shall not have a resistance greater than 90 Ohms for balanced, and 400 Ohms unbalanced at its input points and shall not require a differential input voltage of greater than 200 millivolts for all receivers to assume the correct binary state.

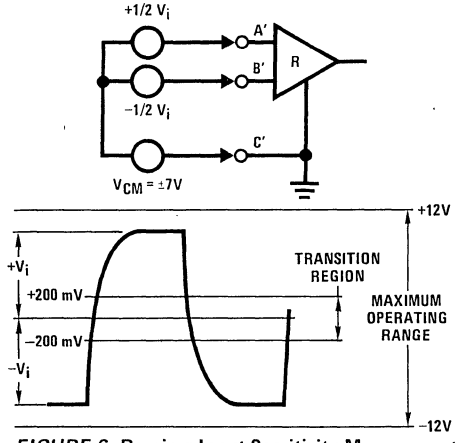


FIGURE 6. Receiver Input Sensitivity Measurement

Note: Designers of terminating hardware should be aware that slow signal transitions with superimposed noise present may give rise to instability or oscillations in the receiving device, and therefore appropriate techniques should be implemented to prevent such behavior. For example, adequate hysteresis and response control may be incorporated into the receiver to prevent such conditions.

5) Fail-safe operation per RS-423 Sec 4.2.5 states that other standards and specifications using the electrical characteristics of the unbalanced interface circuit may require that specific interchange leads be made fail-safe to certain fault conditions. Where fail-safe operation is required by such referencing standards and specifications, a provision shall be incorporated in the load to provide a steady binary condition (either "1" or "0") to protect against certain fault conditions (open or shorted cable).

   The designer should be aware that in circuits employing pull-up resistors, the resistors used become part of the termination.

SIGNAL RISE TIME

The signal rise time is a high frequency component which causes interference (near end cross-talk) to be coupled to adjacent channels in the interconnecting cable. The near-end crosstalk is a function of both rise time and cable length, and in considering wave shaping, both should be considered. Since in the balanced voltage digital interface the output is complementary, there is practically no cross-talk coupled and therefore wave shaping is limited to unbalanced circuits.

Per RS-423 Sec 4.1.6, the rise time of the signal should be controlled so that the signal has reached 90% of V_{SS} between 10% and 30% of the unit interval at the maximum modulation rate. Below 1 kilobaud the time to reach 90% V_{SS} shall be between 100 and 300 microseconds. If a driver is to operate over a range of modulation rates and employ a fixed amount of wave shaping which meets the specification for the maximum modulation rate of the operating range, the wave shaping is considered adequate for all lesser modulation rates.

However a major cause of distortion is the effect the transmission line has on the rise time of the transmitted signal. *Figure 7* shows the effect of line attenuation and delay to a voltage step as it progresses down the cable. The increase of the rise time with distance will have a considerable effect on the distortion at the receiver. Therefore in fixing the amount of wave shaping employed, caution should be taken not to use more than the minimum required.

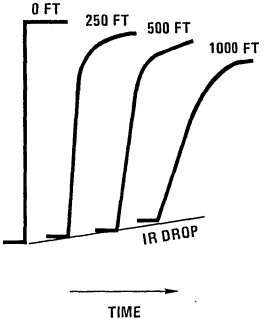


FIGURE 7. Signal Rise Time on Transmission Line vs Line Length

The Driver

The DS1691/DS3691 are low power Schottky TTL line drivers designed to meet the above listed requirements of EIA standard RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. The DS1691/DS3691 employ a mode selection pin which allows the circuit to become either a pair of balanced drivers *(Figure 8)* or 4 independent unbalanced drivers *(Figure 9)*. When configured for unbalanced operation *(Figure 10)* a rise time control pin allows the use of an external capacitor to control rise time for suppression of near end cross-talk to adjacent channels in the interconnect cable. *Figure 11* is the typical rise time vs external capacitor used for wave shaping.

The DS3691 configured for RS-422 is connected V_{CC} = 5V V_{EE} = 0V, and configured for RS-423 connected V_{CC} = 5V V_{EE} = −5V. For applications outside RS-422 conditions and for greater cable lengths the DS1691/DS3691 may be connected with a V_{CC} of 5 volts and V_{EE} of −5 volts. This will create an output which is symmetrical about ground, similar to Mil Standard 188-114.

When configured as balanced drivers *(Figure 8)*, each of the drivers is equipped with an independent TRI-STATE® control pin. By use of this pin it is possible to force the driver into its high impedance mode for applications using party line techniques.

If the common-mode voltage, between driver 1 and all other drivers in the circuit, is small then several line drivers (and receivers) may be incorporated into the system. However, if the common-mode voltage exceeds the TRI-STATE common-mode range of any driver, then the signal will become attenuated by that driver to the extent the common-mode voltage exceeds its common-mode range (See *Figure 12*, top waveform).

It is important then to select a driver with a common-mode range equal to or larger than the common-mode voltage requirement of the system. In the case of RS-422 and RS-423 the minimum common-mode range would be ±7 volts. The DS1692/DS3692 driver is tested to a common-mode range of ±10 volts and will operate within the requirements of such a system (See *Figure 12*, bottom waveform).

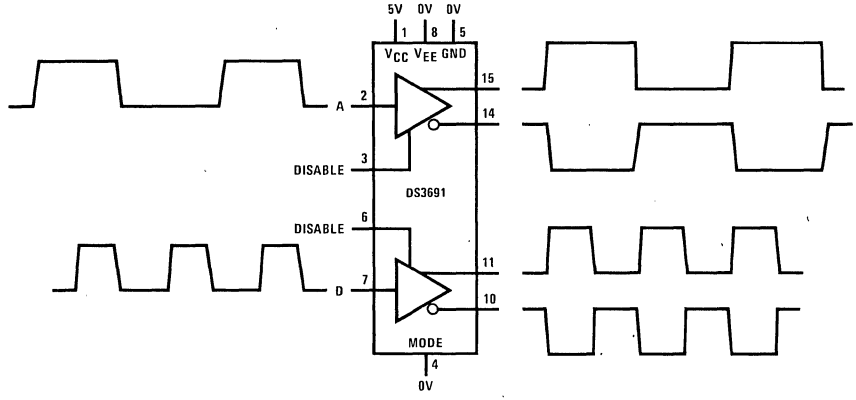


FIGURE 8. DS3691 Connected for Balanced Mode Operation

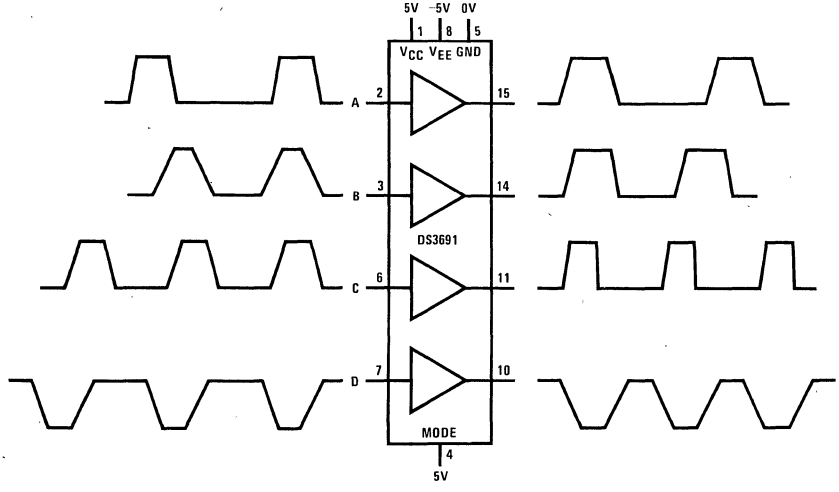


FIGURE 9. DS3691 Connected for Unbalanced Mode Operation

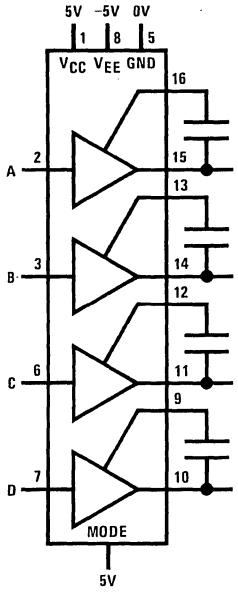


FIGURE 10. Using an External Capacitor to Control Rise Time of DS3691

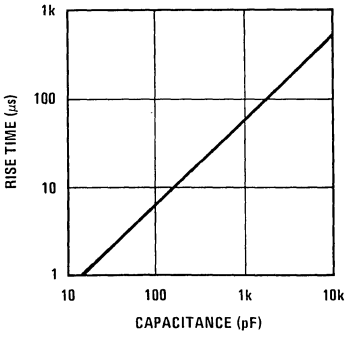


FIGURE 11. DS3691 Rise Time vs External Capacitor

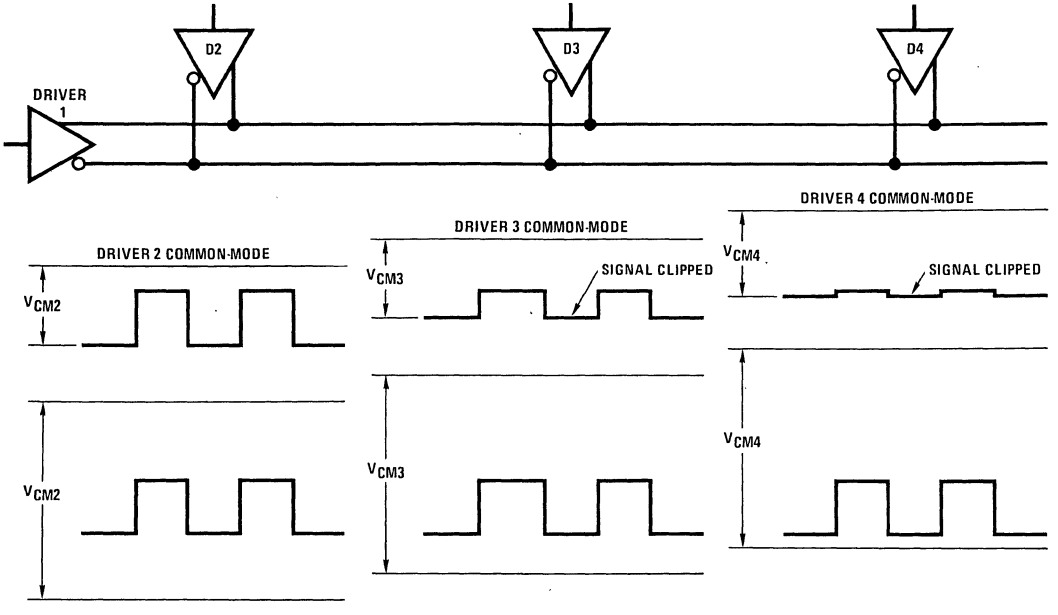


FIGURE 12. Comparison of Drivers without TRI-STATE Common-mode Output Range (Top Waveforms) to DS3691 (Bottom Waveforms)

DS78LS120/DS88LS120
The Receiver

The DS78LS120/DS88LS120 are high performance, dual differential, TTL compatible line receivers which meet or exceed the above listed requirements for both balanced and unbalanced voltage digital interface.

The line receiver will discriminate a ±200 millivolt input signal over a full common-mode range of ±10 volts and a ±300 millivolt signal over a full common-mode range of ±15 volts.

The DS78LS120/DS88LS120 include response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Switching noise which may occur on the input signal can be eliminated by the 50 mV (referred to input) of hysterisis built into the output gate *(Figure 14)*. The DS78LS120/DS88LS120 makes use of a response control pin for the addition of an external capacitor, which will not effect the line termination impedance of the interconnect cable. Noise pulse width rejection versus the value of the response control capacitor is shown in *Figure 15*. The combination of the filter followed by hysteresis will optimize performance in a worse case noise environment. The DS78C120/DS88C120 is identical in performance to the DS78LS120/DS88LS120, except it's compatible with CMOS logic gates.

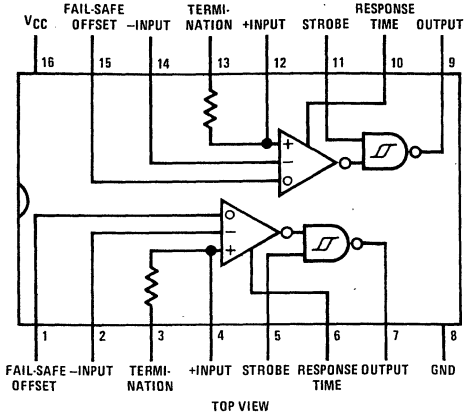


FIGURE 13. DS78LS120/DS88LS120 Dual Differential Line Receiver

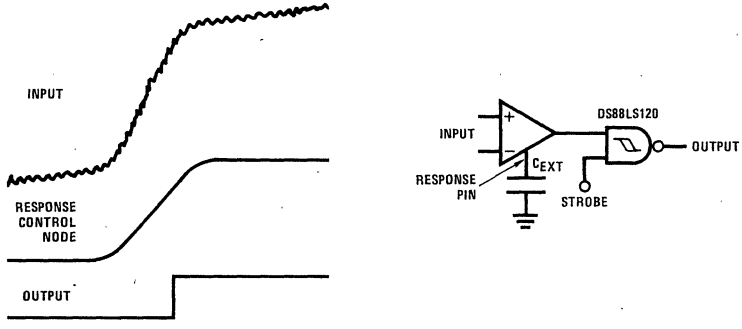


FIGURE 14. Application of DS88LS120 Receiver Response Control and Hysteresis

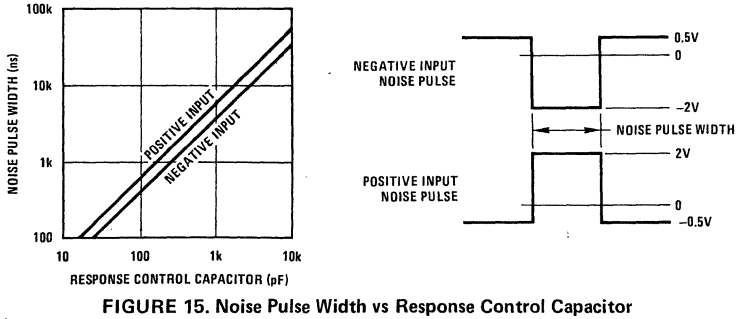


FIGURE 15. Noise Pulse Width vs Response Control Capacitor

FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the loss of signals in the transmission lines. And it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or short. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault condition exists.

The receiver input threshold is ±200 millivolts and an input signal greater than ±200 millivolts insures the receiver will be in a specific logic state. When the offset control input is connected to a V_{CC} = 5 volts, the input thresholds are offset from 200 to 700 millivolts, referred to the non-inverting input, or −200 to −700 millivolts, referred to the inverting input. Therefore, if the input is open or short, the input will remain in a specific state (See *Figure 16*).

It is recommended that the receiver be terminated in 500 Ohms or less to insure it will detect an open circuit in the presence of noise.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the offset to +5 volts, offsets the receiver threshold 0.45 volts. The output is forced to a logic zero state if the input is open or short.

For balanced operation with inputs short or open, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the short or open fault condition. The "strobe" input will disable the A and B receivers and therefore may be used to "sample" the fail-safe detector (See *Figure 17*).

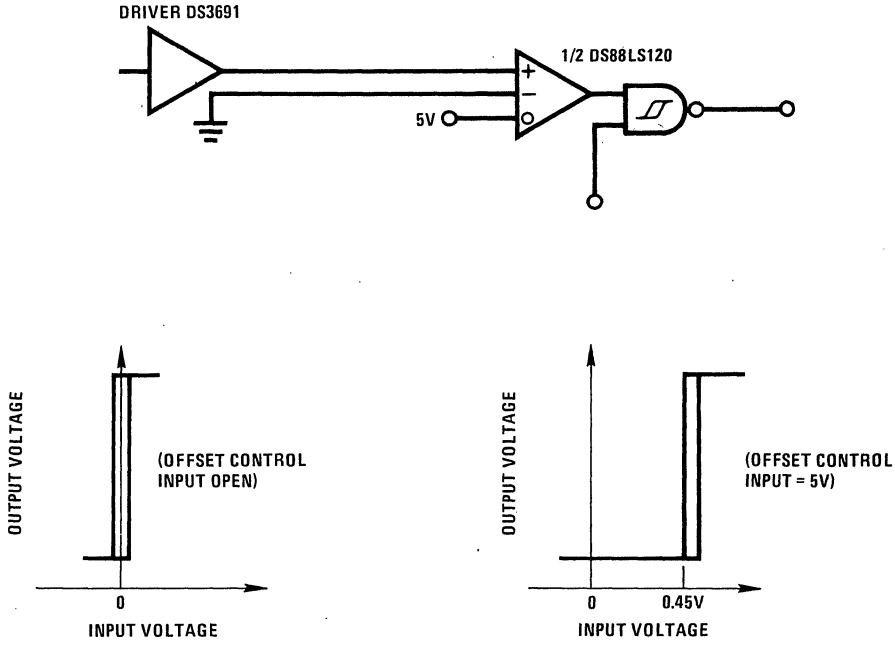


FIGURE 16. Fail-Safe Using the DS88LS120 Threshold Offset for Unbalanced Lines

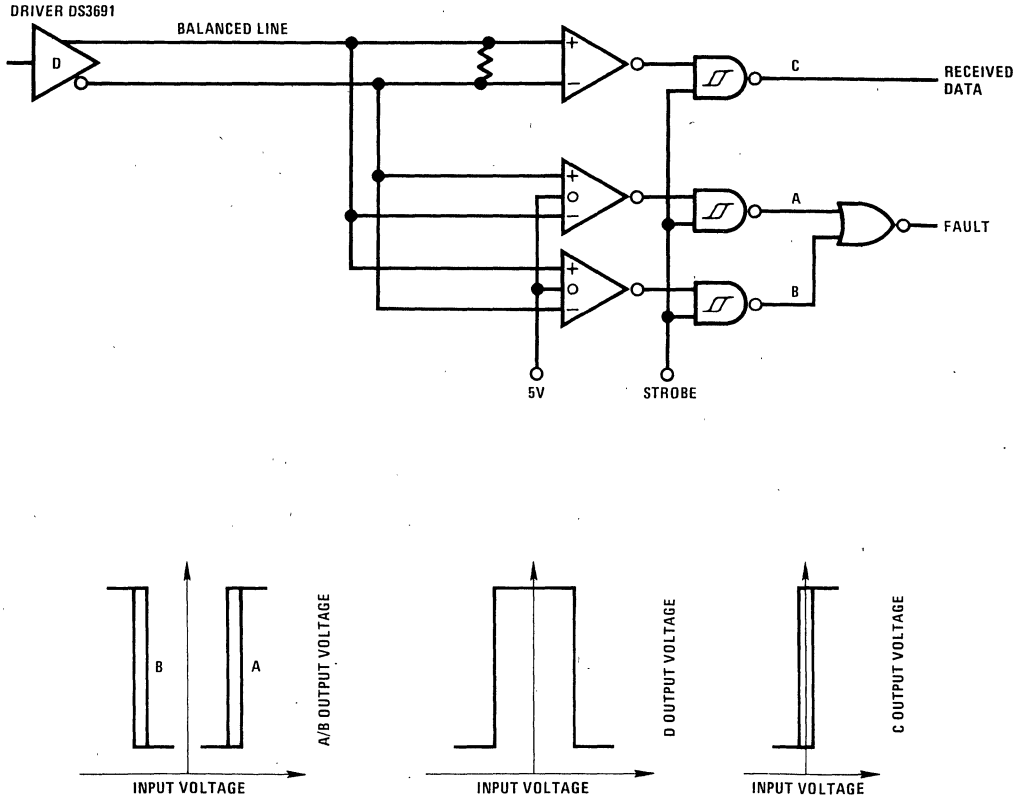


FIGURE 17. Fail-Safe Using the DS88LS120 Threshold Offset for Balanced Lines

Summary of Electrical Characteristics of Some Well Known Digital Interface Standards

National Semiconductor
Application Note 216
Don Tarver
December 1978

FORWARD

Not the least of the problems associated with the design or use of data processing equipment is the problem of providing for or, actually, interconnecting the differing types and models of equipment to form specific processing systems.

The magnitude of the problem becomes apparent when one realizes that every aspect of the electrical, mechanical and architectural format must be specified. The most common of the basic decisions confronting the engineer include:

- Type of logic (negative or positive)
- Threshold levels
- Noise immunity
- Form of transmission
  - Balanced/unbalanced, terminated/unterminated
  - Unidirectional/bidirectional, simplex/multiplexed
- Type of transmission line
- Connector type and pin out
- Bit or byte oriented
- Baud rate

If each make and/or model of equipment presented a unique interface at its I/O ports, "interface" engineering would become a major expenditure associated with the use of data processing equipment.

Fortunately, this is not the case as various interested or cognizant groups have analyzed specific recurring interface areas and recommended "official" standards around which common I/O ports could be structured. Also, the I/O specifications of some equipment with widespread popularity such as the IBM 360/370 computer and DEC minicomputer have become "defacto" standards because of the desire to provide/use equipment which interconnect to them.

Compliance with either the "official" or "defacto" standards on the part of equipment manufacturers is voluntary. However, it is obvious that much can be gained and little lost by providing equipment that offers either the "official" or "defacto" standard I/O ports.

As can be imagined, the entire subject of interface in data processing systems is complicated and confusing, particularly to those not intimately involved in the day-to-day aspects of interface engineering or management. However, at the component level the questions simplify to knowing what standards apply and what circuits or components are available to meet the standards.

This application note summarizes the important electrical characteristics of the most commonly accepted interface standards and offers recommendations on how to use National Semiconductor integrated circuits to meet those standards.

1.0 INTRODUCTION

The interface standards covered in this application note are listed in Table I. The body of the text expands upon the scope and application of each listed standard and summarizes important electrical parameters.

Table II summarizes the National Semiconductor IC's applicable to each standard.

TABLE I. COMMON LINE DRIVER/RECEIVER INTERFACE STANDARDS SUMMARY

INTERFACE AREA	APPLICATION	STANDARD	ORIGIN	COMMENTS
Data Communications Equipment (DCE*) to Data Terminal Equipment (DTE)	U.S.A. Industrial	RS232C	EIA	Unbalanced, Short Lines
		RS422	EIA	Balanced, Long Lines
		RS423	EIA	Unbalanced, RS232 Up-Grade
		RS449	EIA	System Standard Covering Use of RS422, RS423
	International	CCITT Vol. VIII V. 24	International Telephone	Similar to RS232
		CCITT No. 97 X. 26	and Telegraph Consultative	Similar to RS423
		CCITT No. 97 X. 27	Committee	Similar to RS422
	U.S.A. Military	MIL-STD-188C	D.O.D.	Unbalanced, Short Lines
		MIL-STD-188-114	D.O.D.	Similar to RS422, RS423
		MIL-STD-1397 (NTDS—Slow)	Navy	42k bits/sec
		MIL-STD-1397 (NTDS—Fast)	Navy	250k bits/sec
	U.S. Government, Non-Military	FED-STD-1020	GSA	Identical to RS423
		FED-STD-1030	GSA	Identical to RS422
Computer to Peripheral	IBM 360/370	System 360/370 Channel I/O	IBM	Unbalanced Bus
	DEC Mini-Computer	DEC Unibus®	DEC	Unbalanced Bus
Instrument to Computer	Nuclear Instrumentation	CAMAC (IEEE std. 583-1975)	NIM (AEC)	DTL/TTL Logic Levels
	Laboratory Instrumentation	488	IEEE	Unbalanced Bus
Microprocessor to Interface Devices	Microprocessor Circuits	Microbus™	National Semiconductor	Short Line; 8-Bit Parallel, Digital Transmission
Facsimile Equipment to DTE	Facsimile Transmission	RS357	EIA	Incorporates RS232
Automatic Calling Equipment to DTE	Impulse Dialing and Multi-Tone Keying	RS366	EIA	Incorporates RS232
Numerically Controlled Equipment to DTE	Numerically Controlled Equipment	RS408	EIA	Short Lines (<4 Ft.)

*Changed to "Data Circuit—Terminating Equipment"
®Registered trademark of Digital Equipment Corp.

TABLE II. LINE DRIVER/RECEIVER INTEGRATED CIRCUIT SELECTION GUIDE FOR DIGITAL INTERFACE STANDARDS

STANDARD DESIGNATION	PART NUMBER			
	LINE DRIVER		LINE RECEIVER	
	0°C TO +70°C	−55°C TO +125°C	0°C TO +70°C	−55°C TO +125°C
U.S. Industrial Standards				
RS232C	DS1488 DS75150	Not Applicable Not Applicable	DS1489 (A) DS75154	Not Applicable Not Applicable
RS357	See RS232C			
RS366	See RS232C			
RS408	DS75453 DS75454	DS55454 DS55454	DS7820A DS75115	DS7820A DS55115
RS422	DS3691 DS26LS31C DS3487	DS1691A DS26LS31M DS3587	DS88LS120 DS26LS32C DS3486 DS26LS33C DS88C20 DS88C120	DS78LS120 DS26LS32M DS26LS33M DS78C20 DS78C120
RS423	DS3691 DS3692	DS1691A DS1692	DS88LS120 DS88C20 DS88C120	DS78LS120 DS78C20 DS78C120
RS449	See RS422, RS423			
IEEE 488	DS3666 DS75160A DS75161A DS75162A		DS3666 DS75160A DS75161A DS75162A	
CAMAC	See RS232C, RS422, RS423 or IEEE 488			
IBM 360/370 I/O Port	DS75123	Not Applicable	DS75124	Not Applicable
DEC Unibus®	DS36147 DS8641 Transceiver	DS16147 DS7641 Transceiver	DS8640 DS8641 Transceiver	DS7640 DS7641 Transceiver
Microbus™	DS3628 DP8228 DP8216 DP8212 DP8304B Transceiver	DS1628 DP8228M DP8216M DP8212M	DP8304B Transceiver	
Government Standards				
MIL-STD-188C	DS3692	DS1692	DS88LS120	DS78LS120
MIL-STD-188-114	DS3692	DS1692	DS88LS120	DS78LS120
FED-STD-1020	See RS423			
FED-STD-1030	See RS422			
MIL-STD-1397 (NTDS–Slow)	Use Discrete Components and/or Comparators			
MIL-STD-1397 (NTDS–Fast)	Use Discrete Components and/or Comparators			

®Registered trademark of Digital Equipment Corp.

TABLE II. LINE DRIVER/RECEIVER INTEGRATED CIRCUIT SELECTION GUIDE FOR DIGITAL INTERFACE STANDARDS (Continued)

STANDARD DESIGNATION	PART NUMBER			
	LINE DRIVER		LINE RECEIVER	
	0°C TO +70°C	−55°C TO +125°C	0°C TO +70°C	−55°C TO +125°C
International Standards (CCITT)				
1969 White Book Vol. VIII, V. 24	See RS232C			
Circular No. 97, X. 26	See RS422			
Circular No. 97, X. 27	See RS423			

2.0 DATA TERMINAL EQUIPMENT (DTE) TO DATA COMMUNICATIONS EQUIPMENT (DCE) INTERFACE STANDARDS

2.1 Application

The DTE/DCE standards cover the electrical, mechanical and functional interface between/among terminals (i.e., teletypewriters, CRTs, etc.) and communications equipment (i.e., modems, cryptographic sets, etc.).

2.2 U.S. Industrial DTE/DCE Standards

2.2.1 EIA RS232C

The oldest and most widely known DTE/DCE standard. It provides for one-way/non-reversible, single-ended (unbalanced), non-terminated line, serial digital data transmission.

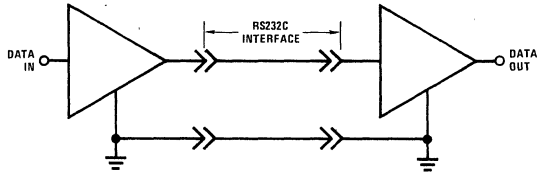


FIGURE 1. EIA RS232C Application

Important features are:

a) Positive logic (±5V min to ±15V max)
b) Fault protection
c) Slew-rate control
d) 50 feet recommended cable length and 20k bits per second data signaling rate.

2.2.2 EIA RS422, RS423

In a move to upgrade system capabilities by utilizing state-of-the-art devices and technology the EIA, in 1975, introduced 2 new specifications covering:

1) Single-ended data transmission at modulation rates up to kilobaud* (RS423)

2) Balanced data transmission at modulation rates up to 10 megabaud (RS422).

2.2.2.1 RS423

RS423 closely resembles RS232C in that it, too, specifies one-way/non-reversible, single-ended, data transmission lines. Key differences between RS423 and RS232C are:

RS423	RS232
4V to 6V Logical "1"	5V to 15V Logical "1"
−4V to −6V Logical "0"	−5V to −25V Logical "0"
100k Baud at 40 Feet	20k Baud at 50 Feet
Balanced Receiver, Referred to Driver Ground, Permitting Ground Potential Difference Between Driver and Receiver	Unbalanced Receiver

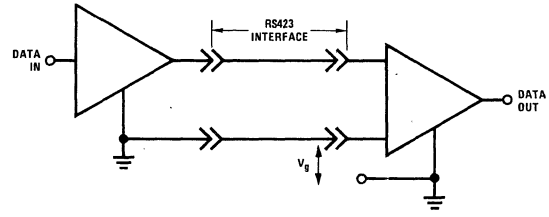


FIGURE 2. EIA RS423 Application

* Modulation rate = reciprocal of minimum pulsewidth (i.e., 20 ms pulse = 50 baud)

TABLE III. EIA RS232C SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	EIA RS232C			UNITS
			MIN	TYP	MAX	
V_{OH}	Driver Output Voltage Open				25	V
V_{OL}	Circuit		−25			V
V_{OH}	Driver Output Voltage Loaded	$3\ k\Omega \leq R_L \leq 7\ k\Omega$	5		15	V
V_{OL}	Output		−15		−5	V
R_O	Driver Output Resistance Power OFF	$-2V \leq V_O \leq 2V$			300	Ω
I_{OS}	Driver Output Short-Circuit Current		−500		500	mA
	Driver Output Slew Rate					
	All Interchange Circuits				30	V/μs
	Control Circuits		6			V/ms
	Rate and Timing Circuits		6			V/ms
		% of Unit Interval	4			%
R_{IN}	Receiver Input Resistance	$3V \leq V_{IN} \leq 25V$	3000		7000	Ω
	Receiver Open Circuit Input Bias Voltage		−2		2	V
	Receiver Input Threshold					
	Output = MARK		−3			V
	Output = SPACE				3	V

TABLE IV. EIA RS423 SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	EIA RS423			UNITS
			MIN	TYP	MAX	
V_O	Driver Unloaded Output Voltage		4		6	V
$\overline{V_O}$			−4		−6	V
V_T	Driver Loaded Output Voltage	$R_L = 450\Omega$	3.6			V
$\overline{V_T}$			−3.6			V
R_S	Driver Output Resistance				50	Ω
I_{OS}	Driver Output Short-Circuit Current	$V_O = 0V$			±150	mA
	Driver Output Rise and Fall Time	Baud Rate ≤ 1k Baud			300	μs
		Baud Rate ≥ 1k Baud			30	% Unit Interval
I_{OX}	Driver Power OFF Current	$V_O = \pm 6V$			±100	μA
V_{TH}	Receiver Sensitivity	$V_{CM} \leq \pm 7V$			±200	mV
V_{CM}	Receiver Common-Mode Range				±10	V
R_{IN}	Receiver Input Resistance		4000			Ω
	Receiver Common-Mode Input Offset				±3	V

2.2.2.2 RS422

RS422 provides for balanced data transmission with unidirectional/non-reversible, terminated or non-terminated transmission lines. Important features are:

a) ±2V to ±6V driver output
b) 0.4V differential output matching
c) ±200 mV receiver input sensitivity
d) 10M baud modulation rate

2.3 International Standards

2.3.1 CCITT 1969 White Book Vol. VIII, V. 24. This standard is identical to RS232C.

2.3.2 CCITT circular No. 97 Com SPA/13, X. 26. This standard is similar to RS422 with the exception that the receiver sensitivity at the specified maximum common-mode voltage (±7V) shall be ±300 mV vs ±200 mV for RS422.

2.3.3 CCITT circular No. 97 Com SPA/13, X. 27. This standard is similar to RS423 with 2 exceptions:

a) The receiver sensitivity is as specified in paragraph X. 26, and

b) The driver output voltage is specified at a load resistance of 3.9 kΩ.

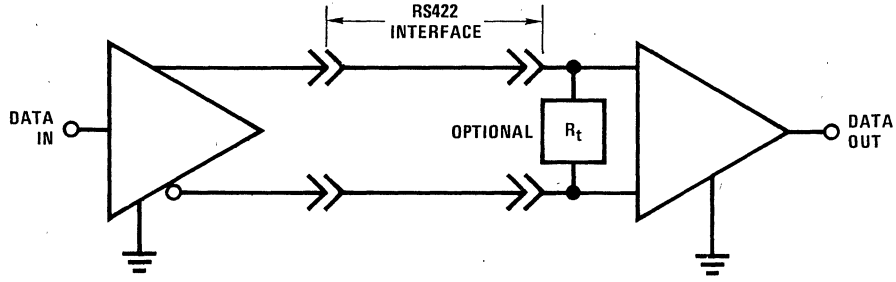


FIGURE 3. EIA RS422 Application

TABLE V. EIA RS422 SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	EIA RS422			UNITS
			MIN	TYP	MAX	
V_O	Driver Unloaded Output Voltage				6	V
$\overline{V_O}$					−6	V
V_T	Driver Loaded Output Voltage	$R_T = 100\Omega$	2			V
$\overline{V_T}$			−2			V
R_S	Driver Output Resistance	Per Output			50	Ω
I_{OS}	Driver Output Short-Circuit Current	$V_O = 0V$			150	mA
	Driver Output Rise Time				10	% Unit Interval
I_{OX}	Driver Power OFF Current	$-0.25V \leq V_O \leq 6V$			±100	μA
V_{TH}	Receiver Sensitivity	$V_{CM} = \pm 7V$			200	mV
V_{CM}	Receiver Common-Mode Voltage		−12		12	V
	Receiver Input Offset		±3			V

2.4 U.S. Military Standards

2.4.1 MIL-STD-188C (Low Level)

The military equivalent to RS232C is MIL-STD-188C. Devices intended for RS232C can be applied to MIL-STD-188C by use of external wave shaping components on the driver end and input resistance and threshold tailoring on the receiver end.

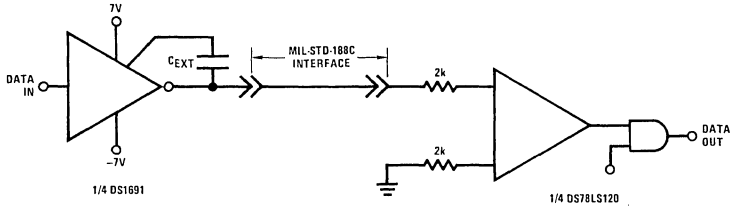


FIGURE 4. MIL-STD-188C Application

TABLE VI. MIL-STD-188C SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	MIL-STD-188C LOW LEVEL LIMITS			UNITS
			MIN	TYP	MAX	
V_{OH}	Driver Output Voltage Open Circuit	(Note 1)	5		7	V
V_{OL}			−7		−5	V
R_O	Driver Output Resistance Power ON	$I_{OUT} \leq 10$ mA			100	Ω
I_{OS}	Driver Output Short-Circuit Current		−100		100	mA
	Driver Output Slew Rate					
	All Interchange Circuits	(Note 2)	5		15	% IU
	Control Circuits					
	Rate and Timing Circuits					
R_{IN}	Receiver Input Resistance	Mod Rate ≤ 200k Baud	6			Ω
	Receiver Input Threshold					
	Output = MARK	(Note 3)			100	μA
	Output = SPACE		−100			μA

Note 1: Ripple <0.5%, V_{OH}, V_{OL} matched to within 10% of each other.

Note 2: Waveshaping required on driver output such that the signal rise or fall time is 5% to 15% of the unit interval at the applicable modulation rate.

Note 3: Balance between marking and spacing (threshold) currents actually required shall be within 10% of each other.

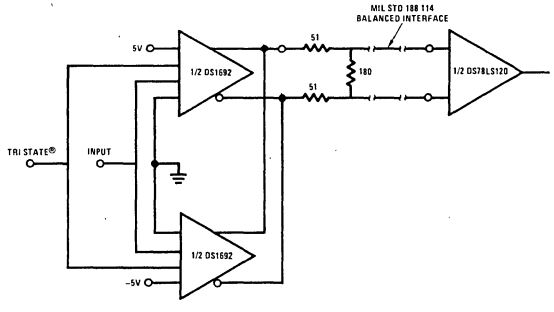


FIGURE 5. MIL-STD-188-114 (Balanced Applications)

2.4.2 MIL-STD-188-114 Balanced

This standard is similar to RS422 with the exception that the driver offset voltage level is limited to ±0.4V vs ±3V allowed in RS422.

2.4.3 MIL-STD-188-114 Unbalanced.

This standard is similar to RS423 with the exception that loaded circuit driver output voltage at R_L = 450Ω must be 90% of the open circuit output voltage vs ±2V at R_S = 100Ω for RS422.

2.4.4 MIL-STD-1397 (Slow and Fast)

2.5 U.S. Government (non-military) standards FED-STD-1020 and 1030 are identical without exception to EIA RS423 and RS422, respectively.

3.0 COMPUTER TO PERIPHERAL INTERFACE STANDARDS

To date, the only standards dealing with the interface between processors and other equipment are the "defacto" standards in the form of specifications issued by IBM and DEC covering the models 360/370 I/O ports and the Unibus®, respectively.

3.1 IBM specification GA-22-6974-0 covers the electrical characteristics, the format of information and the control sequences of the data transmitted between 360/370's and up to 10 I/O ports.

The interface is an unbalanced bus using 95Ω, terminated, coax cables. Devices connected to the bus should feature short-circuit protection, hysteresis in the receivers, and open-emitter drivers. Careful attention should be paid to line lengths and quality in order to limit cable noise to less than 400 mV.

TABLE VII. MIL-STD-1397 SPECIFICATION SUMMARY

	PARAMETER	CONDITIONS	COMPARISON LIMITS (MIL-STD) 1397 (SLOW)	COMPARISON LIMITS (MIL-STD) 1397 (FAST)	UNITS
	Data Transmission Rate		42	250	k Bits/Sec
V_{OH}	Driver Output Voltage		±1.5	0	V
V_{OL}			−10 to −15.5	−3	V
I_{OH}	Driver Output Current		≥−4		mA
I_{OL}			1		mA
R_S	Driver Power OFF Impedance		≥100		kΩ
V_{IH}	Receiver Input Voltage	Fail-Safe Open Circuit	≤4.5	≤−1.1	V
V_{IL}			≥−7.5	≥−1.9	V

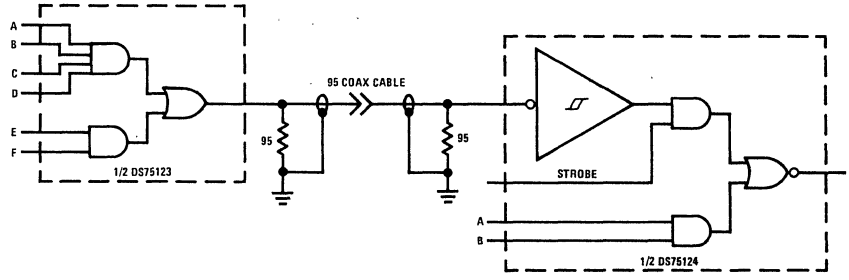


FIGURE 6. IBM 360/370 I/O Application

®Registered trademark of Digital Equipment Corp.

TABLE VIII. IBM 360/370 SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	IBM 360/370			UNITS
			MIN	TYP	MAX	
V_{OH}	Driver Output Voltage	I_{OH} = 123 mA			7	V
V_{OH}		I_{OH} = 30 μA			5.85	V
V_{OH}		I_{OH} = 59.3 mA	3.11			V
V_{OL}		I_{OL} = −240 μA			0.15	V
V_{IH}	Receiver Input Threshold				1.7	V
V_{IL}	Voltage		0.7			V
I_{IH}	Receiver Input Current	V_{IN} = 3.11V			−0.42	mA
I_{IL}		V_{IN} = 0.15V	0.24			mA
	Receiver Input Voltage Range					
V_{IN}	Power ON		−0.15		7	V
V_{IN}	Power OFF		−0.15		6	V
R_{IN}	Receiver Input Impedance	$0.15V \leq V_{IN} \leq 3.9V$	7400			Ω
I_{IN}	Receiver Input Current	V_{IN} = 0.15V			240	μA
Z_O	CABLE Impedance		83		101	Ω
R_O	CABLE Termination	$P_D \geq$ 390 mW	90		100	Ω
	Line Length (Specified as Noise on Signal and Ground Lines)				400	mV

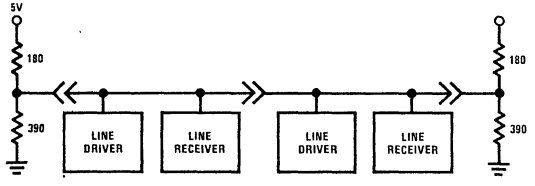


FIGURE 7. DEC Unibus® Application

TABLE IX. DEC UNIBUS ® SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	DEC UNIBUS®			UNITS
			MIN	TYP	MAX	
V_{OL}	Driver Output Voltage	I_{OL} = 50 mA			0.7	V
V_O		Absolute Maximum			7	V
V_{IH}	Receiver Input Voltage		1.7			V
V_{IL}					1.3	V
I_{IH}	Receiver Input Current	V_{IN} = 4V			100	μA
I_{IL}		V_{IN} = 4V Power OFF			100	μA

3.2 DEC Unibus®

Another example of an unofficial industry standard is the interface to a number of DEC minicomputers. This interface, configured as a 120Ω double-terminated data bus is given the name Unibus®. Devices connected to the bus should feature hysteresis in the receivers and open-collector driver outputs. Cable noise should be held to less than 600 mV.

®Registered trademark of Digital Equipment Corp.

4.0 INSTRUMENTATION TO COMPUTER INTERFACE STANDARDS

4.1 Introduction

The problem of linking instrumentation to processors to handle real-time test and measurement problems was largely a custom interface problem. Each combination of instruments demanded unique interfaces, thus inhibiting the wide spread usage of small processors to day-to-day test, measurement and control applications.

Two groups addressed the problem for specific environments. The results are:

a) IEEE 488 bus standard based upon proposals made by HP, and

b) The CAMAC system pioneered by the nuclear physics community.

4.2 IEEE 488

IEEE 488 covers the functional, mechanical and electrical interface between laboratory instrumentation (i.e., signal generators, DPM's, counters, etc.) and processors such as programmable calculators and minicomputers. Equipment with IEEE 488 I/O ports can be readily daisy chained in any combination of up to 15 equipments (including processor) spanning distances of up to 60 feet. 16 lines (3 handshake, 5 control and 8 data lines) are required.

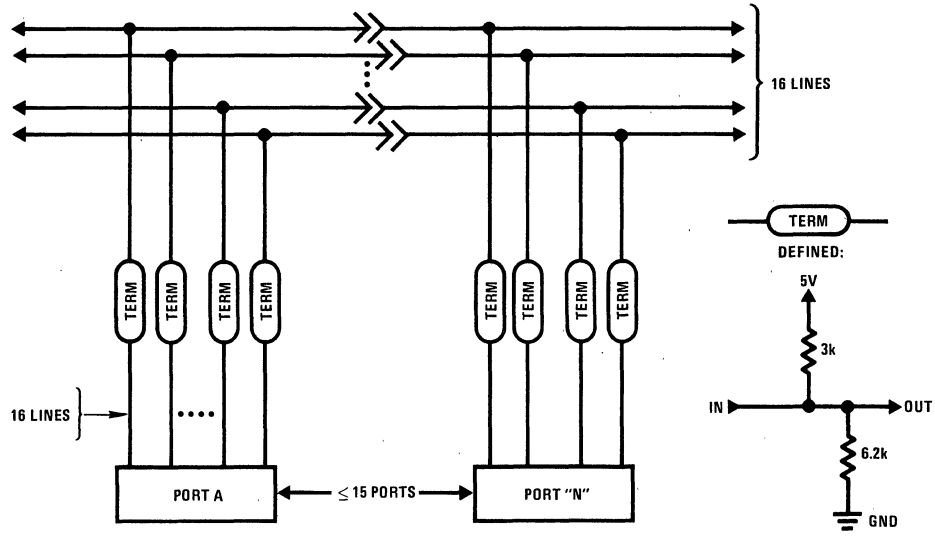


FIGURE 8. IEEE 488 Application

TABLE X. IEEE 488 SPECIFICATION SUMMARY

PARAMETER		CONDITIONS	IEEE 488			UNITS
			MIN	TYP	MAX	
V_{OH}	Driver Output Voltage	I_{OH} = –5.2 mA	2.4			V
V_{OL}		I_{OL} = 48 mA			0.4	V
	Driver Output Current					
I_{OZ}	TRI-STATE®	V_O = 2.4V			±40	μA
I_{OH}	Open Collector	V_O = 5.25V			250	μA
V_{IH}	Receiver Input Voltage	0.4V Hysteresis Recommended	2.0			V
V_{IL}					0.8	V
I_{IH}	Receiver Input Current	V_{IN} = 2.4V			40	μA
I_{IL}		V_{IN} = 0.4V			–1.6	mA
	Receiver Clamp Current	V_{IN} = –1.5V			12	mA
R_{L1}	Termination Resistor	V_{CC} = 5V (±5%)	2850		3150	
R_{L2}		V = Gnd	5890		6510	

4.3 CAMAC

The CAMAC system is the result of efforts by those in the nuclear physics community to standardize the interface between laboratory instruments and computers before the introduction of IEEE 488.

It allows either serial or parallel interconnection of instruments via a "crate" controller.

The electrical requirements of the interfaces are compatible with DTL and TTL logic levels.

5.0 MICROPROCESSOR SYSTEMS INTERFACE STANDARDS

5.1 Microprocessor systems are bus organized systems with two types of bus requirements:

a) Minimal system: for data transfer over short distances (usually on 1 PC board), and,

b) Expanded system: for data transfer to extend the memory or computational capabilities of the system.

5.2 Minimal Systems and Microbus™

Microbus™ considers the interface between MOS/LSI microprocessors and interfacing devices in close physical proximity which communicate over 8-bit parallel unified bus systems. It specifies both the functional and electrical characteristics of the interface and is modeled after the 8060, 8080 and 8900 families of microprocessors as shown in *Figures 8, 9 and 10*.

The electrical characteristics of Microbus are shown in Table XI.

TABLE XI. MICROBUS ELECTRICAL SPECIFICATION SUMMARY

PARAMETER		DRIVER	RECEIVER		UNITS
			STANDARD	HYSTERESIS (RECOMMENDED)	
V_{OL}	Output Voltage (At 1.6 mA)	$\leq$0.4V			
V_{OH}	(At −100 μA)	$\geq$2.4V			
V_{IL}	Input Voltage		0.8	0.6	V
V_{IH}			2.0	2.0	V
	Internal Capacitive Load at 25°C	15	10	10	pF
t_r	Rise Time (Maximum)	100			ns
t_f	Fall Time (Maximum)	100			ns

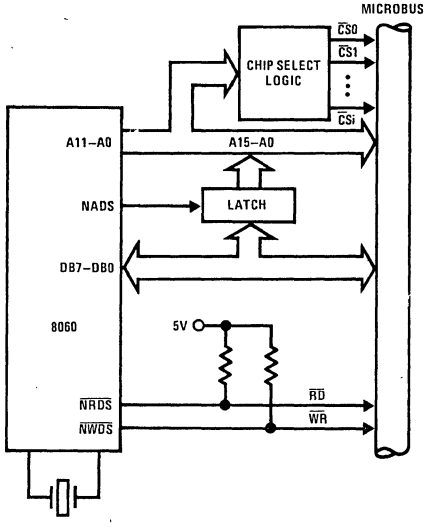


FIGURE 9. 8060 SC/MP II System Model

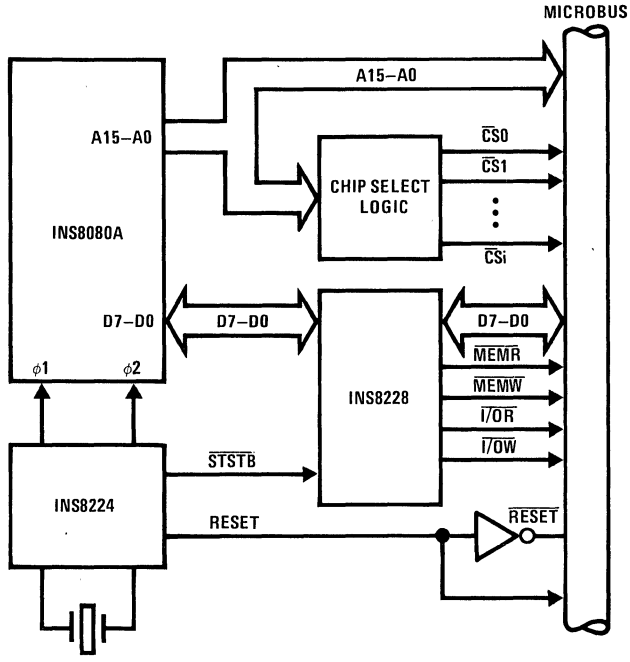


FIGURE 10. 8080 System Model for the Basic Microbus Interface

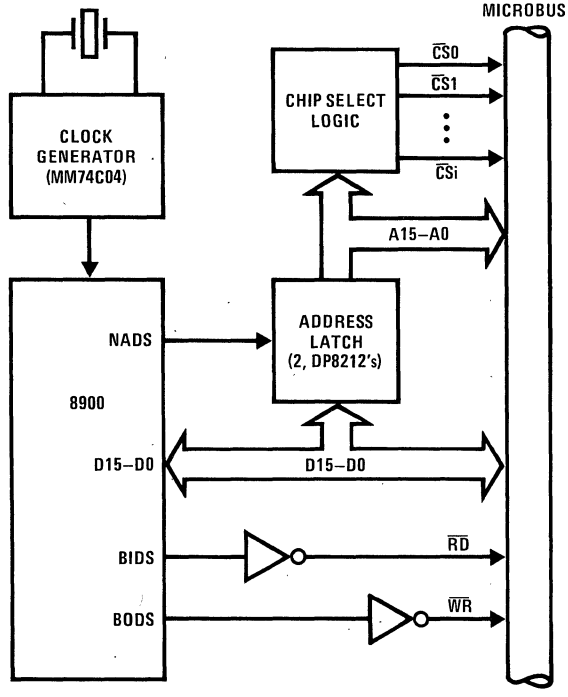


FIGURE 11. 8900 System Model

5.3 Expanded Microprocessor System Interfaces

Since the outputs of most microprocessor devices are limited to a loading of one relative to a TTL load, expanded systems will require buffers on both their address and data lines.

To date, no formal standards exist which govern this interface. However, "defacto" standards are emerging in the form of the specifications for "recommended devices" which are mentioned in the data sheets and application notes for the widely sourced microprocessor devices. Here, the answer to the question of how to provide a "standard" interface is simplified to that of proper usage of recommended devices.

Table XII summarizes the important electrical characteristics of recommended bus drivers for expanded microprocessor systems.

6.0 OTHER INTERFACE STANDARDS

Some other commonly occurring interfaces which have become standardized are:

a) Interface between facsimile terminals and voice frequency communications terminals,

b) Interface between terminals and automatic calling equipment used for data communications, and

c) Interface between numerically controlled equipment and data terminals.

6.1 EIA RS357

RS357 defines the electrical, functional and mechanical characteristics of the interface between analog facsimile equipment to be used for telephone data transmission and the data sets used for controlling/transmitting the data.

Figure 11 summarizes the functional and electrical characteristics of RS357.

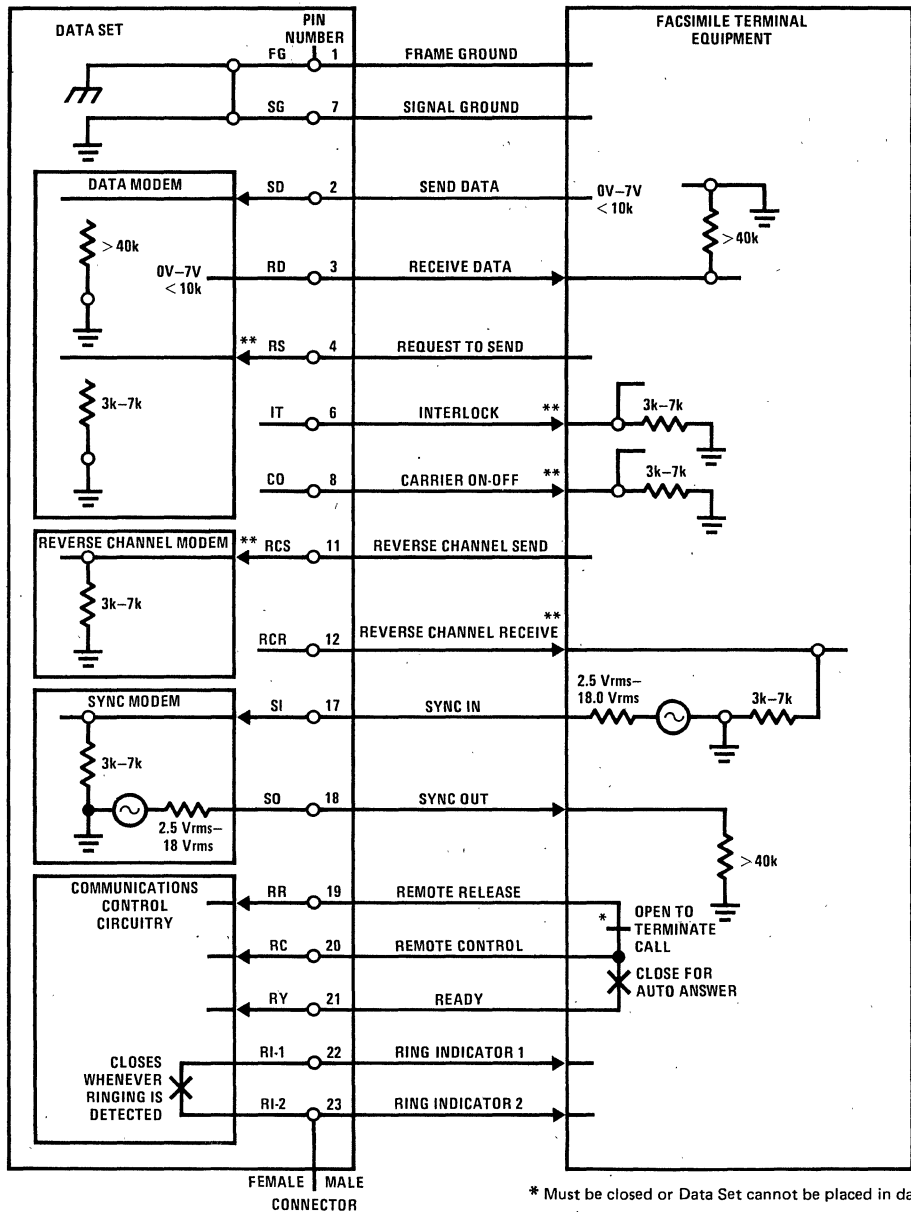
6.2 EIA RS366

RS366 defines the electrical, functional and mechanical characteristics of the interface between automatic calling equipment for data communications and data terminal equipment.

The electrical characteristics are encompassed by RS232C.

TABLE XII. RECOMMENDED SPECIFICATION OF BUS DRIVERS FOR EXPANDED MICROPROCESSOR SYSTEMS

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Driver Input Voltage		2			V
V_{IL}					0.8	V
V_{OH}	Driver Output Voltage	$I_{OH} = -10$ mA	2.4			V
V_{OL}		$I_{OL} = 48$ mA			0.5	V
I_{OS}	Short-Circuit Current	$V_{CC} = 5.25V$			−150	mA
C_L	Bus Drive Capability		300			pF



* Must be closed or Data Set cannot be placed in data mode

** Receive	Sensitivity	Source
ON	3V–25V	5V–25V
OFF	3V–25V	5V–25V

FIGURE 12. Functional and Electrical Characteristics of RS357

6.3 EIA RS408

RS408 recommends the standardization of the 2 interfaces shown in *Figure 13*.

The electrical characteristics of NCE to DTE interface are, in summary, those of conventional TTL drivers (series 7400) with:

$V_{OL} \leq 0.4V$ at $I_{OL} = 48$ mA
$V_{OH} \geq 2.4V$ at $I_{OH} \leq -1.2$ mA, and
$C_L \leq 2000$ pF.

Short circuit protection should be provided.

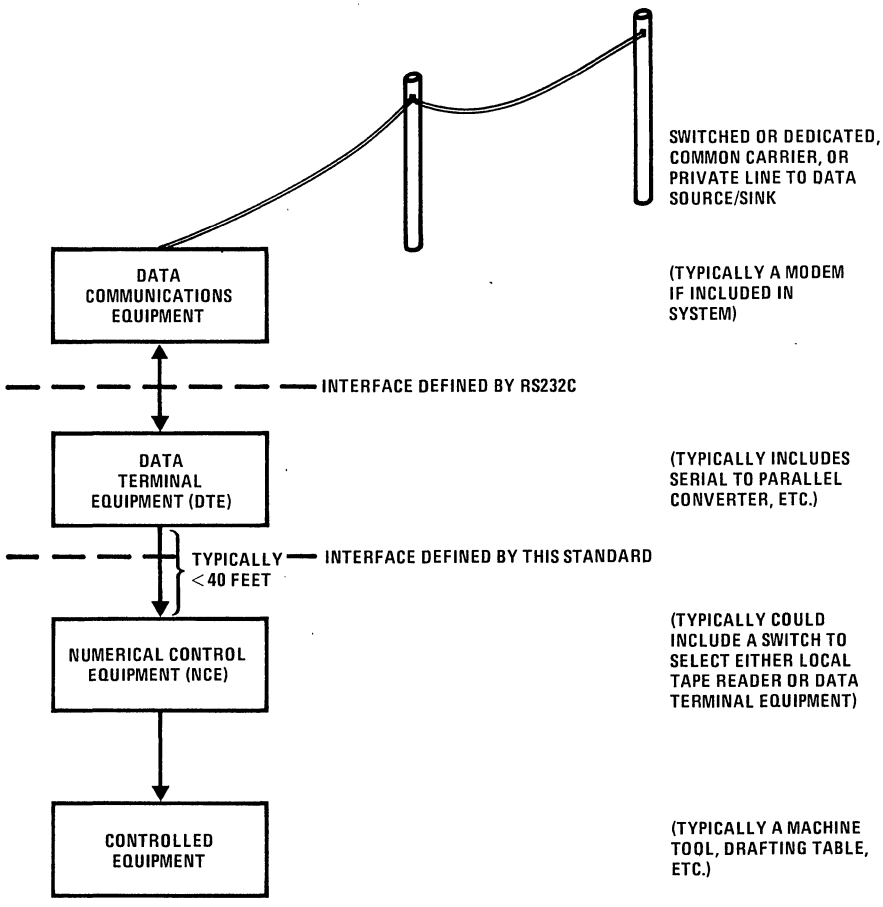


FIGURE 13. EIA RS408 Interface Applications

Section 2
Bus Transceivers

2

TEMPERATURE RANGE		DESCRIPTION	PAGE NUMBER
−55 °C to +125 °C	0 °C to +70 °C		
*DP7303	DP8303	8-Bit TRI-STATE Bidirectional Transceivers	2-5, 2-6
*DP7304B	DP8304B	8-Bit TRI-STATE Bidirectional Transceivers	2-5, 2-11
*DP7307	DP8307	8-Bit TRI-STATE Bidirectional Transceivers	2-5, 2-16
*DP7308	DP8308	8-Bit TRI-STATE Bidirectional Transceivers	2-5, 2-20
*DS26S10M	DS26S10	Quad Bus Transceiver	2-24
*DS26S11M	DS26S11	Quad Bus Transceiver	2-24
—	DS3662	Quad High Speed Trapezoidal Bus Transceiver	2-29
—	AN-259	DS3662—The Bus Optimizer	2-33
—	AN-337	Reducing Noise on Microcomputer Buses	2-40
—	DS3666	IEEE-488 GPIB Transceiver	2-48
—	DS3667	TRI-STATE Bidirectional Transceiver	2-56
—	DS75160A	IEEE-488 GPIB Transceiver	2-61
—	DS75161A	IEEE-488 GPIB Transceiver	2-61
—	DS75162A	IEEE-488 GPIB Transceiver	2-61
*DS7640	DS8640	Quad NOR Unified Bus Receiver	2-68
*DS7641	DS8641	Quad Unified Bus Transceiver	2-70
—	DS8642	Quad Transceiver	2-72
*DS7833	DS8833	Quad TRI-STATE Bus Transceiver	2-75
*DS7834	DS8834	Quad TRI-STATE Bus Transceiver	2-79
*DS7835	DS8835	Quad TRI-STATE Bus Transceiver	2-75
*DS7836	DS8836	Quad NOR Unified Bus Transceiver	2-83
*DS7837	DS8837	Hex Unified Bus Receiver	2-85
*DS7838	DS8838	Quad Unified Bus Transceiver	2-87
*DS7839	DS8839	Quad TRI-STATE Bus Transceiver	2-79
DS8T26AM	DS8T26A	4-Bit Bidirectional Bus Transceiver	2-89
*DS8T28M	DS8T28	4-Bit Bidirectional Bus Transceiver	2-89
DM54S240	DM74S240	Octal TRI-STATE Line Driver/Receiver	LOGIC
DM54S241	DM74S241	Octal TRI-STATE Line Driver/Receiver	LOGIC

*Also available screened in accordance with MIL-STD-883 Class B. Refer to National Semiconductor's "The Reliability Handbook".

BUS CIRCUITS

Data bus circuits are not transmission line circuits in the normal interpretation where the transmission line is electrically long (1/4 wave length) with respect to the baud rate. Like unbalanced transmission lines, the data transmission is susceptible to common-mode noise, such as ground IR noise and induced reactive noise from crosstalk. A bus is a communications method where many elements of a system time share the same signal (address or data) bus. A bus shouldn't extend out of its subsystem's electronic enclosure without special care. Line length in excess of 10 feet is not recommended without slew rate control. Cables should be in the form of twisted pair or flat cable where a signal wire is alternated with a ground wire.

OPEN-COLLECTOR BUS CIRCUITS

Bus Driver		Bus Receiver				Driver/ Receiver/ Transceiver	Circuits/ Package	Device Number		Comments	Page No.
Propagation Delay (ns)	V_{IL} (V)/ I_{OL} (mA)	Propagation Delay (ns)	V_{IL} (V)/ I_{IL} (μA)	V_{IH} (V)/ I_{IH} (μA)	Hysteresis (V)			Commercial 0°C to +70°C	Military −55°C to +125°C		
		23	1.2/−50	1.8/50		Receiver	4	DS8640	DS7640	Quad NOR receiver	2-68
		20	1.05/−50	2.65/50	1	Receiver	4	DS8836	DS7836	Quad NOR receiver	2-83
		20	1.05/−50	2.65/50	1	Receiver	6	DS8837	DS7837		2-85
30	0.9/100	40	1.50/400	1.9/100		Transceiver	4	DS3662		Trapezoidal transceiver	2-29
30	0.7/50	30	1.2/−100	1.8/100		Transceiver	4	DS8641	DS7641		2-70
20	0.7/50	17	1.05/−100	2.65/100	1	Transceiver	4	DS8642			2-72
20	0.8/100	20	1.3/−40	3.1/450		Transceiver	4	DS8838	DS7838	50Ω coax. driver	2-87
10	0.8/100	10	1.75/−100	2.25/100		Transceiver	4	DS26S10	DS26S10M		2-24
10	0.8/100	10	1.75/−100	2.25/100		Transceiver	4	DS26S11	DS26S11M	Input to bus is non-inverting	2-24
8	0.5/50	7	0.8/−500	2/100		Transceiver	4	DS36147	DS16147	Quad bidirectional I/O register	6-35
8	0.5/50	7	0.8/−500	2/100		Transceiver	4	DS36177	DS16177	Quad bidirectional I/O register	6-35
20	0.7/300					Driver	2	DS75450	DS55450	AND separate output transistors	3-51
18	0.7/300					Driver	2	DS75451	DS55451	AND	3-51
26	0.7/300					Driver	2	DS75452	DS55452	NAND	3-51
18	0.7/300					Driver	2	DS75453	DS55453	OR	3-51
27	0.7/300					Driver	2	DS75454	DS55454	NOR	3-51
		30	0.95/50	2/50	0.65	Receiver	1	DM8131	DM7131	6 bit bus comparator	LOGIC
		30	0.95/50	2/50	0.65	Receiver	1	DM8136	DM7136	6 bit bus comparator	LOGIC

TRI-STATE® BUS CIRCUITS

Bus Driver			Bus Receiver				Driver/ Receiver/ Transceiver	Circuits/ Package	Device Number		Comments	Page No.
Propagation Delay Typ (ns)	V_{OL} (V)/ I_{OL} (mA)	V_{OH} (V)/ I_{OH} (mA)	Propagation Delay Typ (ns)	V_{IL} (V)/ I_{IL} (μA)	V_{IH} (V)/ I_{IH} (μA)	Hysteresis (mV)			Commercial 0°C to +70°C	Military −55°C to +125°C		
14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Transceiver	4	DS8833	DS7833	Non-inverting TRI-STATE receiver	2-75
14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Transceiver	4	DS8835	DS7835	Inverting TRI-STATE receiver	2-75
14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Transceiver	4	DS8834	DS7834	Inverting	2-79
14	0.5/50	2.4/−10	20	0.8/−40	2/80	400	Transceiver	4	DS8839	DS7839	Non-inverting	2-79
14	0.5/48	2.4/−10	14	0.85/−200	2/20		Transceiver	4	DS8T26A	DS8T26AM	Inverting	2-89
17	0.5/48	2.4/−10	17	0.85/−200	2/20		Transceiver	4	DS8T28	DS8T28M	Non-inverting	2-89
20	0.6/55	3.6/−1	15	0.95/−250	2/10		Transceiver	4	DP8216	DP8216M	8080 MPU non-inverting	8-11
16	0.6/50	3.6/−1	15	0.95/−250	2/10		Transceiver	4	DP8226	DP8226M	8080 MPU inverting	8-11
4.5	0.55/64	2.4/−3	4.5	0.8/−400	2/50	400	Transceiver	4 or 8	DM74S240	DM54S240	Non-Inverting	LOGIC
6	0.55/64	2.4/−3	6	0.8/−400	2/50	400	Transceiver	4 or 8	DM74S241	DM54S241	Inverting	LOGIC
4.5	0.55/64	2.4/−3	4.5	0.8/−400	2/50	400	Transceiver	8	DM74S940	DM54S940	Non-Inverting	LOGIC
6	0.55/64	2.4/−3	6	0.8/−400	2/50	400	Transceiver	8	DM74S941	DM54S941	Inverting	LOGIC
8	0.5/50	2.4/−5	7	0.8/−500	2/100		Transceiver	4	DS3647	DS1647	Quad bidirectional I/O register	6-35
8	0.5/50	2.4/−5	7	0.8/−500	2/100		Transceiver	4	DS3677	DS1677	Quad bidirectional I/O register	6-35
10	0.5/50	3.6/−5	15	0.8/−250	2/80		Transceiver	8	DP8304B	DP7304B	Bidirectional non-inverting IEEE 488	2-5, 2-11
10	0.5/50	3.6/−5	10	0.8/−250	2/80		Transceiver	8	DP8303	DP7303	Bidirectional inverting	2-5, 2-6
10	0.5/50	3.6/−5	10	0.8/−250	2/80		Transceiver	8	DP8307	DP7307	Bidirectional inverting	2-5, 2-16
11	0.5/50	3.6/−5	15	0.8/−250	2/80		Transceiver	8	DP8308	DP7308	Bidirectional non-inverting	2-5, 2-20
20	0.45/15	3.6/−1					Driver	8	DP8212	DP8212M	8080 MPU data latch and service request f/f	8-4
30	0.45/10	2.4/−1	20	0.8/−250	2/20		Transceiver	8	DP8228	DP8228M	8080 MPU system bus controller and bus driver	8-22
30	0.45/10	2.4/−1	20	0.8/−250	2/20		Transceiver	8	DP8238	DP8238M	8080 MPU system bus controller and bus driver	8-22
20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	Transceiver	8	DS3666		IEEE 488 GPIB	2-48
20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	Transceiver	8	DS3667			2-56
20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	Transceiver	8	DS75160A		IEEE 488 GPIB	2-61
20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	Transceiver	8	DS75161A		IEEE 488 GPIB	2-61
20	0.5/48	2.5/−5.2	20	0.8/−100	2/20	400	Transceiver	8	DS75162A		IEEE 488 GPIB	2-61

Note. Unless otherwise specified, bus circuits listed above are TTL compatible and use 5V supplies.

National Semiconductor

8-Bit TRI-STATE® Bidirectional Transceivers

DP7303/DP8303 (Inverting) with Transmit/$\overline{\text{Receive}}$ and Chip Disable Control Inputs
DP7304B/DP8304B (Non-Inverting) with Transmit/$\overline{\text{Receive}}$ and Chip Disable Control Inputs
DP7307/DP8307 (Inverting) with $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ Control Inputs
DP7308/DP8308 (Non-Inverting) with $\overline{\text{Transmit}}$ and $\overline{\text{Receive}}$ Control Inputs

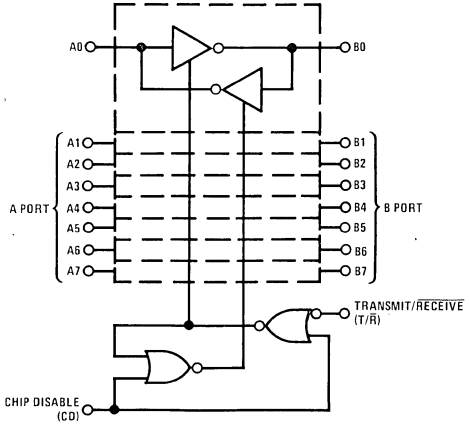
General Description

This family of 8 high speed Schottky 8-bit TRI-STATE bidirectional transceivers are designed to provide bi-directional drive for bus oriented microprocessor and digital communications systems. They are all capable of sinking 16 mA on the A ports and 48 mA on the B ports (bus ports). PNP inputs for low input current and an increased output high (V_{OH}) level allow compatibility with MOS, CMOS, and other technologies that have a higher threshold and less drive capabilities. In addition, they all feature glitch-free power up/down on the B port preventing erroneous glitches on the system bus in power up or down.

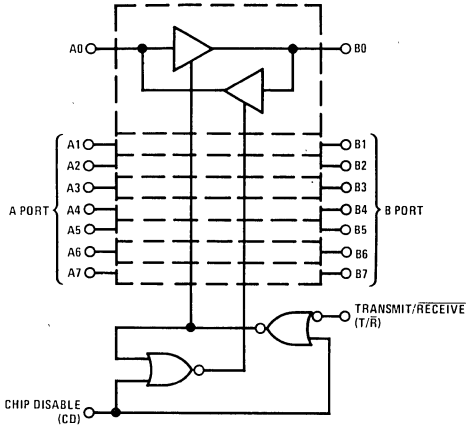
DP7303/DP8303 and DP7304B/DP8304B are featured with Transmit/Receive (T/$\overline{\text{R}}$) and Chip Disable (CD) inputs to simplify control logic. For greater design flexibility, DP7307/DP8307 and DP7308/DP8308 are featured with $\overline{\text{Transmit}}$ ($\overline{\text{T}}$) and $\overline{\text{Receive}}$ ($\overline{\text{R}}$) control inputs.

Logic Diagrams

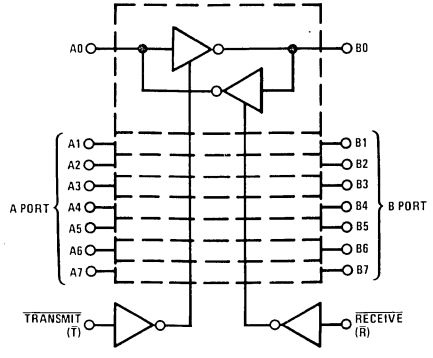
DP7303/DP8303



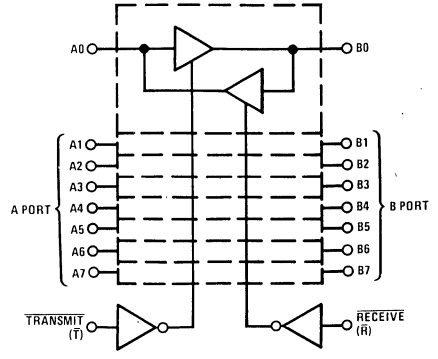
DP7304B/DP8304B



DP7307/DP8307



DP7308/DP8308



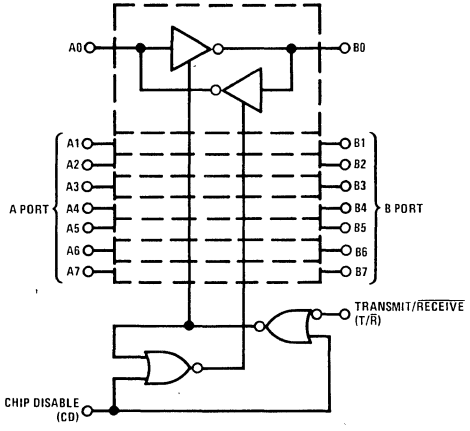
National Semiconductor

DP7303/DP8303 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

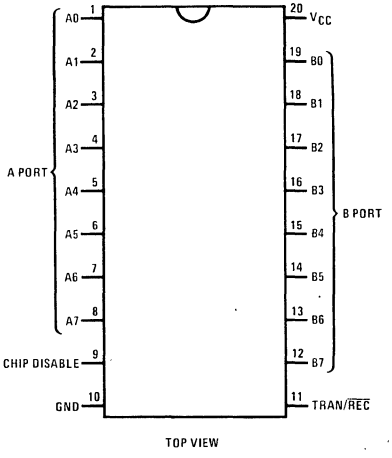
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DP7303J, DP8303J, or DP8303N
See NS Package J20A or N20A

Logic Table

INPUTS		RESULTING CONDITIONS	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 10 seconds)	300°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7303	4.5	5.5	V
DP8303	4.75	5.25	V
Temperature (T_A)			
DP7303	−55	125	°C
DP8303	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
A Port (A0-A7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	DP8303			0.8	V
			DP7303			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = T/$\overline{R}$ = V_{IL}	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = T/$\overline{R}$ = V_{IL}	I_{OL} = 16 mA (8303)		0.35	0.5	V
			I_{OL} = 8 mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_O = 0V, V_{CC} = max, Note 4		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B Port (B0-B7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	DP8303			0.8	V
			DP7303			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = max, Note 4		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA

DC Electrical Characteristics (cont'd.) (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
Control Inputs CD, T/$\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8303			0.8	V
			DP7303			0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	T/$\overline{R}$		−0.1	−0.25	mA
			CD		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
Power Supply Current							
I_{CC}	Power Supply Current	CD = 2.0V = V_{IN}, V_{CC} = max			70	100	mA
		CD = 0.4V, V_{INA} = T/$\overline{R}$ = 2V, V_{CC} = max			100	150	mA

AC Electrical Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, T/$\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 1, R5 = 1k, C4 = 15 pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 2.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 1, R5 = 1k, C4 = 30 pF		20	30	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 0.4V, T/$\overline{R}$ = 0.4V (figure C) S3 = 0, R5 = 5k, C4 = 30 pF		19	30	ns
B Port Data/Mode Specifications						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (figure A) R1 = 100 Ω, R2 = 1k, C1 = 300 pF R1 = 667 Ω, R2 = 5k, C1 = 45 pF		12 7	18 12	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, T/$\overline{R}$ = 2.4V (figure A) R1 = 100 Ω, R2 = 1k, C1 = 300 pF R1 = 667 Ω, R2 = 5k, C1 = 45 pF		15 9	20 14	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 2.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 1, R5 = 100 Ω, C4 = 300 pF S3 = 1, R5 = 667 Ω, C4 = 45 pF		25 16	35 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 0.4V, T/$\overline{R}$ = 2.4V (figure C) S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		22 14	35 25	ns ns

AC Electrical Characteristics (cont'd.) V_{CC} = 5 V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
Transmit/Receive Mode Specifications						
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0," T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S1 = 1, R4 = 100 Ω, C3 = 5 pF S2 = 1, R3 = 1k, C2 = 30 pF		23	35	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1," T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S1 = 0, R4 = 100 Ω, C3 = 5 pF S2 = 0, R3 = 5k, C2 = 30 pF		22	35	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0," T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S1 = 1, R4 = 100 Ω, C3 = 300 pF S2 = 1, R3 = 300 Ω, C2 = 5 pF		26	35	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1," T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S1 = 0, R4 = 1k, C3 = 300 pF S2 = 0, R3 = 300 Ω, C2 = 5 pF		27	35	ns

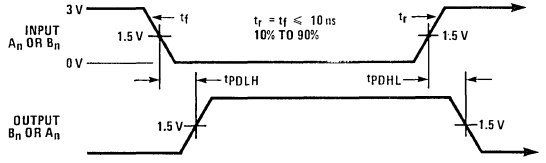
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

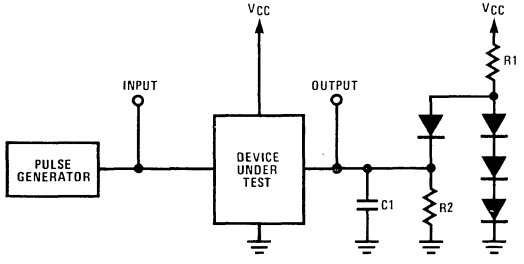
Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5 V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits





NOTE: C1 INCLUDES TEST FIXTURE CAPACITANCE.

FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

Switching Time Waveforms and AC Test Circuits (cont'd.)

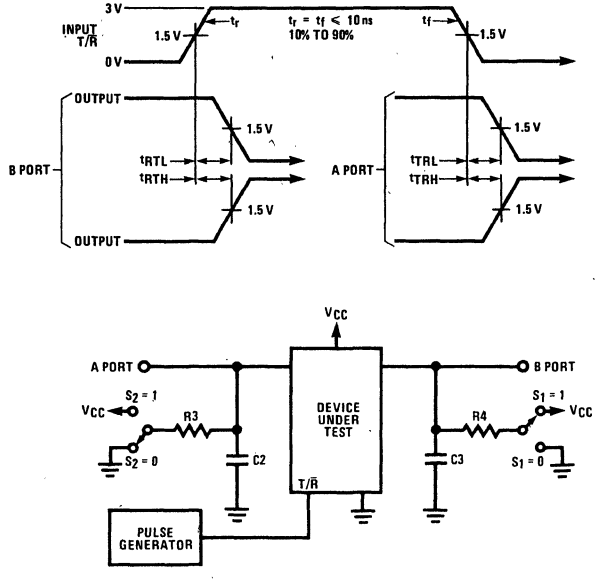


FIGURE B. Propagation Delay from T/$\overline{R}$ to A Port or B Port

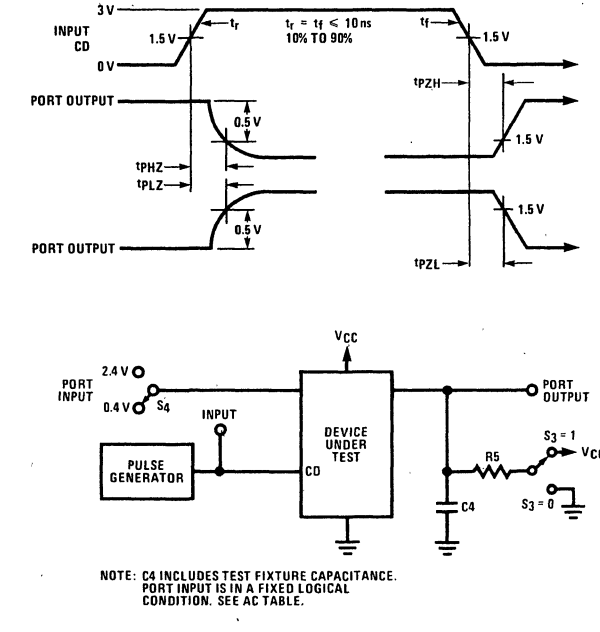


FIGURE C. Propagation Delay to/from TRI-STATE® from CD to A Port or B Port

National Semiconductor

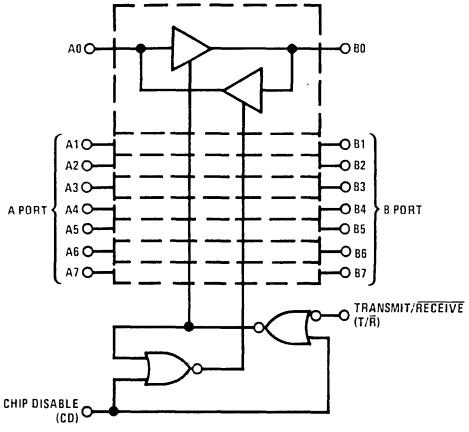
DP7304B/DP8304B

DP7304B/DP8304B 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

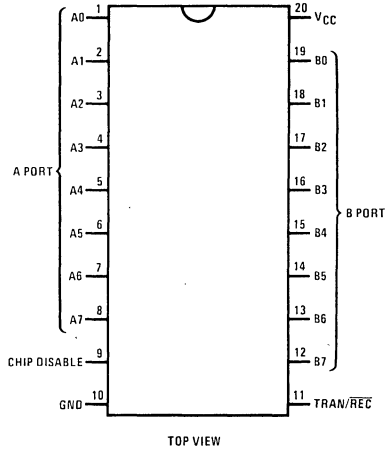
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Transmit/$\overline{\text{Receive}}$ and chip disable simplify control logic
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DP7304BJ, DP8304BJ, or DP8304BN
See NS Package J20A or N20A

Logic Table

INPUTS		RESULTING CONDITIONS	
Chip Disable	Transmit/$\overline{\text{Receive}}$	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X = Don't care

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 10 seconds)	300°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7304B	4.5	5.5	V
DP8304B	4.75	5.25	V
Temperature (T_A)			
DP7304B	−55	125	°C
DP8304B	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
A Port (A0–A7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	CD = T/$\overline{R}$ = V_{IL}	I_{OL} = 16 mA (8304B)		0.35	0.5	V
			I_{OL} = 8 mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_O = 0V, V_{CC} = max, Note 4		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B Port (B0–B7)							
V_{IH}	Logical "1" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}		2.0			V
V_{IL}	Logical "0" Input Voltage	CD = V_{IL}, T/$\overline{R}$ = V_{IL}	DP8304B			0.8	V
			DP7304B			0.7	V
V_{OH}	Logical "1" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	CD = V_{IL}, T/$\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	CD = V_{IL}, T/$\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = max, Note 4		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	CD = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	CD = V_{IL}, T/$\overline{R}$ = V_{IL}, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	CD = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	CD = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA

DC Electrical Characteristics (cont'd.) (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
Control Inputs CD, $T/\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8304B			0.8	V
			DP7304B			0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	$T/\overline{R}$		-0.1	-0.25	mA
			CD		-0.25	-0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = -12 mA			-0.8	-1.5	V
Power Supply Current							
I_{CC}	Power Supply Current	CD = 2.0V, V_{IN} = 0.4V, V_{CC} = max			70	100	mA
		CD = V_{INA} = 0.4V, $T/\overline{R}$ = 2V, V_{CC} = max			90	140	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	CD = 0.4V, $T/\overline{R}$ = 0.4V (figure A), R1 = 1k, R2 = 5k, C1 = 30pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	CD = 0.4V, $T/\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from CD to A Port	B0 to B7 = 0.4V, $T/\overline{R}$ = 0.4V (figure C) S3 = 1, R5 = 1k, C4 = 15pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from CD to A Port	B0 to B7 = 2.4V, $T/\overline{R}$ = 0.4V (figure C) S3 = 0, R5 = 1k, C4 = 15pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from CD to A Port	B0 to B7 = 0.4V, $T/\overline{R}$ = 0.4V (figure C) S3 = 1, R5 = 1k, C4 = 30pF		27	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from CD to A Port	B0 to B7 = 2.4V, $T/\overline{R}$ = 0.4V (figure C) S3 = 0, R5 = 5k, C4 = 30pF		19	25	ns
B Port Data/Mode Specifications						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	CD = 0.4V, $T/\overline{R}$ = 2.4V (figure A)				
		R1 = 100Ω, R2 = 1k, C1 = 300pF		18	23	ns
		R1 = 667Ω, R2 = 5k, C1 = 45pF		11	18	ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	CD = 0.4V, $T/\overline{R}$ = 2.4V (figure A)				
		R1 = 100Ω, R2 = 1k, C1 = 300pF		16	23	ns
		R1 = 667Ω, R2 = 5k, C1 = 45pF		11	18	ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from CD to B Port	A0 to A7 = 0.4V, $T/\overline{R}$ = 2.4V (figure C) S3 = 1, R5 = 1k, C4 = 15pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from CD to B Port	A0 to A7 = 2.4V, $T/\overline{R}$ = 2.4V (figure C) S3 = 0, R5 = 1k, C4 = 15pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from CD to B Port	A0 to A7 = 0.4V, $T/\overline{R}$ = 2.4V (figure C)				
		S3 = 1, R5 = 100Ω, C4 = 300pF		32	40	ns
		S3 = 1, R5 = 667Ω, C4 = 45pF		16	22	ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from CD to B Port	A0 to A7 = 2.4V, $T/\overline{R}$ = 2.4V (figure C)				
		S3 = 0, R5 = 1k, C4 = 300pF		26	35	ns
		S3 = 0, R5 = 5k, C4 = 45pF		14	22	ns

AC Electrical Characteristics (cont'd.) V_{CC} = 5 V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
Transmit/Receive Mode Specifications						
t_{TRL}	Propagation Delay from Transmit Mode to Receive a Logical "0," T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S1 = 0, R4 = 100 Ω, C3 = 5 pF S2 = 1, R3 = 1k, C2 = 30 pF		30	40	ns
t_{TRH}	Propagation Delay from Transmit Mode to Receive a Logical "1," T/$\overline{R}$ to A Port	CD = 0.4 V (figure B) S1 = 1, R4 = 100 Ω, C3 = 5 pF S2 = 0, R3 = 5k, C2 = 30 pF		28	40	ns
t_{RTL}	Propagation Delay from Receive Mode to Transmit a Logical "0," T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S1 = 1, R4 = 100 Ω, C3 = 300 pF S2 = 0, R3 = 300 Ω, C2 = 5 pF		31	40	ns
t_{RTH}	Propagation Delay from Receive Mode to Transmit a Logical "1," T/$\overline{R}$ to B Port	CD = 0.4 V (figure B) S1 = 0, R4 = 1k, C3 = 300 pF S2 = 1, R3 = 300 Ω, C2 = 5 pF		28	40	ns

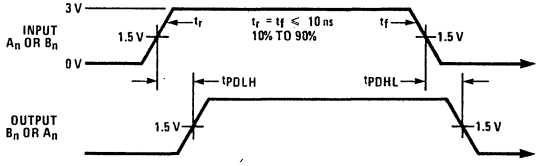
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

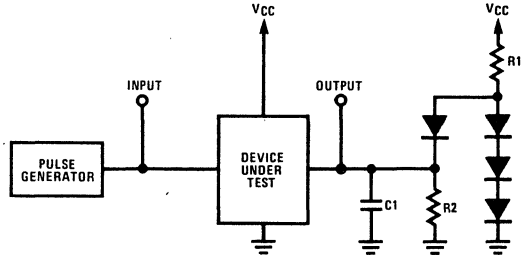
Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5 V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits

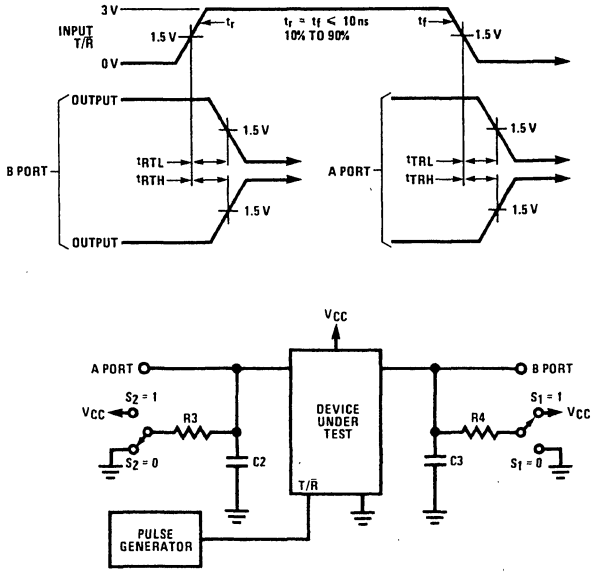




NOTE: C1 INCLUDES TEST FIXTURE CAPACITANCE.

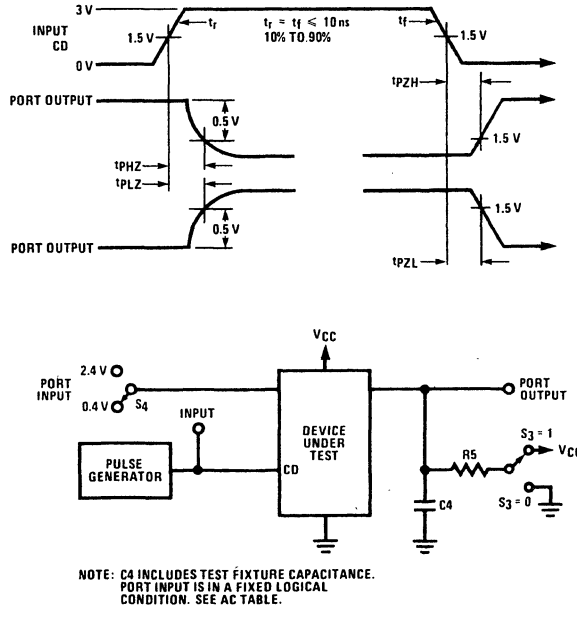
FIGURE A. Propagation Delay from A Port to B Port or from B Port to A Port

Switching Time Waveforms and AC Test Circuits (cont'd.)



NOTE: C2 AND C3 INCLUDE TEST FIXTURE CAPACITANCE.

FIGURE B. Propagation Delay from T/$\overline{R}$ to A Port or B Port



NOTE: C4 INCLUDES TEST FIXTURE CAPACITANCE. PORT INPUT IS IN A FIXED LOGICAL CONDITION. SEE AC TABLE.

FIGURE C. Propagation Delay to/from TRI-STATE® from CD to A Port or B Port

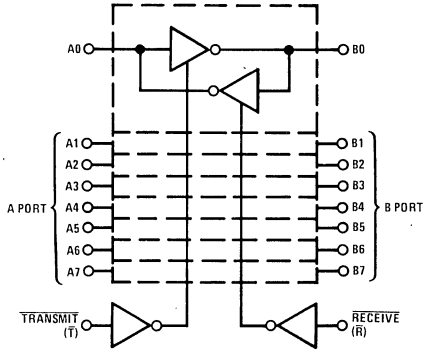
National Semiconductor

DP7307/DP8307 8-Bit TRI-STATE® Bidirectional Transceiver (Inverting)

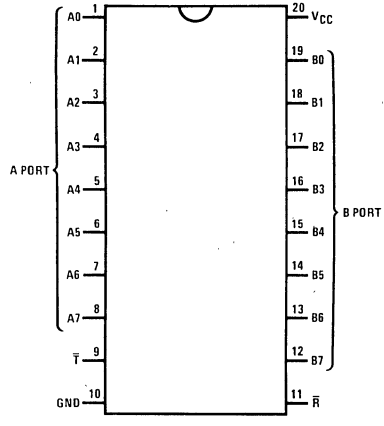
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{T}$ and $\overline{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DP7307J, DP8307J or DP8307N
See NS Package J20A or N20A

Logic Table

CONTROL INPUTS		RESULTING CONDITIONS	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 10 seconds)	300°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7307	4.5	5.5	V
DP8307	4.75	5.25	V
Temperature (T_A)			
DP7307	−55	125	°C
DP8307	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
A Port (A0–A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$	DP8307			0.8	V
			DP7307			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.7$		V
			$I_{OH} = -3$ mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	$I_{OL} = 16$ mA (8307)		0.35	0.5	V
			$I_{OL} = 8$ mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_O = 0V$, V_{CC} = max, Note 4		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{R} = \overline{T} = 2.0V$, V_{CC} = max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_{IN} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V$, $I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			80	μA
B Port (B0–B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$	DP8307			0.8	V
			DP7307			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$	$I_{OH} = -0.4$ mA	$V_{CC}-1.15$	$V_{CC}-0.8$		V
			$I_{OH} = -5$ mA	2.7	3.9		V
			$I_{OH} = -10$ mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$	$I_{OL} = 20$ mA		0.3	0.4	V
			$I_{OL} = 48$ mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T} = V_{IL}$, $\overline{R} = 2.0V$, $V_O = 0V$, V_{CC} = max, Note 4		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_{IH} = 2.7V$			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T} = \overline{R} = 2.0V$, V_{CC} = max, $V_{IH} = 5.25V$				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = 2.0V$, $\overline{R} = V_{IL}$, $V_{IL} = 0.4V$			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R} = 2.0V$, $I_{IN} = -12$ mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R} = 2.0V$	$V_{IN} = 0.4V$			−200	μA
			$V_{IN} = 4.0V$			+200	μA

DC Electrical Characteristics (cont'd.) (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
Control Inputs $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8307			0.8	V
			DP7307			0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	$\overline{R}$		-0.1	-0.25	mA
			$\overline{T}$		-0.25	-0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = -12 mA			-0.8	-1.5	V
Power Supply Current							
I_{CC}	Power Supply Current	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{IN} = 2.0V, V_{CC} = max			70	100	mA
		$\overline{T}$ = 0.4V, V_{INA} = $\overline{R}$ = 2V, V_{CC} = max			100	150	mA

AC Electrical Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		8	12	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		11	16	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 15 pF		10	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 30 pF		25	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V (figure B) S3 = 0, R5 = 5k, C4 = 30 pF		24	35	ns
B Port Data/Mode Specifications						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		12 8	18 12	ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (figure A) R1 = 100Ω, R2 = 1k, C1 = 300 pF R1 = 667Ω, R2 = 5k, C1 = 45 pF		15 9	23 14	ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V (figure B) S3 = 1, R5 = 100Ω, C4 = 300 pF S3 = 1, R5 = 667Ω, C4 = 45 pF		32 18	40 25	ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		25 16	35 25	ns ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits

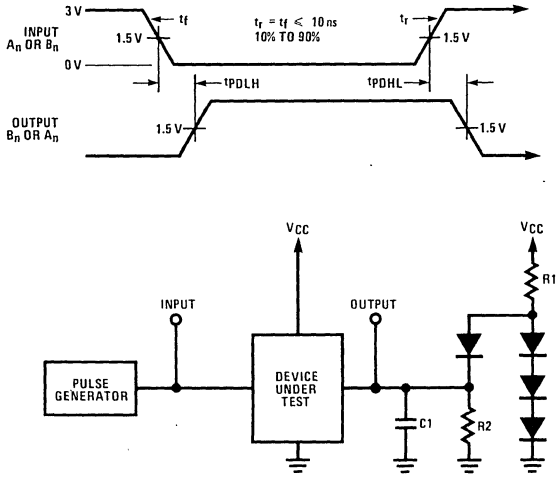


FIGURE A. Propagation Delay from A port to B port or from B port to A port

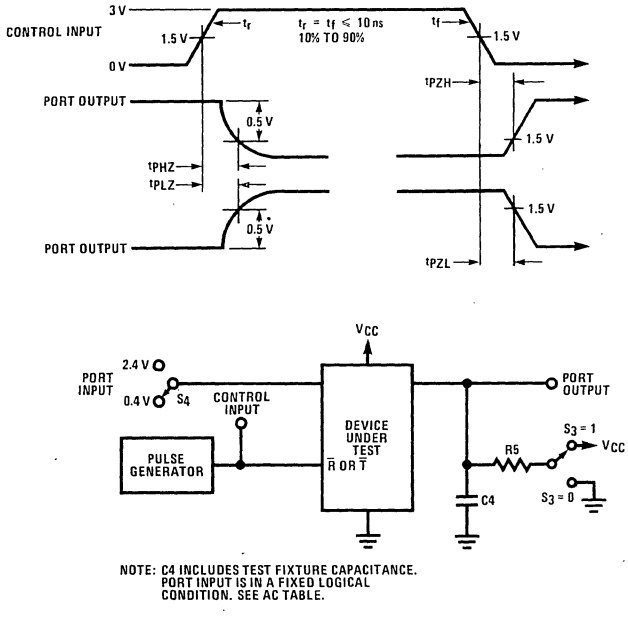


Figure B. Propagation Delay to/from TRI-STATE from $\overline{R}$ to A Port and $\overline{T}$ to B Port

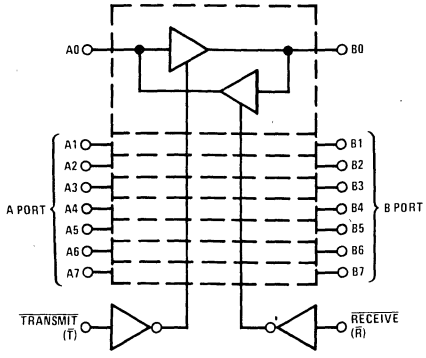
National Semiconductor

DP7308/DP8308 8-Bit TRI-STATE® Bidirectional Transceiver (Non-Inverting)

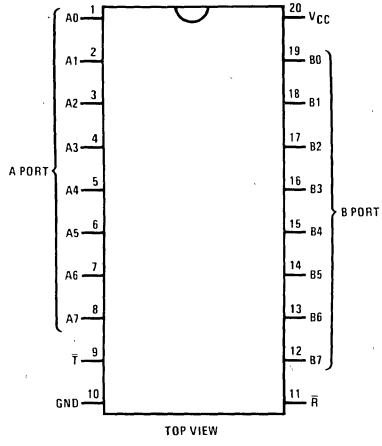
Features

- 8-bit bidirectional data flow reduces system package count
- Bidirectional TRI-STATE inputs/outputs interface with bus oriented systems
- PNP inputs reduce input loading
- Output high voltage interfaces with TTL, MOS, and CMOS
- 48 mA/300 pF bus drive capability
- Pinouts simplify system interconnections
- Independent $\overline{T}$ and $\overline{R}$ controls for versatility
- Compact 20-pin dual-in-line package
- Bus port glitch free power up/down

Logic and Connection Diagrams



Dual-In-Line Package



Order Number DP7308J, DP8308J or DP8308N
See NS Package J20A or N20A

Logic Table

CONTROL INPUTS		RESULTING CONDITIONS	
$\overline{\text{Transmit}}$	$\overline{\text{Receive}}$	A Port	B Port
1	0	OUT	IN
0	1	IN	OUT
1	1	TRI-STATE	TRI-STATE
0	0	Both Active*	

*This is not an intended logic condition and may cause oscillations.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (soldering, 10 seconds)	300°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DP7308	4.5	5.5	V
DP8308	4.75	5.25	V
Temperature (T_A)			
DP7308	−55	125	°C
DP8308	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
A Port (A0-A7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V	DP8308			0.8	V
			DP7308			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.7		V
			I_{OH} = −3 mA	2.7	3.95		V
V_{OL}	Logical "0" Output Voltage	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$	I_{OL} = 16 mA (8308)		0.35	0.5	V
			I_{OL} = 8 mA (both)		0.3	0.4	V
I_{OS}	Output Short Circuit Current	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$, V_O = 0V, V_{CC} = max, Note 4		−10	−38	−75	mA
I_{IH}	Logical "1" Input Current	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{R} = \overline{T}$ = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R}$ = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R}$ = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			80	μA
B Port (B0-B7)							
V_{IH}	Logical "1" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$		2.0			V
V_{IL}	Logical "0" Input Voltage	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$	DP8308			0.8	V
			DP7308			0.7	V
V_{OH}	Logical "1" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V	I_{OH} = −0.4 mA	V_{CC}−1.15	V_{CC}−0.8		V
			I_{OH} = −5 mA	2.7	3.9		V
			I_{OH} = −10 mA	2.4	3.6		V
V_{OL}	Logical "0" Output Voltage	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V	I_{OL} = 20 mA		0.3	0.4	V
			I_{OL} = 48 mA		0.4	0.5	V
I_{OS}	Output Short Circuit Current	$\overline{T} = V_{IL}$, $\overline{R}$ = 2.0V, V_O = 0V, V_{CC} = max, Note 4		−25	−50	−150	mA
I_{IH}	Logical "1" Input Current	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$, V_{IH} = 2.7V			0.1	80	μA
I_I	Input Current at Maximum Input Voltage	$\overline{T} = \overline{R}$ = 2.0V, V_{CC} = max, V_{IH} = 5.25V				1	mA
I_{IL}	Logical "0" Input Current	$\overline{T}$ = 2.0V, $\overline{R} = V_{IL}$, V_{IN} = 0.4V			−70	−200	μA
V_{CLAMP}	Input Clamp Voltage	$\overline{T} = \overline{R}$ = 2.0V, I_{IN} = −12 mA			−0.7	−1.5	V
I_{OD}	Output/Input TRI-STATE Current	$\overline{T} = \overline{R}$ = 2.0V	V_{IN} = 0.4V			−200	μA
			V_{IN} = 4.0V			+200	μA

DC Electrical Characteristics (cont'd.) (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
Control Inputs $\overline{T}$, $\overline{R}$							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage		DP8308			0.8	V
			DP7308			0.7	V
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V			0.5	20	μA
I_I	Maximum Input Current	V_{CC} = max, V_{IH} = 5.25V				1.0	mA
I_{IL}	Logical "0" Input Current	V_{IL} = 0.4V	$\overline{R}$		−0.1	−0.25	mA
			$\overline{T}$		−0.25	−0.5	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
Power Supply Current							
I_{CC}	Power Supply Current	$\overline{T}$ = $\overline{R}$ = 2.0V, V_{IN} = 0.4V, V_{CC} = max			70	100	mA
		$\overline{T}$ = V_{INA} = 0.4V, $\overline{R}$ = 2V, V_{CC} = max			90	140	mA

AC Electrical Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		Conditions	Min	Typ	Max	Units
A Port Data/Mode Specifications						
t_{PDHLA}	Propagation Delay to a Logical "0" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		14	18	ns
t_{PDLHA}	Propagation Delay to a Logical "1" from B Port to A Port	$\overline{T}$ = 2.4V, $\overline{R}$ = 0.4V (figure A) R1 = 1k, R2 = 5k, C1 = 30 pF		13	18	ns
t_{PLZA}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 15 pF		11	15	ns
t_{PHZA}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLA}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{R}$ to A Port	B0 to B7 = 0.4V, $\overline{T}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 30 pF		24	35	ns
t_{PZHA}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{R}$ to A Port	B0 to B7 = 2.4V, $\overline{T}$ = 2.4V (figure B) S3 = 0, R5 = 5k, C4 = 30 pF		21	30	ns
B Port Data/Mode Specifications						
t_{PDHLB}	Propagation Delay to a Logical "0" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (figure A) R1 = 100 Ω, R2 = 1k, C1 = 300 pF R1 = 667 Ω, R2 = 5k, C1 = 45 pF		 18 11	 23 18	 ns ns
t_{PDLHB}	Propagation Delay to a Logical "1" from A Port to B Port	$\overline{T}$ = 0.4V, $\overline{R}$ = 2.4V (figure A) R1 = 100 Ω, R2 = 1k, C1 = 300 pF R1 = 667 Ω, R2 = 5k, C1 = 45 pF		 16 11	 23 18	 ns ns
t_{PLZB}	Propagation Delay from a Logical "0" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V (figure B) S3 = 1, R5 = 1k, C4 = 15 pF		13	18	ns
t_{PHZB}	Propagation Delay from a Logical "1" to TRI-STATE from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 15 pF		8	15	ns
t_{PZLB}	Propagation Delay from TRI-STATE to a Logical "0" from $\overline{T}$ to B Port	A0 to A7 = 0.4V, $\overline{R}$ = 2.4V (figure B) S3 = 1, R5 = 100 Ω, C4 = 300 pF S3 = 1, R5 = 667 Ω, C4 = 45 pF		 25 17	 35 25	 ns ns
t_{PZHB}	Propagation Delay from TRI-STATE to a Logical "1" from $\overline{T}$ to B Port	A0 to A7 = 2.4V, $\overline{R}$ = 2.4V (figure B) S3 = 0, R5 = 1k, C4 = 300 pF S3 = 0, R5 = 5k, C4 = 45 pF		 24 17	 35 25	 ns ns

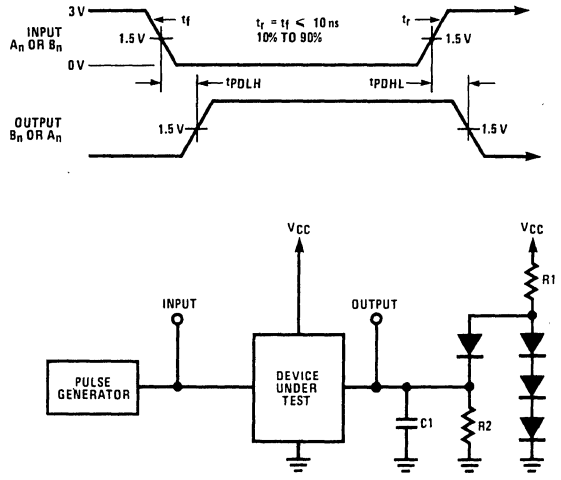
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of Recommended Operating Conditions. All typical values given are for V_{CC} = 5 V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

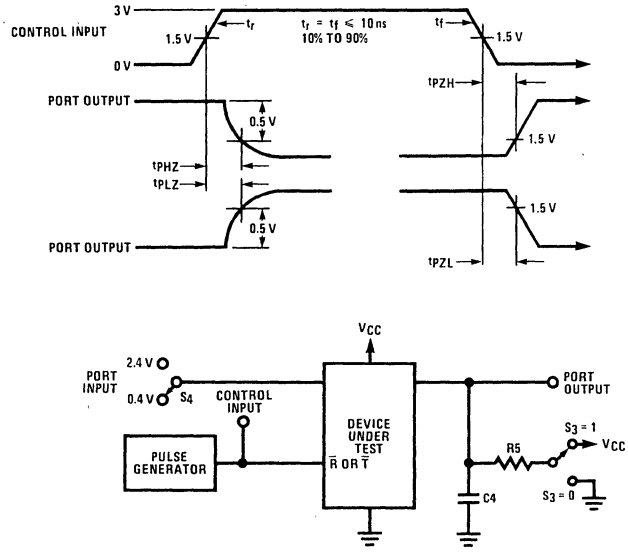
Note 4: Only one output at a time should be shorted.

Switching Time Waveforms and AC Test Circuits



NOTE: C1 INCLUDES TEST FIXTURE CAPACITANCE.

FIGURE A. Propagation Delay from A port to B port or from B port to A port



NOTE: C4 INCLUDES TEST FIXTURE CAPACITANCE.
PORT INPUT IS IN A FIXED LOGICAL CONDITION. SEE AC TABLE.

Figure B. Propagation Delay to/from TRI-STATE from $\overline{R}$ to A Port and $\overline{T}$ to B Port

National Semiconductor

DS26S10, DS26S11 Quad Bus Transceivers

General Description

The DS26S10 and DS26S11 are quad Bus Transceivers consisting of 4 high speed bus drivers with open-collector outputs capable of sinking 100 mA at 0.8V and 4 high speed bus receivers. Each driver output is connected internally to the high speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving 10 Schottky TTL unit loads.

An active low enable gate controls the 4 drivers so that outputs of different device drivers can be connected together for party-line operation.

The bus output high-drive capability in the low state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2V.

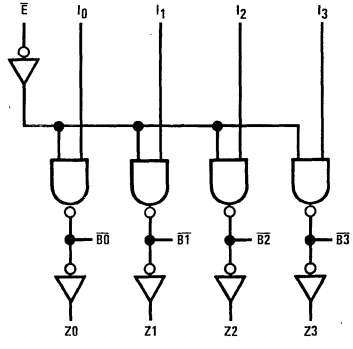
The DS26S10 and DS26S11 feature advanced Schottky processing to minimize propagation delay. The device package also has 2 ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND 1 and GND 2 should be tied to the ground bus external to the device package.

Features

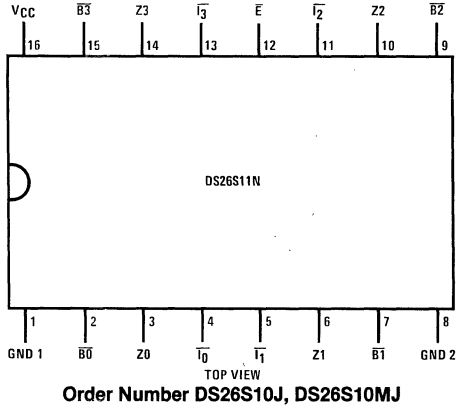
- Input to bus is inverting on DS26S10
- Input to bus is non-inverting on DS26S11
- Quad high speed open-collector bus transceivers
- Driver outputs can sink 100 mA at 0.8V maximum
- Advanced Schottky processing
- PNP inputs to reduce input loading

Logic and Connection Diagrams

DS26S10



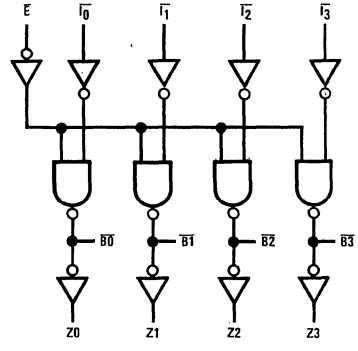
Dual-In-Line Package



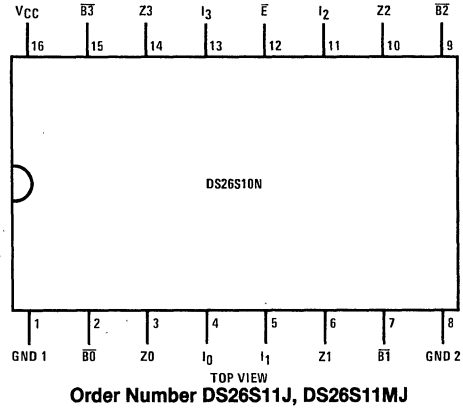
TOP VIEW

Order Number DS26S10J, DS26S10MJ or DS26S10N
See NS Package J16A or N16A

DS26S11



Dual-In-Line Package



TOP VIEW

Order Number DS26S11J, DS26S11MJ or DS26S11N
See NS Package J16A or N16A

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} Max
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Bus	200 mA
Output Current, Into Outputs (Except Bus)	30 mA
DC Input Current	−30 mA to +5 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS26S10XC, DS26S11XC	4.75	5.25	V
DS26S10XM, DS26S11XM	4.5	5.5	V
Temperature (T_A)			
DS26S10XC, DS26S11XC	0	+70	°C
DS26S10XM, DS26S11XM	−55	+125	°C

Electrical Characteristics (Unless otherwise noted)

PARAMETER		CONDITIONS (Note 1)		MIN	TYP (Note 2)	MAX	UNITS
V_{OH}	Output High Voltage (Receiver Outputs)	V_{CC} = Min, I_{OH} = −1 mA, V_{IN} = V_{IL} or V_{IH}	Military	2.5	3.4		V
			Commercial	2.7	3.4		V
V_{OL}	Output Low Voltage (Receiver Outputs)	V_{CC} = Min, I_{OL} = 20 mA, V_{IN} = V_{IL} or V_{IH}				0.5	V
V_{IH}	Input High Level (Except Bus)	Guaranteed Input Logical High for All Inputs		2.0			V
V_{IL}	Input Low Level (Except Bus)	Guaranteed Input Logical Low for All Inputs				0.8	V
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{IL}	Input Low Current (Except Bus)	V_{CC} = Max, V_{IN} = 0.4V	Enable			−0.36	mA
			Data			−0.54	mA
I_{IH}	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 2.7V	Enable			20	μA
			Data			30	μA
I_I	Input High Current (Except Bus)	V_{CC} = Max, V_{IN} = 5.5V				100	μA
I_{SC}	Output Short-Circuit Current (Except Bus)	V_{CC} = Max, (Note 3)	Military	−20		−55	mA
			Commercial	−18		−60	mA
I_{CCL}	Power Supply Current (All Bus Outputs Low)	V_{CC} = Max, Enable = Gnd	DS26S10		45	70	mA
			DS26S11			80	mA

Bus Input/Output Characteristics

PARAMETER		CONDITIONS (Note 1)			MIN	TYP (Note 2)	MAX	UNITS
V_{OL}	Output Low Voltage	V_{CC} = Min	Military	I_{OL} = 40 mA		0.33	0.5	V
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
			Commercial	I_{OL} = 40 mA		0.33	0.5	
				I_{OL} = 70 mA		0.42	0.7	
				I_{OL} = 100 mA		0.51	0.8	
I_O	Bus Leakage Current	V_{CC} = Max		V_O = 0.8V			−50	μA
			Military	V_O = 4.5V			200	
			Commercial	V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input High Threshold	Bus Enable = 2.4V, V_{CC} = Max	Military		2.4	2.0		V
			Commercial		2.25	2.0		V
V_{TL}	Receiver Input Low Threshold	Bus Enable = 2.4V, V_{CC} = Min	Military			2.0	1.6	V
			Commercial			2.0	1.75	V

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5V, 25°C ambient and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics ($T_A = 25°C$, $V_{CC} = 5V$)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Data Input to Bus	$R_B = 50\Omega$, $C_B = 50$ pF (Note 1)	DS26S10		10	15	ns
t_{PHL}	Data Input to Bus				10	15	ns
t_{PLH}	Data Input to Bus		DS26S11		12	19	ns
t_{PHL}	Data Input to Bus				12	19	ns
t_{PLH}	Enable Input to Bus		DS26S10		14	18	ns
t_{PHL}	Enable Input to Bus				13	18	ns
t_{PLH}	Enable Input to Bus		DS26S11		15	20	ns
t_{PHL}	Enable Input to Bus				14	20	ns
t_{PLH}	Bus to Receiver Out	$R_B = 50\Omega$, $R_L = 280\Omega$, $C_B = 50$ pF (Note 1), $C_L = 15$ pF			10	15	ns
t_{PHL}	Bus to Receiver Out				10	15	ns
t_r	Bus	$R_B = 50\Omega$, $C_B = 50$ pF (Note 1)		4.0	10		ns
t_f	Bus			2.0	4.0		ns

Note 1: Includes probe and jig capacitance

Truth Tables

DS26S10

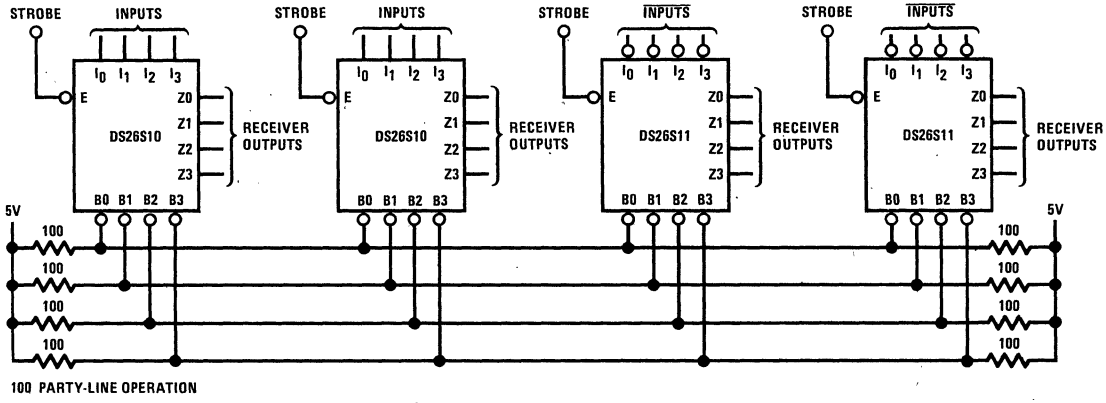
INPUTS		OUTPUTS	
$\overline{E}$	I	$\overline{B}$	Z
L	L	H	L
L	H	L	H
H	X	Y	$\overline{Y}$

DS26S11

INPUTS		OUTPUTS	
$\overline{E}$	$\overline{I}$	$\overline{B}$	Z
L	L	L	H
L	H	H	L
H	X	Y	$\overline{Y}$

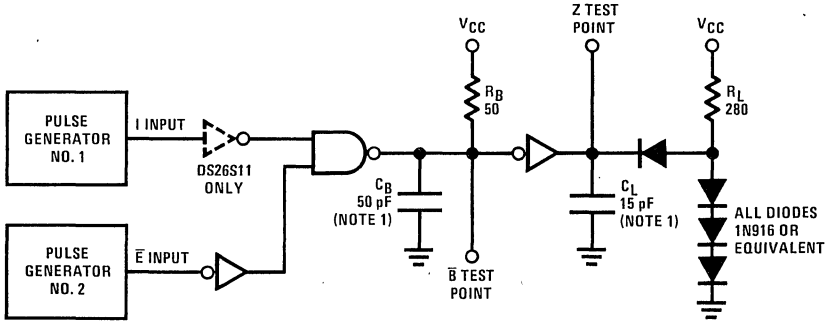
H = High voltage level
L = Low voltage level
X = Don't care
Y = Voltage level of bus (assumes control by another bus transceiver)

Typical Application

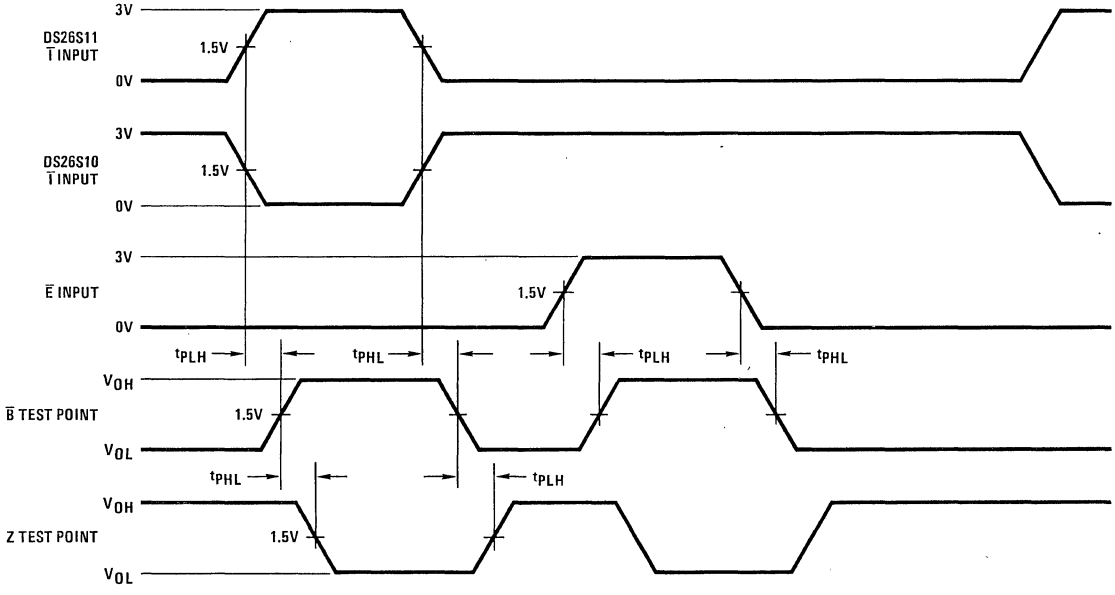


100 PARTY-LINE OPERATION

AC Test Circuit and Switching Time Waveforms

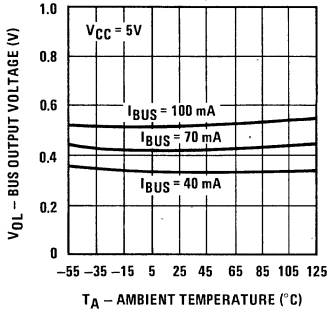


Note 1: Includes probe and jig capacitance.

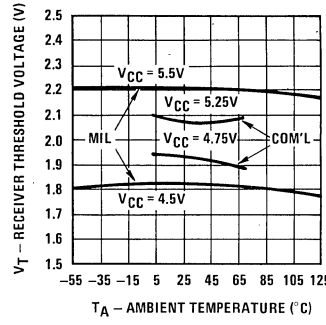


Typical Performance Characteristics

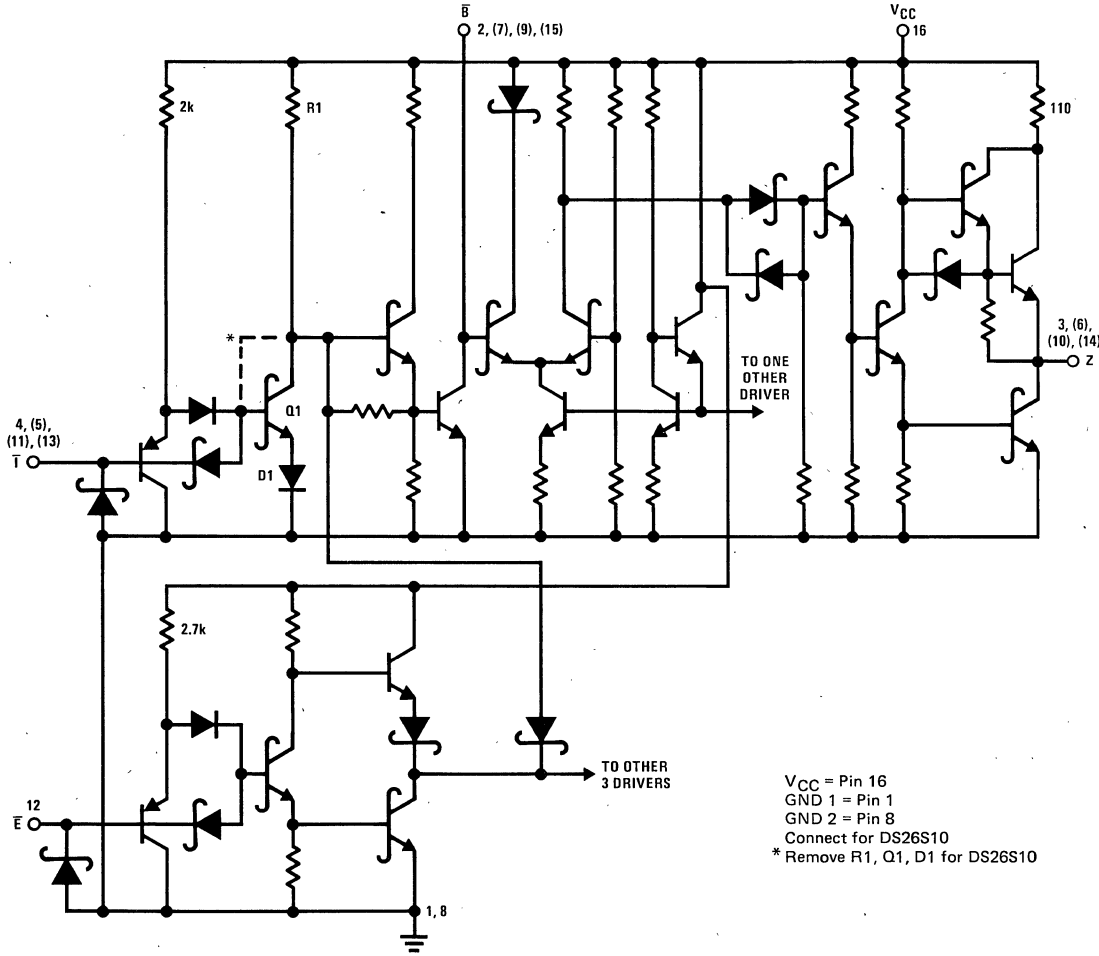
Typical Bus Output Low Voltage vs Ambient Temperature



Receiver Threshold Variation vs Ambient Temperature



Schematic Diagram



V_{CC} = Pin 16
GND 1 = Pin 1
GND 2 = Pin 8
Connect for DS26S10
* Remove R1, Q1, D1 for DS26S10

DS3662 Quad High Speed Trapezoidal™ Bus Transceiver

General Description

The DS3662 is a quad high speed Schottky bus transceiver intended for use with terminated 120Ω impedance lines. It is specifically designed to reduce noise in unbalanced transmission systems. The open collector drivers generate precise trapezoidal waveforms with rise and fall times of 15 ns (typical), which are relatively independent of capacitive loading conditions on the outputs. This reduces noise coupling to the adjacent lines without any appreciable impact on the maximum data rate obtainable with high speed bus transceivers. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity. Tightly controlled threshold levels on the receiver provide equal rejection to both negative and positive going noise pulses on the bus.

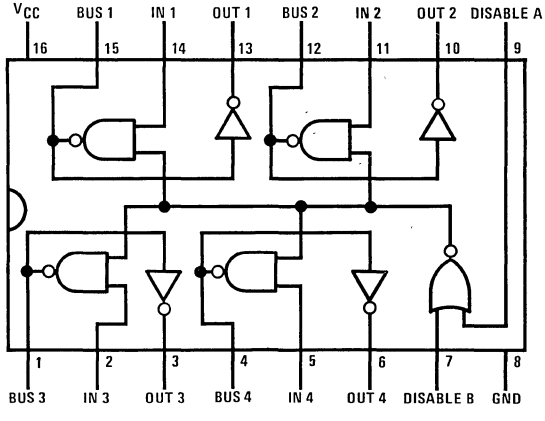
The external termination is intended to be a 180Ω resistor from the bus to 5V logic supply, together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. A two input NOR gate is provided to disable all drivers in a package simultaneously.

Features

- Pin to pin functional replacement for DS8641
- Guaranteed AC specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Temperature insensitive receiver thresholds track bus logic level
- Trapezoidal bus waveforms reduce noise coupling to adjacent lines
- Precision receiver thresholds provide maximum noise immunity and symmetrical response to positive and negative going pulses
- Open collector driver output allows wire-OR connection
- High speed Schottky technology
- 15 μA typical bus termination current with normal V_{CC} or with $V_{CC} = 0V$
- Glitch free power up/down protection on the driver output
- TTL compatible driver and disable inputs, and receiver outputs

Block and Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS3662J or DS3662N
See NS Package J16A or N16A

Trapezoidal™ is a trademark of National Semiconductor

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature Range (T_A)	0	70	°C

* Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions	Min	Typ	Max	Units
DRIVER AND DISABLE INPUTS						
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
I_I	Logical "1" Input Current	$V_{IN} = 5.5V$			1	mA
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.4V$			40	μA
I_{IL}	Logical "0" Input Current	$V_{IN} = 0.4V$		−1	−1.6	mA
V_{CL}	Input Diode Clamp Voltage	$I_{CLAMP} = -12$ mA		−0.8	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT						
V_{OLB}	Low Level Bus Voltage	$V_{DIS} = 0.8V$, $V_{IN} = 2V$, $I_{BUS} = 100$ mA		0.6	0.9	V
I_{IHB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = 5.25V$		10	100	μA
I_{ILB}	Maximum Bus Current	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $V_{CC} = 0V$			100	μA
V_{IH}	High Level Receiver Threshold	$V_{IN} = 0.8V$, $I_{OL} = 16$ mA	1.90	1.70		V
V_{IL}	Low Level Receiver Threshold	$V_{IN} = 0.8V$, $I_{OH} = -400$ μA		1.70	1.50	V
RECEIVER OUTPUT						
V_{OH}	Logical "1" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $I_{OH} = -400$ μA	2.4	3.2		V
V_{OL}	Logical "0" Output Voltage	$V_{IN} = 0.8V$, $V_{BUS} = 4V$, $I_{OL} = 16$ mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	$V_{DIS} = 0.8V$, $V_{IN} = 0.8V$, $V_{BUS} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = 5.25V$, (Note 4)	−40	−70	−100	mA
I_{CC}	Supply Current	$V_{DIS} = 0V$, $V_{IN} = 2V$		50	90	mA

Switching Characteristics (Notes 2 and 3)

Parameter		Conditions	Min	Typ	Max	Units
PROPAGATION DELAYS						
t_{PLHD}	Disable to Bus "1"	*Figure 1*		25	35	ns
t_{PHLD}	Disable to Bus "0"			25	35	ns
t_{PLHB}	Driver Input to Bus "1"	*Figure 2*		20	30	ns
t_{PHLB}	Driver Input to Bus "0"			20	30	ns
t_{PLHR}	Bus to Logical "1" Receiver Output	*Figure 3*		25	40	ns
t_{PHLR}	Bus to Logical "0" Receiver Output			25	40	ns
NOISE IMMUNITY						
t_{rB}, t_{fB}	Rise and Fall Times (10%-90%) of the Driver Output	*Figure 2*	10	15	20	ns
t_{nR}	Receiver Noise Rejection Pulse Width	No Response at Receiver Output as per *Figure 4*		20	10	ns

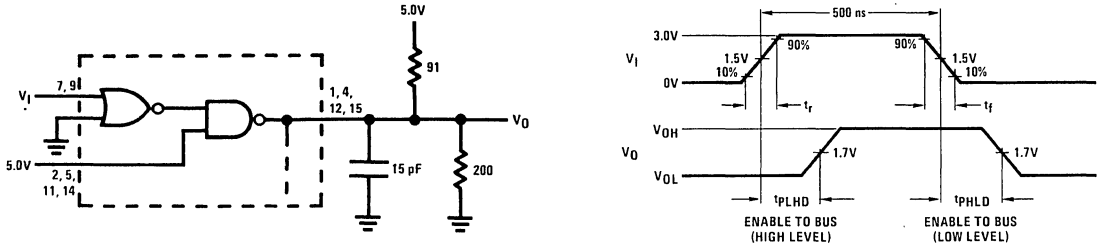
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" and "Recommended Operating Conditions" provide conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the supply and temperature range listed in the table of "Recommended Operating Conditions". All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

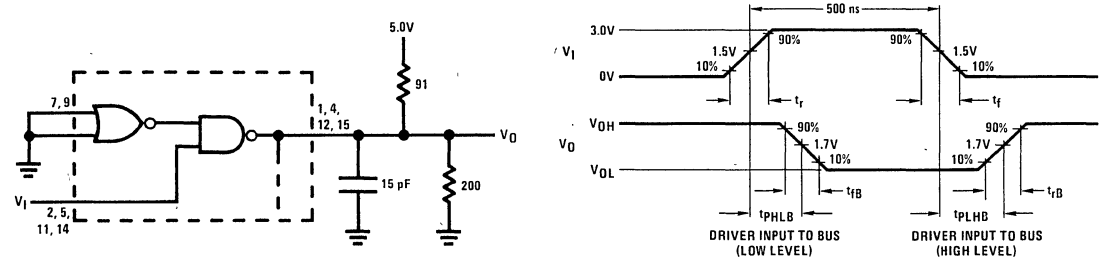
Note 4: Only one output at a time should be shorted.

AC Test Circuits and Switching Waveforms



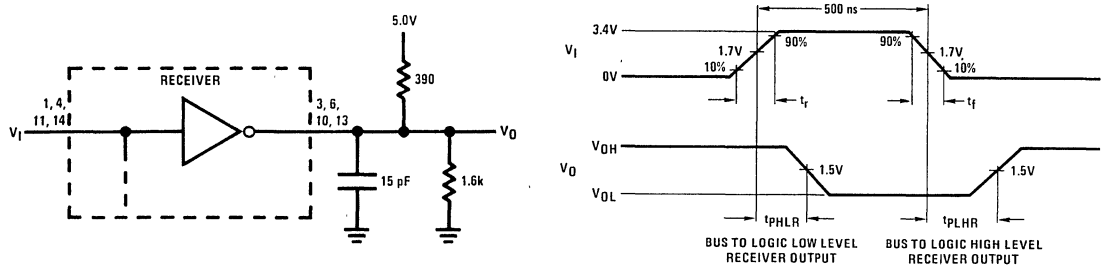
Note. $t_r = t_f = 2.5$ ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz.

FIGURE 1. Disable Delays



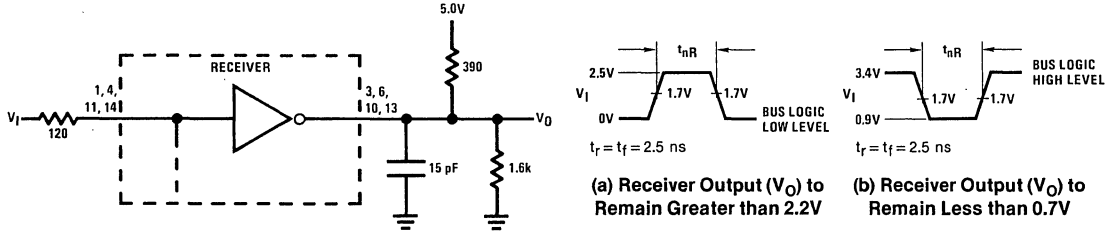
Note. $t_r = t_f = 2.5$ ns. Pulse width = 500 ns measured between 1.5V levels. f = 1 MHz.

FIGURE 2. Driver Propagation Delays



Note. $t_r = t_f = 15$ ns. Pulse width = 500 ns measured between 1.7V levels. f = 1 MHz.

FIGURE 3. Receiver Propagation Delays



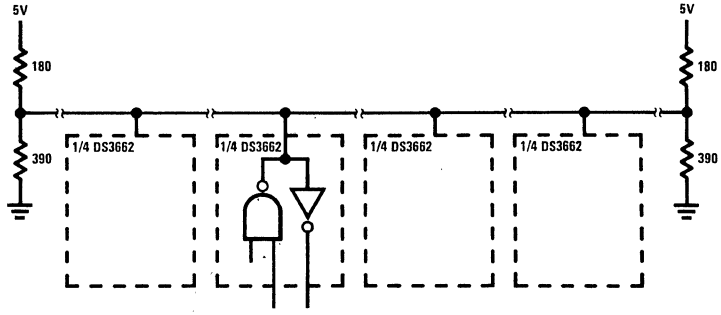
(a) Receiver Output (V_O) to Remain Greater than 2.2V

(b) Receiver Output (V_O) to Remain Less than 0.7V

FIGURE 4. Receiver Noise Immunity: "No Response at Output" Input Waveforms

Typical Application

120Ω Unified Data Bus



DS3662 — The Bus Optimizer

National Semiconductor
Application Note 259
R.V. Balakrishnan
April 1981

I. Introduction

A single ended Bus is an unbalanced Data Transmission medium, which is timeshared by several system elements. Like any unbalanced system, it is highly susceptible to common-mode noise, such as ground noise and crosstalk. In general, the latter determines the maximum physical length of the Bus that can be incorporated with acceptable reliability. Crosstalk is a major problem in high speed computer Buses which employ Schottky Transceivers for increased data rate capability. It is therefore highly desirable to minimize crosstalk noise in Bus circuits to allow for longer Buses and to provide higher system reliability.

This article describes the operation of the DS3662 Quad High Speed Trapezoidal Bus Tranceiver, which has been specially designed to minimize crosstalk problems. The Driver generates precise Trapezoidal waveforms that reduce noise coupling to adjacent Bus channels. The Receiver uses a low pass filter, whose time constant is matched to the Driver slew rate to provide maximum noise rejection with acceptable signal delay characteristics. Precision high speed circuitry optimizes noise immunity without sacrificing the high data rate capability of Schottky Tranceivers.

II. The Problem

Conventional Bus Drivers are designed to provide high output currents for charging and discharging relatively large Bus capacitances quickly. These high speed transitions are characterized by peak slew rates of up to 5 volts/ns around the mid-region of the transition. This can cause considerable noise coupling to adjacent lines, commonly referred to as crosstalk. Crosstalk also includes noise induced by sources external to the Bus. Additional noise may be generated due to reflections at imperfect terminations.

Bus Receivers are designed to respond to high speed transitions and to provide low propagation delays. Unfortunately, their fast response results in high noise sensitivity. The combined effect of the noise on the Bus and the sensitivity of the Receiver to the noise severely limits the Bus performance.

III. The Solution

The above situation can be considerably improved by employing noise reduction techniques in both the Driver and the Receiver circuits. Slew rate control can be used in the Driver to reduce crosstalk, and Receiver noise sensitivity can be reduced by using a low pass filter at its input. These techniques are commonly used in line transmission circuits where the associated data rates in general are considerably lower. However, these techniques do present some difficulties in high speed Bus circuits. Increased rise and fall times, resulting from slew rate control, can affect data rates unless care is taken to limit the maximum rise and fall times to minimum pulse width requirements. With any appreciable slew rate control, the rise and fall times of the resulting Driver output waveform will be comparable to the pulse widths at maximum data rates. This condition dictates high fidelity of the transmitted waveform and precise Receiver thresholds at the middle of the Bus voltage swing in order to minimize pulse width distortion. *Figure 1* illustrates the different sources of pulse width distortion due to the trapezoidal nature of the signal.

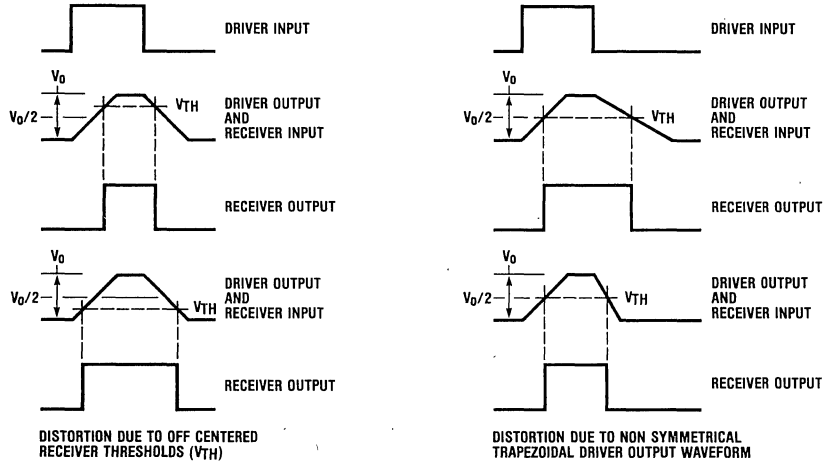


Figure 1. Pulse Width Distortion

The low pass filter in the Receiver should provide optimum noise rejection without introducing excessive delay in passing the signal waveform. In addition, the Receiver should have a symmetrical response to positive and negative going transitions in order to maintain a low level of pulse width distortion, as well as equal noise rejection to positive and negative going noise pulses. The response of an ideal low pass filter to signal and noise pulses is shown in *Figure 2*.

The DS3662 overcomes these and other problems by using high speed linear circuitry with on-chip capacitors for controlling slew rate and low pass filtering. The Driver is of open collector type intended for use with terminated 120 ohm Buses. The external termination consists of a 180 ohm resistor from the Bus to +5 volts logic supply with a 390 ohm resistor from the Bus to ground. Such a termination results in a Bus logic high level of 3.4 volts with V_{CC} at 5 volts (see *Figure 2*). The Bus can be terminated at one or both ends as shown in *Figure* 3.

IV. The Driver

Using a Miller integrator circuit, the Driver generates a linearly rising and falling waveform with a constant slew rate of 0.2 volts/ns (typical) during the entire period of transition. This corresponds to typical rise and fall times of 15 ns. *Figure 4* compares the output waveform of a typical Schottky Driver and the DS3662 under different capacitive loads. It should be noted that even under heavy loading, the regular Drivers have peak slew rates that are considerably higher than the average. In contrast, the trapezoidal waveform provides considerably lower slew rate with slightly higher rise and fall times. Such an increase in rise and fall time has very little effect on data rates. In fact, the high fidelity of the transmitted waveform allows pulse widths as low as 20 ns to be transmitted on the Bus, as shown in *Figure 5*.

The block diagram of the Driver is shown in *Figures 6* and *7*. When a high to low transition is applied to the input, switch 'S' opens and node 'A' is pulled low by the current source 'I'. This switches the amplifier output to a high state. The slew rate of the output transition is limited by the charging current through the capacitor, a constant value equal to I/C volts/sec.

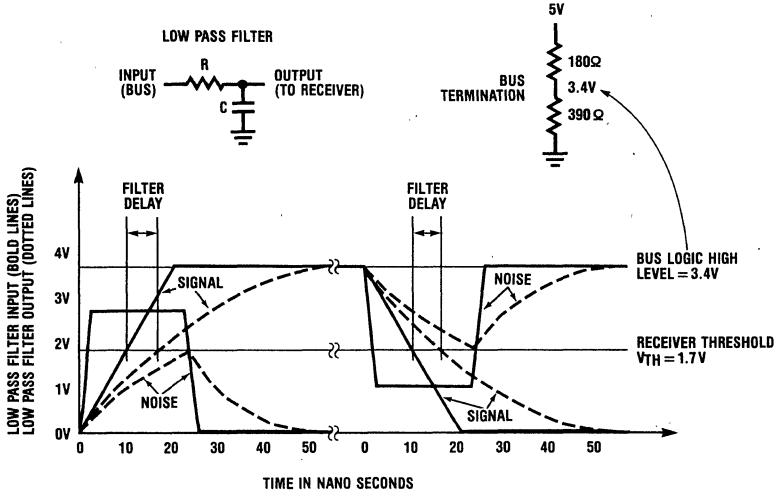


Figure 2. Ideal Receiver Low Pass Filter Response

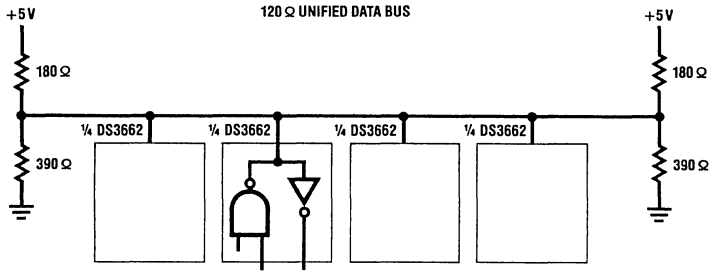
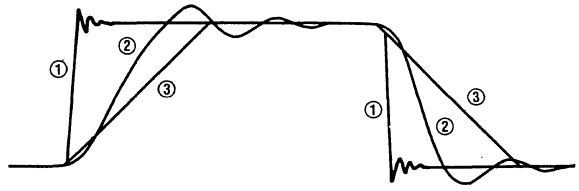


Figure 3. Bus Termination



①— TYPICAL HIGH SPEED DRIVER OUTPUT UNLOADED
②— TYPICAL HIGH SPEED DRIVER OUTPUT LOADED
③— TYPICAL OUTPUT OF CONTROLLED SLEW RATE DRIVER WHICH IS LOAD INDEPENDENT

①$t_r = t_f \approx 3$ ns
②$t_r = t_f \approx 10$ ns
③$t_r = t_f \approx 15$ ns

NOTE: THE WORD 'LOADING' HERE REFERS TO CAPACITIVE LOADING ONLY.

Figure 4. Waveform Comparison

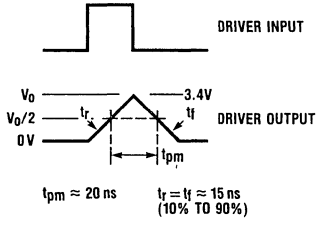


Figure 5. Minimum Pulse Width Driver Output

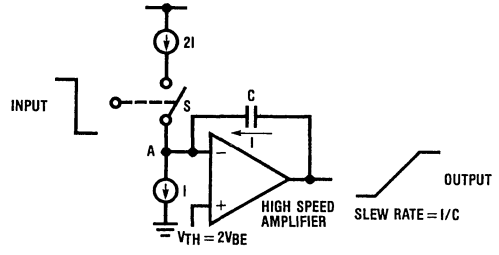


Figure 6. Driver

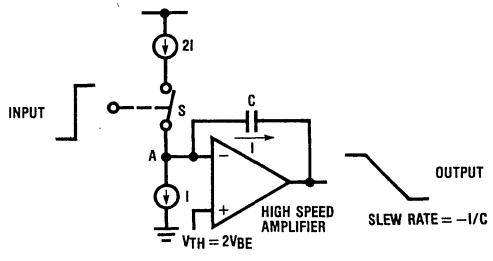


Figure 7. Driver

Likewise, when a low to high transition is applied to the input, switch 'S' closes and node 'A' is pulled up by the '2I' current source, switching the amplifier output to a low state. The capacitor now has an equal but opposite charging current which once again limits the slew rate to $-I/C$ volts/sec. The inherent tracking ability of I.C. current sources provide equal rise and fall times resulting in a symmetrical output waveform.

The on-chip capacitors are fabricated using back to back junction diodes. The use of junction capacitors reduces die area and the back to back connection allows operation with either polarity. The capacitor terminal, connected to the amplifier input, remains at $V_{th} \simeq 1.6$ volts during the output transition. This voltage, being close to the middle of the output swing, reduces the effect of the capacitor voltage sensitivity on the output waveshape.

V. The Receiver

The Receiver consists of a low pass filter followed by a high speed comparator with a typical threshold of 1.7 volts (see *Figure 8*). This threshold value corresponds to the mid-point voltage of the 0 to 3.4 volt Bus swing. It is derived from a potential divider allowing the Bus logic levels to track with V_{CC} variations. If the low pass filter capacitor is voltage insensitive, this circuit will provide equal propagation delay for positive and negative going signal transitions on the Bus. In addition, it will also provide equal noise rejection to a positive and negative going pulse (see *Figure 2*). However, the junction capacitors, being voltage sensitive, will exhibit non-symmetrical response in the above circuit. This problem is overcome in the DS3662 Receiver by using a back to back junction capacitor with the ground end biased at 1.7 volts (see *Figure 9*). Although the capacitor still varies with the voltage at node 'A', the variation is symmetrical about 1.7 volts (the middle of the Bus swing) and therefore will provide an identical response to transitions of either polarity.

VI. Transceiver Performance

The characteristics of the trapezoidal Transceiver are fully detailed in the device data sheet. Some of the more important specifications are discussed below. Both AC and DC specifications are guaranteed over a 0-70°C temperature range and a supply range of 4.75-5.25 volts.

The Driver typically has a propagation delay of 15ns with a maximum of 30ns. The Receiver propagation delays are specified at 25ns typical and 40ns maximum. The Driver output rise and fall times are guaranteed to be within 10 to 20ns with a typical of 15ns. The noise immunity of the Receiver is specified in terms of the width of a 2.5 volt pulse that is guaranteed to be rejected by the Receiver (see *Figure 10*). The Receiver typically rejects a 20ns pulse going positive from ground level or going negative from a 3.4 volt logic 1 level. Worst case rejection is specified at 10ns.

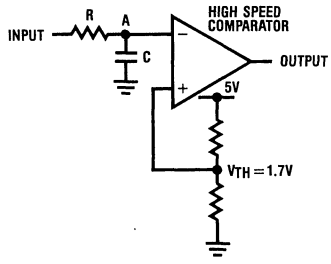


Figure 8. Receiver

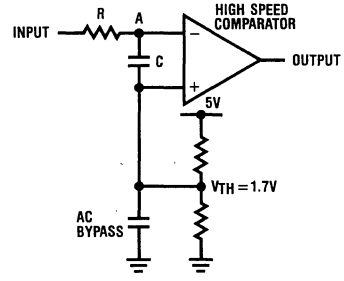
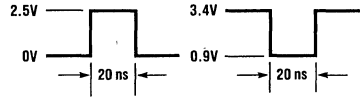


Figure 9. Receiver



REJECTS POSITIVE OR NEGATIVE GOING NOISE PULSES OF PULSE WIDTHS UP TO 20 ns TYPICAL.
DETECTS AND PROPAGATES TRAPEZOIDAL SIGNAL PULSES IN 20 ns TYPICAL.

Figure 10. Receiver Noise Immunity

The AC response of the DS3662 Driver and Receiver are depicted in *Figures 11* and *12* respectively. *Figure 11* shows the typical Driver output waveform as compared to a standard high speed Transceiver output. Oscillograms in *Figure 12* demonstrate the ability of the Receiver to distinguish the trapezoidal signal from the noise. Here the Receiver rejects a noise pulse of 19ns width, while accepting a narrower signal pulse (=16ns) of the same amplitude (The signal is triangular since the pulse width is smaller than the rise and fall time of the Trapezoidal Driver output).

The performance of the Transceiver under actual operating condition is demonstrated in *Figures 13* through *15*. Oscillograms in *Figure 13* clearly show the capability of the DS3662 in real life situations. Here it is compared with the DS8834 under identical conditions. The Transceivers drive a minicomputer Bus (flat ribbon cable) 100 feet long, terminated at the far end with taps at various lengths for connecting to the Receiver input. The cable is randomly folded to generate crosstalk between the various parts. In addition a noise pulse is induced on the signal line by driving an adjacent line with a pulse generator. This corresponds to the second dominant pulse in the Bus waveforms at approximately 600ns from the main signal pulse. As can be seen, the DS8834 with fast rise and fall times on the Driver output generates more crosstalk and its Receiver easily responds to this crosstalk and to the externally induced noise (even though it has hysteresis!), limiting the useful Bus length to less than 10 feet. In contrast, the DS3662's Driver generates much less crosstalk and its Receiver is immune to the induced noise even when the noise amplitude exceeds the signal amplitude as seen in the oscillogram at 50 feet. When the same experiment was repeated with the DS8641, it responded to the noise even at 10 feet as shown in *Figure 14*.

Figure 15 shows the plots of maximum data rate versus line length for the three Transceivers discussed above under two different conditions. The graph in *Figure 15a* is obtained with no consideration to the pulse width distortion whereas the one in *Figure 15b* is obtained for a maximum allowable pulse width distortion of ±10%. A square waveform is used so that the pulse width distortion criteria will apply to both positive and negative going pulses. These graphs clearly show that the DS3662 can be used at considerably higher data rates with lower distortion for longer distances than the other two Transceivers (*Figure 15b*) although the others have a slightly higher data rate capability at short distances with high timing distortion (*Figure 15a*).

VII. Conclusion

The DS3662, with its combination of a trapezoidal Driver and a noise rejecting Receiver utilizing on chip capacitors, represents a significant improvement in high speed Bus circuits and a solution to Bus noise problems commonly encountered in Mini and Microcomputer systems.

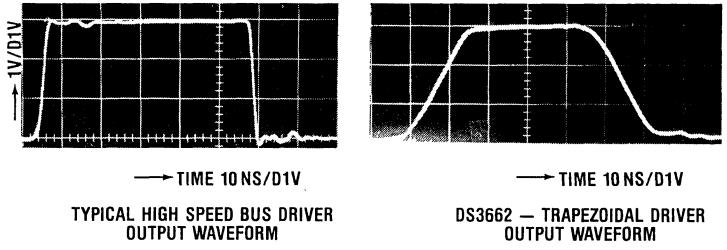


Figure 11.

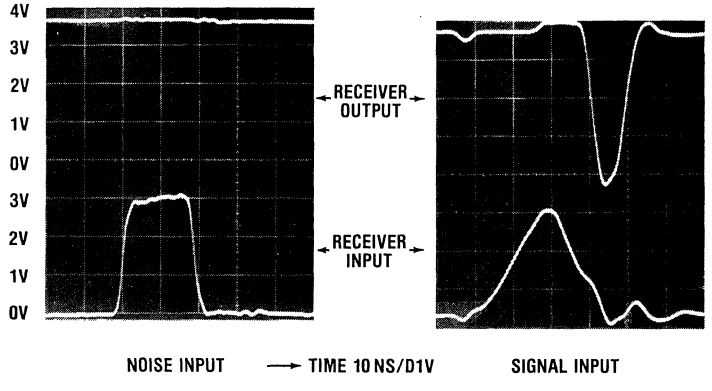


Figure 12. DS3662 Receiver Response

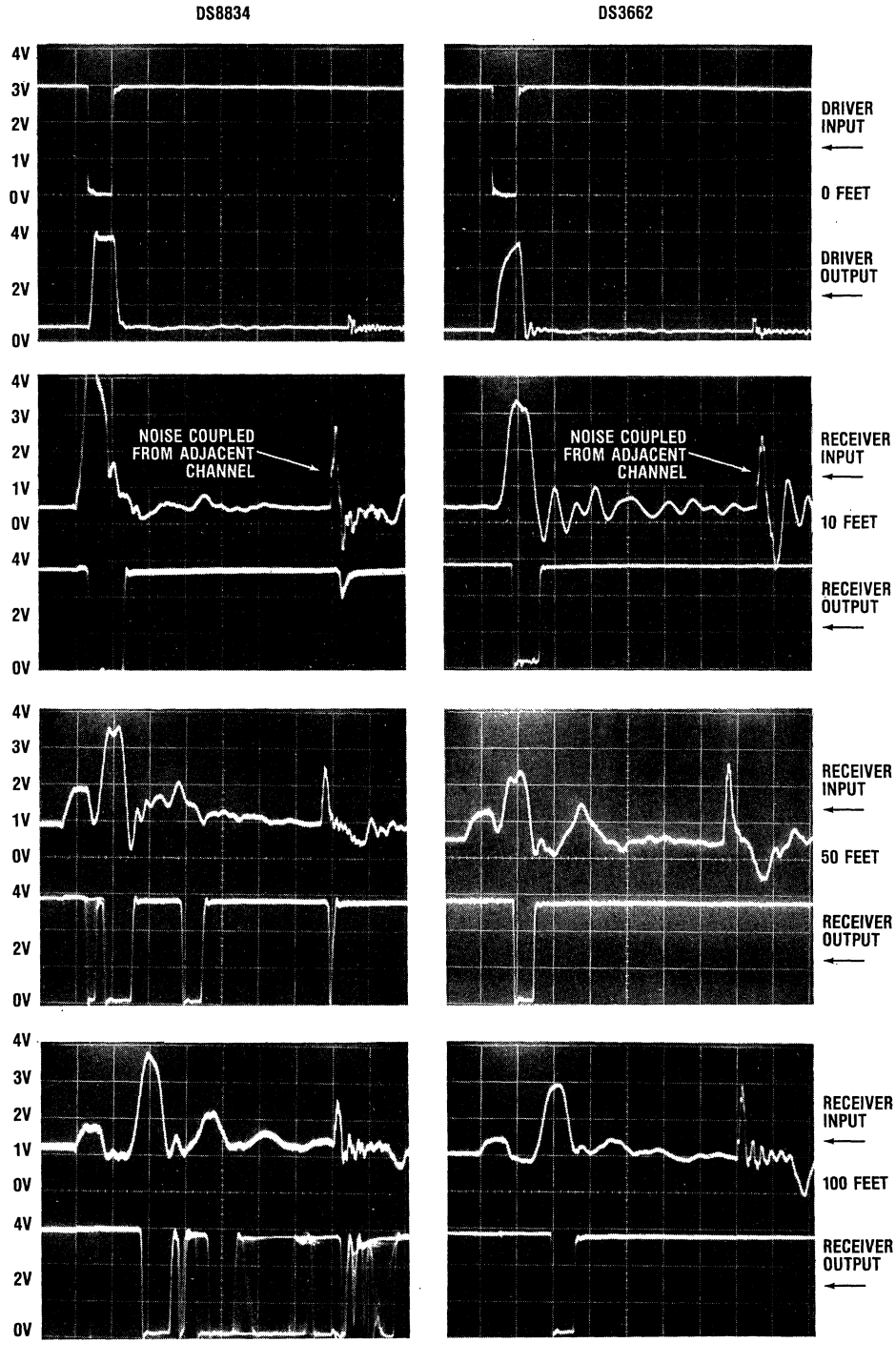

DS8834
DS3662
4V
3V
2V
1V
0V
DRIVER INPUT
0 FEET
DRIVER OUTPUT
NOISE COUPLED FROM ADJACENT CHANNEL
RECEIVER INPUT
10 FEET
RECEIVER OUTPUT
50 FEET
100 FEET
→ TIME 100 NS/DIV

Figure 13.

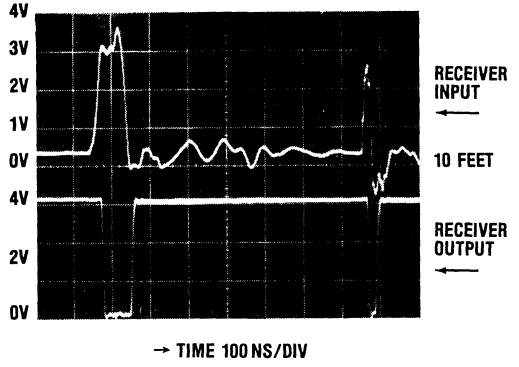


Figure 14.

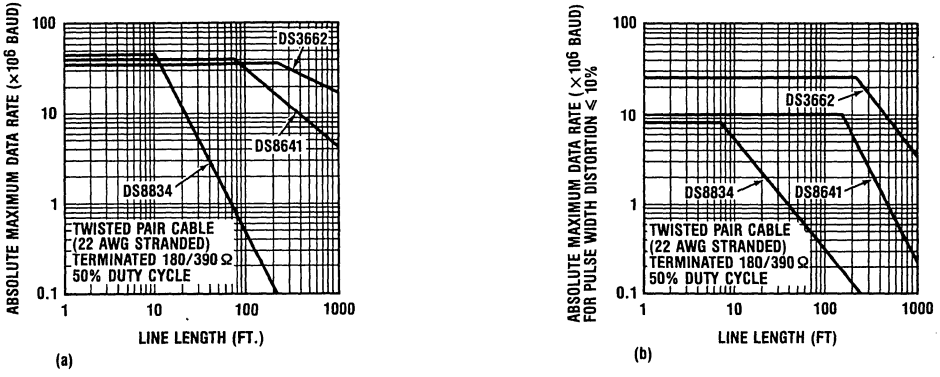


Figure 15. Data Rate vs. Line Length

AN-337

Reducing Noise on Microcomputer Buses

National Semiconductor
Application Note 337
R. V. Balakrishnan
May 1983

Abstract: *This paper focuses on the noise components that have a significant impact on the performance of a high speed microcomputer bus. An overview of their nature is followed by ways to minimize their contribution by suitable design of the PC board backplane, the termination network and the bus transceiver. The DS3662 trapezoidal bus transceiver, which is specifically designed to minimize such noise on high speed buses, is presented along with its performance data. And to conclude, some possible new transceiver designs for further improvement of the bus performance are explored.*

INTRODUCTION

As the microcomputer bus bandwidth is extended to handle ever increasing clock rates, the noise susceptibility of a single-ended bus poses a serious threat to the overall system integrity. Thus, it is mandatory that the various noise contributions be taken into account in the design of the bus transceiver, the PC board backplane and the bus terminations to avoid intermittent or total failure of the system.

Although noise such as crosstalk and reflections are inevitable in any practical bus configuration, their impact on the system can be determined and minimized by careful design of all three components mentioned above. The combined contribution of the noise under worst-case conditions should be within the noise margin for reliable bus operation.

The design of the transceiver plays a significant role in minimizing crosstalk and reflection. The bus can be optimized for minimum noise at a given bandwidth by using a trapezoidal driver having suitable rise and fall times along with a matched low pass filtered receiver which provides a symmetrical noise margin. The DS3662 is one such transceiver, the first member in the family of trapezoidal bus transceivers available from National Semiconductor Corporation. This device represents a significant improvement in high speed bus circuit design and provides a solution to commonly encountered bus noise problems.

THE MICROCOMPUTER BUS

A typical microcomputer bus usually consists of a printed circuit board backplane with signal and ground traces on one side and a ground plane on the other. The length ranges from a few inches to several feet with as many as 32 closely spaced (0.6″ typical) card edge connectors. Each signal line interacts with the ground plane to form a transmission line with characteristic impedance 'Z' in the range of 90Ω–120Ω typical. It is desirable to have as large a 'Z' as possible in order to reduce the drive requirement of the bus driver and to reduce the power dissipated at the terminations. But much larger values of 'Z' translate to significantly larger physical dimensions and therefore are not very practical.

The bus appears like a transmission line to any signal having a transition time 't_r' less than the round trip delay '$2T_L$' of the bus. The bus delay 'T_L' is given by:

$$T_L = L\sqrt{L1\ C1} \quad (1)$$

where L = length of the bus
L1 = distributed inductance per unit length
C1 = distributed capacitance per unit length

For a typical unloaded 100Ω microstrip line, C1 ≈ 20 pF/ft and L1 ≈ 0.2 μH/ft. Therefore, $T_L = 2.0$ ns/ft. This corresponds to approximately half the speed of light. However, the capacitive loading at each connector on the backplane increases the delay time significantly. The loaded delay time 'T_{LL}' is given by:

$$T_{LL} = T_L\sqrt{1 + (C_L/C1)} \quad (2)$$

where C_L = distributed load capacitance/unit length

Given a 10 pF loading at each connector (connector + transceiver capacitance) and a 0.6″ spacing between connectors, $C_L = 200$ pF/ft and $T_{LL} = 6.6$ ns/ft. So even a 6″ long bus has a $2T_{LL} = 6.6$ ns, which is higher than the transition time (t_r) of many high speed bus drivers. When in doubt, it is always better to use the transmission line approach than the lumped circuit approach as the latter is an approximation of the former. Also, the transmission line analysis gives more pessimistic (worst-case) values of crosstalk and reflection and is, hence, safer.

CROSSTALK REDUCTION

The crosstalk is due to the distributed capacitive coupling C_C and the distributed inductive coupling L_C between two lines. When crosstalk is measured on an undriven sense line next to a driven line (both terminated at their characteristic impedances), the near end crosstalk and the far end crosstalk have quite distinct features, as shown in *Figure 1*. Their respective peak amplitudes are:

$$V_{NE} = K_{NE}(2T_L)(V_I/t_r) \quad \text{for } t_r > 2T_L \quad (3)$$

$$V_{NE} = K_{NE}(V_I) \quad \text{for } t_r < 2T_L \quad (4)$$

$$V_{FE} = K_{FE}(L)(V_I/t_r) \quad (5)$$

where V_I = signal swing on the drive line.

The coupling constants are given by the expressions:

$$K_{NE} = \frac{L\,(C_C Z + L_C/Z)}{4T_L} \quad (6)$$

$$K_{FE} = \frac{C_C Z - L_C/Z}{2} \text{ ns/ft} \quad (7)$$

The near end component reduces to zero at the far end and vice versa. At any point in between, the crosstalk is a fractional sum of near and far end crosstalk waveforms shown.

It should be noted from expressions 6 and 7 that the far end crosstalk can have either polarity whereas the near end crosstalk always has the same polarity as the signal causing it. In microstrip backplanes the far end crosstalk pulse is usually the opposite polarity of the original signal.

Although the real world bus is far from the ideal situation depicted in *Figure 1*, several useful observations that apply to a general case can be made:

1. The crosstalk always scales with the signal amplitude.
2. Absolute crosstalk amplitude is proportional to slew rate V_I/t_r, not just $1/t_r$.
3. Far end crosstalk width is always t_r.
4. For $t_r < 2T_L$, the near end crosstalk amplitude V_{NE} expressed as a fraction of signal amplitude V_I is a function of physical layout only.
5. The higher the value of 't_r' the lower the percentage of crosstalk (relative to signal amplitude).

The corresponding design implications are:

1. The noise margin expressed as a percentage of the signal swing is what's important, not the absolute noise margin. Therefore, to improve noise immunity, the percentage noise margin has to be maximized. This is achieved by reducing the receiver threshold uncertainty region and by centering the threshold between the high and low levels.
2. Smaller signal amplitude with the same transition time reduces bus drive requirements without reducing noise immunity.
3. Far end crosstalk is eliminated if the receiver is designed to reject pulses having pulse widths less than or equal to t_r.
4. When $t_r < 2T_L$, the near end crosstalk immunity for a given percentage noise margin has to be built into the backplane PC layout. Since $(V_{NE}/V_I) = K_{NE}$ for this case, K_{NE} should be kept lower than the available worst-case noise margin. K_{NE} may be reduced by either increasing the spacing between lines or by introducing a ground line in between. The ground line, in addition to increasing the spacing between the signal lines, forces the electric field lines to converge on it, significantly reducing crosstalk.
5. For minimum crosstalk the rise and fall times of the signal waveform should be as large as possible consistent with the minimum pulse width requirements of the bus. A driver that automatically limits the slew rate of the transition can go a long way in reducing crosstalk.

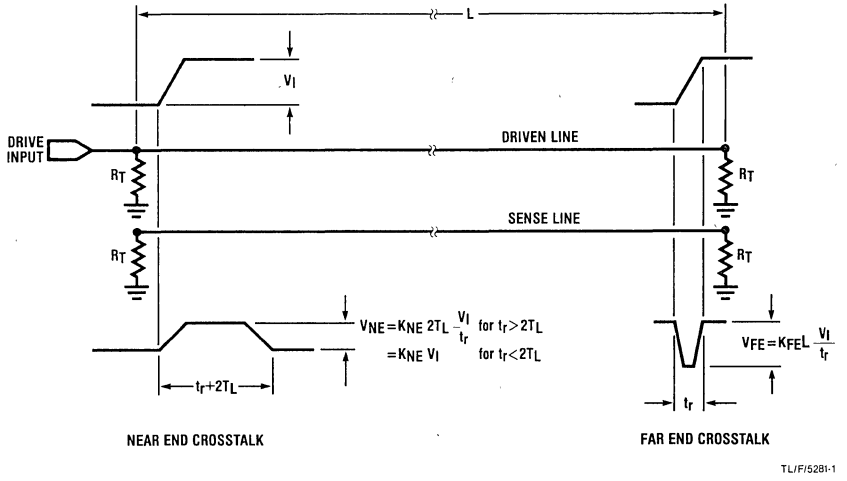


FIGURE 1. Crosstalk Under Ideal Conditions

CROSSTALK MEASUREMENT

When multiple lines on either side of the sense lines switch simultaneously the crosstalk is considerably larger, typically 3.5 times the single line switching case for microstrip backplanes. Also, the location of the drivers on the driven lines and the receiver on the sense line for worst-case crosstalk differs for the near end and far end cases as shown in *Figures 2 and 3* for a uniformly loaded bus. But if the far end crosstalk is not of the opposite polarity, then the combined effect of far end and near end crosstalk could have a larger amplitude and pulse width at a point near the middle of the sense line in *Figure 2*. So in a general case, or in the case of a non-uniformly loaded bus, it is advisable to check the sense line at several locations along the length of the bus to determine the worst-case crosstalk. The measurement should be made for both the positive and the negative transition of the drive signal.

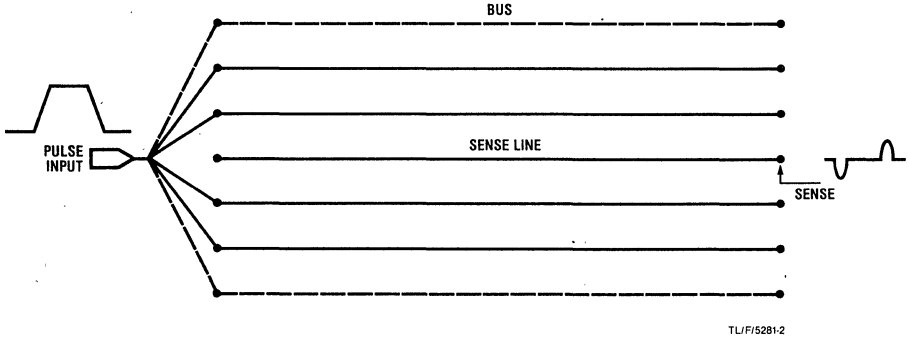
THE TERMINATION

A properly terminated transmission line has no reflections. But a practical microcomputer bus is neither a perfect transmission line nor is it properly terminated under all conditions. The capacitive loading at discrete locations, such as a used card slot, act as sources of reflection. However, in the limiting case when the bus is uniformly populated with a large number of modules, the bus behaves like a lower impedance transmission line. The loaded impedance 'Z_L' of the bus is given by the expression:

$$Z_L = \frac{Z}{\sqrt{1 + C_L/C1}} \qquad (8)$$

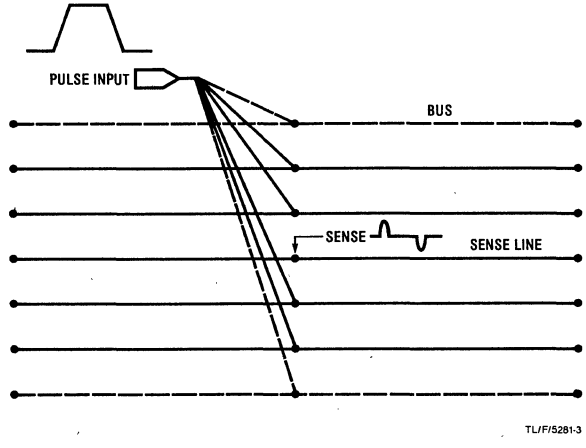
where Z = unloaded line impedance

Unfortunately, uniform loading of the bus is not guaranteed at all times and even if it were (by dummy loading of



Note: All lines terminated at both ends (not shown)

FIGURE 2. Worst-Case Far End Crosstalk Measurement



Note: All lines terminated at both ends (not shown)

FIGURE 3. Worst-Case Near End Crosstalk Measurement

the unused slots) Z_L is usually too low for proper termination of the bus. For example, a 10 pF per module loading of the 100Ω microstrip bus at 0.6" spacing results in a $Z_L = 30\Omega$. One such termination at each end will require a 200 mA drive capacity on the bus driver for a nominal 3V swing. Such large drive currents and low value terminations increase the power dissipation of the system significantly in addition to causing other problems such as increased ground drop, inductive drops in traces due to large current being switched, etc. As a compromise the bus is usually terminated at an impedance higher than Z_L but less than or equal to Z. Consequently, there is always some amount of reflection present. For a perfect transmission line the reflection coefficient 'Γ' is given by the well known expression:

$$\Gamma = \frac{Z - R_t}{Z + R_t} \tag{9}$$

where Z = impedance of the bus
R_t = termination resistance

The net effect, in the general case of a nonuniformly loaded bus, is that it may take several round trip bus delays after a bus driver output transition, before the quiescent voltage level is established. However, this delay is avoided by using a bus driver that has sufficient drive to generate a large enough voltage step during the first transition to cross well beyond the receiver threshold region under the worst-case load conditions.

Figure 4 illustrates the driver output waveform under such a condition. Here the fully loaded bus (with $Z_L = 30\Omega$), of the previous example, is driven by the DS3662 bus transceiver at the mid point. The driver is actually driving two transmission lines of $Z_L = 30\Omega$ in either direction from the middle and hence the initial step is given by:

$$V1 = \left(\frac{Z_L}{2}\right) 2I_S \tag{10}$$

where I_S = Standing current on the bus due to each termination

For the DS3662, the termination can be designed for $2I_S = 100$ mA and therefore:

$V1 = (30/2)100 = 1.5V$

This value of the initial swing is large enough to cross the narrow threshold region of the receiver as shown and therefore no waiting period is required for the reflections to build up the output high level. On the negative transition the problem is less critical due to the much higher sink capability of the DS3662 during pull down.

Reflections can also be caused by resistive loading of the bus by the DC input current of the receiver. The resulting reflection coefficient (Γ) is given by the expression:

$$\Gamma = -1/2 \left(\frac{I_R}{I_S}\right) \tag{11}$$

where I_R = receiver input current

Having a receiver with a high input impedance not only makes this component of reflection insignificant but also reduces the DC load on the driver, allowing the use of lower value termination resistors. This is particularly true when a large number of modules are connected to the bus.

The design implications of the above discussion may be summarized as follows:

1. If the driver has adequate drive to produce the necessary voltage swing under the worst-case loading ($Z_L/2$), reflections do not restrict the bus performance. This translates to a 100 mA minimum drive requirement for a typical microstrip bus.

2. If the drive is insufficient, time should be allowed for the reflections to build up the voltage level before the data is sampled.

3. For signals such as clock, strobe, etc., wherein the edge is used for triggering events, it is mandatory that the driver meet the above drive requirements if delayed or multiple triggering is to be avoided.

4. An ideal TTL bus transceiver should have at least a 100 mA drive, a high input impedance receiver with a narrow threshold uncertainty region.

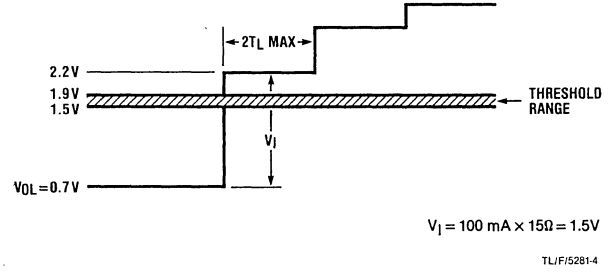


FIGURE 4. Worst-Case DS3662 Output Transition for $Z_L = 15\Omega$ and $R_T = 50\Omega$

THE DS3662 TRANSCEIVER

The DS3662 quad trapezoidal bus transceiver has been designed specifically to minimize the noise problems discussed previously. The driver generates precise trapezoidal waveforms that reduce crosstalk and the receiver uses a low pass filter to reject noise pulses having pulse widths up to the maximum driver output transition times. Precision output circuitry optimizes noise immunity without sacrificing the high data rate capability of Schottky transceivers.

Figure 5 shows the recommended configuration for microcomputer buses. The use of a 3.4V source with a single termination resistor at each end reduces the average power dissipation of the bus. However, a two resistor termination connected between the line and the power rails, having the same Thevenin's equivalent, can be substituted for lower cost.

Using a Miller integrator circuit, the driver generates a linearly rising and falling waveform with a constant slew rate of 0.2 V/ns (*Figure 7*). This corresponds to a nominal transition time of 15 ns. *Figure 6* compares the output waveform of a typical high speed driver to that of DS3662 under different load conditions. It should be noted that even under heavy loading, the regular drivers have peak slew rates that are much higher than the average. On the other hand, the trapezoidal waveform has a much lower slew rate with only a slight increase in the transition time. Such an increase in the transition time has little or no effect on the data rates. In fact, the high fidelity of the DS3662 driver output waveform allows pulse widths as low as 20 ns to be transmitted on the bus.

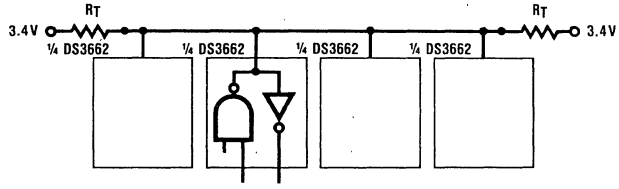
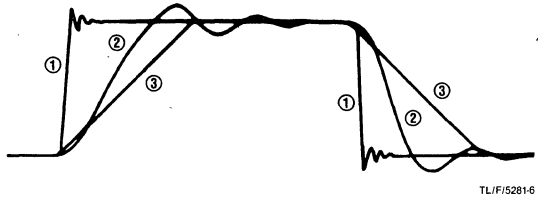


FIGURE 5. Recommended Bus Termination for Heavily Loaded Microstrip Backplanes



Note 1: Typical high speed driver output unloaded; $t_r = t_f \approx 3$ ns

Note 2: Typical high speed driver output loaded; $t_r = t_f \approx 10$ ns

Note 3: Typical output of controlled slew rate driver which is load independent; $t_r = t_f \approx 15$ ns

FIGURE 6. Waveform Comparison

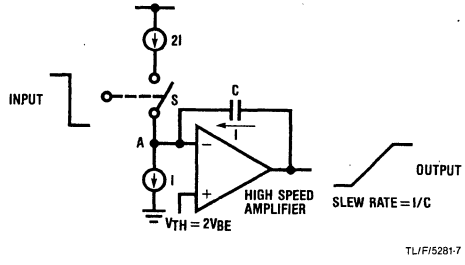


FIGURE 7. DS3662 Driver

The receiver consists of a low pass filter followed by a high speed comparator, with a typical threshold of 1.7V (*Figure 8*). The noise immunity of the receiver is specified in terms of the width of a 2.5V pulse that is guaranteed to be rejected by the receiver (*Figure 9*). The receiver typically rejects a 20 ns pulse going positive from the ground level or going negative from the 3.4V logic 1 level. The receiver threshold lies within a specified 400 mV region over the supply and temperature range and is centered between the low and high levels of the bus for a symmetrical noise margin.

Other features of the device include a 100 μA maximum DC bus loading specification under power ON or OFF condition and a glitch-free power up/down protection on the bus output.

Figure 10 shows the typical driver output waveform as compared to a standard high speed transceiver output. Oscillograms in *Figure 11* demonstrate the ability of the receiver to distinguish the trapezoidal signal from noise. Here the receiver rejects a noise pulse of 19 ns width, while accepting a narrower signal pulse (16 ns) of the same peak amplitude (the signal is triangular because of the pulse width which is smaller than the transition time).

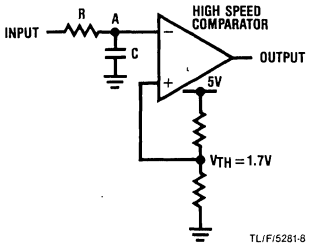
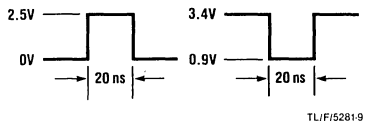


FIGURE 8. DS3662 Receiver



Rejects positive or negative going noise pulses of pulse widths up to 20 ns typical. Detects and propagates trapezoidal signal pulses in 20 ns typical.

FIGURE 9. Receiver Noise Immunity

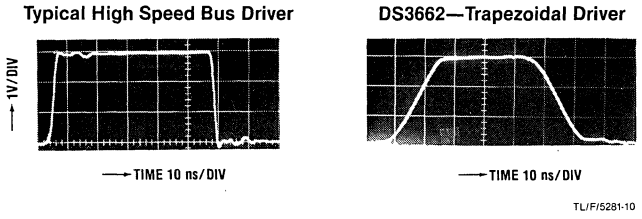


FIGURE 10. Output Waveforms

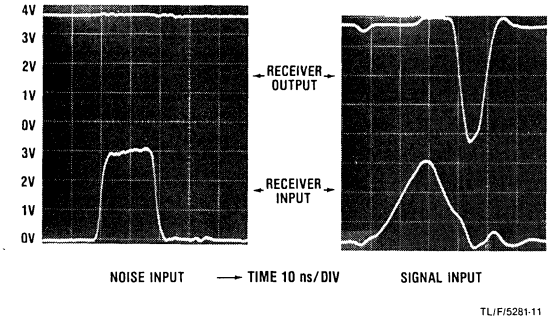


FIGURE 11. DS3662 Receiver Response

The performance of the transceiver under actual operating conditions is demonstrated in *Figure 12*. The oscillograms clearly show the capability of the DS3662 in real life situations. Here it is compared with the DS8834 under identical conditions. The transceivers drive a minicomputer bus (flat ribbon cable) 100 feet long, terminated at the far end with taps at various lengths for connecting to the receiver input. The cable is randomly folded to generate crosstalk between the various parts. In addition, a noise pulse induced on the signal line by driving an adjacent line with a pulse generator. As can be seen, the DS8834 device with fast rise and fall times on the driver output generates more crosstalk and its receiver easily responds to this crosstalk and to the externally induced noise (even though it has hysteresis!), limiting the useful length of the bus to less than 10 feet. In contrast, the DS3662's driver generates much less crosstalk and its receiver is immune to the induced noise even when the noise amplitude exceeds the signal amplitude as seen on the oscillogram at 50 feet.

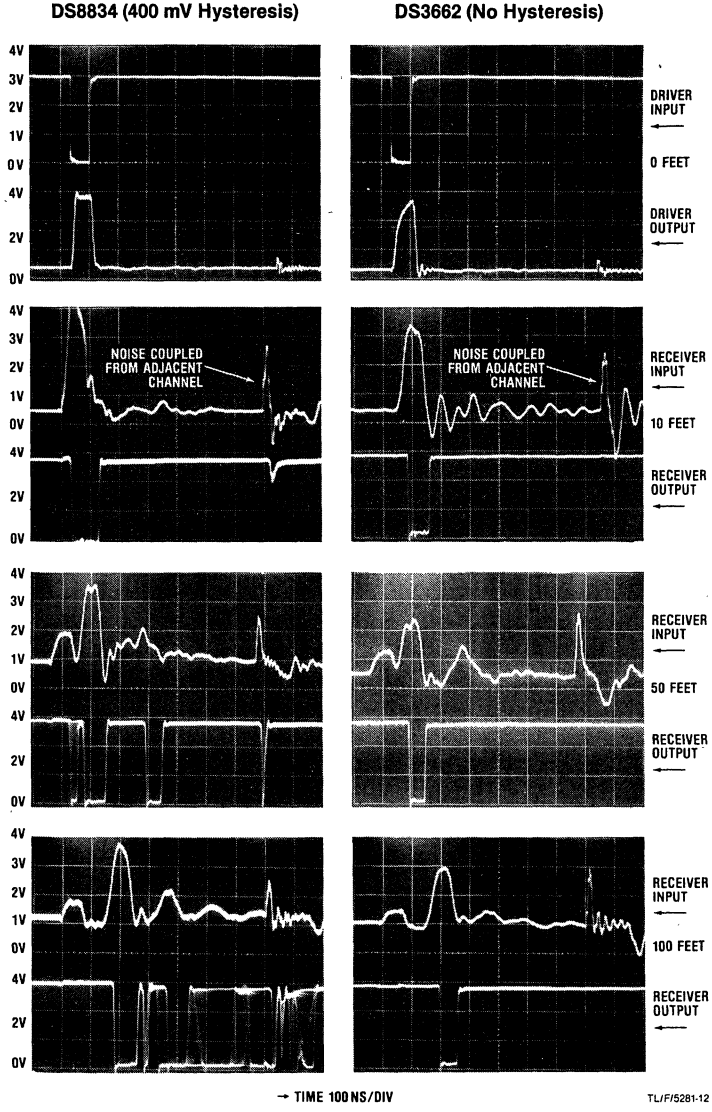


FIGURE 12. DS3662 vs Typical Schottky Transceiver—Real World Performance

WHAT NEXT?

Since crosstalk scales with the signal amplitude, reducing the signal swing has no effect on the noise immunity as long as the percentage noise margin remains the same. On the other hand, there are several advantages in having a lower signal swing. It reduces the drive current requirement of the driver thus reducing its output capacitance. Lower capacitive loading on the bus decreases its impedance reducing the drive requirement even further. Having a lower current drive not only reduces the power dissipated at the terminations but also allows better matching of the termination due to the increased line impedance. In the ideal limiting case the driver has negligible loading effect on the bus and thus allows perfect termination under all load conditions.

In practice however, there are some obvious limitations. The receiver thresholds have to be maintained within tighter limits at lower signal swings to maintain the same percentage noise margin. Also, the capacitive loading is difficult to reduce beyond a certain point, due to the diminishing return in the way of lower current rating, as the loaded bus impedance approaches the unloaded impedance. However, the capacitance of an open collector driver output can be reduced significantly by using a Schottky diode as shown in *Figure 13.* The diode isolates the driver capacitance when the output is disabled. Using reduced signal swings and precise receiver thresholds, such a transceiver can provide significant improvements in microcomputer bus performance.

CONCLUSION

A well designed bus transceiver goes a long way in improving the noise immunity of a single-ended TTL bus. Further improvements in bus performance may come from the use of reduced voltage swings and better transceiver designs for lower bus loading and tighter receiver threshold limits. Although such approaches may not be TTL compatible, the improvement in performance gained may indeed justify a new standard for bus transceivers.

REFERENCES

1) Bill Fowler, *"Transmission Line Characteristics,"* National Semiconductor—Application Note 108, May 1974

2) A. Feller, H. P. Kaupp and J. J. Digiacomo, *"Crosstalk And Reflections In High Speed Digital Systems,"* proceedings—Fall Joint Computer Conference, pp. 511-525, 1965

3) R. V. Balakrishnan, *"Bus Optimizer,"* National Semiconductor—Application Note 259, April 1981

4) David Montgomery, *"Borrowing RF Techniques For Digital Design,"* Computer Design, pp. 207-217, May 1982

5) R. V. Balakrishnan, *"Eliminating Crosstalk Over Long Distance Busing,"* Computer Design, pp. 155-162, March 1982

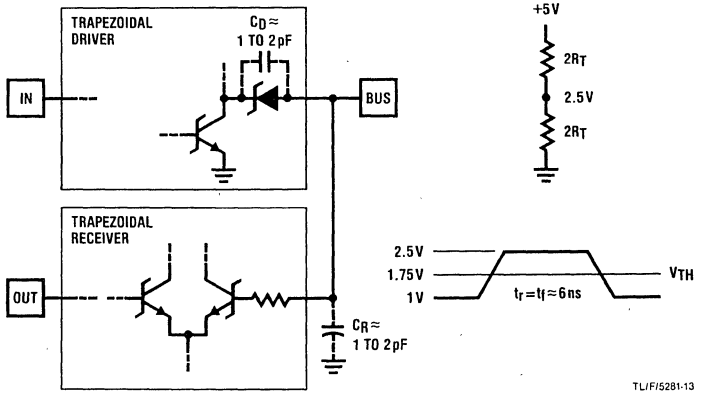


FIGURE 13. High Speed Bus Transceiver with Low Output Loading for Microcomputer Backplanes

National Semiconductor

DS3666 IEEE-488 GPIB Transceiver

General Description

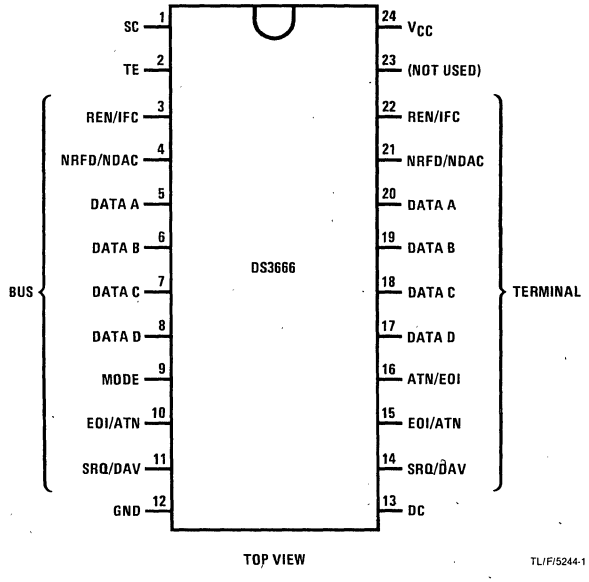
The DS3666 is a high-speed-Schottky 8-channel bi-directional transceiver designed to interface TTL/MOS logic to the IEEE Standard 488-1978 General Purpose Interface Bus. PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. The IEEE-488 required bus termination is provided internally with an active turn-off feature which disconnects the termination from the bus when V_{CC} is removed. A power up/down protection circuit is included at all bus outputs to provide glitch-free operation during V_{CC} power up or down. Implementing the IEEE-488 bus interface is accomplished by connecting two DS3666 devices together using the expansion control inputs provided. Each device is assigned to 4 data channels and 4 management signal channels to achieve the 16-line format.

Features

- 8-channel bi-directional non-inverting transceivers
- Bi-directional control implemented with TRI-STATE® output design
- Meets IEEE Standard 488-1978
- High speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- On-chip bus terminators
- No bus loading when V_{CC} is removed
- Power up/down protection (glitch-free)
- Mode control implements 2-device expansion for complete IEEE-488 interface configuration
- Accommodates multi-controller systems

Connection Diagram

Dual-In-Line Package



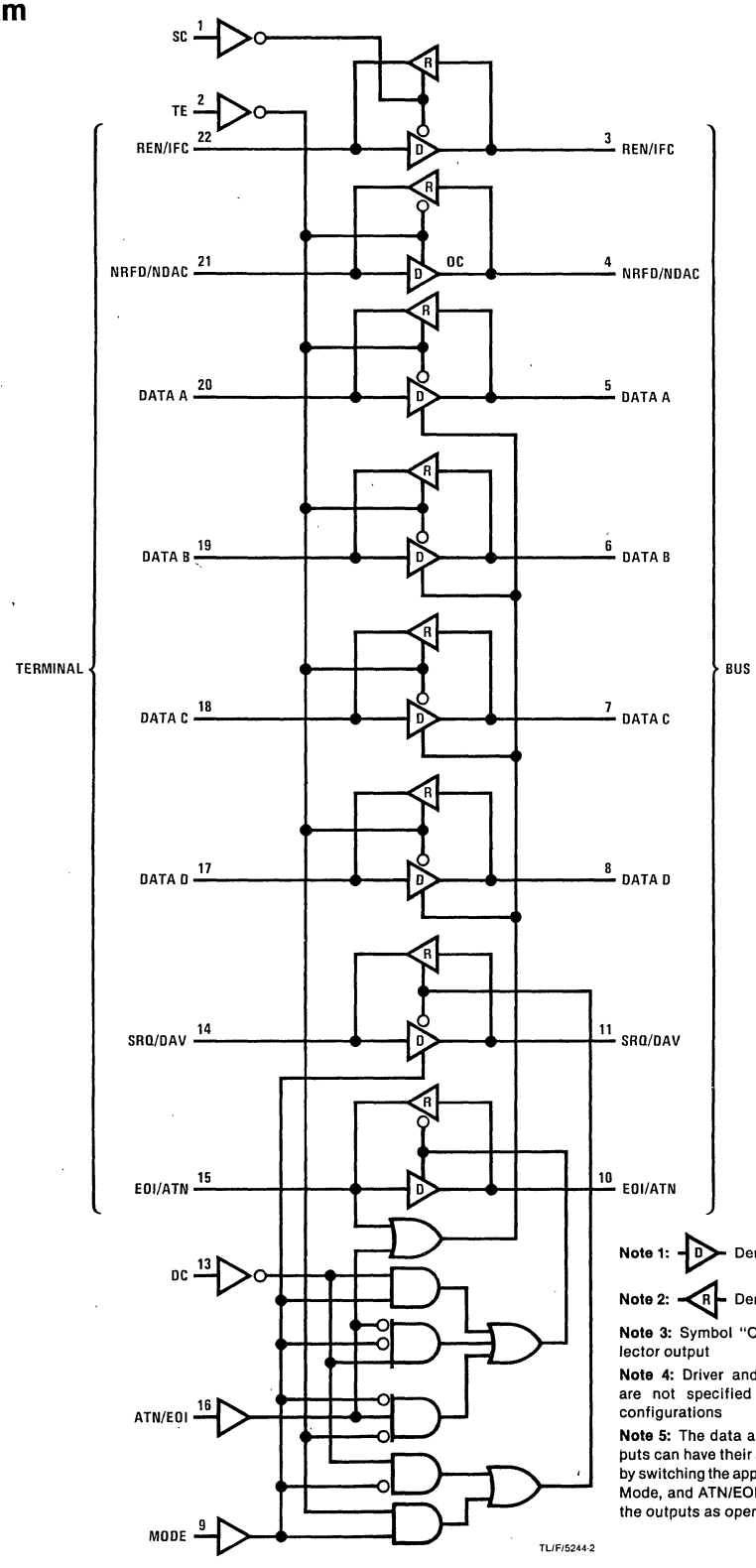
TOP VIEW

TL/F/5244-1

Order Number DS3666N
See NS Package N24C

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Logic Diagram



TL/F/5244-2

Note 1: D Denotes driver

Note 2: R Denotes receiver

Note 3: Symbol "OC" specifies open collector output

Note 4: Driver and receiver outputs that are not specified "OC" are totem-pole configurations

Note 5: The data and SRQ/DAV driver outputs can have their active pull-ups disabled by switching the appropriate inputs EOI/ATN, Mode, and ATN/EOI. This mode configures the outputs as open collector.

Device Truth Tables

TRANSCEIVER DIRECTION

Control Input Level					Transceiver Signal Direction				
Mode	SC	TE	DC	ATN/EOI	REN/IFC	NRFD/NDAC	SRQ/DAV	EOI/ATN	Data
X	H	X	X	X	T				
X	L	X	X	X	R				
X	X	H	X	X		R			T
X	X	L	X	X		T			R
H	X	H	X	X			T		
H	X	L	X	X			R		
H	X	X	H	X				R	
H	X	X	L	X				T	
L	X	X	H	X			T		
L	X	X	L	X			R		
L	X	H	X	H				T	
L	X	L	X	H				R	
L	X	X	H	L				R	
L	X	X	L	L				T	

OUTPUT CONFIGURATION

Control Input Level			Transceiver Bus Output Configuration	
Mode	ATN/EOI	EOI/ATN*	Data	SRQ/DAV
X	H	H	Totem-Pole	
X	H	L	Totem-Pole	
X	L	H	Totem-Pole	
X	L	L	Open Collector	
H	X	X		Totem-Pole
L	X	X		Open Collector

H = High level input

L = Low level input

X = Don't care

T = Transmit, i.e., signal outputted to bus

R = Receive, i.e., signal outputted to terminal

*The EOI/ATN transceiver signal level is sensed for internal logic control of bus port data output configuration

Functional Description

The DS3666 is an 8-channel bi-directional transceiver with internal logic specifically configured to implement the IEEE-488 bus interface. Expansion logic is included so that two DS3666 devices may be interconnected to form the complete 16-line interface. This approach is equivalent to pairing the DS75160A and the DS75162A devices to implement the 16-line bus. The port connections to the bus lines have internal terminators, in accordance with the IEEE-488 Standard, that are deactivated when the device is powered down. This feature guarantees no bus loading when $V_{CC} = 0V$. The bus port data outputs have a control mode that either enables or disables the active upper stage of the totem-pole configuration. When the upper stage is disabled, the data outputs operate as open collector outputs, which are necessary for parallel polling. In compliance with the system organization of the management signal lines, the NRFD/NDAC bus port output is a fixed open collector configuration. Also, the SRQ/DAV bus port output is configured so that the SRQ output is open collector in the expanded implementation of the device. Transceiver direction control is divided into three groups. The NRFD/NDAC and data lines are controlled by the TE input. The REN/IFC line is controlled by the SC input. And the EOI/ATN and SRQ/DAV lines are controlled by the TE or DC input, depending on the expansion mode. A special case is the direction of the designated EOI line, which is a function of both the TE and DC inputs, as well as the logic level present on the ATN line.

TABLE OF SIGNAL LINE ABBREVIATIONS

Signal Line Classification	Mnemonic	Definition
Control Signals	DC	Direction Control
	TE	Talk Enable
	SC	System Controller
Data I/O Ports	Data A, Data B, Data C, Data D	Bi-directional Data Transceivers
Management Signals	ATN	Attention
	DAV	Data Valid
	EOI	End or Identify
	IFC	Interface Clear
	NDAC	Not Data Accepted
	NRFD	Not Ready for Data
	REN	Remote Enable
	SRQ	Service Request

IEEE-488 Interface Configuration Truth Tables (see Configuration Diagram)

MANAGEMENT SIGNALS

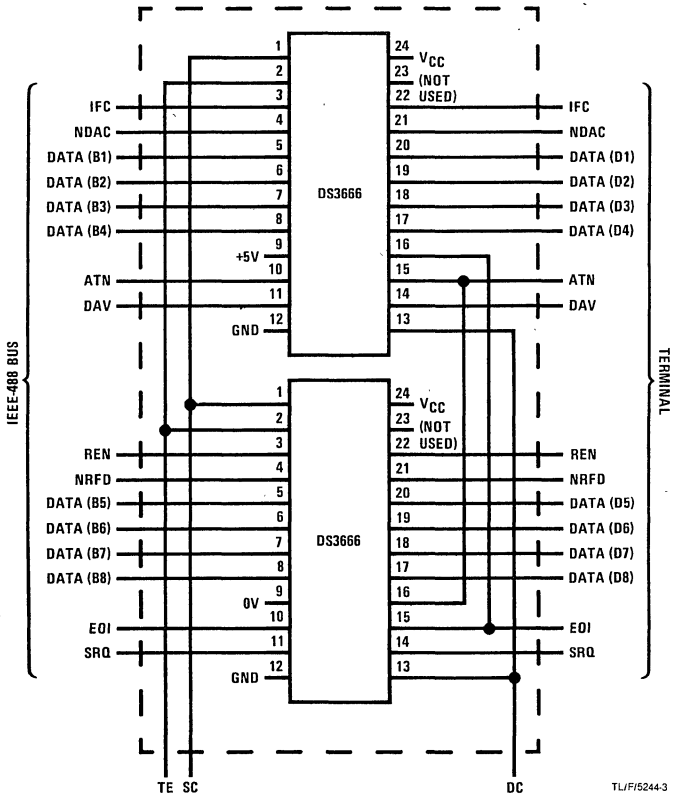
Control Input Level				Transceiver Signal Direction							
SC	TE	DC	ATN*	EOI	REN	IFC	SRQ	NRFD	NDAC	DAV	
H	H	H		R		T	T	T	R	R	T
H	H	L		T		T	T	R	R	R	T
H	L	H		R		T	T	T	T	T	R
H	L	L		T		T	T	R	T	T	R
L	H	H		R		R	R	T	R	R	T
L	H	L		T		R	R	R	R	R	T
L	L	H		R		R	R	T	T	T	R
L	L	L		T		R	R	R	T	T	R
X	H	X	H		T						
X	L	X	H		R						
X	X	H	L		R						
X	X	L	L		T						

DATA SIGNALS

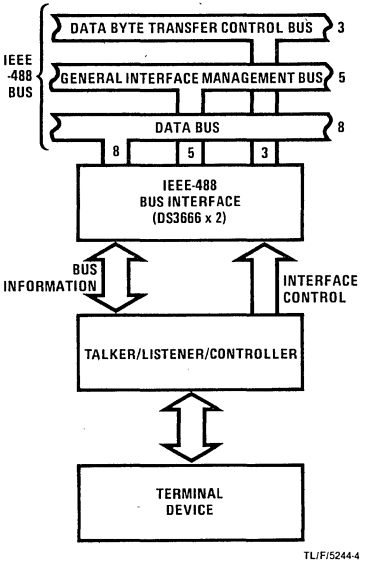
Control Input Level			Data Transceivers	
ATN	EOI	TE	Direction	Bus Port Configuration
X	X	L	R	Input
H	H	H	T	Totem-Pole Output
H	L	H	T	Totem-Pole Output
L	H	H	T	Totem-Pole Output
L	L	H	T	Open Collector Output

H = High level input
L = Low level input
X = Don't care
T = Transmit, i.e., signal outputted to bus
R = Receive, i.e., signal outputted to terminal
*The ATN signal level is sensed for internal multiplex control of EOI transmission direction logic

IEEE-488 Interface Configuration Implementation Using the DS3666



Terminal Interface Block Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Maximum Power Dissipation* at 25°C Molded Package	2005 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 16.0 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C
I_{OL}, Output Low Current: Bus		48	mA
Terminal		16	mA

Electrical Characteristics (Notes 2 and 3)

Parameter			Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage				2			V
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IK}	Input Clamp Voltage		$I_I = -18$ mA			−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus			400	500		mV
V_{OH}	High-Level Output Voltage	Terminal	$I_{OH} = -800\ \mu A$		2.7	3.5		V
		Bus (Note 5)	$I_{OH} = -5.2$ mA		2.5	3.4		
V_{OL}	Low-Level Output Voltage	Terminal	$I_{OL} = 16$ mA			0.3	0.5	V
		Bus	$I_{OL} = 48$ mA			0.4	0.5	
I_{IH}	High-Level Input Current	Terminal and Control Inputs	$V_I = 5.5V$			0.2	100	μA
			$V_I = 2.7V$			0.1	20	
I_{IL}	Low-Level Input Current		$V_I = 0.5V$			−10	−100	μA
V_{BIAS}	Terminator Bias Voltage at Bus Port	Bus	Driver Disabled	$I_{I(bus)} = 0$ (No Load)	2.5	3.0	3.7	V
I_{LOAD}	Terminator Bus Loading Current		Driver Disabled	$V_{I(bus)} = -1.5V$ to 0.4V	−1.3			mA
				$V_{I(bus)} = 0.4V$ to 2.5V	0		−3.2	
				$V_{I(bus)} = 2.5V$ to 3.7V			2.5 −3.2	
				$V_{I(bus)} = 3.7V$ to 5V	0		2.5	
				$V_{I(bus)} = 5V$ to 5.5V	0.7		2.5	
			$V_{CC} = 0$, $V_{I(bus)} = 0V$ to 2.5V				40	μA
I_{OS}	Short-Circuit Output Current	Terminal	$V_I = 2V$, $V_O = 0V$ (Note 4)		−15	−35	−75	mA
		Bus (Note 5)			−35	−75	−150	
I_{CC}	Supply Current		$V_I = 0.8V$, SC = 2.0V, TE = 2.0V, DC = 2.0V, Mode = 2.0V, ATN/EOI = 2.0V			90	135	mA
C_{IN}	Bus-Port Capacitance	Bus	$V_{CC} = 5V$ or 0V, $V_I = 0V$ to 2V, f = 1 MHz			20	30	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: This characteristic does not apply to the NRFD/NDAC bus output since it is open collector.

Switching Characteristics $V_{CC} = 5.0V \pm 5\%$, $T_A = 0°C$ to $70°C$ (Note 1)

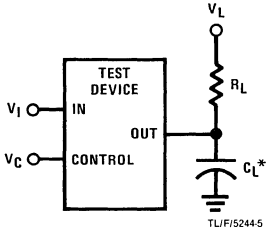
	Parameter	From	To	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time, Low to High Level Output	Terminal	Bus	$V_L = 2.3V$, $R_L = 38.3\Omega$, $C_L = 30$ pF, *Figure 1*		10	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					14	20	
t_{PLH}	Propagation Delay Time, Low to High Level Output	Bus	Terminal	$V_L = 5.0V$, $R_L = 240\Omega$, $C_L = 30$ pF, *Figure 2*		14	20	ns
t_{PHL}	Propagation Delay Time, High to Low Level Output					10	20	
t_{PZH}	Output Enable Time to High Level	Control Inputs (Note 2) (Note 3)	Bus	$V_I = 3.0V$, $V_L = 0V$, $R_L = 480\Omega$, $C_L = 15$ pF, *Figure 1*		23	40	ns
t_{PHZ}	Output Disable Time from High Level					15	27	
t_{PZL}	Output Enable Time to Low Level			$V_I = 0V$, $V_L = 2.3V$, $R_L = 38.3\Omega$, $C_L = 15$ pF, *Figure 1*		28	48	ns
t_{PLZ}	Output Disable Time from Low Level					17	35	
t_{PZH}	Output Enable Time to High Level	Control Inputs (Note 2) (Note 3)	Terminal	$V_I = 3.0V$, $V_L = 0V$, $R_L = 3\ k\Omega$, $C_L = 15$ pF, *Figure 1*		18	45	ns
t_{PHZ}	Output Disable Time from High Level					22	33	
t_{PZL}	Output Enable Time to Low Level			$V_I = 0V$, $V_L = 5V$, $R_L = 280\Omega$, $C_L = 15$ pF, *Figure 1*		28	56	ns
t_{PLZ}	Output Disable Time from Low Level					20	35	
t_{PZH}	Output Pull-Up Enable Time	ATN/EOI Input (Note 2)	Bus Data Outputs	$V_I = 3V$, $V_L = 0V$, $R_L = 480\Omega$, $C_L = 15$ pF, *Figure 1*		10	20	ns
t_{PHZ}	Output Pull-Up Disable Time					10	20	

Note 1: Typical values are for $V_{CC} = 5.0V$ and $T_A = 25°C$ and are meant for reference only.

Note 2: Refer to functional truth table for control input definition.

Note 3: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

Switching Load Configurations

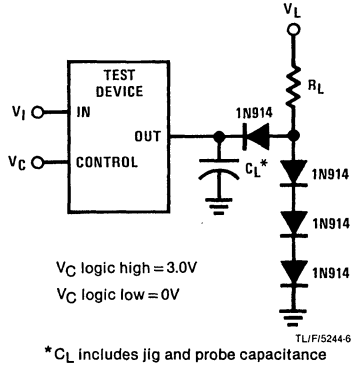


V_C logic high = 3.0V

V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 1



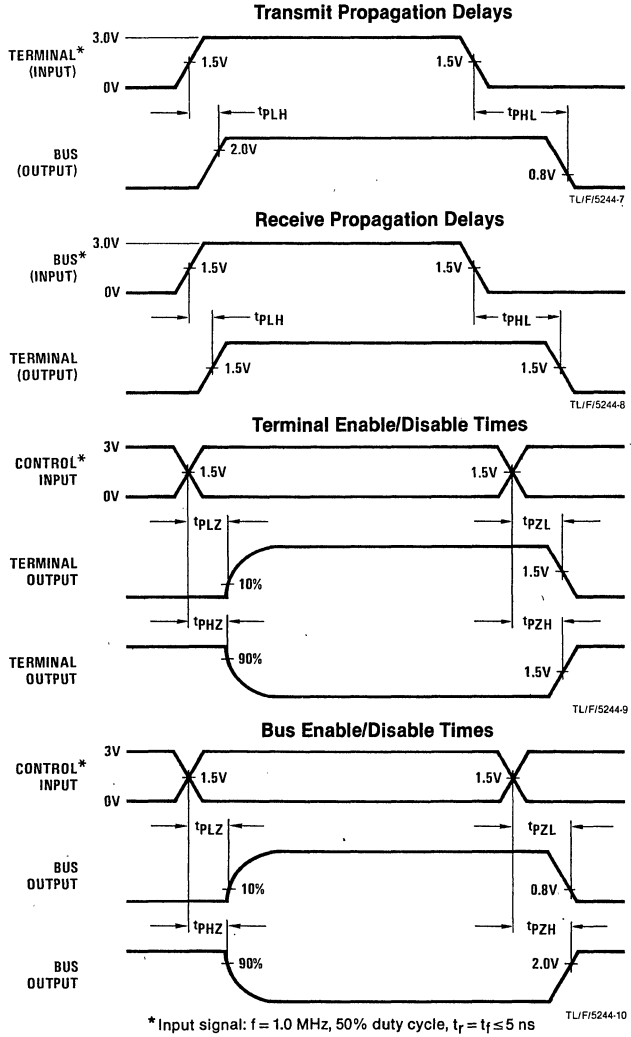
V_C logic high = 3.0V

V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 2

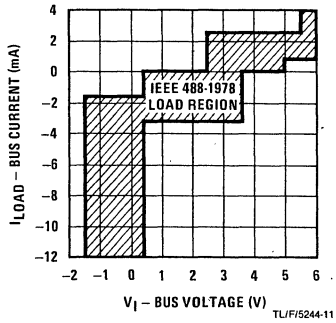
Switching Waveforms



*Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns

Performance Characteristics

Bus Port Load Characteristic



Refer to Electrical Characteristics Table

IEEE-488 Specification Summary

Logic Nomenclature. When referring to the IEEE-488 specification publication, the following logic conventions are used:

1) A "true" condition corresponds to a logic low signal level.
2) A "false" condition corresponds to a logic high signal level.

Bus Specification. The IEEE-488 bus is comprised of 16 signal lines intended for digital data exchange at a maximum rate of 1 Mbaud and for a maximum transmission path length of 20 meters.

Terminal Devices. The IEEE-488 bus will support a maximum of 15 interconnected devices. These devices may be configured in four different modes of operation:

1) Talk only (e.g., counter)
2) Listen only (e.g., printer)
3) Listen and talk (e.g., multimeter)
4) Listen, talk, and control (e.g., calculator)

Data Bus. The data bus has 8 signal lines, denoted DIO_1 through DIO_8. These lines carry data and interface messages in a bi-directional asynchronous, bit parallel, byte serial form.

Data Byte Transfer Control Bus. These 3 signal lines are used to control the transfer of data bytes across the data bus lines.

1) NRFD (Not Ready for Data). This signal originates from a listen device and indicates to a talker that a listen device is not ready to accept data.
2) DAV (Data Valid). This signal originates from a talker device and indicates to a listen device that data present on the data bus is valid.
3) NDAC (Not Data Accepted). This signal originates from a listen device and indicates to a talker device that data on the data bus has not been accepted.

General Interface Management Bus. These 5 signal lines provide general management of all bus operations.

1) ATN (Attention). This signal originates from a controller device and indicates to other devices on the bus how the data bus information is to be interpreted.
2) IFC (Interface Clear). This signal originates from a controller device and causes all interface logic to be set to a known state.
3) REN (Remote Enable). This signal originates from a controller device and is used in conjunction with other messages to tell a remote device which of two sources of information is to be used. The source is designated as being remote or local.
4) SRQ (Service Request). This signal is generated by a remote device to indicate to the controller device a need for attention.
5) EOI (End or Identify). This signal is generated by a talker device to indicate the end of a multibyte transfer. This signal may also originate from a controller, in conjunction with ATN to execute a polling sequence.

National Semiconductor

DS3667 TRI-STATE® Bidirectional Transceiver

General Description

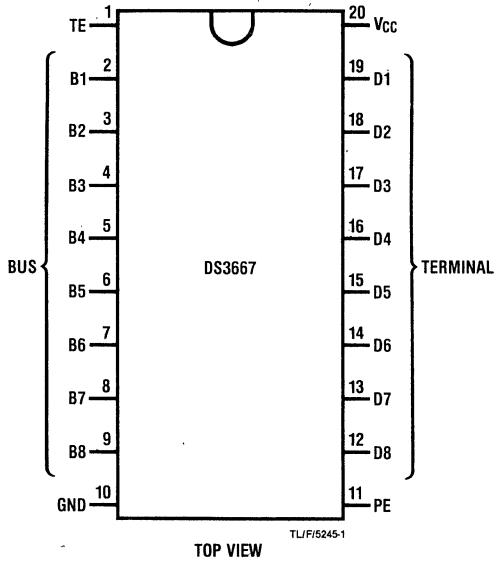
The DS3667 is a high speed Schottky 8-channel bidirectional transceiver designed for digital information and communication systems. Pin selectable totem-pole/open collector outputs are provided at all driver outputs. This feature, together with the Dumb Mode which puts both driver and receiver outputs in TRI-STATE at the same time, means higher flexibility of system design. PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. A power up/down protection circuit is included at all outputs to provide glitch-free operation during V_{CC} power up or down.

Features

- 8-channel bidirectional non-inverting transceivers
- Bidirectional control implemented with TRI-STATE output design
- High speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- Pin selectable totem-pole/open collector outputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- Power up/down protection (glitch-free)
- Dumb Mode capability

Connection Diagram

Dual-In-Line Package

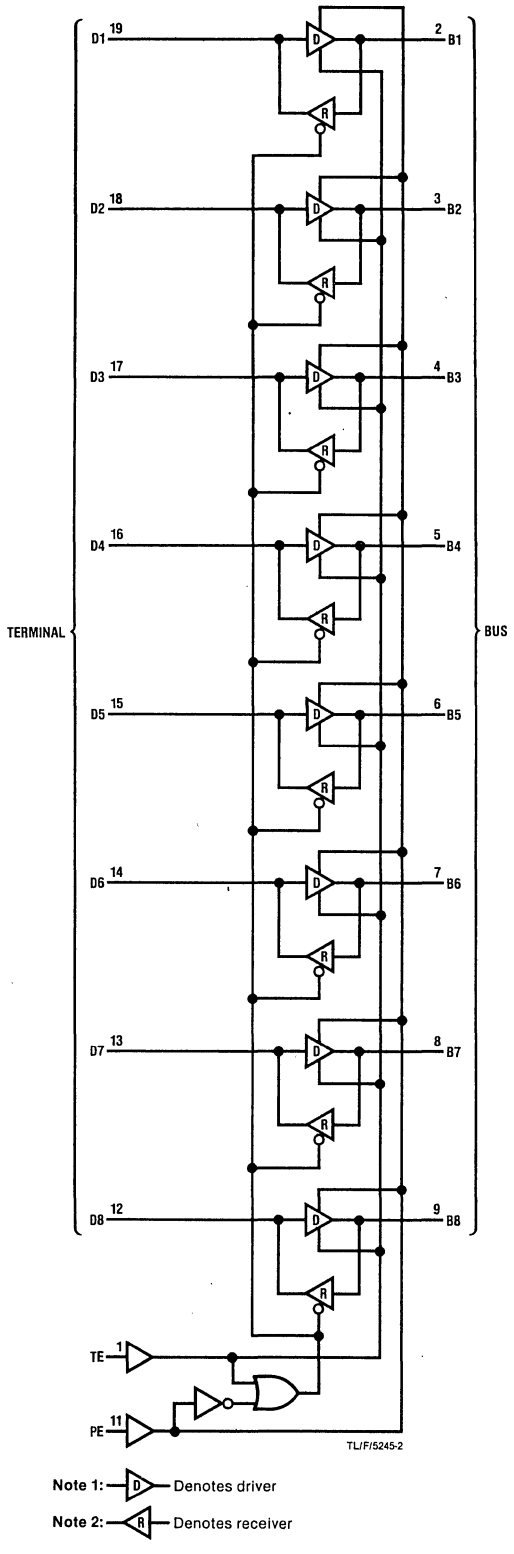


TOP VIEW

Order Number DS3667N
See NS Package N20A

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Logic Diagram



Note 1: D — Denotes driver

Note 2: R — Denotes receiver

Functional Truth Table

Control Input Level		Data Transceivers		
TE	PE	Mode	Bus Port	Terminal Port
H	H	T	Totem-Pole Output	Input
H	L	T	Open Collector Output	Input
L	H	R	Input	Output
L	L	D	TRI-STATE	TRI-STATE

H: High Level Input
L: Low Level Input
T: Transmitting Mode
R: Receiving Mode
D: Dumb Mode

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1832 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 14.7 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C
I_{OL}, Output Low Current			
Bus		48	mA
Terminal		16	mA

Electrical Characteristics (Notes 2 and 3)

Parameter			Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{IK}	Input Clamp Voltage		$I_I = -18$ mA		−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus		400	500		mV
V_{OH}	High Level Output Voltage	Terminal	$I_{OH} = -800\ \mu A$	2.7	3.5		V
		Bus	$I_{OH} = -5.2$ mA	2.5	3.4		
V_{OL}	Low Level Output Voltage	Terminal	$I_{OL} = 16$ mA		0.3	0.5	V
		Bus	$I_{OL} = 48$ mA		0.4	0.5	
I_{IH}	High Level Input Current	TE, PE	$V_I = 5.5V$		0.2	100	μA
			$V_I = 2.7V$		0.1	20	
		Terminal and Bus	$V_I = 4V$			200	
I_{IL}	Low Level Input Current	Terminal and TE, PE	$V_I = 0.5V$		−10	−100	μA
		Bus			−0.4	−1.0	mA
I_{OS}	Short Circuit Output Current	Terminal	$V_I = 2V$, $V_O = 0V$ (Note 4)	−15	−35	−75	mA
		Bus		−50	−120	−200	
I_{CC}	Supply Current		Transmit, TE = 2V, PE = 2V, $V_I = 0.8V$		75	100	mA
			Receive, TE = 0.8V, PE = 2V, $V_I = 0.8V$		65	90	
C_{IN}	Bus-Port Capacitance	Bus	$V_{CC} = 0V$, $V_I = 0V$, f = 10 kHz (Note 5)		20	30	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: This parameter is guaranteed by design. It is not a tested parameter.

Switching Characteristics $V_{CC} = 5.0V \pm 5\%$, $T_A = 0°C$ to $70°C$ (Note 1)

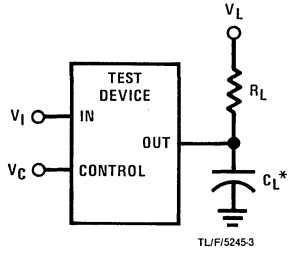
Parameter	From	To	Conditions	Min	Typ	Max	Units
t_{PLH} Propagation Delay Time, Low to High Level Output	Terminal	Bus	$V_L = 2.3V$, $R_L = 38.3\Omega$, $C_L = 30$ pF, *Figure 1*		10	20	ns
t_{PHL} Propagation Delay Time, High to Low Level Output					14	20	ns
t_{PLH} Propagation Delay Time, Low to High Level Output	Bus	Terminal	$V_L = 5.0V$, $R_L = 240\Omega$, $C_L = 30$ pF, *Figure 2*		15	20	ns
t_{PHL} Propagation Delay Time, High to Low Level Output					10	20	ns
t_{PZH} Output Enable Time to High Level	TE (Note 2) (Note 3)	Bus	$V_I = 3.0V$, $V_L = 0V$, $R_L = 480\Omega$, $C_L = 15$ pF, *Figure 1*		19	30	ns
t_{PHZ} Output Disable Time from High Level					15	20	ns
t_{PZL} Output Enable Time to Low Level			$V_I = 0V$, $V_L = 2.3V$, $R_L = 38.3\Omega$, $C_L = 15$ pF, *Figure 1*		24	40	ns
t_{PLZ} Output Disable Time from Low Level					17	30	ns
t_{PZH} Output Enable Time to High Level	TE, PE (Note 2) (Note 3)	Terminal	$V_I = 3.0V$, $V_L = 0V$, $R_L = 3$ kΩ, $C_L = 15$ pF, *Figure 1*		19	35	ns
t_{PHZ} Output Disable Time from High Level					17	25	ns
t_{PZL} Output Enable Time to Low Level			$V_I = 0V$, $V_L = 5V$, $R_L = 280\Omega$, $C_L = 15$ pF, *Figure 1*		27	40	ns
t_{PLZ} Output Disable Time from Low Level					17	30	ns
t_{PZH} Output Pull-Up Enable Time	PE (Note 2)	Bus	$V_I = 3V$, $V_L = 0V$, $R_L = 480\Omega$, $C_L = 15$ pF, *Figure 1*		10	20	ns
t_{PHZ} Output Pull-Up Disable Time					10	20	ns

Note 1: All typical values are for $T_A = 25°C$, $V_{CC} = 5V$.

Note 2: Refer to Functional Truth Table for control input definition.

Note 3: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

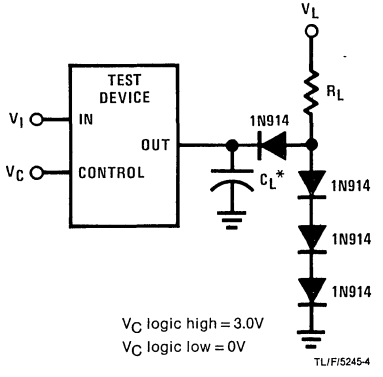
Switching Load Configurations



V_C logic high = 3.0V
V_C logic low = 0V

* C_L includes jig and probe capacitance

FIGURE 1



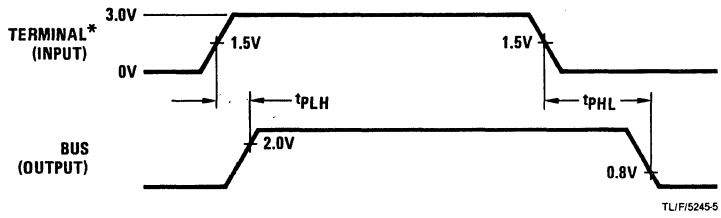
V_C logic high = 3.0V
V_C logic low = 0V

* C_L includes jig and probe capacitance

FIGURE 2

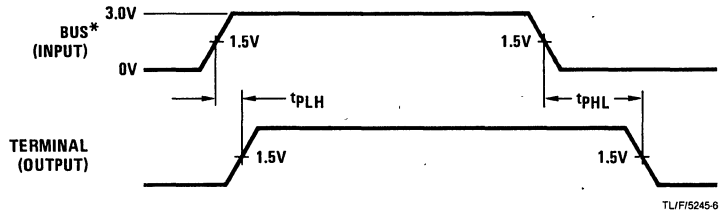
Switching Waveforms

Transmit Propagation Delays



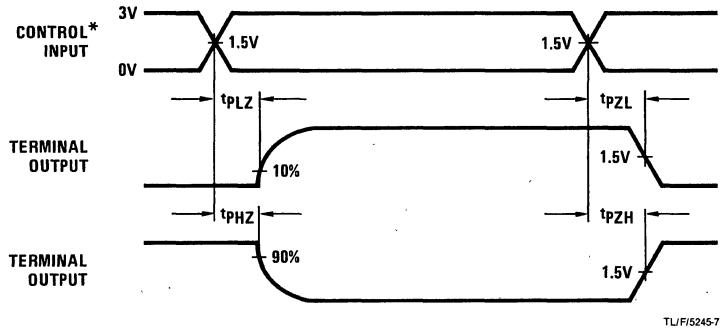
TL/F/5245-5

Receive Propagation Delays



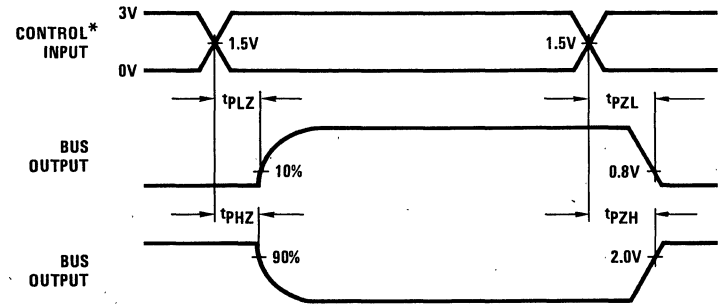
TL/F/5245-6

Terminal Enable/Disable Times



TL/F/5245-7

Bus Enable/Disable Times



TL/F/5245-8

* Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns

National Semiconductor

Bus Transceivers

DS75160A/DS75161A/DS75162A IEEE-488 GPIB Transceivers

General Description

This family of high-speed-Schottky 8-channel bi-directional transceivers is designed to interface TTL/MOS logic to the IEEE Standard 488-1978 General Purpose Interface Bus (GPIB). PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. The IEEE-488 required bus termination is provided internally with an active turn-off feature which disconnects the termination from the bus when V_{CC} is removed. A power up/down protection circuit is included at all bus outputs to provide glitch-free operation during V_{CC} power up or down.

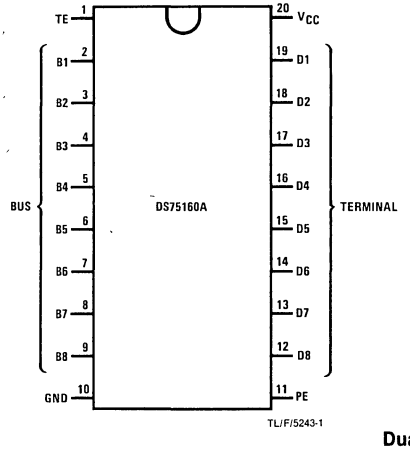
The General Purpose Interface Bus is comprised of 16 signal lines—8 for data and 8 for interface management. The data lines are always implemented with DS75160A, and the management lines are either implemented with DS75161A in a single-controller system, or with DS75162A in a multi-controller system.

Features

- 8-channel bi-directional non-inverting transceivers
- Bi-directional control implemented with TRI-STATE® output design
- Meets IEEE Standard 488-1978
- High-speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- On-chip bus terminators
- No bus loading when V_{CC} is removed
- Power up/down protection (glitch-free)
- Pin selectable open collector mode on DS75160A driver outputs
- Accommodates multi-controller systems

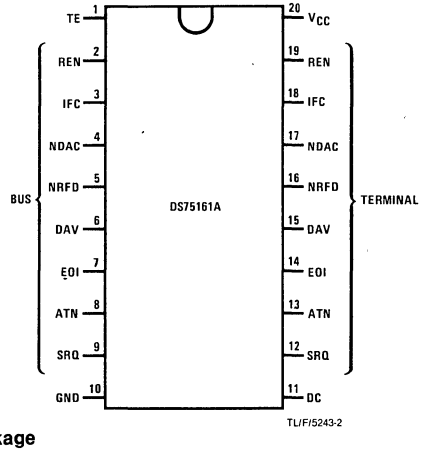
Connection Diagrams (Top Views)

Dual-In-Line Package



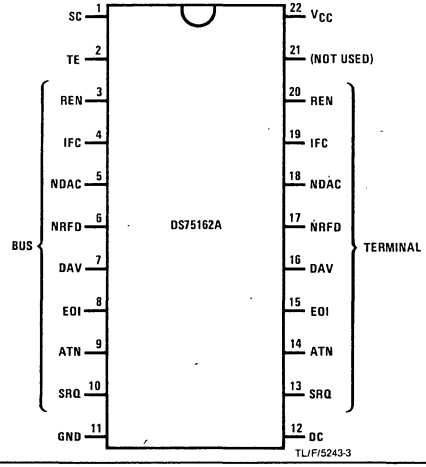
TL/F/5243-1

Dual-In-Line Package



TL/F/5243-2

Dual-In-Line Package



TL/F/5243-3

Order Number DS75160AN, DS75161AN or DS75162AN
See NS Package N20A or N22A

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Functional Description

DS75160A

This device is an 8-channel bi-directional transceiver with one common direction control input, denoted TE. When used to implement the IEEE-488 bus, this device is connected to the eight data bus lines, designated DIO_1–DIO_8. The port connections to the bus lines have internal terminators, in accordance with the IEEE-488 Standard, that are deactivated when the device is powered down. This feature guarantees no bus loading when $V_{CC} = 0V$. The bus port outputs also have a control mode that either enables or disables the active upper stage of the totem-pole configuration. When this control input, denoted PE, is in the high state, the bus outputs operate in the high-speed totem-pole mode. When PE is in the low state, the bus outputs operate as open collector outputs which are necessary for parallel polling.

DS75161A

This device is also an 8-channel bi-directional transceiver which is specifically configured to implement the eight management signal lines of the IEEE-488 bus. This device, paired with the DS75160A, forms the complete 16-line interface between the IEEE-488 bus and a single controller instrumentation system. In compliance with the system organization of the management signal lines, the SRQ, NDAC, and NRFD bus port outputs are open collector. In contrast to the DS75160A, these open collector outputs are a fixed configuration. The direction control is divided into three groups. The DAV, NDAC, and NRFD transceiver directions are controlled by the TE input. The ATN, SRQ, REN, and IFC transceiver directions are controlled by the DC input. The EOI transceiver direction is a function of both the TE and DC inputs, as well as the logic level present on the ATN channel. The port connections to the bus lines have internal terminators identical to the DS75160A.

DS75162A

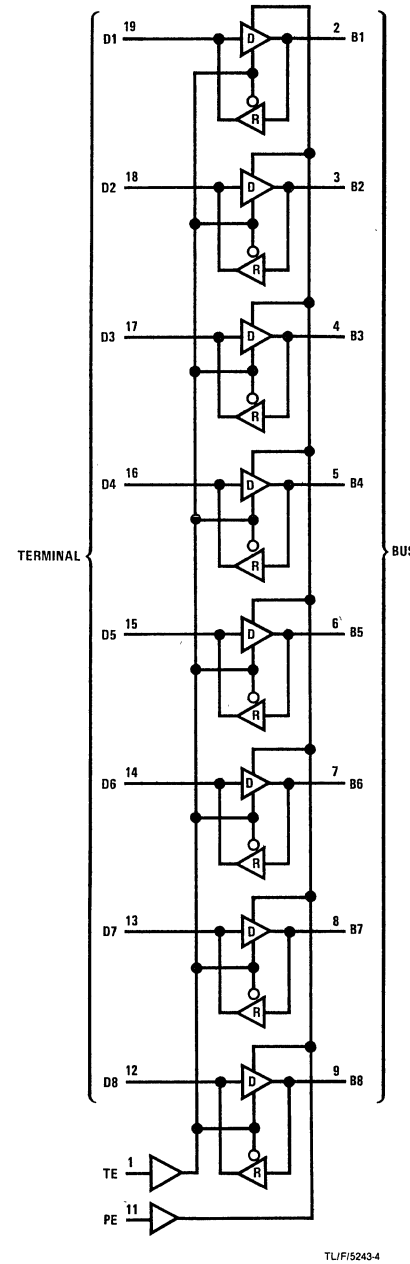
This device is identical to the DS75161A, except that an additional direction control input is provided, denoted SC. The SC input controls the direction of the REN and IFC transceivers that are normally controlled by the DC input on the DS75161A. This additional control function is instrumental in implementing multiple controller systems.

TABLE OF SIGNAL LINE ABBREVIATIONS

Signal Line Classification	Mnemonic	Definition	Device
Control Signals	DC	Direction Control	DS75161A/DS75162A
	PE	Pull-Up Enable	DS75160A
	TE	Talk Enable	All
	SC	System Controller	DS75162A
Data I/O Ports	B1–B8	Bus Side of Device	DS75160A
	D1–D8	Terminal Side of Device	
Management Signals	ATN	Attention	DS75161A/DS75162A
	DAV	Data Valid	
	EOI	End or Identify	
	IFC	Interface Clear	
	NDAC	Not Data Accepted	
	NRFD	Not Ready for Data	
	REN	Remote Enable	
	SRQ	Service Request	

Logic Diagrams

DS75160A



TL/F/5243-4

Note 1: Denotes driver

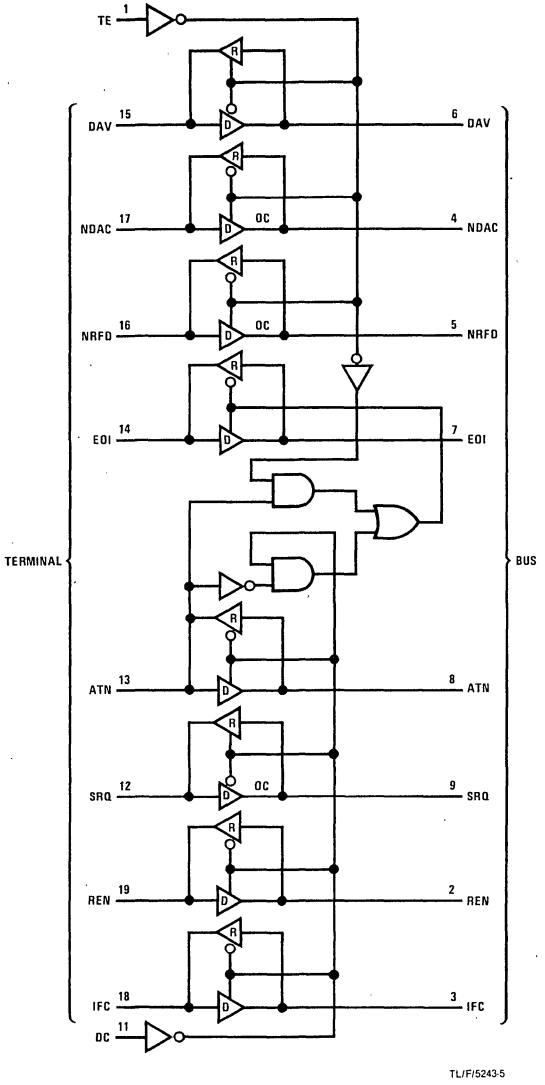
Note 2: Denotes receiver

Note 3: Driver and receiver outputs are totem-pole configurations

Note 4: The driver outputs of DS75160A can have their active pull-ups disabled by switching the PE input (pin 11) to the logic low state. This mode configures the outputs as open collector.

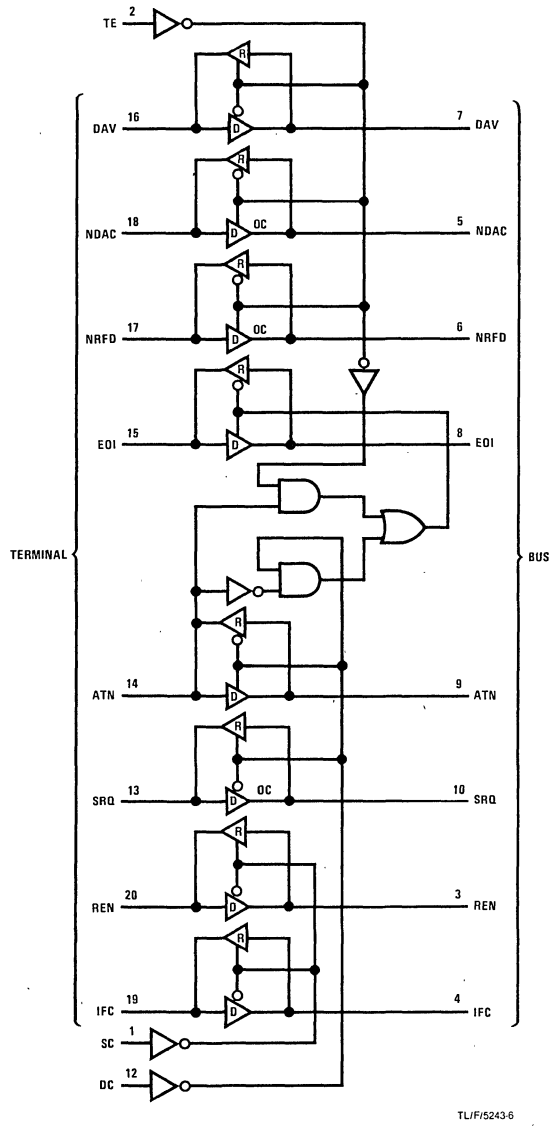
Logic Diagrams (Continued)

DS75161A



TL/F/5243-5

DS75162A



TL/F/5243-6

Note 1: Denotes driver

Note 2: Denotes receiver

Note 3: Symbol "OC" specifies open collector output

Note 4: Driver and receiver outputs that are not specified "OC" are totem-pole configurations

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1897 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C
I_{OL}, Output Low Current			
Bus		48	mA
Terminal		16	mA

*Derate molded package 15.2 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

Parameter			Conditions		Min	Typ	Max	Units
V_{IH}	High-Level Input Voltage				2			V
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IK}	Input Clamp Voltage		$I_I = -18$ mA			−0.8	−1.5	V
V_{HYS}	Input Hysteresis	Bus			400	500		mV
V_{OH}	High-Level Output Voltage	Terminal	$I_{OH} = -800\ \mu A$		2.7	3.5		V
		Bus (Note 5)	$I_{OH} = -5.2$ mA		2.5	3.4		
V_{OL}	Low-Level Output Voltage	Terminal	$I_{OL} = 16$ mA			0.3	0.5	V
		Bus	$I_{OL} = 48$ mA			0.4	0.5	
I_{IH}	High-Level Input Current	Terminal and TE, PE, DC, SC Inputs	$V_I = 5.5V$			0.2	100	μA
			$V_I = 2.7V$			0.1	20	
I_{IL}	Low-Level Input Current		$V_I = 0.5V$			−10	−100	μA
V_{BIAS}	Terminator Bias Voltage at Bus Port	Bus	Driver Disabled	$I_{I(bus)} = 0$ (No Load)	2.5	3.0	3.7	V
I_{LOAD}	Terminator Bus Loading Current		Driver Disabled	$V_{I(bus)} = -1.5V$ to 0.4V	−1.3			mA
				$V_{I(bus)} = 0.4V$ to 2.5V	0		−3.2	
				$V_{I(bus)} = 2.5V$ to 3.7V			2.5 −3.2	
				$V_{I(bus)} = 3.7V$ to 5V	0		2.5	
				$V_{I(bus)} = 5V$ to 5.5V	0.7		2.5	
			$V_{CC} = 0$, $V_{I(bus)} = 0V$ to 2.5V				40	μA
I_{OS}	Short-Circuit Output Current	Terminal	$V_I = 2V$, $V_O = 0V$ (Note 4)		−15	−35	−75	mA
		Bus (Note 5)			−35	−75	−150	
I_{CC}	Supply Current	DS75160A	Transmit, TE = 2V, PE = 2V, $V_I = 0.8V$			85	125	mA
			Receive, TE = 0.8V, PE = 2V, $V_I = 0.8V$			70	100	
		DS75161A	TE = 0.8V, DC = 0.8V, $V_I = 0.8V$			84	125	
		DS75162A	TE = 0.8V, DC = 0.8V, SC = 2V, $V_I = 0.8V$			85	125	
C_{IN}	Bus-Port Capacitance	Bus	$V_{CC} = 5V$ or 0V, $V_I = 0V$ to 2V, f = 1 MHz			20	30	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: This characteristic does not apply to outputs on DS75161A and DS75162A that are open collector.

Switching Characteristics $V_{CC} = 5.0V \pm 5\%$, $T_A = 0°C$ to $70°C$ (Note 1)

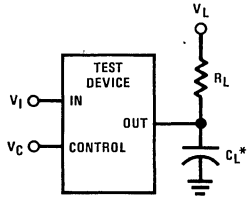
Parameter	From	To	Conditions	DS75160A			DS75161A			DS75162A			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{PLH} Propagation Delay Time, Low to High Level Output	Terminal	Bus	$V_L = 2.3V$, $R_L = 38.3\Omega$, $C_L = 30$ pF, *Figure 1*		10	20		10	20		10	20	ns
t_{PHL} Propagation Delay Time, High to Low Level Output					14	20		14	20		14	20	ns
t_{PLH} Propagation Delay Time, Low to High Level Output	Bus	Terminal	$V_L = 5.0V$, $R_L = 240\Omega$, $C_L = 30$ pF, *Figure 2*		14	20		14	20		14	20	ns
t_{PHL} Propagation Delay Time, High to Low Level Output					10	20		10	20		10	20	ns
t_{PZH} Output Enable Time to High Level	TE, DC, or SC (Note 2) (Note 3)	Bus	$V_I = 3.0V$, $V_L = 0V$, $R_L = 480\Omega$, $C_L = 15$ pF, *Figure 1*		19	32		23	40		23	40	ns
t_{PHZ} Output Disable Time from High Level					15	22		15	25		15	25	ns
t_{PZL} Output Enable Time to Low Level			$V_I = 0V$, $V_L = 2.3V$, $R_L = 38.3\Omega$, $C_L = 15$ pF, *Figure 1*		24	35		28	48		28	48	ns
t_{PLZ} Output Disable Time from Low Level					17	25		17	27		17	27	ns
t_{PZH} Output Enable Time to High Level	TE, DC, or SC (Note 2) (Note 3)	Terminal	$V_I = 3.0V$, $V_L = 0V$, $R_L = 3\ k\Omega$, $C_L = 15$ pF, *Figure 1*		17	33		18	40		18	40	ns
t_{PHZ} Output Disable Time from High Level					15	25		22	33		22	33	ns
t_{PZL} Output Enable Time to Low Level			$V_I = 0V$, $V_L = 5V$, $R_L = 280\Omega$, $C_L = 15$ pF, *Figure 1*		25	39		28	52		28	52	ns
t_{PLZ} Output Disable Time from Low Level					15	27		20	35		20	35	ns
t_{PZH} Output Pull-Up Enable Time (DS75160A Only)	PE (Note 2)	Bus	$V_I = 3V$, $V_L = 0V$, $R_L = 480\Omega$, $C_L = 15$ pF, *Figure 1*		10	17		NA			NA		ns
t_{PHZ} Output Pull-Up Disable Time (DS75160A Only)					10	15		NA			NA		ns

Note 1: Typical values are for $V_{CC} = 5.0V$ and $T_A = 25°C$ and are meant for reference only.

Note 2: Refer to Functional Truth Tables for control input definition.

Note 3: Test configuration should be connected to only one transceiver at a time due to the high current stress caused by the V_I voltage source when the output connected to that input becomes active.

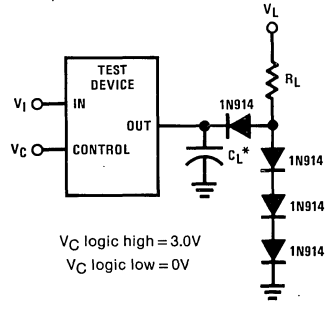
Switching Load Configurations



V_C logic high = 3.0V
V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 1 TL/F/5243-7



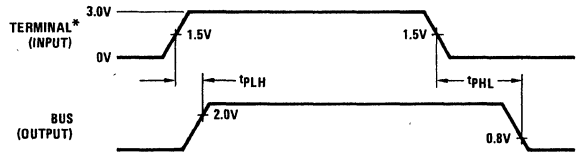
V_C logic high = 3.0V
V_C logic low = 0V

*C_L includes jig and probe capacitance

FIGURE 2 TL/F/5243-8

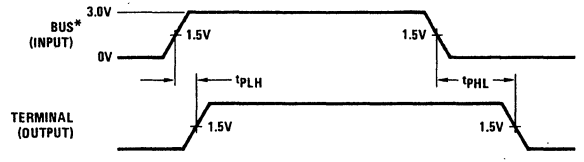
Switching Waveforms

Transmit Propagation Delays



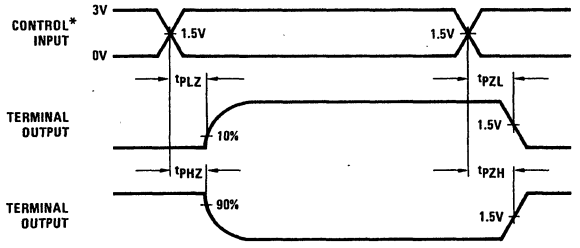
TL/F/5243-9

Receive Propagation Delays



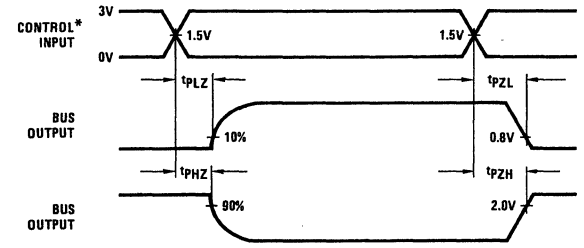
TL/F/5243-10

Terminal Enable/Disable Times



TL/F/5243-11

Bus Enable/Disable Times

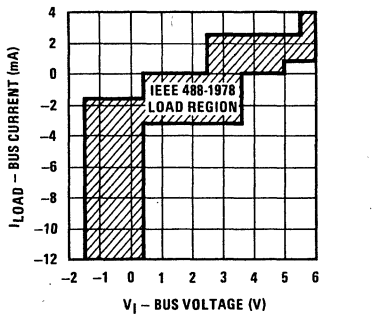


TL/F/5243-12

*Input signal: f = 1.0 MHz, 50% duty cycle, $t_r = t_f \leq 5$ ns

Performance Characteristics

Bus Port Load Characteristic



TL/F/5243-13

Refer to Electrical Characteristics table

Functional Truth Tables

DS75160A

Control Input Level		Data Transceivers	
TE	PE	Direction	Bus Port Configuration
H	H	T	Totem-Pole Output
H	L	T	Open Collector Output
L	X	R	Input

DS75161A

Control Input Level			Transceiver Signal Direction							
TE	DC	ATN*		EOI	REN	IFC	SRQ	NRFD	NDAC	DAV
H	H		R		R	R	T	R	R	T
H	L		T		T	T	R	R	R	T
L	H		R		R	R	T	T	T	R
L	L		T		T	T	R	T	T	R
H	X	H		T						
L	X	H		R						
X	H	L		R						
X	L	L		T						

DS75162A

Control Input Level				Transceiver Signal Direction							
SC	TE	DC	ATN*		EOI	REN	IFC	SRQ	NRFD	NDAC	DAV
H	H	H		R		T	T	T	R	R	T
H	H	L		T		T	T	R	R	R	T
H	L	H		R		T	T	T	T	T	R
H	L	L		T		T	T	R	T	T	R
L	H	H		R		R	R	T	R	R	T
L	H	L		T		R	R	R	R	R	T
L	L	H		R		R	R	T	T	T	R
L	L	L		T		R	R	R	T	T	R
X	H	X	H		T						
X	L	X	H		R						
X	X	H	L		R						
X	X	L	L		T						

H = High level input
L = Low level input
X = Don't care
T = Transmit, i.e., signal outputted to bus
R = Receive, i.e., signal outputted to terminal
* The ATN signal level is sensed for internal multiplex control of EOI transmission direction logic

National Semiconductor

DS7640/DS8640 Quad NOR Unified Bus Receiver

General Description

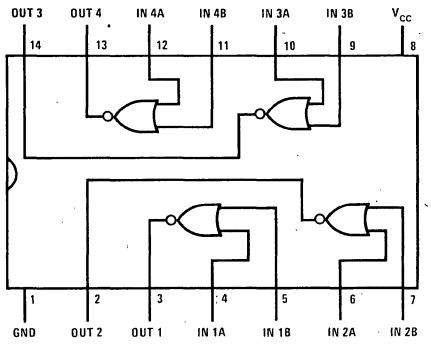
The DS7640 and DS8640 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input threshold providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus.

Features

- Low input current with normal V_{CC} or V_{CC} = 0V (30μA typ)
- High noise immunity (1.1V typ)
- Temperature-insensitive input thresholds track bus logic levels
- TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (19 ns typ)

Connection Diagram

Dual-In-Line Package

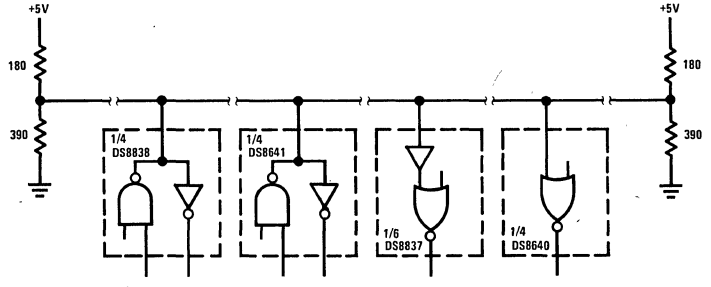


TOP VIEW

Order Number DS7640J, DS8640J or DS8640N
See NS Package J14A or N14A

Typical Application

120Ω Unified Data Bus



Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7640	4.5	5.5	V
DS8640	4.75	5.25	V
Temperature (T_A)			
DS7640	−55	+125	°C
DS8640	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Threshold	$V_{OUT} = V_{OL}$	DS7640	1.80	1.50		V
			DS8640	1.70	1.50		V
V_{IL}	Low Level Input Threshold	$V_{OUT} = V_{OH}$	DS7640		1.50	1.20	V
			DS8640		1.50	1.30	V
I_{IH}	Maximum Input Current	$V_{IN} = 4V$	$V_{CC} = V_{MAX}$		30	80	μA
			$V_{CC} = 0V$		1.0	50	μA
I_{IL}	Maximum Input Current	$V_{IN} = 0.4V$, $V_{CC} = V_{MAX}$			1.0	50	μA
V_{OH}	Output Voltage	$I_{OH} = -400\mu A$, $V_{IN} = V_{IL}$		2.4			V
V_{OL}	Output Voltage	$I_{OL} = 16$ mA, $V_{IN} = V_{IH}$			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{IN} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Power Supply Current	$V_{IN} = 4V$, (Per Package)			25	40	mA

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays	(Notes 5 and 6)	Input to Logic "1" Output	10	23	35	ns
			Input to Logic "0" Output	10	15	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7640 and across the 0°C to +70°C range for the DS8640. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, $C_{LOAD} = 15$ pF total, measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 6: Apply for $V_{CC} = 5V$, $T_A = 25°C$.

National Semiconductor

DS7641/DS8641 Quad Unified Bus Transceiver

General Description

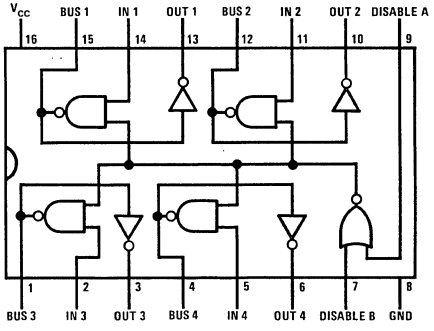
The DS7641 and DS8641 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate tight thresholds for better bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously.

Features

- 4 separate driver/receiver pairs per package
- Guaranteed minimum bus noise immunity of 0.6V, 1.1V typ
- Temperature insensitive receiver thresholds track bus logic levels
- 30μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

Connection Diagram

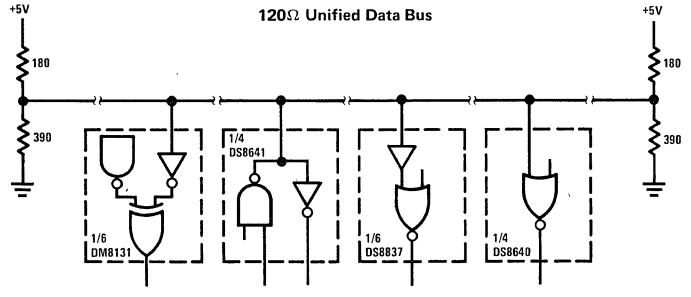
Dual-In-Line Package



TOP VIEW

Order Number DS7641J, DS8641J or DS8641N
See NS Package J16A or N16A

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input and Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, (V_{CC})			
DS7641	4.5	5.5	V
DS8641	4.75	5.25	V
Temperature Range, (T_A)			
DS7641	−55	+125	°C
DS8641	0	+70	°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Electrical Characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER AND DISABLE INPUTS							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_I	Logical "1" Input Current	V_{IN} = 5.5V				1	mA
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	I_{DIS} = −12 mA, I_{IN} = −12 mA, I_{BUS} = −12 mA, T_A = 25°C			−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT							
V_{OLB}	Low Level Bus Voltage	V_{DIS} = 0.8V, V_{IN} = 2V, I_{BUS} = 50 mA			0.4	0.7	V
I_{IHB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = V_{MAX}			30	100	μA
I_{ILB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 0V			2	100	μA
V_{IH}	High Level Receiver Threshold	V_{IND} = 0.8V, V_{OL} = 16 mA	DS7641	1.80	1.50		V
			DS8641	1.70	1.50		V
V_{IL}	Low Level Receiver Threshold	V_{IND} = 0.8V, V_{OH} = −400μA	DS7641		1.50	1.20	V
			DS8641		1.50	1.30	V
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 0.5V, I_{OH} = −400μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 4V, I_{OL} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = V_{MAX}, (Note 4)		−18		−55	mA
I_{CC}	Supply Current	V_{DIS} = 0V, V_{IN} = 2V, (Per Package)			50	70	mA

Switching Characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays (Note 7)					
	Disable to Bus "1"	(Note 5)		19	30	ns
	Disable to Bus "0"			15	30	ns
	Driver Input to Bus "1"			17	25	ns
	Driver Input to Bus "0"			17	25	ns
	Bus to Logical "1" Receiver Output	(Note 6)		20	30	ns
	Bus to Logical "0" Receiver Output			18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7641 and across the 0°C to +70°C range for the DS8641. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground. C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{BUS} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 6: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 7: The following apply for V_{CC} = 5V, T_A = 25°C unless otherwise specified.

National Semiconductor

DS8642 Quad Transceiver

General Description

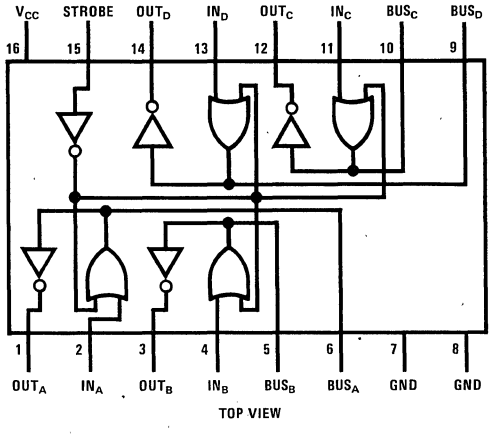
The DS8642 is a quad transceiver designed for bus organized data transmission systems terminated by 50Ω impedance. The bus can be terminated at one or both ends. It has four bus drivers with a common strobe gate and four bus receivers. Bus driver outputs can be "OR-tied" with up to 19 other drivers and with up to 20 bus receiver loads. The bus loading is 2k when V_{CC} = 0V.

Features

- 100 mA Drive Capability
- Four separate driver/receiver pairs
- Open collector driver output allows wire-OR connection
- 50Ω line termination
- Completely TTL compatible on driver and disable inputs, and receiver outputs

Logic and Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS8642J
or DS8642N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DISABLE/DRIVER INPUT							
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−0.9	−1.6	mA
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1	mA
V_{CD}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
RECEIVER INPUT/BUS OUTPUT							
V_{IHB}	Logical "1" Input Voltage	V_{CC} = Max		3.1			V
V_{ILB}	Logical "0" Input Voltage	V_{CC} = Min				1.4	V
V_{CDB}	Input Clamp Diode	I_{IN} = −50 mA			−1.0	−1.5	V
I_{IHB}	Logical "1" Input Current	V_{CC} = Max, V_{INB} = V_{CC}			180	450	μA
I_{ILB}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−40	μA
V_{OLB}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 100 mA			0.4	0.8	V
I_{OL}	Logical "0" Output Current	V_{CC} = Min, V_{OL} = 0.8V		100			mA
I_{OHB}	Power "OFF" Bus Current	V_{CC} = 0V, V_{INB} = 5.25V			1.7	2.65	mA
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −1 mA		2.4	3.2		V
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{OUT} = 5.5V				100	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Min, V_{OUT} = 0V, (Note 4)		−10	−28	−55	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA			0.3	0.45	V
I_{CC}	Supply Current	V_{CC} = Max			49	64	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8642. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

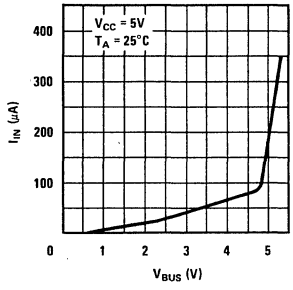
Note 4: Only one output at a time should be shorted.

Switching Characteristics $T_A = 25°C$, nominal power supplies unless otherwise noted

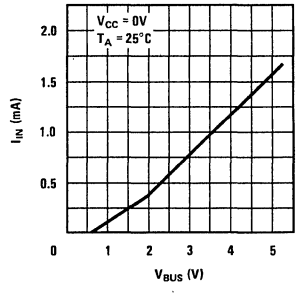
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" From Data Input to Receiver Output	*(Figure 1)*		34	50	ns
t_{pd1}	Propagation Delay to a Logical "1" From Data Input to Receiver Output	*(Figure 1)*		25	50	ns
t_{pd0}	Propagation Delay to a Logical "0" From Strobe Input to Receiver Output	*(Figure 1)*		38	55	ns
t_{pd1}	Propagation Delay to a Logical "1" From Strobe Input to Receiver Output	*(Figure 1)*		25	55	ns

Typical Performance Characteristics

Receiver ON Impedance



Receiver OFF Impedance



AC Test Circuit and Switching Time Waveforms

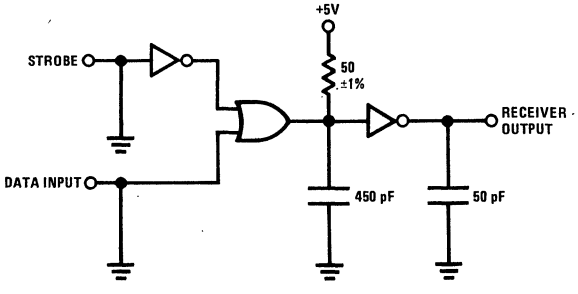
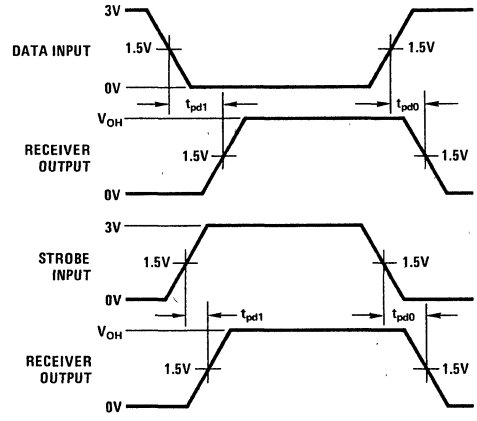


FIGURE 1.



f = 5 MHz
Pulse Width = 100 ns
$t_r = t_f \approx 5$ ns

National Semiconductor

DS7833/DS8833, DS7835/DS8835 Quad TRI-STATE® Bus Transceivers

General Description

This family of TRI-STATE bus transceivers offer extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated dc or ac, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DS7833/DS8833 and DS7835/DS8835 employ TRI-STATE outputs on the receiver also.

The DS7833/DS8833 are non-inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

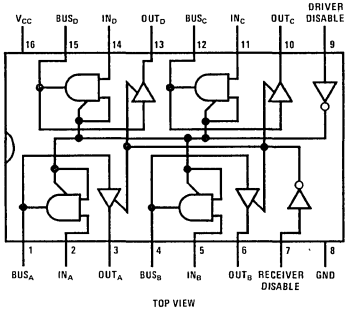
The DS7835/DS8835 are inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

Features

- Receiver hysteresis — 400 mV typ
- Receiver noise immunity — 1.4V typ
- Bus terminal current for normal V_{CC} or V_{CC} = 0V — 80μA max
- Receivers
  - Sink — 16 mA at 0.4V max
  - Source — 2.0 mA (Mil) at 2.4V min; 5.2 mA (Com) at 2.4V min
- Drivers
  - Sink — 50 mA at 0.5V max; 32 mA at 0.4V max
  - Source — 10.4 mA (Com) at 2.4V min; 5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- DS7833/DS8833, DS7835/DS8835 receivers have TRI-STATE outputs
- Capable of driving 100Ω dc—terminated buses
- Compatible with Series 54/74

Connection Diagrams

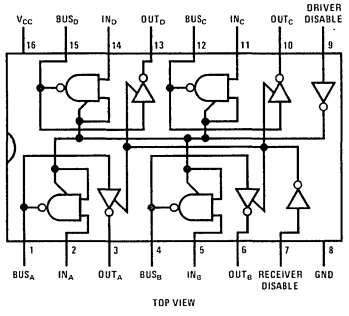
Dual-In-Line Package



TOP VIEW

Order Number DS7833J, DS8833J or DS8833N
See NS Package J16A or N16A

Dual-In-Line Package



TOP VIEW

Order Number DS7835J, DS8835J or DS8835N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7833, DS7835	4.5	5.5	V
DS8833, DS8835	4.75	5.25	V
Temperature (T_A)			
DS7833, DS7835	−55	+125	°C
DS8833, DS8835	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min	DS7833, DS8833, DS8835				0.8	V
			DS7835				0.7	
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
I_{IT}	Driver Low Level Disabled Input Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	μA
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage			DS7833, DS7835	1.4	1.75	2.1	V
				DS8833, DS8835	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage			DS7833, DS7835	0.8	1.35	1.6	V
				DS8833, DS8835	0.8	1.35	1.5	V
I_B	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max			25	80	μA
			V_{CC} = 0V			5.0	80	μA
		V_{CC} = Max, V_{BUS} = 0.4V				−2.0	−40	μA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7833, DS7835	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS8833, DS8835	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7833, DS7835	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8833, DS8835	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OT}	Output Disabled Current	V_{CC} = Max, Disable Inputs = 2.0V	V_{OUT} = 2.4V				40	μA
			V_{OUT} = 0.4V				−40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)		DS7833, DS7835	−28	−40	−70	mA
				DS8833, DS8835	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max		DS7833/DS8833		84	116	mA
				DS7835/DS8835		75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7833, DS7835 and across the 0°C to +70°C range for the DS8833, DS8835. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logic "0" From Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" From Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" From Bus to Output	*(Figure 2)*	DS7833/DS8833		24	45	ns
			DS7835/DS8835		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" From Bus to Output	*(Figure 2)*	DS7833/DS8833		12	30	ns
			DS7835/DS8835		18	30	ns
t_{PHZ}	Delay From Disable Input to High Impedance State (From Logic "1" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver		8.0	20	ns
			Receiver		6.0	15	ns
t_{PLZ}	Delay From Disable Input to High Impedance State (From Logic "0" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver		20	35	ns
			Receiver		13	25	ns
t_{PZH}	Delay From Disable Input to Logic "1" Level (From High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver		24	40	ns
			Receiver		16	35	ns
t_{PZL}	Delay From Disable Input to Logic "0" Level (From High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver		19	35	ns
			Receiver DS7833/DS8833		15	30	ns
			Receiver DS7835/DS8835		33	50	ns

AC Test Circuits

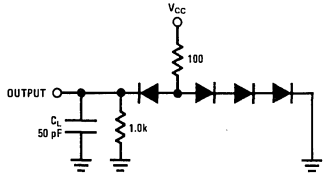


FIGURE 1. Driver Output Load

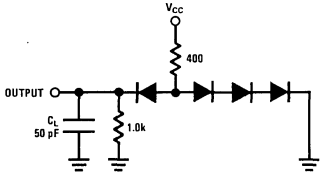
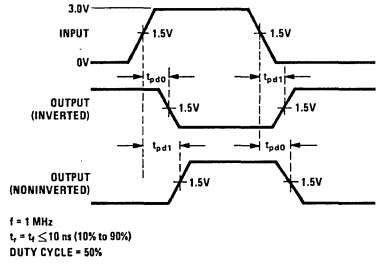


FIGURE 2. Receiver Output Load

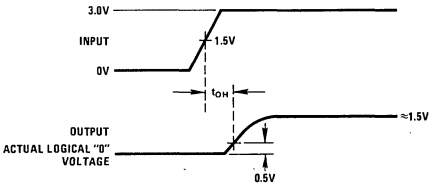
Switching Time Waveforms

t_{pd1} & t_{pd0}



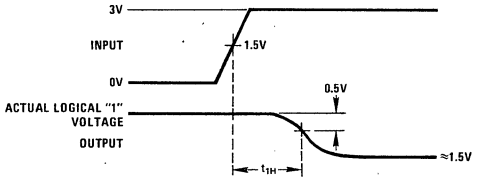
f = 1 MHz
$t_r = t_f \leq 10$ ns (10% to 90%)
DUTY CYCLE = 50%

t_{PLZ}

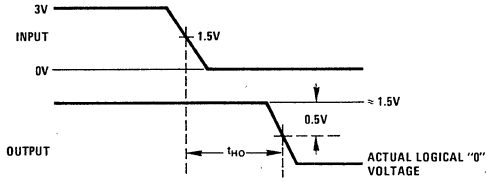


Switching Time Waveforms (Continued)

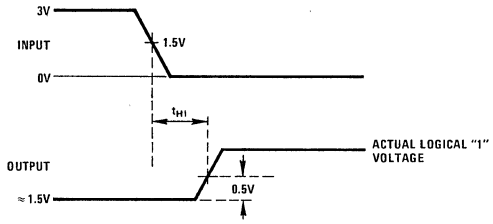
t_{PHZ}



t_{PZL}



t_{PZH}



DS7834/DS8834, DS7839/DS8839 Quad TRI-STATE® Bus Transceivers

General Description

This family of TRI-STATE bus transceivers offers extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated dc or ac, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low, allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. Both devices utilize a high current TRI-STATE output driver. The DS7834/DS8834 and DS7839/DS8839 employ TTL outputs on the receiver.

The DS7839/DS8839 are non-inverting quad transceivers with two common inverter driver disable controls.

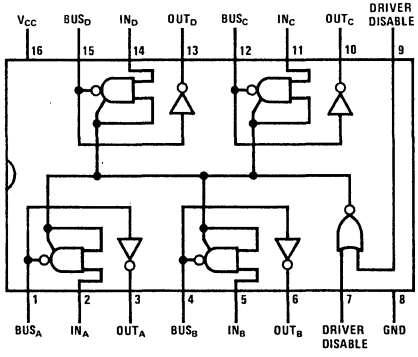
The DS7834/DS8834 are inverting quad transceivers with two common inverter driver disable controls.

Features

- Receiver hysteresis — 400 mV typ
- Receiver noise immunity — 1.4V typ
- Bus terminal current for normal V_{CC} or V_{CC} = 0V — 80μA max
- Receivers
  - Sink — 16 mA at 0.4V max
  - Source — 2.0 mA (Mil) at 2.4V min; 5.2 mA (Com) at 2.4V min
- Drivers
  - Sink — 50 mA at 0.5V max; 32 mA at 0.4V max
  - Source — 10.4 mA (Com) at 2.4V min; 5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- Receivers have TRI-STATE outputs
- Capable of driving 100Ω dc–terminated buses
- Compatible with Series 54/74

Connection Diagrams

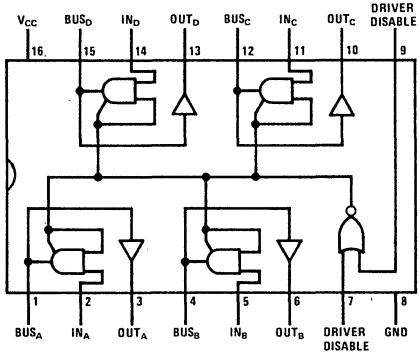
Dual-In-Line Package



TOP VIEW

Order Number DS7834J, DS8834J or DS8834N
See NS Package J16A or N16A

Dual-In-Line Package



TOP VIEW

Order Number DS7839J, DS8839J or DS8839N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 Seconds)	300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7834, DS7839	4.5	5.5	V
DS8834, DS8839	4.75	5.25	V
Temperature (T_A)			
DS7834, DS7839	−55	+125	°C
DS8834, DS8839	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min					0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{IND}	Driver Disabled Input Low Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	μA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage	V_{CC} = Max		DS7834, DS7839	1.4	1.75	2.1	V
				DS8834, DS8839	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage	V_{CC} = Min		DS7834, DS7839	0.8	1.35	1.6	V
				DS8834, DS8839	0.8	1.35	1.5	V
I_{BH}	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max, Disable Input = 2.0V			25	80	μA
			V_{CC} = 0V			5.0	80	μA
		V_{CC} = Max, V_{BUS} = 0.4V, Disable Input = 2.0V					−40	μA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7834, DS7839	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS7834, DS8839	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7834, DS7839	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8834, DS8839	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)		DS7834, DS7839	−28	−40	−70	mA
				DS8834, DS8839	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max				75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7834, DS7839 and across the 0°C to +70°C range for the DS8834, DS8839. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logic "0" from Input to Bus	*(Figure 1)*	DS7839/DS8839		14	30	ns
			DS7834/DS8834		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" from Input to Bus	*(Figure 1)*	DS7839/DS8839		14	30	ns
			DS7834/DS8834		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" from Bus to Output	*(Figure 2)*	DS7839/DS8839		24	45	ns
			DS7834/DS8834		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" from Bus to Output	*(Figure 2)*	DS7839/DS8839		12	30	ns
			DS7834/DS8834		18	30	ns
t_{PHZ}	Delay from Disable Input to High Impedance State (from Logic "1" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver Only		8	20	ns
t_{PLZ}	Delay from Disable Input to High Impedance State (from Logic "0" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver Only		20	35	ns
t_{PZH}	Delay from Disable Input to Logic "1" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver Only		24	40	ns
t_{PZL}	Delay from Disable Input to Logic "0" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver Only		19	35	ns

AC Test Circuit

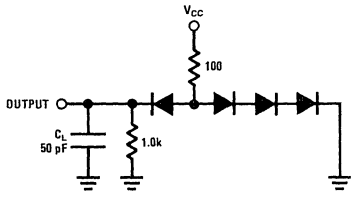


FIGURE 1. Driver Output Load

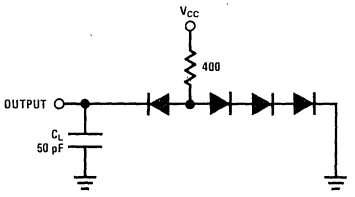
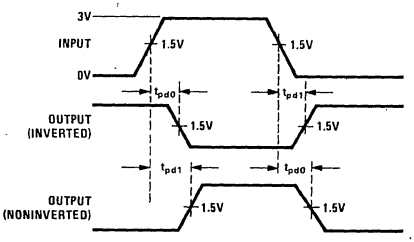


FIGURE 2. Receiver Output Load

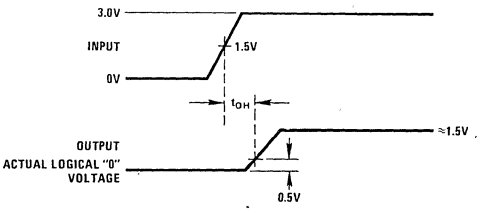
Switching Time Waveforms

t_{pd1} and t_{pd0}

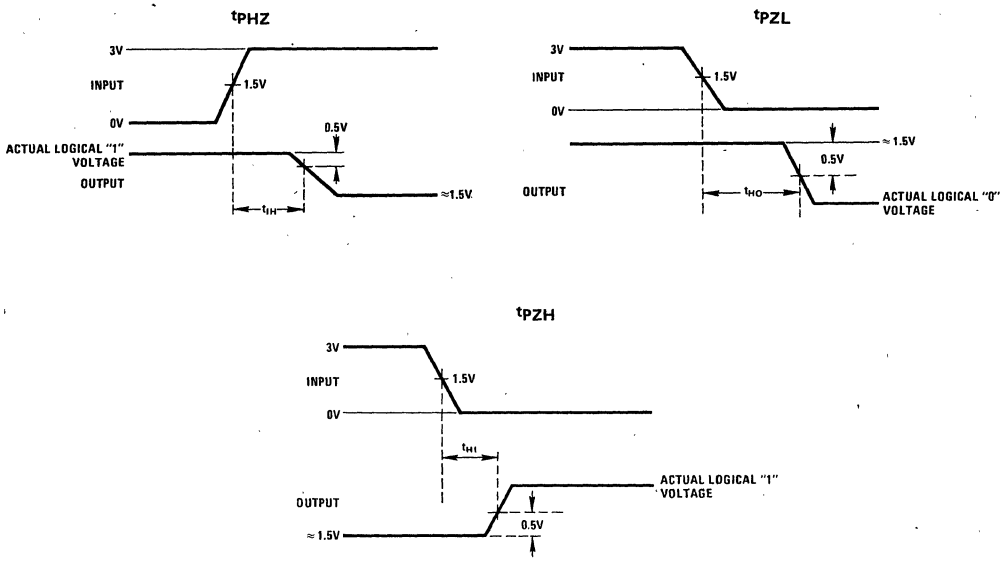


f = 1 MHz
$t_r = t_f \leq 10$ ns (10% to 90%)
Duty Cycle = 50%

t_{PLZ}



Switching Time Waveforms (Continued)



Truth Table

DISABLE INPUT	DRIVER INPUT (IN_X)	RECEIVER INPUT/ BUS OUTPUT (BUS_X)	RECEIVER OUTPUT (OUT_X)	MODE OF OPERATION
DS7834/DS8834				
1	X		$\overline{BUS}$	Receive bus signal
0	1	0	1	Drive bus
0	0	1	0	Drive bus
DS7839/DS8839				
1	X		BUS	Receive bus signal
0	1	1	1	Drive bus
0	0	0	0	Drive bus

X = Don't care

National Semiconductor

Bus Transceivers

DS7836/DS8836 Quad NOR Unified Bus Receiver

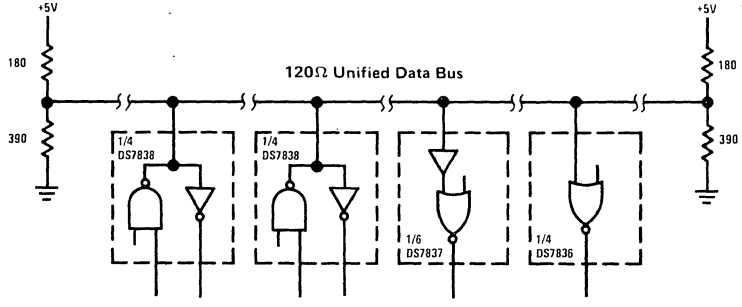
General Description

The DS7836/DS8836 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Performance is optimized for systems with bus rise and fall times $\leq 1.0\ \mu s/V$.

Features

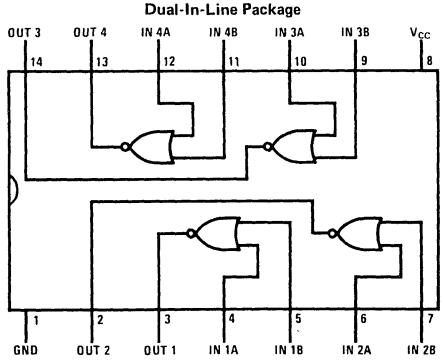
- Low input current with normal V_{CC} or $V_{CC} = 0V$ (15 μA typ)
- Built-in input hysteresis (1V typ)
- High noise immunity (2V typ)
- Temperature-insensitive input thresholds track bus logic levels
- TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (18 ns typ)

Typical Application



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS7836J or DS8836J
See NS Package J14A

Order Number DS8836N
See NS Package N14A

Absolute Maximum Ratings

Supply Voltage	7.0V
Current Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7836	4.5	5.5	V
DS8836	4.75	5.25	V
Temperature (T_A)			
DS7836	−55	+125	°C
DS8836	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	High Level Input Threshold	V_{CC} = Max		DS7836	1.65	2.25	2.65	V
				DS8836	1.80	2.25	2.50	V
V_{IL}	Low Level Input Threshold	V_{CC} = Min		DS7836	0.97	1.30	1.63	V
				DS8836	1.05	1.30	1.55	V
I_{IN}	Maximum Input Current	V_{IN} = 4V	V_{CC} = Max			15	50	μA
			V_{CC} = 0V			1	50	μA
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.5V, I_{OUT} = −400μA			2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 4V, I_{OUT} = 16 mA				0.25	0.4	V
I_{SC}	Output Short Circuit Current	V_{IN} = 0.5V, V_{OUT} = 0V, V_{CC} = Max, (Note 4)			−18		−55	mA
I_{CC}	Power Supply Current	V_{IN} = 4V, (Per Package)				25	40	mA
V_{CL}	Input Clamp Diode Voltage	I_{IN} = −12 mA, T_A = 25°C				−1	−1.5	V

Switching Characteristics

V_{CC} = 5V, T_A = 25°C unless otherwise specified.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays	(Notes 4 and 5)	Input to Logical "1" Output		20	30	ns
			Input to Logical "0" Output		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7836 and across the 0°C to +70°C range for the DS8836. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Fan-out of 10 load, C_{LOAD} = 15 pF total, measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 5: Fan-out of 10 load, C_{LOAD} = 15 pF total, measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

National Semiconductor

Bus Transceivers

DS7837/DS8837 Hex Unified Bus Receiver

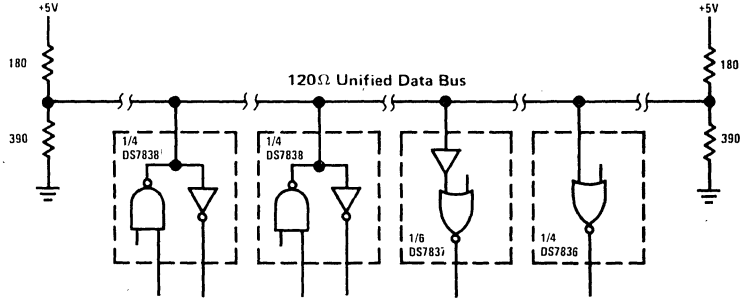
General Description

The DS7837/DS8837 are high speed receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The receiver design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Disable inputs provide time discrimination. Disable inputs and receiver outputs are TTL compatible. Performance is optimized for systems with bus rise and fall times $\leq 1.0\ \mu s/V$.

Features

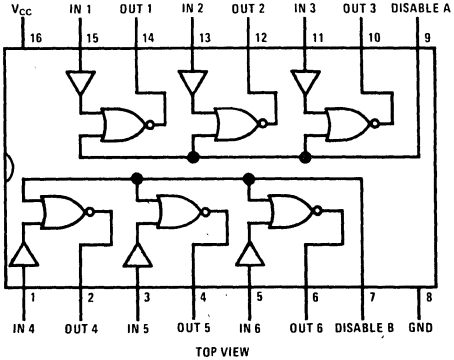
- Low receiver input current for normal V_{CC} or $V_{CC} = 0V$ (15 μA typ)
- Six separate receivers per package
- Built-in receiver input hysteresis (1V typ)
- High receiver noise immunity (2V typ)
- Temperature insensitive receiver input thresholds track bus logic levels
- TTL compatible disable and output
- Molded or cavity dual-in-line or flat package
- High speed

Typical Application



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS7837J or DS8837J
See NS Package J16A

Order Number DS8837N
See NS Package N16A

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	5.5V
Operating Temperature Range	
DS7837	−55°C to +125°C
DS8837	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7837	4.5	5.5	V
DS8837	4.75	5.25	V
Temperature (T_A)			
DS7837	−55	+125	°C
DS8837	0	+70	°C

Electrical Characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	High Level Receiver Threshold	V_{CC} = Max	DS7837	1.65	2.25	2.65	V
			DS8837	1.80	2.25	2.50	V
V_{TL}	Low Level Receiver Threshold	V_{CC} = Min	DS7837	0.97	1.30	1.63	V
			DS8837	1.05	1.30	1.55	V
I_{IH}	Maximum Receiver Input Current	V_{IN} = 4V	$V_{CC} = V_{MAX}$		15.0	50.0	μA
			V_{CC} = 0V		1.0	50.0	μA
I_{IL}	Logical "0" Receiver Input Current	V_{IN} = 0.4V, $V_{CC} = V_{MAX}$			1.0	50.0	μA
V_{IH}	Logical "1" Input Voltage		Disable	2.0			V
V_{IL}	Logical "0" Input Voltage		Disable			0.8	V
I_{IH}	Logical "1" Input Current	Disable Input	V_{IND} = 2.4V			80.0	μA
			V_{IND} = 5.5V			2.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 4V, V_{IND} = 0.4V, Disable Input				−3.2	mA
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.5V, V_{IND} = 0.8V, I_{OH} = −400μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 4V, V_{IND} = 0.8V, I_{OL} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{IN} = 0.5V, V_{IND} = 0V, V_{OS} = 0V, $V_{CC} = V_{MAX}$, (Note 4)		−18.0		−55.0	mA
I_{CC}	Power Supply Current	V_{IN} = 4V, V_{IND} = 0V, (Per Package)			45.0	60.0	mA
V_{CL}	Input Clamp Diode	V_{IN} = −12 mA, V_{IND} = −12 mA, T_A = 25°C			−1.0	−1.5	V

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays	V_{IND} = 0V, Receiver	Input to Logical "1" Output, (Note 5)		20	30	ns
			Input to Logical "0" Output, (Note 6)		18	30	ns
		Input = 0V, Disable, (Note 7)	Input to Logical "1" Output		9	15	ns
			Input to Logical "0" Output		4	10	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7837 and across the 0°C to +70°C range for the DS8837. All typicals values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positve, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 6: Fan-out of 10 load, C_{LOAD} =15 pF total. Measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 7: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

National Semiconductor

DS7838/DS8838 Quad Unified Bus Transceiver

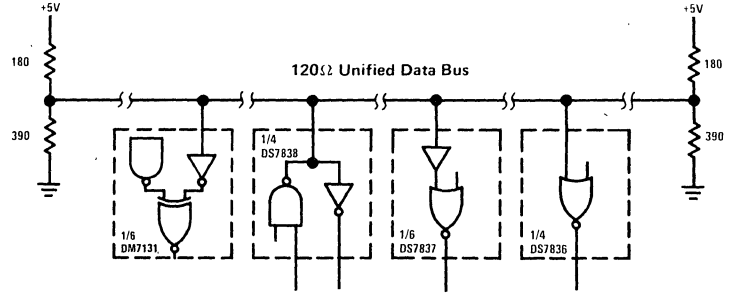
General Description

The DS7838/DS8838 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously. Receiver performance is optimized for systems with bus rise and fall times $\leq 1.0\mu s/V$.

Features

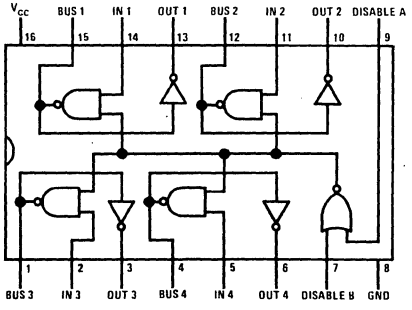
- 4 totally separate driver/receiver pairs per package
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature-insensitive receiver thresholds track bus logic levels
- 20μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

Typical Application



Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS7838J or DS8838J
See NS Package J16A

Order Number DS8838N
See NS Package N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input and Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Operating Temperature Range	
DS7838	−55°C to +125°C
DS8838	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, (Soldering, 10 sec)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Electrical Characteristics

DS7838/DS8838: The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER AND DISABLE INPUTS							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_I	Logical "1" Input Current	V_{IN} = 5.5V				1	mA
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	I_{DIS} = −12 mA, I_{IN} = −12 mA, I_{BUS} = −12 mA, T_A = 25°C			−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT							
V_{OLB}	Low Level Bus Voltage	V_{DIS} = 0.8V, V_{IN} = 2V, I_{BUS} = 50 mA			0.4	0.7	V
I_{IHB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = V_{MAX}			20	100	μA
I_{ILB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 0V			2	100	μA
V_{IH}	High Level Receiver Threshold	V_{IND} 0.8V, V_{OL} = 16 mA, V_{CC} = Max	DS7838	1.65	2.25	2.65	V
			DS8838	1.80	2.25	2.50	V
V_{IL}	Low Level Receiver Threshold	V_{IND} = 0.8V, V_{OH} = −400μA, V_{CC} = Min	DS7838	0.97	1.30	1.63	V
			DS8838	1.05	1.30	1.55	V
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 0.5V, I_{OH} = −400μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 4V, I_{OL} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = V_{MAX}, (Note 4)		−18		−55	mA
I_{CC}	Supply Current	V_{DIS} = 0V, V_{IN} = 2V, (Per Package)			50	70	mA
t_{pd}	Propagation Delays (Note 8)						
	Disable to Bus "1"	(Note 5)			19	30	ns
	Disable to Bus "0"	(Note 5)			15	23	ns
	Driver Input to Bus "1"	(Note 5)			17	25	ns
	Driver Input to Bus "0"	(Note 5)			9	15	ns
	Bus to Logical "1" Reciever Output	(Note 6)			20	30	ns
	Bus to Logical "0" Receiver Output	(Note 7)			18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7838 and across the 0°C to +70°C range for the DS8838. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{BUS} = 1.5V, V_{IN} = 0V to 3.0V pulse.

Note 6: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3.0V pulse.

Note 7: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 2.3V to V_{OUT} = 1.5V V_{IN} = 0V to 3.0V pulse.

Note 8: These apply for V_{CC} = 5V, T_A = 25°C unless otherwise specified.

National Semiconductor

Bus Transceivers

DS8T26A, DS8T26AM, DS8T28, DS8T28M 4-Bit Bidirectional Bus Transceivers

General Description

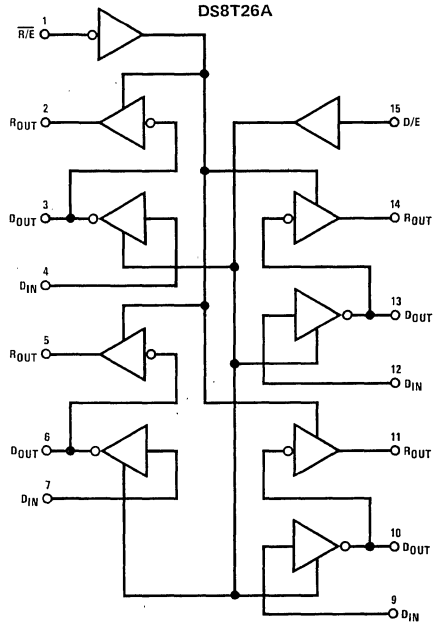
The DS8T26A, DS8T28 consist of 4 pairs of TRI-STATE® logic elements configured as quad bus drivers/receivers along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the DS8T26A, DS8T28 from conventional multi-IC implementations. In addition, the DS8T26A, DS8T28's ultra high speed while driving heavy bus capacitance (300 pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

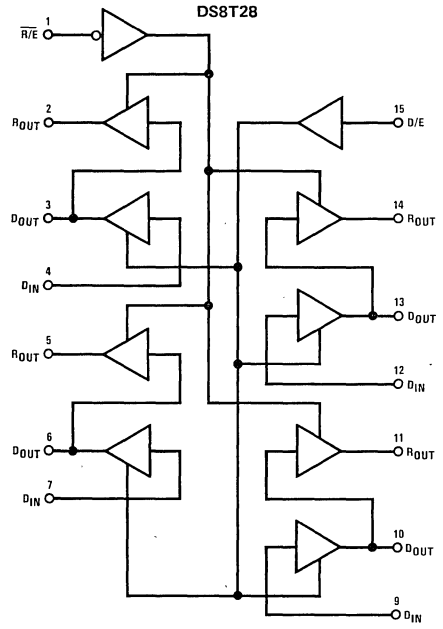
Both the driver and receiver gates have TRI-STATE outputs and low current PNP inputs. PNP inputs reduce input loading to 200 μA maximum.

Features

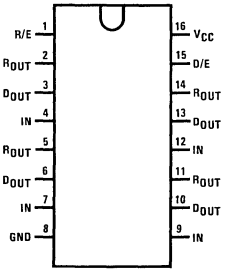
- Inverting outputs in the DS8T26A
- Non-inverting outputs in the DS8T28
- TRI-STATE outputs
- Low current PNP inputs
- Fast switching times (20 ns)
- Advanced Schottky processing
- Driver glitch free power up/down
- Non-overlapping TRI-STATE

Logic and Connection Diagrams





Dual-In-Line Package



TOP VIEW

Order Number DS8T26AJ, DS8T26AMJ, DS8T28J, DS8T28MJ, DS8T26AN or DS8T28N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

All Output and Supply Voltages	−0.5V to +7V
All Input Voltages	−1V to +5.5V
Output Currents	±150 mA
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS8T26A, DS8T28	4.75	5.25	V
DS8T26AM, DS8T28M	4.5	5.5	V
Temperature (T_A)			
DS8T26A, DS8T28	0	70	°C
DS8T26AM, DS8T28M	−55	+125	°C

Electrical Characteristics (Notes 2, 3 and 4)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−200	μA
I_{IL}	Low Level Input Current (Disabled)	V_{IN} = 0.4V			−25	μA
I_{IH}	High Level Input Current (D_{IN}, D_E)	V_{IN} = V_{CC} Max			25	μA
V_{OL}	Low Level Output Voltage, (Pins 3, 6, 10, 13)	I_{OUT} = 48 mA			0.5	V
V_{OH}	High Level Output Voltage, (Pins 3, 6, 10, 13)	I_{OUT} = −10 mA	2.4			V
I_{OS}	Short-Circuit Output Current, (Pins 3, 6, 10, 13)	V_{OUT} = 0V, V_{CC} = V_{CC} Max	−50		−150	mA
RECEIVER						
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−200	μA
I_{IH}	High Level Input Current (R_E)	V_{IN} = V_{CC} Max			25	μA
V_{OL}	Low Level Output Voltage	I_{OUT} = 20 mA			0.5	V
V_{OH}	High Level Output Voltage, (Pins 2, 5, 11, 14)	I_{OUT} = −100 μA	3.5			V
		I_{OUT} = −2 mA	2.4			V
I_{OS}	Short-Circuit Output Current, (Pins 2, 5, 11, 14)	V_{OUT} = 0V, V_{CC} = V_{CC} Max	−30		−75	mA
BOTH DRIVER AND RECEIVER						
V_{TL}	Low Level Input Threshold Voltage	V_{CC} = Min, V_{IN} = 0.8V, I_{OL} = Max	0.85			V
V_{TH}	High Level Input Threshold Voltage	V_{CC} = Max, V_{IN} = 0.8V, I_{OH} = Max			2	V
I_{OZ}	Low Level Output OFF Leakage Current	V_{OUT} = 0.5V			−100	μA
I_{OZ}	High Level Output OFF Leakage Current	V_{OUT} = 2.4V			100	μA
V_I	Input Clamp Voltage	I_{IN} = −12 mA			−1.0	V
I_{CC}	Power Supply Current					
	DS8T26A	V_{CC} = V_{CC} Max			87	mA
	DST28	V_{CC} = V_{CC} Max			110	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS8T26AM, DS8T28M and across the 0°C to +70°C range for the DS8T26A, DS8T28. All typicals are given for V_{CC} = 5V and T_A = 25°C.

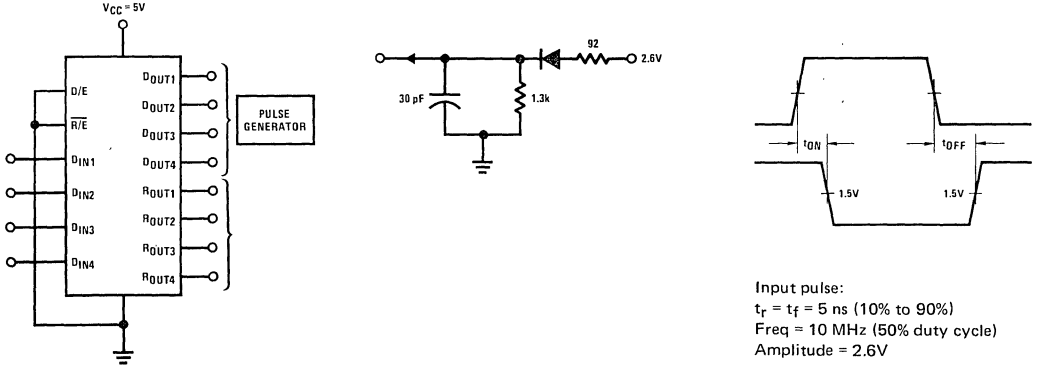
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics

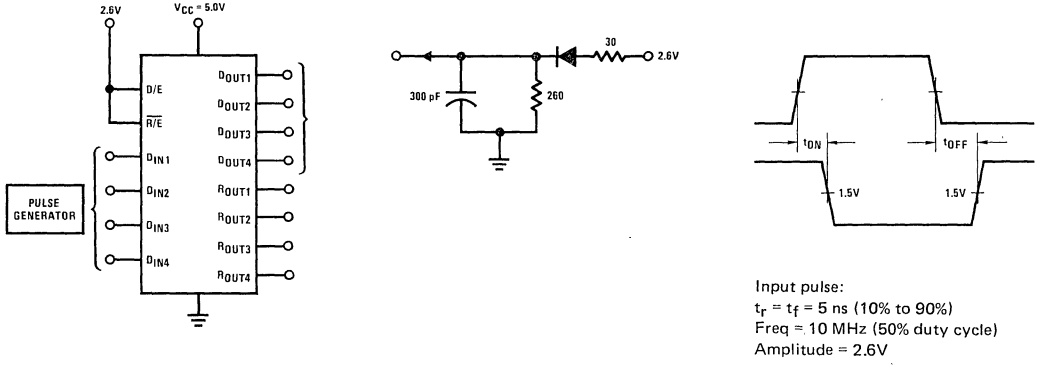
PARAMETER		CONDITIONS	DS8T26A MAX	DS8T28 MAX	UNITS
Propagation Delay					
t_{ON}	D_{OUT} to R_{OUT}, *(Figure 1)*	C_L = 30 pF	14	17	ns
t_{OFF}	D_{OUT} to R_{OUT}, *(Figure 1)*		14	17	ns
t_{ON}	D_{IN} to D_{OUT}, *(Figure 2)*	C_L = 300 pF	14	17	ns
t_{OFF}	D_{IN} to D_{OUT}, *(Figure 2)*		14	17	ns
Data Enable to Data Output					
t_{PZL}	High Z to O, *(Figure 3)*	C_L = 300 pF	25	28	ns
t_{PLZ}	O to High Z, *(Figure 3)*		20	23	ns
Receiver Enable to Receiver Output					
t_{PZL}	High Z to O, *(Figure 4)*	C_L = 30 pF	20	23	ns
t_{PLZ}	O to High Z, *(Figure 4)*		15	18	ns

AC Test Circuits and Switching Time Waveforms



Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 10 MHz (50% duty cycle)
Amplitude = 2.6V

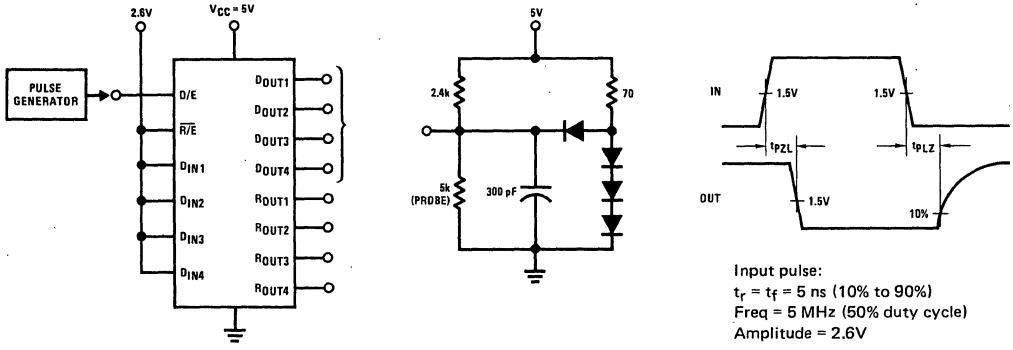
FIGURE 1. Propagation Delay (D_{OUT} to R_{OUT})



Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 10 MHz (50% duty cycle)
Amplitude = 2.6V

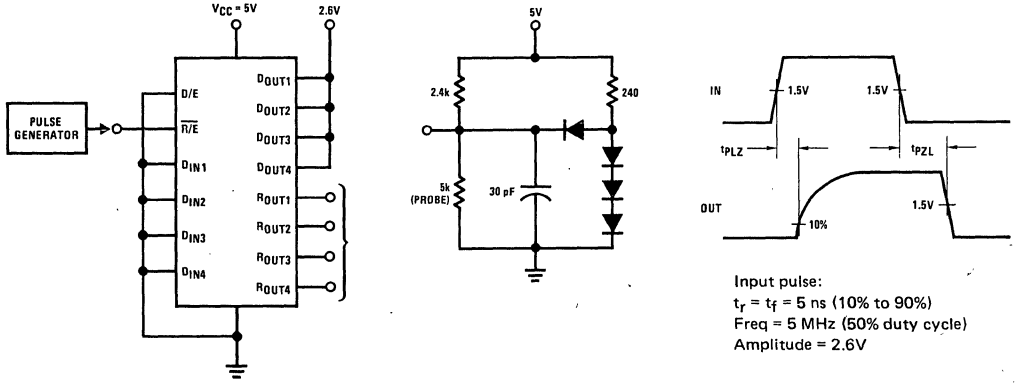
FIGURE 2. Propagation Delay (D_{IN} to D_{OUT})

AC Test Circuits and Switching Time Waveforms (Continued)



Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 5 MHz (50% duty cycle)
Amplitude = 2.6V

FIGURE 3. Propagation Delay (Data Enable to Data Output)



Input pulse:
$t_r = t_f$ = 5 ns (10% to 90%)
Freq = 5 MHz (50% duty cycle)
Amplitude = 2.6V

FIGURE 4. Propagation Delay ($\overline{\text{Receive/Enable}}$ to Receiver Output)

Section 3
Peripheral/Power Drivers

3

TEMPERATURE RANGE		DESCRIPTION	PAGE NUMBER
−55 °C to +125 °C	0 °C to +70 °C		
*DP7310	DP8310	Octal Latched Peripheral Drivers	3-4
*DP7311	DP8311	Octal Latched Peripheral Drivers	3-4
*DS1611	DS3611	Dual AND Peripheral Driver	3-11
*DS1612	DS3612	Dual NAND Peripheral Driver	3-11
*DS1613	DS3613	Dual OR Peripheral Driver	3-11
*DS1614	DS3614	Dual NOR Peripheral Driver	3-11
—	DS3616	Bubble Memory Coil Driver	3-17
*DS1631	DS3631	Dual AND CMOS Peripheral Driver	3-24
*DS1632	DS3632	Dual NAND CMOS Peripheral Driver	3-24
*DS1633	DS3633	Dual OR CMOS Peripheral Driver	3-24
*DS1634	DS3634	Dual NOR CMOS Peripheral Driver	3-24
—	DS3654	Printer Solenoid Driver	3-29
—	DS3656	Quad Peripheral Driver	3-33
—	DS3658	Quad High Current Peripheral Driver	3-35
—	DS3668	Quad High Current Peripheral Driver	3-38
—	DS3669	Quad High Current Peripheral Driver	3-41
—	DS3680	Quad Negative Voltage Relay Driver	3-44
—	DS3686	Dual Positive Voltage Relay Driver	3-47
*DS1687	DS3687	Dual Negative Voltage Relay Driver	3-49
—	DS75450	Dual AND Peripheral Driver	3-51
*DS55451	DS75451	Dual AND Peripheral Driver	3-51
*DS55452	DS75452	Dual NAND Peripheral Driver	3-51
*DS55453	DS75453	Dual OR Peripheral Driver	3-51
*DS55454	DS75454	Dual NOR Peripheral Driver	3-51
*DS55461	DS75461	Dual AND Peripheral Driver	3-62
*DS55462	DS75462	Dual NAND Peripheral Driver	3-62
*DS55463	DS75463	Dual OR Peripheral Driver	3-62
*DS55464	DS75464	Dual NOR Peripheral Driver	3-62
—	MM74C908	Dual CMOS 30V Driver	CMOS
—	MM74C918	Dual CMOS 30V Driver	CMOS
	AN-213	Safe Operating Areas for Peripheral Drivers	3-68

*Also available screened in accordance with MIL-STD-883 Class B. Refer to National Semiconductor's "The Reliability Handbook".

PERIPHERAL/POWER DRIVERS

Output High Voltage (V)	Latch-Up Voltage (Note 3) (V)	Output Low Voltage (V)	Output Low Current (mA)	Propagation Delay Typ (ns)	ON Power Supply Current (mA)	Drivers/ Package	Input Compatibility (Logic)	Logic Function (Driver ON)	Device Number and Temperature Range		Page No.
									0°C to +70°C	−55°C to +125°C	
30		0.5	100	40	152	8	TTL	Note 5	DP8310	DP7310	3-4
30		0.5	100	40	125	8	TTL	Note 6	DP8311	DP7311	3-4
20	13.5	0.6	100	70	90	2	TTL	Note 7	DS3616		3-17
65	30	1.5	600		65	4	TTL/LS	NAND	DS3656		3-33
70	35	0.7	600	2430	65	4	TTL/LS	NAND	DS3658		3-35
70	Note 8	1.5	600	2000	80	4	TTL/LS	NAND	DS3668		3-38
70	35	0.7	600		65	4	TTL/LS	AND	DS3669		3-41
30	20	0.7	300	31	55	2	TTL	AND	DS75450		3-51
30	20	0.7	300	31	55	2	TTL	AND	DS75451	DS55451	3-51
30	20	0.7	300	31	55	2	TTL	NAND	DS75452	DS55452	3-51
30	20	0.7	300	31	55	2	TTL	OR	DS75453	DS55453	3-51
30	20	0.7	300	31	55	2	TTL	NOR	DS75454	DS55454	3-51
35	30	0.7	300	33	55	2	TTL	AND	DS75461	DS55461	3-62
35	30	0.7	300	33	55	2	TTL	NAND	DS75462	DS55462	3-62
35	30	0.7	300	33	55	2	TTL	OR	DS75463	DS55463	3-62
35	30	0.7	300	33	55	2	TTL	NOR	DS75464	DS55464	3-62
56	40	1.4	300	150	8	2	CMOS	AND	DS3631	DS1631	3-24
56	40	1.4	300	150	8	2	CMOS	NAND	DS3632	DS1632	3-24
56	40	1.4	300	150	8	2	CMOS	OR	DS3633	DS1633	3-24
56	40	1.4	300	150	8	2	CMOS	NOR	DS3634	DS1634	3-24
80	50	0.7	300	125	75	2	TTL/CMOS	AND	DS3611	DS1611	3-11
80	50	0.7	300	125	75	2	TTL/CMOS	NAND	DS3612	DS1612	3-11
80	50	0.7	300	125	75	2	TTL/CMOS	OR	DS3613	DS1613	3-11
80	50	0.7	300	125	75	2	TTL/CMOS	NOR	DS3614	DS1614	3-11
−2.1	−60	−60	−50	10,000	4.4	4	TTL/CMOS	(Note 4)	DS3680		3-44
(Note 1)	56	1.3	300	1000	28	2	TTL/CMOS	NAND	DS3686		3-47
(Note 1)	−56	−1.3	300	1000	28	2	TTL/CMOS	NAND	DS3687	DS1687	3-49
13.5	15	V_{CC}−1.8	300	150	0.015	2	CMOS	AND	MM74C908, MM74C918		CMOS CMOS
(Note 1)	45	1.6	250	1000	70	10	(Note 2)	(Note 2)	DS3654		3-29

Note 1: The DS3686, DS3687 and DS3654 contain an internal inductive fly-back clamp circuit connected from the output to ground. As an example, DS3686 driving a relay solenoid connected to 28V would clamp the output voltage fly-back transient at 56V caused by the solenoid's stored inductive current. This clamp protects the circuit output and quenches the fly-back.

Note 2: The DS3654 is a 10-bit shift register followed by 10 enabled drivers. The input circuit is equivalent to a 4k resistor to ground, and the logic input thresholds are 2.8V and 0.8V. The recommended power supply voltage is 7.5V to 9.5V. The circuit can be cascaded to be a 20 or 30-bit shift register.

Note 3: Latch-up voltage is the maximum voltage the output can sustain when switching an inductive load.

Note 4: DS3680 has a differential input circuit.

Note 5: DP8310 inverting, positive edge latching.

Note 6: DP8311 inverting, fall through latch.

Note 7: Bubble memory coil driver.

Note 8: DS3668 35V, latch-up with output fault protection.

National Semiconductor

DP7310/DP8310/DP7311/DP8311 Octal Latched Peripheral Drivers

General Description

The DP7310/8310, DP7311/8311 Octal Latched Peripheral Drivers provide the function of latching eight bits of data with open collector outputs, each driving up to 100mA DC with an operating voltage range of 30 volts. Both devices are designed for low input currents, high input/output voltages, and feature a power up clear (outputs off) function.

The DP7310/8310 are positive edge latching. Two active low write/enable inputs are available for convenient data bussing without external gating.

The DP7311/8311 are fall through latches. The active low strobe input latches data or allows fall through operation when held at logic "0". The latches are cleared (outputs off) with a logic "0" on the clear pin.

Features

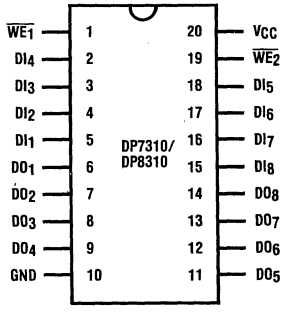
- High current, high voltage open collector outputs
- Low current, high voltage inputs
- All outputs simultaneously sink rated current "DC" with no thermal derating at maximum rated temperature.
- Parallel latching or buffering
- Separate active low enables for easy data bussing
- Internal "glitch free" power up clear
- 10% V_{CC} tolerance

Applications

- High current high voltage drivers
- Relay drivers
- Lamp drivers
- LED drivers
- TRIAC drivers
- Solenoid drivers
- Stepper motor drivers
- Level translators
- Fiber-optic LED drivers

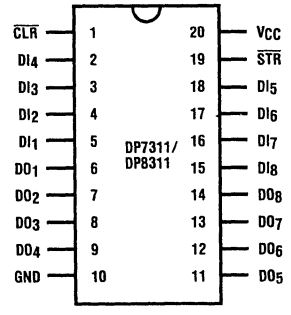
Connection Diagrams

Dual-In-Line Package



TL/F5246

Dual-In-Line Package



TL/F5246

Order Number DP7310J, DP7311J, DP8310J, DP8311J, DP8310N or DP8311N
See NS Package J20A or N20A

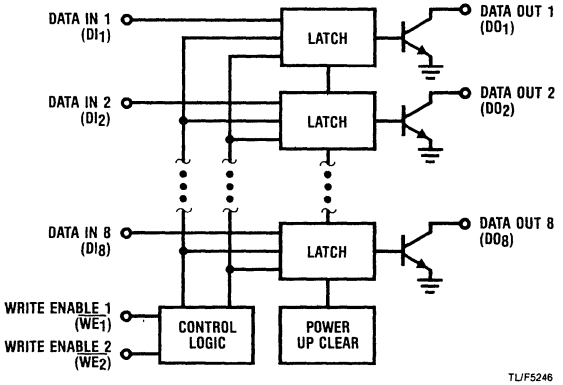
Logic Table

DP7310/DP8310			
Write Enable 1 $\overline{WE_1}$	Write Enable 2 $\overline{WE_2}$	Data Input DI_{1-8}	Data Output DO_{1-8}
0	0	X	Q
0	↓	0	1
0	↓	1	0
↓	0	0	1
↓	0	1	0
0	1	X	Q
1	0	X	Q
1	1	X	Q

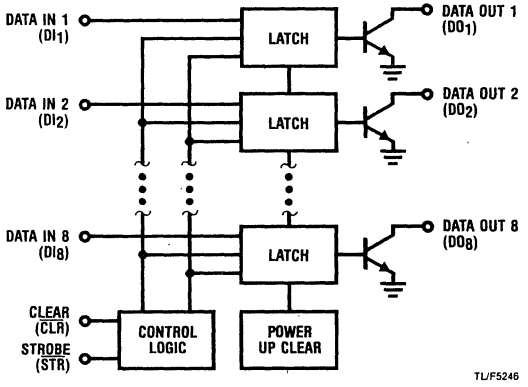
DP7311/DP8311			
Clear $\overline{CLR}$	Strobe $\overline{STR}$	Data Input DI_{1-8}	Data Output DO_{1-8}
1	1	X	Q
1	0	0	1
1	0	1	0
0	X	X	1

X = Don't Care
1 = Outputs Off
0 = Outputs On
Q = Pre-existing Output
↓ = Positive Edge Transition

Block Diagram DP7310/DP8310



Block Diagram DP7311/DP8311



Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	35V
Output Voltage	35V
Maximum Power Dissipation* at 25°C	
Cavity Package	1821 mW
Molded Package	2005 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 12.1 mW/°C above 25°C; derate molded package 16.0 mW/°C above 25°C.

Operating Conditions

	Min.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature			
DP7310/DP7311	−55	+125	°C
DP8310/DP8311	0	+70	°C
Input Voltage		30	V
Output Voltage		30	V

DC Electrical Characteristics DP7310/DP8310, DP7311/DP8311 (Notes 2 and 3)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
V_{OL}	Logical "0" Output Voltage	Data outputs latched to logical "0", V_{CC} = min.				
	DP7310/DP7311	I_{OL} = 75 ma			0.4	V
	DP8310/DP8311	I_{OL} = 100 mA		0.35	0.5	V
I_{OH}	Logical "1" Output Current	Data outputs latched to logical "1", V_{CC} = min.				
	DP7310/DP7311	V_{OH} = 25V			500	μA
	DP8310/DP8311	V_{OH} = 30V		2.5	250	μA
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V, V_{CC} = max.		0.1	25	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 30V, V_{CC} = max.		1	250	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, V_{CC} = max.		−215	−300	μA
V_{clamp}	Input Clamp Voltage	I_{IN} = −12 mA		−0.8	−1.5	V
I_{CC0}	Supply Current, Outputs On	Data outputs latched to a logical "0". All inputs are at logical "1", V_{CC} = max.				
	DP7310			100	125	mA
	DP8310			100	152	mA
	DP7311			88	117	mA
	DP8311			88	125	mA
I_{CC1}	Supply Current, Outputs Off	Data outputs latched to a logic "1". Other conditions same as I_{CC0}.				
	DP7310			40	47	mA
	DP8310			40	57	mA
	DP7311			25	34	mA
	DP8311			25	36	mA

AC Electrical Characteristics DP7310/DP8310: $V_{CC} = 4.5V$, $T_A = -55°C$ to $125°C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0}	High to Low Propagation Delay Write Enable Input to Output	Figure 1		40	120	ns
t_{pd1}	Low to High Propagation Delay Write Enable Input to Output	Figure 1		70	150	ns
t_{SETUP}	Minimum Set-Up Time Data In to Write Enable Input	$t_{HOLD} = 0$ ns Figure 1	45	20		ns
t_{pWH}, t_{pWL}	Minimum Write Enable Pulse Width	Figure 1	60	25		ns
t_{THL}	High to Low Output Transition Time	Figure 1		16	35	ns
t_{TLH}	Low to High Output Transition Time	Figure 1		38	70	ns
C_{IN}	"N" Package Note 4			5	15	pF

AC Electrical Characteristics DP7311/DP8311: $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0}	High to Low Propagation Delay Data In to Output	Figure 2		30	60	ns
t_{pd1}	Low to High Propagation Delay Data In to Output	Figure 2		70	100	ns
t_{SETUP}	Minimum Set-Up Time Data In to Strobe Input	$t_{HOLD} = 0$ ns Figure 2	0	−25		ns
t_{pWL}	Minimum Strobe Enable Pulse Width	Figure 2	60	35		ns
t_{pdC}	Propagation Delay Clear to Data Output	Figure 2		70	135	ns
t_{pWC}	Minimum Clear Input Pulse Width	Figure 2	60	25		ns
t_{THL}	High to Low Output Transition Time	Figure 2		20	35	ns
t_{TLH}	Low to High Output Transition Time	Figure 2		38	60	ns
C_{IN}	Input Capacitance — Any Input	Note 4		5	15	pF

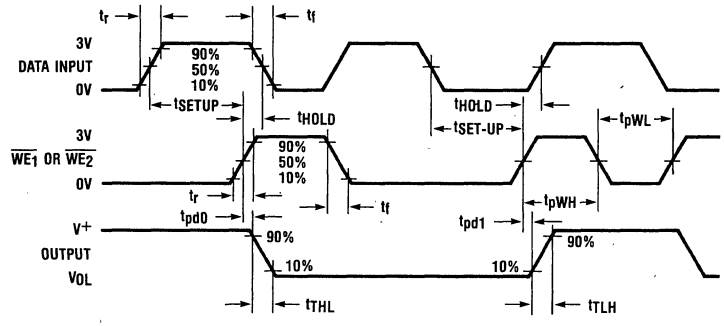
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min./max. limits apply across the −55°C to +125°C temperature range for the DP7310/DP7311 and across the 0°C to +70°C for the DP8310/DP8311. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

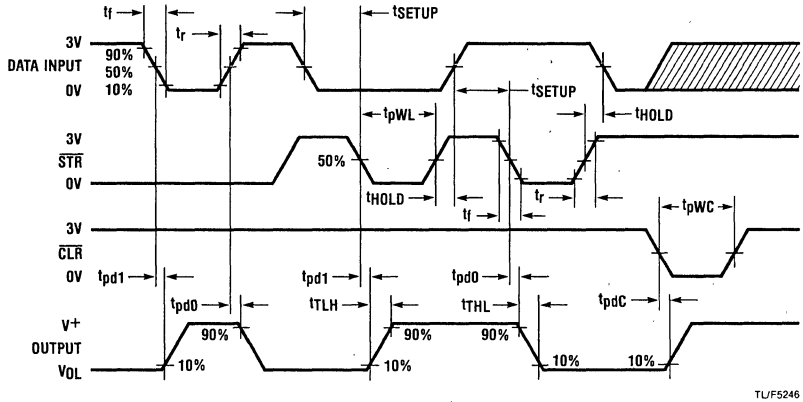
Note 4: Input capacitance is guaranteed by periodic testing. $f_{TEST} = 10$ kHz at 300 mV, $T_A = 25°C$

Switching Time Waveform DP7310/DP8310



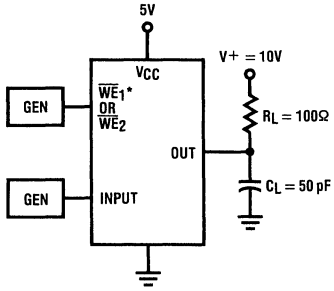
TL/F5246

Switching Time Waveform DP7311/DP8311



TL/F5246

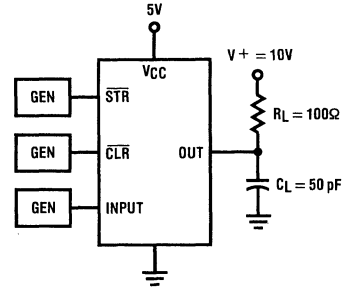
Switching Time Test Circuits DP7310/DP8310 DP7311/DP8311



*WE1 = 0V WHEN THE INPUT = WE2

TL/F5246

FIGURE 1



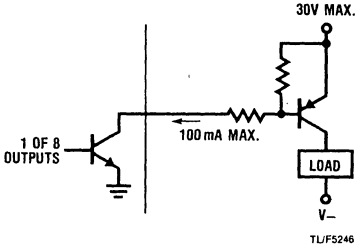
PULSE GENERATOR CHARACTERISTICS:
$Z_O = 50\Omega$, $t_r = t_f = 5$ ns

TL/F5246

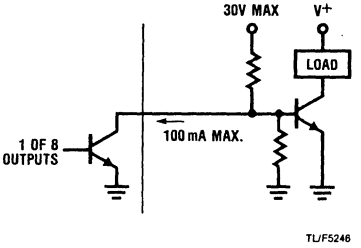
FIGURE 2

Typical Applications DP8310/11 Buffering High Current Device (Notes 1 and 2)

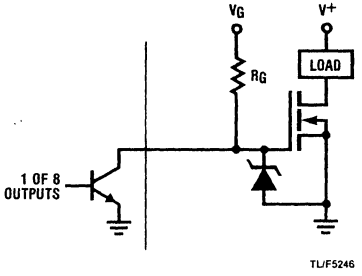
PNP High Current Driver



NPN High Current Driver

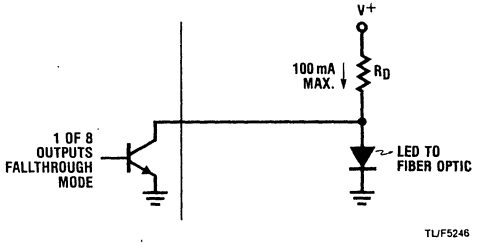


VMOS High Current Driver

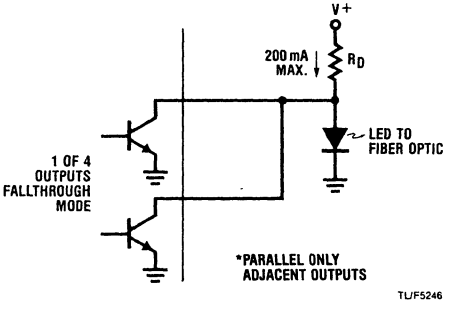


Eight Output/Four Output Fiber Optic LED Driver

DP8311 100 mA Drivers

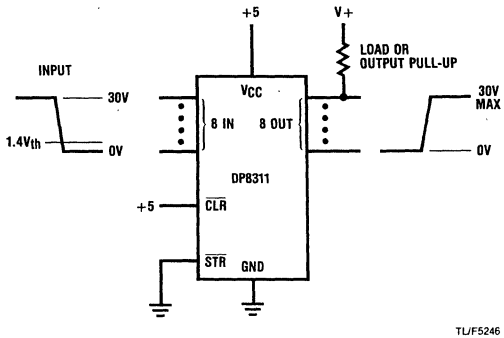


DP8311 Parallel Outputs (200 mA) Drivers*

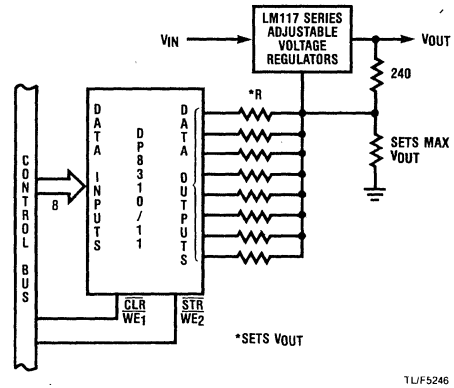


Typical Applications (cont'd)

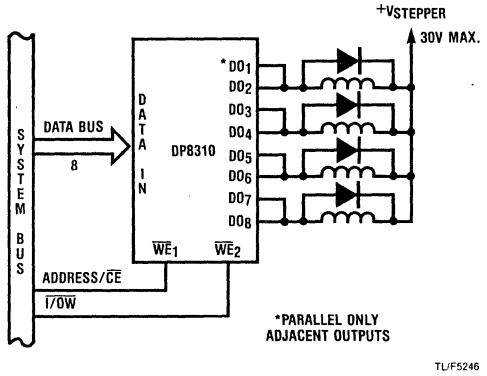
8-Bit Level Translator-Driver



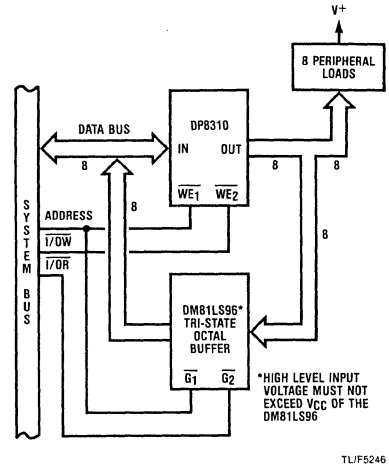
Digital Controlled 256 Level Power Supply from 1.2 Volts to 30 Volts



200 mA Drive for a 4 Phase Bifilar Stepper Motor



Reading the State of the Latched Peripherals



Note 1: Always use good V_{CC} bypass and ground techniques to suppress transients caused by peripheral loads.

Note 2: Printed circuit board mounting is required if these devices are operated at maximum rated temperature and current (all outputs on DC).

National Semiconductor

DS1611/DS3611, DS1612/DS3612, DS1613/DS3613, DS1614/DS3614 Dual Peripheral Drivers

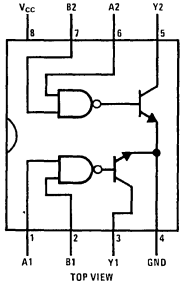
General Description

The DS1611 series of dual peripheral drivers was designed for those applications where a higher breakdown voltage is required than that provided by the DS75451 series. The pin outs for the circuits are identical to those of the DS75451 through DS75454. The DS1611 series parts feature high voltage outputs (80V breakdown in the "OFF" state) as well as high current (300 mA in the "ON" state). Typical applications include power drivers, relay drivers, lamp drivers, MOS drivers, and memory drivers.

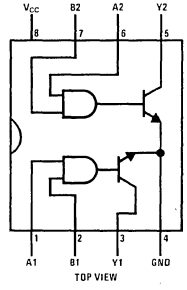
Features

- 300 mA output current capability per driver
- High voltage outputs (80V)
- TTL compatible
- Input clamping diodes
- Choice of logic function

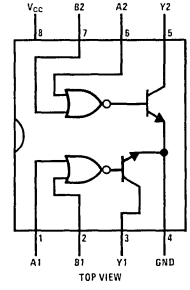
Connection Diagrams (Dual-In-Line and Metal Can Packages)



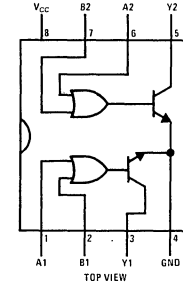
Order Number DS1611J-8, DS3611J-8 or DS3611N



Order Number DS1612J-8, DS3612J-8 or DS3612N

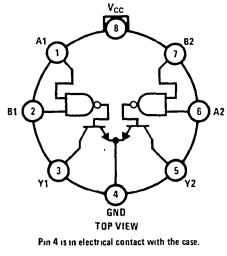


Order Number DS1613J-8, DS3613J-8 or DS3613N

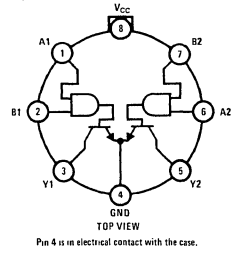


Order Number DS1614J-8, DS3614J-8 or DS3614N

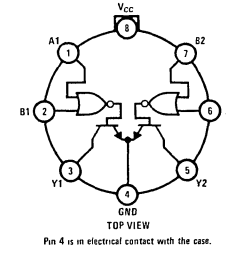
See NS Package J08A or N08A



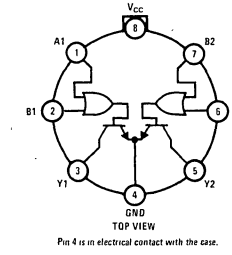
Order Number DS1611H or DS3611H



Order Number DS1612H or DS3612H



Order Number DS1613H or DS3613H



Order Number DS1614H or DS3614H

See NS Package H08C

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage (Note 5)	80V
Continuous Output Current	300 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
TO-5 Package	787 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS161X	4.5	5.5	V
DS361X	4.75	5.25	V
Temperature (T_A)			
DS161X	−55	+125	°C
DS361X	0	+70	°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C; derate TO-5 package 5.25 mW/°C above 25°C.

Electrical Characteristics DS1611/DS3611, DS1612/DS3612, DS1613/DS3613, DS1614/DS3614 (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	*(Figure 1)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*				−1.2	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, *(Figure 1)*	DS1611, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS1612, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS1613, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS1614, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS3611, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
			DS3612, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
			DS3613, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
			DS3614, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
V_{OH}	Output Breakdown Voltage	V_{CC} = Min, *(Figure 1)*	V_{IH} = 2V, I_{OH} = 300 μA	DS1611, DS1613	80			V
			V_{IH} = 2V, I_{OH} = 100 μA	DS3611, DS3613	80			V
			V_{IL} = 0.8V, I_{OH} = 300 μA	DS1612, DS1614	80			V
			V_{IL} = 0.8V, I_{OH} = 100 μA	DS3612, DS3614	80			V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 2)*					1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 2)*					40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*				−1	−1.6	mA
I_{CCH}	Supply Current	V_{CC} = Max, Outputs High, *(Figures 4 and 5)*	V_I = 5V	DS1611/ DS3611			11	mA
				DS1613/ DS3613			14	mA
			V_I = 0V	DS1612/ DS3612			14	mA
				DS1614/ DS3614			17	mA
I_{CCL}	Supply Current	V_{CC} = Max, Outputs Low, *(Figures 4 and 5)*	V_I = 0V	DS1611/ DS3611			69	mA
				DS1613/ DS3613			73	mA
			V_I = 5V	DS1612/ DS3612			71	mA
				DS1614/ DS3614			79	mA

Switching Characteristics V_{CC} = 5.0V, T_A = 25°C

DS1611/DS3611, DS1612/DS3612, DS1613/DS3613, DS1614/DS3614

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PD1}	Propagation Delay Time, Low-To-High Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 6)*	DS1611/ DS3611		130		ns
			DS1612/ DS3612		110		ns
			DS1613/ DS3613		125		ns
			DS1614/ DS3614		220		ns
t_{PD0}	Propagation Delay Time, High-To-Low Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 6)*	DS1611/ DS3611		125		ns
			DS1612/ DS3612		110		ns
			DS1613/ DS3613		125		ns
			DS1614/ DS3614		150		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS3611, DS3612, DS3613, DS3614, and −55°C to +125°C temperature range for the DS1611, DS1612, DS1613 and DS1614. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

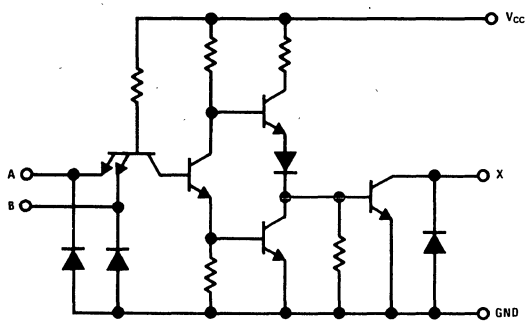
Note 4: Maximum junction temperature is 150°C.

Note 5: Maximum voltage to be applied to either output in the "OFF" state.

Note 6: Delay is measured with a 50Ω load to 10V, 15 pF load capacitance, measured from 1.5V input to 50% point on output.

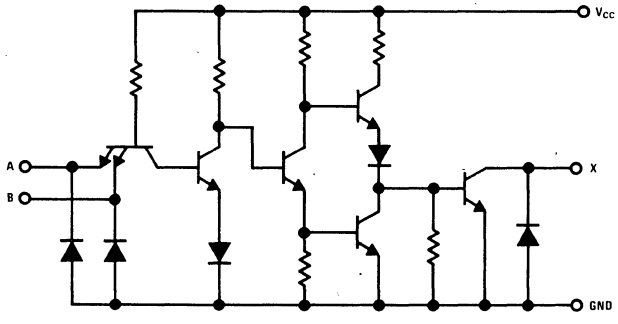
Schematic Diagrams (each driver)

DS3611 Dual AND Peripheral Driver



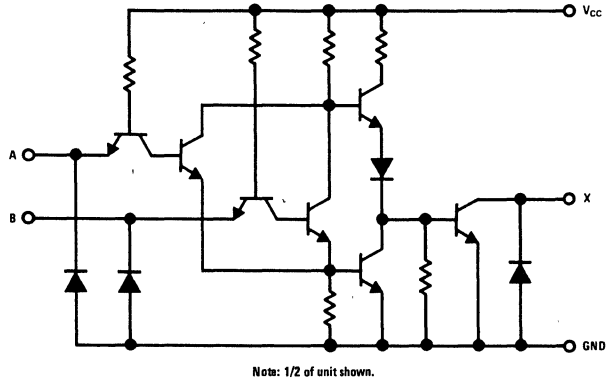
Note: 1/2 of unit shown.

DS3612 Dual NAND Peripheral Driver



Note: 1/2 of unit shown.

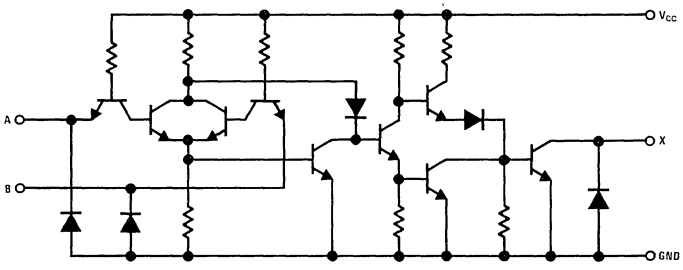
DS3613 Dual OR Peripheral Driver



Note: 1/2 of unit shown.

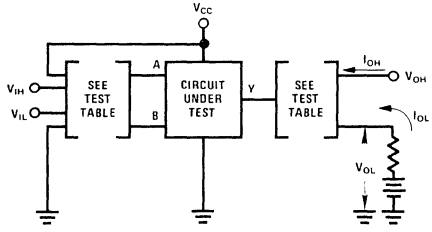
Schematic Diagrams (Continued)

DS3614 Dual NOR Peripheral Driver



Note: 1/2 of unit shown.

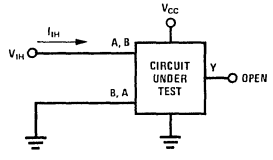
Test Circuits



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS3611	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OH} I_{OL}	V_{OH} V_{OL}
DS3612	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} I_{OH}	V_{OL} V_{OH}
DS3613	V_{IH} V_{IL}	GND V_{IL}	I_{OH} I_{OL}	V_{OH} V_{OL}
DS3614	V_{IH} V_{IL}	GND V_{IL}	I_{OL} I_{OH}	V_{OL} V_{OH}

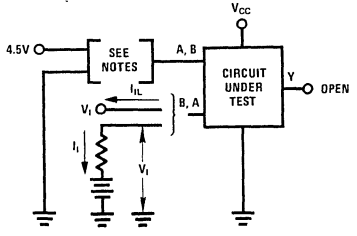
NOTE: Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, V_{OH}, V_{OL}



Each input is tested separately.

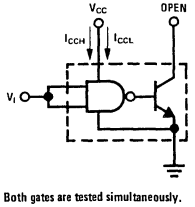
FIGURE 2. I_I, I_{IH}



Note 1: Each input is tested separately.

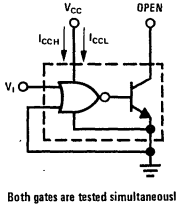
Note 2: When testing DS3613 and DS3614 input not under test is grounded. For all other circuits it is at 4.5V.

FIGURE 3. V_I, I_{IL}



Both gates are tested simultaneously.

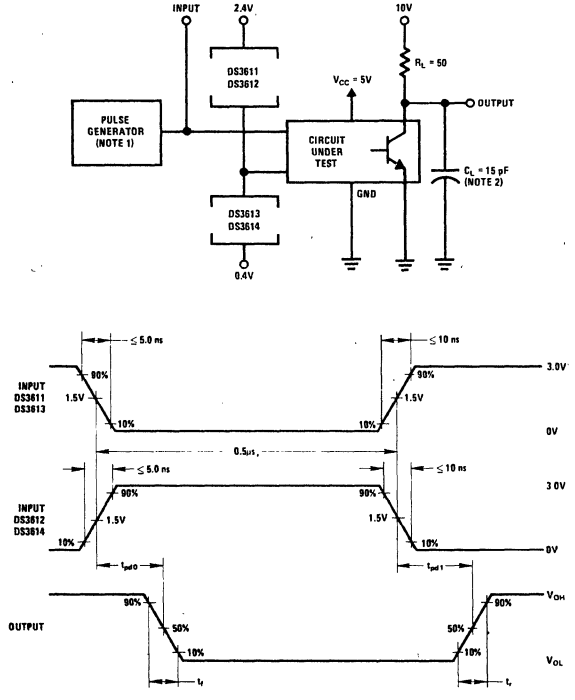
FIGURE 4. I_{CCH}, I_{CCL} for AND, NAND Circuits



Both gates are tested simultaneously.

FIGURE 5. I_{CCH}, I_{CCL} for OR, NOR Circuits

Test Circuit and Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 6. Switching Times of Complete Drivers

National Semiconductor

DS3616 Bubble Memory Coil Driver

General Description

The DS3616 bubble memory coil driver provides the function of driving the high current coils of a bubble memory device. The control inputs A, B, $\overline{CS}$ and HLD-EN are TTL compatible to insure easy interfacing to MOS control circuits. Internal logic controls the output sinking and sourcing transistors to drive the X and Y bubble memory coils in a bridged push-pull configuration.

Sourcing transistors are driven into saturation by the on-chip voltage booster for maximum current drive to the coil.

The internal power up/down control circuit prevents glitches and noise on the outputs during system initialization.

$\overline{CS}$ enables the output drive transistors. A pause capability is available from the HLD-EN input to allow asynchronous operation (refer to Typical Applications data).

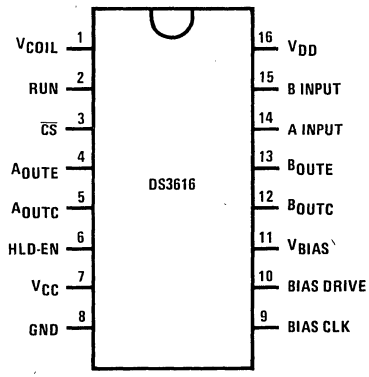
The DS3616 is characterized to operate from 0°C to 70°C.

Features

- Two high current push-pull outputs
- TTL compatible low current inputs
- Two power supplies + 5V and +12V
- Internal clamp diodes
- Power up/down control circuit
- Optional internal voltage booster
- Run output for function driver control

Connection Diagram

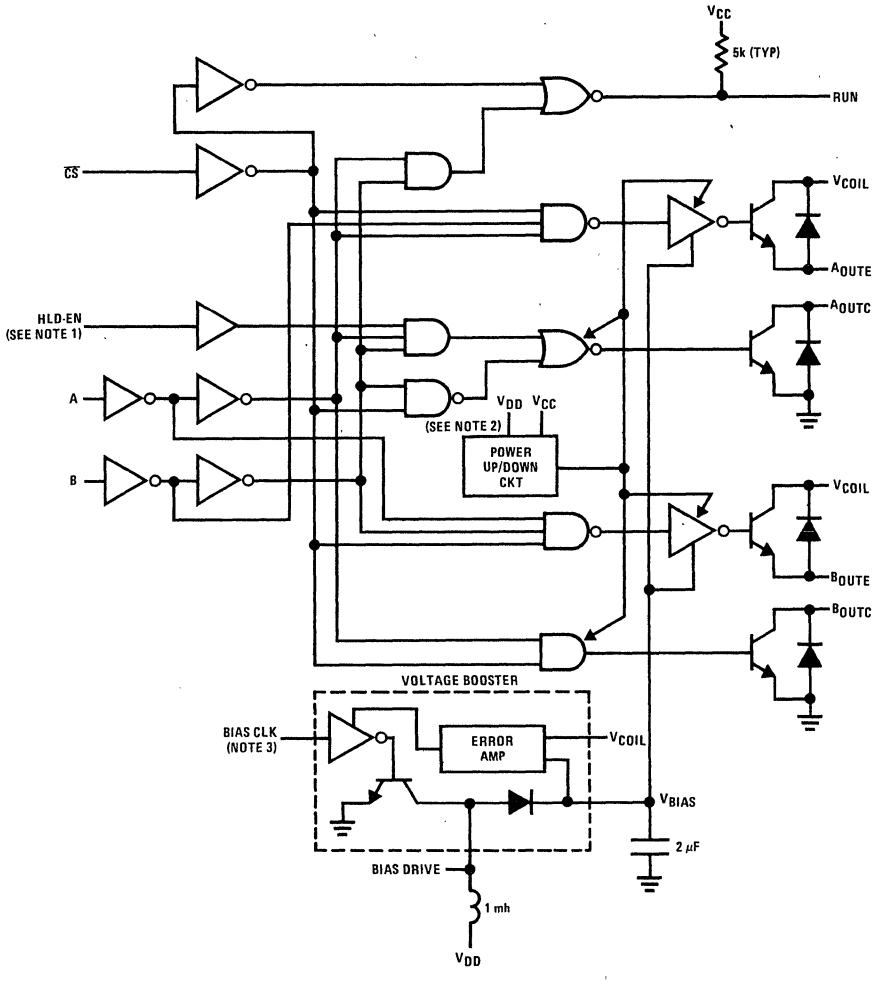
Dual-In-Line Package



TOP VIEW

Order Number DS3616N
See NS Package N16A

Functional Block Diagram



Functional Tables (Note 2)

HLD-EN = 0					
A	B	$\overline{CS}$	A_{OUT}	B_{OUT}	Run
X	X	1	Z	Z	0
0	0	0	Z	Z	1
0	1	0	0	1	1
1	0	0	1	0	1
1	1	0	0	0	0

HLD-EN = 1					
A	B	$\overline{CS}$	A_{OUT}	B_{OUT}	Run
X	X	1	Z	Z	0
0	0	0	Z	Z	1
0	1	0	0	1	1
1	0	0	1	0	1
1	1	0	Z	0	0

Note 1: When used as Y driver, HLD-EN is in Logic "0" state.

Note 2: Run output is independent of the power-up clear circuit and functions down to $V_{CC} = 3V$. (See Typical Applications.)

Note 3: If BIAS CLK stops, it must remain in a Logic "1" state to prevent excessive DC current in the inductor.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	7V
Supply Voltage (V_{DD})	15V
Coil Source Voltage (V_{COIL})	14V
V_{BIAS}–V_{COIL}	6.5V
Peak Output Current (Coil Outputs)	1A
V_{BIAS} Drive Current	300 mA
Maximum Power Dissipation* at 25°C Molded Package	1950 mW

*Derate molded package 15.6 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Typ	Max	Units
T_A Operating Temperature	0		70	°C
Supply Voltage (V_{CC})	4.75 (4.5)**	5	5.25	V
Supply Voltage (V_{DD})	11.4 (10.8)**	12	12.6	V
Coil Source Voltage (V_{COIL})	7	10	13.5	V
V_{BIAS}–V_{COIL}	4.0	4.8	6	V
Peak Coil Output Current			950	mA
Peak V_{BIAS} Drive Current			200	mA

** Min supply voltage for functionality during power up/down sequences.

Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage	$V_{CC} = 4.75V$	2.0			V
V_{IL}	Low Level Input Voltage	$V_{CC} = 4.75V$			0.8	V
V_{OD}	Differential Output Voltage	$I_O = 850$ mA, $V_{COIL} = 13.5V$, $V_{BIAS} = 18.5V$, $V_{CC} = 4.75V$, $V_{DD} = 11.4V$	11.7	12.2	12.7	V
V_{OCLAMP}	Output Clamp Diode Voltage	$I_O = -850$ mA, Lower Clamp	−0.9		−1.5	V
		$I_O = 850$ mA, Upper Clamp	0.9		1.5	V
V_{ICLAMP}	Input Clamp Diode Voltage	$I_I = -12$ mA		−0.9	−1.5	V
V_{OHR}	Run High Level Output Voltage	$I_{OH} = -400\ \mu A$, $V_{CC} = 4.75V$	2.4	3.3		V
		$I_{OH} = -100\ \mu A$, $V_{CC} = 4.75V$	3.5	4.1	4.45	V
V_{OLR}	Run Low Level Output Voltage	$I_{OL} = 5$ mA, $V_{CC} = 4.75V$		0.2	0.5	V
I_I	Maximum Input Current at Maximum Input Voltage	$V_{CC} = 5.25V$, $V_{IN} = 5.5V$		1	100	μA
I_{IH}	High Level Input Current	$V_{CC} = 5.25V$, $V_{IN} = 2.4V$		1	40	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.25V$, $V_{IL} = 0.4V$		−160	−250	μA
V_{CCEN}	V_{CC} Power Up Enable Voltage		3.2	3.8	4.4	V
V_{DDEN}	V_{DD} Power Up Enable Voltage		8.0	9.5	10.5	V
V_{BIAS}	Regulator Threshold Voltage	$V_{COIL} = 10V$, $V_{DD} = 12V$, $V_{CC} = 5V$	14.0	14.8	16	V
V_F	Bias Diode Voltage	$I_F = 100$ mA		0.9	1.5	V
I_R	Bias Diode Leakage Current	$V_{REVERSE} = 20V$		5	500	μA
V_{OL}	$V_{CE(SAT)}$ of V_{BIAS} Output Transistor	$V_{CC} = 4.75V$, Bias Drive = 100 mA		0.3	0.6	V
I_{OFF}	Leakage Current of V_{BIAS} Output Transistor	$V_{OH} = 20V$		5	500	μA
I_{LCU}	Leakage Current of the Upper Drive	$V_{COIL} = 13.5V$, $V_{OUT} = 0V$		10	1000	μA
I_{LCL}	Leakage Current of the Lower Drive	$V_{OUT} = 15V$		10	1000	μA
$I_{CC1(E)}$	V_{CC} Supply Current Chip Enabled	A = 3.0V, B = 0.4V, $\overline{CS} = 0.4V$, HLD-EN = 0.4V, $V_{CC} = 5.25V$		55	90	mA
$I_{CC0(D)}$	V_{CC} Supply Current Chip Disabled	A = B = HLD-EN = 0.4V, $\overline{CS} = 3.0V$, $V_{CC} = 5.25V$		17	33	mA
I_{DD}	V_{DD} Supply Current	$V_{DD} = 12.6V$		4.5	7	mA
$I_{BIAS1(E)}$	V_{BIAS} Current Chip Enabled	$V_{BIAS} = 18.5V$, $V_{COIL} = 13.5V$ Same Input Conditions as I_{CC1}		40	60	mA
$I_{BIAS0(D)}$	V_{BIAS} Current Chip Disabled	$V_{BIAS} = 18.5V$, $V_{COIL} = 13.5V$ Same Input Conditions as I_{CC0}		5	8	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to 70°C temperature range for the DS3616. $V_{CC} = 5V \pm 5\%$, $V_{DD} = 12V \pm 5\%$. During power up/down, for functional operation, $V_{CC} = +5\%, -10\%$; $V_{DD} = +5\%, -10\%$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Switching Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 4.75V$, $V_{DD} = 11.4V$

Parameter		Conditions	Min	Typ	Max	Units
$t_{R(E)}$	Rise Time for A_{OUT} or B_{OUT} Emitters	*Figure 1*		40	100	ns
$t_{F(E)}$	Fall Time for A_{OUT} or B_{OUT} Emitters			15	50	ns
$t_{R(C)}$	Rise Time for A_{OUT} or B_{OUT} Collectors	*Figure 2*		15	50	ns
$t_{F(C)}$	Fall Time for A_{OUT} or B_{OUT} Collectors			25	50	ns
$t_{ON(E)}$	Turn ON Time for A_{OUT} or B_{OUT} Emitters	*Figure 1*		85	150	ns
$t_{OFF(E)}$	Turn OFF Time for A_{OUT} or B_{OUT} Emitters			45	120	ns
$t_{ON(C)}$	Turn ON Time for A_{OUT} or B_{OUT} Collectors	*Figure 2*		70	150	ns
$t_{OFF(C)}$	Turn OFF Time for A_{OUT} or B_{OUT} Collectors			55	120	ns
$t_{CSON(E)}$	Time for $\overline{CS}$ to Enable Output Emitters	*Figure 3*		70	150	ns
$t_{CSOFF(E)}$	Time for $\overline{CS}$ to TRI-STATE® Output Emitters			50	120	ns
$t_{CSON(C)}$	Time for $\overline{CS}$ to Enable Output Collectors	*Figure 4*		50	120	ns
$t_{CSOFF(C)}$	Time for $\overline{CS}$ to TRI-STATE Output Collectors			60	120	ns
$t_{R(RUN)}$	Rise Time for Run Output	*Figure 5*		50	70	ns
$t_{F(RUN)}$	Fall Time for Run Output			10	20	ns
$t_{ON(RUN)}$	Turn ON Time for Run Output			70	110	ns
$t_{OFF(RUN)}$	Turn OFF Time for Run Output			40	70	ns
t_{PLZ}	Propagation Delay for HLD-EN to TRI-STATE A_{OUT} Collector	*Figure 6*		65	120	ns
t_{PZL}	Propagation Delay for HLD-EN Turn ON A_{OUT} Collector			45	120	ns
t_{CHARGE}	Charge Up Time for V_{BIAS}	1 mh, 2 μF, $f_{CLK} = 800$ kHz		2	5	ms
t_{dON}	Turn ON Time of Clamp Diodes	*Figure 7*		30	50	ns
IMB	DC Imbalance under AC Conditions	*Figure 8*		±0.1		V
BIAS CLK	Duty Cycle		40	50	60	%
	Frequency		600	800	1000	kHz

TRI-STATE® is a registered trademark of National Semiconductor Corp.

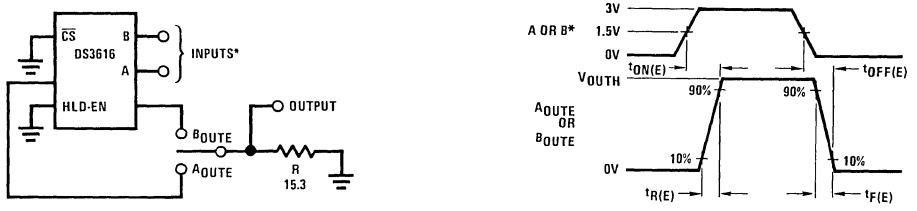
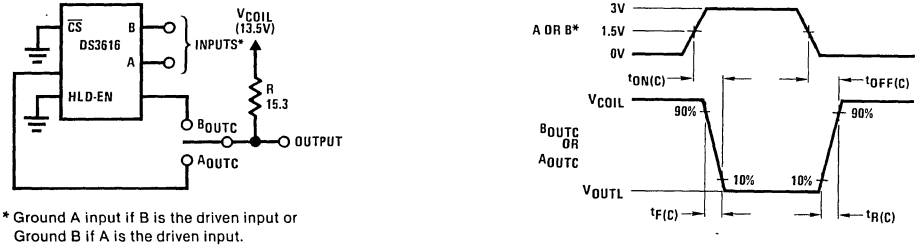
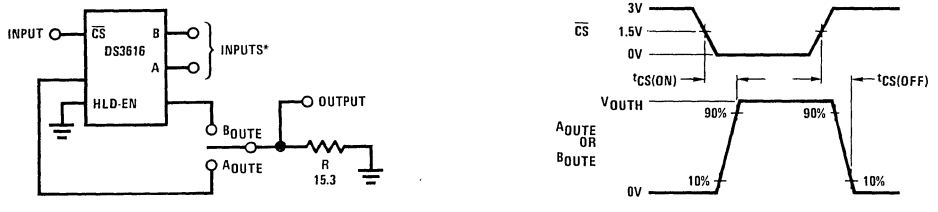


FIGURE 1. Test Set-Up and Timing Waveforms for A_{OUT} and B_{OUT} Emitters



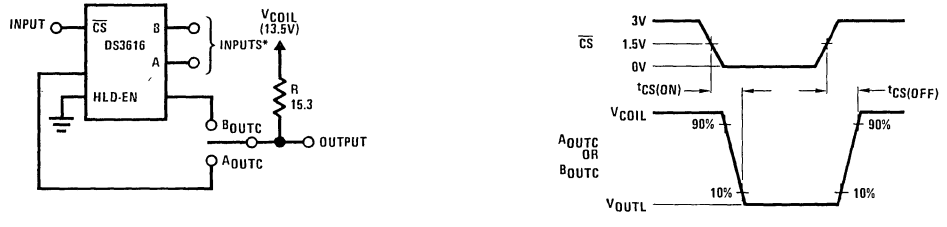
* Ground A input if B is the driven input or Ground B if A is the driven input.

FIGURE 2. Test Set-Up and Timing Waveforms for A_{OUT} and B_{OUT} Collectors



* For A_{OUTE} and B_{OUTC}, A = 3V, B = 0V; for B_{OUTE} and A_{OUTC}, A = 0V, B = 3V.

FIGURE 3. Test Set-Up and Timing Waveforms for A_{OUT} and B_{OUT} Emitters



* For A_{OUTE} and B_{OUTC}, A = 3V, B = 0V; for B_{OUTE} and A_{OUTC}, A = 0V, B = 3V.

FIGURE 4. Test Set-Up and Timing Waveforms for A_{OUT} and B_{OUT} Collectors

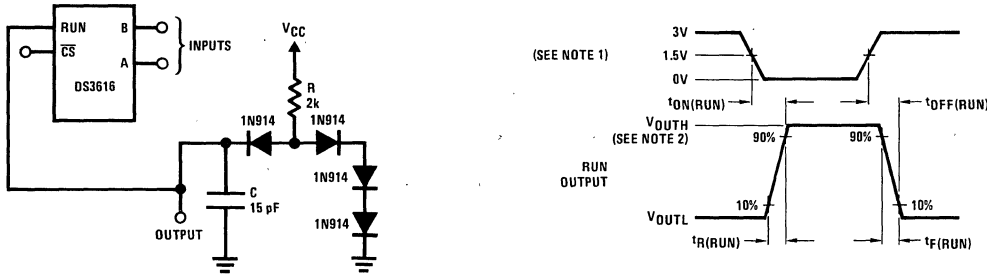
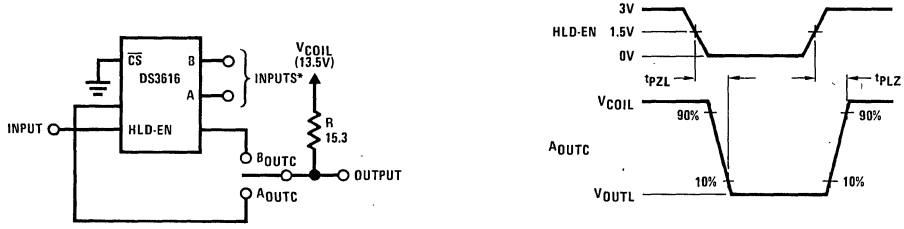


FIGURE 5. Test Set-Up and Timing Waveforms for Run Output



*Input Conditions: A = B = 3V

FIGURE 6. Test Set-Up and Timing Waveforms for A_{OUTC} TRI-STATE

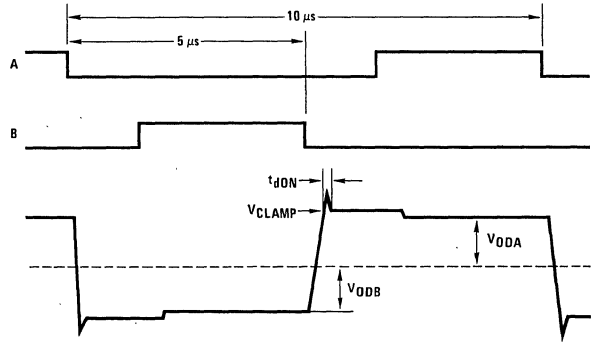


FIGURE 7. AC Switching Characteristics

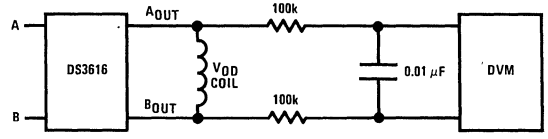


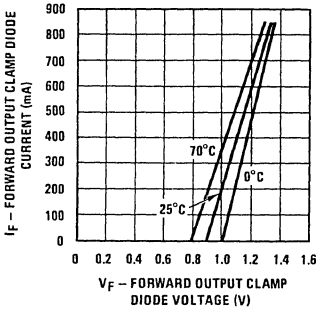
FIGURE 8. DC Imbalance Test Circuit

Note 1: Output waveforms may be generated with $\overline{CS}$ = input, A = B = 0V or B = input, A = 3V, $\overline{CS}$ = 0V

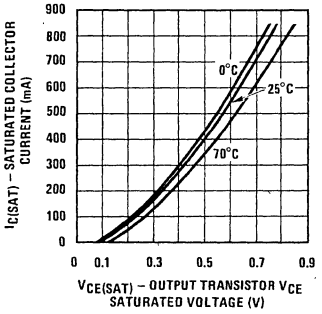
Note 2: Reference V_{OUTH} is set at 4V, which includes the active pull-up voltage plus charge-up voltage due to the internal 5 kΩ resistor to V_{CC} (typical rise time = 12 ns).

Typical Characteristics

I_F vs V_F of Output Clamp Diode Over Ambient Temperature



$I_{C(SAT)}$ vs $V_{CE(SAT)}$ of Output Transistors Over Ambient Temperature



Typical Applications *(Figures 9 and 10)*

The coil driver circuit is used to generate triangular current waveforms for the bubble memory coils. The currents are generated by switching the coil driver in such a way that a voltage pulse is applied to the coil. The coil inductance integrates the voltage into a current ramp. When the pulse is switched OFF the current is commutated by two on-chip clamp diodes and current ramps down to zero. At that time the opposite polarity pulse is applied to the coil, which causes the current to ramp in the opposite direction.

The Run output drives the chip enable input of the function driver (DS3615). It goes low when A = B = 1, indicating the controller has stopped the coils, or when $\overline{CS} = 1$ indicating the bubble is not selected. In the event of a system power loss, A and B are to be set to logic 1 by the controller. This stops the coil driver and causes the Run output to go to zero which disables the function driver. The Run output is guaranteed to stay at Logic "0" and coil drive outputs in Logic "0" state or high impedance condition (if A = B = 1 or $\overline{CS} = 1$) down to $V_{CC} = 3V$, at which time the function driver and coil driver power supply sensors will have disabled all outputs driving the bubble.

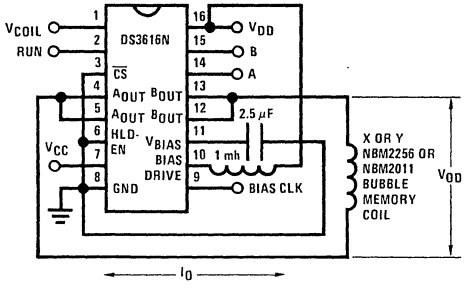


FIGURE 9. Typical Application

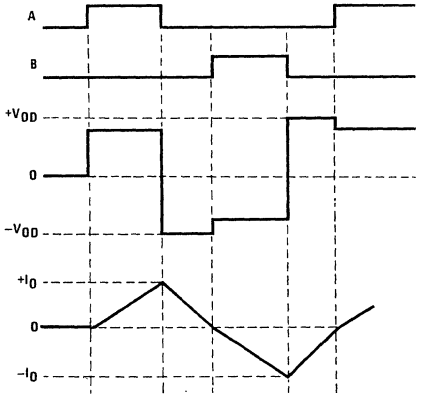


FIGURE 10. Coil Current and Voltage Waveforms

National Semiconductor

DS1631/DS3631, DS1632/DS3632, DS1633/DS3633, DS1634/DS3634 CMOS Dual Peripheral Drivers

General Description

The DS1631 series of dual peripheral drivers was designed to be a universal set of interface components for CMOS circuits.

Each circuit has CMOS compatible inputs with thresholds that track as a function of V_{CC} (approximately 1/2 V_{CC}). The inputs are PNPs providing the high impedance necessary for interfacing with CMOS.

Outputs have high voltage capability, minimum breakdown voltage is 56V at 250μA.

The outputs are Darlington connected transistors. This allows high current operation (300 mA max) at low internal V_{CC} current levels since base drive for the output transistor is obtained from the load in proportion to the required loading conditions. This is essential in order to minimize loading on the CMOS logic supply.

Typical V_{CC} = 5V power is 28 mW with both outputs ON. V_{CC} operating range is 4.5V to 15V.

The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance OFF state with the same breakdown levels as when V_{CC} was applied.

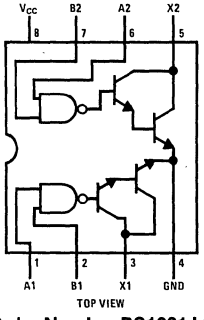
Pin-outs are the same as the respective logic functions found in the following popular series of circuits: DS75451, DS75461, DS3611. This feature allows direct conversion of present systems to the MM74C CMOS family and DS1631 series circuits with great power savings.

The DS1631 series is also TTL compatible at V_{CC} = 5V.

Features

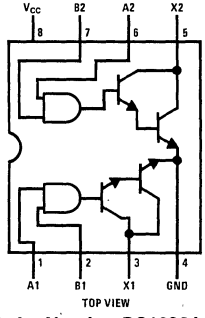
- CMOS compatible inputs
- TTL compatible inputs
- High impedance inputs — PNP's
- High output voltage breakdown — 56V min
- High output current capability — 300 mA max
- Same pin-outs and logic functions as DS75451, DS75461 and DS3611 series circuits
- Low V_{CC} power dissipation (28 mW both outputs "ON" at 5V)

Connection Diagrams (Dual-In-Line and Metal Can Packages)



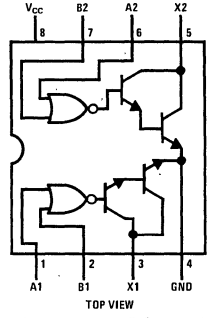
TOP VIEW

Order Number DS1631J-8, DS3631J-8 or DS3631N



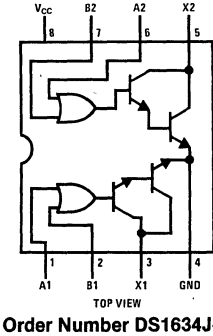
TOP VIEW

Order Number DS1632J-8, DS3632J-8 or DS3632N



TOP VIEW

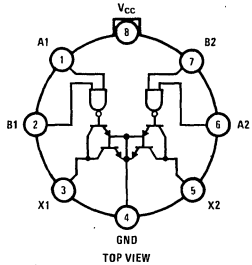
Order Number DS1633J-8, DS3633J-8 or DS3633N



TOP VIEW

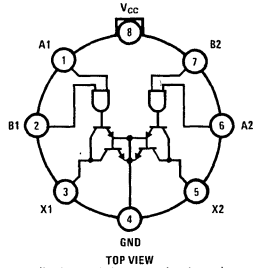
Order Number DS1634J-8, DS3634J-8 or DS3634N

See NS Package J08A or N08A



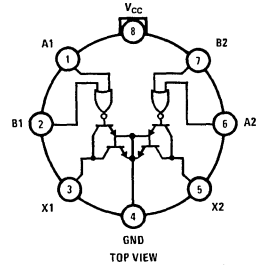
TOP VIEW
(Pin 4 is electrically connected to the case.)

Order Number DS1631H or DS3631H



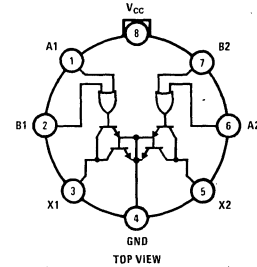
TOP VIEW
(Pin 4 is electrically connected to the case.)

Order Number DS1632H or DS3632H



TOP VIEW
(Pin 4 is electrically connected to the case.)

Order Number DS1633H or DS3633H



TOP VIEW
(Pin 4 is electrically connected to the case.)

Order Number DS1634H or DS3634H

See NS Package H08C

Absolute Maximum Ratings (Note 1)

Supply Voltage	16V
Voltage at Inputs	−0.3V to V_{CC} +0.3V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
TO-5 Package	787 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C; derate TO-5 package 5.2 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1631/DS1632/ DS1633/DS1634	4.5	15	V
DS3631/DS3632/ DS3633/DS3634	4.75	15	V
Temperature, T_A			
DS1631/DS1632/ DS1633/DS1634	−55	+125	°C
DS3631/DS3632/ DS3633/DS3634	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
ALL CIRCUITS								
V_{IH}	Logical "1" Input Voltage	*(Figure 1)*	V_{CC} = 5V		3.5	2.5		V
			V_{CC} = 10V		8.0	5		V
			V_{CC} = 15V		12.5	7.5		V
V_{IL}	Logical "0" Input Voltage	*(Figure 1)*	V_{CC} = 5V			2.5	1.5	V
			V_{CC} = 10V			5.5	2.0	V
			V_{CC} = 15V			7.5	2.5	V
I_{IH}	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V, *(Figure 2)*				0.1	10	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, *(Figure 3)*	V_{CC} = 5V			−50	−120	μA
			V_{CC} = 15V			−200	−360	μA
V_{OH}	Output Breakdown Voltage	V_{CC} = 15V, I_{OH} = 250 μA, *(Figure 1)*			56	65		V
V_{OL}	Output Low Voltage	V_{CC} = Min, *(Figure 1)*, DS1631, DS1632, DS1633, DS1634	I_{OL} = 100 mA			0.85	1.1	V
			I_{OL} = 300 mA			1.1	1.4	V
		V_{CC} = Min, *(Figure 1)*, DS3631, DS3632, DS3633, DS3634	I_{OL} = 100 mA			0.85	1.0	V
			I_{OL} = 300 mA			1.1	1.3	V
DS1631/DS3631								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output Low		7	11	mA
			V_{CC} = 15V	Both Drivers		14	20	mA
$I_{CC(1)}$		*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output High		2	3	mA
			V_{CC} = 15V, V_{IN} = 15V	Both Drivers		7.5	10	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				200		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
DS1632/DS3632								
$I_{CC(0)}$	Supply Currents	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output Low		8	12	mA
			V_{CC} = 15V, V_{IN} = 15V			18	23	mA
$I_{CC(1)}$		V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output High		2.5	3.5	mA
			V_{CC} = 15V			9	14	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
DS1633/DS3633								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output Low		7.5	12	mA
			V_{CC} = 15V			16	23	mA
$I_{CC(1)}$		*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output High		2	4	mA
			V_{CC} = 15V, V_{IN} = 15V			7.2	15	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				200		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns

Electrical Characteristics (Continued)

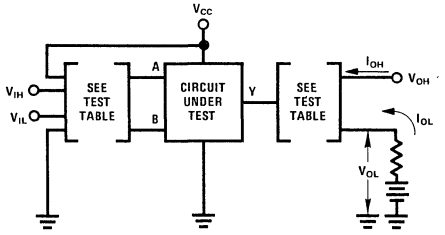
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DS1634/DS3634								
$I_{CC(0)}$	Supply Currents	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output Low		7.5	12	mA
			V_{CC} = 15V, V_{IN} = 15V			18	23	mA
$I_{CC(1)}$		V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output High		3	5	mA
			V_{CC} = 15V			11	18	mA
t_{PD1}	Propagation to "1"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
t_{PD0}	Propagation to "0"	V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1631, DS1632, DS1633 and DS1634 and across the 0°C to +70°C range for the DS3631, DS3632, DS3633 and DS3634. All typical values are for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Test Circuits



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS3631	V_{IH}	V_{IH}	I_{OH}	V_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
DS3632	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	I_{OH}	V_{OH}
DS3633	V_{IH}	GND	I_{OH}	V_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
DS3634	V_{IH}	GND	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	I_{OH}	V_{OH}

Note: Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, V_{OH}, V_{OL}

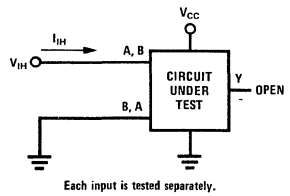
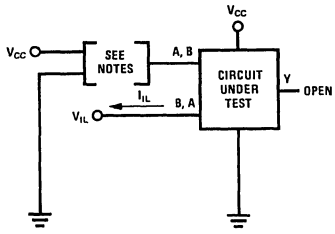


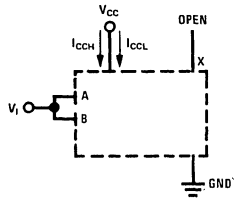
FIGURE 2. I_{IH}

Test Circuits (Continued)



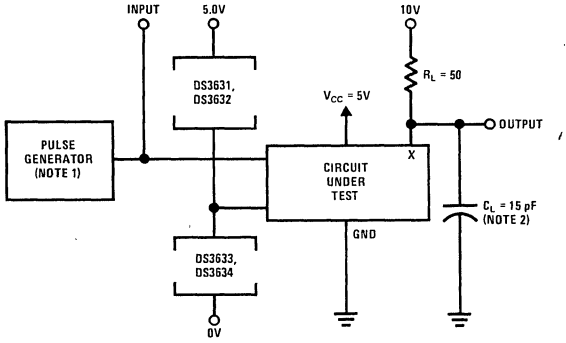
Note A: Each input is tested separately.
Note B: When testing DS1633 and DS1634 input not under test is grounded. For all other circuits it is at V_{CC}.

FIGURE 3. I_{IL}

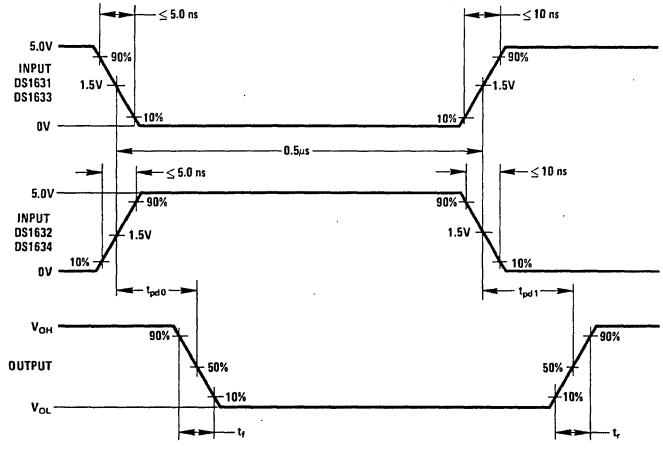


Both gates are tested simultaneously.

FIGURE 4. I_{CC}



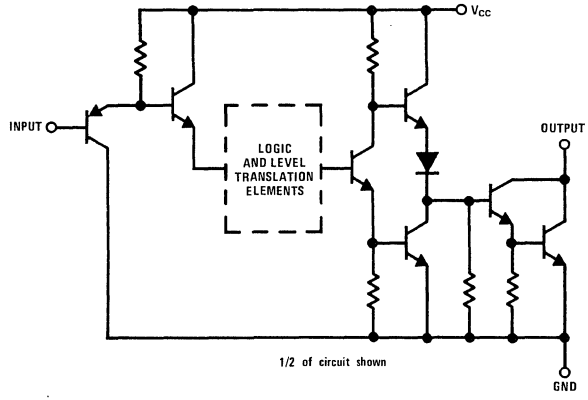
Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: PRR = 500 kHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 5. Switching Times.

Schematic Diagram (Equivalent Circuit)



DS3654 Printer Solenoid Driver

General Description

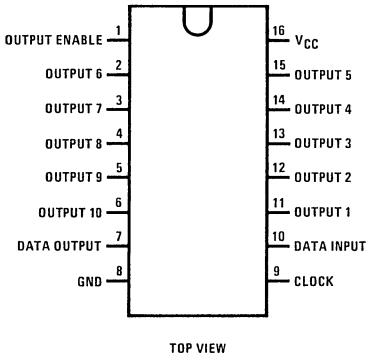
The DS3654 is a serial-to-parallel 10-bit shift register with a clock and data input, a data output from the tenth bit, and 10 open-collector clamped relay driver outputs suitable for driving printer solenoids.

Timing for the circuit is shown in *Figure 1*. Data input is sampled on the positive clock edge. Data output changes on the negative clock edge, and is always active. Enable transfers data from the shift register to the open-collector outputs. Internal circuitry inhibits output enable for power supply voltage less than 6V.

Each output sinks 250 mA and is internally clamped to ground at 50V to dissipate energy stored in inductive loads.

Connection Diagram

Dual-In-Line Package



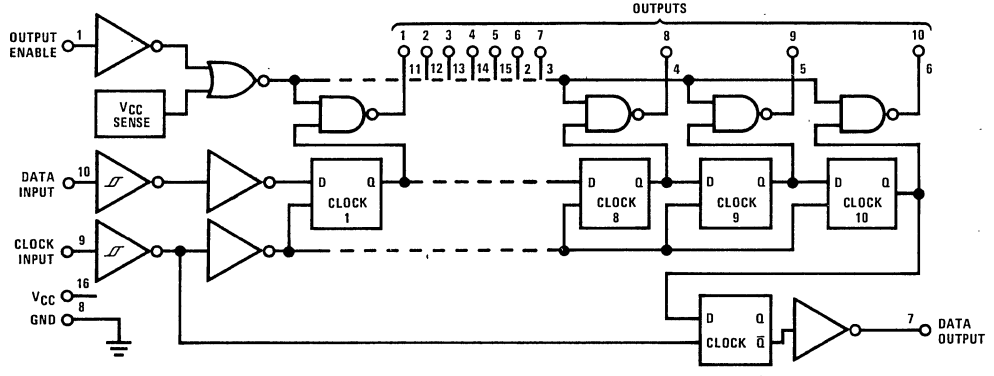
TOP VIEW

Order Number DS3654J or DS3654N
See NS Package J16A or N16A

Pin Descriptions

Pin No.	Function
1	Output Enable
2	Output 6
3	Output 7
4	Output 8
5	Output 9
6	Output 10
7	Data Output
8	Ground
9	Clock Input
10	Data Input
11	Output 1
12	Output 2
13	Output 3
14	Output 4
15	Output 5
16	V_{CC}

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	9.5V max
Input Voltage	−0.5V min. 9.5V max
Output Supply, Vp-p	45V max
Storage Temperature Range	−65°C to +150°C
Output Current (Single Output)	0.4A
Ground Current	4.0A
Peak Power Dissipation, t < 10 ms, Duty Cycle <5%	4.5W Max
Maximum Power Dissipation* at 25°C	
Cavity Package	1635 mW
Molded Package	1687 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.9 mW/°C above 25°C; derate molded package 13.5 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	7.5	9.5	V
Temperature (T_A)	0	+70	°C
Output Supply (Vp-p)		40	V

Electrical Characteristics (Notes 2, 3 and 4) Vp-p = 30V unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage		2.6			V
Logical "0" Input Voltage				0.8	V
Logical "1" Output Voltage Clamp	I_{CLAMP} = 0.1A, V_{EN} = 0V	45	50	65	V
Logical "1" Output Current	V_{OH} = 40V, V_{EN} = 0			1.0	mA
Logical "0" Output Voltage	I_{OL} = 250 mA, V_{EN} = 2.6V			1.6	V
Logical "1" Input Current					
Clock	T_A = 70°C, V_{CL} = 2.6V	0.2	0.33		mA
Enable	T_A = 70°C, V_{EN} = 2.6V	0.2	0.33		mA
Data	T_A = 70°C, V_D = 2.6V	0.3	0.57		mA
Clock	T_A = 0°C, V_{CL} = 2.6V		0.33	0.5	mA
Enable	T_A = 0°C, V_{EN} = 2.6V		0.33	0.5	mA
Data	T_A = 0°C, V_D = 2.6V		0.57	0.75	mA
Logical "0" Input Current					
Clock	T_A = 70°C, V_{CL} = 1V		125		μA
Enable	T_A = 70°C, V_{EN} = 1V		125		μA
Data	T_A = 70°C, V_D = 1V		220		μA
Input Pull-Down Resistance					
Clock	T_A = 25°C, $V_{CL} < V_{CC}$		8		kΩ
Enable	T_A = 25°C, $V_{EN} < V_{CC}$		8		kΩ
Data	T_A = 25°C, $V_D < V_{CC}$		4.5		kΩ
Supply Current (I_{CC})					
Outputs Disabled	$T_A \geq$ 25°C, V_{EN} = 0, V_{DO} = 0, V_{CC} = 9.5V		27	40	mA
Outputs Enabled	$T_A \geq$ 25°C, V_{EN} = 2.6, I_{OL} = 250 mA Each Bit		55	70	mA
Data Output Low (V_{DOL})	V_D = 0, I_{OL} = 0		0.01	0.5	V
Data Output High (V_{DOH})	V_D = 2.6, I_{OH} = −0.75 mA	2.6	3.4		V
Data Output Pull-Down Resistance	V_D = 0, V_{DO} = 1V		14		kΩ

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 7.5V to 9.5V power supply range. All typical values given are for V_{CC} = 8.5V and T_A = 25°C.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

Switching Characteristics 0°C to +70°C, T_A = 25°C, nominal power supplies unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clk, Data and Enable Inputs	*(Figure 1)*				
t_{FC}				2.0	μs
t_{RC}	$t_{BIT} \geq 10\ \mu s$			2.0	μs
t_{CLK}		2			μs
$\overline{t_{CLK}}$		3.5			μs
t_{HOLD}				1.0	μs
$t_{SET\text{-}UP}$				1.0	μs
t_{RE}, $t_{RD\ IN}$				1.0	μs
t_{FE}, $t_{FD\ IN}$				5.0	μs
Output 1–10	Vp-p = 20V				
t_{RO}	R_L = 100Ω, C_L < 100 pF		1.2		μs
t_{FO}	R_L = 100Ω, C_L < 100 pF		1.2		μs
t_{PDEH}			3.5		μs
t_{PDEL}			3.0		μs
Data Output					
t_{PDH}, t_{PDL}	R_L = 5 kΩ, $C_L \leq$ 10 pF		0.8	2.5	μs
t_{RD}			0.4		μs
t_{FD}			0.4		μs
Clock to Enable Delay					
t_{CE}		2 t_{BIT}			μs
Enable to Clock Delay		t_{BIT}			μs

Switching Time Waveforms

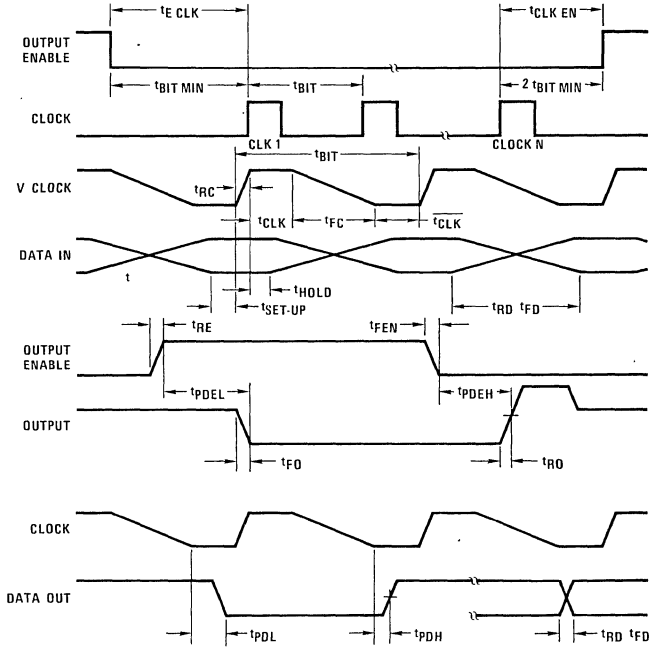


FIGURE 1. Shift Timing

Definition of Terms

V_{p-p}: Output power supply voltage. The return for open-collector relay driver outputs.

t_{BIT}: Period of the incoming clock.

V_{CLK}: The voltage at the clock input.

t_{CLK}: The portion of t_{BIT} when $V_{CLK} \geq 2.6V$.

$t_{\overline{CLK}}$: The portion of t_{BIT} when $V_{CLK} \leq 0.8V$

$t_{SET\text{-}UP}$: The time prior to the end of $t_{\overline{CLK}}$ required to insure valid data at the shift register input for subsequent clock transitions.

t_{HOLD}: The time following the start of t_{CLK} required to transfer data within the shift register.

National Semiconductor

DS3656 Quad Peripheral Driver

General Description

The DS3656 is a quad peripheral driver designed for use in automotive applications. Logically it is an open collector NAND function with all inputs compatible with 74LS and CMOS series products. An enable input is provided that is common to each driver. When taken to a logic zero level all outputs will turn off. Also, overvoltage is detected.

The DS3656 has features associated with the output structure that make it highly versatile to many applications. Each output is capable of 600 mA sink currents and offers 65V standoff voltage in non-inductive applications. A clamp network capable of handling 800 mA is incorporated in each output which eliminates the need of an external network to quench the high voltage backswing caused when switching inductive loads up to 30V (reference AN-213).

The DS3656 is intended to operate from a 12V automotive battery. Internal to the device is its own voltage regulator which permits the device to operate during the wide voltage variation seen in many automotive applications. An overvoltage-protection circuit is incorporated that will cause the outputs to turn off when the supply exceeds 30V. The circuit is designed to withstand worst case fault conditions that occur in automotive applications, such as high voltage transients and reverse battery connection. In this type of environment an external 100Ω resistor must be connected in series with the V_{CC} line.

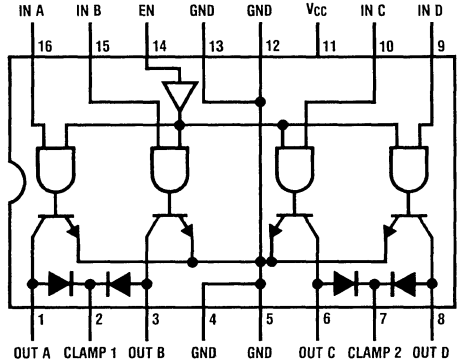
The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a copper PC board the power rating of the device will significantly improve.

Features

- Quad automotive peripheral driver
- 600 mA output current capability
- High voltage outputs — 65V
- Clamp diode provided for inductive loads
- Built in regulator
- Overvoltage failsafe
- TTL/LS/CMOS compatible diode clamped inputs
- High power dissipation package
- Guaranteed to withstand worst case fault conditions

Connection Diagram

Dual-In-Line Package



Order Number DS3656N
See NS Package N16A

Truth Table

Enable	In X	Out X
H	H	L
H	L	H
L	X	H

H = high level L = low level X = irrelevant

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC} (Note 2)	65V
Input Voltage	7V
Output Voltage	65V
Continuous Output Current	1.2A
Junction Temperature	150°C
Thermal Resistance (Junction to Ambient)	
DS3656N Plugged in a Socket	60°C/W
DS3656N Soldered in a PC Board	35°C/W
DS3656N Soldered in a PC Board with 6 in^2 Cn Foil	20°C/W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	10.5	17.0	V
Temperature	−40	105	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Power Supply Voltage		10.5	17	V
I_{CC}	Power Supply Current			65	mA
V_{IH}	High Level Input Voltage		2.0		V
V_{IL}	Low Level Input Voltage			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = 2.7V$		20	μA
I_{IL}	Low Level Input Current	$V_{IN} = 0.4V$		−360	μA
V_{ICL}	Input Clamp Voltage	$I_{IN} = -10$ mA		−1.5	V
V_{OL}	Low Level Output Voltage	$I_L = 600$ mA, $V_{CC} = 10.5V$		1.5	V
I_{OH}	High Level Leakage Current	$V_{OH} = 65V$		1.0	mA
V_F	Output Diode Forward Voltage	$I_F = 800$ mA		2.5	V
I_R	Output Diode Reverse Leakage	$V_R = 65V$		1.0	mA
B_{VCER}	V_{OH1} Switching Capacitive or Resistive Load			65	V
L_{VCEO}	V_{OH2} Switching Inductive Clamped Load			30	V

Switching Characteristics $V_{CC} = 13.2V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		10	μs
t_{PHL}	Propagation Delay Time High to Low Level Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		10	μs
t_{TLH}	Transition Time Low to High Level Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		500	ns
t_{THL}	Transition Time High to Low Level Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		500	ns
t_{PLH}	Enable to Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		10	μs
t_{PHL}	Enable to Output	$V_{CC} = 13.2V$, $R_L = 30\Omega$, $C_L = 15$ pF		10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: Unless otherwise specified min/max limits apply across the −40°C to +105°C temperature range.

National Semiconductor

DS3658 Quad High Current Peripheral Driver

General Description

The DS3658 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. A unique input circuit combines TTL compatibility with high impedance. In fact, its extreme low input current allows it to be driven directly by a CMOS device.

The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch-up during turn off (inductive fly back protection—refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3658 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

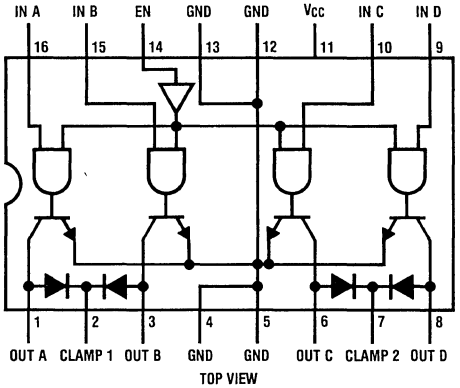
- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Single saturated transistor outputs
- Low standby power, 10 mW typical
- High impedance TTL compatible inputs
- Outputs may be tied together for increased current capacity
- High output current
  - 600 mA per output
  - 2.4A per package
- No output latch-up at 35V
- Low output ON voltage (350 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS3658N
See NS Package N16A

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	L	Z
L	L	Z

H = High state
L = Low state
Z = High impedance state

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	15V
Output Voltage	70V
Output Current	1.5A
Continuous Power Dissipation @ 25°C Free-Air (Note 5)	2075 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Ambient Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	$V_{IN}=5.25V$, $V_{CC}=5.25V$		1.0	10	μA
I_{IL}	Input Low Current	$V_{IN}=0.4V$			±10	μA
V_{IK}	Input Clamp Voltage	$I_I=-12$ mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	$I_L=300$ mA		0.2	0.4	V
		$I_L=600$ mA (Note 4)		0.35	0.7	V
I_{CEX}	Output Leakage Current	$V_{CE}=70V$, $V_{IN}=0.8V$			100	μA
V_F	Diode Forward Voltage	$I_F=800$ mA		1.0	1.6	V
I_R	Diode Leakage Current	$V_R=70V$			100	μA
I_{CC}	Supply Current	All Inputs High		50	65	mA
		All Inputs Low		2	4	mA

Switching Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{HL}	Turn On Delay	$R_L=60\Omega$, $V_L=30V$		226	500	ns
t_{LH}	Turn Off Delay	$R_L=60\Omega$, $V_L=30V$		2430	8000	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

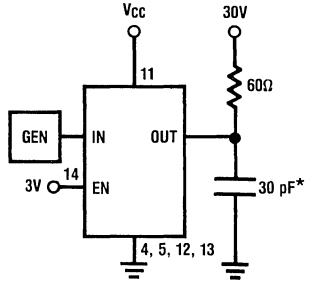
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A=25°C$ and $V_{CC}=5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: All sections of this quad circuit may conduct rated current simultaneously; however, power dissipation averaged over a short interval of time must fall within specified continuous dissipation ratings.

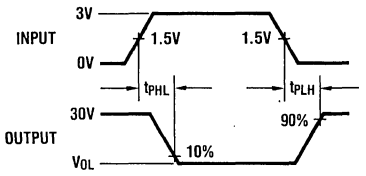
Note 5: For operation over 25°C free-air temperature, derate linearly to 1328 mW @70°C @ the rate of 16.6 mW/°C.

AC Test Circuit



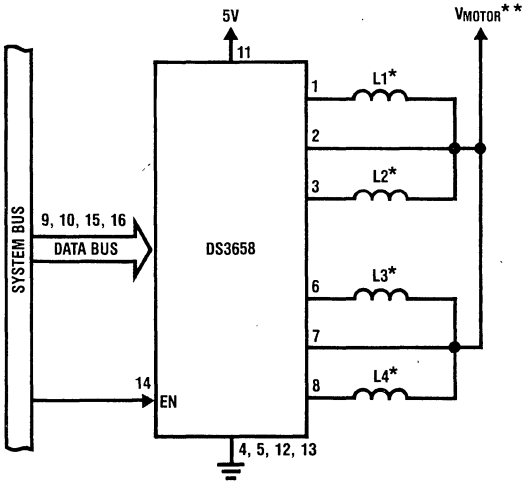
* Includes probe and jig capacitance

Switching Waveforms

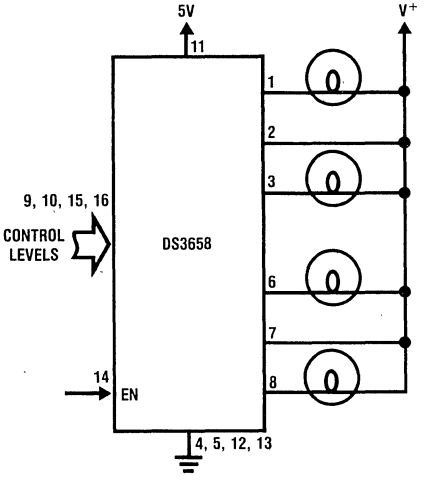


Typical Applications

Stepping Motor Driver



Lamp Driver



* L1, L2, L3, L4 are the windings of a bifilar stepping motor.

** V_{MOTOR} is the supply voltage of the motor.

National Semiconductor

DS3668 Quad Fault Protected Peripheral Driver

General Description

The DS3668 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. Unlike most peripheral drivers available, a unique fault protection circuit is incorporated on each output. When the load current exceeds 1.0 A (approximately) on any output for more than a built-in delay time, nominally 25 μs, that output will be shut off by its protection circuitry with no effect on other outputs. This condition will prevail until that protection circuitry is reset by toggling the corresponding input or the enable pin low for at least 0.5 μs. The 25 μs built-in delay is provided to ensure that the protection circuitry is not triggered by turn-on surge currents associated with certain kinds of loads.

The DS3668's inputs combine TTL compatibility with high input impedance. In fact, its extreme low input current allows it to be driven directly by a MOS device. The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch up during turn off (inductive fly-back protection — refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3668 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when the input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

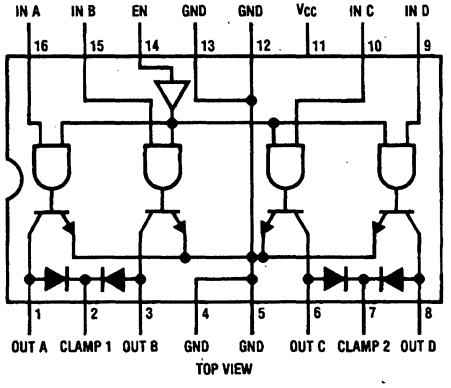
- Relay drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Output fault protection
- High impedance TTL compatible inputs
- High output current — 600 mA per output
- No output latch-up at 35V
- Low output ON voltage (550 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly-back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail-safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram *

Dual-In-Line Package



TOP VIEW

TL/F/5225–1

* See Page 3 for the detail of output protection.

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	L	Z
L	L	Z

H = High state
L = Low state
Z = High impedance state

Order Number DS3668N
See NS Package N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	15V
Output Voltage	70V
Continuous Power Dissipation @25°C Free-Air (Note 5)	2075 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Ambient Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	$V_{IN}=5.25V$, $V_{CC}=5.25V$		1.0	20	μA
I_{IL}	Input Low Current	$V_{IN}=0.4V$			±10	μA
V_{IK}	Input Clamp Voltage	$I_I=-12$ mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	$I_L=300$ mA		0.2	0.7	V
		$I_L=600$ mA (Note 4)		0.55	1.5	V
I_{CEX}	Output Leakage Current	$V_{CE}=70V$, $V_{IN}=0.8V$			100	μA
V_F	Diode Forward Voltage	$I_F=800$ mA		1.2		V
I_R	Diode Leakage Current	$V_R=70V$			100	μA
I_{CC}	Supply Current	All Inputs High		62	80	mA
		All Inputs Low		20		mA
I_{TH}	Protection Circuit Threshold Current			1		A

Switching Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{HL}	Turn On Delay	$R_L=60\Omega$, $V_L=30V$		300		ns
t_{LH}	Turn Off Delay	$R_L=60\Omega$, $V_L=30V$		2000		ns
t_{FZ}	Protection Enable Delay (after Detection of fault)			25		μs
t_{RL}	Input Low Time For Protection Circuit Reset		1.0			μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

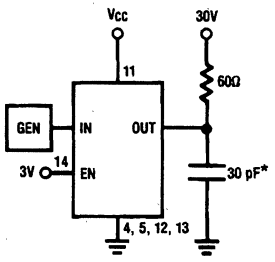
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A=25°C$ and $V_{CC}=5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: All sections of this quad circuit may conduct rated current simultaneously; however, power dissipation averaged over a short interval of time must fall within specified continuous dissipation ratings.

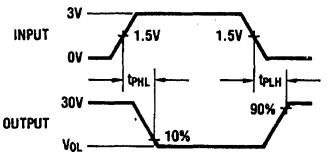
Note 5: For operation over 25°C free-air temperature, derate linearly to 1328 mW @ 70°C @ the rate of 16.6 mW/°C.

AC Test Circuit



TL/F/5225–2

Switching Waveforms

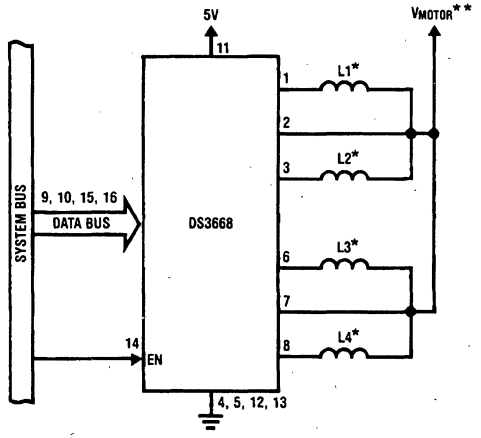


TL/F/5225–3

*Includes probe and jig capacitance

Typical Application

Stepping Motor Driver

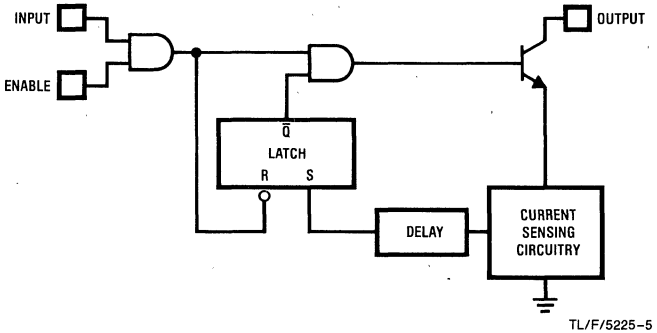


TL/F/5225–4

*L1, L2, L3, L4 are the windings of a bifilar stepping motor.

**V_{MOTOR} is the supply voltage of the motor.

Protection Circuit Block Diagram



TL/F/5225–5

National Semiconductor

Peripheral/Power Drivers

PRELIMINARY

DS3669 Quad High Current Peripheral Driver

General Description

The DS3669 is a non-inverting quad peripheral driver similar to the DS3658. These drivers are designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. A unique input circuit combines TTL compatibility with high impedance. In fact, its extreme low input current allows it to be driven directly by a CMOS device.

The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch-up during turn off (inductive fly back protection—refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3669 incorporates circuitry that guarantees glitch-free power up or down operation.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

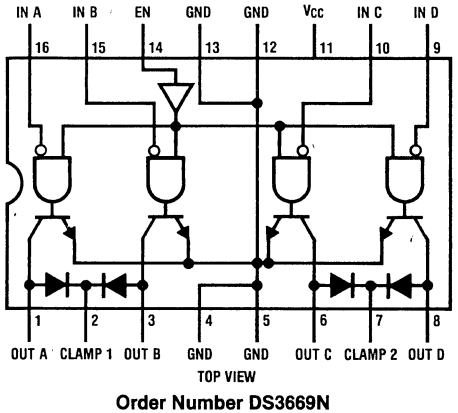
- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Single saturated transistor outputs
- Low standby power, 10 mW typical
- High impedance TTL compatible inputs
- Outputs may be tied together for increased current capacity
- High output current
  - 600 mA per output
  - 2.4A per package
- No output latch-up at 35V
- Low output ON voltage (350 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- 2W power package

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS3669N
See NS Package N16A

Truth Table

IN	EN	OUT
L	H	L
H	H	Z
L	L	Z
H	L	Z

H = High state
L = Low state
Z = High impedance state

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	15V
Output Voltage	70V
Output Current	1.5A
Continuous Power Dissipation @ 25°C Free-Air (Note 5)	2075 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage	4.75	5.25	V
Ambient Temperature	0	70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{IH}	Input High Current	$V_{IN} = 5.25V$, $V_{CC} = 5.25V$		1.0	10	μA
I_{IL}	Input Low Current	$V_{IN} = 0.4V$			± 10	μA
V_{IK}	Input Clamp Voltage	$I_I = -12$ mA		−0.8	−1.5	V
V_{OL}	Output Low Voltage	$I_L = 300$ mA		0.2	0.4	V
		$I_L = 600$ mA (Note 4)		0.35	0.7	V
I_{CEX}	Output Leakage Current	$V_{CE} = 70V$, $V_{IN} = 2V$, $V_{EN} = 0.8V$			100	μA
V_F	Diode Forward Voltage	$I_F = 800$ mA		1.0	1.6	V
I_R	Diode Leakage Current	$V_R = 70V$			100	μA
I_{CC}	Supply Current	All Inputs Low EN = 2.0V		50	65	mA
		All Inputs High		2	4	mA

Switching Characteristics (Note 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{HL}	Turn On Delay	$R_L = 60\Omega$, $V_L = 30V$		226	500	ns
t_{LH}	Turn Off Delay	$R_L = 60\Omega$, $V_L = 30V$		2430	8000	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

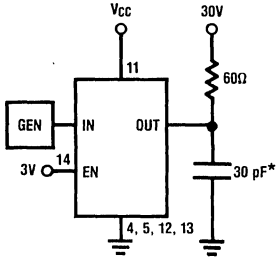
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: All sections of this quad circuit may conduct rated current simultaneously; however, power dissipation averaged over a short interval of time must fall within specified continuous dissipation ratings.

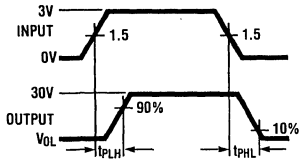
Note 5: For operation over 25°C free-air temperature, derate linearly to 1328 mW @70°C @ the rate of 16.6 mW/°C.

AC Test Circuit



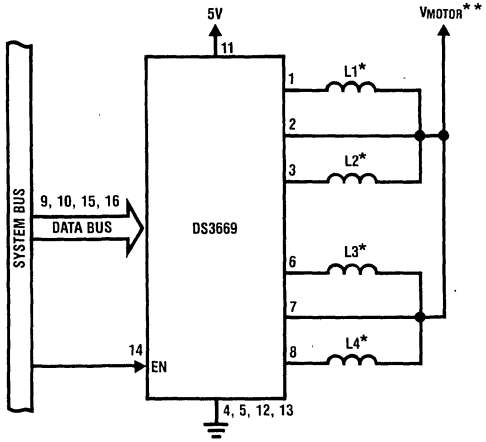
*Includes probe and jig capacitance

Switching Waveforms



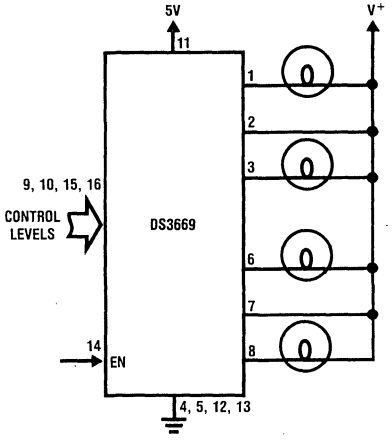
Typical Applications

Stepping Motor Driver



*L1, L2, L3, L4 are the windings of a bifilar stepping motor.
**V_{MOTOR} is the supply voltage of the motor.

Lamp Driver



National Semiconductor

DS3680 Quad Negative Voltage Relay Driver

General Description

The DS3680 is a quad high voltage negative relay driver designed to operate over wide ranges of supply voltage, common-mode voltage, and ambient temperature, with 50 mA sink capability. These drivers are intended for switching the ground end of loads which are directly connected to the negative supply, such as in telephone relay systems.

Since there may be considerable noise and IR drop between logic ground and negative supply ground in many applications, these drivers are designed to operate with a high common-mode range ($\pm$ 20V referenced to negative supply ground). Each driver has a common-mode range separate from the other drivers in the package, which permits input signals from more than one element of the system.

With low differential input current requirements (typically 100 μA), these drivers are compatible with TTL, LS and CMOS logic. Differential inputs permit either inverting or non-inverting operation.

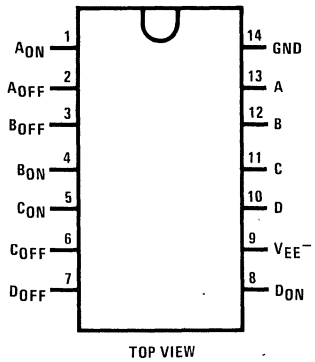
The driver outputs incorporate transient suppression clamp networks, which eliminate the need for external networks when used in applications of switching inductive loads. A fail-safe feature is incorporated to insure that, if the V_{ON} input or both inputs are open, the driver will be OFF.

Features

- -10V to -60V operation
- Quad 50 mA sink capability
- TTL/LS/CMOS or voltage comparator input
- High input common-mode voltage range
- Very low input current
- Fail-safe disconnect feature
- Built-in output clamp diode

Connection Diagram

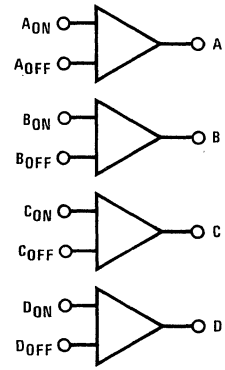
Dual-In-Line Package



TOP VIEW

Order Number DS3680J or DS3680N
See NS Package J14A or N14A

Logic Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage: GND to V_{EE}^-, and Any Pin	−70V
Positive Input Voltage: Input to GND	20V
Negative Input Voltage: Input to V_{EE}^-	−5V
Differential Input Voltage: V_{ON} to V_{OFF}	±20V
Inductive Load	$L_L \leq 5h$ $I_L \leq 50$ mA
Output Current	−100 mA
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1398 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 11.2 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage: GND to V_{EE}^-	−10	−60	V
Input Voltage: Input to GND	−20	20	V
Logic ON Voltage: V_{ON} Referenced to V_{OFF}	2	20	V
Logic OFF Voltage: V_{ON} Referenced to V_{OFF}	−20	0.8	V
Temperature Range	−25	85	°C

Electrical Characteristics (Notes 2 and 3)

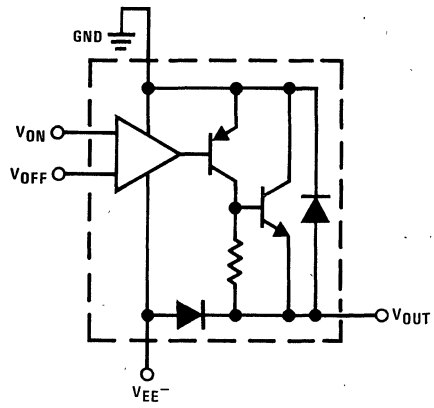
Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage		2.0	1.3		V
V_{IL}	Logic "0" Input Voltage			1.3	0.8	V
I_{INH}	Logic "1" Input Current	$V_{IN} = 2V$		40	100	μA
		$V_{IN} = 7V$		375	1000	μA
I_{INL}	Logic "0" Input Current	$V_{IN} = 0.4V$		−0.01	−5	μA
		$V_{IN} = -7V$		−1	−100	μA
V_{OL}	Output ON Voltage	$I_{OL} = 50$ mA		−1.6	−2.1	V
I_{OFF}	Output Leakage	$V_{OUT} = V_{EE}^-$		−2	−100	μA
I_{FS}	Fail-Safe Output Leakage	$V_{OUT} = V_{EE}^-$ (Inputs Open)		−2	−100	μA
I_{LC}	Output Clamp Leakage Current	$V_{OUT} = GND$		2	100	μA
V_C	Output Clamp Voltage	$I_{CLAMP} = -50$ mA Referenced to V_{EE}^-		−2	−1.2	V
V_P	Positive Output Clamp Voltage	$I_{CLAMP} = 50$ mA Referenced to GND		0.9	1.2	V
$I_{EE(ON)}$	ON Supply Current	All Drivers ON		−2	−4.4	mA
$I_{EE(OFF)}$	OFF Supply Current	All Drivers OFF		−1	−100	μA
$t_{PD(ON)}$	Propagation Delay to Driver ON	$L = 1h$, $R_L = 1k$, $V_{IN} = 3V$ Pulse		1	10	μs
$t_{PD(OFF)}$	Propagation Delay to Driver OFF	$L = 1h$, $R_L = 1k$, $V_{IN} = 3V$ Pulse		1	10	μs

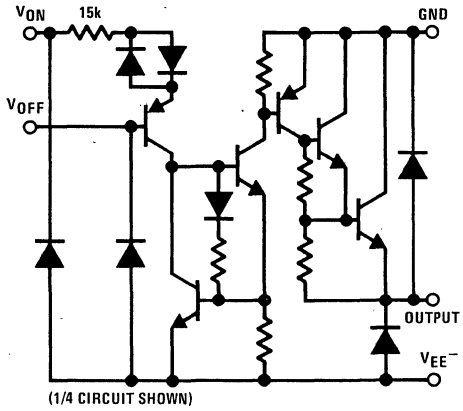
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, the min/max limits of the table of "Electrical Characteristics" apply within the range of the table of "Operating Conditions". All typical values are given for $V_{EE}^- = 52V$, and $T_A = 25°C$.

Note 3: All current into device pins shown as positive, out of the device as negative. All voltages are referenced to ground unless otherwise noted.

Schematic Diagrams





National Semiconductor

Peripheral/Power Drivers

DS3686 Dual Positive Voltage Relay Driver

General Description

The DS3686 is a high voltage/current positive voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/LS compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of 54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at 5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90 mW.

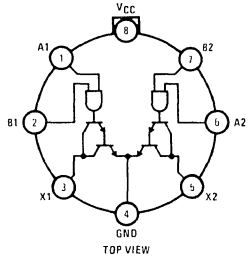
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

Features

- TTL/LS/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

Connection Diagrams

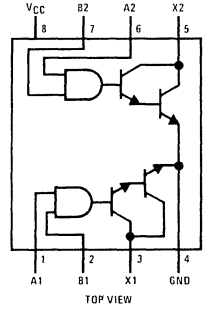
Metal Can Package



Pin 4 is in electrical contact with the case

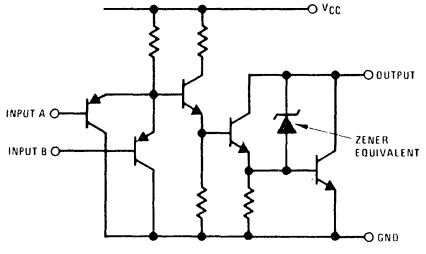
Order Number DS3686H
See NS Package H08C

Dual-In-Line Package



Order Number DS3686J-8 or DS3686N
See NS Package J08A or N08A

Schematic Diagram



Truth Table

Positive logic: $\overline{AB} = X$

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
TO-5 Package	787 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C; derate TO-5 package 5.2 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

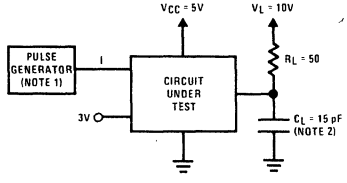
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	$R_L = 180\Omega$, $V_L = 54V$, $V_O \leq 2.5V$			2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, $V_{IN} = 5.5V$				0.01	40	μA
V_{IL}	Logical "0" Input Voltage	$R_L = 180\Omega$, $V_L = 54V$, $V_O \leq 53.8V$					0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, $V_{IN} = 0.4V$				−150	−250	μA
V_{CD}	Input Clamp Voltage	$V_{CC} = 5V$, $I_{CLAMP} = -12$ mA, $T_A = 25°C$				−1.0	−1.5	V
V_{OH}	Output Breakdown	V_{CC} = Max, $V_{IN} = 0V$, $I_{OUT} = 5$ mA			56	65		V
I_{OH}	Output Leakage	V_{CC} = Max, $V_{IN} = 0.4V$, $V_{OUT} = 54V$				0.5	250	μA
V_{OL}	Output ON Voltage	V_{CC} = Min, $V_{IN} = 2.4V$	DS3686	I_{OL} = 100 mA		0.85	1.0	V
				I_{OL} = 300 mA		1.0	1.2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, $V_{IN} = 0V$, Outputs Open				2	4	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, $V_{IN} = 3V$, Outputs Open				18	28	mA
t_{PD0}	Propagation Delay to a Logical "0" (Output Turn ON)	$C_L = 15$ pF, $V_L = 10V$, $R_L = 50\Omega$, $T_A = 25°C$, $V_{CC} = 5V$				50		ns
t_{PD1}	Propagation Delay to a Logical "1" (Output Turn OFF)	$C_L = 15$ pF, $V_L = 10V$, $R_L = 50\Omega$, $T_A = 25°C$, $V_{CC} = 5V$				1		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3686. All typicals are given for $V_{CC} = 5V$ and $T_A = 25°C$.

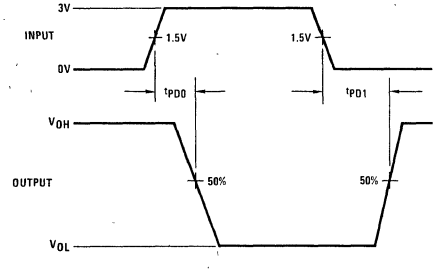
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms



Note 1: The pulse generator has the following characteristics: PRR = 100 kHz, 50% duty cycle, $Z_{OUT} \cong 50\Omega$, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.



National Semiconductor

DS1687/DS3687 Negative Voltage Relay Driver

General Description

The DS1687/DS3687 is a high voltage/current negative voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/LS compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of −54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at −5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90 mW.

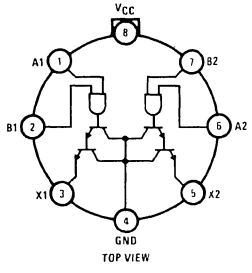
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

Features

- TTL/LS/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (−65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

Connection Diagrams

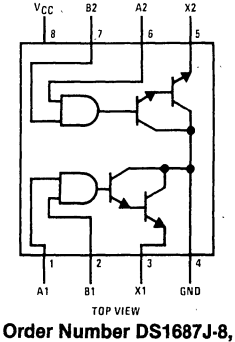
Metal Can Package



Pin 4 is in electrical contact with the case

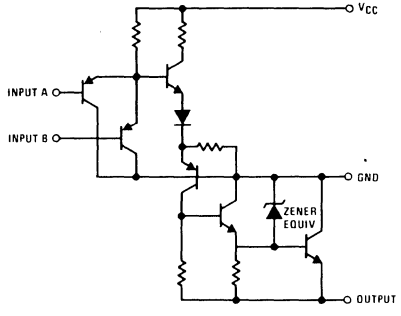
Order Number DS1687H
or DS3687H
See NS Package H08C

Dual-In-Line Package



Order Number DS1687J-8,
DS3687J-8 or DS3687N
See NS Package J08A or N08A

Schematic Diagram



Truth Table

Positive logic: $\overline{AB} = X$

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1133 mW
Molded Package	1022 mW
TO-5 Package	787 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1687	4.5	5.5	V
DS3687	4.75	5.25	V
Temperature, T_A			
DS1687	−55	+125	°C
DS3687	0	+70	°C

*Derate cavity package 7.6 mW/°C above 25°C; derate molded package 8.2 mW/°C above 25°C; derate TO-5 package 5.2 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

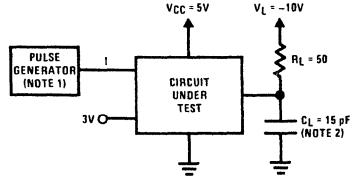
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage				2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V				1.0		μA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−150	−250	μA
V_{CD}	Input Clamp Voltage	V_{CC} = 5V, I_{CLAMP} = −12 mA, T_A = 25°C				−1.0	−1.5	V
V_{OH}	Output Breakdown	V_{CC} = Max, V_{IN} = 0V, I_{OUT} = −5 mA			−56	−65		V
I_{OH}	Output Leakage	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = −54V				−0.5	−250	μA
V_{OL}	Output ON Voltage	V_{CC} = Min, V_{IN} = 2V	DS1687	I_{OL} = −100 mA		−0.9	−1.1	V
				I_{OL} = −300 mA		−1.0	−1.3	V
			DS3687	I_{OL} = −100 mA		−0.9	−1.0	V
				I_{OL} = −300 mA		−1.0	−1.2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 0V, Outputs Open				2	4	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 3V, Outputs Open				18	28	mA
$t_{PD(ON)}$	Propagation Delay to a Logical "0" (Output Turn ON)	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5V				50		ns
$t_{PD(OFF)}$	Propagation Delay to a Logical "1" (Output Turn OFF)	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5V				1.0		μs

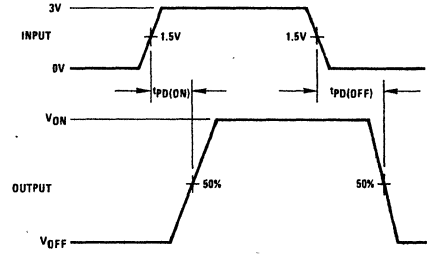
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1687 and across the 0°C to +70°C range for the DS3687. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms





Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $Z_{OUT} \cong 50\Omega$, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor

Peripheral/Power Drivers

DS55450/DS75450 Series Dual Peripheral Drivers

General Description

The DS55450/DS75450 series of dual peripheral drivers are a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

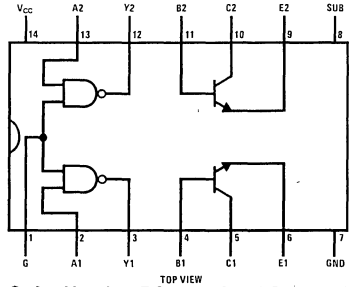
The DS75450 is a general purpose device featuring two standard Series 54/74 TTL gates and two uncommitted, high current, high voltage NPN transistors. The device offers the system designer the flexibility of tailoring the circuit to the application.

The DS55451/DS75451, DS55452/DS75452, DS55453/DS75453 and DS55454/DS75454 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

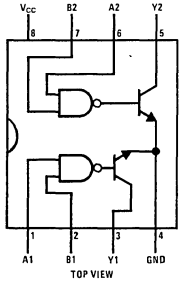
Features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

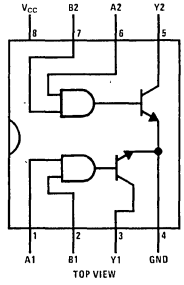
Connection Diagrams (Dual-In-Line and Metal Can Packages)



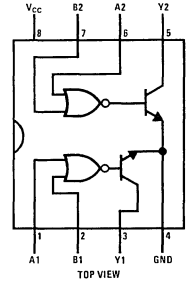
Order Number DS75450J or DS75450N
See NS Package J14A or N14A



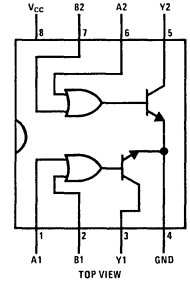
Order Number DS55451J-8, DS75451J-8 or DS75451N



Order Number DS55452J-8, DS75452J-8 or DS75452N

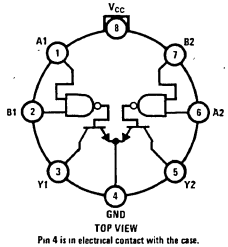


Order Number DS55453J-8, DS75453J-8 or DS75453N

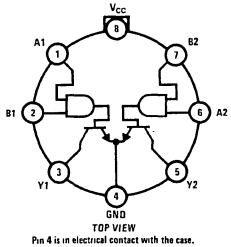


Order Number DS55454J-8, DS75454J-8 or DS75454N

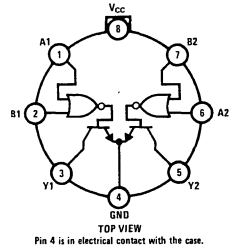
See NS Package J08A or N08A



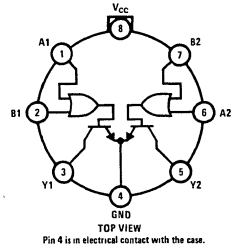
Order Number DS55451H or DS75451H



Order Number DS55452H or DS75452H



Order Number DS55453H or DS75453H



Order Number DS55454H or DS75454H

See NS Package H08C

Absolute Maximum Ratings (Note 1)

Supply Voltage, (V_{CC}) (Note 2)	7.0V
Input Voltage	5.5V
Inter-emitter Voltage (Note 3)	5.5V
V_{CC}-to-Substrate Voltage	
DS75450	35V
Collector-to-Substrate Voltage	
DS75450	35V
Collector-Base Voltage	
DS75450	35V
Collector-Emitter Voltage (Note 4)	
DS75450	30V
Emitter-Base Voltage	
DS75450	5.0V
Output Voltage (Note 5)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	30V
Collector Current (Note 6)	
DS75450	300 mA
Output Current (Note 6)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	300 mA
DS75450 Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
DS75451/2/3/4 Maximum Power Dissipation† at 25°C	
Cavity Package	1090 mW
Molded Package	957 mW
TO-5 Package	760 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions (Note 7)

	MIN	MAX	UNITS
Supply Voltage, (V_{CC})			
DS5545X	4.5	5.5	V
DS7545X	4.75	5.25	V
Temperature, (T_A)			
DS5545X	−55	+125	°C
DS7545X	0	+70	°C

*Derate cavity package 8.7 mW/°C above 25°C; derate molded package 9.7 mW/°C above 25°C.

†Derate cavity package 7.3 mW/°C above 25°C; derate molded package 7.7 mW/°C above 25°C; derate TO-5 package 5.1 mW/°C above 25°C.

Electrical Characteristics DS75450 (Notes 8 and 9)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
TTL GATES							
V_{IH}	High Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OH} = −400μA, *(Figure 2)*		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 16 mA *(Figure 1)*			0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 4)*	Input A			1	mA
			Input G			2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 4)*	Input A			40	μA
			Input G			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*	Input A			−1.6	mA
			Input G			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, *(Figure 5)*, (Note 10)		−18		−55	mA
I_{CCH}	Supply Current	V_{CC} = Max, V_I = 0V, Outputs High, *(Figure 6)*			2	4	mA
I_{CCL}	Supply Current	V_{CC} = Max, V_I = 5V, Outputs Low, *(Figure 6)*			6	11	mA
OUTPUT TRANSISTORS							
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100μA, I_E = 0		35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100μA, R_{BE} = 500Ω		30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3V, (Note 11)	T_A = +25°C, I_C = 100 mA	25			
			T_A = +25°C, I_C = 300 mA	30			
			T_A = 0°C, I_C = 100 mA	20			
			T_A = 0°C, I_C = 300 mA	25			
V_{BE}	Base-Emitter Voltage	(Note 11)	I_B = 10 mA, I_C = 100 mA		0.85	1	V
			I_B = 30 mA, I_C = 300 mA		1.05	1.2	V
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	(Note 11)	I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
			I_B = 30 mA, I_C = 300 mA		0.5	0.7	V

Electrical Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9)

PARAMETER		CONDITIONS				MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage	*(Figure 7)*				2			V
V_{IL}	Low-Level Input Voltage							0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA						−1.5	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, *(Figure 7)*	V_{IL} = 0.8V	I_{OL} = 100 mA	DS55451, DS55453		0.25	0.5	V
					DS75451, DS75453		0.25	0.4	V
				I_{OL} = 300 mA	DS55451, DS55453		0.5	0.8	V
					DS75451, DS75453		0.5	0.7	V
			V_{IH} = 2V	I_{OL} = 100 mA	DS55452, DS55454		0.25	0.5	V
					DS75452, DS75454		0.25	0.4	V
				I_{OL} = 300 mA	DS55452, DS55454		0.5	0.8	V
					DS75452, DS75454		0.5	0.7	V
I_{OH}	High-Level Output Current	V_{CC} = Min, *(Figure 7)*	V_{OH} = 30V	V_{IH} = 2V	DS55451, DS55453			300	μA
					DS75451, DS75453			100	μA
				V_{IL} = 0.8V	DS55452, DS55454			300	μA
					DS75452, DS75454			100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 9)*						1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 9)*						40	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 8)*					−1	−1.6	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = Max, *(Figure 10)*	V_I = 5V		DS55451/DS75451		7	11	mA
			V_I = 0V		DS55452/DS75452		11	14	mA
			V_I = 5V		DS55453/DS75453		8	11	mA
			V_I = 0V		DS55454/DS75454		13	17	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = Max, *(Figure 10)*	V_I = 0V		DS55451/DS75451		52	65	mA
			V_I = 5V		DS55452/DS75452		56	71	mA
			V_I = 0V		DS55453/DS75453		54	68	mA
			V_I = 5V		DS55454/DS75454		61	79	mA

Switching Characteristics

DS75450 (V_{CC} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		12	22	ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		8	15	ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{TLH}	Transition Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			7	12	ns
t_{THL}	Transition Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			9	15	ns
V_{OH}	High-Level Output Voltage After Switching	V_S = 20V, $I_C \approx$ 300 mA, R_{BE} = 500Ω, *(Figure 15)*		V_S−6.5			mV
t_D	Delay Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			8	15	ns
t_R	Rise Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			12	20	ns
t_S	Storage Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			7	15	ns
t_F	Fall Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			6	15	ns

Switching Characteristics (Continued)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (V_{CC} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		26	35	ns
			DS55453/DS75453		18	25	ns
			DS55454/DS75454		27	35	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		24	35	ns
			DS55453/DS75453		16	25	ns
			DS55454/DS75454		24	35	ns
t_{TLH}	Transition Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*			5	8	ns
t_{THL}	Transition Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*			7	12	ns
V_{OH}	High-Level Output Voltage After Switching	V_S = 20V, $I_O \approx$ 300 mA, *(Figure 15)*		V_S–6.5			mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: The voltage between two emitters of a multiple-emitter transistor.

Note 4: Value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500Ω.

Note 5: The maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 6: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 7: For the DS75450 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

Note 8: Unless otherwise specified min/max limits apply across the –55°C to +125°C temperature range for the DS55450 series and across the 0°C to +70°C range for the DS75450 series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 9: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

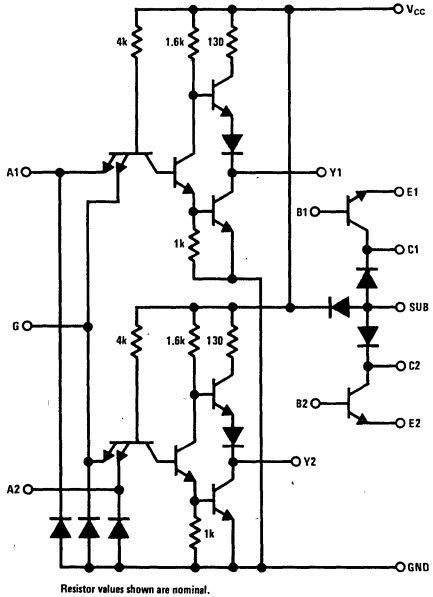
Note 10: Only one output at a time should be shorted.

Note 11: These parameters must be measured using pulse techniques. t_W = 300μs, duty cycle < 2%.

Note 12: Applies to output transistors only.

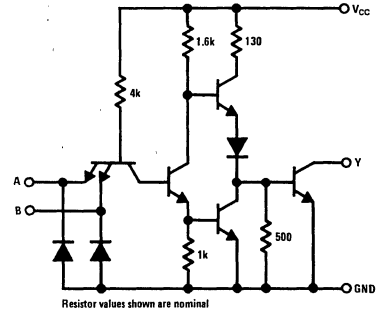
Schematic Diagrams

DS75450



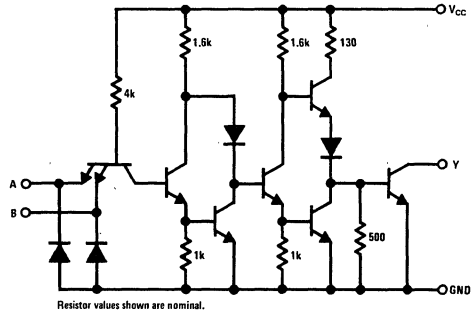
Resistor values shown are nominal.

DS55451/DS75451



Resistor values shown are nominal.

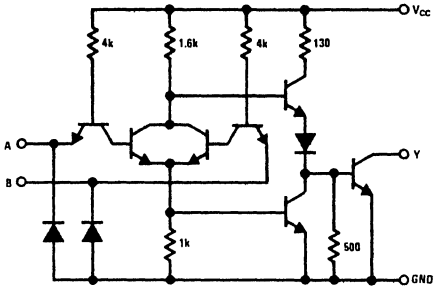
DS55452/DS75452



Resistor values shown are nominal.

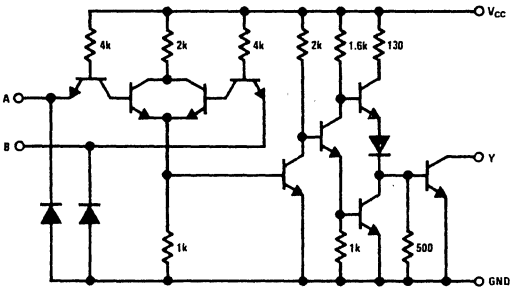
Schematic Diagrams (Continued)

DS55453/DS75453



Resistor values shown are nominal.

DS55454/DS75454



Resistor values shown are nominal.

Truth Tables (H = high level, L = low level)

DS55451/DS75451

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55452/DS75452

A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

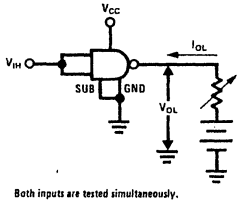
DS55453/DS75453

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55454/DS75454

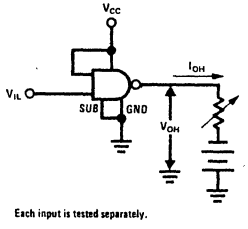
A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

DC Test Circuits



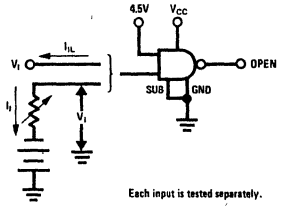
Both inputs are tested simultaneously.

FIGURE 1. V_{IH}, V_{OL}



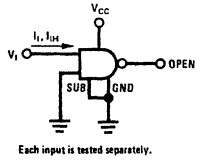
Each input is tested separately.

FIGURE 2. V_{IL}, V_{OH}



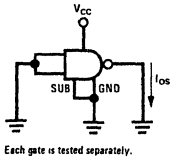
Each input is tested separately.

FIGURE 3. V_I, I_{IL}



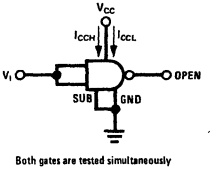
Each input is tested separately.

FIGURE 4. I_I, I_{IH}



Each gate is tested separately.

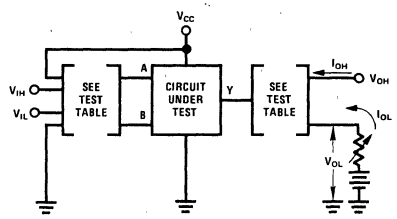
FIGURE 5. I_{OS}



Both gates are tested simultaneously

FIGURE 6. I_{CCH}, I_{CCL}

DC Test Circuits (Continued)



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS54451	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS54452	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
DS54453	V_{IH} V_{IL}	Gnd V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS54454	V_{IH} V_{IL}	Gnd V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}

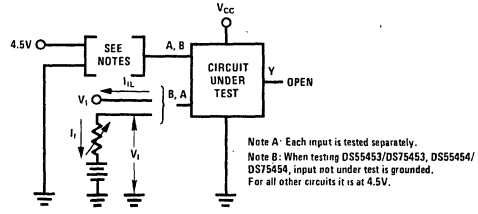


FIGURE 8. V_I, I_{IL}

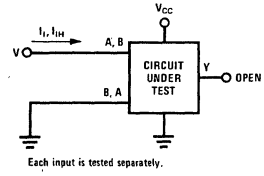


FIGURE 9. I_I, I_{IH}

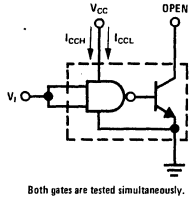


FIGURE 10. I_{CCH}, I_{CCL} for AND, NAND Circuits

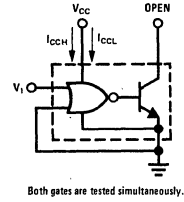
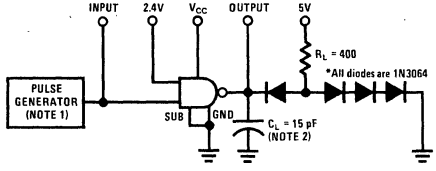
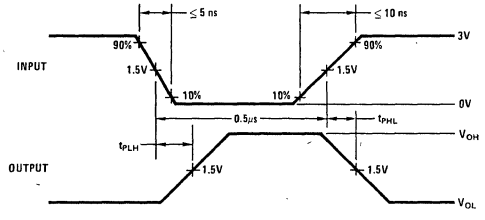


FIGURE 11. I_{CCH}, I_{CCL} for OR, NOR Circuits

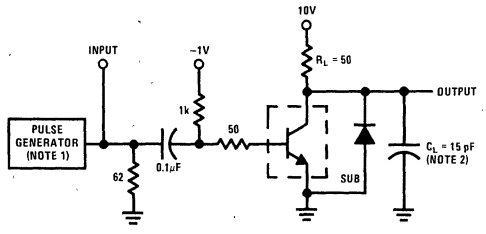
AC Test Circuits and Switching Time Waveforms

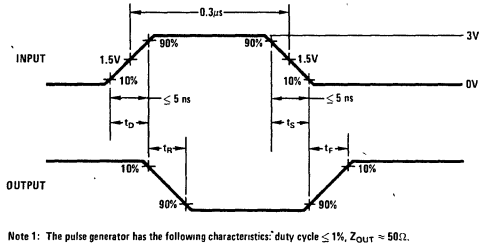




Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L include probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate (DS75450 Only)

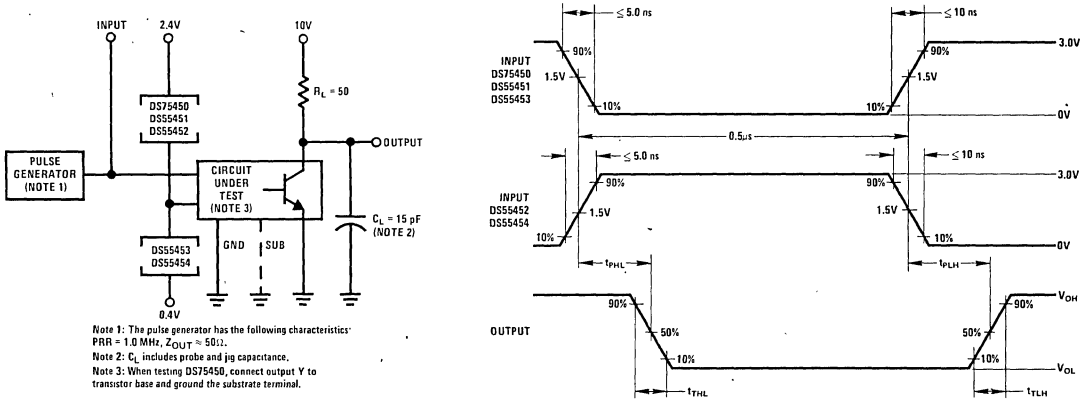




Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

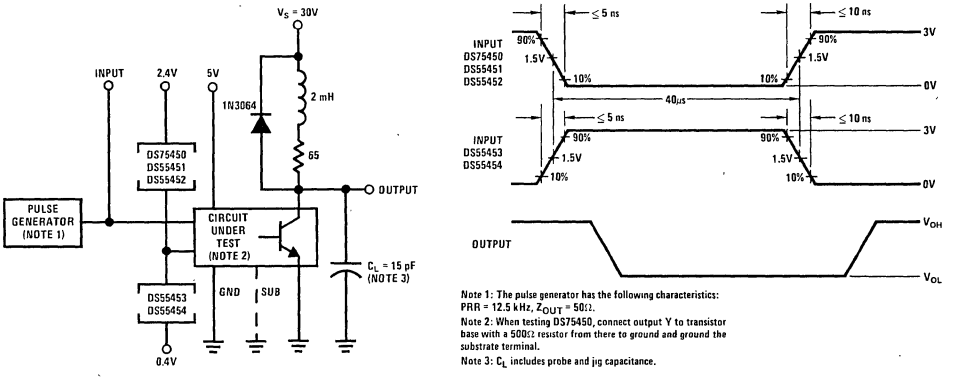
FIGURE 13. Switching Times, Each Transistor (DS75450 Only)

AC Test Circuits and Switching Time Waveforms (Continued)



Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.
Note 3: When testing DS75450, connect output Y to transistor base and ground the substrate terminal.

FIGURE 14. Switching Times of Complete Drivers



Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} = 50\Omega$.
Note 2: When testing DS75450, connect output Y to transistor base with a 500Ω resistor from there to ground and ground the substrate terminal.
Note 3: C_L includes probe and jig capacitance.

FIGURE 15. Latch-Up Test of Complete Drivers

Typical Performance Characteristics

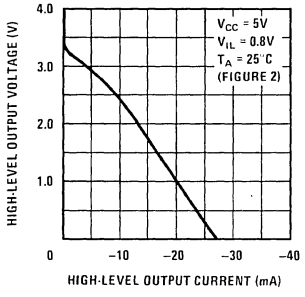


FIGURE 16. DS75450 TTL Gate High-Level Output Voltage vs High-Level Output Current

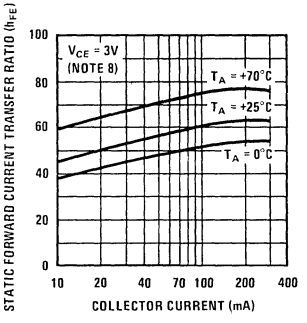


FIGURE 17. DS75450 Transistor Static Forward Current Transfer Ratio vs Collector Current

Typical Performance Characteristics (Continued)

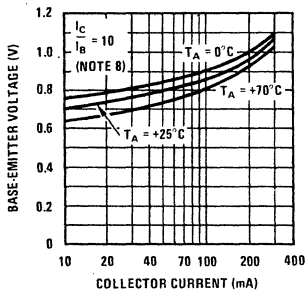


FIGURE 18. DS75450 Transistor Base-Emitter Voltage vs Collector Current

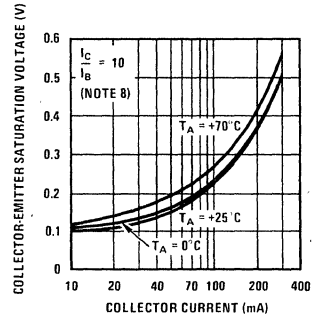


FIGURE 19. Transistor Collector-Emitter Saturation Voltage vs Collector Current

Typical Applications

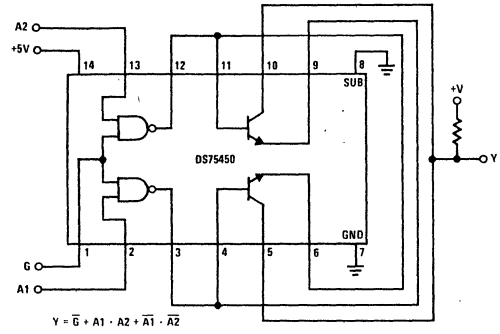


FIGURE 20. Gated Comparator

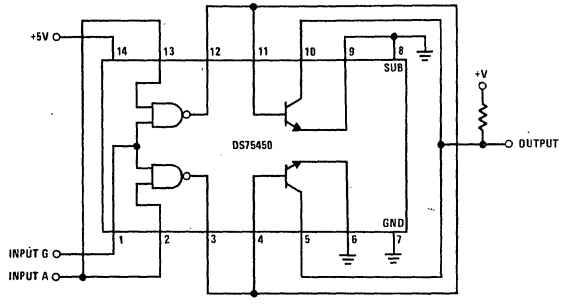


FIGURE 21. 500 mA Sink

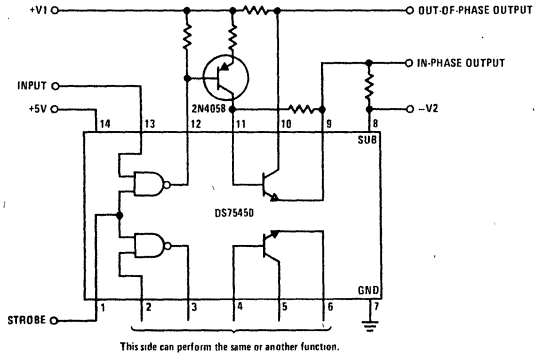


FIGURE 22. Floating Switch

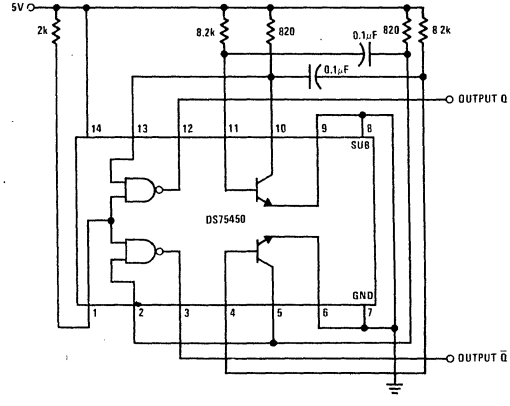
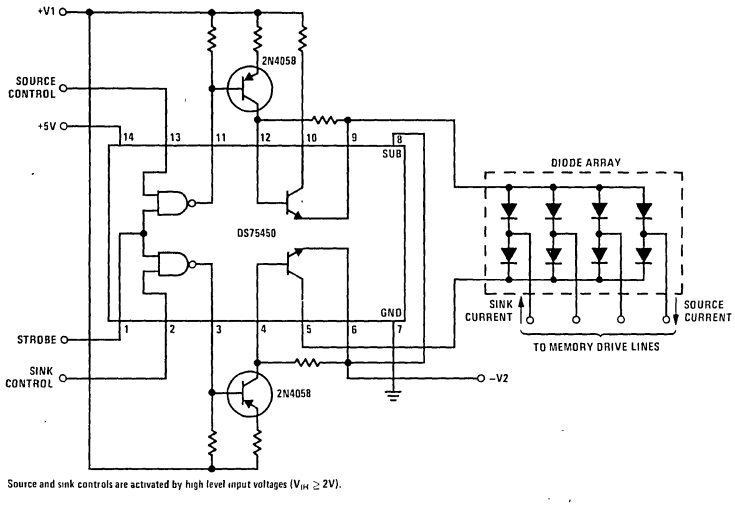


FIGURE 23. Square-Wave Generator

Typical Applications (Continued)



Source and sink controls are activated by high level input voltages ($V_{IH} \geq 2V$).

FIGURE 24. Core Memory Driver

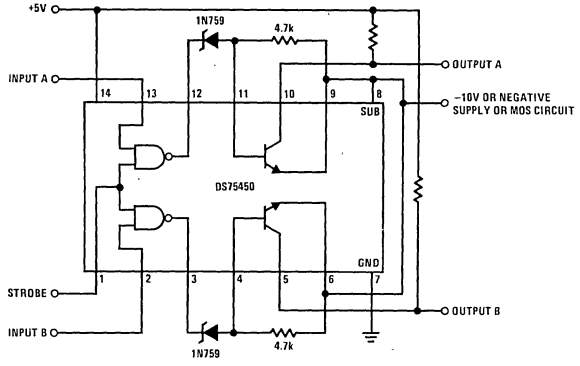


FIGURE 25. Dual TTL-to-MOS Driver

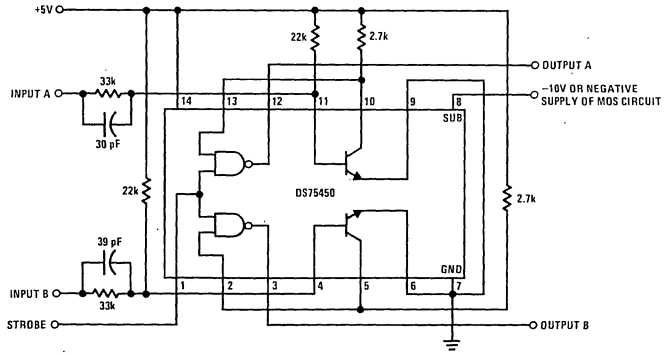


FIGURE 26. Dual MOS-to-TTL Driver

Typical Applications (Continued)

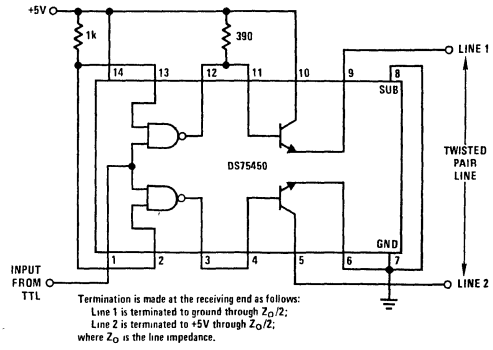


FIGURE 27. Balanced Line Driver

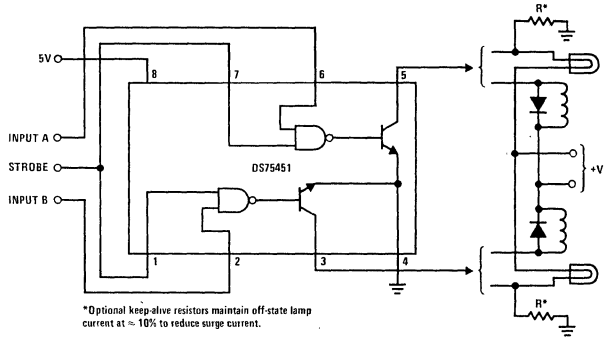


FIGURE 28. Dual Lamp or Relay Driver

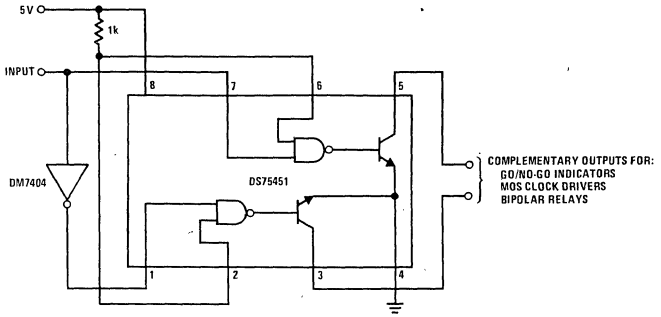


FIGURE 29. Complementary Driver

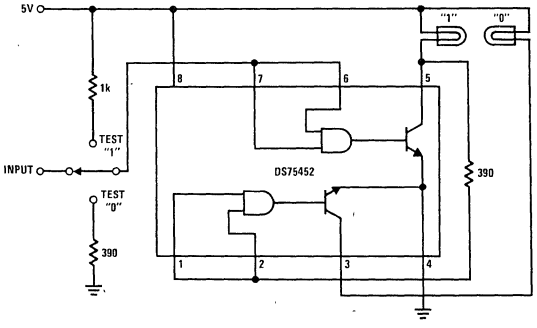


FIGURE 30. TTL or DTL Positive Logic-Level Detector

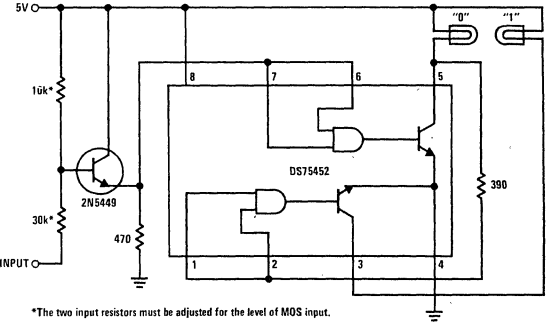


FIGURE 31. MOS Negative Logic-Level Detector

Typical Applications (Continued)

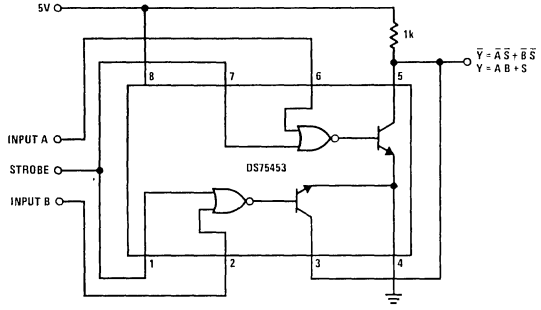
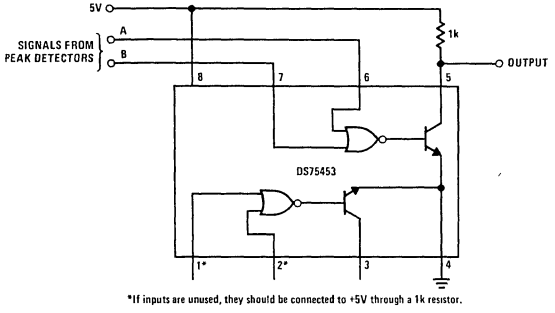


FIGURE 32. Logic Signal Comparator



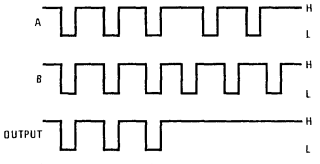


FIGURE 33. In-Phase Detector

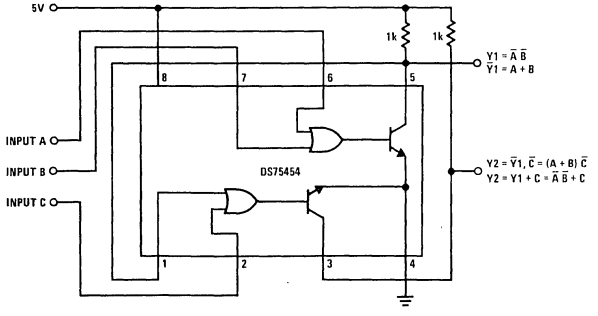


FIGURE 34. Multifunction Logic-Signal Comparator

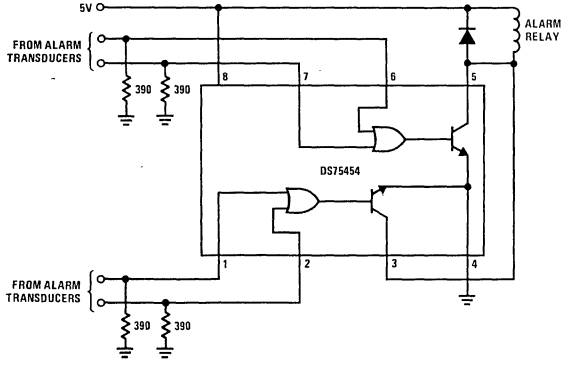


FIGURE 35. Alarm Detector

National Semiconductor

DS55461/2/3/4, DS75461/2/3/4 Series Dual Peripheral Drivers

General Description

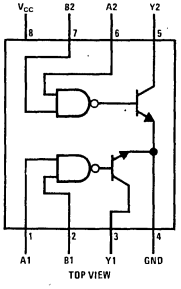
The DS55461/2/3/4 series of dual peripheral drivers are functionally interchangeable with DS55451/2/3/4 series peripheral drivers, but are designed for use in systems that require higher breakdown voltages at the expense of slightly slower switching speeds. Typical applications include power drivers, logic buffers, lamp drivers, relay drivers, MOS drivers, line drivers and memory drivers.

The DS55461/DS75461, DS55462/DS75462, DS55463/DS75463 and DS55464/DS75464 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

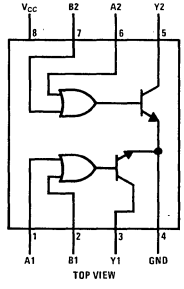
Features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 30V
- Medium speed switching
- Circuit flexibility for varied applications and choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages

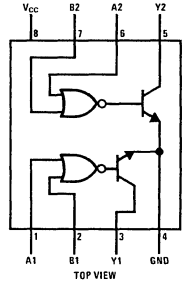
Connection Diagrams (Dual-In-Line and Metal Can Packages)



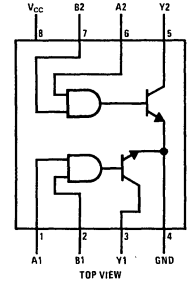
Order Number DS55461J-8, DS75461J-8 or DS75461N



Order Number DS55462J-8, DS75462J-8 or DS75462N

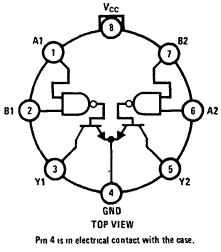


Order Number DS55463J-8, DS75463J-8 or DS75463N

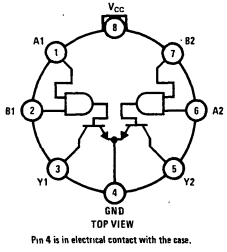


Order Number DS55464J-8, DS75464J-8 or DS75464N

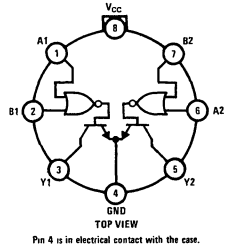
See NS Package J08A or N08A



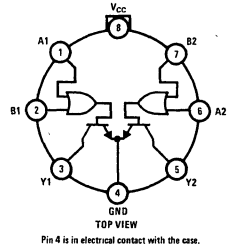
Order Number DS55461H or DS75461H



Order Number DS55462H or DS75462H



Order Number DS55463H or DS75463H



Order Number DS55464H or DS75464H

See NS Package H08C

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	7V
Input Voltage	5.5V
Inter-emitter Voltage (Note 3)	5.5V
Output Voltage (Note 4)	
DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	35V
Output Current (Note 5)	
DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	300 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1090 mW
Molded Package	957 mW
TO-5 Package	760 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

*Derate cavity package 7.3 mW/°C above 25°C; derate molded package 7.7 mW/°C above 25°C; derate TO-5 package 5.1 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS5546X	4.5	5.5	V
DS7546X	4.75	5.25	V
Temperature (T_A)			
DS5546X	−55	+125	°C
DS7546X	0	+70	°C

Electrical Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 (Notes 6 and 7)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	*(Figure 1)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 1)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.2	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, *(Figure 1)*	DS55461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.5	V
				I_{OL} = 300 mA		0.36	0.8	V
			DS55462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.5	V
				I_{OL} = 300 mA		0.35	0.8	V
			DS55463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.5	V
				I_{OL} = 300 mA		0.39	0.8	V
			DS55464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.5	V
				I_{OL} = 300 mA		0.38	0.8	V
			DS75461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.4	V
				I_{OL} = 300 mA		0.36	0.7	V
			DS75462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.4	V
				I_{OL} = 300 mA		0.35	0.7	V
			DS75463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.4	V
				I_{OL} = 300 mA		0.39	0.7	V
			DS75464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.4	V
				I_{OL} = 300 mA		0.38	0.7	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{OH} = 35V, *(Figure 1)*	V_{IH} = 2V	DS55461, DS55463			300	μA
				DS75461, DS75463			100	μA
			V_{IL} = 0.8V	DS55462, DS55464			300	μA
				DS75462, DS75464			100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 3)*					1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 3)*					40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 2)*				−1	−1.6	mA
I_{CCH}	Supply Current	V_{CC} = Max, Outputs High, *(Figures 4 and 5)*	V_I = 5V	DS55461/ DS75461, DS55463/ DS75463		8	11	mA
			V_I = 0V	DS55462/ DS75462		13	17	mA
				DS55464/ DS75464		14	19	mA

Electrical Characteristics (Continued)

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 (Notes 6 and 7)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
I_{CCL}	Supply Current	V_{CC} = Max, Outputs Low, *(Figures 4 and 5)*	V_I = 0V	DS55461/ DS75461		61	76	mA
				DS55463/ DS75463		63	76	mA
			V_I = 5V	DS55462/ DS75462		65	76	mA
				DS55464/ DS75464		72	85	mA

Switching Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 6)*	DS55461/ DS75461, DS55463/ DS75463		45	55	ns
			DS55462/ DS75462, DS55464/ DS75464		50	65	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 6)*	DS55461/ DS75461, DS55463/ DS75463		30	40	ns
			DS55462/ DS75462, DS55464/ DS75464		40	50	ns
t_{TLH}	Transition Time, Low-To-High Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 6)*	DS55461/ DS75461		8	20	ns
			DS55462/ DS75462		12	25	ns
			DS55463/ DS75463		8	25	ns
			DS55464/ DS75464		12	20	ns
t_{THL}	Transition Time, High-To-Low Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 6)*	DS55461/ DS75461		10	20	ns
			DS55462/ DS75462, DS55464/ DS75464		15	20	ns
			DS55463/ DS75463		10	25	ns
V_{OH}	High-Level Output Voltage After Switching	V_S = 30V, $I_O \approx 300$ mA, *(Figure 7)*		V_S–10			mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: This is the voltage between two emitters of a multiple-emitter transistor.

Note 4: This is the maximum voltage which should be applied to any output when it is in the "OFF" state.

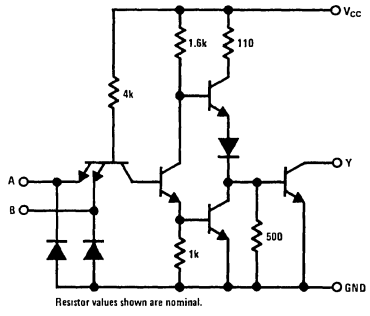
Note 5: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 6: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55XXX series and across the 0°C to +70°C range for the DS75XXX series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 7: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

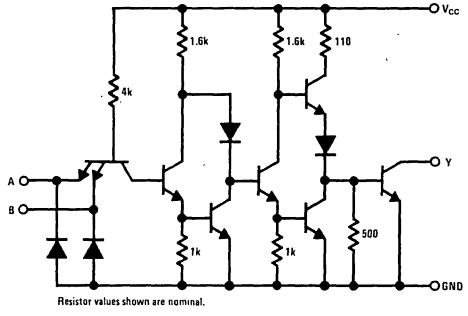
Schematic Diagrams

DS55461/DS75461



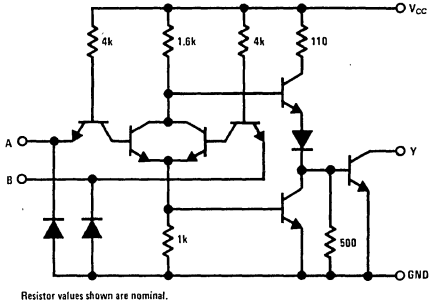
Resistor values shown are nominal.

DS55462/DS75462



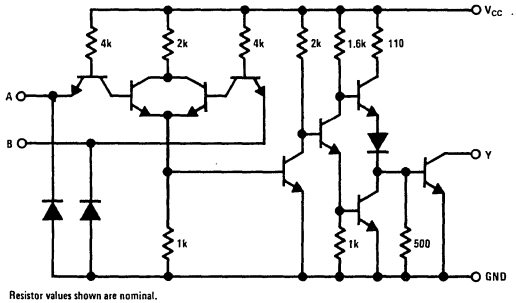
Resistor values shown are nominal.

DS55463/DS75463



Resistor values shown are nominal.

DS55464/DS75464



Resistor values shown are nominal.

Truth Tables (H = high level, L = low level)

DS55461/DS75461

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55462/DS75462

A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

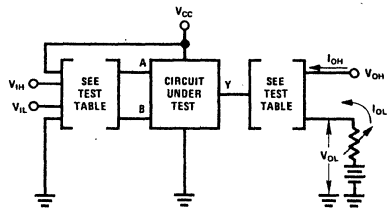
DS55463/DS75463

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55464/DS75464

A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

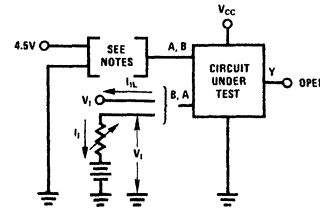
DC Test Circuits



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS55461	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS55462	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
DS55463	V_{IH} V_{IL}	Gnd V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS55464	V_{IH} V_{IL}	Gnd V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

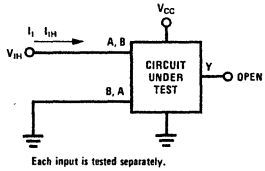
Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, I_{OH}, V_{OL}



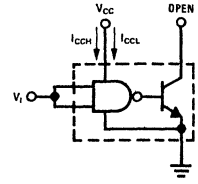
Note 1: Each input is tested separately.
Note 2: When testing DS55463/DS75463 and DS75464, input not under test is grounded.
For all other circuits it is at 4.5V.

FIGURE 2. V_I, I_{IL}



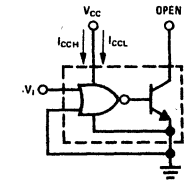
Each input is tested separately.

FIGURE 3. I_I, I_{IH}



Both gates are tested simultaneously.

FIGURE 4. I_{CCH}, I_{CCL} for AND, NAND Circuits



Both gates are tested simultaneously.

FIGURE 5. I_{CCH}, I_{CCL} for OR, NOR Circuits

Switching Characteristics

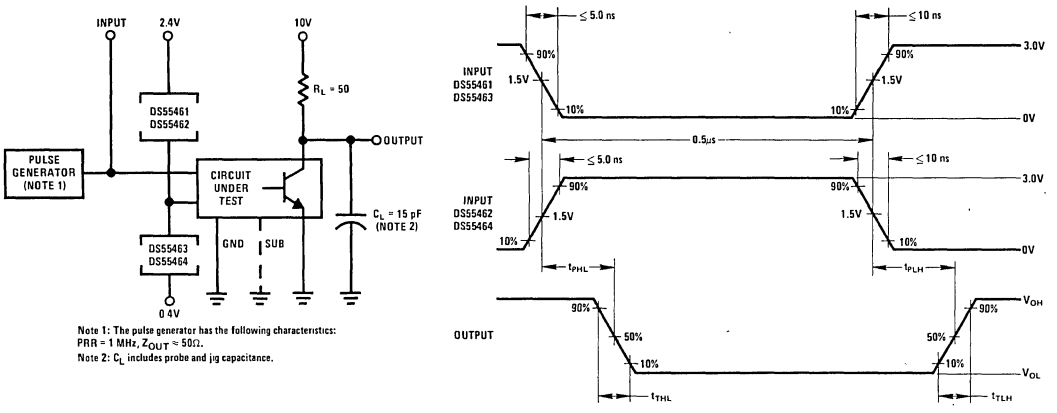


FIGURE 6. Switching Times of Complete Drivers

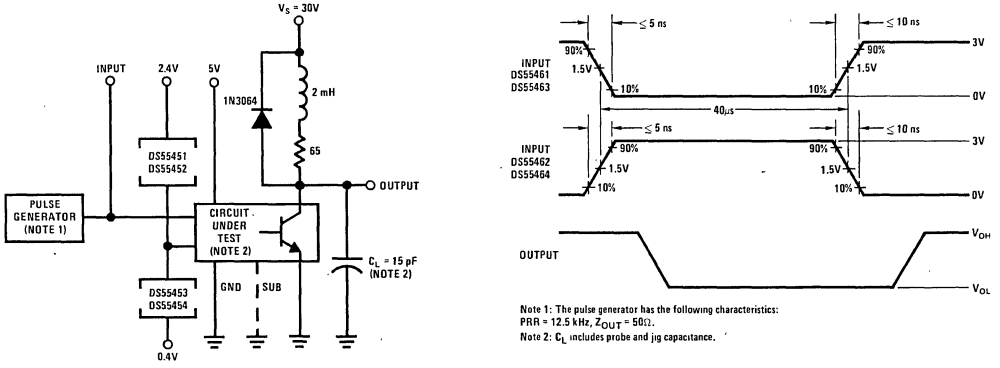


FIGURE 7. Latch-Up Test of Complete Drivers

Safe Operating Areas for Peripheral Drivers

National Semiconductor
Application Note 213
Bill Fowler
October 1978

Peripheral Drivers is a broad definition given to Interface Power devices. The devices generally have open-collector output transistors that can switch hundreds of milliamps at high voltage, and are driven by standard Digital Logic gates. They serve many applications such as: Relay Drivers, Printer Hammer Drivers, Lamp Drivers, Bus Drivers, Core Memory Drivers, Voltage Level Transistors, and etc. Most IC devices have a specified maximum load such as one TTL gate can drive ten other TTL gates. Peripheral drivers have many varied load situations depending on the application, and requires the design engineer to interpret the limitations of the device vs its application. The major considerations are *Peak Current*, *Breakdown Voltage*, and *Power Dissipation*.

OUTPUT CURRENT AND VOLTAGE CHARACTERISTICS

Figure 1 shows the circuit of a typical peripheral driver, the DS75451. The circuit is equivalent to a TTL Gate driving a 300 mA output transistor. *Figure 2* shows the characteristics of the output transistor when it is ON and when it is OFF. The output transistor is capable of sinking more than one amp of current when it is ON, and is specified at a V_{OL} = 0.7V at 300 mA. The output transistor is also specified to operate with voltages up to 30V without breaking down, but there is more to that as shown by the breakdown voltages labeled BVCES, BVCER, and LVCEO.

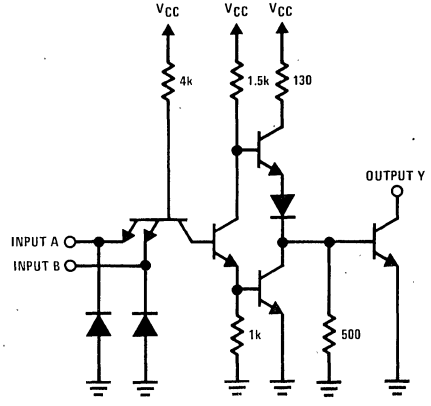


FIGURE 1. Typical Peripheral Driver DS75451

BVCES corresponds to the breakdown voltage when the output transistor is held off by the lower output transistor of the TTL gate, as would happen if the power supply (V_{CC}) was 5V. BVCER corresponds to the breakdown voltage when the output transistor is held off by the 500 resistor, as would happen if the power supply (V_{CC}) was off (0V). LVCEO corresponds to the breakdown voltage of the output transistor if it could be measured with the base open. LVCEO can be measured by exceeding the breakdown voltage BVCES and measuring the voltage at output currents of 1 to 10 mA on a transistor curve tracer (LVCEO is sometimes measured in an Inductive Latch-Up Test). Observe that all breakdown voltages converge on LVCEO at high currents, and that destructive secondary breakdown voltage occurred (shown as dotted line) at high currents and high voltage corresponding to exceeding the power dissipation of the device. The characteristics of secondary breakdown voltage vary with the length of time the condition exists, device temperature, voltage, and current.

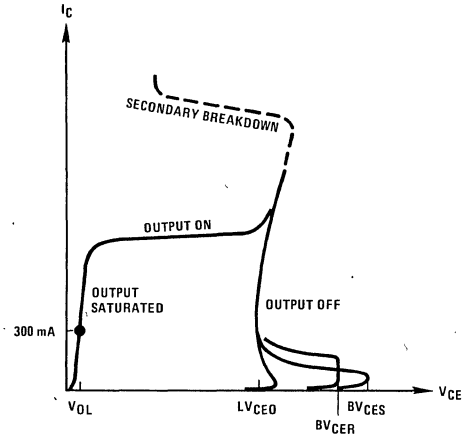


FIGURE 2. Output Characteristics ON and OFF

OUTPUT TRANSFER CHARACTERISTICS VS INDUCTIVE AND CAPACITIVE LOADS

Figure 3 shows the switching transfer characteristics superimposed on the DC characteristics of the output transistor for an inductive load. *Figure 4* shows the switching transfer characteristics for a capacitor load. In both cases in these examples, the load voltage (V_B) exceeds LVCEO. When the output transistor turns on with an inductive load the initial current through the load is 0 mA, and the transfer curve switches across to the left (V_{OL}) and slowly charges the inductor. When the output transistor turns off with an inductive load, the initial current is I_{OL}, which is sustained by the inductor and the transistor curve switches across to the right (V_B) through a high current and high voltage area which exceeds LVCEO and instead of turning off (shown as dotted line) the device goes into secondary breakdown. It is generally not a good practice to let the output transistor's voltage exceed LVCEO with an inductive load.

In a similar case with a capacitive load shown in *Figure 4*, the switching transfer characteristics rotate counter clockwise through the DC characteristics, unlike the inductive load which rotated clockwise. Even though the switching transfer curve exceeds LVCEO, it didn't

go into secondary breakdown. Therefore, it is an acceptable practice to let the output transistor voltage exceed LVCEO, but not exceed BVCER with a capacitive load.

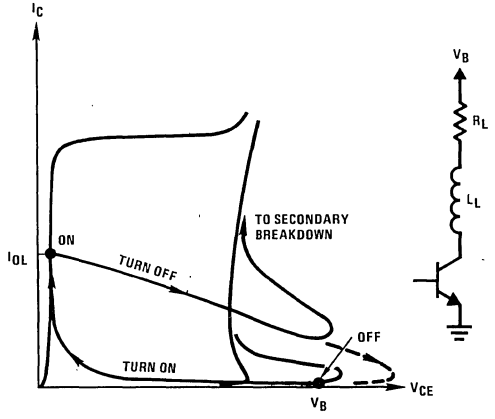


FIGURE 3. Inductive Load Transfer Characteristics

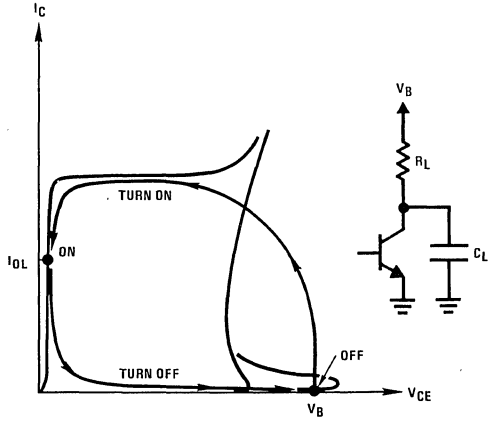


FIGURE 4. Capacitive Load Transfer Characteristics

Figure 5 shows an acceptable application with an inductive load. The load voltage (V_B) is less than LVCEO, and the inductive voltage spike caused by the initial inductive current is quenched by a diode connected to V_B.

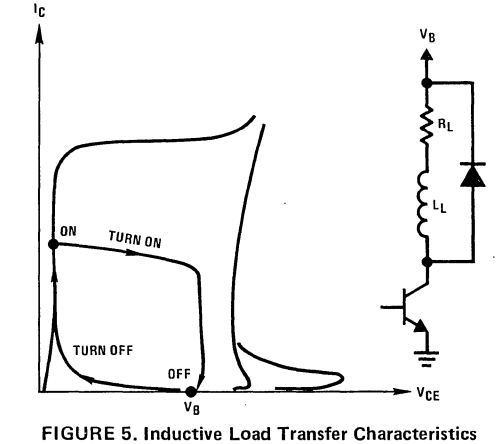


FIGURE 5. Inductive Load Transfer Characteristics Clamped by Diode

Figure 6 shows the switching transfer characteristics of a capacitive load which leads to secondary breakdown. This condition occurs due to high sustained currents, not breakdown voltage. In this example, the large capacitor prevented the output transistor from switching fast enough through the high current and high voltage region; in turn the power dissipation of the device was exceeded and the output transistor went into secondary breakdown.

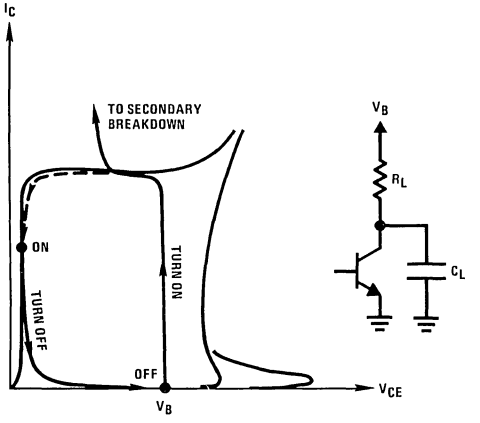


FIGURE 6. Capacitive Load Transfer Characteristics

Figure 7 shows another method of quenching the inductive voltage spike caused by the initial inductive current. This method dampens the switching response by the addition of R_D and C_D. The values of R_D and C_D are chosen to critically dampen the values of R_L and L_L; this will limit the output voltage to 2 x V_B.

$$\frac{L_L}{(R_L + R_D)} \times \sqrt{\frac{1}{L_L C_D}} \leq 0.5$$

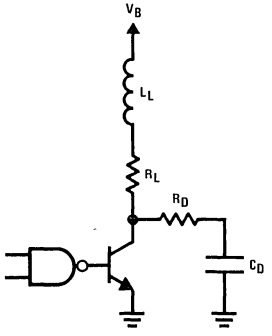


FIGURE 7. Inductive Load Dampened by Capacitor

Figure 8 shows a method of reducing high sustaining currents in a capacitive load. R_D in series with the capacitor (C_L) will limit the switching transistor without effecting final amplitude of the output voltage, since the IR drop across R_D will be zero after the capacitor is charged.

As an additional warning, beware of parasitic reactance. If the driver's load is located some distance from the driver (as an example: on the inclosure panel or through a connecting cable) there will be additional inductive and capacitance which may cause ringing on the driver

output which will exceed LVCEO or transient current that exceeds the sustaining current of the driver. A 300 mA current through a small inductor can cause a good size transient voltage, as compared with a 20 mA transient current observed with TTL gates. For no other reason than to reduce the noise associated with these transients, it is good pracitce to dampen the driver's output.

In conclusion, transient voltage associated with inductive loads can damage the peripheral driver, and transient currents associated with capacitive loads can also damage the driver. In some instances the device may not exhibit failure with the first switching cycle, but its conditions from ON to OFF will worsen after many cycles. In some cases the device will recover after the power has been turned off, but its long term reliability may have been degraded.

POWER DISSIPATION

Power Dissipation is limited by the IC Package Thermal Reactance and the external thermal reactance of the environment (PC board, heat sink, circulating air, etc.). Also, the power dissipation is limited by the maximum allowable junction temperature of the device. There are two contributions to the power: the internal bias currents and voltage of the device, and the power on the output of the device due to the Driver Load.

POWER LIMITATIONS OF PACKAGE

Figure 9 shows the equivalent circuit of a typical power device in its application. Power is shown equivalent to electrical current, thermal resistance is shown equivalent to electrical resistance, the electrical reactance C and L are equivalent to the capacity to store heat, and the propagation delay through the medium. There are two mediums of heat transfer: conduction through mass and radiant convection. Convection is insignificant compared with conduction and isn't shown in the thermal resistance circuits. From the point power is generated (device junction) there are three possible paths to the ultimate heat sink: 1. through the device leads; 2. through the device surface by mechanical connection; and 3. through the device surface to ambient air. In all cases, the thermal paths are like delay lines and have a corresponding propagation delay. The thermal resistance is proportional to the length divided by the cross sectional area of the material. The Thermal Inductance is proportional to the length of the material (copper, molding compound, etc.) and inversely proportional to the cross sectional area. The thermal capacity is proportional to the volume of the material.

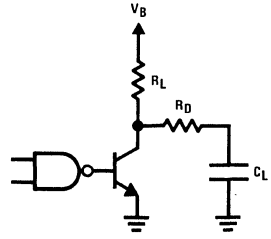


FIGURE 8. Capacitive Load with Current Limiting Resistor

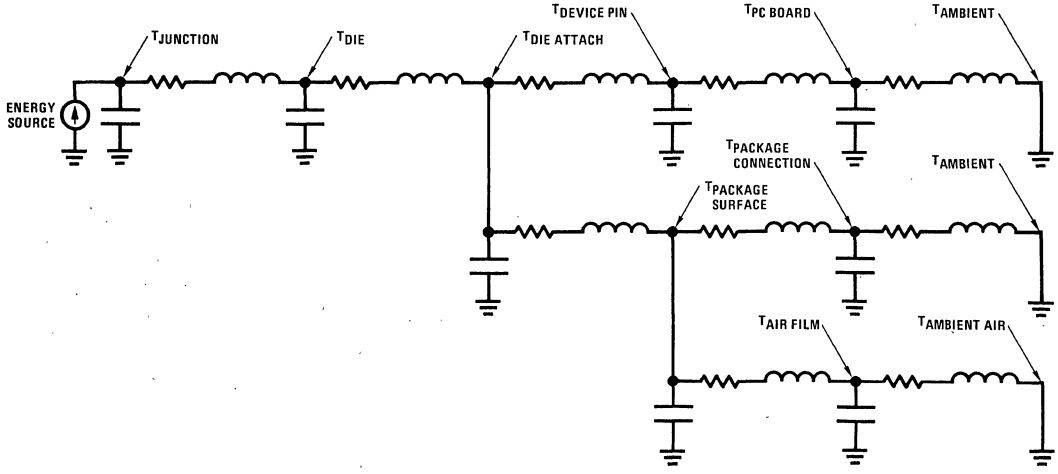


FIGURE 9. Thermal Reactance from Junction to Ambient

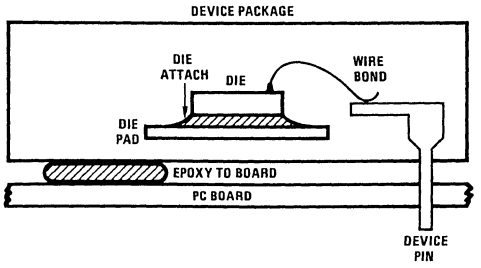


FIGURE 10. Components of Thermal Reactance for a Typical IC Package

National Semiconductor specifies the thermal resistance from device junction through the device leads soldered in a small PC board, measure in one cubic foot of still air. *Figure 11* shows the maximum package power rating for an 8 pin Molded, an 8 pin Ceramic, 14 pin Molded and a 14 pin Ceramic package. The slope of the line corresponds to thermal resistance ($\phi_{JA} = \Delta P/\Delta T$).

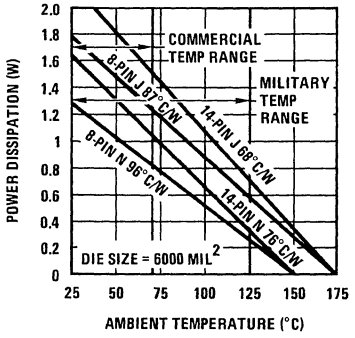


FIGURE 11. Maximum Package Power Rating

The maximum allowable junction temperature for ceramic packages is 175°C; operation above this temperature will reduce the reliability and life of the device below an acceptable level. At a temperature of 500°C the aluminum metallization paths on the die start to melt. The maximum allowable junction temperature for a molded device is 150°C, operations above this may cause the difference in thermal expansion between the molding compound and package lead frame to sheer off the wire bonds from the die to the package lead. The industry standard for a molded device is 150°C, but National further recommends operation below 135°C if the device in its application will encounter a lot of thermal cycling (such as powered on and off over its life).

The way to determine the maximum allowable power dissipation from *Figure 11*, is to project a line from the maximum ambient temperature (T_A) of the application vertically (shown dotted in *Figure 12*), until the line intercepts the diagonal line of the package type, and then project a line (shown dotted) horizontally until the line intercepts the Power Dissipation Axis (P_{MAX}).

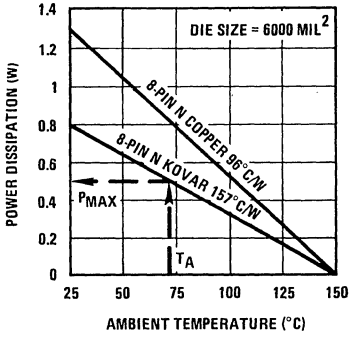


FIGURE 12. Maximum Package Rating Copper vs Kovar Lead Frame Packages

Figure 11 shows that 14 pin packages have less thermal resistance than 8 pin packages; which should be expected since it has more pins to conduct heat and has more surface area. Something that may not be expected is that the Thermal Resistance of the molded devices is comparable to the ceramic devices. The reason for the lower thermal resistance of the molded devices is the Copper lead frame, which is a better thermal conductor than the Kovar lead frame of the ceramic package. Almost all the peripheral drivers made by National Semiconductor are constructed with Copper lead frames (refer to ϕ_{JA} on the specific devices data sheet). The difference between the thermal resistance of Copper and Kovar in a molded package is shown in *Figure 12*.

Another variance in thermal resistance is the size of the IC die. If the contact area to the lead frame is greater, then the thermal resistance from the Die to the Lead Frame is reduced. This is shown in *Figure 13*. The thermal resistance shown in *Figure 11* corresponds to die that are 6000 mil^2 in area.

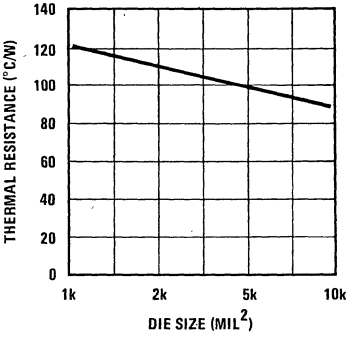


FIGURE 13. Thermal Resistance vs Die Size

In most applications the prime medium for heat conduction is through the device leads to the PC board, but the thermal resistance can be significantly improved by cooling air driven across the surface of the package. The conduction to air is limited by a stagnant film of air at the surface of the package. The film acts as an additional thermal resistance. The thickness of the film is proportional to its resistance. The thickness of the film is reduced by the velocity of the air across the package as shown in *Figure 14*. In most cases, the thermal resistance is reduced 25% at 250 linear feet/min, and 30% at 500 linear feet/min, above 500 linear feet/min the improvement flattens out.

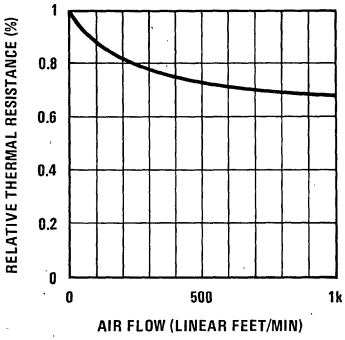


FIGURE 14. Thermal Resistance vs Air Velocity

The thermal resistance can also be improved by connecting the package to the PC board copper or by attaching metal wings to the package. The improvement by these means is outside the control of the IC manufacturer, but is available from the manufacture of the heat sink device. If the IC is mounted in a socket rather than soldered to a PC board, the thermal resistance through the device leads will worsen. In most cases, the thermal resistance is increased by 20%; again this is a variable subject to the specific socket type.

The maximum package rating shown in this note corresponds to a 90% confidence level that the package will have thermal resistance equal to or less than the value shown. The thermal resistance varies ±5% about the mean due to variables in assembly and package material.

CALCULATIONS OF POWER DISSIPATION

Most IC devices (such as T^2L) operate at power levels well below the device package rating, but peripheral drivers can easily be used at power levels that exceed the package rating unknowingly, if the power dissipation isn't calculated. As an example, the DS3654 Ten Bit Printer Driver could dissipate 3 watts (DC and, even more AC), and it is only in a 0.8 watt package. In this example, the device would be destroyed in moments, and may even burn a hole in the PC board it is mounted on. The DS3654 data sheet indicated that the 10 outputs could sink 300 mA with a Vol of 1 volt, but it wasn't intended that all the outputs would be at the same time, and if so, not for a long period. The use of the DS3654 requires that the power be calculated vs the duty cycle of the outputs.

The DC power dissipation is pretty obvious, but in another example, a customer used the DS3686 relay driver to drive a 6.5 H inductive load. The DS3687 has an internal clamp network to quench the inductive back swing at 60V. At 5 Hz the device dissipates 2 watts, with transient peaks up to 11 watts. After 15 minutes of operation, the driver succumbs to thermal overload and becomes non-functional. The DS3687 was intended for telephone relay, which in most applications switches 20 times a day.

Peripheral driver will dissipate peak power levels that greatly exceed the average DC power. This is due to the capacity of the die and package to consume the transient energy while still maintaining the junction temperature at a safe level. This capacity is shown as a capacitor in *Figure 9*. In the lab (under a microscope) a device may be observed to glow orange around the parameter of the junction under excessive peak power without damage to the device. *Figure 15* shows a plot of maximum peak power vs applied time for the DS3654, and the same information plotted as energy vs applied time. To obtain these curves, the device leakage current when it switches off was used to monitor device limitation. Note in *Figure 15* there is a transition in the curve about 10 μs. At this point, the thermal capacity of the die has been exceeded. The thermal delay to the next thermal capacity (the package) was too long, and limited the peak power. These levels are not suggested operating levels, but an example of a Peripheral Driver to handle peak transient power.

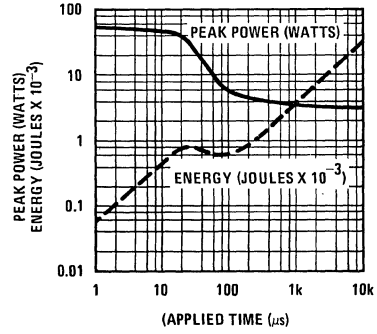


FIGURE 15. Peak Power and Energy vs the Period of Time the Power was Applied

To calculate power dissipation, the only information available to the design engineer is the parametric limits in the device data sheet, and the same information about the load reactance. If the calculations indicate the device is within its limits of power dissipation, then using those parametric limits is satisfactory. If the calculation of power dissipation is marginal, the parametric limits used in the calculations might be worst case at low temperature instead of high temperature

due to a positive temperature coefficient (T_C) of resistance. IC resistors and resistors associated with the load generally have a positive T_C. On the other hand, diodes and transistor emitter base voltages have a negative T_C; which may in some circuits negate the effect of the resistors T_C. Peripheral output transistors have a positive T_C associated with V_{OL}; while output Darlington transistors have a negative T_C at low currents and may be flat at high currents. *Figure 16* shows an example of power dissipation vs temperature; note that the power dissipation at the applications maximum temperature (T_A) was less than the power dissipation at lower temperatures. Since maximum junction temperature is the concern of the calculation, then maximum ambient temperature power should be used. The junction temperature may be determined by projecting a line (shown dotted in *Figure 16*), with a slope proportional to ϕ_{JA} back to the horizontal axis (shown as T_J). If the point is below the curve then T_J will be less than 150°C. T_J must not exceed the maximum junction temperature for that package type. In this example, T_J is less than 150°C as required by a molded package. To calculate the power vs temperature, it is necessary to characterize the device parameters vs temperature. Unfortunately, this information is not always provided by IC manufacturers in the device data sheets. A method to calculate I_{CC} vs temperature is to measure a device, then normalize the measurements vs the typical value for I_{CC} in the data sheet, then worst case the measurements by adding 30%. Thirty percent is normally the worst-case resistor tolerance that IC devices are manufactured to.

CALCULATION OF OUTPUT POWER WITH AN INDUCTIVE LOAD

For this example, the device output circuit is similar to the DS3654 (10-Bit Printer Solenoid Driver) and the DS3686 and DS3687 (Telephone Relay Driver) as shown in *Figure 17*. Special features of the circuit type are the Darlington output transistors Q1 and Q2 and the zener diode from the collector of Q2 to the base of Q2. The Darlington output requires very little drive from the logic gate driving it and in turn dissipates less power when the output is turned ON and OFF, than a single saturating transistor output would. The zener diode (D_Z) quenches the inductive backswing when the output is turned OFF.

Device and Load Characteristics Used for Power Calculation

V_{OL}	Output Voltage ON	1.5V
V_C	Output Clamp Voltage	65V
V_B	Load Voltage	30V
R_L	Load Resistance	120 Ω
L_L	Load Inductance	5h
T_{ON}	Period ON	100 ms
T_{OFF}	Period OFF	100 ms
T	Total Period	200 ms

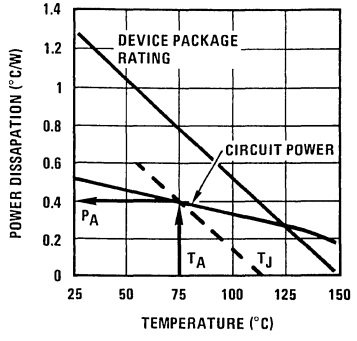


FIGURE 16. IC Power Dissipation vs Temperature

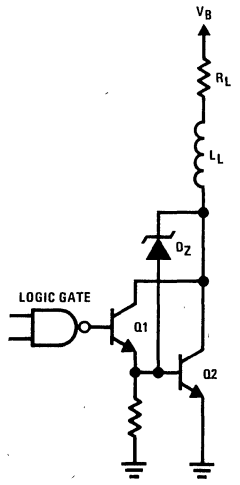


FIGURE 17. Peripheral Driver with Inductive Load

Refer to *Figure 18* voltage and current waveforms corresponding to the power dissipation calculated for this example of an inductive load.

P_{ON} = Average power dissipation in device output when device is ON during total period (T)

$$\tau = \frac{L_L}{R_L} = \frac{5h}{120\ \Omega} = 41.7\ ms$$

$$I_L = \frac{V_B - V_{OL}}{R_L} = \frac{30 - 1.5}{120} = 237.5\ mA$$

$$I_P = I_L\,(1 - e^{-T_{ON}/\tau})$$

$$I_P = 237.5\ mA\ (1 - e^{-100\ ms/41.7\ ms})$$

$$I_P = 215.9\ mA$$

$$P_{ON} = V_{OL} \times I_L \times \frac{T_{ON}}{T}\left[1 - \int_o^{T_{ON}} \frac{e^{-t/\tau}\,dt}{T_{ON}}\right]$$

$$P_{ON} = V_{OL} \times I_L \times \frac{T_{ON}}{T}\left[1 - \frac{\tau}{T_{ON}}\,(1 - e^{-T_{ON}/\tau})\right]$$

$$P_{ON} = 1.5 \times 237.5\ mA \times \frac{100}{200}\left[1 - \frac{41.7}{100}(1 - e^{-100/41.7})\right]$$

$$P_{ON} = 110.6\ mW$$

P_{OFF} = Average power dissipation in device output when device is OFF during total period (T)

$$I_R = \frac{V_C - V_B}{R_L} = \frac{65 - 30}{120\ \Omega} = 291.7\ mA$$

$$t_x = \tau\,\ell n\left(\frac{I_L + I_R}{I_R}\right)$$

$$t_x = 41.7\ ms\ \ell n\left(\frac{219.8 + 291.7}{291.7}\right) = 23.1\ ms$$

$$P_{OFF} = V_C \times \frac{t_x}{T}\left[(I_P + I_R) \int_o^{t_x} \frac{e^{-t/\tau}dt}{t_x} - I_R\right]$$

$$P_{OFF} = V_C \times \frac{t_x}{T}\left[(I_P + I_R) \times \frac{\tau}{t_x}\,(1 - e^{-t_x/\tau}) - I_R\right]$$

$$P_{OFF} = 65 \times \frac{23.1}{200}\left[(215.9\ mA + 291.7\ mA)\ \frac{41.7}{23.1}\right.$$

$$\left.(1 - e^{-23.1/41.7}) - 291.7\ mA\right]$$

$$P_{OFF} = 736\ mW$$

P_O = Average power dissipation in device output

$$P_O = P_{ON} + P_{OFF} = 110.6 + 736 = 846.6\ mW$$

In the above example, driving a 120 Ω inductive load at 5 Hz, the power dissipation exceeded a more simple calculation of power dissipation, which would have been:

$$P_O = \frac{V_{OL}\,(V_B - V_{OL})}{R_L} \times \frac{T_{ON}}{T}$$

$$P_O = \frac{1.5\,(30 - 1.5)}{120} \times \frac{100\ ms}{200\ ms} = 182.5\ mW$$

An error 460% would have occurred by not including the reactive load. The total power dissipation must also include other outputs (if the device has more than one output), and the power dissipation due to the device power supply currents. This is an example where the load will most likely exceed the device package rating. If the load is fixed, the power can be reduced by changing the period (T) and duty rate (T_{ON}/T_{OFF}).

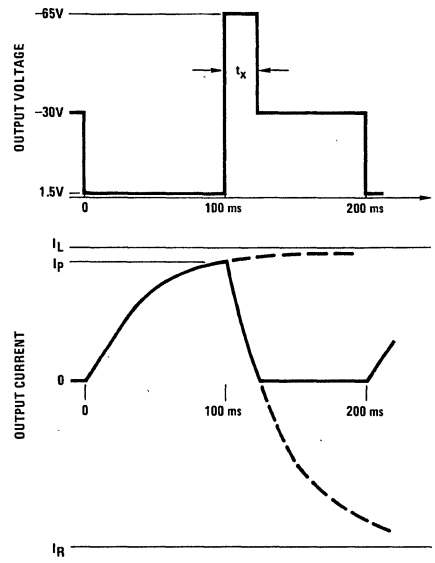


FIGURE 18. Voltage and Current Waveforms Corresponding to Inductive Load.

CALCULATION OF OUTPUT POWER WITH AN INCANDESCENT LAMP

An incandescent lamp is equivalent to a reactive load. The reactance is related to the period of time required to heat the lamp and the filaments positive temperature coefficient of resistance. *Figure 19* shows the transient response for a typical lamp used on instrument panels, and the equivalent electrical model for the lamp. Much like IC packages the lamp has a thermal circuit and its associated propagation delay. This lamp filament has an 8 ms time constant, and a longer 250 ms time constant from the lamp body to ambient. The DC characteristics are shown in *Figure 20*. Note the knee in the characteristics at 2 volts; this is where power starts to be dissipated in the form of light. This subject is important, since more peripheral drivers are damaged by lamps than any other load.

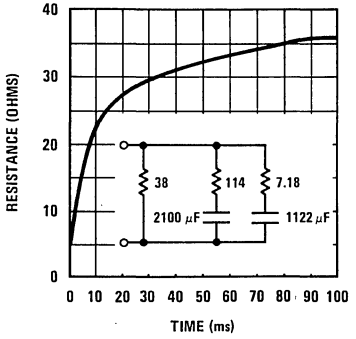


FIGURE 19. Transient Response of an Incandescent Lamp

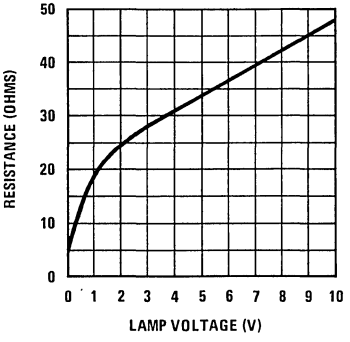


FIGURE 20. DC Characteristics of an Incandescent Lamp

Figure 21 shows the transient response of a driver similar to a DS75451 driving the lamp characterized in *Figures 19 and 20*. The equivalent load doesn't include the reactance of the lamp base to ambient, which has a 250 ms time constant, since 10 ms to an IC is equivalent to DC. The peak transient current was 1 amp, settling to 200 ms, with an 8 ms time constant. Observe the peak current is clamped at 1 amp, by the sinking ability of the driver; otherwise the peak current may have been 1.2 amps. The DS75451 is only rated at 300 mA, but it is reasonable to assume it could sink 1 amp because of the designed forced β required for switching response and worst case operating temperature.

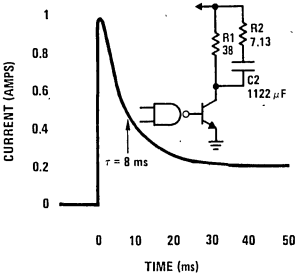


FIGURE 21. Transient Incandescent Lamp Current

Calculation of the energy dissipated by a peripheral driver for the transient lamp current shown in *Figure 21* is shown below, and the plot of energy vs time is shown in *Figure 22*. *Figure 22* also includes as a reference the maximum peak energy from *Figure 15*. It can be seen from *Figure 22* that in this example there is a good safety margin between the lamp load and the reference max peak energy. If there were more drivers than one per package under the same load, the margin would have been reduced. Also, if the peripheral driver couldn't saturate because it couldn't sink the peak transient lamp current, then the energy would also reduce the margin of safe operation.

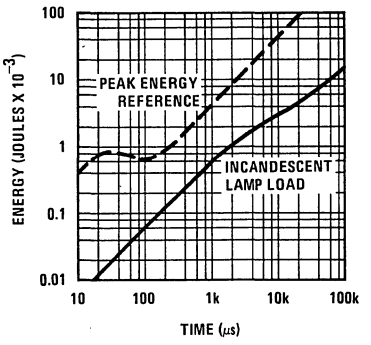


FIGURE 22. Energy vs Time for a Peripheral Driver with an Incandescent Lamp Load

CALCULATION OF ENERGY IN AN INCANDESCENT LAMP

$$\text{Energy} = \int_0^t V_{OL}\,(I_{R1} + I_{R2})\,dt$$

$$i_{R1} = \frac{V_B - V_{OL}}{R1} = I_{R1}$$

$$i_{R2} = \left(\frac{V_B - V_{OL}}{R2}\right) e^{-t/\tau}$$

$$= I_{R2}\, e^{-t/\tau} \qquad \tau = R2C2$$

$$\text{Energy} = \int_0^t V_{OL}\,(I_{R1} + I_{R2}\, e^{-t/\tau})\,dt$$

$$= V_{OL}\quad [I_{R1}t + I_{R2}\tau\,(i - e^{-t/\tau})]$$

Given: $V_{OL} = 0.6V$
$I_{R1} = 0.2$ Amps
$I_{R1} + I_{R2} = 1$ Amp

A common technique used to reduce the 10 to 1 peak to DC transient lamp current is to bias the lamp partially ON, so the lamp filament is warm. This can be accomplished as shown in *Figure 23*. From *Figure 20* it can be seen that the lamp resistance at 0V is 5.7 Ω, but at 1V the resistance is 18 Ω. At 1V the lamp doesn't start to emit light. Using a lamp resistance of 100 Ω and lamp voltage of 1V, R_B was calculated to be approximately 100 Ω. This circuit will reduce the peak lamp current from 1 amp to 316 mA.

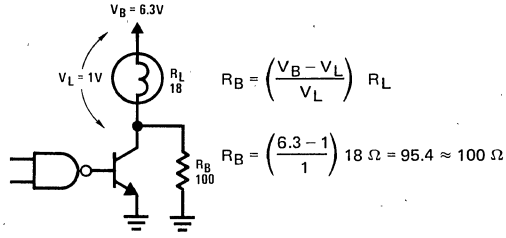


FIGURE 23. Circuit Used to Reduce Peak Transient Lamp Current

PERIPHERAL DRIVER SECTION

National Semiconductor has a wide selection of peripheral drivers as shown in the selection guide, *Figure 24*. The DS75451, DS75461, DS3631 and the DS3611 series have the same selection of logic function in an 8-pin package. The DS75461 is a high voltage selection of the DS75451 and may switch slower. The DS3611 and DS3631 are very high voltage circuits and were intended for slow relay applications. The DS3680, DS3686, and DS3687 were intended for 56V telephone relay applications. The DS3654 contains a 10-bit shift register followed by ten 250 mA clamped drivers. The DS3654 was intended for printer solenoid applications.

High current and high voltage peripheral drivers find many applications associated with digital systems, and it is the intention of the application note to insure that reliability and service life of peripheral drivers equal or exceed the performance of the other logic gates made by National.

For additional information, please contact Digital Interface Marketing Manager at National or one of the many field application engineers world wide.

Output High Voltage (V)	Latch-Up Voltage (Note 3) (V)	Output Low Voltage (V)	Output Low Current (mA)	Propagation Delay Typ (ns)	ON Power Supply Current (mA)	Drivers/ Package	Input Compatibility (Logic)	Logic Function (Driver ON)	Device Number and Temperature Range	
									0°C to +70°C	−55°C to +125°C
30		0.5	100	40	152	8	TTL	Note 5	DP8310	DP7310
30		0.5	100	40	125	8	TTL	Note 6	DP8311	DP7311
20	13.5	0.6	100	70	90	2	TTL	Note 7	DS3616	
65	30	1.5	600		65	4	TTL/LS	NAND	DS3656	
70	35	0.7	600	2430	65	4	TTL/LS	NAND	DS3658	
70	Note 8	1.5	600	2000	80	4	TTL/LS	NAND	DS3668	
70	35	0.7	600		65	4	TTL/LS	AND	DS3669	
30	20	0.7	300	31	55	2	TTL	AND	DS75450	
30	20	0.7	300	31	55	2	TTL	AND	DS75451	DS55451
30	20	0.7	300	31	55	2	TTL	NAND	DS75452	DS55452
30	20	0.7	300	31	55	2	TTL	OR	DS75453	DS55453
30	20	0.7	300	31	55	2	TTL	NOR	DS75454	DS55454
35	30	0.7	300	33	55	2	TTL	AND	DS75461	DS55461
35	30	0.7	300	33	55	2	TTL	NAND	DS75462	DS55462
35	30	0.7	300	33	55	2	TTL	OR	DS75463	DS55463
35	30	0.7	300	33	55	2	TTL	NOR	DS75464	DS55464
56	40	1.4	300	150	8	2	CMOS	AND	DS3631	DS1631
56	40	1.4	300	150	8	2	CMOS	NAND	DS3632	DS1632
56	40	1.4	300	150	8	2	CMOS	OR	DS3633	DS1633
56	40	1.4	300	150	8	2	CMOS	NOR	DS3634	DS1634
80	50	0.7	300	125	75	2	TTL/CMOS	AND	DS3611	DS1611
80	50	0.7	300	125	75	2	TTL/CMOS	NAND	DS3612	DS1612
80	50	0.7	300	125	75	2	TTL/CMOS	OR	DS3613	DS1613
80	50	0.7	300	125	75	2	TTL/CMOS	NOR	DS3614	DS1614
−2.1	−60	−60	−50	10,000	4.4	4	TTL/CMOS	(Note 4)	DS3680	
(Note 1)	56	1.3	300	1000	28	2	TTL/CMOS	NAND	DS3686	
(Note 1)	−56	−1.3	300	1000	28	2	TTL/CMOS	NAND	DS3687	DS1687
13.5	15	$V_{CC}-1.8$	300	150	0.015	2	CMOS	AND	MM74C908, MM74C918	
(Note 1)	45	1.6	250	1000	70	10	(Note 2)	(Note 2)	DS3654	

Note 1: The DS3686, DS3687 and DS3654 contain an internal inductive fly-back clamp circuit connected from the output to ground. As an example, DS3686 driving a relay solenoid connected to 28V would clamp the output voltage fly-back transient at 56V caused by the solenoid's stored inductive current. This clamp protects the circuit output and quenches the fly-back.

Note 2: The DS3654 is a 10-bit shift register followed by 10 enabled drivers. The input circuit is equivalent to a 4k resistor to ground, and the logic input thresholds are 2.8V and 0.8V. The recommended power supply voltage is 7.5V to 9.5V. The circuit can be cascaded to be a 20 or 30-bit shift register.

Note 3: Latch-up voltage is the maximum voltage the output can sustain when switching an inductive load.

Note 4: DS3680 has a differential input circuit.

Note 5: DP8310 inverting, positive edge latching.

Note 6: DP8311 inverting, fall through latch.

Note 7: Bubble memory coil driver.

Note 8: DS3668 35V, latch-up with output fault protection.

FIGURE 24. Peripheral/Power Driver Selection Guide

Section 4
Level Translators/ Buffers

4

TEMPERATURE RANGE		DESCRIPTION	PAGE NUMBER
−55 °C to +125 °C	0 °C to +70 °C		
—	DP8480	10k ECL to TTL Level Translator with Latch	4-4
—	DP8481	TTL to 10k ECL Level Translator with Latch	4-7
—	DP8482	100k ECL to TTL Level Translator with Latch	4-10
—	DP8483	TTL to 100k Level Translator with Latch	4-13
DS1630	DS3630	Hex CMOS Compatible Buffer	4-16
*DS7800	DS8800	Dual Voltage Level Translator	4-19
*DS7810	DS8810	Quad 2-Input TTL-to-MOS Interface Gate	4-22
*DS7811	DS8811	Quad 2-Input TTL-to-MOS Interface Gate	4-22
*DS7812	DS8812	Hex TTL-to-MOS Inverter	4-22
*DS78L12	DS88L12	Hex TTL-to-MOS Inverter/Interface Gate	4-25
*DS7819	DS8819	Quad 2-Input TTL-to-MOS Gate	4-27
MM54C901	MM74C901	Hex Inverting TTL Buffer	CMOS
MM54C902	MM74C902	Hex Non-Inverting TTL Buffer	CMOS
MM54C903	MM74C903	Hex Inverting PMOS Buffer	CMOS
MM54C904	MM74C904	Hex Non-Inverting PMOS Buffer	CMOS
MM54C906	MM74C906	Hex Open Drain N-Channel Buffer	CMOS
MM54C907	MM74C907	Hex Open Drain P-Channel Buffer	CMOS

*Also available screened in accordance with MIL-STD-883 Class B. Refer to National Semiconductor's "The Reliability Handbook".

LEVEL TRANSLATORS/BUFFERS

INPUT	OUTPUT	OUTPUT CHARACTERISTICS	LOGIC FUNCTION	DEVICE NUMBER		Page No.
				0°C to +70°C	−55°C to +125°C	
10k ECL	TTL	TRI-STATE® Fall Through Latch	Inverting	DP8480		4-4
TTL	10k ECL	Gated Fall Through Latch	Inverting	DP8481		4-7
100k ECL	TTL	TRI-STATE Fall Through Latch	Inverting	DP8482		4-10
TTL	100k ECL	Gated Fall Through Latch	Inverting	DP8483		4-13
CMOS	CMOS	50 ns Prop. Delay at 500 pF	Hex Buffer	DS3630	DS1630	4-16
TTL	PMOS	Open-Collector −30V to 30V	Dual 2-Input Gate	DS8800	DS7800	4-19
TTL	MOS	Open-Collector 0.4V to 14V	Quad 2-Input Gate	DS8810	DS7810	4-22
TTL	MOS	Open-Collector 0.4V to 14V	Quad 2-Input Gate	DS8811	DS7811	4-22
TTL	MOS	Open-Collector 0.4V to 14V	Hex Inverter	DS8812	DS7812	4-22
TTL	MOS	Active Pull-Up 0.4V to 14V	Hex Inverter	DS88L12	DS78L12	4-25
TTL	MOS	Open-Collector 0.4V to 14V	Quad 2-Input Gate	DS8819	DS7819	4-27
CMOS	TTL	Active Pull-Up 0.4V @ 2.6 mA	Hex Inverter	MM74C901	MM54C901	CMOS
CMOS	TTL	Active Pull-Up 0.4V @ 3.2 mA	Hex Buffer	MM74C902	MM54C902	CMOS
CMOS	PMOS	Active Pull-Up 0V to 15V	Hex Inverter	MM74C903	MM54C903	CMOS
CMOS	PMOS	Active Pull-Up 0V to 15V	Hex Buffer	MM74C904	MM54C904	CMOS
CMOS	NMOS	Open Drain 0V to 15V	Hex Buffer	MM74C906	MM54C906	CMOS
CMOS	PMOS	Open Drain V_{CC} to V_{CC} − 15V	Hex Buffer	MM74C907	MM54C907	CMOS

National Semiconductor

Level Translators/Buffers
PRELIMINARY

DP8480 10k ECL to TTL Level Translator with Latch

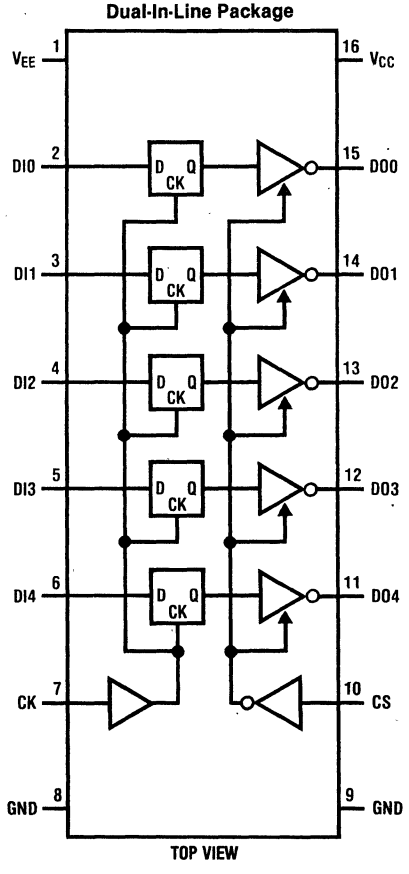
General Description

This circuit translates ECL input levels to TTL output levels and provides a fall-through latch. The TRI-STATE® outputs are designed to drive large capacitive loads. The clock and chip select inputs are ECL.

Features

- 16-pin flat-pack or DIP
- TRI-STATE outputs
- ECL control inputs
- 5.5 ns typical propagation delay with 50 pF load
- Outputs are TRI-STATE during power up/down for glitch free operation
- 10k ECL input compatible

Logic and Connection Diagram



Truth Table

DI	DO	CK	CS
H	L	L	L
L	H	L	L
X	DO	H	L
X	Hi-Z	X	H

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number DP8480N or DP8480F
See NS Package N16A or F16B

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Note 1)

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage	GND to V_{EE}
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Storage Temperature	−65°C to 150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−5.2V ± 10%
V_{CC} Supply Voltage	5.0V ± 10%
T_A, Ambient Temperature	0°C to 75°C

Electrical Characteristics (TTL Logic) Notes 2, 3 and 4

Parameter		Conditions	Min	Typ	Max	Units
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA	2.5			V
I_{0D}	Output Low Drive Current	Force 5V with Output Low		150		mA
I_{1D}	Output High Drive Current	Force 0V with Output High		−150		mA
I_{OZ}	TRI-STATE Output Current			1		μA
I_{CC}	Supply Current				62.5	mA

Electrical Characteristics (ECL Logic) Notes 2 and 3

Parameter		Conditions	T_A	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	V_{EE} = −5.2V	0°C 25°C 75°C	−1870 −1850 −1830		−1490 −1475 −1450	mV
V_{IH}	Input High Voltage	V_{EE} = −5.2V	0°C 25°C 75°C	−1145 −1105 −1045		−840 −810 −720	mV
I_{IL}	Input Low Current				0.5		μA
I_{IH}	Input High Current				350		μA
I_{EE}	Supply Current					−50	mA

Switching Characteristics Notes 2 and 5

Parameter		Conditions	Min	Typ	Max	Units
t_{CDOL}	Clock to Data Out Low Delay	C_L = 50 pF		6.75	11.5	ns
t_{CDOH}	Clock to Data Out High Delay	C_L = 50 pF		6.75	11.5	ns
t_{DIDOH}	Data In to Data Out High Delay	C_L = 50 pF		5.5	9.5	ns
t_{DIDOL}	Data In to Data Out Low Delay	C_L = 50 pF		5.5	9.5	ns
t_S	Data Set-Up Time	C_L = 50 pF	3.0	1.0		ns
t_H	Data Hold Time	C_L = 50 pF	3.0	1.0		ns
t_{CPW}	Clock Pulse Width	C_L = 50 pF	5.0	3.0		ns
t_{ZE}	Delay from Chip Select to Active State from Hi-Z State	C_L = 50 pF		8		ns
t_{EZ}	Delay from Chip Select to Hi-Z State from Active State	C_L = 50 pF		8		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

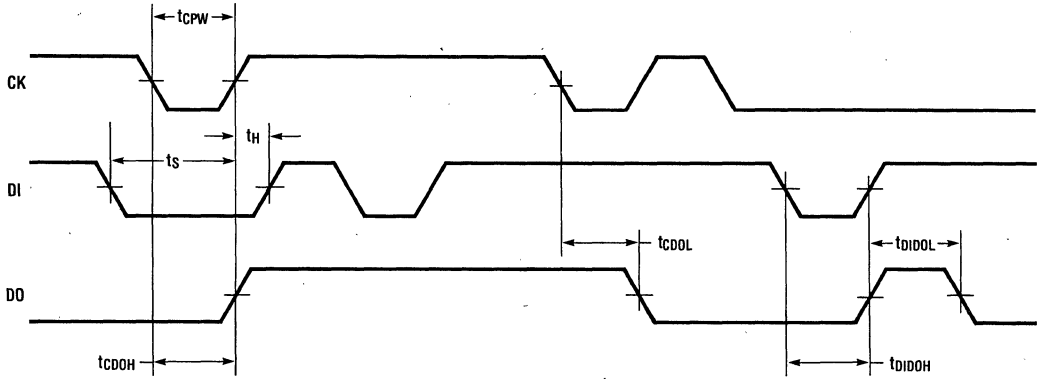
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 75°C ambient temperature range in still air and across the specified supply variations. All typical values are for T_A = 25°C and nominal supply.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

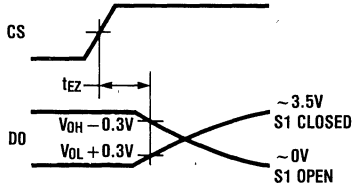
Note 4: When DC testing I_{1D} or I_{0D} a 15Ω resistor should be in series with the output. Only one output should be tested at a time.

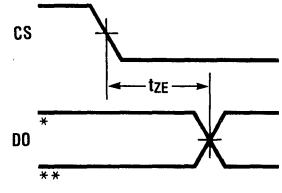
Note 5: Unless otherwise specified, all AC measurements are referenced from the 50% level of the ECL input to the 0.8V level on negative transitions or the 2.4V level on positive transitions of the output. ECL input rise and fall times are 2.0 ns ± 0.2 ns from 20% to 80%.

Switching Time Waveforms



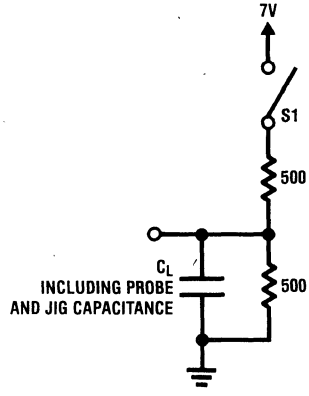
S1 open





*S1 closed
**S1 open

Test Load



National Semiconductor

Level Translators/Buffers
PRELIMINARY

DP8481 TTL to 10k ECL Level Translator with Latch

General Description

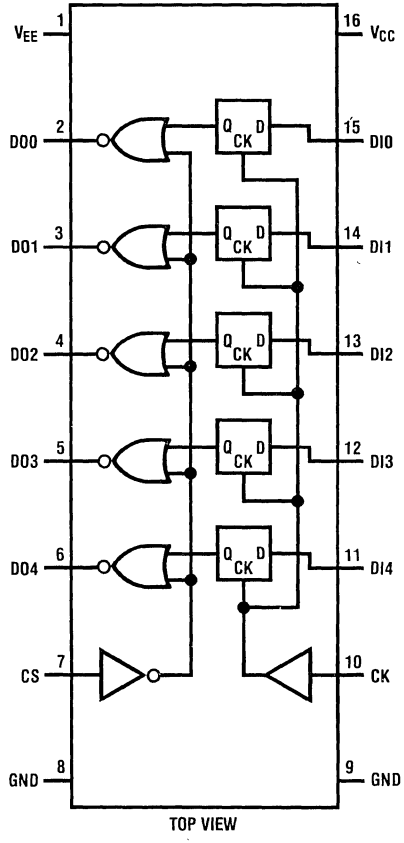
This circuit translates TTL input levels to ECL output levels and provides a fall-through latch. The outputs are gated with CS providing for wire ORing of outputs. The clock and chip select inputs are ECL.

Features

- 16-pin flat-pack or DIP
- ECL control inputs
- CS provided for wire ORing of output bus
- 10k ECL I/O compatible
- 4.0 ns typical propagation delay

Logic and Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Table

DI	DO	CK	CS
H	L	L	H
L	H	L	H
X	DO	H	H
X	L	X	L

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number DP8481N or DP8481F
See NS Package N16A or F16B

Absolute Maximum Ratings (Note 1)

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage (ECL)	GND to V_{EE}
Input Voltage (TTL)	−1V to 5.5V
Output Current	50 mA
Maximum Power Dissipation* at 25°C Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−5.2V ± 10%
V_{CC} Supply Voltage	5.0V ± 10%
T_A, Ambient Temperature	0°C to 75°C

Electrical Characteristics (TTL Logic) Notes 2 and 3

Parameter		Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{IL}	Input Low Current	$V_{IN} = 0.5V$		−50		μA
I_{IH}	Input High Current	$V_{IN} = 2.5V$		1.0		μA
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -12$ mA		−0.8		V
I_{CC}	Supply Current				30	mA

Electrical Characteristics (ECL Logic) Notes 2 and 3

Parameter		Conditions	T_A	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	$V_{EE} = -5.2V$	0°C 25°C 75°C	−1870 −1850 −1830		−1490 −1475 −1450	mV
V_{IH}	Input High Voltage	$V_{EE} = -5.2V$	0°C 25°C 75°C	−1145 −1105 −1045		−840 −810 −720	mV
I_{IL}	Input Low Current				0.5		μA
I_{IH}	Input High Current				350		μA
V_{OL}	Output Low Voltage	$V_{EE} = -5.2V$	0°C 25°C 75°C	−1870 −1850 −1830		−1665 −1650 −1625	mV
V_{OH}	Output High Voltage	$V_{EE} = -5.2V$	0°C 25°C 75°C	−1000 −960 −900		−840 −810 −720	mV
V_{OLC}	Output Low Voltage	$V_{EE} = -5.2V$	0°C 25°C 75°C			−1645 −1630 −1605	mV
V_{OHC}	Output High Voltage	$V_{EE} = -5.2V$	0°C 25°C 75°C	−1020 −980 −920			mV
I_{EE}	Supply Current					−90	mA

Switching Characteristics Notes 2 and 4

Parameter		Conditions	Min	Typ	Max	Units
t_{CDOL}	Clock to Data Out Low Delay			4.0	6.5	ns
t_{CDOH}	Clock to Data Out High Delay			4.0	6.5	ns
t_{DIDOH}	Data In to Data Out High Delay			4.0	6.5	ns
t_{DIDOL}	Data In to Data Out Low Delay			4.0	6.5	ns
t_S	Data Set-Up Time to Clock		3.0	1.0		ns
t_H	Data Hold Time		3.0	1.0		ns
t_{CPW}	Clock Pulse Width		5.0	3.0		ns
t_{CSDOH}	Chip Select to Data Out High Delay			3.0	4.5	ns
t_{CSDOL}	Chip Select to Data Out Low Delay			3.0	4.5	ns
t_{SCS}	Data Set-Up Time to Chip Select		5.5	3.0		ns

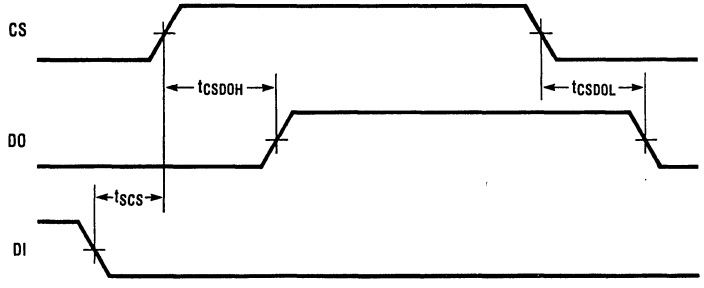
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

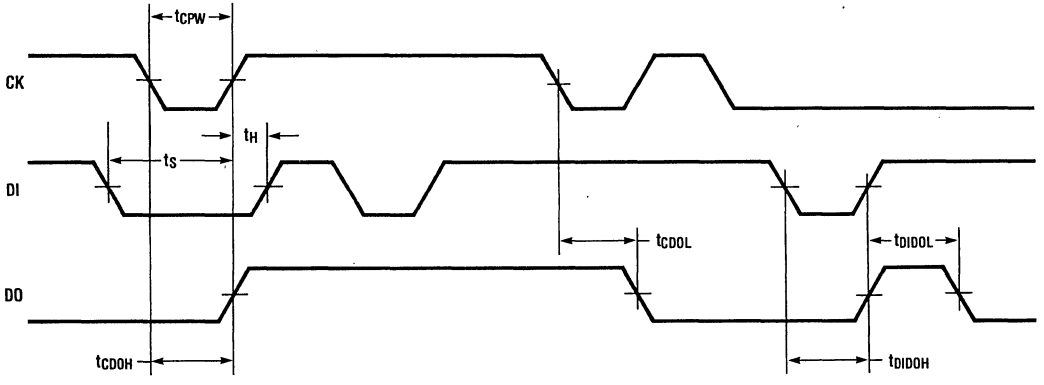
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 75°C ambient temperature range in still air and across the specified supply variations. All typical values are for 25°C and nominal supply.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: Unless otherwise specified, all AC measurements are referenced from the 1.5V level of the TTL input and to/from the 50% point of the ECL signal and a 50Ω resistor to −2V is the load. ECL input rise and fall times are 2.0 ns ± 0.2 ns from 20% to 80%. TTL input characteristic is 0V to 3V with $t_r = t_f \leq 3$ ns measured from 10% to 90%.

Switching Time Waveforms





National Semiconductor

Level Translators/Buffers
PRELIMINARY

DP8482 100k ECL to TTL Level Translator with Latch

General Description

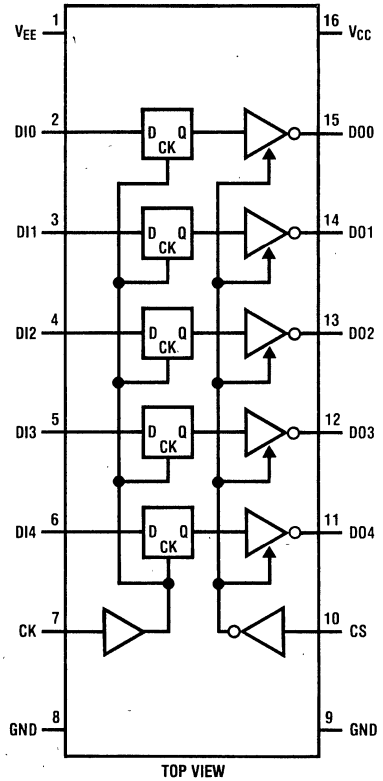
This circuit translates ECL input levels to TTL output levels and provides a fall-through latch. The TRI-STATE® outputs are designed to drive large capacitive loads. The clock and chip select inputs are ECL.

Features

- 16-pin flat-pack or DIP
- TRI-STATE outputs
- ECL control inputs
- 5.5 ns typical propagation delay with 50 pF load
- Outputs are TRI-STATE during power up/down for glitch free operation
- 100k ECL input compatible

Logic and Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Table

DI	DO	CK	CS
H	L	L	L
L	H	L	L
X	DO	H	L
X	Hi-Z	X	H

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number DP8482N or DP8482F
See NS Package N16A or F16B

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Note 1)

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage	GND to V_{EE}
Output Voltage	5.5V
Maximum Power Dissipation* at 25°C	
Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−4.5V ± 7%
V_{CC} Supply Voltage	5.0V ± 10%
T_A, Ambient Temperature	0°C to 85°C

Electrical Characteristics (TTL Logic) Notes 2, 3 and 4

Parameter		Conditions	Min	Typ	Max	Units
V_{OL}	Output Low Voltage	I_{OL} = 8 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH} = −1 mA	2.5			V
I_{0D}	Output Low Drive Current	Force 5V with Output Low		150		mA
I_{1D}	Output High Drive Current	Force 0V with Output High		−150		mA
I_{OZ}	TRI-STATE Output Current			1		μA
I_{CC}	Supply Current				62.5	mA

Electrical Characteristics (ECL Logic) Notes 2 and 3

Parameter		Conditions	T_A	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	V_{EE} = −4.5V		−1810		−1475	mV
V_{IH}	Input High Voltage	V_{EE} = −4.5V		−1165		−880	mV
I_{IL}	Input Low Current				0.5		μA
I_{IH}	Input High Current				350		μA
I_{EE}	Supply Current					−50	mA

Switching Characteristics Notes 2 and 5

Parameter		Conditions	Min	Typ	Max	Units
t_{CDOL}	Clock to Data Out Low Delay	C_L = 50 pF		6.75	11.5	ns
t_{CDOH}	Clock to Data Out High Delay	C_L = 50 pF		6.75	11.5	ns
t_{DIDOH}	Data In to Data Out High Delay	C_L = 50 pF		5.5	9.5	ns
t_{DIDOL}	Data In to Data Out Low Delay	C_L = 50 pF		5.5	9.5	ns
t_S	Data Set-Up Time	C_L = 50 pF	3.0	1.0		ns
t_H	Data Hold Time	C_L = 50 pF	3.0	1.0		ns
t_{CPW}	Clock Pulse Width	C_L = 50 pF	5.0	3.0		ns
t_{ZE}	Delay from Chip Select to Active State from Hi-Z State	C_L = 50 pF		8		ns
t_{EZ}	Delay from Chip Select to Hi-Z State from Active State	C_L = 50 pF		8		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

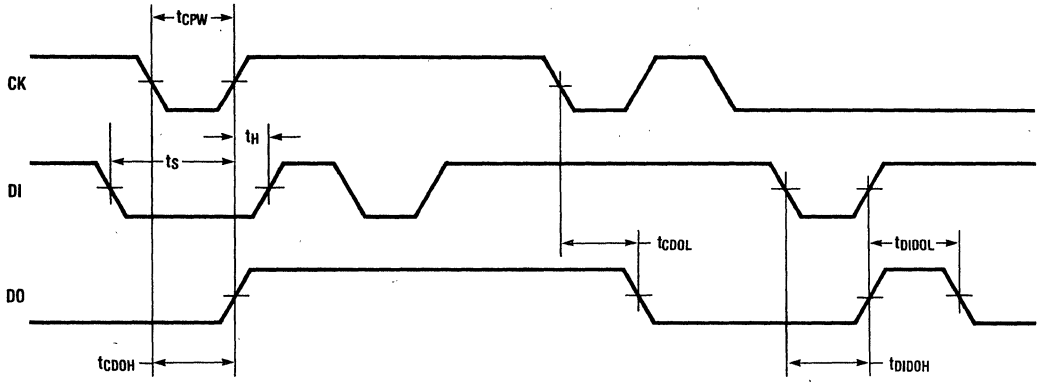
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 85°C ambient temperature range in still air and across the specified supply variations. All typical values are for T_A = 25°C and nominal supply.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

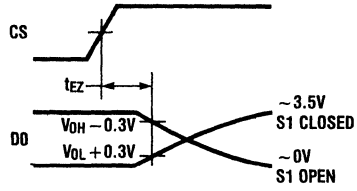
Note 4: When DC testing I_{1D} or I_{0D} a 15Ω resistor should be in series with the output. Only one output should be tested at a time.

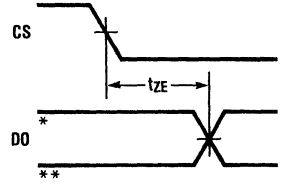
Note 5: Unless otherwise specified, all AC measurements are referenced from the 50% level of the ECL input to the 0.8V level on negative transitions or the 2.4V level on positive transitions of the output. ECL input rise and fall times are 0.7 ns ± 0.1 ns from 20% to 80%.

Switching Time Waveforms



S1 open

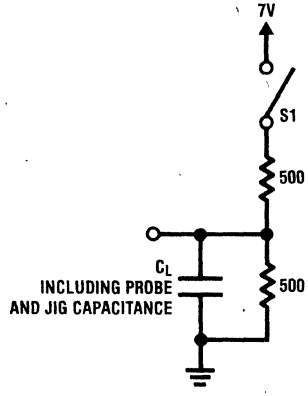




*S1 closed

**S1 open

Test Load



National Semiconductor

Level Translators/Buffers
PRELIMINARY

DP8483 TTL to 100k ECL Level Translator with Latch

General Description

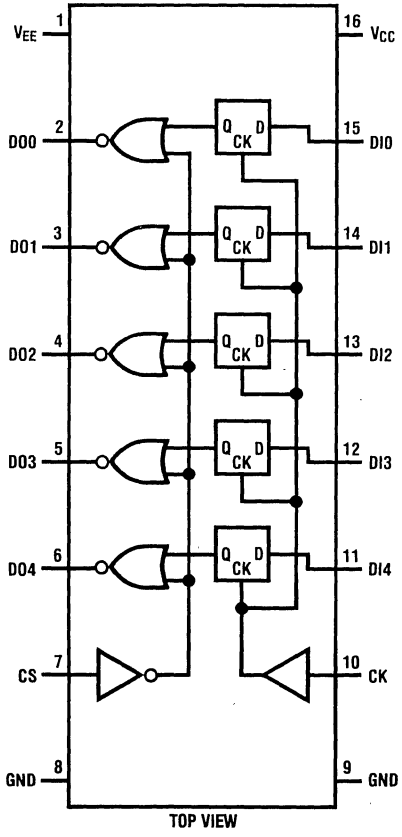
This circuit translates TTL input levels to ECL output levels and provides a fall-through latch. The outputs are gated with CS providing for wire ORing of outputs. The clock and chip select inputs are ECL.

Features

- 16-pin flat-pack or DIP
- ECL control inputs
- CS provided for wire ORing of output bus
- 100k ECL I/O compatible
- 4.0 ns typical propagation delay

Logic and Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Table

DI	DO	CK	CS
H	L	L	H
L	H	L	H
X	DO	H	H
X	L	X	L

H = high level (most positive)
L = low level (most negative)
X = don't care

Order Number DP8483N or DP8483F
See NS Package N16A or F16B

Absolute Maximum Ratings (Note 1)

V_{EE} Supply Voltage	−8V
V_{CC} Supply Voltage	7V
Input Voltage (ECL)	GND to V_{EE}
Input Voltage (TTL)	−1V to 5.5V
Output Current	50 mA
Maximum Power Dissipation* at 25°C Molded Package	1476 mW
Storage Temperature	−65°C to +150°C

*Derate molded package 11.8 mW/°C above 25°C.

Recommended Operating Conditions

V_{EE} Supply Voltage	−4.5V ± 7%
V_{CC} Supply Voltage	5.0V ± 10%
T_A, Ambient Temperature	0°C to 85°C

Electrical Characteristics (TTL Logic) Notes 2 and 3

Parameter		Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.0			V
I_{IL}	Input Low Current	V_{IN} = 0.5V		−50		μA
I_{IH}	Input High Current	V_{IN} = 2.5V		1.0		μA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA		−0.8		V
I_{CC}	Supply Current				30	mA

Electrical Characteristics (ECL Logic) Notes 2 and 3

Parameter		Conditions	T_A	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	V_{EE} = −4.5V		−1810		−1475	mV
V_{IH}	Input High Voltage	V_{EE} = −4.5V		−1165		−880	mV
I_{IL}	Input Low Current				0.5		μA
I_{IH}	Input High Current				350		μA
V_{OL}	Output Low Voltage	V_{EE} = −4.5V		−1810	−1705	−1620	mV
V_{OH}	Output High Voltage	V_{EE} = −4.5V		−1025	−955	−880	mV
V_{OLC}	Output Low Voltage	V_{EE} = −4.5V				−1610	mV
V_{OHC}	Output High Voltage	V_{EE} = −4.5V		−1035			mV
I_{EE}	Supply Current					−90	mA

Switching Characteristics Notes 2 and 4

Parameter		Conditions	Min	Typ	Max	Units
t_{CDOL}	Clock to Data Out Low Delay			4.0	6.5	ns
t_{CDOH}	Clock to Data Out High Delay			4.0	6.5	ns
t_{DIDOH}	Data In to Data Out High Delay			4.0	6.5	ns
t_{DIDOL}	Data In to Data Out Low Delay			4.0	6.5	ns
t_S	Data Set-Up Time to Clock		3.0	1.0		ns
t_H	Data Hold Time		3.0	1.0		ns
t_{CPW}	Clock Pulse Width		5.0	3.0		ns
t_{CSDOH}	Chip Select to Data Out High Delay			3.0	4.5	ns
t_{CSDOL}	Chip Select to Data Out Low Delay			3.0	4.5	ns
t_{SCS}	Data Set-Up Time to Chip Select		5.5	3.0		ns

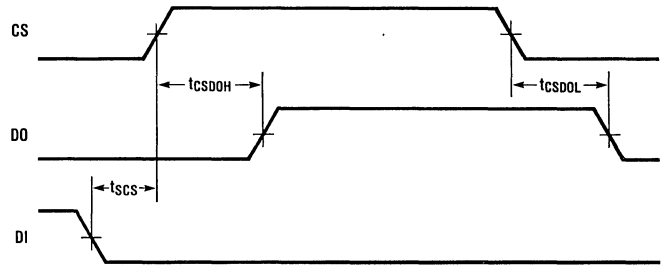
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

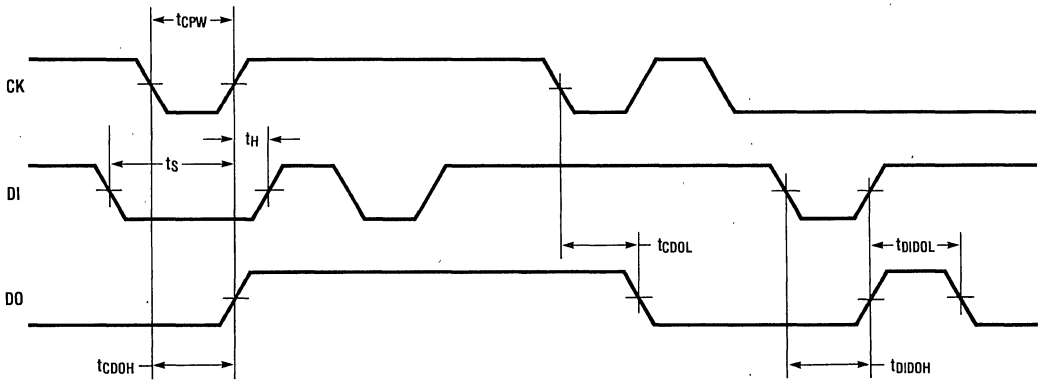
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 85°C ambient temperature range in still air and across the specified supply variations. All typical values are for 25°C and nominal supply.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative. All voltages are referenced to ground, unless otherwise specified.

Note 4: Unless otherwise specified, all AC measurements are referenced from the 1.5V level of the TTL input and to/from the 50% point of the ECL signal and a 50Ω resistor to −2V is the load. ECL input rise and fall times are 0.7 ns ± 0.1 ns from 20% to 80%. TTL input characteristic is 0V to 3V with $t_r = t_f \leq 3$ ns measured from 10% to 90%.

Switching Time Waveforms





National Semiconductor

DS1630/DS3630 Hex CMOS Compatible Buffer

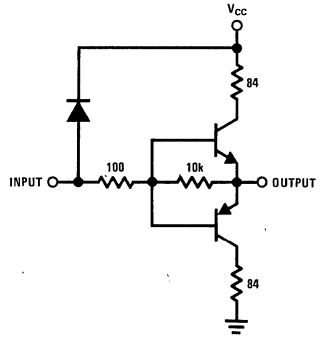
General Description

The DS1630/DS3630 is a high current buffer intended for use with CMOS circuits interfacing with peripherals requiring high drive currents. The DS1630/DS3630 features low quiescent power consumption (typically 50μW) as well as high-speed driving of capacitive loads such as large MOS memories. The design of the DS1630/DS3630 is such that V_{CC} current spikes commonly found in standard CMOS circuits cannot occur, thereby, reducing the total transient and average power when operating at high frequencies.

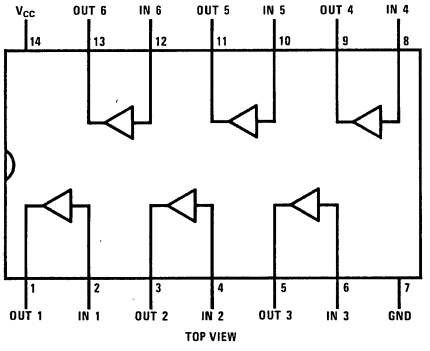
Features

- High-speed capacitive driver
- Wide supply voltage range
- Input/output may interface to TTL
- Input/output CMOS compatibility
- No internal transient V_{CC} current spikes
- 50μW typical standby power

Equivalent Schematic and Connection Diagrams

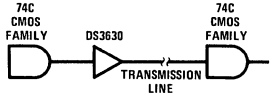


Dual-In-Line Package

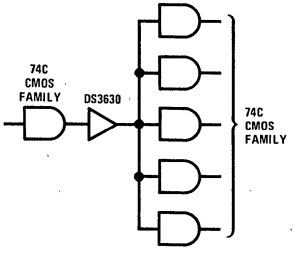


Order Number DS1630J, DS3630J or DS3630N
See NS Package J14A or N14A

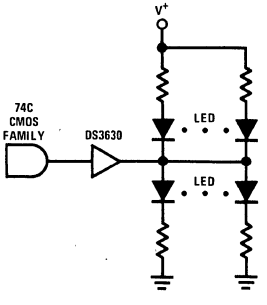
Typical Applications



CMOS To Transmission Line Interface



CMOS To CMOS Interface



LED Driver

Absolute Maximum Ratings (Note 1)

Supply Voltage	16V
Input Voltage	16V
Output Voltage	16V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	3	15	V
Temperature (T_A)			
DS1630	−55	+125	°C
DS3630	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{INH} Logical "1" Input Current	$V_{IN} = V_{CC}$, $I_{OUT} = -400\mu A$	DS1630		90	200	μA
		DS3630		90	200	μA
	$V_{IN} = V_{CC} - 2.0V$, $I_{OUT} = 16$ mA	DS1630		0.5	3.2	mA
		DS3630		0.5	1.5	mA
I_{INL} Logical "0" Input Current	$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		−0.15	−1	mA
		DS3630		$V_{CC}-150$	−800	μA
V_{OH} Logical "1" Output Voltage	$V_{IN} = V_{CC}$, $I_{OUT} = -400\mu A$	DS1630	$V_{CC}-1$	$V_{CC}-0.75$		V
		DS3630	$V_{CC}-0.9$	$V_{CC}-0.75$		V
	$V_{IN} = V_{CC} - 0.4V$, $I_{OUT} = 16$ mA	DS1630	$V_{CC}-2.5$	$V_{CC}-2.0$		V
		DS3630	$V_{CC}-2.5$	$V_{CC}-2.0$		V
V_{OL} Logical "0" Output Voltage	$V_{IN} = 0V$, $I_{OUT} = 400\mu A$	DS1630		0.75	1	V
		DS3630		0.75	0.9	V
	$V_{IN} = 0V$, $I_{OUT} = 16$ mA	DS1630		0.95	1.3	V
		DS3630		0.95	1.3	V
	$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		1.2	1.6	V
		DS3630		1.2	1.5	V

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0} Propagation Delay to a Logical "0"	$C_L = 50$ pF		30	45	ns
	$C_L = 250$ pF		40	60	ns
	$C_L = 500$ pF		50	75	ns
t_{pd1} Propagation Delay to a Logical "1"	$C_L = 50$ pF		15	25	ns
	$C_L = 250$ pF		35	50	ns
	$C_L = 500$ pF		50	75	ns

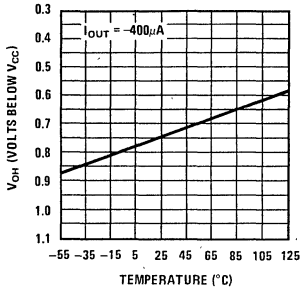
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1630 and across the 0°C to +70°C range for the DS3630. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

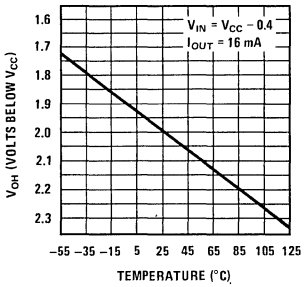
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Performance Characteristics

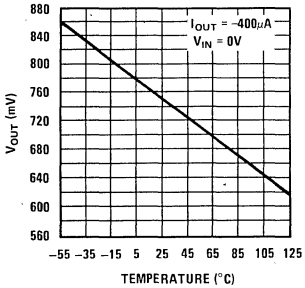
V_{OH} vs Temperature, $V_{IN} = V_{CC}$



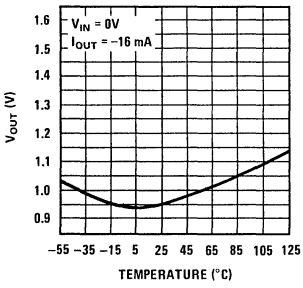
V_{OH} Active vs Temperature



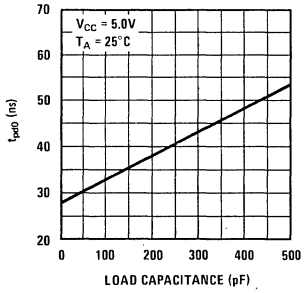
V_{OL} vs Temperature



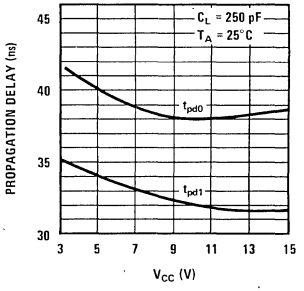
V_{OL} vs Temperature



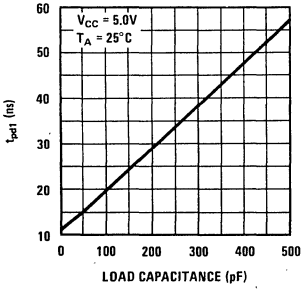
t_{pdo} vs Load Capacitance



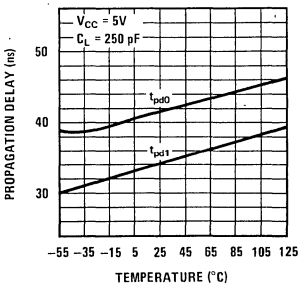
Propagation Delay vs V_{CC}



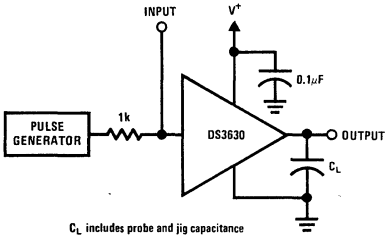
t_{pd1} vs Load Capacitance



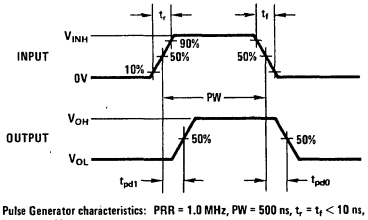
Propagation Delay vs Temperature



AC Test Circuit and Switching Time Waveforms



C_L includes probe and jig capacitance



Pulse Generator characteristics: PRR = 1.0 MHz, PW = 500 ns, $t_r = t_f < 10$ ns, V_{IN} = 0 to V_{CC}

National Semiconductor

DS7800/DS8800 Dual Voltage Level Translator

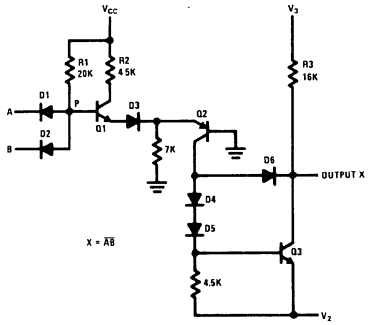
General Description

The DS7800/DS8800 are dual voltage translators designed for interfacing between conventional TTL or LS voltage levels and those levels associated with high impedance junction or MOS FET-type devices. The design allows the user a wide latitude in his selection of power supply voltages, thus providing custom control of the output swing. The translator is especially useful in analog switching; and since low power dissipation occurs in the "off" state, minimum system power is required.

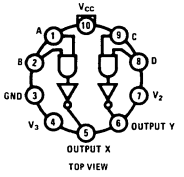
Features

- 31 volt (max) output swing
- 1 mW power dissipation in normal state
- Standard 5V power supply
- Temperature range:
  DS7800 −55°C to +125°C
  DS8800 0°C to +70°C
- Compatible with all MOS devices

Schematic and Connection Diagrams



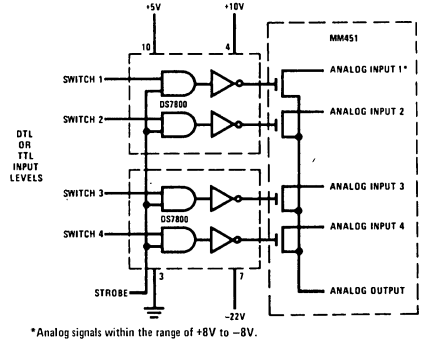
Metal Can Package



Order Number DS7800H
or DS8800H
See NS Package H10C

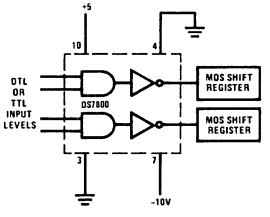
Typical Applications

4-Channel Analog Switch



*Analog signals within the range of +8V to −8V.

Bipolar to MOS Interfacing



Absolute Maximum Ratings (Note 1)

V_{CC} Supply Voltage	7.0V
V2 Supply Voltage	−30V
V3 Supply Voltage	30V
V3-V2 Voltage Differential	40V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Maximum Power Dissipation* at 25°C	690 mW
Metal Can (TO-5) Package	

*Derate metal can package 4.6 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7800	4.5	5.5	V
DS8800	4.75	5.25	V
Temperature (T_A)			
DS7800	−55	+125	°C
DS8800	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP (NOTE 6)	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			5	μA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−0.2	−0.4	mA
I_{OL}	Output Sink Current	V_{CC} = Min, V_{IN} = 2V, V3 Open	DS7800	1.6			mA
			DS8800	2.3			mA
I_{OH}	Output Leakage Current	V_{CC} = Max, V_{IN} = 0.8V (Notes 4 and 7)				10	μA
R_O	Output Collector Resistor	T_A = 25°C		11.5	16.0	20.0	kΩ
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V (Note 7)				V_2 + 2.0	V
$I_{CC(MAX)}$	Power Supply Current Output "ON"	V_{CC} = Max, V_{IN} = 4.5V (Note 5)			0.85	1.6	mA
$I_{CC(MIN)}$	Power Supply Current Output "OFF"	V_{CC} = Max, V_{IN} = 0V (Note 5)			0.22	0.41	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Transition Time to Logical "0" Output	T_A = 25°C, C = 15 pF (Note 8)	25	70	125	ns
t_{pd1}	Transition Time to Logical "1" Output	T_A = 25°C, C = 15 pF (Note 9)	25	62	125	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7800 and across the 0°C to +70°C range for the DS8800.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Current measured is drawn from V_3 supply.

Note 5: Current measured is drawn from V_{CC} supply.

Note 6: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V, V_2 = −22V, V_3 = +8V.

Note 7: Specification applies for all allowable values of V_2 and V_3.

Note 8: Measured from 1.5V on input to 50% level on output.

Note 9: Measured from 1.5V on input to logic "0" voltage, plus 1V.

Theory of Operation

The two input diodes perform the AND function on TTL input voltage levels. When at least one input voltage is a logical "0", current from V_{CC} (nominally 5.0V) passes through R_1 and out the input(s) which is at the low voltage. Other than small leakage currents, this current drawn from V_{CC} through the 20 kΩ resistor is the only source of power dissipation in the logical "1" output state.

When both inputs are at logical "1" levels, current passes through R_1 and diverts to transistor Q_1, turning it on and thus pulling current through R_2. Current is then supplied to the PNP transistor, Q_2. The voltage losses caused by current through Q_1, D_3, and Q_2 necessitate that node P reach a voltage sufficient to overcome these losses before current begins to flow. To achieve this voltage at node P, the inputs must be raised to a voltage level which is one diode potential lower than node P. Since these levels are exactly the same as those experienced with conventional TTL, the interfacing with these types of circuits is achieved.

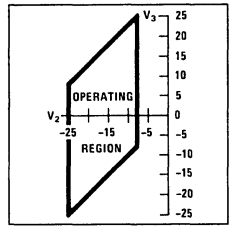
Transistor Q_2 provides "constant current switching" to the output due to the common base connection of Q_2. When at least one input is at the logical "0" level, no current is delivered to Q_2; so that its collector supplies essentially zero current to the output stage. But when both inputs are raised to a logical "1" level current is supplied to Q_2. Since this current is relatively constant, the collector of Q_2 acts as a constant current source for the output stage. Logic inversion is performed since logical "1" input voltages cause current to be supplied to Q_2 and to Q_3. And when Q_3 turns on the output voltage drops to the logical "0" level.

The reason for the PNP current source, Q_2, is so that the output stage can be driven from a high impedance. This allows voltage V_2 to be adjusted in accordance with the application. Negative voltages to −25V can be applied to V_2. Since the output will neither source nor sink large amounts of current, the output voltage range is almost exclusively dependent upon the values selected for V_2 and V_3.

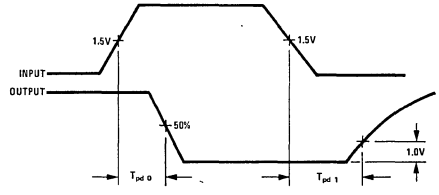
Maximum leakage current through the output transistor Q_3 is specified at 10 μA under worst-case voltage between V_2 and V_3. This will result in a logical "1" output voltage which is 0.2V below V_3. Likewise the clamping action of diodes D_4, D_5, and D_6, prevents the logical "0" output voltage from falling lower than 2V above V_2, thus establishing the output voltage swing at typically 2 volts less than the voltage separation between V_2 and V_3.

Selecting Power Supply Voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V_2 is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V_3 is governed by supply V_2. With a value chosen for V_2, V_3 may be selected as any value along a vertical line passing through the V_2 value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



Switching Time Waveforms



National Semiconductor

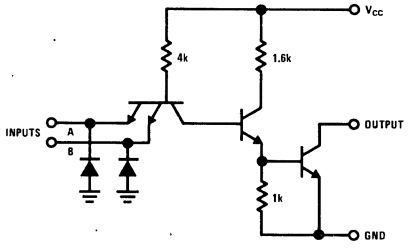
DS7810/DS8810 Quad 2-Input TTL-MOS Interface Gate
DS7811/DS8811 Quad 2-Input TTL-MOS Interface Gate
DS7812/DS8812 Hex TTL-MOS Inverter

General Description

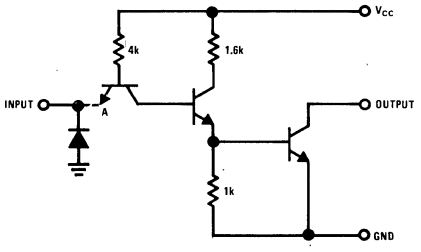
These Series 54/74 compatible gates are high output voltage versions of the DM5401/DM7401 (SN5401/SN7401), DM5403/DM7403 (SN5403/SN7403), and DM5405/DM7405 (SN5405/SN7405). Their open-collector outputs may be "pulled-up" to +14 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

In addition the devices may be used in applications where it is desirable to drive low current relays or lamps that require up to 14 volts.

Schematic and Connection Diagrams

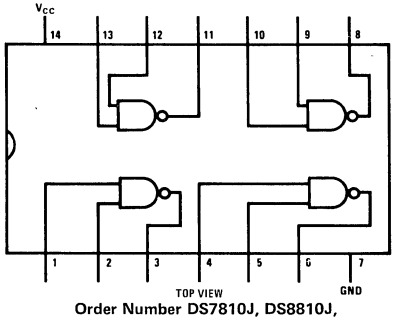


DS7810/DS8810, DS7811/DS8811



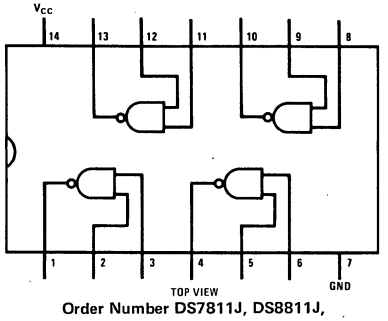
DS7812/DS8812

Dual-In-Line Package



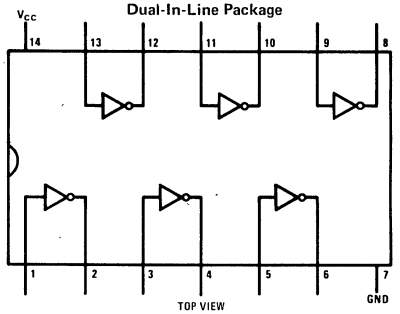
Order Number DS7810J, DS8810J, or DS8810N
See NS Package J14A or N14A

Dual-In-Line Package



Order Number DS7811J, DS8811J, DS7811W or DS8811N
See NS Package J14A, N14A or W14A

Dual-In-Line Package



Order Number DS7812J, DS8812J, DS7812W or DS8812N
See NS Package J14A, N14A or W14A

Absolute Maximum Ratings (Note 1)

V_{CC}	7V
Input Voltage	5.5V
Output Voltage	14V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1254 mW
Molded Package	1106 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 8.36 mW/°C above 25°C; derate molded package 8.85 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS78XX	4.5	5.5	V
DS88XX	4.75	5.25	V
Temperature (T_A)			
DS78XX	−55	+125	°C
DS88XX	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{CLAMP}	Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{OH}	Logical "1" Output Current	V_{CC} = Min,	V_{IN} = 0.8V			250	μA
		V_{OUT} = 10V	V_{IN} = 0.0V			40	μA
I_{OL}	Logical "0" Output Current	V_{CC} = Min, V_{IN} = 2.0V, V_{OUT} = 0.4V		16			mA
V_{OH}	Logical "1" Output Breakdown Voltage	V_{CC} = Min, V_{IN} = 0V, I_{OUT} = 1 mA		14			V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V, I_{OUT} = 16 mA				0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.6	mA
$I_{CC(MAX)}$	Logical "0" Supply Current (Each Gate)	V_{CC} = Max, V_{IN} = 5.0V			3.0	5.1	mA
$I_{CC(MIN)}$	Logical "1" Supply Current (Each Gate)	V_{CC} = Max, V_{IN} = 0V			1.0	1.8	mA

Switching Characteristics T_A = 25°C, V_{CC} = 5V

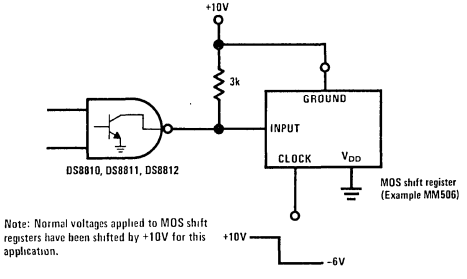
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay Time to a Logical "0"	C_{OUT} = 15 pF, R_L = 1k	4	12	18	ns
t_{pd1}	Propagation Delay Time to a Logical "1"		18	29	45	ns

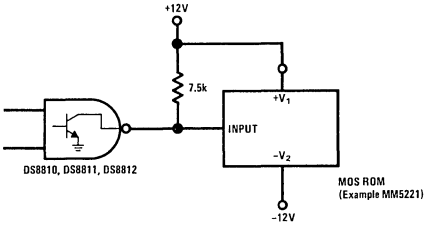
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range " they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7810, DS7811, and DS7812 and across the 0°C to +70°C range for the DS8810, DS8811, and DS8812.

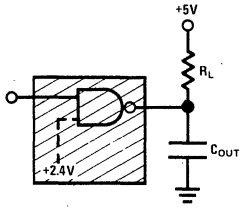
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

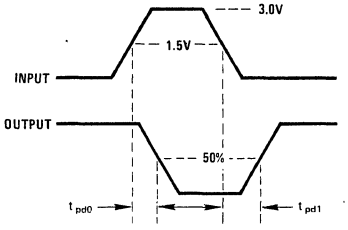
Typical Applications





AC Test Circuit and Switching Time Waveforms





f = 1 MHz
$t_r = t_f = 10$ ns
PW = 100 ns

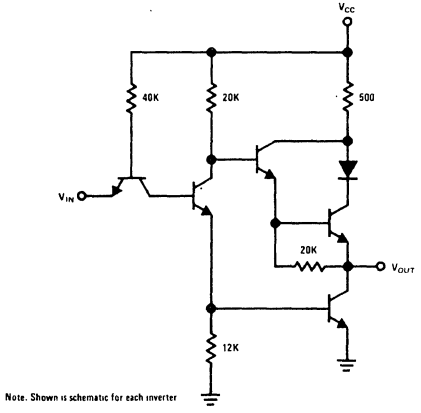
National Semiconductor

DS78L12/DS88L12 Hex TTL-MOS Inverter/Interface Gate

General Description

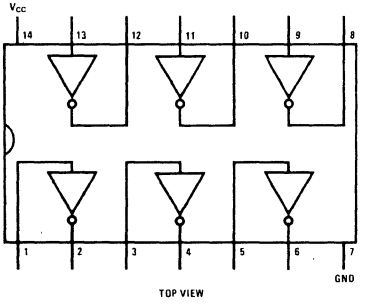
The DS78L12/DS88L12 is a low power TTL to MOS hex inverter element. The outputs may be "pulled up" to +14V in the logical "1" state, thus providing guaranteed interface between TTL and MOS logic levels. The gate may also be operated with V_{CC} levels up to +14V without resistive pull-ups at the outputs and still providing a guaranteed logical "1" level of V_{CC} − 2.2V with an output current of −200μA.

Schematic and Connection Diagrams



Note. Shown is schematic for each inverter

Dual-In-Line Package

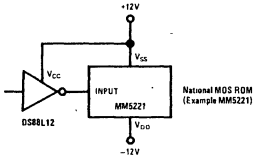


TOP VIEW

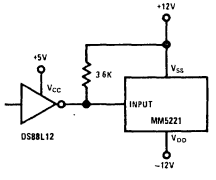
Order Number DS78L12J, DS88L12J
Order Number DS88L12N
Order Number DS78L12W
See NS Package J14A, N14A or W14A

Typical Applications

TTL Interface to MOS ROM Without Resistive Pull-Up



TTL Interface to MOS ROM With Resistive Pull-Up



AC Test Circuits

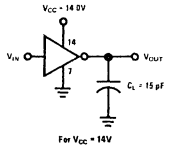


Figure 1

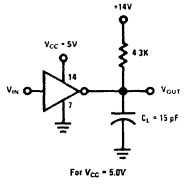
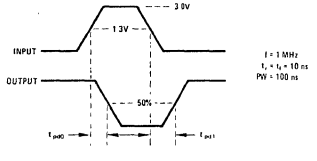


Figure 2

Switching Time Waveforms



Absolute Maximum Ratings (Note 1)

Supply Voltage	15V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 10 sec)	300°C

*Derate cavity package 8.72 mW/°C above 25°C; derate molded package 9.66 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS78L12	4.5	5.5	V
DS88L12	4.75	5.25	V
Temperature (T_A)			
DS78L12	−55	125	°C
DS88L12	0	70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = 14.0V		2.0	1.3		V
		V_{CC} = Min		2.0	1.3		V
V_{IL}	Logical "0" Input Voltage	V_{CC} = 14.0V			1.3	0.7	V
		V_{CC} = Min			1.3	0.7	V
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.7V	V_{CC} = 14.0V, I_{OUT} = −200μA	11.8	12.0		V
			V_{CC} = Min, I_{OUT} = 200μA	14.5	15.0		V
		V_{IN} = 0V, V_{CC} = Min, I_{OUT} = −5.0μA (Note 6)					V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 2.0V	V_{CC} = 14.0V, I_{OUT} = 12 mA		0.5	1.0	V
			V_{CC} = Min, I_{OUT} = 3.6 mA		0.2	0.4	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V	V_{CC} = 14.0V		<1	20	μA
			V_{CC} = Max		<1	10	μA
		V_{IN} = 5.5V	V_{CC} = 14.0V		<1	100	μA
			V_{CC} = Max		<1	100	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	V_{CC} = 14.0V		−320	−500	μA
			V_{CC} = Max		−100	−180	μA
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V (Note 4)	V_{CC} = 14.0V	−10	−25	−50	mA
			V_{CC} = Max	−3	−8	−15	mA
I_{CCH}	Supply Current — Logical "1" (Each Inverter)	V_{IN} = 0V	V_{CC} = 14.0V		0.32	0.50	mA
			V_{CC} = Max		0.11	0.16	mA
I_{CCL}	Supply Current — Logical "0" (Each Inverter)	V_{IN} = 5.25V	V_{CC} = 14.0V		1.0	1.5	mA
			V_{CC} = Max		0.3	0.5	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" from Input to Output	T_A = 25°C	V_{CC} = 5.0V *(Figure 2)*		27	45	ns
			V_{CC} = 14.0V *(Figure 1)*		11	20	ns
t_{pd1}	Propagation Delay to a Logical "1" from Input to Output	T_A = 25°C	V_{CC} = 5.0V *(Figure 2)*, (Note 5)		79	100	ns
			V_{CC} = 14.0V *(Figure 1)*		34	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78L12 and across the 0°C to +70°C range for the DS88L12.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: t_{pd1} for V_{CC} = 5.0V is dependent upon the resistance and capacitance used.

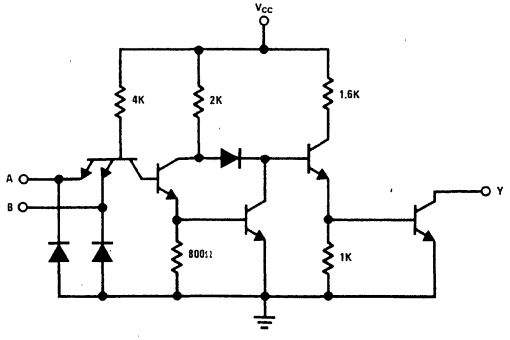
Note 6: $V_{OH} = V_{CC} - 1.1V$ for the DS88L12 and $V_{CC} - 1.4V$ for the DS78L12.

National Semiconductor

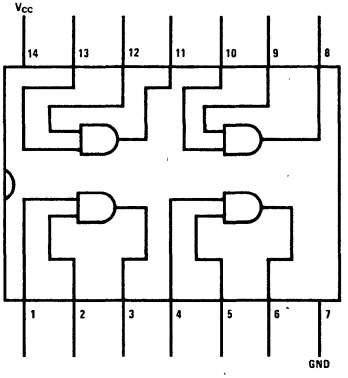
DS7819/DS8819 Quad 2-Input TTL-MOS AND Gate

The DS7819/DS8819 is the high output voltage version of the SN5409. Its open-collector outputs may be "pulled-up" to 14V in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS7819J or DS8819J
Order Number DS8819N
Order Number DS7819W
See NS Package J14A, N14A or W14A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1254 mW
Molded Package	1106 mW
Lead Temperature (Soldering, 10 sec)	300°C

*Derate cavity package 8.36 mW/°C above 25°C; derate molded package 8.85 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7819	4.5	5.5	V
DS8819	4.75	5.25	V
Temperature (T_A)			
DS7819	−55	+125	°C
DS8819	0	70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{OH}	Logical "1" Output Current	V_{CC} = Min	V_{IN} = 2.0V, V_{OUT} = 10V			40.0	μA
			V_{IN} = 4.5V, V_{OUT} = 14V			1.0	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 0.8V, I_{OUT} = 16 mA				0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40.0	μA
			V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.6	mA
I_{CCH}	Logical "1" Supply Current	V_{CC} = Max, V_{IN} = 5V			11.0	21.0	mA
I_{CCL}	Logical "0" Supply Current	V_{CC} = Max, V_{IN} = 0V			20.0	33.0	mA
V_{CL}	Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V

Switching Characteristics T_A = 25°C, V_{CC} = 5V

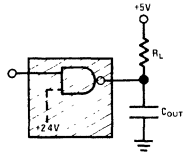
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	C_{OUT} = 15 pF, R_L = 400Ω		16.0	24.0	ns
t_{pd1}	Propagation Delay to a Logical "1"			16.0	32.0	ns

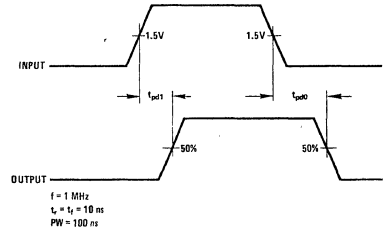
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7819 and across the 0°C to +70°C range for the DS8819.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms





Section 5
Display Controllers/ Drivers

5

*Also available screened in accordance with MIL-STD-883 Class B. Refer to National Semiconductor's "The Reliability Handbook".

DP8350 CRT CONTROLLER SERIES SELECTION GUIDE

Item No.	Parameter		DP8350 Value		DP8352 Value		DP8353 Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	(5)		(7)		(7)	
2		Scan Lines per Character (Height)	(7)		(9)		(9)	
3	Character Field Cell Size	Dots per Character (Width)	7		9		9	
4		Scan Lines per Character (Height)	10		12		12	
5	Number of Video Characters per Row		80		32		80	
6	Number of Video Character Rows per Frame		24		16		25	
7	Number of Video Scan Lines (Item 4 × Item 6)		240		192		300	
8	Frame Refresh Rate (Hz)		f1 = 60	f0 = 50	f1 = 60	f0 = 50	f1 = 60	f0 = 50
9	Delay after Vertical Blank Start to Start of Vertical Sync (Number of Scan Lines)		4	30	27	53	0	32
10	Vertical Sync Width (Number of Scan Lines)		10	10	3	3	3	3
11	Interval between Vertical Blank Start and Start of Video (Number of Scan Lines of Video Blanking)		20	72	68	120	20	84
12	Total Scan Lines per Frame (Item 7 + Item 11)		260	312	260	312	320	384
13	Horizontal Scan Frequency (Line Rate) (Item 8 × Item 12)		15.6 kHz		15.6 kHz		19.20 kHz	
14	Number of Character Times per Scan Line		100		50		102	
15	Character Clock Rate (Item 13 × Item 14)		1.56 MHz		0.78 MHz		1.9584 MHz	
16	Character Time (1 ÷ Item 15)		641 ns		1282 ns		510.6 ns	
17	Delay after Horizontal Blank Start to Horizontal Sync Start (Character Times)		0		6		5	
18	Horizontal Sync Width (Character Times)		43		4		9	
19	Dot Frequency (Item 3 × Item 15)		10.92 MHz		7.02 MHz		17.6256 MHz	
20	Dot Time (1 ÷ Item 19)		91.6 ns		142.4 ns		56.7 ns	
21	Vertical Blanking Output Stop before Start of Video (Number of Scan Lines)		1		0		1	
22	Cursor Enable on All Scan Lines of a Row? (Yes or No)		Yes		Yes		Yes	
23	Does the Horizontal Sync Pulse Have Serrations during Vertical Sync? (Yes or No)		No		Yes		No	
24	Width of Line Buffer Clock Logic "0" State within a Character Time (Number of Dot Time Increments)		4		5		5	
25	Serration Pulse Width, if Used (Character Times)		—		4		—	
26	Horizontal Sync Pulse Active State Logic Level (1 or 0)		1		0		1	
27	Vertical Sync Pulse Active State Logic Level (1 or 0)		0		0		1	
28	Vertical Blanking Pulse Active State Logic Level (1 or 0)		1		1		1	

Video Monitor Format: Ball Brothers TV-12, TV-120 or Equivalent. (DP8350)

Video Monitor Format: RS-170-Compatible (Standard American TV). (DP8352)

Video Monitor Format: Motorola M3003 or Equivalent. (DP8353)

LED DISPLAY SEGMENT DRIVERS

Drivers/ Package	I_O/Segment (mA)		V_{MAX} (V)		Comments	Device Number		Page No.
	Sink* (Common Anode)	Source (Common Cathode)	Input	Supply		0°C to +70°C	−55°C to +125°C	
4		30	10	10	Programmable constant current	DS75493	DS55493	5-109
4	50	50	15	10		DS75491		5-106
5	50	50	15	10		DS8861		5-136
6	32		5.5	7	Programmable output, active high latch	DS8859A		5-133
6	32		5.7	7	Programmable output, active low latch	DS8869A		5-133
8		18	10	7	Constant current output	DS8867		5-139
8		50	36	36		DS8654		5-113
14	25		6.6	7	BCD input, dual-display driver	DS8669		5-123

*Digit drivers with output sink capability may be used to drive segments of "common anode" displays

LED DISPLAY DIGIT DRIVERS

Drivers/ Package	I_O /Digit (mA)		V_{MAX} (V)		Comments	Device Number		Page No.
	Sink (Common Cathode)	Source (Common Anode)	Input	Supply		0°C to +70°C	−55°C to +125°C	
4		50	10	10		DS75491		5-106
6	50		10	10	DS75492 pinout, 4.5V to 9V systems	DS8877		5-147
6	150		10	10	Enable control	DS75494	DS55494	5-111
6	250		10	10		DS75492		5-106
6	350		10	10	DS75492 pinout, Darlington output	DS8870		5-141
8	40		11	11		DS8871		5-143
8	350		25	25	Open-collector saturating outputs	DS8692		5-126
8	500		15	10		DS8863		5-136
	500		23	18		DS8963		5-136
		50	36	36		DS8654		5-113
9	40		11	11		DS8872		5-143
	40		11	11	Low battery indicator	DS8873		5-143
	50		10	10	Serial shift register input	DS8874		5-145
	100		10	10	3-cell operation—low battery indicator	DS8973		5-166
	100		10	10	No low battery indicator	DS8975		5-166
10	400		9.5	45	Serial input	DS3654		3-29
14	80		10	10	On-board osc., 4 line code input, low battery indicator	DS8664		5-117
	80	13	10	10	6 sink, 8 source outputs	DS8666		5-120

GAS DISCHARGE DISPLAY DRIVERS

Device Type	Drivers/ Package	Comments	Device Number		Page No.
			0°C to +70°C	−55°C to +125°C	
Cathode drivers	7	BCD to 7-segment	DS8880	DS7880	5-149
	7	BCD to 7-segment with comma and DP	DS8884A		5-156
	7	MOS to high voltage cathode buffer	DS8885		5-158
	8	Active high inputs	DS8889	DS7889	5-160
Anode drivers	6	Active low inputs	DS8891A		5-164
	8	Active high inputs	DS8887		5-160
	8	Active low inputs	DS8897A	DS7897A	5-160

VACUUM FLUORESCENT DISPLAY DRIVERS

Device Type	Drivers/ Package	Comments	Device Number		Page No.
			0°C to +70°C	−55°C to +125°C	
Ground driver (segments)	8	7-segment plus DP	DS8654		5-113
Anode driver (digit)	8		DS8654		5-113
	16	4 line BCD input	DS8881		5-152

PRINTER DRIVERS

Device Type	Drivers/ Package	Description	Device Number		Page No.
			0°C to +70°C	−55°C to +125°C	
Mechanical printer		Relay driver	DS3680		3-44
		10 hammer serial input driver	DS3654		3-29
		Seiko model 310 print head, interface set	DS8692, DS8693, DS8694		5-126 5-126 5-126
Thermal printer		8-digit driver	DS8654		5-113
		Diode matrix	DS8656		5-113

National Semiconductor

Display Controllers/Drivers

DP8350 Series CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits. Three standard products are available, designated DP8350, DP8352, DP8353. Custom devices, however, are available in a broad range of mask programmable options.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock may be inputted to the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMs, or DM86S64-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, vertical blanking, horizontal sync, and vertical sync.

The DP8350 Series CRTC provides for a wide range of programmability using internal mask programmable ROMs:

- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame
- Format of Video Outputs

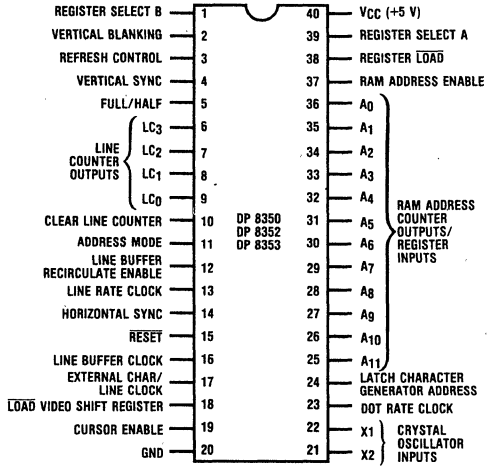
The CRTC also provides system sync and program inputs including Refresh Control, Reset, and Address Mode.

TRI-STATE is a registered trademark of National Semiconductor Corp.

Features

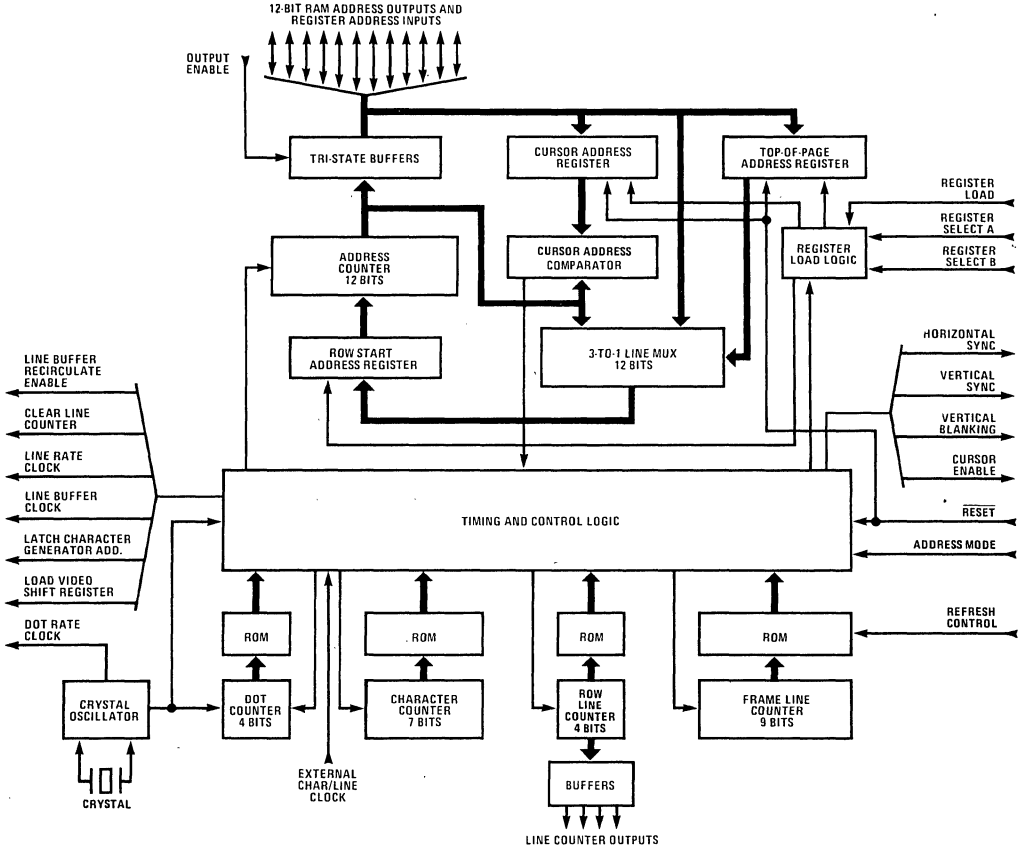
- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Internal top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 2 programmable refresh rates, pin selectable
- Programmable characters/row (128 max.)
- Progammable character field size (up to 16 dots x 16 scan line field size)
- Programmable scan lines/frame (512 max.)
- Programmable character rows/frame
- Single +5V power supply
- Inputs and outputs TTL compatible
- Direct interface with DM86S64 character generator
- Ease of system design/application

Connection Diagram



Order Number DP8350N, DP8352N or DP8353N
See NS Package N40A

Block Diagram



The Video Display

Discussion of the CRT Controller necessitates an understanding of the video display as presented by a raster scan monitor. The resolution of the data displayed on the monitor screen is a function of the dot size. As shown in Figure 1, the dot size is determined by the frequency of the system dot clock. The visible size of the dot can be modified to less than 100% by external gating of the serial video data. The CRT Controller organizes the dots into cell groupings that define video rows. These cells are accessed by a specific horizontal address output (4096 maximum) and are resolved by a row scan-line-counter output (16 maximum) as shown in Figure 2. The relation of the video portion of a frame to the horizontal blanking and vertical blanking intervals is shown in Figure 3 in a two-dimensional format.

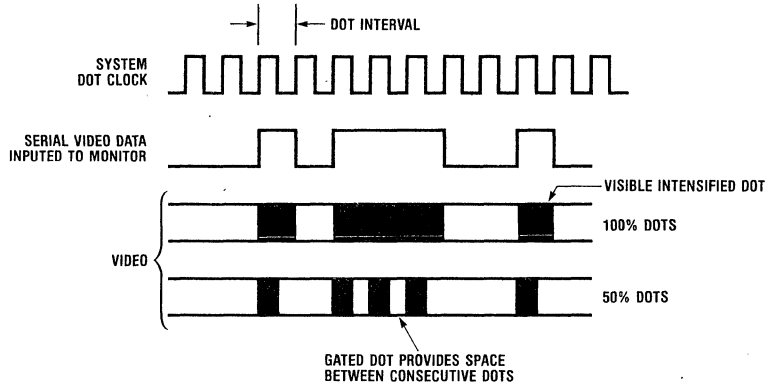


Figure 1. Dot Definition

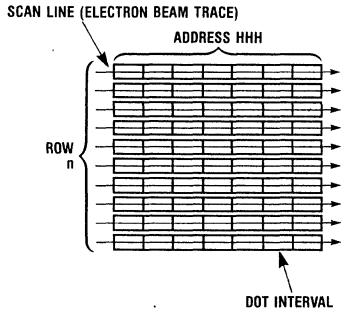


Figure 2. Character Cell Definition (Example Shown is a 7 x 10 Character Cell)

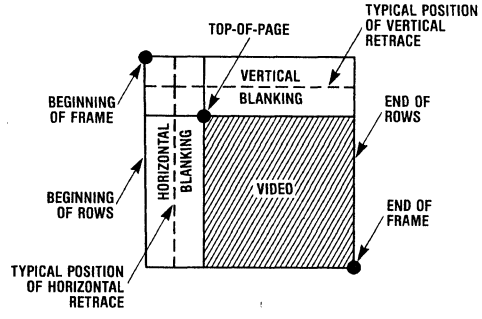


Figure 3. Frame Format Definition

Character Generation/Timing Outputs

The CRT controller provides 11 interface timing outputs for line buffers, character generator ROMs, DM86S64-type latch/ROM/shift register combination character generators, and system status timing. All outputs are buffered to provide TTL compatible direct interface to popular system circuits such as:

- DM86S64 Series Character Generators
- MM52116 Series Character ROMs
- DM74166 Dot Shift Register
- MM5034, MM5035 Octal 80-Bit Shift Registers (Line Buffers)

Dot Rate Clock: This output is provided for use in system synchronization and interface to the dot shift register used in character generation. This output is non-inverting with respect to an external clock applied to the X1 oscillator input (see Figure 6). The dot rate clock output exhibits a 50% duty cycle. All CRTC output logic transitions are synchronous with the rising edge of the Dot Rate Clock output.

Latch Character Generator Address (Character Rate Clock): This output provides an active clock pulse at character rate frequency which is active at all times. The rising edge of this pulse is synchronous with the beginning of each character cell. This output is intended for direct interface to character/video generation data latch registers.

Line Rate Clock: This output provides an active clock pulse at scan-line rate frequency (horizontal frequency), which is active at all times. The falling edge of this pulse is synchronous with the beginning of horizontal blanking. This output is intended for direct interface to character generation scan line counters.

Load Video Shift Register: This output provides a character rate signal intended for direct interface to the video dot shift register used in character generation. Active low pulses are outputted only during video time. As a result of the inactive time, horizontal and vertical video blanking can be derived from this output signal.

Clear Line Counter: This output signal is active only during the first scan line of all rows. It exhibits an active low pulse identical and synchronous to the Line Rate Clock and is provided for direct interface to character generation scan line counters.

Line Counter Outputs (LC_0 to LC_3): These outputs clock at line rate frequency, synchronous with the falling edge of the line rate clock, and provide a consecutive binary count for each scan line within a row. These outputs are provided for system designs that require decoded information indicating the present scan line position within a row. These outputs are always active, however, the next to the last row during vertical blanking will exhibit an invalid line count as a function of internal frame synchronization.

Line Buffer Clock: This output directly interfaces to data shift registers when they are incorporated as line buffers in a system design (see Figure 16). This signal is active at character rate frequency and is intended for shift registers that shift on a falling edge clock. This output is inactive during all horizontal blanking intervals yielding the number of active clocks per scan line equal to the number of video characters per row. For custom requirements, the duty cycle of this output is mask programmable.

Line Buffer Recirculate Enable: This output is provided to control the input loading mode of the data shift register (line buffer) when used in a system design. The format of this output is intended for shift registers that load external data into the input with the mode control in the low state, and load output data into the input (recirculate) with the mode control in the high state. This output will transition to the low state, synchronous with the line rate clock falling edge, for one complete scan line of each row. The position of this scan line will either be the first scan line of the addressed row, or the last scan line of the previous row depending upon the logic level of the address mode input (pin 11), tabulated in Table 3.

Memory Address Outputs/Inputs and Registers

Address Outputs (A_0-A_{11}): These 12 address bits (4k) are bi-directional TRI-STATE® outputs that directly interface to the system RAM memory address bus.

In the output mode (enabled), these outputs will exhibit a specific 12-bit address for each video character cell to be displayed on the CRT screen. This 12-bit address increments sequentially at character rate frequency and is valid at the address bus 2 character times prior to the addressed character appearing as video on the CRT screen. This pipelining by 2 characters is provided to allow sufficient time for first, accessing the RAM memory, and second, accessing the character generation memory with the RAM memory data. Since a character cell is comprised of several scan lines of the CRT beam, the sequential address output string for a given video row is identically repeated for each scan line within the row. The starting address for each video scan line is stored within an internal 12-bit register called the Row Start Register. At the beginning of each video scan line, the internal address counter logic is preset with the contents of the Row Start Register (see Figure 4). To accomplish row by row sequential addressing, internal logic updates the Row Start Register at the beginning of the first scan line of a video row with the last address + 1 of the last scan line of the previous video row. Since the number of address locations on the video screen display is typically much less than the 4k dimension of the 12-bit address bus, an internal 12-bit register called the Top Of Page Register, contains the starting address of the first video row. Internal logic loads the contents of this top of page register into the Row Start Register at the beginning of the first scan line of the first video row. The Top Of Page Register is loaded with address zero whenever the Reset input is pulsed to the logic "0" state.

In the input mode (disabled), external addresses can be loaded into the internal 12-bit registers by external control of the register select A, register select B, and register $\overline{\text{load}}$ inputs (see Table 1). As a result of specific external loading of the contents of the Row Start Register, Top Of Page Register, and the Cursor Register, row by row page scrolling, non-sequential row control, and cursor location control, can easily be accomplished.

During the non-video intervals, the address output operation is modified. During all horizontal blanking intervals, the incrementing of the address counter is inhibited and the address count is held constant at the last video address + 1. For example, if a video row has an 80 character cell format and addressing for the video portion of a given scan line starts at address 1, the address counter will increment up through address 81. Address 81 is held constant during the horizontal blanking interval until 3 character times before the next video scan line. At this point, the address counter is internally loaded with the contents of the Row Start Register which may contain address 1 or 81 as a function of internal control, or a new address that was loaded from the external bus. During vertical blanking, however, this loading of the internal address counter with the contents of the Row Start Register is inhibited providing scan line by scan line sequential address incrementing. This allows minimum access time to the CRTC when the address counter outputs are being used for dynamic RAM refresh.

RAM Address Enable Input: At all times the status of the bi-directional address outputs is controlled externally by the logic level of the enable input. A 'low' logic level at this input places the address outputs in the TRI-STATE® (disabled) input mode. A 'high' logic level at this input places the address outputs in the active (enabled) output mode.

Register $\overline{\text{Load}}$/Select Inputs: When the Register $\overline{\text{Load}}$ input is pulsed to the logic 'low' state, the Top Of Page, Row Start, or Cursor Register will be loaded with a 12-bit address which originates from either the internal address counter or the external address bus (refer to discussion on register loading constraints). The destination register is selected prior to the load pulse by setting the register select inputs to the appropriate state as defined in Table 1.

Table 1. Register Load Truth Table

Register Select A (Pin 39)	Register Select B (Pin 1)	Register Load Input (Pin 38)	Register Loading Destination
0	0	0	No Select
0	1	0	Top-of-Page
1	0	0	Row-Start*
1	1	0	Cursor
X	X	1	No Load

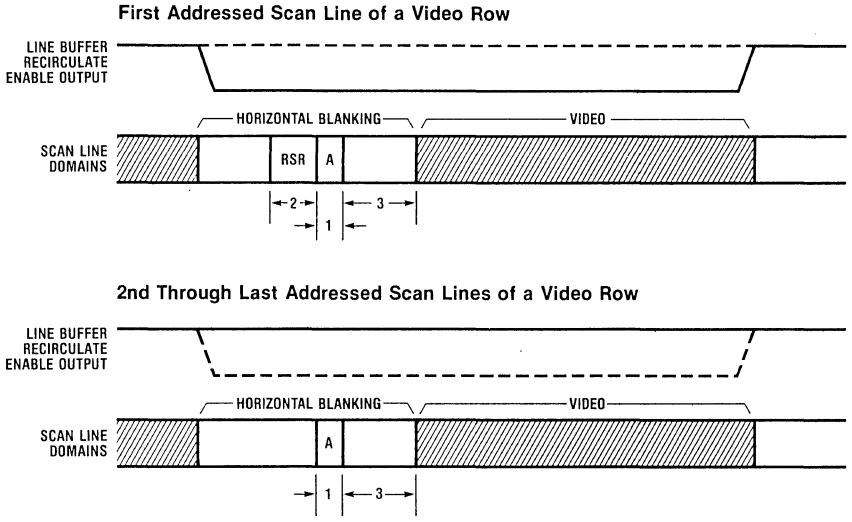
*During the vertical blanking interval, a load to this register is internally routed to the Top-Of-Page register.

Internal Registers and Loading Constraints: There are 3 internal 12-bit registers that facilitate video screen management with respect to row-by-row page scrolling, non-sequential row control and cursor location. These registers can be loaded with addresses from the external address bus while the address outputs are disabled (RAM address enable inut in the low state), by controlling the register select and load inputs within the constraints of each register.

The Row-Start Register (RSR) holds the starting address for each scan line of the video portion of a frame. The video addressing format is completely determined by the contents of this register. With no external loading, the RSR is automatically loaded by internal control such that row-by-row sequential addressing is achieved. Referring to Figure 4, the RSR is loaded automatically once for each video row during the first addressed scan line. The source of the loaded address is internally controlled such that the RSR load for the first video row comes from the Top-Of-Page Register. The RSR load for all subsequent video rows comes from the address counter which holds the last displayed address + 1. If non-sequential row formatting is desired, the RSR can be loaded externally with a 12-bit address. However, this external load must be made prior to the internal automatic load. Generally speaking, the external load to the RSR should be made during the video domain of the last addressed scan line of the previous row. Figure 4 indicates the internal automatic loading intervals which must be avoided, if the load must be made during the horizontal blanking interval. Once an external address has been loaded to the RSR, the next occurring internal automatic RSR load will be inhibited by internal detection logic. If an external load is made to the RSR during the vertical blanking interval, the 12-bit address is loaded into the Top-Of-Page Register instead of the RSR as a result of internal control. This internal function is performed due to the fact that the address loaded into the RSR for the first video row can only come from the Top-Of-Page Register.

The Top-Of-Page register (TOPR) holds the address of the first character of the first video row. As a function of internal control the contents of this register are loaded into the RSR at the beginning of the first addressed scan line of the first video row (see Figure 4). This loading operation is strictly a function of internal control and cannot be overridden by an external load to the RSR. For this reason, any external load to the RSR during the vertical blanking interval is interpreted internally as a TOPR load. When the Reset input is pulsed to the logic "0" state, the TOPR register is loaded with address zero by internal control. This yields a video page display with the first row of sequential addressing beginning at zero. Page scrolling can be accomplished by externally loading a new address into the TOPR. This loading operation can be performed at any time during the frame prior to the interval where the TOPR is loaded automatically into the RSR (see Figure 4). Once the TOPR has been loaded, it does not have to be accessed again until the contents are to be modified.

The Cursor Register (CR) holds the present address of the cursor location. A true comparison of the address counter outputs and the contents of the CR results in a Cursor Enable output signal delayed by two character times. When the $\overline{\text{Reset}}$ input is pulsed to the logic "0" state, the contents of the CR are set to address zero by internal control. Modifying the contents of the CR is accomplished by external loading at any time during this frame. Typically, loading is performed only during intervals when the address outputs are not actively controlling the video display. Once the CR has been loaded, it does not have to be accessed again until the contents are to be modified.



Note 1: Dimensions are in character time intervals.

Note 2: "A" denotes the interval that the address counter is preset with the contents of the Row Start Register.

Note 3: "RSR" denotes the interval that the Row Start Register is internally loaded with either the contents of the Top-Of-Page Register (1st video row) or the last video address + 1 from the address counter.

Figure 4. Automatic Internal Loading Intervals

Video-Related Outputs

Horizontal Sync: This output provides the necessary scan line rate sync signal for direct interface to either three-terminal or composite sync monitors. The pulse width, position, and logic polarity are mask programmable, in character time increments, for custom requirements. This output may also be mask programmed to have RS-170 compatible serration pulses during the vertical sync interval (refer to DP8352 format and Figure 15).

Vertical Sync: This output provides the necessary frame rate sync signal for direct interface to either three-terminal or composite sync monitors. The pulse width, position, and logic polarity are mask programmable, in scan line increments, for custom requirements.

Cursor Enable: This output provides a signal that is intended to be combined with the video signal to display a cursor attribute which serves as a visual pointer for video RAM location. Internally, the 12-bit address count is continuously being compared with the 12-bit address stored in the Cursor Register. When a true compare is detected, an active high level signal will be present at the Cursor Enable output, delayed by 2 character times after the corresponding address bus output. The signal is delayed by 2 character times so that it will be coincident with the video information resulting from the corresponding address. Mask programmability allows the cursor enable output signal to be formatted such that a signal will be outputted for all addressed scan lines of a video character cell or any single scan line of that cell. The cursor enable output signal is inhibited during the horizontal and vertical blanking intervals so that video blanking is maintained. When the addressing is advanced by setting the address mode input (pin 11) in the logic "0" state, the cursor enable signal will also be shifted with respect to the scan line count. Specifically, for a character cell with the cursor output active on all addressed scan lines of the cell, the first scan line of the cursor signal will occur at the last scan line count of the previous video row, and the last scan line count of the addressed character cell will have no cursor output signal. This mode of operation gives rise to a unique situation for the first video row where the first addressed scan line of a character cell has no cursor output signal since its advanced scan line position is inhibited by the vertical blanking interval.

CRT System Control Functions

Refresh Control Input: This input provides a logic level selectable CRT system refresh rate. Typically, this input will select either a 60 Hz or 50 Hz refresh rate to provide geographical marketing flexibility. However, mask programmability provides the capability of a wide range of frequencies for custom requirements. For definition of the input logic truth table and the refresh rate format, refer to Table 2 and the standard device type format tables.

Table 2. Refresh Rate Select Truth Table

Refresh Control (Pin 3) Logic Level	Frame Refresh Rate			
	Symbol	DP8350	DP8352	DP8353
1	f1	60 Hz	60 Hz	60 Hz
0	f0	50 Hz	50 Hz	50 Hz

Vertical Blanking Output: This output provides a signal that transitions at the end of the last video scan line of the last video row and indicates the beginning of the vertical blanking interval. This signal transitions back to the inactive state during the row of scan lines just prior to the first video row. The transition position within this last row of vertical blanking, as well as the active logic polarity, is a function of the particular device format (item 21 of the format tables) or is mask programmable for custom requirements.

Address Mode: When a system utilizes a line buffer shift register, the first scan line of addressing for a row is used to load the shift register. As a result of this loading operation, addressing for a particular row will not begin accessing the video RAM until the second scan line of addressing for the row. It also follows that the first scan line of a row can only exhibit addressed data for the previous video row that is in the shift register. This offset in addressing becomes a problem for character generation designs that output video on the first scan line of a row (with respect to the line counter outputs). The result is invalid data being displayed for the first scan line. One solution would be to utilize a character generation design that began outputting video on the second scan line of a row. However, since most single chip character generators begin video on the first scan line, the DP8350 series CRT controller provides a pin selectable advanced addressing mode which will compensate for addressing shifts resulting from shift register loading. Referring to Table 3, a high logic level at this input will cause addressing to be coincident with the scan line counter positions of a row, and a low logic level at this input will cause addressing to start on the last scan line counter position of the previous row. This shifted alignment of the addressing, with respect to the designated scan lines of a row, is diagrammed in Figure 5. Characteristically, it follows that, when addressing is advanced by one scan line, the Line Buffer Recirculate Enable output and the Cursor Enable output are also advanced by one scan line. This advanced position of the Cursor Enable output may deserve special consideration depending upon the system design.

Table 3. Address Mode Truth Table

Address Mode Input (Pin 11) (Logic Level)	New Row Addressing At Address Outputs and Line Buffer Recirculate Enable Logic Low Level (Scan Line Position)
0	Last scan line of previous row
1	First scan line of row

Full/Half Row Control: This control input is provided for applications that require the option of half-page addressing. As an example, if the normal video page format is 80 characters/row by 24 rows, setting this input to the logic "0" state will cause the video format to become evenly spaced at 80 characters/row by 12 rows. Specifically, when this input is in the logic "0" state, row addressing is repeated for every other row. This yields successive groups of two rows of identical addressing. The second row of addressing, however, has the Load Video Shift Register output and the Cursor Enable output internally inhibited to provide the necessary video blanking. Setting this input to the logic "1" state yields normal frame addressing.

External Character/Line Rate Clock: This input is intended to aid testing of the CRTC and is not meant to be used as an active input in a CRT system. When this input is left open, it is guaranteed not to interfere with normal operation.

$\overline{\text{Reset}}$ Input: This input is provided for power-up synchronization. When brought to the logic "0" state, device operation is halted. Internal logic is set at the beginning of vertical blanking, and the Top-Of-Page Register and the Cursor Register are loaded with address zero. When this input returns to the logic "1" state, device operation resumes at the vertical blanking interval followed by video addressing which begins at zero. This input has hysteresis and may be connected through a resistor to V_{CC} and through a capacitor to ground to accomplish a power-up Reset. The logic "0" state should be maintained for a minimum of 250 ns.

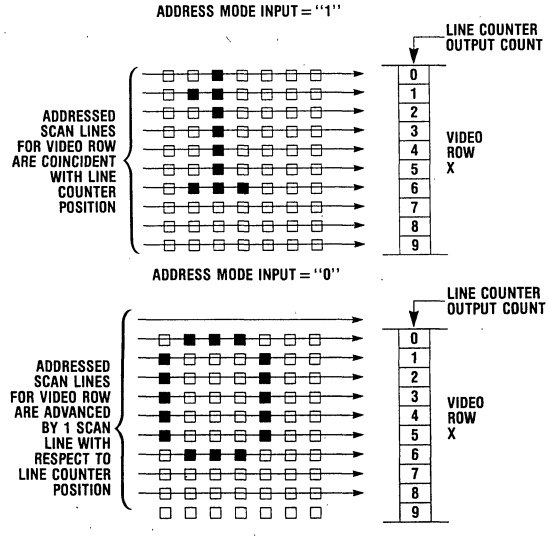


Figure 5. Address Mode Functionality

Crystal Inputs X1 and X2: The "Pierce"-type oscillator is controlled by an external crystal providing parallel resonant operation. Connection of external bias components is made to pin 22 (X1) and pin 21 (X2) as shown in Figure 6. It is important that the crystal be mounted in close proximity to the X1 and X2 pins to ensure that printed circuit trace lengths are kept to an absolute minimum. Typical specifications for the crystal are shown in Table 4 for each of the standard products, DP8350, DP8352, and DP8353. When customer mask options require higher frequencies, it may be necessary to change the crystal specifications and biasing components. If the CRTC is to be clocked by an external system dot clock, pin 22 (X1) should be driven directly by Schottky family logic while pin 21 (X2) is left open. The typical threshold for pin 22 (X1) is $V_{CC}/2$.

Table 4. Typical Crystal Specifications

Parameter	Specification		
	DP8350	DP8352	DP8353
Type	At-Cut		
Frequency	10.92 MHz	7.02 MHz	17.6256 MHz
Tolerance	0.005% at 25°C		
Stability	0.01% from 0°C to +70°C		
Resonance	Fundamental, Parallel		
Maximum Series Resistance	50Ω		
Load Capacitance	20 pF		

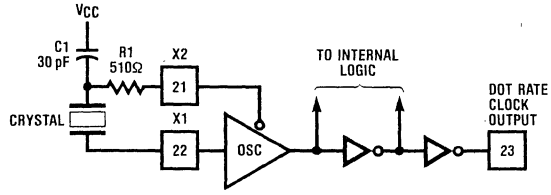


Figure 6. Dot Clock Oscillator Configuration with Typical External Bias Circuitry Shown

Custom Order Mask Programmability: The DP8350 Series CRT controller is available in three standard options designated DP8350, DP8352, and DP8353. The functional format of these devices was selected to meet the typical needs of CRT terminal designs. In order to accommodate specific customer formats, the DP8350 series CRT controller is mask programmable with a diverse range of options available. The items listed in the program table worksheet indicate the available options, while Table 5 tabulates the programming constraints.

Table 5. Mask Programming Limitations

Designation	Parameter	Min. Value	Max. Value
f_{DOT}	Dot Rate Frequency	DC	30 MHz
f_{CHAR}	Character Rate Frequency	DC	2.5 MHz
—	Line Buffer Clock Logic "0" Width (Item 20 × Item 24)	200 ns	
Item 3	Dots per Character Field Width	4	16
Item 4	Scan Lines per Character Field	2	16
Item 12	Scan Lines per Frame		512
Item 14	Character Times per Row — Video	5	122
	Character Times per Row — Blanking	6	123
Item 11	Scan Lines per Vertical Blanking	(Item 4) + 2	
If the cursor enable output, Item 22, is active on only one line of a character row, then Item 21 value must be either "1" or "0" or equivalent to the line selected for the cursor enable output.			

DP8350 Series Custom Order Format Table

This table is provided as a worksheet to aid in determining the programmed configuration for custom mask options. Refer to Table 5 for a list of programming limitations.

Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)		
2		Scan Lines per Character (Height)		
3	Character Field Block Size	Dots per Character (Width)		
4		Scan Line per Character (Height)		
5	Number of Video Characters per Row			
6	Number of Video Character Rows per Frame			
7	Number of Video Scan Lines (Item 4 × Item 6)			
8	Frame Refresh Rate (Hz) (two pin selectable frequencies allowed) (Item 13 ÷ Item 12)		f1=	f0=
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)			
10	Vertical Sync Width (Number of Scan Lines)			
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)			
12	Total Scan Lines per Frame (Item 7 + Item 11)			
13	Horizontal Scan Frequency (Line Rate) (kHz) (Item 8 × Item 12)			
14	Number of Character Times per Scan Line			
15	Character Clock Rate (MHz) (Item 13 × Item 14)			
16	Character Time (ns) (1 ÷ Item 15)			
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)			
18	Horizontal Sync Width (Character Times)			
19	Dot Frequency (MHz) (Item 3 × Item 15)			
20	Dot Time (ns) (1 ÷ Item 19)			
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines) (Range = Item 4 − 1 line to 0 lines)			
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?			
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)			
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments) (Typically ½ Item 3 rounded up)			
25	Serration Pulse Width, if used (Character Times) (See Figure 13)			
26	Horizontal Sync Pulse Active state logic level (1 or 0)			
27	Vertical Sync Pulse Active state logic level (1 or 0)			
28	Vertical Blanking Pulse Active state logic level (1 or 0)			

Video Monitor: Manufacturer and Model No. (For Engineering Reference)

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Operating Conditions (Note 6)

	Min.	Max.	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	+70	°C

Electrical Characteristics $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to +70°C (Notes 2, 3, and 5)

	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Logic "1" Input Voltage All Inputs Except X1, X2 $\overline{RESET}$ $\overline{RESET}$		2.0 2.6			V V
V_{IL}	Logic "0" Input Voltage All Inputs Except X1, X2				0.8	V
V_{HYS}	$\overline{RESET}$ Input Hysteresis			0.4		V
V_{clamp}	Input Clamp Voltage All Inputs Except X1, X2	$I_{IN} = -12$ mA		−0.8	−1.2	V
I_{IH}	Logic "1" Input Current A_0-A_{11}	Enable Input = 0V, $V_{CC} = 5.25V$, $V_{IN} = 5.25V$		10	100	μA
	All Other Inputs Except X1, X2	$V_{CC} = 5.25V$, $V_{IN} = 5.25V$		2.0	20	μA
I_{IL}	Logic "0" Input Current A_0-A_{11}	Enable Input = 0V, $V_{CC} = 5.25V$, $V_{IN} = 0.5V$		−20	−100	μA
	All Other Inputs Except X1, X2	$V_{CC} = 5.25V$, $V_{IN} = 0.5V$		−20	−100	μA
V_{OH}	Logic "1" Output Voltage	$I_{OH} = -100\,\mu A$	3.2	4.1		V
		$I_{OH} = -1$ mA	2.5	3.3		V
V_{OL}	Logic "0" Output Voltage	$I_{OL} = 5$ mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	$V_{CC} = 5V$, $V_{OUT} = 0V$ (Note 4)	10	40	100	mA
I_{CC}	Power Supply Current (Note 10)	$V_{CC} = 5.25V$		220	300	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min./max. limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$ and are intended for reference only.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max. or min. are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Electrical specifications do not apply to pin 17, external char/line clock, as this pin is used for production testing only.

Note 6: Functional operation of device is not guaranteed when operated beyond specified operating condition limits.

Switching Characteristics $V_{CC} = 5.0V \pm 5\%$, $T_A = 25°C$ (Note 7)

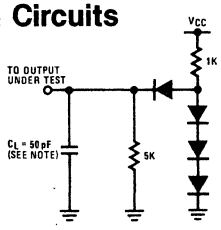
	Parameter	Load Circuit	Notes	Min.	Typ.	Max.	Units
Symmetry	Dot Rate Clock Output High Symmetry With Crystal Control	1		50% − 4	50% − 2	50% + 1	ns
t_{pd1}	XI Input to Dot Rate Clock Output Positive Edge	1			17	22	ns
t_{pd0}	XI Input to Dot Rate Clock Output Negative Edge	1			21	26	ns
t_{D1}	Dot Clock to Load Video Shift Register Negative Edge	1			6.0	10	ns
t_{D2}	Dot Clock to Load Video Shift Register Positive Edge	1			11	15	ns
t_{D3}	Dot Clock to Latch Character Generator Positive Edge	1			8.0	13	ns
t_{D4}	Dot Clock to Latch Character Generator Negative Edge	1			6.0	10	ns

Switching Characteristics (Cont'd.) $V_{CC} = 5.0V \pm 5\%$, $T_A = 25°C$ (Note 7)

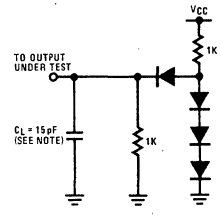
	Parameter	Load Circuit	Notes	Min.	Typ.	Max.	Units
$t_{D2}-t_{D3}$	Latch Character Generator Positive Edge to Load Video Shift Register Positive Edge	1		0	3.0		ns
t_{D5}	Dot Clock to Line Buffer Clock Negative Edge	1			23	35	ns
t_{PW1}	Line Buffer Clock Pulse Width	1	8,9	N(DT)	N(DT)+8	N(DT)+12	ns
t_{D6}	Dot Clock to Cursor Enable Output Transition	1			24	36	ns
t_{D7}	Dot Clock to Valid Address Output	1			15	25	ns
t_{D8_0}	Latch Character Generator to Line Rate Clock Neg. Transition	1	8,10		425 + DT	500 + DT	ns
t_{D8_1}	Latch Character Generator to Line Rate Clock Pos. Transition	1	8,10		300 + DT	400 + DT	ns
t_{D9_0}	Latch Character Generator to Clear Line Counter Neg. Transition	1	8,10		525 + DT	700 + DT	ns
t_{D9_1}	Latch Character Generator to Clear Line Counter Pos. Transition	1	8,10		290 + DT	400 + DT	ns
$t_{D8_1}-t_{D9_1}$	Clear Line Counter Pos. Transition to Line Rate Clock Pos. Transition	1	10		10	60	ns
t_{D10}	Line Rate Clock to Line Counter Output Transition	1			60	120	ns
t_{D11}	Line Rate Clock to Line Buffer Recirculate Enable Transition	1			195	300	ns
t_{D12}	Line Rate Clock to Vertical Blanking Transition	1			160	300	ns
t_{D13}	Line Rate Clock to Vertical Sync Transition	1			220	300	ns
t_{D14}	Latch Character Generator to Horizontal Sync Transition	1			96	150	ns
t_{S1}	Register Select Set-up Before Register Load Negative Edge			0			ns
t_{H1}	Register Select Hold After Register Load Positive Edge			0			ns
t_{S2}	Valid Address Input Set-Up Before Register Load Positive Edge			250			ns
t_{H2}	Valid Address Hold Time After Register Load Positive Edge			0			ns
t_{PW2}	Register Load Required Pulse Width			150	65		ns
t_{LZ}, t_{HZ}	Delay from Enable Input to Address Output High Impedance State from Logic "0" and Logic "1"	2			15	30	ns
t_{ZL}, t_{ZH}	Delay from Enable Input to Logic "0" and Logic "1" from Address Output High Impedance State	2			17	30	ns

Note 7: Typical values are for $V_{CC} = 5.0V$ and $T_A = 25°C$ and are meant for reference only.
Note 8: "DT" denotes dot rate clock period time, item 20 from option format table.
Note 9: "N" denotes value of item 24 from option format table.
Note 10: Revised since last issue.

Switching Load Circuits



Load Circuit 1



Load Circuit 2

Note: C_L includes probe and jig capacitance. All diodes are 1N914 or equivalent.

Switching Waveforms

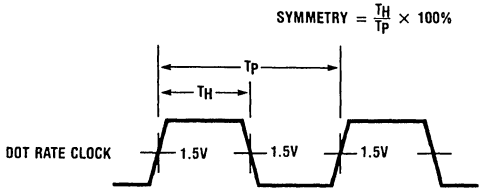


Figure 7. Dot Rate Clock Output Waveform Symmetry with Crystal Control

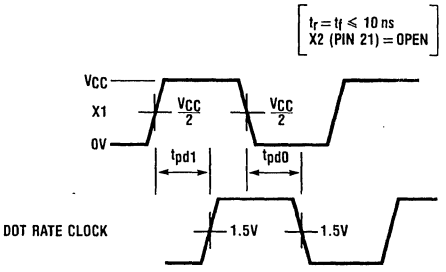
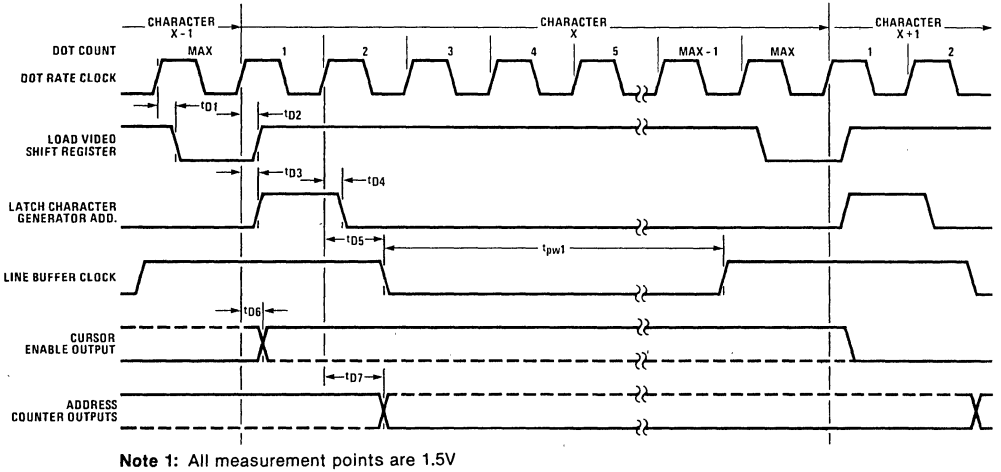
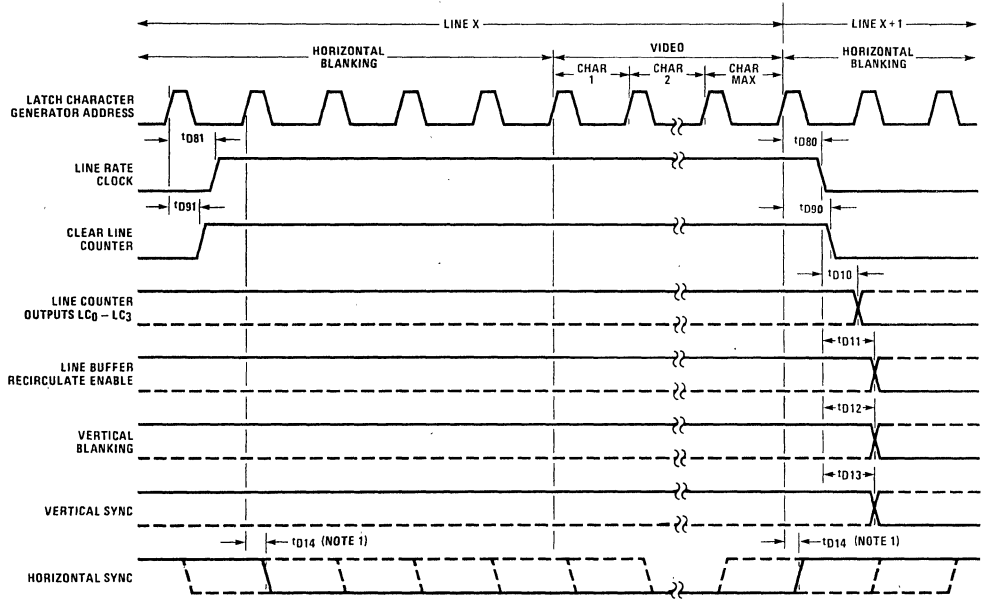


Figure 8. X1 Input to Dot Rate Clock Output Propagation Delay



Note 1: All measurement points are 1.5V

Figure 9. Dot/Character Rate Timing

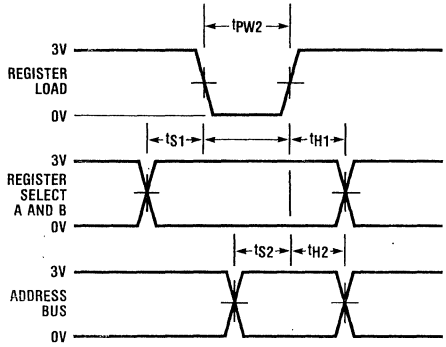


Note 1: Actual polarity and position of the horizontal sync start and stop points is a function of the particular device format.

Note 2: All measurement points are 1.5V.

Figure 10. Character/Line Rate Timing

Switching Waveforms (cont'd)



Note 1: All measurement points are 1.5V.

Note 2: $t_r = t_f \leq 10$ns.

Note 3: Address enable (pin 37) = 0V.

Figure 11. Register Select and Load Waveforms

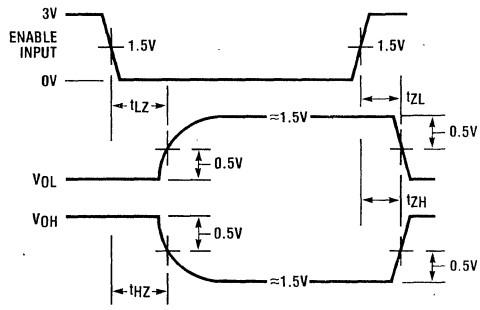
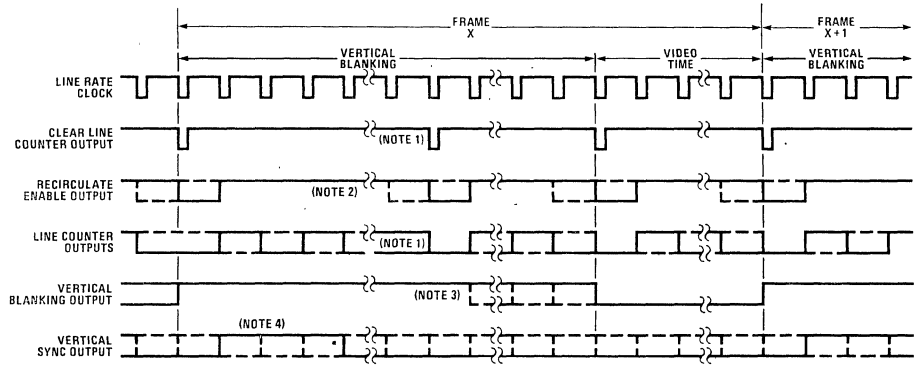


Figure 12. Address Output Enable/Disable Waveforms

Timing Diagrams



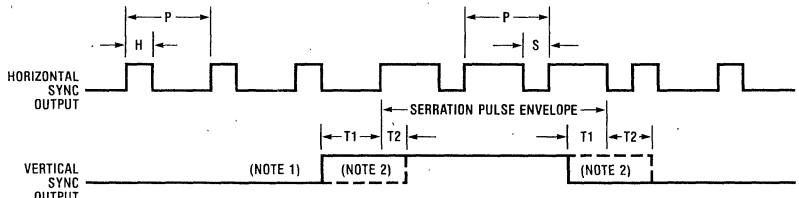
Note 1: One full row before start of video the line counter is set to zero state — this provides line counter synchronization in cases where the number of lines in vertical blanking are not even multiples of the number of lines per row.

Note 2: The position of the line buffer recirculate enable logic low level is a function of the logic level of the address mode input (see Table 3).

Note 3: The stop point of the vertical blanking output active signal is a function of device type or custom option, and will always be within one row prior to video.

Note 4: The transition start and stop points of the vertical sync output signal are a function of device type or custom option.

Figure 14. Line/Frame Rate Functional Diagram



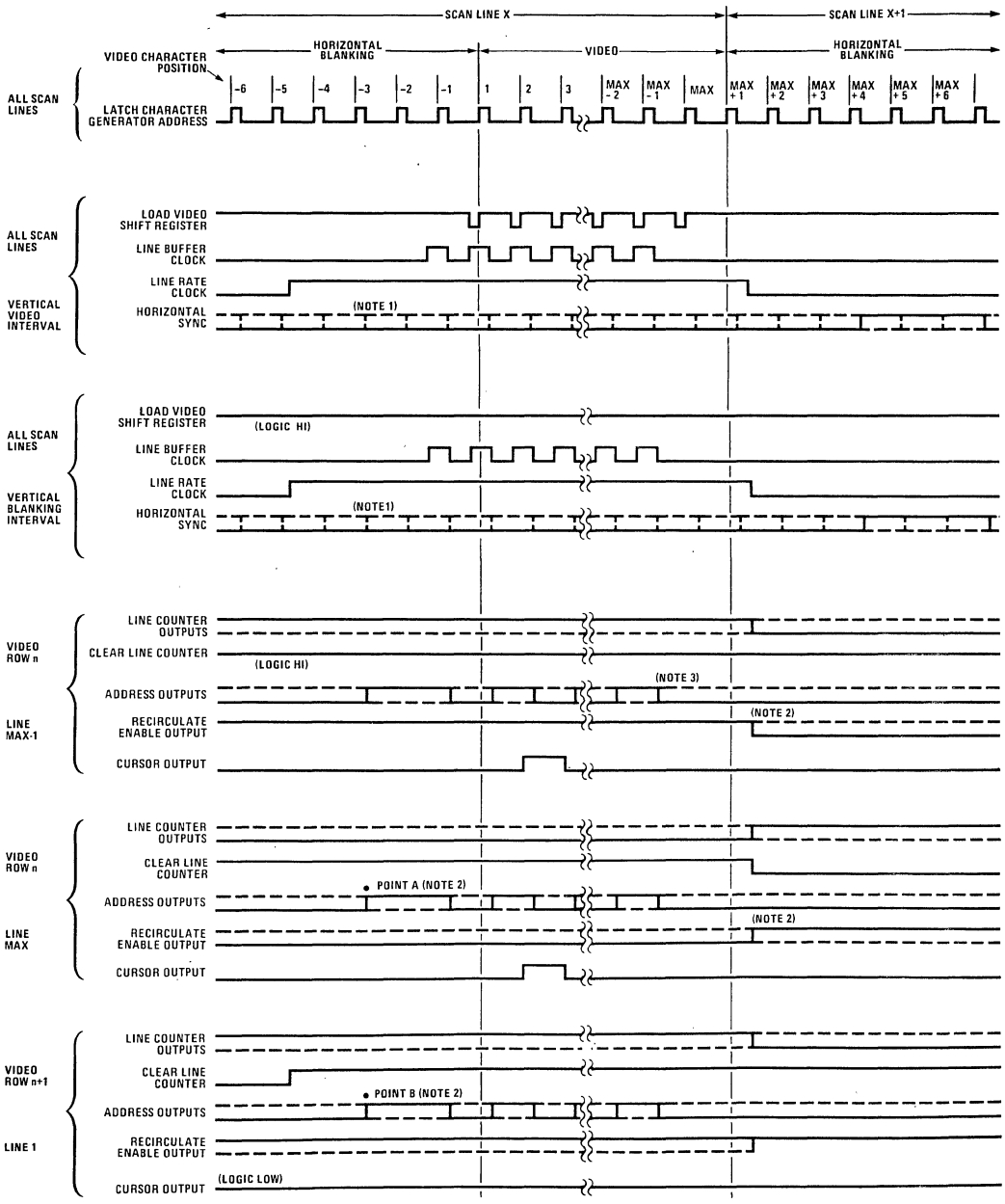
P = HORIZONTAL SCAN TIME PERIOD (ITEM 14 FROM PROGRAM TABLE)
H = HORIZONTAL SYNC WIDTH (ITEM 18 FROM PROGRAM TABLE)
S = SERRATION PULSE WIDTH (ITEM 25 FROM PROGRAM TABLE)
T1 = P-H (MAX)
T2 = H-1 CHARACTER TIME (MAX)

Note 1: The vertical sync transition point is always coincident with the beginning of horizontal blanking.

Note 2: T1 and T2 intervals represent the range of alignment offset between the vertical sync pulse and the serration pulse envelope and is a function of the horizontal sync position with respect to the beginning of horizontal blanking.

Figure 15. Serration Pulse Format

Timing Diagrams (cont'd)



Note 1: The horizontal sync output start and stop point positions are a function of device type or custom option.

Note 2: The position of the recirculate enable output logic "0" level is dependent on the state of the address mode input. When address mode = "0", recirculate enable occurs on the max. line of a character row (solid line) and the address counter outputs roll over to the new row address at point A. When address mode = "1", recirculate enable occurs on the first line of a character row (dashed line) and the address counter outputs roll over to the new row address at point B.

Note 3: The address counter outputs clock to the address of the last character of a video row plus 1. This address is then held during the horizontal blanking interval until video minus three character times. At this point the outputs are modified to the contents of the Row Start Register (RSR).

Figure 13. Character/Line Rate Functional Diagram

Applications

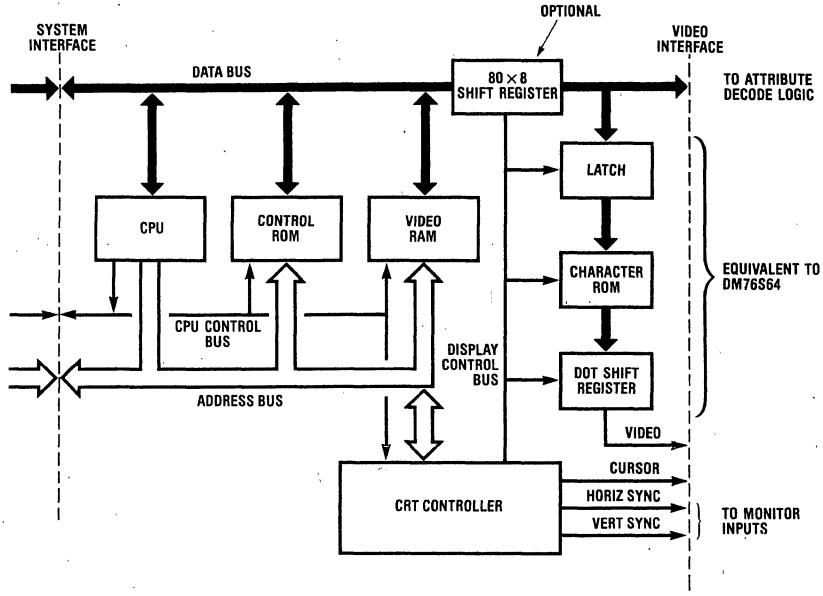


Figure 16. General System Block Diagram

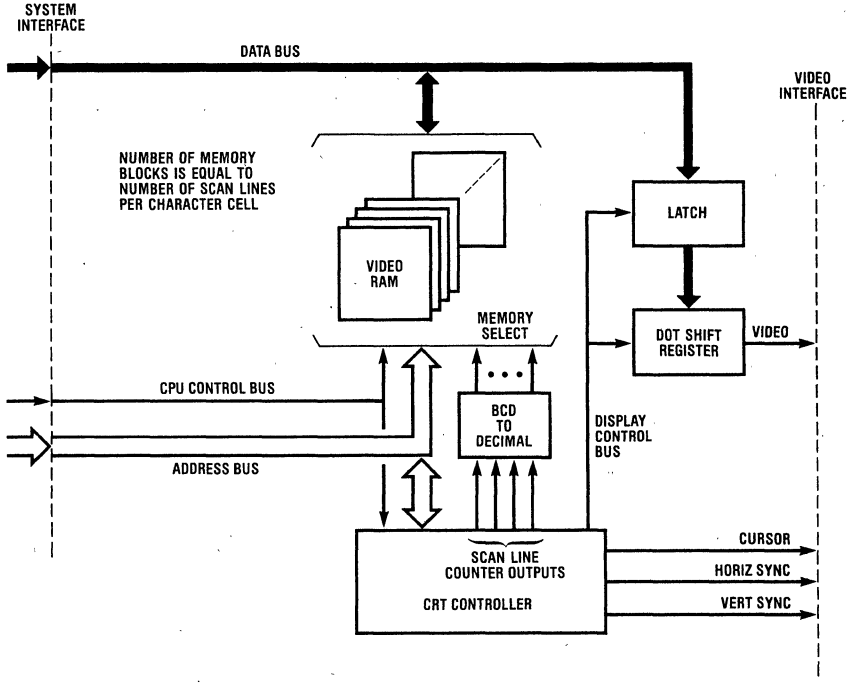


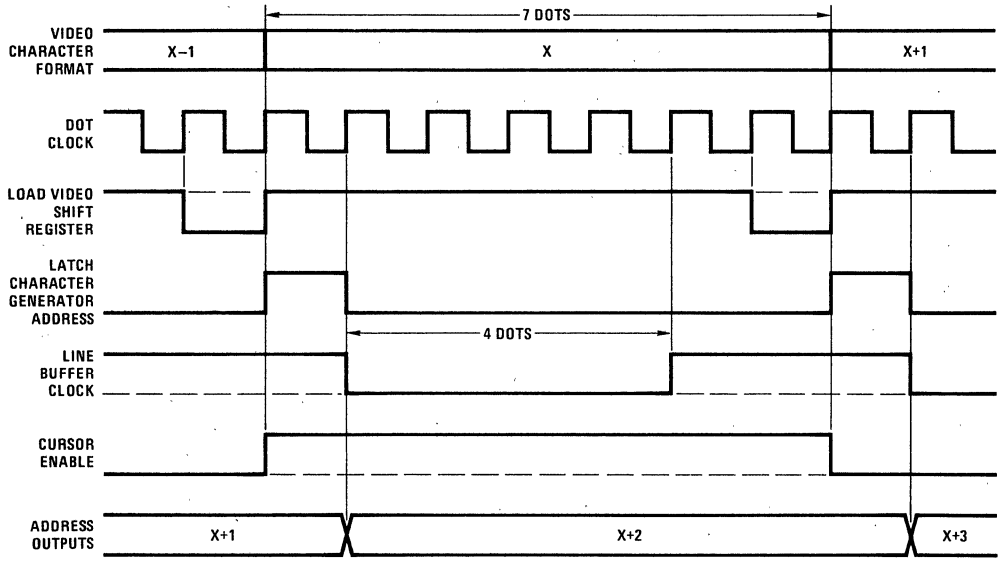
Figure 17. Dot-By-Dot Graphics Block Diagram

DP8350 CRT Controller

Table 6. Characteristic Format

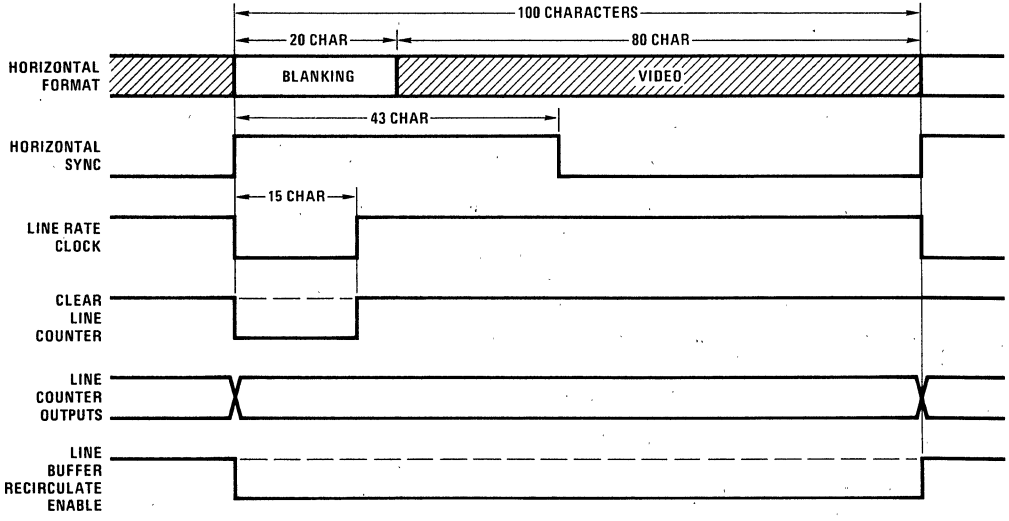
Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	(5)	
2		Scan Lines per Character (Height)	(7)	
3	Character Field Cell Size	Dots per Character (Width)	7	
4		Scan Line per Character (Height)	10	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		24	
7	Number of Video Scan Lines (Item 4 × Item 6)		240	
8	Frame Refresh Rate (Hz)		f1 = 60	f0 = 50
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)		4	30
10	Vertical Sync Width (Number of Scan Lines)		10	10
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)		20	72
12	Total Scan Lines per Frame (Item 7 + Item 11)		260	312
13	Horizontal Scan Frequency (Line Rate) (Item 8 × Item 12)		15.6 kHz	
14	Number of Character Times per Scan Line		100	
15	Character Clock Rate (Item 13 × Item 14)		1.56 MHz	
16	Character Time (1 ÷ Item 15)		641 ns	
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)		0	
18	Horizontal Sync Width (Character Times)		43	
19	Dot Frequency (Item 3 × Item 15)		10.92 MHz	
20	Dot Time (1 ÷ Item 19)		91.6 ns	
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines)		1	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No)		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		4	
25	Serration Pulse Width, if used (Character Times)		—	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

Video Monitor Format: Ball Brothers TV-12, TV-120 or Equivalent.



NOTE: DASHED LINES IN WAVEFORMS DENOTE INACTIVE STATE LOGIC LEVELS.

Figure 18. DP8350 Video Character Signals



NOTE: DASHED LINES IN WAVEFORMS DENOTE INACTIVE STATE LOGIC LEVELS.

Figure 19. DP8350 Scan Line Signals

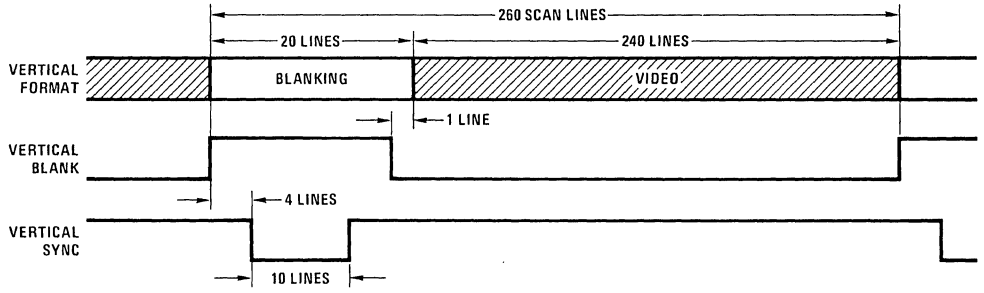


Figure 20. DP8350 60 Hz Refresh Rate Frame Signals

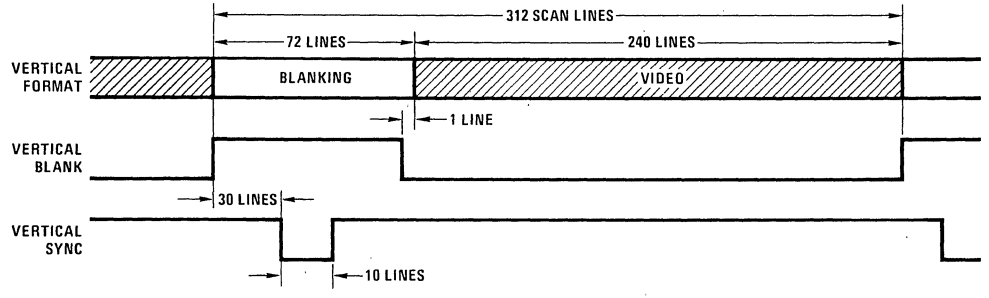


Figure 21. DP8350 50 Hz Refresh Rate Frame Signals

DP8352 CRT Controller

Table 7. Characteristic Format

Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	(7)	
2		Scan Lines per Character (Height)	(9)	
3	Character Field Cell Size	Dots per Character (Width)	9	
4		Scan Line per Character (Height)	12	
5	Number of Video Characters per Row		32	
6	Number of Video Character Rows per Frame		16	
7	Number of Video Scan Lines (Item 4 × Item 6)		192	
8	Frame Refresh Rate (Hz)		f1 = 60	f0 = 50
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)		27	53
10	Vertical Sync Width (Number of Scan Lines)		3	3
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)		68	120
12	Total Scan Lines per Frame (Item 7 + Item 11)		260	312
13	Horizontal Scan Frequency (Line Rate) (Item 8 × Item 12)		15.6 kHz	
14	Number of Character Times per Scan Line		50	
15	Character Clock Rate (Item 13 × Item 14)		0.78 MHz	
16	Character Time (1 ÷ Item 15)		1282 ns	
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)		6	
18	Horizontal Sync Width (Character Times)		4	
19	Dot Frequency (Item 3 × Item 15)		7.02 MHz	
20	Dot Time (1 ÷ Item 19)		142.4 ns	
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines)		0	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No)		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		Yes	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		5	
25	Serration Pulse Width, if used (Character Times)		4	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		0	
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

Video Monitor Format: RS-170-Compatible (Standard American TV).

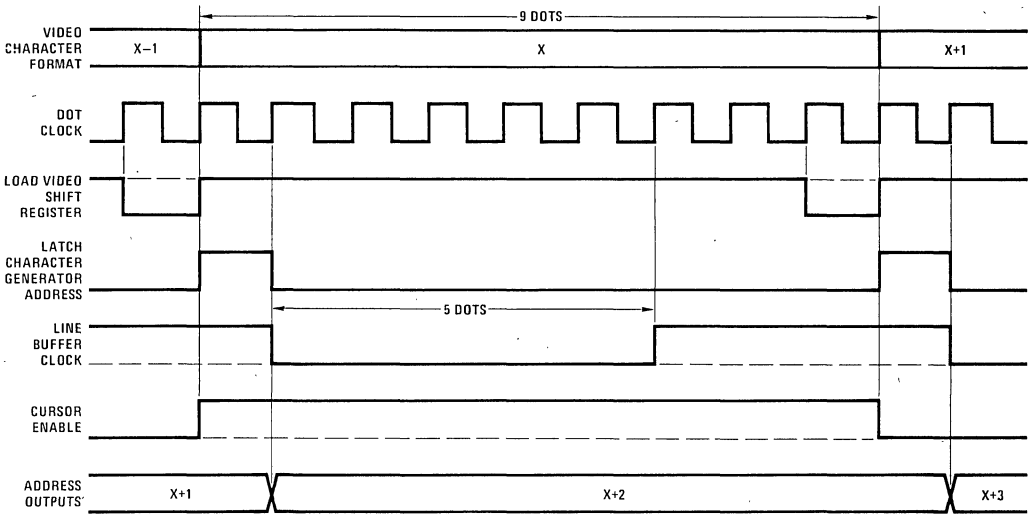


Figure 22. DP8352 Video Character Signals

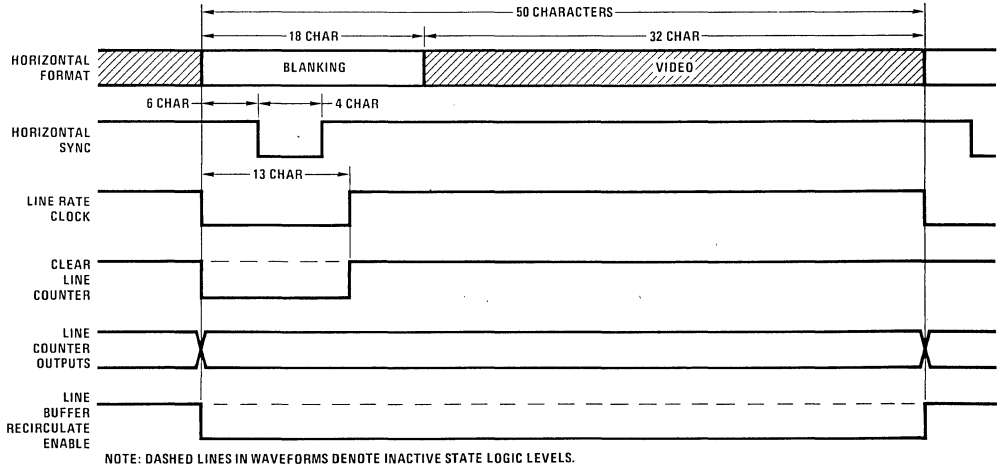


Figure 23. DP8352 Scan Line Signals

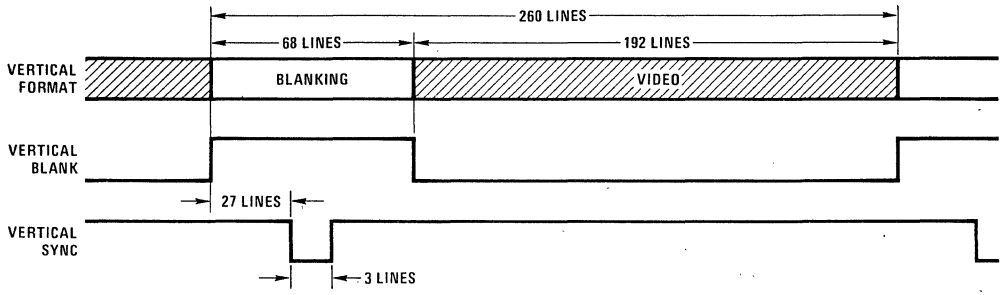


Figure 24. DP8352 60 Hz Refresh Rate Frame Signals

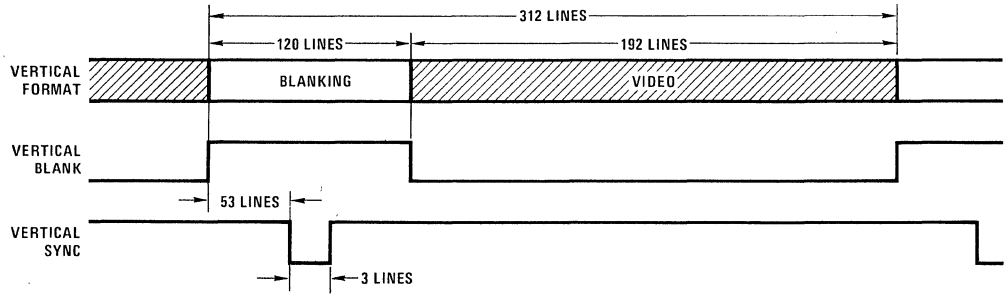


Figure 25. DP8352 50 Hz Refresh Rate Frame Signals

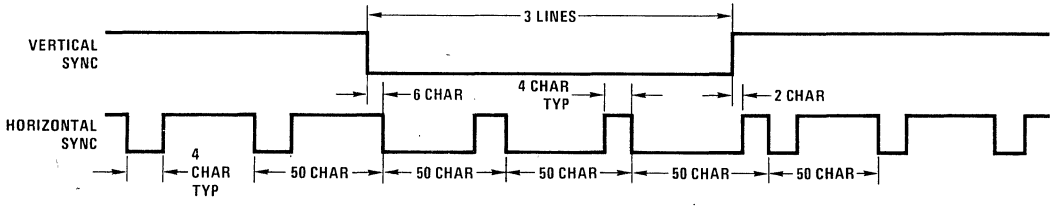
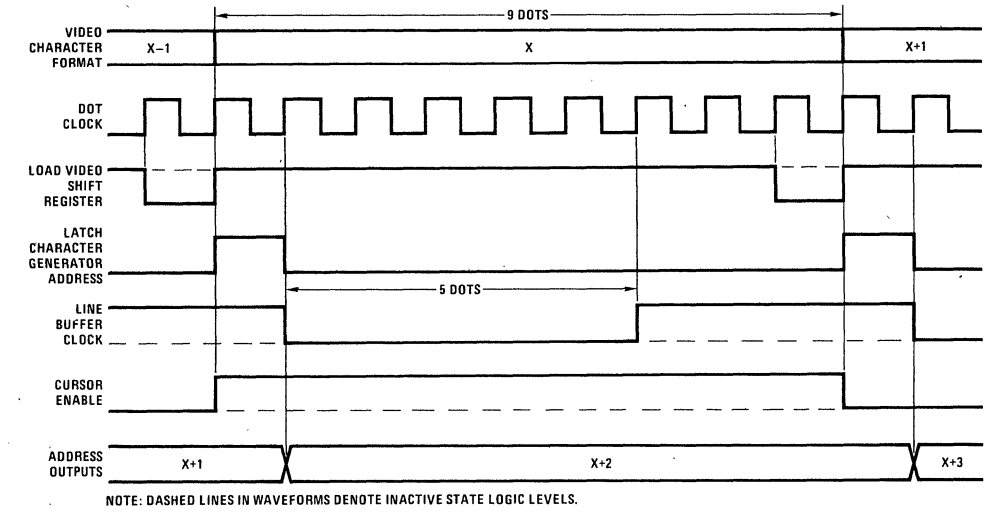


Figure 26. DP8352 Serration Pulse Format

Table 8. Characteristic Format

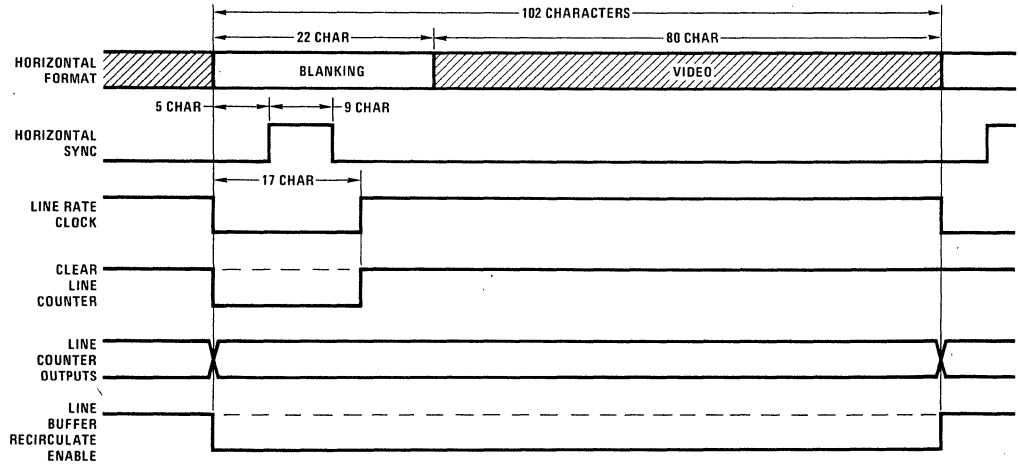
Item No.	Parameter		Value	
1	Character Font Size (Reference Only)	Dots per Character (Width)	(7)	
2		Scan Lines per Character (Height)	(9)	
3	Character Field Cell Size	Dots per Character (Width)	9	
4		Scan Line per Character (Height)	12	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		25	
7	Number of Video Scan Lines (Item 4 × Item 6)		300	
8	Frame Refresh Rate (Hz)		f1 = 60	f0 = 50
9	Delay after Vertical Blank start to start of Vertical Sync (Number of Scan Lines)		0	32
10	Vertical Sync Width (Number of Scan Lines)		3	3
11	Interval between Vertical Blank start and start of Video (Number of Scan Lines of Video Blanking)		20	84
12	Total Scan Lines per Frame (Item 7 + Item 11)		320	384
13	Horizontal Scan Frequency (Line Rate) (Item 8 × Item 12)		19.20 kHz	
14	Number of Character Times per Scan Line		102	
15	Character Clock Rate (Item 13 × Item 14)		1.9584 MHz	
16	Character Time (1 ÷ Item 15)		510.6 ns	
17	Delay after Horizontal Blank start to Horizontal Sync start (Character Times)		5	
18	Horizontal Sync Width (Character Times)		9	
19	Dot Frequency (Item 3 × Item 15)		17.6256 MHz	
20	Dot Time (1 ÷ Item 19)		56.7 ns	
21	Vertical Blanking Output Stop before start of Video (Number of Scan Lines)		1	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No)		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		5	
25	Serration Pulse Width, if used (Character Times)		—	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		1	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

Video Monitor Format: Motorola M3003 or Equivalent.



NOTE: DASHED LINES IN WAVEFORMS DENOTE INACTIVE STATE LOGIC LEVELS.

Figure 27. DP8353 Video Character Signals



NOTE: DASHED LINES IN WAVEFORMS DENOTE INACTIVE STATE LOGIC LEVELS.

Figure 28. DP8353 Scan Line Signals

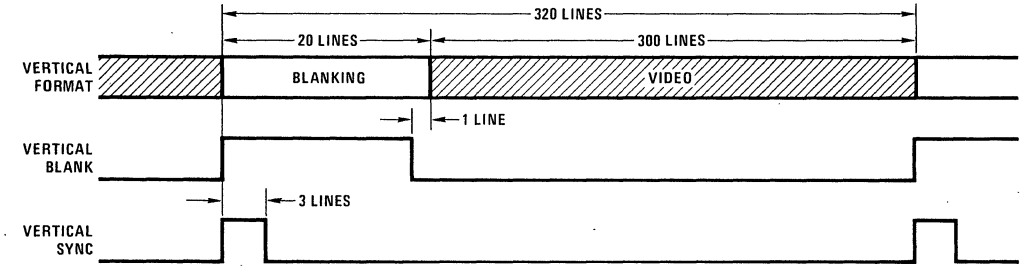


Figure 29. DP8353 60 Hz Refresh Rate Frame Signals

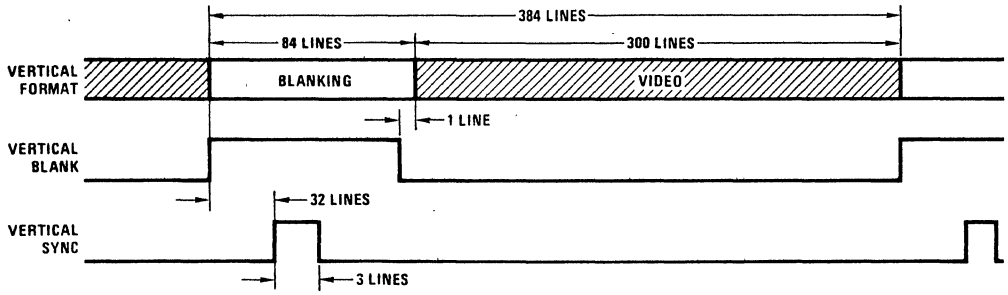


Figure 30. DP8353 50 Hz Refresh Rate Frame Signals

A Low Component Count Video Data Terminal Using the DP8350 CRT Controller and the INS8080 CPU

National Semiconductor
Application Note 199
Al Brilliott
August 1978

INTRODUCTION

The DP8350 is an I^2L – LS technology integrated circuit, designed to provide all control signals for a cathode ray tube (CRT) display system. This application note explains a system using the DP8350 and the INS8080 microprocessor. The design philosophy shows how the DP8350 interfaces to the INS8080, completing the function of a video data terminal with a minimum component count. After reading and understanding this application note the reader will realize the ease and flexibility of designing video terminals with the DP8350*. To thoroughly understand this application note the reader must be familiar with the DP8350 and the INS8080 microprocessor.

The video data terminal described is divided into the following sections, *(Figure 1).*

The DP8350 CRT controller (CRTC).

The 8080 μP system which includes ROM, RAM, interrupt instruction port, oscillator, and control support chips.

The character generator.

The communication element.

The keyboard and baud rate select ports.

THE CRTC

The DP8350 generates all the required control and timing signals for displaying video information on the video monitor. Here is a summary of the controller's functions:

Dot clock, control, and counter outputs for the character generator.

Bidirectional RAM address refresh counter for refreshing the video RAM and allowing microprocessor loading to the internal DP8350 registers.

Direct drive horizontal and vertical sync signal outputs.

Direct cursor address location output. The cursor is internally delayed or pipelined, allowing for the access time of video RAM and the character generator ROM, *(Figure 1).*

THE CPU

The microprocessor provides CRTC, operator, and external machine control for the system. When the CRT controller is not actively refreshing the video RAM, (i.e., during vertical retrace or blank scan lines), the microprocessor is enabled for system housekeeping, *(Figure 2).* This method of multiplexing the RAM with the CPU and the CRTC eliminates the need for line buffers.

*The DP8350 is equivalent to the INS8276

THE CHARACTER GENERATOR

The character generator consists of 3 elements: an address latch to hold the input address to the character ROM allowing for the access time of the ROM; the character ROM that stores the ASCII character in a form for parallel to serial conversion by the shift register; the shift register converts the character ROMs parallel output to serial form. The serial output from the shift register is the true video output, modulating the video monitors electron beam which writes characters on the screen. All of the 3 elements of the character generator are combined in the DM8678, *(Figure 3).* The DP8350 CRTC provides all the control signals for the DM8678.

THE COMMUNICATION ELEMENT

The INS8250 is the asynchronous communication element (ACE) for the data terminal. The ACE allows the CPU portion of the data terminal communication with peripherals or host computers at the correct baud rate, *(Figure 1).* The ACE is programmed by the CPU to send and receive serial data at the standard baud rates from 110 to 4800 baud. The ACE, in conjunction with the DS1488 and DS1489 line drivers and receivers, also provides full RS232C synchronous communication if higher baud rates are desired. System communication speed must always be considered to insure the baud rate does not exceed the time required for the CPU to process a data byte. Asynchronous communication at baud rates higher than 4800 are possible by adding a line buffer.

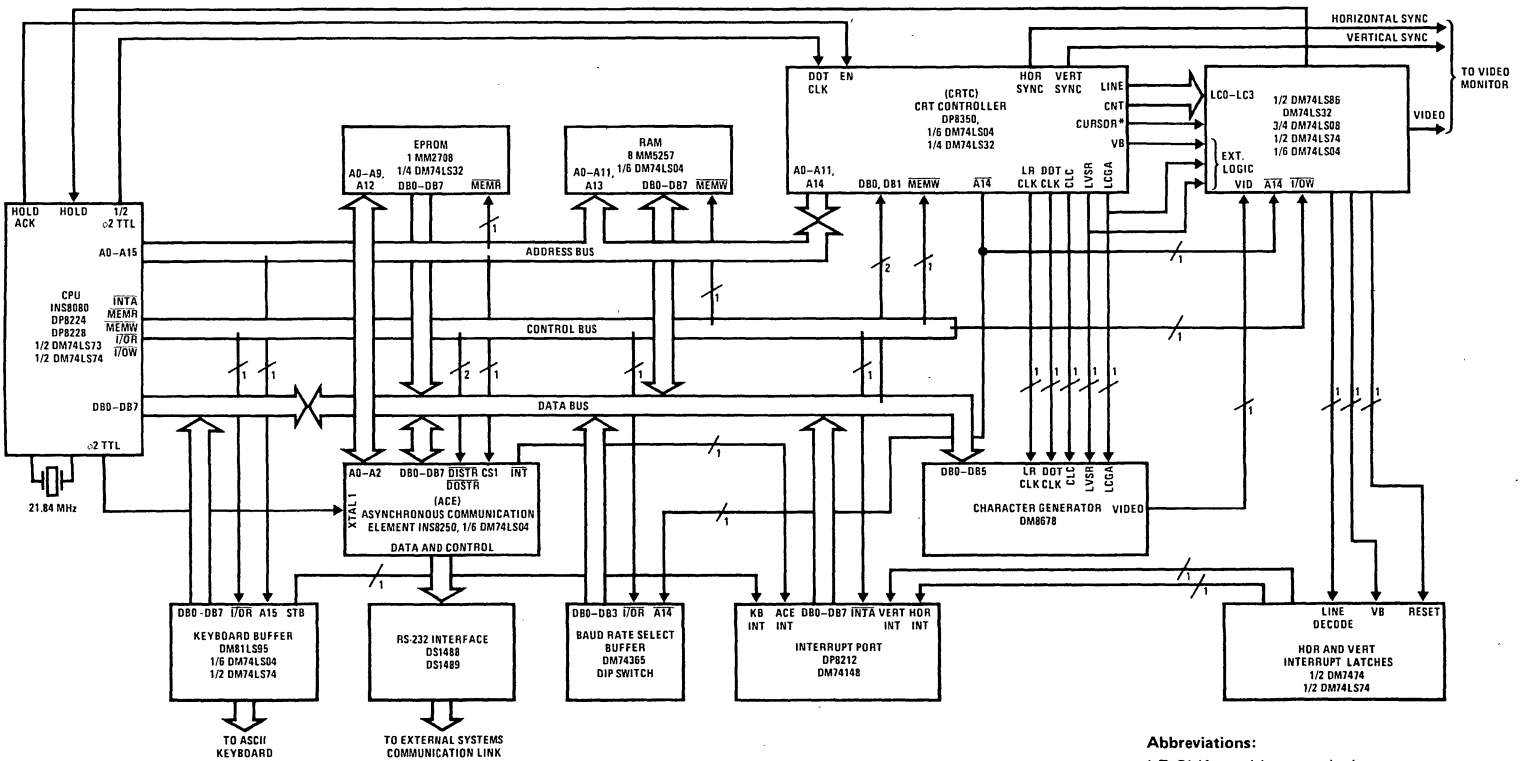
SYSTEM INITIALIZATION

Application of the terminal's power supply resets the microprocessor, the communication element, and the CRT controller. Resetting the ACE is necessary to clear the interrupt. Resetting the CRTC is not absolutely necessary since the microprocessor loads the cursor and top of page registers in the initialization routine.

Following the reset all interrupts are disabled to avoid unwanted interrupts from the CRTC, ACE, or I/O ports. Refer to the initialization routine in the flowchart.

The stack pointer is loaded to the bottom of scratch pad RAM (3FFFH) for use as the register save pointer, *(Figure 4).*

The entire RAM is written with ASCII spaces generating a cleared screen. After completion of the screen clear loop the CPU writes 000H to the cursor and the top of page registers in the DP8350 CRTC. The routine homes the cursor to the upper left corner of the screen. The top of page register was loaded with 000H, therefore, the video RAM is refreshed by the CRTC from that starting address to the last address on the screen of video RAM (1920 characters).



*The cursor is internally pipelined by the CRTC to allow for access time of the RAM and the character generator.

Abbreviations:

LR CLK	Line rate clock
CLC	Clear line counter
LVSR	Load video shift register
LCGA	Latch character generator address
Line CNT	Line counter
EN	Enable
VID	Video
KB INT	Keyboard interrupt
VB	Vertical blanking

FIGURE 1. Video Data Terminal Detailed Block Diagram

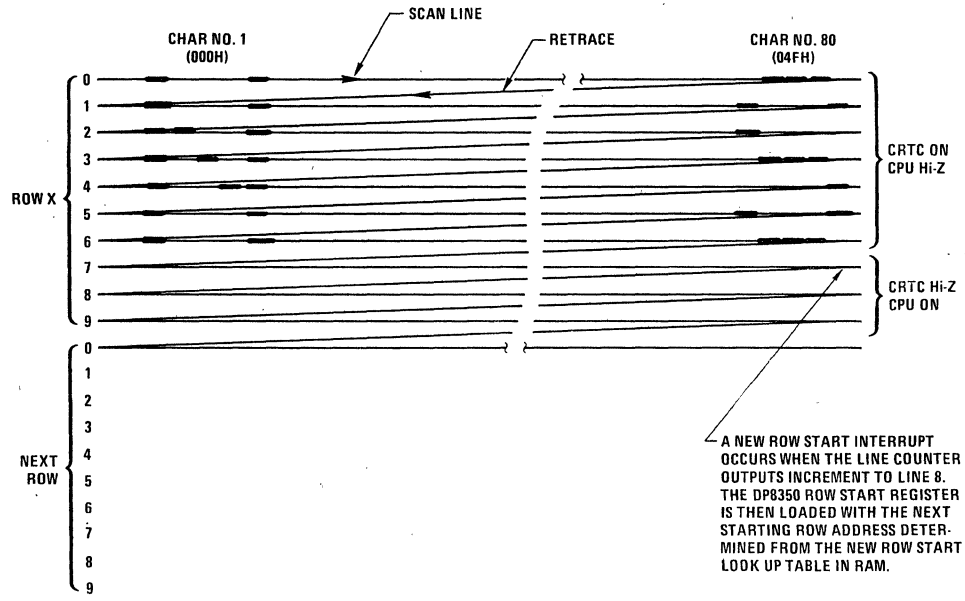


FIGURE 2. Row Start Interrupting and Multiplexing the INS8080 with the DP8350

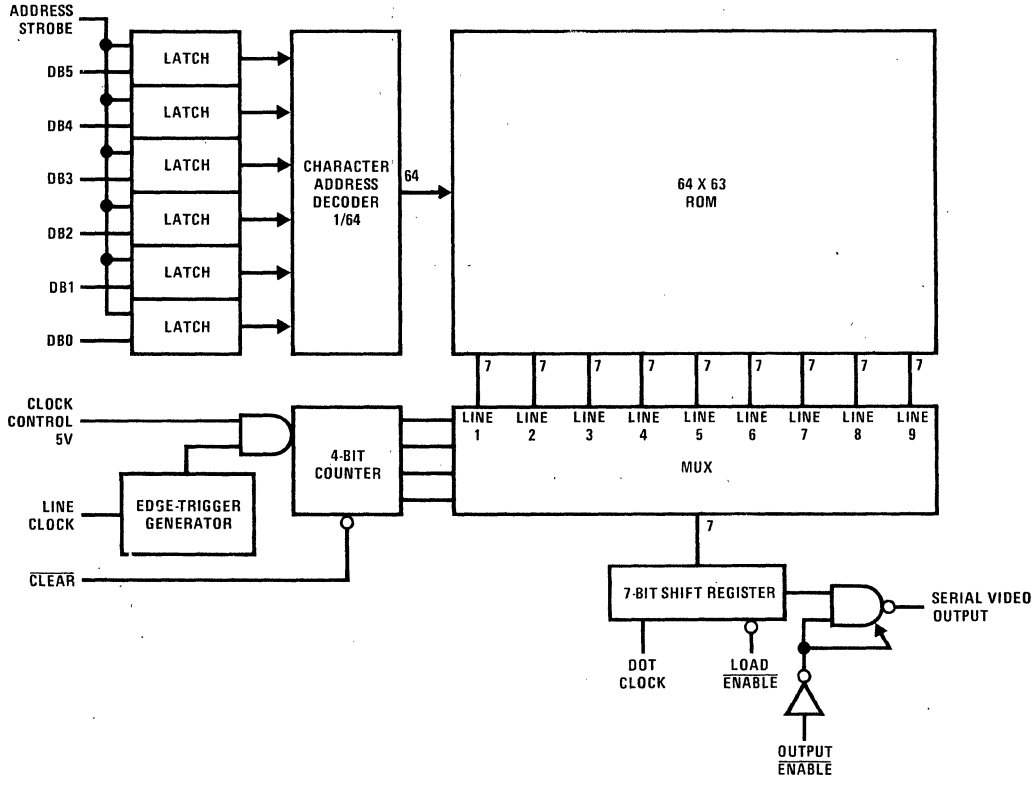


FIGURE 3. DM8678 Character Generator Block Diagram

The CPU is ready to perform the communication element (ACE) load routine. First, the baud rate divisor for the ACE must be determined. The baud rate select switch is read providing a code which corresponds to the appropriate 16-bit divisor for the ACE. This divisor determines the baud rate at which the ACE will communicate. Any additional programming requirements needed for the ACE to communicate with host computer systems could also be done at this time. The software in this system does not contain any additional programming for the ACE. There are many programming modes related to the ACE. Details of these modes are beyond the scope of this application note.

The row start look-up table, *(Figure 5)*, is loaded up by a simple algorithm that loads and adds the data for referencing a row number to that row's starting address. The reference table, *(Figure 6)*, is initialized next by direct loading. This table provides the CPU with top of page, bottom of page, next row load, cursor row, and scratch row numbers for system housekeeping.

Finally, the new row start and vertical interrupt latches are cleared, *(Figure 7)*. The register pointers are loaded and the CPU is forced in a wait loop with interrupts enabled.

NON-SEQUENTIAL ADDRESSING

The data terminal described here was designed for non-sequential starting row addressing. In many systems sequential row addressing is used. If a character row consists of 10 scan lines the RAM is addressed 10 repetitive times from 000H through 04FH, *(Figure 2)*. The next row is refreshed in the same manner from 050H to 09FH. The starting row address is sequential 000H, 050H, 0A0H–EB0H for row numbers 0H, 1H, 2H,–2FH, respectively. Non-sequential row addressing would be equivalent to 050H, 000H, 0A0H–EB0H for row numbers 1H, 0H,–2FH, respectively, *(Figure 4)*.

In conjunction with the CPU, non-sequential row addressing is quite easily accomplished with the DP8350 since this is one of the features designed into the part. Accomplishing this task basically requires the following sequence of events. Assume the CRTC has finished writing a video row in the middle of the monitor's screen. This system has a 5 x 7 character font in a 7 x 10 field, *(Figure 2)*. At the completion of the last video scan line 7 the CRTC line counters continue to count the last 3 lines. Video is not present since the character is only 7 scan lines high. The blank scan lines are 7, 8, and 9 permitting the CRTC address outputs to be TRI-STATED®, allowing the CPU to run. When the line counter outputs increment to scan line 8 an interrupt signals the CPU. The interrupt occurring is the new row start interrupt. The interrupt routine fetches the next CRTC row number from the reference table *(Figure 6)*. This number is converted to the new starting row address, explained later, and loaded to the CRTC row start register. The CPU finishes the routine by clearing the interrupt, readying itself for the next new row start interrupt. The entire routine takes 1 scan line of time, approximately 64 μs. The CRTC continues to scan the video RAM from that new starting address on for the next 7 repetitive scan lines of the next row. Many advantages become apparent using the non-sequential addressing scheme. Scrolling up or down with the cursor always on the screen may be done faster and easier from a hardware/software standpoint. Exchanging one row with another row is fast since it is not necessary to rewrite the video RAM. Row swapping is useful for higher end terminals requiring row editing functions.

ADDRESS MAP

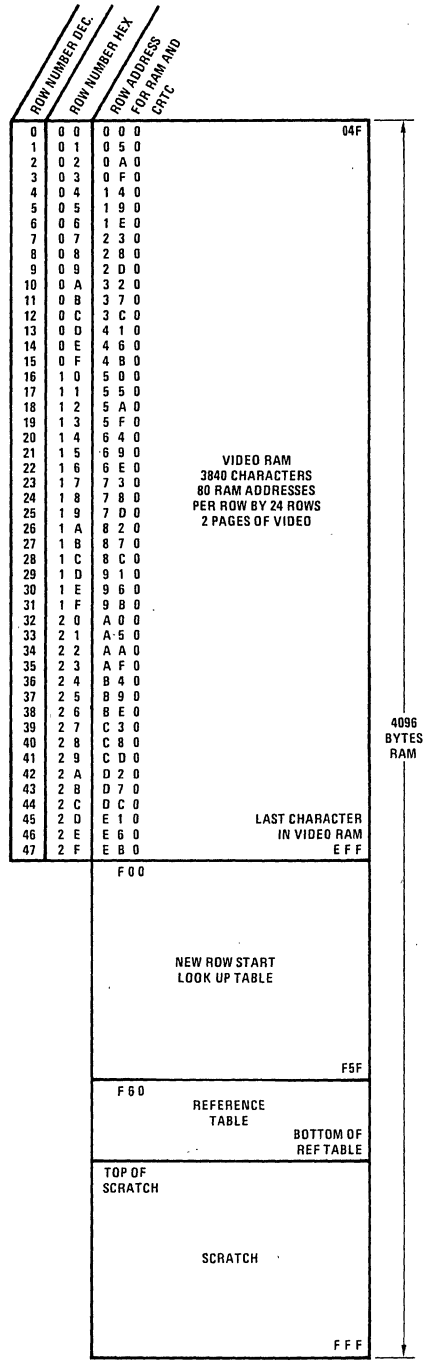


FIGURE 4. RAM Organization

MEMORY REFERENCE TABLES

Page 1

ROW NUMBER DEC	ROW NUMBER HEX	NRS HIGH ADDRESS	NRS HIGH ROW DATA	NRS LOW ADDRESS	NRS LOW ROW DATA
0	0 0	3 F 0 0	3 0	3 F 3 0	0 0
1	0 1	3 F 0 1	3 0	3 F 3 1	5 0
2	0 2	3 F 0 2	3 0	3 F 3 2	A 0
3	0 3	3 F 0 3	3 0	3 F 3 3	F 0
4	0 4	3 F 0 4	3 1	3 F 3 4	4 0
5	0 5	3 F 0 5	3 1	3 F 3 5	9 0
6	0 6	3 F 0 6	3 1	3 F 3 6	E 0
7	0 7	3 F 0 7	3 2	3 F 3 7	3 0
8	0 8	3 F 0 8	3 2	3 F 3 8	8 0
9	0 9	3 F 0 9	3 2	3 F 3 9	D 0
10	0 A	3 F 0 A	3 3	3 F 3 A	2 0
11	0 B	3 F 0 B	3 3	3 F 3 B	7 0
12	0 C	3 F 0 C	3 3	3 F 3 C	C 0
13	0 D	3 F 0 D	3 4	3 F 3 D	1 0
14	0 E	3 F 0 E	3 4	3 F 3 E	6 0
15	0 F	3 F 0 F	3 4	3 F 3 F	B 0
16	1 0	3 F 1 0	3 5	3 F 4 0	0 0
17	1 1	3 F 1 1	3 5	3 F 4 1	5 0
18	1 2	3 F 1 2	3 5	3 F 4 2	A 0
19	1 3	3 F 1 3	3 5	3 F 4 3	F 0
20	1 4	3 F 1 4	3 6	3 F 4 4	4 0
21	1 5	3 F 1 5	3 6	3 F 4 5	9 0
22	1 6	3 F 1 6	3 6	3 F 4 6	E 0
23	1 7	3 F 1 7	3 7	3 F 4 7	3 0

Page 2

ROW NUMBER DEC	ROW NUMBER HEX	NRS HIGH ADDRESS	NRS HIGH ROW DATA	NRS LOW ADDRESS	NRS LOW ROW DATA
24	1 8	3 F 1 8	3 7	3 F 4 8	8 0
25	1 9	3 F 1 9	3 7	3 F 4 9	D 0
26	1 A	3 F 1 A	3 8	3 F 4 A	2 0
27	1 B	3 F 1 B	3 8	3 F 4 B	7 0
28	1 C	3 F 1 C	3 8	3 F 4 C	C 0
29	1 D	3 F 1 D	3 9	3 F 4 D	1 0
30	1 E	3 F 1 E	3 9	3 F 4 E	6 0
31	1 F	3 F 1 F	3 9	3 F 4 F	B 0
32	2 0	3 F 2 0	3 A	3 F 5 0	0 0
33	2 1	3 F 2 1	3 A	3 F 5 1	5 0
34	2 2	3 F 2 2	3 A	3 F 5 2	A 0
35	2 3	3 F 2 3	3 A	3 F 5 3	F 0
36	2 4	3 F 2 4	3 B	3 F 5 4	4 0
37	2 5	3 F 2 5	3 B	3 F 5 5	9 0
38	2 6	3 F 2 6	3 B	3 F 5 6	E 0
39	2 7	3 F 2 7	3 C	3 F 5 7	3 0
40	2 8	3 F 2 8	3 C	3 F 5 8	8 0
41	2 9	3 F 2 9	3 C	3 F 5 9	D 0
42	2 A	3 F 2 A	3 D	3 F 5 A	2 0
43	2 B	3 F 2 B	3 D	3 F 5 B	7 0
44	2 C	3 F 2 C	3 D	3 F 5 C	C 0
45	2 D	3 F 2 D	3 E	3 F 5 D	1 0
46	2 E	3 F 2 E	3 E	3 F 5 E	6 0
47	2 F	3 F 2 F	3 E	3 F 5 F	B 0

FIGURE 5. New Row Start Look Up Table

FUNCTION	ADDRESS	DATA	INITIALIZED DATA
Last Row #	3F60	XY	17
8080 Row #	3F61	XY	00
First Row #	3F62	XY	00
Character #	3F63	XY	00
CRTC Row #	3F64	XY	00
Row Save #	3F65	XY	00
Temp. 1	3F66	XY	00
Temp. 2	3F67	XY	00

FIGURE 6. Reference Table

COMMAND		FUNCTION
OUT	40	Clear new row start and vertical interrupt latches
IN	80	Read keyboard
IN	40	Read baud rate select switch

FIGURE 7. Input/Output Space

DEVICE	ADDRESS*
ROM	0000 to 0FFF
RAM	3000 to 3FFF
CRTC	5000 to 5FFF
ACE	9000 to 9007

*Direct device selecting was used to minimize the system component count

FIGURE 8. CPU Addressing Space

ROW NUMBER DEC	ROW NUMBER HEX	NRS HIGH ADDRESS	NRS HIGH ROW DATA	NRS LOW ADDRESS	NRS LOW ROW DATA
32	2 0	3 F 2 0	3 A	3 F 5 0	0 0

Row Start Address for Row 20H.
3XXX Selects RAM.
5XXX Selects CRTC.

FIGURE 9. Example From the New Row Start Look Up Table

ROW LOADING DETAILS

Obtaining the next starting row address for the CRT controller is accomplished by an addressing and adding scheme from the new row start look-up table. The same scheme is used to determine any needed address, given the row number.

Figure 9 shows a row number and address taken from the new row start look-up table.

The row number is loaded from the reference table in RAM to a register. The CPU determines the starting address from the row number and stores it in a 16-bit pointer register. The higher order 4 bits contain address for the RAM or the CRT controller, *(Figure 8)*.

Here are the details of how this is accomplished. Refer to the new row start interrupt in the software listing and *Figure 9*.

The CPU D-E registers are loaded to point to a row number in the reference table. The number is put in the accumulator and moved into the E register. The D-E register in this example now contains 3F20 which points to NRS HIGH ROW DATA (3A). The addressed data is moved to the accumulator and then to the H register. If it was desired to point to the CRTC then 20H would have been added to it first. The D-E register still contains 3F20H. To obtain the NRS LOW ROW DATA the E register is moved to the accumulator and 30H is added to it. Now the D-E register contains 3F50H and points to NRS LOW ROW DATA (00H). The data is loaded to the accumulator and then to the L register. The H-L registers contain 3A00H which is the starting row address for row number 20H. The method just described is used throughout the terminals program to move the cursor, load the top of page, and load the new starting row address in the CRTC.

VERTICAL INTERRUPT

The vertical interrupt occurs when the CRTC has completed refreshing a video page (1920 characters) of information. Vertical blanking identifies that condition and interrupts the CPU forcing it to the vertical interrupt routine. Refer to the vertical interrupt in the flow chart. The routine moves the first row number to the CRTC row number, updating it so the next new row start load occurs with the top of the page address or the first row of the video screen.

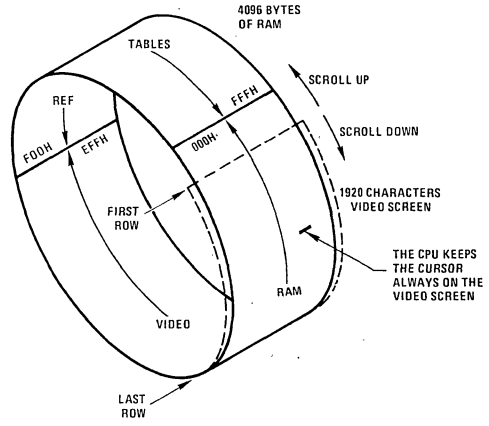
KEYBOARD INTERRUPT

The external keyboard requirements are ASCII outputs with a suitable strobe to interrupt the CPU for keyboard servicing. Refer to the keyboard interrupt in the flow chart. After the keyboard buffer is read the data byte is tested for a (CNTL E), new baud rate command. If the test fails the CPU writes the data byte to the ACE. Passing the test forces the CPU to read the baud switch and load the ACE with the new baud rate.

ACE INTERRUPT

As mentioned above, a data byte read from the keyboard that is not a baud rate command enters the accumulator. The CPU writes the data byte from the accumulator to the transmitter holding register in the ACE. The ACE proceeds to shift out the data byte, with the appropriate start and stop bits, serially from the (SOUT) output. The data is shifted to the serial input (SIN) of the ACE and loaded into the receiver holding register. When the register is full the ACE interrupts the CPU, initializating the ACE service routine. Refer to the ACE interrupt in the flow chart.

The CPU reads the receiver holding register in the ACE. Reading the ACE resets the interrupt. The data byte now resides in the accumulator. The CPU tests for a control or an escape function. The function is executed if test conditions are met. Refer to the keyboard interrupt routine in the software listing. The data byte is written to the video RAM at the cursor address which appears on the monitor screen. The cursor and character numbers are incremented as long as it is not at the end of a row. A character at the end of a row requires further testing to recognize the following situations. Is it the last row on the monitor's screen? Or is it on the maximum row of the video RAM? Essentially, the cursor is forced to stay visible on the video monitor's screen and video RAM is always kept out of scratch pad RAM, *(Figure 10)*.



The video screen is allowed to scroll only through the video RAM (000H to EFFH). The CPU keeps the video screen within these bounds by loading the new row start register with that address range only (row 00H to 2FH).

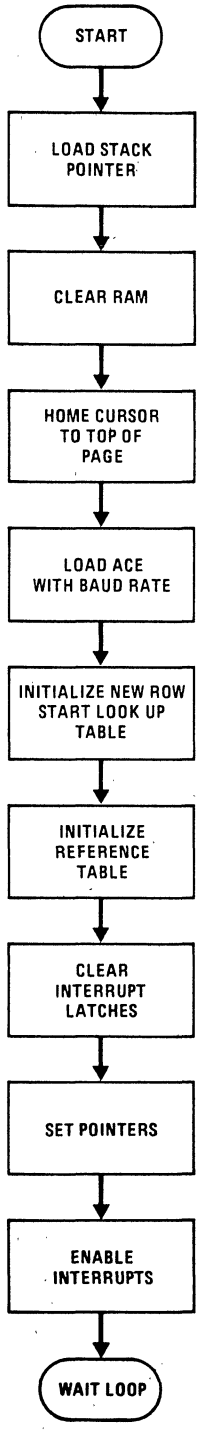
FIGURE 10. Drum Analogy for the RAM

FULL/HALF DUPLEX OPERATION

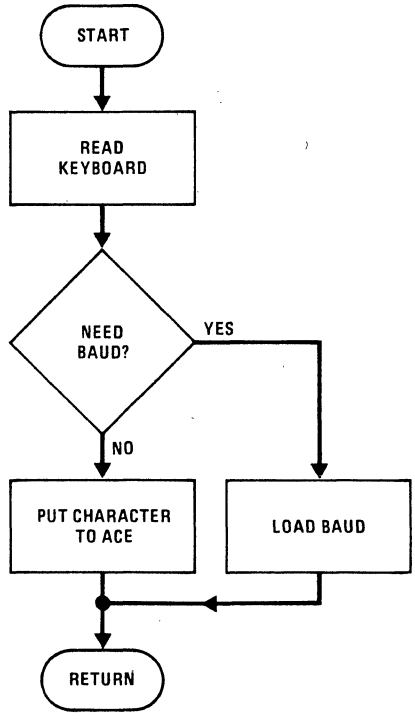
The data terminal and a host computer in the full duplex mode of operation would receive the serial information, process it, and send it back to the SIN input of ACE. Using the terminal in a stand-alone mode for testing, the serial out SOUT is tied to the serial in SIN of the ACE. In the half duplex mode a data byte is sent to the host computer at the same time it is sent to the terminal. When the data terminal is set up to communicate with a host computer the full duplex mode of operation is desirable.

DP8350/INS8080 VIDEO DATA TERMINAL BASIC SOFTWARE FLOW CHART

Initilization

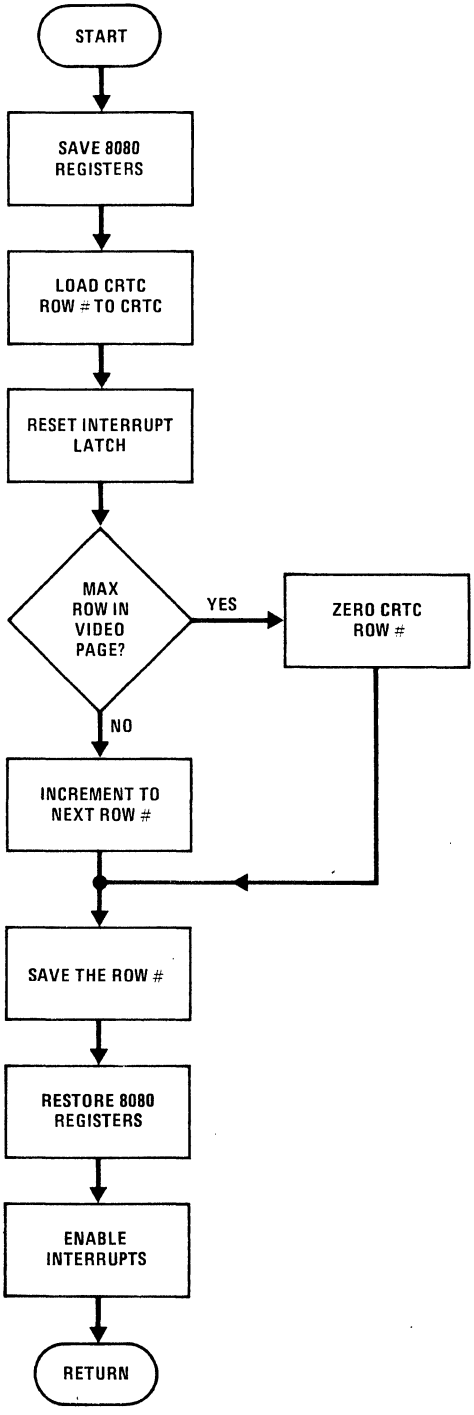


Keyboard Interrupt

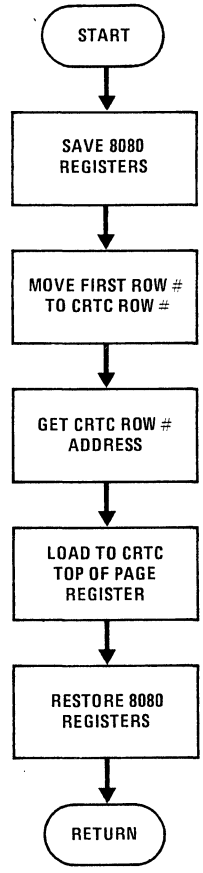


DP8350/INS8080 VIDEO DATA TERMINAL BASIC SOFTWARE FLOW CHART (Continued)

New Row Start Interrupt

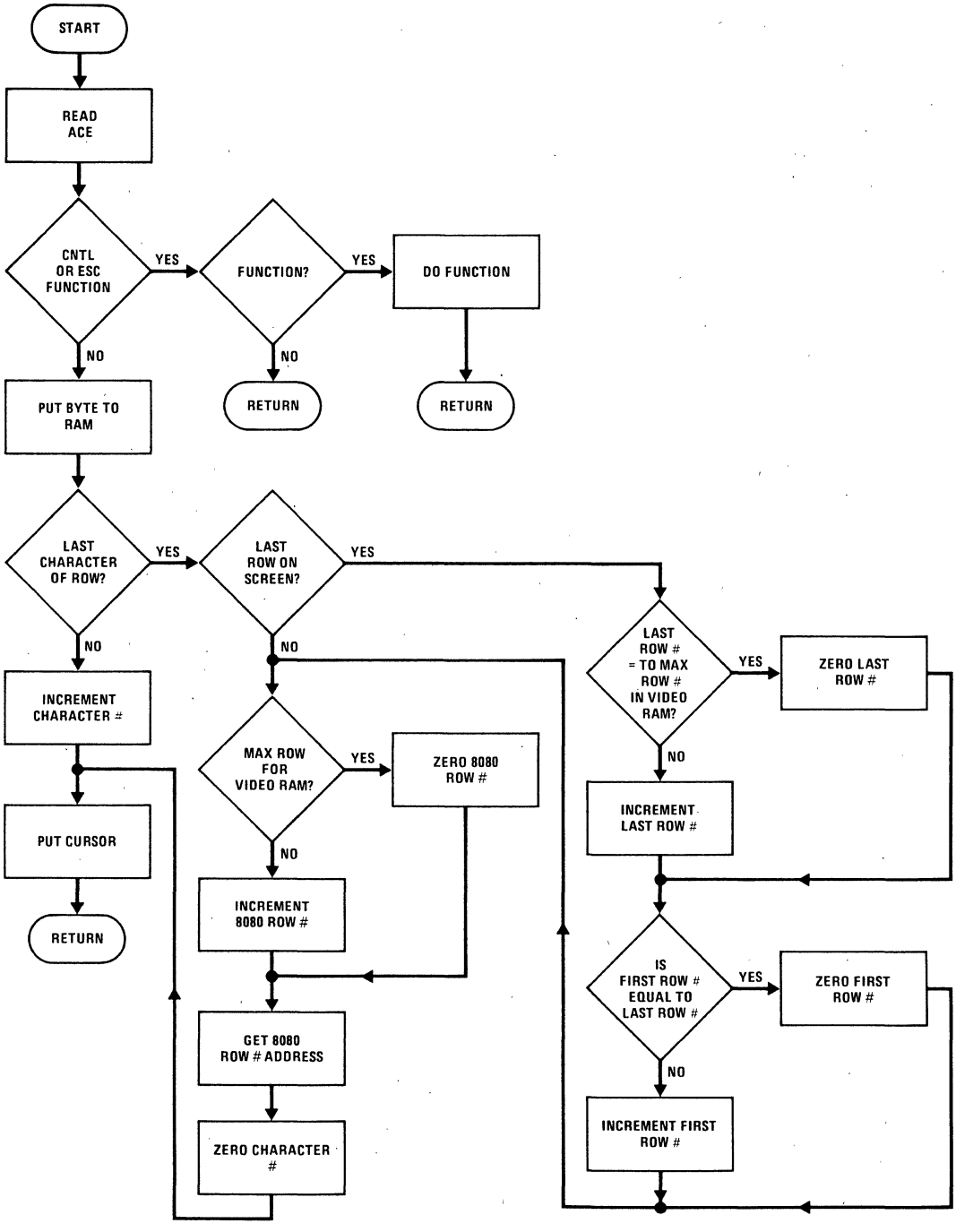


Vertical Interrupt



DP8350/INS8080 VIDEO DATA TERMINAL BASIC SOFTWARE FLOW CHART (Continued)

ACE Interrupt

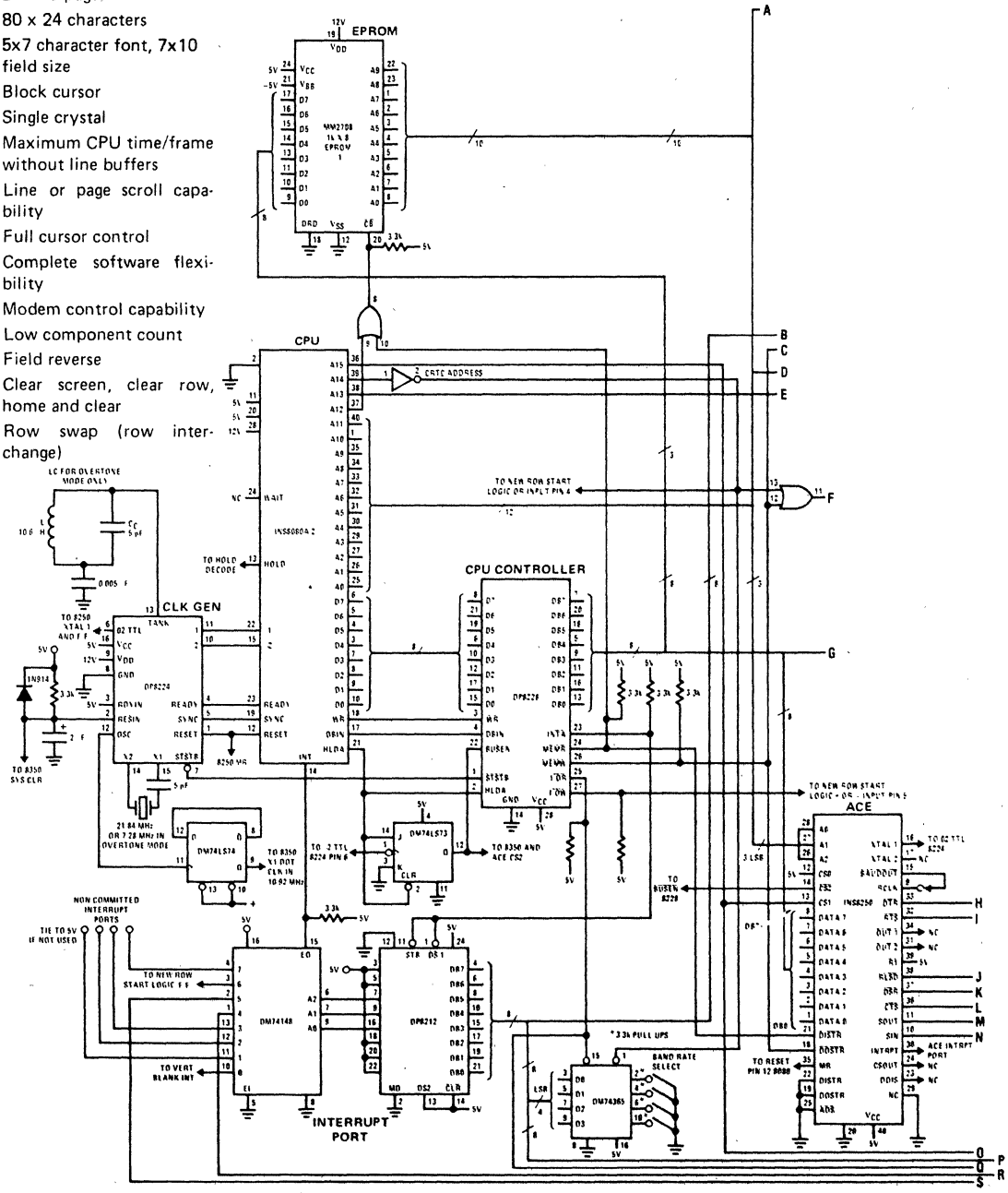


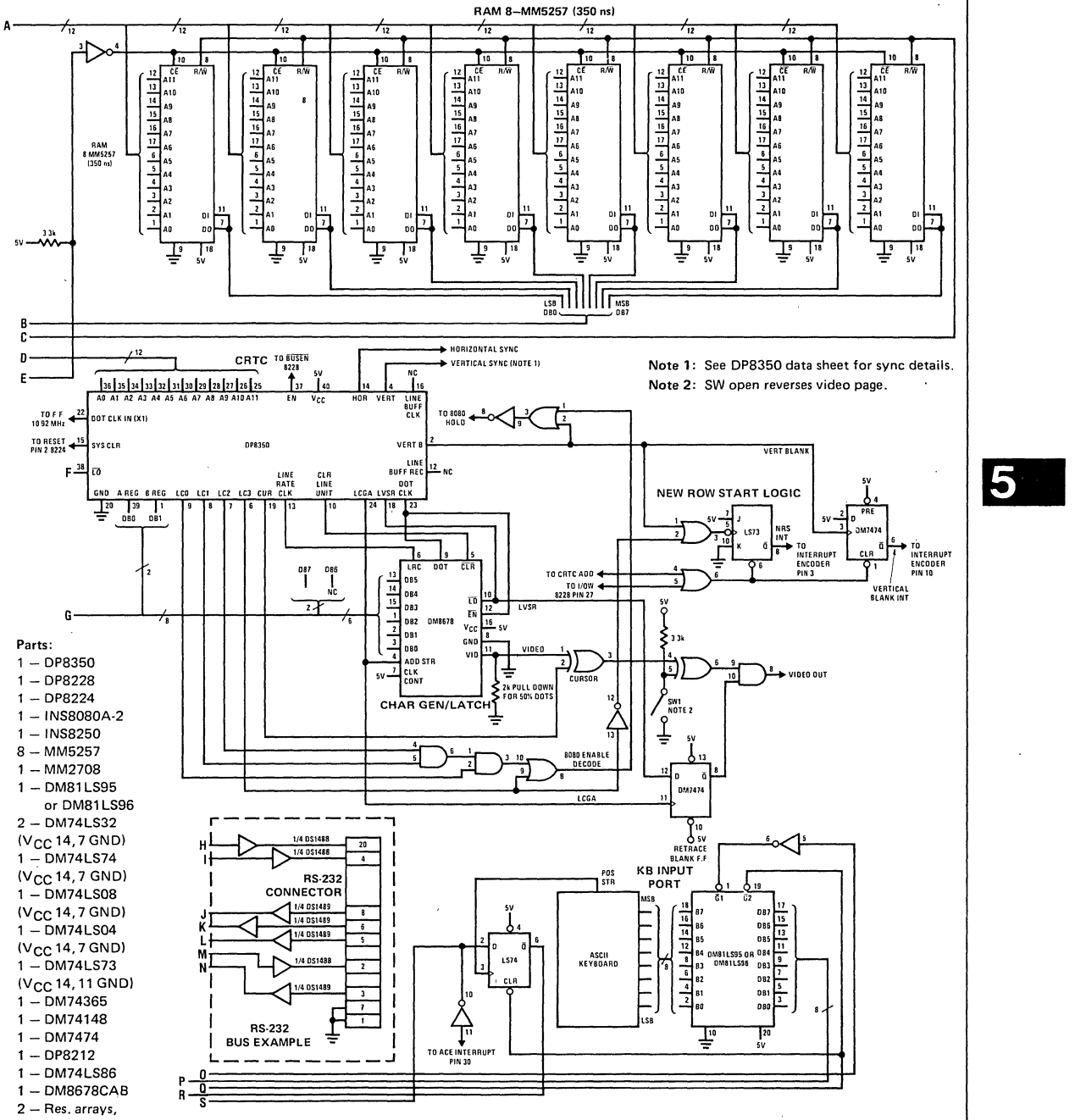
```
                        TITLE CRTC , 8080A 02/15/78

                ;** NATIONAL SEMICONDUCTOR S
                ;   SERIES PROGRAMMABLE CRT CONTROLLER BOARD **

                ;AL BRILLIOTT-JIM TROUTNER

      0060      LASTROW =           060
      0061      ROW8080 =           061
      0062      FIRSTRO =           062
      0063      CHARNUM =           063
      0064      CRTCROW =           064
      0065      ROWSAVE =           065
      0066      TEMP1   =           066
      0067      TEMP2   =           067
      0068      IMASK   =           068

0000                  =0000
0000 F3     START     DI                  ;DISABLE INTERRUPTS
0001 31FF3F           LXI     SP,03FFF    ;LOAD STACK POINTER
0004 C33B00           JMP     INIT        ;JUMP TO INITILIZE ROUTINE
0007                  =0008
0008 C32502           JMP     NEWRO       ;NEW ROW START INTERRUPT
000B                  =0010
0010 C34A01           JMP     INTACE      ;ACE INTERUPT
0013                  =0018
0018 C93601           JMP     INTKB       ;KEYBOARD INTERUPT
001B                  =0038
0038 C34F02           JMP     VERTI       ;VERTICAL INTERUPT
003B 210030 INIT      LXI     H,03000     ;1ST RAM ADDRESS
003E 0E20             MVI     C,020       ;ASCII SPACE INTO C REG
0040 3E3F             MVI     A,03F       ;MAX RAM ADDRESS
0042 71     CLRAM     MOV     M,C         ;ASCII SPACE INTO MEM
0043 23               INX     H           ;NEXT RAM ADDRESS
0044 BC               CMP     H           ;MAX RAM ADDRESS?
0045 C24200           JNZ     CLRAM       ;IF NO THEN NEXT ADD
0048 0E00             MVI     C,000
004A 3E40             MVI     A,040
004C 71     CLRAM1    MOV     M,C
004D 23               INX     H
004E BC               CMP     H
004F C24C00           JNZ     CLRAM1
0052 CD8700           CALL    HMCUR       ;GO TO CUR HOME ROUTINE
0055 CD9300           CALL    BAUD        ;GO TO BAUD LOAD ROUTINE

                ;NEW ROW START LOOK UP TABLE GENERATION

0058 21003F           LXI     H,03F00     ;N R S  HIGH ADDRESS
005B 11303F           LXI     D,03F30     ;N R S  LOW ADDRESS
005E 010030           LXI     B,03000     ;N R S  ADDRESS DATA
0061 70     NRS       MOV     M,B         ;STORE TO N R S  DATA TABLE
0062 79               MOV     A,C         ;N R S  DATA LOW TO ACC
0063 12               STAX    D           ;STORE TO N R S  DATA TABLE L
0064 C650             ADI     050         ;ACC READY FOR NEXT LOAD
0066 4F               MOV     C,A         ;ACC TO N R S  DATA HIGH
0067 78               MOV     A,B         ;N R S  DATA TO ACC
0068 CE00             ACI     000         ;ADD CARRY BIT TO DATA HIGH
006A 47               MOV     B,A         ;MOVE RESULT TO N R S  DATA H
006B 2C               INR     L           ;INCREMENT N R S  HIGH ADD
006C 1C               INR     E           ;INCREMENT N R S  LOW ADD
006D 7B               MOV     A,E         ;N R S  ADD LOW TO ACC
006E FE60             CPI     LASTROW     ;MAX TABLE ADDRESS
0070 C26100           JNZ     NRS         ;IF FALSE JUMP

                ;REFERENCE TABLE INITILIZE

0073 3E17             MVI     A,017       ;LAST ROW NUMBER TO ACC
0075 12               STAX    D           ;STORE TO REFERENCE TABLE

                ;CLEAR PERIPHERAL INTERRUPT FLOPS

0076 D340             OUT     040         ;N R S  INTERRUPT CLEAR
0078 DB80             IN      080         ;KEYBOARD INTERRUPT CLEAR

                ;SET UP POINTERS

007A 11603F           LXI     D,03F60     ;POINT D-E TO REFERENCE TABLE
007D 210030           LXI     H,03000     ;POINT H-L TO 1ST RAM LOCATI
0080 010090           LXI     B,09000     ;POINT B-C TO ACE

                ;WAIT LOOP FOR INTERUPTS

0083 FB     BACK      EI                  ;ENABLE INTERRUPTS
0084 C38300           JMP     BACK        ;LOOP UNTIL INTERRUPTED

                ;HOME UP CURSOR

0087 210050 HMCUR     LXI     H,05000     ;POINT B-C TO CRTC
008A 3E02             MVI     A,002       ;T O P  REGISTER SELECT
008C 77               MOV     M,A         ;T O P  LOAD
008D 3C               INR     A           ;CURSOR REGISTER SELECT
008E 77               MOV     M,A         ;CURSOR LOADS TO T O P
008F 210030           LXI     H,03000     ;POINT H-L TO 1ST RAM ADD
0092 C9               RET                 ;RETURN

                ;BAUD RATE SELECT

0093 D5     BAUD      PUSH    D           ;SAVE D-E REGISTERS
0094 DB40             IN      040         ;READ BAUD SELECT CODE
0096 E60F             ANI     00F         ;ZERO THE HIGH ORDER 4 BITS
0098 FE00             CPI     000
009A CAD400           JZ      B110        ;110 BAUD ROUTINE
009D FE01             CPI     001
009F CADA00           JZ      B150        ;150 BAUD ROUTINE
00A2 FE02             CPI     002
00A4 CAE000           JZ      B300        ;300 BAUD ROUTINE
00A7 FE03             CPI     003
00A9 CAE600           JZ      B600        ;600 BAUD ROUTINE
00AC FE04             CPI     004
00AE CAEC00           JZ      B1200       ;1200 BAUD ROUTINE
00B1 FE05             CPI     005
00B3 CAF200           JZ      B1800       ;1800 BAUD ROUTINE
00B6 FE06             CPI     006
00B8 CAF800           JZ      B2000       ;2000 BAUD ROUTINE
00BB FE07             CPI     007
00BD CAFE00           JZ      B2400       ;2400 BAUD ROUTINE
00C0 FE08             CPI     008
00C2 CA0401           JZ      B3600       ;3600 BAUD ROUTINE
00C5 FE09             CPI     009
00C7 CA0A01           JZ      B4800       ;4800 BAUD ROUTINE
00CA FE0A             CPI     00A
00CC CA1001           JZ      B7200       ;7200 BAUD ROUTINE
00CF FE0B             CPI     00B
00D1 CA1601           JZ      B9600       ;9600 BAUD ROUTINE

                ;BAUD RATE SET UP ROUTINES

00D4 116305 B110      LXI     D,00563     ;110 BAUD DIVISOR
00D7 C31C01           JMP     ACELD       ;GO TO ACE LOAD ROUTINE
00DA 11F303 B150      LXI     D,003F3     ;150 BAUD DIVISOR
00DD C31C01           JMP     ACELD
00E0 11F901 B300      LXI     D,001F9     ;300 BAUD DIVISOR
00E3 C31C01           JMP     ACELD
00E6 11FC00 B600      LXI     D,000FC     ;600 BAUD DIVISOR
00E9 C31C01           JMP     ACELD
00EC 117E00 B1200     LXI     D,0007E     ;1200 BAUD DIVISOR
00EF C31C01           JMP     ACELD
00F2 115400 B1800     LXI     D,00054     ;1800 BAUD DIVISOR
00F5 C31C01           JMP     ACELD
00F8 114C00 B2000     LXI     D,0004C     ;2000 BAUD DIVISOR
00FB C31C01           JMP     ACELD
00FE 113F00 B2400     LXI     D,0003F     ;2400 BAUD DIVISOR
0101 C31C01           JMP     ACELD
0104 112A00 B3600     LXI     D,0002A     ;3600 BAUD DIVISOR
0107 C31C01           JMP     ACELD
010A 112000 B4800     LXI     D,00020     ;4800 BAUD DIVISOR
010D C31C01           JMP     ACELD
0110 111500 B7200     LXI     D,00015     ;7200 BAUD DIVISOR
0113 C31C01           JMP     ACELD
0116 111000 B9600     LXI     D,00010     ;9600 BAUD DIVISOR
0119 C31C01           JMP     ACELD

                ;ACE LOAD ROUTINE

011C 010390 ACELD     LXI     B,09003     ;POINT B C TO ACE
011F 3E83             MVI     A,083       ;INIT BAUD LOAD - 8 BITS
0121 02               STAX    B           ;DO INIT BAUD LOAD
0122 0E01             MVI     C,001       ;POINT TO BAUD HIGH
0124 7A               MOV     A,D         ;GET BAUD HIGH
0125 02               STAX    B           ;STORE BAUD HIGH TO ACE
0126 0E00             MVI     C,000       ;POINT ACE TO BAUD LOW
0128 7B               MOV     A,E         ;GET BAUD LOW
0129 02               STAX    B           ;STORE BAUD LOW TO ACE
012A 0E03             MVI     C,003       ;RESET DLAB TO ZERO
012C 79               MOV     A,C         ;INIT ACE T/R
012D 02               STAX    B           ;PUT TO ACE
012E 0E01             MVI     C,001       ;INTERRUPT ENABLE REG
0130 79               MOV     A,C         ;SELECT RECEIVED DATA INTERR
0131 02               STAX    B           ;LOAD IT
0132 0E00             MVI     C,000       ;RESTORE B-C ACE POINTER
0134 D1               POP     D           ;RESTORE D-E REGISTERS
0135 C9               RET                 ;RETURN

                ;KEYBOARD INTERRUPT ROUTINE

0136 DB80   INTKB     IN      080         ;READ KEYBOARD
0138 FB               EI                  ;ENABLE INTERRUPTS
0139 FE05             CPI     005         ;NEED BAUD RATE? (CNTL E)
013B CA9300           JZ      BAUD        ;IF YES GO TO BAUD ROUTINE
013E FE12             CPI     012         ;INVERT NEXT CNTL R
0140 CA4803           JZ      IVERTN
0143 FE13             CPI     013         ;INVERT ROW CNTL S
0145 CA5403           JZ      IVERTR
0148 02               STAX    B           ;STORE BYTE TO ACE
0149 C9               RET                 ;RETURN

                ;ACE INTERUPT ROUTINE

014A 0A     INTACE    LDAX    B           ;LOAD ACE DATA BYTE TO ACC
014B FB               EI                  ;ENABLE INTERRUPTS
014C FE7E             CPI     07E
014E CA7001           JZ      FUNC        ;TEST FOR ESC COMAMD
0151 FE7F             CPI     07F         ;TEST FOR DEL COMAND
0153 CA7001           JZ      FUNC
0156 5F               MOV     E,A         ;SAVE CHAR IN REG E
0157 E660             ANI     060         ;MASK OUT BITS FOR CNTL TEST
0159 CA7001           JZ      FUNC        ;IF ZERO JMP TO CNTL FUNC
015C 3A683F           LDA     03F68       ;LOAD INVERT MASK
015F B3               ORA     E           ;OR MASK AND CHAR
0160 77               MOV     M,A         ;STORE DATA BYTE TO RAM

                ;ADVANCE CURSOR

0161 1E63   ADCUR     MVI     E,CHARNUM   ;POINT B-C TO CHAR #
0163 1A               LDAX    D           ;LOAD CHAR # TO ACC
0164 23               INX     H           ;NEXT CHAR LOCATION
0165 FE4F             CPI     04F         ;LAST CHAR OF ROW?
0167 CA8E01           JZ      NXRO        ;IF TRUE JUMP TO NEXT ROW
016A C601             ADI     001         ;INCREMENT CHAR #
016C 12               STAX    D           ;STORE CHAR # TO RAM REF
016D C3B301           JMP     PCUR        ;PUT CURSOR

                ;TEST FOR FUNCTION

0170 7B     FUNC      MOV     A,E
0171 FE01             CPI     001         ;HOME AND CLEAR CNTL A (SOH)
0173 CA0000           JZ      START
0176 FE0D             CPI     00D         ;CARRAGE RETURN
0178 CA6E02           JZ      CR
017B FE11             CPI     011         ;SAVE ROW # CNTL Q (DC1)
017D CA7802           JZ      SAVRO
0180 FE0C             CPI     00C         ;ADVANCE CURSOR CNTL L (FF)
0182 CA6101           JZ      ADCUR
0185 FE02             CPI     002         ;HOME UP CNTL B (STX)
0187 CAA402           JZ      HOME
018A FE1A             CPI     01A         ;SWAP   CNTL Z (SUB)
018C CAB502           JZ      SWAP
018F FE0A             CPI     00A         ;LINEFEED
0191 CA8D02           JZ      LF
0194 FE08             CPI     008         ;BACKSPACE CNTL H (BS)
0196 CAE002           JZ      BS
0199 FE0B             CPI     00B         ;UP CURSOR CNTL K (VT)
019B CAF102           JZ      UPCUR
019E FE18             CPI     018         ;CLEAR ROW CNTL X (CAN)
01A0 CA3003           JZ      CLROW
01A3 FE07             CPI     007         ;RING BELL CNTL G (BEL)
01A5 CA4503           JZ      BELL
01A8 FE12             CPI     012         ;INVERT NEXT CNTL R (DC2)
01AA CA4803           JZ      IVERTN
01AD FE13             CPI     013         ;INVERT ROW CNTL S (DC3)
01AF CA5403           JZ      IVERTR
01B2 C9               RET                 ;RETURN

                ;STORE CURSOR TO CRTC FROM H-L REGISTERS

01B3 7C     PCUR      MOV     A,H         ;H REG TO ACC
01B4 C620             ADI     020         ;SET H-L REG TO CRTC ADD
01B6 67               MOV     H,A         ;H IS CRTC ADD
01B7 3603             MVI     M,003       ;CURSOR REGISTER SELECT
01B9 7C               MOV     A,H         ;H REG SET BACK TO VIDIO RAM
01BA D620             SUI     020         ;ADDRESS
01BC 67               MOV     H,A
01BD C9               RET                 ;RETURN

                ;LAST ROW ON SCREEN

01BE CDDC01 NXRO      CALL    NXRO1       ;GO TO NEXT ROW SUBROUTINE
01C1 CDF301           CALL    ZCHAR       ;ZERO CHARACTER
01C4 E5     CLROW3    PUSH    H           ;SAVE H-L
01C5 1E60             MVI     E,LASTROW   ;POINT D-E TO LASTROW
01C7 1A               LDAX    D
01C8 C601             ADI     001         ;POINT AC TO FIRST ROW OFF SC
01CA FE30             CPI     030         ;CK IF LAST ROW IN RAM
01CC CAD701           JZ      ROZERO
```

Continued on page 5-42

FEATURES

- Keyboard input port
- Serial I/O up to 9600 baud
  - 4k bytes RAM
  - 1k byte ROM
- 2 video pages
- 80 x 24 characters
- 5x7 character font, 7x10 field size
- Block cursor
- Single crystal
- Maximum CPU time/frame without line buffers
- Line or page scroll capability
- Full cursor control
- Complete software flexibility
- Modem control capability
- Low component count
- Field reverse
- Clear screen, clear row, home and clear
- Row swap (row interchange)





Note 1: See DP8350 data sheet for sync details.

Note 2: SW open reverses video page.

Parts:

- 1 — DP8350
- 1 — DP8228
- 1 — DP8224
- 1 — INS8080A-2
- 1 — INS8250
- 8 — MM5257
- 1 — MM2708
- 1 — DM81LS95 or DM81LS96
- 2 — DM74LS32 (V_{CC} 14, 7 GND)
- 1 — DM74LS74 (V_{CC} 14, 7 GND)
- 1 — DM74LS08 (V_{CC} 14, 7 GND)
- 1 — DM74LS04 (V_{CC} 14, 7 GND)
- 1 — DM74LS73 (V_{CC} 14, 11 GND)
- 1 — DM74365
- 1 — DM74148
- 1 — DM7474
- 1 — DP8212
- 1 — DM74LS86
- 1 — DM8678CAB
- 2 — Res. arrays, 3.3k
- 1 — 21.84 MHz Xtal

Bypass capacitors on all parts

```
01CF CD8302 LOOP5   CALL    LDHL1           ;LOAD H,L WITH ADD  OF LASTRO
01D2 CD3B03         CALL    CLROW2
01D5 E1             POP     H               ;RESTORE H,L
01D6 C9             RET
01D7 3E00   ROZERO  MVI     A,000           ;LOAD ROW ZERO
01D9 C2CF01         JMP     LOOP5
                    ;NEXT ROW
01DC 1E60   NXRO1   MVI     E,LASTROW       ;POINT D-E REG TO LAST ROW
01DE 1A             LDAX    D               ;PUT LAST ROW # TO ACC
01DF EB             XCHG                    ;EXCHANGE H-L WITH D-E
01E0 23             INX     H               ;H-L  IS NOW AT 8080 ROW #
01E1 BE             CMP     M               ;COMPARE LAST ROW # WITH
01E2 CA0502         JZ      SCROLL          ;8080 ROW # IF TRUE SCROLL
                    ;INCREMENT 8080 ROW #
01E5 3E2F   INCRO   MVI     A,02F           ;TEST FOR MAX ROW AND
01E7 BE             CMP     M               ;JUMP TO ZERO ROW IF TRUE
01E8 CAFB01         JZ      ZROW            ;ZERO ROW
01EB 34             INR     M               ;INCREMENT THE 8080 ROW #
01EC EB             XCHG                    ;POINT H-L TO CHAR #
01ED 1E61           MVI     E,ROW8080
01EF CD8202         CALL    LDHL
01F2 C9             RET                     ;RETURN
                    ;ZERO CHARACTER
01F3 3E00   ZCHAR   MVI     A,000           ;PUT CHAR # TO ZERO
01F5 32633F         STA     03F63           ;AND STORE
01F8 C3B301         JMP     PCUR            ;GO TO PUT CURSOR ROUTINE
                    ;ZERO 8080 ROW #
01FB 3600   ZROW    MVI     M,000           ;8080 ROW # TO ZERO
01FD 2E00           MVI     L,000           ;N P S  ADDRESS HIGH
01FF 56             MOV     D,M             ;N P S  DATA HIGH TO D REG
0200 2E30           MVI     L,030           ;N P S  ADDRESS LOW
0202 5E             MOV     E,M             ;N P S  DATA LOW TO E REG
0203 EB             XCHG                    ;EXCHANGE H-L WITH D-E
0204 C9             RET                     ;RETURN
                    ;ROW SCROLL
0205 2B     SCROLL  DCX     H               ;POINT H-L TO LAST ROW#
0206 3E2F           MVI     A,02F           ;BEFORE SCRATCH TABLES
0208 BE             CMP     M               ;TEST FOR THE LAST ROW
0209 CA1902         JZ      ZLRO            ;JUMP TO ZERO LAST ROW IF TR
020C 34             INR     M               ;INCREMENT TO NEXT ROW
020D 2E62   ROLO    MVI     L,FIRSTRO       ;POINT H-L TO FIRST ROW#
020F BE             CMP     M               ;IS FIRST LOW = TO LAST ROW
0210 CA1E02         JZ      ZFRO            ;JUMP TO ZERO FIRST R
0213 34             INR     M               ;INCREMENT TO NEXT ROW
0214 2E61           MVI     L,ROW8080       ;POINT H-L TO 8080 ROW
0216 C3E501         JMP     INCRO           ;GO TO INCREMENT ROW ROUTINE
0219 3600   ZLRO    MVI     M,000           ;PUT LAST ROW# TO ZERO
021B C30D02         JMP     ROLO            ;GO TO ROUTINE FOR FIRST ROW
021E 3600   ZFRO    MVI     M,000           ;PUT FIRST ROW# TO ZERO
0220 2E61           MVI     L,ROW8080       ;POINT H-L TO 8080 ROW
0222 C3E501         JMP     INCRO           ;GO TO INCREMENT ROW ROUTINE
                    ;NEW ROW START INTERRUPT
0225 F5     NEWRO   PUSH    PSW             ;SAVE ACC AND FLAGS
0226 E5             PUSH    H               ;SAVE H-L REG
0227 D5             PUSH    D
0228 11643F         LXI     D,03F64         ;POINT D-E TO CRTCROW #
022B 1A             LDAX    D               ;LOAD ACC WITH CRTC ROW #
022C 5F             MOV     E,A             ;N P S  DATA ADD HIGH TO E
022D 1A             LDAX    D               ;ROW DATA HIGH INTO ACC
022E C620           ADI     020
0230 67             MOV     H,A             ;N P S  DATA ADD HIGH INTO H
0231 7B             MOV     A,E
0232 C630           ADI     030             ;ACC TO N P S  DATA LOW
0234 5F             MOV     E,A             ;N P S  DATA ADD LOW TO E REG
0235 1A             LDAX    D               ;ROW DATA LOW TO ACC
0236 6F             MOV     L,A             ;N P S DATA ADD LOW INTO L
0237 3601           MVI     M,001           ;STORE N P S  TO CRTC
0239 D340           OUT     040             ;RESET N P S  AND VERT INTER
023B 1E64           MVI     E,CRTCROW
023D 1A             LDAX    D
023E FE2F           CPI     02F             ;TEST FOR CRTC MAX ROW
0240 CA4A02         JZ      ZCRTC           ;IF TRUE ZERO ACC
0243 3C             INR     A               ;INCREMENT TO NEXT ROW
0244 12     LOOP    STAX    D               ;STORE NEXT ROW NUMBER
0245 D1             POP     D
0246 E1             POP     H               ;RESTORE H-L REG
0247 F1             POP     PSW             ;RESTORE ACC AND FLAGS
0248 FB             EI
0249 C9             RET                     ;RETURN
                    ;ZERO CRTCROW
024A 3E00   ZCRTC   MVI     A,000           ;ZERO ACC
024C C34402         JMP     LOOP
                    ;VERTICAL INTERPUPT
024F F5     VERTI   PUSH    PSW             ;SAVE ACC AND FLAGS
0250 E5             PUSH    H               ;SAVE H REG
0251 D5             PUSH    D
0252 1E62           MVI     E,FIRSTRO       ;POINT D-E TO FIRST ROW #
0254 1A             LDAX    D               ;LOAD 1ST ROW # INTO ACC
0255 1E64           MVI     E,CRTCROW       ;POINT D-E TO CRTCROW #
0257 12             STAX    D               ;UPDATE CRTCROW #
0258 E63F           ANI     03F             ;REMOVE MARKER
025A 5F             MOV     E,A             ;POINT H-L TO CRTC FIRST ROW
025B 1A             LDAX    D
025C C620           ADI     020
025E 67             MOV     H,A
025F 7B             MOV     A,E
0260 C630           ADI     030
0262 5F             MOV     E,A
0263 1A             LDAX    D
0264 6F             MOV     L,A
0265 3602           MVI     M,002           ;STORE TOP OF PAGE
0267 D340           OUT     040
0269 D1             POP     D
026A E1             POP     H
026B F1             POP     PSW             ;RESTORE ACC AND FLAGS
026C FB             EI
026D C9             RET                     ;RETURN

                    ;CARRAGE RETURN
026E 1E63   CR      MVI     E,CHARNUM       ;POINT D-E TO CHAR #
0270 3E00           MVI     A,000
0272 12             STAX    D
0273 1E61           MVI     E,ROW8080
0275 CD8202         CALL    LDHL
0278 C3B301         JMP     PCUR            ;CURSOR TO THE BEGINNING OF R
                    ;SAVE ROW
027B 1E61   SAVPO   MVI     E,ROW8080       ;POINT D-E TO 8080 ROW#
027D 1A             LDAX    D               ;PUT 8080 ROW # TO ACC
027E 1E65           MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE
0280 12             STAX    D               ;STORE ROW SAVE # IN REF TAB
0281 C9             RET                     ;RETURN
                    H-L ROW DATA LOAD ROUTINE
0282 1A     LDHL    LDAX    D               ;LOAD ACC WITH D-E DATA
0283 5F     LDHL1   MOV     E,A             ;POINT D-E TO N P S  DATA HI
0284 1A             LDAX    D               ;ROW # TO N P S  DATA HIGH
0285 67             MOV     H,A             ;ROW # TO H REG
0286 7B             MOV     A,E             ;PUT 1ST ROW # TO ACC
0287 C630           ADI     030             ;ACC TO N P S  ADD LOW
0289 5F             MOV     E,A             ;POINT D-E TO N P S  DATA LOW
028A 1A             LDAX    D               ;ROW # TO N P S DATA LOW
028B 6F             MOV     L,A             ;ROW # TO L REG
028C C9             RET                     ;RETURN
                    ;LINEFEED
028D CDDC01 LF      CALL    NXRO1           ;GO NEXT ROW SUBROUTINE
0290 CDC401         CALL    CLROW3          ;OFF SCREEN CLEAR ROW ROUTINE
0293 1E61           MVI     E,ROW8080       ;MOVE REFERENCE ROW # TO H-L
0295 CD8202         CALL    LDHL            ;LOAD H-L
0298 3A633F ADDCH   LDA     03F63           ;CHAR # TO ACC
029B 85             ADD     L               ;ADD THE CHAR # TO THE
029C 6F             MOV     L,A             ;FIRST ROW ADDRESS
029D 7C             MOV     A,H             ;IF A CARRY OCCURED ADD TO
029E CE00           ACI     000             ;THE DATA HIGH
02A0 67             MOV     H,A             ;H-L POINTS TO LINE FED ROW
02A1 C3B301         JMP     PCUR            ;PUT CURSOR TO LINE FED ROW
                    ;HOME CURSOR TO T O P
02A4 1E62   HOME    MVI     E,FIRSTRO       ;POINT D-E TO 1ST ROW
02A6 1A             LDAX    D               ;STORE FIRSTROW TO ROW8080
02A7 1E61           MVI     E,ROW8080
02A9 12             STAX    D
02AA CD8302         CALL    LDHL1           ;MOVE REFERENCE ROW TO H-L
02AD 3E00           MVI     A,000           ;PUT CHAR # BACK
02AF 32633F         STA     03F63           ;TO ZERO
02B2 C3B301         JMP     PCUR            ;PUT CURSOR HOME
                    ;SWAP ROWS
02B5 1E65   SWAP    MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE # AND
02B7 CD8202         CALL    LDHL            ;PUT IN H-L REG
02BA 22663F         SHLD    03F66           ;STORE ROW SAVE # TO TEMP 1 *
02BD 1E61           MVI     E,ROW8080       ;POINT D-E TO 8080 ROW # AND
02BF CD8202         CALL    LDHL            ;PUT ADDRESS IN H-L REG
02C2 1E65           MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE # AND
02C4 1A             LDAX    D               ;PUT IN ACC
02C5 5F             MOV     E,A             ;8080 ROW # TO ADD HIGH
02C6 7C             MOV     A,H             ;STORE 8080 ROW # TO N P S
02C7 12             STAX    D               ;DATA HIGH
02C8 7B             MOV     A,E
02C9 C630           ADI     030
02CB 5F             MOV     E,A             ;PUT 8080 ROW # TO
02CC 7D             MOV     A,L             ;N P S  DATA LOW
02CD 12             STAX    D               ;8080 ROW # IS NOW IN ROW SA
02CE 24663F         LHLD    03F66           ;PUT ROW SAVE # BACK TO H-L
02D1 1E61           MVI     E,ROW8080       ;COMENT SAME AS ABOVE
02D3 1A             LDAX    D
02D4 5F             MOV     E,A
02D5 7C             MOV     A,H
02D6 12             STAX    D
02D7 7B             MOV     A,E
02D8 C630           ADI     030
02DA 5F             MOV     E,A
02DB 7D             MOV     A,L
02DC 12             STAX    D
02DD C39802         JMP     ADDCH           ;JUMP TO ADD CHAR
                    ;BACK SPACE
02E0 1E63   BS      MVI     E,CHARNUM       ;POINT THE D-E REG TO CHAR #
02E2 1A             LDAX    D               ;AND PUT IN ACC
02E3 FE00           CPI     000             ;TEST FOR THE CHAR # =
02E5 CAEE02         JZ      UPROW           ;TO ZERO  JUMP IF TRUE
02E8 3D             DCR     A               ;DECREMENT CHAR #
02E9 12             STAX    D               ;STORE DECREMENTED CHAR #
02EA 2B             DCX     H               ;DEC H-L FOR NEW CURSOR LOCA
02EB C3B301         JMP     PCUR            ;PUT CURSOR IN DECREMENTED LO
                    ;NEXT ROW UP
02EE 3E4F   UPROW   MVI     A,04F           ;MOVE THE CHAR #
02F0 12             STAX    D               ;TO ROW AND STORE IT
                    ;MOVE CURSOR UP
02F1 EB     UPCUR   XCHG                    ;POINT H-L TO 8080 ROW AND D-
02F2 2E61           MVI     L,ROW8080       ;TO NEW CURSOR LOCATION
02F4 7E             MOV     A,M             ;TEST IF NEXT UP CURSOR WILL
02F5 23             INX     H               ;BE ON THE FIRST ROW
02F6 BE             CMP     M               ;IF TRUE JUMP TO
02F7 CA0803         JZ      UPSCL           ;UP SCROLL ROUTINE
02FA 2B             DCX     H               ;POINT H-L BACK TO 8080 ROW #
02FB FE00   BACK1   CPI     000             ;IF 8080 ROW # IS EQUAL TO
02FD CA1E03         JZ      BR48            ;ZERO JUMP TO ROW 48 ROUTINE
0300 3E             DCR     M               ;DECREMENT 8080 ROW #
0301 EB     LOOP1   XCHG                    ;POINT H-L TO NEW CURSOR LOCA
0302 CD8202         CALL    LDHL            ;AND D-E TO 8080 ROW #  JUMP
0305 C39802         JMP     ADDCH           ;TO ADD CHARACTER ROUTINE
0308 7E     UPSCL   MOV     A,M             ;PUT FIRST ROW # INTO ACC
0309 FE00           CPI     000             ;TEST IF FIRST ROW # IS = TO
030B CA2403         JZ      FR048           ;ZERO  IF TRUE JUMP TO ROW
030E 35             DCR     M               ;48 ROUTINE
030F 2E60   LOOP2   MVI     L,LASTROW
0311 7E             MOV     A,M
0312 FE00           CPI     000
0314 CA2A03         JZ      LR048
0317 35             DCR     M
0318 2E61   LOOP3   MVI     L,ROW8080       ;POINT H-L TO 8080 ROW #
031A 7E             MOV     A,M             ;AND LOAD TO ACC
031E C3FE02         JMP     BACK1
```

```
534 031E 3E2F   R048    MVI     A,02F           ;CHANGE 8080 ROW #
535 0320 77             MOV     M,A             ;TO 23D AND STORE
536 0321 C30103         JMP     LOOP1           ,JUMP TO POINTER EXCHANGE ROU
537
538 0324 3E2F   FR048   MVI     A,02F
539 0326 77             MOV     M,A
540 0327 C30F03         JMP     LOOP2
541
542 032A 3E2F   LR048   MVI     A,02F           ,PUT THE 1ST ROW TO
543 032C 77             MOV     M,A             ,17H
544 032D C31803         JMP     LOOP3           ,JUMP TO 8080 ROW # STORE
545
546                     ;CLEAR ROW ROUTINE
547
548 0330 CD3603 CLROW.  CALL    CLROW1
549 0333 C36E02         JMP     CR
550
551 0336 1E61   CLROW1  MVI     E,ROW8080
552 0338 CD8202         CALL    LDHL            ,PUT ROW DATA IN H-L REG
553 033B 3E50   CLROW2  MVI     A,050           ,INTILIZE LOOP COUNTER.
554 033D 3620   LOOP4   MVI     M,020           ,STORE ASCII SPACE IN MEM
555 033F 3D             DCR     A               ,DECREMENT LOOP COUNTER.
556 0340 C8             RZ                      ,RETURN IF ZERO BIT IS SET
557 0341 23             INX     H               ,NEXT LOCATION
558 0342 C33D03         JMP     LOOP4           ,CLEAR NEXT LOCATION.
559
560 0345 D301   BELL.   OUT     001             ,RING BELL
561 0347 C9             RET
562
563 0348 AF     IVERTN  XRA     A
564 0349 1E68           MVI     E,IMASK         ,POINT D,E TO MASK
565 034B 1A             LDAX    D
566 034C 17             RAL                     ,CK BIT 8 STATUS
567 034D DA5203         JC      RESET
568 0350 3E80           MVI     A,080           ,INVERT BIT 8
569 0352 12     RESET   STAX    D               ,STORE OUT NEW MASK
570 0353 C9             RET
571
572 0354 E5     IVERTR  PUSH    H
573 0355 1E61           MVI     E,ROW8080
574 0357 CD8202         CALL    LDHL            ,LOAD 1ST ADD  OF 8080ROW TO
575 035A 1E50           MVI     E,050           ,SET COUNTER
576 035C 7E     LOOP6   MOV     A,M             ,GET CHAR
577 035D 17             RAL                     ,CK BIT 8 STATUS AND INVERT
578 035E DA7003         JC      RESET1
579 0361 1F             RAR
580 0362 F680           ORI     080             ,MASK BIT 8 HIGH
581 0364 77     BACK2   MOV     M,A             ,STORE MOD  CHAR TO MEM
582 0365 23             INX     H               ,POINT TO NEXT MEM
583 0366 7B             MOV     A,E
584 0367 FE01           CPI     001
585 0369 CA7603         JZ      DONE            ,RETURN IF COUNT = ZERO
586 036C 1D             DCR     E               ,DEC  COUNTER
587 036D C35C03         JMP     LOOP6
588
589 0370 1F     RESET1  RAR
590 0371 E67F           ANI     07F             ,RESET BIT 8
591 0373 C36403         JMP     BACK2
592
593 0376 E1     DONE    POP     H
594 0377 C9             RET
595      0000            END     START
```

```
A       0007    ACELD   011C    ADCUR   0161    ADDCH   0298
B       0000    B110    00D4    B1200   00EC    B150    00DA
B1800   00F2    B2000   00F8    B2400   00FE    B300    00E0
B3600   0104    B4800   010A    B600    00E6    B7200   0110
B9600   0116    BACK    0083    BACK1   02FB    BACK2   0364
BAUD    0093    BELL    0345    BS      02E0    C       0001
CHARNU  0063    CLRAM   0042    CLRAM1  004C    CLROW   0330
CLROW1  0336    CLROW2  033B    CLROW3  01C4    CR      026E
CRTCRO  0064    D       0002    DONE    0376    E       0003
FIRSTR  0062    FR048   0324    FUNC    0170    H       0004
HMCUR   0087    HOME    02A4    IMASK   0068    INCRO   01E5
INIT    003B    INTACE  014A    INTKB   0136    IVERTN  0348
IVERTR  0354    L       0005    LASTRO  0060    LDHL    0282
LDHL1   0283    LF      028D    LOOP    0244    LOOP1   0301
LOOP2   030F    LOOP3   0318    LOOP4   033D    LOOP5   01CF
LOOP6   035C    LR048   032A    M       0006    NEWRO   0225
NRS     0061    NXRO    01BE    NXRO1   01DC    PCUR    01B3
PSW     0006    RESET   0352    RESET1  0370    R048    031E
ROLO    020D    ROW808  0061    ROWSAV  0065    ROZERO  01D7
SAVRO   027B    SCROLL  0205    SP      0006    START   0000
SWAP    02B5    TEMP1   0066 *  TEMP2   0067 *  UPCUR   02F1
UPROW   02EE    UPSCL   0308    VERTI   024F    ZCHAR   01F3
ZCRTC   024A    ZFRO    021E    ZLRO    0219    ZROW    01FB

 NO ERROR LINES
SOURCE CHECKSUM = 403F
OBJECT CHECKSUM = 0F51
INPUT FILE    1 CRT80A SRC ON JIMFM
OBJECT FILE   1 CRT80A LM ON JIMFM
```


DEFINITIONS

ACE – Asynchronous communication element
CRTC – Cathode ray tube controller
Video Page – Visible screen data
Video RAM – Entire portion of RAM used only for display
First Row # – Address for top row of video page
Last Row # – Address for bottom row of video page
CRTC Row # – Address for next row load
8080 Row # – Address for cursor row
Character # – Character location in a row
XXXH are hexidecimal numbers

REFERENCES

National Semiconductor Data Sheets:

DP8350 Series Programmable CRT Controllers
INS8250 Asynchronous Communications Element
DM8678 Bipolar Character Generator
INS8080 Assembly and Reference Manuals

National Semiconductor Application Notes:

Simplify CRT Terminal Design with the DP8350, AN-198

DM8678 Bipolar Character Generator, AN-167

Data Bus and Differential Line Drivers and Receivers, AN-83

Transmission Line Characteristics, AN-108

Hardware Reference Manual BLC 80/10 Board Level Computer. National Semiconductor Microcomputer Systems Chapter 6 – System Interfacing.

Graphics Using the DP8350 Series of CRT Controllers

National Semiconductor
Application Note 212
Charles Carinalli
December 1978

The DP8350 CRT Controller series is a versatile building block for both low and high-end CRT terminal applications. This application note demonstrates how the DP8350 may be used in CRT graphics applications. Although this presentation is general, when specific examples are given the DP8350 ROM programmed version of the DP8350 series will be used (80 characters per row, 24 character rows, 5 x 7 character, 7 x 10 character field size).

BACKGROUND INFORMATION

The basic function of the DP8350 CRT controller is to control the elements of the "video loop" *(Figure 1).* A memory address generated by the CRT controller is presented to the CRT memory, which stores a record of what appears on the CRT display. The character generator converts this stored information into serial video data to the CRT monitor. The intensity of the CRT electron beam is modulated by this video data and its position is controlled by the horizontal and vertical sync pulses generated by the CRT controller.

The CRT screen video area is divided into character cells *(Figure 2).* Each cell has a unique CRT memory address. The DP8350 must present the correct character cell address to the CRT memory at the appropriate CRT beam location. Use of the line counter outputs of the DP8350 make possible the subdivision of each character cell address into the unique scan line of the present CRT beam location.

For the DP8350 and its unique internal ROM program format, each character cell is composed of 70 dots (7 dots wide and 10 dots high) *Figure 3.* When using the DP8350, each of these dots may be active video data. Typically however, in alphanumeric display systems, the character generator will provide cell to cell character spacing on the CRT screen by blanking some number of rows and columns of dots. That is why the DP8350's 7 x 10 dot field is used with a 5 x 7 character generator (2 horizontal and 3 vertical dot spaces).

In fact, it is the character generator that restricts the use of the full character cell dot field, not the DP8350! Using a character generator which allows video on every scan line and all dots of the cell width, makes graphic capability possible. This type of graphic display generation is called "character generator graphics."

All of the dots on the CRT display may also be independently controlled by a separate CRT memory address location; this is called "memory mapped graphics."

Both of these graphics display generation techniques will be discussed here, with demonstrations of how the DP8350 series may be used to reduce total component count.

CHARACTER GENERATOR GRAPHICS

In this graphics system *(Figure 4)* the character generator block contains a ROM that has been programmed with graphic symbols whose size is contained within the character cell size. This ROM may at the same time contain alphanumeric characters that do not use the full character cell size.

The block representation and operation of this system is the same as the alphanumeric's system previously described. The CRT memory presents the same character cell data to the character generator on every scan line of that character cell address. The character generator ROM is organized with addresses defining a particular symbol and addresses defining which scan line of a character row the CRT electron beam is currently on; thus defining the video data for that scan line of the symbol. The scan line address data comes directly from the DP8350. The parallel data that results is video data for that screen address cell width. This data is then serially shifted to the CRT monitor with a parallel to serial shift register.

This system allows every scan line of a character row to have active video information; thus the graphics symbol may be programmed to all sides of the character cell providing continuity from cell to cell both horizontally and vertically. At the same time, the alphanumeric's character may be programmed with cell to cell spacing.

Character generator graphics is the simplest most cost-effective approach to CRT graphics. It requires a minimum of software development and hardware support. The DP8350 CRT controller provides all the required timing and control pulses for the CRT memory, character generator, and CRT monitor.

Graphics capability with this system, however, is somewhat limited since individual dot control is not possible; only character cell symbol control is available. This system does apply well in such applications as bar graphs, circuit schematics, or flow charts and when these need to be combined with alphanumeric data.

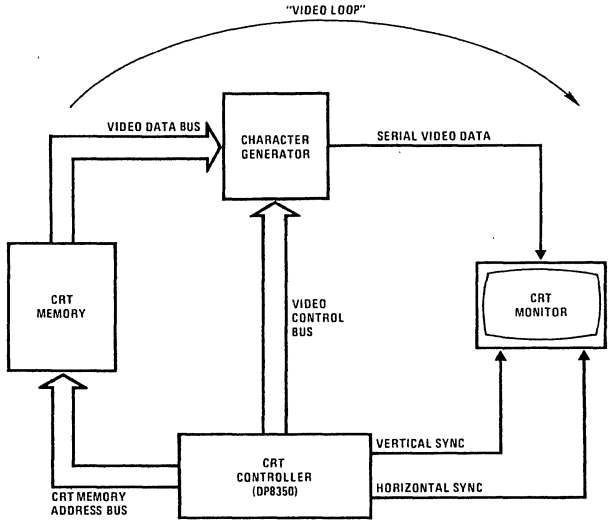


FIGURE 1. Elements of the "Video Loop"

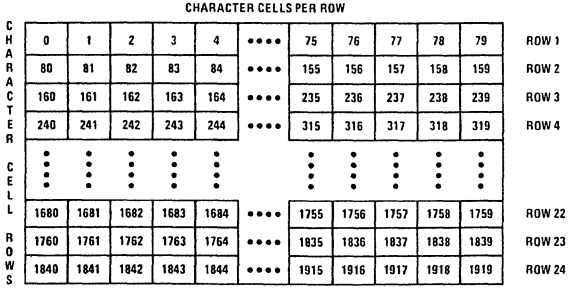


FIGURE 2. CRT Screen Cell Address Map Presented to CRT Memory by the DP8350 (Top of Page Register Contains Address 0) Character Cells Per Row = 80 Character Rows Per Frame = 24

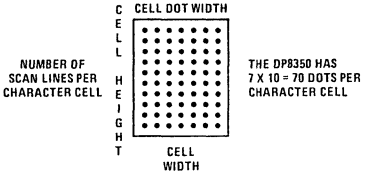


FIGURE 3. The DP8350 Character Cell is 7 Dots Wide and 10 Dots High

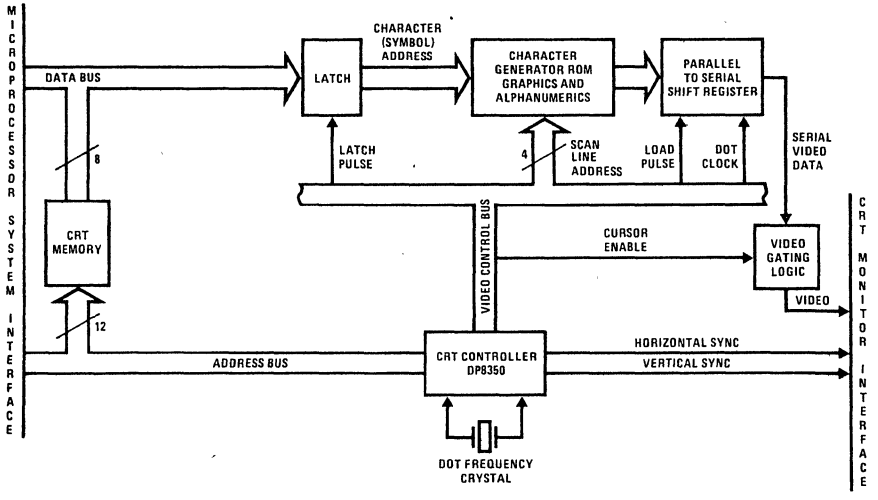


FIGURE 4. Character Generator Graphics

CHARACTER GENERATOR GRAPHICS—WITH LINE BUFFERS

Modification of the character generator graphics block diagram is possible with the addition of a recirculating line buffer placed between the CRT memory and the character generator *(Figure 5)*. In this case the character generator addresses for a character row are loaded serially into this shift register on the scan line before the first video scan line of a character row. These addresses are then recirculated for the number of scan lines per character row minus one (then the next character row of addresses is loaded). This system allows access to the CRT memory by the system controller on all but one scan line of a video character row. In contrast, the system previously described would have allowed access only during blanking intervals. In systems that require heavy access to the CRT memory to update screen information, this approach is very attractive.

In this case, as before, all the required control pulses for the "video loop" are provided by the DP8350 CRT controller.

MEMORY MAPPED GRAPHICS

If a very high resolution graphics display is required, every dot of the CRT display may be independently controlled. In this case, every dot of the CRT screen may be mapped to a specific CRT memory data bit—thus the name Memory Mapped Graphics. This type of system is obviously a more costly type of graphics, since to control every dot not only is there a need for more CRT memory, but the microprocessor overhead in such a system will be greater—both software and hardware. In any case, the DP8350 easily adapts to such a system as demonstrated in *Figure 6*.

In this approach, if you subdivide each character cell such that each scan line of the cell may be independently addressed, then from the CRT memory block instead of 8 bits of data defining a character cell code to the character generator, you get 8 bits of direct video data. Then the CRT memory block serves double duty—CRT memory storage and symbol or character generator. All that is left to do is convert this parallel video data to serial video data as before.

In the case of the DP8350 internal ROM format program, each cell is 7 dots wide; thus only 7 bits of video data are needed per character cell/scan line address. The DP8350 addresses the memory block as before with the character cell address, but in this case also with the scan line address. In this manner, the DP8350 series has a maximum address capability of 16 bits (64k).

VARIATIONS

If memory mapped graphics is desirable but standard alphanumerics is also required, combination of these techniques is possible. For example, if only a small portion of the CRT screen need be memory mapped and the remainder can be character generator alphanumerics and/or graphic symbols. In this case a higher order data bit from CRT memory defines whether the lower order data bits are graphics video data or ASCII and graphics symbol code. *Figure 7* is a block diagram of such a system.

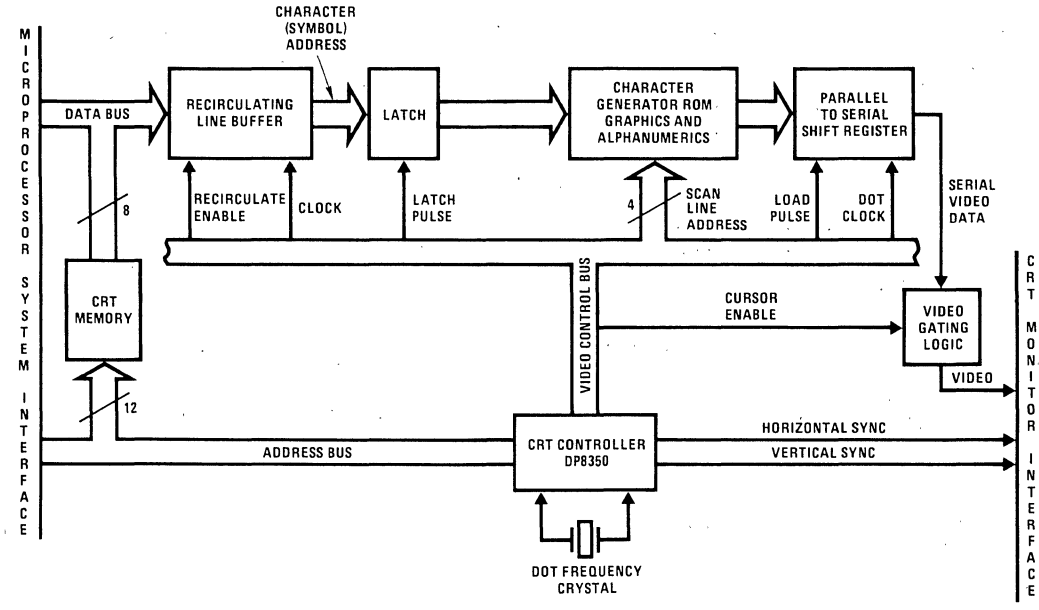


FIGURE 5. Character Generator Graphics (With Line Buffer)

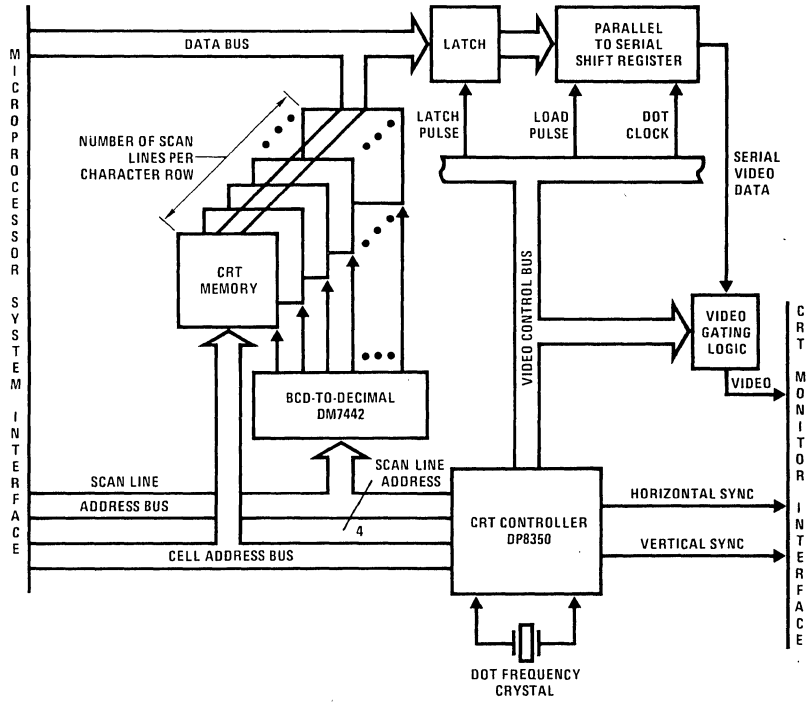


FIGURE 6. Dot by Dot (Memory Mapped) Graphics

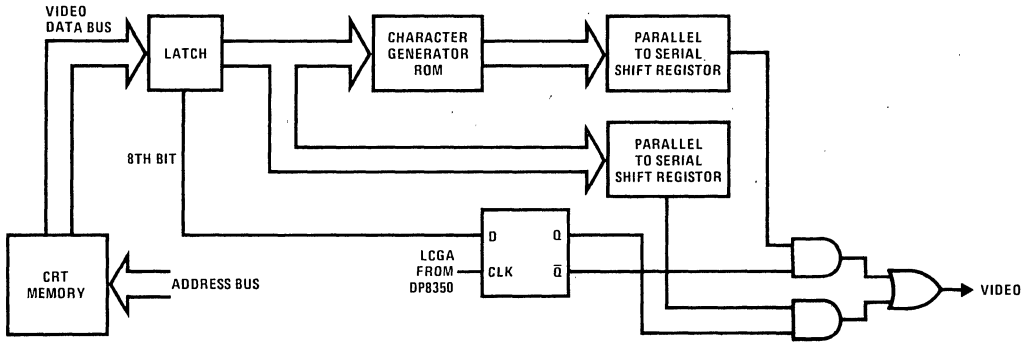


FIGURE 7. Combined Character Generator and Memory Mapped Graphics.

SUMMARY

This application note has demonstrated 2 basic graphics techniques that may be implemented using the DP8350 CRT controller. Variations to these techniques are possible such as changing character cell sizes and subdividing the character cell into dot blocks. In most cases, these variations are done to decrease hardware or software overhead. Since the DP8350 series of CRT controllers offer display format flexibility through internal ROM program variations—the device adapts equally well to these graphics variations as it does to the standard applications.

The fact that all the required control functions for the "video loop" are contained within the same chip—the DP8350—makes it very effective in these types of applications; as a result it will produce the minimum chip count and cost.

Graphics/ Alphanumerics Systems Using the DP8350

National Semiconductor
Application Note 243
Mike Evans
April 1980

This application note summarizes some CRT terminal circuits, each with an increasing degree of graphics capability, and then goes into detail to describe a system having full graphics capability, with all dots individually programmable. All these applications use the DP8350 CRT Controller.

Here are some of the features of the full graphics system.

Hardware Features

- The hardware is designed for a 24 row by 80 column display, with 7 dots per column and 10 lines per row
- All ICs are made by National Semiconductor
- Low I.C. cost, all parts readily available
- Fits on one standard BLC80 (SBC80) card
- System performance only limited by software
- 8080 Mnemonics — useable with STARPLEX or Intellec Development Systems
- All graphics programs very fast
  Example: One dot takes 500μs maximum to plot
- During display time, each 7-dot cycle may be shared by the microprocessor
- 8 bit word comprises MSB as attribute and next 7 bits as 7 dot word of a character line
- Can input display data serially or parallel
- Can output display data serially or parallel
- Baud rate programmable from 110 to 56k baud
- Can be used as slave to main system
- Can copy characters from alphanumeric ROM or symbol EPROM
- 13k bytes of RAM available for user software or back-up display storage
- Analog inputs — joystick or waveforms
- Easily expandable to color graphics

Software Features

- The software is programmed for any display configuration of rows, columns, dots per column and lines per row. The hardware is designed for a 24 row by 80 column display, with 7 dots per column and 10 lines per row.
- Can perform most dumb terminal functions, including scrolling
- Simultaneous display of alphanumerics and graphics
- Identical terminals can display same information with inputs from either
- Can save displays in computer storage
- Can load displays from computer storage
- Can erase any part of display or all of it
- Can draw a rectangle linking any 2 horizontal and 2 vertical coordinates
- Can transfer in 1/10th second max any area of display to any other area or to/from back-up display storage
- Smooth movement of subject in any direction
- Immediate display of fixed diagrams
- In-system emulation of programs available

The DP8350 CRT Controller provides incrementing video addresses starting from the Top of Page address, or from a new Row Start address. These addresses and the Cursor address are loaded into their respective registers from the address bus. All video control signals are provided by the 8350, so that apart from the crystal oscillator, no extra video circuitry is required.

The DP8350 has so far been considered to be useable only in dumb terminals, whereas in fact is is easy to adapt it to more complex terminals with full graphics capability. Following is a summary of the functions of the various combinations of alphanumerics/graphics displays beginning with a dumb terminal using a monitor with 24 × 80 characters.

Dumb Terminal

The basic dumb terminal design is shown in Figure 1. Usually the microprocessor loads the Character Position RAM (or Refresh RAM) only during horizontal or vertical blanking, or during the last 3 lines of a row. The CRTC then sequentially addresses this RAM during display time. The ASCII data from this RAM (for the character selected) is outputted to the ROM of the Character Generator. The 7-dot word of this character for the line being displayed is then loaded into a shift register, and shifted out as video to the monitor during the next 7-dot cycle. The ROM, line counter and shift register can be one IC, such as the DM8678 DAB Character Generator, which contains all ASCII upper case characters.

The logical choice of CRT Controller for this simple CRT terminal is the DP8350, which mates perfectly with the DM8678. The most common application is for a 24 row by 80 column display with the character field comprising of 10 lines each of 7 dots. The character itself occupies 7 lines each of 5 dots, leaving 3 lines for vertical character spacing, and 2 dots for horizontal character spacing.

Refer to AN198 and AN199 for further information on alphanumeric applications of CRTs.

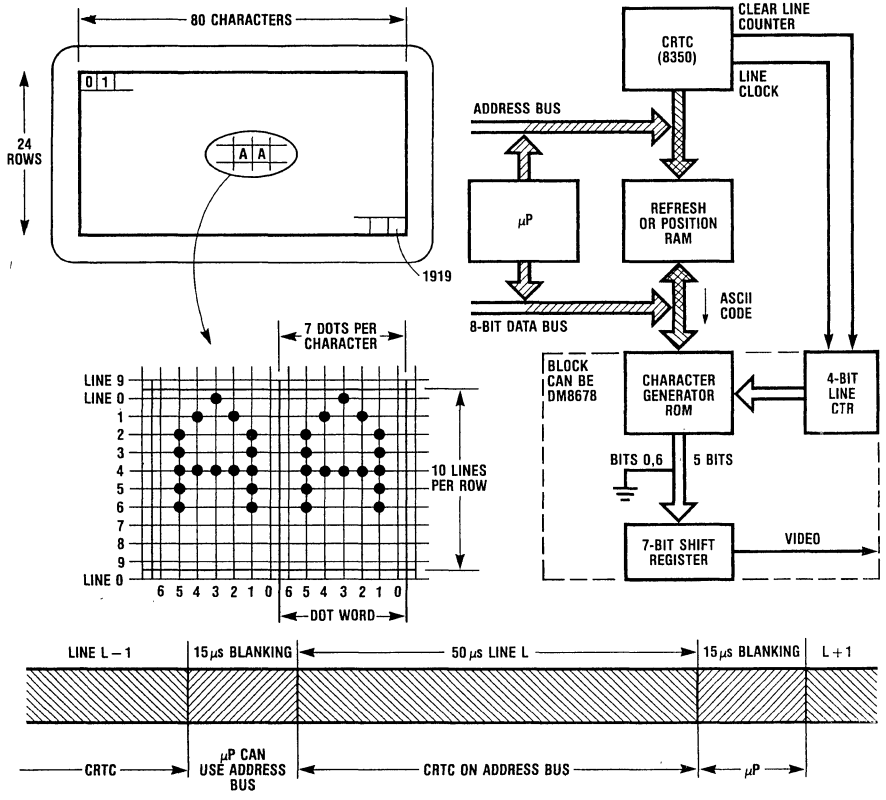


Figure 1. Simplest CRT Terminal

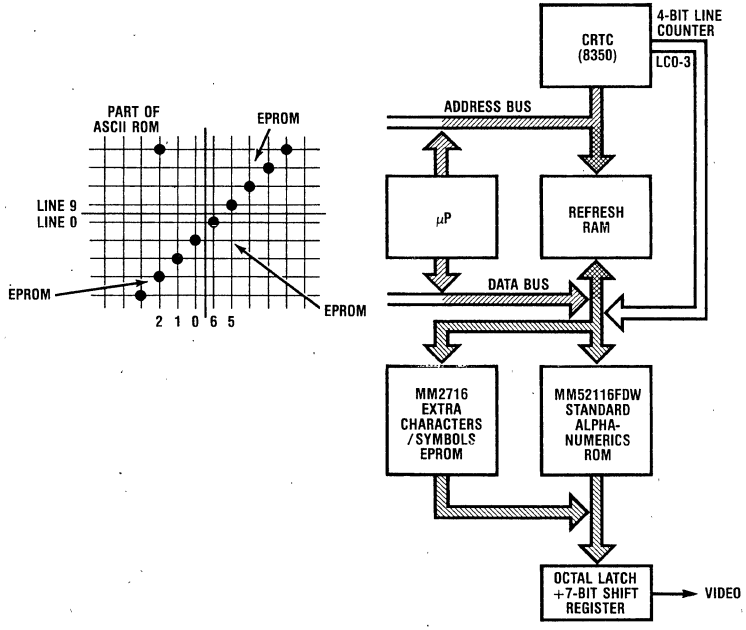
Disadvantages for Graphics

- Only characters in the Character Generator ROM can be selected
- Characters not continuous to adjacent fields
- Microprocessor thru-put 30% of maximum — not desirable for graphics

Alphanumeric Characters with Extra Symbols

When characters or symbols are required that are different from those in the ROM, then an extra EPROM such as the MM2716 can be added as shown in Figure 2. The standard characters can be selected from a separate ROM such as the MM52116FDW which contains all 128 standard ASCII characters. The EPROM is preprogrammed with additional characters or symbols. The 8350 outputs sequential addresses to the Refresh RAM, and each address is two dot cycles ahead of the shifting dot word.

The data out from the RAM must be valid 150ns after each address change. The MSB of the data selects ROM or EPROM, and the remaining 7 bits select the character. The line of the character is decoded from the 4-bit line counter outputs coming from the 8350. The ROM/EPROM now has 640-150ns (>450ns) to output the valid dot word. This has to be latched into an octal latch and held for one dot cycle before it can be loaded into the 7-bit shift register. The dots are then shifted out in the dot cycle.



Refresh RAM MSB:

0 selects alphanumeric ROM

1 selects symbol EPROM

Figure 2. Fixed Character ROM + Symbol EPROM

Disadvantages For Graphics

- Fixed graphics possible with continuous display, but limited to 128 different characters, and 128 standard alphanumerics, for all 1920 positions.
- Also it is not possible to change characters/symbols once the EPROM has been programmed.
- The Microprocessor is still slow thru-put.

Limited Graphics Terminal

To be able to generate *any* graphics symbol, a character RAM must replace the fixed ROM characters. Characters or symbols can be loaded into the RAM as required from a ROM or a pre-programmed EPROM like the MM2716 (refer to Figure 3). But now, new graphics characters can be written into the RAM from the Microprocessor. These can either be derived internally from the μP or obtained directly from peripherals (such as serially to an Asynchronous Communications Element like the INS8250, or parallel from an external I/O port).

This limited graphics application thus requires two RAMs, the Refresh RAM (or Character Position RAM), and the Character RAM. The Refresh RAM outputs the selected character address, and the 8350 line counter outputs select the line in the Character RAM. The 7 dots outputted from this RAM are latched into the Octal Latch and held for one dot cycle. The 8th bit of data can be used as an attribute control bit. The 7 LSBs are then loaded into the 7-bit shift register.

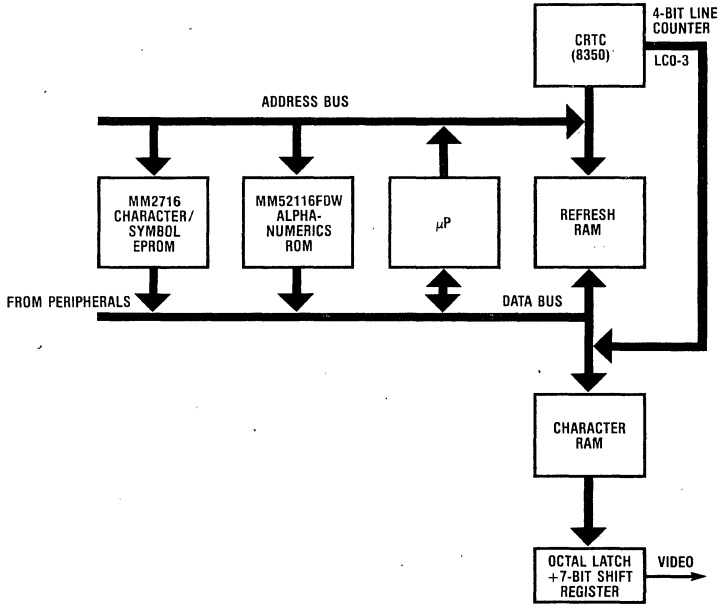


Figure 3. Character RAM with ROM/EPROM Look-Up

Disadvantage for Graphics

- Only 256 possible characters per display, with the 8-bit data bus, but can re-load different characters for a new frame.

Advantages

- Can now load standard characters or symbols from EPROM, either at switch-on or during normal running.
- Can also load characters/symbols/graphics from the μP or peripherals, e.g., to create graphics drawings to connect to adjacent positions.
- Can now be a very fast system — by isolating the μP address bus from the CRTC address bus, the μP can share the dot cycle with CRTC.
- Refresh RAM and character RAM can be made the same IC by using one 8k x 8 quasistatic RAM.

With the new 8k x 8 quasistatic RAMs such as the NMC4864, the first quarter can be used as a Refresh RAM for the 1920 character positions. The RAM data outputs containing the character address can then be latched into an octal tri-state latch. If the 8350 address bus is then disabled, the octal tri-state latch can feed back to the RAM second half address inputs, along with the enabled 8350 line counter outputs. The data out from the RAM now contains the next 7-dot word to be displayed and this is then loaded into the shift register. This takes the last two thirds of the dot cycle, the first third is for the μP. With the fast cycle time of the quasistatic RAMs this 3 part cycle can easily be accomplished in one 7-dot cycle. (Refer to Figure 4.)

With the method just described it is only possible to display 256 different characters for any one page, because each character consists of 10 lines, almost filling the second half of the quasistatic RAM. If this is acceptable, then a limited graphics terminal can be easily implemented using a microprocessor, with one MM2716 instruction set EPROM, one MM52116FDW character ROM, one MM2716 symbol EPROM, one DP8350 CRT Controller, the NMC4864 quasistatic RAM, and a DM74166 shift register. The logic and drive circuitry required to control the sequencing comprises a further 15 SSI ICs. This application has not yet been built, awaiting availability of the quasistatic RAMs.

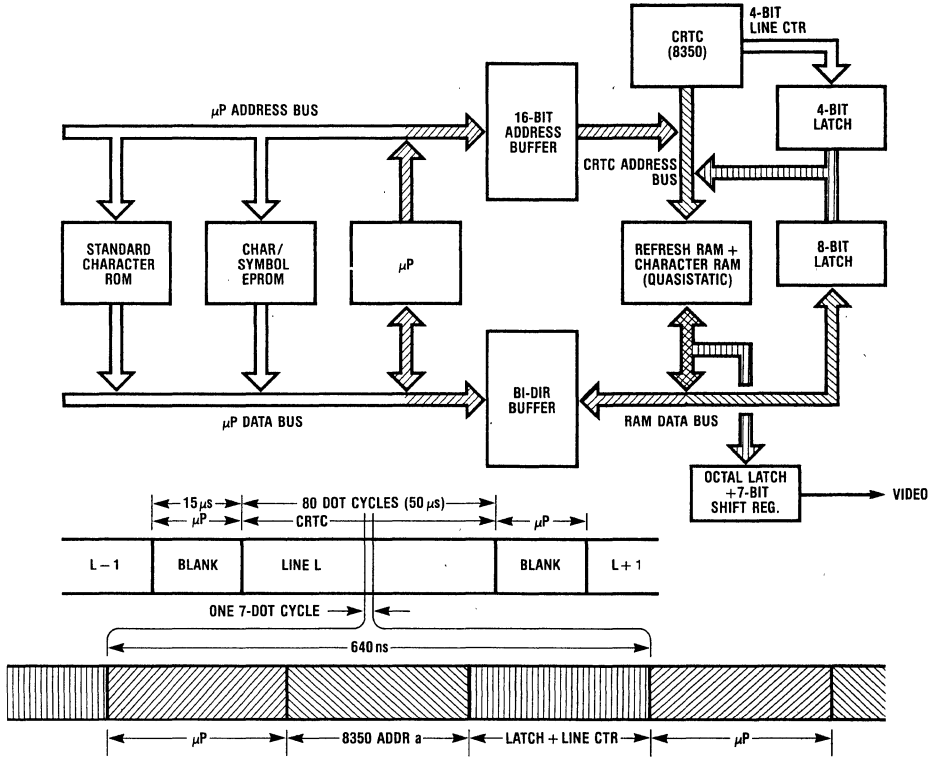


Figure 4. Limited Graphics Using a Buffered CRTC Address Bus and a Quasistatic RAM

Advantages

- **Only one IC, an 8k x 8 quasistatic RAM, used for both the refresh RAM and character RAM**
- **Fast, although μP may be in the wait state for a maximum of 600ns. This is no problem because the fastest μP instruction cycle is 1μs, so there will be no effect on maximum thru-put.**

Disadvantages

- **No quasistatics available at the time of writing**
- **Full graphics capability not possible**

Full Graphics Capability

We need to be able to select any dot on the display, for full graphics capability, while still using the CRT controller to sequence every line of every row, as it does in the simple terminal (See Figure 5).

With the standard 24 × 80 character display, full graphics can be achieved by using a 24 (rows) by 80 (columns) by 10 (lines) address RAM, and selecting the 7 dots as the data word for the character position on the display and the line of that character position.

This means that alphanumeric characters can be displayed in exactly the same format as with a simple terminal, by copying the character from ROM or EPROM into the selected 10 line by 7-dot field, line by line.

Full graphics capability is also easily implemented once the relevant software algorithms have been determined.

So for full graphics, every dot is one bit of memory. There is no refresh RAM, refer to Figure 6. The CRTC scans through the Display RAM, a line at a time for each row on the CRT, causing the RAM outputs to be read every 7 dot cycle. The RAM output is shifted out two dot cycles later. The microprocessor may write into the Display RAM each 7-dot word, with "1's" representing dots.

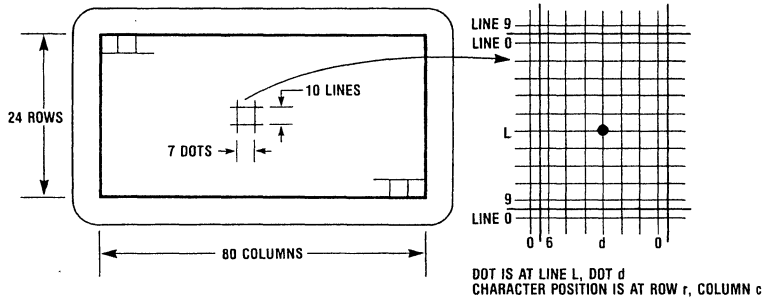


Figure 5. Full Graphics Capability Requires Individual Dot Selection

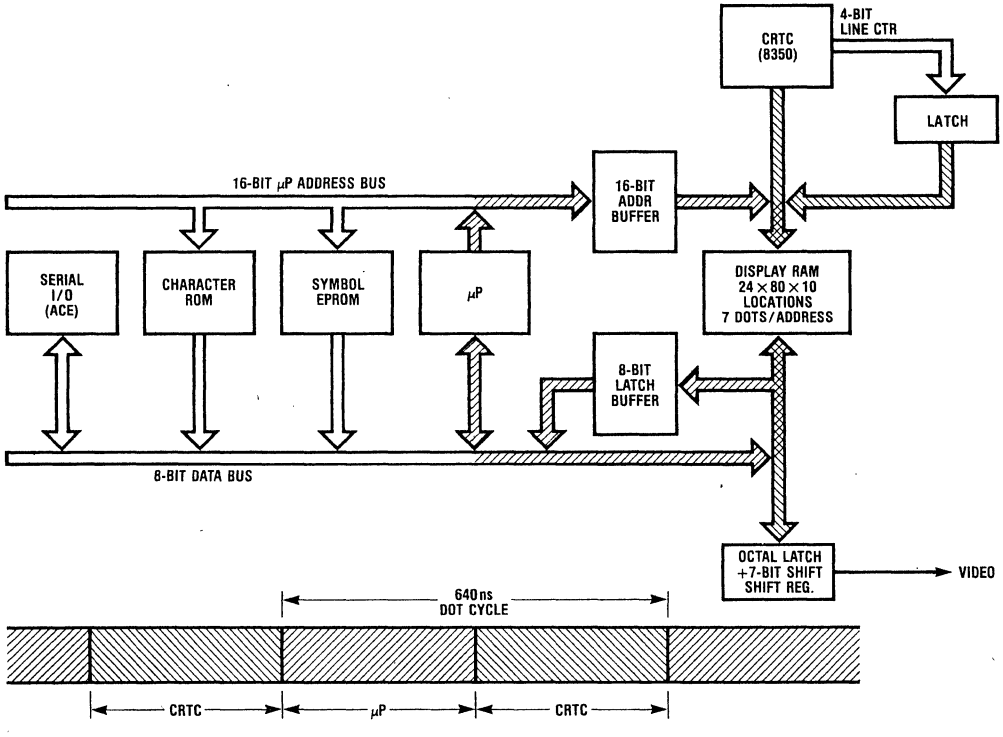


Figure 6. Full Graphics System

CRTC Address Bus Configuration

The particular RAM address to be written into is determined by its 10 x 7 character field position and the selected line of that field; refer to Figure 7.

The 11 least significant addresses A_0 to A_{10} contain character position information from position 0 to 1919, and the next 4 addresses A_{11} to A_{14} are the 8350 line counter outputs via a tri-state buffer. The most significant bit, A_{15} is used to select the RAM when HI, and the EPROMs and peripherals when LO

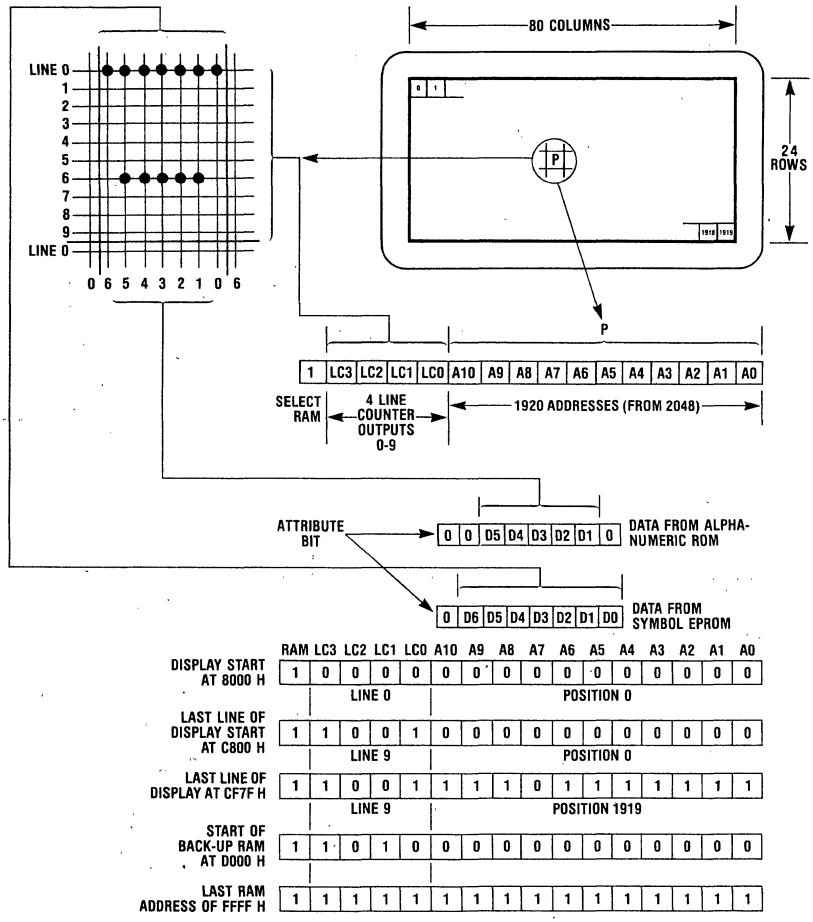


Figure 7. RAM Addressing

Graphics Design Criteria

In the simple CRT applications, the microprocessor is used mainly to re-write the Refresh RAM as new information is fed in, either from the keyboard, or from the main computer (via ACE). The μP can still be used in this application for alphanumerics/graphics, but it is also desirable if it can perform graphics computations, such as drawing lines from the inputted coordinates.

This requires the microprocessor to be able to write 7 dot words quickly to the Display RAM. The best way to implement this is to time multiplex the dot cycle with the CRTC so that whenever the μP requires access to the Display RAM, it merely waits for its slot in the next dot cycle, which could be up to 640ns later. The information is either written or read after 360ns, that is a maximum of 1μs after the memory access request, which is fast enough. Now the μP no longer has to wait for blanking to be able to operate, it continues its normal operation and only enters the WAIT state during RAM access. Although this is for up to 1μs, in fact it is in general invisible because the μP memory access takes at least 700ns.

The Microprocessor

The 8080A-2 was chosen for the following reasons:

- FAST — takes 21.84 MHz (2 × 8350 frequency) divided by 9 (in the 8224), to give a clock cycle of 2.427 MHz, i.e., 0.41μs per microcycle, or 1.6μs for a short instruction
- Software can be developed on STARPLEX™ or Intellec Development Systems
- INS8080A-2, DP8224 and DP8238 are low cost and available from National
- Associated circuitry previously designed in Application Note AN199

Note the DP8238 has advanced MEMW mode — desirable so that the microprocessor can go into the WAIT state earlier in the write cycle.

Interrupts

The INS8259 is ideal as as an Interrupt Controller, because most interrupt signals in the system are positive going, saving D-type flip-flops. It can also be used to mask off interrupts when necessary.

Interrupt Priority

1) *Horizontal Sync* from the 8350, highest priority if row start has to be quickly changed, normally masked off
2) *Paralleled 8-Bit I/O Port*, highest priority if CRTC card is part of a master system, otherwise masked off
3) *Vertical Sync* from the 8350, normally highest priority, need to quickly change the Top of Page register for scrolling, to change the display before the new frame begins
4) *ACE*, INS8250 — during serial block transfers this will take highest priority
5) *Keyboard* — the time to press the keys is much longer than the interrupt wait time so can be low priority
6) *A/D Converter* — time for conversion is 100μs so again can be low priority

Display RAM

The system requires a RAM with 24 × 80 × 10 addresses, each of 8 bits (representing 7 dots + 1 attribute bit), and a cycle time of 640ns/2 or 320ns. Using static RAMs 19.2k bytes would require 40 ICs, whereas using dynamic RAMs 16 ICs are necessary, totalling 32k bytes. This leaves 13k bytes available as spare RAM.

Advantages of Dynamic RAMs

- Only 16, 16-pin packages instead of 40, 18-pin packages
- Less than $10 for 16,000 bits
- Fast access and cycle times using the MM5290-2 (average cycle time is 320ns). Even faster times with the 5V only 16k MM5295
- Standby current only 5% of operating current
- Less average power dissipation than for static RAMs

This means average power dissipation is 30mA × 12V × ½ × ½ × 16 or 1.5W for all 16 packages (only one bank is accessed per cycle by the CRTC for half the dot cycle time). For 40, 4k × 1 static RAMs, average power is 80mA × 50V × 40 or 16W. Note that if the MM5295 5V, 16k × 1 dynamic RAM is selected, power dissipation will be even further reduced, with access and cycle times about half the 3 rail version.

Disadvantages

- Not easy to interface to
- Need to be refreshed every 2ms — see "Refreshing of Dynamic RAMs"
- 3 supply rails needed, +12V, +5V, −5V, but these are already required for the 8080

Refreshing of the Dynamic RAMs

With 16k dynamic RAMs all 128 rows of every RAM have to be refreshed every 2ms maximum to maintain valid data. It is possible to manipulate the addressing of the CRTC address bus to the dynamic RAM multiplexed address bus, so that there is no need for a separate refresh counter. This is because for any display row, the 8350 sequences all 80 characters, starting at line 0 and ending at line 9. Thus we can use the 3 least significant bits of the line counter outputs (A_{11}, A_{12}, A_{13}, from LC0, LC1, LC2) for three of the dynamic RAM row address bits, (corresponding to lines 0 to 7 of each display row), and the four least significant bits of the character position address (A_0 to A_3) for the remaining four RAM row address bits. See Figure 8.

Unfortunately, because 19k addresses are required, it is necessary to use two banks of RAM (8 RAMs in each bank), giving a total of 32k × 8. This leaves 13k bytes available for scratch pad, display storage, and in-system emulation of programs. Therefore each row of this second bank of dynamic RAMs also has to be refreshed. By using address bit A_4 to select the bank, all rows of the dynamic RAMs are therefore refreshed every 32 characters, which in fact is eight lines, or in effect one row of the display. The worst case is when the 32 characters are split over two display rows. There is no problem during the vertical blanking because the 8350 still outputs incrementing addresses and LCGA continues to activate the control logic. So refreshing still continues during blanking. Thus the longest period any RAM row goes without a refresh cycle is 65μs per line × 10 lines per row × 2 rows = 1.3ms, which is still within the 2ms maximum at 70°C. *In other words, dynamic RAM refreshing is automatically performed by the 8350 sequencing the address and no extra circuitry is required.*

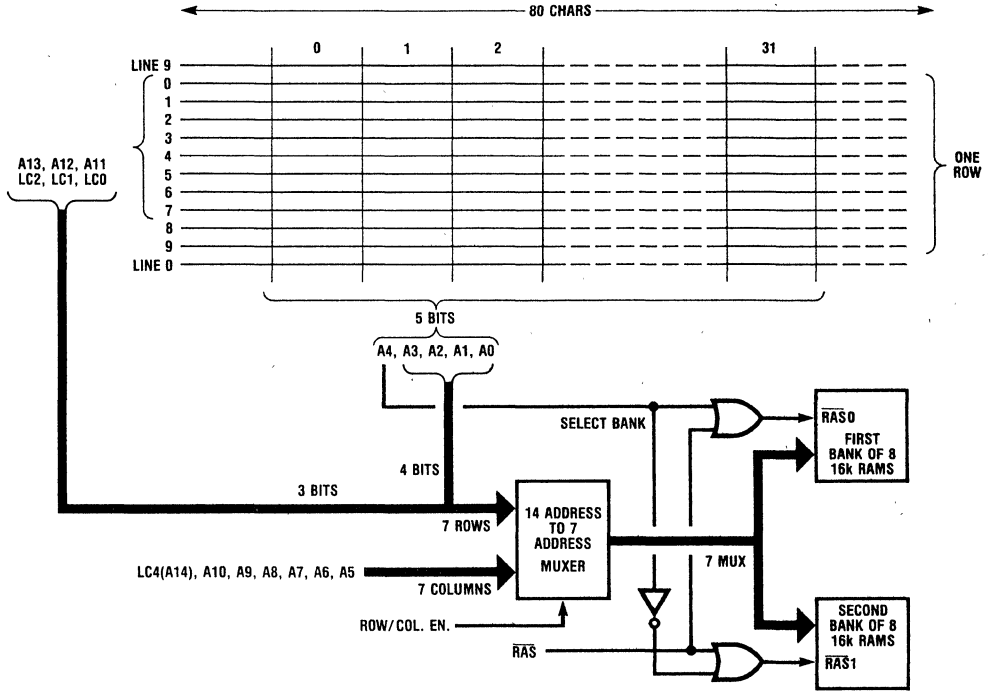


Figure 8. Automatic RAM Refresh

CRT Controller

A graphics/alphanumeric CRT Controller requires the following (See Figure 9):

1) All monitor signals provided — the 8350 provides Vert/Horiz sync and vertical banking
2) Cursor signal — the 8350 has cursor enable
3) Fast dot clock, a 7-dot cycle clock continuous, and a shift register clock only during display — the 8350 has dot clock, LCGA and LVSR
4) Line counter output 4-bit, tri-state — the 8350 has line counter output (but not tri-state)
5) Ability to set top of page, row start and cursor reg at any time — the 8350 can do this using LD REG, RA and RB inputs during the time the μP is on the CRTC address bus. RA and RB can be data bus bits DB0 and DB1, and LD REG can be decoded from the address bus
6) 50 Hz or 60 Hz capability — the 8350 has a frequency select input
7) Incrementing position address, tri-state — the 8350 has this, with a maximum enable/disable time of 30 ns

   This parameter is important in this application where it is necessary to switch the memory from the CRTC address to the microprocessor address, and back to the CRTC address all in one 7 dot cycle of 640 ns. Other CRT controllers are not capable of enabling and disabling the CRTC address so quickly.

Hence the DP8350 requires no extra circuitry apart from a Quad Latch to disable the Line Counter outputs. The 8350 has internal ROMs which determine how many rows (24), columns (80), lines per row (10), and dots per column (7). Versions of the 8350 are available with other combinations.

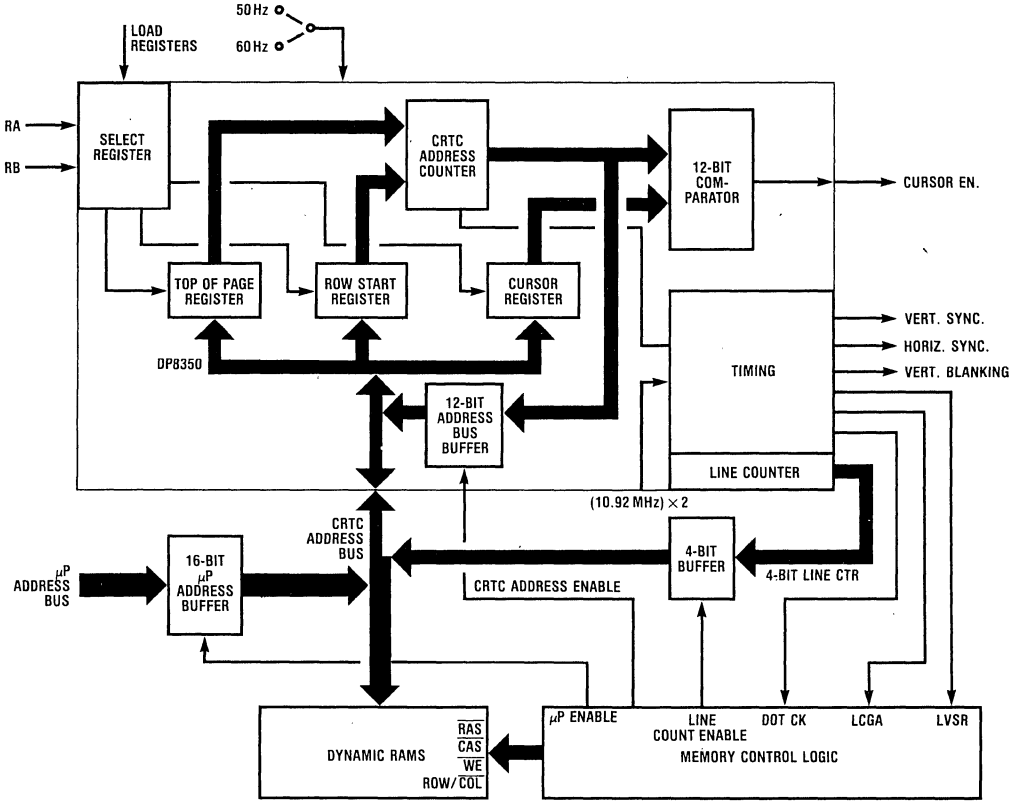


Figure 9. 8350 Block Diagram

System Timing

The standard timing for the dumb terminal type of application is shown in the timing section of Figure 1, with the microprocessor inactive during display time. This is undesirable for graphics applications where full use of the microprocessor is required for computations and peripheral control with very fast baud rate. To determine the timing sequence it is first necessary to calculate the CRTC frequency required for the dot clock.

CRTC Frequency = d × [c + (characters during horizontal blanking)] × [(r × l) + (lines during vertical blanking)] × (line input frequency)

where d = dots per character,
c = columns on display
r = rows on display
l = lines per row

For the standard 8350,

$f = 7 \times (80 + 20) \times [(24 \times 10) + 20] \times 60\,Hz$

$= 7 \times 100 \times 260 \times 60\,Hz = 10.92\,MHz$

This is too slow for the DP8224 which divides the crystal frequency by 9 to provide the clock to the microprocessor. The 8224 frequency can therefore be 21.84 MHz as in Figure 10, and this is divided by 2 to provide the 8350 dot clock of 10.92 MHz, or 91.6 ns per dot. A 7-dot cycle is 641 ns or 1.560 MHz. This is divided by 2, i.e., 780k Hz, to provide a clock frequency for the A/D converter.

The 8080 frequency is 21.84/9 MHz or 2.427 MHz. This frequency is also applied to the ACE to provide the clock for the Baud Rate divider. The baud rate is determined from 2.427 MHz/(16 × Baud Divisor).

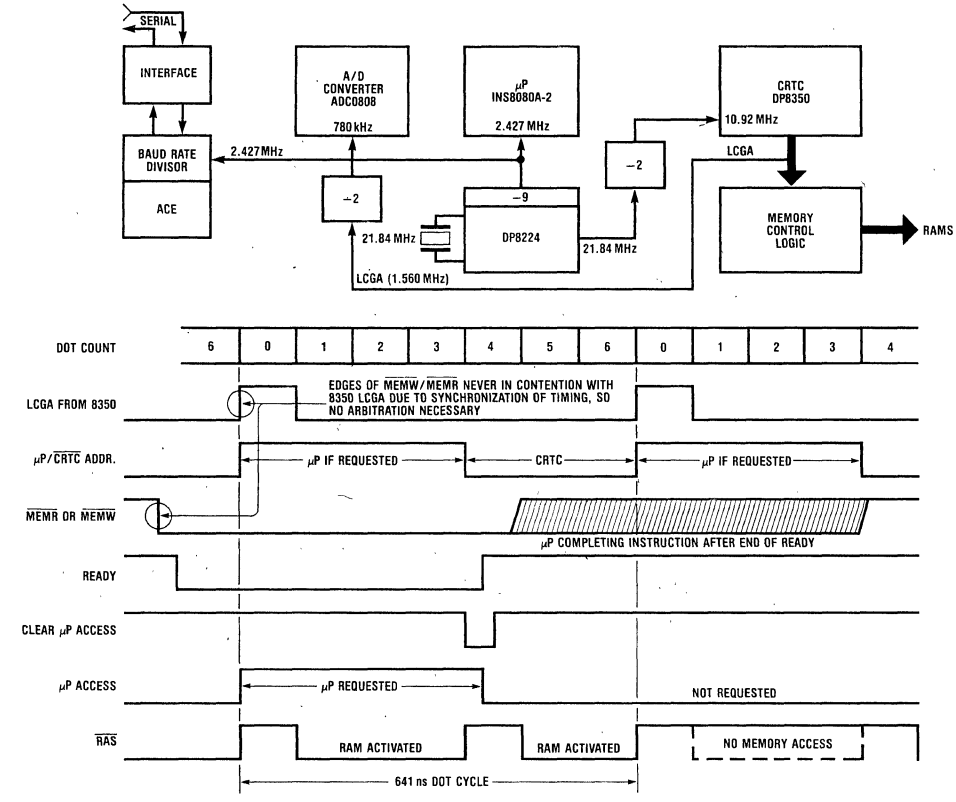


Figure 10. System Timing Control Circuit and Diagram

7 Dot Cycle Timing

Figure 11 shows how the 7-dot cycle time of 641 ns can be time multiplexed into two separate control sequences; Microprocessor and CRTC. It is necessary that the new 7-dot word to be displayed, is available at the commencement of the dot cycle shift. Therefore the 8350 must access the CRTC address bus for the second half of the 7-dot cycle, in fact for the last 3 dots of the cycle. This allows the time period taken by the first 4 dots to be used by the microprocessor, so that the microprocessor address output appears on the CRTC address bus for the first four dots, but only if a μP access is requested.

The CRTC 15-bit address is time multiplexed into 7 rows and 7 columns to be applied to the dynamic RAMs, using 2 DS3648 muliplexer-drivers, with bit A4 selecting the bank. It is therefore necessary to latch in first the rows with RAS (Row Address Strobe), and then the columns with CAS (Column Address Strobe), for both the μP half-cycle and the CRTC half-cycle. All the set-up and hold times are met by the circuitry of Figure 12. If the μP is not requesting RAM access during its half-cycle, then RAS does not occur, although CAS still does. This is because RAS enables CAS internally in the dynamic RAMs, so that if RAS does not occur, the CAS has no effect and the RAM remains in standby mode. This is also the case in selecting the banks with RAS0 or RAS1.

In the second half-cycle, the CRTC always reads the RAM, so WE remains HI, but in the first half-cycle the μP may request a READ or WRITE. WE remains HI for READ, and for WRITE remains LO while RAS is low. Note that the 8350 outputs the address word two dot cycles in advance, and therefore it is necessary to latch and then hold the dot word for one dot cycle. It is then latched into the 7-bit parallel-in serial-out shift register. The 8th bit from the latch can be used as an attribute bit.

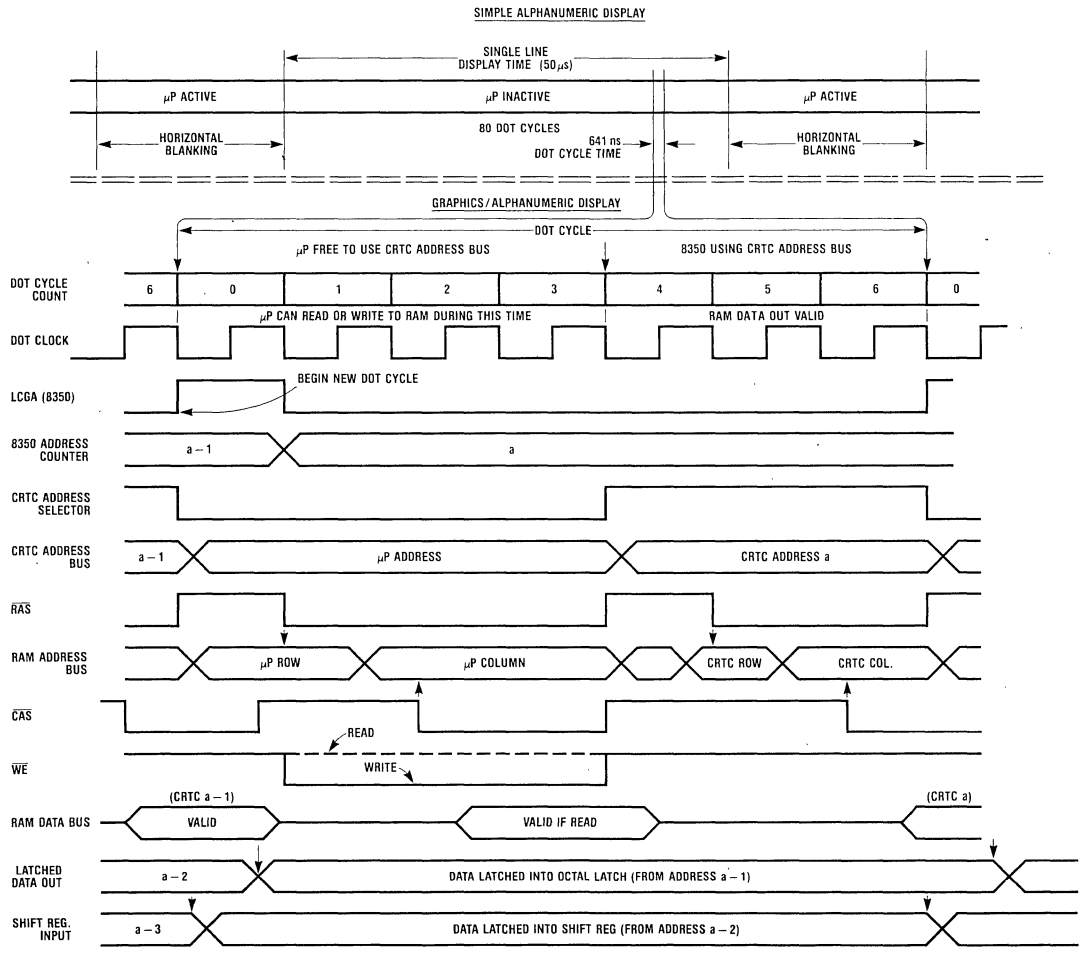


Figure 11. Memory Control Logic Timing Diagram

Figure 12 shows the Memory Control Logic required to correctly sequence the control signals and busses to the dynamic RAMs and associated components. The interfacing from the 8080 microprocessor (via signals MEMR and MEMW) is such that whenever the μP requests to read or write to the dynamic RAMs, the μP Access Flip-flops access the RAMs at the start of the next μP cycle. At the end of these four dots, the information has either been latched into an 8-bit latch (for READ), or written into the RAMs (for WRITE). The READY signal goes active at this time which ensures that valid information is read at the end of the μP cycle; refer to Figure 10. Also the fact that MEMR and MEMW occur at fixed intervals relative to the dot cycle signal, LCGA, means that system contention cannot occur. Therefore there is no need for arbitration between these two signals when a microprocessor cycle is requested.

This also applies when selecting the 8350 to change Top of Page, Row Start and Cursor. To select any of these 3 registers, the μP data bus bits D0 and D1 are connected to R_A and R_B to select the required register.

The information to be latched into the selected register has to be valid on the the CRTC address bus. Because this is time shared with the 8350 address counter, which outputs the incrementing display addresses during the second half of every 7-dot cycle, the CRTC register information has to be valid for the first half of the next dot cycle. The CRTC is selected with DS6/7 and MEMW, so that REGISTER LOAD occurs just after the CRTC register information becomes valid on the CRTC address bus. The 8350 spec requires that the address be valid 250ns before REGISTER LOAD trailing edge (old data sheets do not state this), and that R_A and R_B are valid at the leading edge. Note that the 8350 internal address counter can be enabled or disabled within 30ns of the ADDRESS ENABLE changing state.

All the Logic for Memory Control is Schottky, due to the very fast timing required in the system. Note that the cycle time of the CRTC half-cycle is 270ns, which is less than the 320ns specified for the MM5290-2. This parameter is specified at 320ns for power dissipation reasons, and because the μP is not fast enough to use its half-cycle every 7-dot cycle or 641ns, the average cycle time is greater than 320ns

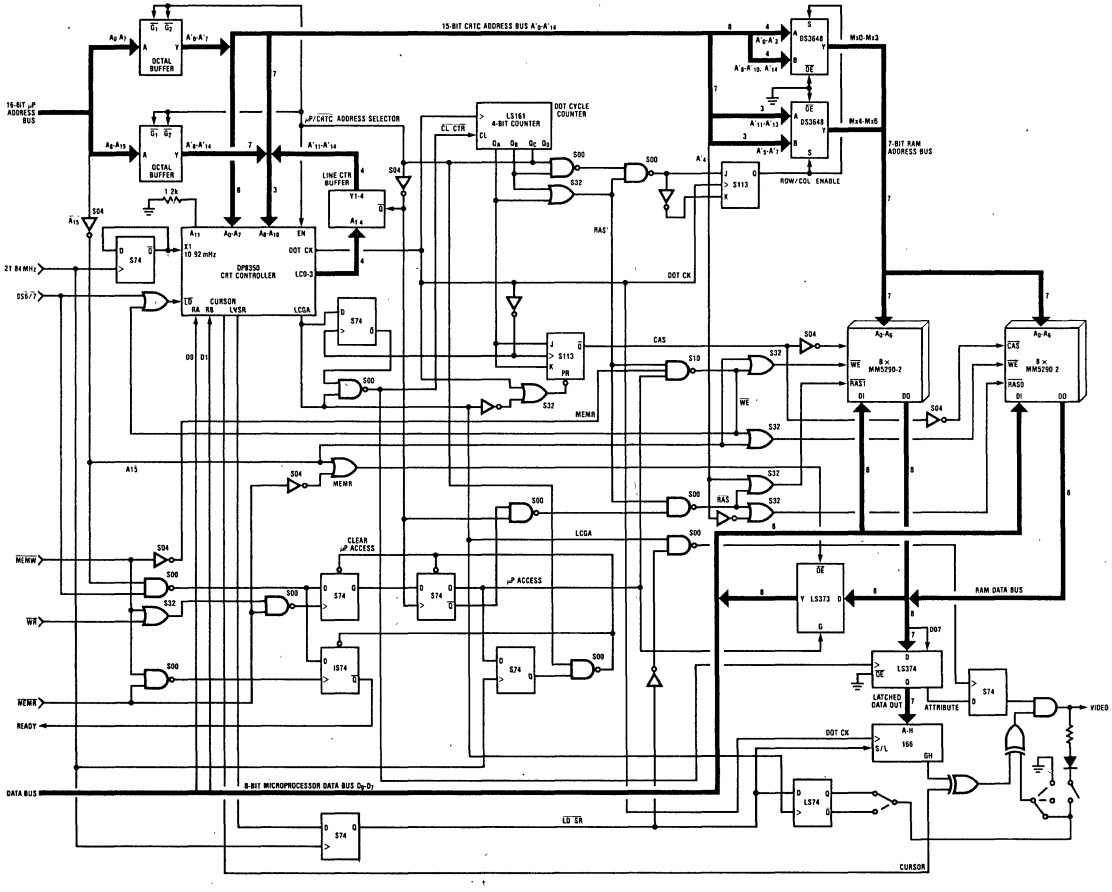


Figure 12. 8350 Graphics Memory Control Logic

System Configuration

Figures 13 and 14 together show the system block diagram. The peripheral components of Figure 13 are used with the microprocessor circuitry of Figure 14. The right hand half of Figure 14 is equivalent to the circuitry of Figure 12.

The LS138 address decoder is used for both I/O and memory addressing. Referring to Figure 15 address map, the peripherals are designated as I/O, and the EPROMs, ROM, CRTC and dynamic RAMs as memory. With address bit A15 HI, the 32k dynamic RAM block is selected. With address bits A14 and A15 LO, the LS138 outputs are selected. A11, A12, and A13 are decoded to select which one of the LS138 outputs goes LO, so that when memory is addressed, each section is 2k bytes. This includes the CRTC which requires 4k bytes from 3000H to 3FFFH for 2 pages. The top four address bits select the CRTC and the remaining 12 address bits are latched into the selected register.

When addressing I/O, address bits A0-A7 also appear respectively on A8 to 15, so that with A6 and A7 LO, i.e., I/O address 00H to 3FH, each LS138 output is now 8 bytes selected by A3, A4, and A5. Bits A0, A1, and A2 are then connected as required to the peripherals, to select the addressed byte.

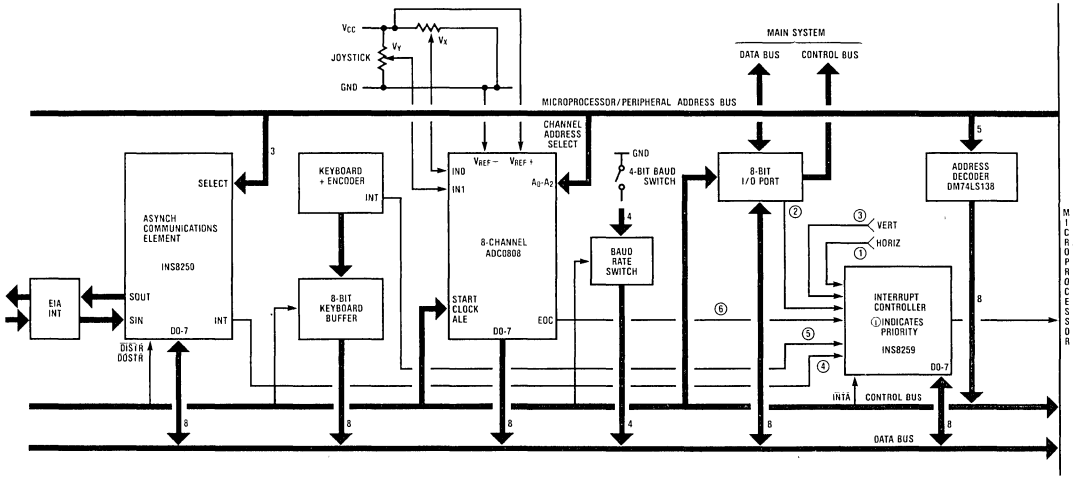


Figure 13. Interfacing to Various Peripherals

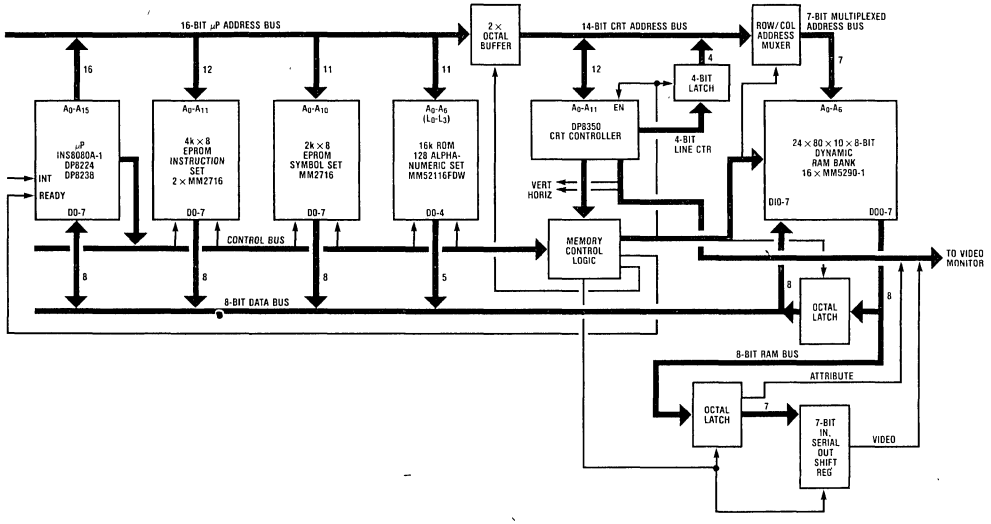


Figure 14. Complex Alphanumeric/Graphics/Symbol Display Terminal

Peripherals

I/O Port

IN 00H or OUT 00H select the 8-bit parallel I/O port, which basically is two octal latches with tri-state outputs. The 8 output bits may be connected to a master 8-bit data bus. When an external 8-bit data word is latched into the input octal latch, an interrupt causes this to be enabled on the μP data bus, when acknowledged with the instruction IN 00H. To output to the master databus, OUT 00H causes the μP data to be latched into the output latch and this also provides an external interrupt to the master system. The master can then read this data by enabling the output octal latch. Data can be transferred fast because the I/O port normally has the highest priority interrupt (IR 3 of the 8259), when required.

Interrupt Controller INS8250

This was also mentioned in an earlier section. At initialization, it is set up to remain in the fully nested mode, so that only higher priority interrupts may interrupt an existing interrupt. Otherwise a lower priority interrupt has to wait for the higher one to finish. Normally the horizontal sync interrupt to IR2 is masked off if there is no need to change ROW START or soft scroll display data off the screen line by line. The I/O address to select the 8259 can be either 10H or 11H; refer to the 8259 data sheet and the software to determine whether A0 is '0' or '1'. Each interrupt routine has to end with a SET END OF INTERRUPT instruction.

Keyboard

The instruction IN 18H reads the ASCII data on the keyboard after a keyboard interrupt has been acknowledged.

Serial I/O Using the ACE INS8250

The INS8250 with its associated EIA RS 232 interface allows serial data to be received or transmitted 8 bits at a time, with the instructions IN 20H or OUT 20H. The baud rate is previously determined as described in the software section. Other ACE registers may be accessed, by connecting A0, A1 and A2 of the μP address bus to the same designations on ACE, so that ACE addresses are from 20H to 26H. During block transfers, such as dumping a picture on the screen into an external memory, or loading from the memory, the higher priority inputs can be masked off for fast transfers.

Baud Rate Switch

See 'Baud Rate' for application, the instruction OUT 28H will read the 4 switch positions.

A/D Converter ADC0808

This 8 analog channel, 8-bit A/D converter, has first to be initialized to commence a conversion on one of the channels. Address bits A0, A1 and A2 are used to select the channel, so that instruction OUT 3nH starts a conversion on INPUT n. The conversion takes about 100μs with the 780kHz clock, so the μP can continue operating during conversion. The END OF CONVERSION signal then interrupts the μP, which when acknowledged reads the 8-bit data with the instruction IN 3nH, although n is not important in reading the A/D.

The A/D converter being only one 28-pin chip, is ideal for demonstrating the graphics capabilities of the system. For instance, an x-y joystick can be connected to INPUT 0 and INPUT 1, so that the movement of the joystick draws on the screen.

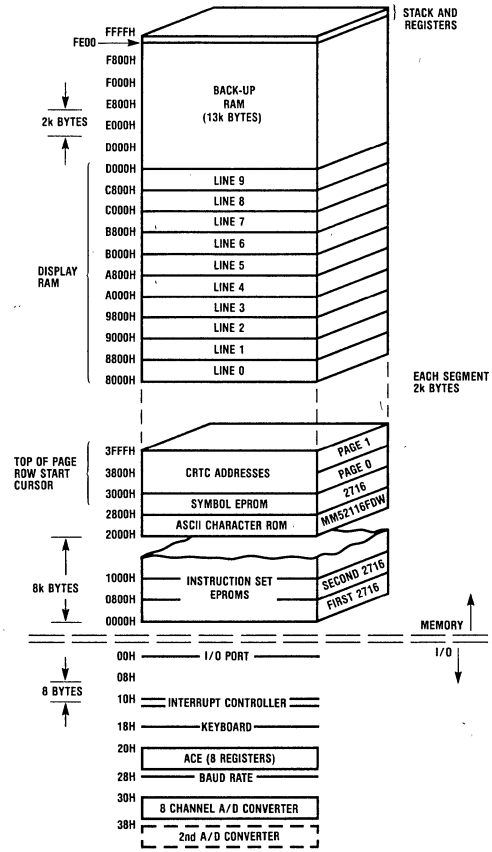


Figure 15. I/O and Memory Map

System Operation and Software

The software was developed purely for demonstration purposes to show the versatility and power of the system. All the software has been tested, but the system could be much more powerful with additional software. The 13k bytes of back-up RAM are also useful in this respect. The software was developed on National's STARPLEX™ Development System. The instruction set so far is just under 4k bytes, so two 2716's are used, but these may be replaced by 2732's if the chip select pins are reconnected, so that extension up to 8k bytes is possible with no extra IC sockets.

Parameter Definitions

The software is structured as in Figure 16. The philosophy was to make it versatile, easy to understand, and easy to modify or add to.

The registers are stored in the dynamic RAMs starting at FE00H in the non-display section. The Top of Stack is also in the RAMs at the highest location, FFFFH. This allows for about 240 nested two-byte PUSHes or CALLs, which is comfortable. Any register may easily be relocated merely by changing its address, similarly any new registers may be added to the list.

The addresses of the various memory and I/O locations are also listed and defined in the front section so these can be changed as desired.

For complete versatility, the display parameters are also listed in the front section so that any different value of parameters from those listed need be changed only in this section. The values of the parameters or constants are those of the standard DP8350 around which the hardware has been designed.

Thus by defining most parameters in the software once, at the beginning, the subsequent routines/subroutines will be valid for different applications and should not need to be altered, merely added to. Not many macros were used in order to save EPROM instruction space.

Interrupt Entry Locations

These are in 8-byte increments beginning at 0010H. The 16 bytes before this are saved for power-up initialization to disable interrupts and set Top of Stack.

Each interrupt location calls that interrupt subroutine. At the end of the subroutine, the system returns to output an END OF INTERRUPT to the 8259, and then returns to the original subroutine in progress when the higher priority interrupt occurred. If no interrupt was in progress, the program returns to the WAIT LOOP which enables all unmasked interrupts to the μP.

Look-Up Tables

This has three sections. First, the BAUD RATE DIVISOR look-up table contains all the 16-bit divisors required for baud rates from 110 baud to 19k baud.

The next look-up table contains PROGRAM LABELS, used in the SEARCH FOR PROGRAM subroutine. The first row contains all the first characters of the program labels, the second row contains the second character, up to the fourth row contains the fourth character. Each program consists of four characters.

The third table is the address list so that once the SEARCH subroutine has located the desired label, it alters the program counter to the equivalent section of this table, which then calls up the program requested.

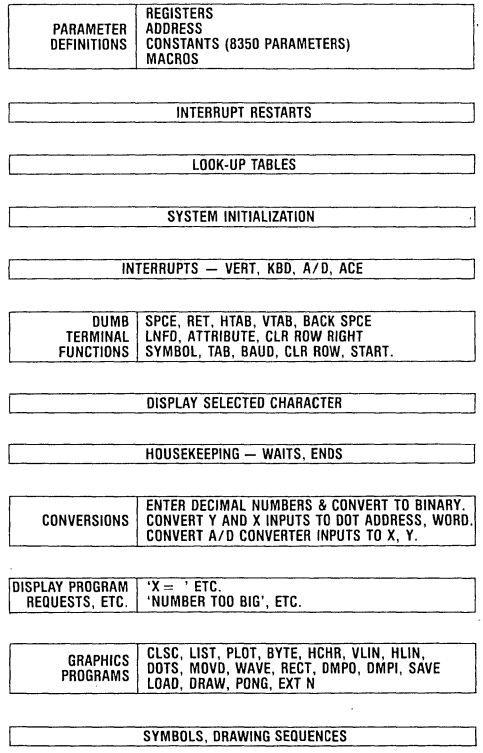


Figure 16. Graffiti — Software Structure

System Initialization

After disabling interrupts and setting Top of Stack, the 32k addresses of RAM are cleared one byte at a time, so that the screen is blank within half a second of switch-on. The cursor is then homed to the first character position. First the Top of Page register is set to 0 in the CRTC and then the cursor register is set to 0, both in the RAM and the CRTC. The column count is also reset.

The ACE is next set up including the baud rate (see Baud Rate section). Next, the Interrupt Controller is set up, and after this the system enters the WAIT LOOP system, enabling the interrupts to wait for an interrupt.

Interrupts

1) *Horizontal Interrupt* is normally masked off but may be unmasked for two reasons: either during scrolling, so that each row can be soft scrolled off the screen a line at a time, or during editing to delete a row, so that a jump in ROW START to the next row has to occur every frame at this new row. This new row must be loaded after horizontal blanking of the last line before the jump row is to begin.

   Note that if the ROW START register is not loaded, each row start address is the last display address incremented.

2) *Port Interrupt* is normally masked off, but must be unmasked if transfer of data to a master system is necessary.

3) *Vertical Interrupt* is used for two purposes. One is to scroll the display by one row, once the scroll semaphore bit has been set in one of the associated subroutines, this is begun at vertical interrupt so that screen flicker does not occur. The other is to change a graphics display every frame so that smooth transition of a subject across the screen is attained. An example of this is the program PONG. The flow chart for Vertical Interrupt is shown in Figure 17.

4) *ACE Interrupt* is by far the most complex because data received by this chip then has to be operated on to determine what action to take. The flow chart for ACE Interrupt is shown in Figure 18. Assuming the interrupt is because ACE has received data available, the ASCII data is checked for a function input. If not a function, but a program is already in progress awaiting inputted data, then this character is saved in the Input Character register. If the character was entered while the cursor was in the first four positions of a row, then the character is saved in a register determined by the column position of the cursor. This saves the character to recall it in a look-up comparison later, while searching for a program. Unless the ASCII code was a function, the character is displayed in the cursor positon (see Displaying Characters).

   If the ASCII code entered is a function, then first CARRIAGE RETURN is checked for. If negative, then all the other functions are checked for and if positive, that particular function is executed. If the input is in fact a carriage return, then a check is made to see if the cursor was in the 5th position, signifying a four character graphics program has been requested. The system then goes to search in a look-up table for a program corresponding to the four ASCII characters entered in order. If a program is found, the system then calls the requested graphics program and executes it. If not, then a carriage return is executed.

5) *Keyboard Interrupt* in most systems is a simple subroutine, merely accepting the ASCII data word from the keyboard and outputting it to the ACE (see Displaying Characters).

6) *A/D Converter Interrupt* sets the A/D semaphore bit.

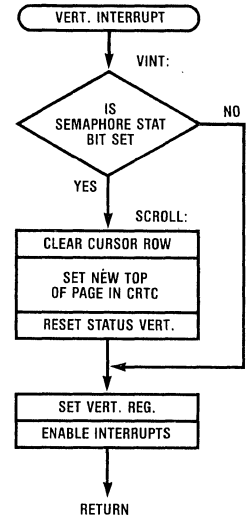


Figure 17. Vertical Interrupt Flow Chart

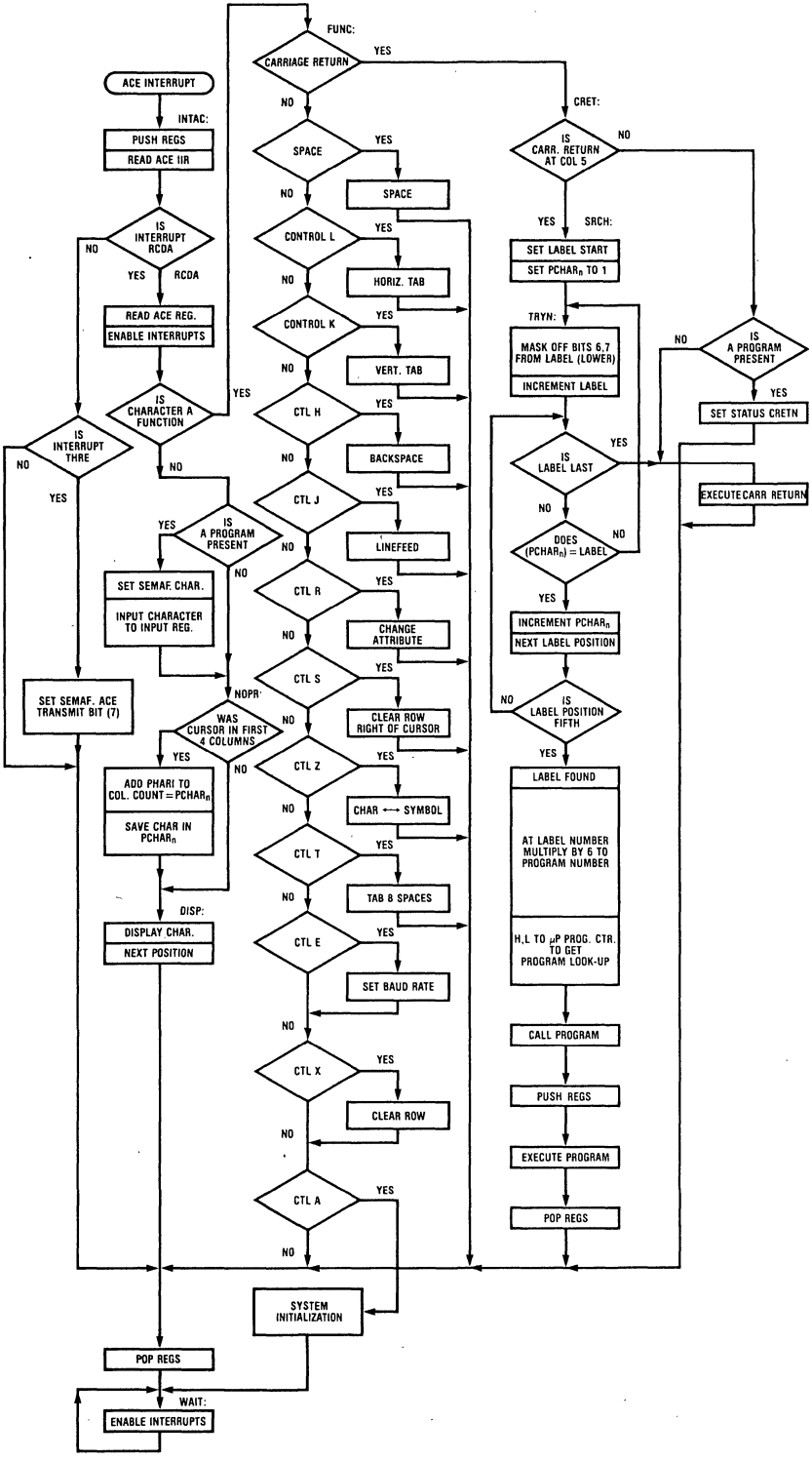


Figure 18. ACE Interrupt Flow Chart

Functions

A number of dumb terminal functions are available with the present software: carriage return, line feed, advance cursor, backspace, up cursor, tab 8 postions, clear row, clear row right of cursor, scroll up one row, and selecting attributes. Attributes available are half-intensity characters and character inversion. Each 7-dot location has its own attribute bit.

Baud Rate

The 4-bit BAUD SWITCH is used to select the BAUD RATE at switch on, or during operation if CTL E is entered. The μP then reads the switch setting and loads the corresponding 16-bit BAUD RATE DIVISOR into the INS8250 Asynchronous Communications Element. Baud rates from 110 to 19k are available, and up to 56k is feasible if the 8080A-2 μP is selected for fast data rates.

Displaying Characters

When a key is depressed, the keyboard outputs the ASCII code of the key selected, which is read by the μP when the keyboard interrupt is acknowledged. The μP then outputs the same ASCII data to the INS8250 ACE to be transmitted serially via the RS232 interface. This can be connected to a main computer, or an identical terminal, or back to the serial input of the ACE. When the ACE receives the returning 8 bits, it outputs a RECEIVED DATA AVAILABLE INTERRUPT or RCDA. The received data is then read by the μP, which selects the ASCII character from the 128 character ROM (MM52116FDW) using the ASCII code as address. The alphanumeric character is copied line by line into the dynamic RAM in the position of the cursor.

Initially all RAM locations are '0' and the dots are written as '1', in a 7-dot word. See Figure 19. Then every frame, as the 8350 scans each line, the 7-dot word for each character postion is latched from the RAM into the 7-bit shift register, and outputted serially during the next 7-dot cycle so that each '1' appears as a dot. The standard ASCII characters are displayed in a 7 line by 5 dot format or font. The 7 lines are copied line by line into the first 7 lines of the 10 line character field, leaving lines 7 through 9 as vertical spacing between characters. Data bits 1 through 5 are used for characters, leaving dots 0 and 6 as spacing between adjacent characters. The keyed character then appears on the screen and the cursor is incremented to the next position.

Additional Symbols

An additional 2716 EPROM with pre-programmed electronic symbols can be selected instead of the ROM, so that circuit diagrams can be drawn on the screen. Each symbol in the EPROM can be 10 lines of up to 7 dots so that each character may be continuous into the next — a necessity for circuit diagrams. The EPROM is selected by typing CTL Z on the keyboard and then a key, which can be either upper or lower case. This then displays the appropriate symbol in a similar manner to an alphanumeric character. To return to alphanumerics again, another CTL Z is required from the keyboard.

Two sequences are also stored in this EPROM, at addresses 1D00H and 1E00H. When either of these are called up by the program DRAW, a circuit diagram is drawn on the screen. This is an efficient way of storing circuit diagrams. Each circuit sequence, requires about 200 bytes, which is not a lot to cover most of the screen, much less than the 19k bytes normally required to save every dot.

Although the symbol EPROM was programmed for electronic symbols, other kinds of symbols may be programmed into this EPROM, such as mechanical symbols.

Programming this EPROM is not easy. Assuming ASCII characters are to be used to select each symbol, then the addresses A_6, A_5, A_4 must be 100, 101, 110, 111 corresponding to ASCII codes 4XH to 7XH, where X is address A_3, A_2, A_1, A_0. The 4 lines LC 3, LC 2, LC 1 and LC 0 go to address bits A_{10}, A_9, A_8, A_7. The EPROM is selected with 00011B to A_{15}, A_{14}, A_{13}, A_{12}, A_{11}. In other words, to select the first line of character A (41H), the address would be 1841H, and for the second line 18C1H etc.

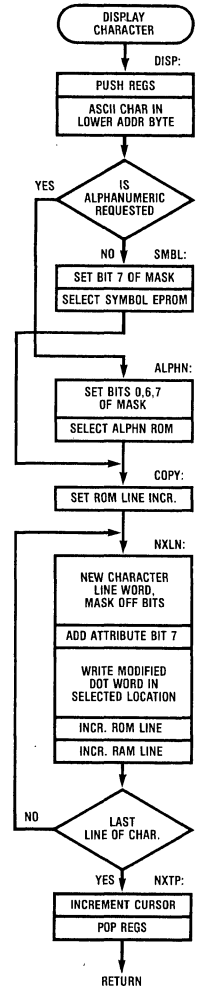


Figure 19. Displaying a Character

Locating the Position of a Dot

The standard DP8350 displays 80 horizontal characters for each of 24 rows, each character field comprising 10 lines of 7 dots. Thus there are 80 x 7 or 560 horizontal dots and 24 x 10 or 240 vertical dots in the display. Let the value of the horizontal dot position be x, where $0 \leq x < 560$, and y be the vertical dot position, where $0 \leq y < 240$. Refer to Figure 20.

If the x and y values are inputted to the microprocessor, it can then compute the character position, the line number and the dot position number. First, the Row Number r is INTEGER (y/10). This then has to be multiplied by 80 to produce the ROW START number. The Column Number then has to be added to this to obtain the Character Position Number, where the Column Position c is INTEGER (x/7). The line of the row is (y – r), and the dot number is (x – c) for the computed character position.

For the 8080 microprocessor, multiplication and division of numbers is laborious and time consuming. It is therefore easier to use the program subroutine shown in Figure 21 to compute the character position, line number, and dot number. A separate subroutine then computes the dot word from the dot number. This 7-dot word is then ORed with the word already in the computed dynamic RAM location. All this can be demonstrated using the program PLOT.

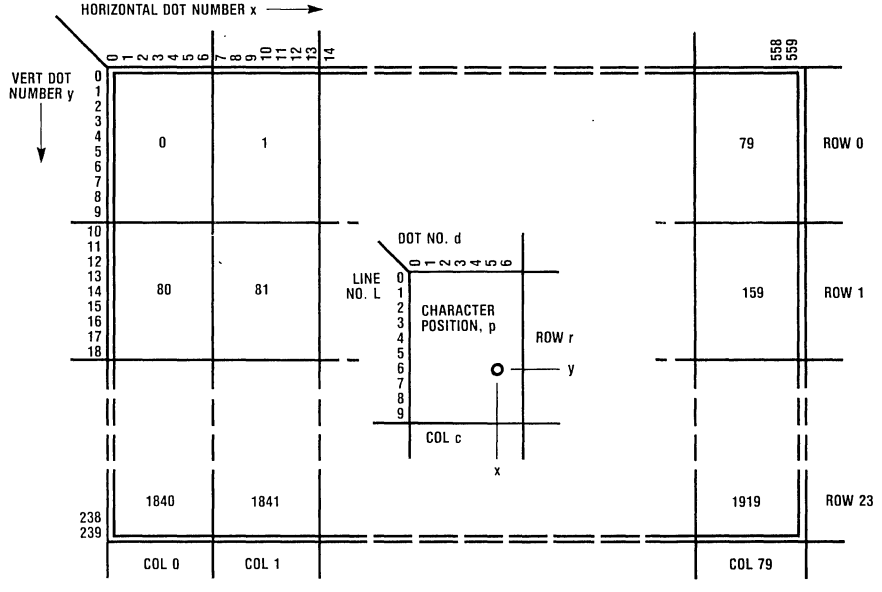
This computation takes an average of 300μs and a maximum of 500μs. Hence up to 3,000 dots can be plotted per second for any values of x and y to create a graphics display.

A good demonstration of the graphics capability is to connect an x-y joystick to two analog inputs of the A/D converter and by selecting the program MOVD (move dot), moving the joystick. The joystick can be moved quickly from one extreme to another and all dots on the way are displayed. This program can also use a dot as the cursor, using the joystick to select its position, and then to depress keys whenever a desired character is required at the character position of the dot.

Dot Word Transfers

With the use of the ACE, it is possible to unload the contents of the RAM into either an identical terminal to copy the display, or to store it in a main computer. It can then be recalled from the computer at a later date and re-loaded into the RAM to be displayed. Or if desired, sections of the display can be transferred. Copying from or to the display can be fast, because 7 dots are read or written at a time. An example of this is to use the programs SAVE and LOAD. A section of the display (such as a circuit diagram) can be saved in the back-up RAM, and then loaded back on to the display in a different area. The diagram appears almost instantly.

This extra 13k bytes of back-up RAM can also be used as additional memory for in system emulation of programs, or for powerful computing capability for graphics calculations.



ROW r = INTEGER (y/10), LINE L = y – r
COLUMN c = INTEGER (X/7), DOT NUMBER d = x – c
DOT AT LOCATION x,y IS IN CHARACTER POSITION p, LINE L, DOT NO. d, WHERE p = 80r + c

Figure 20. CRT Display/8350 Character Address Positions

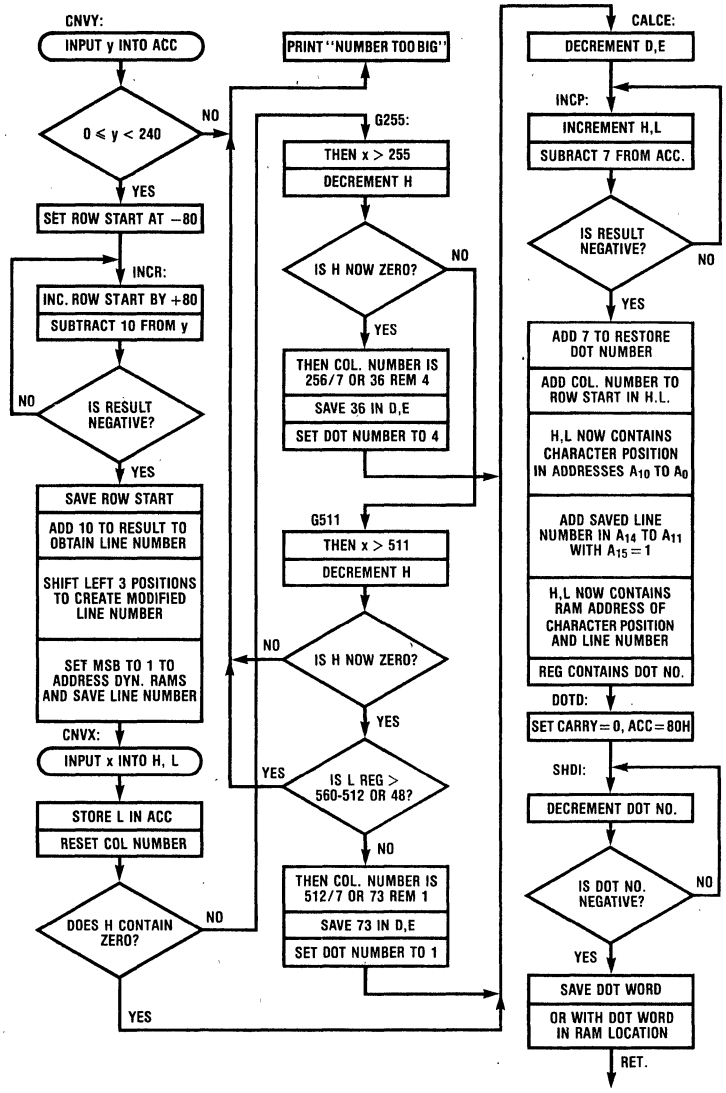


Figure 21. Flow Chart to Add Dot x, y to Display

Graphics Programs

To perform various graphics functions it was decided to select the necessary software with four letter program labels, followed by a carriage return. As long as the label derived starts at the first column of a row, the program requested is called up and executed. Some programs request information from the operator. PLOT is an example of this, where the values Y1 and X1 are requested by the display. The user types in the desired values in normal decimal, signifying the end of the number with a carriage return. After both y and x have been entered, the program continues, in this case plotting a dot at Y1, X1.

Conversion of Entered Decimal Numbers

The conversion of the decimal numbers entered and saved in the Input Number registers, is performed by the subroutine ENTR. First the last decimal number entered (obviously units) is tested for ASCII number units and then saved. The second number (tens) if entered, is then tested and decremented until 0 is reached, and each decrement, 10 is added to the total number. Then the third number (hundreds) is tested and decremented to 0, each time 100 is added to the total. At the end of the conversion, H, L register contains the total number in binary. This is then saved in the respective register.

Conversion of 2 Hexadecimal Characters to an 8-Bit Word

This subroutine takes 2 ASCII characters each in the range 0 to 9, A to F, and converts them to a binary word. First, the 3 ASCII code bits are masked off the number first entered. This is shifted left 4 times and added to the masked off 4 bits of the second number entered. This 8-bit word is now 7 dots plus one attribute bit. With this method, it is easy to write/read words quickly on to the display, in the selected location. This can be demonstrated with the program DMPI (dump-in) as in the next two sections.

Display Loading

The starting address is first entered (anywhere from 8000 H to FDFFH) by keying in the first two hex numbers when requested by B = (byte), no carriage return, then the last two hex numbers. This is repeated for the end address. The bytes are then entered 2 ASCII characters at a time. If the addresses are between 8000H and CFFFH, the words will appear on the display. For example, 7F will appear as 7 dots, or 83 will appears as the 2 right-hand dots with attribute. In this way a picture can be loaded on to the display.

Use of Back-up RAM

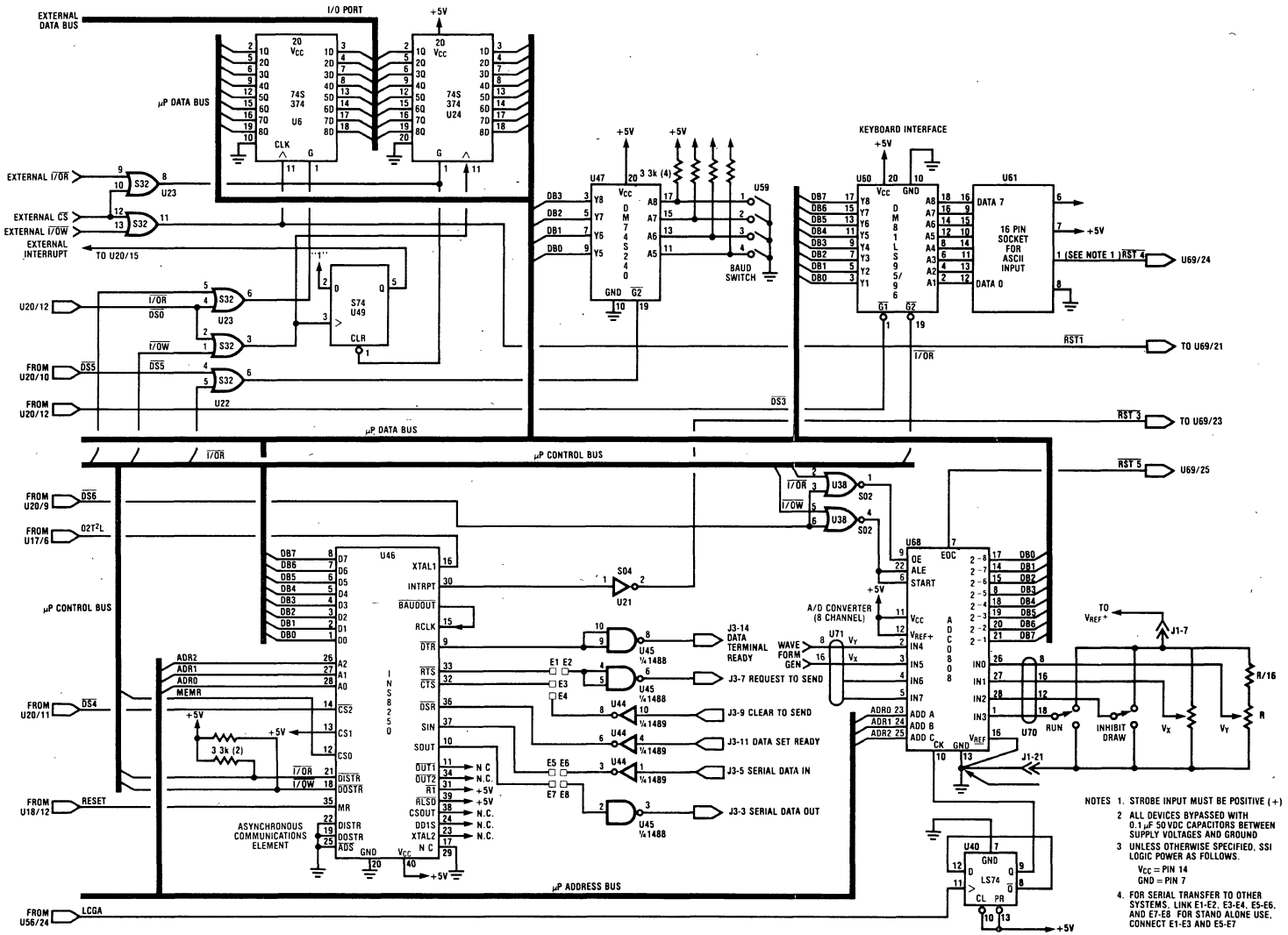
If the DMPI addresses are between D000H and FDFFH, the information is stored in the back-up RAM. This is useful for in-system emulation, for example. By calling up the program EXT0 (External 0), if a program has previously been loaded in the back-up RAM, starting at address D000H, this program will then be executed after EXT0, carriage return. Another use of this section of RAM is the storage of different sequences of circuit diagrams other than those in the symbol EPROM. The program DRAW can then call up the starting address.

Additional Software

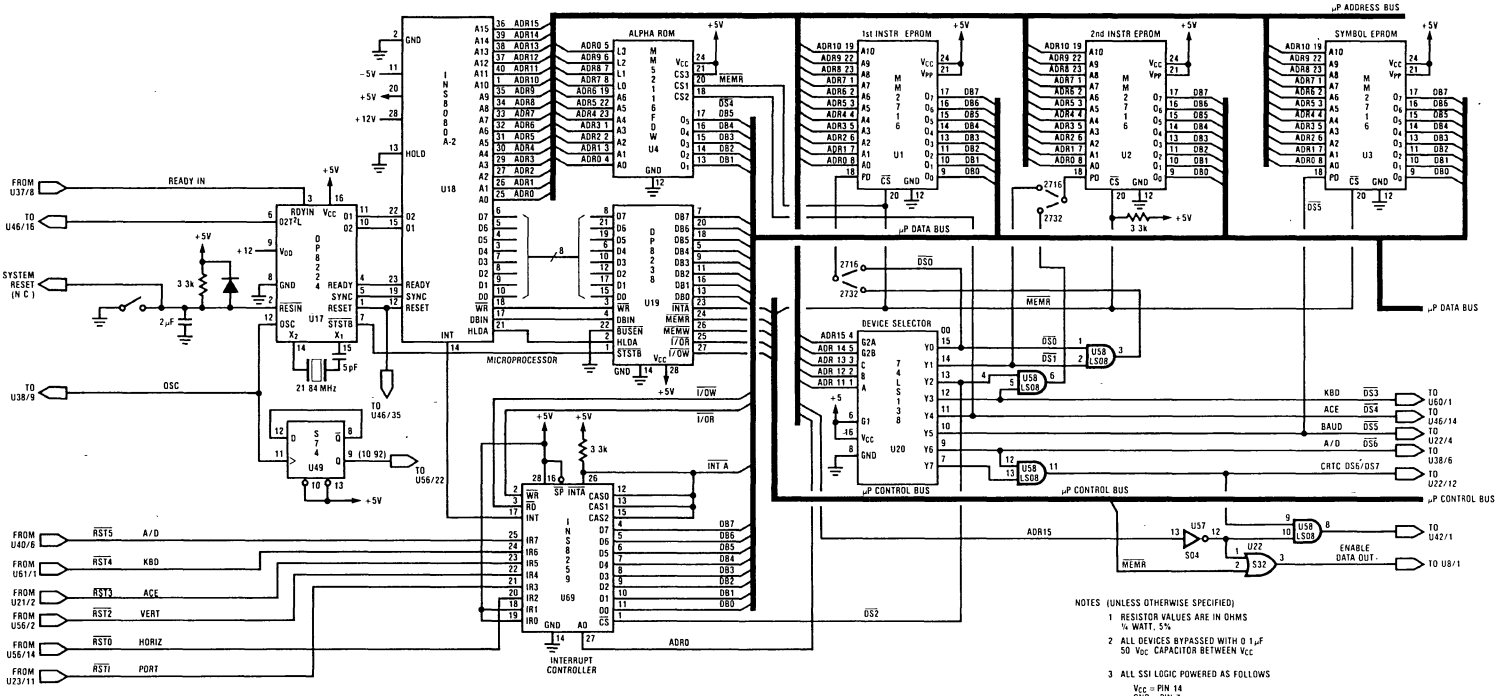
The power and versatility of this system is easily demonstrated with the existing software. This can be added to as required with new software, calling up existing subroutines where possible. Up to 4k bytes of additional software can be incorporated without any hardware modifications (other than moving two links to select 2732s instead of 2716s).

Conclusion

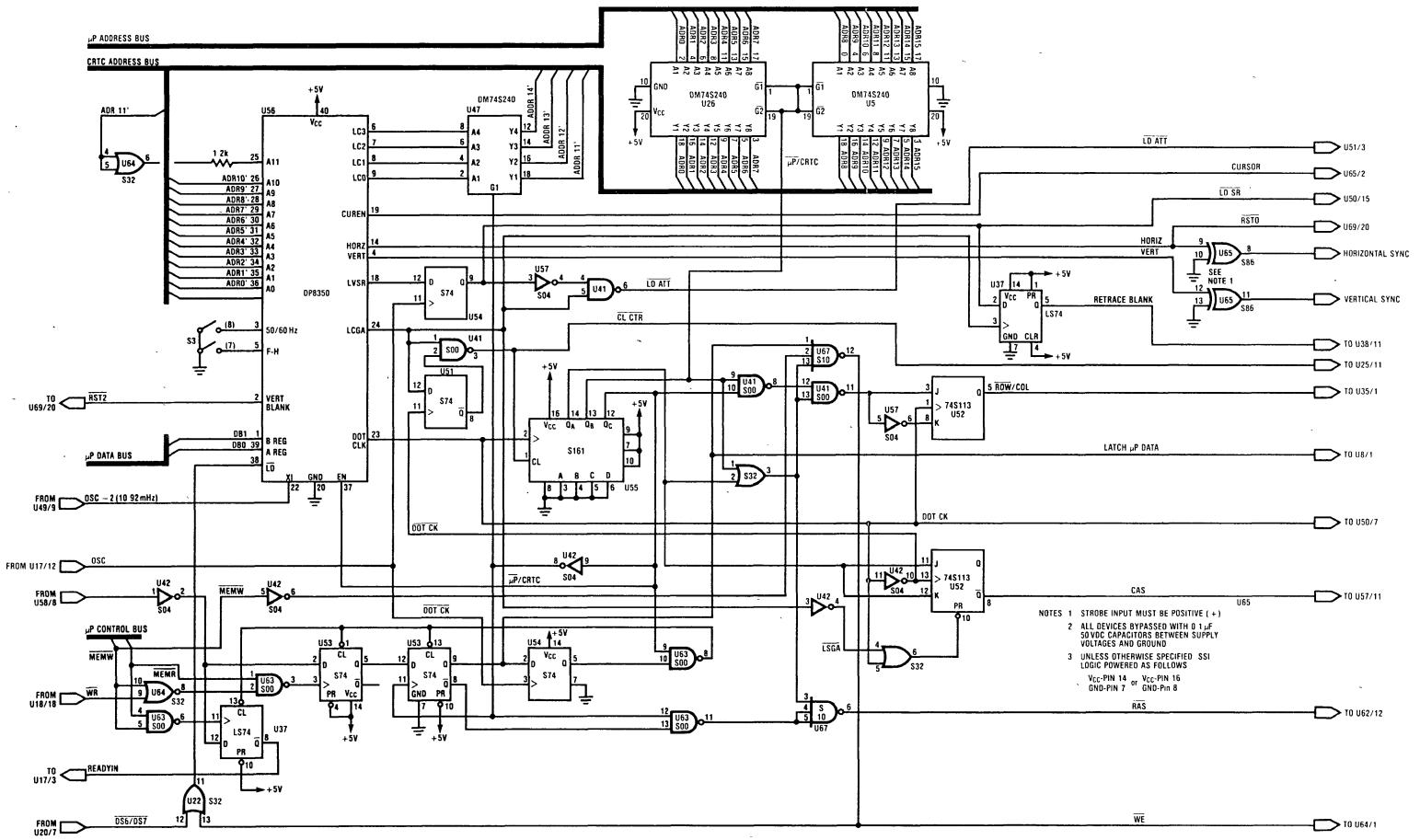
So using all National Semiconductor ICs, at a cost of a few hundred dollars, the hardware for an intelligent terminal with full graphics capability can be fitted on one BLC80/SBC80 size card. The design is easily expandable to systems requiring color. The biggest modification is to the memory; instead of one bit per dot, 3 bits are required for blue, green, and red, to give 8 possible combinations per dot. A small number of extra logic ICs are required, as are minor additions to the software. To select the color, a CTL key can be used followed by the code for the color. This color will then be written until changed by the CTL key. A different CTL key followed by a number could previously have set the background.



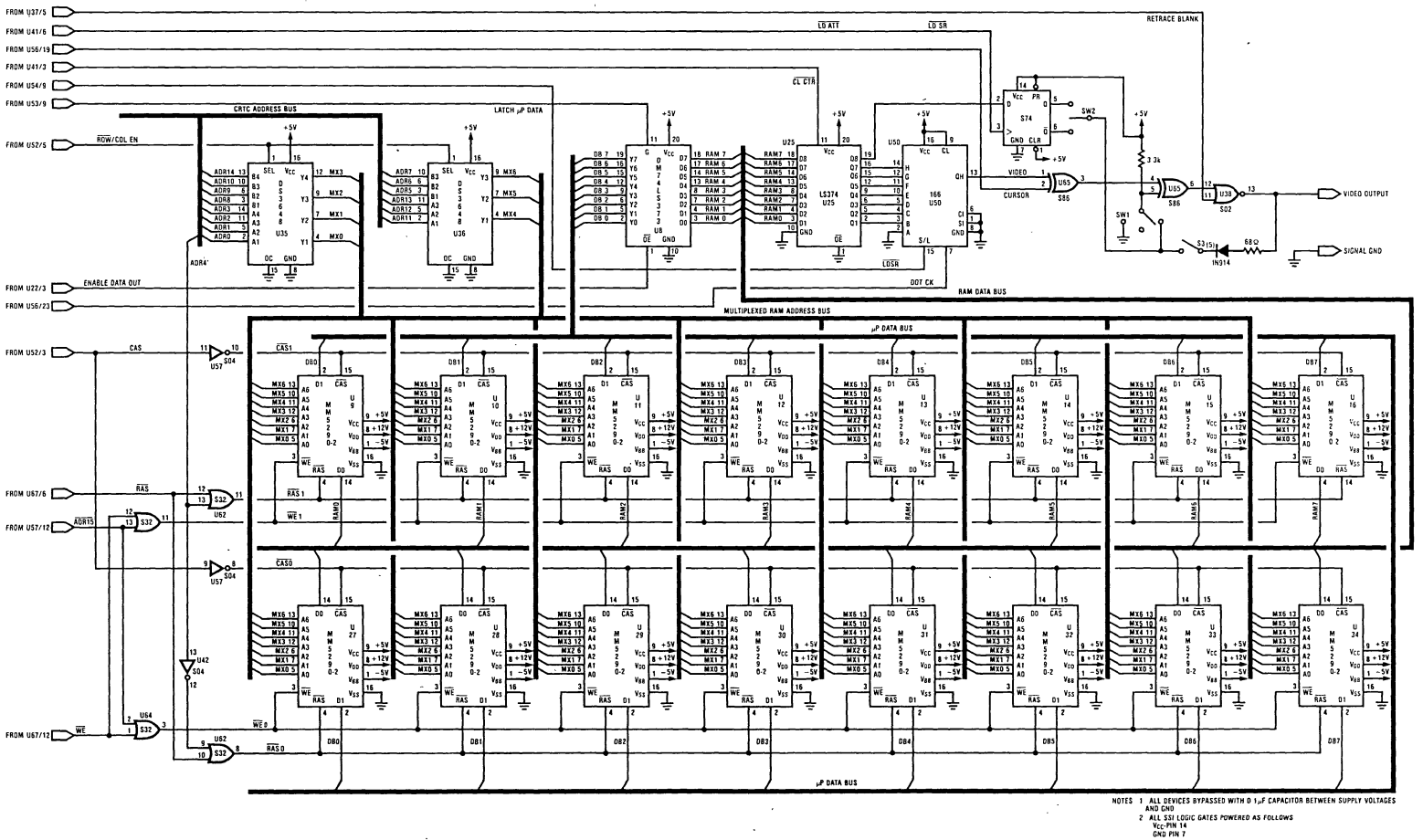
DP8350/INS8080 Full Graphics Video Terminal System — Peripheral Interface Block



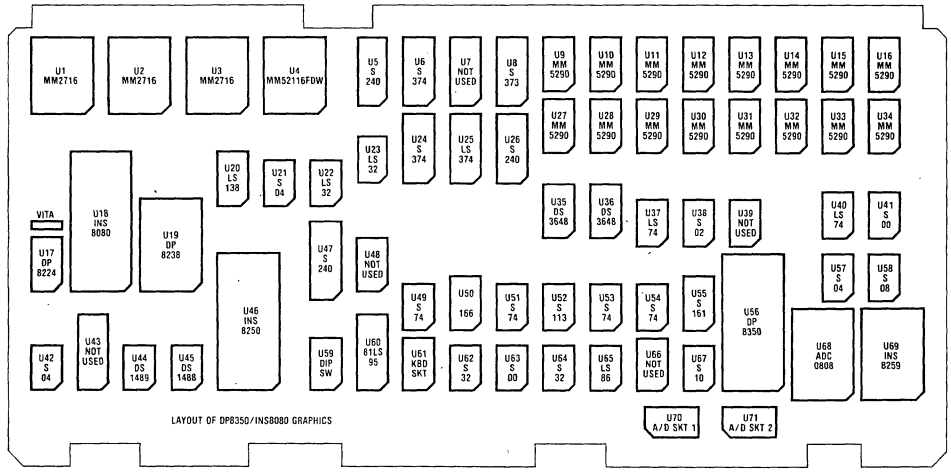
DP8350/INS8080 Full Graphics Video Terminal System — CPU, EPROM and Interrupt Block



DP8350/INS8080 Full Graphics Video Terminal System — Memory Control



DP8350/INS8080 Full Graphics Video Terminal System — Memory/Video



Layout of DP8350/INS8080 Graphics

Present Capabilities of Alphanumerics/Graphics System

Dumb Terminal Functions

** All 128 ASCII Characters Displayable
** Space
** Carriage Return
** Horizontal Tab (→) or (CTL L)
** Backspace (←) or (CTL H)
** Linefeed (↓) or (CTL I)
** Vertical Tab (↑) or (CTL K)
** Select/Deselect Attribute (CTL R) with SW-1 or S-3
** Tab 8 Spaces (Tab) (CTL T)
** Clear Cursor Row (CTL X)
** Clear Row Right of Cursor (CTL S)
** Initialize System (CTL A)
** Select Baud Rate from 110 to 19,200 Using S-1 and CTL E
** Scrolling Upwards

Non-Standard Character/Symbol Selection

** By selecting CTL Z, symbols can be displayed for each key of the keyboard, including shifted and control keys. Also can deselect back to standard ASCII characters with CTL Z.

Graphics Programs

*CLSC: Clears screen only, leaving 13k back-up RAM unaffected.

*LIST: Lists all graphics programs.

*PLOT: Plots a dot at X, Y. X is the number of horizontal dot positions from the left of screen, from 0 to 7 × 80 for the 8350, i.e., $0 \leqslant x \leqslant 559$. Y is the number of vertical dots from the top of the screen, from 0 to 10 × 24, i.e, $\leqslant 0 \leqslant y$ 239. The operator keys in the decimal values of Y and then X when requested by the display.

*VLIN: Draws a vertical line between Y1 and Y2 at X. These values are entered decimally by keyboard when requested by the display.

*HLIN: Draws a horizontal line between X1 and X2 at Y1. These values are entered decimally by keyboard when requested by the display.

*RECT: Draws a rectangle linking lines X1, X2, Y1, and Y2.

*PONG: Bounces a dot around the screen between the four walls of the display.

*DRAW: Draws a diagram on the screen from a sequence of operations saved in ASCII code in memory. The START address of the sequence is determined by the first four hexadecimal characters entered on the keyboard. The address 1D00H selects a DC voltage restoring circuit sequence located in the symbol EPROM. Address 1E00H selects a logic circuit and waveforms. Test sequences can be loaded into back-up RAM using program 'DMPI' at the starting and end address entered. This start address is then called up by 'DRAW.' The end address must contain 0 (zero).

*SAVE: Saves in the back-up RAM a section of display contained within rows R1 to R2, and columns C1 to C2. These values are entered decimally by keyboard when requested by display. The start address in the back-up RAM is selected by the first four hexadecimal characters entered on the keyboard.

*LOAD: Loads from the back-up RAM to a section of display bounded by R1, R2, C1, C2. These values are entered decimally by keyboard when requested by the display. The back-up RAM start address is selected as in SAVE.

*DOTS: Plots N dots on any line Y1 at postions X1, Y1; . . . XN, Y1; and then any new line entered in decimal by the operator. Ends the program by entering 0 (zero) when the next Y1 is requested.

*MOVD: Uses the 8-channel 8-bit A/D converter to monitor the voltages on a X-Y joystick, an inhibit-draw switch, and an exit-program switch. In the DRAW mode consecutive dots are plotted to create a picture as described by the movement of the joystick. All these input signals are connected to the first A/D socket. In the inhibit DRAW mode the dot is moved around by the joystick as a cursor, and by keying in from the keyboard the desired charcter, this character will appear in the character field of the dot.This moving dot can be used to erase existing dots, or erase characters by keying 'SPACE' in the desired position. To exit the program, set the EXIT program switch in EXIT-DRAW mode with the Inhibit-Draw Switch in INHIBIT.

*WAVE: Uses the A/D converter to create waveforms on the screen when the signals are connected to the second A/D socket.

*DMPO: Unloads any part of RAM to an external system starting at an address keyed in by the operator in hexadecimal characters (four) and ending at another similarly entered address. The RAM is unloaded 7 dots at a time per line of character and converted to two ASCII characters and then transmitted serially.

*DMPI: Loads any part of RAM from an external source (or the keyboard) starting at an address selected by the first four hexadecimal characters entered on the keyboard and ending at another similarly entered address. The RAM is loaded 7 dots at a time per line of character, keyed in by two hexadecimal characters, for each word. The addresses selected can be display addresses 8000H to CFFFH or back-up RAM addresses D000 to FFFFH (warning: FE00H upwards are registers and FFFFH downwards are stack). Thus a complete picture could be loaded on to the display. Alternately a program could be loaded into back-up RAM at EXT0 (D000H), EXT1 (D800H), EXT2 (E000H), or EXT3 (F000H). the characters 'EXTn' can then be typed in on the keyboard and this will then select the instructions beginning at address EXTn. Thus in-system emulation is easily accomplished.

*EXT0: Executes a program beginning at RAM address D000H. The program must previously have been entered using DMPI selecting D000H as the starting address.

*EXT1: As EXT0 but starts at D800H.

*EXT2: As EXT0 but starts at E000H.

*EXT3: As EXT0 but starts at F000H.

Software Design for a High Speed (38.4 kbaud) Data Terminal

National Semiconductor
Application Note 270
Wong Hee
Nick Samaras
February 1982

INTRODUCTION

This application note describes a high speed CRT terminal designed around the DP8350 CRT controller and the INS8080 microprocessor. The hardware is a modified version of the circuit described in Application Note AN-199. The software was redesigned and optimized for terminal speed and function. In its present form it is upwards compatible with the Hazeltine 1500 video terminal and has a limited graphics capability. Furthermore, it is able to communicate with a host computer via an RS-232 port, at 38.4 kbaud, without using fill-in characters or handshaking. One 2k by 8 EPROM contains all the software required to implement the terminal. An optional EPROM can be used to add features such as menu display or to transform the terminal into a calculator (in the local mode). The absence of the second EPROM does not affect the operation of the terminal as the software checks for its presence.

DATA TERMINAL FEATURES

- Modes: remote/local
- Limited graphics
- Window scrolling
- Line transmitting and local editing
- Hazeltine 1500 compatible*
- Video display: two pages, 24 × 80 characters/page
- Upper/lower case
- Scrolling plus screen roll up/roll down
- Cursor: blinking (two rates)
- Line, character insert/delete
- Attributes: dual intensity/inverse video
- Full duplex RS-232 port; 110-38400 baud
- Keyboard input: 7-bit parallel
- Full cursor control and addressing
- Cursor enable/disable
- Single board (BLC/SBC) compatible design

*The majority of the software written for the Hazeltine 1500 will run with no modification. However, there are differences.

UNIQUE FEATURES

Graphics Capability: The graphics capability of this terminal, although limited by the number of symbols (34), proves to be very helpful. Typical uses include digital waveform generation (e.g., logic analyzer display), and graph oriented displays such as histograms. A graphics menu is available in the local mode. Entering ↑Q† from the keyboard will result in a two line menu display. Line 23 displays upper and lower case characters, while line 24 displays the corresponding graphics symbols (see *Figure 3*). In local, entering ↑B will switch the terminal to the graphics mode; the ESC key can be used to exit. In remote mode, the format requirements for graphics display generation are summarized by the flowchart shown at the bottom of this page.

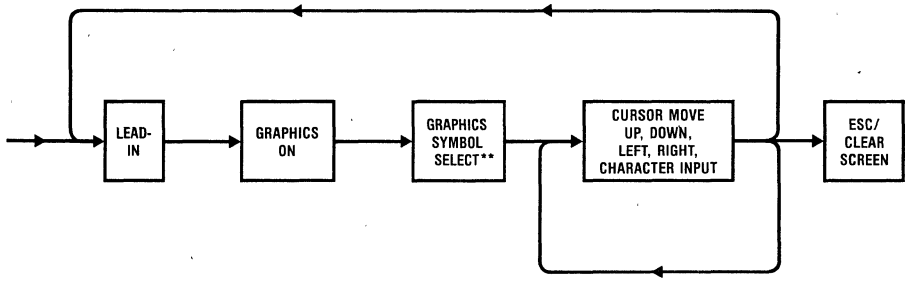
The same flowchart can be used in local, if the "lead-in"†† block is omitted.

Typical transmission sequences are:
7E, 02, 42, 10, 1B
7E, 02, 63, 10, 10, 10,...,10, 1B
7E, 02, 42, 8, 8, 8, 4A, 7E, 0C, 7E, 0C, 1B

All the graphics symbols, along with the upper and lower case characters, are coded into one 2716 EPROM. As a result, both the character set and the graphics symbols may be customized. The total number of available fonts is 128. The field on each displayed character is 7 rows by 10 columns. The alphanumeric symbols occupy a 5 by 7 subfield typically, except for those requiring descenders; they occupy a 5 by 9 section, while the graphics symbols utilize the whole 7 by 10 field.

Transmit: The data terminal can transmit one line of text upon receipt of the 14H code from the keyboard in local mode. Alternately, the host CPU can request transmission by sending 14H prefixed by the 7E lead-in code.

†Note that ↑ indicates a control key entry.
††Lead-in code: 7E.



**Includes the ASCII characters A-Q, a-q, space and DEL.

The same function can be used in a relatively unconventional way when programming in BASIC. The majority of BASIC interpreters used in small business systems or home computers incorporate a line-oriented editor, almost adequate for most of the tasks they have to perform. The basic problem with such editors is that they cannot change the flow of the program easily. In other words they cannot change line numbers. This is a shortcoming, as it is both annoying and tedious having to retype segments of text in order to change the program flow, just because the editor cannot handle altering line numbers only.

This terminal offers an efficient solution to this problem. Simply stated, it allows changing line numbers only. Here is a brief description of a typical sequence leading to text and/or line number modification. Let us assume that a BASIC interpreter is used and that the program that needs to be changed is in memory. Using the list command, the program lines to be modified can be displayed. Now, while in the Command Mode of BASIC, the terminal is switched to local. The user has effectively at his disposal a screen-oriented editor. The cursor can be moved about and text changed as desired; that, of course, includes line numbers. When the editing is completed, the user positions the cursor on the line that was altered and types ↑T. In response, the cursor scans the line, inverting the attributes. At the same time the line is transmitted to the host CPU in the same order as it was scanned, from left to right. Attribute inversion serves as feedback to the user. After the last character of each line has been transmitted, the cursor returns to the beginning of the following line. As a result, consecutive ↑T keyboard entries transmit successive lines. Thus, altering the flow of a BASIC program involves entering the local mode, changing line numbers, transmitting the modified program lines, and switching back to on-line operation. All this can be accomplished at a fraction of the time usually required otherwise. Finally, entering similar lines of text such as the ones found in "PRINT" statements, can be accomplished easily by switching to local, typing the first line and transmitting it; then moving the cursor up one line, changing the line number along with parts of the text that are different, retransmitting the line, and so on. In this way the user can create a long program segment while operating repetitively on one line.

Insert/Delete with Range: This is a rather unusual function that can assist in generating psuedo "screen window" effects. Specifically, a pre-selected number of display lines can scroll while the rest of the display remains fixed. Each "window" is defined as N lines by 80 characters, where: $1 < N < 48$, counting from the current cursor location to the end of page. The brief BASIC program that follows demonstrates the use of this function. In this example the display lines 1 through 4, and 19 through 24 remain "frozen". The message (100 lines long) is displayed on lines 5 through 18, demonstrating the scrolling of a section of the display.

```
100  PRINT CHR$ (&H7E) + CHR$ (&H11) + " d";
110  FOR I = 1 TO 100
120  PRINT CHR$ (&H7E) + CHR$ (&H1D) + CHR$ (&H49)
       + CHR$ (12);
130  PRINT, "WINDOW SCROLLING LINE:", I,
       CHR$ (&H0D);
140  NEXT I
```

80 Character Software FIFO: This is one of the key items that allows terminal communication at 38.4 kbaud without handshaking. An 80 character first-in, first-out software buffer is used. The incoming characters are stored temporarily in this buffer, while the microprocessor is servicing interrupts. As time becomes available, the characters are retrieved from the FIFO and processed. That includes performing a terminal function or moving an ASCII character to the video memory. The software allows for a large number of concurrent service requests such as row start, keyboard, as well as multiple ACE interrupts.

Fast Service Routine for Row Start Interrupt: Conventional row start address look-up and loading are not done during the row start interrupt time; instead, a simple row counting routine is used. The terminal count (a software counter) generates a triggering signal for video RAM wrap-around address loading. The use of this technique improves the system throughput substantially. Cursor and Top of the Page address loading (i.e., writing to the appropriate DP8350's registers) is done during the vertical retrace interval.

Keyboard Controlled Mode Selection: The operating mode of the terminal can be selected from the keyboard. To aid the user in identifying which mode the terminal is in, two cursor blinking rates are used. The low rate indicates remote mode; a high rate indicates local.

Other functions that can be selected from the keyboard are:
1) Upper/lower case. The default mode upon power up is determined by reading the SW3 switch setting.
2) Next page. A software switch that selects for display page one or two.

Read Cursor: In the local mode the present cursor location can be displayed on line 24, columns 79-80. For example, if the cursor is located on line 8, column 66, entering ↑E from the keyboard will result in a display of "Ag" at the bottom right hand corner of the screen. This can save time in looking up the ASCII equivalent codes of the X, Y cursor coordinates to be used in cursor addressing. (Note that, ↑E = ENQ = 05H.)

The following is an example of how this could be used in a BASIC program.

```
PRINT CHR$ (&H7E) + CHR$ (&H11) + "Ag"
```

Upon execution of the above statement, the cursor will move to line 8, column 66.

Menu Display: In the local mode the user has access to a menu display that summarizes the terminal's functions, along with the corresponding control codes (see *Figure 1*). This feature is optional and resides in EPROM #2. The important thing to note is that various kinds of menu/HELP displays can be implemented easily in this fashion. This function can be accessed from the keyboard. Alternately, a dedicated HELP key (that generates the 1D code) can be used.

ACKNOWLEDGEMENTS

We would like to thank Barry Siegel for his invaluable guidance and support. Also we would like to thank Ron Christopherson for contributing so much of his time to this project.

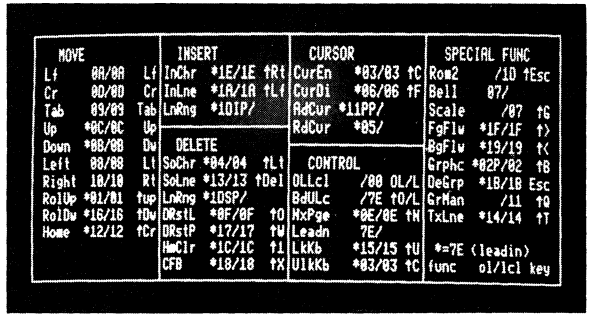


FIGURE 1. Sample Menu Display

Character Generator Fonts

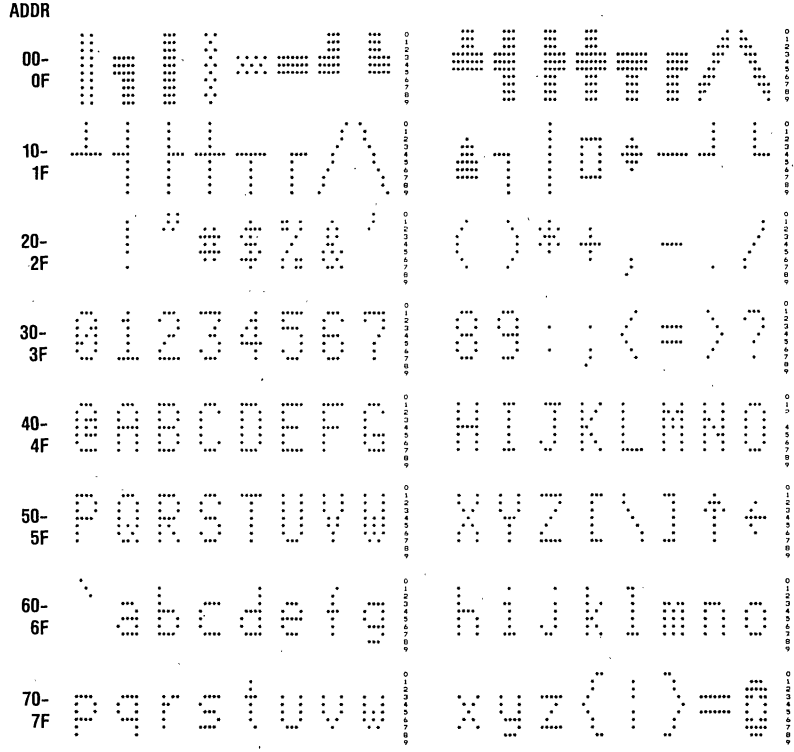


FIGURE 2. Sample Character Font

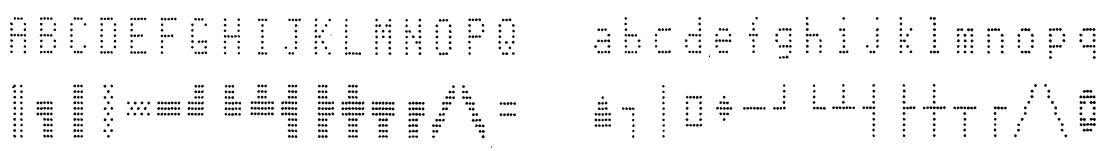
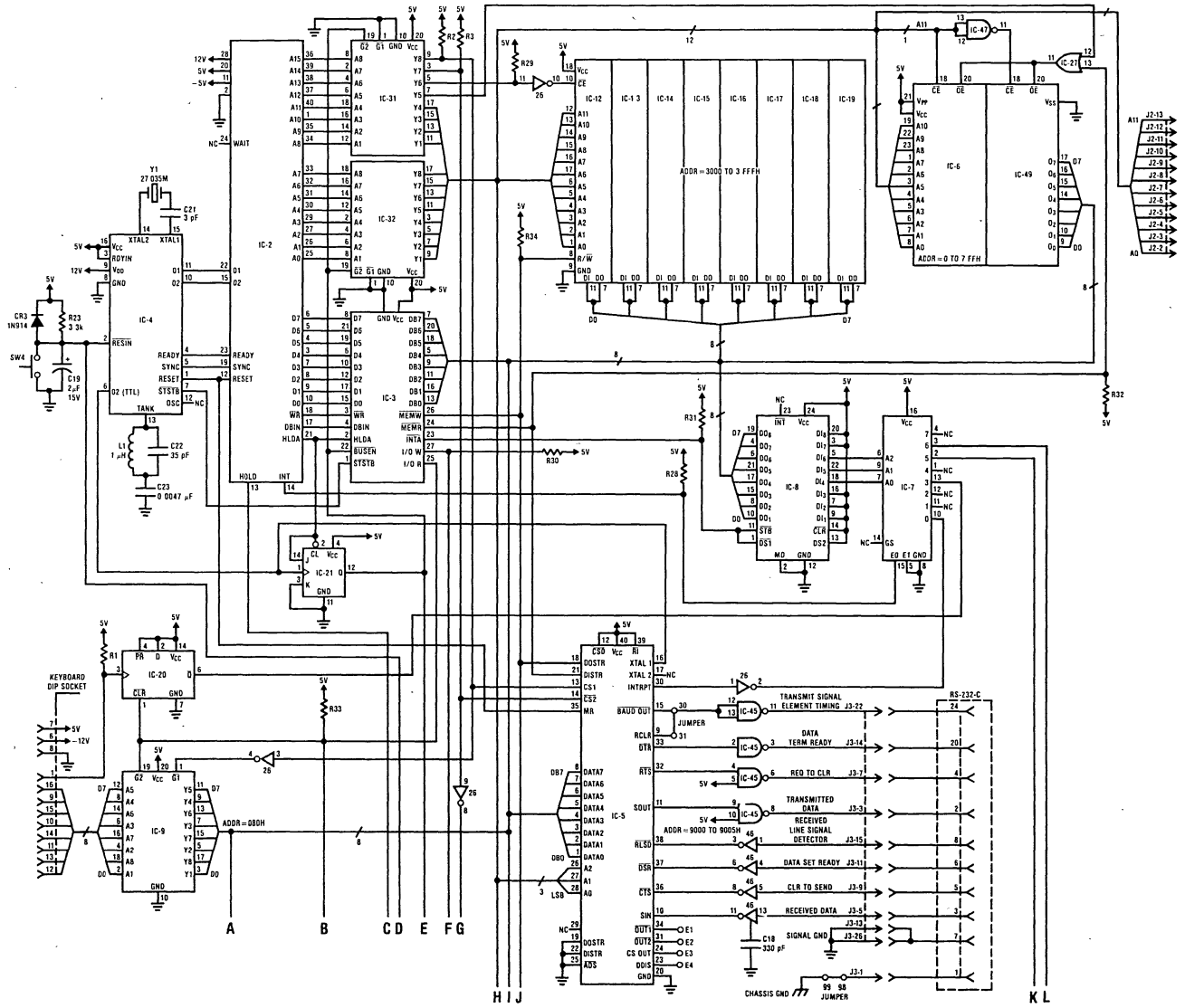
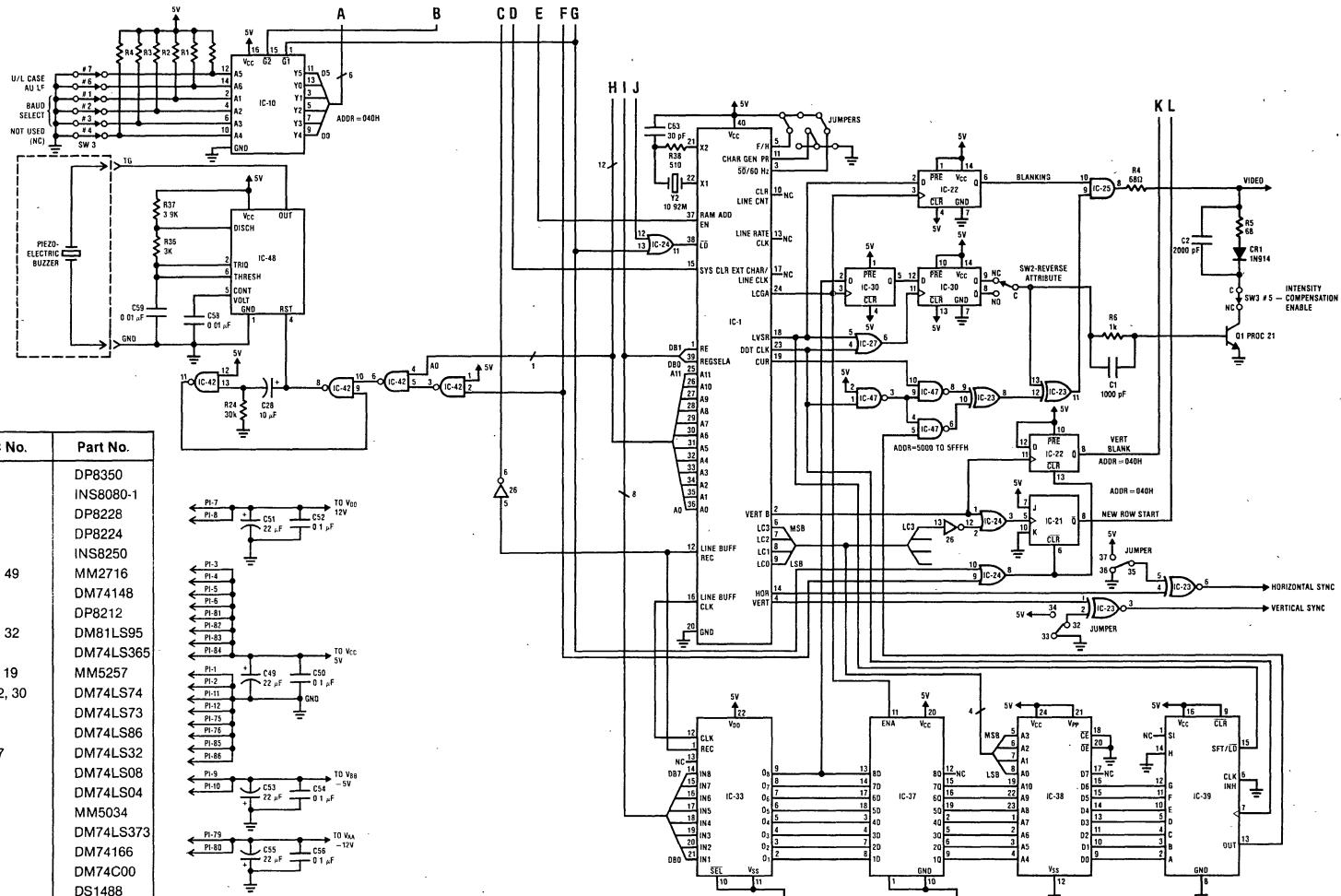


FIGURE 3. Graphics Menu Shown at the Bottom of the Screen

A complete listing of the software for the "High Speed Data Terminal" can be found on pages 5-84 through 5-103. A HEX dump of the character generator set is included on pages 5-82 and 5-83 and the schematic diagram on pages 5-79 and 5-80.


IC-31
IC-32
IC-2
IC-3
IC-4
IC-9
IC-5
IC-6
IC-49
IC-7
IC-8
IC-12
IC-13
IC-14
IC-15
IC-16
IC-17
IC-18
IC-19
IC-20
IC-21
IC-45
IC-47
IC-27
ADDR = 3000 TO 3 FFFH
ADDR = 0 TO 7 FFH
ADDR = 9000 TO 9005H
ADDR = 0B0H
KEYBOARD DIP SOCKET
TRANSMIT SIGNAL ELEMENT TIMING J3-22
DATA TERM READY J3-14
REQ TO CLR J3-7
TRANSMITTED DATA J3-3
RECEIVED LINE SIGNAL DETECTOR J3-15
DATA SET READY J3-11
CLR TO SEND J3-9
RECEIVED DATA J3-5
SIGNAL GND J3-13
J3-26
RS-232-C
CHASSIS GND
99 98 JUMPER
A
B
C D E F G
H I J
K L



IC No.	Part No.
1	DP8350
2	INS8080-1
3	DP8228
4	DP8224
5	INS8250
6, 38, 49	MM2716
7	DM74148
8	DP8212
9, 31, 32	DM81LS95
10	DM74LS365
12 to 19	MM5257
20, 22, 30	DM74LS74
21	DM74LS73
23	DM74LS86
24, 27	DM74LS32
25	DM74LS08
26	DM74LS04
33	MM5034
37	DM74LS373
39	DM74166
42	DM74C00
45	DS1488
46	DS1489
47	DM74LS00
48	LM555

All pull-up resistors = 4.7k 1/4W

CONTROL FUNCTIONS SUMMARY

Functions	On-Line / Local	Remarks
Cursor Move/Control		
Line feed	0A / 0A	
Carriage return	0D / 0D	
Tab	09 / 09	
Cursor up	7E, 0C / 0C	
Cursor down	7E, 0B / 0B	
Cursor left	08 / 08	
Cursor right	10 / 10	
Home	7E, 12 / 12	
Home and clear	7E, 1C / 1C	
Enable cursor	7E, 03 / 03	
Disable cursor	7E, 06 / 06	
Address cursor	7E, 11, X, Y /	Remote only
Read cursor	7E, 05 / 05	
Insert		
Character insert	7E, 1E / 1E	
Line insert	7E, 1A / 1A	
Line insert with range	7E, 1D,49,Y	Remote only
Delete		
Character strip	7E, 04 / 04	
Character delete	7F / 7F	
Line delete	7E, 13 / 13	
Line delete with range	7E, 1D,53,Y /	Remote only
Clear to end of line	7E, 0F / 0F	
Clear to end of page	7E, 17 / 17	
Miscellaneous		
Local/remote	/ 00	Local only
Upper/lower case	/ 7E	Local only
Next page	7E, 0E / 0E	
Keyboard lock	7E, 15 / 15	
Keyboard unlock	7E, 03 / 03	
Bell	07 /	Remote only
Special Functions		
Function menu	/ 1D	A summary of available functions and their corresponding codes (local mode only).
Graphics on	7E, 02 / 02	Enter graphics mode.
Graphics off	7E, 1B / 1B	Exit graphics mode.
Graphics menu	/ 11	Line 23 displays upper and lower case characters and line 24 the corresponding graphics symbols (local).
Line transmit	7E, 14 / 14	Transmits the cursor line and inverts its attributes.
Foreground follows	7E, 1F / 1F	
Background follows	7E, 19 / 19	
Clear foreground	7E, 18 / 18	
Scale	/ 07	The line above the cursor becomes a scale (1-80). This is an aid for graphics and text alignment (local).
Roll up	7E, 01 / 01	
Roll down	7E, 16 / 16	

CHARACTER GENERATOR HEX DUMP

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	14	14	14	14	14	14	14	14	14	14	0	0	0	0	0	0
10	0	0	0	7C	7C	7C	1C	1C	1C	1C	0	0	0	0	0	0
20	1C	1C	1C	1C	1C	1C	1C	1C	1C	1C	0	0	0	0	0	0
30	14	8	14	8	14	8	14	8	14	8	0	0	0	0	0	0
40	0	0	0	55	2A	55	0	0	0	0	0	0	0	0	0	0
50	0	0	0	7F	7F	7F	0	0	0	0	0	0	0	0	0	0
60	1C	1C	1C	7C	7C	7C	0	0	0	0	0	0	0	0	0	0
70	1C	1C	1C	1F	1F	1F	0	0	0	0	0	0	0	0	0	0
80	1C	1C	1C	7F	7F	7F	0	0	0	0	0	0	0	0	0	0
90	1C	1C	1C	7C	7C	7C	1C	1C	1C	1C	0	0	0	0	0	0
A0	1C	1C	1C	1F	1F	1F	1C	1C	1C	1C	0	0	0	0	0	0
B0	1C	1C	1C	7F	7F	7F	1C	1C	1C	1C	0	0	0	0	0	0
C0	0	0	0	7F	7F	7F	1C	1C	1C	1C	0	0	0	0	0	0
D0	0	0	0	1F	1F	1F	1C	1C	1C	1C	0	0	0	0	0	0
E0	1	3	7	E	C	18	38	70	60	40	0	0	0	0	0	0
F0	40	60	70	38	18	C	E	7	3	1	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
100	0	0	8	1C	1C	3E	3E	3E	0	0	0	0	0	0	0	0
110	0	0	0	0	78	8	8	8	8	8	0	0	0	0	0	0
120	8	8	8	8	8	8	8	8	8	8	0	0	0	0	0	0
130	0	0	3E	22	22	22	22	3E	0	0	0	0	0	0	0	0
140	0	0	8	1C	3E	1C	8	0	0	0	0	0	0	0	0	0
150	0	0	0	0	7F	0	0	0	0	0	0	0	0	0	0	0
160	8	8	8	8	78	0	0	0	0	0	0	0	0	0	0	0
170	8	8	8	8	F	0	0	0	0	0	0	0	0	0	0	0
180	8	8	8	8	7F	0	0	0	0	0	0	0	0	0	0	0
190	8	8	8	8	78	8	8	8	8	8	0	0	0	0	0	0
1A0	8	8	8	8	F	8	8	8	8	8	0	0	0	0	0	0
1B0	8	8	8	8	7F	8	8	8	8	8	0	0	0	0	0	0
1C0	0	0	0	0	7F	8	8	8	8	8	0	0	0	0	0	0
1D0	0	0	0	0	F	8	8	8	8	8	0	0	0	0	0	0
1E0	1	2	2	4	8	8	10	20	20	40	0	0	0	0	0	0
1F0	40	20	20	10	8	8	4	2	2	1	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
200	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
210	0	8	8	8	8	8	0	8	0	0	0	0	0	0	0	0
220	A	A	14	0	0	0	0	0	0	0	0	0	0	0	0	0
230	0	0	14	3E	14	3E	14	0	0	0	0	0	0	0	0	0
240	0	8	1E	28	1C	A	3C	8	0	0	0	0	0	0	0	0
250	0	32	32	4	8	10	26	26	0	0	0	0	0	0	0	0
260	0	8	14	14	18	2A	24	1A	0	0	0	0	0	0	0	0
270	8	8	10	0	0	0	0	0	0	0	0	0	0	0	0	0
280	0	8	10	20	20	20	10	8	0	0	0	0	0	0	0	0
290	0	8	4	2	2	2	4	8	0	0	0	0	0	0	0	0
2A0	0	8	2A	1C	2A	8	0	0	0	0	0	0	0	0	0	0
2B0	0	0	8	8	3E	8	8	0	0	0	0	0	0	0	0	0
2C0	0	0	0	0	0	0	8	8	10	0	0	0	0	0	0	0
2D0	0	0	0	0	3E	0	0	0	0	0	0	0	0	0	0	0
2E0	0	0	0	0	0	0	0	8	0	0	0	0	0	0	0	0
2F0	0	2	2	4	8	10	20	20	0	0	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
300	0	1C	22	26	2A	32	22	1C	0	0	0	0	0	0	0	0
310	0	8	18	8	8	8	8	3E	0	0	0	0	0	0	0	0
320	0	1C	22	2	C	10	20	3E	0	0	0	0	0	0	0	0
330	0	3E	2	4	C	2	22	1C	0	0	0	0	0	0	0	0
340	0	4	C	14	24	3E	4	4	0	0	0	0	0	0	0	0
350	0	3E	20	3C	2	2	22	1C	0	0	0	0	0	0	0	0
360	0	1C	22	20	3C	22	22	1C	0	0	0	0	0	0	0	0
370	0	3E	22	2	4	8	8	8	0	0	0	0	0	0	0	0
380	0	1C	22	22	1C	22	22	1C	0	0	0	0	0	0	0	0
390	0	1C	22	22	1E	2	2	1C	0	0	0	0	0	0	0	0
3A0	0	0	0	8	0	0	8	0	0	0	0	0	0	0	0	0
3B0	0	0	0	8	0	0	8	8	10	0	0	0	0	0	0	0
3C0	0	4	8	10	20	10	8	4	0	0	0	0	0	0	0	0
3D0	0	0	0	3E	0	3E	0	0	0	0	0	0	0	0	0	0
3E0	0	10	8	4	2	4	8	10	0	0	0	0	0	0	0	0
3F0	0	1C	22	2	4	8	0	8	0	0	0	0	0	0	0	0

CHARACTER GENERATOR HEX DUMP (Continued)

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
400	0	1C	22	2E	2A	2E	20	1E	0	0	0	0	0	0	0	0
410	0	1C	22	22	3E	22	22	22	0	0	0	0	0	0	0	0
420	0	3C	22	22	3C	22	22	3C	0	0	0	0	0	0	0	0
430	0	1C	22	20	20	20	22	1C	0	0	0	0	0	0	0	0
440	0	3C	22	22	22	22	22	3C	0	0	0	0	0	0	0	0
450	0	3E	20	20	3C	20	20	3E	0	0	0	0	0	0	0	0
460	0	3E	20	20	3C	20	20	20	0	0	0	0	0	0	0	0
470	0	1C	22	20	20	2E	22	1E	0	0	0	0	0	0	0	0
480	0	22	22	22	3E	22	22	22	0	0	0	0	0	0	0	0
490	0	1C	8	8	8	8	8	1C	0	0	0	0	0	0	0	0
4A0	0	1E	4	4	4	4	24	18	0	0	0	0	0	0	0	0
4B0	0	22	24	28	30	28	24	22	0	0	0	0	0	0	0	0
4C0	0	20	20	20	20	20	20	3E	0	0	0	0	0	0	0	0
4D0	0	22	36	2A	2A	22	22	22	0	0	0	0	0	0	0	0
4E0	0	22	22	32	2A	26	22	22	0	0	0	0	0	0	0	0
4F0	0	1C	22	22	22	22	22	1C	0	0	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
500	0	3C	22	22	3C	20	20	20	0	0	0	0	0	0	0	0
510	0	1C	22	22	22	2A	24	1A	0	0	0	0	0	0	0	0
520	0	3C	22	22	3C	28	24	22	0	0	0	0	0	0	0	0
530	0	1C	22	20	1C	2	22	1C	0	0	0	0	0	0	0	0
540	0	3E	8	8	8	8	8	8	0	0	0	0	0	0	0	0
550	0	22	22	22	22	22	22	1C	0	0	0	0	0	0	0	0
560	0	22	22	22	14	14	8	8	0	0	0	0	0	0	0	0
570	0	22	22	22	2A	2A	2A	14	0	0	0	0	0	0	0	0
580	0	22	22	14	8	14	22	22	0	0	0	0	0	0	0	0
590	0	22	22	22	1C	8	8	8	0	0	0	0	0	0	0	0
5A0	0	3E	2	4	8	10	20	3E	0	0	0	0	0	0	0	0
5B0	0	E	8	8	8	8	8	E	0	0	0	0	0	0	0	0
5C0	0	20	20	10	8	4	2	2	0	0	0	0	0	0	0	0
5D0	0	38	8	8	8	8	8	38	0	0	0	0	0	0	0	0
5E0	0	8	1C	2A	8	8	8	8	0	0	0	0	0	0	0	0
5F0	0	0	8	10	3E	10	8	0	0	0	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
600	10	8	4	0	0	0	0	0	0	0	0	0	0	0	0	0
610	0	0	0	1C	2	1E	22	1E	0	0	0	0	0	0	0	0
620	0	20	20	20	3C	22	22	3C	0	0	0	0	0	0	0	0
630	0	0	0	1E	20	20	20	1E	0	0	0	0	0	0	0	0
640	0	2	2	2	1E	22	22	1E	0	0	0	0	0	0	0	0
650	0	0	0	1C	22	3E	20	1C	0	0	0	0	0	0	0	0
660	0	4	8	8	1C	8	8	8	0	0	0	0	0	0	0	0
670	0	0	0	1E	22	22	1E	2	1C	0	0	0	0	0	0	0
680	0	20	20	20	3C	22	22	22	0	0	0	0	0	0	0	0
690	0	8	0	18	8	8	8	1C	0	0	0	0	0	0	0	0
6A0	0	4	0	4	4	4	24	18	0	0	0	0	0	0	0	0
6B0	0	10	10	12	14	18	14	12	0	0	0	0	0	0	0	0
6C0	0	18	8	8	8	8	8	1C	0	0	0	0	0	0	0	0
6D0	0	0	0	36	2A	2A	2A	2A	0	0	0	0	0	0	0	0
6E0	0	0	0	3C	22	22	22	22	0	0	0	0	0	0	0	0
6F0	0	0	0	1C	22	22	22	1C	0	0	0	0	0	0	0	0

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
700	0	0	0	3C	22	22	3C	20	20	0	0	0	0	0	0	0
710	0	0	0	1E	22	22	1E	2	2	0	0	0	0	0	0	0
720	0	0	0	16	18	10	10	10	0	0	0	0	0	0	0	0
730	0	0	0	1E	20	1C	2	3C	0	0	0	0	0	0	0	0
740	0	8	8	1C	8	8	8	4	0	0	0	0	0	0	0	0
750	0	0	0	22	22	22	22	1C	0	0	0	0	0	0	0	0
760	0	0	0	22	22	22	14	8	0	0	0	0	0	0	0	0
770	0	0	0	22	22	2A	2A	14	0	0	0	0	0	0	0	0
780	0	0	0	22	14	8	14	22	0	0	0	0	0	0	0	0
790	0	0	0	22	22	22	1E	2	1C	0	0	0	0	0	0	0
7A0	0	0	0	3E	4	8	10	3E	0	0	0	0	0	0	0	0
7B0	6	8	8	10	20	10	8	8	6	0	0	0	0	0	0	0
7C0	0	8	8	8	0	8	8	8	0	0	0	0	0	0	0	0
7D0	30	8	8	4	2	4	8	8	30	0	0	0	0	0	0	0
7E0	0	0	0	7F	0	7F	0	0	0	0	0	0	0	0	0	0
7F0	0	1C	3E	36	22	22	36	3E	1C	0	0	0	0	0	0	0

```
 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    1
CRT801

                                TITLE CRT801
                        ;May 1980
 0000'                  ASEG
                        ORG     00000h
                        ;constants
 000A                   LF      equ     0Ah
 000D                   CR      equ     0Dh
 0020                   SPC     equ     020h
 007E                   LINC    equ     07Eh    ;leadin code
 0060                   RWRG    equ     low RR48-low RR1+2
 0003                   KULCDE  equ     03h     ;kbd unlock code
                        ;I/O ports
 0080                   KBDPRT  equ     080h    ;keyboard
 0040                   ROWPRT  equ     040h    ;row interrupt
 0040                   VERPRT  equ     040h    ;vertical interrupt
 0040                   SETSW   equ     040h    ;baud sel,autolf,u/lcase
 0002                   LCLIND  equ     2       ;local indicator
 0001                   BELPRT  equ     1       ;bell
                        ;ace
 9000                   ACEDTA  equ     09000h  ;data
 9001                   ACEITR  equ     ACEDTA+1;interrupt mask
 9003                   ACECTL  equ     ACEDTA+3;control
 9005                   ACESTU  equ     ACEDTA+5;transmit status

                        ;ram assignment
 3FFF                   FROWH   equ     03FFFh  ;first row reg pair
 3FFE                   FROW    equ     FROWh-1 ;
 3FFD                   LROWH   equ     FROWh-2 ;last row reg pair
 3FFC                   LROW    equ     FROWh-3 ;
 3FFB                   CROWH   equ     FROWh-4 ;cursor row reg pair
 3FFA                   CROW    equ     FROWh-5 ;
 3FF9                   CURH    equ     CROW-1  ;cursor reg pair
 3FF8                   CUR     equ     CROW-2  ;
 3FF7                   TOPH    equ     CUR-1   ;top of page reg pair
 3FF6                   TOP     equ     CUR-2   ;
 3FF5                   NRW     equ     TOP-1   ;row counter
 3FF4                   VCALEN  equ     TOP-2   ;vert calc routine enable
 3FF3                   GSYMBL  equ     VCALEN-1;graphics symbol
 3FF2                   AULF    equ     GSYMBL-1;auto linefeed,0=auto lf
 3FF1                   LOCLM   equ     AULF-1  ;local mode,0=remote
 3FF0                   ULCASE  equ     AULF-2  ;upper/lower case,0=lower
 3FEF                   GECNTL  equ     AULF-3  ;graphic enable,0=disable
 3FEE                   KBDLCK  equ     AULF-4  ;keyboard lock,0=unlock
 3FED                   RTECTL  equ     KBDLCK-1;cursor blink rate cntl
 3FEC                   CUREN   equ     KBDLCK-2;cursor enable,0=off
 3FEB                   CURTMR  equ     KBDLCK-3;cursor blinking timer
 3FEA                   FFWCT   equ     KBDLCK-4;ace fifo word count
 3FE9                   LEADIN  equ     KBDLCK-5;leadin mode,0=no leadin

 3FE8                   ICMD    equ     KBDLCK-6;insert char mode,0=insert
 3FE7                   CPYCTL  equ     ICMD-1  ;row copy direction cntl
 3FE6                   FFWRT   equ     CPYCTL-1;fifo write pointer
 3FE5                   FFRD    equ     CPYCTL-2;fifo read pointer
 3FE5                   STK     equ     FFRD    ;stack      3FE4h down
 3FA3                   LINP    equ     FFEND+4 ;leadin parameter storage
 3FA2                   LINWCT  equ     FFEND+3 ;leadin word count

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    2
CRT801
 3FA1                   LINFH   equ     FFEND+2 ;leadin func jmp addr high
 3FA0                   LINF    equ     FFEND+1 ;leadin func jmp addr low
 3F9F                   FFEND   equ     03F9Fh  ;ace fifo end
 3F50                   FFSTRT  equ     03F50h  ;ace fifo start 3F50/3F9Fh
 3F20                   FBG     equ     03F20h  ;fore/background cntl
 3F00                   DMYROW  equ     03F00h  ;dummy row  3F00/3F4Fh
 3780                   FCHR2   equ     03780h  ;page 2, 1st char

                        ;INTERRUPTS
                        ;*********************************************
 0000   F3              START:  DI                      ;restart 0
 0001   21 3F00                LXI     H,DMYROW        ;clr non video ram
 0004   F9                     SPHL
 0005   C3 00E2                JMP     INIT
                        ;---------------------------------------
                        ;row interrupt
 0008   F5              ROW:    PUSH    PSW             ;restart 1
 0009   0C                     INR     C
 000A   C2 0066                JNZ     NOWRAP          ;no wrap arroud
 000D   C3 0061                JMP     VRWRAP          ;do wrap arround
                        ;---------------------------------------
                        ;vertical interrupt
 0010   E5              VERT:   PUSH    H               ;restart 2
 0011   21 3FF5                LXI     H,NRW
 0014   4E                     MOV     C,M             ;load NRW
 0015   C3 07AE                JMP     VTSUB
                        ;---------------------------------------
```

```
                        ;ace duplicate interrupt
0018    C3 0038         ACEDUP: JMP     ACE             ;restart 3
                        ;{FUNCTION} disable cursor
001B    21 3FEC         DICUR:  LXI     H,CUREN         ;disable cursor
001E    77                      MOV     M,A             ;a=0
001F    C9                      RET
                        ;---------------------------------------
                        ;keyboard interrupt
0020    E5              KBD:    PUSH    H               ;restart 4
0021    F5                      PUSH    PSW
0022    21 3FEE                 LXI     H,KBDLCK        ;keyboard lock cntl
0025    C3 02C9                 JMP     KBDINT
                        ;---------------------------------------
                        ;row duplicate interrupt
0028    F5              ROWDP:  PUSH    PSW             ;restart 5
0029    0C                      INR     C
002A    C2 0066                 JNZ     NOWRAP
002D    C3 0061                 JMP     VRWRAP
                        ;---------------------------------------
                        ;vertical duplicate interrupt
0030    C3 0010         VERTDP: JMP     VERT            ;restart 6
0033    EB              TABSTP: XCHG                    ;hl=crow
0034    D1                      POP     D               ;remove call
0035    D1                      POP     D
0036    73                      MOV     M,E             ;return org crow
0037    C9                      RET
                        ;---------------------------------------
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    3
CRT801
 0038
                        ;ACE INTERRUPT
                        ;***********************************************
0038    E5              ACE:    PUSH    H
0039    F5                      PUSH    PSW
003A    21 3FEB                 LXI     H,CURTMR
003D    D5                      PUSH    D
003E    AF                      XRA     A
003F    77                      MOV     M,A     ;reset cursor timer
0040    2B                      DCX     H       ;FFWCT
0041    34                      INR     M       ;fifo empty?
0042    C2 0244                 JNZ     STFIFO  ;no, store to fifo

0045    2B                      DCX     H       ;leadin
0046    B6                      ORA     M
0047    3A 9000                 LDA     ACEDTA  ;read ace
004A    FB                      EI
004B    C2 0283                 JNZ     LINMDE  ;leadin mode

004E    E6 7F           FIFACE: ANI     07Fh
0050    11 0267                 LXI     D,FFCHK
0053    D5                      PUSH    D       ;pseudo call
0054    FE 0A                   CPI     LF
0056    CA 03B1                 JZ      LFEED
0059    CD 015C                 CALL    CALJMP
005C    E6 87                   ANI     087h    ;leadin+jmp addr high
005E    F8                      RM              ;leadin required, return
005F    67              LCLFUN: MOV     H,A     ;jmp addr high
0060    E9                      PCHL            ;do function


                        ;row interrupt continue
                        ;***********************************************
0061    3E 01           VRWRAP: MVI     A,1
0063    32 5000                 STA     05000h  ;wrap arround addr
0066    D3 40           NOWRAP: OUT     ROWPRT  ;clr row flip/flop
0068    F1                      POP     PSW
0069    FB                      EI
006A    C9                      RET


                        ;WRITE TO ACE
                        ;***********************************************
006B    3E 0D           SNDCR:  MVI     A,CR
006D    57              WTACEA: MOV     D,A

006E    3A 9005         WTACED: LDA     ACESTU  ;check status
0071    FE 60                   CPI     060h    ;hold/tx register
0073    DA 006E                 JC      WTACED  ;not ready
0076    CD 075E                 CALL    $DLY    ;delay

0079    7A              OUTACE: MOV     A,D
007A    32 9000                 STA     ACEDTA  ;write to ace
007D    C9                      RET
                        PAGE
```

```
 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    4
CRT801
  007E
                        ;ROW START LOOKUP TABLE     (start addr=7Eh)
                        ;*********************************************
  007E    3EB0          ROW47D: dw      03EB0h
  0080    3000          ROW48D: dw      03000h
  0082    3050          ROW1:   dw      03050h
  0084    30A0          ROW2:   dw      030A0h
  0086    30F0          ROW3:   dw      030F0h
  0088    3140          ROW4:   dw      03140h
  008A    3190          ROW5:   dw      03190h
  008C    31E0          ROW6:   dw      031E0h
  008E    3230          ROW7:   dw      03230h
  0090    3280          ROW8:   dw      03280h
  0092    32D0          ROW9:   dw      032D0h
  0094    3320          ROW10:  dw      03320h
  0096    3370          ROW11:  dw      03370h
  0098    33C0          ROW12:  dw      033C0h
  009A    3410          ROW13:  dw      03410h
  009C    3460          ROW14:  dw      03460h
  009E    34B0          ROW15:  dw      034B0h
  00A0    3500          ROW16:  dw      03500h
  00A2    3550          ROW17:  dw      03550h
  00A4    35A0          ROW18:  dw      035A0h
  00A6    35F0          ROW19:  dw      035F0h
  00A8    3640          ROW20:  dw      03640h
  00AA    3690          ROW21:  dw      03690h
  00AC    36E0          ROW22:  dw      036E0h
  00AE    3730          ROW23:  dw      03730h
  00B0    3780          ROW24:  dw      03780h
  00B2    37D0          ROW25:  dw      037D0h
  00B4    3820          ROW26:  dw      03820h
  00B6    3870          ROW27:  dw      03870h
  00B8    38C0          ROW28:  dw      038C0h
  00BA    3910          ROW29:  dw      03910h
  00BC    3960          ROW30:  dw      03960h
  00BE    39B0          ROW31:  dw      039B0h
  00C0    3A00          ROW32:  dw      03A00h
  00C2    3A50          ROW33:  dw      03A50h
  00C4    3AA0          ROW34:  dw      03AA0h
  00C6    3AF0          ROW35:  dw      03AF0h
  00C8    3B40          ROW36:  dw      03B40h
  00CA    3B90          ROW37:  dw      03B90h
  00CC    3BE0          ROW38:  dw      03BE0h
  00CE    3C30          ROW39:  dw      03C30h
  00D0    3C80          ROW40:  dw      03C80h
  00D2    3CD0          ROW41:  dw      03CD0h
  00D4    3D20          ROW42:  dw      03D20h
  00D6    3D70          ROW43:  dw      03D70h
  00D8    3DC0          ROW44:  dw      03DC0h
  00DA    3E10          ROW45:  dw      03E10h
  00DC    3E60          ROW46:  dw      03E60h
  00DE    3EB0          ROW47:  dw      03EB0h
  00E0    3F00          ROW48:  dw      03F00h
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    5
CRT801
  00E2
                        ;INITIALIZE
                        ;*********************************************
  00E2    3E 20         INIT:   MVI     A,SPC   ;space
  00E4    16 E9                 MVI     D,low LEADIN;byte count
  00E6    CD 04C7               CALL    DRLLP   ;store spaces
  00E9    AF                    XRA     A
  00EA    32 3FA2               STA     LINWCT  ;zero leadin word count
  00ED    16 17                 MVI     D,256-low LEADIN;byte count
  00EF    CD 04C7               CALL    DRLLP   ;store zeros
  00F2    31 3FE7               LXI     SP,STK+2
  00F5    21 5050               LXI     H,05050h
  00F8    E5                    PUSH    H       ;set up fifo rd/wrt ptrs
  00F9    CD 04AE               CALL    CURULK  ;enable cursor,unlock kbd
  00FC    32 3FEA               STA     FFWCT   ;zero fifo word count(FFh)
  00FF    23                    INX     H       ;RTECTL
  0100    36 1C                 MVI     M,01Ch  ;cursor blink cntl
  0102    2E FC                 MVI     L,low LROW;last row
  0104    36 B0                 MVI     M,low RR24
  0106    2E FE                 MVI     L,low FROW;first row
  0108    36 82                 MVI     M,low RR1
  010A    DB 80                 IN      KBDPRT  ;clear keyboard intr
  010C    CD 04CE               CALL    CLRSCN  ;clear screen
  010F    CD 07BF               CALL    ACESW   ;init ace, read setsw
  0112    3E 3F         PATTN:  MVI     A,03Fh
  0114    21 3780               LXI     H,FCHR2 ;1st byte of page 2
  0117    75            PTNLP:  MOV     M,L     ;write pattern
  0118    23                    INX     H
  0119    BC                    CMP     H
```

```
011A    C2 0117             JNZ     PTNLP
011D    D3 01               OUT     BELPRT  ;ring bell for ready

                    ;CALCULATE SCREEN ADDR AFTER VERTICAL INTERRUPT
011F    2E EB       VCAL:   MVI     L,low CURTMR
0121    7E                  MOV     A,M
0122    2F                  CMA
0123    34                  INR     M       ;cursor timer
0124    23                  INX     H       ;cursor enable
0125    A6                  ANA     M
0126    23                  INX     H       ;rate cntl
0127    A6                  ANA     M       ;blink rate mask
0128    C4 0174             CNZ     CURLOC  ;cursor on
012B    3E 20               MVI     A,020h  ;8350 offset
012D    84                  ADD     H       ;offset addr high
012E    67                  MOV     H,A     ;=5Fh if cursor off
012F    E5                  PUSH    H       ;save cursor
0130    2A 3FFE             LHLD    FROW
0133    2B                  DCX     H       ;fetch row start
0134    7E                  MOV     A,M
0135    C6 20               ADI     020h    ;offset addr high
0137    57                  MOV     D,A
0138    2B                  DCX     H
                    PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    6
CRT801
  0139
0139    5E                  MOV     E,M     ;de=top of page
013A    7D                  MOV     A,L     ;calc row wrap constant
013B    0F                  RRC             ;divide by 2
013C    C6 8F               ADI     08Fh    ;add offset
013E    E1                  POP     H       ;cursor location
013F    F3                  DI
0140    22 3FF8             SHLD    CUR     ;update cursor
0143    EB                  XCHG
0144    22 3FF6             SHLD    TOP     ;update top of page
0147    21 3FF5             LXI     H,NRW
014A    77                  MOV     M,A     ;row wrap constant
014B    2B                  DCX     H       ;VCALEN
014C    36 00               MVI     M,0     ;disable VCAL routine
014E    FB          WAIT:   EI
014F    76                  HLT
0150    7E                  MOV     A,M     ;VCALEN
0151    B7                  ORA     A       ;check from vert intr
0152    CA 014E             JZ      WAIT    ;no
0155    C3 011F             JMP     VCAL    ;do screen calculations

                    ;CALCULATE JMP ADDR
0158    2E E9       CJMP:   MVI     L,low LEADIN
015A    E6 7F               ANI     07Fh    ;mask 1st bit
015C    FE 20       CALJMP: CPI     SPC
015E    DA 0168             JC      FUNC    ;0-1Fh, func
0161    FE 7E               CPI     07Eh
0163    DA 0372             JC      CHAR    ;20-7Dh, char input
0166    D6 5E               SUI     05Eh    ;7E/7Fh to 20/21h
0168    2B          FUNC:   DCX     H       ;insert mode
0169    74                  MOV     M,H     ;h<>0,defeat insert mode
016A    07          JMPADD: RLC             ;*2, msb=0
016B    5F                  MOV     E,A     ;d=02h (jmp tbl)
016C    1A                  LDAX    D       ;fetch jmp addr low
016D    6F                  MOV     L,A
016E    13                  INX     D
016F    1A                  LDAX    D       ;fetch jmp addr high
0170    C9                  RET

                    ;CALCULATE CUR LOC AND CUR TO END DIFF
0171    3E 50       DFCLOC: MVI     A,80
0173    90                  SUB     B       ;cursor to end difference

                    ;CALCULATE CURSOR LOCATION
0174    2A 3FFA     CURLOC: LHLD    CROW
0177    2B                  DCX     H
0178    56                  MOV     D,M
0179    2B                  DCX     H
017A    5E                  MOV     E,M
017B    68                  MOV     L,B
017C    19                  DAD     D       ;hl=cursor address
017D    C9                  RET
                    PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    7
CRT801
  017E
                    ;ROW WRAP AROUND LOOKUP TABLE   (start addr=17Eh)
                    ;***********************************************
017E    00E0        RR47D:  dw      00E0h
0180    0082        RR48D:  dw      0082h
0182    0084        RR1:    dw      0084h
```

```
0184    0086          RR2:    dw      0086h
0186    0088          RR3:    dw      0088h
0188    008A          RR4:    dw      008Ah
018A    008C          RR5:    dw      008Ch
018C    008E          RR6:    dw      008Eh
018E    0090          RR7:    dw      0090h
0190    0092          RR8:    dw      0092h
0192    0094          RR9:    dw      0094h
0194    0096          RR10:   dw      0096h
0196    0098          RR11:   dw      0098h
0198    009A          RR12:   dw      009Ah
019A    009C          RR13:   dw      009Ch
019C    009E          RR14:   dw      009Eh
019E    00A0          RR15:   dw      00A0h
01A0    00A2          RR16:   dw      00A2h
01A2    00A4          RR17:   dw      00A4h
01A4    00A6          RR18:   dw      00A6h
01A6    00A8          RR19:   dw      00A8h
01A8    00AA          RR20:   dw      00AAh
01AA    00AC          RR21:   dw      00ACh
01AC    00AE          RR22:   dw      00AEh
01AE    00B0          RR23:   dw      00B0h
01B0    00B2          RR24:   dw      00B2h
01B2    00B4          RR25:   dw      00B4h
01B4    00B6          RR26:   dw      00B6h
01B6    00B8          RR27:   dw      00B8h
01B8    00BA          RR28:   dw      00BAh
01BA    00BC          RR29:   dw      00BCh
01BC    00BE          RR30:   dw      00BEh
01BE    00C0          RR31:   dw      00C0h
01C0    00C2          RR32:   dw      00C2h
01C2    00C4          RR33:   dw      00C4h
01C4    00C6          RR34:   dw      00C6h
01C6    00C8          RR35:   dw      00C8h
01C8    00CA          RR36:   dw      00CAh
01CA    00CC          RR37:   dw      00CCh
01CC    00CE          RR38:   dw      00CEh
01CE    00D0          RR39:   dw      00D0h
01D0    00D2          RR40:   dw      00D2h
01D2    00D4          RR41:   dw      00D4h
01D4    00D6          RR42:   dw      00D6h
01D6    00D8          RR43:   dw      00D8h
01D8    00DA          RR44:   dw      00DAh
01DA    00DC          RR45:   dw      00DCh
01DC    00DE          RR46:   dw      00DEh
01DE    00E0          RR47:   dw      00E0h
01E0    0082          RR48:   dw      0082h
01E2    0084          RR1D:   dw      0084h

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    8
CRT801
                      ;JUMP ADDRESS CONSTANTS
                      ;**********************************************
                      ;A15     :- 0=no leadin required
                      ;A14/A12:- parameter count
                      ;A11     :- 0=local function
 1000                 W1      equ     01000h  ;one para adder
 2000                 W2      equ     02000h  ;two para adder
 8000                 LIN     equ     08000h  ;leadin adder
 0800                 NLC     equ     00800h  ;not local adder

 0A5F                 F1      equ     RTN+NLC
 03B9                 F2      equ     CARRTN
 03B1                 F3      equ     LFEED
 0C34                 F4      equ     BELL+NLC
 060A                 F5      equ     TAB
 0437                 F6      equ     FS
 041F                 F7      equ     BS

 844E                 F8      equ     UPCUR+LIN
 8460                 F9      equ     DWNCUR+LIN
 84D8                 F10     equ     HOMCUR+LIN
 85F3                 F11     equ     NPAGE+LIN
 8472                 F12     equ     ROLUP+LIN
 848C                 F13     equ     ROLDWN+LIN

 84AE                 F14     equ     CURULK+LIN
 8DD1                 F15     equ     RDCUR+LIN+NLC
 ADA2                 F16     equ     ADDCUR+LIN+NLC+W2

 84F1                 F17     equ     FGNDF+LIN
 84F7                 F18     equ     BGNDF+LIN

 836B                 F19     equ     INSCHAR+LIN
 8358                 F20     equ     STOFCH+LIN
 8505                 F21     equ     INSLNE+LIN
 8512                 F22     equ     STOFLNE+LIN
 AD26                 F23     equ     ISLRG+LIN+NLC+W2
 9E8A                 F24     equ     GRAPH+LIN+NLC+W1
```

```
0419                    F25     equ     DEL
83DB                    F26     equ     DCROW+LIN
84C0                    F27     equ     DRTLN+LIN
84BA                    F28     equ     DRTPG+LIN
8642                    F29     equ     CFB+LIN
84CE                    F30     equ     CLRSCN+LIN

8CB6                    F31     equ     KBLK+LIN+NLC
801B                    F32     equ     DICUR+LIN
871D                    F33     equ     SNDLNE+LIN
87BF                    F34     equ     ACESW+LIN
0AC5                    F35     equ     LINSET+NLC
86BC                    F36     equ     DEGRPH+LIN
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    9
CRT801
  01E4
                        ;PUT A WORD TO ACE
  01E4    57            KBDACE: MOV     D,A
  01E5    3A 9005               LDA     ACESTU
  01E8    E6 20                 ANI     020h
  01EA    CA 01E5               JZ      KBDACE+1;not ready
  01ED    C3 0079               JMP     OUTACE

                        ;ACE BAUD RATE CONSTANTS
  01F0    06AB          B110:   dw      1707    ;       0
  01F2    0139          B600:   dw      313     ;       1
  01F4    009C          B1200:  dw      156     ;0.3%   2
  01F6    004E          B2400:  dw      78      ;0.3%   3
  01F8    0027          B4800:  dw      39      ;0.3%   4
  01FA    0014          B9600:  dw      20      ;2.3%   5
  01FC    000A          B19200: dw      10      ;2.3%   6
  01FE    0005          B38400: dw      5       ;2.3%   7

                        ;FUNCTION JUMP TABLE    (start addr=200h)
                        ;*********************************************
  0200    0A5F          TBLJMP: dw      F1      ;null/toggle local
  0202    8472                  dw      F12     ;A:roll up
  0204    9E8A          CB:     dw      F24     ;B:graphics mode
  0206    84AE                  dw      F14     ;C:on cursor/unlock kbd
  0208    8358                  dw      F20     ;D:strip off character
  020A    8DD1          CE:     dw      F15     ;E:read cursor
  020C    801B                  dw      F32     ;F:disable cursor
  020E    0C34          CG:     dw      F4      ;G:bell/scale
  0210    041F                  dw      F7      ;H:cursor left
  0212    060A                  dw      F5      ;I:tab
  0214    03B1                  dw      F3      ;J:line feed
  0216    8460                  dw      F9      ;K:cursor down
  0218    844E                  dw      F8      ;L:cursor up
  021A    03B9                  dw      F2      ;M:carriage return
  021C    85F3                  dw      F11     ;N:next page
  021E    84C0                  dw      F27     ;O:delete rest of line
  0220    0437                  dw      F6      ;P:cursor right
  0222    ADA2          CQ:     dw      F16     ;Q:address cursor/menu
  0224    84D8                  dw      F10     ;R:home cursor
  0226    8512                  dw      F22     ;S:strip off a line
  0228    871D                  dw      F33     ;T:transmit a line
  022A    8CB6          CU:     dw      F31     ;U:lock keyboard
  022C    84BC                  dw      F13     ;V:roll down
  022E    84BA                  dw      F28     ;W:delete rest of page
  0230    8642                  dw      F29     ;X:clear fore/background
  0232    84F7                  dw      F18     ;Y:background follows
  0234    8505                  dw      F21     ;Z:insert line
  0236    86BC                  dw      F36     ;1B:esc/defeat graphics
  0238    84CE                  dw      F30     ;1C:home and clear screen
  023A    AD26          C1D:    dw      F23     ;1D:insert/strip lne/rng
  023C    836B                  dw      F19     ;1E:insert character
  023E    84F1                  dw      F17     ;1F:foreground follows
  0240    0AC5          C7E:    dw      F35     ;7E:leadin/ace,u/l-case
  0242    0419                  dw      F25     ;7F:delete

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    10
CRT801
                        ;STORE A WORD TO ACE FIFO
  0244    3E 50         STFIFO: MVI     A,80
  0246    BE                    CMP     M       ;exceeding 80 words?
  0247    3A 9000               LDA     ACEDTA  ;read ace
  024A    DA 032C               JC      OVRNG   ;more than 80 words
  024D    2E E6                 MVI     L,low FFWRT
  024F    54                    MOV     D,H     ;set up write pointer high
  0250    5E                    MOV     E,M     ;set up write pointer low
  0251    12                    STAX    D       ;store to fifo
  0252    7B                    MOV     A,E
  0253    3C                    INR     A       ;advance pointer
  0254    FE A0                 CPI     low FFEND+1;exceeding 80 words?
  0256    DA 025A               JC      WFFRNG  ;less than 80 words
  0259    1F                    RAR             ;fifo start again
```

```
025A    77          WFFRNG: MOV     M,A     ;advance write pointer
025B    FB                  EI

025C    D1          CMRTN:  POP     D
025D    F1                  POP     PSW
025E    E1                  POP     H

                    ;{FUNCTION} unused keys
025F    C9          RTN:    RET


                    ;KEY BOARD RETURN, addr high=2h
0260    AF          KLCRTN: XRA     A       ;enable keyboard
0261    32 3FEE             STA     KBDLCK
0264    C3 025C             JMP     CMRTN

                    ;CHECK FIFO AND RETURN, addr high=2h
0267    21 3FEA     FFCHK:  LXI     H,FFWCT ;fifo word count
026A    35                  DCR     M       ;fifo empty?
026B    FA 025C             JM      CMRTN   ;empty


                    ;READ A WORD FROM ACE FIFO
026E    2E E5       RDFIFO: MVI     L,low FFRD
0270    54                  MOV     D,H     ;set up read pointer high
0271    5E                  MOV     E,M     ;set up read pointer low
0272    7B                  MOV     A,E
0273    3C                  INR     A       ;advance read pointer
0274    FE A0               CPI     low FFEND+1;exceeding 80 words?
0276    DA 027A             JC      RFFRNG  ;less than 80 words
0279    1F                  RAR             ;fifo start again
027A    77          RFFRNG: MOV     M,A     ;store read pointer
027B    2E E9               MVI     L,low LEADIN
027D    7E                  MOV     A,M
027E    B7                  ORA     A       ;leadin mode=0?
027F    1A                  LDAX    D       ;read fifo word
0280    CA 004E             JZ      FIFACE  ;not leadin, normal entry
                    PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    11
CRT801
0283

                    ;LEADIN MODE
0283    E6 7F       LINMDE: ANI     07Fh    ;mask input
0285    11 0267             LXI     D,FFCHK
0288    D5                  PUSH    D       ;pseudo call
0289    2E A2               MVI     L,low LINWCT
028B    5E                  MOV     E,M     ;leadin word count
028C    1D                  DCR     E       ;word count=0?
028D    F2 02B3             JP      LINPRA  ;parameter entries
0290    FE 20               CPI     SPC     ;control codes?
0292    D2 02C2             JNC     ILELIN  ;not cntl code, error
0295    CD 016A             CALL    JMPADD  ;fetch jmp address
0298    B7                  ORA     A
0299    F2 02C2             JP      ILELIN  ;code requires no leadin
029C    E6 77               ANI     077h    ;word count/jmp addr high
029E    67                  MOV     H,A     ;save
029F    E6 70               ANI     070h    ;mask word count
02A1    CA 02BE             JZ      LINEXE  ;do function

02A4    0F          LINPFN: RRC             ;right justify word count
02A5    0F                  RRC
02A6    0F                  RRC
02A7    0F                  RRC
02A8    32 3FA2             STA     LINWCT  ;store to word count reg
02AB    3E 07               MVI     A,07h
02AD    A4                  ANA     H       ;get jmp addr high
02AE    67                  MOV     H,A
02AF    22 3FA0             SHLD    LINF    ;save function jmp addr
02B2    C9                  RET

02B3    73          LINPRA: MOV     M,E     ;leadin word count-1
02B4    16 00               MVI     D,0     ;d=0,e=word count-1
02B6    23                  INX     H       ;LINP
02B7    19                  DAD     D       ;hl=para pointer
02B8    77                  MOV     M,A     ;store word
02B9    C0                  RNZ             ;word count<>0, next word
02BA    2A 3FA0             LHLD    LINF    ;load leadin jmp address
02BD    AF                  XRA     A

02BE    32 3FE9     LINEXE: STA     LEADIN  ;defeat leadin
02C1    E9                  PCHL            ;do function

02C2    D3 01       ILELIN: OUT     BELPRT  ;illegal code after leadin
02C4    AF                  XRA     A       ;a=0, reset leadin
```

```
                        ;(FUNCTION) set leadin mode
  02C5   32 3FE9        LINSET: STA     LEADIN  ;a<>0, set leadin
  02C8   C9                     RET


                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    12
CRT801
  02C9
                        ;keyboard interrupt continue
  02C9   AF             KBDINT: XRA     A
  02CA   32 3FEB                STA     CURTMR  ;reset cursor blink timer
  02CD   B6                     ORA     M       ;keyboard locked?
  02CE   DB 80                  IN      KBDPRT  ;read keyboard
  02D0   FB                     EI
  02D1   D5                     PUSH    D
  02D2   C2 0327                JNZ     KNACTV  ;keyboard not active

  02D5   B7                     ORA     A
  02D6   CA 0333                JZ      TGLCL   ;toggle local
                                                ;defeat graphics
  02D9   77                     MOV     M,A     ;lock keyboard
  02DA   11 0260                LXI     D,KLCRTN
  02DD   D5                     PUSH    D       ;generate pseudo call

  02DE   23                     INX     H       ;GECNTL
  02DF   B6                     ORA     M
  02E0   23                     INX     H       ;ULCASE
  02E1   FE 61                  CPI     061h
  02E3   DA 02EC                JC      NLCSE   ;not lower case
  02E6   FE 7B                  CPI     07Bh
  02E8   D2 02EC                JNC     NLCSE   ;not lower case
  02EB   96                     SUB     M       ;u/l case cntl,m=20h/0

  02EC   23             NLCSE:  INX     H       ;local
  02ED   5E                     MOV     E,M
  02EE   1C                     INR     E       ;local mode?
  02EF   C2 01E4                JNZ     KBDACE  ;write to ace

  02F2   FE A0          LCL:    CPI     0A0h    ;parameter entry?
  02F4   D2 068D                JNC     LGPARA  ;yes

  02F7   CD 0158                CALL    CJMP    ;get jmp addr
  02FA   E6 0F                  ANI     0Fh
  02FC   FE 08                  CPI     08h     ;local?
  02FE   DA 005F                JC      LCLFUN  ;do local function
  0301   7B                     MOV     A,E     ;read lookup tbl ptr
  0302   FE 05                  CPI     low CB+1;cntl B?
  0304   CA 06B7                JZ      ENGRPH  ;enable graphics mode
  0307   FE 0B                  CPI     low CE+1;cntl E?
  0309   CA 0773                JZ      LRDCUR  ;display cursor location
  030C   FE 0F                  CPI     low CG+1;cntl G?
  030E   CA 0784                JZ      SCALE   ;put scale
  0311   FE 23                  CPI     low CQ+1;cntl Q?
  0313   CA 06D5                JZ      PGM     ;put graphics menu
  0316   FE 41                  CPI     low C7E+1
  0318   CA 07CD                JZ      ATGUL   ;init ace,toggle u/l case
  031B   FE 3B                  CPI     low C1D+1
  031D   CA 034F                JZ      ROM2    ;do rom2 functions
  0320   FE 2B                  CPI     low CU+1;cntl U?
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    13
CRT801
  0322
  0322   C0                     RNZ             ;unused keys
  0323   D1                     POP     D       ;pseudo rtn+lock kbd
  0324   C3 0261                JMP     KLCRTN+1


  0327   EE 03          KNACTV: XRI     KULCDE  ;lock/unlock kbd?
  0329   CA 025A                JZ      CMRTN-2 ;unlock keyboard
  032C   3E 50          OVRNG:  MVI     A,80    ;for FFWCT
  032E   D3 01                  OUT     BELPRT
  0330   C3 025A                JMP     CMRTN-2 ;lock kbd

  0333   23             TGLCL:  INX     H       ;GECNTL
  0334   77                     MOV     M,A     ;disable graphics mode
  0335   32 3FE9                STA     LEADIN  ;reset leadin
  0338   2E F1                  MVI     L,low LOCLM
  033A   7E                     MOV     A,M
  033B   2F                     CMA             ;toggle local
  033C   77                     MOV     M,A
  033D   CD 07E8                CALL    EDACE   ;en/disable ace
  0340   C2 0345                JNZ     ONLINE
  0343   3E 1E                  MVI     A,03h XOR 01Dh
  0345   EE 1D          ONLINE: XRI     01Dh
```

```
0347    00                      nop             ;out lclprt
0348    00                      nop
0349    32 3FED                 STA     RTECTL  ;select blink rate
034C    C3 025C                 JMP     CMRTN

                        ;JMP TO ROM2
034F    3A 0800         ROM2:   LDA     0800h   ;check presence of rom2
0352    FE 55                   CPI     055h    ;=55h?
0354    C0                      RNZ             ;not exist
0355    C3 0801                 JMP     0801h   ;ok, do jmp



                        ;{FUNCTION} stripe off a character
0358    CD 0171         STOFCH: CALL    DFCLOC  ;get cur loc and diff
035B    3D                      DCR     A
035C    CA 0434                 JZ      BELL    ;last column, error
035F    23              STOFLP: INX     H
0360    56                      MOV     D,M
0361    2B                      DCX     H
0362    72                      MOV     M,D     ;do copy
0363    23                      INX     H
0364    3D                      DCR     A
0365    C2 035F                 JNZ     STOFLP
0368    C3 03A4                 JMP     PSPC    ;put a space

                        ;{FUNCTION} insert character
036B    AF              INSCHAR:XRA     A
036C    32 3FE8                 STA     ICMD    ;enable insert mode
036F    C3 038D                 JMP     INSCHR
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    14
CRT801
  0372

                        ;CHARACTER INPUT
0372    D1              CHAR:   POP     D       ;pseudo return
0373    2E 20                   MVI     L,low FBQ
0375    AE                      XRA     M       ;add attribute
0376    AD                      XRA     L       ;remove space code

0377    2A 3FFA                 LHLD    CROW    ;calculate cursor loc
037A    2B                      DCX     H
037B    56                      MOV     D,M
037C    2B                      DCX     H
037D    5E                      MOV     E,M
037E    68                      MOV     L,B     ;row start+cursor
037F    19                      DAD     D       ;hl=cursor address
0380    77                      MOV     M,A     ;write to screen

0381    3E 4F                   MVI     A,79
0383    A8                      XRA     B       ;last column?
0384    CA 03C0                 JZ      LSTCHR  ;last, do scroll
0387    04              MIDCHR: INR     B       ;else advance cursor
0388    3A 3FE8                 LDA     ICMD    ;insert mode?
038B    B7                      ORA     A
038C    C0                      RNZ             ;not insert mode

038D    3E 4F           INSCHR: MVI     A,79
038F    90                      SUB     B       ;byte counter
0390    CA 03AB                 JZ      ILCHAR  ;cursor at last column

0393    2A 3FFA                 LHLD    CROW
0396    5E                      MOV     E,M
0397    23                      INX     H
0398    56                      MOV     D,M     ;d=row end+1
0399    1B                      DCX     D       ;row end
039A    EB                      XCHG
039B    2B              INSLP:  DCX     H
039C    56                      MOV     D,M
039D    23                      INX     H
039E    72                      MOV     M,D     ;do copy
039F    2B                      DCX     H
03A0    3D                      DCR     A
03A1    C2 039B                 JNZ     INSLP

03A4    3E 80           PSPC:   MVI     A,080h
03A6    A2                      ANA     D       ;get character attribute
03A7    F6 20                   ORI     SPC     ;add space
03A9    77                      MOV     M,A
03AA    C9                      RET

03AB    3C              ILCHAR: INR     A       ;make a<>0
03AC    D3 01                   OUT     BELPRT
03AE    C3 03CE                 JMP     DICMD   ;defeat insert char mode
                        PAGE
```

```
 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    15
CRT801
  03B1
                        ;{FUNCTION} line feed
  03B1    3A 3FF2       LFEED:  LDA     AULF    ;auto line feed?
  03B4    B7                    ORA     A
  03B5    C2 03C1               JNZ     LFD     ;do line feed
  03B8    C9                    RET

                        ;{FUNCTION} carriage return
  03B9    3A 3FF2       CARRTN: LDA     AULF    ;auto line feed?
  03BC    B7                    ORA     A
  03BD    C2 04DE               JNZ     ZROCUR  ;do cr only


  03C0    47            LSTCHR: MOV     B,A     ;set cursor to 1st col

  03C1    11 3FFC       LFD:    LXI     D,LROW
  03C4    2A 3FFA               LHLD    CROW
  03C7    24                    INR     H
  03C8    1A                    LDAX    D
  03C9    BD                    CMP     L       ;crow=lrow?
  03CA    7E                    MOV     A,M     ;next row
  03CB    32 3FFA               STA     CROW    ;crow+1
  03CE    32 3FEB       DICMD:  STA     ICMD    ;defeat insert char mode
  03D1    C0                    RNZ             ;not last row

  03D2    EB            LFSCR:  XCHG            ;last row, do scroll
  03D3    F3                    DI
  03D4    77                    MOV     M,A     ;lrow+1
  03D5    2E FE                 MVI     L,low FROW
  03D7    5E                    MOV     E,M     ;de=row wrap arround tbl
  03D8    1A                    LDAX    D
  03D9    77                    MOV     M,A     ;frow+1
  03DA    FB                    EI


                        ;{FUNCTION} clear cursor row
  03DB    2A 3FFA       DCROW:  LHLD    CROW

  03DE    EB            CLRROW: XCHG
  03DF    21 0000               LXI     H,0
  03E2    39                    DAD     SP
  03E3    EB                    XCHG
  03E4    F3                    DI
  03E5    F9                    SPHL
  03E6    E1                    POP     H       ;lookup row start
  03E7    F9                    SPHL            ;sp=row start
  03E8    FB                    EI
  03E9    2A 3F20               LHLD    FBG     ;space + attribute
                        PAGE
 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    16
CRT801
  03EC
  03EC    E5            PUSHSP: PUSH    H       ;do clear row
  03ED    E5                    PUSH    H
  03EE    E5                    PUSH    H
  03EF    E5                    PUSH    H
  03F0    E5                    PUSH    H
  03F1    E5                    PUSH    H
  03F2    E5                    PUSH    H
  03F3    E5                    PUSH    H
  03F4    E5                    PUSH    H
  03F5    E5                    PUSH    H       ;10
  03F6    E5                    PUSH    H
  03F7    E5                    PUSH    H
  03F8    E5                    PUSH    H
  03F9    E5                    PUSH    H
  03FA    E5                    PUSH    H
  03FB    E5                    PUSH    H
  03FC    E5                    PUSH    H
  03FD    E5                    PUSH    H
  03FE    E5                    PUSH    H
  03FF    E5                    PUSH    H       ;20
  0400    E5                    PUSH    H
  0401    E5                    PUSH    H
  0402    E5                    PUSH    H
  0403    E5                    PUSH    H
  0404    E5                    PUSH    H
  0405    E5                    PUSH    H
  0406    E5                    PUSH    H
  0407    E5                    PUSH    H
  0408    E5                    PUSH    H
  0409    E5                    PUSH    H       ;30
  040A    E5                    PUSH    H
  040B    E5                    PUSH    H
  040C    F3                    DI
```

```
040D    E5                      PUSH    H
040E    E5                      PUSH    H
040F    E5                      PUSH    H
0410    E5                      PUSH    H
0411    E5                      PUSH    H
0412    E5                      PUSH    H
0413    E5                      PUSH    H
0414    E5                      PUSH    H       ;40
0415    EB                      XCHG
0416    F9                      SPHL
0417    FB              BSRTN:  EI
0418    C9                      RET


                        ;{FUNCTION} delete
0419    3E 20           DEL:    MVI     A,SPC
041B    CD 06CB                 CALL    STSP    ;store space
041E    AF                      XRA     A       ;do back space
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    17
CRT801
 041F
                        ;{FUNCTION} back space
041F    C4 06C1         BS:     CNZ     CHKGM   ;check graphics mode
0422    F3              BS1:    DI
0423    05                      DCR     B       ;cursor-1
0424    F2 0417                 JP      BSRTN   ;not 1st column
0427    04                      INR     B
0428    FB                      EI
0429    3A 3FEF                 LDA     GECNTL
042C    B7                      ORA     A       ;graphics mode?
042D    C0                      RNZ             ;defeat wrap arround
042E    CD 0451                 CALL    UCUR1   ;up cursor one row
0431    C8                      RZ              ;crow=frow?
0432    06 4F                   MVI     B,79    ;set cursor to last col
0434    D3 01           BELL:   OUT     BELPRT
0436    C9                      RET

                        ;{FUNCTION} forward cursor
0437    CD 06C1         FS:     CALL    CHKGM   ;check graphics mode
043A    3E 4F                   MVI     A,79
043C    B8                      CMP     B       ;last column?
043D    C2 0387                 JNZ     MIDCHR  ;not last column
0440    3A 3FEF                 LDA     GECNTL
0443    B7                      ORA     A       ;graphics mode?
0444    C0                      RNZ             ;defeat wrap arround
0445    CD 0463                 CALL    DCUR1   ;down cursor one row
0448    C8                      RZ              ;crow=lrow?
0449    06 00                   MVI     B,0     ;set cursor to 1st col
044B    D3 01                   OUT     BELPRT
044D    C9                      RET

                        ;{FUNCTION} up cursor one row
044E    CD 06C1         UPCUR:  CALL    CHKGM   ;check graphics mode
0451    11 3FFA         UCUR1:  LXI     D,CROW
0454    2A 3FFE                 LHLD    FROW
0457    1A                      LDAX    D       ;crow
0458    24                      INR     H       ;hl=row wrap arround tbl
0459    BD                      CMP     L       ;crow=frow?
045A    C2 04A7                 JNZ     $4
045D    D3 01                   OUT     BELPRT  ;crow=frow, ring bell
045F    C9                      RET

                        ;{FUNCTION} down cursor one row
0460    CD 06C1         DWNCUR: CALL    CHKGM   ;check graphics mode
0463    11 3FFA         DCUR1:  LXI     D,CROW
0466    2A 3FFC                 LHLD    LROW
0469    1A                      LDAX    D       ;crow
046A    24                      INR     H       ;hl=row wrap arroud tbl
046B    BD                      CMP     L       ;crow=lrow?
046C    C2 04A9                 JNZ     $5
046F    D3 01                   OUT     BELPRT  ;crow=lrow, ring bell
0471    C9                      RET
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    18
CRT801
 0472
                        ;{FUNCTION} roll up
0472    11 3FFA         ROLUP:  LXI     D,CROW
0475    2A 3FFE                 LHLD    FROW
0478    1A                      LDAX    D
0479    24                      INR     H       ;hl=row wrap arround tbl
047A    BD                      CMP     L       ;crow=frow?
047B    7E                      MOV     A,M     ;next row
047C    F3                      DI
047D    32 3FFE                 STA     FROW    ;frow+1
0480    C2 0484                 JNZ     RUNEQ
```

```
0483    12                      STAX    D       ;crow+1
0484    EB              RUNEQ:  XCHG            ;d=1,h=3Fh
0485    2E FC                   MVI     L,low LROW
0487    5E                      MOV     E,M     ;de=row wrap arround tbl
0488    1A                      LDAX    D       ;next row
0489    77                      MOV     M,A     ;lrow+1
048A    FB                      EI
048B    C9                      RET

                        ;{FUNCTION} roll down
048C    11 3FFA         ROLDWN: LXI     D,CROW
048F    3A 3FFC                 LDA     LROW
0492    D6 04                   SUI     4       ;up one row
0494    6F                      MOV     L,A
0495    26 01                   MVI     H,1     ;hl=row wrap arround tbl
0497    1A                      LDAX    D       ;crow
0498    D6 04                   SUI     4
049A    BD                      CMP     L       ;crow=lrow?
049B    7E                      MOV     A,M     ;up one row
049C    F3                      DI
049D    32 3FFC                 STA     LROW    ;lrow-1
04A0    C2 04A4                 JNZ     RDNEQ
04A3    12                      STAX    D       ;crow-1
04A4    1E FE           RDNEQ:  MVI     E,low FROW
04A6    1A                      LDAX    D
04A7    D6 04           $4:     SUI     4
04A9    6F              $5:     MOV     L,A     ;hl=row wrap arround tbl
04AA    7E                      MOV     A,M
04AB    12                      STAX    D       ;frow-1
04AC    FB                      EI
04AD    C9                      RET

                        ;{FUNCTION} enable cursor, unlock keyboard
04AE    AF              CURULK: XRA     A
04AF    32 3FEE                 STA     KBDLCK  ;unlock keyboard
04B2    2F                      CMA             ;enable cursor
04B3    C3 001B                 JMP     DICUR

                        ;{FUNCTION} lock keyboard
04B6    32 3FEE         KBLK:   STA     KBDLCK  ;lock keyboard
04B9    C9                      RET
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    19
CRT801
04BA
                        ;{FUNCTION} delete rest of page
04BA    3A 3FFA         DRTPG:  LDA     CROW
04BD    CD 04E9                 CALL    CTLRW2  ;clear crow+1 to lrow

                        ;{FUNCTION} delete rest of line
04C0    CD 0171         DRTLN:  CALL    DFCLOC  ;get cursor loc and diff
04C3    57                      MOV     D,A     ;save
04C4    3A 3F20                 LDA     FBG
04C7    77              DRLLP:  MOV     M,A     ;store space/attribute
04C8    23                      INX     H
04C9    15                      DCR     D
04CA    C2 04C7                 JNZ     DRLLP   ;until end of line
04CD    C9                      RET

                        ;{FUNCTION} clear screen
04CE    CD 06BC         CLRSCN: CALL    DEGRPH  ;defeat graphics mode
04D1    2A 3FFE                 LHLD    FROW
04D4    7D                      MOV     A,L
04D5    CD 04E6                 CALL    CTLRW1  ;clear frow to lrow

                        ;{FUNCTION} home cursor
04D8    3A 3FFE         HOMCUR: LDA     FROW
04DB    32 3FFA                 STA     CROW    ;crow=frow
04DE    06 00           ZROCUR: MVI     B,0     ;set cursor to 1st col
04E0    C9                      RET

                        ;CLEAR TO LAST ROW
04E1    16 01           CLRWLP: MVI     D,1
04E3    5F                      MOV     E,A     ;de=row wrap arround tbl
04E4    1A                      LDAX    D       ;next row
04E5    6F                      MOV     L,A
04E6    CD 03DE         CTLRW1: CALL    CLRROW  ;clear whole row
04E9    2A 3FFC         CTLRW2: LHLD    LROW
04EC    BD                      CMP     L       ;row=lrow?
04ED    C2 04E1                 JNZ     CLRWLP  ;until last row
04F0    C9                      RET


                        ;{FUNCTION} foreground follows
04F1    11 2020         FGNDF:  LXI     D,02020h;foreground spaces
04F4    C3 04FA                 JMP     LDFGD
```

```
                                ;{FUNCTION} background follows
 04F7    11 A0A0        BGNDF:  LXI     D,0A0A0h;background spaces
 04FA    21 0000        LDFGD:  LXI     H,0
 04FD    39                     DAD     SP
 04FE    EB                     XCHG
 04FF    31 3F50                LXI     SP,DMYROW+80
 0502    C3 03EC                JMP     PUSHSP  ;store in dummy row
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    20
CRT801
  0505
                                ;{FUNCTION} insert a line
 0505    CD 0590        INSLNE: CALL    CRLR    ;calc crow/lrow diff
 0508    21 3FFA                LXI     H,CROW
 050B    73                     MOV     M,E     ;set crow=lrow
 050C    C2 054B                JNZ     MOVDWN  ;move row contents
 050F    C3 058C                JMP     DRWZCU  ;else, del lrow/zero cur

                                ;{FUNCTION} strip off a line
 0512    CD 0590        STOFLNE:CALL    CRLR    ;get crow/lrow diff
 0515    CA 058C                JZ      DRWZCU  ;del lrow/zero cursor
 0518    E5             SLNERG: PUSH    H       ;else do move
 0519    21 3FE7                LXI     H,CPYCTL
 051C    36 00                  MVI     M,0     ;copy upward
 051E    CD 0550                CALL    MOVROW  ;move row contents
 0521    E1                     POP     H       ;get original crow
 0522    22 3FFA                SHLD    CROW    ;back to crow
 0525    C9                     RET

                                ;{FUNCTION} insert/strip off line with range
 0526    2A 3FFA        ISLRG:  LHLD    CROW
 0529    3A 3FA3                LDA     LINP    ;read 2nd parameter
 052C    3D                     DCR     A
 052D    E6 3F                  ANI     03Fh    ;40/7Fh offset to 0/3Fh
 052F    FE 38                  CPI     038h
 0531    D0                     RNC             ;error
 0532    FE 17                  CPI     017h
 0534    DA 053C                JC      ISNPA
 0537    FE 20                  CPI     020h
 0539    D8                     RC              ;error
 053A    D6 09                  SUI     9
 053C    3C             ISNPA:  INR     A
 053D    57                     MOV     D,A
 053E    3A 3FA4                LDA     LINP+1  ;read 1st parameter
 0541    FE 53                  CPI     "S"     ;strip off?
 0543    7A                     MOV     A,D
 0544    CA 051B                JZ      SLNERG  ;do strip off line
 0547    CD 05C1        ILNERG: CALL    IRWOS   ;offset row by para
 054A    7A                     MOV     A,D     ;return para
 054B    21 3FE7        MOVDWN: LXI     H,CPYCTL
 054E    36 04                  MVI     M,4     ;copy downward

                                ;MOVE ROW CONTENTS,UP/DOWN CNTL BY CPYCTL
 0550    F5             MOVROW: PUSH    PSW     ;save row count
 0551    2A 3FFA                LHLD    CROW
 0554    5E                     MOV     E,M
 0555    23                     INX     H
 0556    56                     MOV     D,M
 0557    1B                     DCX     D       ;crow end
 0558    D5                     PUSH    D       ;save
 0559    21 3FE7                LXI     H,CPYCTL;direction control
 055C    11 3FFA                LXI     D,CROW
 055F    1A                     LDAX    D       ;read crow
 0560    96                     SUB     M       ;direction cntl
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    21
CRT801
  0561
 0561    6F                     MOV     L,A
 0562    26 01                  MVI     H,1     ;hl=row wrap arround tbl
 0564    7E                     MOV     A,M     ;lookup +/- one row
 0565    12                     STAX    D       ;update crow
 0566    6F                     MOV     L,A
 0567    25                     DCR     H       ;hl=row start table
 0568    5E                     MOV     E,M
 0569    23                     INX     H
 056A    56                     MOV     D,M
 056B    1B                     DCX     D       ;+/- row end
 056C    E1                     POP     H       ;rtn current row last loc
 056D    06 10                  MVI     B,80/5  ;copy 80 characters
 056F    1A             CPLP:   LDAX    D       ;read
 0570    77                     MOV     M,A     ;copy
 0571    2B                     DCX     H       ;next byte
 0572    1B                     DCX     D       ;next byte
 0573    1A                     LDAX    D       ;do 5 times for speed
 0574    77                     MOV     M,A
```

```
0575  2B                    DCX   H
0576  1B                    DCX   D
0577  1A                    LDAX  D       ;3
0578  77                    MOV   M,A
0579  2B                    DCX   H
057A  1B                    DCX   D
057B  1A                    LDAX  D       ;4
057C  77                    MOV   M,A
057D  2B                    DCX   H
057E  1B                    DCX   D
057F  1A                    LDAX  D       ;5
0580  77                    MOV   M,A
0581  2B                    DCX   H
0582  1B                    DCX   D
0583  05                    DCR   B
0584  C2 056F              JNZ   CPLP    ;finish 80 bytes?
0587  F1                    POP   PSW     ;row count
0588  3D                    DCR   A
0589  C2 0550              JNZ   MOVROW  ;next row
058C  47              DRWZCU: MOV   B,A   ;zero cursor
058D  C3 03DB              JMP   DCROW   ;and delete cursor row

                      ;CALCULATE ROW DIFFERENCE
0590  2A 3FFA        CRLR: LHLD  CROW    ;calc crow to lrow
0593  3A 3FFC              LDA   LROW
0596  5F              FRCR: MOV   E,A
0597  95                    SUB   L       ;get the difference
0598  D2 05A0              JNC   $2      ;within range
059B  3E 60           $D2:  MVI   A,RWRG  ;over range
059D  83                    ADD   E
059E  95                    SUB   L
059F  B7                    ORA   A       ;clear carry
05A0  1F              $2:   RAR           ;row diff /2
05A1  C9                    RET
                      PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    22
CRT801
 05A2

                      ;(FUNCTION) address cursor
05A2  2A 3FA3        ADDCUR: LHLD  LINP   ;read leadin parameter
05A5  7C                    MOV   A,H

05A6  11 5010        CALCX:  LXI   D,0501Oh;calc x coordinate
05A9  BA                     CMP   D
05AA  DA 05B3               JC    CX4FD  ;00/4Fh=loc 0/79
05AD  92                     SUB   D      ;50/7Fh offset to 0/2F
05AE  BB                     CMP   E
05AF  DA 05B3               JC    CX4FD  ;50/5Fh offset to 0/15
05B2  93                     SUB   E      ;60/7Fh offset to 0/31
05B3  47              CX4FD: MOV   B,A    ;then set cursor

05B4  3E 1F           CALCY: MVI   A,01Fh
05B6  A5                     ANA   L      ;0/1F,20/3F,40/5F,60/7Fh
05B7  FE 18                  CPI   018h   ;offset to 00/1Fh
05B9  DA 05BE               JC    CY17D  ;00/17h=row 0/23
05BC  D6 18                  SUI   018h   ;18/1Fh=row 0/7
05BE  2A 3FFE         CY17D: LHLD  FROW   ;offset first row

05C1  07              IRWOS: RLC          ;diff*2,msb=0
05C2  85                     ADD   L      ;frow+offset
05C3  DA 05CB               JC    ROSFFU ;>FFh
05C6  FE E1                  CPI   low RR48+1
05C8  DA 05CD               JC    ROSEOD ;less than E0h,ok
05CB  D6 60           ROSFFU: SUI   RWRG   ;row range
05CD  32 3FFA         ROSEOD: STA   CROW   ;then update crow
05D0  C9                     RET


                      ;(FUNCTION) read cursor
05D1  CD 05E0        RDCUR:  CALL  RDX    ;read cursor x coord
05D4  CD 006D                CALL  WTACEA ;write to ace

05D7  CD 05E7                CALL  RDY    ;read cursor y coord
05DA  CD 006D                CALL  WTACEA ;write to ace

05DD  C3 074A                JMP   CRACE  ;cr for termination

05E0  78              RDX:   MOV   A,B
05E1  FE 20                  CPI   020h   ;if 0/1Fh add offset
05E3  D0                     RNC          ;20/4Fh=cursor loc 32/79
05E4  C6 60                  ADI   060h   ;60/7Fh=cursor loc 0/31
05E6  C9                     RET
```

```
05E7    2A 3FFE         RDY:    LHLD    FROW
05EA    3A 3FFA                 LDA     CROW
05ED    CD 0596                 CALL    FRCR    ;calc frow/crow diff
05F0    C6 60                   ADI     060h    ;60/77h=row 0/23
05F2    C9                      RET
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    23
CRT801
 05F3
                        ;{FUNCTION} next page
05F3    16 30           NPAGE:  MVI     D,030h  ;page offset
05F5    21 3FFA                 LXI     H,CROW
05F8    F3                      DI
05F9    7E              NPLP:   MOV     A,M
05FA    FE B1                   CPI     0B1h
05FC    DA 0601                 JC      NPLT    ;a< B1,B2-B0h
05FF    92                      SUB     D       ;a>=B1,B2-E0h
0600    92                      SUB     D
0601    82              NPLT:   ADD     D
0602    77                      MOV     M,A
0603    2C                      INR     L       ;do crow/lrow/frow
0604    2C                      INR     L
0605    FA 05F9                 JM      NPLP    ;if pass frow, end
0608    FB                      EI
0609    C9                      RET

                        ;{FUNCTION} tab
060A    2A 3FFA         TAB:    LHLD    CROW
060D    E5                      PUSH    H       ;save crow
060E    CD 0667                 CALL    SCATT

0611    13              TDADSP: INX     D       ;next character
0612    2D                      DCR     L       ;end of row?
0613    CC 067A                 CZ      DRCFL   ;down one row, get 1st loc
0616    1A                      LDAX    D       ;read character
0617    84                      ADD     H       ;check attribute
0618    FA 0635                 JM      TSATT   ;diff, find same attrib
061B    FE 20                   CPI     SPC     ;space?
061D    C2 0611                 JNZ     TDADSP  ;loop until space
0620    13              TSANSP: INX     D       ;next character
0621    2D                      DCR     L       ;end of row?
0622    CC 067A                 CZ      DRCFL   ;down one row, get 1st loc
0625    1A                      LDAX    D       ;read character
0626    84                      ADD     H       ;check attribute
0627    FA 0635                 JM      TSATT   ;diff, find same attrib
062A    FE 20                   CPI     SPC     ;non space?
062C    CA 0620                 JZ      TSANSP  ;loop until non space
062F    D1              TMCUR:  POP     D       ;remove saved crow
0630    3E 50                   MVI     A,80
0632    95                      SUB     L       ;calc cursor location
0633    47                      MOV     B,A     ;move cursor
0634    C9                      RET
0635    13              TSATT:  INX     D       ;next character
0636    2D                      DCR     L       ;end of row?
0637    CC 067A                 CZ      DRCFL   ;down one row,get 1st loc
063A    1A                      LDAX    D       ;read character
063B    84                      ADD     H       ;check attribute
063C    FA 0635                 JM      TSATT   ;loop until same attrib
063F    C3 062F                 JMP     TMCUR   ;move cursor
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    24
CRT801
 0642
                        ;{FUNCTION} clear fore/background to space
0642    2A 3FFA         CFB:    LHLD    CROW
0645    24                      INR     H
0646    E5                      PUSH    H       ;save
0647    CD 0667                 CALL    SCATT
064A    1A              CFBLP:  LDAX    D       ;read character
064B    84                      ADD     H       ;test attribute
064C    FA 0653                 JM      CFBDIF  ;diff attrib
064F    3E 20                   MVI     A,SPC   ;if same attrib,
0651    B4                      ORA     H       ;put a space
0652    12                      STAX    D
0653    13              CFBDIF: INX     D       ;next character
0654    2D                      DCR     L       ;character counter-1
0655    C2 064A                 JNZ     CFBLP   ;until finish 80 char
0658    E1                      POP     H       ;saved crow
0659    3A 3FFC                 LDA     LROW
065C    BD                      CMP     L       ;row=lrow?
065D    C8                      RZ              ;no more
065E    6E                      MOV     L,M     ;else next row
065F    E5                      PUSH    H       ;save
0660    CD 0681                 CALL    $3
0663    C3 064A                 JMP     CFBLP
0666    C9                      RET
```

```
                        ;SET UP CHAR COUNTER AND ATTRIB
0667    CD 0174         SCATT:  CALL    CURLOC  ;get cursor location
066A    EB                      XCHG            ;put in de
066B    21 8050                 LXI     H,08050h;mask/char count
066E    3A 3F20                 LDA     FBG
0671    A4                      ANA     H
0672    67                      MOV     H,A
0673    22 3FA5                 SHLD    LINP+2  ;save count,attrib
0676    7D                      MOV     A,L
0677    90                      SUB     B       ;get cur to end diff
0678    6F                      MOV     L,A     ;put in l
0679    C9                      RET


                        ;DOWN ONE ROW AND GET ADDR ON 1ST COLUMN
067A    CD 0463         DRCFL:  CALL    DCUR1   ;down cursor one row
067D    CA 0033                 JZ      TABSTP  ;crow=lrow, no tab
0680    6E                      MOV     L,M     ;next row
0681    25              $3:     DCR     H
0682    2B              $1:     DCX     H
0683    56                      MOV     D,M     ;addr high
0684    2B                      DCX     H
0685    5E                      MOV     E,M     ;addr low
0686    2A 3FA5                 LHLD    LINP+2  ;count and attrib
0689    C9                      RET
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    25
CRT801
  068A
                        ;{FUNCTION} graphics
068A    3A 3FA3         GRAPH:  LDA     LINP    ;read leadin parameter
068D    21 107E         LGPARA: LXI     H,0107Eh
0690    3D                      DCR     A
0691    E6 3F                   ANI     03Fh
0693    BC                      CMP     H       ;h=010h
0694    DA 06AD                 JC      $G1     ;"A" to "P"
0697    FE 3E                   CPI     03Eh    ;delete
0699    CA 06B2                 JZ      $G3
069C    94                      SUB     H       ;h=010h
069D    FE 0F                   CPI     0Fh     ;space?
069F    CA 06B2                 JZ      $G3     ;space
06A2    BC                      CMP     H       ;h=010h
06A3    DA 06AC                 JC      $G2     ;> "Q"
06A6    FE 20                   CPI     020h
06A8    DA 06AD                 JC      $G1     ;"a" to "p"
06AB    2C                      INR     L       ;set l to 7Fh
06AC    7D              $G2:    MOV     A,L     ;L=7Eh or 7Fh
06AD    CD 06D0         $G1:    CALL    STSCN   ;put symbol to screen
06B0    C6 1E                   ADI     01Eh
06B2    D6 1E           $G3:    SUI     01Eh
06B4    32 3FF3                 STA     GSYMBL  ;for non/destructive move

06B7    3E 80           ENGRPH: MVI     A,080h
06B9    C3 06BD                 JMP     DEGRPH+1

                        ;{FUNCTION} defeat graphics
06BC    AF              DEGRPH: XRA     A
06BD    32 3FEF                 STA     GECNTL
06C0    C9                      RET



                        ;CHECK GRAPHICS MODE AND PUT SYMBOL TO SCREEN
06C1    3A 3FEF         CHKGM:  LDA     GECNTL
06C4    B7                      ORA     A       ;graphics mode?
06C5    C8                      RZ              ;no, rtn to func
06C6    3A 3FF3                 LDA     GSYMBL
06C9    B7                      ORA     A       ;non destructive move?
06CA    F8                      RM              ;yes
06CB    21 3F20         STSP:   LXI     H,FBG
06CE    AE                      XRA     M       ;get attribute
06CF    AD                      XRA     L       ;remove space code
06D0    CD 0174         STSCN:  CALL    CURLOC
06D3    77                      MOV     M,A     ;write to screen
06D4    C9                      RET
                        PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    26
CRT801
  06D5
                        ;PUT GRAPHIC MENU TO SCREEN (LOCAL)
06D5    CD 070C         PGM:    CALL    RUADD

06D8    CD 06F3                 CALL    P38SYM  ;print ascii A/Q
06DB    CD 06F3                 CALL    P38SYM  ;print ascii a/q
```

```
06DE    CD 070C             CALL    RUADD

06E1    CD 0700             CALL    P32SYM  ;print ascii 0h/Fh
06E4    F6 7E               ORI     07Eh    ;print ascii 7Eh
06E6    CD 06F7             CALL    P6SYM   ;4 spaces
06E9    EE 30               XRI     030h    ;print ascii 10/1Fh
06EB    CD 0700             CALL    P32SYM
06EE    F6 7F               ORI     07Fh    ;print ascii 7Fh
06F0    C3 06F7             JMP     P6SYM   ;4 spaces

06F3    F6 41       P38SYM: ORI     041h    ;change symbol
06F5    16 10               MVI     D,16    ;counter
06F7    14          P6SYM:  INR     D
06F8    CD 0702             CALL    PGMLP
06FB    16 04       P4SP:   MVI     D,4
06FD    C3 04C4             JMP     DRLLP-3 ;put 4 spaces

0700    16 10       P32SYM: MVI     D,16    ;print 32 symbols

0702    77          PGMLP:  MOV     M,A
0703    23                  INX     H
0704    73                  MOV     M,E     ;FBG
0705    23                  INX     H
0706    3C                  INR     A       ;next symbol
0707    15                  DCR     D
0708    C2 0702             JNZ     PGMLP
070B    C9                  RET


070C    CD 0472     RUADD:  CALL    ROLUP   ;up one row
070F    26 00               MVI     H,0
0711    6F                  MOV     L,A     ;hl=lrow
0712    CD 0682             CALL    $1      ;lrow 1st loc
0715    EB                  XCHG
0716    CD 06FB             CALL    P4SP    ;put 4 spaces
0719    5F                  MOV     E,A     ;FBG
071A    E6 80               ANI     080h    ;get attribute
071C    C9                  RET
                    PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    27
CRT801
 071D

                    ;{FUNCTION} transmit a line
071D    06 00       SNDLNE: MVI     B,0     ;set cursor to 1st loc
071F    CD 0174             CALL    CURLOC  ;get row start
0722    E5                  PUSH    H       ;save row start
0723    11 004F             LXI     D,79    ;find row end
0726    19                  DAD     D       ;hl=row end, clear carry
0727    16 40               MVI     D,040h  ;rotated space
0729    7E          LENDLP: MOV     A,M     ;read char
072A    17                  RAL             ;mask out msb
072B    AA                  XRA     D       ;space? , clear carry
072C    C2 0734             JNZ     LNSP    ;until find a non-space
072F    2B                  DCX     H
0730    1D                  DCR     E
0731    C2 0729             JNZ     LENDLP  ;repeat loop
0734    E1          LNSP:   POP     H       ;hl=row start again
0735    56          SNDLP:  MOV     D,M     ;read character
0736    3E 60               MVI     A,060h  ;screen all cntl codes
0738    A2                  ANA     D
0739    C2 073E             JNZ     SNCNTL  ;not control code
073C    16 2A               MVI     D,"*"   ;cntl code,send "*" instead
073E    CD 006E     SNCNTL: CALL    WTACED  ;write to ace
0741    7E                  MOV     A,M     ;read char again
0742    EE 80               XRI     080h    ;invert attribute
0744    77                  MOV     M,A     ;store back
0745    23                  INX     H       ;next character
0746    1D                  DCR     E
0747    F2 0735             JP      SNDLP   ;until end of line

074A    CD 006B     CRACE:  CALL    SNDCR   ;send cr for termination
074D    3A 3FF1             LDA     LOCLM
0750    B7                  ORA     A       ;local?
0751    C8                  RZ              ;remote,no time delay

0752    CD 075E     $D3:    CALL    $DLY    ;do delay
0755    15                  DCR     D       ;d was 0Dh
0756    C2 0752             JNZ     $D3
0759    D3 01               OUT     BELPRT  ;delay done,ring bell
075B    C3 0463             JMP     DCUR1   ;move cursor to next row
075E    E5          $DLY:   PUSH    H
075F    D5                  PUSH    D
```

```
0760    CD 07F0             CALL    LUBD    ;lookup baud constant
0763    3E 1F               MVI     A,01Fh  ;chg delay at high bauds
0765    B3                  ORA     E
0766    5F                  MOV     E,A
0767    CD 059B     $D1:    CALL    $D2
076A    1B                  DCX     D
076B    15                  DCR     D
076C    14                  INR     D
076D    F2 0767             JP      $D1
0770    D1                  POP     D
0771    E1                  POP     H
0772    C9                  RET
                    PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    28
CRT801
  0773
                    ;DISPLAY CURSOR LOCATION (LOCAL)
0773    CD 05E7     LRDCUR: CALL    RDY     ;y coordinate
0776    2A 3FFC             LHLD    LROW    ;get print out loc
0779    5E                  MOV     E,M
077A    23                  INX     H
077B    56                  MOV     D,M
077C    1B                  DCX     D       ;lrow last location
077D    12                  STAX    D       ;put to screen
077E    CD 05E0             CALL    RDX     ;x coordinate
0781    1B                  DCX     D
0782    12                  STAX    D       ;put to screen
0783    C9                  RET

                    ;SCALE (LOCAL)
0784    21 3FFE     SCALE:  LXI     H,FROW
0787    3A 3FFA             LDA     CROW
078A    BE                  CMP     M       ;frow=crow
078B    CC 048C             CZ      ROLDWN  ;if equ,roll down
078E    2A 3FFA             LHLD    CROW    ;get print out loc
0791    2B                  DCX     H
0792    2B                  DCX     H
0793    CD 0682             CALL    $1
0796    EB                  XCHG            ;hl=loc
0797    1E 31               MVI     E,"1"

0799    16 B1       SCLLP1: MVI     D,"1"+080h
079B    3E BA               MVI     A,"9"+081h
079D    72          SCLLP2: MOV     M,D
079E    14                  INR     D       ;"1" to "9"
079F    23                  INX     H       ;next location
07A0    BA                  CMP     D       ;exceeding "9"?
07A1    C2 079D             JNZ     SCLLP2
07A4    3E 39               MVI     A,"9"
07A6    73                  MOV     M,E
07A7    1C                  INR     E       ;"1" to "8"
07A8    23                  INX     H       ;next location
07A9    BB                  CMP     E       ;exceeding "8"?
07AA    C2 0799             JNZ     SCLLP1
07AD    C9                  RET

                    ;VERTICAL INTERRUPT CONTINUE
                    ;*********************************************
07AE    2B          VTSUB:  DCX     H       ;VCALEN
07AF    74                  MOV     M,H     ;h<>0, enable VCAL routine
07B0    2A 3FF8             LHLD    CUR     ;get cursor
07B3    36 03               MVI     M,3     ;write to DP8350
07B5    2A 3FF6             LHLD    TOP     ;top of page
07B8    36 02               MVI     M,2     ;write to DP8350
07BA    D3 40               OUT     VERPRT  ;clr vert intr flip/flop
07BC    E1                  POP     H
07BD    FB                  EI
07BE    C9                  RET
                    PAGE

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    29
CRT801
  07BF
                    ;(FUNCTION) ace, auto line feed, upper/lower case
07BF    DB 40       ACESW:  IN      SETSW   ;read switch settings
07C1    E6 10               ANI     010h
07C3    32 3FF2             STA     AULF    ;set auto lf flag

07C6    DB 40               IN      SETSW   ;read switch again
07C8    E6 20               ANI     020h
07CA    C3 07D2             JMP     STUL    ;set u/l case flag
```

```
                        ;INIT ACE,TOGGLE ULCASE (LOCAL)
07CD    3A 3FF0     ATGUL:  LDA     ULCASE
07D0    EE 20               XRI     020h    ;toggle u/l case
07D2    32 3FF0     STUL:   STA     ULCASE

07D5    CD 07F0             CALL    LUBD    ;lookup baud constant

07D8    21 9003             LXI     H,ACECTL
07DB    74                  MOV     M,H     ;set DLAB

07DC    2E 01               MVI     L,1
07DE    72                  MOV     M,D     ;set baud high
07DF    2B                  DCX     H
07E0    73                  MOV     M,E     ;set baud low

07E1    2E 03               MVI     L,3
07E3    36 02               MVI     M,2     ;7 bit,1 stop bit

07E5    3A 3FF1             LDA     LOCLM   ;local?
07E8    3C          EDACE:  INR     A
07E9    21 9000             LXI     H,ACEDTA
07EC    5E                  MOV     E,M     ;remove ace input
07ED    23                  INX     H       ;ACEITR mask
07EE    77                  MOV     M,A     ;en/disable ace intr
07EF    C9                  RET

07F0    DB 40       LUBD:   IN      SETSW   ;lookup baud constant
07F2    E6 0E               ANI     0Eh
07F4    C6 F0       BADDR:  ADI     low B110;add base addr
07F6    6F                  MOV     L,A
07F7    26 01               MVI     H,1
07F9    5E                  MOV     E,M     ;get baud low
07FA    23                  INX     H
07FB    56                  MOV     D,M     ;get baud high
07FC    C9                  RET
                            END     START
```

```
 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    30
CRT801
Macros:

Symbols:
$1      0682    $2      05A0    $3      0681    $4      04A7
$5      04A9    $D1     0767    $D2     059B    $D3     0752
$DLY    075E    $G1     06AD    $G2     06AC    $G3     06B2
ACE     0038    ACECTL  9003    ACEDTA  9000    ACEDUP  0018
ACEITR  9001    ACESTU  9005    ACESW   07BF    ADDCUR  05A2
ATGUL   07CD    AULF    3FF2    B110    01F0    B1200   01F4
B19200  01FC    B2400   01F6    B38400  01FE    B4800   01F8
B600    01F2    B9600   01FA    BADDR   07F4    BELL    0434
BELPRT  0001    BGNDF   04F7    BS      041F    BS1     0422
BSRTN   0417    C1D     023A    C7E     0240    CALCX   05A6
CALCY   05B4    CALJMP  015C    CARRTN  03B9    CB      0204
CE      020A    CFB     0642    CFBDIF  0653    CFBLP   064A
CG      020E    CHAR    0372    CHKGM   06C1    CJMP    0158
CLRROW  03DE    CLRSCN  04CE    CLRWLP  04E1    CMRTN   025C
CPLP    056F    CPYCTL  3FE7    CQ      0222    CR      000D
CRACE   074A    CRLR    0590    CROW    3FFA    CROWH   3FFB
CTLRW1  04E6    CTLRW2  04E9    CU      022A    CUR     3FF8
CUREN   3FEC    CURH    3FF9    CURLOC  0174    CURTMR  3FEB
CURULK  04AE    CX4FD   05B3    CY17D   05BE    DCROW   03DB
DCUR1   0463    DEGRPH  06BC    DEL     0419    DFCLOC  0171
DICMD   03CE    DICUR   001B    DMYROW  3F00    DRCFL   067A
DRLLP   04C7    DRTLN   04C0    DRTPG   04BA    DRWZCU  058C
DWNCUR  0460    EDACE   07E8    ENGRPH  06B7    F1      0A5F
F10     84D8    F11     85F3    F12     8472    F13     848C
F14     84AE    F15     8DD1    F16     ADA2    F17     84F1
F18     84F7    F19     836B    F2      03B9    F20     8358
F21     8505    F22     8512    F23     AD26    F24     9E8A
F25     0419    F26     83DB    F27     84C0    F28     84BA
F29     8642    F3      03B1    F30     84CE    F31     8CB6
F32     801B    F33     871D    F34     87BF    F35     0AC5
F36     86BC    F4      0C34    F5      060A    F6      0437
F7      041F    F8      844E    F9      8460    FBG     3F20
FCHR2   3780    FFCHK   0267    FFEND   3F9F    FFRD    3FE5
FFSTRT  3F50    FFWCT   3FEA    FFWRT   3FE6    FGNDF   04F1
FIFACE  004E    FRCR    0596    FROW    3FFE    FROWH   3FFF
FS      0437    FUNC    0168    GECNTL  3FEF    GRAPH   068A
GSYMBL  3FF3    HOMCUR  04DB    ICMD    3FE8    ILCHAR  03AB
ILELIN  02C2    ILNERG  0547    INIT    00E2    INSCHA  036B
INSCHR  038D    INSLNE  0505    INSLP   039B    IRWOS   05C1
ISLRG   0526    ISNPA   053C    JMPADD  016A    KBD     0020
KBDACE  01E4    KBDINT  02C9    KBDLCK  3FEE    KBDPRT  0080
KBLK    04B6    KLCRTN  0260    KNACTV  0327    KULCDE  0003
LCL     02F2    LCLFUN  005F    LCLIND  0002    LDFGD   04FA
LEADIN  3FE9    LENDLP  0729    LF      000A    LFD     03C1
LFEED   03B1    LFSCR   03D2    LGPARA  068D    LIN     8000
LINC    007E    LINEXE  02BE    LINF    3FA0    LINFH   3FA1
LINMDE  0283    LINP    3FA3    LINPFN  02A4    LINPRA  02B3
```

```
LINSET  02C5    LINWCT  3FA2    LNSP    0734    LOCLM   3FF1
LRDCUR  0773    LROW    3FFC    LROWH   3FFD    LSTCHR  03C0
LUBD    07F0    MIDCHR  0387    MOVDWN  054B    MOVROW  0550
NLC     0800    NLCSE   02EC    NOWRAP  0066    NPAGE   05F3
NPLP    05F9    NPLT    0601    NRW     3FF5    ONLINE  0345

 STARPLEX MACRO-ASSEMBLER V2.0          PAGE    31
CRT801
OUTACE  0079    OVRNG   032C    P32SYM  0700    P38SYM  06F3
P4SP    06FB    P6SYM   06F7    PATTN   0112    PGM     06D5
PGMLP   0702    PSPC    03A4    PTNLP   0117    PUSHSP  03EC
RDCUR   05D1    RDFIFO  026E    RDNEG   04A4    RDX     05E0
RDY     05E7    RFFRNG  027A    ROLDWN  048C    ROLUP   0472
ROM2    034F    ROSEOD  05CD    ROSFFU  05CB    ROW     0008
ROW1    0082    ROW10   0094    ROW11   0096    ROW12   0098
ROW13   009A    ROW14   009C    ROW15   009E    ROW16   00A0
ROW17   00A2    ROW18   00A4    ROW19   00A6    ROW2    0084
ROW20   00A8    ROW21   00AA    ROW22   00AC    ROW23   00AE
ROW24   00B0    ROW25   00B2    ROW26   00B4    ROW27   00B6
ROW28   00B8    ROW29   00BA    ROW3    0086    ROW30   00BC
ROW31   00BE    ROW32   00C0    ROW33   00C2    ROW34   00C4
ROW35   00C6    ROW36   00C8    ROW37   00CA    ROW38   00CC
ROW39   00CE    ROW4    0088    ROW40   00D0    ROW41   00D2
ROW42   00D4    ROW43   00D6    ROW44   00D8    ROW45   00DA
ROW46   00DC    ROW47   00DE    ROW47D  007E    ROW48   00E0
ROW48D  00B0    ROW5    008A    ROW6    008C    ROW7    008E
ROW8    0090    ROW9    0092    ROWDP   0028    ROWPRT  0040
RR1     0182    RR10    0194    RR11    0196    RR12    0198
RR13    019A    RR14    019C    RR15    019E    RR16    01A0
RR17    01A2    RR18    01A4    RR19    01A6    RR1D    01E2
RR2     0184    RR20    01A8    RR21    01AA    RR22    01AC
RR23    01AE    RR24    01B0    RR25    01B2    RR26    01B4
RR27    01B6    RR28    01B8    RR29    01BA    RR3     0186
RR30    01BC    RR31    01BE    RR32    01C0    RR33    01C2
RR34    01C4    RR35    01C6    RR36    01C8    RR37    01CA
RR38    01CC    RR39    01CE    RR4     0188    RR40    01D0
RR41    01D2    RR42    01D4    RR43    01D6    RR44    01D8
RR45    01DA    RR46    01DC    RR47    01DE    RR47D   017E
RR48    01E0    RR48D   0180    RR5     018A    RR6     018C
RR7     018E    RR8     0190    RR9     0192    RTECTL  3FED
RTN     025F    RUADD   070C    RUNEG   0484    RWRG    0060
SCALE   0784    SCATT   0667    SCLLP1  0799    SCLLP2  079D
SETSW   0040    SLNERG  0518    SNCNTL  073E    SNDCR   006B
SNDLNE  071D    SNDLP   0735    SPC     0020    START   0000
STFIFO  0244    STK     3FE5    STOFCH  0358    STOFLN  0512
STOFLP  035F    STSCN   06D0    STSP    06CB    STUL    07D2
TAB     060A    TABSTP  0033    TBLJMP  0200    TDAOSP  0611
TGLCL   0333    TMCUR   062F    TOP     3FF6    TOPH    3FF7
TSANSP  0620    TSATT   0635    UCUR1   0451    ULCASE  3FF0
UPCUR   044E    VCAL    011F    VCALEN  3FF4    VERPRT  0040
VERT    0010    VERTDP  0030    VRWRAP  0061    VTSUB   07AE
W1      1000    W2      2000    WAIT    014E    WFFRNG  025A
WTACEA  006D    WTACED  006E    ZROCUR  04DE

No  Fatal error(s)
```

National Semiconductor

Display Controllers/Drivers
PRELIMINARY

DP-XXX Advanced Graphic CRT Controller, AGCRTC

General Description

The DP-XXX advanced graphic CRT controller, AGCRTC, provides a versatile, powerful and flicker-free solution to all raster scan graphic systems.

The AGCRTC performs six major tasks:

1) screen update
2) asynchronized pixel transfer
3) dynamic RAM refresh control
4) line drawing
5) text processing
6) scrolling

Multiple AGCRTCs can be used in the same system for color graphics or for faster system throughput.

Features

- Supports maximum 2048 pixels by 2048 lines raster scan display
- 16 or 32-bit wide data bus and 20-bit wide address bus
- Maximum frame buffer size up to 16 megapixels
- Screen parameters are programmable, including sync, blanking, screen size, etc.
- System parameters are programmable, including refresh, data bus width
- Supports both interlaced and noninterlaced raster scan displays.
- Supports BITBLT with clipping window
- Fast scrolling—a 1k by 1k display area can be scrolled in any direction within one frame time at 70 Hz, noninterlaced
- Line drawing at 200 ns per pixel
- Supports proportional spacing for word processing
- Horizontal and vertical SYNC inputs allow the AGCRTC to lock to other video sources
- AGCRTC generates either composite SYNC or separate vertical and horizontal SYNCs
- Dynamic RAM refresh support
- Supports color graphics
- Easy interfacing to all popular microprocessors
- Versatile handshake signals for maximum utilization of the available bus bandwidth
- Pipelined data input and output structures for high system throughputs
- Maximum transfer rate, 320 megapixels per second
- High-speed CMOS technology
- 68-pin leaded chip carrier

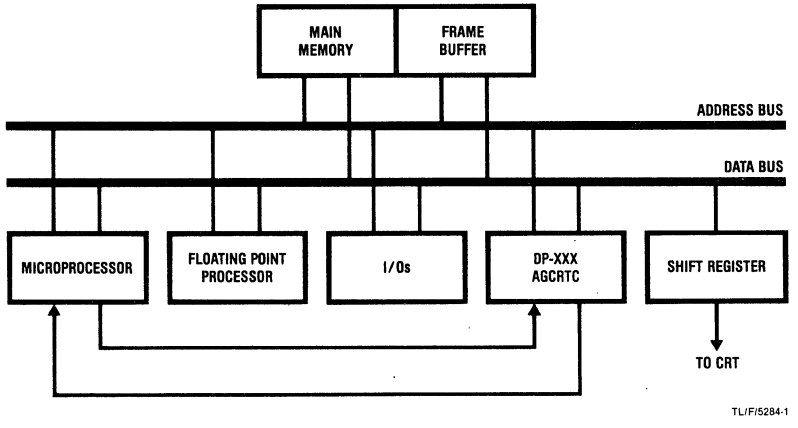


FIGURE 1. Single Bus System Diagram

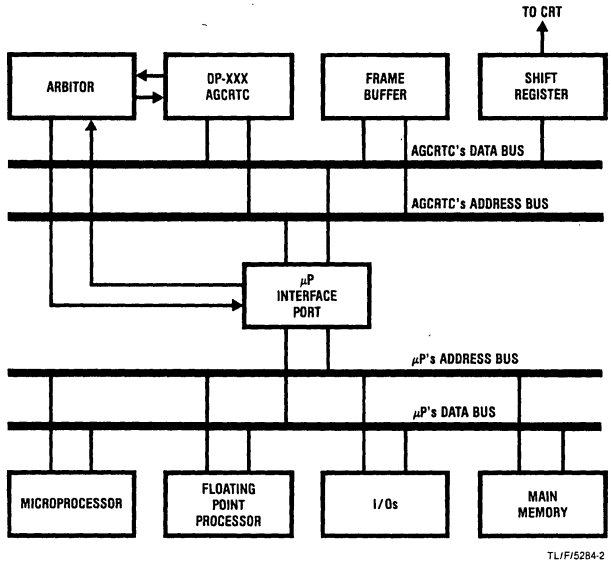


FIGURE 2. Dual Bus System Diagram

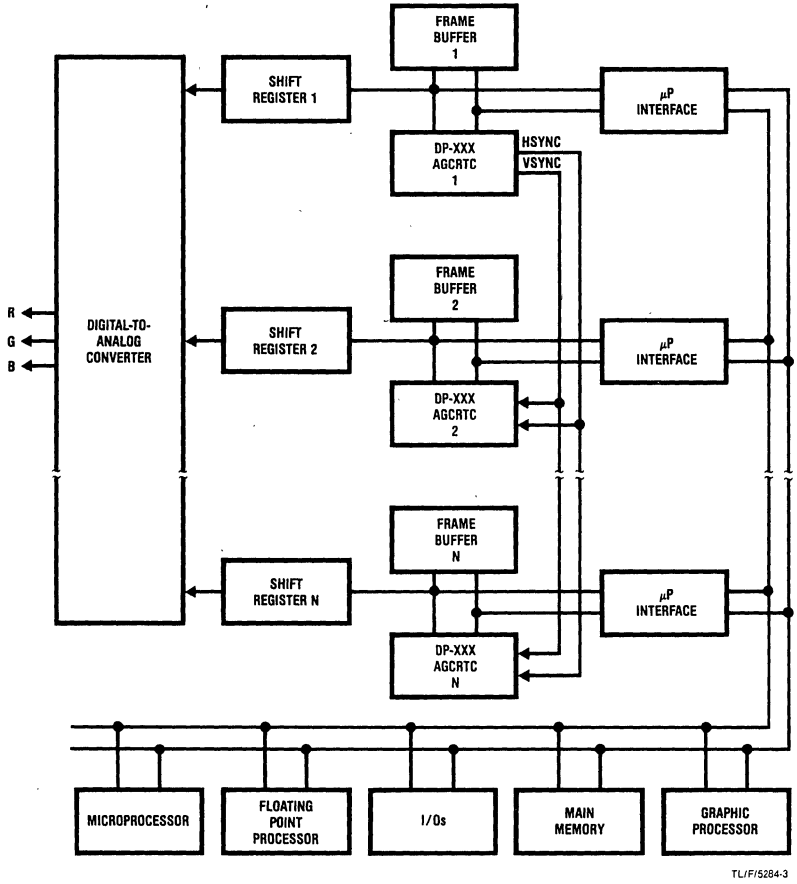


FIGURE 3. Multiple Bitplanes, Multiple AGCRTCs System

National Semiconductor

DS75491 MOS-to-LED Quad Segment Driver
DS75492 MOS-to-LED Hex Digit Driver

General Description

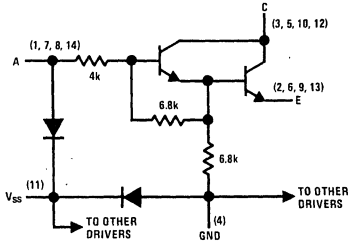
The DS75491 and DS75492 are interface circuits designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

Features

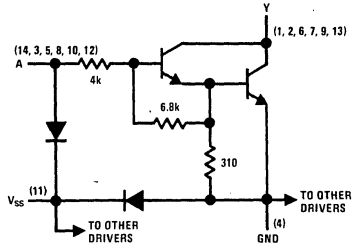
- 50 mA source or sink capability per driver (DS75491)
- 250 mA sink capability per driver (DS75492)
- MOS compatability (low input current)
- Low standby power
- High-gain Darlington circuits

Schematic and Connection Diagrams

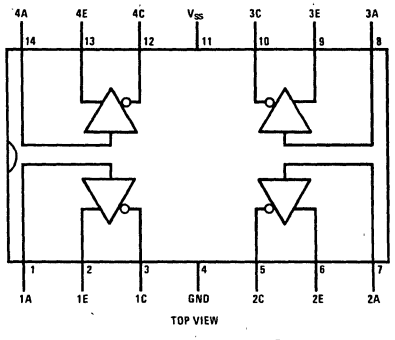
DS75491 (each driver)



DS75492 (each driver)

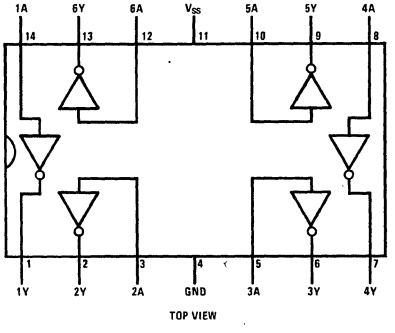


DS75491 Dual-In-Line Package



TOP VIEW

DS75492 Dual-In-Line Package



TOP VIEW

Order Number DS75491J, DS75492J, DS75491N or DS75492N
See NS Package J14A or N14A

Absolute Maximum Ratings (Note 1)

	DS75491	DS75492
Input Voltage Range (Note 4)	−5V to V_{SS}	−5V to V_{SS}
Collector Output Voltage (Note 5)	10V	10V
Collector Output to Input Voltage	10V	10V
Emitter to Ground Voltage ($V_I \geq 5V$)	10V	
Emitter to Input Voltage	5V	
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	10V
Collector Output Current		
Each Collector Output	50 mA	250 mA
All Collector Outputs	200 mA	600 mA
Continuous Total Dissipation	600 mW	600 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C	300°C
Maximum Power Dissipation at 25°C		
Cavity Package	1308 mW*	1364 mW†
Molded Package	1207 mW*	1280 mW†

*Derate cavity package 8.72 mW/°C above 25°C; derate molded package 9.66 mW/°C above 25°C.
†Derate cavity package 9.09 mW/°C above 25°C; derate molded package 10.24 mW/°C above 25°C.

Electrical Characteristics DS75491 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CE\ ON}$	"ON" State Collector Emitter Voltage	Input = 8.5V through 1 kΩ, V_E = 5V, I_C = 50 mA	T_A = 25°C		0.9	1.2	V
			T_A = 0–70°C			1.5	V
$I_{C\ OFF}$	"OFF" State Collector Current	V_C = 10V, V_E = 0V	I_{IN} = 40μA			100	μA
			V_{IN} = 0.7V			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, V_E = 0, I_C = 20 mA			2.2	3.3	mA
I_E	Emitter Reverse Current	V_{IN} = 0, V_E = 5V, I_C = 0				100	μA
I_{SS}	Current Into V_{SS} Terminal					1	mA

DS75492 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, I_{OUT} = 250 mA	T_A = 25°C		0.9	1.2	V
			T_A = 0–70°C			1.5	V
I_{OH}	High Level Output Current	V_{OH} = 10V	I_{IN} = 40μA			200	μA
			V_{IN} = 0.5V			200	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA			2.2	3.3	mA
I_{SS}	Current Into V_{SS} Terminal					1	mA

Switching Characteristics DS75491 (V_{SS} = 7.5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output (Collector)	V_{IH} = 4.5V, V_E = 0, R_L = 200Ω, C_L = 15 pF		100		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output (Collector)			20		ns

DS75492 (V_{SS} = 7.5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 7.5V, R_L = 39Ω, C_L = 15 pF		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS75491 and DS75492.

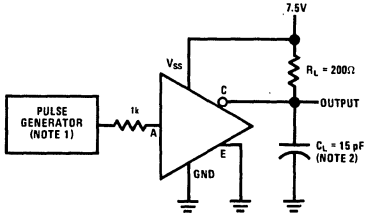
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The input is the only device terminal which may be negative with respect to ground.

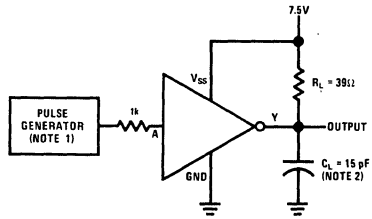
Note 5: Voltage values are with respect to network ground terminal unless otherwise noted.

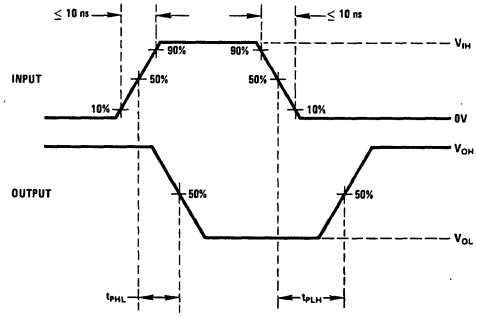
AC Test Circuits and Switching Time Waveforms

DS75491



DS75492





Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 100 kHz, t_W = 1μs.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor

DS55493/DS75493 Quad LED Segment Driver

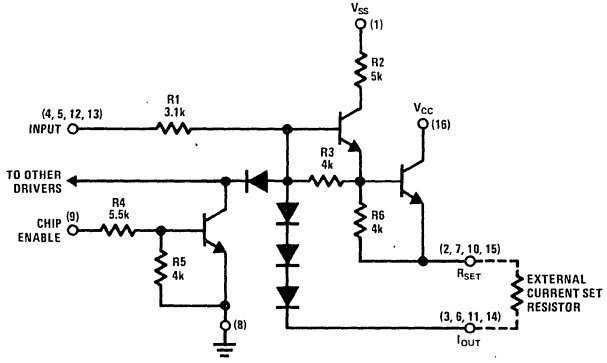
General Description

The DS55493/DS75493 is a quad LED segment driver. It is designed to interface between MOS IC's and LED's. An external resistor is required for each segment to drive the output current which is approximately equal to $0.7V/R_L$ and is relatively constant, independent of supply variations. Blanking can be achieved by taking the chip enable (CE) to a logical "1" level.

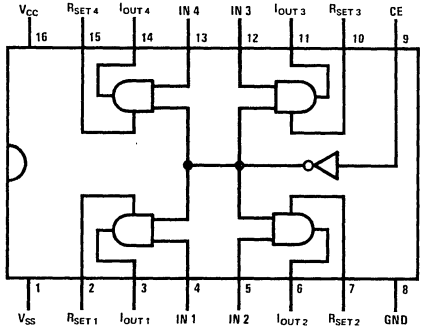
Features

- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Output current regulation
- Quad high gain circuits

Schematic and Connection Diagrams

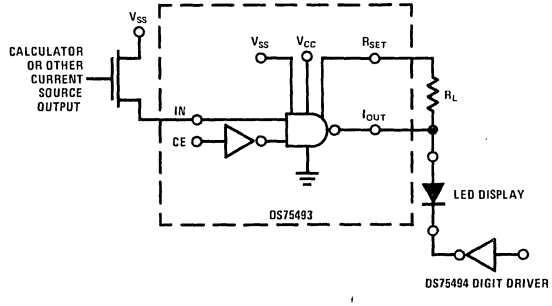


Dual-In-Line Package



Order Number DS55493J, DS75493J
or DS75493N
See NS Package J16A or N16A

Typical Application



Truth Table

CE	V_{IN}	I_{OUT}
0	1	ON
0	0	OFF
1	X	OFF

X = Don't care

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	V_{CC}
Storage Temperature Range	−65°C to +150°C
Output Current (I_{OUT})	−25 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.14 mW/°C above 25°C; derate molded package 10.24 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{CC}	3.2	8.8	V
V_{SS}	6.5	8.8	V
Temperature, T_A			°C
DS75493	0	+70	°C
DS55493	−55	+125	°C

Electrical Characteristics ($V_{SS} \geq V_{CC}$) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{IN}	Input Current	V_{SS} = Max, V_{IN} = 8.8V, V_{CC} = Open, V_{CE} = 0V				3.2	mA
		I_{OUT} = R_{SET} @ 0V, V_{CE} = 8.8V				3.6	mA
I_{CE}	Chip Enable Input Current	V_{CC} = Max, V_{SS} = Max, V_{CE} = 8.8V, All Other Pins to Gnd				2.1	mA
I_{OUT}	Output Current	I_{OUT} @ 2.15V, R_L = 50Ω	V_{CC} = Min, V_{SS} = 6.5V, I_{CE} = 80μA, V_{IN} = 6.5V Through 1.0 kΩ	−8	−13		mA
			V_{CE} = 0V, V_{IN} = 8.8V		−16	−20	mA
I_{OL}	Output Leakage Current	I_{OUT} = R_{SET} @ 0V, Measure Current to Gnd, V_{SS} = 8.8V	V_{CC} = Min, V_{CE} = 0V V_{IN} = 8.8V Through 100 kΩ			−100	μA
			V_{CE} = 6.5V Through 1.0 kΩ, V_{IN} = 8.8V			−200	μA
I_{CC}	Supply Current, V_{CC}	V_{CC} = Max, V_{SS} = Max, All Other Pins to Gnd				40	μA
I_{SS}	Supply Current	V_{CC} = 0V, All Other Pins to Gnd				40	μA
		V_{CC} = Min, V_{SS} = 8.8V	I_{OUT} @ 2.15V, V_{CE} = 8.8V Through 100 kΩ, R_L = 50Ω		0.5	1.5	mA
			I_{OUT} = Open, R_{SET} = Open, V_{CE} = 0V			1.4	mA

Switching Characteristics T_A = 25°C, nominal power supplies unless otherwise noted

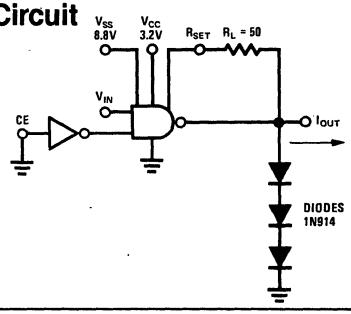
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd(OFF)}$	Propagation Delay to a Logical "0" From Input to Output	(See AC Test Circuit)		170	300	ns
$t_{pd(ON)}$	Propagation Delay to a Logical "1" From Input to Output	(See AC Test Circuit)		11	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

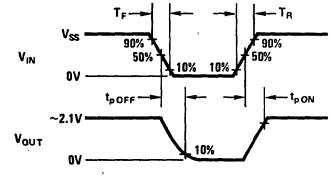
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75493 and across the −55°C to +125°C range for the DS55493.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit



Switching Time Waveforms



National Semiconductor

Display Controllers/Drivers

DS55494/DS75494 Hex Digit Driver

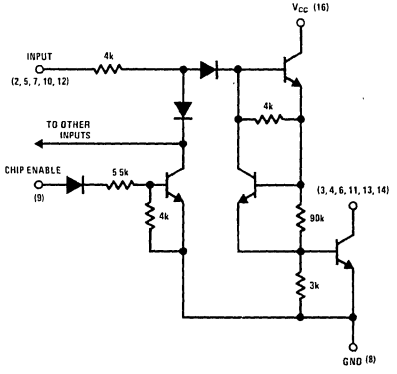
General Description

The DS55494/DS75494 is a hex digit driver designed to interface between most MOS devices and common cathodes configured LED's with a low output voltage at high operating currents. The enable input disables all the outputs when taken high.

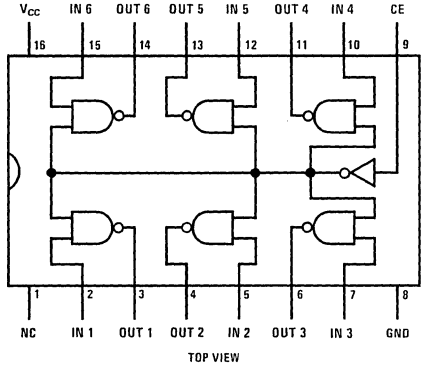
Features

- 150 mA sink capability
- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Low voltage saturating outputs
- Hex high gain circuits

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS55494J, DS75494J or DS75494N
See NS Package J16A or N16A

Truth Table

ENABLE	V_{IN}	V_{OUT}
0	0	1
0	1	0
1	X	1

X = don't care

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.55 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	3.2	8.8	V
Temperature, T_A			
DS75494	0	+70	°C
DS55494	−55	+125	°C

Electrical Characteristics (Notes 2 and 3)

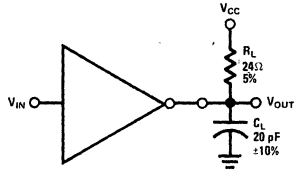
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{CC} = Min, V_{IN} = 8.8V	V_{CE} = 8.8V through 100k				2.0	mA
			V_{CE} = 8.8V				2.7	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = −5.5V					−20	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OH} = 8.8V	V_{IN} = 8.8V through 100k, V_{CE} = 0V				400	μA
			V_{IN} = 8.8V, V_{CE} = 6.5V through 1.0k				400	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 150 mA, V_{IN} = 6.5V through 1.0k, V_{CE} = 8.8V through 100k		DS75494		0.25	0.35	V
				DS55494		0.25	0.4	V
I_{CC}	Supply Current	V_{CC} = Max	One Driver "ON", V_{IN} = 8.8V	DS75494			8.0	mA
				DS55494			10.0	mA
			All Other Pins to GND	V_{CE} = 6.5V through 1.0k			100	μA
				V_{IN} = 8.8V through 100k			100	μA
			All Other Pins to GND				40	μA
t_{OFF}	Output "OFF" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See ac Test Circuits				0.04	1.2	μs
t_{ON}	Output "ON" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See ac Test Circuits				13	100	ns

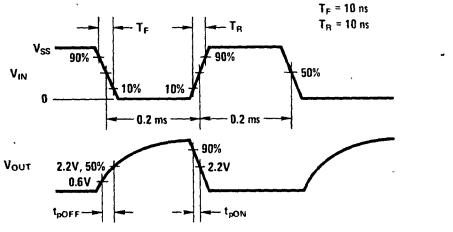
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75494 and across the −55°C to +125°C range for the DS55494.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuit and Switching Time Waveforms





DS8654 8-Output Display Driver (LED, VF, Thermal Printer) DS8656 Diode Matrix

General Description

DS8654 is an 8-digit driver with emitter/follower outputs. It can source up to 50 mA at a low impedance, and operates with a constant internal drive current over a wide range of power supply—from 4.5V to 33V. The DS8654 can be used to drive electrical or mechanical, multiplexed or unmultiplexed display systems. It can be used as a segment driver for common cathode displays with external current limiting resistors or can drive incandescent or fluorescent displays directly, both digits (anodes) and segments (grids). It will be necessary to run the device at a lower duty cycle, to keep the maximum package dc power dissipation less than 600 mW while operating all 8 outputs at high supply voltage and large source current. The inputs are MOS compatible and eliminate the need for level shifting since inputs are referenced to the most negative supply of system.

System Description

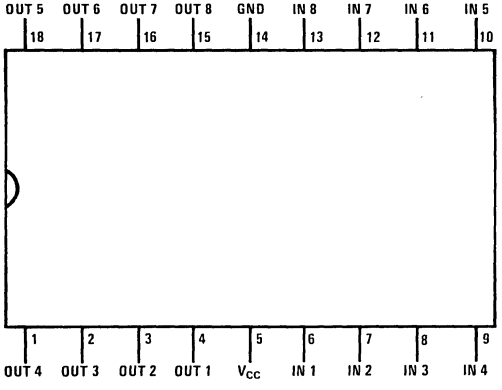
The DS8654 and DS8656 are specifically designed to operate a thermal printing head for calculator or other uses. In this application the same segment in each digit is selected at the same time, reducing the overall time for a complete print cycle. The DS8654 is an 8-digit driver. With a 15-digit print head, two of the DS8654 are required.

The DS8656 diode arrays are used to prevent "sneak" currents in the resistive print head. In a 15-digit print head with one alphanumeric digit there are 119 resistor segments requiring 119 diodes. For ease of assembly, the DS8656 is configured in four groups of three common cathode diodes in each group. In the system, ten parts of DS8656 are required.

The whole system is designed to operate from a +19V supply for the print head and an 8-cell nickel-cadmium battery supplying −8V to −11.6V for the rest of the electronics. The 8-segment drive transistors require LV_{CER}'s of 33V min, β of > 100 at I_C = 500 mA, and $V_{SAT} \leq 1.0$V at 800 mA with 15 mA drive.

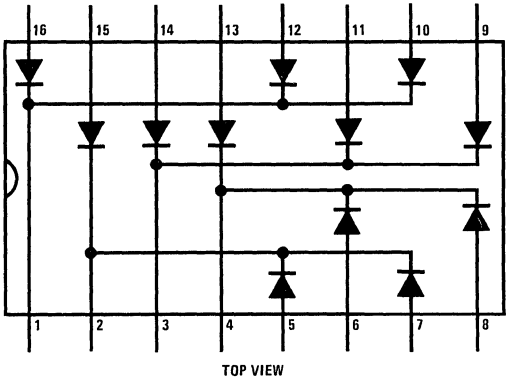
Connection Diagrams

Dual-In-Line Package



Order Number DS8654N
See NS Package N18A

Dual-In-Line Package



TOP VIEW

Order Number DS8656N
See NS Package N16A

Absolute Maximum Ratings DS8654 (Note 1)

Supply Voltage	36V
Input Voltage	36V
Output Voltage	V_{CC} − 36V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation at 25°C	
Molded Package (DS8654)*	1563 mW
Molded Package (DS8656)†	1280 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 12.5 mW/°C above 25°C.

†Derate molded package 10.24 mW/°C above 25°C.

Operating Conditions DS8654

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	33	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics DS8654 (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 6.5V		390	500	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V		13	40	μA
I_{OFF}	"Off" State Leakage Current	V_{OUT} = V_{CC} − 33V		0.01	−100	μA
V_{ON}	"On" State Output Voltage	V_{CC} = Max, I_{IN} = 500μA, I_{OH} = −50 mA		V_{CC}−1.8	V_{CC}−2.5	V
$I_{CC(OFF)}$	Supply Current	V_{CC} = Max, V_{IN} = V_{OUT} = Gnd		0.01	1.0	mA
$I_{CC(ON)}$	Supply Current (All Outputs "ON")	V_{CC} = Max, V_{IN} = 6.5V, I_{OUT} = 0 mA		7.5	10	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8654. All typicals are given for V_{CC} = 30V and T_A = 25°C.

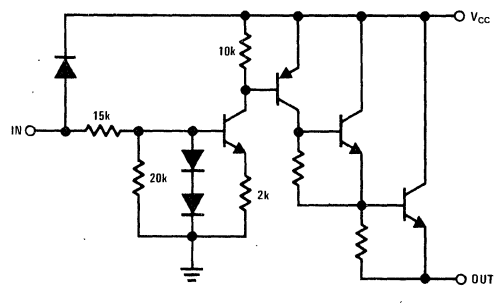
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Electrical Characteristics DS8656 (T_A = 0°C to +70°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_R	Peak Inverse Voltage	I_R = 0.1 mA	35			V
V_F	Forward Voltage	I_F = 50 mA			1.5	V
t_r	Reverse Recov. Time	I_F = 50 mA to I_R = 0.1 mA at V_R = 30V			1.0	μs

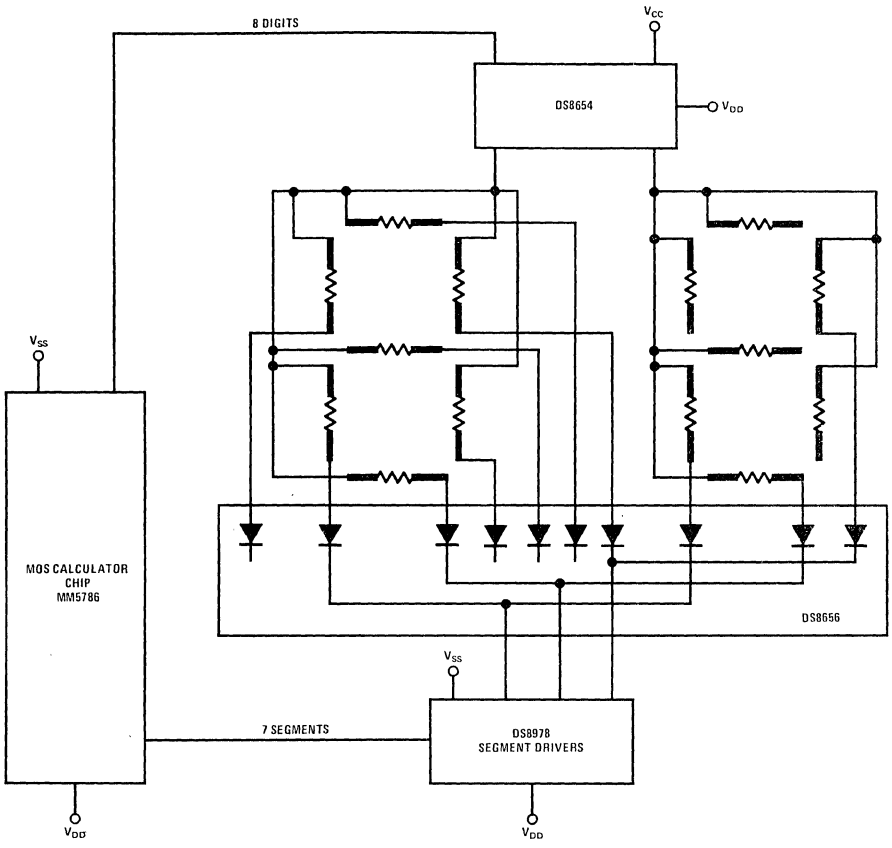
Schematic Diagram

DS8654

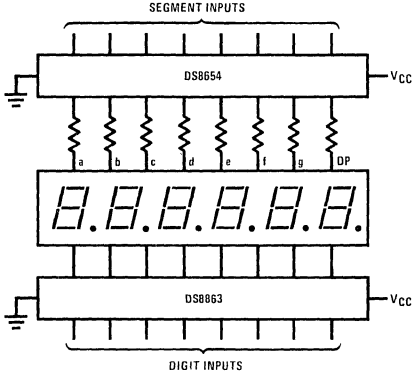


Typical Applications

Thermal Printer

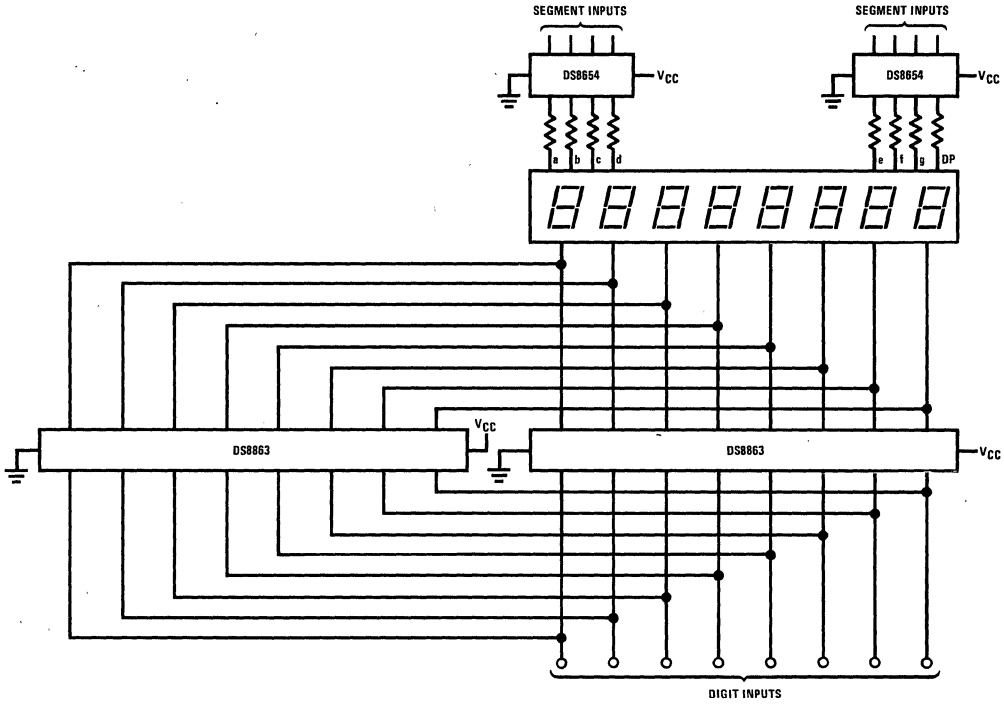


LED Display—0 mA to 50 mA Peak Segment Current

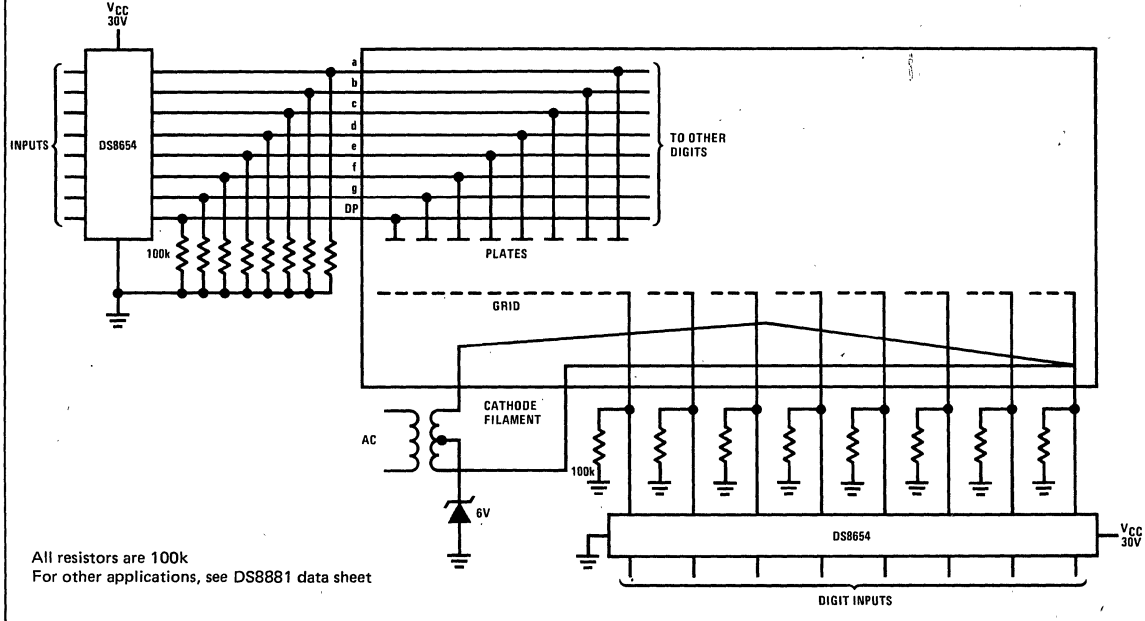


Typical Applications (Continued)

LED Display—50 mA to 100 mA Peak Segment Current



VF Display



All resistors are 100k
For other applications, see DS8881 data sheet

National Semiconductor

DS8664 14-Digit Decoder/Driver With Low Battery Indicator

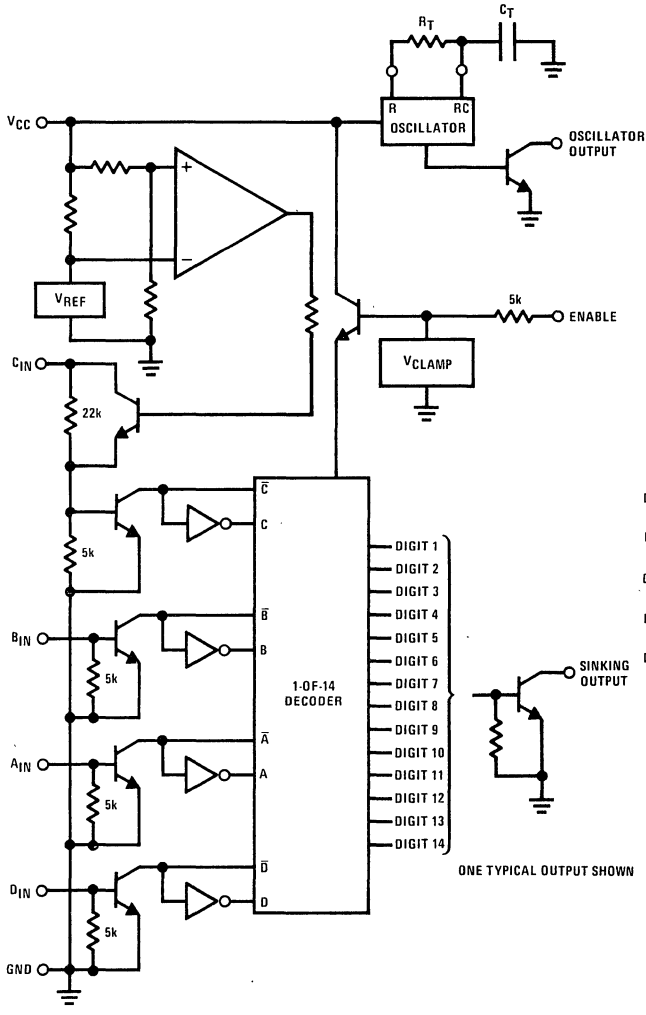
General Description

The DS8664 circuit is a 14-digit decoder/driver with an 80 mA sink capability. The circuit has current threshold inputs, and is designed to be driven by P-channel MOS. The enable input permits interdigit blanking of the decoded outputs. An open-collector output oscillator is provided for system timing (two passive external components are required). A low-battery indicator is provided at the "C" input with a nominal trip point of 3.25V at 25°C.

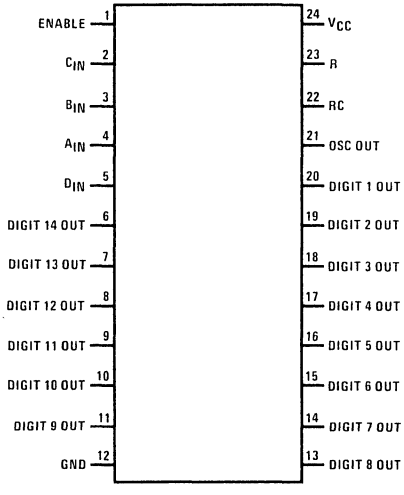
Features

- Oscillator frequency accuracy allows maximum system speed
- Inter-digit blanking with the enable input provides ghost-free display operation
- Low-battery indicator accuracy provides consistent low-battery indication

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS8664N
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	±10V
Input Current	±1.5 mA
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	2005 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 16.04 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	2.9	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage Decoder Inputs	V_{CC} = Max, V_{ENABLE} = 4.9V	I_{IN} = 260μA	0.50			V
			I_{IN} = 1400μA			1.50	V
V_{IH}	Enable Input	V_{CC} = Max, I_{ENABLE} = 260μA, T_A = 25°C		3.0	4.2	5.1	V
I_{IH}	Logical "1" Input Current Decoder Inputs	V_{CC} = Max, V_{ENABLE} = 4.9V		260			μA
I_{IH}	Enable Input	V_{CC} = Max		260			μA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max, V_{ENABLE} = 4.9V, I_{IL} = 25μA	A_{IN},B_{IN},D_{IN}			0.30	V
			C_{IN}			0.50	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{ENABLE} = 4.9V, V_{IL} = Max				25	μA
V_{OH}	C Input (Low-Battery Output)	V_{CC} = 3.1V, T_A = 25°C	I_{IN} = 300μA	4.9	7.3		V
			I_{IN} = 400μA	6.5	10.0		V
V_{OL}	C Input (Low-Battery Output)	V_{CC} = 3.4V, I_{IN} = 1300μA, T_A = 25°C			1.0	3.0	V
I_{OH}	Logical "1" Output Current Except Pin R	V_{CC} = Max, V_{OH} = 10.0V, V_{ENABLE} = 4.9V, V_{RC} = 0.6V				50	μA
I_{OS}	Output Short Circuit Current Pin R Only	V_{CC} = Max, V_{RC} = 0.6V		−0.15	−0.28	−0.45	mA
V_{OL}	Logical "0" Output Voltage Digit Outputs	V_{CC} = Min, I_{OL} = 80 mA, V_{ENABLE} = 4.9V			0.35	0.55	V
$V_{OL(OSC)}$	Oscillator Output	V_{CC} = Min, I_{OL} = 6 mA, V_{RC} = 1.5V			0.20	0.55	V
V_{OL}	Pin R	V_{CC} = Min, I_{OL} = 60μA, V_{RC} = 1.5V			0.10	0.25	V
I_{CC}	Supply Current—Enabled	V_{CC} = Max, V_{ENABLE} = 4.9V			15.0	22.0	mA
I_{CC}	Supply Current—Disabled	V_{CC} = Max, V_{ENABLE} = 1.0V			6.0	12.0	mA
f_{OSC}	Oscillator Frequency	R_T = 35k ±2%, C_T = 100 pF ±5%,	V_{CC} = Min to 4.5V	300	350	400	kHz
		R_T = 33k ±2%, C_T = 100 pF ±5%,	V_{CC} = 7.9V to Max	320	360	400	kHz
D.C.	Duty Cycle (t_{PWH}/τ)	R_T = 35k ±2%, C_T = 100 pF ±5%,	V_{CC} = Min to 4.5V	0.46	0.56	0.66	
		R_T = 33k ±2%, C_T = 100 pF ±5%,	V_{CC} = 7.9V to Max	0.46	0.56	0.66	

Switching Characteristics V_{CC} = 4.0V, T_A = 25°C unless otherwise specified.

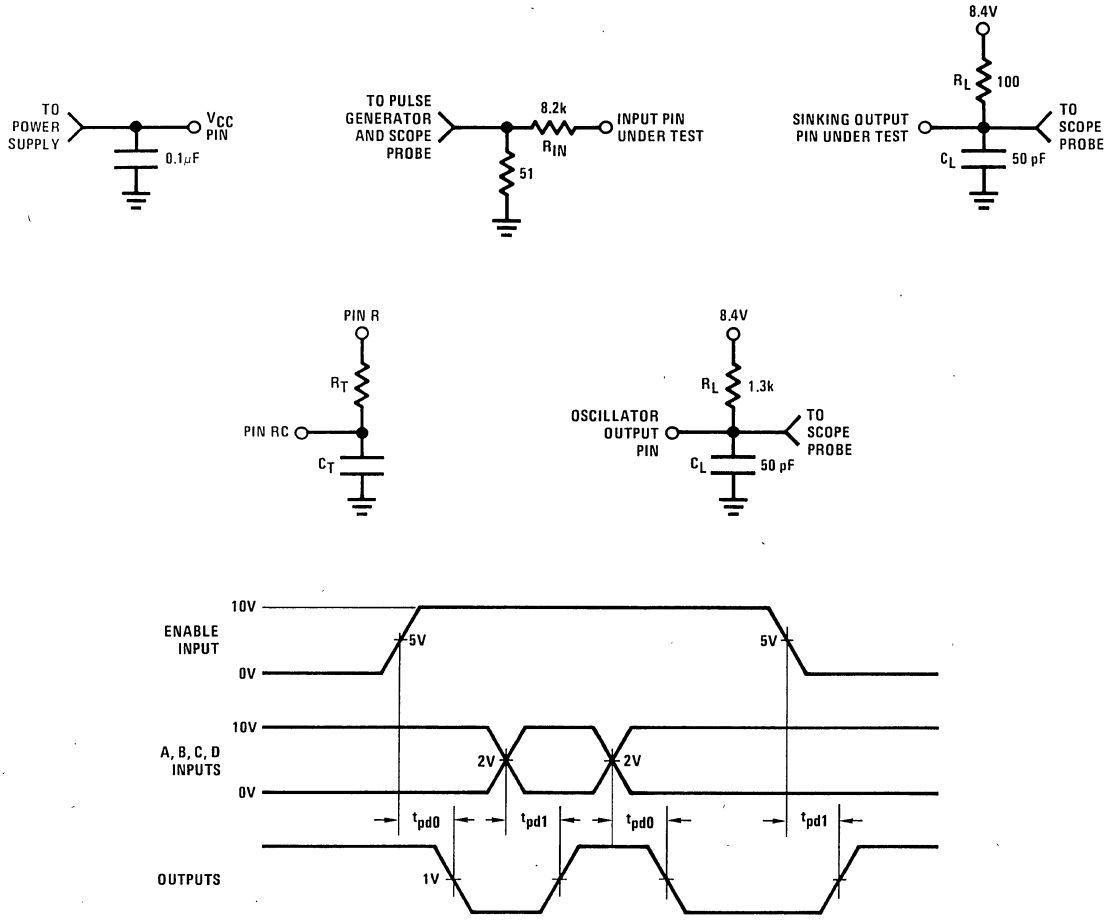
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1} or t_{pd0}	Propagation Delay From A, B, C, D Inputs to Digit Outputs	R_{IN} = 8.2k, V_{ENABLE} = 10V, R_L = 100Ω, C_L = 50 pF			500	ns
t_{pd0}	Propagation Delay to a Logical "0" From Enable Input to Digit Outputs	R_{IN} = 8.2k, R_L = 100Ω, C_L = 50 pF	30	80	200	ns
t_{pd1}	Propagation Delay to a Logical "1" From Enable Input to Digit Outputs	R_{IN} = 8.2k, R_L = 100Ω, C_L = 50 pF	100	250	500	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range; all typical values are given for V_{CC} = 4.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuits and Switching Time Waveforms



Note: Input voltage rise and fall times are 120 ns from 10% to 90% points.

Truth Table

A_{IN}	B_{IN}	C_{IN}	D_{IN}	DIG. OUT ON
0	0	0	0	NONE
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13
0	1	1	1	14
1	1	1	1	NONE

National Semiconductor

DS8666 14-Digit Decoder/Driver

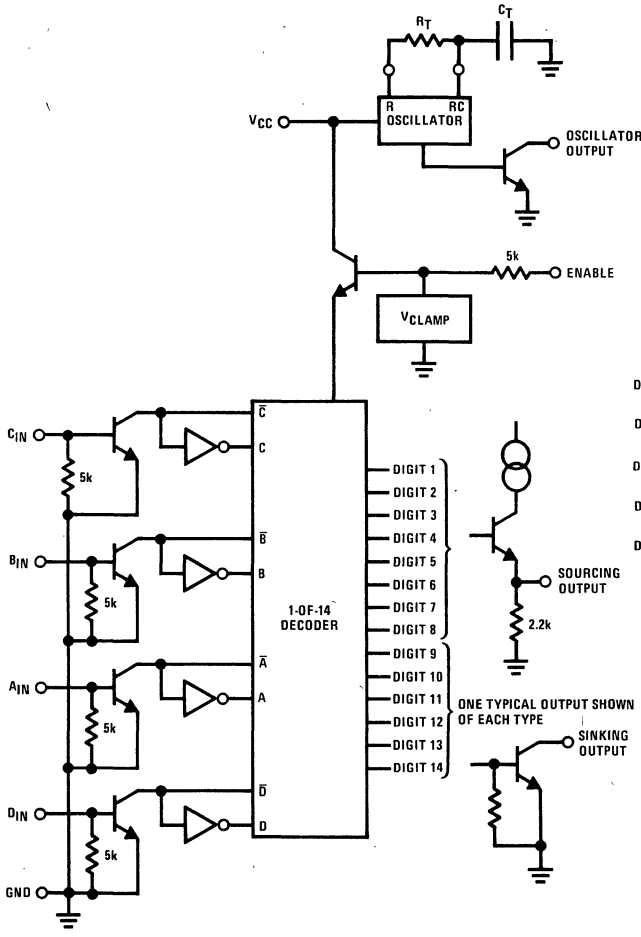
General Description

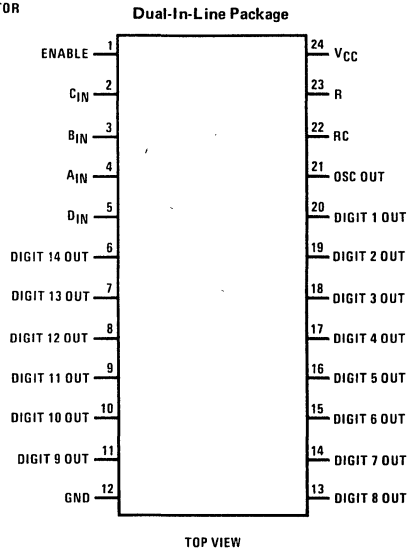
The DS8666 circuit is a 14-digit decoder/driver. Six outputs have an 80 mA sink capability, and eight of the outputs have a 13 mA nominal source drive capability to drive external grounded-emitter transistor bases. The circuit has current threshold inputs, and is designed to be driven by P-channel MOS. An enable input is provided to allow for inter-digit blanking of the decoded outputs. An open-collector output oscillator is provided for system timing (two passive external components are required).

Features

- Oscillator frequency accuracy allows maximum system speed
- Inter-digit blanking with the enable input provides ghost-free display operation

Logic and Connection Diagrams





TOP VIEW

Order Number DS8666N
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Input Current	±1.5 mA
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	2005 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 16.04 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	7.9	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage Decoder Inputs	V_{CC} = Max, V_{ENABLE} = 6.7V	I_{IN} = 390 μA	0.50			V
			I_{IN} = 1400 μA			1.50	V
V_{IH}	Enable Input	V_{CC} = Max, I_{ENABLE} = 140 μA		5.0	6.3	7.0	V
I_{IH}	Logical "1" Input Current Decoder Inputs	V_{CC} = Max, V_{ENABLE} = 6.7V		390			μA
I_{IH}	Enable Input	V_{CC} = Max		140			μA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max, V_{ENABLE} = 6.7V, I_{IL} = 25 μA				0.30	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{ENABLE} = 6.7V, V_{IL} = Max				25	μA
$I_{OH(OSC)}$	Oscillator Output	V_{CC} = Max, V_{OH} = 10.0V, V_{RC} = 0.6V				50	μA
I_{OH}	Digit 1–8 Outputs	V_{CC} = Max, V_{OH} = 1.00V, V_{ENABLE} = 6.7V		−7.0	−13.0	−20.0	mA
I_{OH}	Logical "1" Output Current Digit 9–14 Outputs	V_{CC} = Max, V_{OH} = 10.0V, V_{ENABLE} = 6.7V				50	μA
I_{OS}	Output Short-Circuit Current Pin R Only	V_{CC} = Max, V_{RC} = 0.6V		−0.15	−0.30	−0.45	mA
$V_{OL(OSC)}$	Oscillator Output	V_{CC} = Min, I_{OL} = 6 mA, V_{RC} = 1.5V				0.50	V
V_{OL}	Logical "0" Output Voltage Digit 1–8 Outputs	V_{CC} = Min, V_{ENABLE} = 6.7V	I_{OL} = 40 μA			0.40	V
	Digit 9–14 Outputs		I_{OL} = 80 mA		0.35	0.50	V
	Pin R		I_{OL} = 60 μA, V_{RC} = 1.5V		0.10	0.20	V
I_{CC}	Supply Current—Enabled	V_{CC} = Max, V_{ENABLE} = 6.7V, V_{OH} = 1.00V, (Sourcing Output "ON")			26.0	35.0	mA
I_{CC}	Supply Current—Disabled	V_{CC} = Max, V_{ENABLE} = 1.0V			5.0	7.0	mA
f_{OSC}	Oscillator Frequency	R_T = 33k ±2%, C_T = 100 pF ±5%	V_{CC} = Min	320	360	400	kHz
			V_{CC} = Max				
D.C.	Duty Cycle (t_{PWH}/τ)	R_T = 33k ±2%, C_T = 100 pF ±5%	V_{CC} = Min	0.46	0.56	0.66	
			V_{CC} = Max				

Switching Characteristics V_{CC} = 8.4V, T_A = 25°C

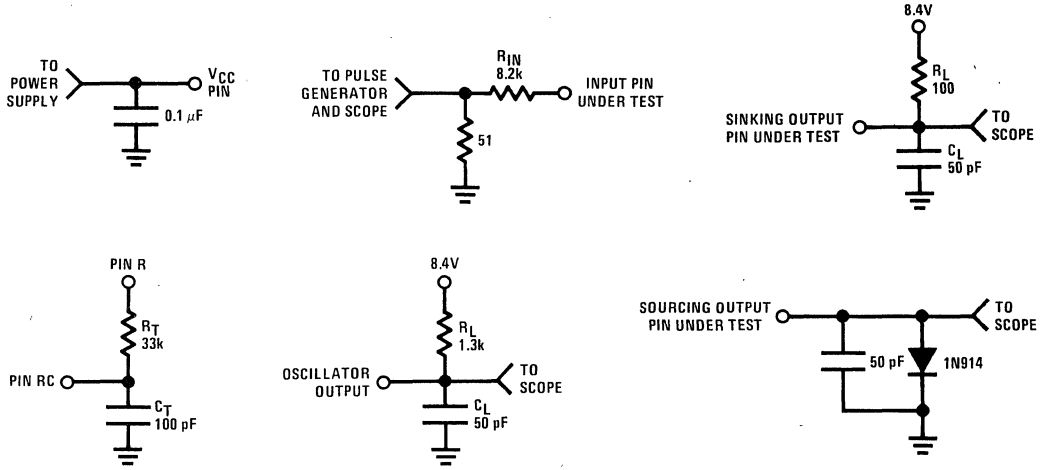
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0} or t_{pd1}	Propagation Delay From A, B, C, D Inputs to Digit Outputs	R_{IN} = 8.2k, V_{ENABLE} = 10V, C_L = 50 pF			500	ns
t_{pd0} or t_{pd1}	Propagation Delay From Enable Input to Digit Outputs	R_{IN} = 8.2k, C_L = 50 pF			500	ns

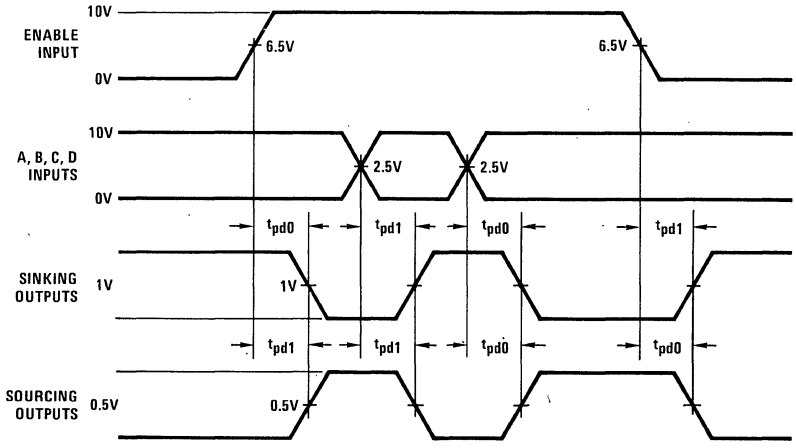
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C for the DS8666. All typicals are given for V_{CC} = 8.4V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

AC Test Circuits and Switching Time Waveforms





Note. Input rise and fall times are 120 ns between 10% and 90% points.

Truth Table

A_{IN}	B_{IN}	C_{IN}	D_{IN}	DIG. OUT ON
0	0	0	0	NONE
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13
0	1	1	1	14
1	1	1	1	NONE

DS8669 2-Digit BCD to 7-Segment Decoder/Driver

General Description

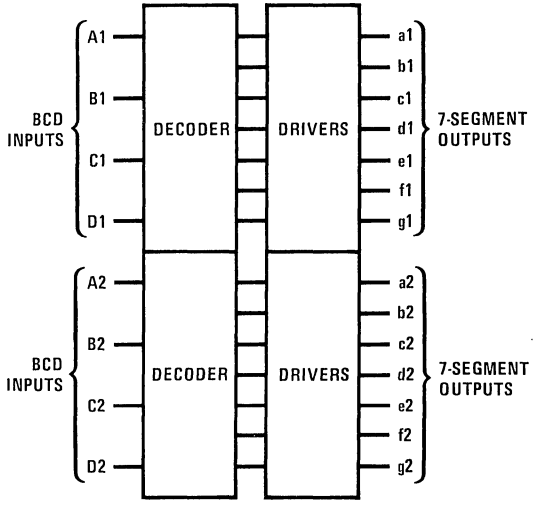
The DS8669 is a 2-digit BCD to 7-segment decoder/driver for use with common anode LED displays. The DS8669 drives 2 7-segment LED displays without multiplexing. Outputs are open-collector, and capable of sinking 25 mA/segment. Applications include TV and CB channel displays.

Features

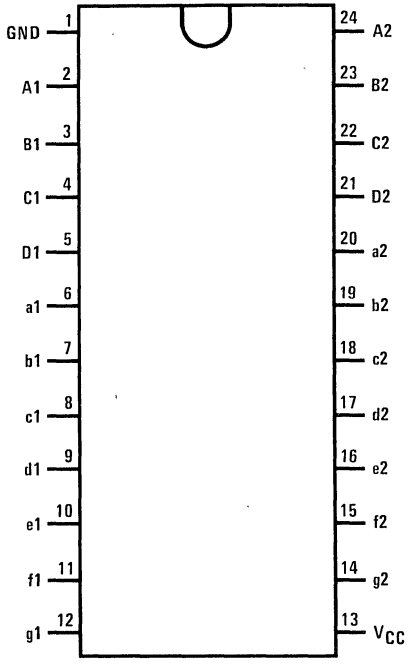
- Direct 7-segment drive
- 25 mA/segment current sink capability
- Low power requirement—16 mA typ
- Very low input currents—2 μA typ
- Input clamp diodes to both V_{CC} and ground
- No multiplexing oscillator noise

5

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS8669N
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Current	20 mA
Output Voltage	12V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	2005 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 16.04 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	6.0	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics V_{CC} = 5.25V, (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min	2.0		V_{CC}+0.6	V
V_{IL}	Logical "0 ' Input Voltage	V_{CC} = Min	−0.3		0.8	V
I_o	Logical "1" Output Leakage Current	V_{CC} = Max, V_{OUT} = 10V			50	μA
V_{OL}	Logical "0" Output Voltage	I_{OL} = 25 mA, V_{CC} = Min		0.4	0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = V_{CC} = Max		2.0	10	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0V, V_{CC} = Max		−0.1	−10	μA
I_{CC}	Supply Current	All Outputs Low, V_{CC} = Max		16	25	mA
V_{IC}	Input Clamp Voltage	I_{IN} = 10 mA			V_{CC}+1.5V	V
		I_{IN} = −10 mA			−1.5	V
t_{pd0}	Propagation Delay to a Logical "0" From Any Input to Any Output	R_L = 400Ω, C_L = 50 pF, T_A = 25°C			10	μs
t_{pd1}	Propagation Delay to a Logical "1" From Any Input to Any Output				10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8669. All typicals are given for V_{CC} = 5.25V and T_A = 25°C.

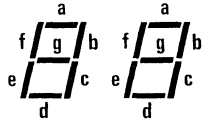
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Truth Table

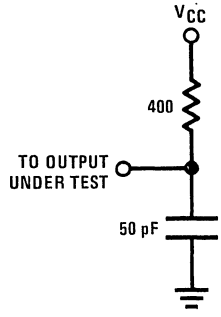
INPUT LEVELS				SEGMENT OUTPUTS														
D_N	C_N	B_N	A_N	a1	b1	c1	d1	e1	f1	g1	a2	b2	c2	d2	e2	f2	g2	DISPLAY 1	DISPLAY 2
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
0	0	0	1	1	0	0	1	1	1	1	1	0	0	1	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	0	0	1	0	0	1	0	2	2
0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1	1	0	3	3
0	1	0	0	1	0	0	1	1	0	0	1	0	0	1	1	0	0	4	4
0	1	0	1	0	1	0	0	1	0	0	0	1	0	0	1	0	0	5	5
0	1	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	6	6
0	1	1	1	0	0	0	1	1	1	1	0	0	0	1	1	1	1	7	7
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8	8
1	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	9	9
1	0	1	0	0	1	1	0	0	0	1	1	0	0	1	0	0	0	C	H
1	0	1	1	0	0	0	1	0	0	0	1	0	0	0	0	1	1	A	J
1	1	0	0	0	0	1	1	0	0	0	1	1	1	0	0	0	1	P	L
1	1	0	1	0	1	1	0	0	0	0	0	1	1	1	0	0	0	E	F
1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	0	-	-
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	(Blank)	(Blank)

"0" = Segment ON
"1" = Segment OFF

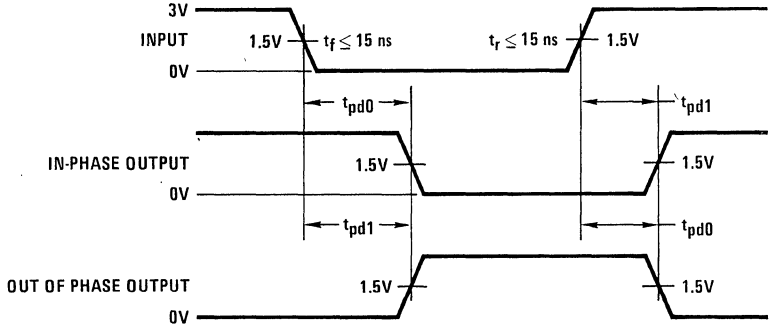
Display Segment Notation



AC Test Circuit



Switching Time Waveforms



National Semiconductor

DS8692, DS8693, DS8694 Printing Calculator Interface Set

General Description

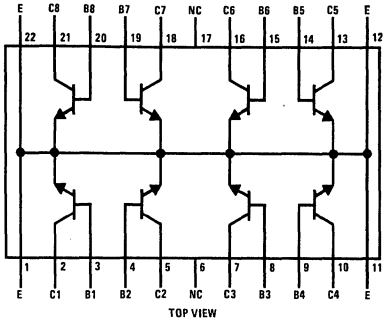
Two DS8692 IC's and one each of the DS8693 and DS8694 provide the complete interface necessary between the MM5787 calculator chip and the Seiko Model 310 printing head. The DS8692 is an array of eight common emitter output transistors each capable of sinking 350 mA, with open collector saturating outputs. The DS8693 contains the interface logic for the color solenoid driver, motor driver, and 7-column character select solenoid drivers. The DS8694 contains the interface logic for 8-column solenoid drivers plus the clock oscillator and timing signal buffer. The color and character select solenoid latch outputs of both are constant current outputs supplying the base current for the DS8692 arrays. These outputs also feature active pull-down. The motor drive latch output is an open collector capable of sinking 20 mA.

Features

- Provides complete interface package for printing calculators with minimum number of packages and minimum number of external components
- 350 mA sink capability

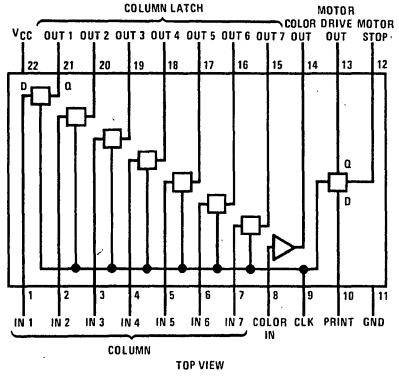
Connection Diagrams

Dual-In-Line Package



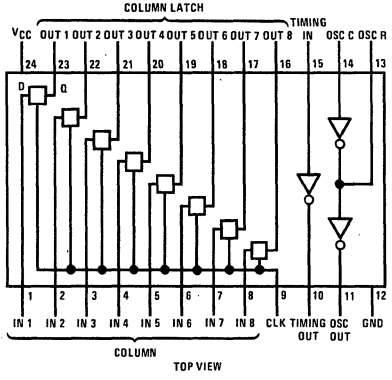
Order Number DS8692N
See NS Package N22A

Dual-In-Line Package



Order Number DS8693N
See NS Package N22A

Dual-In-Line Package



Order Number DS8694N
See NS Package N24A

Absolute Maximum Ratings DS8692—Transistor Array (Note 1)

Collector to Base Voltage	25V	Power Dissipation (T_A = 25°C)	650 mW
Collector to Emitter Voltage	25V	Operating Junction Temperature	150°C max
Collector to Emitter Voltage (Note 4)	15V	Operating Temperature Range	0°C to +70°C
Emitter to Base Voltage	6V	Storage Temperature Range	−65°C to +150°C
Collector Current (Continuous)	0.4A	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics DS8692 (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CEO}	Collector to Emitter Breakdown Voltage	I_C = 500 μA, I_B = 0	15			V
V_{CES}	Collector to Emitter Breakdown Voltage	I_C = 1 mA, V_{BE} = 0	25			V
V_{CBO}	Collector to Base Breakdown Voltage	I_C = 1 mA, I_E = 0	25			V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = 350 mA, I_B = 7.0 mA, (Note 7)		0.6	1.0	V
$V_{BE(SAT)}$	Base to Emitter Saturation Voltage	I_C = 350 mA, I_B = 7.0 mA, (Note 7)		0.8	1.05	V

Absolute Maximum Ratings DS8693 (Note 1)

Supply Voltage	12V
Input Voltage	12V
Output Voltage	
All Pins Except Pin 13	12V
Pin 13	19V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1897 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 15.18 mW/°C above 25°C.

Operating Conditions DS8693

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	8.5	11.0	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics DS8693 (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
COLUMN DRIVERS						
I_{IN}	Input Current	V_{IN} = 2.7V	50			μA
		V_{IN} = 9.5V			250	μA
V_{OL}	Output OFF Voltage	V_{CC} = Min, V_{IN} = 2.7V, V_{CLOCK} = 3.5V, I_{OUT} = 1 mA			0.4	V
I_{OH}	Output ON Current	V_{CC} = Min, V_{IN} = 7.0V, V_{CLOCK} = 3.5V, V_{OUT} = 1.0V	−7		−17	mA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_{IN} = 2.7V, V_{CLOCK} = 3.5V, V_{OUT} = 0V			−1.2	mA
CLOCK INPUT						
I_{IN}	Input Current	V_{IN} = 3.5V			300	μA
		V_{IN} = 1.6V	50			μA
V_{IH}	Logical "1" Input High Voltage		3.5			V
V_{IL}	Logical "0" Input Low Voltage				1.6	V
MOTOR DRIVER						
$I_{IN(PRINT)}$	Input Current	V_{IN} = 2.3V	50			μA
		V_{IN} = 9.5V			250	μA
$I_{IL(STOP)}$	Input Low Current (Stop)	V_{CC} = Min, $V_{IN(STOP)}$ = 0.4V, (Stop Switch Closed)			−700	μA
$V_{IH(STOP)}$	Input High Voltage (Stop)	V_{CC} = Max, $I_{IN(STOP)}$ = −10 μA, (Stop Switch Open)			2.5	V
V_{OL}	Output Low Voltage	V_{CC} = Min, V_{PRINT} = 7V, I_{OUT} = 15 mA			0.5	V

Electrical Characteristics (Continued) DS8693

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
MOTOR DRIVER (Continued)						
I_{OX}	Output Leakage Current	V_{CC} = Max, V_{PRINT} = 2.3V, V_{STOP} = 0.8V, V_{OUT} = 15V			100	μA
$I_{IH(STOP)}$	Logical "1" Input High Current				−10	μA
COLOR DRIVER						
I_{IN}	Input Current	V_{IN} = 3.5V			300	μA
		V_{IN} = 1.7V	50			μA
V_{OL}	Output OFF Voltage	V_{CC} = Min, V_{IN} = 1.7V, I_{OUT} = 1 mA			0.4	V
I_{OH}	Output ON Current	V_{CC} = Min, V_{IN} = 3.5V, V_{OUT} = 1.0V	−8		−18	mA
$I_{CC(SB)}$	Stand-by Supply Current, (Note 6)	V_{CC} = Max, $V_{COLUMN\ IN}$/V_{PRINT} = 0V, V_{COLOR} = 0V, V_{CLOCK} = 3.5V			55	mA

Absolute Maximum Ratings DS8694 (Note 1)

Supply Voltage	12V
Input Voltage	
All Pins Except Pin 15	12V
Pin 15	19V
Output Voltage	12V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	2005 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 16.04 mW/°C above 25°C.

Operating Conditions DS8694

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	8.5	11.0	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics DS8694 (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
COLUMN DRIVER						
I_{IN}	Input Current	V_{IN} = 2.7V			50	μA
		V_{IN} = 9.5V			250	μA
V_{OL}	Output OFF Voltage	V_{CC} = Min, V_{IN} = 2.7V, V_{CLOCK} = 3.5V, I_{OUT} = 1 mA			0.4	V
I_{OH}	Output ON Current	V_{CC} = Min, V_{IN} = 7.0V, V_{CLOCK} = 3.5V, V_{OUT} = 1.0V	−7		−17	mA
I_{OS}	Output Short-Circuit Current	V_{CC} = Max, V_{IN} = 2.7V, V_{CLOCK} = 3.5V, V_{OUT} = 0V			−1.2	mA
CLOCK INPUT						
I_{IN}	Input Current	V_{IN} = 3.5V			300	μA
		V_{IN} = 2.7V	50			μA
V_{IH}	Logical "1" Input High Voltage		3.5			V
V_{IL}	Logical "0" Input Low Voltage				1.6	V
TIMING BUFFER						
I_{IN}	Input Current	V_{IN} = 2V			−50	μA
		V_{IN} = 17V			880	μA
V_{OL}	Output Low Voltage	I_{OUT} = 50 μA, V_{IN} = 10V			0.5	V
V_{OH}	Output High Voltage	I_{OUT} = −50 μA, V_{IN} = 7V	V_{CC}−1.0			V
OSCILLATOR						
f_{OSC}	Frequency	V_{CC} = Max, R = 18k, C = 0.0015 μFd, (Note 5)	85	100	115	kHz
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OUT} = 50 μA			0.5	V
V_{OH}	Output High Voltage	I_{OUT} = −50 μA	V_{CC}−1.0			V
DC	Duty Cycle	V_{CC} = Max	40	50	60	%
V_{OSC}	Osc. V_{CC} Turn ON Voltage		6.0	7.7	8.5	V
$I_{CC(SB)}$	Stand-by Supply Current	V_{CC} = Max, $V_{COLUMN\ IN}$/ V_{PRINT} = 0V, I_{CLOCK} = 300 μA			55	mA

Switching Characteristics DS8694

V_{CC} = 5V, T_A = 25°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
COLUMN DRIVERS (DS8693, DS8694) *(Figure 3)*						
PW_{COLUMN}	Column In Pulse Width		1.1			μs
PW_{CLOCK}	Clock Pulse Width		1.0			μs
t_d	Delay of Column In Pulse After Clock Transitions to Low State for Output to Latch		0.1			μs
t_{PD0}	Propagation Delay to a Logical "0" From Clock to Column Out Output	Column In = 0V			10.0	μs
t_{PD1}	Propagation Delay to a Logical "1" From Clock to Column Output	Column In = 7V			1300	μs
t_{PD0}	Propagation Delay to a Logical "0" From Column In to Column Out	Clock = 7V			10	μs
t_{PD1}	Propagation Delay to a Logical "1" From Column In to Column Out	Clock = 7V			1300	μs
COLOR DRIVER (DS8693) *(Figure 4)*						
t_{PD0}	Propagation Delay to a Logical "0" From Color In to Color Out				10.0	μs
t_{PD1}	Propagation Delay to a Logical "1" From Color In to Color Out				10.0	μs
MOTOR DRIVER (DS8693) *(Figure 6)*						
PW_{PRINT}	Print Signal Pulse Width		1			μs
PW_{STOP}	Stop Signal Pulse Width		1			μs
PW_{CLOCK}	Clock Pulse Width		1			μs
t_{PD0}	Propagation Delay to a Logical "0" From Print to Motor Drive Out				10	μs
t_{PD1}	Propagation Delay to a Logical "1" From Motor Stop (High-to-Low Transition) to Motor Drive Out	Print = 0V, Clock = 7.0V			10	μs
TIMING SIGNAL BUFFER (DS8694) *(Figure 5)*						
PW_{TIMING}	Timing Signal Pulse Width		1	1000		ms
t_r	Rise Time	C_{LOAD} = 35 pF			500	ns
t_f	Fall Time	C_{LOAD} = 35 pF			500	ns
t_{PD0}	Propagation Delay to a Logical "0" From Timing In to Timing Out				10	μs
t_{PD1}	Propagation Delay to a Logical "1" From Timing In to Timing Out				10	μs
CLOCK OSCILLATOR (DS8694) *(Figure 7)*						
f_{OSC}	Oscillator Frequency	(Note 5)	85	100	115	kHz
DC	Duty Cycle		40	50	60	%
t_r	Rise Time	C_{LOAD} = 70 pF			500	ns
t_r	Fall Time	C_{LOAD} = 70 pF			500	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8692, DS8693, DS8694. All typicals are given for V_{CC} = 10V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute basis.

Note 4: Ratings refer to a high current point where collector-emitter voltage is lowest.

Note 5: Oscillator frequency is determined by external R between "Osc R" and "Osc C" and external C from "Osc C" to ground. 2k > R > 20k.

Note 6: Column outputs operate on approximately 1/16 duty cycle in normal operation.

Note 7: Measured with one output on at a time.

System Connection Diagram

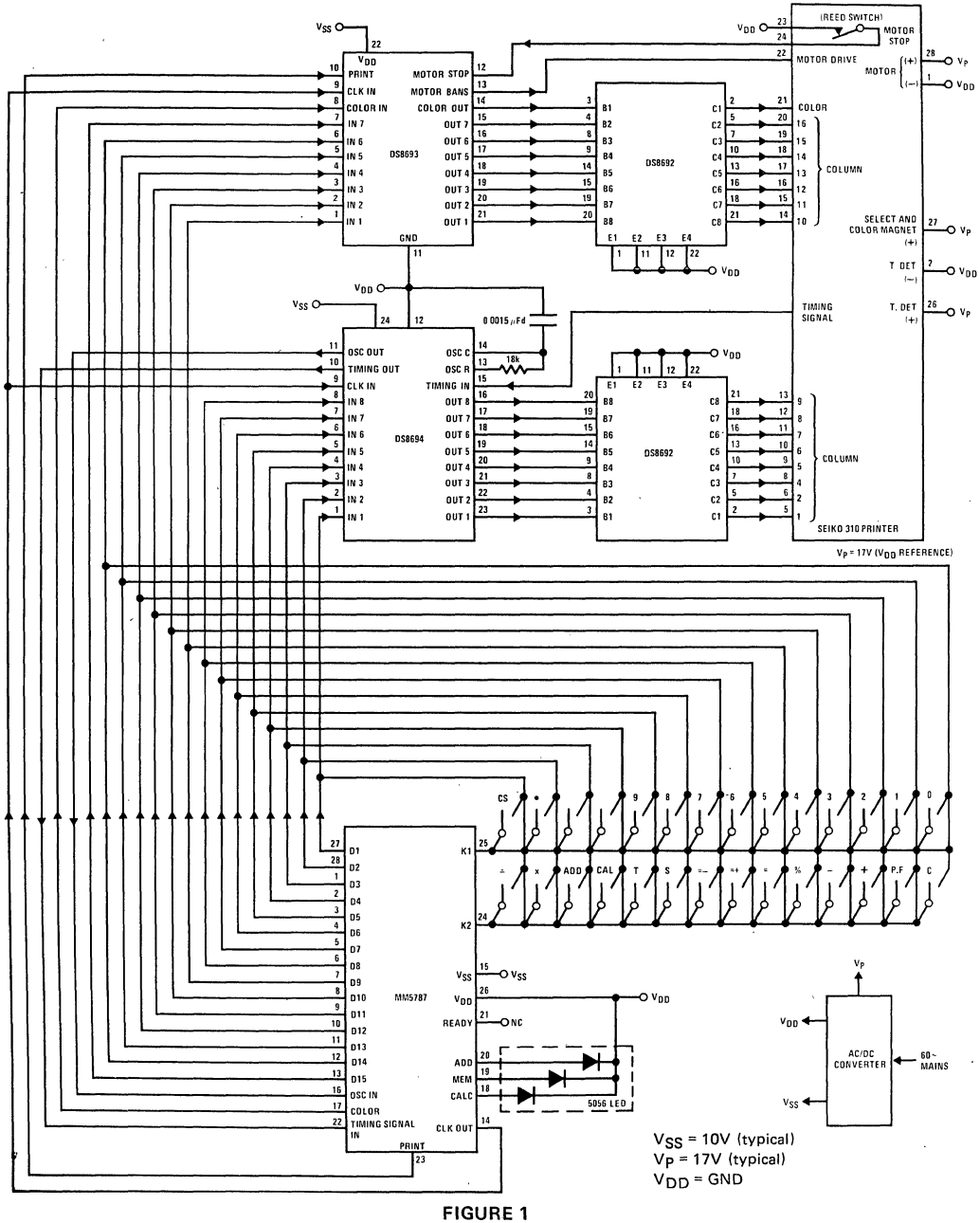
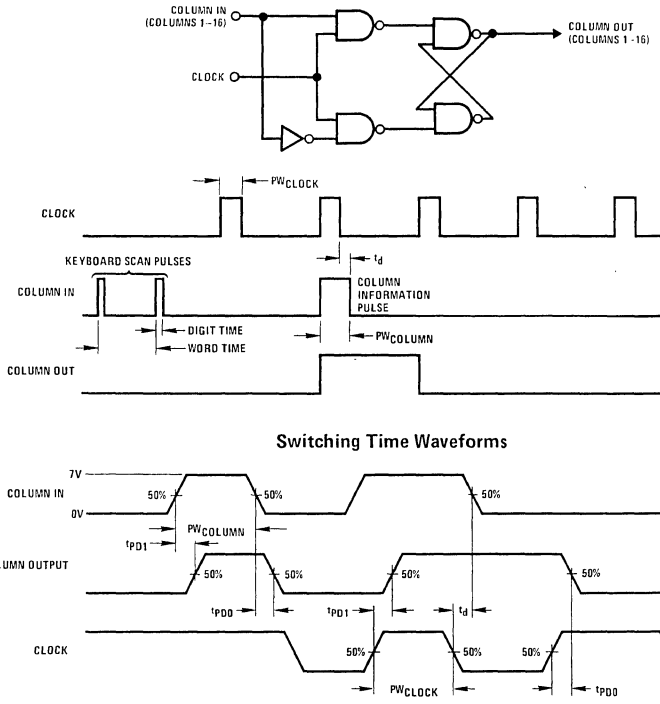


FIGURE 1

Logic and Timing Diagrams



Switching Time Waveforms

FIGURE 3. DS8693, DS8694 Column Latch

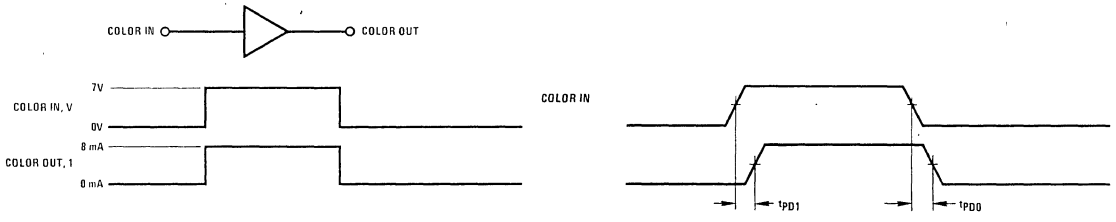


FIGURE 4. DS8693 Color Driver

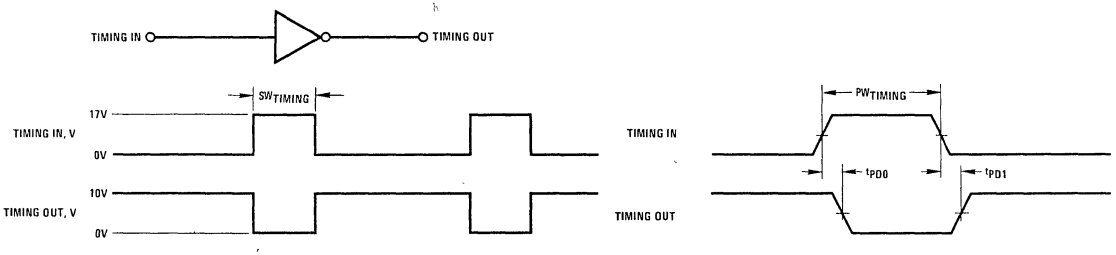
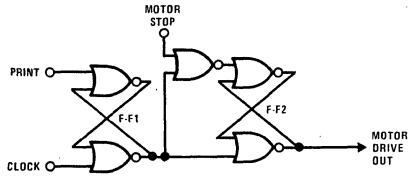
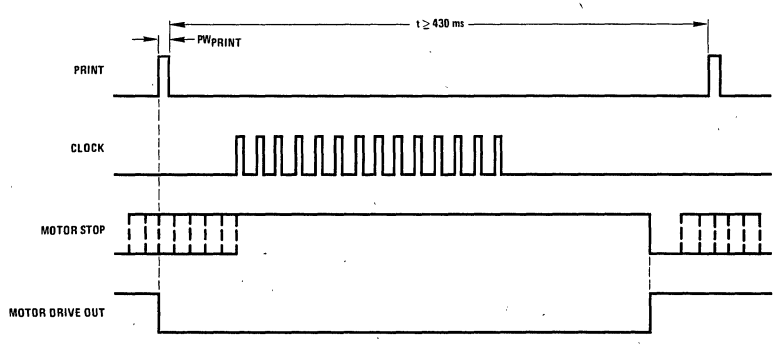


FIGURE 5. DS8694 Timing Signal Buffer

Logic and Timing Diagrams





Switching Time Waveforms

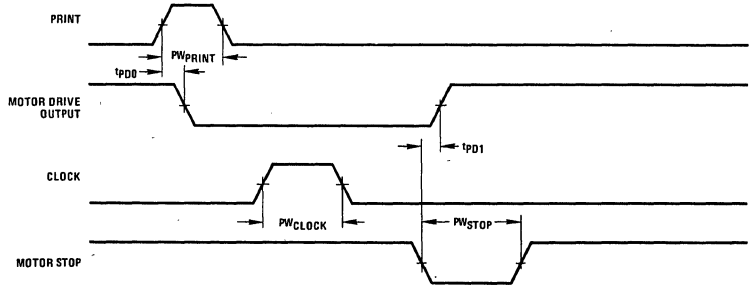
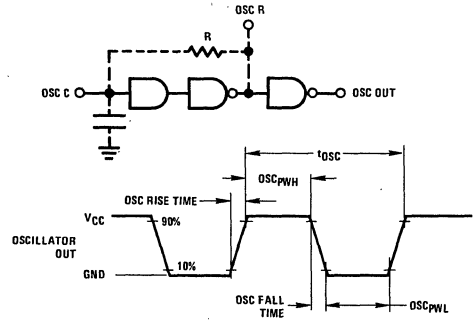


FIGURE 6. DS8693 Motor Drive Latch



$$85\ \text{kHz} \leq 1/t_{OSC} \leq 115\ \text{kHz}$$

$$d = \text{duty cycle} = \frac{OSC_{PWH}}{OSC_{PWH} + OSC_{PWL}}$$

$$40\% \leq d \leq 60\%$$

FIGURE 7. DS8694 Oscillator Diagram

DS8859A, DS8869A Open Collector Hex Latch LED Drivers

General Description

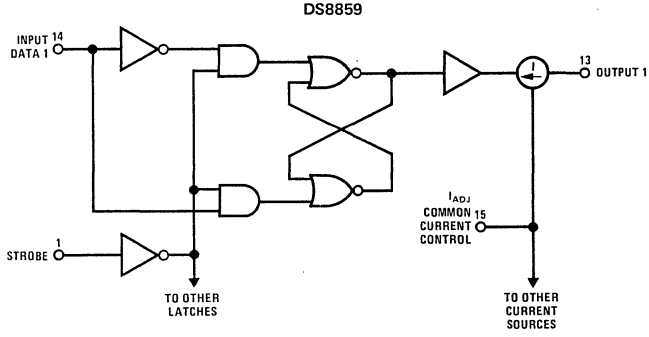
The DS8859A, DS8869A are TTL compatible open collector hex latch LED drivers with programmable current sink outputs. The current sinks are nominally set at 14 mA but may be adjusted by external resistors for any value between 0–32 mA. Each device contains six latches which may be set by input data terminals. An active low strobe common to all six latches enables the data input terminals. The DS8859A current sink outputs are switched on by entering a high level into the latches and the DS8869A current sink outputs are switched on by entering a low level into the latches.

The devices are available in either a molded or cavity package. In order not to damage the devices there is a limit placed on the power dissipation allowable for each package type. This information is shown in the graph included in this data sheet.

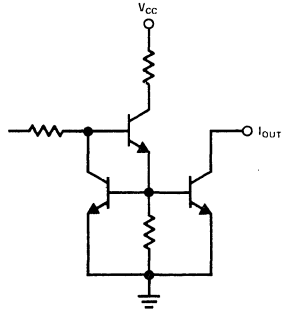
Features

- Built-in latch
- Programmable output current
- TTL compatible inputs
- 32 mA output sink

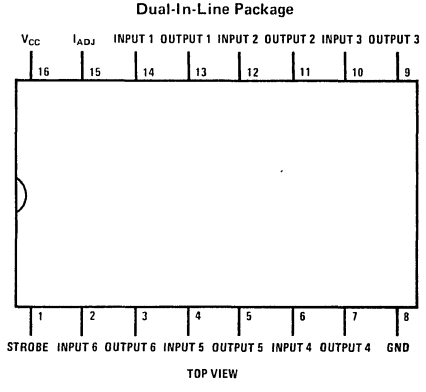
Logic Diagram



Output Circuit



Connection Diagram



Truth Table

COMMON STROBE	INPUT DATA	DS8859 OUTPUT (t + 1)	DS8869 OUTPUT (t + 1)
0	0	OFF	ON
0	1	ON	OFF
1	X	OUTPUT (t)	OUTPUT (t)

Order Number DS8859AJ, DS8869AJ, DS8859AN or DS8869AN
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.55 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V				40	μA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.0	−1.6	mA
V_{CD}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA			−1.1	−1.5	V
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{IL} = 0.8V, V_{OH} = 5.5V, V_{IH} = 2.0V				250	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OL} = 16 mA, V_{IH} = 2V, V_{IADJ} = V_{CC} MIN				0.4	V
I_{CC}	Supply Current	V_{CC} = Max, Current Sources "OFF," (See Truth Table), (Note 4)				50	mA
I_{SINK}	Output Current	V_{CC} = 5.0V, V_{OUT} = 2.0V, T_A = 25°C, (Note 4)	V_{IADJ} = 5V	32			mA
			I_{ADJ} = Open	9	14	26	mA

Switching Characteristics T_A = 25°C, V_{CC} = 5V

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	C_{OUT} = 15 pF, R_L = 390Ω, (Note 5)	Data to Output			36	ns
			Strobe to Output			50	ns
t_{pd1}	Propagation Delay to a Logical "1"		Data to Output			150	ns
			Strobe to Output			150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

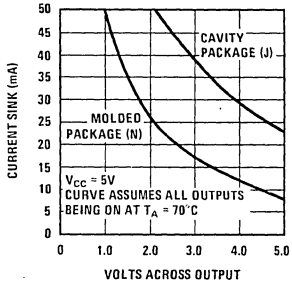
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: See graphs for changes in I_{SINK} versus changes in temperature and V_{CC}.

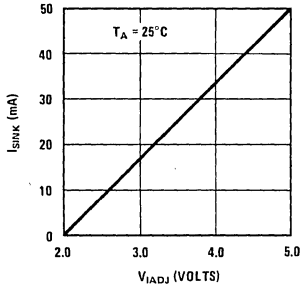
Note 5: C_{OUT} includes device output capacitance of approximately 8.5 pF and wiring capacitance.

Typical Performance Characteristics

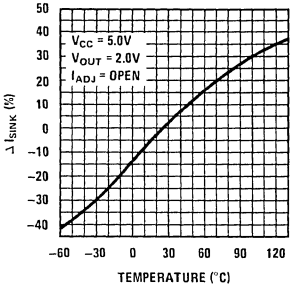
Max Power Dissipation Curves



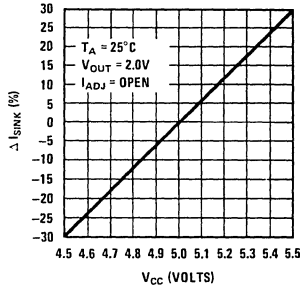
I_{SINK} vs V_{IADJ} (See Figure 1)



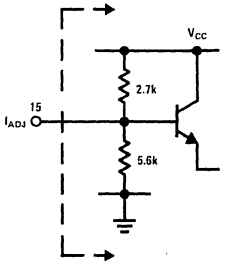
Δ I_{SINK} vs Temperature



Δ I_{SINK}/V_{CC}



I_{SINK} Adjustment Circuit



I_{ADJ} may be programmed by a voltage source or by resistors.

FIGURE 1.

National Semiconductor

DS8861 MOS-to-LED 5-Segment Driver
DS8863 MOS-to-LED 8-Digit Driver
DS8963 MOS-to-LED 8-Digit Driver

General Description

The DS8861, DS8863 and DS8963 are designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays.

The DS8861 is a 5-segment driver capable of sinking or sourcing up to 50 mA from each driver.

The DS8863 is an 8-digit driver. Each driver is capable of sinking up to 500 mA.

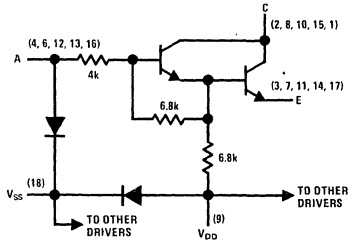
The DS8963 is identical to the DS8863 except it is intended for operation at up to 18V.

Features

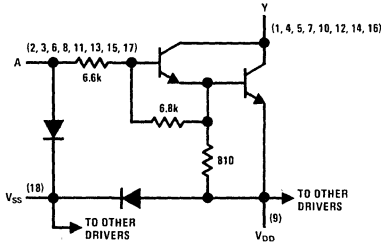
- 50 mA source or sink capability per driver, DS8861
- 500 mA sink capability per driver, DS8863, DS8963
- MOS compatibility (low input current)
- Low standby power
- High gain Darlington circuits

Schematic and Connection Diagrams

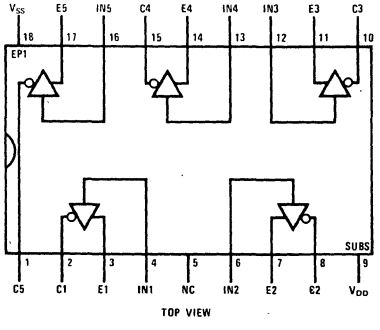
DS8861



DS8863/DS8963

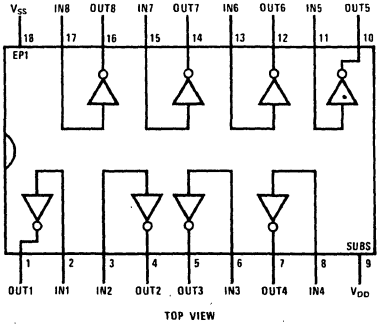


Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

Order Numbers DS8861N, DS8863N or DS8963N
See NS Package N18A

Absolute Maximum Ratings

	DS8861	DS8863	DS8963
Input Voltage Range (Note 1)	−5V to V_{SS}	−5V to V_{SS}	−5V to V_{SS}
Collector (Output) Voltage (Note 2)	10V	10V	18V
Collector (Output)-to-Input Voltage	10V	10V	18V
Emitter-to-Ground Voltage ($V_I \geq 5V$)	10V		
Emitter-to-Input Voltage	5V		
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	10V	18V
Collector (Output) Current			
Each Collector (Output)	50 mA	500 mA	500 mA
All Collectors (Output)	200 mA	600 mA	600 mA
Continuous Total Dissipation	800 mW	800 mW	800 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Maximum Power Dissipation at 25°C			
Molded Package	1476 mW*	1563 mW†	1563 mW†
Lead Temperature (Soldering, 10 sec)	300°C	300°C	300°C

*Derate molded package 11.81 mW/°C above 25°C.
†Derate molded package 12.5 mW/°C above 25°C.

Electrical Characteristics DS8861 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{CEON}	"ON" State Collector Emitter Voltage	Input = 8V through 1 kΩ, V_E = 5V, I_C = 50 mA	T_A = 25°C		0.9	1.2	V
						1.5	V
I_{COFF}	"OFF" State Collector Current	V_C = 10V, V_E = 0	I_{IN} = 40μA			100	μA
			V_{IN} = 0.7V			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, V_E = 0, I_C = 20 mA			2.2	3.3	mA
I_E	Emitter Reverse Current	V_{IN} = 0, V_E = 5V, I_C = 0				100	μA
I_{SS}	Current Into V_{SS} Terminal					1	mA

DS8863/DS8963 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage	V_{IN} = 7V, I_{OUT} = 500 mA	T_A = 25°C			1.5	V
						1.6	V
I_{OH}	High Level Output Current	V_{OH} = 10V*	I_{IN} = 40μA			250	μA
			V_{IN} = 0.5V			250	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA				2	mA
I_{SS}	Current Into V_{SS} Terminal					1	mA

*18V for the DS8963

Switching Characteristics DS8861 (V_{SS} = 7.5V, T_A = 25°C)

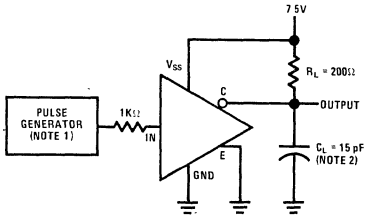
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output (Collector)	V_{IH} = 4.5V, V_E = 0		100		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output (Collector)	R_L = 200Ω, C_L = 15 pF		20		ns

DS8863/DS8963 (V_{SS} = 7.5V, T_A = 25°C)

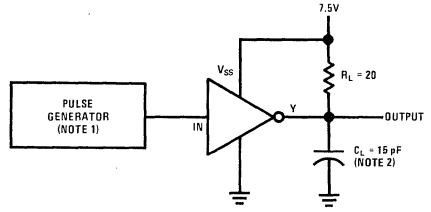
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 8V, R_L = 20Ω,		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF		30		ns

Note 1: The input is the only device terminal which may be negative with respect to ground.
Note 2: Voltage values are with respect to network ground terminal unless otherwise noted.

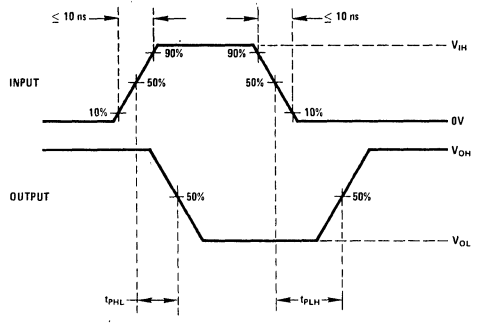
AC Test Circuits and Waveforms



DS8861



DS8863



NOTE 1: THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: Z_{OUT} = 50Ω, PRR = 100 KHz, t_W = 1μs.

NOTE 2: C_L INCLUDES PROBE AND JIG CAPACITANCE.

National Semiconductor

Display Controllers/Drivers

DS8867 8-Segment Constant Current Driver

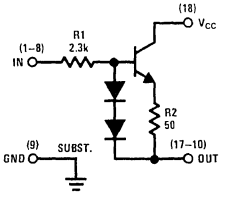
General Description

The DS8867 is an 8-segment driver designed to be driven from MOS circuits operating at 8V ±10% minimum V_{SS} supply and will supply 14 mA typically to an LED display. The output current is insensitive to V_{CC} variations.

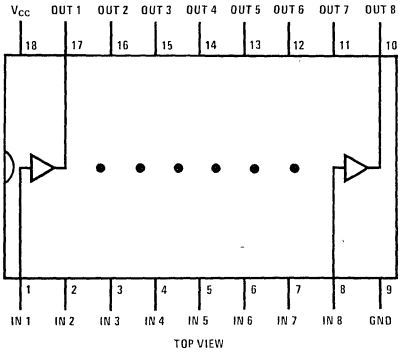
Features

- Internal current control—no external resistors
- 100% efficient, no standby power
- Operates in three and four cell battery systems
- Inputs and outputs grouped for easy PC layout

Schematic and Connection Diagrams



Dual-In-Line Package

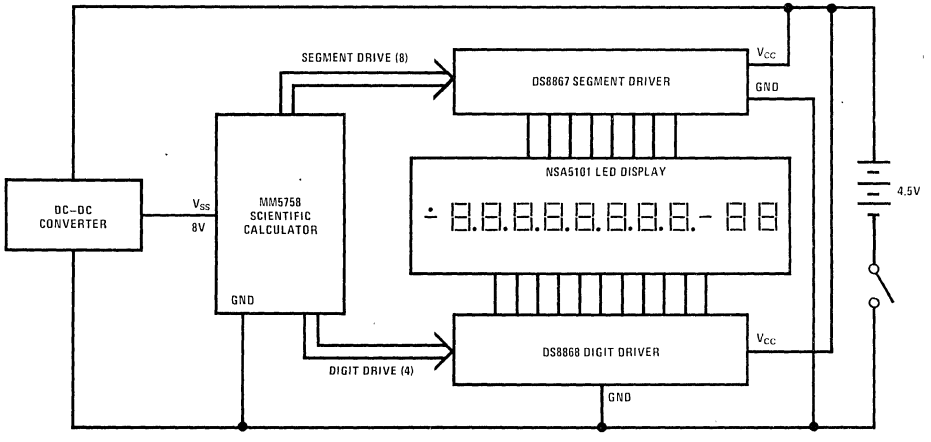


TOP VIEW

Order Number DS8867N
See NS Package N18A

Typical Application

Typical 3 Cell Scientific Calculator Circuit



Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1345 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 10.76 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	3.3	6.0	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min, V_{OH} = 2.3V, I_{IH} = 500μA			4.9	5.4	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{OL} = 1.8V, V_{IL} = 2.0V			0.1	10	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{OH} = 2.3V, I_{IH} = 500μA		−8	−14	−18	mA
I_{OL}	Logical "0" Output Current	V_{CC} = Max, V_{OL} = 1.0V, V_{IL} = 1.3V			−0.5	−10	μA
$I_{CC\ OFF}$	Supply Current	V_{CC} = Max	All V_{OL} = 1.0V, V_{IL} = 1.3V, (Standby)		4	50	μA
$I_{CC\ ON}$			All V_{OH} = 2.3V, V_{IH} = 7.8V		112	150	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C.

DS8870 Hex LED Digit Driver

General Description

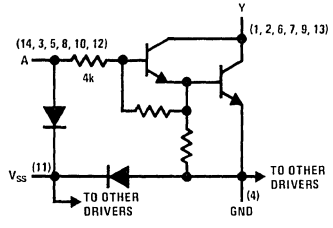
The DS8870 is an interface circuit designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

Features

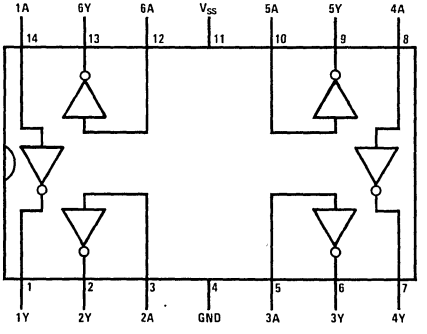
- Sink capability per driver—350 mA
- MOS compatibility (low input current)
- Low standby power
- High-gain Darlington circuits

Schematic and Connection Diagrams

DS8870 (Each Driver)



Dual-In-Line Package



Order Number DS8870J or DS8870N
See NS Package J14A or N14A

Absolute Maximum Ratings (Note 1)

Input Voltage Range (Note 4)	−5V to V_{SS}
Collector Output Voltage	10V
Collector Output to Input Voltage	10V
Voltage at V_{SS} Terminal with Respect to Any Other Device Terminal	10V
Collector Output Current	
Each Collector Output	350 mA
All Collector Outputs	600 mA
Continuous Total Dissipation	800 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1308 mW
Molded Package	1207 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 8.72 mW/°C above 25°C; derate molded package 9.66 mW/°C above 25°C.

Electrical Characteristics (V_{SS} = 10V) (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, I_{OUT} = 350 mA, T_A = 25°C		1.2	1.4	V
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, I_{OUT} = 350 mA			1.6	V
I_{OH}	High Level Output Current	V_{OH} = 10V, I_{IN} = 40μA			200	μA
I_{OH}	High Level Output Current	V_{OH} = 10V, V_{IN} = 0.5V			200	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA		2.2	3.3	mA
I_{SS}	Current Into V_{SS} Terminal				1	mA

Switching Characteristics (V_{SS} = 7.5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 7.5V, R_L = 39Ω, C_L = 15 pF		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	V_{IH} = 7.5V, R_L = 39Ω, C_L = 15 pF		30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The input is the only device terminal which may be negative with respect to ground.

National Semiconductor

DS8871, DS8872, DS8873 Saturating LED Cathode Drivers

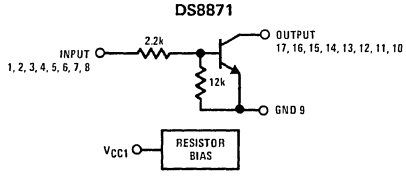
General Description

The DS8871, DS8872, and DS8873 are bipolar integrated circuits designed to interface between MOS calculator circuits and common cathode LED displays operating in the multiplexed mode with a digit current of up to 40 mA. The DS8871 is an 8-digit driver; the DS8872 is a 9-digit driver; and the DS8873 is a 9-digit driver with a built-in battery condition indicator that turns on the digit 9 decimal point when the battery voltage drops to 6.5V (typical). In a typical calculator system operating on a 9V battery, the low battery indicator comes on as a warning that the battery should be replaced. But the calculator (MM5737 or equivalent) will still function properly for awhile.

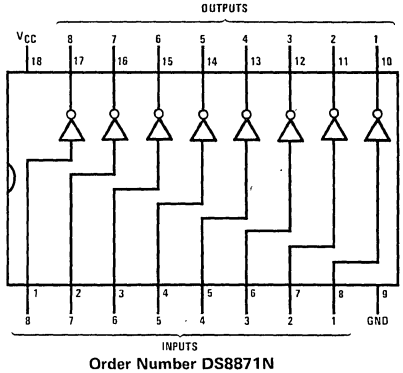
Features

- Single saturating transistor output
- Low battery indicator
- MOS compatible inputs
- Inputs and outputs clustered for easy wiring
- Drivers consume no standby power

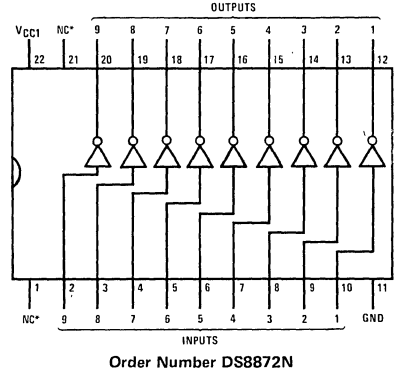
Schematic Diagram



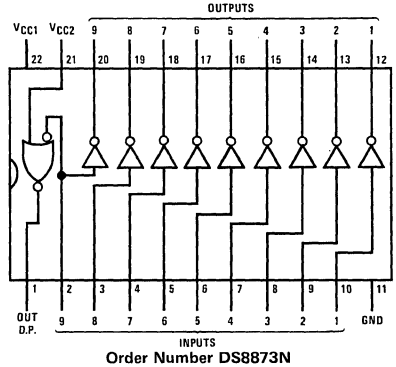
Connection Diagrams (Dual-In-Line Packages, Top Views)



Order Number DS8871N
See NS Package N18A



Order Number DS8872N
See NS Package N22A



Order Number DS8873N
See NS Package N22A

Absolute Maximum Ratings (Note 1)

Supply Voltage	V_{CC1} = 11V
Supply Voltage (Note 4)	V_{CC2} = 11V
Input Voltage	11V
Output Voltage	8V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation at 25°C	
Molded Package (DS8871)*	1563 mW
Molded Package (DS8872, DS8873)†	1771 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 12.5 mW/°C above 25°C.
†Derate molded package 14.17 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC1}	4.0	9.5	V
Supply Voltage, V_{CC2} (Note 4)	4.0	9.5	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V		28	45	μA
I_{IH}	Logical "1" Input Current	V_{IN} = 4.5V		1.7	2.5	mA
V_{OL}	Logical "0" Output Voltage	V_{IN} = 3.2V, I_{OL} = 40 mA		0.35	0.5	V
I_{OL}	Logical "0" Output Current	V_{IN} = 3.2V, V_{OL} = 0.5V			40	mA
I_{CEX}	Output Leakage Current	V_{OH} = 6V, I_{IN} = 25 μA			40	μA
$I_{DP(ON)}$	Decimal Point Output Current	V_{CC2} = 6.25V, V_{DP} = 2.5V, V_{IN9} = 3.2V, (Note 4)	−5.0	−7.0		mA
$I_{DP(OFF)}$	Decimal Point Output Current	V_{CC2} = 7V, V_{IN9} = 3.2V, V_{DP} = 1V, (Note 4)		−1	−100	μA
I_{CC1}	Supply Current, V_{CC1}	V_{CC1} = 6.5V, V_{IN} = 0V		1	100	μA
I_{CC2}	Supply Current, V_{CC2}	V_{CC2} = 9.5V, V_{IN9} = 4.5V, (Note 4)		0.9	1.2	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies to DS8873 only.

Typical Applications

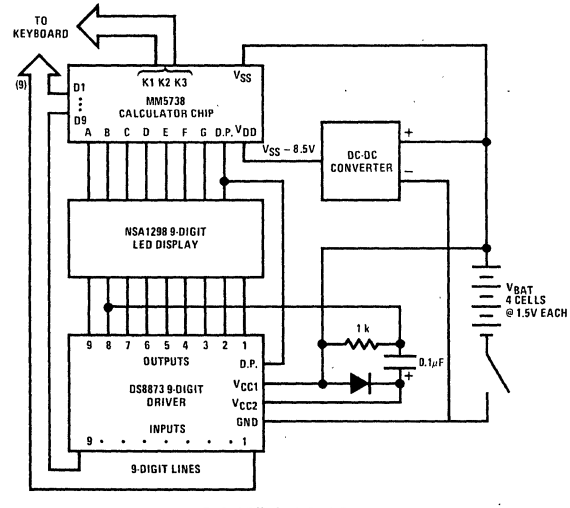


FIGURE 1. 4-Cell System

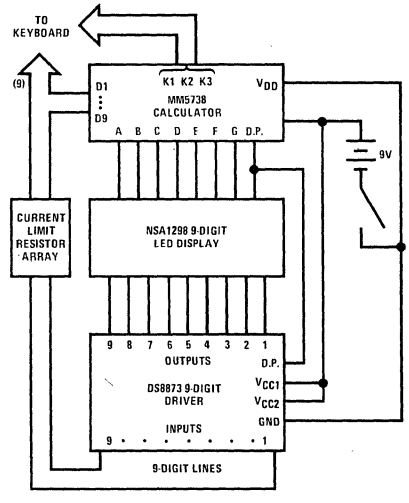


FIGURE 2. 9V System

DS8874 9-Digit Shift Input LED Driver

General Description

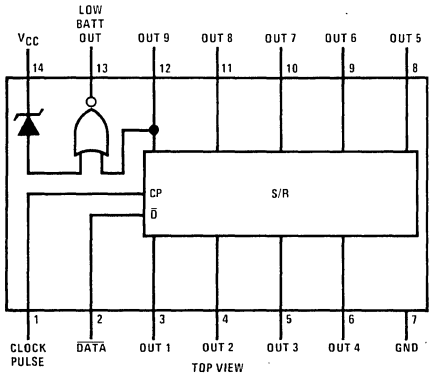
The DS8874 is a 9-digit LED driver which incorporates a shift register input decoding circuit and a low battery indicator. Outputs will sink 110 mA at less than 0.5V drop when sequentially selected. When the V_{CC} supply falls below 6.5V typical, segment current will be furnished at digit 9 time to indicate a low battery condition. Pin 13 is generally connected to the decimal point segment on the display so that when a low battery condition exists, the left-most decimal point lights up. The digit driver is intended to be used with the MM5784N 5-function, 9-digit accumulating memory calculator circuit, or any other circuit which supplies the 9-digit information in a similar serial format.

Features

- 110 mA digit sink
- Low battery indicator
- Minimum number of connections
- MOS compatible inputs

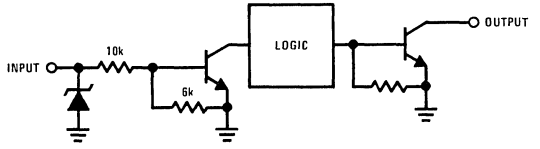
Connection Diagram

Dual-In-Line Package



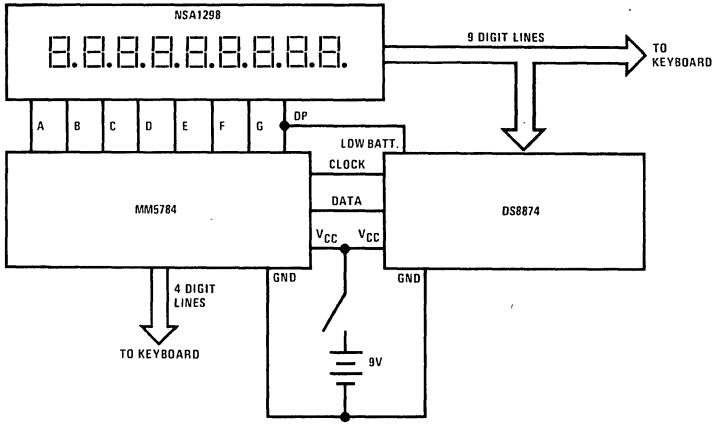
Order Number DS8874N
See NS Package N14A

Equivalent Schematic



Typical Application

Typical Application of the DS8874 Digit Driver with the MM5784 5-Function Calculator Circuit, NSA1298 9-Digit LED Display and a 9V Battery



Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	3V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1280 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 10.24 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	6.0	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

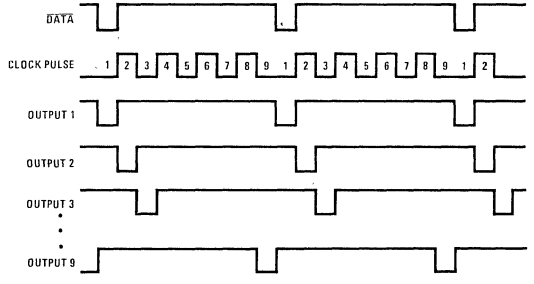
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 3V		0.25	0.4	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.8V		0.05	0.1	mA
V_{CCL}	Decimal Point "ON"	V_{dp} = 2.3V, I_{dp} = −4 mA, O9 = V_{OL}			6.0	V
V_{CCH}	Decimal Point "OFF"	V_{dp} = 1V, I_{dp} = −10μA, O9 = V_{OL}	7.0			V
I_{OH}	Logical "1" Output Current	V_{CC} = Max, Output Not Selected			100	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, Output Selected, I_{O1} = 80 mA		0.45	1	V
		V_{CC} = Max, Output Selected, I_{O1} = 110 mA		0.6	1.5	V
I_{CC}	Supply Current	V_{CC} = Max, One Output Selected		13	19	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Timing Diagram (Upper Level More Positive)



DS8877 6-Digit LED Driver

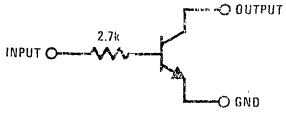
General Description

The DS8877 is a 6-digit LED driver designed as a pin-for-pin replacement for the DS75492 in applications where digit current is in the 5 to 50 mA range. Since the outputs saturate to less than 0.6V, the DS8877 will work on lower battery voltages than most digit drivers. The DS8877 draws *no* standby power.

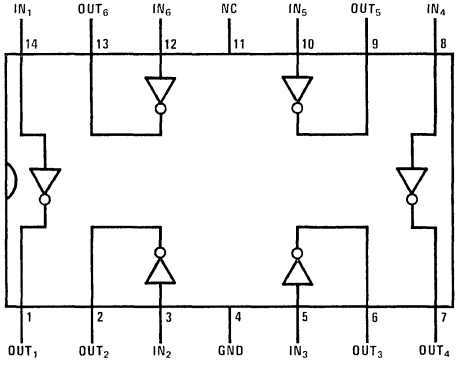
Features

- No standby power
- No supply connection
- Operates in 4.5V,6V or 9V systems
- Pin-for-pin replacement for DS75492 in low current applications

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS8877N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Supply Voltage	None Required
Input Voltage	10V
Output Voltage	10V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1106 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 8.85 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

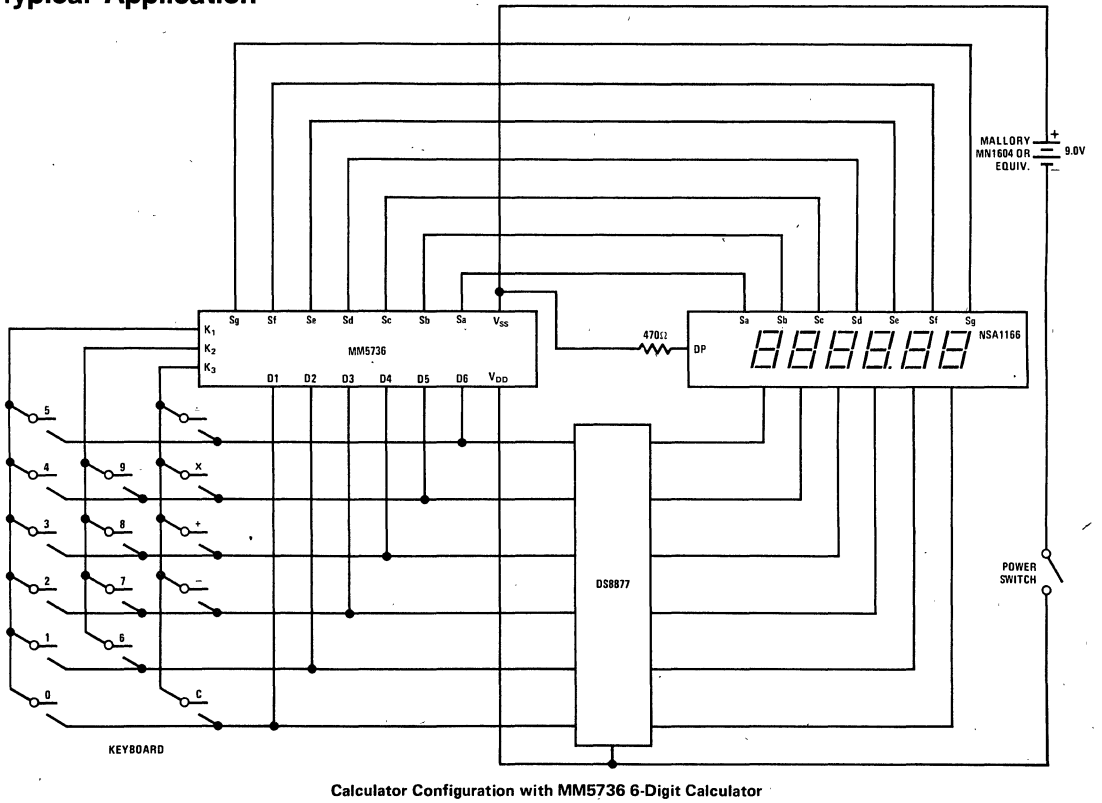
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage		5.0			V
I_{IH}	Logical "1" Input Current	V_{IH} = 5.0V			1.2	mA
V_{IL}	Logical "0" Input Voltage				0.35	V
I_L	Logical "0" Input Current	V_{IL} = 0.35V			20	μA
I_{CEX}	Logical "1" Output Current	V_C = 8.0V, V_{IN} = 0.35V			100	μA
V_{OL}	Logical "0" Output Voltage	I_{OL} = 35 mA, V_{IN} = 5.0V			0.5	V
I_{OL}	Logical "0" Output Current	V_{OL} = 0.5V, V_{IN} = 5.0V	35	50		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Application



Calculator Configuration with MM5736 6-Digit Calculator

National Semiconductor

Display Controllers/Drivers

DS7880/DS8880 High Voltage 7-Segment Decoder/Driver

General Description

The DS7880/DS8880 is custom designed to decode four lines of BCD and drive a gas-filled seven-segment display tube.

Each output constitutes a switchable, adjustable current sink which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sinks have a voltage compliance from 3V to at least 80V; typically the output current varies 1% for output voltage changes of 3 to 50V. Each bit line of the decoder switches a current sink on or off as prescribed by the input code. Each current sink is ratioed to the b-output current as required for even illumination of all segments.

Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the Program input in accordance with the programming curve. The circuit design provides a one-to-one correlation between program input current and b-segment output current.

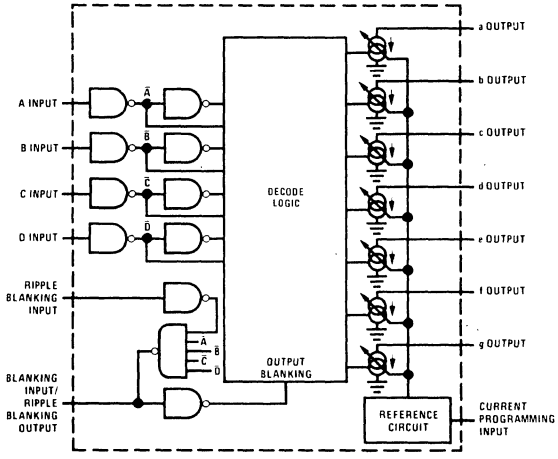
The Blanking Input provides unconditional blanking of any output display, while the Ripple Blanking pins allow simple leading- or trailing-zero blanking.

Features

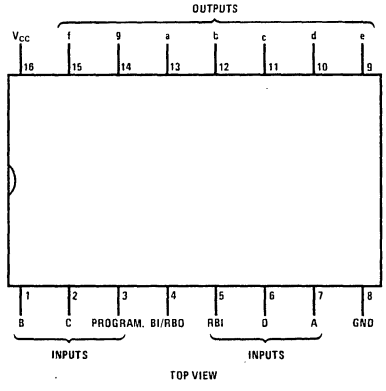
- Current sink outputs
- Adjustable output current – 0.2 to 1.5 mA
- High output breakdown voltage – 110V typ
- Suitable for multiplex operation
- Blanking and Ripple Blanking provisions
- Low fan-in and low power

5

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS7880J or DS8880J
Order Number DS8880N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

V_{CC}	7V
Input Voltage (Except BI)	6V
Input Voltage (BI)	V_{CC}
Segment Output Voltage	80V
Power Dissipation	600 mW
Transient Segment Output Current (Note 4)	50 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 sec)	300°C

*Derate cavity package 10.06 mW/°C above 25°C; derate molded package 11.81 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7880	4.5	5.5	V
DS8880	4.75	5.25	V
Temperature (T_A)			
DS7880	−55	+125	°C
DS8880	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −200μA, RBO		2.4	3.7		V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 8 mA, RBO			0.13	0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, Except BI	V_{IN} = 2.4V		2	15	μA
			V_{IN} = 5.5V		4	400	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V	Except BI		−300	−600	μA
			BI		−1.2	−2.0	mA
I_{CC}	Power Supply Current	V_{CC} = Max, R_P = 2.2k, All Inputs = 0V			27	43	mA
V_{CD}	Input Diode Clamp Voltage	V_{CC} = Max, T_A = 25°C, I_{IN} = −12 mA			−0.9	−1.5	V
$\Delta\lvert I_O \rvert$	SEGMENT OUTPUTS "ON" Current Ratio	All Outputs = 50V, I_{OUT}b = Ref.	Outputs a, f, and g	0.84	0.93	1.02	
			Output c	1.12	1.25	1.38	
			Output d	0.90	1.00	1.10	
			Output e	0.99	1.10	1.21	
$I_{b\ ON}$	Output b "ON" Current	V_{CC} = 5V, V_{OUT}b = 50V, All Other Outputs ≥ 5V, T_A = 25°C	R_P = 18.1k	0.15	0.20	0.25	mA
			R_P = 7.03k	0.45	0.50	0.55	mA
			R_P = 3.40k	0.90	1.00	1.10	mA
			R_P = 2.20k	1.35	1.50	1.65	mA
V_{SAT}	Output Saturation Voltage	V_{CC} = Min, R_P = 1k±5%, I_{OUT}b = 2 mA, (Note 5)			0.8	2.5	V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, BI = 0V, R_P = 2.2k			0.003	3	μA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250μA, BI = 0V, R_P = 2.2k		80	110		V
t_{pd}	Propagation Delays	V_{CC} = 5V, T_A = 25°C					
	BCD Input to Segment Output				0.4	10	μs
	BI to Segment Output				0.4	10	μs
	RBI to Segment Output				0.7	10	μs
	RBI to RBO				0.4	10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7880 and across the 0°C to +70°C range for the DS8880. All typical values are for T_A = 25°C and V_{CC} = 5V.

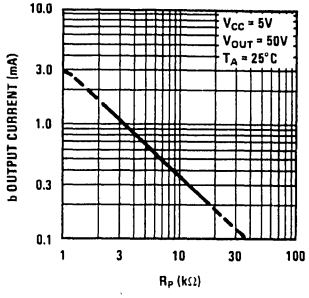
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

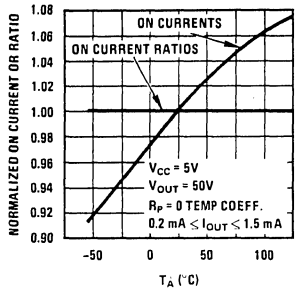
Note 5: For saturation mode the segment output currents are externally limited and ratioed.

Typical Performance Characteristics

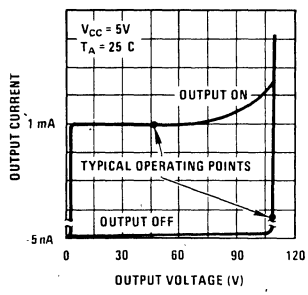
Output Current Programming



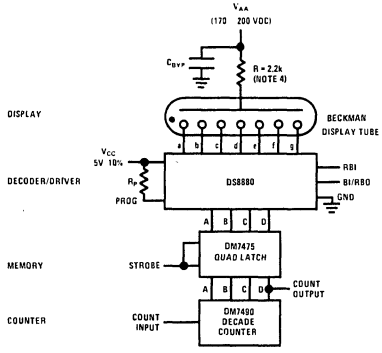
On Currents vs Temperature



Output Characteristic

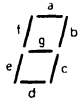


Typical Application



Truth Table

DECIMAL OR FUNCTION	RBI†	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	DISPLAY
0	1	0	0	0	0	1	0	0	0	0	0	0	1	0
1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	X	0	0	1	0	1	0	0	1	0	0	1	0	2
3	X	0	0	1	1	1	0	0	0	0	1	1	0	3
4	X	0	1	0	0	1	1	0	0	1	1	0	0	4
5	X	0	1	0	1	1	0	1	0	0	1	0	0	5
6	X	0	1	1	0	1	0	1	0	0	0	0	0	6
7	X	0	1	1	1	1	0	0	0	1	1	1	1	7
8	X	1	0	0	0	1	0	0	0	0	0	0	0	8
9	X	1	0	0	1	1	0	0	0	0	1	0	0	9
10	X	1	0	1	0	1	0	0	0	1	0	0	0	A
11	X	1	0	1	1	1	1	1	0	0	0	0	0	b
12	X	1	1	0	0	1	0	1	1	0	0	0	1	C
13	X	1	1	0	1	1	1	0	0	0	0	1	0	d
14	X	1	1	1	0	1	0	1	1	0	0	0	0	E
15	X	1	1	1	1	1	0	1	1	1	0	0	0	F
BI*	X	X	X	X	X	0*	1	1	1	1	1	1	1	
RBI	0	0	0	0	0	0	1	1	1	1	1	1	1	



SEGMENT IDENTIFICATION

*BI/RBO used as input only

†X = Don't care

National Semiconductor

Display Controllers/Drivers

DS8881 Vacuum Fluorescent Display Driver

General Description

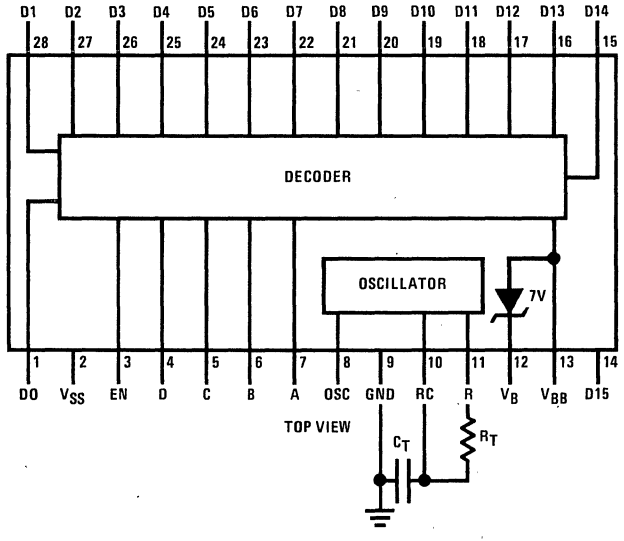
The DS8881 vacuum fluorescent display driver will drive 16-digit grids of a vacuum fluorescent display. The decode inputs select one of the sixteen outputs to be pulled high. The device contains an oscillator for supplying clock signals to the MOS circuit, the filament bias zener and 50 kΩ pull-down resistors for each grid. Outputs will source up to 7 mA. The DS8881 is designed for 9V operation. If the enable input is pulled low, all outputs are disabled.

Features

- Oscillator frequency accuracy and stability allows maximum system speed
- Interdigit blanking with the enable input provides ghost-free display operation
- 50 kΩ pull-down resistors for each grid
- 7V filament bias zener

Connection Diagram

Dual-In-Line Package



Order Number DS8881N
See NS Package N28A

Truth Table

All outputs not shown high are off (low)

INPUTS					DIGIT OUTPUTS															
E_N	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
H	L	L	L	L	H															
H	L	L	L	H		H														
H	L	L	H	L			H													
H	L	L	H	H				H												
H	L	H	L	L					H											
H	L	H	L	H						H										
H	L	H	H	L							H									
H	L	H	H	H								H								
H	H	L	L	L									H							
H	H	L	L	H										H						
H	H	L	H	L											H					
H	H	L	H	H												H				
H	H	H	L	L													H			
H	H	H	L	H														H		
H	H	H	H	L															H	
H	H	H	H	H																H
L	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

Absolute Maximum Ratings (Note 1)

Supply Voltage ($V_{SS} - V_{BB}$)	38V
Input Current	10 mA
Output Current	−20 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	2168 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 17.35 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{SS}	5.0	9.5	V
V_{BB}	Gnd	−26	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS				MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{SS} = Max	Enable	I_{IN} = 260 μA				5.1	V
			A, B, C, D	I_{IN} = 1400 μA				1.5	V
I_{IH}	Logical "1" Input Current	V_{SS} = Max	Enable A, B, C, D					260	μA
V_{IL}	Logical "0" Input Voltage	V_{SS} = Max	Enable					1.0	V
			A, B, C, D					0.3	V
I_{IL}	Logical "0" Input Current	V_{SS} = Max	Enable	V_{IN} = 0V				−1.0	μA
			A, B, C, D	$V_{IN} = V_{IL(MAX)}$		25			μA
V_{OH}	Logical "1" Output Voltage	Digit Output, I_{OH} = −7 mA				V_{SS}−2.5			V
I_{OH}	Logical "1" Output Current	V_{SS} = Max, Osc. Output, V_{RC} = 0.6V, V_{OH} = 10V						50	μA
I_{OS}	Output Short-Circuit Current	V_{SS} = Min, Pin R, V_{RC} = 0.6V, V_R = 0V				−150		−450	μA
R_{OUT}	Output Pull-Down Resistor	V_{SS} = Min, Digit Output				30	50	85	kΩ
V_{OL}	Logical "0" Output Voltage	V_{SS} = Min	Osc. Pin R	V_{RC} = 1.6V	I_{OL} = 6 mA			0.5	V
					I_{OL} = 60 μA			0.2	V
		V_{SS} = Max	Digit Output	V_{ENABLE} = 1V	I_{OL} = 10 μA			V_{BB}+1.4	V
I_{SS}	Supply Current	V_{SS} = 9.5V	I_{OH} = 0	V_{ENABLE} = 5.1V			9.0	12.5	mA
				V_{ENABLE} = 1V			5.0	9.0	mA
I_{BB}	Supply Current	V_{SS} = 9.5V, V_{BB} = −26V	I_B = 0, I_{IN} = 300 μA, (Note 4)	V_{ENABLE} = 1V			−0.8	−1.5	mA
				V_{ENABLE} = 5.1V			−3.0	−5.0	mA
V_B	Filament Bias Voltage	I_B = 10 mA				V_{BB}+6.4	V_{BB}+6.9	V_{BB}+7.4	V

Switching Characteristics T_A = 25°C unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" From Enable Input to Digit Output	R'_L = 4.7 kΩ, C'_L = 50 pF, V_{BB} = −23V, V_{SS} = 8V			1	μs
t_{pd0}	Propagation Delay to a Logical "0" A, B, C, D to Digit Output				1	μs
t_{pd1}	Propagation Delay to a Logical "1" From Enable Input to Digit Output				300	ns
t_{pd1}	Propagation Delay to a Logical "1" From A, B, C, D to Digit Output				500	ns
t_{FALL}	Oscillator Output Transition Time From 1 to 0	V_{SS} = 9.5V, R_L = 6k to V_{SS}, C_L = 25 pF			50	ns
f_{OSC}	Oscillator Frequency	7V < V_{SS} < 9.5V, R_T = 27 kΩ,±2%, R_L = 1.3k, C_T = 100 pF ±5%, C_L = 50 pF	320	360	400	kHz
dc	Oscillator Duty Cycle		46	56	66	%

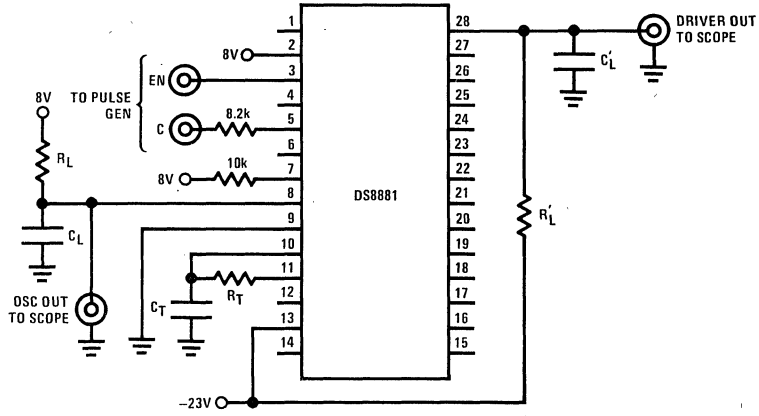
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C for the DS8881. All typicals are given for V_{CC} = 5V and T_A = 25°C.

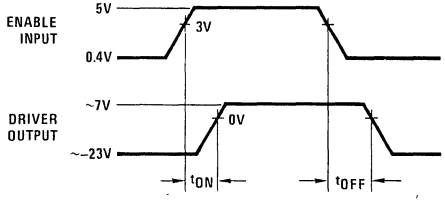
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

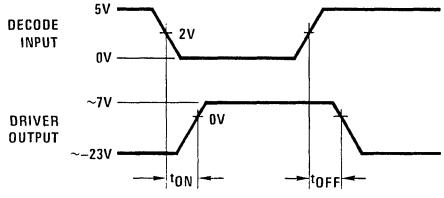
Note 4: Approximately 50% of input current on pins 4, 5, 6, 7 is shunted to V_{BB}. If minimum I_{BB} is desired, then I_{IN} should be minimized by using resistors in series with the inputs.

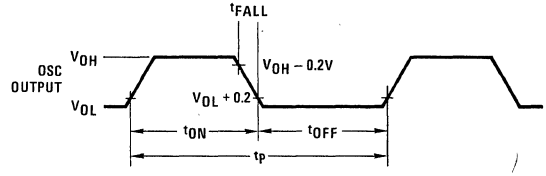
AC Test Circuit



Switching Time Waveforms





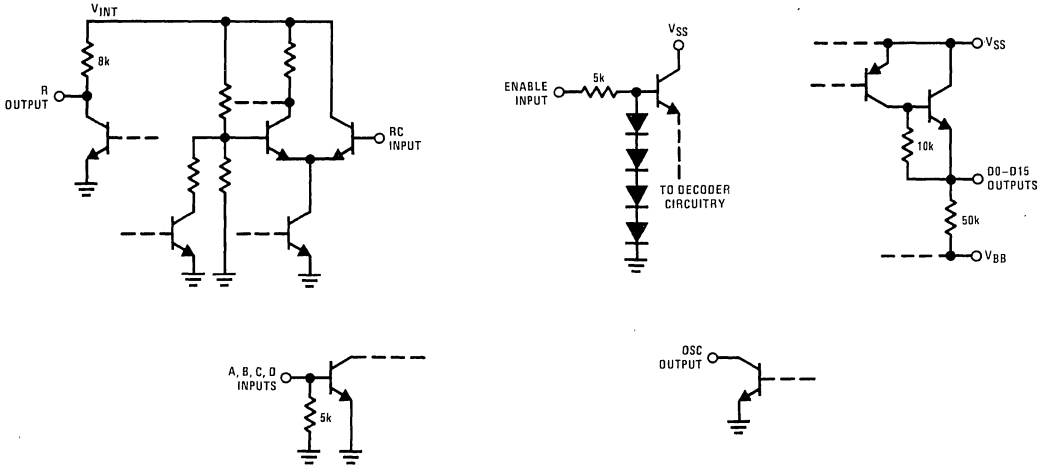


$$\text{Duty Cycle} = \frac{t_{ON}}{t_p}$$

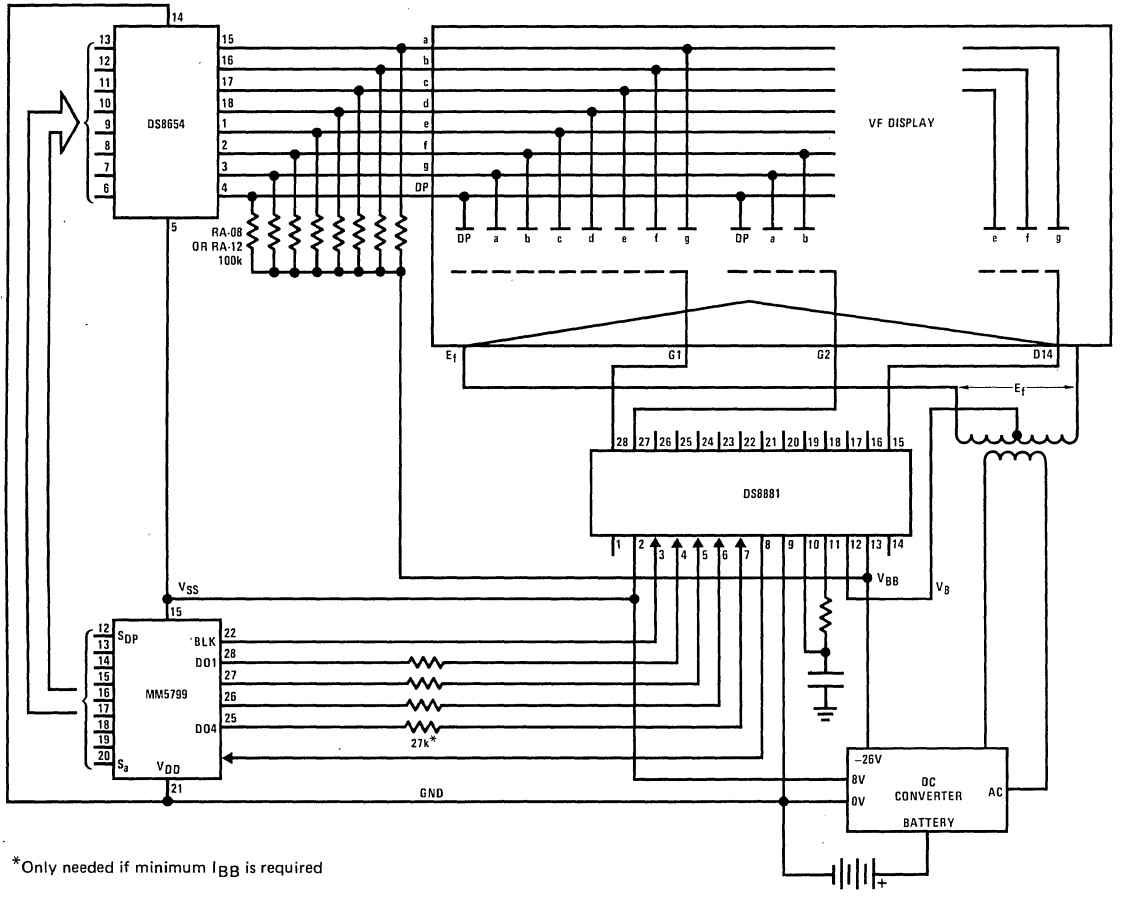
$$\text{Frequency} = \frac{1}{t_p}$$

($t_r = t_f = 10$ ns from 10% to 90% of input)

Input-Output Schematics



Typical Application



*Only needed if minimum I_{BB} is required

National Semiconductor

Display Controllers/Drivers

DS8884A High Voltage Cathode Decoder/Driver

General Description

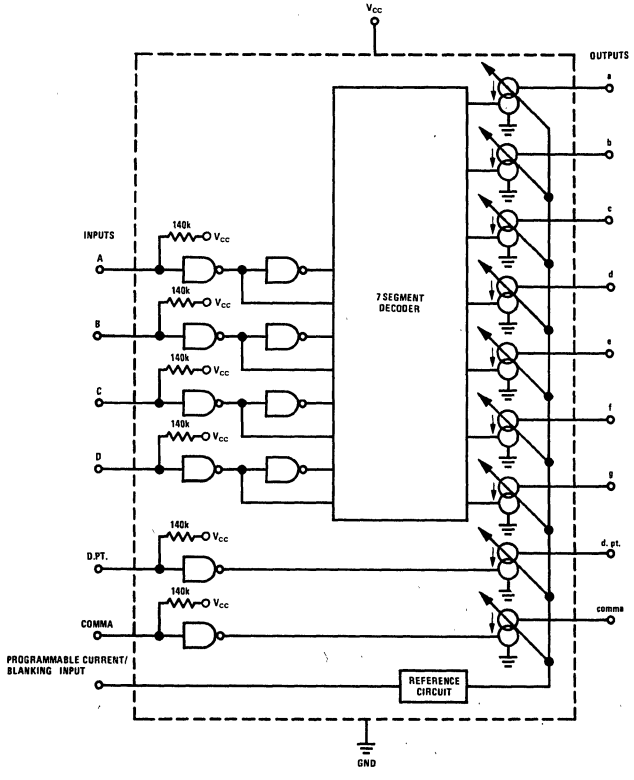
The DS8884A is designed to decode four lines of BCD input and drive seven-segment digits of gas-filled readout displays.

All outputs consist of switchable and programmable current sinks which provide constant current to the tube cathodes, even with high tube anode supply tolerance. Output currents may be varied over the 0.2 to 1.2 mA range for multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the program input in accordance with the programming curve. Unused outputs must be tied to V_{CC}.

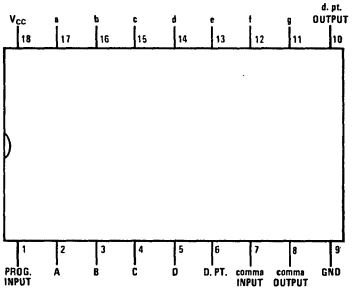
Features

- Usable with AC or DC input coupling
- Current sink outputs
- High output breakdown voltage
- Low input load current
- Intended for multiplex operation.
- Input pullups increase noise immunity
- Comma/d.pt. drive

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS8884AN
See NS Package N18A

Absolute Maximum Ratings (Note 1)

V_{CC}	7V
Input Voltage (Note 4)	V_{CC}
Segment Output Voltage	80V
Power Dissipation	600 mW
Transient Segment Output Current (Note 5)	50 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1714 mW

*Derate molded package 13.71 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = 4.75V		2.0		V
V_{IL}	Logical "0" Input Voltage	V_{CC} = 4.75V			1.0	V
I_{IH}	Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 2.4V			15	μA
I_{IL}	Logical "0" Input Current	V_{CC} = 5.25V, V_{IN} = 0.4V			−250	μA
I_{CC}	Power Supply Current	V_{CC} = 5.25V, R_P = 2.8k, All Inputs = 5V			40	mA
V_{I+}	Positive Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = 1 mA		5.0		V
V_{I-}	Negative Input Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C			−1.5	V
	SEGMENT OUTPUTS					
ΔI_O	"ON" Current Ratio	All Outputs = 50V, I_{OUT} b = Ref., All Outputs		0.9	1.1	
$I_{b\ ON}$	Output b "ON" Current	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C	R_P = 18.1k	0.15	0.25	mA
			R_P = 7.03k	0.45	0.55	mA
			R_P = 3.40k	0.90	1.10	mA
			R_P = 2.80k	1.08	1.32	mA
I_{CEX}	Output Leakage Current	V_{OUT} = 75V			5	μA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250μA		80		V
t_{pd}	Propagation Delay of Any Input to Segment Output	V_{CC} = 5V, T_A = 25°C			10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS8884A. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This limit can be higher for a current limiting voltage source.

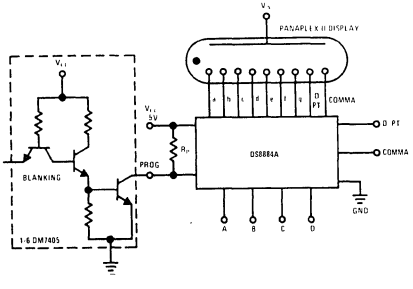
Note 5: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

Truth Table

FUNCTION	D PT	COMMA	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	1	1	0	0	1	1	1	1	1
2	1	1	0	0	1	0	0	0	1	0	0	1	0	2
3	1	1	0	0	1	1	0	0	0	0	1	1	0	3
4	1	1	0	1	0	0	1	0	0	1	1	0	0	4
5	1	1	0	1	0	1	0	1	0	0	1	0	0	5
6	1	1	0	1	1	0	0	1	0	0	0	0	0	6
7	1	1	0	1	1	1	0	0	0	1	1	1	1	7
8	1	1	1	0	0	0	0	0	0	0	0	0	0	8
9	1	1	1	0	0	1	0	0	0	0	1	0	0	9
10	1	1	1	0	1	0	1	1	0	0	0	1	1	
11	1	1	1	0	1	1	1	1	0	0	0	1	0	
12	1	1	1	1	0	0	0	0	1	1	1	0	0	
13	1	1	1	1	0	1	0	1	1	0	0	0	0	
14	1	1	1	1	1	0	1	1	1	1	1	0	0	
15	1	1	1	1	1	1	1	1	1	1	1	1	1	
*D PT	0	1	X	X	X	X	X	X	X	X	X	X	X	
*Comma	0	0	X	X	X	X	X	X	X	X	X	X	X	

*Decimal point and comma can be displayed with or without any numeral.

Typical Application



Typical Performance Characteristics (see DS7880 data sheet)

National Semiconductor

Display Controllers/Drivers

DS8885 MOS to High Voltage Cathode Buffer

General Description

The DS8885 interfaces MOS calculator or counter-latch-decoder-driver circuits directly to 7-segment, high-voltage, gas-filled displays. The six inputs A, B, D, E, F, G are decoded to drive the 7-segment of the tube.

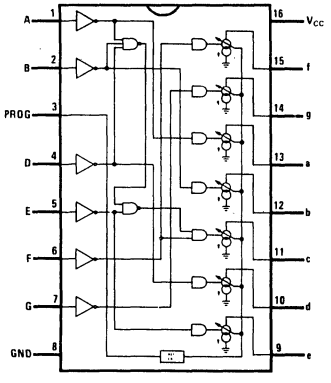
Each output constitutes a switchable, adjustable current source which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sources have a voltage compliance from 3V to at least 80V. Each current source is ratioed to the b-output current as required for even illumination of all segments. Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting a program resistor (R_P) from V_{CC} to the program input.

Features

- Current source outputs
- Adjustable output currents 0.2 to 1.5 mA
- High output breakdown voltage 80V min
- Suitable for multiplex operation
- Low fan-in and low power
- Blanking via program input
- Also drives overrange, polarity, decimal point cathodes

Connection Diagram

Dual-In-Line Package



TOP VIEW

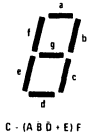
Order Number DS8885J or DS8885N
See NS Package J16A or N16A

Truth Tables

A	B	D	E	F	G	DISPLAY
1	1	1	1	1	0	0
0	1	0	0	0	0	1
1	1	1	1	0	1	2
1	1	1	0	0	1	3
0	1	0	0	1	1	4
1	0	1	0	1	1	5
1	0	1	1	1	1	6
1	1	0	0	0	0	7
1	1	1	1	1	1	8
1	1	1	0	1	1	9
0	0	1	1	1	1	b
1	1	0	0	1	1	c
1	1	0	1	1	1	A
0	1	0	1	1	1	H
0	1	1	1	1	0	U
0	0	0	0	0	1	–
0	0	0	0	0	0	

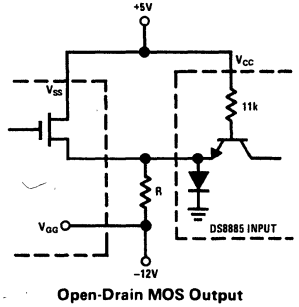
INPUT*	OUTPUT*
0	1 (OFF)
1	0 (ON)

*Positive Logic

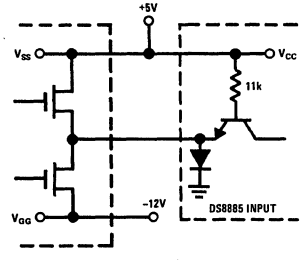


C = (A B D + E) F

Typical Applications



Open-Drain MOS Output



Push-Pull MOS Output

Absolute Maximum Ratings (Note 1)

V_{CC}	7V
Input Voltage	6V
Segment Output Voltage	80V
Power Dissipation	600 mW
Transient Segment Output Current (Note 4)	50 mA
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.06 mW/°C above 25°C; derate molded package 11.81 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min					0.8	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			2	15	μA
			V_{IN} = 5.5V			4	400	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−300	−600	μA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs = 0V, R_P = 2.2k				22	31	mA
V_I	Input Diode Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C				−0.9	−1.5	V
SEGMENT OUTPUTS								
I_O	"ON" Current Ratio	All Outputs = 50V, I_{OUT} b = Ref.	Outputs a, f, and g		0.84	0.93	1.02	
			Output c		1.12	1.25	1.38	
			Output d		0.90	1.00	1.10	
			Output e		0.99	1.10	1.21	
$I_{b\ ON}$	Output b "ON" Current	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C		R_P = 18.1k	0.15	0.20	0.25	mA
				R_P = 7.03k	0.45	0.50	0.55	mA
				R_P = 3.40k	0.90	1.00	1.10	mA
				R_P = 2.20k	1.35	1.50	1.65	mA
V_{SAT}	Output Saturation Voltage	V_{CC} = Min, I_{OUT} b = 2 mA, R_P = 1k ±5%, (Note 5)				0.8	2.5	V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, V_{IN} = 0.8V, R_P = 1k				0.003	3	μA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250μA, V_{IN} = 0.8V			80	110		V
t_{pd}	Propagation Delay of Input to Segment Output	V_{CC} = 5V, T_A = 25°C				0.4	10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8885. All typical values are for T_A = 25°C and V_{CC} = 5V.

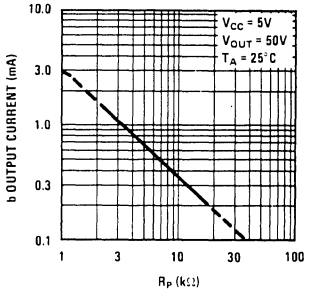
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode drive in multiplex applications.

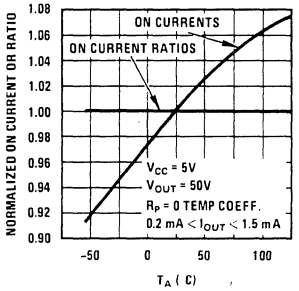
Note 5: For saturation mode the segment output currents are externally limited and ratioed.

Typical Performance Characteristics

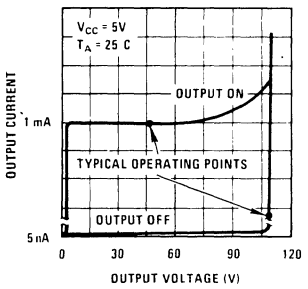
Output Current Programming



On Currents vs Temperature



Output Characteristic



National Semiconductor

DS8887 8-Digit High Voltage Anode Driver (Active-High Inputs)
DS7889/DS8889 8-Segment High Voltage Cathode Driver (Active-High Inputs)
DS7897A/DS8897A 8-Digit High Voltage Anode Driver (Active-Low Inputs)

General Description

The DS8887 and DS7897A/DS8897A are designed to drive the individual anodes of a 7-segment (cathodes) high-voltage gas discharge panel in a time multiplexed fashion.

When driven with appropriate input signals, the driver will switch voltage and impedance levels at the anode. This will allow or prevent ionization of gas around selected cathode in order to form a numeric display. This main application is to interface with MOS outputs (fully-decoded) and the anodes of a gas-discharge panel, since the devices can source up to 16 mA at a low impedance and can tolerate more than 55V in the "OFF" state.

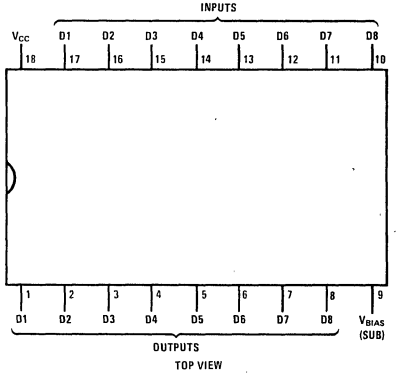
DS7889/DS8889 is capable of driving 8 segments of a high-voltage display tube with a constant output sink current, which can be adjusted by external program resistor, R_P. The program current is half that of output "ON" current. In the "OFF" state the outputs can tolerate more than 80V. The ratio of "ON" output currents is within ±10%. Inputs have negative clamp diodes. Active high input logic. The main application of the device is to interface MOS circuits to high-voltage displays. Unused outputs should have corresponding inputs connected to V_{EE}.

Features

- Versatile circuits for a wide range of display applications
- High breakdown voltages
- Low power dissipation

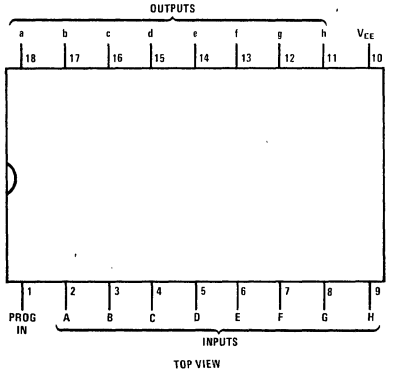
Connection Diagrams (dual-in-line packages)

DS8887, DS7897/DS8897



Order Number DS7897AJ, DS8887J, DS8897AJ or DS8897AN
See NS Package J18A or N18A

DS7889/DS8889



Order Number DS7889J, DS8889J or DS8889N
See NS Package J18A or N18A

Absolute Maximum Ratings (Note 1)

Supply Voltage ($V_{CC} - V_{BIAS}$) (Note 2)
- DS8887, DS7897A, DS8897A: −60V

Input Voltage
- DS8887, DS7897A/DS8897A: −20V
- DS7899/DS8889 (Note 3): 35V

Output Voltage
- DS8887, DS7897A/DS8897A: −65V
- DS7889/DS8889: 85V

Storage Temperature Range: −65°C to +150°C

DS7889/DS8889 Maximum Power Dissipation* at 25°C
- Cavity Package: 1436 mW
- Molded Package: 1563 mW

DS8887, DS7897A/DS8897A Maximum Power Dissipation† at 25°C
- Cavity Package: 1496 mW
- Molded Package: 1714 mW

Lead Temperature (Soldering, 10 seconds): 300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage ($V_{CC} - B_{BIAS}$)			
DS8887, DS7897A/DS8897A	−40	−60	V
Temperature (T_A)			
DS7889, DS7897A	−55	+125	°C
DS8897' DS8889, DS8897A	0	+70	°C

*Derate cavity package 11.49 mW/°C above 25°C; derate molded package 12.5 mW/°C above 25°C.

†Derate cavity package 11.97 mW/°C above 25°C; derate molded package 13.71 mW/°C above 25°C.

Electrical Characteristics (Notes 2, 3 and 4)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DS8887, DS8897A, DS7897A								
V_{IH}	Logical "1" Input Voltage	V_{OUT} = −1.4V, I_{OUT} = −16 mA, DS8887			−2.0			V
V_{IL}	Logical "0" Input Voltage	V_{OUT} = −60V, I_{OUT} = −100μA, DS8887					−5.5	V
I_{IH}	Logical "1" Input Current	V_{OUT} = −1.4V, I_{OUT} = −16 mA, DS8897A, DS7897A			−300			μA
I_{IL}	Logical "0" Input Current	V_{OUT} = −60V, I_{OUT} = −100μA, DS8897A, DS7897A					−10	μA
I_I	Input Current	DS8887	V_{IN} = −1.0V			335	550	μA
			V_{IN} = −6.0V			−0.2	−25	μA
			V_{IN} = −12V		−0.10		−0.65	mA
		DS7897A, DS8897A, V_{IN} = −12V			−0.45		−1.5	mA
$V_{OUT\ OFF}$	Output "OFF" Voltage	I_{OUT} = −100μA, I_{IN} = 0μA			−60	−77		V
$I_{OUT\ OFF}$	Output "OFF" Current	V_{OUT} = −55V, I_{IN} = 0μA				−0.03	−5.0	μA
$V_{OUT\ ON}$	Output "ON" Voltage	I_{OUT} = −16 mA	V_{IN} = −2.0V, DS8887			−1.0	−1.4	V
			I_{IN} = −300μA, DS8897A, DS7897A				−1.4	V
I_{BIAS}	V_{BIAS} Current	I_{OUT} = −16 mA, V_{BIAS} = −60V	V_{IN} = −1.0V, DS8887, (Note 5)			−2.2	−4.0	mA
			I_{IN} = −300μA, DS8897A, DS7897A (One Driver Only)				−1.0	mA
DS7889/DS8889								
I_I	Input Current	V_{IN} = 6.0V			150	250	350	μA
I_{IL}	Logical "0" Input Current	I_{OUT} = 5.0μA, V_{OUT} = 75V					7.0	μA
I_{IH}	Logical "1" Input Current	I_{OUT} = 1.4 mA, I_{IP} = 850μA, V_{OUT} = 50V			80			μA
V_I	Input Clamp Voltage	I_{IN} = −1.0 mA, T_A = 25°C				−0.68	−0.85	V
V_{OH}	Output Breakdown Voltage	I_{OUT} = 100μA, I_{IN} = 0μA			80			V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, −0.1 mA ≤ I_{IN} ≤ 7.0μA				0.02	5.0	μA
I_{PROG}	Prog. Input Voltage	I_{IP} = 150μA			1.8	2.3		V
		I_{IP} = 850μA				4.0	4.5	V
I_{OL}	Logical "0" Output Current	V_{OUT} = 50V, 80μA ≤ I_{IN} ≤ I_{IP}	I_{IP} = 150μA	DS7889	210	300	390	μA
				DS8889	240	300	360	μA
			I_{IP} = 400μA	DS7889	660	800	940	μA
				DS8889	680	800	920	μA
			I_{IP} = 850μA	DS7889	1.45	1.7	1.95	mA
				DS8889	1.53	1.7	1.87	mA
ΔI_O	Output Current Ratio	I_{OUT} b Ref = 1.7 mA, V_{OUT} = 50V			0.9	1.0	1.1	

Switching Characteristics $T_A = 25°C$ unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DS8887						
t_{ON}	Propagation Delay from Input to Output "ON"	(See ac Test Circuit and Switching Time Waveforms)			5.0	μs
t_{RISE}	Propagation Delay from Input to Output "ON"	(See ac Test Circuit and Switching Time Waveforms)			1.0	μs
DS7889/DS8889						
t_{pd0}	Propagation Delay to a Logical "0" from Input to Output	R_P = 6.0k to 6.0V, R_{OUT} = 1.0k to 6.0V		37	100	ns
t_{pd1}	Propagation Delay to a Logical "1" from Input to Output	Input Ramp Rate ≤ 15 ns, Freq = 1.0 MHz dc = 50%, Amplitude = 6.0V		92	200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

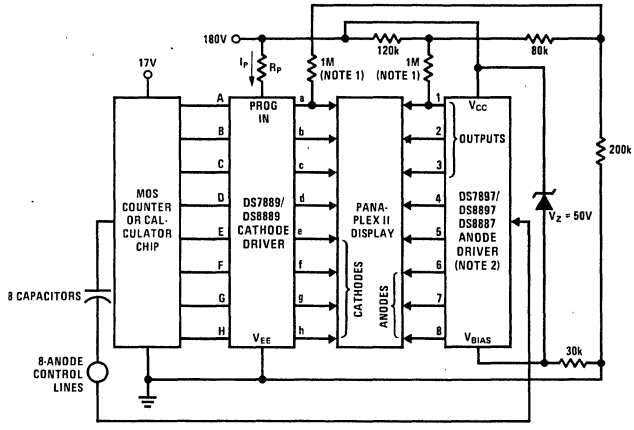
Note 2: All voltage shown for DS8887, DS7897A/DS8897A W.R.T. V_{CC} = 0V. All currents into device pins shown as positive, out of device pins as negative. All values shown as max or min on absolute basis.

Note 3: All voltages for DS7889/DS8889 with respect to V_{EE} = 0V.

Note 4: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7889 and DS7897A, and across the 0°C to +70°C range for the DS8887, DS8889 and DS8897A. All typicals are given for T_A = 25°C.

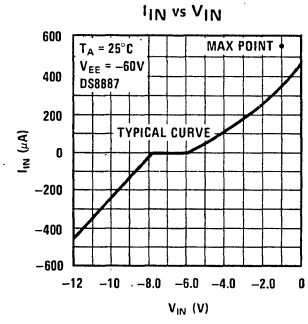
Note 5: Supply currents specified for any one input = −1.0V. All other inputs = −5.5V and selected output having 16 mA load.

Typical Application

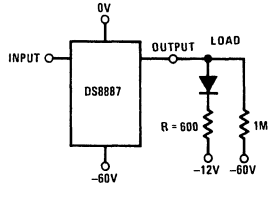


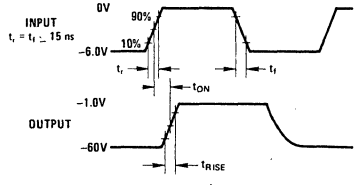
Note 1: All outputs of both cathode and anode driver have loads as shown for output a and digit 1.
Note 2: Use DS8887 for active-high inputs and DS8897 for active-low inputs.

Typical Performance Characteristics



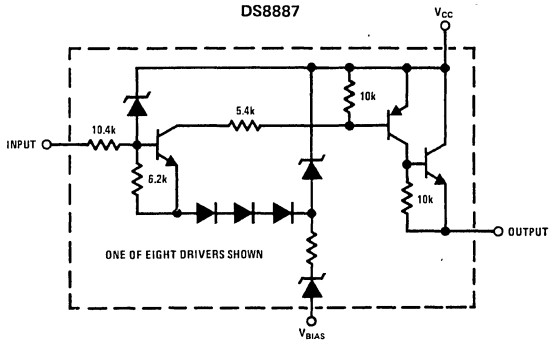
AC Test Circuit and Switching Time Waveforms



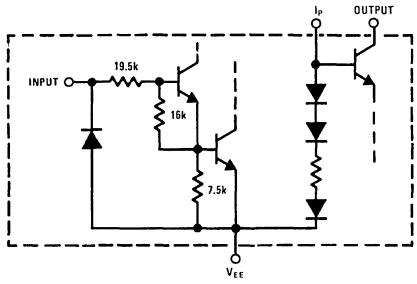


Logic Diagrams

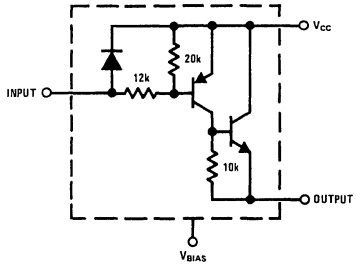
DS8887



DS7889/DS8889



DS7897A/DS8897A



National Semiconductor

DS8891A High Voltage Anode Drivers (Active-Low Inputs)

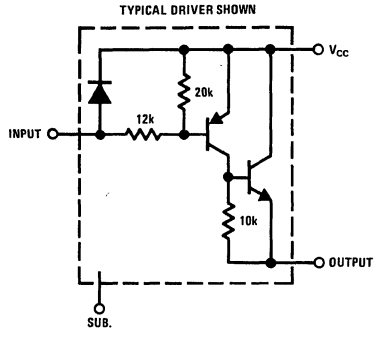
General Description

The DS8891A is a 6 digit anode driver intended for use with seven segment, common anode, high voltage, gas discharge display panels operating in a multiplexed mode. The driver switches voltage and impedance levels at the display's anode allowing or preventing ionization of gas around selected cathodes, forming a numeric display. The device acts as a buffer between MOS outputs (fully decoded) and the anodes of a gas-discharge panel, and it can source up to 16 mA at a low impedance and can withstand more than 55V in the off state.

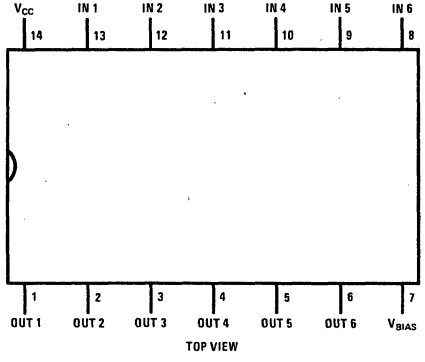
Features

- High breakdown voltage
- Low power dissipation
- Easy interface to clock and calculator circuits

Schematic and Connection Diagrams

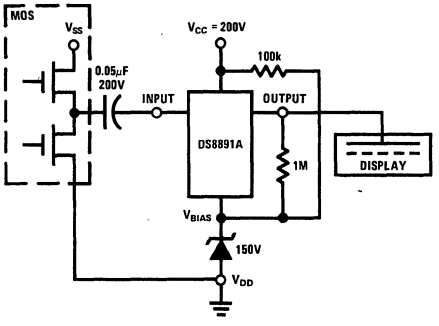


Dual-In-Line Package



Order Number DS8891AJ
or DS8891AN
See NS Package J14A or N14A

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage ($V_{CC} - V_{BIAS}$)	−60V
Input Voltage	−20V
Output Voltage	−65V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1398 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.55 mW/°C above 25°C; derate molded package 11.18 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, $V_{CC} - V_{BIAS}$	−45	−55	V
Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input Current	V_{BIAS} = Min, V_{IN} = −12V	−0.6		−1.5	mA
I_{IH}	Logical "1" Input Current	V_{BIAS} = Min, V_{OL} = −2.0V	−300			μA
I_{IL}	Logical "0" Input Current	V_{BIAS} = Min, V_{OUT} = −60V, I_{OUT} = −100μA			−10	μA
I_{OH}	Logical "1" Output Current	V_{BIAS} = Max, I_{IN} = 0μA, V_{OH} = −55V			−5	μA
V_{OL}	Logical "0" Output Voltage	I_{OL} = −16 mA, I_{IH} = −300μA			−2.0	V
V_{BD}	Output Breakdown Voltage	V_{BIAS} = Max, I_{IN} = 0μA, I_{OUT} = −100μA	−60			V
I_{BIAS}	Supply Current (Substrate)	V_{BIAS} = Max, I_{IH} = −300μA, I_{OL} = −16 mA, (One Driver Only)			−1.0	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8891A.

Note 3. All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to V_{CC} = 0V, unless otherwise noted. All values shown as max or min on absolute value basis.

National Semiconductor

DS8973, DS8975 9-Digit LED Drivers

General Description

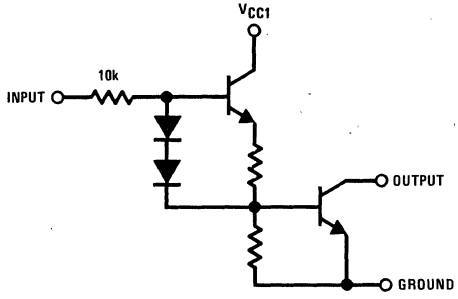
The DS8973 is a 9-digit driver designed to operate from 3-cell battery supplies. Each driver will sink 100 mA to less than 0.7V when driven by only 0.1 mA. Each input is blocked by diodes so that the input can be driven below ground with virtually no current drain. This is especially important in calculator systems employing a dc-to-dc converter on the negative side of the battery. If the converter were on the positive side of the battery, the converter would have to handle all of the display current, as well as the MOS calculator chip current. But if it is on the negative side, it only has to handle the MOS current. The DS8973 is designed for the more efficient operating mode. The DS8975 is identical to the DS8973 but does not specify the low battery indicator.

Features

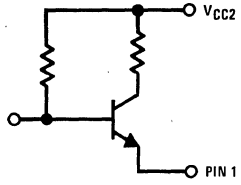
- Nine complete digit drivers
- Built-in low battery indicator
- High current outputs—100 mA
- Straight through pin out for easy board layout

Equivalent Circuit Diagrams

Typical Driver Circuit

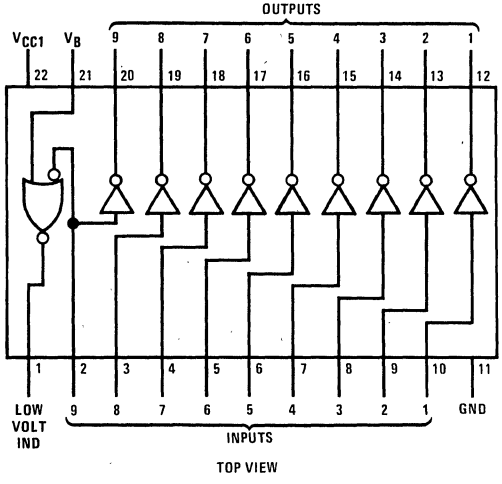


Typical D.P. Out Circuit



Connection Diagrams

Dual-In-Line Package



TOP VIEW

Order Number DS8973N or DS8975N
See NS Package N22A

Absolute Maximum Ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1673 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 13.39 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_B)	3.0	5.5	V
Supply Voltage (V_{CC1})	3.0	9.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Max		3.9			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IH} = 3.9V		0.1		0.3	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max				0.5	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IL} = 0.5V				40	μA
V_{BH}	High Battery Threshold	V_{OT} (Pin 1) = 1V, $I_{OT} \leq -50\mu A$, $T_A = 25°C$, V_{IH} (Pin 2) = 3.9V	DS8973	3.6			V
V_{BL}	Low Battery Threshold	V_{OT} (Pin 1) = 2.1V, $I_{OT} \geq -6$ mA, $T_A = 25°C$, V_{IH} (Pin 2) = 3.9V	DS8973			3.2	V
I_{CEX}	Logical "1" Output Current	V_{CC} = Min, V_{OH} = 9.5V, V_{IL} = 0.5V				50	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 100 mA, V_{IH} = 3.9V				0.7	V
I_{CC1}	Supply Current	V_{CC} = Max, One Input "ON"				6	mA
I_B	Pin 21 (High Battery Supply)	V_{CC} = Max, V_B = Max				1.2	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Applications

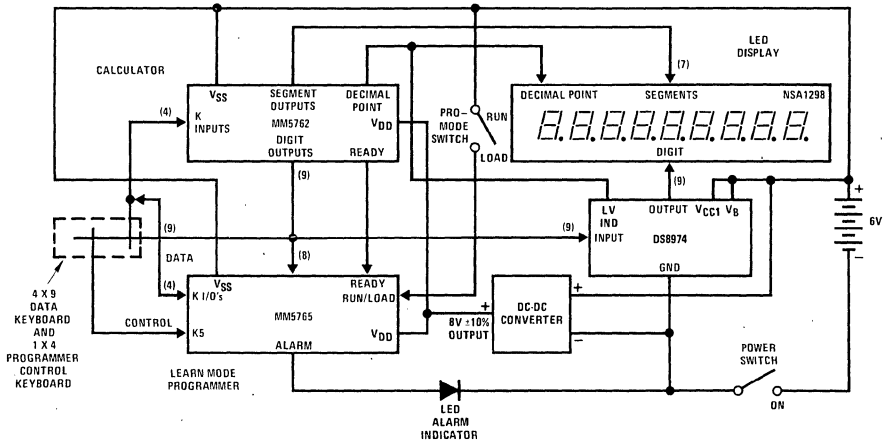


FIGURE 1. 6V Programmable Statistical Calculator

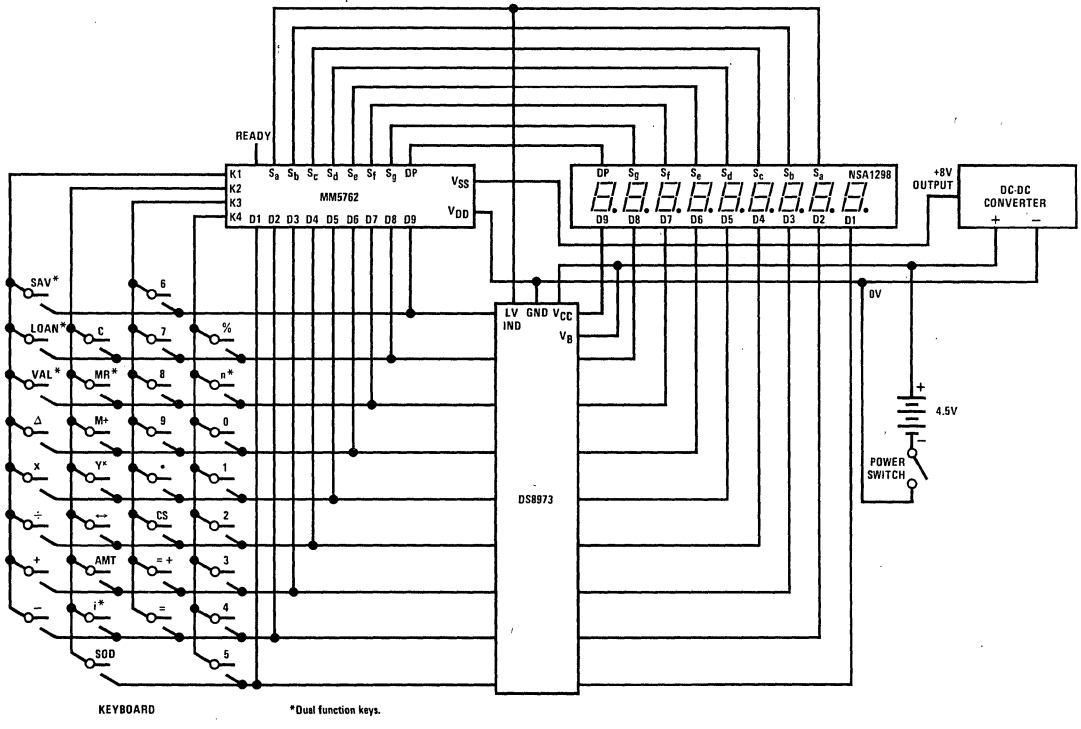


FIGURE 2. Complete Calculator Schematic For 3-Cell System

Driving 7-Segment Gas Discharge Display Tubes with National Semiconductor Circuits

INTRODUCTION

Circuitry for driving high voltage cold cathode gas discharge 7-segment displays, such as Sperry Information Displays* and Burroughs Panaplex II, is greatly simplified by a complete line of monolithic integrated circuits from National Semiconductor. These products also make possible reduced cost of system implementation. They are: DS8880 high voltage cathode decoder/driver; DS8884A high voltage cathode decoder/driver; DS8885 MOS to high voltage cathode buffer; DS8889 low power cathode driver; DS8887 8-digit anode driver; DS8980, DS8981 latch/decoder/cathode drivers.

In addition to satisfying all the displays' parameter requirements, including high output breakdown voltage, these circuits have capability of programming segment current, and providing constant current sinking for the display segments. This feature alleviates the problem of achieving uniformity of brightness with unregulated display anode voltage. The National circuits can drive the displays directly.

Sperry Information Displays* and Burroughs Panaplex II are used principally in calculators and digital instruments. These 7-segment, multi-digit displays form characters by passing controlled currents through the appropriate anode/segment combinations. The cathode in any digit will glow when a voltage greater than the ionization voltage is applied between it (the cathode) and the anode for that digit. In the multiplexed mode of operation, a digit position is selected by driving the anode for that digit with a positive voltage pulse. At the same time, the selected cathode segments are driven with a negative current pulse. This causes the potential between the anode and the selected cathodes to exceed the ionization level, causing a visible glow discharge.

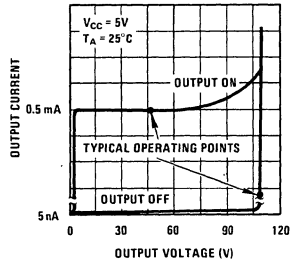
Generally, these displays exhibit the following characteristics: low "on" current per segment—from 200μA (in DC mode) to 1.2 mA (in multiplex mode); high tube anode supply voltage—180V to 200V; and moderate ionization voltage—170V. Once the element fires, operating voltage drops to approximately 150V and light output becomes a direct function of current, which is controlled by current limiting or current regulating cathode circuits. Current regulation therefore is most desirable since brightness will then be constant for large anode voltage changes. Tube anode to cathode "off" voltage is approximately 100V; and maximum "off" cathode leakage is 3μA to 5μA.

*Now called Beckman Displays

Correspondingly, specifications for the cathode driver must be complimentary, approximately as follows: A high "off" output breakdown voltage 80V minimum; typical "on" output voltage of 50V; maximum "on" output current of 1.5 mA per segment; and maximum "off" leakage current of 3μA to 5μA.

To allow operation without anode voltage regulation, the cathode driver must be able to sink a constant current in each output, with the output

(a) Cathode Driver Output Characteristic



(b) On Currents vs Temperature

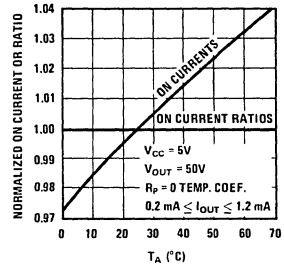


FIGURE 1.

"on" voltage ranging from 5V to 50V (see Figure 1). The following is a brief description of the circuits now offered by National:

DS8880 High Voltage Cathode Decoder/Driver

The DS8880 offers 7-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs; and programmable output current from 0.2 mA to 1.5 mA.

Application

The circuit has a built-in BCD decoder and can interface directly to Sperry and Panaplex II displays, minimizing external components (Figure 2). The inputs can be driven by TTL or MOS outputs directly. It is optimized for use in systems with 5V supplies.

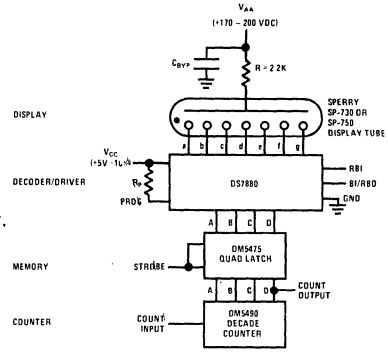


FIGURE 2. DC Operation From TTL

The DS8880 decoder/driver provides for unconditional as well as leading and trailing zero blanking. It utilizes negative input voltage clamp diodes. Typically, output current varies only 1% for output voltage changes of 3V to 50V. Operating power supply voltage is 5V. The device can be used for multiplexed or DC operation.

Available in 16-pin cavity DIP packages, the DS7880 is guaranteed over the full military operating temperature range of −55°C to +125°C; the DS8880 in molded DIP over the industrial range of 0°C to +70°C.

DS8980, DS8981

The DS8980, DS8981 offer 7-segment and decimal point outputs with high output breakdown voltage of 80V minimum, constant current, programmable from 0.1 mA to 4.0 mA and independent of the V_{CC} voltage, latched BCD inputs and decimal point input.

Application

The circuits have similar applications as DS8880. The devices will operate with a power supply range of from 4.75V to 15.0V. The input fall-through latches are enabled by a high logic level at the enable input for the DS8980, and by a low logic level for the DS8981.

Available in 18-pin molded dual-in-line packages, and guaranteed over the commercial range of 0°C to +70°C.

DS8884A High Voltage Cathode Decoder/Driver

The DS8884A offers 9-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs, programmable from 0.2 mA to 1.2 mA. It also offers input negative and positive voltage clamp diodes for DC restoring, and low input load current of −0.25 mA maximum.

Application

DS8884A decodes four lines of BCD input and drives 7-segment digits of gas-filled displays. There are two separate inputs and two additional outputs for direct control of decimal point and comma cathodes. The inputs can be DC coupled to TTL (Figure 3) or MOS outputs (Figure 4), or AC-coupled to TTL or MOS outputs (Figure 5) using only a capacitor. This means the device is useful in applications where level shifting is required. It can be used in multiplexed operation, and is available in an 18-pin molded DIP package.

Other advantages of the DS8884A are: typical output current variation of 1% for output voltage changes of 3V to 50V; and operating power supply

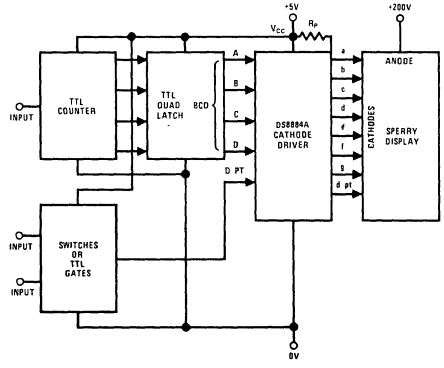


FIGURE 3. Interfacing Directly With TTL Output

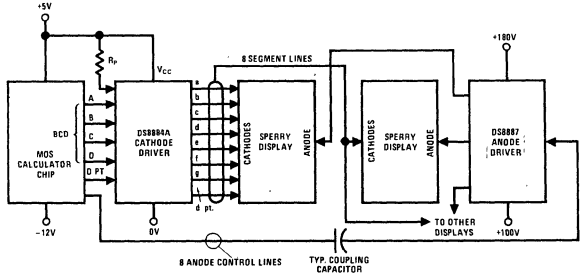
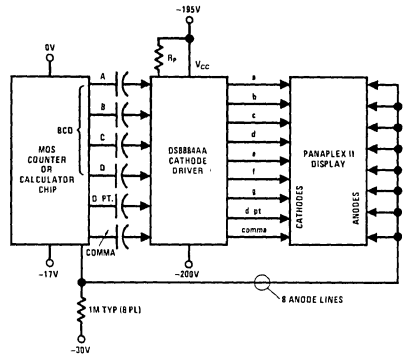


FIGURE 4. BCD Data Interfacing Directly With MOS Output



NOTE: Capacitive coupling between the logic and the segment drivers may be used only when the segment drivers are turned "OFF" during digit-to-digit transitions.

FIGURE 5. Cathode BCD Data AC Coupled From MOS Output

voltage of 5V. Inputs have pull-up resistors to increase noise immunity in AC coupled applications.

The DS8884A is guaranteed over the 0°C to +70°C operating temperature range.

DS8885 MOS to High Voltage Cathode Buffer

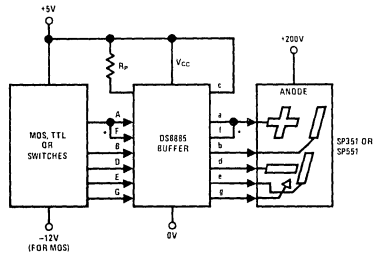
The DS8885 features seven constant current-sink outputs; programmable output current of 0.2 mA to 1.5 mA; high output breakdown voltage of 80V minimum; and capability for blanking through program current input. It operates from a +5V supply.

Application

DS8885 is best suited for interfacing 7-segment fully decoded MOS chips to digit displays. It is also useful for driving polarity, overrange, and decimal point segments.

DS8885 has 6 inputs and 7 outputs. Output c is decoded internally; the other 6 outputs are directly controlled by the 6 corresponding inputs. A typical application of this device is interfacing between an MOS calculator chip with 7-segment decoded outputs (open-drain or push-pull) and Sperry/ Panaplex II displays (Figure 6).

When the DS8885 is used to drive minus and plus (polarity) cathodes, overrange, and decimal points, output c should be tied to V_{CC} so it does not saturate (Figure 7). This leaves 6 inputs and 6 outputs related one-to-one. The inputs can be driven directly from TTL or MOS outputs.



*Output may be paralleled for cathodes requiring more current, providing the corresponding inputs are also paralleled.

FIGURE 7. Polarity, Overrange, Decimal Point Driving

The DS8885 is available in 16-pin molded DIP package, and is guaranteed over the operating temperature range of 0°C to +70°C.

DS8889 Low Power Cathode Driver

The DS8889 requires no power supply since power is derived from program current. It offers extremely low standby power—only 1 mW internally. Features include programmable output currents 0.3 mA to 1.7 mA; 8 constant current-sink outputs; and input negative voltage clamp diodes for DC restoring. Outputs have 80V minimum breakdown voltage.

The device is suitable for multiplexed operation from fully decoded chips and is capable of driving decimal point segments simultaneously with numeric segments.

Application

The DS8889 has 8 inputs and 8 outputs, and interfaces directly between 7-segment decoded MOS outputs and numeric display tubes (Figures 8 and 9). It is optimized for use in systems with a limited number of power supplies.

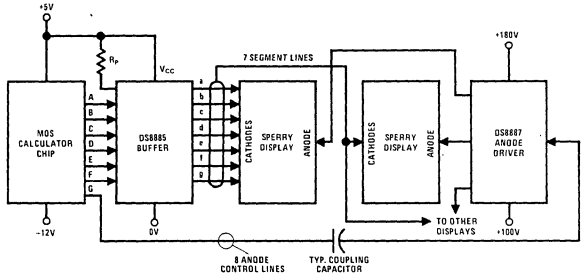


FIGURE 6. Fully Decoded MOS Cathode Outputs

The program input is characterized in terms of input current, therefore any supply (greater than 5V) can provide proper operation by connecting a single resistor to the program pin from the supply.

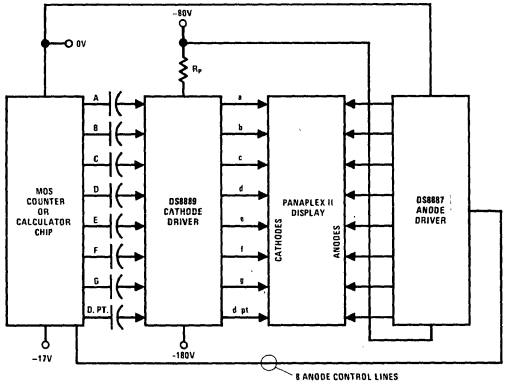
The DS8889, guaranteed for the 0°C to +70°C operating temperature range, is offered in the 18-pin molded DIP.

DS8887 8-Digit Anode Driver

The DS8887 interfaces directly to MOS chips and operates from a −40V to −80V power supply.

The DS8887 can operate virtually any multiplex display system requiring more output performance from the MOS chip than is available (Figures 4, 6, 8 and 9). It has low input current and voltage swing requirements but can drive up to 16 mA, and exhibits -55V minimum output breakdown voltage.

The DS8887 is available in the 18-pin molded DIP package; and is guaranteed over the operating temperature range of 0°C to +70°C.



NOTE: Capacitive coupling between the logic and the segment drivers may be used only when the segment drivers are turned "OFF" during digit-to-digit transitions.

FIGURE 8. Decoded Cathode Data AC Coupled From MOS Output

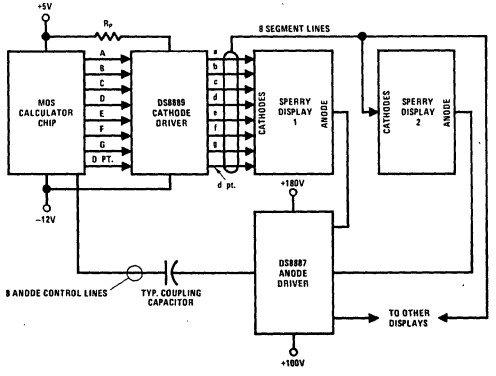


FIGURE 9. Decoded Cathode Data Direct Coupled From MOS Output

Driving 7-Segment LED Displays with National Semiconductor Circuits

National Semiconductor
Application Note 99
Charles Carinalli
May 1974

INTRODUCTION

There are many different information display technologies available today, including liquid crystals, gas-discharge tubes, fluorescent tubes, incandescent lamps, and light emitting diodes (LEDs). Each technology has its own particular drive requirement. This note will focus on 7-segment LED display drive requirements and demonstrate that National Semiconductor has a full line of display drivers that meet the requirements for most any 7-segment LED drive application.

WHY ARE LED DRIVERS NEEDED?

The purpose of 7-segment LED drivers is to act as an interface element between data input and the display. This interface is necessary when either the input data format or circuitry current capabilities do not allow direct connection between input and display. To satisfy these needs, National's 7-segment LED drivers are divided into two basic categories.

1. Internally decoded (BCD to 7-segment)
   DM5446A/DM7446A
   DM5447A/DM7447A
   DM5448/DM7448
   DM7856/DM8856
   DM8857
   DM7858/DM8858
2. Non-decoding, direct drive (MOS to 7-segment)
   DM75491 DM8864
   DM75492 DM8865
   DM8861 DM8866
   DM8863

Thus, National has circuits that will drive 7-segment LEDs from either fully decoded circuits or from non-decoded outputs.

CONFIGURATIONS AND CONSTRUCTION OF 7-SEGMENT LEDs

LEDs are segregated into two groupings with regard to construction, see Figure 1.

Common anode displays are constructed on a common substrate which forms the anode of the diodes, while each of the seven cathodes are bonded out to separate pins. The second type, common cathode, has the cathode fabricated on a common substrate with the anodes bonded out to individual pins. Due to these radically different configurations, drive circuits are usually tailored in their design for one or the other type. Tailoring in this respect means either sinking current (active low) or sourcing current (active high) when referenced to segment drive. In addition, drive requirements are quite variable because of LED light intensity requirements as well as digit size

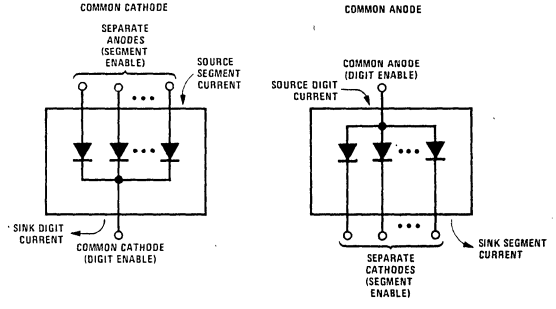


FIGURE 1. 7-Segment LED Construction

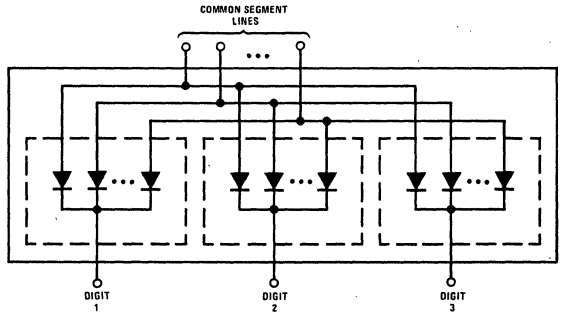


FIGURE 2. Multi-Digit 7-Segment LED

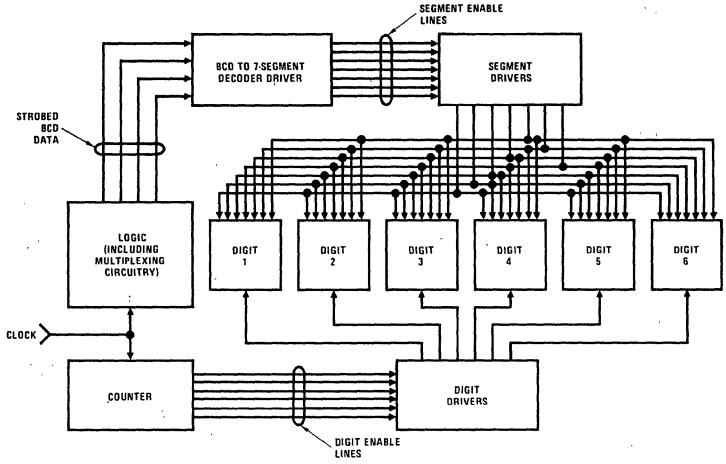


FIGURE 3. A Typical Multiplexing Scheme

and efficiency. Thus the system designer needs a degree of latitude not only with respect to the type of display used but also the drive current available.

7-segment LEDs can be purchased in either single or multi-digit display packages. Single digit displays have individual segment and common pins while multi-digits have paralleled segment pins and separate digit pins equal to the number of digits in the package, see Figure 2.

Multi-digit displays, due to their configuration, must be driven in a multiplex mode of drive, where segment drivers are time shared by all the digits. This is contrasted to the single digit displays which may be driven in either the multiplex or the non-multiplex (direct drive) mode. The nonmultiplex mode uses separate segment drivers for each digit of the display. Multiplex operation has a decided cost saving advantage over nonmultiplex operation especially when the number of digits being driven is large.

MODES OF 7-SEGMENT LED DRIVE

In the multiplex mode of drive the LED digits in a multi-digit format are driven by a single set of segment drivers while each digit is selected by its own digit driver. Figure 3 shows the circuitry needed to implement a typical six digit multiplexed display.

Each digit is selected individually by enabling its digit driver whose control is determined by a counter or equivalent circuitry operating at some clock frequency. Strobed data, by way of the counter and multiplex circuitry, is then displayed on the selected digit by the single set of segment drivers. If the strobe rate is high enough, from about 250 to 1,000 Hz depending on external conditions, the display will appear flicker free to the human eye. The BCD-to-7-segment decoder converts BCD data to the desired 7-segment output format.

In the multiplex mode each digit has a reduced duty cycle and is operated at somewhat higher than average or typical dc operating current levels. The amount of current will be a function of the number of digits, duty cycle, and the type and efficiency of the display used. Since currents are higher than average so also will be the LED brightness due to the nearly linear brightness versus current curve for most LEDs. The human eye will detect the brightness peaks and through a partially integrating and peak detecting action will perceive a higher display brightness at some average current level in the multiplex mode than the same average current in the nonmultiplex (direct drive) mode. The result is that a multiplexed display will operate at a lower total power than the same display operated in the nonmultiplex mode with the same apparent brightness.

In the nonmultiplex mode of 7-segment LED drive each digit has its own set of segment drivers thereby dropping the digit driver select requirement of multiplexed operation. In this case, the common digit pin may be tied to the highest potential if common anode or the lowest if common cathode. It is evident that in a nonmultiplexed display the driver package count would be high since each digit requires its own set of segment and possibly decoder drivers. If a large number of digits are used the segment driver package count would equal the number of digits while in the multiplex mode this count is equal to one. Granted, in the multiplex mode additional control circuitry is required. Consideration of the relative cost of this circuitry in comparison to the segment decoder driver circuitry in the nonmultiplex mode results, in general, in the fact that if the number of digits in the display equals or is more than four, total package count and/or cost is less in the multiplex mode of drive.

In most MOS circuits multiplex operation is ideal since the counter, multiplexer, and BCD to 7-segment decoders or equivalent circuitry can usually be incorporated on the same chip along with calculator, clock or other function. In this case the only external interface components required would be the digit and segment drivers since MOS circuits are generally unable to sink or source the higher current required for most multiplex operations.

In summary, LED driver requirements for multiplex or nonmultiplex drive operation require either segment, digit or BCD to 7-segment drivers. Analysis of the particular system needs with regard to the number of digits and relative circuit costs should be the determining factor for multiplex or nonmultiplex operation. Circuit requirements for multiplex operation will in general require relatively high current capabilities.

NATIONAL'S 7-SEGMENT LED DRIVERS

Table I lists the 7-segment LED drivers available from National. Each circuits application is divided into groupings with respect to common anode or cathode, digit or segment, multiplex or nonmultiplex areas. Additionally, current capabilities are also specified for each product.

From the table it is evident that some of the circuits may be used in dual roles – both multiplex or nonmultiplex; common cathode or anode. In general, what will determine whether one drivers application is multiplex or nonmultiplex is that drivers current capability. The direction of current flow through the driver (source or sink) is the determining factor in dual application with regard to common anode or cathode.

Table II lists the operating temperature range and package types for the 7-segment LED drivers.

In the following sections each circuit is described in greater detail and typical applications are given.

BCD TO 7-SEGMENT DECODER DRIVERS

DM5446A/DM7446A, DM5447A/DM7447A, DM5448/DM7448

This family of BCD to 7-segment decoder drivers was designed for the most general possible display drive applications including display technologies other than LEDs. The difference between the circuits is in their output stage configurations. These differences will be discussed separately later.

The circuits convert the standard 4-bit BCD input to the popular 7-segment output format. All input BCD codes above 9 are decoded into unique patterns that verify operation. The circuits are TTL-DTL compatible and operate off of a single 5.0V supply.

Added features included in all circuits are a ripple blanking input pin as well as a lamp test pin for display turn on. In addition the blanking input/ripple blanking output pin may be used to modulate display intensity.

TABLE I. National 7-Segment LED Drivers

DEVICE NUMBER	COMMON CATHODE		COMMON ANODE		DIGIT DRIVER	SEGMENT DRIVER	INTERNAL DECODING	CURRENT CAPABILITY AND FEATURES
	Multiplex	Nonmultiplex	Multiplex	Nonmultiplex				
DM5446A/DM7446A DM5447A/DM7447A			X	X		X	X	Up to 40 mA Sink, Open Collector High Breakdown (30/15V) TTL Input Compatibility
DM5448/DM7448		X	X*	X*		X	X	1.3 mA Source, Adjustable Externally, TTL Input Compatibility
DM7856/DM8856		X	X*	X*		X	X	6.0 mA Typical Source, TTL Input Compatibility
DM8857	X	X				X	X	50 mA Typical Source, Externally Adjustable, TTL Input Compatibility
DM7858/DM8858	X	X				X	X	Adjustable Source Current 0 to 50 mA, TTL Input Compatibility patibility
DM75491	X	X	X	X	X	X		50 mA Source/Sink, 4 Drivers per Package, MOS Input Compatibility
DM75492	X		X	X	X	X**		250 mA Sink, 6 Drivers per Package, MOS Input Compatibility
DM8861	X	X	X	X	X	X		50 mA Source/Sink, 5 Drivers per Package, MOS Input Compatibility
DM8863	X		X	X	X	X**		500 mA Sink, 8 Drivers per Package, MOS Input Compatibility
DM8864	X		X	X	X	X**		50 mA Sink, 9 Drivers per Package, MOS Input Compatibility
DM8865	X		X	X	X	X**		50 mA Sink, 8 Drivers per Package, MOS Input Compatibility
DM8866	X		X	X	X	X**		50 mA Sink, 7 Drivers per Package, MOS Input Compatibility

*With the use of an external transistor/segment.

**For common anode LED's.

TABLE II. Operating Temperature Range and Package Type

DEVICE NUMBER	OPERATING TEMPERATURE RANGE		NUMBER OF PINS			PACKAGE TYPE		
	0°C to +70°C	−55°C to +125°C	14	16	18	Plastic Molded DIP (N)	Ceramic DIP (J)	Flat Pack (W)
DM5446A, DM5447A		X		X			X	X
DM7446A, DM7447A	X			X		X	X	X
DM5448		X		X			X	X
DM7448	X			X		X	X	X
DM7856		X		X			X	X
DM8856	X			X		X	X	X
DM8857	X			X			X	
DM7858		X		X			X	X
DM8858	X			X		X	X	X
DM75491	X		X			X	X	X
DM75492	X		X			X	X	X
DM8861	X				X	X		
DM8863	X				X	X		
DM8865	X				X	X		
DM8866	X				X	X		
DM8864	X		22			X		

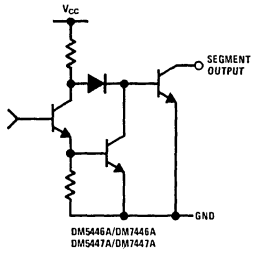


FIGURE 4a. Output Stage

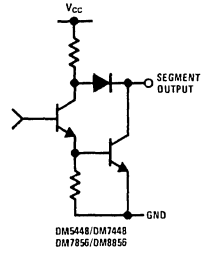
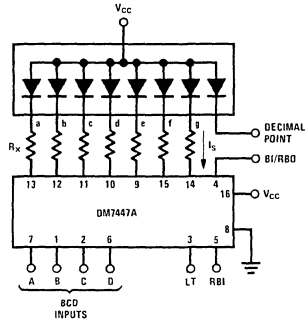


FIGURE 4b. Output Stage



THE FOLLOWING EQUATION MAY BE USED TO DETERMINE THE APPROPRIATE VALUE OF R_X (SEGMENT CURRENT LIMIT RESISTOR) FOR SOME LED CURRENT/SEGMENT I_S (mA).

$$R_X = \frac{V_{CC} - 0.3 - V_{LED\ (@\ I_S)}}{I_S}\ k\Omega$$

($I_S \leq 40$ mA)

WHERE $V_{LED\ (@\ I_S)}$ IS THE DIODE (LED) VOLTAGE DROP AT OPERATING CURRENT I_S.

EXAMPLE:

$I_S = 20$ mA

$V_{LED\ (@\ I_S)} = 3.4V$*

$V_{CC} = 5.0V$

$R_X = 65\Omega$

*MAN-1 OR EQUIVALENT

FIGURE 5. Nonmultiplex Application of the DM7447A

DM5446A/DM7446A, DM5447A/DM7447A

These circuits feature active-low, open collector high current outputs (Figure 4a). Each output is capable of sinking up to 40 mA at a maximum internal drop of 0.4V. This high current capability makes these circuits particularly well suited for driving the large MAN-1 or equivalent type displays directly. The circuits are also applicable, with or without the use of external current limit resistors, to driving lower current displays in the multiplex mode of drive.

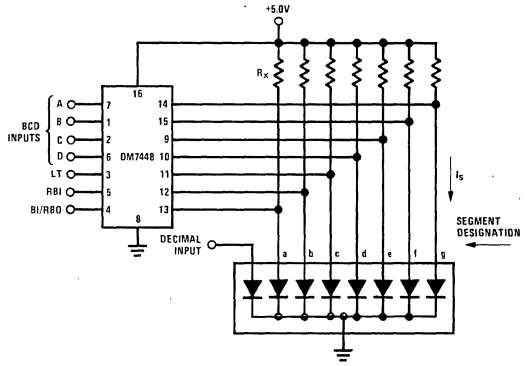
The DM5446A and DM7446A outputs are capable of withstanding 30V at a maximum leakage of 250μA over temperature. The DM5447A and DM7447A have a 15V output capability at a maximum leakage over temperature of 250μA. This standoff voltage ability makes the circuits applicable for direct drive to indicator lamp type displays. Figure 5 shows a typical application of the circuits with LEDs.

Refer to Table II for the operating temperature range and package types for the DM5446A/DM7446A and DM5447A/DM7447A.

DM5448/DM7448

The DM5448/DM7448 has active high passive pull-up outputs (Figure 4b) with a TTL fanout of 4. The typical output source current is 2.0 mA at an output voltage of 0.85V. Each output is capable of sinking 6.4 mA with a maximum internal drop of 0.4V. Since the output current level is low the circuit can be used to drive low current common cathode displays operating in the nonmultiplex mode.

The major application of the DM5448/DM7448 is to drive logic circuits, operate high-voltage loads such as electroluminescent displays through buffer transistors or SCR switches, or high-current



R_X MAY BE CALCULATED USING THE FOLLOWING EQUATION

$$R_X = \frac{5.0 - V_{LED}}{I_S - 1.6}\ k\Omega = \frac{3.3}{I_S - 1.6}\ k\Omega \quad \left[\begin{array}{l} V_{LED} = 1.7V\ @\ 5.0\ mA \\ R_X \geq 650\Omega \end{array}\right]$$

WHERE:

R_X = PULL-UP RESISTOR VALUE

I_S = CURRENT PER SEGMENT IN mA

EXAMPLE:

I_S = 5.0 mA

R_X = 970Ω

FIGURE 6. Nonmultiplex Application of the DM7448

loads through buffer transistors. Figure 6 shows the DM7448 in a low current direct drive LED application.

The operating temperature range and package types for the DM5448/DM7448 are given in Table II.

BCD TO 7-SEGMENT LED DRIVERS

DM7856/DM8856, DM8857, DM7858/DM8858

This series of three circuits was designed to provide a wide range of current capabilities in driving common cathode 7-segment LEDs operating in the multiplex or nonmultiplex mode. The circuits, discussed individually below, have output stages with varying source current capability designed for specific as well as general applications.

All circuits accept 4-bit BCD and decode this input to the desired 7-segment output format for direct drive to LEDs. In addition, the circuits feature a lamp test pin for display turn-on check, ripple blanking-input pin and blanking input/ripple blanking output pin which may be used to modulate display intensity.

The three circuits are TTL-DTL compatible and provide full decoding of the 16 possible input combinations. All parts operate off of a single 5.0V supply.

DM7856/DM8856

The DM7856/DM8856 output stages, passive-pullup (active high, Figure 4b), provide a typical source current of 6.0 mA at an output voltage of 1.7V. This current level was designed for directly driving, without the use of external current limit resistors, the MAN-4 or equivalent type displays in the nonmultiplex mode of operation.

Each output has a fan-out of 4 and is capable of sinking 6.4 mA with a maximum internal drop of 0.4V making the circuit suitable for use with logic circuits. With the use of an external buffer transistor per output the circuit may be used to drive high current common anode LED displays as well as high voltage electroluminescent displays. Figure 7 shows a typical application of the DM8856.

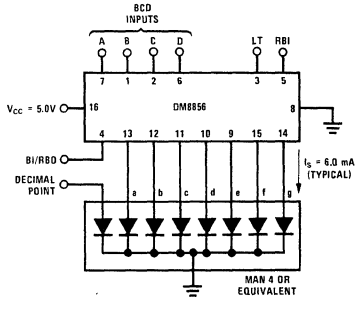


FIGURE 7. Nonmultiplex Application of the DM8856

Operating temperature range and package types for the DM7856/DM8856 are given in Table II.

DM8857

The output stages of the DM8857, active pull-up (active-high, Figure 4c), source a typical current

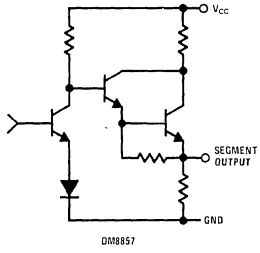


FIGURE 4c. Output Stage

of 50 mA at an output voltage of 2.3V. The circuit was designed to be used with MAN-4 or equivalent type displays operating in the multiplex mode of drive. With this high current capability the circuit can drive up to 16 such digits.

The applications of this circuit obviously are not limited to just the MAN-4 type of display. Common cathode displays with high dc current requirements or lower multiplex current levels may be driven by this circuit with the use of an external current limit resistor per segment. A typical application of the DM8857 is given in Figure 8.

Table II gives the operating temperature range and package type for the DM8857.

DM7858/DM8858

The DM7858/DM8858 output stages are active pull-up (active-high, Figure 4d) like those of the

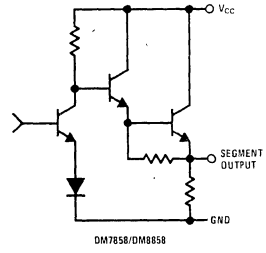
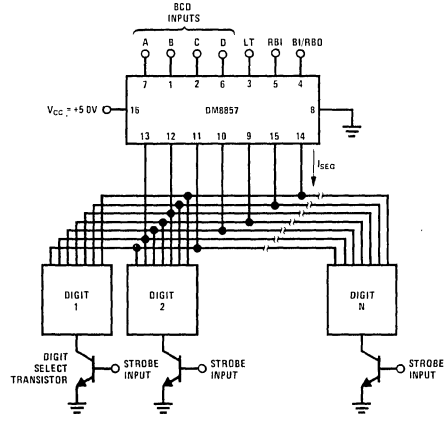


FIGURE 4d. Output Stage

DM8857. The output stages are exactly the same as the DM8857 except that the internal current limit resistor per output has been removed. External current limit resistors must then be used. This allows the circuit to be customized for a particular common cathode multiplex or non-multiplex application. Each output stage, through its own external resistor, can be programmed to some current from 50 mA down to 0 mA. Care must be taken in not shorting the outputs to ground because of the excessive current flow that would result from the Darlington upper stage. See Figure 9 for a typical application of the DM8858.



FOR MULTIPLEX OR NONMULTIPLEX APPLICATIONS WHERE AN EXTERNAL CURRENT LIMIT RESISTOR PER SEGMENT IS REQUIRED SEE THE OUTPUT CURRENT VS VOLTAGE CURVE FOR THE DM8857 AND USE THE EQUATION GIVEN IN FIGURE 9 TO CALCULATE THE RESISTOR VALUE.

DM8857 Output Current vs Voltage

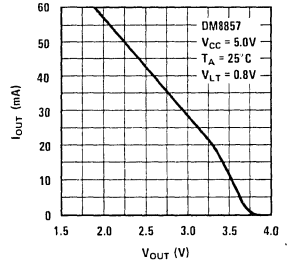


FIGURE 8. DM8857 Typical Multiplexing Scheme

Maximum output source current per segment for the DM7858/DM8858 is 50 mA. Operating temperature range and package types are given in Table II.

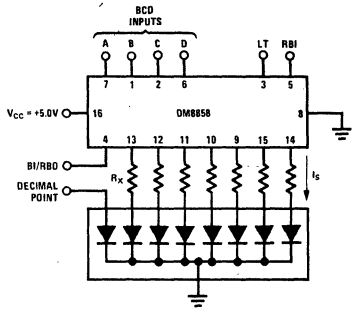
Special care must be taken in the use of the DM7858 ceramic and the DM8858 plastic DIP's with regard to not exceeding the maximum operating junction temperature of the devices. The maximum junction temperature of the DM7858J is 150°C and must be derated based on a thermal resistance of 80°C/Watt, junction to ambient. The maximum junction temperature for the DM8858N is 150°C and must be derated based on a thermal resistance of 140°C/Watt, junction to ambient.

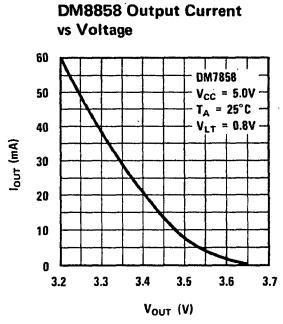
DM75491, DM8861 MOS TO LED SEGMENT DRIVERS

The DM75491 and DM8861 were designed for MOS calculator applications. Both circuits feature low input current, 3.3 mA maximum at 10V input, making them suitable for direct drive from MOS circuits. The circuits are used to drive the paralleled segments in multi-digit displays. Since both circuits feature accessable collectors and emitters they may be used as either common cathode or anode segment drivers. They feature a source or sink current capability of up to 50 mA with a maximum collector to emitter drop of 1.5V over the operating temperature range. In addition, each output is specified to have a maximum leakage of 100μA at an output voltage of 10V over temperature. Both circuits operate from a single supply that can have a maximum voltage of 10V.

DM75491 FOUR SEGMENT DRIVER

The DM75491 is a four segment driver whose main application is with multi-digit LEDs operating in the multiplex mode of drive. Each package contains four separate segment drivers, each driver





TO FIND THE APPROPRIATE VALUE OF THE SEGMENT CURRENT LIMIT RESISTOR R_X THE FOLLOWING EQUATION SHOULD BE USED.

$$R_X = \frac{V_{OUT} - V_D}{I_S}$$

WHERE:

I_S = SEGMENT CURRENT

V_D = LED DIODE DROP AT CURRENT I_S

V_{OUT} = DM8858 OUTPUT VOLTAGE AT CURRENT I_S (SEE GRAPH)

EXAMPLE:

I_S = 5.0 mA

V_D = 1.7V (AT 5.0 mA)

FROM GRAPH (V_{CC} = 5.0V, T_A = 25°C)

V_{OUT} = 3.53V (AT 5.0 mA)

$$R_X = \frac{3.53V - 1.7V}{5.0\ mA}$$

R_X = 360Ω

THE SAME EQUATION MAY BE USED WHEN EITHER THE DM7858 OR THE DM8858 ARE OPERATING IN THE MULTIPLEX MODE OF DRIVE. IF THE ADDITIONAL VOLTAGE DROP DUE TO THE DIGIT DRIVER IS TAKEN INTO CONSIDERATION THE NEW EQUATION WOULD HAVE THE FOLLOWING FORM:

$$R_X = \frac{V_{OUT} - V_D - V_{DR}}{I_S}$$

V_{DR} = DIGIT DRIVER DROP AT CURRENT I_S

FIGURE 9. DM8858 Applications

with free collector and emitter points, see Figure 4e.

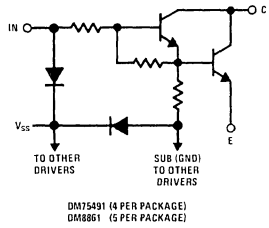


FIGURE 4e. Circuit Schematic

In the multiplex mode of drive, a six digit calculator needs only two DM75491's to drive the segments in the display, see Figure 10. The total of eight segment drivers allows drive to each of the individual seven segments plus logic control for the decimal point. Figure 11 shows the DM75491 used in an 8 digit calculator application.

Table II lists the package type and temperature range of the DM75491.

DM8861 FIVE SEGMENT DRIVER

The DM8861 is a five segment driver which like the DM75491 is used with multi-digit LEDs operating in the multiplex mode of drive. Each package contains five separate drivers, each driver with free collector and emitter points, Figure 4e.

A typical application of the DM8861 is given in Figure 11 where the DM8861 is combined with the DM75491 to provide a total of nine independent sources of LED segment current from an MOS calculator. This allows control of the 7-segments plus decimal point and minus sign. This combination of circuits is not solely applicable to just the 8 digit calculator configuration shown but can be used with a display having as many digits as desired as long as the multiplexed segment current requirement does not exceed 50 mA.

As with the DM75491, the DM8861 is also applicable to use with common anode displays as well as common cathode since each driver has its collector bonded out to a separate pin.

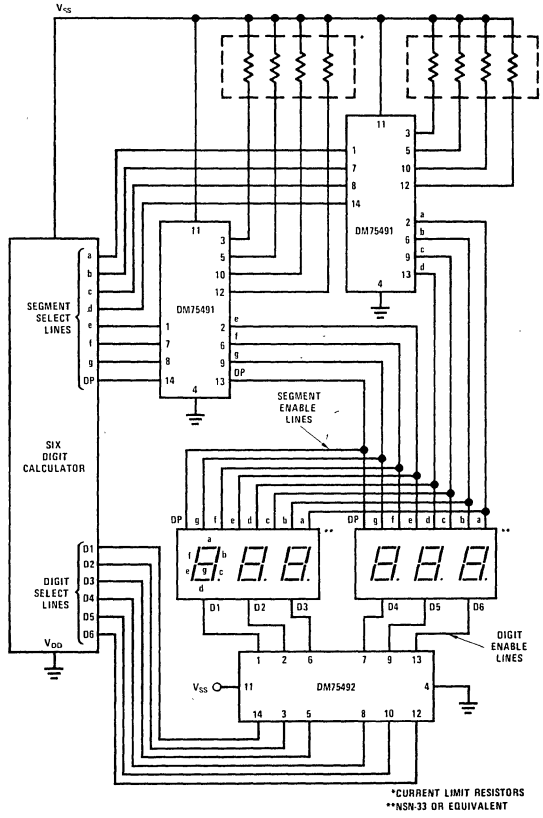


FIGURE 10. 6-Digit Calculator

Refer to Table II for operating temperature range and package type for the DM8861.

DM75492, DM8863 MOS TO LED DIGIT DRIVERS

The DM75492 and DM8863 are digit drivers designed to drive multi-digit common cathode LEDs directly from MOS circuits. Since digit currents are quite high in multiplex operation MOS circuits usually cannot sink the required digit select current, therefore these circuits provide the required current buffering. The two circuits have different current handling capability as well as different numbers of drivers per package, each will be discussed individually later.

The circuits are totally compatible for use with both the DM75491 and the DM8861. The most common usage of the circuits is in MOS calculator applications where the DM75491 or the DM8861 source the segment current and either the DM75492 or the DM8863 sink the digit current.

DM75492 SIX DIGIT DRIVER

The DM75492 is a six digit LED driver designed to be used with common cathode multi-digit displays operating in the multiplex mode of drive.

The circuit features six high gain Darlington connected transistors, with collectors open and emitters tied to ground (Figure 4f), capable of

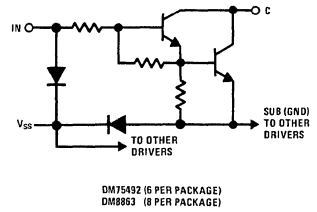
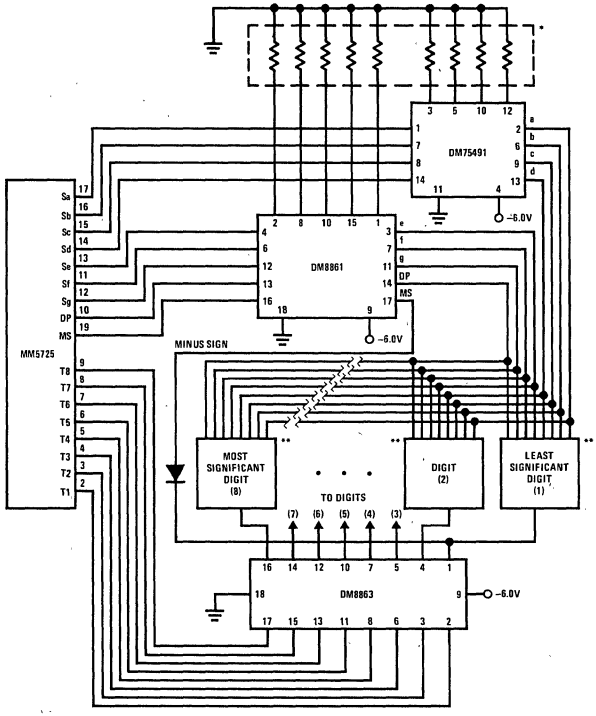


FIGURE 4f. Circuit Schematic

sinking up to 250 mA with a maximum collector to ground drop of 1.5V over the operating temperature range. Low input current of 3.3 mA maximum at 10V makes the drivers suitable for direct connection to MOS circuits. Output leakage is 200μA maximum at 10V over temperature. Maximum V_{CC} is 10V.



In Figure 10 the DM75492 is shown along with the DM75491 in a typical six digit calculator application. Since the calculator circuit shown is operated in the multiplex mode of drive only one DM75492 is required, replacing at least six transistors and resistors for the equivalent discrete circuit.

The operating temperature range and package type for the DM75492 is given in Table II.

DM8863 EIGHT DIGIT DRIVER

The DM8863 is an eight digit LED driver designed to be used in conjunction with either the DM75491 and/or the DM8861 in driving eight common cathode LED digits operating in the multiplex mode of drive.

This circuit features eight separate high gain Darlington connected transistor circuits, see Figure 4f. Each Darlington transistor pair is capable of sinking 500 mA with a maximum collector to ground drop of 1.6V. Each collector can withstand 10V at a maximum leakage of 250μA in the off state. Maximum input current is 2.0 mA at 10V, making the circuit particularly well suited for direct drive from MOS circuits.

Figure 11 shows the DM8863 used in a typical 8-digit calculator application. The important feature of the DM8863 is the very high sink current capability. This allows multiplex operation of large digits or large numbers of digits without the use of discrete high current transistors.

Another application of the DM8863 is shown in Figure 12. In this case the DM8863 is used along with the MM4311/MM5311 series digital clock circuits in the implementation of a 6-digit clock display. Here the DM8863 is used as a segment driver for a common anode display. The use of the DM8863 in this manner replaces a total of 14 resistors and 7 transistors.

The DM8863 uses a single supply with a maximum voltage of 10V. Table II specifies the operating temperature range and package type for the DM8863.

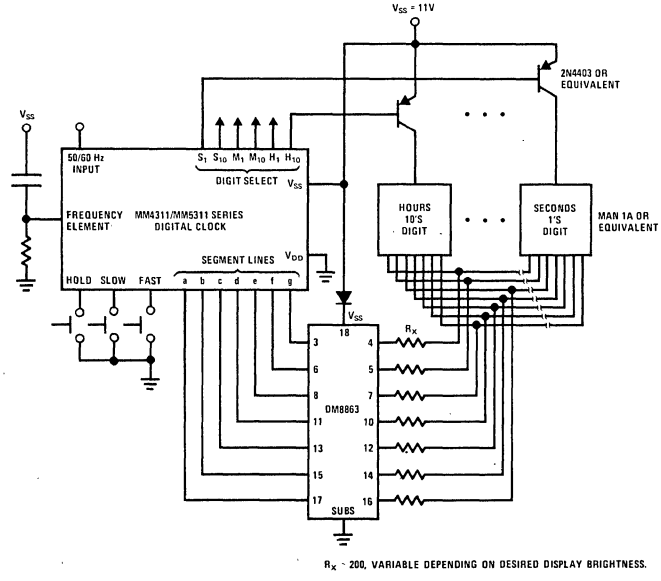


FIGURE 12. Digital Clock Using DM8863

DM8864, DM8865, DM8866 MOS TO LED DIGIT DRIVERS

The DM8864, DM8865, and DM8866 were designed to drive common cathode nine, eight, and seven digit displays respectively. The applications of these drivers are similar to those of the DM75492 and DM8863 except that operating current levels are lower.

All circuits feature maximum input current of 2.0 mA at a voltage of 6.5V. Output sink capability is 50 mA at a maximum collector to ground drop of 1.5V. Output leakage is 40μA (max) at an output voltage of 6.0V. All circuits operate from a supply that can vary from 5.0V to 9.5V.

DM8864 NINE DIGIT DRIVER

The DM8864 is a nine digit common cathode LED driver. Each package contains nine separate digit drivers. The circuit also features a "low battery" indicator driver which will light a decimal point whenever a 9.0V battery drops below 6.5V typical.

Figure 13 shows the DM8864 in a typical calculator drive application. The operating temperature range and package type for the DM8864 is given in Table II.

DM8865 EIGHT DIGIT DRIVER

The DM8865 is an eight digit common cathode LED driver. Eight separate drivers are contained within each package. As with the DM8864 and DM8866 the DM8865 can also be used as a segment driver for common anode displays in the multiplex or nonmultiplex mode as long as the segment current does not exceed 50 mA.

Table II gives the operating temperature range and package type for the DM8865.

DM8866 SEVEN DIGIT DRIVER

The DM8866 is a seven digit common cathode LED driver. Each package contains seven separate digit drivers. Logic is also provided for a "low battery" indicator which will detect a 9.0V battery drop to below 6.5V typical and drive a decimal point.

Table II lists the package type and temperature range of the DM8866.

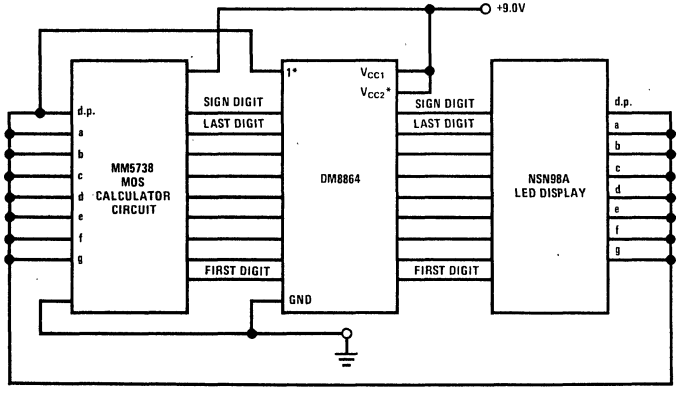


FIGURE 13. A Typical Application of the DM8864, Showing a Complete 8-Digit, 5 Function Calculator with Memory.

Section 6
Memory Support

6

TEMPERATURE RANGE		DESCRIPTION	PAGE NUMBER
−55°C to +125°C	0°C to +70°C		
—	DS0025C	2-Phase PMOS Clock Driver	6-4
*DS0026	DS0026C	2-Phase PMOS Clock Driver	6-7
*DS0056	DS0056C	2-Phase PMOS Clock Driver	6-7
—	DS3245	Quad MOS Clock Driver	6-14
DS1617	DS3617	Bubble Memory Sense Amplifier	6-17
*DS1628	DS3628	Octal TRI-STATE MOS Driver	6-24
*DS1644	DS3644	Quad TTL-to-MOS Clock Drivers	6-27
*DS1674	DS3674	Quad TTL-to-MOS Clock Drivers	6-27
*DS1645	DS3645	Hex TRI-STATE TTL-to-MOS Latch/Drivers	6-30
*DS1675	DS3675	Hex TRI-STATE TTL-to-MOS Latch/Drivers	6-30
*DS1647	DS3647	Quad TRI-STATE I/O Registers	6-35
*DS1677	DS3677	Quad TRI-STATE I/O Registers	6-35
*DS16147	DS36147	Quad TRI-STATE I/O Registers	6-35
*DS16177	DS36177	Quad TRI-STATE I/O Registers	6-35
*DS1648	DS3648	TRI-STATE TTL-to-MOS Multiplexer/Driver	6-41
*DS1678	DS3678	TRI-STATE TTL-to-MOS Multiplexer/Driver	6-41
*DS1649	DS3649	Hex TRI-STATE TTL-to-MOS Driver	6-46
*DS1679	DS3679	Hex TRI-STATE TTL-to-MOS Driver	6-46
*DS1651	DS3651	Quad High Speed MOS Sense Amplifiers	6-49
*DS1653	DS3653	Quad High Speed MOS Sense Amplifiers	6-49
*DS1671	DS3671	Dual Bootstrapped 2-Phase Clock Driver	6-55
—	DS3685	Hex TRI-STATE Latch	6-59
*DS16149	DS36149	Hex MOS Drivers	6-62
*DS16179	DS36179	Hex MOS Drivers	6-62
*DS55325	DS75325	Memory Drivers	6-66
—	DS75361	Dual TTL-to-MOS Driver	6-73
—	DS75362	Dual TTL-to-MOS Driver	6-78
—	DS75365	Quad TTL-to-MOS Driver	6-83
—	AN-76	Applying Modern Clock Drivers to MOS Memories	6-88

*Also available screened in accordance with MIL-STD-883 Class B. Refer to National Semiconductor's "The Reliability Handbook".

4k & 16k N-CHANNEL MOS MEMORY INTERFACE CIRCUITS

Page No.	Device Number and Name	5V Clock Drivers	12V Clock Drivers	4k RAM Address Drivers	16k RAM Address Drivers	Data I/O	Timing & Control Drivers
6-17	DS3617 Bubble Memory Sense Amplifier						
6-24	DS3628 Octal TRI-STATE® MOS Driver	•			•		•
6-27	DS3644, DS3674 Quad MOS Clock Driver		•				
6-14	DS3245 Quad MOS Clock Driver		•				
6-30	DS3645, DS3675 Hex TRI-STATE MOS Driver Latch			•			
6-35	DS3647, DS3677, DS36147, DS36177 Quad TRI-STATE MOS Memory I/O Register					•	
6-41	DS3648, DS3678 TRI-STATE MOS Multiplexer/Driver	•		•	•		•
6-46	DS3649, DS3679 Hex TRI-STATE MOS Driver	•		•			•
6-59	DS3685 Hex TRI-STATE Latch						
6-62	DS36149, DS36179 Hex MOS Driver	•		•			•
6-66	DS75325 Memory Driver						
6-73	DS75361 Dual TTL-to-MOS Driver		•				
6-78	DS75362 Dual TTL-to-MOS Driver		•				
6-83	DS75365 Quad TTL-to-MOS Driver		•				
2-5	DP8303, DP8304B, DP8307, DP8308 8-Bit Bidirectional Transceiver					•	
8-11	DP8216, DP8226 4-Bit Bidirectional Transceiver					•	
2-89	DS8T26, DS8T28 Quad TRI-STATE Bus Driver					•	
8-4	DP8212 8-Bit Input/Output Port					•	

P-CHANNEL MOS INTERFACE CIRCUITS

FUNCTION	CHARACTERISTICS	TEMPERATURE		PAGE NO.
		0°C to +70°C	−55°C to +125°C	
Clock Driver	Dual, 30V, Drive 1000 pF @ 1 MHz	DS0025C		6-4
Clock Driver	Dual, 20V, Drive 1000 pF @ 5 MHz	DS0026C	DS0026	6-7
Clock Driver	Same as DS0026, May Use Pull-Up Resistor	DS0056C	DS0056	6-7
Clock Driver	Same as DS0026, May Be Bootstrapped	DS3671	DS1671	6-55
Differential Sense Amplifier	Quad TRI-STATE ±7 mV Sensitivity	DS3651	DS1651	6-49
Differential Sense Amplifier	Quad Open-Collector ±7 mV Sensitivity	DS3653	DS1653	6-49

Note. Refer to Application Note 76 for additional information on clock drivers.

National Semiconductor

DS0025C Two Phase MOS Clock Driver

General Description

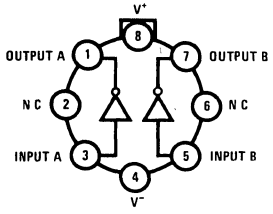
The DS0025C is a monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL line drivers or buffers such as the DS8830 or DM7440. Two input coupling capacitors are used to perform the level shift from TTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse widths may be set by selection of the input capacitor eliminating the need for tight input pulse control.

Features

- 8-lead TO-5 or 8-lead or 14-lead dual-in-line package
- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DS8830, DM7440
- "Zero" Quiescent Power

Connection Diagrams

Metal Can Package

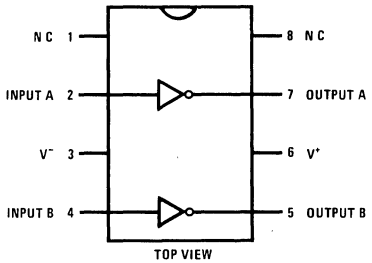


Note: Pin 4 connected to case.

TOP VIEW

Order Number DS0025CH
See NS Package H08C

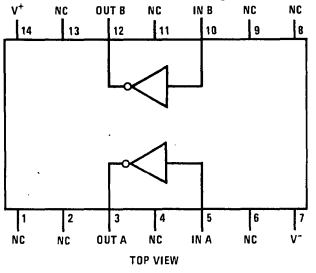
Dual-In-Line Package



TOP VIEW

Order Number DS0025CN
or DS0025CJ-8
See NS Package N08A or J08A

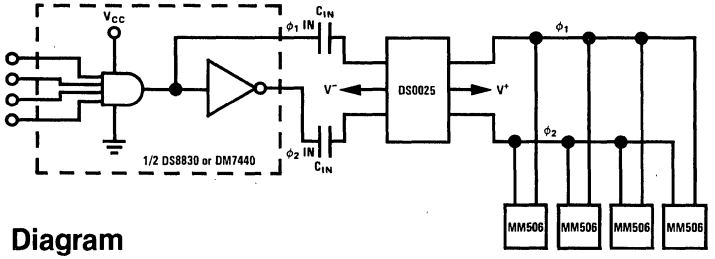
Dual-In-Line Package



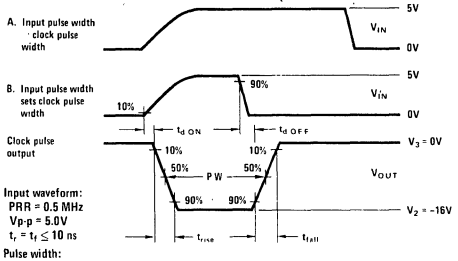
TOP VIEW

Order Number DS0025CJ
See NS Package J14A

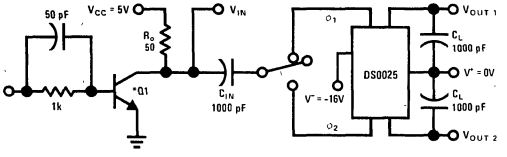
Typical Application



Timing Diagram



AC Test Circuit



*Q1 is selected high speed NPN switching transistor.

Absolute Maximum Ratings (Note 1)

(V^+ – V) Voltage Differential	30V
Input Current	100 mA
Peak Output Current	1.5A
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Maximum Power Dissipation* at 25°C	
8-Pin Cavity Package	1150 mW
14-Pin Cavity Package	1410 mW
Molded Package	1080 mW
Metal Can (TO-5) Package	670 mW

*Derate 8-pin cavity package 7.8 mW/°C above 25°C; derate 14-pin cavity package 9.5 mW/°C above 25°C; derate molded package 8.7 mW/°C above 25°C; derate metal can (TO-5) package 4.5 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3) See test circuit.

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{dON}	Turn-On Delay Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF			15	30	ns
t_{RISE}	Rise Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF			25	50	ns
t_{dOFF}	Turn-Off Delay Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF (Note 4)			30	60	ns
t_{FALL}	Fall Time	C_{IN} = 0.001μF, R_{IN} = 0Ω,	(Note 4)	60	90	120	ns
		C_L = 0.001μF	(Note 5)	100	150	250	ns
PW	Pulse Width (50% to 50%)	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF (Note 5)			500		ns
V_{O+}	Positive Output Voltage Swing	V_{IN} = 0V, I_{OUT} = −1 mA		V^+−1.0	V^+−0.7V		V
V_{O-}	Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA			V^-+0.7V	V^-+1.5V	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS0025C.

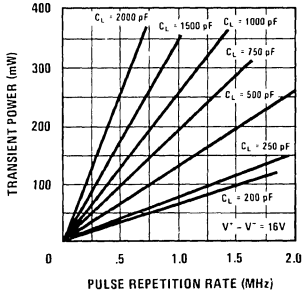
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Parameter values apply for clock pulse width determined by input pulse width.

Note 5: Parameter values for input pulse width greater than output clock pulse width.

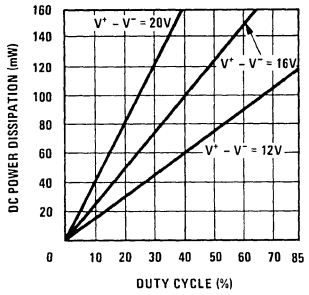
Typical Performance

Transient Power vs Rep. Rate



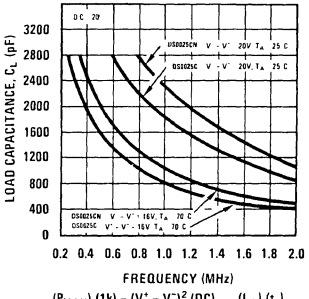
$P_{AC} = (V^+ - V^-)^2 f C_L$

DC Power (P_{DC}) vs Duty Cycle



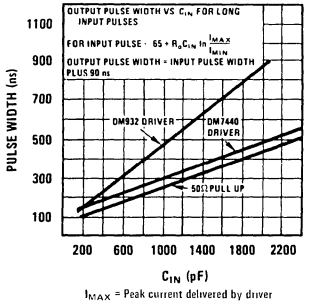
$$P_{DC} = \frac{(V^+ - V^-)^2 (DC)}{1k}$$

Maximum Load Capacitance



$$C_L < \frac{(P_{MAX})(1k) - (V^+ - V^-)^2 (DC)}{(f)(1k)(V^+ - V^-)^2} < \frac{(I_{pk})(t_r)}{V^+ - V^-}$$

Output PW Controlled by C_{IN}



I_{MAX} = Peak current delivered by driver

$$I_{MIN} \sim \frac{V_{DC}}{R1} = \frac{0.6}{1k}$$

Applications Information (Reference AN-76)

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents from V^- to V^+ cannot occur.

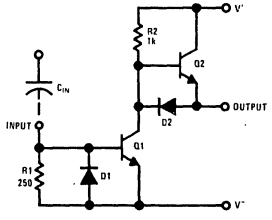


FIGURE 1. DS0025 Schematic (One-Half Circuit)

Fan-Out Calculation

The drive capability of the DS0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

Transient Current

The maximum peak output current of the DS0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L (V^+ - V^-)}{t_r} \qquad (1)$$

Typical rise times into 1000 pF load is 25 ns For $V^+ - V^- = 20V$, I = 0.8A.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \qquad (2)$$

For $V^+ - V^- = 20V$, f = 1.0 MHz, C_L = 1000 pF, P_{AC} = 400 mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

= 80 mW for $V^+ - V^- = 20V$, DC = 20%

Package Power Dissipation

Total average power = transient output power + internal power

Example Calculation

How many MM506 shift registers can be driven by a DS0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30-50 ns and 16V amplitude over the temperature range 0-70°C?

Power Dissipation:

At 70°C the DS0025CN can dissipate 870 mW when soldered into printed circuit board.

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one-half of the DS0025C, 870 mW ÷ 2 can be dissipated.

435 mW = 50 mW + transient output power

385 mW = transient output power

Using equation (2) at 16V, 1 MHz and 350 mW, each half of the DS0025CN can drive a 1367 pF load. This is less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 1367 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is 1367/80 or 17 registers.

National Semiconductor

DS0026, DS0056 5 MHz Two Phase MOS Clock Drivers

General Description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to ($V^+ - 0.1V$) in the off state.

For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

These devices are available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt ceramic DIP, and TO-8 packages.

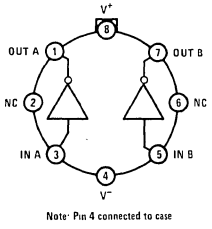
Features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

6

Connection Diagrams (Top Views)

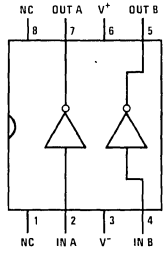
TO-5 Package



Note: Pin 4 connected to case

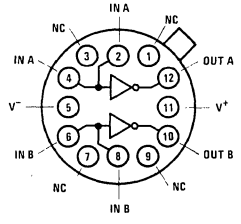
Order Number DS0026H or DS0026CH
See NS Package H08C

Dual-In-Line Package



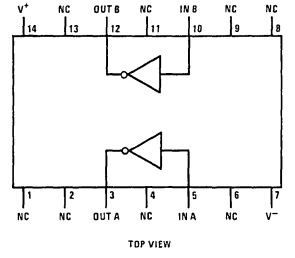
Order Number DS0026CJ-8, DS0026CN or DS0026J-8
See NS Package J08A or N08A

TO-8 Package



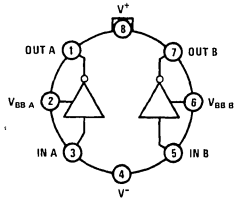
Order Number DS0026G or DS0026CG
See NS Package G12C

Dual-In-Line Package



Order Number DS0026J or DS0026CJ
See NS Package J14A

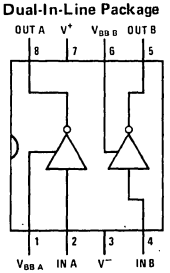
TO-5 Package



Note: Pin 4 connected to case.

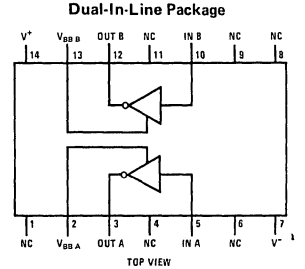
Order Number DS0056H or DS0056CH
See NS Package H08C

Dual-In-Line Package



Order Number DS0056J-8, DS0056CJ-8 or DS0056CN
See NS Package J08A or N08A

Dual-In-Line Package



Order Number DS0056J or DS0056CJ
See NS Package J14A

Absolute Maximum Ratings (Note 1)

$V^+ - V^-$ Differential Voltage	22V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A
Maximum Power Dissipation* at 25°C	
Cavity Package (8-Pin)	1150 mW
Cavity Package (14-Pin)	1380 mW
Molded Package	1040 mW
Metal Can (TO-5) Package	660 mW

Operating Temperature Range	
DS0026, DS0056	−55°C to +125°C
DS0026C, DS0056C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate 8-pin cavity package 7.7 mW/°C above 25°C; derate 14-pin cavity package 9.3 mW/°C above 25°C; derate molded package 8.4 mW/°C above 25°C; derate metal can (TO-5) package 4.4 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logic "1" Input Voltage	$V^- = 0V$		2	1.5		V
I_{IH}	Logic "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logic "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logic "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OL}	Logic "1" Output Voltage	$V_{IN} - V^- = 2.4V$			V^-+0.7	V^-+1.0	V
V_{OH}	Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$, $V_{BB} \geq V^+ + 1.0V$	DS0026	V^+−1.0	V^+−0.7		V
			DS0056	V^+−0.3	V^+−0.1		V
$I_{CC(ON)}$	"ON" Supply Current (one side on)	$V^+ - V^- = 20V$ $V_{IN} - V^- = 2.4V$ (Note 6)	DS0026		30	40	mA
			DS0056		12	30	mA
$I_{CC(OFF)}$	"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0V$	70°C		10	100	μA
			125°C		10	500	μA

Switching Characteristics (T_A = 25°C) (Notes 5 and 7)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ON}	Turn-on Delay	*(Figure 1)*		5	7.5	12	ns
		(Figure 2)			11		ns
t_{OFF}	Turn-off Delay	*(Figure 1)*			12	15	ns
		(Figure 2)			13		ns
t_r	Rise Time	*(Figure 1)*,	C_L = 500 pF		15	18	ns
		(Note 5)	C_L = 1000 pF		20	35	ns
		(Figure 2),	C_L = 500 pF		30	40	ns
		(Note 5)	C_L = 1000 pF		36	50	ns
t_f	Fall Time	*(Figure 1)*,	C_L = 500 pF		12	16	ns
		(Note 5)	C_L = 1000 pF		17	25	ns
		(Figure 2),	C_L = 500 pF		28	35	ns
		(Note 5)	C_L = 1000 pF		31	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply for $V^+ - V^-$ = 10V to 20V, C_L = 1000 pF, over the temperature range of −55°C to +125°C for the DS0026, DS0056 and 0°C to +70°C for the DS0026C, DS0056C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: All typical values for the T_A = 25°C.

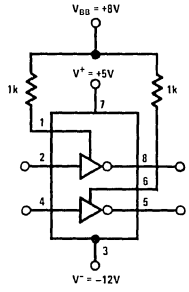
Note 5: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

Note 6: I_{BB} for DS0056 is approximately $(V_{BB} - V^-)/1\ k\Omega$ (for one side) when output is low.

Note 7: The high current transient (as high as 1.5A) through the resistance of the external interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

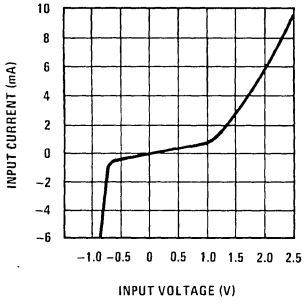
Typical V_{BB} Connection

DS0056

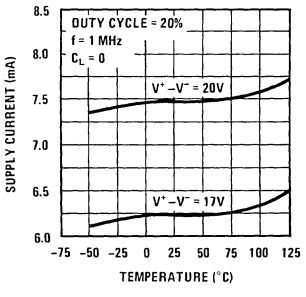


Typical Performance Characteristics

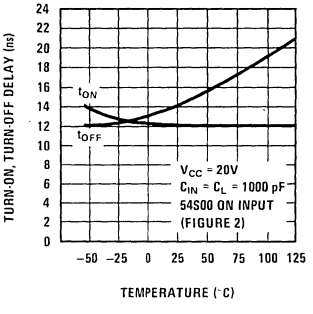
Input Current vs Input Voltage



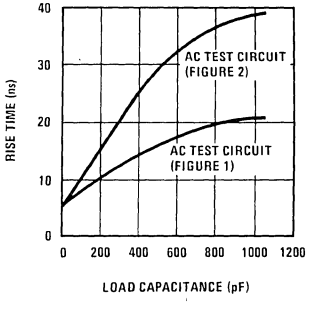
Supply Current vs Temperature



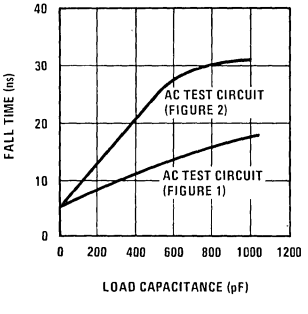
Turn-On and Turn-Off Delay vs Temperature



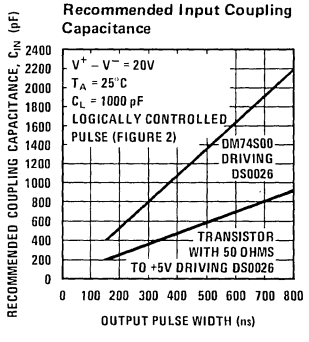
Rise Time vs Load Capacitance



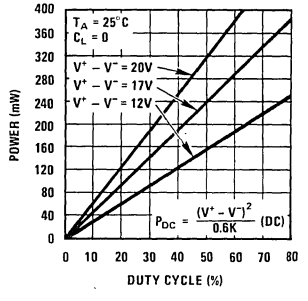
Fall Time vs Load Capacitance



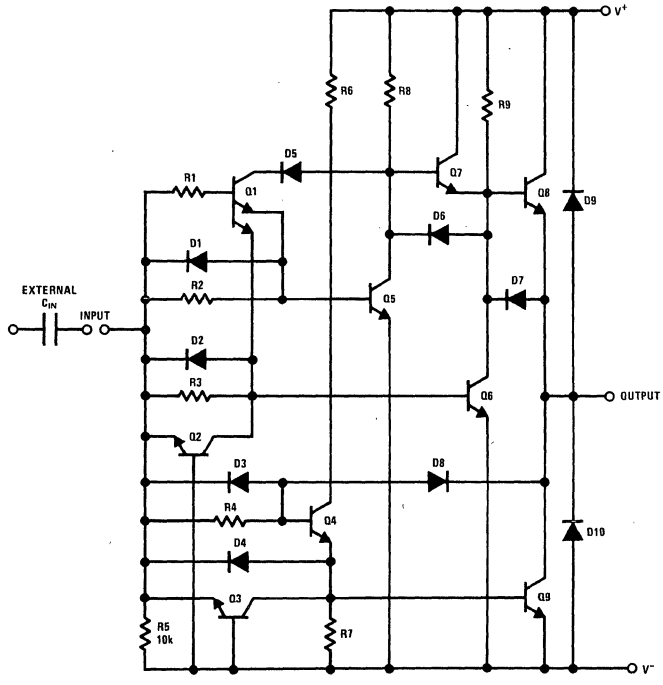
Recommended Input Coupling Capacitance



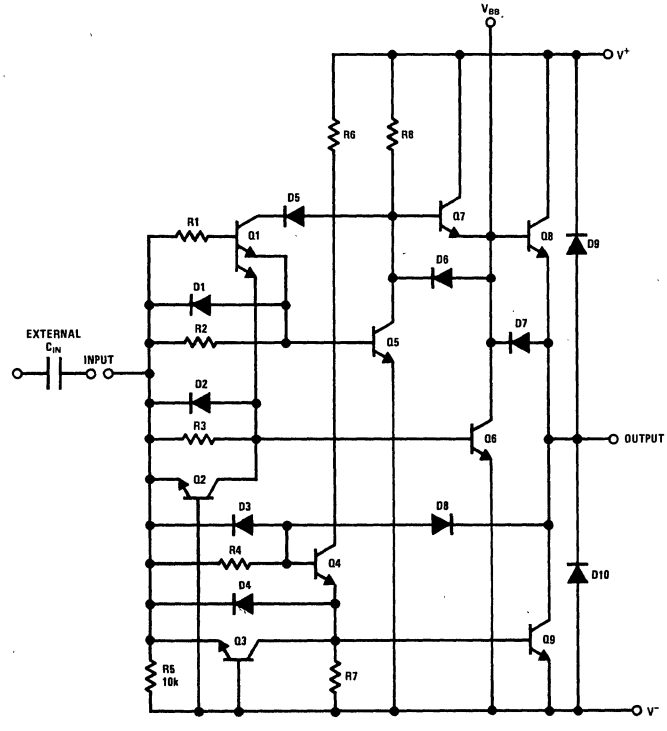
DC Power (P_{DC}) vs Duty Cycle



Schematic Diagrams

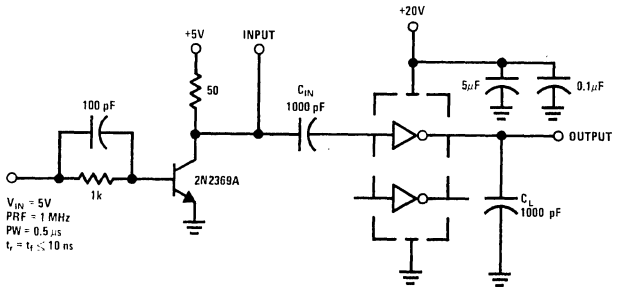


1/2 DS0026



1/2 DS0056

AC Test Circuits and Switching Time Waveforms



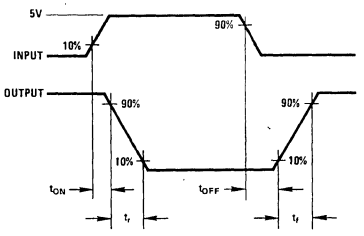
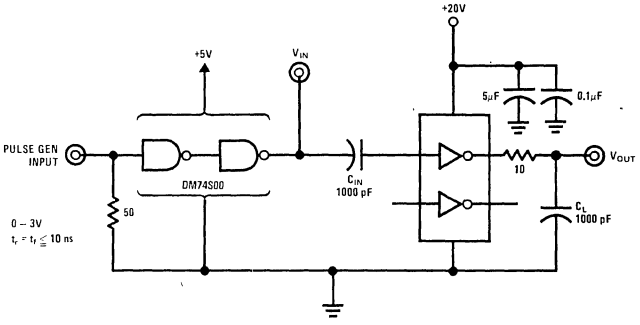


FIGURE 1.



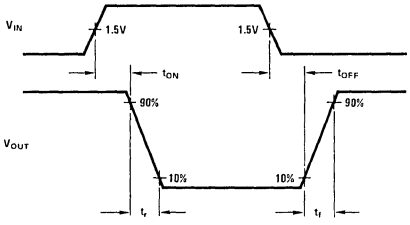
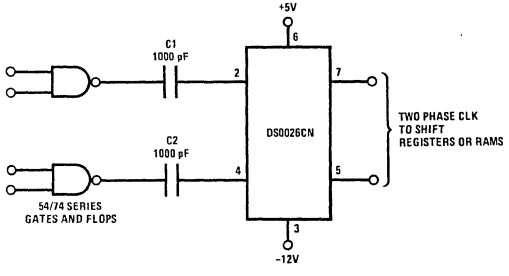


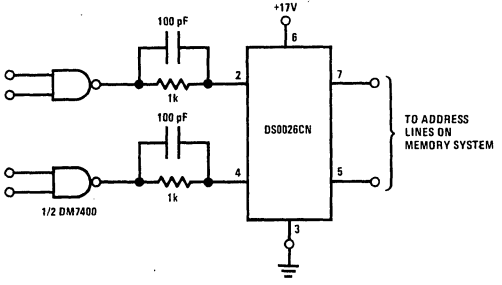
FIGURE 2.

Typical Applications

AC Coupled MOS Clock Driver



DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



Application Hints

DRIVING THE MM5262 WITH THE DS0056 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 6* shows the clock

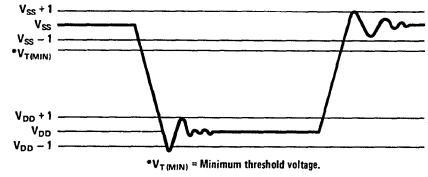


FIGURE 6. Clock Waveform

specification, in diagram form, with idealized ringing sketched in. The ringing of the clock about the V_{SS} level is particularly critical. If the $V_{SS} - 1$ V_{OH} is not maintained, at *all* times, the information stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were −1.3V, the clock going to $V_{SS} - 1$ would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.

Controlling the clock ringing is particulary difficult because of the relative magnitude of the allowable ringing, compared to the magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damping resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10 ohms to 20 ohms is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

The recommended clock driver for use with the MM4262/MM5262 is the DS0056/DS0056C dual clock driver. This device is designed specifically for use with dynamic circuits using a substrate, V_{BB}, supply. Typically it will drive a 1000 pF load with 20 ns rise and fall times. *Figure 7* shows a schematic of a single driver.

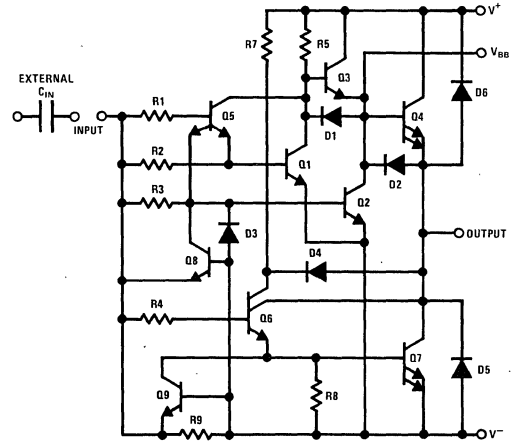


FIGURE 7. Schematic of 1/2 DS0056

In the case of the MM5262, V^+ is a +5V and V_{BB} is +8.5V. V_{BB} should be connected to the V_{BB} pin shown in *Figure 7* through a 1 kΩ resistor. This allows transistor Q4 to saturate, pulling the output to within a $V_{CE(SAT)}$ of the V^+ supply. This is critical because as was shown before, the $V_{SS} - 1.0$V clock level must not be exceeded at any time. Without the V_{BB} pull up on the base of Q4 the output at best will be 0.6V below the V^+ supply and can be 1V below the V^+ supply reducing the noise margin or this line to zero.

Application Hints (Continued)

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 8* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

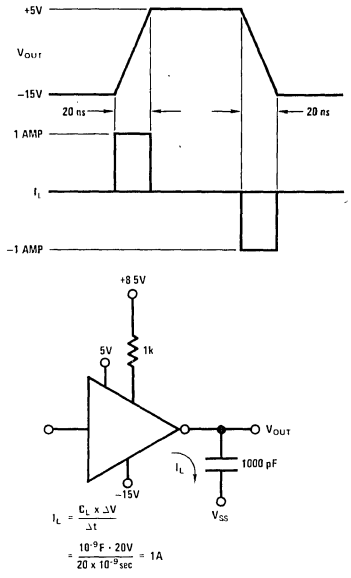


FIGURE 8. Clock Waveforms (Voltage and Current)

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies, A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. A bypass capacitor for each DS0056 is recommended. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0056 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since this noise is difficult to detect with an oscilloscope it is often overlooked.

Lastly, the clock lines must be considered as noise generators. *Figure 9* shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock tranisent from the 7404 because of the inductance, L.

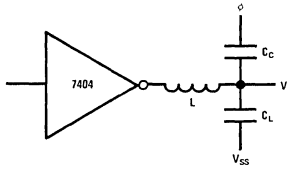


FIGURE 9. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \left(\frac{1}{56+1}\right) = 0.35V$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.3V of noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1\ mA$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262, coupling noise from the $\phi 2$ clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from $\phi 1$ clock.

National Semiconductor

DS3245 Quad MOS Clock Driver

General Description

The DS3245 is a quad bipolar-to-MOS clock driver with TTL compatible inputs. It is designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

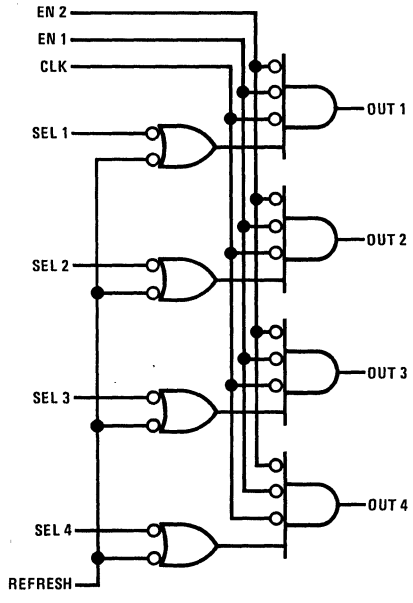
Only 2 supplies, 5 V_{DC} and 12 V_{DC}, are required without compromising the usual high V_{OH} specification obtained by circuits using a third supply.

The device features 2 common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

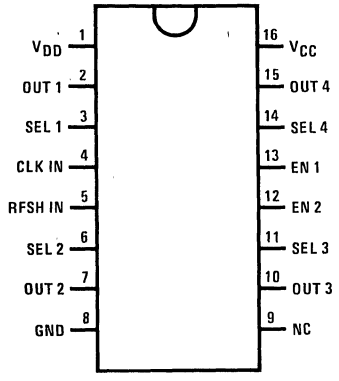
Features

- TTL compatible inputs
- Operates from 2 standard supplies: 5 V_{DC}, 12 V_{DC}
- Internal bootstrap circuit eliminates need for external PNP's
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function equivalent to Intel 3245

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3245J or DS3245N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +85°C
Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5 to +7V
Supply Voltage, V_{DD}	−0.5 to +14V
All Input Voltages	−1.0 to V_{DD}
Outputs for Clock Driver	−1.0 to V_{DD} +1V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Electrical Characteristics T_A = 0°C to +75°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{FD}	Select Input Load Current	V_F = 0.45V			−0.25	mA
I_{FE}	Enable Input Load Current	V_F = 0.45V			−1.0	mA
I_{RD}	Select Input Leakage Current	V_R = 5V			10	μA
I_{RE}	Enable Input Leakage Current	V_R = 5V			40	μA
V_{OL}	Output Low Voltage	I_{OL} = 5 mA, V_{IH} = 2V			0.45	V
		I_{OL} = −5 mA	−1.0			V
V_{OH}	Output High Voltage	I_{OH} = −1 mA, V_{IL} = 0.8V	V_{DD}−0.50			V
		I_{OH} = 5 mA			V_{DD}+1.0	V
V_{IL}	Input Low Voltage, All Inputs				0.8	V
V_{IH}	Input High Voltage, All Inputs		2			V
V_{CLAMP}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA		−1.0	−1.5	V

Power Supply Current Drain

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Current from V_{CC} Output in High State	V_{CC} = 5.25V, V_{DD} = 12.6V		26	34	mA
I_{DD}	Current from V_{DD} Output in High State	V_{CC} = 5.25V, V_{DD} = 12.6V		23	30	mA
I_{CC}	Current from V_{CC} Output in Low State	V_{CC} = 5.25V, V_{DD} = 12.6V		29	39	mA
I_{DD}	Current from V_{DD} Output in Low State	V_{CC} = 5.25V, V_{DD} = 12.6V		13	19	mA

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Switching Characteristics $T_A = 0°C$ to $+75°C$, $V_{CC} = 5V \pm 5\%$, $V_{DD} = 12V \pm 5\%$

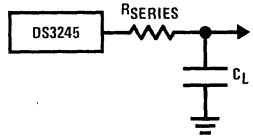
PARAMETER		CONDITIONS	MIN (Note 3)	TYP (Notes 4, 6)	MAX (Note 5)	UNITS
t_{-+}	Input to Output Delay	$R_{SERIES} = 0$	5	11		ns
t_{DR}	Delay Plus Rise Time	$R_{SERIES} = 0$		20	32	ns
t_{+-}	Input to Output Delay	$R_{SERIES} = 0$	3	7		ns
t_{DF}	Delay Plus Fall Time	$R_{SERIES} = 0$		18	32	ns
t_T	Output Transition Time	$R_{SERIES} = 20\Omega$	10	17	25	ns
t_{DR}	Delay Plus Rise Time	$R_{SERIES} = 20\Omega$		27	38	ns
t_{DF}	Delay Plus Fall Time	$R_{SERIES} = 20\Omega$		25	38	ns

Capacitance $T_A = 25°C$ (Note 7)

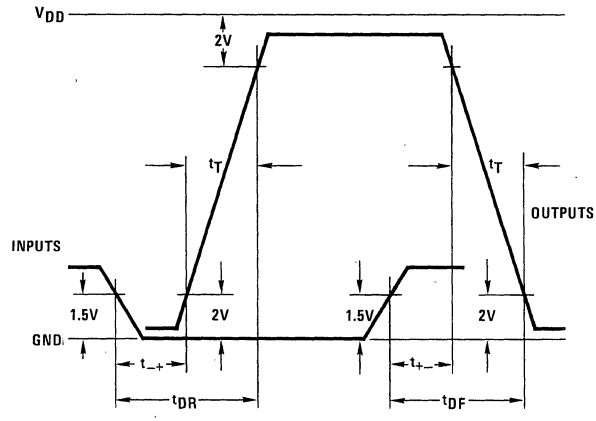
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance, $\overline{I1}$, $\overline{I2}$, $\overline{I3}$, $\overline{I4}$			5	8	pF
C_{IN}	Input Capacitance, $\overline{R}$, $\overline{C}$, $\overline{E1}$, $\overline{E2}$			8	12	pF

Note 3: $C_L = 150$ pF
Note 4: $C_L = 200$ pF } These values represent a range of total stray plus clock capacitance for nine 4k RAMs.
Note 5: $C_L = 250$ pF
Note 6: Typical values are measured at 25°C.
Note 7: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, $V_{BIAS} = 2V$, $V_{CC} = 0V$, and $T_A = 25°C$.

AC Test Circuit and Switching Time Waveforms



Input pulse amplitudes: 3V
Input pulse rise and fall times:
5 ns between 1V and 2V
Measurement points: see waveforms



National Semiconductor

DS1617/DS3617 Bubble Memory Sense Amplifier

General Description

The DS1617 and the DS3617 are bubble memory sense amplifiers that convert low level signals from magneto-resistive detectors of the bubble memory into TTL compatible output levels. Internal functions consist of an input bias circuit, an internally AC coupled amplifier, a high speed precision comparator, two flip-flops, a TRI-STATE® output stage and a power fail detector.

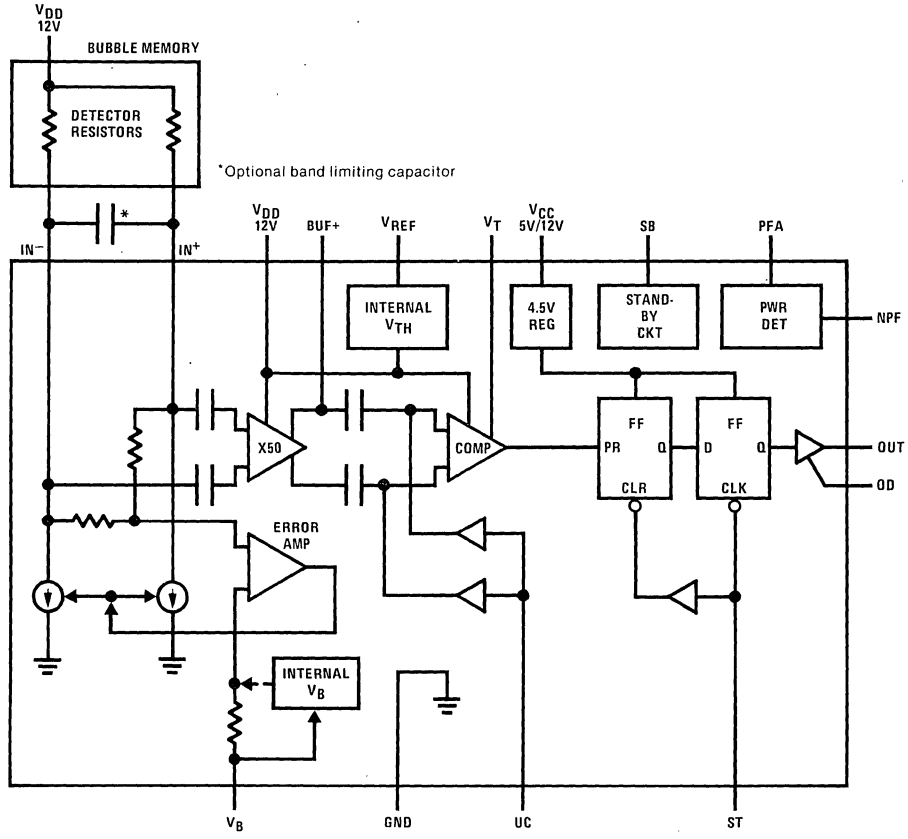
TTL compatible control inputs allow either average-to-peak or the conventional clamp and strobe (peak-to-peak) sensing of the input signal. The threshold voltage and the input bias voltage are externally adjustable allowing compatibility with different types of bubble memories.

Although specifically designed for bubble memory interfacing, they are easily adaptable for any application requiring detection of mV level signals in the 25 kHz to 4 MHz range. Typical application areas include fiber optic receivers, plated wire memory sense amplifiers and pulse discriminators.

Features

- Single 12V or 12V/5V operation
- On-chip adjustable detector bias circuit
- Choice of average-to-peak or clamp and strobe sensing
- Guaranteed tight threshold limits over the specified temperature and supply voltage range
- Threshold externally adjustable over 0 mV to 20 mV range (typical)
- On-chip reference for a 3.2 mV threshold (typical)
- TRI-STATE output
- No offset nulling requirement due to on-chip AC coupling at the input
- Power fail detector with adjustable trip level senses both supplies
- Compatible with a wide range of bubble memories
- Standard 16-pin dual-in-line package

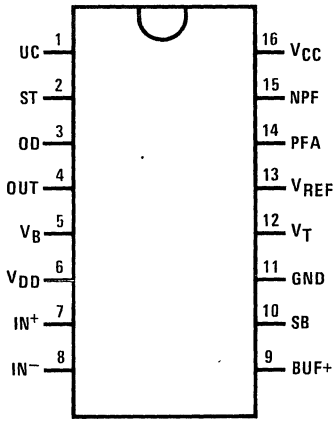
Block Diagram



TRI-STATE® is a registered trademark of National Semiconductor Corp.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS1617J, DS3617J or DS3617N
See NS Package J16A or N16A

Functional Pin Description

ANALOG INPUTS

Differential Analog Inputs (IN^+ and IN^-): These are high impedance inputs for bubble memory detectors. They also provide the bias current to the detectors at a constant DC voltage. The sense-amp threshold is positive with respect to the IN^+ input.

Bias Voltage Input (V_B): When an external DC voltage (between 4V and 8V) is applied to this input, the internal error amplifier will adjust the bias current sources to maintain the average common-mode voltage of IN^+ and IN^- inputs at this value. This input can be connected to V_{DD} to obtain an internally set bias voltage of 7V typical. This voltage is derived on-chip from a resistor divider connected across the V_{DD} supply.

Threshold Adjust Input (V_T): An externally applied DC voltage in the range of 0V to 10V at this input will set the threshold of the sense-amplifier in the 0 mV to 20 mV range. The threshold is linearly related to this voltage.

Power Fail Adjust Input (PFA): The trip voltage of 5V and 12V supplies can be set to a fraction of their nominal values by applying an external reference voltage to this input (see graph). When precise power fail detection is not required this input may be grounded to obtain a trip voltage between 35% and 65% of the nominal supply levels (i.e., 5V and 12V).

ANALOG OUTPUTS

Buffered Bubble Signal Output (BUF+): This is the preamplifier output which is in phase with the IN^+ input. It provides an amplified version of the input differential signal (X25) at a low impedance for monitoring purposes.

Internal Reference for V_T (V_{REF}): This output, when connected to V_T input, provides a threshold of 3.2 mV typical. This voltage is derived on the chip from a potential divider connected across the V_{DD} supply. When V_B is also derived in the same fashion, the threshold will track the amplitude variations of the bubble signal resulting from the V_{DD} supply variations.

DIGITAL INPUTS

Unclamp Input (UC): A logic low level on this input causes clamping of the differential inputs of the comparator to a common voltage. When a logic high level is applied, the inputs are unclamped within a few nanoseconds (5 ns typ). The capacitive coupling of the preamplifier outputs to the inputs of the comparator enables referencing of the threshold to any point on the input waveform by using this input. This pin is shorted to V_{CC} or V_{DD} when the average-to-peak sensing method is used.

Strobe Input (ST): A high-to-low transition of this input causes the transfer of data from an internal latch to the output flip-flop. As long as this input is low the internal latch cannot be set by the comparator. For clamp and strobe sensing, this input can be tied to the unclamp input and used as a single UC/ST control line.

Output Disable (OD): A logic high level at this input causes the data output to go into the high impedance state (TRI-STATE).

Standby Input (SB): When the sense-amp is not in use this input can be used to reduce power consumption. A logic high level applied to this input puts the sense-amp in standby mode and TRI-STATEs the data output pin. The power fail detector circuit is not affected by this input.

DIGITAL OUTPUTS

Data Output (OUT): This output is high for signals crossing the threshold and low for those below the threshold. The data on this pin is valid a short time after the negative transition of the strobe signal and will remain valid until the next negative transition of the strobe signal.

Power Fail Detect Output (NPF): This output goes low when either one or both of the supplies fall below the trip voltage. It will remain low until both of the supplies fall below a minimum level which is 4V for V_{DD} and 2.8V for V_{CC}. It is an open collector output with an internal pull-up of 5 kΩ (typical). The circuit is insensitive to transients on the supplies and will typically reject a 500 ns pulse that goes 1V below the trip voltage.

POWER SUPPLIES

Analog Supply (V_{DD}): 12V.

Digital Supply (V_{CC}): 5V to 12V. This supply is internally regulated to 4.5V and hence can be tied to V_{DD} for single supply operation, but a standard 5V logic supply reduces power consumption and also permits power fail detection of the 5V supply.

Absolute Maximum Ratings (Note 1)

Supply Voltages (V_{DD}, V_{CC})	14V
Input Voltages	
Sense Inputs (IN^+, IN^-)	14V
V_T Input	14V
V_{BIAS} Input (V_B)	14V
Control Inputs (UN, ST, OD, SB)	14V
PFA Input	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1635 mW
Molded Package	1687 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.9 mW/°C above 25°C; derate molded package 13.5 mW/°C above 25°C.

Recommended Operating Conditions

	Min	Max	Units
V_{DD} Supply Voltage			
DS1617	10.8	13.2	V
DS3617	11.4	12.6	V
V_{CC} Supply Voltage			
DS1617	4.5	13.2	V
DS3617	4.75	12.6	V
Temperature (T_A)			
DS1617	−55	125	°C
DS3617	0	70	°C
PFA Input Voltage	0	1.5	V
V_{BIAS} Input Voltage (V_B)	0	13.2	V
V_T Input Voltage (V_T) (Threshold Adjust)	−0.25	10	V
Sense Input Common-Mode Voltage (V_{CM})	4	8	V
Input Bias Current (I_B) (Into IN^+ and IN^- Inputs)	0.1	10	mA

DC Electrical Characteristics (Notes 2 and 3)

	Parameter		Conditions		Min	Typ	Max	Units
ANALOG INPUTS AND OUTPUTS								
V_{IB}	Input Bias Voltage (at IN^+ and IN^- Inputs)		Internal (Note 4)	I_B in mA	Typ −0.15	0.588 V_{DD} + 0.01 I_B	Typ +0.15	V
			External (Note 5)	I_B in mA	Typ −0.1	V_B + 0.01 I_B	Typ +0.1	
$\Delta V_{IB\,(temp)}$	Input Bias Voltage Variation with Temperature (IN^+ and IN^- Inputs)		I_B = 5 mA					
			−55°C < T_A < 125°C (DS1617)			±10		mV
			0°C < T_A < 70°C (DS3617)			±5		mV
I_{VT}	Input Current for V_T Input		V_T = 0V to 5V			−1	−10	μA
I_{VB}	Input Current for V_B Input		V_B = 4V to 8V			−2	−10	μA
V_{REF}	Internal Reference Voltage				0.98 Typ	0.125 V_{DD}	1.02 Typ	V
$\Delta V_{TP\,(temp)}$ (V_{CC}, V_{DD})	Temperature Variation of Power Fail Threshold		Set by V_{PFA} (See Graphs)					
			−55°C < T_A < 125°C (DS1617)			±0.6		%
			0°C < T_A < 70°C (DS3617)			±0.2		%
DIGITAL OUTPUTS (OUT, NPF)								
V_{OH}	Logical "1" Output Voltage	OUT	OD = 0.8V, SB = 0.8V, I_{OH} = −400 μA		2.4	2.8		V
		NPF	I_{OH} = −100 μA		2.4	3.8		
V_{OL}	Logical "0" Output Voltage	OUT	OD = 0.8V, SB = 0.8V, I_{OL} = 10 mA			0.4	0.5	V
		NPF	V_{CC} = 4V, V_{DD} = 10V, V_{PFA} = 1.5V, I_{OL} = 5 mA			0.35	0.5	
I_{OS}	Output Short Circuit Current		V_O = 0V, V_{CC} = V_{DD} = Max					mA
		OUT	OD = 0.8V, SB = 0.8V		−10	−20	−50	
		NPF	V_{PFA} = 0V		−0.5	−1	−1.5	
I_{OD}	TRI-STATE Output Current	OUT Only	OD = 2.0V, SB = 0.8V or OD = 0.8V, SB = 2.0V	V_O = 0.4V			−100	μA
				V_O = 4.0V			100	
I_{PS}	Output Sink Current on NPF Output During Power Fail		V_O = 0.5V, V_{PFA} = 1.5V	V_{CC} = 0V, V_{DD} = 4V	1	6		mA
				V_{CC} = 2.8V, V_{DD} = 0V	1	6		
CONTROL INPUTS (UC, ST, OD, SB)								
V_{IH}	Logical "1" Input Voltage				2			V
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IH}	Logical "1" Input Current		V_{IN} = 4V				20	μA
I_{IL}	Logical "0" Input Current		V_{IN} = 0.4V				−200	μA
POWER SUPPLY CURRENTS								
I_{DDA}	Active V_{DD} Supply Current		SB = 0.8V			25	45	mA
I_{CCA}	Active V_{CC} Supply Current		SB = 0.8V			10	20	
I_{DDS}	Standby V_{DD} Supply Current		SB = 2.0V			12	25	
I_{CCS}	Standby V_{CC} Supply Current		SB = 2.0V			2	4	

AC Electrical Characteristics (Note 2)

Parameter		Conditions		Min	Typ	Max	Units
SENSE INPUT CHARACTERISTICS							
V_{TH}	Differential Input Threshold Voltage	$V_B = 7V$ See *Figure 5* for Test Waveforms		0.97 × Typ − 0.0005	0.00213 × V_T	1.03 × Typ + 0.0005	V
V_{TR}	Threshold Adjustment Range		DS1617	0 to 8	− 0.5 to 20		mV
			DS3617	0 to 10	− 0.5 to 20		mV
f_{BW}	Preamp Bandwidth	@ ±3 dB, $V_B = 7V$, $-55°C < T_A < 125°C$			0.025 to 4		MHz
		@ ±0.1 dB, $V_B = 7V$, $-55°C < T_A < 125°C$			0.1 to 1		
R_{IN}	Differential Input Resistance				150		kΩ
C_{IN}	Differential Input Capacitance				12		pF
$\Delta V_{TH(temp)}$	Threshold Variation with Temperature	$V_{DD} = 12V$	$-55°C < T < 125°C$ (DS1617)		±0.1		mV
			$0°C < T < 70°C$ (DS3617)		±0.05		mV
T_{PC}	Effective Time Constant of Preamp AC Couplings	(From Sense Input to Comparator Inputs) UC = 3V			6		µs
T_{CL}	Clamp Circuit Time Constant	(Time Constant Associated with the Comparator Inputs when UC = 3V)			12		µs
TIMING REQUIREMENTS							
t_d	Delay Time, UC or ST Input High to Sense Input High	*Figure 2*		50			ns
t_s	Data Set-Up Time, Sense Input High to UC or ST Input Low	*Figure 2*		100			ns
t_{pwi}	Minimum Input Pulse Width at Threshold	*Figure 2*		100			ns
t_{pws}	Minimum Strobe Pulse Width	*Figure 2*		30			ns
t_{ON}	Power-Up Time from SB Low to Full Operation					100	µs
t_{OFF}	Power-Down Time from SB High to Reduced Power					1	µs
SWITCHING CHARACTERISTICS							
t_P	ST Input Low to Valid Data at the Output	*Figures 1 and 3*, OD = 0.8V, $C_L = 30$ pF, R1 = 5k, R2 = 1k			30	50	ns
TRI-STATE DELAYS FROM OD TO OUT							
t_{LZ}	Output Low to TRI-STATE	*Figures 1 and 4* $C_L = 15$ pF, R1 = 1k, R2 = 1k			15	35	ns
t_{HZ}	Output High to TRI-STATE				15	35	ns
t_{ZL}	Output TRI-STATE to Active Low				15	40	ns
t_{ZH}	Output TRI-STATE to Active High				15	40	ns

Note 1: "Absolute maximum ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" and "Recommended Operating Conditions" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the supply and temperature range listed in the table of "Recommended Operating Conditions". All typical values are for $V_{CC} = 12V$, $V_{CC} = 5V$ and $T_A = 25°C$ unless otherwise specified.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: V_B pin tied to V_{DD}.

Note 5: V_B pin connected to the external bias voltage.

Example Threshold Calculations

1. Find external voltage V_T to be applied for a 5 mV typical threshold. What is this tolerance of this threshold?

$V_{TH}(typ) = 0.00213 \times V_T = 0.005V$
Therefore, $V_T = 0.005/0.00213 = \mathbf{2.347V}$
$V_{TH}(min) = 0.97 \times 0.005 - 0.0005 = 4.35$ mV
$V_{TH}(max) = 1.03 \times 0.005 + 0.0005 = 5.65$ mV
Hence, $\mathbf{V_{TH} = 5 \pm 0.65}$ mV
and **Tolerance = ± 0.65 mV**

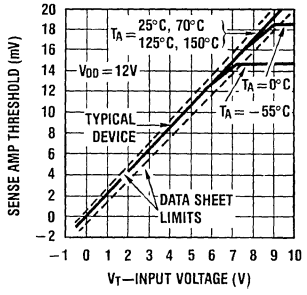
2. Find V_{TH} and its tolerance for $V_{DD} = 12V$ when internal reference (V_{REF}) is used for V_T.

$V_T(typ) = V_{REF}(typ) = 0.125 \times V_{DD} = 1.5V$
$V_T(min) = V_{REF}(min) = 0.98 \times 1.5 = 1.47V$
$V_T(max) = V_{REF}(max) = 1.02 \times 1.5 = 1.53V$
$V_{TH}(typ) = 0.00213 \times V_T(typ) = 3.20$ mV
$V_{TH}(min) = 0.97 \times 0.00213 \times V_T(min) - 0.0005 = 2.54$ mV
$V_{TH}(max) = 1.03 \times 0.00213 \times V_T(max) + 0.0005 = 3.86$ mV
Hence, $\mathbf{V_{TH} = 3.20 \pm 0.66}$ mV

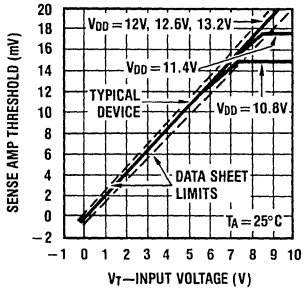
Note. Since V_{REF} is directly related to V_{DD}, the V_{TH} will follow the supply variations. But as long as the input bias voltage V_B is also derived in the same way (i.e., using a potential divider across V_{DD}), the threshold will track the amplitude changes in the bubble detector signal resulting from the V_{DD} supply variations.

Performance Characteristics

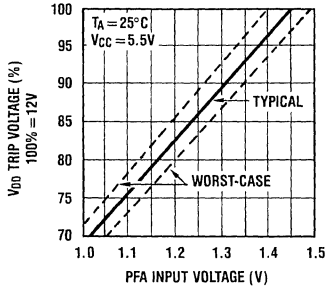
Threshold Transfer Function at Various Temperatures



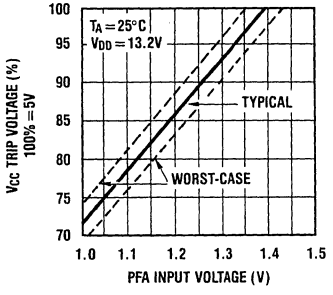
Threshold Transfer Function at Various Supply Voltages



Power Fail Trip Voltage Transfer Function for V_{DD}



Power Fail Trip Voltage Transfer Function for V_{CC}



6

AC Test Circuit and Switching Time Waveforms

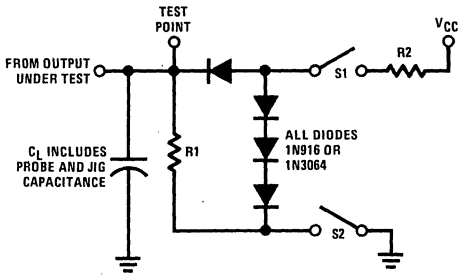
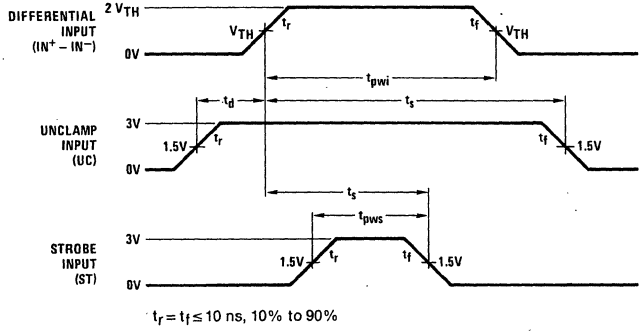


FIGURE 1. Output Load Circuit



$t_r = t_f \leq 10$ ns, 10% to 90%

FIGURE 2. Delay, Set-Up and Hold Times

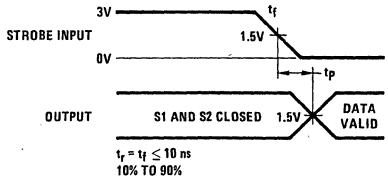
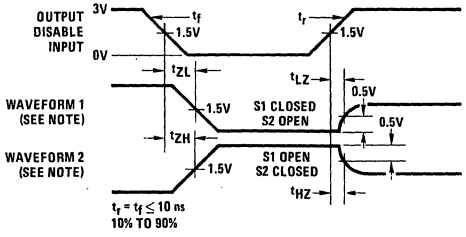
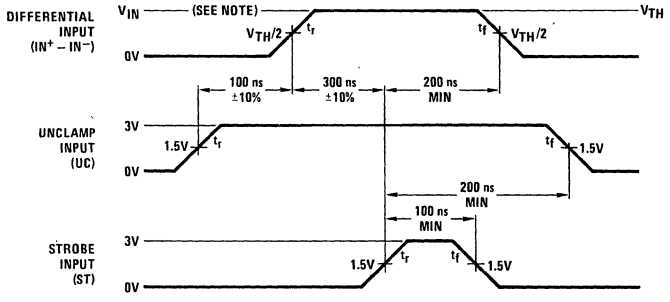


FIGURE 3. Propagation Delay from Strobe Input to Output



Note. Waveform 1 shows the output with internal conditions such that the output is low except when disabled by the output disable input. Waveform 2 shows the output with internal conditions such that the output is high except when disabled by the output disable input.

FIGURE 4. Propagation Delay from Output Disable to Output



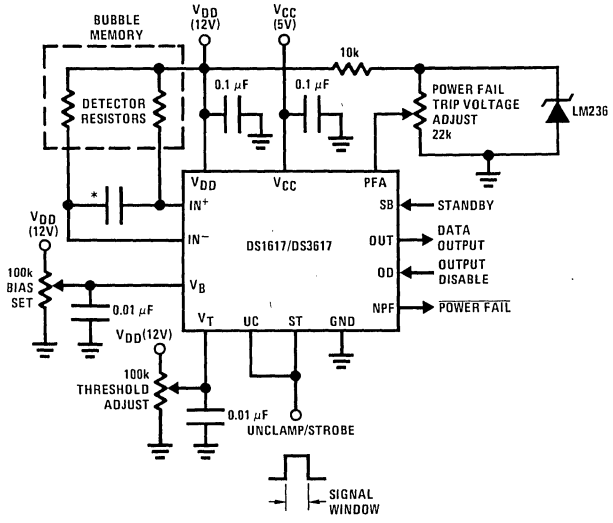
$t_r = t_f \leq 10$ ns, 10% to 90%

Note. To determine the sense amplifier threshold, the input signal amplitude, V_{IN}, is varied around the set threshold value, V_{TH}, while monitoring the OUT pin on a scope. When V_{IN} is close to the threshold, the output will switch between Logic 0 and Logic 1 due to the noise on the input signal. The mid value of the threshold can be determined by adjusting V_{IN} to obtain equal brightness of high (V_{OH}) and low (V_{OL}) level output traces on the scope. In the above set-up, the signal is strobed after a 300 ns delay to allow for any overshoot or transients to settle. This method results in accurate threshold measurement that is relatively independent of input signal rise time. But due to AC coupling of the preamp, with an effective time constant of 6 μs, the signal at the input of the comparator droops by 5% in 300 ns, which has to be accounted for. Hence, $V_{TH} = V_{IN} \times 0.95$.

FIGURE 5. Sense Input Threshold Measurement

Typical Applications

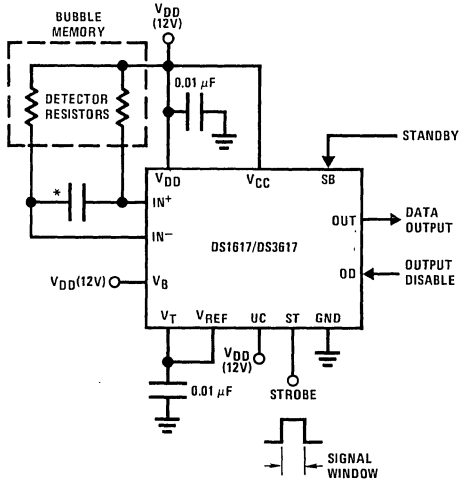
Bubble Memory Sense Amplifier with Adjustable Threshold and Bias Voltage



Note. The control inputs are set up for clamp-strobe or peak-to-peak sensing

*Optional band limiting capacitor

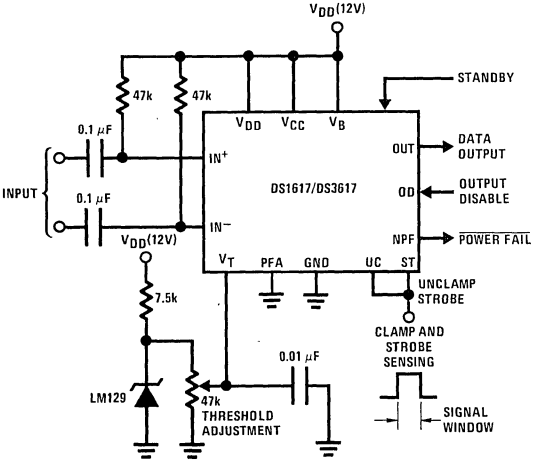
Bubble Memory Sense Amplifier with Internally Set Threshold (3 mV typ) and Input Bias Voltage (7V typ)



Note. The control inputs are set up for average-to-peak sensing

*Optional band limiting capacitor

A General Purpose Precision Sense Amplifier with the Threshold Controlled by an External Reference



National Semiconductor

DS1628/DS3628 Octal TRI-STATE® MOS Drivers

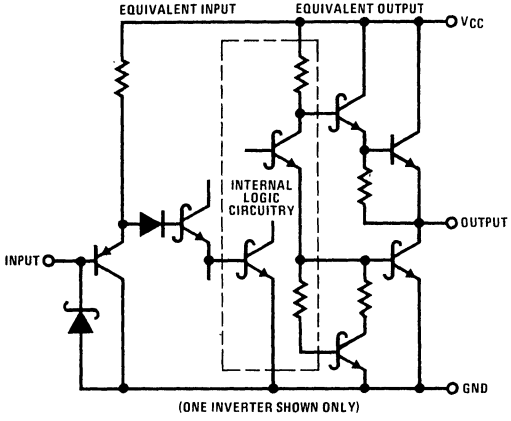
General Description

The DS1628/DS3628 are octal Schottky memory drivers with TRI-STATE® outputs designed to drive high capacitive loads associated with MOS memory systems. The drivers' output (V_{OH}) is specified at 3.4 V to provide additional noise immunity required by MOS inputs. A PNP input structure is employed to minimize input currents. The circuit employs Schottky-clamped transistors for high speed. A NOR gate of two inputs, DIS1 and DIS2, controls the TRI-STATE mode.

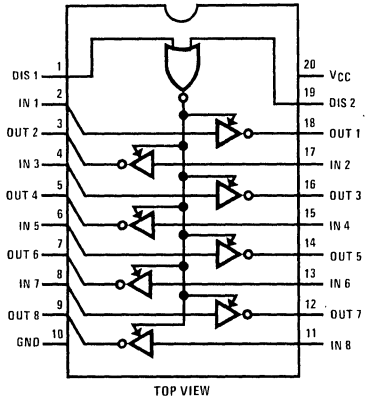
Features

- High speed capabilities
  - typ 5 ns driving 50 pF & 8 ns driving 500 pF
- TRI-STATE outputs
- High V_{OH} (3.4 V min)
- High density
  - eight drivers and two disable controls for TRI-STATE in a 20-pin package
- PNP inputs reduce DC loading on bus lines
- Glitch-free power up/down

Schematic and Connection Diagrams



Dual-In-Line Package



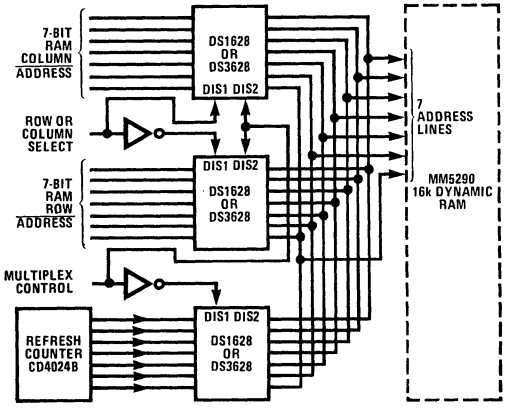
Order Number
DS1628J, DS3628J, DS3628N
See NS Package J20A or N20A

Truth Table

Disable Input		Input	Output
DIS 1	DIS 2		
H	H	X	Z
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

H = high level
L = low level
X = don't care
Z = high impedance (off)

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1667 mW
Molded Package	1832 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 11.1 mW/°C above 25°C; derate molded package 14.7 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1628	−55	+125	°C
DS3628	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 0.5V			−180	−400	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V I_{IN} = −18mA			−0.7	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V I_{OH} = −10μA	DS1628	3.4	4.3		V
			DS3628	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V I_{OL} = 10μA	DS1628		0.25	0.4	V
			DS3628		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V I_{OH} = −1.0mA	DS1628	2.5	3.9		V
			DS3628	2.7	3.9		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V I_{OL} = 20mA	DS1628/DS3628		0.35	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V V_{OUT} = 0V	(Note 6)		−150		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V V_{OUT} = 4.5V	(Note 6)		150		mA
Hi-Z	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V	DIS1 or DIS2 = 2.0V	−40	0.1	40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	One DIS Input = 3.0V All other Inputs = X, Outputs at Hi-Z		90	120	mA
			DIS1, DIS2 = 0V, others = 3V Outputs on		70	100	mA
			All Inputs = 0V, Outputs off		25	50	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 6)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	(Figure 1)	C_L = 50pF		4.0	5.0	ns
			C_L = 500pF		6.5	8.0	ns
t_{S-+}	Storage Delay Positive Edge	(Figure 1)	C_L = 50pF		4.2	5.0	ns
			C_L = 500pF		6.5	8.0	ns
t_F	Fall Time	(Figure 1)	C_L = 50pF		4.2	6.0	ns
			C_L = 500pF		19	22	ns
t_R	Rise Time	(Figure 1)	C_L = 50pF		5.2	7.0	ns
			C_L = 500pF		20	24	ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50pF to GND	R_L = 2kΩ to V_{CC} (Figure 2)		19	25	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50pF to GND	R_L = 2kΩ to GND (Figure 2)		13	20	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50pF to GND	R_L = 400Ω to V_{CC} (Figure 3)		18	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50pF to GND	R_L = 400Ω to GND (Figure 3)		8.5	15	ns

AC Test Circuits and Switching Time Waveforms

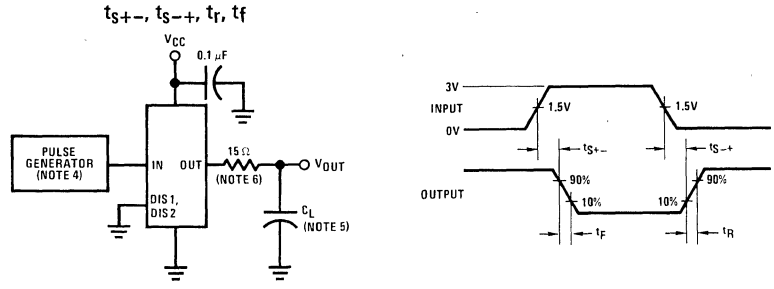
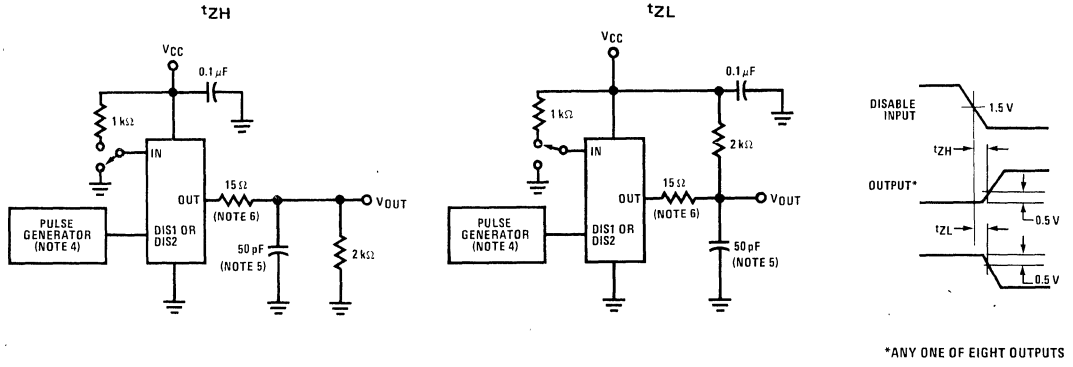


FIGURE 1



*ANY ONE OF EIGHT OUTPUTS

FIGURE 2

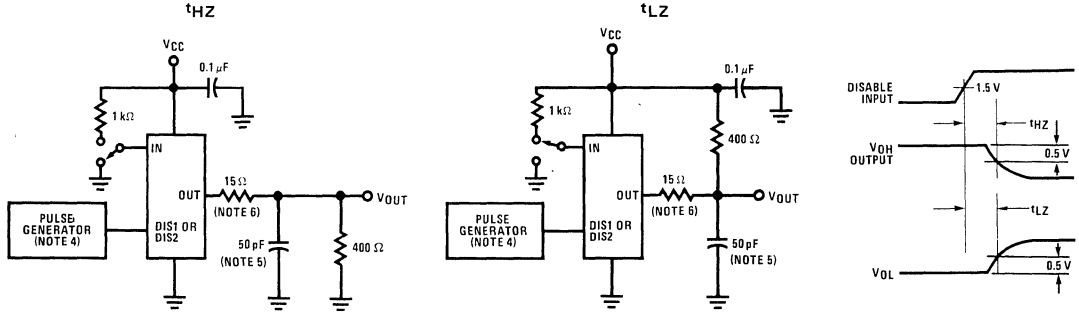


FIGURE 3

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1628 and across the 0°C to +70°C range for the DS3628. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages references to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 5: C_L includes probe and jig capacitance.

Note 6: When measuring output drive current and switching response for the DS1628 and DS3628 a 15 Ω resistor should be placed in series with each output.

National Semiconductor

DS1644/DS3644, DS1674/DS3674 Quad TTL to MOS Clock Drivers

General Description

The DS1644/DS3644 and DS1674/DS3674 are quad bipolar-to-MOS clock drivers with TTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs thereby minimizing input loading.

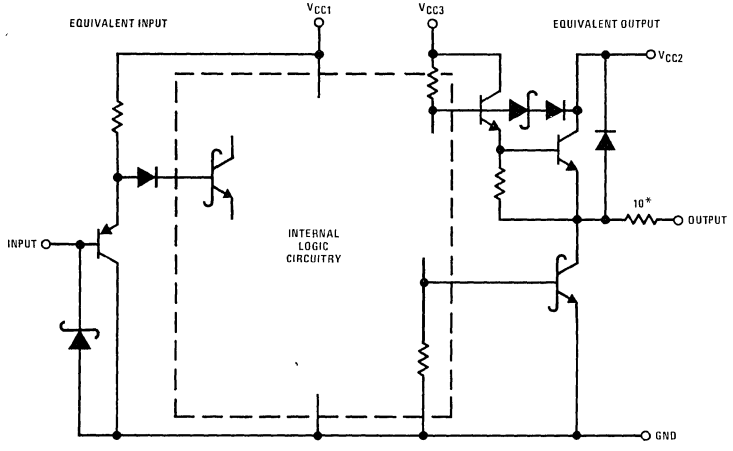
The circuit may be connected to provide a 12V clock output amplitude as required by 4k RAMs or a 5V clock output amplitude as required by 16k RAMs.

The DS1644/DS3644 contains a 10Ω resistor in series with each output to dampen the transients caused by the fast-switching output, while the DS1674/DS3674 has a direct, low impedance output for use with or without an external damping resistor.

Features

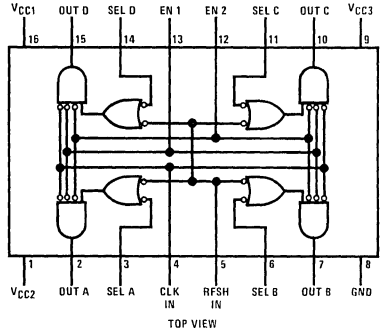
- TTL compatible inputs
- 12V clock or 5V clock driver
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with MC3460 and 3235
- Built-in damping resistors (DS1644/DS3644)

Schematic and Connection Diagrams



* DS1644/DS3644 only

Dual-In-Line Package



TOP VIEW

Order Number DS3644J, DS3674J, DS3644N or DS3674N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	
V_{CC1}	7V
V_{CC2}	13.5V
V_{CC3}	16V
Input Voltage	−1.0V to +7V
Output Voltage	−1.0V to +16V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{CC1}			
DS1644, DS1674	4.5	5.5	V
DS3644, DS3674	4.75	5.25	V
V_{CC2}			
DS1644, DS1674	4.5	13.2	V
DS3644, DS3674	4.75	12.6	V
V_{CC3}			
DS1644, DS1674	V_{CC2}	16.5	V
DS3644, DS3674	V_{CC2}	15.75	V
Temperature, T_A			
DS1644, DS1674	−55	+125	°C
DS3644, DS3674	0	+70	°C

Electrical Characteristics

5V operation, (V_{CC1} = V_{CC2} = 5V, V_{CC3} = 12V); 12V operation, (V_{CC1} = 5V, V_{CC2} = 12V, V_{CC3} = V_{CC2} + (3V ±10%)); DS1644, DS1674, ±10% power supply tolerances; DS3644, DS3674, ±5% power supply tolerances, unless otherwise noted. (Notes 2, 3 and 4).

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = 5.5V	Select Inputs		0.01	10	μA
			All Other Inputs		0.04	40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	Select Inputs		−40	−250	μA
			All Other Inputs		−0.16	−1.0	mA
V_{CD}	Input Clamp Voltage	I_I = −12 mA			−0.8	−1.5	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −1 mA, V_{IL} = 0.8V		V_{CC2}−0.5	V_{CC2}−0.2		V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 5 mA, V_{IH} = 2.0V			0.3	0.5	V
V_{OC}	Output Clamp Voltage	I_{OC} = 5 mA, V_{IL} = 0.8V			V_{CC2}+0.8	V_{CC2}+1.5	V
I_{CCH}	Supply Current Output High	All Inputs V_{IN} = 0V Outputs Open					
	I_{CC1}		V_{CC1} = Max		18	27	mA
	I_{CC2}		12V Operation		−2	−4	mA
	I_{CC3}				2	4	mA
	I_{CC2}		5V Operation		−8	−16	mA
	I_{CC3}				8	16	mA
I_{CCL}	Supply Currents Outputs Low	All Inputs V_{IN} = 5V Outputs Open					
	I_{CC1}		V_{CC1} = 5.25V		25	40	mA
	I_{CC2}		V_{CC2} = 12.6V			3	mA
	I_{CC3}		V_{CC3} = 15.75V		16	25	mA

Switching Characteristics

T_A = 25°C unless otherwise noted, (Note 4), *(Figures 1, 2, 3 and 4)*

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	R_D = 10Ω	C_L = 100 pF		8	11	ns
			C_L = 400 pF		12	16	ns
t_{S-+}	Storage Delay Positive Edge	R_D = 10Ω	C_L = 100 pF		10	13	ns
			C_L = 400 pF		13	16	ns
t_F	Fall Time	R_D = 10Ω	C_L = 100 pF		9	16	ns
			C_L = 400 pF		17	24	ns
t_R	Rise Time	R_D = 10Ω	C_L = 100 pF		8	12	ns
			C_L = 400 pF		13	19	ns
t_{pd0}	Propagation Delay to a Logical "0"	R_D = 10Ω	C_L = 100 pF		17	27	ns
			C_L = 400 pF		29	40	ns
t_{pd1}	Propagation Delay to a Logical "1"	R_D = 10Ω	C_L = 100 pF		18	25	ns
			C_L = 400 pF		26	35	ns

Notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1644, DS1674 and across the 0°C to +70°C range for the DS3644, DS3674. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: For AC measurements, a 10Ω resistor must be placed in series with the output of the DS1674/DS3674. This resistor is internal to the DS1644/DS3644 and need not be added.

AC Test Circuits and Switching Time Waveforms

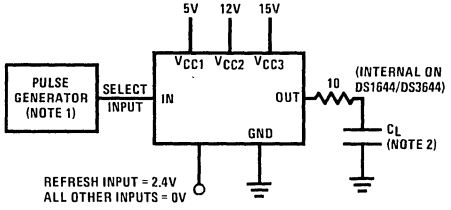


FIGURE 1. 12V Operation

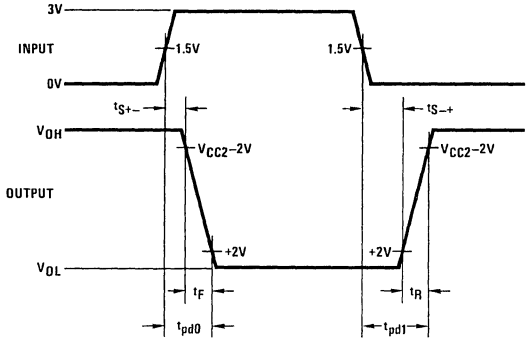


FIGURE 2. 12V Operation

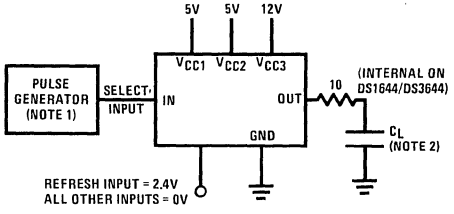


FIGURE 3. 5V Operation

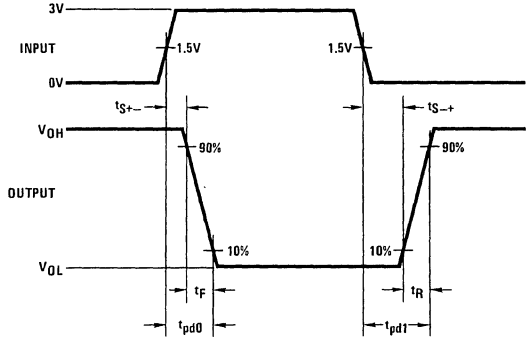


FIGURE 4. 5V Operation

Note 1: The pulse generator has the following characteristics. PPR = 1 MHz, $t_R \leq 10$ ns, Z_{OUT} = 50Ω.

Note 2: C_L includes probe and jig capacitance.

Truth Table

INPUT					OUTPUT
ENABLE 1	ENABLE 2	SELECT INPUT	CLOCK INPUT	REFRESH INPUT	
1	X	X	X	X	0
X	1	X	X	X	0
X	X	X	1	X	0
X	X	1	X	1	0
0	0	0	0	X	1
0	0	X	0	0	1

National Semiconductor

DS1645/DS3645, DS1675/DS3675 Hex TRI-STATE® TTL to MOS Latches/Drivers

General Description

The DS1645/DS3645 and DS1675/DS3675 are hex MOS latches/drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are used to reduce input currents, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE® outputs which allow bus operation.

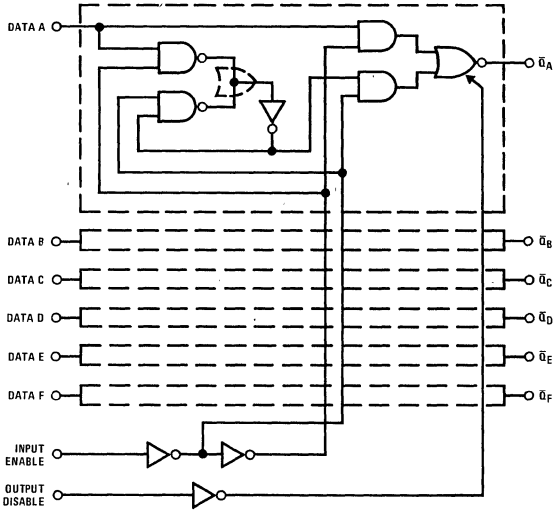
The DS1645/DS3645 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1675/DS3675 has a direct, low impedance output for use with or without an external resistor.

The circuit employs a fall-through-latch which captures the data in parallel with the output, thereby eliminating the delay normally encountered in other latch circuits. The DS1645/DS3645 and DS1675/DS3675 may be used for input address lines or input/output data lines of a MOS memory system.

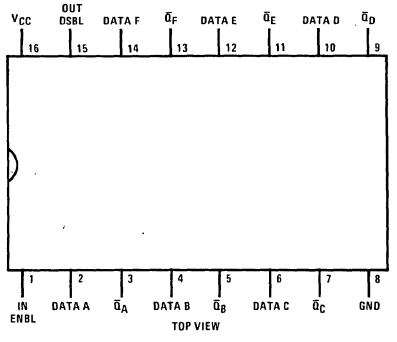
Features

- TTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- TRI-STATE outputs
- Built-in damping resistor (DS1645/DS3645)

Logic and Connection Diagrams



Dual-In-Line Package



Order Number DS1645J, DS1675J, DS3645J, DS3675J, DS3645N or DS3675N
See NS Package J16A or N16A

Truth Table

INPUT ENABLE	OUTPUT DISABLE	DATA	OUTPUT	OPERATION
1	0	1	0	Data Feed-Through
1	0	0	1	Data Feed-Through
0	0	X	Q	Latched to Data Present when Enable Went Low
X	1	X	Hi-Z	High Impedance Output

X = Don't care
Hi-Z = TRI-STATE mode

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1645, DS1675	−55	+125	°C
DS3645, DS3675	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage				2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage						0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5.5V	Enable Inputs			0.1	40	μA
		V_{CC} = 5.5V	Data Inputs			0.2	80	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0.5V	Enable Inputs			−50	−250	μA
		V_{CC} = 5.5V	Data Inputs			−100	−500	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA		DS1645, DS1675	2.7	3.6		V
				DS3645, DS3675	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA		DS1645, DS1675		0.25	0.4	V
				DS3645, DS3675		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA		DS1645	2.4	3.5		V
				DS1675	2.5	3.5		V
				DS3645	2.6	3.5		V
				DS3675	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA		DS1645		0.6	1.1	V
				DS1675		0.4	0.5	V
				DS3645		0.6	1.0	V
				DS3675		0.4	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)				−250		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)				150		mA
I_{HZ}	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, Output Disable = 2.0V			−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Output Disable = 3V All Other Inputs = 0V			60	100	mA
			Input Enable = 3V All Other Inputs = 0V			40	80	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1645 and DS1675 and across the 0°C to +70°C range for the DS3645 and DS3675. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

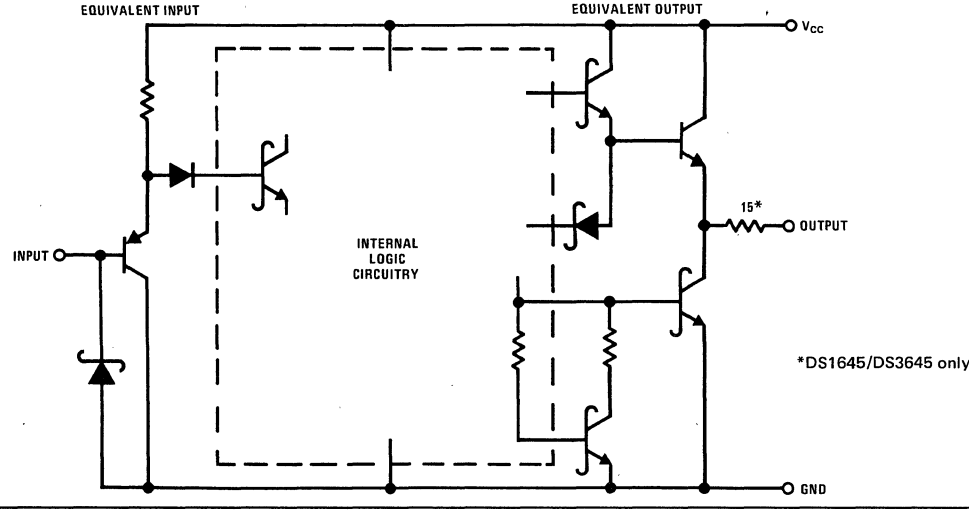
Note 4: When measuring output drive current and switching response for the DS1675 and DS3675 a 15 ohm resistor should be placed in series with each output. This resistor is internal to the DS1645/DS3645, and need not be added.

Switching Characteristics

V_{CC} = 5V, T_A = 25°C, unless otherwise noted. (Note 4)

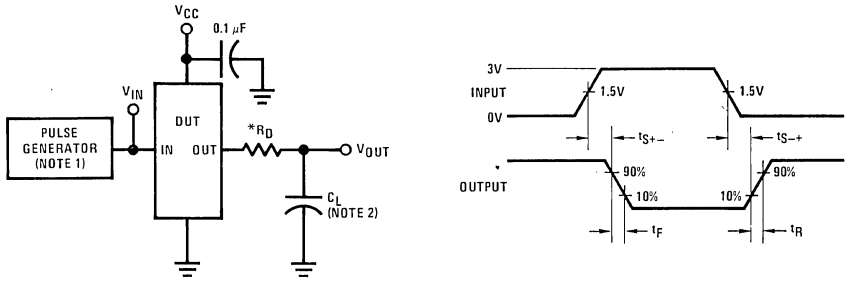
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		8	12	ns
t_{S-+}	Storage Delay Positive Edge	*(Figure 1)*	C_L = 50 pF		6	8	ns
			C_L = 500 pF		9	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		21	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		22	35	ns
t_{SET-UP}	Set-Up Time on Data Input Before Input Enables Goes Low			10	0		ns
t_{HOLD}	Hold Time on Data Input After Input Enable Goes Low			15	5		ns
t_W	Minimum Width of Enable Pulse to Latch Data			20	5		ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to V_{CC}, *(Figure 2)*			10	15	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to Ground, *(Figure 2)*			10	15	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF, R_L = 400Ω to V_{CC}, *(Figure 3)*			16	25	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF, R_L = 400Ω to Ground, *(Figure 3)*			16	25	ns

Schematic Diagram



AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_R, t_F

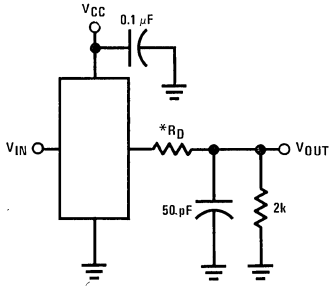


Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

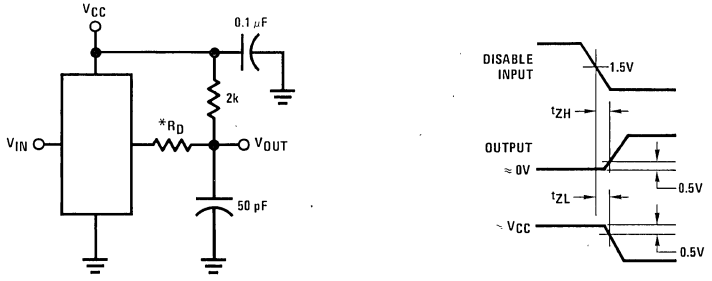
Note 2: C_L includes probe and jig capacitance.

FIGURE 1

t_{ZH}



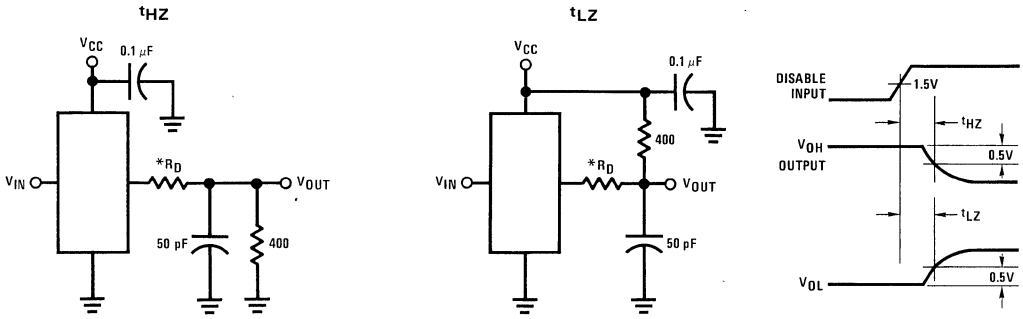
t_{ZL}



*Internal on DS1645 and DS3645

FIGURE 2

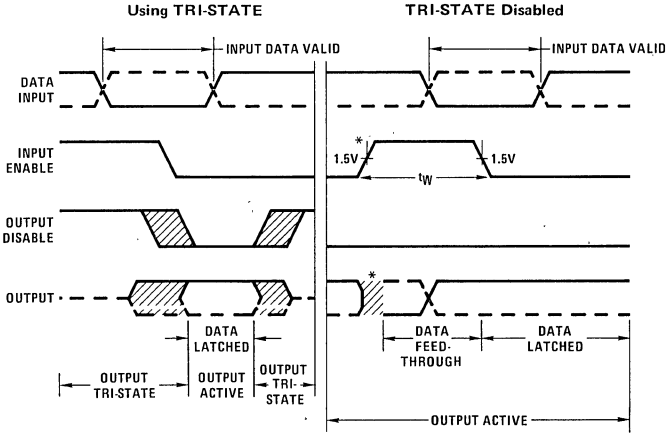
AC Test Circuits and Switching Time Waveforms (Continued)



*Internal on DS1645 and DS3645

FIGURE 3

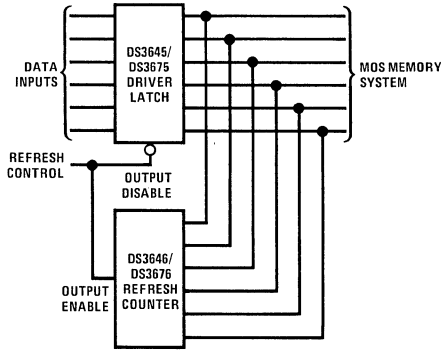
Operating Waveforms



*When the Input Enable makes a positive transition the output will be indeterminate for a short duration. The positive transition of the Input Enable normally occurs during a don't-care timing state at the output.

Typical Applications

The DS3645 and DS3675 latch/driver has TRI-STATE outputs, which allows the outputs to be tied with those of another TRI-STATE driver, such as the DS3646 and DS3676 refresh counter. The DS3645 and DS3675 can be disabled while the alternate driver controls the address lines into the memory system.



National Semiconductor

DS1647/DS3647, DS1677/DS3677, DS16147/DS36147, DS16177/DS36177 Quad TRI-STATE® MOS Memory I/O Registers

General Description

The DS1647/DS3647 series are 4-bit I/O buffer registers intended for use in MOS memory systems. The circuits employ a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. The circuits use Schottky-clamped transistor logic for minimum propagation delay and employ PNP input transistors so that input currents are low, allowing large fan-out to these circuits needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

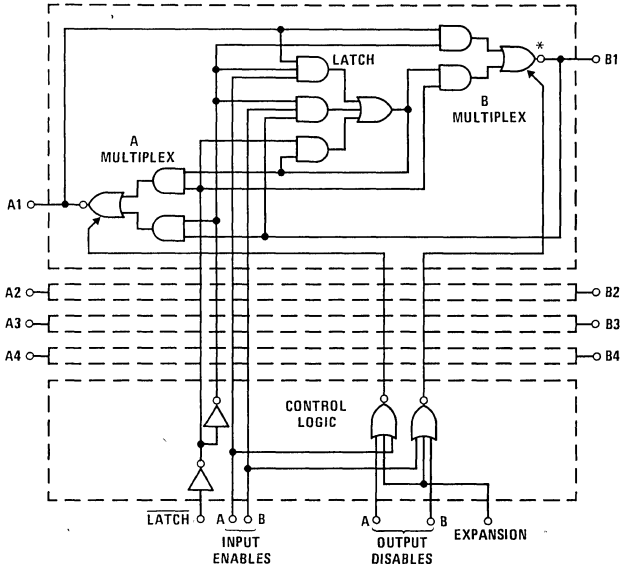
The "B" port outputs in the DS16147/DS36147 and DS16177/DS36177 are open collectors, and in the DS1647/DS3647 and DS1677/DS3677 they are TRI-STATE. The "B" port outputs are also designed for use in bus organized data transmission systems and can sink 80 mA and source −5.2 mA. The "A" port outputs in all four types are TRI-STATE.

Data going from port "A" to port "B" is inverted in the DS1647/DS3647 and DS16147/DS36147 and is not inverted in the DS1677/DS3677 and DS16177/DS36177. Data going from port "B" to port "A" is inverted in all four types.

Features

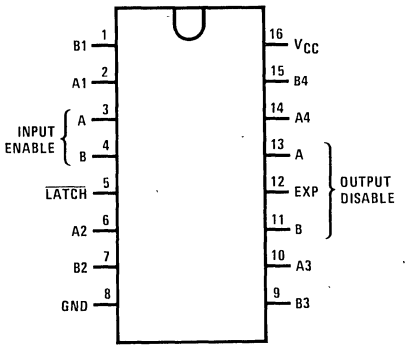
- PNP inputs minimize loading
- Fall-through latch design
- Propagation delay of only 15 ns
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL compatible
- Transmission line driver output

Logic and Connection Diagrams



*Inverting DS1647/DS3647 and DS16147/DS36147 only

Dual-In-Line Package



TOP VIEW

Order Number DS1647D, DS3647D, DS1677D, DS3677D, DS16147D, DS36147D, DS16177D, DS36177D, DS3647N, DS3677N, DS36147N or DS36177N
See NS Package D16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	−1.5V to +7V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1647, DS1677, DS16147, DS16177	−55	+125	°C
DS3647, DS3677, DS36147, DS36177	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logic "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logic "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logic "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V	Latch, Disable Inputs		0.1	40	μA
			Expansion		0.2	80	μA
			A Ports, B Ports		0.2	100	μA
			Enable Inputs		0.4	200	μA
$I_{IN(0)}$	Logic "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V	Latch, Disable Inputs		−25	−250	μA
			Expansion		−50	−500	μA
			A Ports, B Ports		−50	−500	μA
			Enable, Inputs		−0.1	−1.25	mA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.6	−1.2	V
$V_{OL(A)}$	Logic "0" Output Voltage A Ports	V_{CC} = 4.5V, I_{OL} = 20 mA			0.4	0.5	V
$V_{OL(B)}$	Logic "0" Output Voltage B Ports	V_{CC} = 4.5V	I_{OL} = 30 mA		0.3	0.4	V
			I_{OL} = 50 mA		0.4	0.5	V
$V_{OH(A)}$	Logic "1" Output Voltage A Ports	I_{OH} = −1 mA	V_{CC} = 5V	3.0	3.4		V
			V_{CC} = 4.5V	2.5	3.4		V
$V_{OH(B)}$	Logic "1" Output Voltage B Ports	I_{OH} = −5.2 mA, (Note 4)	V_{CC} = 5V	2.9	3.3		V
			V_{CC} = 4.5V	2.4	3.3		V
$I_{OS(A)}$	Output Short-Circuit Current A Port	V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V, (Note 5)		−30	−50	−100	mA
$I_{OS(B)}$	Output Short-Circuit Current B Port	V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V, (Notes 4 and 5)		−30	−60	−100	mA
I_{CC}	Power Supply Current	Exp = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS1647, DS16147		100	110	mA
			DS3647, DS36147		100	140	mA
		Enable A, Latch = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS1647, DS16147		70	80	mA
			DS3647, DS36147		70	105	mA
		Exp = 3V, A Ports = 0V, B Ports Open, All Other Pins = 0V	DS1677, DS16177		105	115	mA
			DS3677, DS36177		105	145	mA
		Enable A, Latch, A Ports = 3V, B Ports Open, All Other Pins = 0V	DS1677, DS16177		75	85	mA
			DS3677, DS36177		75	110	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1647, DS1677, DS16147, DS16177 and across the 0°C to +70°C range for the DS3647, DS3677, DS36147, DS36177. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Not applicable to DS16147/DS36147 or DS16177/DS36177.

Note 5: Only one output at a time should be shorted.

Switching Characteristics (V_{CC} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DATA TRANSFER B PORT TO A PORT, ALL DEVICES						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 280 Ω, *(Figures 1 and 4)*		7.5	15	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 280 Ω, *(Figures 1 and 4)*		6.0	12	ns
A PORT CONTROL FROM OUTPUT DISABLE A INPUT, ALL DEVICES						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 1 and 5)*		13	20	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 1 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 1 and 7)*		10	15	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 1 and 8)*		25	35	ns
DATA TRANSFER A PORT TO B PORT, DS1647/DS3647						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		6.5	12	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		8.0	15	ns
DATA TRANSFER A PORT TO B PORT, DS1677/DS3677						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		12.5	20	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, R_L = 100 Ω, *(Figures 2 and 4)*		8.5	15	ns
DATA TRANSFER A PORT TO B PORT DS16147/DS36147						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, *(Figures 3 and 4)*		18	25	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, *(Figures 3 and 4)*		7.0	15	ns
DATA TRANSFER A PORT TO B PORT, DS16177/DS36177						
t_{pd0}	Propagation Delay to a Logic "0"	C_L = 50 pF, *(Figures 3 and 4)*		13.5	21	ns
t_{pd1}	Propagation Delay to a Logic "1"	C_L = 50 pF, *(Figures 3 and 4)*		18	25	ns
B PORT CONTROL FROM OUTPUT DISABLE B INPUT, DS1647/DS3647, DS1677/DS3677						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 2 and 5)*		15	25	ns
t_{HZ}	Delay to High Impedance from Logic "1"	*(Figures 2 and 6)*		14	20	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 2 and 7)*		10	16	ns
t_{ZH}	Delay to Logic "1" from High Impedance	*(Figures 2 and 8)*		25	35	ns
B PORT CONTROL FROM OUTPUT DISABLE B INPUT, DS16147/DS36147, DS16177/DS36177						
t_{LZ}	Delay to High Impedance from Logic "0"	*(Figures 3 and 5)*		15	25	ns
t_{ZL}	Delay to Logic "0" from High Impedance	*(Figures 3 and 7)*		11	17	ns
LATCH SET-UP AND HOLD TIMES, ALL DEVICES						
t_{SET-UP}	Set-Up Time of Data Input Before $\overline{\text{Latch}}$ Goes Low		10	0		ns
t_{HOLD}	Hold Time of Data Input After $\overline{\text{Latch}}$ Goes Low		0			ns

Product Description

DEVICE NUMBER	B PORT TO A PORT FUNCTION	A PORT TO B PORT FUNCTION	A PORT OUTPUTS	B PORT OUTPUTS
DS1647/DS3647	Inverting	Inverting	TRI-STATE	TRI-STATE
DS1677/DS3677	Inverting	Non-Inverting	TRI-STATE	TRI-STATE
DS16147/DS36147	Inverting	Inverting	TRI-STATE	Open-Collector
DS16177/DS36177	Inverting	Non-Inverting	TRI-STATE	Open-Collector

Truth Table

INPUT ENABLES		$\overline{\text{LATCH}}$	OUTPUT DISABLES		EXPANSION	A PORTS A1–A4 ALL DEVICES	B PORTS B1–B4 DS1647, DS16147 DS3647, DS36147	B PORTS B1–B4 DS1677, DS16177 DS3677, DS36177	COMMENTS
A	B		A	B					
1	0	1	0	0	0	Hi-Z	$\overline{A}$	A	Data In on A, output to B
0	1	1	0	0	0	$\overline{B}$	Hi-Z	Hi-Z	Data In on B, output to A
1	0	0	0	0	0	Hi-Z	$\overline{A}$	A	Data stored which is present when latch goes low
0	1	0	0	0	0	$\overline{B}$	Hi-Z	Hi-Z	Data stored which is present when latch goes low
1	0	X	0	1	0	Hi-Z	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data In on A, may be latched
0	1	X	1	0	0	Hi-Z	Hi-Z	Hi-Z	Both A and B in Hi-Z state, Data In on B, may be latched
X	X	X	X	X	1	Hi-Z	Hi-Z	Hi-Z	Both A and B in Hi-Z state

AC Test Circuits

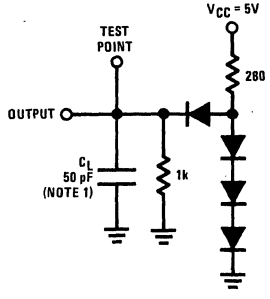


FIGURE 1. A Port Load, All Circuits

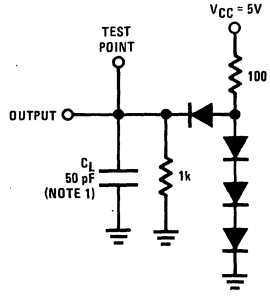


FIGURE 2. B Port Load, DS3647, DS3677

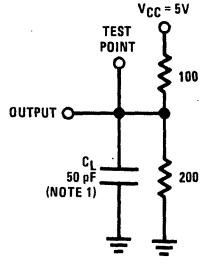
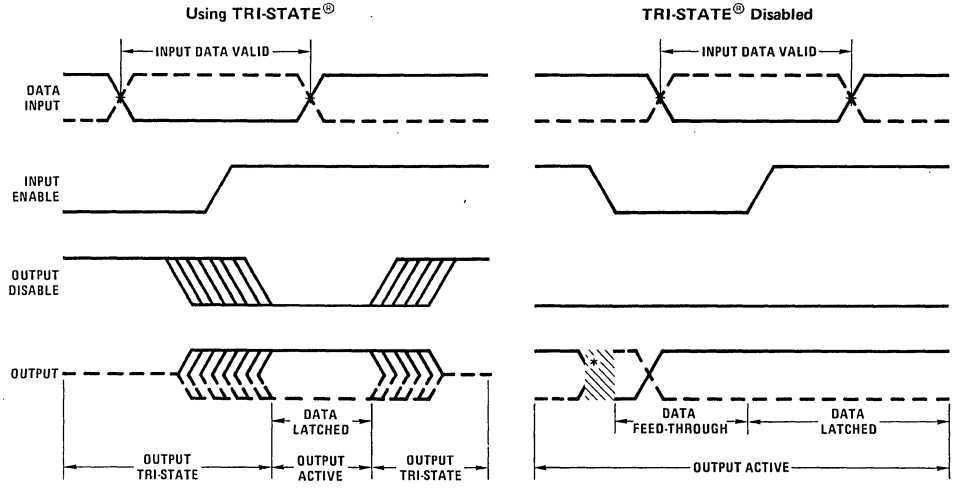


FIGURE 3. B Port Load, DS36147, DS36177

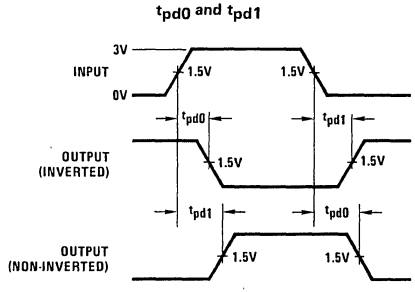
Note 1: C_L includes probe and jig capacitance.

Operating Waveforms



*When the Input Enable makes a negative transition, the output will be indeterminate for a short duration. The negative transition of the Input Enable normally occurs during a don't-care timing state at the output.

Switching Time Waveforms



Input Characteristics: f = 1 MHz, $t_R = t_F \leq 5$ ns (10% to 90% points), duty cycle = 50%, $Z_{OUT} = 50\ \Omega$

FIGURE 4

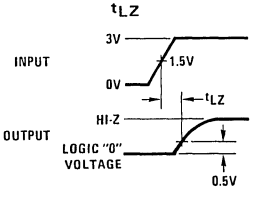


FIGURE 5

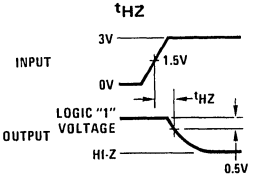


FIGURE 6

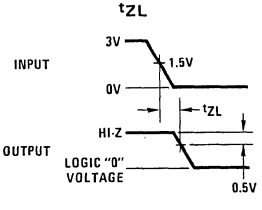


FIGURE 7

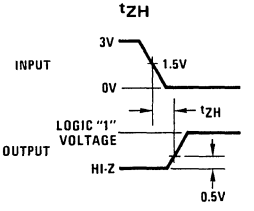
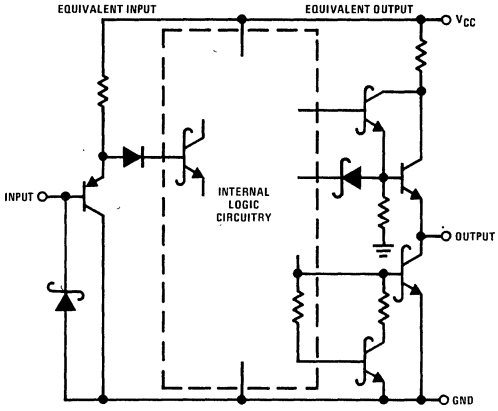


FIGURE 8

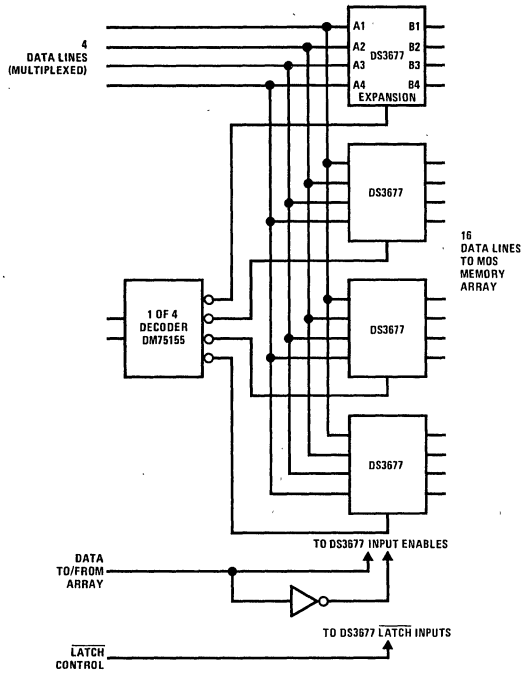
Schematic Diagram



Note. Data pins A1—A4 and B1—B4 consist of an input and an output tied together.

Typical Application

The diagram below shows how the DS3677 can be used as a register capable of multiplexing data lines.



National Semiconductor

DS1648/DS3648, DS1678/DS3678 TRI-STATE® TTL to MOS Multiplexers/Drivers

General Description

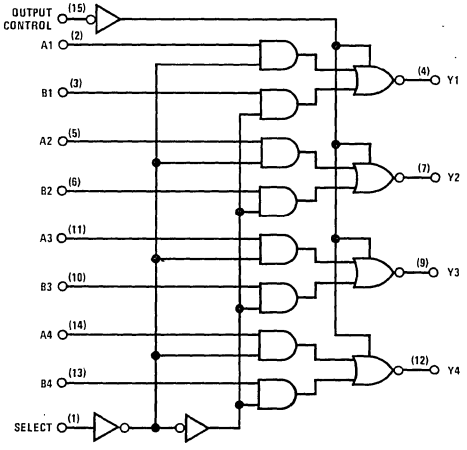
The DS1648/DS3648 and DS1678/DS3678 are quad 2-input multiplexers with TRI-STATE outputs designed to drive the large capacitive loads (up to 500 pF) associated with MOS memory systems. A PNP input structure is employed to minimize input currents so that driver loading in large memory systems is reduced. The circuit employs Schottky-clamped transistors for high speed and TRI-STATE outputs for bus operation.

The DS1648/DS3648 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1678/DS3678 has a direct, low impedance output for use with or without an external resistor.

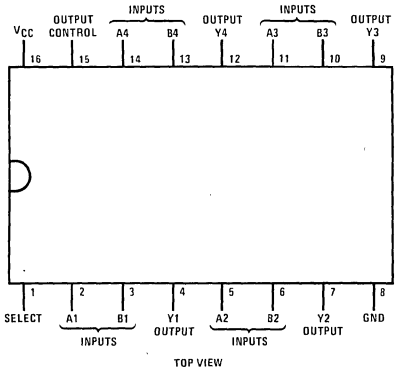
Features

- TRI-STATE outputs interface directly with system bus
- Schottky-clamped for better ac performance
- PNP inputs to minimize input loading
- TTL compatible
- High-speed capacitive load drivers
- Built-in damping resistor (DS1648/DS3648 only)

Logic and Connection Diagrams

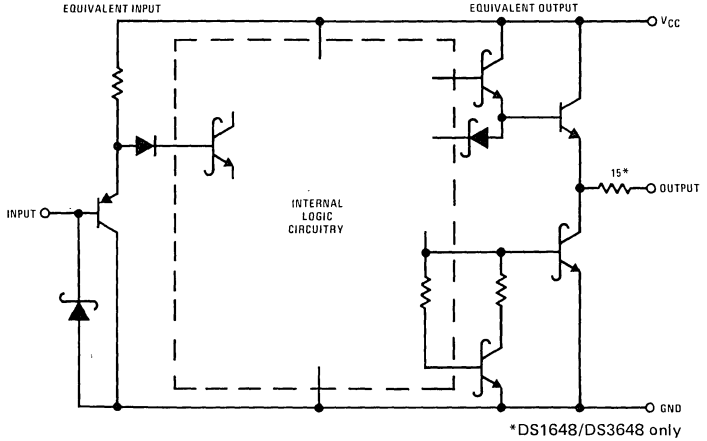


Dual-In-Line Package



Order Number DS1648J, DS3648J, DS1678J, DS3678J, DS3648N or DS3678N
See NS Package J16A or N16A

Schematic Diagram



*DS1648/DS3648 only

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1648, DS1678	−55	+125	°C
DS3648, DS3678	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = −10 μA	DS1648/DS1678	2.7	3.6		V
			DS3648/DS3678	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 10 μA	DS1648/DS1678		0.25	0.4	V
			DS3648/DS3678		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1648	2.4	3.5		V
			DS1678	2.5	3.5		V
			DS3648	2.6	3.5		V
			DS3678	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1648		0.6	1.1	V
			DS1678		0.4	0.5	V
			DS3648		0.6	1.0	V
			DS3678		0.4	0.5	V
I_{1D}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)			−250		mA
I_{0D}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)			150		mA
$I_{Hi\text{-}Z}$	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, Output Control = 2.0V		−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Output Control = 3V, All Other Inputs at 0V		42	60	mA
			All Inputs at 0V		20	32	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1648 and DS1678 and across the 0°C to +70°C range for the DS3648 and DS3678. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

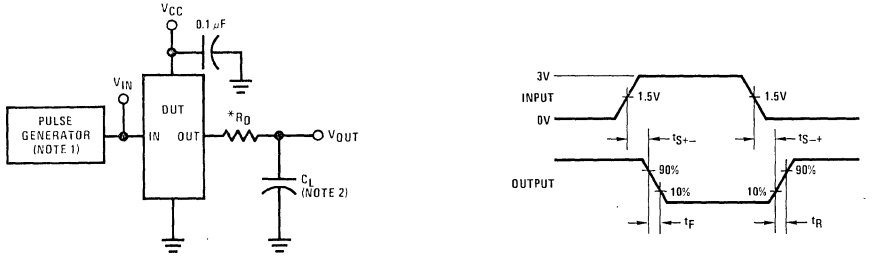
Note 4: When measuring output drive current and switching response for the DS1678 and DS3678 a 15 Ω resistor should be placed in series with each output. This resistor is internal to the DS1648/DS3648 and need not be added.

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		5	7	ns
			C_L = 500 pF		9	12	ns
t_{S-+}	Storage Delay Positive Edge	*(Figure 1)*	C_L = 50 pF		6	8	ns
			C_L = 500 pF		9	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		22	35	ns
t_{ZL}	Delay from Output Control Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to V_{CC}, *(Figure 2)*			10	15	ns
t_{ZH}	Delay from Output Control Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to Gnd, *(Figure 2)*			8	15	ns
t_{LZ}	Delay from Output Control Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF, R_L = 400 Ω to V_{CC}, *(Figure 3)*			15	25	ns
t_{HZ}	Delay from Output Control Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF, R_L = 400 Ω to Gnd, *(Figure 3)*			10	25	ns
t_{S+-}	Propagation Delay to Logical "0" Transition When Select Selects A	C_L = 50 pF, *(Figure 1)*			12	15	ns
t_{S-+}	Propagation Delay to Logical "1" Transition When Select Selects A	C_L = 50 pF, *(Figure 1)*			14	17	ns
t_{S+-}	Propagation Delay to Logical "0" Transition When Select Selects B	C_L = 50 pF, *(Figure 1)*			16	20	ns
t_{S-+}	Propagation Delay to Logical "1" Transition When Select Selects B	C_L = 50 pF, *(Figure 1)*			14	20	ns

AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_R, t_F

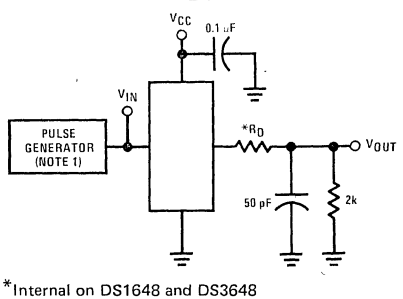


Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

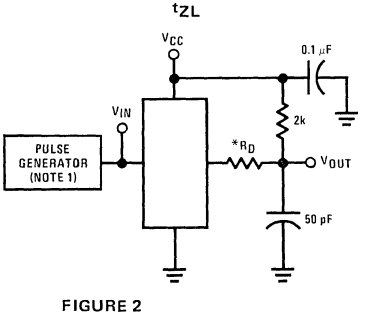
Note 2: C_L includes probe and jig capacitance.

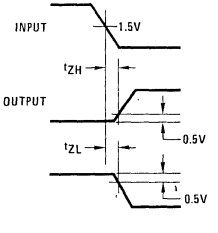
FIGURE 1

t_{ZH}



t_{ZL}

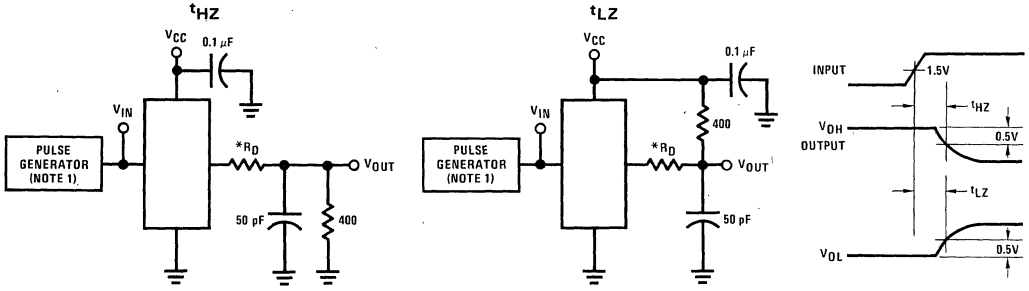




*Internal on DS1648 and DS3648

FIGURE 2

AC Test Circuits and Switching Time Waveforms (Continued)



*Internal on DS1648 and DS3648

FIGURE 3

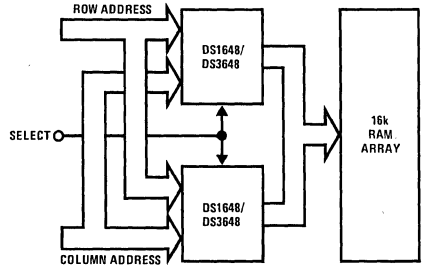
Truth Table

OUTPUT CONTROL	INPUTS			OUTPUTS
	SELECT	A	B	
H	X	X	X	Hi-Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High level
L = Low level
X = Don't care
Hi-Z = TRI-STATE mode

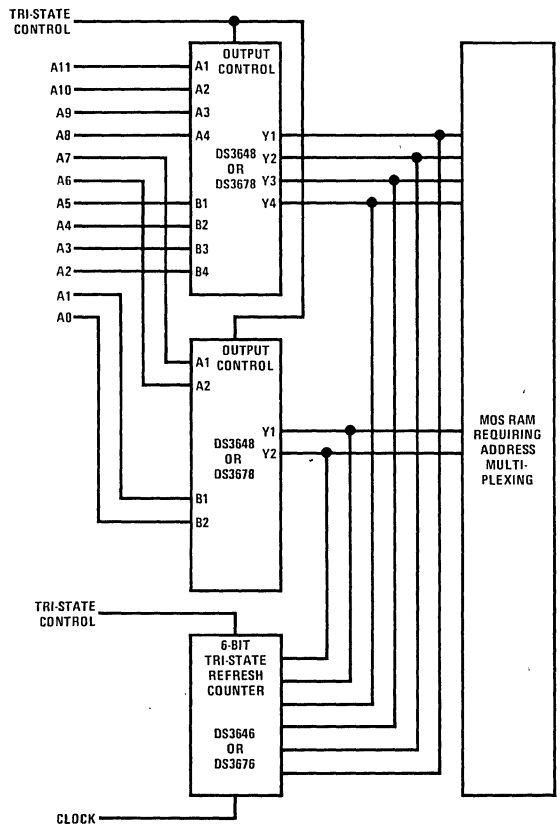
Typical Applications

Addressing 16k RAM

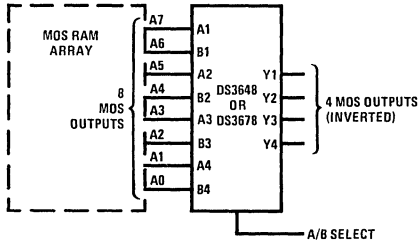


Typical Applications (Continued)

Refreshing Using TRI-STATE Counter



2:1 Multiplexing of RAM Outputs



National Semiconductor

DS1649/DS3649, DS1679/DS3679 Hex TRI-STATE® TTL to MOS Drivers

General Description

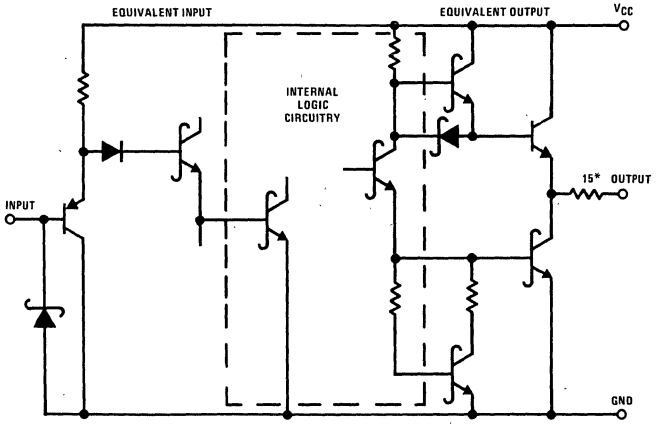
The DS1649/DS3649 and DS1679/DS3679 are Hex TRI-STATE MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs for bus operation.

The DS1649/DS3649 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 30 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15 Ω damping resistor (DS1649/DS3649)
- Same pin-out as DM8096 and DM74366

Schematic Diagram



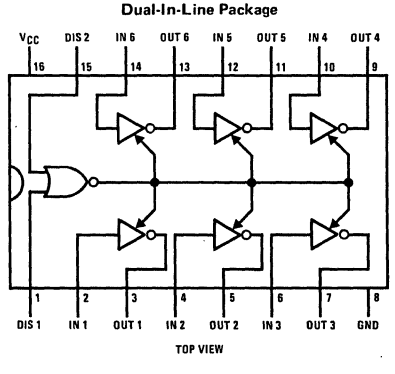
*DS1649/DS3649 only

Truth Table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	Hi-Z
1	0	X	Hi-Z
1	1	X	Hi-Z

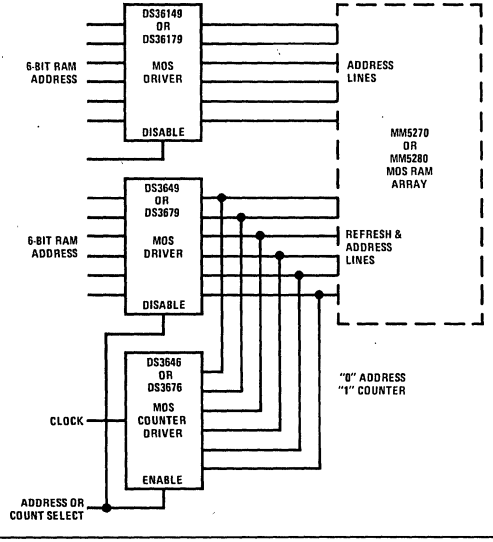
X = Don't care
Hi-Z = TRI-STATE mode

Connection Diagram



Order Number DS1649J, DS3649J, DS1679J, DS3679J, DS3649N or DS3679N
See NS Package J16A or N16A

Typical Application



Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1649, DS1679	−55	+125	°C
DS3649, DS3679	0	+70	°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Electrical Characteristics (Note 2 and 3)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage				2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage						0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V	V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V	V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V	I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V	I_{OH} = −10 μA	DS1649/DS1679	2.7	3.6		V
				DS3649/DS3679	2.8	3.6		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V	I_{OL} = 10 μA	DS1649/DS1679		0.25	0.4	V
				DS3649/DS3679		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V	I_{OH} = −1.0 mA	DS1649	2.4	3.5		V
				DS1679	2.5	3.5		V
				DS3649	2.6	3.5		V
				DS3679	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V	I_{OL} = 20 mA	DS1649		0.6	1.1	V
				DS1679		0.4	0.5	V
				DS3649		0.6	1.0	V
				DS3679		0.4	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V	V_{OUT} = 0V (Note 4)			−250		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V	V_{OUT} = 4.5V (Note 4)			150		mA
Hi-Z	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V DIS1 or DIS2 = 2.0V			−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	One DIS Input = 3.0V All Other Inputs = X			42	75	mA
			All Inputs = 0V			11	20	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		7.5	12	ns
t_{S-+}	Storage Delay Position Edge	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		8	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		21	35	ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF to Gnd	R_L = 2 kΩ to V_{CC} *(Figure 2)*		10	15	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF to Gnd	R_L = 2 kΩ to Gnd *(Figure 2)*		8	15	
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF to Gnd	R_L = 400 Ω to V_{CC} *(Figure 3)*		15	25	
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF to Gnd	R_L = 400 Ω to Gnd *(Figure 3)*		10	25	ns

Notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1649 and DS1679 and across the 0°C to +70°C range for the DS3649 and DS3679. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1679 and DS3679 a 15 Ω resistor should be placed in series with each output. This resistor is internal to the DS1649/DS3649 and need not be added.

AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_R, t_F

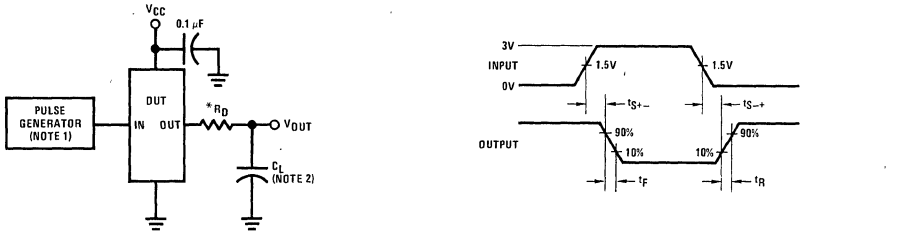


FIGURE 1

t_{ZH} t_{ZL}

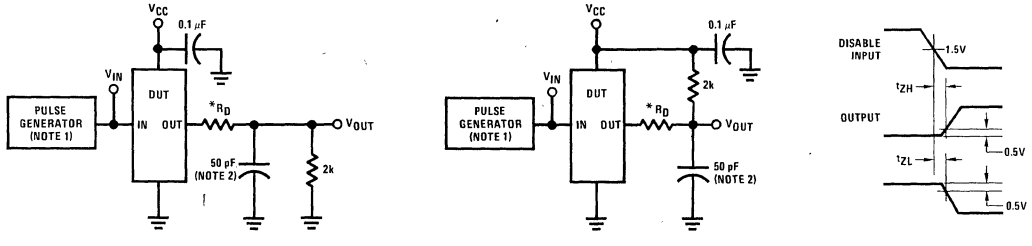


FIGURE 2

t_{HZ} t_{LZ}

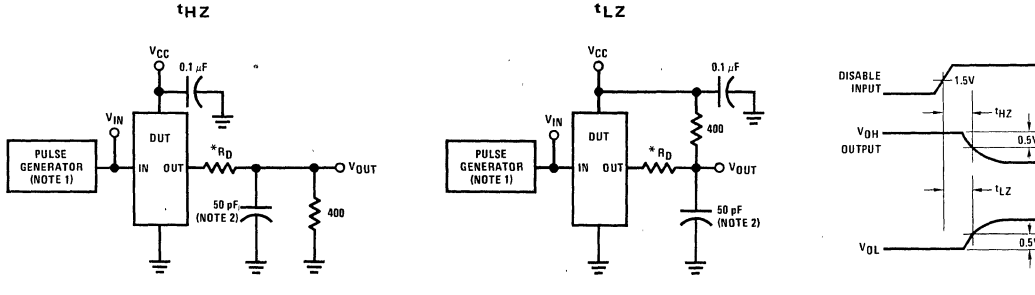


FIGURE 3

*Internal on DS1649 and DS3649

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 2: C_L includes probe and jig capacitance.

National Semiconductor

DS1651/DS3651, DS1653/DS3653 Quad High Speed MOS Sense Amplifiers

General Description

The DS1651/DS3651 and DS1653/DS3653 are TTL compatible high speed circuits intended for sensing in a broad range of MOS memory system applications. Switching speeds have been enhanced over conventional sense amplifiers by application of Schottky technology, and TRI-STATE® strobing is incorporated, offering a high impedance output state for bused organization.

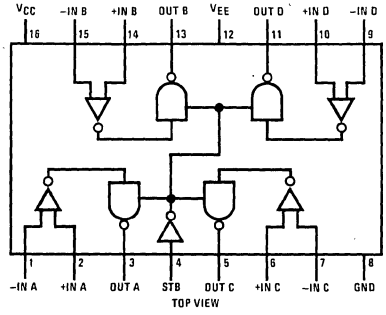
The DS1651/DS3651 has active pull-up outputs, and the DS1653/DS3653 offers open collector outputs providing implied "AND" operations.

Features

- High speed
- TTL compatible
- Input sensitivity — ±7 mV
- TRI-STATE outputs for high speed buses
- Standard supply voltages — ±5V
- Pin and function compatible with MC3430 and MC3432

Connection Diagram

Dual-In-Line Package



Order Number DS1651J, DS1653J, DS3651J, DS3653J, DS3651N or DS3653N
See NS Package J16A or N16A

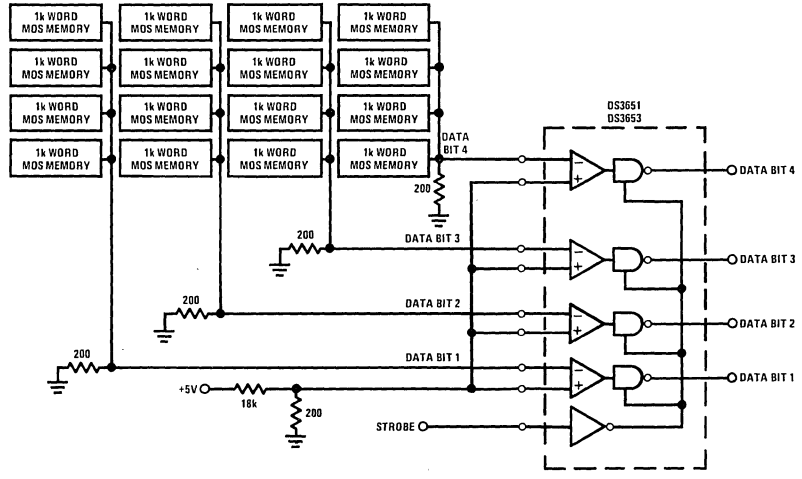
Truth Table

INPUT	STROBE	OUTPUT	
		DS3651	DS3653
$V_{ID} \geq 7$ mV $T_A = 0°C$ to $+70°C$	L	H	Open
	H	Open	Open
-7 mV $\leq V_{ID} \leq +7$ mV $T_A = 0°C$ to $+70°C$	L	X	X
	H	Open	Open
$V_{ID} \leq -7$ mV $T_A = 0°C$ to $+70°C$	L	L	L
	H	Open	Open

L = Low logic state
H = High logic state
Open = TRI-STATE
X = Indeterminate state

Typical Applications

A Typical MOS Memory Sensing Application for a 4k word by 4-bit memory arrangement employing 1103 type memory devices



Note. Only 4 devices are required for a 4k word by 16-bit memory system.

Absolute Maximum Ratings

(Note 1)

Power Supply Voltages
- V_{CC} +7 V_{DC}
- V_{EE} −7 V_{DC}

Differential-Mode Input Signal Voltage Range, V_{IDR} ±6 V_{DC}

Common-Mode Input Voltage Range, V_{ICR} ±5 V_{DC}

Strobe Input Voltage, $V_{I(S)}$ 5.5 V_{DC}

Storage Temperature Range −65°C to +150°C

Maximum Power Dissipation* at 25°C
- Cavity Package 1509 mW
- Molded Package 1476 mW

Lead Temperature (Soldering, 10 seconds) 300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS1651, DS1653	4.5	5.5	V_{DC}
DS3651, DS3653	4.75	5.25	V_{DC}
Supply Voltage (V_{EE})			
DS1651, DS1653	−4.5	−5.5	V_{DC}
DS3651, DS3653	−4.75	−5.25	V_{DC}
Operating Temperature (T_A)			
DS1651, DS1653	−55	+125	°C
DS3651, DS3653	0	+70	°C
Output Load Current, (I_{OL})		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	−5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range (V_{ICR})	−3.0	+3.0	V_{DC}
Input Voltage Range (Any Input to GND), (V_{IR})	−5.0	+3.0	V_{DC}

Electrical Characteristics

V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, Min ≤ T_A ≤ Max, unless otherwise noted (Notes 2 and 3)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IS}	Input Sensitivity, (Note 5) (Common-Mode Voltage Range = −3V ≤ V_{IN} ≤ 3V)	Min ≤ V_{CC} ≤ Max Min ≥ V_{EE} ≥ Max					±7.0	mV
V_{IO}	Input Offset Voltage					2		mV
I_{IB}	Input Bias Current	V_{CC} = Max, V_{EE} = Max					20	µA
I_{IO}	Input Offset Current					0.5		µA
$V_{IL(S)}$	Strobe Input Voltage (Low State)						0.8	V
$V_{IH(S)}$	Strobe Input Voltage (High State)				2			V
$I_{IL(S)}$	Strobe Current (Low State)	V_{CC} = Max, V_{EE} = Max, V_{IN} = 0.4V					−1.6	mA
$I_{IH(S)}$	Strobe Current (High State)	V_{CC} = Max, V_{EE} = Max	V_{IN} = 2.4V	DS3651, DS3653			40	µA
			V_{IN} = V_{CC}				1	mA
			V_{IN} = 2.4V	DS1651, DS1653			100	µA
			V_{IN} = V_{CC}				1	mA
V_{OH}	Output Voltage (High State)	V_{CC} = Min, V_{EE} = Min	I_O = −400 µA	DS1651/DS3651	2.4			V
V_{OL}	Output Voltage (Low State)	V_{CC} = Min, V_{EE} = Min	I_O = 16 mA	DS3651, DS3653			0.45	V
				DS1651, DS1653			0.50	
I_{CEX}	Output Leakage Current	V_{CC} = Min, V_{EE} = Min	V_O = Max	DS1653/DS3653			250	µA
I_{OS}	Output Current Short Circuit	V_{CC} = Max, V_{EE} = Max, (Note 4)		DS1651/DS3651	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	V_{CC} = Max, V_{EE} = Max		DS3651			40	µA
				DS1651			100	µA
I_{CC}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				45	60	mA
I_{EE}	High Logic Level Supply Current	V_{CC} = Max, V_{EE} = Max				−17	−30	mA

Switching Characteristics

V_{CC} = 5 V_{DC}, V_{EE} = −5 V_{DC}, T_A = 25°C unless otherwise noted.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, *(Figure 3)*	DS1651/ DS3651		23	45	ns
			DS1653/ DS3653		22	50	ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)	5 mV + V_{IS}, *(Figure 3)*	DS1651/ DS3651		22	55	ns
			DS1653/ DS3653		24	65	ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	*(Figure 1)*	DS1651/ DS3651		16	21	ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)	*(Figure 1)*	DS1651/ DS3651		7	18	ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)	*(Figure 1)*	DS1651/ DS3651		19	27	ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)	*(Figure 1)*	DS1651/ DS3651		14	29	ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	*(Figure 2)*	DS1653/ DS3653		16	25	ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)	*(Figure 2)*	DS1653/ DS3653		13	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

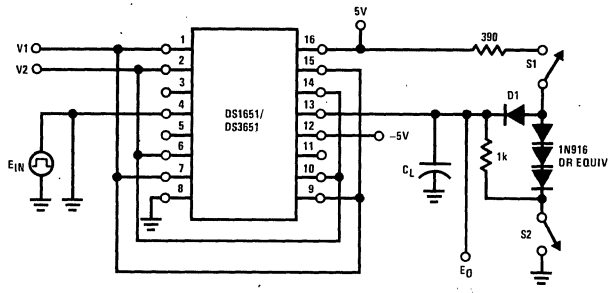
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3651, DS3653 and across the −55°C to +125°C range for the DS1651, DS1653. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{EE} = −5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with sense amplifiers is, what is the minimum differential input voltage required at the sense amplifier input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS1651, DS1653 and DS3651, DS3653 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents, and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200Ω at each input.

AC Test Circuits and Switching Time Waveforms



Note. Output of channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz
Duty cycle = 50%

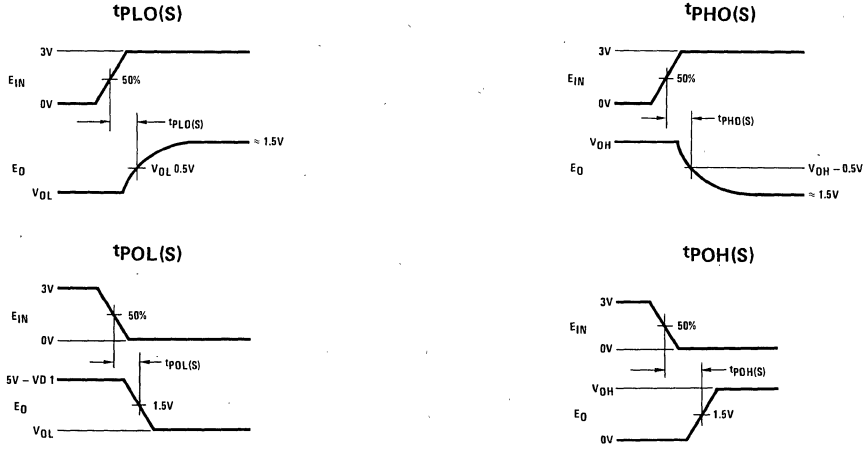
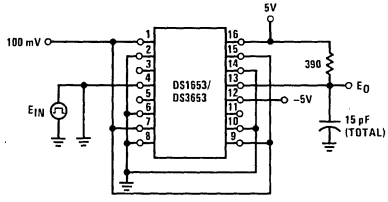
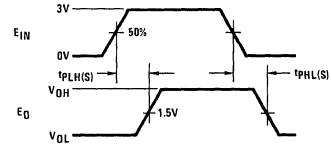


FIGURE 1. Strobe Propagation Delay $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHL(S)}$ and $t_{POH(S)}$

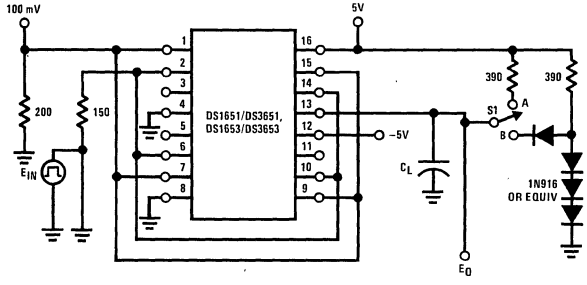


Note. Output of channel B shown under test, other channels are tested similarly.

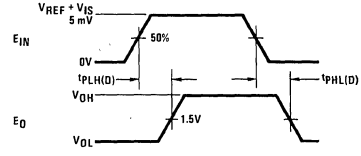


Note. E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz, duty cycle = 500 ns

FIGURE 2. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$



Note. Output of channel B shown under test, other channels are tested similarly.
S1 at "A" for DS1653/DS3653, C_L = 15 pF total for DS1653/DS3653
S1 at "B" for DS1651/DS3651, C_L = 50 pF total for DS1651/DS3651

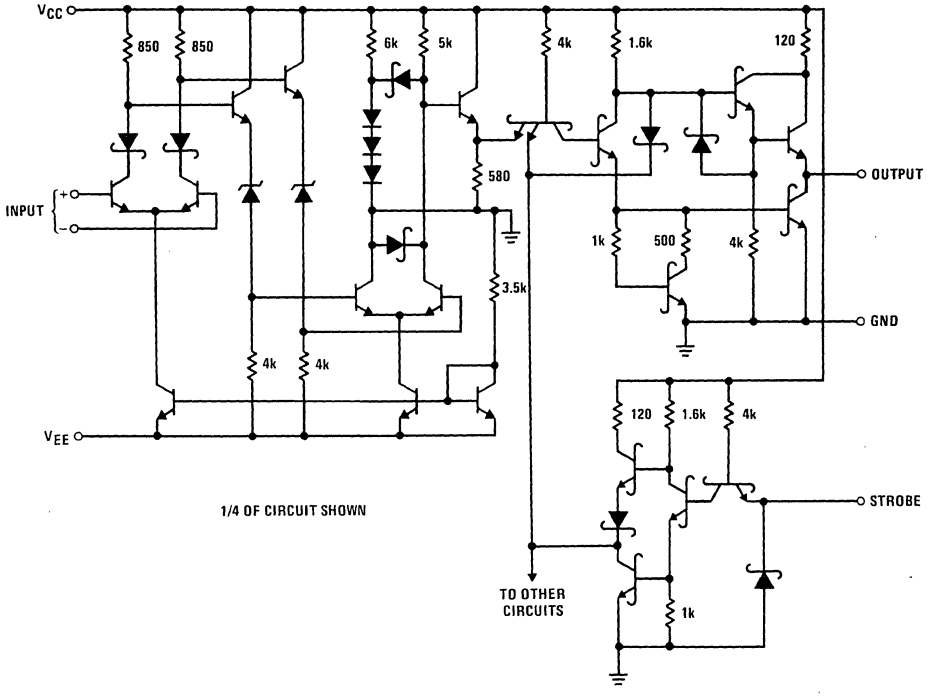


E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1 MHz, duty cycle = 500 ns

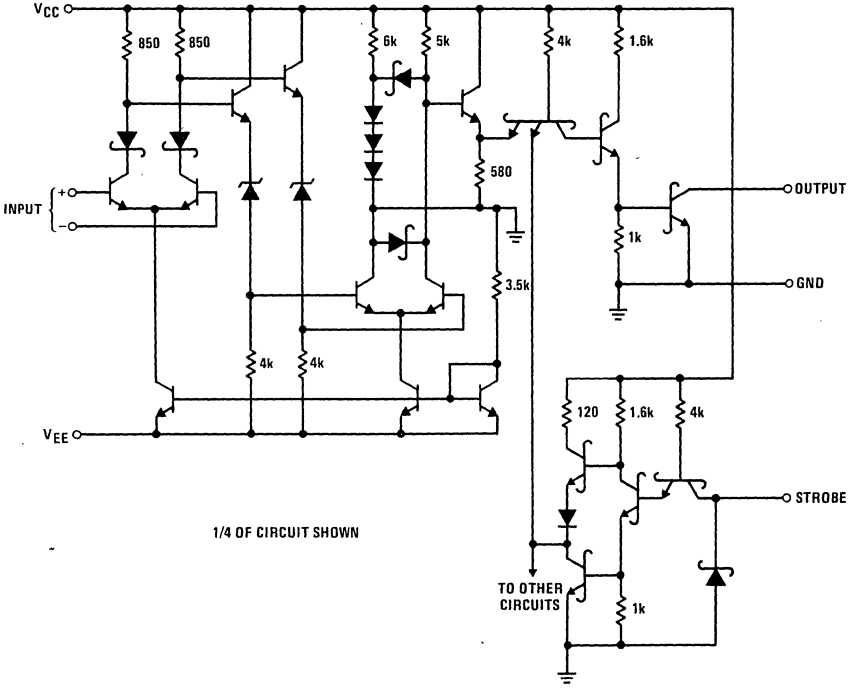
FIGURE 3. Differential Input Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$

Schematic Diagrams

DS1651/DS3651

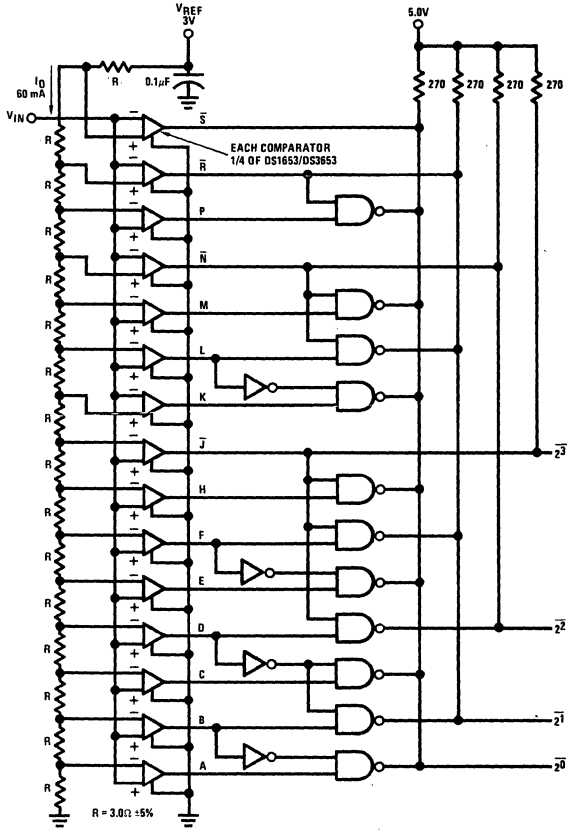


DS1653/DS3653



Typical Applications (Continued)

4-Bit Parallel A/D Converter



$\overline{2^0} = (\overline{A} + B)\ (\overline{C} + D)\ (\overline{E} + F)\ (\overline{H} + J)\ (\overline{K} + L)\ (\overline{M} + N)\ (\overline{P} + R)\ (\overline{S})$

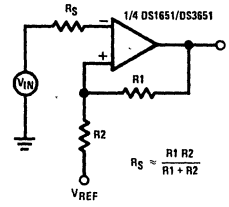
$\overline{2^1} = (\overline{B} + D)\ (\overline{F} + J)\ (\overline{L} + N)\ (\overline{R})$

$\overline{2^2} = (\overline{D} + J)\ (\overline{N})$

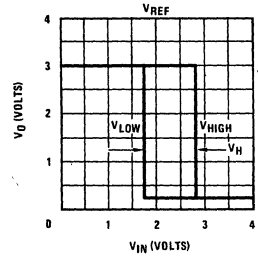
$\overline{2^3} = \overline{J}$

Conversion time ≅ 50 ns

Level Detector with Hysteresis



Transfer Characteristics and Equations for Level Detector with Hysteresis



$$V_{HIGH} = V_{REF} + \frac{R2\ [V_{O(MAX)} - V_{REF}]}{R1 + R2}$$

$$V_{LOW} = V_{REF} + \frac{R2\ [V_{O(MIN)} - V_{REF}]}{R1 + R2}$$

Hysteresis Loop (V_H)

$$V_H = V_{HIGH} - V_{LOW} = \frac{R2}{R1 + R2}\ [V_{O(MAX)} - V_{O(MIN)}]$$

National Semiconductor

Memory Support

DS1671/DS3671 Bootstrapped Two Phase MOS Clock Driver

General Description

The DS1671/DS3671 is a high speed dual MOS clock driver and interface circuit. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL outputs and converts them to MOS logic levels. It may be driven from standard 54/74 and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The circuit can be used in both P-channel and N-channel MOS memory system drive applications.

The DS1671/DS3671 is intended to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for an 8k by 16-bit 1103 RAM memory system.

Each driver uses output bootstrapping to provide a higher voltage to the output stage, thus eliminating the need for an additional V_{DD} supply. The bootstrapping function is accomplished by connecting a small value capacitor (typically 200 pF) from each output to each drivers bootstrap node.

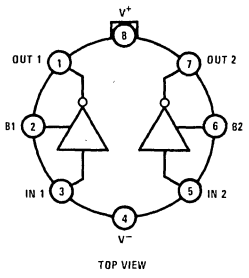
Features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5A
- TTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Swings to 0.4V of GND for RAM address drive

6

Connection Diagrams

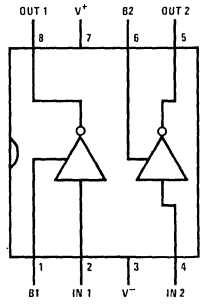
Metal Can Package



TOP VIEW

Order Number DS1671H or DS3671H
See NS Package H08C

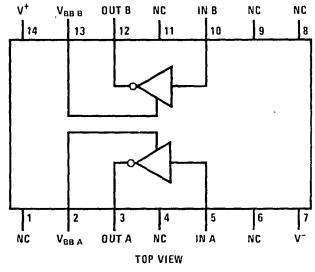
Dual-In-Line Package



TOP VIEW

Order Number DS1671J-8, DS3671J-8
or DS3671N
See NS Package J08A or N08A

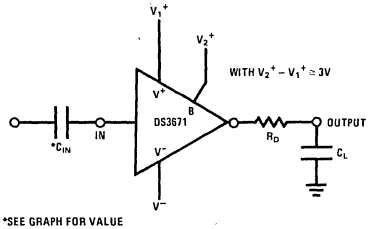
Dual-In-Line Package



TOP VIEW

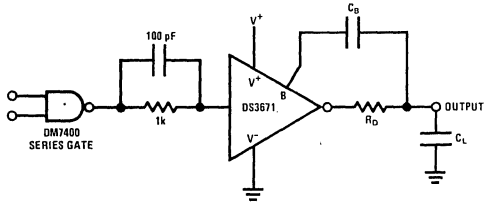
Order Number DS1671J
or DS3671J
See NS Package J14A

Typical Applications



*SEE GRAPH FOR VALUE

DS3671 Operating with Extra Supply
to Inhance Output Voltage Level



Bootstrap Clock Driver Driven from a TTL Gate

Absolute Maximum Ratings (Note 1)

$V^+ - V^-$ Differential	22V
$V_B - V^-$ Differential	40V
$V_B - V^+$ Differential	20V
Input Voltage ($V_{IN} - V^-$)	5.5V
Input Current	100 mA
Peak Output Current	1.5A
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package (8-Pin)	1150 mW
Cavity Package (14-Pin)	1380 mW
Molded Package	1040 mW
Metal Can (TO-5) Package	660 mW

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
$V^+ - V^-$ Differential		20	V
$V_B - V^-$ Differential		40	V
$V_B - V^+$ Differential		20	V
Operating Temperature Range			
DS3671	0	+70	°C
DS1671	−55	+125	°C

*Derate 8-pin cavity package 7.7 mW/°C above 25°C; derate 14-pin cavity package 9.3 mW/°C above 25°C; derate molded package 8.4 mW/°C above 25°C; derate metal can (TO-5) package 4.4 mW/°C above 25°C.

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	$V^- = 0V$		2.0	1.5		V
I_{IH}	Logical "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logical "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logical "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OH}	Logical "1" Output Voltage	$V_B \geq V^+ + 1.0V$, $V_{IN} - V^- \equiv 0.4V$,	DS3671	$V^+-1.0$	$V^+-0.75$		V
		$I_O = 0$ mA	DS1671	$V^+-1.2$	$V^+-0.75$		V
V_{OL}	Logical "0" Output Voltage	$V_{IN} - V^- = 2.4V$, $I_O = 0$ mA			$V^-+0.6$	$V^-+1.0$	V
R_B	Bootstrap Control Resistor			1.1	2.0	3.3	kΩ
$I_{CC(ON)}$	Supply Current One Side "ON"	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$, $V_B = V^+$			30	40	mA
$I_{CC(OFF)}$	Supply Current "OFF"	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0V$	DS3671		10	100	μA
			DS1671		50	500	μA

Switching Characteristics $T_A = 25°C$, $V^+ = 20V$, $V^- = 0V$

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	$R_D = 10\Omega$, $C_L = 1000$ pF			7.5	15	ns
t_{pd1}	Propagation Delay to a Logical "1"	$R_D = 10\Omega$, $C_L = 1000$ pF			12	15	ns
t_r	Rise Time	$R_D = 10\Omega$	$C_L = 500$ pF		25	35	ns
			$C_L = 1000$ pF		31	40	ns
t_f	Fall Time	$R_D = 10\Omega$	$C_L = 500$ pF		30	40	ns
			$C_L = 1000$ pF		38	50	ns

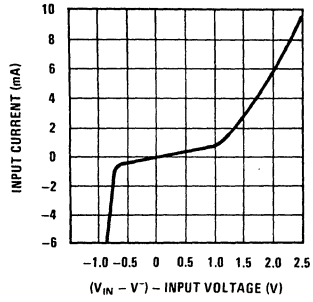
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1671 and across the 0°C to +70°C range for the DS3671. All typicals at 25°C.

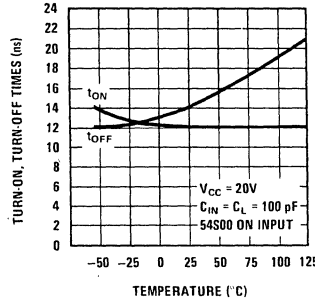
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Performance Characteristics

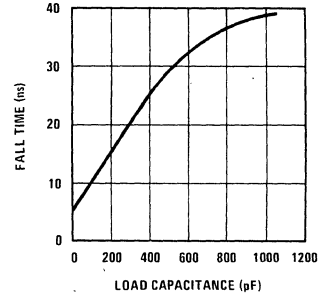
Input Current vs Input Voltage



Turn-On and Turn-Off Time vs Temperature

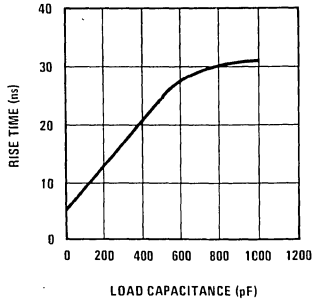


Fall Time vs Load Capacitance

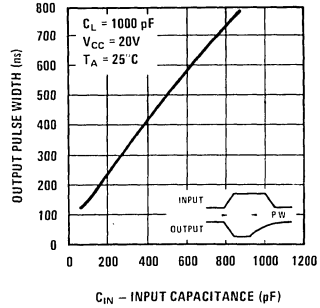


Typical Performance Characteristics (Continued)

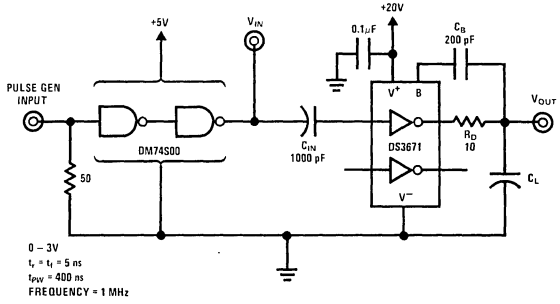
Rise Time vs Load Capacitance

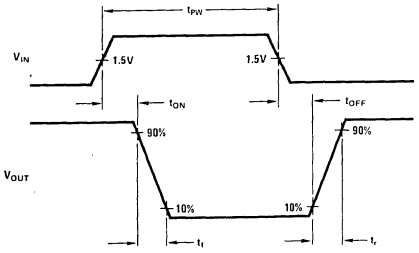


Output Pulse Width When Controlled Only by Input Coupling Capacitor

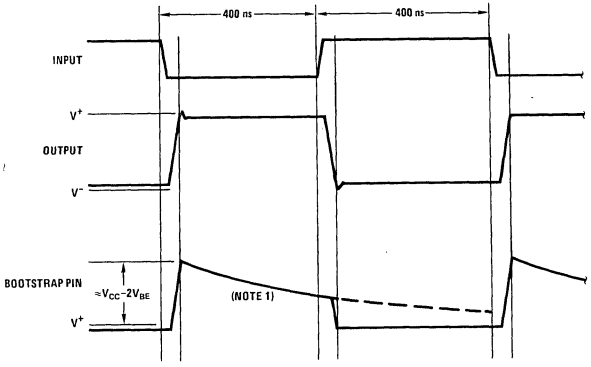


AC Test Circuit and Switching Time Waveforms





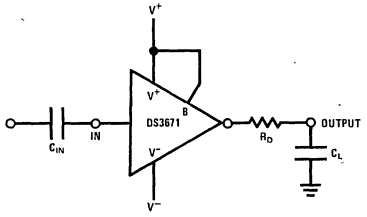
Node Voltage Waveforms



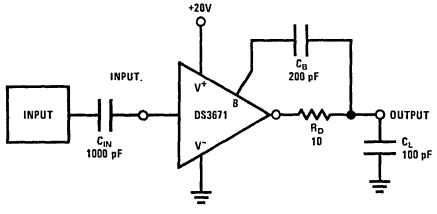
Note 1: The fall time has an exponential decay with the following time constant: $t_B = C_B R_B$. The range of values for R_B (resistor tolerance, and temperature coefficient included) can be found in the table of electrical characteristics.

Note 2: The high current transient (as high as 1.5A) through the resistance of the external interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant DC resistance, it can subtract from the switching response.

Typical Applications (Continued)

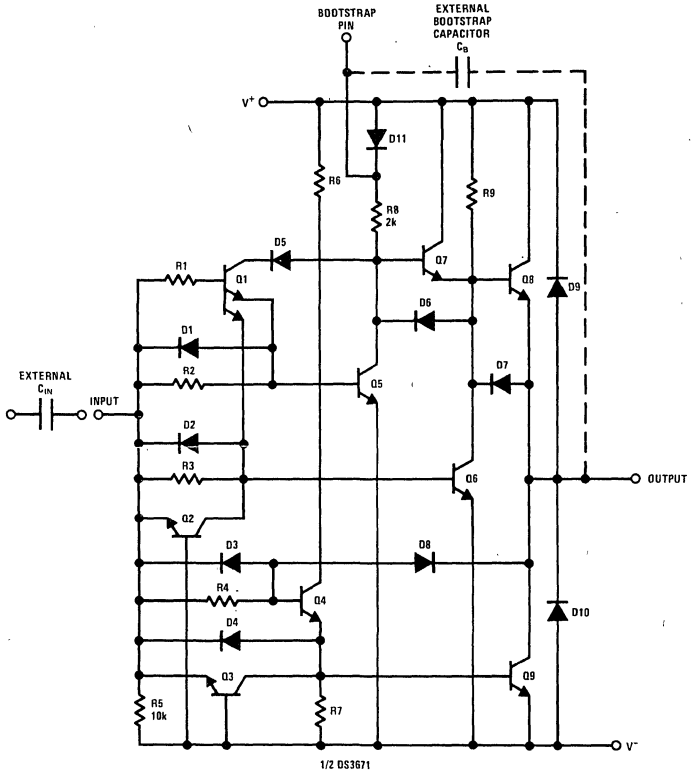


DS3671 Connected as DS0026 with Equivalent Characteristics



Typical Bootstrap

Schematic Diagram (One Driver)



National Semiconductor

Memory Support
PRELIMINARY

DS3685 Hex TRI-STATE® Latch

General Description

The DS3685 is a hex latch. PNP input transistors are used to reduce input currents, allowing large fan-out to these drivers. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs which allow bus operation.

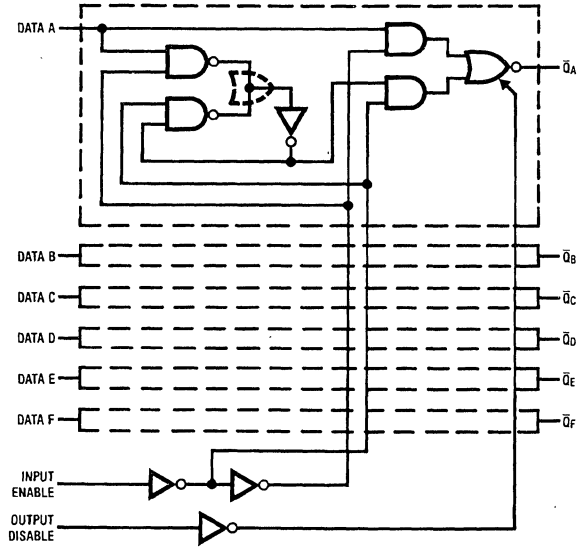
The circuit employs a fall-through latch which captures the data in parallel with the output, thereby eliminating the delay normally encountered in other latch circuits.

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Features

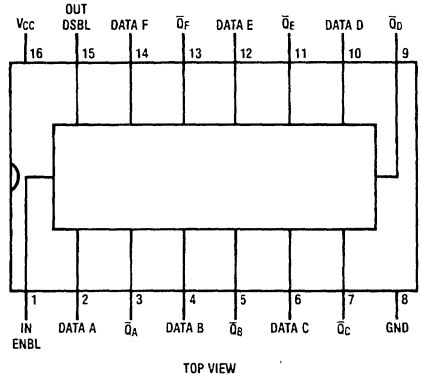
- TTL/LS compatible inputs
- PNP inputs minimize loading
- TRI-STATE outputs
- Fall-through latch design
- Minimum skew

Logic and Connection Diagrams



TL/F/5220–1

Dual-In-Line Package



TOP VIEW

TL/F/5220–2

Order Number DS3685J or DS3685N
See NS Package J16A or N16A

Truth Table

Input Enable	Output Disable	Data	Output	Operation
1	0	1	0	Data Feed-Through
1	0	0	1	Data Feed-Through
0	0	X	Q	Latched to Data Present when Enable Went Low
X	1	X	Hi-Z	High Impedance Output

X = don't care
Hi-Z = TRI-STATE mode

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1433 mW
Molded Package	1362 mW

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Parameter		Conditions		Min	Typ	Max	Units
$V_{IN}(1)$	Logical "1" Input Voltage			2.0			V
$V_{IN}(0)$	Logical "0" Input Voltage					0.8	V
$I_{IN}(1)$	Logical "1" Input Current	V_{IN} = 5.5V, V_{CC} = Max	Enable Inputs		0.1	40	μA
			Data Inputs		0.2	80	μA
$I_{IN}(0)$	Logical "0" Input Current	V_{IN} = 0.5V, V_{CC} = Max	Enable Inputs		−50	−300	μA
			Data Inputs		−100	−500	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA			−0.75	−1.2	V
I_{OS}	Output Short-Circuit Current	V_{CC} = Max, V_{OUT} = 0V, (Note 4)		−40		−100	mA
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min	I_{OH} = −1 mA	2.5	3.5		V
			I_{OH} = −10 μA	2.8	3.8		V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min	I_{OL} = 20 mA		0.4	0.5	V
			I_{OL} = 10 μA		0.25	0.35	V
I_{HZ}	TRI-STATE Output Current	V_{OUT} = 0.4V to 2.4V, Output Disable = 2V		−40		40	μA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs = 3V = 0V, Enable = 3V				90	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C, unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time Low-to-High Level Output	C_L = 15 pF, R_L = 280Ω, *(Figures 1 and 2)*		5.5	7.0	ns
t_{PLH}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 280Ω, *(Figures 1 and 2)*		4.5	6.0	ns
t_{PHL}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF, R_L = 280Ω, *(Figures 1 and 2)*		8		ns
t_{PLH}	Propagation Delay Time, High-to-Low Level Output	C_L = 50 pF, R_L = 280Ω, *(Figures 1 and 2)*		6		ns
t_{SET-UP}	Set-Up Time on Data Input Before Input Enable Goes Low		10	0		ns
t_{HOLD}	Hold Time on Data Input After Input Enable Goes Low		0			ns
t_{ZL}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 15 pF, *(Figures 1 and 3)*		8.2	15	ns
t_{ZH}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 15 pF, *(Figures 1 and 3)*		17	24	ns
t_{LZ}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 15 pF, *(Figures 1 and 4)*		7.7	14	ns
t_{HZ}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 15 pF, *(Figures 1 and 4)*		5.5	12	ns

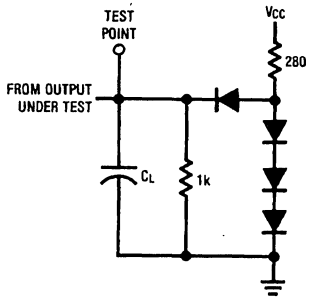
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3685. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

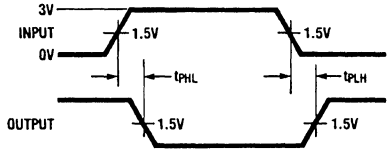
Note 4: Only one output should be shorted at one time.

AC Test Circuit and Switching Time Waveforms



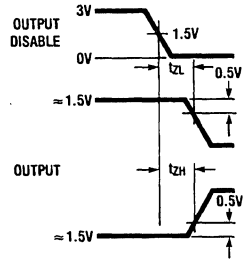
TL/F/5220-3

FIGURE 1



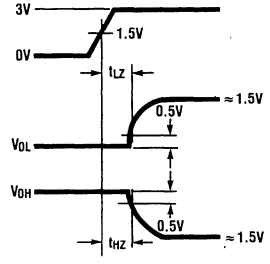
TL/F/5220-4

FIGURE 2



TL/F/5220-5

FIGURE 3

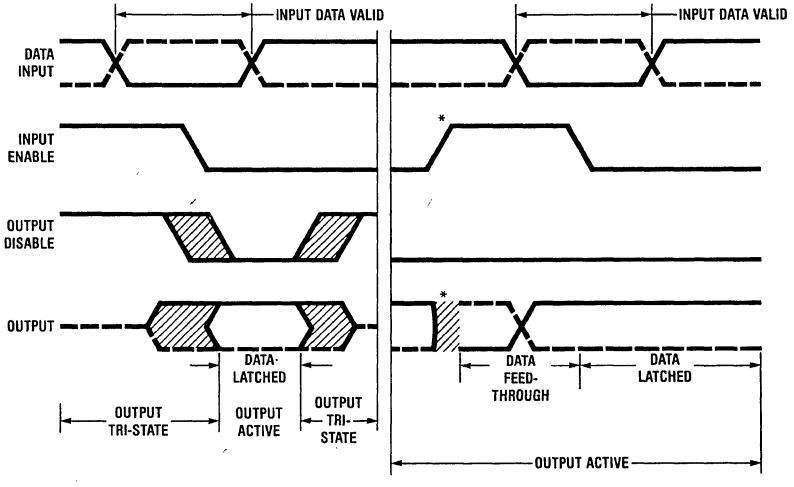


TL/F/5220-6

FIGURE 4

Input characteristics: PRR ≤ 1 MHz, $Z_{OUT} = 50\Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Operating Waveforms



TL/F/5220-7

*When the Input Enable makes a positive transition the output will be indeterminate for a short duration. The positive transition of the Input Enable normally occurs during a don't-care timing state at the output.

National Semiconductor

DS16149/DS36149, DS16179/DS36179 Hex MOS Drivers

General Description

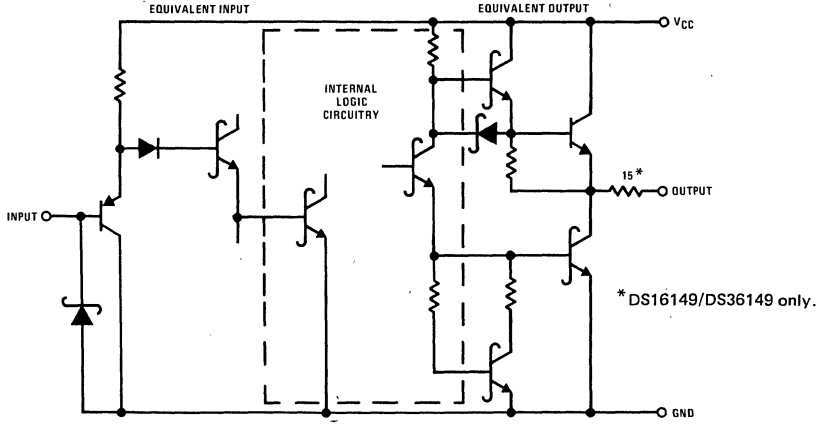
The DS16149/DS36149 and DS16179/DS36179 are Hex MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and a disable control that places the outputs in the logic "1" state (see truth table). This is especially useful in MOS RAM applications where a set of address lines has to be in the logic "1" state during refresh.

The DS16149/DS36149 has a 15 Ω resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS16179/DS36179 has a direct low impedance output for use with or without an external resistor.

Features

- High speed capabilities
  - Typ 9 ns driving 50 pF
  - Typ 29 ns driving 500 pF
- Built-in 15 Ω damping resistor (DS16149/DS36149)
- Same pin-out as DM8096 and DM74366

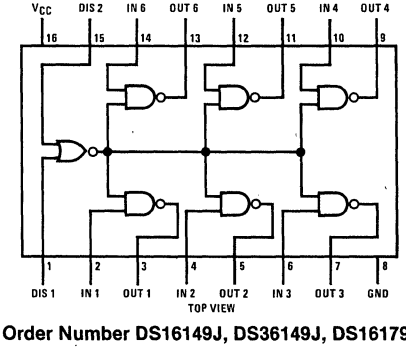
Schematic Diagram



*DS16149/DS36149 only.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS16149J, DS36149J, DS16179J, DS36179J, DS36149N or DS36179N
See NS Package J16A or N16A

Truth Table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	1
1	0	X	1
1	1	X	1

X = Don't care

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1371 mW
Molded Package	1280 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 9.1 mW/°C above 25°C; derate molded package 10.2 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS16149, DS16179	−55	+125	°C
DS36149, DS36179	0	+70	°C

DC Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 0.5V			−50	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V I_{IN} = −18 mA			−0.75	−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V I_{OH} = −10μA	DS16149/DS16179	3.4	4.3		V
			DS36149/DS36179	3.5	4.3		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V I_{OL} = 10μA	DS16149/DS16179		0.25	0.4	V
			DS36149/DS36179		0.25	0.35	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V I_{OH} = −1.0 mA	DS16149	2.4	3.5		V
			DS16179	2.5	3.5		V
			DS36149	2.6	3.5		V
			DS36179	2.7	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V I_{OL} = 20 mA	DS16149		0.6	1.1	V
			DS16179		0.4	0.5	V
			DS36149		0.6	1.0	V
			DS36179		0.4	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V V_{OUT} = 0V, (Note 4)			−250		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V V_{OUT} = 4.5V, (Note 4)			150		mA
I_{CC}	Power Supply Current	V_{CC} = 5.5V	Disable Inputs = 0V All Other Inputs = 3V		33	60	mA
			All Inputs = 0V		14	20	mA

Switching Characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{S+-}	Storage Delay Negative Edge	*(Figure 1)*	C_L = 50 pF		4.5	7	ns
			C_L = 500 pF		7.5	12	ns
t_{S-+}	Storage Delay Positive Edge	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		8	13	ns
t_F	Fall Time	*(Figure 1)*	C_L = 50 pF		5	8	ns
			C_L = 500 pF		22	35	ns
t_R	Rise Time	*(Figure 1)*	C_L = 50 pF		6	9	ns
			C_L = 500 pF		26	35	ns
t_{LH}	Delay from Disable Input to Logical "1"	R_L = 2 kΩ to Gnd, C_L = 50 pF, *(Figure 2)*			15	22	ns
t_{HL}	Delay from Disable Input to Logical "0"	R_L = 2 kΩ to V_{CC}, C_L = 50 pF, *(Figure 3)*			11	18	ns

Notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS16149 and DS16179 and across the 0°C to +70°C range for the DS36149 and DS36179. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS16179 and DS36179 a 15 Ω resistor should be placed in series with each output. This resistor is internal to the DS16149/DS36149 and need not be added.

AC Test Circuits and Switching Time Waveforms

t_{S+-}, t_{S-+}, t_R, t_F

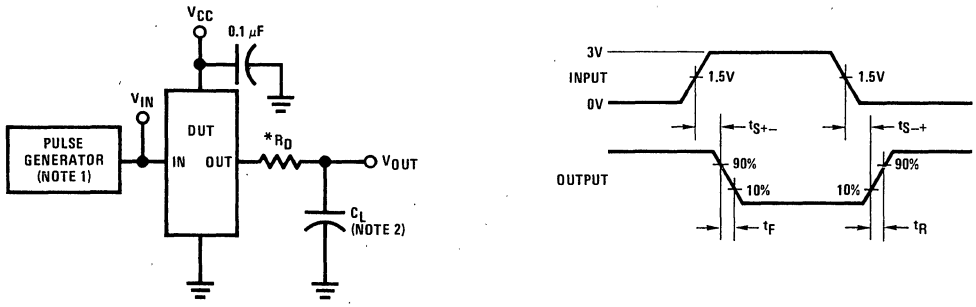


FIGURE 1

t_{LH}

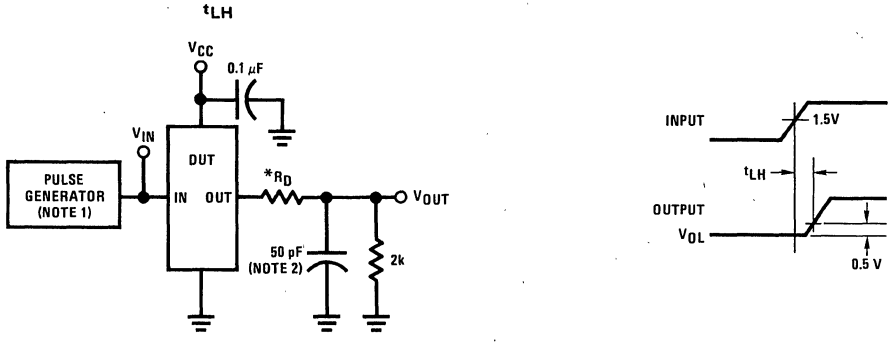


FIGURE 2

t_{HL}

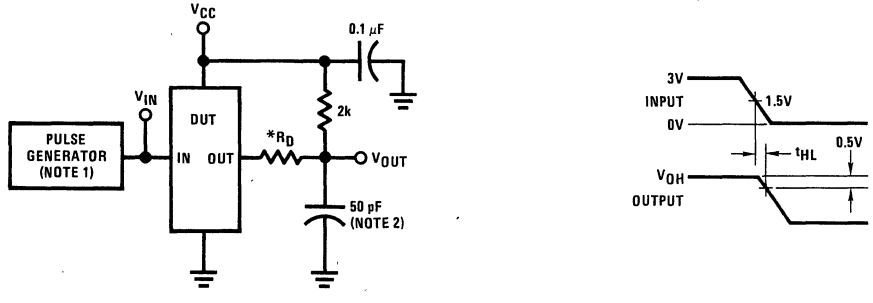


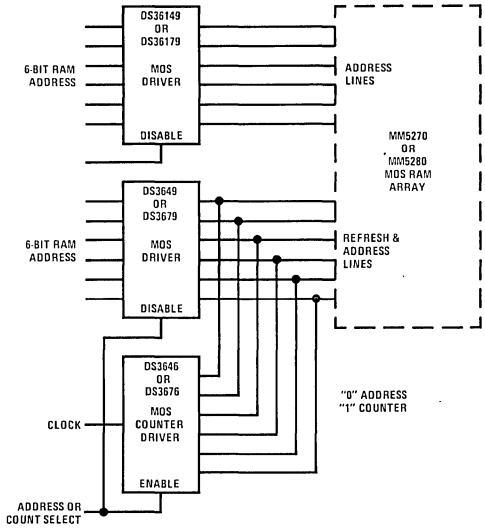
FIGURE 3

*Internal on DS16149 and DS36149

Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10% and 90% points ≤ 5 ns.

Note 2: C_L includes probe and jig capacitance.

Typical Application



National Semiconductor

DS55325/DS75325 Memory Drivers

General Description

The DS55325 and DS75325 are monolithic memory drivers which feature high current outputs as well as internal decoding of logic inputs. These circuits are designed for use with magnetic memories.

The circuit contains two 600 mA sink-switch pairs and two 600 mA source-switch pairs. Inputs A and B determine source selection while the source strobe (S_1) allows the selected source turn on. In the same manner, inputs C and D determine sink selection while the sink strobe (S_2) allows the selected sink turn on.

Sink-output collectors feature an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This protects the outputs from voltage surges associated with switching inductive loads.

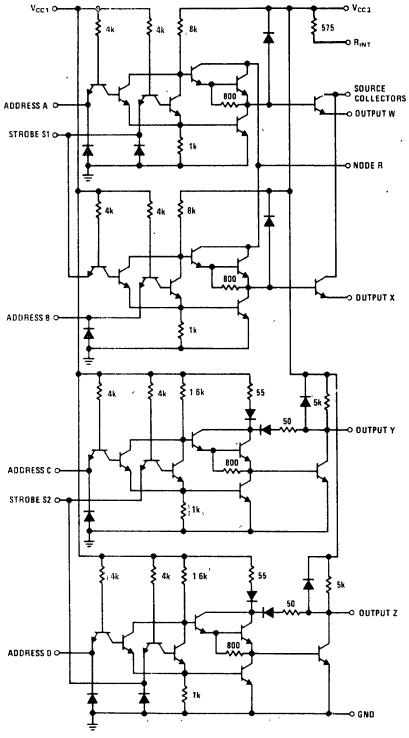
The source stage features Node R which allows extreme flexibility in source current selection by controlling the amount of base drive to each source transistor. This method of setting the base drive brings the power associated with the resistor outside the package thereby allowing the circuit to operate at higher source currents for a given junction temperature. If this method of source current setting is not desired, then Nodes R and R_{INT} can be shorted externally activating an internal resistor connected from V_{CC2} to Node R. This provides adequate base drive for source currents up to 375 mA with V_{CC2} = 15V or 600 mA with V_{CC2} = 24V.

The DS55325 operates over the fully military temperature range of −55°C to +125°C, while the DS5325 operates from 0°C to +70°C.

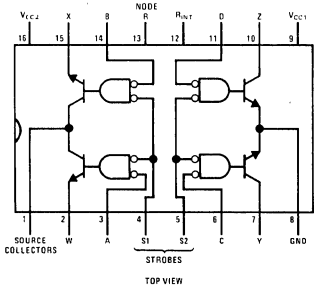
Features

- 600 mA output capability
- 24V output capability
- Dual sink and dual source outputs
- Fast switching times
- Source base drive externally adjustable
- Input clamping diodes
- TTL compatible

Schematic and Connection Diagrams



Dual-In-Line Package



Order Number DS55325J, DS75325J, or DS75325N
See NS Package J14A or N14A

Truth Table

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at any one time.

Absolute Maximum Ratings (Note 1)

Supply Voltage V_{CC1} (Note 5)	7V
Supply Voltage V_{CC2} (Note 5)	25V
Input Voltage (Any Address or Strobe Input)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Temperature (T_A)			
DS55325	−55	+125	°C
DS75325	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	*(Figures 1 and 2)*			2			V
V_{IL}	Low Level Input Voltage	*(Figures 3 and 4)*					0.8	V
V_I	Input Clamp Voltage	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{IN} = −12 mA, T_A = 25°C, *(Figure 5)*				−1.3	−1.7	V
I_{OFF}	Source Collectors Terminal "OFF" State Current	V_{CC1} = 4.5V, V_{CC2} = 24V, *(Figure 1)*	Full Range	DS55325			500	μA
				DS75325			200	μA
			T_A = 25°C	DS55325		3	150	μA
				DS75325		3	200	μA
V_{OH}	High Level Sink Output Voltage	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{OUT} = 0, *(Figure 2)*			19	23		V
V_{SAT}	Saturation Voltage Source Outputs	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SOURCE} ≈ −600 mA, *(Figure 3)*, (Notes 4 and 6)	Full Range				0.9	V
			T_A = 25°C	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
V_{SAT}	Saturation Voltage Sink Outputs	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SINK} ≈ 600 mA, *(Figure 4)*, (Notes 4 and 6)	Full Range				0.9	V
			T_A = 25°C	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
I_I	Input Current at Maximum Input Voltage	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 5.5V, *(Figure 5)*	Address Inputs				1	mA
			Strobe Inputs				2	mA
I_{IH}	High Level Input Current	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 2.4V, *(Figure 5)*	Address Inputs			3	40	μA
			Strobe Inputs			6	80	μA
I_{IL}	Low Level Input Current	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 0.4V, *(Figure 5)*	Address Inputs			−1	−1.6	mA
			Strobe Inputs			−2	−3.2	mA
$I_{CC\,OFF}$	Supply Current, All Sources and Sinks "OFF"	V_{CC1} = 5.5V, V_{CC2} = 24V, T_A = 25°C, *(Figure 6)*	V_{CC1}			14	22	mA
			V_{CC2}			7.5	20	mA
I_{CC1}	Supply Current From V_{CC1}, Either Sink "ON"	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SINK} = 50 mA, T_A = 25°C, *(Figure 7)*				55	70	mA
I_{CC2}	Supply Current From V_{CC2}, Either Source "ON"	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SOURCE} = −50 mA, T_A = 25°C, *(Figure 8)*				32	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55325 and across the 0°C to +70°C range for the DS75325. All typical values are at T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

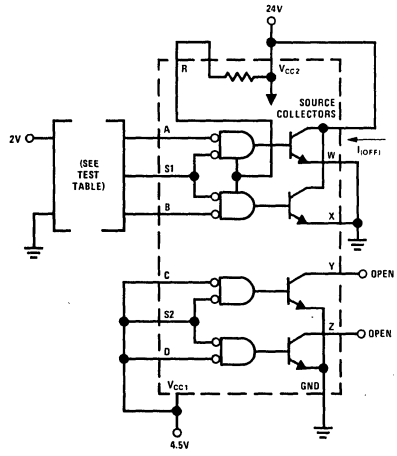
Note 5: Voltage values are with respect to network ground terminal.

Note 6: These parameters must be measured using pulse techniques. t_W = 200μs, duty cycle ≤ 2%.

Switching Characteristics (V_{CC1} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 25 pF	Source Outputs, V_{CC2} = 20V, R_L = 1 kΩ, *(Figure 10)*		55		ns
			Sink Outputs, V_{CC2} = 15V, R_L = 24Ω, *(Figure 9)*		7	15	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 25 pF	Source Outputs, V_{CC2} = 20V, R_L = 1 kΩ, *(Figure 10)*		7		ns
			Sink Outputs, V_{CC2} = 15V, R_L = 24Ω, *(Figure 9)*		9	20	ns
t_S	Storage Time, Sink Outputs	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, *(Figure 9)*			15	30	ns

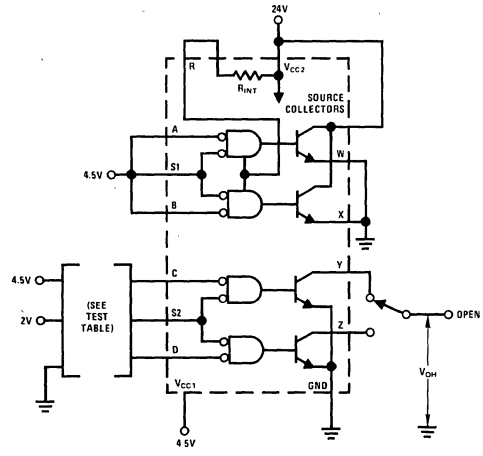
DC Test Circuits



TEST TABLE

A	B	S1
GND	GND	2V
2V	2V	GND

FIGURE 1. I_{OFF}

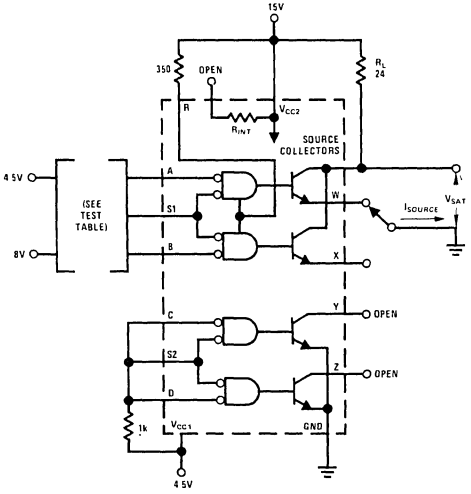


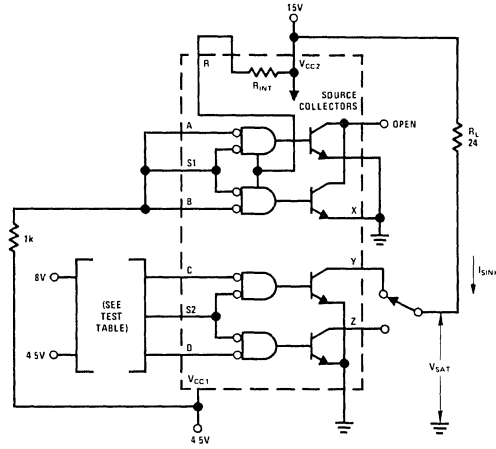
TEST TABLE

C	D	S2	Y	Z
2V	4.5V	GND	V_{OH}	OPEN
GND	4.5V	2V	V_{OH}	OPEN
4.5V	2V	GND	OPEN	V_{OH}
4.5V	GND	2V	OPEN	V_{OH}

FIGURE 2. V_{IH} and V_{OH}

DC Test Circuits (Continued)





Note 1: Figures 3 and 4 parameters must be measured using pulse techniques. $t_W = 200\mu s$, duty cycle $\leq 2\%$.

TEST TABLE

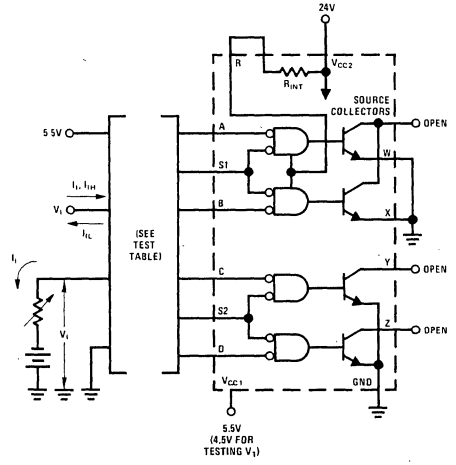
A	B	S1	W	X
0.8V	4.5V	0.8V	GND	OPEN
4.5V	0.8V	0.8V	OPEN	GND

FIGURE 3. V_{IL} and Source V_{SAT}

TEST TABLE

C	D	S2	Y	Z
0.8V	4.5V	0.8V	R_L	OPEN
4.5V	0.8V	0.8V	OPEN	R_L

FIGURE 4. V_{IL} and Sink V_{SAT}



TEST TABLES

I_I, I_{IH}

APPLY V_I = 5.5V MEASURE I_I / APPLY V_I = 2.4V MEASURE I_{IH}	GROUND	APPLY 5.5V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_I = 0.4V, MEASURE I_{IL} / APPLY I_I = −10 mA, MEASURE V_I	APPLY 5.5V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5. V_I, I_I, I_{IH}, and I_{IL}

DC Test Circuits (Continued)

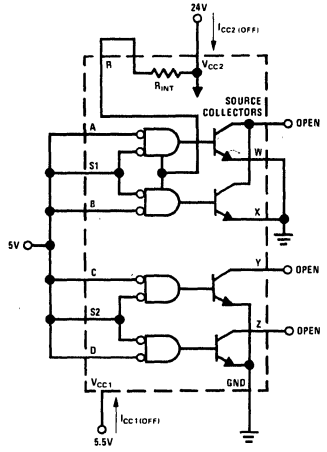
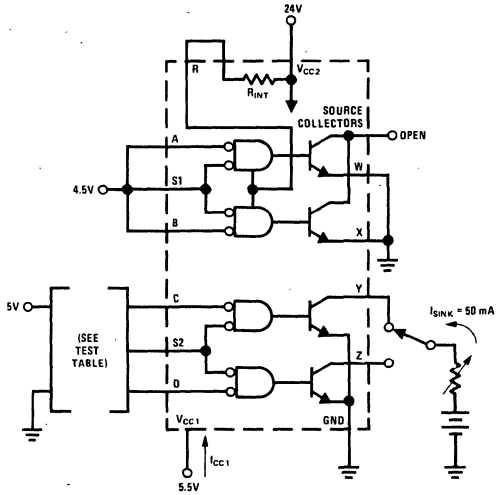


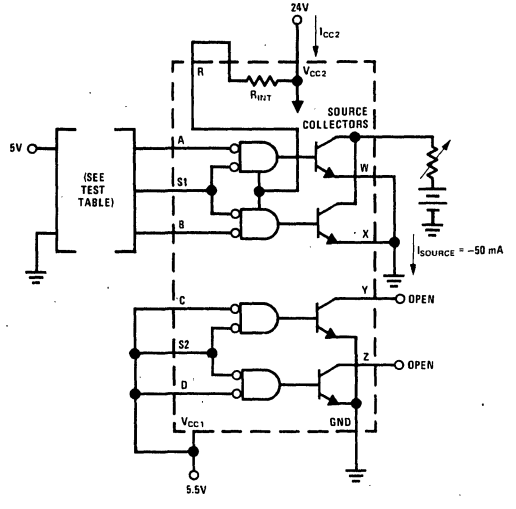
FIGURE 6. $I_{CC1(OFF)}$ and $I_{CC2(OFF)}$



TEST TABLE

C	D	S2	Y	Z
GND	5V	GND	$I_{(SINK)}$	OPEN
5V	GND	GND	OPEN	$I_{(SINK)}$

FIGURE 7. I_{CC1}, Either Sink On

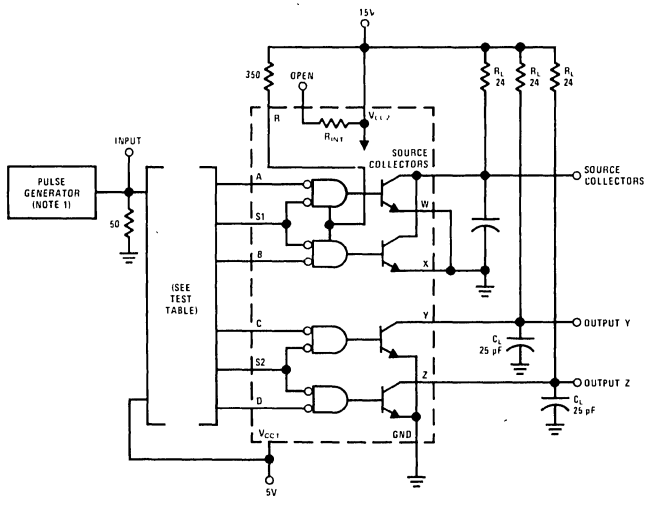


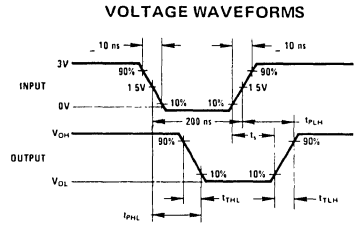
TEST TABLE

A	B	S1
GND	5V	GND
5V	GND	GND

FIGURE 8. I_{CC2}, Either Source On

DC Test Circuits (Continued)





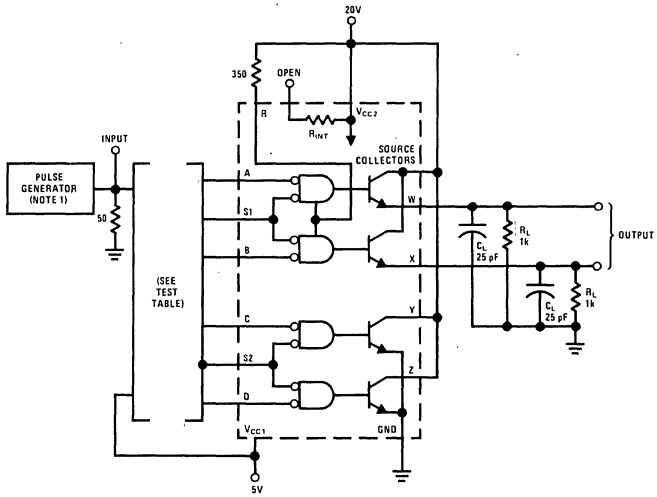
Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, duty cycle ≤ 1%.

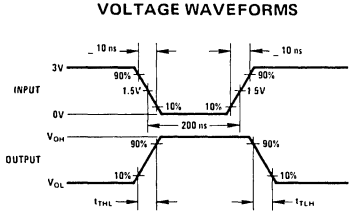
Note 2: C_L includes probe and jig capacitance

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1

FIGURE 9. Switching Times





Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, duty cycle ≤ 1%.

Note 2: C_L includes probe and jig capacitance.

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2

FIGURE 10. Transition Times of Source Outputs

Applications

External Resistor Calculation

A typical magnetic-memory word drive requirement is shown in Figure 11. A source-output transistor of one DS75325 delivers load current (I_L). The sink-output transistor of another DS75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \quad (1)$$

where: R_{ext} is in kΩ,

$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts, V_S is the source output voltage in volts with respect to ground, I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \quad (2)$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94\ I_L \quad (3)$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(min)}$ = 20V and V_L = 3V while I_L of 500 mA flows. Using Equation 1:

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ k\Omega$$

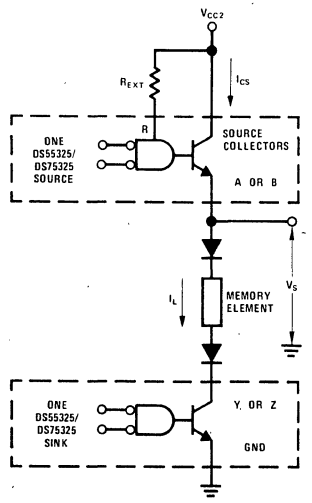
and from Equation 2:

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\ (500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.



Note 1: For clarity, partial logic diagrams of two DS55325's are shown.
Note 2: Source and sink shown are in different packages.

FIGURE 11. Typical Application Data

DS75361 Dual TTL-to-MOS Driver

General Description

The DS75361 is a monolithic integrated dual TTL-to-MOS driver interface circuit. The device accepts standard TTL input signals and provides high-current and high-voltage output levels for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103 and MM5270 and MM5280.

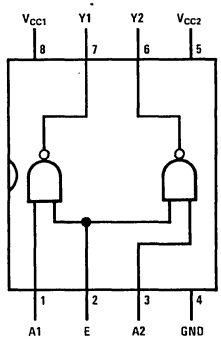
The DS75361 operates from standard TTL 5V supplies and the MOS V_{SS} supply in many applications. The device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V; however, it is designed for use over a much wider range of V_{CC2}.

Features

- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V
- Diode-clamped inputs
- TTL compatible
- Operates from standard bipolar and MOS supplies
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS75361J-8 or DS75361N
See NS Package J08A or N08A

Absolute Maximum Ratings (Note 1)

Supply Voltage Range of V_{CC1} (Note 1)	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1022 mW
Lead Temperature 1/16 Inch from Case for 60 Seconds: J Package	300°C
Lead Temperature 1/16 Inch from Case for 10 Seconds: N or P Package	200°C

*Derate molded package 8.2 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Operating Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-Level Output Voltage	V_{IL} = 0.8V, I_{OH} = −50μA		V_{CC2}−1	V_{CC2}−0.7		V
		V_{IL} = 0.8V, I_{OH} = −10 mA		V_{CC2}−2.3	V_{CC2}−1.8		V
V_{OL}	Low-Level Output Voltage	V_{IH} = 2V, I_{OL} = 10 mA			0.15	0.3	V
		V_{CC2} = 15V to 24V, V_{IH} = 2V, I_{OL} = 40 mA			0.25	0.5	V
V_O	Output Clamp Voltage	V_I = 0V, I_{OH} = 20 mA				V_{CC2}+1.5	V
I_I	Input Current at Maximum Input Voltage	V_I = 5.5V				1	mA
I_{IH}	High-Level Input Current	V_I = 2.4V	A Inputs			40	μA
			E Input			80	μA
I_{IL}	Low-Level Input Current	V_I = 0.4V	A Inputs		−1	−1.6	mA
			E Input		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, Both Outputs High	V_{CC1} = 5.25V, V_{CC2} = 24V, All Inputs at 0V, No Load			2	4	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, Both Outputs High					0.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, Both Outputs Low	V_{CC1} = 5.25V, V_{CC2} = 24V, All Inputs at 5V, No Load			16	24	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, Both Outputs Low				7	11	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	V_{CC1} = 0V, V_{CC2} = 24V, All Inputs at 5V, No Load				0.5	mA

Switching Characteristics (V_{CC1} = 5V, V_{CC2} = 20V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			25	40	ns
t_{THL}	Transition Time, High-to-Low Level Output			21	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	36	55	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	31	47	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

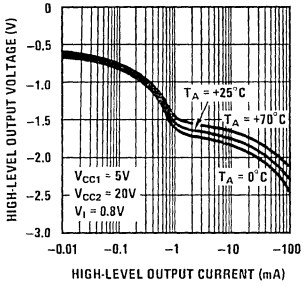
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75361. All typical values are for T_A = 25°C and V_{CC1} = 5V and V_{CC2} = 20V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

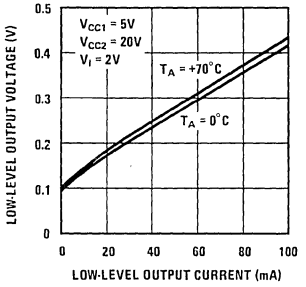
Note 4: This rating applies between the A input of either driver and the common E input.

Typical Performance Characteristics

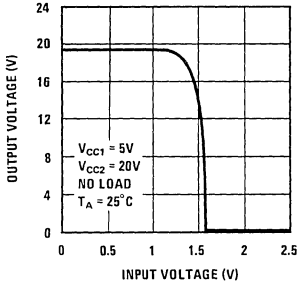
High-Level Output Voltage vs Output Current



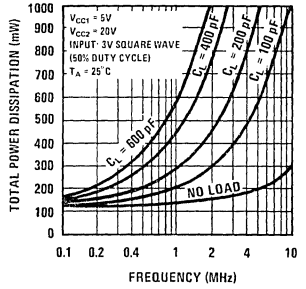
Low-Level Output Voltage vs Output Current



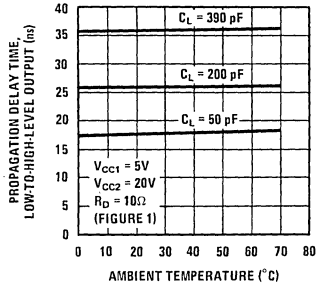
Voltage Transfer Characteristics



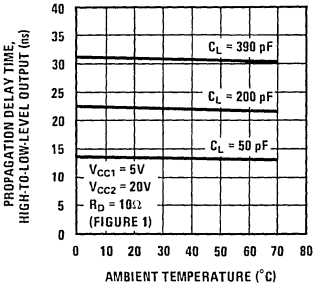
Total Dissipation (Both Drivers) vs Frequency



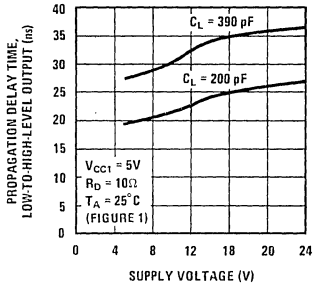
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



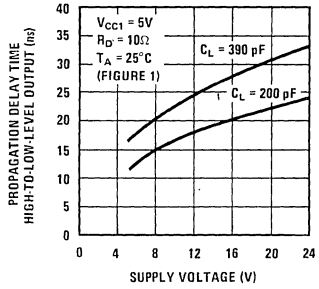
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



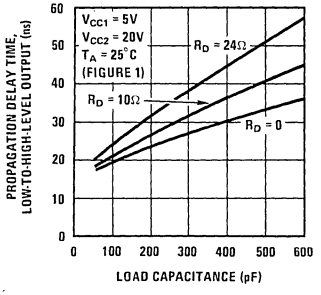
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



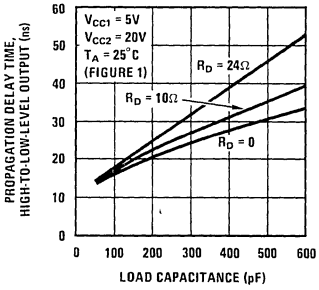
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



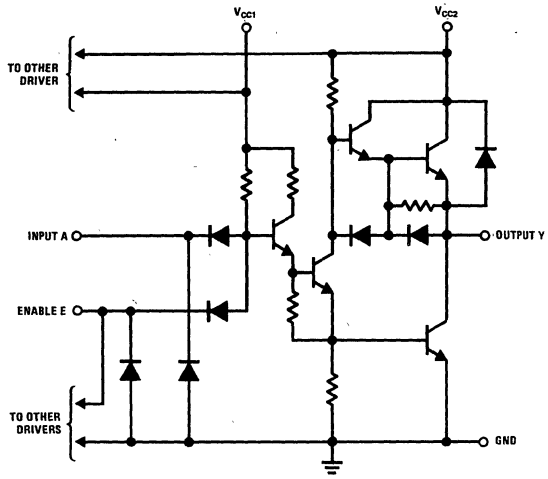
Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



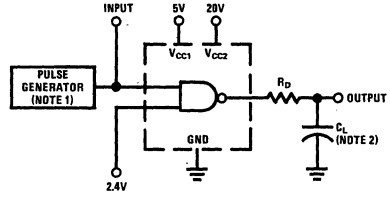
Propagation Delay Time, High-to-Low Level Output vs Load Capacitance

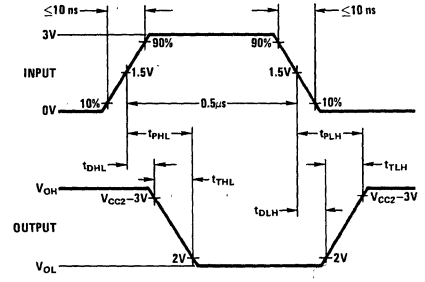


Schematic Diagram (1/2 shown)



AC Test Circuit and Switching Time Waveforms





Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 1. Switching Times, Each Driver

Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 3)*.

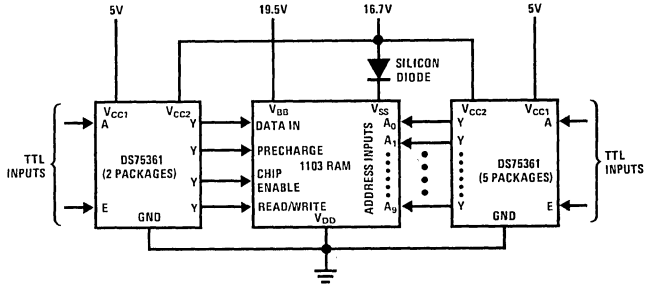
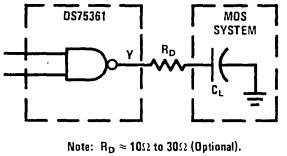


FIGURE 2. Interconnection of DS75361 Devices with 1103 RAM



Note: $R_D \approx 10\Omega$ to 30Ω (Optional).

FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75361 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75361 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75361 as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{p_L t_L + p_H t_H}{T}$$

$$P_{C(AV)} \approx C\, V_C^2\, f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + p_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 4*.

p_L, p_H, p_{LH}, and p_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75361 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, and duty cycle = 60% outputs high ($t_H/T = 0.6$). Also, assume V_{OH} = 19.3V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{2\text{ mA}}{2}\right) + (20V)\left(\frac{0\text{ mA}}{2}\right)\right](0.6) + \left[(5V)\left(\frac{16\text{ mA}}{2}\right) + (20V)\left(\frac{7\text{ mA}}{2}\right)\right](0.4)$$

$P_{DC(AV)}$ = 47 mW per channel

$P_{C(AV)} \approx (200\text{ pF})\,(19.2V)^2\,(2\text{ MHz})$

$P_{C(AV)} \approx 148$ mW per channel.

For the total device dissipation of the two channels:

$P_{T(AV)} \approx 2\,(47 + 148)$

$P_{T(AV)} \approx 390$ mW typical for total package.

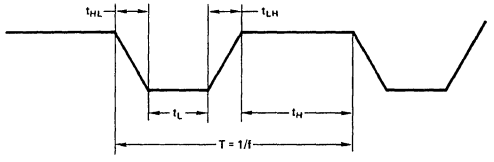


FIGURE 4. Output Voltage Waveform

National Semiconductor

DS75362 Dual TTL-to-MOS Driver

General Description

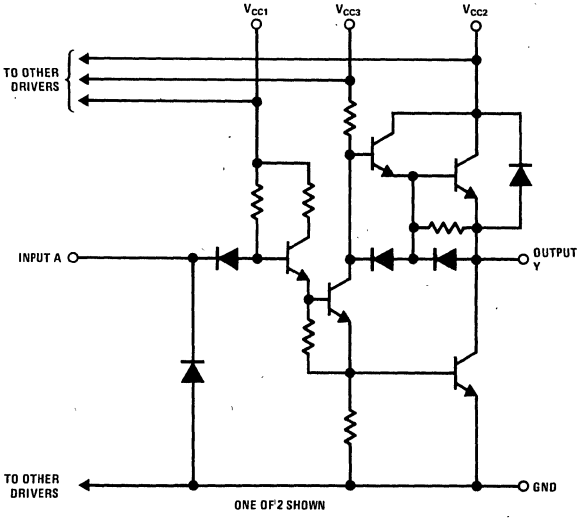
The DS75362 is a dual monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75362 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

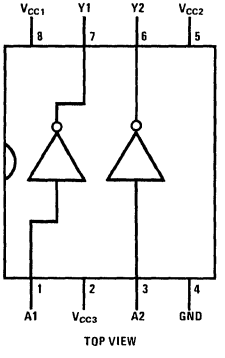
Features

- Dual positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Schematic and Connection Diagrams



Dual-In-Line Package



Order Number DS75362J-8 or DS75362N
See NS Package J08A or N08A

Absolute Maximum Ratings (Note 1)

Supply Voltage Range of V_{CC1}	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Supply Voltage Range of V_{CC3}	−0.5V to 30V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Molded Package	1022 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 8.2 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Supply Voltage (V_{CC3})	V_{CC2}	28	V
Voltage Difference Between Supply Voltages: $V_{CC3}-V_{CC2}$	0	10	V
Operating Ambient Temperature Range (T_A)	0	70	°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage		2			V
V_{IL}	Low-Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA			−1.5	V
V_{OH}	High-Level Output Voltage	$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -100\mu A$	$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
		$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA	$V_{CC2}-1.2$	$V_{CC2}-0.9$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -50\mu A$	$V_{CC2}-1$	$V_{CC2}-0.7$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA	$V_{CC2}-2.3$	$V_{CC2}-1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA		0.15	0.3	V
		$V_{CC3} = 15V$ to 28V, $V_{IH} = 2V$, $I_{OL} = 40$ mA		0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA			$V_{CC2}+1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$			1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$			40	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$		−1	−1.6	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 0V, No Load		2	4	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High			−1.1	+0.25	mA
				−1.1	−1.6	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High			1.1	1.8	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, All Outputs Low	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 5V, No Load		15	23.5	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, All Outputs Low				1.5	mA
$I_{CC3(L)}$	Supply Current from V_{CC3}, All Outputs Low			8	12.5	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 0V, No Load			0.25	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High				0.5	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	$V_{CC1} = 0V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 5V, No Load			0.25	mA
$I_{CC3(S)}$	Supply Current from V_{CC3}, Stand-by Condition				0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75362. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$ and $V_{CC2} = 20V$ and $V_{CC3} = 24V$.

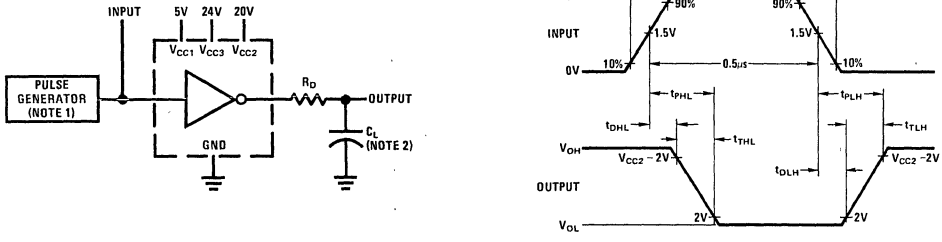
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between any two inputs of any one of the gates.

Switching Characteristics (V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 200 pF, R_D = 24Ω, (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			20	33	ns
t_{THL}	Transition Time, High-to-Low Level Output			20	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	31	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	30	46	ns

AC Test Circuit and Switching Time Waveforms

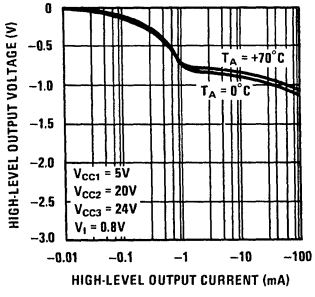


Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

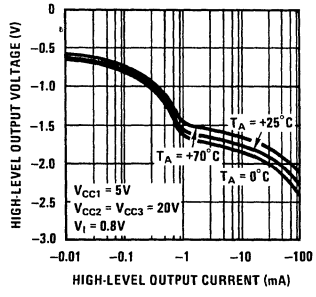
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

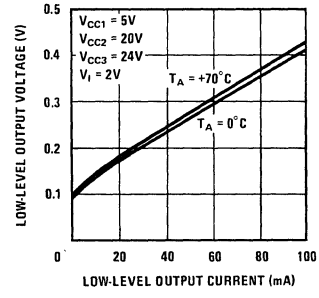
High-Level Output Voltage vs Output Current



High-Level Output Voltage vs Output Current

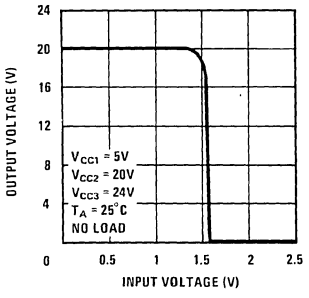


Low-Level Output Voltage Output Current

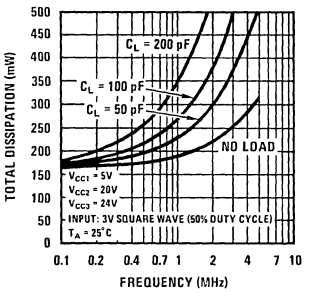


Typical Performance Characteristics (Continued)

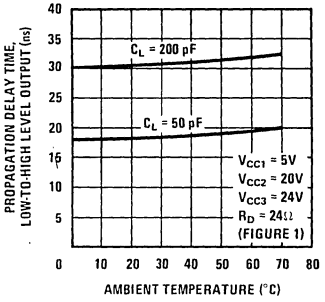
Voltage Transfer Characteristics



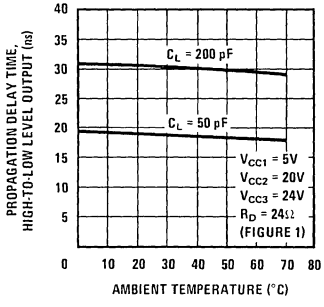
Total Dissipation (Two Drivers) vs Frequency



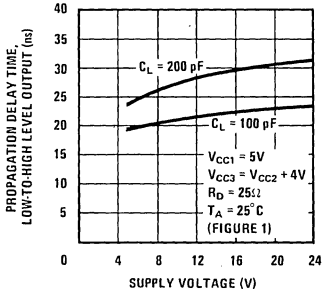
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



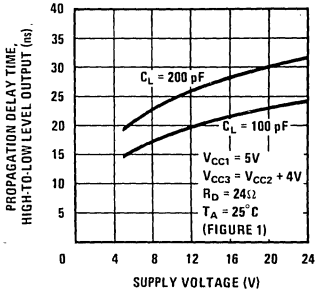
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



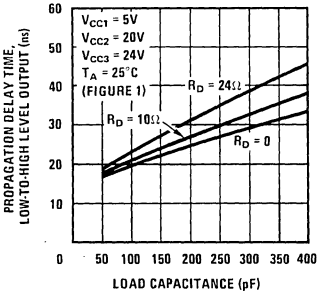
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



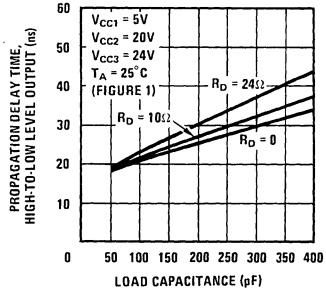
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance

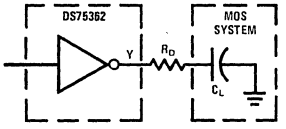


Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



Typical Application

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 2).*



Note: $R_D \approx 10\Omega$ to 30Ω (Optional).

FIGURE 2. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot In Certain DS75362 Applications.

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75362 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75362 as a function of load capacitance and frequency. Average power dissipation by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{p_L t_L + p_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + p_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 3.*

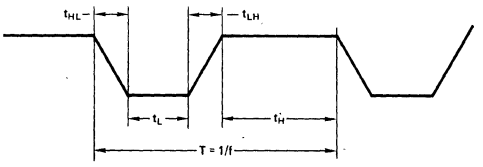


FIGURE 3. Output Voltage Waveform

p_L, p_H, p_{LH}, and p_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75362 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from two channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume two channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{4\text{ mA}}{4}\right) + (20V)\left(\frac{-2.2\text{ mA}}{4}\right) + (24V)\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5V)\left(\frac{31\text{ mA}}{4}\right) + (20V)\left(\frac{0\text{ mA}}{4}\right) + (24V)\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$$P_{DC(AV)} = 58\text{ mW per channel}$$

$$P_{C(AV)} \approx (100\text{ pF})(19.9V)^2(2\text{ MHz})$$

$$P_{C(AV)} \approx 79\text{ mW per channel.}$$

For the total device dissipation of the two channels

$$P_{T(AV)} \approx 2(58 + 79)$$

$$P_{T(AV)} \approx 274\text{ mW typical for total package.}$$

DS75365 Quad TTL-to-MOS Driver

General Description

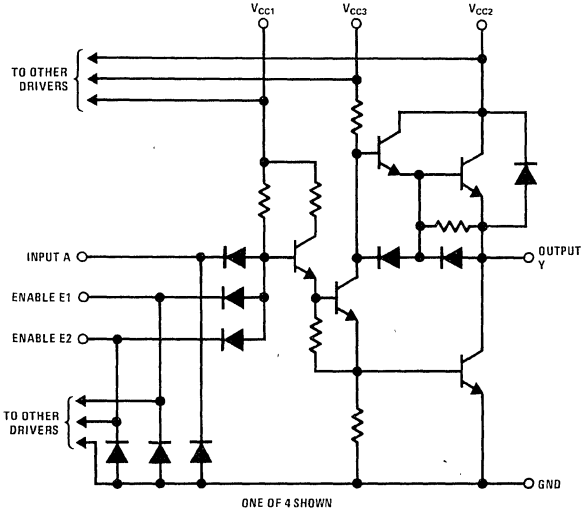
The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75365 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

Features

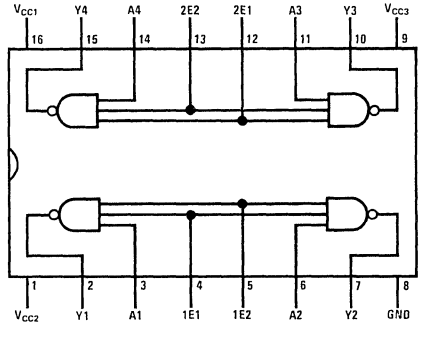
- Quad positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- Interchangeable with Intel 3207
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- Two common enable inputs per gate-pair
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

Schematic and Connection Diagrams



ONE OF 4 SHOWN

Dual-In-Line Package



TOP VIEW

Positive Logic: $Y = \overline{A \cdot E1 \cdot E2}$

Order Number DS75365J
or DS75365N
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

Supply Voltage Range of V_{CC1}	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Supply Voltage Range of V_{CC3}	−0.5V to 30V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Supply Voltage (V_{CC3})	V_{CC2}	28	V
Voltage Difference Between Supply Voltages: $V_{CC3}-V_{CC2}$	0	10	V
Operating Ambient Temperature Range (T_A)	0	70	°C

Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-Level Output Voltage	$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -100\mu A$		$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
		$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2}-1.2$	$V_{CC2}-0.9$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -50\mu A$		$V_{CC2}-1$	$V_{CC2}-0.7$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2}-2.3$	$V_{CC2}-1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC3} = 15V$ to 28V, $V_{IH} = 2V$, $I_{OL} = 40$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA				$V_{CC2}+1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$	A Inputs			40	μA
			E1 and E2 Inputs			80	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$	A Inputs		−1	−1.6	mA
			E1 and E2 Inputs		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 0V, No Load			4	8	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High				−2.2	+0.25	mA
					−2.2	−3.2	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High				2.2	3.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, All Outputs Low	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 5V, No Load			31	47	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, All Outputs Low					3	mA
$I_{CC3(L)}$	Supply Current from V_{CC3}, All Outputs Low				16	25	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 0V, No Load				0.25	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High					0.5	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	$V_{CC1} = 0V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 5V, No Load				0.25	mA
$I_{CC3(S)}$	Supply Current from V_{CC3}, Stand-by Condition					0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75365. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$ and $V_{CC2} = 20V$ and $V_{CC3} = 24V$.

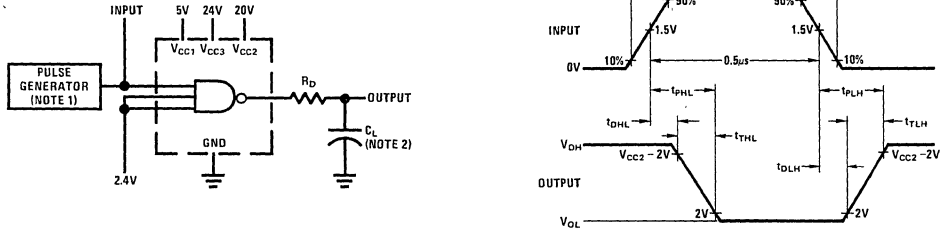
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between any two inputs of any one of the gates.

Switching Characteristics (V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 200 pF, R_D = 24Ω, (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			20	33	ns
t_{THL}	Transition Time, High-to-Low Level Output			20	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	31	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	30	46	ns

AC Test Circuit and Switching Time Waveforms

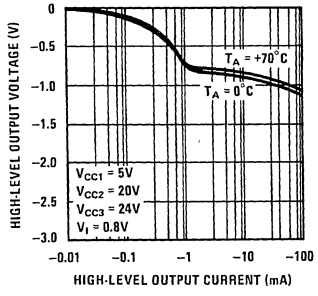


Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

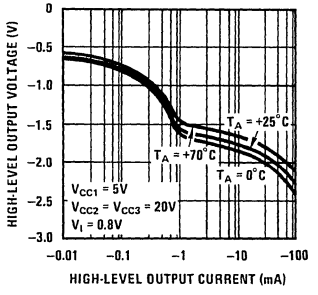
FIGURE 1. Switching Times, Each Driver

Typical Performance Characteristics

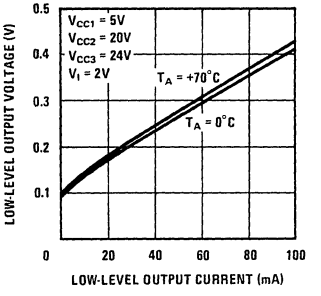
High-Level Output Voltage vs Output Current



High-Level Output Voltage vs Output Current

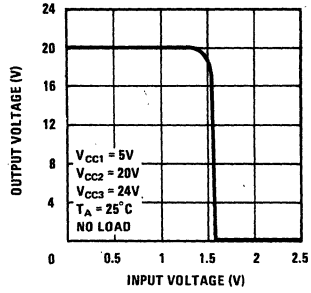


Low-Level Output Voltage Output Current

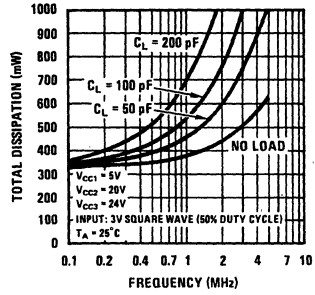


Typical Performance Characteristics (Continued)

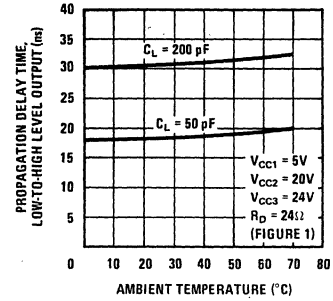
Voltage Transfer Characteristics



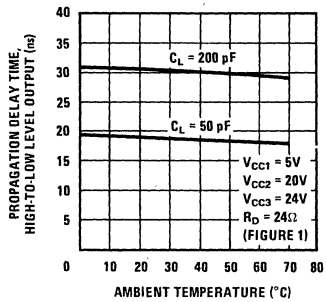
Total Dissipation (All Four Drivers) vs Frequency



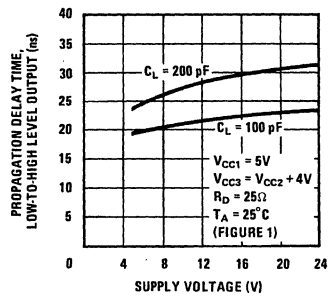
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



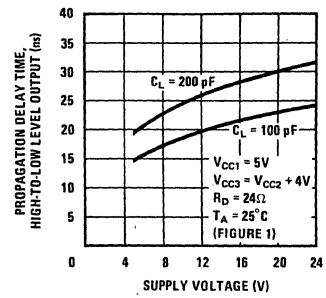
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



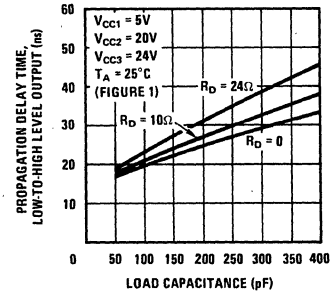
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



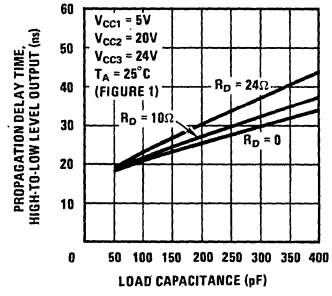
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



Typical Applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 3).*

Typical Applications (Continued)

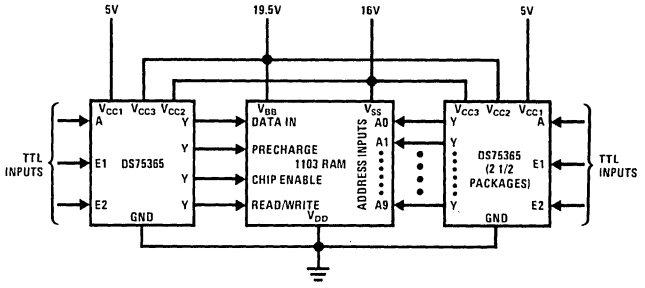
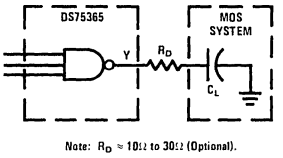


FIGURE 2. Interconnection of DS75365 Devices With 1103-Type Silicon-Gate MOS RAM



Note: $R_D \approx 10\Omega$ to 30Ω (Optional).

FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot In Certain DS75365 Applications

Thermal Information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75365 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75365 as a function of load capacitance and frequency. Average power dissipation by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{p_L t_L + p_H t_H}{T}$$

$$P_{C(AV)} \approx C\, V_C{}^2\, f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + p_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 4.*

p_L, p_H, p_{LH}, and p_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75365 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H >> t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from all four channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume all four channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{4\text{ mA}}{4}\right) + (20V)\left(\frac{-2.2\text{ mA}}{4}\right) + (24V)\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5V)\left(\frac{31\text{ mA}}{4}\right) + (20V)\left(\frac{0\text{ mA}}{4}\right) + (24V)\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58 mW per channel

$P_{C(AV)} \approx$ (100 pF) $(19.9V)^2$ (2 MHz)

$P_{C(AV)} \approx$ 79 mW per channel.

For the total device dissipation of the four channels:

$P_{T(AV)} \approx 4\,(58 + 79)$

$P_{T(AV)} \approx$ 548 mW typical for total package.

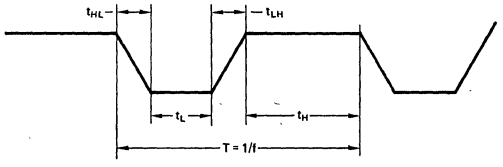


FIGURE 4. Output Voltage Waveform

Applying Modern Clock Drivers to MOS Memories

National Semiconductor
Application Note 76
B. Siegel
M. Scott
October 1975

INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input wave forms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types shift registers and RAM's (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of driver, monolithic integrated circuit drivers, the DS0025, DS0026 and DS0056 are selected as examples because of their low cost.

The DS0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage-gold doped process utilizing a collector sinker to minimize $V_{CE\,SAT}$.

The DS0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. The DS0056 is a variation of the DS0026 circuit which allows the system designer to modify the output performance of the circuit. The DS0056 can be connected (using a second power supply) to increase the positive output voltage level and reduce the effect of cross coupling capacitance between the clock lines in the system. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking required, reliability and cost. Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

TABLE I. DS0025 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		15	ns
t_{OFF}	C_{IN} = 0.0022μF, R_{IN} = 0Ω	30	ns
t_r	C_L = 0.0001μF, RO = 50Ω	25	ns
t_f		150	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 1.0$	V
On Supply Current (V^+)	I_{IN} = 10 mA	17	mA

TABLE II. DS0026 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		7.5	ns
t_{OFF}	C_{IN} = 0.001μF, R_{IN} = 0Ω	7.5	ns
t_r	RO = 50Ω, C_L = 1000 pF	25	ns
t_f		25	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 0.5$	V
On Supply Current (V^+)	I_{IN} = 10 mA	28	mA

The TO-5 ("H") package is rated at 750 mW still air (derate at 200°C/W above 25°C) soldered to PC board. This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on heat sink increases driving capability by 50%.

The 8-pin ("N") molded mini-DIP is rated at 600 mW still air (derate at 90°C/W above 25°C) soldered to PC board (derate at 1.39W). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

To TO-8 ("G") package is rated at 1.5W still air (derate at 100°C/W above 25°C) and 2.3W with clip-on heat sink (Wakefield type 215-1.9 or equivalent-derate at 15 mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

Additional information is given in the section of this data book on Maximum Power Dissipation (page 2).

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

1. Package and heat sink selection
2. Average dc power, P_{DC}
3. Average ac power, P_{AC}
4. Numbers of drivers per package, n

From the package heat sink, and maximum ambient temperature one can determine P_{MAX}, which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of dc power and ac power in each driver times the number of drivers. The total of which must be less than the package power rating.

$$P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \qquad (1)$$

Average dc power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

$$P_{DC} = P_{IN} + P_{OFF} + P_{ON} \qquad (2)$$

For most types of clock drivers, the first two terms are negligible (less than 10 mW) and may be ignored.

Thus:

$$P_{DC} \cong P_{ON} = \frac{(V^+ - V^-)^2}{Req} \times (DC)$$

where:

$V^+ - V^-$ = Total voltage across the driver

Req = Equivalent device resistance in the "ON" state

$$= V^+ - V^-/I_{S(ON)} \qquad (3)$$

DC = Duty Cycle

$$= \frac{\text{"ON" Time}}{\text{"ON" Time + "OFF" Time}}$$

For the DS0025, Req is typically 1 kΩ while Req is typically 600Ω for the DS0026. Graphical solutions for P_{DC} appear in *Figure 1.* For example if V^+ = +5V, V^- = −12V, Req = 500 Ω, and DC = 25%, then P_{DC} = 145 mW. However, if the duty cycle was only 5%, P_{DC} = 29 mW. Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.

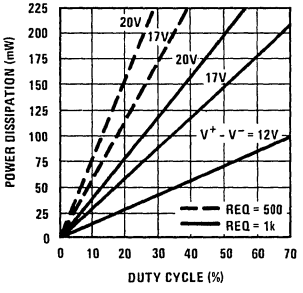


FIGURE 1. P_{DC} vs Duty Cycle

In addition to P_{DC}, the power driving a capacitive load is given approximately by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L \qquad (4)$$

where:

f = Operating frequency

C_L = Load capacitance

Graphical solutions for P_{AC} are illustrated in *Figure 2.* Thus, any type of clock driver will dissipate internally 290 mW per MHz per thousand pF of load. At 5 MHz, this would be 1.5W for a 1000 pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.

Combining equations (1), (2), (3) and (4) yields a criterion for the maximum load capacitance which can be driven by a given driver:

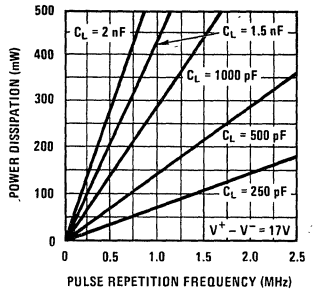


FIGURE 2. P_{AC} vs PRF

$$C_L \leq \frac{1}{f}\left[\frac{P_{MAX}}{n\,(V^+ - V^-)^2} - \frac{(DC)}{Req}\right] \qquad (5)$$

As an example, the DS0025CN can dissipate 890 mW at T_A = 70°C when soldered to a printed circuit board. Req is approximately equal to 1k. For V^+ = 5V, V^- = −12V, f = 1 MHz, and dc = 20%, C_L is:

$$C_L \leq \frac{1}{10^6}\left[\frac{(890 \times 10^{-3})}{(2)\,(17)^2} - \frac{0.2}{1 \times 10^3}\right]$$

$$C_L \leq 1340 \text{ pF (each driver)}$$

A typical application might involve driving an MM5013 triple 64-bit shift register with the DS0025. Using the conditions above and the clock line capacitance of the MM5013 of 60 pF, a single DS0025 can drive 1340 pF/60 pF, or 00 MM5013's.

In summary, the maximum capacitive load that any clock driver can drive is determined by package type and rating, heat sink technique, maximum system ambient temperature, ac power (which depends on frequency, voltage across the device, and capacitive load) and dc power (which is principally determined by duty cycle).

Rise and Fall Time Considerations

In general rise and fall times are determined by (a) clock driver design, (b) reflected effects of heavy external load, and (C) peak transient current available. Details of these are included in Appendixes I and II. *Figures AI-3, AI-4, AII-2 and AIII-3* illustrate performance under various operating conditions. Under light loads, performance is determined by internal design of the driver; for moderate loads, by load C_L being reflected (usually as $C_{L/\beta}$) into the driver, and for large loads by peak output current where:

$$\frac{\Delta V}{\Delta T} = \frac{I_{OUT\ PEAK}}{C_L}$$

Logic rise and fall times must be known in order to assure non-overlap of system timing.

Note the definition of rise and fall times in this application note follow the convention that rise time is the transition from logic "0" to logic "1" levels and vice versa for fall times. Since MOS logic is inverted from normal TTL, "rise time" as used in this note is "voltage fall" and "fall time" is "voltage rise."

Power Supply Decoupling

Although power supply decoupling is a wide spread and accepted practice, the question often arises as to how much and how often. Our own experience indicates that each clock driver should have at least 0.1μF decoupling to ground at the V^+ and V^- supply leads. Capacitors should be located as close as is physically possible to each driver. Capacitors should be non-inductive ceramic discs. This decoupling is necessary because currents in the order of 0.5 to 1.5 amperes flow during logic transitions.

There is a high current transient (as high as 1.5A) during the output transition from high to low through the V^- lead. If the external interconnecting wire from the driving circuit to the V^- lead is electrically long, or has significant dc resistance the current transient will appear as negative feedback and subtract from the switching response. To minimize this effect, short interconnecting wires are necessary and high frequency power supply decoupling capacitors are required if V^- is different from the ground of the driving circuit.

Clock Line Overshoot and Cross Talk

Overshoot: The output waveform of a clock driver can, and often does, overshoot. It is particularly evident on faster drivers. The overshoot is due to the finite inductance of the clock lines. Since most MOS registers require that clock signals not exceed V_{SS}, some method must be found in large systems to eliminate overshoot. A straightforward approach is shown in *Figure 3.* In this instance,

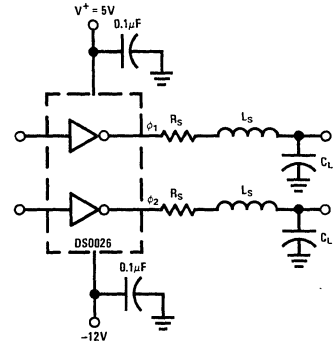


FIGURE 3. Use of Damping Resistor to Eliminate Clock Overshoot

a small damping resistor is inserted between the output of the clock driver and the load. The critical value for R_S is given by:

$$R_S = 2\sqrt{\frac{L_S}{C_L}} \qquad (6)$$

In practice, analytical determination of the value for R_S is rather difficult. However, R_S is readily determined empirically, and typical values range in value between 10 and 50Ω.

Use of the damping resistor has the added benefit of essentially unloading the clock driver; hence a greater number of loads may often be driven by a given driver. In the limit, however, the maximum value that may be used for R_S will be determined by the maximum allowable rise and fall time needed to assure proper operation of the MOS register. In short:

$$t_{r(MAX)} = t_{f(MAX)} \leq 2.2\ R_S C_L \qquad (7)$$

One last word of caution with regard to use of a damping resistor should be mentioned. The power dissipated in R_S can approach $(V^+ - V^-)^2 f C_L$ and accordingly the resistor wattage rating may be in excess of 1W. There are, obviously, applications where degradation of t_r and t_f by use of damping resistors cannot be tolerated. *Figure 4* shows a practical circuit which will limit overshoot to a diode drop. The clamp network should physically be located in the center of the distributed load in order to minimize inductance between the clamp and registers.

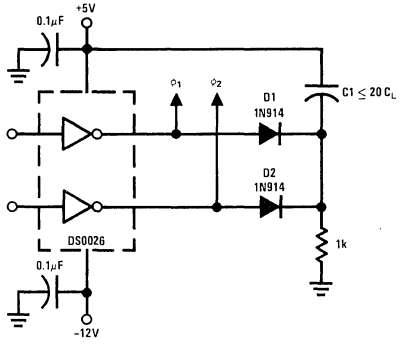


FIGURE 4. Use of High Speed Clamp to Limit Clock Overshoot

Cross Talk: Voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice versa) during the transition of ϕ_1 to MOS logic "1." The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. *Figure 5* illustrates the problem.

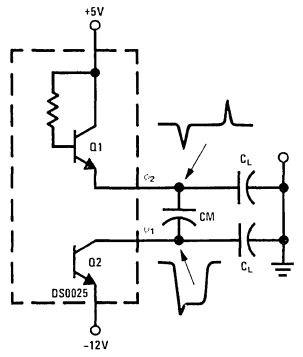


FIGURE 5. Clock Line Cross Talk

The negative going transition of ϕ_1 (to MOS logic "1") is capacitively coupled via C_M to ϕ_2. Obviously, the larger C_M is, the larger the spike. Prior to ϕ_1's transition, Q1 is "OFF" since only μA are drawn from the device.

The DS0056 connected as shown in *Figure 6* will minimize the effect of cross talk. The external resistors to the higher power supply pull the base of a Q1 up to a higher level and forward bias the collector base junction of Q1. In this bias condition the output impedance of the DS0056 is very low and will reduce the amplitude of the spikes.

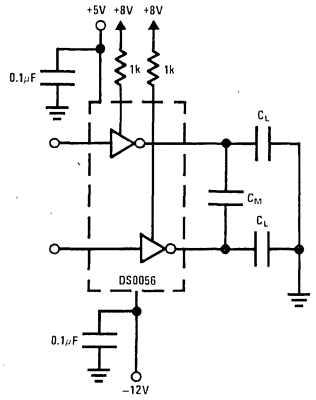


FIGURE 6. Use of DS0056 to Minimize Clock Line Cross Talk

Input Capacitive Coupling

Generally, MOS shift registers are powered from +5V and −12V supplies. A level shift from the TTL levels (+5V) to MOS levels (−12V) is therefore required. The level shift could be made utilizing a PNP transistor or zener diode. The disadvantage to dc level shifting is the increased power dissipation and propagation delay in the level shifting device. Both the DS0025, DS0026 and DS0056 utilize input capacitors when level shifting from

TTL to negative MOS capacitors. Not only do the capacitors perform the level shift function without inherent delay and power dissipation, but as will be shown later, the capacitors also enhance the performance of these circuits.

CONCLUSION

The practical aspects of driving MOS memories with low cost clock drivers has been discussed in detail. When the design guide lines set forth in this paper are followed and reasonable care is taken in circuit layout, the DS0025, DS0026 and DS0056 provide superior performance for most MOS input interface applications.

REFERENCES

1. Bert Mitchell, *"New MOS Clock Driver for MOS Shift Registers,"* National Semiconductor, AN-18, March 1969.

2. John Vennard, *"MOS Clock Drivers,"* National Semiconductor, MB-9, December 1969.

3. Dale Mrazek, *"MOS Delay Lines,"* National Semiconductor, AN-25, April 1969.

4. Dale Mrazek, *"MOS Clock Savers,"* National Semiconductor, MB-5.

5. Dale Mrazek, *"Silicon Disc's Challenge Magnetic Disc Memories,"* EDN/EEE Magazine, Sept. 1971.

6. Richard Percival, *"Dynamic MOS Shift Registers Can Also Simulate Stack and Silo Memories,"* Electronics Magazine, November 8, 1971.

7. Bapat and Mrazek, *"Dynamic MOS Random Access Memory System Considerations,"* National Semiconductor, AN-50, August 1971.

8. Don Femling, *"Using the MM5704 Keyboard Interface in Keyboard Systems,"* National Semiconductor, AN-52.

APPENDIX I

DS0025 Circuit Operation

The schematic diagram of the DS0025 is shown in *Figure AI-1.* With the TTL driver in the logic "0" state Q1 is "OFF" and Q2 is "ON" and the output is at approximately one V_{BE} below the V^+ supply.

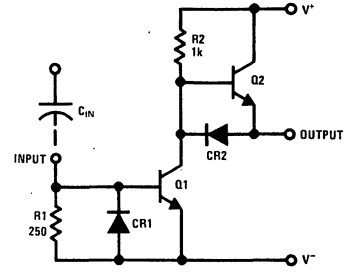


FIGURE AI-1. DS0025 Schematic (One-Half Circuit)

When the output of the TTL driver goes high, current is supplied to the base of Q1, through C_{IN}, turning it "ON." As the collector of Q1 goes negative, Q2 turns "OFF." Diode CR2 assures turn-on of Q1 prior to Q2's turn-off minimizing current spiking on the V^+ line, as well as providing a low impedance path around Q2's base emitter junction.

The negative voltage transition (to MOS logic "1") will be quite linear since the capacitive load will force Q1 into its linear region until the load is discharged and Q1 saturates. Turn-off begins when the input current decays to zero or the output of the TTL driver goes low. Q1 turns "OFF" and Q2 turns "ON" charging the load to within a V_{BE} of the V^+ supply.

Rise Time Considerations

The logic rise time (voltage fall) of the DS0025 is primarily a function of the ac load, C_L, the available input current and total voltage swing. As shown in *Figure AI-2,*

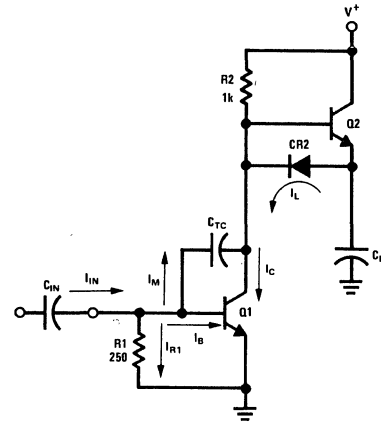


FIGURE AI-2. Rise Time Model for the DS0025

the input current must charge the Miller capacitance of Q1, C_{TC}, as well as supply sufficient base drive to Q1 to discharge C_L rapidly. By inspection:

$$I_{IN} = I_M + I_B + I_{R1} \qquad \text{(AI-1)}$$

$$I_{IN} \cong I_M + I_B, \text{ for } I_M >> I_{R1} \text{ \& } I_B >> I_{R1}$$

$$I_B = I_{IN} - C_{TC} \frac{\Delta V}{\Delta t} \qquad \text{(AI-2)}$$

If the current through R2 is ignored,

$$I_C = I_B h_{FEQ1} = I_L + I_M \qquad \text{(AI-3)}$$

where:

$$I_L = C_L \frac{\Delta V}{\Delta t}$$

Combining equations AI-1, AI-2, AI-3 yields:

$$\frac{\Delta V}{\Delta t}[C_L + C_{TC}(h_{FEQ1} + 1)] = h_{FEQ1} I_{IN} \qquad \text{(AI-4)}$$

or

$$t_r \cong \frac{[C_L + (h_{FEQ1} + 1)C_{TC}]\ \Delta V}{h_{FEQ1}\ I_{IN}} \qquad \text{(AI-5)}$$

Equation (AI-5) may be used to predict t_r as a function of C_L and ΔV. Values for C_{TC} and h_{FE} are 10 pF and 25 respectively. For example, if a DM7440 with peak output current of 50 mA were used to drive a DS0025 loaded with 1000 pF, rise times of:

$$\frac{(1000\text{ pF} + 250\text{ pF})\ (17\text{V})}{(50\text{ mA})\ (20)}$$

or 21 ns may be expected for $V^+ = 5.0$V, $V^- = -12$V, *Figure AI-3* gives rise time for various values of C_L.

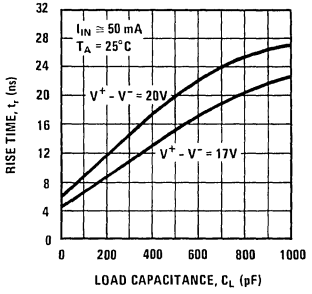


FIGURE AI-3. Rise Time vs C_L for the DS0025

Fall Time Considerations

The MOS logic fall time (voltage rise) of the DS0025 is dictated by the load, C_L, and the output capacitance of Q1. The fall time equivalent circuit of DS0025 may be approximated with the circuit of *Figure AI-4.* In actual

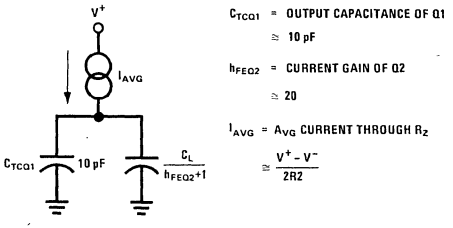


FIGURE AI-4. Fall Time Equivalent Circuit

practice, the base drive to Q2 drops as the output voltage rises toward V^+. A rounding of the waveform occurs as the output voltage reaches to within a volt of V^+. The result is that equation (AI-7) predicts conservative values of t_f for the output voltage at the beginning of the voltage rise and optimistic values at the end. *Figure AI-5* shows t_f as function of C_L.

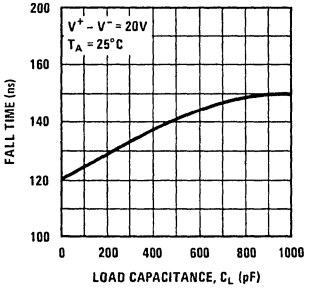


FIGURE AI-5. DS0025 Fall Time vs C_L

Assuming h_{FE2} is a constant of the total transition:

$$\frac{\Delta V}{\Delta t} = \frac{\left(\frac{V^+ - V^-}{2R2}\right)}{C_{TCQ1} + C_L/h_{FEQ1+1}} \qquad \text{(AI-6)}$$

or

$$t_f \cong 2R2\left(C_{TCQ1} + \frac{C_L}{h_{FEQ+1}}\right) \qquad \text{(AI-7)}$$

DS0025 Input Drive Requirements

Since the DS0025 is generally capacitively coupled at the input, the device is sensitive to current not input voltage. The current required by the input is in the 50–60 mA region. It is therefore a good idea to drive the DS0025 from TTL line drivers, such as the DM7440 or DM8830. It is possible to drive the DS0025 from standard 54/74 series gates or flip-flops but t_{ON} and t_r will be somewhat degraded.

Input Capacitor Selection

The DS0025 may be operated in either the logically controlled mode (pulse width out ≅ pulse width in) or C_{IN} may be used to set the output pulse width. In the latter mode a long pulse is supplied to the DS0025.

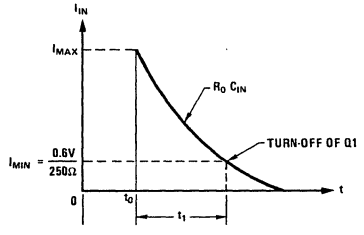


FIGURE AI-6. DS0025 Input Current Waveform

The input current is of the general shape as shown in *Figure AI-6*. I_{MAX} is the peak current delivered by the TTL driver into a short circuit (typically 50–60 mA). Q1 will begin to turn-off when I_{IN} decays below V_{BE}/R1 or about 2.5 mA. In general:

$$I_{IN} = I_{MAX}\, e^{-t/R0}\, C_{IN} \qquad \text{(AI-8)}$$

where:

R0 = Output impedance of the TTL driver

C_{IN} = Input coupling capacitor

Substituting $I_{IN} = I_{MIN} = \frac{V_{BE}}{R1}$ and solving for t_1 yields:

$$t_1 = R0C_{IN}\ \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-9)}$$

The total pulse width must include rise and fall time considerations. Therefore, the total expression for pulse width becomes:

$$t_{PW} \cong \frac{t_r + t_f}{2} + t_1$$

$$= \frac{t_r + t_f}{2} + R0C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-10)}$$

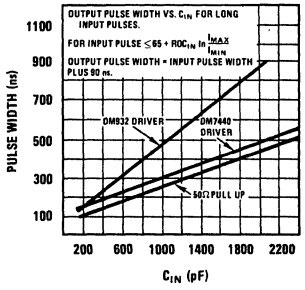


FIGURE AI-7. Output PW Controlled by C_{IN}

The logic "1" output impedance of the DM7440 is approximately 65Ω and the peak current (I_{MAX}) is about 50 mA. The pulse width for C_{IN} = 2,200 pF is:

$$t_{PW} \cong \frac{25\text{ ns} + 150\text{ ns}}{2} + (65\Omega)(2200\text{ pF})\ \ln$$

$$\frac{50\text{ mA}}{2.5\text{ mA}} = 517\text{ ns}$$

A plot of pulse width for various types of drivers is shown in *Figure AI-7*. For applications in which the output pulse width is logically controlled, C_{IN} should be chosen 2 to 3 times larger than the maximum pulse width dictated by equation (AI-10).

DC Coupled Operation

The DS0025 may be direct-coupled in applications when level shifting to a positive value only. For example, the MM1103 RAM typically operates between ground and +20V. The DS0025 is shown in *Figure AI-8* driving the addres or precharge line in the logically controlled mode.

If DC operation to a negative level is desired, a level translator such as the DS7800 or DH0034 may be employed as shown in *Figure AI-9*. Finally, the level shift may be accomplished using PNP transistors are shown in *Figure AI-10*.

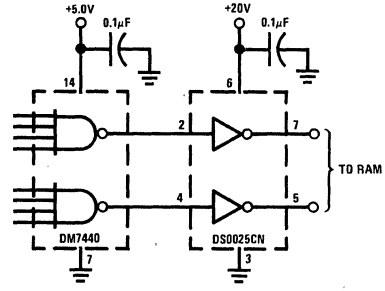


FIGURE AI-8. DC Coupled DS0025 Driving 1103 RAM

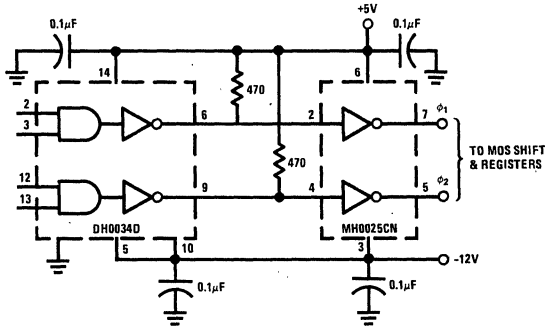


FIGURE AI-9. DC Coupled Clock Driver Using DH0034

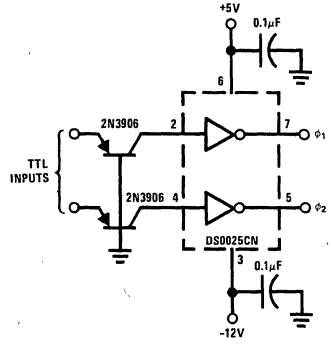


FIGURE AI-10. Transistor Coupled DS0025 Clock Driver

APPENDIX II

DS0026 Circuit Operation

The schematic of the DS0026 is shown in *Figure AII-1*. The device is typically ac coupled on the input and responds to input current as does the DS0025. Internal current gain allows the device to be driven by standard TTL gates and flip-flops.

With the TTL input in the low state Q1, Q2, Q5, Q6 and Q7 are "OFF" allowing Q3 and Q4 to come "ON." R6 assures that the output will pull up to within a V_{BE} of V^+ volts. When the TTL input starts toward logic "1," current is supplied via C_{IN} to the bases of Q1 and Q2 turning them "ON." Simultaneously, Q3 and Q4 are snapped "OFF." As the input voltage rises (to about 1.2V), Q5 and Q6 turn-on. Multiple emitter transistor Q5 provides additional base drive to Q1 and Q2 assuring their complete and rapid turn-on. Since Q3 and Q4 were rapidly turned "OFF" minimal power supply current spiking will occur when Q7 comes "ON."

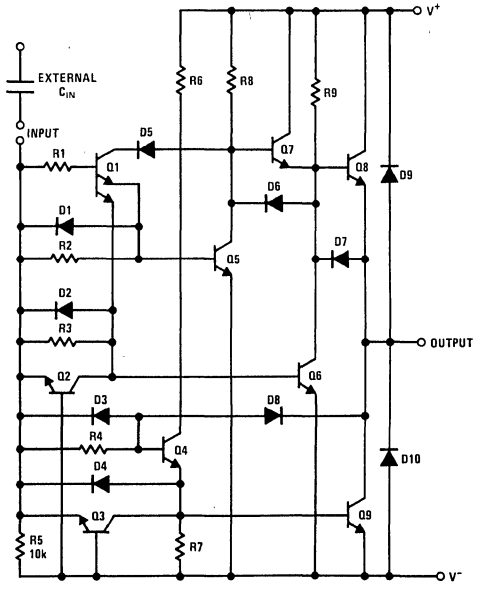


FIGURE AII-1. DS0026 Schematic (One-Half Circuit)

Q6 now provides sufficient base drive to Q7 to turn it "ON." The load capacitance is then rapidly discharged toward V^-. Diode D4 affords a low impedance path to Q6's collector which provides additional drive to the load through current gain of Q7. Diodes D1 and D2 prevent avalanching Q3's and Q4's base-emitter junction as the collectors of Q1 and Q2 go negative. The output of the DS0026 continues negative stopping about 0.5V more positive than V^-.

When the TTL input returns to logic "0," the input voltage to the DS0026 goes negative by an amount proportional to the charge on C_{IN}. Transistors Q8 and Q9 turn-on, pulling stored base charge out of Q7 and Q2 assuring their rapid turn-off. With Q1, Q2, Q6 and Q7 "OFF," Darlington connected Q3 and Q4 turn-on and rapidly charge the load to within a V_{BE} of V^+.

Rise Time Considerations

Predicting the MOS logic rise time (voltage fall) of the DS0026 is considerably involved, but a reasonable approximation may be made by utilizing equation (AI-5), which reduces to:

$$t_r \cong [C_L + 250 \times 10^{-12}]\ \Delta V \qquad \text{(AII-1)}$$

For C_L = 1000 pF, V^+ = 5.0V, V^- = −12V, $t_r \cong$ 21 ns. *Figure AII-2* shows DS0026 rise times vs C_L.

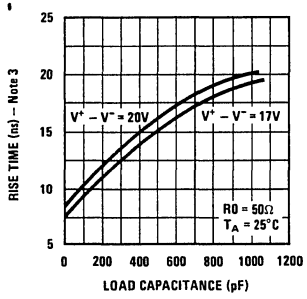


FIGURE AII-2. Rise Time vs Load Capacitance

Fall Time Considerations

The MOS logic fall time of the DS0026 is determined primarily by the capacitance Miller capacitance of Q5 and Q1 and R5. The fall time may be predicted by:

$$t_f \cong (2.2)(R5)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \cong (4.4 \times 10^3)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \qquad \text{(AII-2)}$$

where:

C_S = Capacitance to ground seen at the base of Q3

= 2 pF

$h_{FE}{}^2 = (h_{FEQ3} + 1)(h_{FEQ4} + 1)$

$\cong$ 500

For the values given and C_L = 1000 pF, $t_f \cong$ 17.5 ns. *Figure AII-3* gives t_f for various values of C_L.

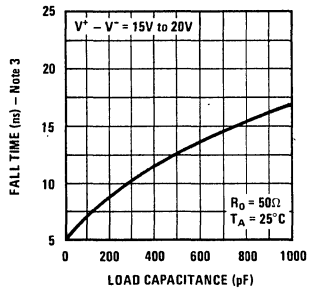


FIGURE AII-3. Fall Time vs Load Capacitance

DS0026 Input Drive Requirements

The DS0026 was designed to be driven by standard 54/74 elements. The device's input characteristics are shown in *Figure AII-4*. There is breakpoint at $V_{IN} \cong 0.6V$ which corresponds to turn-on of Q1 and Q2. The input current then rises with a slope of about 600Ω (R2 || R3) until a second breakpoint at approximately 1.2V is encountered, corresponding to the turn-on of Q5 and Q6. The slope at this point is about 150Ω (R1 || R2 || R3 || R4).

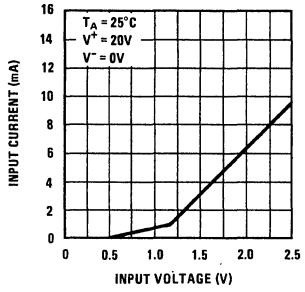


FIGURE AII-4. Input Current vs Input Voltage

The current demanded by the input is in the 5–10 mA region. A standard 54/74 gate can source currents in excess of 20 mA into 1.2V. Obviously, the minimum "1" output voltage of 2.5V under these conditions cannot be maintained. This means that a 54/74 element must be dedicated to driving 1/2 of a DS0026. As far as the DS0026 is concerned, the current is the determining turn-on mechanism not the voltage output level of the 54/74 gate.

Input Capacitor Selection

A major difference between the DS0025 and DS0026 is that the DS0026 requires that the output pulse width be logically controlled. In short, the input pulse width ≅ output pulse width. Selection of C_{IN} boils down to choosing a capacitor small enough to assure the capacitor takes on nearly full charge, but large enough so that the input current does not drop below a minimum level to keep the DS0026 "ON." As before:

$$t_1 = R0C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AII-3)}$$

or

$$C_{IN} = \frac{t_1}{R0 \ln \frac{I_{MAX}}{I_{MIN}}} \qquad \text{(AII-4)}$$

In this case R0 equals the sum of the TTL gate output impedance plus the input impedance of the DS0026 (about 150Ω). I_{MIN} from *Figure AII-5* is about 1 mA. A standard 54/74 series gate has a high state output impedance of about 150Ω in the logic "1" state and an output (short circuit) current of about 20 mA into 1.2V. For an output pulse width of 500 ns,

$$C_{IN} = \frac{500 \times 10^{-9}}{(150\Omega + 150\Omega) \ln \frac{20\text{ mA}}{1\text{ mA}}} = 560\text{ pF}$$

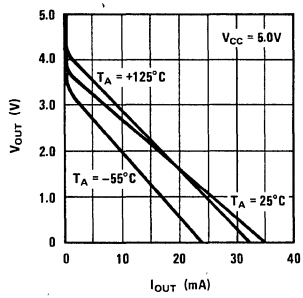


FIGURE AII-5. Logical "1" Output Voltage vs Source Current

In actual practice it's a good idea to use values of about twice those predicted by equation (AII-4) in order to account for manufacturing tolerances in the gate, DS0026 and temperature variations.

A plot of optimum value for C_{IN} vs desired output pulse width is shown in *Figure AII-6*.

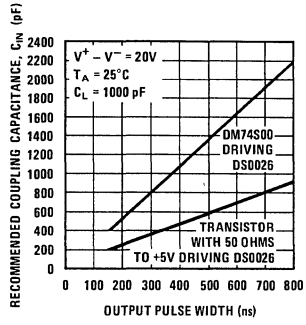


FIGURE AII-6. Suggested Input Capacitance vs Output Pulse Width

DC Coupled Applications

The DS0026 may be applied in direct coupled applications. *Figure AII-7* shows the device driving address or pre-charge lines on an MM1103 RAM.

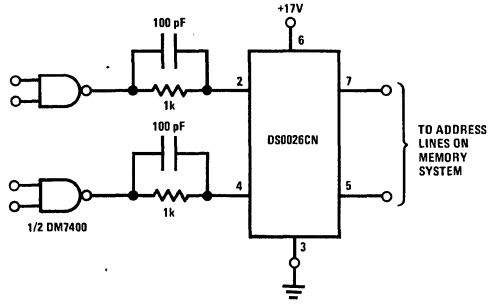


FIGURE AII-7. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

For applications requiring a dc level shift, the circuit of *Figure AII-8 or AII-9* are recommended.

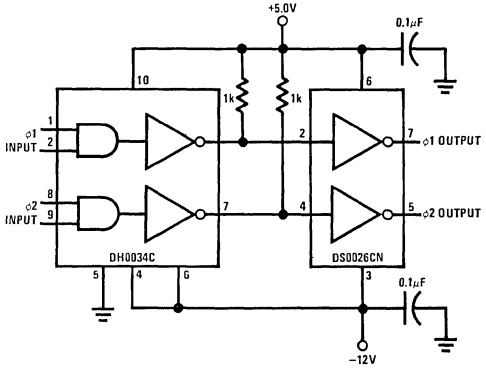


FIGURE AII-8. Transistor Coupled MOS Clock Driver

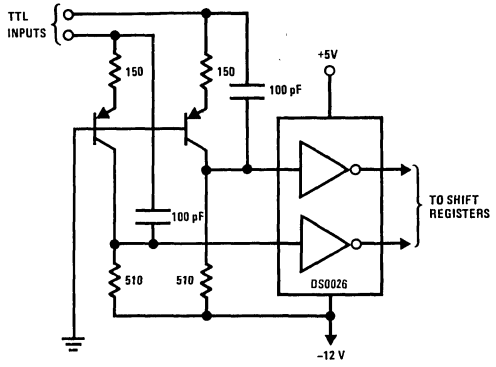


FIGURE AII-9. DC Coupled MOS Clock Driver

APPENDIX III

MOS Interface Circuits

MOS Clock Drivers

MH0007	Direct coupled, single phase, TTL compatible clock driver.
MH0009	Two phase, direct or ac coupled clock driver.
MH0012	10 MHz, single phase direct coupled clock driver.
MH0013	Two phase, ac coupled clock driver.
DS0025C	Low cost, two phase clock driver.
DS0026C	Low cost, two phase, high speed clock driver.
DS3671	Dual bootstrapped MOS driver.
DS3674	Quad MOS clock driver.
DS75361	Dual TTL-to-MOS driver.
DS75365	Quad TTL-to-MOS driver.

MOS RAM Memory Address and Precharge Drivers

DS0025C	Dual address and precharge driver.
DS0026C	Dual high speed address and precharge driver.

TTL to MOS Interface

DH0034	Dual high speed TTL to negative level converter.
DS8800	Dual TTL to negative level converter.
DS8810/DS8812/ DS8819	Open collector TTL to positive high level MOS converter gates.
DS88L12	Active pull-up TTL to positive high level MOS converter gates.
DS3645/DS3675	Hex TRI-STATE® MOS driver.
DS3647/DS3677	Quad TRI-STATE MOS driver I/O register.
DS3648/DS3678	TRI-STATE MOS driver multiplexer.
DS3649/DS3679	Hex TRI-STATE MOS driver.
DS36149/DS36179	Hex TRI-STATE MOS driver.

MOS to TTL Converters and Sense Amps

DS75107, DS75207	Dual sense amp for MM1103 1k MOS RAM memory.

Voltage Regulators for MOS Systems

LM309, LM340 Series	Positive regulators.
LM320 Series	Negative regulators.
LM325 Series	Dual +/− regulators.

Section 7
Dynamic Memory Support

7

The DP8400 Family of Memory Interface Circuits

National Semiconductor
Application Note 302
Charles Carinalli
Mike Evans
March 1983

INTRODUCTION

The rapid development in dynamic random access memory (DRAM) chip storage capability, coupled with significant component cost reductions, has allowed designers to build large memory arrays with high performance specifications. However, the development of memory arrays continues to have a common set of problems generated by the complex timing and refresh requirements of DRAMs. These include: how to quickly drive the memories to take advantage of their speed, minimization of board space required by the support circuitry and the need for error detection and correction. Unfortunately, these problems must be addressed with each new system design. Full system solutions will vary greatly, depending on the DRAM array size, memory speed, and the processor.

This application note introduces a complete family of DRAM support circuits that provides a straightforward solution to the above problems while allowing a high degree of flexibility in application with little or no performance penalty. The DP8400 family (Table I) includes DRAM controllers, an expandable error detection/correction circuit, octal address buffers and system control circuits. The LSI blocks are designed with flexible interfaces, making application possible with all existing DRAMs including the recently announced 256Ks. Additionally, interface is easy to all popular microprocessors with memory word widths possible from 8 to 80 bits.

TABLE I. DP8400 FAMILY MEMBERS

DP8400	Expandable Error Checker/Corrector
DP8408, DP8409	DRAM Controllers
DP84240, DP84244	DRAM Buffer Drivers
DP84300 Series	Microprocessor Interface Circuits

FULL FUNCTION DRAM CONTROLLER

The heart of any DRAM array design is the controller function. Previous LSI controllers supplied a minimum function of address multiplexing with an on-board refresh counter. This required external delay line timing and logic to control memory access, additional logic to perform memory refresh, and external drivers to drive the capacitive memory array. The complete solution results in significant access delay in relation to DRAM speeds and skews in output sequencing, as well as a large component count.

A previous LSI solution brought much of this logic on-chip. However, it is limited in application to certain microprocessors and has the disadvantage of all access timing originating from an external clock, whose phase uncertainty generates a delay in actually knowing when an access has started.

The DP8409 multi-mode dynamic RAM controller/driver is the first controller to resolve all of these problems. This Schottky bipolar device provides the flexibility of external access control, along with automatic access timing generation, without the need for an external timing generator clock. In addition, on-board capacitive drivers allow direct drive for over 88 DRAMs. With the simple addition of refresh clocks, the circuit can perform hidden refresh automatically. But possibly one of the DP8409's most important advantages is its upgradability for use with 256K DRAMs.

All Control On-Chip

Figure 1 is a block diagram of the DP8409. The ADS input strobes the parallel memory address into the row latches R0-8, the column latches C0-8, and bank select B0 and B1. The nine output drivers may be multiplexed between the row or column input latches, or the 9-bit on-chip refresh counter. One of four $\overline{RAS}$ outputs is selected during an access cycle by setting the bank select inputs B0 or B1. All four $\overline{RAS}$ outputs are active during refresh. Either external or automatic control is available on-chip for the $\overline{CAS}$ output, while an on-chip buffer is provided to minimize skew associated with $\overline{WE}$ output generation.

All DRAM address and control outputs on the DP8409 can directly drive in excess of 500 pF, or the equivalent of 88 DRAMs (4 banks of 22 DRAMs). All output drivers are closely matched, significantly reducing output skew. Each output stage has symmetrical high and low logic level drive capability, insuring matched rise and fall time characteristics.

Flexibility and Upgradability to 256K

The 9 multiplexed address outputs and 9-bit internal refresh counter of the DP8409 not only guarantee its use with all current DRAMs (16K and 64Ks), but also enable direct addressing capability for the forthcoming 256K DRAMs. Careful design of memory boards, using the current 64K DRAMs with the DP8409, will insure direct upgradability to 256K DRAMs. This can be done by simply allowing for board address extension by two bits and designing the ninth address trace (Q8) of the DP8409 to connect to pin 1 of the DRAMs (A8). This is, in general, a nonconnected pin in 64Ks and the ninth address in 256Ks. All that need be done is to remove the 64Ks and replace them with 256Ks, thereby increasing the memory on the same board by a 4 to 1 ratio. The resulting development cost saving can be significant.

Three mode pins (M0, M1 and M2) offer externally selectable modes of operation, a key reason for the DP8409's application flexibility (Table II). The operational modes are divided between external and automatic memory control. Modes 0, 3b, and 4 provide full control of access and refresh for systems with external memory controllers or for special purpose applications. Here all timing can be directly controlled by the external system as shown in *Figure 2.*

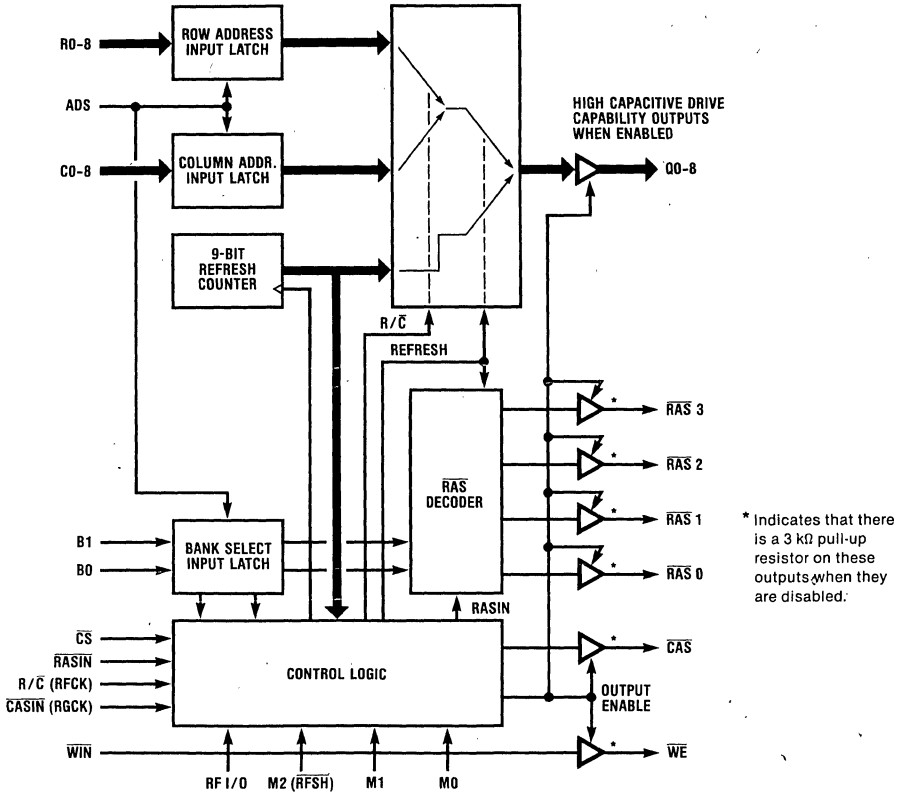


FIGURE 1. DP8409 Block Diagram

TABLE II. DP8409 MODE SELECT OPTIONS

Mode	(RFSH) M2	M1	M0	Mode of Operation	Conditions
0	0	0	0	Externally Controlled Refresh	RF I/O = EOC
1	0	0	1	Auto Refresh—Forced	RF I/O = Refresh Request (RFRQ)
2	0	1	0	Internal Auto Burst Refresh	RF I/O = EOC
3a	0	1	1	All RAS Auto Write	RF I/O = EOC
3b	0	1	1	Externally Controlled All RAS Access	All RAS Active
4	1	0	0	Externally Controlled Access	
5	1	0	1	Auto Access, Slow t_{RAH}, Hidden Refresh	
6	1	1	0	Auto Access, Fast t_{RAH}	
7	1	1	1	Set End of Count	

Modes 1, 5 and 6 provide on-chip automatic access sequencing with hidden refresh capability. A graphic example of the automatic access modes of the DP8409 is shown in *Figure 3*. All DRAM access timing and control is generated from one input strobe, RASIN; no external clock is required. On-chip delays insure proper address and control sequencing once the valid parallel address is presented to the fall-through input latches of the DP8409. When the RASIN transitions high-to-low, the decoded RAS output transitions low, strobing the row address into the DRAM array. An on-chip delay automatically generates a guaranteed selectable (mode 5 or 6) row address hold time. At this point, the DP8409 switches the address outputs from the row latch to the column latch. Then another on-chip delay generates a guaranteed column address set-up time before CAS, so that the CAS output automatically strobes the column address into the DRAM array. Read or write cycles are controlled by the system through independent control of the WE buffer that is provided on-chip to minimize delay skewing. The automatic access mode makes the dynamic RAM appear static with respect to access timing. In this mode, only one signal, RASIN, is needed after valid parallel addresses are presented to the DP8409 to initiate proper access sequencing. Access timing (RASIN to CAS), with full output loading of 88 DRAMs in the auto access mode, is determined by the dash number given on the DP8409 data sheet. All performance characteristics are specified over the full operating temperature and supply ranges.

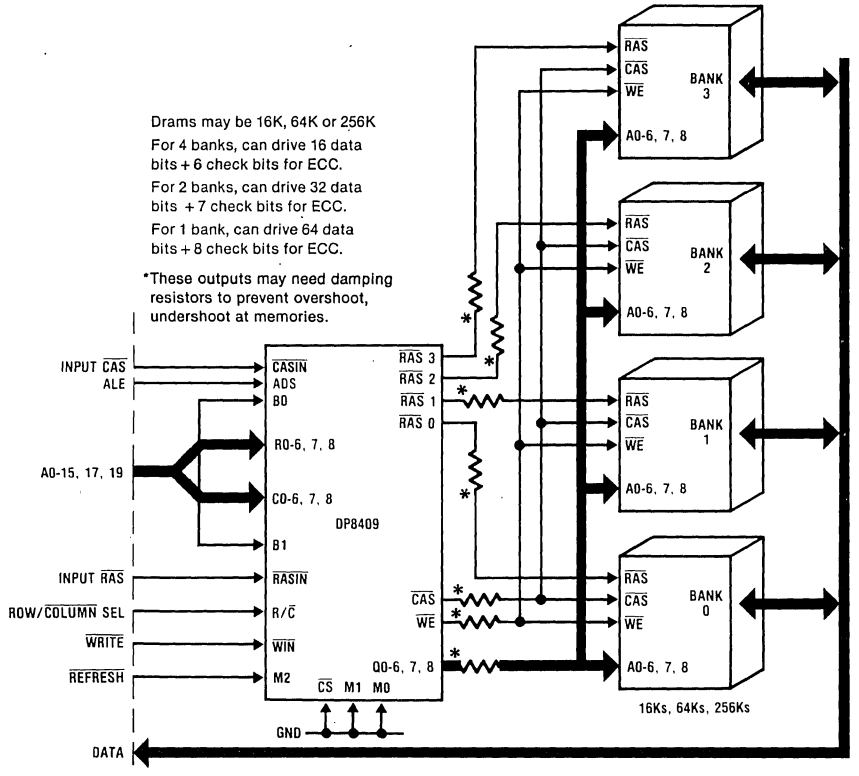


FIGURE 2. Typical Application of DP8409 Using External Control and Refresh in Modes 0 and 4

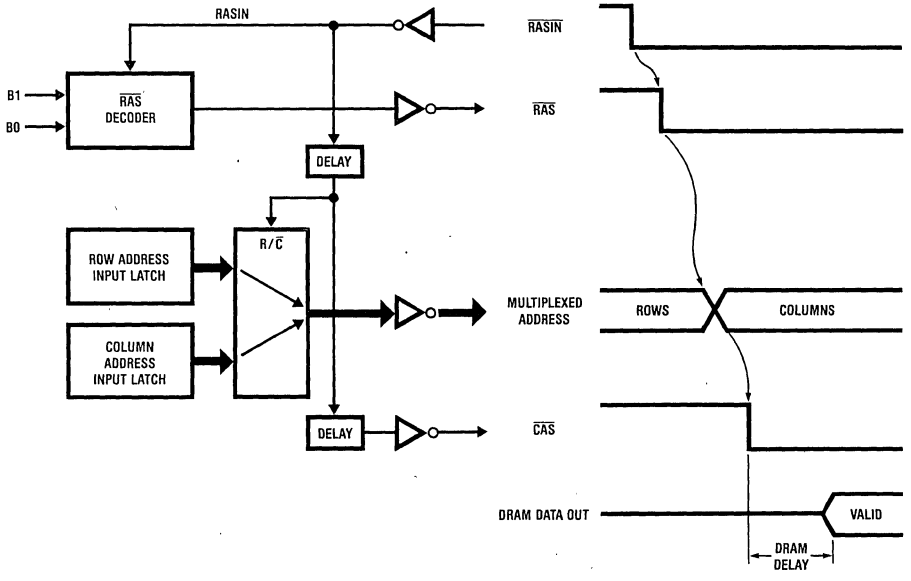


FIGURE 3. This figure demonstrates the automatic accessing capability of the DP8409. Only one strobing edge, RASIN, is required for generation of all DRAM access timing signals. This is accomplished with on-chip delay generators, eliminating the need for external delay lines. No access timing clock is necessary.

Refreshing

The DP8409 also provides hidden refresh capability while in one of the automatic access modes *(Figure 4)*. In this mode, it will automatically perform a refresh without the system being interrupted. To do this, the DP8409 requires two clock signals, refresh clock (RFCK) which defines the refresh period (usually 16 μs), and $\overline{RAS}$ generator clock (RGCK), which is typically the microprocessor clock.

Highest priority is given to hidden refreshing through use of level sensing of RFCK. A refresh cycle begins when RFCK transitions to a high level. If during the time RFCK is high the DP8409 is deselected ($\overline{CS}$ in the high state) and the processor is accessing another portion of the system such as another memory segment, or ROM, or a peripheral, then a hidden refresh is performed. When a read or write cycle is initiated by the processor, the $\overline{RASIN}$ input on the DP8409 transitions low. With $\overline{CS}$ high, this causes the present state of the internal refresh counter to be placed on the address outputs, followed by the four $\overline{RAS}$ outputs transitioning low, strobing the refresh address into the DRAM array. When the cycle ends, $\overline{RASIN}$ will terminate, thus forcing the $\overline{RAS}$ outputs back to their inactive state and ending the hidden refresh. The refresh counter is then incremented and another microprocessor cycle can begin immediately. However, to save power, the DP8409 will allow only one hidden refresh to occur during a given RFCK cycle.

In the event that a hidden refresh does not occur, the DP8409 must force a refresh before the RFCK's next positive-going transition. The system is notified after the negative-going RFCK transition that a hidden refresh has not occurred, via the refresh request output (RF I/O pin). The system acknowledges the request for a forced refresh by setting M2 (refresh) low on the DP8409 and preventing further access to the DP8409. The DP8409 then uses RGCK to generate an automatic forced refresh. The refresh request pin then returns to the inactive state, and the DP8409 allows the processor to take full system control after the forced refresh has been completed.

OCTAL MEMORY DRIVERS

When the memory array becomes large and the 88-DRAM drive capability of the DP8409 becomes insufficient, additional address and control buffers are required. However, like any other element in a DRAM system, selection of the improper driver can have significant impact on system performance.

In the past, this function has been performed using Schottky logic family circuits such as the DM74S240 octal inverter or the DM74S244 octal buffer. The output stages of these devices have good drive capability, but their performance with heavy capacitive loads is not ideal for DRAM arrays. The key disadvantage of these devices is their nonsymmetrical rise and fall time characteristics and their long propagation delays with heavy load capacitance. The former is a result of impedance mismatch in the upper and lower output stages. The latter stems from process capability and circuit design techniques not tailored to the DRAM application. The combined result of all these factors is increased output skew in address and control lines when these devices are used as buffers.

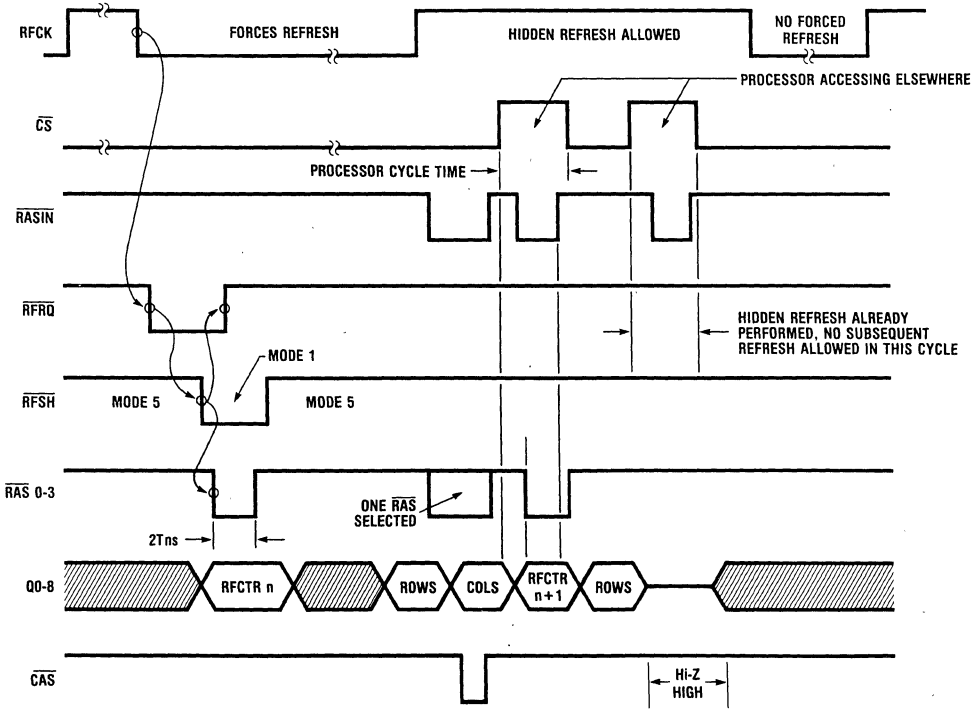


FIGURE 4. Hidden and Forced Refresh Timing of the DP8409

Two new devices are now available for this application. The DP84240 is pin and function compatible with the DM74S240. The DP84244 is likewise compatible with the DM74S244. However, this is where the similarity between the devices ends. Both the DP84240 and the DP84244 have been designed specifically to drive DRAM arrays. *Figure 5* shows a typical application of the DP84244, used in conjunction with the DP8409, to drive a very large memory array.

Figures 6a, 6b show some typical performance curves for these circuits. Note that, at over 500 pF, the propagation delay through these drivers is on the order of 15 ns. This delay includes propagation delay and rise or fall time. Even with this high speed, chip power dissipation is still maintained at a reasonable level as demonstrated by the graphs shown in *Figures 7a, 7b* of power versus frequency.

The DP84240 and the DP84244 are fabricated on a high performance oxide-isolated Schottky bipolar process. Special circuit techniques have been used to minimize internal delays and skews. Additionally, both rise and fall time characteristics track closely as a function of load capacitance. This has been accomplished through impedance matching of the upper and lower output stages. The result of these characteristics is a substantial reduction of skew in both the address and control lines to the DRAM array.

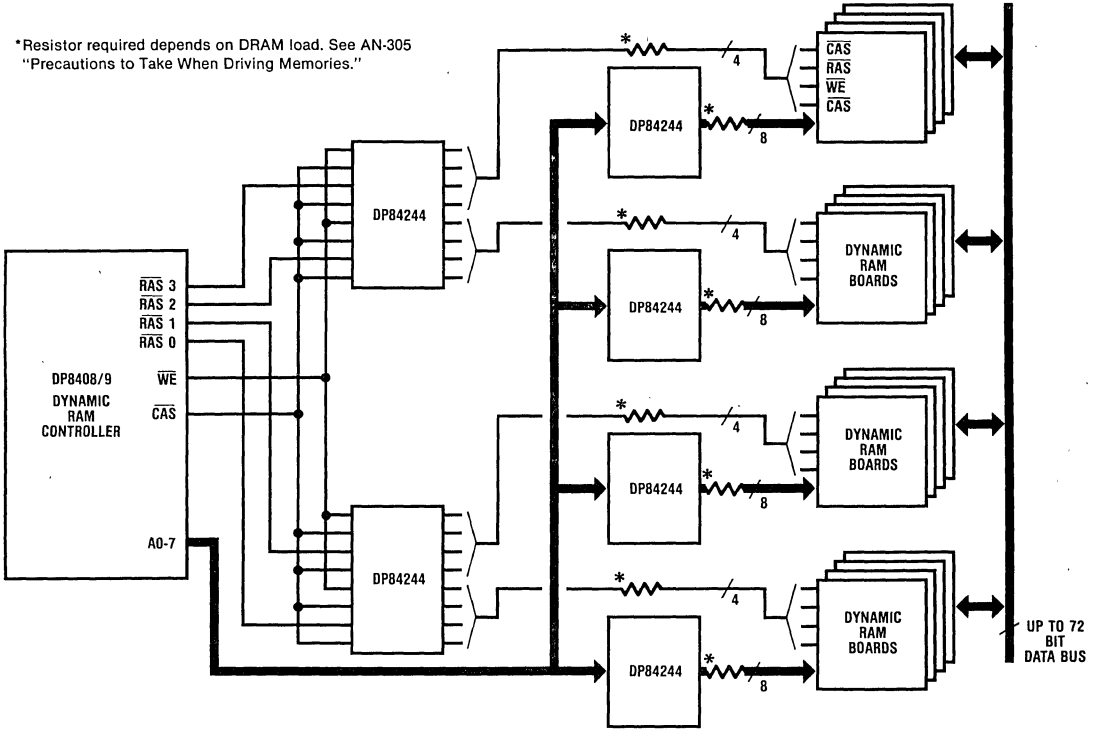


FIGURE 5. The DP84244 Used as a Buffer in a Large Memory Array (greater than 88 DRAMs) Controlled by the DP8409

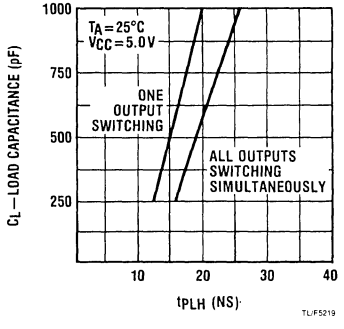


FIGURE 6a. t_{PLH} Measured to 2.7V on Output vs. C_L

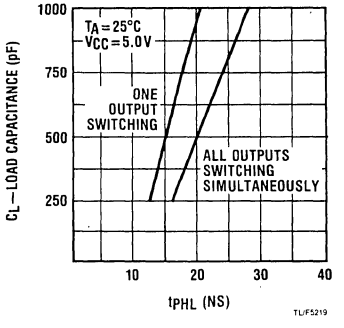


FIGURE 6b. t_{PHL} Measured to 0.8V on Output vs. C_L

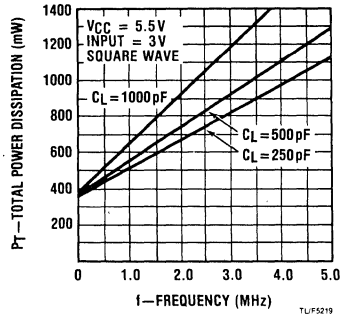


FIGURE 7a. Typical Power Dissipation for DP84240 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

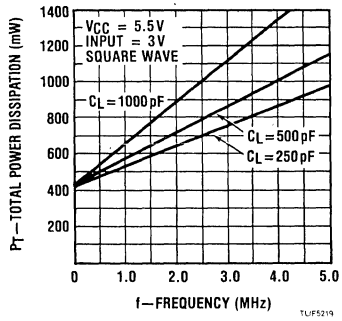


FIGURE 7b. Typical Power Dissipation for DP84244 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

The output stages of the DP84240 and the DP84244, although well matched, are relatively low impedance. Output impedance is under 10Ω. Some DRAM arrays will require the addition of damping resistors in series with the outputs of the drivers. These damping resistors are used to minimize undershoot which may have a harmful effect on the DRAMs if allowed to become large. This undershoot is caused by the high transient currents from the drivers necessary to drive the capacitive loads. These high currents pass through a distributed inductive/capacitive circuit created by the board traces and the DRAM load, causing the undershoot.

The damping resistor has specifically not been placed on-chip because its value is dependent on the DRAM array size and board layout. In fact, address lines will quite often require a different resistor value from the DRAM control lines. The resistor must be tuned for a particular board layout since too high a resistor will produce an excessively slow edge and too low a resistor will not remove the undershoot. Values for damping resistors may vary from 15Ω to 150Ω, depending on the application. Placing any value of damping resistor on-chip, other than a value less than the minimum, severely restricts the application of these high performance circuits.

Another key advantage of both the DP84240 and the DP84244 is their low input capacitance. Previous address buffer/drivers (such as the DM74S240/244) have high input capacitance. Fast edges at the inputs of these drivers become slower and distorted due to this dynamic input capacitance. This problem must be factored as an additional delay through these drivers—a delay not shown by the data sheet specifications. Additionally, the problem becomes increasingly severe as multiple driver inputs are used in parallel for bus expansion applications.

Both the DP84240 and the DP84244 are designed to significantly reduce both static and dynamic input capacitance. When these devices are driven with standard logic circuits, no appreciable overhead delay need be added to the basic device delay specifications due to input pulse distortion.

ERROR CORRECTION

The determination of whether a DRAM system requires error correction must be resolved early in the system design. A positive answer to this question may have far-reaching impact on board development time and component cost. It is clear, however, that such a decision cannot be taken lightly.

The type and origin of errors in DRAM systems are many and can result from a number of sources (Table III). Current estimates of soft error rates due to alpha particles in 64K RAMs indicate some hope that these error rates will be similar or possibly better than those found in 16K DRAMS—but the facts are still somewhat unclear. However, it is clear that the introduction in the near future of 256K DRAMs with even smaller memory cells and greater chip densities will place a significant challenge on DRAM chip designers to keep these rates down. It is believed by some that error correction may become mandatory in future DRAM system designs. Currently, the decision to add error correction is not so straightforward. It depends on many factors, not the least of which is the end user's perception of its value to system uptime and reliability.

TABLE III. THE SOURCES AND TYPES OF MEMORY ERRORS

Error Type	Sources	System Action
Soft	• Alpha particles • System noise • Chip patterns • Power glitches	Temporary system error—may be overwritten with a low probability of repetition
Hard	• Stuck memory bit • Memory chip interface • Interface circuit failure	Permanent failure—may act as logic 1 or 0

Generally, error correction will always be found in highly reliable systems using DRAMs, such as process control equipment, banking terminals, and military systems where high data integrity and minimum downtime are priorities. However, the importance of error correction has grown substantially, to the point that it is now used as a selling feature in the vast majority of large memory-based systems. In fact, some major computer houses have adopted guidelines for use by their designers in the development of DRAM arrays. A somewhat common set has been found—if the memory array is on the order of 1/4 million bytes, then word parity should be used. This permits the detection of single bit errors but does not allow error correction. When the total memory approaches 1/2 million bytes, then double bit error detection and single bit error correction should be added.

The decision to add error correction to a system is costly, both in memory overhead and control hardware. Table IV

TABLE IV. CHECK BIT OVERHEAD FOR MULTIPLE BIT ERROR DETECTION AND SINGLE BIT ERROR CORRECTION

Number of Bits in Memory Data Word	Number of Check Bits Required	Percentage of Excess Memory
8	5	63%
16	6	38%
24	6 (7)	25% (29%)
32	7	22%
48	7 (8)	15% (17%)
64	8	13%

Note: The number stated assumes the use of the DP8400; the number in parentheses is required by other error correction circuits.

lists the number of additional memory chips required to support single bit error correction and double bit error detection as a function of the memory data word width.

This table also shows the percentage of DRAM overhead required to implement this function. Adding error correction also increases the memory access delay, since the information contained in the overhead chips must be analyzed in each read and generated in each write operation.

DP8400 Expandable Error Correction Chip

The DP8400 expandable error checker/corrector is shown in block diagram form in *Figure 8*. This circuit offers a high degree of flexibility in applications which range from 8-bit to 80-bit data words. It is a 16-bit chip that is easily expandable with the simple addition of more DP8400s for each 16-bit word increment.

Figures 9a, 9b and 9c demonstrate its basic operation in the write and read memory access cycles. *Figure 9a* shows the normal write cycle, where system data is used by the DP8400 to generate parity bits, called check bits, based on certain combinations of the data bits. This combination is defined by the DP8400's matrix shown in *Figure 10.* Whenever a '1' occurs in any row, the corresponding input data bit at the top of the column helps determine the parity for that check bit labeled at the end of the row. These check bits are written along with the data at the same memory address. Also, during a memory write cycle the DP8400 checks system byte parity. This is parity associated with the data bytes transmitted between the processor and the memory card. This is an optional feature that may prove very valuable in multiple board memory systems.

Sometime later a read will occur at this same memory address. The reading of memory data may be performed in two ways, as shown in *Figures 9b and 9c.* In the read cycle, the DP8400 uses the data read from memory and internally regenerates check bits using the same matrix. These newly generated check bits are then compared (using X-OR gates) with the check bits read from memory to detect errors. The result of this comparison is called a syndrome word. Any differences in the generated versus read check bits will result in at least one syndrome bit true. This indicates an error in either the read data or check bit field or both.

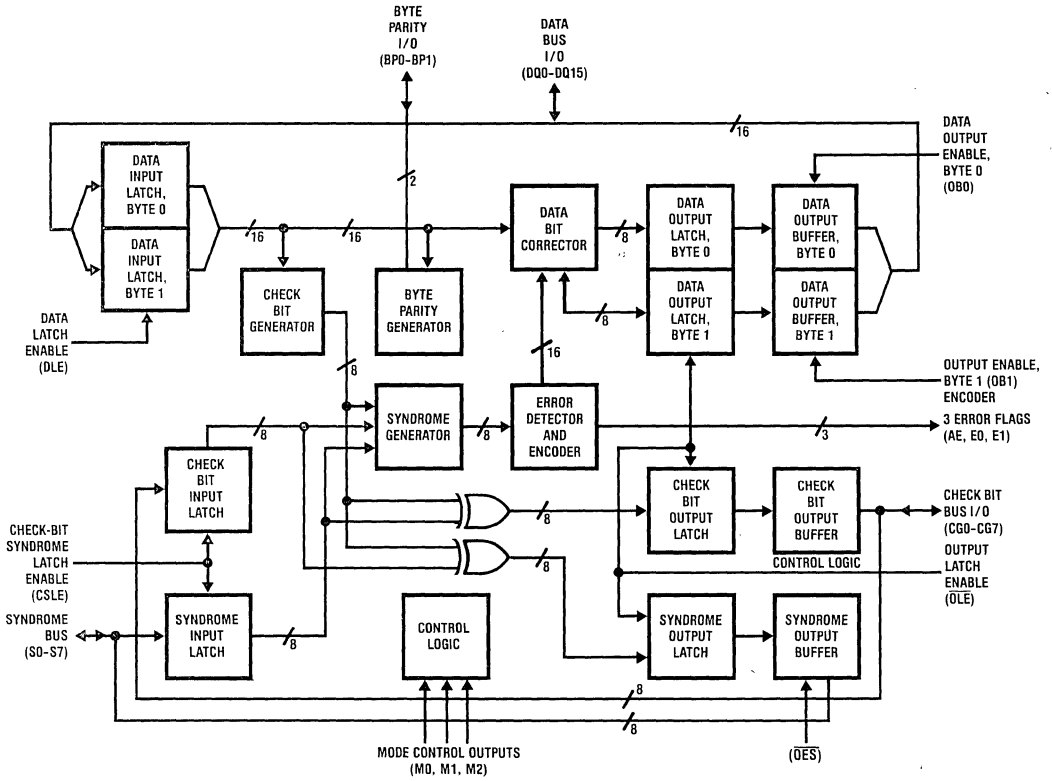


FIGURE 8. DP8400 Simplified Block Diagram

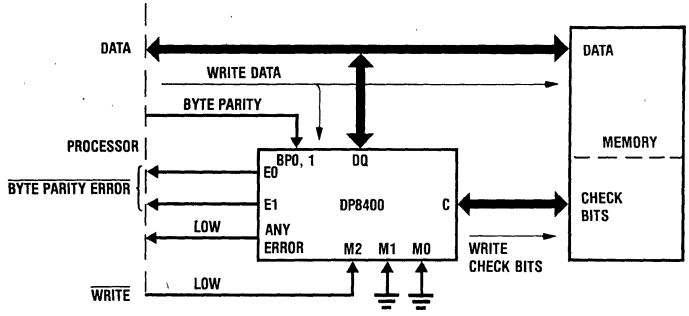


FIGURE 9a. Normal Write Mode with DP8400

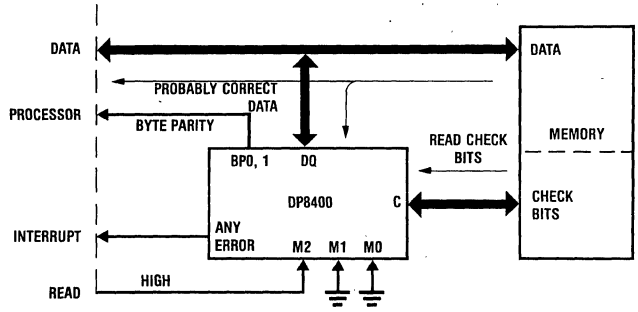


FIGURE 9b. Normal Read Mode Using the Error Monitoring Method with the DP8400

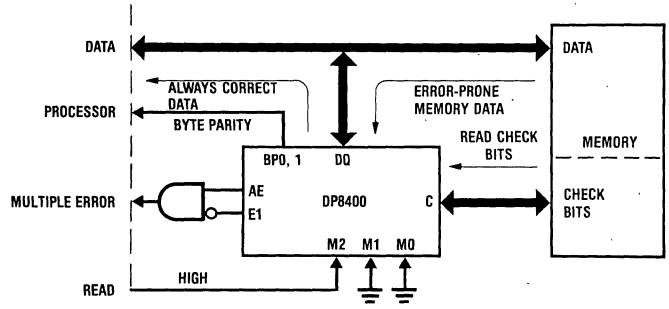


FIGURE 9c. Normal Read Mode Using the Always Correct Method with the DP8400

											1	1	1	1	1	1	DQ0-15
		0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	
		GENERATE CHECK BITS →																
GENERATED SYNDROMES	0	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0
	1	0	0	0	1	0	0	1	1	1	0	1	0	1	0	1	1	1
	2	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	2*
	3	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	3*
	4	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	4
	5	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	5
		4	8	9	7	5	1	3	9	E	B	D	3	C	7	F	F	0
		3	3	2	0	2	3	2	1	3	0	0	1	2	3	2	1	1

GENERATED CHECK BITS

HEXADECIMAL EQUIVALENT OF SYNDROME BITS

* C2, C3 generate odd parity

FIGURE 10. DP8400 Matrix

A key advantage of the DP8400 is that it has three error flags detailing the type of error occurrence. These are generated using the syndrome word in the manner shown in *Figure 11.* The resulting error type identifications are shown in Table V. The three error flags allow complete error type identification, plus the unique determination of double bit errors, which will be key during the discussion of double bit error correction. Also, on a memory read, the DP8400 generates byte parity bits for transmission to the processor along with the data.

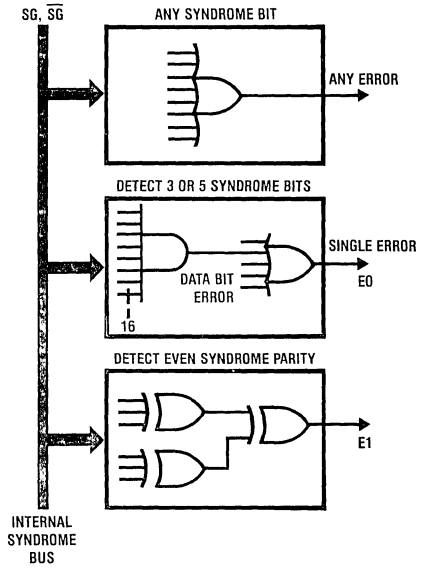


FIGURE 11. The DP8400 Error Encoder Generating 3 Error Flags

TABLE V. ERROR FLAGS AFTER NORMAL READ

AE	E1	E0	Error Type
0	0	0	No error
1	1	0	Single check bit error
1	1	1	Single data error
1	0	0	Double-bit error
All Others			Invalid conditions

There are two basic memory read methods that may be used with the DP8400. The first is shown in *Figure 9b* and is called the error monitoring method. Here, the read data is assumed to be correct and the processor immediately acts on the data. If the DP8400 detects an error, the processor is interrupted using the any error flag (AE). Using this method, there is no detection delay in most memory reads since errors seldom occur, but when an error does occur, the processor must be capable of accepting an interrupt and a read cycle extension to obtain the corrected data from the DP8400.

A second approach is called the always correct method, *Figure 9c.* In this case, the data is always assumed to be in error and the processor always waits for the DP8400 to analyze whether an error exists. Then the corrected or unchanged data is read from the DP8400. Although this method results in longer memory read time, every memory read will always be of the same delay except when a double error occurs. The selection of which method to use depends on many factors, including the processor, system structure, and performance.

Double Bit Error Correct

The probability of double bit errors in DRAM systems is relatively low, but as memory array sizes grow, the occurrence of these error types must be considered. Adopting certain practices, such as rewriting a memory location whenever an error is detected, or using "memory scrubbing" techniques, can significantly reduce the probability of a double soft error occurrence. Memory scrubbing is when the system, during low usage, actually accesses memory solely for the purpose of identifying and correcting single soft errors. This is an important technique if there are segments of the memory that are not always being accessed so that soft error occurrences would not be quickly found.

The occurrence of a double error comprising one soft and one hard must now be considered. This type of error has a higher probability than two soft errors. The hard error may be due to a catastrophic chip failure, and a subsequent soft error will create two errors. This can be a source of concern since most error correction chips cannot handle double errors of this type. Therefore, most systems will "crash" when a catastrophic chip failure is coupled with a soft error in the same memory address.

The DP8400 has been designed to handle just such an occurrence. It can correct any double bit error, as long as at least one of the errors is a hard error. The DP8400 does this without the need for extra hardware required for the basic double bit detect/single bit correct system implementation. This method is called the double complement correct technique and is demonstrated in *Figure 12* using a 4-bit data word for simplicity. In this example, a single hard error is located in the most significant bit of a particular memory location and a soft error occurs at the next bit. The position of the errors is not important since the errors may be distributed in either the data or check bit field or both. First, the data word and corresponding check bits are written to this memory location. When a later read of this location occurs, step A, two errors are directly reported by the DP8400 error flags. The system detects this, disables memory, and places the DP8400 in the complement write mode. This causes the previously read data and check bits to be complemented in the DP8400 and written back to the same memory address, step B, writing over the previous soft error. Obviously this does not modify the cell where the hard error exists. The system then reads from the same address again, but this time it places the DP8400 in the complement read mode, step C. The DP8400 again complements the memory data and check bits and generates new check bits based on the new data word. At this point, the chip detects a single bit error in the bit position where the soft error occurred, and using the conventional single error correction procedure, returns corrected data to the system, step D.

In the second read, the complement read, the hard error repeats since this bit location again receives a bit which is complemented with respect to itself. But the soft error has

been overwritten and does not repeat. Effectively, the memory has complemented the hard bit error position twice and the soft bit error position only once, while the DP8400 complements both positions twice. Therefore, after the second read, there is only one error left, the soft error. Since this is now a single error it can be directly corrected.

After the complement correct cycle, the memory must be rewritten with the corrected data since the address now contains data that is complemented. Full error reporting is available from the DP8400 after the second read, the complement read, of memory. This is shown in Table VI.

This method is a very effective tool to avoid system crash due to memory chip failure, and can do much to reduce unscheduled field service calls. The only time the system will see a double error that is not directly correctable is when a double soft error occurs. The probability of this is very low if the previously discussed techniques are used. The extra time taken to do an additional read and write of memory is insignificant when the alternative is a system that has a catastrophic failure that requires immediate field service. Using this technique, software may be provided in the system to warn the operator that the system is in a degraded operational mode and that field service should occur shortly. In the meantime, the system will continue to operate properly. The key to the effectiveness of the DP8400 in this application is its three error flags which allow complete error reporting—including a unique double error indication.

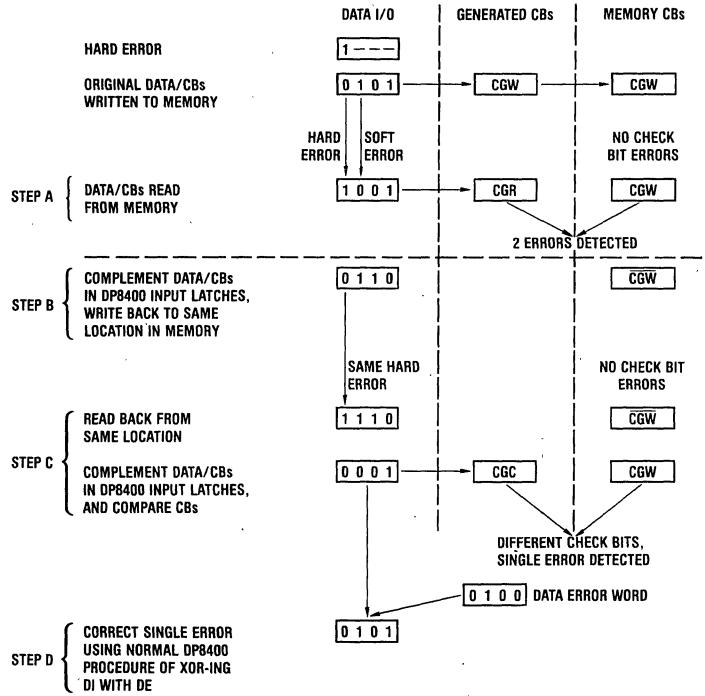


FIGURE 12. Double Error Correct Complement Hard Error Method—1 Hard Error and 1 Soft Error in Data Bits

TABLE VI. DP8400 ERROR FLAGS AFTER A COMPLEMENT READ

AE	E1	E0	Error Type
0	0	0	Two hard errors
1	1	0	One hard error, one soft check bit error
1	1	1	One hard error, one soft data bit error
1	0	0	Two soft errors, not corrected

MICROPROCESSOR INTERFACE CIRCUITS

The major 8-bit and 16-bit microprocessors have different control signal timing. There are also a number of speed options. The DP8400 family was designed, not for a specific microprocessor, but rather, significant control flexibility has been provided on both the DP8409 and the DP8400 for easy interface to any microprocessor. However, a certain amount of "glue" is necessary to interface to these LSI circuits, usually in the form of a number of MSI/SSI logic circuits,. Not only can this be costly in board space utilization, but it is usually the one place where the most design related problems occur in system development.

Figures 13 and 14 show the DP8400 family solution to this problem—the DP84300 series of microprocessor interface circuits. *Figure 13* shows how the DP84300 refresh timer and the DP843X2 microprocessor interface circuit connect to the DP8409 and various microprocesssors. *Figure 14* shows the DP8409 and the DP8400 together in a microprocessor-based memory system using DRAMs, with double bit error detect and single bit error correct capability. In addition, it shows that with the simple addition of some standard data buffers, how the system can implement byte writing to the DRAM array.

This system structure requires the insertion of few or no wait states during a memory access cycle, thus maximizing throughput. The DP84300 circuits have been designed to work with the DP8409 to control refreshing so that system throughput is affected only when absolutely necessary. First, in any refresh clock period of 16 μs, hidden refreshing is given maximum opportunity. This can be helped with the optional DP84300 refresh interval generator which offers maximum high-to-low ratioing of RFCK. Second, when a hidden refresh does not occur in a particular RFCK cycle, a forced refresh may still not affect a slow access cycle. The worst-case is when an access is pending during a forced refresh, in which case a three wait state delay is usually the maximum penalty.

Usually two DP84300 type chips would be required to interface between any microprocessor and the DP8400/DP8409 combined system. These chips would handle the read/write control as well as error detection and correction control. Table VII shows the individual DP84300 circuits that would be used in systems with no error correction, thus requiring only the DP8409 DRAM controller.

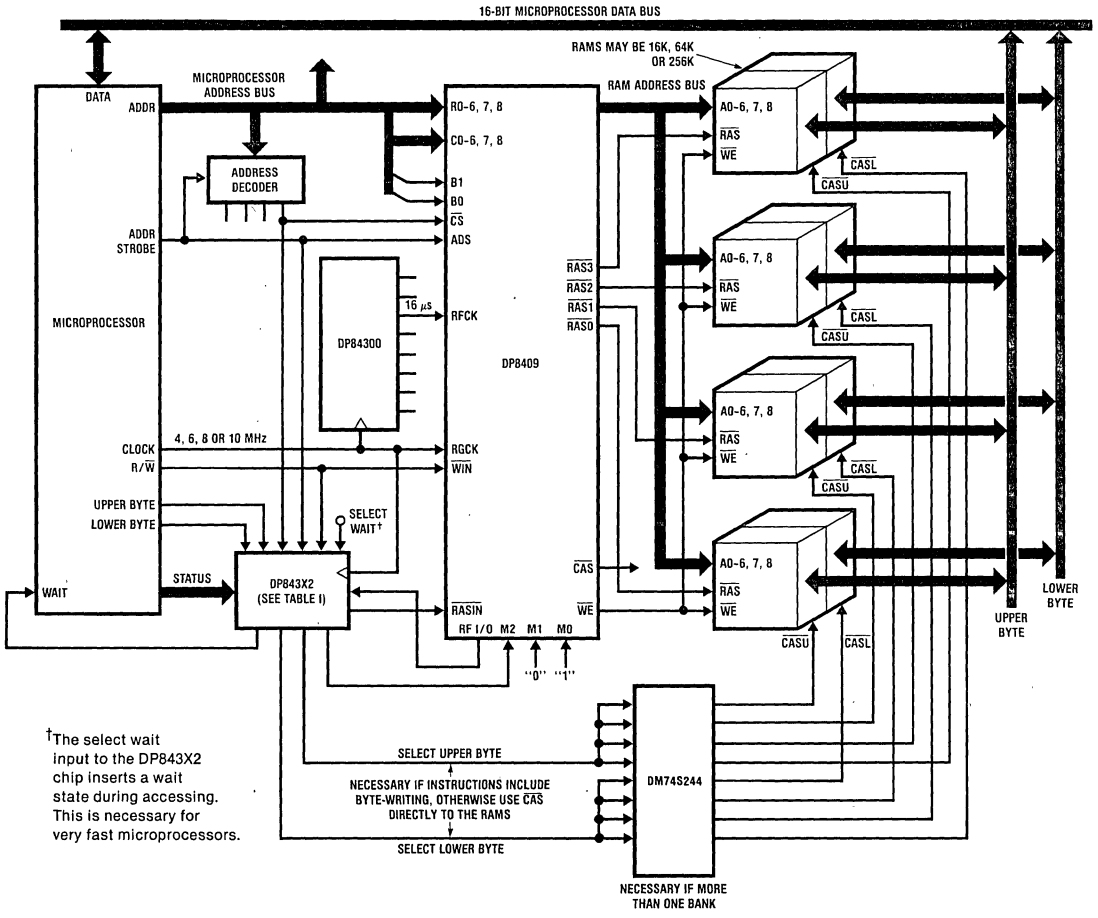


FIGURE 13. Connecting the DP8409 Between 16-Bit Microprocessor and Memory

The DP8400 DRAM interface family provides complete solutions to memory support. This begins with the LSI functions such as the DP8400 expandable error checker/corrector and the DP8409 DRAM controller/driver. It continues with the DP84240 and the DP84244 high performance buffer/drivers. Finally, it concludes with easy interface to popular microprocessors with the use of the DP84300 series. It is the first family of DRAM support circuits designed for universal applications with multiple microprocessors.

Data sheets and more detailed application information are available for all the members of the DP8400 family. Contact your local National Semiconductor representative or National Semiconductor directly.

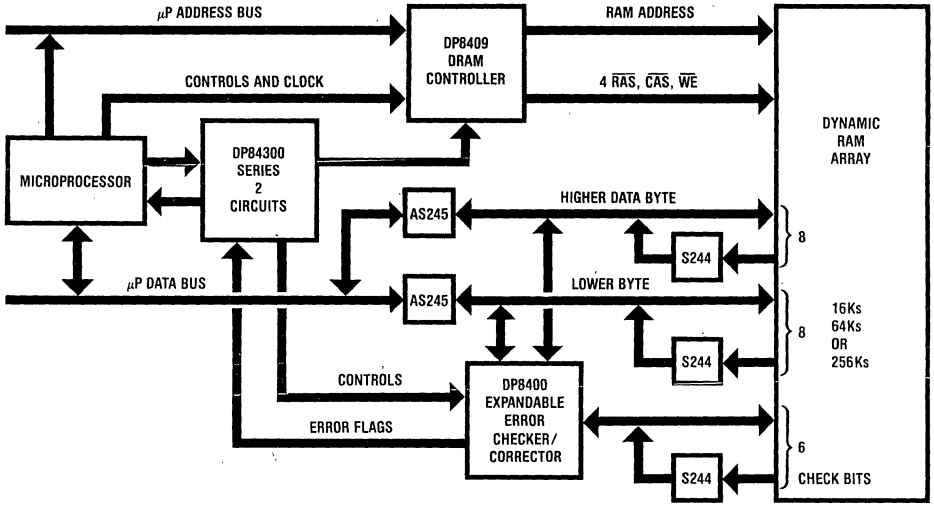


FIGURE 14. Flexible application of the DP8409 and DP8400. This figure shows an application with a 16-bit microprocessor.

TABLE VII. THE DP84300 SERIES OF INTERFACE CIRCUITS FOR VARIOUS 16-BIT MICROPROCESSORS

16-Bit Microprocessor	System Using Only DP8409
National 16032	DP84312
Motorola 68000	DP84322
Intel 8086/8	DP84332
Zilog 8000	(2) 74S64 (1) 74S04

National Semiconductor

DP84240/DP84244 Octal TRI-STATE® MOS Drivers

General Description

The DP84240 and DP84244 are octal TRI-STATE drivers which are designed for heavy capacitive load applications such as fast data buffers or as memory address drivers. The DP84240 is an inverting driver which is pin-compatible with both the 74S240 and AM2965. The DP84244 is a non-inverting driver which is pin-compatible with the 74S244 and AM2966. These parts are fabricated using an oxide isolation process, for much faster speeds, and are designed for load capacitances of 250pF or greater.

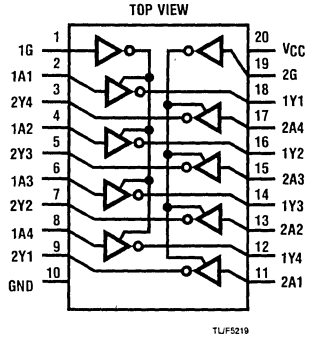
Features

- t_{pd} specified with 250pF and 500pF loads
- Output specified from 0.8V to 2.7V
- Designed for symmetric rise and fall times at 500pF
- Outputs glitch free at power up and power down
- PNP inputs reduce DC loading on bus lines
- Low static and dynamic input capacitance
- Low skew times between edges and pins
- AC parameters specified with all outputs switching simultaneously

TRI-STATE® is a registered trademark of National Semiconductor Corporation

Connection Diagrams

DP84240



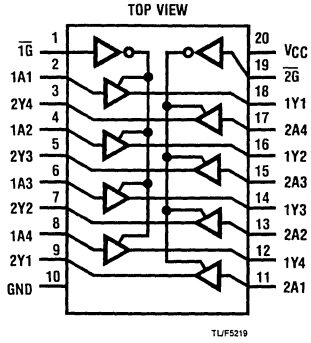
Truth Tables

DP84240

Inputs $\overline{G}$	Inputs A	Outputs Y
H	X	Z
L	L	H
L	H	L

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance

DP84244



Inputs $\overline{G}$	Inputs A	Outputs Y
H	X	Z
L	L	L
L	H	H

Order Number DP84240J, DP84244J, DP84240N or DP84244N
See NS Package J20A or N20A

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity package	1667mW
Molded Package	1832mW
Lead Temperature (soldering, 10 seconds)	300°C

*Derate cavity package 11.1mW/°C above 25°C: derate molded package 14.7mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.5	5.5	V
T_A Ambient Temperature	0	+70	°C

Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $0 \leq T_A \leq 70°C$. See Notes 2 and 3.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1' Input Current	$V_{IN} = 2.7V$		0.1	20	μA
		$V_{IN} = 7.0V$			100	μA
$I_{IN(0)}$	Logical "0" Input Current	$0 \leq V_{IN} \leq 0.4V$		−50	−200	μA
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -18mA$		−1	−1.2	V
V_{OH}	Logical "1" Output Voltage	$I_{OH} = -100\mu A$ $I_{OH} = -1mA$	$V_{CC} - 1.15$ $V_{CC} - 1.5$	4.3 3.9		V
V_{OL}	Logical "0" Output Voltage	$I_{OL} = 10\mu A$ $I_{OL} = 12mA$		0.2 0.3	0.4 0.5	V
I_{1D}	Logical "1" Drive Current	$V_{OUT} = 1.5V$	−75	−250		mA
I_{0D}	Logical "0" Drive Current	$V_{OUT} = 1.5V$	+100	+150		mA
Hi-Z	TRI-STATE Output Current	$0.4V \leq V_{OUT} \leq 2.7V$	−100		+100	μA
I_{CC}	Supply Current DP84240	All Outputs Open All Outputs High All Outputs Low All Outputs Hi-Z		 16 74 80	 50 125 125	mA
	DP84244	All Outputs High All Outputs Low All Outputs Hi-Z		40 100 115	75 130 150	

Switching Characteristics

$V_{CC} = 5V \pm 10\%$, $0 \leq T_A \leq 70°C$, all outputs loaded with specified load capacitance and all eight outputs switching simultaneously. (See Note 3.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay from LOW-to-HIGH Output	Figures 1 & 3 $C_L = 250pF$	9	16	27	ns
		Figures 1 & 3 $C_L = 500pF$	10	20	33	
t_{PHL}	Propagation Delay from HIGH-to-LOW Output	Figures 1 & 3 $C_L = 250pF$	9	16	25	ns
		Figures 1 & 3 $C_L = 500pF$	12	20	31	
t_{PLZ}	Output Disable Time from LOW	Figures 2 & 4, $S = 1$, $C_L = 50pF$		11	24	ns
t_{PHZ}	Output Disable Time from HIGH	Figures 2 & 4, $S = 2$, $C_L = 50pF$		12	24	ns
t_{PZL}	Output Enable Time to LOW	Figures 2 & 4, $S = 1$, $C_L = 500pF$		30	45	ns
t_{PZH}	Output Enable Time to HIGH	Figures 2 & 4, $S = 2$, $C_L = 500pF$		23	35	ns
t_{SKEW}	Output-to-Output Skew See Note 4.	Figures 1 & 3 $C_L = 500pF$		3		ns

Capacitance

$T_A = 25°C$, $f = 1MHz$, $V_{CC} = 5V \pm 10\%$. See Note 3.

Parameter	Conditions	Typ	Units
C_{IN}	All other inputs tied low	6	pF
C_{OUT}	Output in TRI-STATE	20	pF

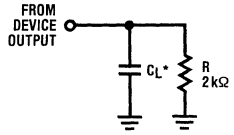
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins shown as positive; all currents out of device pins shown as negative; all voltages referenced to ground unless otherwise noted. All values shown as max. or min. are on an absolute value basis.

Note 3: Typical characteristics are taken at $V_{CC} = 5.0V$ and $T_A = 25°C$.

Note 4: The output-to-output skew is primarily a function of the number of outputs switching and the capacitive loading on those outputs. See *Figures 5* and *6* for the switching time variations.

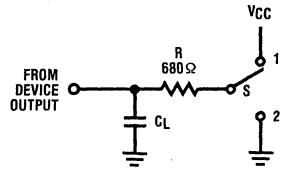
Switching Test Circuits



*C_L INCLUDES PROBE AND JIG CAPACITANCES

TL/F5219

FIGURE 1. Capacitive Load Switching

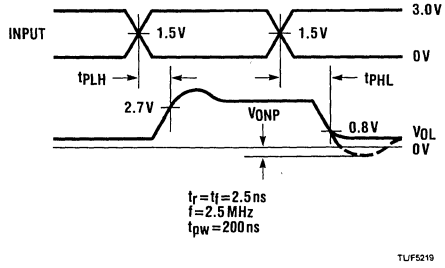


TL/F5219

FIGURE 2. Three-State Enable/Disable

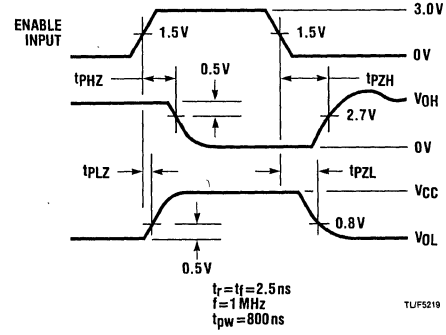
Typical Switching Characteristics

Voltage Waveforms



TL/F5219

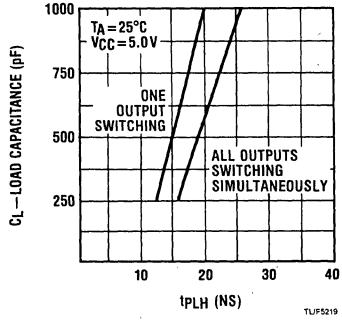
FIGURE 3. Output Drive Levels



TL/F5219

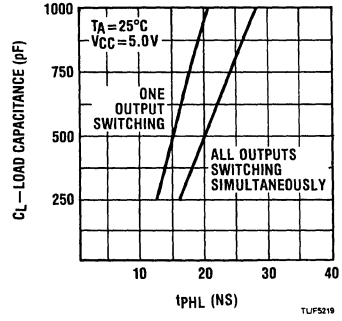
FIGURE 4. Three-State Control Levels

Typical Performance Curves



TL/F5219

FIGURE 5. t_{PLH} Measured to 2.7V on Output vs. C_L



TL/F5219

FIGURE 6. t_{PHL} Measured to 0.8V on Output vs. C_L

Typical Performance Curves (Continued)

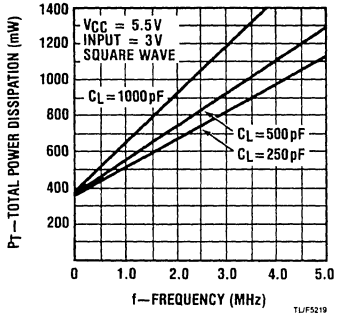


FIGURE 7. Typical Power Dissipation for DP84240 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

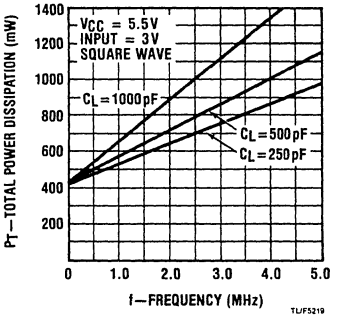
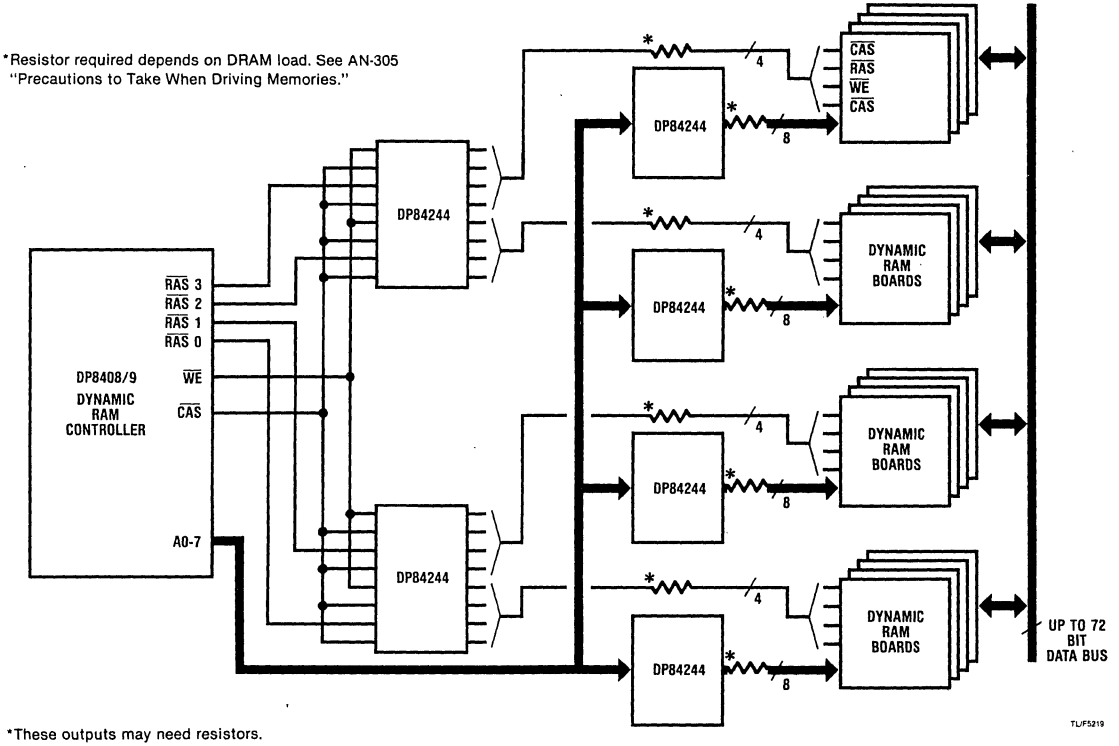


FIGURE 8. Typical Power Dissipation for DP84244 at V_{CC} = 5.5V (All 8 drivers switching simultaneously)

Typical Application



*These outputs may need resistors.
See App. Note "Precautions to Take When Driving Memories."

DP84244 used as a buffer in a large memory array (greater than 88 dynamic RAMs)

A family of single-chip dynamic RAM controllers provides the access-timing and refreshing capability for any chip made, or projected.

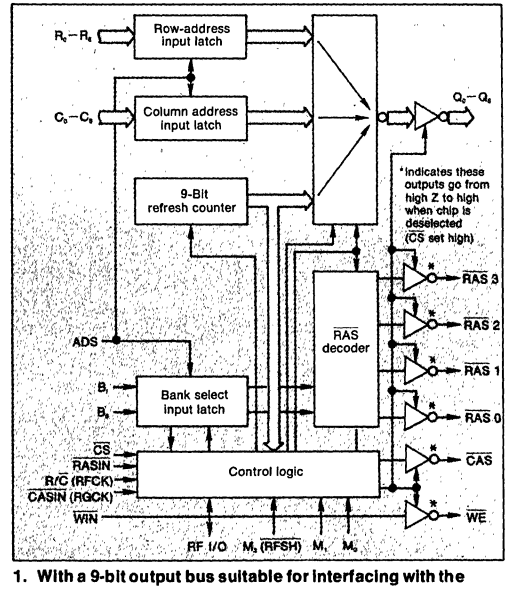
Single-chip controllers cover all RAMs from 16-k to 256-k

While the high performance and low cost of MOS dynamic RAMs make them the most widely used digital semiconductor devices, operating them is more difficult than most other memory chips. Demands are growing for both the automatic sequencing of RAM-access timing and the automatic control of refreshing. National Semiconductor's response is the DP8400 family of memory-interface circuits. The first two members, the DP8408 and the DP8409, are powerful single-chip dynamic-RAM controllers housed in 48-pin dual-in-line packages and, more important, designed to drive the entire range of dynamic RAMs.

The DP8408's eight address outputs drive all current 16-k and 64-k dynamic RAMs. The DP8409, with nine address outputs, not only handles the same RAMs as the 8408, but can control the coming generation of 256-k memory chips. Both devices are pin-compatible, which means a system designed with the DP8408 to control 64-k chips can be directly upgraded to the DP8409 when 256-k RAMs appear on the market. Another benefit for designers is alternate-sourcing—the first DP8400 devices are available from Monolithic Memories (Sunnyvale, CA).

The DP8408, a subset of the DP8409, fits into applications that do not require automatic refreshing. But it does have automatic access modes. The DP8409 is designed for any type of dynamic RAM system, from small microprocessor-based systems to large memory boards. An automatic-accessing mode makes it desirable in mainframes, since it reduces skew time to that of just one chip, while offering tracking of the RAM input controls. This faster accessing permits the use of slower RAMs. With 64-k RAMs, for example, the cost savings between 200-ns and 150-ns devices is significant when large quantities are involved.

Microprocessor users will prefer the DP8409 to other controllers because a single chip performs all the basic automatic access sequencing and automatic refreshing control. (If desired, external refreshing can be used with either controller.) Fast automatic accessing eliminates the need for the wait states that are normally required in faster microprocessors. Automatic refreshing eliminates complicated refresh-arbitration control circuitry while offering a



1. With a 9-bit output bus suitable for interfacing with the largest dynamic RAMs (256 k), National Semiconductor's DP8409 RAM controller drives every RAM available. Features include automatic accessing, automatic refreshing, and high-impedance outputs when not selected. An 8-bit version, the DP8408, operates with RAMs up to 64 kbits, and is used in applications that do not require automatic refreshing.

Mike Evans, Applications Manager, Logic Group
Charles Carinalli, Design Manager, Interface Circuits

Published in *Electronic Design*, February 4, 1982.
Reprinted by permission.

hidden refresh feature to increase the system throughput. The DP8409 offers full control, including byte writing, of the 68000, 8086, and Z8000 microprocessors, and National Semiconductor's new 16032 16-bit microprocessor.

Controlling a dynamic RAM is no simple task (see "Dynamic RAM Operation—from $\overline{RAS}$ to $\overline{CAS}$"). Three timing delays are required for an access, and refreshing must be performed continually. With the arrival of powerful 16-bit processors and their large, direct memories, a single-chip controller becomes necessary for efficient system design. Propagation timing delays through the controller must be in the tens of nanoseconds to minimize total access time. Moreover, to eliminate the propagation delays caused by additional memory drivers, a controller should be capable of directly driving a large number of RAMs. The controller must also reduce component cost and conserve PC-board area.

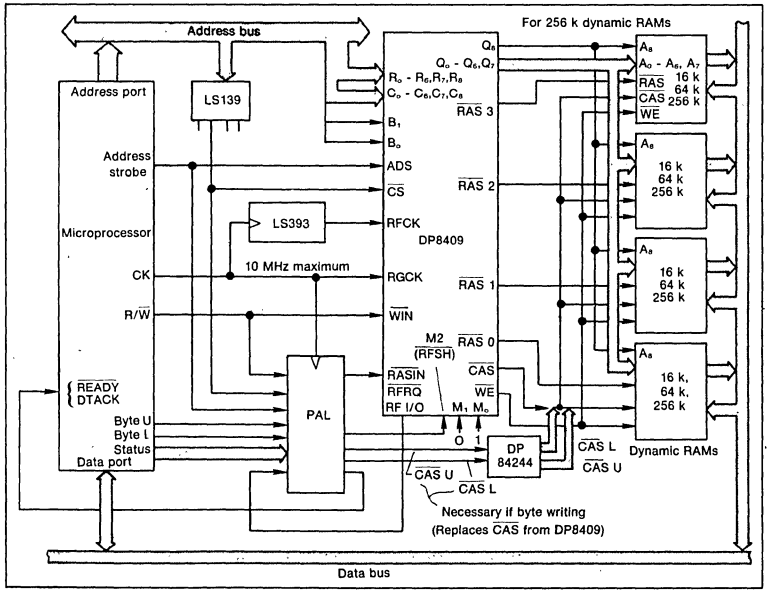
To fulfill these requirements, the DP8408 and 8409 are fabricated in bipolar technology rather than MOS. LSI capability exists in bipolar technology, and bipolar dynamic-RAM controllers are already available. Two such controllers, Intel's 8202 and AMD's 2964 (AMZ8164), represented early attempts to bring timing delays under system control.

In the Intel device, the clock is independent of the access-request signal, causing excessive synchronizing delays before the appearance of the output signals. This leads to long system access times, and for most 16-bit microprocessors requires the insertion of wait states. The AMD controller is an address multiplexer with an on-board refresh counter and bank selection for up to four banks of RAMs. While this device drives a small number of RAMs, AMD offers octal memory drivers that can be placed between the 2964 and the RAMs. Delays become progressively longer as timing signals proceed through the delay timer, the 2964, and the additional drivers. And external components are needed to initiate timing delays. Quite simply, the DP8408 and DP8409 go well beyond the access-time and functional capabilities of the 8202 and 2964.

On board the RAM controllers

A functional block diagram of the DP8409 is shown in Fig. 1. The DP8408 is similar, except for its 8-bit-wide multiplexed address-bus and the fact that its R/C and $\overline{CASIN}$ inputs do not provide dual functions as RFCK and RGCK inputs, as they do in the 8409.

The multiplexed address outputs of both controllers can be selected from the row or column input latches, or from the refresh counter. A high level on input signal ADS enables input row-addresses, R_0



2. The interface of the DP8409 RAM controller to a 16-bit microprocessor looks ahead to the day when 256-kbit dynamic RAMs are available. By designing-in the controller now, no modifications to printed-circuit boards will be necessary when 256-k devices are developed. Simply exchanging controller chips will allow the memory-control capability of a microprocessor to increase by four times.

through R_8, input column-addresses C_0 through C_8, and bank-select inputs B_0 and B_1 into their respective input latches. ADS also latches these signals on its low-going edge. In a normal RAM access, B_0 and B_1 are decoded to determine which bank is selected. By enabling one of the four RAS outputs (when $\overline{\text{RASIN}}$ goes low), the contents of the row-address latch are strobed into the selected RAMs.

Now the control logic causes the row addresses to be replaced with the column addresses, and CAS goes low as determined by the control logic. This causes the contents of the column-address latch to be strobed into the selected RAMs.

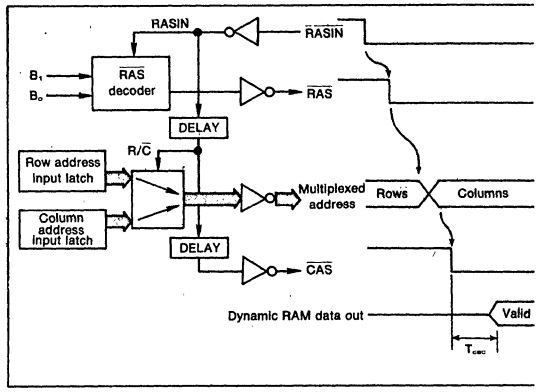
On a write cycle, $\overline{\text{WE}}$ must be low as $\overline{\text{CAS}}$ goes low; on a read cycle, $\overline{\text{WE}}$ must be high. For a read-modify-write cycle, $\overline{\text{WE}}$ must go low some time after $\overline{\text{CAS}}$—this is specified in RAM data sheets. To simplify control, $\overline{\text{WE}}$ follows $\overline{\text{WIN}}$ unconditionally 20 ns later, typically. Three mode pins—M_0, M_1, and M_2 (M_2 is refresh mode)—offer externally selected operating modes. For example, mode 5—automatic access—identified by code 101, can be changed to mode 1—forced refresh—identified by code 100, when M_2 is driven low. These modes include automatic and external control of accesses, and various refreshing modes.

Input pin $\overline{\text{CS}}$ selects or deselects the controller to allow for multiaddressing of memory. For accesses, $\overline{\text{CS}}$ is normally low, but to access a second DP8409 sharing the same memory, $\overline{\text{CS}}$ of the first 8409 must go high. This puts the three-state address outputs in a high-impedance high-state through an external 5-kΩ pull-up resistor, and sets the control signals to a high impedance to prevent them from drifting low; a low level can result in a false access. Switching between chips takes about 30 ns, providing fast multiaddressing. Refreshing must be performed using only one chip. As $\overline{\text{CS}}$ goes high in mode 5, deselection is overridden and, provided RFCK is already high, hidden refreshing can occur.

Input/output pin RF I/O can be used to clear the refresh counter when it has been set low by an external open-collector gate. It also sends out an end-of-count signal—a low level—when the refresh counter has filled (counts are selectable to 127, 255, or 511). This is a useful feature for burst refreshing. In the automatic-refresh mode, RF I/O becomes the signal Refresh Request.

No problems with capacitive loads

One important asset of the DP8408 and 8409 is their ability to drive high-capacitance loads. RAM inputs are generally specified as having a maximum input capacitance of 10 pF/pin, but in large RAM systems, the worst-case input capacitance is usually on the order of 2.5 pF per input. However, one or two devices



3. The DP8408/8409's automatic-accessing capability uses on-chip delay paths to provide faster access while saving on external delay-timing circuitry. On-chip Schottky inverters track extremely well with temperature and voltage, keeping access-times stable.

in a system can go up to 10 pF, especially at high temperature. On the other hand, RAM input currents carry specifications of around 10 μA maximum, but actual input currents seldom exceed 3 μA per input in large systems. Of the two parameters—capacitance and input current—high capacitance always causes more system problems.

In addition to a RAM's input capacitance, designers must consider the capacitance of the PC-board traces. The value of capacitance depends on trace length, nearness to other traces, board thickness, etc. Generally, this amounts to about 3.2 pF per input, giving a total worst-case input capacitance of 5.7 pF/input.

The output stages of the DP8408/8409 can drive up to 88 RAMs, or 500 pF of capacitive loading. Looking at it another way, the controllers can drive four banks each of 16-data bits plus 6 associated check bits for error correction; two banks of 32 data bits with 7 check bits; one bank of 64 data bits with 8 check bits; or any smaller combination. Output rise and fall times are proportional to the capacitive loading, and more than 500 pF increases transition time. Similarly, less than 500 pF decreases propagation delays.

The output-driver stages of the DP8409/8409 are matched. Each stage has symmetrical high and low drive capability, which require that the high and low on-resistances be the same. High output currents are needed to quickly charge or discharge the effective RAM load capacitance on each output. In most applications, a series damping resistor is required between each output and the RAM to minimize undershoot. Undershoot occurs at RAM inputs having both inductive board traces and high capacitive loads on high-to-low transitions.

The value of the series damping resistor depends heavily on the board layout. Address lines usually use a value different from control lines, but both are functions of layout and input loading. The resistor is almost tuned to a specific board since too high a value yields an excessively slow edge, while too low a value does not remove the undershoot. In any case, damping-resistor values vary from 15 to 100 Ω.

Control over all RAMs

The DP8408 and 8409 are designed to control all multiplexed-address dynamic RAMs. The DP8408, with eight multiplexed address outputs and an 8-bit refresh counter, controls 16-k dynamic RAMs (+5 V or three-power-supply types) and both configurations of 64-k RAMs (128 rows by 512 columns or 256 rows by 256 columns). Memory users can specify either of the two 64-k RAM configurations provided the refresh counter on the DP8408 is used. This replaces on-the-RAM refresh counters offered by some RAM manufacturers.

The DP8409's nine address pins and 9-bit refresh counter allow it to control 16-k, 64-k, and 256-k RAMs. Designers can take advantage of the 8409's 256-k capability by building current memory boards using the device. No modifications will be needed when the 256-k RAMs are available. By simply providing for two new input address lines and connecting Q_8 (the ninth multiplexed address output) to A_8 (pin 1) of the RAMs, the memory size can be increased instantly by a factor of four. Figure 2 shows how the connections are made.

Automatic accessing capability is provided by the 8408 and 8409 using on-chip delay paths to generate the correct timing sequence (Fig. 3). These delays are initiated from only one input signal, $\overline{\text{RASIN}}$. This generates all the access-sequencing required by most RAMs. Automatic accessing operates in the following manner: First, $\overline{\text{RASIN}}$ is used to generate the selected $\overline{\text{RAS}}$ output as decoded from bank-select signals B_1 and B_0. $\overline{\text{RASIN}}$ is also fed to the first series of Schottky inverters to produce the necessary delay before rows can be switched to columns. This guarantees exceeding the row-address hold time (t_{RAH}) of most RAMs. For 64-k RAMs, t_{RAH} varies from 20 to 25 ns, so the minimum specification for the 8408 and 8409, 30 ns, is on the safe side. If the address outputs are driving 500-pF loads, switching from row addresses to valid column addresses takes 10 ns. The second series of inverters set $\overline{\text{CAS}}$ low 12 ns (typically) after the columns are valid.

The inverters track with temperature and V_{CC}, as do the output driver stages. Tracking of the output paths holds over the specified temperature and V_{CC} ranges. Since Schottky-logic parameters do not vary significantly with temperature or V_{CC}, the absolute times are not affected by more than 25% over the 0 to 70°C range. At the end of an access-cycle, $\overline{\text{RASIN}}$ goes high and the sequence repeats at a higher speed to terminate the cycle.

An automatic-access mode offers two important advantages: First, there is no need for external timing delay circuitry—this saves cost, memory-board area, and the timing skews that external circuitry introduces. Second, this sequence is much faster than a clocked sequencing approach—that is, the delay from $\overline{\text{RASIN}}$ input to $\overline{\text{CAS}}$ output is much shorter. Benefits include a faster system access time, the possibility of eliminating a wait state in a microprocessor memory-access cycle, or the ability to choose slower RAMs (a lower-cost solution) without affecting access time. And since both chips need no external memory drivers, the timing skews are confined to just one chip.

If automatic timing is not desired, another mode allows all timing to be under the control of the relevant external control signals. $\overline{\text{RASIN}}$ initiates the selected $\overline{\text{RAS}}$ output, R/$\overline{\text{C}}$ selects either the row or column address, and $\overline{\text{CASIN}}$ controls $\overline{\text{CAS}}$.

Refreshing comes in many forms

The DP8408 performs refresh operations only under external control. The microprocessor system decides when a refresh is needed by setting M_2 ($\overline{\text{REFRESH}}$) low to place the refresh counter contents on the address outputs. Then the system sets $\overline{\text{RASIN}}$ low to allow all four RAS outputs to low-stroke the refresh address into the rows of all four banks of RAMs. $\overline{\text{CAS}}$ is inhibited, preventing a false write, and the RAM data outputs remain in a high-impedance state.

A refresh cycle ends when $\overline{\text{RASIN}}$ goes high and the refresh counter increments, ready for the next refresh cycle. Most RAMs require that all 128 rows be refreshed in 2 ms, or 256 rows in 4 ms. This can be accomplished by either guaranteeing a refresh on one row every 16 μs, or performing a burst refresh of 128 rows at the start of each 2-ms period, until RF I/O indicates end-of-count. Most system designers prefer one refresh every 16 μs. But this can involve inhibiting normal memory accessing, and requires refresh arbitration.

The end-of-count indication on RF I/O can be set under external system control to either 127 or 255 for burst-refresh applications. Actually, the internal address counter still counts to its maximum value, independent of the end-of-count value—the RF I/O value is a result of counter decode and does not reset the counter. This simplifies the RAM interface since the higher-order address bit-count is ignored by RAMs with 128 rows.

In addition to providing the external-control

refresh mode of the 8408, the 8409 performs hidden refreshing in one of the automatic-access modes. To attain maximum throughput, it is obviously advantageous to perform refreshes without interrupting the system. The DP8409 can do this by monitoring the $\overline{CS}$ input to see if it is high. If $\overline{CS}$ is high, the RAMs are not being accessed. If $\overline{CS}$ is high for one cycle, the 8409 performs a hidden refresh during this cycle, and stops in time for the system to start another access. But if a hidden refresh does not occur in a specific 16-μs time slot, a refresh must be forced, possibly by stopping the system.

To perform auto-refreshing, the DP8409 must receive two clock signals: the 16-μs refresh-period clock, RFCK, and RGCK, the RAS-generator clock; RGCK can be the microprocessor clock. To keep the number of pins at 48, RFCK and RGCK share pins with other signals. In the automatic-access mode (mode 5), neither R/$\overline{C}$ nor $\overline{CASIN}$ are used, so these duplicate as RFCK and RGCK in modes 1 and 5. To stop the

Dynamic RAM operation—from $\overline{RAS}$ to $\overline{CAS}$

The operation of a dynamic RAM (see figure) is, in a word, complex: Not only do its multiplexed address inputs require delayed timing signals, but it must be refreshed continually.

During an access to a RAM, the first step requires that a row address be presented to the multiplexed address inputs. As the row-address signal ($\overline{RAS}$) goes low, the address is latched into the row latch, and decoded to the memory array. There, the outputs from the selected row are presented to the sense amplifiers. Row addresses must be held on the address inputs for a predetermined time—t_{RAIL}, or row-address hold-time—after $\overline{RAS}$ switches low.

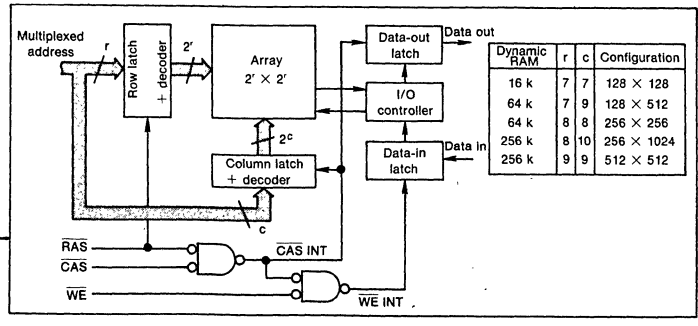
At this time, the row address can be replaced by a column-address. When a column address is valid, the column-address strobe ($\overline{CAS}$) goes low to latch the address into the column latch. Column-addresses are decoded to allow a selected sense amplifier to send data to the output data-latch (during a read cycle). In a write cycle, with the Write Enable signal ($\overline{WE}$) already low, a low-going $\overline{CAS}$ signal causes the selected cell to be set to the value at the data input.

The RAM block diagram shows the chip's operation, including the internal gating of the control signals. One key feature is that $\overline{RAS}$ internally controls $\overline{CAS}$. Thus, if $\overline{RAS}$ is already low when $\overline{CAS}$ goes low, a normal read or write cycle follows, and the chip consumes its full operating current. On the other hand, if $\overline{CAS}$ goes low while $\overline{RAS}$ is high, $\overline{CAS}$ $\overline{INT}$ is inhibited along with $\overline{RAS}$, and the RAM consumes only the current required for standby. In this case, the chip is deactivated. Similarly, $\overline{WE}$ $\overline{INT}$ is controlled by both $\overline{RAS}$ and $\overline{CAS}$.

This simplifies bank selection by using different $\overline{RAS}$ outputs to select the banks. $\overline{CAS}$ and $\overline{WE}$ can be common to all the RAM-banks, along with the multiplexed addressing. For example, in a four-bank system, only one $\overline{RAS}$ goes low in any access-cycle. This activates all the RAMs in a selected bank, but does not activate RAMs in the other three banks. These latter RAMs remain in the standby mode. The common data bus accesses only the selected bank, whether reading or writing.

Besides a complex sequencing arrangement, dynamic RAMs must be refreshed to prevent the capacitor in each cell from losing its charge, which represents information. If any row is not accessed for too long a period of time—the refresh period—capacitors will discharge, causing the voltage to drop below the sense-amplifier threshold. Then, when the row is finally accessed, its outputs will appear as all zeros or all ones, depending on which side of the sense amplifier is accessed.

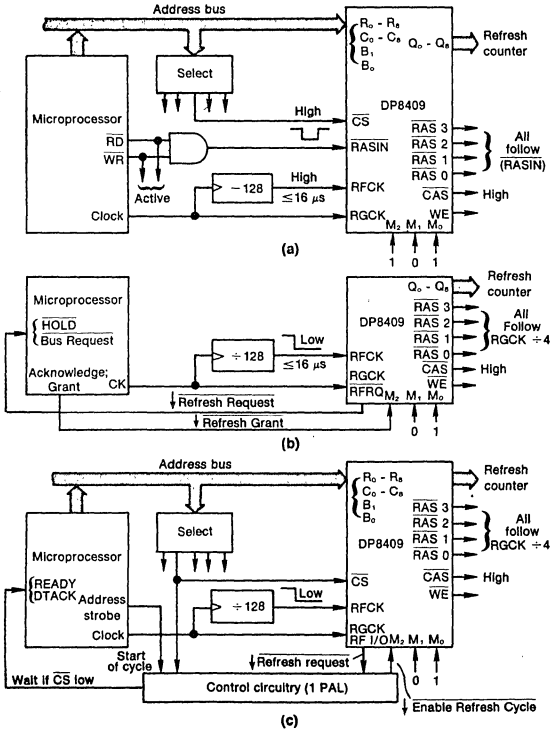
Most RAMs have 2-ms minimum refresh times, but 64-k dynamic RAMs are typically much higher. When accessing a row for refresh, $\overline{RAS}$ is needed for a strobe, but $\overline{CAS}$ is not necessary. The simplest approach to refreshing is to access a refresh counter that increments at the end of each refresh $\overline{RAS}$. For some RAMs, 128 rows must be refreshed in 2 ms, while others require refreshing 256 rows in 4 ms. With distributed refreshing, one row must be refreshed every 16 μs for proper operation.



Dynamic RAM	r	c	Configuration
16 k	7	7	128 × 128
64 k	7	9	128 × 512
64 k	8	8	256 × 256
256 k	8	10	256 × 1024
256 k	9	9	512 × 512

system, the DP8409 gives preference to hidden refreshing using RFCK as a level reference. The 16-μs cycle commences as RFCK goes high; if CS goes high while RFCK is high, the refresh counter is enabled on the address outputs, overriding the internal three-state signals (Fig. 4a). All four RAS outputs follow $\overline{\text{RASIN}}$, so to perform a refresh, $\overline{\text{RASIN}}$ must be set low. In smaller systems, $\overline{\text{RASIN}}$ is set low every time a microprocessor performs a read or write cycle. Each time the processor accesses something other than RAM—a peripheral or ROM or another memory segment—a hidden refresh is performed.

The DP8409 detects that $\overline{\text{CS}}$ is high when the processor accesses another section of the system and places the present state of the refresh counter outputs on the multiplexed address bus to memory. When the Read or Write output of the microprocessor is activated, $\overline{\text{RASIN}}$ follows. This causes all four RAS outputs to low-strobe the refresh address into the RAMs. When the cycle ends, $\overline{\text{RASIN}}$ ends, forcing the four $\overline{\text{RAS}}$ outputs back to their inactive states. This ends the hidden refresh.



4. Automatic refreshing can be performed in three different ways with the DP8409 controller. A hidden refresh (a) occurs while the microprocessor is reading or writing elsewhere in the system. Although undesirable, forced refreshing (b) can be performed by stopping the microprocessor. A better technique for forced refreshing (c) is to insert wait states into the processor timing cycle.

At this time, the refresh counter increments, and another microprocessor cycle can begin immediately. This cycle can be a memory access; therefore, the previous refresh cycle has been completely hidden from the microprocessor. The DP8409 allows only one such hidden refresh cycle to occur within a clock cycle of RFCK to minimize power dissipation.

If a hidden refresh does not occur, the DP8409 must force a refresh before RFCK begins a new cycle on a low-to-high transition. Therefore, as RFCK goes low (and a hidden refresh has not occurred), RF I/O (Refresh Request) goes low requesting that a refresh be performed. When the system acknowledges the request, it sets M_2 (refresh) low, and prevents further accesses to the DP8409. The 8409 then sends out the refresh-counter contents and interrogates RGCK—in most applications, RGCK is 100 to 150 ns. The 8409 waits one full cycle of RGCK before setting all four RAS outputs low. This guarantees that the minimum RAS precharge time of the RAMs is exceeded. Then RF I/O goes high, allowing the system to recognize that holding is about to end. Most microprocessors allow enough time so that as refresh finishes, they are almost ready to begin again. The $\overline{\text{RAS}}$ outputs remain low for the next two clock periods to exceed the minimum t_{RAS} time for refreshing—200 ns is about the right time. When all $\overline{\text{RAS}}$ outputs go high, the refresh counter increments.

A minimum component-count solution to forced refreshing is to connect RF I/O to the Hold or Bus-Request input of a microprocessor, and the Hold Acknowledge or Bus Grant output to M_2 (Fig. 4b). For some microprocessors, it may be preferable to continue operation without going into hold, and with additional circuitry, the approach can be easily implemented as shown in Fig. 4c. Using this technique of forced refreshing, the control circuit monitors the refresh-request output. When this output switches low, the control circuit waits for a new microprocessor cycle to begin. If the next cycle is for the segment of memory controlled by the DP8409, $\overline{\text{CS}}$ and the control circuitry will be set low. The control circuitry issues a Wait signal to the microprocessor, which is removed when refreshing has ended. If $\overline{\text{CS}}$ is set high, the refresh cycle begins and ends without affecting other system cycles. In effect, this is still a hidden refresh.□

National Semiconductor

DP8408 Dynamic RAM Controller/Driver

General Description

Dynamic memory system designs, which formerly required several support chips to drive the memory array, can now be implemented with a single IC. . . the DP8408 Dynamic RAM Controller/Driver. The DP8408 is capable of driving all 16k and 64k Dynamic RAMs (DRAMs). Since the DP8408 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, the major performance disadvantage of multiple-chip memory drive and control.

The DP8408's 6 modes of operation offer a wide selection of DRAM control capabilities. Memory access may be controlled externally or on-chip automatically; an on-chip refresh counter makes refreshing less complicated.

The DP8408 is a 48-pin DRAM Controller/Driver with 8 multiplexed address outputs and control signals. It consists of two 8-bit address latches, an 8-bit refresh counter, and control logic. All output drivers are capable of driving 500 pF loads with propagation delays of 25 ns. The DP8408 timing parameters are specified driving the typical load capacitance of 88 DRAMs, including trace capacitance.

The DP8408 has 3 mode-control pins: M2, M1, and M0, where M2 is in general $\overline{\text{REFRESH}}$. These 3 pins select 6 modes of operation. Inputs B1 and B0 in the memory access modes (M2 = 1), are select inputs which select one of four $\overline{\text{RAS}}$ outputs. During normal access, the 8 address outputs can be selected from the Row Address Latch or the Column Address Latch. During refresh, the 8-bit on-chip refresh counter is enabled onto the address bus and in this mode all $\overline{\text{RAS}}$ outputs are selected, while $\overline{\text{CAS}}$ is inhibited.

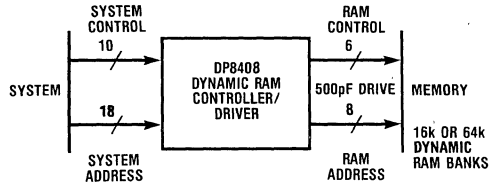
The DP8408 can drive up to 4 banks of DRAMs, with each bank comprised of 16k's, or 64k's. Control signal outputs $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ are provided with the same drive capability. Each $\overline{\text{RAS}}$ output drives one bank of DRAMs so that the four $\overline{\text{RAS}}$ outputs are used to select the banks, while $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and the multiplexed addresses can be connected to all of the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the data outputs in TRI-STATE®. Only the bank with its associated $\overline{\text{RAS}}$ low will be written to or read from.

Operational Features

- All DRAM drive functions on one chip — minimizes skew on outputs, maximizes AC performance
- On-chip capacitive-load drives (specified to drive up to 88 DRAMs)
- Drives directly all 16k and 64k DRAMs
- Capable of addressing 64k and 256k words
- Propagation delays of 25 ns typical at 500 pF load
- $\overline{\text{CAS}}$ goes low automatically after column addresses are valid if desired
- Auto Access mode provides $\overline{\text{RAS}}$, Row to Column, select, then $\overline{\text{CAS}}$ automatically and fast
- $\overline{\text{WE}}$ follows $\overline{\text{WIN}}$ unconditionally—offering READ, WRITE or READ-MODIFY-WRITE cycles
- On-chip 8-bit refresh counter with selectable End-of-Count (127 or 255)
- End-of-Count indicated by RF I/O pin going low at 127 or 255
- Low input on RF I/O resets 8-bit refresh counter
- $\overline{\text{CAS}}$ inhibited during refresh cycle
- Fall-through latches on address inputs controlled by ADS
- TRI-STATE outputs allow multi-controller addressing of memory
- Control output signals go high-impedance logic "1" when disabled for memory sharing
- Power-up: counter reset, control signals high, address outputs TRI-STATE, and End-of-Count set to 127

Mode Features

- 6 modes of operation: 3 access, 1 refresh, and 2 set-up
- 2 externally controlled modes: 1 access (Mode 4) and 1 refresh (Modes 0, 1, 2)
- 2 auto-access modes $\overline{\text{RAS}} \rightarrow \text{R}/\overline{\text{C}} \rightarrow \overline{\text{CAS}}$ automatic, with t_{RAH} = 20 or 30 ns minimum (Modes 5, 6)
- Externally controlled All-$\overline{\text{RAS}}$ Access modes for memory initialization (Mode 3)
- End-of-Count value of Refresh Counter set by B1 and B0 (Mode 7)



DP8408 Interface Between System & DRAM Banks

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Block Diagram

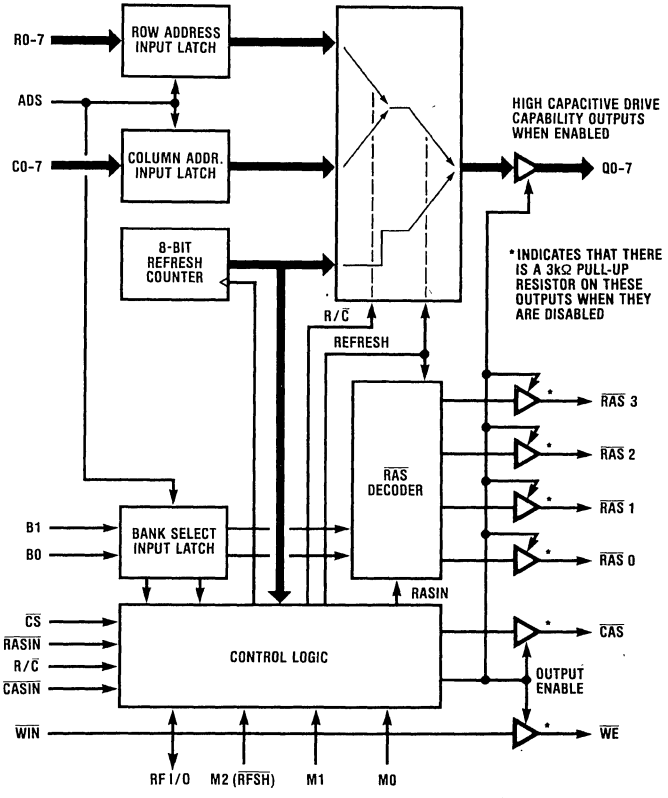
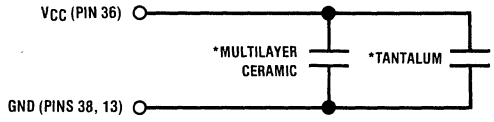


Table 1. DP8408 Mode Select Options

Mode	(RFSH) M2	M1	M0	Mode of Operation	Conditions
0	0	0	0	Externally Controlled Refresh	RF I/O = $\overline{EOC}$
1	0	0	1		
2	0	1	0		
3	0	1	1	Externally Controlled All-$\overline{RAS}$ Write	All-$\overline{RAS}$ Active
4	1	0	0	Externally Controlled Access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto Access, Slow t_{RAH}	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto Access, Fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set End of Count	See Table 3 for Mode 7

Pin Definitions

V_{CC}, GND, GND — $V_{CC} = 5V \pm 5\%$. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 8 address bits change in the same direction simultaneously. A recommended solution would be a 1μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected as close as possible to pins 36 and 38 to reduce lead inductance. See Figure below.



*Capacitor values should be chosen depending on the particular application.

R0-R7: Row Address Inputs.

C0-C7: Column Address Inputs.

Q0-Q7: Multiplexed Address Outputs — Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.*

$\overline{RASIN}$: Row Address Strobe Input — Enables selected $\overline{RAS}_n$ output when M2 ($\overline{RFSH}$) is high, or all $\overline{RAS}_n$ outputs when $\overline{RFSH}$ is low.

R/$\overline{C}$: Row/Column Select Input — Selects either the row or column address input latch onto the output bus.

$\overline{CASIN}$: Column Address Strobe Input — Inhibits $\overline{CAS}$ output when high in Modes 4 and 3. In Mode 6 it can be used to prolong $\overline{CAS}$ output.

ADS: Address (Latch) Strobe Input — Row Address, Column Address, and Bank Select Latches are fall-through with ADS high; Latches on high-to-low transition.

$\overline{CS}$: Chip Select Input — TRI-STATE's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (except in Mode 0); enables all outputs when low.

M0, M1, M2: Mode Control Inputs — These 3 control pins determine the 6 major modes of operation of the DP8408 as depicted in Table 1.

RF I/O — The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low when M2 = 0 and the End-of-Count output is at 127 or 255 (see Table 3).

$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output — Buffered output from $\overline{WIN}$.*

$\overline{CAS}$: Column Address Strobe Output — In Modes 5 and 6, $\overline{CAS}$ goes low following valid column address. In Modes 3 and 4, it transitions low after R/$\overline{C}$ goes low, or follows $\overline{CASIN}$ going low if R/$\overline{C}$ is already low. $\overline{CAS}$ is high during refresh.*

$\overline{RAS}$ 0-3: Row Address Strobe Outputs — Selects a memory bank decoded from B1 and B0 (see Table 2), if $\overline{RFSH}$ is high. If $\overline{RFSH}$ is low, all banks are selected.*

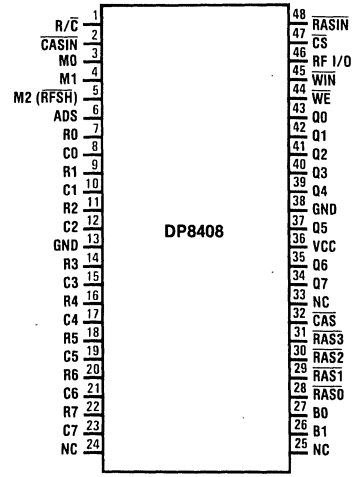
B0, B1: Bank Select Inputs — Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes low. Also used to define End-of-Count in Mode 7 (Table 3).

*These outputs may need damping resistors to prevent overshoot, undershoot. See AN-305 "Precautions to Take When Driving Memories."

Table 2. Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Connection Diagram



NC = NO CONNECTION

Order Number DP8408N, DP8408N-2 DP8408N-3, DP8408D, DP8408D-2 or DP8408D-3
See NS Package N48A or D48A

Conditions for all Modes

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, $\overline{\text{RASIN}}$ and R/$\overline{\text{C}}$ are initially high. When the address inputs are enabled into the address latches, the row addresses appear on the Q outputs. The address strobe also inputs the bank-select address, (B0 and B1). If $\overline{\text{CS}}$ is low, all outputs are enabled. When $\overline{\text{CS}}$ is transitioned high, the address outputs go TRI-STATE and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other DP8408s for multi-addressing. All outputs go active about 50 ns after the chip is selected again. If $\overline{\text{CS}}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive Capability

The DP8408 has timing parameters that are specified with up to 600 pF loads. In a typical memory system this is equivalent to about 88, 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 6. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

Because of distributed trace capacitance and inductance and DRAM input capacitance, current spikes can be created, causing overshoots and undershoots at the DRAM inputs that can change the contents of the DRAMs or even destroy them. To remove these spikes, a damping resistor (low inductance, carbon) can be inserted between the DP8408 driver outputs and the DRAMs, as close as possible to the DP8408. The values of the damping resistors may differ between the different control outputs; $\overline{\text{RAS}}$'s $\overline{\text{CAS}}$, Q's and $\overline{\text{WE}}$. The damping resistors should be determined by the first prototypes (not wire-wrapped due to larger distributed capacitance and inductance). The best values for the damping resistors are the critical values giving a critically damped transition on the control outputs. Typical values for the damping resistors will be between 15Ω and 100Ω, the lower the loading the higher the value. (For more information, see AN-305 "Precautions to Take When Driving Memories.")

DP8408 Driving any 16k or 64k DRAMs

The DP8408 can drive any 16k or 64k DRAMs. All 16k DRAMs are basically the same configuration, including the newer 5V-only version. Hence, in most applications, different manufacturers' DRAMs are interchangeable (for the same supply-rail chips), and the DP8408 can drive all 16k DRAMs (see Figure 1a).

There are three basic configurations for the 5V-only 64k DRAMs: a 128-row by 512-column array with an on-RAM refresh counter, a 128-row by 512-column array with no on-RAM refresh counter, and a 256-row by 256-column array with no on-RAM refresh counter. The DP8408 can drive all three configurations, and at the same time allows them all to be interchangeable (as shown in Figures 1b and 1c), providing maximum flexibility in the choice of DRAMs. Since the 8-bit on-chip refresh counter can be used as a 7-bit refresh counter for the 128-row configuration, or as an 8-bit refresh counter for the 256-row configuration, the on-RAM refresh counter (if present) is never used. As long as 128 rows are refreshed every 2 ms (i.e. 256 rows in 4 ms) all DRAM types are correctly refreshed.

When the DP8408 is in a refresh mode, the RF I/O pin indicates that the on-chip refresh counter has reached its end-of-count. This end-of-count is selectable as 127 or 255 to accommodate 16k or 64k DRAMs, respectively. Although the end-of-count may be chosen to be either of these values, the counter is not reset and always counts to 255 before rolling over to zero.

Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{\text{WE}}$, determines what type of memory access cycle the memory will perform. If $\overline{\text{WE}}$ is kept high while $\overline{\text{CAS}}$ goes low, a read cycle occurs. If $\overline{\text{WE}}$ goes low before $\overline{\text{CAS}}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{\text{CAS}}$ goes low. If $\overline{\text{WE}}$ goes low later than t_{CWD} after $\overline{\text{CAS}}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{\text{WE}}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{\text{WE}}$, which follows $\overline{\text{WIN}}$.

Power-Up Initialize

When V_{CC} is first applied to the DP8408, an initialize pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to TRI-STATE. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

DP8408 Driving any 16k or 64k Dynamic RAMs

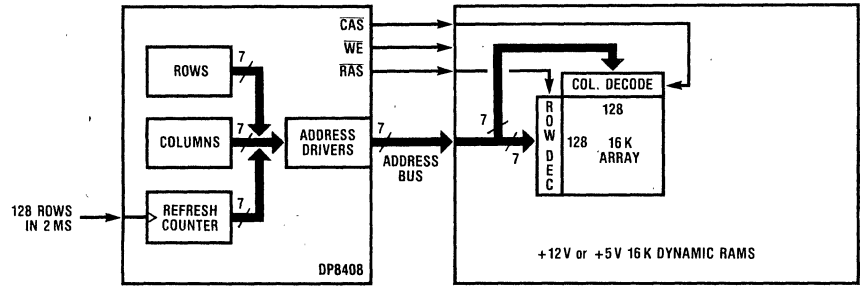


FIGURE 1a. DP8408 with any 16k DRAMS

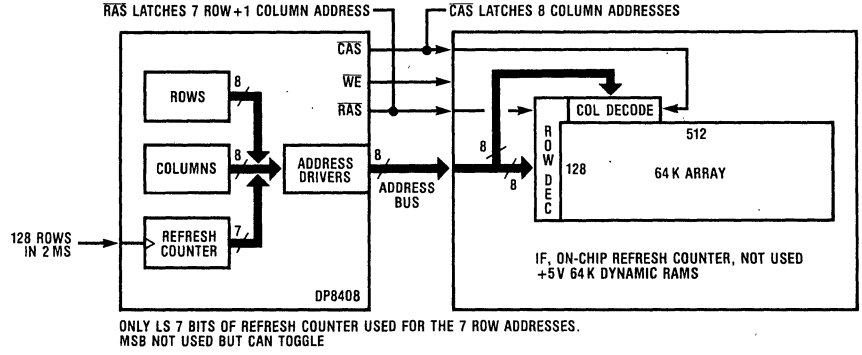


FIGURE 1b. DP8408 with 128 Row × 512 Column 64k DRAM

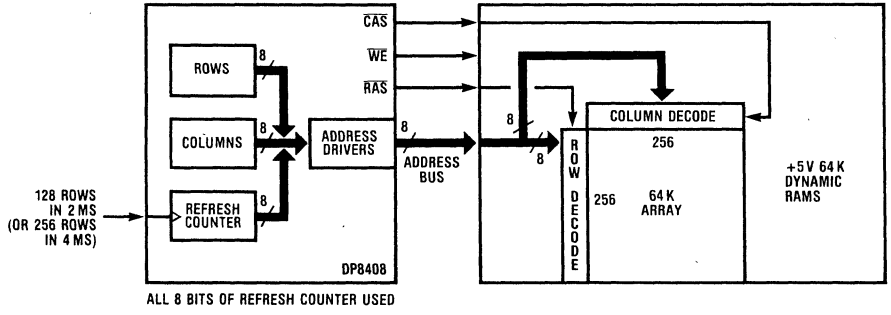


FIGURE 1c. DP8408 with 256 × 256 Column 64k DRAM

DP8408 Functional Mode Descriptions

Note: All delay parameters stated in text refer to the DP8408. Substitute the respective delay numbers for the DP8408-2 or DP8408-3 when using these devices.

Modes 0,1,2 — Externally Controlled Refresh

In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled. When $\overline{RAS}$ occurs, the enabled row in the DRAM is refreshed. In the Externally Controlled Refresh mode, all $\overline{RAS}$ outputs are enabled following $\overline{RASIN}$, and $\overline{CAS}$ is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either $\overline{RASIN}$ or $\overline{RFSH}$ goes low-to-high after a refresh. RF I/O goes low when the count is 127 or 255, as set by End-of-Count (see Table 3), with $\overline{RASIN}$ and $\overline{RFSH}$ low. To reset the counter to all zeroes, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{RASIN}$ and RFSH must be skewed transitioning low such that the refresh address is valid on the address outputs of the controller before the $\overline{RAS}$ outputs go low. The amount of time that RFSH should go low before $\overline{RASIN}$ does depends on the capacitive loading of the address and $\overline{RAS}$ lines. For the load specified in the switching characteristics of this data sheet, 10ns is sufficient. Refer to Figure 2.

To perform externally controlled burst refresh, $\overline{RASIN}$ is toggled while RFSH is held low. The refresh counter increments with $\overline{RASIN}$ going low to high, so that the DRAM rows are refreshed in succession by $\overline{RASIN}$ going high to low.

Mode 3 — Externally Controlled All-$\overline{RAS}$ Write

This mode is useful at system initialization. The memory address is provided by the processor, which also performs the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the DP8408 for the next write cycle.

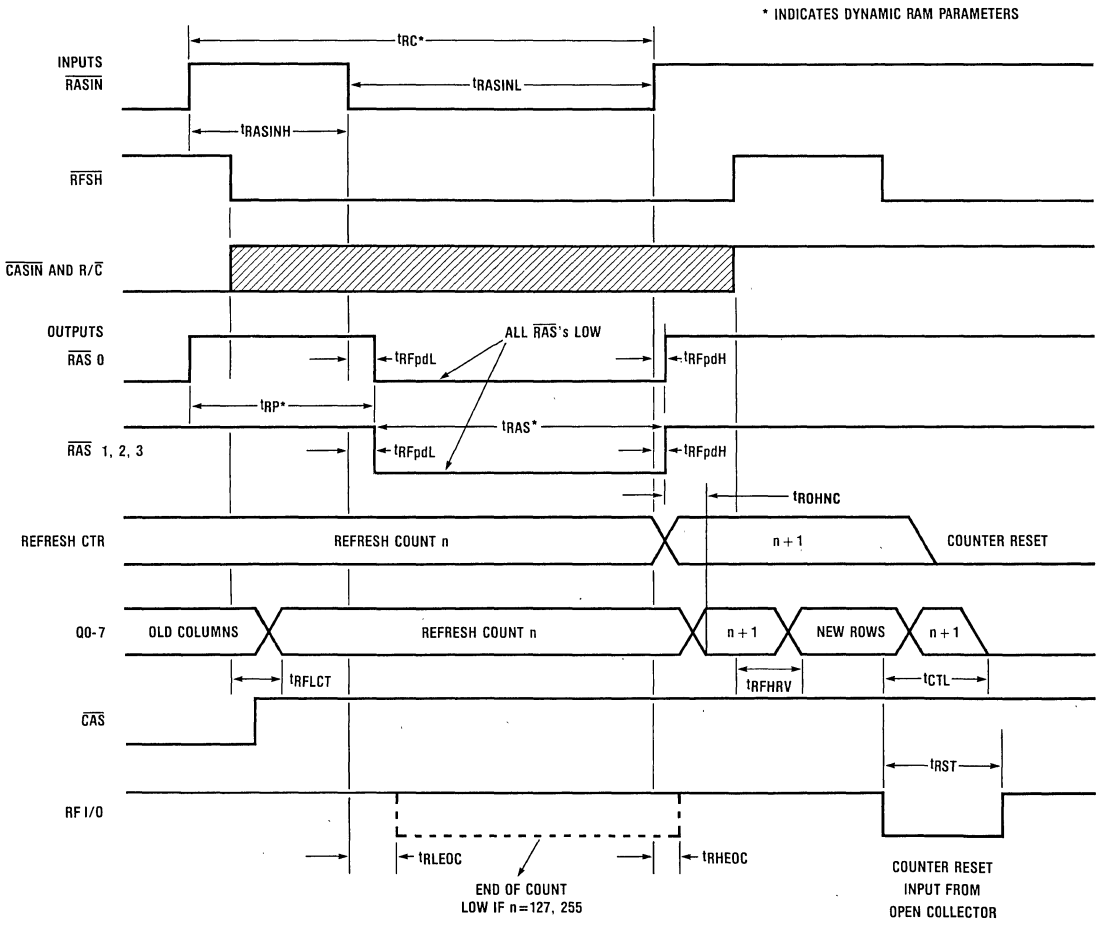


FIGURE 2. External Control Refresh Cycle (MODES 0,1,2)

Mode 4 — Externally Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. The application of modes 0 and 4 are shown in Figure 3.

Output Address Selection

Refer to Figure 4a. With M2 ($\overline{RFSH}$) and R/$\overline{C}$ high, the row address latch contents are transferred to the multiplexed address bus output Q0-Q7, provided $\overline{CS}$ is set low. The column address latch contents are output after R/$\overline{C}$ goes low. $\overline{RASIN}$ can go low after the row addresses have been set up on Q0-Q7. This selects one of the $\overline{RAS}$ outputs, strobing the row address on the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 ns later column addresses appear on the Q outputs.

Automatic $\overline{CAS}$ Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/$\overline{C}$. If $\overline{CASIN}$ is high, then R/$\overline{C}$ going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time (see Figure 4b). If $\overline{CASIN}$ is low when R/$\overline{C}$ goes low, $\overline{CAS}$ will be automatically generated, following the row to column transition by about 20 ns (see Figure 4a). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0 ns or − 10 ns. In other words, a t_{ASC} greater than 0 ns is safe. This feature reduces timing-skew problems, thereby improving access time of the system.

Fast Memory Access

AC parameters t_{DIF1}, t_{DIF2} may be used to determine the minimum delays required between $\overline{RASIN}$, R/$\overline{C}$, and $\overline{CASIN}$ (see Application Brief 9; "Fastest DRAM Access Mode").

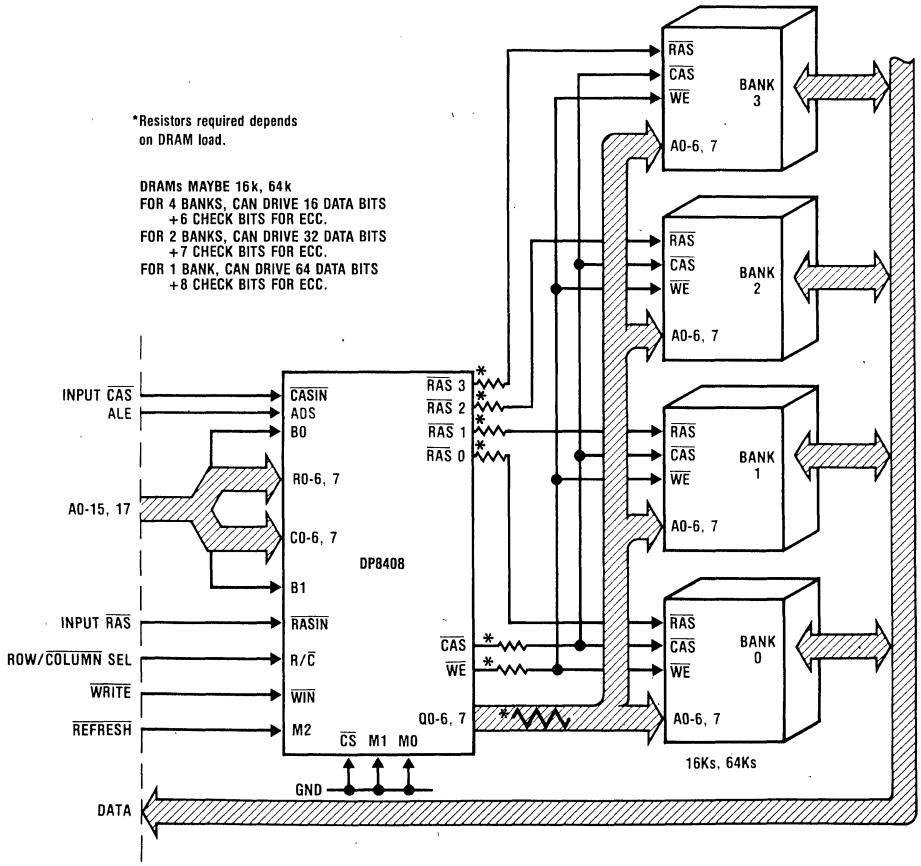


FIGURE 3. Typical Application of DP8408 Using Externally Controlled Access and Refresh in Modes 0 and 4

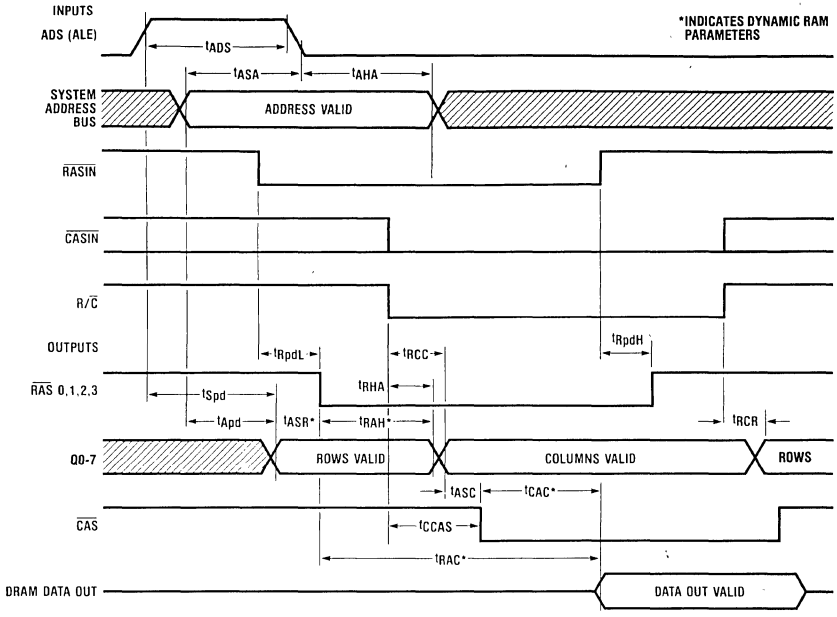


FIGURE 4a. Read Cycle Timing (Mode 4)

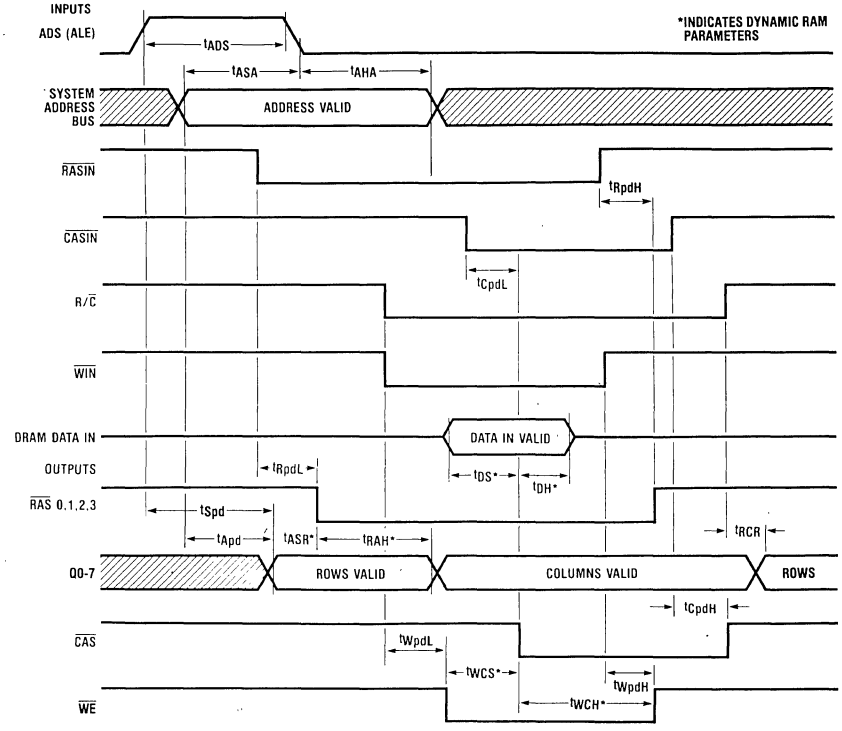


FIGURE 4b. Write Cycle Timing (Mode 4)

Mode 5 — Automatic Access

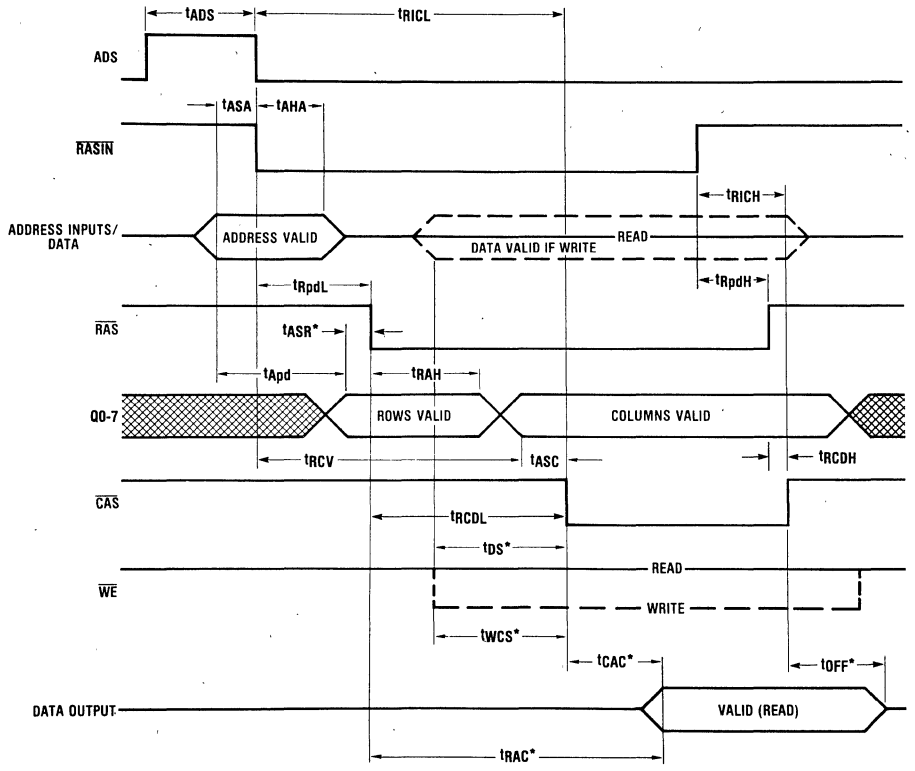
The Auto Access mode has two advantages over the Externally Controlled Access mode, due to the fact that all outputs except $\overline{WE}$ are initiated from $\overline{RASIN}$. First, inputs R/$\overline{C}$ and $\overline{CASIN}$ are unnecessary. Secondly, because the output control signals are derived internally from one input signal ($\overline{RASIN}$), timing-skew problems are reduced, thereby reducing memory access time substantially or allowing use of slower DRAMs. The automatic access features of Mode 5 (and Mode 6) of the DP8408 make DRAM accessing appear essentially "static".

Automatic Access Control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for t_{RAH}, (the Row-Address hold-time of the DRAM), the column address is set up and then $\overline{CAS}$ occurs. This is all performed automatically by the DP8408 in this mode.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27ns later, by which time the row address is already valid on the address output of the DP8408. The Address Set-Up time (t_{ASR}), is 0ns on most DRAMs. The DP8408 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 5a).

Next, the row address is disabled after t_{RAH} (30ns minimum); in most DRAMs, t_{RAH} minimum is less than 30ns. The column address is then set up and t_{ASC} later, $\overline{CAS}$



*INDICATES DYNAMIC RAM PARAMETERS

FIGURE 5a. Modes 5, 6 Timing ($\overline{CASIN}$ High in Mode 6

occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15ns); to $\overline{RAS}$ (27ns); to rows held (50ns); to columns valid (25ns); to $\overline{CAS}$ (23ns) = 140ns (that is, 125ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs. This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

Mode 6 — Fast Automatic Access

The Fast Access mode is similar to Mode 5, but has a faster t_{RAH} of 20ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a t_{RAH} of 10ns to 15ns) in applications requiring fast access times; $\overline{RASIN}$ to $\overline{CAS}$ is typically 105ns.

In this mode, the R/$\overline{C}$ pin is not used, but $\overline{CASIN}$ is used to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 5b. This is desirable with fast cycle-times where $\overline{RAS}$ has to be terminated as soon as possible before the next $\overline{RAS}$ begins (to meet the precharge time, or t_{RP}, requirements of the DRAM). $\overline{CAS}$ may then be held low by $\overline{CASIN}$ to extend the data output valid time from the DRAM to allow the system to read the data. $\overline{CASIN}$ subsequently going high ends $\overline{CAS}$. If this extended $\overline{CAS}$ is not required, $\overline{CASIN}$ should be set high in Mode 6.

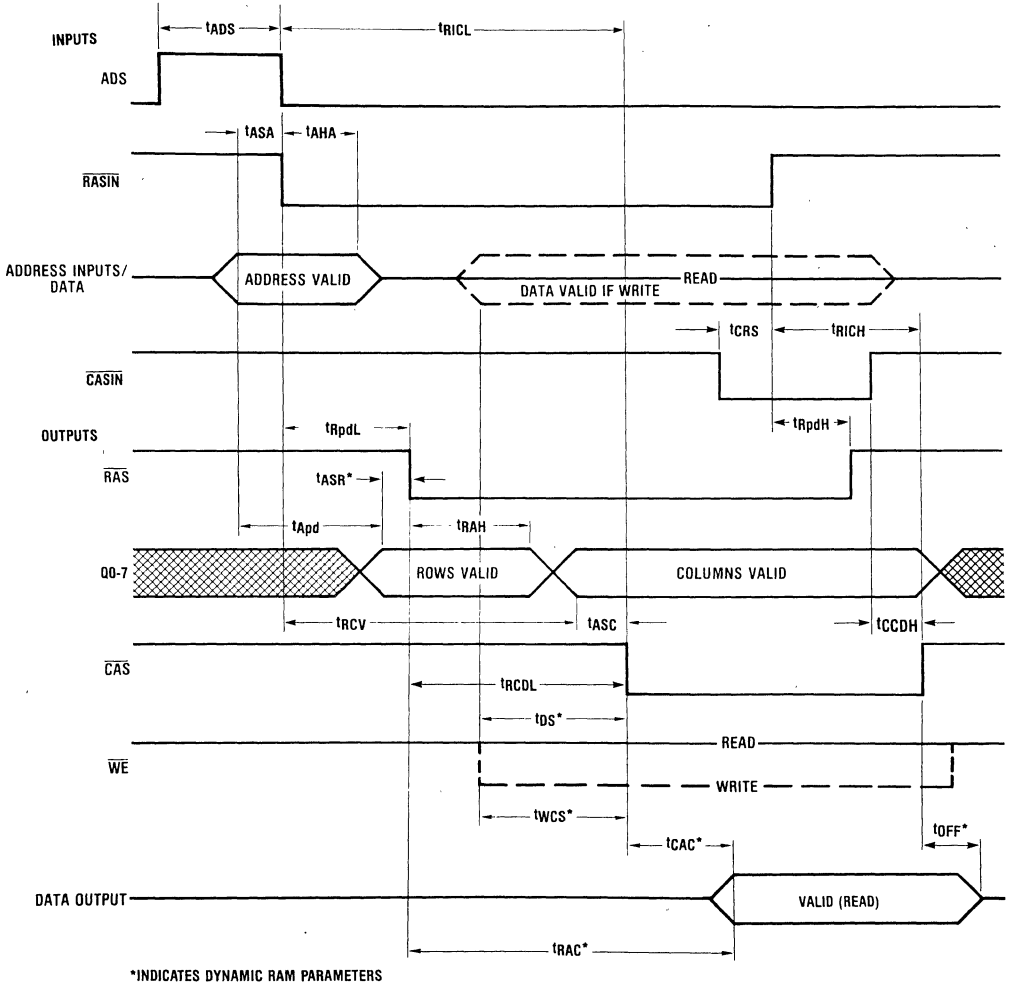


FIGURE 5b. Mode 6 Timing, Extended $\overline{CAS}$

Mode 7 — Set End-of-Count

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same EOC is 127; with B1 = 0 and B0 = 1, EOC is 255; and with B1 = 1 and B0 = 0, EOC is 127. This selected value of EOC will be used until the next Mode 7 selection. At power-up the EOC is automatically set to 127 (B1 and B0 set to 11).

Table 3. Mode 7

Bank Select (Strobed by ADS)		End of Count Selected
B1	B0	
0	0	127
0	1	255
1	0	127
1	1	127

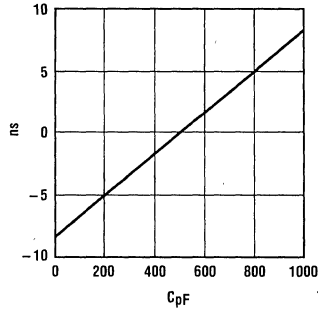


FIGURE 6. Change in Propagation Delay vs. Loading Capacitance Relative to a 500pF Load

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Storage Temperature Range	−65°C to +150°C
Input Voltage	5.5V
Output Current	150mA
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 23.6mW/°C above 25°C; derate molded package 22.7mW/°C above 25°C.

Maximum Power Dissipation* at 25°C	
Cavity Package	3542mW
Molded Package	2833mW

Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.75	5.25	V
T_A Ambient Temperature	0	+70	°C

Electrical Characteristics $V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ unless otherwise noted (Notes 2, 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_C	Input Clamp Voltage	V_{CC} = Min., $I_C = -12mA$		−0.8	−1.2	V
I_{IH1}	Input High Current for ADS, R/$\overline{C}$ only	$V_{IN} = 2.5V$		2.0	100	μA
I_{IH2}	Input High Current for All Other Inputs*	$V_{IN} = 2.5V$		1.0	50	μA
I_I RSI	Output Load Current for RF I/O	$V_{IN} = 0.5V$, Output High		−1.5	−2.5	mA
I_I CTL	Output Load Current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	$V_{IN} = 0.5V$, Chip Deselect		−1.5	−2.5	mA
I_{IL1}	Input Low Current for ADS, R/$\overline{C}$ only	$V_{IN} = 0.5V$		−0.1	−1.0	mA
I_{IL2}	Input Low Current for All Other Inputs*	$V_{IN} = 0.5V$		−0.05	−0.5	mA
V_{IL}	Input Low Threshold				0.8	V
V_{IH}	Input High Threshold		2.0			V
V_{OL1}	Output Low Voltage*	$I_{OL} = 20mA$		0.3	0.5	V
V_{OL2}	Output Low Voltage for RF I/O	$I_{OL} = 10mA$		0.3	0.5	V
V_{OH1}	Output High Voltage*	$I_{OH} = -1mA$	2.4	3.5		V
V_{OH2}	Output High Voltage for RF I/O	$I_{OH} = -100\mu A$	2.4	3.5		V
I_{1D}	Output High Drive Current*	$V_{OUT} = 0.8V$ (Note 3)		−200		mA
I_{0D}	Output Low Drive Current*	$V_{OUT} = 2.7V$ (Note 3)		200		mA
I_{OZ}	TRI-STATE Output Current (Address Outputs)	$0.4V \leq V_{OUT} \leq 2.7V$, $\overline{CS} = 2.0V$, Mode 4	−50	1.0	50	μA
I_{CC}	Supply Current	V_{CC} = Max.		210	285	mA

*Except RF I/O Output.

Switching Characteristics: DP8408/DP8408-3 $V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ unless otherwise noted (Notes 2, 4, 5).

The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0–Q7, $C_L = 500pF$; $\overline{RAS0}$–$\overline{RAS3}$, $C_L = 150pF$; $\overline{WE}$, $C_L = 500pF$; $\overline{CAS}$, $C_L = 600pF$, unless otherwise noted. See Figure 7 for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Access Parameter	Conditions	8408			8408 – 3			Units
			Min	Typ	Max	Min	Typ	Max	
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 5a	95	125	160	95	125	185	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 5a, 5b	80	105	140	80	105	160	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 5a	40	48	60	40	48	70	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 5a, 5b	50	63	80	50	63	95	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 5a		98	125		98	145	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 5a, 5b		78	105		78	120	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 5a		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 5a		40	65		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 5b	40	54	70	40	54	80	ns
t_{RAH}	Row Address Hold Time (Mode 5)	Figure 5a	30			30			ns
t_{RAH}	Row Address Hold Time (Mode 6)	Figures 5a, 5b	20			20			ns
t_{ASC}	Column Address Setup Time (Mode 5)	Figure 5a	8			8			ns
t_{ASC}	Column Address Setup Time (Mode 6)	Figures 5a, 5b	6			6			ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	Figure 5a		90	120		90	140	ns

Switching Characteristics (Cont'd)

Symbol	Access Parameter	Conditions	8408			8408 – 3			Units
			Min	Typ	Max	Min	Typ	Max	
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	Figures 5a, 5b		75	105		75	120	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 4a, 4b, 5a, 5b	20	27	35	20	27	40	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 4a, 4b, 5a, 5b	15	23	32	15	23	37	ns
t_{APDL}	Address Input to Output Low Delay	Figures 4a, 4b, 5a, 5b		25	40		25	46	ns
t_{APDH}	Address Input to Output High Delay	Figures 4a, 4b, 5a, 5b		25	40		25	46	ns
t_{SPDL}	Address Strobe to Address Output Low	Figures 4a, 4b		40	60		40	70	ns
t_{SPDH}	Address Strobe to Address Output High	Figures 4a, 4b		40	60		40	70	ns
t_{ASA}	Address Setup Time to ADS	Figures 4a, 4b, 5a, 5b	15			15			ns
t_{AHA}	Address Hold Time from ADS	Figures 4a, 4b, 5a, 5b	15			15			ns
t_{ADS}	Address Strobe Pulse Width	Figures 4a, 4b, 5a, 5b	30			30			ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 4b	15	25	30	15	25	35	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 4b	15	30	60	15	30	70	ns
t_{CRS}	$\overline{CASIN}$ Setup Time to $\overline{RASIN}$ High (Mode 6)	Figure 5b	35			35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	Figure 4b	32	41	68	32	41	77	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay	Figure 4b	25	39	50	25	39	60	ns
t_{RCC}	Column Select to Column Address Valid	Figure 4a		40	58		40	67	ns
t_{RCR}	Row Select to Row Address Valid	Figures 4a, 4b		40	58		40	67	ns
t_{RHA}	Row Address Held from Column Select	Figure 4a	10			10			ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low (Mode 4 Auto $\overline{CAS}$)	Figure 7a		65	90				ns
t_{DIF1}	Maximum ($t_{RPDL} - t_{RHA}$)	See Mode 4 description			13			18	ns
t_{DIF2}	Maximum ($t_{RCC} - t_{CPDL}$)	See Mode 4 description			13			18	ns
	Refresh Parameter								
t_{RC}	Refresh Cycle Period	Figure 2	100			100			ns
$t_{RASINL,H}$	Pulse Width of $\overline{RASIN}$ during Refresh	Figure 2	50			50			ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figure 2	35	50	70	35	50	80	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figure 2	30	40	55	30	40	65	ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS}$ = X, Figure 2		47	60		47	70	ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	Figure 2		45	60		45	70	ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	Figure 2		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	C_L = 50pF, Figure 2			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	C_L = 50pF, Figure 2			80			80	ns
t_{RST}	Counter Reset Pulse Width	Figure 2	70			70			ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	Figure 2			100			100	ns
	TRI-STATE Parameter								
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	Figure 8 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi-Z from High	C_L = 15pF, Figure 8 R2 = 1k, S1 open		20	40		20	40	ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	Figure 8 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ High to Address Output Hi-Z from Low	C_L = 15pF, Figure 8, R1 = 1k, S2 open		25	50		25	50	ns

Switching Characteristics (Cont'd)

Symbol	TRI-STATE Parameter	Conditions	8408			8408 – 3			Units
			Min	Typ	Max	Min	Typ	Max	
t_{HZH}	$\overline{CS}$ Low to Control Output High from Hi-Z High	Figure 8 R2 = 750Ω, S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z High from High	C_L = 15pF, Figure 8 R2 = 750Ω, S1 open		40	75		40	75	ns
t_{HZL}	$\overline{CS}$ Low to Control Output Low from Hi-Z High	Figure 8 S1, S2 open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ High to Control Output Hi-Z High from Low	C_L = 15pF, Figure 8, R2 = 750Ω, S1 open		50	80		50	80	ns

Switching Characteristics: DP8408-2

$V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ unless otherwise noted (Notes 2, 4, 5, 7). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0-Q7, C_L = 500pF; $\overline{RAS}$0-$\overline{RAS}$3, C_L = 150pF; $\overline{WE}$, C_L = 500pF; $\overline{CAS}$, C_L = 600pF, unless otherwise noted. See Figure 7 for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Access Parameter	Conditions	8408 – 2						Units
			Min	Typ	Max	Min	Typ	Max	
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 5a	75	100	130				ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 5a, 5b	65	90	115				ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 5a	40	48	60				ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 5a, 8b	50	63	80				ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 5a		75	100				ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 5a, 5b		65	85				ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 5a		27	40				ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 5a		40	65				ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 5b	40	54	70				ns
t_{RAH}	Row Address Hold Time (Mode 5) (Note 7)	Figure 5a	20						ns
t_{RAH}	Row Address Hold Time (Mode 6) (Note 7)	Figures 5a, 5b	12						ns
t_{ASC}	Column Address Setup Time (Mode 5)	Figure 5a	3						ns
t_{ASC}	Column Address Setup Time (Mode 6)	Figures 5a, 8b	3						ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	Figure 5a		80	105				ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	Figures 5a, 5b		70	90				ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 4a, 4b, 5a, 5b	20	27	35				ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 4a, 4b, 5a, 5b	15	23	32				ns
t_{APDL}	Address Input to Output Low Delay	Figures 4a, 4b, 5a, 5b		25	40				ns
t_{APDH}	Address Input to Output High Delay	Figures 4a, 4b, 5a, 5b		25	40				ns
t_{SPDL}	Address Strobe to Address Output Low	Figures 4a, 4b		40	60				ns
t_{SPDH}	Address Strobe to Address Output High	Figures 4a, 4b		40	60				ns
t_{ASA}	Address Set-up Time to ADS	Figures 4a, 4b, 5a, 5b	15						ns
t_{AHA}	Address Hold Time from ADS	Figures 4a, 4b, 5a, 5b	15						ns
t_{ADS}	Address Strobe Pulse Width	Figures 4a, 4b, 5a, 5b	30						ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 4b	15	25	30				ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 4b	15	30	60				ns
t_{CRS}	$\overline{CASIN}$ Set-up Time to $\overline{RASIN}$ High (Mode 6)	Figure 5b	35						ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	Figure 4b	32	41	58				ns

Switching Characteristics (Cont'd)

Symbol	Access Parameter	Conditions	8408 – 2						Units
			Min	Typ	Max	Min	Typ	Max	
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	Figure 4b	25	39	50				ns
t_{RCC}	Column Select to Column Address Valid	Figure 4a		40	58				ns
t_{RCR}	Row Select to Row Address Valid	Figures 4a, 4b		40	58				ns
t_{RHA}	Row Address Held from Column Select	Figure 4a	10						ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low (Mode 4 Auto $\overline{CAS}$)	Figure 7a		55	75				ns
t_{DIF1}	Maximum ($t_{RPDL} - t_{RHA}$)	See Mode 4 description			13				ns
t_{DIF2}	Maximum ($t_{RCC} - t_{CPDL}$)	See Mode 4 description			13				ns
	Refresh Parameter								
t_{RC}	Refresh Cycle Period	Figure 2	100						ns
$t_{RASINL,H}$	Pulse Width of $\overline{RASIN}$ during Refresh	Figure 2	50						ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figure 2	35	50	70				ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figure 2	30	40	55				ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS}$ = X, Figure 2		47	60				ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	Figure 2		45	60				ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	Figure 2		30	55				ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	C_L = 50pF, Figure 2			80				ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	C_L = 50pF, Figure 2			80				ns
t_{RST}	Counter Reset Pulse Width	Figure 2	70						ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	Figure 2			100				ns
	TRI-STATE Parameter								
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60				ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi-Z from High	C_L = 15pF, Figures 9, 12 R2 = 1k, S1 open		20	40				ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60				ns
t_{LZ}	$\overline{CS}$ High to Address Output Hi-Z from Low	C_L = 15pF, Figures 9, 12 R1 = 1k, S2 open		25	50				ns
t_{HZH}	$\overline{CS}$ Low to Control Output High from Hi-Z High	Figures 9, 12 R2 = 750Ω, S1 open		50	80				ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z High from High	C_L = 15pF, Figures 9, 12 R2 = 750Ω, S1 open		40	75				ns
t_{HZL}	$\overline{CS}$ Low to Control Output Low from Hi-Z High	Figure 12, S1, S2 open		45	75				ns
t_{LHZ}	$\overline{CS}$ High to Control Output Hi-Z High from Low	C_L = 15pF, Figure 12, R2 = 750Ω, S1 open		50	80				ns

Input Capacitance $T_A = 25°C$ (Notes 2, 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance ADS, R/$\overline{C}$			8		pF
C_{IN}	Input Capacitance All Other Inputs			5		pF

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F = 2.5ns$, $f = 2.5MHz$, $t_{PW} = 200ns$. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50pF.

Note 6: Applies to all DP8408 versions unless otherwise specified.

Note 7: The DP8408-2 device can only be used with memory devices that meet the t_{RAH} specification indicated.

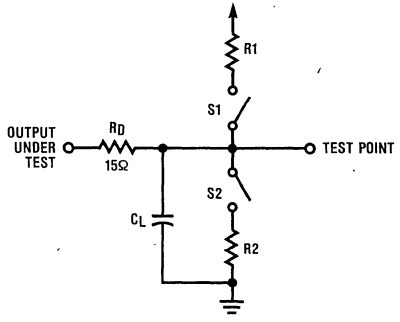


FIGURE 7. Output Load Circuit

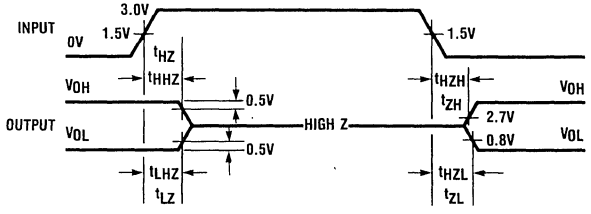


FIGURE 8. Waveform

Applications

If external control is preferred, the DP8408 may be used in Modes 0 or 4, as in Figure 3.

If basic auto access and refresh are required, then in cases where the user requires the minimum of external complexity, Modes 0 and 5 are ideal, as shown in Figure 9a. The DP843X2 is used to provide proper arbitration between memory access and refresh. This chip supplies all the necessary control signals to the processor as well as the DP8408. Furthermore, two separate $\overline{CAS}$ outputs are also included for systems using byte-writing. The refresh clock RFCK may be divided down from either RGCK using an IC counter such as the DM74LS393 or better still, the DP84300 Programmable Refresh Timer. The DP84300 can provide RFCK periods ranging from 15.4μs to 15.6μs based on the input clock of 2 to 10 MHz. Figure 9b shows the general timing diagram for interfacing the DP8408 to different microprocessors using the interface controller DP843X2.

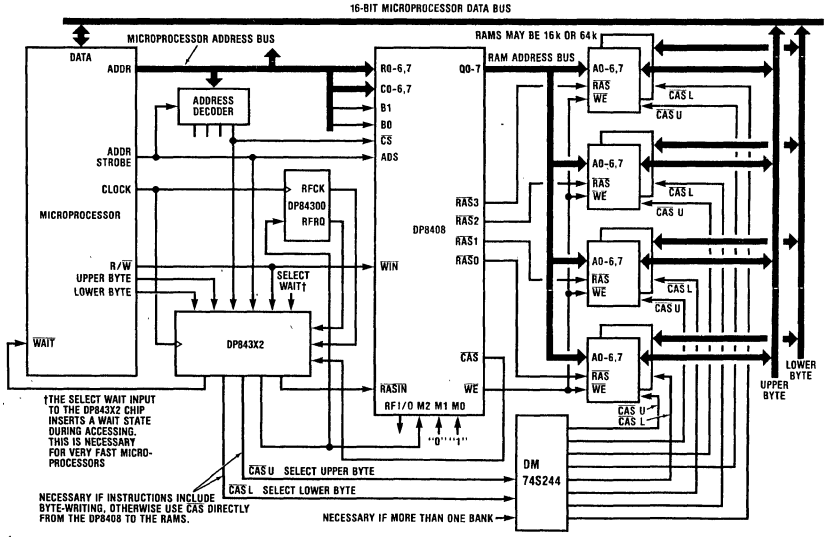


FIGURE 9a. Connecting the DP8408 Between the 16-Bit Microprocessor and Memory

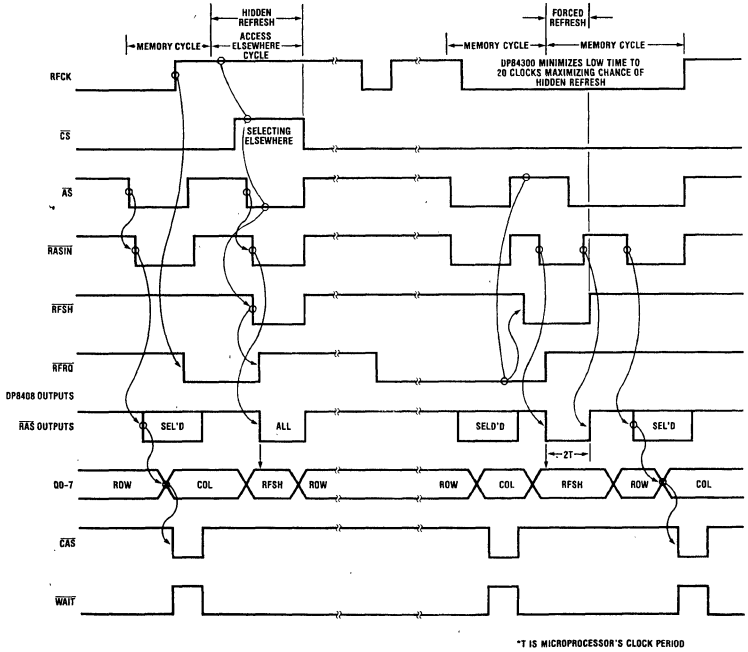


FIGURE 9b. DP8408 Auto Refresh

DP8409 Multi-Mode Dynamic RAM Controller/Driver

General Description

Dynamic memory system designs, which formerly required several support chips to drive the memory array, can now be implemented with a single IC. . . the DP8409 Multi-Mode Dynamic RAM Controller/Driver. The DP8409 is capable of driving all 16k and 64k Dynamic RAMs (DRAMs) as well as 256k DRAMs. Since the DP8409 is a one-chip solution (including capacitive-load drivers), it minimizes propagation delay skews, the major performance disadvantage of multiple-chip memory drive and control.

The DP8409's 8 modes of operation offer a wide selection of DRAM control capabilities. Memory access may be controlled externally or on-chip automatically; an on-chip refresh counter makes refreshing (either externally or automatically controlled) less complicated; and automatic memory initialization is both simple and fast.

The DP8409 is a 48-pin DRAM Controller/Driver with 9 multiplexed address outputs and 6 control signals. It consists of two 9-bit address latches, a 9-bit refresh counter, and control logic. All output drivers are capable of driving 500 pF loads with propagation delays of 25 ns. The DP8409 timing parameters are specified driving the typical load capacitance of 88 DRAMs, including trace capacitance.

The DP8409 has 3 mode-control pins: M2, M1, and M0, where M2 is in general $\overline{\text{REFRESH}}$. These 3 pins select 8 modes of operation. Inputs B1 and B0 in the memory access modes (M2 = 1), are select inputs which select one of four $\overline{\text{RAS}}$ outputs. During normal access, the 9 address outputs can be selected from the Row Address Latch or the Column Address Latch. During refresh, the 9-bit on-chip refresh counter is enabled onto the address bus and in this mode all $\overline{\text{RAS}}$ outputs are selected, while $\overline{\text{CAS}}$ is inhibited.

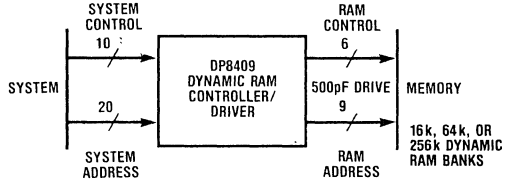
The DP8409 can drive up to 4 banks of DRAMs, with each bank comprised of 16k's, 64k's, or 256k's. Control signal outputs $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ are provided with the same drive capability. Each $\overline{\text{RAS}}$ output drives one bank of DRAMs so that the four $\overline{\text{RAS}}$ outputs are used to select the banks, while $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and the multiplexed addresses can be connected to all of the banks of DRAMs. This leaves the non-selected banks in the standby mode (less than one tenth of the operating power) with the data outputs in TRI-STATE®. Only the bank with its associated $\overline{\text{RAS}}$ low will be written to or read from.

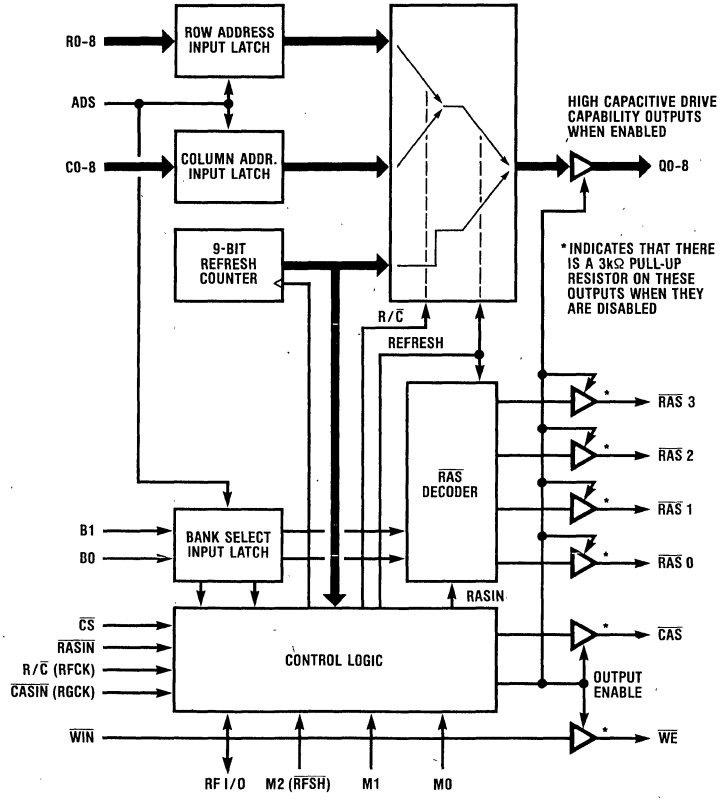
Operational Features

- All DRAM drive functions on one chip — minimizes skew on outputs, maximizes AC performance
- On-chip capacitive-load drives (specified to drive up to 88 DRAMs)
- Drives directly all 16k, 64k, and 256k DRAMs
- Capable of addressing 64k, 256k, or 1M words
- Propagation delays of 25 ns typical at 500 pF load
- $\overline{\text{CAS}}$ goes low automatically after column addresses are valid if desired
- Auto Access mode provides $\overline{\text{RAS}}$, row to column select, then $\overline{\text{CAS}}$ automatically and fast
- $\overline{\text{WE}}$ follows $\overline{\text{WIN}}$ unconditionally—offering READ, WRITE or READ-MODIFY-WRITE cycles
- On-chip 9-bit refresh counter with selectable End-of-Count (127, 255, or 511)
- End-of-Count indicated by RF I/O pin going low at 127, 255, or 511
- Low input on RF I/O resets 9-bit refresh counter
- $\overline{\text{CAS}}$ inhibited during refresh cycle
- Fall-through latches on address inputs controlled by ADS
- TRI-STATE outputs allow multi-controller addressing of memory
- Control output signals go high-impedance logic "1" when disabled for memory sharing
- Power-up: counter reset, control signals high, address outputs TRI-STATE, and End-of-Count set to 127

Mode Features

- 8 modes of operation: 3 access, 3 refresh, and 2 set-up
- 2 externally controlled modes: 1 access and 1 refresh (Modes 0, 4)
- 2 auto-access modes $\overline{\text{RAS}} \rightarrow \text{R}/\overline{\text{C}} \rightarrow \overline{\text{CAS}}$ automatic, with t_{RAH} = 20 or 30 ns minimum (Modes 5, 6)
- Auto-access mode allows Hidden Refreshing (Mode 5)
- Forced Refresh requested on RF I/O if no Hidden Refresh (Mode 5)
- Forced Refresh performed after system acknowledge of request (Mode 1)
- Automatic Burst Refresh mode stops at End-of-Count of 127, 255, or 511 (Mode 2)
- 2 All-$\overline{\text{RAS}}$ Access modes externally or automatically controlled for memory initialization (Modes 3a, 3b)
- Automatic All-$\overline{\text{RAS}}$ mode with external 8-bit counter frees system for other set-up routines (Mode 3a)
- End-of-Count value of Refresh Counter set by B1 and B0 (Mode 7)





DP8409 Functional Block Diagram

Pin Definitions

V_{CC}, GND, GND — $V_{CC} = 5V \pm 5\%$. The three supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. There are also two ground pins to reduce the low level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 9 address bits change in the same direction simultaneously. A recommended solution would be a 1μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected as close as possible to pins 36 and 38 to reduce lead inductance. See Figure below.

*Capacitor values should be chosen depending on the particular application.

R0-R8: Row Address Inputs.

C0-C8: Column Address Inputs.

Q0-Q8: Multiplexed Address Outputs — Selected from the Row Address Input Latch, the Column Address Input Latch, or the Refresh Counter.*

$\overline{RASIN}$: Row Address Strobe Input — Enables selected $\overline{RAS_n}$ output when M2 ($\overline{RFSH}$) is high, or all $\overline{RAS_n}$ outputs when $\overline{RFSH}$ is low.

R/$\overline{C}$ (RFCK) — In Auto-Refresh Mode this pin is the external Refresh Clock Input: one refresh cycle has to be performed each clock period. In all other modes it is Row/Column Select Input: selects either the row or column address input latch onto the output bus.

$\overline{CASIN}$ (RGCK) — In Auto-Refresh Mode, Auto Burst Mode, and All-$\overline{RAS}$ Auto-Write Mode, this pin is the $\overline{RAS}$ Generator Clock input. In all other modes it is $\overline{CASIN}$ (Column Address Strobe Input), which inhibits $\overline{CAS}$ output when high in Modes 4 and 3b. In Mode 6 it can be used to prolong $\overline{CAS}$ output.

ADS: Address (Latch) Strobe Input — Row Address, Column Address, and Bank Select Latches are fall-through with ADS high; Latches on high-to-low transition.

$\overline{CS}$: Chip Select Input — TRI-STATE's the Address Outputs and puts the control signal into a high-impedance logic "1" state when high (unless refreshing in one of the Refresh Modes). Enables all outputs when low.

M0, M1, M2: Mode Control Inputs — These 3 control pins determine the 8 major modes of operation of the DP8409 as depicted in Table 1.

Table 1. DP8409 Mode Select Options

Mode	(RFSH) M2	M1	M0	Mode of Operation	Conditions
0	0	0	0	Externally Controlled Refresh	RF I/O = $\overline{EOC}$
1	0	0	1	Auto Refresh — forced	RF I/O = Refresh Request ($\overline{RFRQ}$)
2	0	1	0	Internal Auto Burst Refresh	RF I/O = $\overline{EOC}$
3a	0	1	1	All $\overline{RAS}$ Auto Write	RF I/O = $\overline{EOC}$; All $\overline{RAS}$ Active
3b	0	1	1	Externally Controlled All $\overline{RAS}$ Access	All $\overline{RAS}$ Active
4	1	0	0	Externally Controlled Access	Active $\overline{RAS}$ defined by Table 2
5	1	0	1	Auto Access, Slow t_{RAH}, Hidden Refresh	Active $\overline{RAS}$ defined by Table 2
6	1	1	0	Auto Access, Fast t_{RAH}	Active $\overline{RAS}$ defined by Table 2
7	1	1	1	Set End of Count	See Table 3 for Mode 7

RF I/O — The I/O pin functions as a Reset Counter Input when set low from an external open-collector gate, or as a flag output. The flag goes active-low in Modes 0 and 2 when the End-of-Count output is at 127, 255, or 511 (see Table 3). in Auto-Refresh Mode it is the Refresh Request output.

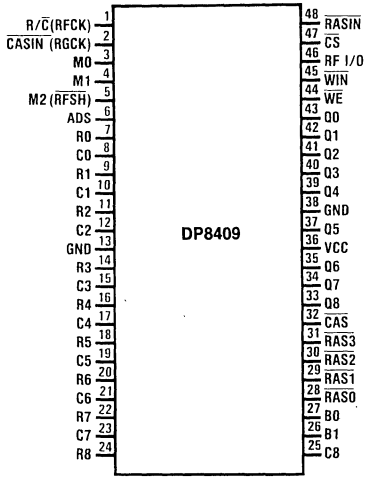
$\overline{WIN}$: Write Enable Input.

$\overline{WE}$: Write Enable Output — Buffered output from $\overline{WIN}$.*

$\overline{CAS}$: Column Address Strobe Output — In Modes 3a, 5, and 6, $\overline{CAS}$ transitions low following valid column address. In Modes 3b and 4, it goes low after R/$\overline{C}$ goes low, or follows $\overline{CASIN}$ going low if R/$\overline{C}$ is already low. $\overline{CAS}$ is high during refresh.*

$\overline{RAS}$ 0-3: Row Address Strobe Outputs — Selects a memory bank decoded from B1 and B0 (see Table 2), if $\overline{RFSH}$ is high. If $\overline{RFSH}$ is low, all banks are selected.*

B0, B1: Bank Select Inputs — Strobed by ADS. Decoded to enable one of the $\overline{RAS}$ outputs when $\overline{RASIN}$ goes low. Also used to define End-of-Count in Mode 7 (Table 3).



Order Number DP8409N, DP8409N-2, DP8409N-3, DP8409D, DP8409D-2, DP8409D-3
See NS package N48A or D48A

Pin Configuration

Conditions for all Modes

Input Addressing

The address block consists of a row-address latch, a column-address latch, and a resettable refresh counter. The address latches are fall-through when ADS is high and latch when ADS goes low. If the address bus contains valid addresses until after the valid address time, ADS can be permanently high. Otherwise ADS must go low while the addresses are still valid.

In normal memory access operation, $\overline{RASIN}$ and R/$\overline{C}$ are initially high. When the address inputs are enabled into the address latches, the row addresses appear on the Q outputs. The address strobe also inputs the bank-select address, (B0 and B1). If $\overline{CS}$ is low, all outputs are enabled. When $\overline{CS}$ is transitioned high, the address outputs go TRI-STATE and the control outputs first go high through a low impedance, and then are held by an on-chip high impedance. This allows output paralleling with other DP8409s for multi-addressing. All outputs go active about 50ns after the chip is selected again. If $\overline{CS}$ is high, and a refresh cycle begins, all the outputs become active until the end of the refresh cycle.

Drive Capability

The DP8409 has timing parameters that are specified with up to 600pF loads. In a typical memory system this is equivalent to about 88, 5V-only DRAMs, with trace lengths kept to a minimum. Therefore, the chip can drive four banks each of 16 or 22 bits, or two banks of 32 or 39 bits, or one bank of 64 or 72 bits.

Less loading will slightly reduce the timing parameters, and more loading will increase the timing parameters, according to the graph of Figure 10. The AC performance parameters are specified with the typical load capacitance of 88 DRAMs. This graph can be used to extrapolate the variations expected with other loading.

Because of distributed trace capacitance and inductance and DRAM input capacitance, current spikes can be created, causing overshoots and undershoots at the DRAM inputs that can change the contents of the DRAMs or even destroy them. To remove these spikes, a damping resistor (low inductance, carbon) can be inserted between the DP8409 driver outputs and the DRAMs, as close as possible to the DP8409. The values

of the damping resistors may differ between the different control outputs; $\overline{RAS}$'s, $\overline{CAS}$, Q's, and $\overline{WE}$. The damping resistors should be determined by the first prototypes (not wire-wrapped due to the larger distributed capacitance and inductance). The best values for the damping resistors are the critical values giving a critically damped transition on the control outputs. Typical values for the damping resistors will be between 15Ω and 100Ω, the lower the loading the higher the value. (For more information, see AN-305 "Precautions to Take When Driving Memories.")

DP8409 Driving any 16k or 64k DRAMs

The DP8409 can drive any 16k or 64k DRAMs. All 16k DRAMs are basically the same configuration, including the newer 5V-only version. Hence, in most applications, different manufacturers' DRAMs are interchangeable (for the same supply-rail chips), and the DP8409 can drive all 16k DRAMs (see Figure 1a).

There are three basic configurations for the 5V-only 64k DRAMs: a 128-row by 512-column array with an on-RAM refresh counter, a 128-row by 512-column array with no on-RAM refresh counter, and a 256-row by 256-column array with no on-RAM refresh counter. The DP8409 can drive all three configurations, and at the same time allows them all to be interchangeable (as shown in Figures 1b and 1c), providing maximum flexibility in the choice of DRAMs. Since the 9-bit on-chip refresh counter can be used as a 7-bit refresh counter for the 128-row configuration, or as an 8-bit refresh counter for the 256-row configuration, the on-RAM refresh counter (if present) is never used. As long as 128 rows are refreshed every 2ms (i.e. 256 rows in 4ms) all DRAM types are correctly refreshed.

DP8409 Interface Between System & DRAM Banks

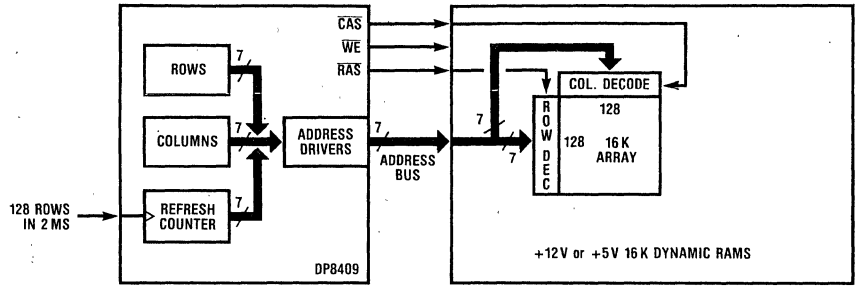


FIGURE 1a. DP8409 with any 16k DRAMS

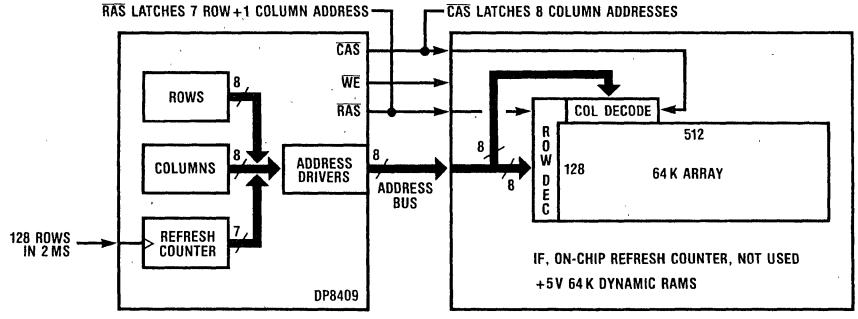


FIGURE 1b. DP8409 with 128 Row × 512 Column 64k DRAM

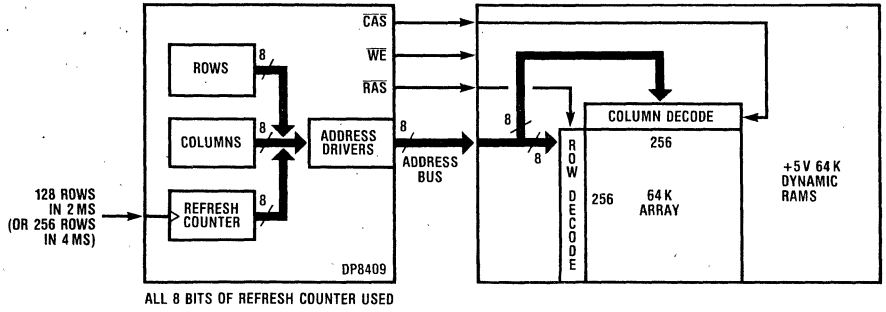


FIGURE 1c. DP8409 with 256 × 256 Column 64k DRAM

When the DP8409 is in a refresh mode, the RF I/O pin indicates that the on-chip refresh counter has reached its end-of-count. This end-of-count is selectable as 127, 255 or 512 to accommodate 16k, 64k, or 256k DRAMs. Although the end-of-count may be chosen to be any of these, the counter always counts to 511 before rolling over to zero.

Read, Write, and Read-Modify-Write Cycles

The output signal, $\overline{WE}$, determines what type of memory access cycle the memory will perform. If $\overline{WE}$ is kept high while $\overline{CAS}$ goes low, a read cycle occurs. If $\overline{WE}$ goes low before $\overline{CAS}$ goes low, a write cycle occurs and data at DI (DRAM input data) is written into the DRAM as $\overline{CAS}$ goes low. If $\overline{WE}$ goes low later than t_{CWD} after $\overline{CAS}$ goes low, first a read occurs and DO (DRAM output data) becomes valid; then data DI is written into the same address in the DRAM when $\overline{WE}$ goes low. In this read-modify-write case, DI and DO cannot be linked together. The type of cycle is therefore controlled by $\overline{WE}$, which follows $\overline{WIN}$.

Power-Up Initialize

When V_{CC} is first applied to the DP8409, an initialize pulse clears the refresh counter, the internal control flip-flops, and sets the End-of-Count of the refresh counter to 127 (which may be changed via Mode 7). As V_{CC} increases to about 2.3 volts, it holds the output control signals at a level of one Schottky diode-drop below V_{CC}, and the output address to TRI-STATE. As V_{CC} increases above 2.3 volts, control of these outputs is granted to the system.

DP8409 Functional Mode Descriptions

Note: All delay parameters stated in text refer to the DP8409. Substitute the respective delay numbers for the DP8409-2 or DP8409-3 when using these devices.

Mode 0 — Externally Controlled Refresh

Figure 2 is the Externally Controlled Refresh Timing. In this mode, the input address latches are disabled from the address outputs and the refresh counter is enabled. When $\overline{RAS}$ occurs, the enabled row in the DRAM is refreshed. In the Externally Controlled Refresh mode, all $\overline{RAS}$ outputs are enabled following $\overline{RASIN}$, and $\overline{CAS}$ is inhibited. This refreshes the same row in all four banks. The refresh counter increments when either $\overline{RASIN}$ or $\overline{RFSH}$ goes low-to-high after a refresh. RF I/O goes low when the count is 127, 255, or 511, as set by End-of-Count (see Table 3), with $\overline{RASIN}$ and $\overline{RFSH}$ low. To reset the counter to all zeroes, RF I/O is set low through an external open-collector driver.

During refresh, $\overline{RASIN}$ and RFSH must be skewed transitioning low such that the refresh address is valid on the address outputs of the controller before the $\overline{RAS}$ outputs go low. The amount of time that RFSH should go low before $\overline{RASIN}$ does depends on the capacitive loading of the address and $\overline{RAS}$ lines. For the load specified in the switching characteristics of this data sheet, 10ns is sufficient. Refer to Figure 2.

To perform externally controlled burst refresh, $\overline{RASIN}$ is toggled while RFSH is held low. The refresh counter increments with $\overline{RASIN}$ going low to high, so that the DRAM rows are refreshed in succession by $\overline{RASIN}$ going high to low.

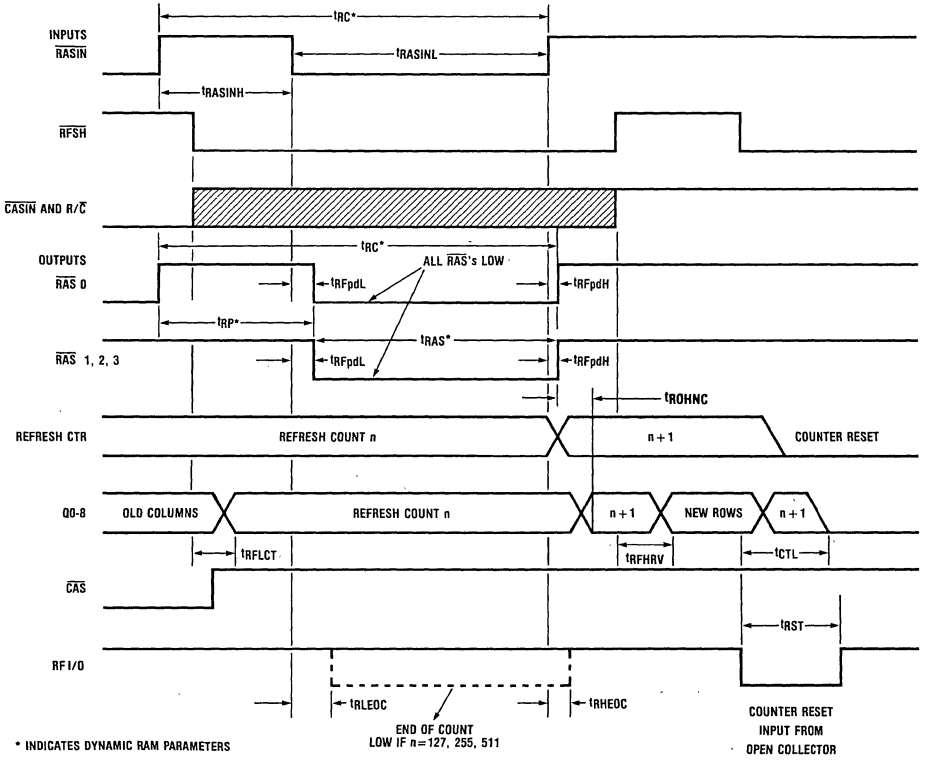


FIGURE 2. External Control Refresh Cycle (Mode 0)

Mode 1 — Automatic Forced Refresh

In Mode 1, the R/$\overline{C}$ (RFCK) pin becomes RFCK (refresh cycle clock), instead of R/$\overline{C}$, and $\overline{CAS}$ remains high. If RFCK is kept permanently high, then whenever M2 ($\overline{RFSH}$) goes low, an externally controlled refresh will occur and all $\overline{RAS}$ outputs will follow $\overline{RASIN}$, strobing the refresh counter contents to the DRAMs. The RF I/O pin will always output high, but when set low externally through an open-collector driver, the refresh counter resets as normal. This externally controlled method may be preferred when operating in the Automatic Access mode (Mode 5), where hidden or forced refreshing is undesirable, but refreshing is still necessary.

If RFCK is an input clock signal, one (and only one) refresh cycle must take place every RFCK cycle. Refer to Figure 9. If a hidden refresh does not occur while RFCK is high, in Mode 5, then RF I/O ($\overline{Refresh\ Request}$) goes low immediately after RFCK goes low, indicating to the system that a forced refresh is requested. The system must allow a forced refresh to take place while RFCK is low (refer to Figure 3). The $\overline{Refresh\ Request}$ signal on RF I/O may be connected to a $\overline{Hold}$ or $\overline{Bus\ Request}$ input to the system. The system acknowledges the $\overline{Hold}$ or $\overline{Bus\ Request}$ when ready, and outputs Hold Acknowledge or $\overline{Bus\ Request\ Acknowledge}$. If this is connected to the M2 ($\overline{RFSH}$) pin, a forced-refresh cycle will be initiated by the DP8409, and $\overline{RAS}$ will be internally generated on all four $\overline{RAS}$ outputs, to strobe the refresh counter contents on the address outputs into all the DRAMs. An external $\overline{RAS}$ Generator Clock ($\overline{RGCK}$) is required for this function. It is fed to the $\overline{CASIN}$ (RGCK) pin, and may be up to 10 MHz. Whenever M2 goes low (inducing a forced refresh), $\overline{RAS}$ remains high for one to two periods of RGCK, depending on when M2 goes low relative to the high-to-low triggering edge of RGCK; $\overline{RAS}$ then goes low for two periods, performing a refresh on all banks. In order to obtain the minimum delay from M2 going low to $\overline{RAS}$ going low, M2 should go low t_{RFSRG} before the next falling edge of RGCK. The Refresh Request on RF I/O is terminated as $\overline{RAS}$ begins, so that by the time the system has acknowledged the removal of the request and disabled its Acknowledge, (i.e., M2 goes high), Refresh $\overline{RAS}$ will have ended, and normal operations can begin again in the Automatic Access mode (Mode 5). If it is desired that Refresh $\overline{RAS}$ end in less than 2 periods of RGCK from the time $\overline{RAS}$ went low, then M2 may be high earlier than t_{RQHRF} after RGCK goes low and $\overline{RAS}$ will go high t_{RFRH} after M2, if $\overline{CS}$ is low. If $\overline{CS}$ is high, the $\overline{RAS}$ will go high impedance high after 25ns after M2 goes high.

To allow the forced refresh, the system will have been inactive for about 4 periods of RGCK, which can be as fast as 400 ns every RFCK cycle. To guarantee a refresh of 128 rows every 2 ms, a period of up to 16 μs is required for RFCK. In other words, the system may be down for as little as 400 ns every 16 μs, or 2.5% of the time. Although this is not excessive, it may be preferable to perform a Hidden Refresh each RFCK cycle, which is allowed while still in the Auto-Access mode, (Mode 5).

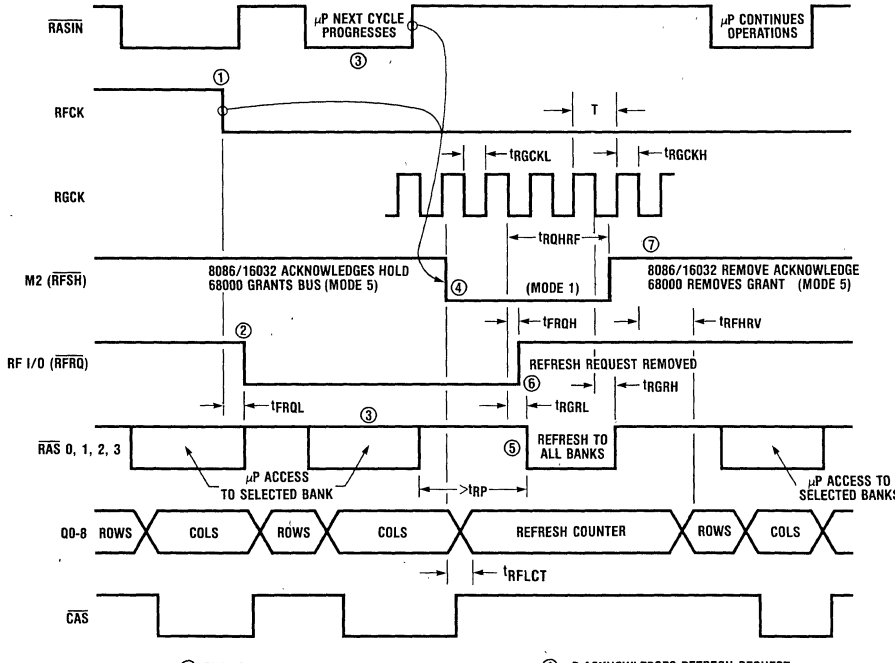


FIGURE 3. DP8409 Performing a Forced Refresh (Mode 5→1→5) with Various Microprocessors

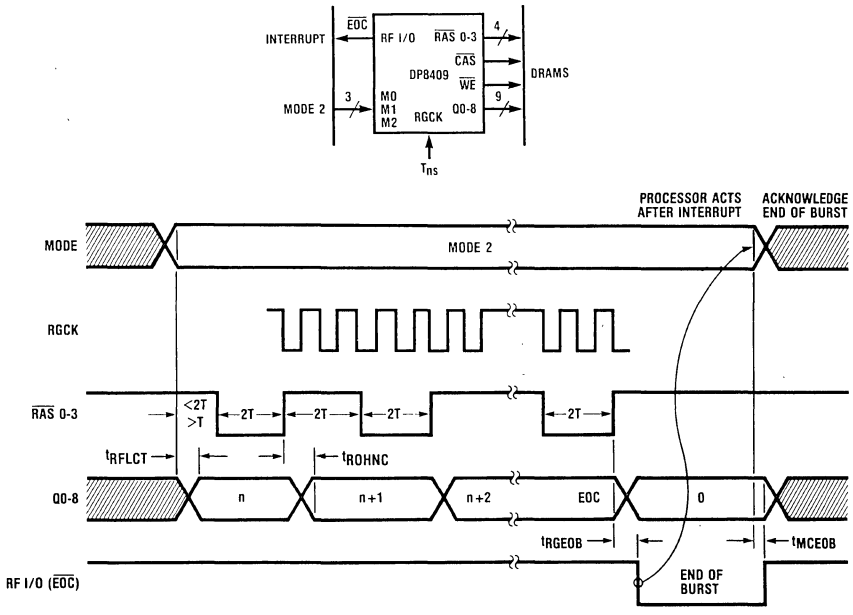


FIGURE 4. Auto-Burst Mode, Mode 2

Mode 2 — Automatic Burst Refresh

This mode is normally used before and/or after a DMA operation to ensure that all rows remain refreshed, provided the DMA transfer takes less than 2 ms (see Figure 4). When the DP8409 enters this mode, CASIN (RGCK) becomes the RAS Generator Clock (RGCK), and RASIN is disabled. CAS remains high, and RF I/O goes low when the refresh counter has reached the selected End-of-Count and the last RAS has ended. RF I/O then remains low until the Auto-Burst Refresh mode is terminated. RF I/O can therefore be used as an interrupt to indicate the End-of-Burst condition.

The signal on all four RAS outputs is just a divide-by-four of RGCK; in other words, if RGCK has a 100 ns period, RAS is high and low for 200 ns each cycle. The refresh counter increments at the end of each RAS, starting from the count it contained when the mode was entered. If this was zero, then for a RGCK with a 100 ns period with End-of Count set to 127, RF I/O will go low after $128 \times 0.4\,\mu s$, or $51.2\,\mu s$. During this time, the system may be performing operations that do not involve DRAM. If all rows need to be burst refreshed, the refresh counter may be cleared by setting RF I/O low externally before the burst begins.

Burst-mode refreshing is also useful when powering down systems for long periods of time, but with data retention still required while the DRAMs are in standby. To maintain valid refreshing, power can be applied to the DP8409 (set to Mode 2), causing it to perform a complete burst refresh. When end-of-burst occurs (after $26\,\mu s$), power can then be removed from the DP8409 for 2 ms, consuming an average power of 1.3% of normal operating power. No control signal glitches occur when switching power to the DP8409.

Mode 3a — All-RAS Automatic Write

Mode 3a is useful at system initialization, when the memory is being cleared (i.e., with all-zeroes in the data field and the corresponding check bits for error detection and correction). This requires writing the same data to each location of memory (every row of each column of each bank). All RAS outputs are activated, as in refresh, and so are CAS and WE. To write to all four banks simultaneously, every row is strobed in each column, in sequence, until data has been written to all locations.

To select this mode, B1 and B0 must have previously been set to 00, 01, or 10 in Mode 7, depending on the DRAM size. For example, for 16k DRAMs, B1 and B0 are 00. For 64k DRAMs, B1 and B0 are 01, so that for the configuration of Figure 1b, the 8 refresh counter bits are strobed by RAS into the 7 row addresses and the ninth column address. After this Automatic-Write process, B1 and B0 must be set again in Mode 7 to 00 to set End-of-Count to 127. For the configuration of Figure 1c, B1 and B0 set to 01 will work for Automatic-Write and End-of-Count equals 255.

In this mode, R/C is disabled, WE is permanently enabled low, and CASIN (RGCK) becomes RGCK. RF I/O goes low whenever the refresh counter is 127, 255, or 511 (as set by End-of-Count in Mode 7), and the RAS outputs are active.

Referring to Figure 5a, an external 8-bit counter (for 64k DRAMs) with TRI-STATE outputs is required and must be connected to the column address inputs. It is enabled only during this mode, and is clocked from RF I/O. The DP8409 refresh counter is used to address the rows, and the column address is supplied by the external counter. Every row for each column address is written to in all four banks. At the End-of-Count RF I/O goes low, which clocks the external counter.

Therefore, for each column address, the refresh counter first outputs row-0 to the address bus and all four $\overline{RAS}$ outputs strobe this row address into the DRAMs (see Figure 5b). A minimum of 30ns after $\overline{RAS}$ goes low (t_{RAH} = 30ns), the refresh counter is disabled and the column address input latch is enabled onto the address bus. About 14ns after the column address is valid, $\overline{CAS}$ goes low, (t_{ASC} = +14ns), strobing the column address into the DRAMs. When $\overline{RAS}$ and $\overline{CAS}$ go high the refresh counter increments to the next row and the cycle repeats. Since $\overline{WE}$ is kept low in this mode, the data at DI (input data) of the DRAMs is written into each row of the latched column. During each cycle $\overline{RAS}$ is high for two periods of RGCK and low for two periods, giving a total write-cycle time of 400ns minimum, which is adequate for most 16k and 64k DRAMs. On the last row of a column, RF I/O increments the external counter to the next column address.

At the end of the last column address, an interrupt is generated from the external counter to let the system know that initialization has been completed. During the entire initialization time, the system can be performing other initialization functions. This approach to memory initialization is both automatic and fast. For instance, if four banks of 64k DRAMs are used, and RGCK is 100ns, a write cycle to the same location in all four banks takes 400ns, so the total time taken in initializing the 64k DRAMs is 65k × 400ns or 26ms. When the system receives the interrupt, the external counter must be permanently disabled. ADS and $\overline{CS}$ are interfaced by the system, and the DP8409 mode is changed. The interrupt must then be disabled.

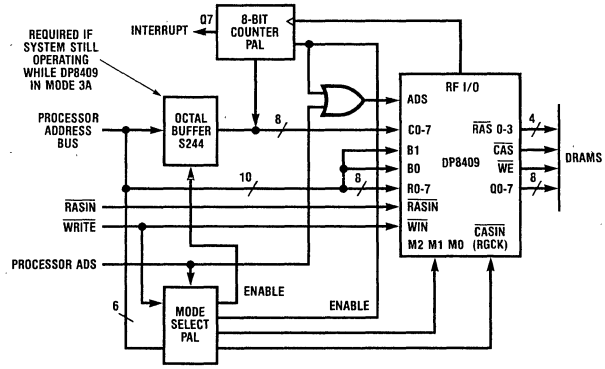


FIGURE 5a. DP8409 Extra Circuitry Required for All-$\overline{RAS}$ Auto Write Mode, Mode 3a

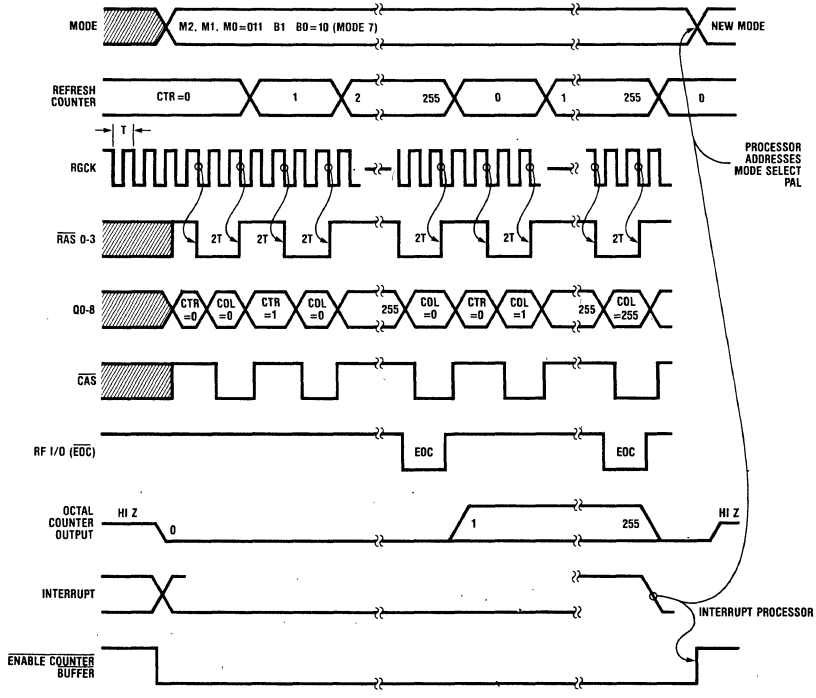


FIGURE 5b. DP8409 All-$\overline{RAS}$ Auto Write Mode, Mode 3a, Timing Waveform

Mode 3b — Externally Controlled All-$\overline{RAS}$ Write

To select this mode, B1 and B0 must first have been set to 11 in Mode 7. This mode is useful at system initialization, but under processor control. The memory address is provided by the processor, which also performs the incrementing. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$ (supplied by the processor), strobing the row address into the DRAMs. R/$\overline{C}$ can now go low, while $\overline{CASIN}$ may be used to control $\overline{CAS}$ (as in the Externally Controlled Access mode), so that $\overline{CAS}$ strobes the column address contents into the DRAMs. At this time $\overline{WE}$ should be low, causing the data to be written into all four banks of DRAMs. At the end of the write cycle, the input address is incremented and latched by the DP8409 for the next write cycle. This method is slower than Mode 3a since the processor must perform the incrementing and accessing. Thus the processor is occupied during RAM initialization, and is not free for other initialization operations. However, initialization sequence timing is under system control, which may provide some system advantage.

Mode 4 — Externally Controlled Access

This mode facilitates externally controlling all access-timing parameters associated with the DRAMs. The application of modes 0 and 4 are shown in Figure 6.

Output Address Selection

Refer to Figure 7a. With M2 ($\overline{RFSH}$) and R/$\overline{C}$ high, the row address latch contents are transferred to the multiplexed address bus output Q0-Q8, provided $\overline{CS}$ is set low. The column address latch contents are output after R/$\overline{C}$ goes low. $\overline{RASIN}$ can go low after the row addresses have been set up on Q0-Q8. This selects one of the $\overline{RAS}$ outputs, strobing the row address on the Q outputs into the desired bank of memory. After the row-address hold-time of the DRAMs, R/$\overline{C}$ can go low so that about 40 ns later column addresses appear on the Q outputs.

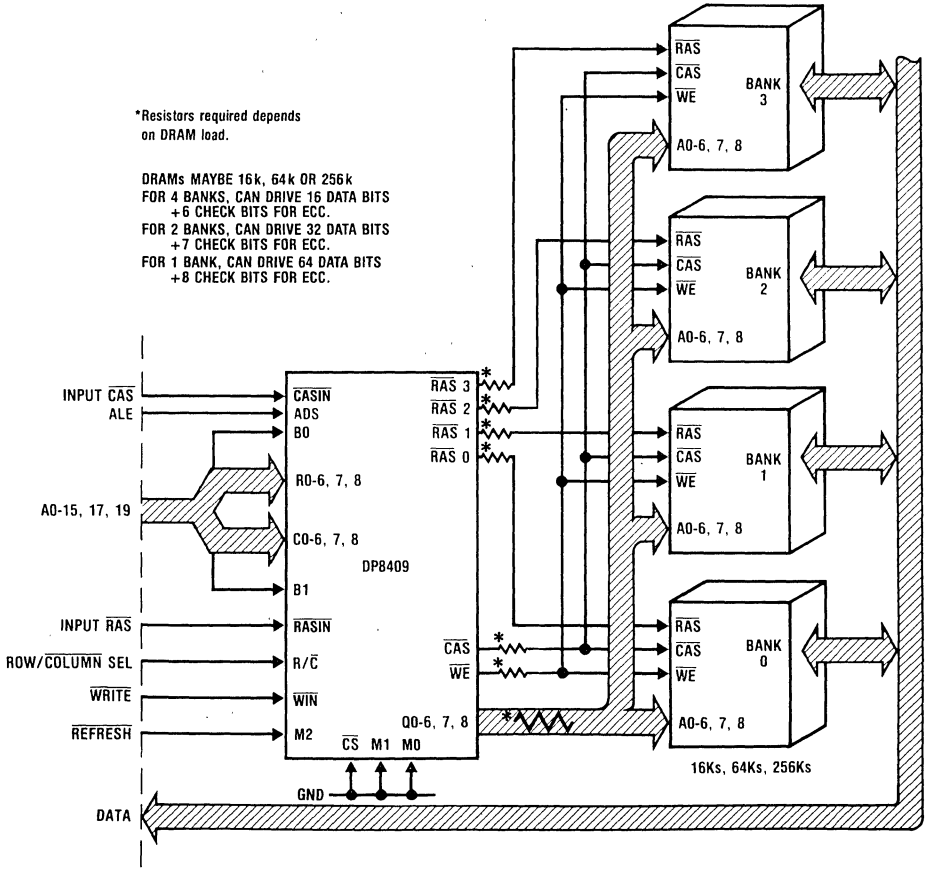


FIGURE 6. Typical Application of DP8409 Using External Control Access and Refresh in Modes 0 and 4

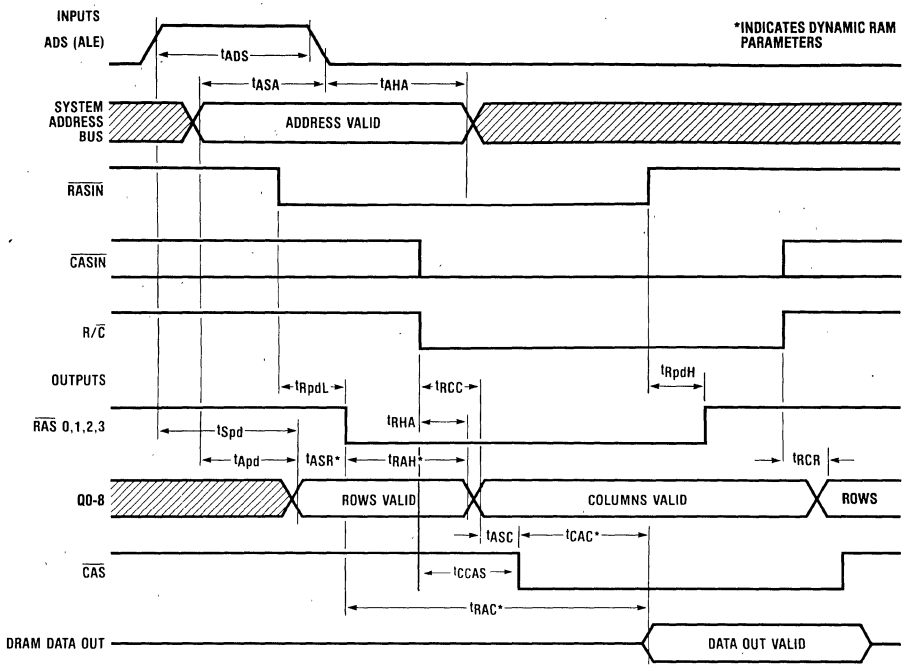


FIGURE 7a. Read Cycle Timing (MODE 4)

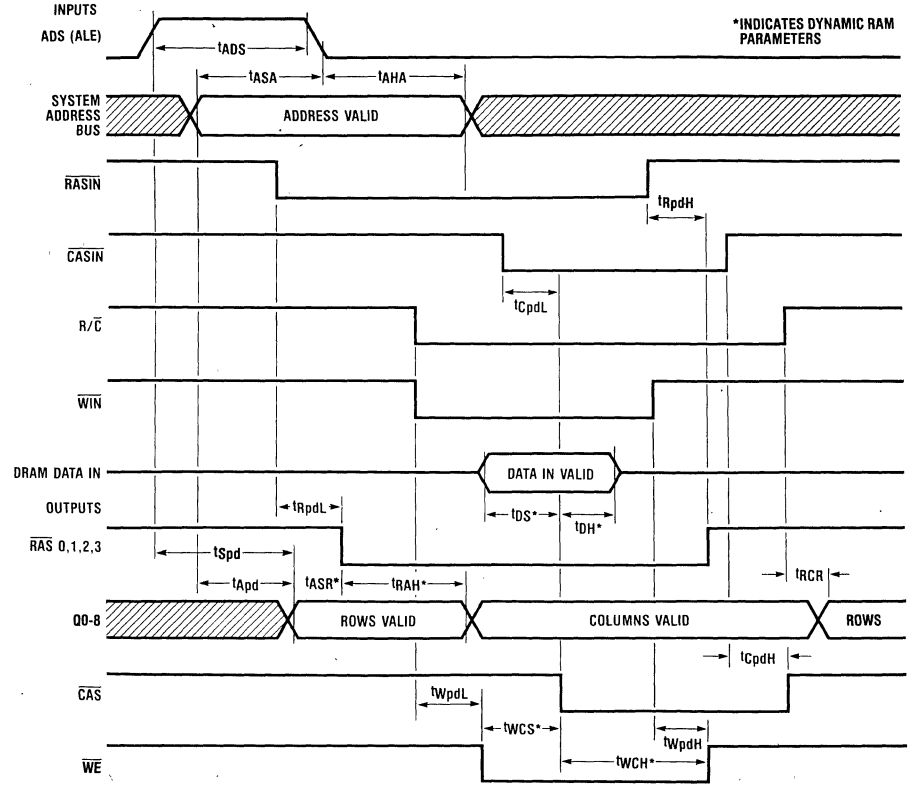


FIGURE 7b. Write Cycle Timing (Mode 4)

Automatic CAS Generation

In a normal memory access cycle $\overline{CAS}$ can be derived from inputs $\overline{CASIN}$ or R/$\overline{C}$. If $\overline{CASIN}$ is high, then R/$\overline{C}$ going low switches the address output drivers from rows to columns. $\overline{CASIN}$ then going low causes $\overline{CAS}$ to go low approximately 40 ns later, allowing $\overline{CAS}$ to occur at a predictable time (see Figure 7b). If $\overline{CASIN}$ is low when R/$\overline{C}$ goes low, $\overline{CAS}$ will be automatically generated, following the row to column transition by about 20 ns (see Figure 7a). Most DRAMs have a column address set-up time before $\overline{CAS}$ (t_{ASC}) of 0 ns or − 10 ns. In other words, a t_{ASC} greater than 0 ns is safe.

Fast Memory Access

AC parameters t_{DIF1}, t_{DIF2} may be used to determine the minimum delays required between $\overline{RASIN}$, R/$\overline{C}$, and $\overline{CASIN}$ (see Application Brief 9; "Fastest DRAM Access Mode").

Mode 5 — Automatic Access with Hidden Refresh

The Auto Access with Hidden Refresh mode has two advantages over the Externally Controlled Access mode, due to the fact that all outputs except $\overline{WE}$ are initiated from $\overline{RASIN}$. First, inputs R/$\overline{C}$ and $\overline{CASIN}$ are unnecessary and can be used for other functions (see Refreshing, below). Secondly, because the output control signals are derived internally from one input signal ($\overline{RASIN}$), timing-skew problems are reduced, thereby reducing memory access time substantially or allowing use of slower DRAMs. The automatic access features of Mode 5 (and Mode 6) of the DP8409 make DRAM accessing appear essentially "static".

Automatic Access Control

The major disadvantage of DRAMs compared to static RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for t_{RAH}, (the Row-Address hold-time of the DRAM), the column address is set up and then $\overline{CAS}$ occurs. This is all performed automatically by the DP8409 in this mode.

Provided the input address is valid as ADS goes low, $\overline{RASIN}$ can go low any time after ADS. This is because the selected $\overline{RAS}$ occurs typically 27 ns later, by which time the row address is already valid on the address output of the DP8409. The Address Set-Up time (t_{ASR}), is 0 ns on most DRAMs. The DP8409 in this mode (with ADS and $\overline{RASIN}$ edges simultaneously applied) produces a minimum t_{ASR} of 0 ns. This is true provided the input address was valid t_{ASA} before ADS went low (see Figure 8a).

Next, the row address is disabled after t_{RAH} (30 ns minimum); in most DRAMs, t_{RAH} minimum is less than 30 ns. The column address is then set up and t_{ASC} later, $\overline{CAS}$ occurs. The only other control input required is $\overline{WIN}$. When a write cycle is required, $\overline{WIN}$ must go low at least 30 ns before $\overline{CAS}$ is output low.

This gives a total typical delay from: input address valid to $\overline{RASIN}$ (15 ns); to $\overline{RAS}$ (27 ns); to rows held (50 ns); to columns valid (25 ns); to $\overline{CAS}$ (23 ns) = 140 ns (that is, 125 ns from $\overline{RASIN}$). All of these typical figures are for heavy capacitive loading, of approximately 88 DRAMs.

This mode is therefore extremely fast. The external timing is greatly simplified for the memory system designer: the only system signal required is $\overline{RASIN}$.

Refreshing

Because R/$\overline{C}$ and $\overline{CASIN}$ are not used in this mode, R/$\overline{C}$ becomes RFCK (refresh clock) and $\overline{CASIN}$ becomes RGCK ($\overline{RAS}$ generator clock). With these two signals it is possible to perform refreshing without extra ICs, and without holding up the processor.

One refresh cycle must occur during each refresh clock period and then the refresh address must be incremented to the next refresh cycle. As long as 128 rows are refreshed every 2 ms (one row every 16 μs), all 16k and 64k DRAMs will be correctly refreshed. The cycle time of RFCK must, therefore, be less than 16 μs. RFCK going high sets an internal refresh-request flip-flop. First the DP8409 will attempt to perform a hidden refresh so that the system throughput will not be affected. If, during the time RFCK is high, $\overline{CS}$ on the DP8409 goes high and $\overline{RASIN}$ occurs, a hidden refresh will occur. In this case, $\overline{RASIN}$ should be considered a common read/write strobe. In other words, if the processor is accessing elsewhere (other than the DRAMs) while RFCK is high, the DP8409 will perform a refresh. The refresh counter is enabled to the address outputs whenever $\overline{CS}$ goes high with RFCK high, and all $\overline{RAS}$ outputs follow $\overline{RASIN}$. If a hidden refresh is taking place as RFCK goes low, the refresh continues. At the start of the hidden refresh, the refresh-request flip-flop is reset so no further refresh can occur until the next RFCK period starts with the positive-going edge of RFCK. Refer to Figure 9.

To determine the probability of a Hidden Refresh occurring, assume each system cycle takes 400 ns and RFCK is high for 8 μs, then the system has 20 chances to not select the DP8409. If during this time a hidden refresh did not occur, then the DP8409 forces a refresh while RFCK is low, but the system chooses when the refresh takes place. After RFCK goes low, (and the internal-request flip-flop has not been reset), RF I/O goes low indicating that a refresh is requested to the system. Only when the system acknowledges this request by setting M2 ($\overline{RFSH}$) low does the DP8409 initiate a forced refresh (which is performed automatically). Refer to Mode 1, and Figure 3. The internal refresh request flip-flop is then reset.

Figure 9 illustrates the refresh alternatives in Mode 5. If a hidden refresh has occurred and $\overline{CS}$ again goes high before RFCK goes low, the chip is deselected. All the control signals go high-impedance high (logic "1") and the address outputs go TRI-STATE until $\overline{CS}$ again goes low. This mode (combined with Mode 1) allows very fast access, and automatic refreshing (possibly not even slowing down the system), with no extra ICs. Careful system design can, and should, provide a higher probability of hidden refresh occurring. The duty cycle of RFCK need not be 50-percent; in fact, the low-time should be designed to be a minimum. This is determined by the worst-case time (required by the system) to respond to the DP8409's forced-refresh request.

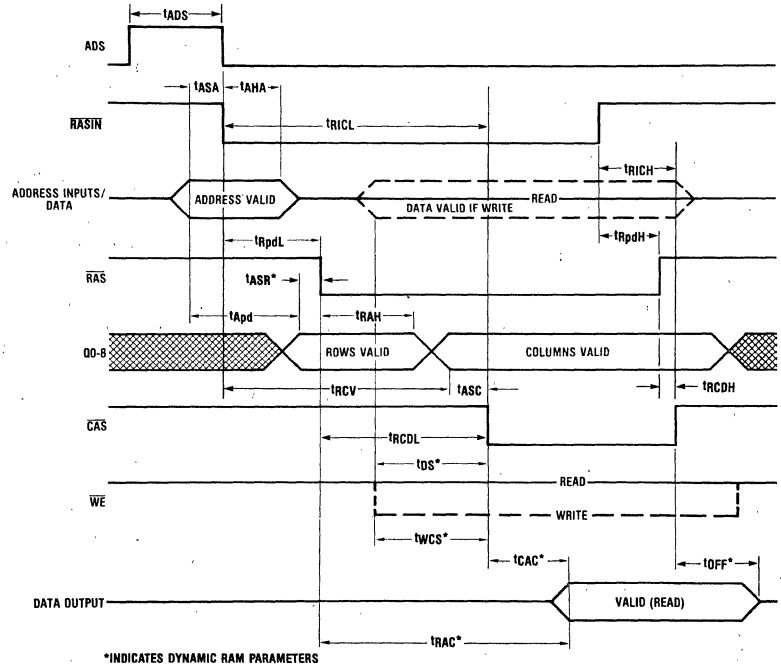


FIGURE 8a. Modes 5, 6 Timing ($\overline{\text{CASIN}}$ High in Mode 6)

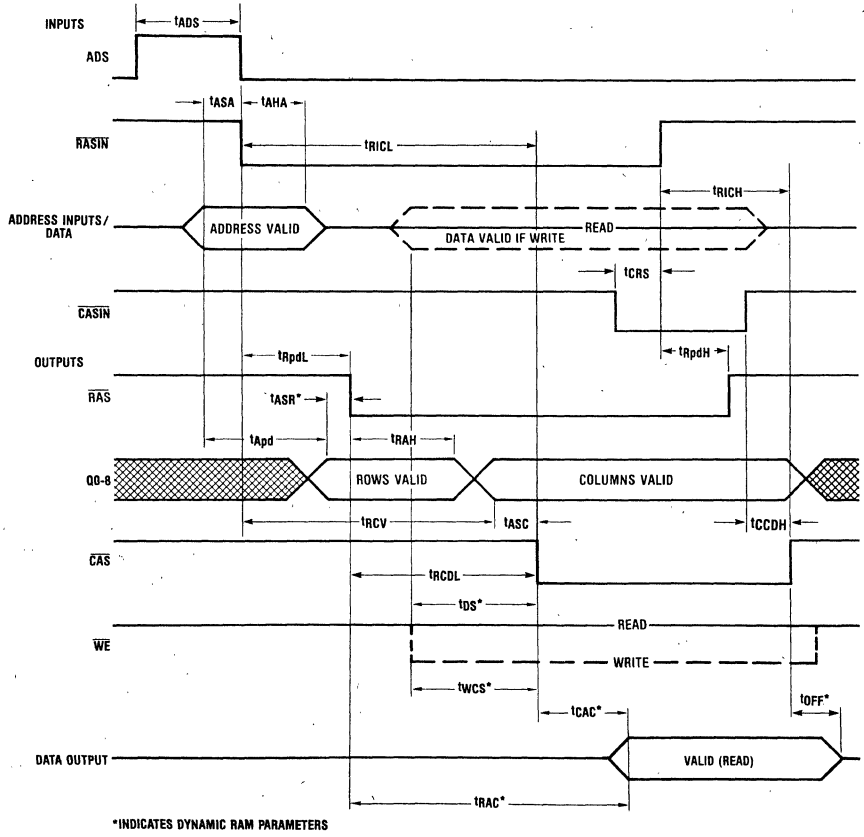
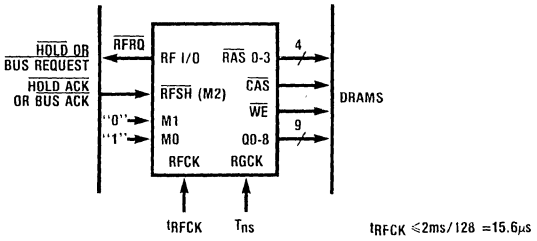


FIGURE 8b. Mode 6 Timing, Extended $\overline{\text{CAS}}$



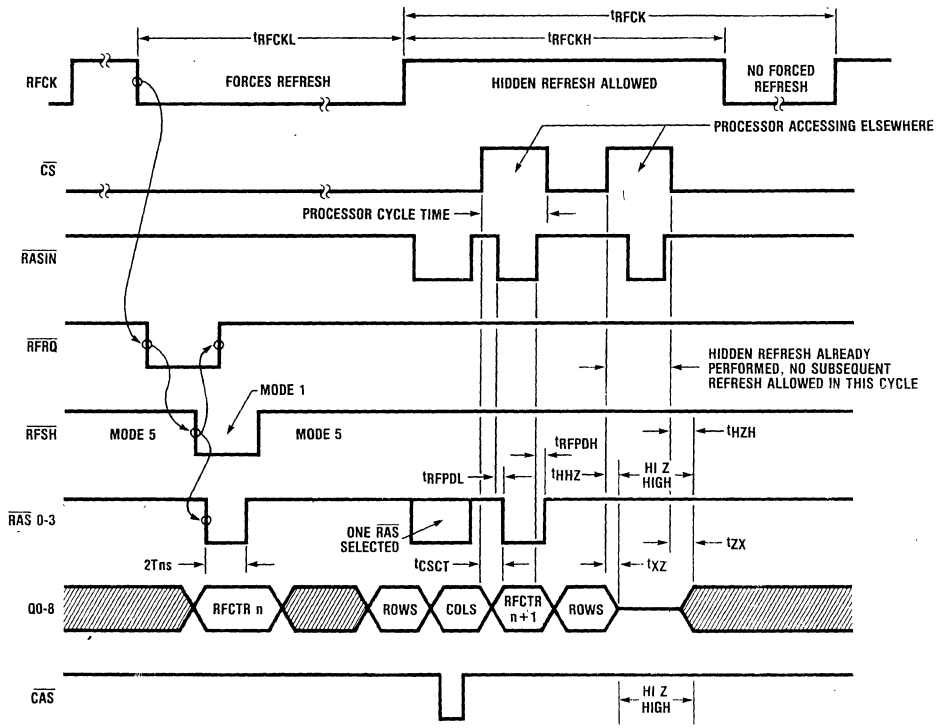


FIGURE 9. Hidden Refreshing (Mode 5) and Forced Refreshing (Mode 1) Timing

Table 2. Memory Bank Decode

Bank Select (Strobed by ADS)		Enabled $\overline{RAS}_n$
B1	B0	
0	0	$\overline{RAS}_0$
0	1	$\overline{RAS}_1$
1	0	$\overline{RAS}_2$
1	1	$\overline{RAS}_3$

Note that $\overline{RASIN}$ going low earlier than t_{CSRL} after $\overline{CS}$ goes low may result in the DP8409 interpreting the $\overline{RASIN}$ as a hidden refresh $\overline{RASIN}$ if no hidden refresh has occurred in the current RFCK cycle. In this case, all $\overline{RAS}$ outputs would go low for a short time. Thus, it is suggested that when using Mode 5, $\overline{RASIN}$ should be held high until t_{CSRL} after $\overline{CS}$ goes low if a refresh is not intended. Similarly, $\overline{CS}$ should be held low for a minimum of t_{CSRL} after $\overline{RASIN}$ returns high when ending the access in Mode 5.

Mode 6 — Fast Automatic Access

The Fast Access mode is similar to Mode 5, but has a faster t_{RAH} of 20ns, minimum. It therefore can only be used with fast 16k or 64k DRAMs (which have a t_{RAH} of 10ns to 15ns) in applications requiring fast access times; $\overline{RASIN}$ to $\overline{CAS}$ is typically 105ns.

In this mode, the R/$\overline{C}$ (RFCK) pin is not used, but $\overline{CASIN}$ (RGCK) is used as $\overline{CASIN}$ to allow an extended $\overline{CAS}$ after $\overline{RAS}$ has already terminated. Refer to Figure 8b. This is desirable with fast cycle-times where $\overline{RAS}$ has to be terminated as soon as possible before the next $\overline{RAS}$ begins (to meet the precharge time, or t_{RP}, requirements of the DRAM). $\overline{CAS}$ may then be held low by $\overline{CASIN}$ to extend the data output valid time from the DRAM to allow the system to read the data. $\overline{CASIN}$ subsequently going high ends $\overline{CAS}$. If this extended $\overline{CAS}$ is not required, $\overline{CASIN}$ should be set high in Mode 6.

There is no internal refresh-request flip-flop in this mode, so any refreshing required must be done by entering Mode 0 or Mode 2.

Mode 7 — Set End-of-Count

The End-of-Count can be externally selected in Mode 7, using ADS to strobe in the respective value of B1 and B0 (see Table 3). With B1 and B0 the same $\overline{EOC}$ is 127; with B1 = 0 and B0 = 1, $\overline{EOC}$ is 255; and with B1 = 1 and B0 = 0, $\overline{EOC}$ is 511. This selected value of $\overline{EOC}$ will be used until the next Mode 7 selection. At power-up the $\overline{EOC}$ is automatically set to 127 (B1 and B0 set to 11).

Table 3. Mode 7

Bank Select (Strobed by ADS)		End of Count Selected
B1	B0	
0	0	127
0	1	255
1	0	511
1	1	127

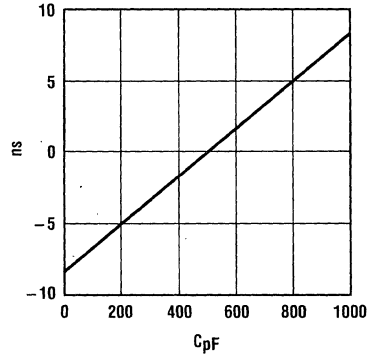


FIGURE 10. Change in Propagation Delay vs. Loading Capacitance Relative to a 500pF Load

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Storage Temperature Range	−65°C to +150°C
Input Voltage	5.5V
Output Current	150mA
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 23.6mW/°C above 25°C; derate molded package 22.7mW/°C above 25°C.

Maximum Power Dissipation* at 25°C	
Cavity Package	3542mW
Molded Package	2833mW

Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.75	5.25	V
T_A Ambient Temperature	0	+70	°C

Electrical Characteristics $V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ unless otherwise noted (Notes 2, 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_C	Input Clamp Voltage	V_{CC} = Min., $I_C = -12mA$		−0.8	−1.2	V
I_{IH1}	Input High Current for ADS, R/$\overline{C}$ only	$V_{IN} = 2.5V$		2.0	100	μA
I_{IH2}	Input High Current for All Other Inputs*	$V_{IN} = 2.5V$		1.0	50	μA
I_I RSI	Output Load Current for RF I/O	$V_{IN} = 0.5V$, Output High		−1.5	−2.5	mA
I_I CTL	Output Load Current for $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	$V_{IN} = 0.5V$, Chip Deselect		−1.5	−2.5	mA
I_{IL1}	Input Low Current for ADS, R/$\overline{C}$ only	$V_{IN} = 0.5V$		−0.1	−1.0	mA
I_{IL2}	Input Low Current for All Other Inputs*	$V_{IN} = 0.5V$		−0.05	−0.5	mA
V_{IL}	Input Low Threshold				0.8	V
V_{IH}	Input High Threshold		2.0			V
V_{OL1}	Output Low Voltage*	$I_{OL} = 20mA$		0.3	0.5	V
V_{OL2}	Output Low Voltage for RF I/O	$I_{OL} = 10mA$		0.3	0.5	V
V_{OH1}	Output High Voltage*	$I_{OH} = -1mA$	2.4	3.5		V
V_{OH2}	Output High Voltage for RF I/O	$I_{OH} = -100\mu A$	2.4	3.5		V
I_{1D}	Output High Drive Current*	$V_{OUT} = 0.8V$ (Note 3)		−200		mA
I_{0D}	Output Low Drive Current*	$V_{OUT} = 2.7V$ (Note 3)		200		mA
I_{OZ}	TRI-STATE Output Current (Address Outputs)	$0.4V \leq V_{OUT} \leq 2.7V$, $\overline{CS} = 2.0V$, Mode 4	−50	1.0	50	μA
I_{CC}	Supply Current	V_{CC} = Max.		250	325	mA

*Except RF I/O Output.

Switching Characteristics: DP8409/DP8409-3 $V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0-Q8, $C_L = 500pF$; $\overline{RAS0}$-$\overline{RAS3}$, $C_L = 150pF$; $\overline{WE}$, $C_L = 500pF$; $\overline{CAS}$, $C_L = 600pF$, unless otherwise noted. See Figure 11 for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Access Parameter	Conditions	8409			8409 – 3			Units
			Min	Typ	Max	Min	Typ	Max	
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a	95	125	160	95	125	185	ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b	80	105	140	80	105	160	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a	40	48	60	40	48	70	ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b	50	63	80	50	63	95	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a		98	125		98	145	ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b		78	105		78	120	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a		27	40		27	40	ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 8a		40	65		40	65	ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 8b	40	54	70	40	54	80	ns
t_{RAH}	Row Address Hold Time (Mode 5)	Figure 8a	30			30			ns
t_{RAH}	Row Address Hold Time (Mode 6)	Figures 8a, 8b	20			20			ns
t_{ASC}	Column Address Setup Time (Mode 5)	Figure 8a	8			8			ns
t_{ASC}	Column Address Setup Time (Mode 6)	Figures 8a, 8b	6			6			ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	Figure 8a		90	120		90	140	ns

Switching Characteristics (Cont'd)

Symbol	Access Parameter	Conditions	8409			8409 – 3			Units
			Min	Typ	Max	Min	Typ	Max	
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	Figures 8a, 8b		75	105		75	120	ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 7a, 7b, 8a, 8b	20	27	35	20	27	40	ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 7a, 7b, 8a, 8b	15	23	32	15	23	37	ns
t_{APDL}	Address Input to Output Low Delay	Figures 7a, 7b, 8a, 8b		25	40		25	46	ns
t_{APDH}	Address Input to Output High Delay	Figures 7a, 7b, 8a, 8b		25	40		25	46	ns
t_{SPDL}	Address Strobe to Address Output Low	Figures 7a, 7b		40	60		40	70	ns
t_{SPDH}	Address Strobe to Address Output High	Figures 7a, 7b		40	60		40	70	ns
t_{ASA}	Address Set-up Time to ADS	Figures 7a, 7b, 8a, 8b	15			15			ns
t_{AHA}	Address Hold Time from ADS	Figures 7a, 7b, 8a, 8b	15			15			ns
t_{ADS}	Address Strobe Pulse Width	Figures 7a, 7b, 8a, 8b	30			30			ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 7b	15	25	30	15	25	35	ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 7b	15	30	60	15	30	70	ns
t_{CRS}	$\overline{CASIN}$ Set-up Time to $\overline{RASIN}$ High (Mode 6)	Figure 8b	35			35			ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	Figure 7b	32	41	68	32	41	77	ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	Figure 7b	25	39	50	25	39	60	ns
t_{RCC}	Column Select to Column Address Valid	Figure 7a		40	58		40	67	ns
t_{RCR}	Row Select to Row Address Valid	Figures 7a, 7b		40	58		40	67	ns
t_{RHA}	Row Address Held from Column Select	Figure 7a	10			10			ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low (Mode 4 Auto $\overline{CAS}$)	Figure 7a		65	90				ns
t_{DIF1}	Maximum ($t_{RPDL} - t_{RHA}$)	See Mode 4 description			13			18	ns
t_{DIF2}	Maximum ($t_{RCC} - t_{CPDL}$)	See Mode 4 description			13			18	ns
	Refresh Parameter								
t_{RC}	Refresh Cycle Period	Figure 2	100			100			ns
$t_{RASINL,H}$	Pulse Width of $\overline{RASIN}$ during Refresh	Figure 2	50			50			ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figures 2, 9	35	50	70	35	50	80	ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figures 2, 9	30	40	55	30	40	65	ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS}$ = X, Figures 2,3,4		47	60		47	70	ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	Figures 2, 3		45	60		45	70	ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	Figures 2, 4		30	55		30	55	ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	C_L = 50pF, Figure 2			80			80	ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	C_L = 50pF, Figure 2			80			80	ns
t_{RGEOB}	RGCK Low to End-of-Burst Low	C_L = 50pF, Figure 4			95			95	ns
t_{MCEOB}	Mode Change to End-of-Burst High	C_L = 50pF, Figure 4			75			75	ns
t_{RST}	Counter Reset Pulse Width	Figure 2	70			70			ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	Figure 2			100			100	ns
$t_{RFCKL,H}$	Minimum Pulse Width of RFCK	Figure 9	100			100			ns
T	Period of $\overline{RAS}$ Generator Clock	Figure 3	100			100			ns
t_{RGCKL}	Minimum Pulse Width Low of RGCK	Figure 3	35			40			ns
t_{RGCKH}	Minimum Pulse Width High of RGCK	Figure 3	35			40			ns
t_{FRQL}	RFCK Low to Forced $\overline{RFRQ}$ Low	C_L = 50pF, Figure 3		20	30		20	30	ns

Switching Characteristics (Cont'd)

Symbol	Refresh Parameter	Conditions	8409			8409 – 3			Units
			Min	Typ	Max	Min	Typ	Max	
t_{FRQH}	RGCK Low to Forced $\overline{RFRQ}$ High	$C_L = 50pF$, Figure 3		50	75		50	75	ns
t_{RGRL}	RGCK Low to $\overline{RAS}$ Low	Figure 3	50	65	95	50	65	95	ns
t_{RGRH}	RGCK Low to $\overline{RAS}$ High	Figure 3	40	60	85	40	60	85	ns
t_{RQHRF}	$\overline{RFSH}$ Hold Time from $\overline{RFSH}$ $\overline{RQST}$ (RF I/O)	Figure 3	2T			2T			ns
t_{RFRH}	$\overline{RFSH}$ High to $\overline{RAS}$ High (ending forced RFSH)	See Mode 1 Descrip.	55	80	110	55	80	125	ns
t_{RFSRG}	$\overline{RFSH}$ Low Set-up to RGCK Low (Mode 1)	See Mode 1 Descrip.	35			40			ns
t_{CSCT}	$\overline{CS}$ High to RFSH Counter Valid	Figure 9		55	70		55	75	ns
t_{CSRL}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low	See Mode 5 Descrip.	10			15			ns
	TRI-STATE Parameter								
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi-Z from High	$C_L = 15pF$, Figures 9, 12 R2 = 1k, S1 open		20	40		20	40	ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60		35	60	ns
t_{LZ}	$\overline{CS}$ High to Address Output Hi-Z from Low	$C_L = 15pF$, Figures 9, 12, R1 = 1k, S2 open		25	50		25	50	ns
t_{HZH}	$\overline{CS}$ Low to Control Output High from Hi-Z High	Figures 9, 12 R2 = 750Ω, S1 open		50	80		50	80	ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z High from High	$C_L = 15pF$, Figures 9, 12 R2 = 750Ω, S1 open		40	75		40	75	ns
t_{HZL}	$\overline{CS}$ Low to Control Output Low from Hi-Z High	Figure 12, S1, S2 open		45	75		45	75	ns
t_{LHZ}	$\overline{CS}$ High to Control Output Hi-Z High from Low	$C_L = 15pF$, Figure 12, R2 = 750Ω, S1 open		50	80		50	80	ns

Switching Characteristics: DP8409-2

$V_{CC} = 5.0V \pm 5\%$, $0°C \leq T_A \leq 70°C$ unless otherwise noted (Notes 2, 4, 5). The output load capacitance is typical for 4 banks of 22 DRAMs each or 88 DRAMs including trace capacitance. These values are: Q0-Q8, $C_L = 500pF$; $\overline{RAS0}$-$\overline{RAS3}$, $C_L = 150pF$; $\overline{WE}$, $C_L = 500pF$; $\overline{CAS}$, $C_L = 600pF$, unless otherwise noted. See Figure 11 for test load. Switches S1 and S2 are closed unless otherwise noted, and R1 and R2 are 4.7kΩ unless otherwise noted. Maximum propagation delays are specified with all outputs switching.

Symbol	Access Parameter	Conditions	8409 – 2						Units
			Min	Typ	Max	Min	Typ	Max	
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a	75	100	130				ns
t_{RICL}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b	65	90	115				ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a	40	48	60				ns
t_{RICH}	$\overline{RASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b	50	63	80				ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a		75	100				ns
t_{RCDL}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figures 8a, 8b		65	85				ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 5)	Figure 8a		27	40				ns
t_{RCDH}	$\overline{RAS}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 8a		40	65				ns
t_{CCDH}	$\overline{CASIN}$ to $\overline{CAS}$ Output Delay (Mode 6)	Figure 8b	40	54	70				ns
t_{RAH}	Row Address Hold Time (Mode 5) (Note 7)	Figure 8a	20						ns

Switching Characteristics (Cont'd)

Symbol	Access Parameter	Conditions	8409 – 2						Units
			Min	Typ	Max	Min	Typ	Max	
t_{RAH}	Row Address Hold Time (Mode 6) (Note 7)	Figures 8a, 8b	12						ns
t_{ASC}	Column Address Setup Time (Mode 5)	Figure 8a	3						ns
t_{ASC}	Column Address Setup Time (Mode 6)	Figures 8a, 8b	3						ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 5)	Figure 8a		80	105				ns
t_{RCV}	$\overline{RASIN}$ to Column Address Valid (Mode 6)	Figures 8a, 8b		70	90				ns
t_{RPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 7a, 7b, 8a, 8b	20	27	35				ns
t_{RPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay	Figures 7a, 7b, 8a, 8b	15	23	32				ns
t_{APDL}	Address Input to Output Low Delay	Figures 7a, 7b, 8a, 8b		25	40				ns
t_{APDH}	Address Input to Output High Delay	Figures 7a, 7b, 8a, 8b		25	40				ns
t_{SPDL}	Address Strobe to Address Output Low	Figures 7a, 7b		40	60				ns
t_{SPDH}	Address Strobe to Address Output High	Figures 7a, 7b		40	60				ns
t_{ASA}	Address Set-up Time to ADS	Figures 7a, 7b, 8a, 8b	15						ns
t_{AHA}	Address Hold Time from ADS	Figures 7a, 7b, 8a, 8b	15						ns
t_{ADS}	Address Strobe Pulse Width	Figures 7a, 7b, 8a, 8b	30						ns
t_{WPDL}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 7b	15	25	30				ns
t_{WPDH}	$\overline{WIN}$ to $\overline{WE}$ Output Delay	Figure 7b	15	30	60				ns
t_{CRS}	$\overline{CASIN}$ Set-up Time to $\overline{RASIN}$ High (Mode 6)	Figure 8b	35						ns
t_{CPDL}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	Figure 7b	32	41	58				ns
t_{CPDH}	$\overline{CASIN}$ to $\overline{CAS}$ Delay (R/$\overline{C}$ low in Mode 4)	Figure 7b	25	39	50				ns
t_{RCC}	Column Select to Column Address Valid	Figure 7a		40	58				ns
t_{RCR}	Row Select to Row Address Valid	Figures 7a, 7b		40	58				ns
t_{RHA}	Row Address Held from Column Select	Figure 7a	10						ns
t_{CCAS}	R/$\overline{C}$ Low to $\overline{CAS}$ Low (Mode 4 Auto $\overline{CAS}$)	Figure 7a		55	75				ns
t_{DIF1}	Maximum ($t_{RPDL} - t_{RHA}$)	See Mode 4 description			13				ns
t_{DIF2}	Maximum ($t_{RCC} - t_{CPDL}$)	See Mode 4 description			13				ns
	Refresh Parameter								
t_{RC}	Refresh Cycle Period	Figure 2	100						ns
$t_{RASINL,H}$	Pulse Width of $\overline{RASIN}$ during Refresh	Figure 2	50						ns
t_{RFPDL}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figures 2, 9	35	50	70				ns
t_{RFPDH}	$\overline{RASIN}$ to $\overline{RAS}$ Delay during Refresh	Figures 2, 9	30	40	55				ns
t_{RFLCT}	$\overline{RFSH}$ Low to Counter Address Valid	$\overline{CS}$ = X, Figures 2,3,4		47	60				ns
t_{RFHRV}	$\overline{RFSH}$ High to Row Address Valid	Figures 2, 3		45	60				ns
t_{ROHNC}	$\overline{RAS}$ High to New Count Valid	Figures 2, 4		30	55				ns
t_{RLEOC}	$\overline{RASIN}$ Low to End-of-Count Low	C_L = 50pF, Figure 2			80				ns
t_{RHEOC}	$\overline{RASIN}$ High to End-of-Count High	C_L = 50pF, Figure 2			80				ns
t_{RGEOB}	RGCK Low to End-of-Burst Low	C_L = 50pF, Figure 4			95				ns
t_{MCEOB}	Mode Change to End-of-Burst High	C_L = 50pF, Figure 4			75				ns
t_{RST}	Counter Reset Pulse Width	Figure 2	70						ns
t_{CTL}	RF I/O Low to Counter Outputs All Low	Figure 2			100				ns

Switching Characteristics (Cont'd)

Symbol	Access Parameter	Conditions	8409 – 2						Units
			Min	Typ	Max	Min	Typ	Max	
$t_{RFCKL,H}$	Minimum Pulse Width of RFCK	Figure 9	100						ns
T	Period of $\overline{RAS}$ Generator Clock	Figure 3	100						ns
t_{RGCKL}	Minimum Pulse Width Low of RGCK	Figure 3	35						ns
t_{RGCKH}	Minimum Pulse Width High of RGCK	Figure 3	35						ns
t_{FRQL}	RFCK Low to Forced $\overline{RFRQ}$ Low	$C_L = 50pF$, Figure 3		20	30				ns
t_{FRQH}	RGCK Low to Forced $\overline{RFRQ}$ High	$C_L = 50pF$, Figure 3		50	75				ns
t_{RGRL}	RGCK Low to $\overline{RAS}$ Low	Figure 3	50	65	95				ns
t_{RGRH}	RGCK Low to $\overline{RAS}$ High	Figure 3	40	60	85				ns
t_{RQHRF}	$\overline{RFSH}$ Hold Time from $\overline{RFSH}$ $\overline{RQST}$ (RF I/O)	Figure 3	2T						ns
t_{RFRH}	$\overline{RFSH}$ High to $\overline{RAS}$ High (ending forced RFSH)	See Mode 1 Descrip.	55	80	110				ns
t_{RFSRG}	$\overline{RFSH}$ Low Set-up to RGCK Low (Mode 1)	See Mode 1 Descrip.	35						ns
t_{CSCT}	$\overline{CS}$ High to RFSH Counter Valid	Figure 9		55	70				ns
t_{CSRL}	$\overline{CS}$ Low to Access $\overline{RASIN}$ Low	See Mode 5 Descrip.	10						ns
t_{ZH}	$\overline{CS}$ Low to Address Output High from Hi-Z	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60				ns
t_{HZ}	$\overline{CS}$ High to Address Output Hi-Z from High	$C_L = 15pF$, Figures 9, 12 R2 = 1k, S1 open		20	40				ns
t_{ZL}	$\overline{CS}$ Low to Address Output Low from Hi-Z	Figures 9, 12 R1 = 3.5k, R2 = 1.5k		35	60				ns
t_{LZ}	$\overline{CS}$ High to Address Output Hi-Z from Low	$C_L = 15pF$, Figures 9, 12 R1 = 1k, S2 open		25	50				ns
t_{HZH}	$\overline{CS}$ Low to Control Output High from Hi-Z High	Figures 9, 12 R2 = 750Ω, S1 open		50	80				ns
t_{HHZ}	$\overline{CS}$ High to Control Output Hi-Z High from High	$C_L = 15pF$, Figures 9, 12 R2 = 750Ω, S1 open		40	75				ns
t_{HZL}	$\overline{CS}$ Low to Control Output Low from Hi-Z High	Figure 12, S1, S2 open		45	75				ns
t_{LHZ}	$\overline{CS}$ High to Control Output Hi-Z High from Low	$C_L = 15pF$, Figure 12, R2 = 750Ω, S1 open		50	80				ns

Input Capacitance $T_A = 25°C$ (Notes 2, 6)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance ADS, R/$\overline{C}$			8		pF
C_{IN}	Input Capacitance All Other Inputs			5		pF

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: This test is provided as a monitor of Driver output source and sink current capability. Caution should be exercised in testing this parameter. In testing these parameters, a 15Ω resistor should be placed in series with each output under test. One output should be tested at a time and test time should not exceed 1 second.

Note 4: Input pulse 0V to 3.0V, $t_R = t_F = 2.5ns$, $f = 2.5MHz$, $t_{PW} = 200ns$. Input reference point on AC measurements is 1.5V. Output reference points are 2.7V for High and 0.8V for Low.

Note 5: The load capacitance on RF I/O should not exceed 50pF.

Note 6: Applies to all DP8409 versions unless otherwise specified.

Note 7: The DP8409-2 device can only be used with memory devices that meet the t_{RAH} specification indicated.

Applications

If external control is preferred, the DP8409 may be used in Mode 0 or 4, as in Figure 6.

If basic auto access and refresh are required, then in cases where the user requires the minimum of external complexity, Modes 1 and 5 are ideal, as shown in Figure 13a. The DP843X2 is used to provide proper arbitration between memory access and refresh. This chip supplies all the necessary control signals to the processor as well as the DP8409. Furthermore, two separate $\overline{CAS}$ outputs are also included for systems using byte-writing. The refresh clock RFCK may be divided down from either RGCK using an IC counter such as the DM74LS393 or better still, the DP84300 Programmable Refresh Timer. The DP84300 can provide RFCK periods ranging from 15.4μs to 15.6μs based on the input clock of 2 to 10 MHz. Figure 13b shows the general timing diagram for interfacing the DP8409 to different microprocessors using the interface controller DP843X2.

If the system is complex, requiring automatic access and refresh, burst refresh, and all-banks auto-write, then more circuitry is required to select the mode. This may be accomplished by utilizing a PAL. The PAL has two functions. One as an address comparator, so that when the desired port address occurs (programmed in the PAL), the comparator gates the data into a latch, where it is connected to the mode pins of the DP8409. Hence the mode of the DP8409 can be changed as desired with one PAL chip merely by addressing the PAL location, and then outputting data to the mode-control pins. In this manner, all the automatic modes may be selected, assigning R/C as RFCK always, and $\overline{CASIN}$ as RGCK always. The output from RF I/O may be used as End-of-Count to an interrupt, or Refresh Request to $\overline{HOLD}$ or $\overline{BUS\ REQUEST}$. A complex system may use Modes 5 and 1 for automatic access and refresh, Modes 3a and 7 for system initialization, and Mode 2 (auto-burst refresh) before and after DMA.

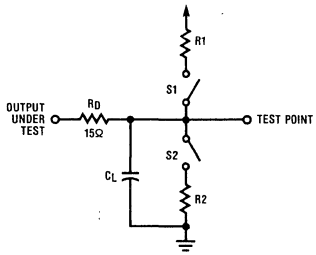


FIGURE 11. Output Load Circuit

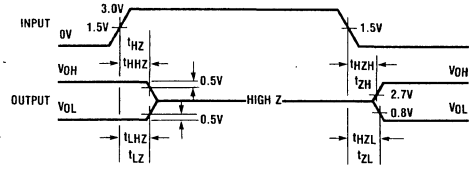


FIGURE 12. Waveform

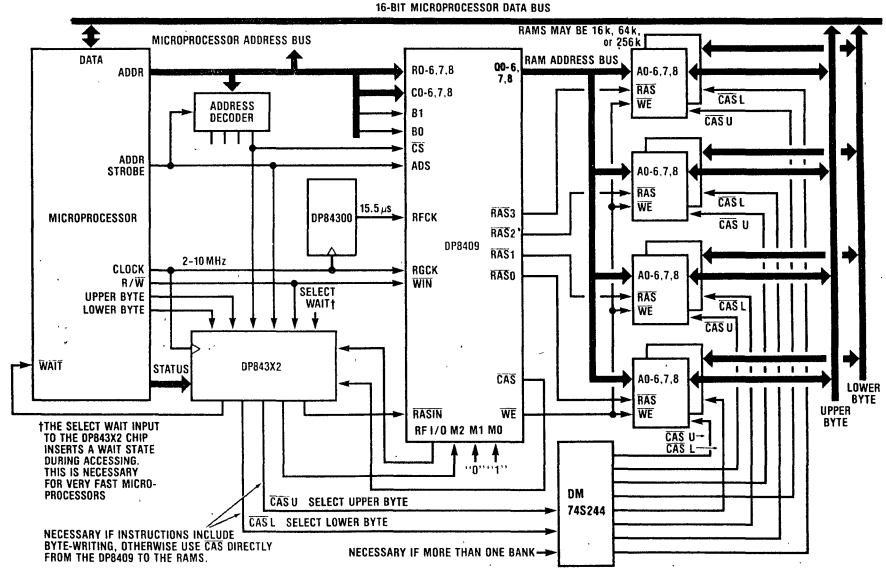


FIGURE 13a. Connecting the DP8409 Between the 16-bit Microprocessor and Memory

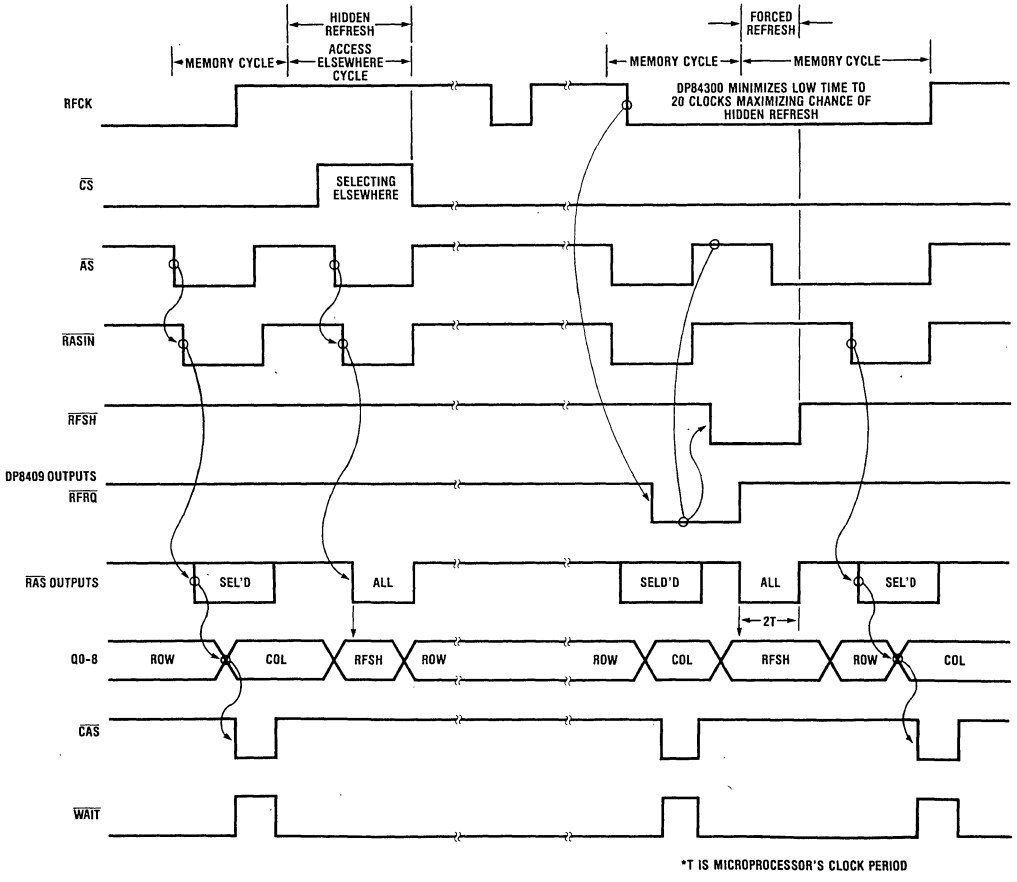


FIGURE 13b. DP8409 Auto Refresh

National Semiconductor

Dynamic Memory Support

PRELIMINARY

DP8419 High Speed Dynamic RAM Controller/Driver

General Description

The DP8419 High Speed DRAM Controller/Driver combines the most popular memory control features of the DP8408/9 DRAM Controller/Driver with the high speed of Bipolar Oxide Isolation processing.

The DP8419 retains the high capacitive-load drive capability of the DP8408/9 as well as its most frequently used access and refresh modes, allowing it to directly replace the DP8408/9 in applications using only modes 0, 1, 4 and 5. Thus, the DP8419 will allow most DP8408/9 users to directly upgrade their system simply by replacing their old controller chip with the DP8419.

Since only two of the three mode pins from the DP8408/9 are necessary to select the four available DP8419 modes, M1 of the DP8408/9 is called RAHS on the DP8419 and allows the user the option of selecting t_{RAH} to suit his DRAMs.

Figure 1 shows the DP8419 pinout. It is identical to that of the DP8408/9, except for pin 4 which has become RAHS.

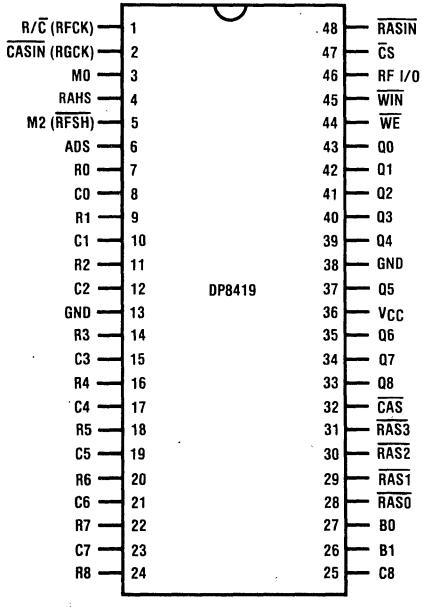
Table 1 is a DP8419 mode table. Pins 3 and 5 are used to select from the four available operational modes. Note that the mode selection scheme is identical to that of the DP8408/9 with M1 (pin 4) tied low.

Features

- Pin and functionally compatible with the DP8408/9 DRAM Controllers in most applications
- Significantly faster memory access and refresh due to Bipolar Oxide Isolation processing
- Choice of t_{RAH} is pin selectable
- Nibble mode accessing available in external control mode

Connection Diagram

Dual-In-Line Package



TOP VIEW

FIGURE 1.

Table 1. DP8419 Mode Select Options

Mode	(RFSH) M2	M0	Mode of Operation
0	0	0	Externally Controlled Refresh
1	0	1	Auto Refresh — Forced
4	1	0	Externally Controlled Access
5	1	1	Auto Access (Hidden Refresh)

DP8408, DP8409 Application Hints

National Semiconductor
Application Brief #1
Tim Garverick
June 1983

The DP8408, DP8409 dynamic RAM controllers have been well received by dynamic memory users because they perform functions formerly requiring multiple integrated circuit chips. These controllers are designed to be suitable for a variety of DRAM control methods. As a result of the many combinations of ways in which inputs to these chips may be varied, it was inevitable that certain conditions exist that would cause the DP8408, DP8409 to respond in an undesirable way. Feedback from customers using these chips has resulted in thorough investigations of such conditions. The following are constraints on the use of the DRAM controllers which are not addressed in their data sheets. The majority of customers will find that most of the items on this list are not pertinent to their particular application, and those that are impose minimal restrictions.

1) The on-chip refresh counter resets when the RFI/O pin goes low for a refresh request in mode 5 if this pin is excessively loaded with capacitance. The data sheet suggests that this pin not be loaded with greater than 50 pF. Since RFI/O, in most cases, needs only to drive a low capacitance in a refresh control circuit, this limit is not unreasonable.

2) When the DP8408, DP8409 is in a refresh mode, the RFI/O pin indicates that the on-chip refresh counter has reached its end-of-count. This end-of-count is selectable as 127, 255 or 511 (511 is available only on the DP8409) to accommodate 16k, 64k or 256k DRAMs, respectively. Although the end-of-count may be chosen to be any of these, the counter always counts to 511 (255 for the DP8408) before rolling over to zero.

3) In mode 5, the DP8409 requests a refresh when RFI/O goes low following RFCK (R/$\overline{C}$). DP8409s with date code 8209 or earlier, have a slight functional difference from later DP8409s. With $\overline{CS} = 1$, RFI/O goes low for only about 10 ns when RFCK goes low, for early DP8409s. It stays high until mode 1 is entered and then responds as specified in the data sheet. DP8409s with date codes after 8209 function as shown in the data sheet with $\overline{CS} = 1$. If $\overline{CS} = 0$ all DP8409s operate as specified in the data sheet.

4) When going from mode 0, 1 or 2 (refresh) to mode 5 of the DP8408, if $\overline{CASIN}$ and R/$\overline{C}$ are both low, a glitch occurs on the $\overline{CAS}$ output. Since neither of these inputs is used in these modes, one or both should be held high.

5) Most DRAMs specify 0 ns row address set-up time to $\overline{RAS}$. In order to guarantee this, the row address to the DP8408, DP8409 must be valid 10 ns before $\overline{RASIN}$ transitions low to initiate an access. In terms of the data sheet parameters, maximum (t_{APD}-t_{RPDL}) = 10 ns.

6) When changing modes from refresh to access, again sufficient time must be allowed for the row address to be valid before $\overline{RAS}$ occurs. In this case, the address outputs of the DP8408, DP8409 are changing from the refresh counter to the row address inputs. In order for the row address to be set up a minimum of 0 ns before $\overline{RAS}$ goes low, $\overline{RASIN}$ should not go low until 30 ns after the change from refresh to access mode.

7) Both the low and high pulse widths of $\overline{RAS}$ have minimum requirements during refresh. When in mode 0, the $\overline{RASIN}$ to $\overline{RAS}$ low delay is longer than the $\overline{RASIN}$ to $\overline{RAS}$ high delay. In terms of the data sheet parameters, maximum ($t_{RFPDL} - t_{RFPDH}$) = 25 ns. Thus, the minimum low pulse width of $\overline{RAS}$ in mode 0 equals the $\overline{RASIN}$ low pulse width minus 25 ns. The minimum high pulse width of $\overline{RAS}$ in mode 0 equals the $\overline{RASIN}$ high pulse width.

8) The fastest memory access may be accomplished using mode 4 and external delay lines (see App. Brief #9).

9) In the data sheet, it is specified that $\overline{CS}$ should go low 15 ns (t_{CSLR}) before $\overline{RASIN}$ goes low to initiate an access in mode 5. This is to prevent the possibility of a glitch on the $\overline{RAS}$ outputs, resulting from the DP8409 interpreting the $\overline{RASIN}$ as a hidden refresh. For the same reason, $\overline{CS}$ should be held low for a minimum of 15 ns after $\overline{RASIN}$ returns high, ending the access in mode 5.

10) If the DP8409 is being used in mode 5 and $\overline{CS} = 1$, and if $\overline{RASIN}$ goes low within 15 ns before RFCK (R/$\overline{C}$) goes low, up to a 15 ns glitch may occur on the refresh request pin, RFI/O. However, since $\overline{CS}$ is high, a hidden refresh will occur as it normally would with RFCK high. If the glitch on RFI/O were detected and interpreted as a forced refresh request, no forced refresh would be allowed by the DP8409 since a hidden refresh was allowed. This would not cause any problem, however, since the hidden refresh has taken care of the refresh requirement for that period of RFCK. Also, this forced refresh request could not be detected if the system does not check RFI/O for a low state while $\overline{RASIN}$ is low (i.e., an access is taking place).

DP8408/9
Fastest DRAM Access Mode

National Semiconductor
Application Brief # 9
Tim Garverick
Rusty Meier
February 1983

If one desires the fastest possible operation of the DP8408/9 multi-mode dynamic RAM controller/driver in accessing DRAMs, mode 4, externally controlled access mode should be considered.

In using mode 4 there are three input signals which must be considered:

1) $\overline{RASIN}$ — generates $\overline{RAS}$
2) R/$\overline{C}$ — switches between rows and columns on the address outputs
3) $\overline{CASIN}$ — generates $\overline{CAS}$

In producing these signals a delay will be needed between $\overline{RASIN}$ and R/$\overline{C}$ and between R/$\overline{C}$ and $\overline{CASIN}$. (**Note:** In mode 4 external generation of $\overline{CASIN}$ can produce $\overline{CAS}$ faster than automatic generation of $\overline{CAS}$.)

Two important parameters have been added to the DP8408/9 data sheets that help one compute the minimum acceptable delays between the above-mentioned signals. These parameters are:

1) t_{DIF1} = MAXIMUM ($t_{RPDL} - t_{RHA}$) = 13 ns
   where t_{RPDL} = $\overline{RASIN}$ to $\overline{RAS}$ delay
   t_{RHA} = row address held from column select
2) t_{DIF2} = MAXIMUM ($t_{RCC} - t_{CPDL}$) = 13 ns
   where t_{RCC} = column select to column address valid
   t_{CPDL} = $\overline{CASIN}$ to $\overline{CAS}$ delay

These parameters are specified as being less than what would be calculated using the min/max values given for t_{RCC}, t_{CPDL}, t_{RPDL} and t_{RHA} in the DP8408/9 specification sheets, because on-chip delays track over temperature and supply variations.

The equation for the delay between $\overline{RASIN}$ and R/$\overline{C}$ that guarantees the specified DRAM t_{RAH} is:

$$\text{min delay required} = t_{DIF1} + t_{RAH} = 13\text{ ns} + t_{RAH}$$

where t_{RAH} = DRAM minimum row address hold time from $\overline{RAS}$

The equation for the delay between R/$\overline{C}$ and $\overline{CASIN}$ that guarantees the specified DRAM t_{ASC} is:

$$\text{min delay required} = t_{DIF2} + t_{ASC} = 13\text{ ns} + t_{ASC}$$

where t_{ASC} = DRAM minimum column address set-up time to $\overline{CAS}$

To produce the above-mentioned delays between signals, a ±2 ns resolution delay line can be used as follows:

(assuming t_{RAH} = 20 ns, t_{ASC} = 0 ns)
$\overline{RASIN}$ to R/$\overline{C}$ delay = 13 ns + 20 ns = 33 ns
R/$\overline{C}$ to $\overline{CASIN}$ delay = 13 ns + 0 ns = 13 ns

Thus, R/$\overline{C}$ must follow $\overline{RASIN}$ by a minimum of 33 ns and $\overline{CASIN}$ must follow R/$\overline{C}$ by a minimum of 13 ns. With a delay line of ± 2 ns resolution, the $\overline{RASIN}$ to R/$\overline{C}$ and R/$\overline{C}$ to $\overline{CASIN}$ delays can be typicals of 35 ns and 15 ns, respectively. (See *Figures 1* and *2* below.)

This scheme will provide a maximum $\overline{RASIN}$ to $\overline{CAS}$ delay of:

35 ns + 15 ns + 2 ns (resolution uncertainty) + MAXIMUM (t_{CPDL}) = 52 ns + MAXIMUM (t_{CPDL})

For the DP8408/9-2, MAXIMUM (t_{CPDL}) = 58 ns.

For the DP8408/9 (no dash), MAXIMUM (t_{CPDL}) = 68 ns (not 58 ns as indicated in data sheets up to November 1982).

The fastest mode 4 accesses (with the assumed delay line and DRAM parameters) are therefore, 110 ns and 120 ns, respectively, for the -2 and non-dash parts.

The maximum $\overline{RASIN}$ to $\overline{CAS}$ delay (t_{RICL}) in mode 5 (auto mode) for the DP8408/9-2 (which guarantees a min t_{RAH} of 20 ns) is 130 ns. The maximum t_{RICL} in mode 5 for the DP8408/9 (no dash) is 160 ns.

Thus, it is shown that if the features offered by the DP8408/9 automatic modes can be sacrificed, mode 4 (externally controlled access) may be used to obtain the fastest memory access.

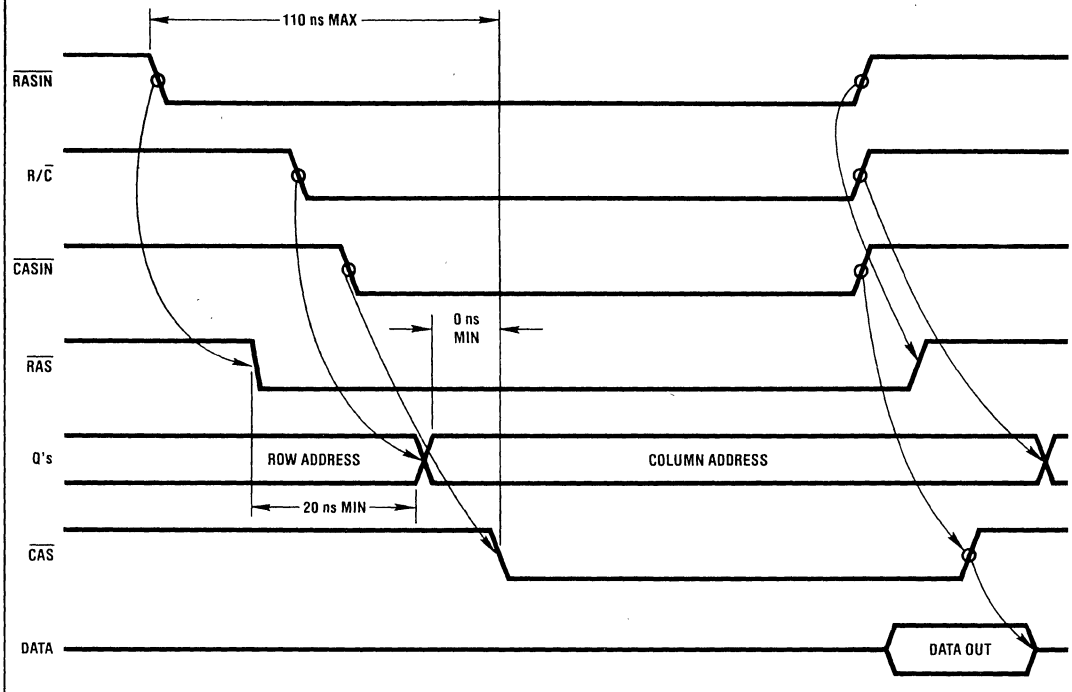


Figure 1. Mode 4 Timing Relationships

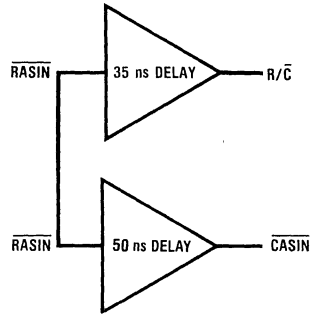


Figure 2. Mode 4 Externally Generated Signals

Precautions to Take When Driving Memories

National Semiconductor
Application Note AN-305
June 1982
Mike Evans

As memory prices continue their relentless reduction of cost per bit, more and more systems designers are incorporating memories into their designs. In general these memories comprise a number of dynamic RAMs, such as the 64k × 1. In this × 1 configuration, the number of RAMs required is a multiple of the bus width. Most new system designs use 16-bit microprocessors, so that a typical memory will comprise from 16 to 64 DRAMs, thus providing from 64k to 256k addressing capability. This means the memory drivers have to drive upwards of 16 RAMs. The drivers may be part of an integrated circuit dynamic RAM controller such as the DP8408/DP8409, or they may be on a separate chip such as the DP84240/DP84244 octal memory drivers. The recommendations in this article are valid for any type of memory driver. The purpose of the article is to forewarn new designers using memories of problems they will encounter if adequate precautions are not taken.

A typical configuraton of a 16-bit wide memory is shown in *Figure 1*. Each driver address output goes to every dynamic RAM, as does $\overline{WE}$. $\overline{CAS}$ outputs go to half the number of RAMs assuming byte writing is required. $\overline{RAS}$ outputs each go only to one bank. Note that these loads are not true for the data inputs and outputs. Each data I/O only connects to its respective bit, so the loading is only one RAM per bank for data. In general, this is why buffers are not required on the data bus when interfacing to memory. Data In of the RAMs can be linked directly to Data Out for any one bit, and also to the corresponding bit on the data bus. This is true for normal read and write operations, but if read-modify-write cycles are employed, the Data Out signals must be buffered from the data bus.

Using this typical memory configuration may not be as simple as it seems. Without care and attention, problems can arise for the unprepared, and there are two areas in particular which may cause memory errors or memory damage: one is voltage overshoot caused by inductive traces and high capacitive loads, the other is switching spikes caused by switching high capacitive loads.

Overshoot and Undershoot
(Undershoot is Negative Overshoot)

When a system requires a number of dynamic RAMs, the result is high capacitance loads, caused by a combination of RAM input capacitance and trace capacitance. Each dynamic RAM has a specified input capacitance of 10pF maximum, but most dynamic RAMs are closer to 2 to 3pF. Very few actually get close to 10pF, even under worst case conditions of high temperature and V_{CC}. It is safe, therefore, to assume a much lower average input capacitance when using 16 or more RAMs. In fact, the input capacitance of most inputs is due more to the package than the input gating, because the silicon gate inputs of the transistors in today's market have such high impedance. A typical maximum would be 2.5pF. Control inputs such as $\overline{RAS}$ and $\overline{CAS}$ connect to more than one transistor input. For example, on the National Semiconductor 64k × 1 dynamic RAM, the NMC4164, $\overline{RAS}$ goes to two transistors and $\overline{CAS}$ to four. In general, this is true for most manufacturers' RAMs, so a more typical maximum input capacitance would be 3pF for $\overline{RAS}$ and 3.5pF for $\overline{CAS}$. RAM input currents are so small as to be negligible. The input current is quoted as 10μA maximum, but again most RAMs are much less than this in a typical memory. Driving DRAMs, therefore, is not a problem of DC drive capability, but rather a problem of capacitance drive capability.

Driving DRAM input capacitance is further compounded by printed circuit traces, and even more so by wire-wrapping. Both can be represented by a transmission line with distributed capacitance and inductance. Thus, the total load is equivalent to a complex impedance comprising the distributed trace inductance, and a capacitance comprising distributed trace capacitance and RAM input capacitance as shown in *Figure 2a*.

The effect is an overshoot or undershoot at the dynamic RAM inputs that occurs each time a memory driver changes state, as shown in *Figure 2b*. As the driver output changes state, the load capacitance cannot be instantaneously charged or discharged because the current available is limited both by the driver transistor impedance, and the equivalent series resistance from the supply rail through the chip to the trace resistance. This current will be similar in value to the quoted short circuit current of the driver stage; therefore, there is a spike of current that lasts as long as it takes to change the voltage of all the capacitances. For the driver stages of the DP8408/DP8409, or the DP84240/DP84244, the typical short circuit current is 100mA per stage. This is true for either direction, so that the high-to-low transition takes roughly the same time as the low-to-high transition, minimizing skew times on all the driver outputs, as they transition in either direction. Assuming the output low voltage, V_{OL}, is 0.2V and the output high voltage, V_{OH}, is 3.2V, and that the charge/discharge current is constant at I_{SC}, then the current spike will exist for a time, T,

where,

$$T = C_L \times (V_{OH} - V_{OL})/I_{SC}$$
$$= 500\,pF \times 3.0\,V/100\,mA = 15\,ns$$

C_L (500pF) is the load capacitance of typically 64 to 88 dynamic RAMs, in other words, four banks comprising 16 data bits and possibly six check bits if error correction is required.

In fact, due to the trace inductance, the rate of change of current will not be a step function, so that the current waveform looks like a spike. Even so, the rapid rate of change of current, di/dt, into the trace inductance L, will create a potentially excessive voltage "e" across this inductance. As an example, if the current changes from 0 to 100mA in 6ns, and the composite trace inductance is 0.3μH, then the voltage across this inductance is "e," where,

$$e = L\ di/dt$$
$$= 0.3\mu H \times 100mA/6ns = 5V$$

In other words, at this rate of change in current, even a small inductance can be dangerous for two reasons. First, the dynamic RAMs at the far end of the trace could be destroyed, unless they have clamping diodes to V_{CC} and GND (most do not), or second, the returning voltage may exceed the threshold it has just passed causing a second and then third change of state. If this sudden glitch occurs on a control signal input such as $\overline{RAS}$, the memory contents may be inadvertently changed.

It is therefore necessary to remove the spike. The most common approach is to insert a damping resistor in the path between the driver and the RAMs, fairly close to the driver, as shown by R_D in *Figure 2a*. The best value for the resistor is the critical value giving a critically damped transition. Too high a value will cause overdamping which results in a slow transition. This slow edge may create excessive skew problems and slow down the memory cycle, or even worse, the edge may be slow enough that the RAM cycle never begins internally. If the damping resistor value is too low, the undershoot or overshoot may not be removed. It is therefore recommended that the resistor be determined on the first prototypes (not wire-wrapped prototypes because the value will be different due to the larger distributed inductance and capacitance). Also, the values may be different for the control lines, particularly $\overline{CAS}$. If there are a number of banks, and a $\overline{RAS}$ is used to select each bank, then the damping resistor in this line will be higher.

Typical values for the damping resistors will be between 15Ω and 100Ω, the lower the loading, the higher the values. Some IC manufacturers offer octal memory drivers with on-chip series resistors fixed at ≈25Ω. Unless this is the critical value required for all the lines, problems will arise. The DP8400 family has been designed with equivalent internal values of approximately 10Ω, allowing for any external value of damping resistor.

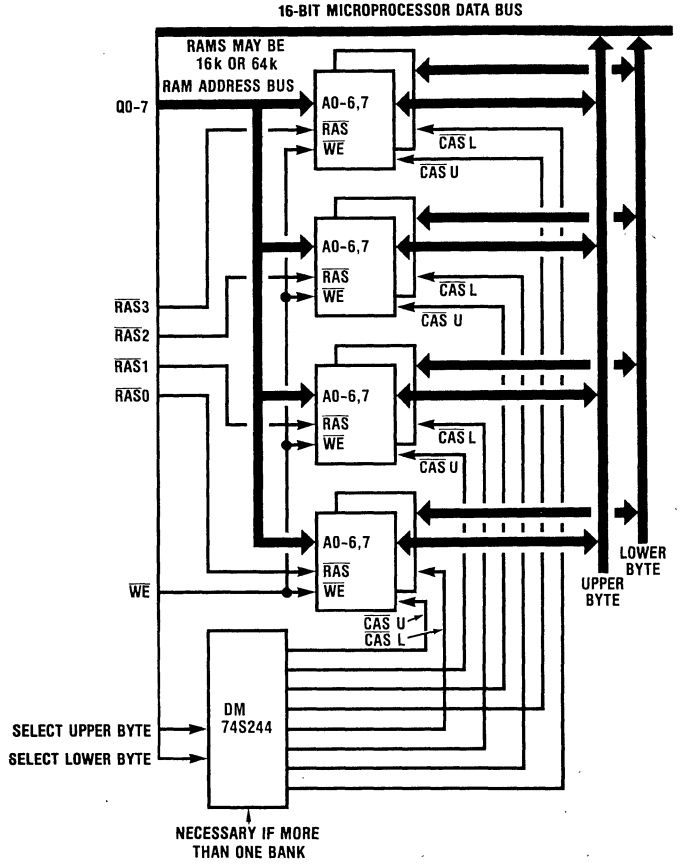


Figure 1. Typical 16-Bit Memory with Byte Write Address

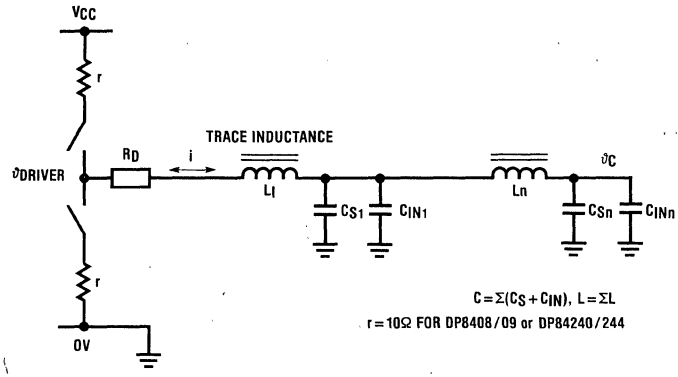


Figure 2a. Complex Load Impedance Caused by Distributed Trace Inductance L and Capacitance C_S, and RAM Input Capacitance C_{IN}

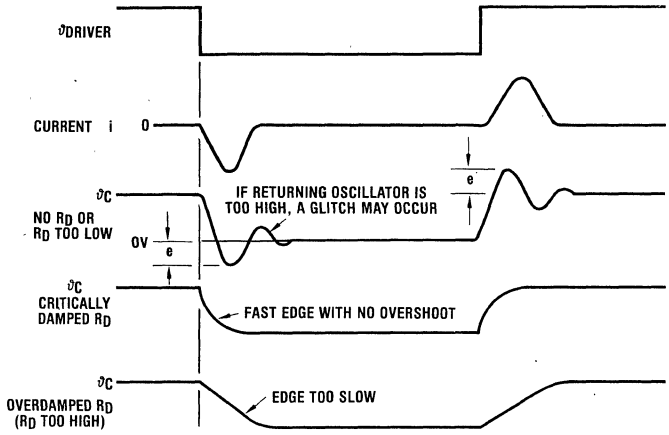


Figure 2b. Timing Waveforms Showing the Effect of Variations of R_D on Signals Appearing at the RAM

Switching Current Spikes

Another major undesirable effect of the fast current spikes is the effect on the V_{CC} and GND pins. The worst case is when all eight or nine address outputs switch in the same direction at the same time, as shown in *Figure 3a*. If each driver can source or sink 100mA, then a current of approximately 1A could enter or exit the driver chip in a period of 20ns. The resistance and inductance of the V_{CC} and GND lines to the chip can cause excessive drops during this switching time (see waveforms in *Figure 3a*), which may, in turn, upset latches either in the DP8408/DP8409, or externally. A ceramic capacitor connected across V_{CC} and GND pins will largely remove the spike. A 1μF multilayer ceramic is recommended. This should be fitted as close as possible to the pins in order to reduce lead inductance. The DP8408/DP8409 pin configuration facilitates this with GND and V_{CC} pins 0.2" apart so that the ceramic capacitor can be fitted as close to the chip as possible. The second GND pin should also be decoupled. These GND and V_{CC} pins are located in the center of the package to reduce bonding lead lengths. In fact, the lead resistance is five times lower than if the supply pins were in the corners. An example of how this spike can be reduced would be the previous example of a 1A change in supply current switching in 20ns with a 1μF ceramic capacitor decoupling GND and V_{CC}. The voltage drop "v" is 1A $\times$ 20ns/1μF, or 20mV.

If the decoupling capacitor was 0.01 μF, the drop would be 2V. Tantalum or other types of capacitors are lower frequency capacitors and have only a small effect in reducing the voltage spike. Ceramic capacitors are high frequency, and multilayer capacitors with lower inductance have a greater effect in reducing the voltage spike and are therefore recommended. As a further recommendation, the dynamic RAMs should be similarly decoupled with approximately a 0.1 μF ceramic capacitor on each RAM. Wire-wrapped boards, in particular, need special attention.

There are some other precautions that may be considered when driving memories. First, be aware that IC sockets increase load capacitance and inductance, so it becomes a matter of the importance of removability of chips, and maintainability. Also, shorter, thicker trace lengths will reduce the load, and good GND and V_{CC} connections will help reduce the voltage spikes around the memory board. For wire-wrapped designs, GND and V_{CC} should be multiwired.

With proper decoupling and correct selection of damping resistors, integrated circuit dynamic RAM controllers will function as expected to ease the burden of the system designer.

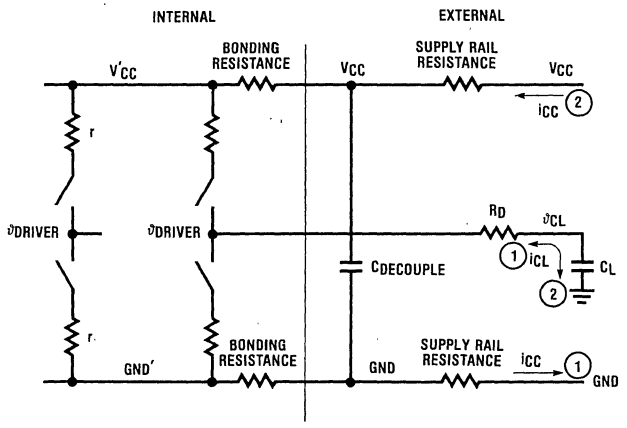


Figure 3a. Effect of Switching All Outputs Simultaneously in the Same Direction

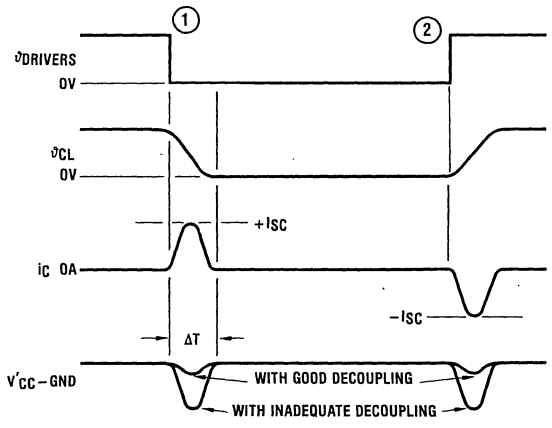


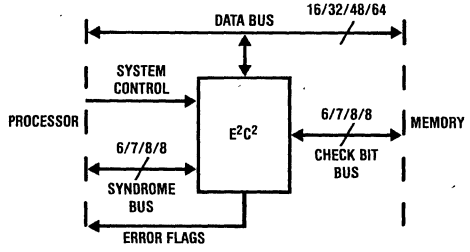
Figure 3b. Timing Waveforms Showing Internal Supply Rail Drops During Output Switching

National Semiconductor

DP8400 — E^2C^2 Expandable Error Checker and Corrector

General Description

The DP8400 Expandable Error Checker and Corrector (E^2C^2) aids system reliability and integrity by detecting errors in memory data and correcting single or double-bit errors. The E^2C^2 data I/O port sits across the processor-memory data bus as shown, and the check bit I/O port connects to the memory check bits. Error flags are provided, and a syndrome I/O port is available. Fabricated using high speed Schottky technology in a 48-pin dual-in-line package, the DP8400 has been designed such that its internal delay times are minimal, maintaining maximum memory performance.



For a 16-bit word, the DP8400 monitors data between the processor and memory, with its 16-bit bidirectional data bus connected to the memory data bus. The DP8400 uses an encoding matrix to generate 6 check bits from the 16 bits of data. In a WRITE cycle, the data word and the corresponding check bits are written into memory. When the same location of memory is subsequently read, the E^2C^2 generates 6 new check bits from the memory data and compares them with the 6 check bits read from memory to create 6 syndrome bits. If there is a difference (causing some syndrome bits to go high), then that memory location contains an error and the DP8400 indicates the type of error with 3 error flags. If the error is a single-bit error, the DP8400 will automatically correct it.

The DP8400 is easily expandable to other data configurations. For a 32-bit data bus with 7 check bits, two DP8400s can be used in cascade with no other ICs. Three DP8400s can be used for 48 bits, and four DP8400s for 64 data bits, both with 8 check bits. In all these configurations, single and double-error detection and single-error correction are easy to implement.

When the memory is more unreliable, or better system integrity is preferred, then in any of these configurations, double-error correction can be performed. One approach requires a further memory WRITE-READ cycle using complemented data and check bits from the DP8400. If at least one of the two errors is a hard error, the DP8400 will correct both errors. This implementation requires no more memory check bits or DP8400s than the single-error correct configurations.

The DP8400 has a separate syndrome I/O bus which can be used for error logging or error management. In addition, the DP8400 can be used in BYTE-WRITE applications (for up to 72 data bits) because it has separate byte controls for the data buffers. In 16 or 32-bit systems, the DP8400 will generate and check system byte parity, if required, for integrity of the data supplied from or to the processor. There are three latch controls to enable latching of data in various modes and configurations.

Operational Features

- Fast single and double-error detection
- Fast single-error correction
- Double-error correction after catastrophic failure with no additional ICs or check bits
- Functionally expandable to 100% double-error correct capability
- Functionally expandable to triple-error detect
- Directly expandable to 32 bits using 2 DP8400s only
- Directly expandable to 48 bits using 3 DP8400s only
- Directly expandable to 64 bits using 4 DP8400s only
- Expandable to and beyond 64 bits in fast configuration with extra ICs
- 3 error flags for complete error recording
- 3 latch enable inputs for versatile control
- Byte parity generating and checking
- Separate byte controls for outputting data in BYTE-WRITE operation
- Separate syndrome I/O port accessible for error logging and management
- On-chip input and output latches for data bus, check bit bus and syndrome bus
- Diagnostic capability for simulating check bits
- Memory check bit bus, syndrome bus, error flags and internally generated syndromes available on the data bus
- Self-test of E^2C^2 on the memory card under processor control
- Full diagnostic check of memory with the E^2C^2
- Complete memory failure detectable
- Power-on clears data and syndrome input latches

Timing Features

16-BIT CONFIGURATION

WRITE Time: 35 ns from data-in to check bits valid
DETECT Time: 35 ns from data-in to Any Error (AE) flag set
CORRECT Time: 70 ns from data-in to correct data out

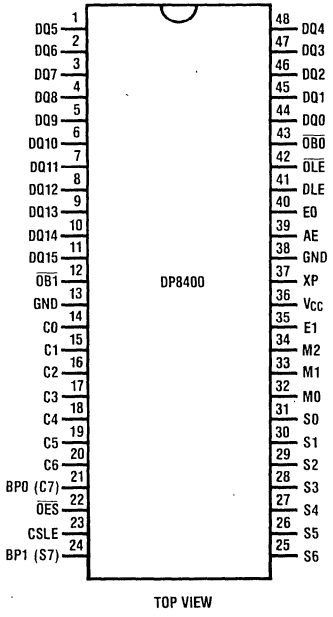
Timing Features (Continued)

32-BIT CONFIGURATION

WRITE Time: 65 ns from data-in to check bits valid
DETECT Time: 60 ns from data-in to Any Error (AE) flag set
CORRECT Time: 125 ns from data-in to correct data out

DP8400 Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DP8400N-4 or DP8400D-4
See NS Package N48A or D48A

Pin Definitions See *Figure 1* for abbreviations

V_{CC}, GND, GND: 5.0V ± 5%. The 3 supply pins have been assigned to the center of the package to reduce voltage drops, both DC and AC. Also there are two ground pins to reduce the low-level noise. The second ground pin is located two pins from V_{CC}, so that decoupling capacitors can be inserted directly next to these pins. It is important to adequately decouple this device, due to the high switching currents that will occur when all 16 data bits change in the same direction simultaneously. A recommended solution would be a 1 μF multilayer ceramic capacitor in parallel with a low-voltage tantalum capacitor, both connected close to pins 36 and 38 to reduce lead inductance.

DQ0-DQ15: Data I/O port. 16-bit bidirectional data bus which is connected to the input of DIL0 and DIL1 and the output of DOB0 and DOB1, with DQ8-DQ15 also to CIL.

C0-C6: Check-bit I/O port. 7-bit bidirectional bus which is connected to the input of the CIL and the output of the COB. COB is enabled whenever M2 is low.

S0-S6: Syndrome I/O port. 7-bit bidirectional bus which is connected to the input of the SIL and the output of the SOB.

DLE: Input data latch enable. When high, DIL0 and DIL1 outputs follow the input data bus. When low, DIL0 and DIL1 latch the input data.

CSLE: Input check bit and syndrome latch enable. When high, CIL and SIL follow the input check and syndrome bits. When low, CIL and SIL latch the input check and syndrome bits. If $\overline{OES}$ is low, SIL remains latched.

$\overline{OLE}$: Output latch enable. $\overline{OLE}$ enables the internally generated data to DOL0, and DOL1, COL and SOL when low, and latches when high.

XP: Multi-expansion, which feeds into a three-level comparator. With XP at 0V, only 6 or 7 check bits are available for expansion up to 40 bits, allowing byte parity capability. With XP open or at V_{CC}, expansion beyond 40 bits is possible, but byte parity capability is no longer available. When XP is at V_{CC}, CG6 and CG7, the internally generated upper two check bits, are set low. When XP is open, CG6 and CG7 are set to word parity.

BP0 (C7): When XP is at 0V, this pin is byte-0 parity I/O. In the Normal WRITE mode, BP0 receives system byte-0 parity, and in the Normal READ mode outputs system byte-0 parity. When XP is open or at V_{CC}, this pin becomes C7 I/O, the eighth check bit for the memory check bits, for 48-bit expansion and beyond.

BP1 (S7): When XP is at 0V, this pin is byte-1 parity I/O. In the Normal WRITE mode, BP1 receives system byte-1 parity, and in the Normal READ mode outputs system byte-1 parity. When XP is open or at V_{CC}, this pin becomes S7 I/O, the eighth syndrome bit for 48-bit expansion and beyond.

AE: Any error. In the Normal READ mode, when low, AE indicates no error and when high, indicates that an error has occurred. In any WRITE mode, AE is permanently low.

E0: In the Normal READ mode, E0 is high for a single-data error, and low for other conditions. In the Normal WRITE mode, E0 becomes $\overline{PE0}$ and is low if a parity error exists in byte-0 as transmitted from the processor.

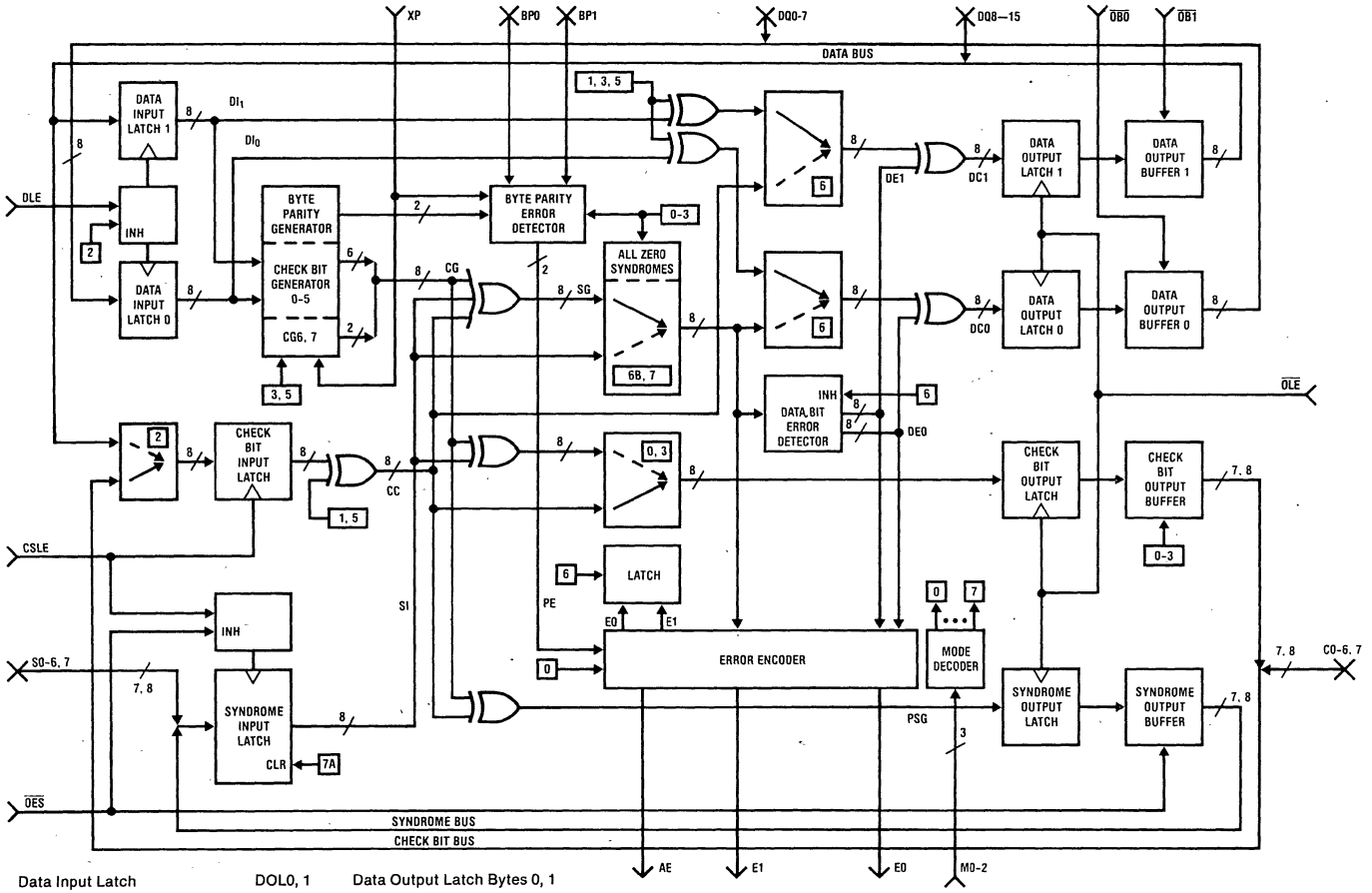
E1: In the Normal READ mode, E1 is high for a single-data error or a single check bit error, and low for no error and double-error. In the Normal WRITE mode, E1 becomes $\overline{PE1}$ and is low if a parity error exists in byte-1 as transmitted from the processor.

$\overline{OB0}$, $\overline{OB1}$: Output byte-0 and output byte-1 enables. These inputs, when low, enable DOL0 and DOL1 through DOB0 and DOB1 onto the data bus pins DQ0-DQ7 and DQ8-DQ15. When $\overline{OB0}$ and $\overline{OB1}$ are high the DOB0, DOB1 outputs are TRI-STATE®.

$\overline{OES}$: Output enable syndromes. I/O control of the syndrome latches. When high, SOB is TRI-STATED and external syndromes pass through the syndrome input latch with CSLE high. When $\overline{OES}$ is low, SOB is enabled and the generated syndromes appear on the syndrome bus, also CSLE is inhibited internally to SIL.

M0, M1, M2: Mode control inputs. These three controls define the eight major operational modes of the DP8400. Table III depicts the modes.

TRI-STATE® is a registered trademark of National Semiconductor Corp.



DIL	Data Input Latch	DOL0, 1	Data Output Latch Bytes 0, 1
CG	Check Bit Generator	COL	Check Bit Output Latch
CIL	Check Bit Input Latch	SOL	Syndrome Output Latch
CC	Check Bit Complementor	DOB0, 1	Data Output Buffer Bytes 0, 1
SIL	Syndrome Input Latch	COB	Check Bit Output Buffer
PSG	Partial Syndrome Generator	SOB	Syndrome Output Buffer
SG	Syndrome Generator	EE	Error Encoder
DED	Data Error Detector	DC0, 1	Data Corrector Bytes 0, 1
DE0, 1	Data Error Bytes 0, 1		
PE	Parity Error		

[n] mode of operation signifies active signal

FIGURE 1. DP8400 Block Diagram

SYSTEM WRITE *(Figure 2a)*

The Normal WRITE mode is mode 0 of Table III. Referring to the block diagram in *Figure 9a* and the timing diagram of *Figure 9b*, the 16 bits of data from the processor are enabled into the data input latches, DIL0 and DIL1, when the input data latch enable (DLE) is high. When this goes low, the input data is latched. The check bit generator (CG) then produces 6 parity bits, called check bits. Each parity bit monitors different combinations of the input data-bits. In the 16-bit configuration, assuming no syndrome bits are being fed in from the syndrome bus into the syndrome input latch, the 6 check bits enter the check bit output latch (COL), when the output latch enable $\overline{OLE}$ is low, and are latched in when $\overline{OLE}$ goes high. Whenever M2 (READ/$\overline{WRITE}$) is low, the check bit output buffer COB always enables the COL contents onto the external check bit bus. Also the data error decoder (DED) is inhibited during $\overline{WRITE}$ so no correction can take place. Data output latches DOL0 and DOL1, when enabled with $\overline{OLE}$, will therefore see the contents of DIL0 and DIL1. If valid system data is still on the data bus, a memory WRITE will write to memory the data on the data bus and the check bits output from COB. If the system has vacated the data bus, output enables ($\overline{OB0}$ and $\overline{OB1}$) must be set low so that the original data word with its 6 check bits can be written to memory.

SYSTEM READ

There are two methods of reading data: the error monitoring method *(Figure 2b)*, and the always correct method *(Figure 2c)*. Both require fast error detection, and the second, fast correction. With the first method, the memory data is only monitored by the E^2C^2, and is assumed to be correct. If there is an error, the Any Error flag (AE) goes high, requiring further action from the system to correct the data. With the always correct method, the memory data is assumed to be possibly in error. Memory data is removed and the corrected, or already correct, data is output from the E^2C^2 by enabling $\overline{OB1}$ and $\overline{OB0}$. To detect an error (referring to *Figures 10a and 10b*) first DLE and CSLE

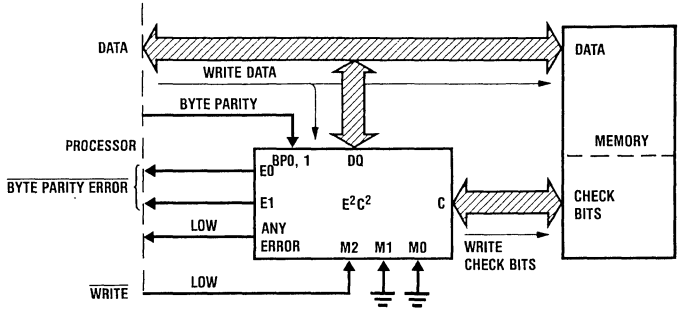


FIGURE 2a. Normal WRITE Mode with E^2C^2

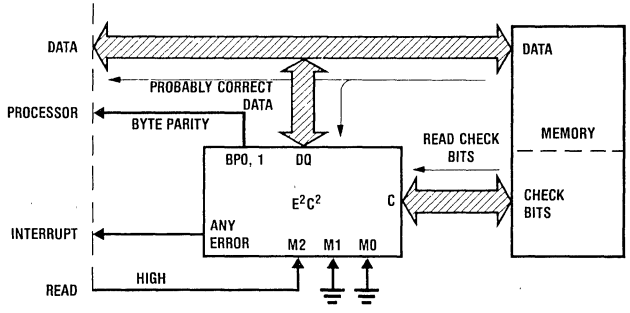


FIGURE 2b. Normal READ Mode, Error Monitoring Method with E^2C^2

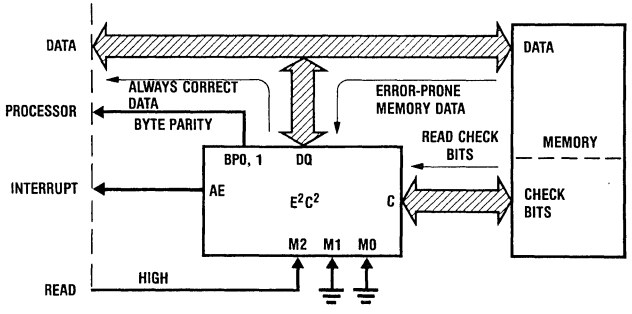


FIGURE 2c. Normal READ Mode, Always Correct Method with E^2C^2

go high to enter data bits and check bits from memory into DIL0, DOL1 and CIL. The 6 check bits generated in CG from DIL0 and DOL1 are then compared with CIL to generate syndromes on the internal syndrome bus (SG). Any bit or bits of SG that go high indicate an error to the error encoder (EE).

If data correction is required $\overline{OB0}$ and $\overline{OB1}$ must be set low (after memory data has been disabled) to enable data output buffers DOB0 and DOB1. The location of any data bit error is determined by the data error decoder (DED), from the syndrome bits. The bit in error is complemented in the DOL for correction. The other 15 bits from DED pass the DIL contents directly to the DOL, so that DOL now contains corrected data.

ERROR DETERMINATION

The three error flags, for a 16-bit example, are decoded from the internally generated syndromes as shown in *Figure 3.* First, if any error has occurred, the generated check bits will be different from the memory check bits, causing some of the syndrome bits to go high. By OR-ing the syndrome bits, the output will be an indication of any error.

If there is a single-data error, then (from the matrix in Table IV) it can be seen that any data error causes either 3 or 5 syndrome bits to go high. 16 AND gates decode which bit is in error and the bit in error is XOR-ed with the corresponding bit of the DIL to correct it, whereas the other 15 decoder outputs are low, causing the corresponding 15 bits in DIL to transfer to DOL directly. DOL now contains corrected data. The 16 AND gate outputs are OR-ed together causing E0 to go high, so that E0 is the single-data-error indication. If the error is a double-error, then either 2,

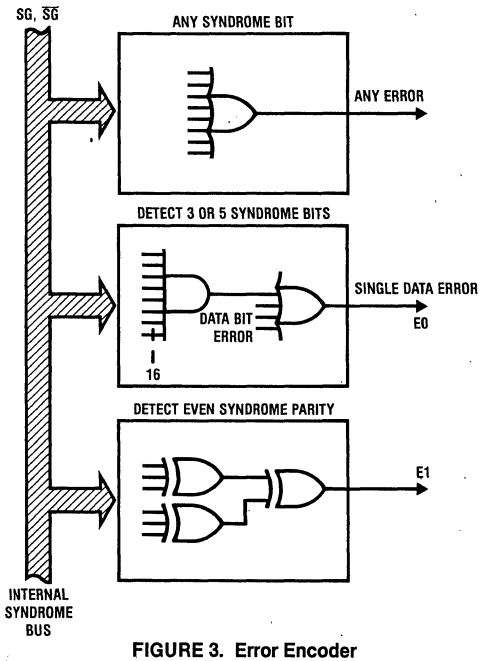


FIGURE 3. Error Encoder

4 or 6 of the syndrome bits will be high. The syndromes for two errors (including one or two check bit errors) are the two sets of syndromes for each individual error bit, XOR-ed together. By performing a parity check on the syndrome bits, flag E1 will indicate $\overline{even}$/odd parity. If there is still an error, but it is not one of these errors, then it is a detectable triple-bit error. Some triple-bit errors are not detectable as such and may be interpreted as single-bit errors and falsely corrected as single-data errors. This is true for all standard ECC circuits using a Modified Hamming-code matrix. The DP8400 is capable, with its Rotational Syndrome Word Generator matrix, of determining all triple-bit errors using twice as many DP8400s and twice as many check bits.

ERROR FLAGS

Three error flags are provided to allow full error determination. Table I shows the error flag outputs for the different error types in Normal READ mode. If there is an error, then ANY ERROR will go high, at a time t_{DEV} *(Figure 10b)* after data and check bits are presented to the DP8400. The other two error flags E0 and E1 become valid t_{DE0} and t_{DE1} later.

The error flags differentiate between no error single check bit error, single data-bit error, double-bit error. Because the DP8400 can correct double errors, it is important to know that two errors have occurred, and not just a multiple-error indication. The error flags will remain valid as long as DLE and CSLE are low, or if DLE is high, and data and check bits remain valid.

BYTE PARITY SUPPORT

Some systems require extra integrity for transmission of data between the different cards. To achieve this, individual byte parity bits are transmitted with the data bits in both directions. The DP8400 offers byte parity support for up to 40 data bits. If the processor generates byte parity when transferring information to the memory, during the WRITE cycle, then each byte parity bit can be connected to the corresponding byte parity I/O pin on the DP8400, either BP0 or BP1. The DP8400 develops its own internal byte parity bits from the two bytes of data from the processor, and compares them with BP0 and BP1 using an exclusive-OR for both parities. The output of each exclusive-OR is fed to the error flags E0 and E1 as $\overline{PE0}$ and $\overline{PE1}$, so that a byte parity error forces its respective error flag low, as in Table II. These flags are only valid for the Normal WRITE (mode 0) and XP at 0V. The DP8400 checks and generates even byte parity.

When transferring information from the memory to the processor, the DP8400 receives the memory data, and outputs the corresponding byte parity bits on BP0 and BP1 to the processor. The processor block can then check data integrity with its own byte parity generator. If in fact memory data was in error, the DP8400 derives BP0 and BP1 from the memory input data, and not the corrected data, so when corrected data is output from the DP8400, the processor will detect a byte parity error.

If correct byte parity is required, transfer of corrected output data in the DOL to DIL will result in correct byte parity at BP0 and BP1. This can be part of a normal memory re-WRITE cycle once an error has occurred.

TABLE I. ERROR FLAGS AFTER NORMAL READ (MODE 4)

AE	E1	E0	Error Type
0	0	0	No error
1	1	0	Single check bit error
1	1	1	Single-data error
1	0	0	Double-bit error
All Others			Invalid conditions

TABLE II. ERROR FLAGS AFTER NORMAL WRITE (MODE 0)

AE	E1 ($\overline{PE1}$)	E0 ($\overline{PE0}$)	Error Type
0	1	1	No parity error
0	1	0	Parity error, byte 0
0	0	1	Parity error, byte 1
0	0	0	Parity error, bytes 0, 1

TABLE III. DP8400 MODES OF OPERATION

Mode	M2 (R/W)	M1	M0	$\overline{OES}$	Operation
0	0	0	0	X	Normal WRITE DIL → DOL, CG → COL → COB
1	0	0	1	X	Complement WRITE $\overline{DIL}$ → DOL, $\overline{CIL}$ → COL → COB
2	0	1	0	X	Diagnostic WRITE, DLE inhibited DQ8-DQ15 ⊕ CG → SOL → SOB DQ8-DQ15 → CIL → COL → COB
3	0	1	1	X	Complement data-only WRITE $\overline{DIL}$ → DOL, (CG0, 1, 4, 5, $\overline{CG2}$, $\overline{CG3}$) → COL → COB
4	1	0	0	X	Normal READ DIL ⊕ DE → DOL, CIL → COL
5	1	0	1	X	Complement READ $\overline{DIL}$ ⊕ DE → DOL, $\overline{CIL}$ → COL
6A	1	1	0	0	READ generated syndromes, check bit bus, error flags, SG0-SG6 → DQ0-DQ6, CIL0-CIL6 → DQ8-DQ14, E1 → DQ7, E0 → DQ15
6B	1	1	0	1	READ syndrome bus, check bit bus, error flags, SIL0-SIL6 → DQ0-DQ6, CIL0-CIL6 → DQ8-DQ14, E1 → DQ7, E0 → DQ15
7A	1	1	1	0	Generated syndromes replace with zero 0 → SIL → SG, CIL → COL, DIL ⊕ DE → DOL
7B	1	1	1	1	Generated syndromes replace SIL → SG, CIL → COL, DIL ⊕ DE → DOL

TABLE IV. DATA-IN TO CHECK BIT GENERATE, OR DATA BIT ERROR TO SYNDROME-GENERATE MATRIX (16-BIT CONFIGURATION)

		0	1	2	3	4	5	6	7	8	9	1 0	1 1	1 2	1 3	1 4	1 5	
		GENERATE CHECK BITS →																
GENERATED SYNDROMES	0	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0
	1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	1
	2	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	2*
	3	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	3*
	4	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	4
	5	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	5
		4	8	9	7	5	1	3	9	E	B	D	3	C	7	F	F	0
		3	3	2	0	2	3	2	1	3	0	0	1	2	3	2	1	1

DQ0-15

GENERATED CHECK BITS

HEXADECIMAL EQUIVALENT OF SYNDROME BITS

* C2, C3 generate odd parity

MODES OF OPERATION

There are three mode-control pins, M2, M1 and M0, offering 8 major modes of operation, according to Table III.

M2 is the READ/$\overline{\text{WRITE}}$ control. In normal operation, mode 0 is Normal WRITE and mode 4 is Normal READ. By clamping M0 and M1 low, and setting M2 low during WRITE and high during READ, the DP8400 is very easy to use for normal operation. The other modes will be covered in later sections.

16-Bit Configuration

The first two rows on top of the check bit generate matrix (Table IV) indicate the data position of DQ0 to DQ15. The left side of the matrix, listed 0 to 5, corresponds to syndromes S0 to S5. S0 is the least significant syndrome bit. There are two rows of hexadecimal numbers below the matrix. They are the hex equivalent of the syndrome patterns. For example, syndrome pattern in the first column of the matrix is 001011. Its least significant four bits (0010) equal hexadecimal 4, and the remaining two bits (11) equal hexadecimal 3.

Check bit generation is done by selecting different combinations of data bits and generating parities from them. Each row of the check bit generate matrix corresponds to the generation of a check bit numbered on the right hand side of the matrix, and the ones in that row indicate the selection of data bits.

The following are the check bit generate equations for 16-bit wide data words:

$CG0 = DQ2 \oplus DQ3 \oplus DQ4 \oplus DQ5 \oplus DQ6 \oplus DQ7 \oplus DQ9 \oplus DQ10 \oplus DQ11 \oplus DQ13 \oplus DQ14 \oplus DQ15$

$CG1 = DQ3 \oplus DQ6 \oplus DQ8 \oplus DQ9 \oplus DQ11 \oplus DQ13 \oplus DQ14 \oplus DQ15$

$^{*}CG2 = DQ0 \oplus DQ3 \oplus DQ4 \oplus DQ8 \oplus DQ10 \oplus DQ12 \oplus DQ13 \oplus DQ14 \oplus DQ15 \oplus 1$

$^{*}CG3 = DQ1 \oplus DQ2 \oplus DQ7 \oplus DQ8 \oplus DQ9 \oplus DQ10 \oplus DQ12 \oplus DQ14 \oplus DQ15 \oplus 1$

$CG4 = DQ0 \oplus DQ1 \oplus DQ5 \oplus DQ7 \oplus DQ8 \oplus DQ11 \oplus DQ13 \oplus DQ15$

$CG5 = DQ0 \oplus DQ1 \oplus DQ2 \oplus DQ4 \oplus DQ5 \oplus DQ6 \oplus DQ8 \oplus DQ12 \oplus DQ13 \oplus DQ14$

*CG2 and CG3 are odd parities.

The following error map (Table V) depicts the relationship between all possible error conditions and their associated syndrome patterns. For example, if a syndrome pattern is S0 – 5 = 111101, data bit 14 is in error.

Figure 4 shows how to connect one DP8400 in a 16-bit configuration, in order to detect and correct single or double-bit errors. For a Normal WRITE, processor data is presented to the DP8400, where it is fed through DIL0 and DIL1 to the check bit generator. This generates 6 parity bits from different combinations of data bits, according to Table IV. The numbers in the row below the table are the hexadecimal equivalent of the column bits (with bits 6, 7 low). A '1' in any row indicates that the data bit in that column is connected to the parity generator for that row. For example, check bit 1 generates parity from data bits 3, 6, 8, 9, 11, 13, 14, and 15.

Check bits 0, 1, 4, 5, and 6 generate even parity, and check bits 2 and 3 generate odd parity. This is done to insure that a total memory failure is detected. If all check bits were even parity, then all zeros in the data word would generate all check bits zero and a total memory failure would not be detected when a memory READ was performed. Now all-zero-data bits produce C2 and C3 high and a total memory failure will be detected. When reading back from the same location, the memory data bits (possibly in error) are fed to the same check bit generator, where they are compared to the memory check bits (also possibly in error) using 6 exclusive-OR gates. The outputs of the XORs are the syndrome bits, and these can be determined according to Table IV for one data bit error. For example, an error in bit 2 will produce the syndrome word 101001 (for S5 to S0 respectively). The syndrome word is decoded by the error encoder to the error flags, and the data-error decoder to correct a single data bit error. Assuming the memory data has been latched in the DIL, by making DLE go low, memory data can be disabled. Then by setting $\overline{\text{OB0}}$ and $\overline{\text{OB1}}$ low, corrected data will appear on the data bus. The syndromes are available as outputs on pins S0-5 when $\overline{\text{OES}}$ is low. It is also possible to feed in syndromes to SIL when $\overline{\text{OES}}$ is high and CSLE goes high. This can be useful when using the Error Management Unit shown in *Figure 4.* C6 and S6 are not used for 16 bits. It is safe therefore to make C6 appear low, through a 2.7 kΩ resistor to ground. The same applies for S6 if syndromes are input to the DP8400. If $\overline{\text{OES}}$ is permanently low, S6 may be left open.

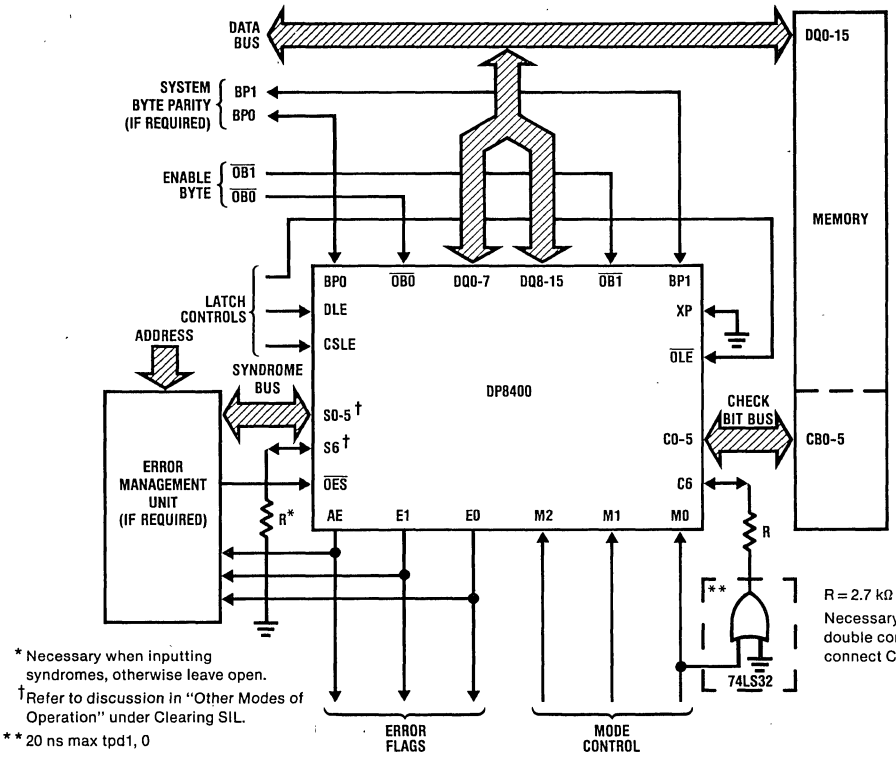
Any 16-bit memory correct system using the DP8400 without syndrome inputs must keep the $\overline{\text{OES}}$ pin grounded, then all the syndrome I/O pins may be left open. The reason for this is that the DP8400 resets the syndrome input latch at power up. If the $\overline{\text{OES}}$ pin is grounded, the syndrome input latch will remain reset for normal operations.

The parameter t_{NMR} (see *Figure 10b*), new mode recognized time, is measured from M2 (changing from READ to WRITE) to the valid check bits appearing on the check bit bus, provided the $\overline{\text{OLE}}$ was held low.

TABLE V. SYNDROME DECODE TO BIT IN ERROR FOR 16-BIT DATA WORD

	S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Syndrome Bits	S1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	S2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	S3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S5	S4																
0	0	NE	C0	C1	D	C2	D	D	3	C3	D	D	9	D	10	T	D
0	1	C4	D	D	11	D	T	T	D	D	7	T	D	T	D	D	15
1	0	C5	D	D	6	D	4	T	D	D	2	T	D	12	D	D	14
1	1	D	5	T	D	0	D	D	13	1	D	D	T	D	T	8	D

NE = no error
Number = single data bit in error
Cn = check bit n in error
D = two bits in error
T = three errors detected



* Necessary when inputting syndromes, otherwise leave open.

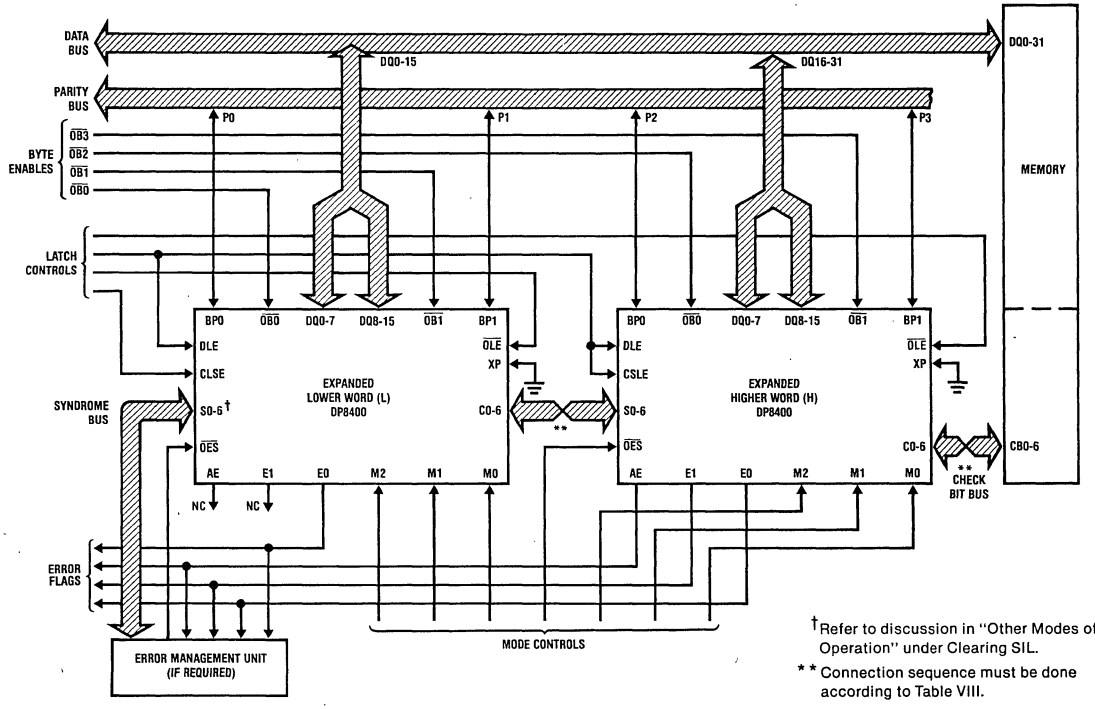
† Refer to discussion in "Other Modes of Operation" under Clearing SIL.

** 20 ns max tpd1, 0

R = 2.7 kΩ

Necessary only when incorporating double complement correct. Otherwise connect C6 to GND through R.

FIGURE 4. 16-Bit Configuration Using One DP8400



† Refer to discussion in "Other Modes of Operation" under Clearing SIL.

** Connection sequence must be done according to Table VIII.

FIGURE 5. 32-Bit Error Detection and Correction

The parameter t_{MCR} (see *Figure 10b*), mode change recognized time, is measured from M2 (changing from WRITE to READ) when both E1 and E2 become invalid. This is required when a memory correcting system employs the DP8400 with byte parity checking. The E1 and E2 pins flag the byte parity error in a memory WRITE cycle. When the DP8400 switches to a subsequent memory READ cycle, it requires t_{MCR} for E1 and E2 to be switched to flag any READ error(s).

EXPANDED OPERATION

32-Bit Configuration

Figure 5 shows how to connect two DP8400s in cascade to detect single and double-bit errors, and to correct single-data errors. The same circuit will also correct double-bit errors once a double-error has been detected, provided at least one error is a hard error. The lower chip L is in effect a slave to the higher chip H, which controls the memory check bits and error reporting. The check bit bus of L is reordered and connected to the syndrome bus of H, as shown in *Figure 5*.

In a Normal WRITE mode, referring to *Figures 13a, 13b, and 13c*, the 6 check bits generated from the lower 16 bits (CGL) are transferred via the COL to the COB of L, provided $\overline{OLE}$ is high and M2 (R/$\overline{W}$) of L is low. These partial check bits from L then appear at SIL of H, so that with CSLE high, they combine with the 6 check bits generated in H with an overlap of one bit, to produce 7 check bits. With M2 (R/$\overline{W}$) of H low, these 7 check bits are output from COB to memory.

A READ cycle may consist of DETECT ONLY or DETECT THEN CORRECT, depending on the system approach. In both approaches, L writes its partial check bits, CGL, to H as in WRITE mode. H develops the syndrome bits from CGL, CGH and the 7 check bits read from memory in CIL. H then outputs from its error encoder (EE) if there is an error. If corrected data is required, H already knows if it has a single-data error from its syndrome bits, but if not, it must transfer partial syndromes back to L. These partial syndromes PSH, (CGH XOR-ed with CIL), are stored in SOL of H. L must therefore change modes from WRITE to READ, while H outputs the partial syndromes from its SOB by setting $\overline{OES}$ low. The partial syndromes are fed into CIL of L and XOR-ed with CGL to produce syndrome bits at SGL. The data error decoder, DED, then corrects the error in L. The DED of H will already have corrected an error in the higher 16 bits. Only one error in 32 bits can be corrected as a single-data error, the chip with no error does not change the contents of its DIL when it is enabled in DOL. Table VI shows the 3 error flags of H, which become valid during the DETECT cycle. E0 of L becomes valid during the CORRECT cycle, so that the 4 flags provide complete error reporting.

TABLE VI. ERROR FLAGS AFTER NORMAL READ (32-BIT CONFIGURATION)

AE (H)	E1 (H)	E0 (H)	E0 (L)*	Error Type
0	0	0	0	No error
1	1	0	0	Single-check bit error
1	1	1	0	Single-data bit error (H)
1	1	0	1	Single-data bit error (L)
1	0	0	0	Double-bit error
All Others				Invalid conditions

* E0 (L) is valid after transfer of partial syndromes from higher to lower

Equations for 32-bit expansion:

$$t_{DCB32} = t_{DCB16} + t_{SCB16}$$
$$t_{DEV32} = t_{DCB16} + t_{SEV16}$$
$$t_{DCD32}\ (\text{High Chip}) = t_{DCB16} + t_{SCD16}$$
$$t_{DCD32}\ (\text{Low Chip}) = t_{DCB16} + t_{BR}{}^{*} + t_{CCD16}$$

*t_{BR}: Bus reversing time (25 ns)

32-Bit Matrix

Table VII shows a 32-bit matrix using two DP8400s in cascade as in *Figure 5*. This is one of 12 matrices that work for 32 bits. The matrix for bits 0 to 15 (lower chip) is the matrix of Table IV for 16-bit configuration, with row 6 always '0'. The matrix for bits 16 to 31 (higher chip) uses the same row combinations but interchanged, for example, the 3rd row (row 2) of L matrix is the same as the 6th row (row 5) of the H matrix. This means row 5 of H is in fact check bit 2 of H. Thus, the 6th row (row 5) combines generated check bit 5 (CG5) of L and generated check bit 2 of H. Check bit 5 of L therefore connects to the syndrome bit 2 (CG2) of H, and the composite generated check bit is written to check bit 2 of memory. Thus C2 performs a parity check on bits 0, 1, 2, 4, 5, 6, 8, 12, 13, 14, of L, and bits 16, 19, 20, 24, 26, 28, 29, 30, 31, of H. CG2 and CG3 generate odd parity, so that CG5 of L generates even parity which combines with CG2 of H generating odd parity. CG3 of L and CG3 of H both generate odd parity causing C3 to memory to represent even parity. Only 6 check bits are generated in each chip, the 7th (CG6) is always zero with XP grounded. Thus CG6 of L combines with CG0 of H so that C0 to memory is the parity of bits 18, 19, 20, 21, 22, 23, 25, 26, 27, 29, 30, 31. Similarly C6 to memory is only CG2 of L. The 7 composite generated check bits of H can now be written to memory.

When reading data and check bits from memory, CG6-CG0 of L are combined with CG6-CG0 of H in the same combination as WRITE. Memory check bits are fed into C6-C0 of H and compared with the 7 combined parity bits

TABLE VII. DATA BIT ERROR TO SYNDROME-GENERATE MATRIX (32-BIT CONFIGURATION)

	L																H																
											1	1	1	1	1	1																		
	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	DQ0-31
0	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	1
1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	5
*2	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
*3	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	3
4	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	4
5	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	2
6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0
	4	8	9	7	5	1	3	9	E	B	D	3	C	7	F	F	2	A	A	1	2	2	3	8	B	9	8	1	A	3	B	9	0	HEX
	3	3	2	0	2	3	2	1	3	0	0	1	2	3	2	1	3	1	4	6	6	5	4	5	3	4	6	5	2	7	6	7	1	

SYNDROMES

GENERATED CHECK BITS

* CG2, CG3 generate odd parity

TABLE VIII. CHECK BIT PORT TO SYNDROME PORT INTERCONNECTIONS FOR EXPANSION TO 32 BITS

		LS		LC	HS		HC		
Syndrome I/O to Management	S0	0		0	1		1	C0	Check Bit I/O to Memory
	S1	1		1	5		5	C1	
	S2	2		2	6		6	C2	
	S3	3		3	3		3	C3	
	S4	4		4	4		4	C4	
	S5	5		5	2		2	C5	
	S6	6		6	0		0	C6	

TABLE IX. SYNDROME DECODE TO BIT IN ERROR FOR 32-BIT DATA WORD

		S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Syndrome Bits		S1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		S2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		S3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S6	S5	S4																
0	0	0	NE	C0	C1	D	C2	D	D	3	C3	D	D	9	D	10	T	D
0	0	1	C4	D	D	11	D	T	T	D	D	7	17	D	T	D	D	15
0	1	0	C5	D	D	6	D	4	T	D	D	2	28	D	12	D	D	14
0	1	1	D	5	16	D	0	D	D	13	1	D	D	24	D	T	8	D
1	0	0	C6	D	D	22	D	T	T	D	D	25	18	D	T	D	D	T
1	0	1	D	27	21	D	T	D	D	T	23	D	D	T	D	T	T	D
1	1	0	D	19	20	D	T	D	D	T	26	D	D	30	D	T	T	D
1	1	1	T	D	D	29	D	T	T	D	D	31	T	D	T	D	D	T

NE = no error Cn = check bit n in error T = three errors detected
Number = single data bit in error D = two bits in error

in H, to produce 7 syndrome bits S6-S0. H can now determine if there is any error, and if it has a single-data error, it can locate it and correct it without transferring partial syndromes to L. As an example of a DETECT cycle, CG5 of L combines with CG2 of H and is compared in H with memory check bit 2.

If L is now set to mode 4, Normal READ, and $\overline{OES}$ of H is set low, the partial syndromes of H (CG6-CG0 of H XOR-ed with C6-C0 of H) are transferred and shifted to L. L receives these partial syndromes (S6-S0 of H) as check bit inputs C2, C1, C4, C3, C5, C0, C6 respectively, and compares them with CG6-CG0 respectively, to produce syndrome bits S6-S0. L now decodes these syndromes to correct any single-data error in data bits 0 to 15. For example, partial syndrome bit 2 of H combines with generated check bit 5 of L to produce syndrome bit 5 in L. An error in data bit 10 will create syndrome bits in L as 0001101 from S6-S0, and these will appear on S6-S0 of L with $\overline{OES}$ low. An error in H will appear as per the H matrix. For example, an error in bit 16 will cause S6-S0 of L to be 0110010.

If $\overline{OES}$ of L is set low, this syndrome combination appears on pins S6 to S0. For errors in bits 0 to 15, the syndrome outputs will be according to Table VII. For errors in bits 16 to 31, the syndrome outputs from L will still be according to Table VII due to the shifting of partial syndrome bits from H to L. The syndrome outputs from L are unique for each of the possible 32 bits in error.

If there is a check bit error, only one syndrome bit will be high. For example, if C5 is in error, then S1 of L will be high. For double-errors, an even number of syndrome bits will be high, derived from XOR-ing the two single-bit error syndromes. As mentioned previously, this is only one of the 12 approaches to connecting two chips for 32 bits, 6 of which are mirror images.

Table VIII depicts the exact connection for 32-bit expansion. LS equals syndrome bits of L. LC equals check bits of L. HS equals syndrome bits of H. HC equals check bits of H. Syndrome bits S0 to S6 of L are connected to system syndrome bits S0 to S6. LC and HS columns are lined together showing the check bit port of L connected to the syndrome port of H in the exact sequence as shown in Table VIII. For example, check bit C0 of L is connected to the syndrome bit S1 of H, and check bit C6 of L is connected to the syndrome bit S0 of H. Check bits of H are connected to the system check bits in the order shown. Check bit C1 of H is connected to the system check bit C0.

Expansion for Data Words Requiring 8 Check Bits

For 16-bit and 32-bit configurations, XP is set permanently low. In 48-bit or 64-bit configurations, XP is either set permanently to V_{CC} or left open, according to Table X, to provide 8 check bits and syndrome bits.

TABLE X. XP: EXPANSION STATUS

XP	Status	Data Bus
0V	BP0 and BP1 are byte parity I/O CG6 = 0	< 40 Bits
Open	No byte parity I/O, CG6 and CG7 = word parity	≥ 40 Bits
V_{CC}	No byte parity I/O, CG6 and CG7 = 0	≥ 40 Bits

48-Bit Expansion

Three DP8400s are required for 48 bits, with the higher chip using all 8 of its check bits to the memory. No byte parity is available for 48 or 64 bits. XP of all three chips must be at V_{CC}. The three chips are connected in cascade

TABLE XI. CHECK BIT PORT TO SYNDROME PORT INTERCONNECTIONS FOR EXPANSION TO 48 BITS

		LL S		LL C	LH S		LH C	HL S		HL C		
Syndrome I/O to Management	S0	0		0	1		1	6		6	C0	Check Bit I/O to Memory
	S1	1		1	5		5	1		1	C1	
	S2	2		2	6		6	4		4	C2	
	S3	3		3	3		3	7		7	C3	
	S4	4		4	4		4	2		2	C4	
	S5	5		5	2		2	3		3	C5	
	S6	6		6	0		0	5		5	C6	
	S7	7		7	7		7	0		0	C7	

For example: S0 of LL is connected to system syndrome S0. C0 of LL is connected to S1 of LH. C1 of LH is connected to S6 of HL. C6 of HL is connected to system check bit C0.

TABLE XII. SYNDROME DECODE TO BIT IN ERROR FOR 48-BIT DATA WORD

Syndrome Bits																	
			S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
			S1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
			S3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
S7	S6	S5	S4																
0	0	0	0	NE	C0	C1	D	C2	D	D	3	C3	D	D	9	D	10	T	D
0	0	0	1	C4	D	D	11	D	T	T	D	D	7	17	D	T	D	D	15
0	0	1	0	C5	D	D	6	D	4	T	D	D	2	28	D	12	D	D	14
0	0	1	1	D	5	16	D	0	D	D	13	1	D	D	24	D	T	8	D
0	1	0	0	C6	D	D	22	D	T	T	D	D	25	18	D	T	D	D	T
0	1	0	1	D	27	21	D	32	D	D	T	23	D	D	T	D	T	T	D
0	1	1	0	D	19	20	D	33	D	D	T	26	D	D	30	D	T	T	D
0	1	1	1	44	D	D	29	D	T	40	D	D	31	T	D	T	D	D	T
1	0	0	0	C7	D	D	T	D	T	43	D	D	T	T	D	T	D	D	T
1	0	0	1	D	T	35	D	T	D	D	T	T	D	D	T	D	T	T	D
1	0	1	0	D	T	41	D	39	D	D	T	T	D	D	T	D	T	T	D
1	0	1	1	42	D	D	T	D	T	47	D	D	T	T	D	T	D	D	T
1	1	0	0	D	T	38	D	37	D	D	T	T	D	D	T	D	T	T	D
1	1	0	1	36	D	D	T	D	T	45	D	D	T	T	D	T	D	D	T
1	1	1	0	34	D	D	T	D	T	T	D	D	T	T	D	T	D	D	T
1	1	1	1	D	T	46	D	T	D	D	T	T	D	D	T	D	T	T	D

NE = no error
Number = single data bit in error
Cn = check bit n in error
D = two bits in error
T = three errors detected

as in *Figure 6*, but with the HH chip removed. The error flags are as Table XV, but with AE (HH) and E1 (HH) becoming AE (HL) and E1 (HL), and E0 (HH) removed.

48-Bit Matrix

The matrix for 48 bits is that for 64 bits shown (in Table XVI) but only using bits 0 to 47. This is one of many matrices for 48-bit expansion using the basic 16-bit matrix. The matrix shown uses 2 zeroes for CG6 and CG7, for all three chips, with XP set to V_{CC}. Other matrices may use CG6 and CG7 as word parity with XP open.

64-Bit Expansion

There are two basic methods of expansion to 64 bits, both requiring 8 check bits to memory, and four DP8400s. One is the cascade method of *Figure 6*, requiring no extra ICs. With this method partial check bits have to be transferred through three chips in the WRITE or DETECT mode, and partial syndrome bits transferred back through three chips in CORRECT mode. This method is similar to *Figure 5*, 32-bit approach. The connections between the check bit bus and syndrome bus for each of the chip pairs are shown in Table XIII.

The error flags of HH are valid during the DETECT cycle as in Table XV, and the other error flags are valid during the CORRECT cycle.

A faster method of 64-bit expansion shown in *Figure 7* requires a few extra ICs, but can WRITE in 57 ns, DETECT in 57 ns or DETECT THEN CORRECT in 116 ns. In the WRITE mode, all four sets of check bits are combined externally in the 8 74S280 parity generators. These generate 8 composite check bits from the system data, which are then enabled to memory. In the DETECT mode, again 8 composite check bits are generated, from the memory data this time, and compared with the memory check bits to produce 8 external syndrome bits. These syndrome bits may be OR-ed to determine if there is any error. By making the 74S280 outputs $\overline{\text{SYNDROMES}}$, then any bit low causes the 74S30 NAND gate to go high, giving any error indication. To correct the error, these syndrome bits are fed re-ordered into SIL of each DP8400 now set to mode 7B. This enables the syndromes directly to SG and then

DED of each chip. One chip will output corrected data, while the other three output non-modified data (but still correct).

Equations for fast 64-bit expansion:

$t_{DCB64} = t_{DCB16} + t_{pd}(74S280) + t_{pd}(74S240)$
$t_{DEV64} = t_{DCB16} + t_{pd}(74S280) + t_{pd}(74S30)$
$t_{DCD64} = t_{DCB16} + t_{pd}(74S280) + t_{pd}(74ALS533) + t_{SCD16}$

64-Bit Matrix

With the 64-bit matrix shown in Table XVI, it is necessary to set at least one chip with CG6, CG7 non-zero. The highest chip, connected to data bits 48 to 63, has XP set open, so that its CG6 and CG7 are word parity. The syndrome word of the highest chip will now have either 5 or 7 syndrome bits high, but inside the chip CG6 and CG7 remove two of these in a READ so that the chip sees the normal 3 or 5 syndrome bits.

TABLE XIII. CHECK BIT PORT TO SYNDROME PORT INTERCONNECTIONS FOR EXPANSION TO 64 BITS

		LL S		LL C	LH S		LH C	HL S		HL C	HH S		HH C		
Syndrome I/O to Management	S0	0		0	1		1	6		6	7		7	C0	Check Bit I/O to Memory
	S1	1		1	5		5	1		1	0		0	C1	
	S2	2		2	6		6	4		4	1		1	C2	
	S3	3		3	3		3	7		7	2		2	C3	
	S4	4		4	4		4	2		2	3		3	C4	
	S5	5		5	2		2	3		3	4		4	C5	
	S6	6		6	0		0	5		5	5		5	C6	
	S7	7		7	7		7	0		0	6		6	C7	

For example: S0 of LL is connected to system syndrome S0. C0 of LL is connected to S1 of LH. C1 of LH is connected to S6 of HL. C6 of HL is connected to S7 of HH. C7 of HH is connected to system check bit C0.

TABLE XIV. SYNDROME DECODE TO BIT IN ERROR FOR 64-BIT DATA WORD

Syndrome Bits S7 S6 S5 S4																	
	S0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	S1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	S2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	S3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0 0 0 0		NE	C0	C1	D	C2	D	D	3	C3	D	D	9	D	10	T	D
0 0 0 1		C4	D	D	11	D	T	T	D	D	7	17	D	T	D	D	15
0 0 1 0		C5	D	D	6	D	4	T	D	D	2	28	D	12	D	D	14
0 0 1 1		D	5	16	D	0	D	D	13	1	D	D	24	D	T	8	D
0 1 0 0		C6	D	D	22	D	T	T	D	D	25	18	D	T	D	D	T
0 1 0 1		D	27	21	D	32	D	D	T	23	D	D	T	D	T	T	D
0 1 1 0		D	19	20	D	33	D	D	T	26	D	D	30	D	T	T	D
0 1 1 1		44	D	D	29	D	T	40	D	D	31	T	D	T	D	D	T
1 0 0 0		C7	D	D	T	D	T	43	D	D	T	T	D	T	D	D	51
1 0 0 1		D	T	35	D	T	D	D	57	T	D	D	58	D	T	T	D
1 0 1 0		D	T	41	D	39	D	D	59	T	D	D	T	D	T	T	D
1 0 1 1		42	D	D	55	D	T	47	D	D	T	T	D	T	D	D	63
1 1 0 0		D	T	38	D	37	D	D	54	T	D	D	52	D	T	T	D
1 1 0 1		36	D	D	50	D	T	45	D	D	60	T	D	T	D	D	62
1 1 1 0		34	D	D	53	D	T	T	D	D	48	T	D	T	D	D	61
1 1 1 1		D	49	46	D	T	D	D	T	T	D	D	T	D	56	T	D

NE = no error
Number = single data bit in error
Cn = check bit n in error
D = two bits in error
T = three errors detected

TABLE XV. ERROR FLAGS AFTER NORMAL READ (ANY 64-BIT CONFIGURATION)

AE (HH)	E1 (HH)	E0 (HH)	E0 (HL)	E0 (LH)	E0 (LL)	Error Type
0	0	0	0	0	0	No error
1	1	0	0	0	0	Single-check bit error
1	1	1	0	0	0	Single-data bit error in HH
1	1	0	1	0	0	Single-data bit error in HL
1	1	0	0	1	0	Single-data bit error in LH
1	1	0	0	0	1	Single-data bit error in LL
1	0	0	0	0	0	Double-error

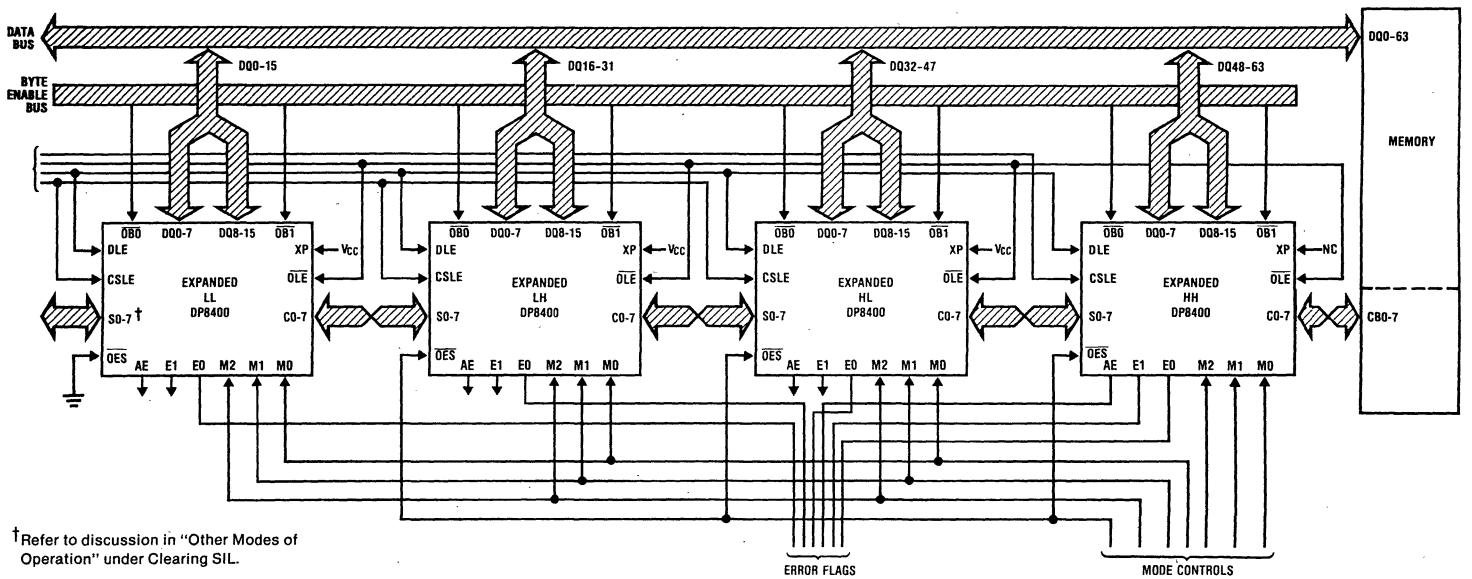


FIGURE 6. Cascade Expansion Using No Extra ICs (64-Bit Configuration)

TABLE XVI. DATA BIT ERROR TO SYNDROME-GENERATE MATRIX (64-BIT CONFIGURATION)

SYNDROMES	LL	LH	HL	HH	
	1 1 1 1 1 1	1 1 1 1 2 2 2 2 2 2 2 2 2 2 3 3	3 3 3 3 3 3 3 3 4 4 4 4 4 4 4 4	4 4 5 5 5 5 5 5 5 5 5 5 6 6 6 6	DQ0-63
	0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5	6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1	2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7	8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3	
0	0 0 1 1 1 1 1 1 0 1 1 1 0 1 1 1	0 0 0 1 0 0 1 0 1 1 0 1 0 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	7
1	0 0 0 1 0 0 1 0 1 1 0 1 0 1 1 1	1 1 1 0 1 1 1 0 1 0 0 0 1 1 1 0	0 0 0 1 0 0 1 0 1 1 0 1 0 1 1 1	0 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1	0
2	1 0 0 1 1 0 0 0 1 0 1 0 1 1 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1 0 0 0 1 0 1 1 0 0 1 0 1 0 1	0 0 0 1 0 0 1 0 1 1 0 1 0 1 1 1	1
3	0 1 1 0 0 0 0 1 1 1 1 0 1 0 1 1	0 1 1 0 0 0 0 1 1 1 1 0 1 0 1 1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 1 1 0 0 0 1 0 1 0 1 1 1 1	2
4	1 1 0 0 0 1 0 1 1 0 0 1 0 1 0 1	1 1 0 0 0 1 0 1 1 0 0 1 0 1 0 1	1 0 0 1 1 0 0 0 1 0 1 0 1 1 1 1	0 1 1 0 0 0 0 1 1 1 1 0 1 0 1 1	3
5	1 1 1 0 1 1 1 0 1 0 0 0 1 1 1 0	1 0 0 1 1 0 0 0 1 0 1 0 1 1 1 1	0 1 1 0 0 0 0 1 1 1 1 0 1 0 1 1	1 1 0 0 0 1 0 1 1 0 0 1 0 1 0 1	4
6	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1	1 1 1 0 1 1 1 0 1 0 0 0 1 1 1 0	1 1 1 0 1 1 1 0 1 0 0 0 1 1 1 0	5
7	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 0 1 1 1 0 1 1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	6
	4 8 9 7 5 1 3 9 E B D 3 C 7 F F	2 A A 1 2 2 3 8 B 9 8 1 A 3 B 9	4 4 0 2 0 4 2 4 6 2 0 6 0 6 2 6	9 1 3 F B 3 7 3 D 7 B 7 9 F F F	0 HEX
	3 3 2 0 2 3 2 1 3 0 0 1 2 3 2 1	3 1 4 6 6 5 4 5 3 4 6 5 2 7 6 7	5 6 E 9 D C C A 7 A B 8 7 D F B	E F D 8 C E C B F 9 9 A D E D B	1

GENERATED CHECK BITS

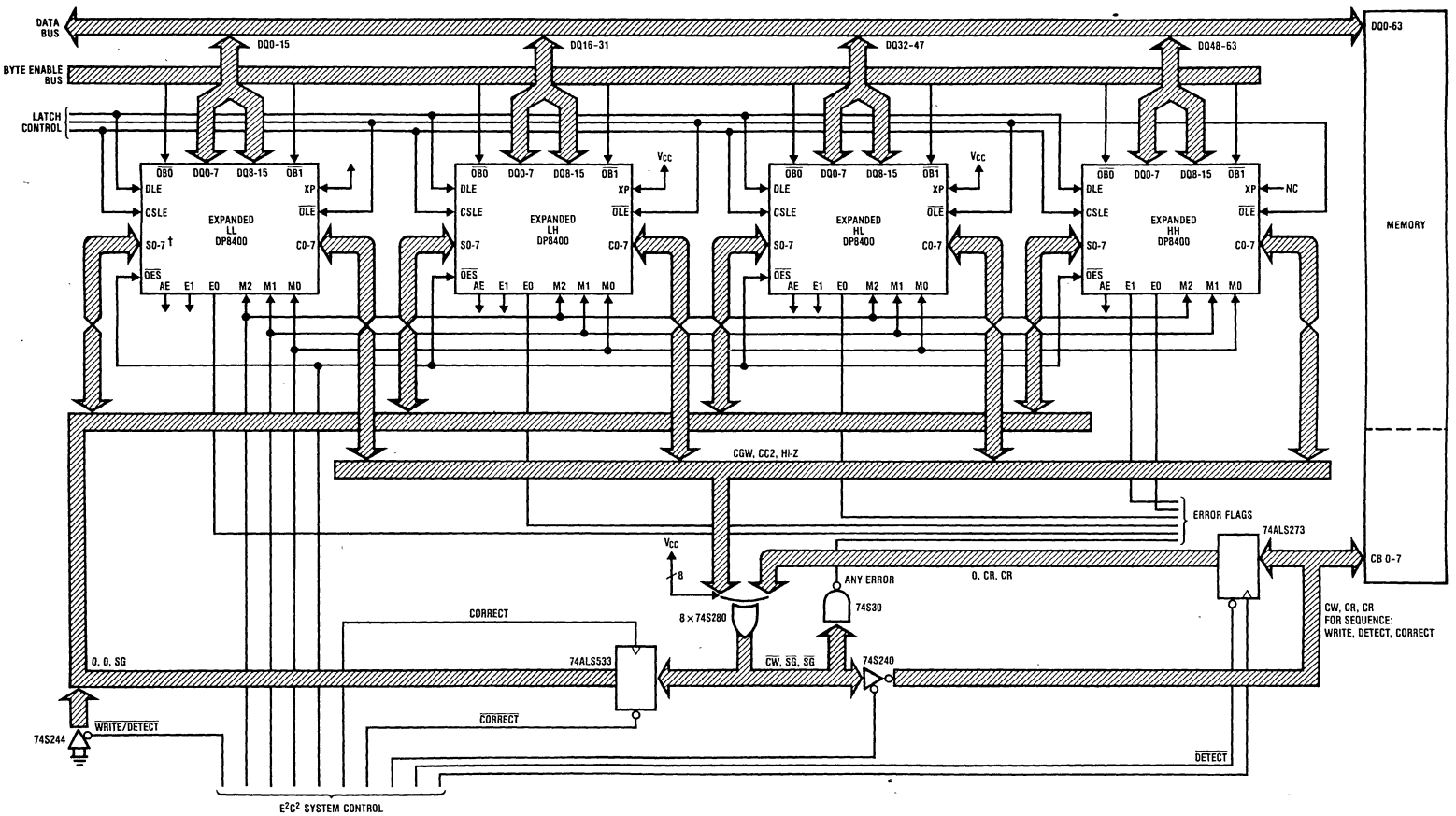


FIGURE 7. Parallel Expansion (Fast 64-Bit Configuration)

OTHER MODES OF OPERATION

Double Error Correction, using the Double-Complement Approach

The DP8400 can be made to correct two errors, using no extra ICs or check bits, if at least one of the two errors detected is a hard error. This does require an extra memory WRITE and READ. Nevertheless, if a permanent failure exists, and an additional error occurs (creating two errors), both errors can be corrected, thereby saving a system crash.

Once a double error has been detected, the system puts the DP8400 in COMPLEMENT mode by setting M0 high. First a WRITE cycle is required and M2 is set low, putting the chip in mode 1, Table III, (COMPLEMENT WRITE), so that the contents of DIL are complemented into DOL, and the contents of CIL complemented into COL. $\overline{OB0}$ and $\overline{OB1}$ are set low so that complemented data and check bits can be written back to the same location of memory. Writing back complemented data to a location with a hard error forces the error to repeat itself. For example, if cell N of a particular location is jammed permanently high, and a low is written to it, a high will be read. However, when the data is complemented a low is again written, so that a high is read back for the second time. After a second READ (this second READ is a COMPLEMENT READ) of the location, data and check bits from the memory are re-complemented, so that bit N now contains a low. In other words, the error in bit N has corrected itself, while the other bits are true again. If there are two hard errors in a location, both are automatically corrected and the DP8400 detects no error on COMPLEMENT READ, as in *Figure 8a*. *Figure 8b* also shows that if one error is soft, the hard error will disappear on the second READ and the DP8400 corrects the soft error as a single-error. Therefore, in both cases, the DOL contains corrected data, ready to be enabled by $\overline{OB0}$ and $\overline{OB1}$. A WRITE to memory at this stage removes the complemented data written at the start of the sequence.

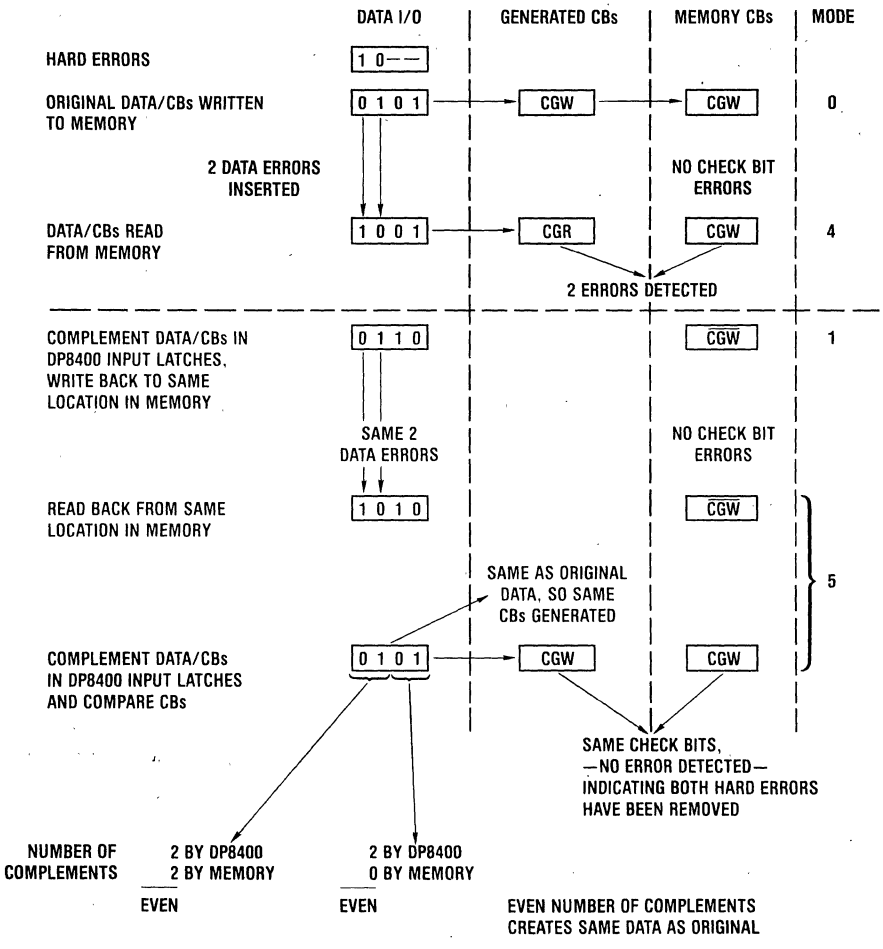


FIGURE 8a. Double Error Correct Complement Hard Error Method—2 Hard Errors in Data Bits

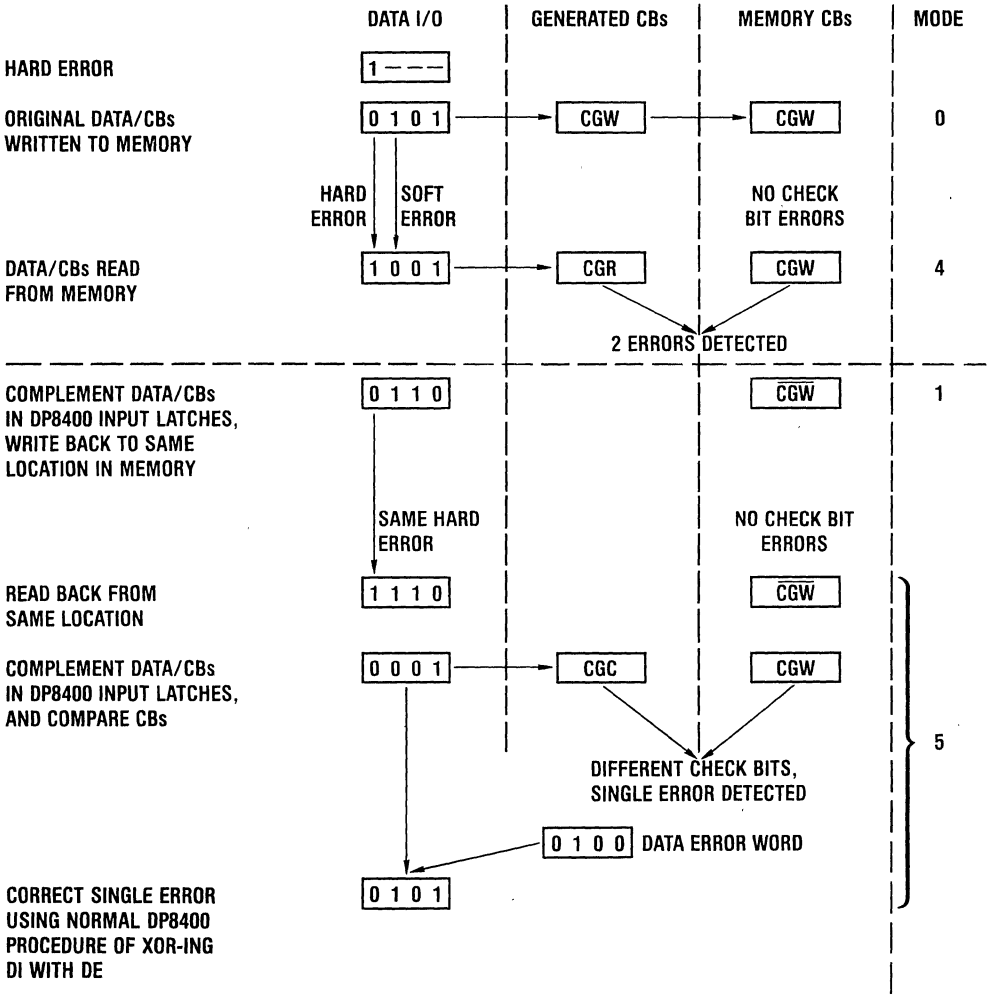


FIGURE 8b. Double Error Correct Complement Hard Error Method — 1 Hard Error, 1 Soft Error In Data Bits

The examples shown in *Figures 8a and 8b* are for 4 data bits. This approach will work for any number of data bits, but for simplicity these examples show how complementing twice corrects two errors in the data bits. The double COMPLEMENT approach also works for any two errors providing at least one is hard. In other words, one data-bit error and one check bit error, or two check bit errors are also corrected if one or both are hard. At the end of the COMPLEMENT READ cycle, the error flags indicate whether the data was correctable or not, as shown in Table XVII. If both the errors were soft, then the data was not correctable and the error flags indicate this.

This approach is ideal where double errors are rare but may occur. To avoid a system crash, a double-error detect now causes the system to enter a subroutine to set the DP8400 in COMPLEMENT mode. This method is also useful in bulk-memory applications, where RAMs are used with known cell failures, and is applicable in 16, 32, 48 or 64-bit configurations. In the 16-bit configuration, modes 1 and 5 of Table III are used. In the 32-bit expanded configuration, modes 1, 5 and 5 are used for the highest chip, and modes 3, 3 and 4 for the lower chip for WRITE, DETECT, and CORRECT. With the lower chip it is necessary to wrap around DOL (after latching its contents in mode 3), back to DIL and perform a Normal READ in mode 4 in the lower chip.

TABLE XVII. ERROR FLAGS AFTER COMPLEMENT READ (MODE 5)

AE	E1	E0	Error Type
0	0	0	Two hard errors
1	1	0	One hard error, one soft check bit error
1	1	1	One hard error, one soft data bit error
1	0	0	Two soft errors, not corrected

Double-Error Correct with Error Logging

Figures 4 and 5 show the E^2C^2 syndrome port connected to an error management unit (EMU). This scheme stores syndromes and the address of locations that fail, thereby logging the errors. Subsequent errors in a memory location that has already stored syndromes in the EMU, can then be removed by injecting the stored syndromes of the first error. To save the addresses and syndromes when power to the EMU is removed, it is necessary to be able to transfer information via the E^2C^2 syndrome port to the processor data bus. This is also useful for logging the errors in the processor. Transfer in the opposite direction is also necessary.

Data Bus to Syndrome Bus Transfer

This is necessary when transferring syndrome information to the error management unit, which is connected to the external syndrome bus. First, data to make CG = 0 (all data bits high) must be latched in DIL. Then in mode 2, data is fed to CIL, XOR-ed with 0, and output via SOL with $\overline{OES}$ low to the syndrome bus. Data is therefore fed directly from the system to the syndrome bus, and this cycle may be repeated as long as DLE is kept low, forcing CG to remain zero.

Syndrome Bus to Data Bus Transfer

This is important when information in the error logger or error management unit has to be read. The DP8400 is set to mode 6B with $\overline{OES}$ high, and with $\overline{OB0}$, $\overline{OB1}$ and $\overline{OLE}$ low. If CSLE is high, the syndrome bus and check bit bus data appear on the lower and upper bytes of the data bus to be read by the system. Also E1 and E0 values that were valid when mode 6 was entered, appear on DQ7 and DQ15.

Full Diagnostic Check of Memory

Using mode 2, it is possible to transfer the upper byte of the data bus directly to the CIL, with CSLE high, without affecting DIL. These simulated check bits then appear on the check bit bus with $\overline{OLE}$ low, which also causes the previously latched contents of DIL to transfer to DOL. By enabling $\overline{OB0}$ and $\overline{OB1}$ data can be written to memory with the simulated check bits. A Normal READ cycle can then aid the system in determining that the memory bits are functioning correctly, since the processor knows the check bits and data it sent to the E^2C^2. Another solution is to put the E^2C^2 in mode 6 and read the memory check bits directly back to the processor.

Self-Test of the E^2C^2 On-Card

Again using mode 2, data written from the processor data bus upper byte to CIL may be stored in CIL, by taking CSLE low. Data can now be fed into DIL from the processor, with DLE set high, as in a Normal READ mode (mode 4). Providing CSLE is kept low, the DP8400 will use the simulated check bits in CIL to perform a diagnostic READ, with valid error reporting and correcting. This may be repeated with new data provided CSLE is kept low. In this way memory is not used, thus by reading corrected data in mode 4, and by reading the generated syndromes, and error flags E0 and E1, the DP8400 can be tested completely on-card without involving memory.

Monitoring Generated Syndromes and Memory Check Bits

Mode 6A enables SG0-SG6 onto DQ0-DQ6, and CIL0-CIL6 onto DQ8-DQ14, provided $\overline{OLE}$, $\overline{OB0}$ and $\overline{OB1}$ are low. Also the two error flags, E1 and E0 (latched from the previous READ mode), appear on DQ7 and DQ15. This may be used for checking the internal syndromes, for reading the memory check bits, or for diagnostics by checking the latched error flags.

Clearing SIL

In the 16-bit only configuration, or the lower chip of expanded configurations, and in various modes of operation in the higher expanded chips, it is required that SIL be maintained at zero. At power-up initialization, both SIL and DIL are reset to all low. If $\overline{OES}$ is kept low, SIL will remain reset because CSLE is inhibited to SIL. Another method is to keep $\overline{OLE}$ always high and the syndrome bus externally set low, or set low whenever CSLE can be used to clear SIL.

Mode 7A also forces the SIL to be cleared whenever CSLE occurs, and also these zero syndromes go to the internal syndrome bus SG. This puts the DP8400 in a PASS-THROUGH mode where the DIL contents pass to DOL and CIL contents to COL, if $\overline{OLE}$ is low.

Power-Up Initialization of Memory

Both SIL and DIL are reset low at power-up initialization. This facilitates writing all zeroes to the memory data bits to set up the memory. The check bits corresponding to all-zero data will appear on the check bit bus if the DP8400 is set to mode 0 and $\overline{OLE}$ is set low. All-zero data appears on the data bus when $\overline{OB0}$ and $\overline{OB1}$ are also set low. The system can now write zero-data and corresponding check bits to every memory location.

Byte Writing

Figure 14a shows the block diagram of a 16-bit memory correction system consisting of a DP8400 error correction chip and a DP8409 DRAM controller chip. There are 12 control signals associated with the interface. Six of the signals are standard DP8400 input signals, three are standard DP8409 input signals, and three are buffer control signals. The buffer control signals, $\overline{PBUF0}$ and $\overline{PBUF1}$, control when data words or bytes from the DP8400/memory data bus are gated to the processor bus and when data words or bytes from the processor are gated to the DP8400/memory data bus.

When the processor is reading or writing bytes to memory, words will always be read or written by the DP8400 and DP8409 error correction and DRAM controller section. The High Byte Enable and Address Data Bit Zero signals from the processor should control the byte transfers via the ocal bus transceiver signals $\overline{PBUF0}$ and $\overline{PBUF1}$. The buffer control signal, $\overline{DOUTB}$, controls when data from memory is gated onto the DP8400/memory data bus.

Figure 14b shows the timing relationships of the 12 control signals, along with the DP8400/memory data bus and some of the DRAM control signals ($\overline{RAS}$ and $\overline{CAS}$). RGCK is the $\overline{RAS}$ generator clock of the DP8409 which is used in Mode 1 (Auto Refresh mode), along with being the system clock.

Having two separate byte enable pins, $\overline{OB0}$ and $\overline{OB1}$, it is fairly easy to implement byte writing using the DP8400. First it is necessary to read from the location to which the byte is to be written. To do this the DP8400 is put in normal Read mode (Mode 4), which will detect and correct a single bit error. $\overline{WIN}$ is kept high and $\overline{RASIN}$ is pulled low, causing the DP8409, now in Mode 5 (Auto Access mode), to start a read memory cycle. The data word and check bits from memory are then enabled onto the DP8400/memory data bus by pulling $\overline{DOUTB}$ low. The data and check bits are valid on the bus after the $\overline{RASIN}$ to $\overline{CAS}$ time (t_{RAC}) plus the column access time (t_{CAC}) of the particular memories used. DLE,CSLE can then be pulled low in order to latch the memory data into the input latches of the DP8400. Next $\overline{OLE}$ can be pulled low to enable the corrected memory word, or the original memory word if no error was present, into the data output latches. The corrected memory word will be available at the data output latches "t_{DCD16}" after the memory word was available at the data input latches. Once the corrected data is available at the output latches $\overline{OLE}$ can be pulled high to latch the corrected data. After this DLE,CSLE can be pulled high in order to enable the input data latches again and $\overline{DOUTB}$ can be pulled high to disable the memory data from the DP8400/memory data bus.

There is no reason to use the data or check bit input latches (DLE,CSLE) of the DP8400 during the read cycle time period if the memory data and checkbits are valid throughout the cycle.

Now the DP8400 can be put into a write cycle (Mode 0 = M2 = Low). At this time the byte to be written to memory and the other byte from memory can be enabled onto the DP8400/memory data bus ($\overline{OB0}$, $\overline{PBUF1}$ or $\overline{OB1}$, $\overline{PBUF0}$ go low). DLE,CSLE can now transition low to latch the new memory word into the data input latch. Next $\overline{OLE}$ is pulled low to enable the output latches. When the new checkbits are valid, t_{DCB16} after the data word is valid on the DP8400/memory data bus, $\overline{OLE}$ and $\overline{DLE}$ can be pulled high to latch the new memory word into the output latches, and then $\overline{WIN}$ can be pulled low to write the data into memory. $\overline{RASIN}$ should be held low long enough to cause the new data and check bits to be stored into memory ($\overline{WIN}$ data hold time).

DLE,CSLE and $\overline{OLE}$ could transition high and low simultaneously instead of being sequenced as was done in this example.

Also a READ-MODIFY-WRITE cycle was performed, taking approximately 30% longer than a normal memory WRITE cycle. A READ and then a WRITE memory cycle could have been used in the above example but it would have taken longer.

Because data from the processor was valid at the same time as data from memory, memory buffers were used ($\overline{PBUF0}$,$\overline{PBUF1}$,$\overline{DOUTB}$).

A byte READ from memory is no different from a normal READ. This approach may be used for a 16-bit processor using byte writing, or an 8-bit processor using a 16-bit memory to reduce the memory percentage of check bits, or with memory word sizes greater than two bytes.

Beyond Single-Error Correct

With the advent of larger semiconductor memories, the frequency of the soft errors will increase. Also some memory system designers may prefer to buy less expensive memories with known cell, row or column failures, thus, more hard errors. All this means that double-error correct, triple-error detect capability, and beyond will become increasingly important. The DP8400 can correct two errors, provided one or both are hard errors, with no extra components, using the double complement approach. There are two other approaches to enhance reliability and integrity. One is to use the error management unit to log errors using the syndrome bus, and then to output these syndromes, when required, back to the DP8400.

Double Syndrome Decoding

The other approach takes advantage of the Rotational Syndrome Word Generator matrix. This matrix is an improvement of the Modified Hamming-code, so that if, on a second DP8400, the data bus is shifted or rotated by one bit, and 2 errors occur, the syndromes for this second chip will be different from the first for any 2 bits in error. Both chips together output a unique set of syndromes for any 2 bits in error. This can be decoded to correct any 2-bit error. This is not possible with other Modified Hamming-code matrices.

Absolute Maximum Ratings (Note 1)

Storage Temperature Range	−65°C to +150°C
Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Output Sink Current	50 mA
Maximum Power Dissipation* at 25°C	
Molded Package	3269mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate molded package 26.2mW/°C above 25°C.

Operating Conditions

	Min	Max	Unit
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	70	°C

Electrical Characteristics (Note 2) $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to 70°C unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Threshold				0.8	V
V_{IH}	Input High Threshold		2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_C = −18 mA		−0.8	−1.5	V
I_{IH}	Input High Current	V_{IN} = 2.7V		1	160	μA
I_{IH} (XP)	Input High Current	V_{CC} = Max, XP = 5.25V		2.5	3.6	mA
I_{IL} (XP)	Input Low Current	V_{CC} = Max, XP = 0V		−2.5	−3.6	mA
I_{IL} (BP0/C7)	Input Low Current	V_{CC} = Max, V_{IN} = 0.5V		−100.0	−500	μA
I_{IL} (BP1/S7)	Input Low Current	V_{CC} = Max, V_{IN} = 0.5V		−100.0	−500	μA
I_{IL} (CSLE)	Input Low Current	V_{CC} = Max, V_{IN} = 0.5V		−150.0	−750	μA
I_{IL} (DLE)	Input Low Current	V_{CC} = Max, V_{IN} = 0.5V		−200.0	−1000	μA
I_{IL}	Input Low Current	V_{CC} = Max, V_{IN} = 0.5V		−50.0	−250	μA
I_I	Input High Current (Max)	V_{IN} = 5.5V (Except XP Pin)			1.0	mA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA (Except BP0, BP1) I_{OL} = 4 mA (BP0, BP1 Only)		0.3 0.3	0.5 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = −100 μA I_{OH} = −1 mA	2.7 2.4	3.2 3.0		V V
I_{OS}	Output Short Current (Note 3)	V_{CC} = Max		−55	−100	mA
I_{CC}	Supply Current	V_{CC} = Max		340	410	mA
C_{IN} (I/O)	Input Capacitance All Bidirectional Pins	Note 4		8.0		pF
C_{IN}	Input Capacitance All Unidirectional Input Pins	Note 4		5.0		pF

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: Only one output at a time should be shorted.

Note 4: Input capacitance is guaranteed by periodic testing. F test = 10 kHz at 300 mV, $T_A = 25°C$.

Note 5: All switching parameters measured from 1.5V of input to 1.5V of output. Input pulse amplitude 0V to 3V, $t_r = t_f = 2.5$ ns.

DP8400-4 Switching Characteristics (Note 5)

$V_{CC} = 5.0V \pm 5\%$, $T_A = 0°C$ to $70°C$, $C_L = 50$ pF, unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{DCB16}	Data Input Valid to Check Bit Valid	*Figure 9b*			35	55	ns
t_{DEV16}	Data Input to Any Error Valid	*Figures 10b, 11b*			35	45	ns
t_{DCD16}	Data Input Valid to Corrected Data Valid	*Figure 10b*, $\overline{OB0}$, $\overline{OB1}$ Low			70	85	ns
t_{DSI}	Data Input Set-Up Time Before DLE, CSLE H to L	*Figures 10b, 13d*			−40	−10	ns
t_{DHI}	Data Input Hold Time After DLE, CSLE H to L	*Figures 10b, 13d*		16	10		ns
t_{DSO}	Data Input Set-Up Time Before $\overline{OLE}$ L to H	*Figure 10b*		20	12		ns
t_{DHO}	Data Input Hold Time After $\overline{OLE}$ L to H	*Figure 10b*		20	12		ns
t_{DE0}	E0 Valid After AE Valid	*Figures 9b, 10b, 13d*			20	30	ns
t_{DE1}	E1 Valid After AE Valid	*Figures 9b, 10b, 13d*			12	30	ns
t_{IEV}	DLE, CSLE High to Any Error Flag Valid (Input Data Previously Valid)	*Figure 10b*			60	80	ns
t_{IEX}	DLE, CSLE High to Any Error Flag Invalid	*Figures 9b, 10b*			60	77	ns
t_{ILE}	DLE, CSLE High Width to Guarantee Valid Data Latched	*Figures 10b, 13d*	DLE	25			ns
			CSLE	50			ns
t_{OLE}	$\overline{OLE}$ Low Width to Guarantee Valid Data Latched	*Figure 13d*		25			ns
t_{ZH}	High Impedance to Logic 1 from $\overline{OB0}$, $\overline{OB1}$, $\overline{OES}$	*Figures 9b, 10b*			32	50	ns
	M2 H to L	*Figure 13d*			70	85	ns
t_{HZ}	Logic 1 to High Impedance from $\overline{OB0}$, $\overline{OB1}$, $\overline{OES}$, M2 L to H	*Figures 9b, 10b, 13d*, $C_L = 15$ pF			25	40	ns
t_{ZL}	High Impedance to Logic 0 from $\overline{OB0}$, $\overline{OB1}$, $\overline{OES}$	*Figures 9b, 10b*			30	45	ns
	M2 H to L	*Figure 13d*			70	85	ns
t_{LZ}	Logic 0 to High Impedance from $\overline{OB0}$, $\overline{OB1}$, $\overline{OES}$, M2 H to L	*Figures 9b, 10b, 13d* $C_L = 15$ pF			25	40	ns
t_{PPE}	Byte Parity Input Valid to Parity Error Flags Valid	*Figure 9b*			40	55	ns
t_{DPE}	Data In Valid to Parity Error Flags Valid	*Figures 9b, 13d*			60	75	ns
t_{DBP}	Data in Valid to Byte Parity Output Valid	*Figure 9b*			36	50	ns
t_{MCR}	Mode Change Recognize Time	*Figures 9b, 10b*			60	100	ns

DP8400-4 Switching Characteristics (Continued) (Note 5)

$V_{CC} = 5.0V \pm 5\%$, $T_A = 0°C$ to $70°C$, $C_L = 50$ pF, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{NMR}	New Mode Recognize Time	*Figure 10b*		60	100	ns
t_{CDV}	Mode Valid to Complement Data Valid	*Figure 11b*		55	72	ns
t_{CCV}	Mode Valid to Complement Check Bit Valid	*Figure 11b*		55	72	ns
t_{SCB}	Syndrome Input Valid to Check Bit Valid	*Figure 13d*		28	41	ns
t_{SEV}	Syndrome Input Valid (CGL) to Any Error Valid	*Figure 13d*		25	39	ns
t_{SCD}	Syndrome Inputs Valid to Corrected Data Valid	*Figure 13d*		55	75	ns
t_{DSB}	Data Input Valid to Syndrome Bus Valid	*Figure 13d*, $\overline{OES}$ Low		45	58	ns
t_{CSB}	Check Bit Inputs Valid to Syndrome Bus Valid	*Figure 13d*, $\overline{OES}$ Low		40	51	ns
t_{CEV}	Check Bit Inputs Valid (PSH) to Any Error Valid	*Figure 13d*		35	45	ns
t_{CCD}	Check Bit Input Valid (PSH) to Corrected Data Valid	*Figure 13d*		70	82	ns
t_{DCB32}	Data Input Valid to Check Bit Valid	*Figure 13d*		63	96	ns
t_{DEV32}	Data Input Valid to Any Error Valid	*Figure 13d*		60	94	ns
t_{DCD32}	Data Input Valid to Corrected Data Out	*Figure 13d*, $\overline{OB0}$, $\overline{OB1}$ Low		125	157	ns

Note 1: "Absolute Maximum Ratings" are the values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: Only one output at a time should be shorted.

Note 4: Input capacitance is guaranteed by periodic testing. F test = 10 kHz at 300 mV, $T_A = 25°C$.

Note 5: All switching parameters measured from 1.5V of input to 1.5V of output. Input pulse amplitude 0V to 3V, $t_r = t_f = 2.5$ ns.

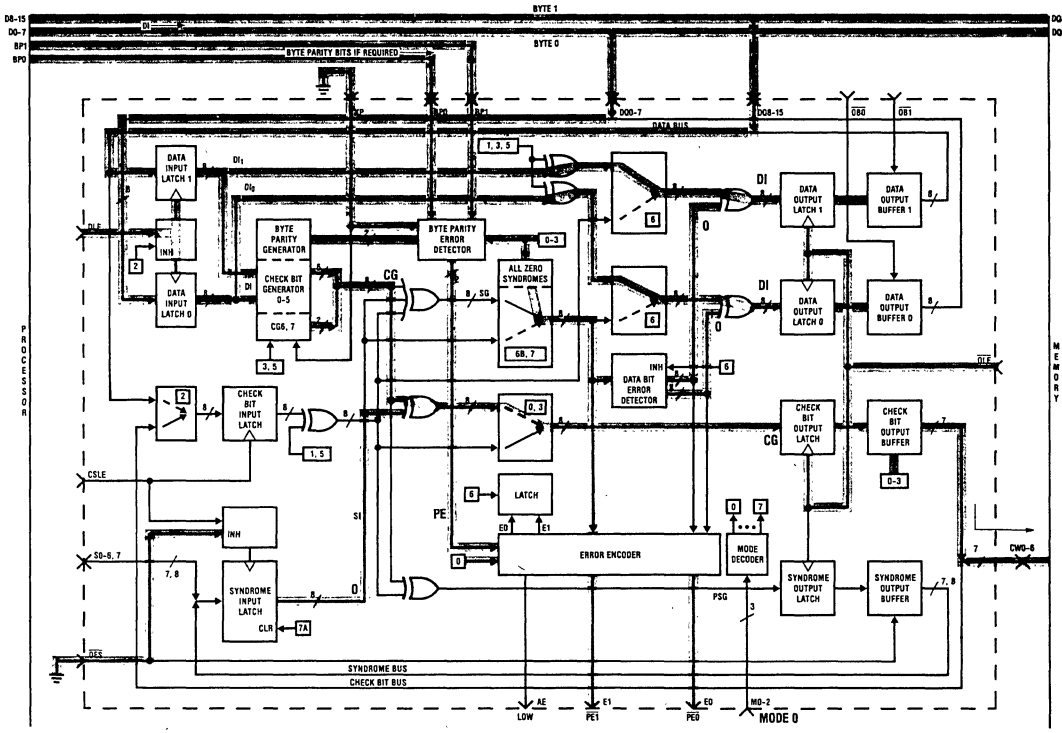


FIGURE 9a. DP8400 16-Bit Configuration, Normal WRITE with Byte Parity Error Detect If Required

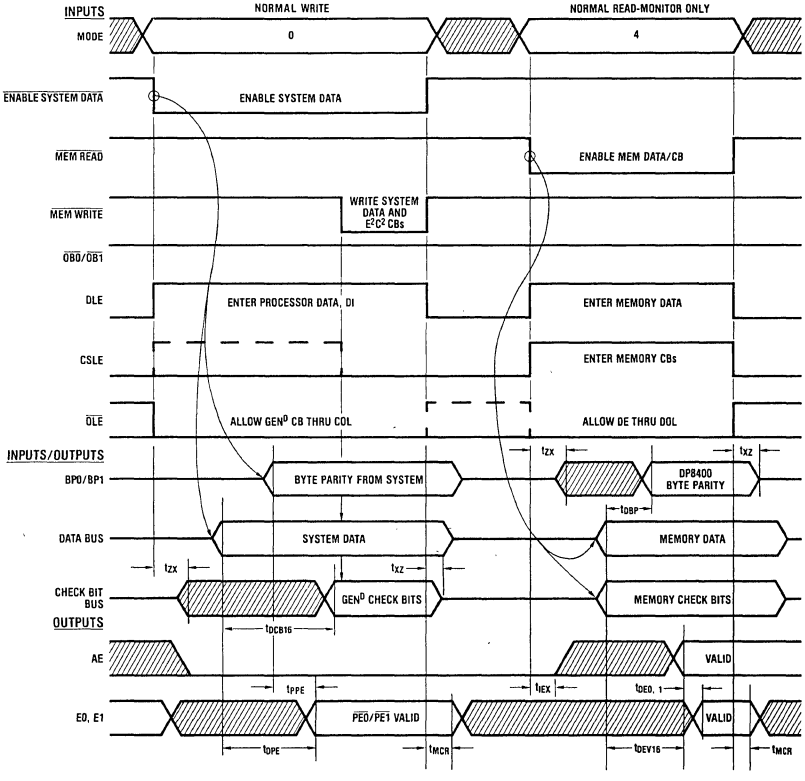


FIGURE 9b. DP8400 16-Bit Configuration, Normal WRITE and Normal READ Timing Diagram

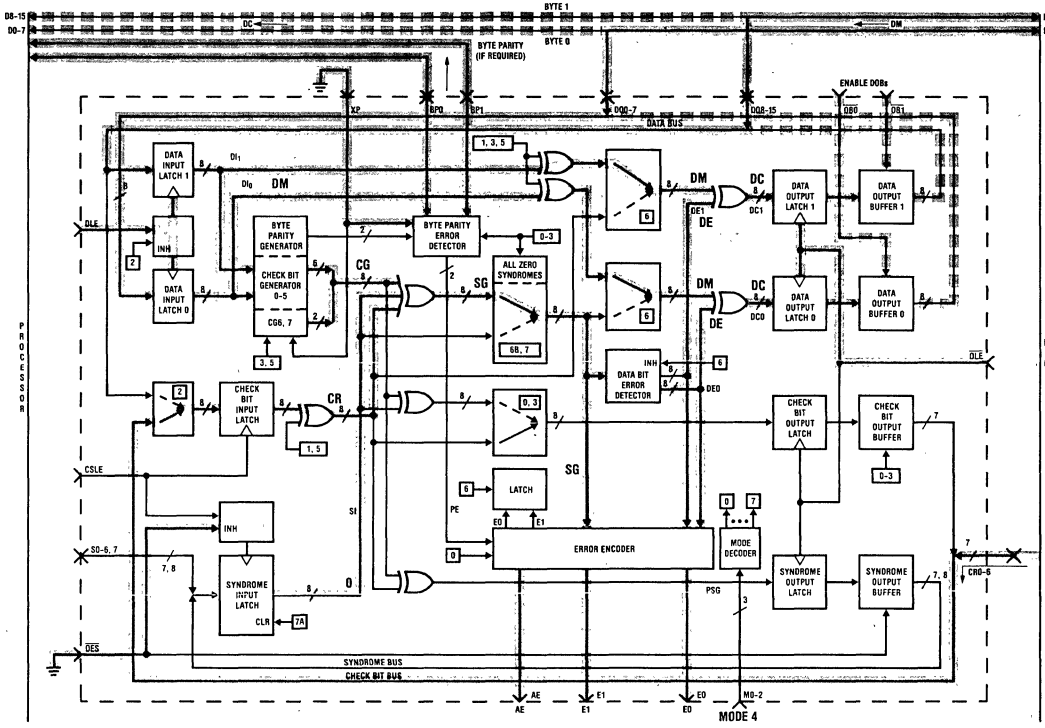
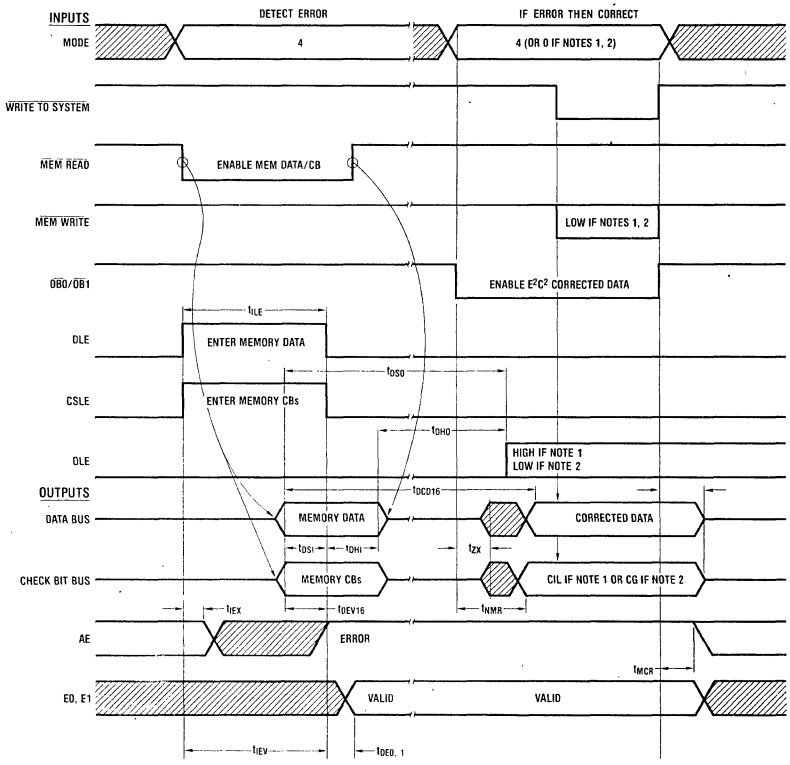


FIGURE 10a. DP8400 16-Bit Configuration, Normal READ — Detect Error (And Correct if Required---)



Note 1: If rewriting correct data and CBs to same location and single data error was detected.

Note 2: If rewriting correct data and CBs to same location and single check bit error was detected.

FIGURE 10b. DP8400 16-Bit Configuration, DETECT THEN CORRECT Timing Diagram

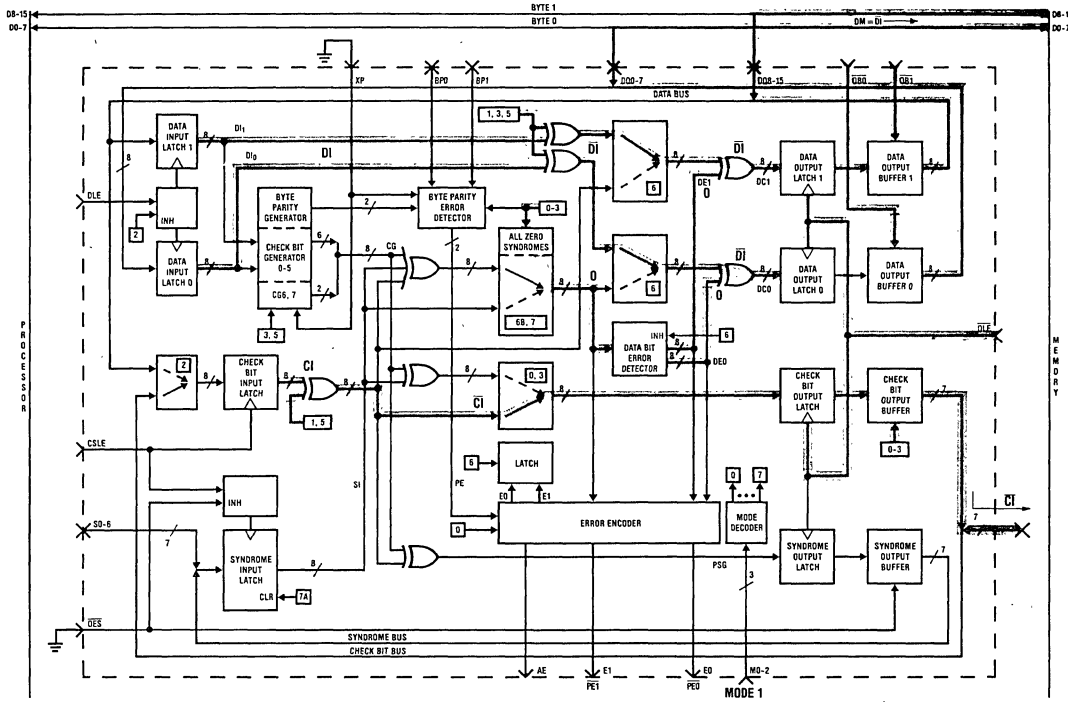
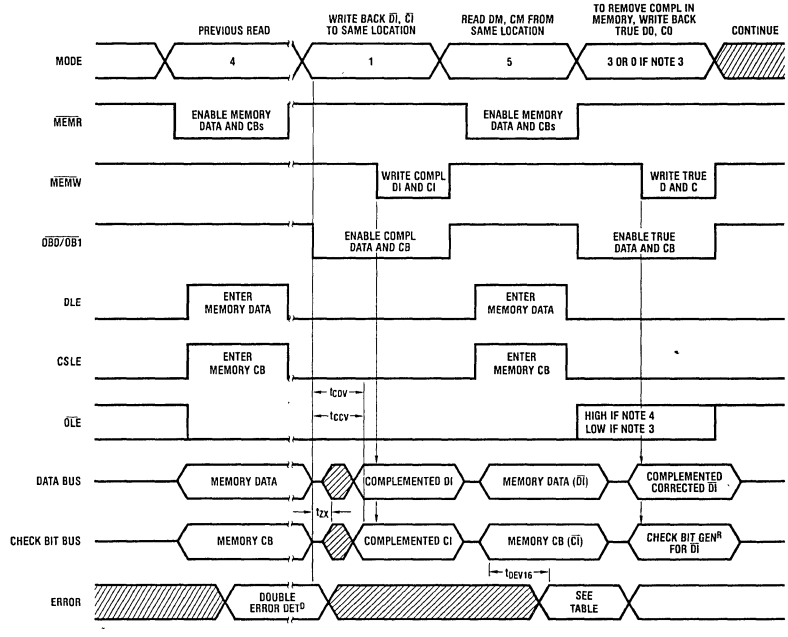


FIGURE 11a. DP8400 16-Bit Configuration, COMPLEMENT WRITE



Note 3: If rewriting corrected data and CBs back to same location and 1 soft data bit error was detected.

Note 4: If rewriting corrected data and CBs back to same location and 2 hard errors or 1 soft check bit was detected.

FIGURE 11b. DP8400 16-Bit Configuration, Detect 2 Errors, COMPLEMENT WRITE, COMPLEMENT READ, Output Corrected Data Timing Diagram

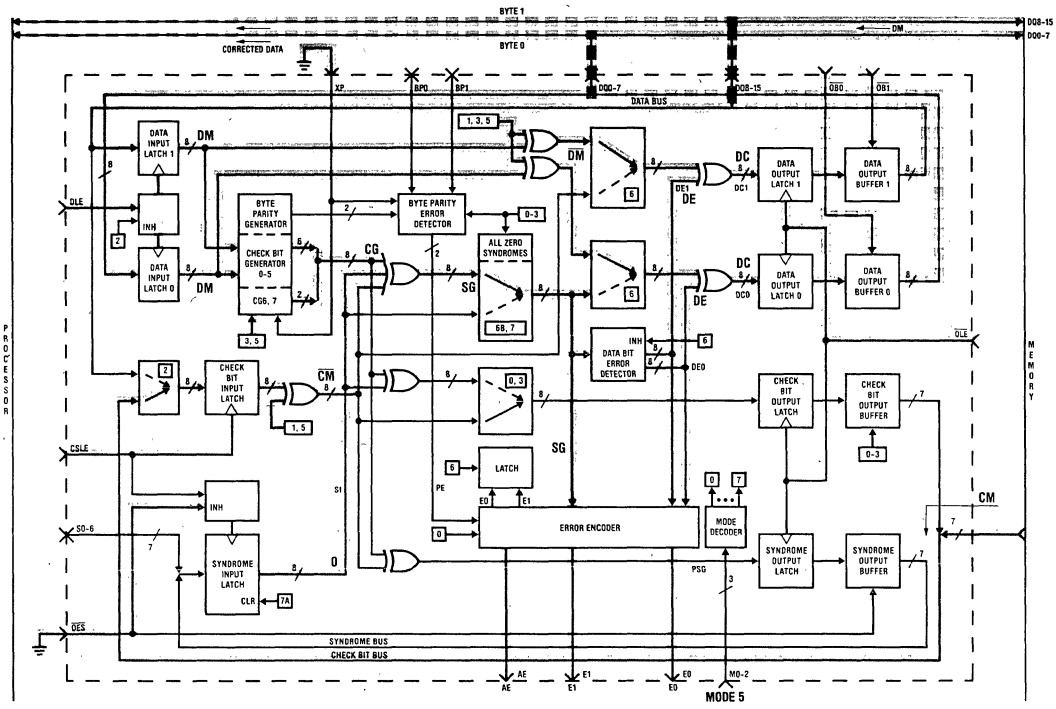


FIGURE 11c. DP8400 16-Bit Configuration, COMPLEMENT READ and Output Corrected if One or Two Hard Errors (---)

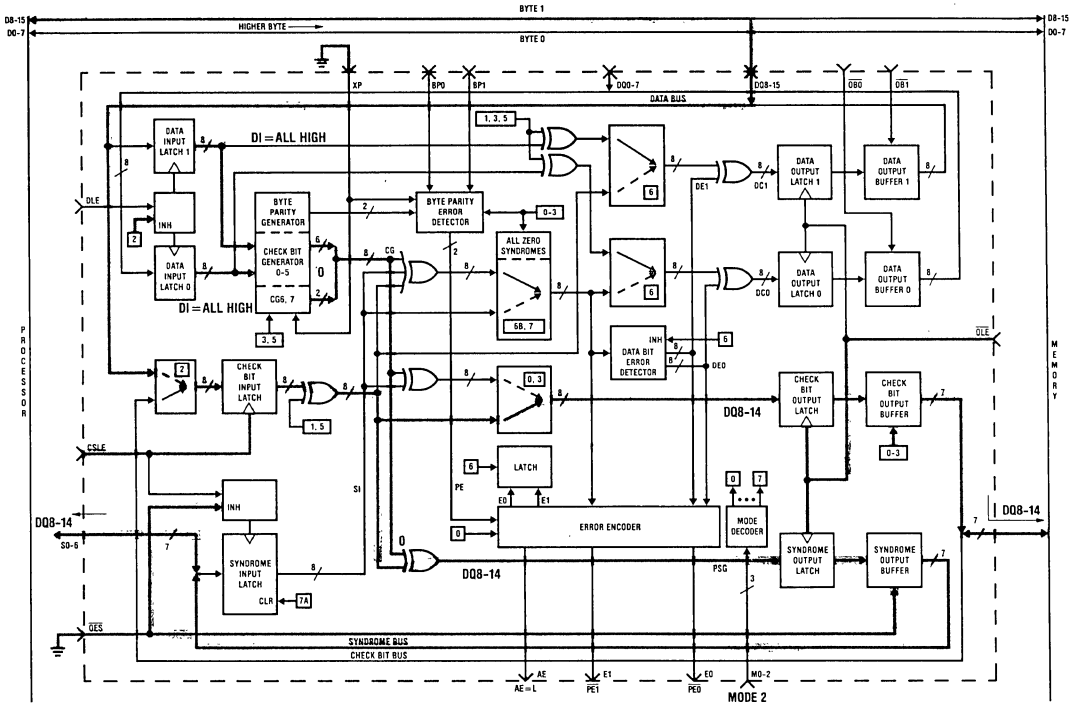


FIGURE 12a. DP8400 16-Bit Configuration, Diagnostic WRITE, READ. Data Bus to Check Bit Bus or Syndrome Bus (Providing DI = HIGH in Previous Cycle to Set CG = All Zero For Transfer to S).

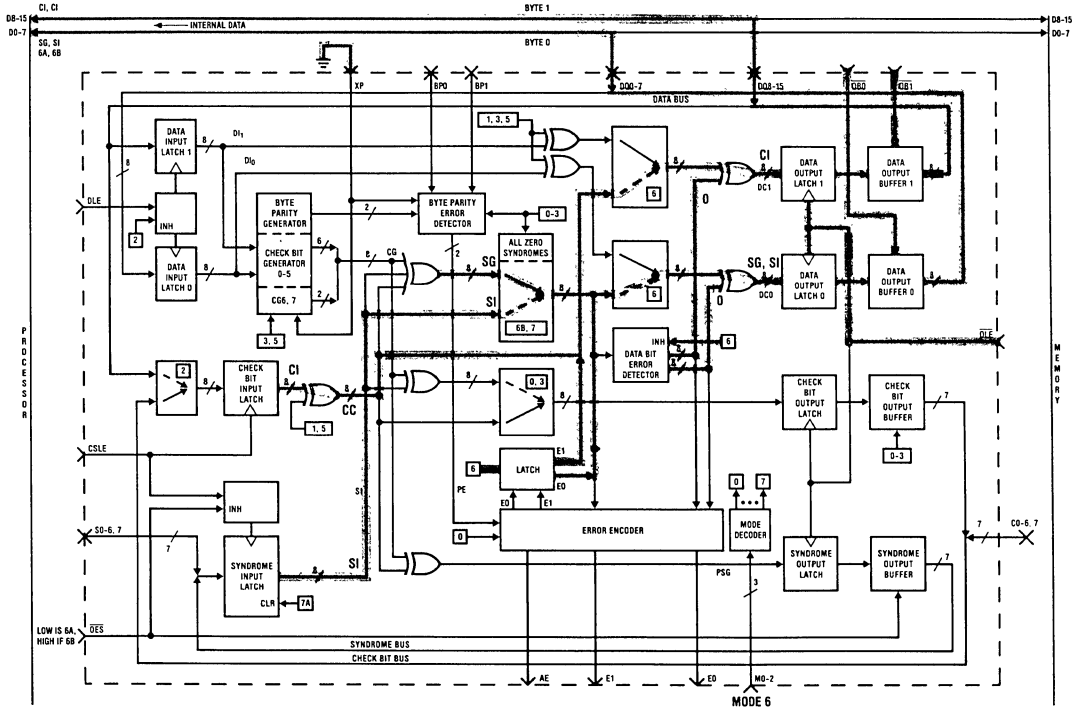
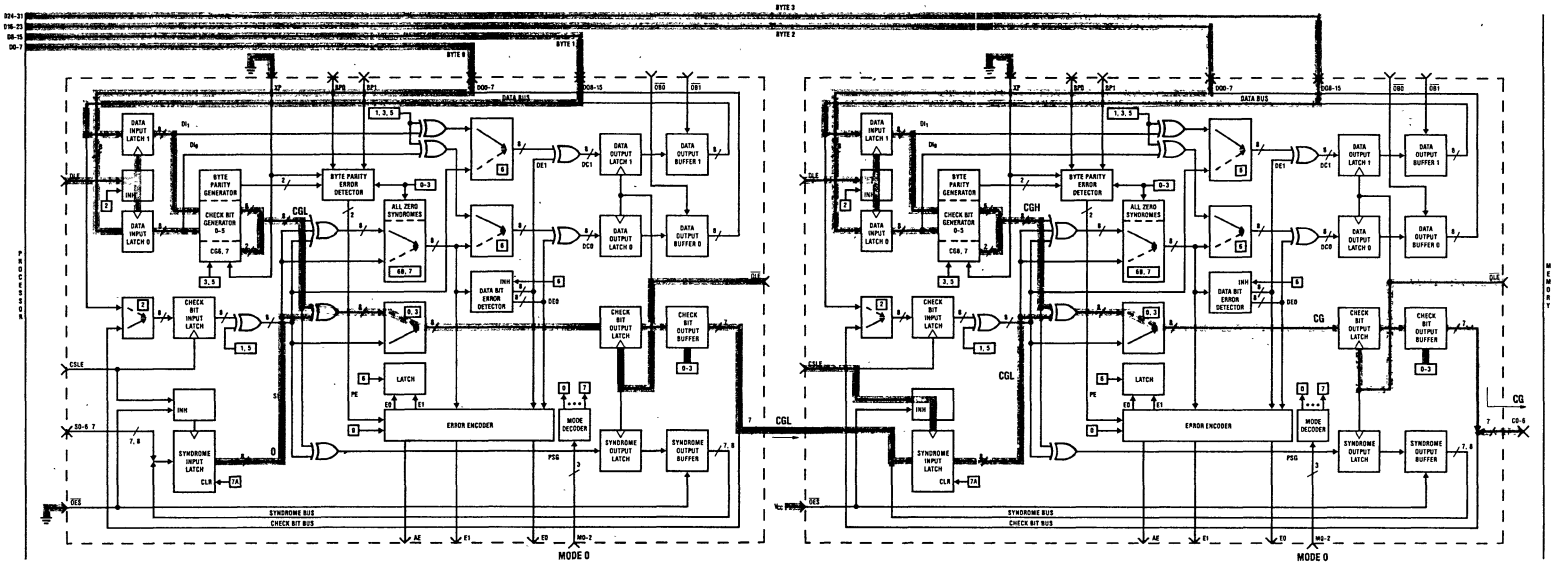
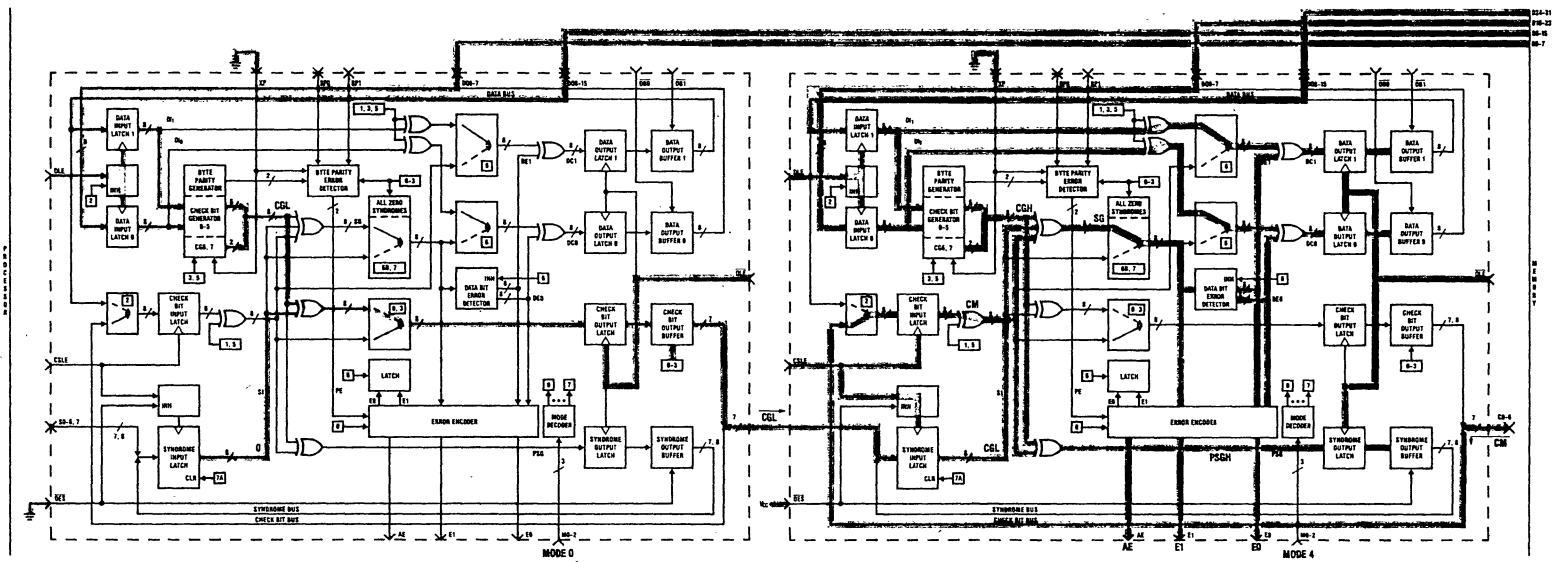


FIGURE 12b. DP8400 16-Bit Configuration, Monitor on Data Bus — Memory Check Bits



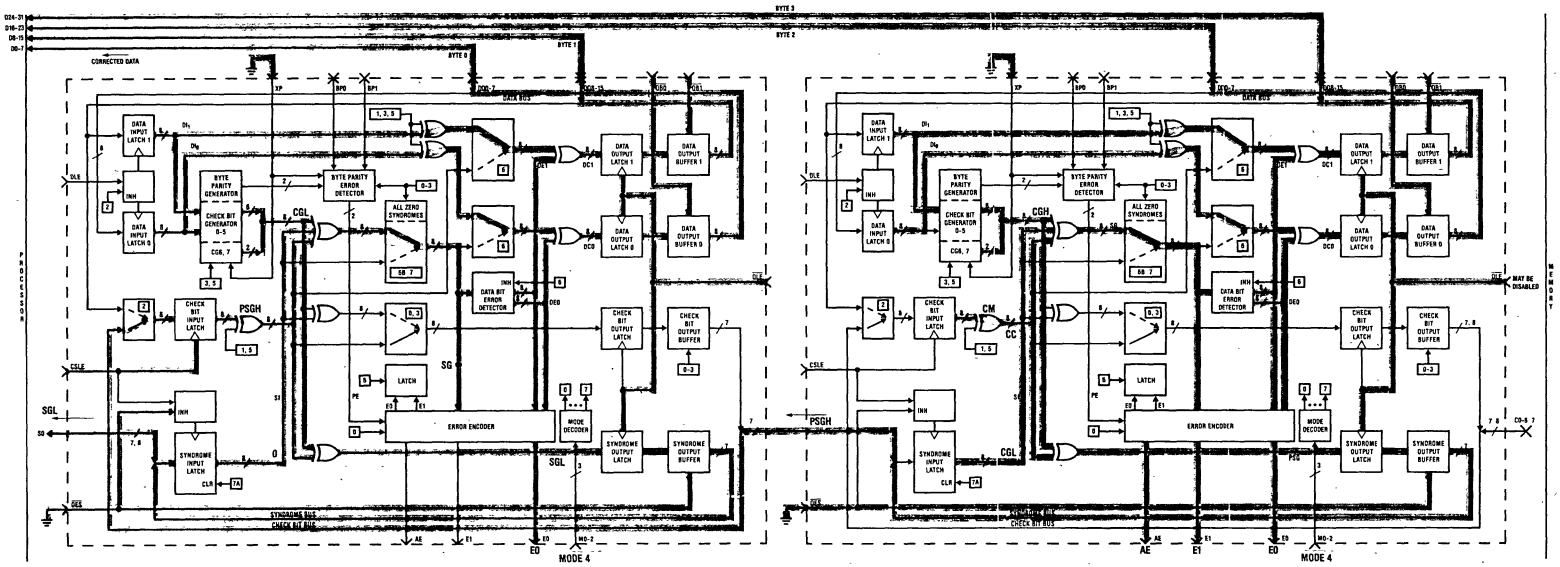
DP8400 (L) DP8400 (H)

FIGURE 13a. DP8400 32-Bit Configuration, WRITE



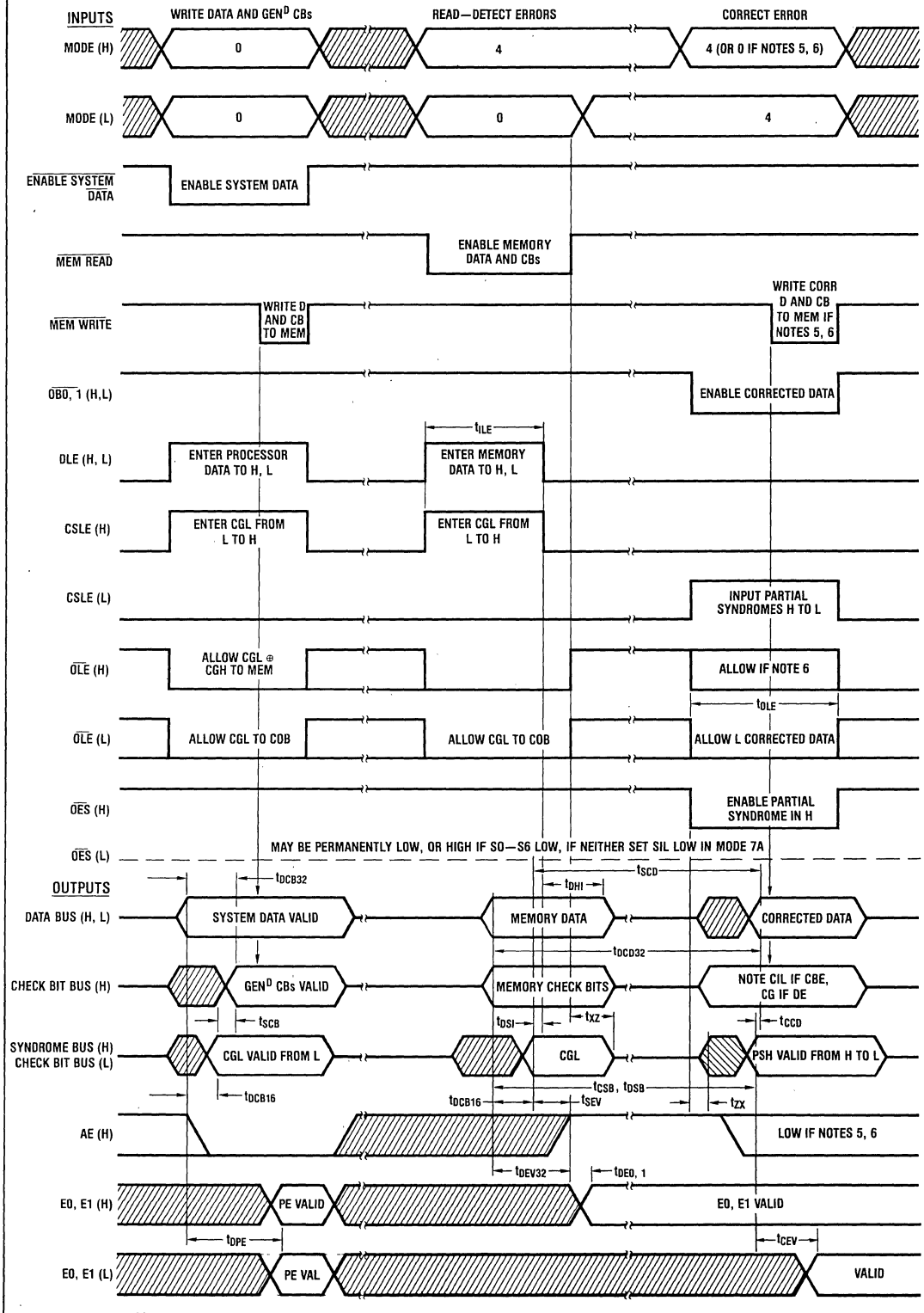
DP8400 (L) DP8400 (H)

FIGURE 13b. DP8400 32-Bit Configuration, READ Detect Error Only



DP8400 (L) DP8400 (H)

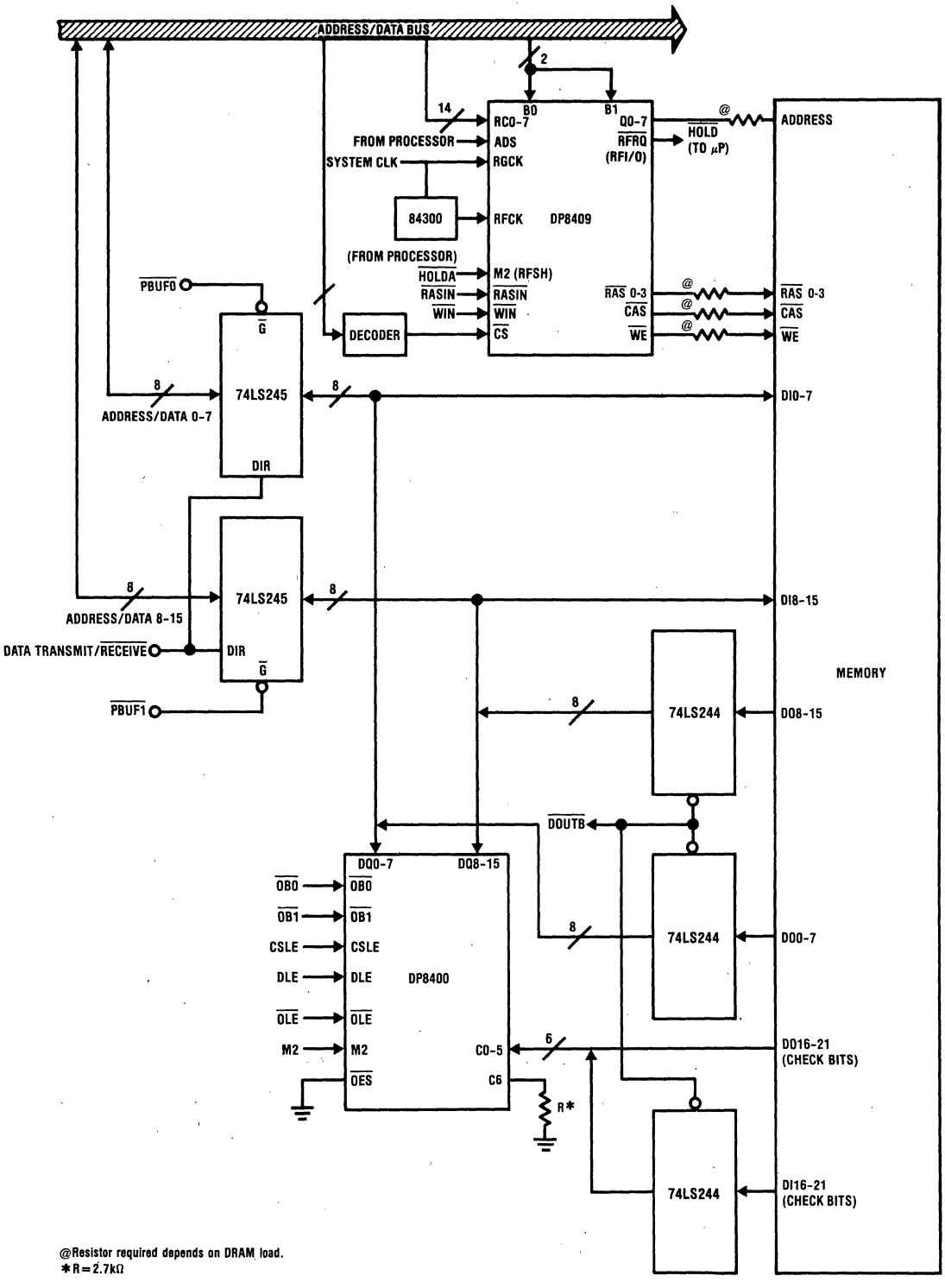
FIGURE 13c. DP8400 32-Bit Configuration, READ Correct Data



Note 5: If rewriting corrected data and CBs back to same location and single data error was detected.

Note 6: If rewriting corrected data and CBs back to same location and single check bit error was detected.

FIGURE 13d. DP8400 32-Bit Configuration, WRITE, DETECT and CORRECT Timing Diagram



@Resistor required depends on DRAM load.
*R = 2.7kΩ

FIGURE 14a. DP8400/8409 System Interface Block Diagram (See Figure 14b for Byte Write Control Timing)

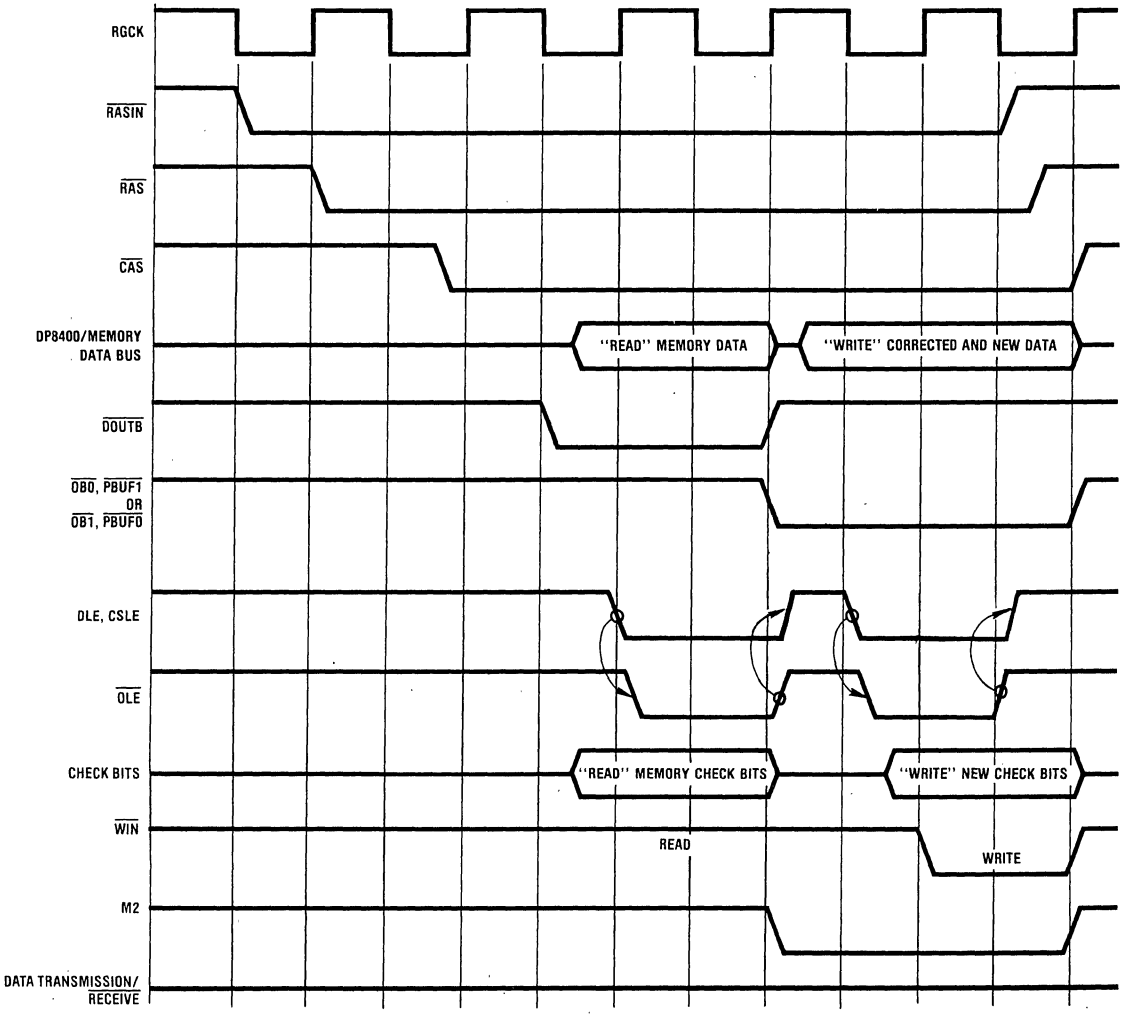


FIGURE 14b. DP8400 16-Bit Configuration, Byte Write Timing

Expanding the Versatility of the DP8400

National Semiconductor
Application Note AN-306
June 1982
Mike Evans

Basic Operation of the DP8400

Introducing error correction capabilities to a memory incurs some penalties—extra memory, additional access times, and extra control circuitry. The DP8400 has been designed to minimize the last two, and for some data word widths, less extra memory is required than for other error correction circuits.

In systems using error correction, extra memory is needed for check bits, which are merely parity bits, each derived from different combinations of the data bits. If a single error does occur, the error correction circuit can determine which bit is in error and then complement that bit, to re-create the original data word. As the memory data word widens, the ratio of check bits to memory data bits is reduced. As a rough guide, starting with four data bits and four check bits, one additional check bit is required each time the data word doubles.

A circuit diagram of how the DP8400 generates the check bits in a write cycle and corrects errors in a read cycle is shown in *Figure 1a*, which uses four data bits and four check bits. A 4-bit example is shown in *Figure 1b*. In a write cycle, the data input latch, DIL, receives the system data and generates four parity bits or check bits, which pass through the check bit output latch, COL, and buffer, to be written to the selected memory location with the system data. This delays every write cycle, but fortunately the DP8400 takes only 30 ns extra to generate the (six) check bits. When this location is subsequently read, the four memory data bits pass through DIL to generate four new checks bits. The four memory check bits pass through the check bit input latch, CIL, and are fed into four Exclusive-OR gates with the four generated check bits. The outputs of these gates are called syndrome bits, and obviously, if there are no errors, the two sets of check bits will be the same and no syndrome bits will go high. If there is an error in the check bits, only the corresponding syndrome bit will go high; in this case the data bits are still correct. If one of the data bits is in error, three syndrome bits will go high (in the case of DP8400, three or five will go high), and the syndrome word is unique for any of the bits in error. The four AND-gates decode which bit is in error and complement it out of the second set of Exclusive-OR gates. The other three output bits remain the same as the input bits, so the corrected word is now available to the system.

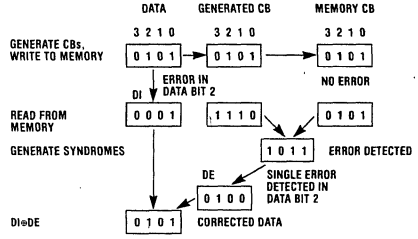


Figure 1b. Example of Single Error Correction

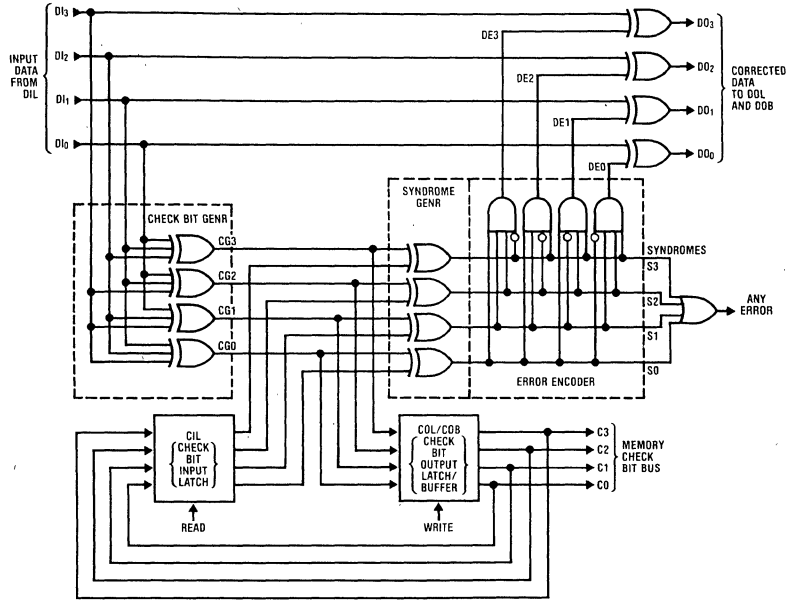


Figure 1a. Error Correction 4-Bit Functional Diagram

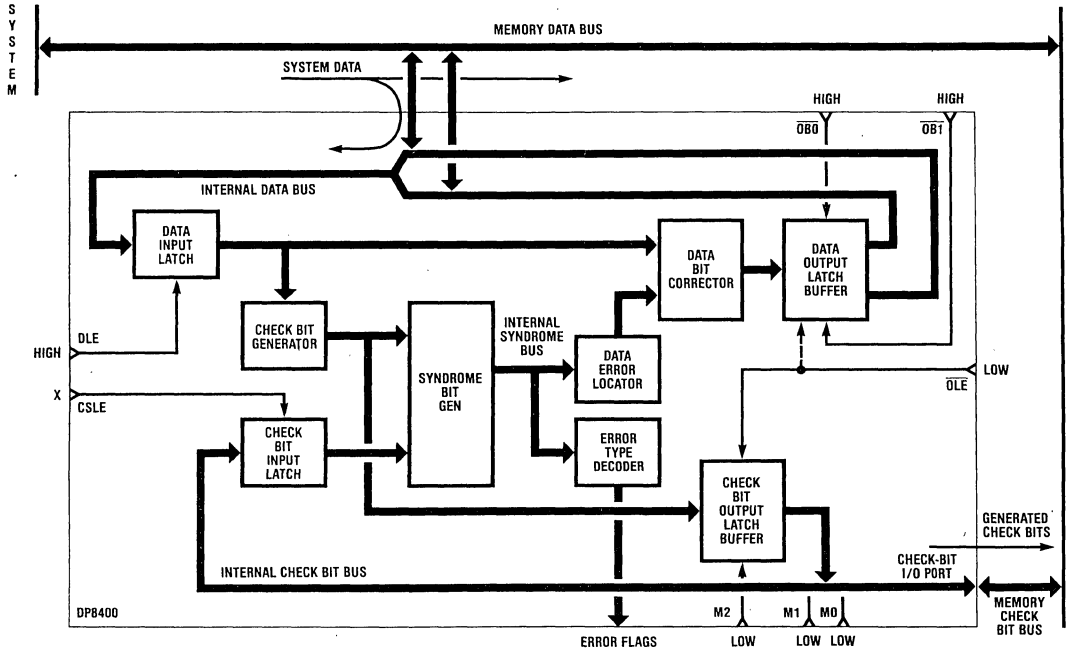


Figure 2a. DP8400 Read From Memory Cycle

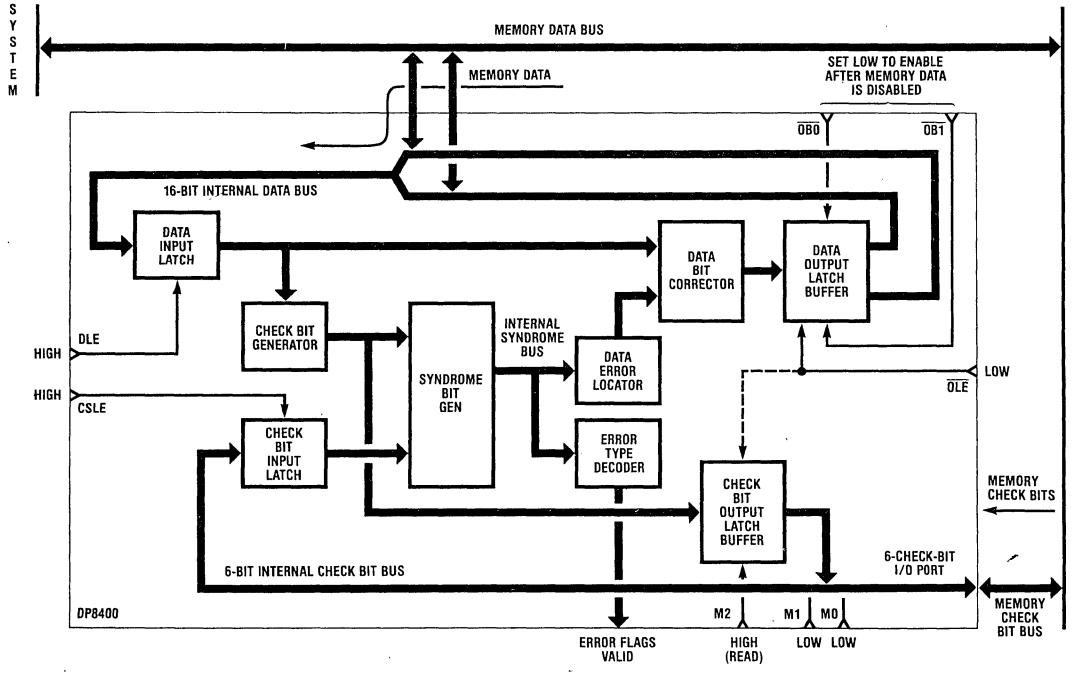


Figure 2a. DP8400 Write to Memory Cycle

In the case of the DP8400 with 16 data bits and 6 check bits, there are 16 AND-gates to decode the 6 syndrome bits to determine the data bit in error. Table 1 shows the DP8400 matrix, called a Nelson Code, which has some unique features concerned with double soft error correction. For the purposes of this description, the matrix may be considered to be a form of Modified Hamming Code. The matrix has two functions: horizontally it tells us the value of the generated check bits for any data word when writing to memory, and vertically it tells us the syndrome word for any data bit in error. In a write cycle to memory, a '1' in any row indicates that the data bit in that column helps generate the parity bit in that row. For example, check bit 1 checks the parity of data bits 3, 6, 8, 9, 11, 13, 14 and 15, and generates even parity for those data bits. In a read cycle from memory, three or five of the six syndrome bits will go high for a single data bit error, and the columns represent the syndrome word, so the data bit in error is the number at the top of the column for that syndrome word. The 16 AND-gates each decode one of the 16 syndrome words shown in the columns of Table 1, to locate the error. If there is a data bit error, one of the outputs of the 16 AND-gates will go high, to complement the data bit in error.

If two errors have occurred, the syndrome word is simply the Exclusive-OR of the syndrome words of the two individual bits in error, whether data or check bits, and is always even parity. First, if two check bits are in error, the corresponding two syndrome bits will go high. Second, for one data bit and one check bit error, then either two, four or six syndrome bits will go high. Finally, if two data bits are in error, again two, four or six syndrome bits go high. Thus a parity check on the syndromes will indicate any two errors. This is important because if we know there are two errors, the DP8400 can attempt to correct them. The third error flag, E1, is the parity of the syndrome bus and check bit error. The DP8400 provides three error flags AE (Any Error), E0 and E1, as shown in Table 2, so that the exact nature of the error can be determined.

Configuration and Control of the DP8400

The DP8400 has a 16-bit data I/O port and an 8-bit check bit I/O port (6 bits used with 16 data bits) for applications with memories used with 16-bit microprocessors. The 16-bit data I/O port sits on the memory data bus, and the 6 check bit I/O port connects directly to the check bit section of memory. In other words, each memory location now contains 16 data bits with 6 check bits. The DP8400 is expandable to beyond 80 data bits, each additional 16 data bits requiring an additional DP8400 without the need for extra logic circuitry. 32-bit wide memory busses are also a popular width for minicomputers. In addition, 16-bit microprocessor systems may use 32-bit memory, because this larger memory data width requires only 7 check bits, a lower percentage overhead of check bits to data bits.

Figures 2a and *2b* show a simplified block diagram of the DP8400 with its control signals. The numerous control signals provide ease of use in the many varied applications of this chip. There are three latch enable signals DLE, CSLE and $\overline{\text{OLE}}$. Whenever DLE is high, data on the data I/O port D0-15 is entered into the data input latch DIL, and is latched in as DLE goes low. This allows either processor or memory data to be present on the data bus for only 3ns prior to, and held over for 10ns after DLE goes low. The data can then be removed if desired. Similarly, CSLE, when high, allows check bits on the check bit I/O port and external data on the syndrome I/O port to enter the check bit and syndrome input latches (CIL and SIL), respectively. These are latched in as CSLE goes low. (In 16-bit operation, $\overline{\text{OES}}$, Output Enable Syndromes, will be set low permanently, inhibiting CSLE to SIL, which remains in the power-up reset condition so that it does not affect the simplified block diagram.) $\overline{\text{OLE}}$, when set low, allows internal information into the data and check bit output latches (and the syndrome output latch, not shown). As $\overline{\text{OLE}}$ goes high, this information becomes latched. For some less complex designs, DLE, CSLE and $\overline{\text{OLE}}$ may be linked together. Providing $\overline{\text{OLE}}$ was low to allow corrected data into DOL, then $\overline{\text{OB0}}$ and $\overline{\text{OB1}}$, when set low, enable the two data output buffers to present corrected data to the system. Data is enabled or disabled within 15ns of these inputs going low or high, respectively.

The DP8400 has three mode pins, M2, M1 and M0, which offer eight major modes of operation, designated 0 to 7. The most important two are Normal Write and Normal Read, and for these M1 and M0 are set low. M2 is READ/$\overline{\text{WRITE}}$ so Normal Write is mode 0 and Normal Read is mode 4. Other modes are used for the Double Complement Correct approach (Modes 1, 3 and 5) and for diagnostics (Modes 2 and 6). Mode 7 is used when expanded to more than 16 data bits and fast correction times are required.

Normal Operation With a 16 Data Bit Memory

The basic requirements for normal operation of the DP8400 are that it generate check bits, detect errors and correct them with minimum delays, and that it be easy to use. In normal operation M1 and M0 are set low. *Figure 2a* shows how the DP8400 generates check bits when writing data to memory. DLE may be kept high, $\overline{\text{OLE}}$ low, CSLE low, and M2 low so that the DP8400 is in Mode 0. System data is presented to the data I/O port on pins D0-15, and enters DIL, where it connects to the check bit generator CG. The six generated check bits pass through COL and are enabled (with M2 low) onto the check bit I/O port. The six generated check bits will appear 30ns after the 16 data bits are presented to the data I/O port. A write to memory will now store the 16 data bits and 6 corresponding check bits in the selected location of memory. The write cycle is therefore slowed down by 30ns, which in most memory systems is not significant.

Figure 2b shows the paths when reading from memory, with DLE set high to enter the memory data bits into DIL, and CSLE also set high to enter memory check bits into CIL. M2 is set high so that the DP8400 is in Mode 4. The Any Error flag, AE, becomes valid 35ns after memory data and check bits are valid. Error flags E1 and E0 become valid approximately 15ns later. Thus, if AE is low, no further operations are necessary. For fast 16-bit microprocessor systems, it may be necessary to introduce a wait state every read cycle to first determine if an error exists. If no error is detected the wait state is removed and the read cycle continues.

If an error is detected, then the error flags E1 and E0 must be examined to determine the required action. If

the error is a single data bit error, DOL will by now contain corrected data. If there is no check bit error, then COL, which follows CIL when in Mode 4, now contains the original check bits. By taking $\overline{OLE}$ high, corrected data bits are latched in DOL, and correct check bits in COL. The memory is now disabled, so that $\overline{OB0}$ and $\overline{OB1}$ can be set low to enable corrected data onto the data bus, and M2 set low to enable the contents of COL onto the check bit bus. A write to the same location of memory will therefore remove the data bit error if it was a soft error. The microprocessor can read the corrected data once the wait signal is removed.

If the error is a single check bit error, DLE should be set low. DOL contains the contents of DIL, still correct data. Memory can now be disabled so that $\overline{OB0}$ and $\overline{OB1}$, when set low, output correct data, and M2 when set low, allows the generated check bits from DIL to be output on the check bit I/O port. A write to the same location of memory will remove the check bit error if it was a soft error. The microprocessor now reads this correct data when the wait signal is removed. If a double bit error is detected, then other approaches may be taken, as described in the data sheet and later in this application note.

The primary features of the DP8400 are discussed in the data sheet; there are, however, a number of other features that become very useful once a designer becomes acquainted with error correcting techniques. These include: expansion beyond 16 data bits, diagnostic routines, error logging (allowing some double error correction), and a novel approach offering fast correction of any double error. This application note discusses how the DP8400 has been designed to function in all of these applications, making it the most versatile and comprehensive error correction chip available.

Error Checking and Correcting for Wider-Than-16-Bits Data Widths

At present, most 16-bit microprocessor systems use a 16-bit wide main memory, partly for simplicity, and also because main memories, in general, have not become large enough in size to justify otherwise. The data sheet shows how to accomplish this with one DP8400, utilizing the matrix of Table 1. It is fairly easy to use a memory of twice the microprocessor data width to reduce total chip count when incorporating error correction capability. One example would be a complex 8-bit microprocessor using large main memory. If the memory data width is kept at eight bits, then five check bits are required for error correction for each byte of data. If four banks of memory are required, each bank comprising 13 chips, then 52 total memory chips are required and only 62% of the memory is used for system data. If the memory data width is increased to 16 bits for the same microprocessor-based system, then six check bits are required.

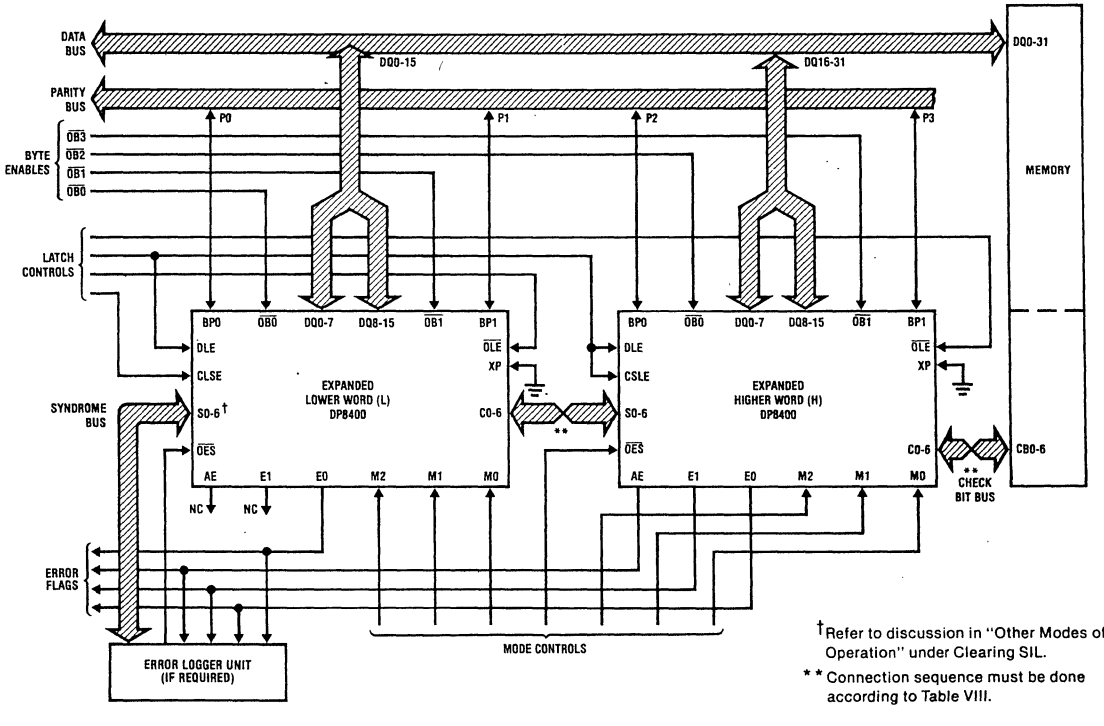


Figure 3. 32-Bit Error Detection and Correction

The memory now comprises two banks each of 22 chips, totaling 44 memory chips—a savings of eight memory chips. This saving is offset somewhat by the need to incorporate byte-writing capability, which does require extra components and slows down the memory write cycle. One DP8400 is still needed, using all 16 bits, and two bidirectional buffers are also required.

As a second example, using a 16-bit microprocessor with a memory of eight banks, each comprising 16 bits of data and six check bits, the total is 8 x 22 or 176 memory chips. Once the memory is widened to 32 data bits with seven check bits, only four banks are required, and the total number of memory chips reduces to 4 x 39, or 156—a savings of 20 memory chips. This is offset a little by the fact that an extra DP8400 is required, and slightly slower memory write and read cycles are necessary. In some cases, therefore, widening the memory data bus becomes more practical for larger memories.

Saving memory chips is just one reason why there is a need to be able to expand the DP8400 beyond 16 data bits. Most minicomputers now use 32-bit wide data busses, and soon there will be some 32-bit microprocessors. Other systems use 24 bits, 48 bits, 52 bits, 64 bits or a variety of other data widths. The DP8400 has been configured to be expandable to any data width, even beyond 80 bits, merely by inserting an additional DP8400 for each 16-bit increment in memory data.

A section of the chip shown in the data sheet Block Diagram comprises the syndrome input and output latches, SIL and SOL, and a dedicated syndrome I/O port. This port has a number of uses not normally needed in simple 16-bit single error correction applications.

One use of this syndrome port is for data widths wider than 16 bits. Only one DP8400 is required with 16 data bits or less, but if a system uses more than 16 memory data bits, additional DP8400s are required. For example, two DP8400s, one with its 16-bit data port connected to the lower word, and the other to the higher word, can be configured to generate check bits, and detect and correct errors for a 32-bit memory as shown in *Figure 3*. For writing to memory, both chips will still generate six check bits from the two words of 16 bits. But with more than 26 total data bits, seven check bits are required. Therefore, it is necessary to combine the two sets of check bits to produce seven composite check bits to be written to memory as shown in the flow path depicted in *Figure 4a*. This is achieved by outputting the six generated check bits from the lower word DP8400 (designated L), and inputting them to H, the higher word DP8400. The syndrome port of H is available to receive these check bits from L, to be loaded into SIL of H, provided CSLE is high. The six outputs from SIL combine with the six check bits generated in H to create seven composite check bits, and this 7-bit combination is output on the check bit port to the memory check bits. Table 2 shows one of twelve possible ways to combine the two sets of check bits. Note that the lower word matrix for bits 0 and 15 is identical to Table 1 with the addition of all "0"s for the seventh check bit. The higher word matrix for bits 16 to 31 uses the same rows but in a different order, implying that the check bits from L must be cross-connected to H. For example, memory check bit 5 is generated from check bit 1 of L and check bit 5 of H. Both chips are therefore set to normal write mode when generating check bits.

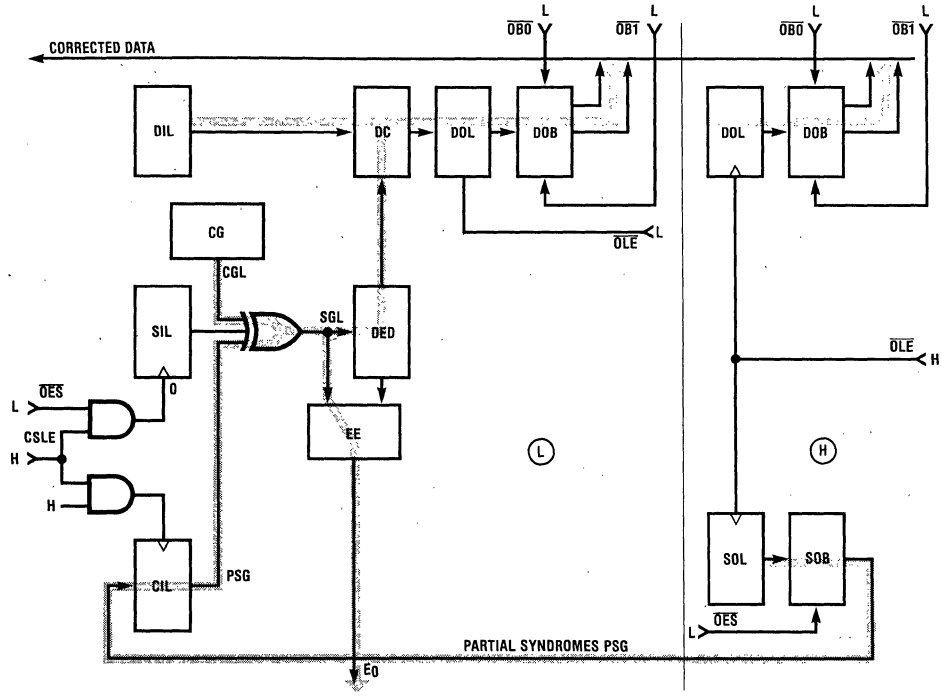


Figure 4a. E²C² 32-Bit Configuration, Error-Correct Flow Path

When reading from memory, the two chips first need to detect for an error. *Figure 4b* shows the flow path through the chips. L is set to normal write mode and H to normal read mode. Memory data is supplied to both chips so that L generates six check bits from the lower word data bits, and feeds them to SIL of H, the same as for writing. H also generates its own check bits which combine with those from L, and these seven composite check bits are compared with the seven memory check bits fed into CIL of H. This combining, plus comparison of check bits, is equivalent to seven 3-input Exclusive-OR gates. The output of these Exclusive-OR gates are the seven syndrome bits, and these can be decoded to determine the type of error. First, if there is no error, error flag AE of H will remain inactive because memory data is correct, provided $\overline{OLE}$ is kept low, and DOL of both L and H will contain correct data. Second, if there is a memory check bit error, only one of the seven syndromes will go high and the three error flags of H will indicate a check bit error as in Table 3. Note that memory data is still correct, and with $\overline{OLE}$ low, DOL of both L and H contain correct data. Third, if there is a single data error in bits 16-31, the syndromes of H are such that the data error locator will locate the error and correct it, so again DOL of both L and H contain correct data. This is because the seventh syndrome bit is low for an error in the higher word, so that we have a six syndrome bit word as in Table 1, to be decoded as normal to correct the error. In each of these three cases, DOL of both L and H contained correct data, and the common condition for these is either that AE(H) is "0", or E1(H) is "1".

The fourth case is more complex. In the previous three cases, correct data has been available in both DOL about 50ns after memory data became valid. Now with a single data error in bits 0-15, AE(H) is a "1", EI(H) a "1", and EO(H) a "0", but L does not have sufficient information to locate the error. It is first necessary to feed back the partially generated syndromes of H back to L, and this is achieved by reversing the direction of the common bus. First L is placed in normal read mode so that L's generated check bits become disabled. Next, the partial syndromes in H are enabled onto the bus by setting $\overline{OES}$ of H low, so that its syndrome I/O port outputs the combined Exclusive-OR of CG(H) and CIL(H), which is transferred to CIL of L. These partial syndromes then combine with CG(L) to generate valid syndrome bits in L, demonstrated by the flow path of *Figure 4c*. If there is, in fact, a data bit error in bits 0-15, the seventh syndrome bit will go low, allowing the remaining six bits to be decoded to locate the error as per the columns of Table 2. This switching around of the common bus, therefore, takes more time to correct the error in L, equivalent to a total time of approximately 100ns. The fifth kind of error is identified as a double error. In this case, the error flags indicate the double error and the system can take the necessary action.

A logical approach when using two DP8400s would be to first see if there is any need to reverse the common bus by monitoring AE(H), and when it is low, to output directly from DOL of both chips by setting $\overline{OB0}$ and $\overline{OB1}$ of each low. The System Data Valid flag should be set active at this time. If the AE(H) output is high and the error flags do not indicate a double error, then the common bus should be switched around and the System Data Valid signal set true. If the error is a double error, the user may utilize a number of alternatives, including the Double Complement Correct method.

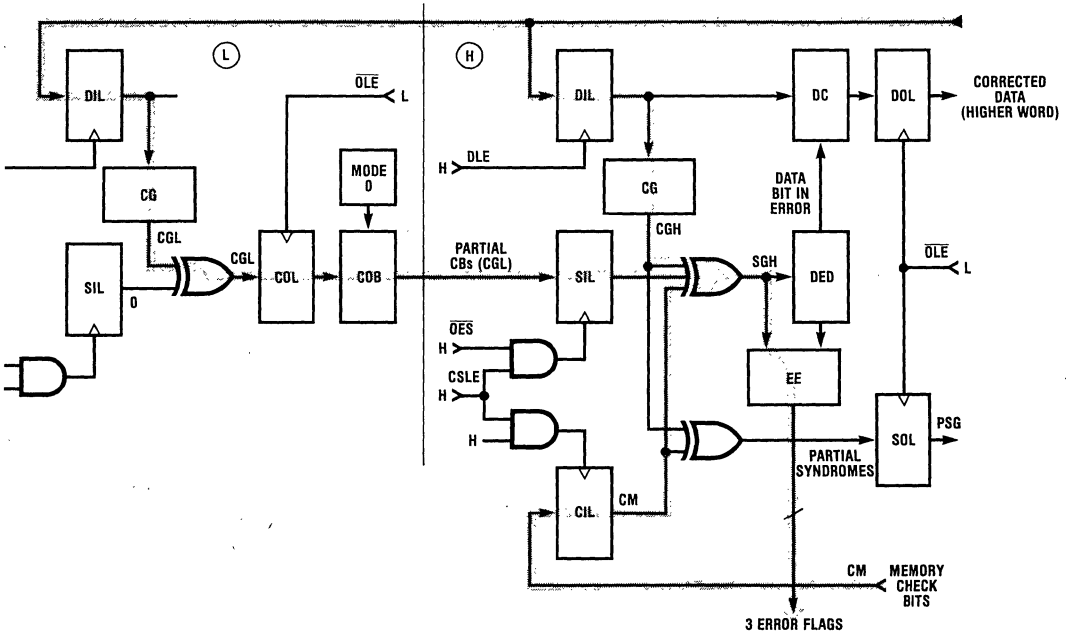


Figure 4b. E²C² 32-Bit Configuration, Detect Flow Path

Table 1. Data In to Check Bit Generate, or Data Bit Error to Syndrome-Generate Matrix (16-Bit Configuration)

		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
		GENERATE CHECK BITS																DQ0-15
GENERATED SYNDROMES	0	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0
	1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	1
	2	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	2*
	3	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	3*
	4	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	4
	5	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	5
		4	8	9	7	5	1	3	9	E	B	D	3	C	7	F	F	0
		3	3	2	0	2	3	2	1	3	0	0	1	2	3	2	1	1
		HEXADECIMAL EQUIVALENT OF SYNDROME BITS																

GENERATED CHECK BITS

*C2, C3 generate odd parity.

Table 2. Data Bit Error to Syndrome-Generate Matrix (32-Bit Configuration)

		L															H															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
																																		DQ0-31
	0	0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	1
	1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	5
	*2	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	6
SYNDROMES	*3	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	3
	4	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	4
	5	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	2
	6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0
		4	8	9	7	5	1	3	9	E	B	D	3	C	7	F	F	2	A	A	1	2	2	3	8	B	9	8	1	A	3	B	9	0	HEX
		3	3	2	0	2	3	2	1	3	0	0	1	2	3	2	1	3	1	4	6	6	5	4	5	3	4	6	5	2	7	6	7	1	

GENERATED CHECK BITS

*CG2, CG3 generate odd parity.

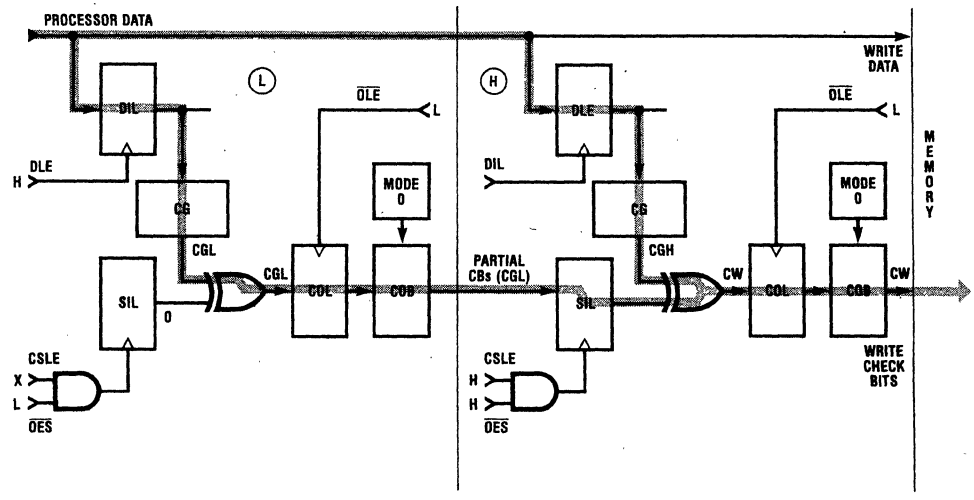


Figure 4c. E²C² 32-Bit Configuration, Write Flow Path

Table 3. Error Flags After Normal Read (32-Bit Configuration)

AE (H)	E1 (H)	E0 (H)	E0 (L)*	Error Type
0	0	0	0	No error
1	1	0	0	Single check bit error
1	1	1	0	Single data bit error (H)
1	1	0	1	Single data bit error (L)
1	0	0	0	Double bit error
All Others				Invalid conditions

*E0 (L) is valid after transfer of partial syndromes from higher to lower.

This approach to wider data width error detection and correction is termed the cascade configuration, and it requires only the one additional DP8400. The cascade approach can be used with up to five DP8400s controlling 80 data bits. The advantage is that only one additional DP8400 is required per 16 data bits, although write and read times become progressively slower as the number of DP8400s is increased. This is because of the time taken for the generated check bits to ripple through from the lowest to highest chips when writing and detecting, and then ripple back the other way for correcting.

In many memory systems, speed is of utmost importance and for faster systems, it is possible to connect the DP8400s in a parallel configuration using additional ICs. Application Note AN-308 describes this approach in detail.

The user may, therefore, select one of these approaches (or a combination of both) for systems using memory data widths of more than 16 bits.

Diagnostic Capabilities of the DP8400

The DP8400 has been designed with system fault diagnosis in mind. In fact, it is possible under microprocessor control with the DP8400 in situ on the memory board to fully test every gate inside the DP8400 activated in normal operation, and also to diagnose all memory check bits. The DP8400 has two main diagnostic modes — modes 2 and 6. In other words, with M1 set high and M0 set low, information can be written to or read from the chip.

Mode 6 allows the memory check bits to be read onto the higher byte bits 8–14, and syndromes to be read on the lower byte bits 0–6, as shown in *Figure 5a*. The remaining two bits, 7 and 15, are the error flags E1 and E0 that were valid when mode 6 was entered. The syndrome bits will be the internally generated syndromes if $\overline{OES}$ is low (mode 6A), or external syndromes input on the syndrome I/O port if $\overline{OES}$ is high (mode 6B). The external syndromes could be obtained from an error logger/syndrome injector unit — this is an error logger with the capability of injecting syndromes back to the DP8400. Therefore, by being able to read the externally stored syndromes, the microprocessor can monitor or store the syndromes whenever needed.

Mode 2 transfers system data from the higher byte into CIL, instead of DIL, to simulate check bits. This can be used in three ways. First, as shown in *Figure 5b*, the simulated check bits can be latched in CIL by taking CSLE low. If the DP8400 is now set to normal read, mode 4, and new data is presented then, provided DLE is high and CSLE is kept low, the DP8400 will perform a normal read operation as if it were reading memory check bits. The results of this simulated read may be checked by enabling DOL to see if an error (if inserted) was corrected. Or as a further check, by entering mode 6, the predicted generated syndromes and error flags may be checked. Second, also while in mode 2, the simulated check bits appear at the check bit port (from the data bus higher byte) available to be written to the check bit portion of memory as shown in *Figure 4c*. $\overline{OLE}$ is set high before the original simulated check bits are removed and then memory data is subsequently placed on the data bus. A write to memory will now write known data and simulated check bits to the selected location. By writing known data to the memory check bits in mode 2, and then reading the memory check bits in mode 6, each check bit in each location can be validated. Third, it is possible in mode 2 with $\overline{OES}$ low to transfer data from the higher byte to the syndrome I/O port, also shown in *Figure 5c*. But first the generated check bits must be all low. This is attained by previously loading all "1"s into DIL in an earlier cycle. This is useful when using an error logger in conjunction with the DP8400 to feed the syndrome word into the logger whenever an error occurs.

Error Logging with Syndrome Injection Capability

An important application of the dedicated syndrome I/O port is for error logging. This is because the internally generated syndromes derived during reading are available on this port, provided $\overline{OES}$ is set low. These syndromes indicate the exact location of a single error, whether it is in the data bits or check bits; they are therefore useful to be stored for error logging. Every time an error occurs when indicated by error flag AE, the syndromes corresponding to this error can be logged.

The syndrome word can be fed from SOL via the Syndrome Output Buffer onto the external syndrome bus. An Error Logger connected to this bus, as shown in *Figure 6*, will store the syndrome word in the same location as the corresponding address of each error that occurs. An intelligent error logger will differentiate between new errors and ones that have occurred previously, by logging only new errors and ignoring ones that have already occurred. An easy way to determine this would be to compare the incoming memory address with the address of errors contained in the logger. If a match is not found and an error occurs, the new address and corresponding syndromes are logged. If a match is

found, then whether an error occurs or not, no further action is necessary. Tag bits may be provided to indicate whether the error is hard or soft.

For example, if an error has already been logged at a particular address and that address is re-written to, then if the error repeats subsequently, it is a hard error, and if not, it is a soft error. So, if a tag bit is set when a write occurs to a previously logged address and a subsequent error is detected at that address, a second tag bit is set indicating a hard error. A better approach would be to have the DP8400 correct and rewrite to the same location all in the same cycle, as soon as a single error is detected. The first error detected in a location is classified as a soft error until it recurs, and if an error does recur, a tag bit is set to indicate a hard error. It is assumed here that multiple soft errors will not occur in the same location.

Now that the error logger contains error information, it is necessary for the microprocessor to retrieve it. The DP8400 makes this easy, because the external syndrome bus data can be transferred to the data bus as described for operation in mode 6. If the error logger is made capable of outputting stored syndromes, and subsequently outputting the corresponding address one byte at a time, then all the relevant information can be retrieved by the microprocessor. The user may choose to store this in nonvolatile memory in the event of a power failure. When power returns, it will be desirable to restore this information back to the error logger, and this can be achieved by first loading DIL with all "1"s to create all generated check bits low. Now the addresses and syndromes can be loaded from the higher byte of the microprocessor through the syndrome I/O port one byte at a time, with DP8400 in mode 2, to the error logger.

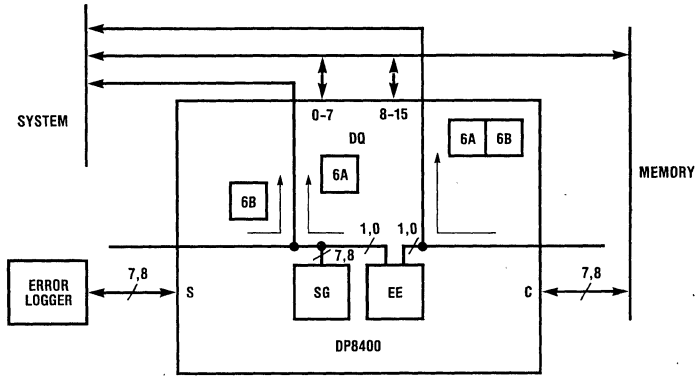


Figure 5a. Read Internal Generated Syndromes and Check Bit Port (Mode 6A) or Read Syndrome Port and Check Bit Port (Mode 6B)

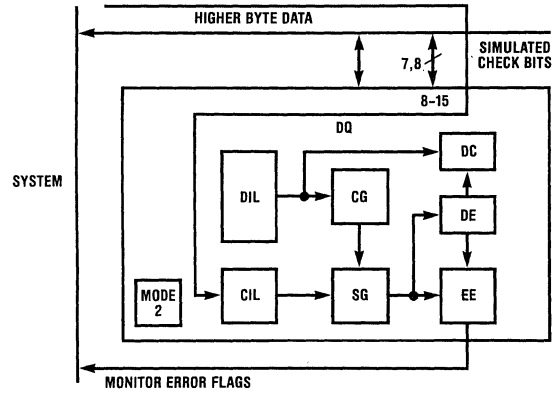
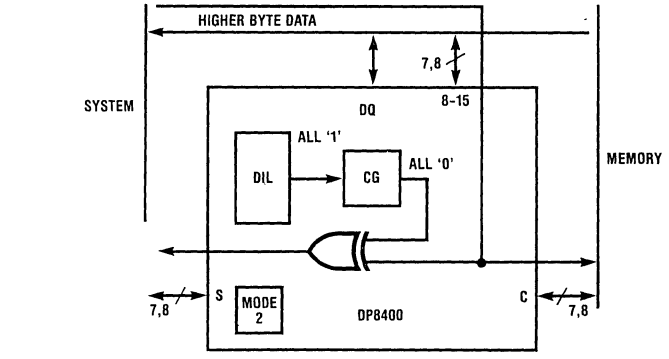


Figure 5b. Diagnostic Read—Compare Simulated Check Bits with Check Bits Generated from Data Stored in Previous Cycle



1) DIAGNOSTIC WRITE: WRITE HIGHER DATA BYTE TO CHECK BIT BUS (MODE 2)

2) TRANSFER HIGHER DATA BYTE TO SYNDROME BUS (MODE 2, PREVIOUS CYCLE LATCHED ALL '1's IN DIL TO MAKE CG=0)

Figure 5c. DP8400: Mode 2

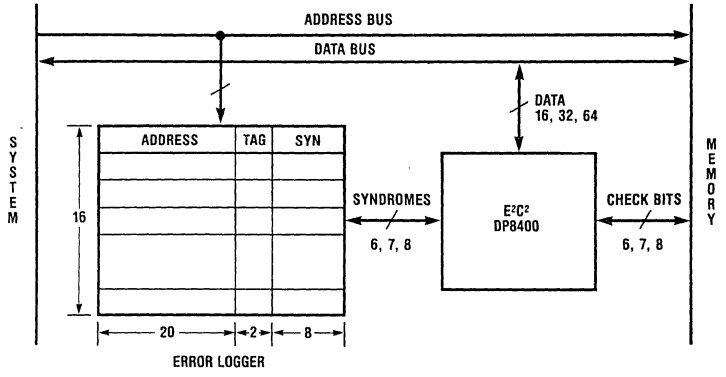


Figure 6. Error Logger Connected to DP8400 Syndrome Port

Correcting Double Errors Using the Error Logger

It is possible to take the error logging function one stage further. As described so far, the error logger has been storing single errors (data bit or check bit). What if a double error is detected? If it is detected without any previous history at that address, one solution would be to perform a Double Complement to attempt to correct both errors. If this is not done, no useful information can be obtained. If both errors are corrected, the error logger records the syndromes of both, and tags whether they were both hard, or one hard and one soft. But, if there is a previous history at this address of a single error, then it is fair to assume that the second error has subsequently occurred. In this case, if the error logger could be made to inject the syndromes of the first error into the DP8400, the DP8400 would correct this error so that its DOL would then contain data with one error (if both errors are data bit errors). It is necessary at this point to wrap-around DOL back to DIL and allow the DP8400 to correct the second error. This approach is much faster than the Double Complement approach and at the same time offers full error logging capability.

Any Double Error Correction Using The Double Syndrome Decode Approach

The data sheet shows how the DP8400 can perform double error correction using the Double Complement Approach, provided at least one of the errors was hard. For very large memories, this may not be adequate, as some systems will require total double error correction capability—quickly, without having to wait two additional memory cycles. Some of these systems will also required triple error detect capability. Fortunately, the matrix of the DP8400 has been configured to allow both of these capabilities. Most modern error detection/correction matrices use a modified version of Hamming's original code. The Hamming code allows single errors to be corrected, however, two errors may not be detected as such. For 16 data bits, five check bits are required. Modified Hamming codes allow double error detect capability, as well, by arranging that the Exclusive-OR of the syndrome words of any two bits in error produces an even parity syndrome word. A parity check on the syndrome bus will, therefore, indicate two errors (or no error, but in this case, the Any Error flag will be inactive). For 16 data bits, six check bits are required for single/double error detect and single error correction capabilities.

The DP8400 has a matrix that goes one step further by using a version of the Nelson code. This costs no additional on-chip gates to those required for a Modified Hamming code. To be able to correct any two errors, it is necessary to be able to determine their location, and no present version of the Modified Hamming code is able to do this. There are matrices that do exist that can generate 12 check bits from 16 data bits (or 14 check bits from 32 data bits) for writing, and then generate 12 (or 14) syndrome bits when reading, so that the location of both errors can be determined and corrected. But, because most applications do not require this degree of integrity and associated expense, they are not very popular. It would be ideal if two DP8400s could be configured as in *Figure 7a*, with each generating a different set of check bits and a different set of syndrome bits so that the double syndrome word could be unique and decodable for any two bits in error. Fortunately, National Semiconductor has achieved this by incorporating a feature called the Rotational Syndrome Word Generator, which uses rotated data to the secondary DP8400.

The primary DP8400 generates check bits when writing, and syndrome bits when reading, as in a normal 16-bit system. But the data port of the secondary DP8400 receives data shifted by a number of bits, usually one bit. In other words, for this secondary chip, system data bit 0 connects to DQ1, system data bit 1 to DQ2, etc. Each DP8400 has its own dedicated six memory check bits, which are obviously different from each other due to the data shifting on the secondary DP8400. The Nelson code is such that during a read, not only does each DP8400 generate a different set of syndrome bits, but the double syndrome word (comprising 12 bits for 16 data bits) is unique for any two bits in error. It is necessary to be able to output these syndromes as they occur and to do this, $\overline{OES}$ of both chips is set low during the time memory data is valid.

Now that we have a unique double syndrome word for any two bits in error, it is necessary to decode it to correct both errors. The easiest way to do this is to connect the double syndrome word to the address inputs of a registered PROM (a PROM with latchable data out) as shown in *Figure 7b*. In this example, 12 syndrome bits require 4k addressing capability, and 32k registered PROMs will be made available soon. Some of the addresses of the RPROM will be used for double errors and each address will be unique for any two bits in error. The corresponding data out could, therefore, contain one of the syndrome words. Double errors may be caused by two data bit errors, a data bit and primary check bit error, a data bit and secondary check bit error, a primary and secondary check bit error, or two errors in either primary or secondary check bits. In these cases, if the RPROM address stores the syndrome word for one of the two errors, this will be available at the output of the RPROM when enabled.

First of all, this data must be latched in the RPROM register, and then the $\overline{OES}$ input to each DP8400 must be set high to deactivate the two syndrome output buffers. Next, the RPROM data must be enabled onto the primary syndrome bus so the primary DP8400 can enter this syndrome word, representing one of the two bits in error with CSLE high. At the same time, the primary DP8400 must be set to mode 7 so that the syndrome word appears on the internal syndrome bus, replacing the generated syndromes. If $\overline{OLE}$ is now set from low to high, DOL will contain either one or no error, depending on where the two errors were located. In other words, the DP8400 has just corrected one of the errors. By setting $\overline{OLE}$ low, then disabling memory and enabling $\overline{OB0}$ and $\overline{OB1}$ of the primary DP8400, this data is output on the data bus and back into the DIL with DLE high. There is now only one data error, and this can be corrected by setting the DP8400 to normal read, mode 4.

Thus, both errors have been corrected at a fairly fast rate. For example, for a 50ns RPROM, the total time to generate double syndromes, feed back a one-error syndrome word to the primary DP8400, correct it, wraparound, and correct again, may take less than 120ns total.

Only a few of the addresses in the RPROM are required for double errors. Some double syndrome words represent single errors and triple errors. All single bit errors also produce a unique double syndrome word different from all double bit errors.

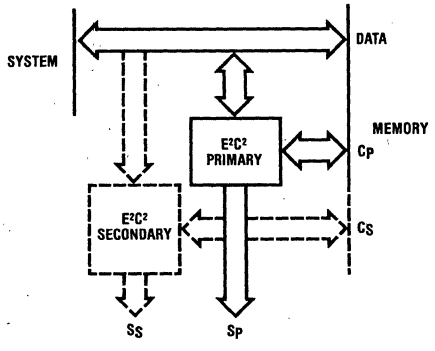


Figure 7a. 2 Different Generators

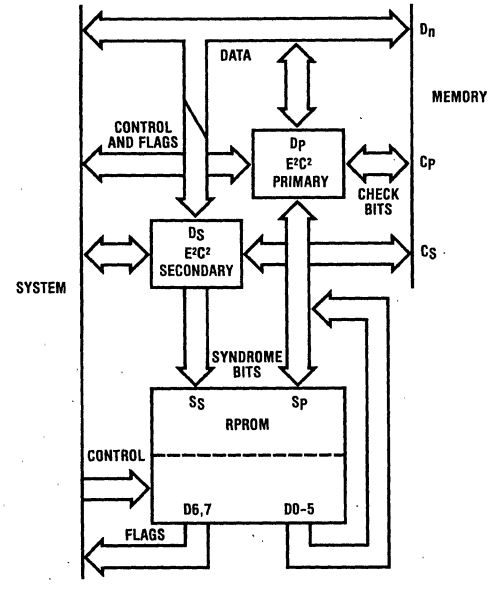


Figure 7b

In fact, nearly all triple bit errors produce unique double syndrome words different from single and double bit errors. Those that do not produce unique double syndrome words, duplicate double syndrome words of other single, double, and triple bit errors; however, these comprise only about 5 percent of the total. We can say, therefore, that this approach will correct not only all double bit errors, but will detect 95 percent of all triple bit errors. Note that with error correction systems utilizing the modified Hamming code, the majority of triple bit errors are interpreted as single bit errors and falsely corrected as such. It is up to the designer to determine the chances of three errors occurring in a memory location, and the (likely) consequences that they will be falsely corrected. If this condition is undesirable, then the Double Syndrome Decode Method offers greatly enhanced integrity; in fact, if the three errors detected do have a unique double syndrome word, they can be corrected. As stated, no presently used Modified Hamming code offers a unique double syndrome word for multiple errors; this is only possible with a Nelson code. This example was largely for 16 data bits, but the idea will work for other data widths.

In the 16-bit example, the RPROM has to output only six bits representing the syndrome bits of a bit in error. This leaves two spare bits which can be used as flags, and the user can program his RPROM accordingly. One solution is to use these flags to indicate the type of action required — whether to correct at all, correct once, or correct twice by wrapping around.

Block Diagram of the DP8400

This Application Note discusses first the single error correction, showing a simplified block diagram of the chip for both a write cycle to generate check bits, and a read cycle to detect errors and correct single bit errors.

The most important requirement when accessing memory is that these operations be performed with minimal memory delays. The DP8400, therefore, has been structured internally to minimize series propagation delays through the chip. A full block diagram of the DP8400 is shown, and first impressions are that there might be excessive delays in the various paths due to the additional blocks that have been added to the basic functional block diagram. In fact, this is not the case, because the DP8400 has been configured in bipolar Schottky logic and uses the AND-OR-INVERT gate in many of the blocks. This type of gate structure is used in multiplexers, Exclusive-OR gates and fall-through latches. It is possible, therefore, to combine these functions into one wide gate, reducing the propagation delays through some of these blocks to that of one gate. For example, the check bit output latch COL receives its input from an Exclusive-OR gate followed by a multiplexer. These three functions can be combined into one wide gate, and this greatly reduces the time taken to generate check bits.

The DP8400 — A Versatile Error Checker/ Corrector for All Applications

It was shown earlier how the DP8400 was able to detect single and double errors, and correct single errors. For 8-and 16-bit systems, these could easily be accomplished with a minimum of extra circuitry. The DP8400 can also be used in complex high integrity systems. In fact, investigations are still progressing as to its immense capabilities. It is the only error correction circuit capable of these features, and yet it still provides very fast throughput. For these reasons, the DP8400 should become the industry standard error correction chip for the foreseeable future.

DP8400s in 64-Bit Expansion

National Semiconductor
Application Note AN-308
Chuck Pham
June 1982

The purpose of this Application Note is to provide memory designers with detailed information on the DP8400 parallel expansion method. This method allows fast check bit generation, error detection, and error correction. A thorough understanding of the 16-bit implementation is a prerequisite. Included in this note are the following: error correction expansion matrix; detailed steps for check bit generation, error detection and error correction; an example of a single error correction; and the detailed wiring diagram for the 64-bit configuration.

The Error Correction Expansion Matrix

For a 16-bit word, the DP8400 reads data between the processor and memory, with its 16-bit bidirectional data bus connected to the memory data bus. The DP8400 uses an encoding matrix to generate six check bits from the 16 bits of data. This 16-bit matrix contains 16 unique syndrome patterns corresponding to each error location which allows the DP8400's Data Error Decoder (DED) to identify the data error location.

The DP8400 is easily expandable to other data configurations. For a 32-bit data word with seven check bits, two DP8400s are used. Three DP8400s can be used for 48 bits, four DP8400s for 64 bits, and five DP8400s for 80 bits, all with eight check bits. In order to expand the DP8400, additional check bits are required to provide the unique characteristic of the single data error syndrome. For expansion beyond 24 bits, check bits 6 and 7 (C6 and C7) are used. Note that these check bits can be configured to be always either zero or word parity, depending on the input voltage level of the Expansion Pin (XP). By rearranging all eight check bits (C0- C7) of each DP8400, we can obtain many different matrices that meet the above requirement. One of these is shown in Table 1. For illustration, this matrix will be used throughout this application note to clarify the E^2C^2 expansion concept.

Check Bit Generation, Error Detection And Error Correction

Check Bit Generation (*Figure 1*)

In the Check Bit Generation mode, all four DP8400s are set to mode 0, normal write. The 64 bits of data from the system data bus are enabled into the Data Input Latches (DIL) of each DP8400. The individual Check Bit Generators (CG) of the four DP8400s then produce eight parity bits, or partial check bits, derived from the input data. (Note that all the syndrome input latches should be cleared so that only the partial check bits will pass through the Check Bit Output Latches/Buffers (COL and COB)). In the normal write mode, the COBs are always enabled onto each check bit port. This allows the partial

Table 1. Data Bit Error to Syndrome-Generate Matrix, 64-Bit Configuration

The partial code of device 0:

Error Locations (Data Bit Numbers)																
0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	C3
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C6
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C7

The partial code of device 1:

16	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**	**27**	**28**	**29**	**30**	**31**	
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C6
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
0	1	1	0	0	0	0	0	1	1	1	1	0	1	0	1	C3
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C7

The partial code of device 2:

32	**33**	**34**	**35**	**36**	**37**	**38**	**39**	**40**	**41**	**42**	**43**	**44**	**45**	**46**	**47**	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C6
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	C3
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C7
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0

The partial code of device 3:

48	**49**	**50**	**51**	**52**	**53**	**54**	**55**	**56**	**57**	**58**	**59**	**60**	**61**	**62**	**63**	
1	1	0	0	0	1	0	1	1	0	0	1	0	1	0	1	C4
1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	C5
0	1	1	0	0	0	0	1	1	1	1	0	1	0	1	1	C3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	C6
1	0	0	1	1	0	0	0	1	0	1	0	1	1	1	1	C2
0	0	1	1	1	1	1	1	0	1	1	1	0	1	1	1	C0
0	0	0	1	0	0	1	0	1	1	0	1	0	1	1	1	C1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	C7

check bits to be combined externally in the eight 74S280s' parity generators/checkers to produce eight composite check bits. Table 2 shows how these check bits are generated.

Table 2. Composite Check Bit Generation

Ccomp. 0	= C(0)0 ⊕ C(1)1 ⊕ C(2)6 ⊕ C(3)4
Ccomp. 1	= C(0)1 ⊕ C(1)5 ⊕ C(2)3 ⊕ C(3)5
Ccomp. 2	= C(0)2 ⊕ C(1)6 ⊕ C(2)5 ⊕ C(3)3
Ccomp. 3	= C(0)3 ⊕ C(1)4 ⊕ C(2)4 ⊕ C(3)6
Ccomp. 4	= C(0)4 ⊕ C(1)3 ⊕ C(2)2 ⊕ C(3)2
Ccomp. 5	= C(0)5 ⊕ C(1)2 ⊕ C(2)7 ⊕ C(3)0
Ccomp. 6	= C(0)6 ⊕ C(1)0 ⊕ C(2)1 ⊕ C(3)1
Ccomp. 7	= C(0)7 ⊕ C(1)7 ⊕ C(2)0 ⊕ C(3)7

Notes:
Ccomp: composite check bit.
C(X)N: the partial check bit N of device X.
(Refer to Table 1 for clarification.)

To aid in fast error detection during memory read cycles, these composite check bits are complemented and written into memory along with the system data. If the system data has vacated the data bus, the Output Enables ($\overline{OB0}$ and $\overline{OB1}$) must be set low so that the original data word with its eight composite check bits can be written into memory.

Detection Mode (*Figure 2*)

In the Detection mode, again all the DP8400s are set to mode 0, normal write, then the partial check bits derived from the memory data bits are generated in a manner similar to that described for the check bit generation mode. These partial check bits are then associatively compared with the memory check bits in the eight 74S280s to produce eight external $\overline{\text{Composite Syndrome}}$ bits. As explained in the check bit generation mode, the composite check bits are complemented before being written into memory. This shows why complemented Composite Syndrome bits are produced instead of true composite syndromes. Then, if any bits on the $\overline{\text{Composite Syndrome}}$ bus go low, this will cause the 74S30 NAND gate to go high, giving the $\overline{\text{Any Error}}$ indication. If there is no error, all $\overline{\text{Composite Syndrome}}$ bits remain high. These $\overline{\text{Syndrome}}$ bits are also latched into the 74ALS533 Octal D-type Transparent Latch (with inverted output). The composite syndromes are then fed into the syndrome ports of the DP8400s in different combinations for each, for error-type determination and/or error correction.

Correction Mode: (*Figure 3*)

Upon receiving the Any Error indication during the detection mode, it takes an additional step to determine the error type and to correct a single data error. All the DP8400s should be set to mode 7B (which is mode 7 with $\overline{OES}$ high), this mode enables the external syndromes directly to the Syndrome Generator (SG) and then the Data Error Decoder (DED) of each chip. For a single data error, the input syndrome will be unique for that error location; consequently, only one DP8400 can decode that error location and correct that bit. The other three do not indicate an error and do not change their data output latch contents. This corrected data can be output to the system data bus by means of $\overline{OB0}$ and $\overline{OB1}$. The DP8400 that decodes the data error location will indicate a single data error, while all others indicate a check bit error. If there was a single check bit error or a double bit error, then all the DP8400s will indicate a check bit error or a double bit error, respectively, through their error flags.

An Example of a Single Data Error Correction

Assuming all zero data is to be written into memory, we obtain the following set of partial check bits for all DP8400s:

C0 = 0	C4 = 0
C1 = 0	C5 = 0
C2 = 1	C6 = 0
C3 = 1	C7 = 0

Note that each DP8400 contains the basic 16-bit matrix (C0–C5). Therefore, the first six partial check bits are the same for all devices; only C6 and C7 are different. With the 64-bit configuration using the above 64-bit matrix, C6 = C7 = 0 (by connecting XP directly to V_{CC}) for the devices 0, 1, and 2; and C6 = C7 = word parity (by leaving XP pin floating) for the device 3. However, with all zero data, word parity is also zero (even parity). Therefore, the above partial check bits are obtained.

Using the formulas given in Table 2, the composite check bits are as follows:

Ccomp. 0	= 0 ⊕ 0 ⊕ 0 ⊕ 0 = 0
Ccomp. 1	= 0 ⊕ 0 ⊕ 1 ⊕ 0 = 1
Ccomp. 2	= 1 ⊕ 0 ⊕ 0 ⊕ 1 = 0
Ccomp. 3	= 1 ⊕ 0 ⊕ 0 ⊕ 0 = 1
Ccomp. 4	= 0 ⊕ 1 ⊕ 1 ⊕ 1 = 1
Ccomp. 5	= 0 ⊕ 1 ⊕ 0 ⊕ 0 = 1
Ccomp. 6	= 0 ⊕ 0 ⊕ 0 ⊕ 0 = 0
Ccomp. 7	= 0 ⊕ 0 ⊕ 0 ⊕ 0 = 0

Note that these composite check bits are complemented before they are written into memory. Thus, the memory check bits read later from memory are 1100 0101.

If an error has occurred in the data position 35 which is bit 3 of device 2, then the partial check bits C(3)N produced during the detection mode are as follows:

C(3)0 = 1	C(4) = 0
C(3)1 = 1	C(5) = 0
C(3)2 = 0	C(6) = 0
C(3)3 = 1	C(7) = 0

The partial check bits of other devices are unchanged. Consequently, the newly generated composite check bits (Ccomp) and the total syndrome bits are:

Bit #	Newly Generated Composite Check Bits		Memory Check Bits		$\overline{\text{Composite Syndrome}}$
0	0	⊕	1	=	1
1	1	⊕	0	=	1
2	0	⊕	1	=	1
3	1	⊕	0	=	1
4	0	⊕	0	=	0
5	1	⊕	0	=	1
6	1	⊕	1	=	0
7	1	⊕	1	=	0

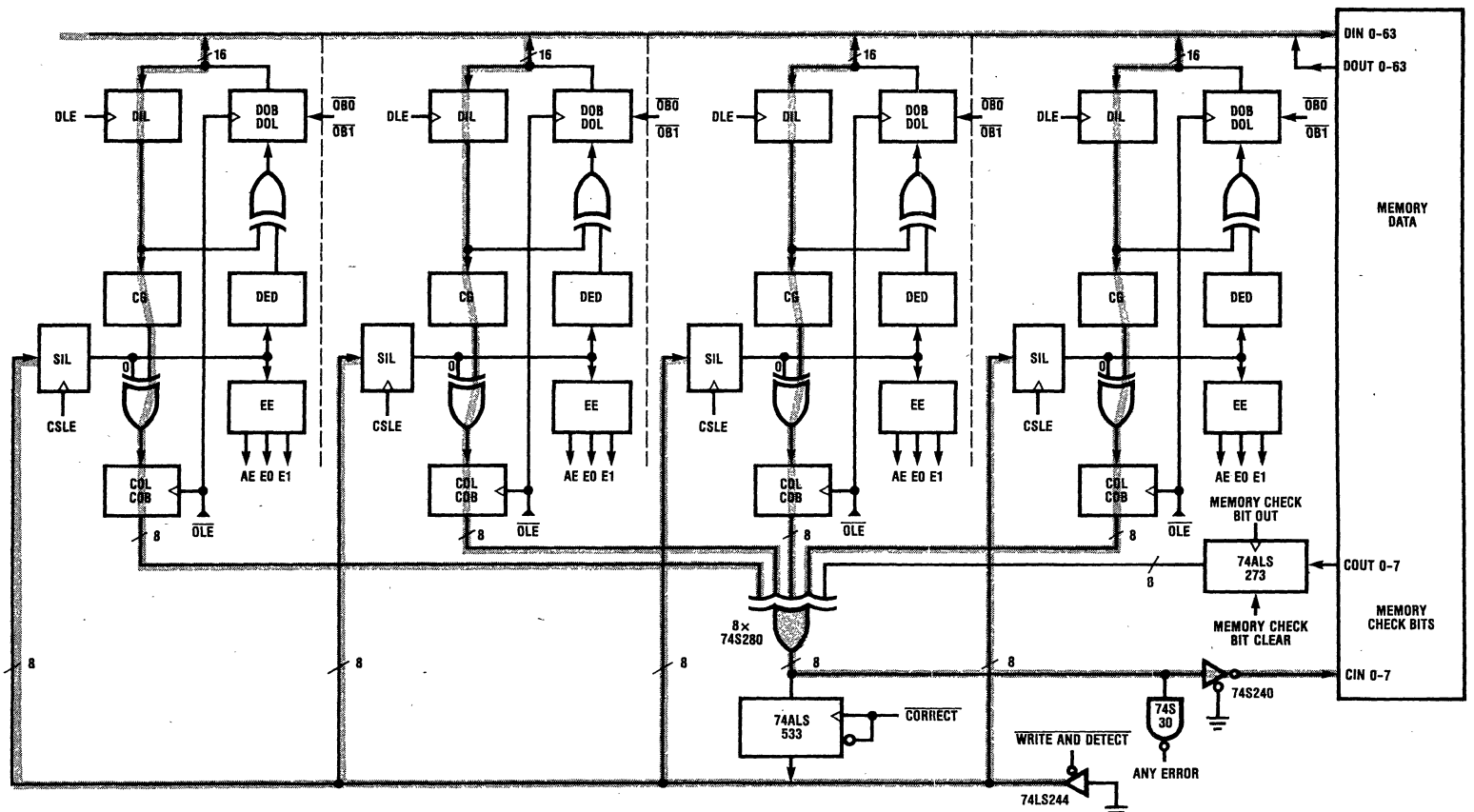


Figure 1. E^2C^2 Simplified Block Diagram—
64-Bit Parallel Expansion, Check-Bit Generation

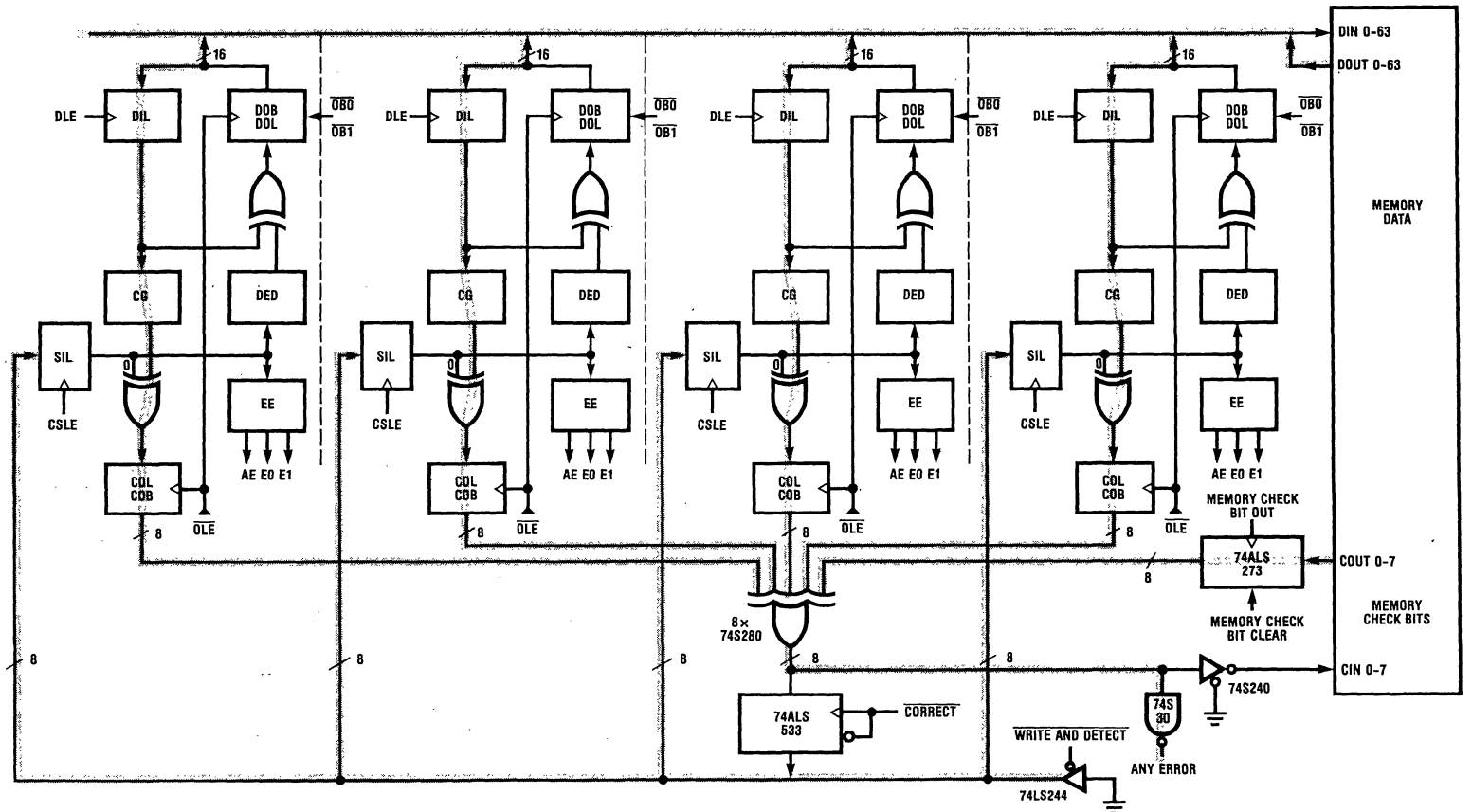


Figure 2. E^2C^2 Simplified Block Diagram — 64-Bit Parallel Expansion, Error Detection

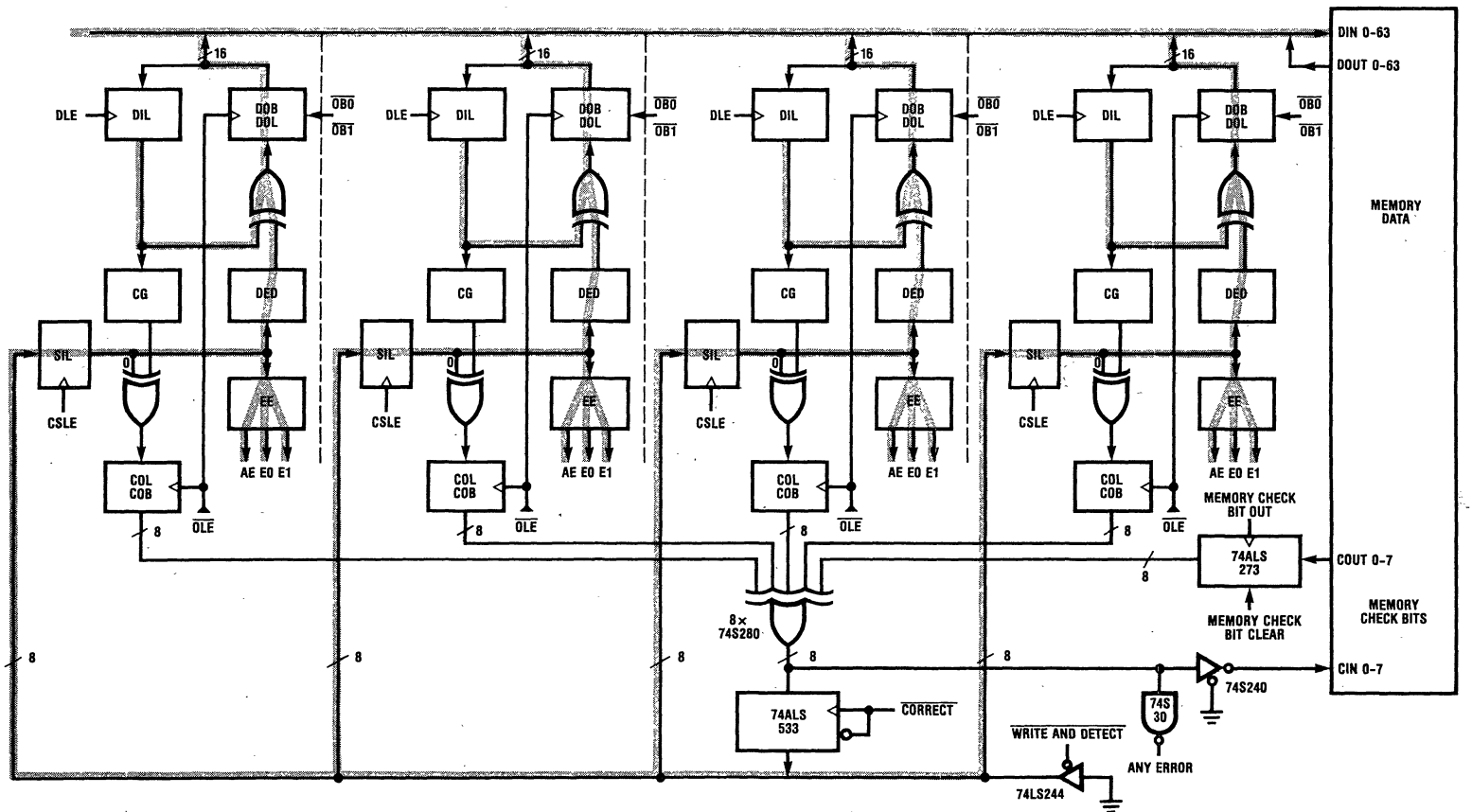


Figure 3. E^2C^2 Simplified Block Diagram — 64-Bit Parallel Expansion, Error Determination and Correction

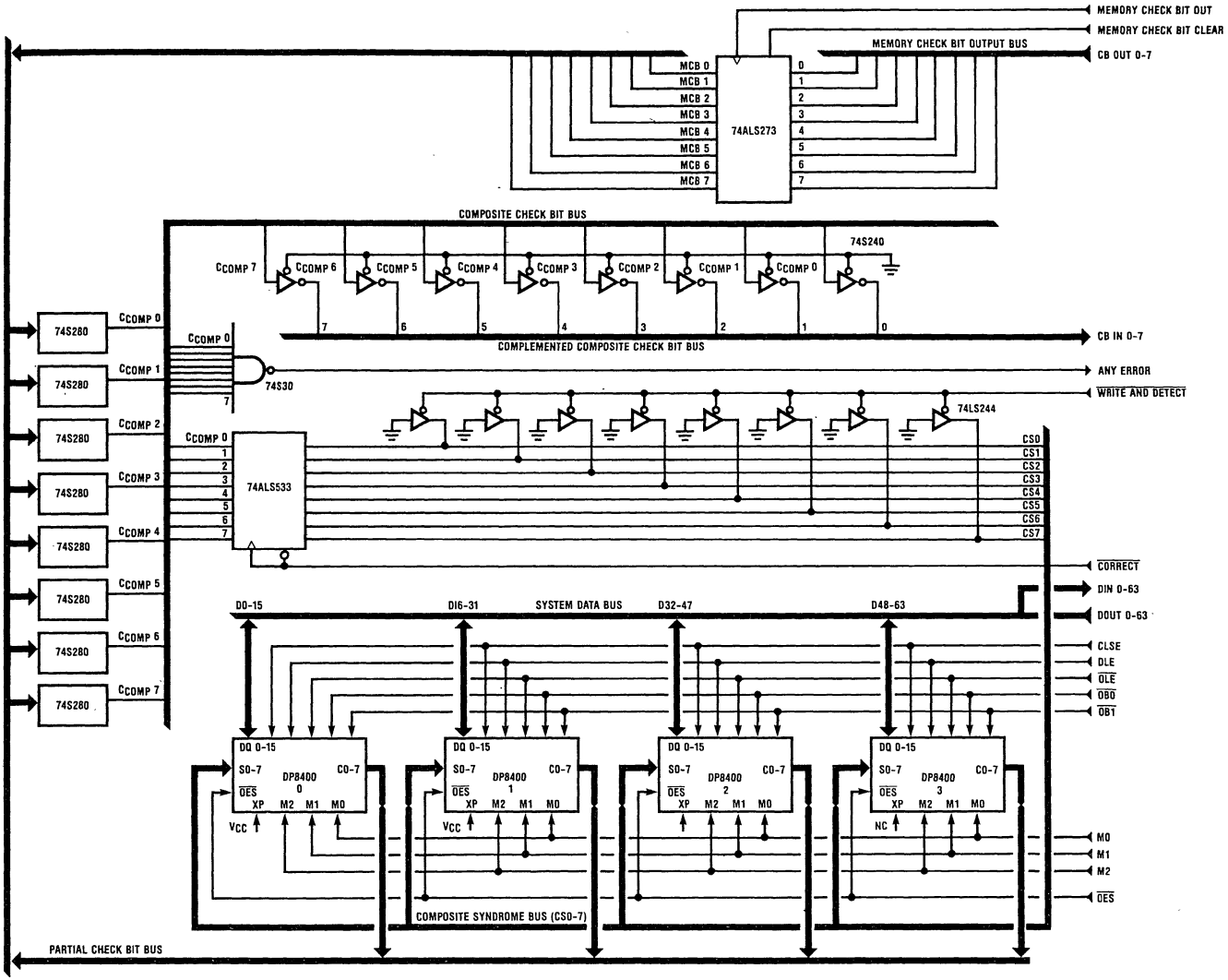


Figure 4. E²C² 64-Bit Parallel Expansion, Detailed Block Diagram

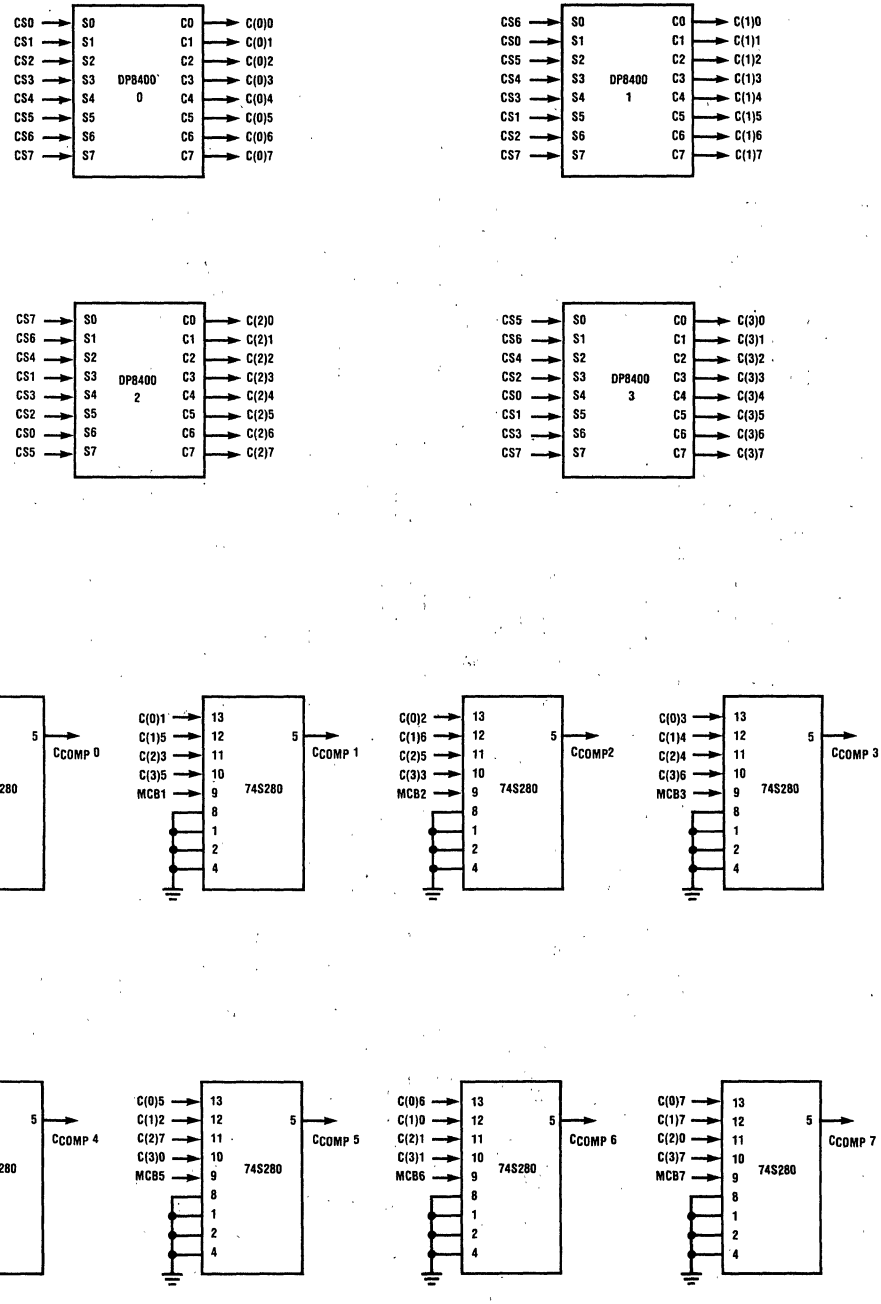


Figure 5. E^2C^2 64-Bit Parallel Expansion, Detailed Connection Diagram

The composite syndrome 1101 0000 is that of the error location 35. Since the syndrome is unique and fed re-ordered to each DP8400, only device 2 will recognize this syndrome pattern and complement its data bit 3. Then the corrected data can be output to the system data bus when $\overline{OB0}$ and $\overline{OB1}$ of all four DP8400s go low. Devices 0, 1, and 3 all output the same data they received from memory. Only device 2 changes its (erroneous) data. Refer to *Figure 6* below for the timing diagrams of a memory write and memory read cycle (detect then correct).

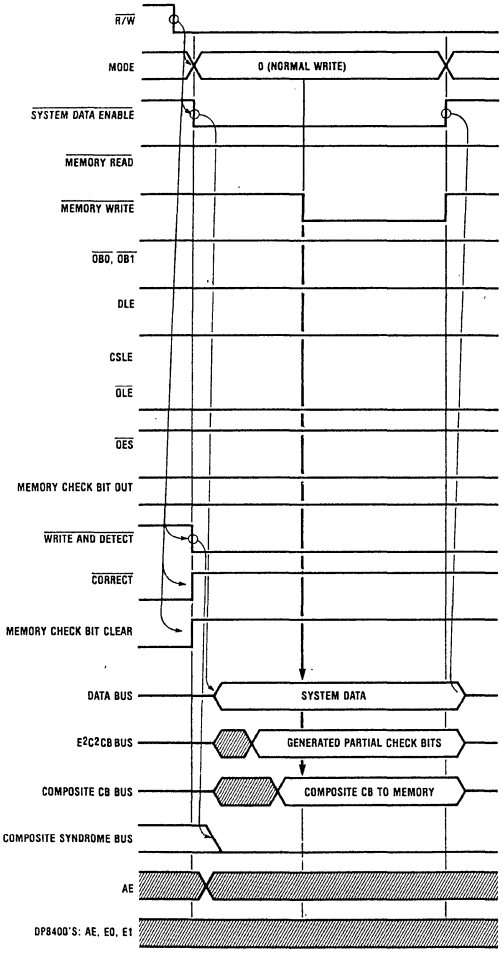


Figure 6A. E^2C^2 64-Bit Parallel Expansion Memory Write Cycle

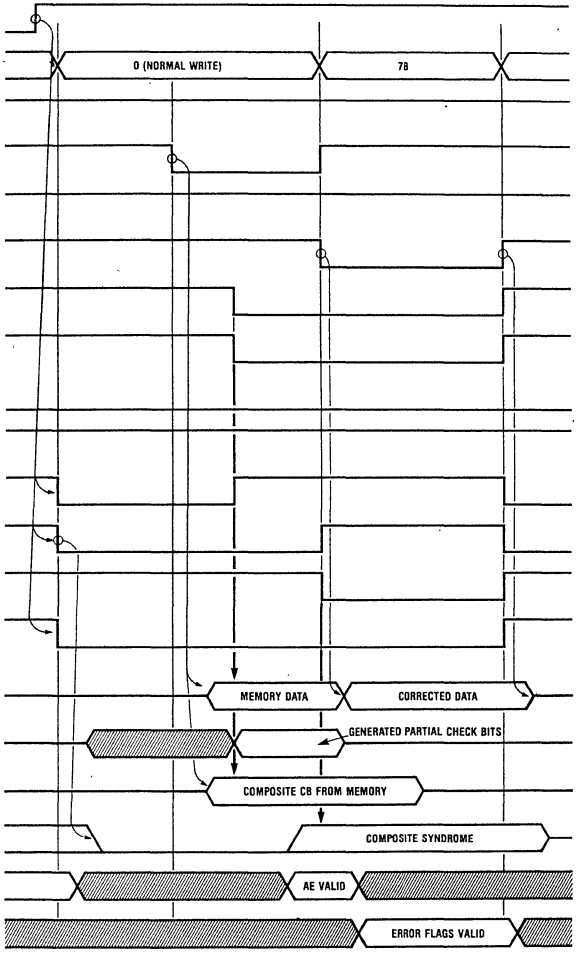


Figure 6B. E^2C^2 64-Bit Parallel Expansion Memory Read Cycle (Detect Then Correct)

ERROR CORRECTION THE HARD WAY

A double complement correct cycle in an ECC system forms a sophisticated double-bit error correction and management system

by Bob Nelson

The use of parity, the most common error detection method, can be expanded from simple error detection in data words to the correction of single-bit errors by means of a double complement correct cycle. The double complement method can also be used to advantage in combination with error checking and correction systems to detect and correct hard and soft combinations of double-bit errors, provided no more than one of such errors is soft. In addition, this technique points the way to more sophisticated double-bit error correction and error management systems.

A parity bit is assigned a value of 1 or 0 on the basis of the number of 1s in the data word. The value of the parity bit depends on whether the parity system chosen is odd or even. Thus, in an odd parity system, the sum of the 1s in the data word and the parity bit will always be odd, whereas in an even parity system, the sum of the 1s in the data word and the parity bit will always be even (Fig 1). All examples in this discussion, except for those in Fig 1, use odd parity. A single parity bit can be used to detect a single-bit error occurring during a memory read cycle, and the technique can be expanded to provide even further error handling.

Parity error detection and correction

During a memory write, the parity bit which is created as a result of the data is written to the memory along with the data word for storage. When a read cycle occurs, parity generation is again performed on the data word, creating a new parity bit, which is then compared with the original parity bit read from memory. If a difference exists between the two parity bits, an error has occurred. Although this error cannot be located with the information given, and may have occurred in any bit location in the data word or even in the parity bit, if it is a hard error, its location can be determined through the use of additional memory cycles.

Data Word	Parity	Number of 1s	System
10001010	1	4	even
10001010	0	3	odd
01101001	1	5	odd

Fig 1 Odd and even parity. Value of parity bit is generated to satisfy chosen parity system (even or odd) so that sum of all 1s, including parity bit, will conform to even or odd parity system

If an error is detected during a memory read cycle, a simple procedure called the double complement method will determine if the error is hard, and, if so, correct it. The method includes a routine during which the suspect data and parity bit are complemented and presented to the same location in memory for a write cycle. Following the write, a read cycle is performed, and if the error is a hard error, the memory will repeat it by providing the data with the error bit complemented again. After a second complement, the data will be correct. At the end of such a correct cycle the memory contains the complemented data, and one additional write cycle must be performed to restore the data in memory (Fig 2).

During a double complement correct cycle involving a data word containing an even number of bit locations, the parity test is performed after the second read and before the second complement. If the error is hard, a parity error will once again be detected following the second read. If the error is soft, a parity error will not result following the second read. For data words containing an odd number of bit locations, parity testing

1st write	11010011	0	original data
1st read	11010111	0	PE (parity error)
$D \rightarrow \overline{D}$	00101000	1	data are complemented
2nd write	00101000	1	complemented data
2nd read	00101100	1	PE (parity error)
$\overline{D} \rightarrow D$	11010011	0	data are complemented

↑ hard error location

Fig 2 Hard error correction with parity. Single parity bit can be used to correct single-bit hard error with double complement method. On each memory read, original parity bit is read and new parity check is done on bits in data word. New parity bit is then compared with that read for validity

Bob Nelson is responsible for digital systems applications and new product definition at National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. His engineering career began at the Burroughs Corp, where he worked on semiconductor memory systems and system interface design for large mainframe computers. Mr Nelson completed his basic engineering studies at Citrus College, Azusa, Calif, following undergraduate work at Pasadena City College.

Published in *Computer Design*, December, 1981.
Reprinted by permission.

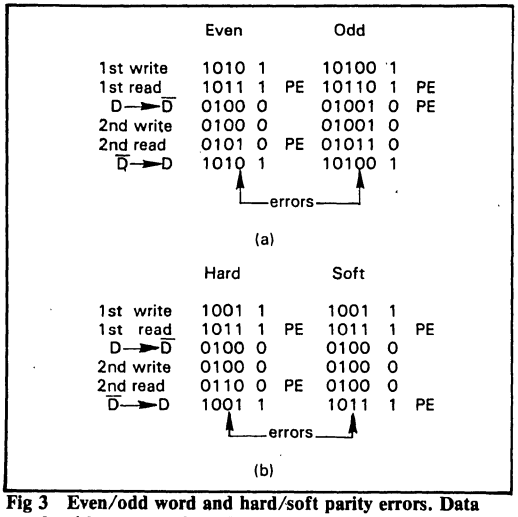


Fig 3 Even/odd word and hard/soft parity errors. Data words with even number of bits do not yield parity error on second read (a), nor soft error (b). Hard error, however, will be corrected

must be performed at different times during the correct cycle. In both cases, a double complement correct cycle can determine the type of error and, if it is hard, correct it (Fig 3).

If the bit in error is hard, the double complement correct can also be used to determine the bit's location in the data word. To do this, the data word and parity must be stored in a register when an error is detected. At the conclusion of the hard error correcting cycle, the location of the failing bit is determined by comparing the correct data with the contents of the register (Fig 4).

Thus, the use of a single parity bit not only makes it possible to deduce the error type, but also to locate and correct hard errors. This technique is useful for low cost terminal and word processing systems since, where retry is acceptable, the small amount of additional hardware

...the double complement method...also points the way to more sophisticated double-bit error correction and error management systems.

required can often eliminate the cost of an unscheduled service call. If a hard error can be detected, a double complement correct cycle will correct it, and the technique combined with an error checking and correction (ECC) system can also provide extended error correction capability when hard errors are involved.

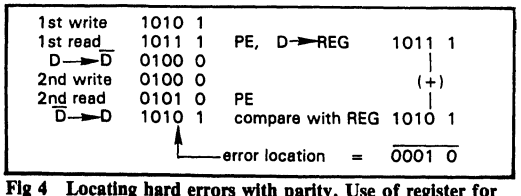


Fig 4 Locating hard errors with parity. Use of register for temporary storage enables double complement cycle to locate single hard error

ECC and double complement

The double complement method in combination with an ECC system can correct additional errors, both hard and soft. The ECC system under discussion here uses the code implemented by National Semiconductor in the DP8400 ECC device (Fig 5) to perform 1-bit error correction and 2-bit error detection. In an ECC system for 16-bit data words, such as the one discussed here, six parity bits are generated. Each of the parity bits is assigned a value as a function of the sum of the 1s in a unique combination of selected bits in the data word. Partial word parity bits in an ECC system are referred to as check bits. For simplicity, odd parity will be used in the examples, although in most ECC systems, including those implemented with the DP8400, a combination of odd and even parity is used to improve memory diagnostic capabilities.

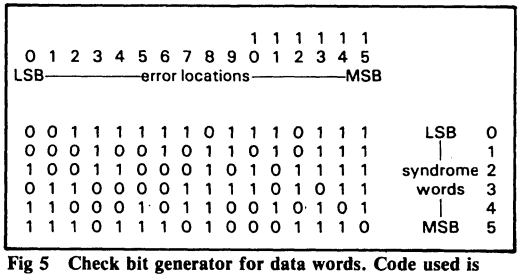


Fig 5 Check bit generator for data words. Code used is that implemented in National Semiconductor's DP8400 ECC device

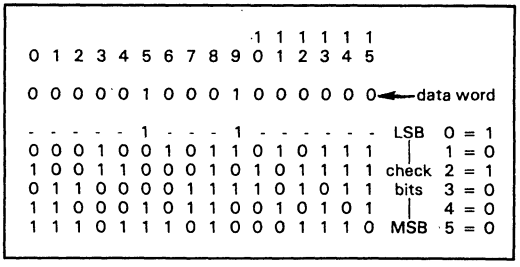


Fig 6 Error check bits are generated by presenting the data word to ECC code matrix and noting corresponding 1s. In first row, bits 5 and 9 correspond with 1s in matrix. Thus, to maintain odd parity LSB of check bits is set to 1

An ECC code forms a matrix (Fig 6) to which a data word can be presented for the generation of check bits. Given a data word, such as 0000010001000000, and the uppermost horizontal row of the matrix in Fig 7, check bit 0 is to be assigned a value based on the sum of corresponding 1s in that row and the data word. Using odd parity, the corresponding 1s in locations 5 and 9 dictate

Write	0000010001000000	000101	
Read	0000010001010000	000101	error in 11
Generate	0000010001010000	010110	new check bits
XOR check bits		010011	syndrome bits

Fig 7 Generating syndromes for locating error. Syndrome word is result of exclusive OR (XOR) of error check bits. No-error condition would result in syndrome word of all 0s

a value of 1 for the parity bit. For check bit 1, the selected location of correspondence is 9 only. Check bit 1 is assigned a value of 0 for odd parity. The complete set of check bits for this particular word is 000101 (05 HEX).

After check bit generation, the data and check bits go to the memory. During the read a new set of check bits are generated and compared against the check bits read from memory. The results of this check bit compare, an exclusive OR (XOR) function, are the syndromes (Fig 7). The single error indicating syndrome word is unique and is interpreted by the syndrome decoder to indicate the column in the matrix corresponding to the error location. The matrix or code is therefore a check bit generator for data, but a syndrome generator for error locations.

The...method in combination with an ECC system can correct additional errors, both hard and soft.

	5 9		
1st write	0000000000000000	110011	original data
1st read	0000010001000000	110011	2 errors
D→D	1111101110111111	001100	complement
2nd write	1111101110111111	001100	
2nd read	1111101111111111	001100	hard error fixed
D→D	0000010000000000	110011	complement
		000010	new check bits
		110001	syndromes for bit 5

Fig 8 Correction of hard and soft errors. In the case of data word with one hard and one soft error, double complement method has corrected hard error and determined existence of soft error, which is then located by syndrome word and can be corrected

The check bits, or partial word parity bits, generated by modified Hamming codes and the code used in the DP8400, are also capable of providing complete error reporting. Since the single error reporting syndrome words contain an odd number of 1s and the total number of 1s is greater than one, 2-bit errors can easily be distinguished from a 1-bit or detectable triple-bit error. The DP8400 monolithic ECC device performs this error determination by counting the number of 1s in the error indicating syndrome words. When no error exists, the syndrome word contains no 1s, and when a single check is in error, a single 1 is present in the syndrome word. When an odd number of data bits are in error, the number of 1s in the syndrome word is odd and greater than 1 (3 or 5 in this example); if an even number of bits are in error, the syndrome word contains an even number of 1s greater than 0 (2, 4, or 6).

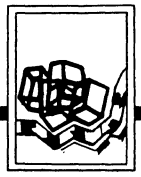
An ECC system implemented with the DP8400 can, at minimum, detect 100% of 2-bit errors; all of these errors are correctable if no more than one of them is soft. The device has complement write and read modes to allow the double complement correct technique to be used with no additional hardware, and other ECC devices can be used with additional components to implement the function.

In Fig 8, a soft error exists in location 5 and a hard error in location 9. During a memory read, the generated

The matrix or code is...a check bit generator for data, but a syndrome generator for error locations.

syndromes are the XOR of the single error that indicates syndrome words representing the error locations. 110001 (+) 001011 = 111010 [31 (+) 0B = 3A HEX]. Since a double error is indicated—an even number of 1s in the syndrome word—the data and check bits are complemented and placed in the output registers for presentation to the memory. After the memory write and subsequent read, the new data are complemented and stored in the data input latch. The error in location 5 remains in the data. A new set of check bits is generated from the data in the data input latch and compared with that in the check bit input latch, producing the syndrome word 110001 (31 HEX), which corrects the remaining error.

A detected double-bit error followed by a double complement correct cycle is properly reported as to initial error type. If the detected errors were both soft, for example, no change would occur in the data or check bit, and the ECC device error flags would again report a double-bit error. If, after the second read and complement, the error flags still report a single-bit error, the hard error (of a hard and soft combination) has been corrected and only the soft error remains. Of course, the single remaining error will be corrected in the normal manner by the ECC device. In the case of a double hard error, the error flags will report a no-error condition following the second read cycle, indicating that both errors were corrected and that the data are valid.



SPECIAL REPORT ON MEMORY SYSTEMS DESIGN

SIMPLIFICATION OF 2-BIT ERROR CORRECTION

Bit by bit, errors can be detected and eliminated through the use of an error matrix

by Bob Nelson

A computer-generated code, which generally obeys the rules attributed to the Hamming code and many of its variations, can be used to extend error detection and error correcting efficiency in an error checking and correction system. Such a code has been implemented by National Semiconductor on the DP8400, an expandable error checking and correction device packaged in a 48-pin dual inline package. The DP8400 can be used in a minimum hardware implementation of a 2-bit error correction system which will serve as an introduction to the rotational syndrome word generator, and also lead the way to expanding the error correcting capabilities even further.

Syndrome words

The code used in an error checking and correction (ECC) system designed to correct 1-bit errors and detect 2-bit errors for 16-bit data words may be viewed as a 16 x 6 matrix (Fig 1). The matrix describes the error locations and the syndrome bit positions so that the upper left bit of the matrix defines the least significant bit (LSB) for both the error locations and the syndrome bit locations. Each vertical column of the matrix contains the syndrome word (syndrome bits) for that error location in the data word. For any number of errors, the syndrome word generated by presenting the data word to the matrix is the exclusive OR (XOR) of the syndrome words defined by the error positions. To correct an error, the location of the error must be uniquely identified, and thus the 16 vertical columns must each be unique. A modified Hamming code generates a unique syndrome word for every possible data bit error location and hence may be referred to as a syndrome word generator.

Using syndrome words containing an odd number of 1s is the most common "modification" to the Hamming code. By ensuring that the syndrome words (vertical columns in the matrix) contain either three or five 1s, all applicable error conditions may be defined by counting the syndromes. The absence of a syndrome (ie, a syndrome containing all 0s and no 1s) indicates no error; an odd number greater than one (3 or 5 in this case) defines the location of a single-bit error. Any simultaneous double error will provide a syndrome word containing an even number of 1s greater than zero, while a single 1 in the syndrome word is indicative of a failure in the check bit portion of memory.

The rotational syndrome word generator described here also contains an odd number of 1s in each syndrome word. One additional characteristic common to both the Hamming code and most of its modified versions is that byte parity is an integral part of the matrix itself. However, the code implemented in the DP8400 ECC device and discussed here does not consider byte parity, or word parity, as a part of the code itself.

A 2-bit error correction system may be implemented in either of two ways. A code designed to allow 2-bit error correction may be used, or an existing single-bit error correct code may be extended by adding a second, different code which will ensure that each syndrome

Bob Nelson is responsible for digital systems applications and new product definition at National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. His engineering career began at the Burroughs Corp, where he worked on semiconductor memory systems and system interface design for large mainframe computers. Mr Nelson completed his basic engineering studies at Citrus College, Azusa, Calif, following undergraduate work at Pasadena City College.

Published in *Computer Design*, January, 1982.
Reprinted by permission.

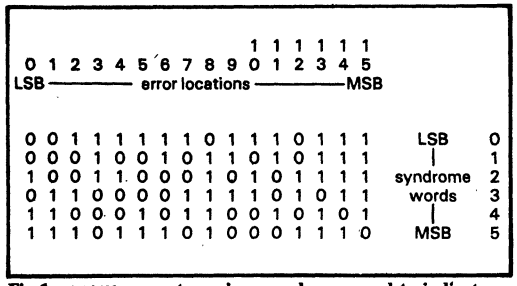


Fig 1 DP8400 generates unique syndrome word to indicate single-bit error position. Generated syndrome word containing all 0s means there is no error in data word.

word generated for any two error locations will be unique. Thus, a secondary, and different, 16 x 6 matrix connected to the primary matrix to form a 16 x 12 matrix will allow double-bit error correction if the XOR of the two 12-bit syndrome words produces a unique word for any two error locations.

Second matrix

The definition of an ECC matrix requires specifying a correspondence between error locations and syndrome words that defines the error location for each set of single-error syndromes. If a matrix is resequenced such that any error location corresponds to a syndrome word different from the original (primary) matrix, a second matrix has been created. For a 16-bit ECC matrix, 16!, or 2.092279 x 10^13, different codes exist. If a second code exists such that when it is combined with the first code (each containing the same syndrome words, but in a different sequence), a unique, larger syndrome word is generated for any two error locations, then an expandable code has been created (Fig 2).

The matrix, or code, used in the DP8400 device is defined such that if a second matrix, identical to the first but shifted by one bit position, is combined with the first, it would form just such a larger matrix. This matrix is fully rotational in that the secondary matrix need only be rotated, or shifted one error bit position to the left or right with respect to the primary matrix, to form larger, unique syndrome words regardless of the assigned correspondence of the primary matrix.

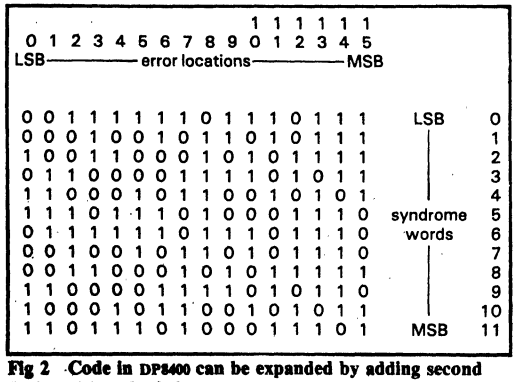


Fig 2 Code in DP8400 can be expanded by adding second device with code shifted by one bit position. Note that bottom six bits of each column are identical to top six bits in column to immediate right.

Implementation of this code in the DP8400 allows the data word size to be extended beyond 80 bits, using one device for each additional 16-bit word or portion thereof. The code function as a rotational syndrome word generator exists for all these defined word widths (Fig 3).

In addition to the rotational syndrome word generator, the DP8400 has two important features that permit an easy implementation of a 2-bit error correction system. During a memory read, the error indicating syndromes can be accessed directly by outputting them to the syndrome input/output (I/O) ports; syndrome can also be presented to the syndrome I/O ports to be XORed with the internally generated syndromes inside the DP8400. The internal syndrome decoder is provided with the result.

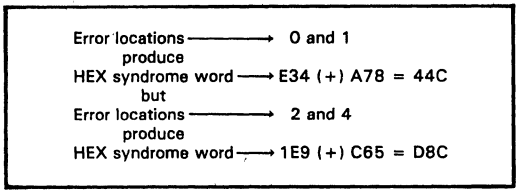


Fig 3 Unique syndrome is produced for each pair of error locations which is XOR of the locations. That syndrome can be decoded to identify pair in error.

If, for example, the internally generated 2-bit error syndromes are XORed with externally provided syndromes, representing one of the bits in error, the resulting syndromes representing the unknown error will be presented to the internal syndrome decoder. Once the unknown error is corrected, the data can be output to the data bus. The apparently correct data return zero syndromes (those containing all 0s) which, when XORed with the syndromes being injected, produce the syndromes representing the unknown error and present them to the syndrome decoder. This second error can then be corrected.

Using syndrome words containing an odd number of 1s is the most common "modification" to the Hamming code.

As described, the DP8400 is implemented for a 16-bit system. This "primary" ECC device will provide at its syndrome I/O pins the primary, or least significant six, syndrome bits of an extended matrix ECC system. A "secondary" ECC device is interfaced to the memory system with the data pin-to-system data bit correspondence rotated by one bit position, thus producing the extended matrix just described. The second device requires a second set of check bits; these secondary, or most significant six, syndrome bits are provided by the second DP8400.

The resulting 12-bit syndrome word can be externally decoded to provide the syndromes to be injected to effect 2-bit error correction. In system use, the externally decoded syndromes will be stored in a register. After the syndrome I/O port of the primary ECC device has been "turned around," the register outputs are enabled to allow syndrome injection.

Each of the DP8400 devices provides a set of error flags. Since each device maintains an independent check bit field in memory, errors occurring within a given check bit field are easily and quickly determined. If the errors, regardless of number, are confined solely to the check bit field of one of the devices, a no-error condition will be indicated.

The syndrome word generated by this system is unique for any combination of 2-bit data errors; both devices see an even number, greater than zero, of 1s in the syndrome word (Fig 4). For 2-bit errors involving one data bit and one check bit in either the primary or secondary check bit fields, the DP8400s report an even, greater than zero, and odd number of 1s in the syndromes; again, the syndromes are unique. The remaining type of 2-bit error, that in which both errors occur in either the primary or secondary check bit fields, produces its own unique syndrome word. However, since one DP8400 reports an even number of 1s in its syndrome word and the other reports all 0s, the data are known to be valid. In addition, in this particular 2-bit error correct system, nearly half of the 3-bit errors result in unique syndrome words and are therefore correctable as well.

Location/Error			Syndromes		Location/Error			Syndromes	
Data	Sec	Prim	Sec	Prim	Data	Sec	Prim	Sec	Prim
2	0	0	even	even	1	0	1	odd	even
1	1	1	even	even	2	1	0	odd	even
1	0	0	odd	odd	0	1	2	odd	even
0	1	1	odd	odd	1	1	0	even	odd
3	0	0	odd	odd	2	0	1	even	odd
1	0	2	odd	odd	0	2	1	even	odd
1	2	0	odd	odd					

Fig 4 Number and type of errors can be determined by looking at combination of even or odd numbers of 1s in the primary and secondary check bit fields.

Decoding the syndromes

A programmable read only memory (PROM) or electrically programmable read only memory (EPROM) is required as an external syndrome decoder for this 2-bit error correction system. The PROM address inputs are provided by the 12 syndrome bits generated by the two ECC devices. The least significant six bits of the PROM output byte provide, when required, the syndrome bits for subsequent injection into the primary DP8400. The remaining two bits of the PROM output byte provide flags defining the type of error and the contents of the six LSBs of the PROM output byte [Fig 5(a)].

The DP8400's error flags provide initial error determination; if an error that is not a single-bit error occurs, the external syndrome decoder will provide further error determination. Some types of error do not require syndrome injection and are referred to as "zero-pass" correctable errors. An example of such an error is one with a data bit and a secondary check bit in error. This type of error is corrected by the primary ECC device. An error type that requires "one-pass" correction is one with two data bits in error. In this case, syndromes representing a known error are injected into the DP8400, allowing correction of the unknown error. The remaining single error is then corrected.

The remaining error type, the "two-pass" error, can sometimes be a correctable 3-bit error. The syndromes representing a 2-bit error condition are injected, allowing correction of one error. The remaining 2-bit error produces a new set of syndromes which requires external (second-pass) decoding to produce a set of

MSB 7	6	5	4	3	2	1	LSB 0	
0	0	X	X	X	X	X	X	1 pass correctable
0	1	X	X	X	X	X	X	2 pass correctable
0	X	X	X	X	X	X	X	bits 0 to 5 = syndromes
1	0	X	X	X	X	X	X	not correctable
1	1	X	X	X	X	X	X	0 pass correctable
1	X	X	X	X	X	X	X	bits 0 to 5 < > syndromes

(a)

MSB 7	6	5	4	3	2	1	LSB 0	
1	X	X	X	X	X	X	1	primary check bit(s) in error
1	X	X	X	X	X	1	X	secondary check bit(s) in error
1	X	X	X	X	1	X	X	data bit(s) in error
1	X	X	0	0	X	X	X	1 bit in error
1	X	X	0	1	X	X	X	2 bits in error
1	X	X	1	0	X	X	X	3 bits in error
1	X	X	1	1	X	X	X	4 or more bits in error
1	1	0	X	X	X	X	X	output data from secondary ECC
1	1	1	X	X	X	X	X	output data from primary ECC

(b)

Fig 5 When a PROM is used as external syndrome decoder, its output byte can supply additional data about the error and how it is to be most efficiently corrected.

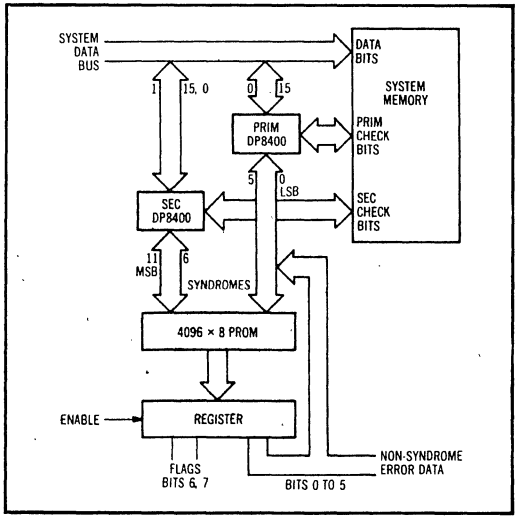


Fig 6 A 2-bit ECC system can be implemented with two DP8400s, a 4k-byte PROM for external syndrome decoding, and a register for temporary storage of syndromes error data. Note that the altered sequence of the lines from the secondary DP8400 reflects the bit rotation needed to expand the unique matrix.

```
3000 '*************************************************************************
3010 '***     'DC16AROM.BAS'          Bob Nelson - Sunnyvale CA - 9/15/81     ***
3020 '***     This program generates the syndrome decoder ROM code  for       ***
3030 '***     use in implementing a primary syndrome injection two  bit       ***
3040 '***     correction code generated by a single bit left   rotation       ***
3050 '***     of the secondary matrix.      The primary is a  Rotational      ***
3060 '***     Syndrome Generator as defined by National   Semiconductor      ***
3070 '***     in the DP8400.  The LPRINT routine may be replaced with a       ***
3080 '***     FILE generator or OUTP routine to facilitate the use of a       ***
3090 '***     PROM/EPROM programmer.....................................      ***
3100 '*************************************************************************
3110 '
3120 DEFINT A-Z:DIM SYND(16), PRI(16), ROM(4096,1)
3130 READ A:B=A:FOR C=0 TO 14:READ D:SYND(C)=D*64+A:PRI(C)=A:A=D
3140 NEXT:SYND(15)=B*64+A:PRI(15)=D
3150 DATA 52,56,41,7,37,49,35,25,62,11,13,19,44,55,47,31: 'NSC 80F/2 MATRIX
3160 ROM(0,1)=224:FOR A=1 TO 4095:ROM(A,1)=184:NEXT
3170 FOR A=0 TO 13:FOR B=A+1 TO 14:FOR C=B+1 TO 15                  '300 - 560
3180 AD=SYND(A) XOR SYND(B) XOR SYND(C):AE=PRI(A) XOR PRI(B)
3190 IF ROM(AD,1)=184 THEN ROM(AD,1)=AE+64 ELSE ROM(AD,1)=183
3200 NEXT:NEXT:NEXT
3210 FOR A=0 TO 14:FOR B=A+1 TO 15                                  '200 - 120
3220 AD=SYND(A) XOR SYND(B):ROM(AD,1)=PRI(A)
3230 FOR C=0 TO 5:P=2^C                                             '201 - 720
3240 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
3250 IF (PRI(A) AND P)=0 THEN AF=PRI(A)+P+64 ELSE AF=PRI(A)-P+64
3260 IF ROM(AE,1)=184 THEN ROM(AE,1)=AF ELSE ROM(AE,1)=183
3270 NEXT
3280 FOR C=0 TO 5:S=64*2^C                                          '210 - 720
3290 IF (AD AND S)=0 THEN AE=AD+S ELSE AE=AD-S
3300 IF ROM(AE,1)=184 THEN ROM(AE,1)=PRI(A) ELSE ROM(AE,1)=183
3310 NEXT:NEXT:NEXT
3320 FOR A=0 TO 15:AD=SYND(A):ROM(AD,1)=228                         '100 -  16
3330 FOR B=0 TO 5:P=2^B                                             '101 -  96
3340 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
3350 ROM(AE,1)=205
3360 FOR C=B+1 TO 5:P=2^C                                           '102 - 240
3370 IF (AE AND P)=0 THEN AF=AE+P ELSE AF=AE-P
3380 IF ROM(AF,1)=184 THEN ROM(AF,1)=213 ELSE ROM(AF,1)=183
3390 NEXT:NEXT
3400 FOR B=0 TO 5:S=64*2^B                                          '110 -  96
3410 IF (AD AND S)=0 THEN AE=AD+S ELSE AE=AD-S
3420 ROM(AE,1)=238
3430 FOR C=B+1 TO 5:S=64*2^C                                        '120 - 240
3340 IF (AE AND S)=0 THEN AF=AE+S ELSE AF=AE-S
3450 IF ROM(AF,1)=184 THEN ROM(AF,1)=245 ELSE ROM(AF,1)=183
3460 NEXT:NEXT
3470 FOR B=0 TO 5:P=2^B:FOR C=0 TO 5:S=64*2^C                       '111 - 596
3480 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
3490 IF (AD AND S)=0 THEN AE=AE+S ELSE AE=AE-S
3500 FOR D=0 TO 5:E=2^D
3510 IF ROM(AE,1)=D THEN ROM(AE,1)=183:GOTO 3540
3520 IF ROM(AE,1)=184 THEN ROM(AE,1)=P
3530 NEXT D
3540 NEXT C:NEXT B:NEXT A
3550 FOR A=0 TO 5:FOR B=0 TO 5                                      '011 -  36
3560 AD=2^A+64*2^B:ROM(AD,1)=235
3570 FOR C=A+1 TO 5:AE=AD+2^C                                       '012 -  90
3580 IF ROM(AE,1)=184 THEN ROM(AE,1)=243 ELSE ROM(AE,1)=183
3590 NEXT
3600 FOR C=B+1 TO 5:AE=AD+64*2^C                                    '021 -  90
3610 IF ROM(AE,1)=184 THEN ROM(AE,1)=243 ELSE ROM(AE,1)=183
3620 NEXT:NEXT:NEXT
3630 FOR A=0 TO 5:AD=2^A:ROM(AD,1)=225                              '001 -   6
3640 FOR B=A+1 TO 5:AE=AD+2^B:ROM(AE,1)=233                         '002 -  15
3650 FOR C=B+1 TO 5:AF=AE+2^C                                       '003 -  20
3660 IF ROM(AF,1)=184 THEN ROM(AF,1)=241
3670 NEXT:NEXT:NEXT
3680 FOR A=0 TO 5:AD=64*2^A:ROM(AD,1)=226                           '010 -   6
3690 FOR B=A+1 TO 5:AE=AD+64*2^B:ROM(AE,1)=234                      '020 -  15
3700 FOR C=B+1 TO 5:AF=AE+64*2^C                                    '030 -  20
3710 IF ROM(AF,1)=184 THEN ROM(AF,1)=242
3720 NEXT:NEXT:NEXT
3730 B=0:C=0:FOR A=0 TO 4095:H$=HEX$(ROM(A,1)):       'LPRINT ARRAY
3740 B=B+1:C=C+1:IF LEN(H$)=1 THEN H$="0"+H$
3750 LPRINT USING "\   \";H$;:IF C<>16 THEN 3770
3760 C=0:LPRINT"  ";HEX$(A)
3770 IF B<>256 THEN 3790
3780 B=0:LPRINT:LPRINT
3790 NEXT
```

```
1000 '*************************************************************************
1010 '***     'DC16AMAP.BAS'        Bob Nelson - Sunnyvale CA - 9/15/81     ***
1020 '***     This program generates the syndrome maps for  a  primary      ***
1030 '***     syndrome injection implementation of a 16 bit  word  two      ***
1040 '***     bit error correct system utilizing a Rotational Syndrome      ***
1050 '***     Word Generator as implemented in the DP8400 by  National      ***
1060 '***     Semiconductor.    These maps are based on single bit left     ***
1070 '***     rotation of the secondary matrix.  The 'c' and 'd' notes      ***
1080 '***     in the maps denote  non-correctable  and  non-detectable      ***
1090 '***     three bit error conditions.....................               ***
1100 '*************************************************************************
1110 '
1120 DEFINT A-Z:DIM SYND(16),PRI(16),ROM(1132,1):P$="PRIMARY":S$="SECONDARY"
1130 READ A:B=A:FOR C=0 TO 14:READ D:SYND(C)=D*64+A:PRI(C)=A:A=D
1140 NEXT:SYND(15)=B*64+A:PRI(15)=D
1150 DATA 52,56,41,7,37,49,35,25,62,11,13,19,44,55,47,31: 'NSC 80F/2 MATRIX
1160 LPRINT "ONE DATA ERROR SYNDROME MAP":LPRINT
1170 FOR A=0 TO 15:LPRINT USING"##";A;:LPRINT"  ";:NEXT:LPRINT:LPRINT
1180 FOR A=0 TO 15:LPRINT HEX$(SYND(A));" ";:NEXT:LPRINT
1190 FOR A=1 TO 4:LPRINT:NEXT
1200 LPRINT"TWO DATA ERROR CORRECT SYNDROME MAP":LPRINT
1210 FOR A=1 TO 15:LPRINT USING"##";A;:LPRINT"   ";:NEXT:LPRINT:LPRINT
1220 FOR A=0 TO 14:FOR B=A+1 TO 15:AD=SYND(A) XOR SYND(B)          '200 - 120
1230 ROM(X,1)=AD:H$=HEX$(AD):IF LEN(H$)=2 THEN H$="0"+H$
1240 LPRINT H$;"  ";:X=X+1:NEXT B:LPRINT USING"###";A
1250 LPRINT TAB((A+1)*5+1);:NEXT A:FOR A=1 TO 4:LPRINT:NEXT
1260 FOR A=0 TO 5:S=64*2^A:FOR B=0 TO 5:P=2^B:FOR C=0  TO 15       '111 - 576
1270 AD=SYND(C):IF (AD AND P)=0 THEN AD=AD+P ELSE AD=AD-P
1280 IF (AD AND S)=0 THEN AD=AD+S ELSE AD=AD-S
1290 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT:A$=" "
1300 LPRINT"ONE DATA, ONE PRI, ONE SEC CHECK ERROR SYNDROME MAPS":LPRINT
1310 LPRINT:X=120:FOR A=0 TO 5:LPRINT"SECONDARY CHECK BIT";A:LPRINT
1320 FOR F=0 TO 15:LPRINT USING"##";F;:LPRINT"  ";:NEXT F:LPRINT:LPRINT
1330 FOR B=0 TO 5:FOR C=0 TO 15:FOR E=0 TO 119
1340 IF ROM(E,1)=ROM(X,1) THEN A$="d":E0=E0+1:GOTO 1370 ELSE NEXT E
1350 FOR D=120 TO 695:IF D=X THEN D=D+1
1360 IF ROM(D,1)=ROM(X,1) THEN A$="c":E2=E2+1 ELSE NEXT D
1370 H$=HEX$ (ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
1380 LPRINT H$;A$;:X=X+1:A$=" ":NEXT C:LPRINT USING"####";B
1390 NEXT B:LPRINT:LPRINT:NEXT A
1400 LPRINT"576 ONE DATA, ONE PRI, ONE SEC CHECK errors are possible."
1410 LPRINT E0;"TWO DATA errors are not detectable.":LPRINT E2;
1420 LPRINT "ONE DATA, ONE PRI, ONE SEC CHECK errors are not correctable."
1430 LPRINT 100*((576-E0)/576):"PERCENT DETECT - ";
1440 LPRINT 100*((576-E0-E2)/576;"PERCENT CORRECT"
1450 FOR A=1 TO 4:LPRINT:NEXT:EA=E0:E0=0:EC=E2:E2=0
1460 X=0:FOR A=0 TO 15:AD=SYND(A):ROM(X,1)=AD:X=X+1:NEXT           '100 -  16
1470 FOR A=0 TO 5:P=2^A:FOR B=0 TO 5:S=64*2^B                      '011 -  36
1480 AD=P+S:ROM(X,1)=AD:X=X+1:NEXT:NEXT
1490 FOR A=0 TO 15:FOR B=A+1 TO 15:FOR C=B+1 TO 15                 '300 - 560
1500 AD=SYND(A) XOR SYND(B) XOR SYND(C)
1510 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT
1520 FOR A=0 TO 5:P0=2^A:FOR B=A+1 TO 5:P1=2^B                     '102 - 240
1530 FOR C=0 TO 15:AD=SYND(C):IF (AD AND P0)=0 THEN AD=AD+P0 ELSE AD=AD-P0
1540 IF (AD AND P1)=0 THEN AD=AD+P1 ELSE AD=AD-P1
1550 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT
1560 FOR A=0 TO 5:S0=64*2^A:FOR B=A+1 TO 5:S1=64*2^B               '120 - 240
1570 FOR C=0 TO 15:AD=SYND(C):IF (AD AND S0)=0 THEN AD=AD+S0 ELSE AD=AD-S0
1580 IF (AD AND S1)=0 THEN AD=AD+S1 ELSE AD=AD-S1
1590 ROM(X,1)=AD:X=X+1:NEXT:NEXT:NEXT
1600 LPRINT"THERE DATA BIT ERROR SYNDROME MAPS":LPRINT:LPRINT
1610 X=52:A$="  ":FOR A=0 TO 13:LPRINT"DATA bit";A:LPRINT
1620 FOR D=A+2 TO 15:LPRINT USING"##";D;:LPRINT"   ";:NEXT:LPRINT:LPRINT
1630 FOR B=A+1 TO 14:FOR C=B+1 TO 15:FOR E=16 TO 51
1640 IF ROM(E,1)=ROM(X,1) THEN A$="d ":E0=E0+1:GOTO 1690 ELSE NEXT E
1650 FOR F=612 TO 1091
1660 IF ROM(F,1)=ROM(X,1) THEN A$="c ":E1=E1+1:GOTO 1690 ELSE NEXT F
1670 FOR G=52 TO 611:IF G=X THEN G=G+1
1680 IF ROM(G,1)=ROM(X,1) THEN A$="c ":E2=E2+1 ELSE NEXT G
1690 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
1700 LPRINT H$;A$;:X=X+1:A$="  ":NEXT C:LPRINT USING "###";B
1710 LPRINT TAB((B-A)*5+1);:NEXT B:LPRINT:LPRINT:NEXT A
1720 LPRINT"560 THREE DATA BIT errors are possible.":LPRINT E0;
1730 LPRINT"ONE PRI, ONE SEC CHECK errors are not detectable.":LPRINT E1;
1740 LPRINT"ONE DATA, TWO PRI or TWO SEC CHECK errors are not correctable."
1750 LPRINT E2;"THREE DATA BIT errors are not correctable."
1760 LPRINT 100*((560-E0)/560);"PERCENT DETECT - ";
1770 LPRINT 100*((560-E0-E1-E2)/560);"PERCENT CORRECT"
1780 FOR A=1 TO 4:LPRINT:NEXT A:EA=EA+E0:EB=EB+E1:EC+EC+E2
1790 LPRINT"ONE DATA, TWO PRIMARY CHECK ERROR SYNDROME MAPS":LPRINT:LPRINT
1800 A$=" ":E0=0:E1=0:E2=0:FOR A=0 TO 4:LPRINT"PRIMARY check bit";A:LPRINT
1810 FOR F=0 TO 15:LPRINT USING "##";F;:LPRINT"  ";:NEXT F:LPRINT:LPRINT
1820 FOR B=A+1 TO 5:FOR C=0 TO 15:FOR E=852 TO 1091
```

```
1830 FOR F=52 TO 611
1840 IF ROM(F,1)=ROM(X,1) THEN A$="c":E2=E2+1:GOTO 1860 ELSE NEXT F
1850 IF ROM(E,1)=ROM(X,1) THEN A$="c":E1-E1+1 ELSE NEXT E
1860 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
1870 LPRINT H$;A$;:X=X+1:A$=" ":NEXT C:LPRINT USING "####";B
1880 NEXT B:LPRINT:LPRINT:NEXT A
1890 LPRINT"240 ONE DATA, TWO PRIMARY CHECK errors are possible."
1900 LPRINT E1;"ONE DATA, TWO SECONDARY CHECK errors are not correctable."
1910 LPRINT E2;"THREE DATA BIT errors are not correctable."
1920 LPRINT"100 PERCENT DETECT - ";100*((240-E1-E2)/240);"PERCENT CORRECT"
1930 FOR A=1 TO 4:LPRINT:NEXT A:EB=EB+E1+E2:E1=0:E2=0
1940 LPRINT"ONE DATA, TWO SECONDARY CHECK ERROR SYNDROME MAPS":LPRINT
1950 LPRINT:FOR A=0 TO 4:LPRINT"SECONDARY check bit";A:LPRINT
1960 FOR F=0 TO 15:LPRINT USING "##";F;:LPRINT"  ";:NEXT F:LPRINT:LPRINT
1970 FOR B=A+1 TO 5:FOR C=6 TO 15:FOR E=612 TO 851
1980 FOR F=52 TO 611
1990 IF ROM(F,1)=ROM(X,1) THEN A$="c":E2=E2+1:GOTO 2010 ELSE NEXT F
2000 IF ROM(E,1)=ROM(X,1) THEN A$="c":E1=E1+1 ELSE NEXT E
2010 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
2020 LPRINT H$;A$;:X=X+1:A$=" ":NEXT C:LPRINT USING "####";B
2030 NEXT B:LPRINT:LPRINT:NEXT A
2040 LPRINT"240 ONE DATA, TWO SECONDARY CHECK errors are possible."
2050 LPRINT E1;"ONE DATA, TWO PRIMARY CHECK errors are not correctable."
2060 LPRINT E2;"THREE DATA BIT errors are not correctable."
2070 LPRINT"100 PERCENT DETECT - ";100*((240-E1-E2)/240);"PERCENT CORRECT"
2080 FOR A=1 TO 4:LPRINT:NEXT A:EB=EB+E1+E2:A$="  ":C0=1:C1=64
2090 IF W=1 THEN P$="SECONDARY":S$="PRIMARY":C0=64:C1=1
2100 X=0:FOR A=0 TO 15:AD=SYND(A):FOR B=0 TO 5:P=C0*2^B        '101/110 -  96
2105 IF (AD AND P)=0 THEN AE=AD+P ELSE AE=AD-P
2110 ROM(X,1)=AE:X=X+1:NEXT B:NEXT A
2120 FOR A=0 TO 5:S=C1*2^A:FOR B=0 TO 15:FOR C=B+1 TO 15       '210/201 - 720
2130 AD=SYND(B) XOR SYND(C):IF (AD AND S)=0 THEN AE=AD+S ELSE AE=AD-S
2140 ROM(X,1)=AE:X=X+1:NEXT C:NEXT B:NEXT A
2150 FOR A=0 TO 5:AD=C1*2^A:FOR B=0 TO 4:AE=AD+C0*2^B          '012/021 -  90
2160 FOR C=B+1 TO 5:ROM(X,1)=AE+C0*2^C:X=X+1:NEXT:NEXT:NEXT
2170 A$="  ":LPRINT"TWO DATA, ONE ";:LPRINT S$;
2180 LPRINT" CHECK ERROR SYNDROME MAPS":LPRINT:LPRINT
2190 X=96:E0=0:E1=0:E2=0:FOR A=0 TO 5:LPRINT S$;
2200 LPRINT" check bit";A:LPRINT
2210 FOR F=1 TO 15:LPRINT USING"##";F;:LPRINT"   ";:NEXT F:LPRINT:LPRINT
2220 FOR B=0 TO 14:FOR C=B+1 TO 15;FOR D=0 TO 95
2230 IF ROM(D,1)=ROM(X,1) THEN A$="d ":E0=E0+1:GOTO 2280 ELSE NEXT D
2240 FOR G=96 TO 815:IF G=X THEN G=G+1
2250 IF ROM(G,1)=ROM(X,1) THEN A$="c ":E2=E2+1:GOTO 2280 ELSE NEXT G
2260 FOR E=816 TO 905
2270 IF ROM(E,1)=ROM(X,1) THEN A$="c ":E1+E1+1 ELSE NEXT E
2280 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
2290 LPRINT H$;A$;:X=X+1:A$="  ":NEXT C:LPRINT USING"####";B
2300 LPRINT TAB((B+1)*5+1);:NEXT B:LPRINT:LPRINT:NEXT A
2310 LPRINT"720 TWO DATA, ONE ";:LPRINT MID$(S$,1,3);
2320 LPRINT" CHECK errors are possible."
2330 LPRINT E0;"ONE DATA, ONE ";:LPRINT MID$(P$,1,3);
2340 LPRINT" CHECK errors are not detectable.":LPRINT E1;"TWO ";
2350 LPRINT MID$(P$,1,3);:LPRINT", ONE ";:LPRINT MID$(S$,1,3);
2360 LPRINT" CHECK errors are not correctable."
2370 LPRINT E2;"TWO DATA, ONE ";:LPRINT MID$(S$,1,3);
2380 LPRINT" CHECK errors are not correctable."
2390 LPRINT 100*((720-E0)/720);"PERCENT DETECT - ";
2400 LPRINT 100*((720-E0-E1-E2)/720);"PERCENT CORRECT"
2410 FOR A=1 TO 4:LPRINT:NEXT:EA=EA+E0:EB=EB+E1:EC=EC+E2
2420 LPRINT"TWO ";:LPRINT MID$(P$,1,3);:LPRINT", ONE ";:LPRINT MID$(S$,1,3);
2430 LPRINT" CHECK ERROR SYNDROME MAPS":LPRINT:LPRINT
2440 X=816:E0=0:E1=0:E2=0:FOR A=0 TO 5:LPRINT S$;
2450 LPRINT" check bit";A:LPRINT
2460 FOR F=1 TO 5:LPRINT USING "##";F;:LPRINT"   ";:NEXT F:LPRINT:LPRINT
2470 FOR B=0 TO 4:FOR C=B+1 TO 5
2480 FOR D=96 TO 815:IF ROM(D,1)=ROM(X,1) THEN A$="c ":E1=E1+1 ELSE NEXT D
2490 H$=HEX$(ROM(X,1)):IF LEN(H$)=2 THEN H$="0"+H$
2500 LPRINT H$;A$;:X=X+1:A$="  ":NEXT C:LPRINT USING"##";B
2510 LPRINT TAB((B+1)*5+1);:NEXT B:LPRINT:LPRINT:NEXT A:LPRINT"90 TWO ";
2520 LPRINT MID$(P$,1,3);:LPRINT", ONE ";:LPRINT MID$(S$,1,3);
2530 LPRINT" CHECK errors are possible.":LPRINT E1;"TWO DATA, ONE ";
2540 LPRINT MID$(S$,1,3);:LPRINT" CHECK errors are not correctable."
2550 LPRINT"100 PERCENT DETECT - ";100*((90-E1)/90);"PERCENT CORRECT"
2560 FOR A=1 TO 4:LPRINT:NEXT A:EA=EA+E0:EB=EB+E1:EC=EC+E2
2570 IF W=0 THEN W=1:GOTO 2090
2580 FOR A=1 TO 4:LPRINT:NEXT
2590 LPRINT"3290 THREE BIT ERRORS (all types) are possible."
2600 LPRINT EA;"of these errors cannot be detected."
2610 LPRINT EB+EC;"of these errors cannot be located."
2620 LPRINT 100*((3290-EA)/3290);"PERCENT DETECT - ";
2630 LPRINT 100*((3290-EA-EB-EC)/3290);"PERCENT CORRECT"
```

single-bit error syndromes. The error status at this point is that of a "one pass" error, and correction proceeds accordingly.

When a zero-pass error or a noncorrectable error occurs, the six LSBs from the PROM provide additional information. For example, a hexadecimal coded output from the PROM [Fig 5(b)] defines a 2-bit error in which one bit in error is a data bit and the other a primary check bit. The primary ECC device detects a 2-bit error while the secondary device detects only the data bit in error. Bit 5 of the PROM output directs the secondary device to output corrected data to the system. In most cases, bit 5 is a 1, and corrected data are output from the primary ECC device. Bits 0 through 4 of the PROM output define the error type and the number of bits in error (Fig 6) when the MSB (bit 7) is a 1. When the MSB is a 0, syndromes are required for correction, and bits 0 through 5 represent those syndromes.

Some types of error do not require syndrome injection and are referred to as "zero-pass" correctable errors.

The first of the two programs provided here is called "DC16AROM.BAS," and is a listing in hexadecimal representing the contents of the syndrome decoding PROM. The file may be presented to an output port for loading a PROM programmer if minor program changes are made. The second program, called "DC16AMAP.BAS," generates all the required syndrome maps, which include flags for all correctable 3-bit errors. These programs were written in Microsoft Basic and are compilable.

EFFORTLESS ERROR MANAGEMENT

Basic application of error management techniques is based on error history, including the double complement error correction cycle

by Bob Nelson

When implemented only in hardware, error management is generally limited to simple error logging. In most systems, error logging hardware is designed to capture the location of one error and use this information for maintenance purposes. In more sophisticated systems, however, software extends the error management function: after hardware obtains error information, data are accumulated on disk to expand storage capacity for information relating to error locations. Beyond the error information storage function of error management, which is useful for maintenance, some systems implement a correction procedure based on error history. If two errors occur in a memory word where an error has previously occurred, it is likely that both errors can be corrected. The basic error management system described in this article will provide a high correction rate for all 2-bit errors, except when two soft errors simultaneously occur in a memory word with no error history.

Error management system

The error management system comprises the central processing unit (CPU), the system memory, an error checking and correction (ECC) device, and an error management unit (EMU). The CPU is a 16-bit machine and requires commensurate memory. Actual memory, including the six check bits that the ECC device requires, is 22 bits wide. The ECC device is based on the DP8400 monolithic ECC unit manufactured by National Semiconductor. The EMU is a hypothetical device that can be implemented in hardware, partially or entirely, depending on system requirements.

The DP8400 provides several functions and features that allow easy implementation of a minimum hardware error management system. Error indicating syndrome words must be available to the EMU directly and syndrome injection capability must exist. (See "Simplification of 2-Bit Error Correction," Jan 1982, pp 127-136, for a discussion of the DP8400's syndrome input/output ports.) The DP8400 also provides the hardware required to perform a double complement correct cycle. Error flags must be provided to discriminate between 2-bit and detectable 3-bit errors; the DP8400 provides three such flags to include this function.

Vertical columns in the matrix shown in Fig 1 represent the single data bit error indicating syndrome words. A double data bit error syndrome word results from exclusive ORing (XOR) the two single-bit error indicating syndrome words that correspond to the bit locations in error. A detectable triple data bit syndrome word is any one of the ten syndrome words, not included as part of the matrix, which contains either three or five 1s. Syndrome words that represent check bit errors contain 1s in the syndrome word bit positions corresponding to the check bits in error, and 0s in the remaining bit positions. An error condition involving the data and check bit fields provides a syndrome word that represents the data bit(s) in error, XORed with a syndrome word representing the check bit(s) in error.

Error management unit

The EMU is memory intensive and uses memory in the form of an associative stack. Three fields constitute each of the 16 words in the stack: the 8-bit address field, which is the associative portion of the word; the 2-bit

Bob Nelson is responsible for digital systems applications and new product definition at National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. His engineering career began at the Burroughs Corp, where he worked on semiconductor memory systems and system interface design for large mainframe computers. Mr Nelson completed his basic engineering studies at Citrus College, Azusa, Calif, following undergraduate work at Pasadena City College.

Published in *Computer Design*, February, 1982.
Reprinted by permission.

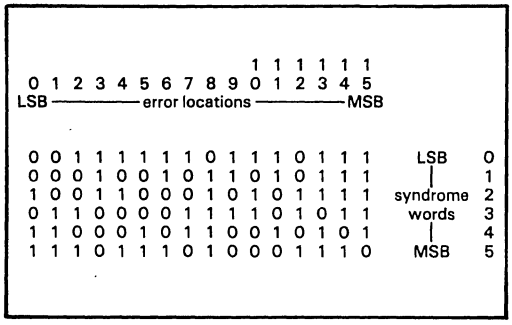


Fig 1 DP8400 syndrome word generator. Presenting errors to unique matrix produces syndrome words.

tag field; and the 6-bit syndrome field (Fig 2). The pointer addresses the stack. The EMU also contains a syndrome comparator, a temporary syndrome register, and a tag bit attribute register and comparator. The EMU monitors most ECC flags and provides flags of its own both to the ECC device and to the CPU; monitoring the memory address and comparing that address to the

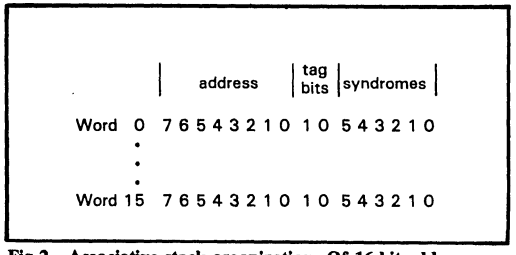


Fig 2 Associative stack organization. Of 16-bit address, eight address bits are most significant bits. Tag bits indicate type of error, and syndrome bits contain syndrome word.

stack's address field is a major function of the EMU. When the "stack full" flag is off, however, the number of words in the match area is limited by the location of the stack pointer. If a match occurs, ie, if the current memory address is an address at which an error occurred previously, the information obtained from the previous error can be used to correct more than one error bit. Each EMU function will be defined in a subsequent section of this article.

Single-bit error: first occurrence

Absence of a match, accompanied by single-bit error indicating flags, defines the first occurrence of such an error in the current address. The error may be in the data bit or check bit field of memory. Error address, tag bits (Fig 3), and single-bit error indicating syndrome word are stored in the EMU stack. Tag bits are assigned a value of 00, indicating a soft single-bit error. The stack pointer is then incremented and the ECC device corrects the single-bit error in the usual way. Stored syndromes contain an odd number of 1s. In Fig 4, data bit 5 fails at memory address 52 HEX, check bit 3 fails at address 45 HEX, and data bit 9 fails at address C7 HEX. Since the errors have not occurred previously at these addresses, they are given a tag bit value of 00. Logging errors should not impact the speed or function of the ECC system in performing single-bit error correction.

Tag Bits	Information Status
00	soft single-bit error
01	firm single-bit error
10	hard single-bit error
11	hard double-bit error

Fig 3 Tag bit field of stack indicates error type for more efficient processing by error management system. Tag bit field could be extended in other systems to provide more error information.

Double-bit error: first occurrence

When a double-bit error occurs at an address with no error history, the EMU exercises the only available option, a double complement correct cycle. As the ECC device enters the complement write mode, the syndrome word that represents the double-bit error condition is stored in the temporary syndrome register. Then the ECC system performs a double complement correct cycle to generate a second set of error flags. If two soft errors caused the initial indication of a 2-bit error, the second set of error flags will also indicate two errors and represent a noncorrectable condition. Any double-bit error situation other than that of two soft errors will produce error flags that indicate a correctable condition at the conclusion of the double complement correct cycle.

One hard and one soft

Error flags produced after the second complement of the double complement correct cycle indicate a single error if the initial error condition was one hard and one soft. At that point, the hard error will have been "corrected" and the remaining soft error indicated. The ECC device will generate a new single-bit error indicating syndrome word, which the EMU will XOR with the previously stored double-bit error indicating syndrome word. The result, which is the single-bit hard error indicating syndrome word, is stored in the stack.

To identify the bit as a single hard error, the tag bit field is set to a value of 10. After the error information is stored, the stack pointer is incremented. The ECC device corrects the single error in the usual manner. The remaining soft error may be either a check bit error or a data bit error. Fig 5 illustrates a soft error in data bit location 2 and a hard error in data bit location 11. A double complement cycle corrects the error in location 11. Representing the soft error, a new syndrome word is then XORed with the original syndrome word to produce

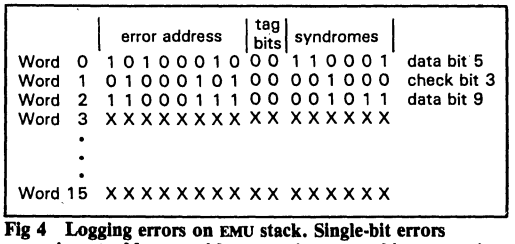


Fig 4 Logging errors on EMU stack. Single-bit errors occurring at addresses with no previous error history receive tag bit value of 00.

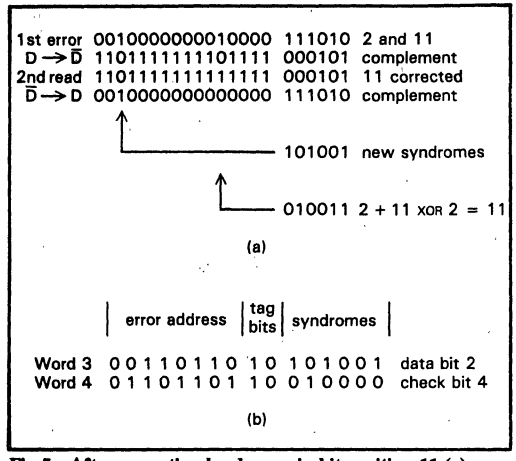


Fig 5 After correcting hard error in bit position 11 (a), system stores hard error syndrome on associative stack (b) and sets tag bit field to indicate single-bit hard error.

	error address	tag bits	syndromes	
Word 0	1 0 1 0 0 0 1 0	0 0	1 1 0 0 0 1	data bit 5
Word 1	0 1 0 0 0 1 0 1	0 0	0 0 1 0 0 0	check bit 3
Word 2	1 1 0 0 0 1 1 1	0 0	0 0 1 0 1 1	data bit 9
Word 3	0 0 1 1 0 1 1 0	1 0	1 0 1 0 0 1	data bit 2
Word 4	0 1 1 0 1 1 0 1	1 0	0 1 0 0 0 0	check bit 4
Word 5	1 0 0 0 0 1 0 0	1 1	1 0 1 0 0 0	2 hard
Word 6	X X X X X X X X	X X	X X X X X X	
•				
•				
•				
Word 15	X X X X X X X X	X X	X X X X X X	

Fig 6 Contents of EMU's stack containing initial occurrence of each error type.

the syndrome word that represents the hard error. These hard error syndromes are stored as shown in Fig 6, which also shows the storage of a hard check bit error at address 6D HEX.

Two hard

An ECC "no-error" flag, following a double complement correct cycle, indicates an initial error condition of two hard errors. Data following the second complement are correct; since no error exists, a syndrome word of all zeros is generated. The EMU will store the error address, the tag bits, and the contents of the temporary register. Tag bits will be given a value of 11, indicating a double-bit hard error. The stored syndrome word is then XORed with the contents of the temporary syndrome register and the new syndrome word from the ECC device (as with a one soft/one hard error condition), and the stack pointer is incremented. In this example, the information obtained from a double-bit hard error at address 84 HEX, including a syndrome word of 101000, is stored. A 2-bit error indicating syndrome word provides no information regarding the location of the errors. Errors in data bit locations 13 and 15, for example, produce the stored syndrome word as would errors in check bit locations 3 and 5. Fig 6 illustrates the contents of the associative stack portion of the EMU following the first occurrence of each type of error discussed. Word 5 in the stack represents the double-bit hard error.

Logging the errors

As errors occur at new addresses, error data are stored in the stack and the stack pointer is incremented. When information is entered in stack word 15 a "stack full" flag is set. The stack full flag directs the pointer to the lowest word address location in the stack containing the value 00 in the tag bit field. After storing data, the stack pointer goes to the next highest word address location that contains a 00 in the tag bit field. The stack contains the most recent error addresses at which single-bit soft errors occurred and all addresses at which firm or hard errors occurred. When no tag bit field contains 00, the "overflow" flag is provided and no additional stack storage occurs. However, logged error information is available to the system. One of the DP8400 modes, for example, allows data to be provided to the syndrome input/output ports and output through the data input/output ports, a capability that allows the error information to be dumped to the system disk for an additional level of storage. In another mode, the DP8400 can internally transfer data from the data input to the syndrome output, allowing the stack to be loaded from the system disk via the data bus.

Error locations are stored in real time by the logging procedure. Error resolution is defined by the correspondence of the memory address bits to the EMU address inputs. The EMU described here has eight address inputs that allow chip level error resolution in a 1M-byte memory system when 64k-bit dynamic random access memories are used. Since the EMU does not monitor the least significant eight memory address lines, error information—specifically the address and syndromes as stored in the EMU—represents a memory chip location. If a "read error" match occurs, only the tag bits and/or the stored syndrome word may be updated. Therefore, each unique error address can exist in a single stack location. Each stored word location defines one defective bit (chip) location if the syndrome word indicates a single-bit error. In some cases, the error information will represent two hard errors, which normally cannot be located.

Relocating the errors

In response to new error information, it may be desirable to change the error locations as defined by the syndrome words stored in the EMU. If a single-bit error is accompanied by an address match and tag bits representing a stored single-bit soft error, but if the syndrome comparison indicates that a different bit is in error, the syndrome field of the matching stack word should be changed to the new syndrome word. The ECC will correct the single-bit error in the normal manner, and the most recent soft error information for that memory address will be maintained. Previous soft error information can be off-loaded to a secondary storage device prior to the update.

Stored Error	Tags	Detected Error
1 bit, firm	01	1 soft, 1 hard
1 bit, hard	10	1 soft, 1 hard
1 bit, soft	00	1 soft, 1 hard
1 bit, soft	00	2 soft
1 bit, firm	01	2 hard
1 bit, hard	10	2 hard

Fig 7 Errors for syndrome injection in order of probability. Syndrome injection in the DP8400 allows faster correction than double complement method.

Maintenance help
Maintenance tools are a by-product of the EMU system. During the ECC procedure, error locations are identified and error types determined. EMU generated flags, which are provided when the stack contents reach a defined level, allow the error information to be offloaded to the system disk and the EMU to be cleared and reloaded with selected error information from disk. After the error information is loaded on disk, the system can be powered-down for maintenance. Following system power-up, suspect information about error location may be written to the EMU. This extended logging capability is part of the total error management system.

Redefinition
When a single-bit error occurs in a location at which a single-bit error has occurred previously, and the stored syndrome word is the same as the single-bit error indicating syndrome word generated by the ECC device, it may be necessary to redefine the error type. If the match provides tag information indicating a soft error (tag field = 00), the tag field will be changed to 01 to indicate a single-bit firm error. Such a redefinition is valid. For instance, a firm error may be an unproved hard error or an error-prone memory device sensitive to alpha particles, system noise, or both. Such an error can be treated as either a soft error or a hard error, or be given a definition based on the present error. For the purpose of this discussion, a firm error will be treated as a hard error.

With...double complement correct cycles, 100% of 2-bit errors can be corrected when...one of the errors is hard, regardless of...error history.

Although a soft error can occur in any given location within a chip, a second soft error is most likely to occur within the same chip. Error-prone chips are identified and tagged as firm error locations. In the EMU, both the syndromes and the address field are compared, providing higher error resolution within a word. In this EMU, the tag bit field is updated and the syndrome field is rewritten (if the second error is not in the same chip, the most recent single-bit error location in that word will be stored). The ECC device corrects the single-bit error in the normal manner.

Double-bit error: subsequent occurrence
When a double-bit error occurs and the EMU obtains a match, the contents of the tag bit field dictate the possible courses of action (Fig 7). If the tag bits are 11, for example, a double complement correct cycle is the only option. If the tag bits indicate a single-bit hard error location, a double complement correct cycle could be implemented. On the other hand, it is reasonable to assume that the stored syndrome word represents one of the two present error locations; in that case the error can be corrected without additional memory cycles.

One hard—one soft, one hard
If a match is obtained, tag bits are 10, and a 2-bit error has been detected, it is most likely that one error is soft and the other hard. Syndrome injection will obtain the fastest correction. The syndrome word in the stack, which usually represents the hard error location, is presented to the DP8400. There it is XORed with the internally generated syndrome word to provide the resulting soft error syndrome word, which is then presented to the syndrome decoder. After the ECC device corrects the soft error, it generates new check bits and zero syndromes. XORing the new syndromes with the still-injected hard error syndrome word, the unit decodes the hard error location and corrects the second error. This procedure allows correction of 2-bit errors without additional memory cycles, once the location of the hard error has been determined. Although a firm error is treated as a hard error, it must be given special consideration during system maintenance.

One soft—one soft, one hard
If a 2-bit error is detected and a match obtained with a tag of 01, the highest probability is that one error is soft and one is hard. The syndrome word from the stack is injected into the DP8400, where it is XORed with the internally generated syndrome word, providing the result to the syndrome decoder. Correcting the soft error, the ECC device generates new check bits and syndromes, XORs the new syndromes with the still-injected hard error syndrome word provided by the EMU, decodes the known error location, and corrects it. When the location of one error has been determined, this procedure allows high speed correction of 2-bit errors without additional memory cycles.

One soft—two soft
If a match is obtained, tag bits are 01, and a 2-bit error is detected, both errors are probably soft and can be corrected by syndrome injection. The syndrome word in the stack (which often represents one of the soft error locations) is presented to the DP8400, where it is XORed with the syndrome word, generated internally to provide the unknown soft error syndrome word to the syndrome decoder. Correcting the soft error, the ECC device generates new check bits and zero syndromes. XORing the new syndromes with the still-injected "known" soft error indicating syndrome word, it decodes the error location and corrects the second error. Thus, two soft errors can be corrected if the location of one is known.

One firm or hard—two hard
If two hard errors occur at an address where a single-bit hard error has been recorded previously, syndrome injection will usually accomplish the correction. The syndrome word in the stack, which most likely represents one of the hard error locations, is presented to the DP8400 where it is XORed with the internally generated syndrome word, providing the result to the syndrome decoder. The ECC device corrects the first error and generates new check bits and zero syndromes. XORing the new syndromes with the still-injected "known"

error indicating syndrome word, the unit corrects the second error. This procedure allows high speed correction of two hard errors when the location of one is known.

Double complement

The double complement error correction cycle is effective for locating hard errors in an error management system. This technique is effective when speed of error correction is of less concern than system integrity. Use of the double complement correct cycle following the detection of every error enhances error determination and correction. Immediate determination of single-bit hard errors improves the possibility that double-bit errors in the same defined address can be corrected. The next level of error detection and correction efficiency, using the double complement correct cycle for each detected error, includes those error types noted in Fig 8.

Stored Error	Tags	Detected Error
1 bit, soft	00	2 hard
1 bit, firm	01	2 soft
1 bit, hard	10	2 soft

Fig 8 Errors for double complement correction. When speed is of less priority, double complement method allows more precise error detection, logging, and correction.

One soft—two hard

A no-error indication from the ECC device following the double complement correct cycle will complete the definition of the error type—defined as a 2-bit error by the syndrome word stored in the temporary syndrome register—as a 2-bit hard error. If a match occurs but the tag bit field indicates a single-bit soft error, the tag bit field can be changed to 11, indicating two hard errors, and the syndrome field replaced with the contents of the temporary syndrome register. Error information can be offloaded to a secondary storage device before this update.

One firm or hard—two soft

If the ECC device generates error flags indicating a double-bit error at the conclusion of the double complement correct cycle, the 2-bit error that instigated the cycle remains and contains two soft errors. Since the only recorded error at the current memory location is hard, the errors are not recoverable and system operation terminates. In some systems, a firm error may be defined as a soft error, and data may be recovered. When offloading of soft errors is practiced, the disk or other storage mechanism can be interrogated for prior memory errors at the current address. These soft errors can be corrected if proper information is available.

Two hard—double error

When a match occurs and the tag bits indicate that an earlier 2-bit error has been recorded for the present memory address, ECC device's error flags identify the error type after the double complement correct cycle. If the present error is soft, system operation must be terminated—assuming that no additional relevant information regarding errors at this address is available from other sources. If the second set of error flags indicates that the present error is a 2-bit hard error, the errors can be corrected. Comparing the syndrome words in the temporary syndrome register and the stack will provide additional information. If the syndrome words do not match, three or four hard errors exist and system operation must be terminated.

Locating two hard errors

When the presence of two hard errors has been determined, a subsequent access at the same address will most likely indicate a single-bit error. If the single-bit error is in one of the two locations that had defined the previous 2-bit hard error, adequate information is available to locate the other error. The temporary syndrome register will store the single-bit error indicating syndrome word. Data are corrected by the double complement correct cycle, and the syndrome word in the stack can be replaced by the contents of the temporary syndrome register. The double-bit hard error indicating syndrome word can be offloaded and the word replaced. The new word will then be offloaded and XORed with the first syndrome word, keeping the result in the secondary storage element. Secondary storage is available for interrogation if additional errors occur in the same address. In more sophisticated error management systems, additional tag bits are made available in the EMU stack. One of these tag bits can be used to indicate that additional error information exists in secondary storage for that error address.

Summary

The simplified error management system presented here allows correction of double-bit errors if one of the errors has previously occurred. With the use of double complement correct cycles, 100% of 2-bit error correction is provided when at least one of the errors is hard, regardless of previous error history. Enhanced error logging is provided with error type determination capability. Maintenance aids are provided through the DP8400's bidirectional data transfer capability between the syndrome input/output and data input/output ports.

National Semiconductor

Dynamic Memory Support
PRELIMINARY

DP84300 Programmable Refresh Timer

General Description

The DP84300 programmable refresh timer is a logic device which produces the desired refresh clock required by all dynamic memory systems.

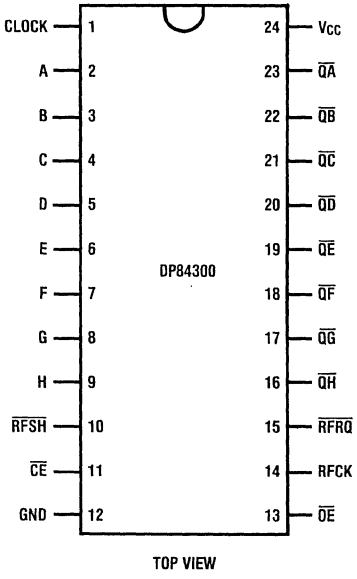
Additional circuitry has been included in the device to minimize logic required by memory systems to perform refresh control.

Features

- One chip solution to produce RFCK timing for the DP8408 and DP8409 dynamic RAM controllers
- Programmable refresh clock timer allows for a maximum refresh period with most system clocks
- Timing is completely synchronous with the input clock, preventing race conditions present in some memory controllers
- Includes a refresh request output, simplifying the design of refresh logic in discrete controllers

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DP84300N-3
See NS Package N24C

Block Diagram

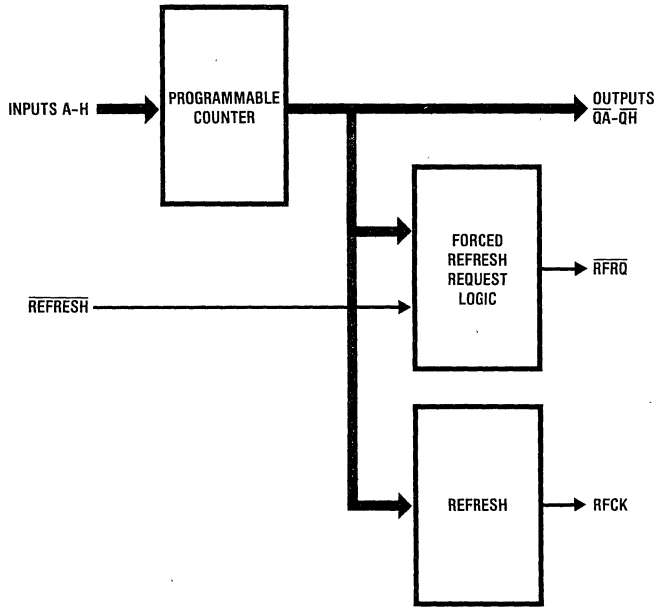


FIGURE 1

7

Recommended Operating Conditions (Commercial)

	Min	Typ	Max	Units
V_{CC}, Supply Voltage	4.75	5.00	5.25	V
I_{OH}, High Level Output Current			−3.2	mA
I_{OL}, Low Level Output Current			16	mA
T_A, Operating Free Air Temperature	0		75	°C

Electrical Characteristics over recommended operating temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5	V
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 2.4V, V_{IL} = 0.8V			100	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 0.4V, V_{IL} = 0.8V			−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−250	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max		150	180	mA

DP84300-3 Switching Characteristics over recommended ranges of temperature and V_{CC}

Symbol	Parameter		Conditions R_L = 667Ω	Commercial T_A = 0°C to +75°C V_{CC} = 5.0V ± 5%			Units
				Min	Typ	Max	
t_{PD}	Clock to Output		C_L = 45 pF		15	25	ns
t_{PZX}	Pin 13 to Output Enable		C_L = 45 pF		15	25	ns
t_{PXZ}	Pin 13 to Output Disable		C_L = 5 pF		15	25	ns
t_{PZX}	Input to Output Enable		C_L = 45 pF		25	35	ns
t_{PXZ}	Input to Output Disable		C_L = 5 pF		25	35	ns
t_W	Width of Clock	High		25			ns
		Low		25			ns
t_{su}	Set-Up Time			35			ns
t_H	Hold Time			0	−15		ns

Mnemonic Description

INPUT SIGNALS

CLOCK — Provides a time base for the programmable divider.

A-H — Program inputs A through H. These inputs select the number of clock cycles that will produce one refresh period. These inputs are binary encoded, with input A the LSB, and H the MSB. Additionally, all zeros produce the maximum count of 256, and an input of one will reset the counter to one.

$\overline{\text{REFRESH}}$ — This input is used to reset the refresh request output ($\overline{\text{RFRQ}}$).

$\overline{\text{OE}}$ — Output enable. Places the outputs in TRI-STATE®.

$\overline{\text{CE}}$ — Counter enable. This input, when low, enables the timer clock and, when high, stalls the timer.

OUTPUT SIGNALS

$\overline{\text{QA}}$-$\overline{\text{QH}}$ — Refresh timer outputs $\overline{\text{QA}}$ through $\overline{\text{QH}}$. Timer starts at programmed input and counts down to one.

$\overline{\text{RFRQ}}$ — Refresh request. This output goes low on the rising edge of the refresh clock (RFCK). The first input clock edge after the $\overline{\text{REFRESH}}$ input is set low clears this output.

RFCK — Refresh clock. The period of the clock is determined by setting conditions on input pins A through H. This output is low for 20 clocks, and high for the remainder of the period.

Functional Description

The DP84300 block diagram is shown in *Figure 1*. This circuit is basically an 8-bit programmable counter. The user selects the number of input clock cycles required per refresh period and sets the binary equivalent on inputs A through H. A signal of that period is produced at the refresh clock (RFCK) output. This output stays low for 20 clock cycles, and goes high for the balance of the period.

When used with the DP8409 dynamic RAM controller, this duty cycle allows the DP8409 the maximum probability to perform a hidden refresh, while still allowing ample time for the DP8409 to perform a forced refresh when needed.

An additional output is provided to ease the design of systems that don't use the DP8409. This output is called refresh request ($\overline{\text{RFRQ}}$). Refresh request becomes true at the rising edge of refresh clock, and becomes false on the first rising edge of the input clock after a refresh.

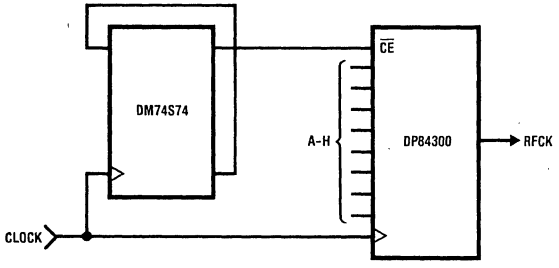
In systems where a divisor of more than 256 is needed, an expansion input ($\overline{\text{CE}}$) has been provided. When this input is high, all counter-related timing is suspended. This excludes actions due to the $\overline{\text{REFRESH}}$ input. The circuits in *Figures 2a and 2b* show how to expand the range of the timer by 2x or by up to 4096 clock cycles. *Figures 3a and 3b* show two typical applications using the DP84300.

By using the clock enable input, it is also possible to change the duty cycle of the refresh clock. The circuits in *Figures 4a and 4b* show how this may be done.

To reset the counter to a known state, select an input divisor of one. On the next clock edge the counter will reset to one. On the next clock edge whatever input divisor that is present on input A-H will be loaded into the counters.

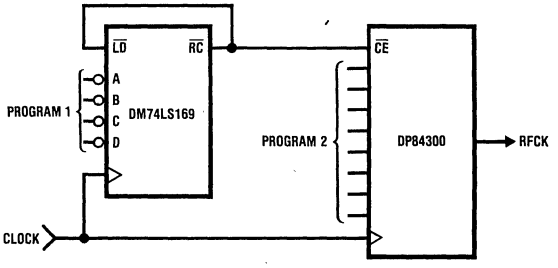
TABLE I. DIVIDER CONSTANTS FOR GENERATION OF A 15.5 μs CLOCK

CPU Clock Frequency	Divisor Input	Actual Period of Output	% Chance of Hidden Refresh
2 MHz	31	15.5 μs	35%
3 MHz	46	15.3 μs	56%
4 MHz	62	15.5 μs	67%
5 MHz	77	15.6 μs	74%
6 MHz	93	15.5 μs	78%
7 MHz	109	15.6 μs	81%
8 MHz	124	15.5 μs	83%
9 MHz	140	15.6 μs	85%
10 MHz	155	15.5 μs	87%



Period of RFCK = 2x program input

FIGURE 2a. Expansion of Clock Divisor by 2x



Period of RFCK 2 = program A x program B
$\overline{\text{RFCK}}$ is low for 20x program 1 clocks
Maximum period of RFCK is 4096 clocks

FIGURE 2b. Typical Expansion for the DP84300

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Functional Description (Continued)

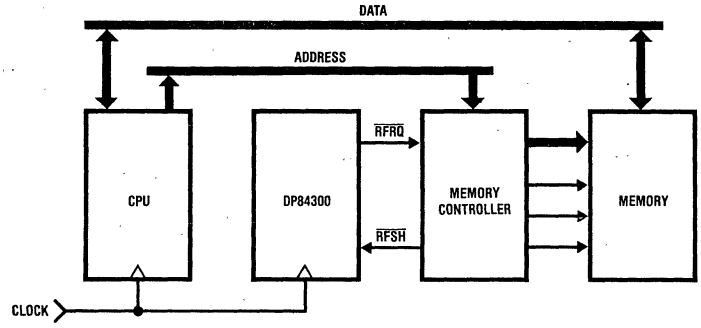


FIGURE 3a. Dynamic Memory System Using DP84300

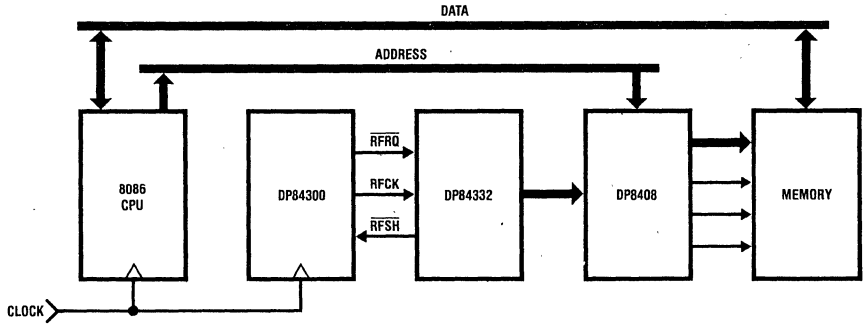


FIGURE 3b. 8086 System Using Dynamic RAMs DP8408, DP84300, and DP84332

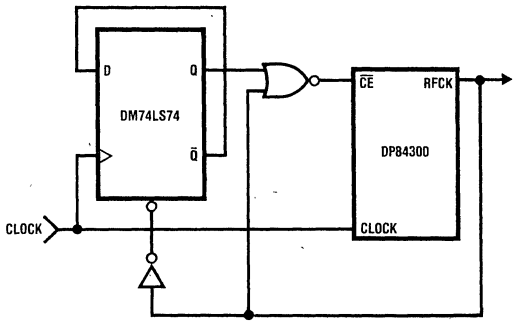


FIGURE 4a. Circuit for Extending RFCK Low to 40 Clocks

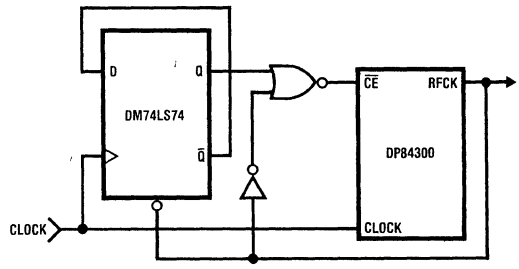
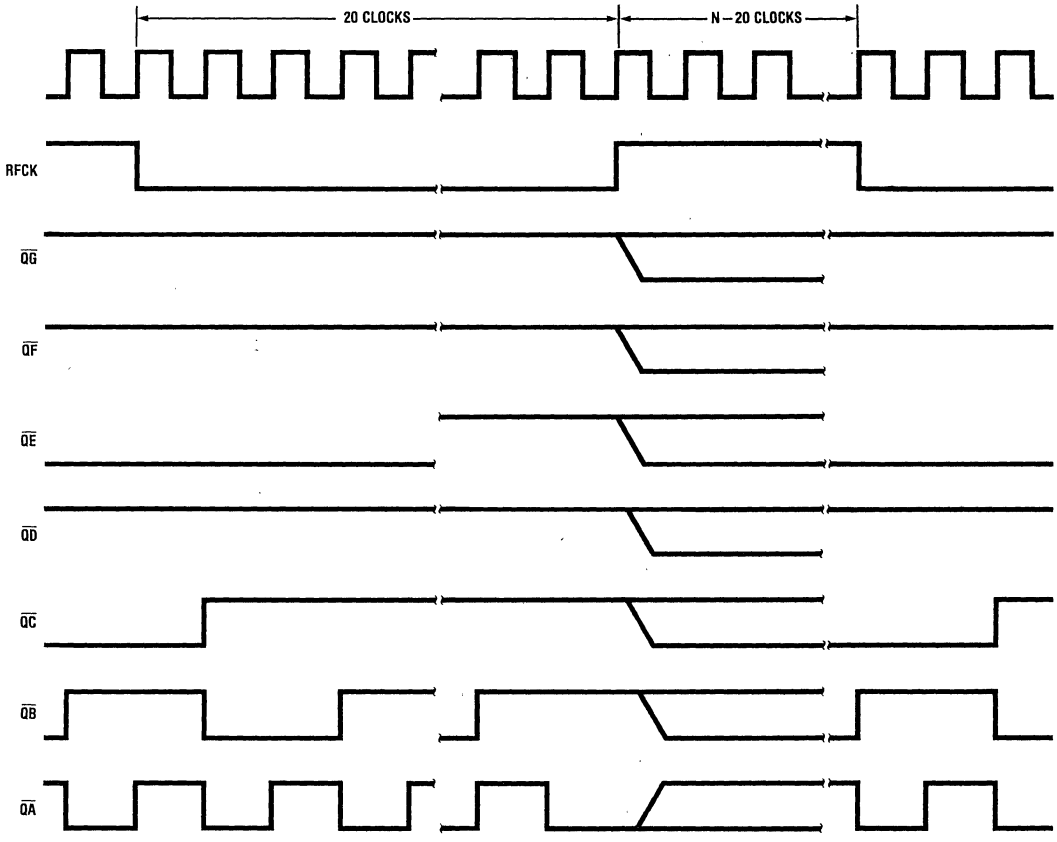


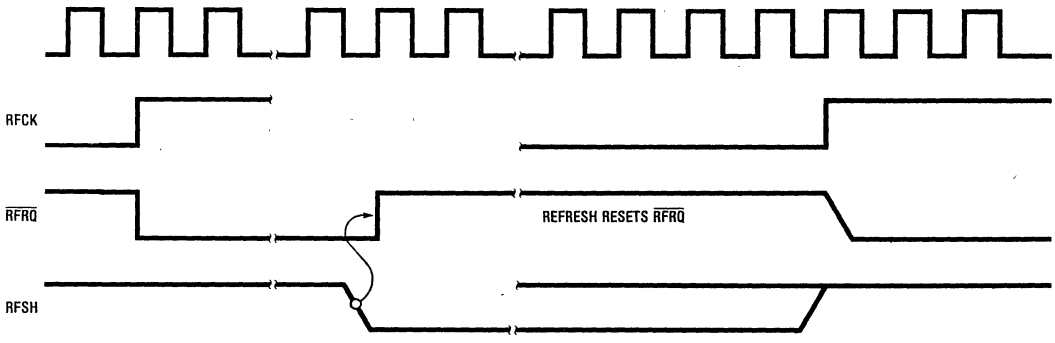
FIGURE 4b. Circuit for Extending RFCK High by 2x

Timing Diagrams

Refresh Timer Outputs



$\overline{\text{REFRESH REQUEST}}$ ($\overline{\text{RFRQ}}$) Output Timing



National Semiconductor

Dynamic Memory Support

PRELIMINARY

DP84312 Dynamic RAM Controller Interface Circuit for the NS16032 CPU

General Description

The DP84312 dynamic RAM controller interface is a Programmable Array Logic (PAL)* device which allows for easy interface between the DP8409 dynamic RAM Controller and the NS16032 microprocessor.

Using timing signals from the NS16201 timing and control unit and the NS16032, the DP84312 supplies all control signals needed to perform memory read, write, byte write, and refresh.

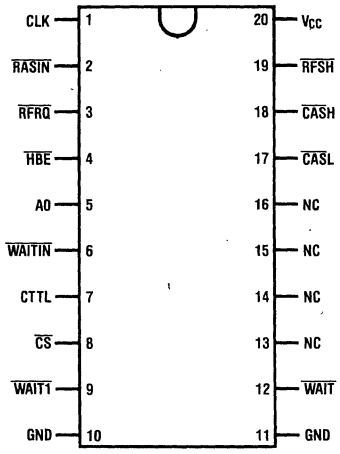
*PAL is a registered trademark of Monolithic Memories, Inc.

Features

- Low parts count memory system
- Allows the DP8409 to perform hidden refresh
- Allows for the insertion of wait states for slow dynamic RAMs
- Supplies independent $\overline{\text{CAS}}$s for byte writing
- Possibility of operation at 8MHz with no wait states
- 20-pin 0.3 inch wide package
- Standard National Semiconductor PAL part (DMPAL16R6)
- PAL logic equations can be modified by the user for his specific application and programmed into any of the PALs in the National Semiconductor PAL family, including the new high speed PALs.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DP84312N-3
See NS Package N20A

Recommended Operating Conditions (Commercial)

	Min	Typ	Max	Units
V_{CC}, Supply Voltage	4.75	5.00	5.25	V
I_{OH}, High Level Output Current			−3.2	mA
I_{OL}, Low Level Output Current			24 (Note 2)	mA
T_A, Operating Free Air Temperature	0		75	°C

Electrical Characteristics over recommended operating temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5	V
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 2.4V, V_{IL} = 0.8V			100	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 0.4V, V_{IL} = 0.8V			−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−250	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max		150	225 (Note 1)	mA

DP84312-3 Switching Characteristics over recommended ranges of temperature and V_{CC}

Symbol	Parameter		Conditions R_L = 667Ω	Commercial T_A = 0°C to +75°C V_{CC} = 5.0V ± 5%			Units
				Min	Typ	Max	
t_{WD}	$\overline{\text{WAITIN}}$ to $\overline{\text{WAIT}}$ Delay		C_L = 45 pF		25	40	ns
t_{PD}	Clock to Output		C_L = 45 pF		15	25	ns
t_{PZX}	Pin 11 to Output Enable		C_L = 45 pF		15	25	ns
t_{PXZ}	Pin 11 to Output Disable		C_L = 5 pF		15	25	ns
t_w	Width of Clock	High		25			ns
		Low		25			ns
t_{su}	Set-Up Time			40			ns
t_h	Hold Time			0	−15		ns

Note 1: I_{CC} = max at minimum temperature.
Note 2: One output at a time; otherwise 16 mA.

System Block Diagram

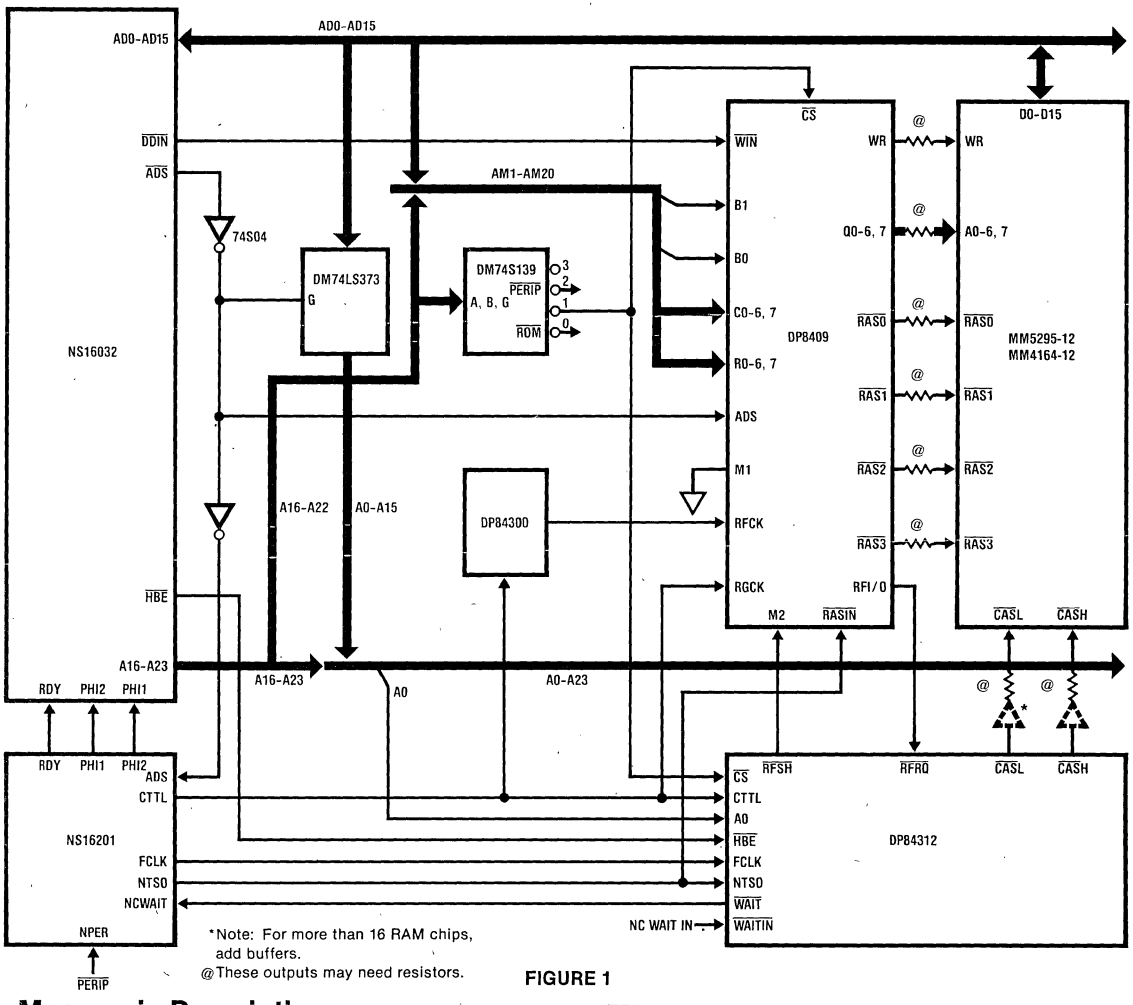


FIGURE 1

Mnemonic Description

INPUT SIGNALS

CLK — Clock input. This clock comes from the FCLK output of the NS16201 timing and control unit, and supplies timing for the internal logic.

$\overline{RASIN}$ — $\overline{RAS}$ input. This input is connected to the NTSO pin of the NS16201. This signal marks the start of a memory cycle.

$\overline{RFRQ}$ — Refresh request. The DP8409 requests a forced refresh with this input.

$\overline{HBE}$, A0 — Address select inputs. These inputs select the type of write during a write cycle, and select their respective $\overline{CAS}$ outputs. These inputs must remain stable throughout the memory cycle.

$\overline{WAITIN}$ — This wait input allows other devices to use the NCWAIT line of the NS16201 clock chip.

CTTL — System clock input. This clock is used to synchronize the memory system to the microprocessor clock.

$\overline{CS}$ — Chip select. This input is used to determine if a memory cycle or a hidden refresh cycle is to be performed.

$\overline{WAIT1}$ — Insert one wait state. This input allows the use of slow memories with a microprocessor using a fast clock by inserting a wait state in selected memory cycles.

V_{CC}, GND — 5.0V ± 5%.

OUTPUT SIGNALS

$\overline{RFSH}$ — Refresh. This output switches the DP8409 to a refresh mode.

$\overline{CASH}$, $\overline{CASL}$ — $\overline{CAS}$ outputs. $\overline{CASH}$ is for controlling the high bank of dynamic RAMs, while $\overline{CASL}$ controls the $\overline{CAS}$ line of the lower bank of RAMs. If only eight RAMs are used in each bank, the $\overline{CAS}$ outputs will directly drive the memories. For larger arrays, these outputs should be buffered with a high current driver, such as the DP84244 MOS driver.

$\overline{WAIT}$ — This output controls the insertion of wait states. This output is ORed with $\overline{WAITIN}$ to allow other devices to insert wait states.

Functional Description

The DP84312 detects the start of a memory cycle when NTSO from the NS16032 timing and control unit (TCU) goes low. The NTSO signal is also used to supply $\overline{RASIN}$ to the DP8409 dynamic RAM controller. After the DP8409 has latched the row address and supplied the column address to the DRAMs, the DP84312 latches the column address. The DP84312 supplies two $\overline{CAS}$ outputs, one for the high byte of memory, and the other for the low byte. The ability to control the upper and lower bytes of memory separately is important during a memory write cycle where one byte of memory is to be written (byte write).

By connecting $\overline{WAIT1}$ of the DP84312 to ground, all selected memory cycles will have one wait state inserted. This allows an NS16032 operating at high CPU clock frequencies to use slower dynamic RAMs.

Memory refresh may be achieved in one of two ways: hidden or forced. Hidden refresh is accomplished whenever a refresh is requested (internal to the DP8409) and an unselected memory cycle occurs. With a hidden refresh, the DP84312 does nothing while the DP8409 performs the refresh. If no refresh has occurred before the trailing edge of refresh clock, the DP8409 will request a forced refresh. The DP84312 detects this request, and allows the current memory cycle to finish. It then outputs wait states to the CPU, which will hold the CPU if it requests a memory cycle. During this time the DP84312 has switched the dynamic RAM controller to the auto refresh mode, allowing it to perform a refresh. At the end of the refresh cycle, the DP8409 is switched back to the auto access mode, and the wait is removed after a sufficient $\overline{RAS}$ precharge time. The total forced refresh takes four CPU clock cycles; of which some, none or all may be actual wait states. If the CPU does not request a memory cycle during this refresh cycle, the refresh will not impact the CPU's performance.

The DP84312 can possibly be operated at 8 MHz with no wait states (WAIT1 = "1") given the following conditions:

$T2 + T3 = 250$ ns
NTSO generation = 15 ns max.
$\overline{RASIN}$ to $\overline{CAS}$ delay DP8409-2 = 130 ns max.
External $\overline{CASH,L}$ generation using 74S02 and 74S240
7.5 ns (74S02) + 10 ns (74S240) – 7.5 ns (less load on 8409 $\overline{CAS}$ line) = 10 ns max.
Transceiver delay = 12 ns max.
NS16032 data setup = 20 ns max.
$\therefore$ Minimum $t_{CAC} = 63$ ns
$= 250 - 15 - 130 - 10 - 12 - 20$
Minimum $t_{RAS} = 250$ ns
Minimum $t_{RP} = 250$ ns
Minimum $t_{RAH} = 20$ ns

The DP84312 is a standard National Semiconductor PAL part (DMPAL16R6). The user can modify the PAL equations to support his particular application. The DP84312 logic equations, function table (functional test), and logic diagram can be seen at the end of this Data Sheet.

Timing Diagrams

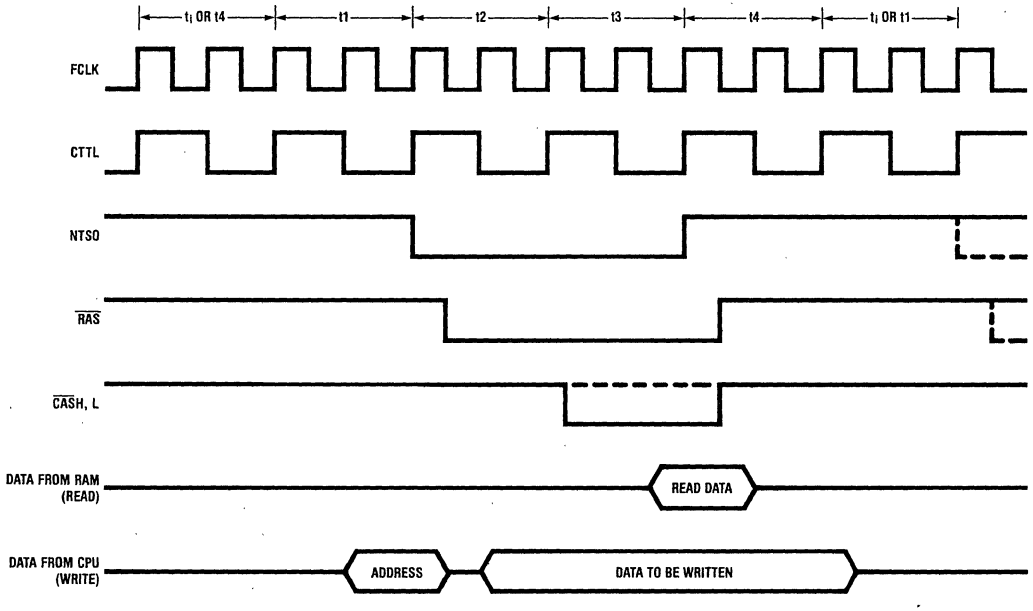


FIGURE 2a. Read, Write, or Hidden Refresh Memory Cycle for the NS16032-DP8409 Interface

Timing Diagrams (Continued)

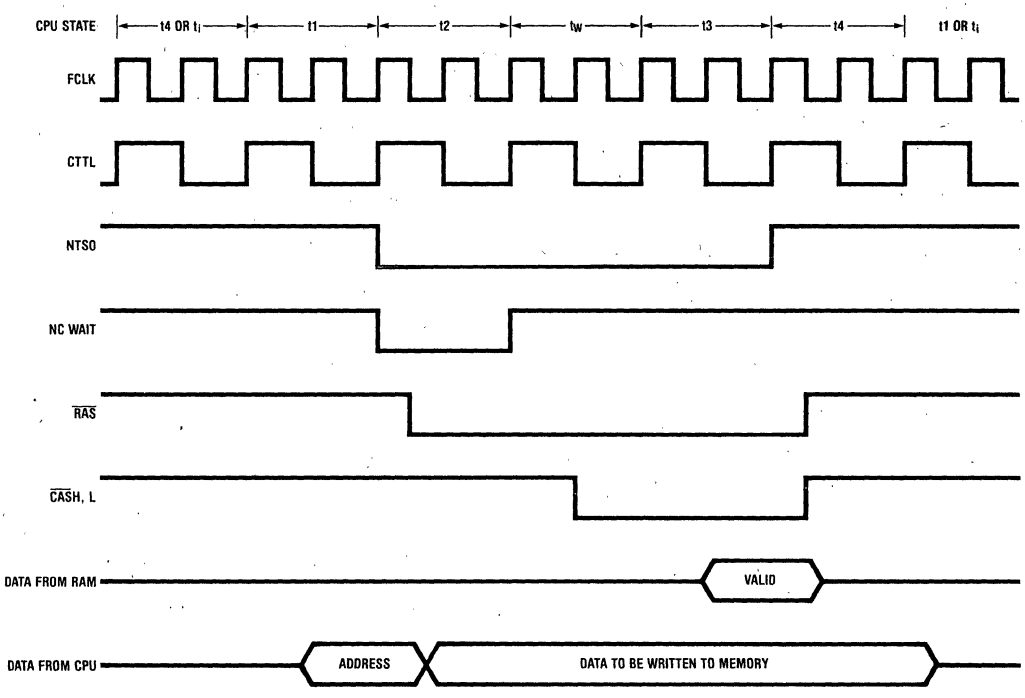


FIGURE 2b. Read or Write Memory Cycle with One Wait

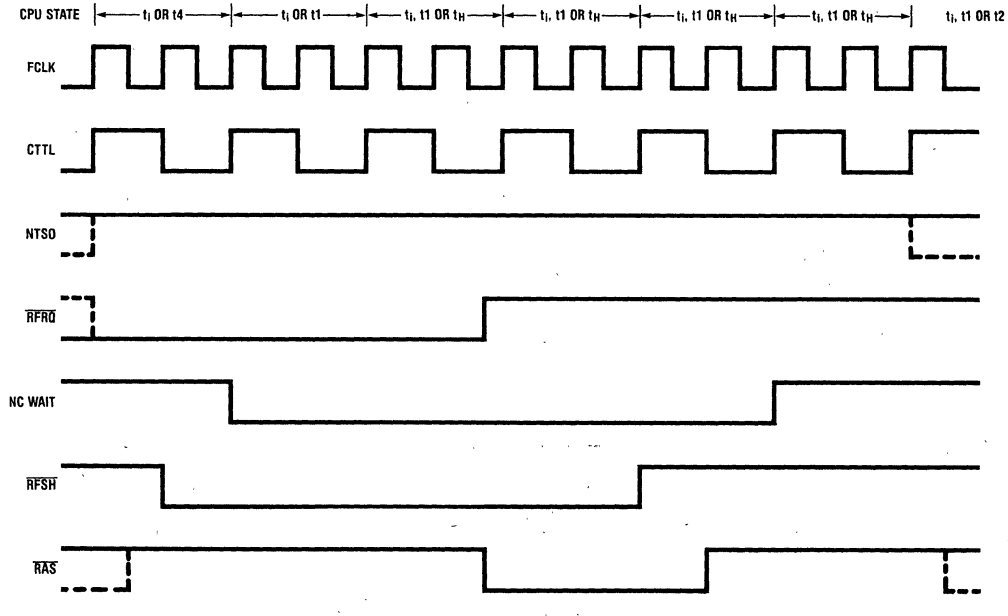


FIGURE 2c. Forced Refresh Cycle

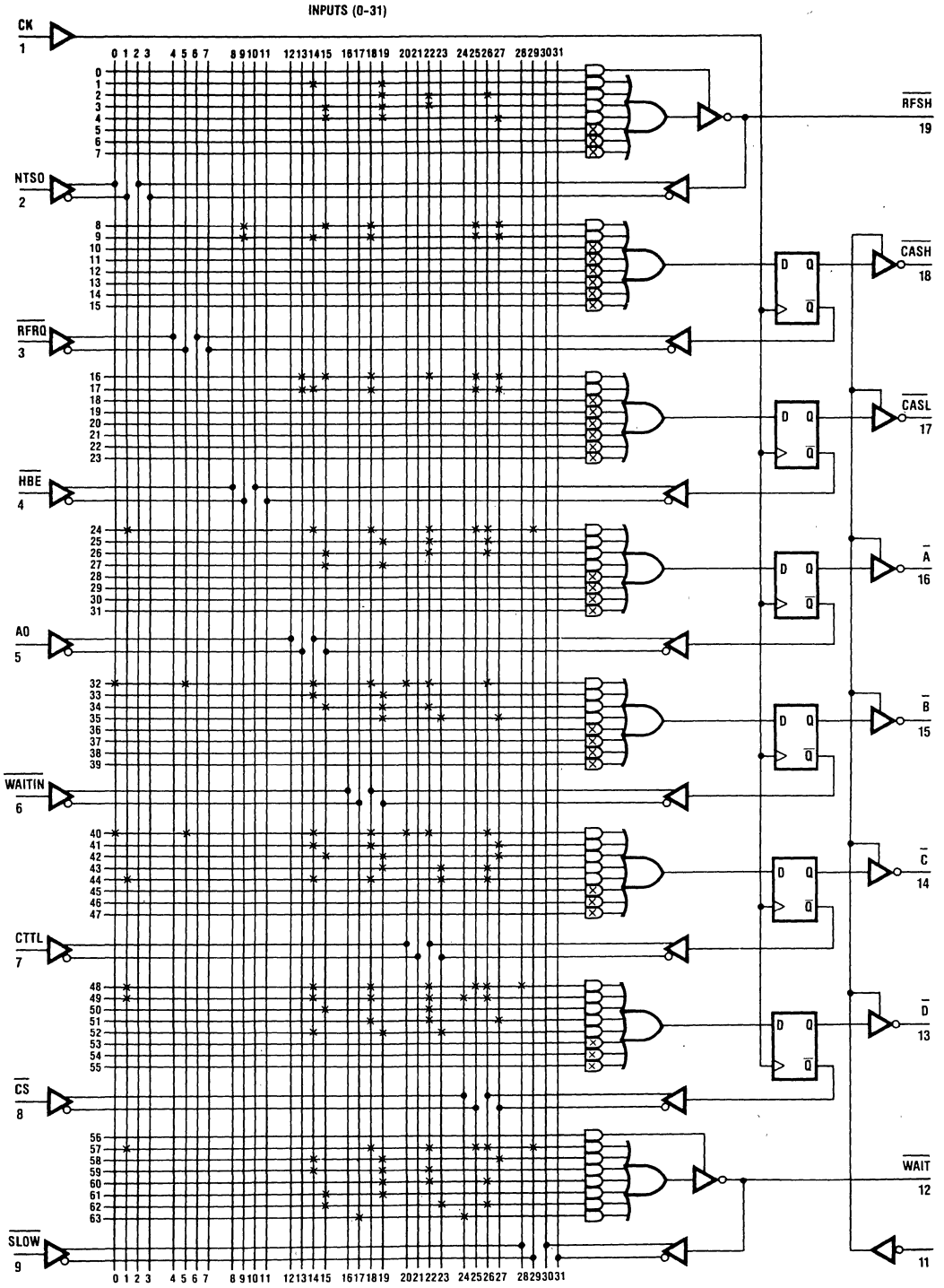
PAL16R6
DP84312
Interface Circuit for the NS16032/DP8409
Memory System
CK NTSO /RFRQ /HBE A0 /WAITIN CTTL /CS /SLOW
GND /OE /WAIT /D /C /B /A /CASL /CASH /RFSH VCC

```
CASH: = A • /B • /C • D •HBE • CS +
        /A • /B • D • HBE • CS

CASL: = A • /B • /C • D • /A0 • CS +
        /A • /B • D /A0 • CS

A     := /A • /B • /C • /D • /NTSO • CS • SLOW +
         B • /C • /D +
         A • /C • /D +
         A • B

B     := /A • /B • /C • /D • NTSO • RFRQ • CTTL +
         /A • B +
         A • B • /C +
         B • C • D

C     := /A • /B • /C • /D • NTSO • RFRQ • CTTL +
         /A • /B • D +
         A • B • D +
         B • C • /D +
         /A • /B • C • /D • /NTSO

D     := /A • /B • /C • /D • /NTSO • CS • /SLOW +
         /A • /B • /C • /D • /NTSO • /CS +
         A • /C +
         /B • /C • D +
         /A • B • C

IF (VCC) WAIT = /B • /C • /D • /NTSO • CS • SLOW +
         /A • B • D +
         B • /C • /D +
         A • B +
         A • C • /D +
         /CS • WAITIN

IF (VCC) RFSH = /A • B +
         B • /C • /D +
         A • B • /C +
         A • B • C
```

Function Table

CK	NTSO	$\overline{RFRQ}$	$\overline{HBE}$	A0	$\overline{WAITIN}$	CTTL	$\overline{CS}$	$\overline{SLOW}$	$\overline{OE}$	CASH	CASL	A	B	C	D	WAIT	RFSH
C	H	H	L	L	H	H	H	H	L	X	X	X	X	X	X	X	X
C	H	H	L	L	H	H	H	H	L	L	L	L	L	L	L	L	L
C	L	X	L	L	H	X	L	H	L	L	L	L	L	L	H	L	L
C	L	X	L	L	H	X	L	H	L	H	H	L	L	H	H	L	L
C	X	X	L	L	H	X	L	H	L	H	H	L	L	H	L	L	L
C	H	X	L	L	H	X	L	H	L	L	L	L	L	L	L	L	L
C	L	X	L	H	H	X	L	L	L	L	L	H	L	L	L	H	L
C	X	X	L	H	H	X	L	L	L	L	L	H	L	L	H	L	L
C	X	X	L	H	H	X	L	L	L	H	L	L	L	L	H	L	L
C	X	X	L	H	H	X	L	L	L	H	L	L	L	H	H	L	L
C	X	X	L	H	H	X	L	L	L	H	L	L	L	H	L	L	L
C	H	X	L	L	H	X	H	H	L	L	L	L	L	L	L	L	L
C	L	X	L	L	H	X	H	X	L	L	L	L	L	L	H	L	L
C	X	X	L	L	L	X	H	X	L	L	L	L	L	H	H	H	L
C	H	X	L	L	H	X	H	X	L	L	L	L	L	H	L	L	L
C	H	X	L	L	H	X	H	X	L	L	L	L	L	L	L	L	L
C	H	L	X	X	H	H	X	X	L	L	L	L	H	H	L	L	H
C	H	X	X	X	H	L	X	X	L	L	L	L	H	H	H	H	H
C	H	H	X	X	H	H	X	X	L	L	L	L	H	L	H	H	H
C	H	H	X	X	H	L	X	X	L	L	L	L	H	L	L	H	H
C	H	H	X	X	H	H	X	X	L	L	L	H	H	L	L	H	H
C	H	H	X	X	H	L	X	X	L	L	L	H	H	L	H	H	H
C	H	H	X	X	H	H	X	X	L	L	L	H	H	H	H	H	H
C	H	H	X	X	H	L	X	X	L	L	L	H	H	H	L	H	L
C	H	H	X	X	H	H	X	X	L	L	L	H	L	H	L	H	L
C	H	H	X	X	H	X	H	H	L	L	L	L	L	L	L	L	L
C	L	H	X	X	L	X	H	X	L	L	L	L	L	L	H	H	L
C	L	H	X	X	L	X	H	X	L	L	L	L	L	H	H	H	L
C	L	H	X	X	L	X	H	X	L	L	L	L	L	H	L	H	L
C	L	X	X	X	H	X	H	X	L	L	L	L	L	H	L	L	L
C	H	X	X	X	H	X	H	X	L	L	L	L	L	L	L	L	L
C	H	H	H	H	H	H	H	H	H	Z	Z	Z	Z	Z	Z	Z	Z

DP84312 Logic Diagram PAL16R6



National Semiconductor

Dynamic Memory Support
PRELIMINARY

DP84322 Dynamic RAM Controller Interface Circuit for the 68000 CPU

General Description

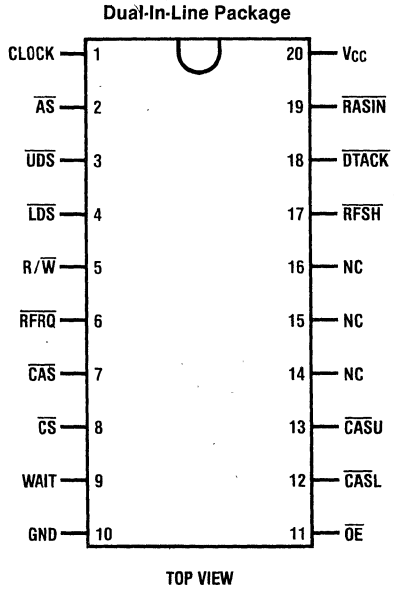
The DP84322 dynamic RAM controller interface is a Programmable Array Logic (PAL)* device which allows for easy interface between the DP8409 dynamic RAM Controller and the 68000 microprocessor.

The DP84322 supplies all the control signals needed to perform memory read, write and refresh. Logic is included for inserting a wait state when using fast CPUs.

Features

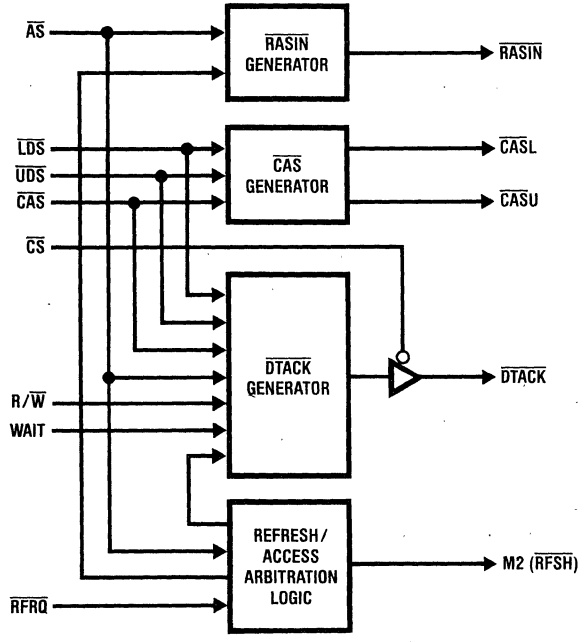
- Provides 3-chip solution for the 68000 CPU and dynamic RAM interface
- Works with all 68000 speed versions
- Possibility of operation at 8 MHz with no wait states
- Performs hidden refresh
- $\overline{DTACK}$ is automatically inserted for both memory access and memory refresh
- Performs forced refresh using typically 4 CPU clocks
- Standard National Semiconductor PAL part (DMPAL16R4)
- PAL logic equations can be modified by the user for his specific application and programmed into any of the PAL in the National Semiconductor PAL family, including the new high speed PAL's.

Connection Diagram



Order Number DP84322N-3
See NS package N20A

Block Diagram



*PAL is a registered trademark of Monolithic Memories, Inc.

Recommended Operating Conditions (Commercial)

	Min	Typ	Max	Units
V_{CC}, Supply Voltage	4.75	5.00	5.25	V
I_{OH}, High Level Output Current			−3.2	mA
I_{OL}, Low Level Output Current			24 (Note 2)	mA
T_A, Operating Free Air Temperature	0		75	°C

Electrical Characteristics over recommended operating temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5	V
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 2.4V, V_{IL} = 0.8V			100	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 0.4V, V_{IL} = 0.8V			−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−250	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max		150	225 (Note 1)	mA

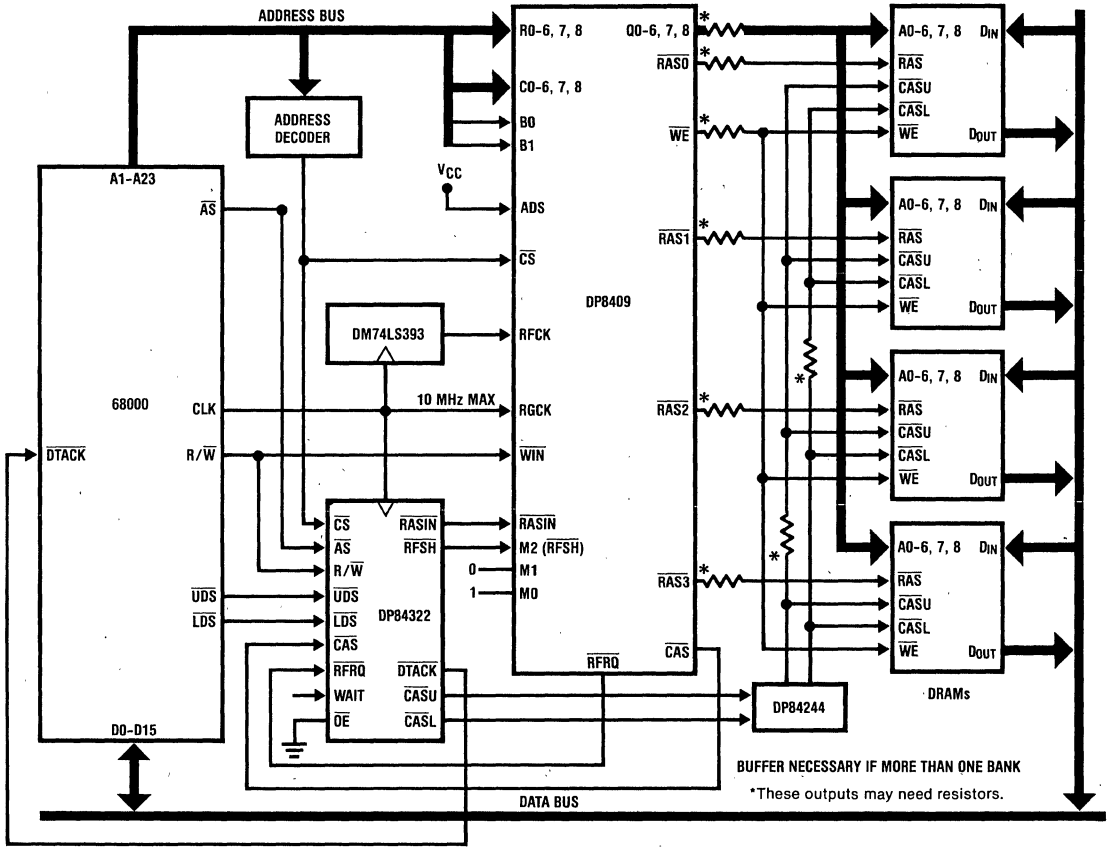
Switching Characteristics over recommended ranges of temperature and V_{CC}

Symbol	Parameter		Test Conditions R_L = 667Ω	Commercial T_A = 0°C to +75°C V_{CC} = 5.0V ± 5%			Units
				Min	Typ	Max	
t_{PD}	Input to Output		C_L = 45 pF		25	40	ns
t_{PD}	Clock to Output				15	25	ns
t_{PZX}	Pin 11 to Output Enable				15	25	ns
t_{PXZ}	Pin 11 to Output Disable		C_L = 5 pF		15	25	ns
t_{PZX}	Input to Output Enable		C_L = 45 pF		25	40	ns
t_{PXZ}	Input to Output Disable		C_L = 5 pF		25	40	ns
t_w	Width of Clock	High		25			ns
		Low		25			ns
t_{su}	Set-Up Time			40			ns
t_h	Hold Time			0	−15		ns

Note 1: I_{CC} = max at minimum temperature.
Note 2: One output at a time; otherwise 16 mA.

System Block Diagram

DP84322 and DP8409 for 68000 CPU



Mnemonic Description

INPUT SIGNALS

CLOCK	The clock signal determines the timing of the outputs and should be connected directly to the 68000 clock input.
$\overline{AS}$	Address Strobe from the 68000 CPU. This input is used to generate $\overline{RASIN}$ to the DP8409.
$\overline{UDS}$, $\overline{LDS}$	Upper and lower data strobe from the 68000 CPU. These inputs, together with $\overline{AS}$, R/$\overline{W}$, provide $\overline{DTACK}$ to the 68000.
R/$\overline{W}$	Read/write from the 68000 CPU, when WAIT = 0. Selects processor speed when WAIT = 1 ("1" = 4 to 6 MHz, "0" = 8 MHz).
$\overline{CAS}$	Column Address Strobe from the DP8409. This input, together with $\overline{LDS}$ and $\overline{UDS}$, provides two separate $\overline{CAS}$ outputs for accessing upper and lower memory data bytes.
$\overline{CS}$	Chip Select. This input enables $\overline{DTACK}$ output. $\overline{CS}$ = 0, $\overline{DTACK}$ output is enabled; $\overline{CS}$ = 1, $\overline{DTACK}$ output is TRI-STATE®.
$\overline{RFRQ}$	Refresh Request. This input requests the DP84322 for a forced refresh.
WAIT	This input allows the necessary wait state to be inserted for memory access cycles.

OUTPUT SIGNALS

$\overline{RASIN}$	This output provides a memory cycle start signal to the DP8409 and provides $\overline{RAS}$ timing during hidden refresh.
$\overline{CASU}$, $\overline{CASL}$	These signals are the separate $\overline{CAS}$ outputs needed for byte writing.
$\overline{DTACK}$	This output is used to insert wait states into the 68000 memory cycles when selected and during a forced refresh cycle where the CPU attempts to access the memory. This output is enabled when $\overline{CS}$ input is low and TRI-STATED when $\overline{CS}$ is high.
$\overline{RFSH}$	This output controls the mode of the DP8409. It always goes low for 4 CPU clock periods when $\overline{AS}$ is inactive and a forced refresh is requested through $\overline{RFRQ}$ input. This allows the DP8409 to perform an automatic forced refresh.

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Functional Description

MEMORY ACCESS

As a 68000 bus cycle begins, a valid address is output on the address bus A1-A23. This address is decoded to provide Chip Select ($\overline{CS}$) to the DP8409. After the address becomes valid, $\overline{AS}$ goes low and it is used to set $\overline{RASIN}$ low from the DP84322 interface circuit. Note that $\overline{CS}$ must go low for a minimum of 10 ns before the assertion of $\overline{RASIN}$ for a proper memory access. As an example, with a 8 MHz 68000, the address is valid for at least 30 ns before $\overline{AS}$ goes active. $\overline{AS}$ then has to ripple through the DP84322 to produce $\overline{RASIN}$. This means the address is valid for a minimum of 40 ns before $\overline{RASIN}$ goes low, and the decoding of $\overline{CS}$ should take less than 30 ns. At this speed the DM74LS138 or DM74LS139 decoders can be selected to guarantee the 10 ns minimum required by $\overline{CS}$ set-up time going low before the access $\overline{RASIN}$ goes low (t_{CSRL} of the DP8409). This is important because a false hidden refresh may take place when the minimum t_{CSRL} is not met. Typically $\overline{RASIN}$ occurs at the end of S2. Subsequently, selected $\overline{RAS}$ output, row to column select and then $\overline{CAS}$ will automatically follow $\overline{RASIN}$ as determined by mode 5 of the DP8409. Mode 5 guarantees a 30 ns minimum for row address hold time (t_{RAH}) and a minimum of 8 ns column address set-up time (t_{ASC}). If the system requires instructions that use byte writing, then $\overline{CASU}$ and $\overline{CASL}$ are needed for accessing upper and lower memory data bytes, and they are provided by the DP84322. In the DP84322, $\overline{LDS}$ and $\overline{UDS}$ are gated with $\overline{CAS}$ from the DP8409 to provide $\overline{CASL}$ and $\overline{CASU}$, therefore designers need not be concerned about delaying $\overline{CAS}$ during write cycles to assure valid data being written into memory. The 8 MHz 68000 specifies during a write cycle that data output is valid for a minimum of 30 ns before $\overline{DS}$ goes active. Thus, $\overline{CASL}$ and $\overline{CASU}$ will not go low for at least 40 ns after the output data becomes stable, guaranteeing the 68000 valid data is written to memory.

Furthermore, the gating of $\overline{UDS}$, $\overline{LDS}$ and $\overline{CAS}$ allows the DP84322 interface controller to support the test and set instruction (TAS). The 68000 utilizes the read-modify-write cycle to execute this instruction. The TAS instruction provides a method of communication between processors in a multiple processor system. Because of the nature of this instruction, in the 68000, this cycle is indivisible and the Address Strobe $\overline{AS}$ is asserted throughout the entire cycle, however $\overline{DS}$ is asserted twice for two accesses: a read then a write. The dynamic RAM controller and the DP84322 respond to this read-modify-write instruction as follows (refer to the TAS instruction timing diagram for clarification). First, the selected $\overline{RAS}$ goes low as a result of $\overline{AS}$ going low, and this $\overline{RAS}$ output will remain low throughout the entire cycle. Then the DP84322's selected $\overline{CAS}$ output ($\overline{CASL}$ or $\overline{CASU}$) goes low to read the specified data byte. After this read, $\overline{DS}$ goes high causing the selected $\overline{CAS}$ to go high. A few clocks later R/$\overline{W}$ goes low and then $\overline{DS}$ is reasserted. As $\overline{DS}$ goes low, the selected $\overline{CAS}$ goes low strobing the CPU's modified data into memory, after which the cycle is ended when $\overline{AS}$ goes high.

The two $\overline{CAS}$ outputs from the DP84322, however, can only drive one memory bank. For additional driving capability, a memory driver such as the DP84244 should be added to drive loads of up to 500 pF.

Since this DP84322 interface circuit is designed to operate with all of the 68000 speed versions, a status input called WAIT is used to distinguish the 8 MHz from the others. The WAIT input should be set low for 6 MHz or less allowing full speed of operation with no wait states. Data Transfer Acknowledge input ($\overline{DTACK}$) of the 68000 at these speeds is automatically inserted during S2 for every memory transaction cycle and is then negated at the end of that cycle when $\overline{UDS}$ and/or $\overline{LDS}$ go high. For the 8 MHz 68000 however, a wait state is required for every memory transaction cycle. At these speeds, the WAIT input is set high, selecting the DP8409's $\overline{CAS}$ output to generate $\overline{DTACK}$ and again $\overline{DTACK}$ is negated at the end of the cycle when $\overline{UDS}$ or $\overline{LDS}$ goes high. Note that $\overline{DTACK}$ output is enabled only when the DP8409's $\overline{CS}$ is low. Therefore when the 68000 is accessing I/O or ROM (in other words, when the DP8409 is not selected), the DP84322's $\overline{DTACK}$ output goes high impedance logic '1' through the external pull-up resistor and it is now up to the designer to supply $\overline{DTACK}$ for a proper bus cycle.

The following table indicates the maximum memory speed in terms of the DRAM timing parameters: t_{CAC} (access-time from $\overline{CAS}$) and t_{RP} ($\overline{RAS}$ precharge time) required by different 68000 speed versions:

Microprocessor Clock	Maximum t_{CAC}	Minimum t_{RP}	Minimum t_{RAS}
8 MHz	125 ns	140 ns	220 ns
6 MHz	90 ns	170 ns	290 ns
4 MHz	270 ns	280 ns	450 ns

Pin 5 (R/$\overline{W}$ input to the DP84322) is not used as R/$\overline{W}$ when the WAIT input is high. Therefore, when WAIT is high and pin 5 is low, this is configured for the 8 MHz 68000. The dynamic RAM controller in this configuration operates in mode 5 and mode 1.

When both WAIT and pin 5 are high, this is configured for 4 MHz and 6 MHz 68000, allowing only two microprocessor clocks for memory refresh. Furthermore, the designer can use the DP8408 because the dynamic RAM controller now operates in mode 0 and mode 5 or mode 6. In addition, the programmable refresh timer, DP84300, should be used to determine the refresh rate (RFCK) and to provide the refresh request ($\overline{RFRQ}$) input to the DP84322. The refresh timer can provide over two hundred different divisors. $\overline{RFRQ}$ is given at the beginning of every RFCK cycle and remains active until M2 goes low for memory refresh. The DP84322 samples $\overline{RFRQ}$ when $\overline{AS}$ is high, then sets M2 low for two microprocessor clocks, taking the DP8408 or DP8409 to the external control refresh mode. $\overline{RASIN}$ for this refresh is also issued by the DP84322. If a memory access is pending, $\overline{RASIN}$ for this access will not be given until it is delayed for approximately one microprocessor clock, allowing $\overline{RAS}$ precharge time for the dynamic RAMs.

The following table indicates different memory speeds in terms of the DRAM parameters required by 4 MHz and 6 MHz 68000:

Microprocessor Clock	Maximum t_{CAC}	Minimum t_{RAS}	Minimum t_{RP}	Minimum t_{RAH}
4 MHz	290 ns	200 ns	225 ns	20 ns
6 MHz	110 ns	125 ns	140 ns	20 ns

DP8408, DP8409 operate in mode 6 and mode 0.

Functional Description (Continued)

When WAIT = 1, pin 5 = 0 (8 MHz), the PAL controller supports read and write cycles with one inserted wait state, forced refresh with five wait states inserted if $\overline{CS}$ is valid, and hidden refresh. This PAL mode does not support the TAS instruction.

When WAIT = pin 5 = 1 (4-6 MHz), the PAL controller supports read and write cycles with no wait states inserted, and forced refresh with two wait states inserted if $\overline{CS}$ is valid. This PAL mode does not support the TAS instruction and only supports hidden refresh when used in mode 5 with the DP8409 controller.

The DP84322 can possibly be operated at 8 MHz with no wait states (WAIT = "0") given the following conditions:

FAST PAL (PAL16R4A)
S2 + S3 + S4 + S5 = 250 ns
$\overline{RASIN}$ delay = 60 ns ($\overline{AS}$ low max.)
+ 25 ns (Fast PAL delay) = 85 ns max.
$\overline{RASIN}$ to $\overline{CAS}$ delay DP8409-2 = 130 ns max.
External $\overline{CASH,L}$ generation using 74S02 and 74S240
7.5 ns (74S02) + 10 ns (74S240) − 7.5 ns (less load on 8409 $\overline{CAS}$ line) = 10 ns max.
Transceiver delay (74LS245) = 12 ns max.
68000 data setup into S6 = 40 ns min.
∴ Minimum t_{CAC} = 53 ns
= 250 − 85 − 130 − 10 − 12 + 40
Minimum t_{RAS} = 240 ns
Minimum t_{RP} = 150 ns
Minimum t_{RAH} = 20 ns

REFRESH CYCLE

Since the access sequence timing is automatically derived from $\overline{RASIN}$ in mode 5, R/$\overline{C}$ and $\overline{CASIN}$ are not used and now become Refresh Clock (RFCK) and $\overline{RAS}$-generator clock (RGCK) respectively. The Refresh Clock RFCK may be divided down from RGCK, which is the microprocessor clock, using the DM74LS393 or DM74LS390. RFCK provides the refresh time interval and RGCK the fast clock for all $\overline{RAS}$ refresh if forced refreshing is necessary. The DP8409 offers both hidden refresh in mode 5 and forced refresh in mode 1 with priority placed on hidden refreshing. Assume 128 rows are to be refreshed, then a 16 μs maximum clock period is needed for RFCK to distribute refreshing of all the rows over the 2 ms period.

The DP8409 provides hidden refreshing in mode 5 when the refresh clock (RFCK) is high and the microprocessor is not accessing RAM. In other words, when the DP8409's chip select is inactive because the microprocessor is accessing elsewhere, all four $\overline{RAS}$ outputs follow $\overline{RASIN}$, strobing the contents of the on-chip refresh counter to every memory bank. $\overline{RASIN}$ going high terminates the hidden refresh and also increments the refresh counter, preparing it for the next refresh cycle. Once a hidden refresh has taken place, a forced refresh will not be requested by the DP8409 for the current RFCK cycle.

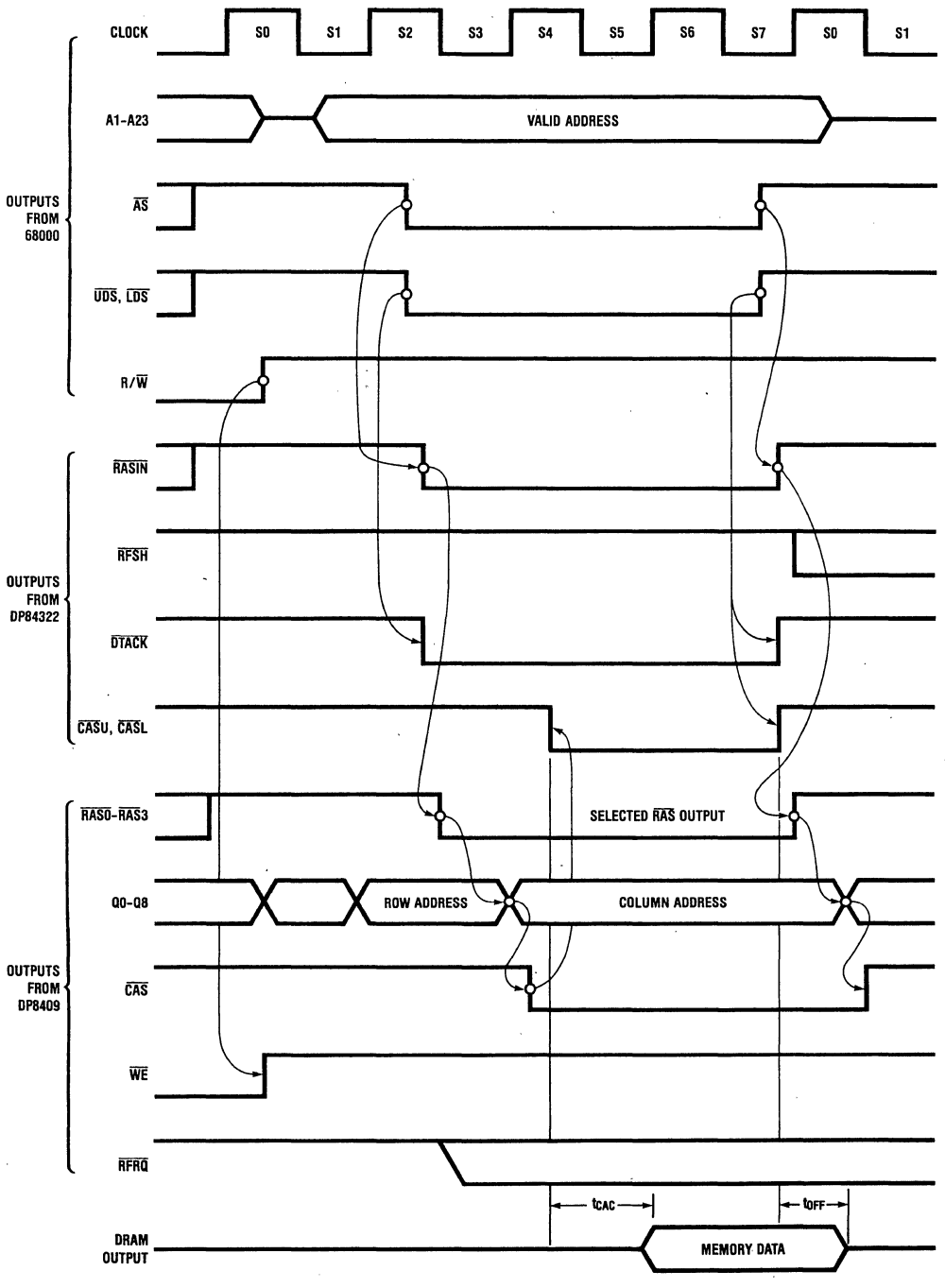
However, if the microprocessor continuously accessed the DP8409 and memory while RFCK was high, a hidden refresh could not have taken place and now the system must force a refresh. Immediately after RFCK goes low, the Refresh Request signal ($\overline{RFRQ}$) from the DP8409 goes low, indicating a forced refresh is necessary. First, when $\overline{RFRQ}$ goes low any time during S2 to S7, the controller interface circuit waits until the end of the current memory access cycle and then sets M2 ($\overline{RFSH}$) low. This refresh takes four microprocessor clocks to complete. If the current cycle is another memory cycle, the 68000 will automatically be put in four wait states. Alternately, when $\overline{RFRQ}$ goes low while $\overline{AS}$ is high during S0 to S1, M2 is now set low at S2. Therefore, it requires an additional microprocessor clock for this refresh. Once the DP8409 is in mode 1 forced refresh, all the $\overline{RAS}$ outputs remain high until two RGCK trailing edges after M2 goes low, when all $\overline{RAS}$ outputs go low. This allows a minimum of one and a half clock periods of RGCK for $\overline{RAS}$ precharge time. As specified in the DP8409 data sheet, the $\overline{RAS}$ outputs remain low for two clock periods of RGCK. The refresh counter is incremented as the $\overline{RAS}$ outputs go high. Once the forced refresh has ended, M2 is brought high, the DP8409 back to mode 5 auto access. Note that $\overline{RASIN}$ for the pending access is not given until it has been delayed for a full microprocessor clock, allowing $\overline{RAS}$ precharge time for the coming access.

If the 68000 bus is inactive (i.e., the 68000's instruction queue is full, or the 68000 is executing internal operations such as a multiply instruction, or the 68000 is in halt state...) and a refresh has been requested, a refresh will also take place because $\overline{RFRQ}$ is continuously sampled while $\overline{AS}$ is high. Therefore, refreshing under these conditions will be transparent to the microprocessor. Consequently, the system throughput is increased because the DP84322 allows refreshing while the 68000 bus is inactive.

The 84322 is a standard National Semiconductor PAL part (DMPAL16R4). The user can modify the PAL equations to support his particular application. The 84322 logic equations function table (functional test), and logic diagram can be seen at the end of this data sheet.

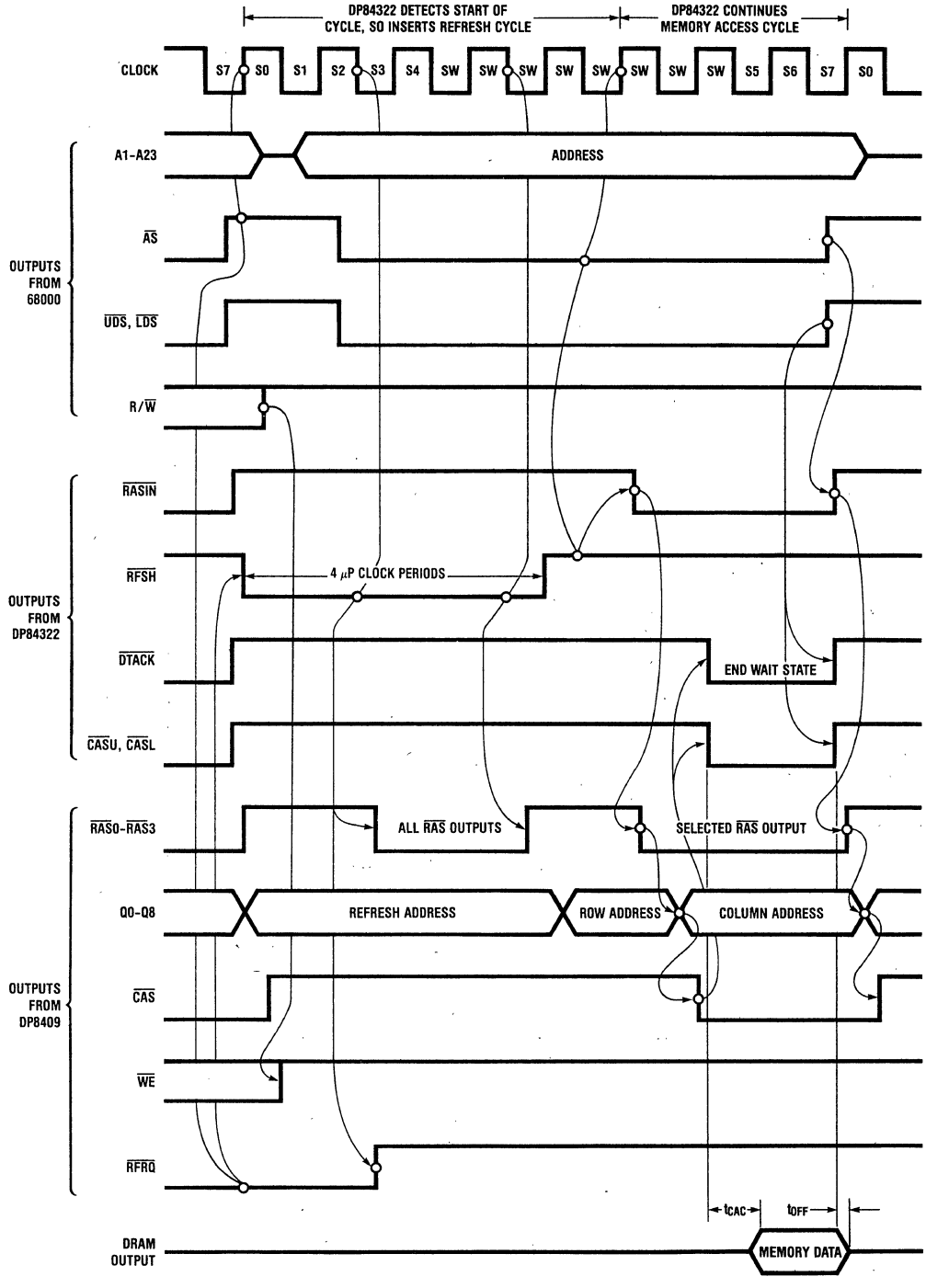
Timing Diagrams

68000 Memory Read Cycle (Wait = 0, Pin 5 = R/$\overline{W}$)



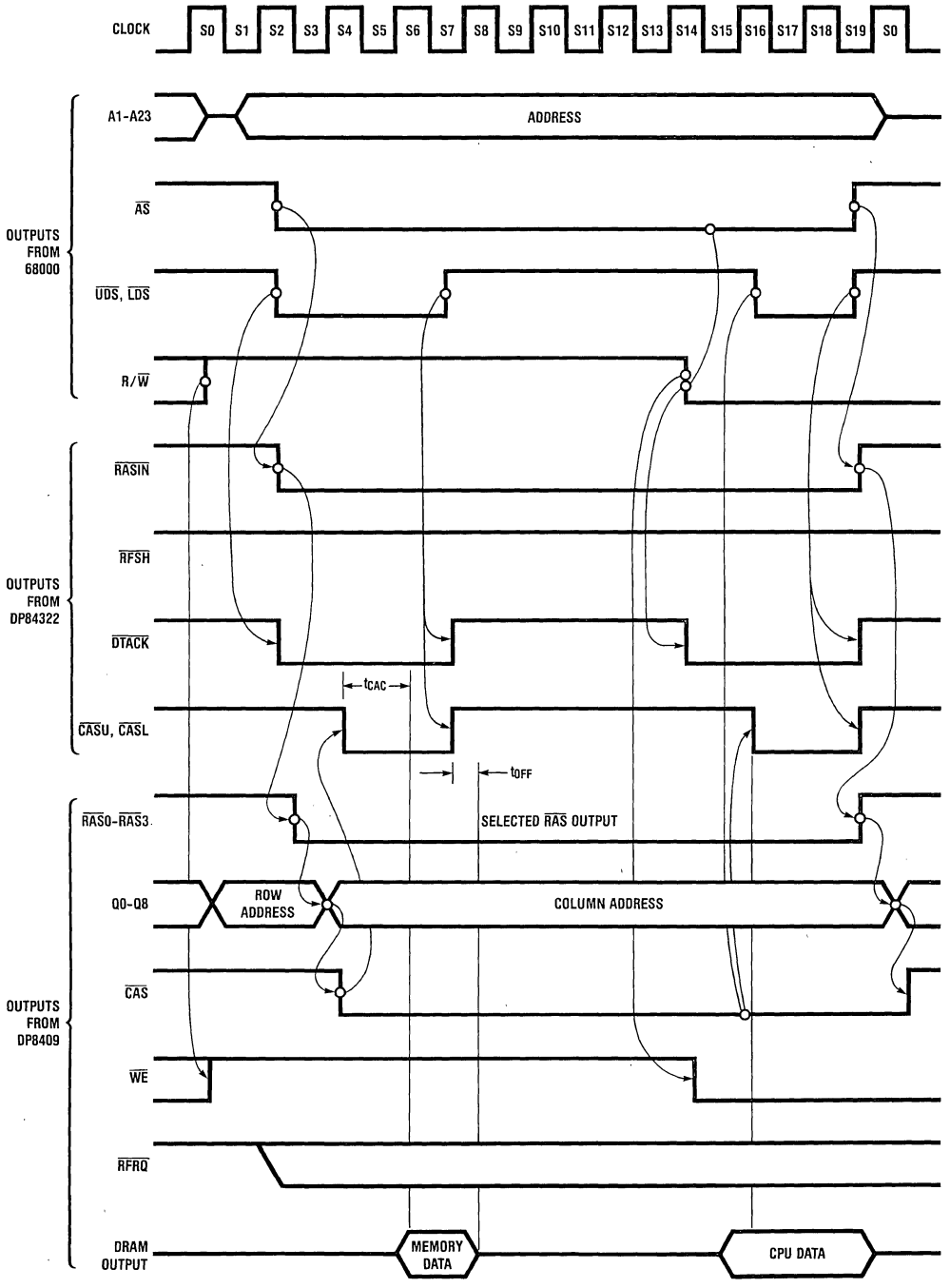
Timing Diagrams (Continued)

68000 Memory Read Cycle and Forced Refresh (Wait = 0, Pin 5 = R/$\overline{W}$)
(4 wait clock periods inserted for forced refresh)



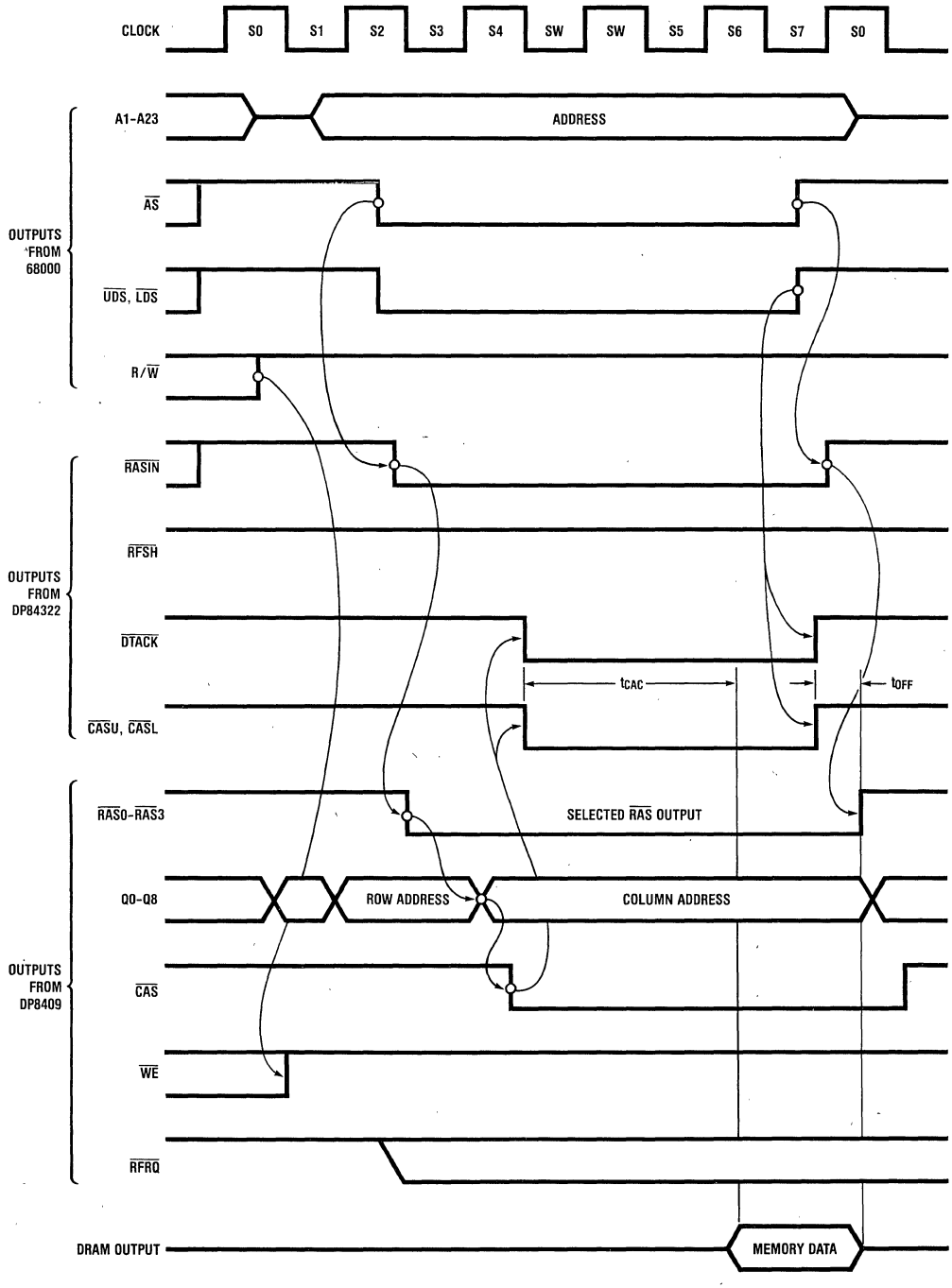
Timing Diagrams (Continued)

TAS Instruction Cycle (Wait = 0, Pin 5 = R/$\overline{W}$)



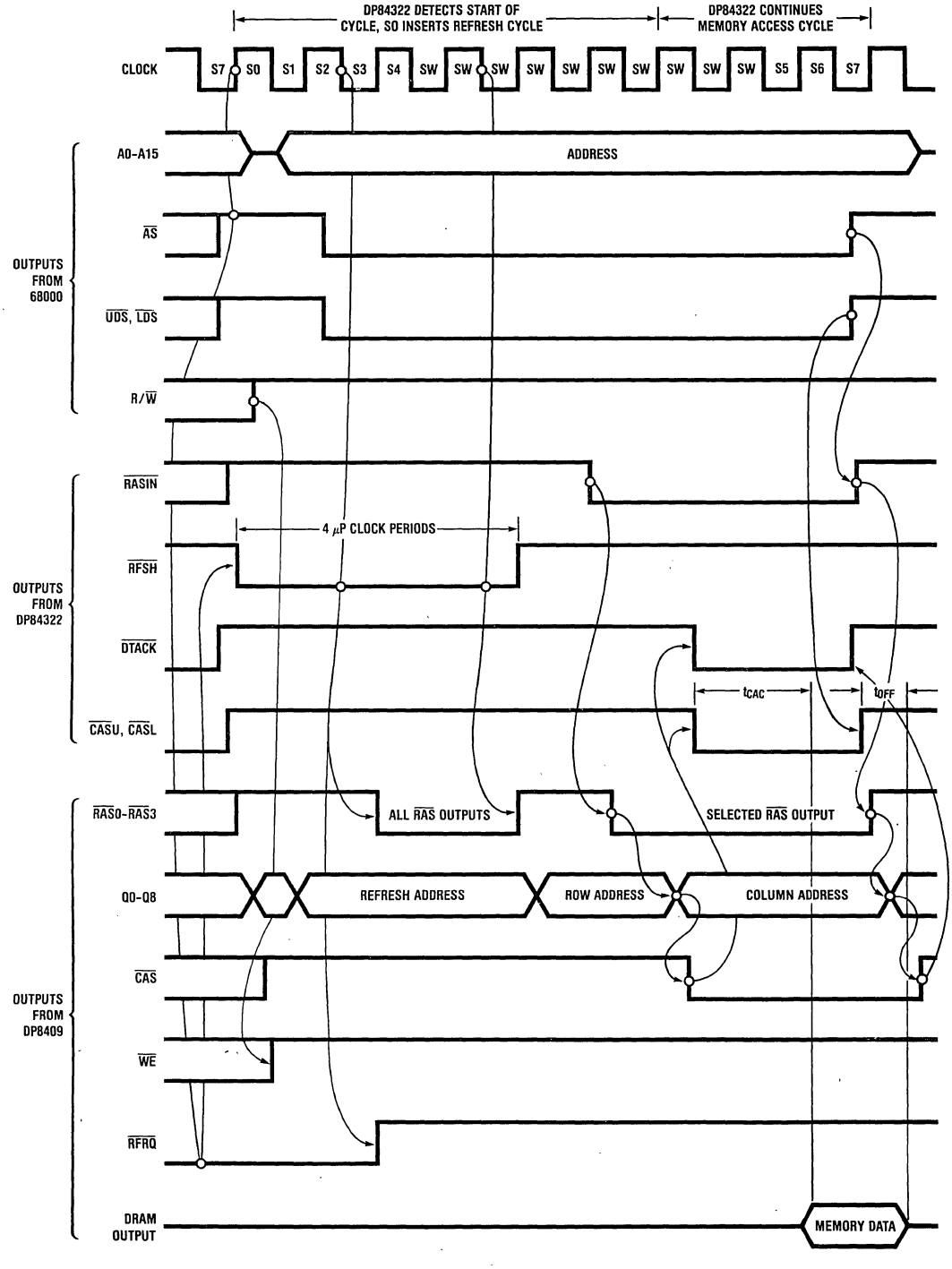
Timing Diagrams (Continued)

Memory Read Cycle (Wait = 1, Pin 5 = 0)



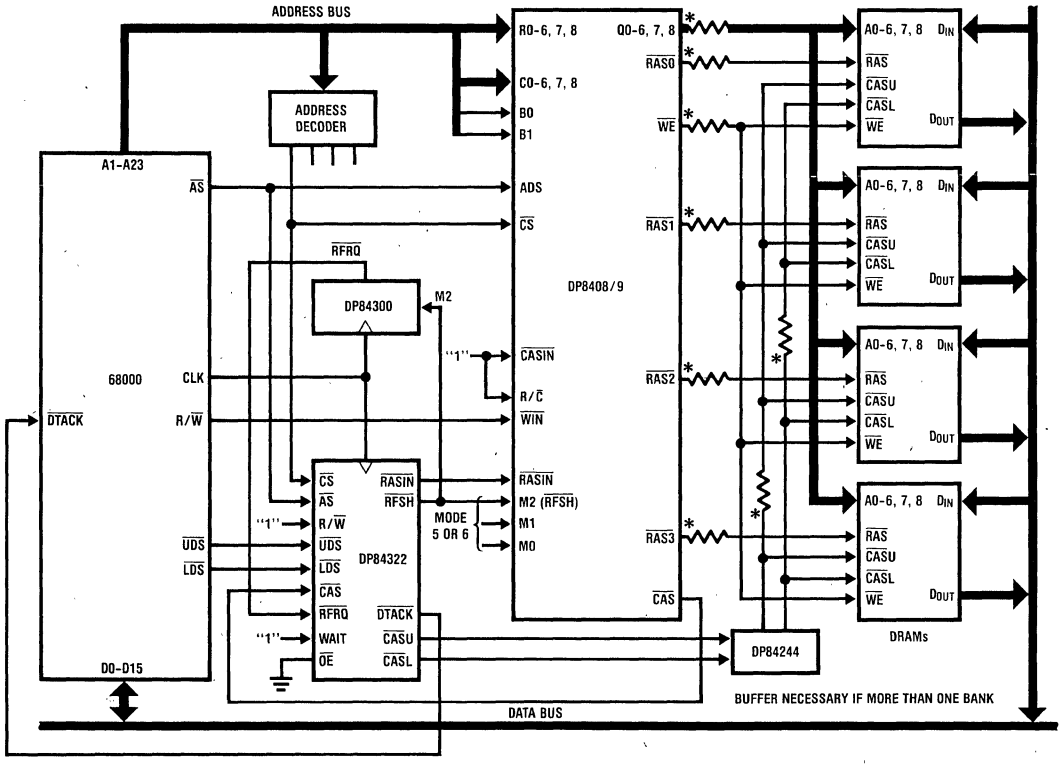
Timing Diagrams (Continued)

Memory Read Cycle and Forced Refresh (Wait = 1, Pin 5 = 0)



Modified System Block Diagram

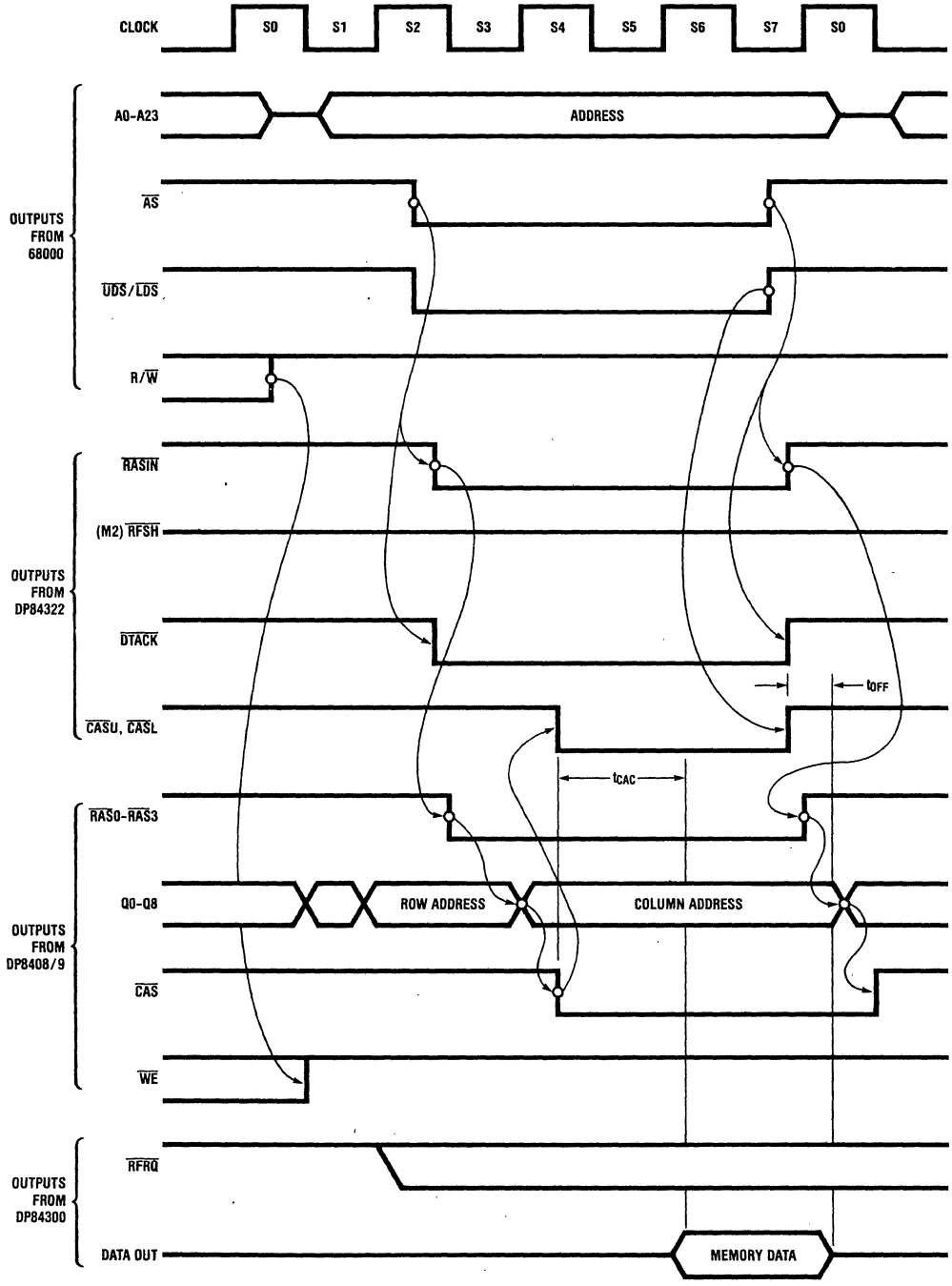
DP8408, DP8409 and 68000 Interface



*These outputs may need resistors.

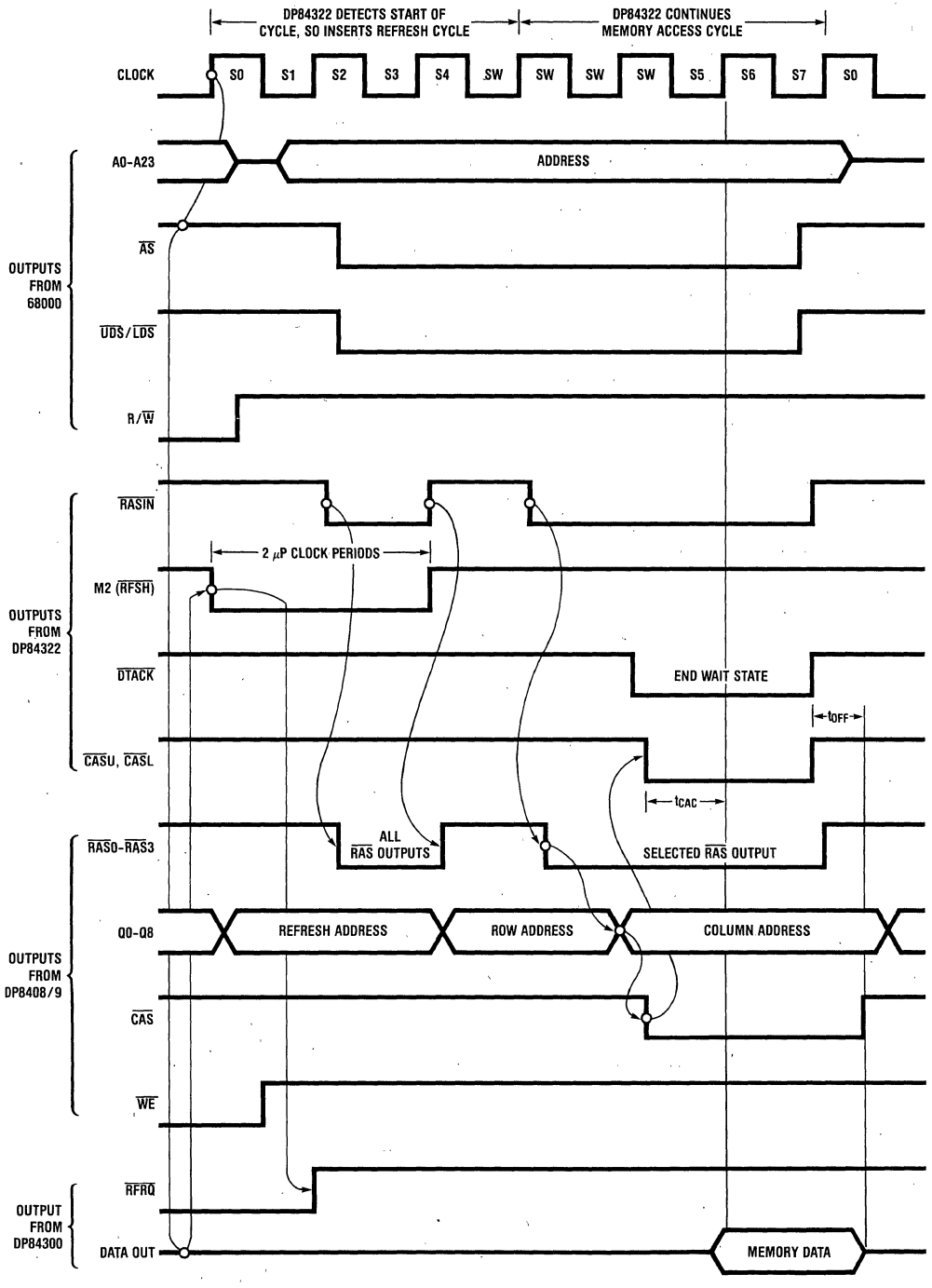
Timing Diagrams (Continued)

68000 Memory Read Cycle (Wait and Pin 5 = 1)



Timing Diagrams (Continued)

68000 Memory Read Cycle and Memory Refresh (Wait and Pin 5 = 1)



PAL16R4
DP84322
Dynamic RAM Controller Interface for the
MC68000-DP8409 Memory System
CK /AS /UDS /LDS R /RFRQ /CAS /CS WAIT GND
/OE /CL /CU /C /B /A /RFSH /DTACK /RASIN VCC

IF (VCC) RASIN = AS • /RFSH • /A +
RFSH • R • A • WAIT

IF (CS) DTACK = /R • CAS • WAIT +
UDS • /A • /B • /WAIT +
LDS • /A • /B • /WAIT +
AS • /R • /A • /B • /WAIT +
AS • /RFSH • R • /A • /B • WAIT

RFSH := /AS • RFRQ +
RFSH • /R • /C • WAIT +
RFSH • R • /A • WAIT +
RFSH • /C • /WAIT

A := RFSH

B: = A

C := B

IF (VCC) CU = UDS • CDS

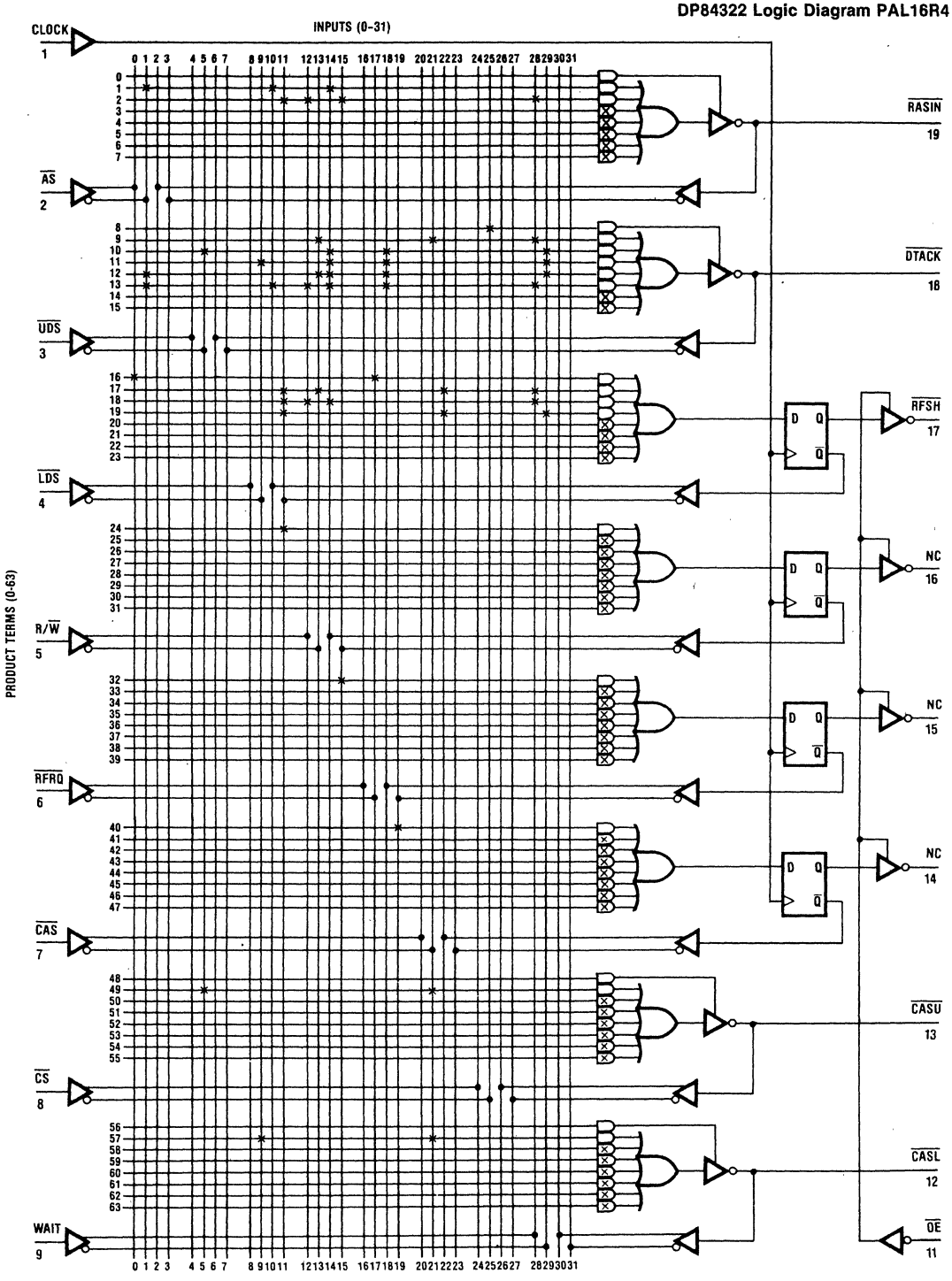
IF (VCC) CL = LDS • CAS

Function Table

CK	$\overline{AS}$	$\overline{UDS}$	$\overline{LDS}$	R	$\overline{RFRQ}$	$\overline{CAS}$	$\overline{CS}$	WAIT	$\overline{OE}$	$\overline{CL}$	$\overline{CU}$	$\overline{C}$	$\overline{B}$	$\overline{A}$	$\overline{RFSH}$	$\overline{DTACK}$	$\overline{RASIN}$
C	H	L	L	H	H	H	H	L	L	H	H	X	X	X	X	X	H
C	H	L	L	H	H	L	H	L	L	L	L	X	X	X	X	X	H
C	H	L	H	H	H	L	H	L	L	H	L	X	X	X	X	X	H
C	H	H	L	H	H	L	H	L	L	L	H	X	X	X	X	X	H
C	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	Z	H
C	L	L	H	H	H	H	L	L	L	H	H	H	H	H	H	L	L
C	L	L	H	H	H	L	L	L	L	H	L	H	H	H	H	L	L
C	L	H	H	H	H	L	L	L	L	H	H	H	H	H	H	H	L
C	L	H	H	L	H	L	L	L	L	H	H	H	H	H	H	L	L
C	L	L	H	L	H	L	L	L	L	H	L	H	H	H	H	L	L
C	H	H	H	L	H	H	L	L	L	H	H	H	H	H	H	H	H
C	H	H	H	L	L	H	L	L	L	H	H	H	H	H	L	H	H
C	H	H	H	L	L	H	L	L	L	H	H	H	H	L	L	H	H
C	L	H	L	L	H	H	L	L	L	H	H	H	L	L	L	H	H
C	L	H	L	L	H	H	L	L	L	H	H	L	L	L	L	H	H
C	L	H	L	L	H	H	L	L	L	H	H	L	L	L	H	H	H
C	L	H	L	L	H	H	L	L	L	H	H	L	L	H	H	H	L
C	L	H	L	L	H	L	L	L	L	L	H	L	H	H	H	L	L
C	L	H	L	L	H	L	L	L	L	L	H	H	H	H	H	L	L
C	H	H	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H
C	H	H	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H
C	H	H	H	L	L	H	L	H	L	H	H	H	H	L	L	H	H
C	L	L	L	L	H	H	L	H	L	H	H	H	L	L	L	H	H
C	L	L	L	L	H	H	L	H	L	H	H	L	L	L	L	H	H
C	L	L	L	L	H	H	L	H	L	H	H	L	L	L	H	H	H
C	L	L	L	L	H	H	L	H	L	H	H	L	L	H	H	H	L
C	L	L	L	L	H	L	L	H	L	L	L	L	H	H	H	L	L
C	H	H	H	L	H	L	L	H	L	H	H	H	H	H	H	L	H
C	H	H	H	L	H	H	H	H	L	H	H	H	H	H	H	Z	H
C	H	H	H	H	L	H	L	H	L	H	H	H	H	H	L	H	H
C	H	H	H	H	L	H	L	H	L	H	H	H	H	L	L	H	L
C	L	L	H	H	H	H	L	H	L	H	H	H	L	L	H	H	H
C	L	L	H	H	H	H	L	H	L	H	H	L	L	H	H	H	L
C	L	L	H	H	H	L	L	H	L	H	L	L	H	H	H	L	L
C	H	H	H	H	H	L	L	H	L	H	H	H	H	H	H	H	H
C	H	H	H	H	H	H	L	H	H	H	H	Z	Z	Z	Z	H	H

7

DP84322 Logic Diagram PAL16R4



National Semiconductor

Dynamic Memory Support
PRELIMINARY

DP84332 Dynamic RAM Controller Interface Circuit for the 8086 and 8088 CPUs

General Description

The DP84332 dynamic RAM controller interface is a Programmable Array Logic* (PAL) device which allows for easy interface between the DP8408 dynamic RAM controller and the 8086 and 8088 microprocessors. No wait states are required for memory access. Memory refreshing may be hidden (no wait states) or forced (up to three wait states).

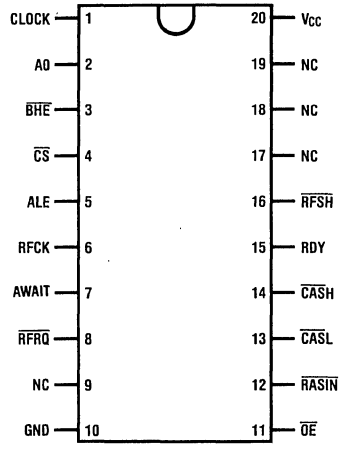
The DP84332 supplies all the control signals needed to perform memory read, write, and refresh. Logic is also included to insert a wait state when using slow memory.

Features

- Low parts count controller for the DP8408/DP8409
- Works with 8086 systems configured in min or max mode
- Performs hidden refresh using the DP8408 dynamic RAM controller
- Compatible with both the 8086 and 8088 microprocessors
- Capable of working at all CPU clock frequencies up to 8 MHz
- Standard National Semiconductor PAL part (DMPAL16R8)
- PAL logic equations can be modified by the user for his specific application and programmed into any of the PALs in the National Semiconductor family, including the new high speed PALs.

Connection Diagram

Dual-In-Line Package

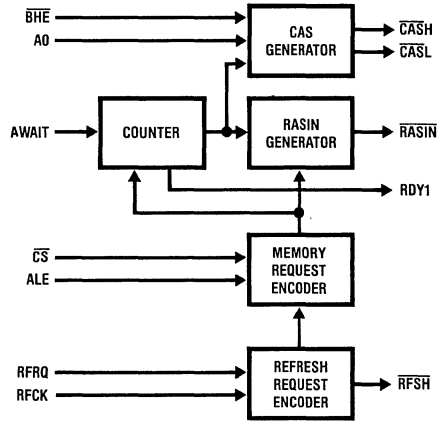


TOP VIEW

TL/F/5000-1

Order Number DP84322N-3
NS Package Number N20A

Block Diagram



TL/F/5000-2

*PAL is a registered trademark of Monolithic Memories, Inc.

Recommended Operating Conditions (Commercial)

	Min	Typ	Max	Units
V_{CC}, Supply Voltage	4.75	5.00	5.25	V
I_{OH}, High Level Output Current			−3.2	mA
I_{OL}, Low Level Output Current			24 (Note 2)	mA
T_A, Operating Free Air Temperature	0		75	°C

Electrical Characteristics over recommended operating temperature range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = Max	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = Max			0.5	V
I_{OZH}	Off-State Output Current High Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 2.4V, V_{IL} = 0.8V			100	μA
I_{OZL}	Off-State Output Current Low Level Voltage Applied	V_{CC} = Max, V_{IH} = 2V, V_O = 0.4V, V_{IL} = 0.8V			−100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−250	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max		150	225 (Note 1)	mA

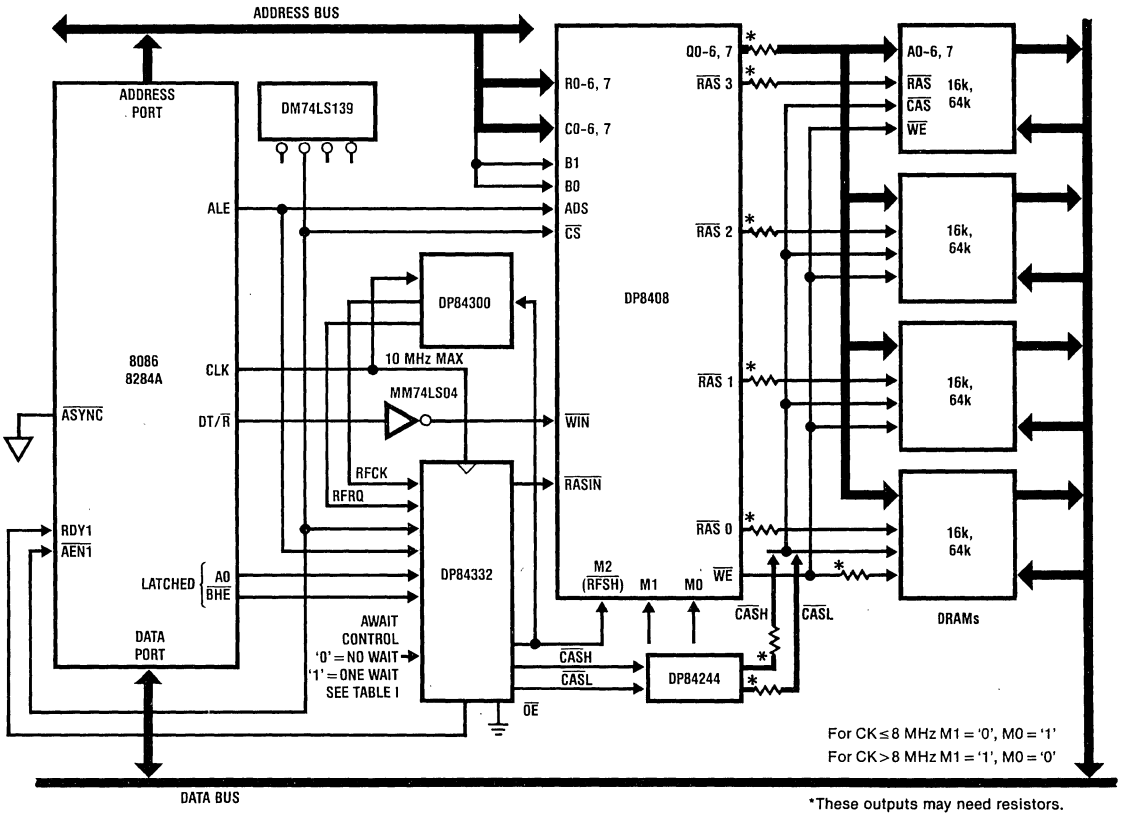
DP84332-3 Switching Characteristics over recommended ranges of temperature and V_{CC}

Symbol	Parameter		Conditions R_L = 667Ω	Commercial T_A = 0°C to +75°C V_{CC} = 5.0V ± 5%			Units
				Min	Typ	Max	
t_{PD}	Clock to Output		C_L = 45 pF		15	25	ns
t_{PZX}	Pin 11 to Output Enable		C_L = 45 pF		15	25	ns
t_{PXZ}	Pin 11 to Output Disable		C_L = 5 pF		15	25	ns
t_W	Width of Clock	High		25			ns
		Low		25			ns
t_{su}	Set-Up Time			40			ns
t_H	Hold Time			0	−15		ns

Note 1: I_{CC} = max at minimum temperature.
Note 2: One output at a time; otherwise 16 mA.

System Block Diagram

Interfacing the DP8408 to an 8086 System



Mnemonic Description

INPUT SIGNALS

CLOCK	The CLOCK signal determines the timing of the outputs and should be connected directly to the 8086 clock.
A0, $\overline{BHE}$	These inputs come from the 8086 CPU. They must remain stable during the memory cycle for proper operation of the $\overline{CAS}$ outputs.
$\overline{CE}$	Chip enable. This input is used to select the memory and enable the hidden refresh logic.
ALE	Address latch enable. This input is used to indicate the beginning of a memory cycle.
RFCK	Refresh clock. The period of this input determines the refresh interval. The duty cycle of this clock will determine the length of time that the circuit will attempt a hidden refresh.
AWAIT	When connected to V_{CC}, the DP84332 will insert an extra wait state in selected memory cycles.
$\overline{RFRQ}$	Refresh request. This input requests the DP84332 to perform a refresh. The state of the RFCK input will determine what type of refresh will be performed.

OUTPUT SIGNALS

$\overline{RASIN}$	This output provides a memory cycle start signal to the DP8408, and provides $\overline{RAS}$ timing during refresh.
$\overline{CASH}$, $\overline{CASL}$	These signals are the separate $\overline{CAS}$s needed for byte writing. Their presence is controlled by $\overline{BHE}$ and A0 respectively.
RDY	This output is used to insert a wait state into the 8086 memory cycles when selected and during a forced refresh cycle where the 8086 attempts to access the memory. The 8284A clock circuit should be configured so that ASYNC is enabled.
RFSH	This output controls the mode of the DP8408 dynamic RAM controller. When low, it switches the DP8408 into an all $\overline{RAS}$ refresh mode. This signal is also used to reset the refresh request logic.

Functional Description

A memory cycle starts when chip select ($\overline{CS}$) and address latch enable (ALE) are true. RASIN is supplied from the DP84332 to the DP8408 dynamic RAM controller, which then supplies a RAS signal to the selected dynamic RAM bank. After the necessary row address hold time, the DP8408 switches the address outputs to the column address. The DP84332 then supplies the required $\overline{CAS}$ signals ($\overline{CASH}$, $\overline{CASL}$) to the RAM. For byte operations, only one $\overline{CAS}$ will be activated. To differentiate between a read and a write, the DT/$\overline{R}$ signal from the CPU is inverted and supplied by the DP8408 to the memory array.

A refresh cycle is started by one of two conditions. One is when a refresh is requested (RFRQ is true), refresh clock (RFCK) is high, and a non-selected memory cycle is started (CE is not true, ALE is high). This is called hidden refresh because it is transparent to the CPU. In this case, the address supplied to the memories comes from the refresh counter in the DP8408, and no $\overline{CAS}$ signals are generated from the DP84332. The second form of refresh occurs when a refresh is requested, refresh clock is low, and there is no memory cycle in progress. This is called forced refresh, because the CPU will be forced to wait during the next memory cycle to allow for the refresh to be performed. In this case, a refresh is performed as before, but any attempt to access memory is delayed by wait states until after the refresh is finished. In either case, the refresh request is cleared by the refresh line ($\overline{RFSH}$) which also goes to the DP8408.

In a standard memory cycle, the access can be slowed down by one clock cycle to accommodate slower memories. This extra wait state will not appear during the hidden refresh cycle, so faster devices on the CPU bus will not be affected.

With higher speed systems, memory speed requirements will affect the performance of the system. Table I shows memory speed requirements at three different CPU clock speeds.

TABLE I. MEMORY SPEED REQUIREMENTS

CPU Clock Frequency	t_{CAC}		t_{RAH}
	No Wait States	1 Wait State	
8 MHz	≤105 ns	≤223 ns	≤30 ns
5 MHz	≤170 ns	≤370 ns	≤30 ns

t_{CAC} = access time from $\overline{CAS}$ including delay through buffers (DP84244)
t_{RAH} = row address hold time from $\overline{RAS}$

System Description

For memory operation, the DP84332 can be directly connected between the control signals from the CPU chip set and the DP8408 dynamic RAM controller. Each $\overline{CAS}$ output of the DP84332 is capable of driving eight memory devices. If additional drive is required, a DP84244 buffer can be used to increase the fanout to the full capabilities of the DP8408 (eight memories per output of the DP84244).

The 84332 is a standard National Semiconductor PAL part (DMPAL16R8). The user can modify the PAL equations to support his particular application. The 84332 logic equations, function table (functional test) and logic diagram can be seen at the end of this data sheet.

Refresh Request Logic

To generate the refresh request for the DP84332, external circuitry is required. *Figure 1* shows how this can be implemented, using standard SSI and MSI logic. A DM74LS393 counter is used to time the period between refresh cycles, while the DM74LS74 flip-flop is used to record the need of a new refresh. A better solution is to use the 24-pin DP84300 programmable refresh timer, as shown in *Figure 2*. This part allows a maximum amount of time for a hidden refresh to occur before lowering the refresh clock output, and implements the refresh request logic.

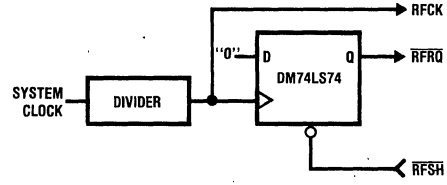


FIGURE 1. Using a Flip-Flop and a Counter for Refresh Request Logic

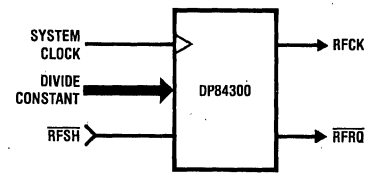
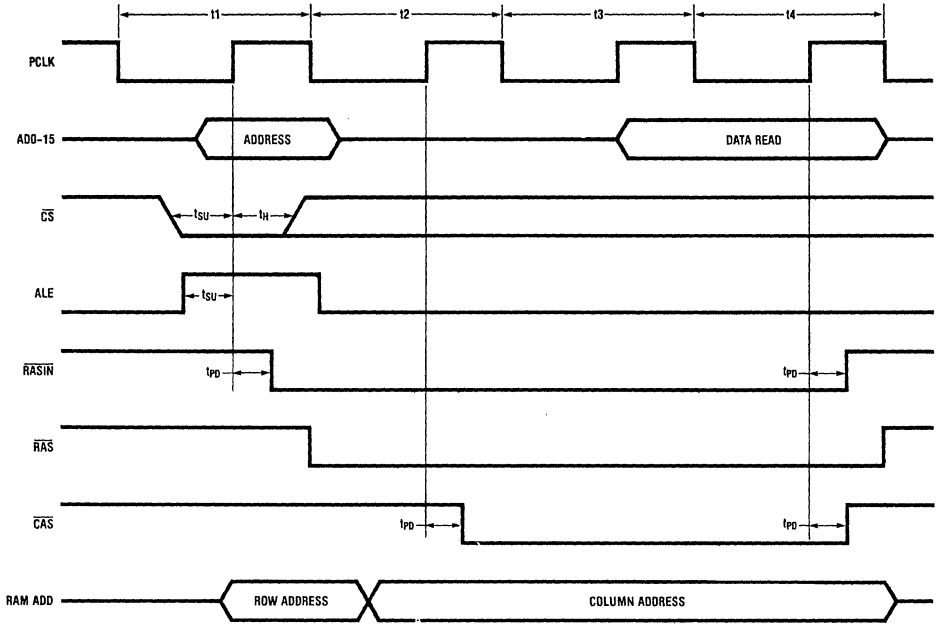


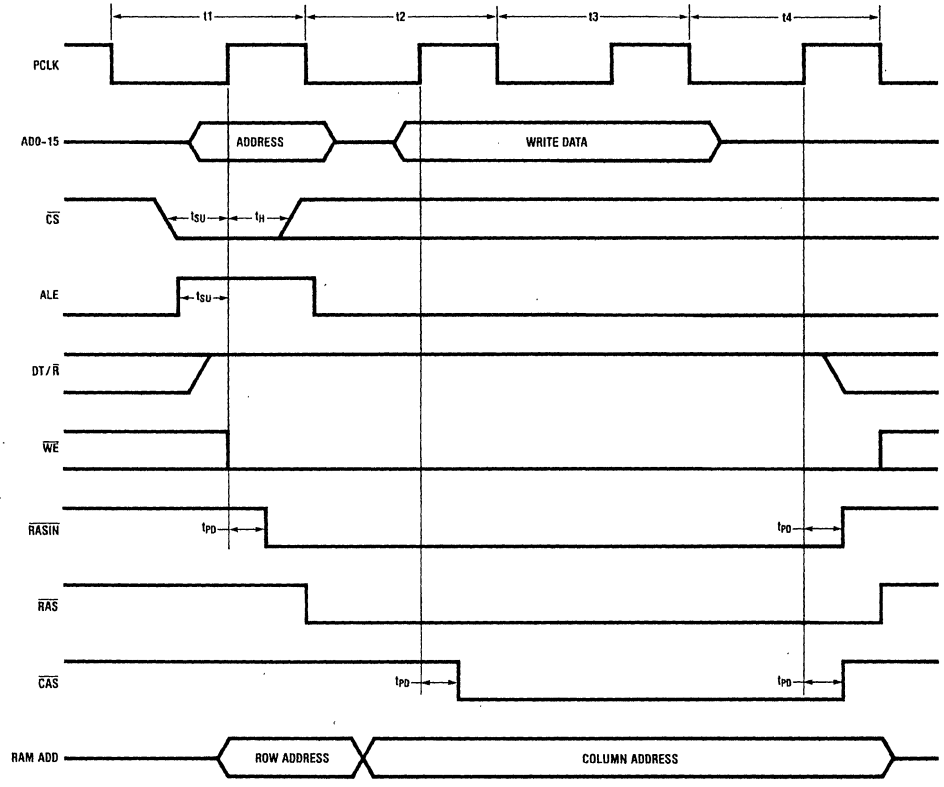
FIGURE 2. Using the DP84300 Refresh Counter for Refresh Request Logic

Timing Diagrams

Read Timing

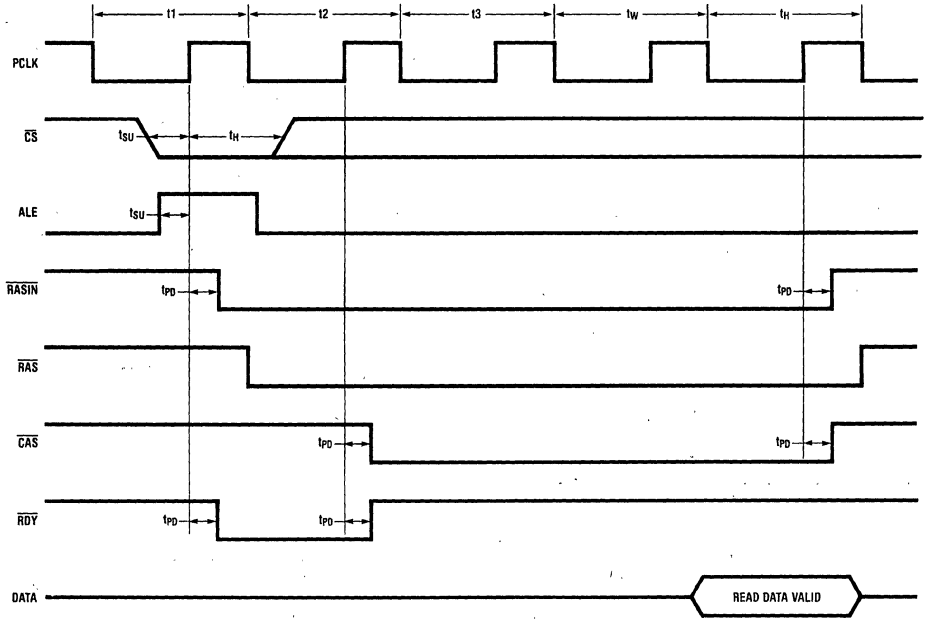


Write Timing

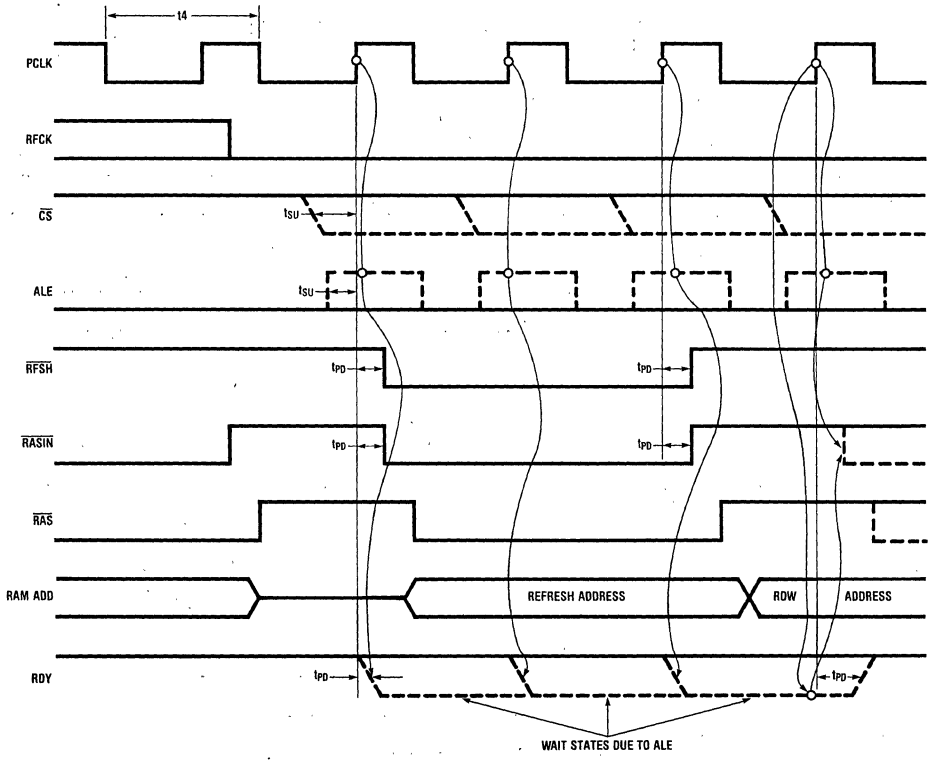


Timing Diagrams (Continued)

Memory Cycle with 1 Wait State

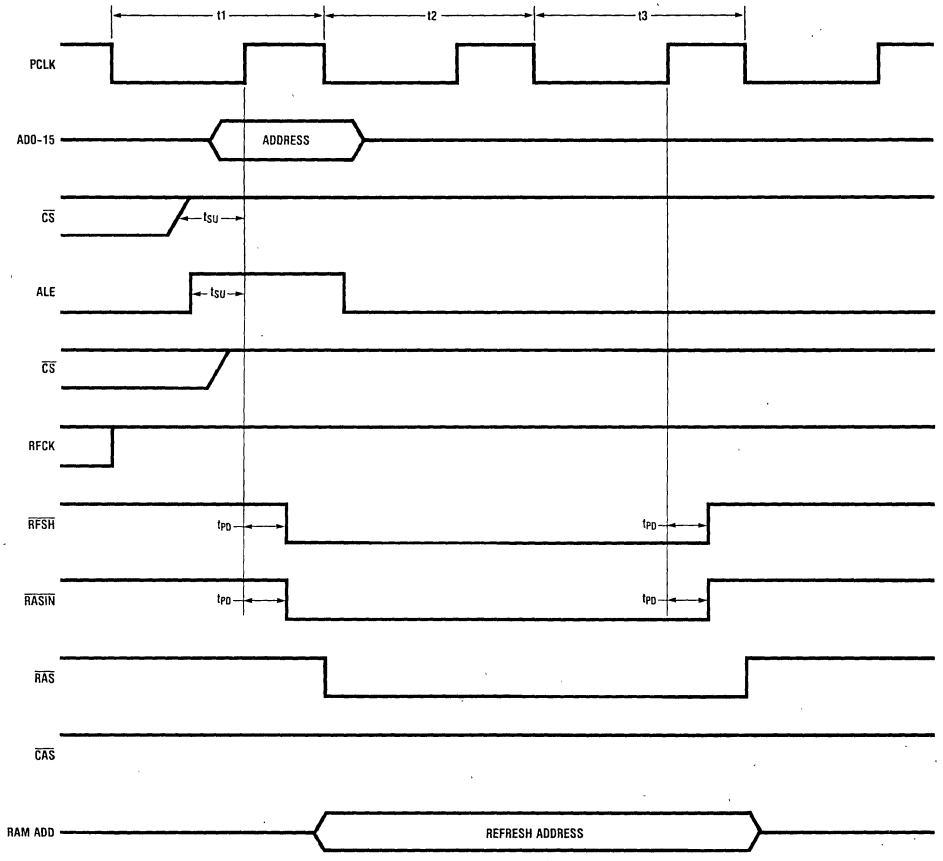


Forced Refresh



Timing Diagrams (Continued)

Transparent Refresh



16R8
DP84332
Dynamic RAM Controller Interface for the 8086-8408 System
CK A0 /BHE /CS ALE RFCK WAIT /RFRQ NC GND /OE /RASIN /CA /CB
RDY /RFSH /A /B /MRQ VCC

MRQ:= /RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • CS • ALE • /RFCK +
MRQ • RASIN +
RASIN • /CA • /CB • RDY • RFSH • /A • /MRQ • CS • ALE

B:= RASIN • /CA • /CB • RFSH • /A • /B +
RASIN • /CA • /CB • /RDY • /RFSH • /A • /B • WAIT +
RASIN • RDY • /RFSH • A • /B

A:= RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /WAIT +
RASIN • RDY • /RFSH • /A • B +
RASIN • RDY • /RFSH • A • /B

RFSH:= /RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • /CS • ALE • RFCK +
/RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • /RFCK +
RASIN • /CA • /CB • RFSH • /A • /B

/RDY:= /RASIN • /CA • /CB • RDY • /RFSH • /A • /B • MRQ • RFRQ • CS • ALE • /RCFK +
RASIN • /CA • /CB • RDY • RFSH • /A • /MRQ • CS • ALE +
/RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • /RFRQ • CS • ALE • WAIT +
/RASIN • /CA • /CB • /RDY • /RFSH • /A • /B • MRQ • /RFRQ • WAIT +
RASIN • /CA • /CB • /RDY • RFSH • /A +
/RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • CS • ALE • RFCK • WAIT

CB:= RASIN • /CA • /CB • /RFSH • /A • /B • BHE +
RASIN • CB • RDY • /RFSH • /A • B • WAIT +
RASIN • CB • RDT • /RFSH • A • /B

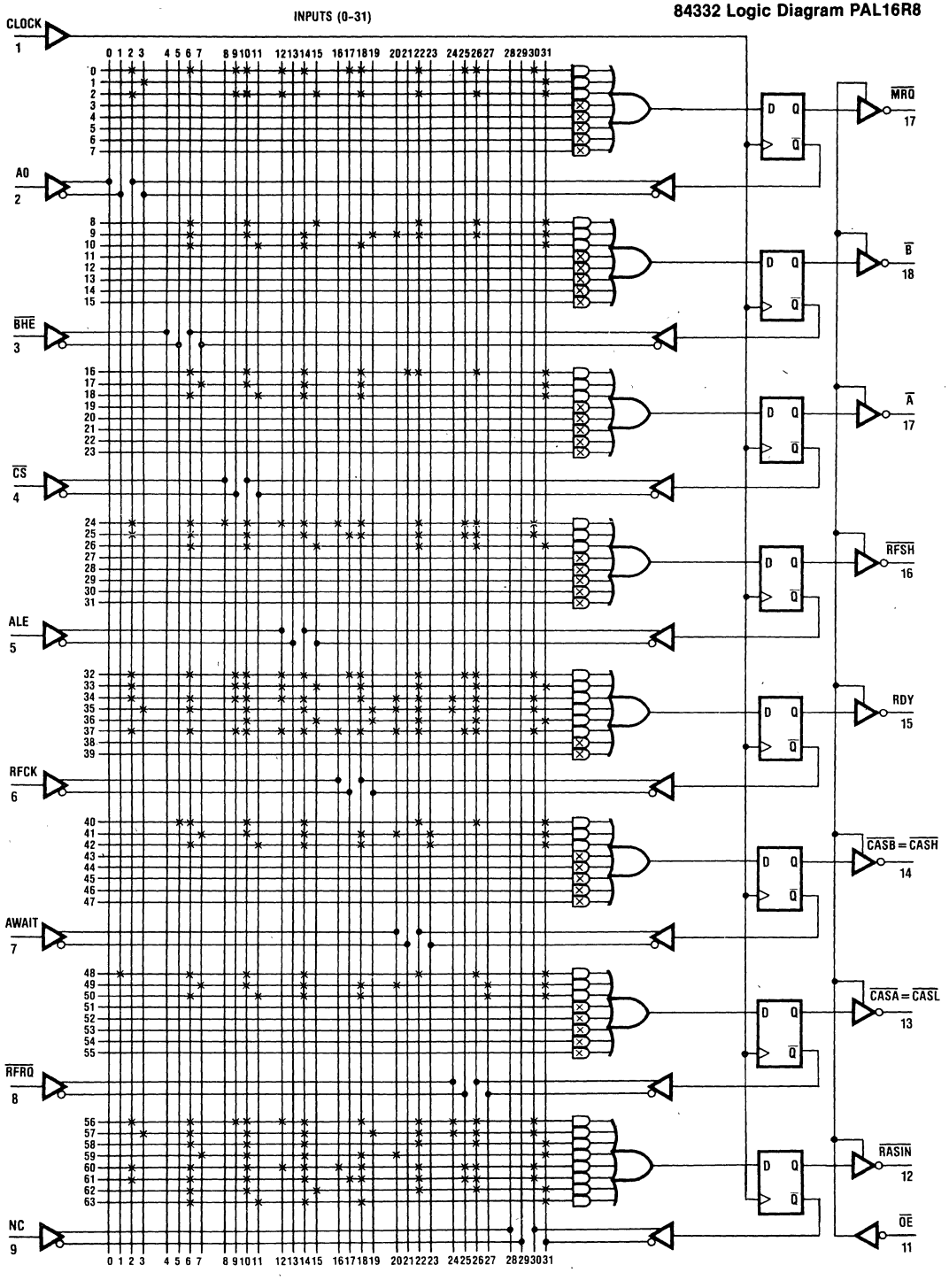
CA:= RASIN • /CA • /CB • /RFSH • /A • /B • /A0 +
RASIN • CA • RDY • /RFSH • /A • B • WAIT +
RASIN • CA • RDY • RFSH • A • /B

RASIN:= /RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • /RFRQ • CS • ALE +
/RASIN • /CA • /CB • /RDY • /RFSH • /A • /B • MRQ • /RFRQ +
RASIN • /CA • /CB • /RFSH • /A • /B +
RASIN • RDY • /RFSH • /A • B • WAIT +
/RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • ALE • RFCK +
/RASIN • /CA • /CB • RDY • /RFSH • /A • /B • /MRQ • RFRQ • /RFCK +
RASIN • /CA • /CB • RFSH • /A • /B +
RASIN • RDY • /RFSH • A • /B

Function Table

CK	A0	$\overline{BHE}$	$\overline{CS}$	ALE	RFCK	WAIT	$\overline{RFRQ}$	$\overline{OE}$	$\overline{RASIN}$	$\overline{CA}$	$\overline{CB}$	RDY	$\overline{RFSH}$	$\overline{A}$	$\overline{B}$	$\overline{MRQ}$
C	L	L	H	L	H	L	H	L	X	X	X	X	X	X	X	X
C	L	L	H	L	H	L	H	L	H	H	H	H	H	H	H	H
C	X	X	L	H	X	L	H	L	L	H	H	H	H	H	H	H
C	L	H	L	L	X	L	H	L	L	L	H	H	H	L	H	H
C	L	H	L	L	X	L	H	L	L	L	H	H	H	L	L	H
C	X	X	H	L	H	L	H	L	H	H	H	H	H	H	H	H
C	X	X	L	H	X	H	H	L	L	H	H	L	H	H	H	H
C	H	H	L	L	X	H	H	L	L	H	H	H	H	H	L	H
C	H	H	L	L	X	H	H	L	L	H	H	H	H	L	H	H
C	H	H	L	L	X	H	H	L	L	H	H	H	H	L	L	H
C	X	X	H	L	H	H	H	L	H	H	H	H	H	H	H	H
C	X	X	H	H	H	X	L	L	L	H	H	H	L	H	H	H
C	X	X	H	L	X	X	X	L	L	H	H	H	L	H	L	H
C	X	X	X	L	X	X	H	L	H	H	H	H	H	H	H	H
C	X	X	X	L	L	X	L	L	L	H	H	H	L	H	H	H
C	X	X	X	L	X	X	X	L	L	H	H	H	L	H	L	H
C	X	X	X	L	X	X	H	L	H	H	H	H	H	H	H	H
C	X	X	L	H	L	X	L	L	L	H	H	L	L	H	H	L
C	H	L	L	L	X	X	X	L	L	H	H	L	L	H	L	L
C	H	L	L	L	X	X	H	L	H	H	H	L	H	H	H	L
C	H	L	L	L	X	L	H	L	L	H	H	H	H	H	H	H
C	H	L	L	L	X	L	H	L	L	H	L	H	H	L	H	H
C	H	L	L	L	X	L	H	L	L	H	L	H	H	L	L	H
C	X	X	L	L	X	L	H	L	H	H	H	H	H	H	H	H
C	X	X	X	L	L	X	L	L	L	H	H	H	L	H	H	H
C	X	X	L	H	X	H	X	L	L	H	H	L	L	H	L	L
C	L	L	L	L	X	H	X	L	H	H	H	L	H	H	H	L
C	L	L	L	L	X	H	H	L	L	H	H	L	H	H	H	H
C	L	L	L	L	X	H	H	L	L	L	L	H	H	H	L	H
C	L	L	L	L	X	H	H	L	L	L	L	H	H	L	H	H
C	L	L	L	L	X	H	H	L	L	L	L	H	H	L	L	H
C	X	X	L	L	X	H	H	L	H	H	H	H	H	H	H	H
C	X	X	L	H	H	H	L	L	L	H	H	L	H	H	H	H
C	X	X	L	L	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z

84332 Logic Diagram PAL16R8



8086 PAL

Interfacing the DP8408/09 To Various Microprocessors

National Semiconductor
Application Note AN-309
Chuck Pham
June 1982

High storage density and low cost have made dynamic RAMs the designer's choice in most memory applications. However, the major drawback of dynamic RAMs is the complex timing involved. First, a $\overline{RAS}$ must occur with the row address previously set up on the multiplexed address bus. After the row address has been held for some minimum time after $\overline{RAS}$ (namely the row address hold time of the dynamic RAMs, t_{RAH}), the column address is set up and then $\overline{CAS}$ occurs. In addition, refreshing must be done periodically to keep all memory cells charged.

With the introduction of the DP8408 Dynamic RAM Controller/Driver, the above complexities are simplified. The DP8408 is housed in a 48-pin package with eight multiplexed address outputs (Q0-7) and six control outputs ($\overline{RAS}$0-3, $\overline{CAS}$, $\overline{WE}$). It consists of two 8-bit address latches and an 8-bit refresh counter. All the output drivers are capable of driving 500pF loads.

The following discussion demonstrates a typical application of the DP8408 Dynamic RAM Controller/Driver in Z8000™- and Z80®-based systems. The DP8408 basically has six modes of operation: Externally Controlled Refresh, Externally Controlled All-$\overline{RAS}$ Write, Externally Controlled Access, Auto Access (slow t_{RAH}), Auto Access (fast t_{RAH}) and Set End of Count.

The DP8408, operating in the auto access mode, requires only $\overline{RASIN}$ to initiate a memory access cycle because all the dynamic RAM's control signals are automatically delayed from this input. (Refer to *Figure 1* for the auto access timing sequence.)

In the following applications, the DP8408 operates in either mode 5 or mode 6 Auto Access and mode 1 or 2 Externally Controlled Refresh to provide minimum additional logic.

The DP8408 and Z8000 Interface

Memory Access Cycle:

Figure 2a shows the detailed block diagram of the Z8000 and the DP8408 interface. Consider a memory cycle of the Z8000; first, the memory address is output on the Address and Data multiplexed bus (AD0-15) during T1 and is latched to the DP8408 by $\overline{AS}$. Simultaneously, $\overline{MREQ}$ goes low and is used to provide $\overline{RASIN}$ to initiate a memory transaction cycle. Then the selected $\overline{RAS}$ output, row address hold time (t_{RAH}), column address set up time (t_{ASC}) and $\overline{CAS}$ output will follow $\overline{RASIN}$ as determined by the auto access modes. A maximum of one wait state is required for 6MHz and 10MHz CPUs. This wait state is automatically inserted by the $\overline{CAS}$ output of the DP8408. For systems using byte-writing, the DM74S158 provides two separate $\overline{CAS}$ outputs for accessing the low and high byte of memory. Note that $\overline{DS}$ from the Z8000 is also gated with the DP8408's CAS output to generate $\overline{CASL}$ and $\overline{CASH}$. This guarantees the valid data from the Z8000 being written into memory during memory write cycles. Refer to *Figure 3* for the detailed memory transaction cycle timing.

The following formula allows the designer to determine the proper memory speed in terms of t_{CAC} (access time from $\overline{CAS}$):

$$t_{CAC}\ \text{max.} = 3 \times t_{cC} - tdc(MR) - t_{RICL} - t_{CASdly} - t_{sDR}(C) - 15.$$

The Z8000 parameters:

t_{cC}: clock cycle time
$t_{sDR}(C)$: read data to clock ↓ set up time
tdc(MR): clock to $\overline{MREQ}$ delay

The DP8408, 74S158 and 74LS245 parameters:

t_{RICL}: RASIN to CAS delay
t_{CASdly}: the propagation delay of the 74S158
15ns: the propagation delay of the 74LS245 (at 50pF load)

For the 10MHz CPU and the DP8408:

t_{CAC} max. = 300 − 40 − 131 − 14 − 10 − 15 = 90ns.

- t_{RICL} max. (mode 6) = 131ns at 15pF load.
- t_{CASdly} max. = 14ns at 50pF load.

Since $\overline{MREQ}$ is connected directly to $\overline{RASIN}$, t_{RP} ($\overline{RAS}$ precharge time) and t_{RAS} ($\overline{RAS}$ pulse width) are determined by $\overline{MREQ}$ high and low, respectively.

Memory Refresh Cycle:

The Z8000 CPU contains a refresh rate counter for automatic memory refresh. This counter should be programmed during the processor initialization to determine the refresh rate. Since memory refresh is automatically inserted by the Z8000, there is no additional refresh arbitration logic allowed. The CPU's STATUS 3 (ST3) output can be directly connected to the M2 ($\overline{RFSH}$) pin of the DP8408. During the memory refresh cycle, ST3 goes low, setting the DP8408 in the external control refresh mode (mode 2). Then all four $\overline{RAS}$ outputs will follow $\overline{MREQ}$ to strobe the DP8408's refresh address to all memory banks (the Z8000 refresh address is ignored). As $\overline{MREQ}$ goes high again, the DP8408 increments its refresh counter, preparing it for the next refresh cycle. Refer to *Figure 4* for the refresh cycle timing. Note that ST3 also goes low during the internal cycle, I/O reference cycle and interrupt acknowledge cycle, but the memory will not be refreshed because $\overline{MREQ}$ is not active during these cycles. The DP8408 on-chip refresh counter will not be incremented when M2 goes low unless $\overline{MREQ}$ is inserted.

PAL is a registered trademark of Monolithic Memories, Inc.
Z80 and Z80A are registered trademarks of Zilog Corp.
Z8000 is a trademark of Zilog Corp.

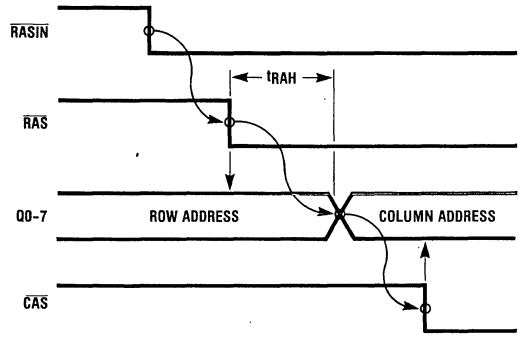


Figure 1. Auto Access Timing Sequence (Mode 5 or Mode 6)

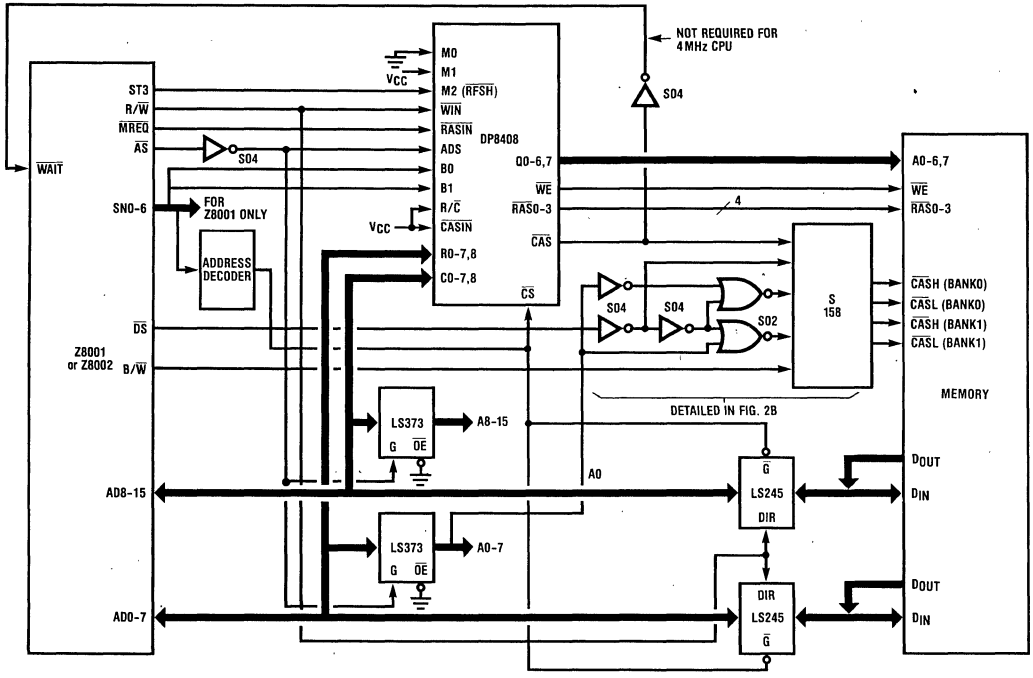


Figure 2a. Z8000 and DP8408 Interface

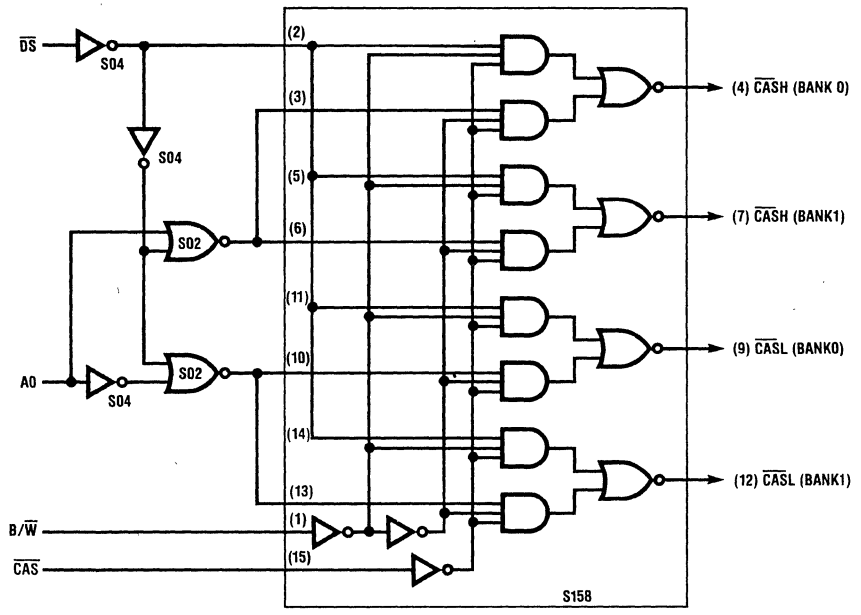


Figure 2b. CASH and CASL Decoder

When the processor is in either halt state (by executing the privileged HALT instruction) or single-stepping mode (when STOP input is low), it introduces memory refresh cycles. However, care should be taken when the CPU is in either a WAIT state or a Bus Acknowledge cycle, that the dynamic RAM refresh will not take place. If these conditions occur over a long period of time, a burst refresh is recommended. This can be done by toggling RASIN while keeping M2 low, until all the rows of the dynamic RAM have been refreshed, then the CPU can resume its operations.

The DP8408 and Z80A® Interface

Instruction Fetch Cycle:

Figure 5 shows the detailed interconnections between the DP8408, the Z80® and the Dynamic RAMs. *Figure 6* shows the timing during an M1 cycle (op code fetch). The program counter is output on the address bus at the beginning of the M1 cycle. One-half clock later, MREQ goes active. This input is used to provide RASIN to the DP8408 to access the dynamic memory. Subsequently, the selected RAS output, Row to Column Select and then CAS output will automatically follow RASIN as determined by the Auto Access modes of the DP8408. The RD line also goes active to indicate a memory read cycle is in progress. After t_{CAC} (access time from CAS), read data becomes valid. This data is sampled on the rising edge of T3, then both MREQ and RD go inactive. Immediately following this, RFSH goes low, putting the DP8408 in the Externally Controlled Refresh mode. The MREQ goes active causing all four RAS outputs to go active to perform a refresh to all the banks of the dynamic RAMs. Note that during memory refresh cycles, the refresh address from the CPU is output on the address bus. However, the contents of the DP8408 on-chip refresh counter are used instead to provide the row address to the dynamic memory array. Since the Z80 provides only a 7-bit refresh address, it is an advantage to use the DP8408 8-bit refresh counter to support 64k dynamic RAMs directly. The DP8408 refresh counter is incremented as MREQ returns high, ending the memory refresh. The RFSH goes inactive returning the DP8408 back to the Auto Access mode, preparing it for the next access cycle.

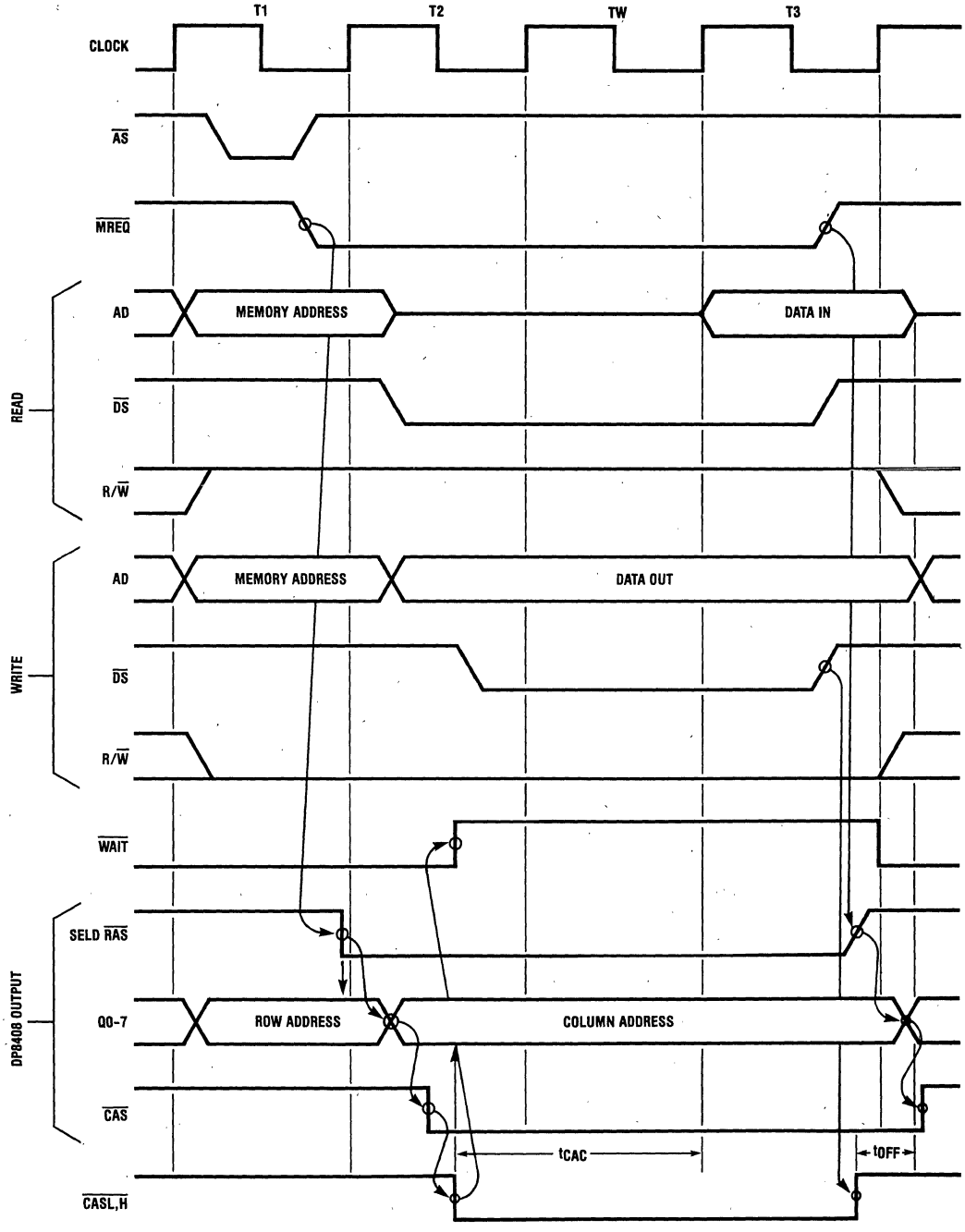


Figure 3. Memory Transaction Cycles

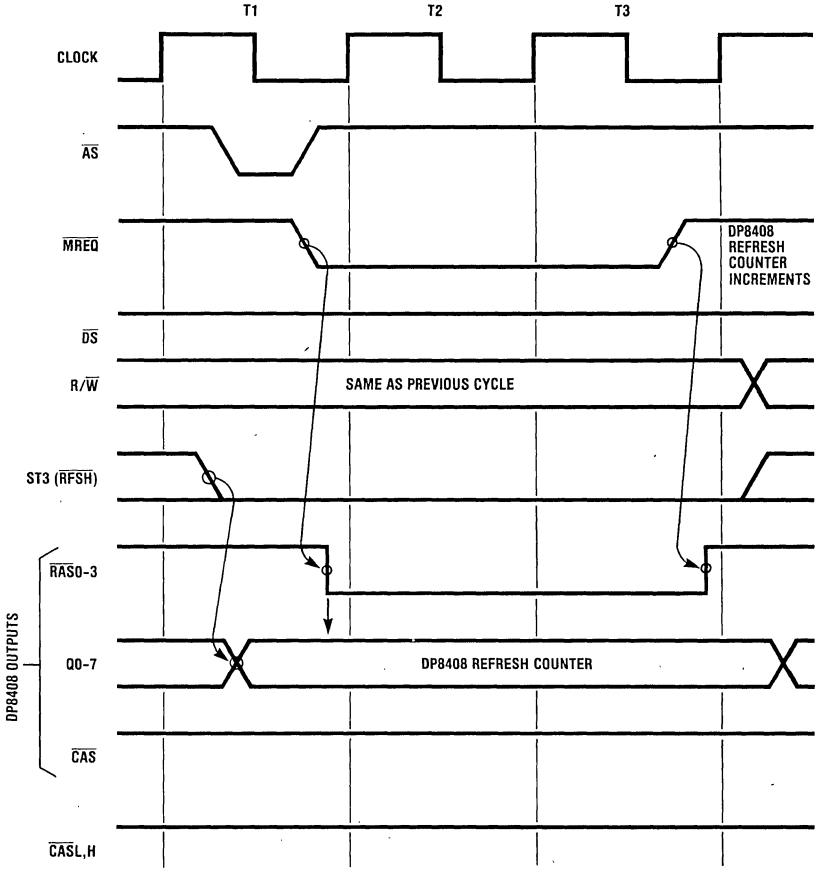


Figure 4. Memory Refresh Cycle

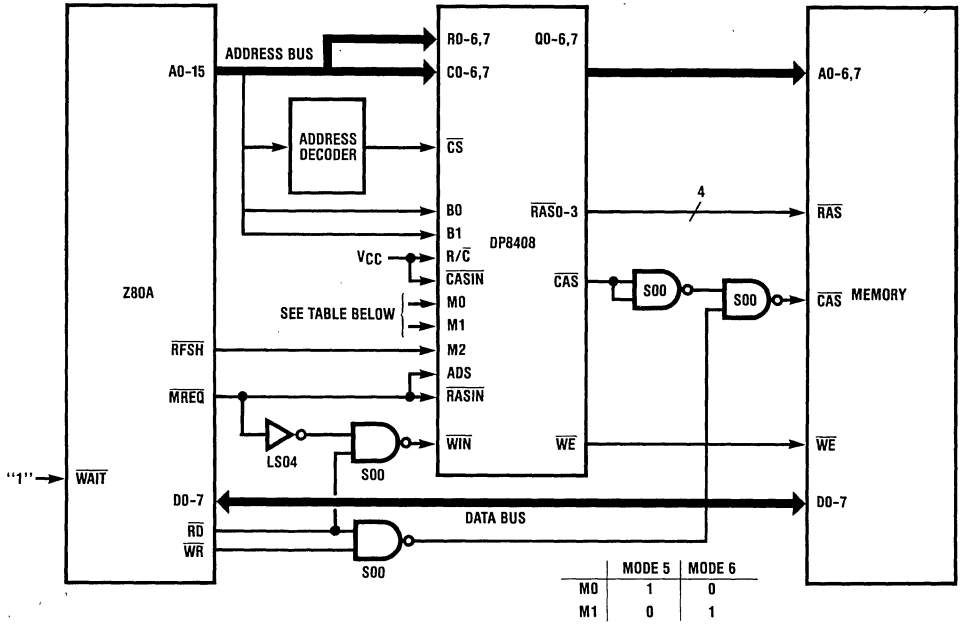


Figure 5. DP8408 and Z80A Interface

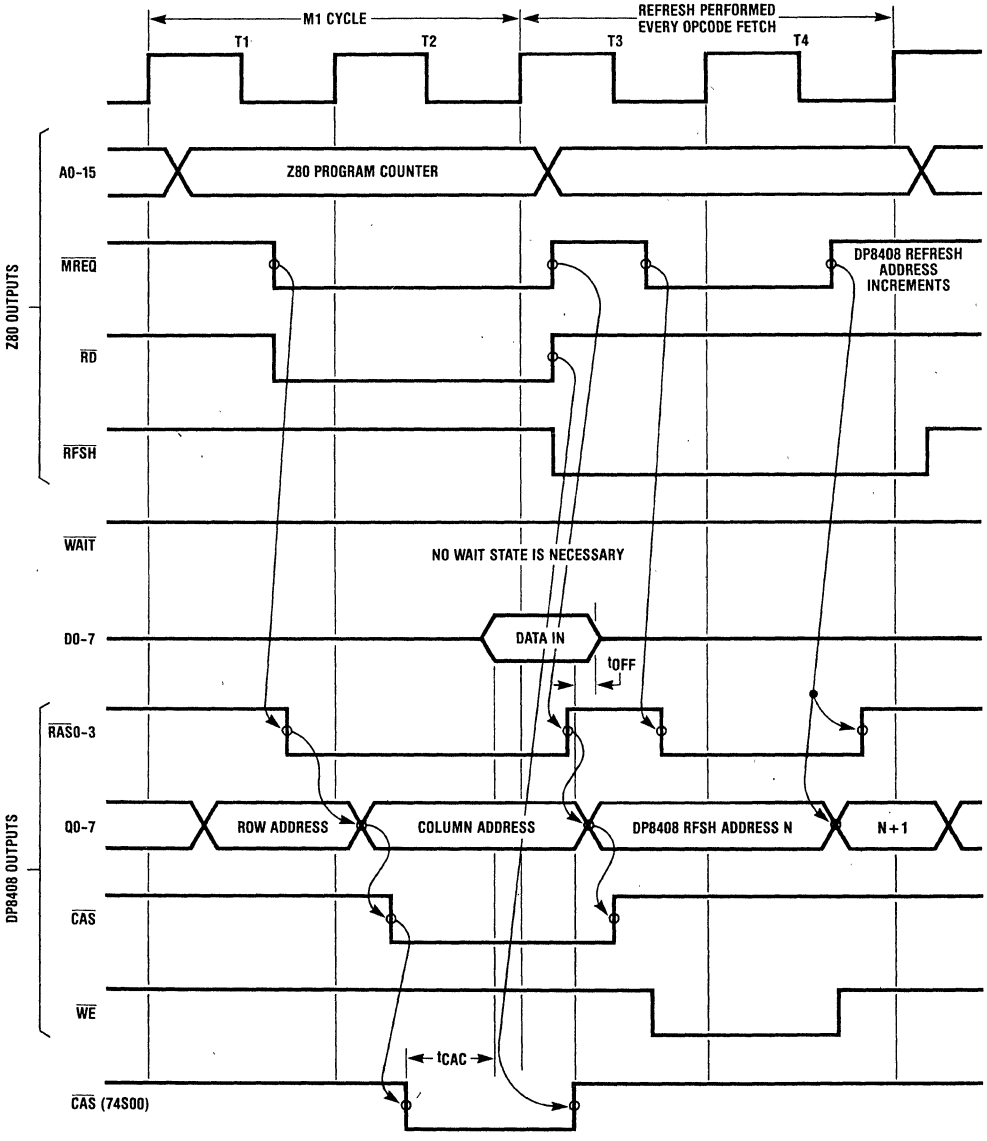


Figure 6. Z80A Op Code Fetch Cycle Showing Memory Refresh

Memory Access Cycle:

Figure 7 shows the timing of the memory read and memory write cycle other than for the M1 op code fetch cycle. Similar to the op code fetch cycle, $\overline{MREQ}$ is used to provide $\overline{RASIN}$. $\overline{MREQ}$ goes active after the address to the memory has had time to stabilize. Again, $\overline{RAS}$ output, Row to Column Select and then $\overline{CAS}$ output will automatically follow $\overline{RASIN}$ to access the specified memory location. For a memory read cycle, both $\overline{MREQ}$ and $\overline{RD}$ go active, and as a result, $\overline{WIN}$ remains high (refer to *Figure 5*), which allows a memory read operation to occur. On the other hand, only $\overline{MREQ}$ goes active during a write cycle, which forces $\overline{WIN}$ low, indicating an early write cycle. It should be noted that the $\overline{CAS}$ output to the memory array will not go low until $\overline{WR}$ goes low during memory write cycles as this guarantees the valid CPU data will be written into memory.

It is worth mentioning that the Z80 CPU provides powerful block transfer instructions. An example is the LDIR (load, increment and repeat); using only this instruction, the programmer can move any block of data from the location pointed to by the D and E registers. This operation is repeated until the byte counter (B and C registers) reaches zero. Thus, this single instruction can move any block of data from one location to any other. Due to the fact that this instruction is refetched after each data byte transfer, the memory refresh cycle always takes place even though a transfer of up to 64k bytes of data may be performed. Furthermore, when the CPU has executed the software HALT instruction and is waiting for an interrupt before normal CPU operations can resume, the CPU executes NOP instructions to maintain memory refresh activity.

However, care should be taken when the CPU is in either WAIT state or a Bus Acknowledge cycle, the dynamic RAM refresh will not take place. If these conditions occur long enough, a burst refresh is recommended, and it can be done by toggling $\overline{RASIN}$ while keeping M2 low until all the rows of the dynamic RAM have been refreshed before the CPU can resume its operation.

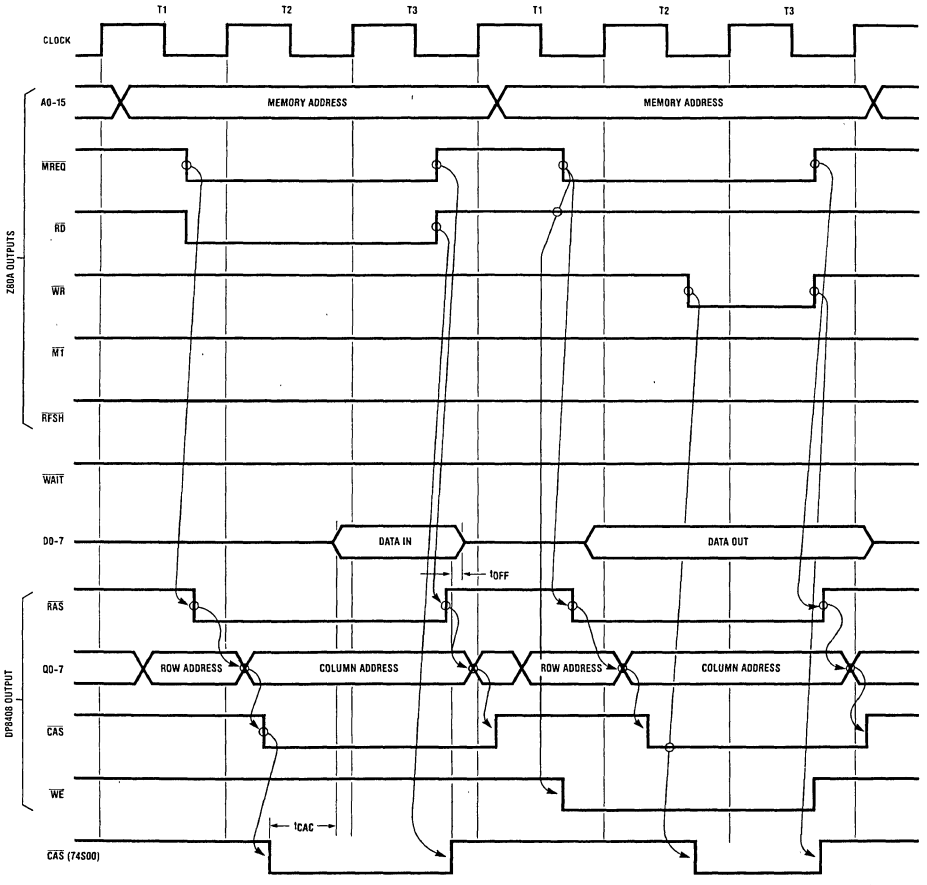


Figure 7. Z80A Memory Read and Memory Write Cycle

The following formulas allow designers to select the appropriate dynamic memory, based on different CPU and DP8408 speed versions, to allow the CPU full speed of operation:

max. t_{CAC}: $1.5 \times t_{Cmin} - t_{DL\phi}(MR) - tRICL - t_{CASDLY} - t_{S\phi}(D)$

min. t_{RP}: $tw(MRH) = tw(\phi H) + t_f - 20$

min. t_{RAS}: $tw(MRL) - 20 = t_C - 50$

Dynamic RAM Parameters:

t_{CAC}: access time from $\overline{CAS}$

t_{RP}: $\overline{RAS}$ precharge time

t_{RAS}: $\overline{RAS}$ pulse width

Z80 Parameters:

t_C: clock period

$tw(\phi H)$: clock pulse width, clock high

tf: clock fall time

$t_{DL\phi}(MR)$: $\overline{MREQ}$ delay from falling edge of clock, $\overline{MREQ}$ low

$t_{S\phi}(D)$: Data set up time to rising edge of clock during M1 cycle

DP8408 and 74S00 Parameters:

t_{RICL}: $\overline{RASIN}$ to $\overline{CAS}$ output delay

t_{CASDLY}: propagation delay of the two 74S00 NAND gates

For example, if the Z80A (4MHz) and the DP8408 are used, then:

max. t_{CAC}: $1.5(250) - 85 - 132 - 13 - 50 = 95$ns

min. t_{RP}: $110 + 20 - 20 = 110$ns

min. t_{RAS}: $t_C - 50 = 200$ns

t_{RICL} max. (mode 6): 132ns at 15pF load

t_{CASDLY} max.: 13ns at 50pF load

Therefore, in this case, the designer should choose a dynamic memory which has maximum t_{CAC} of 95ns, minimum t_{RP} of 110ns and minimum t_{RAS} of 200ns.

DP8409 and MC68B09E Interface

DP8409 Overview:

The DP8409 Dynamic RAM Controller/Driver is designed to control all multiplexed-address dynamic RAMs. It consists of two 9-bit address latches and a 9-bit refresh counter, thus allowing control of all 16k, 64k, and the coming generation 256k dynamic RAMs. More important, all the DP8409 outputs are capable of driving 500pF loads.

The DP8409 basically has eight modes of operation: Externally Controlled Refresh, Automatic Forced Refresh, Internal Auto Burst Refresh, All $\overline{RAS}$ Auto Write, Externally Controlled Access, Auto Access (slow t_{RAH} and with hidden refresh), Fast Auto Access (fast t_{RAH}) and Set End of Count. Of all these modes, Auto Access (mode 5) and Auto Forced Refresh (mode 1) are the most popular and will be used throughout this application. Mode 5 requires only $\overline{RASIN}$ to initiate a memory access cycle, because all the dynamic RAM's control signals are automatically delayed from this input, as shown in *Figure 1*. To attain maximum system throughput, it is obviously advantageous to perform refreshes without interrupting the system. The DP8409 can do this by monitoring the $\overline{CS}$ input to see if it is high. If $\overline{CS}$ is high, the RAMs are not being accessed. If $\overline{CS}$ is high for one cycle, the DP8409 performs a hidden refresh during this cycle, and stops in time for the system to start another access. But if a hidden refresh does not occur in a specific time slot, a refresh must be forced and this can be done by using Mode 1, Automatic Forced Refresh.

To perform automatic forced refresh, the DP8409 must receive two clock signals: the refresh period clock, RFCK, and RGCK, the $\overline{RAS}$-generator clock; RGCK can be the microprocessor clock. It takes approximately four RGCK clock periods to perform this automatic forced refresh. The DP8409 gives preference to hidden refresh using RFCK as a level reference. The refresh time slot commences as RFCK goes high. If $\overline{CS}$ goes high while RFCK is high, the refresh counter is enabled in the address outputs. All four $\overline{RAS}$ outputs follow $\overline{RASIN}$; so to perform a hidden refresh, $\overline{RASIN}$ must be set low and the refresh counter gets incremented as $\overline{RASIN}$ goes high. The DP8409 allows only one such hidden refresh to occur with a clock cycle of RFCK to minimize power consumption.

If a hidden refresh does not occur the DP8409 must force a refresh before RFCK begins a new cycle on a low-to-high transition. Therefore, as RFCK goes low (and a hidden refresh has not occurred), RF I/O (Refresh Request) goes low, requesting that a refresh be performed. When the system acknowledges the request, it sets M2 low, and prevents further access to the DP8409. Then two RGCK negative edges after M2 has gone low, all four $\overline{RAS}$ outputs go low and and remain low for two RGCK clock periods. After all four $\overline{RAS}$ outputs have gone low, M2 can go high any time to end the Automatic Forced Refresh. The DP8409 allows only one automatic refresh to occur within a clock cycle of RFCK.

Memory Access:

The MC68B09E starts a memory access cycle when E goes low, then the memory address becomes valid on the Address Bus A0-15. This address is decoded to provide Chip Select ($\overline{CS}$) to the DP8409. Then Q goes high and sets $\overline{RASIN}$ low from the PAL® Control Logic as shown in *Figure 12*. Note that $\overline{CS}$ must go low for a minimum of 10ns before the assertion of $\overline{RASIN}$ for a proper memory access. This is important because a false hidden refresh may take place when this 10ns minimum setup time is not met. $\overline{RASIN}$ goes low initiating the auto access sequence as shown in *Figure 1*. Mode 5 guarantees a 30ns minimum for row address hold time and a minimum of 8ns column address set up time. $\overline{RASIN}$ remains low until E goes low at the end of the current access cycle. Using the 16R6 A-1 Programmable Array Logic (25ns PAL), the maximum access time from $\overline{CAS}$ of the selected dynamic RAM is determined as follows:

Max. t_{CAC}: $3 \times 125 - 25 - 160 - 40 = 150$ ns 8409

t_{CAC}: $3 \times 125 - 25 - 130 - 40 = 180$ ns 8409-2

Q high to E low: 3×125 ns (8 MHz clock) $= 375$ ns

Q high to $\overline{RASIN}$ low: 25ns (16R6 A-1 PAL Parameter)

$\overline{RASIN}$ to $\overline{CAS}$ Output low: 160ns (DP8409's t_{RICL}, Mode 5, at 500pF load)
130 ns (DP8409-2's t_{RICL})

Read data setup time (before E going low): 40ns

Memory Refresh:

As described above, $\overline{RASIN}$ goes active when Q and/or E are high. This scheme, therefore, maximizes chances for hidden refresh because $\overline{CS}$ is high during nondynamic memory cycle. For example, when the CPU is executing internal operation or the CPU is accessing ROM or I/O, $\overline{CS}$ is high during these times. The DP8409 therefore performs a hidden refresh as $\overline{RASIN}$ goes low, assuming that RFCK is high.

However, if no hidden refresh occurs while RFCK was high, RF I/O goes low immediately after the RFCK high-to-low transition requests a forced refresh. The PAL Control Logic samples RF I/O, when E and Q are high and low respectively, to set M2 (RFSH) low, as shown in *Figure 13*. Once M2 has gone low, a forced refresh automatically occurs (as described in the DP8409 Overview). M2 remains low for four system clock periods to allow for this forced refresh. If the current microprocessor cycle is a non-dynamic memory cycle ($\overline{CS}$ is high), this refresh is transparent to the microprocessor and $\overline{STRETCH}$ remains high (E and Q are not stretched). Nevertheless, if the current cycle is a dynamic memory access cycle, $\overline{STRETCH}$ goes low stretching E and Q for a maximum of four system clocks. $\overline{RASIN}$ for the pending access will be issued a full system clock after M2 has gone high; this is to allow some $\overline{RAS}$ precharge time for the dynamic RAM. After this, memory will be accessed in the manner as described in the Memory Access Cycle.

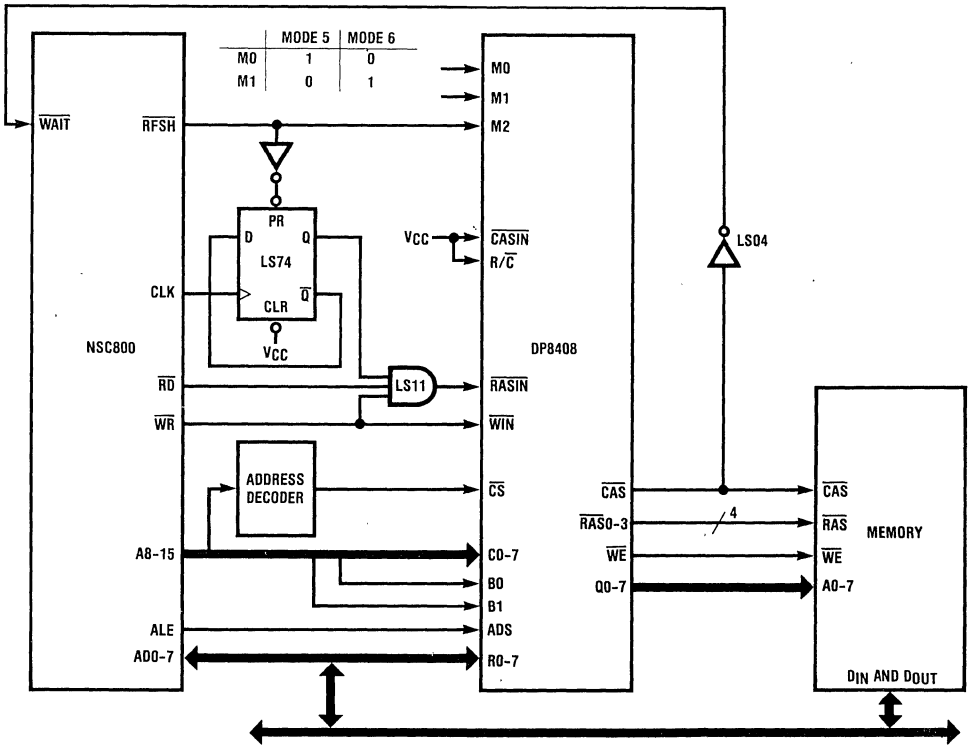


Figure 8. NSC800 and DP8408 Interface

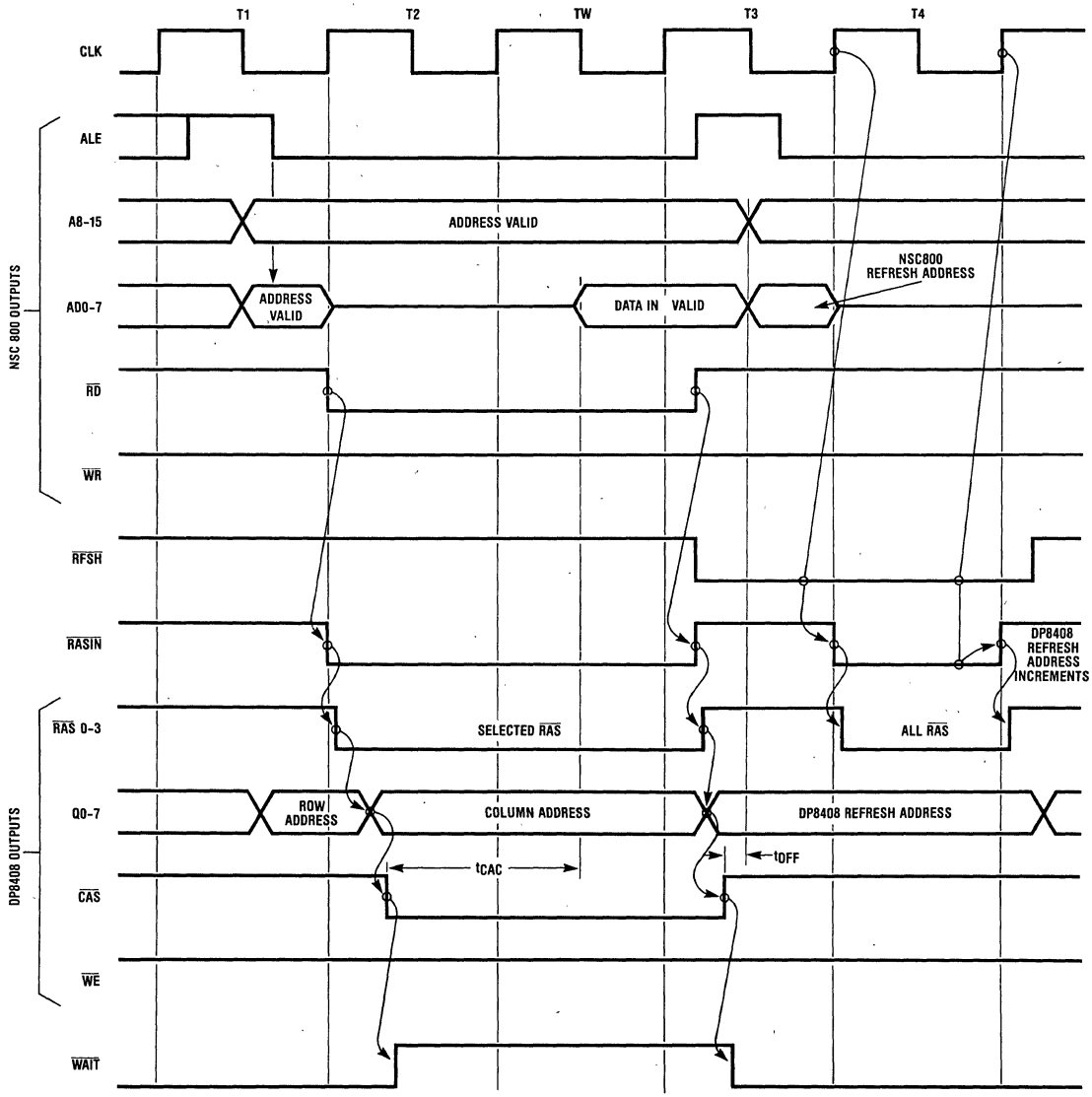


Figure 9. NSC800 Op Code Fetch Cycle Showing Memory Refresh

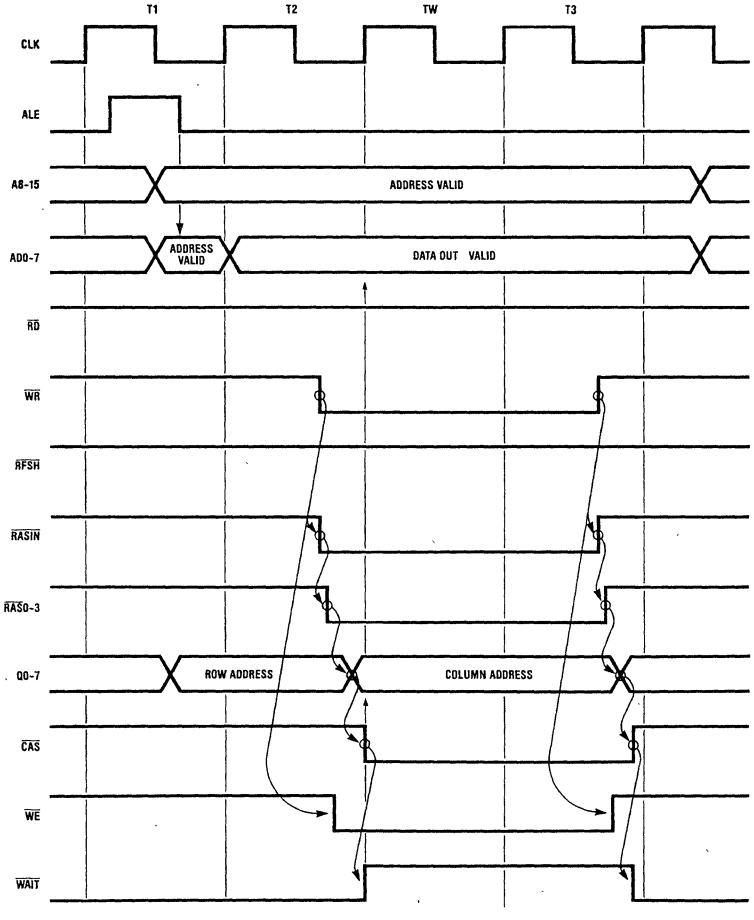


Figure 10. NSC800 Memory Write Cycle

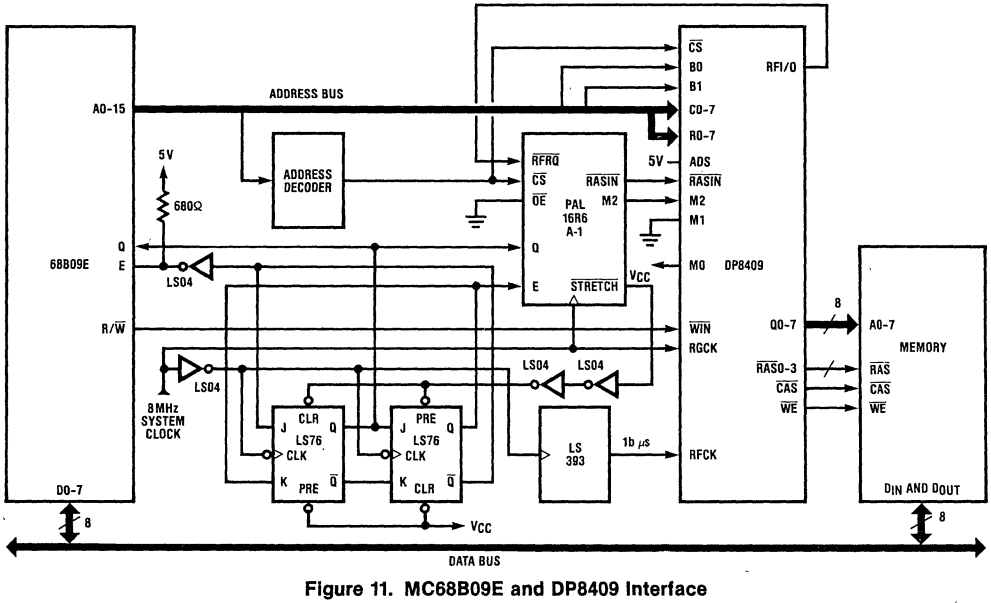
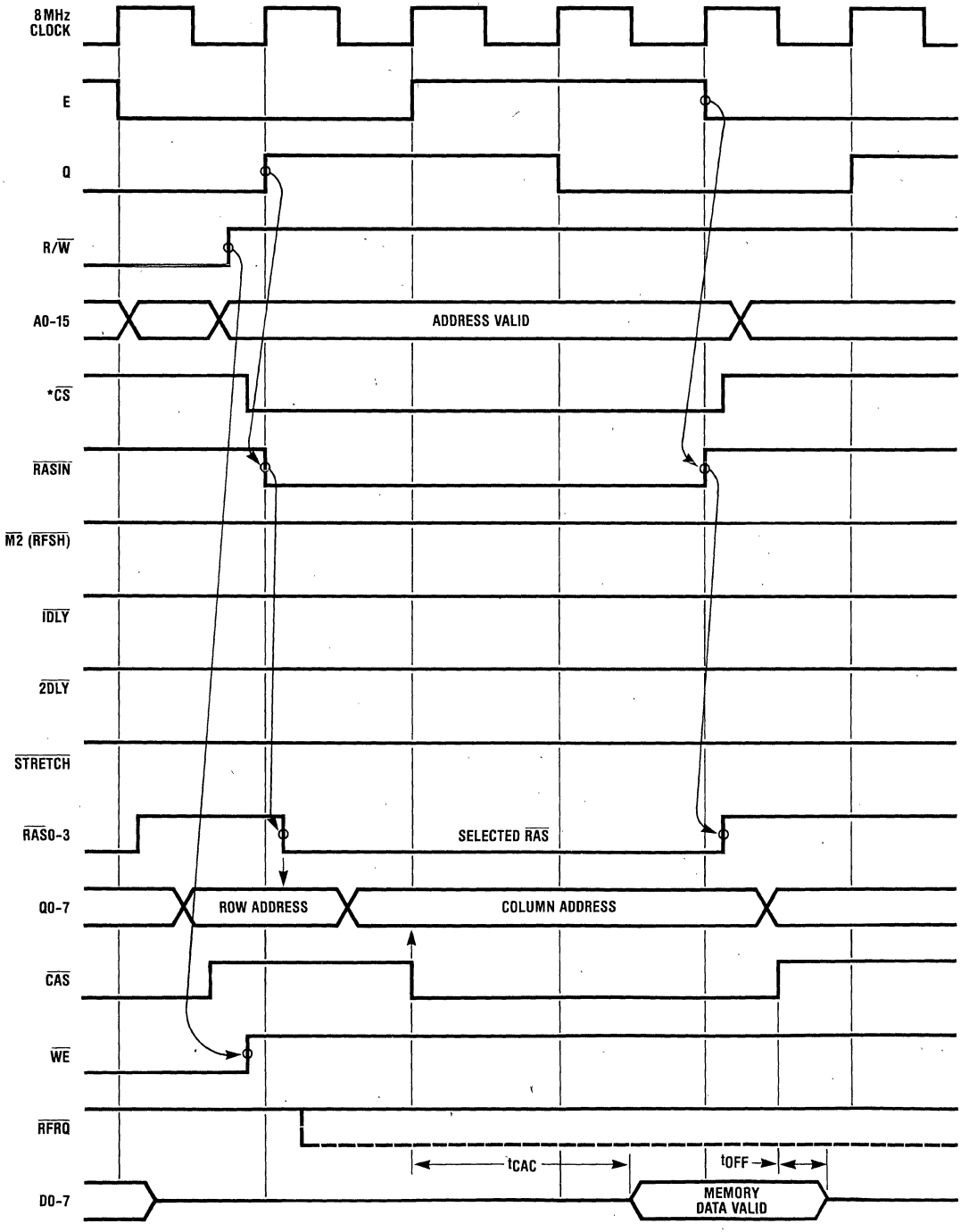


Figure 11. MC68B09E and DP8409 Interface



*IF CS IS HIGH THROUGHOUT THIS CYCLE (RFCK IS ALSO HIGH), HIDDEN REFRESH OCCURS INSTEAD OF A MEMORY ACCESS.

Figure 12. MC68B09E Memory Read Cycle

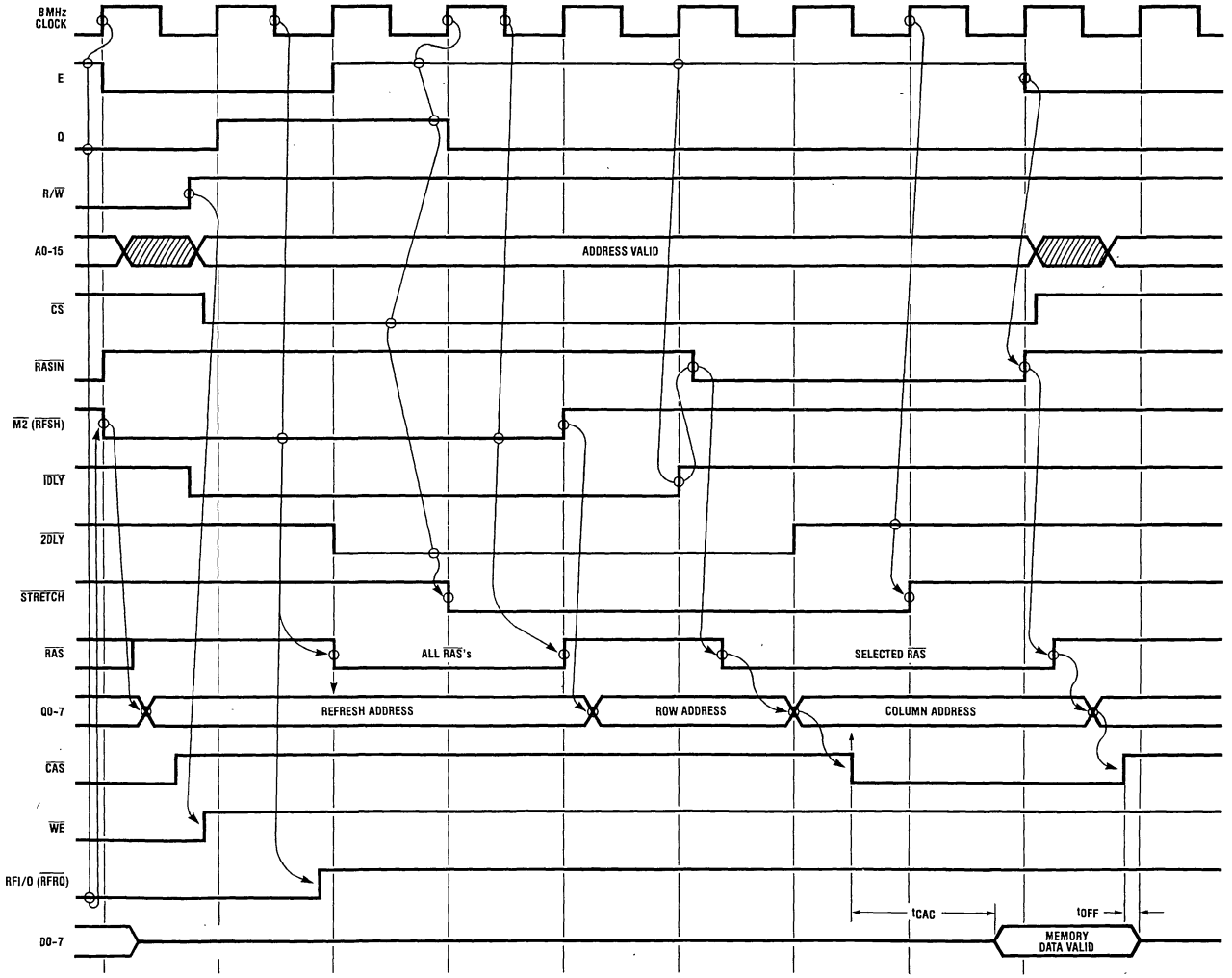


Figure 13. MC68B09E Forced Refresh and Memory Read Cycle

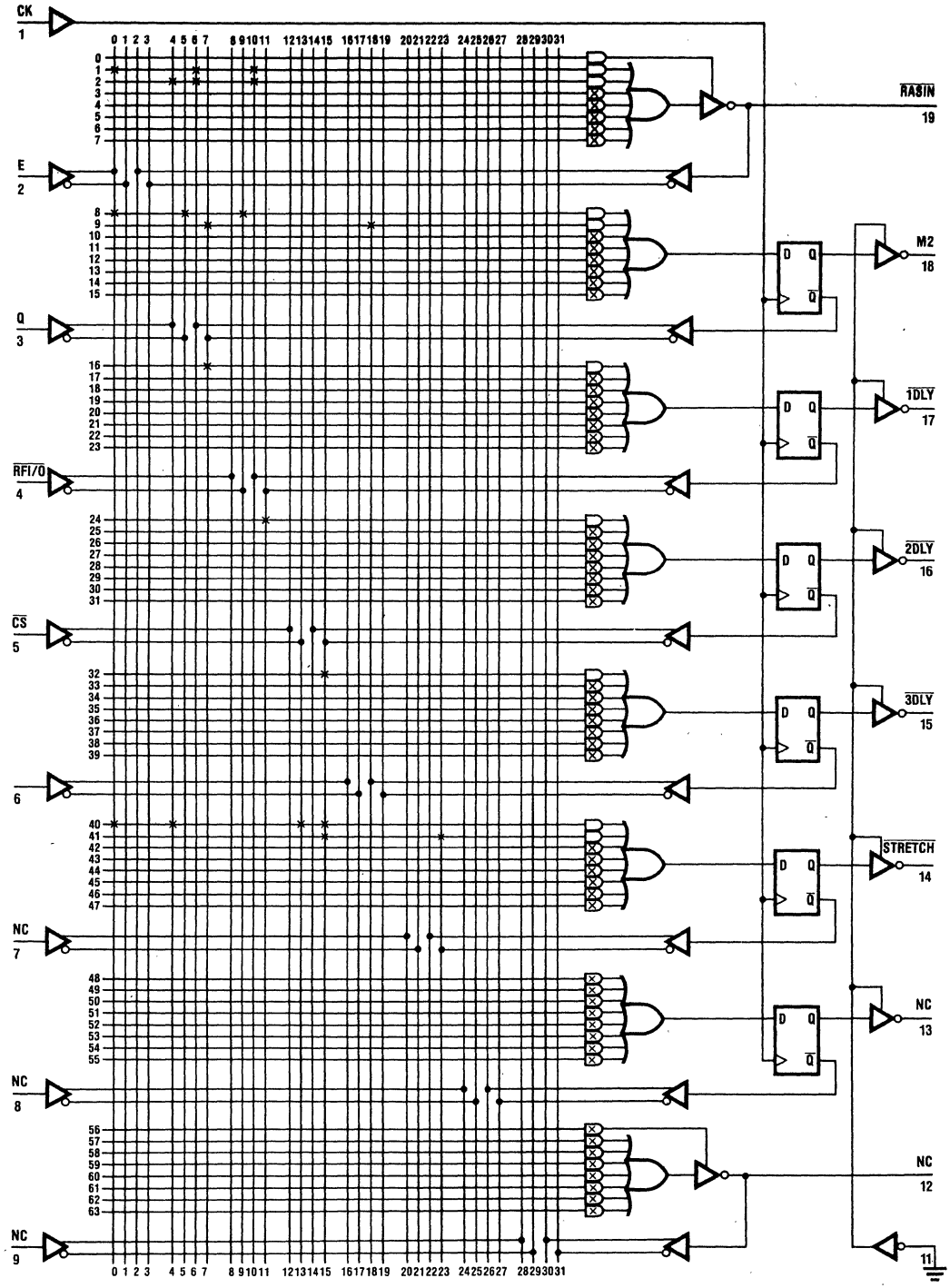


Figure 14. PAL (16R6 A-1) Control Logic

Memory Systems with ECC Using the DP8400

National Semiconductor
Application Brief #2
Brian Edem
June 1982

This brief explains how a memory system can easily perform single error correction, double error detection, auto accessing and refreshing of memory, and byte writing.

Figure 1 shows the NS16032 with DP8409, DP8400, and a 2-PAL® (Programmable Array Logic) controller. The memory cycle for the NS16032 starts at the CPU clock cycle where the address strobe goes active. At the middle of this clock cycle, the 74ALS02 latch is set, providing RASIN to the DP8409 Dynamic RAM Controller, which starts its Auto Access cycle. The latch output is also sent to the two PAL controllers, indicating that a memory cycle has started. On the next PAL clock cycle (50 ns later), the PAL will enter one of five memory cycles: Read, Byte-Write, Word-Write, or Cycle Inhibit.

For a read cycle, one wait state will be needed, so the controller pulls the NCWAIT line low for one CPU clock cycle. Three CPU clock cycles after RASIN, the corrected data is latched at the output of the DP8400, the memory buffers are disabled, and the DP8400's output buffers are enabled. At the beginning of the fifth CPU clock cycle, the CPU latches the data from the data bus, and the PAL deactivates all control signals, resets the 74ALS02 latch, and outputs an interrupt to the CPU if a double error is detected. This allows the CPU to gracefully crash or perform a memory test on the system.

In a byte-write cycle, the data must first be read from memory to be corrected if necessary. The new byte to be written, along with the byte that remains unchanged, will then be written to memory with the new checkbits.

The byte-write memory cycle needs two wait states, so the PAL controller first pulls the NCWAIT line low for two CPU clock cycles. Three CPU clock cycles after RASIN is activated, corrected data is latched at the output of the DP8400. Also at this time the memory buffers are disabled, the new byte from the CPU and the unaddressed memory byte from the DP8400 are enabled onto the internal data bus, creating a new word of data. A half of the CPU clock cycle after the new data is enabled, it is latched into the DP8400, the mode of which has been changed to generate check bits. A half of the CPU clock cycle after the data has been latched into the input of the DP8400, the data is again latched at the output to the DP8400 along with the newly generated check bits. Also at this time, a write strobe is generated by the PAL. At the end of the write strobe, the PAL outputs a reset pulse, resetting the 74ALS02 latch. If a double bit error occurred during the read portion of the memory cycle, then the interrupt will be triggered.

For a word-write cycle, no wait states are used. The buffer from the CPU is enabled, the DP8400 is put into a write mode, and the DP8409 is instructed to write memory. After CAS has occurred, the PAL controller resets the 74ALS02 latch.

During any memory cycle that the dynamic RAM is not selected, the controller effectively performs a cycle inhibit, allowing the DP8409 to perform a refresh if needed. One CPU clock cycle after the cycle starts, the 74ALS02 latch is cleared. The DP8409 will use this short RASIN strobe to generate an All-RAS strobe if a hidden refresh is pending.

If a hidden refresh has not occurred in the allocated time (period of RFCK high), a forced refresh will be requested. The PAL controller will wait for the end of the current memory cycle, and immediately request a cycle hold, and then switch the DP8409 to the auto refresh mode. While the NS16201 is in the cycle hold state, NTSO will stay high, preventing the start of another memory cycle. After sufficient time has been allowed for the DP8409 to perform a forced refresh, the PAL controller will remove the cycle hold.

Figure 2 shows how, using the 68000, DP8409 and DP8400, and a controller, the same functions can be performed with a memory system controlled by a 68000 microprocessor. Timing for the 68000 system is similar to that for the NS16000, except for forced refresh and the generation of RASIN. The 68000 does not have a feature equivalent to cycle hold, so DTACK (Data Acknowledge) must be delayed if a memory cycle is requested during a forced refresh.

PAL is a registered trademark of Monolithic Memories, Inc.

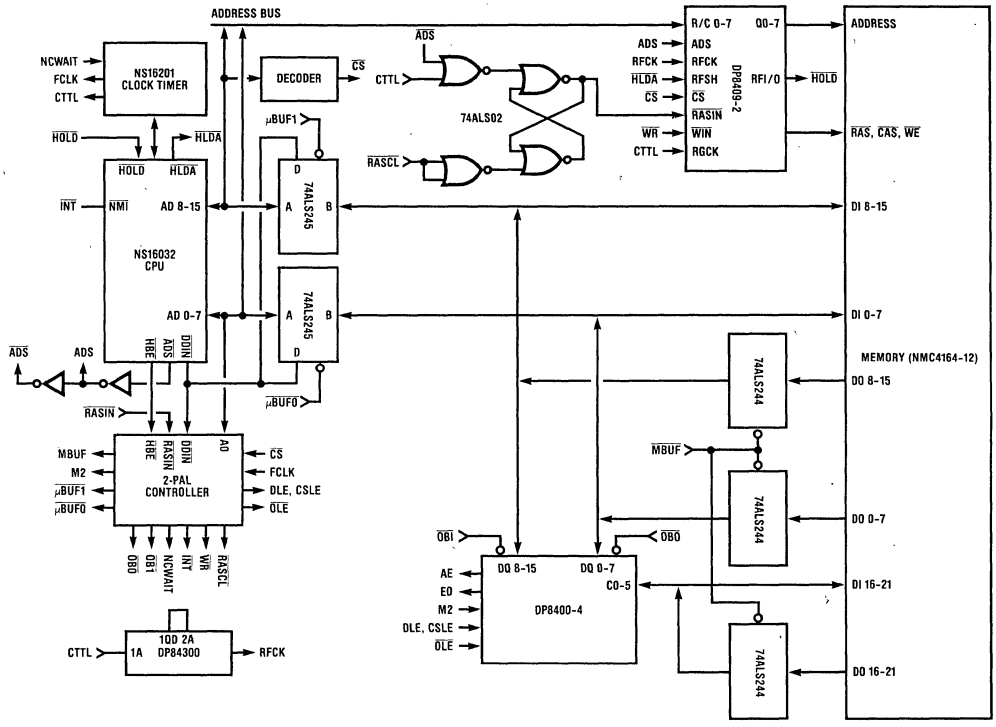


Figure 1. Memory System for NS16032 Using DP8409, DP8400, and 64k Dynamic RAMs, Performing Error Checking/Correcting, Refreshing and Byte-Writing

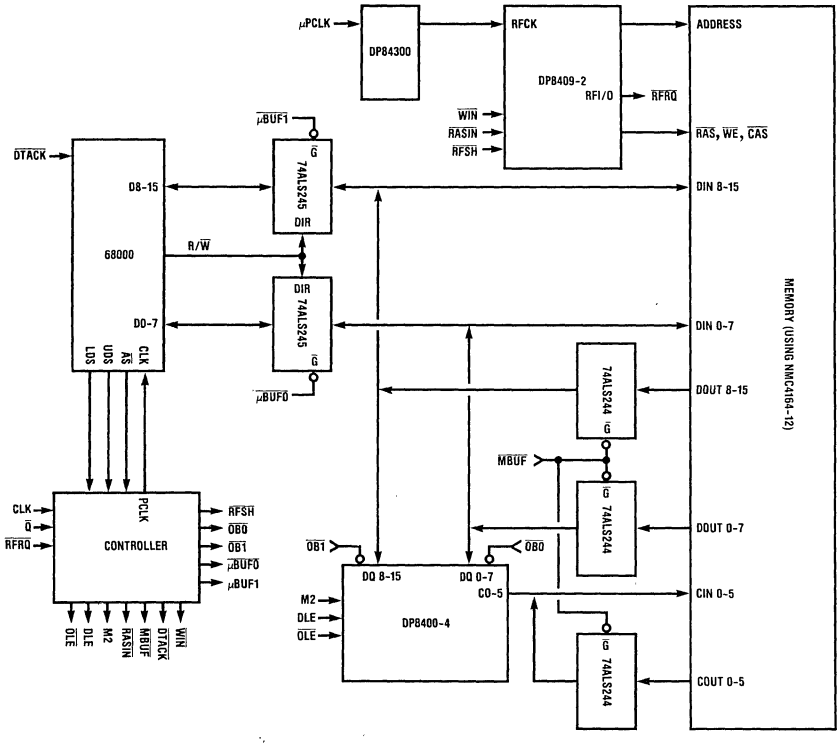


Figure 2. Memory System for the 68000 Using DP8409, DP8400 and 64k Dynamic RAMs

Section 8
Microprocessor Support

8

*Also available screened in accordance with MIL-STD-883 Class B. Refer to National Semiconductor's "The Reliability Handbook".

MICROPROCESSOR SUPPORT CIRCUITS

DESCRIPTION	GENERAL PURPOSE	8080 CPU	PART NUMBER		PAGE NO.
			0°C to +70°C	−55°C to +125°C	
8-Bit I/O Port	•	•	DP8212	DP8212M	8-4
4-Bit Parallel Receiver/Driver	•	•	DP8216, DP8226	DP8216M, DP8226M	8-11 8-11
Clock Generator/Driver		•	DP8224		8-16
System Controller/Bus Driver		•	DP8228, DP8238	DP8228M, DP8238M	8-22 8-22
8-Bit 48 mA Bus Transceiver	•		DP8303	DP7303	2-6
8-Bit 48 mA Bus Transceiver	•		DP8304B	DP7304B	2-11
8-Bit 48 mA Bus Transceiver	•		DP8307	DP7307	2-16
8-Bit 48 mA Bus Transceiver	•		DP8308	DP7308	2-20
CRT Controller	•	•	DP8350		5-6
CRT Controller	•	•	DP8352,		5-6
CRT Controller	•	•	DP8353		5-6
Octal D-Type Latch	•		MM74C373	MM54C373	CMOS
Octal D-Type Flip-Flop	•		MM74C374	MM54C374	CMOS
16-Key Encoder	•		MM74C922	MM54C922	CMOS
20-Key Encoder	•		MM54C923	MM54C923	CMOS
Octal Transparent D Latch	•		DM74LS373	DM54LS373	LOGIC
Octal Edge-Triggered D Flip-Flop	•		DM74LS374	DM54LS374	LOGIC

National Semiconductor

Microprocessor Support

DP8212/DP8212M 8-Bit Input/Output Port

General Description

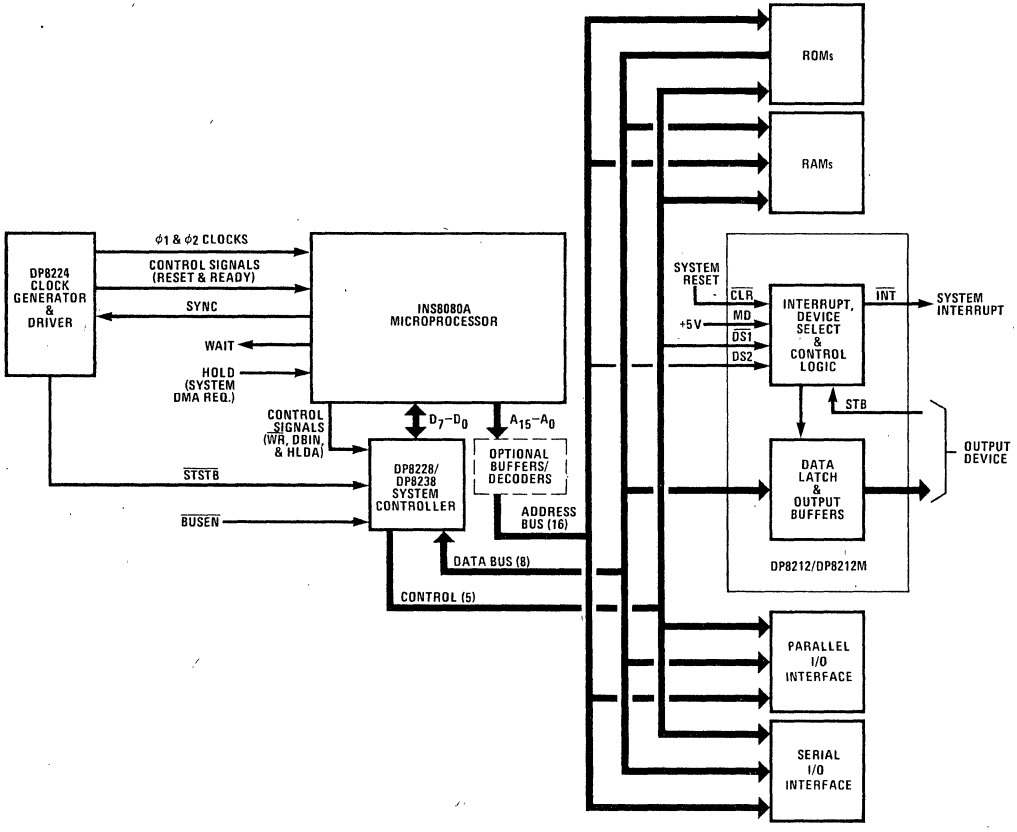
The DP8212/DP8212M is an 8-bit input/output port contained in a standard 24-pin dual-in-line package. The device, which is fabricated using Schottky Bipolar technology, is part of National Semiconductor's N8080A microcomputer family. The DP8212/DP8212M can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The DP8212/DP8212M includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

Features

- 8-Bit Data Latch and Buffer
- Service Request Flip-flop for Generation and Control of Interrupts
- 0.25mA Input Load Current
- TRI-STATE TTL Output Drive Capability
- Outputs Sink 15mA
- Asynchronous Latch Clear
- 3.65V Output for Direct Interface to INS8080A
- Reduces System Package Count by Replacing Buffers, Latches, and Multiplexers in Microcomputer Systems

N8080A Microcomputer Family Block Diagram



Absolute Maximum Ratings

Storage Temperature	−65°C to +160°C
All Output or Supply Voltages	−0.5V to +7V
All Input Voltages	−1.0V to 5.5V
Output Currents	125 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1903 mW
Molded Package	2005 mW

*Derate cavity package 12.7 mW/°C above 25°C; derate molded package 16.0 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DP8212M	4.50	5.50	V_{DC}
DP8212	4.75	5.25	V_{DC}
Operating Temperature (T_A)			
DP8212M	−55	+125	°C
DP8212	0	+75	°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

Electrical Characteristics ($Min \leq T_A \leq Max$, $Min \leq V_{CC} \leq Max$, unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_F	Input Load Current, STB, DS2, $\overline{CLR}$, DI_1–DI_8 Inputs	$V_F = 0.45V$				−0.25	mA
I_F	Input Load Current, MD Input	$V_F = 0.45V$				−0.75	mA
I_F	Input Load Current, $\overline{DS1}$ Input	$V_F = 0.45V$				−1.0	mA
I_R	Input Leakage Current STB, DS2, $\overline{CLR}$, DI_1–DI_8 Inputs	$V_R = V_{CC}$ Max				10	μA
I_R	Input Leakage Current, MD Input	$V_R = V_{CC}$ Max				30	μA
I_R	Input Leakage Current, $\overline{DS1}$ Input	$V_R = V_{CC}$ Max				40	μA
V_C	Input Forward Voltage Clamp	$I_C = -5$ mA				−1	V
V_{IL}	Input "Low" Voltage		DP8212M			0.80	V
			DP8212			0.85	V
V_{IH}	Input "High" Voltage			2.0			V
V_{OL}	Output "Low" Voltage	$I_{OL} = 10$ mA	DP8212M			0.45	V
		$I_{OL} = 15$ mA	DP8212			0.45	V
V_{OH}	Output "High" Voltage	$I_{OH} = -0.5$ mA	DP8212M	3.40	4.0		V
		$I_{OH} = -1.0$ mA	DP8212	3.65	4.0		V
I_{SC}	Short-Circuit Output Current	$V_O = 0V$, $V_{CC} = 5V$		−15		−75	mA
$\|I_O\|$	Output Leakage Current, High Impedance State	$V_O = 0.45V/V_{CC}$ Max				20	μA
I_{CC}	Power Supply Current		DP8212M		90	145	mA
			DP8212		90	130	mA

Capacitance *

$F = 1MHz$, $V_{BIAS} = 2.5V$, $V_{CC} = 5V$, $T_A = 25°C$.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
C_{IN}	DS1, MD Input Capacitance		9	12	pF
C_{IN}	DS2, $\overline{CLR}$, STB, DI_1–DI_8 Input Capacitance		5	9	pF
C_{OUT}	DO1–DO8 Output Capacitance		8	12	pF

*This parameter is sampled and not 100% tested.

Switching Characteristics

(Min $\leq T_A \leq$ Max, Min $\leq V_{CC} \leq$ Max)

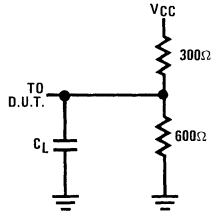
SYMBOL	PARAMETER	CONDITIONS	DP8212M		DP8212		UNITS
			MIN	MAX	MIN	MAX	
t_{PW}	Pulse Width		40		30		ns
t_{PD}	Data to Output Delay	(Note 5)		30		30	ns
t_{WE}	Write Enable to Output Delay	(Note 5)		50		40	ns
t_{SET}	Data Set-Up Time		20		15		ns
t_H	Data Hold Time		30		20		ns
t_R	Reset to Output Delay	(Note 5)		55		40	ns
t_S	Set to Output Delay	(Note 5)		35		30	ns
t_E	Output Enable/Disable Time	(Note 6)		50		45	ns
t_C	Clear to Output Delay	(Note 5)		65		55	ns

Switching Conditions

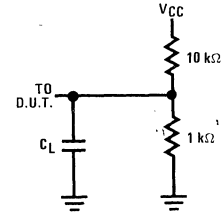
Conditions of Test:

1. Input Pulse Amplitude = 2.5V.
2. Input Rise and Fall Times = 5ns.
3. Between 1V and 2V Measurements made at 1.5V with 15mA & 30pF Test Load.
4. C_L includes jig and probe capacitance.
5. C_L = 30 pF.
6. C_L = 30 pF except for DP8212M $t_{E(DISABLE)}$ C_L = 5 pF

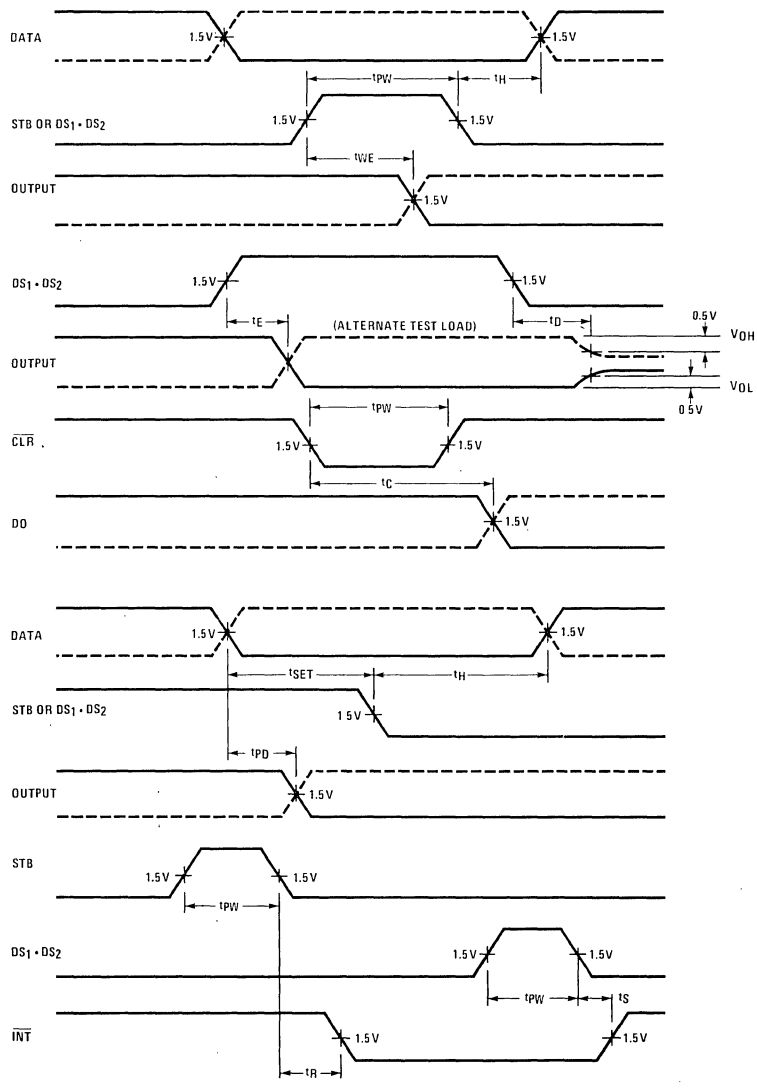
Test Load



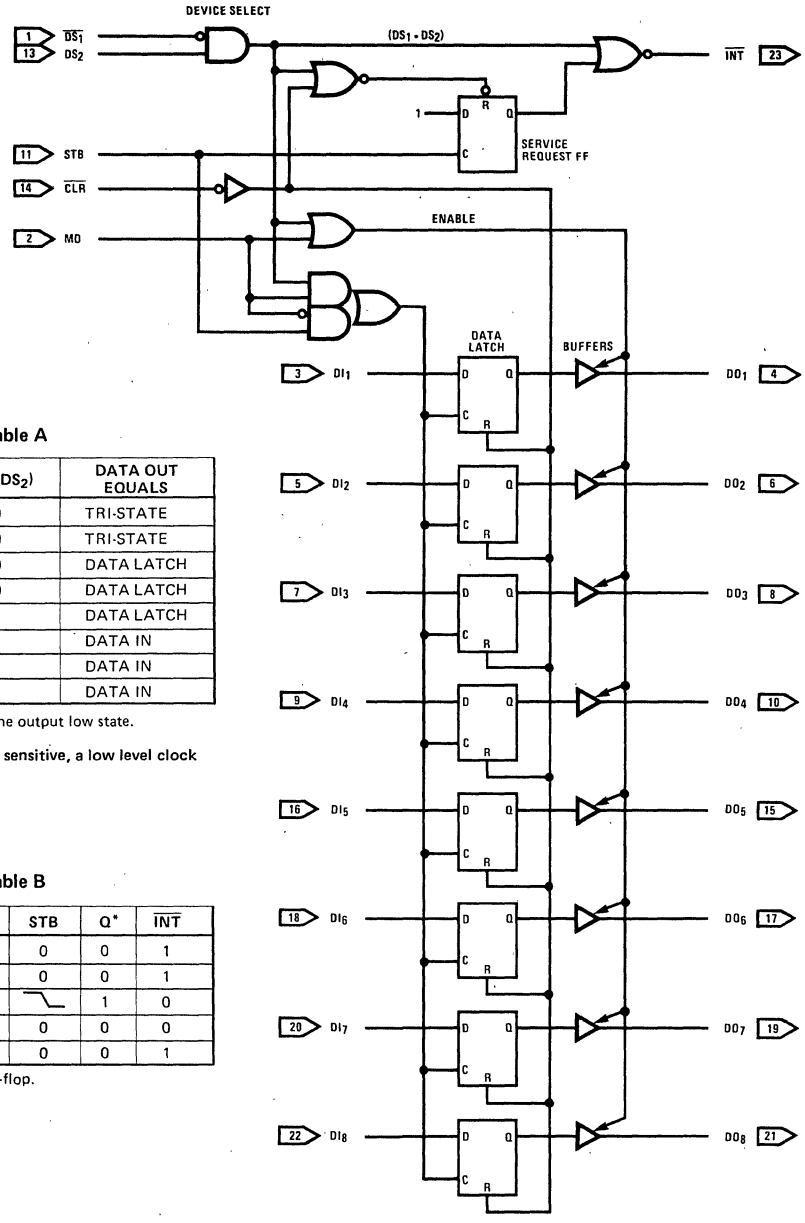
Alternate Test Load
(Refer to Timing Diagram)



Timing Diagram



Logic Diagram



Logic Table A

STB	MD	$(DS_1 \cdot DS_2)$	DATA OUT EQUALS
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

$\overline{CLR}$ ⌥ resets data latch to the output low state.

The data latch clock is level sensitive, a low level clock latches the data.

Logic Table B

$\overline{CLR}$	$(DS_1 \cdot DS_2)$	STB	Q*	$\overline{INT}$
0 RESET	0	0	0	1
1	0	0	0	1
1	0	⌥	1	0
1	1 RESET	0	0	0
1	0	0	0	1

*Internal Service Request flip-flop.

Functional Pin Definitions

The following describes the function of all the DP8212/DP8212M input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Device Select ($\overline{DS_1}$, DS_2): When $\overline{DS_1}$ is low and DS_2 is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously reset (cleared) when the device is selected.

Mode (MD): When high (output mode), the output buffers are enabled and the source of the data latch clock input is the device selection logic ($DS_1 \cdot DS_2$). When low (input mode), the state of the output buffers is determined by the device selection logic ($DS_1 \cdot DS_2$) and the source of the data latch clock input is the strobe (STB) input.

Functional Pin Definitions (Continued)

Strobe (STB): Used as data latch clock input when the mode (MD) input is low (input mode). Also used to synchronously set the service request flip-flop, which is negative edge triggered.

Data In (DI_1 – DI_8): Eight-bit data input to the data latch, which consists of eight D-type flip-flops. Incorporating a level sensitive clock while the data latch clock input is high, the Q output of each flip-flop follows the data input. When the clock input returns low, the data latch stores the data input. The clock input high overrides the clear ($\overline{CLR}$) input data latch reset.

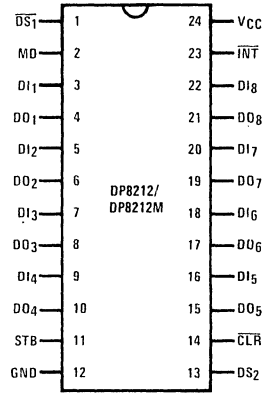
Clear ($\overline{CLR}$): When low, asynchronously resets (clears) the data latch and the service request flip-flop. The service request flip-flop is in the non-interrupting state when reset.

OUTPUT SIGNALS

Interrupt ($\overline{INT}$): Goes low (interrupting state) when either the service request flip-flop is synchronously set by the strobe (STB) input or the device is selected.

Data Out (DO_1 – DO_8): Eight-bit data output of data buffers, which are TRI-STATE, non-inverting stages. These buffers have a common control line that either enables the buffers to transmit the data from the data latch outputs or disables the buffers by placing them in the high-impedance state.

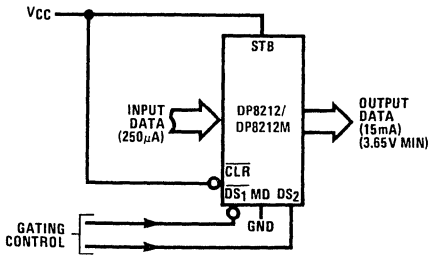
Connection Diagram

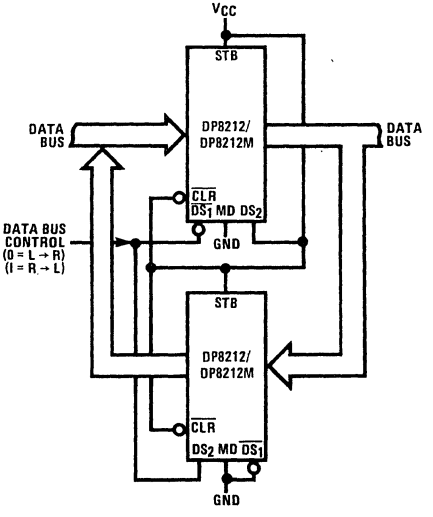


Order Number DP8212J, DP8212N or DP8212MJ
See NS Package J24A or N24A

Applications in Microcomputer Systems

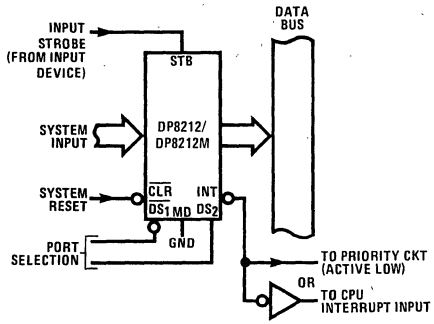
Gated Buffer
(TRI-STATE)



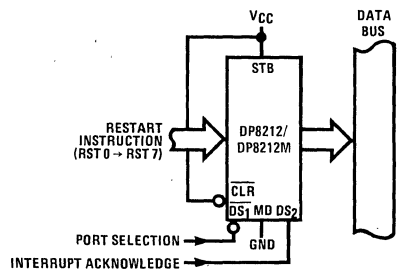


Applications in Microcomputer Systems (Continued)

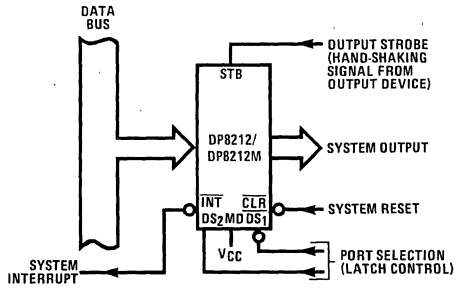
Interrupting Input Port



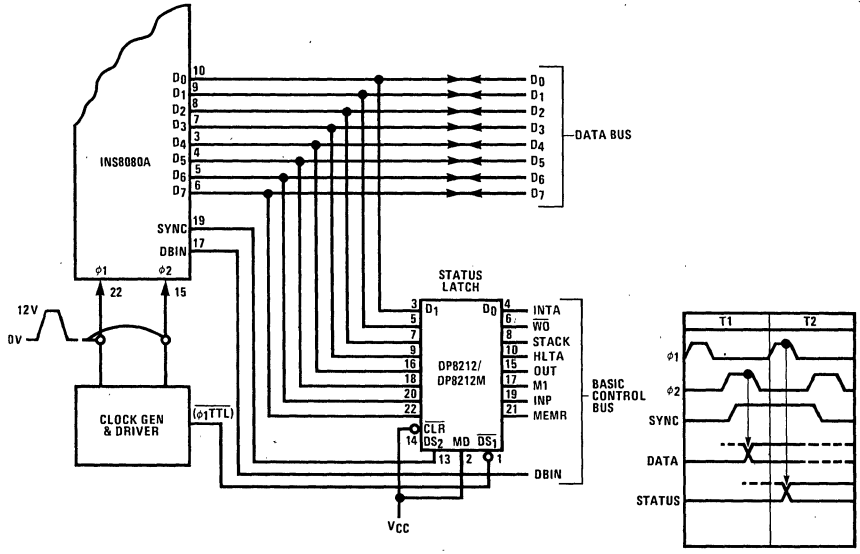
Interrupt Instruction Port



Output Port (with Hand-Shaking)



INS8080A Status Latch



DP8216/DP8216M, DP8226/DP8226M 4-Bit Bidirectional Bus Transceivers

General Description

The DP8216/DP8216M and DP8226/DP8226M are 4-bit bidirectional bus drivers for use in bus oriented applications. The non-inverting DP8216/DP8216M and inverting DP8226/DP8226M drivers are provided for flexibility in system design.

Each buffered line of the four-bit driver consists of two separate buffers that are TRI-STATE® to achieve direct bus interface and bidirectional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB); this side is used to interface to the system side components such as memories, I/O, etc., because its interface is TTL compatible and it has high drive (50 mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bidirectional bus. The DO outputs on this side of the driver have a special high voltage output drive capability so that direct interface to the 8080 type CPUs is achieved with an adequate amount of noise immunity.

The $\overline{CS}$ input is a device enable. When it is "high" the output drivers are all forced to their high-impedance state. When it is a "low" the device is enabled and the direction of the data flow is determined by the DIEN input.

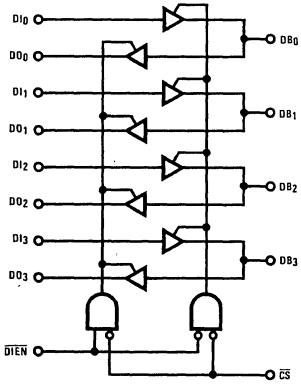
The DIEN input controls the direction of data flow, which is accomplished by forcing one of the pair of buffers into its high-impedance state and allowing the other to transmit its data. A simple two-gate circuit is used for this function.

Features

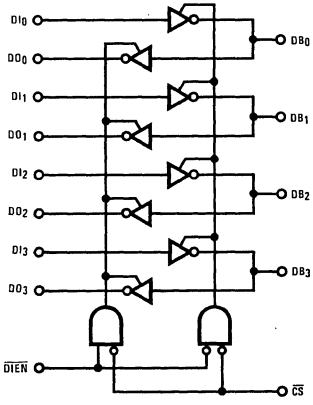
- Data bus buffer driver for 8080 type CPUs
- Low input load current – 0.25 mA maximum
- High output drive capability for driving system data bus – 50 mA at 0.5 V
- Power up-down protection
- DP8216/DP8216M have non-inverting outputs
- DP8226/DP8226M have inverting outputs
- Output high voltage compatible with direct interface to MOS
- TRI-STATE outputs
- Advanced Schottky processing
- Available in military and commercial temperature ranges

Logic and Connection Diagrams

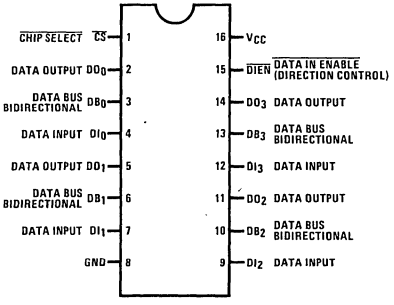
DP8216/DP8216M



DP8226/PD8226M



Dual-In-Line Package



Order Number DP8216J, DP8216N, DP8226J, DP8226N, DP8216MJ or DP8226MJ
See NS Package J16A or N16A

Absolute Maximum Ratings (Note 1)

	Min	Max	Units
All Output and Supply Voltages	−0.5	+7.0	V
All Input Voltages	−1.0	+5.5	V
Output Currents		125	mA
Storage Temperature	−65	+150	°C
Maximum Power Dissipation* at 25°C			
Cavity Package		1509	mW
Molded Package		1476	mW
Lead Temperature (soldering, 10 seconds)		+300	°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DP8216M, DP8226M	4.5	5.5	V
DP8216, DP8226	4.75	5.25	V
Temperature, T_A			
DP8216M, DP8226M	−55	+125	°C
DP8216, DP8226	0	+70	°C

Electrical Characteristics DP8216, DP8226 V_{CC} = 5 V ± 5% (Notes 2, 3, and 4)

Parameter		Conditions	Limits			Units
Symbol	Description		Min	Typ	Max	
DRIVERS						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		−0.03	−0.25	mA
I_R	Input Leakage Current	V_R = 5.25 V			10	μA
V_C	Input Clamp Voltage	I_C = −5 mA			−1.2	V
$V_{OL}1$	Output Low Voltage	I_{OL} = 25 mA		0.3	0.45	V
$V_{OL}2$	Output Low Voltage	DP8216 I_{OL} = 55 mA DP8226 I_{OL} = 50 mA		0.5	0.6	V
V_{OH}	Output High Voltage	I_{OH} = −10 mA	2.4	3.0		V
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0 V	−30	−75	−120	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45 V/5.5 V			100	μA
RECEIVERS						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		−0.08	−0.25	mA
V_C	Input Clamp Voltage	I_C = −5 mA			−1.2	V
V_{OL}	Output Low Voltage	I_{OL} = 15 mA		0.3	0.45	V
$V_{OH}1$	Output High Voltage	I_{OH} = −1 mA	3.65	4.0		V
I_{SC}	Output Short Circuit Current	$V_O \approx 0$ V	−15	−35	−65	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45 V/5.5 V			20	μA
CONTROL INPUTS ($\overline{CS}$, $\overline{DIEN}$)						
V_{IL}	Input Low Voltage				0.95	V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		−0.15	−0.5	mA
I_R	Input Leakage Current	V_R = 5.25 V			20	μA
I_{CC}	Power Supply Current DP8216 DP8226			 95 85	 130 120	 mA mA

Electrical Characteristics DP8216M, DP8226M V_{CC} = 5V ±10% (Notes 2, 3 and 4)

Parameter		Conditions	Limits			Units
Symbol	Description		Min	Typ	Max	
DRIVERS						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.90	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		-0.08	-0.25	mA
I_R	Input Leakage Current	V_R = 5.5 V			40	μA
V_C	Input Clamp Voltage	I_C = -5 mA			-1.2	V
V_{OL1}	Output Low Voltage	I_{OL} = 25 mA		0.3	0.45	V
V_{OL2}	Output Low Voltage	I_{OL} = 45 mA		0.5	0.6	V
V_{OH}	Output High Voltage	I_{OH} = -5 mA	2.4	3.0		V
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0 V	-30	-75	-120	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45 V/5.5 V			100	μA
RECEIVERS						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.9	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		-0.08	-0.25	mA
V_C	Input Clamp Voltage	I_C = -5 mA			-1.2	V
V_{OL}	Output Low Voltage	I_{OL} = 15 mA		0.3	0.45	V
V_{OH1}	Output High Voltage	I_{OH} = -0.5 mA	3.4	3.8		V
V_{OH2}	Output High Voltage	I_{OH} = -2 mA	2.4			V
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0 V	-15	-35	-65	mA
$\|I_O\|$	Output Leakage Current TRI-STATE	V_O = 0.45 V/5.5 V			20	μA
CONTROL INPUTS ($\overline{CS}$, $\overline{DIEN}$)						
V_{IL}	Input Low Voltage DP8216M DP8226M				 0.95 0.9	 V V
V_{IH}	Input High Voltage		2			V
I_F	Input Load Current	V_F = 0.45 V		-0.15	-0.5	mA
I_R	Input Leakage Current	V_R = 5.5 V			80	μA
I_{CC}	Power Supply Current DP8216M DP8226M			 95 85	 130 120	 mA mA

Switching Characteristics (Notes 2, 3, and 4)

Parameter		Conditions	Limits			Units
Symbol	Description		Min	Typ	Max	
DP8216M, DP8226M, V_{CC} = 5V ±10%						
t_{PD1}	Input to Output Delay, DO Outputs	C_L = 30 pF, R_1 = 300 Ω, R_2 = 600 Ω		15	25	ns
t_{PD2}	Input to Output Delay, DB Outputs	C_L = 300 pF, R_1 = 90 Ω, R_2 = 180 Ω				
	DP8216M			19	33	ns
	DP8226M			16	25	ns
t_E	Output Enable Time	DO Outputs: C_L = 30 pF, R_1 = 300 Ω/10 kΩ, R_2 = 600 Ω/1 kΩ DB Outputs: C_L = 300 pF, R_1 = 90 Ω/10 kΩ, R_2 = 180 Ω/1 kΩ				
	DP8216M			42	75	ns
	DP8226M			36	62	ns
t_D	Output Disable Time	DO Outputs: C_L = 5 pF, R_1 = 300 Ω/10 kΩ, R_2 = 600 Ω/1 kΩ DB Outputs: C_L = 5 pF, R_1 = 90 Ω/10 kΩ, R_2 = 180 Ω/1 kΩ				
	DP8216M			16	40	ns
	DP8226M			16	38	ns
DP8216, DP8226 V_{CC} = 5.0 V ± 5%						
t_{PD1}	Input to Output Delay, DO Outputs	C_L = 30 pF, R_1 = 300 Ω, R_2 = 600 Ω		15	25	ns
t_{PD2}	Input to Output Delay, DB Outputs	C_L = 300 pF, R_1 = 90 Ω, R_2 = 180 Ω				
	DP8216			20	30	ns
	DP8226			16	25	ns
t_E	Output Enable Time	DO Outputs: C_L = 30 pF, R_1 = 300 Ω/10 kΩ, R_2 = 600 Ω/1 kΩ DB Outputs: C_L = 300 pF, R_1 = 90 Ω/10 kΩ, R_2 = 180 Ω/1 kΩ				
	DP8216			45	65	ns
	DP8226			35	54	ns
t_D	Output Disable Time	DO Outputs: C_L = 5 pF, R_1 = 300 Ω/10 kΩ, R_2 = 600 Ω/1 kΩ DB Outputs: C_L = 5 pF, R_1 = 90 Ω/10 kΩ, R_2 = 180 Ω/1 kΩ		20	35	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DP8216M and DP8226M and across the 0°C to +70°C temperature range for the DP8216 and DP8226. All typical values are given for V_{CC} = 5 V and T_A = 25°C.

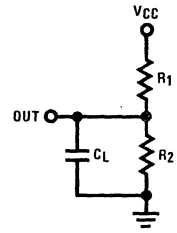
Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 4: Only one output at a time should be shorted.

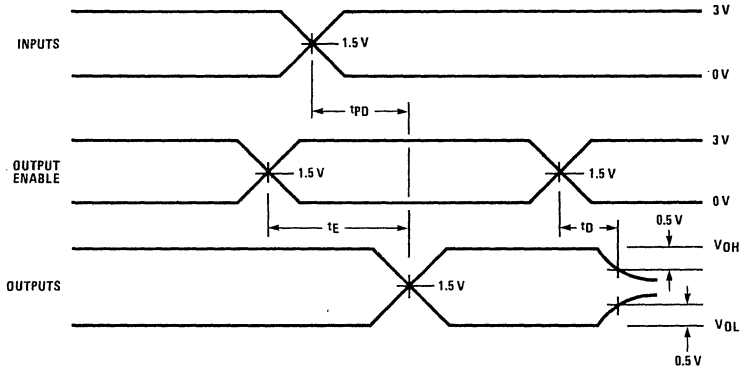
Test Conditions

Input pulse amplitude of 2.5 V.
Input rise and fall times of 5.0 ns between 1.0 V and 2.0 V.
Output loading is 5.0 mA and 10 pF.
Speed measurements are made at 1.5 V levels.

Test Load Circuit



Switching Time Waveforms



Capacitance $T_A = 25°C$

Symbol	Parameter	Limit Min.	Limit Typ.	Limit Max.	Unit
C_{IN}	Input Capacitance		4	6	pF
C_{OUT}	Output Capacitance				
	DO Outputs		6	10	pF
	DB Outputs		13	18	pF

Note: This parameter is periodically sampled and is not 100% tested. Condition of measurement is f = 1 MHz, V_{BIAS} = 2.5 V, V_{CC} = 5.0 V, and T_A = 25°C.

National Semiconductor

DP8224 Clock Generator and Driver

General Description

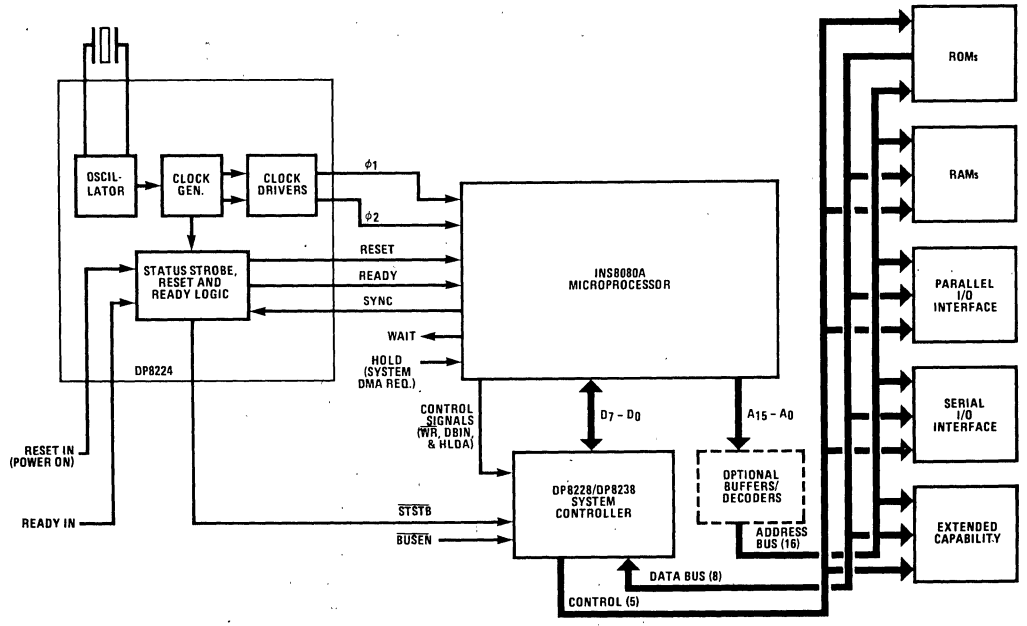
The DP8224 is a clock generator/driver contained in a standard, 16-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates clocks and timing for National Semiconductor's N8080A microcomputer family.

Included in the DP8224 is an oscillator circuit that is controlled by an external crystal, which is selected by the designer to meet a variety of system speed requirements. Also included in the chip are circuits that provide: a status strobe for the DP8228 or DP8238 system controllers, power-on reset for the INS8080A microprocessor, and synchronization of the READY input to the INS8080A.

Features

- Crystal-Controlled Oscillator for Stable System Operation
- Single Chip Clock Generator and Driver for INS8080A Microprocessor
- Provides Status Strobe for DP8228 or DP8238 System Controllers
- Provides Power-On Reset for INS8080A Microprocessor
- Synchronizes READY Input to INS8080A Microprocessor
- Provides Oscillator Output for Synchronization of External Circuits
- Reduces System Component Count

N8080A Microcomputer Family Block Diagram



Absolute Maximum Ratings (Note 2)

Supply Voltage	
V_{CC}	7V
V_{DD}	15V
Input Voltage	−1V to +5.5V
Storage Temperature Range	−65°C to +150°C
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.8 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{CC}	4.75	5.25	V
V_{DD}	11.4	12.6	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Note 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_F	Input Current Loading	V_F = 0.45V			−0.25	mA
I_R	Input Leakage Current	V_R = 5.25V			10	μA
V_C	Input Forward Clamp Voltage	I_C = −5 mA			−1.0	V
V_{IL}	Input "Low" Voltage	V_{CC} = 5V			0.8	V
V_{IH}	Input "High" Voltage	$\overline{RESIN}$ Input	2.6			V
		All Other Inputs	2.0			V
$V_{IH}-V_{IL}$	$\overline{RESIN}$ Input Hysteresis	V_{CC} = 5V	0.25			V
V_{OL}	Output "Low" Voltage					
	(ϕ1, ϕ2), Ready, Reset, $\overline{STSTB}$	I_{OL} = 2.5 mA			0.45	V
	Osc., ϕ2 (TTL)	I_{OL} = 10 mA			0.45	V
	Osc., ϕ2 (TTL)	I_{OL} = 15 mA			0.45	V
V_{OH}	Output "High" Voltage					
	ϕ1, ϕ2	I_{OH} = −100 μA	9.4			V
	Ready, Reset	I_{OH} = −100 μA	3.6			V
	Osc., ϕ2 (TTL), $\overline{STSTB}$	I_{OH} = −1 mA	2.4			V
I_{SC}	Output Short-Circuit Current (All Low Voltage Outputs Only), (Note 1)	V_O = 0V, V_{CC} = 5V	−10		−60	mA
I_{CC}	Power Supply Current				115	mA
I_{DD}	Power Supply Current				12	mA

Note 1: Caution — ϕ1 and ϕ2 output drivers do not have short circuit protection.

Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 3: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DP8224. All typical values are for T_A = 25°C, V_{CC} = 5V, and V_{DD} = 12V.

Crystal Requirements*

Tolerance	0.005% at 0°C to +70°C	Equivalent Resistance	75Ω to 20Ω
Resonance	Fundamental**	Power Dissipation (Min)	4 mW
Load Capacitance	20 pF to 30 pF		

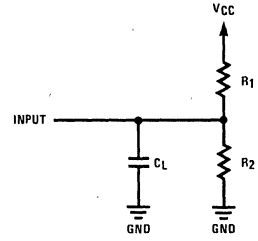
*It is good design practice to ground the case of the crystal

**With tank circuit, use 3rd overtone mode

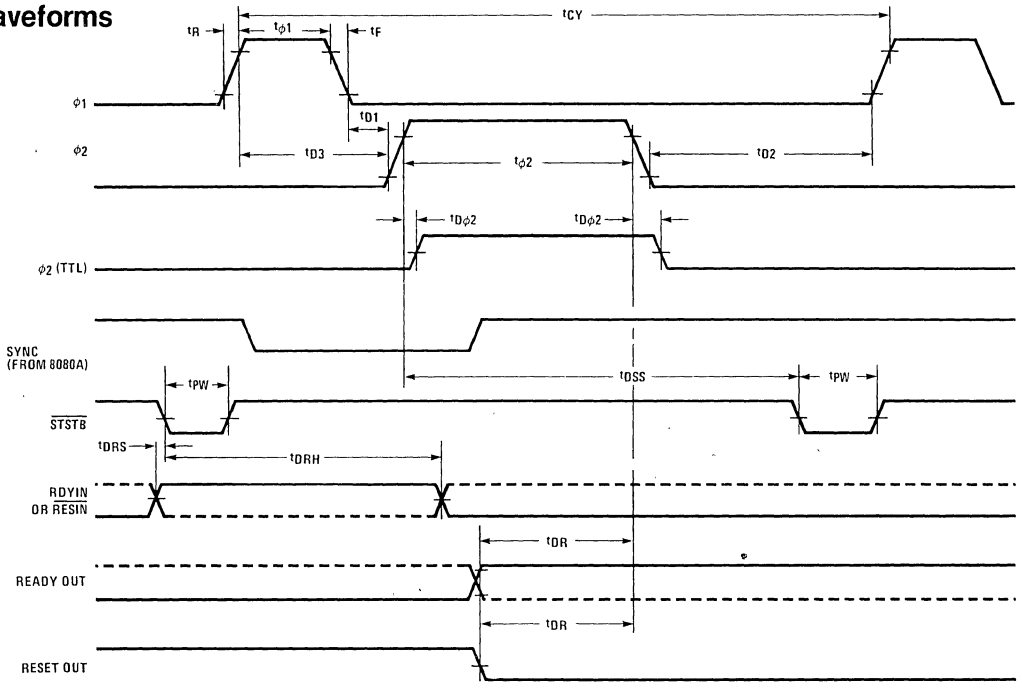
Switching Characteristics (Note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\phi 1}$	$\phi 1$ Pulse Width	C_L = 20 pF to 50 pF	$\frac{2t_{CY}}{9} - 20$			ns
$t_{\phi 2}$	$\phi 2$ Pulse Width		$\frac{5t_{CY}}{9} - 35$			ns
t_{D1}	$\phi 1$ to $\phi 2$ Delay		0			ns
t_{D2}	$\phi 2$ to $\phi 1$ Delay		$\frac{2t_{CY}}{9} - 14$			ns
t_{D3}	$\phi 1$ to $\phi 2$ Delay		$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9} + 20$	ns
t_r	$\phi 1$ and $\phi 2$ Rise Time				20	ns
t_f	$\phi 1$ and $\phi 2$ Fall Time				20	ns
$t_{D\phi 2}$	$\phi 2$ to $\phi 2$ (TTL) Delay	$\phi 2$ TTL, C_L = 30 pF, R1 = 300Ω, R2 = 600Ω	−5		15	ns
t_{DSS}	$\phi 2$ to $\overline{STSTB}$ Delay	$\overline{STSTB}$, C_L = 15 pF R1 = 2 kΩ, R2 = 4 kΩ	$\frac{6t_{CY}}{9} - 30$		$\frac{6t_{CY}}{9}$	ns
t_{PW}	$\overline{STSTB}$ Pulse Width		$\frac{t_{CY}}{9} - 15$			ns
t_{DRS}	RDYIN Set-Up Time to Status Strobe		$50 - \frac{4t_{CY}}{9}$			ns
t_{DRH}	RDYIN Hold Time After $\overline{STSTB}$		$\frac{4t_{CY}}{9}$			ns
t_{DR}	READY or RESET to $\phi 2$ Delay	Ready and Reset, C_L = 10 pF, R1 = 2 kΩ, R2 = 4 kΩ	$\frac{4t_{CY}}{9} - 25$			ns
t_{CLK}	CLK Period			$\frac{t_{CY}}{9}$		ns
f_{MAX}	Maximum Oscillating Frequency		27			MHz
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{DD} = 12V, V_{BIAS} = 2.5V, f = 1 MHz			8	pF

Test Circuit



Waveforms



VOLTAGE MEASUREMENT POINTS: $\phi 1$, $\phi 2$ Logic "0" = 1.0V, Logic "1" = 8.0V. All other signals measured at 1.5V.

Switching Characteristics (For t_{CY} = 488.28 ns)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\phi 1}$	$\phi 1$ Pulse Width	$\phi 1$ and $\phi 2$ Loaded to C_L = 20 to 50 pF Ready & Reset Loaded to 2 mA/10 pF All Measurements Referenced to 1.5V unless Specified Otherwise	89			ns
$t_{\phi 2}$	$\phi 2$ Pulse Width		236			ns
t_{D1}	Delay $\phi 1$ to $\phi 2$		0			ns
t_{D2}	Delay $\phi 2$ to $\phi 1$		95			ns
t_{D3}	Delay $\phi 1$ to $\phi 2$ Leading Edges		109		129	ns
t_r	Output Rise Time				20	ns
t_f	Output Fall Time				20	ns
t_{DSS}	$\phi 2$ to $\overline{STSTB}$ Delay		296		326	ns
$t_{D\phi 2}$	$\phi 2$ to $\phi 2$ (TTL) Delay		−5		15	ns
t_{PW}	Status Strobe Pulse Width		40			ns
t_{DRS}	RDYIN Set-Up Time to $\overline{STSTB}$		−167			ns
t_{DRH}	RDYIN Hold Time after $\overline{STSTB}$		217			ns
t_{DR}	READY or RESET to $\phi 2$ Delay		192			ns
f_{MAX}	Oscillator Frequency				18.432	MHz

Functional Pin Definitions

The following describes the function of all of the DP8224 input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Crystal Connections (XTAL 1 and XTAL 2): Two inputs that connect an external crystal to the oscillator circuit of the DP8224. Normally, a fundamental mode crystal is used to determine the basic operating frequency of the oscillator. However, overtone mode crystals may also be used. The crystal frequency is 9 times the desired microprocessor speed (that is, crystal frequency equals $1/t_{CY} \times 9$). When the crystal frequency is above 10 MHz, a selected capacitor (3 to 10 pF) may have to be connected in series with the crystal to produce the exact desired frequency. *Figure A.*

Tank: Allows the use of overtone mode crystals with the oscillator circuit. When an overtone mode crystal is used, the tank input connects to a parallel LC network that is ac coupled to ground. The formula for determining the resonant frequency of this LC network is as follows:

$$F = \frac{1}{2\pi\sqrt{LC}}$$

Synchronizing (SYNC) Signal: When high, indicates the beginning of a new machine cycle. The INS8080A microprocessor outputs a status word (which describes the current machine cycle) onto its data bus during the first state (SYNC interval) of each machine cycle.

Reset In ($\overline{\text{RESIN}}$): Provides an automatic system reset and start-up upon application of power as follows. The $\overline{\text{RESIN}}$ input, which is obtained from the junction of an external RC network that is connected between V_{CC} and ground, is routed to an internal Schmitt Trigger circuit. This circuit converts the slow transition of the power supply rise into a sharp, clean edge when its input reaches a predetermined value. When this occurs, an internal D-type flip-flop is synchronously reset, thereby providing the RESET output signal discussed below.

For manual system reset, a momentary contact switch that provides a low (ground) when closed is also connected to the $\overline{\text{RESIN}}$ input.

Ready In (RDYIN): An asynchronous READY signal that is re-clocked by a D-type flip-flop of the DP8224 to provide the synchronous READY output discussed below.

+5 Volts: V_{CC} supply.

+12 Volts: V_{DD} supply.

Ground: 0 volt reference.

OUTPUT SIGNALS

Oscillator (OSC): A buffered oscillator signal that can be used for external timing purposes.

ϕ_1 and ϕ_2 Clocks: Two non-TTL compatible clock phases that provide nonoverlapping timing references for internal storage elements and logic circuits of the INS8080A microprocessor. The two clock phases are produced by an internal clock generator that consists of a divide-by-nine counter and the associated decode gating logic. Figure B.

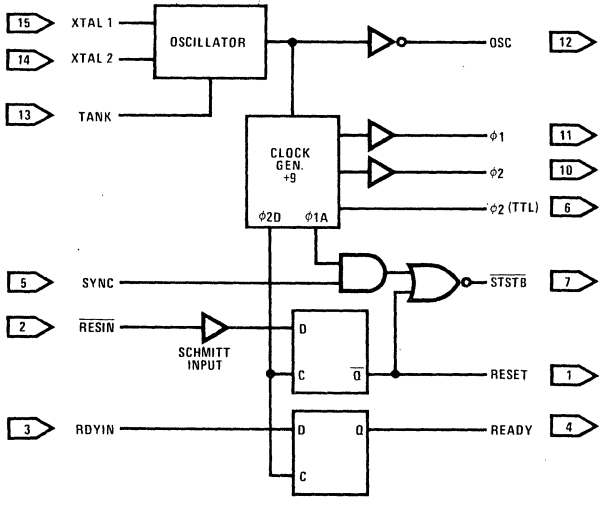
ϕ_2 (TTL) Clock: A TTL ϕ_2 clock phase that can be used for external timing purposes.

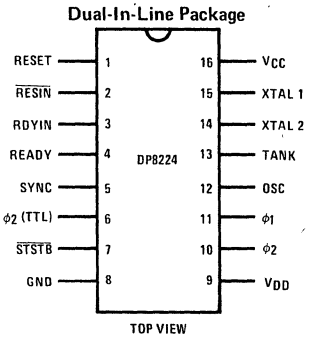
Status Strobe ($\overline{\text{STSTB}}$): Activated (low) at the start of each new machine cycle. The $\overline{\text{STSTB}}$ signal is generated by gating a high-level SYNC input with the ϕ_{1A} timing signal from the internal clock generator of the DP8224. The $\overline{\text{STSTB}}$ signal is used to clock status information into the status latch of the DP8228 system controller and bus driver.

Reset: When the RESET signal is activated, the content of the program counter of the INS8080A is cleared. After RESET, the program will start at location 0 in memory.

Ready: The READY signal indicates to the INS8080A that valid memory or input data is available. This signal is used to synchronize the INS8080A with slower memory or input/output devices.

Logic and Connection Diagrams





Order Number DP8224J or DP8224N
See NS Package J16A or N16A

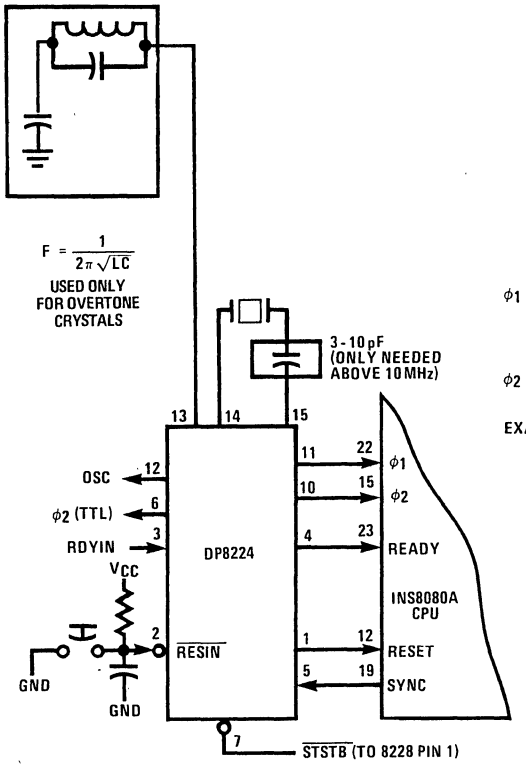
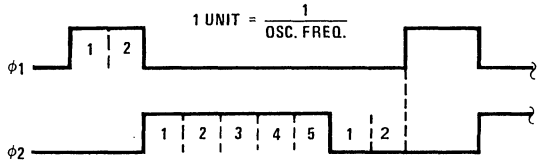


Figure A. DP8224 Connection Diagram



EXAMPLE: (8080 t_{CY} = 500 ns)
OSC = 18 mHz/55 ns
$\phi 1$ = 110 ns (2 x 55 ns)
$\phi 2$ = 275 ns (5 x 55 ns)
$\phi 2 - \phi 1$ = 110 ns (2 x 55 ns)

Figure B. DP8224 Clock Generator Waveforms

National Semiconductor

DP8228/DP8228M, DP8238/DP8238M System Controller and Bus Driver

General Description

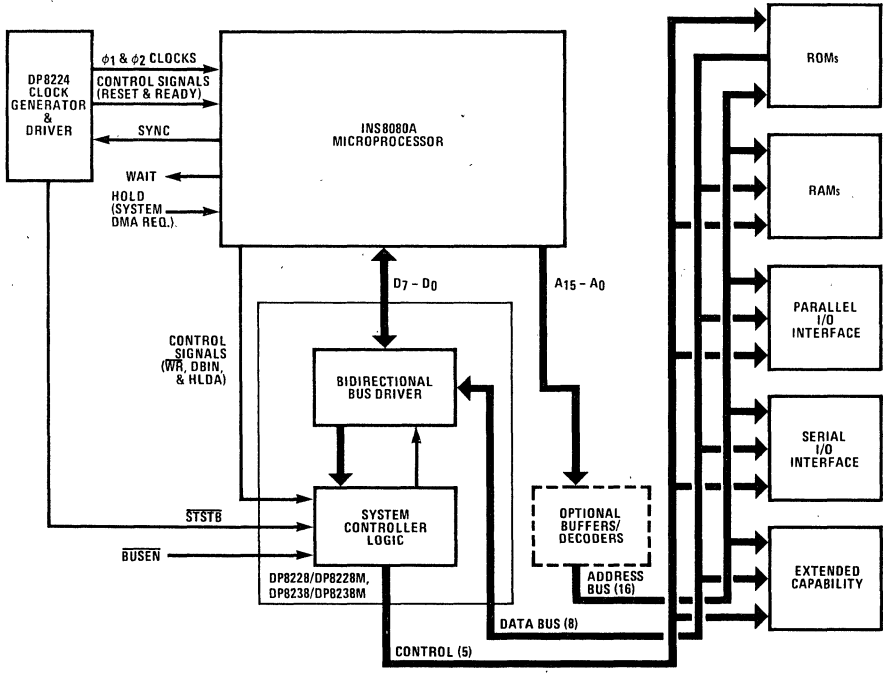
The DP8228/DP8228M, DP8238/DP8238M are system controller/bus drivers contained in a standard, 28-pin dual-in-line package. The chip, which is fabricated using Schottky Bipolar technology, generates all the read and write control signals required to directly interface the memory and input/output components of National Semiconductor's INS8080A microcomputer family. The chip also provides drive and isolation for the bidirectional data bus of the INS8080A microprocessor. Data bus isolation enables the use of slower memory and input/output components in a system, and provides for enhanced system noise immunity.

A user-selected single-level interrupt vector (RST 7) is provided by the device for use in the interrupt structure of small systems that need only one basic vector. No additional components (such as an interrupt instruction port) are required to use the single interrupt vector in these systems. The devices also generate an Interrupt Acknowledge ($\overline{INTA}$) control signal for each byte of a multibyte CALL instruction when an interrupt is acknowledged by the INS8080A. This feature permits the use of a multilevel priority interrupt structure in large, interrupt-driven systems.

Features

- Single Chip System Controller and Bus Driver for INS8080A Microcomputer Systems
- Allows Use of Multibyte CALL Instructions for Interrupt Acknowledge
- Provides User-Selected Single-Level Interrupt Vector (RST 7)
- Provides Isolation for Data Bus
- Supports A Wide Variety of System Bus Structures
- Reduces System Component Count
- DP8238/DP8238M Provides Advanced Input/Output Write and Memory Write Control Signals for Large System Timing Control

N8080A Microcomputer Family Block Diagram



Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Supply Voltage, V_{CC}	−0.5V to +7V
Input Voltage	−1.5V to +7V
Output Current	100 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	2179 mW
Molded Package	2361 mW

*Derate cavity package 14.5 mW/°C above 25°C; derate molded package 18.9 mW/°C above 25°C.

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DP8228M, DP8238M	4.50	5.50	V_{DC}
DP8228, DP8238	4.75	5.25	V_{DC}
Operating Temperature (T_A)			
DP8228M, DP8238M	−55	+125	°C
DP8228, DP8238	0	+70	°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.

Electrical Characteristics

(Min ≤ T_A ≤ Max, Min ≤ V_{CC} ≤ Max, unless otherwise noted)

	PARAMETER	CONDITIONS		MIN	TYP (Note 1)	MAX	UNITS
V_C	Input Clamp Voltage, All Inputs	V_{CC} = Min, I_C = −5 mA			0.6	−1.0	V
I_F	Input Load Current	V_{CC} = Max					
	$\overline{STSTB}$	V_F = 0.45V for DP8228,DP8238				500	μA
	D2 and D6	V_F = 0.40V for DP8228M, DP8238M				750	μA
	D0, D1, D4, D5 and D7					250	μA
	All Other Inputs					250	μA
I_R	Input Leakage Current	V_{CC} = Max, V_R = V_{CC}					
	DB0–DB7					20	μA
	All Other Inputs					100	μA
V_{TH}	Input Threshold Voltage, All Inputs	V_{CC} = 5V		0.8		2.0	V
I_{CC}	Power Supply Current	V_{CC} = Max	DP8228, DP8238		160	190	mA
			DP8228M, DP8238M		160	210	mA
V_{OL}	Output Low Voltage						
	D0–D7	V_{CC} = Min, I_{OL} = 2 mA	DP8228M, DP8238M			0.50	V
			DP8228, DP8238			0.45	V
	All Other Outputs	V_{CC} = Min, I_{OL} = 10 mA	DP8228M, DP8238M			0.50	V
			DP8228, DP8238			0.45	V
V_{OH}	Output High Voltage						
	D0–D7	V_{CC} = Min, I_{OH} = −10 μA	DP8228M, DP8238M	3.3	3.8		V
			DP8228, DP8238	3.6	3.8		V
	All Other Outputs	V_{CC} = Min, I_{OH} = −1 mA		2.4	3.8		V
I_{OS}	Short Circuit Current, All Outputs	V_{CC} = 5V, V_O = 0V		15		90	mA
$I_{O(OFF)}$	OFF State Output Current	V_{CC} = Max, V_O = V_{CC}				100	μA
	All Control Outputs	V_{CC} = Max, V_O = 0.45V				−100	μA
I_{INT}	INTA Current	(See Test Conditions, *Figure 3*)				5	mA

Note 1: Typical values are for T_A = 25°C and typical supply voltages.

Capacitance

V_{BIAS} = 2.5V, V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz.

PARAMETER		MIN	TYP (Note 1)	MAX	UNITS
C_{IN}	Input Capacitance		8	12	pF
C_{OUT}	Output Capacitance Control Signals		7	15	pF
I/O	I/O Capacitance (D or DB)		8	15	pF

This parameter is periodically sampled and not 100% tested.

Switching Characteristics

(Min $\leq V_{CC} \leq$ Max, Min $\leq T_A \leq$ Max)

PARAMETER		CONDITIONS	DP8228M, DP8238M		DP8228, DP8238		UNITS
			MIN	MAX	MIN	MAX	
t_{PW}	Width of Status Strobe		25		22		ns
t_{SS}	Set-Up Time, Status Inputs D0–D7		8		8		ns
t_{SH}	Hold Time, Status Inputs D0–D7		5		5		ns
t_{DC}	Delay from $\overline{STSTB}$ to Any Control Signal	*(Figure 2)*	20	75	20	60	ns
t_{RR}	Delay from DBIN to Control Outputs	*(Figure 2)*		30		30	ns
t_{RE}	Delay from DBIN to Enable/ Disable 8080 Bus	*(Figure 1)*		45		45	ns
t_{RD}	Delay from System Bus to 8080 Bus during Read	*(Figure 1)*		45		30	ns
t_{WR}	Delay from $\overline{WR}$ to Control Outputs	*(Figure 2)*	5	60	5	45	ns
t_{WE}	Delay to Enable System Bus DB0–DB7 after $\overline{STSTB}$	*(Figure 2)*		30		30	ns
t_{WD}	Delay from 8080 Bus D0–D7 to System Bus DB0–DB7 during Write	*(Figure 2)*	5	40	5	40	ns
t_E	Delay from System Bus Enable to System Bus DB0–DB7	*(Figure 2)*		30		30	ns
t_{HD}	HLDA to Read Status Outputs	*(Figure 2)*		25		25	ns
t_{DS}	Set-Up Time, System Bus Inputs to HLDA		10		10		ns
t_{DH}	Hold Time, System Bus Inputs to HLDA		20		20		ns

Test Conditions

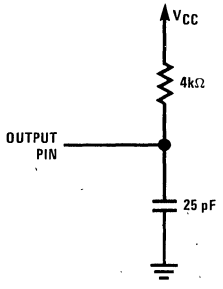


FIGURE 1. Test Load

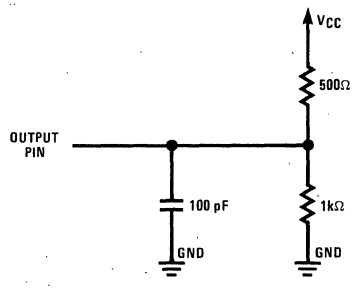


FIGURE 2. Test Load

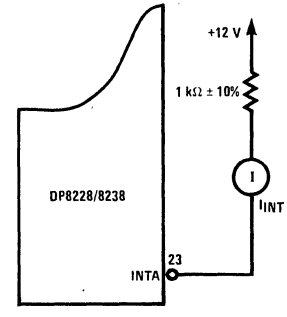
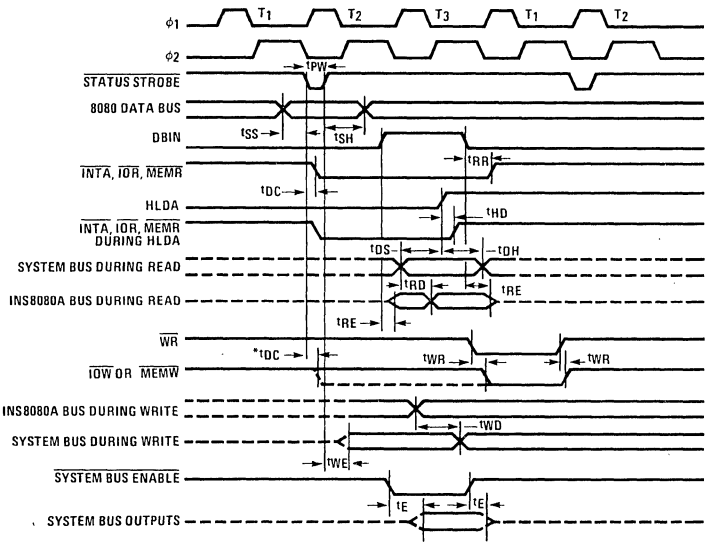


FIGURE 3. INTA Test Circuit (For RST 7)

Timing Diagram



VOLTAGE MEASUREMENT POINTS: D_0 - D_7 (when outputs) Logic "0" = 0.8 V, Logic "1" = 3.0 V. All other signals measured at 1.5 V.

*Advanced $\overline{I/OW}$ $\overline{MEMW}$ for 8238 only.

Functional Pin Definitions

The following describes the function of all of the DP8228/DP8228M, DP8238/DP8238M pinouts. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Status Strobe ($\overline{STSTB}$): Activated (low) at the start of each new machine cycle. The $\overline{STSTB}$ input is used to store a status word (refer to chart) from the INS8080A microprocessor into the internal status latch of the DP8228, DP8238. The status word is latched when the $\overline{STSTB}$ returns to the high state. The INS8080A outputs this status word onto its data bus during the first state (SYNC interval) of each machine cycle.

Data Bus In (DBIN): When high, indicates that the INS8080A data bus is in the input mode. The DBIN signal is used to gate data from memory or an input/output device onto the data bus.

Write ($\overline{WR}$): When low, indicates that the data on the INS8080A data bus are stable for WRITE memory or output operation.

Hold Acknowledge (HLDA): When high, indicates that the INS8080A data and address buses will go to their high impedance state. When in the data bus read mode, DBIN input in the high state, a high HLDA input will latch the data bus information into the driver circuits and gate off the applicable control signal $\overline{I/OR}$, $\overline{MEMR}$, or $\overline{INTA}$ (return to the output high state).

Bus Enable ($\overline{BUSEN}$): Asynchronous DMA input to the internal gating array. When low, normal operation of the internal bidirectional bus driver and gating array occurs. When high, the bus driver and gating array are driven to their high impedance state.

V_{CC} Supply: +5 volts.

Ground: 0 volt reference.

OUTPUT SIGNALS

Memory Read ($\overline{MEMR}$): When low, signals data to be loaded in from memory. The $\overline{MEMR}$ signal is generated by strobing in status word 1, 2, or 4. (Refer to status word chart.)

Memory Write ($\overline{MEMW}$): When low, signals data to be stored in memory. The $\overline{MEMW}$ signal is generated for the DP8238 by strobing in status word 3 or 5. (Refer to status word chart.) For the DP8228, the $\overline{MEMW}$ signal is generated by gating a low-level $\overline{WR}$ input with the strobed in status word 3 or 5.

Input/Output Read ($\overline{I/OR}$): When low, signals data to be loaded in from an addressed input/output device. The $\overline{I/OR}$ signal is generated by strobing in status word 6.

Input/Output Write ($\overline{I/OW}$): When low, signals data to be transferred to an addressed input/output device. The $\overline{I/OW}$ signal for the DP8238 is generated by strobing in status word 7. For the DP8228 the $\overline{I/OW}$ signal is generated by gating in a low-level $\overline{WR}$ input with the strobed in status word 7.

Interrupt Acknowledge ($\overline{INTA}$): When low, indicates that an interrupt has been acknowledged by the INS8080A microprocessor. The $\overline{INTA}$ signal is generated by strobing in status word 8 or 10.

Single Level Interrupt (RST 7): When the $\overline{INTA}$ output is tied to 12 V through a 1 kΩ resistor, strobing in status word 8 or 10 will cause the CPU data bus outputs, when active, to go to the high state.

INPUT/OUTPUT SIGNALS

CPU Data (D_7 - D_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the INS8080A microprocessor. The bus provides bidirec-

Functional Pin Definitions (Continued)

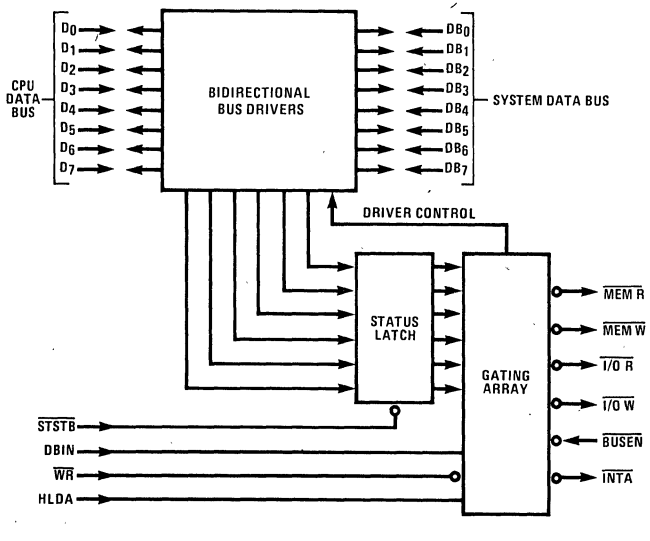
tional communication between the CPU, memory, and input/output devices for instructions and data transfers. A status word (which describes the current machine cycle) is also outputted on this data bus during the first microcycle of each machine cycle (SYNC = logic 1).

System Data (DB_7 - DB_0) Bus: This bus comprises eight TRI-STATE input/output lines that connect to the memory and input/output components of the system. The internal bidirectional bus driver isolates the DB_7 - DB_0 Data Bus from the D_7 - D_0 Data Bus.

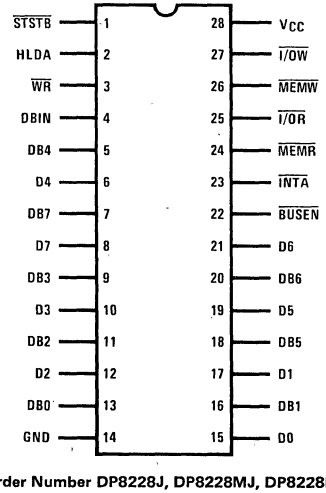
Status Word Chart

Machine Cycle	Status Word	Data Bus Bit								Control Signal
		D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Instruction Fetch	1	1	0	1	0	0	0	1	0	$\overline{MEMR}$
Memory Read	2	1	0	0	0	0	0	1	0	$\overline{MEMR}$
Memory Write	3	0	0	0	0	0	0	0	0	$\overline{MEMW}$
Stack Read	4	1	0	0	0	0	1	1	0	$\overline{MEMR}$
Stack Write	5	0	0	0	0	0	1	0	0	$\overline{MEMW}$
Input Read	6	0	1	0	0	0	0	1	0	$\overline{I/OR}$
Output Write	7	0	0	0	1	0	0	0	0	$\overline{I/OW}$
Interrupt Acknowledge	8	0	0	1	0	0	0	1	1	$\overline{INTA}$
Halt Acknowledge	9	1	0	0	0	1	0	1	0	(none)
Interrupt Acknowledge While Halt	10	0	0	1	0	1	0	1	1	$\overline{INTA}$

Block and Connection Diagrams



Dual-In-Line Package



Order Number DP8228J, DP8228MJ, DP8228N, DP8238J, DP8238MJ or DP8238N
See NS Package J28A or N28A

Section 9
Data Communications Support

9

National Semiconductor

Data Communications Support

DP8340 Serial Bi-Phase Transmitter/Encoder

General Description

The DP8340 generates a complete encoding of parallel data for high speed serial transmission which conforms to the protocol as defined by the IBM 3270 information display system standard. The DP8340 converts parallel input data into a serial data stream. Although the IBM standard covers bi-phase serial data transmission over a coax line, the DP8340 also adapts to general high speed serial data transmission over other than coax lines, at frequencies either higher or lower than the IBM standard.

The DP8340 and its complementary chip, the DP8341 (receiver/decoder) have been designed to provide maximum flexibility in system designs. The separation of the transmitter/receiver functions provides convenient addition of more receivers at one end of a bi-phase line without the need of unused transmitters. This is specifically advantageous in control units where typical bi-phase data is multiplexed over many bi-phase lines and the number of receivers generally exceeds the number of transmitters.

Features

- Ten bits per data byte transmission
- Single-byte or multi-byte transmission
- Internal parity generation (even or odd)
- Internal crystal controlled oscillator used for the generation of all required chip timing frequencies
- Clock output directly drives receiver (DP8341) clock input
- Input data holding register
- Automatic clear status response feature
- Line drivers at data outputs provide easy interface to bi-phase coax line or general transmission lines
- <2ns driver output skew
- Bipolar technology provides TTL input/output compatibility
- Data outputs power up/down glitch free
- Internal power up clear and reset
- Single +5V power supply

Connection Diagram

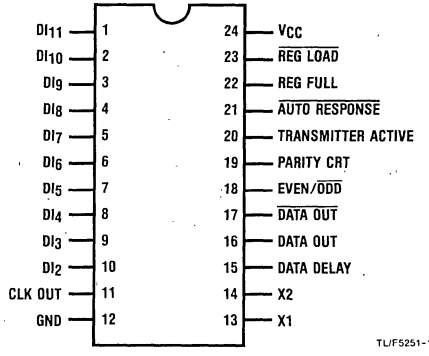


FIGURE 1. Pin-Out Diagram

Order Number DP8340J or DP8340N
See NS Package J24A or N24A

Block Diagram

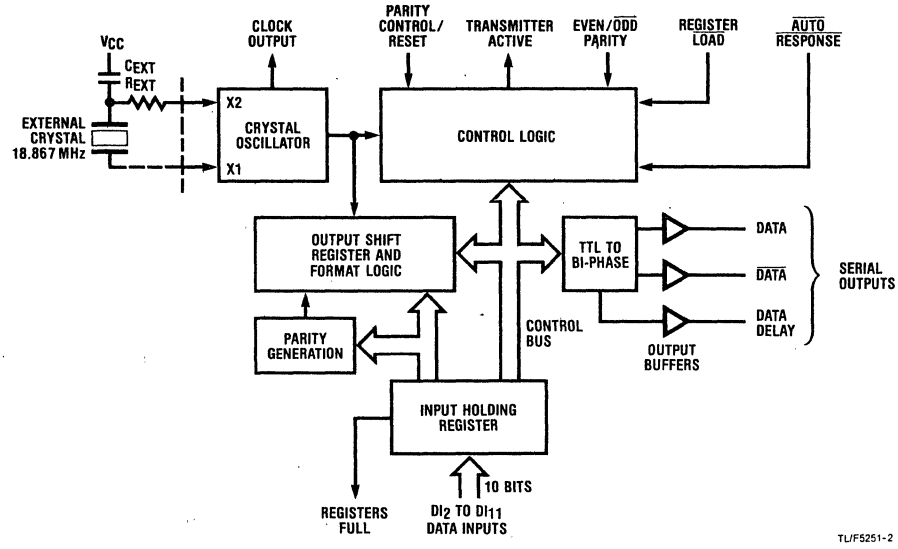


FIGURE 2. DP8340 Serial Bi-Phase Transmitter/Encoder Block Diagram

Block Diagram Functional Description

Figure 2 is a block diagram of the DP8340 Bi-Phase Transmitter/Encoder. The transmitter/encoder contains a crystal oscillator whose input is a crystal with a frequency eight (8) times the data rate. A Clock Output is provided to drive the DP8341 receiver/decoder Clock Input and other system components at the oscillator frequency. Additionally, the oscillator drives the control logic and output shift register/format logic blocks.

Data is parallel loaded from the system data bus to the transmitter/encoder's input holding register. This data is in turn loaded by the transmitter/encoder to its output shift register if this register was empty at the time of the load. During this load, message formatting and parity are generated. The formatted message is then shifted out at the bit rate frequency to the TTL to Bi-Phase block which generates the proper data bit formatting. The three data outputs, DATA, $\overline{\text{DATA}}$, and DATA DELAY provide for flexible interface to the coax line with a minimum of external components.

The Control Logic block interfaces to all blocks to insure proper chip operation and sequencing. It controls the type of parity generation through the Even/Odd Parity input. An additional feature provided by the transmitter/encoder is generation of odd parity and placement in bit 10 position while still maintaining even or odd parity in the bit 12 position. This is the format of data word bytes and other commands in the 3270 Standard. The Parity Control input is the pin which controls when this operation is in effect.

Another feature of the transmitter/encoder is the internal TT/AR (Transmission Turnaround/Auto Response) capability. After each Write type message from the control unit in the 3270 Standard, the receiving unit must respond with clean status (bits 2 through 11). With the transmitter/ encoder this function is accomplished simply by forcing the $\overline{\text{Auto-Response}}$ input to the Logic "0" state.

Operation of the transmitter/encoder is automatic. After the first data byte is loaded, the Transmitter Active output is set and the transmitter/encoder immediately formats the input data and serially shifts it out its data outputs. If the message is a multi-byte message, the internal format logic will modify the message data format for multibyte as long as the next byte is loaded to the input holding register before the last data bit of the previous data byte is transferred out of the internal output shift register. After all data is shifted out of the transmitter/encoder the Transmitter Active output will return to the inactive state.

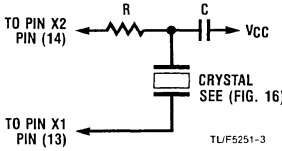
Detailed Pin/Functional Description

Crystal Inputs X1 and X2

The oscillator is controlled by an external, parallel resonant crystal connected between the X1 and X2 pins. Normally, a fundamental mode crystal is used to determine the operating frequency of the oscillator; however, overtone mode crystals may be used.

Crystal Specifications (Parallel Resonant)

Type	AT-cut crystal
Tolerance	0.005% at 25°C
Stability	0.01% from 0°C to +70°C
Resonance	Fundamental (Parallel)
Maximum Series Resistance	Dependent on Frequency (For 18.867 MHz, 50Ω)
Load Capacitance	15pF



FREQ	R	C
<20 MHz	500Ω ±10%	30pF
>20 MHz	120Ω ±10%	15pF

FIGURE 3. Connection Diagram

If the DP8340 transmitter is clocked by a system clock (crystal oscillator not used), pin 13 (X1 input) should be clocked directly using a Schottky series (74S) circuit. Pin 14 (X2 input) may be left open. The clocking frequency must be set at eight times the data bit rate. Maximum input frequency is 28 MHz. For the IBM 3270 Interface, this frequency is 18.867 MHz. At this frequency, the serial bit rate will be 2.358 Mbits/sec.

Clock Output

The Clock Output is a buffered output derived directly from the crystal oscillator block and clocks at the oscillator frequency. It is designed to directly drive the DP8341 receiver/decoder Clock Input as well as other system components.

Registers Full

This output is used as a flag by the external operating system. A logic "1" (active state) on this output indicates that both the internal output shift register and the input holding register contain active data. No additional data should be loaded until this output returns to the logic "0" state (inactive state).

Transmitter Active

This output will be in the logic "1" state while the transmitter/encoder is about to transmit or in the process of transmitting data. Otherwise, it will assume the logic "0" state indicating no data presently in either the input holding or output shift registers.

$\overline{\text{Register Load}}$

The $\overline{\text{Register Load}}$ input is used to load data from the Data Inputs to the input holding register. The loading function is edge sensitive, the data present during the logic "0" state of this input is loaded, and the input data must be valid before the logic "0" to logic "1" transition. It is after this transition that the transmitter/encoder begins formatting of data for serial transmission.

$\overline{\text{Auto Response}}$ (TT/AR)

This input provides for automatic clear data transmission (all bits in logic "0") without the need of loading all zero's. When a logic "0" is forced on this input the transmitter/encoder immediately responds with transmission of "clean status". This function is necessary after the completion of each write type command and in other functions in the 3270 specification. In the logic "1" state the transmitter/encoder transmits data entered on the Data Inputs.

Even/$\overline{\text{Odd}}$ Parity

This input sets the internal logic of the DP8340 transmitter/encoder to generate either even or odd parity for the data byte in the bit 12 position. When this pin is in the logic "0" state odd parity is generated. In the logic "1" state even parity is generated. This feature is useful when the control unit is performing a loop back check and at the same time the controller wishes to verify proper data transmission with its receiver/decoder.

Parity Control/Reset

Depending on the type of message transmitted, it is at times necessary in the IBM 3270 specification to generate an additional parity bit in the bit 10 position. The bit generated is odd parity on the previous eight (8) bits of data. When the Parity Control input is in the logic "1" state the data entered at the Data Bit 10 position is placed in the transmitted word. With the Parity Control input in the logic "0" state the Data Bit 10 input is ignored and odd parity on the previous data bits is placed in the normal bit 10 position while overall word parity (bit 12) is even or odd (controlled by Even/$\overline{\text{Odd}}$ Parity input). This eliminates the need for external logic to generate the parity on the data bits.

Truth Table

Parity Control Input	Transmitted Data Bit 10
Logic "1"	Data entered on Data Input 10
Logic "0"	Odd Parity on 8-bit data byte

When this input is driven to a voltage that exceeds the power supply level (7V to 13V) the transmitter/encoder is reset.

Serial Outputs — DATA, $\overline{\text{DATA}}$, and DATA DELAY

These three output pins provide for convenient application of data to the Bi-Phase Coax line (see Figure 15 for application). The Data outputs are a direct bit representation of the Bi-Phase data while the DATA DELAY output provides the necessary increment to clearly define the four (4) DC levels of the pulse. The DATA and $\overline{\text{DATA}}$ outputs add flexibility to the DP8340 transmitter/encoder for use in high speed differential line driving applications.

Functional Timing Waveforms — Message Format

Single Byte Transmission

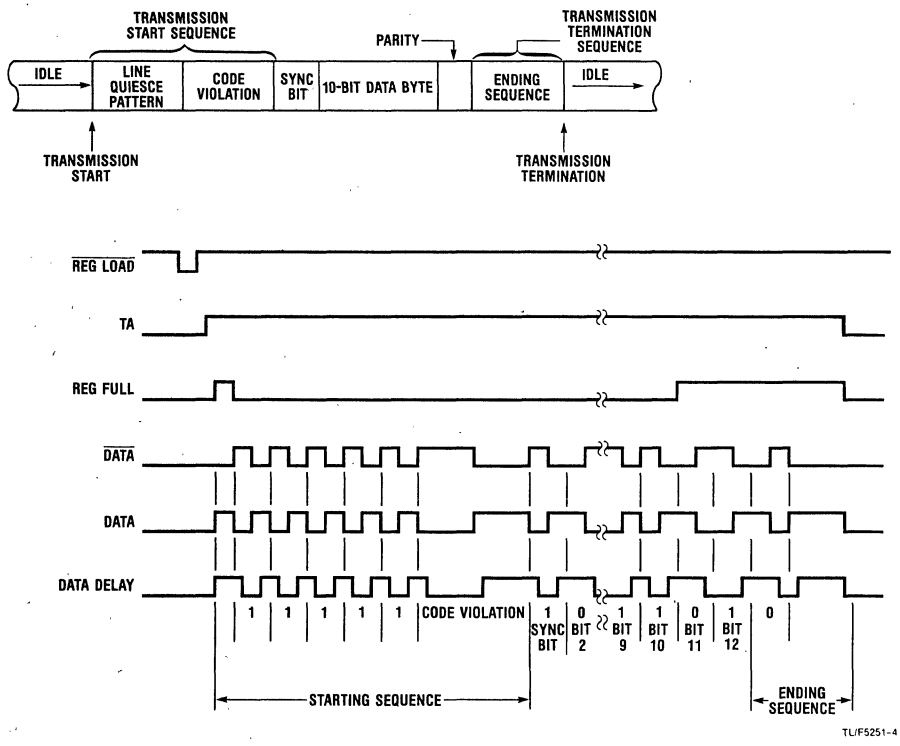


FIGURE 4. Overall Timing Waveforms for Single Byte

Multi-Byte Transmission

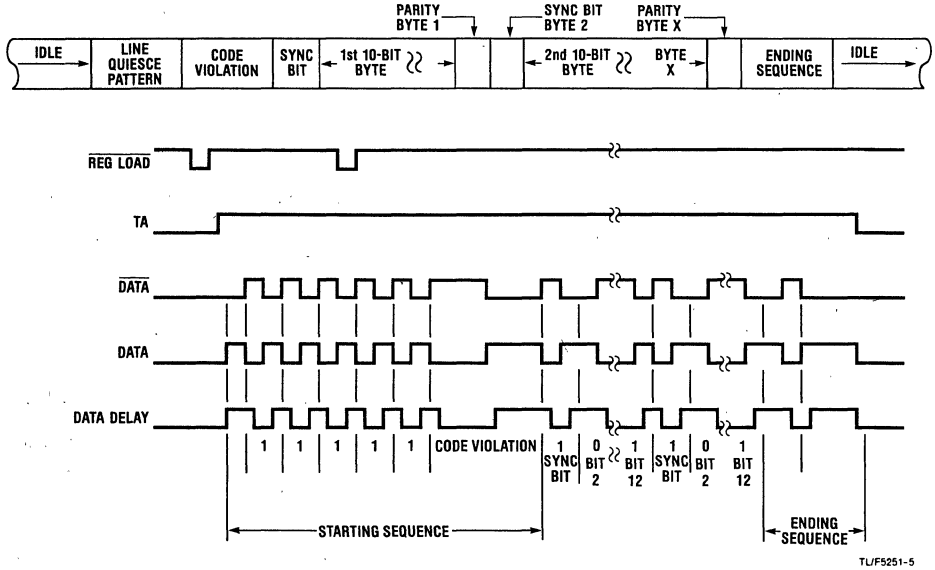


FIGURE 5. Overall Timing Waveforms for Multi-Byte

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Output Voltage	5.25V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 seconds)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	2237 mW
Molded Package	2500 mW

* Derate cavity package 14.9 mW/°C above 25°C; derate molded package 20 mW/°C above 25°C.

Operating Conditions

	Min.	Max.	Units
Supply Voltage, (V_{CC})	4.75	5.25	V
Ambient Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Logic "1" Input Voltage (All Inputs Except X1 and X2)		2.0			V
V_{IL}	Logic "0" Input Voltage (All Inputs Except X1 and X2)				0.8	V
V_{CLAMP}	Input Clamp Voltage (All Inputs Except X1 and X2)	$I_{IN} = -12$ mA		−0.8	−1.2	V
I_{IH}	Logic "1" Input Current Register Load Input	$V_{CC} = 5.25$V, $V_{IN} = 5.25$V		0.3	120	μA
	All Others Except X1 and X2			0.1	40	μA
I_{IL}	Logic "0" Input Current Register Load Input	$V_{CC} = 5.25$V, $V_{IN} = 0.5$V		−15	−300	μA
	All Inputs Except X1 and X2			−5	−100	μA
V_{OH1}	Logic "1" All Outputs Except CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY	$I_{OH} = -100\mu$A	3.2	3.9		V
		$I_{OH} = -1$ mA	2.5	3.4		V
V_{OH2}	Logic "1" for CKL OUT, DATA, $\overline{DATA}$ and DATA DELAY Outputs	$I_{OH} = -10$ mA	2.6	3.0		V
V_{OL1}	Logic "0" All Outputs Except CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY	$I_{OL} = 5$ mA		0.35	0.5	V
V_{OL2}	Logic "0" for CLK OUT, DATA, $\overline{DATA}$ and DATA DELAY Outputs	$I_{OL} = 20$ mA		0.4	0.6	V
I_{OS1}	Short Circuit Current for All Outputs Except CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY	$V_{OUT} = 0$V Note 4	−10	−30	−100	mA
I_{OS2}	Short Circuit Current for DATA, $\overline{DATA}$, and DATA DELAY Outputs	$V_{OUT} = 0$V Note 4	−50	−140	−250	mA
I_{OS3}	Short Circuit Current for CLK OUT	Note 4	−30	−90	−200	mA
I_{CC}	Power Supply Current	$V_{CC} = 5.25$V		170	250	mA

Timing Characteristics Oscillator Frequency = 18.867 MHz (Notes 2 and 3)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd1}	$\overline{REG\ LOAD}$ to Transmitter Active (T_A) Positive Edge	Load Circuit 1 Figure 7		60	90	ns
t_{pd2}	$\overline{REG\ LOAD}$ to REG FULL; Positive Edge	Load Circuit 1 Figure 7		45	75	ns
t_{pd3}	Register Full to T_A; Negative Edge	Load Circuit 1 Figure 7		40	70	ns
t_{pd4}	Positive Edge of $\overline{REG\ LOAD}$ to Positive Edge of DATA	Load Circuits 1 & 2 Figure 9		50	80	ns
t_{pd5}	$\overline{REG\ LOAD}$ to $\overline{DATA}$; Positive Edge	Load Circuits 1 & 2 Figure 9, Note 6		380	475	ns
t_{pd6}	$\overline{REG\ LOAD}$ to DATA DELAY; Positive Edge	Load Circuits 1 & 2 Figure 9, Note 6		160	250	ns

Timing Characteristics (Continued) Oscillator Frequency = 18.867 MHz (Notes 2 and 3)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd7}	Positive Edge of $\overline{DATA}$ to Negative Edge of DATA DELAY	Load Circuit 2 Figure 9, Note 6		100	115	ns
t_{pd8}	Positive Edge of DATA DELAY to Negative Edge of $\overline{DATA}$	Load Circuit 2 Figure 9, Note 6		110	125	ns
t_{pd9}, t_{pd10}	Skew between DATA and $\overline{DATA}$	Load Circuit 2 Figure 9		2	6	ns
t_{pd11}	Negative Edge of Auto Response to Positive Edge of TA	Load Circuit 1 Figure 10		70	110	ns
t_{pd12}	Maximum Time Delay to Load Second Byte After Positive Edge of REG FULL	Load Circuit 1 Figure 8, Note 6			4×T−50	ns
t_{pd13}	X1 to CLK OUT; Positive Edge	Load Circuit 2 Figure 13		21	30	ns
t_{pd14}	X1 to CLK OUT; Negative Edge	Load Circuit 2 Figure 13		23	33	ns
t_{pd15}	Negative Edge of AR to Positive Edge of REG FULL	Load Circuit 1 Figure 10		45	75	ns
t_{pd16}	Skew between TA and REG FULL during Auto Response	Load Circuit 1 Figure 10		50	80	ns
t_{pd17}	$\overline{REG\ LOAD}$ to REG FULL; Positive Edge for Second Byte	Load Circuit 1 Figure 14		45	75	ns
t_{pw1}	$\overline{REG\ LOAD}$ Pulse Width	Figure 12	40			ns
t_{pw2}	First REG FULL Pulse Width (note 5)	Load Circuit 1 Figure 7, Note 6		8×T+60	8×T+100	ns
t_{pw3}	REG FULL Pulse Width Prior to Ending Sequence(Note 5)	Load Circuit 1, Figure 7, Note 6		5×B		ns
t_{pw4}	Pulse Width for Auto Response	Figure 10	40			ns
t_S	Data Setup Time prior to $\overline{REG\ LOAD}$ Positive Edge. Hold Time (t_H) = 0 ns	Figure 12		15	25	ns
t_{r1}	Rise Time for DATA, $\overline{DATA}$, and DATA DELAY Output Waveform	Load Circuit 2 Figure 11		7	13	ns
t_{f1}	Fall Time for DATA, $\overline{DATA}$, and DATA DELAY Output Waveform	Load Circuit 2 Figure 11		5	11	ns
t_{r2}	Rise Time for TA and REG FULL	Load Circuit 1 Figure 15		20	30	ns
t_{f2}	Fall Time for TA and REG FULL	Load Circuit 1 Figure 15		15	25	ns
f_{MAX}	Data Rate Frequency (Clock Input must be 8X this Frequency)	Note 7	DC		3.5	Mbits/s

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min./max. limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

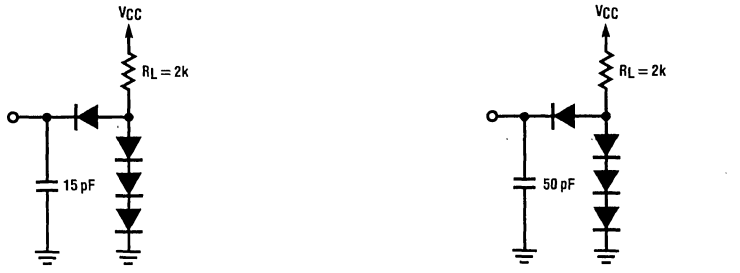
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max. or min. are so classified on absolute basis.

Note 4: Only one output should be shorted at a time.

Note 5: T = 1/(Oscillator Frequency), unit for T should be ns. B = 8T

Note 6: Oscillator Frequency Dependent.

Note 7: For the IBM 3270 Interface, the data rate frequency is 2.358 Mbits/s.



Load Circuit 1 Load Circuit 2

TL/F5251-6

FIGURE 6. Test Load Circuits

Timing Waveforms

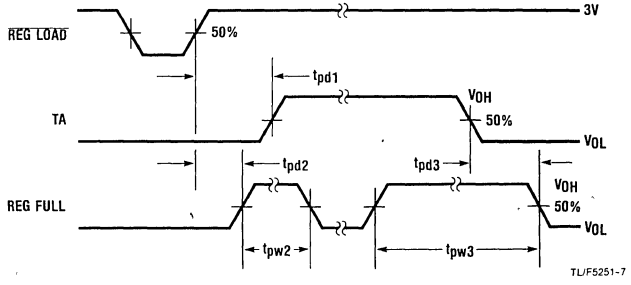


FIGURE 7. Timing Waveforms for Single Byte Transfer

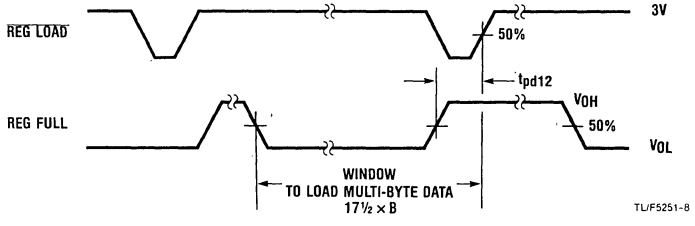


FIGURE 8. Maximum Window to Load Multi-Byte Data

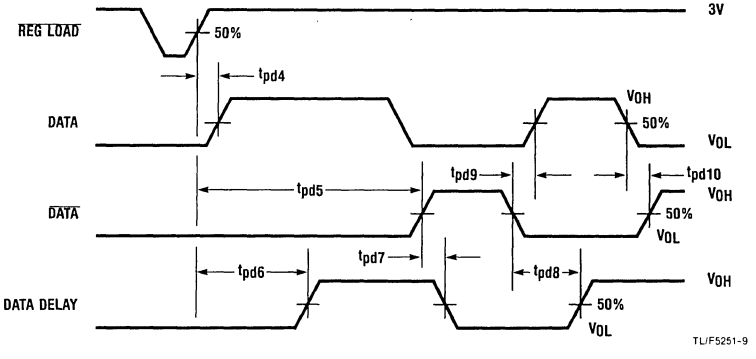


FIGURE 9. Timing Waveforms for Three Serial Outputs

Timing Waveforms (Continued)

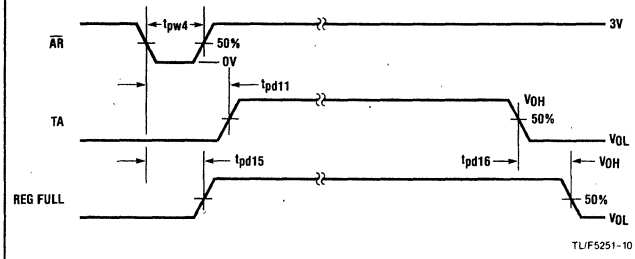


FIGURE 10. Timing Waveforms for $\overline{\text{Auto-Response}}$

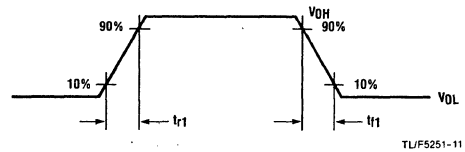


FIGURE 11. Output Waveform for DATA, $\overline{\text{DATA}}$, DATA DELAY (Load Circuit 2)

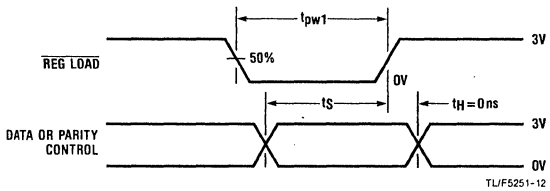


FIGURE 12. Register Load Waveform Requirement

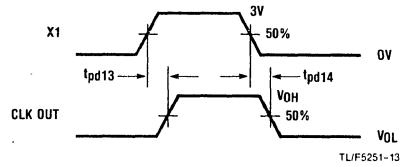


FIGURE 13. Timing Waveforms For Clock Pulse

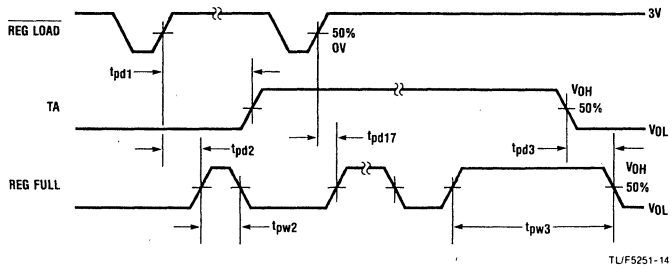


FIGURE 14. Timing Waveforms For Two Byte Transfer

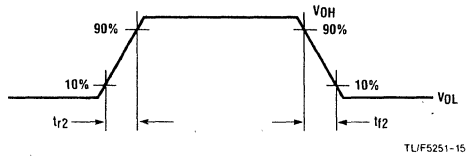


FIGURE 15. Rise and Fall Time Measurement for TA and REG Full

Typical Applications

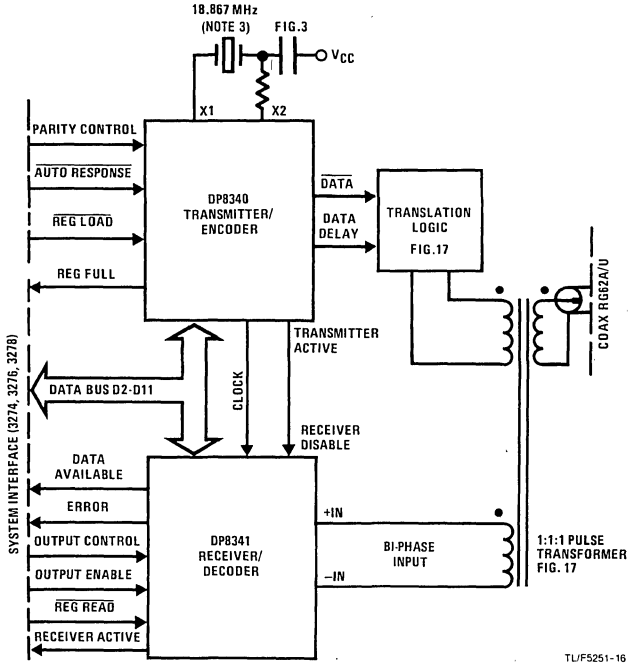
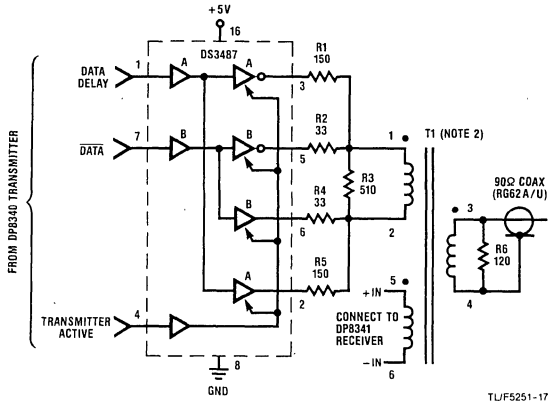


FIGURE 16. Typical Application For IBM 3270 Interface



Notes: 1) Resistance values are in ohms, ±5%, ¼W
2) T1 is a 1:1:1 pulse transformer, $L_{MIN} = 500\mu H$ for 18MHz system clock
Pulse Engineering Part No. 5763
Technitrol Part No. 11LHA or equivalent transformers
3) Crystal manufacturer Midland Ross Corp. NEL Unit Part No. NE-18A
@ 18.867MHz.

FIGURE 17. Translation Logic

National Semiconductor

Data Communications Support

DP8341 Serial Bi-Phase Receiver/Decoder

General Description

The DP8341 provides complete decoding of data for high speed serial data communications. In specific, the DP8341 recognizes serial data that conforms to the IBM 3270 Information Display System Standard and converts it into ten (10) bits of parallel data. Although this standard covers Bi-Phase serial data transmission over a coax line, this device easily adapts to generalized high speed serial data transmission on other than coax lines at frequencies either higher or lower than the IBM 3270 standard.

The DP8341 receiver and its complementary chip, the DP8340 transmitter, are designed to provide maximum flexibility in system designs. The separation of transmitter and receiver functions allows addition of more receivers at one end of the Bi-Phase line without the necessity of adding unused transmitters. This is advantageous specifically in control units where typically Bi-Phase data is multiplexed over many Bi-Phase lines and the number of receivers generally outnumber the number of transmitters. The separation of transmitter and receiver function provides an additional advantage in flexibility of data bus organization. The data bus outputs of the receiver are TRI-STATE®, thus enabling the bus configuration to be organized as either a common transmit/receive (bi-directional) bus or as separate transmit and receive busses for higher speed.

Features

- DP8341 receives ten (10) bit data bytes and conforms to the IBM 3270 Interface Display System Standard
- Separate receiver and transmitter provide maximum system design flexibility
- Even parity detection
- High sensitivity input on receiver easily interfaces to coax line
- Standard TTL data input on receiver provides generalized transmission line interface and also provides hysteresis
- Data holding register
- Multi-byte or single byte transfers
- TRI-STATE receiver data outputs provide flexibility for common or separated transmit/receive data bus operation.
- Data transmission error detection on receiver provides for both error detection and error type definition
- Bi-polar technology provides TTL input/output compatibility with excellent drive characteristics
- Single +5V power supply operation

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Connection Diagram

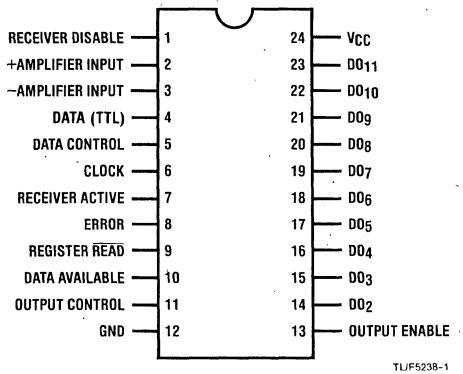


FIGURE 1. Pin-Out Diagram

Order Number DP8341J or DP8341N
See NS Package J24A or N24A

Block Diagram

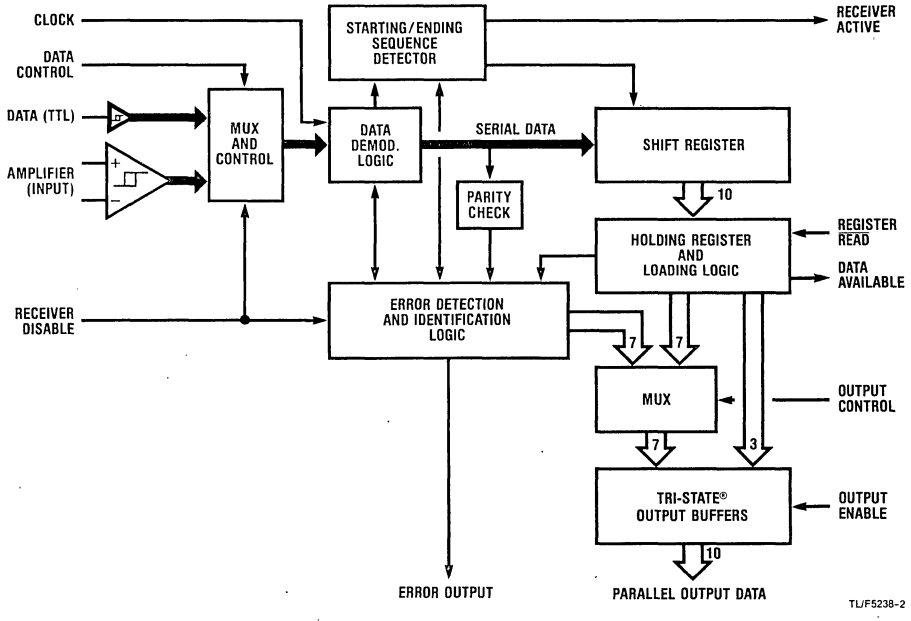


FIGURE 2. DP8341 Serial Bi-Phase Receiver/Decoder Block Diagram

Block Diagram Functional Description

Figure 2 is a block diagram of the DP8341. This chip is essentially a serial in/parallel out shift register. However, the serial input data must conform to a very specific format (see *Figures 3-5*). The message will not be recognized unless the format of the starting sequence is correct. Deviations from the format in the data, sync bit, parity or ending sequence will cause an error to be detected, terminating the message.

Data enters the receiver through the differential input amplifier or the TTL Data input. The differential amplifier is a high sensitivity input which may be used by connecting it directly to a transformer coupled coax line, or other transmission medium. The TTL Data input provides 400 mV of hysteresis and recognizes TTL logic levels. The data then enters the demodulation block.

The data demodulation block samples the data at eight (8) times the data rate and provides signals for detecting the starting sequence, ending sequence, and errors. Detection of the starting sequence sets the Receiver Active output high and enables the input shift register.

As the ten bits of data are shifted into the shift register, the receiver will verify that even parity is maintained on the data bits and the sync bit. After one complete data byte is received, the contents of the input shift register is parallel loaded to the holding register, assuming the holding register is empty, and the Data Available output is set. If the holding register is full, this load will be delayed until that register has been read. If another data byte is received when the shift register and the holding register are full a Data Overflow Error will be detected, terminating the message. Data is read from the holding register through the TRI-STATE Output Buffers. The Output Enable input is the TRI-STATE control for these outputs and the Register Read input signals the receiver that the read has been completed.

When the receiver detects an ending sequence the Receiver Active output will be reset to a logic "0" indicating the message has been terminated. A message will also terminate when an error is detected. The Receiver Active output used in conjunction with the Error output allows quick response to the transmitting unit when an error free message has been received.

The Error Detection and Identification block insures that valid data reaches the outputs of the receiver. Detection of an error sets the Error output to a logic "1" and resets the Receiver Active output to a logic "0" terminating the message. The error type may be read from the data bus outputs by setting the Output Control input to logic "0" and enabling the TRI-STATE outputs. The data bit outputs have assigned error definitions (see error code definition table). The Error output will return to a logic "0" when the next starting sequence is received, or when the error is read (Output Control to logic "0" and a Register Read performed).

The Receiver Disable input is used to disable both the amplifier and TTL Data receiver inputs. It will typically be connected directly to the Transmitter Active output of the DP8340 transmitter circuit (see *Figure 12*).

Detailed Functional Pin Description

Receiver Disable

This input is used to disable the receiver's data inputs. The Receiver Disable input will typically be connected to the Transmitter Active output of the DP8340. However, at the system controller it is necessary for both the transmitter and receiver to be active at the same time in the loop-back check condition. This variation can be accomplished with the addition of minimal external logic.

Truth Table

Receiver Disable	Data Inputs
Logic "0"	Active
Logic "1"	Disabled

Amplifier Inputs

The receiver has a differential input amplifier which may be directly connected to the transformer coupled coax line. The amplifier may also be connected to a differential type TTL line. The amplifier has 20 mV of hysteresis.

Data Input

This input can be used either as an alternate data input or as a power-up check input. If the system designer prefers to use his own amplifier, instead of the one provided on the receiver, then this TTL input may be used. Using this pin as an alternate data input allows self-test of the peripheral system without disturbing the transmission line.

Data Control

This input is the control pin that selects which of the inputs are used for data entry to the receiver.

Truth Table

Data Control	Data Input To
Logic "0"	Data Input
Logic "1"	Amplifier Inputs

Note: This input is also used for testing. When the inut voltage is raised to 7.5 V the chip resets.

Clock Input

This input is the internal clock of the receiver. It must be set at eight (8) times the line data bit rate. For the IBM 3270 Standard, this frequency is 18.87 MHz or a data bit rate of 2.358 MHz. The crystal-controlled oscillator provided in the DP8340 transmitter also operates at this frequency. The Clock Output of the transmitter is designed to directly drive the receiver's Clock Input. In addition, the receiver is designed to operate correctly to a data bit rate of 3.5 MHz.

Receiver Active

The purpose of this output is to inform the external system when the DP8341 is in the process of receiving a message. This output will transition to a logic "1" state after the receipt of a valid starting sequence and transition to logic "0" when a valid ending sequence is received or an error is detected. This output combined with the Error output will inform the operating system of the end of an error free data transmission.

Error

The Error output transitions to a logic "1" when an error is detected. Detection of an error causes the Receiver Active and the Data Available outputs to transition to a logic "0". The Error output returns to a logic "0" after the error register has been read or when the next starting sequence is detected.

Register Read

The Register Read input when driven to the logic "0" state signals the receiver that data in the holding register is being read by the external operating system. The data present in the holding register will continue to remain valid until the Register Read input returns to the logic "1" condition. At this time, if an additional byte is present in the input shift register it will be transferred to the holding register, otherwise the data will remain valid in the holding register. The Data Available output will be in the logic "0" state for a short interval while a new byte is transferred to the holding register after a register read.

Data Available

This output indicates the existence of a data byte within the output holding register. It may also indicate the presence of a data byte in both the holding register and the input shift register. This output will transition to the logic "1" state as soon as data is available and return to the logic "0" state after each data byte has been read. However, even after the last data byte has been read and the Data Available output has assumed the logic "0" state, the last data byte read from the holding register will remain until new data has been received.

Output Control

The Output Control input determines the type of information appearing at the data outputs. In the logic "1" state data will appear, in the logic "0" state error codes are present.

Truth Table

Output Control	Data Outputs
Logic "0"	Error Codes
Logic "1"	Data

Output Enable

The Output Enable input controls the state of the TRI-STATE Data outputs.

Truth Table

Output Enable	TRI-STATE® Data Outputs
Logic "0"	Disabled
Logic "1"	Active

Data Outputs

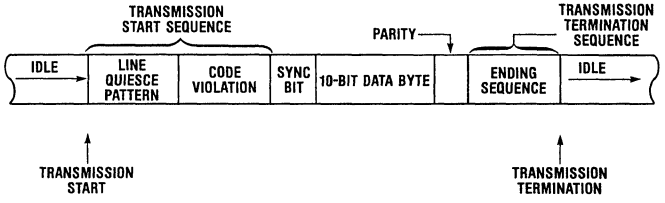
The DP8341 has a ten (10) bit TRI-STATE data bus. Seven bits are multiplexed with error bits. The error bits are defined in the table below. The Output Control input is the multiplexer control for the Data/Error bits.

Error Code Definition

Data Bit	Error Type
DO2	Data Overflow (Byte not removed from holding register when it and the input shift register are both full and new data is received)
DO3	Parity Error (Odd parity detected)
DO4	Transmit Check conditions (existence of errors on any or all of the following data bits: DO3, DO5, and DO6
DO5	An invalid ending sequence
DO6	Loss of mid-bit transition detected at other than normal ending sequence time
DO7	New starting sequence detected before data byte in holding register has been read
DO8	Receiver disabled during receiver active mode

Message Format

Single Byte Transmission



Multi-Byte Transmission

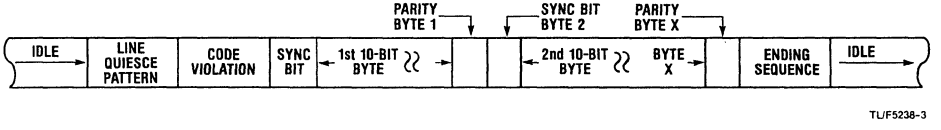


FIGURE 3. IBM 3270 Message Format

Message Format

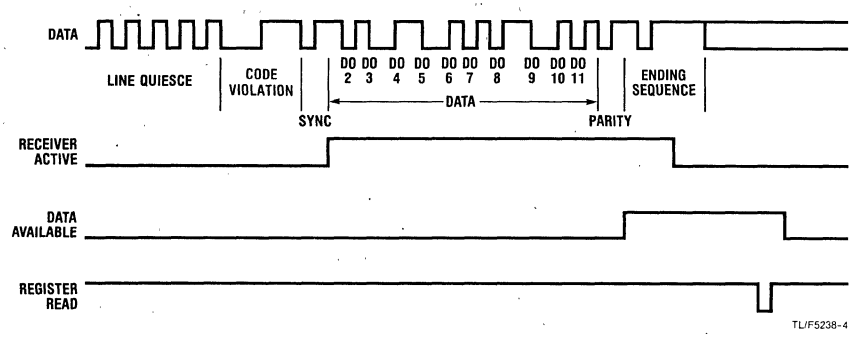


FIGURE 4A. Single Byte Message

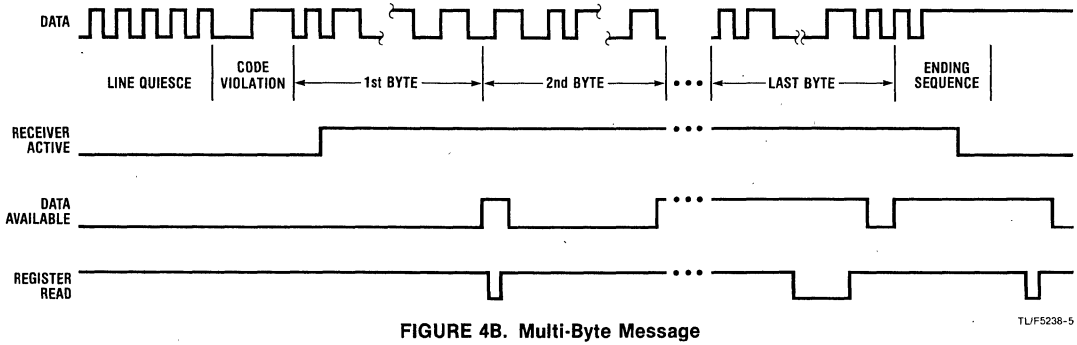


FIGURE 4B. Multi-Byte Message

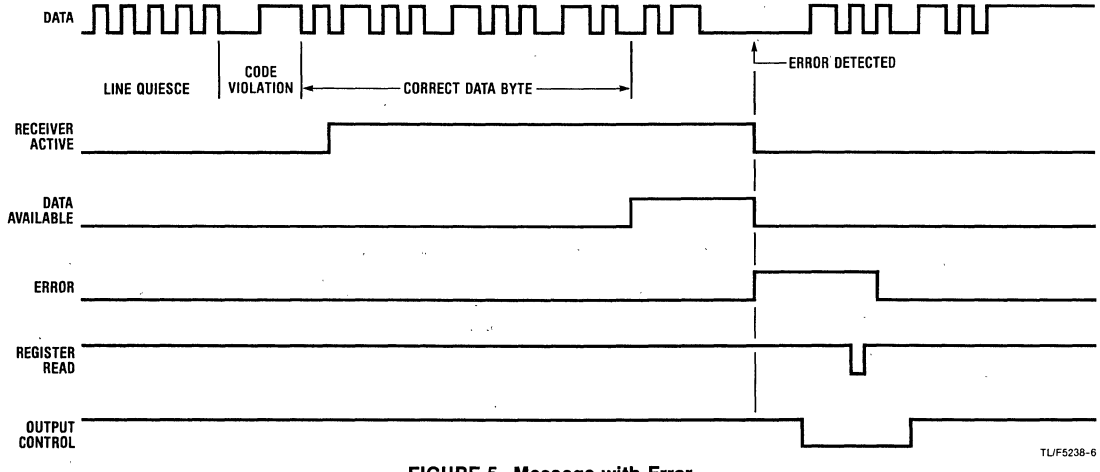


FIGURE 5. Message with Error

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	+5.5V
Output Voltage	5.25V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 seconds)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	2040 mW
Molded Package	2237 mW

*Derate cavity package 13.6 mW/°C above 25°C; derate molded package 17.9 mW/°C above 25°C.

Operating Conditions

	Min.	Max.	Units
Supply Voltage, (V_{CC})	4.75	5.25	V
Ambient Temperature, (T_A)	0	+70	°C

Electrical Characteristics (Notes 2, 3, and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level		2.0			V
V_{IL}	Input Low Level				0.8	V
$V_{IH}-V_{IL}$	Data Input Hysteresis (TTL, Pin 4)		0.2	0.4		V
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -12$ mA		−0.8	−1.2	V
I_{IH}	Logic "1" Input Current	$V_{CC} = 5.25V$, $V_{IN} = 5.25V$		2	40	μA
I_{IL}	Logic "0" Input Current	$V_{CC} = 5.25V$, $V_{IN} = 0.5V$		−20	−250	μA
V_{OH}	Logic "1" Output Voltage	$I_{OH} = -100$ μA	3.2	3.9		V
		$I_{OH} = -1$ mA	2.5	3.2		V
V_{OL}	Logic "0" Output Voltage	$I_{OL} = 5$ mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	$V_{CC} = 5V$, $V_{OUT} = 0V$ (See Note 4)	−10	−20	−100	mA
I_{OZ}	TRI-STATE® Output Current	$V_{CC} = 5.25V$, $V_O = 2.5V$	−40	1	+40	μA
		$V_{CC} = 5.25V$, $V_O = 0.5V$	−40	−5	+40	μA
A_{HYS}	Amplifier Input Hysteresis		5	20	30	mV
I_{CC}	Power Supply Current	$V_{CC} = 5.25V$		160	250	mA

Timing Characteristics (Notes 2, 6, 7, and 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{D1}	Output Data to Data Available Positive Edge		5	20	40	ns
T_{D2}	Register Read Positive Edge to Data Available Negative Edge		10	25	45	ns
T_{D3}	Error Positive Edge to Data Available Negative Edge		10	30	50	ns
T_{D4}	Error Positive Edge to Receiver Active Negative Edge		5	20	40	ns
T_{D5}	Register Read Positive Edge to Error Negative Edge		20	45	75	ns
T_{D6}	Delay from Output Control to Error Bits from Data Bits		5	20	50	ns
T_{D7}	Delay from Output Control to Data Bits from Error Bits		5	20	50	ns
T_{D8}	First Sync Bit Positive Edge to Receiver Active Positive Edge			3.5*T +70		ns
T_{D9}	Receiver Active Positive Edge to First Data Available Positive Edge			92*T		ns
T_{D10}	Negative Edge of Ending Sequence to Receiver Active Negative Edge			11.5*T +50		ns
T_{D11}	Data Control Set-up Multiplexer Time Prior to Receiving Data through Selected Input		40	30		ns

Timing Characteristics (Cont'd) (Notes 2, 6, 7, and 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{PW1}	Register Read (Data) Pulse Width		40	30		ns
T_{PW2}	Register Read (Error) Pulse Width		40	30		ns
T_{PW3}	Data Available Logic "0" State between Data Bytes		25	45		ns
T_S	Output Control Set-up Time Prior to Register Read Negative Edge		0	−5		ns
T_H	Output Control Hold Time After the Register Read Positive Edge		0	−5		ns
T_{ZE}	Delay from Output Enable to Logic "1" or Logic "0" from High Impedance State	Load Circuit 2		25	35	ns
T_{EZ}	Delay from Output Enable to High Impedance State from Logic "1" or Logic "0"	Load Circuit 2		25	35	ns
F_{MAX}	Data Bit Frequency (Clock Input must be 8× the Data Bit Frequency)		DC		3.5	MBits/s

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min./max. limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max. or min. are so classified on absolute value basis.

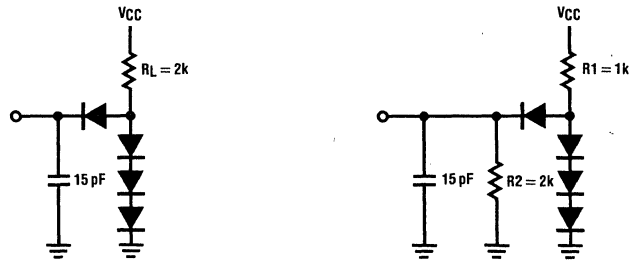
Note 4: Only one output at a time should be shorted.

Note 5: Input characteristics do not apply to amplifier inputs (pins 2 & 3).

Note 6: Unless otherwise specified, all AC measurements are referenced to the 1.5V level of the input to the 1.5V level of the output and load circuit 1 is used.

Note 7: AC tests are done with input pulses supplied by generators having the following characteristics: $Z_{OUT} = 50\Omega$ and $T_r \leq 5ns$, $T_f \leq 5ns$.

Note 8: T = 1/ (clock input frequency), units for "T" should be ns.



Load Circuit 1 **Load Circuit 2**

TL/F5238-7

FIGURE 6. Test Load Circuits

Timing Waveforms

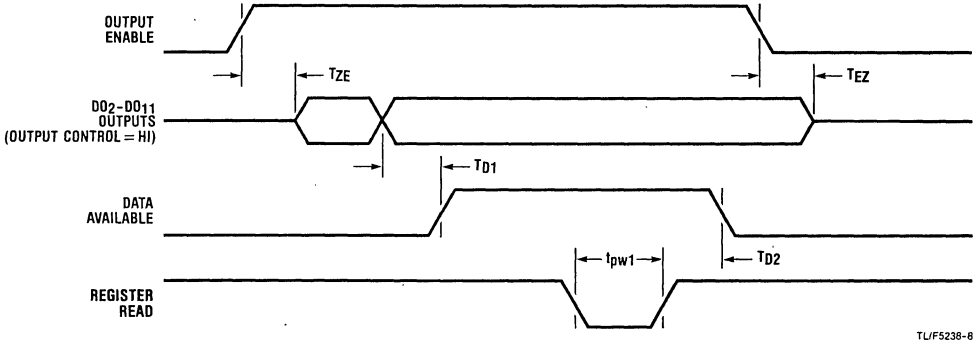


FIGURE 7. Data Sequence Timing

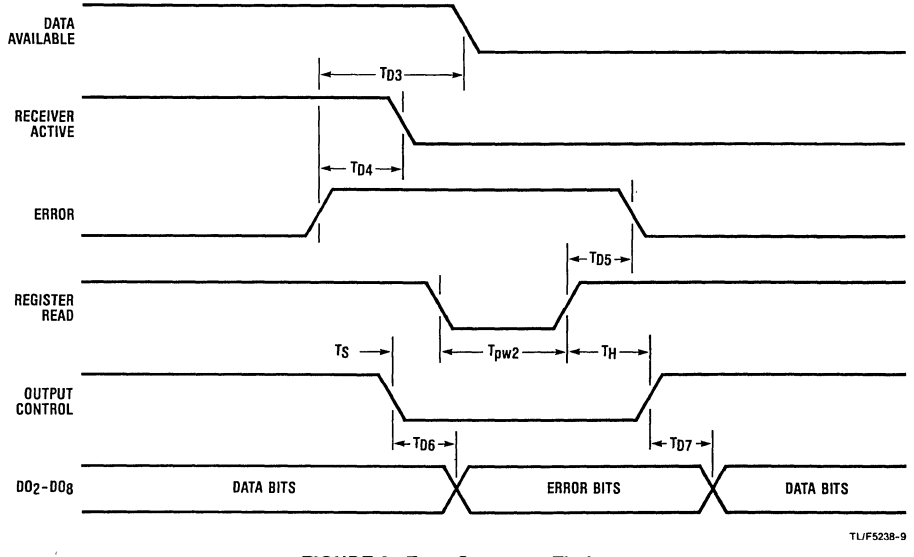


FIGURE 8. Error Sequence Timing

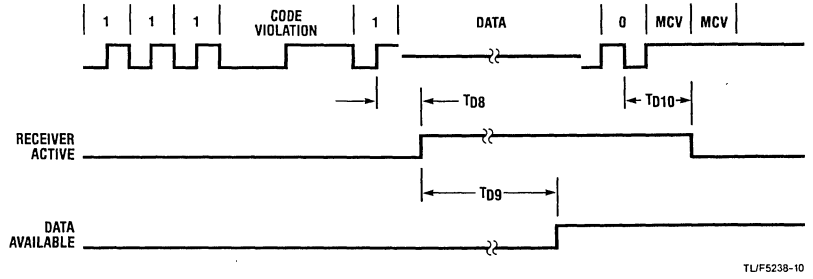


FIGURE 9. Message Timing

Timing Waveforms (Continued)

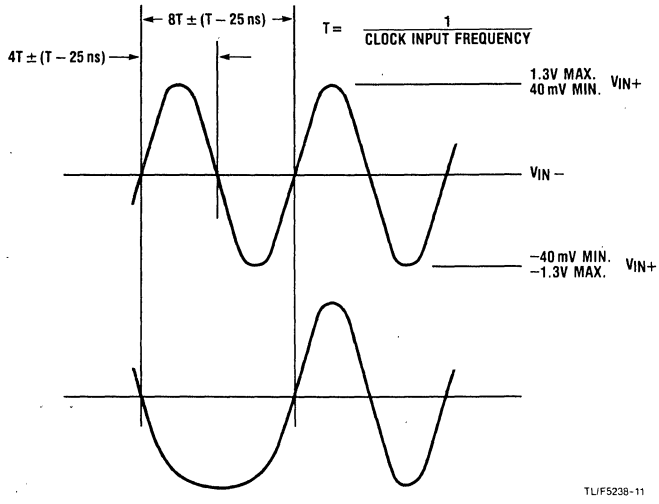


FIGURE 10. Data Waveform Constraints: Amplifier Inputs

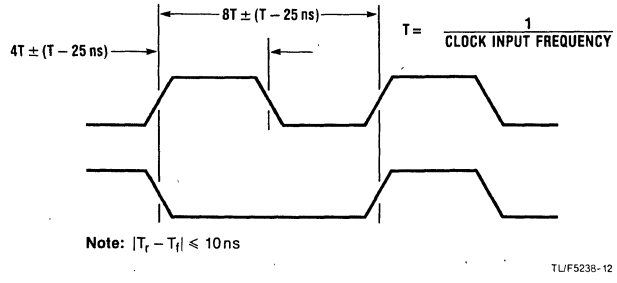
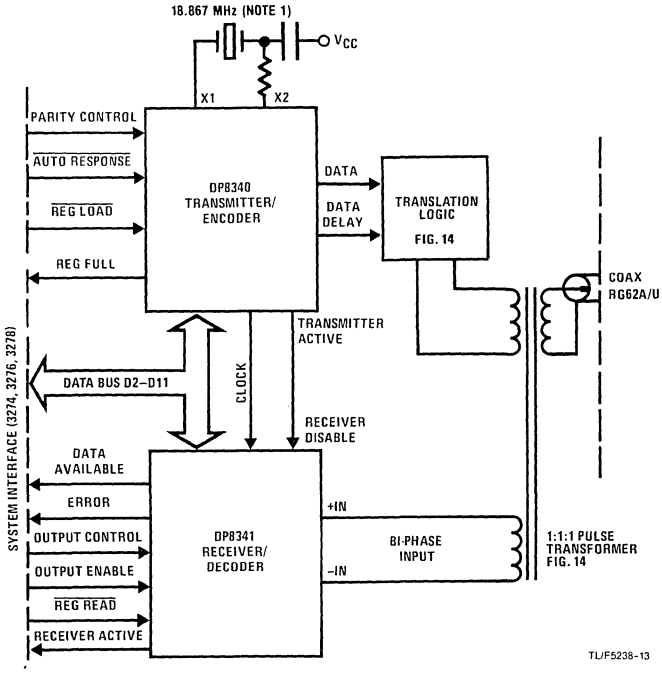


FIGURE 11. Data Waveform Constraints: Data Input (TTL)

Typical Applications



Note 1: Crystal manufacturer Midland Ross Corp.
NEL Unit Part No. NE18A @ 18.867MHz

FIGURE 12. Typical Application for IBM 3270 Interface

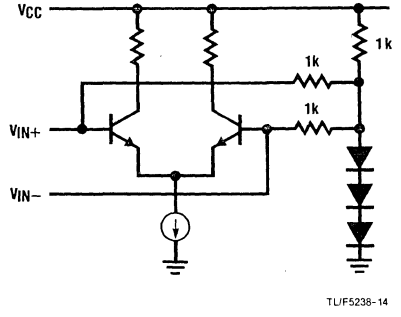
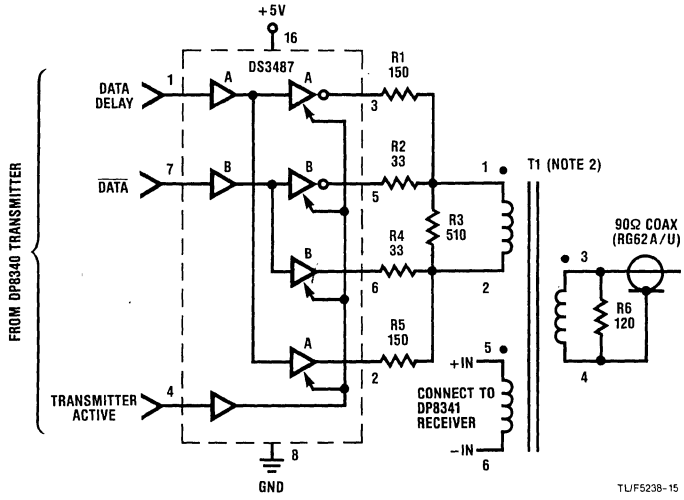


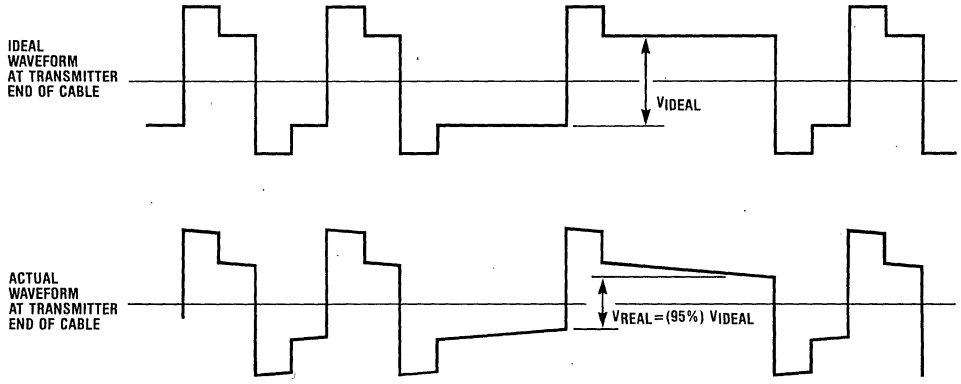
FIGURE 13. Equivalent Circuit for DP8341 Input Amplifier

Typical Applications (Continued)



Notes: 1) Resistance values are in ohms, ±5%, ¼W
2) T1 is a 1:1:1 pulse transformer, $L_{MIN} = 500\mu H$ for 18MHz system clock
Pulse Engineering Part No. 5762
Technitrol Part No. 11LHA or equivalent transformers

FIGURE 14. Translation Logic



* TO MAINTAIN LOSS AT 95% OF IDEAL SIGNAL, SELECT TRANSFORMER INDUCTANCE SUCH THAT:

$$L(MIN) = \frac{10{,}000}{f_{CLK}}$$

f_{CLK} = SYSTEM CLOCK FREQUENCY (e.g., 18.87MHz)

EXAMPLE:

$$L = \frac{10{,}000}{18.87 \times 10^6} \longrightarrow L(MIN) = 530\mu H$$

Notes: 1) Less inductance will cause greater amplitude attenuation
2) Greater inductance may decrease signal rise time slightly and increase ringing, but these effects are generally negligible.

TL/F/5238-16

FIGURE 15. Transformer Selection

National Semiconductor

Data Communications Support

DP8342 High-Speed Serial Transmitter/Encoder

General Description

The DP8342 generates a complete encoding of parallel data for high speed serial transmission. It generates a five bit starting sequence, three bit code violation, followed by a syn bit and eight bit per byte of data plus a parity bit. A three-bit ending code signals the termination of the transmission. The DP8342 adapts to generalized high speed serial data transmission as well as the coax lines at a maximum data rate of 3.5 MHz.

The DP8342 and its complementary chip, the DP8343 (receiver/decoder) have been designed to provide maximum flexibility in system designs. The separation of the transmitter/receiver functions provides convenient addition of more receivers at one end of a bi-phase line without the need of unused transmitters. This is specifically advantageous in control units where typical bi-phase data is multiplexed over many bi-phase lines and the number of receivers generally exceeds the number of transmitters.

Features

- Eight bits per data byte transmission
- Single-byte or multi-byte transmission
- Internal parity generation (even or odd)
- Internal crystal controlled oscillator used for the generation of all required chip timing frequencies
- Clock output directly drives receiver (DP8343) clock input
- Input data holding register
- Automatic clear status response feature
- Line drivers at data outputs provide easy interface to bi-phase coax line or general transmission media
- <2ns driver output skew
- Bipolar technology provides TTL input/output compatibility
- Data outputs power up/down glitch free
- Internal power up clear and reset
- Single +5V power supply

Connection Diagram

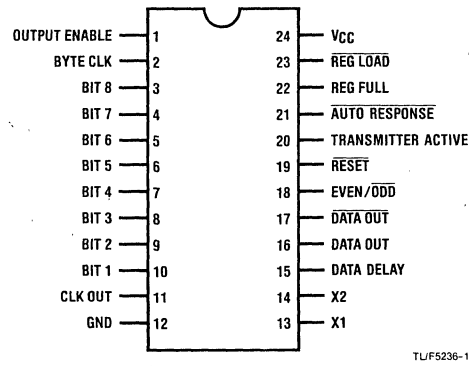


FIGURE 1.

Order Number DP8342J or DP8342N
See NS Package J24A or N24A

Block Diagram

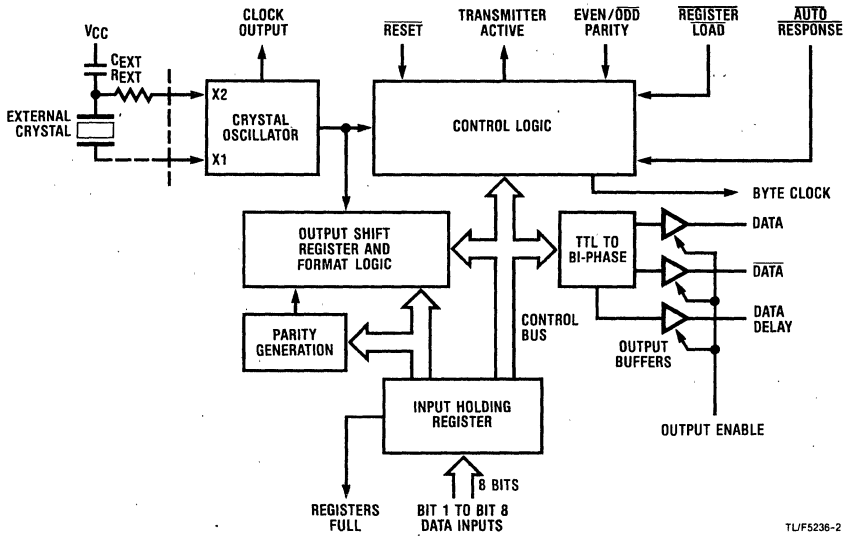


FIGURE 2.

Functional Description

Figure 2 is a block diagram of the DP8342 Bi-Phase Transmitter/Encoder. The transmitter/encoder contains a crystal oscillator whose input is a crystal with a frequency eight (8) times the data rate. A Clock Output is provided to drive the DP8342 receiver/decoder Clock Input and other system components at the oscillator frequency. Additionally, the oscillator drives the control logic and output shift register/format logic blocks.

Data is parallel loaded from the system data bus to the transmitter/encoder's input holding register. This data is in turn loaded by the transmitter/encoder to its output shift register if this register was empty at the time of the load. During this load, message formatting and parity are generated. The formatted message is then shifted out at the bit rate frequency to the TTL to Bi-Phase block which generates the proper data bit formatting. The data outputs, DATA, $\overline{\text{DATA}}$, and DATA DELAY provide for flexible interface to the transmission medium with little or no external components.

The control Logic block interfaces to all blocks to insure proper chip operation and sequencing. It controls the type of parity generation through the Even/$\overline{\text{Odd}}$ Parity input. An additional feature provided by the transmitter/encoder is the Reset and Output-TRI-STATE® capability. Another feature of the DP8342 is the Byte Clock output which keeps track of the number of bytes transferred.

The transmitter/encoder is also capable of internal TT/AR (Transmission Turnaround/Auto Response). When the $\overline{\text{Auto-Response}}$ ($\overline{\text{AR}}$) input is forced to the logic "0" state, the transmitter/encoder responds with clean status (all zeros on data bits).

Operation of the transmitter/encoder is automatic. After the first data byte is loaded, the Transmitter Active output is set and the transmitter/encoder immediately formats the input data and serially shifts it out its data outputs. If the message is a multi-byte message, the internal format logic will modify the message data format for multibyte as long as the next byte is loaded to the input holding format logic will modify the message data format for multibyte as long as the next byte is loaded to the input hlding register before the last data bit of the previous data byte is transferred out of the internal output shift register. After all data is shifted out of the transmitter/encoder the Transmitter Active output will return to the inactive state.

Detailed Pin/Functional Description

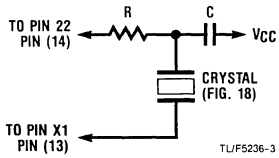
Crystal Inputs X1 and X2

The oscillator is controlled by an external, parallel resonant crystal connected between the X1 and X2 pins. Normally, a fundamental mode crystal is used to determine the operating frequency of the oscillator; however, overtone mode crystals may be used.

Crystal Specifications (Parallel Resonant)

Type	<20 MHz AT-cut or >20 MHz BT-cut
Tolerance	0.005% at 25°C
Stability	0.01% from 0°C to +70°C
Resonance	Fundamental (Parallel)
Maximum Series Resistance	Dependent on Frequency (For 20 MHz, 50Ω)
Load Capacitance	15pF

Connection Diagram



FREQ	R	C
<20 MHz	500Ω	30pF
>20 MHz	120Ω	15pF

If the DP8342 transmitter is clocked by a system clock (crystal oscillator not used), pin 13 (X1 input) should be clocked directly using a Schottky series (74S) circuit. Pin 14 (X2 input) may be left open. The clocking frequency must be set at eight times the data bit rate. Maximum input frequency is 28 MHz.

Clock Output

The Clock Output is a buffered output derived directly from the crystal oscillator block and clocks at the oscillator frequency. It is designed to directly drive the DP8343 receiver/decoder Clock Input as well as other system components.

Registers Full

This output is used as a flag by the external operating system. A logic "1" (active state) on this output indicates that both the internal output shift register and the input holding register contain active data. No additional data should be loaded until this output returns to the logic "0" state (inactive state).

Transmitter Active

This output will be in the logic "1" state while the transmitter/encoder is about to transmit or in the process of transmitting data. Otherwise, it will assume the logic "0" state indicating no data presently in either the input holding or output shift registers.

$\overline{\text{Register Load}}$

The Register Load input is used to load data from the Data Inputs to the input holding register. The loading function is level sensitive, the data present during the logic "0" state of this input is loaded, and the input data must be valid before the logic "0" to logic "1" transition. It is after this transition that the transmitter/encoder begins formatting of data for serial transmission.

$\overline{\text{Auto Response}}$ (TT/AR)

This input provides for automatic clear data transmission (all bits in logic "0") without the need of loading all zero's. When a logic "0" is forced on this input the transmitter/encoder immediately responds with transmission of "clean status". When this input is in the logic "1" state the transmitter/encoder transmits data entered on the Data Inputs.

Even/$\overline{\text{Odd}}$ Parity

This input sets the internal logic of the DP8342 transmitter/encoder to generate either even or odd parity for the data byte in the bit 10 position. When this pin is in the logic "0" state odd parity is generated. In the logic "1" state even parity is generated. This feature is useful when the control unit is performing a loop back check and at the same time the controller wishes to verify proper data transmission with its receiver/decoder.

Serial Outputs — DATA, $\overline{\text{DATA}}$, and DATA DELAY

These three output pins provide for convenient application of data to the Bi-Phase transmission line. The Data outputs are a direct bit representation of the Bi-Phase data while the Data Delay output provides the necessary increment to clearly define the four (4) DC levels of the pulse. The DATA and $\overline{\text{DATA}}$ outputs add flexibility to the DP8342 transmitter/encoder for use in high speed differential line driving applications. The typical DATA to $\overline{\text{DATA}}$ skew is 2ns.

$\overline{\text{RESET}}$

When a logic "0" is forced on this input, all outputs except Clock Output are latched low.

Output Enable

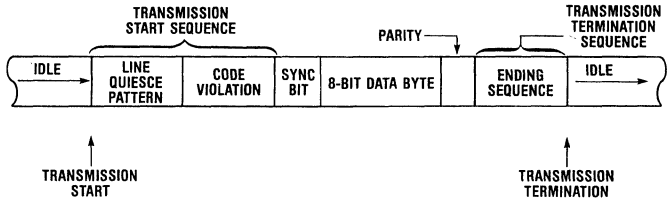
When a logic "0" is forced on this input the three serial data outputs are in the high impedance state.

Byte Clock

This pin registers a pulse at the end of each byte transmission. The number of pulses registered corresponds to the number of bytes transmitted.

Message Format

Single Byte Transmission



Multi-Byte Transmission

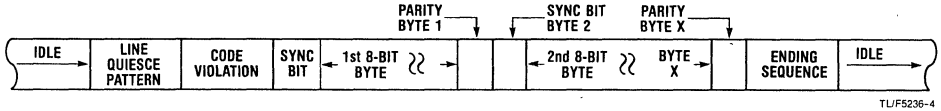


FIGURE 3.

Functional Timing Waveforms

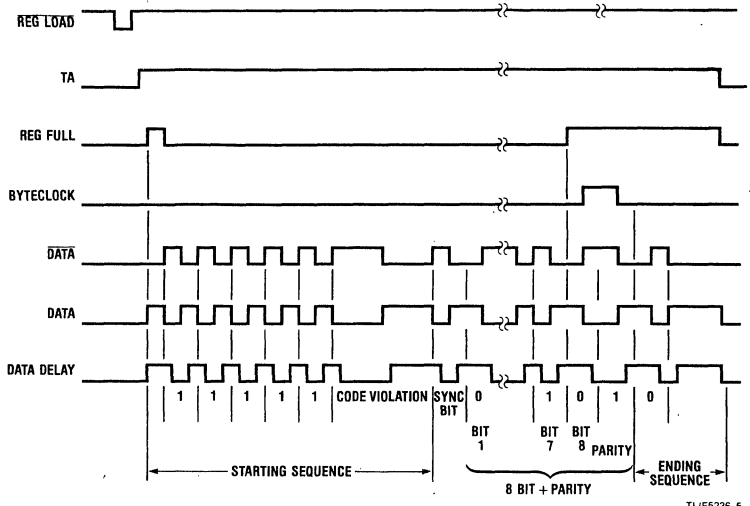


FIGURE 4. Overall Timing Waveforms for Single Byte

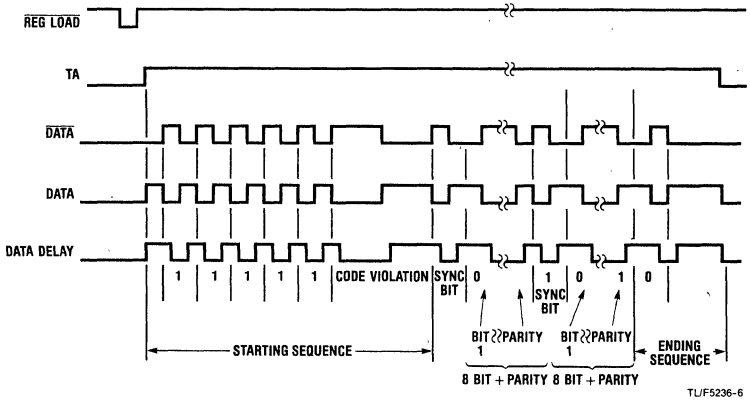


FIGURE 5. Overall Timing Waveforms for Multi-Byte

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Input Voltage	5.5V
Output Voltage	5.25V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	2237 mW
Molded Package	2500 mW

*Derate cavity package 14.9 mW/°C above 25°C; derate molded package 20 mW/°C above 25°C.

Operating Conditions

	Min.	Max.	Units
Supply Voltage, (V_{CC})	4.75	5.25	V
Ambient Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage (All Inputs Except X1 and X2)	$V_{CC} = 5V$	2.0			V
V_{IL}	Logic "0" Input Voltage (All Inputs Except X1 and X2)	$V_{CC} = 5V$			0.8	V
V_{CLAMP}	Input Clamp Voltage (All Inputs Except X1 and X2)	$I_{IN} = -12\,mA$		−0.8	−1.2	V
I_{IH}	Logic "1" Input Current Register Load Input	$V_{CC} = 5.25V$, $V_{IN} = 5.25V$		0.3	120	μA
	All Others Except X1 and X2			0.1	40	μA
I_{IL}	Logic "0" Input Current Register Load Input	$V_{CC} = 5.25V$, $V_{IN} = 0.5V$		−15	−300	μA
	All Inputs Except X1 and X2			−5	−100	μA
V_{OH1}	Logic "1" All Outputs Except CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY	$I_{OH} = -100\,\mu A$, $V_{CC} = 4.75V$	3.2	3.9		V
		$I_{OH} = -1\,mA$	2.5	3.4		V
V_{OH2}	Logic "1" for CKL OUT, DATA, $\overline{DATA}$ and DATA DELAY Outputs	$V_{CC} = 4.75V$, $I_{OH} = -10\,mA$	2.6	3.0		V
V_{OL1}	Logic "0" All Outputs Except CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY	$V_{CC} = 4.75V$, $I_{OL} = 5\,mA$		0.35	0.5	V
V_{OL2}	Logic "0" for CLK OUT, DATA, $\overline{DATA}$ and DATA DELAY Outputs	$V_{CC} = 4.75V$, $I_{OL} = 20\,mA$		0.4	0.6	V
I_{OS1}	Output Short Circuit Current for All Except CLK OUT, DATA, $\overline{DATA}$, and DATA DELAY Outputs	Note 5, $V_{OUT} = 0V$	−10	−30	−100	mA
I_{OS2}	Output Short Circuit Current DATA, $\overline{DATA}$, and DATA DELAY Outputs	Note 5, $V_{OUT} = 0V$	−50	−140	−250	mA
I_{OS3}	Output Short Circuit Current for CLK OUT	Note 5, $V_{OUT} = 0V$	−30	−90	−200	mA
I_{CC}	Power Supply Current	$V_{CC} = 5.25V$		170	250	mA

Timing Characteristics $V_{CC} = 5V \pm 5\%$, $T_A = 0°C$ to 70°C, Oscillator Frequency = 28 MHz (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	$\overline{REG\ LOAD}$ to Transmitter Active (T_A) Positive Edge	Load Circuit 1 Figure 6		60	90	ns
t_{pd2}	$\overline{REG\ LOAD}$ to Register Full; Positive Edge	Load Circuit 1 Figure 6		45	75	ns
t_{pd3}	T_A to Register Full; Negative Edge	Load Circuit 1 Figure 6		40	70	ns
t_{pd4}	Positive Edge of $\overline{REG\ LOAD}$ to Positive Edge of DATA	Load Circuit 2 Figure 9		50	80	ns
t_{pd5}	$\overline{REG\ LOAD}$ to $\overline{DATA}$; Positive Edge	Load Circuit 2 Figure 9		280	380	ns
t_{pd6}	$\overline{REG\ LOAD}$ to DATA DELAY; Positive Edge	Load Circuit 2 Figure 9		150	240	ns
t_{pd7}	Positive Edge of $\overline{DATA}$ to Negative Edge of DATA DELAY	Load Circuit 2 Figure 9		70	85	ns

Timing Characteristics (Continued) Oscillator Frequency = 28MHz (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd8}	Positive Edge of DATA DELAY to Negative Edge of $\overline{DATA}$	Load Circuit 2 Figure 9		80	95	ns
t_{pd9}, t_{pd10})	Skew between DATA and $\overline{DATA}$	Load Circuit 2 Figure 9		2	6	ns
t_{pd11}	Negative Edge of $\overline{Auto\ Response}$ ($\overline{AR}$) to Positive Edge of TA	Load Circuit 1 Figure 10		70	100	ns
t_{pd12}	Maximum Time Delay to Load Second Byte After Positive Edge of REG FULL	Load Circuit 1 Figure 8, Note 7			4×T−50	ns
t_{pd13}	X1 to CLK OUT; Positive Edge	Load Circuit 2 Figure 11		21	30	ns
t_{pd14}	X1 to CLK OUT; Negative Edge	Load Circuit 2 Figure 11		23	33	ns
t_{pd15}	Negative Edge of $\overline{AR}$ to Positive Edge of REG FULL	Load Circuit 1 Figure 10		45	75	ns
t_{pd16}	Skew between TA and REG FULL during $\overline{Auto\ Response}$	Load Circuit 1 Figure 10		50	80	ns
t_{pd17}	$\overline{REG\ LOAD}$ to REG FULL; Positive Edge for Second Byte	Load Circuit 1 Figure 7		45	75	ns
t_{pd18}	REG FULL to BYTE CLK; Negative Edge	Load Circuit 1 Figure 7		60	90	ns
t_{pd19}	REG FULL to BYTE CLK; Positive Edge	Load Circuit 1 Figure 7		145	180	ns
t_{ZH}	Output Enable to DATA, $\overline{DATA}$, or DATA Delay outputs: HiZ to High	CL = 50pF Figures 17, 17		25	45	ns
t_{ZL}	Output Enable to DATA, $\overline{DATA}$, OR DATA Delay Outputs; HiZ to High	CL = 50pF Figures 16, 17		15	30	ns
t_{HZ}	Output Enable to DATA, $\overline{DATA}$, or DATA Delay Outputs; High to HiZ	CL = 15pF Figures 16, 17		65	100	ns
t_{LZ}	Output Enable to DATA, $\overline{DATA}$, or DATA Delay Outputs; Low to HiZ	CL = 15pF Figures 16, 17		45	70	ns
t_{pw1}	$\overline{REG\ LOAD}$ Pulse Width	Figure 12	40			ns
t_{pw2}	First REG FULL Pulse Width (Note 6)	Load Circuit 1 Figure 7, Note 7		8×T+60	8×T+100	ns
t_{pw3}	REG FULL Pulse Width Prior to Ending Sequence (Note 6)	Load Circuit 1 Figure 7		5×B		ns
t_{pw4}	Pulse Width for $\overline{Auto\ Response}$	Figure 10	40			ns
t_{pw5}	Pulse Width for BYTE CLK	Load Circuit 1 Figure 7, Note 7		8×T+30	8×T+80	ns
t_s	Data Setup Time prior to $\overline{REG\ LOAD}$ Positive Edge. Hold Time = 0ns	Figure 12		15	23	ns
t_{r1}	Rise Time for DATA, $\overline{DATA}$, and DATA DELAY Output Waveform	Load Circuit 2, Figure 13		7	13	ns
t_{f1}	Fall Time for DATA, $\overline{DATA}$, and DATA DELAY Output Waveform	Load Circuit 2, Figure 13		5	11	ns
t_{r2}	Rise Time for TA and REG FULL	Load Circuit 1 Figure 14		20	30	ns
t_{f2}	Fall Time for TA and REG FULL	Load Circuit 1 Figure 14		15	25	ns
f_{MAX}	Data Rate Frequency (Clock Input must be 8X this Frequency)		DC		3.5	Mbits/s
C_{IN}	Input Capacitance — Any Input	Note 4		5	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.
Note 2: Unless otherwise specified, min./max. limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.
Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max. or min. are so classified on absolute basis.
Note 4: Input capacitance is guaranteed by periodic testing. $f_{TEST} = 10kHz$ at 300mV, $T_A = 25°C$.
Note 5: Only one output should be shorted at a time.
Note 6: T = 1/(Oscillator Frequency). Unit for T should be in ns. B = 8T.
Note 7: Oscillator Frequency Dependent.

Timing Waveforms (Continued)

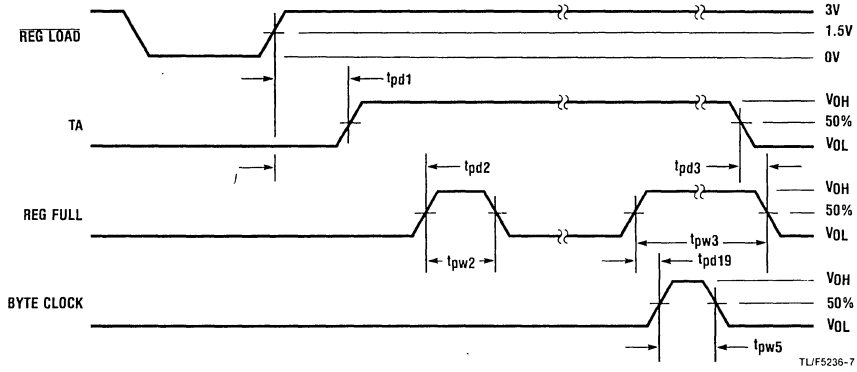


FIGURE 6. Single Byte Transfer

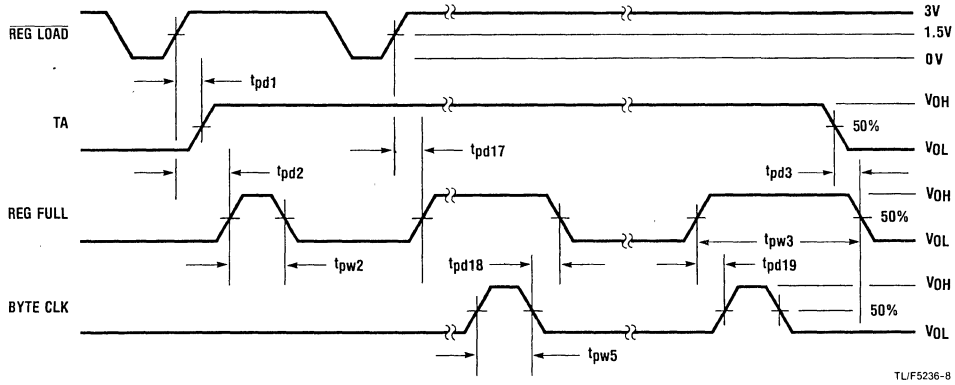


FIGURE 7. Two-Byte Transfer

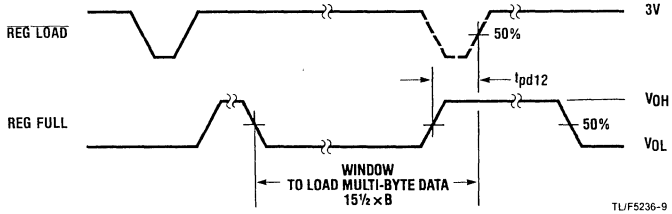


FIGURE 8. Maximum Window to Load Multi-Byte Data

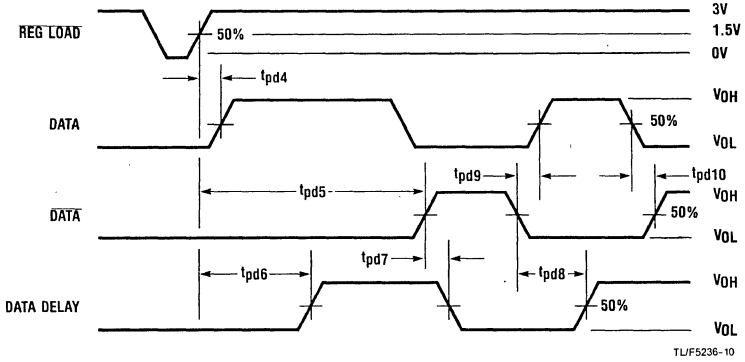


FIGURE 9. Three Serial Outputs

Timing Waveforms (Continued)

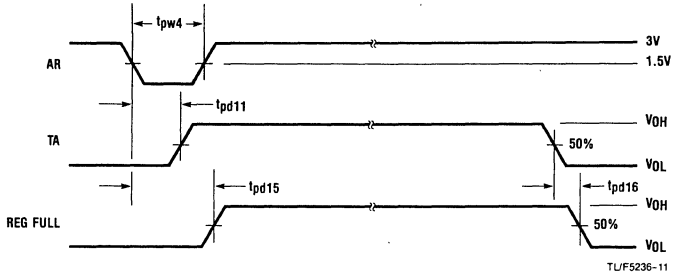


FIGURE 10. $\overline{\text{Auto-Response}}$

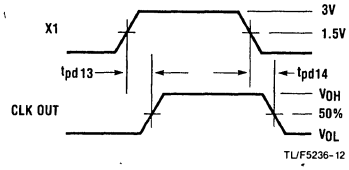


FIGURE 11. Clock Pulse

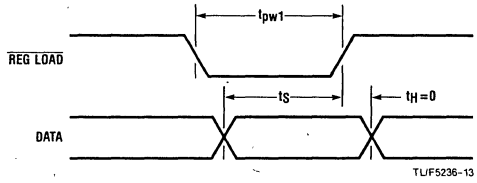


FIGURE 12. $\overline{\text{REG LOAD}}$

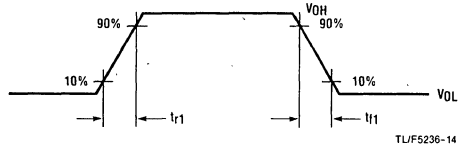


FIGURE 13. Output Waveform for DATA, $\overline{\text{DATA}}$, DATA DELAY (Load Circuit 2)

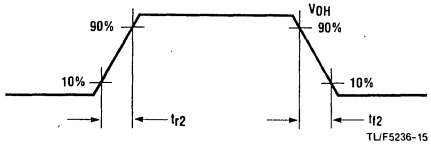
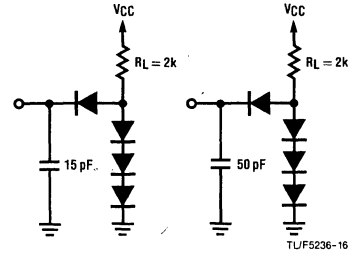


FIGURE 14. Rise and Fall Time Measurement for TA and REG FULL



Load Circuit 1 Load Circuit 2

FIGURE 15. Test Load Circuits

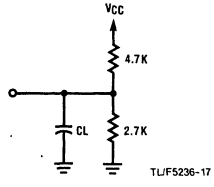


FIGURE 16. Load Circuit for Output TRI-STATE Test

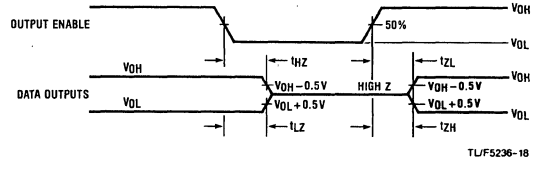


FIGURE 17. TRI-STATE Test

Typical Applications

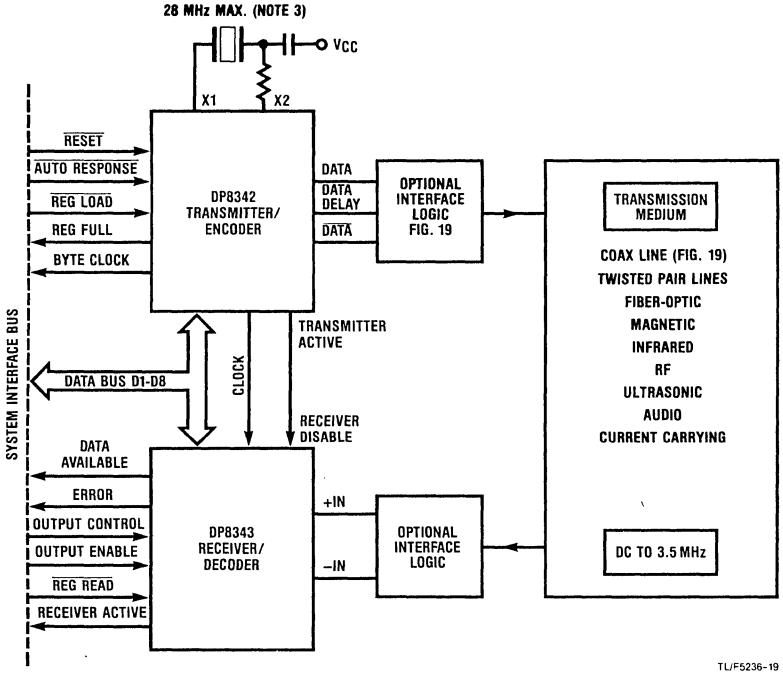
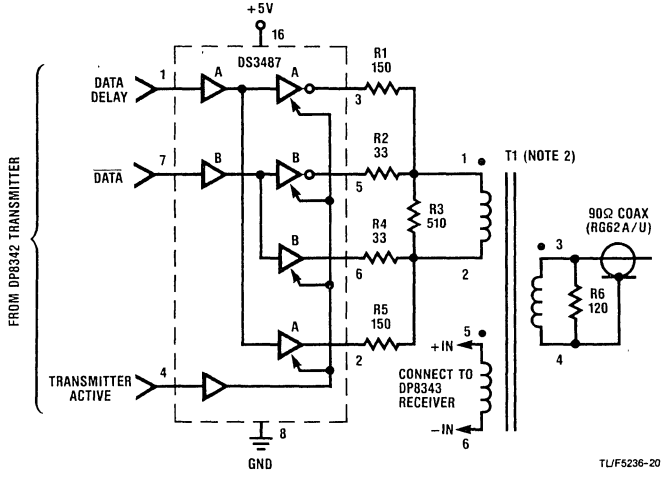
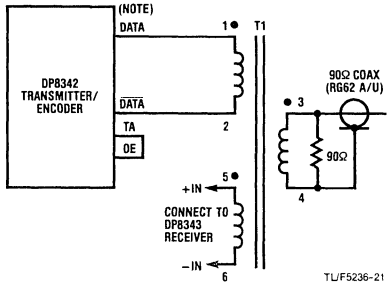


FIGURE 18.



Notes: 1) Resistance values are in ohms, ±5%, ¼W
2) T1 is a 1:1:1 pulse transformer, L = 500μH for 18 to 28MHz system clock.
Pulse Engineering Part No. 5762
Technitrol Part No. 11LHA or equivalent transformer
3) Crystal manufacturer Midland Ross Corp. NEL Unit Part No. NE-18A @ 28MHz.

FIGURE 19. Interface Logic for a Coax Transmission Line



Note: Data rates up to 3.5Mbits/s at 5000ft still apply.

FIGURE 20. Direct Interface for a Coax Transmission Line (Non-IBM Voltage Levels)

National Semiconductor

Data Communications Support

DP8343 High-Speed Serial Receiver/Decoder

General Description

The DP8343 provides complete decoding of data for high speed serial data communications. In specific, the DP8343 receiver recognizes Bi-Phase serial data sent from its complementary chip, the DP8342 transmitter, and converts it into eight (8) bits of parallel data. These devices are easily adapted to generalized high speed serial data transmission systems that operate at bit rates up to 3.5 MHz.

The DP8343 receiver and the DP8342 transmitter are designed to provide maximum flexibility in system designs. The separation of transmitter and receiver functions allows addition of more receivers at one end of the Bi-Phase line without the necessity of adding unused transmitters. This is advantageous in control units where the data is typically multiplexed over many lines and the number of receivers generally exceeds the number of transmitters. The separation of transmitter and receiver function provides an additional advantage in flexibility of data bus organization. The data bus outputs of the receiver are TRI-STATE®, thus enabling the bus configuration to be organized as either a common transmit/receive (bi-directional) bus or as separate transmit and receive busses for higher speed.

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Features

- DP8343 receives eight (8) bit data bytes
- Separate receiver and transmitter provide maximum system design flexibility
- Even parity detection
- High sensitivity input on receiver easily interfaces to coax line
- Standard TTL data input on receiver provides generalized transmission line interface and also provides hysteresis
- Data holding register
- Multi-byte or single byte transfers
- TRI-STATE receiver date outputs provide flexibility for common or separated transmit/receive data bus operation
- Data transmission error detection on receiver provides for both error detection and error type definition
- Bipolar technology provides TTL input/output compatibility with excellent drive characteristics
- Single +5V power supply operation

Connection Diagram

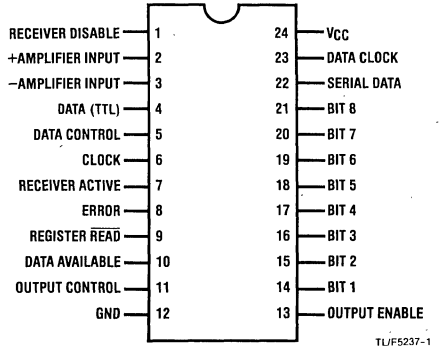


FIGURE 1.

Order Number DP8343J or DP8343N
See NS Package J24A or N24A

Block Diagram

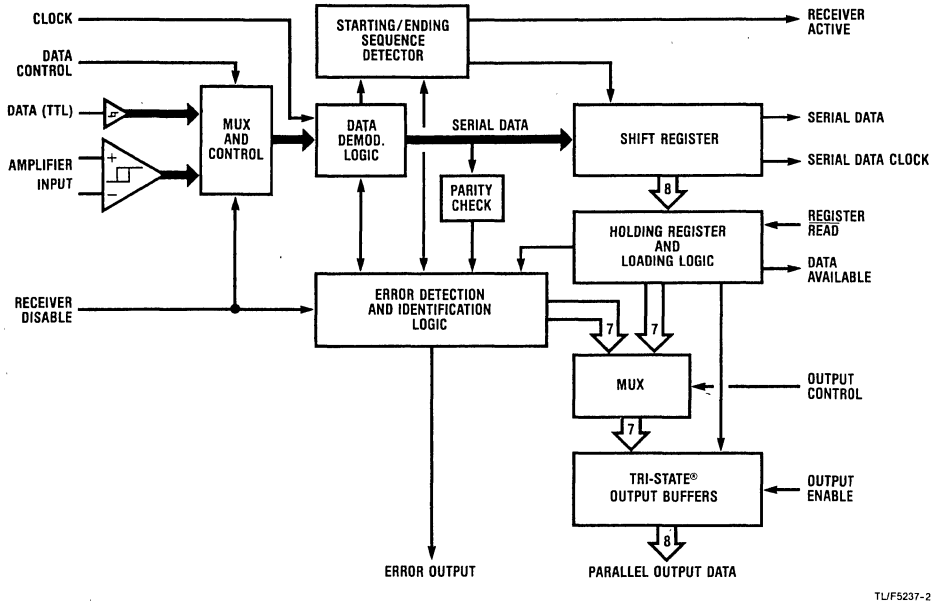


FIGURE 2. DP8343 Bi-Phase Receiver

Block Diagram Functional Description

Figure 2 is a block diagram of the DP8343 receiver. This chip is essentially a serial in/parallel out shift register. However, the serial input data must conform to a very specific format (see *Figures 3-6*). The message will not be recognized unless the format of the starting sequence is correct. Deviations from the format in the data, sync bit, parity or ending sequence will cause an error to be detected, terminating the message.

Data enters the receiver through the differential input amplifier or the TTL Data input. The differential amplifier is a high sensitivity input which may be used by connecting it directly to a transformer coupled coax line, or other transmission medium. The TTL Data input provides 400 mV of hysteresis and recognizes TTL logic levels. The data then enters the demodulation block.

The data demodulation block samples the data at eight (8) times the data rate and provides signals for detecting the starting sequence, ending sequence, and errors. Detection of the starting sequence sets the Receiver Active output high and enables the input shift register.

As the eight bits of data are shifted into the shift register, the receiver will verify that even parity is maintained on the data bits and the sync bit. Serial Data and Serial Data Clock, the inputs to the shift register, are provided for use with external error detecting schemes. After one complete data byte is received, the contents of the input shift register is parallel loaded to the holding register, assuming the holding register is empty, and the Data Available output is set. If the holding register is full, this load will be delayed until that register has been read or the start of another data byte is received, in which case a Data Overflow Error will be detected, terminating the message. Data is read from the holding register through the TRI-STATE Output Buffers. The Output Enable input is the TRI-STATE control for these outputs and the Register Read input signals the receiver that the read has been completed.

When the receiver detects an ending sequence the Receiver Active output will be reset to a logic "0" indicating the message has been terminated. A message will also terminate when an error is detected. The Receiver Active output used in conjunction with the Error output allows quick response to the transmitting unit when an error free message has been received.

The Error Detection and Identification block insures that valid data reaches the outputs of the receiver. Detection of an error sets the Error output to a logic "1" and resets the Receiver Active output to a logic "0" terminating the message. The error type may be read from the data bus outputs by setting the Output Control input to logic "0" and enabling the TRI-STATE outputs. The data bit outputs have assigned error definitions (see error code definition table). The Error output will return to a logic "0" when the next starting sequence is received, or when the error is read (Output Control to logic "0" and a Register Read performed).

The Receiver Disable input is used to disable both the amplifier and TTL Data receiver inputs. It will typically be connected directly to the Transmitter Active output of the DP8342 transmitter circuit.

Detailed Functional Pin Description

Receiver Disable

This input is used to disable the receiver's data inputs. The Receiver Disable input will typically be connected to the Transmitter Active output of the DP8342. However, at the system controller it may be necessary for both the transmitter and receiver to be active at the same time. This variation can be accomplished with the addition of minimal external logic.

Truth Table

Receiver Disable	Data Inputs
Logic "0"	Active
Logic "1"	Disabled

Amplifier Inputs

The receiver has a differential input amplifier which may be directly connected to the transformer coupled coax line. The amplifier may also be connected to a differential type TTL line. The amplifier has 20mV of hysteresis.

Data Input

This input can be used either as an alternate data input or as a power-up check input. If the system designer prefers to use his own amplifier, instead of the one provided on the receiver, then this TTL input may be used. Using this pin as an alternate data input allows self-test of the peripheral system without disturbing the transmission line.

Data Control

This input is the control pin that selects which of the inputs are used for data entry to the receiver.

Truth Table

Data Control	Data Input To
Logic "0"	Data Input
Logic "1"	Amplifier Inputs

Note: This input is also used for testing. When the input voltage is raised to 7.5V the chip resets.

Clock Input

This input is the internal clock of the receiver. It must be set at eight (8) times the line data bit rate. The crystal-controlled oscillator provided in the DP8342 transmitter also operates at this frequency. The Clock Output of the transmitter is designed to directly drive the receiver's Clock Input. In addition, the receiver is designed to operate correctly to a data bit rate of 3.5MHz.

Receiver Active

The purpose of this output is to inform the external system when the DP8343 is in the process of receiving a message. This output will transition to a logic "1" state after a receipt of a valid starting sequence and transition to logic "0" when a valid ending sequence is received or an error is detected. This output combined with the Error output will inform the operating system of the end of an error free data transmission.

Error

The Error output transitions to a logic "1" when an error is detected. Detection of an error causes the Receiver Active and the Data Available outputs to transition to a logic "0". The Error output returns to a logic "0" after the error register has been read or when the next starting sequence is detected.

Register Read

The Register Read input when driven to the logic "0" state signals the receiver that data in the holding register is being read by the external operating system. The data present in the holding register will continue to remain valid until the Register Read input returns to the logic "1" condition. At this time, if an additional byte is present in the input shift register it will be transferred to the holding register, otherwise the data will remain valid in the holding register. The Data Available output will be in the logic "0" state for a short interval while a new byte is transferred to the holding register after a register read.

Data Available

This output indicates the existence of a data byte within the output holding register. It may also indicate the presence of a data byte in both the holding register and the input shift register. This output will transition to the logic "1" state as soon as data is available and return to the logic "0" state after each data byte has been read. However, even after the last data byte has been read and the Data Available output has assumed the logic "0" state, the last data byte read from the holding register will remain until new data has been received.

Output Control

The Output Control input determines the type of information appearing at the data outputs. In the logic "1" state data will appear, in the logic "0" state error codes are present.

Truth Table

Output Control	Data Outputs
Logic "0"	Error Codes
Logic "1"	Data

Output Enable

The Output Enable input controls the state of the TRI-STATE Data outputs.

Truth Table

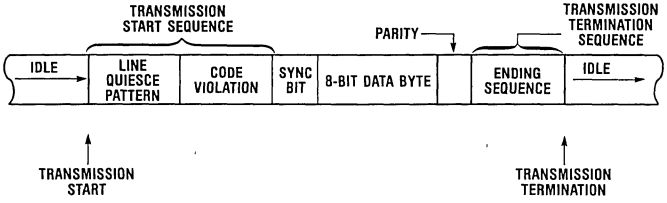
Output Enable	TRI-STATE Data Outputs
Logic "0"	Disabled
Logic "1"	Active

Data Outputs

The DP8343 has an eight (8) bit TRI-STATE data bus. Seven bits are multiplexed with error bits. The error bits are defined in the table below. The Output Control input is the multiplexer control for the Data/Error bits.

Message Format

Single Byte Transmission



Multi-Byte Transmission

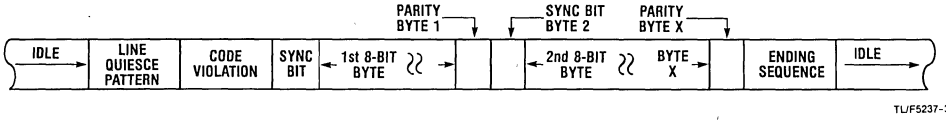


FIGURE 3.

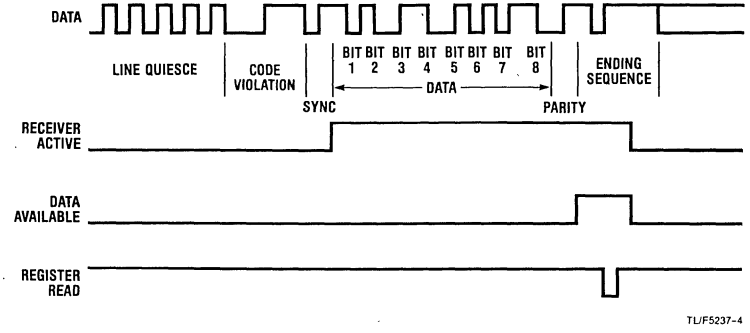


FIGURE 4A. Single Byte (8-Bit) Message

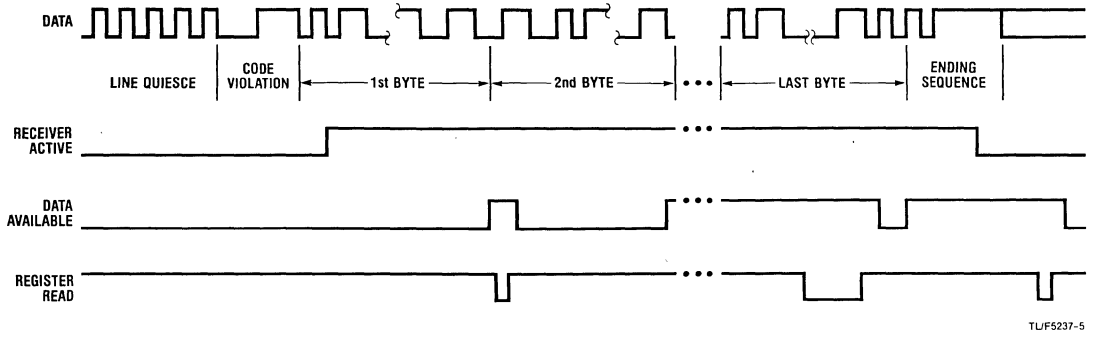


FIGURE 4B. Multi-Byte Message

Error Code Definition

Data Bit DP8343	Error Type
Bit 1	Data Overflow (Byte not removed from holding register when it and the input shift register are both full and new data is received)
Bit 2	Parity Error (Odd parity detected)
Bit 3	Transmit Check conditions (existence of errors on any or all of the following data bits: Bit 2, Bit 4, and Bit 5)
Bit 4	An invalid ending sequence
Bit 5	Loss of mid-bit transition detected at other than normal ending sequence time
Bit 6	New starting sequence detected before data byte in holding register has been read
Bit 7	Receiver disabled during receiver active mode

Serial Data

The Serial Data output is the serial data coming into the input shift register.

Data Clock

The Data Clock output is the clock to the input shift register.

Message Format (Continued)

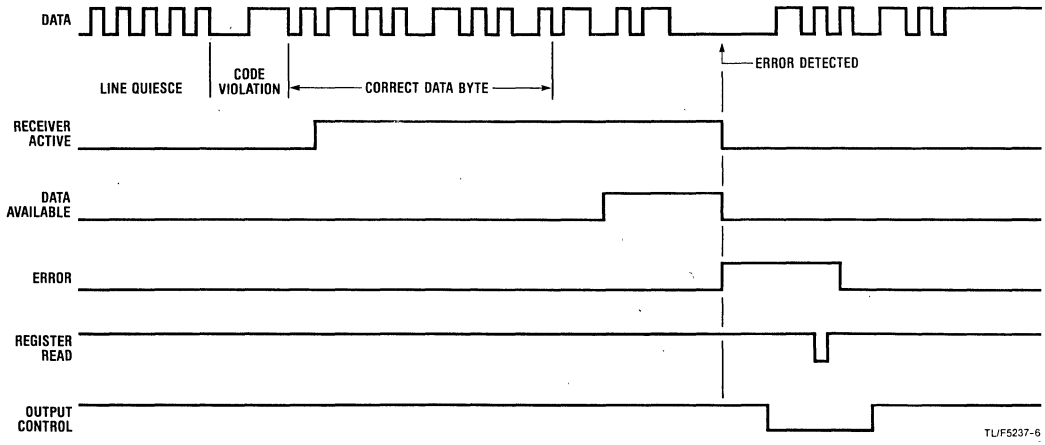


FIGURE 5. Message with Error

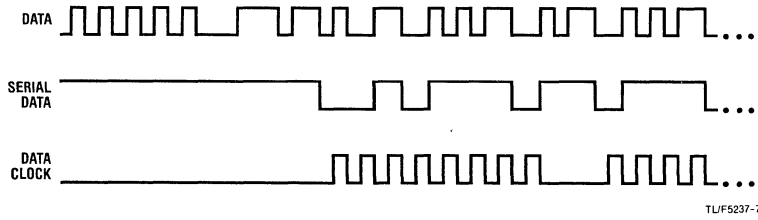


FIGURE 6. Data Clock and Serial Data

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.25V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 seconds)	300°C
Maximum Power Dissipation* at 25°C	
Cavity Package	2040 mW
Molded Package	2237 mW

* Derate cavity package 13.6 mW/°C above 25°C; derate molded package 17.9 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage, (V_{CC})	4.75	5.25	V
Ambient Temperature, T_A	0	+70	°C

Electrical Characteristics (Notes 2, 3, and 5)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input High Level		2.0			V
V_{IL}	Input Low Level				0.8	V
$V_{IH}-V_{IL}$	Data Input Hysteresis (TTL, Pin 4)		0.2	0.4		V
V_{CLAMP}	Input Clamp Voltage	$I_{IN} = -12mA$		−0.8	−1.2	V
I_{IH}	Logic "1" Input Current	$V_{CC} = 5.25V$, $V_{IN} = 5.25V$		2	40	μA
I_{IL}	Logic "0" Input Current	$V_{CC} = 5.25V$, $V_{IN} = 0.5V$		−20	−250	μA
V_{OH}	Logic "1" Output Voltage	$I_{OH} = -100\mu A$	3.2	3.9		V
		$I_{OH} = -1mA$	2.5	3.2		V
V_{OL}	Logic "0" Output Voltage	$I_{OL} = 5mA$		0.35	0.5	V
I_{OS}	Output Short Circuit Current	$V_{CC} = 5V$, $V_{OUT} = 0V$ (See Note 4)	−10	−20	−100	mA
I_{OZ}	TRI-STATE® Output Current	$V_{CC} = 5.25V$, $V_O = 2.5V$	−40	1	+40	μA
		$V_{CC} = 5.25V$, $V_O = 0.5V$	−40	−5	+40	μA
A_{HYS}	Amplifier Input Hysteresis		5	20	30	mV
I_{CC}	Power Supply Current	$V_{CC} = 5.25V$		160	250	mA

Timing Characteristics (Notes 2, 6, 7, and 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{D1}	Output Data to Data Available Positive Edge		5	20	40	ns
T_{D2}	Register Read Positive Edge to Data Available Negative Edge		10	25	45	ns
T_{D3}	Error Positive Edge to Data Available Negative Edge		10	30	50	ns
T_{D4}	Error Positive Edge to Receiver Active Negative Edge		5	20	40	ns
T_{D5}	Register Read Positive Edge to Error Negative Edge		20	45	75	ns
T_{D6}	Delay from Output Control to Error Bits from Data Bits		5	20	50	ns
T_{D7}	Delay from Output Control to Data Bits from Error Bits		5	20	50	ns
T_{D8}	First Sync Bit Positive Edge to Receiver Active Positive Edge			3.5*T +70		ns
T_{D9}	Receiver Active Positive Edge to First Data Available Positive Edge			76*T		ns
T_{D10}	Negative Edge of Ending Sequence to Receiver Active Negative Edge			11.5*T +50		ns
T_{D11}	Data Control Set-up Multiplexer Time Prior to Receiving Data through Selected Input		40	30		ns
T_{D12}	Serial Data Set-Up Prior to Data Clock Positive Edge			3*T		ns

Timing Characteristics (Continued) (Notes 2, 6, 7, and 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{PW1}	Register Read (Data) Pulse Width		40	30		ns
T_{PW2}	Register Read (Error) Pulse Width		40	30		ns
T_{PW3}	Data Available Logic "0" State between Data Bytes		25	45		ns
T_S	Output Control Set-up Time Prior to Register Read Negative Edge		0	−5		ns
T_H	Output Control Hold Time After the Register Read Positive Edge		0	−5		ns
T_{ZE}	Delay from Output Enable to Logic "1" or Logic "0" from High Impedance State	Load Circuit 2		25	35	ns
T_{EZ}	Delay from Output Enable to High Impedance State from Logic "1" or Logic "0"	Load Circuit 2		25	35	ns
F_{MAX}	Data Bit Frequency (Clock Input must be 8× the Data Bit Frequency)		DC		3.5	MBits/s

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min./max. limits apply across the 0°C to +70°C temperature range and the 4.75V to 5.25V power supply range. All typical values are for $T_A = 25°C$ and $V_{CC} = 5.0V$.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max. or min. are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

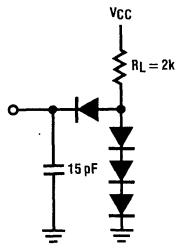
Note 5: Input characteristics do not apply to amplifier inputs (pins 2 & 3).

Note 6: Unless otherwise specified, all AC measurements are referenced to the 1.5V level of the input to the 1.5V level of the output and load circuit 1 is used.

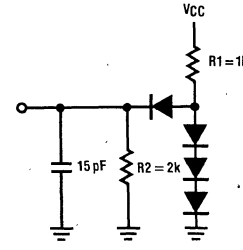
Note 7: AC tests are done with input pulses supplied by generators having the following characteristics: $Z_{OUT} = 50\Omega$, $T_r \leq 5ns$, and $T_f \leq 5ns$.

Note 8: T = 1/ (clock input frequency), units for "T" should be ns.

Test Load Circuits



Load Circuit 1



Load Circuit 2

TL/F5237-8

FIGURE 7.

Timing Waveforms

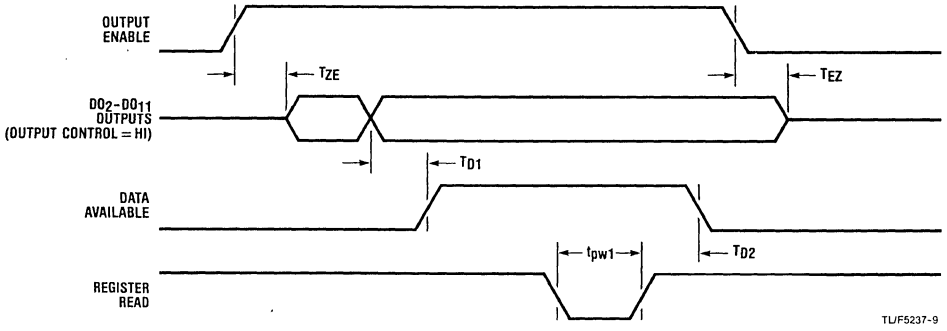


FIGURE 8. Data Sequence Timing

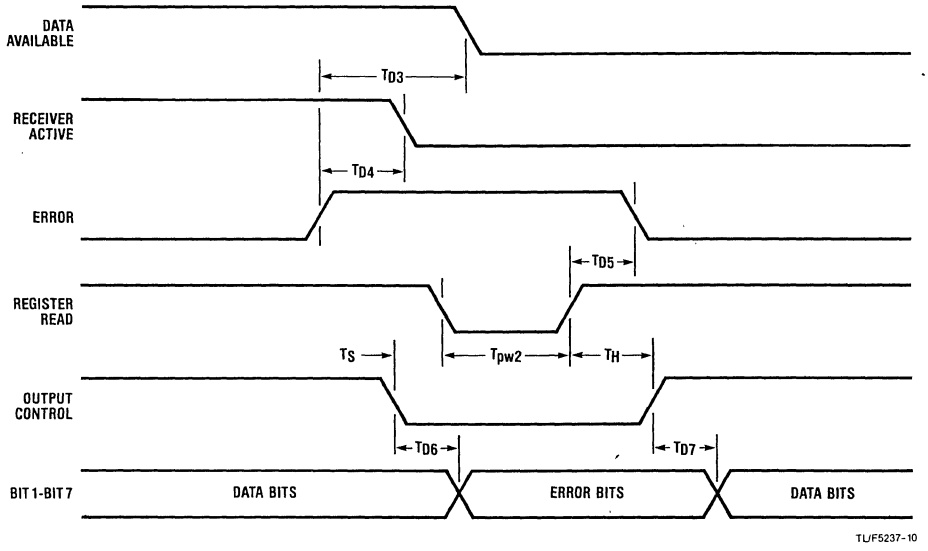


FIGURE 9. Error Sequence Timing

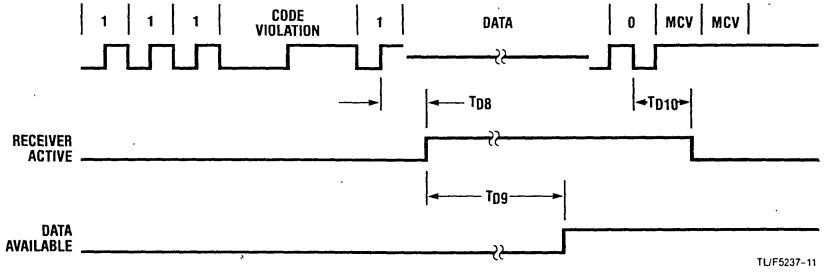
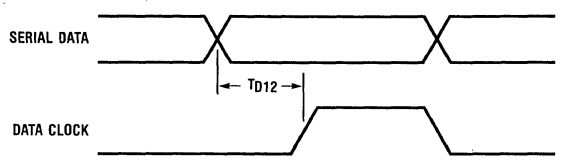
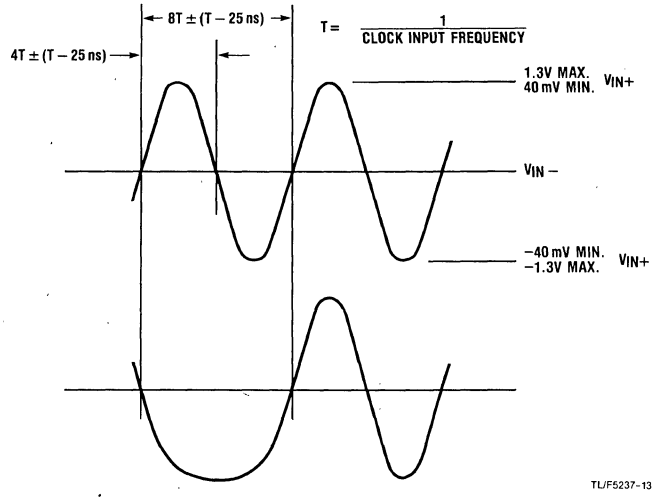


FIGURE 10. Message Timing



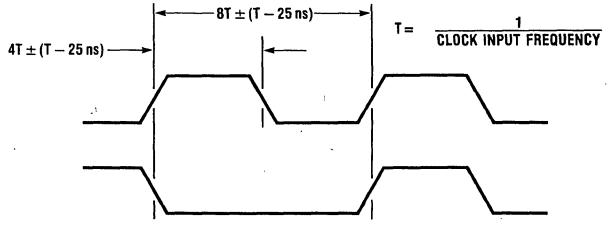
TL/F5237-12

FIGURE 11. Data Clock and Serial Data Timing



TL/F5237-13

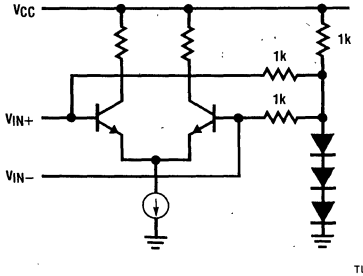
FIGURE 12. Data Waveform Constraints: Amplifier Inputs



Note: $|T_r - T_f| \leq 10$ ns

TL/F5237-14

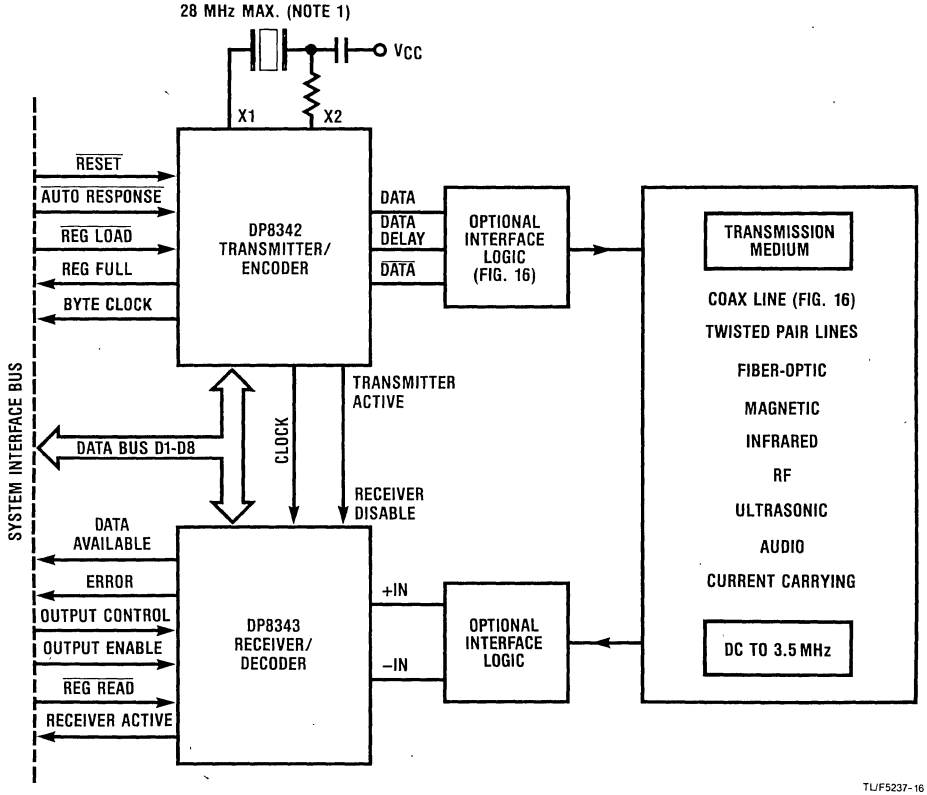
FIGURE 13. Data Waveform Constraints: Data Input (TTL)



TL/F5237-15

FIGURE 14. Equivalent Circuit for DP8343 Input Amplifier

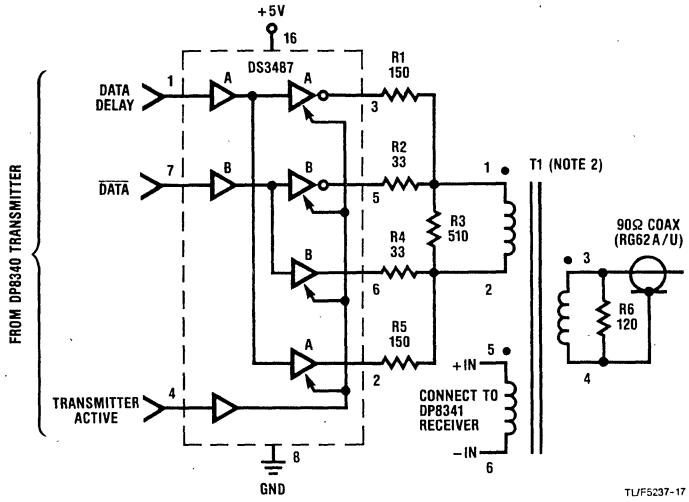
Typical Applications



Note 1: Crystal manufacturer Midland Ross Corp., NEL Unit Part No. NE-18A @ 28MHz

FIGURE 15.

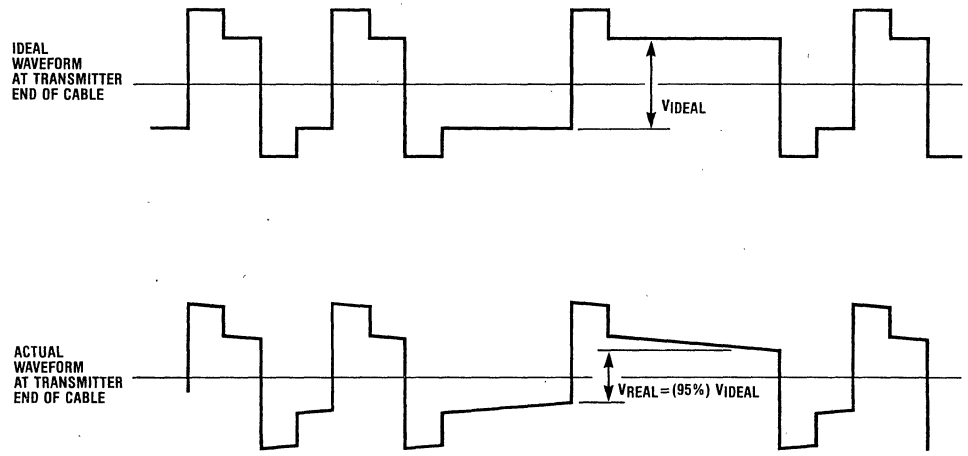
Typical Applications (Continued)



Notes: 1) Resistance values are in ohms, ±5%, ¼W.

2) T1 is a 1:1:1 pulse transformer, $L_{MIN} = 500\mu H$ for 18 MHz system clock.
Pulse Engineering Part No. 5762
Technitrol Part No. 11LHA or equivalent transformers.

FIGURE 16. Interface Logic for A Coax Transmission Line



*** TO MAINTAIN LOSS AT 95% OF IDEAL SIGNAL, SELECT TRANSFORMER INDUCTANCE SUCH THAT:**

TL/F5237-18

$$L(MIN) = \frac{10{,}000}{f_{CLK}}$$

f_{CLK} = SYSTEM CLOCK FREQUENCY (e.g., 18.87 MHz)

EXAMPLE:

$$L = \frac{10{,}000}{18.87 \times 10^6} \longrightarrow L(MIN) = 530\mu H$$

Notes: 1) Less inductance will cause greater amplitude attenuation.

2) Greater inductance may decrease signal rise time slightly and increase ringing, but these effects are generally negligible.

FIGURE 17. Transformer Selection

Section 10
Disk Support

10

LSI Components for Winchester Disk Drives and Controllers

National Semiconductor
Application Note 334
Mike Evans
John Payne
Tim Stout
March 1983

INTRODUCTION

Designing an LSI solution for disk system data path electronics requires careful examination of the total disk market place. The objective is to have a high performance solution able to handle state-of-the-art, 14-inch drives while still being reasonably priced for the lower performance, highly cost-sensitive 5 1/4-inch market. The OEM Winchester disk market consists of three main device types: 14-inch, 8-inch and 5 1/4-inch. OEM supplied 14-inch drives range from capacities of 40 megabytes upwards to 1 gigabyte with data rates of 10–24 megabits/second and access times of 25 ms. The 8-inch Winchester drives evolved from scaling of the 14-inch drives and are suitable devices for minicomputer environments. Storage capacities vary from 16 megabytes to 200 megabytes with typical data rates of 7–9 megabits/second and typical access times of 30 ms. The 5 1/4-inch Winchester drive offers a high performance, high capacity version of the established 5 1/4-inch floppy disk. It is thus ideally suited to packaging in microcomputer-based systems. Initially, 5 1/4-inch drives offered 6 megabytes of storage with typical access times of 170 ms. Recently, devices have been announced with storage capacities of over 100 megabytes and access time of 30 ms. Data rates are typically 5 Mbits/second, but will increase.

PERFORMANCE/STANDARDS SET DESIGN AIMS

The rapid evolution of Winchester drives has pushed storage capacities, data rates and access times to the limit. The DP8460 series hard disk chip set has been designed to handle data rates as high as 25 megabits/second to interface with the fastest drives now available. The chip set uses the latest bipolar and CMOS processing techniques as shown in *Figure 1.*

The use of high density run-length-limited codes is well established in the 14-inch market and will migrate to the 8-inch and 5 1/4-inch drives. A further consideration of the design was the ability to work with such codes. Similarly, as storage densities increase, the necessity for ECC (error checking and correcting) electronics becomes apparent. Specific codes have yet to become standard since some in use today are considered inadequate for the future. The hard disk chip set design was required to anticipate such future developments. Furthermore, the design and functional partitioning had to take into account existing standards such as SMD and ANSI X3.101 and yet allow flexibility in areas where standards are still emerging. Finally, the introduction of removable media cartridges places increasing emphasis on programmable format.

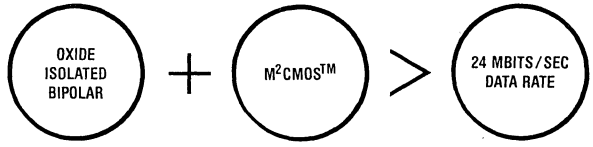


FIGURE 1. Two New Processes Provide Fast Data Rate Capability

FUNCTIONS COMMON TO ALL DISK SYSTEMS

There are certain functions which all disk systems typically perform (*Figure 2*). As one looks at the data path of a disk system during a read operation, following it from the recording head to the host, there emerge eight well defined functions that are common to all disk drives.

These are:

1. Select the desired head and preamplify the signal from it.
2. Convert the data signal from an analog waveform into a sequence of digital pulses.
3. Generate a clock and synchronized data from the digital pulse train using phase-locked-loop techniques.
4. Decode the synchronized data using the clock.
5. Deserialize the data into byte-wide blocks and byte-align.
6. Identify the desired sector and strip off synchronization information, addressing information, and error check information.
7. Buffer the valid data from the desired sector.
8. Transfer the data into the hosts's main storage.

Six similar functions are required for writing the data:

1. Transfer the data out of the host's main storage.
2. Buffer the data.
3. Identify the desired sector, then append synchronization and error checking fields to the data field.
4. Serialize the data.
5. Encode the data.
6. Select the correct recording head and drive it with the encoded data signal.

A disk system is typically separated into two subsystems, the drive and the controller. However, there is no single definition as to which functions are performed in which place, the major disk-to-controller interfaces make the division in different places.

In the floppy extension interface (ST506), the drive performs the functions related to head selection, driving, preamplification, and the analog-to-digital conversion. Everything else is done in the controller. For the SMD and ANSI X3.101 interfaces the drive also performs read clock generation, data decoding, and data encoding. Finally, with the intelligent disk interface, all of the functions are performed by the drive except DMA, which is done by the controller.

The DP8460 series will work with all of the interfaces discussed above. The chips implementing the various functions are placed in the drive or the controller depending upon the particular interface used. The first chips in the set, the pulse detector, data separator, and disk data controller perform all of the functions discussed above with the exception of head operations.

The DP8464 pulse detector converts the analog signal from the head preamplifier into digital pulses. The DP8460 data separator performs read clock generation utilizing an internal phase-locked-loop and data signal decoding. The DP8466 disk data controller performs the remaining functions.

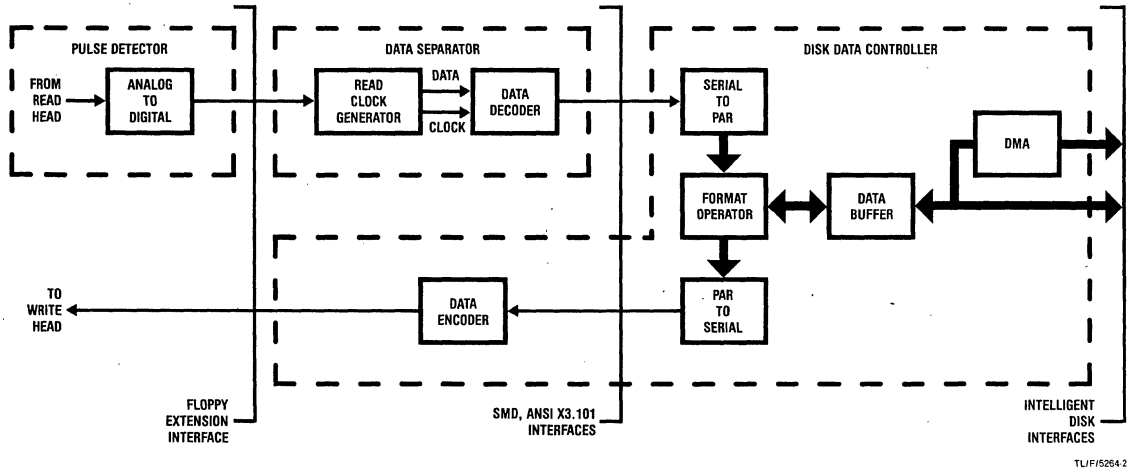


FIGURE 2. Disk Data Path Functions

DP8464 PULSE DETECTOR

The pulse detector receives the analog signal from the read/write head amplifier and converts the peaks to digital pulses. It is always situated in the disk drive. The primary purpose of the pulse detector is to convert the analog signal received from the recording head into a sequence of digital pulses that can be decoded by the data separator (*Figure 3*). Each flux reversal of the recording media represents a coded "1"; the absence of a reversal in a given window time represents a coded "0".

The pulse detector sees flux reversals as signal peaks from the recording head, and produces digital output pulses coinciding with the position of the incoming signal peaks.

Figure 4a is a plot of relative pulse amplitude versus bits per inch (or recording density). As the recording density increases, bit interaction causes the signal amplitude to decrease.

Pulse shapes as received by the pulse detector are shown in *Figure 4b*. Regions 1 and 2, the ones predominantly associated with disk drives, are characterized by the analog signal returning to the baseline between pulses.

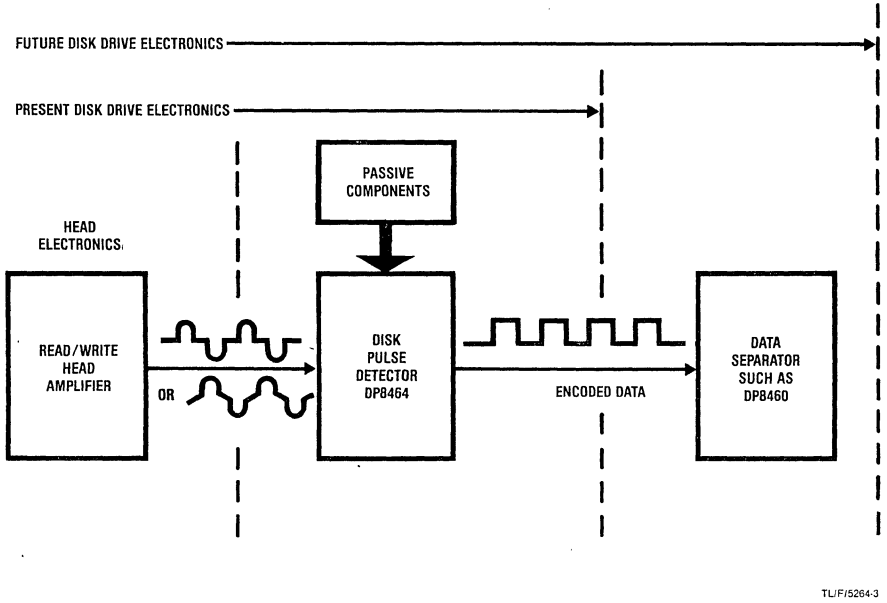


FIGURE 3. Pulse Detector in a Disk System

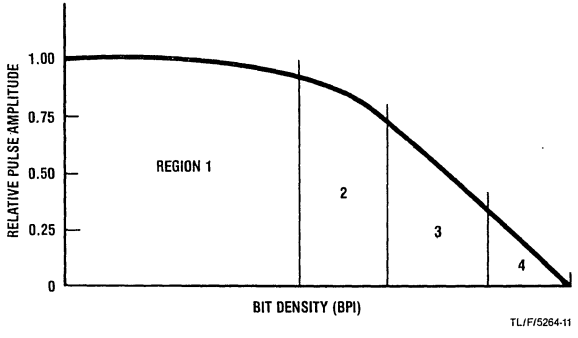


FIGURE 4a. Pulse Amplitude vs Bit Density

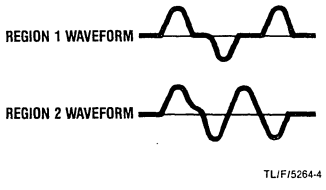


FIGURE 4b. Typical Waveforms

Peak detection is complicated by the susceptibility of the circuitry to noise peaks during this period. The trickiest part of the pulse detector design is to distinguish between signal peaks and noise peaks.

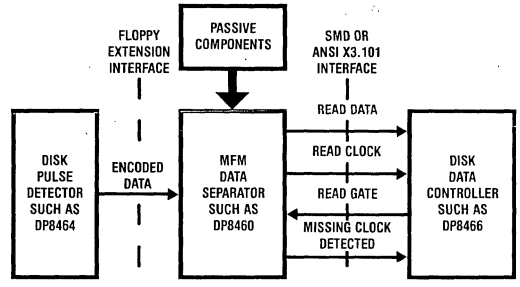
Region 1 is characterized by minimal amplitude distortion with a prolonged return to the baseline. Drives using thin film media or thin film head technology or run-length-limited codes characteristically produce such pulses. The region 1 detector functions by enabling the differentiator from a threshold comparator (*Figure 5*). Only if the signal is greater than a preset threshold will an output pulse be enabled. Since noise peaks are characteristically of low amplitude, this approach effectively eliminates output pulses due to noise.

Average signal strengths from the recording head will vary from track to track and even along the same track. Hence, use of threshold comparison and signal processing mandates automatic gain control (AGC) circuitry to maintain a constant output from the wideband amplifier.

Region 2 is characterized by some amplitude distortion and a tendency for the signal to return to the baseline. Drives using conventional ferrite heads with MFM typically produce such pulses. The pulse detector will work with most drives operating in regions 1 and 2.

DATA SEPARATOR

The DP8460 data separator performs the two basic functions of read clock generation (using an internal phase-locked-loop) and MFM decoding (for MFM systems). It is usable with all of the interfaces discussed in this article. It receives encoded data from a pulse detector and outputs data and clock signals to the controller (*Figure 6*). A block diagram of the chip is shown in *Figure 7*.



*Soft-sectored disks only

FIGURE 6. Data Separator in a Hard Disk System

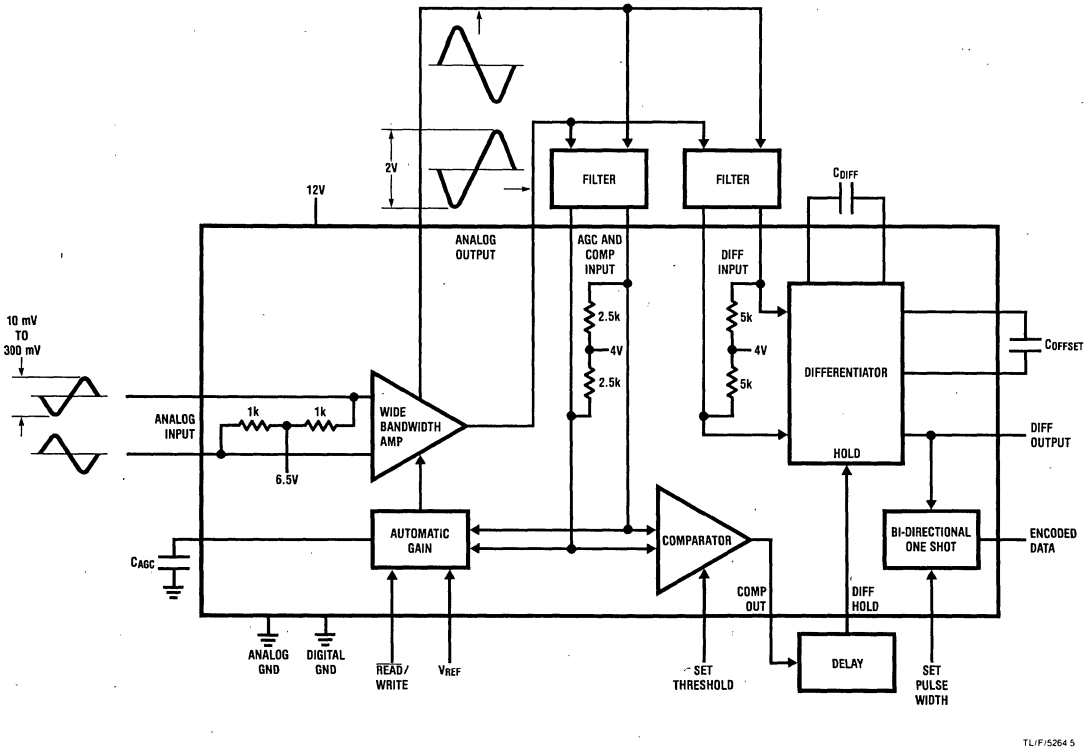


FIGURE 5. Pulse Detector Block Diagram

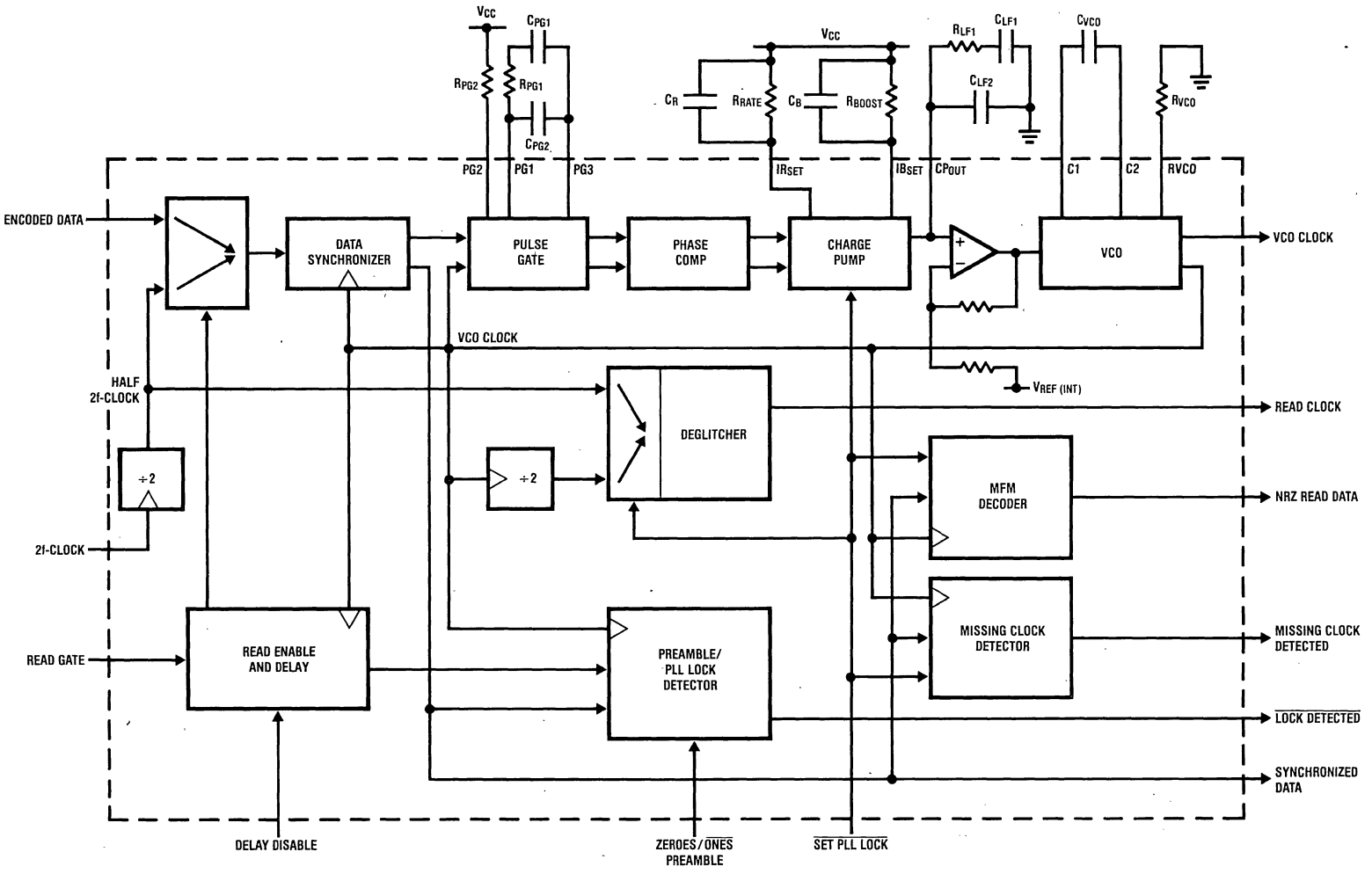


FIGURE 7. Data Separator Detailed Block Diagram

The upper half of the block diagram is the phase-locked-loop which is the heart of the chip. The PLL may be used with disks employing MFM or run-length-limited codes. A serial data output is derived from the incoming raw data that is synchronized to the clock generated by the PLL. The synchronized data and clock pair then connect to an external data decoder for run-length-limited codes. When MFM encoding is used, the output connects internally to the MFM decoder.

The PLL features two user-selectable tracking rates. A high tracking rate is used while the PLL is locking onto the data stream, but once lock-on is achieved, a more stable and slower tracking rate is used. This offers an extremely quick lock-on time of less than two bytes, while allowing reliable operation by removing bit shift distortions when reading the actual data. The tracking rate switches when the external SET PLL LOCK signal goes active. When the chip is not read-enabled, the PLL tracks an external clock source. In a servo system, this is typically the servo clock, while stepper motor drives use a crystal. This allows the PLL to be at frequency when data decoding begins.

Internal to the phase-locked-loop is a clock gate circuit which delays the data signal by an amount equal to half of the window. No external delay lines are required. The delay is guaranteed to be within a specified narrow time slot for all internal sources of error combined.

To generate the read clock, a clock multiplexer and deglitcher are used. The ANSI X3.101 specification calls for only one clock between the drive and controller, which is a combined read clock/servo clock signal. The SMD specification, on the other hand, specifies both clocks are to be on the interface simultaneously. The chip follows the ANSI specification so that it can work in both systems.

When SET PLL LOCK goes active, the READ CLOCK output switches from external clock to the PLL clock. The switch back takes place when the READ GATE signal goes inactive. The deglitcher ensures that no short clock periods are ever sent to the controller as a result of the switch between the two clocks.

The other portion of the chip is a data decoder that is used with systems using the MFM data code. Before lock-on the MFM decoder assumes that every incoming pulse is a clock pulse and not MFM data. When SET PLL LOCK goes active, the phase pattern between clock pulses and data pulses is frozen to allow decoding of the data. The output of this section is sent to the controller as NRZ READ DATA along with the synchronous READ CLOCK.

The missing clock detector monitors the incoming data pattern for an MFM missing clock violation. If there is an incoming address mark, and a missing clock is detected, the chip activates the signal MISSING CLOCK DETECTED.

DISK DATA CONTROLLER

The DP8466 disk data controller is designed to control the data transfer between the disk drive and the system as shown in *Figure 8.* All other functions are left to a microcontroller or microprocessor. The DDC interfaces to the data separator, on one side, and the system bus or an intelligent disk interface, on the other side. The primary data path functions are to sequence the format field, identify the desired sector, serialize memory data when writing to disk, and to deserialize and byte-align the disk data. Other data path functions performed are data buffering and DMA handling. See *Figure 9* for a block diagram of the chip.

It is inadequate to store data on the disk media directly as received from the host. Various extra fields are needed. The external PLL needs a preamble field in order to achieve lock-on. The deserializer needs a synch field to distinguish the end of the preamble to establish byte boundaries within the serial data stream. Address fields, called headers, are needed to identify and locate specific blocks of data. Error checking and correcting fields are typically appended to the data, as well as various types of postambles and gaps.

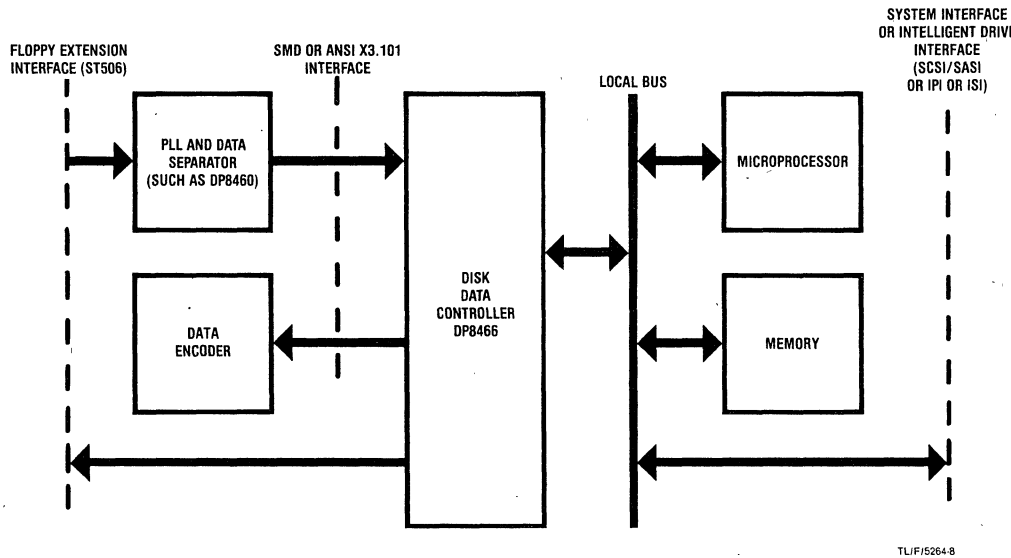
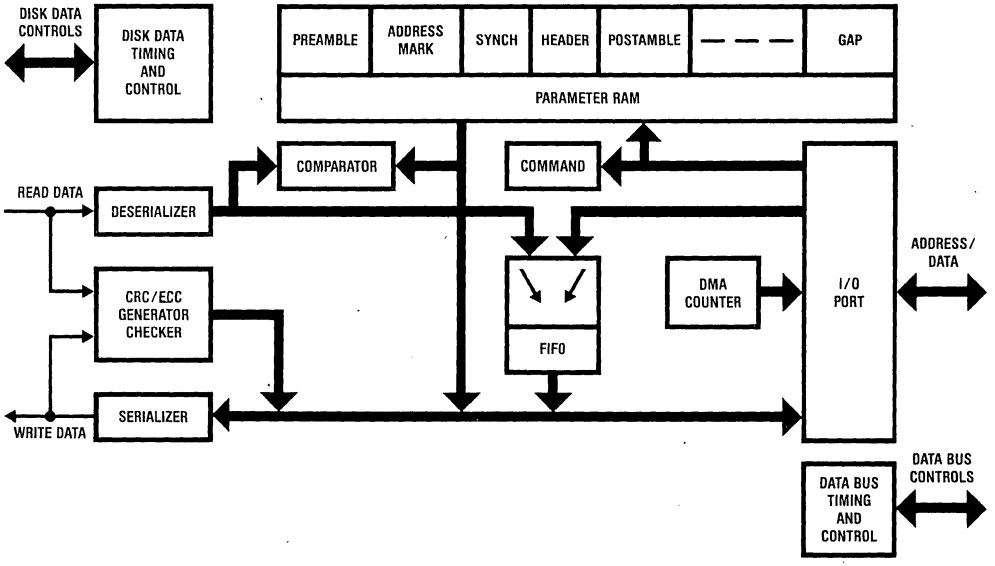
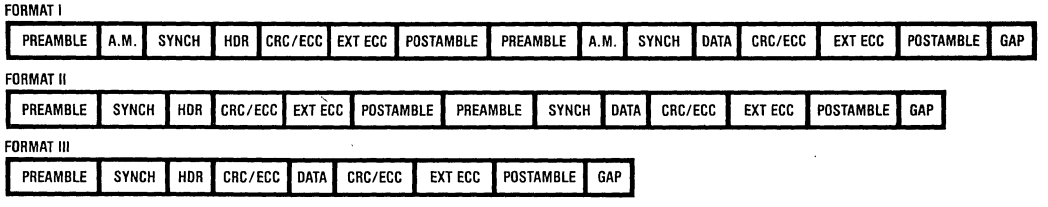


FIGURE 8. Disk Data Controller in a Disk System



TL/F/5264-9

FIGURE 9. Disk Data Controller Block Diagram



TL/F/5264-10

FIGURE 10. Typical Disk Formats

The particular sequence and combination of fields used in storing information on the disk is called the format. There is no standard format which is used in all disk drives, but three popular formats are shown in *Figure 10.* To meet all the different needs of these drives, the chip is externally programmable. The user chooses his own preamble, synch pattern, address mark, postamble and gap, and the order of the format. This is usually performed only once, at initialization. During normal operations such as reading to, or writing from the disk, header information is written to the chip from the microprocessor, along with the mode of operation to be performed such as single or multi-sector, read, or write. Information in the status register or the error register may be accessed.

The serializer converts the parallel data from memory into a serial bitstream and outputs it as NRZ data coincident with the WRITE CLOCK, to interface direct to the SMD or ANSI interfaces. The DDC may also be configured to output MFM encoded data to interface easily to the floppy extension (ST506) interface. The deserializer converts the serial bitstream into byte-wide data for memory. The deserializer features a comparator which is not only used to perform the initial byte-boundary synchronization but is also used in identifying header address.

An internal 32-byte (16-word) FIFO buffers memory data transfers. This FIFO is sufficiently deep to allow extensive microprocessor usage during transfer operations without causing overruns. The chip can be set to transfer data 8 bits or 16 bits at a time. Direct memory access (DMA) capabilities are also included on-chip. A counter provides a 16-bit address field which can be strobed out of the I/O bus prior to valid data. DMA handshake and control signals are provided. This eliminates the need for an external DMA controller chip, and allows faster memory transfers.

Cyclic redundancy check (CRC) or ECC calculations are made on-chip and appended to the data stream when writing, or checked with the CRC/ECC appendage when reading. When the on-chip CRC/ECC codes are undesirable, external circuitry may be used. The disk data controller has two control pins for communication with such circuitry.

Besides the standard features discussed above, the chip has a number of special features. A unique interrupt, called HFASM, notifies the microprocessor that the header failed but the sector numbered matched; this is usually a serious condition requiring immediate attention. If this condition occurs, the last header field read is stored internally and is accessible to the microprocessor. Sector interlocking is available for special microprocessor format sequencing. In multiple sector operations, checkpoint interrupts to the microprocessor are available.

National Semiconductor

Disk Support
PRELIMINARY

DP8460 Data Separator

General Description

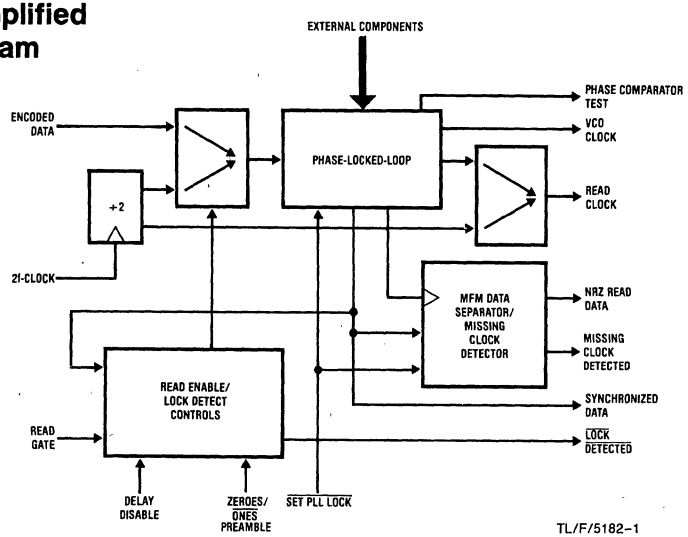
The DP8460 Data Separator is designed for application in disk drive memory systems, and depending on system requirements, may be located either in the drive or in the controller. It receives digital pulses from a pulse detector circuit (such as the DP8464 Disk Pulse Detector), if the DP8460 is situated in the drive, or from the Floppy Extension Interface if it is situated in the controller. After locking on to the frequency of these input pulses, it separates them into synchronized data and clock signals. If the input pulses are MFM encoded data, the data is made available as decoded NRZ data to be deserialized directly by a controller (such as the DP8466 Disk Data Controller). If a run-length-limited code is used, the synchronized data output is available to allow external circuitry to perform the data decoding function. All of the digital input and output signals are TTL compatible and only a single +5V supply is required. The chip is housed in a standard narrow 24-pin dual-in-line package (DIP) and is fabricated using Advanced Schottky bipolar analog and digital circuitry. This high speed I.C. process allows the chip to work with data rates up to 25Mbit/sec. There are three versions of the chip, each having a different decode window error specification. All three versions (−2, −3, −4) will operate from 2 to 25Mbit/sec, with respectively increasing window errors, as specified in the Electrical Characteristics Table.

The DP8460 features a phase-lock-loop (PLL) consisting of a pulse gate, phase comparator, charge pump, buffering amplifier, and voltage-controlled-oscillator (VCO). Pins are provided for the user to select the values of the external filtering components required for the pulse gate and amplifier, the frequency setting components required for the VCO, and two current setting resistors for the charge pump. The DP8460 has been designed to lock on to the incoming preamble data pattern within the first two bytes, using a high rate of charge pump current. Once lock-on has been achieved, the charge pump switches to a lower rate (both rates being determined by the external resistors) to maintain stability for the remainder of the read operation. At this time the READ CLOCK output switches, without glitching, from half the 2f-CLOCK frequency to half the VCO CLOCK frequency. After lock-on, with soft sectored disks, the MISSING CLOCK DETECTED output indicates when a missing clock in an address mark field occurs so the controller can align byte boundaries to begin deserialization of the incoming data.

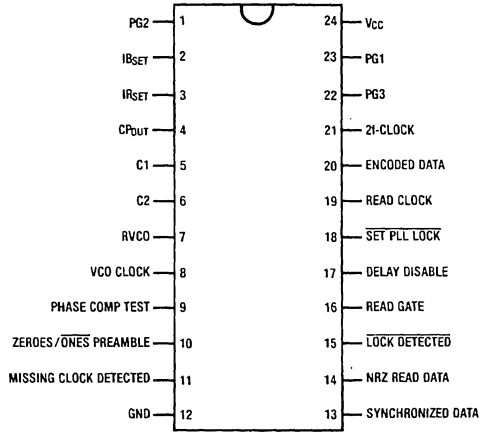
Features

- Operates at data rates up to 25Mbit/sec
- Separates MFM data into read clock and serial NRZ data
- 4 byte preamble-lock indication capability
- Preamble recognition of MFM encoded "0"s or "1"s
- User-determined PLL loop filter network
- PLL charge pump has two user-determined tracking rates
- External control of track rate switchover
- No glitch on READ CLOCK at switchover
- Synchronized data provided as an output (for RLL codes)
- ORed phase comparator outputs for monitoring bit-shift
- Missing clock detected for soft sectored disks
- Less than ½W power consumption
- Standard narrow 24-pin DIP
- Single +5V supply

DP8460 Simplified Block Diagram



TL/F/5182–1



TOP VIEW

TL/F/5182–2

PIN DEFINITIONS:

Power Supply

24 Vcc +5V ±5%

12 Ground

TTL Level Logic Inputs

16 READ GATE: This is an active high input signal that sets the DP8460 Data Separator into the Read Mode.

17 DELAY DISABLE: This input determines the delay from READ GATE going high to the time the DP8460 enters the Read Mode. If DELAY DISABLE is set high, this delay is within one cycle of the 2f-CLOCK signal. If DELAY DISABLE is set low, the delay is thirty two cycles of the 2f-CLOCK, as shown in *Figure 1.*

18 SET PLL LOCK: This input allows the user to determine when the on-chip PLL will go into the low track rate. A high level at this input results in the PLL being in the high track rate. If this input is connected to the LOCK DETECTED output, the PLL will go into the low track rate mode immediately after lock is detected.

10 ZEROES/ONES PREAMBLE: A high level on this input enables the circuit to recognize an All Zeros data preamble. A low level results in the recognition of an All Ones data preamble.

20 ENCODED DATA: This input is connected to the output of the head amplifier/pulse-detecting network located in the disk drive. Each positive edge of the ENCODED DATA waveform identifies a change of flux on the disk. In the case of MFM encoded data, the input will be raw MFM.

21 2f-CLOCK: This is a system clock input, which is either a signal generated from the servo track (for systems utilizing servo tracks), or a signal buffered from a crystal.

TTL Level Logic Outputs

8 VCO CLOCK: This is the output of the on-chip VCO, transmitted from an Advanced Schottky-TTL buffer. It is synchronized to the MFM data output and, if needed, it can be used as the 2f-CLOCK for encoding MFM when writing to the disk.

15 LOCK DETECTED: This output goes active low only after both PLL Lock has occurred and the preamble pattern has been recognized. It remains low until READ GATE goes inactive.

14 NRZ READ DATA: This is the NRZ decoded data output, whose leading edges coincide with the trailing edge of READ CLOCK.

13 SYNCHRONIZED DATA: This output is the same encoded data that is input to the chip, but is synchronous with the negative edge of the VCO CLOCK.

11 MISSING CLOCK DETECTED: When a missing clock is detected, this output will be a single pulse (of width equal to one cycle of READ CLOCK) occurring as shown in *Figure 2.*

19 READ CLOCK: This is half VCO CLOCK frequency during read mode after PLL Lock; it is half 2f-CLOCK frequency at all other times. A deglitcher is utilized to ensure that no short clock periods occur during either switchover.

9 PHASE COMP TEST: This output is the logical "OR" of the Phase Comparator outputs, and may be used for the testing of the disk media.

Analog Signals

23, 22, PG1, PG3: The external capacitors and resistor of the Pulse Gate filter are connected to these pins.

1 PG2: This is the Pulse Gate current supply.

3 IRSET: The current into the rate set pin (V_{BE}/R_{Rate}) is half the charge pump output current for the slow tracking rate.

2 IBSET: The current into the boost set pin (V_{BE}/R_{Boost}) is half the amount by which the charge pump current is increased for the high tracking rate. (I_{HIRATE} = I_{RATE} Set + I_{BOOST} Set).

4 CPOUT: CHARGE PUMP OUT/BUFFER AMP IN is available for connection of external filter components, for the phase-lock-loop. In addition to being the charge pump output node, this pin is also the noninverting input to the op-amp of the Buffer Amplifier.

7 RVCO: The current into this pin determines the operating currents within the VCO.

5, 6 VCO C1, C2: An external capacitor connected across these pins sets the nominal VCO frequency.

Absolute Maximum Ratings

Supply Voltage	7V
TTL Inputs	7V
Output Voltages	7V
Input Current (CPOUT, IRSET, IBSET, RVCO)	2mA
Storage Temperature	−65°C to 150°C

Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CC}	Supply Voltage		4.75	5.00	5.25	V
T_A	Ambient Temperature		0	25	70	°C
I_{OH}	High Logic Level Output Current	V_{CO} Clock Others			−2000 −400	μA
I_{OL}	Low Logic Level Output Current	V_{CO} Clock Others			20 8	mA
f_{DATA}	Input Data Rate		2.0		25	Mbit/sec
t_{WCK}	Width of 2f-CLOCK, High or Low		10			ns
t_{WPD}	Width of ENCODED DATA Pulse, High or Low (Note 2)		0.25t			ns
V_{IH}	High Logic Level Input Voltage		2			V
V_{IL}	Low Logic Level Input Voltage				0.8	V

DC Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_I = −18mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min., I_{OH} = Max.	V_{CC}−2V	V_{CC}−1.6V		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = Max.			0.5	V
I_{IH}	High Level Input Current	V_{CC} = Max., V_I = 2.7V			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max., V_I = 0.4V			−200	μA
I_O	Output Drive Current	V_{CC} = Max., V_O = 2.125V[1]	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = Max.			100	mA
I_{OUT}	Charge Pump Output Current	$I_{RSET} = V_{BE}/R_{RATE}$ $I_{BSET} = V_{BE}/R_{BOOST}$	−10% −10%	$2\times I_{RSET}$ $2\times(I_{RSET}+I_{BSET})$	+10% +10%	mA

1. This value has been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.
2. t is defined as the period of the encoded data

AC Electrical Characteristics Over Recommended V_{CC} and Operating Temperature Range.

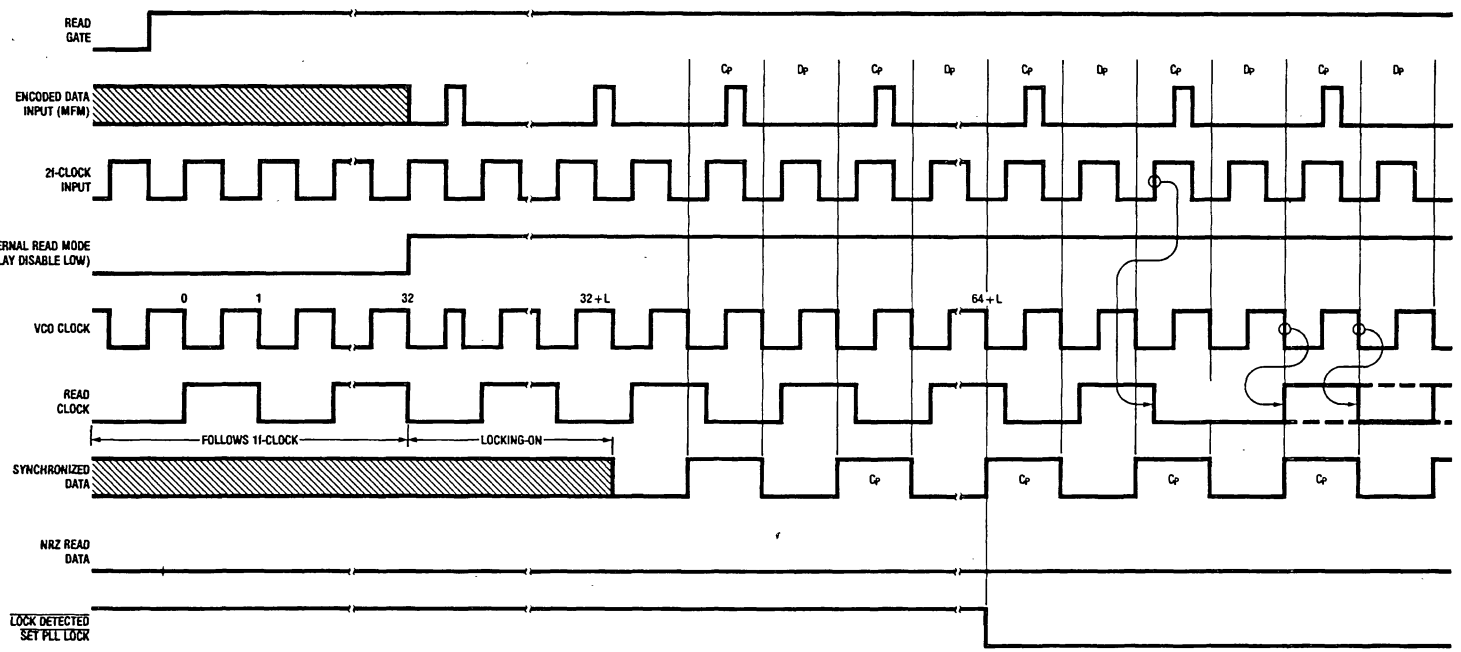
(All Parts unless stated otherwise) ($t_R = t_F = 2.0$ns, $V_{IH} = 3.0$V, $V_{IL} = 0$V)

Symbol	Parameter	Min	Typ	Max	Units
t_{READ}	Positive READ CLOCK transitions from READ GATE set active until PLL Lock sequence begins (DELAY DISABLE low)		16	17	—
t_{READ}	Positive READ CLOCK transitions from READ GATE set active until PLL Lock sequence begins (DELAY DISABLE high)		1	1	—
$t_{DECODE\ NRZ}$	Number of READ CLOCK cycles required to output each decoded MFM data bit[4]	—	2	3	T-clock
$t_{TRANSMIT\ MFM}$	Positive READ CLOCK transitions required to transmit input MFM to output	1	2	3	—
$t_{READ\ ABORT}$	Number of READ CLOCK cycles after READ GATE set low to read operation abort			2	T-clock
t_{WINDOW}	Variance of center of decode window from nominal[7] DP8460-2 DP8460-3 DP8460-4			$2+0.6\%\tau$ $3+0.8\%\tau$ $4+1.0\%\tau$	ns
$\phi_{LINEARITY}$	Phase range for charge pump output linearity[2]	$-\pi$		$+\pi$	Radians
K_1	Phase Comparator — Charge Pump gain constant[5]		$\frac{V_{BE}}{\pi R}$		Amps/rad
$V_{CONTROL}$	Charge pump output voltage swing from nominal		±100		mV
K_{VCO} (=A×K_2)	VCO gain constant (ω_{VCO} = VCO center frequency in rad/s)[6]	$\frac{1.4\omega_C}{V_{BE}}$	$\frac{1.6\omega_C}{V_{BE}}$	$\frac{1.8\omega_C}{V_{BE}}$	rad/sec. V
f_{VCO}	VCO center frequency variation over temperature and V_{CC}	−5		+5	%
$f_{MAX\ VCO}$	VCO maximum frequency	70			MHz
t_{HOLD}	Time READ CLOCK is held low during changeover after lock detection has occurred[3]			1½	T-clock
$t_{MFMSKEW}$	Output skew between VCO clock and Synchronized Data				ns
$t_{NRZSKEW}$	Output skew between READ CLOCK, NRZ READ DATA and MISSING CLOCK DETECTED				ns

1. A sample calculation of frequency variation vs. control voltage: $V_{IN} = \pm 0.2$V; $K_{VCO} = \frac{\omega_{OUT}}{V_{IN}} = \frac{0.4\ \omega_C}{0.2V} = \frac{2.0\ \omega_C}{V}$ $\frac{(rad/sec)}{(volt)}$
2. $-\pi$ to $+\pi$ with respect to 2f VCO CLOCK
3. T-clock is defined as the time required for one period of the READ CLOCK to occur.
4. This number remains fixed after PLL Lock occurs.
5. With respect to VCO CLOCK; $I_{PUMP\ OUT} = 2\ I_{SET}$
   $I_{SET} = \frac{V_{BE}}{R_{SET}}$
6. Although specified as the VCO gain constant, this is the gain from the Buffer Amplifier input to the VCO output.
7. τ is defined as the period of the incoming data stream

External Component Selection (All Parts)

Symbol	Component	Min	Typ	Max	Unit
R_{VCO}	VCO Frequency Setting Resistor	990		1010	Ω
C_{VCO}	VCO Frequency Setting Capacitor	15			pF
R_{LF}	Loop Filter Resistor	TBD		TBD	Ω
C_{LF1}	Loop Filter Capacitor 1	20		TBD	pF
C_{LF2}	Loop Filter Capacitor 2	20		TBD	pF
R_{RATE}	Charge Pump I_{RATE} Set Resistor	1.2		6.5	kΩ
R_{BOOST}	Charge Pump (High Rate) I_{BOOST} Resistor	0.4		∞	kΩ
R_{PG2}	Delay Time Setting Resistor	0		150	kΩ
R_{PG1}	Pulse Gate Resistor	TBD		TBD	kΩ
C_{PG1}	Pulse Gate Capacitor C1	20		TBD	pF
C_{PG2}	Pulse Gate Capacitor C2	20		TBD	pF
C_R	I_{RATE} Bypass Capacitor	1000			pF
C_B	I_{BOOST} Bypass Capacitor	1000			pF



TL/F/5182–3

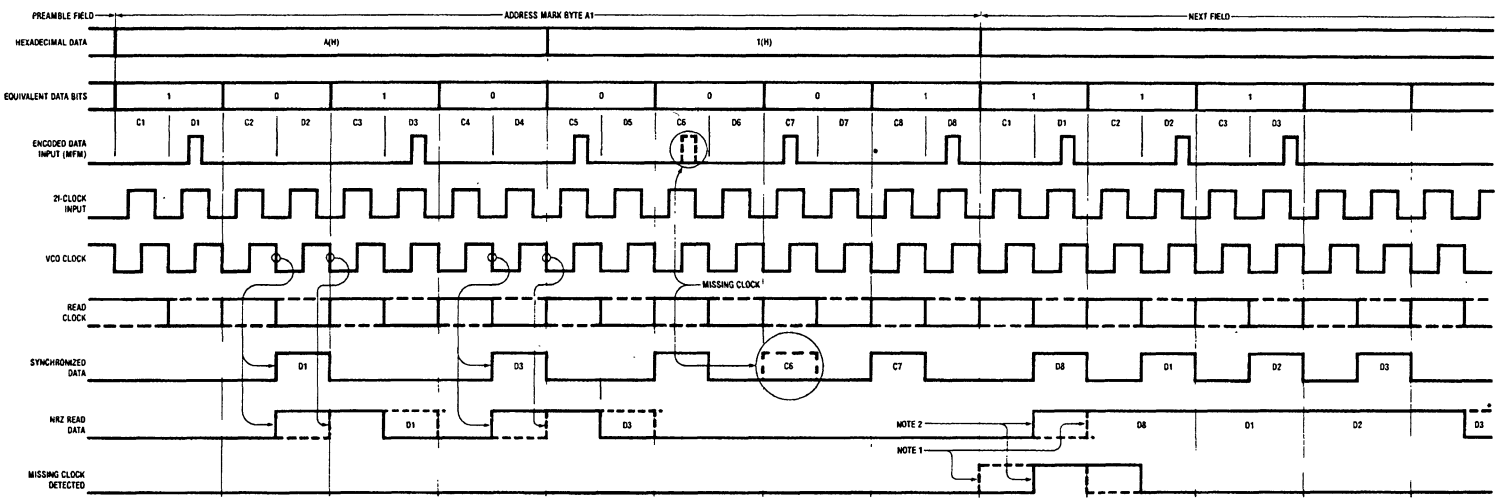
C_P, D_P = preamble clock and preamble data bits respectively.

L = Number of 2f-clock cycles required for VCO to lock (typically ≈ 20 2f-clock cycles), but determined by external component values

At 32 + L, VCO has just locked.

At 64 + L, circuit has confirmed lock (has been in lock for 16 MFM clock bits). This sequence shows the MFM preamble pattern.

FIGURE 1. Lock-on Sequence Waveform Diagram



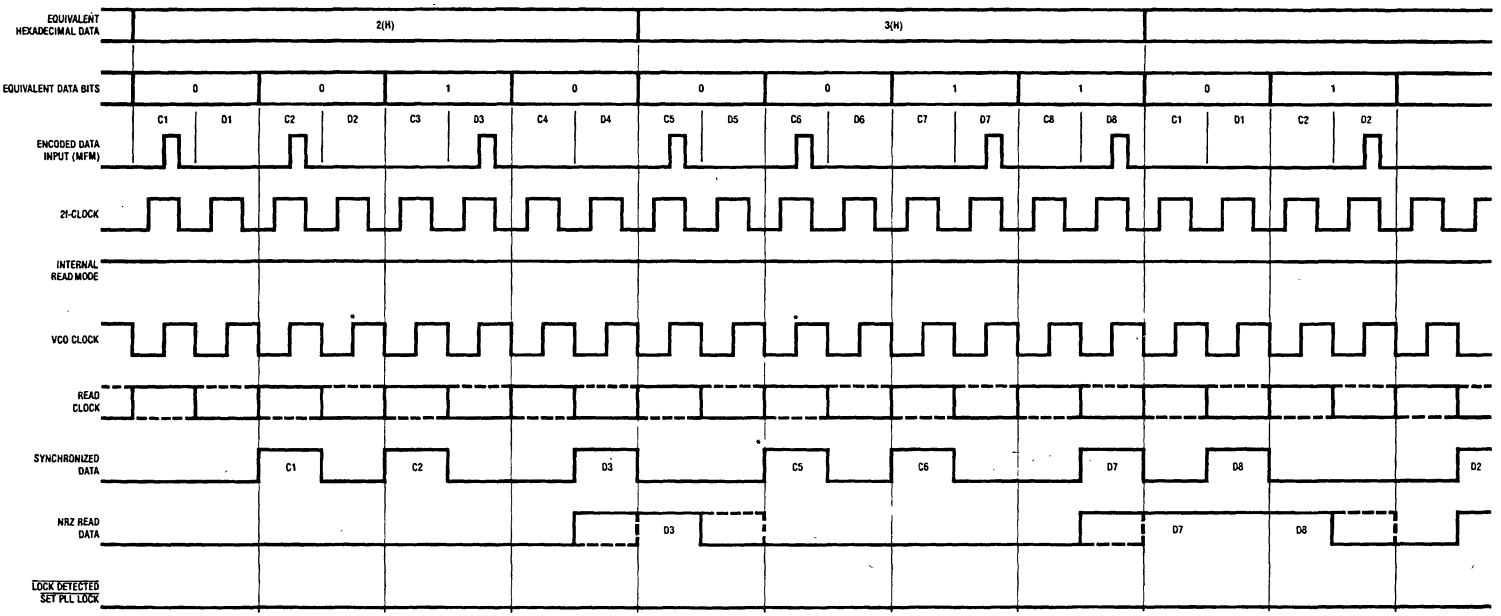
TL/F/5182–4

* READ CLOCK and NRZ READ DATA may be delayed by one VCO clock period depending on the phase of the internal clock at activation of READ GATE input.

① MISSING CLOCK DETECTED is one READ CLOCK period ahead of the chip issuing D8 on the NRZ READ DATA output when READ CLOCK is delayed by one VCO clock period

② MISSING CLOCK DETECTED is synchronous with the chip issuing D8 on the NRZ READ DATA Output when READ CLOCK is not delayed

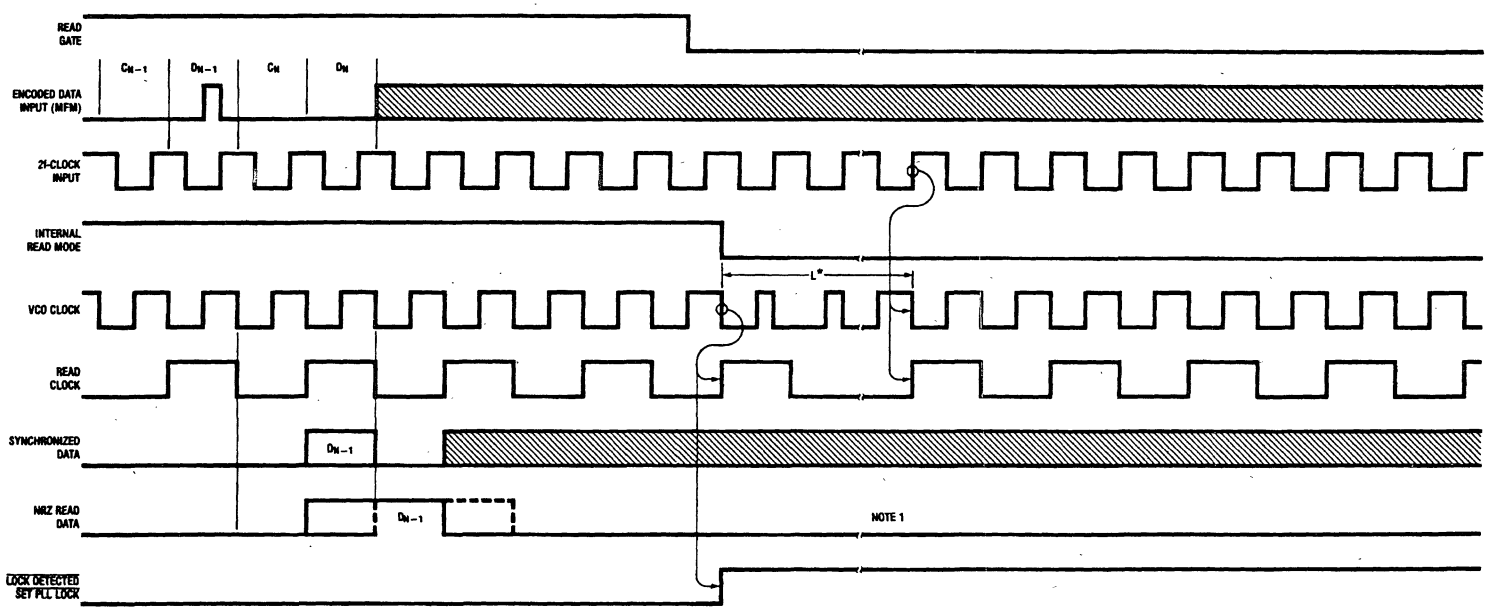
FIGURE 2. Missing Clock Detection Waveform Diagram



TL/F/5182–5

* READ CLOCK and NRZ READ DATA may be delayed by one VCO clock period with respect to Synchronized Data depending on the phase of the internal clock at activation of READ GATE input.

FIGURE 3. Locked-on Waveform Diagram

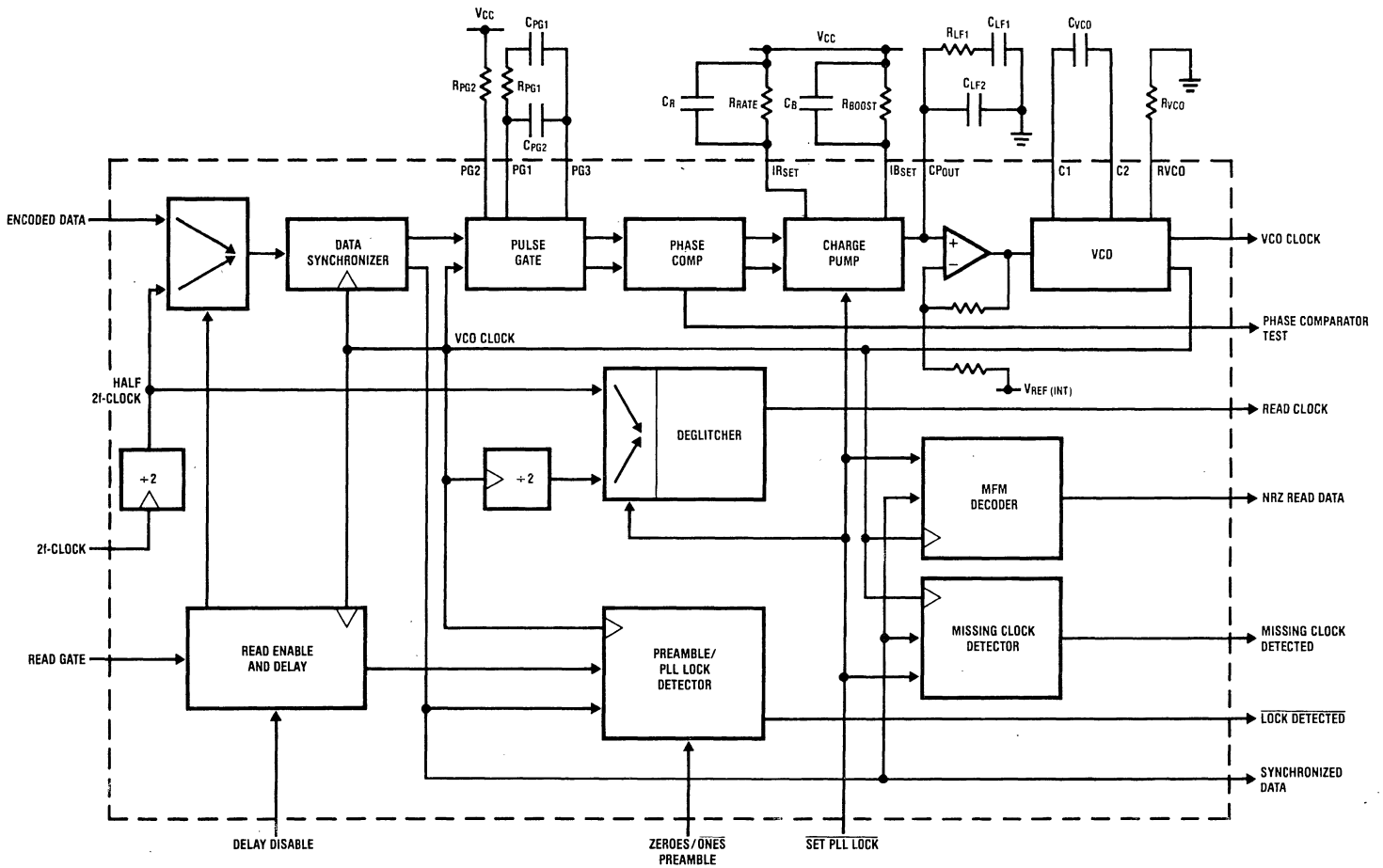


TL/F/5182–6

* L indicates the number of cycles required for the VCO to lock to the 2f-CLOCK

NOTE 1: READ GATE going low will always result in NRZ READ DATA going low regardless of the state of the last bit

FIGURE 4. Lock-Ending Sequence Waveform Diagram


VCC
CPG1
RPG2
RPG1
CPG2
PG2
PG1
PG3
VCC
CR
RRATE
CB
RBOOST
IRSET
IBSET
RLF1
CLF1
CLF2
CPOUT
CVCO
RVCO
C1
C2
RVCO
ENCODED DATA
DATA SYNCHRONIZER
PULSE GATE
PHASE COMP
CHARGE PUMP
VCO
VCO CLOCK
PHASE COMPARATOR TEST
VREF (INT)
VCO CLOCK
HALF 2f-CLOCK
÷2
2f-CLOCK
÷2
DEGLITCHER
READ CLOCK
MFM DECODER
NRZ READ DATA
READ GATE
READ ENABLE AND DELAY
PREAMBLE/ PLL LOCK DETECTOR
MISSING CLOCK DETECTOR
MISSING CLOCK DETECTED
LOCK DETECTED
SYNCHRONIZED DATA
DELAY DISABLE
ZEROES/ONES PREAMBLE
SET PLL LOCK

TL/F/5182–7

CIRCUIT OPERATION

When the READ GATE input goes high, the DP8460 Data Separator enters the read mode after a period determined by the state of the DELAY DISABLE pin. This may be either one or thirty two 2f-CLOCK cycles. Referring to *Figure 1*, once in the read mode, the phase-locked-loop reference signal is switched from 2f-CLOCK input to the ENCODED DATA input. The PLL, initially in the high-tracking rate mode, then attempts to lock onto the incoming encoded data stream. By careful selection of the loop filter components, this can be within 2 bytes. Preamble pattern recognition then can begin. As soon as two bytes of the selected preamble are detected, (the selection is determined by the ZEROES/ONES PREAMBLE pin) the LOCK DETECTED output goes low. In a typical MFM disk drive application, the LOCK DETECTED output is directly connected to the SET PLL LOCK input. With this connection, track rate selection, clock output switchover, and data output enabling will occur after four consecutive preamble bytes have been fed into the chip, from the time the read mode began.

A low level on the SET PLL LOCK causes the PLL Charge Pump to switch from the high to low tracking rate. At the same time the source of the READ CLOCK signal is switched from half the frequency of the 2f-CLOCK to half the VCO clock. The MFM decoder also becomes enabled and begins to output decoded NRZ data. If the preamble is being decoded, and it is a zeroes data preamble, the NRZ READ DATA output will remain low until the end of the preamble. It will then output NRZ data some 2f-CLOCK periods after the preamble field has ended, as shown in *Figures 2* and *3*.

Figure 4 shows the sequence when READ GATE goes low, signifying the end of a read operation. The PLL reference signal is switched back to half the 2f-CLOCK and the LOCK DETECTED output (and therefore the SET PLL LOCK input) goes high. The PLL then returns to the high tracking rate, and the output signals return to their initial conditions.

CIRCUIT DESCRIPTION

1. Read Enable and Delay: If the DELAY DISABLE input is connected low, then thirty two 2f-CLOCK cycles after READ GATE goes active, the DP8460 will go into the read mode. If the DELAY DISABLE input is connected high, the chip will go into the read mode one 2f-CLOCK cycle after READ GATE goes active. This feature allows the user to choose the time at which the PLL Lock Sequence begins and thus accommodates systems with short preambles.

2. Pulse Gate, including Input Multiplexer and Data Synchronizer: The Input Multiplexer selects the input to the phase-lock-loop. While the chip is in the bypassed mode, the PLL is locked on half the 2f-CLOCK frequency, but in the read mode, the Input Multiplexer switches to the ENCODED DATA signal. The VCO CLOCK then begins to synchronize with the ENCODED DATA signal. The Pulse Gate allows a reference signal from the VCO into the Phase Comparator only when a ENCODED DATA bit is valid. The Pulse Gate utilizes a scheme which delays the incoming data by one-half the period of the 2f-CLOCK. This optimizes the position of the decode window and allows input jitter up to ± half the 2f-CLOCK period, assuming no error in the decode window position. The decode window error can be determined from the specification in the Electrical Characteristics Table.

3. Phase Comparator: The Phase Comparator receives its inputs from the Pulse Gate, and is edge-triggered from these inputs to provide charge-up and charge-down outputs.

4. Charge Pump: The high speed charge pump consists of a switchable constant current source and sink. The charge pump constant current is set by connecting external resistors to Vcc from the charge current rate set (IRSET) and current boost set (IBSET) pins. Before lock is indicated, the PLL is in the fast tracking rate and both resistors determine the current. In the slow tracking rate after lock-on, only the IRSET resistor determines the charge pump current. The output of the charge pump feeds into external filter components and the Buffer Amplifier.

5. Buffer Amplifier: The input of the Buffer Amplifier is internally connected to the charge pump's constant current source/sink output as well as the external Loop Filter components. The Buffer Amplifier is configured as a high input impedance amplifier which allows for the connection of external PLL filter components to the Charge Pump output pin CPOUT. The output of the Buffer Amplifier is internally connected to the VCO control input.

6. VCO: The Voltage-Controlled-Oscillator requires a resistor from the RVCO pin to ground and a capacitor between pins C1 and C2, to set the center frequency. The VCO frequency can be varied from nominal by approximately ±20%, as determined by its control input voltage.

7. PLL Lock-on/Preamble Pattern Detector: To recognize preamble, the preamble pattern from the disk must consist exclusively of either data bit zeroes (encoded into ..10.. MFM clock pulses) when the ZEROES/ONES PREAMBLE pin is set high, or data bit ones (encoded into ..01.. MFM clock pulses) when set low. The preamble pattern must be long enough to allow the PLL to lock, and subsequently for the Preamble Pattern Detector circuit to detect two complete bytes.

Once the chip is in the read mode, the VCO proceeds to lock on to the incoming data stream. The Preamble Pattern Detector then searches for a continuous pattern of 10101010101010101010101010101010 (16 consecutive pulses at the data rate) to indicate lock has been achieved. The LOCK DETECTED output then goes low.

Any deviation from the above-mentioned one-zero pattern at any time before PLL Lock is detected will reset the PLL Lock Detector. The lock detection procedure will then start again.

8. MFM Decoder: The MFM Decoder receives synchronized MFM data from the Pulse Gate and converts it to NRZ READ DATA. For run-length-limited codes the MFM Decoder and Missing Clock Detector will not be used.

9. Missing Clock Detector: This block is only required for soft-sectored drives, and is used to detect a missing clock violation of the MFM pattern. The missing clock is inserted when writing to soft-sectored disks to indicate the location of the Address Mark in both the ID and the Data fields of each sector. Once PLL Lock has been indicated, the Missing Clock Detector circuit is enabled. MISSING CLOCK DETECTED will go active only if the incoming data pattern contains one suppressed clock bit framed by two adjacent clock bits. The output signal goes high for one cycle of READ CLOCK.

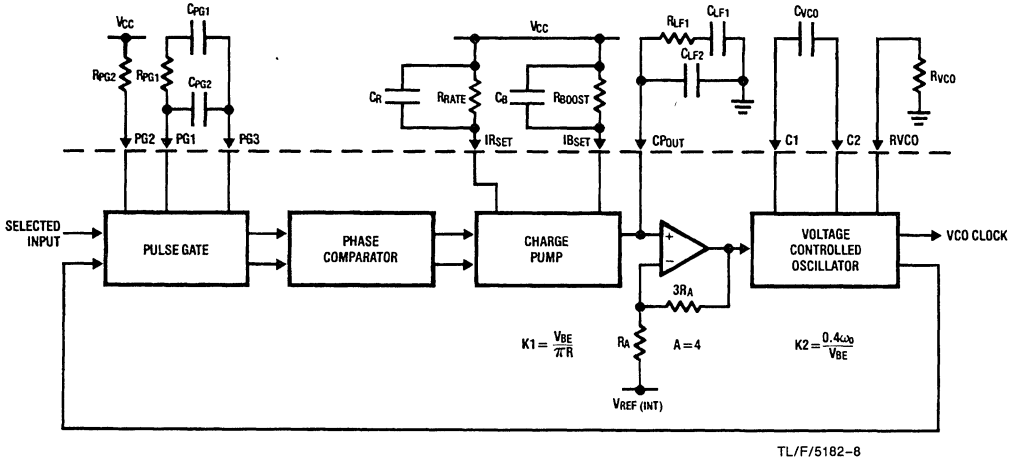
10. Clock Multiplexer and Deglitcher: When the SET PLL LOCK input changes state this circuit switches the source of the READ CLOCK signal between the half 2f-CLOCK frequency and the half VCO CLOCK frequency. A deglitcher circuit is utilized to ensure that no short clock periods occur during either switchover.

BIT-JITTER TOLERANCE

The three options of the DP8460, the −4, −3 and −2 offer decreasing window errors (respectively) so that the parts may be selected for different data rates (up to 25Mbit/sec). The −4 part will be used in most low data rate applications. As an example, at the 5Mbit/sec data rate of most 5¼ inch drives, T = 200ns so that from the Electrical Characteristics Table, t_{WINDOW} = (4 + (1% of 200ns)) or 6ns. The chip therefore contributes up to 6ns of window error, out of the total allowable error of 50ns (half the 2f-clock period of 100ns). This allows the disk drive to have a margin of 44ns of jitter on the transition position before an error will occur.

ANALOG CONNECTIONS TO THE DP8460

External passive components are required for the Pulse Gate, Charge Pump, Loop Filter and VCO as shown in *Figure 5*. The information provided here is for guidelines only. The user should select values according to his own system requirements. Phase-Locked Loops are complex circuits that require detailed knowledge of the specific system. Factors such as loop gain, stability, response to change of signal, lock-on time, etc are all determined by the external components. In many disk systems these factors are critical, and National Semiconductor recommends the designer be knowledgeable of phase-locked-loops, or seek the advice of an expert. Inaccurate design will probably result in excessive disk error rates. The phase-locked-loop in the DP8460 has many advantages over all but the most sophisticated discrete designs, and if the component values are selected correctly, it will offer significant performance advantages. This should result in a reduction of disk error rates over equivalent discrete designs.



TL/F/5182–8

FIGURE 5. Phase-Locked-Loop Section

Pulse Gate

There are four external components connected to the Pulse Gate as shown in *Figure 6* with the associated internal components. The values of R_{PG1}, R_{PG2}, C_{PG1}, and C_{PG2} are dependent on the data rate. R_{PG1} is proportional to the data rate, while R_{PG2}, C_{PG1} and C_{PG2} are inversely proportional. Table I shows component values for the data rates given. For other data rates, use the equations R_{PG1} = (TBD × f_{VCO}) kΩ, R_{PG2} = ((TDB / f_{VCO}) − 0.89) kΩ, C_{PG1} = (TBD / f_{VCO}) pF and C_{PG2} = (TBD / f_{VCO}) pF, where f_{VCO} is the VCO frequency in MHz. As an example, at 5Mbits/sec data rate, f_{VCO} = 10 MHz. This produces R_{PG1} = ... kΩ, R_{PG2} = ... kΩ, C_{PG1} = ... pF and C_{PG2} = ... pF. Components with 5% tolerance will suffice.

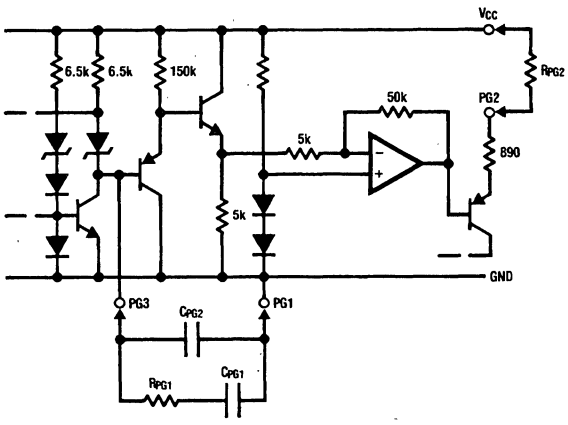
Data Rate	R_{PG2}	R_{PG1}	C_{PG1}	C_{PG2}
2Mbit/sec	16kΩ			
5Mbit/sec	4.7kΩ			
10Mbit/sec	1.9kΩ			
15Mbit/sec	750Ω			
20Mbit/sec	300Ω			
25Mbit/sec	0			

TABLE I. Pulse Gate Component Selection Chart

Charge Pump

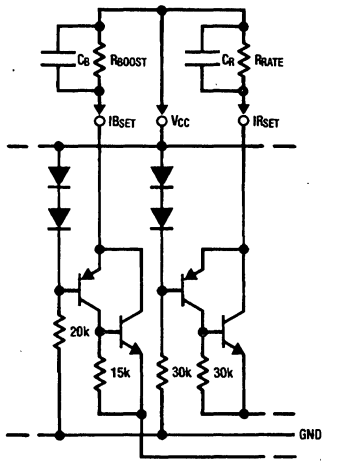
Resistors R_{RATE} and R_{BOOST} determine the charge pump current. The Charge Pump bidirectional output current is approximately (within ±10%) twice the input current. In the high tracking rate with $\overline{\text{SET PLL LOCK}}$ high, the input current is I_{BSET} + I_{RSET}, ie, the sum of the currents through R_{BOOST} and R_{RATE} from Vcc. In the low tracking rate, with $\overline{\text{SET PLL LOCK}}$ low, this input current is I_{RSET} only.

A recommended approach would be to select R_{RATE} first. The External Component Limits table allows R_{RATE} to be 1.2kΩ to 6.5kΩ, so for simplicity select R_{RATE} = 3.3kΩ. A typical loop gain change of 4:1 for high to low tracking rate would require R_{BOOST} = R_{RATE} /3 or 1.1kΩ. Referring to *Figure 7* the input current is effectively V_{BE} / R_{RATE} in the low tracking rate, where V_{BE} is an internal voltage. This means that the current into or out of the loop filter is approximately 2 V_{BE} / R_{RATE}, or in this example approximately 0.4mA. Note that although it would seem the overall gain is dependent on V_{BE}, this is not the case. The loop gain is altered internally by an amount inversely proportional to V_{BE}, as detailed in the section on the Loop Filter. This means that as V_{BE} varies with temperature or device spread, the gain will remain constant for a particular fixed values of R_{RATE} and R_{BOOST}. This alleviates the need for potentiometers to select values for each device. The tolerance required for these two resistors will depend on the total loop gain tolerance allowed, but 5% would be typical. Also Vcc by-pass capacitors are required for these two resistors. A value of 1000pF is suitable for each.



TL/F/5182–9

FIGURE 6. Pulse Gate Controls



TL/F/5182–10

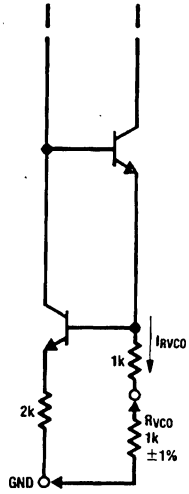
FIGURE 7. I_{RATE} Set and I_{BOOST} Set

VCO

The value of R_{VCO} is fixed at 1 kΩ ±1% in the External Component Limits table. This requires a resistor more accurate than 1% to allow for temperature variations. *Figure 8* shows how R_{VCO} is connected to the internal components of the chip. This value was fixed at 1kΩ to set the VCO operating current such that optimum performance of the VCO is obtained for production device spreads. This means fixed value components will be adequate to set the VCO center frequency for production runs. The value of C_{VCO} can therefore be determined from the VCO frequency f_{VCO}, using the equation: $C_{VCO} = 1 / (R_{VCO})(f_{VCO})$ where f_{VCO} is twice the input data rate. As an example, for a 5Mbit/sec data rate, f_{VCO} = 10Mhz, requiring that C_{VCO} = 100pF. The capacitor tolerance also should be better than 1%. The capacitor is connected to internal circuitry of the chip as shown in *Figure 9*.

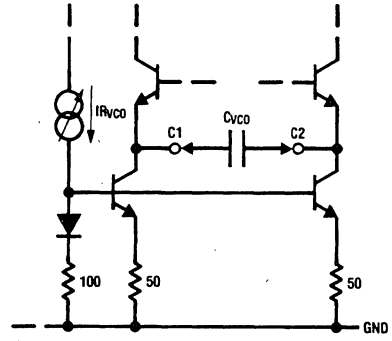
This equation does not cover the whole range of data rates. As the data rate increases and C_{VCO} gets smaller, the effects of unwanted parasitic capacitances influence the frequency. As a guide the graph of *Figure 10* shows approximately the value of C_{VCO} for a given data rate.

The center frequency may be checked by applying pulses at the ENCODED DATA input with READ GATE set high. The input frequency should be varied above and below the chosen center frequency until the VCO stops tracking. Typically this will be 20% either side of the center frequency.



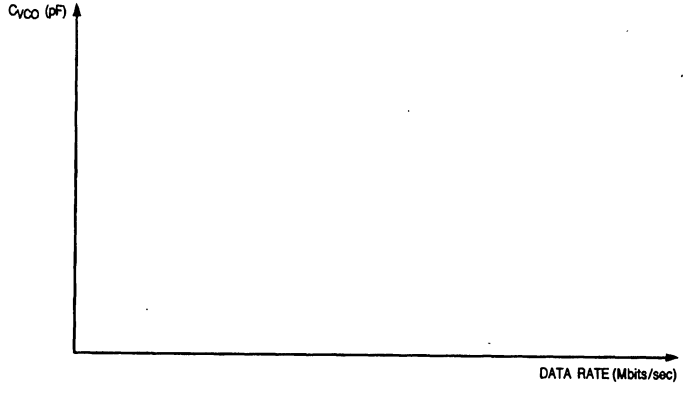
TL/F/5182–11

FIGURE 8. VCO Current Setting Resistor



TL/F/5182–12

FIGURE 9. VCO Capacitor



TL/F/5182–13

FIGURE 10. VCO Capacitor Value for Disk Data Rates

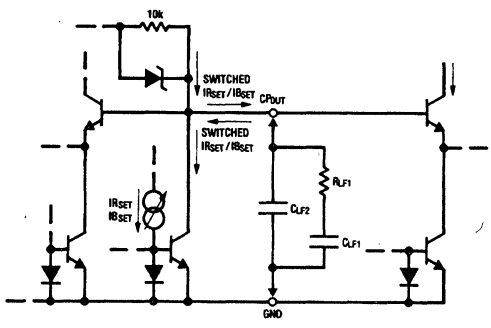
Loop Filter

The input current into the Buffer Amplifier is offset by a matched current out of the Charge Pump, and even so is much less than the switching current in or out of the Charge Pump. It can therefore be assumed that all the Charge Pump switching current goes into the Loop Filter components R_{LF1} and C_{LF1} and C_{LF2}. The tolerance of these components should be the same as R_{RATE} and R_{BOOST}, and will determine the overall loop gain variation. The three components connected to the Charge Pump output are shown in *Figure 11*. Note the return current goes to analog GND, which should be electrically very close to the GND pin itself.

The value of capacitor C_{LF1} basically determines loop stability-the larger the value the longer the loop takes to respond to an input change. If C_{LF1} is too small, the loop will track any jitter on the ENCODED DATA input and the VCO output will follow this jitter, which is undesirable. The value of C_{LF1} should therefore be large enough so that the PLL is fairly immune to phase jitter but not large enough that the loop won't respond to longer term data rate changes that occur on the disk drive.

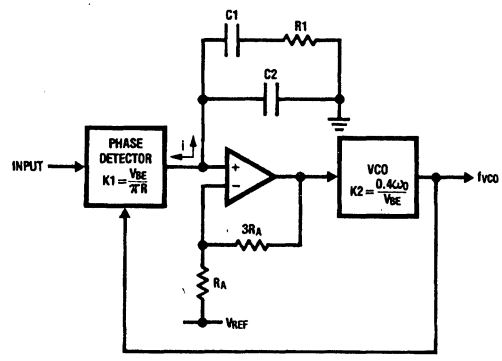
The damping resistor R_{LF1} is required to damp any oscillation on the VCO input that would otherwise occur due to step function changes on the input. A value of R_{LF1} that would give a phase margin of around 45 degrees would be a reasonable starting point.

The main function of the capacitor C_{LF2} is to integrate the effects of the VCO frequency on the VCO input voltage. Typically its value will be about one tenth of C_{LF1}.



TL/F/5182–14

FIGURE 11. Charge Pump Out



TL/F/5182–15

FIGURE 12. Loop Response Components

Figure 12 shows the relevant phase-locked-loop blocks that determine system response, namely the Phase Detector, Filter/Buffer Amplifier, and VCO. The Phase Detector (Phase Comparator and Charge Pump) produces an aggregate output current i which is proportional to the phase difference between the input signal and the VCO signal. The constant (K_1) is $V_{BE}/\pi R$ amps per radian. R is either R_{RATE} or $R_{RATE} \parallel R_{BOOST}$. This aggregate current feeds into or out of the filter impedance (Z), producing a voltage to the VCO that regulates the VCO frequency. The VCO gain constant is 0.4 ω_{VCO}/V_{BE} radians per second per volt. Under steady state conditions, i will be zero and there will be no phase difference between the input signal and the VCO. Any change of input signal will produce a change in VCO frequency that is determined by the loop gain equation. This equation is determined from the gain constants K_1, A and K_2 and the filter v/i response.

The impedance Z of the filter is:

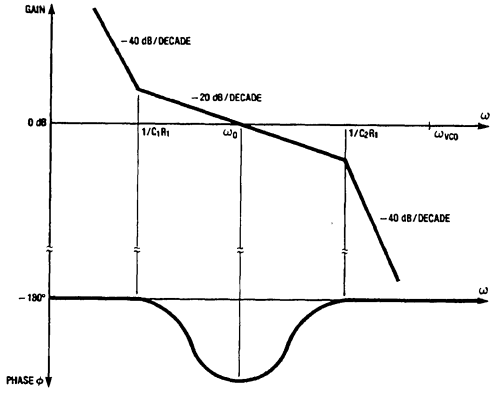
$$\frac{1}{sC_2} \parallel \left(\frac{1}{sC_1} + R_1\right) = \frac{1 + sC_1R_1}{sC_1\left(1 + \frac{C_2}{C_1} + sC_2R_1\right)}$$

If $C_2 \ll C_1$ then the impedance Z approximates to:

$$\frac{1 + sC_1R_1}{sC_1\ (1 + sC_2R_1)}$$

The overall loop gain is then $G(s) = \frac{K_1AK_2}{s} \times \frac{1 + sC_1R_1}{sC_1(1 + sC_2R_1)}$

The desired Bode plot of gain and phase is shown in *Figure 13*, with −20dB/decade slope at ω_O for stability at unity gain.



TL/F/5182–16

FIGURE 13. Bode Plot of Loop Response

If the point of inflexion of the phase curve is at ω_O, (the loop natural frequency and therefore the closed loop bandwidth), then it can be shown that for a phase margin ϕ,

$$C_2R_1 = \frac{1 - \sin\phi}{\omega_O \cos\phi} \text{ sec}$$

$$C_1R_1 = \frac{1}{\omega_O{}^2 C_2R_1} \text{sec}$$

$$\text{and } C_1 = \frac{K_1 A K_2}{\omega_O{}^2} \times \frac{1 + \omega_O C_1R_1}{1 + \omega_O C_2R_1} \text{ F}$$

As an example, if we want the PLL to lock-on within two bytes of preamble in the high tracking rate mode, and the disk data rate is 5Mbits/sec, or one bit every 200ns.

(Thus f_{VCO} = 10MHz)

time to lock = 16 × 0.2μs = 3.2μs

Closed loop bandwidth f_O> (0.3/3.2) MHz or about 100kHz

(the factor 0.3 is a rule of thumb guideline derived from the product of rise time and bandwidth).

Select a bandwidth f_O = 200kHz so that $\omega_O = 2\pi \times 200\text{kHz}$ (giving a ratio of $f_{VCO} / f_O = 50$)

Select a phase margin ϕ between 30° and 70° for stability.

Choose $\phi = 45°$ for optimum response

$$\text{Then } C_2R_1 = \frac{(1 - \sin 45°)}{2\pi \times 200 \times 10^3 \times \cos 45°} = 0.33 \times 10^{-6} \text{ sec}$$

$$\text{and } C_1R_1 = \frac{1}{(2\pi \times 200 \times 10^3)^2 \times 0.33 \times 10^{-6}} = 1.92 \times 10^{-6} \text{ sec}$$

To determine C1, we need to know K_1, A and K_2.

$$K_1 = \frac{V_{BE}}{\pi R} \text{ amps per radian}$$

In the high tracking rate, R = 1.1k ‖ 3.3k = 825Ω for our example from the Charge Pump calculations

$$\text{So } K_1 = \frac{V_{BE}}{\pi \times 825} \text{ amps/radian}$$

the Buffer Amplifier gain A is internally set to 4.0

$$K_2 = \frac{0.4\omega_{VCO}}{V_{BE}} \text{ radians per sec per volt}$$

$$K_2 = \frac{0.4 \times 2\pi \times 10^7}{V_{BE}} \text{ radians per sec per volt}$$

$$\text{so } C_1 = \frac{V_{BE}}{\pi \times 825} \times 4.0 \times \frac{0.4 \times 2\pi \times 10^7}{V_{BE} \times (2\pi \times 200 \times 10^3)^2} \times \frac{1 + (2\pi \times 200 \times 10^3 \times 1.92 \times 10^{-6})}{1 + (2\pi \times 200 \times 10^3 \times 0.33 \times 10^{-6})} \text{ F}$$

The V_{BE} in the K_1 equation cancels with the V_{BE} in the K_2 equation provided good matching is maintained on the DP8460.

Thus C_1 = 5.923 × 10^{-8}F. Select C_1 to be 0.056μF

$$\therefore R_1 = \frac{1.92 \times 10^{-6}}{56000 \times 10^{-12}} \Omega = 34.28\Omega. \text{ Select } R_1 = 33\Omega$$

$$\therefore C_2 = \frac{0.33 \times 10^{-6}}{33} \text{ F} = 10^{-8}\text{F} = 0.01\mu\text{F}. \text{ Select } C_2 = 0.01\mu\text{F}$$

The calculated values are only a guide, the user should then empirically test the loop and determine stability, lock-on time, jitter tolerance, etc.

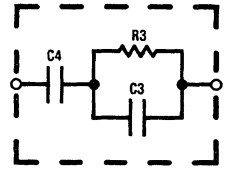
Note that capacitor C_2 affects the amount by which the Charge Pump switching current affects the filter voltage. Obviously as C_2 is increased in value ripple will decrease, but the closer the −40dB/decade slope gets to ω_o on the Bode plot the more unstable the loop will be. Thus if C_2 is made too large the loop will oscillate.

Resistor R_1 determines where the low-frequency end −40dB/decade slope changes into the −20dB/decade slope. The wider the −20dB/decade slope is around unity gain, the more stable the loop becomes. If R_1 is too large it will reduce the impact of C_1, while too small a value will increase instability. The capacitor C_1 strongly effects the response of the loop. Too high a value will slow down the response time, but make it less prone to jitter or frequency shift whereas too low a value will improve response time while tending to react to jitter.

Other filter combinations may be used, other than R_{LF1} in series with C_{LF1}, all in parallel with C_{LF2}. For example the filter shown in *Figure 14* will also perform similarly, and in fact for some systems it will yield superior performance.

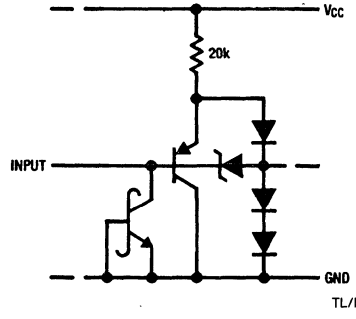
DIGITAL CONNECTIONS TO THE DP8460

Figure 17 shows a connection diagram for the DP8460 in a typical application. All logic inputs and outputs are TTL compatible as shown in *Figures 15* and *16*. The VCO CLOCK output is 74AS compatible and can therefore drive up to 40 74AS (or 74F) inputs, or 10 74S inputs, or 100 74ALS inputs, or 50 of 74LS inputs. All other outputs are 74ALS compatible and so will drive up to 16 74AS inputs, or 4 74S inputs, or 40 74ALS inputs or 20 74LS inputs. All inputs are 74ALS compatible and therefore can be driven easily from any 74 series devices. The raw MFM from the pulse detector in the drive is connected to the ENCODED DATA input. The DELAY DISABLE input determines whether attempting lock-on will begin immediately after READ GATE is set or after 2 bytes. Typically in a hard-sectored drive, READ GATE is set active as the sector pulse appears, meaning a new sector is about to pass under the head. Normally the preamble pattern does not begin immediately, because gap bytes from the preceding sector usually extend just beyond the sector pulse. Allowing 2 bytes to pass after the sector pulse helps ensure that the PLL will begin locking on to preamble, and will not be chasing non-symmetrical gap bits. Attempting to lock-on to a fixed ....1010.... preamble pattern speeds up lock-on, and after another two bytes the PLL will nominally have locked-on. Thus DELAY DISABLE should be set low for this kind of disk drive.



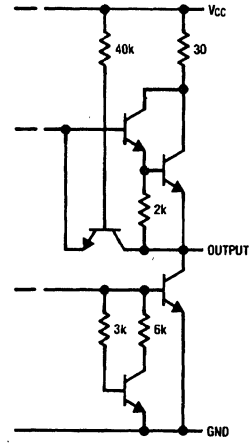
TL/F/5182–17

FIGURE 14. Alternate Loop Filter Configuration



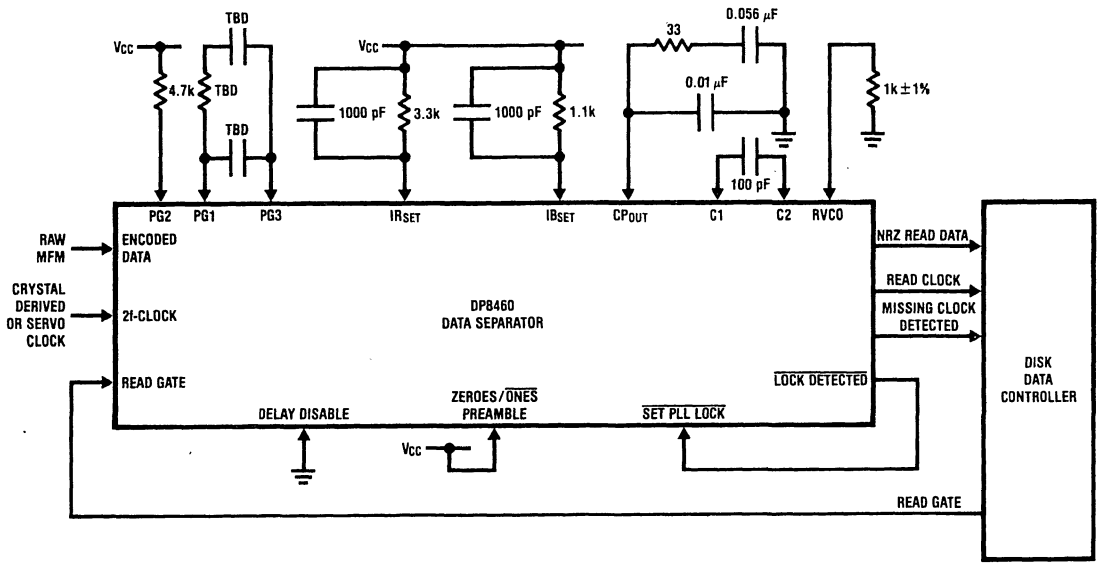
TL/F/5182–18

FIGURE 15. Logic Inputs



TL/F/5182–19

FIGURE 16. Logic Outputs



TL/F/5182–20

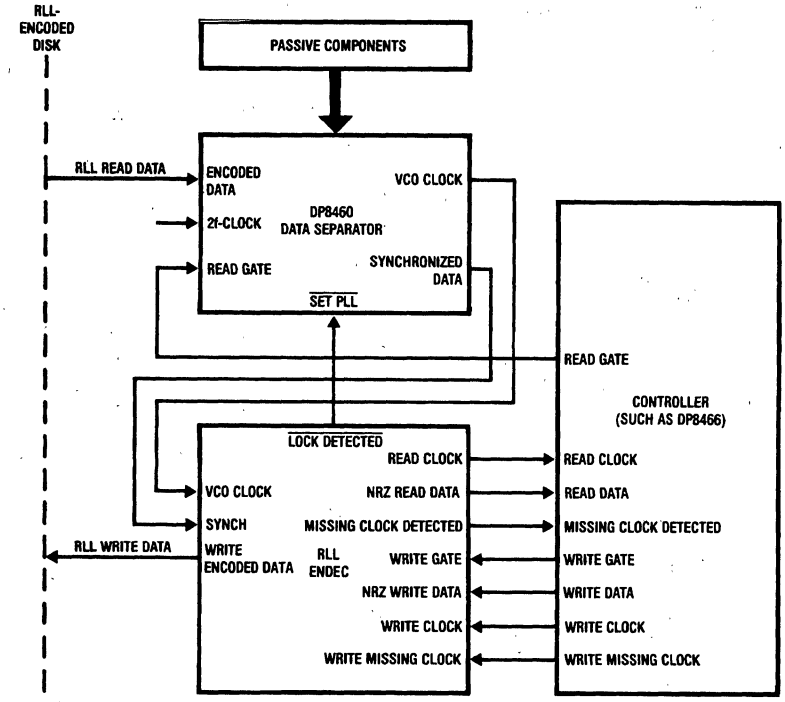
FIGURE 17. Typical Connection to DP8460 for:
1) MFM Data Input, 5Mbit/sec Data Rate
2) 32 Bit Delay to Enable
3) All Zeroes (NRZ) Preamble

For soft sectored drives, the controller normally will not wait for the index pulse before it attempts lock-on, so that READ GATE may go active at any time. Chances are the head will not be over a preamble field and therefore there is no need to wait 2 bytes before attempting lock-on. DELAY DISABLE can therefore be set high. If a non-preamble field is passing by as READ GATE goes active, the DP8460 will not indicate lock, and no data decoding will occur nor will MISSING CLOCK DETECTED go active. Normally, if lock-on has not been achieved after a certain time limit, the controller will de-activate READ GATE and then try again.

For MFM encoded disk drives, the $\overline{\text{LOCK DETECTED}}$ output will be connected back to the $\overline{\text{SET PLL LOCK}}$ input. As the PLL achieves lock-on, the DP8460 will automatically switch to the slower tracking rate and decoded data will appear at the NRZ READ DATA output. Also the READ CLOCK output will switch from half the 2f-clock frequency to the disk data rate frequency. If a delay is required before the changeover occurs, a time delay may be inserted between the two pins.

Some drives have an all-ONES data preamble instead of all-ZEROES and the DP8460 must be set to the type being used before it can properly decode data. The ZEROES/$\overline{\text{ONES}}$ PREAMBLE input selects which preamble type the chip is to lock-on to.

If the drive uses a run-length-limited (RLL) code such as '2, 7', instead of MFM, the phase-locked-loop function of the DP8460 may still be used. *Figure* 18 shows how the DP8460 may be connected to a RLL ENDEC circuit. The RLL ENDEC performs encoding of NRZ data to RLL encoded data, and RLL encoded data back to NRZ data. The RLL ENDEC can use the SYNCHRONIZED DATA output of the DP8460 along with VCO CLOCK to lock-on to the preamble and then decode data. Once lock-on has been detected, the RLL ENDEC can set the $\overline{\text{SET PLL LOCK}}$ input of the DP8460 low so that the tracking rate can be changed.



TL/F/5182–21

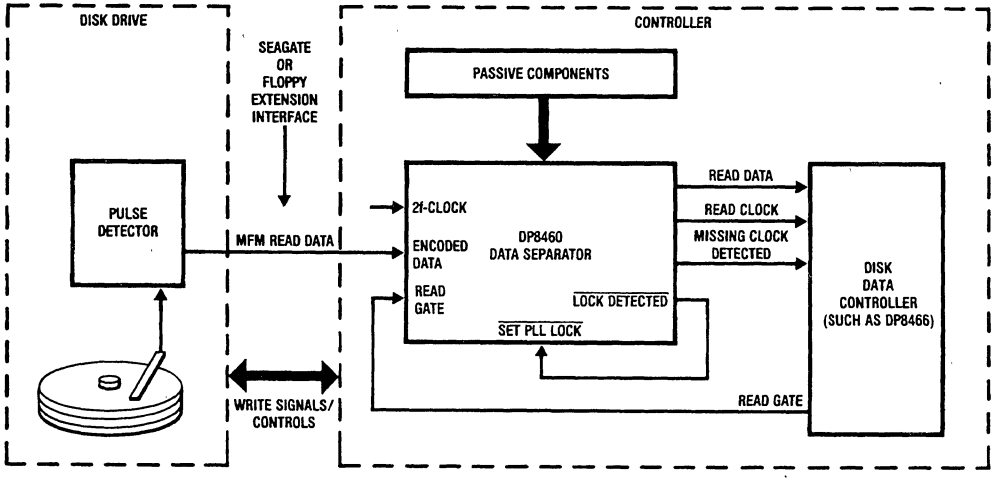
FIGURE 18. DP8460 with Run-Length-Limited (RLL) Codes

APPLICATIONS OF THE DP8460 DATA SEPARATOR

The DP8460 is the first integrated circuit to place on one chip a PLL with features that offer the improved speed and reliability required by the disk industry. Not only does the chip simplify disk system design, but also provides fast lock-on to the incoming preamble. Once locked on, the loop is set into a more stable mode. This inherent loop stability allows for a sizeable amount of jitter on the data stream, such as is encountered in many disk systems. Once in the stable tracking rate, the SYNCHRONIZED DATA output represents the incoming ENCODED DATA and is synchronous with VCO CLOCK. If the disk is MFM encoded, then the chip can decode the synchronized data into NRZ READ DATA and READ CLOCK. These are available as outputs from the chip allowing the NRZ READ DATA to be deserialized using the READ CLOCK.

The DP8460 is capable of operating at up to 25Mbits/sec data rates and so is compatible with a wide assortment of disk drives. The faster data rates of the 8-inch and 14-inch disk drives will mandate the selection of either the DP8460-3 or -2 parts with their narrower window margins on the incoming data stream. This will also be the case when 5¼-inch drives achieve higher data rates. Some 8-inch and 14-inch disk drives incorporate the functions of the DP8460, but use many discrete ICs. In these cases, replacing these components with the DP8460 will offer reduced P.C. board area, lower cost, and improved performance while simplifying circuit testing.

Most 5¼-inch and many 8-inch and 14-inch disk drives manufactured at present do not incorporate any of the functions of the DP8460. This is so primarily because the PLL function is difficult to design and implement, and requires circuitry which covers a large area of the printed circuit card. This is undesirable both from the drive size aspect and from the cost aspect (the cost includes soldering, testing, and adjusting the components). Consequently, most smaller disk drives output MFM encoded data so that the phase-locked-loop and data separation have to be performed by the controller. The DP8460 will therefore replace these functions in controller designs, as shown in *Figure 19*.

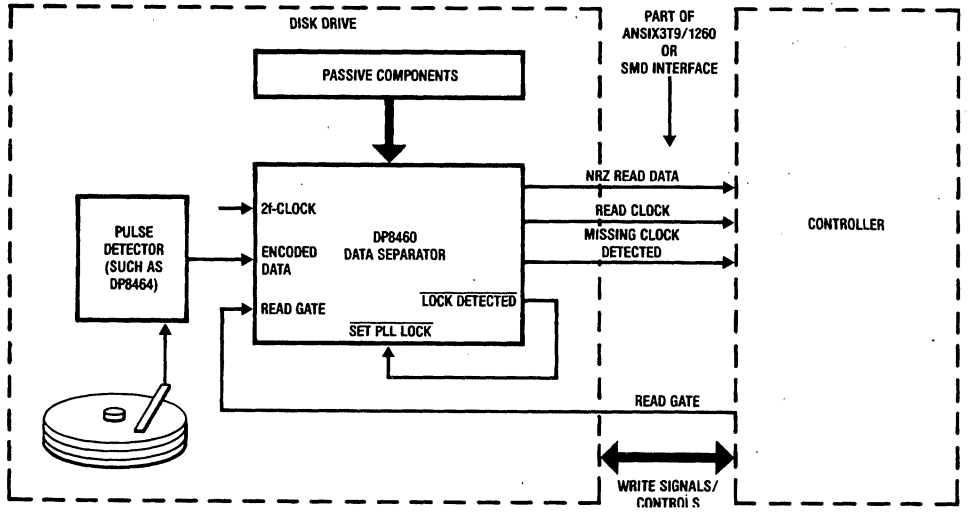


TL/F/5182-22

FIGURE 19. DP8460 in the Controller

System design criteria may now change because the DP8460 is a one-chip solution, requiring only a few external passive components with fixed values. It operates from a +5V supply, consumes about 0.5W, and is housed in a narrow 24-pin package. The circuitry has been designed so that the external resistors and capacitors need not be adjustable; the user chooses the values according to the disk drive requirements. Once selected, they will be fixed for that particular drive type. These features make it possible to transfer these functions to the disk drive, as shown in *Figure 20*. Apart from a slight increase in board area, the advantages outweigh the disadvantages. First, the components selected are fixed for each type of drive and this facilitates the problem of interchangeability of drives. At present, controllers are adjusted to function with each specific drive; with the DP8460 in the drive, component adjustment will no longer be required. Second there is often a problem of reliability of data transfer. Because the MFM data is clock encoded, this signal is susceptible to noise, bit shift, etc. Soft errors will sometimes occur when the incoming disk data bit position is outside the Pulse Gate window as it is being synchronized to the VCO clock in the phase-locked-loop. Obviously, the nearer the PLL is to the MFM source, the less chance there is that errors will occur. Thus placing the DP8460 in the drive will increase the reliability of data transfer within the sysem.

A third advantage is data rate upgrading. Most 5¼-inch drives have 5Mbit/sec data rate because the early drives were made with this data rate. This meant the controllers had to be designed with PLLs which operate at this data rate. It is therefore difficult for drive manufacturers to introduce new drives that are not compatible with existing controllers. Since no new standard data rate has emerged, they must continue to produce drives at this data rate to be compatible with the controllers on the market. With the DP8460 in the drive, and its associated components set for the drive's data rate, it no longer becomes a problem to increase the data rate, assuming the controllers digital circuitry can accommodate the change. This will allow the manufacturers to increase the bit density and therefore the capacity of their drives.



TL/F/5182–23

FIGURE 20. DP8460 in the Disk Drive

National Semiconductor

Disk Support
PRELIMINARY

DP8464 Disk Pulse Detector

General Description

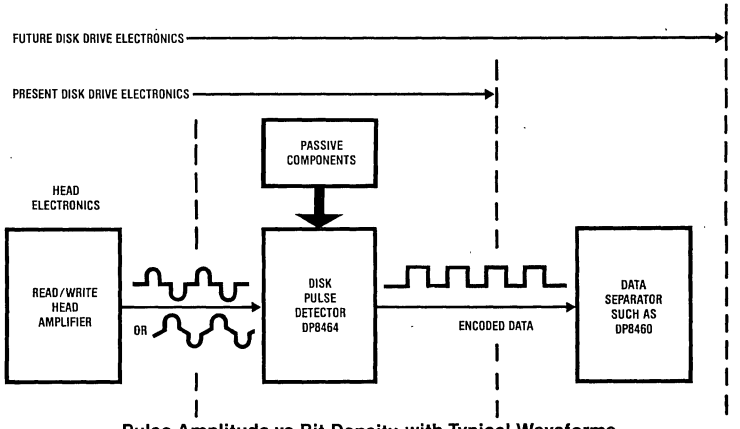
The DP8464 disk pulse detector utilizes analog and digital circuitry to detect amplitude peaks of the signal received from the read/write amplifier fitted in the heads of disk drives. The DP8464 produces a TTL compatible output which, on the positive edge, indicates a signal peak. Electrically, these peaks correspond to 1s or flux reversals on the magnetic medium. The signal received when reading a disk is therefore a series of pulses which alternate in polarity. The disk pulse detector must accurately determine the time positions of these peaks. This task is complicated by variable pulse amplitudes depending on the media type, head position, head type, and read/write amplifier circuit gain. Additionally, as the bit density on the disk increases the amplitude decreases and significant bit interaction occurs resulting in pulse distortion.

The graph below shows how pulse amplitude varies with the number of bits per inch (or recording density). The predominant disk applications are associated with the first two regions on the graph, regions 1 and 2. Typical waveforms received by the pulse detector for regions 1 and 2 operation are shown next to the graph. A region 1 signal is characterized by the waveform returning to the baseline between pulses. A region 2 waveform will go from a tendency to return to the baseline (called shouldering) to almost sinusoidal at the higher frequencies.

The disk pulse detector is fabricated using the advanced Schottky process, and has been designed to function with data rates up to 25 megabits/second. The DP8464 is housed in a standard narrow 24-pin package. Normally, it will be fitted in the disk drive, and its output may be directly connected to the DP8460 data separator.

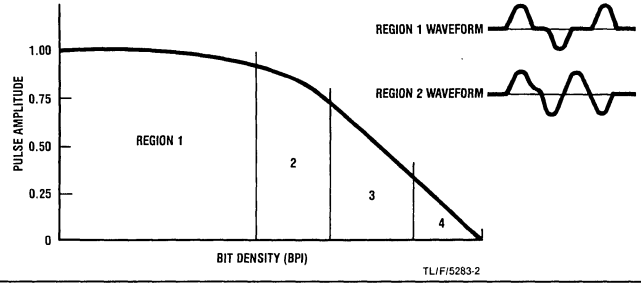
Features

- Connects directly with the disk head read/write amplifier
- Wide input signal amplitude range—from 20 mVpp to 600 mVpp differential
- Data rates up to 25 Mbits/sec
- On-chip wideband differential AGC amplifier, differentiator, comparator gating circuitry, output pulse generator
- Adjustable comparator threshold
- Selectable attack and differentiator capacitors
- Inputs and outputs TTL compatible
- Output may connect directly to the DP8460 data separator
- Standard narrow 24-pin dual-in-line package
- Standard supply: 12V ± 10%



Pulse Amplitude vs Bit Density with Typical Waveforms

TL/F/5283-1



TL/F/5283-2

Functional Description

DETECTOR OPERATION

Region 1 is the high resolution area characterized by a large spread between flux reversals and a definite return to baseline (no signal) between these peaks. Pulses of this type are predominantly found in systems which use thin film heads, plated media and systems which utilize run-length-limited coding techniques (like the 2,7 code) which spread the distance between flux reversals.

The main circuit blocks of the DP8464 are shown in *Figure 1*. The output from the read/write amplifier is fed directly to the amplifier input of the DP8464. This amplifier is a high bandwidth amplifier with automatic gain control (AGC). The amplifier's output voltage is fed back via an external filter to an internal fullwave rectifier and compared against the external voltage on the V_{REF} pin. The AGC circuit adjusts the gain of the amplifier to make the peak to peak differential analog output four times the voltage on V_{REF}. The circuit is designed for a V_{REF} of 1V which produces constant 4V peak to peak differential output for differential input signals ranging from 20 mVpp to 300 mVpp.

The peak detection is performed by feeding the output of the wideband amplifier through an external filter to the differentiator. The differentiator output changes state when the input pulse changes direction, generally this will be at the peaks. However, if the signal exhibits shouldering (the tendency to return to the baseline) as seen in region 1 and the upper part of region 2, the differentiator will also respond to noise near the baseline. To avoid this, the signal is also fed to a comparator which is used to define a level around the baseline. Data detection is prevented when the input is less than this level. The threshold for this comparator is externally set via the SET THRESHOLD pin. The comparator output feeds the hold input of the differentiator. The output of the differentiator then drives the bi-directional one-shot. A 4 Vpp differential output voltage will produce a 1V fullwave rectified signal at the input of the comparator. Therefore, if the voltage on the SET THRESHOLD pin is 0.3V, the input must be larger than ± 300 mV before the differentiator is allowed to trigger the one-shot. This comparator circuit thus acts as a gating channel to prevent any noise near the baseline from contaminating the data. The diff output, encoded data, and comp out are all standard TTL outputs. The pulse width of the encoded data can be adjusted from 20 ns to 200 ns via the set pulse width.

The timing of the gating channel with respect to the differentiator output is critical. If the delay through the comparator is longer than the delay through the differentiator, then the window is not centered around the peak of the waveform and the circuit will not perform optimally. The correct operation is to have the differentiator output switch in the middle of the comparator output waveform. Often, to make the differentiator less sensitive to high frequency noise, an RLC filter will be used in place of the differentiator capacitor. This will increase the delay time through the differentiator. To cancel out the effect of this delay, an external delay can be inserted between comp out and diff hold.

Offset of the differentiator is critical to the performance of the circuit. Offset will cause "pulse pairing" which simply means that every other pulse is delayed. This happens because a positive offset will delay all the positive pulses. This obviously will ruin the encoded data. The DP8464 provides two C_{OFFSET} pins for an external capacitor. This capacitor will bandlimit the differential signal going into offset adjust circuitry in the differentiator. In this way, the differentiator is actively corrected to eliminate the initial offset and drift with temperature and time.

The wideband amplifier output is provided to allow the use of external filters to the differentiator and to the AGC circuit. The filter to the differentiator enables the user to limit the bandwidth for noise considerations. The filter to the AGC circuit allows the user to insert a lead network to prevent the AGC amplifier from responding to frequency induced amplitude changes.

The DP8464 has a READ/WRITE control pin which is used to minimize the effect on the AGC amplifier of a write-to-read transition. This allows a reduction in the size of the track gap on disk. This pin may be connected to the WRITE GATE output of the DP8466 disk data controller.

Functional Description (Continued)

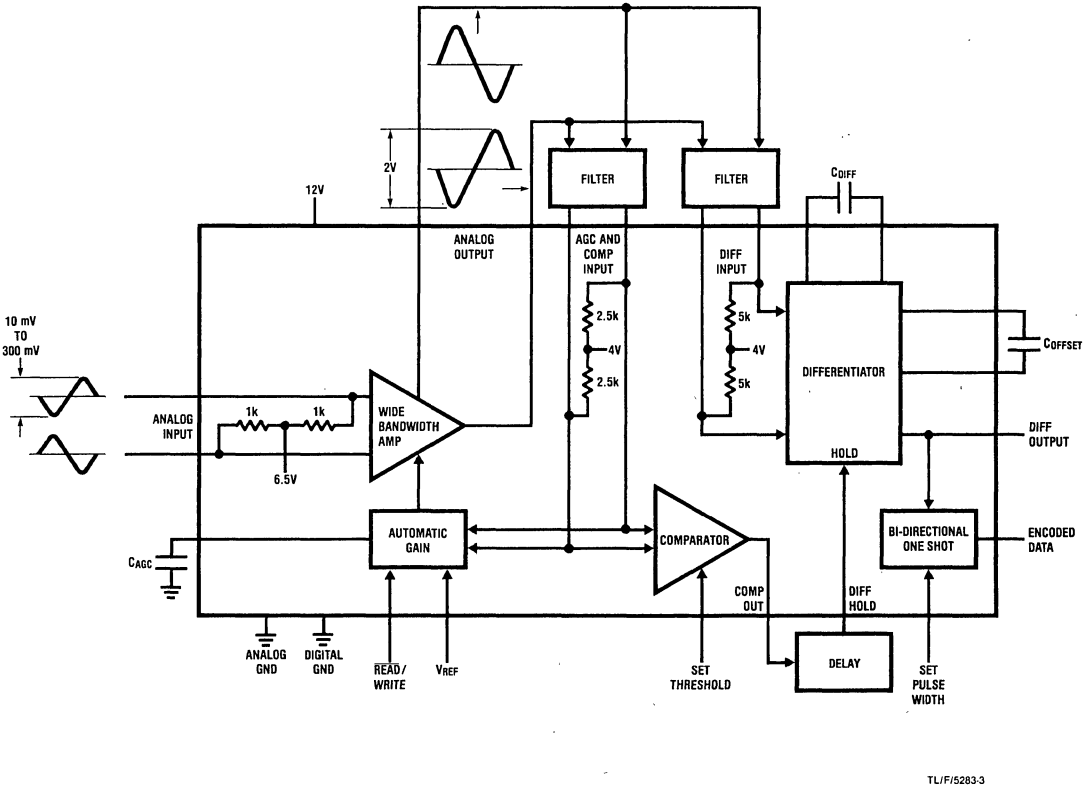


FIGURE 1. Pulse Detector Block Diagram

National Semiconductor

Disk Support
PRELIMINARY

DP8466 Disk Data Controller

General Description

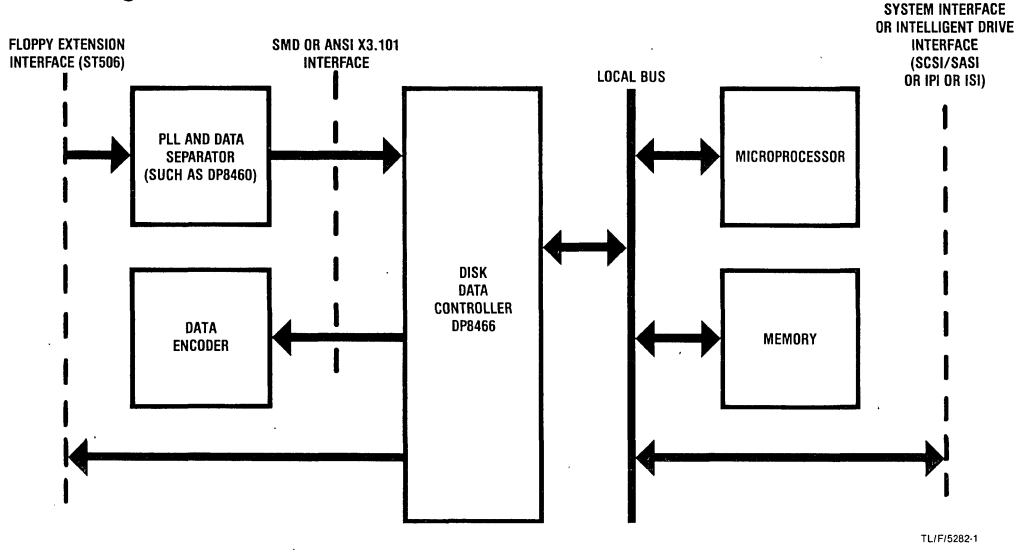
The disk data controller (DDC) performs many of the functions in the data path electronics of either disk controllers or intelligent disk drives. It interfaces between serial data on the disk side and the memory/microprocessor bus on the system side. The primary function of the chip is to correctly identify the selected sector on disk and then transfer the sector's data to or from memory, utilizing a 32-byte (16-word) FIFO buffer with optional DMA control. The 48-pin chip is fabricated using the M^{2}CMOS^{TM} process, which allows complex functions to be implemented with high operating speeds and modest power consumption. Internal gate delays of 2 ns allow the DDC to function with data rates over 24 Mbits/sec, enabling it to be used with all sizes of Winchester and floppy disk drives.

The disk side of the DDC interfaces directly with drives compatible with the ESDI, SMD or ANSI X3.101 interfaces. If the DDC is part of a controller that interfaces directly to the ST506 (floppy extension interface), then the DP8460 data separator may be used and its signals will connect directly to the DDC. The DDC may be part of an intelligent disk drive that has SCSI (SASI) or IPI or ISI compatible interfaces.

Features

- Useable with Winchester, floppy, optical and vertically recorded drives
- Disk data rates up to 24 Mbits/sec
- Meets requirements of all standard disk drive interfaces
- User programmable format
- Compatible with all disk drive sizes, fixed or removable
- Compatible with hard and soft sectored drives
- Single or multiple sector operation
- Independent header and data operations
- Internal CRC or ECC, or external ECC, for header and data
- Internal ECC has programmable polynomial and correction span
- Configurable for disk formatting
- System side interfaces to memory and microprocessor
- Easily controlled by popular 8-bit or 16-bit microprocessors
- 8 or 16-bit wide memory transfers
- Internal data buffering with 32-byte FIFO
- Single channel 32-bit or dual channel 16-bit DMA controller
- Powerful data path diagnostics
- Low power consumption at lower data rates and standby
- Single +5V power supply
- Standard 48-pin DIP

Block Diagram



TL/F/5282-1

M^{2}CMOS^{TM} is a trademark of National Semiconductor Corp.

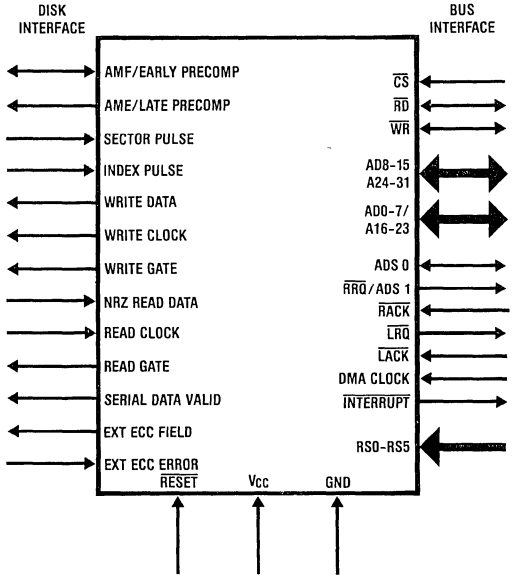
The system side of the DDC may interface directly to the main system bus, or the local bus of a larger system. The DDC has a 16-bit I/O bus and associated microprocessor/DMA handshake signals. The I/O bus is used both for disk data transfers to or from memory (user-selectable for 8 or 16 data bits) and for microprocessor access. The microprocessor may have a multiplexed or separate address and data bus. The DDC has two DMA channels available for memory transfer operations. In a typical low-end system the DDC connects directly to the main system bus, and only one DMA channel is required to output memory addresses. The on-chip DMA issues the address on the I/O bus, followed by the data to be transferred between the DDC and memory. The DDC has variable burst transfer length capability that allows microprocessor usage of the bus during transfer operations. The DDC supports a second mode of DMA capability which is ideal for intelligent disk drives or higher-end systems that use a buffer memory. One DMA channel controls disk-memory transfers, and the second controls memory-system transfers.

To be compatible with the differing needs of these disk drives, the DDC has been configured so that the format and mode of operation are user programmable. The user selects the length and pattern of the preamble, address mark (if required), synch, postamble, and gap of both the ID and data segments of the sector. At system initialization, the microprocessor loads these parameters into the parameter RAM of the DDC. For normal transactions such as reading from or writing to the disk, the desired ID bytes must first be loaded into the DDC, followed by the disk drive command. The DDC can also be configured to format disks.

Extensive diagnostic and interrogation features are provided on-chip. CRC or ECC calculations are performed on both the ID and data segments that pass through the DDC. The ECC code may be an internally generated 32-bit fully programmable ECC code or up to 15 bytes of externally generated ECC code. The DDC contains status and error registers that can be accessed by the microprocessor.

Control functions not in the data path electronics have been omitted to allow for versatility in interfacing to different drive requirements. The drive control signals may be provided by either a dedicated microcontroller or a microprocessor I/O port.

DDC Connection Diagram (48 pins)



TL/F/5282-2

Section 11
Frequency Synthesis

11

Frequency Synthesizers Selection Guide

Product Type	Frequency Bands	Power (mA)	Tuning Resolution	Page No.
PLL FREQUENCY SYNTHESIZERS				
DS8906	AM/FM	160	500 Hz/12.5 kHz	11-4
DS8907	AM/FM	160	10 kHz/25 kHz	11-10
DS8908	AM/FM	160	1 kHz, 9 kHz, 10 kHz, 20 kHz	11-16
AN-335 Digital PLL Synthesis				11-40

Product Type	Divide Modulus	Power (mA)	f_{MAX}	Page No.
HIGH FREQUENCY PRESCALERS				
Single (Fixed) Modulus Dividers				
DS8626	÷ 40	125	120 MHz	11-27
DS8627	÷ 24	7/10	130/225 MHz	11-30
DS8628	÷ 20	7/10	130/225 MHz	11-30
DS8629	÷ 100	135	120 MHz	11-27
DS8621	÷ 64, ÷ 256	32	275 MHz, 1.2 GHz	11-33
Dual-Modulus Dividers				
DS8614	÷ 20/21	7/10	130/225 MHz	11-23
DS8615	÷ 32/33	7/10	130/225 MHz	11-23
DS8616	÷ 40/41	7/10	130/225 MHz	11-23
DS8617	÷ 64/65	7/10	130/225 MHz	11-23
DS8622	÷ 126/128, ÷ 252/256	32	550 MHz, 1.2 GHz	11-36

National Semiconductor

DS8906 AM/FM Digital Phase-Locked Loop Synthesizer

General Description

The DS8906 is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, a 120 MHz ECL/I^2L dual modulus programmable divider, and a 20-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necessary division codes for each frequency, and logic state information for radio function inputs/outputs.

The Colpitts reference oscillator for the PLL operates at 4 MHz. A chain of dividers is used to generate a 500 kHz clock signal for the external controller. Additional dividers generate a 12.5 kHz reference signal for FM and a 500 Hz reference signal for AM/SW. One of these reference signals is selected by the data from the controller for use by the phase comparator. Additional dividers are used to generate a 50 Hz timing signal used by the controller for "time-of-day".

Data is transferred between the frequency synthesizer and the controller via a 3 wire bus system. This consists of a data input line, an enable line, and a clock line. When the enable line is low, data can be shifted from the controller into the frequency synthesizer. When the enable line is transitioned from low to high, data entry is disabled and data present in the shift register is latched.

From the controller 22-bit data stream, the first 2 bits address the device permitting other devices to share the same bus. Of the remaining 20-bit data word, the next 14-bits are used for the PLL divide code. The remaining 6 bits are connected via latches to output pins. These 6 bits can be used to drive radio functions such as gain, mute, FM, AM, LW and SW only. These outputs are open collector. Bit 18 is used internally to select the AM or FM local oscillator input and to select between the 500 Hz and 12.5 kHz reference. A high level at bit 18 indicates FM and a low level indicates AM.

The PLL consists of a 14-bit programmable I^2L divider, an ECL phase comparator, an ECL dual modulus (p/p + 1) prescaler, and a high speed charge pump. The programmable divider divides by (N+1), N being the number loaded into the shift register (bits 1–14 after address). It is clocked by the AM input via an ECL ÷ 7/8 prescaler, or through a ÷ 63/64 prescaler from the FM input. The AM input will work at frequencies up to 8 MHz, while the FM input works up to 120 MHz. The AM band is tuned with a frequency resolution of 500 Hz and the FM band is tuned with a resolution of 12.5 kHz. The buffered AM and FM inputs are self-biased and can be driven directly by the VCO thru a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator.

The high speed charge pump consists of a switchable constant current source (−0.3 mA) and a switchable constant current sink (+0.3 mA). If the VCO frequency is low, the charge pump will source current, and sink current if the VCO frequency is high.

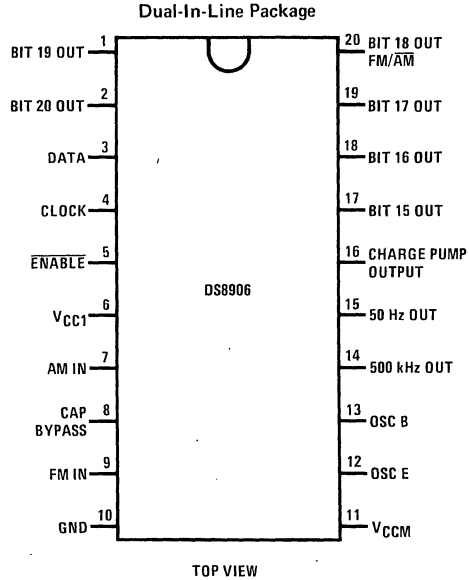
A separate V_{CCM} pin (typically drawing 1.5 mA) powers the oscillator and reference chain to provide controller clocking frequencies when the balance of the PLL is powered down.

Features

- Uses inexpensive 4 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of 12.5 kHz allows usage of 10.7 MHz ceramic filter distribution.
- Serial data entry for simplified control.
- 50 Hz output for "time-of-day" reference with separate low power supply (V_{CCM}).
- 6-open collector buffered outputs for band switching and other radio functions.
- Separate AM and FM inputs. AM input has 15 mV (typical) hysteresis.

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS8906N
See NS Package N20A

Absolute Maximum Ratings (Note 1)

Supply Voltage	
(V_{CC1})	7V
(V_{CCM})	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
V_{CC1}	4.75	5.25	V
V_{CCM}	4.5	6.0	V
Temperature, T_A	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2.1			V
I_{IH}	Logical "1" Input Current	$V_{IN} = V_{CC1}$			0	10	μA
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IL}	Logical "0" Input Current	Data, Clock, and $\overline{ENABLE}$ Inputs, $V_{IN} = 0V$			−5	−25	μA
I_{OH}	Logical "1" Output Current						
	All Bit Outputs, 50 Hz Output	$V_{OH} = 5.25V$				50	μA
	500 kHz Output	$V_{OH} = 2.4V$, $V_{CCM} = 4.5V$				−250	μA
V_{OL}	Logical "0" Output Voltage						
	All Bit Outputs	$I_{OL} = 5$ mA				0.5	V
	50 Hz Output, 500 kHz Output	$I_{OL} = 250$ μA				0.5	V
I_{CC1}	Supply Current (V_{CC1})	All Bit Outputs High			90	160	mA
$I_{CCM(STANDBY)}$	V_{CCM} Supply Current	$V_{CCM} = 6.0V$, All Other Pins Open			1.5	4.0	mA
I_{OUT}	Charge Pump Output Current	$1.2V \leq V_{OUT} \leq V_{CCM} - 1.2V$	Pump Up	−0.10	−0.30	−0.6	mA
		$V_{CCM} \leq 6.0V$	Pump Down	0.10	0.30	0.6	mA
			TRI-STATE®		0	±100	nA
$I_{CCM(OPERATE)}$	V_{CCM} Supply Current	$V_{CCM} = 6.0V$, $V_{CC1} = 5.25V$, All Other Pins Open			2.5	6.0	mA

TRI-STATE® is a registered trademark of National Semiconductor Corp.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r \leq 10$ ns, $t_f \leq 10$ ns

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(MIN)(F)}$	F_{IN} Minimum Signal Input	AM and FM Inputs, $0°C \leq T_A \leq 70°C$			20	100	mV (rms)
$V_{IN(MAX)(F)}$	F_{IN} Maximum Signal Input	AM and FM Inputs, $0°C \leq T_A \leq 70°C$		1000	1500		mV (rms)
$F_{OPERATE}$	Operating Frequency Range	$V_{IN} = 100$ mV rms	AM	0.4		8	MHz
	(Sine Wave Input)	$0°C \leq T_A \leq 70°C$	FM	60		120	MHz
R_{IN} (FM)	AC Input Resistance, FM	120 MHz, $V_{IN} = 100$ mV rms		300			Ω
R_{IN} (AM)	AC Input Resistance, AM	2 MHz, $V_{IN} = 100$ mV rms		1000			Ω
C_{IN}	Input Capacitance, FM and AM	$V_{IN} = 120$ MHz		3	6	10	pF
$t_{\overline{EN}1}$	Minimum $\overline{ENABLE}$ High Pulse Width				625	1250	ns
$t_{\overline{EN}0}$	Minimum $\overline{ENABLE}$ Low Pulse Width				375	750	ns
$t_{CLK\overline{EN}0}$	Minimum Time Before ENABLE Goes Low that CLOCK Must be Low				−50	0	ns
$t_{\overline{EN}0CLK}$	Minimum Time After ENABLE Goes Low that CLOCK Must Remain Low				275	550	ns
$t_{CLK\overline{EN}1}$	Minimum Time Before $\overline{ENABLE}$ Goes High that Last Positive CLOCK Edge May Occur				300	600	ns
t_{EN1CLK}	Minimum Time After ENABLE Goes High Before an Unused Positive CLOCK Edge May Occur				175	350	ns

AC Electrical Characteristics (Continued) $V_{CC} = 5V$, $T_A = 25°C$, $t_r \leq 10$ ns, $t_f \leq 10$ ns

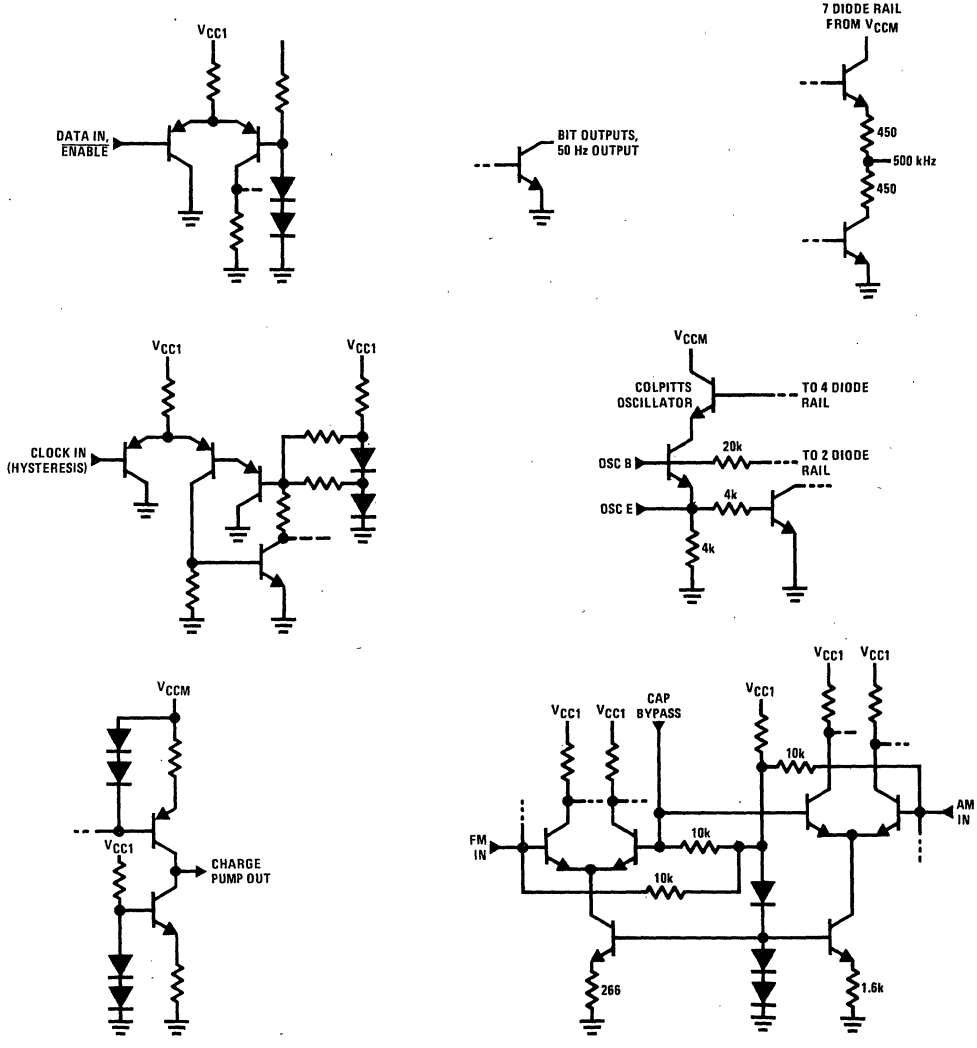
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{CLKH}	Minimum CLOCK High Pulse Width			275	550	ns
t_{CLKL}	Minimum CLOCK Low Pulse Width			400	800	ns
t_{DS}	Minimum DATA Setup Time, Minimum Time Before CLOCK that DATA Must be Valid			150	300	ns
t_{DH}	Minimum DATA Hold Time, Minimum Time After CLOCK that DATA Must Remain Valid			400	800	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS8906.

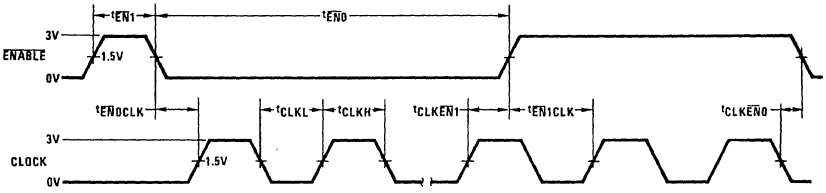
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Schematic Diagrams (DS8906 AM/FM PLL Typical Input/Output Schematics)

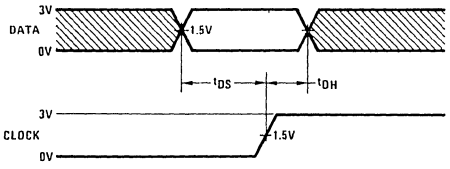


Timing Diagrams *

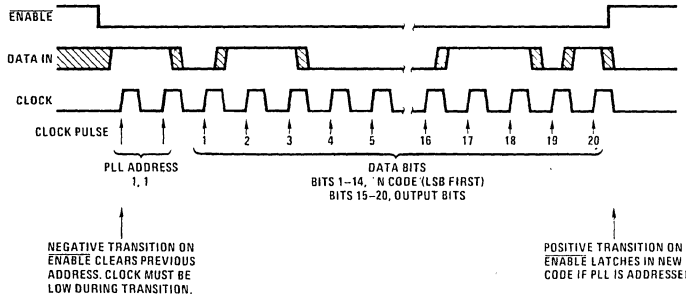
$\overline{\text{ENABLE}}$ vs CLOCK



CLOCK vs DATA



AM/FM Frequency Synthesizer (Scan Mode)



* Timing diagrams are not drawn to scale. Scale within any one drawing may not be consistent, and intervals are defined positive as drawn.

SERIAL DATA ENTRY INTO THE DS8906

Serial information entry into the DS8906 is enabled by a low level on the $\overline{\text{ENABLE}}$ input. One binary bit is then accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low for the specified time preceding and following the negative transition of the $\overline{\text{ENABLE}}$ input.

The first 2 bits accepted following the negative transition of the $\overline{\text{ENABLE}}$ input are interpreted as address. If these address bits are *not* 1,1, *no* further information will be accepted from the DATA inputs, and the internal data latches *will not* be changed when $\overline{\text{ENABLE}}$ returns high.

If these first 2 bits *are* 1,1, then all succeeding bits are *accepted* as data, and are shifted successively into the internal shift register as long as $\overline{\text{ENABLE}}$ remains low.

Any *data* bits preceding the 20th to last bit will be shifted out, and are thus irrelevant. Data bits are counted as any bits following 2 valid (1,1) address bits with the $\overline{\text{ENABLE}}$ low.

When the $\overline{\text{ENABLE}}$ input returns high, any further serial data input is inhibited. Upon this positive transition of the $\overline{\text{ENABLE}}$, the data in the internal shift register is transferred into the internal data latches. Note that until this time, the states of the internal data latches have remained unchanged.

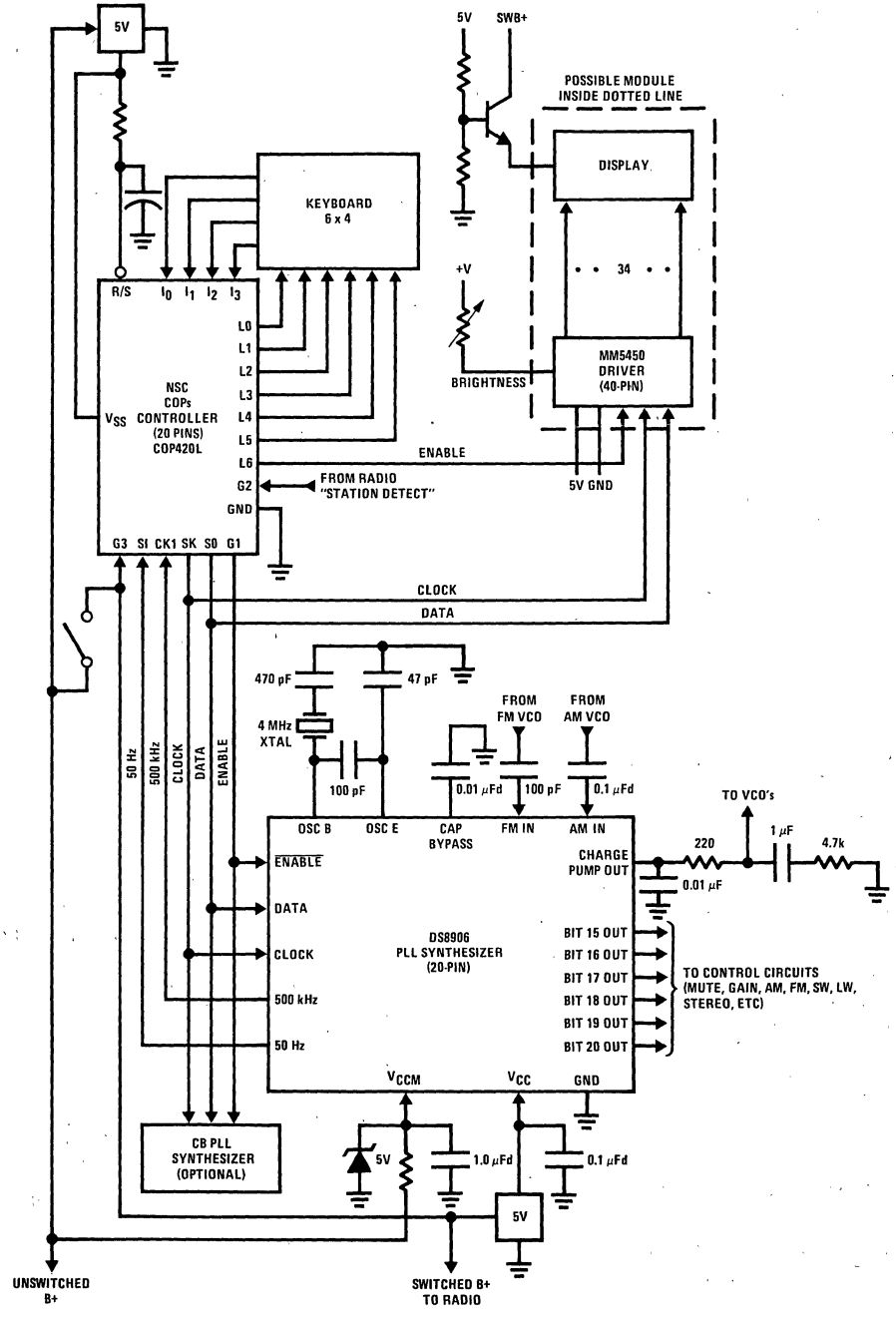
These data bits are interpreted as follows:

DATA BIT POSITION	DATA INTERPRETATION	
Last	Bit 20 Output (Pin 2)	
2nd to Last	Bit 19 Output (Pin 1)	
3rd to Last	Bit 18 Output (FM/$\overline{\text{AM}}$) (Pin 20)	
4th to Last	Bit 17 Output (Pin 19)	
5th to Last	Bit 16 Output (Pin 18)	
6th to Last	Bit 15 Output (Pin 17)	
7th to Last	MSB of N	(2^{13}) ÷N
8th to Last		(2^{12})
9th to Last		(2^{11})
10th to Last		(2^{10})
11th to Last		(2^{9})
12th to Last		(2^{8})
13th to Last		(2^{7})
14th to Last		(2^{6})
15th to Last		(2^{5})
16th to Last		(2^{4})
17th to Last		(2^{3})
18th to Last		(2^{2})
19th to Last		(2^{1})
20th to Last	LSB of N	(2^{0})

Note. The actual divide code is N+1, i.e., the number loaded plus 1.

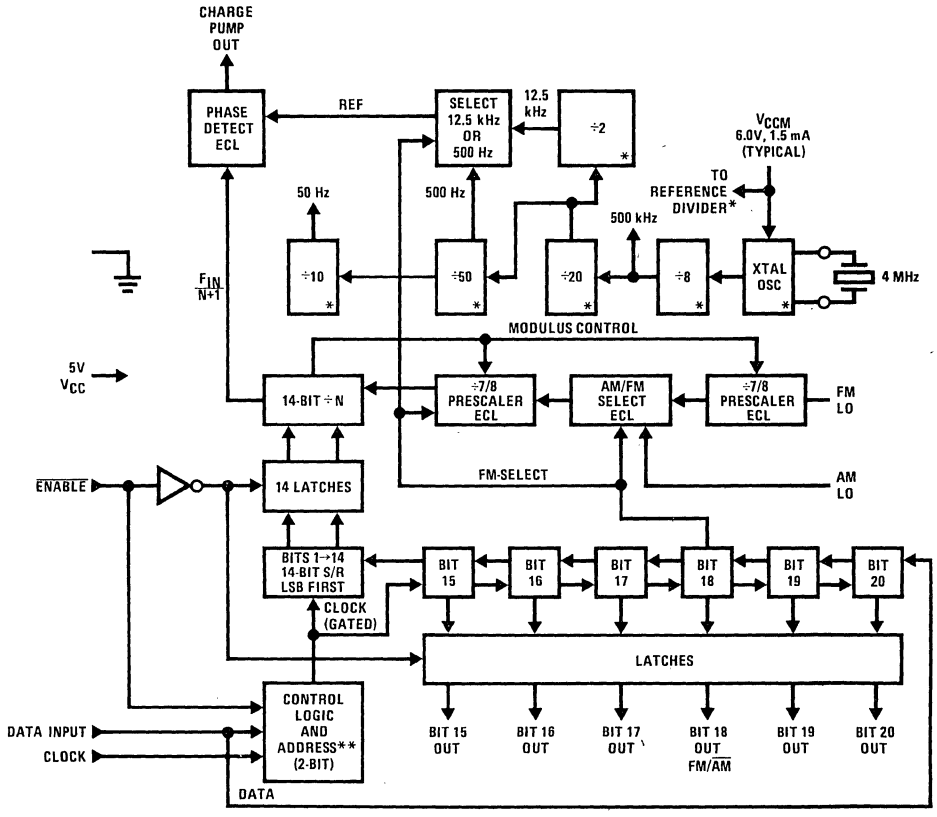
Typical Application Additional application notes are located at the back of section 11.

Electronically Tuned Radio Controller System; Direct Drive LED



Logic Diagram

AM/FM PLL Synthesizer



* Sections operating from V_{CCM} supply
** Address (1, 1)

National Semiconductor

DS8907 AM/FM Digital Phase-Locked Loop Frequency Synthesizer

General Description

The DS8907 is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, a 120 MHz ECL/I^2L dual modulus programmable divider, and an 18-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necessary division codes for each frequency, and logic state information for radio function inputs/outputs.

The Colpitts reference oscillator for the PLL operates at 4 MHz. A chain of dividers is used to generate a 500 kHz clock signal for the external controller. Additional dividers generate a 25 kHz reference signal for FM and a 10 kHz reference signal for AM. One of these reference signals is selected by the data from the controller for use by the phase comparator.

Data is transferred between the frequency synthesizer and the controller via a 3 wire bus system. This consists of a data input line, an enable line, and a clock line. When the enable line is low, data can be shifted from the controller into the frequency synthesizer. When the enable line is transitioned from low to high, data entry is disabled and data present in the shift register is latched.

From the controller 20-bit data stream, the first 2 bits address the device permitting other devices to share the same bus. Of the remaining 18-bit data word, the next 13 bits are used for the PLL divide code. The remaining 5 bits are connected via latches to output pins. These 5 bits can be used to drive radio functions such as gain, mute, FM, AM and stereo only. These outputs are open collector. Bit 16 is used internally to select the AM or FM local oscillator input and to select between the 10 kHz and 25 kHz reference. A high level at bit 16 indicates FM and a low level indicates AM.

The PLL consists of a 13-bit programmable I^2L divider, an ECL phase comparator, an ECL dual modulus (p/p+1) prescaler, and a high speed charge pump. The programmable divider divides by (N+1), N being the number loaded into the shift register (bits 1–13 after address). It is clocked by the AM input via an ECL ÷ 7/8 prescaler, or through a ÷ 63/64 prescaler from the FM input. The AM input will work at frequencies up to 15 MHz, while the FM input works up to 120 MHz. The AM band is tuned with a frequency resolution of 10 kHz and the FM band is tuned with a resolution of 25 kHz. The buffered AM and FM inputs are self biased and can be driven directly by the VCO through a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator. The high speed charge pump consists of a switchable constant current source (–0.3 mA) and a switchable constant current sink (+0.3 mA). If the VCO frequency is low, the charge pump will source current, and sink current if the VCO frequency is high. When using an AFC the charge pump output may be forced into TRI-STATE® by applying a low level to the charge pump enable input.

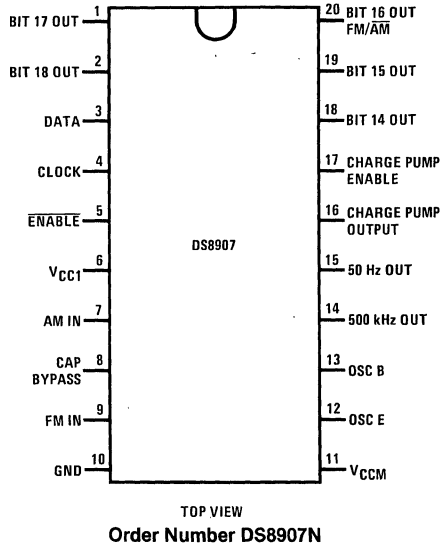
A separate V_{CCM} pin (typically drawing 1.5 mA) powers the oscillator and reference chain to provide controller clocking frequencies when the balance of the PLL is powered down.

Features

- Uses inexpensive 4 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of 25 kHz allows usage of 10.7 MHz ceramic filter distribution
- Serial data entry for simplified control
- 50 Hz output for "time-of-day" reference driven from separate low power V_{CCM}
- 5-open collector buffered outputs for controlling various radio functions
- Separate AM and FM inputs. AM input has 15 mV (typical) hysteresis

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS8907N
See NS Package N20A

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Note 1)

Supply Voltage	
(V_{CC1})	7V
(V_{CCM})	7V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
V_{CC1}	4.75	5.25	V
V_{CCM}	4.5	6.0	V
Temperature, T_A	0	70	°C

DC Electrical Characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2.1			V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.7V			0	10	μA
V_{IL}	Logical "0" Input Voltage					0.7	V
I_{IL}	Logical "0" Input Current	Data, Clock, and $\overline{\text{ENABLE}}$ Inputs, V_{IN} = 0V			−5	−25	μA
I_{IL}	Logical "0" Input Current	Charge Pump Enable, V_{IN} = 0V			−250	−450	μA
I_{OH}	Logical "1" Output Current						
	All Bit Outputs, 50 Hz Output	V_{OH} = 5.25V				50	μA
	500 kHz Output	V_{OH} = 2.4V, V_{CCM} = 4.5V				−250	μA
V_{OL}	Logical "0" Output Voltage						
	All Bit Outputs	I_{OL} = 5 mA				0.5	V
	50 Hz Output, 500 kHz Output	I_{OL} = 250 μA				0.5	V
I_{CC1}	Supply Current (V_{CC1})	All Bit Outputs High			90	160	mA
$I_{CCM(STANDBY)}$	V_{CCM} Supply Current	V_{CCM} = 6.0V, All Other Pins Open			1.5	4.0	mA
I_{OUT}	Charge Pump Output Current	1.2V ≤ V_{OUT} ≤ V_{CCM} − 1.2V, V_{CCM} ≤ 6.0V	Pump Up	−0.10	−0.30	−0.6	mA
			Pump Down	0.10	0.30	0.6	mA
			TRI-STATE®		0	±100	nA
$I_{CCM(OPERATE)}$	V_{CCM} Supply Current	V_{CCM} = 6.0V, V_{CC1} = 5.25V, All Other Pins Open			2.5	6.0	mA

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, $t_r \leq 10$ ns, $t_f \leq 10$ ns

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(MIN)(F)}$	F_{IN} Minimum Signal Input	AM and FM Inputs, 0°C ≤ T_A ≤ 70°C			20	100	mV (rms)
$V_{IN(MAX)(F)}$	F_{IN} Maximum Signal Input	AM and FM Inputs, 0°C ≤ T_A ≤ 70°C		1000	1500		mV (rms)
$F_{OPERATE}$	Operating Frequency Range (Sine Wave Input)	V_{IN} = 100 mV rms, 0°C ≤ T_A ≤ 70°C	AM	0.4		8	MHz
			FM	60		120	MHz
R_{IN} (FM)	AC Input Resistance, FM	120 MHz, V_{IN} = 100 mV rms		300			Ω
R_{IN} (AM)	AC Input Resistance, AM	2 MHz, V_{IN} = 100 mV rms		1000			Ω
C_{IN}	Input Capacitance, FM and AM	V_{IN} = 120 MHz		3	6	10	pF
$t_{\overline{EN}1}$	Minimum $\overline{\text{ENABLE}}$ High Pulse Width				625	1250	ns
$t_{\overline{EN}0}$	Minimum $\overline{\text{ENABLE}}$ Low Pulse Width				375	750	ns
$t_{CLK\overline{EN}0}$	Minimum Time Before ENABLE Goes Low that CLOCK Must be Low				−50	0	ns
$t_{\overline{EN}0CLK}$	Minimum Time After ENABLE Goes Low that CLOCK Must Remain Low				275	550	ns
$t_{CLK\overline{EN}1}$	Minimum Time Before $\overline{\text{ENABLE}}$ Goes High that Last Positive CLOCK Edge May Occur				300	600	ns

AC Electrical Characteristics (Continued) V_{CC} = 5V, T_A = 25°C, $t_r \leq 10$ ns, $t_f \leq 10$ ns

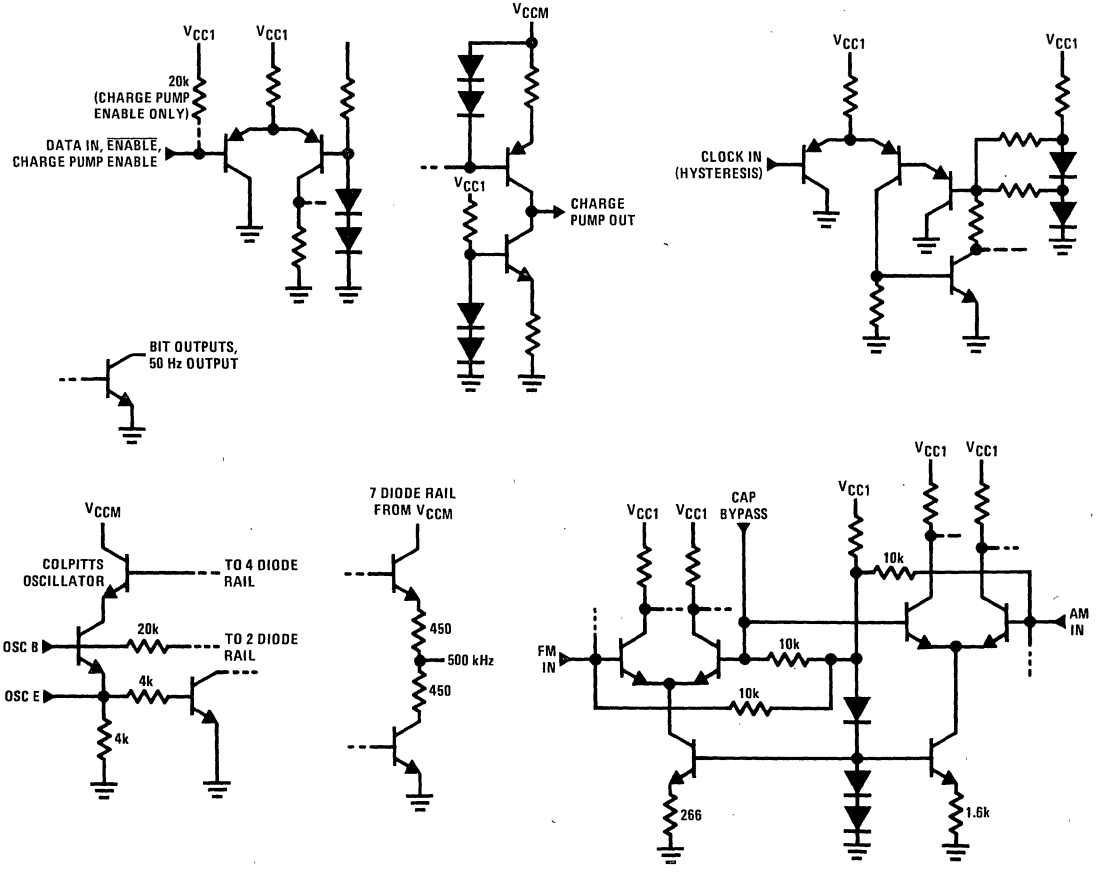
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{EN1CLK}	Minimum Time After ENABLE Goes High Before an Unused Positive CLOCK Edge May Occur			175	350	ns
t_{CLKH}	Minimum CLOCK High Pulse Width			275	550	ns
t_{CLKL}	Minimum CLOCK Low Pulse Width			400	800	ns
t_{DS}	Minimum DATA Setup Time, Minimum Time Before CLOCK that DATA Must be Valid			150	300	ns
t_{DH}	Minimum DATA Hold Time, Minimum Time After CLOCK that DATA Must Remain Valid			400	800	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

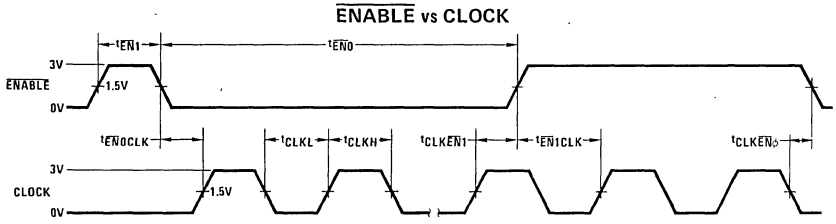
Note 2: Unless otherwise specified min/max limits apply across the −40°C to +85°C temperature range for the DS8907.

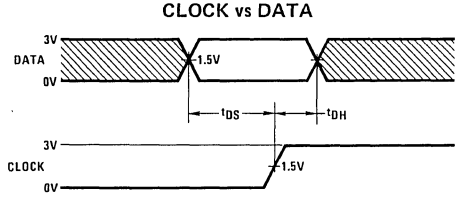
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

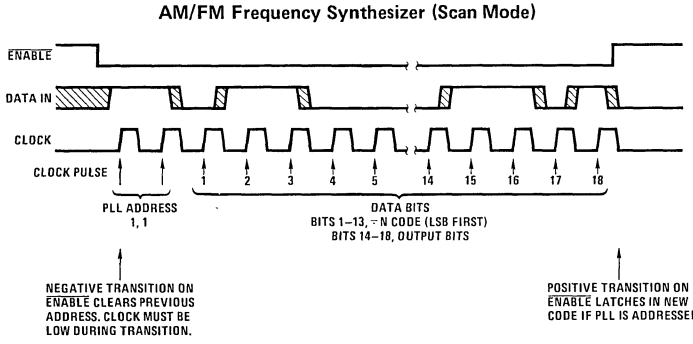
Schematic Diagrams (DS8907 AM/FM PLL Typical Input/Output Schematics)



Timing Diagrams*







*Timing diagrams are not drawn to scale. Scale within any one drawing may not be consistent, and intervals are defined positive as drawn.

SERIAL DATA ENTRY INTO THE DS8907

Serial information entry into the DS8907 is enabled by a low level on the ENABLE input. One binary bit is then accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low for the specified time preceding and following the negative transition of the ENABLE input.

The first two bits accepted following the negative transition of the ENABLE input are interpreted as address. If these address bits are *not* 1,1, *no* further information will be accepted from the DATA inputs, and the internal data latches *will not* be changed when ENABLE returns high.

If these first two bits *are* 1,1, then all succeeding bits are *accepted* as data, and are shifted successively into the internal shift register as long as ENABLE remains low.

Any data bits preceding the 18th to last bit will be shifted out, and thus are irrelevent. Data bits are counted as any bits *following* two valid address bits (1,1) with the ENABLE low, When the ENABLE input returns high, any further serial data entry is inhibited. Upon this positive transition, the data in the internal shift register is transferred into the internal data latches. Note that until this time, the states of the internal data latches have remained unchanged.

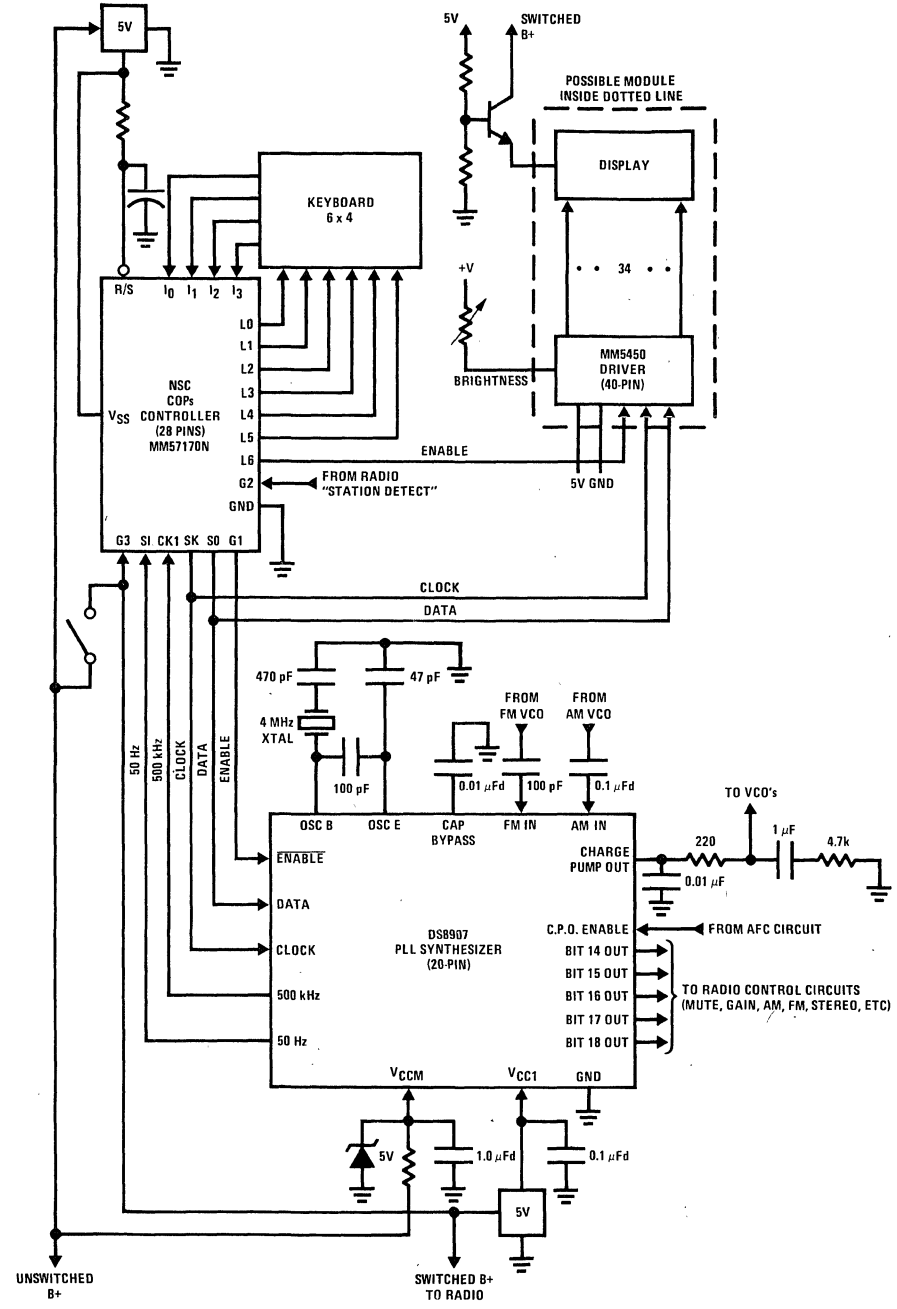
These data bits are interpreted as follows:

DATA BIT POSITION	DATA INTERPRETATION	
Last	Bit 18 Output (Pin 2)	
2nd to Last	Bit 17 Output (Pin 1)	
3rd to Last	Bit 16 Output (FM/$\overline{AM}$) (Pin 20)	
4th to Last	Bit 15 Output (Pin 19)	
5th to Last	Bit 14 Output (Pin 18)	
6th to Last	MSB of ÷N (2^{12})	÷N
7th to Last	(2^{11})	
8th to Last	(2^{10})	
9th to Last	(2^{9})	
10th to Last	(2^{8})	
11th to Last	(2^{7})	
12th to Last	(2^{6})	
13th to Last	(2^{5})	
14th to Last	(2^{4})	
15th to Last	(2^{3})	
16th to Last	(2^{2})	
17th to Last	(2^{1})	
18th to Last	LSB of ÷N (2^{0})	

Note. The actual divide code is N+1, ie., the number loaded plus 1.

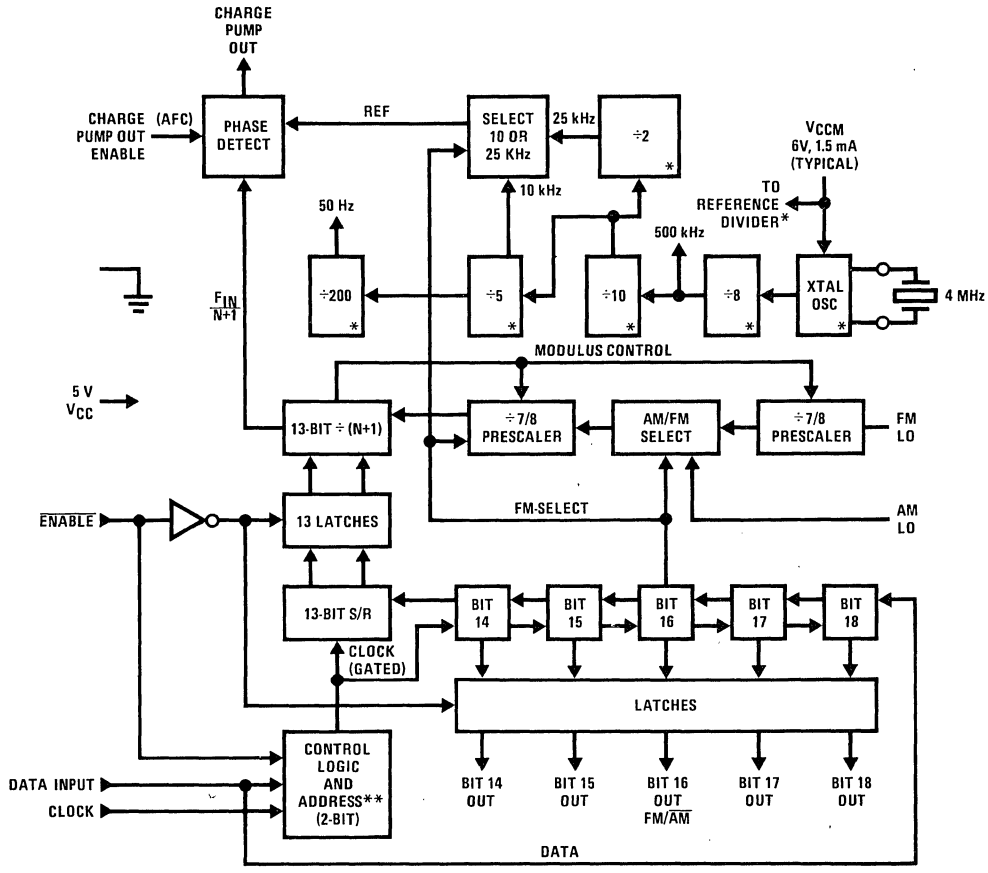
Typical Application Additional application notes are located at the back of section 11.

Electronically Tuned Radio Controller System; Direct Drive LED



Logic Diagram

AM/FM PLL/Synthesizer (Serial Data 20-Pin Package)



* Sections operating from V_{CCM} supply.

** Address (1, 1)

National Semiconductor

DS8908 AM/FM Digital Phase-Locked Loop Frequency Synthesizer

General Description

The DS8908 is a PLL synthesizer designed specifically for use in AM/FM radios. It contains the reference oscillator, a phase comparator, a charge pump, an operational amplifier, a 120 MHz ECL/I^2L dual modulus programmable divider, and a 19-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necessary division codes for each frequency, and logic state information for radio function inputs/outputs.

A 3.96 MHz pierce oscillator and divider chain generate a 1.98 MHz external controller clock, a 20 kHz, 10 kHz, 9 kHz, and 1 kHz reference signals, and a 50 Hz time-of-day signal. The oscillator and divider chain are sourced by the V_{CCM} pin thus providing a low power controller clock drive and time-of-day indication when the balance of the PLL is powered down.

The 21-bit serial data stream is transferred between the frequency synthesizer and the controller via a 3-wire bus system comprised of a data line, a clock line, and an enable line.

The first 2 bits in the serial data stream address the synthesizer thus permitting other devices such as display drivers to share the same bus. The next 14 bits are used for the PLL (N + 1) divide code. The 15th bit is used internally to select the AM or FM local oscillator input. A high level on this bit enables the FM input and a low level enables the AM input. The 16th and 17th bits are used to select one of the 4 reference frequencies. The 18th and 19th bits are connected via latches to open collector outputs. These outputs can be used to drive radio functions such as gain, mute, AM, FM, or charge pump current source levels.

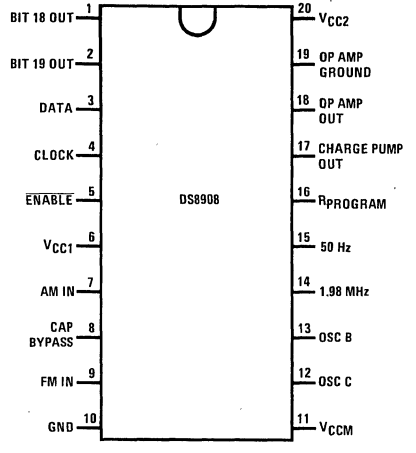
The PLL consists of a 14-bit programmable I^2L divider, an ECL phase comparator, an ECL dual modulus (p/p + 1) prescaler, a high speed charge pump, and an operational amplifier. The programmable divider divides by (N + 1), N being the number loaded into the shift register. The programmable divider is clocked through a ÷7/8 prescaler by the AM input or through a ÷63/64 prescaler by the FM input. The AM input will work at frequencies up to 15 MHz, while the FM input works up to 120 MHz. The VCO can be tuned with a frequency resolution of either 1 kHz, 9 kHz, 10 kHz, or 20 kHz.The buffered AM and FM inputs are self-biased and can be driven directly by the VCO through a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator. The high speed charge pump consists of a switchable constant current source and sink. The charge pump can be programmed to deliver from 75 μA to 750 μA of constant current by connection of an external resistor from pin $R_{PROGRAM}$ to ground or the open collector bit outputs. Connection of programming resistors to the bit outputs enables the controller to adjust the loop gain for the particular reference frequency selected. The charge pump will source current if the VCO frequency is high and sink current if the VCO frequency is low. The low noise operational amplifier provided has a high impedance JFET input and a large output voltage range. The op amp's negative input is common with the charge pump output and its positive input is internally biased.

Features

- Uses inexpensive 3.96 MHz reference crystal
- F_{IN} capability greater than 120 MHz allows direct synthesis at FM frequencies
- FM resolution of either 10 kHz or 20 kHz allows usage of 10.7 MHz ceramic filter distribution
- Serial data entry for simplified control
- 50 Hz output for time-of-day reference driven from separate low power V_{CCM}
- 2 open collector buffered outputs for controlling various radio functions or loop gain
- Separate AM and FM inputs; AM input has 15 mV (typical) hysteresis
- Programmable charge pump current sources enable adjustment of system loop gain
- Operational amplifier provides high impedance load to charge pump output and a wide voltage range for the VCO input

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number DS8908N
See NS Package N20A

Absolute Maximum Ratings (Note 1)

Supply Voltage	
(V_{CC1})(V_{CCM})	7V
(V_{CC2})	17V
Input Voltage	7V
Output Voltage	7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
V_{CC1}	4.5	5.5	V
V_{CC2}	V_{CC1} + 1.5	15.0	V
V_{CCM}	3.5	5.5	V
Temperature, T_A	−40	+85	°C

DC Electrical Characteristics (Notes 2 and 3)

	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	Logical "1" Input Voltage			2.0			V
I_{IH}	Logical "1" Input Current	$V_{IN} = 2.7V$			0	10	μA
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IL}	Logical "0" Input Current	Data, Clock, and $\overline{\text{ENABLE}}$ Inputs, $V_{IN} = 0V$			−5	−25	μA
I_{OH}	Logical "1" Output Current						
	All Bit Outputs, 50 Hz Output	$V_{OH} = 5.5V$				50	μA
	1.98 MHz Output	$V_{OH} = 2.4V$, $V_{CCM} = 4.5V$				−250	μA
V_{OL}	Logical "0" Output Voltage						
	All Bit Outputs	$I_{OL} = 5$ mA				0.5	V
	50 Hz Output, 1.98 MHz Output	$I_{OL} = 250$ μA				0.5	V
	1.98 MHz Output	$I_{OL} = 20$ μA, $T_A > 70°C$				0.3	V
		$I_{OL} = 20$ μA, $T_A \leq 70°C$				0.4	V
I_{CC1}	Supply Current (V_{CC1})	All Bit Outputs High				160	mA
I_{CCM}	V_{CCM} Supply Current	$V_{CCM} = 5.5V$, All Other Pins Open			2.5	4.0	mA
I_{OUT}	Charge Pump Output Current	$3.33k \leq R_{PROG} \leq 33.3k$	Pump Up	−20	I_{PROG}	+20	%
		I_{OUT} Measured Between	Pump Down	−20	I_{PROG}	+20	%
		Pin 17 and Pin 18	TRI-STATE®		0	±250	nA
		$I_{PROG} = V_{CC1}/2\ R_{PROG}$					
I_{CC2}	V_{CC2} Supply Current	$V_{CCM} = 5V$, $V_{CC1} = 5.5V$, $V_{CC2} = 15V$ All Other Pins Open			6.7	11	mA
OP_{VOH}	Op Amp Minimum High Level	$V_{CC1} = 4.5V$, $I_{OH} = -750$ μA		$V_{CC2} - 0.4$			V
OP_{VOL}	Op Amp Maximum Low Level	$V_{CC1} = 5.5V$, $I_{OL} = 750$ μA				0.6	V
CPO_{BIAS}	Charge Pump Bias Voltage Delta	CPO Shorted to Op Amp Output CPO = TRI-STATE Op Amp I_{OL}: 750 μA vs −750 μA				100	mV

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r \leq 10$ ns, $t_f \leq 10$ ns

	Parameter	Conditions		Min	Typ	Max	Units
$V_{IN(MIN)(F)}$	F_{IN} Minimum Signal Input	AM and FM Inputs, $-40°C, \leq T_A \leq 85°C$			20	100	mV(rms)
$V_{IN(MAX)(F)}$	F_{IN} Maximum Signal Input	AM and FM Inputs, $-40°C \leq T_A \leq 85°C$		1000	1500		mV(rms)
$F_{OPERATE}$	Operating Frequency Range	$V_{IN} = 100$ mV rms	AM	0.5		15	MHz
	(Sine Wave Input)	$-40°C \leq T_A \leq 85°C$	FM	80		120	MHz
R_{IN} (FM)	AC Input Resistance, FM	120 MHz, $V_{IN} = 100$ mV rms		600			Ω
R_{IN} (AM)	AC Input Resistance, AM	15 MHz, $V_{IN} = 100$ mV rms		1000			Ω
C_{IN}	Input Capacitance, FM and AM	$V_{IN} = 120$ MHz (FM), 15 MHz (AM)		3	6	10	pF
t_{EN1}	Minimum ENABLE High Pulse Width				625	1250	ns

TRI-STATE® is a registered trademark of National Semiconductor Corp.

AC Electrical Characteristics (Continued) $V_{CC} = 5V$, $T_A = 25°C$, $t_r \leq 10$ ns, $t_f \leq 10$ ns

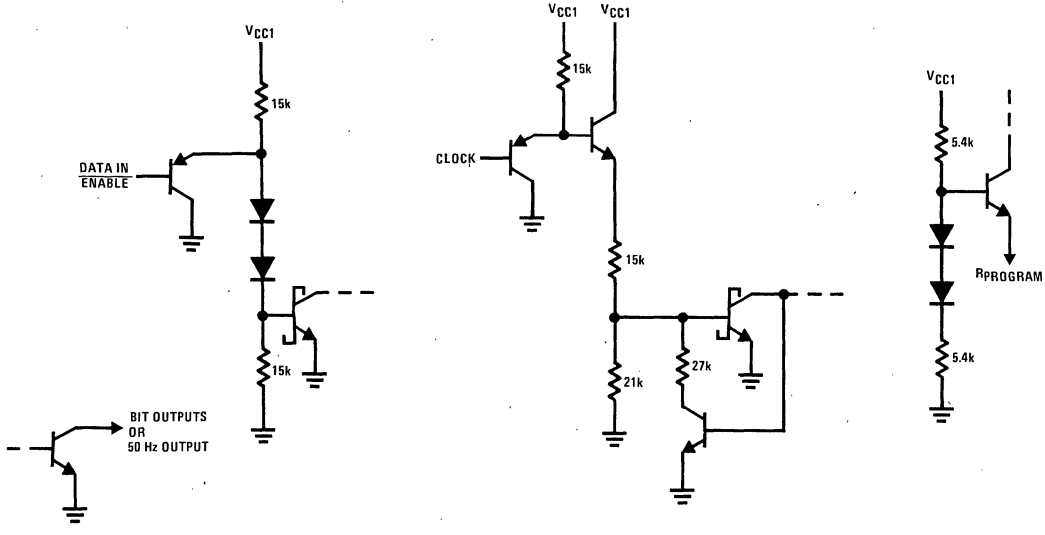
Parameter		Conditions	Min	Typ	Max	Units
$t_{\overline{EN}0}$	Minimum $\overline{\text{ENABLE}}$ Low Pulse Width			375	750	ns
$t_{CLK\overline{EN}0}$	Minimum Time Before $\overline{\text{ENABLE}}$ Goes Low that CLOCK Must be Low			−50	0	ns
$t_{\overline{EN}0CLK}$	Minimum Time After $\overline{\text{ENABLE}}$ Goes Low that CLOCK Must Remain Low			275	550	ns
$t_{CLK\overline{EN}1}$	Minimum Time Before $\overline{\text{ENABLE}}$ Goes High that Last Positive CLOCK Edge May Occur			300	600	ns
$t_{\overline{EN}1CLK}$	Minimum Time After $\overline{\text{ENABLE}}$ Goes High Before an Unused Positive CLOCK Edge May Occur			175	350	ns
t_{CLKH}	Minimum CLOCK High Pulse Width			275	550	ns
t_{CLKL}	Minimum CLOCK Low Pulse Width			400	800	ns
t_{DS}	Minimum DATA Set-Up Time, Minimum Time Before CLOCK that DATA Must be Valid			150	300	ns
t_{DH}	Minimum DATA Hold Time, Minimum Time After CLOCK that DATA Must Remain Valid			400	800	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

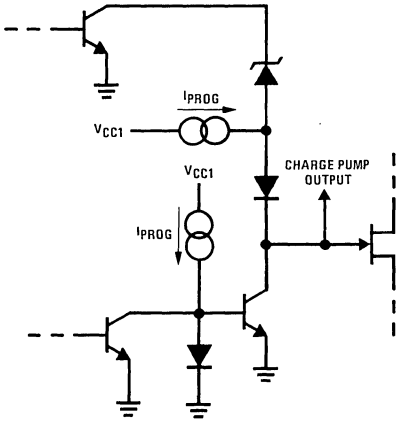
Note 2: Unless otherwise specified min/max limits apply across the −40°C to +85°C temperature range for the DS8908.

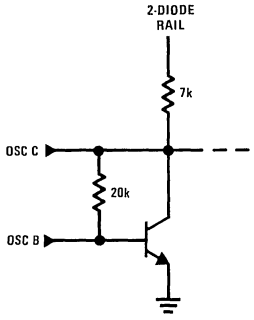
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

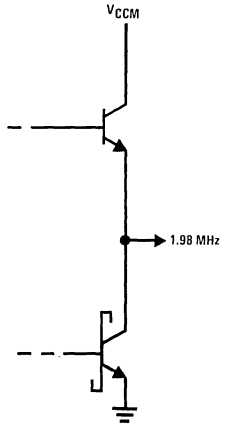
Schematic Diagrams (DS8908 AM/FM PLL Typical Input/Output Schematics)

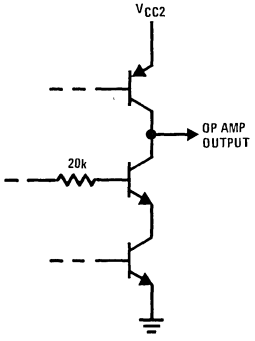


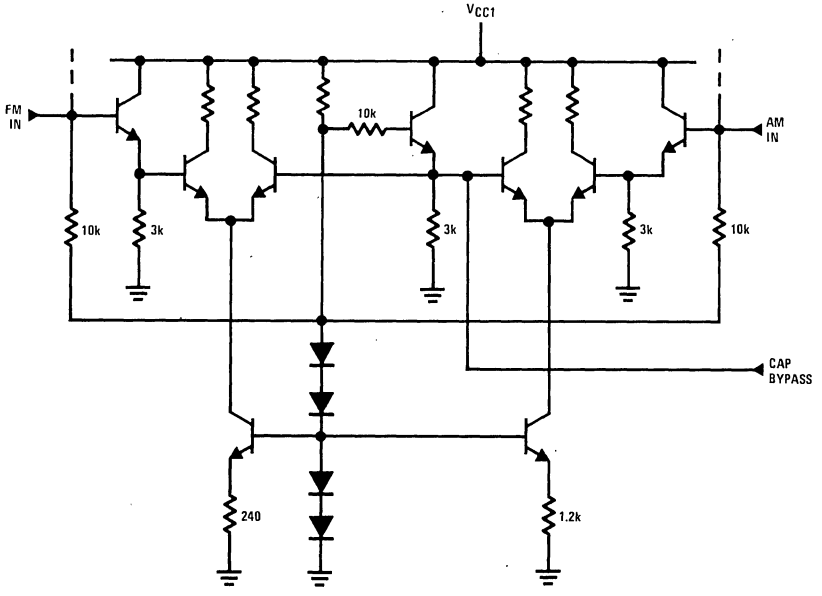
Schematic Diagrams (Continued)



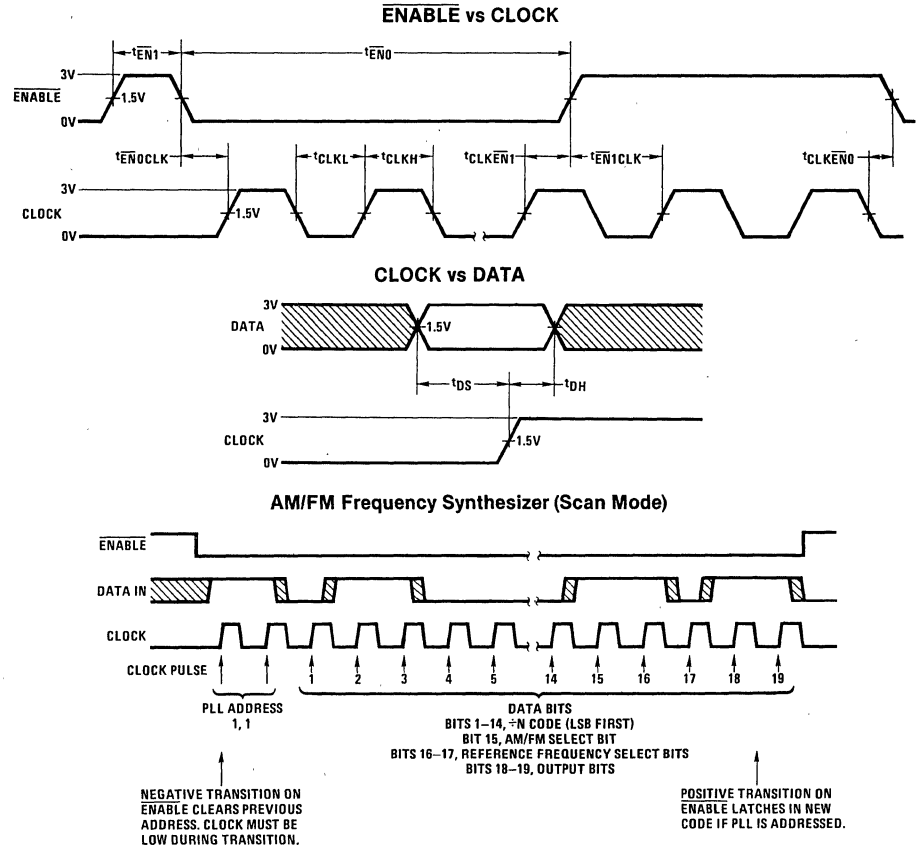








Timing Diagrams*



*Timing diagrams are not drawn to scale. Scale within any one drawing may not be consistent, and intervals are defined positive as drawn.

Serial Data Entry into the DS8908

Serial information entry into the DS8908 is enabled by a low level on the ENABLE input. One binary bit is then accepted from the DATA input with each positive transition of the CLOCK input. The CLOCK input must be low for the specified time preceding and following the negative transition of the ENABLE input.

The first two bits accepted following the negative transition of the ENABLE input are interpreted as address. If these address bits are *not* 1,1, *no* further information will be accepted from the DATA inputs, and the internal data latches *will not* be changed when ENABLE returns high.

If these first two bits *are* 1,1, then all succeeding bits are *accepted* as data, and are shifted successively into the internal shift register as long as ENABLE remains low.

Any data bits preceding the 19th to last bit will be shifted out, and thus are irrelevant. Data bits are counted as any bits *following* two valid address bits (1,1) with the ENABLE low. When the ENABLE input returns high, any further serial data entry is inhibited. Upon this positive transition, the data in the internal shift register is transferred into the internal data latches. Note that until this time, the states of the internal data latches have remained unchanged.

These data bits are interpreted as follows:

Data Bit Position	Data Interpretation	
Last	Bit 19 Output (Pin 2)	
2nd to Last	Bit 18 Output (Pin 1)	
3rd to Last	Ref. Freq. Select Bit(1) 17	
4th to Last	Ref. Freq. Select Bit(1) 16	
5th to Last	AM/FM Select Bit 15	
6th to Last	(2^{13})	÷N(2)
7th to Last	(2^{12})	
8th to Last	(2^{11})	
9th to Last	(2^{10})	
10th to Last	(2^{9})	
11th to Last	(2^{8})	
12th to Last	(2^{7})	
13th to Last	(2^{6})	
14th to Last	(2^{5})	
15th to Last	(2^{4})	
16th to Last	(2^{3})	
17th to Last	(2^{2})	
18th to Last	(2^{1})	
19th to Last	LSB of ÷N (2^{0})	

Note 1: See Reference Frequency Select Truth Table.

Note 2: The actual divide code is N + 1, ie., the number loaded plus 1.

Truth Table

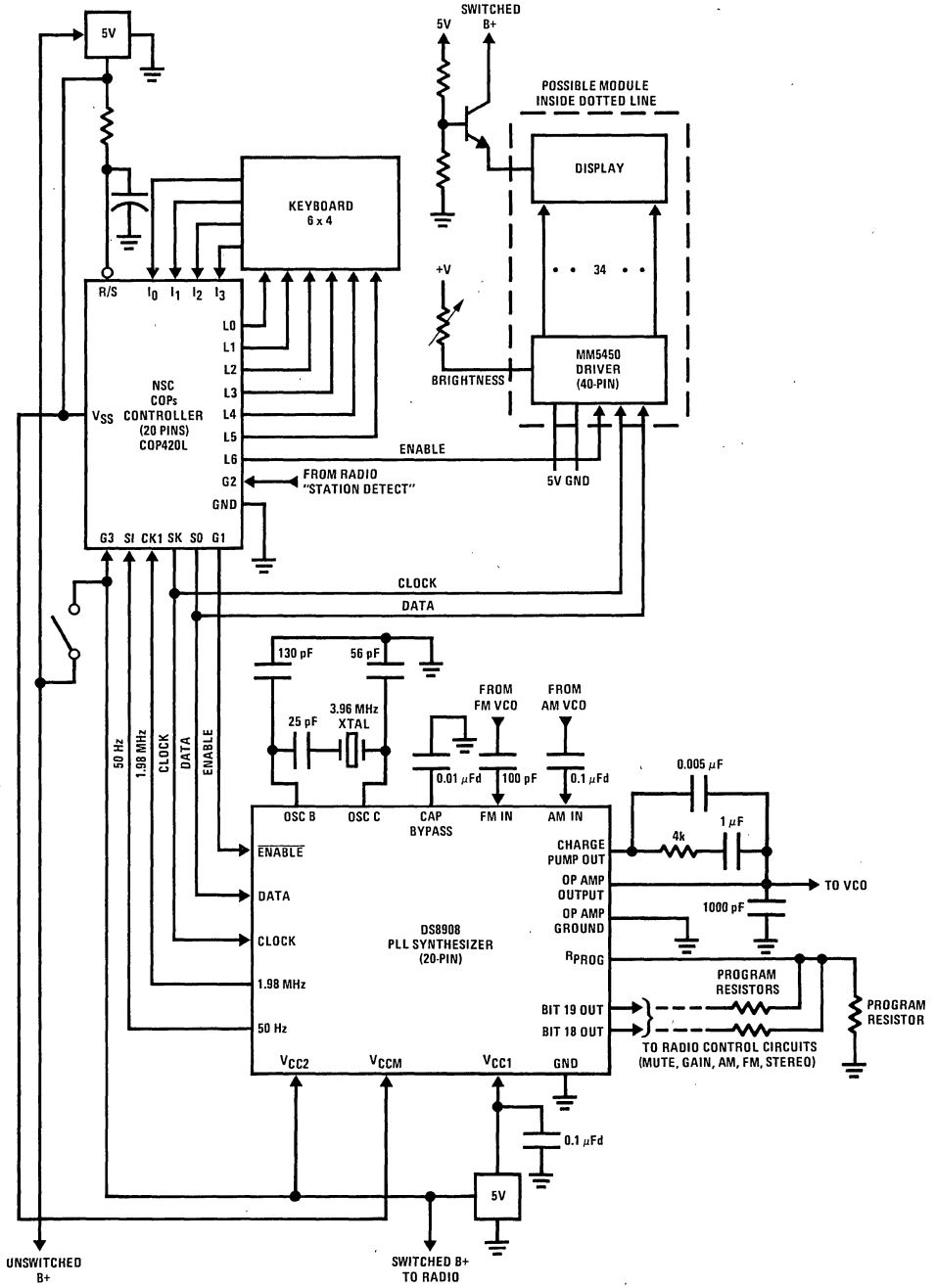
REFERENCE FREQUENCY SELECTION TRUTH TABLE

Serial Data		Reference Frequency
Bit 16	Bit 17	(kHz)
1	1	20
1	0	10
0	1	9
0	0	1

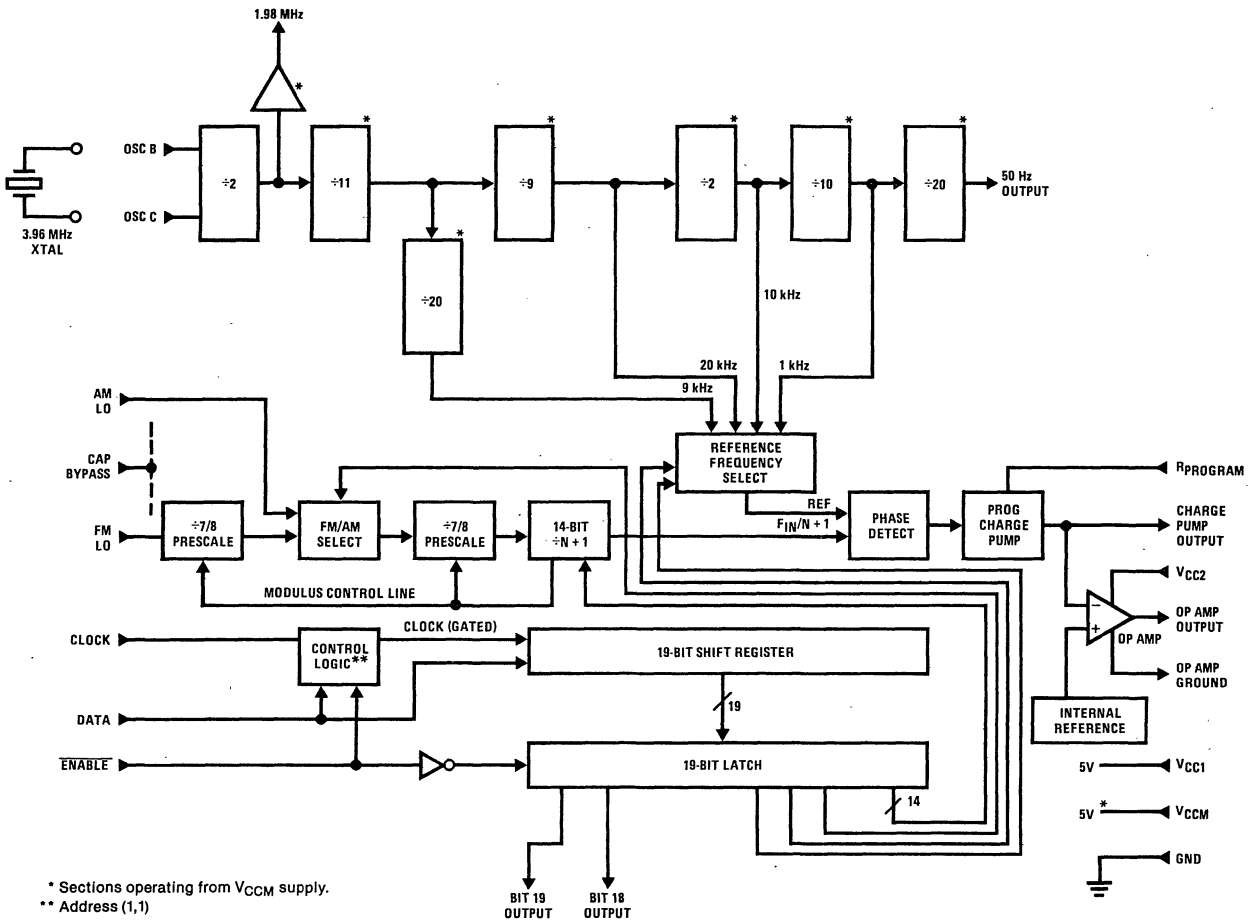
Typical Application

Additional application notes are located at the back of section 11.

Electronically Tuned Radio Controller System; Direct Drive LED



AM/FM PLL/Synthesizer (Serial Data 20-Pin Package)



* Sections operating from V_{CCM} supply.
** Address (1,1)

National Semiconductor

DS8614, DS8615, DS8616, DS8617 130/225 MHz Low Power Dual Modulus Prescalers

General Description

The DS8614 series products are low power dual modulus prescalers which divide by 20/21, 32/33, 40/41, and 64/65, respectively. The modulus control (MC) input selects division by N when at a high TTL level and division by N + 1 when at a low TTL level. The clock inputs are buffered, providing 40 mVrms input sensitivity. The two outputs provide the user the option to wire either a totem-pole or open-collector output structure. Additionally, the user can wire a resistor between the two output pins to minimize edge transition emissions. The outputs are designed to drive positive edge triggered PLLs. These products can be operated from either an unregulated 6.8V to 13.5V source or regulated 5V ± 10% source. Unregulated operation is obtained by connecting V_S to the source with V_{REG} open. Regulated operation is obtained by connecting both V_S and V_{REG} to the supply source.

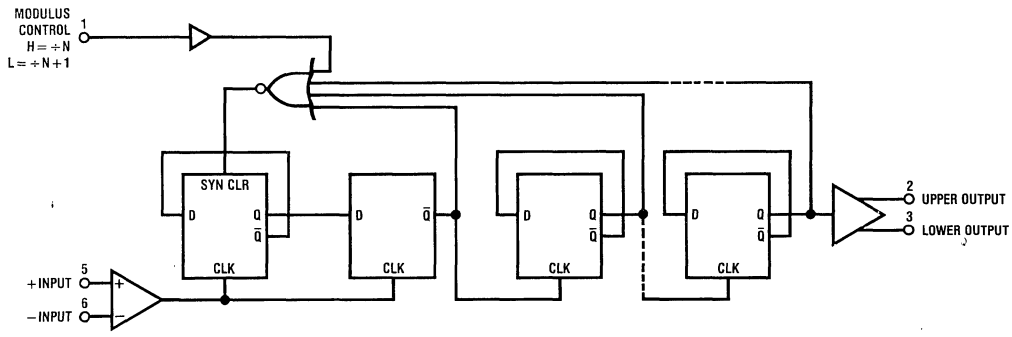
The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 225 MHz.

Features

- Input frequency: 130 MHz (-4, -3); 225 MHz (-2, std)
- Low power: 10 mA (-4, -2); 7 mA (-3, std)
- Input sensitivity: 100 mVrms (-4, -3); 40 mVrms (-2, std)
- Pin compatible with Motorola MC12015-17 prescalers
- Unregulated/regulated power supply option

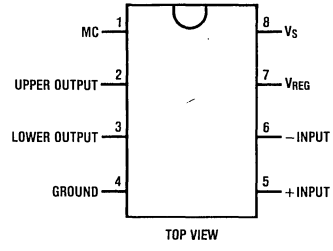
Logic Diagram

Generalized ÷ N/N + 1



Connection Diagram

Dual-In-Line Package



Order Number DS8614N, DS8615N, DS8616N or DS8617N (-4, -3, -2)
See NS Package N08E

Absolute Maximum Ratings (Note 1)

V_S, Unregulated Supply Voltage	15V
V_{REG}, Regulated Supply Voltage	7V
Modulus Control Input Voltage	7V
Open-Collector Output Voltage	7V
Operating Free Air Temperature Range	−30°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	DS8614-4 DS8615-4 DS8616-4 DS8617-4		DS8614-3 DS8615-3 DS8616-3 DS8617-3		DS8614-2 DS8615-2 DS8616-2 DS8617-2		DS8614 DS8615 DS8616 DS8617		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_S	Unregulated Supply Voltage	V_{REG} = Open	6.8	13.5	6.8	13.5	6.8	13.5	5.5	13.5	V
V_{REG}	Regulated Supply Voltage	V_S and V_{REG} Shorted	4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
f_{MAX}	Toggle Frequency	V_{IN} = 100 mVrms	20	130	20	130		225		225	MHz
V_{IN}	Input Signal Amplitude		100	300	100	300	40	300	40	300	mVrms
V_{SLW}	Slew Rate		20		20		20		20		V/μs
I_{OH}	High Level Output Current			−400		−400		−400		−400	μA
I_{OL}	Low Level Output Current			2.0		2.0		2.0		2.0	mA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	DS8614-4 DS8615-4 DS8616-4 DS8617-4		DS8614-3 DS8615-3 DS8616-3 DS8617-3		DS8614-2 DS8615-2 DS8616-2 DS8617-2		DS8614 DS8615 DS8616 DS8617		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High Level MC Input Voltage	V_S = 13.5V, V_{REG} = Open	2.0		2.0		2.0		2.0		V
V_{IL}	Low Level MC Input Voltage	$V_{REG} = V_S$ = 4.5V		0.8		0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA, Pins 2 and 3 Shorted	$V_{REG}-2$		$V_{REG}-2$		$V_{REG}-2$		$V_{REG}-2$		V
I_{CEX}	Open-Collector High Level Output	Lower Output = 5.5V		100		100		100		100	μA
V_{OL}	Low Level Output Voltage	V_{REG} = 4.5V, I_{OL} = 2 mA		0.5		0.5		0.5		0.5	V
I_I	Max MC Input Current	V_S = 13.5V, V_{REG} = Open, V_{IH} = 7V		100		100		100		100	μA
I_{IH}	High Level MC Input Current	V_{REG} = 4.5V, V_{IH} = 2.7V		20		20		20		20	μA
I_{IL}	Low Level MC Input Current	V_S = 13.5V, V_{REG} = Open, V_{IL} = 0.4V		−200		−100		−200		−100	μA
I_S	Supply Current, Unregulated Mode	V_S = 13.5V, V_{REG} = Open		10		7		10		7	mA
I_{REG}	Supply Current, Regulated Mode	$V_S = V_{REG}$ = 5.5V		10		7		10		7	mA

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $T_A = -30°C$ to $70°C$

Symbol	Parameter		Conditions	Min	Max	Units
$t_{MODULUS}$	Modulus Set-Up Time (Notes 4 and 5)	DS8614			55	
		DS8615, DS8616			65	ns
		DS8617			75	
R_{IN}	AC Input Resistance		V_{IN} = 100 MHz and 50 mVrms	1.0		kΩ
C_{IN}	Input Capacitance		V_{IN} = 100 MHz and 50 mVrms	3	10	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

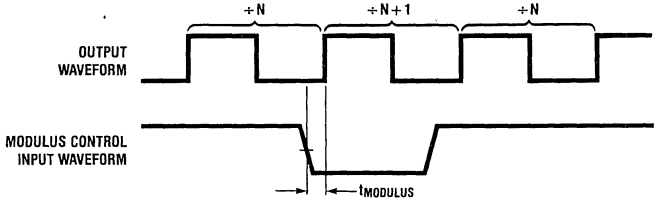
Note 2: Unless otherwise specified min/max limits apply across the −30°C to +70°C temperature range.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: $t_{MODULUS}$ = the period of time the modulus control level must be defined prior to the positive transition of the prescaler output to ensure proper modulus selection.

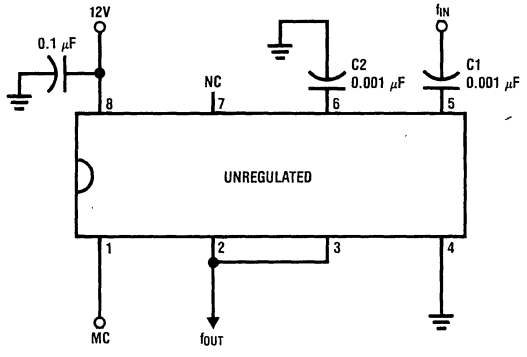
Note 5: See Timing Diagrams.

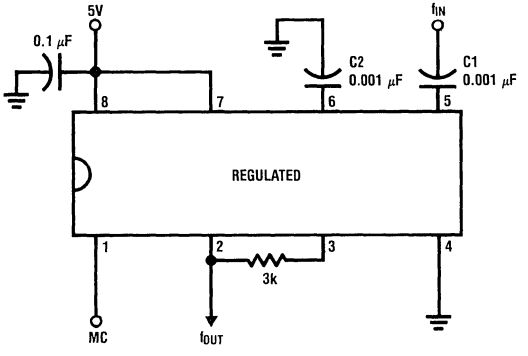
Timing Diagram



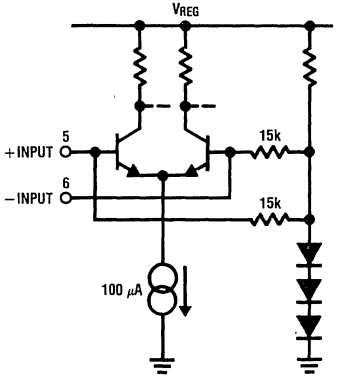
The logic state of the modulus control input just prior to the output's rising edge will determine the modulus ratio of the device immediately following that rising edge. The pulse width difference of N and N + 1 operation occurs during the output = HI condition.

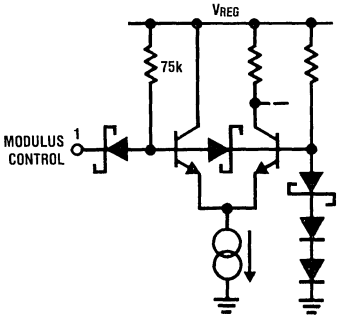
Typical Applications

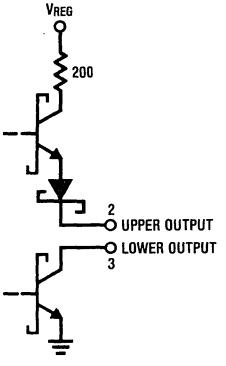




Schematic Diagrams







Application Hints

OPERATING NOTES

The signal source is usually capacitively coupled to the input. At higher frequencies a 0.001 μF input capacitor (C1) is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pull-down resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.001 μF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

The input waveform may be sinusoidal, but below about 20 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 20V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided.

For regulated mode operation connect V_S to V_{REG} to ensure proper operation (see Typical Application diagram).

National Semiconductor

DS8626 120 MHz Divide-by-40 Prescaler
DS8629 120 MHz Divide-by-100 Prescaler

General Description

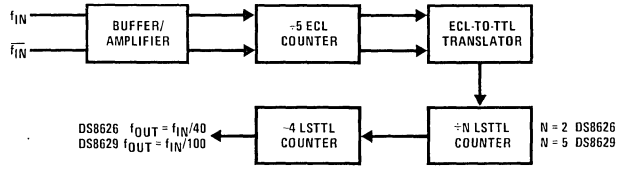
The DS8626 and DS8629 are fixed ratio counters combining ECL and Low Power Schottky technology on a single monolithic substrate. Both provide high frequency capability and TTL compatibility. A single 5.2V ±10% supply is needed.

The device can be operated in a single-ended or differential input mode, with the signal source typically capacitively coupled to the input. An input amplifier is included to allow use of extremely small amplitude, high frequency signals. The output of the device is a square wave of frequency $f_{OUT} = f_{IN}/100$ for the DS8629 and $f_{OUT} = f_{IN}/40$ for the DS8626. The output is standard Low Power Schottky.

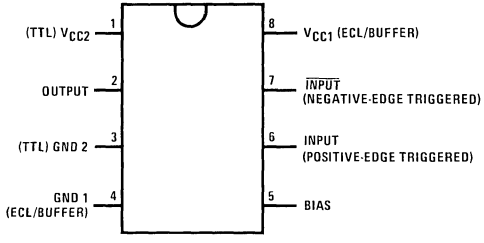
Features

- High frequency, dc–120 MHz–small input amplitude
- Sine wave input 30 MHz $< f_{IN} <$ 120 MHz
- TTL compatible output
- May be used with TTL input
- Single supply operation 5.2V ±10%
- Single ended or differential input modes
- Positive or negative-edge triggered
- Count down sequence avoids broadcast FM IF harmonics

Logic and Connection Diagrams



Dual-In-Line Package

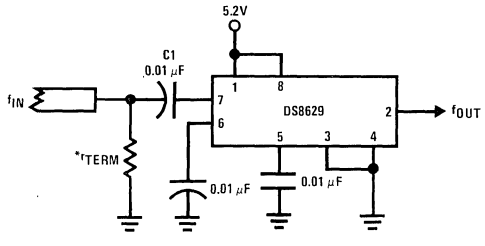


TOP VIEW

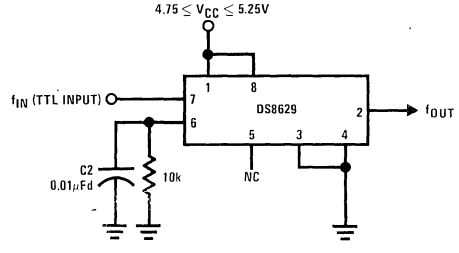
Order Number DS8626N or DS8629N
See NS Package N08A

Typical Applications

High Frequency–Single-Ended Input



TTL Input–dc $< f_{IN} < f_{MAX}$



*r_{TERM} is the termination impedance

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.68	5.72	V
Temperature (T_A)	0	+70	°C

Electrical Characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN1(p-p)}$	Input Voltage (Peak-To-Peak)	Single-Ended @ 120 MHz		200		1000	mV
$V_{IN2(p-p)}$	Input Voltage (Peak-To-Peak)	Differential @ 120 MHz		100		1000	mV
f_{SINE}	Input Frequency with Sine Wave	V_{IN} = 600 mVp-p		30		120	MHz
f_{TTL}	Input Frequency with TTL Input			0		120	MHz
dv	Minimum Slew Rate of Square Wave Input	V_{IN} = 600 mVp-p				100	V/μs
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OH} = −10 μA		2.9			V
		V_{CC} = Min, I_{OH} = −400 μA		2.4			V
		V_{CC} = Min, I_{OH} = −1.6 mA		2.0			V
I_{OS}	Output Short-Circuit Current	V_{CC} = Max		−10		−40	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min	I_{OL} = 8 mA DS8629			0.5	V
			I_{OL} = 1 mA DS8626			0.4	V
I_{CC}	Supply Current	V_{CC} = Max	DS8629		90	135	mA
			DS8626		80	125	mA
Z_{IN}	Input Impedance	V_{IN} = 0.1 V_{p-p} to 1 V_{p-p} Freq. = 120 MHz		100	200	350	Ω

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to 70°C range for the DS8629 and DS8626. All typical values are for T_A = 25°C and V_{CC} = 5.2V.

Note 3: All currents into device pins shown as positive, out of device pins negative, all voltage referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Application Hints

OPERATING NOTES

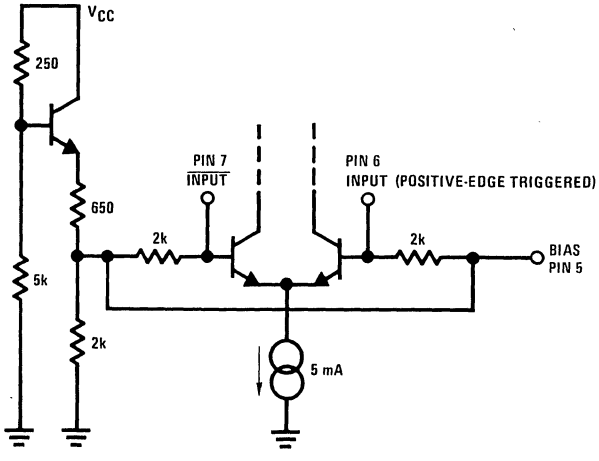
Two ground and two V_{CC} connections are provided separating the ECL and buffer/amplifier stages from the TTL section, isolating the noise transients inherent in the TTL structure. In most cases, shorting the two grounds externally to a good ground plane and the V_{CC}'s to a wide V_{CC} bus will provide sufficient isolation. All components used in the circuit layout should be suitable for the frequencies involved and leads should be kept short to minimize stray inductance. A well by-passed voltage source should be used.

The signal source is usually capacitively coupled to the input. At higher frequencies a 0.01 μF input capacitor (C1) is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pull-down resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.01 μF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

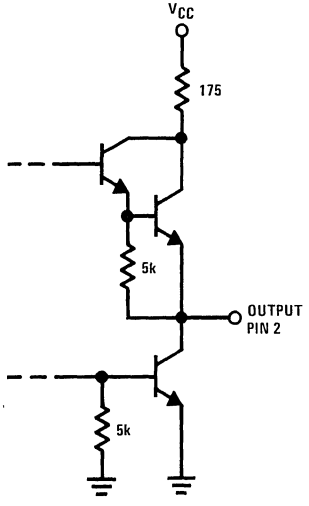
The input waveform may be sinusoidal, but below about 30 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 100 V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided. If it is desired to use a TTL input signal source, the unused input should have a 10 kΩ resistor added to ground and the input coupling capacitor should be eliminated with the TTL source dc coupled to the input.

The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 160 MHz (typically).

Input Configuration



Output Configuration



National Semiconductor

DS8627, DS8628 130/225 MHz Low Power Prescalers

General Description

The DS8627 and DS8628 are low power fixed ratio prescalers which divide by 24 and 20, respectively. The inputs can be driven either single or double-ended and they are buffered, providing 40/100 mVrms input sensitivity. The output provided is open-collector and is capable of interfacing with TTL and CMOS.

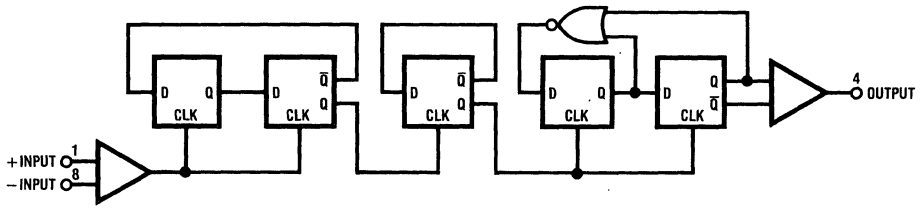
The device can be used in phase-locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more usable level. A digital frequency display system can also be derived separately or in conjunction with a phase-locked loop, and it can extend the useful range of many inexpensive frequency counters to 225 MHz.

Features

- Input frequency: 130 MHz (-4, -3); 225 MHz (-2, std)
- Low power: 10 mA (-4, -2); 7 mA (-3, std)
- Input sensitivity: 100 mVrms (-4, -3); 40 mVrms (-2, std)

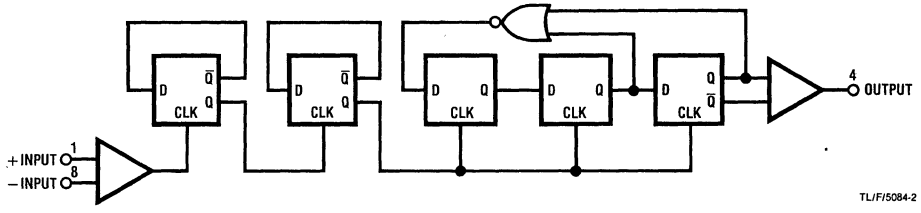
Logic Diagrams

DS8627 (÷ 24)



TL/F/5084-1

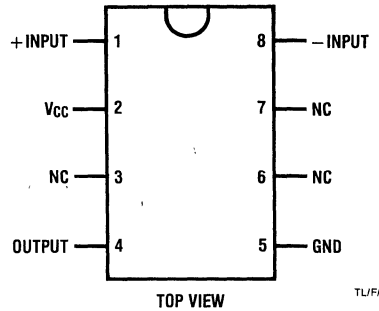
DS8628 (÷ 20)



TL/F/5084-2

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5084-3

Order Number DS8627N or DS8628N (-4, -3, -2)
See NS Package N08E

Absolute Maximum Ratings (Note 1)

V_{CC} Supply Voltage	7V
V_{IN} Input Voltage	$< V_{CC}$
Open-Collector Output Voltage	7V
Operating Free Air Temperature Range	−30°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	DS8627-4 DS8628-4		DS8627-3 DS8628-3		DS8627-2 DS8628-2		DS8627 DS8628		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage		4.5	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
f_{MAX}	Toggle Frequency	V_{IN} = 100 mVrms	20	130	20	130	20	225	20	225	MHz
V_{IN}	Input Signal Amplitude		100	300	100	300	40	300	40	300	mVrms
V_{SLW}	Slew Rate		20		20		20		20		V/μs
I_{OL}	Low Level Output Current			3		3				3	mA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	DS8627-4 DS8628-4		DS8627-3 DS8628-3		DS8627-2 DS8628-2		DS8627 DS8628		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
I_{CEX}	Open-Collector High Level Output	Output = 5.5V		100		100		100		100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 3 mA		0.4		0.4		0.4		0.4	V
I_{CC}	Supply Current	V_{CC} = 5.5V		10		7		10		7	mA

AC Electrical Characteristics V_{CC} = 5V ± 10%, T_A = −30°C to 70°C

Symbol	Parameter	Conditions	Min	Max	Units
R_{IN}	AC Input Resistance	V_{IN} = 100 MHz and 50 mVrms	1.0		kΩ
C_{IN}	Input Capacitance		3	10	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −30°C to +70°C temperature range.

Note 3: All currents into device pins are shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

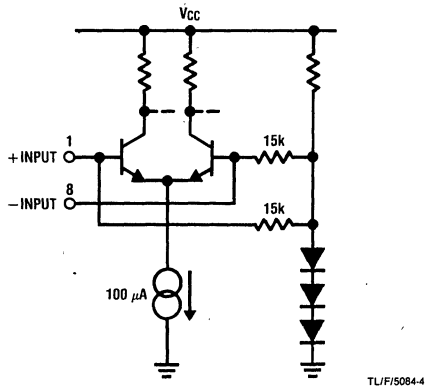
Application Hints

OPERATING NOTES

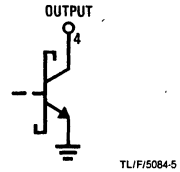
The signal source is usually capacitively coupled to the input. At higher frequencies a 0.001 μF input capacitor is usually sufficient, with larger values used at the lower frequencies. If the input signal is likely to be interrupted, it may be desirable to connect a 100 kΩ resistor between one input and ground to stabilize the device. In the single-ended mode, it is preferable to connect the resistor to the unused input. In the differential mode, the resistor can be connected to either input. The addition of the 100 kΩ pull-down resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions. In addition, in the single ended mode, a capacitor of 0.001 μF should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be made larger for lower frequencies.

The input waveform may be sinusoidal, but below about 20 MHz the operation of the circuit becomes dependent on the slew rate of the input rather than amplitude. A square wave input with a slew rate of greater than 20V/μs will permit correct operation down to lower frequencies, provided the proper input coupling capacitor is provided.

Schematic Diagrams

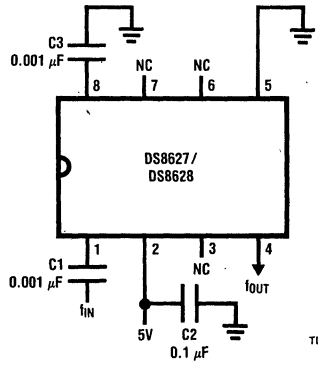


TL/F/5084-4



TL/F/5084-5

Typical Application



TL/F/5084-6

National Semiconductor

Frequency Synthesis
PRELIMINARY

DS8621 275 MHz/1.2 GHz VHF/UHF Prescaler

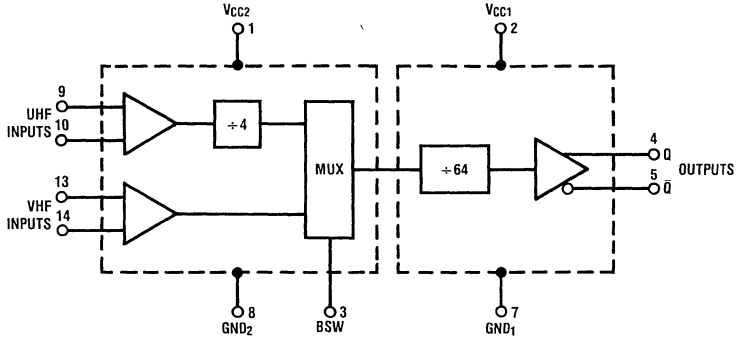
General Description

The DS8621 is a low power, high speed prescaler intended for use in frequency synthesized television tuners. The device performs division by 64 from the VHF input and division by 256 from the UHF input. The VHF and UHF inputs are buffered providing 50 mVrms sensitivity at frequencies in excess of 275 MHz and 1.2 GHz respectively. (The VHF and UHF input signals can be applied either single or double-ended.) The TTL compatible bandswitch (BSW) input selects the VHF inputs when at a low level and the UHF inputs when at a high level. The outputs are complementary ECL structures which have controlled edge-transition rates to minimize spurious harmonic emissions. The device operates from a 5V ± 10% supply source. V_{CC2} and GND_2 power the VHF and UHF input stages while V_{CC1} and GND_1 power the remainder of the circuit, thus limiting internal feedback.

Features

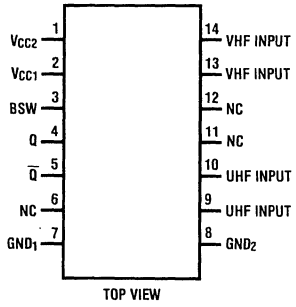
- Broadband operation
- High sensitivity
- Separate VHF and UHF inputs
- Low power
- Pin compatible with RCA (CA3179) and Motorola (MC12071)

Logic Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Truth Table

BSW	Input Mode	Modulus
0	VHF	64
1	UHF	256

Order Number DS8621N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

V_{CC1}, Supply Voltage	7V
V_{CC2}, Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	−30°C to +70°C
Storage Temperature Range	−65°C to +150°C

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
	Supply Voltages				
	V_{CC1}		4.5	5.5	V
	V_{CC2}		4.5	5.5	V
f_{MAX}	Toggle Frequency				
	VHF	V_{IN} = 100 mVrms	80	275	MHz
	UHF		80	1200	MHz
V_{IN}	Input Signal Sensitivity				
	VHF	80 MHz–275 MHz	20	500	mVrms
	UHF	80 MHz–450 MHz	100	500	mVrms
		450 MHz–1200 MHz	50	500	mVrms
	Input Slew Rate				
	VHF		20		V/μs
	UHF		20		V/μs
I_{OH}	High Level Output Current			−300	μA
I_{OL}	Low Level Output Current			300	μA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level BSW Input Voltage	V_{CC} = 5.5V	2.0		V
V_{IL}	Low Level BSW Input Voltage	V_{CC} = 4.5V		0.8	V
I_I	Max High Level BSW Input Current	V_{CC} = 4.5V V_{IH} = 7V		100	μA
I_{IH}	High Level BSW Input Current	V_{CC} = 4.5V V_{IH} = 2.7V		20	μA
I_{IL}	Low Level BSW Input Current	V_{CC} = 5.5V V_{IL} = 0.4V		−100	μA
	Output Voltage Range	Refer to Output Load Diagram	0.75	1.6	Vp-p
I_{CC}	Supply Current	V_{CC} = 5.5V		32.0	mA

AC Electrical Characteristics V_{CC} = 5V ± 10%, T_A = −30°C to +70°C

Parameter	Conditions	Min	Max	Units
Output Rise/Fall Time	Refer to Output Load Diagram	40	110	ns

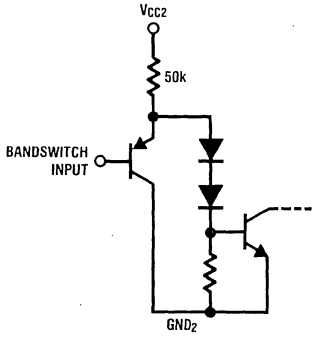
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −30°C to +70°C temperature range.

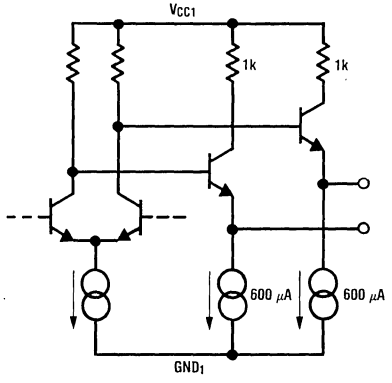
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Typical Input/Output Schematics

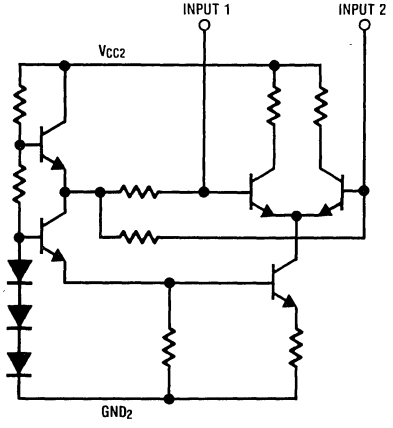
Bandswitch Buffer



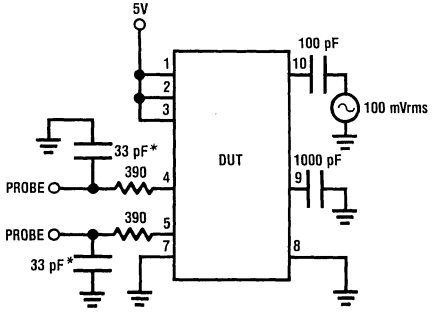
Output Buffer



UHF/VHF Input Buffers



Output Load Diagram



* includes capacitance of probes

National Semiconductor

Frequency Synthesis
PRELIMINARY

DS8622 500 MHz/1.2 GHz Dual Modulus VHF/UHF Prescaler

General Description

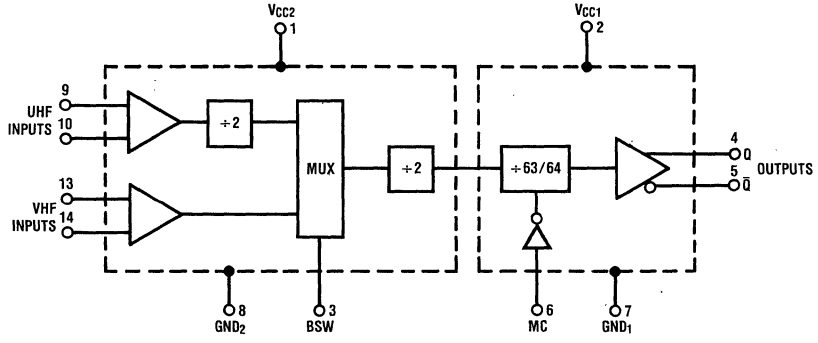
The DS8622 is a low power broadband dual modulus prescaler intended for use in frequency synthesized television tuners. The device features separate VHF and UHF buffered inputs, VHF input division by 126 or 128, UHF input division by 252 or 256, TTL compatible bandswitch and modulus control inputs, complementary ECL outputs, and 5V operation.

The VHF and UHF inputs cover a frequency range from 80 MHz to 1200 MHz and can be driven either single or double-ended. The bandswitch (BSW) input selects the VHF inputs when at a low level and the UHF inputs when at a high level. The modulus control (MC) input selects division by 126 or 252 when at a high level and division by 128 or 256 when at a low level. The dual modulus feature of this prescaler can provide frequency resolution steps of 3.9 kHz, 7.8 kHz, or 15.6 kHz as shown in the table of Possible Operating Conditions. The outputs are internally edge-transition controlled to minimize spurious harmonic emissions. The device operates from a standard 5V ± 10% supply source. V_{CC2} and GND_2 power the VHF and UHF input stages, and V_{CC1} and GND_1 power the remainder of the circuit, thus limiting internal feedback.

Features

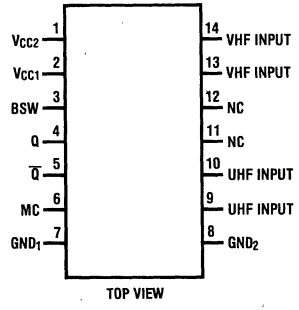
- Broadband operation
- Increased frequency resolution
- High input sensitivity
- Separate VHF and UHF inputs
- Low power

Logic Diagram



Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Truth Table

BSW	MC	Input Mode	Modulus
0	0	VHF	128
0	1	VHF	126
1	0	UHF	256
1	1	UHF	252

Order Number DS8622N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

V_{CC1}, Supply Voltage	7V	Operating Free Air Temperature Range	−30°C to +70°C
V_{CC2}, Supply Voltage	7V	Storage Temperature Range	−65°C to +150°C
BSW, MC Input Voltage	7V		

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
	Supply Voltages				
	V_{CC1}		4.5	5.5	V
	V_{CC2}		4.5	5.5	V
f_{MAX}	Toggle Frequency				
	VHF	V_{IN} = 100 mVrms	80	550	MHz
	UHF		80	1200	MHz
V_{IN}	Input Signal Sensitivity				
	VHF	80 MHz–550 MHz	50	500	mVrms
	UHF	80 MHz–550 MHz	100	500	mVrms
		550 MHz–1200 MHz	50	500	mVrms
	Input Slew Rate				
	VHF		20		V/μs
	UHF		20		V/μs
I_{OH}	High Level Output Current			−300	μA
I_{OL}	Low Level Output Current			300	μA

DC Electrical Characteristics (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage (Note 4)	V_{CC} = 5.5V	2.0		V
V_{IL}	Low Level Input Voltage (Note 4)	V_{CC} = 4.5V		0.8	V
I_I	Max Input Current (Note 4)	V_{CC} = 4.5V V_{IH} = 7V		100	μA
I_{IH}	High Level Input Current (Note 4)	V_{CC} = 4.5V V_{IH} = 2.7V		20	μA
I_{IL}	Low Level Input Current (Note 4)	V_{CC} = 5.5V V_{IL} = 0.4V		−100	μA
	Output Voltage Range	Refer to Output Load Diagram	0.75	1.6	Vp-p
I_{CC}	Supply Current			32.0	mA

AC Electrical Characteristics V_{CC} = 5V ± 10%, T_A = −30°C to +70°C

Symbol	Parameter	Conditions	Min	Max	Units
$t_{MODULUS}$	Modulus Set-Up Time (Note 5)			65	ns
t_{SEL}	BSW Select Time			20	μs
	Output Rise/Fall Time	Refer to Output Load Diagram	40	110	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −30°C to +70°C temperature range.

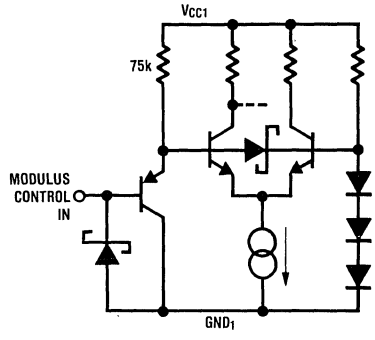
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies to BSW and MC inputs.

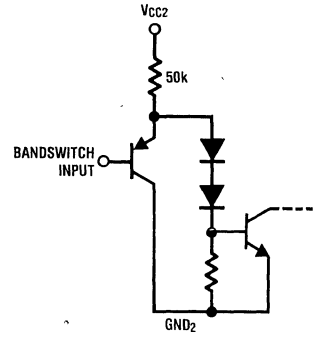
Note 5: $t_{MODULUS}$ = the period of time the modulus control level must be defined prior to the positive transition of the prescale output to ensure proper modulus selection.

Typical Input/Output Schematics

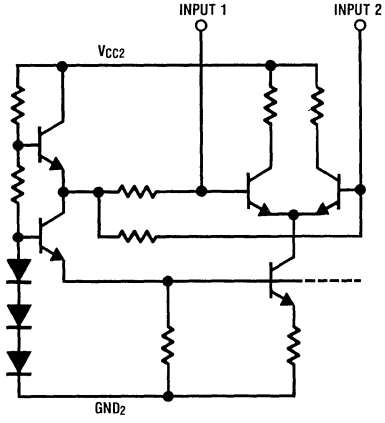
Modulus Control Buffer



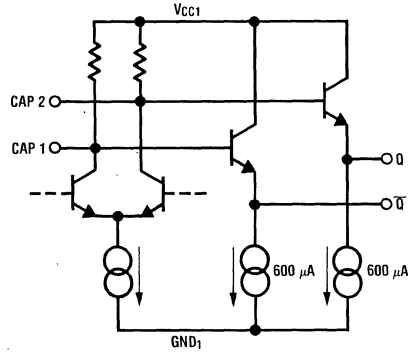
Bandswitch Buffer



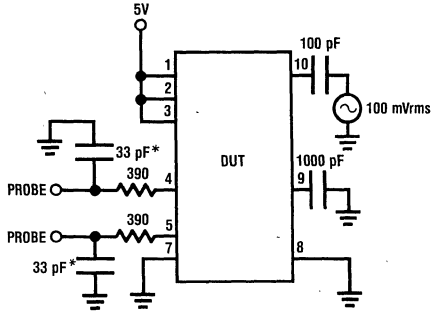
UHF/VHF Input Buffers



Output Buffer



Output Load Diagram



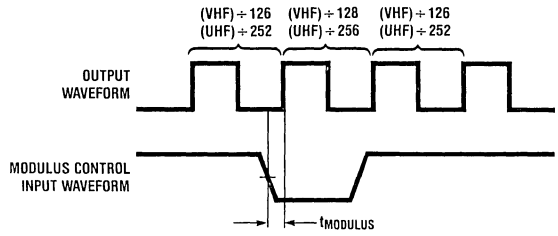
* Includes capacitance of probes.

POSSIBLE OPERATING CONDITIONS

Reference Frequency (kHz)	Mode	Frequency Resolution (kHz)	Min Lock Frequency* (MHz)
15.625	VHF	31.25	124.03125
	UHF	62.5	248.0625
7.8125	VHF	15.625	62.015625
	UHF	31.25	124.03125
3.90625	VHF	7.8125	31.0078
	UHF	15.625	62.015625

* Frequencies obtainable using minimum continuous N code.

Timing Diagram



The modulus control input level is sensed immediately prior to the output low-to-high level transition. The prescaler's modulus value will respond to the change in the modulus control input level immediately *after* that same output low-to-high level transition.

Digital PLL Synthesis

National Semiconductor
Application Note 335
Craig Davis
Tom Mills
Keith Mueller
April 1983

I. System Concepts

INTRODUCTION

Digital tuning systems are fast replacing the conventional mechanical systems in AM/FM and television receivers. The desirability of the digital approach is mainly due to the following features:

- Precise tuning of station frequencies
- Exact digital frequency display
- Keyboard entry of desired frequency
- Virtually unlimited station memory
- Up/down scanning through the band
- Station "search" (stop on next active station)
- Power on to the last station
- Easy option for time-of-day clock

In addition, recent developments in large scale integrated circuit technology and new varactor diodes for the AM band have made the cost-benefit picture for digital tuning very attractive. System partitioning is extremely important in optimizing this cost-benefit picture, as will be discussed.

SYSTEM DESCRIPTION

A simplified block diagram of a typical digitally tuned receiver is shown in *Figure 1*. Notice this receiver could be one for AM, FM, marine radio, or television; it makes no difference. The frequency synthesizer block generates the local oscillator frequency for the receiver, just as a conventional mechanical tuner would. However, the phase-locked-loop (PLL) acts as an integral frequency multiplier of an accurate crystal controlled reference frequency while the mechanical type provides a continuously variable frequency output with no reference. Some method of controlling the value of the multiplier for channel tuning must be provided. The other RF, IF, and audio/video circuitry will be the same as in the mechanical tuning method.

There are many different ways to partition the frequency synthesizer system to perform the digital tuning function.

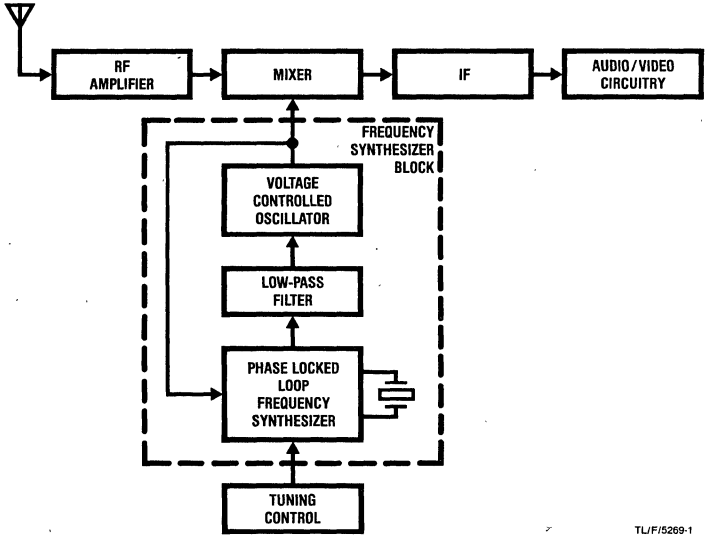


FIGURE 1. Block Diagram of a Digitally Tuned Receiver

COPS™ is a trademark of National Semiconductor Corp.

PROGRAMMABLE CONTROLLER FUNCTION

The most cost-effective application of different IC process technologies is shown in *Figure 2.* The controller is separate from the PLL. The controller can be as simple as a mask programmable microcontroller* or as complicated as a high-powered microprocessor system. It can be done most economically with NMOS technology because of the logic density possible and the small size of the RAM/ROM memory cells. It could also be CMOS for extremely low power consumption in standby mode.

BASIC PHASE-LOCKED-LOOP FUNCTION

The DS8906/7/8 series of PLLs utilize a dual-modulus frequency synthesis technique. The reasons for this and the PLL itself will now be discussed.

Figure 3 is a diagram of the most simple phase-locked-loop. A particular reference frequency is generated by a crystal oscillator and some fixed divider, and this goes into one side of a digital phase comparator. A voltage controlled oscillator (VCO) feeds directly into the other input of the phase comparator. The output of the phase comparator is an error signal which is filtered and fed back to the VCO as a DC control voltage.

In lock, the phase error must be zero, so f_{IN} equals f_{REF}. This system provides only one output frequency, that being equal to the reference frequency.

Figure 4 is basically the same but now a programmable divide-by-N counter is between the VCO and the phase comparator. The input to the phase comparator (f_{IN}) now becomes the output frequency of the VCO (f_{OUT}) divided by N, where N is the division code loaded into the programmable counter. This means f_{OUT}/N must equal f_{REF}. Thus, the VCO output frequency becomes $N \times f_{REF}$, and f_{OUT} can now be changed in integral steps of f_{REF} by merely changing N.

*Such as National's COPS™ family.

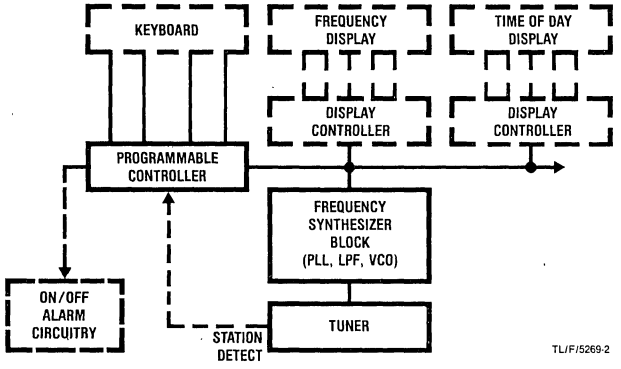


FIGURE 2. System Block Diagram

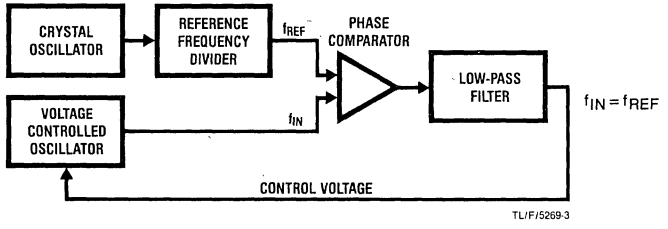


FIGURE 3. Basic Phase-Locked-Loop

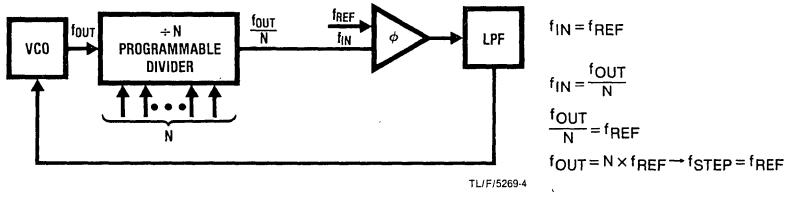
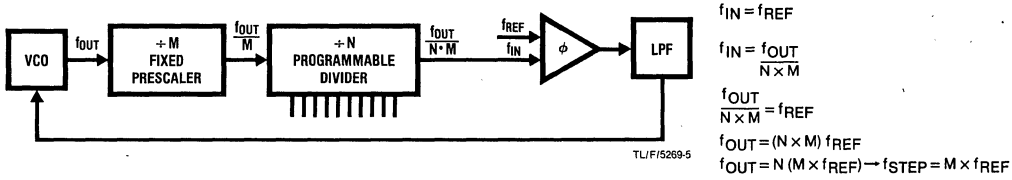


FIGURE 4. Basic PLL Frequency Synthesizer

In applications where the output frequency desired exceeds the maximum clock frequency of available programmable dividers, a common solution is to add a prescaler preceding the programmable divider, as shown in *Figure 5*. In this case $f_{OUT} = N (M \times f_{REF})$ and so the output frequency step size becomes $M \times f_{REF}$. So, while this technique allows higher frequency operation, it does so at the expense of either increased channel spacing for a given reference frequency, or decreased reference frequency if a specific channel spacing is required. This latter limitation is often undesirable as it can cause increased lock-on time, decreased scanning rates, and sidebands at undesirable frequencies.

Figure 6 shows the basic dual-modulus scheme. Here, a dual-modulus prescaler is substituted for the fixed prescaler and the modulus is controlled by programmable counters. The advantage to this approach is that the step size is again equal to the reference frequency while the prescaling still allows the programmable counters to operate at lower frequencies. As in the fixed prescale technique, only the prescaler needs to be high speed. The DS8906/7/8 prescale by 7/8 for AM and in a similar fashion by 63/64 in FM.



$f_{IN} = f_{REF}$

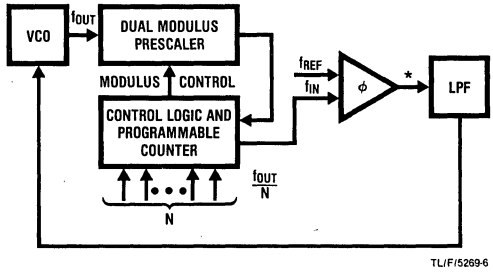
$f_{IN} = \frac{f_{OUT}}{N \times M}$

$\frac{f_{OUT}}{N \times M} = f_{REF}$

$f_{OUT} = (N \times M)\, f_{REF}$

$f_{OUT} = N (M \times f_{REF}) \rightarrow f_{STEP} = M \times f_{REF}$

FIGURE 5. PLL Frequency Synthesizer with Fixed Prescaler



$f_{IN} = \frac{f_{OUT}}{N} = f_{REF}$

$f_{OUT} = N \times f_{REF} \rightarrow f_{STEP} = f_{REF}$

*if $f_{REF} = f_{IN}$, then "tuned"
if $f_{REF} \neq f_{IN}$, then "not tuned"

FIGURE 6. Basic Dual-Modulus Frequency Synthesizer

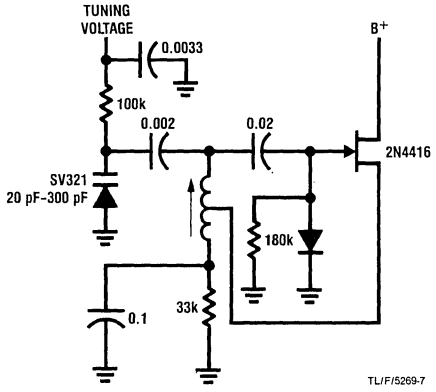
II. Application Hints

VOLTAGE CONTROLLED OSCILLATORS

In all radio and television applications, the voltage controlled oscillator (VCO) is a varactor tuned, LC type of circuit. The LC circuit is used over the various RC current controlled circuits because of their superior noise characteristics. *Figure 7* shows a collection of popular VCOs used in radio and television tuners. The AM VCO is a Hartley design chosen for wide tuning range. Commonly used varactors will show a capacitance change of 350 pF at 1V to 20 pF at 8V, which if used in a low capacitance oscillator circuit, can produce a tuning range approaching 3 to 1.

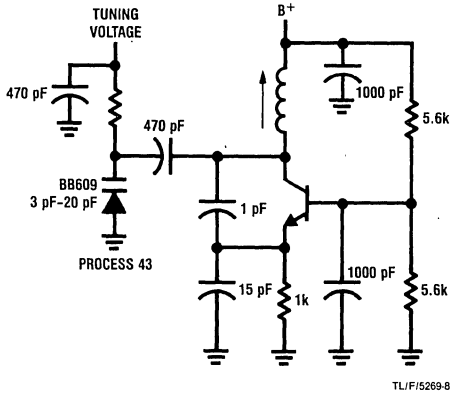
In the higher frequency ranges, above 50 MHz, Colpitts oscillators are used because stray circuit capacitance will be in parallel with desired feedback capacitance and not cause undesirable spurious resonances that might occur with the tapped coil Hartley design. The FM VCO shown is a grounded base design with feedback from collector to emitter. A UHF television oscillator is also shown. It too is a grounded base oscillator, but using a transmission line as the resonant element instead of a coil. The transmission line and tuning capacitors are arranged in π network which offers improved noise characteristics over a parallel tuned circuit. This circuit will tune over almost an octave.

Hartley Oscillator



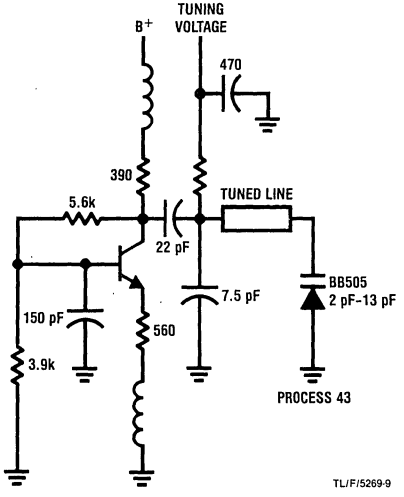
50 kHz ~ 15 MHz VCO
Tuning range ≃ 3:1

Colpitts Oscillator



50 MHz ~ 300 MHz VCO
Tuning range ≃ 2:1

Colpitts Oscillator



500 MHz ~ 1000 MHz VCO
Tuning range ≃ 1.8:1

FIGURE 7. Typical VCO Circuits (Typical Values Shown)

PLL LOOP FILTER CALCULATIONS

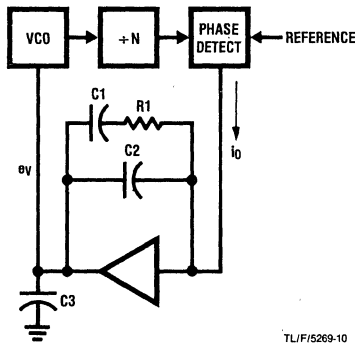
Andrzej Przedpelski, in two articles published in Electronic Design (#19, Sept. 13, 1978 and #10, May 10, 1978) explains how to calculate the three time constants associated with a third order type 2 loop which is typically used with the DS8906/7/8 series. *Figure 8* explains his method and shows a sample calculation. His articles illustrate how to calculate three time constants, and plot open loop gain and phase, and closed loop noise response.

It should be noted that VCO gain, K_V, is in terms of radians per second per volt, and phase detector gain, K_D, is in terms of amps per radian. The phase detector gain for the DS8906/7/8 series is $\pm I_{OUT}$ divided by 4π.

Figure 9 illustrates an example calculation of time constants, and a plot of open loop gain and phase based on the preceding analysis.

REFERENCES

1. Manassewitsch V., *"Frequency Synthesizers"* (Wiley, New York, 1976)
2. Rohde, A. L., *"Digital PLL Frequency Synthesizers"* (Prentice Hall, Englewood Cliffs, 1983)
3. Egan, W.F., *"Frequency Synthesis By Phase Lock"* (Wiley, New York, 1981)



$T1 = R1C1$

$T2 = R1C2$

$$\frac{eV}{i_O} = \frac{1 + ST1}{SC1\,(1 + ST2)}$$

$$G(S) = \frac{K_D\,K_V}{NS^2C1}\left(\frac{1 + ST1}{1 + ST2}\right)$$

$$T2 = \frac{1 - \tan\phi\,\cos\phi}{\omega_O \cos\phi}$$

$$T1 = \frac{1}{\omega_O{}^2 T2}$$

$$C1 = \frac{K_D\,K_V}{N\omega_O{}^2}\left(\frac{-\omega_O T1 - 1}{\omega_O T2 + 1}\right)$$

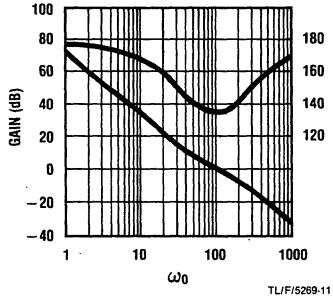
where θ = desired phase margin

ω_O = loop natural frequency

≈ closed loop bandwidth

Note: DS8908 op amp requires C3 ≈ 1000 pF for compensation.

FIGURE 8. Third Order Type 2 Loop



VHF loop, running at 100 MHz, ref = 10 kHz

$K_V = 2.5$ MHz/V = 15.7 Mrad/sec/V

$$K_D = \frac{400\,\mu A}{4\pi} = 31.8\,\mu A/\text{radian}$$

$$N = \frac{100\text{ MHz}}{10\text{ kHz}} = 10{,}000,\ \omega_O = 2\pi \times 100\text{ Hz}$$

$\theta = 45°$ (desired phase margin)

$T2 = 6.6 \times 10^{-4}$ sec

$T1 = 3.84 \times 10^{-3}$ sec

$C1 = 0.3\,\mu F$

so $R1 = T1/C1 = 13\,k\Omega$

$C2 = T2/R1 = 0.05\,\mu F$

FIGURE 9. Example of Gain and Phase Calculation

DUAL-MODULUS COUNTING RANGE LIMITATIONS

- Minimum count limitations
- Maximum count limitations

The DS8906/7/8 series PLLs utilize a dual-modulus counting scheme internally based on a 63/64 prescale modulus in FM mode in order that all of the U.S. FM frequency assignments could be reached using a 25 kHz reference. The counter modulus $N = 64A + B$ where B is the 6 least significant bits of N and A is the 7th and greater significant bits of N.

$$N = 64A + B$$
$$N = 64A + \overline{63} - B \quad (B = 63 - \overline{B})$$
$$1 + N = 64A + 63 + 1 - 64\overline{B} + 63\overline{B}$$
$$1 + N = 64\,(A + 1 - \overline{B}) + 63\overline{B}$$

The last equation is in the final form used internally by the DS8906/7/8. The equation indicates that, if N is loaded into the device, it will solve for N + 1.

The minimum continuous N modulus (code) the equation dictates should occur when $A = \overline{B}$. $\overline{B}$ maximum = 63 implies $A = \overline{62}$, B = 63 should be an illegal N + 1 code (N + 1 = 3969). However, because this is just inside the lower FM band limits, extra circuitry was added to enable this particular code's operation. The actual minimum N + 1 code for these PLLs thus becomes the case when $A = 61$, $\overline{B} = 61$, N + 1 minimum = 3907. There are legitimate N + 1 codes below this 3907 value, however, they are not continuous. (i.e., Starting at 3907 and counting down, one additional code is in error every 63 codes. Thereafter, these erroneous codes are the cases where $A < \overline{B}$.) The sequence of illegal codes is shown in *Figure 10.*

Loaded Value of N	A	$\overline{B}$	Status	Actual Locked N + 1 Value
3906	61	61	OK	3907
3905	61	62	illegal	3907
3904	61	63	illegal	3907
3903	60	0	OK	3904
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3843	60	60	OK	3844
3842	60	61	illegal	3844
3841	60	62	illegal	3844
3840	60	63	illegal	3844
3839	59	0	OK	3840
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3780	59	59	OK	3781
3779	59	60	illegal	3781
3778	59	61	illegal	3781
3777	59	62	illegal	3781
3776	59	63	illegal	3781
3775	58	0	OK	3776
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
3717	58	58	OK	3718
3716	58	59	illegal	3718
3715	58	59	illegal	3718
3714	58	60	illegal	3718
3713	58	61	illegal	3718
3712	58	63	illegal	3718
3711	57	0	OK	3712
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•

TL/F/5269-12

FIGURE 10. FM Mode Dual-Modulus Counting Below the Minimum Continuous N Code of 3906

Maximum code limits for these dual-modulus PLLs are determined by the N code bit length. The DS8906 and DS8908 have a 14-bit N counter allowing 16,383 counts. The DS8907 has a 13-bit N node length, allowing a maximum N count of 8,191. See *Figure 11* for table operating ranges of the DS8906, DS8907 and DS8908 PLLs.

CONCLUSION

The major application for the DS8906/7/8 PLLs are synthesizers for AM-FM radios, and have been widely accepted in the marketplace. *Figure 12* shows the block diagram of such a radio. In this application the following performance relating to the PLL tuning system is realized.

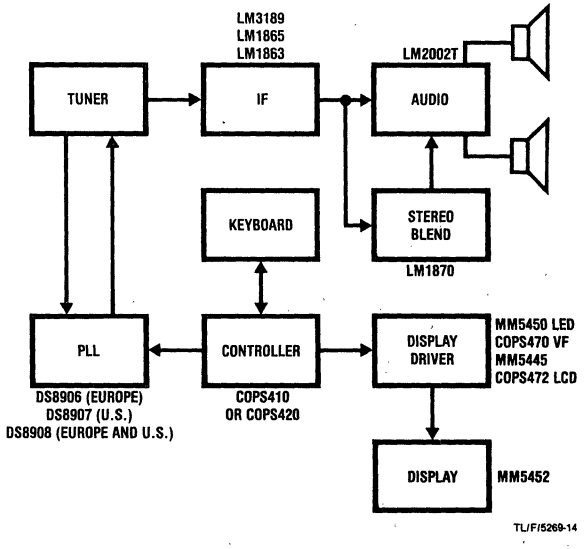
PLL Loop Bandwidth	300 Hz
Reference Frequency Sidebands	>60 dB
Signal-to-Noise Ratio	
AM: 30% modulation	>50 dB
FM: 22.5 kHz deviation	>55 dB
Switching Speed (one channel)	<1.5 ms

Product	Input	Ref (Hz)	f_{IN} (Hz)	
			Min*	Max
DS8906	AM	500	24.5k	8.193M
	FM	12.5k	48.8375M	120M
DS8907	AM	10k	490k	15M
	FM	25k	97.675M	120M
DS8908	AM	1k	49k	15M
		9k	441k	15M
		10k	490k	15M
		20k	980k	15M
	FM	1k	3.907M	15M
		9k	35.163M	120M
		10k	39.07M	120M
		20k	78.14M	120M

TL/F/5269-13

*The minimum frequency shown is obtained when the minimum continuous N code is utilized and it assumes the edge rates >20V/μs.

FIGURE 11. Product Operating Frequency Range



TL/F/5269-14

FIGURE 12. AM-FM Digitally Tuned Radio System

Section 12
Interface Appendices

12

Interface Cross Reference Guide

National Semiconductor

Device Designation	National's Direct Replacement	National's Closest Replacement
AMD		
AM26LS30DC	DS3691J	
AM26LS30PC	DS3691N	
AM26LS31DC	DS26LS31CJ	
AM26LS31PC	DS26LS31CN	
AM26LS32DC	DS26LS32ACJ	DS26LS32CJ
AM26LS32PC	DS26LS32ACN	DS26LS32CN
AM26LS33DC	DS26LS33ACJ	DS26LS33CJ
AM26LS33PC	DS26LS33ACN	DS26LS33CN
AM26S10DC	DS26S10J	
AM26S10PC	DS26S10N	
AM26S11DC	DS26S11J	
AM26S11PC	DS26S11N	
AM26S12DC		DS8838J
AM26S12PC		DS8838N
AM2965DC		DP84240J
AM2965PC		DP84240N
AM2966DC		DP84244J
AM2966PC		DP84244N
N8T26AB	DS8T26AN	
N8T26AF	DS8T26AJ	
N8T28F	DS8T28J	
N8T28N	DS8T28N	
D8212	DP8212J	
P8212	DP8212N	
D8216	DP8216J	
P8216	DP8216N	
D8224	DP8224J	
AM8224PC	DP8224N	
D8226	DP8226J	
P8226	DP8226N	
AM8228PC	DP8228N	
D8228	DP8228J	
AM8238PC	DP8238N	
D8238	DP8238J	
DP8303J	DP8303J	
DP8303N	DP8303N	
DP8304BJ	DP8304BJ	
DP8304BN	DP8304BN	
DP8307J	DP8307J	
DP8307N	DP8307N	
DP8308J	DP8308J	
DP8308N	DP8308N	
DS8838J	DS8838J	
DS8838N	DS8838N	

The manufacturer's most current data sheets take precedence over this guide.

AMD TO NATIONAL'S INTERFACE

Interface Cross Reference Guide (Continued)

National Semiconductor

NATIONAL'S INTERFACE TO FAIRCHILD

Device Designation	National's Direct Replacement	National's Closest Replacement
FAIRCHILD		
μA1488DC	DS1488J	
μA1488PC	DS1488N	
μA1489ADC	DS1489AJ	
μA1489APC	DS1489AN	
μA1489DC	DS1489J	
μA1489PC	DS1489N	
μA3680DC	DS3680J	
μA3680PC	DS3680N	
75107ADC	DS75107J	
75107APC	DS75107N	
75107BDC		DS75107J
75107BPC		DS75107N
75108ADC	DS75108J	
75108APC	DS75108N	
75108BDC		DS75108J
75108BPC		DS75108N
75150RC	DS75150J-8	
75150TC	DS75150N	
75154DC	DS75154J	
75154PC	DS75154N	
75450BDC	DS75450J	
75450BPC	DS75450N	
75451ARC	DS75451J-8	
75451ATC	DS75451N	
75451BRC	DS75451J-8	
75451BTC	DS75451N	
75452ARC	DS75452J-8	
75452ATC	DS75452N	
75452BRC	DS75452J-8	
75452BTC	DS75452N	
75453ARC	DS75453J-8	
75453ATC	DS75453N	
75453BRC	DS75453J-8	
75453BTC	DS75453N	
75461RC	DS75461J-8	
75461TC	DS75461N	
75462RC	DS75462J-8	
75462TC	DS75462N	
75471TC		DS3611N
75472TC		DS3612N
75491PC	DS75491N	
75492PC	DS75492N	
75492APC		DS75492N
μA8T26ADC	DS8T26AJ	
μA8T26APC	DS8T26AN	
μA8T28DC	DS8T28J	
μA8T28PC	DS8T28N	
9614DC	DS75114J	
9614PC	DS75114N	
9615DC	DS75115J	
9615PC	DS75115N	
9616DC		DS1488J
9616PC		DS1488N
9617DC		DS1489AJ
9617DC		DS1489J
9617PC		DS75154N
9636ARC		DS3691J
9636ATC		DS3691N
9637ARC		DS3486J
9637ATC		DS3486N
9640DC	DS26S10J	
9640PC	DS26S10N	
9643PC		DS75322N
9643TC		DS75322N
9645DC		DS3245J
9645PC		DS3245N

The manufacturer's most current data sheets take precedence over this guide.

Interface Cross Reference Guide (Continued)

National Semiconductor

Device Designation	National's Direct Replacement	National's Closest Replacement
INTEL		
D3245	DS3245J	
D8212	DP8212J	
P8212	DP8212N	
D8216	DP8216J	
P8216	DP8216N	
D8224	DP8224J	
D8224	DP8224N	
D8226	DP8226J	
P8226	DP8226N	
D8228	DP8228J	
D8228	DP8228N	
D8238	DP8238J	
P8238	DP8238N	
D8286	DP8304BJ	
P8286	DP8304BN	
D8287	DP8303J	
P8287	DP8303N	

The manufacturer's most current data sheets take precedence over this guide.

INTEL TO NATIONAL'S INTERFACE

Device Designation	National's Direct Replacement	National's Closest Replacement
MMI		
74S408N	DP8408N	
74S409N	DP8409N	
74S780N	DP8400N	

The manufacturer's most current data sheets take precedence over this guide.

Interface Cross Reference Guide (Continued)

National Semiconductor

Device Designation	National's Direct Replacement	National's Closest Replacement
MOTOROLA		
MMH0026CG	DS0026CH	DS0026CG
MMH0026CL	DS0026CJ	
MMH0026CN	DS0026CN	
MMH0026CP1	DS0026CN	
MMH0026G	DS0026H	
MMH0026L	DS0026J	
MC12015P	DS8615N	
MC12016P	DS8616N	
MC12017P	DS8617N	
MC12071P	DS8621N	
MC1472P1		DS3612N
MC1472P1		DS3632N
MC1472U		DS3612J-8
MC1472U		DS3632J-8
MC1488L	DS1488J	
MC1488P	DS1488N	
MC1489AL	DS1489AJ	
MC1489AP	DS1489AN	
MC1489L	DS1489J	
MC1489P	DS1489N	
AM26LS31DC	DS26LS31CJ	
AM26LS31PC	DS26LS31CN	
MC26S10L	DS26S10J	
MC26S10P	DS26S10N	
MC3430L	DS3651J	
MC3430P	DS3651N	
MC3431L		DS3651J
MC3431P		DS3651N
MC3432L	DS3653J	
MC3432P	DS3653N	
MC3433L		DS3653J
MC3433P		DS3653N
MC3437L	DS8837J	
MC3437P	DS8837N	
MC3438L	DS8838J	
MC3438P	DS8838N	
MC3450L		DS3650J
MC3450P		DS3650N
MC3451P		DS3451N
MC3452P	DS3652N	
MC3486L	DS3486J	
MC3486P	DS3486N	
MC3487L	DS3487J	
MC3487P	DS3487N	
MC3490P		DS8887N
MC3491P		DS8889N
MC3494P		DS8897N
MC6880AL	DS8T26AJ	
MC6880AP	DS8T26AN	
MC6889L	DS8T28J	
MC6889P	DS8T28N	
MC75107L	DS75107J	
MC75107P	DS75107N	
MC75108L	DS75108J	
MC75108P	DS75108N	
MC75125L	DS75125J	
MC75125P	DS75125N	
MC75127L	DS75127J	
MC75127P	DS75127N	
MC75128L	DS75128J	
MC75128P	DS75128N	
MC75129L	DS75129J	
MC75129P	DS75129N	
MC75325L	DS75325J	
MC75491P	DS75491N	
MC75492P	DS75492N	
MC8T13L	DS75121J	
MC8T13P	DS75121N	
MC8T14L	DS75122J	
MC8T14P	DS75122N	
MC8T23L	DS75123J	
MC8T23P	DS75123N	
MC8T24L	DS75124J	
MC8T24P	DS75124N	
MC8T26AL	DS8T26AJ	DS8834J
MC8T26AP	DS8T26AN	DS8834N
MC8T28L	DS8T28J	
MC8T28P	DS8T28N	
DS8641N	DS8641N	
DS8641J	DS8641N	

MOTOROLA TO NATIONAL'S INTERFACE

The manufacturer's most current data sheets take precedence over this guide.

Interface Cross Reference Guide (Continued)

Device Designation	National's Direct Replacement	National's Closest Replacement
SIGNETICS		
MC1488F	DS1488J	
MC1488N	DS1488N	
MC1489AN	DS1489AN	
MC1489AF	DS1489AJ	
MC1489F	DS1489J	
MC1489N	DS1489N	
NE582F		DS75494J
NE582N		DS75494N
75S107F		DS75107J
75S107N		DS75107N
75S108F		DS75108J
75S108N		DS75108N
75S207F		DS75207J
75S207N		DS75207N
75S208F		DS75208J
75S208N		DS75208N
N8T13F	DS75121J	
N8T13N	DS75121N	
N8T14F	DS75122J	
N8T14N	DS75122N	
N8T15F		DS75150J-8
N8T15N		DS75150N
N8T23F	DS75123J	
N8T23N	DS75123N	
N8T24F	DS75124J	
N8T24N	DS75124N	
N8T26AF	DS8T26AJ	
N8T26AN	DS8T26AN	
N8T28F	DS8T28J	
N8T28N	DS8T28N	
N8T34F	DS8834J	
N8T34N	DS8834N	
N8T37F	DS8837J	
N8T37N	DS8837N	
N8T38F	DS8838J	
N8T38N	DS8838N	
N8T380F	DS8836J	DS8640J
N8T380N	DS8836N	DS8640N
*DS8820AF	DS8820AJ	
*DS8820AN	DS8820AN	
*DS8820F	DS8820J	
*DS8820N	DS8820N	
*DS8830F	DS8830J	
*DS8830N	DS8830N	
*DS8880F	DS8880J	
*DS8880N	DS8880N	

The manufacturer's most current data sheets take precedence over this guide.

*Signetics has announced plans to obsolete these products.

Interface Cross Reference Guide (Continued)

National Semiconductor

Device Designation	National's Direct Replacement	National's Closest Replacement
SPRAGUE		
UDN3611H	DS3611J-8	
UDN3611M	DS3611N	
UDN3612H	DS3612J-8	
UDN3612M	DS3612N	
UDN3613H	DS3613J-8	
UDN3613M	DS3613N	
UDN3614H	DS3614J-8	
UDN3614M	DS3614N	

he manufacturer's most current data sheets take precedence over this guide.

SPRAGUE TO NATIONAL'S INTERFACE

Interface Cross Reference Guide (Continued)

National Semiconductor

NATIONAL'S INTERFACE TO TEXAS INSTRUMENTS

Device Designation	National's Direct Replacement	National's Closest Replacement
TEXAS INSTRUMENTS		
MC1488J	DS1488J	
MC1488N	DS1488N	
MC1489AJ	DS1489AJ	
MC1489AN	DS1489AN	
MC1489J	DS1489J	
MC1489N	DS1489N	
AM26LS31CJ	DS26LS31CJ	
AM26LS31CN	DS26LS31CN	
AM26LS32ACJ	DS26LS32ACJ	DS26LS32CJ
AM26LS32ACN	DS26LS32ACN	DS26LS32CN
AM26LS33AJ	DS26LS33ACJ	DS26LS33CJ
AM26LS33AN	DS26LS33ACN	DS26LS33CN
AM26S10CJ	DS26S10J	
AM26S10CN	DS26S10N	
AM26S11CJ	DS26S11J	
AM26S11CN	DS26S11N	
MC3486J	DS3486J	
MC3486N	DS3486N	
MC3487J	DS3487J	
MC3487N	DS3487N	
SN74LS424J	DP8224J	
SN74LS424N	DP8224N	
SN74S412J	DP8212J	
SN74S412N	DP8212N	
SN74S428N	DP8228N	
SN74S436N	DS36149N	
SN74S437N	DS36179N	
SN74S438N	DP8238N	
SN75107AJ		DS75107J
SN75107AN		DS75107N
SN75107BJ	DS75107J	
SN75107BN	DS75107N	
SN75108AJ		DS75108J
SN75108AN		DS75108N
SN75108BJ	DS75108J	
SN75108BN	DS75108N	
SN75113J	DS75113J	
SN75113N	DS75113N	
SN75114J	DS75114J	
SN75114N	DS75114N	
SN75115J	DS75115J	
SN75115N	DS75115N	
SN75121J	DS75121J	
SN75121N	DS75121N	
SN75122J	DS75122J	
SN75122N	DS75122N	
SN75123J	DS75123J	
SN75123N	DS75123N	
SN75124J	DS75124J	
SN75124N	DS75124N	
SN75125J	DS75125J	
SN75125N	DS75125N	
SN75127J	DS75127J	
SN75127N	DS75127N	
SN75128J	DS75128J	
SN75128N	DS75128N	
SN75129J	DS75129J	
SN75129N	DS75129N	
SN75150J	DS75150J-8	
SN75150N	DS75150N	
SN75154J	DS75154J	
SN75154N	DS75154N	
SN75160N	DS75160AN	
SN75160AN	DS75160AN	
SN75161N	DS75161AN	
SN75161AN	DS75161AN	
SN75162N	DS75162AN	
SN75162AN	DS75162AN	
SN75182J	DS8820AJ	
SN75182N	DS8820AN	
SN75183J	DS8830J	
SN75183N	DS8830N	
SN75188J	DS1488J	
SN75188N	DS1488N	
SN75189AJ	DS1489AJ	
SN75189AN	DS1489AN	
SN75189J	DS1489J	
SN75189N	DS1489N	
SN75207BN	DS75207N	
SN75207J		DS75207J
SN75208BJ	DS75208J	
SN75208J		DS75208J
SN75208N		DS75208N
SN75325J	DS75325J	
SN75325N	DS75325N	
SN75361AJG	DS75361J-8	
SN75361AP	DS75361N	
SN75365J	DS75365J	
SN75365N	DS75365N	
SN75369J		DS0026CJ-8
SN75369N		DS0026CN
SN75437ANE	DS3658N	
SN75437NE	DS3658N	
SN75450BJ	DS75450J	
SN75450BN	DS75450N	
SN75451BJG	DS75451J-8	
SN75451BP	DS75451N	
SN75452BJG	DS75452J-8	
SN75452BP	DS75452N	
SN75453BJG	DS75453J-8	
SN75453BP	DS75453N	
SN75454BJG	DS75454J-8	
SN75454BP	DS75454N	
SN75461JG	DS75461J-8	
SN75461P	DS75461N	
SN75462JG	DS75462J-8	
SN75462P	DS75462N	
SN75463JG	DS75463J-8	
SN75463P	DS75463N	
SN75464JG	DS75464J-8	
SN75464P	DS75464N	
SN75471JG		DS3611J-8
SN75471P		DS3611N
SN75472JG		DS3612J-8
SN75472P		DS3612N
SN75473JG		DS3613J-8
SN75473P		DS3613N
SN75474JG		DS3614J-8
SN75474P		DS3614N
SN75477JG		DS3612J-8
SN75477P		DS3612N
SN75480N	DS8880N	
SN75491AN		DS75491N
SN75491N	DS75491N	
SN75492AN		DS75492N
SN75492J	DS75492J	
SN75492N	DS75492N	
SN75494N		DS75494N
N8T13J	DS75121J	
N8T13N	DS75121N	
N8T14J	DS75122J	
N8T14N	DS75122N	
N8T23J	DS75123J	
N8T23N	DS75123N	
N8T24J	DS75124J	
N8T24N	DS75124N	
N8T26AJ	DS8T26AJ	
N8T26AN	DS8T26AN	
DS8820AJ	DS8820AJ	
DS8820AN	DS8820AN	
DS8830J	DS8830J	
DS8830N	DS8830N	
DS8831J	DS8831J	
DS8831N	DS8831N	
DS8832J	DS8832J	
DS8832N	DS8832N	

The manufacturer's most current data sheets take precedence over this guide.

Understanding Integrated Circuit Package Power Capabilities

National Semiconductor
Application Note 336
Charles Carinalli
Josip Huljev
March 1983

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

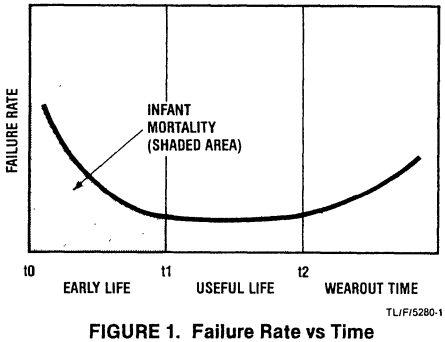


FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30 degree rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

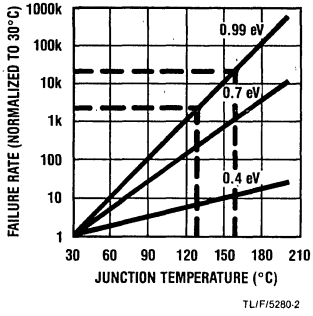


FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3 and 4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit, flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature
T_A = Ambient temperature in the vicinity of the device
P_D = Total power dissipation (in watts)
θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All interface circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using interface components.

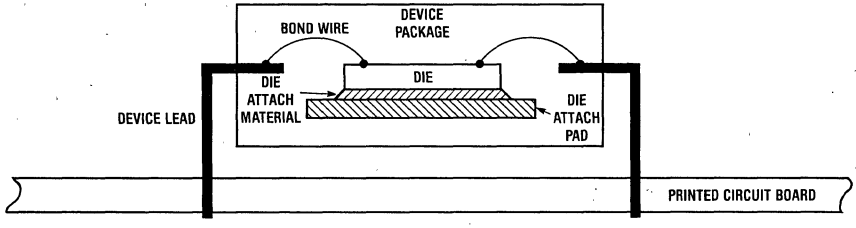


FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

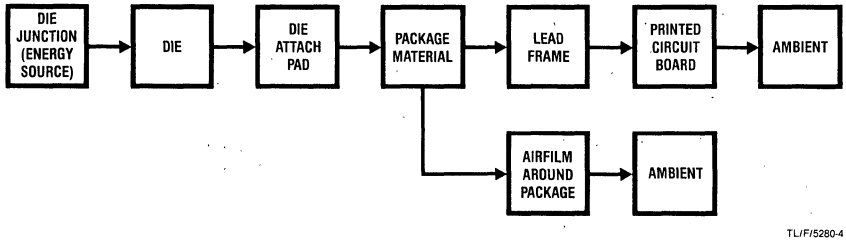


FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C:

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, how safe is 108°C?

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D@25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

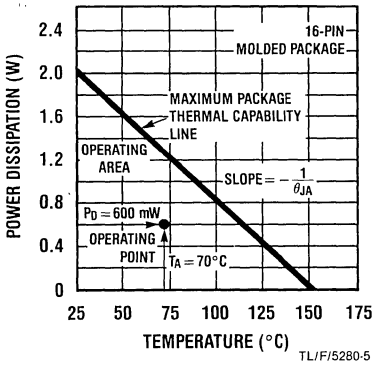


FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all interface circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

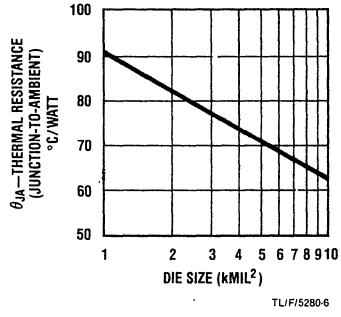


FIGURE 6. Thermal Resistance vs Die Size

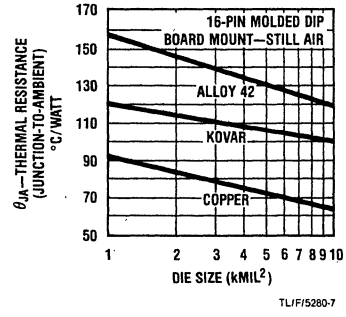


FIGURE 7. Thermal Resistance vs Lead Frame Material

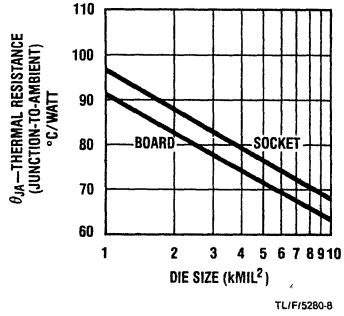


FIGURE 8. Thermal Resistance vs Board or Socket Mount

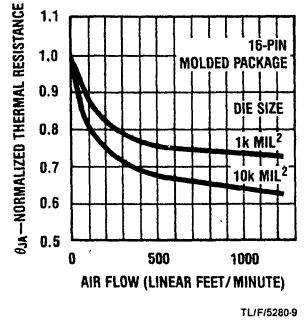


FIGURE 9. Thermal Resistance vs Air Flow

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and 11 show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Interface Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Interface Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ± 10% to ± 15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the interface data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

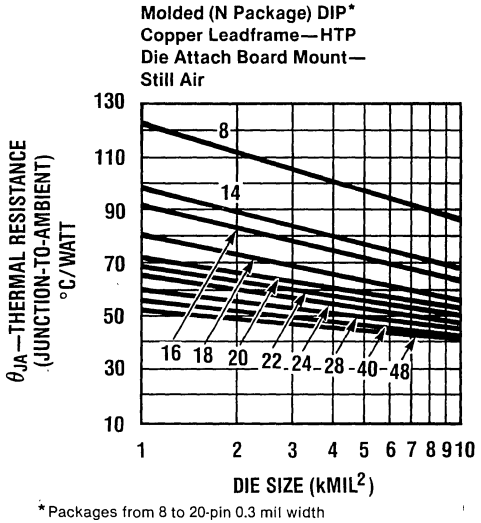
Maximum Power Dissipation* at 25°C

Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

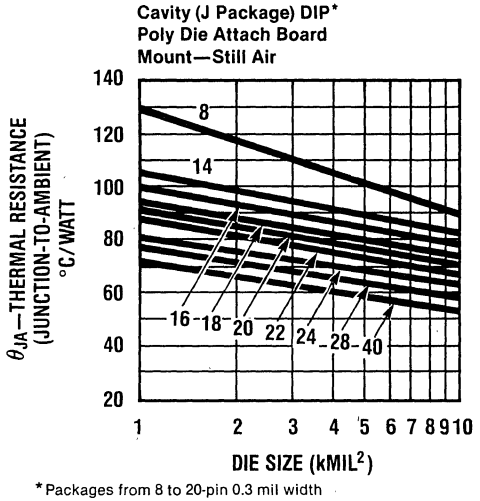
$$P_D @ 70°C = 1476\,mW - (11.8\,mW/°C) \times (70°C - 25°C)$$
$$= 945\,mW$$



*Packages from 8 to 20-pin 0.3 mil width
22-pin 0.4 mil width
24 to 40-pin 0.6 mil width

TL/F/5280-10

FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)



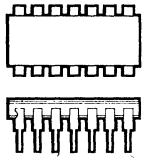
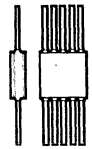
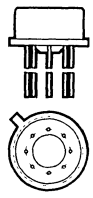
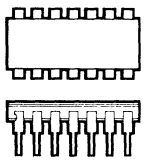
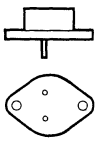
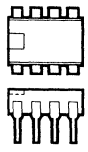
*Packages from 8 to 20-pin 0.3 mil width
22-pin 0.4 mil width
24 to 48-pin 0.6 mil width

TL/F/5280-11

FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

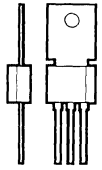
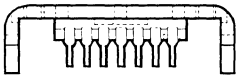
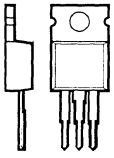
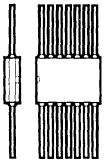
National Semiconductor

Industry Package Cross-Reference Guide

	NSC	Signetics	Fairchild	Motorola	TI	RCA	Silicon General	AMD	Raytheon
 14/16 Lead Glass/Metal DIP	D	I	D	L		D	D	D	D, M
 Glass/Metal Flat-Pack	F	Q	F	F	F, S	K	F	F	J, F, Q
 TO-99, TO-100, TO-5	H	T, K, L, DB	H	G	L	S*, V1**	T	H	T, H
 8, 14 and 16-Lead Low-Temperature Ceramic DIP	J	F	R, D	U	J				DC, DD
 TO-3 (Steel)	K			KS			K		K
TO-3 (Aluminum)	KC	DA	K	K	K		K		LK, TK
 8, 14 and 16-Lead Plastic DIP	N	V, A, B	T, P	P	P, N	E	M, N	PC	N, DN, DP, MP

*With dual-in-line formed leads.

**With radially formed leads.

	NSC	Signetics	Fairchild	Motorola	TI	RCA	Silicon General	AMD	Raytheon
 TO-202 (D-40, Durawatt)	P				KD				
 "SGS" Type Power DIP	S		BP						
 TO-220	T	U	U		KC				
 Low Temperature Glass Hermetic Flat Pack	W		F	F	W			FM	
 TO-92 (Plastic)	Z	S	W	P	LP				

SECTIONS 13 THROUGH 20 FOR FUTURE EXPANSION IN SUPPLEMENT BOOKS

Section 21
Bipolar PROMs

21

Introduction

GENERAL

This generic Schottky PROM family by National Semiconductor makes available to the industry one of the widest selections in sizes and organizations. Four-bit wide PROMs are provided with 256 to 4096 words in pin compatible 16 and 18 pin dual-in-line packages. The 8-bit wide devices range from 32 to 4096 words in a variety of packages. Being 'generic,' all PROMs share a common programming algorithm.

TITANIUM-TUNGSTEN FUSES

National's new Programmable Read-Only Memories (PROMs) feature titanium-tungsten (Ti:W) fuse links designed to program efficiently with only 10.5 Volts applied. The high performance and reliability of these PROMs are the result of fabrication by a Schottky bipolar process, of which the titanium-tungsten metalization is an integral part, and the use of an on-chip programming circuit.

A major advantage of the titanium-tungsten fuse technology is the low programming voltage of the fuse links. At 10.5 Volts, this virtually eliminates the need for guard-ring devices and wide spacings required for other fuse technologies. Care is taken, however, to minimize voltage drops across the die and to reduce parasitics. The device is designed to ensure that worst-case fuse operating current is low enough for reliable long-term operation. The Darlington programming circuit is liberally designed to insure adequate power density for blowing the fuse links. The complete circuit design is optimized to provide high performance over the entire operating ranges of V_{CC} and temperature.

TESTABILITY

The Schottky PROM die includes extra rows and columns of fusable links for testing the programmability of each chip. These test fuses are placed at the worst-case chip locations to provide the highest possible confidence in the programming tests in the final product. A ROM pattern is also permanently fixed in the additional circuitry and coded to provide a parity check of input address levels. These and other test circuits are used to test for correct operation of the row and column-select circuits and functionality of input and enable gates. All test circuits are available at both wafer and assembled device levels to allow 100% functional and parametric testing at every stage of the test flow.

RELIABILITY

As with all National products, the Ti:W PROMs are subjected to an on-going reliability evaluation by the Reliability Assurance Department. These evaluations employ accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. To date, nearly 7.4 million Schottky Ti:W PROM device hours have been logged, with samples in Epoxy B molded DIP (N-package) and CERDIP (J-package). Device performance in all package configurations is excellent.

Bipolar PROM Selection Guide

Size (Bits)	Organization		DIP (Pins)	Part Number	TAA (Max) in nS	TEA (Max) in nS	ICC (Max) in mA	Temperature Celsius
256	32 x 8	OC	16	DM54S188	45	30	110	−55 to +125
	32 x 8	OC	16	DM74S188	35	20	110	0 to +70
	32 x 8	TS	16	DM54S288	45	30	110	−55 to +125
	32 x 8	TS	16	DM74S288	35	20	110	0 to +70
1024	256 x 4	OC	16	DM54S387	60	30	130	−55 to +125
	256 x 4	OC	16	DM74S387	50	25	130	0 to +70
	256 x 4	TS	16	DM54S287	60	30	130	−55 to +125
	256 x 4	TS	16	DM74S287	50	25	130	0 to +70
2048	512 x 4	OC	16	DM54S570	65	35	130	−55 to +125
	512 x 4	OC	16	DM74S570	55	30	130	0 to +70
	512 x 4	TS	16	DM54S571	65	35	130	−55 to +125
	512 x 4	TS	16	DM74S571	55	30	130	0 to +70
	512 x 4	OC	16	DM54S570A	60	35	130	−55 to +125
	512 x 4	OC	16	DM74S570A	45	25	130	0 to +70
	512 x 4	TS	16	DM54S571A	60	35	130	−55 to +125
	512 x 4	TS	16	DM74S571A	45	25	130	0 to +70
	512 x 4	TS	16	DM54S571B	50	35	130	−55 to +125
	512 x 4	TS	16	DM74S571B	35	25	130	0 to +70
	256 x 8	TS	20	DM54LS471	70	35	100	−55 to +125
	256 x 8	TS	20	DM74LS471	60	30	100	0 to +70
4096	512 x 8	OC	20	DM54S473	75	35	155	−55 to +125
	512 x 8	OC	20	DM74S473	60	30	155	0 to +70
	512 x 8	TS	20	DM54S472	75	35	155	−55 to +125
	512 x 8	TS	20	DM74S472	60	30	155	0 to +70
	512 x 8	OC	20	DM54S473A	60	35	155	−55 to +125
	512 x 8	OC	20	DM74S473A	45	25	155	0 to +70
	512 x 8	TS	20	DM54S472A	60	35	155	−55 to +125
	512 x 8	TS	20	DM74S472A	45	25	155	0 to +70
	512 x 8	TS	20	DM54S472B	50	35	155	−55 to +125
	512 x 8	TS	20	DM74S472B	35	25	155	0 to +70
	512 x 8	OC	24	DM54S475	75	40	170	−55 to +125
	512 x 8	OC	24	DM74S475	65	35	170	0 to +70
	512 x 8	TS	24	DM54S474	75	40	170	−55 to +125
	512 x 8	TS	24	DM74S474	65	35	170	0 to +70
	512 x 8	OC	24	DM54S475A	60	35	170	−55 to +125
	512 x 8	OC	24	DM74S475A	45	25	170	0 to +70
	512 x 8	TS	24	DM54S474A	60	35	170	−55 to +125
	512 x 8	TS	24	DM74S474A	45	25	170	0 to +70
	512 x 8	TS	24	DM54S474B	50	35	170	−55 to +125
	512 x 8	TS	24	DM74S474B	35	25	170	0 to +70
	512 x 8	REG	24*	DM77SR474	40**	30	185	− 55 to + 125
	512 x 8	REG	24*	DM87SR474	35**	25	185	0 to + 70
	512 x 8	REG	24*	DM77SR476	40**	30	185	− 55 to + 125
	512 x 8	REG	24*	DM77SR25	40**	30	185	− 55 to + 125
	512 x 8	REG	24*	DM87SR476	35**	25	185	0 to + 70
	512 x 8	REG	24*	DM87SR25	35**	25	185	0 to + 70
	1024 x 4	OC	18	DM54S572	75	45	140	−55 to +125
	1024 x 4	OC	18	DM74S572	60	35	140	0 to +70
	1024 x 4	TS	18	DM54S573	75	45	140	−55 to +125
	1024 x 4	TS	18	DM74S573	60	35	140	0 to +70
	1024 x 4	OC	18	DM54S572A	60	35	140	−55 to +125
	1024 x 4	OC	18	DM74S572A	45	25	140	0 to +70
	1024 x 4	TS	18	DM54S573A	60	35	140	−55 to +125
	1024 x 4	TS	18	DM74S573A	45	25	140	0 to +70
	1024 x 4	TS	18	DM54S573B	50	35	140	−55 to +125
	1024 x 4	TS	18	DM74S573B	35	25	140	0 to +70

* – 24 Pin Narrow Dual Inline Package

** – Set up Time

Bipolar PROM Selection Guide

Size (Bits)	Organization		DIP (Pins)	Part Number	TAA (Max) in nS	TEA (Max) in nS	ICC (Max) in mA	Temperature Celsius
8192	1024 x 8	OC	24	DM77S180	75	35	170	−55 to +125
	1024 x 8	TS	24*	DM77S280	75	35	170	−55 to +125
	1024 x 8	OC	24	DM87S180	55	30	170	0 to +70
	1024 x 8	TS	24*	DM87S280	55	30	170	0 to +70
	1024 x 8	OC	24	DM77S181	75	35	170	−55 to +125
	1024 x 8	TS	24*	DM77S281	75	35	170	−55 to +70
	1024 x 8	OC	24	DM87S181	55	30	170	0 to +70
	1024 x 8	TS	24*	DM87S281	55	30	170	0 to +70
	1024 x 8	TS	24	DM77LS181	175	70	100	−55 to +125
	1024 x 8	TS	24	DM87LS181	120	50	100	0 to +70
	1024 x 8	TS	24	DM77S181A	65	35	170	−55 to +125
	1024 x 8	TS	24	DM87S181A	45	30	170	0 to +70
	1024 x 8	REG.	24*	DM77SR181	50**	30	175	−55 to +125
	1024 x 8	REG.	24*	DM87SR181	40**	25	175	0 to +70
	2048 x 4	OC	18	DM77S184	75	35	140	−55 to +125
	2048 x 4	OC	18	DM87S184	55	30	140	0 to +70
	2048 x 4	TS	18	DM77S185	75	35	140	−55 to +125
	2048 x 4	TS	18	DM87S185	55	30	140	0 to +70
	2048 x 4	TS	18	DM77S185A	60	30	140	−55 to +125
	2048 x 4	TS	18	DM87S185A	45	25	140	0 to +70
	2048 × 4	TS	18	DM77S185B	50	30	140	−55 to +125
	2048 × 4	TS	18	DM87S185B	35	25	140	0 to +70
16384	2048 x 8	OC	24	DM77S190	80	40	175	−55 to +125
	2048 x 8	TS	24*	DM77S290	80	40	175	−55 to +125
	2048 x 8	OC	24	DM87S190	65	30	175	0 to +70
	2048 x 8	TS	24*	DM87S290	65	30	175	0 to +70
	2048 x 8	OC	24	DM77S191	80	40	175	−55 to +125
	2048 x 8	TS	24*	DM77S291	80	40	175	−55 to +125
	2048 x 8	OC	24	DM87S191	65	30	175	0 to +70
	2048 x 8	TS	24*	DM87S291	65	30	175	0 to +70
	2048 x 8	TS	24	DM77S191A	60	35	175	−55 to +125
	2048 x 8	TS	24	DM87S191A	45	30	175	0 to +70
	2048 × 8	TS	24	DM77S191B	50	30	175	−55 to +125
	2048 × 8	TS	24	DM87S191B	35	25	175	0 to +70
	4096 × 4	TS	20	DM77S195A	60	30	170	−55 to +125
	4096 × 4	TS	20	DM87S195A	45	25	170	0 to +70
	4096 × 4	TS	20	DM77S195B	50	30	170	−55 to +125
	4096 × 4	TS	20	DM87S195B	35	25	170	0 to +70
32768	4096 × 8	TS	24	DM77S321	65	35	185	−55 to +125
	4096 × 8	TS	24	DM87S321	55	30	185	0 to +70
	4096 × 8	TS	24*	DM77S421	65	35	185	−55 to +125
	4096 × 8	TS	24*	DM87S421	55	30	185	0 to +70

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	-0.5 to +7.0V
Input Voltage (Note 2)	-1.2 to +5.5V
Output Voltage (Note 2)	-0.5 to +5.5V
Storage Temperature	-65 to +150C
Lead Temperature (10 seconds)	300C

* -- 24 Pin Narrow Dual Inline Package

** – Set up Time

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
Military	4.50	5.50	V
Commercial	4.75	5.25	V
Ambient Temperature (T_A)			
Military	−55	+125	°C
Commercial	0	+70	°C
Logical "0" Input Voltage	0	0.8	V
Logical "1" Input Voltage	2.0	5.5	V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits do not apply during programming. For the programming ratings, refer to the programming instructions.

National Semiconductor

DM54/74S188, DM54/74S288 (32 X 8) 256-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 32 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

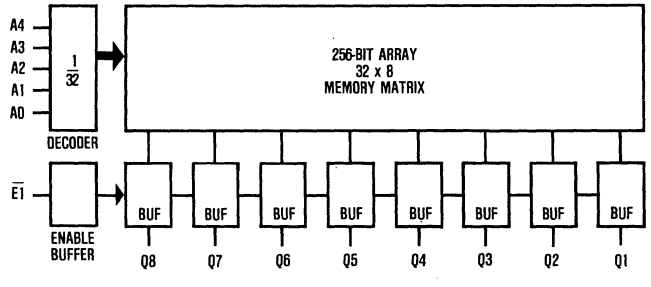
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

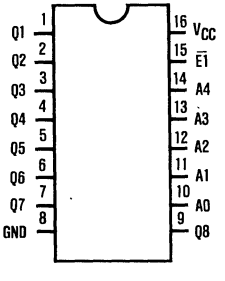
Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—22ns typ
  - Enable access—15ns typ
  - Enable recovery—15ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S188		X	X		N,J
DM74S288		X		X	N,J
DM54S188	X		X		J
DM54S288	X			X	J

Block and Connection Diagram





Order Number;
DM74S188 J, DM74S288 J,
DM54S188 J, DM54S288 J
See NS Package J16A

Order Number;
DM74S188 N or DM74S288 N
See NS Package N16A

DC Electrical Characteristics (Note 3)

Sym	Parameter	Conditions	DM54S188/288			DM74S188/288			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		-80	-250		-80	-250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		70	110		70	110	mA
TRI-STATE® Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	-20		-70	-20		-70	mA
I_{OZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V			+50			+50	μA
	(TRI-STATE)	Chip Disabled			-50			-50	μA
V_{OH}	Output Voltage High	I_{OH} = -2.0mA	2.4	3.2					V
		I_{OH} = −6.5mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol	DM54S188/288			DM74S188/288			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		22	45		22	35	ns
TEA	Enable Access Time	TEVQV		15	30		15	20	ns
TER	Enable Recovery Time	TEXQX		15	35		15	25	ns
TZX	Output Enable Time	TEVQX		15	30		15	20	ns
TXZ	Output Disable Time	TEXQZ		15	35		15	25	ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

DM54/74S387, DM54/74S287 (256 X 4) 1024-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 256 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

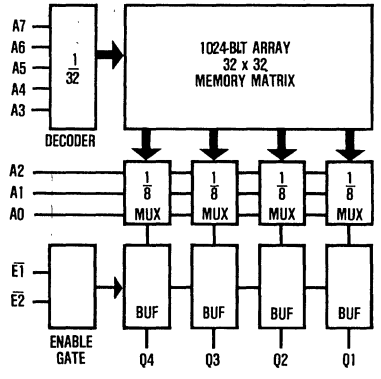
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

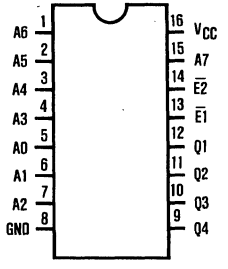
Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—35ns typ
  - Enable access—15ns typ
  - Enable recovery—15ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S387		X	X		N,J
DM74S287		X		X	N,J
DM54S387	X		X		J
DM54S287	X			X	J

Block and Connection Diagram





Order Number;
DM74S387 J, DM74S287 J,
DM54S387 J, DM54S287 J
See NS Package J16A

Order Number;
DM74S387 N or DM74S287 N
See NS Package N16A

DC Electrical Characteristics (Note 3)

Sym	Parameter	Conditions	DM54S387/287			DM74S387/287			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		-80	-250		-80	-250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		80	130		80	130	mA
TRI-STATE® Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	-20		-70	-20		-70	mA
I_{OZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V			+50			+50	μA
	(TRI-STATE)	Chip Disabled			-50			-50	μA
V_{OH}	Output Voltage High	I_{OH} = -2.0mA	2.4	3.2					V
		I_{OH} = 6.5mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol	DM54S387/287			DM74S387/287			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		35	60		35	50	ns
TEA	Enable Access Time	TEVQV		15	30		15	25	ns
TER	Enable Recovery Time	TEXQX		15	30		15	25	ns
TZX	Output Enable Time	TEVQX		15	30		15	25	ns
TXZ	Output Disable Time	TEXQZ		15	30		15	25	ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

DM54/74S570, DM54/74S571; DM54/74S570A, DM54/74S571A; DM54/74S571B (512 x 4) 2048-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 512 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

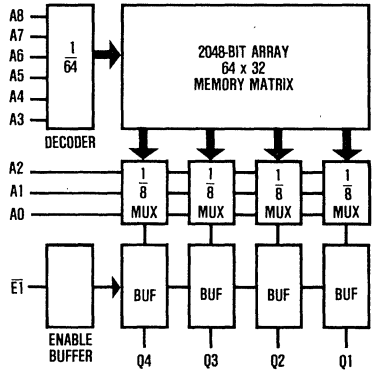
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

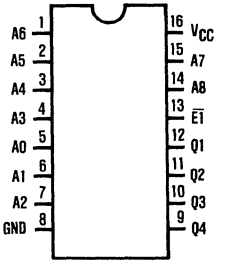
Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—30ns typ
  - Enable access—15ns typ
  - Enable recovery—15ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S570		X	X		N,J
DM74S571		X		X	N,J
DM54S570	X		X		J
DM54S571	X			X	J

Block and Connection Diagram





Order Number;
DM74S570 J, DM74S571 J,
DM54S570 J, or DM54S571 J
See NS Package J16A

Order Number;
DM74S570 N or DM74S571 N
See NS Package N16A

DC Electrical Characteristics (Note 3)

Sym	Parameter	Conditions	DM54S570/571			DM74S570/571			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		-80	-250		-80	-250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		90	130		90	130	mA
TRI-STATE® Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	-20		-70	-20		-70	mA
I_{OZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V			+50			+50	μA
	(TRI-STATE)	Chip Disabled			-50			-50	μA
V_{OH}	Output Voltage High	I_{OH} = -2.0mA	2.4	3.2					V
		I_{OH} = 6.5mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol	DM54S570/571			DM74S570/571			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		40	65		40	55	ns
TEA	Enable Access Time	TEVQV		20	35		20	30	ns
TER	Enable Recovery Time	TEXQX		20	35		20	30	ns
TZX	Output Enable Time	TEVQX		20	35		20	30	ns
TXZ	Output Disable Time	TEXQZ		20	35		20	30	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol		DM54S571A, B/570A			DM74S571A, B/570A			Units
				Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV	571A/570A		30	60		30	45	ns
			571B		30	50		30	35	ns
TEA	Enable Access Time	TEVQV			15	35		15	25	ns
TER	Enable Recovery Time	TEXQX			15	35		15	25	ns
TZX	Output Enable Time	TEVQX			15	35		15	25	ns
TXZ	Output Disable Time	TEXQZ			15	35		15	25	ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

DM54/74LS471
(256 X 8) 2048-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 256 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state.

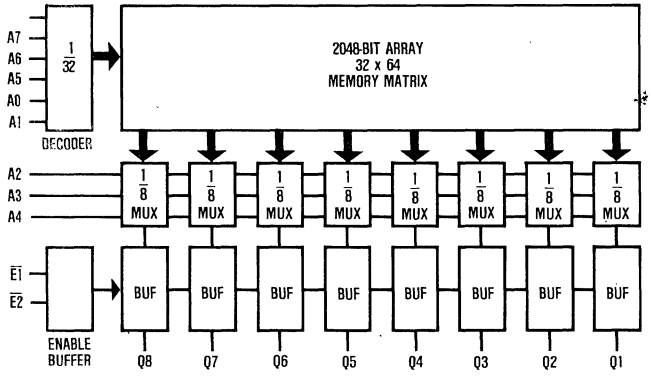
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

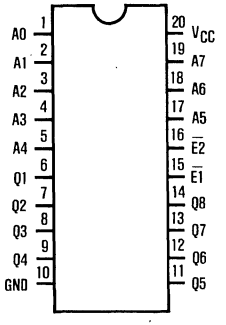
Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—40ns typ
  - Enable access—15ns typ
  - Enable recovery—15ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74LS471		X		X	N,J
DM54LS471	X			X	J

Block and Connection Diagram





Order Number;
DM74LS471 J,
DM54LS471 J,
See NS Package J20B

Order Number;
DM74LS471 N
See NS Package N20A

DC Electrical Characteristics (Note 3)

Sym	Parameter	Conditions	DM54LS471			DM74LS471			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		-80	-250		-80	-250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		75	100		75	100	mA
TRI-STATE® Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	-20		-70	-20		-70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V			+50			+50	μA
		Chip Disabled			-50			-50	μA
V_{OH}	Output Voltage High	I_{OH} = -2.0mA	2.4	3.2					V
		I_{OH} = 6.5mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol	DM54LS471			DM74LS471			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		45	70		40	60	ns
TEA	Enable Access Time	TEVQV		15	35		15	30	ns
TER	Enable Recovery Time	TEXQX		15	35		15	30	ns
TZX	Output Enable Time	TEVQX		15	35		15	30	ns
TXZ	Output Disable Time	TEXQZ		15	35		15	30	ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

DM54/74S473, DM54/74S472; DM54/74S473A, DM54/74S472A; DM54/74S472B (512 × 8) 4096-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

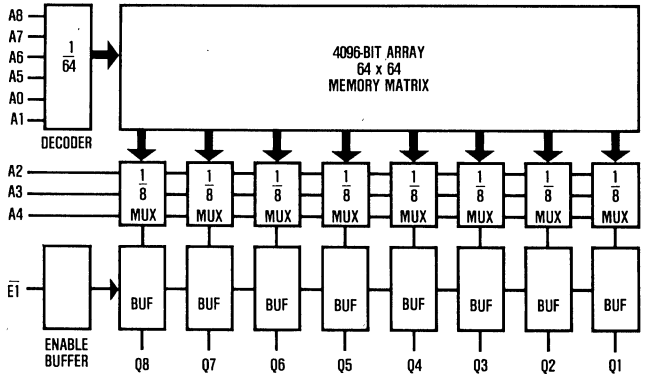
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

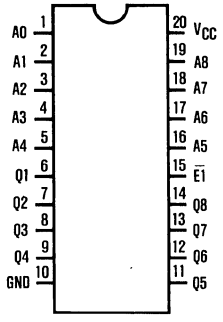
Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—25ns typ
  - Enable access—15ns typ
  - Enable recovery—15ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S473		X	X		N,J
DM74S472		X		X	N,J
DM54S473	X		X		J
DM54S472	X			X	J

Block and Connection Diagram





Order Number;
DM74S473 J, DM74S472 J,
DM54S473 J, or DM54S472 J
See NS Package J20B

Order Number;
DM74S473 N or DM74S472 N
See NS Package N20A

DC Electrical Characteristics (Note 3)

Sym	Parameter	Conditions	DM54S473/472			DM74S473/472			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		-80	-250		-80	-250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		110	155		110	155	mA
TRI-STATE® Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	-20		-70	-20		-70	mA
I_{OZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V			+50			+50	μA
	(TRI-STATE)	Chip Disabled			-50			-50	μA
V_{OH}	Output Voltage High	I_{OH} = -2.0mA	2.4	3.2					V
		I_{OH} = 6.5mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol	DM54S473/472			DM74S473/472			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		40	75		40	60	ns
TEA	Enable Access Time	TEVQV		15	35		15	30	ns
TER	Enable Recovery Time	TEXQX		15	35		15	30	ns
TZX	Output Enable Time	TEVQX		15	35		15	30	ns
TXZ	Output Disable Time	TEXQZ		15	35		15	30	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol		DM54S473A/472A, B			DM74S473A/472A, B			Units
				Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV	473A/472A		25	60		25	45	ns
			472B		25	50		25	35	ns
TEA	Enable Access Time	TEVQV	473A/472A		15	35		15	30	ns
			472B		15	35		15	25	ns
TER	Enable Recovery Time	TEXQX	473A/472A		15	35		15	30	ns
			472B		15	35		15	25	ns
TZX	Output Enable Time	TEVQX	473A/472A		15	35		15	30	ns
			472B		15	35		15	25	ns
TXZ	Output Disable Time	TEXQZ	473A/472A		15	35		15	30	ns
			472B		15	35		15	25	ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

DM54/74S475, DM54/74S474; DM54/74S475A, DM54/74S474A; DM54/74S474B (512 x 8) 4096-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 512 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

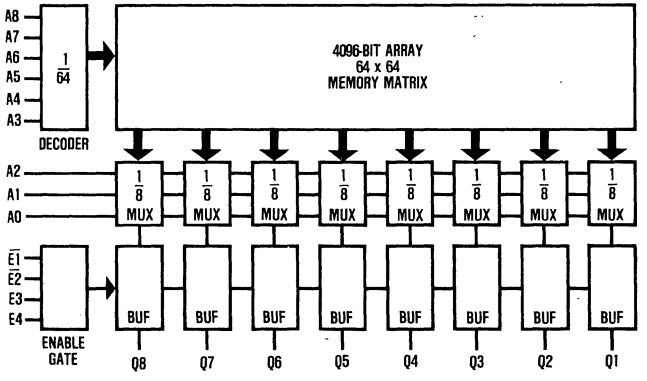
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

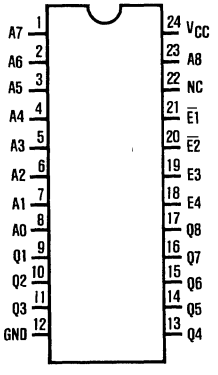
Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—25ns typ
  - Enable access—15ns typ
  - Enable recovery—15ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S475		X	X		N,J
DM74S474		X		X	N,J
DM54S475	X		X		J
DM54S474	X			X	J

Block and Connection Diagram





Order Number:
DM74S475 J, DM74S474 J,
DM54S475 J, or DM54S474 J
See NS Package J24A

Order Number:
DM74S475 N or DM74S474 N
See NS Package N24A

DC Electrical Characteristics (Note 3)

Sym	Parameter	Conditions	DM54S475/474			DM74S475/474			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		-80	-250		-80	-250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		115	170		115	170	mA
TRI-STATE® Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	-20		-70	-20		-70	mA
I_{OZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V			+50			+50	μA
	(TRI-STATE)	Chip Disabled			-50			-50	μA
V_{OH}	Output Voltage High	I_{OH} = -2.0mA	2.4	3.2					V
		I_{OH} = 6.5mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol	DM54S475/474			DM74S475/474			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		40	75		40	65	ns
TEA	Enable Access Time	TEVQV		20	40		20	35	ns
TER	Enable Recovery Time	TEXQX		20	40		20	35	ns
TZX	Output Enable Time	TEVQX		20	40		20	35	ns
TXZ	Output Disable Time	TEXQZ		20	40		20	35	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol		DM54S475A/474A, B			DM74S475A/474A, B			Units
				Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV	475A/474A		25	60		25	45	ns
			474B		25	50		25	35	ns
TEA	Enable Access Time	TEVQV			15	35		15	25	ns
TER	Enable Recovery Time	TEXQX			15	35		15	25	ns
TZX	Output Enable Time	TEVQX			15	35		15	25	ns
TXZ	Output Disable Time	TEXQZ			15	35		15	25	ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

Bipolar PROMs
PRELIMINARY

DM77/87SR474, DM77/87SR474B (512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR474 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR474 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0-A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

The DM77/87SR474 also features an initialize function, $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of the $\overline{INIT}$ is all lows, providing a $\overline{CLEAR}$ function when not programmed.

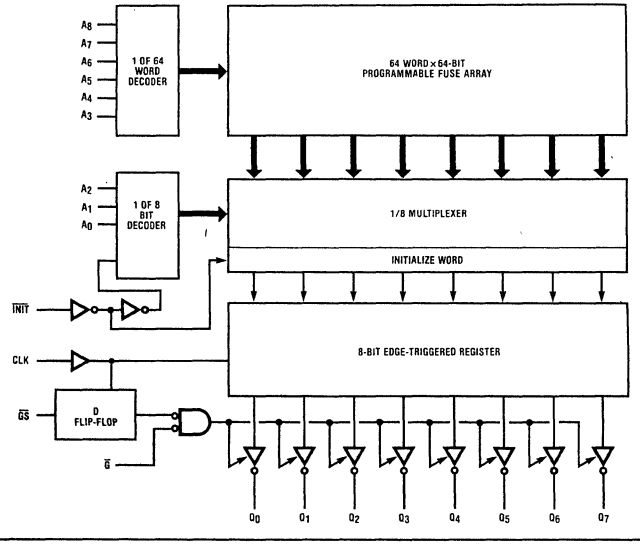
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

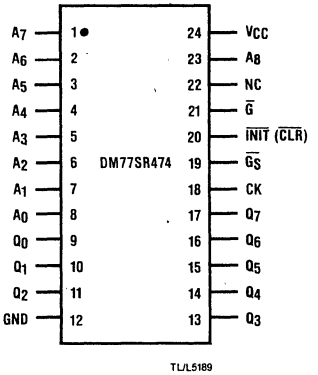
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable synchronous register INITIALIZE
- 24-pin, 300 mil thin-dip package
- 35ns address setup and 20ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature
- Pinout compatible with DM77SR181 (1k x 8) Registered PROM for future expansion

TRI-STATE® is a registered trademark of National Semiconductor Corp.
TRI-SAFE™ is a trademark of National Semiconductor Corp.

Block and Connection Diagrams



TL/L5189



TL/L5189

Order Number DM77SR474J, DM87SR474J, DM87SR474N, DM77SR474BJ, DM87SR474BJ or DM87SR474BN
See NS Package J24F or N24C

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77SR474			DM87SR474			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}	Input Load Current	V_{CC} = Max., V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max., V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max., V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{CEX} = 2.4V			50			50	μA
V_C	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max., Inputs Grounded All Outputs Open		135	185		135	185	mA
	TRI-STATE Parameters								
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max. (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max., V_O = 0.45 to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0mA	2.4	3.2					V
		I_{OH} = −6.5mA				2.4	3.2		V

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.
Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR474			DM87SR474			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{S(A)}$	Address to CLK (High) Setup Time	SR474	55	20		50	20		ns
		SR474B	40	20		35	20		
$t_{H(A)}$	Address to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ to CLK (High) Setup Time		30	20		25	20		ns
$t_{H(\overline{INIT})}$	$\overline{INIT}$ to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(CLK)}$ $t_{PLH(CLK)}$	Delay from CLK (High) to Output (High or Low)	SR474		15	30		15	27	ns
		SR474B		15	25		15	20	
$t_{WH(CLK)}$ $t_{WL(CLK)}$	CLK Width (High or Low)		25	13		20	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to CLK (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to CLK (High) Hold Time		5	0		5	0		ns
$t_{PZL(CLK)}$ $t_{PZH(CLK)}$	Delay from CLK (High) to Output Active (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Output Active (High or Low)			15	30		15	25	ns
$t_{PLZ(CLK)}$ $t_{PHZ(CLK)}$	Delay from CLK (High) to Output Inactive (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (Low) to Output Inactive (TRI-STATE)			15	30		15	25	ns

National Semiconductor

Bipolar PROMs
PRELIMINARY

DM77/87SR476, DM77/87SR25, DM77/87SR476B, DM77/87SR25B (512 x 8) 4k-Bit Registered TTL PROM

General Description

The DM77/87SR476 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8-bits and is available in the TRI-STATE® output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR476 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0-A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

The DM77SR476 also features an initialize function, $\overline{INIT}$.

TRI-STATE® is a registered trademark of National Semiconductor Corp.
TRI-SAFE™ is a trademark of National Semiconductor Corp.

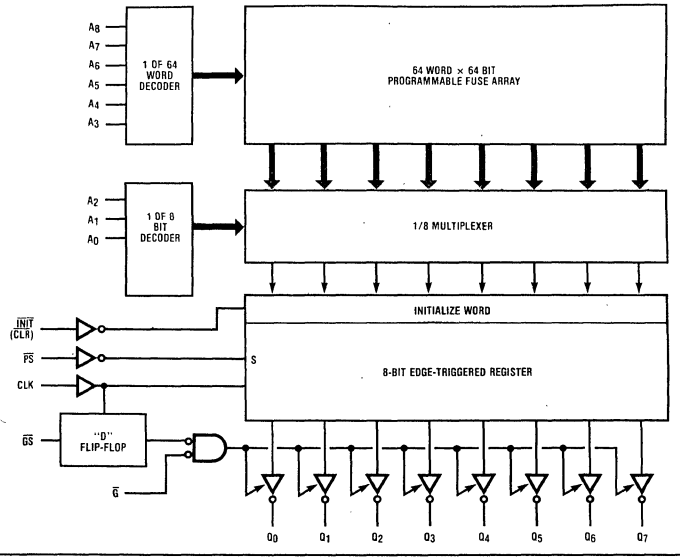
The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the output register when $\overline{INIT}$ is brought low. The unprogrammed state of the $\overline{INIT}$ is all lows, which makes it compatible with the CLEAR function on the AM27S25. $\overline{PS}$ loads ones into the output registers when brought low.

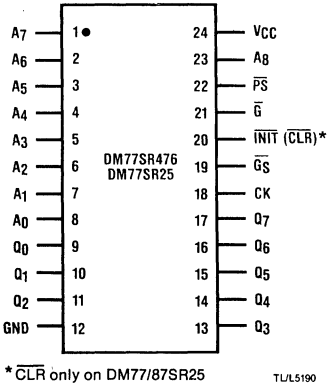
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with AM27S25
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable asynchronous INITIALIZE (SR476 only)
- 24-pin, 300 mil thin-dip package
- 35ns address setup and 20ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature
- Preset input

Block and Connection Diagrams





* $\overline{CLR}$ only on DM77/87SR25 TL/L/5190

Order Number DM77SR476J, DM77SR25J, DM77/87SR476N, DM77/87SR25N, DM77SR476BJ, DM77SR25BJ, DM77/87SR476BN or DM77/87SR25BN
See NS Package J24F or N24C

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77SR476, 476B DM77SR25, 25B			DM87SR476, 476B DM87SR25, 25B			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}	Input Load Current	V_{CC} = Max., V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max., V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max., V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{CEX} = 2.4V			50			50	μA
V_C	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max., Inputs Grounded All Outputs Open		135	185		135	185	mA
	TRI-STATE Parameters								
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max. (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max., V_O = 0.45 to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0mA	2.4	3.2					V
		I_{OH} = −6.5mA				2.4	3.2		V

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.
Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter		DM77SR476, 476B DM77SR25, 25B			DM87SR476, 476B DM87SR25, 25B			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{S(A)}$	Address to CLK (High) Setup Time	SR476, SR25	55	20		50	20		ns
		SR476B, SR25B	40	20		35	20		
$t_{H(A)}$	Address to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(CLK)}$ $t_{PLH(CLK)}$	Delay from CLK (High) to Output (High or Low)	SR476, SR25		15	30		15	27	ns
		SR476B, SR25B		15	25		15	20	
$t_{WH(CLK)}$ $t_{WL(CLK)}$	CLK Width (High or Low)		25	13		25	13		ns
$t_{S(\overline{GS})}$	$\overline{GS}$ to CLK (High) Setup Time		10	0		10	0		ns
$t_{H(\overline{GS})}$	$\overline{GS}$ to CLK (High) Hold Time		5	0		5	0		ns
$t_{PLH(\overline{PS})}$	Delay from $\overline{PS}$ (Low) to Output (High)			20	30		20	25	ns
$t_{PLH(\overline{INIT})}$ $t_{PHL(\overline{INIT})}$	Delay from $\overline{INIT}$ (Low) to Output (Low or High)			20	30		20	25	ns
$t_{WL(\overline{PS})}$	$\overline{PS}$ Pulse Width (Low)		15	10		15	10		ns
$t_{WL(\overline{INIT})}$	$\overline{INIT}$ Pulse Width (Low)		15	10		15	10		
$t_{S(\overline{PS})}$	$\overline{PS}$ Recovery (High) to CLK (High)		25	10		20	10		ns
$t_{S(\overline{INIT})}$	$\overline{INIT}$ Recovery (High) to CLK (High)		25	10		20	10		ns
$t_{PZL(CLK)}$ $t_{PZH(CLK)}$	Delay from CLK (High) to Active Output (High or Low)			20	35		20	30	ns
$t_{PZL(\overline{G})}$ $t_{PZH(\overline{G})}$	Delay from $\overline{G}$ (Low) to Active Output (Low or High)			15	30		15	25	ns
$t_{PLZ(CLK)}$ $t_{PHZ(CLK)}$	Delay from CLK (High) to Inactive Output (TRI-STATE)			20	35		20	30	ns
$t_{PLZ(\overline{G})}$ $t_{PHZ(\overline{G})}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns

National Semiconductor

DM54/74S572, DM54/74S573; DM54/74S572A, DM54/74S573A; DM54/74S573B (1024 x 4) 4096-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 1024 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

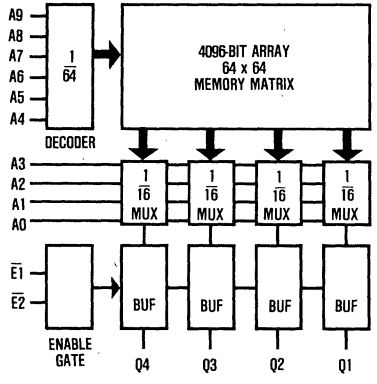
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

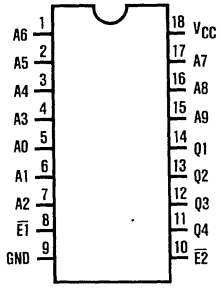
- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—25ns typ
  - Enable access—15ns typ
  - Enable recovery—15ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM74S572		X	X		N,J
DM74S573		X		X	N,J
DM54S572	X		X		J
DM54S573	X			X	J

Block and Connection Diagram



Order Number;
DM74S572 J, DM74S573 J,
DM54S572 J, or DM54S573 J
See NS Package J18A



Order Number;
DM74S572 N or DM74S573 N
See NS Package N18A

DC Electrical Characteristics (Note 3)

Sym	Parameter	Conditions	DM54S572/573			DM74S572/573			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		-80	-250		-80	-250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		100	140		100	140	mA
TRI-STATE® Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	-20		-70	-20		-70	mA
I_{OZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V			+50			+50	μA
	(TRI-STATE)	Chip Disabled			-50			-50	μA
V_{OH}	Output Voltage High	I_{OH} = -2.0mA	2.4	3.2					V
		I_{OH} = 6.5mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol	DM54S572/573			DM74S572/573			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		40	75		40	60	ns
TEA	Enable Access Time	TEVQV		20	45		20	35	ns
TER	Enable Recovery Time	TEXQX		20	45		20	35	ns
TZX	Output Enable Time	TEVQX		20	45		20	35	ns
TXZ	Output Disable Time	TEXQZ		20	45		20	35	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol		DM54S572A/573A, B			DM74S572A/573A, B			Units
				Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV	572A/573A		25	60		25	45	ns
			573B		25	50		25	35	ns
TEA	Enable Access Time	TEVQV			15	35		15	25	ns
TER	Enable Recovery Time	TEXQX			15	35		15	25	ns
TZX	Output Enable Time	TEVQX			15	35		15	25	ns
TXZ	Output Disable Time	TEXQZ			15	35		15	25	ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result

National Semiconductor

DM77/87S180/DM77/87S181; DM77/87S181A; DM77/87S280/DM77/87S281; DM77/87S281A (1024 × 8) 8192-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 1024 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

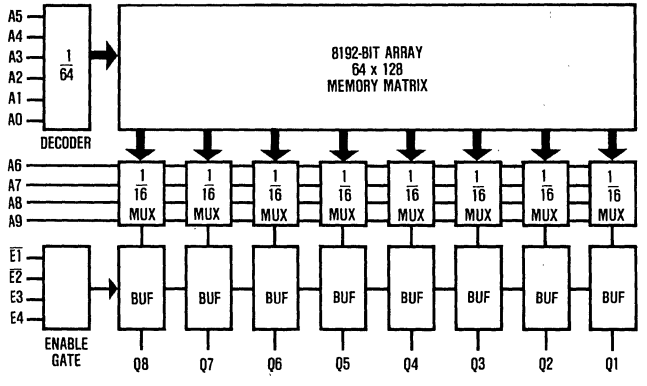
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

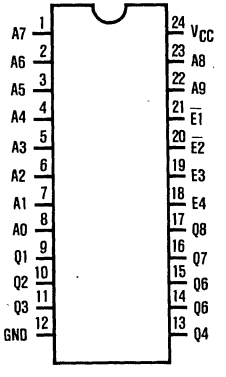
Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—35ns typ
  - Enable access—15ns typ
  - Enable recovery—15ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package	24-Pin Standard	24-Pin Narrow-Dip
DM87S180		X	X		N,J	X	
DM87S181		X		X	N,J	X	
DM77S180	X		X		J	X	
DM77S181	X			X	J	X	
DM87S280		X	X		N,J		X
DM87S281		X		X	N,J		X
DM77S280	X		X		J		X
DM77S281	X			X	J		X

Block and Connection Diagram





Order Number;
DM87S180 J, DM87S181 J,
DM77S180 J, DM77S181 J
See NS Package J24A

Order Number:
DM87S280 J, DM87S281 J,
DM77S280 J, DM77S281 J
See NS Package J24C

Order Number;
DM87S180 N or DM87S181 N
See NS Package N24A

Order Number:
DM87S280 N, or DM87S281 N
See NS Package N24C

DC Electrical Characteristics (Note 3)

Sym	Parameter	Conditions	DM77S180/181 DM77S280/281			DM87S180/181 DM87S280/281			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		-80	-250		-80	-250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open		115	170		115	170	mA
TRI-STATE® Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	-20		-70	-20		-70	mA
I_{OZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V			+50			+50	μA
	(TRI-STATE)	Chip Disabled			-50			-50	μA
V_{OH}	Output Voltage High	I_{OH} = -2.0mA	2.4	3.2					V
		I_{OH} = 6.5mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol	DM77S180/181 DM77S280/281			DM87S180/181 DM87S280/281			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		40	75		40	55	ns
TEA	Enable Access Time	TEVQV		15	35		15	30	ns
TER	Enable Recovery Time	TEXQX		15	35		15	30	ns
TZX	Output Enable Time	TEVQX		15	35		15	30	ns
TXZ	Output Disable Time	TEXQZ		15	35		15	30	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Sym	Parameter	JEDEC Symbol	DM77S181A			DM87S181A			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV		35	65		35	45	ns
TEA	Enable Access Time	TEVQV		15	35		15	30	ns
TER	Enable Recovery Time	TEXQX		15	35		15	30	ns
TZX	Output Enable Time	TEVQX		15	35		15	30	ns
TXZ	Output Disable Time	TEXQZ		15	35		15	30	ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

DM77/87LS181
(1024 X 8) 8192-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 1024 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in TRI-STATE® versions.

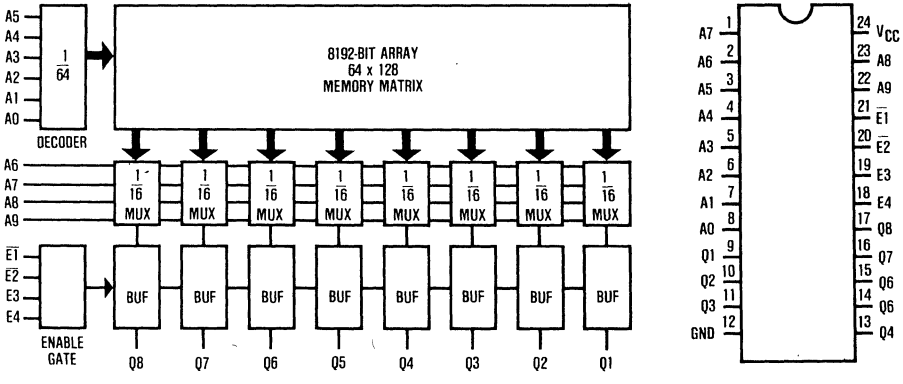
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—100ns typ
  - Enable access—35ns typ
  - Enable recovery—35ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87LS181		X		X	N,J
DM77LS181	X			X	J

Block and Connection Diagram



Order Number;
DM87LS181-J,
or DM77LS181-J
See NS Package J24A

Order Number;
DM87LS181-N
See NS Package N24A

DC Electrical Characteristics (Note 3)

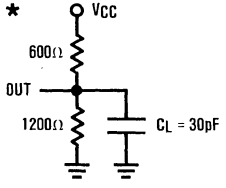
Sym	Parameter	Conditions	DM77LS181			DM87LS181			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V			-150			-100	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 5.5V			40			50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 8mA			0.50			0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = -18mA			-1.2			-1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open			100			100	mA
TRI-STATE® Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	-10		-70	-10		-85	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.5 to 5.5V Chip Disabled			+50 -50			+40 -40	μA μA
V_{OH}	Output Voltage High	I_{OH} = -1.0mA I_{OH} = 1.6mA	2.4	3.2		2.4	3.2		V V

AC Electrical Characteristics (With Specified Load* and Operating Conditions)

Sym	Parameter	JEDEC Symbol	DM77LS181			DM87LS181			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	Address Access Time	TAVQV			120			100	ns
TEA	Enable Access Time	TEVQV			70			50	ns
TER	Enable Recovery Time	TEXQX			70			50	ns
TZX	Output Enable Time	TEVQX			70			50	ns
TXZ	Output Disable Time	TEXQZ			70			50	ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.



National Semiconductor

DM77/87SR181
(1024 × 8) 8k-Bit Registered TTL PROM

General Description

The DM77/87SR181 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on chip. This devices is organized as 1024-words by 8-bits and is available in the tri-state output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR181 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable ($\overline{GS}$) is high before the rising edge of the clock, or if the asynchronous chip enable ($\overline{G}$) is held high. The outputs are enabled when $\overline{GS}$ is brought low before the rising edge of the clock and $\overline{G}$ is held low. The $\overline{GS}$ flip-flop is designed to power up to the "OFF" state with the application of V_{CC}.

Data is read from the PROM by first applying an address to inputs A0-A9. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

TRI-STATE® is a registered trademark of National Semiconductor Corp.
TRI-SAFE™ is a trademark of National Semiconductor Corp.

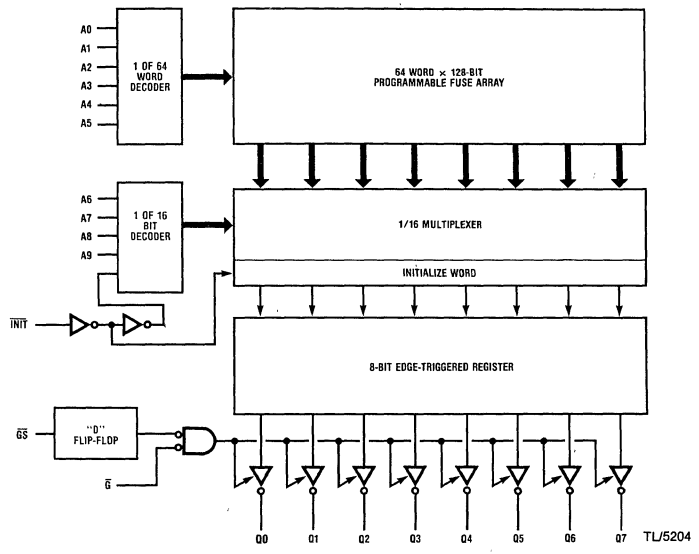
The DM77SR181 also features an initialize function $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a low on $\overline{INIT}$. The initialize function is synchronous and is loaded into the output register on the next rising edge of the clock. The unprogrammed state of the $\overline{INIT}$ is all lows.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- Programmable register INITIALIZE
- 24-pin, 300 mil package
- 40ns address setup and 20ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE® outputs
- Low voltage TRI-SAFE™ programming
- All parameters guaranteed over temperature

Block Diagram



TL/5204

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77SR181			DM87SR181			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}	Input Load Current	V_{CC} = Max., V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max., V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max., V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = 16mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max., V_{CEX} = 2.4V			50			50	μA
V_C	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max., Inputs Grounded All Outputs Open		115	175		115	175	mA
	TRI-STATE Parameters								
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max. (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max., V_O = 0.45 to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0mA	2.4	3.2					V
		I_{OH} = −6.5mA				2.4	3.2		V

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.
Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics

Symbol	Parameter	Conditions	DM77SR181			DM87SR181			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
$t_{S(A)}$	Address to CLK (High) Setup Time	C_L = 30pF	50	20		40	20		ns
$t_{H(A)}$	Address to CLK (High) Hold Time		0	−5		0	−5		ns
t_S(INIT)	INIT to CLK (High) Setup Time		35	20		30	20		ns
t_H(INIT)	INIT to CLK (High) Hold Time		0	−5		0	−5		ns
$t_{PHL(CLK)}$	Delay from CLK (High) to Output (High or Low)			15	30		15	20	ns
$t_{WH(CLK)}$ $t_{WL(CLK)}$	CLK Width (High or Low)		25	13		20	13		ns
$t_{S(GS)}$	$\overline{GS}$ to CLK (High) Setup Time		15	0		15	0		ns
$t_{H(GS)}$	$\overline{GS}$ to CLK (High) Hold Time		5	0		5	0		ns
$t_{PZL(CLK)}$	Delay from CLK (High) to Active Output (High or Low)	C_L = 30pF		20	30		20	25	ns
$t_{PZH(CLK)}$				20	30		20	25	ns
$t_{PZL(G)}$	Delay from $\overline{G}$ (Low) to Active Output (High or Low)			15	30		15	25	ns
$t_{PZH(G)}$				15	30		15	25	ns
$t_{PLZ(CLK)}$	Delay from CLK (High) to Inactive Output (TRI-STATE)	C_L = 5pF (Note 1)		20	30		20	25	ns
$t_{PHZ(CLK)}$				20	30		20	25	ns
$t_{PLZ(G)}$	Delay from $\overline{G}$ (High) to Inactive Output (TRI-STATE)			15	30		15	25	ns
$t_{PHZ(G)}$				15	30		15	25	ns

Note: All typical values are for V_{CC} = 5V, T_A = 25°C.

National Semiconductor

DM77/87S184, DM77/87S185, DM77/87S185A, DM77/87S185B (2048 × 4) 8192-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 2048 words by 4 bits configuration. A memory enable input is provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

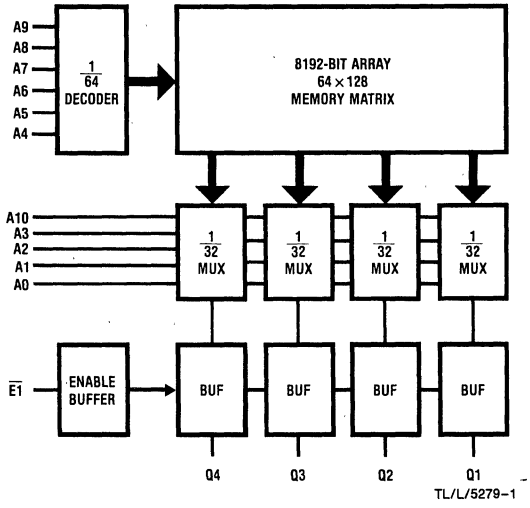
- Advanced titanium-tungsten (Ti-W) fuses
- Schottky-clamped for high speed
  - Address access—35 ns max (B Version)
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

	Military	Commercial	Open-Collector	TRI-STATE	Package
DM87S184		X	X		N,J
DM87S185		X		X	N,J
DM77S184	X		X		J
DM77S185	X			X	J

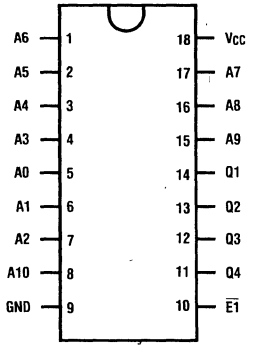
TRI-STATE® is a registered trademark of National Semiconductor Corp.

TRI-SAFE™ and STARPLEX™ are trademarks of National Semiconductor Corp.

Block and Connection Diagram



TL/L/5279–1



TOP VIEW

TL/L/5279–2

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77S184/185			DM87S184/185			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
	(Open-Collector Only)	V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		100	140		100	140	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current :	V_O = 0V, V_{CC} = Max (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol	Parameters	DM77S184/185			DM87S184/185			Units
			Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	Address Access Time		40	70		40	55	ns
TEA	TEVQV	Enable Access Time		15	30		15	25	ns
TER	TEXQX	Enable Recovery Time		15	30		15	25	ns
TZX	TEVQX	Output Enable Time		15	30		15	25	ns
TXZ	TEXQZ	Output Disable Time		15	30		15	25	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	JEDEC Symbol		Parameters	DM77S185A/B			DM87S185A/B			Units
				Min	Typ	Max	Min	Typ	Max	
TAA	TAVQV	185A	Address Access Time		30	60		30	45	ns
		185B			25	50		25	35	ns
TEA	TEVQV		Enable Access Time		15	30		15	25	ns
TER	TEXQX		Enable Recovery Time		15	30		15	25	ns
TZX	TEVQX		Output Enable Time		15	30		15	25	ns
TXZ	TEXQZ		Output Disable Time		15	30		15	25	ns

Note 3: These limits apply over the entire operating range unless otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

DM77/87S190, DM77/87S191; DM77/87S290, DM77/87S291; DM77/87S190A, DM77/87S191A; DM77/87S290A, DM77/87S291A; DM77/87S190B, DM77/87S191B; DM77/87S290B, DM77/87S291B (2048 × 8) 16,384-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 2048 words by 8 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 8 outputs go to the "OFF" or high impedance state. The memories are available in both open-collector and TRI-STATE® versions.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

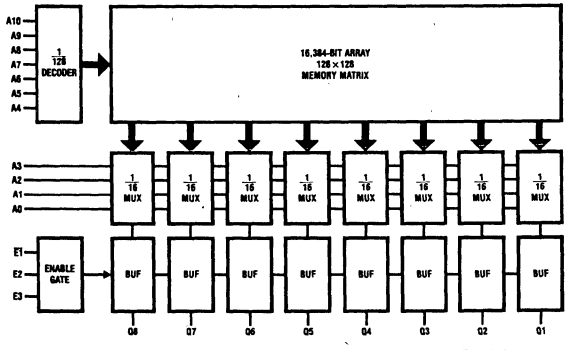
Features

- Advanced tungsten (W) fuses
- Schottky-clamped for high speed
  - Address access—35 ns max (B version)
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

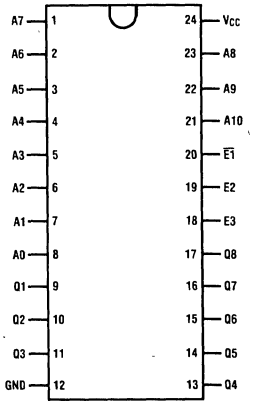
	Military	Commercial	Open-Collector	TRI-STATE	Package	24-Pin Standard	24-Pin Thin-Dip
DM87S190		X	X		N,J	X	
DM87S191		X		X	N,J	X	
DM77S190	X		X		J	X	
DM77S191	X			X	J	X	
DM87S290		X	X		N,J		X
DM87S291		X		X	N,J		X
DM77S290	X		X		J		X
DM77S291	X			X	J		X

TRI-STATE® is a registered trademark of National Semiconductor Corporation
TRI-SAFE™ and STARPLEX™ are trademarks of National Semiconductor Corporation

Block and Connection Diagrams



TL/L/5278–1



TOP VIEW
TL/L/5278–2

AC Electrical Characteristics (With Standard Load and Operating Conditions)

JEDEC Symbol		Sym	Parameter	DM77S190/191 DM77S290/291			DM87S190/191 DM87S290/291			Units
				Min	Typ	Max	Min	Typ	Max	
TAVQV	191A	t_{AA}	Address Access Time		35	60		35	45	ns
	191B				30	30		30	35	ns
TEVQV		t_{EA}	Enable Access Time		15	35		15	30	ns
TEXQX		t_{ER}	Enable Recovery Time		15	35		15	30	ns
TEVQX		t_{ZX}	Output Enable Time		15	35		15	30	ns
TEXQZ		t_{XZ}	Output Disable Time		15	35		15	30	ns

DC Electrical Characteristics (Note 3)

Symbols	Parameter	Condition	DM77S190/191 DM77S290/291			DM87S190/191 DM87S290/291			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{OZ}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Input Grounded All Outputs Open		120	175		120	175	mA
TRI-STATE Parameters									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V Chip Disabled	−50		50	−50		50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = −6.5 mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

JEDEC Symbol		Sym	Parameter	DM77S191A/B DM77S291A/B			DM87S191A/B DM87S291A/B			Units
				Min	Typ	Max	Min	Typ	Max	
TAVQV	191A/291A	t_{AA}	Address Access Time		30	60		30	45	ns
	191B/291B				30	50		30	35	ns
TEVQV		t_{EA}	Enable Access Time		15	35		15	25	ns
TEXQX		t_{ER}	Enable Recovery Time		15	35		15	25	ns
TEVQX		t_{ZX}	Output Enable Time		15	35		15	25	ns
TEXQZ		t_{XZ}	Output Disable Time		15	35		15	25	ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

National Semiconductor

Bipolar PROMs
PRELIMINARY

DM77S195A/DM87S195A, DM77S195B/DM87S195B (4096 x 4) 16,384-Bit TTL PROM

General Description

These Schottky memories are organized in the popular 4096 words by 4 bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the 4 outputs go to the OFF or high impedance state. The memories are available in TRI-STATE® version only.

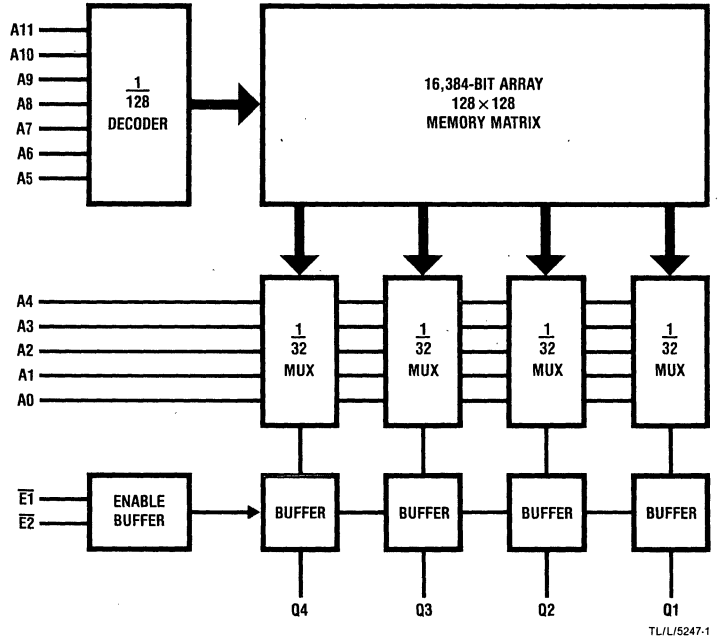
PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

Features

- Advanced tungsten (W) fuse technology
- Schottky-clamped for high speed
  - Address access—30 ns typ
  - Enable access—15 ns typ
  - Enable recovery—15 ns typ
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming

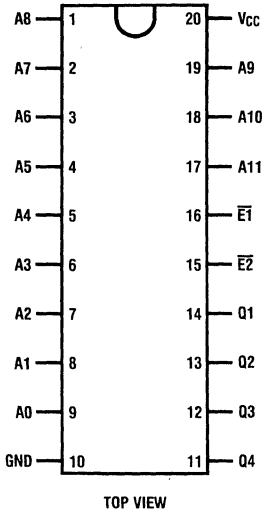
	Military	Commercial	TRI-STATE	Package
DM87S195A/B		X	X	N,J
DM77S195A/B	X		X	J

Block and Connection Diagrams



TL/L/5247-1

Dual-In-Line Package



TOP VIEW

TL/L/5247-2

TRI-STATE® is a registered trademark of National Semiconductor Corp.
TRI-SAFE™ is a trademark of National Semiconductor Corp.

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77S195A/B			DM87S195A/B			Units
			Min	Typ	Max	Min	Typ	Max	
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0V, V_{IN} = 2.0V T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1 MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, Inputs Grounded All Outputs Open			170			170	mA
TRI-STATE PARAMETERS									
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45V to 2.4V			+50			+50	μA
		Chip Disabled			−50			−50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0 mA	2.4	3.2					V
		I_{OH} = 6.5 mA				2.4	3.2		V

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.

Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

AC Electrical Characteristics (with standard load and operating conditions)

Symbol		Parameter		DM77S195A/195B			DM87S195A/195B			Units
Alternate	JEDEC Standard			Min	Typ	Max	Min	Typ	Max	
t_{AA}	TAVQV	Address Access Time	195A		30	60		30	45	ns
			195B		30	50		25	35	ns
t_{EA}	TEVQV	Enable Access Time			15	30		15	25	ns
t_{ER}	TEXQX	Enable Recovery Time			15	30		15	25	ns
t_{ZX}	TEVQX	Output Enable Time			15	30		15	25	ns
t_{XZ}	TEXQZ	Output Disable Time			15	30		15	25	ns

National Semiconductor

Bipolar PROMs
PRELIMINARY

DM77/87S321, DM77/87S421; DM77/87S321A, DM77/87S421A (4096 x 8) 32,768-Bit TTL PROMs

General Description

These Schottky memories are organized in the popular 4,096 words by 8-bits configuration. Memory enable inputs are provided to control the output states. When the device is enabled, the outputs represent the contents of the selected word. When disabled, the eight outputs go to the "OFF" or high impedance state.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions.

The DM77/87S321 and DM77/87S421 program the same as all other nonregistered PROMs from National.

Features

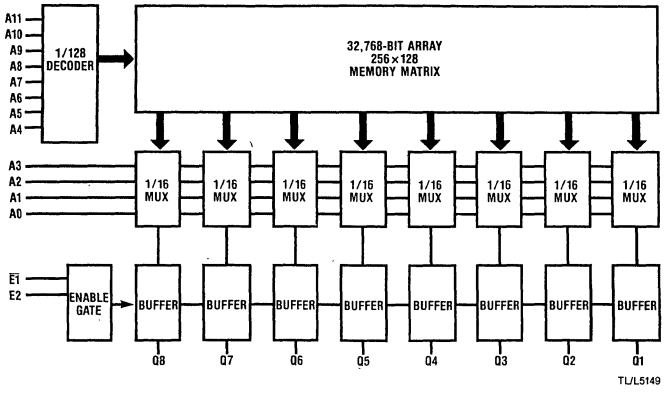
- Advanced fuse technology
- Schottky-clamped for high speed
  - Address access—35 ns typ.
  - Enable access—20ns typ.
  - Enable recovery—20ns typ.
- PNP inputs for reduced input loading
- All DC and AC parameters guaranteed over temperature
- Low voltage TRI-SAFE™ programming
- Generic programming.

	Military	Commercial	TRI-STATE®	Package
DM87S321, A		X	X	N,J
DM77S321, A	X		X	J
DM87S421, A		X	X	N,J*
DM77S421, A	X		X	J*

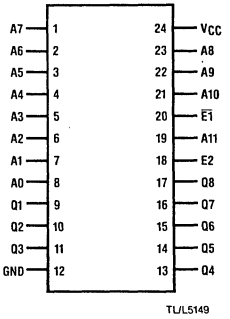
*Thin-Dip (0.3") package

TRI-STATE® is a registered trademark of National Semiconductor Corp.
TRI-SAFE™ is a trademark of National Semiconductor Corp.

Block and Connection Diagrams



TL/L5149



TL/L5149

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	DM77S321/421			DM87S321/421			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}	Input Load Current	V_{CC} = Max., V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current	V_{CC} = Max., V_{IN} = 2.7V			25			25	μA
		V_{CC} = Max., V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min., I_{OL} = 12mA		0.35	0.50		0.35	0.45	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min., I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	V
C_I	Input Capacitance	V_{CC} = 5.0, V_{IN} = 2.0V T_A = 25°C, 1MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5.0V, V_O = 2.0V T_A = 25°C, 1MHz, Outputs Off		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max., All Outputs Open		135	185		135	185	mA
	TRI-STATE Parameters								
I_{OS}	Short Circuit Output Current	V_O = 0V, V_{CC} = Max. (Note 4)	−20		−70	−20		−70	mA
I_{OZ}	Output Leakage (TRI-STATE)	V_{CC} = Max., V_O = 0.45 to 2.4V Chip Disabled	−50		+50	−50		+50	μA
V_{OH}	Output Voltage High	I_{OH} = −2.0mA	2.4	3.2					V
		I_{OH} = −6.5mA				2.4	3.2		V

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	Parameter	JEDEC Symbol	DM77S321/421			DM87S321/421			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
T_{AA}	Address Access Time	TAVQV		40	65		40	55	ns
T_{EA}	Enable Access Time	TEVQV		20	35		20	30	ns
T_{ER}	Enable Recovery Time	TEXQX		20	35		20	30	ns
T_{ZX}	Output Enable Time	TEVQX		20	35		20	30	ns
T_{XZ}	Output Disable Time	TEXQZ		20	35		20	30	ns

AC Electrical Characteristics (With Standard Load and Operating Conditions)

Symbol	Parameter	JEDEC Symbol	DM77S321A/421A			DM87S321A/421A			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
T_{AA}	Address Access Time	TAVQV		35			35		ns
T_{EA}	Enable Access Time	TEVQV		20			20		ns
T_{ER}	Enable Recovery Time	TEXQX		20			20		ns
T_{ZX}	Output Enable Time	TEVQX		20			20		ns
T_{XZ}	Output Disable Time	TEXQZ		20			20		ns

Note 3: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5.0V and T_A = 25°C.
Note 4: During I_{OS} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Non-Registered PROM Programming Procedure

National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical "0") for all addresses. To generate high (logical "1") levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed:

1. Programming should be attempted only at ambient temperatures between 15 and 30 degrees Celsius.

2. Address and enable inputs must be driven with TTL logic levels during programming and verification.

3. Programming will occur at the selected address when V_{CC} is at 10.5 volts, and at the selected bit location when the output pin, representing that bit, is at 10.5 volts, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:

   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to one or more "active low" chip enable inputs.

   b) Increase V_{CC} from nominal to 10.5 volts (plus or minus 0.5V) with a slew rate between 1.0 and 10.0V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750mA at 11.0 volts.

   c) Select the output where a logical high is desired by raising that output voltage to 10.5 volts (plus or minus 0.5V). Limit the slew rate from 1.0 to 10.0V/μs. This voltage change may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20kΩ minimum (Remember that the outputs of the device are disabled at this time).

   d) Enable the device by taking the chip enable(s) to a low level. This is done with a pulse of 10μs. The 10μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.

   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0 volts (plus or minus 0.2V). Verification at a V_{CC} level of 4.0 volts will guarantee proper output states over the V_{CC} and temperature range of the programmed part. The device must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.

   f) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.

   g) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Note: Since only an enabled device is programmed, it is possible to program these parts at the board level if all programming parameters are complied with.

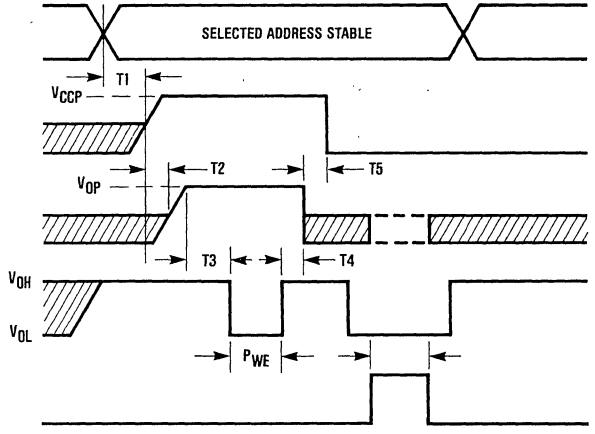
Programming Parameters Do not test or you may program the device

Sym	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} During Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Non-Registered PROM

T1 = 100ns min.
T2 = 5μs min. T2 may be > 0 if V_{CCP} rises at the same rate or faster than (V_{OP})
T3 = 100ns min.
T4 = 100ns min.
T5 = 100ns min.

P_{WE} is repeated for 5 additional pulses after verification of V_{OH} indicates a bit has been programmed.



Registered PROM Programming Procedure

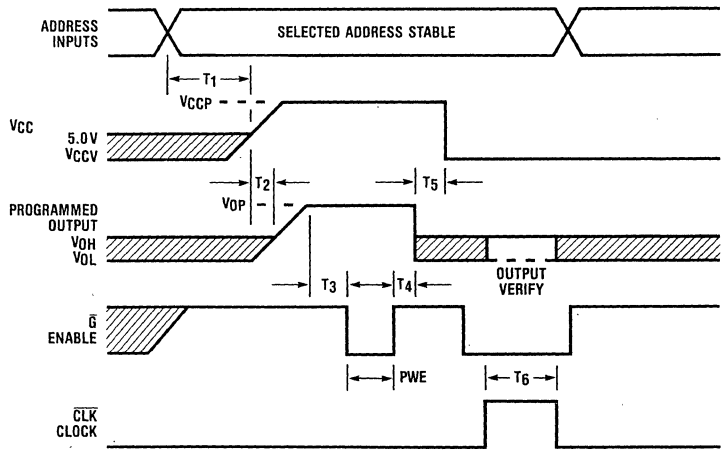
National Schottky PROMs are shipped from the factory with all fuses intact. As a result, the outputs will be low (logical '0') for all addresses. To generate high (logical '1') levels at the outputs, the device must be programmed. Information regarding commercially available programming equipment may be obtained from National. If it is desired to build your own programmer, the following conditions must be observed.

1. Programming should be attempted only at ambient temperatures between 15°C and 30°C.
2. Address and Enable inputs must be driven with TTL logic levels during programming and verification.
3. Programming will occur at the selected address when V_{CC} is at 10.5V, and at the selected bit location when the output pin, representing that bit, is at 10.5V, and the device is subsequently enabled. To achieve these conditions in the appropriate sequence, the following procedure must be followed:
   a) Select the desired word by applying high or low levels to the appropriate address inputs. Disable the device by applying a high level to asynchronous chip Enable input $\overline{G}$. $\overline{GS}$ is held low during the entire programming time.
   b) Increase V_{CC} from nominal to 10.5V (±0.5V) with a slew rate between 1.0 and 10V/μs. Since V_{CC} is the source of the current required to program the fuse as well as the I_{CC} for the device at the programming voltage, it must be capable of supplying 750mA at 11V.
   c) Select the output where a logical high is desired by raising that output voltage to 10.5V (±0.5V). Limit the slew rate from 1.0 to 10V/μs. This voltage change may occur simultaneously with the increase in V_{CC}, but must not precede it. It is critical that only one output at a time be programmed since the internal circuits can only supply programming current to one bit at a time. Outputs not being programmed must be left open or connected to a high impedance source of 20kΩ minimum. (Remember that the outputs of the device are disabled at this time.)
   d) Enable the device by taking the chip enable ($\overline{G}$) to a low level. This is done with a pulse of 10μs. The 10μs duration refers to the time that the circuit (device) is enabled. Normal input levels are used and rise and fall times are not critical.
   e) Verify that the bit has been programmed by first removing the programming voltage from the output and then reducing V_{CC} to 4.0V (±0.2V). Verification at a V_{CC} level of 4.0V will guarantee proper output states over the V_{CC} and temperature range of the programmed part. Each data verification must be preceded by a positive going (low to high) clock edge to load the data from the array into the output register. The device must be enabled to sense the state of the outputs. During verification, the loading of the output must be within specified I_{OL} and I_{OH} limits. Steps b, c, and d must be repeated up to 10 times or until verification that the bit has been programmed.
   f) The initialize word is programmed by setting $\overline{INIT}$ input to a logic low and programming the initialize word output by output in the same manner as any other address. This can be accomplished by inverting the A9 address input from the PROM programmer and applying it to the $\overline{INIT}$ input. Using this method, the initialize word will program at address 512.
   g) Following verification, apply five additional programming pulses to the bit being programmed. The programming procedure is now complete for the selected bit.
   h) Repeat steps a through f for each bit to be programmed to a high level. If the procedure is performed on an automatic programmer, the duty cycle of V_{CC} at the programming voltage must be limited to a maximum of 25%. This is necessary to minimize device junction temperatures. After all selected bits are programmed, the entire contents of the memory should be verified.

Programming Parameters Do not test or you may program the device

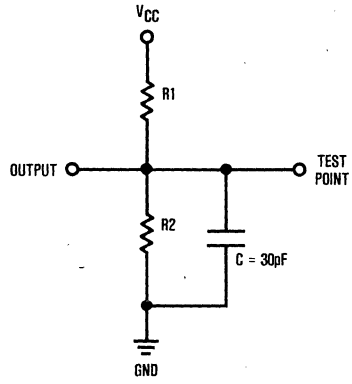
Sym	Parameters	Conditions	Min	Recommended Value	Max	Units
V_{CCP}	Required V_{CC} for Programming		10.0	10.5	11.0	V
I_{CCP}	I_{CC} During Programming	V_{CC} = 11V			750	mA
V_{OP}	Required Output Voltage for Programming		10.0	10.5	11.0	V
I_{OP}	Output Current while Programming	V_{OUT} = 11V			20	mA
I_{RR}	Rate of Voltage Change of V_{CC} or Output		1.0		10.0	V/μs
P_{WE}	Programming Pulse Width (Enabled)		9	10	11	μs
V_{CCV}	Required V_{CC} for Verification		3.8	4.0	4.2	V
M_{DC}	Maximum Duty Cycle for V_{CC} at V_{CCP}			25	25	%

Programming Waveforms Registered PROM



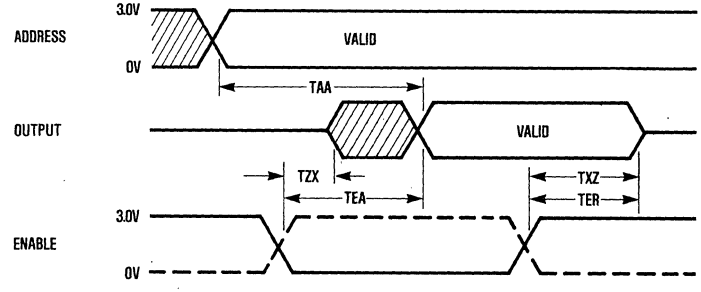
T_1 = 100ns MIN.
T_2 = 5μs MIN. (T_2 MAY BE > 0 IF V_{CCP} RISES AT THE SAME RATE OR FASTER THAN V_{OP}.)
T_3 = 100ns MIN.
T_4 = 100ns MIN.
T_5 = 100ns MIN.
T_6 = 50ns MIN.

Standard Test Load

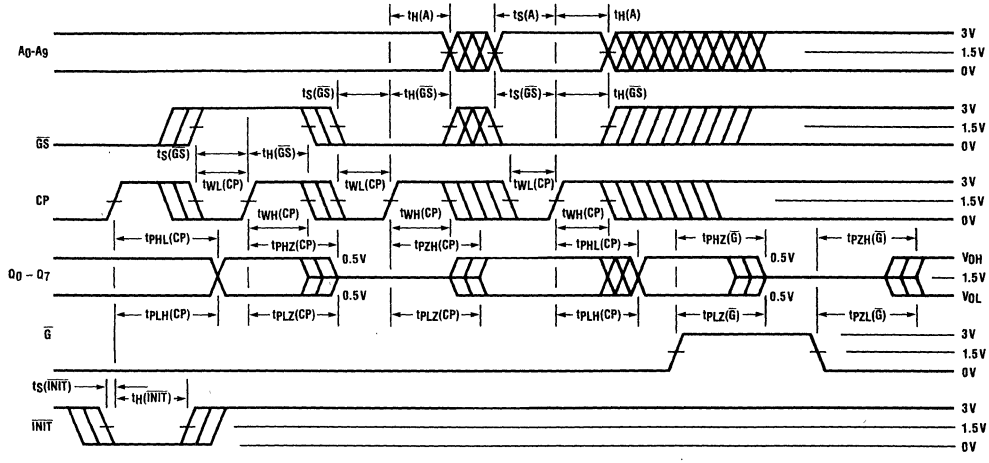


* Device input waveform characteristics are; Repetition rate = 1MHz Source impedance = 50Ω Rise and Fall times = 2.5ns max. (1.0 to 2.0 volt levels)
* TAA is measured with stable enable inputs.
* TEA and TER are measured from the 1.5 volt level on inputs and outputs with all address and enable inputs stable at applicable levels.
* For I_{OL} = 16mA, R1 = 300Ω and R2 = 600Ω for I_{OL} = 12mA, R1 = 400Ω and R2 = 800Ω.
* "C" includes scope and jig capacitance.

Switching Time Waveforms Non-Registered PROM



Switching Waveforms Registered PROM



Key To Timing Diagram

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY		DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L		DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

Approved Programmers for NSC PROMs

MANUFACTURER	SYSTEM #
DATA I/O	5/17/19/29A
PRO-LOG	M910, M980
KONTRON	MPP80S
STAG	PPX
AIM	RP400
DIGELEC	UP803
STARPLEX™	

Quality Enhancement Programs For Bipolar Memory

A+ PROGRAM*			B+ PROGRAM		
Test	**Condition**	**Guaranteed LOT AQL 5**	**Test**	**Condition**	**Guaranteed LOT AQL 5**
D.C. Parametric And Functionality	25°C	0.05	D.C. Parametric And Functionality	25°C	0.05
	Each Temperature Extreme	0.05		Each Temperature Extreme	0.05
A.C. Parametric	25°C	0.4	A.C. Parametric	25°C	0.4
Mechanical	Critical	0.01	Mechanical	Critical	0.01
	Major	0.28		Major	0.28
Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4	Seal Tests Hermetic	Fine Leak (5×10^{-8})	0.4
	Gross	0.4		Gross	0.4

*Includes 160 hours of burn-in at 125°C.

STARPLEX™ is a trademark of National Semiconductor Corp.

National Semiconductor

Bipolar PROMs

DM76S64/DM86S64 Bipolar Character Generator

General Description

The DM76S64/DM86S64 is a 64-character bipolar character generator with serial output designed primarily for the CRT display marketplace, and packaged in a standard 16-pin DIP. The DM76S64/DM86S64 incorporates several CRT system level functions, as well as a 7 x 9 or 5 x 7 row scan character font. The DM76S64/DM86S64 performs the system functions of parallel to serial shifting, character address latching, character spacing and character line spacing. These system functions have required extra packages in the past.

Shifted characters can be generated by the on-chip subtractor.

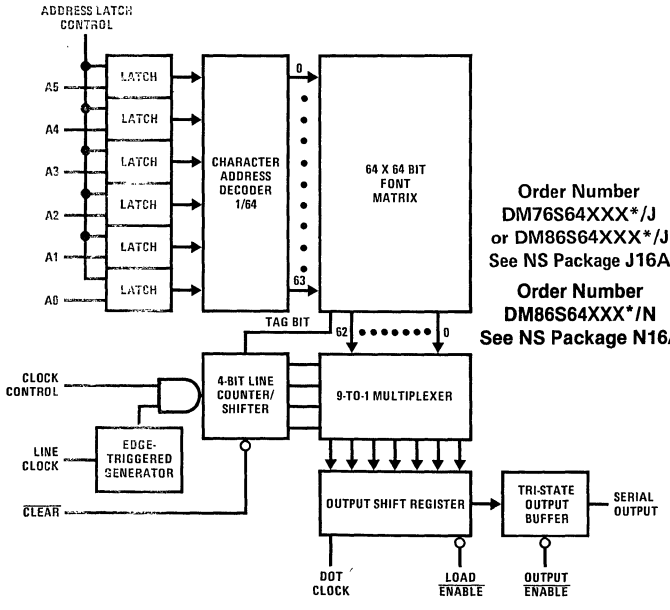
The $\overline{\text{clear}}$ input and the load $\overline{\text{enable}}$ input are active low. Load $\overline{\text{enable}}$ is synchronous with the dot clock. Both the line clock and the dot clock are positive edge-triggered. When the address latch control signal is high, the character addresses "fall through" the latch. And when the address latch control signal goes low, the character addresses are latched.

Features

- 64-character—row scan
- 5 x 7 or 7 x 9 font
- Custom fonts available with shift options
- Serial output
- 16-pin package
- 35 MHz typ clock rate
- On-chip input latches
- On-chip shift register
- On-chip dot blanking
- On-chip row blanking
- TRI-STATE® output

	7 x 9	5 x 7	FONT	PACKAGE
DM76S64BWF/DM86S64BWF	X		Upper Case Block Letters	N, J
DM76S64CAE/DM86S64CAE	X		Shifted Lower Case Block	N, J
DM76S64CAB/DM86S64CAB		X	Upper Case Block Letters	N, J
DM76S64CAH/DM86S64CAH		X	Shifted Lower Case Block	N, J
DM76S64CTA/DM86S64CTA	X		ASCII Character Set	N, J
DM76S64CTB/DM86S64CTB	X		ASCII Numerals and Control	N, J

Block Diagram

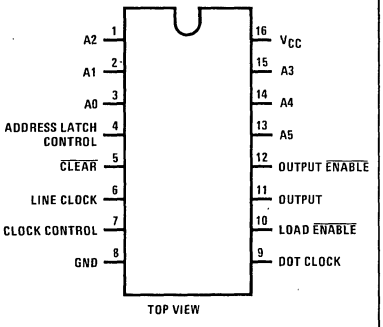


Order Number DM76S64XXX*/J or DM86S64XXX*/J
See NS Package J16A

Order Number DM86S64XXX*/N
See NS Package N16A

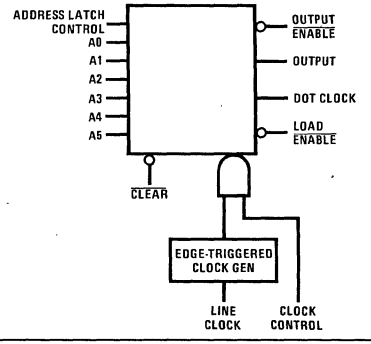
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



* alpha pattern designators

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Note 1)

Supply Voltage	−0.5V to +7V
Input Voltage	−1.5V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM76S64	4.5	5.5	V
DM86S64	4.75	5.25	V
Ambient Temperature (T_A)			
DM76S64	−55	+125	°C
DM86S64	0	+70	°C
Logical "0" Voltage	0	0.8	V
Logical "1" Voltage	2.0	5.5	V

DC Electrical Characteristics (Note 2)

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V			−800	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
I_I	Input Leakage Current	V_{CC} = Max, V_{IN} = 5.5V			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{IL}	Low Level Input Voltage	V_{CC} = Min			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = Min	2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA		−0.8	−1.5	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, Output Open		80	140	mA
TRI-STATE PARAMETERS						
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max	−15		−70	mA
I_{HZ}	Output Leakage	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±40	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2		V

AC Electrical Characteristics (Note 2)

SYM	PARAMETER	CONDITIONS	DM76S64			DM86S64			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Access Time								
T_{DO}	Dot Clock to Output			25	50		25	40	ns
T_{EA}	Output Enable			10	35		10	30	ns
T_{ER}	Output Disable			13	35		13	30	ns
	Set-Up Time								
T_{S1}	Load to Dot Clock		25	7		20	7		ns
T_{S2}	Address to Load	See	335	54		280	54		ns
T_{S3}	Clear to Load	Switching	335	14		280	14		ns
T_{S4}	Control to Line Clock	Time	50	−10		40	−10		ns
T_{S5}	Line Clock to Load	Waveforms	1140	156		950	156		ns
T_{S6}	Address to Address Latch		50	6		40	6		ns
	Hold Time								
T_{H1}	Load from Dot Clock		5	−6		0	−6		ns
T_{H2}	Address from Load		0	−14		0	−14		ns
T_{H3}	Control from Line Clock		120	23		100	23		ns
T_{H4}	Address from Address Latch		50	3		40	3		ns

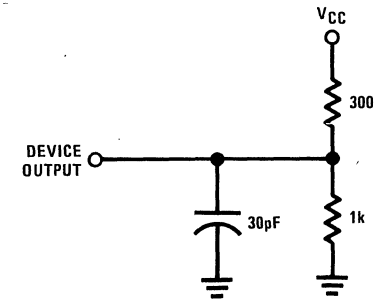
AC Electrical Characteristics (Continued) (Note 2)

SYM	PARAMETER	CONDITIONS	DM76S64			DM86S64			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
	Pulse Width								
T_{W1}	Line Clock		50	12		40	12		ns
T_{W2}	Clear		50	6		40	6		ns
T_{W3}	Dot Clock		25	12		20	12		ns
T_{W4}	Load		40	8		30	8		ns
T_{W5}	Address Latch		50	22		40	22		ns
f_{MAX}	Clock Frequency		18	35		22	35		MHz

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

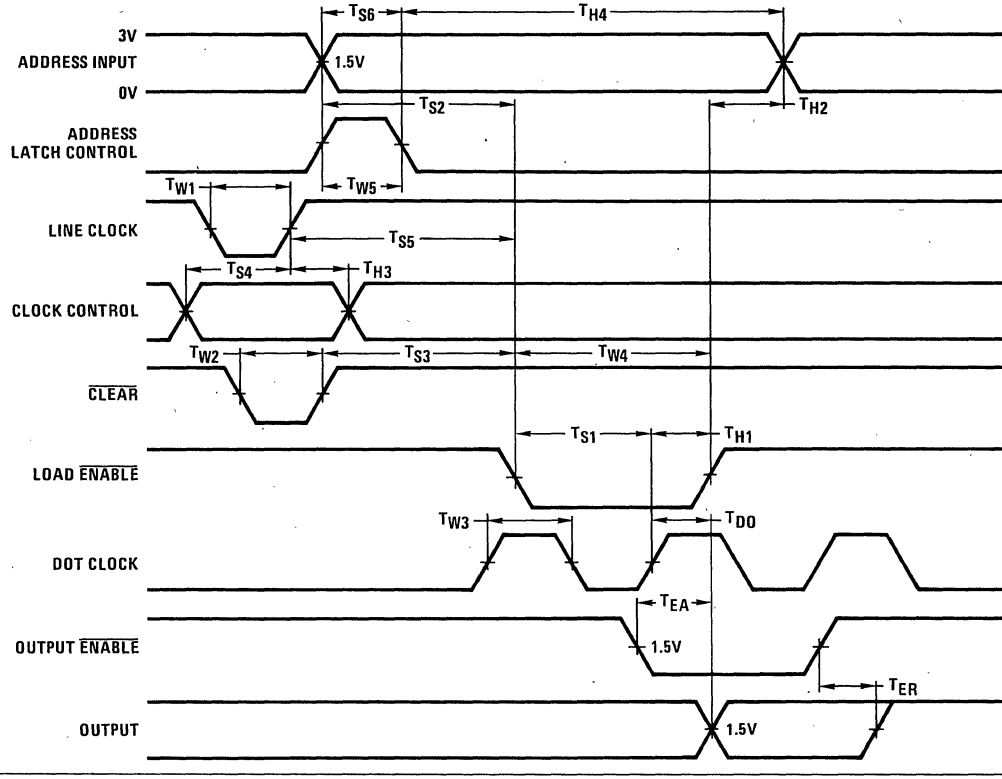
Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Standard Test Load



- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50 Ω, $t_r < 5$ ns and $t_f < 5$ ns (between 1.0V and 2.0V).
- T_{DO} is measured with output enable at a steady low level.

Switching Time Waveforms



Truth Tables

A) ADDRESS LATCH

ADDRESS LATCH CONTROL	FUNCTION PERFORMED
0	Latched
1	Fall Through

B) OUTPUT

OUTPUT $\overline{\text{ENABLE}}$	STATE OF THE OUTPUT
1	Output Hi-Z
0	Data Out

C) 4-BIT LINE COUNTER

CLOCK CONTROL	LINE CLOCK	$\overline{\text{CLEAR}}$	LINE COUNTER
H	⌐	H	Increment line counter
X	X	L	Asynchronous clear resets counter
L	X	H	Clock inhibited
H	⌐	H	No change on high-to-low clock edge

X = Don't care

Definitions

A0–A5: Character address. A 6-bit code which selects 1 of the 64 characters in the font.

$\overline{\text{Clear}}$: Active low clear for mod 16 row counter, (can be used to truncate mod 16 counter).

Line Clock: Clock that advances the line counter. Advances counter on the low-to-high transition.

Clock Control: Enables line clock when high and disables line clock when low.

Load $\overline{\text{Enable}}$: Active low load command which routes data from the character ROM to the "D" inputs of the 7-bit shift register.

Dot Clock: A low-to-high transition of the dot clock loads the shift register if load $\overline{\text{enable}}$ is low or shifts data if load $\overline{\text{enable}}$ is high.

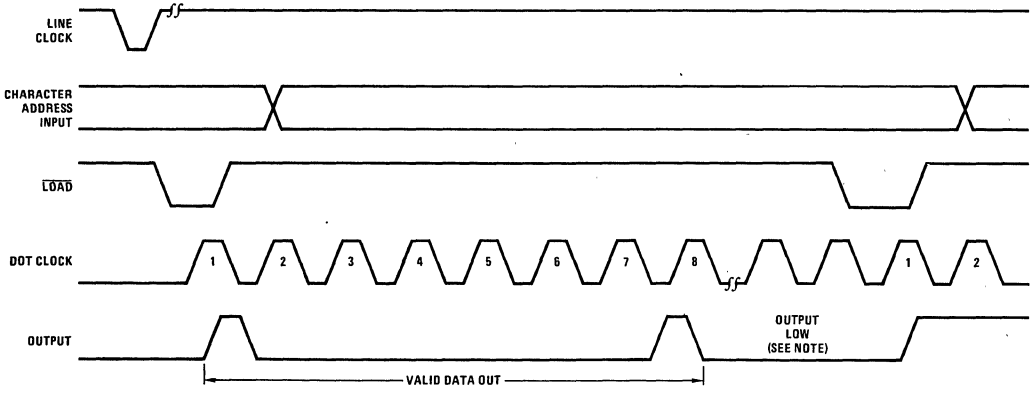
Output $\overline{\text{Enable}}$: An active low output enable. When high the output is in the Hi-Z state.

Output: A TTL TRI-STATE output buffer.

Functional Description

To select a character, a 6-bit binary word must be present at the address inputs A0—A5 when the address latch control is high. This address can be latched by bringing the address latch control signal low after a 40 ns set-up time. When the clear input receives a low pulse, the counter is reset to zero. The shift register can be loaded (T_{S2} ns) after the character is addressed. Data, representing 1 horizontal line of the addressed character, is available at the output when the load enable input is brought low. As shown in *Figure 1*, valid data arrives serially at the output. Dot clock pulses beyond that required to shift out 1 line of the character will add lows to the end of character. This provides a horizontal spacing between characters.

Figure 2 shows how the counter sequences through the rows of addressed lines with the application of clock pulses at the line clock input. Any additional line clocks beyond that required to display the character will put a vertical space between characters. This spacing can be truncated by bringing the clear input low. Detailed system application infomation is contained in application note AN-167 available from National.



Note. Output goes and stays low following the leading edge of the eighth Dot-Clock pulse until Load enable is enabled again and new parallel data is loaded into the shift register.

FIGURE 1. Character Cycle

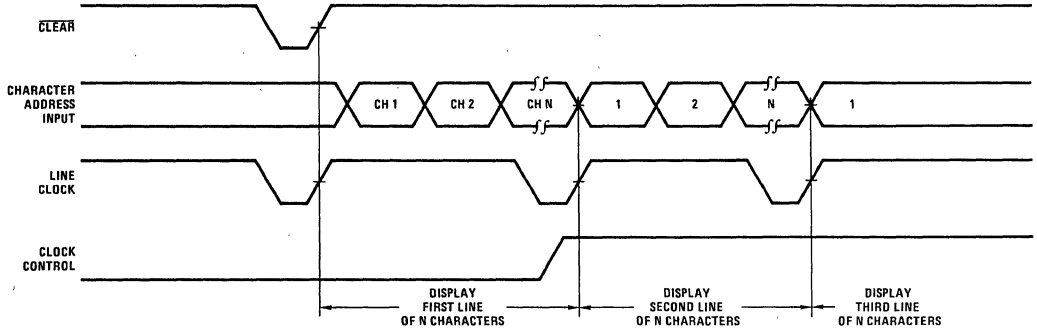


FIGURE 2. Line Cycle

Functional Description (Continued)

A two character display example is shown in *Figure 3* and a typical system timing waveform is shown in *Figure 4.*

A chip select input is provided for expansion of the character font. The various standard fonts are shown in *Figures 5, 6, 7, 8, 9 and 10.* Descending characters in the 5 x 7 fonts are shifted by virtue of their placement in the matrix. Descending characters in the 7 x 9 fonts are shifted (by the on-chip line shifter/counter) the number of lines indicated by the number in the upper left hand corner of the character drawings in the figures.

Character Cycle – ROM data corresponding to 1 line of characters is loaded into the shift register T_{S2} after the ROM is addressed. When load $\overline{\text{enable}}$ goes low, ROM data is allowed to be present at the D input of the shift register via the MUX. The first bit of the ROM data is transferred to the output at the next low-to-high transition of the dot clock. After load $\overline{\text{enable}}$ goes back high, the second to seventh clock pulses shift out the rest of the selected row of the addressed character. Additional clock pulses will shift out low data used for spacing.

Line Cycle – The line counter is a mod 16 counter. A low-to-high transition of the line clock advances the line counter to the next count. If, for any reason, the counts need to be truncated, a low signal at the $\overline{\text{clear}}$ input resets the counter to zero. The clock control may be used as a line clock disable. A high signal at the line clock control terminal enables the counter and a low signal disables the line clock.

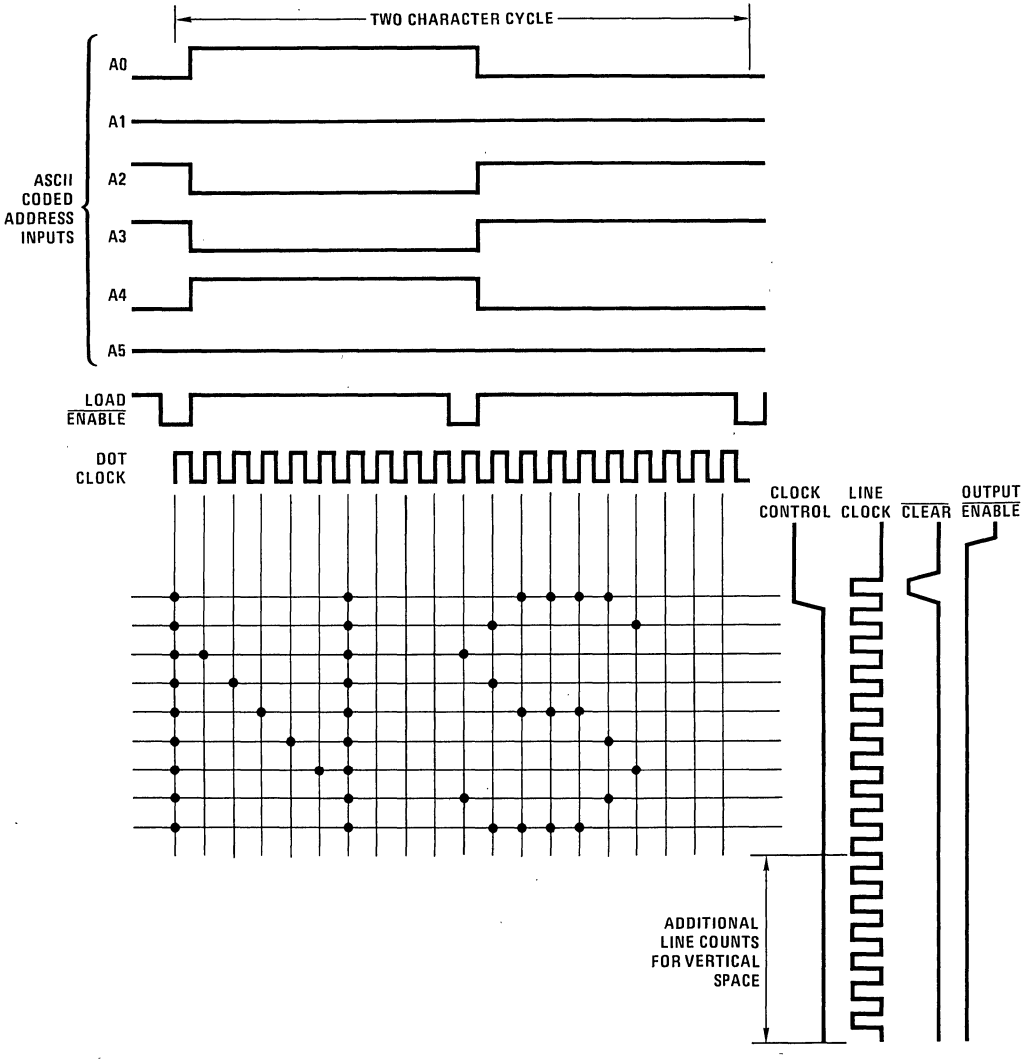
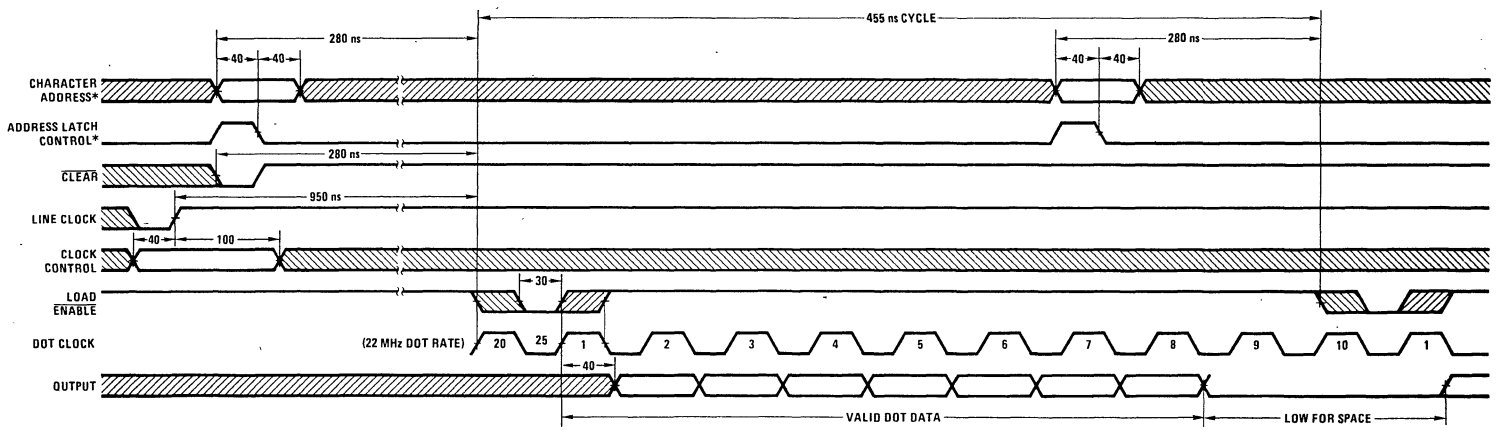


FIGURE 3. Example of Two Characters Display Timing



*Shown here for operation with dynamic memory. For static memory operation the address latch control would be tied high and the character addresses would be stable between each address change occurring 280 ns before the high-to-low transition of Load $\overline{\text{enable}}$.

FIGURE 4. Typical System Timing Waveform

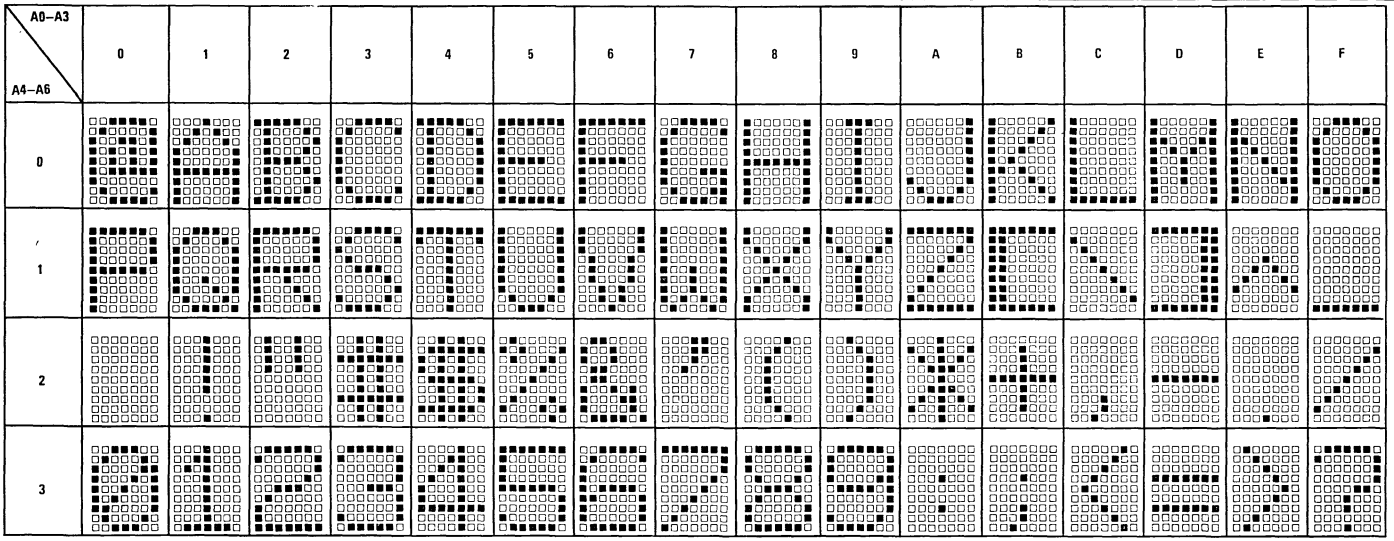


FIGURE 5. DM76S64BWF/DM86S64BWF

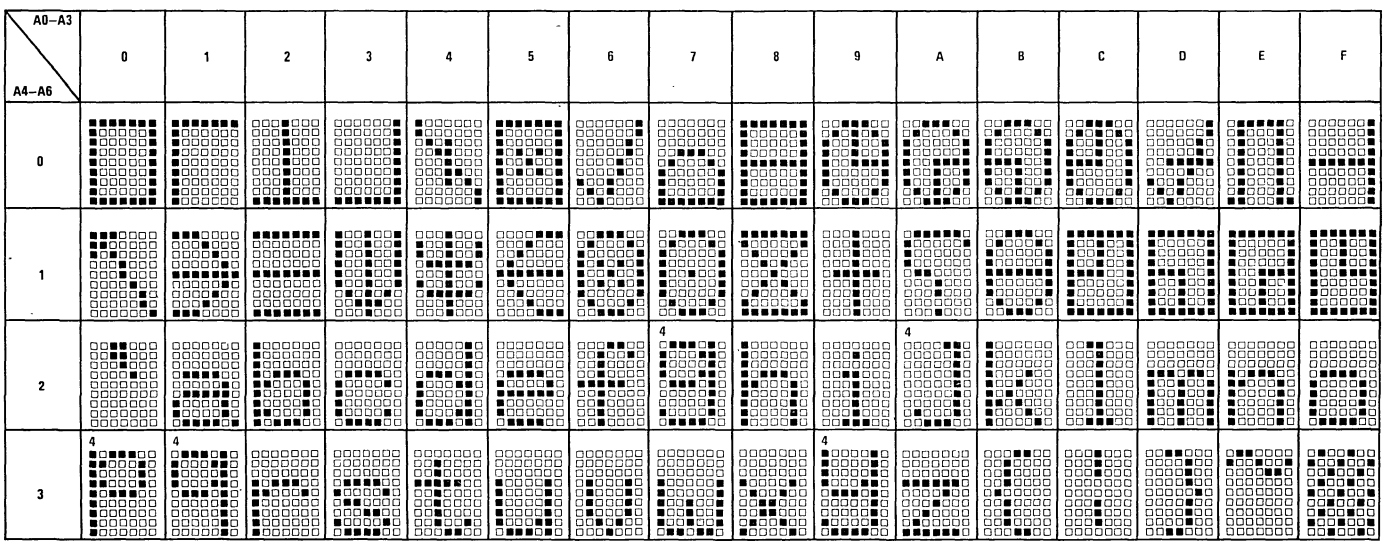


FIGURE 6. DM76S64CAE/DM86S64CAE

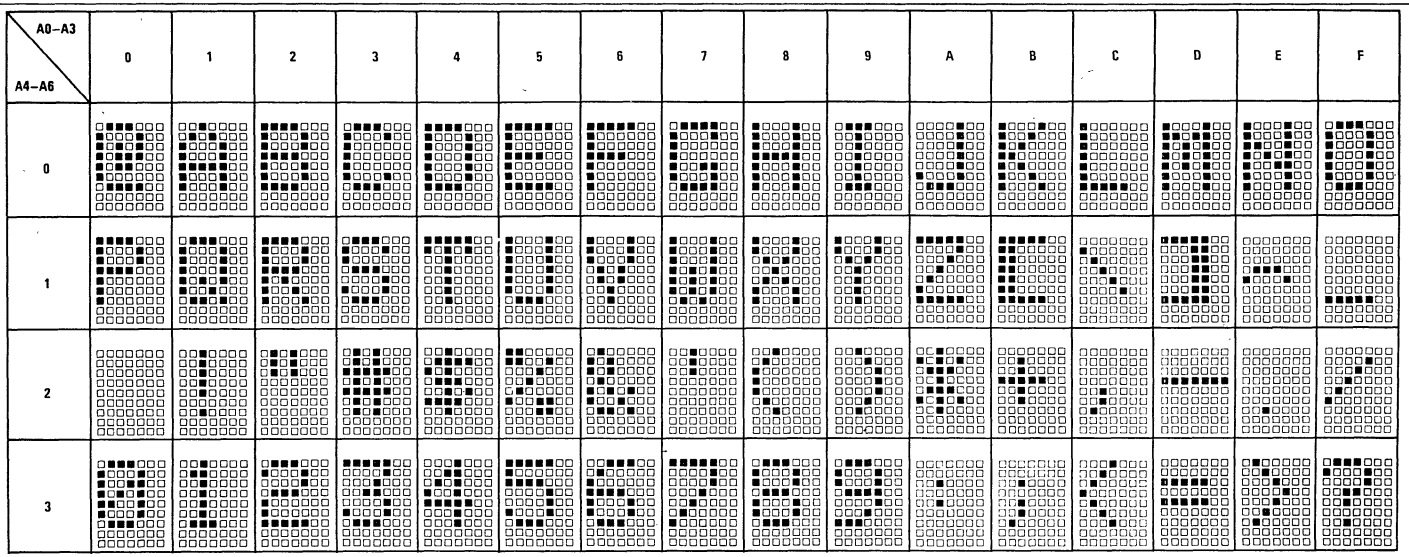


FIGURE 7. DM76S64CAB/DM86S64CAB

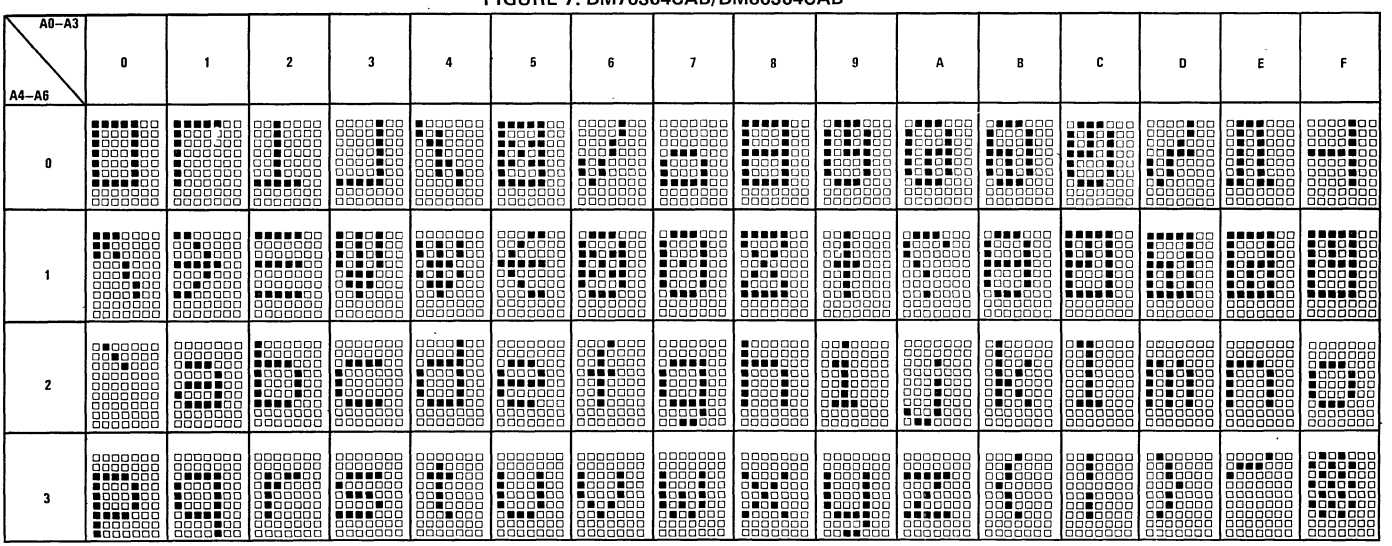


FIGURE 8. DM76S64CAH/DM86S64CAH

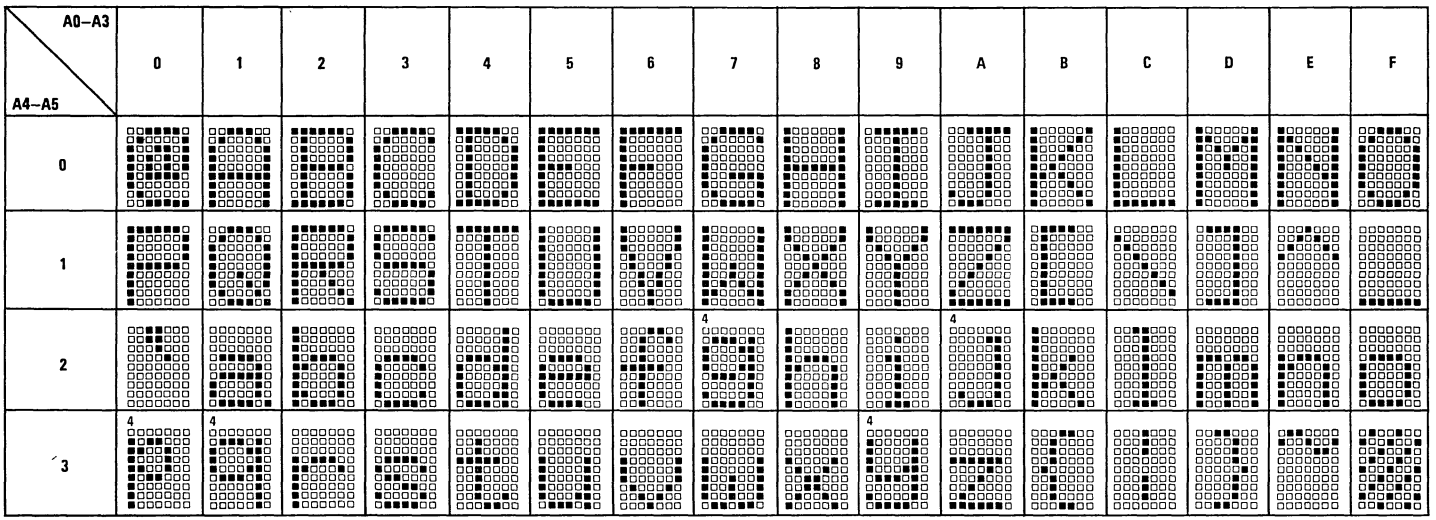


FIGURE 9. DM76S64CTA/DM86S64CTA

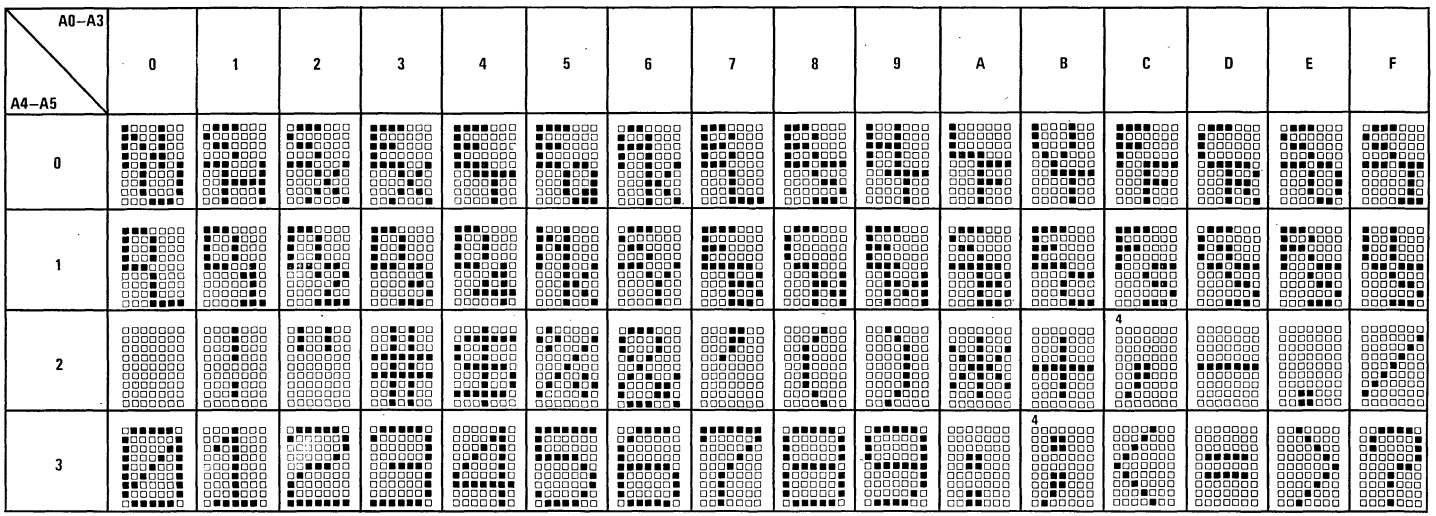


FIGURE 10. DM76S64CTB/DM86S64CTB

DM76S128/DM86S128 Bipolar Character Generator

General Description

The DM76S128/DM86S128 is a 128-character bipolar character generator with serial output designed primarily for the CRT display marketplace, and packaged in a standard 16-pin DIP. The DM76S128/DM86S128 incorporates several CRT system level functions, as well as a 7 x 9 or 5 x 7 row scan character font. The DM76S128/DM86S128 performs the system functions of parallel to serial shifting, character address latching, character spacing and character line spacing. These system functions have required extra packages in the past.

Shifted characters can be generated by the on-chip adder/subtracter.

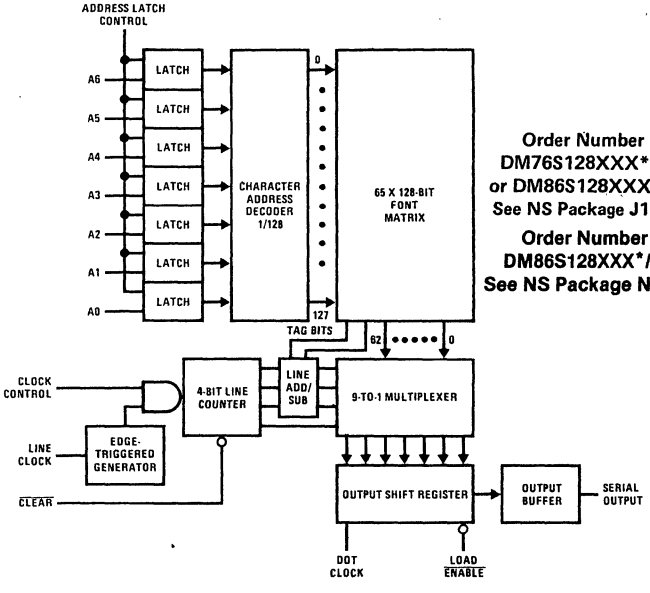
The $\overline{\text{clear}}$ input and the load $\overline{\text{enable}}$ input are active low. Load $\overline{\text{enable}}$ is synchronous with the dot clock. Both the line clock and the dot clock are positive edge-triggered. When the address latch control signal is high, the character addresses "fall through" the latch. And when the address latch control signal goes low, the character addresses are latched.

Features

- 128 character—row scan
- 5 x 7 or 7 x 9 font
- Custom fonts available with shift options
- Serial output
- 16-pin package
- 35 MHz typical clock rate
- On-chip input latches
- On-chip shift register
- On-chip dot blanking
- On-chip row blanking
- Low power—400 mW typical

	7 x 9	5 x 7	FONT	PACKAGE
DM76S128CNC/DM86S128CNC	X		Upper and Shifted Lower Case Block	N, J
DM76S128CND/DM86S128CND		X	Upper and Lower Case Block	N, J
DM76S128CQH/DM86S128CQH	X		ASCII CHARACTER SET	N, J
DM76S128CQJ/DM86S128CQJ		X	ASCII CHARACTER SET	N, J

Block Diagram

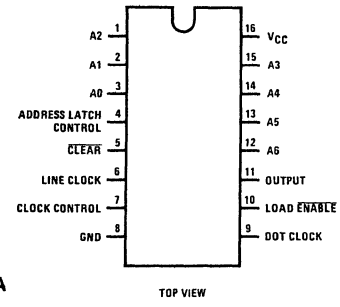


Order Number DM76S128XXX*/J or DM86S128XXX*/J
See NS Package J16A

Order Number DM86S128XXX*/N
See NS Package N16A

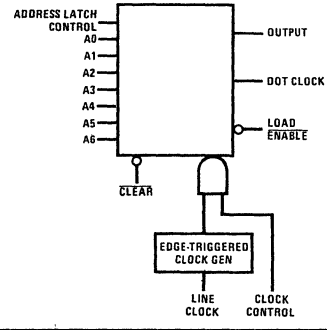
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



*alpha pattern designators

Absolute Maximum Ratings (Note 1)

Supply Voltage	−0.5V to +7V
Input Voltage	−1.5V to +5.5V
Output Voltage	−0.5V to +5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM76S128	4.5	5.5	V
DM86S128	4.75	5.25	V
Ambient Temperature (T_A)			
DM76S128	−55	+125	°C
DM86S128	0	+70	°C
Logical "0" Input Voltage (Low)	0	0.8	V
Logical "1" Input Voltage (High)	2.0	5.5	V

DC Electrical Characteristics (Note 2)

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input Load Current	V_{CC} = Max, V_{IN} = 0.45V			−800	μA
I_{IH}	Input Leakage Current	V_{CC} = Max, V_{IN} = 2.4V			40	μA
I_I	Input Leakage Current	V_{CC} = Max, V_{IN} = 5.5V			1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45	V
V_{OH}	Output Voltage High	I_{OH} = −2 mA	2.4	3.2		V
V_{IL}	Low Level Input Voltage	V_{CC} = Min			0.80	V
V_{IH}	High Level Input Voltage	V_{CC} = Min	2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA		−0.8	−1.5	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz		6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, Output Open		100	140	mA
I_{SC}	Output Short-Circuit Current	V_O = 0V, V_{CC} = Max	−15		−70	mA

AC Electrical Characteristics

DM76S128: T_A = −55°C to +125°C, V_{CC} = 4.5V to 5.5V. C_L = 50 pF.

DM86S128: T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V. C_L = 50 pF.

SYM	PARAMETER	DM76S128			DM86S128			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
	Access Time							
T_{DO}	Dot Clock to Output		25	50		25	40	ns
	Set Up Time							
T_{S1}	Load to Dot Clock	25	7		20	7		ns
T_{S2}	Address to Load	335	54		280	54		ns
T_{S3}	Clear to Load	335	14		280	14		ns
T_{S4}	Control to Line Clock	50	−10		40	−10		ns
T_{S5}	Line Clock to Load	1140	156		950	156		ns
T_{S6}	Address to Address Latch	50	6		40	6		ns
	Hold Time							
T_{H1}	Load from Dot Clock	5	−6		0	−6		ns
T_{H2}	Address from Load	0	−14		0	−14		ns
T_{H3}	Control from Line Clock	120	23		100	23		ns
T_{H4}	Address from Address Latch	50	3		40	3		ns

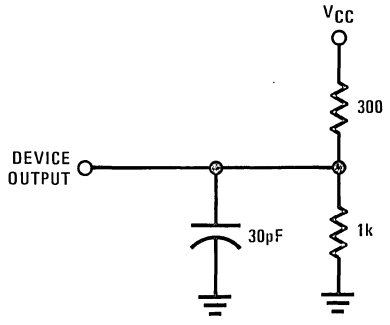
AC Electrical Characteristics (Continued) (With standard load) (Note 2)

SYM	PARAMETER	DM76S128			DM86S128			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
T_{W1}	Line Clock	50	12		40	12		ns
T_{W2}	Clear	50	6		40	6		ns
T_{W3}	Dot Clock	25	12		20	12		ns
T_{W4}	Load	40	8		30	8		ns
T_{W5}	Address Latch	50	22		40	22		ns
f_{MAX}	Clock Frequency	18	35		22	35		MHz

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Standard Test Load



- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50 Ω, $t_r < 5$ ns and $t_f < 5$ ns (between 1.0V and 2.0V).

Truth Tables

A) ADDRESS LATCH

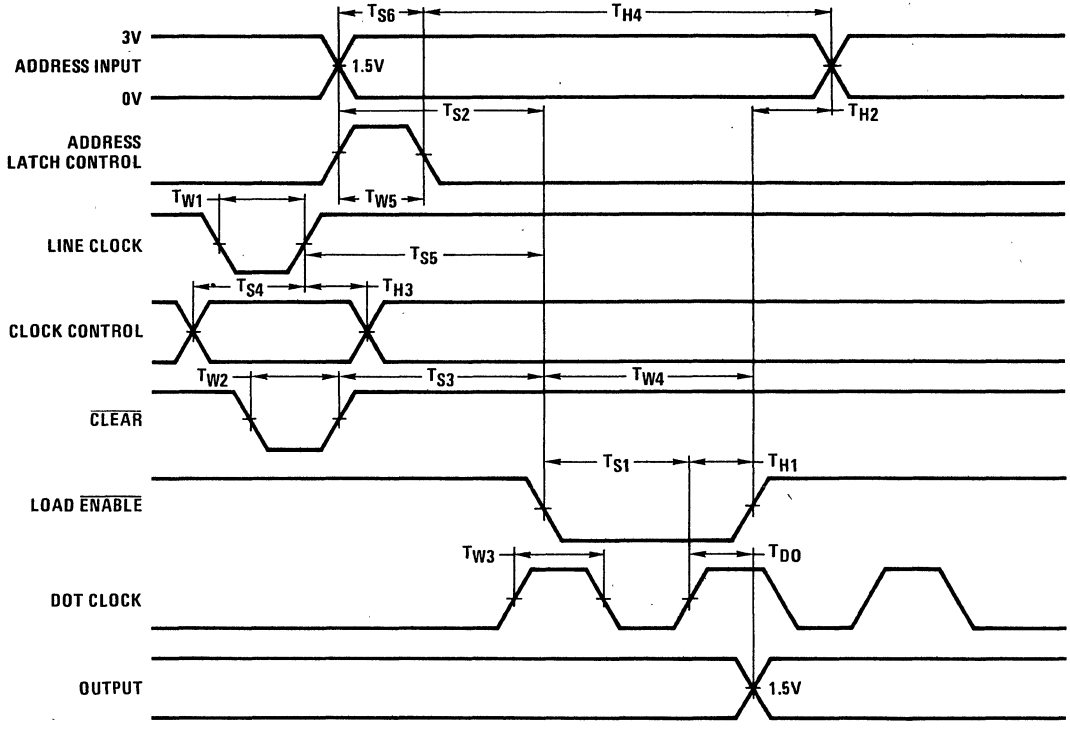
ADDRESS LATCH CONTROL	FUNCTION PERFORMED
0	Latched
1	Fall Through

B) 4-BIT LINE COUNTER

CLOCK CONTROL	LINE CLOCK	$\overline{\text{CLEAR}}$	LINE COUNTER
H	⌐	H	Increment line counter
X	X	L	Asynchronous clear resets counter
L	X	H	Clock inhibited
H	⌐	H	No change on high-to-low clock edge

X = Don't care

Switching Time Waveforms



Definitions

A0–A6: Character address. A 7-bit code which selects 1 of the 128 characters in the font.

$\overline{\text{Clear}}$: Active low clear for mod 16 row counter, (can be used to truncate mod 16 counter).

Line Clock: Clock that advances the line counter. Advances counter on the low-to-high transition.

Clock Control: Enables line clock when high and disables line clock when low.

Load $\overline{\text{Enable}}$: Active low load command which routes data from the character ROM to the "D" inputs of the 7-bit shift register.

Dot Clock: A low-to-high transition of the dot clock loads the shift register if load $\overline{\text{enable}}$ is low or shifts data if load $\overline{\text{enable}}$ is high.

Output: A TTL BI-STATE output buffer.

Functional Description

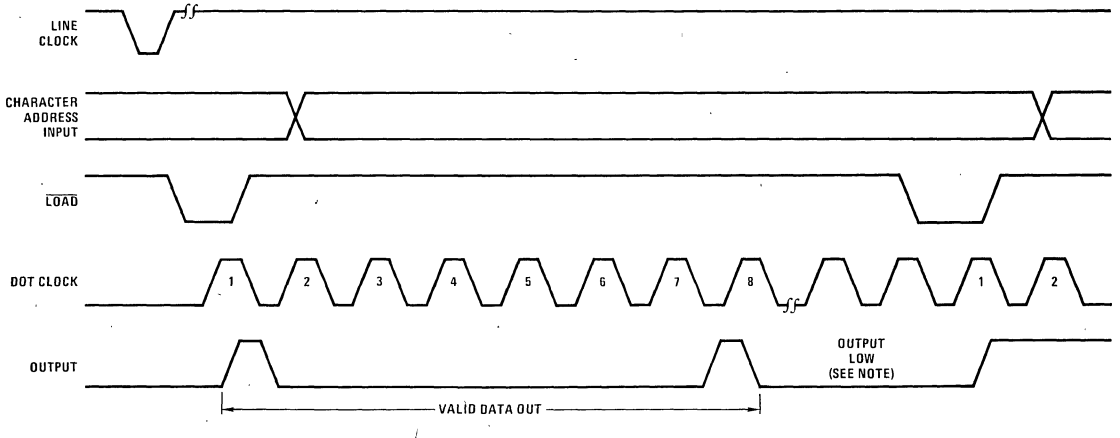
To select a character, a 7-bit binary word must be present at the address inputs A0—A6 when the address latch control is high. This address can be latched by bringing the address latch control signal low after a 40 ns set-up time. When the $\overline{\text{clear}}$ input receives a low pulse, the counter is reset to zero. The shift register can be loaded (T_{S2} ns) after the character is addressed. Data, representing one horizontal line of the addressed character, is available at the output when the load $\overline{\text{enable}}$ input is brought low. As shown in *Figure 1*, valid data arrives serially at the output. Dot clock pulses beyond that required to shift out one line of the character will add lows to the end of character. This provides a horizontal spacing between characters.

Figure 2 shows how the counter sequences through the rows of addressed lines with the application of clock pulses at the line clock input. Any additional line clocks beyond that required to display the character will put a vertical space between characters. This spacing can be truncated by bringing the $\overline{\text{clear}}$ input low.

A two character display example is shown in *Figure 3* and a typical system timing waveform is shown in *Figure 4*. The standard fonts are shown in *Figures 5, 6, 7 and 8*. Descending characters in the 5 x 7 fonts are shifted by virtue of their placement in the matrix. Descending characters in the 7 x 9 fonts are shifted (by th on-chip line shifter/counter) the number of lines indicated by the number in the upper left hand corner of the character drawings in the figures.

Character Cycle — ROM data corresponding to one line of characters is loaded into the shift register T_{S2} after the ROM is addressed. When load $\overline{\text{enable}}$ goes low, ROM data is allowed to be present at the D input of the shift register via the MUX. The first bit of the ROM data is transferred to the output at the next low-to-high transition of the dot clock. After load $\overline{\text{enable}}$ goes back high, the second to seventh clock pulses shift out the rest of the selected row of the addressed character. Additional clock pulses will shift out low data used for spacing.

Line Cycle — The line counter is a mod 16 counter. A low-to-high transition of the line clock advances the line counter to the next count. If, for any reason, the counts need to be truncated, a low signal at the $\overline{\text{clear}}$ input resets the counter to zero. The clock control may be used as a line clock disable. A high signal at the line clock control terminal enables the counter and a low signal disables the line clock.



Note. Output goes and stays low following the leading edge of the eighth Dot-Clock pulse until Load $\overline{\text{enable}}$ is enabled again and new parallel data is loaded into the shift register.

FIGURE 1. Character Cycle

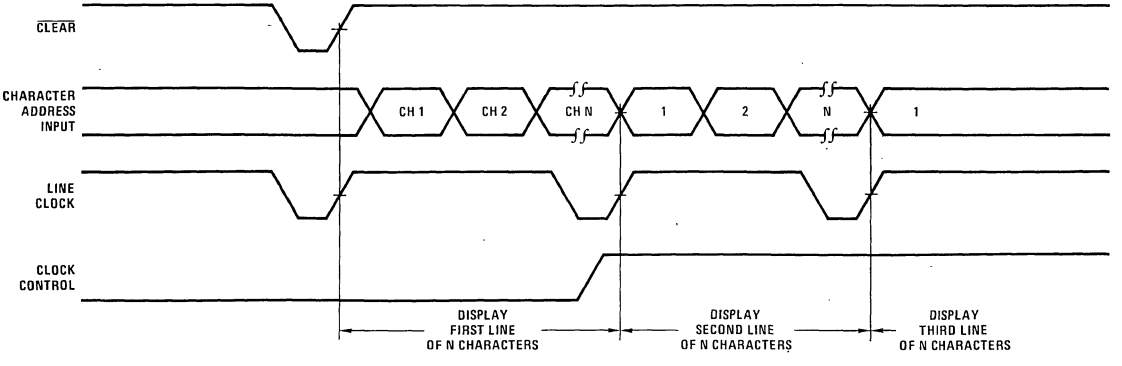


FIGURE 2. Line Cycle

Functional Description (Continued)

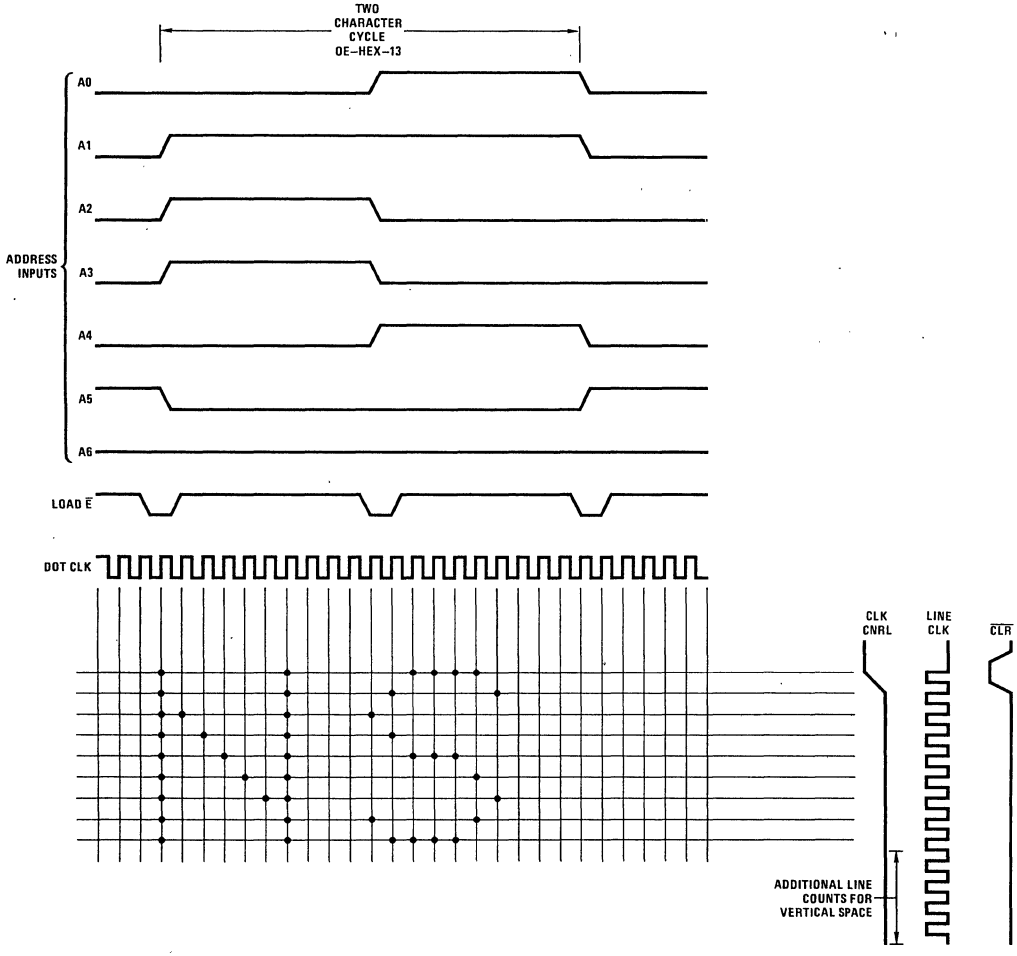
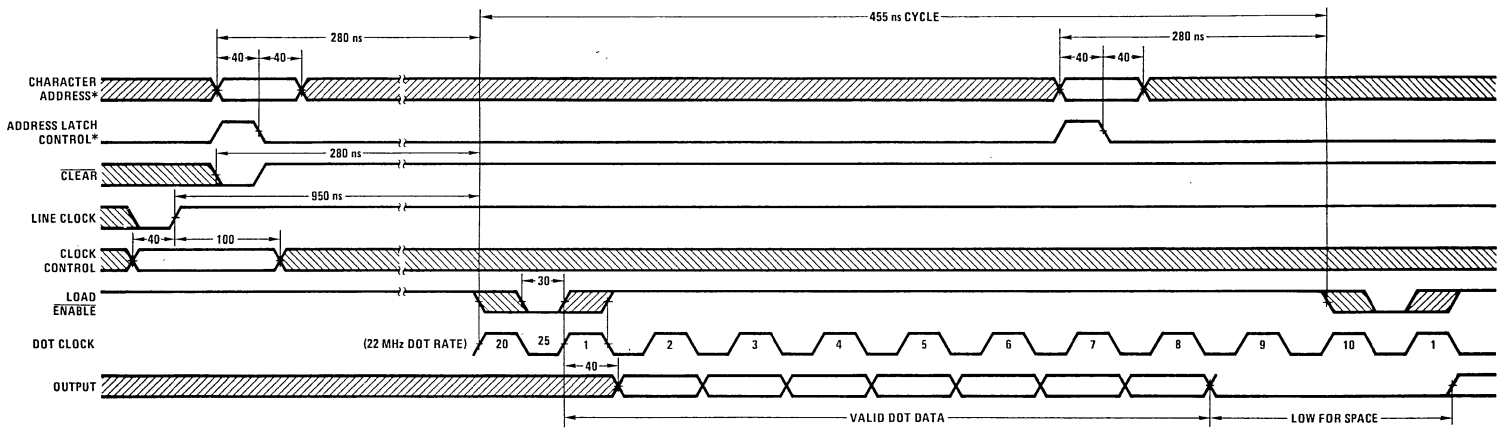


FIGURE 3. Example, Two Character Display Timing – DM86S128CNC



*Shown here for operation with dynamic memory. For static memory operation the address latch control would be tied high and the character addresses would be stable between each address change occurring 280 ns before the high-to-low transition of Load $\overline{\text{enable}}$.

FIGURE 4. Typical System Timing Waveform

Functional Description (Continued)

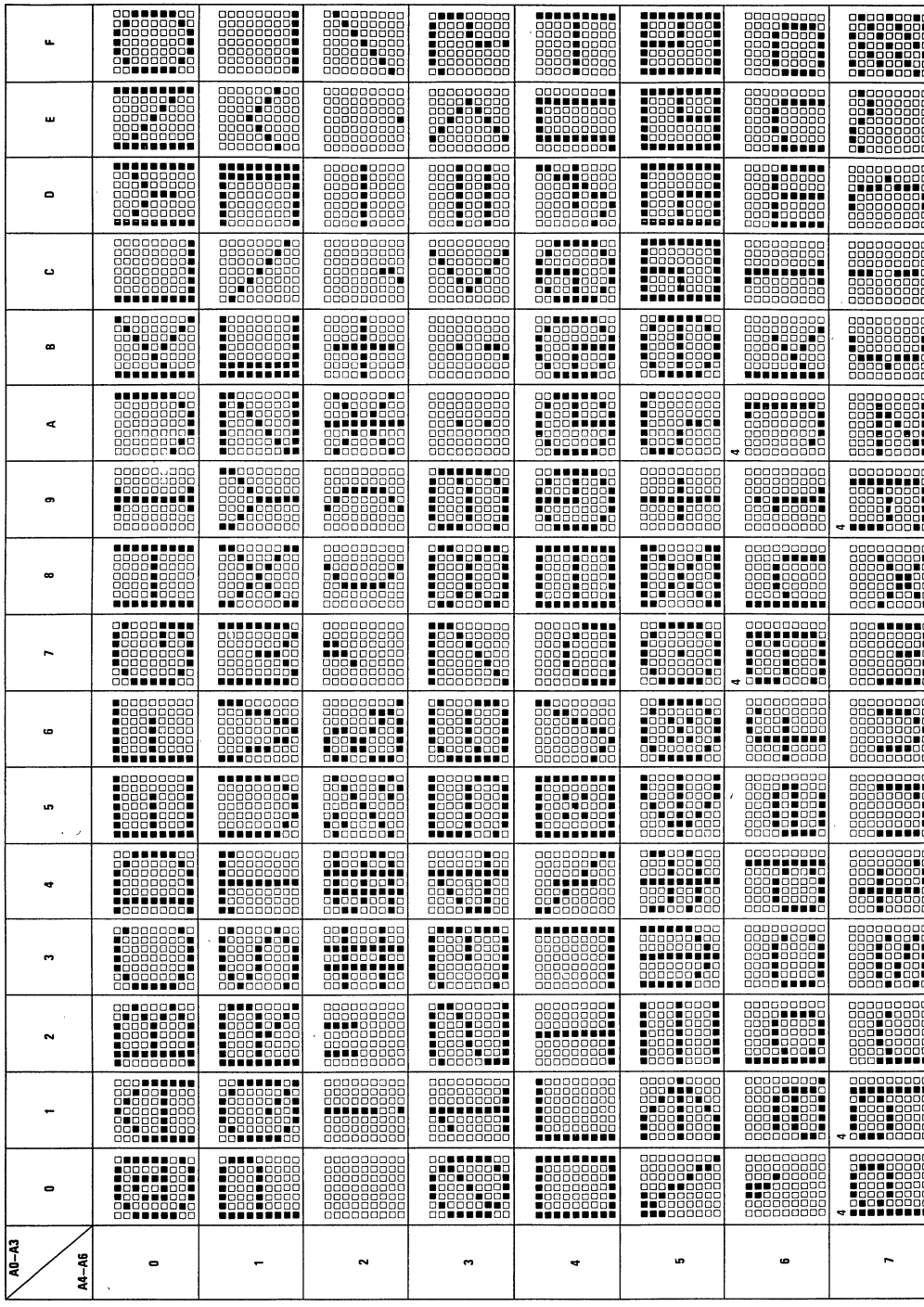


FIGURE 5. DM86S128CNC

Functional Description (Continued)

FIGURE 6. DM86S128CND

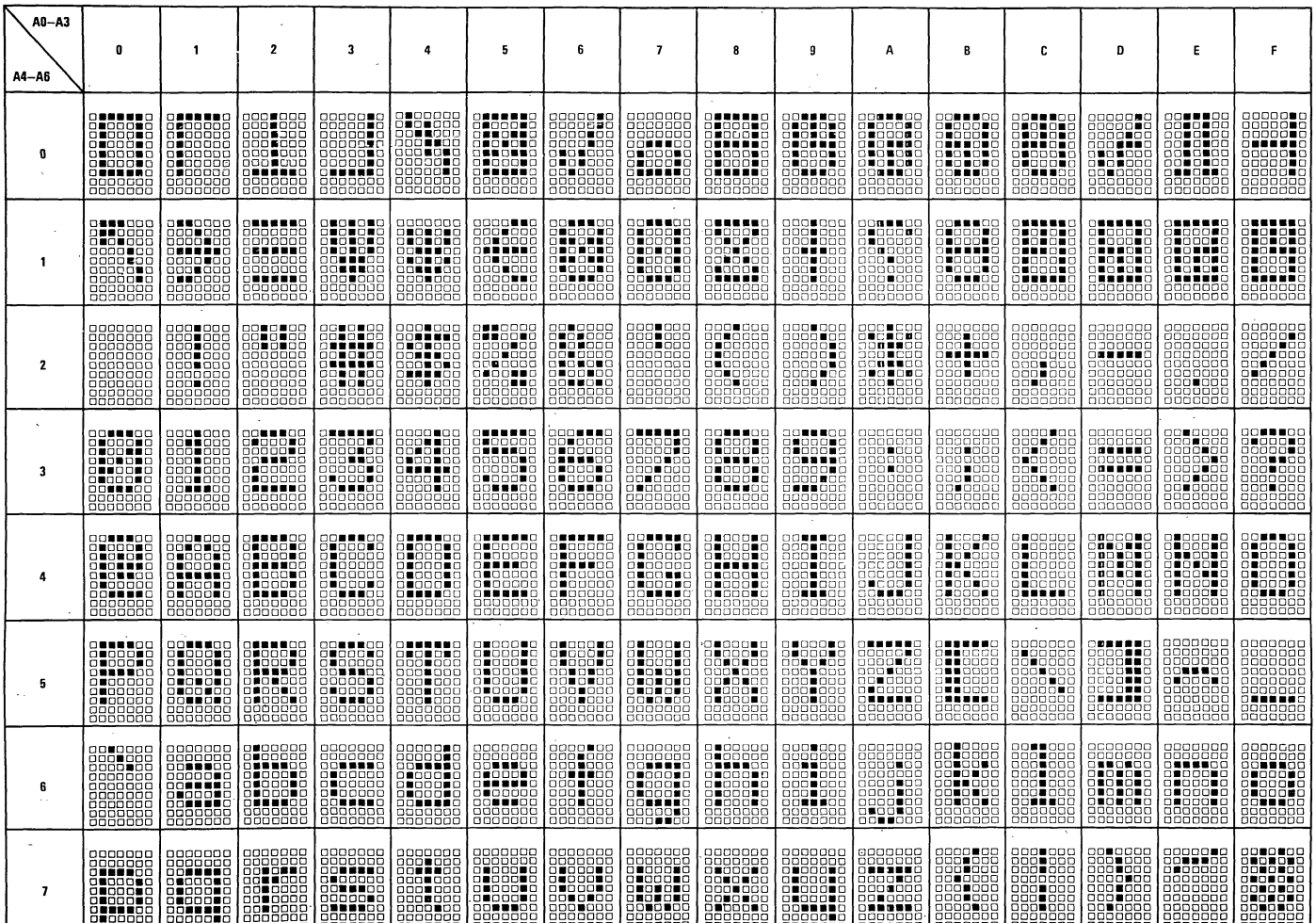


FIGURE 7. DM86S128CQJ

Functional Description (Continued)

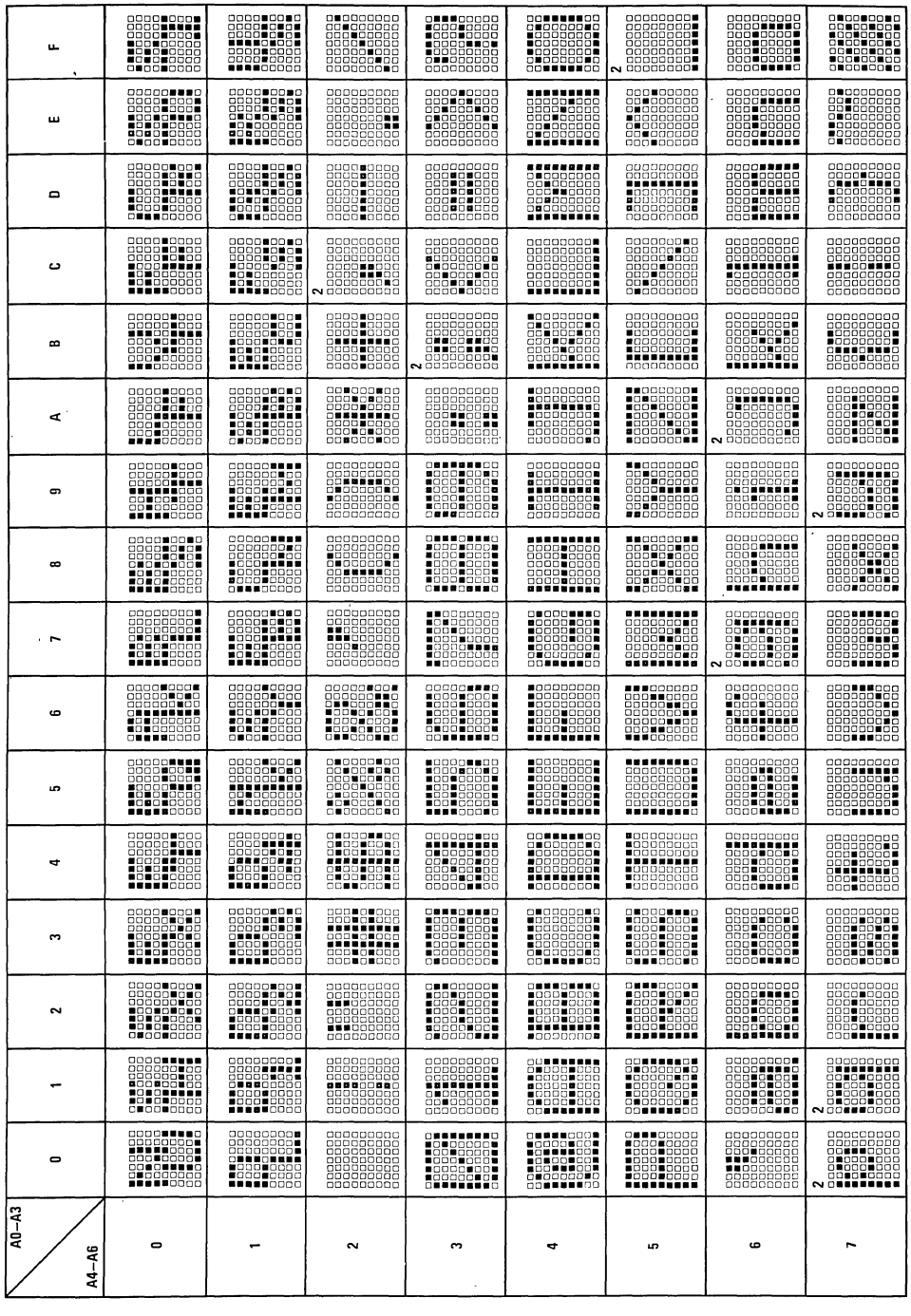


FIGURE 8. DM86S128CQH

Section 22
Bipolar and ECL RAMs

22

National Semiconductor

DM54S189/DM74S189 64-Bit (16 x 4) TRI-STATE® RAM
DM54S289/DM74S289 64-Bit Open-Collector RAM
DM54S189A/DM74S189A High Speed 64-Bit TRI-STATE RAM

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus connected to other similar outputs; yet it retains the fast rise time characteristics of the TTL totem-pole output. Systems utilizing data bus lines with a defined pull-up impedance can employ the open-collector DM54S289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM54S189 outputs are bus connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable is high, the outputs will be in the high-impedance state.

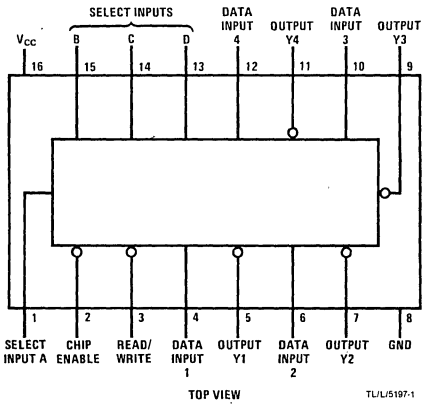
The fast access time of the DM54S189A makes it particularly attractive for implementing high-performance memory functions requiring access times less than 25 ns. The high capacitive drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM54S189A outputs being at a high-impedance during writing, combined with the data inputs being inhibited during reading, means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Features

- Schottky-clamped for high speed applications (S189A)
  - access from chip-enable input 17 ns max
  - access from address inputs 25 ns max
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads (S189, S189A)
- DM54S289/DM74S289 are functionally equivalent and have open-collector outputs
- DM54SXXX is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL circuits
- Chip-enable input simplifies system decoding

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/L/5197-1

Truth Table

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write (Store Complement of Data)	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level
L = Low Level
X = Don't Care

Order Number DM54S189J, DM54S189AJ, DM74S189J, DM74S189AJ, DM54S289J or DM74S289J
See NS Package J16A

Order Number DM74S189N, DM74S189AN or DM74S289N
See NS Package N16E

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM54S189, DM54S289	4.5	5.5	V
DM74S189, DM74S289	4.75	5.25	V
Temperature (T_A)			
DM54S189, DM54S289	−55	+125	°C
DM74S189, DM74S289	0	+70	°C

DM54S189/DM74S189, DM54S289/DM74S289 Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM54S189	2.4	3.4		V
			I_{OH} = −6.5 mA, DM74S189	2.4	3.2		
I_{CEX}	High Level Output Current Open Collector Only	V_{CC} = Min	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM54S189, DM54S289			0.5	V
			DM74S189, DM74S289			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V	DM54S189, DM74S189	−30		−100	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	110	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V	DM54S189, DM74S189			50	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.45V	DM54S189, DM74S189	−50			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"			6.0		pF

DM54S189/DM74S189 Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S189			DM74S189			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{AA}	Access Times from Address		C_L = 30 pF, R_L = 280Ω (*Figure 4*)		25	50		25	35	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns

DM54S189/DM74S189 Switching Characteristics (Continued)

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S189			DM74S189			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	$C_L = 5$ pF, $R_L = 280\Omega$ (*Figure 4*)		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time (*Figure 1*)	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time (*Figure 1*)	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

DM54S289/DM74S289 Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S289			DM74S289			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{AA}	Access Times from Address		$C_L = 30$ pF, $R_{L1} = 300\Omega$, $R_{L2} = 600\Omega$ (*Figure 4*)		25	50		25	35	ns
t_{CHL}	Enable Time from Chip-Enable				12	25		12	17	ns
t_{WHL}	Enable Time from Read/Write	Sense Recovery Time from Read/Write			13	35		13	25	ns
t_{CLH}	Disable Time from Chip-Enable				12	25		12	20	ns
t_{WLH}	Disable Time from Read/Write				13	35		13	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time (*Figure 2*)	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time (*Figure 2*)	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189/289 and across the 0°C to +70°C range for the DM74S189/289. All typicals are given for $V_{CC} = 5.0$V and $T_A = 25$°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded; and the outputs open.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM54S189(A)/DM54S289	4.5	5.5	V
DM74S189(A)/DM74S289	4.75	5.25	V
Temperature (T_A)			
DM54S189(A)/DM54S289	−55	+125	°C
DM74S189(A)/DM74S289	0	+70	°C

DM54S189A/DM74S189A Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA DM54S189A	2.4	3.4		V
			I_{OH} = −6.5 mA DM74S189A	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 16 mA			0.45	V
			I_{OL} = 20 mA			0.5	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.40V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V		−20		−90	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V				40	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.4V		−40			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"			6.0		pF

DM54S189A/DM74S189A Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S189A			DM74S189A			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{AA}	Access Times from Address		$C_L = 30$ pF, $R_L = 280\Omega$ (*Figure 4*)		20	30		20	25	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			11	25		11	17	ns
t_{CZL}	Output Enable Time to Low Level				11	25		11	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	$C_L = 5$ pF, $R_L = 280\Omega$ (*Figure 4*)		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			20			ns
t_{ASW}	Set-Up Time (*Figure 1*)	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			20			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time (*Figure 1*)	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189(A) and across the 0°C to +70°C range for the DM74S189(A). All typicals are given for $V_{CC} = 5.0$V and $T_A = 25$°C.

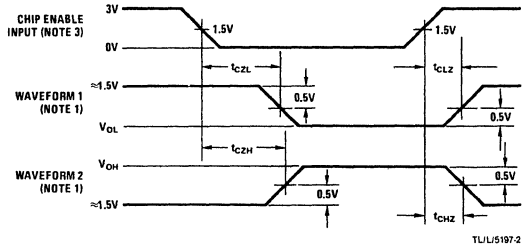
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded; and the outputs open.

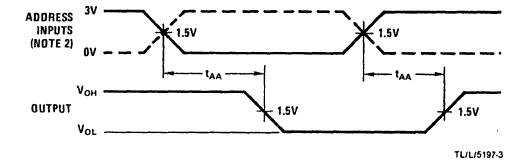
DM54S189(A)/DM74S189(A) Switching Time Waveforms

Enable and Disable Time from Chip-Enable



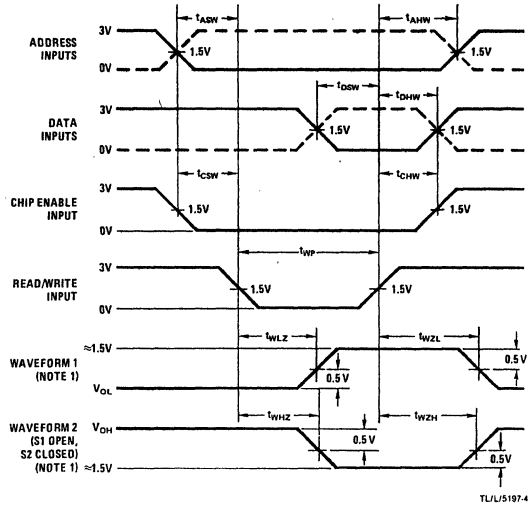
TL/L/5197-2

Access Time from Address Inputs



TL/L/5197-3

Write Cycle



TL/L/5197-4

FIGURE 1

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

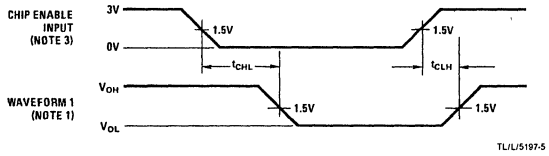
Note 2: When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} \approx 50\Omega$.

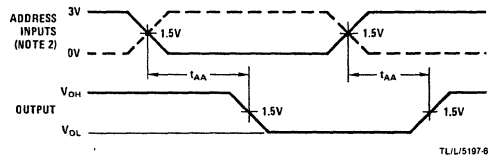
DM54S289/DM74S289 Switching Time Waveforms

Enable and Disable Time from Chip-Enable



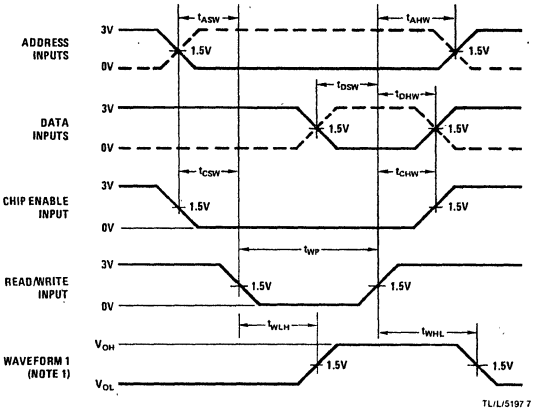
TL/L/5197-5

Access Time from Address Inputs



TL/L/5197-6

Write Cycle



TL/L/5197-7

FIGURE 2

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled.

Note 2: When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} \approx 50\Omega$.

Block Diagram

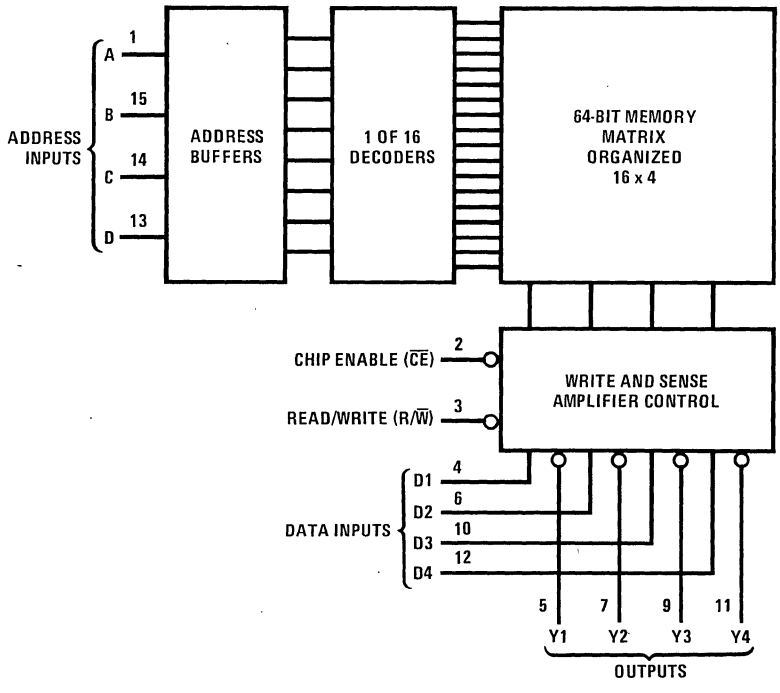
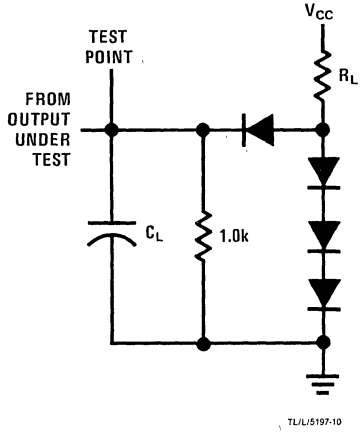


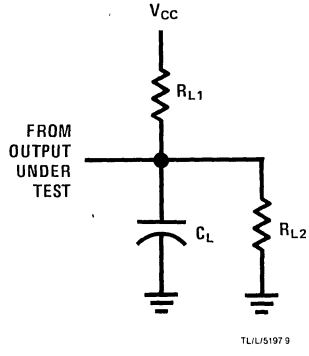
FIGURE 3

AC Test Circuits

DM54S189(A)/DM74S189(A)



DM54S289/DM74S289



C_L includes probe and jig capacitance.
All diodes are 1N3064.

FIGURE 4

National Semiconductor

DM75S06/DM85S06 Open-Collector DM75S07/DM85S07 TRI-STATE DM75S07A/DM85S07A High Speed TRI-STATE Non-Inverting, 64-Bit (16 × 4) RAMs

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs; yet it retains the fast rise time characteristics of the TTL totem-pole output. Systems utilizing data bus lines with a defined pull-up impedance can employ the open-collector DM75S06.

Write Cycle: The information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM85S07 outputs are bus-connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable is high, the outputs will be in the high-impedance state.

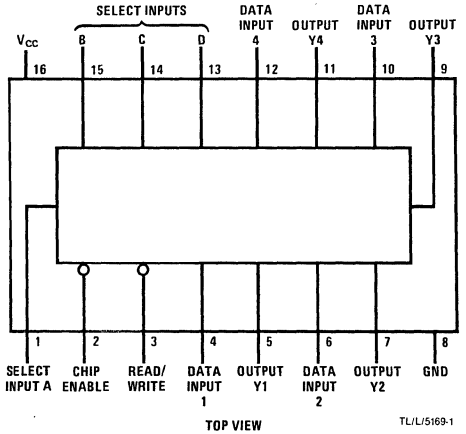
The fast access time of the DM75S07A makes it particularly attractive for implementing high-performance memory functions requiring access times less than 25 ns. The high capacitive drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM75S07 outputs being at a high-impedance during writing, combined with the data inputs being inhibited during reading, means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Features

- Schottky-clamped for high speed applications (75S07A)
  - access from chip-enable input 17 ns max
  - access from address inputs 25 ns max
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads
- DM75S06, DM85S06 are functionally equivalent and have open-collector outputs
- DM75SXX is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL logic circuits
- Chip-enable input simplifies system decoding

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/L/5169-1

Truth Table

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level
L = Low Level
X = Don't Care

Order Number DM75S06J, DM75S07J, DM75S07AJ, DM85S06J, DM85S07J or DM85S07AJ
See NS Package J16A

Order Number DM85S06N, DM85S07N or DM85S07AN
See NS Package N16E

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM75S06/DM75S07(A)	4.5	5.5	V
DM85S06/DM85S07(A)	4.75	5.25	V
Temperature (T_A)			
DM75S06/DM75S07(A)	−55	+125	°C
DM85S06/DM85S07(A)	0	+70	°C

Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM75S07(A)	2.4	3.4		V
			I_{OH} = −5.2 mA, DM85S07(A)	2.4	3.2		V
I_{CEX}	High Level Output Current Open-Collector Only	V_{CC} = Min	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 16 mA			0.45	V
			I_{OL} = 20 mA			0.5	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.40V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V DM75S07(A), DM85S07(A)		−30		−90	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V DM75S07(A), DM85S07(A)				40	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.4V DM75S07(A), DM85S07(A)		−40			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz Output "Off"			6		pF

DM75S07/DM85S07 Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM75S07			DM85S07			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{AA}	Access Times from Address		$C_L = 30$ pF, $R_L = 280\Omega$ (*Figure 4*)		25	50		25	35	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	$C_L = 5$ pF, $R_L = 280\Omega$ (*Figure 4*)		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time (*Figure 1*)	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time (*Figure 1*)	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

DM75S07A/DM85S07A Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM75S07A			DM85S07A			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{AA}	Access Times from Address		$C_L = 30$ pF, $R_L = 280\Omega$ (*Figure 4*)		20	30		20	25	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns

DM75S07A/DM85S07A Switching Characteristics (Continued)

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM75S07A			DM85S07A			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	$C_L = 5$ pF, $R_L = 280\Omega$ (*Figure 4*)		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			20			ns
t_{ASW}	Set-Up Time (*Figure 1*)	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			20			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time (*Figure 1*)	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75S07(A) and across the 0°C to +70°C range for the DM85S07(A). All typicals are given for $V_{CC} = 5.0$V and $T_A = 25$°C.

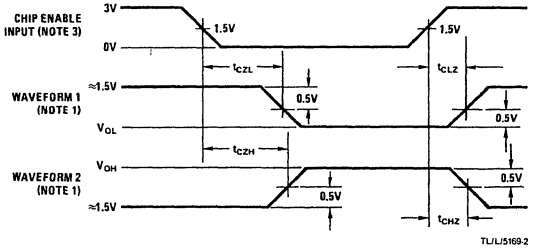
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

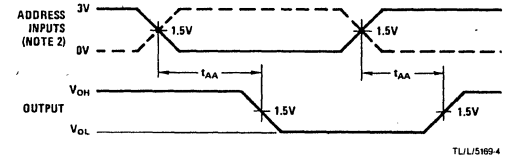
Note 5: I_{CC} is measured with all inputs grounded; and the outputs open.

DM75S07(A)/DM85S07(A) Switching Time Waveforms

Enable and Disable Time from Chip-Enable



Access Time from Address Inputs



Write Cycle

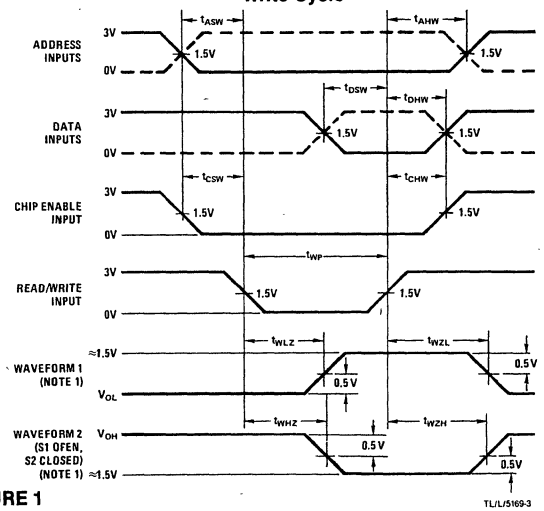


FIGURE 1

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

Note 2: When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} \approx 50\Omega$.

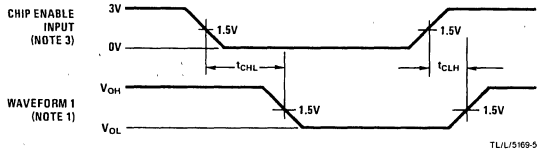
DM75S06/DM85S06 Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

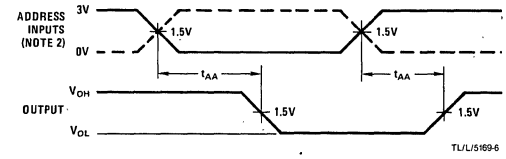
Symbol	Parameter		Conditions	DM75S06			DM85S06			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{AA}	Access Times from Address		$C_L = 30$ pF, $R_{L1} = 300\Omega$, $R_{L2} = 600\Omega$ (*Figure 4*)		25	50		25	35	ns
t_{CHL}	Enable Time from Chip-Enable				12	25		12	17	ns
t_{WHL}	Enable Time from Read/Write	Sense Recovery Time from Read/Write			13	35		13	25	ns
t_{CLH}	Disable Time from Chip-Enable				12	25		12	20	ns
t_{WLH}	Disable Time from Read/Write				13	35		13	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time (*Figure 2*)	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time (*Figure 2*)	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

DM75S06/DM85S06 Switching Time Waveforms

Enable and Disable Time from Chip-Enable



Access Time from Address Inputs



Write Cycle

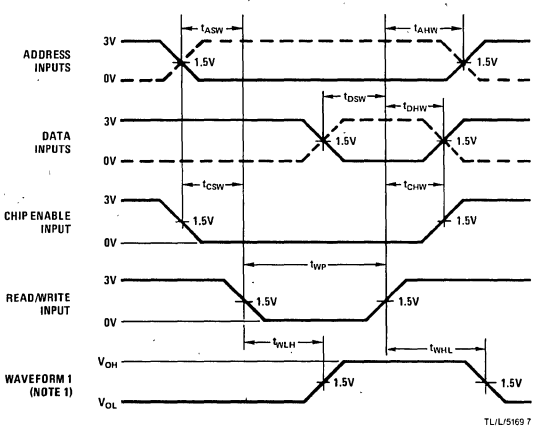


FIGURE 2

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled.

Note 2: When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} \approx 50\Omega$.

Block Diagram

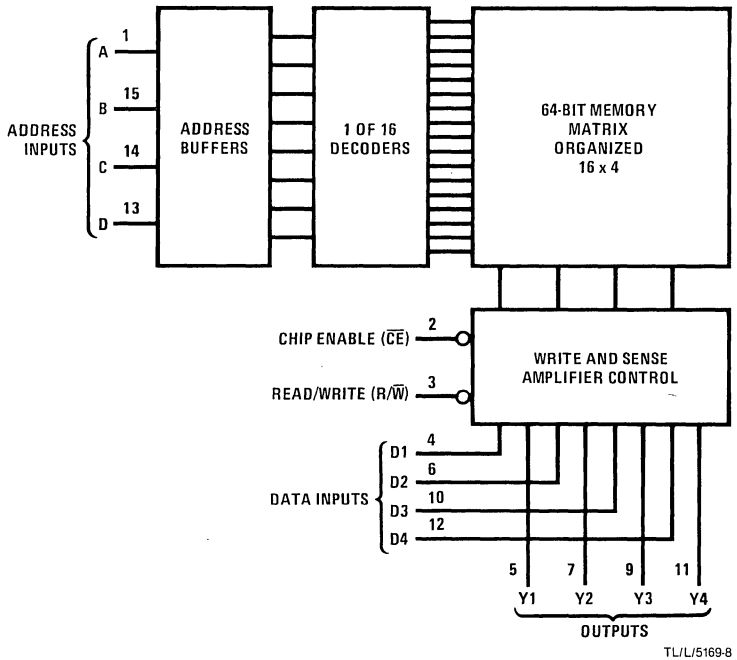
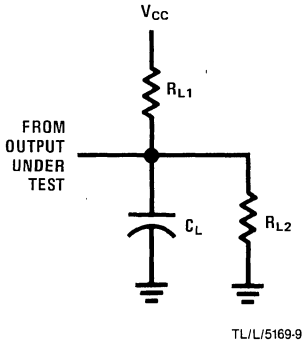


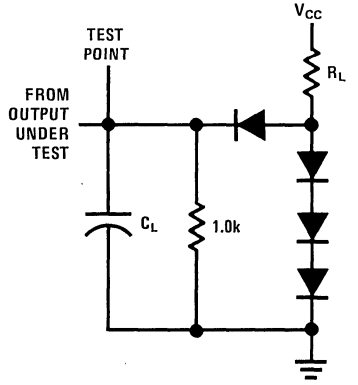
FIGURE 3

AC Test Circuits

DM75S06/DM85S06



DM75S07(A)/DM85S07(A)



C_L includes probe and jig capacitance.
All diodes are 1N3064.

TL/L/5169-10

FIGURE 4

National Semiconductor

DM77S401/DM87S401, DM77S402/DM87S402 First-In, First-Out (FiFo) 64 x 4, 64 x 5 Serial Memories

General Description

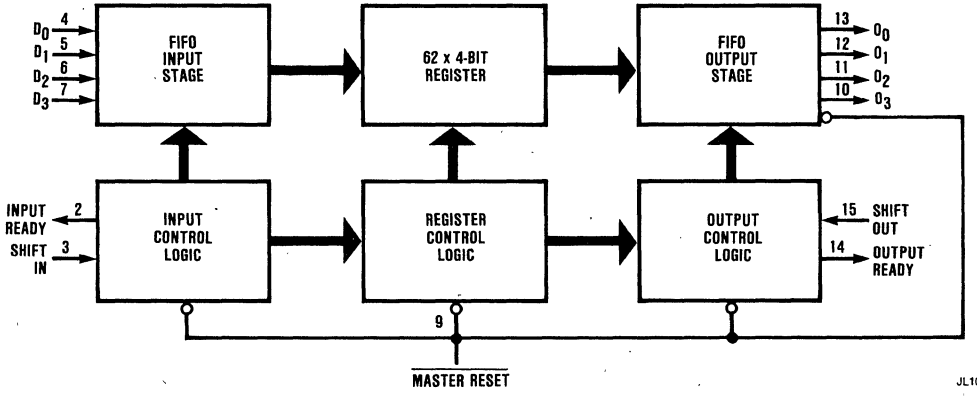
The DM77S401 is an expandable "fall-through" type high-speed First-in, First-out (FiFo) memory organized in 64-word by 4-bit, and 64-word by 5-bit structures respectively. A 10 MHz data rate allows usage in high-speed disc or tape controllers as well as PCM and communications buffer applications.

Features

- 10 MHz shift in, shift out
- TTL inputs and outputs
- Inputs and outputs are symmetrically placed on package
- Easily expandable word and bit dimensions
- Either synchronous or asynchronous operation
- Fairchild F3341 MOS FiFo pin compatible but many times faster!
- Choice of 4-bit or 5-bit data width

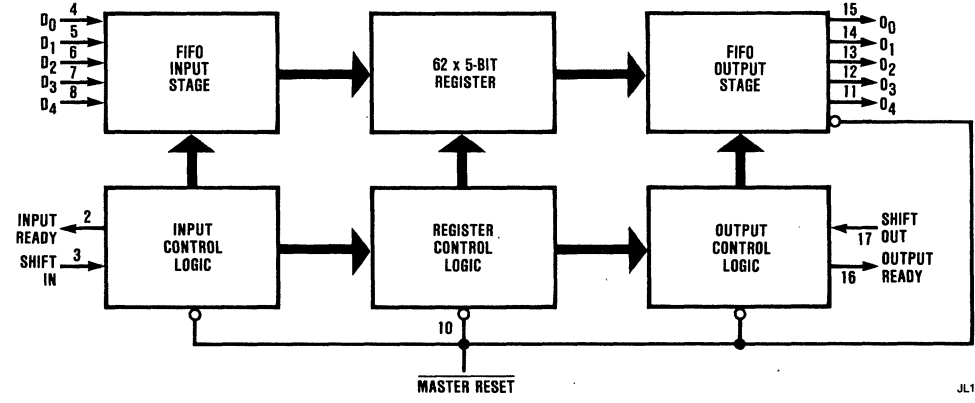
Block Diagrams

DM77/DM87S401
64 x 4



JL1000-1

DM77/DM87S402
64 x 5



JL1000-2

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7 Volts
Input Voltage	7 Volts
Off-State Output Voltage	5.5 Volts
Storage Temperature	−65° to +150° C

Electrical Characteristics Over Operating Conditions DM77/DM87S401; DM77/DM87S402

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Low-Level Input Voltage					0.8	V
V_{IH}	High-Level Input Voltage			2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min,	I_I = -18mA			-1.5	V
I_{IL}	Low-Level D_0-D_4, MR Input Current	V_{CC} = Max,	V_I = 0.45V			-0.4	mA
I_{IH}	High-Level Input Current	V_{CC} = Max,	V_I = 2.4V			50	μA
I_I	Maximum Input Current	V_{CC} = Max,	V_I = 5.5V			1.0	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 8mA			0.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = -0.9mA	2.4			V
I_{OS}	Output Short-Circuit Current (Note 1)	V_{CC} = Max,	V_O = 0V	-20		-90	mA
I_{CC}	Supply Current	V_{CC} = Max Inputs Low, Outputs Open	DM77S401 DM87S401 DM77S402 DM87S402			190 160 210 180	mA

Operating Conditions

Symbol	Parameter	DM77S401/402			DM87S401/402			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature (Note 2)	-55		+125	0		+75	°C
t_{SIH}	Shift In HIGH Time	45	15		35	15		ns
t_{SIL}	Shift In LOW Time	45	22		35	22		ns
t_{IDS}	Input Data Setup	10	−9		0	−9		ns
t_{IDH}	Input Data Hold Time	55	30		45	30		ns
t_{SOH}	Shift Out HIGH Time	45	15		35	15		ns
t_{SOL}	Shift Out LOW Time	45	15		35	15		ns
t_{MRW}	Master Reset Pulse (Note 3)	40	15		35	15		ns
t_{MRS}	Master Reset to SI	45	15		35	15		ns

Note 1: Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
Note 2: Case temperature.
Note 3: Master reset clears all the cells to the empty state, and the data outputs to a LOW state.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	DM77S401/402 Min	DM77S401/402 Typ	DM77S401/402 Max	DM87S401/402 Min	DM87S401/402 Typ	DM87S401/402 Max	Units
f_{IN}	Shift In Rate	7	16		10	16		MHz
t_{IRL}	Shift In to Input Ready LOW		30	60		30	45	ns
t_{IRH}*	Shift In to Input Ready HIGH		33	60		33	45	ns
f_{OUT}	Shift Out Rate	7	16		10	16		MHz
t_{ORL}	Shift Out to Output Ready LOW		40	65		40	55	ns
t_{ORH}**	Shift Out to Output Ready HIGH		45	70		45	60	ns
t_{OD}**	Output Data Delay		38	65		38	55	ns
t_{PT}	Data Throughput or "Fall Through"		1.8	4		1.8	3	μs
t_{MRORL}	Master Reset to OR LOW		30	65		30	60	ns
t_{MRIRH}	Master Reset to IR HIGH		30	65		30	60	ns
t_{IPH}	Input Ready Pulse HIGH	15	22		15	22		ns
t_{OPH}	Output Ready Pulse HIGH	15	22		15	22		ns

*This delay is dependent upon positive pulse width of SI input.

**These delays are dependent upon positive pulse width of SO input.

Functional Description

DATA INPUT

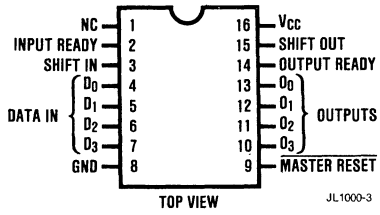
Data is entered in the FiFo on D_0-D_3 (D_0-D_4 on the 402) inputs. If the first location is ready to accept data, the Input Ready (IR) pin will be high. Data then present on the four input pins will be entered to the first location when the Shift In (SI) pin goes high. A high on the SI pin will cause the IR pin to go low. The old data will remain on the first location until SI is brought low again and IR goes low. If SI is brought low before IR goes low, data transfer will not take place until IR goes low. If the FiFo is not full (i.e., all locations contain data), IR will go high, indicating that the first location can accept more data from the four input pins. Simultaneously with IR going high, data will shift to the second location and so forth until it either reaches the output stage or a full location. When the memory is full, IR will remain low and the FiFo will accept no more data.

DATA TRANSFER

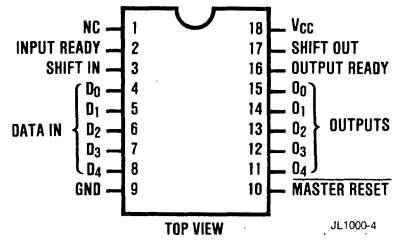
Once data is entered into the second location, the transfer of any full location to the downstream adjacent empty location is automatically activated by an on-chip control. Thus data will stack up at the end of the FiFo while empty locations fill to the front. The time required for the first data to travel from input to output locations is called Data Throughput Time or t_{PT}.

Connection Diagrams

DM77/DM87S401
Dual-In-Line Package



DM77/DM87S402
Dual-In-Line Package



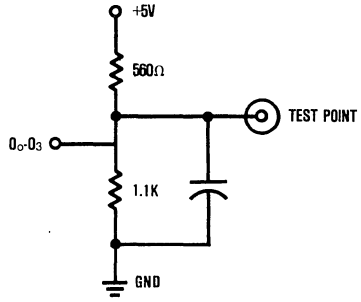
Order Number DM77S401J, DM87S401J, DM77S402J, DM87S402J, DM77S401N, DM87S401N, DM77S402N or DM87S402N
See NS Package J16A or N16A

DATA OUTPUT

Data is output from Pins O_0-O_3 (O_0-O_4 on the 402). When data is shifted into the output stage, Output Ready (OR) goes high to indicate the presence of valid data. When the OR is high, data may be shifted out of O_0-O_3 by pulling Shift Out (SO) high. A high signal on the SO pin will cause the OR pin to go low. When the SO pin is brought low again, and OR is low, any valid data at the next upstream stage is shifted to the output. Then all valid upstream data moves down one location. New valid data on the output stage will again cause OR to go high unless the output stage is empty (all data shifted out), in which case OR stays low.

Input Ready (IR) and Output Ready (OR) may also be used as status signals since IR will stay low for at least t_{PT} if the FiFo is full and OR will stay low for at least t_{PT} if the FiFo is empty.

Standard Test Load



JL1000-5

National Semiconductor

DM77S401A/DM87S401A, DM77S402A/DM87S402A First-In, First-Out (FiFo) 64 x 4, 64 x 5 Serial Memories

General Description

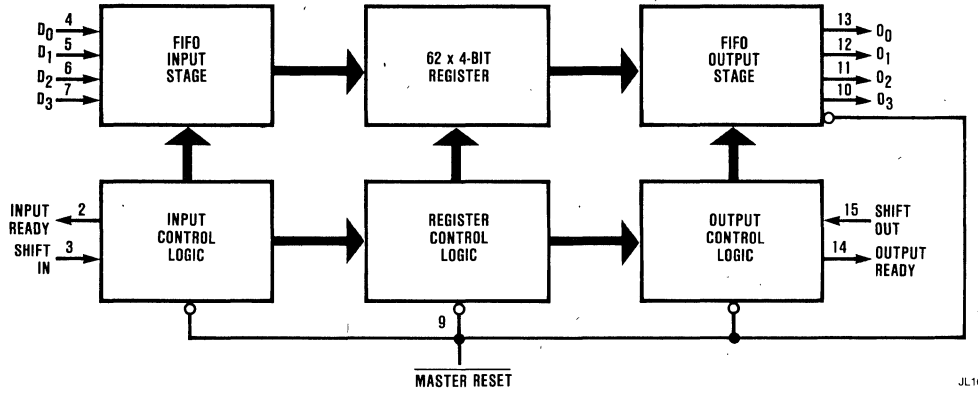
The DM77S401A is an expandable "fall-through" type high-speed First-in, First-out (FiFo) memory organized in 64-word by 4-bit, and 64-word by 5-bit structures respectively. A 15 MHz data rate allows usage in high-speed disc or tape controllers as well as PCM and communications buffer applications.

Features

- 15 MHz shift in, shift out
- TTL inputs and outputs
- Inputs and outputs are symmetrically placed on package
- Easily expandable word and bit dimensions
- Either synchronous or asynchronous operation
- Fairchild F3341 MOS FiFo pin compatible but many times faster!
- Choice of 4-bit or 5-bit data width

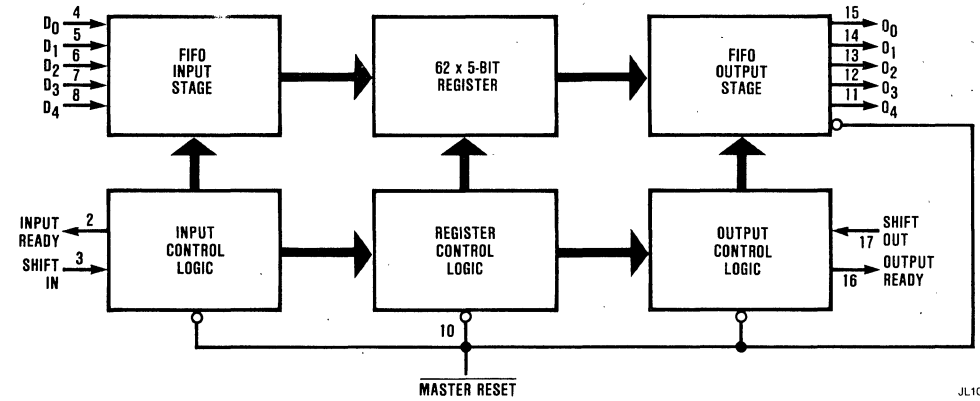
Block Diagrams

DM77/DM87S401A
64 x 4



JL1000-1

DM77/DM87S402A
64 x 5



JL1000-2

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7 Volts
Input Voltage	7 Volts
Off-State Output Voltage	5.5 Volts
Storage Temperature	− 65° to +150° C

Electrical Characteristics Over Operating Conditions DM77/DM87S401A, DM77/DM87S402A

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IL}	Low-Level Input Voltage					0.8	V
V_{IH}	High-Level Input Voltage			2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min,	I_I = -18mA			-1.5	V
I_{IL}	Low-Level D_0-D_4, MR Input Current	V_{CC} = Max,	V_I = 0.45V			-0.4	mA
I_{IH}	High-Level Input Current	V_{CC} = Max,	V_I = 2.4V			50	μA
I_I	Maximum Input Current	V_{CC} = Max,	V_I = 5.5V			1.0	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 8mA			0.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = -0.9mA	2.4			V
I_{OS}	Output Short-Circuit Current (Note 1)	V_{CC} = Max,	V_O = 0V	-20		-90	mA
I_{CC}	Supply Current	V_{CC} = Max Inputs Low, Outputs Open	DM77S401A DM87S401A DM77S402A DM87S402A			200 170 220 190	mA

Operating Conditions

Symbol	Parameter	DM77S401A/402A			DM87S401A/402A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature (Note 2)	-55		+125	0		+75	°C
t_{SIH}	Shift In HIGH Time	35	10		25	10		ns
t_{SIL}	Shift In LOW Time	40	21		33	21		ns
t_{IDS}	Input Data Setup	5	−9		0	−9		ns
t_{IDH}	Input Data Hold Time	45	24		40	24		ns
t_{SOH}	Shift Out HIGH Time	35	10		25	10		ns
t_{SOL}	Shift Out LOW Time	35	10		25	10		ns
t_{MRW}	Master Reset Pulse (Note 3)	30	10		20	10		ns
t_{MRS}	Master Reset to SI	45	10		20	10		ns

Note 1: Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
Note 2: Case temperature.
Note 3: Master reset clears all the cells to the empty state, and the data outputs to a LOW state.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	DM77S401A/402A			DM87S401A/402A			Units
		Min	Typ	Max	Min	Typ	Max	
f_{IN}	Shift In Rate	10	20		15	20		MHz
t_{IRL}	Shift In to Input Ready LOW		25	50		25	40	ns
t_{IRH} *	Shift In to Input Ready HIGH		30	50		30	42	ns
f_{OUT}	Shift Out Rate	10	20		15	20		MHz
t_{ORL}	Shift Out to Output Ready LOW		32	65		32	45	ns
t_{ORH} **	Shift Out to Output Ready HIGH		34	65		34	50	ns
t_{OD} **	Output Data Delay		32	60		32	50	ns
t_{PT}	Data Throughput or "Fall Through"		1.3	2.2		1.3	1.8	μs
t_{MRORL}	Master Reset to OR LOW		26	65		26	60	ns
t_{MRIRH}	Master Reset to IR HIGH		25	65		25	60	ns
t_{IPH}	Input Ready Pulse HIGH	15	22		15	22		ns
t_{OPH}	Output Ready Pulse HIGH	15	22		15	22		ns

*This delay is dependent upon positive pulse width of SI input.

**These delays are dependent upon positive pulse width of SO input.

Functional Description

DATA INPUT

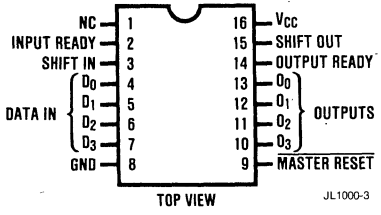
Data is entered in the FiFo on D_0-D_3 (D_0-D_4 on the 402) inputs. If the first location is ready to accept data, the Input Ready (IR) pin will be high. Data then present on the four input pins will be entered to the first location when the Shift In (SI) pin goes high. A high on the SI pin will cause the IR pin to go low. The old data will remain on the first location until SI is brought low again and IR goes low. If SI is brought low before IR goes low, data transfer will not take place until IR goes low. If the FiFo is not full (i.e., all locations contain data), IR will go high, indicating that the first location can accept more data from the four input pins. Simultaneously with IR going high, data will shift to the second location and so forth until it either reaches the output stage or a full location. When the memory is full, IR will remain low and the FiFo will accept no more data.

DATA TRANSFER

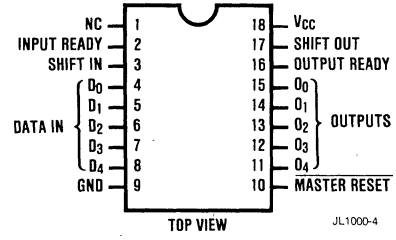
Once data is entered into the second location, the transfer of any full location to the downstream adjacent empty location is automatically activated by an on-chip control. Thus data will stack up at the end of the FiFo while empty locations fill to the front. The time required for the first data to travel from input to output locations is called Data Throughput Time or t_{PT}.

Connection Diagrams

DM77/DM87S401A
Dual-In-Line Package



DM77/DM87S402A
Dual-In-Line Package



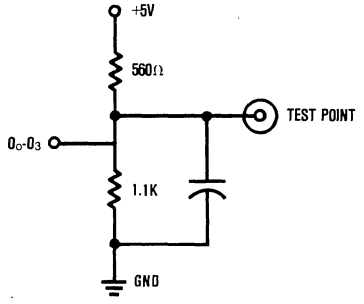
Order Number DM77S401AJ, DM87S401AJ, DM77S402AJ, DM87S402AJ, DM77S401AN, DM87S401AN, DM77S402AN or DM87S402AN
See NS Package J16A or N16A

DATA OUTPUT

Data is output from Pins O_0-O_3 (O_0-O_4 on the 402). When data is shifted into the output stage, Output Ready (OR) goes high to indicate the presence of valid data. When the OR is high, data may be shifted out of O_0-O_3 by pulling Shift Out (SO) high. A high signal on the SO pin will cause the OR pin to go low. When the SO pin is brought low again, and OR is low, any valid data at the next upstream stage is shifted to the output. Then all valid upstream data moves down one location. New valid data on the output stage will again cause OR to go high unless the output stage is empty (all data shifted out), in which case OR stays low.

Input Ready (IR) and Output Ready (OR) may also be used as status signals since IR will stay low for at least t_{PT} if the FiFo is full and OR will stay low for at least t_{PT} if the FiFo is empty.

Standard Test Load



JL1000-5

National Semiconductor

DM75S68/DM85S68 16 x 4 Edge Triggered Registers

General Description

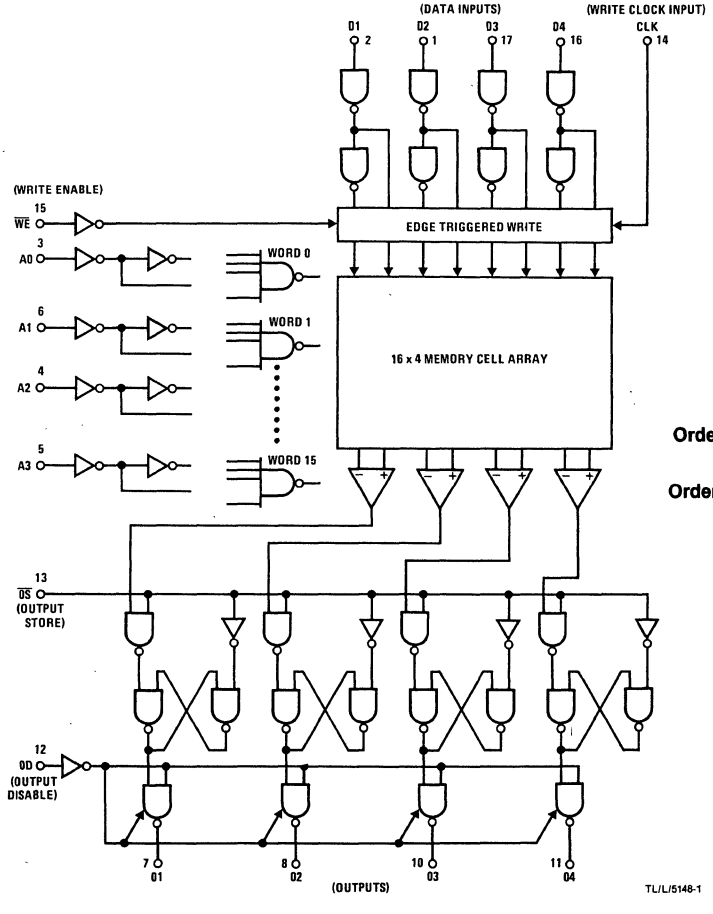
These Schottky memories are addressable "D" register files. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a TRI-STATE® output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state. This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance TRI-STATE condition.

Features

- On-chip output register
- PNP inputs reduce input loading
- Edge triggered write
- High speed—30 ns typ
- All parameters guaranteed over temperature
- TRI-STATE output
- Schottky-clamped for high speed
- Optimized for register stack applications
- Typical power dissipation—350 mW

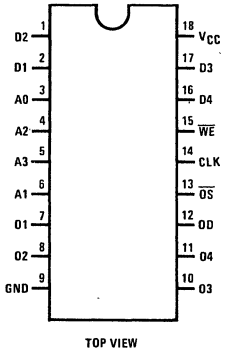
Logic and Block Diagram



TL/L/5148-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/L/5148-2

Order Number DM75S68J or DM85S68J
See NS Package J18A

Order Number DM75S68N or DM85S68N
See NS Package N18A

TRI-STATE® is a registered trademark of National Semiconductor Corp.

Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DM85S68	4.75	5.25	V
DM75S68	4.5	5.5	V
Temperature, T_A			
DM85S68	0	70	°C
DM75S68	−55	+125	°C

Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Parameter		Conditions			Min	Typ	Max	Units
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage						0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM75S68		2.4			V
			I_{OH} = −5.2 mA, DM85S68		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		DM75S68			0.5	V
				DM85S68			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max,	Clock Input				50	μA
		V_{IH} = 2.4V	All Others				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_{IH} = 5.5V					1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max,	Clock Input				−500	μA
		V_{IL} = 0.5V	All Others				−250	μA
I_{OS}	Short Circuit Output Current (4)	V_{CC} = Max, V_{OL} = 0V			−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max				70	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA					−1.2	V
I_{OZ}	TRI-STATE Output Current	V_{CC} = Max	V_O = 2.4V				+40	μA
			V_O = 0.5V				−40	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75S68 and across the 0°C to +70° C range for the DM85S68. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

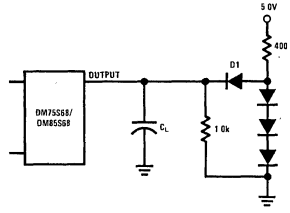
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics over recommended operating range of T_A and V_{CC} unless otherwise noted

Parameter			DM75S68			DM85S68			Units
			Min	Typ	Max	Min	Typ	Max	
t_{ZH}	Output Enable to High Level			20	40		20	35	ns
t_{ZL}	Output Enable to Low Level			14	30		14	24	ns
t_{HZ}	Output Disable Time from High Level			10	18		10	15	ns
t_{LZ}	Output Disable Time from Low Level			12	22		12	18	ns
t_{AA}	Access Time	Address to Output		30	55		30	40	ns
t_{OSA}		Output Store to Output		20	35		20	30	ns
t_{CA}		Clock to Output		25	50		25	40	ns
t_{ASC}	Set-Up Time	Address to Clock	25	5		15	5		ns
t_{DSC}		Data to Clock	15	5		5	0		ns
t_{ASOS}		Address to Output Store	40	15		30	15		ns
t_{WESC}		Write Enable Set-Up Time	10	5		5	0		ns
t_{OSSC}		Store Before Write	15	0		10	0		ns
t_{AHC}	Hold Time	Address from Clock	15	5		10	5		ns
t_{DHC}		Data from Clock	20	5		15	5		ns
t_{AHOS}		Address from Output Store	10	0		5	0		ns
t_{WEHC}		Write Enable Hold Time	20	5		15	5		ns

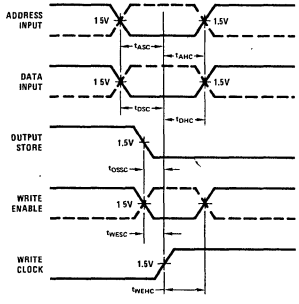
AC Test Circuit and Switching Time Waveforms



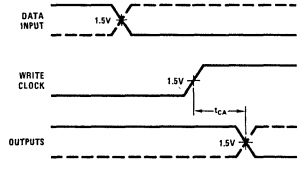
C_L = 5.0 pF for t_{HZ}, t_{LZ}
C_L = 30 pF for all others
C_L includes probe and jig capacitance
All diodes are 1N3064

Write Cycle

Clock Set-Up and Hold Time

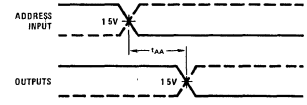


Clock to Output Access

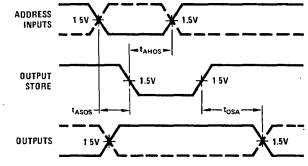


Read Cycle

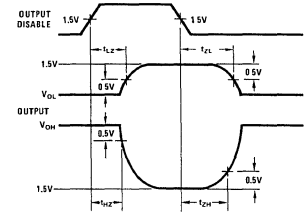
Address to Output Access Time



Output Store Access, Set-Up and Hold Time



Output Disable and Enable Time



Note: Input waveforms supplied by pulse generator having the following characteristics: V = 3.0V, $t_R \leq 2.5$ ns, PRR ≤ 1.0 MHz and Z_{OUT} = 50M.

National Semiconductor

IDM29705/29705A 16-Word by 4-Bit Two-Port RAM/Register File

General Description

The IDM29705 and IDM29705A are 16-word by 4-bit RAM/Register File chips housed in a standard 28-pin dual-in-line package. The IDM29705 and the IDM29705A feature TRI-STATE® outputs. These RAMs, which are fabricated using SCL® (Schottky ECL Technology) feature two separate output ports that enable any two 4-bit words to be read from these outputs simultaneously. Each output port contains a four-bit latch. A common Latch Enable (LE) input is used to control all eight latches. The device, which has two Write Enable (WE) inputs, is designed so that either Write Enable ($WE_{1\ or\ 2}$) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge-triggered.

The device, which has fully decoded A-address and B-address fields, can address any of the 16 memory words for the A-output port and, simultaneously, select any of the 16 words for presentation at the B-output port. Incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load the new data into the device.

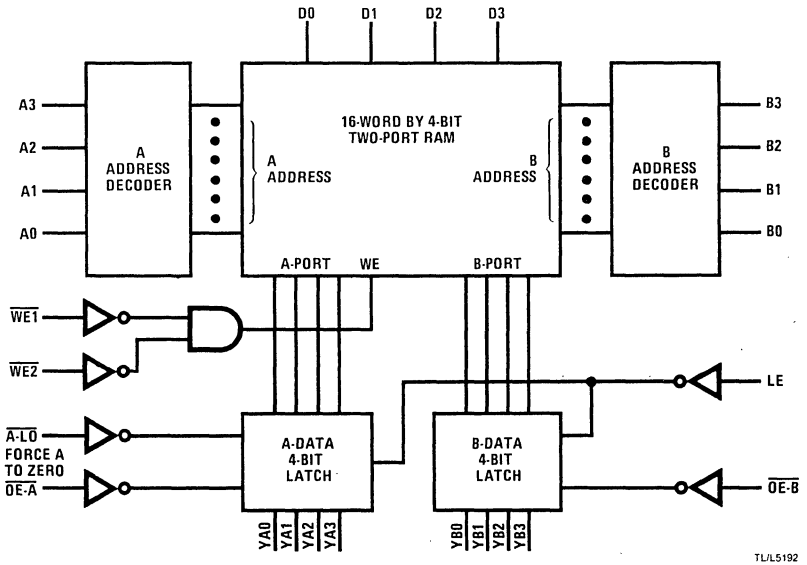
Several of these devices can be cascaded to increase the total number of memory words in the system. When $\overline{OE\text{-}A}$ is high, the A-output port is in the high-impedance mode. $\overline{OE\text{-}B}$, when high, forces the B-output port to the high-impedance state.

The writing of new data into the RAM is controlled by the Write Enable inputs. With both Write Enable inputs low, data is written into the word selected by the B-address field. The memory outputs follow the data inputs during writing if the Latch Enable (LE) is high. With either Write Enable high, no data is written into the RAM.

Features and Benefits

- 16-Word by 4-Bit, 2-Port RAM/Register Files
- Two Output Ports, Each with Separate Output Control
- 4-Bit Latches on Each Output Port
- Non-Inverted Data Output with Respect to Data Input
- Output Enable and Write Enable Inputs Provide Ease in Cascading
- SCL Technology (Schottky ECL) Provides ECL Speeds While Keeping Low Power Schottky Input/Output Voltage and Power Consumption Compatibility
- 100% Reliability Testing in Compliance with MIL-STD-883

IDM29705/29705A Block Diagram



Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +6.3V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5V
DC Output Current, into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Operating Range

P/N	Ambient Temperature	V_{CC}
IDM29705JC	0°C to +70°C	4.75V to 5.25V
IDM29705JM, JM/883	−55°C to +125°C	4.50V to 5.50V
IDM29705AJC, NC	0°C to +70°C	4.75V to 5.25V
IDM29705AJM, JM/883	−55°C to +125°C	4.50V to 5.50V

Standard Screening (conforms to MIL-STD-883 for Class C parts)

Step	MIL-STD-883 Method	Conditions	Level	
			DC, PC	DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C: 24-hour 150°C	100%	100%
Temperature Cycle	1010	C: −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B: 10,000 G	100%	100%
Fine Leak	1014	A: 5×10^{-8} atm-cc/cm^3	100%	100%
Gross Leak	1014	C2: Fluorocarbon	100%	100%
Electrical Test Subgroups 1 and 7 and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening Here for Class B Parts				
Group A Sample Tests Subgroup 1 Subgroup 2 Subgroup 3 Subgroup 7 Subgroup 8 Subgroup 9	5005	See below for definitions of subgroups	 LTPD = 5 LTPD = 7 LTPD = 7 LTPD = 7 LTPD = 7 LTPD = 7	 LTPD = 5 LTPD = 7 LTPD = 7 LTPD = 5 LTPD = 7 LTPD = 5

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level
			DMB, FMB
Burn-In	1015	D: 125°C, 160 hours min	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Group A Subgroups

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum rated temperature
11	Switching	Minimum rated temperature

Electrical Characteristics (over operating temperature range, unless otherwise noted)

Symbol	Parameter	Test Conditions (Note 1)		Min.	Typ (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (IDM29705 only)	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	Mil, I_{OH} = −2.0mA	2.4			Volts
			Com'l, I_{OH} = −4.0mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
			I_{OL} = 16mA (Note 4)			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = min, I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = max, V_{IN} = 0.4V	A_i, B_i			−0.25	mA
			Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = max, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = max, V_{IN} = 5.5V				0.1	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = max, V_{IN} = V_{IH} or V_{IL}	V_o = 2.7V			20	μA
			V_o = 0.4V			−20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = max	29705A	−30		−85	mA
			29705	−25		−85	
I_{CC}	Power Supply Current	V_{CC} = max			120	175	mA
		AJC	V_{CC} = 5.25V, T = 70°C			155	mA
		A/M	V_{CC} = 5.5V, T = 125°C			145	mA

Note 1: For conditions shown as Min. or Max., use the appropriate value specified under Electrical Characteristics for the applicable device type.
Note 2: Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
Note 4: 29705A commercial temperature range only.

Switching Characteristics (Input Levels = 0V and 3.0V, Transitions measured at 1.5V)

Combinational Delays (in nanoseconds) (C_L = 50pF)

Parameters	From	To	Conditions	Comm'l Max. (Note 1) 705	Comm'l Max. (Note 1) 705A	Mil Max. (Note 2) 705	Mil Max. (Note 2) 705A
Access Time	A Address Stable	YA Stable	LE = HIGH	40	30	55	35
	B Address Stable	YB Stable		40	30	55	35
	Both WE LOW	YA = D	LE = HIGH, A = B	45	45	48	45
		YB = D	LE = HIGH	45	45	48	45
Turn-On Time	OE-A or OE-B LOW			25	20	25	25
Turn-Off Time	OE-A or OE-B HIGH	YA or YB Off	C_L = 5pF (Note 3)	20	20	20	20
Reset Time	A-LO LOW	YA LOW		20	20	30	25
Enable Time	LE HIGH	YA and YB Stable		25	20	25	25
	Data In	YA or YB = D	LE = HIGH, WE both LOW, A = B	45	45	45	45

22

Switching Characteristics (Cont'd)

Minimum Setup and Hold Times (in nanoseconds)

Parameters	From	To	Conditions	Comm'l Max. (Note 1) 705	Comm'l Max. (Note 1) 705A	Mil Max. (Note 2) 705	Mil Max. (Note 2) 705A
Data Setup Time	D Stable	Either WE HIGH		20	15	25	20
Data Hold Time	Either WE HIGH	D Changing		0	0	0	0
Address Setup Time	B Stable	Both WE LOW		3	0	5	3
Address Hold Time	Either WE HIGH	B Changing		0	0	0	0
Latch Close Before Write Begins	LE LOW	WE_1 LOW	WE_2 LOW	0	0	0	0
	LE LOW	WE_2 LOW	WE_1 LOW	0	0	0	0
Address Setup Before Latch Closes	A or B Stable	LE LOW		20	15	40	20

Minimum Pulse Widths (in nanoseconds)

Parameters	From	To	Conditions	Comm'l Max. (Note 1) 705	Comm'l Max. (Note 1) 705A	Mil Max. (Note 2) 705	Mil Max. (Note 2) 705A
Write Pulse Width	WE_1	HIGH-LOW-HIGH	WE_2 LOW	25	20	25	20
	WE_2	HIGH-LOW-HIGH	WE_1 LOW	20	20	20	20
A Latch Reset Pulse	A-LO	HIGH-LOW-HIGH		20	15	20	15
Latch Data Capture	LE	LOW-HIGH-LOW	Address Stable	20	15	20	15

Note 1: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$.
Note 2: $-55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$
Note 3: Measured from 1.5V at the input to 0.5V change in the output level.

Function Tables

Write Control

$\overline{WE_1}$	$\overline{WE_2}$	Function	RAM Outputs at Latch Inputs A-Port	RAM Outputs at Latch Inputs B-Port
L	L	Write D into B	A data (A ≠ B)	D input data
X	H	No write	A data	B data
H	X	No write	A data	B data

YA Read

Inputs $\overline{OE\text{-}A}$	Inputs $\overline{A\text{-}LO}$	Inputs LE	YA Output	Function
H	X	X	Z	High impedance
L	L	X	L	Force YA LOW
L	H	H	A-Port RAM data	Latches transparent
L	H	L	NC	Latches retain data

Function Tables (continued)

YB Read

Inputs			
$\overline{OE\text{-}B}$	LE	YB Output	Function
H	X	Z	High impedance
L	H	B-Port RAM data	Latches transparent
L	L	NC	Latches retain data

H = HIGH Z = High impedance
L = LOW NC = No change
X = Don't care

Pinout Descriptions of the IDM29705/29705A

D_3-D_0: Through these inputs new data can be written in the location specified by the B-address inputs.

A_3-A_0: The 4-bit address presented at the A inputs selects one of the 16 memory words for presentation at the A-data latch outputs.

B_3-B_0: The 4-bit address presented at the B inputs selects one of the 16 memory words for presentation at the B-data latch outputs. This address also selects the location into which data is written.

YA_3-YA_0: The four A-data latch outputs.

YB_3-YB_0: The four B-data latch outputs.

$\overline{WE}_1$, $\overline{WE}_2$: Write enable inputs. When both are low, enables data to be written into the RAM location selected by the B-address field. When either Write Enable input is high, no data can be written into memory.

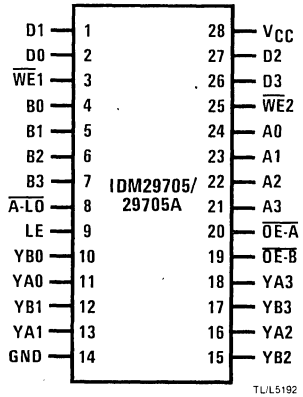
$\overline{OE\text{-}A}$: A-port output enable. When low, data in the A-data latch is present at the YA_i outputs. When high, the YA_i outputs are in the high-impedance mode.

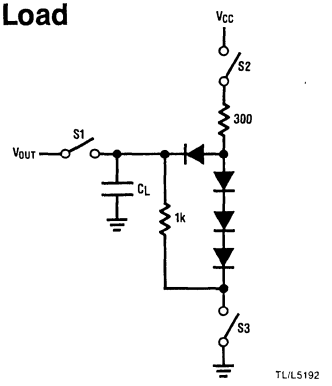
$\overline{OE\text{-}B}$: B-port output enable. When low, data in the B-data latch is presented at the YB_i outputs. When high, the YB_i outputs are in the high-impedance mode.

LE: Latch enable. The LE input acts as control for both the RAM-A and RAM-B output ports. When high the latches are transparent and data from the RAM, as selected by the A and B address inputs, is presented at the outputs. When low, the latches retain the last data read from the RAM regardless of the current A and B address inputs.

$\overline{A\text{-}LO}$: Force A to zero. This input operates to force the A-port latch outputs low independent of the LE input or A address inputs. The A-output bus can be forced low using this control input. With $\overline{A\text{-}LO}$ high, the A latches operate in their normal manner. Once forced low, the A latches remain low independent of the $\overline{A\text{-}LO}$ input if the Latch Enable (LE) is low.

IDM29705/29705A Connection Diagram and Test Load





Note 1: C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.

Note 2: S1, S2, S3 are closed during function tests and all AC tests except output enable tests.

Note 3: S1 and S3 are closed while S2 is open for t_{PZH} test. S1 and S2 are closed while S3 is open for t_{PZL} test.

Note 4: C_L = 5 pF for output disable tests.

National Semiconductor

DM10414, DM10414A 256 x 1 ECL Random Access Memory

General Description

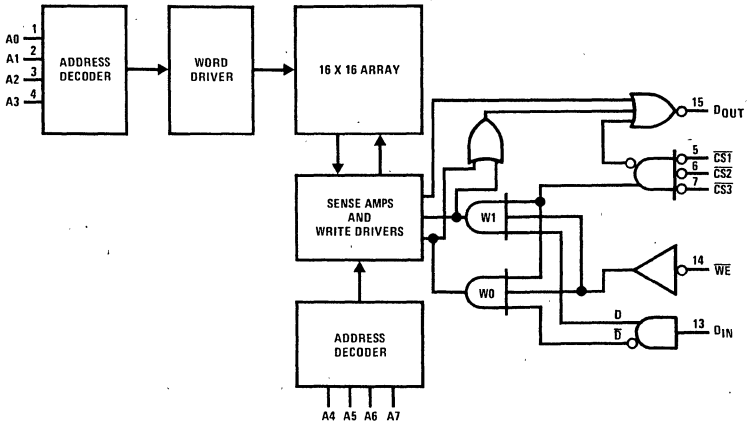
The DM10414, DM10414A is a 256-word by 1-bit ECL random access memory. The fully static memory is designed with active low chip selects and separate I/O pins. The 8 address bits (A0 through A7) are fully decoded on the chip. Applications such as scratch pad, cache, and buffer memories are ideal for this high speed RAM.

An unterminated emitter-follower output is provided to allow the outputs to be wire-ORed. Separate Data In and non-inverted Data Out pins are provided. These RAMs are compatible with compensated and uncompensated 10k ECL families.

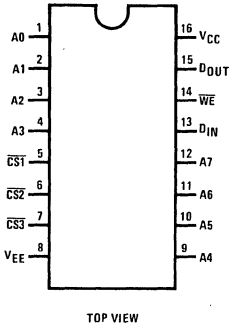
Features

- Fully compatible with standard and voltage compensated 10k series ECL
- Temperature range 0°C to +75°C
- Unterminated emitter-follower output for wire-ORing
- Power dissipation decreases with increasing temperature
- Typical address access
  - DM10414 10 ns
  - DM10414A 7 ns
- Typical chip select access
  - DM10414 4 ns
  - DM10414A 3 ns

Block and Connection Diagrams



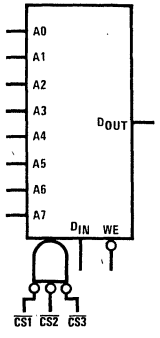
Dual-In-Line Package



TOP VIEW

Order Number DM10414J or DM10414AJ
See NS Package J16A

Logic Symbol



Pin Names

A0–A7	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$	Chip Select Inputs
$\overline{WE}$	Write Enable

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	MODE
H	X	X	L	Not Selected
L	L	H	L	Write 1
L	L	L	L	Write 0
L	H	X	D_{OUT}	Read

L = low (−1.7V nominal)
H = high (−0.9V nominal)
X = don't care

Absolute Maximum Ratings

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{EE})	−5.46	−4.94	V
Ambient Temperature (T_A)	0	+75	°C

DC Electrical Characteristics

V_{EE} = −5.2V, Output Load = 50Ω and 30 pF to −2.0V, T_A = 0°C to +75°C (Notes 1–4)

SYMBOL	PARAMETER	CONDITIONS	T_A	B LIMIT	A LIMIT	UNITS
V_{OH}	Output Voltage High	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000	−840	mV
			+25°C	−960	−810	
			+75°C	−900	−720	
V_{OL}	Output Voltage Low	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1870	−1665	mV
			+25°C	−1850	−1650	
			+75°C	−1830	−1625	
V_{OHC}	Output Voltage High	$V_{IN} = V_{IHB}$ or V_{ILA} Performed on one input at a time	0°C	−1020		mV
			+25°C	−980		
			+75°C	−920		
V_{OLC}	Output Voltage Low	$V_{IN} = V_{IHB}$ or V_{ILA} Performed on one input at a time	0°C		−1645	mV
			+25°C		−1630	
			+75°C		−1605	
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C	−1145	−840	mV
			+25°C	−1105	−810	
			+75°C	−1045	−720	
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	−1490	mV
			+25°C	−1850	−1475	
			+75°C	−1830	−1450	
I_{IH}	Input Current High	$V_{IN} = V_{IHA}$ Performed on one input at a time	0°C to +75°C		220	μA
I_{IL}	Input Current Low, $\overline{CS}$	$V_{IN} = V_{ILB}$ Performed on one input at a time	0°C to +75°C	0.5	170	μA
	All Others			−50		
I_{EE}	Power Supply Current (Pin 8) (Note 5)	All Inputs and Outputs Open	0°C to +75°C	−150		mA

Note 1: Conditions for testing not shown in the tables are chosen to guarantee operation under "worst case" conditions.

Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are: θ_{JA}, (Junction to Ambient) = 90°C/W (still air); θ_{JA} (Junction to Ambient) = 50°C/W (at 400 F.P.M. air flow); θ_{JC} (Juction to Case) = 25°C/W.

Note 4: "A" indicates the most positive value, "B" indicates the most negative value.

Note 5: Typical values at V_{EE} = −5.2V: T_A = 0°C, I_{EE} = −105 mA; T_A = 75°C, I_{EE} = −90 mA.

Functional Description

Addressing the DM10414, DM10414A is achieved by means of the 8 address lines A0–A7. Each of the 2^8 one-zero combinations of the address lines corresponds to a bit location in the memory. The active low Chip Selects together with the unterminated emitter-follower output allows for wire-ORing. A 50Ω resistor to −2V (or an equivalent network) is required to provide a low at the output when the device is off. This termination is required for both single device or wire-ORed operation.

The device is selected with $\overline{CS}$ low and deselected with $\overline{CS}$ high. The operating mode is controlled by the active low Write Enable ($\overline{WE}$). $\overline{WE}$ low causes the data at the Data Input (D_{IN}) to be stored at the selected address. $\overline{WE}$ low also causes the output to be disabled (low due to the 50Ω pull-down resistor). $\overline{WE}$ high causes the data stored at the selected address to be present at the Data Out (D_{OUT}) pin.

AC Electrical Characteristics

V_{EE} = −5.2V ±5%, Output Load = 50Ω, 30 pF to −2.0V, T_A = 0°C to 75°C, 400 LFM

SYMBOL	PARAMETER	CONDITIONS	DM10414A			DM10414			UNITS
			MIN	TYP (NOTE 6)	MAX	MIN	TYP (NOTE 6)	MAX	
READ MODE									
t_{ACS}	Chip Select Access Time	Measured Between 50% Points (Note 7)		3	5		4	7	ns
t_{RCS}	Chip Select Recovery Time			3	5		4	7	ns
t_{AA}	Address Access Time			7	10		10	15	ns
WRITE MODE									
t_W	Write Pulse Width (to Guarantee Writing)	Measured Between 50% Points	6	3.5		8	5		ns
t_{WSD}	Data Set-Up Time Prior to Write		2	0		2	0		ns
t_{WHD}	Data Hold Time After Write		2	0		2	0		ns
t_{WSA}	Address Set-Up Time Prior to Write		3	0		4	0		ns
t_{WHA}	Address Hold Time After Write		2	0		3	1		ns
t_{WSCS}	Chip Select Set-Up Time Prior to Write		2	0		2	0		ns
t_{WHCS}	Chip Select Hold Time After Write		2	0		2	0		ns
t_{WS}	Write Disable Time			3	5		4	7	ns
t_{WR}	Write Recovery Time			3	5		4	7	ns
RISE TIME AND FALL TIME									
t_r	Output Rise Time	Measured Between 50% Points		3			4		ns
t_f	Output Fall Time			3			4		ns

Capacitance

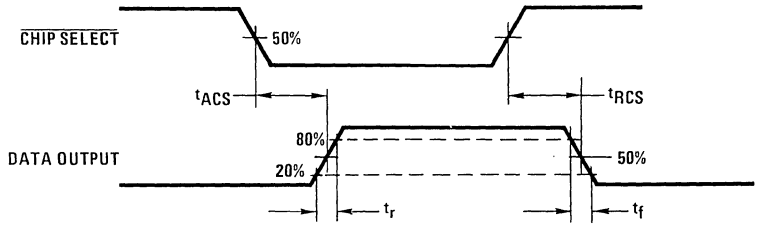
SYMBOL	PARAMETER	CONDITIONS	DM10414A			DM10414			UNITS
			MIN	TYP (NOTE 6)	MAX	MIN	TYP (NOTE 6)	MAX	
C_{IN}	Input Pin Capacitance	Measure With a Pulse Technique		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8	pF

Note 6: Typical values are at V_{EE} = −5.2V, T_A = 25°C and maximum loading.

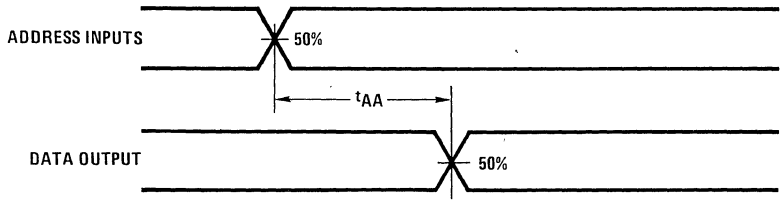
Note 7: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Switching Time Waveforms

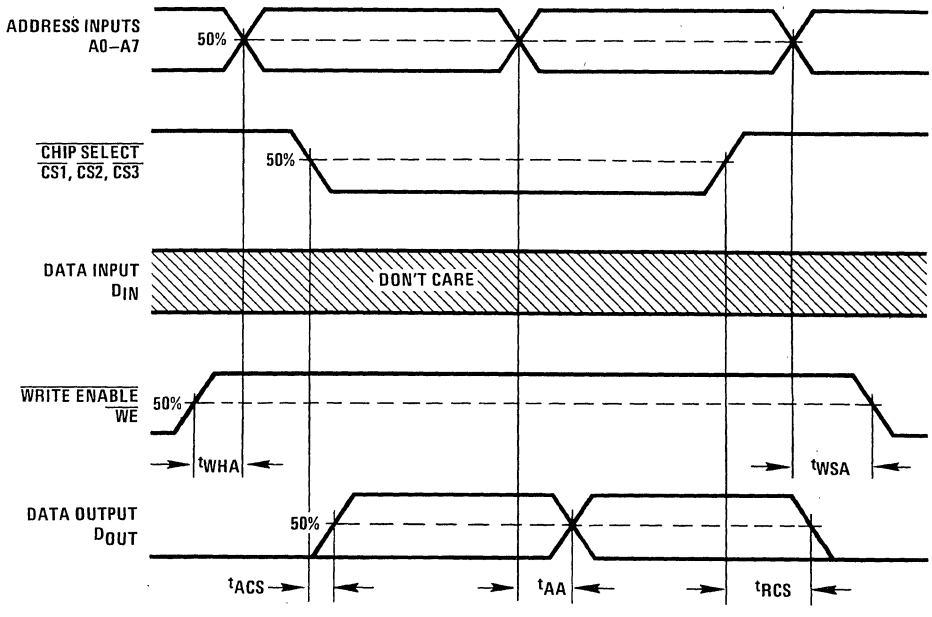
Chip Select Access Time



Address Access Time

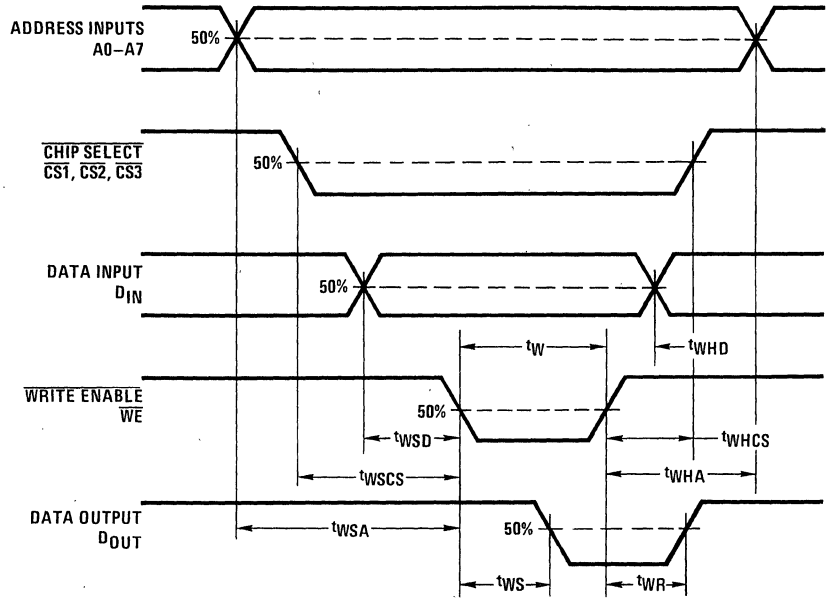


Read Mode



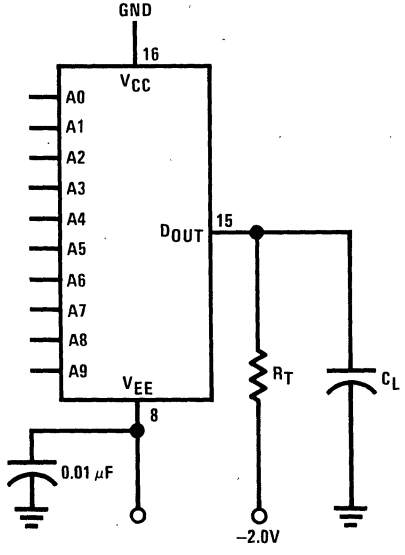
Switching Time Waveforms (Continued)

Write Mode

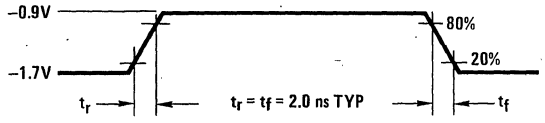


Test Conditions

Loading Conditions



Input Levels



All timing measurements referenced to 50% of input levels
C_L = 30 pF including jig and stray capacitance
R_T = 50Ω

National Semiconductor

DM10415, DM10415A 1024 x 1 ECL Random Access Memory

General Description

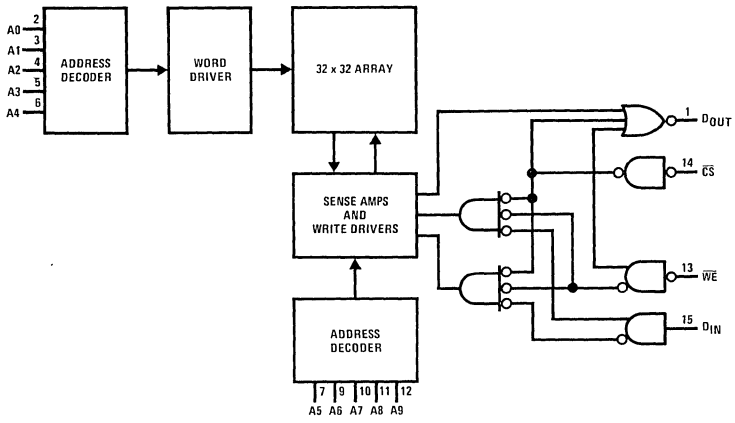
The DM10415, DM10415A is a 1024-word by 1-bit ECL random access memory. This fully static memory is designed with an active low chip select and separate I/O pins. The 10 address bits (A0 through A9) are fully decoded on the chip. Applications such as scratch pad, cache, and buffer memories are ideal for this high speed RAM.

An unterminated emitter-follower output is provided to allow the outputs to be wire-ORed. Separate Data In and non-inverted Data Out pins are provided. These RAMs are compatible with compensated and uncompensated 10k ECL families.

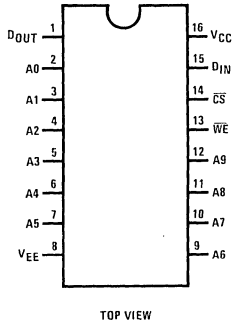
Features

- Fully compatible with standard and voltage compensated 10k series ECL
- Temperature range 0°C to +75°C
- Unterminated emitter-follower output for wire-ORing
- Power dissipation decreases with increasing temperature
- Typical address access
  - DM10415 25 ns
  - DM10415A 12 ns
- Typical chip select access
  - DM10415 7 ns
  - DM10415A 4 ns

Block and Connection Diagrams



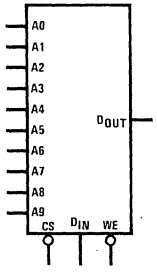
Dual-In-Line Package



TOP VIEW

Order Number DM10415J or DM10415AJ
See NS Package J16A

Logic Symbol



Pin Names

A0–A9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	MODE
H	X	X	L	Not Selected
L	L	H	L	Write 1
L	L	L	L	Write 0
L	H	X	D_{OUT}	Read

L = low (−1.7V nominal)
H = high (−0.9V nominal)
X = don't care

Absolute Maximum Ratings

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{EE})	−5.46	−4.94	V
Ambient Temperature (T_A)	0	+75	°C

DC Electrical Characteristics

V_{EE} = −5.2V, Output Load = 50Ω and 30 pF to −2.0V, T_A = 0°C to +75°C (Notes 1 – 4)

SYMBOL	PARAMETER	CONDITIONS	T_A	B LIMIT	A LIMIT	UNITS
V_{OH}	Output Voltage High	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000	−840	mV
			+25°C	−960	−810	
			+75°C	−900	−720	
V_{OL}	Output Voltage Low	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1870	−1665	mV
			+25°C	−1850	−1650	
			+75°C	−1830	−1625	
V_{OHC}	Output Voltage High	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	−1020		mV
			+25°C	−980		
			+75°C	−920		
V_{OLC}	Output Voltage Low	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C		−1645	mV
			+25°C		−1630	
			+75°C		−1605	
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C	−1145	−840	mV
			+25°C	−1105	−810	
			+75°C	−1045	−720	
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C	−1870	−1490	mV
			+25°C	−1850	−1475	
			+75°C	−1830	−1450	
I_{IH}	Input Current High	$V_{IN} = V_{IHA}$	0°C to +75°C		220	μA
I_{IL}	Input Current Low, $\overline{CS}$	$V_{IN} = V_{ILB}$	0°C to +75°C	0.5	170	μA
	All Others			−50		
I_{EE}	Power Supply Current (Pin 8) (Note 5)	All Inputs and Outputs Open	0°C to +75°C	−150		mA

Note 1: Conditions for testing not shown in the tables are chosen to guarantee operation under "worst case" conditions.

Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are: θ_{JA}, (Junction to Ambient) = 90°C/W (still air); θ_{JA} (Junction to Ambient) = 50°C/W (at 400 F.P.M. air flow); θ_{JC} (Juction to Case) = 25°C/W.

Note 4: "A" indicates the most positive value, "B" indicates the most negative value.

Note 5: Typical values at V_{EE} = −5.2V: T_A = 0°C, I_{EE} = −105 mA; T_A = 75°C, I_{EE} = −90 mA.

Functional Description

Addressing the DM10415/DM10415A is achieved by means of the 10 address lines A0–A9. Each of the 2^{10} one-zero combinations of the address lines corresponds to a bit location in the memory. The active low Chip Select ($\overline{CS}$) together with the unterminated emitter-follower output allows for memory array expansion to 2048 words without additional decoding. This emitter-follower output allows for wire-ORing. A 50Ω resistor to −2V (or an equivalent network) is required to provide a low at the output when the device is off. This termination is required for both single device or wire-ORed operation.

The device is selected with $\overline{CS}$ low and deselected with $\overline{CS}$ high. The operating mode is controlled by the active low Write Enable ($\overline{WE}$). $\overline{WE}$ low causes the data at the Data Input (D_{IN}) to be stored at the selected address. $\overline{WE}$ low also causes the output to be disabled (low due to the 50Ω pull-down resistor). $\overline{WE}$ high causes the data stored at the selected address to be present at the Data Out (D_{OUT}) pin.

AC Electrical Characteristics

V_{EE} = −5.2V, ±5%, Output Load = 50Ω, 30 pF to −2.0V, T_A = 0°C to +75°C, 400 LFM

SYMBOL	PARAMETER	CONDITIONS	DM10415A			DM10415			UNITS
			MIN	TYP (NOTE 6)	MAX	MIN	TYP (NOTE 6)	MAX	
READ MODE									
t_{ACS}	Chip Select Access Time	Measured at 50% of Input to Valid Output (Note 7)		4	8		7	10	ns
t_{RCS}	Chip Select Recovery Time			4	8		7	10	ns
t_{AA}	Address Access Time			12	20		25	35	ns
WRITE MODE									
t_W	Write Pulse Width (to Guarantee Writing)								
	DM10415A	t_{WSA} = 8 ns	12	10		25	20		ns
	DM10415	t_{WSA} = 20 ns							
t_{WSD}	Data Set-Up Time Prior to Write		4	0		5	0		ns
t_{WHD}	Data Hold Time After Write		4	0		5	0		ns
t_{WSA}	Address Set-Up Time Prior to Write								
	DM10415A	t_W = 12 ns	5	3		8	5		ns
	DM10415	t_W = 25 ns							
t_{WHA}	Address Hold Time After Write		3	0		4	1		ns
t_{WSCS}	Chip Select Set-Up Time Prior to Write		4	0		5	0		ns
t_{WHCS}	Chip Select Hold Time After Write		4	0		5	0		ns
t_{WS}	Write Disable Time			4	10		7	10	ns
t_{WR}	Write Recovery Time			4	10		7	10	ns
RISE TIME AND FALL TIME									
t_r	Output Rise Time	Measured Between 20% and 80% Points		5			5		ns
t_f	Output Fall Time			5			5		ns

Capacitance

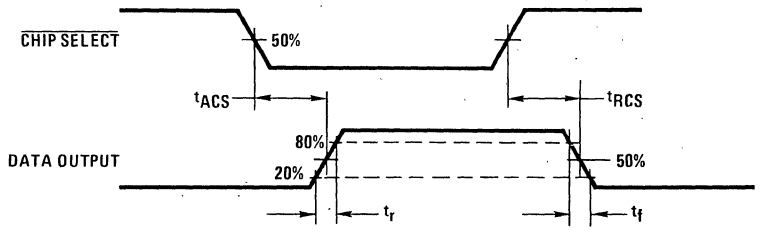
SYMBOL	PARAMETER	CONDITIONS	DM10415A			DM10415			UNITS
			MIN	TYP (NOTE 6)	MAX	MIN	TYP (NOTE 6)	MAX	
C_{IN}	Input Pin Capacitance	Measure With a Pulse Technique		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8	pF

Note 6: Typical values are at V_{EE} = −5.2V, T_A = 25°C and maxumum loading.

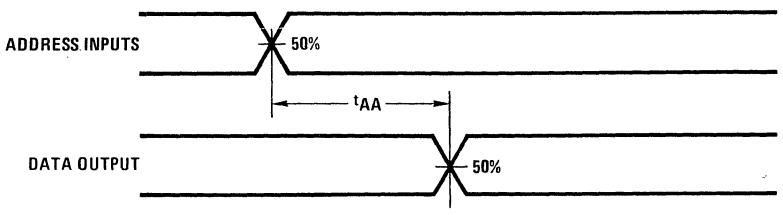
Note 7: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

Switching Time Waveforms

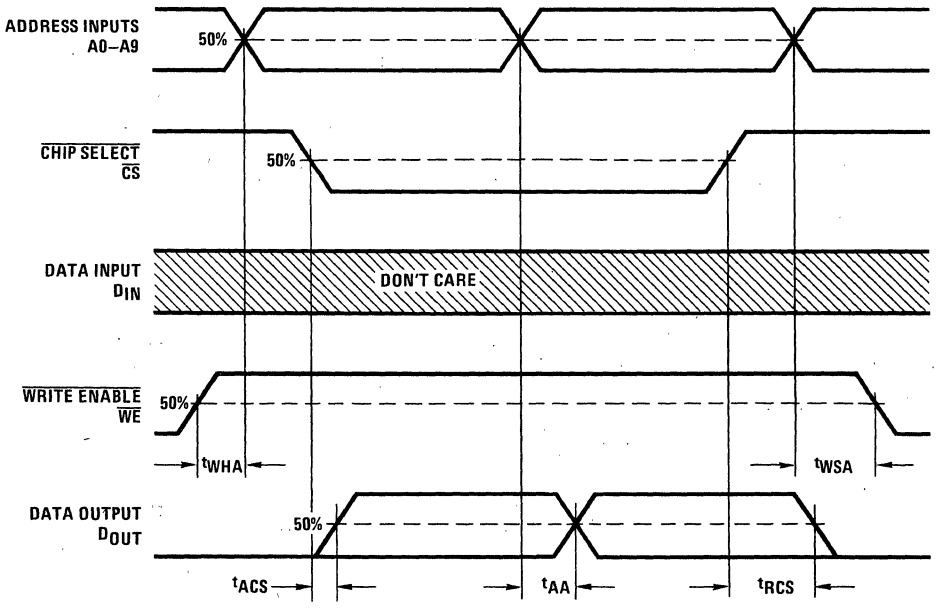
Chip Select Access Time



Address Access Time

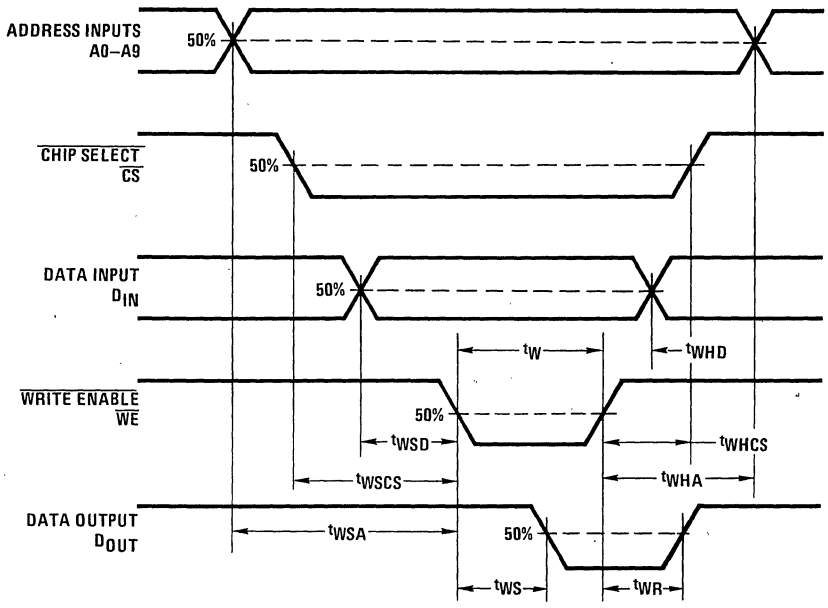


Read Mode



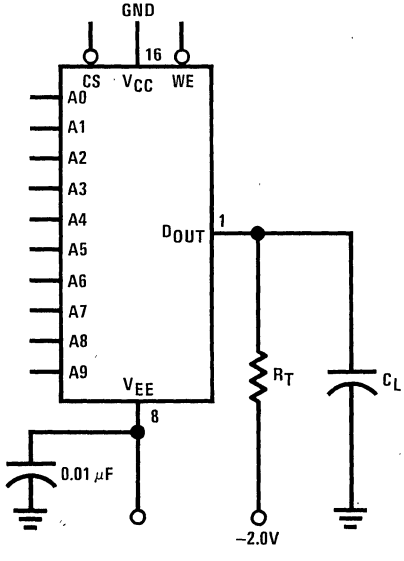
Switching Time Waveforms (Continued)

Write Mode

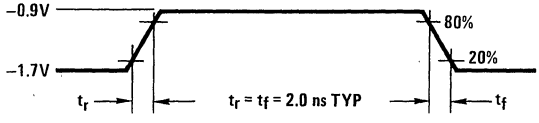


Test Conditions

Loading Conditions



Input Levels



All timing measurements referenced to 50% of input levels
C_L = 30 pF including jig and stray capacitance
R_T = 50Ω

22

National Semiconductor

DM10422 1024-Bit (256 x 4) ECL RAM

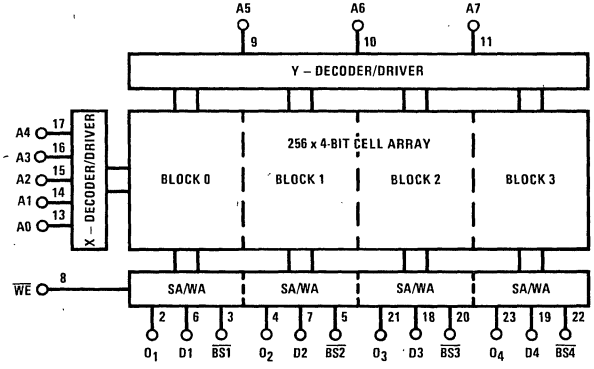
General Description

The DM10422 is normally a 256-word by 4-bit random access memory. However the memory has four Block Select (BS0-BS3) inputs which allow wire-ORing of any of the four blocks for a maximum 1024-word by 1-bit memory. The high speed access time allows its use in scratch pad, buffer, and control storage applications. The device is voltage compensated and is compatible with all 10k logic. Separate Data In and Data Out pins allow the set up of data for a write cycle while performing a read.

Features

- 4 separate Block Select inputs for configurations from 256 x 4 to 1024 x 1
- Maximum address access time—12 ns
- Typical Block Select access time—3.5 ns
- 10k logic compatible

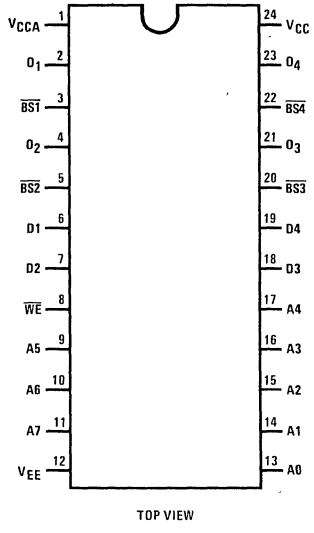
Block and Connection Diagrams



Pin Names

$\overline{BS1}$-$\overline{BS4}$	Block Selects
A0-A7	Address Inputs
$\overline{WE}$	Write Enable
D1-D4	Data Inputs
O_1-O_4	Data Outputs

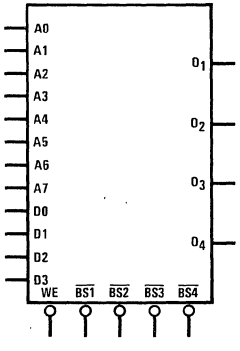
Dual-In-Line Package



TOP VIEW

Order Number DM10422J
See NS Package J24E

Logic Symbol



Truth Table (Positive Logic)

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	DI		
H	X	X	L	Disable
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

Absolute Maximum Ratings

Supply Voltage, V_{EE} to V_{CC}	+0.5V to −7.0V
Input Voltage, V_{IN}	+0.5V to V_{EE}
Output Current	−30 mA
Storage Temperature, T_{stg}	−65°C to +150°C
Storage Temperature Under Bias, T_{stg}(Bias)	−55°C to +125°C

DC Electrical Characteristics

V_{EE} = −5.2V, R_L = 50Ω to −2.0V, T_A = 0°C to +75°C, air flow exceeding 500 LFM

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000		−840	mV
			25°C	−960		−810	
			75°C	−900		−720	
V_{OL}			0°C	−1870		−1665	
			25°C	−1850		−1650	
			75°C	−1830		−1625	
V_{OHC}	Output Threshold Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	−1020			mV
			25°C	−980			
			75°C	−920			
V_{OLC}			0°C			−1645	
			25°C			−1630	
			75°C			−1605	
V_{IH}	Input Voltage	Guaranteed Input Voltage High for All Inputs	0°C	−1145		−840	mV
			25°C	−1105		−810	
			75°C	−1045		−720	
V_{IL}		Guaranteed Input Voltage Low for All Inputs	0°C	−1870		−1490	
			25°C	−1850		−1475	
			75°C	−1830		−1450	
I_{IH}	Input Current	$V_{IN} = V_{IHA}$	0°C to 75°C			220	μA
I_{IL}		$\overline{BS}$	0°C to 75°C	0.5		170	
		Other $V_{IN} = V_{ILB}$		−50			
I_{EE}	Supply Current	All Inputs and Outputs Open, Test Pin 12	0°C	−200	−160		mA
			75°C		−145		

AC Electrical Characteristics

V_{EE} = −5.2V ± 5%, R_L = 50Ω to −2.0V, T_A = 0°C to +75°C, air flow exceeding 500 LFM

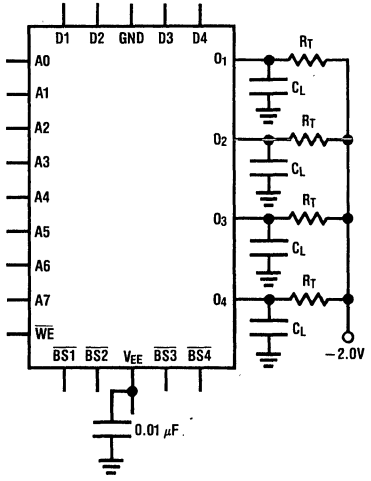
Symbol	Parameter	Conditions	Min	Typ	Max	Units
READ MODE						
t_{ABS}	Block Select Access Time				5.0	ns
t_{RBS}	Block Select Recovery Time				5.0	ns
t_{AA}	Address Access Time				12	ns
WRITE MODE						
t_W	Write Pulse Width	t_{WSA} = 3 ns	7			ns
t_{WSD}	Data Set-Up Time		2.0			ns
t_{WHD}	Data Hold Time		2.0			ns
t_{WSA}	Address Set-Up Time	t_W = 7 ns	3.0			ns
t_{WHA}	Address Hold Time		2.0			ns
t_{WSBS}	Block Select Set-Up Time		2.0			ns
t_{WHBS}	Block Select Hold Time		2.0			ns
t_{WS}	Write Disable Time				5	ns
t_{WR}	Write Recovery Time				7	ns

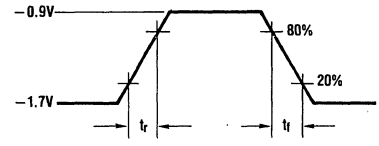
Electrical Characteristics (Continued)

$V_{EE} = -5.2V \pm 5\%$, $R_L = 50\Omega$ to $-2.0V$, $T_A = 0°C$ to $+75°C$, air flow exceeding 500 LFM

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RISE/FALL TIME						
t_r	Output Rise Time			3		ns
t_f	Output Fall Time			3		ns
CAPACITANCE						
C_{IN}	Input Capacitance			4		pF
C_{OUT}	Output Capacitance			7		pF

Test Circuit and Input Waveform





$t_r = t_f = 2.0$ ns $\pm 10\%$

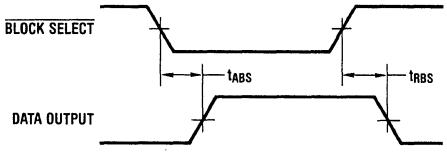
$R_T = 50\Omega$

$C_L = 30$ pF

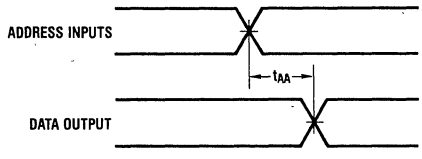
All timing measurements are referenced from 50% of input levels to 50% of input/output levels.

Switching Time Waveforms

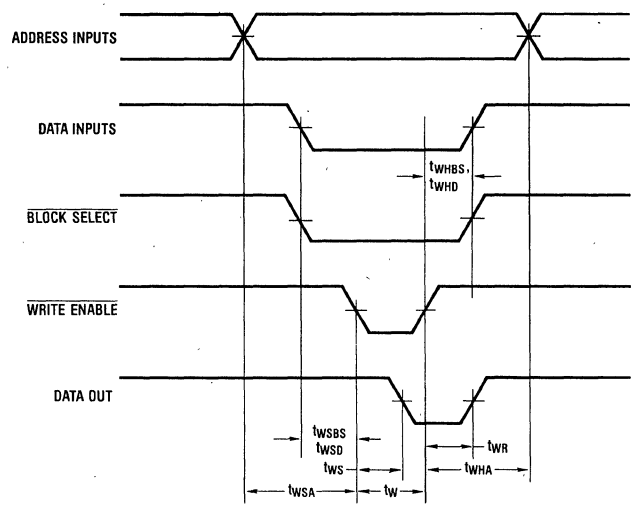
Block Select Access



Address Access Time



Write Mode



DM10422A 1024-Bit (256 x 4) ECL RAM

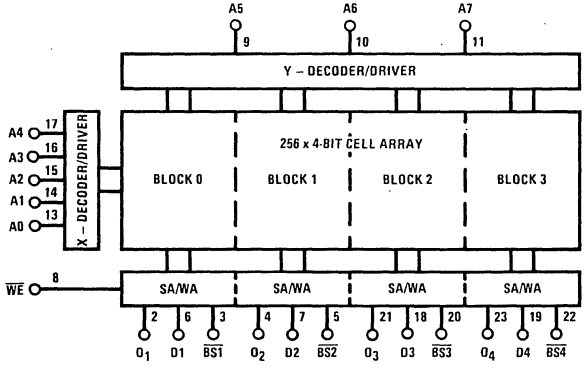
General Description

The DM10422A is normally a 256-word by 4-bit random access memory. However the memory has four Block Select (BS0-BS3) inputs which allow wire-ORing of any of the four blocks for a maximum 1024-word by 1-bit memory. The high speed access time allows its use in scratch pad, buffer, and control storage applications. The device is voltage compensated and is compatible with all 10k logic. Separate Data In and Data Out pins allow the set up of data for a write cycle while performing a read.

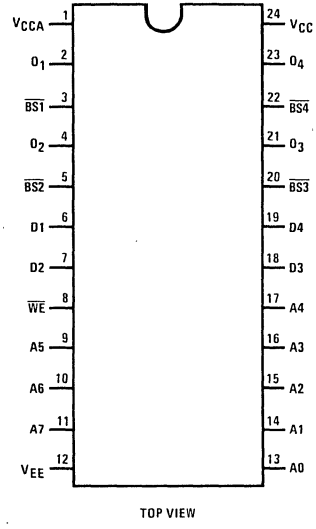
Features

- 4 separate Block Select inputs for configurations from 256 x 4 to 1024 x 1
- Maximum address access time—10 ns
- Typical Block Select access time—3.5 ns
- 10k logic compatible

Block and Connection Diagrams



Dual-In-Line Package



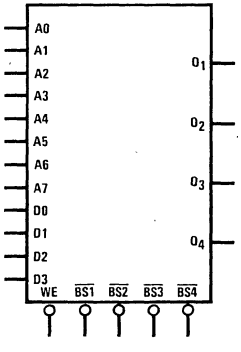
TOP VIEW

Order Number DM10422AJ
See NS Package J24E

Pin Names

$\overline{BS1}$-$\overline{BS4}$	Block Selects
A0-A7	Address Inputs
$\overline{WE}$	Write Enable
D1-D4	Data Inputs
O_1-O_4	Data Outputs

Logic Symbol



Truth Table (Positive Logic)

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	DI		
H	X	X	L	Disable
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

Absolute Maximum Ratings

Supply Voltage, V_{EE} to V_{CC}	+0.5V to −7.0V
Input Voltage, V_{IN}	+0.5V to V_{EE}
Output Current	−30 mA
Storage Temperature, T_{stg}	−65°C to +150°C
Storage Temperature Under Bias, T_{stg}(Bias)	−55°C to +125°C

DC Electrical Characteristics $V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_A = 0°C$ to $+75°C$, air flow exceeding 500 LFM

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{OH}	Output Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	−1000		−840	mV
			25°C	−960		−810	
			75°C	−900		−720	
V_{OL}			0°C	−1870		−1665	
			25°C	−1850		−1650	
			75°C	−1830		−1625	
V_{OHC}	Output Threshold Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	−1020			mV
			25°C	−980			
			75°C	−920			
V_{OLC}			0°C			−1645	
			25°C			−1630	
			75°C			−1605	
V_{IH}	Input Voltage	Guaranteed Input Voltage High for All Inputs	0°C	−1145		−840	mV
			25°C	−1105		−810	
			75°C	−1045		−720	
V_{IL}		Guaranteed Input Voltage Low for All Inputs	0°C	−1870		−1490	
			25°C	−1850		−1475	
			75°C	−1830		−1450	
I_{IH}	Input Current	$V_{IN} = V_{IHA}$	0°C to 75°C			220	μA
I_{IL}		$\overline{BS}$	0°C to 75°C	0.5		170	
		Other		−50			
I_{EE}	Supply Current	All Inputs and Outputs Open, Test Pin 12	0°C	−200	−160		mA
			75°C		−145		

AC Electrical Characteristics $V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_A = 0°C$ to $+75°C$, air flow exceeding 500 LFM

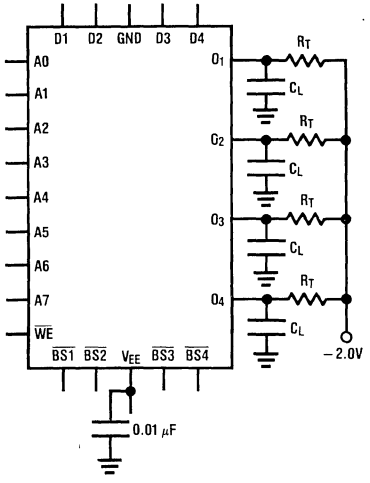
Symbol	Parameter	Conditions	Min	Typ	Max	Units
READ MODE						
t_{ABS}	Block Select Access Time			4	5.0	ns
t_{RBS}	Block Select Recovery Time			4	5.0	ns
t_{AA}	Address Access Time			8	10	ns
WRITE MODE						
t_W	Write Pulse Width	$t_{WSA} = 2$ ns	6	4		ns
t_{WSD}	Data Set-Up Time		2.0			ns
t_{WHD}	Data Hold Time		2.0			ns
t_{WSA}	Address Set-Up Time	$t_W = 6$ ns	2.0			ns
t_{WHA}	Address Hold Time		2.0			ns
t_{WSBS}	Block Select Set-Up Time		2.0			ns
t_{WHBS}	Block Select Hold Time		2.0			ns
t_{WS}	Write Disable Time				5	ns
t_{WR}	Write Recovery Time				7	ns

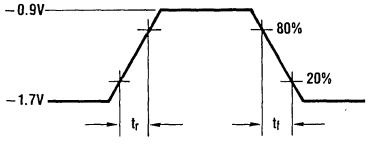
Electrical Characteristics (Continued)

$V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_A = 0°C$ to $+75°C$, air flow exceeding 500 LFM

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RISE/FALL TIME						
t_r	Output Rise Time			3		ns
t_f	Output Fall Time			3		ns
CAPACITANCE						
C_{IN}	Input Capacitance			4		pF
C_{OUT}	Output Capacitance			7		pF

Test Circuit and Input Waveform





$t_r = t_f = 2.0$ ns ± 10%

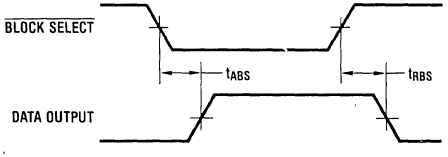
$R_T = 50\Omega$

$C_L = 30$ pF

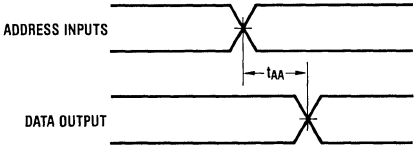
All timing measurements are referenced from 50% of input levels to 50% of input/output levels.

Switching Time Waveforms

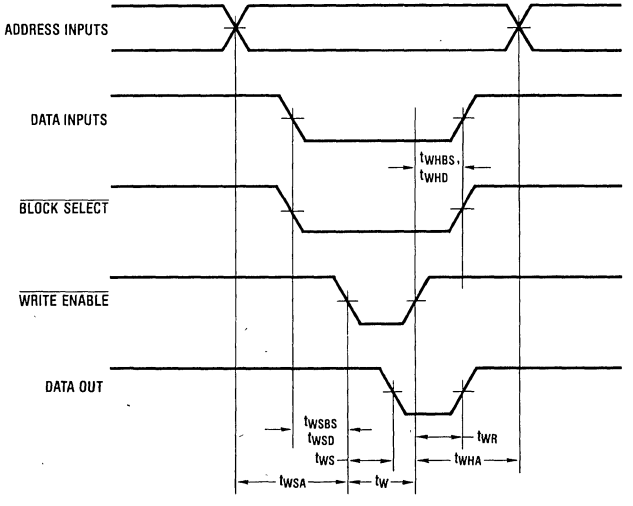
Block Select Access



Address Access Time



Write Mode



National Semiconductor

DM10470 Standard, DM10470A High Speed, DM10470L Low Power 4096-Bit (4096 × 1) ECL RAMs

General Description

The DM10470 is a 4096-bit random access memory organized 4096-words by 1 bit. It is designed for high speed scratch pad and buffer storage applications. It is voltage and temperature compensated and compatible with all 10k logic. It has separate Data In and Data Out pins. The active low Chip Select $\overline{CS}$ and unterminated emitter-follower outputs allow easy expansion.

The DM10470 is speed and power selected to provide cost-performance benefits not available from any other manufacturer.

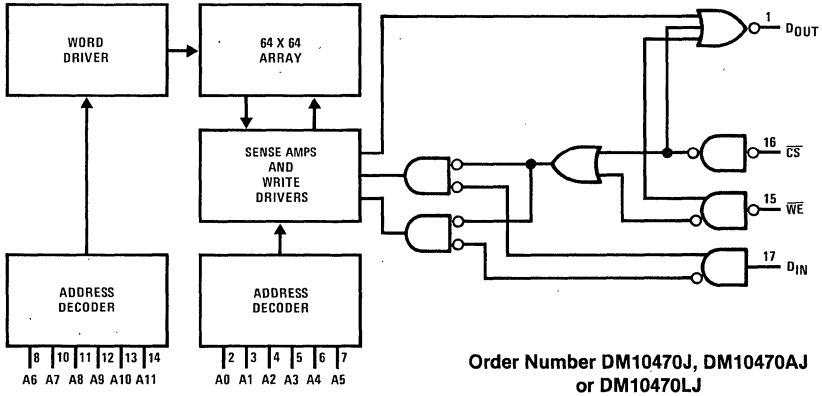
Features

- Three speed-power combinations for maximum cost-performance:

Standard DM10470	25 ns/200 mA max
High speed DM10470A	15 ns/200 mA max
Low power DM10470L	25 ns/130 mA max

- 10k logic compatible
- Unterminated emitter-follower outputs

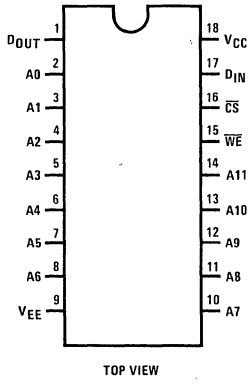
Logic Diagram



Order Number DM10470J, DM10470AJ or DM10470LJ
See NS Package J18A

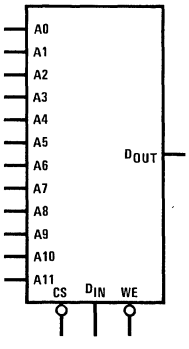
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Symbol



Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

Pin Names

$\overline{CS}$	Chip Select Input
A0-A11	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

Absolute Maximum Ratings

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{EE})	−5.46	−4.94	V
Ambient Temperature (T_A)	0	+75	°C

DC Electrical Characteristics

V_{EE} = −5.2V, output load = 50Ω and 30 pF to −2.0V, T_A = 0°C to +75°C (Notes 1, 2, 3 and 4)

Symbol	Parameter	Conditions	T_A	B Limit	A Limit	Units
V_{OH}	Output Voltage High	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C +25°C +75°C	−1000 −960 −900	−840 −810 −720	mV
V_{OL}	Output Voltage Low	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C +25°C +75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV
V_{OHC}	Output Voltage High	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C +25°C +75°C	−1020 −980 −920		mV
V_{OLC}	Output Voltage Low	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C +25°C +75°C		−1645 −1630 −1605	mV
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C +25°C +75°C	−1145 −1105 −1045	−840 −810 −720	mV
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C +25°C +75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV
I_{IH}	Input Current High	$V_{IN} = V_{IHA}$	0°C to +75°C		220	μA
I_{IL}	Input Current Low, $\overline{CS}$ All Others	$V_{IN} = V_{ILB}$	0°C to +75°C	0.5 −50	170	μA

Note 1: Conditions for testing not shown in the tables are chosen to guarantee operation under worst-case conditions.

Note 2: The specified limits represent the worst-case value for the parameter. Since these worst-case values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: Guaranteed with transverse air flow exceeding 500 linear FPM and 2-minute warm-up period. Typical resistance values of the package are: θ_{JA} (junction to ambient) = 90°C/W (still air); θ_{JA} (junction to ambient) = 50°C/W (at 500 FPM air flow); θ_{JC} (junction to case) = 25°C/W.

Note 4: "A" indicates the most positive value, "B" indicates the most negative value.

AC Electrical Characteristics

$V_{EE} = -5.2V \pm 5\%$, output load = 50Ω, 30 pF to −2.0V, $T_A = 0°C$ to $+75°C$

Symbol	Parameter	Conditions	DM10470A			DM10470			DM10470L			Units
			Min	Typ (Note 6)	Max	Min	Typ (Note 6)	Max	Min	Typ (Note 6)	Max	
READ MODE												
t_{ACS}	Chip Select Access Time	Measured at 50% of Input to 50% of Output (Note 7)		4	8		5	10		5	10	ns
t_{RCS}	Chip Select Recovery Time			4	8		5	10		5	10	ns
t_{AA}	Address Access Time			12	15		18	25		18	25	ns
WRITE MODE												
t_W	Write Pulse Width (to Guarantee Writing)											
	DM10470A	$t_{WSA} = 3$ ns	10			15			15			ns
	DM10470/L	$t_{WSA} = 6$ ns										
t_{WSD}	Data Set-Up Time Prior to Write		2	1		2	1		2	1		ns
t_{WHD}	Data Hold Time After Write		2	0		2	0		2	0		ns
t_{WSA}	Address Set-Up Time Prior to Write											
	DM10470A	$t_W = 10$ ns	3	1		3	1		3	1		ns
	DM10470/L	$t_W = 15$ ns										
t_{WHA}	Address Hold Time After Write		2	0		2	0		2	0		ns
t_{WSCS}	Chip Select Set-Up Time Prior to Write		2	1		2	1		2	1		ns
t_{WHCS}	Chip Select Hold Time After Write		2	0		2	0		2	0		ns
t_{WS}	Write Disable Time	50% of Input to 50% of Output		5	8		5			5	8	ns
t_{WR}	Write Recovery Time			5	8		5			5	8	ns
RISE TIME AND FALL TIME												
t_r	Output Rise Time	Measured Between 20% and 80% Points		3			3			3		ns
t_f	Output Fall Time			3			3			3		ns

Capacitance

Symbol	Parameter	Conditions	DM10470A			DM10470			DM10470L			Units
			Min	Typ (Note 6)	Max	Min	Typ (Note 6)	Max	Min	Typ (Note 6)	Max	
C_{IN}	Input Pin Capacitance	Measure with a Pulse Technique		4	5		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8		7	8	pF

Power Supply Current $V_{EE} = -5.2V$, output load = 50Ω and 30 pF to −2.0V

Symbol	Parameter	Conditions	DM10470A B Limit	DM10470 B Limit	DM10470L B Limit	Units
I_{EE}	Power Supply Current (Pin 8) (Note 5)	All Inputs and Outputs Open, $T_A = 25°C$	−200	−200	−130	mA

Note 5: Typical values at $V_{EE} = -5.2V$: $T_A = 0°C$, $I_{EE} = -145$ mA; $T_A = 25°C$, $I_{EE} = 135$ mA; $T_A = 75°C$, $I_{EE} = 125$ mA.

Note 6: Typical values are at $V_{EE} = -5.2V$, $T_A = 25°C$ and maximum loading.

Note 7: The maximum address access time is guaranteed to be the worst-case bit in the memory using a pseudorandom testing pattern.

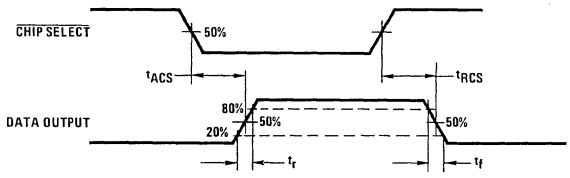
Functional Description

Addressing the DM10470/DM10470A is achieved by means of the 12 address lines, A0–A11. Each of the 2^{12} one-zero combinations of the address lines corresponds to a unique bit location in the memory. The memory array can be expanded to 8192 words without additional decoding, by using the active low Chip Select ($\overline{CS}$) and wire-ORing the unterminated emitter-follower outputs. A 50Ω resistor to −2V (or an equivalent network) is required to provide a low at the output when the device is off. This termination is required for both single device or wire-ORed operation.

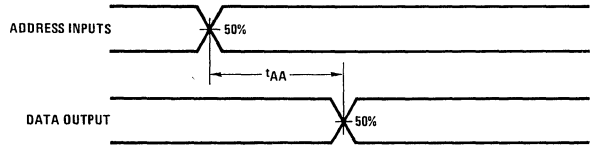
The device is selected with $\overline{CS}$ low and deselected with $\overline{CS}$ high. The operating mode is controlled by the active low Write Enable ($\overline{WE}$). $\overline{WE}$ low causes the data at the Data Input (D_{IN}) to be stored at the selected address. $\overline{WE}$ low also causes the output to be disabled (low due to the 50Ω pull-down resistor). $\overline{WE}$ high causes the data stored at the selected address to be present at the Data Output (D_{OUT}) pin when $\overline{CS}$ is low.

Switching Time Waveforms

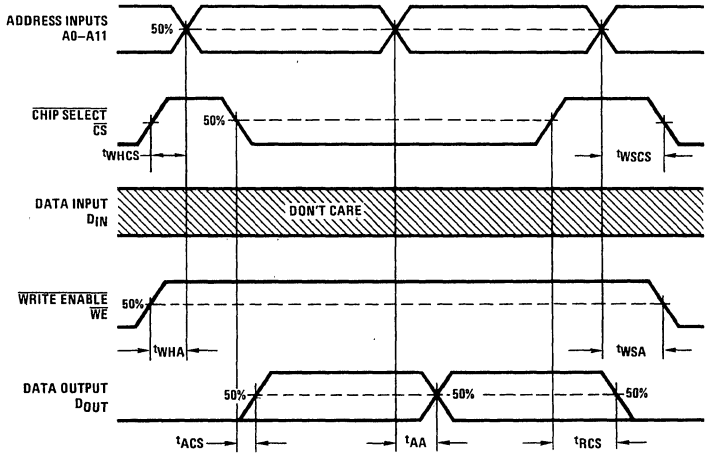
Chip Select Access Time



Address Access Time

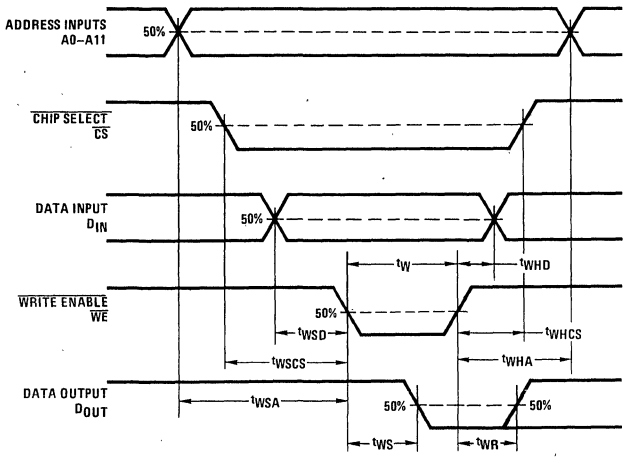


Read Mode



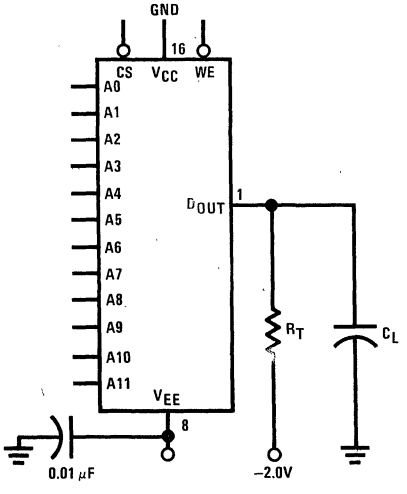
Switching Time Waveforms (Continued)

Write Mode

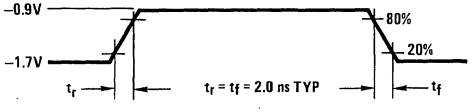


Test Conditions

Loading Conditions



Input Levels



All timing measurements referenced to 50% of input levels
$C_L = 30$ pF including jig and stray capacitance
$R_T = 50\Omega$

National Semiconductor

Bipolar and ECL RAMs
PRELIMINARY

DM10474/DM10474A (1024 x 4) 4096-Bit, 10k ECL RAM

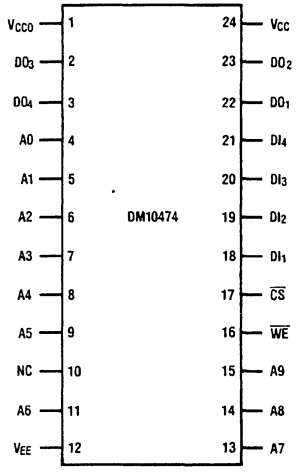
General Description

The DM10474 is a 4096-bit read/write random access memory, organized in the popular 1024 words by 4-bit configuration. The input and output levels are voltage compensated 10k ECL levels. The DM10474A has a maximum access time of 15 ns, and the DM10474 has a maximum access time of 25 ns.

Features

- 1024 words x 4-bit organization
- On chip voltage compensation for improved noise margin
- Fully compatible with industry standard 10k series ECL families
- Address access time: 25 ns max for standard part, 15 ns max for "A" part.
- Chip select access time: 10 ns max for standard part, 6 ns max for "A" part.
- Low power dissipation: −220 mA max for "A" part, −200 mA max for standard.
- Pin compatible with F10474 and MBM10474

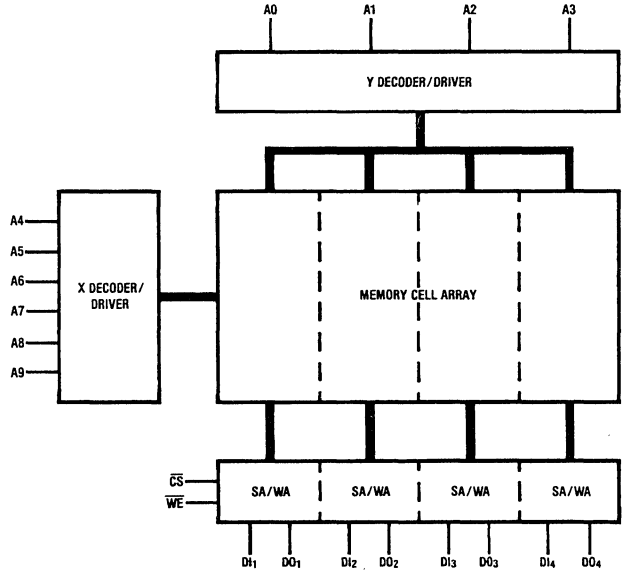
Connection and Block Diagrams



TOP VIEW

TL/L/5164-1

Order Number DM10474J or DM10474AJ
See NS Package J24E



TL/L/5164-2

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	
H	X	X	L	Not Selected
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

H = high voltage level
L = low voltage level
X = don't care

22

DC Electrical Characteristics

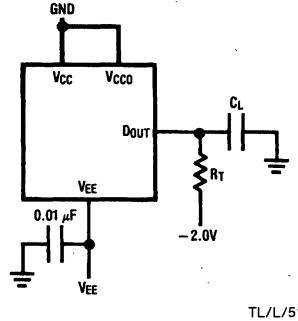
(V_{CC} = 0V, V_{EE} = −5.2V, output load = 50Ω to −2.0V and airflow ≥ 500 LFM unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	0°C 25°C 75°C	−1000 −970 −900		−840 −810 −720	mV
V_{OL}	Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	0°C 25°C 75°C	−1870 −1850 −1830		−1665 −1650 −1625	mV
V_{OHC}	Output High Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	0°C 25°C 75°C	−1020 −980 −920			mV
V_{OLC}	Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	0°C 25°C 75°C			−1645 −1630 −1605	mV
V_{IH}	Input High Voltage (Guaranteed Input Voltage High for All Inputs)	0°C 25°C 75°C	−1145 −1105 −1045		−840 −810 −720	mV
V_{IL}	Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	0°C 25°C 75°C	−1870 −1850 −1830		−1490 −1475 −1450	mV
I_{IH}	Input High Current (V_{IN} = $V_{IH\ max}$)	0° to 75°C			220	μA
I_{IL}	Input Low Current (V_{IN} = $V_{IL\ min}$)	0° to 75°C	−50			μA
I_{IL}	$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	0° to 75°C	0.5		170	μA
I_{EE}	Power Supply Current (All Inputs and Outputs Open)	0° to 75°C	 −200 −220*			mA

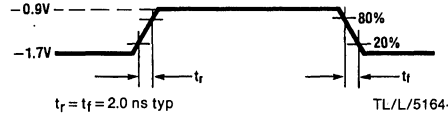
*For the DM10474A,

AC Test Circuit and Switching Time Waveform

(Full guaranteed operating ranges, output load = 50Ω to −2.0V and 30 pF to GND and airflow ≥ 500 LFM unless otherwise noted.)



TL/L/5164-3



$t_r = t_f$ = 2.0 ns typ

TL/L/5164-4

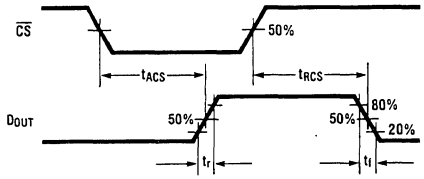
Output Load: RL = 50Ω
C_L = 30 pF
(including jig and stray capacitance)

Note: All timing measurements referenced to 50% input levels.

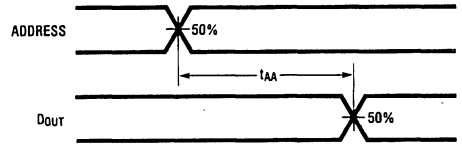
Read Cycle

Symbol	Parameter	DM10474		DM10474A		Units
		Typ	Max	Typ	Max	
t_{AA}	Address Access Time		25		15	ns
t_{ACS}	Chip Select Access Time		10		6	ns
t_{RCS}	Chip Select Recovery Time	10		6		ns

Read Cycle Timing Diagrams



TL/L/5164-5

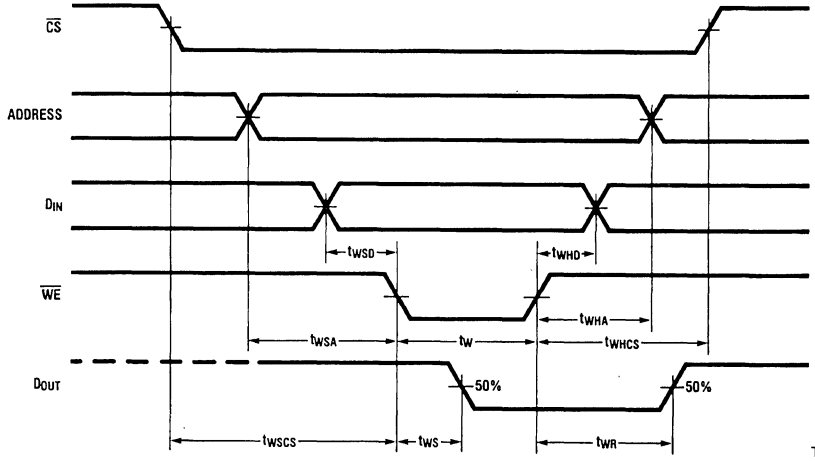


TL/L/5164-6

Write Cycle

Symbol	Parameter	DM10474			DM10474A			Units
		Min	Typ	Max	Min	Typ	Max	
t_W	Write Pulse Width			12			8	ns
t_{WS}	Write Disable Time		4					ns
t_{WR}	Write Recovery Time		4					ns
t_{WSA}	Address Set Up Time		0					ns
t_{WSCS}	Chip Select Set Up Time		0					ns
t_{WSD}	Data Set Up Time		0					ns
t_{WHA}	Address Hold Time		0					ns
t_{WHCS}	Chip Select Hold Time		0					ns
t_{WHD}	Data Hold Time		0					ns

Write Cycle Timing Diagrams



TL/L/5164-7

Rise Time and Fall Time

Symbol	Parameter	DM10474/DM10474A			Units
		Min	Typ	Max	
t_r	Output Rise Time	—	2.5	—	ns
t_f	Output Fall Time	—	2.5	—	ns

Section 23
2900 Family/ Bipolar Microprocessor

23

Introduction

Since its introduction in 1976, the 2900 Family of Bipolar Microprocessor Components has rapidly established itself as the industry standard for bit-slice, microprogrammable system design. National Semiconductor is pleased to have contributed to the success of this family by providing the highest performance components available from any manufacturer. We are firmly committed to continuing this emphasis on performance, since we feel that designers of bipolar systems will continue to demand increased component speed as their system throughput requirements increase. We are not only dedicated to providing components, but also to developing the design techniques that optimize their use in systems. This is evidenced by the expanded Applications section in this book.

To achieve this higher performance, National developed a design technique referred to as SCL[1] and introduced its first 2900 Family product—the IDM2901A—in 1977. This device featured AC characteristics that were 25% faster than anything on the market at that time. In 1978, a speed-selected version of the 2901A—the IDM2901A-1—was introduced. This device further improved performance by an additional 15%. In 1982 an additional 30% performance improvement was provided by the IDM2901A-2, a device that combines the SCL design technique with the latest advances in bipolar LSI processing. All of this has been accomplished without a single compromise with regard to functionality or DC characteristics. In fact, power dissipation in all cases is equal to or less than that of the competing Low Power Schottky devices.

Following its success with the IDM2901, National applied the SCL design technique to the IDM2909A, IDM2910A, IDM2911A, and IDM29705A. These devices also have speed characteristics that are 30%-50% better than those of the competing LS versions.

Not content to simply second source existing 2900 functions, National has also added to the family additional devices that were found to be significantly useful in bit-slice microprocessor design. These include devices from other National product lines — such as the Bipolar Memory and Octal Logic devices found in this book — and certain proprietary functions, such as the 29903 16 x 4 Edge-Triggered Register File.

Even more significantly, National will begin to develop new bit-slices and microsequencers that are architecturally different from other products on the market.

These products, plus other products currently in development, make use of the SCL design philosophy. By using SCL, National has not only set a standard of performance for the 2900 Family that other manufacturers are attempting to duplicate, but also is providing you—the design engineer—with components that allow you to build the highest performance systems possible using bipolar LSI technology.

1. SCL is a design technique that combines the performance advantages of ECL with Low Power Schottky input and output compatibility. For a more detailed description, see the Applications section.

National Semiconductor

2900 Family/
Bipolar Microprocessor

IDM2901A, IDM2901A-1/IDM2901A-2
4-Bit Bipolar Microprocessor

General Description

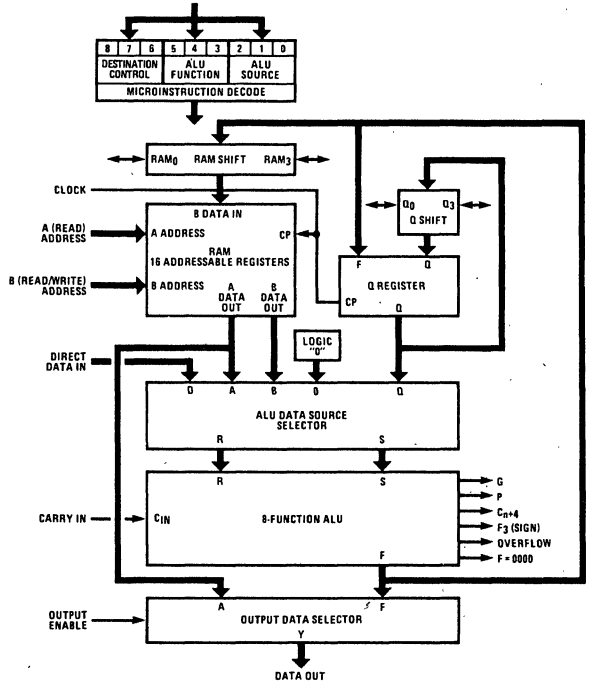
The IDM2901 4-bit bipolar microprocessor slice is a cascadable device designed for use in Central Processing Units, programmable microprocessors, peripheral controllers, and other "high-speed" applications where economy, hardware/software flexibility, and easy expansion are system prerequisities. The building-block architecture and microinstruction format of the IDM2901 permit efficient emulation of most digital-based systems.

As shown in the simplified block diagram, the IDM2901 device consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the required shifting, decoding, and multiplexing circuits. The 9-bit microinstruction word is organized into three groups of three bits each — the first group (bits 0 - 2) selects ALU source operands, the second group (bits 3 - 5) selects the ALU function, and the last group (bits 6 - 8) selects the destination register within the ALU. The slice microprocessor is cascadable with full look-ahead or ripple carry; all outputs are TRI-STATE®, and four status-flag outputs are available. To minimize power consumption and to maximize speed and reliability, the 40-pin LSI chip is fabricated using a National state-of-the-art Low-Power Schottky technology called "SCL".

Features and Benefits

- **Multiple-address architecture** — improves system speed by providing simultaneous yet independent access to two working registers.
- **Multifunction ALU** — performs addition, two subtraction operations, and five logic functions on two source operands.
- **Flexible data-source selection** — for every ALU function, data is selected from five source ports for a total of 203 source operand pairs.
- **Left/right shift independent of ALU** — an arithmetic operation and a left or right shift can be obtained on the same machine cycle.
- **Four status flags** — carry, overflow, zero, and functional sign are available as outputs.
- **Expandable** — Connect any number of IDM2901s together for longer word lengths.
- **Microprogrammable** — three groups of 3 bits each for source operand, ALU function, and destination control.

Block Diagram



Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +6.3 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Operating Range

P/N	Temperature	V_{CC}
IDM2901 JC, NC	T_A = 0°C to +70°C	4.75V to 5.25V
IDM2901 JM, JM/883	T_C = −55°C to +125°C	4.50V to 5.50V
IDM2901A-1 JC, NC	T_A = 0°C to +70°C	4.75V to 5.25V
IDM2901A-1 JM, JM/883	T_C = −55°C to +125°C	4.50V to 5.50V

Standard Screening (Conforms to MIL-STD-883 for Class C parts)

Step	MIL-STD-883 Method	Conditions	Level JC, NC	Level JM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C: 24-hour 150°C	100%	100%
Temperature Cycle	1010	C: −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B: 10,000 G	100%*	100%
Fine Leak	1014	A: 5×10^{-8} atm-cc/cm^3	100%*	100%
Gross Leak	1014	C2: Fluorocarbon	100%*	100%
Electrical Test Subgroups 1 and 7 and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

*Not applicable to IDM2901ANC.

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level JM/883
Burn-In	1015	D: 125°C, 160 hours min	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Group A Subgroups

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum rated temperature
11	Switching	Minimum rated temperature

Electrical Characteristics Over Operating Range IDM2901A/IDM2901A-1

Symbol	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6 mA; $Y_0/Y_1/Y_2/Y_3$	2.4			V
			I_{OH} = −1.0 mA; C_{n+4}	2.4			
			I_{OH} = −800 μA; OVR/P	2.4			
			I_{OH} = −600 μA; F_3	2.4			
			I_{OH} = −600 μA; $RAM_{0,3}/Q_{0,3}$	2.4			
			I_{OH} = −1.6 mA; $\overline{G}$	2.4			

23

Electrical Characteristics (cont'd.)

Symbol	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = min; V_{OH} = 5.5 V, V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output Low Voltage	V_{CC} = min; V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20 mA (Com'l) $Y_0/Y_1/Y_2/Y_3$				0.5	V
			I_{OL} = 16 mA (Mil); $Y_0/Y_1/Y_2/Y_3$				0.5	
			I_{OL} = 16 mA; $\overline{G}/F$ = 0				0.5	
			I_{OL} = 10 mA; C_{n+4}				0.5	
			I_{OL} = 10 mA; OVR/$\overline{P}$				0.5	
			I_{OL} = 8 mA; $F_3/RAM_{0,3}/Q_{0,3}$				0.5	
V_{IH}	Input High Level	Guaranteed input logical high voltage for all inputs			2.0			V
V_{IL}	Input Low Level	Guaranteed input logical low voltage for all inputs					0.8	V
V_I	Input Clamp Voltage	V_{CC} = min; I_{IN} = −18 mA					−1.5	V
I_{IL}	Input Low Current	V_{CC} = max; V_{IN} = 0.5 V	Clock/$\overline{OE}/C_n$				−0.36	mA
			$A_0/A_1/A_2/A_3$				−0.36	
			$B_0/B_1/B_2/B_3$				−0.36	
			$D_0/D_1/D_2/D_3$				−0.36	
			$I_0/I_1/I_2/I_6$				−0.36	
			$I_3/I_4/I_5$				−0.36	
			I_7/I_8				−0.36	
			$RAM_{0,3}/Q_{0,3}$ (Note 4)				−0.36	
I_{IH}	Input High Current	V_{CC} = max; V_{IN} = 2.7 V	Clock/OE				20	μA
			$A_0/A_1/A_2/A_3$				20	
			$B_0/B_1/B_2/B_3$				20	
			$D_0/D_1/D_2/D_3$				20	
			$I_0/I_1/I_2/I_6/I_8$				20	
			$I_3/I_4/I_5/I_7$				20	
			$RAM_{0,3}/Q_{0,3}$ (Note 4)				100	
			C_n				20	
I_I	Input High Current	V_{CC} = max; V_{IN} = 5.5 V					1.0	mA
I_{OZH}, I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = max	$Y_0/Y_1/Y_2/Y_3$	V_O = 2.4 V			50	μA
				V_O = 0.5 V			−50	
			$RAM_{0,3}/Q_{0,3}$	V_O = 2.4 V (Note 4)			100	
				V_O = 0.5 V (Note 4)			−360	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75 V; V_O = 0.5 V	$Y_0/Y_1/Y_2/Y_3/\overline{G}$		−30		−85	mA
			C_{n+4}		−30		−85	
			OVR/$\overline{P}$		−30		−85	
			F_3		−30		−85	
			$RAM_{0,3}/Q_{0,3}$		−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = max	T_A = 25°C			160	245	mA
			JC	T_A = 0°C to +70°C		160	260	mA
				T_A = +70°C		160	220	
			JM	T_C = −55°C to +125°C		160	275	
				T_C = +125°C		160	185	

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5.0 V, 25° C ambient, and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Note 4: These are TRI-STATE outputs internally connected to PNP inputs. Input characteristics are measured with $I_{6,7,8}$ in a state such that the TRI-STATE output is off (high-impedance).

Note 5: "Mil" = IDM2901 JM, JM/883; "Com'l" = IDM2901 JC, NC.

Note 6: Worst case I_{CC} is at minimum temperature.

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +6.3 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Operating Range

P/N	Temperature	V_{CC}
IDM2901A-2 JC, NC	T_A = 0°C to +70°C	4.75V to 5.25V
IDM2901A-2 JM	T_C = −55°C to +125°C	4.50V to 5.50V
IDM2901A-2 JM/883	T_C = −55°C to +125°C	4.50V to 5.50V

Standard Screening (Conforms to MIL-STD-883 for Class C parts)

Step	MIL-STD-883 Method	Conditions	Level JC, NC	Level JM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C: 24-hour 150°C	100%	100%
Temperature Cycle	1010	C: −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B: 10,000 G	100%*	100%
Fine Leak	1014	A: 5×10^{-8} atm-cc/cm^3	100%*	100%
Gross Leak	1014	C2: Fluorocarbon	100%*	100%
Electrical Test Subgroups 1 and 7 and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests				
Subgroup 1	5005	See below for definitions of subgroups	LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

*Not applicable to IDM2901A-2 NC

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level JM/883
Burn-In	1015	D: 125°C, 160 hours min	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Group A Subgroups

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum rated temperature
11	Switching	Minimum rated temperature

Electrical Characteristics Over Operating Range IDM2901A-2

Symbol	Description	Test Conditions (Note 1)		Min	Typ (Note 2)	Max	Units
V_{OH}	Output High Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6 mA; $Y_0/Y_1/Y_2/Y_3$	2.4			V
			I_{OH} = −1.0 mA, C_{n+4}	2.4			
			I_{OH} = −800 μA; OVR/P	2.4			
			I_{OH} = −600 μA; F_3	2.4			
			I_{OH} = −600 μA; $RAM_{0,3}/Q_{0,3}$	2.4			
			I_{OH} = −1.6 mA; $\overline{G}$	2.4			

23

Electrical Characteristics (continued)

Symbol	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = min; V_{OH} = 5.5 V, V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output Low Voltage	V_{CC} = min; V_{IN} = V_{IH} or V_{IL}		I_{OL} = 20 mA (Com'l) $Y_0/Y_1/Y_2/Y_3$			0.5	V
				I_{OL} = 16 mA (Mil); $Y_0/Y_1/Y_2/Y_3$			0.5	
				I_{OL} = 16 mA; $\overline{G}/F$ = 0			0.5	
				I_{OL} = 10 mA; C_{n+4}			0.5	
				I_{OL} = 10 mA; $OVR/\overline{P}$			0.5	
				I_{OL} = 8 mA; $F_3/RAM_{0,3}/Q_{0,3}$			0.5	
V_{IH}	Input High Level	Guaranteed input logical high voltage for all inputs			2.0			V
V_{IL}	Input Low Level	Guaranteed input logical low voltage for all inputs					0.8	V
V_I	Input Clamp Voltage	V_{CC} = min; I_{IN} = −18 mA					−1.5	V
I_{IL}	Input Low Current	V_{CC} = max, V_{IN} = 0.5 V		Clock/$\overline{OE}/C_n$			−0.36	mA
				$A_0/A_1/A_2/A_3$			−0.36	
				$B_0/B_1/B_2/B_3$			−0.36	
				$D_0/D_1/D_2/D_3$			−0.36	
				$I_0/I_1/I_2/I_6$			−0.36	
				$I_3/I_4/I_5$			−0.36	
				I_7/I_8			−0.36	
				$RAM_{0,3}/Q_{0,3}$ (Note 4)			−0.36	
I_{IH}	Input High Current	V_{CC} = max; V_{IN} = 2.7 V		Clock/OE			20	μA
				$A_0/A_1/A_2/A_3$			20	
				$B_0/B_1/B_2/B_3$			20	
				$D_0/D_1/D_2/D_3$			20	
				$I_0/I_1/I_2/I_6/I_8$			20	
				$I_3/I_4/I_5/I_7$			20	
				$RAM_{0,3}/Q_{0,3}$ (Note 4)			100	
				C_n			20	
I_I	Input High Current	V_{CC} = max; V_{IN} = 5.5 V					1.0	mA
I_{OZH}, I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = max	$Y_0/Y_1/Y_2/Y_3$	V_O = 2.4 V			50	μA
				V_O = 0.5 V			−50	
			$RAM_{0,3}/Q_{0,3}$	V_O = 2.4 V (Note 4)			100	
				V_O = 0.5 V (Note 4)			−360	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = 5.75 V, V_O = 0.5 V		$Y_0/Y_1/Y_2/Y_3/\overline{G}$	−30		−85	mA
				C_{n+4}	−30		−85	
				$OVR/\overline{P}$	−30		−85	
				F_3	−30		−85	
				$RAM_{0,3}/Q_{0,3}$	−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = max		T_A = 25°C		160	250	mA
			JC	T_A = 0°C to +70°C		160	265	
			JM	T_C = −55°C to +125°C		160	280	
				T_C = +125°C		160	190	

Note 1: For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5.0 V, 25°C ambient, and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Note 4: These are TRI-STATE outputs internally connected to PNP inputs. Input characteristics are measured with $I_{6,7,8}$ in a state such that the TRI-STATE output is off (high-impedance).

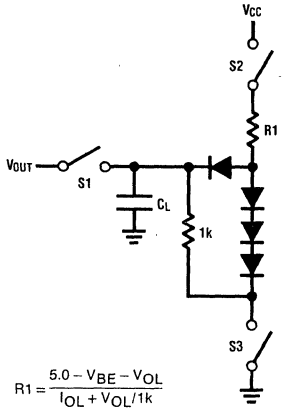
Note 5: "Mil" = IDM2901A-2 JM, JM/883; "Com'l" = IDM2901A-2 JC, NC.

Note 6: Worst case I_{CC} is at minimum temperature.

Figure 1. IDM2901 Microprocessor, Detailed Block Diagram

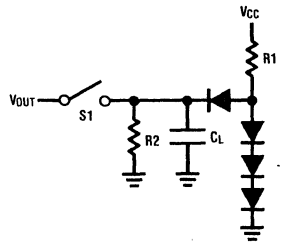
Test Output Load Configurations for IDM2901A, A-1, A-2

A. Three-State Outputs



$$R1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1k}$$

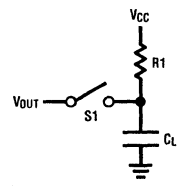
B. Normal Outputs



$$R2 = \frac{2.4V}{I_{OH}}$$

$$R1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R2}$$

C. Open-Collector Outputs



$$R1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Note 1: $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.

Note 2: S1, S2, S3 are closed during function tests and all AC tests except output enable tests.

Note 3: S1 and S3 are closed while S2 is open for t_{PZH} test.
S1 and S2 are closed while S3 is open for t_{PZL} test.

Note 4: $C_L = 5.0$ pF for output disable tests.

TESTING CONSIDERATIONS

Incoming test procedures on this device should be carefully planned, taking into account the high complexity and power levels of the part. The following notes may be useful.

1. Insure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may start to oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5 ns–8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by 100s of millivolts momentarily.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins and they may not actually reach V_{IL} or V_{IH} until the noise has settled. National recommends using $V_{IL} \leq 0.4V$ and $V_{IH} \geq 2.4V$ for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.

Test Output Loads for IDM2901A, A-1, A-2

Pin #	Pin Label	Test Circuit	R1	R2
3	RAM_3	A	560	1k
5	RAM_0	A	560	1k
7	F = 0	C	270	—
13	Q_3	A	560	1k
18	Q_0	A	560	1k
28	F_3	B	620	3.9k
29	G	B	220	1.5k
30	C_{n+4}	B	360	2.4k
31	OVR	B	470	3k
32	P	B	470	3k
33–36	Y_{0-3}	A	220	1k

Architecture

Figure 1 shows a detailed block diagram of the IDM2901. Observe that all data paths are 4 bits wide; however, the 4-bit slice can be cascaded to the number of bits required for a particular application. Although all parts of the bipolar device are important, the two key elements are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Any one of the 16 words in RAM can be read from the A-port (A_3-A_0) or the B-port (B_3-B_0); the selected word for the A-port is determined by the 4-bit A-address field, whereas the B-address field controls the output of the B-port. If the two address codes are identical, the same file data appears simultaneously at both output ports (A and B).

When enabled by RAM EN, new data is written into the file "word" defined by the B-address field; the write function is implemented when the clock input is low.

Each bit of data to be written is input via a 3-input multiplexer; this scheme permits shifting up one bit position (from LSB towards MSB), shifting down one bit position (from MSB towards LSB), or not shifting at all. A similar scheme is used when data is written into the "Q" register.

Each of the A and B data ports drives an associated 4-bit latch. These latches hold the RAM data while the clock input is low; consequently, any possibility of race conditions when writing new data is eliminated.

The high-speed ALU can perform three binary arithmetic and five logic operations on the two 4-bit input words (R_3-R_0 and S_3-S_0). The R-input field is driven from a 2-input multiplexer, whereas the S-input field is driven by a 3-input multiplexer. Both the R- and S-multiplexers have an inhibit capability, where no data is passed – this is equivalent to a "zero" source operand. Referring to figure 1, observe that the A-port output of the RAM and the 4-bit direct-data inputs (D_3-D_0) are connected to the R-input multiplexers; the S-input multiplexer has three inputs – one from the A-port of RAM, one from the B-port of RAM, and one from the Q-register.

With the foregoing input-multiplexer scheme, the inputs (A, B, D, Q, and "Zero"), when taken in pairs, provide any one of ten source operands for the ALU – AB, AD, AQ, A0, BD, BQ, B0, DQ, D0, and Q0. When the A and B address fields for RAM are identical, it is clear that certain combinations (AD/BD, AQ/BQ, and A0/B0) are redundant; that is, the identical function is implemented for either operand. Only seven of the combinations are completely nonredundant. Eight of the ten combinations (source operands) are implemented by the IDM2901A microprocessor. The ALU source operands are selected by three microinstruction inputs – I_0, I_1, and I_2. These inputs are defined in figure 2. Each of the preceding D and Q operands provides an essential function. The D input (direct-data) is used to load the working registers inside the 2901 device; also, this input source can be used to modify data files within the ALU. The Q-register is an internal 4-bit data source that is well suited for a multiply/divide operation; however, for some applications, it can be used as a data-holding register or as an accumulator.

The ALU is a high-speed arithmetic/logic operator that is capable of performing three binary arithmetic functions and five logic functions. Three microinstruction inputs (I_3, I_4, and I_5) are used to select one of the eight functions; these inputs, along with their octal codes, are defined in figure 3.

Micro Code				ALU Source Operands	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	0	Q
L	H	H	3	0	B
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	0

Figure 2. ALU Source Operand Control

Micro Code				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S – R
L	H	L	2	R Minus S	R – S
L	H	H	3	R OR S	R ∨ S
H	L	L	4	R AND S	R ∧ S
H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
H	H	L	6	R EX-OR S	R ∀ S
H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control

Normally, the look-ahead carry mode is used when cascading the ALUs of several microprocessor devices. The carry generate ($\overline{G}$) and carry propagate ($\overline{P}$) outputs are suitable for use in a carry-look-ahead generator. A carry-out (C_{n+4}) is also generated and is available for use as the carry flag in a status register or as a ripple-carry output. Both carry-in (C_n) and carry-out (C_{n+4}) are active-high signals. Three other status-oriented outputs are available from the ALU; these are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU, and, without enabling the TRI-STATE outputs, it can be used to determine positive or negative results. When enabled, the logic level of F_3 is identical to that of sign bit Y_3. The F = 0 output is used for zero detect; F = 0 is high when all F outputs are low. The F = 0 output is of the open-collector type and can be wire ORed between microprocessor slices. The overflow (OVR) output is used to flag arithmetic operations that exceed the available twos-complement number range. When an overflow exists (C_{n+3} and C_{n+4} are of opposite polarity), the OVR output is high.

Outputs from the ALU can be stored in the register file or the Q register, or can be transmitted to the outside world. Eight possible destination codes are defined by microinstruction inputs I_6, I_7, and I_8; the various destination control codes are shown in figure 4. The 4-bit data field (Y_3-Y_0) is a TRI-STATE output that can be directly bus organized. The Y outputs are enabled by $\overline{OE}$; when this control signal is high, the Y-outputs are TRI-STATEd. A 2-input multiplexer is also used at the Y-output port to select either the A port of RAM or the F output of the ALU; this selection is controlled by the previously described microinstruction inputs (I_6, I_7, and I_8).

As previously described, the RAM inputs (register file) are driven by a 3-input multiplexer. Thus, outputs from the ALU can be entered nonshifted, shifted up (towards MSB) one position (x 2), or shifted down (towards LSB) one position (÷ 2). The shifter is equipped with two ports – RAM_0 and RAM_3; both ports consist of a TRI-STATE buffer-driver, each of which supplies one input to the foregoing multiplexer. In the shift-up (x 2) mode, the RAM_3 output driver and the RAM_0 multiplexer input are enabled, whereas in the shift-down (÷ 2) mode, the RAM_0 output driver and RAM_3 multiplexer input are enabled; in the no-shift mode, both drivers are TRI-STATE and neither multiplexer input is enabled. The shifter is controlled by the I_6, I_7, and I_8 microinstruction inputs.

The Q register likewise is driven from a 3-input multiplexer and the Q shifter is equipped with two input/output ports – Q_0 and Q_3. Operation of these two ports is similar to that of the RAM shifter, and the ports are controlled by I_6, I_7, and I_8. In the shift-up or shift-down modes, the Q register is shifted in a specified direction with the input/output terminals of the register being an input (for a shift-up) or an output (for a shift-down). In the no-shift mode, the multiplexer may enter the ALU data into the Q register; in this case, input/output lines of the register are TRI-STATE.

The clock input shown in figure 1 controls the RAM, the A and B latches, and the Q register. When the clock input is high, the A and B latches are open and data from the RAM outputs is allowed to pass through to the ALU or "Y" outputs. When the clock input is low, both latches are closed and the last data entered is retained. When the clock input is low and if the input control code (I_6, I_7, and I_8) has enabled a file-write operation, new data, as defined by the 4-bit B-address field, is written into the RAM file. When enabled, data is clocked into the Q register on the low-to-high transition of the clock pulse.

Source Operands and ALU Functions

Any one of eight source operand pairs can be selected by instruction inputs I_0, I_1, and I_2 for use by the ALU; instruction inputs I_3, I_4, and I_5 then control function selection for the ALU – five logic and three arithmetic functions. In the arithmetic mode, the carry input (C_n) also affects the ALU functions; the carry input has no effect on the "F" result in the logic mode. These control parameters (I_6-I_0 and C_n) are summarized in figure 5 to completely define the ALU/source operand functions.

The ALU functions can also be examined on a task basis: that is, add, subtract, AND, OR, and so on. Again, in the arithmetic mode, the carry input will affect the result, whereas in the logic mode it will not. Figures 6 and 7, respectively, define the various logic and arithmetic functions of the ALU; both carry states ($C_n = 0$/$C_n = 1$) are defined in the function matrices.

Figure 4. ALU Destination Control

Micro Code				RAM Function		Q-Reg. Function		Y Output	RAM Shifter		Q Shifter	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	None	None	F → Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F → B	X	None	A	X	X	X	X
L	H	H	3	None	F → B	X	None	F	X	X	X	X
H	L	L	4	Down	F/2 → B	Down	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	Down	F/2 → B	X	None	F	F_0	IN_3	Q_0	X
H	H	L	6	Up	2F → B	Up	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	Up	2F → B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a TRI-STATE output which is in the high-impedance state.
B = Register Addressed by B inputs.
Up is toward MSB, Down is toward LSB.

Figure 5. Source Operand and ALU Function Matrix

Octal $I_{5,4,3}$	$I_{2,1,0}$ Octal / ALU Source / ALU Function	0 A, Q	1 A, B	2 0, Q	3 0, B	4 0, A	5 D, A	6 D, Q	7 D, 0
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A V Q	A V B	Q	B	A	D V A	D V Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; − = Minus; V = OR, ∧ = AND; ∀ = EX-OR.

Figure 6. ALU Logic Mode Functions (C_n Irrelevant)

Octal $I_{5,4,3}/I_{2,1,0}$	Group	Function
40	AND	A ∧ Q
41		A ∧ B
45		D ∧ A
46		D ∧ Q
30	OR	A V Q
31		A V B
35		D V A
36		D V Q
60	EX-OR	A ∀ Q
61		A ∀ B
65		D ∀ A
66		D ∀ Q
70	EX-NOR	$\overline{A \forall Q}$
71		$\overline{A \forall B}$
75		$\overline{D \forall A}$
76		$\overline{D \forall Q}$
72	INVERT	$\overline{Q}$
73		$\overline{B}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	"ZERO"	0
43		0
44		0
47		0
50	MASK	$\overline{A}$ ∧ Q
51		$\overline{A}$ ∧ B
55		$\overline{D}$ ∧ A
56		$\overline{D}$ ∧ Q

Figure 7. ALU Arithmetic Mode Functions

Octal $I_{5,4,3}/I_{2,1,0}$	C_n = 0 (Low) Group	C_n = 0 (Low) Function	C_n = 1 (High) Group	C_n = 1 (High) Function
00	ADD	A + Q	ADD plus one	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q − 1	PASS	Q
13		B − 1		B
14		A − 1		A
27		D − 1		D
22	1s Comp	− Q − 1	2s Comp (Negate)	− Q
23		− B − 1		− B
24		− A − 1		− A
17		− D − 1		− D
10	Subtract (1s Comp)	Q − A − 1	Subtract (2s Comp)	Q − A
11		B − A − 1		B − A
15		A − D − 1		A − D
16		Q − D − 1		Q − D
20		A − Q − 1		A − Q
21		A − B − 1		A − B
25		D − A − 1		D − A
26		D − Q − 1		D − Q

Pinout Descriptions of IDM2901

Pin functions for the IDM2901 4-bit slice microprocessor are as follows:

$A_3 - A_0$ 4-bit address field used to select one of the file registers whose contents are displayed through the A port of RAM.

$B_3 - B_0$ 4-bit address field used to select one of the file registers whose contents are displayed through the B port of RAM. When the clock is low, new data can be written into the selected B-port register.

$I_8 - I_0$ Nine instruction-control lines — $I_0/I_1/I_2$ determine data sources of ALU, $I_3/I_4/I_5$ select ALU function, and $I_6/I_7/I_8$ select data inputs for the Q register or the register file.

Q_3/RAM_3 Serves as shift data input/output lines for the most significant bit (MSB) of Q register (Q_3) and the register stack (RAM_3). These lines are TRI-STATE outputs that connect to TTL inputs within the IDM2901 device. When the destination code, as defined by $I_6/I_7/I_8$, indicates an up-shift (octal 6 or 7), the TRI-STATE outputs are enabled; accordingly, the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, these output lines are TRI-STATE or serve as LS-TTL inputs. When a down-shift is indicated by the destination code, the Q_3 and RAM_3 pins are used as data inputs to the MSB of the Q register or RAM.

Q_0/RAM_0 These shift lines are similar to Q_3 and RAM_3, except they operate on the least significant bit (LSB) of the Q register and RAM. To transfer data for up- and down-shifts of the Q register and the ALU, the Q_0 and RAM_0 pins are connected, respectively, to the next less-significant device (Q_n and RAM_n) in the cascaded chain.

$D_3 - D_0$ A 4-bit data field that can be selected as a source of external data for ALU — D_0 is the least significant bit.

$Y_3 - Y_0$ 4-bit output data of IDM2901. These lines are TRI-STATE; when enabled, they provide either the ALU output or data from the A port of the register file — the selected source is determined by the destination code, as defined by I_6, I_7, and I_8.

$\overline{OE}$ When the Output Enable ($\overline{OE}$) signal is high, the Y outputs are inactive; when the signal is active-low, the active high or low outputs are enabled.

$\overline{P}/\overline{G}$ Carry generate and propagate outputs — see figure 8 for logic equations.

OVR The overflow flag corresponds to the exclusive-OR of the carry-in and carry-out of the MSB of the ALU. When set high, it indicates that the result of an arithmetic twos-complement operation has overflowed into the sign bit — see figure 8 for the logic equation.

F = 0 An open-collector output that goes high if all data lines ($F_3 - F_0$) are low, that is, the result of an ALU operation is zero.

C_n Carry-in to ALU.

C_{n+4} Carry-out of ALU — see figure 8 for logic equations.

CP Clock input. Outputs of Q register and file are clocked on low-to-high transition; the low interval of the clock input corresponds to the "write enable" period of the 16-by-4 RAM, that is, the "master" latches of the register file. When the clock is low, the output latches store the data previously held at the RAM outputs; thus, synchronous master-slave operation of the register file is permitted.

F_3 Most significant (sign) bit output of the ALU.

Logic Functions for G, P, Cn+4, and OVR

When the IDM2901 is in the add or the subtract mode, four signals (G, P, C_{n+4}, and OVR) are available to indicate carry and overflow conditions. Based on the eight ALU functions, logic equations for these signal are shown in figure 8. (Note: The "R" and "S" inputs are selected according to figure 2.)

Definitions (+ = OR):

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

$I_{5,4,3}$	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions.			
2	R − S	Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions.			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$ ∧ S	LOW	Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions.		
6	R ∀ S	Same as R ∀ S equations, but substitute $\overline{R_i}$ for R_i in definitions.			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$	See Note 1	See Note 2

Note 1: $\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0(G_0 + \overline{C_n})}$ **Note 2:** $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$

Figure 8. Logic Equations for Flag Outputs

Guaranteed Operating Conditions Over Temperature and Voltage for IDM2901A

When operated in a system, the timing requirements for the IDM2901 are defined in tables 1, 2, and 3. Table 1 provides clock characteristics of the IDM2901, table 2 gives the combinational delay times from input to output, and table 3 specifies setup and hold times. If used according to the specified delay and setup times, the device is guaranteed to function properly over the entire operating range. Table 3 defines the time prior to the end of the cycle (low-to-high transition of clock pulse) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Table 1. Cycle Time and Clock Characteristics

Time	IDM2901A	
	JC, NC	JM, JM/883
Read-Modify-Write Cycle (time from selection of A,B registers to end of cycle)	60 ns	75 ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	16 MHz	16 MHz
Minimum Clock Low Time	30 ns	30 ns
Minimum Clock High Time	30 ns	30 ns
Minimum Clock Period	60 ns	75 ns

Table 2. Maximum Combinational Propagation Delays (all in ns; $C_L \leq 50$ pF)

	Commercial IDM2901A JC, NC (0°C to +70°C; 5V ± 5%)								Military IDM2901A JM, JM/883 (−55°C to +125°C; 5V ± 10%)							
To Output / From Input	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3
A, B	65	65	65	60	70	65	70	–	80	80	80	65	85	80	80	–
D (arithmetic mode)	40	40	40	35	55	45	50	–	45	45	45	40	65	55	60	–
D (I = X37)	40	40	–	–	55	–	50	–	45	45	–	–	60	–	60	–
C_n	30	30	20	–	40	30	35	–	35	35	25	–	50	35	45	–
$I_{2,1,0}$	55	50	50	45	60	50	60	–	60	60	55	50	75	60	75	–
$I_{5,4,3}$	50	50	50	45	55	50	50	–	60	60	60	55	70	60	60	–
$I_{8,7,6}$	30	–	–	–	–	–	30	30	35	–	–	–	–	–	35	35
$\overline{OE}$ Enable/Disable	30/25	–	–	–	–	–	–	–	40/25	–	–	–	–	–	–	–
A Bypassing ALU (I = 2xx)	40	–	–	–	–	–	–	–	50	–	–	–	–	–	–	–
Clock ↓ (Note 6)	60	60	60	50	60	55	60	30	65	65	65	55	75	70	75	35

Table 3. Maximum Setup and Hold Times (all in ns) — Note 1

		Commercial IDM2901A JC, NC (0°C to +70°C, 5V ± 5%)		Military IDM2901A JM, JM/883 (−55°C to +125°C, 5V ± 10%)	
From Input	Notes	Setup Time	Hold Time	Setup Time	Hold Time
A, B Source	2, 3, 4, 5	60, $t_{pw}L$ + 20	0	75, $t_{pw}L$ + 25	0
B Destination	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
D (arithmetic mode)		40	0	50	0
D (I = X37)	5	40	0	50	0
C_n		35	0	40	0
$I_{2,1,0}$		45	0	55	0
$I_{5,4,3}$		45	0	55	0
$I_{8,7,6}$	4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
$RAM_{0,3}/Q_{0,3}$		20	0	25	0

Note 1: See figures 9 and 10.

Note 2: If the B address is used as a source operand, allow for the "A, B Source" setup time; if it is used only for the destination address, use the "B Destination" setup time.

Note 3: Where two numbers are shown, both must be met.

Note 4: "$t_{pw}L$" is the clock low time.

Note 5: DVO is the fastest way to load the RAM from the D inputs. This function is obtained with I = X37.

Note 6: Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

Guaranteed Operating Conditions Over Temperature and Voltage for IDM2901A-1

When operated in a system, the timing requirements for the IDM2901A-1 are defined in tables 1, 2, and 3. Table 1 provides clock characteristics of the IDM2901A-1, table 2 gives the combinational delay times from input to output, and table 3 specifies setup and hold times. If used according to the specified delay and setup times, the device is guaranteed to function properly over the entire operating range. Table 3 defines the time prior to the end of the cycle (low-to-high transition of clock pulse) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Table 1. Cycle Time and Clock Characteristics

Time	IDM2901A-1	
	JC, NC	JM, JM/883
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	60 ns	75 ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	16 MHz	16 MHz
Minimum Clock Low Time	30 ns	30 ns
Minimum Clock High Time	30 ns	30 ns
Minimum Clock Period	60 ns	75 ns

Table 2. Maximum Combinational Propagation Delays (all in ns; C_L < 50 pF)

From Input \ To Output	Commercial IDM2901A-1 JC, NC (0°C to +70°C; 5V ± 5%)								Military IDM2901A-1 JM, JM/883 (−55°C to +125°C; 5V ± 10%)							
	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3
A, B	50	50	50	45	55	60	55	–	60	60	60	60	65	75	65	–
D (arithmetic mode)	32	32	32	30	32	40	35	–	40	40	40	40	40	50	45	–
D (I = X37)	32	32	–	–	32	–	35	–	40	40	–	–	40	–	45	–
C_n	25	22	16	–	30	25	35	–	32	30	20	–	40	35	45	–
$I_{2,1,0}$	40	35	35	30	40	45	45	–	50	45	45	40	50	55	55	–
$I_{5,4,3}$	35	35	35	32	40	45	45	–	45	45	45	40	50	55	55	–
$I_{8,7,6}$	25	–	–	–	–	–	30	30	35	–	–	–	–	–	35	35
$\overline{OE}$ Enable/Disable	20/20	–	–	–	–	–	–	–	25/25	–	–	–	–	–	–	–
A Bypassing ALU (I = 2xx)	40	–	–	–	–	–	–	–	50	–	–	–	–	–	–	–
Clock ↓ (Note 6)	50	45	45	40	50	55	55	30	60	55	55	50	60	65	65	35

Table 3. Maximum Setup and Hold Times (all in ns) – Note 1

From Input	Notes	Commercial IDM2901A-1 JC, NC (0°C to +70°C, 5V ± 5%)		Military IDM2901A-1 JM, JM/883 (−55°C to +125°C, 5V ± 10%)	
		Setup Time	Hold Time	Setup Time	Hold Time
A, B Source	2, 3, 4, 5	60, $t_{pw}L$ + 20	0	75, $t_{pw}L$ + 25	0
B Destination	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
D (arithmetic mode)		40	0	50	0
D (I = X37)	5	40	0	50	0
C_n		35	0	40	0
$I_{2,1,0}$		45	0	55	0
$I_{5,4,3}$		45	0	55	0
$I_{8,7,6}$	4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
$RAM_{0,3}/Q_{0,3}$		15/10	0	25/15	0

Note 1: See figures 9 and 10.

Note 2: If the B address is used as a source operand, allow for the "A, B Source" setup time; if it is used only for the destination address, use the "B Destination" setup time.

Note 3: Where two numbers are shown, both must be met.

Note 4: "$t_{pw}L$" is the clock low time.

Note 5: DVO is the fastest way to load the RAM from the D inputs. This function is obtained with I = X37.

Note 6: Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

Guaranteed Operating Conditions Over Temperature and Voltage for IDM2901A-2

When operated in a system, the timing requirements for the IDM2901A-2 are defined in tables 1, 2, and 3. Table 1 provides clock characteristics of the IDM2901A-2, table 2 gives the combinational delay times from input to output, and table 3 specifies setup and hold times. If used according to the specified delay and setup times, the device is guaranteed to function properly over the entire operating range. Table 3 defines the time prior to the end of the cycle (low-to-high transition of clock pulse) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

TABLE 1. Cycle Time and Clock Characteristics

Time	IDM2901A-2	
	JC, NC	JM, JM/883
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	50 ns	65 ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	20 MHz	16 MHz
Minimum Clock Low Time	25 ns	30 ns
Minimum Clock High Time	25 ns	30 ns
Minimum Clock Period	50 ns	65 ns

TABLE 2. Maximum Combinational Propagation Delays (all in ns; C_L 50pF)

	Commercial IDM2901A-2 JC, NC (0°C to +70°C; 5V ± 5%)								Military IDM2901A-2 JM, JM/883 (−55°C to +125°C; 5V ± 10%)							
to Output / from Input	Y	F_3	C_{n+4}	G/P	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3	Y	F_3	C_{n+4}	G/P	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3
A, B	44	44	44	35	44	45	40	–	55	50	50	45	55	55	50	–
D (arithmetic mode)	28	28	28	25	31	34	30	–	37	37	37	34	40	40	37	–
D (I = X37)	28	28	–	–	31	–	30	–	37	37	–	–	40	–	37	–
C_n	25	22	16	–	25	25	25	–	30	25	19	–	33	30	30	–
$I_{2,1,0}$	35	35	35	28	35	39	35	–	45	45	45	45	45	45	40	–
$I_{5,4,3}$	35	35	35	32	35	35	35	–	45	40	40	40	45	45	40	–
$I_{8,7,6}$	25	–	–	–	–	–	30	30	30	–	–	–	–	–	35	35
OE Enable/Disable	20/20	–	–	–	–	–	–	–	25/25	–	–	–	–	–	–	–
A Bypassing ALU (I = 2xx)	35	–	–	–	–	–	–	–	45	–	–	–	–	–	–	–
Clock (Note 6)	40	40	40	40	40	45	45	28	50	45	45	40	55	50	50	30

TABLE 3. Maximum Setup and Hold Times (all in ns) – Note 1

		Commercial IDM2901A-2 JC, NC (0°C to +70°C, 5V ± 5%)		Military IDM2901A-2 JM, JM/883 (−55°C to +125°C, 5V ± 10%)	
From Input	Notes	Setup Time	Hold Time	Setup Time	Hold Time
A, B Source	2, 3, 4, 5	50, $t_{pw}L$ + 20	0	60, $t_{pw}L$ + 20	0
B Destination	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
D (arithmetic mode)		35	0	40	0
D (I = X37)	5	35	0	40	0
C_n		26	0	30	0
$I_{2,1,0}$		35	0	45	0
$I_{5,4,3}$		30	0	45	0
$I_{8,7,6}$	4	$t_{pw}L$ + 10	0	$t_{pw}L$ + 14	0
$RAM_{0,3}/Q_{0,3}$		12/10	0	15/15	0

Note 1: See figures 9 and 10.

Note 2: If the B address is used as a source operand, allow for the "A, B Source" setup time; if it is used only for the destination address, use the "B Destination" setup time.

Note 3: Where two numbers are shown, both must be met.

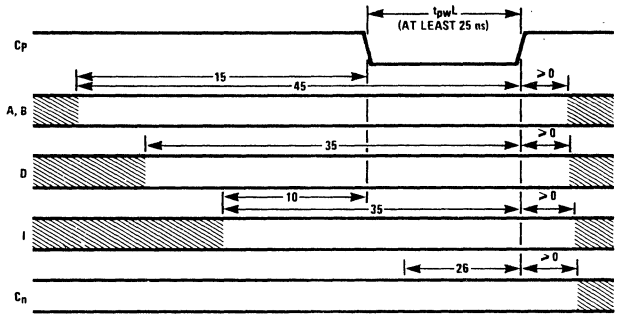
Note 4: "$t_{pw}L$" is the clock low time.

Note 5: DVO is the fastest way to load the RAM from the D inputs. This function is obtained with I = X37.

Note 6: Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

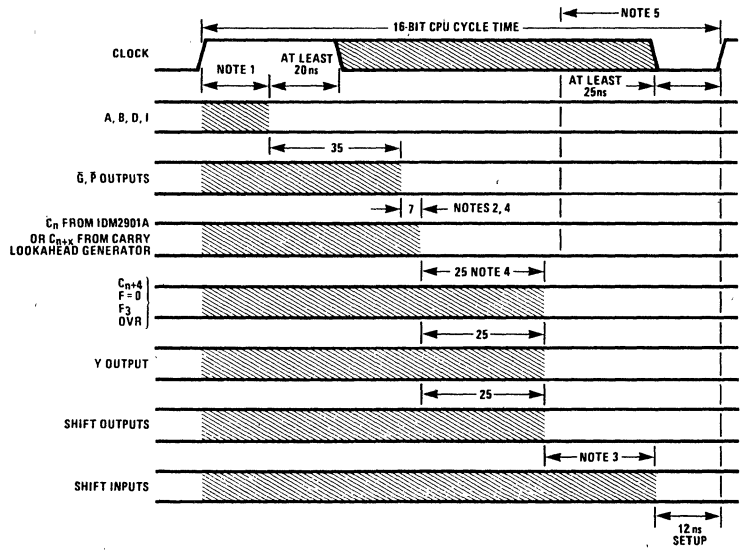
Set-Up and Hold Times (mimimum cycles from each input)

Setup and hold times are defined relative to the low-to-high transition of the clock pulse. At all times, inputs must be stable from the setup time prior to the clock until the hold time after the clock – observe that all hold times are "zero." The set-up times allow sufficient time to perform the correct operation on the correct data so that the correct ALU data can be written into the correct register.



Note: Numbers shown are minimum data-stable times in nanoseconds for commercial product – see table 3 for detailed information.

Figure 9. Setup Times for Input Parameters of IDM2901



Notes:

1. This delay is the max t_{pd} of the register containing A, B, D, and I.
2. 7 ns for look-ahead carry. For ripple carry over 16 bits use 2 x ($C_n \rightarrow C_{n+4}$), or 24 ns.
3. This is the delay associated with the multiplexer between the shift outputs and the shift inputs on the IDM2901.
4. Not applicable for logic operations.
5. Clock rising edge may occur here if add and shift do not occur on same cycle.

Figure 10. Switching Waveforms for 16-Bit System Assuming A, B, D, and I are Driven from Registers with the Same Propagation Delay and Clocked by the IDM2901. (These are maximum times in nanoseconds using commercial product specifications.)

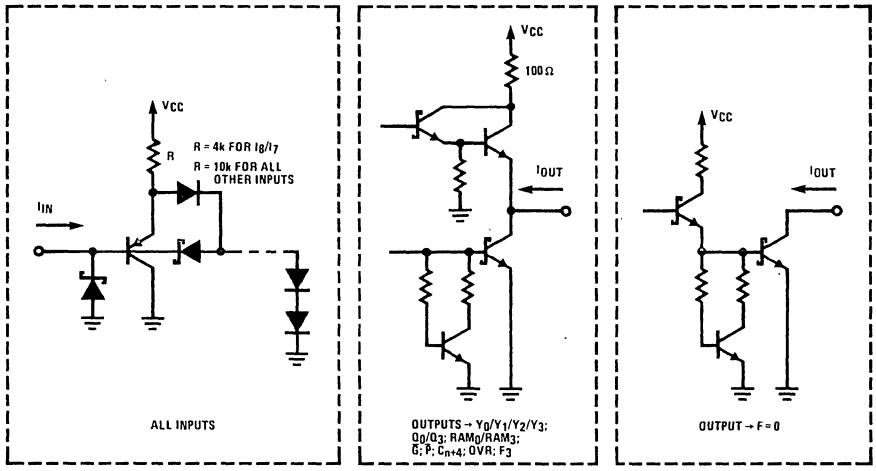


Figure 11. Equivalent Input/Output Current Interface Conditions for IDM2901

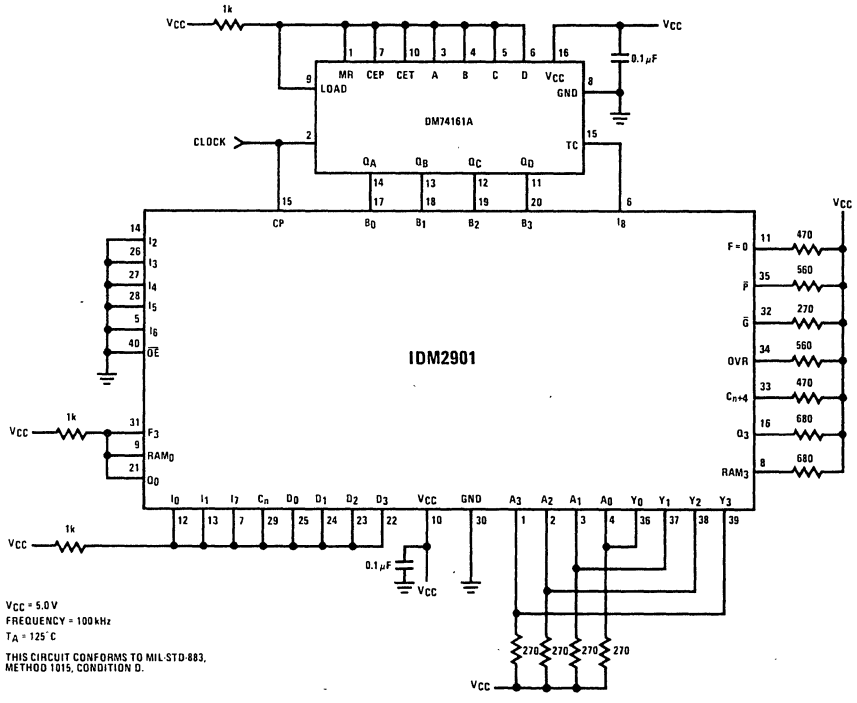
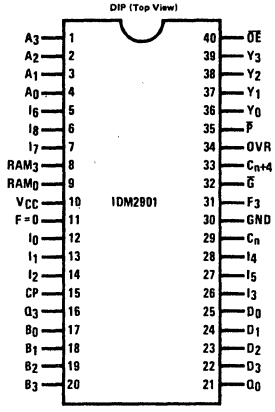


Figure 12. Burn-In Circuit for IDM2901

Connection Diagram



NOTE: PIN 1 IS MARKED FOR ORIENTATION.

Ordering Information

Package Type	Package Number	Temperature Range	Order Number
Molded DIP	N40A	0°C to +70°C	IDM2901ANC/IDM2901A-1NC/IDM2901A-2NC
Hermetic DIP	D40C	0°C to +70°C	IDM2901AJC/IDM2901A-1JC/IDM2901A-2JC
Hermetic DIP	D40C	−55°C to +125°C	IDM2901AJM/IDM2901A-1JM/IDM2901A-2JM
Hermetic DIP	D40C	−55°C to +125°C	IDM2901AJM/883/IDM2901A-1JM/883/IDM2901A-2JM/883

National Semiconductor

2900 Family/
Bipolar Microprocessor

IDM2902 Look-Ahead Carry Generator

General Description

This circuit is a high-speed, look-ahead carry generator, capable of anticipating a carry across four binary adders or groups of adders. It is cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the IDM2901A arithmetic logic units, this generator provides high-speed carry look-ahead capability for any word length. The IDM2902 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALUs are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the IDM2901A data sheet, are also applicable to and compatible with the look-ahead generator. Positive logic equations for the 2902 parts are:

$$C_{n+x} = G_0 + P_0 C_n$$

$$C_{n+y} = G_1 + P_1 G_0 + P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n$$

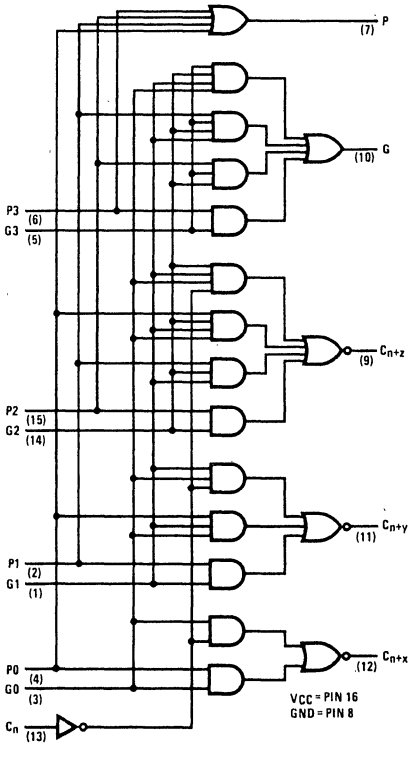
$$G = G_3 (P_3 + G_2)(P_3 + P_2 + G_1)(P_3 + P_2 + P_1 + G_0)$$

$$P = P_3 P_2 P_1 P_0$$

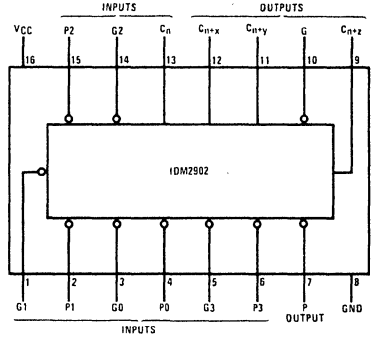
Features and Benefits

Type	Typical Propagation Delay Time	Typical Power Dissipation
IDM2902	7 ns	260 mW

Logic and Connection Diagram



Connection Diagram



Pin Designations

Designation	Pin Nos.	Function
G_0, G_1, G_2, G_3	3, 1, 14, 5	Active Low Carry Generate Inputs
P_0, P_1, P_2, P_3	4, 2, 15, 6	Active Low Carry Propagate Inputs
C_n	13	Carry Input
$C_{n+x}, C_{n+y}, C_{n+z}$	12, 11, 9	Carry Outputs
G	10	Active Low Carry Generate Output
P	7	Active Low Carry Propagate Output
V_{CC}	16	Supply Voltage
GND	8	Ground

Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +6.3V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5V
DC Output Current, into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Operating Range

P/N	Ambient Temperature	V_{CC}
IDM2902JC, NC	0°C to +70°C	4.75V to 5.25V
IDM2902JM, JM/883	−55°C to +125°C	4.50V to 5.50V

Electrical Characteristics Over Operating Temperature Range (unless otherwise noted)

Commercial	T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5%	MIN = 4.75V	MAX = 5.25V
Military	T_A = −55°C to +125°C	V_{CC} = 5.0V ± 10%	MIN = 4.50V	MAX = 5.50V

Parameter	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −0.8mA V_{IN} = V_{IH} or V_{IL}		2.7	3.4		V
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.5	V
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			V
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	V
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −12mA				−1.5	V
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.5V	C_n			−2	mA
			P_3			−4	
			P_2			−6	
			P_0, P_1, G_3			−8.0	
			G_0, G_2			−14	
			G_1			−16	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX, V_{IN} = 2.7V	C_n			50	μA
			P_3			100	
			P_2			150	
			P_0, P_1, G_3			200	
			G_0, G_2			350	
			G_1			400	
I_I	Input HIGH Current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit (Note 4)	V_{CC} = MAX, V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX All Outputs LOW	MIL		62	99	mA
			COM'L		58	94	
		V_{CC} = MAX All Outputs HIGH	MIL		37		mA
			COM'L		35		

Notes:

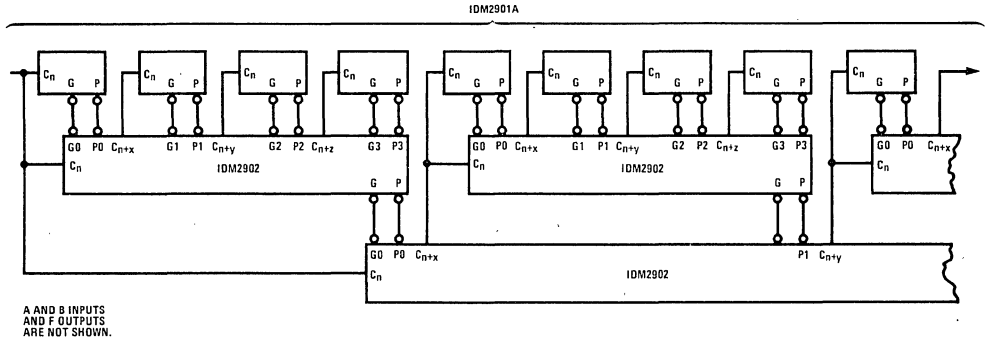
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current times Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Switching Characteristics $V_{CC} = 5.0V$, $T_A = 25°C$, $C_L = 15pF$, $R_L = 400\Omega$

Parameter	From (Input)	To (Output)	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	C_n	C_{n+j}	$P_0 = P_1 = P_2 = 0V$ $G_0 = G_1 = G_2 = 4.5V$		9.0	12	ns
t_{PHL}					9.0	12	
t_{PLH}	P_i	C_{n+j}	$P_i = 0V$ $(j > i)$ $C_n = G_0 = G_1 = G_2 = 4.5V$		6.0	8.0	ns
t_{PHL}					6.0	8.0	
t_{PLH}	G_i	C_{n+j}	$G_i = 0V$ $(j > i)$ $C_n = P_0 = P_1 = P_2 = 4.5V$		7.0	10	ns
t_{PHL}					7.0	10	
t_{PLH}	P_i	G or P	$P_i = 0V$ $(j > i)$ $C_n = G_0 = G_1 = G_2 = 4.5V$		6.0	10	ns
t_{PHL}					6.0	10	
t_{PLH}	G_i	G or P	$G_i = 0V$ $(j > i)$ $C_n = P_0 = P_1 = P_2 = 4.5V$		7.0	10	ns
t_{PHL}					7.0	10	

Typical Application

64-Bit ALU with Full Look-Ahead Carry in Three Levels



A AND B INPUTS AND F OUTPUTS ARE NOT SHOWN.

Ordering Information

Package Type	Package Number	Temperature Range	Order Number
Molded DIP	N16A	0°C to +70°C	IDM2902NC/DM74S182N
Hermetic DIP	J16A (D16C)	0°C to +70°C	IDM2902JC/DM74S182J
Hermetic DIP	J16A (D16C)	−55°C to +125°C	IDM2902JM/DM54S182J
Hermetic DIP	J16A (D16C)	−55°C to +125°C	IDM2902JM/883/DM54S182J/883

National Semiconductor

2900 Family/ Bipolar Microprocessor

IDM2909A/11A Microprogram Sequencer

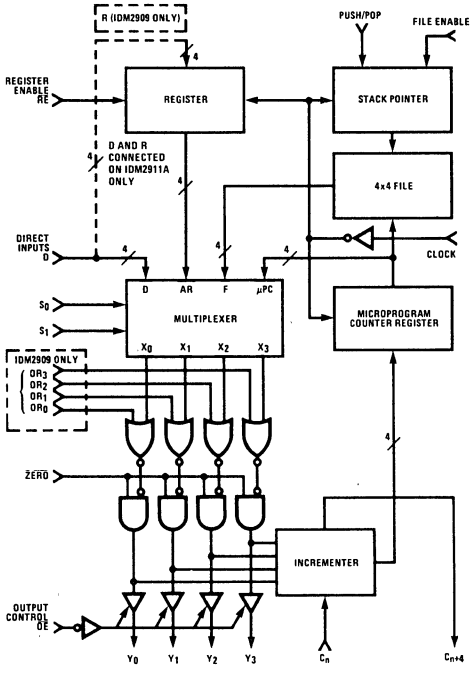
General Description

The IDM2909A is a 4-bit wide address controller that is used to sequence through a series of microinstructions contained in ROM or PROM. Two devices can be interconnected to generate an 8-bit address (256 words), three devices for a 12-bit address (4k words), and so on. For a given device, the 4-bit address field can originate from any one of four sources. These are: (1) direct "D" inputs from an external source, (2) external data from an internal register "R," (3) a push/pop stack that is 4 words deep, and (4) a program counter, which usually contains the last address incremented by "1." Control of the push/pop stack is such that the stack can efficiently execute nested subroutine linkages. Moreover, each of the four TRI-STATE outputs can be ORed with an external input to implement conditional skips or branch instructions; a separate line is used to force the outputs to an "all-zero" state. As shown in the block diagram, the IDM2911A is identical to the IDM2909A, except the four OR inputs are removed and the "D" and "R" inputs are connected. The IDM2909A is housed in a 28-pin dual-in-line package, whereas the IDM2911A is a 20-pin device.

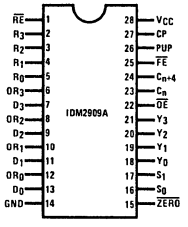
Features and Benefits

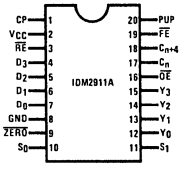
- 4-bit cascadable slice – any number of microwords can be generated.
- Internal address register – provides four address sources.
- Branch input for N-way branches – where "N" is any word in the microcode.
- Cascadable 4-bit microprogram counter.
- 4x4 file with stack pointer and push/pop control – four microsubroutines can be nested.
- Zero input for returning to microcode word "zero."
- Individual OR input for each bit to branch to higher microinstruction (IDM2909A only).
- TRI-STATE outputs.
- All internal registers change state on Low-to-High transition of clock pulse.

Simplified Block Diagram



Connection Diagrams





Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +7.0V
DC Output Current into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Operating Range

P/N	Ambient Temperature	V_{CC}
IDM2909ANC, JC	0°C to +70°C	4.75V to 5.25V
IDM2911ANC, JC	0°C to +70°C	4.75V to 5.25V
IDM2909AJM, JM/883	−55°C to +125°C	4.50V to 5.50V
IDM2911AJM, JM/883	−55°C to +125°C	4.50V to 5.50V

Electrical Characteristics

Commercial T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V
Military T_A = −55°C to +125°C, V_{CC} = 4.50V to 5.50V

Parameter	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output High Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	Mil	I_{OH} = −1.0mA	2.4			V
			Com'l	I_{OH} = −2.6mA	2.4			
V_{OL}	Output Low Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	V
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 16mA (Note 5)				0.5	
V_{IH}	Input High Level	Guaranteed input logical high voltage for all inputs			2.0			V
V_{IL}	Input Low Level	Guaranteed input logical low voltage for all inputs					0.8	V
V_I	Input Clamp Voltage	V_{CC} = min, I_{IN} = −18mA					−1.5	V
I_{IL}	Input Low Current	V_{CC} = max, V_{IN} = 0.4V					−0.36	mA
I_{IH}	Input High Current	V_{CC} = max, V_{IN} = 2.7V					20	μA
I_I	Input High Current	V_{CC} = max, V_{IN} = 7.0V					0.1	mA
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = max			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = max (Note 4)				80	130	mA
I_{OZL}	Output Off Current	V_{CC} = max, $\overline{OE}$ = 2.7V	V_{OUT} = 0.4V				−20	μA
I_{OZH}			V_{OUT} = 2.7V				20	

Notes:

1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2, and D_3. Other inputs open. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. The 16mA guarantee applies only to Y_0, Y_1, Y_2, and Y_3.

Standard Screening (Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level	
			IDM2909A/2911A NC, JC	IDM2909A/2911A JM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour, 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100%*	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/cm^3	100%*	100%
Gross Leak	1014	C Fluorocarbon	100%*	100%
Electrical Test Subgroups 1, 7, and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

*Not applicable to IDM2909ANC or IDM2911ANC.

Group A Subgroups
(as defined in MIL-STD-883, Method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum Rated Temperature
3	DC	Minimum Rated Temperature
7	Function	25°C
8	Function	Maximum and Minimum Rated Temperature
9	Switching	25°C
10	Switching	Maximum Rated Temperature
11	Switching	Minimum Rated Temperature

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level
			IDM2909A/11A JM/883
Burn-In	1015	D 125°C 160 hours min.	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Switching Characteristics Over Operating Range

All parameters are guaranteed worst case over the operating voltage and temperature range for the device type.

IDM2909A/11A JC, NC $T_A = 0°C$ to $+70°C$ $V_{CC} = 4.75V$ to $5.25V$

IDM2909A/11A JM, JM/883 $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$)

Table 1. Minimum Clock Requirements

Minimum Clock Low Time	30
Minimum Clock High Time	30

Table 2. Maximum Combinatorial Propagation Delays

Inputs	Outputs	
	Y_i	C_{n+4}
$\overline{OE}$	25	–
$\overline{ZERO}$	30	35
OR_i	20	30
S_0, S_1	30	35
D_i	20	30
C_n	–	18

Table 3. Maximum Delays from Clock to Outputs

Functional Path	Grade	Clock to Y_i	Clock to C_{n+4}
Register ($S_1 S_0$ = LH)	C	40	45
	M	50	55
μ Program Counter ($S_1 S_0$ = LL)	C	40	45
	M	50	55
File ($S_1 S_0$ = HL)	C	45	50
	M	55	60

$C_L \leq 50pF$
(except output disable tests)

Table 4. Setup and Hold Time Requirements

External Inputs	t_s	t_h
$\overline{RE}$	20	0
R_i	15	0
PUSH/POP	20	0
$\overline{FE}$	20	0
C_n	15	0
D_i	20	0
OR_i	20	0
S_0, S_1	30	0
$\overline{ZERO}$	30	0

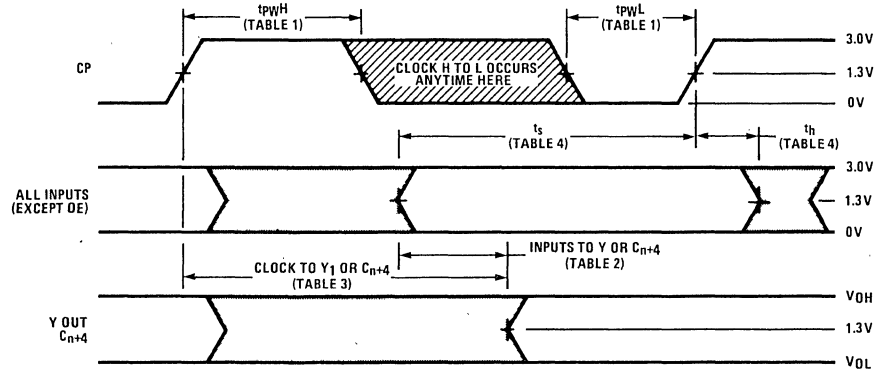


Figure 1. Switching Waveforms (refer to preceding tables for specific values)

Architecture of Microprogram Sequencer

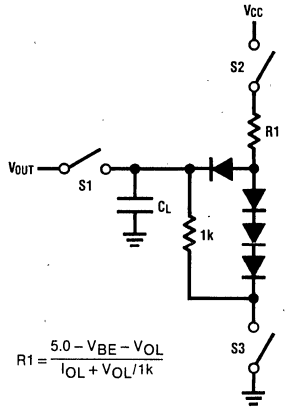
A 4-input multiplexer selects one of four sources for the address of the next microinstruction address; these sources are: the address register, the microprogram counter, direct inputs, and the memory file. The multiplexer is controlled by the S_0/S_1 inputs. As shown in figure 2, the address register consists of four D-type edge-triggered flip-flops with a common clock enable. When the REGISTER ENABLE signal is low, new data is entered on the low-to-high transition of the clock. The "Q" outputs of the address register are available at the input of the multiplexer as a source for the next microinstruction address. The direct inputs (D_0-D_3) can likewise be selected as an address input to the multiplexer.

Both the IDM2909A and the IDM2911A are bipolar microprogram sequencers designed for use in high-speed microprocessors, high-performance computer control units, and other applications where overlap fetch of the microinstruction is required. Each device is cascadable in 4-bit increments such that two devices can address up to 256 words of microprogram memory, three devices up to 4k of memory, and so on. A detailed block diagram of the microprogram sequencer is shown in figure 2.

In the IDM2911A, the 4-bit direct field is also used as an input to the address register, that is, R_0 and D_0 are connected, R_1 and D_1 are connected, and so on. With the "R" and "D" connections made and the OR inputs removed, the IDM2911A can perform an N-way branch, where "N" is any word in the microcode.

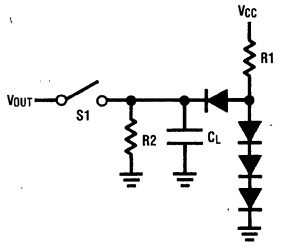
Test Output Load Configurations for IDM2909A/2911A

A. Three-State Outputs



$$R1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1k}$$

B. Normal Outputs



$$R2 = \frac{2.4V}{I_{OH}}$$

$$R1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R2}$$

Note 1: $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.

Note 2: S1, S2, S3 are closed during function tests and all AC tests except output enable tests.

Note 3: S1 and S2 are closed while S2 is open for t_{PZH} test.
S1 and S2 are closed while S3 is open for t_{PZL} test.

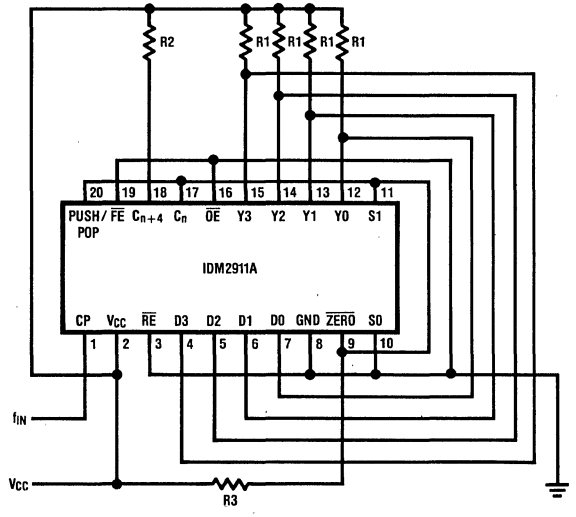
Note 4: $C_L = 5.0$ pF for output disable tests.

Test Output Loads

Pin # (DIP)	Pin Label	Test Circuit	IDM2909		IDM2909A	
			R1	R2	R1	R2
18–21	Y_{0-3}	A	300	1k	220	1k
24	C_{n+4}	B	470	2.4k	220	2.4k

Pin # (DIP)	Pin Label	Test Circuit	IDM2911		IDM2911A	
			R1	R2	R1	R2
12–15	Y_{0-3}	A	300	1k	220	1k
18	C_{n+4}	B	470	2.4k	220	2.4k

Burn-in Circuit for IDM2911A



Notes:
Max $I_{CC} = 200$ mA
$T_A = +125°C$
Resistors = ±5%
R1 = 390Ω
R2 = 560Ω
R3 = 1 kΩ
$f_{IN} = 100$ kHz, 50% duty cycle, 0V–3V
From clock buffer on each board:
V_{CC} min = 5.0V
V_{CC} max = 5.1V

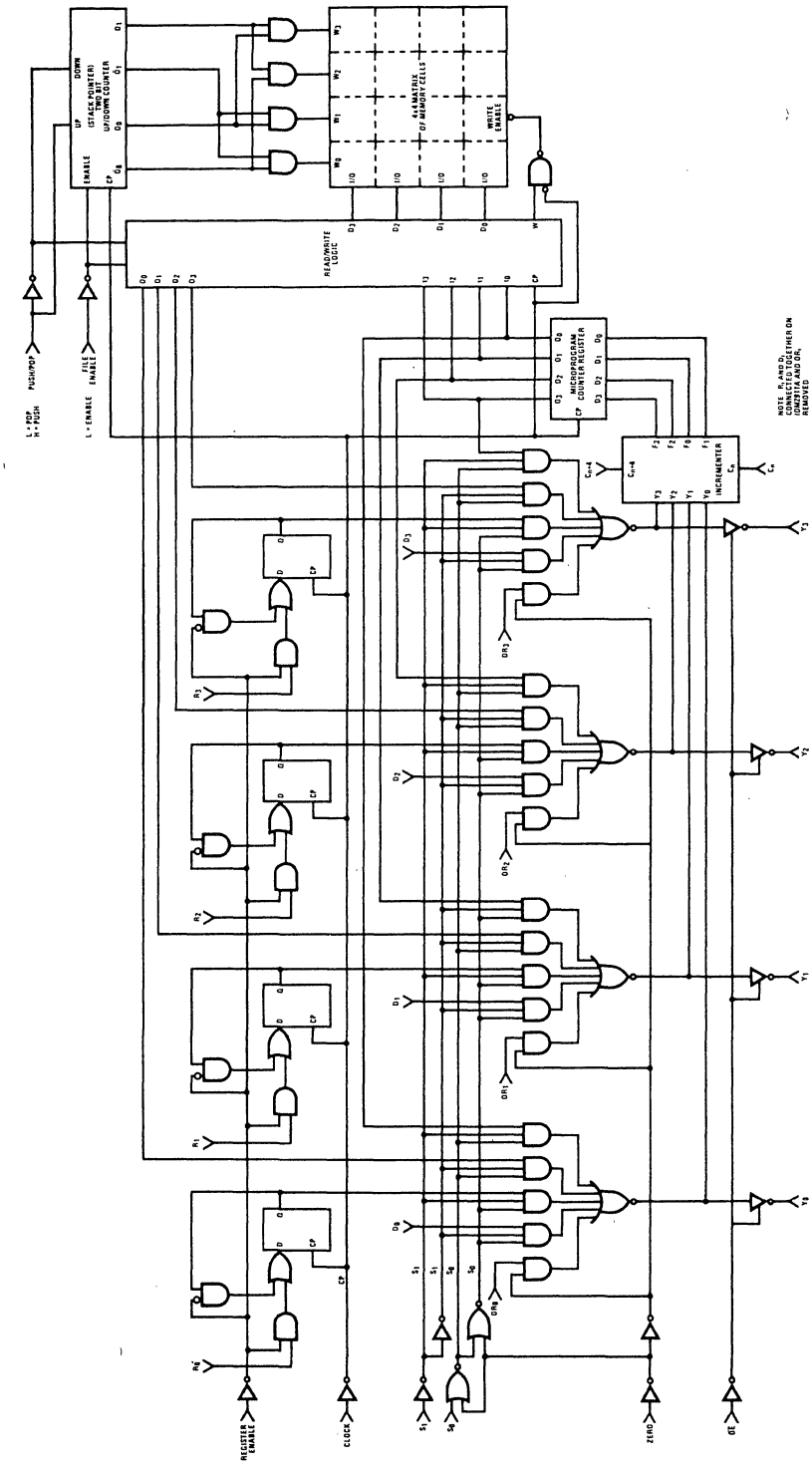


Figure 2. Microprogram Sequencer - Detailed Block Diagram

The microprogram counter consists of a 4-bit incrementer followed by a 4-bit register. The carry-in (C_n) and carry-out (C_{n+4}) features of the incrementer make cascading to larger word lengths easy and straightforward. The microprogram counter can be used in either of two ways. When the least significant bit of C_n is high, the microprogram register (μPC) is loaded on the next clock cycle with the current output word (Y_0-Y_3) plus 1, that is, $Y+1 \rightarrow \mu PC$; thus, sequential microinstructions are executed. When C_n is low, the "Y" outputs are not incremented; accordingly, the same microinstruction can be repeatedly executed. The last address source available at the input of the multiplexer is the 4-bit/4-word stack file; when executing subroutines, the file provides return address linkage. The 4-by-4 memory matrix contains a stack pointer (SP) that always points to the last word written in the file; thus, stack reference operations (looping) can be performed without a push or pop. The stack pointer operates as an up/down counter with separate PUSH/POP and FILE ENABLE inputs. When the enable signal is low and the other signal is high, the "push" operation is enabled. Under these conditions, the stack pointer is incremented and the file is written with the required return linkage, that is, the next microinstruction address following the subroutine jump that initiated the "push." If both input signals (PUSH/POP and FILE ENABLE) are low, a "pop" operation is implemented. During this clock cycle, the return linkage is used to return from the subroutine; the next low-to-high transition of the clock pulse decrements the stack pointer.

When the FILE ENABLE signal is high, the stack pointer is not incremented or decremented, regardless of whether the PUSH/POP signal is high or low. Linkage of the stack pointer is such that any combination of pushes, pops, or stack references can be implemented; one microinstruction subroutine can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested. The ZERO input is used to force all four outputs (Y_0-Y_3) of the multiplexer to the zero (logic 0) state. When the zero input is low, all Y-outputs are low, unless overridden by the OUTPUT ENABLE ($\overline{OE}$) signal. Also, each bit of the Y-output word can be ORed at the input such that conditional logic can be enforced; this allows execution of microinstructions to occur in any programmed sequence.

Definition of Terms and Symbols (Figure 2)

Inputs to IDM2909A/11A:

S_0/S_1	Control lines for address-source selection
$\overline{FE}$/PUP	Control lines for push/pop stack
$\overline{RE}$	Enable signal for internal address register
OR_i	Logic OR input for each address output line
$\overline{ZERO}$	Logic AND input for all output lines
$\overline{OE}$	Output Enable; when $\overline{OE}$ is high, the Y-outputs are TRI-STATE (high impedance)
C_n	Carry-in to incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock inputs

Outputs from the IDM2909A/11A:

Y_i	Address outputs; address inputs to control memory
C_{n+4}	Carry-out from the incrementer
μPC	Contents of the microprogram counter
REG	Contents of the internal register
STK0/STK3	Contents of the push/pop stack. By definition, the word addressed by the stack pointer in the 4-by-4 file is STK0. Data is pushed onto the stack at STK0 and is subsequently pushed to STK1, STK2, and finally to STK3. When the stack is popped, data is removed in the following order: STK3 → STK2 → STK1, and then to STK0. When a push or pop occurs, only the stack pointer changes — the data is not physically shifted within the stack.
SP	Contents of the stack pointer

Terms and symbols external to the IDM2909A/11A:

A	Control memory address
I(A)	Instruction in control memory at address "A"
μWR	Contents of microword register at output of control memory; this register contains the instruction currently being executed
T_n	Period of timing cycle

Operation of the IDM2909A/11A

Select codes for the multiplexer and the truth tables for output control/stack control are shown in figure 3. The two bits (S_0/S_1) from the microword register (plus additional branching logic) determine the data source for the next microinstruction address. The selected data source appears on the Y-outputs of the multiplexer.

A state table for S_0, S_1, $\overline{FE}$, and PUP is shown in figure 4; these signals define not only the address specified by the Y-outputs, but also the state of all internal registers, following the low-to-high transition of the clock pulse. In figure 4, it is assumed that the microprogram counter initially contains some word "J," word "K" is in the address register, and words R_a through R_d are contained in the 4-word push/pop stack.

The sequence for executing a subroutine using the IDM2909A is illustrated in figure 5. For any given clock cycle, the instruction being executed is contained in the microword register (μWR); the contents of this register also directly (or indirectly) control S_0, S_1, $\overline{FE}$, and PUP. At the appropriate time, the starting address of the subroutine is applied to the "D" inputs of the sequencer. The three left-hand columns of figure 5 show the execution sequence of the instructions and the designated execution cycles. At address "J+2," the sequence-control part of the microinstruction contains the command "Jump To Subroutine A." At time t_2, the "J+2" instruction resides in the μWR and the inputs of the sequencer are set up to execute the "jump," and to save the return address. Address bits for subroutine "A" are taken from the microword register and applied to the D-inputs of the multiplexer; the output appears at the Y-port of the multiplexer.

Address Selection

Octal	S_1	S_0	Source for Y Outputs	Symbol
0	L	L	Microprogram Counter	μPC
1	L	H	Register	REG
2	H	L	Push-Pop Stack	STK0
3	H	H	Direct Inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	Push-Pop Stack Change
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 3. Truth Tables for Multiplexer Control Signals

Cycle	$S_1, S_0, \overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	Comment	Principal Use
N N+1	0 0 0 0 –	J J+1	K K	R_a R_b	R_b R_c	R_c R_d	R_d R_a	J –	Pop Stack	End Loop
N N+1	0 0 0 1 –	J J+1	K K	R_a J	R_b R_a	R_c R_b	R_d R_c	J –	Push μPC	Set Up Loop
N N+1	0 0 1 X –	J J+1	K K	R_a R_a	R_b R_b	R_c R_c	R_d R_d	J –	Continue	Continue
N N+1	0 1 0 0 –	J K+1	K K	R_a R_b	R_b R_c	R_c R_d	R_d R_a	K –	Pop Stack; Use AR for Address	End Loop
N N+1	0 1 0 1 –	J K+1	K K	R_a J	R_b R_a	R_c R_b	R_d R_c	K –	Push μPC; Jump to Address in AR	JSR AR
N N+1	0 1 1 X –	J K+1	K K	R_a R_a	R_b R_b	R_c R_c	R_d R_d	K –	Jump to Address in AR	JMP AR
N N+1	1 0 0 0 –	J R_a+1	K K	R_a R_b	R_b R_c	R_c R_d	R_d R_a	R_a –	Jump to Address in STK0; Pop Stack	RTS
N N+1	1 0 0 1 –	J R_a+1	K K	R_a J	R_b R_a	R_c R_b	R_d R_c	R_a –	Jump to Address in STK0; Push μPC	
N N+1	1 0 1 X –	J R_a+1	K K	R_a R_a	R_b R_b	R_c R_c	R_d R_d	R_a –	Jump to Address in STK0	Stack Ref (Loop)
N N+1	1 1 0 0 –	J D+1	K K	R_a R_b	R_b R_c	R_c R_d	R_d R_a	D –	Pop Stack; Jump to Address on D	End Loop
N N+1	1 1 0 1 –	J D+1	K K	R_a J	R_b R_a	R_c R_b	R_d R_c	D –	Jump to Address on D; Push μPC	JSR D
N N+1	1 1 1 X –	J D+1	K K	R_a R_a	R_b R_b	R_c R_c	R_d R_d	D –	Jump to Address on D	JMP D

X = Don't Care, 0 = Low, 1 = High, Assume C_n = High
Note: STK0 is the location addressed by the stack pointer.

Figure 4. Output and Internal Next-Cycle Register States for IDM2909A/11A

Control Memory

Execute Cycle	Microprogram	
	Address	Sequencer Instruction
	J–1	–
t0	J	–
t1	J+1	–
t2	J+2	JSR A
t6	J+3	–
t7	J+4	–
	–	–
	–	–
	–	–
	–	–
t3	A	I(A)
t4	A+1	–
t5	A+2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle		t0	t1	t2	t3	t4	t5	t6	t7	t8	t9
Clock											
Signals											
IDM2909A Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	–	–	–	J+3	J+3	J+3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
IDM2909A Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)		

C_n = High

Figure 5. Execution of Subroutine

Subsequently, the first instruction "I(A)" of the subroutine is accessed and input to μWR. On the next low-to-high transition of the clock, I(A) is loaded into μWR for execution and the return address (J+3) is pushed onto the stack. At t_5, the return instruction is executed. Figure 6 shows a similar instruction sequence where one subroutine is linked to another – the second subroutine consists of only one microinstruction.

Control Memory

Execute Cycle	Microprogram	
	Address	Sequencer Instruction
	J–1	–
t0	J	–
t1	J+1	–
t2	J+2	JSR A
t9	J+3	–
	–	–
	–	–
	–	–
	–	–
t3	A	–
t4	A+1	–
t5	A+2	JSR B
t7	A+3	–
t8	A+4	RTS
	–	–
	–	–
	–	–
	–	–
t6	B	RTS
	–	–
	–	–

Execute Cycle		t0	t1	t2	t3	t4	t5	t6	t7	t8	t9
Clock											
Signals											
IDM2909A Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	–	–	–	J+3	J+3	J+3	A+3	J+3	J+3	–
	STK1	–	–	–	–	–	–	J+3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
IDM2909A Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)

C_n = High

Figure 6. Two Nested Subroutines

Applications Example

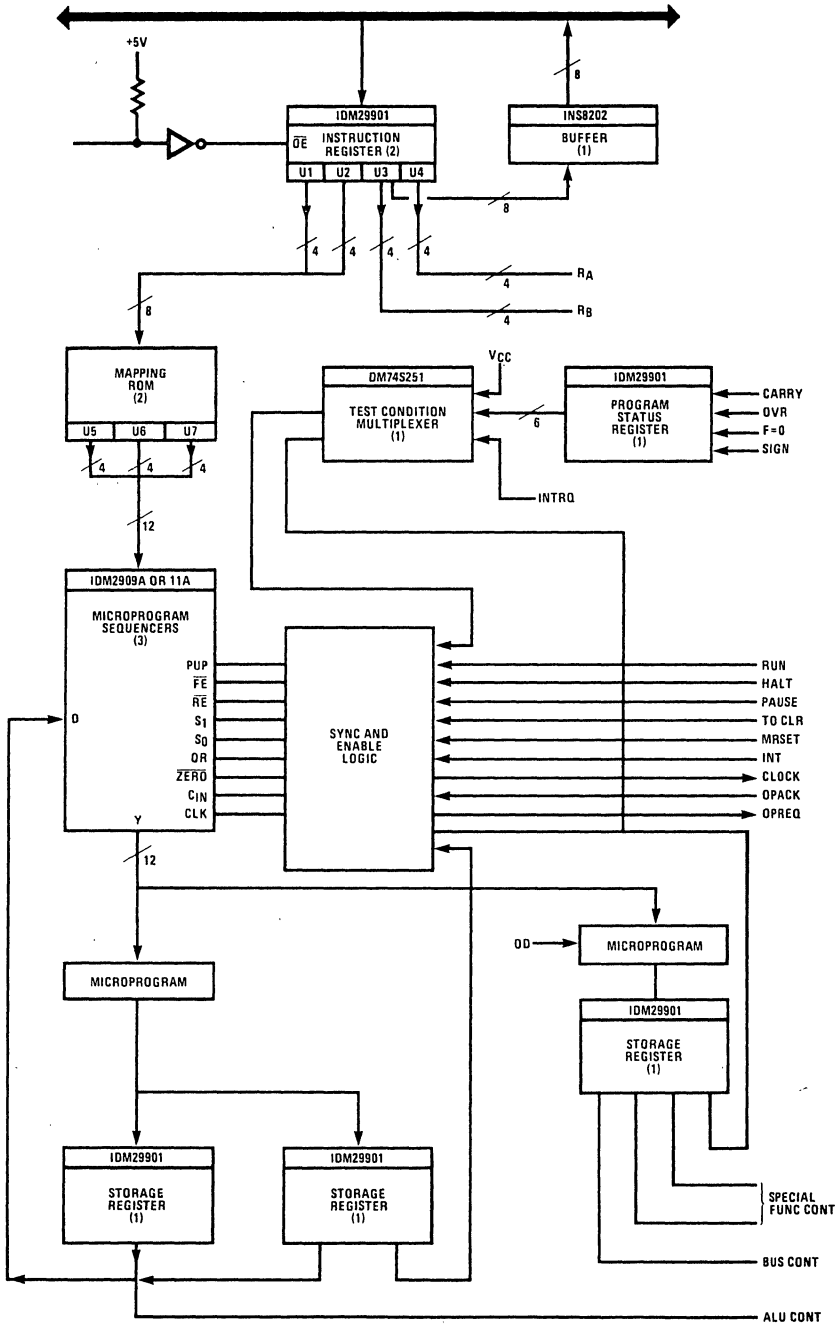


Figure 7. Typical Use of an IDM2909A as a Microprogram Sequencer in a Computer Control Unit

National Semiconductor

2900 Family/
Bipolar Microprocessor
PRELIMINARY

IDM2910A Microprogram Controller

General Description

The IDM2910A Microprogram Controller is a 12-bit wide address controller packaged in a standard 40-pin dual-in-line package. The IDM2910A features TRI-STATE® outputs and is fabricated using SCL (Schottky ECL) technology. The IDM2910A is a microprogram memory address controller that controls the execution sequence of microinstructions. In addition to being able to sequentially access memory, the IDM2910A is also able to conditionally branch to any microinstruction within the 4096 microinstruction range. A five-level last-in, first-out (LIFO) stack provides microsubroutine return linkage. An internal loop counter is included to provide the repeating instructions or perform up to 4096 loop iterations.

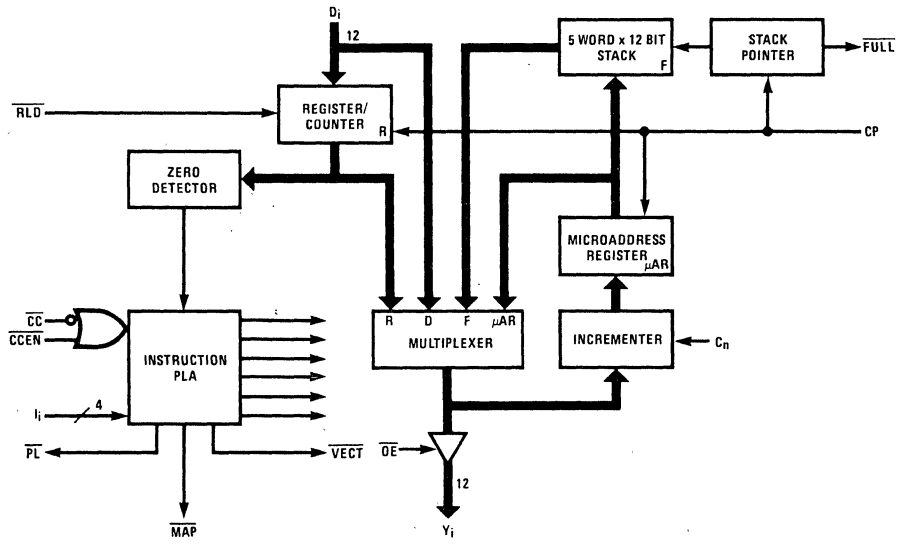
As each microinstruction is executed, the IDM2910A selects a 12-bit address from one of four sources:

1. The Microprogram Address Register which usually contains the increment address of the previous microinstruction.
2. The external Direct Input lines.
3. The Register/Counter which contains an address or data loaded during a previous microinstruction.
4. The LIFO Stack.

Features and Benefits

- Twelve-bit wide address — controls up to 4096 words of microcode with one device
- Internal register/counter — a 12-bit down-counter that may be used to count loop iterations
- Four address sources — the next microprogram address selected from the microprogram address/register data input lines, LIFO stack, or register counter
- Sixteen powerful microinstructions — executes 16 sequence control instructions
- Output enables for three branch address sources — replaces either external decoder or additional bit of microcode
- Positive-edge triggering for all internal registers
- Fast condition-code control — typically a 19ns delay from a condition-code input to an address output
- SCL technology — provides ECL speeds while maintaining low-power Schottky power consumption
- 100% reliability testing in compliance with MIL-STD-883.

IDM2910A Block Diagram



Absolute Maximum Ratings

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +6.3V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5V
DC Output Current, into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Operating Range

Part Number	Ambient Temperature	V_{CC}
IDM2910A JC, NC	0°C to +70°C	4.75V to 5.25V
IDM2910A JM, JM/883	−55°C to +125°C	4.50V to 5.50V

Standard Screening (Conforms to MIL-STD-883 for Class C parts)

Step	MILSTD-883 Method	Conditions	Level	
			DC, NC	DM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C: 24-hour 150°C	100%	100%
Temperature Cycle	1010	C: −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B: 10,000G	100%*	100%
Fine Leak	1014	A: 5×10^{-8} atm-cc/cm^3	100%*	100%
Gross Leak	1014	C2: Fluorocarbon	100%*	100%
Electrical Test Subgroups 1, 7, and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

*Not applicable to IDM2910ANC.

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level DM/883
Burn-In	1015	D: 125°C, 160 hours min	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Group A Subgroups

(as defined in MILSTD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum rated temperature
11	Switching	Minimum rated temperature

Electrical Characteristics

The following conditions apply unless otherwise specified:

Comm'l	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	min = 4.75V	max = 5.25V
Mil	$T_C = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	min = 4.50V	max = 5.50V

DC Characteristics over Operating Range

Symbol	Description	Test Conditions (Note 1)	Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = min, $I_{OH} = -5mA$, $V_{IN} = V_{IH}$ or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = min, $V_{IN} = V_{IH}$ or V_{IL}, Y_{0-11} I_{OL} = 12 mA (Comm'l) Y_{0-11} I_{OL} = 12mA (Mil) $\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$, $\overline{FULL}$ I_{OL} = 8mA			0.5	V
V_{IH}	Input HIGH Level (Note 4)	guaranteed input logical HIGH voltage for all inputs	2.0			V
V_{IL}	Input LOW Level (Note 4)	guaranteed input logical LOW voltage for all inputs			0.8	V
V_I	Input Clamp Voltage	V_{CC} = min, $I_{IN} = -18mA$			−1.5	V
I_{IL}	Input LOW Current	V_{CC} = max, $V_{IN} = 0.5V$			−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = max, $V_{IN} = 2.7V$			30	μA
I_I	Input HIGH Current	V_{CC} = max, $V_{IN} = 5.5V$			1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = max	−20		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = max, $\overline{OE} = 2.4V$, $V_{OUT} = 0.5V$			−50	μA
I_{OZH}	Output OFF Current	V_{CC} = max, $\overline{OE} = 2.4V$, $V_{OUT} = 2.4V$			50	μA
I_{CC}	Power Supply Current	V_{CC} = max | $T_A = 25°C$		160	245	mA
	IDM2910A DC, NC	$T_A = 0°C$ to $+70°C$			260	mA
		$T_A = +70°C$			220	mA
	IDM2910A DM, DM/883	$T_C = -55°C$ to $+125°C$			275	mA
		$T_C = +125°C$			185	mA

Notes:

1. For conditions shown as min or max, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should be tested only in a static- and noise-free environment.

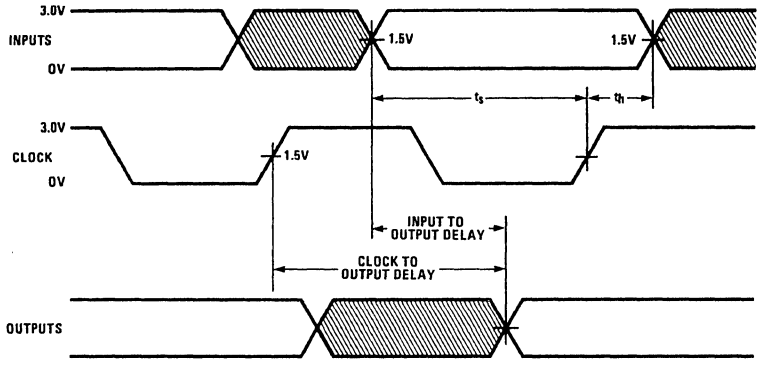


Figure 1. Switching Waveforms

Setup (t_S) and hold (t_h) times for varied inputs are listed in Table A. Combinational input to output delays are listed in Table B. Clock requirements are listed in Table C.

See Figure 3, Switching Waveform Timing, for a typical cycle.

Switching Characteristics

(Refer to Figure 1.)

IDM2910A switching characteristics for the typical, commercial and military operating ranges available are given in Tables A, B, and C on this page and the following page.

Table A contains setup and hold times with respect to the clock low-to-high transition. Table B contains combinational delays from input to output. Table C contains the clock requirements.

All measurements are made at 1.5V with input levels at 0V or 3V. All times are in nanoseconds.

Typical Room Temperature Characteristics

($T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 50pF$)

A. Setup and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$	11	6
$D_i \rightarrow AR$	15	6
I_0-I_3	35	6
$\overline{CC}$	22	6
$\overline{CCEN}$	21	6
C_n	19	6
$\overline{RLD}$	21	6

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$
D_0-D_{11}	14	—	—
I_0-I_3	24	20	—
$\overline{CC}$	21	—	—
$\overline{CCEN}$	21	—	—
CP I = 8, 9, 15	28	—	—
CP (Note) I = 8, 9, 15	28	—	—
CP All Other I	24	—	28
$\overline{OE}$	15/15	—	—

Note: If the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was low, delays are as listed.

C. Clock Requirements

Minimum Clock LOW Time	25	ns
Minimum Clock HIGH Time	25	ns
Minimum Clock Period, I = 8, 9, 15	50	ns
Minimum Clock Period, I = 14	50	ns

Clock periods for other instructions are determined by external conditions.

Guaranteed Characteristics over Commercial Operating Range

IDM2910A DC, NC

($T_A = 0°C$ to $+70°C$, $V_{CC} = 4.75V$ to $5.25V$, $C_L = 50pF$)

A. Setup and Hold Times

Input	t_s	t_h
$D_I \rightarrow R$	14	0
$D_I \rightarrow AR$	25	0
I_0-I_3	35	0
$\overline{CC}$	35	0
$\overline{CCEN}$	35	0
C_n	30	0
$\overline{RLD}$	25	0

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$
D_0-D_{11}	20	—	—
I_0-I_3	35	30	—
$\overline{CC}$	35	—	—
$\overline{CCEN}$	35	—	—
CP I = 8, 9, 15	45	—	—
CP (Note) I = 8, 9, 15	45	—	—
CP All Other I	35	—	30
$\overline{OE}$	25/25	—	—

Note: If the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was low, delays are as listed.

C. Clock Requirements

Minimum Clock LOW Time	30	ns
Minimum Clock HIGH Time	30	ns
Minimum Clock Period, I = 8, 9, 15	60	ns
Minimum Clock Period, I = 14	60	ns

Clock periods for other instructions are determined by external conditions.

Guaranteed Characteristics over Military Operating Range

IDM2910A DM, DM/883

($T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$, $C_L = 50pF$)

A. Setup and Hold Times

Input	t_s	t_h
$D_I \rightarrow R$	17	0
$D_I \rightarrow AR$	30	0
I_0-I_3	40	0
$\overline{CC}$	40	0
$\overline{CCEN}$	40	0
C_n	35	0
$\overline{RLD}$	30	0

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{FULL}$
D_0-D_{11}	25	—	—
I_0-I_3	40	35	—
$\overline{CC}$	40	—	—
$\overline{CCEN}$	40	—	—
CP I = 8, 9, 15	55	—	—
CP (Note) I = 8, 9, 15	55	—	—
CP All Other I	40	—	35
$\overline{OE}$	25/25	—	—

Note: If the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was low, delays are as listed.

C. Clock Requirements

Minimum Clock LOW Time	35	ns
Minimum Clock HIGH Time	35	ns
Minimum Clock Period, I = 8, 9, 15	70	ns
Minimum Clock Period, I = 14	70	ns

Clock periods for other instructions are determined by external conditions.

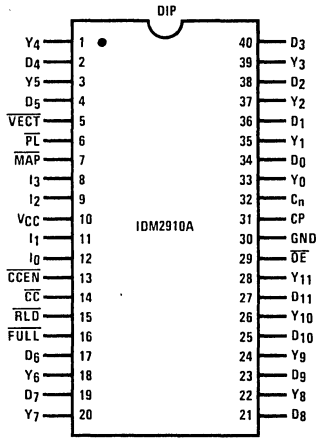


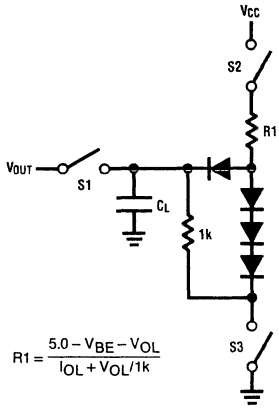
Figure 2. Pin Connection Diagram

Table 1. IDM2910A Pinout Descriptions

Abbreviation	Name	Function
D_i, i = 0 to 11	Direct Inputs	12 direct input lines carrying data into the register/counter or a jump address to be used by the multiplexer. D_0 is LSB.
I_i, i = 0 to 3	Instruction Lines	Four instruction lines. Select one-of-sixteen control instructions for the IDM2910A.
$\overline{CC}$	Condition Code	The outcome of a test is input through this line into the IDM2910A so that it may be used in conditional control instructions. A low on $\overline{CC}$ is interpreted as PASS test.
$\overline{CCEN}$	Condition Code Enable	Conditional control based on the $\overline{CC}$ input is enabled as long as $\overline{CCEN}$ is low. A high on $\overline{CCEN}$ overrides the $\overline{CC}$ input and the IDM2910A will operate as if $\overline{CC}$ were low.
C_n	Carry In	The carry input to the address register incrementer.
$\overline{RLD}$	Register Load	When LOW, will force a load of the register/counter on the next rising edge of the clock. Loading will be performed regardless of instruction or condition.
$\overline{OE}$	Output Enable	The TRI-STATE® control of Y_i outputs.
CP	Clock Pulse	All internal state changes are triggered by the rising edge of the clock.
V_{CC}	+5 Volts	
GND	Ground	
Y_i, i = 0 to 11	Address Outputs	12 address output lines to be used by the microprogram memory in accessing the next microword. Y_0 is LSB.
$\overline{FULL}$	Full Stack	This output will go low one microcycle after the stack becomes full.
$\overline{PL}$	Pipeline Address Enable	May be used to enable the first of three sources (usually pipeline register) onto the branch address bus connected to the D_i inputs.
$\overline{MAP}$	Map Address Enable	May be used to enable the second of three sources (mapping ROM, PROM or RAM) onto the branch address bus connected to the D_i inputs.
$\overline{VECT}$	Vector Address Enable	May be used to enable the third of three sources (usually interrupt starting address) onto the branch address bus connected to the D_i inputs.

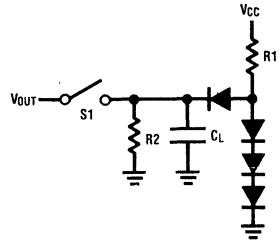
Test Output Load Configurations for IDM2910A

A. Three-State Outputs



$$R1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1k}$$

B. Normal Outputs



$$R2 = \frac{2.4V}{I_{OH}}$$

$$R1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R2}$$

Note 1: $C_L = 50$ pF includes scope probe, wiring and stray capacitances without device in test fixture.

Note 2: S1, S2, S3 are closed during function tests and all AC tests except output enable tests.

Note 3: S1 and S3 are closed while S2 is open for t_{PZH} test.
S1 and S2 are closed while S3 is open for t_{PZL} test.

Note 4: $C_L = 5.0$ pF for output disable tests.

Test Output Loads for IDM2901A

Pin # (DIP)	Pin Label	Test Circuit	R1	R2
—	Y_{0-11}	A	300	1k
5	$\overline{VECT}$	B	470	1.5k
6	$\overline{PL}$	B	470	1.5k
7	$\overline{MAP}$	B	470	1.5k
16	$\overline{FULL}$	B	470	1.5k

The IDM2910A Microinstruction Set

The IDM2910A executes sixteen control instructions. These instructions perform specific functions in addition to the selection of the next microcode word to be executed.

Four of the control instructions are unconditional — the function performed is specified only by the instruction itself.

Ten of the control instructions are conditional branches — based upon the state of an external data-dependent test. Since test results may be forced by suitable circuitry, it follows that the ten control instructions may also be used as unconditionals.

Three of the instructions allow conditional sequencing based upon the contents of the internal register/counter.

The IDM2910A instruction control set is shown in Table 2. One of the conditional branch control instructions is dependent on the external data test and the contents of the internal register/counter.

For the following discussion it is assumed that C_n is tied high.

For the ten conditional control instructions, the results of data dependent tests are applied to the condition code input, $\overline{CC}$. If the input to $\overline{CC}$ is low, the test is considered passed and the action specified under "PASS" (Table 2) will be taken. If the input to $\overline{CC}$ is high, the test is considered failed and the alternate action is taken. In many cases, the alternate action is the selection of the sequentially incremented address. By setting $\overline{CCEN}$ high for any specific microinstruction, $\overline{CC}$ testing will be disabled and a "PASS" will be forced. Other suggestions for using $\overline{CCEN}$ to save one bit of microcode are:

- If there is no data-dependent microcode, $\overline{CCEN}$ can be tied high.
- If data-dependent control instructions are never forced unconditionally, $\overline{CCEN}$ can be tied low.
- If $\overline{CCEN}$ is tied to the source of the IDM2910A instruction bit I_0, control instructions 4, 6, and 10 are left as data-dependent, and the others are made unconditional.

Several of the IDM2910A inputs may be used to modify instruction execution. For 10 of the 16 instructions, the combination of $\overline{CC}$ high and $\overline{CCEN}$ low is used as a test. When $\overline{RLD}$ is low, the direct inputs are loaded into the register/counter overriding any HOLD or DECREMENT ($\overline{DEC}$) operation specified in the microinstruction. The $\overline{OE}$ input, normally low, may be driven high to place the Y outputs in the TRI-STATE® condition.

The LIFO stack contains a 5-word, 12-bit file memory and a stack pointer which addresses the value presently at the top of the stack. Actual control over the stack pointer is possible when using microinstruction 0 (JUMP ZERO or RESET). This microinstruction clears the stack by resetting the stack pointer to zero. The contents at the top of the stack will remain undefined following execution of microinstruction 0, or whenever the stack becomes empty. Any pops performed while the stack is empty will place an undefined address at the F inputs to the multiplexer and the stack pointer will remain at zero.

If five more pushes than pops have occurred since the stack was last empty, the stack will become full. Once the stack is full, the $\overline{FULL}$ output will go low. $\overline{FULL}$ will go low on the first microcycle following the fifth push. If any additional push operations are performed on a full stack, the stack becomes overwritten and any previous information is lost.

Table 2. IDM2910A Microinstruction Set

Hex I_3-I_0	Mnemonic	Name	Reg/Cntr Contents	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH or $\overline{CC}$ = LOW		Reg/ Cntr	Enable
				Y	Stack	Y	Stack		
0	JZ	JUMP ZERO	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	COND JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH COND LD CNTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR ≠ 0	≠ 0	F	HOLD	F	HOLD	DEC	PL
			= 0	PC	POP	PC	POP	HOLD	PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠ 0	D	HOLD	D	HOLD	DEC	PL
			= 0	PC	HOLD	PC	HOLD	HOLD	PL
A	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
B	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
C	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
D	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
E	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
F	TWB	THREE-WAY BRANCH	≠ 0	F	HOLD	PC	POP	DEC	PL
			= 0	D	POP	PC	POP	HOLD	PL

Note 1: If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold; else load. X = Don't Care.

IDM2910A Architecture

The IDM2910A Bipolar Microprogram Controller is intended for use in very high-speed microprocessor applications. Up to 4096 microwords may be addressed using the IDM2910A.

A multiplexer within the IDM2910A selects one of four inputs as the source of the next microinstruction address. The four sources are:

1. the microprogram address register (μAR)
2. the register/counter
3. the direct input lines
4. the LIFO stack

1. The Microprogram Address Register contains a twelve-bit incrementer followed by a twelve-bit register. Two uses for the microprogram address register are:
   a. When carry-in (C_n) is high, the current microprogram address plus one ($Y_i + 1$) is loaded into the address register on the next positive clock transition. Therefore, microprogram words are accessed sequentially.
   b. When carry-in (C_n) is low, the current microprogram address is passed through the incrementer and loaded into the address register on the next position clock transition. Thus, the same microinstruction may be repeated as often as is required.
2. The register/counter contains twelve D-type edge-triggered flip-flops with a common clock enable. When the register load control ($\overline{RLD}$) is low, addresses from the direct input bus are loaded into the register on the next positive-going clock. Some sequence control instructions include a load operation. For most microcomputer systems, these instructions will be sufficient, thereby simplifying the microcode.
3. The Direct Input lines are a direct input source which may be used for microprogram branching.
4. The LIFO stack is a 5-word by 12-bit stack used to provide return address linkage when executing microsubroutines or loops. The stack incorporates a 5 × 12 file (RAM) and a stack pointer that always points to the last entry into the file. Stack reference operations (microprogram looping) may be executed without popping the stack.

The stack pointer is an up/down counter that is incremented whenever a push operation is performed (microinstructions 1, 4, and 5). Once the pointer is incremented, the return address is written into the location indicated by the stack pointer on the positive-going clock following the push.

The stack pointer is decremented whenever the pop operation is performed (microinstructions 8, 10, 11, 13, and 15). The stack pointer is decremented on the positive-going clock following a pop, effectively removing the return address from the top of the stack.

Stack pointer linkage is such that any combination of pushes, pops, or stack references may be performed. For control instruction 0 (JUMP ZERO or RESET), the stack pointer is reset. For each push operation, the microsubroutine nesting depth is increased by one; for each pop operation, the depth decreases by one. The maximum nesting depth is five. Once the stack becomes full, $\overline{FULL}$ goes low and the stack pointer can no longer be incremented. Further pushes will write over the preceding address at the top of the stack. A pop from an empty stack (stack pointer at zero) will place a meaningless address on the Y outputs, and the stack pointer will remain at zero. A stack pointer at zero remains unchanged by any number of additional pops.

The register/counter operates as a twelve-bit down-counter during microinstructions 8, 9, and 15, with register contents zero as a branch condition. This branch condition provides efficient repetition of microinstructions. The internal arrangement of the register/counter is such that if a number N is loaded into it and the register is used as a loop termination counter, the sequence will be executed N + 1 times. A three-way branch condition is available (control instruction 15) under control of both the register/counter and the condition code input ($\overline{CC}$).

The Y output lines are TRI-STATE® allowing the Y outputs to be disabled. When disabled (via $\overline{OE}$), the address lines can be externally driven, allowing automatic checkout of the microcomputer system.

Architectures Using the IDM2910A

Shading illustrates paths which can limit speed.

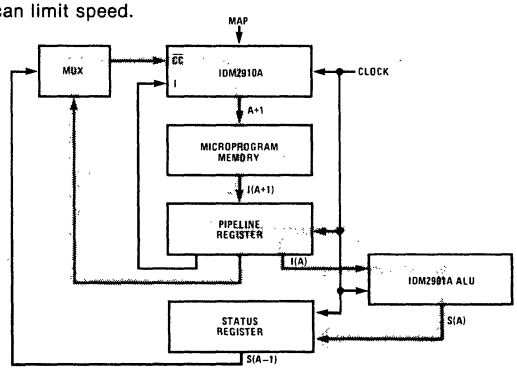


Figure 3a. Single-Level Pipeline Based Architecture

A one-level pipeline provides for better speed than most other architectures. The IDM2910A array and the microprogram memory are in parallel speed paths, rather than in series. This architecture is recommended for IDM2910A designs.

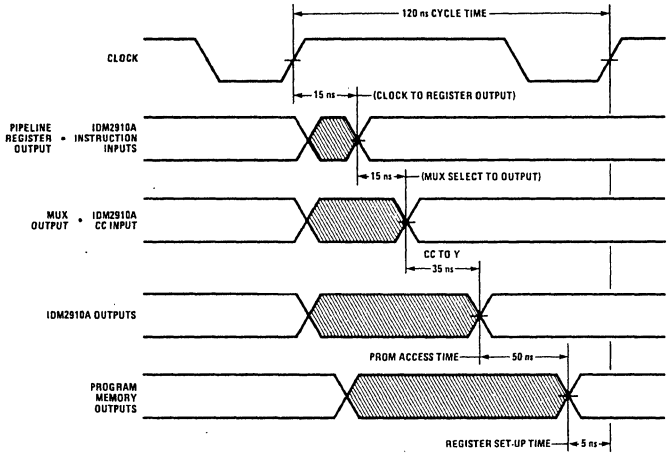


Figure 3b. Typical Timing Waveform for Single-Level Pipeline Based Architecture

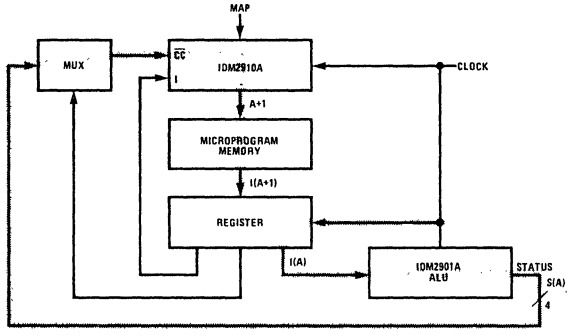


Figure 4. Instruction Based Architecture

The microinstruction being executed is in the register at the microprogram memory output. The IDM2910A and the microprogram memory are in series. Any conditional branches are executed on the same cycle as the ALU operation generating the condition.

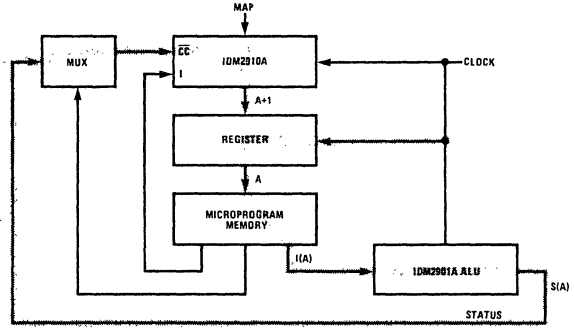


Figure 5. Address Based Architecture

The address of the microinstruction being executed is in the register at the IDM2910A output. The IDM2910A and the microprogram memory are in the critical path. This architecture operates at approximately the same speed as the instruction based architecture, but requires fewer register bits because only the address (typically 10 to 12 bits) is stored instead of the instruction (typically 40 to 60 bits).

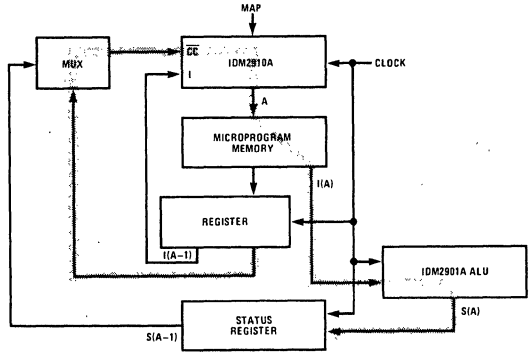


Figure 6. Data Based Architecture

The status register provides for conditional branch control based upon the results of the previous ALU cycle. The IDM2910A and the microprogram memory are in the critical path.

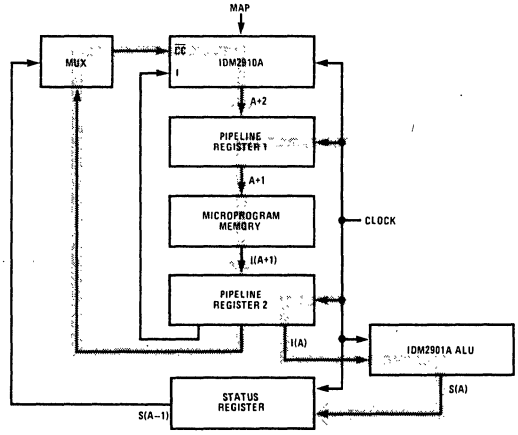


Figure 7. Two-Level Pipeline Architecture

The two-level pipeline provides the maximum possible speed. but is more difficult to program because the selection of a microinstruction occurs two microinstructions ahead of its execution.

IDM2910A Operation

The results of each instruction in determining the Y outputs, and the controlling of the three enable signals ($\overline{PL}$, $\overline{MAP}$, $\overline{VECT}$) are given in Table 2. Also shown is the effect of the microinstructions on the register/counter and the stack after the next positive-going clock. The multiplexer determines which of the internal sources drive the Y output lines. Depending upon the condition of C_n, the address loaded into the microprogram address register will be identical to the Y outputs, or will be one greater. For each microinstruction, only one of the three enable outputs ($\overline{PL}$, $\overline{MAP}$, or $\overline{VECT}$) is low. These three enable signals may be used to control the TRI-STATE® outputs of three external sources of microprogram address to allow them to drive the direct input bus (D_i) without additional logic. The external sources are:

1. A source of microprogram jumps (usually part of a pipeline register).
2. A PROM which maps machine language to a microinstruction starting location (entry point).
3. An optional third source of microinstructions (often a vector from a DMA or interrupt source).

The function performed by three of the control instructions depends upon the contents of the register/counter. The counter is decremented if it contains a non-zero value. If the value in the counter is zero, it is held and a different microprogram next-address is selected. These types of instructions are useful for executing a microinstruction loop a known number of times. The three-way branch control instruction (number 15) is affected by both the external condition code $\overline{CC}$ and the contents of the register/counter.

The following paragraphs describe each of the IDM2910A control instructions. Included with each of the descriptions is an execution flowchart showing typical microprogram flow.

Each of the examples is intended to show a typical microprogram flow as various microprogram control instructions are executed. The typical circuit of Figure 3 is assumed.

The microprogram addresses in the illustrations were chosen arbitrarily and have no significance other than

to illustrate microprogram flow, the only exception being control instruction 0, JZ (JUMP ZERO or RESET), *which always selects the next address to be zero.*

Execution flowcharts should be interpreted as follows:

Each dot relates to one microcycle. While this microcycle is going on the IDM2910A control instruction will be supplied by the microprogram memory word presently in the pipeline register.

A dot surrounded by a circle refers to the control instruction under discussion. Dashed lines refer to conditional actions. Solid lines refer to unconditional actions or to the outcome of =Test Failed= in conditional control instructions.

Dashed arrows refer to conditional branches (address changes other than sequential flow), which will be selected if the test is passed ($\overline{CC}$ = LOW). Solid arrows refer to unconditional branches or to the outcome of =Test Failed= in conditional control instructions.

Parentheses ( ) should be read "contents of," e.g., (D_i) = contents of D_i.

Control Instruction 0

JZ (Jump Zero or Reset) — This control instruction clears the stack pointer and specifies unconditionally that the next address is zero. This control instruction is useful for power-up sequences if the initialization routines start at microprogram memory location zero.

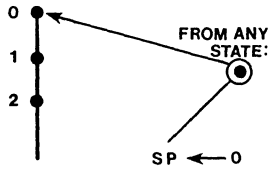


Figure 8. JUMP ZERO (JZ)

Control Instruction 1

CJS (Conditional Jump-to-Subroutine) — This control instruction executes a conditional jump to a subroutine located at the address found in the pipeline register. Referring to Figure 9, the unconditional microprogram flow is from address 50 through address 52. When the contents of address 52 are in the pipeline register, the next address control instruction is CJS. If the conditional test is passed, address 53 will be pushed onto the stack and the next instruction executed will be at address 90. The address pushed onto the stack provides a return link once the microsubroutine starting at address 90 is completed. For example, a Return-from Subroutine (CRTN, control instruction 10) was executed at address 93. If the conditional test fails, the Jump-to-Subroutine will not be executed and the contents at address 53 will be executed. In this manner, the CJS control instruction at address 52 will cause the microprogram word at either address 90 or address 53 to be executed.

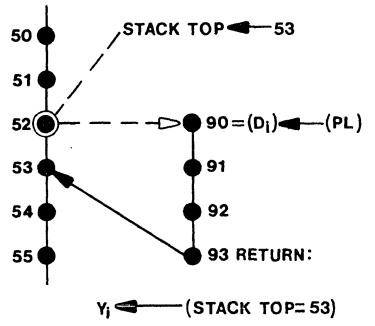


Figure 9. COND JSB PL (CJS)

Control Instruction 2

JMAP (Jump-Map) — This is an unconditional jump control instruction. When JMAP is executed, the $\overline{MAP}$ output is enabled and the next microinstruction address is taken from the mapping PROMs. The JMAP control instruction is normally used towards the end of an instruction-fetch sequence for the microcomputer. At that time the next instruction to be executed should be valid, allowing it to be mapped into the corresponding entry point.

For the example shown, the microinstructions at addresses 50 through 53 would be the fetch sequence, with 53 being the sequence completion. The JMAP control instruction would be contained in the pipeline register with the mapping PROM generating an address 90. Address 90 would be selected by the IDM2910A as the next address to be presented to microprogram memory.

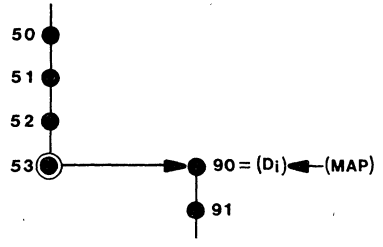


Figure 10. JUMP MAP (JMAP)

Control Instruction 3

CJP (Conditional Jump Pipeline) — This control instruction derives its branch address from the pipeline register branch address field (BR_0 through BR_{11}). See the typical microcomputer system, Figure 11. A technique is thus provided for branching to various microprogram sequences depending upon the state of the condition code inputs ($\overline{CCEN}$ and $\overline{CC}$). State-machines may be designed to execute tests on various inputs and to wait for the condition to go true. When the condition does go true, the system branches and performs a specific function. When the branch occurs, the particular input is usually reset until some point in the future. With CCEN high, this control instruction is the one to use for unconditional jumps.

The example illustrates a conditional jump via the address value defined by the microprogram word located at address 52. When the contents of address 52 are in the pipeline register, the next address passed through the IDM2910A will be either address 53 or address 30, depending upon the state of the condition code input. If the test passes, the address value in the pipeline register (address 30) will be selected by the IDM2910A. If the test fails, the next sequential address (address 53) contained in the micro address register (μAR) will be selected.

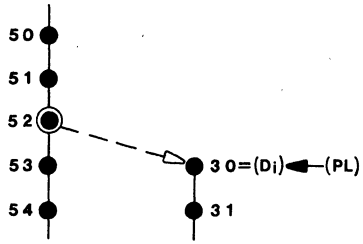


Figure 11. COND JUMP PL (CJP)

Control Instruction 4

PUSH (Unconditional Push/Conditional Load Counter) — This control instruction is primarily used to set up microprogram loops in the microprogram. As shown in Figure 12, when microcode word 52 is in the pipeline register, a push operation is performed on the stack and depending upon the condition code inputs, the register/counter is loaded. A push operation causes the next sequential address (address 53) to be pushed onto the stack. If the condition code test fails, the register/counter is not loaded. If the condition code test passes, the register/counter is loaded with the address value in the pipeline register branch address field. In this manner, a single control instruction can set up a microprogram loop to be executed a specific number of times. While setup is being performed the IDM2910A will unconditionally select the next sequential address contained in the micro address register to be presented to the memory. Control instruction 8 (RFCT) describes the use of the pushed value and the register/counter contents for looping.

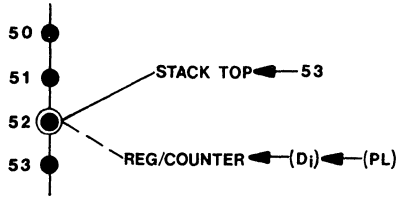


Figure 12. PUSH, COND LD CNTR (PUSH)

Control Instruction 5

JSRP (Conditional Jump-to-Subroutine) — This control instruction is a conditional jump to a subroutine via either the contents of the register/counter or the pipeline register.

As shown in Figure 13, a push operation is always performed and one of two microsubroutines is executed. For this example, either the microsubroutine at address 80 or the microsubroutine at location 90 will be executed. A Return-from-Subroutine (CRTN, control instruction 10) at the end of the microsubroutine will pop the return address (location 55) from the stack. In order for this microinstruction control sequence to operate correctly, the next address fields of both microinstructions 53 and 54 must contain the proper address value. As an example, the next address field of microinstruction 53 must contain address value 90 and microinstruction 54 must contain address value 80. Microinstruction 53 must be loaded into the register/counter while microinstruction 54 is in the pipeline register. If a JSRP is executed at address 54 and the condition code test fails, the contents of the register/counter will be passed through the IDM2910A as the address (address 90) of the next microinstruction. If the condition code test passes, the address value in the pipeline register will be passed through the IDM2910A as the address (address 80) of the next microinstruction. Therefore, this control instruction (JSRP) has the capability of selecting one of two microsubroutines, based upon the results of a condition code test.

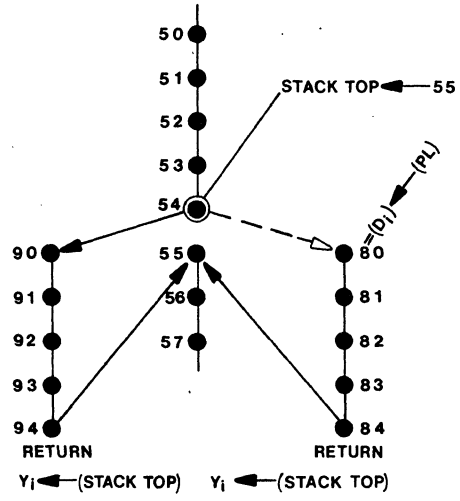


Figure 13. COND JSB R/PL (JSRP)

Control Instruction 6

CJV (Conditional Jump Vector) — This is a conditional jump control instruction. When CJV is executed, the $\overline{\text{VECT}}$ output is enabled and the next microinstruction address is taken from an address generator. The $\overline{\text{VECT}}$ line must control the TRI-STATE® enable line of a register, a buffer, or a PROM, containing the next microprogram address. This instruction provides one technique for performing interrupt type branching at the microprogram level. Since CJV is a conditional control instruction, passing the condition code inputs will allow the vector source address to pass through the IDM2910A. If the condition code test fails the next sequential address will be taken from the address register.

As shown in Figure 14, if CJV is at location 52, and the condition code test passes, microprogram execution will jump to vector address 20 and continue. If the condition code test fails, microprogram execution will continue at address 53.

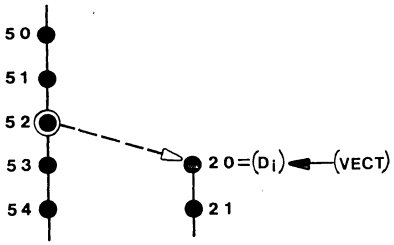


Figure 14. COND JUMP VECTOR (CJV)

Control Instruction 7

JRP (Conditional Jump) — This control instruction is a conditional jump to another routine via the contents of either the register/counter or the pipeline register. JRP is similar to JSRP (control instruction 5), except that no push onto the stack is performed for JRP.

The example shown in Figure 15 shows JRP as a branch to one of two addresses, depending upon the results of the condition code test. Assume the pipeline register contains an address value of 70 when the contents of address 52 are being executed. As the contents of address 53 are clocked into the pipeline register, the address value of 70 is loaded into the register/counter. If the address value of 80 is available when the contents of address 53 are in the pipeline register, either address 70 or address 80 will be passed through the IDM2910A, depending upon the results of the condition code test.

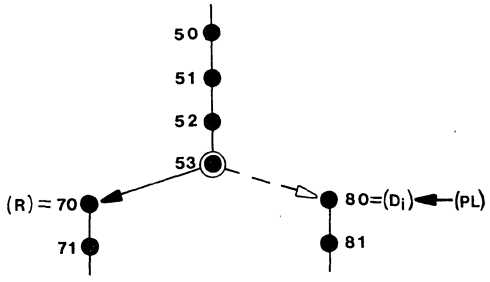


Figure 15. COND JUMP R/PL (JRP)

Control Instruction 8

RFCT (Repeat Loop, Counter Not Equal to Zero) — This control instruction uses the decrementing ability of the register/counter to loop on one or more microinstructions. A preceding instruction, such as PUSH, must have loaded a count value into the register/counter while pushing the next address onto the stack. RFCT tests the register/counter for a non-zero value. If the counter is non-zero, the register/counter is decremented by one and the address of the next instruction is taken from the top of the stack. This sequence will repeat until the register/counter equals zero (the exit condition has been met), causing the next sequential address to be selected ($Y_i = \mu AR$). The stack is popped since looping back is not required anymore.

As shown in Figure 16, a PUSH control instruction would most likely be at address 50. The PUSH will cause address 51 to be pushed onto the stack and will load the register/counter with the count value contained in the pipeline register branch address field.

For this example, the loop test is made at the end of the loop routine (address 54), so the value loaded into the register/counter must be one less than the desired number of passes through the loop. Using the method in the example, a loop may be executed from 1 to 4096 times.

The ability to perform single-microinstruction loops is an efficient way to execute the same microinstruction a specified number of times. Examples are fixed rotates, byte swap, fixed point multiply, and fixed point divide.

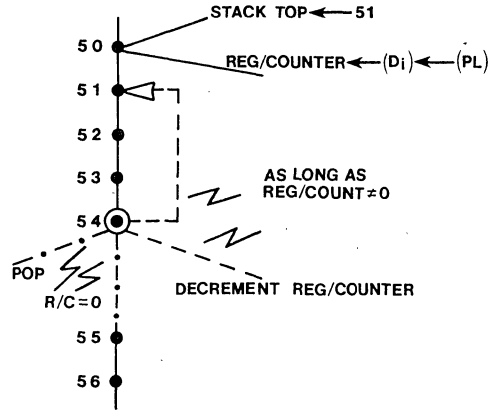


Figure 16. REPEAT LOOP, CNTR ≠ 0 (RFCT)

Control Instruction 9

RPCT (Repeat Pipeline Register, Counter Not Equal to Zero) — This control instruction uses the decrementing ability of the register/counter to loop on one or more microinstructions. RPCT is similar to control instruction RFCT (control instruction 8) except the branch address is taken from the pipeline register whereas RFCT takes it from the file. As long as the register/counter is not zero, RPCT will decrement the value in the register/counter and branch to the address taken from the pipeline register through the D_i inputs. Once the register/counter equals zero, the next address will be selected ($Y_i = \mu AR$). For some cases, this control instruction can be considered to be a one-word extension of the stack. By using RPCT, a microprogram loop using the register/counter can be executed, even though the stack may be completely full. A preceding control instruction must have loaded a count value into the register/counter. RPCT does not perform a pop operation because the stack is not being used.

As shown in Figure 17, microinstruction 51 could be Load Counter and Continue (LDCT, control instruction 12). RPCT is the control instruction at 52 and is shown as a single microinstruction loop. The address in the

pipeline register would be 52. Although a single microinstruction loop is shown, by changing the address in the pipeline register, multi-instruction loops may be performed for a fixed number of times.

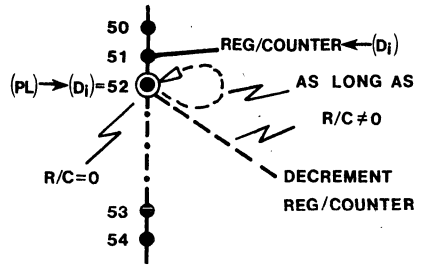


Figure 17. REPEAT PL, CNTR ≠ 0 (RPCT)

Control Instruction 10

CRTN (Conditional Return-from-Subroutine) — This control instruction is used to return from a microsubroutine to the control instruction immediately following the microsubroutine call. CRTN is a conditional return, with the return occurring only if the condition code test passes. If the condition code test fails, the next sequential microinstruction will be executed.

As shown in Figure 18, the use of CRTN is illustrated for both the conditional and the unconditional modes. A Jump-to-Subroutine control instruction is executed at address 52, pushing return address 53 onto the stack and transferring control to address 90. A CRTN is executed at address 93. If the condition code test passes, the microprogram returns to address 53 and the stack is popped. If the condition code test fails, execution continues through to address 97, where the microsubroutine is considered complete. CRTN must now be executed unconditionally. The microinstruction at address 97 is programmed to force $\overline{CCEN}$ high, disabling the condition code test, with the forced pass causing an unconditional return.

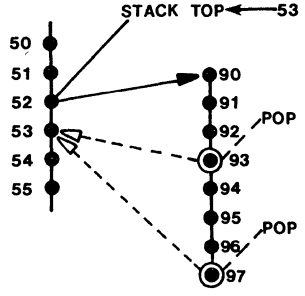


Figure 18. COND RETURN (CRTN)

Control Instruction 11

CJPP (Conditional Jump Pipeline Register Address and Pop Stack — This control instruction provides another method of loop termination and stack maintenance. CJPP is a conditional jump, with the jump occurring only if the condition code test passes. A stack pop will also occur since this jump terminates the loop (whose branch address is located in the stack top).

As shown in Figure 19, a return address is pushed onto the stack and is followed by a short loop. The microinstructions at addresses 52, 53, and 54 are all CJPP control instructions. At address 52, if the condition code test passes, a branch to address 70 and a stack pop will occur. If the condition code test fails, the next sequential address (address 53) will be selected. The same conditions exist for the microinstructions at addresses 53 and 54, with 53 pointing to either address 90 or address 54, and 54 pointing to either address 80 or address 55. Used in this sort of loop, the CJPP control instruction is very useful when several inputs require testing before proceeding to other instructions. This provides the powerful jump-table programming technique at the microprogram level.

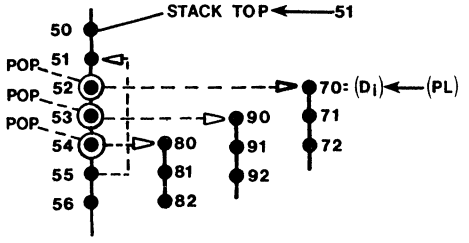


Figure 19. COND JUMP PL & POP (CJPP)

Control Instruction 12

LDCT (Load Counter and Continue) — This control instruction enables the register/counter to be loaded with the value present on the direct input lines. The direct input lines are normally connected to the pipeline register branch address field. For the architecture discussed here, the microinstruction under execution will supply either a branch address or a count value to the register/counter.

There are three methods for loading the register/counter:

1. The conditional load using the PUSH control instruction (number 4).
2. The use of the $\overline{RLD}$ input in conjunction with any of the control instructions.
3. The explicit load using LDCT.

When using $\overline{RLD}$ in conjunction with any other control instruction, any counting or decrementing called for is overridden and a load into the register/counter occurs. The $\overline{RLD}$ input provides additional microinstruction power at the expense of one bit of microinstruction width. LDCT is the exact equivalent of using $\overline{RLD}$ with control microinstruction 14 (CONT). LDCT provides the ability to load the register/counter for those systems in which $\overline{RLD}$ is not under microprogram control.

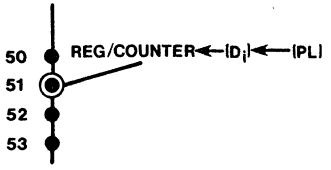


Figure 20. LD CNTR & CONTINUE (LDCT)

Control Instruction 13

LOOP (Test-End-of-Loop) — This control instruction provides a way of conditionally exiting a loop from the bottom. Prior to entering the loop, a branch address must be pushed onto the stack. LOOP will continue to branch back to the address contained on the top of the stack as long as the condition code test fails. When the condition code test passes, the next sequential address is selected ($Y_i = \mu AR$) and the stack is popped.

As shown in Figure 21, the branch address is pushed onto the stack and then the microprogram enters the loop. LOOP is located at address 56. If the condition code test fails, the branch address 52 will be taken from the stack and the program loops to address 52. If the condition code test passes, the loop will terminate and the microinstruction at the next sequential address (taken from the address register) will be executed. Address 52 is popped from the stack once the condition code test passes, thereby performing the required stack maintanance.

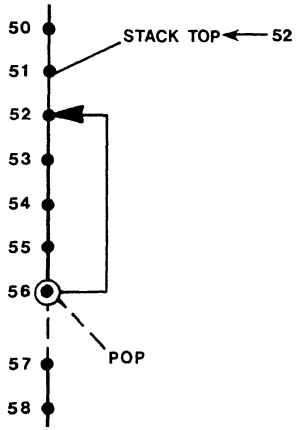


Figure 21. TEST END LOOP (LOOP)

Control Instruction 14

CONT (Continue) — This control instruction increments the address register so the next sequential microinstruction can be executed. CONT should be the default control instruction requested by the firmware when no other control instruction needs performing.

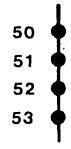


Figure 22. CONTINUE (CONT)

Control Instruction 15

TWB (Three-Way Branch) — This control instruction is the most complex of the 16 IDM2910A control instructions. TWB is a conditional control instruction that can test either the condition code input or the register/counter contents to determine the next branch address. A preceding control instruction, such as a PUSH, must have loaded a count value into the register/counter while pushing the loop branch address onto the stack. As long as the condition code test fails, and the register/counter is not zero, the branch will be to the address on the top of the stack and the register/counter will be decremented. If the register/counter reaches zero, the next branch address is taken from the pipeline register (via the direct input lines). If at any time during the execution of TWB the condition code passes, no branch will occur and the next sequential address will be selected ($Y_i = \mu AR$). Once the loop is exited, for either reason, the stack is popped.

The three-way branch can enhance system performance in a number of ways. Some examples are:

1. Performing a memory search that is terminated either by finding the desired value or by reaching the search limit.
2. Terminating a variable-field-length arithmetic operation upon finding that the contents of the unprocessed portion of the field are all zeros.
3. Performing a key search in a disc controller that is processing variable-length records.
4. Normalizing a floating-point number.

An example of a memory search operation is shown in Figure 23. A PUSH is executed at address 63 to push the return address 64 onto the stack, and to load a count value into the register/counter. The count value must be one less than the number of memory locations to be searched prior to exiting the loop. Address 64 contains a microinstruction that fetches a value from the next memory area to be searched, and compares it with the search key. A test for the results of the search comparison is at address 65. Address 65 also contains TWB for microprogram control. If matching does not occur, the condition code test fails and the microprogram loops back to address 64 to obtain the next search address. Once the register/counter equals zero, the microprogram will branch using the branch address (address 72) taken from the pipeline register. If a match is found during the search, the condition code test will pass during the TWB control instruction and the next sequential address will be taken from the address register. Regardless of which method of exiting the loop is used, the stack will be popped and the loop branch address removed from the top of the stack.

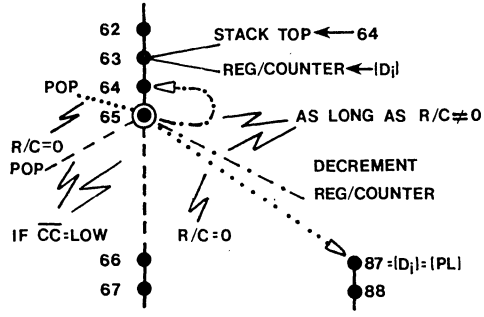


Figure 23. THREE-WAY BRANCH (TWB)

Ordering Information

Package Type	Package Number	Temperature Range	Order Number
Molded DIP	N40A	0°C to +70°C	IDM2910ANC
Hermetic DIP	D40C	0°C to +70°C	IDM2910AJC
Hermetic DIP	D40C	−55°C to +125°C	IDM2910AJM
Hermetic DIP	D40C	−55°C to +125°C	IDM2910AJM/883

National Semiconductor

2900 Family/
Bipolar Microprocessor

IDM29803 16-Way Branch Controller

General Description

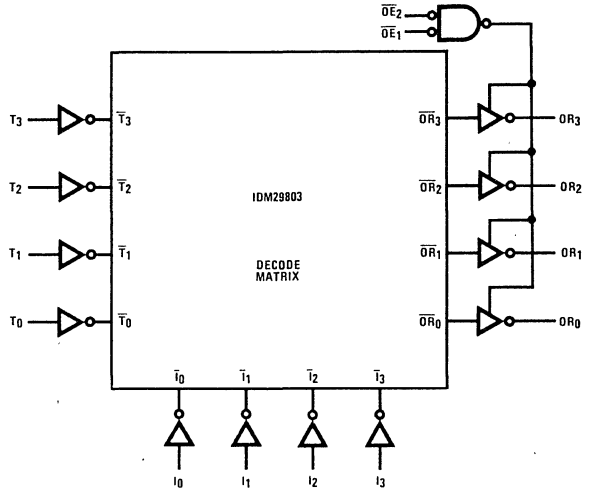
When used in conjunction with the IDM2909A address controller, the IDM29803 provides 16-way branch control. Four different inputs can be tested simultaneously by the 16 instructions of the IDM29803; thus, the four OR inputs of the IDM2909A can be driven by the four outputs of the IDM29803 and a branch can be made to any one of the 16 addresses.

If one test (T) input is being tested, the device will select one of two possible addresses; if two inputs are being tested, the device will select one of four possible addresses and, if three inputs are being tested, one of eight addresses will be selected. If all four inputs are tested, one of sixteen addresses is selected as the field used to drive the OR inputs of the IDM2909A. The "zero" instruction serves as a test inhibit function.

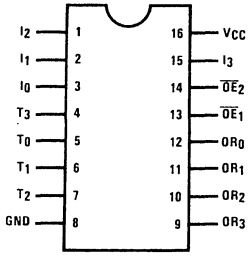
Features and Benefits

- 16 separate instructions – 2-, 4-, 8-, or 16-way branch in one microprogram execution cycle
- Four discrete test inputs
- Four discrete outputs for driving the four OR inputs of the IDM2909A address controller
- Provides a maximum branching capability in a microprogram control unit using the IDM2909A
- Uses low-power Schottky technology
- Meets all requirements of MIL-STD-883

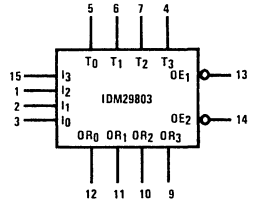
Logic Diagram



Connection Diagram



Logic Symbol



Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +125°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5V
DC Output Current, into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Operating Range

P/N	Ambient Temperature	V_{CC}
Com'l IDM29803DC, NC	0°C to +70°C	4.75V to 5.25V
Mil IDM29803DM, DM/883	−55°C to +125°C	4.50V to 5.50V

DC Electrical Characteristics (Note 2)

PARAMETER		CONDITIONS	Com'l			Mil			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_F	Input Load Current, All Inputs	V_{CC} = Max, V_F = 0.45V		−80	−250		−80	−250	μA
I_R	Input Leakage Current, All Inputs	V_{CC} = Max, V_R = 2.7V			25			25	μA
I_{RB}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{RB} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.45		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
I_{CEX}	Output Leakage Current (Open-Collector Only)	V_{CC} = Max, V_{CEX} = 2.4V			50			50	μA
		V_{CC} = Max, V_{CEX} = 5.5V			100			100	μA
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		80	130		80	130	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 3)	−30	−60	−100	−30	−60	−100	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High	I_{OH} = −2 mA				2.4	3.2		V
		I_{OH} = −6.5 mA	2.4	3.2					V

AC Electrical Characteristics (With standard load)

PARAMETER		CONDITIONS	Com'l			Mil			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{AA}	Address Access Time	*(Figure 1)*	10	35	50	10	35	60	ns
t_{EA}	Enable Access Time	*(Figure 2)*	5	15	25	5	15	30	ns
t_{ER}	Enable Recovery Time	*(Figure 2)*	5	15	25	5	15	30	ns

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 3: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

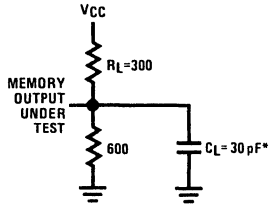
Switching Characteristics Over Operating Range

Symbol	Description	Test Conditions	Com'l Min	Com'l Max	Mil Min	Mil Max	Units
t_{PLH} / t_{PHL}	I_i to OR_i	C_L = 15 pF, R_L = 2.0 kΩ		50		60	ns
t_{PLH} / t_{PHL}	T_i to OR_i			50		60	ns
t_{ZH} / t_{ZL}	OE_i to OR_i			25		30	ns
t_{HZ} / t_{LZ}	OE_i to OR_i			25		30	ns

Definition of Functional Terms

I_0, I_1, I_2, I_3	The four instruction inputs to the device
T_0, T_1, T_2, T_3	The four test inputs for the device
OR_0, OR_1, OR_2, OR_3	The four outputs of the device that are connected to the four OR inputs of the IDM2909A
$\overline{OE}_1, \overline{OE}_2$	Output Enable. When either $\overline{OE}$ input is High, the OR_i outputs are in the high impedance state. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are Low, the OR outputs are enabled and the selected data will be present.

Standard Test Load



*C_L includes probe and jig capacitance

- Input waveforms are supplied by a pulse generator having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50 Ω, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns (between 1.0 V and 2.0 V).
- t_{AA} is measured with both enable inputs at a steady low level.
- t_{EA} and t_{ER} are measured from the 1.5 V on inputs and outputs with all address inputs at a steady level and with the unused enable input at a steady low level.

Switching Time Waveforms

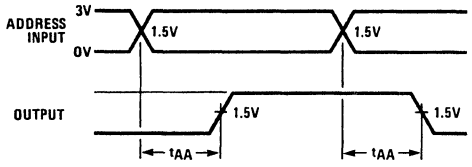


Figure 1. Address Access Time

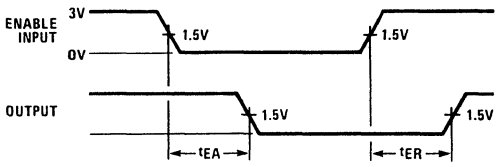


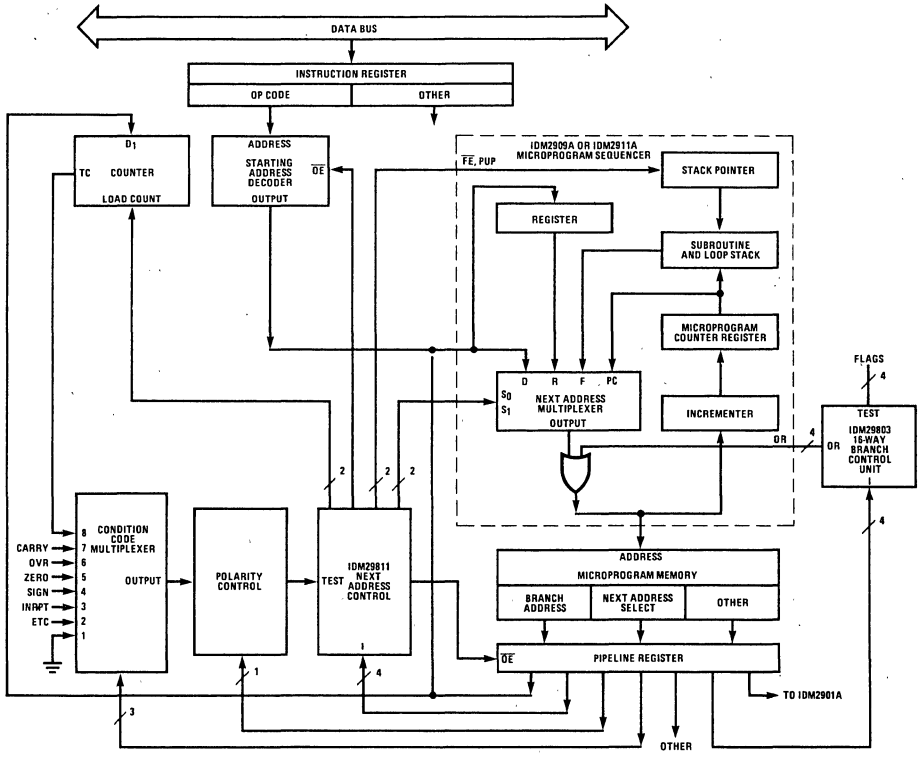
Figure 2. Enable Access Time and Recovery Time

Guaranteed Loading Rules Over Operating Range (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20 μA measured at 2.7 V High and −0.36 mA measured at 0.4 V Low.

Pin Nos.	Input/ Output	Input Load	Output High	Output Low
1	I_2	0.5	–	–
2	I_1	0.5	–	–
3	I_0	0.5	–	–
4	T_3	0.5	–	–
5	T_0	0.5	–	–
6	T_1	0.5	–	–
7	T_2	0.5	–	–
8	GND	–	–	–
9	OR_3	–	100	44
10	OR_2	–	100	44
11	OR_1	–	100	44
12	OR_0	–	100	44
13	OE_1	0.5	–	–
14	OE_2	0.5	–	–
15	I_3	0.5	–	–
16	V_{CC}	–	–	–

Applications Example



Note: The least significant microprogram sequencer is an IDM2909A and the more significant sequencers are IDM2911A's.

A Typical Computer Control Unit Using the IDM2909A, IDM2911A, IDM29803 and IDM29811.

Function Table

Function	I_3	I_2	I_1	I_0	T_3	T_2	T_1	T_0	OR_3	OR_2	OR_1	OR_0
No Test	L	L	L	L	X	X	X	X	L	L	L	L
Test T_0	L	L	L	H	X	X	X	L	L	L	L	L
					X	X	X	H	L	L	L	H
Test T_1	L	L	H	L	X	X	L	X	L	L	L	L
					X	X	H	X	L	L	L	H
Test T_0 & T_1	L	L	H	H	X	X	L	L	L	L	L	L
					X	X	L	H	L	L	L	H
					X	X	H	L	L	L	H	L
					X	X	H	H	L	L	H	H
Test T_2	L	H	L	L	X	L	X	X	L	L	L	L
					X	H	X	X	L	L	L	H
Test T_0 & T_2	L	H	L	H	X	L	X	L	L	L	L	L
					X	L	X	H	L	L	L	H
					X	H	X	L	L	L	H	L
					X	H	X	H	L	L	H	H
Test T_1 & T_2	L	H	H	L	X	L	L	X	L	L	L	L
					X	L	H	X	L	L	L	H
					X	H	L	X	L	L	H	L
					X	H	H	X	L	L	H	H
Test T_0, T_1, & T_2	L	H	H	H	X	L	L	L	L	L	L	L
					X	L	L	H	L	L	L	H
					X	L	H	L	L	L	H	L
					X	L	H	H	L	L	H	H
					X	H	L	L	L	H	L	L
					X	H	L	H	L	H	L	H
					X	H	H	L	L	H	H	L
					X	H	H	H	L	H	H	H
Test T_3	H	L	L	L	L	X	X	X	L	L	L	L
					H	X	X	X	L	L	L	H
Test T_0 & T_3	H	L	L	H	L	X	X	L	L	L	L	L
					L	X	X	H	L	L	L	H
					H	X	X	L	L	L	H	L
					H	X	X	H	L	L	H	H
Test T_1 & T_3	H	L	H	L	L	X	L	X	L	L	L	L
					L	X	H	X	L	L	L	H
					H	X	L	X	L	L	H	L
					H	X	H	X	L	L	H	H
Test T_0, T_1, & T_3	H	L	H	H	L	X	L	L	L	L	L	L
					L	X	L	H	L	L	L	H
					L	X	H	L	L	L	H	L
					L	X	H	H	L	L	H	H
					H	X	L	L	L	H	L	L
					H	X	L	H	L	H	L	H
					H	X	H	L	L	H	H	L
					H	X	H	H	L	H	H	H
Test T_2 & T_3	H	H	L	L	L	L	X	X	L	L	L	L
					L	H	X	X	L	L	L	H
					H	L	X	X	L	L	H	L
					H	H	X	X	L	L	H	H
Test T_0, T_2, & T_3	H	H	L	H	L	L	X	L	L	L	L	L
					L	L	X	H	L	L	L	H
					L	H	X	L	L	L	H	L
					L	H	X	H	L	L	H	H
					H	L	X	L	L	H	L	L
					H	L	X	H	L	H	L	H
					H	H	X	L	L	H	H	L
					H	H	X	H	L	H	H	H
Test T_1, T_2, & T_3	H	H	H	L	L	L	H	X	L	L	L	L
					L	L	H	X	L	L	L	H
					L	H	L	X	L	L	H	L
					L	H	H	X	L	L	H	H
					H	L	L	X	L	H	L	L
					H	L	H	X	L	H	L	H
					H	H	L	X	L	H	H	L
					H	H	H	X	L	H	H	H
Test T_0, T_1, T_2, & T_3	H	H	H	H	L	L	L	L	L	L	L	L
					L	L	L	H	L	L	L	H
					L	L	H	L	L	L	H	L
					L	L	H	H	L	L	H	H
					L	H	L	L	L	H	L	L
					L	H	L	H	L	H	L	H
					L	H	H	L	L	H	H	L
					L	H	H	H	L	H	H	H
					H	L	L	L	H	L	L	L
					H	L	L	H	H	L	L	H
					H	L	H	L	H	L	H	L
					H	L	H	H	H	L	H	H
					H	H	L	L	H	H	L	L
					H	H	L	H	H	H	L	H
					H	H	H	L	H	H	H	L
					H	H	H	H	H	H	H	H

Ordering Information

Package Type	Package Number	Temperature Range	Order Number
Molded DIP	N16A	0°C to +70°C	IDM29803NC
Hermetic DIP	J16A (D16C)	0°C to +70°C	IDM29803JC
Hermetic DIP	J16A (D16C)	−55°C to +125°C	IDM29803JM
Hermetic DIP	J16A (D16C)	−55°C to +70°C	IDM29803JM/883

National Semiconductor

2900 Family/
Bipolar Microprocessor

IDM29811 Next-Address Controller

General Description

The IDM29811 next-address control unit is specifically designed for next address control of the IDM2911A sequencer. The device can be used in high-performance computer control systems, structured state machine designs, or in other applications that utilize microprogramming techniques.

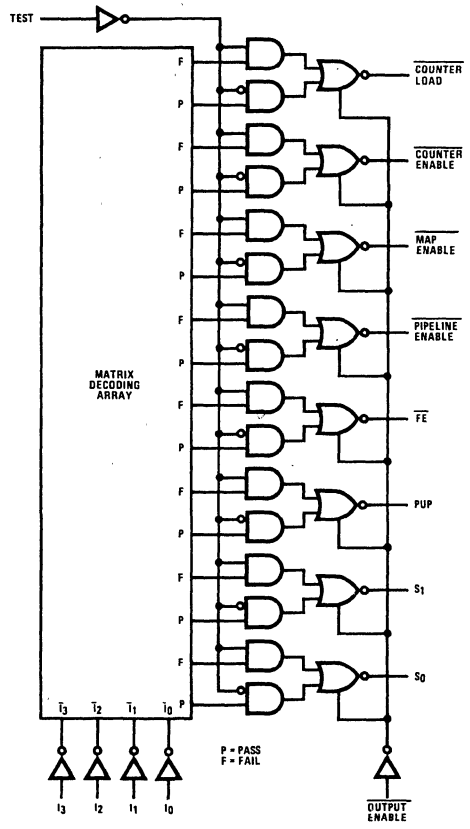
A 4-bit instruction field (I_3-I_0) provides sixteen instructions; also, a test input is available for conditional instructions. Among the conditional instructions that can be executed are: conditional jumps, conditional jump to subroutine, conditional return from subroutine, conditional repeat loops, conditional branch to starting address, and so on.

A single IDM29811 can be used to control any number of IDM2911A sequencers. Using one IDM29811 and three IDM2911As, a sequencer capable of controlling 4k of microprogram memory can be easily implemented.

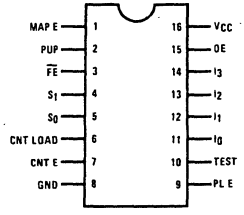
Features and Benefits

- 16 next-address instructions
- Test input for conditional instructions
- Separate outputs to control the IDM2911A, an independent event counter, and a mapping PROM/branch address interface
- Uses low-power Schottky technology
- Meets all requirements of MIL-STD-883

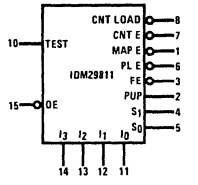
Logic Diagram



Connection Diagram



Logic Symbol



Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +6.3V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +5.5V
DC Output Current, into Outputs	30mA
DC Input Current	−30mA to +5.0mA

Operating Range

P/N	Ambient Temperature	V_{CC}
Com'l IDM29811JC,NC	0°C to +70°C	4.75V to 5.25V
Mil IDM29811JM,JM/883	−55°C to +125°C	4.50V to 5.50V

DC Electrical Characteristics (Note 2)

PARAMETER		CONDITIONS	Com'l			Mil			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
I_{IL}	Input Load Current, All Inputs	V_{CC} = Max, V_{IN} = 0.45V		−80	−250		−80	−250	μA
I_{IH}	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 2.7V			25			25	μA
I_I	Input Leakage Current, All Inputs	V_{CC} = Max, V_{IN} = 5.5V			1.0			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
V_{IL}	Low Level Input Voltage				0.80			0.80	V
V_{IH}	High Level Input Voltage		2.0			2.0			V
V_C	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA		−0.8	−1.2		−0.8	−1.2	V
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz		4.0			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "OFF"		6.0			6.0		pF
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs Grounded, All Outputs Open		70	110		70	110	mA
TRI-STATE PARAMETERS									
I_{SC}	Output Short Circuit Current	V_O = 0V, V_{CC} = Max, (Note 3)	−20	−45	−70	−20	−45	−70	mA
I_{HZ}	Output Leakage (TRI-STATE)	V_{CC} = Max, V_O = 0.45 to 2.4V, Chip Disabled			±50			±50	μA
V_{OH}	Output Voltage High,	I_{OH} = −2 mA				2.4	3.2		V
		I_{OH} = −6.5 mA	2.4	3.2					V

Note 1: Absolute maximum ratings are those values beyond which the device may be permanently damaged. They do not mean that the device may be operated at these values.

Note 2: These limits apply over the entire operating range unless stated otherwise. All typical values are for V_{CC} = 5V and T_A = 25°C.

Note 3: During I_{SC} measurement, only one output at a time should be grounded. Permanent damage may otherwise result.

Switching Characteristics Over Operating Temperature

			Com'l		Mil		
Symbol	Description	Test Conditions	Min.	Max.	Min.	Max.	Units
t_{PLH}	I_i to Any Output	C_L = 15 pF R_L = 2.0 kΩ		30		40	ns
t_{PHL}							
t_{PLH}	Test to Any Output			30		40	ns
t_{PHL}							
t_{ZH}	OE to Any Output			20		30	ns
t_{ZL}							
t_{HZ}	OE to Any Output			20		30	ns
t_{LZ}							

Pinout Descriptions

$I_3/I_2/I_1/I_0$	Four instruction inputs
Test	Condition-code input. When test input is low, the device assumes test has failed; when input is high, the test is assumed to have passed. In either case, a branch is made to one of the conditional-code instructions; refer to the tables which follow.
Counter Load	An output used to drive the parallel load input of an up/down counter.
Counter Enable	An output used to drive the enable input of an up/down counter.
Map Enable	An output that controls the three-state outputs of the mapping PROM or PLA used to provide the initial starting address for each machine instruction.
Pipeline Enable	An output used to control the three-state output of the pipeline register which contains the branch address of the computer control unit.
FE File Enable	An output used to drive the file enable input of the IDM2911A. When this output is low, a stack operation will take place.
PUP	An output used to drive the push/pop input of the IDM2911A address controller. When the PUP output is high, a push will take place if the file is enabled. When the PUP output is low, a pop will take place if the file is enabled.
S_0/S_1	These outputs are used to drive the S_0/S_1 inputs of the IDM2911A address controller. These outputs control whether the direct input, the register, the microprogram counter, or the stack is selected as the source of the next address for the microprogram memory.

Instruction Table

Mnemonic	I_3	I_2	I_1	I_0	Instruction
JZ	L	L	L	L	Jump to Address Zero
CJS	L	L	L	H	Conditional Jump-to-Subroutine with Jump Address in Pipeline Register
JMAP	L	L	H	L	Jump to Address at Mapping PROM Output
CJP	L	L	H	H	Conditional Jump to Address in Pipeline Register
PUSH	L	H	L	L	Push Stack and Conditionally Load Counter
JSRP	L	H	L	H	Jump-to-Subroutine with Starting Address Conditionally Selected from IDM2911A Register or Pipeline Register
CJV	L	H	H	L	Conditional Jump to Vector Address
JRP	L	H	H	H	Jump to Address Conditionally Selected from IDM2911A R-Register or Pipeline Register
RFCT	H	L	L	L	Repeat Loop if Counter is Not Equal to Zero
RPCT	H	L	L	H	Repeat Pipeline Address if Counter is Not Equal to Zero
CRTN	H	L	H	L	Conditional Return-from-Subroutine
CJPP	H	L	H	H	Conditional Jump to Pipeline Address and Pop Stack
LDCT	H	H	L	L	Load Counter and Continue
LOOP	H	H	L	H	Test End of Loop
CONT	H	H	H	L	Continue to Next Address
JP	H	H	H	H	Jump to Pipeline Register Address

Function Table

	Inputs						Outputs				
	Instruction					Test	Next ADDR				
Mnemonic	I_3	I_2	I_1	I_0	Function	Input	Source	File	Counter	MAP E	PL E
JZ	L	L	L	L	JUMP ZERO	K	D	HOLD	LL*	H	L
CJS	L	L	L	H	COND JSB PL	L H	PC D	HOLD PUSH	HOLD HOLD	H H	L L
JMAP	L	L	H	L	JUMP MAP	X	D	HOLD	HOLD	L	H
CJP	L	L	H	H	COND JUMP PL	L H	PC D	HOLD HOLD	HOLD HOLD	H H	L L
PUSH	L	H	L	L	PUSH/COND LD CNTR	L H	PC PC	PUSH PUSH	HOLD LOAD	H H	L L
JSRP	L	H	L	H	COND JSB R/PL	L H	R D	PUSH PUSH	HOLD HOLD	H H	L L
CJV	L	H	H	L	COND JUMP VECTOR	L H	PC D	HOLD HOLD	HOLD HOLD	H H	H H
JRP	L	H	H	H	COND JUMP R/PL	L H	R D	HOLD HOLD	HOLD HOLD	H H	L L
RFCT	H	L	L	L	REPEAT LOOP, CNTR $\neq 0$	L H	F PC	HOLD POP	DEC HOLD	H H	L L
RPCT	H	L	L	H	REPEAT PL, CNTR $\neq 0$	L H	D PC	HOLD HOLD	DEC HOLD	H H	L L
CRTN	H	L	H	L	COND RTN	L H	PC F	HOLD POP	HOLD HOLD	H H	L L
CJPP	H	L	H	H	COND JUMP PL & POP	L H	PC D	HOLD POP	HOLD HOLD	H H	L L
LDCT	H	H	L	L	LOAD CNTR & CONTINUE	X	PC	HOLD	LOAD	H	L
LOOP	H	H	L	H	TEST END LOOP	L H	F PC	HOLD POP	HOLD HOLD	H H	L L
CONT	H	H	H	L	CONTINUE	X	PC	HOLD	HOLD	H	L
JP	H	H	H	H	JUMP PL	X	D	HOLD	HOLD	H	L

L = Low
H = High
X = Don't Care

DEC = Decrement
*LL = Special Case

Truth Table

Mnemonic	Function	Pin No.	14	13	12	11	10	4	5	3	2	6	7	1	9
			Inputs					Outputs							
								Next ADDR Source		File		Counter			
			I_3	I_2	I_1	I_0	TEST	S_1	S_0	$\overline{FE}$	PUP	LOAD	$\overline{EN}$	$\overline{MAP\ E}$	$\overline{PL\ E}$
JZ	JUMP ZERO		L	L	L	L	L	H	H	H	H	L	L	H	L
			L	L	L	L	H	H	H	H	H	L	L	H	L
CJS	COND JSB PL		L	L	L	H	L	L	L	H	H	H	H	H	L
			L	L	L	H	H	H	H	L	H	H	H	H	L
JMAP	JUMP MAP		L	L	H	L	L	H	H	H	H	H	H	L	H
			L	L	H	L	H	H	H	H	H	H	H	L	H
CJP	COND JUMP PL		L	L	H	H	L	L	L	H	H	H	H	H	L
			L	L	H	H	H	H	H	H	H	H	H	H	L
PUSH	PUSH/COND LD CNTR		L	H	L	L	L	L	L	L	H	H	H	H	L
			L	H	L	L	H	L	L	L	H	L	H	H	L
JSRP	COND JSB R/PL		L	H	L	H	L	L	H	L	H	H	H	H	L
			L	H	L	H	H	H	H	L	H	H	H	H	L
CJV	COND JUMP VECTOR		L	H	H	L	L	L	L	H	H	H	H	H	H
			L	H	H	L	H	H	H	H	H	H	H	H	H
JRP	COND JUMP R/PL		L	H	H	H	L	L	H	H	H	H	H	H	L
			L	H	H	H	H	H	H	H	H	H	H	H	L
RFCT	REPEAT LOOP, CTR ≠ 0		H	L	L	L	L	H	L	H	L	H	L	H	L
			H	L	L	L	H	L	L	L	L	H	H	H	L
RPCT	REPEAT PL, CTR ≠ 0		H	L	L	H	L	H	H	H	H	H	L	H	L
			H	L	L	H	H	L	L	H	H	H	H	H	L
CRTN	COND RTN		H	L	H	L	L	L	L	H	L	H	H	H	L
			H	L	H	L	H	H	L	L	L	H	H	H	L
CJPP	COND JUMP PL & POP		H	L	H	H	L	L	L	H	L	H	H	H	L
			H	L	H	H	H	H	H	L	L	H	H	H	L
LDCT	LD CNTR & CONTINUE		H	H	L	L	L	L	L	H	H	L	H	H	L
			H	H	L	L	H	L	L	H	H	L	H	H	L
LOOP	TEST END LOOP		H	H	L	H	L	H	L	H	L	H	H	H	L
			H	H	L	H	H	L	L	L	L	H	H	H	L
CONT	CONTINUE		H	H	H	L	L	L	L	H	H	H	H	H	L
			H	H	H	L	H	L	L	H	H	H	H	H	L
JP	JUMP PL		H	H	H	H	L	H	H	H	H	H	H	H	L
			H	H	H	H	H	H	H	H	H	H	H	H	L

L = Low, H = High

Guaranteed Loading Characteristics Over Operating Range (in unit loads)

Pin Nos.	Input/ Output	Input Load	Output High	Output Low
1	MAP E	–	100	44
2	PUP	–	100	44
3	$\overline{FE}$	–	100	44
4	S_1	–	100	44
5	S_0	–	100	44
6	CNT LOAD	–	100	44
7	CNT E	–	100	44
8	GND	–	–	–
9	PL E	–	100	44
10	TEST	0.5	–	–
11	I_0	0.5	–	–
12	I_1	0.5	–	–
13	I_2	0.5	–	–
14	I_3	0.5	–	–
15	OE	–	100	44
16	V_{CC}	–	–	–

A Low-Power Schottky TTL Unit Load is defined as 20 μA measured at 2.7V High and −0.36 mA measured at 0.4V Low.

National Semiconductor

2900 Family/
Bipolar Microprocessor
PRELIMINARY

DM10900 8-Bit Parity ALU Slice

General Description

The DM10900 8-Bit Microprocessor slice is a cascadable device designed for use in high performance central processing units, microprogrammable controllers, and other applications where hardware/software flexibility, ease of expansion, and ECL 10k compatibility are system requirements. The building block architecture and microinstruction format of the DM10900 permits efficient emulation of most digital systems.

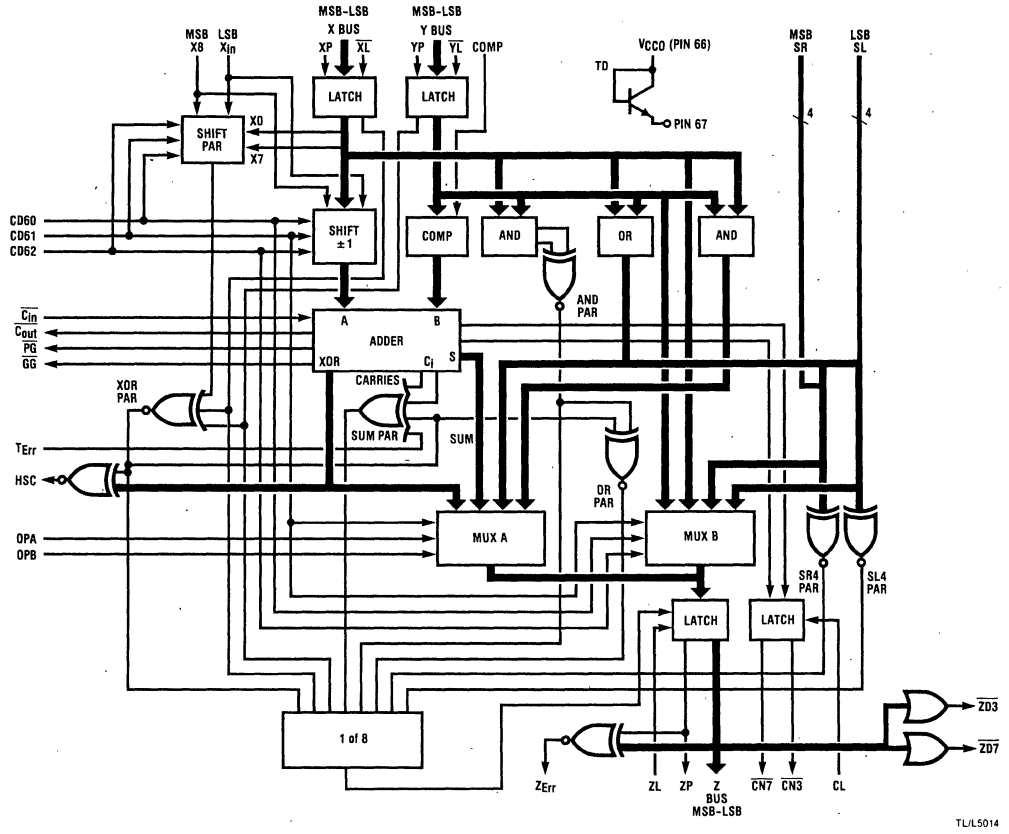
As shown in the block diagram below, the DM10900 consists of a parallel 8-bit adder accessed by two latched input ports. In addition, various logic operations can also be performed on the input data. Shifting circuits and parity detect circuits implemented with ECL, oxide-isolated technology, allow the device to function as a very powerful, high performance ALU.

Features

- Manufactured from high performance, oxide-isolated ECL macrocell array.
- Performs all necessary logic and arithmetic operations.
- Dual port architecture—two 8-bit, latched input ports; one 8-bit, latched output port.
- Internal look-ahead carry with propagate/generate outputs.
- Internal parity detect circuit with parity error output.
- Expandable in 4- or 8-bit increments to form larger word sizes.

Block Diagram

DM10900



Test Temperature

Symbol	0°C	+25°C	+70°C
$V_{IH\ max}$	−0.840	−0.810	−0.730
$V_{IHA\ min}$	−1.145	−1.105	−1.050
$V_{IL\ min}$	−1.95	−1.95	−1.95
$V_{ILA\ max}$	−1.490	−1.475	−1.450
V_{EE}	−5.2	−5.2	−5.2

(A) indicates the most positive value.

Recommended Operating Conditions

V_{EE}	Supply Voltage ($V_{CC} = 0V$)	$-4.68V_{DC}$ to $-5.72V_{DC}$
T_A	Operating Temperature (Functional)	0 to +70°C
	Output Drive	50Ω to $-2.0V_{DC}$
T_J	Junction Temperature	130°C Max.

Electrical Characteristics

Each ECL 10,000 series circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 1000 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to −2.0V. Test procedures are shown for only one input, or for one set of input conditions. Other inputs are tested in the same manner.

Symbol	Parameters	Pin Under Test	DM10900 Test Limits								Voltage Applied to Pins Listed Below:					(V_{CCO}) (V_{CC}) Gnd
			0°C		+25°C			+70°C								
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Unit	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	
I_{EE}	Power Supply Drain Current	9, 43	514	855	514	685	855	514	855	mA_{DC}	—	—	—	—		
I_{INH}	Input Current CD61, $\overline{XL}$, $\overline{YL}$, ZL, $\overline{C_{IN}}$, OPA	55	—	600	—	—	600	—	600	μA_{DC}	—	—	—	—		
	All Others	50	—	250	—	—	250	—	250		50	—	—	—		
I_{INL}		50	0.5	—	0.5	—	—	0.5	—		—	50	—	—		
V_{OH}	Logic High Output Voltage	4	−1.000	−0.840	−0.960	—	−0.810	−0.905	−0.730	V_{DC}	50, 55, 24	31, 56, 54			9, 43	3, 15, 20 26, 60, 68
V_{OL}	Logic Low Output Voltage	4	−1.95	−1.665	−1.95	—	−1.650	−1.95	−1.625	V_{DC}	55, 24	50, 31, 56, 54	—	—		
V_{OHA}	Logic High Threshold Voltage	4	−1.02	—	−0.980	—	—	−0.925	—	V_{DC}	55, 24	31, 56, 54	50	—		
V_{OLA}	Logic Low Threshold Voltage	4	—	−1.645	—	—	−1.630	—	−1.605	V_{DC}	24, 55	31, 54, 56	—	50		

DM10900

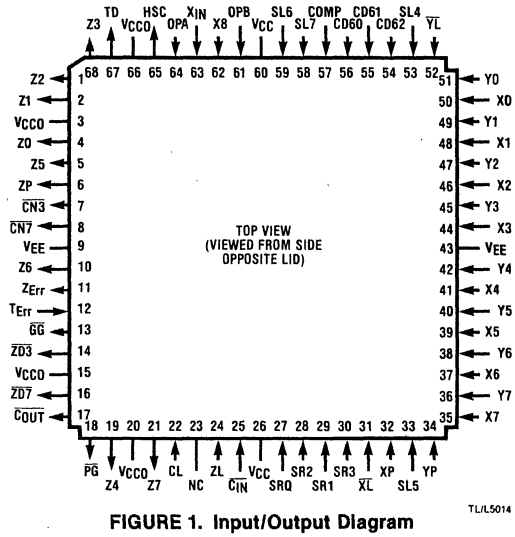


FIGURE 1. Input/Output Diagram

DM10900 Grid Array Package
Drawing Not Available at This Time

Table 1. Pin Assignments

Pin Description	Pin Number	Description
X0	50	Input Bus—LSB Input
X1	48	Input Bus
X2	46	Input Bus
X3	44	Input Bus
X4	41	Input Bus
X5	39	Input Bus
X6	37	Input Bus
X7	35	Input Bus—MSB Input
$\overline{X8}$	62	Shift Interconnect—MSB
$\overline{XL}$	31	X Latch Control Bit
XP	32	X Input Parity Bit
X_{IN}	63	Shift Interconnect—LSB
Y0	51	Input Bus—LSB Input
Y1	49	Input Bus
Y2	47	Input Bus
Y3	45	Input Bus
Y4	42	Input Bus
Y5	40	Input Bus
Y6	38	Input Bus
$\overline{Y7}$	36	Input Bus—MSB Input
$\overline{YL}$	52	Y Latch Control Bit
YP	34	Y Input Parity Bit
$\overline{C_{IN}}$	25	Carry Input
$\overline{C_{OUT}}$	17	Carry Output
$\overline{PG}$	18	Group Propagate Output
$\overline{GG}$	13	Group Generate Output
$\overline{C_{n3}}$	7	Detect System Overflow
$\overline{C_{n7}}$	8	Detect System Overflow
SR0	27	Shift Right Input to Z4
SR1	29	Shift Right Input to Z5
SR2	28	Shift Right Input to Z6
SR3	30	Shift Right Input to Z7
SL4	53	Shift Left Input to Z0
SL5	33	Shift Left Input to Z1

Pin Description	Pin Number	Description
SL6	59	Shift Left Input to Z2
SL7	58	Shift Left Input to Z3
Z0	4	Output Bus—LSB Output
Z1	2	Output Bus
Z2	1	Output Bus
Z3	68	Output Bus
Z4	19	Output Bus
Z5	5	Output Bus
Z6	10	Output Bus
$\overline{Z7}$	21	Output Bus—MSB Output
$\overline{ZD3}$	14	Zero Detect
$\overline{ZD7}$	16	Zero Detect
ZP	6	Parity Detect Output
ZL	24	Z Latch Control Bit
Z_{Err}	11	Bus Error Detect Output
T_{Err}	12	Test Error Input
Comp	57	Control Input Complement
CD60	56	Control Input
CD61	55	Control Input
CD62	54	Control Input
HSC	65	Half Sum Check Output
OPA	64	Control Input
OPB	61	Control Input
V_{EE}	9	−5.2 Volt Supply
V_{EE}	43	−5.2 Volt Supply
V_{CC}	26	Ground
V_{CC}	60	Ground
V_{CCO}	3	Ground
V_{CCO}	15	Ground
V_{CCO}	20	Ground
V_{CCO}	66	Ground
CL	22	Carry Latch Enable
NC	23	Not Used
TD	67	Test Diode

Operation

The basic data input ports to the DM10900 are the X bus and Y bus, each capable of accepting eight data bits. To expand the word size of a DM10900 system, single-bit data paths C_{IN}, C_{OUT}, X_{IN}, and X8 along with 4-bit paths SL and SR are provided. In addition, group propagate and group generate outputs can be used with external carry look-ahead logic in an expanded system for faster operation.

The DM10900 outputs data on the Z bus and provides zero detect signals $\overline{ZD7}$ for outputs Z7–Z4 and $\overline{ZD3}$ for outputs Z3–Z0. In addition, carry signals $\overline{CN3}$ and $\overline{CN7}$ are generated within the adder for determining overflow conditions. Parity circuitry continuously monitors data flow within the ALU slice and provides two error signals.

Each input and output port consists of eight data bits and one odd parity bit. The two input ports are latched and routed to four logic networks which generate a 1-bit shift right or left of X, a complement of Y, a logic OR of X and Y, and a logic AND of X and Y. The shift and complement circuits input to the adder network which provides the arithmetic sum and the logic exclusive-OR. Two 1-of-4 multiplexers select the data path to the Z output bus.

Pin Descriptions

1. **X Input Bus.** These eight data input pins serve as data paths to an internal latch in the ALU. Data is passed through the latch when Latch Control bit, $\overline{XL}$, is brought low and latched when $\overline{XL}$ is brought high. X7 is the most significant bit (MSB) of the X input bus.

2. **Y Input Bus.** These eight data input pins operate identically to the X input bus described above. $\overline{YL}$ is the latch control signal for the Y input bus.

3. **Parity Inputs, XP and YP.** To utilize the parity detect circuitry of the DM10900, parity for X input data and Y input data should be entered on the XP and YP inputs respectively. These bits are used in determining the Z parity output, ZP, and parity error signals, HSC and Z_{Err}.

4. **Shift Interconnects.** Shift interconnect signals X_{IN}, X8, SL and SR are provided to facilitate shift operations in cascaded slice systems.

   For a single-bit shift left, X_{IN} is shifted into the X0 position and for a single-bit shift right, X8 is shifted into the X7 position. SL and SR are used for 4-bit shifts. For a shift left, SL7–SL4 are shifted into Z3–Z0 respectively, while the results of the OR circuit, $(X+Y)_3 - (X+Y)_0$ are shifted into Z7–Z4, respectively. For a shift right, SR3–SR0 are shifted into Z7–Z4, respectively, while the OR circuit outputs $(X+Y)_7 - (X+Y)_4$ are shifted into Z3–Z0, respectively.

5. **Half Sum Check.** HSC is a parity check of the X bus and Y bus along with an error check of the half sum adder network. HSC will detect a single-bit error or any combination of odd number of errors. Half sums are derived from the bit-by-bit Exclusive-OR of the two busses. The half sum bits, along with the input parity bits XP and YP, determine HSC as follows:

   $HSC = HS7 \oplus GS6 \oplus HS5 \oplus HS4 \oplus HS3 \oplus HS2 \oplus HS1 \oplus HS0 \oplus XP \oplus YP \oplus Shift\ PAR$

6. **Carry Signals.** System overflow can be detected by the carry signals $\overline{CN3}$ and $\overline{CN7}$. Overflow occurs when the maximum system word or byte value has been exceeded. Only the overflow from the most significant 8-bit slice is used in a typical system.

   Overflow is detected by the exclusive-OR of the carry out and carry in of the most significant bit in a system. In an 8-bit increment system (8, 16, 24, etc.) overflow can be generated by the exclusive-OR of $\overline{C_{OUT}}$ and $\overline{CN7}$. In a 4-bit increment system (4, 12, 16, etc.) overflow can be generated by the Exclusive-NOR of Z4 and $\overline{CN3}$ ($OF = Z4 \oplus \overline{CN3}$). Z4 is effectively the carry out of the 8-bit slice operating in a 4-bit slice mode.

   Carry in, $\overline{C_{IN}}$, is used to interconnect 8-bit slices in a system. In a ripple carry mode, $\overline{C_{IN}}$ is connected to the carry out, $\overline{C_{OUT}}$, of the previous slice. $\overline{C_{OUT}}$ occurs when the calculated value within the ALU exceeds the maximum capacity, a binary count over 255. $\overline{C_{OUT}}$ is generated by look-ahead carry logic in the 8-bit ALU.

7. **Output Z Bus.** These eight data output pins connect the output data latch to the external system. Data passes through the latch to the Z bus when ZL is high. Z7 is the most significant output bit.

8. **Zero Detect.** $\overline{ZD7}$ and $\overline{ZD3}$ indicate all lows on output latch Z7–Z4 and Z3–Z0, respectively. These outputs go low when their corresponding output bits are all low.

9. **Z Bus Error.** Z_{Err} indicates a single-bit error (or odd number of multiple errors) in data flowing through the multiplexers or output latch. The output parity bit, ZP, is compared with the parity of the Z bus output generating a logic high on Z_{Err} if an error exists.

   Z_{Err} can be tested with the test error input, T_{Err}, when an arithmetic operation is performed. When enabled, a logic high on T_{Err} will result in an incorrect parity of the arithmetic operation output Sum. This will be detected by the Z bus error logic as shown in the block diagram.

10. **Parity Output.** ZP is used to output the parity of the Z bus. It is generated independently of the Z bus, which adds another level of system error check.

    ZP is the Exclusive-OR of the selected function before multiplexing onto the Z bus. For example, if the ALU were performing an AND operation, ZP would be:

    $ZP = XY7 \oplus XY6 \oplus XY5 \oplus \ldots \oplus XY0$

11. **Group Propagate/Generate.** Group propagate, $\overline{PG}$, and group generate, $\overline{GG}$, are used as inputs to external look-ahead carry logic for carry in signals that can be obtained with faster ripple techniques. The propagate output goes low when the maximum value occurs on the ALU outputs (255). Group generate occurs with a value of 256 or greater. These signals are useful only with arithmetic operations.

12. **Test Diode.** A test diode, TD, is connected to Pin 67 for use in measuring junction temperature. Pin 66 is the diode anode; Pin 67 the diode cathode.

Select Line Operation

One-Bit Shift Select

Control inputs CD60, CD61, and CD62 are used to give the ECL 8-bit slice a 1-bit shift left or a 1-bit shift right. A logic L on CD62 results in a 1-bit shift left whereas a logic H results in a 1-bit shift right operation. When CD60 is held at a logic L or CD61 is held at a logic H, no shift operation is performed. Table 2 illustrates the 1-bit shift operation.

Table 2

Operation	CD60	CD61	CD62
No Shift	L	X	X
No Shift	X	H	X
1-Bit Shift Left	H	L	L
1-Bit Shift Right	H	L	H

Mux B Select

Control inputs CD60, CD61, and CD62 are used to select the data path to the ALU output latch. When CD61 is held at a logic H, Mux B is enabled. CD60 and CD62 select ALU functions pass X, pass Y, shift left four bits or shift right four bits. (See Table 3.)

Table 3

Function	ZP	CD61	CD60	CD62
Not Enabled	See Table 4	L	X	X
Pass X	XP	H	L	L
Pass Y	YP	H	L	H
Shift Left 4 Bits	SL4 PAR	H	H	L
Shift Right 4 Bits	SR4 PAR	H	H	H

$SL4\ PAR = [SL4 \oplus SL5\ SL6 \oplus SL7]\overline{\oplus}$
$[(X0 + Y0) \oplus (X1 + Y1) \oplus (X2 + Y2) \oplus (X3 + Y3)]$
$SR4\ PAR = [SR0 \oplus SR1 \oplus SR2 \oplus SR3]\overline{\oplus}$
$[(X4 + Y4) \oplus (X5 + Y5) \oplus (X6 + Y6) \oplus (X7 + Y7)]$

Mux A Select

Control inputs OPA, OPB, and CD61 are used to select the data path to the ALU output latch. When CD61 is held at a logic L, Mux A is enabled, OPA and OPB select ALU functions Sum, XOR, X + Y, or X • Y (see *Figure 11*). See Table 4.

Table 4

Function	ZP	CD61	OPA	OPB
Not Enabled	See Table 3	H	X	X
Sum	Sum PAR	L	L	L
XOR	XOR PAR	L	L	H
X • Y	AND PAR	L	H	L
X + Y	OR PAR	L	H	H

$XOR\ PAR = (Shift\ PAR)\overline{\oplus}[XP \oplus YP]$ where
$Shift\ PAR = [X7 \oplus X_{IN}) \bullet \overline{CD62} + (X8 \oplus X0) \bullet$
$CD62] \bullet CD60 \bullet CD61$
$AND\ PAR = [(X0 \bullet Y0) \oplus (X1 \bullet Y1) \oplus (X2 \bullet Y2) \oplus$
$(X3 \bullet Y3)]\overline{\oplus}[(X4 \bullet Y4) \oplus (X5 \bullet Y5) \oplus$
$(X6 \bullet Y6) \oplus (X7 \bullet Y7)]$
$OR\ PAR = (AND\ PAR)\overline{\oplus}(XOR\ PAR)$
$Sum\ PAR = C_{IN} \oplus C1 \oplus C2 \oplus C3 \oplus C4 \oplus C5 \oplus$
$C6 \oplus C7 \oplus T_{Err} \oplus (XOR\ PAR)$
where C_{IN} is the carry-in for generating bit Z_I for I = 1 to 7.

Complement Y Select

Control input Comp inhibits or enables the complement operation. When Comp is at a logic L, Y data is passed. When Comp is at a logic H, Y is complemented.

Table 5

Operation	Comp
Pass Y	L
Complement Y	H

Table 6

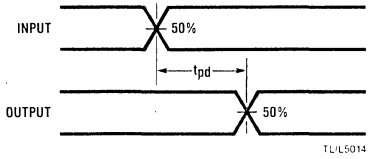
Function	ZP	CD61	CD60	CD62	OPA	OPB	Comp
$X + Y + C_{IN}$	Sum PAR	L	L	X	L	L	L
$X + \overline{Y} \oplus C_{IN}$	Sum PAR	L	L	X	L	L	H
$X \oplus Y$	XOR PAR	L	L	X	L	H	L
$X \oplus \overline{Y}$	XOR PAR	L	L	X	L	H	H
$XSL + Y + C_{IN}$	Sum PAR	L	H	L	L	L	L
$XSL + \overline{Y} + C_{IN}$	Sum PAR	L	H	L	L	L	H
$XSL \oplus Y$	XOR PAR	L	H	L	L	H	L
$XSL \oplus \overline{Y}$	XOR PAR	L	H	L	L	H	H
$XSR + Y + C_{IN}$	Sum PAR	L	H	H	L	L	L
$XSR + \overline{Y} + C_{IN}$	Sum PAR	L	H	H	L	L	H
$XSR \oplus Y$	XOR PAR	L	H	H	L	H	L
$XSR \oplus \overline{Y}$	XOR PAR	L	H	H	L	H	H
X • Y	AND PAR	L	X	X	H	L	X
X + Y	OR PAR	L	X	X	H	H	X
X	XP	H	L	L	X	X	X
Y	YP	H	L	H	X	X	X
Shift Left Four Bits[1]	SL4 PAR	H	H	L	X	X	X
Shift Right Four Bits[2]	SR4 PAR	H	H	H	X	X	X

1. The least significant four bits of X or Y are shifted into the most significant four bits. The four least significant bits are replaced with SL7-SL4 inputs.
2. The most significant four bits of X or Y are shifted into the least significant four bits. The four most significant bits are replaced with SR3-SR0 inputs.

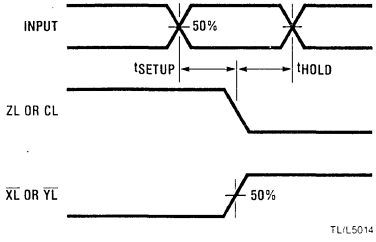
+ Logic Inclusive-OR. • Logical AND. ⊕ Logical Exclusive-OR.

Switching Waveforms

Propagation Delays



Setup and Hold



Setup and Hold

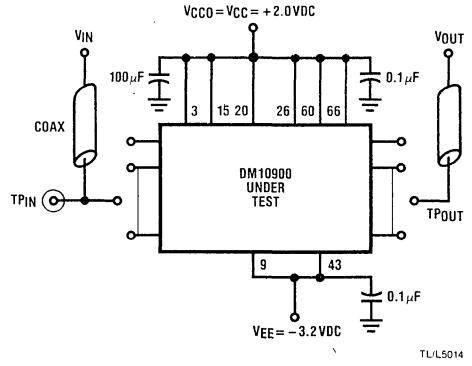
Test Procedure:

a. Establish setup time with long t_{hold}.

b. Keeping the leading edge of the input constant (t_{setup}), vary the trailing edge of the input to determine t_{hold}.

Switching Time Test Circuit

$V_{CCO} = V_{CC} = +2.0\ V_{DC}$



50Ω termination to ground location in each scope channel input.

All input and output cables to the scope are equal lengths of 50Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to output pin and TP_{OUT} to output pin.

Setup and Hold Times (Nanoseconds)
0 to +70°C T_A (T_J not to exceed +115°C)

Input	Clock (Ref. Edge)	Output	Setup (Min.)	Hold (Min.)
X Bus, XP	$\overline{XL}$ (L→H)	All	1.6	+1
Y Bus, YP	$\overline{YL}$ (L→H)	All	1.6	+1
X Bus, Y Bus, Comp.	ZL (H→L)	Z Bus	17.8	0
		ZP	19.2	0
	CL (H→L)	$\overline{CN3}$, $\overline{CN7}$	14.5	0
XP, YP	ZL (H→L)	ZP	11.7	0
$\overline{C_{IN}}$	ZL (H→L)	Z Bus	12	−1
		ZP	14.3	−1
	CL (HB→L)	$\overline{CN3}$, $\overline{CN7}$	8.6	−1
SL, SR	ZL (H→L)	Z Bus	6.1	+0.5
		ZP	12	0
X8, X_{IN}	ZL (H→L)	Z Bus	15.5	−1
		ZP	17.2	−1
	CL (H→L)	$\overline{CN3}$, $\overline{CN7}$	12.1	−1
OPA, OPB	ZL (H→L)	Z Bus, ZP	10.6	+0.5
CD60, CD61, CD62	ZL (H→L)	Z Bus	24.2	+0.5
		ZP	26.1	0
	CL (H→L)	$\overline{CN3}$, $\overline{CN7}$	21.1	−1
$\overline{XL}$, $\overline{YL}$ (H→L Edge)	ZL (H→L)	Z Bus	18.9	−0.5
		ZP	20.4	−1
	CL (H→L)	$\overline{CN3}$, $\overline{CN7}$	15.5	−1
T_{Err}	ZL (H→L)	ZP	7	0

Propagation Delay (Nanoseconds)

Input	Path		Output	0 to 70°C T_A (T_J not to exceed 115°)	
	Via	Mode		Typical	Maximum
X Bus	Adder	XOR	Z Bus	7.9	12.2
Y Bus	Adder	Arith.	Z Bus	11.6	17.8
Comp	Mux B	Logical	Z Bus	6.8	10.8
	Adder	Arith.	$\overline{ZP}$	12.5	19.2
			$\overline{C_{OUT}}$	7.5	11.5
			$\overline{CN3}$, $\overline{CN7}$	9.4	14.4
			$\overline{ZD7}$, $\overline{ZD3}$	13.9	20.7
			HSC	9.8	15.1
			Z_{Err}	16.7	25.7
			$\overline{PG}$	7.5	11.5
			$\overline{GG}$	7.4	11.3
XP			ZP	7.6	11.7
YP			HSC	6.8	10.4
			Z_{Err}	10.5	16.2
C_{IN}	Adder	Arith	Z Bus	7.8	12
			$\overline{ZP}$	9.3	14.3
			$\overline{C_{OUT}}$	2.8	4.3
			$\overline{CN3}$, $\overline{CN7}$	5.5	8.5
			$\overline{ZD7}$, $\overline{ZD3}$	10	15.3
			Z_{Err}	12.3	18.9
SL	MuxB	Shift 4 Bits	Z Bus	4	6.1
SR			$\overline{ZP}$	7.8	12
			$\overline{ZD7}$, $\overline{ZD3}$	6.3	9.7
X8	Adder	Shift 1 Bit	Z Bus	10.1	15.5
			$\overline{ZP}$	11.2	17.2
X_{IN}			$\overline{C_{OUT}}$	6	9.2
			$\overline{CN3}$, $\overline{CN7}$	7.8	12
			$\overline{ZD7}$, $\overline{ZD3}$	12.3	18.9
			$\overline{PG}$	6	9.2
			$\overline{GG}$	5.8	8.9
			HSC	8.6	13.2
			Z_{Err}	15.5	23.8
T_{Err}		Z Parity Error Check	ZP	4.5	7
			Z_{Err}	7.5	11.5
$\overline{XL}$	Latch	Latch X, Y	Z Bus	12.3	18.9
$\overline{YL}$			$\overline{ZP}$	13.3	20.4
			$\overline{C_{OUT}}$	8.3	12.7
			$\overline{CN3}$, $\overline{CN7}$	10	15.4
			$\overline{ZD7}$, $\overline{ZD3}$	14.5	22
			HSC	10.5	16.2
			Z_{Err}	17.4	26.8
			$\overline{PG}$	8.2	12.6
			$\overline{GG}$	8.1	12.4
OPA	Mux A	Select	Z Bus	6.9	10.6
OPB			ZP	5.9	9.1
			$\overline{ZD7}$, $\overline{ZD3}$	9.4	14.4
			Z_{Err}	11.4	17.5
CD60	Adder	Shift 1 Bit	Z Bus	15.7	24.2
CD61			$\overline{ZP}$	17	26.1
CD62			$\overline{C_{OUT}}$	11.6	17.9
			$\overline{CN3}$, $\overline{CN7}$	13.7	21
			$\overline{ZD7}$, $\overline{ZD3}$	18	27.7
			HSC	14.4	22.1
			Z_{Err}	21.3	32.7
			$\overline{PG}$	12	18.5
			$\overline{GG}$	11.9	18.3
ZL	Latch	Latch Z	Z Bus, ZP	3.3	5
			$\overline{ZD7}$, $\overline{ZD3}$	5.5	8.7
			Z_{Err}	7	11.6
CL	Latch	Arith	$\overline{CN3}$, $\overline{CN7}$	2.8	4.3

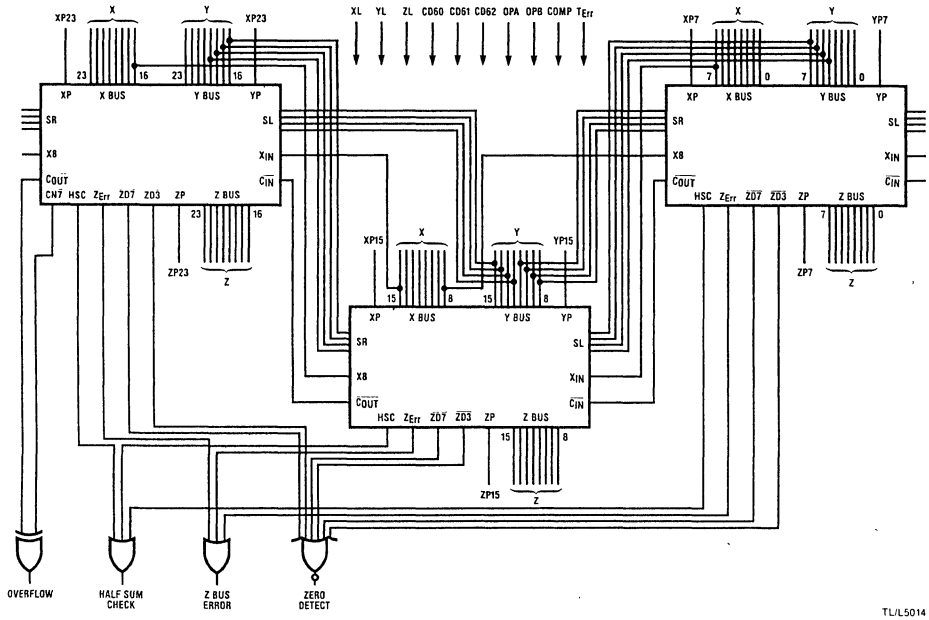


FIGURE 2. 24-Bit ALU Expansion Example

Applications

IDM2900 Family Applications Information

SYSTEM ARCHITECTURE OF THE IDM2901A

The IDM2901 is designed for use in microprogrammed systems; figure 1 illustrates a typical configuration for such a system. All devices use a common clock while two registers provide control signals and data inputs to the CPU. One of the registers serves as a direct-data input to the device, whereas the other register provides a communications link between the 2901, the microprogram sequencer, and the microprogram storage device (RAM, ROM or PROM). The "memory store" device contains microinstruction sequences, typically 28 to 60 bits wide. When selected, these microinstructions control the IDM2901 and other circuits in order to execute the chosen operation. Address lines of the "store" device are driven by the microprogram sequencer. The sequencer can store an address, increment an address, jump to any address, and link subroutines. Control bits for the "next instruction" originate in the "microprogram store." This arrangement plus the fact that the control register is between the storage device and the 2901 means that the instruction can be accessed on one cycle and executed on the next cycle. In summary, as one instruction is executed, the next instruction is being read from microprogram memory. In such a configuration, system speed is improved because "access time" and "execution time" occur in parallel; without the "pipeline instruction register," these two operations would be implemented in serial order. Other speed-enhancement techniques are detailed later under "Speed Enhancement of Bipolar Bit-Slice Microprocessor Systems."

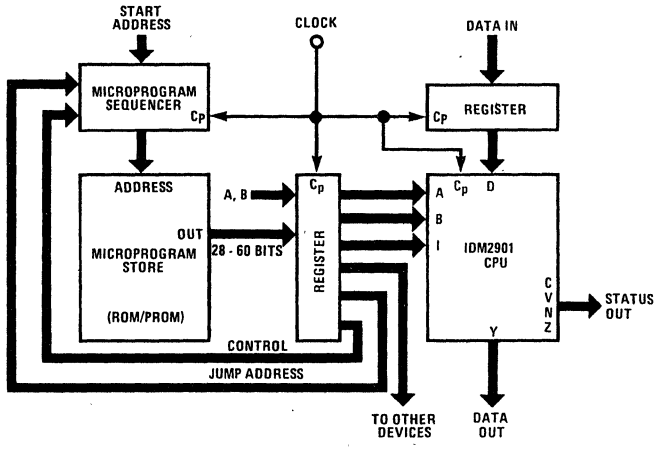


Figure 1. Microprogrammed System Using the IDM2901

EXPANDING THE IDM2901 BIT-SLICE MICROPROCESSOR

The IDM2901 is a 4-bit slice microprocessor; thus, any number of devices can be interconnected to produce, in 4-bit increments. CPUs of 8, 12, 16, 24, 36, or more bits. Figure 2 shows how three devices can be connected to form a 12-bit CPU using ripple carry; figure 3 shows a 16-bit CPU using carry look-ahead, and figure 4 shows the general carry look-ahead scheme for long words.

With exception of the carry interconnections, all expansion schemes are the same. The Q_3 and RAM_3 pins provide bidirectional left/right functions for the most significant bit. Except for the last device in the string, the Q_3 and RAM_3 lines connect, respectively, to the Q_0 and RAM_0 lines of the next device. These connections permit the "Q" register of each device to be shifted left or right as a contiguous n-bit register; also, it allows output data from the ALU to be shifted left or right as a contiguous n-bit word prior to storage in RAM. As shown in the single-slice configuration (see figure 5), the shift lines at the LSB and MSB could be connected to the TRI-STATE multiplexer; the multiplexer can then be controlled by microcode to select appropriate shift-input signals.

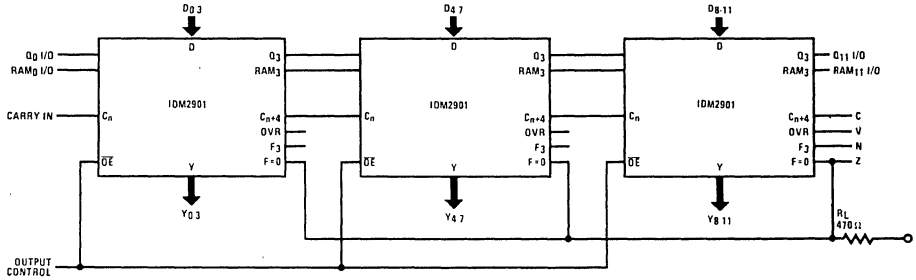


Figure 2. 12-Bit CPU with Ripple Carry

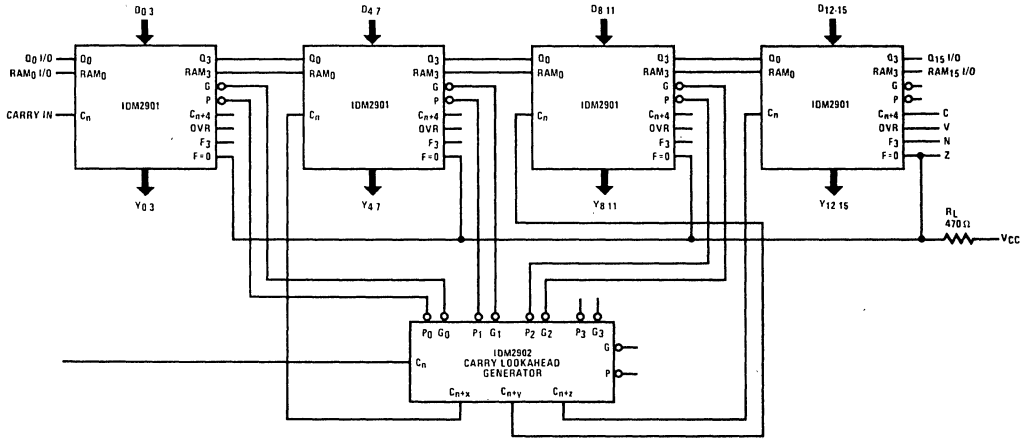


Figure 3. 16-Bit CPU Using Carry Lookahead

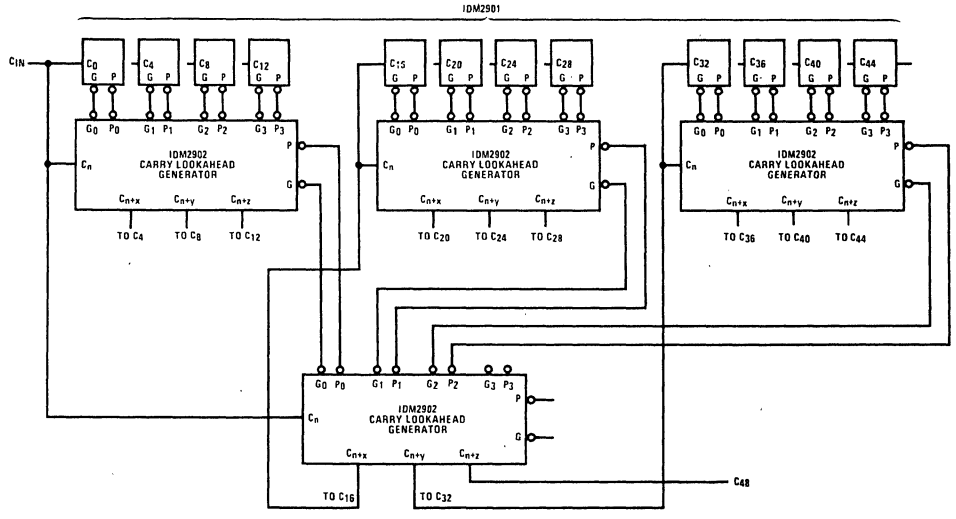


Figure 4. 48-Bit CPU Using Multiple Carry Lookahead

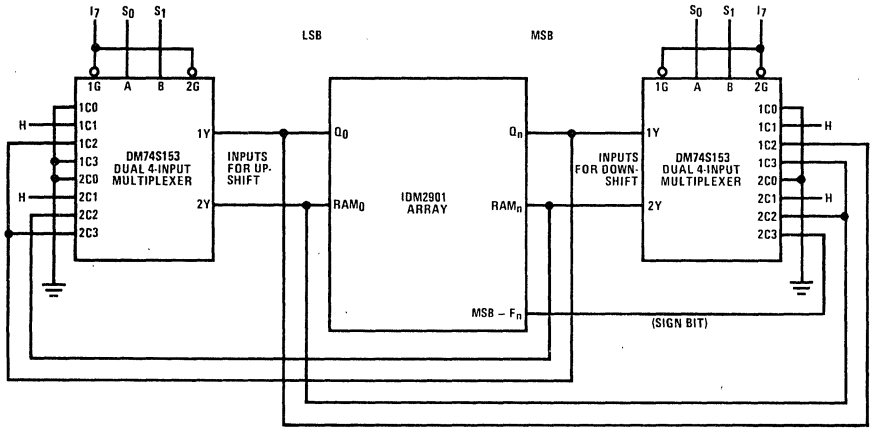


Figure 5. Typical Input/Output Shifting at End of Array

All "F=0" outputs are connected together through a pull-up resistor; this line is high only if the ALU contains all zeroes. Most systems use the "F=0" line as a "0" flag input to the processor status word. The overflow and F_3 pins are meaningful only when twos complement signed arithmetic is used. The overflow (V) output is high when the result of an arithmetic operation is a number requiring more bits than are available, causing the sign bit to be erroneous. The F_3 (MSB of ALU output) is the sign of the result in twos complement notation and indicates the negative (N) bit, of the processor status word. The carry (C) bit of the status word is taken from the most significant processor (D_{12}-D_{15}, figure 3) in the string; carry interconnections between devices can use either ripple carry or carry look-ahead. For ripple carry, the carry-out (C_{n+4}) of each device is connected to the carry-in (C_n) of the next most significant device; for example, C_{n+4} of device D_0-D_3 connects to C_n of D_4-D_7, C_{n+4} of D_4-D_7 connects to C_n of D_8-D_{11}, and so on for all interconnected devices.

As shown in figure 5, during shifting, TRI-STATE multiplexers are used to select new input information for the "Q" register and RAM; the left/right shift data is transferred between devices over bidirectional lines. Figure 5 shows how two dual 4-input multiplexers can be connected to provide four shift modes; in this case, I_7 (from the IDM2901A) is used to select the up-shift or down-shift multiplexer. In this example, the four shift modes are defined below; these are followed by a table that provides an operating summary.

Zero — On a down-shift, the MSB of RAM is set low (logic 0); if the Q register is also shifted, the MSB of this register is likewise set low. For an up-shift, the LSB of the affected register(s) is set low.

One — Same as preceding description for "zero," except the MSB or LSB is set high (logic 1) rather than low (logic 0).

Rotate — Single precision rotate — MSB of RAM shifts into LSB on a right shift; LSB shifts into MSB on a left shift. If shifted, the Q register bits are shifted in the same manner.

Arithmetic — Double-length arithmetic shift provided the Q register is also shifted. On an up-shift, a "zero" is loaded into the LSB of the Q register and the MSB of the Q register is loaded into the LSB of RAM. On a down-shift, the LSB of RAM is loaded into the MSB of the Q register and the MSB (F_n = sign bit) of the ALU output is loaded into the MSB of RAM. (The same bit will also appear in the next least significant RAM bit.)

Code			Source of New Data				Shift	Type
I_7	S_1	S_0	Q_0	Q_n	RAM_0	RAM_n		
H	L	L	0	Q_{n-1}	0	F_{n-1}	Up	Zero
H	L	H	1	Q_{n-1}	1	F_{n-1}	(Right)	One
H	H	L	Q_n	Q_{n-1}	F_n	F_{n-1}		Rotate
H	H	H	0	Q_{n-1}	Q_n	F_{n-1}		Arithmetic
L	L	L	Q_1	0	F_1	0	Down	Zero
L	L	H	Q_1	1	F_1	1	(Left)	One
L	H	L	Q_1	Q_0	F_1	F_0		Rotate
L	H	H	Q_1	F_0	F_1	$RAM_n = RAM_{n-1} = F_n$		Arithmetic

HARDWARE MULTIPLICATION

In its simplest form, interconnection for an 8-bit by 8-bit multiplication is shown in figure 6. This configuration can be easily expanded to 12 bits, 16 bits, or more by simply making the proper connections at the LSB and MSB of each device in the chain. The scheme shown in figure 6 uses the "add-and-shift" technique; thus, one clock cycle is required for each bit of the multiplier. For each clock cycle, the LSB of the multiplier is examined; if the bit is high (logical 1), the multiplicand is added to the partial product to generate a new partial product. The "new" partial product (or multiplicand) is then shifted one position towards the LSB and the multiplier is shifted in the same manner. The "old" LSB of the multiplier is discarded and the cycle is repeated until each bit of the multiplicand is used to generate a partial product. After each bit-operation is completed, the "new" LSB of the multiplier is available at Q_0.

The multiplier is retained in the Q register of the IDM2901 and the multiplicand is held in one of the file registers (R_a); the partial product is developed in yet another file register (R_b). The A-address field inputs (figure 1) are used to address the multiplicand in R_a; the B-address field is used to address the partial product, which resides in R_b. On each cycle, the contents of R_a are conditionally added to the contents of R_b and, depending on the LSB of the Q register as read from the Q_0 output, both the Q-register and the ALU result are shifted one position left. The microinstruction lines for each cycle of the operation are as indicated.

$I_8/I_7/I_6 = 4$ (left-shift register file input and Q register)

$I_5/I_4/I_3 = 0$ (add)

$I_2/I_1/I_0 = 1$ or 3 (select A/B or 0/B as ALU sources)

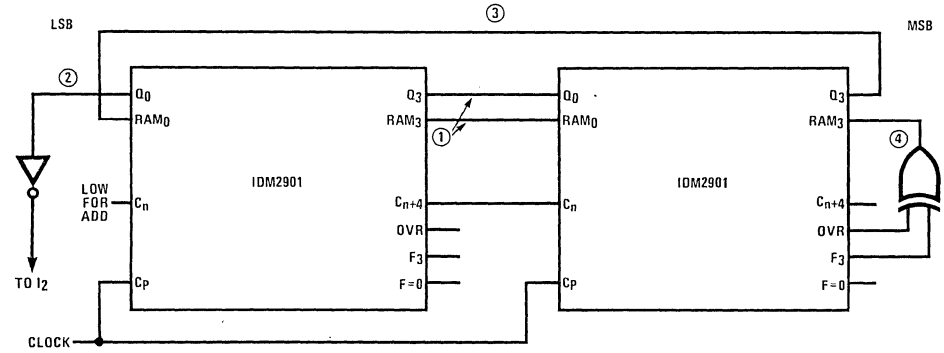


Figure 6. Using Two IDM2901s for 8-bit by 8-Bit Multiply

The circled numbers in figure 6 refer to steps in the multiplication summary that follows.

1. Input and output pins of the Q register and RAM are connected such that the Q register of each 2901 device can be left or right shifted in unison. Likewise, an 8-bit (or n-bit) ALU can be shifted as one integral unit prior to storage in the register file.

2. Source operands of the ALU are determined by the LSB output of the Q register; these operands are: A/B (add multiplicand to partial product) or 0/B (add nothing to partial product). Microinstruction bit I_1 can select between the operands (A/B or 0/B); bit I_1 can be directly driven from the LSB-complement of the multiplier.

3. When the "new" partial product appears at the input of the register file, it is shifted left by the RAM shifter. The LSB of this "new" product is complete and is not affected by future operations; accordingly, it is output at RAM_0, where it is then input to the MSB of the Q register. As each cycle is completed, the LSB of the product is input to the MSB of the Q register; thus, when the operation is completed, the Q register contains the least significant half of the resulting product.

4. As the ALU output is down-shifted for each clock cycle, the sign bit of the new partial product is input to the MSB of the RAM shifter. If overflow has not occurred, the F_3 flag will correctly designate the sign. If an overflow has occurred, the overflow (OVR) output is set high and, in this case, the correct sign is the complement of F_3, that is, $\bar{F}_3$. In summary, the correct sign bit to be shifted into the MSB of the partial product is F_3 (no overflow) or $\bar{F}_3$ (with overflow). On the last cycle, when the MSB of the multiplier is examined, a conditional subtraction is performed — this is because the sign bit of the multiplier carries negative rather than positive arithmetic weight:

$$(Y = -Y_i 2^i + Y_{i-1} 2^{i-1} + \ldots + Y_0 2^0)$$

The foregoing scheme will correctly produce a twos complement product for all multiplicands and multipliers in twos complement notation. Figure 7 shows the input states of the IDM2901s for each step of a signed, twos complement multiplication.

Initial Register States

R	
0	Multiplier
1	Multiplicand
2	X
3	X

Final Register States

R	
0	Multiplier
1	Multiplicand
2	LSH Product
3	MSH Product

S, F →	D	Description	Repeat	Pin States (Octal)										Jump	
				A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	To	If
0 V A	Q	Move Multiplier to Q	–	0	X	0	3	4	X	X	X	X	X		
0 B	B	Clear R_3	–	X	3	2	4	3	X	X	X	X	X		
(O+B)/2 (A+B)/2	B	Cond. Add & Shift	n–1	1	3	4	0	1 or 3 $I_1 = \overline{Q_0 LO}$	0	–	RAM_0	–	F_3 V OVR		
(B–O)/2 (B–A)/2	B	Cond. Subt. & Shift	–	1	3	4	1	1 or 3 $I_1 = \overline{Q_0 LO}$	1	–	RAM_0	–	F_3 V OVR		
0 V Q	B	Move LSH Prod. to R_2	–	X	2	2	3	2	X	X	X	X	X		

X = Don't Care S = Source F = Function D = Destination

Figure 7. Twos Complement Multiplication

BYTE SWAPPING

Sometimes it is expedient or necessary to swap the two halves of a 16-bit word – interchange D_{0-7} with D_{8-15} and vice versa. A fast method of implementing the swap is to rotate the word in RAM, shifting 2 bits at a time – only four shift cycles are required. The same file register is selected at both A and B ports; these two values are added together with carry-in connected to carry-out, producing a single position shift to the right. The ALU is then shifted to the right one more position prior to storage in RAM. For example, the byte swap of R_0 would be implemented by repeating the following set of conditions four times:

$A = B = 0$; $I = 701$; $RAM_0 = RAM_{15}$; $C_{IN} = C_{OUT}$

INSTRUCTION FETCH CYCLE

Generally, execution of a microinstruction begins with an instruction fetch cycle. The address of the instruction to be fetched (and executed) is held in the program counter (PC) and, as the first step, this address must be put in the memory address register. Next, the PC is incremented to point to the next instruction. The instruction obtained from memory is loaded into the program sequencer, which causes a jump to the microcode that executes that particular instruction. The PC can be read out and incremented in one cycle by using destination code "2" and addressing the PC with both the A and B fields. The current value of PC will appear on the Y outputs and (PC+1) will be returned to the register. For example, if PC is in register 15:

$A = B = 15$; $I = 203$; Carry-in = 1

The PC contents will appear at the Y outputs via the A port of RAM. On the low-to-high transition of the clock pulse, the program counter will be incremented and the Y outputs will be loaded into the memory address register. During the next clock cycle, memory is read and, on the succeeding low-to-high transition of the clock, the instruction is put into the instruction register of the program sequencer. Only two microcycles are required to complete the instruction fetch.

FILE EXPANSION

In certain applications, the sixteen registers contained within the IDM2901 are insufficient; thus, the number of registers must be expanded. The expansion is easily implemented via the IDM29903 addressable D register file. As shown in the IDM29903 data sheet, the device consists of sixteen 4-bit words; each word can be read asynchronously or written into on the next clock transition. Figure 8 shows the IDM2901 and the IDM29903 connected together to provide a file that is 32 words deep. As shown by the "file enable" logic and the "expansion interface" connections, it is easy to see how further expansion can be achieved. There are several possibilities which could be used for address decode of this 32-word file. The most versatile decoding system is simply to implement separate addresses for each file, that is, discrete A and B address fields for the IDM2901 and a separate address input for the IDM29903. As shown in the following sequence, extending the number of file registers allows round-robin shifting of information from one device to the other; thus, interfile data management is easily accomplished.

Assume the following file location:

R_0 through R_{15} are in IDM2901
R_{16} through R_{31} are in IDM29903

Then:

1. $R_{0-15} + B_{0-15} \rightarrow B_{0-15}$
2. $R_{0-15} + B_{0-15} \rightarrow B_{16-31}$
3. $R_{16-31} + B_{0-15} \rightarrow B_{0-15}$
4. $R_{16-31} + B_{0-15} \rightarrow B_{16-31}$
5. $R_{16-31} + R_{0-15} \rightarrow Q$

In the configuration shown in figure 8, single-cycle shifts do not work, except that $R_{0\text{-}15}$ can be right-shifted or left-shifted. Other shifts can be performed by making a transfer to the Q register, shifting, and then transferring back to the $R_{15\text{-}31}$ registers.

If system requirements prohibit the use of separate address decodes, common address decoding (figure 9) can be used; in this case, two 5-bit address fields are obtained via the IDM29751 and a 2-to-1 multiplexer is used to control the A/B address fields of the 2901.

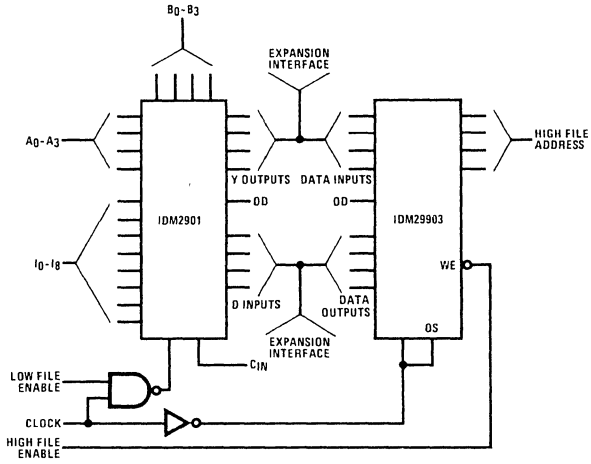


Figure 8. File Expansion Using Separate Address Fields for Each 16-Word File

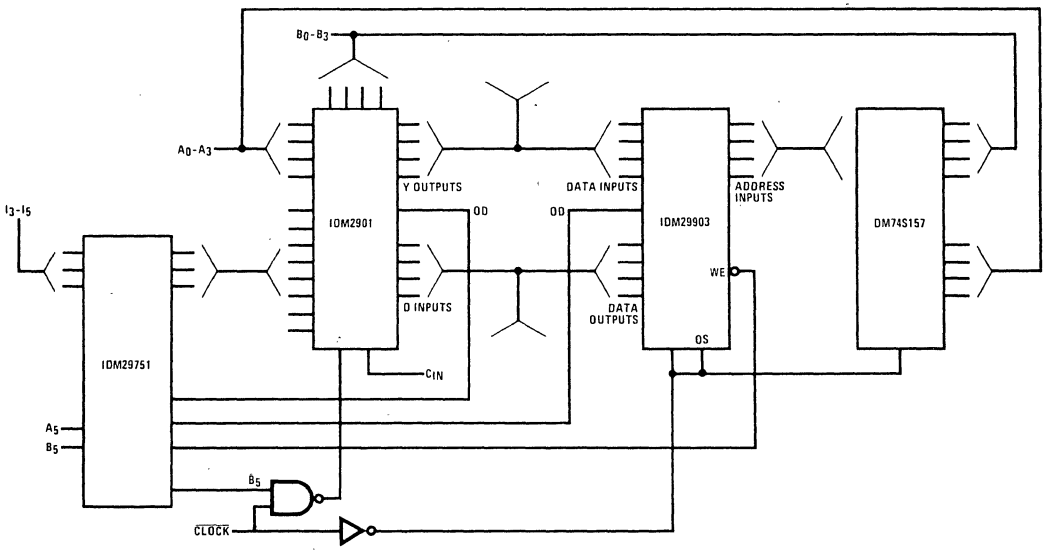


Figure 9. File Expansion Using Common Address Decoding

USING THE IDM2909A/11A IN A COMPUTER CONTROL UNIT

Introduction

In any digital computing system, the Micro Control Unit (MCU) is almost always the most complicated subsystem. The MCU controls and supervises all bus activity, synchronizes internal and external events, and grants or denies access to peripherals and other external systems. Because of these many and varied duties, the MCU is complicated in concept, design, and implementation. The IDM2909A/11A Microprogram Sequencer provides an excellent tool for overall simplification of these parameters.

Computer Architecture

Typically, the architecture of most modern-day computers is as shown in figure 10. A common data bus is used; instructions, address operands, data, and other information is sent over this bus under the direction of a microprogram. The series of instructions within each microprogram selects the source of data and also the destination. Although only one data bus is shown in figure 10, a complicated system may contain several busses – each under control of the MCU.

The address bus in figure 10 is used to select a memory word for some internal function, or to select an input/output port for an external subsystem or peripheral. Data sources for the address bus can be the program counter, the memory address register, a direct memory address controller, an interface controller, or other; these functions are also under control of a microprogram command.

The arithmetic/logic unit (ALU) is that part of the processor that does the computational work. With a complex ALU, a large number of arithmetic and logical functions can be performed. As a minimum, the ALU must perform the arithmetic functions "A+B," "A–B," and "B–A"; usually, these functions can be performed in both fixed point and twos complement binary form. The minimum logical functions performed by the ALU are: "A OR B," "A AND B," and "A EXCLUSIVE-OR B." The arithmetic and logical functions are both implemented by the same circuit configurations – the difference being in gating. Besides the arithmetic and

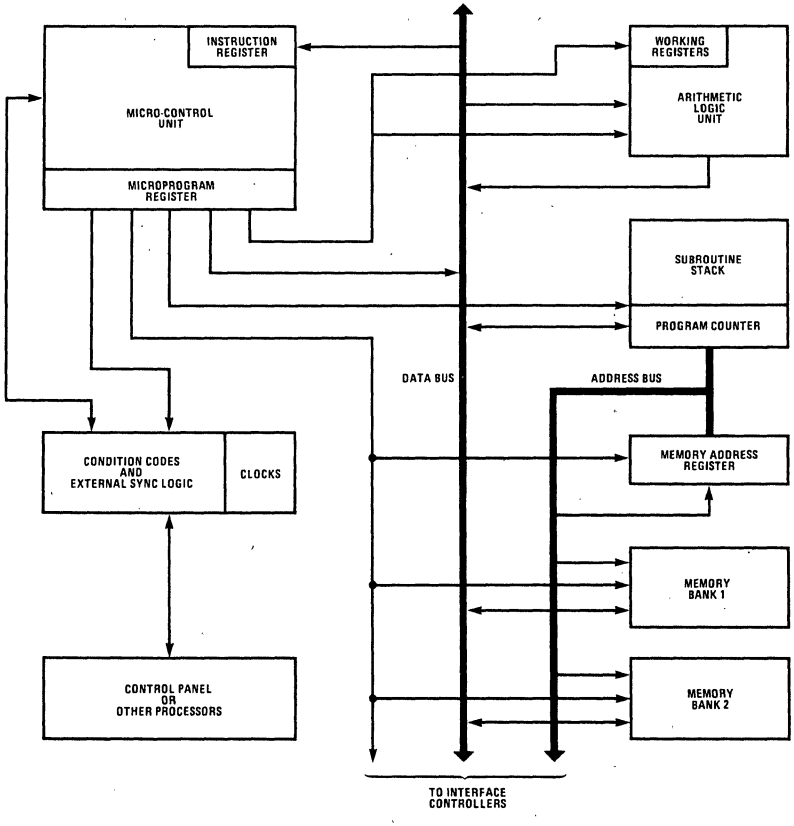


Figure 10. Generalized Computer Architecture

logic capabilities of the ALU, shift and rotate functions are also implemented as part of the basic instruction set. When an arithmetic or logical operation is performed by the ALU, a set of condition codes result. These condition codes include such variables as carry out, A = B, the sign bit, result equals zero, and so on. Along with other status information, these condition codes are stored in a register for later use by the programmer or micro control unit.

Third-generation processors also provide for a general-purpose register set that is available to the programmer to be used to hold variables that are used often — passing arguments to subroutines, referencing memory indirectly, and so on. Depending on the architecture of the machine, the general-purpose registers may be selected directly from the operands in the instruction register, from an address in the microprogram store, or one of the two sources as determined by a bit in the microprogram store.

The program counter and the memory address register are the two main sources of input to the address bus. The program counter contains the address of the next instruction or instruction operand that is to be fetched from main memory, and the memory address register contains instruction address operands that are necessary to fetch the data required for the execution of the current instruction. When exiting a subroutine, a subroutine address stack is provided to allow for easy handling of the return address linkage. The address stack is a last-in/first-out stack that is controlled by a jump-to-subroutine, PUSH, or a return-from-subroutine, POP, instruction from the MCU microprogram word.

In micro- and mini-computer systems, main memory consists of RAMs, ROMs, or more generally a combination of both. Typically, random access memories (RAMs) are slower than the micro control unit and the arithmetic logic unit. On the other hand, read only memories (ROMs) may be much faster than circuits within the MCU. Peripheral devices and multiprocessing systems present the same type of speed-interface problems; also, the MCU must contend with synchronizing events that occur asynchronously.

Control Sequence

The MCU contains an instruction register, micro-program storage, and usually a microprogram register. The initialization, fetch, and execute phases for a typical micro control unit are shown in figure 11. Regardless of system size and complexity, an initialization sequence is required to put control and storage elements in a known state such that control functions can be implemented in an orderly manner. For example, registers, condition codes, flags, and carry/link flip-flops are preset to a logic 1 or cleared to a logic 0. Likewise, it is sometimes necessary to initialize stack registers and/or main memory. The initialization process must be closely supervised to prevent alteration or damage to peripheral interfaces; furthermore, clock pulses must be withheld from the system until the initialization process is complete.

Usually, the initialization phase (1, figure 11) is started in one of three ways: (1) application of system power, (2) a "master reset" that is programmed or implemented by the operator, and (3) a detected error that cannot be corrected by the program. In a power-up generated initialization sequence, care must be given to the circuits that detect the event and generate the timed reset signal; the operating sequence should not start until the entire power system is stable. Furthermore, since some equipment and components may be damaged if they require multiple voltages that are not applied in the proper order, the MCU is often used to sequence the enabling of power supplies.

In state 2 of figure 11, an instruction is fetched from the specified memory location and loaded into the instruction register. During state 3, the program counter is incremented and the previously fetch instruction is decoded. If another operand is required for the current instruction, state 3 is repeated and the various operands are loaded into the appropriate register. This process continues until the requirements of the instruction have been met.

In state 4, the macroinstruction is executed. As in all of the other states, the instruction execution state may require one or more microinstruction cycles. After completing state 4, the MCU returns to the fetch phase and continues to fetch-and-execute the programmed microcode.

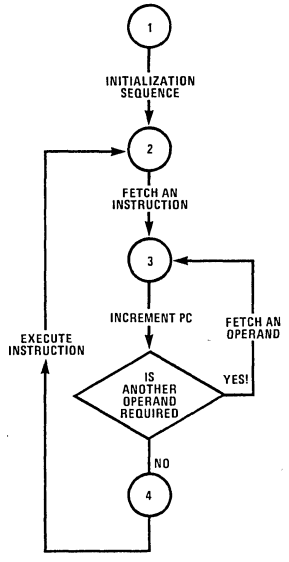


Figure 11. Initialization, Fetch, & Execute Phases for a Typical Microcomputer

Architecture of the Micro Control Unit

Basic components of the MCU are functionally shown in figure 12. The instruction register receives the instruction from main memory via the data bus; to minimize system overhead, the registers, main memory, and data bus are all of the same width. An instruction is broken down into two or more fields: the "Op Code" and one or more operands. The Op Code (Operation Code) is the instruction, whereas the operands are data used by the micro control unit in the execution of the instruction. For example, an operand might be the number of a selected register, a variable to be compared to the

accumulator, the address of an input/output port, and so on. Because the operand may be used as data, it must be presented to the data bus via an open-collector or TRI-STATE device; the Op Code and its subfields must also be distributed to the ALU and various other registers.

Usually, a macroinstruction contains more than one microinstruction; also, different classes of macroinstructions almost always require a different number of microprogram steps. In figure 12, some hardware can be eliminated by using the Op Code as the starting address of the microprogram ROM. This technique is not recommended simply because it is wasteful and inflexible; also, the entire system is affected by changes in the instruction set or the microprogram. To avoid these problems, a mapping ROM can be used.

To allow a greater range of starting addresses for the microprogram ROM, the output of the mapping ROM could be wider than the Op Code field that is used as the address input. Because ROM/PROM field widths are typically 4 bits or 8 bits wide, a reasonable choice for an 8-bit Op Code is a mapping ROM that is 12 bits wide. The starting address, as specified by the mapping ROM, is loaded into the microprogrammer counter which points to the first microinstruction in the microprogram ROM. When the output of the microprogram ROM stabilizes, it is loaded into the microprogram register.

The use of the microprogram register in this manner is called pipelining. The pipeline technique improves the overall machine speed by allowing the address of the microprogram ROM to be changed and its output to settle while the current microinstruction is being executed. The microprogram sequence controller in figure 18 performs two basic functions: (1) synchronizes external events, and (2) uses the output of the test condition multiplexer to determine whether or not microprogram branches, jumps-to-subroutine, and returns-from-subroutine are to be made.

External signals of the microprogram sequence controller can be grouped into five categories: supervisory, condition codes, initialization, synchronization, and interrupts/clocks. The supervisory signals include "Run," "Halt," and "Pause." "Run" is a latched signal that enables the clock to the entire system. "Halt" disables the system clock and is only recognized during the instruction fetch microcycle; this is a latched signal. "Pause" is a level provided to the controller from an outside processor to temporarily suspend MCU control so that the external processor has uncontested access to resources of the computer.

Condition codes are stored in the program status word register and presented to the test condition multiplexer, where any of the codes may be selected by one of the microprogram fields in the microprogram register. If the condition code is true (logical 1), the output of the test condition multiplexer will enable a branch instruction in the microprogram. The condition codes are loaded into the program status word register after every ALU operation or interrupt request.

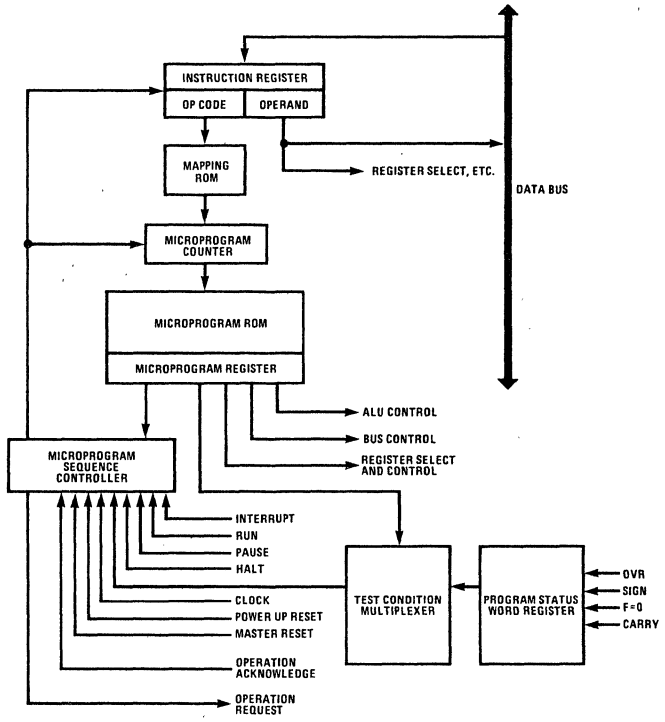


Figure 12. Basic Components of Micro Control Unit

Initialization lines include "Power-Up Reset" and "Master Reset" – these signals have been previously described. Synchronization lines include "Operation Request" and "Operation Acknowledge" – OPREQ and OPACK. These signals are used to synchronize external events whose speed is slower than that of the MCU. For example, when the MCU issues a memory reference instruction, an OPREQ signal is generated and, although the system clock continues to run, it is effectively disconnected from the micro control unit. Once the addressed memory has accessed the data and performed the read or write operation, it generates the OPACK signal; thus, the system clock is enabled to the MCU. When the memory or input/output cycle times are known and can be controlled, the MCU clock period can be adjusted to preclude the requirement for synchronizing signals.

An interrupt may occur at any time; however, it is normally recognized only during an instruction fetch. When the interrupt is recognized, the priority encoded interrupt vector is put into the program status word register and the microprogram ROM is updated with the address of the interrupt service routine. When the interrupt has been serviced, a return to the resident program is made via the previous program counter value.

MCU Instructions

There are two types of instructions recognized within the MCU – machine language or macroinstructions, and random logic replacement or microinstructions. Macroinstructions reside in main memory, are fetched and loaded into the instruction register, and then are decoded into microinstructions which directly control resources of the computer. Two different types of macroinstructions are shown in figure 13. The register-to-register instruction consists of an 8-bit Op Code and two 4-bit operand fields; the branch-on instruction also consists of an 8-bit Op Code but the eight least significant bits define an 8-bit displacement address. In the register-to-register instruction, the operand defines the source and destination registers (A and B), that is, the result of an arithmetic/logic function using registers A and B will be stored in register B. In the branch-on instruction, the condition of the branch is implicit in the Op Code; the sum of the current program counter address and the displacement address will be stored in the program counter if the selected condition is logically true.

The word format for a typical microinstruction is shown in figure 13. The four least significant bits (B_{0-3}) define the type of microinstruction (SEQUENCER FUNCTION) that is being executed. The second 4-bit field selects the "BRANCH CONDITION" (if the microinstruction is a branch instruction); two 1-bit fields may enable the interrupt and pause functions if the microinstruction is an instruction fetch command and disables the interrupts at all other times. The third microinstruction field is composed of two 3-bit subfields which are used to define the source and the destination of data (DATA BUS CONTROL). Depending upon the microinstruction function, the remaining 12-bit field is defined either as an arithmetic logic unit control field or as a microprogram branch address field (ALU & BRANCH ADDRESS BITS). There are various methods of mapping microinstruction control fields; however, for implementation of these fields in the examples that follow, the "ALU and Branch Address" is used.

Register-to-Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Op Code								Reg. B				Reg. A			

Branch On Condition

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Op Code								Displacement							

ALU & Branch Address Bits												Data Bus Control						Synchronization Logic									
Function			Source			Destination			External Gating			Source			Destination			Pause	IEN	Branch Condition				Sequencer Function			
27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Figure 13. Macro- and Micro-Instruction Fields

Implementing an MCU Using an IDM2909A

The IDM2909A address controller permits the designer to use the very latest in microprogramming techniques – microbranching, microsubroutines, and repetitive microinstruction execution. Instead of using sequential circuits which must be parallel loaded and sequentially incremented with separate clock pulses, the IDM2909A uses a combinational incrementer whose output is transferred to the microprogram counter on the rising edge of the clock pulse. As indicated in the data sheet (Part 1 of this manual), the primary function of the IDM2909A is to present an address to the microprogram ROM such that a microinstruction may be fetched and executed. The address information is available from any of four sources – an Address Register, a Microprogram Counter Register, a Direct or Branch Input, and a Subroutine Stack. The address source (figure 14) is chosen by using the one-of-four address multiplexer select lines, S_0 and S_1. The selected address can then be modified by the OR input lines or forced to zero before it is presented at the Y address output lines through a TRI-STATE buffer.

The OR input lines can be used in either of two ways. Selected OR inputs can be set to a logical 1; this will provide the logical OR of the selected address source and the OR input lines at the Y output – in this configuration the address can be "masked." If a microprogram instruction of the SKIP or BRANCH classes is being executed and the microinstruction is aligned on an even address microprogram ROM word (the least significant address bit equals 0), then the least significant OR input may be controlled by an external test condition multiplexer. If the result of the conditional test is logically false (logical 0), then the least significant bit can be modified to avoid the execution of the BRANCH or SKIP instruction. For such functions, all unused OR inputs must be tied to ground; similarly, if the 2, 3, 4, or n least significant bits of the selected address are 0, the associated OR input lines can be modified for an extended address range skip capability.

It is often desirable to get to a predefined state, or address. For instance, if the machine has just been turned on and it is necessary to perform an initialization sequence or a realtime event occurs where the processor control is required but the ongoing process information may not be destroyed, such as an interrupt, the OR inputs may be used. All of the OR inputs must be connected to the output of a positive logic gate so that when the event occurs the output of the gate goes to a logical 1, as do the Y output address lines. The ZERO input provides a similar capability, but it must normally be held at a logical 1 and only "pulled down" to 0 when the event occurs – causing all of the address output lines to go to 0.

For automatic testing of the memory and register system, the TRI-STATE output buffer that drives the Y lines can be used. That is, if the buffer output control (OE) is disabled, the Y lines are set to the high-impedance state which allows output lines of the automatic tester to be connected directly across the outputs.

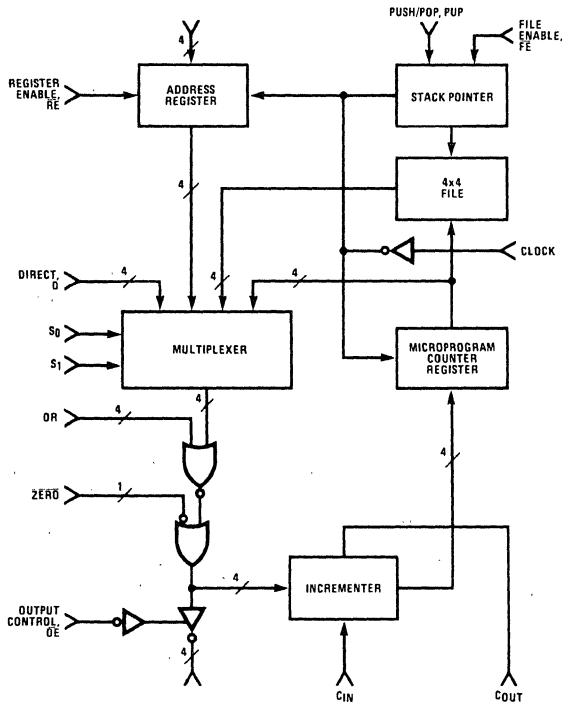


Figure 14. Functional Architecture of IDM2909A

The address register (as well as other storage devices of the IDM2909A) is parallel loaded from the R inputs when the register enable line (RE) is low on a positive-going clock transition. When entering the starting address of a microprogram, this is the ideal register to use because its contents are not only presented to the Y outputs, but also to the incrementer. The incrementer is an adder provided with an off-chip carry-in signal (C_n) and an off-chip carry-out signal (C_{OUT}); accordingly, several IDM2909A devices can be used in a cascade arrangement. The output from the incrementer is connected to a parallel load input on the microprogram counter register where it is loaded on the rising edge of the next clock pulse. If the microprogram counter is selected as the source address by subsequent microinstructions, it will be incremented by each succeeding clock pulse, thereby stepping through the microprogram.

As previously indicated, it is sometimes necessary (and often desirable) to provide a branch instruction and a branch address in a microprogram instruction. In such cases, data lines from the branch address field in the microinstruction can be feedback-connected to the data-direct (D) inputs of the IDM2909A; the source address multiplexer can then select the branch input as the next microinstruction address. On the next clock pulse, the address is incremented and stored in the microprogram counter register.

The push/pop, or last-in/first-out (LIFO) stack, provides the microprogrammer with the same flexibility in subroutine execution that machine language programmers have. A 4-by-4 file whose address is controlled by a 2-bit up/down counter allows 4-deep nesting of microsubroutines. A push/pop control signal (PUP) determines whether the function being performed is a jump-to-subroutine (PUSH) or a return-from-subroutine (POP). When the file enable control line (FE) is low, the push/pop command is executed on the rising edge of the next clock pulse. After the subroutine is completed, a return to the address immediately following the jump-to-subroutine instruction is accomplished by selecting the stack as the source address and simultaneously executing a POP command.

One method of implementing the hardware shown in figure 12 is a configuration such as that in figure 15. Two IDM29901 octal edge-triggered flip-flops with

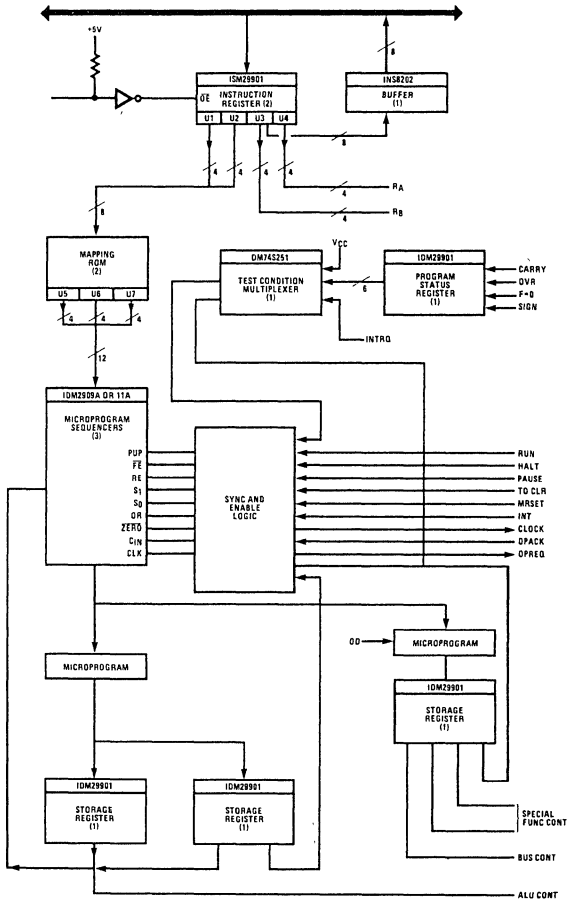


Figure 15. Using the IDM2909A to Implement a Computer Control Unit

TRI-STATE outputs (designated U_1 through U_4) make up the 16-bit instruction register. The most significant (U_1/U_2) registers contain the Op Code, whereas the least significant (U_3/U_4) registers contain the operand field. The TRI-STATE outputs from the Op Code register are connected to the address input of the mapping ROM. If, as shown, the output enable (OE) is held low by pulling up an inverter, troubleshooting and automatic testing of the system can be simplified because the tester has control of the memory system. The buffered output for the operand field is fed back to the eight least significant bits of the data bus for other register-modification purposes. In some applications, the Operand field for ALU functions will be used as two 4-bit subfields to specify a source register (R_A) and a source/destination register (R_B). In fact, this arrangement works extremely well if the IDM2901A microprocessor is used. The active TSL outputs are used for R_A and R_B data.

The two mapping ROMs are connected with common inputs but separate outputs. This memory configuration produces 256 words and a possible unique 16-bit address for each Op Code. There is considerable design flexibility and it is also easy to add additional instructions at a later time. The outputs of the mapping ROMs (or PROMs) connect to the register address inputs of the IDM2909A (or IDM2911A) microsequencers; in turn, the outputs of the sequencers specify address data for the microprogram ROMs. A recommended part type is shown for the region described as the microprogram storage. Since the 2909A or 2911A sequencer solution contains 12 addressing output bits, the size of this storage can grow to 4096 words before the microcontrol design must be modified. Almost any number of PROMs may be used for a system design since the application will dictate the number of words and the width of the word to be used in the microprogram.

As shown in figure 15, the microprogram register is split — one ROM (or PROM) providing special-function control, bus control, and ALU control, while the left side provides next state control and the possible next state jump address or ALU control. In this configuration, the starting address from the mapping ROM is loaded into the internal register of the sequencer at some time before it is needed. Alternately, the direct inputs of the sequencer can be used; this method permits a single-cycle branch to the starting address.

The control bit fields for the ALU supervise all external gating and bit manipulation, whereas the other control fields provide source/destination bus control. Whenever the processor is running, the TRI-STATE output enable lines are held low, enabling the output.

If a "Pause" is implemented (a DMA function as an example), the outputs are disabled so that an external or peripheral processor can gain access to the control line.

Depending upon the application, the sync and enable logic can be relatively simple or it can be very complex. On the one hand, these circuits must satisfy the control requirements of the IDM2909A sequencer and the IDM2901, and on the other hand, they must provide the proper interface with externally-generated control signals. For the most part, internal control (within the MCU) is handled by decoding of the functions shown in figure 16.

The ability to execute the same microinstruction a number of times was mentioned earlier; technically, the value of this capability lies outside the micro control unit. For example, consider the macroinstruction format for a register-to-register instruction as shown in figure 19. If the Op Code is a Shift or Rotate instruction, it is desirable for the programmer to move the data word over a range of 1 to 16 bit positions with a single instruction rather than multiple execution of the same instruction. If the two operand subfields (R_A and R_B) are defined as R_A equals the number of bit positions the data is to be moved and R_B as the affected register, it is easy to see how this function can be implemented. (Additional hardware requirements are shown in figure 17.)

	Microprogram Sequencer Function						Microprogram Sequencer Control							
							O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
	A_4	A_3	A_2	A_1	A_0	Function Description	TEST ENABLE	OR	ZERO	C_{IN}	RE	FE	S0, PUP	S1
Test Condition Disabled or False	0	0	0	0	0	Initialize System	L	X	L	H	H	H	X	X
	0	0	0	0	1	Branch Test	H	L	H	H	H	H	L	L
	0	0	0	1	0	Jump to Subroutine Test	H	L	H	H	H	H	L	L
	0	0	0	1	1	Return from Subroutine	H	L	H	H	H	H	L	L
	0	0	1	0	0	Execute Program	L	L	H	H	H	H	L	L
	0	0	1	0	1	External Carry Control	L	L	H	*	H	H	L	L
	0	0	1	1	0		L	L	H	H	H	H	L	L
	0	0	1	1	1		L	L	H	H	H	H	L	L
	0	1	0	0	0		L	L	H	H	H	H	L	L
	0	1	0	0	1	This Group Undefined	L	L	H	H	H	H	L	L
	0	1	0	1	0		L	L	H	H	H	H	L	L
	0	1	0	1	1		L	L	H	H	H	H	L	L
	0	1	1	0	0		L	L	H	H	H	H	L	L
	0	1	1	0	1		L	L	H	H	H	H	L	L
	0	1	1	1	0	Load Mapped (Starting) Address	L	L	H	H	L	H	H	L
	0	1	1	1	1	Fetch Instruction	H	L	H	H	H	H	L	L
Test Condition Enabled and True	1	0	0	0	0	This State Undefined	L	–	–	–	–	–	–	–
	1	0	0	0	1	Execute Branch	H	L	H	H	H	H	H	H
	1	0	0	1	0	Execute Jump	H	L	H	H	H	L	H	H
	1	0	0	1	1	Execute Return	H	L	H	H	H	L	L	H
	1	0	1	0	0		L	–	–	–	–	–	–	–
	1	0	1	0	1		L	–	–	–	–	–	–	–
	1	0	1	1	0		L	–	–	–	–	–	–	–
	1	0	1	1	1		L	–	–	–	–	–	–	–
	1	1	0	0	0		L	–	–	–	–	–	–	–
	1	1	0	0	1	This State Undefined	L	–	–	–	–	–	–	–
	1	1	0	1	0		L	–	–	–	–	–	–	–
	1	1	0	1	1		L	–	–	–	–	–	–	–
	1	1	1	0	0		L	–	–	–	–	–	–	–
	1	1	1	0	1		L	–	–	–	–	–	–	–
	1	1	1	1	0		L	–	–	–	–	–	–	–
	1	1	1	1	1	Service Interrupt or Pause	H	H	H	H	H	H	X	X

*Value of this bit depends on logic implementation.

Figure 16. Function Table for IDM2909 (or IDM2911) Microprogram Sequencer

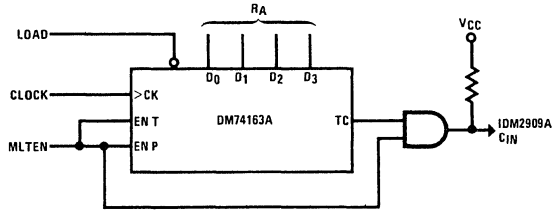


Figure 17. Example of Interactive Microinstruction Control

SPEED ENHANCEMENT OF BIPOLAR BIT-SLICE MICROPROCESSOR SYSTEMS

Review of Critical Timing Paths

In order to identify potential areas for speed improvement, it is helpful to review the critical timing paths in a typical bipolar microprocessor. First, consider the simple system organization shown in figure 18. In this system, the address register is clocked at the beginning of the microcycle. When the microinstruction is valid at the ROM output, two basic paths must be considered. One path consists of accessing data from the registers, propagation through the ALU, and storing the result in a data register and a status register. The other path involves the test condition multiplexer and sequence controller. Typical timing for such a system is shown in figure 19. After the microinstruction is valid, the two paths are indicated by arrows. In a typical system design, the minimum microcycle period is limited by the delay path through the registers and ALU – shown as "ALU Results May Be Clocked" in figure 19.

If the path delays are such that the sequencer output is valid before the path through the registers and ALU has stabilized, a modification to the system shown in figure

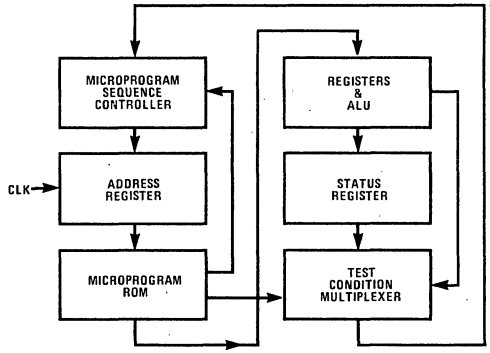


Figure 18. Simplified Block of Microprogrammed Processor

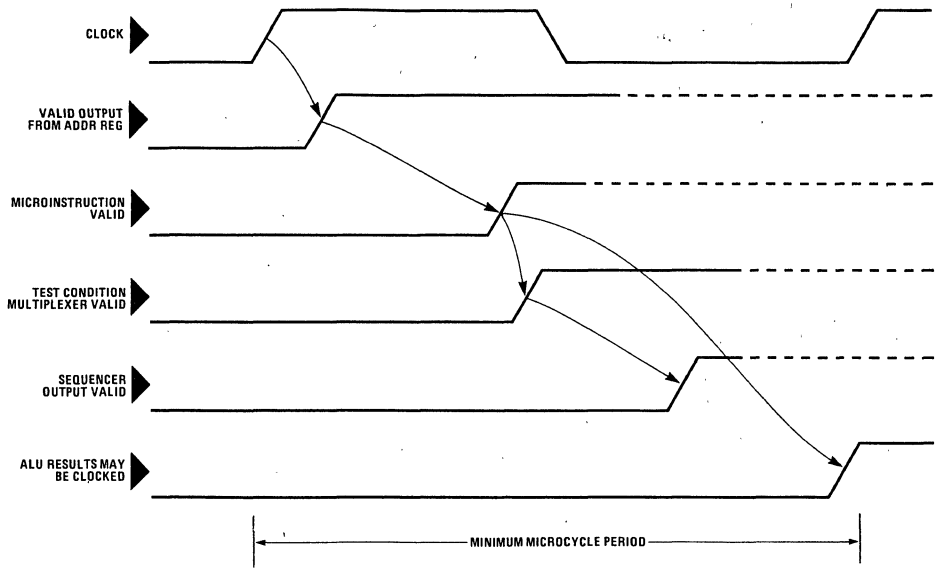


Figure 19. Typical Timing Diagram for Microprogrammed System Shown in figure 18

18 can provide improved performance. Such a modified system with typical timing is shown in figure 20 – this is frequently called a pipelined organization. The name results from the fact that while one microinstruction is being executed, another microinstruction is simultaneously being accessed. A register is added to the output of the ROM and the address register which was used to hold the output of the sequencer logic is not used. The clock causes the next microinstruction to appear at the output of the microprogram register. The sequencer output is allowed to access the microprogram ROM to fetch the next microinstruction while the data is propagating through the registers and ALU. In this way, the access time of the ROM may be overlapped with the execution of the microinstruction by the registers and ALU.

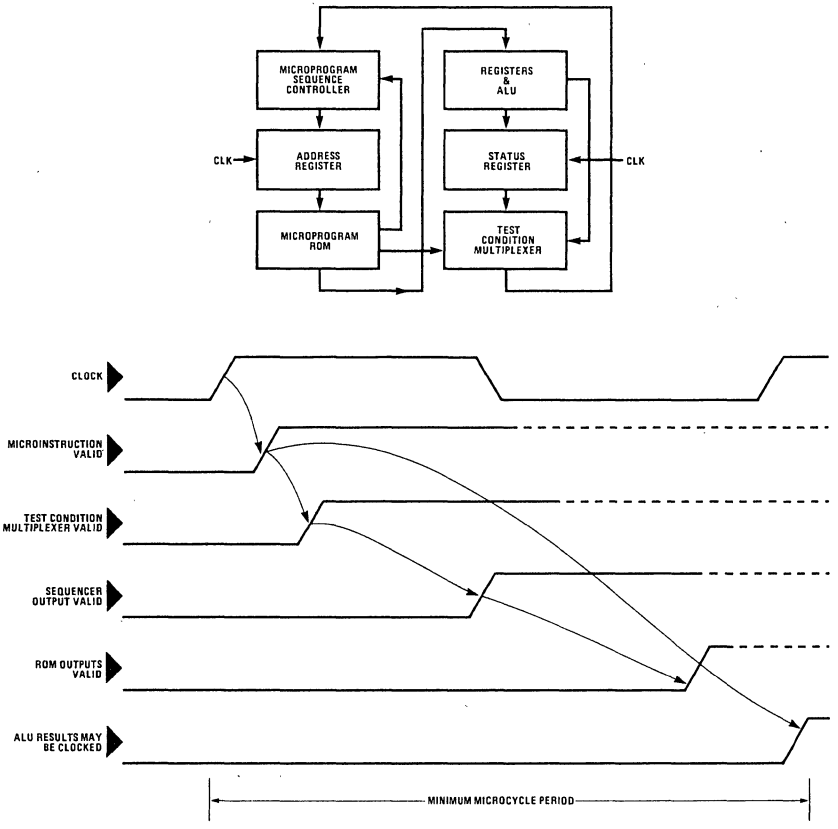


Figure 20. Pipelined Organization with Typical Timing

Predicting Test Condition Results for Higher Performance

In order for the pipelined organization of figure 20 to provide a performance advantage over the simple system shown in figure 18, the delay path through the sequencer and microprogram ROM must be faster than the path through the registers and ALU. In the timing diagram of figure 20, the sequencer output is valid early enough for the total access time of the ROM to be overlapped, that is, the ROM access time does not influence the required duration of the microcycle period. To satisfy this condition, the sequencer logic must be relatively high speed, and most importantly, the test condition multiplexer inputs must be valid at an early point in the microcycle. The latter requirement is quite unfortunate, since it implies that test conditions based upon the result of ALU operations in the current microcycle may not be used. This forces the user to either provide more status register bits (the status register outputs contain the results of operations performed on earlier microcycles) and/or execute an additional microinstruction in order to perform an operation and test the result. Thus the consequences of not permitting test conditions based upon the result of the current ALU operation cost the user both additional hardware and execution time.

An effective solution to this problem is to design the system so that the sequencer logic is conditioned on the basis of a predicted value for the test condition multiplexer output, and the ROM is accessed on this assump-

tion. After the ALU result is stable and has propagated through the test condition multiplexer, the predicted value of the multiplexer output is compared with the actual value of its output. If the predicted value was correct, the next microinstruction in sequence (i.e., the one which was being accessed) is executed. On the other hand, if the predicted value of the test condition multiplexer is different from the actual value, the conditioning of the sequencer logic is modified correspondingly, and the time duration of the microcycle is extended in order to allow time for the modification to propagate through the sequence controller logic and access the ROM. Since the microprogrammer can frequently predict the results of test conditions with a frequency of success that is much better than 50%, a relatively small fraction of the microcycles must be extended. Two examples that illustrate where the programmer can, with a high degree of success, predict results of a test condition are:

- Testing for a stack overflow condition. The stack pointer (contained in an internal register) is compared with a boundary value (contained in another register). It is of course extremely infrequent that the result of this test indicates an overflow condition in normal circumstances.
- Test of a loop counter. In a microprogrammed multiply or divide algorithm, a loop counter must be tested on each pass through the loop. For a 16-bit machine, the test would typically be performed 16 times but the result could be accurately predicted 15/16 of the time.

Variable Microcycle Period

As was discussed earlier, the delay through the registers and ALU is typically the path which limits system performance. The magnitude of this delay can vary considerably depending upon which micro-operation is being performed. Table 1 lists a variety of operations together with the microcycle period requirements for a pipelined system which was designed to use the recently announced IDM2901. Note that the longest operation requires about 75% more execution time than the shortest operation (this percentage difference is even greater for a system using the first generation version of the 2901).

Table 1. Microcycle Period Requirements for Various Operations Using a Pipelined System

Operation Performed	Microcycle Time (ns)
Logic operation; status register not modified; no test of result	98
Arithmetic operation; status register not modified; no test of result	133
Add and shift; status register not modified; no test of result	172
Multiply cycle; Q_0 used to determine I_1 of 2901	172
Arithmetic operation; status register modified; no test of result	169
Arithmetic operation; status register not modified; result used as test condition (no extend caused by incorrect prediction)	165

The most straightforward design approach is to simply calculate the worst case time period, and design the clock generator circuit to provide that time for all operations. It is evident that a speed improvement would be obtained if the clock generator could be programmed to modify the microcycle period in accordance with the requirements of the operation which is to be performed. If the operations which establish the worst case time period are performed relatively infrequently, then the system performance improvement which can be achieved by programming the microcycle period is greater than might first be imagined.

Examples of Performance with Various System Configurations

In order to illustrate the performance which results from the various system organizations described above, it is helpful to present numerical values which were obtained from a design study. Five system organizations were considered. The systems were evaluated based upon the time required to execute a variety of instructions typical of those used by a minicomputer. These results are useful for gaining an insight into the performance which may be obtained for a particular type of system organization. Obviously, the results of these studies are dependent upon component specifications — ROMs, registers, gates, and LSI devices. Thus, when choosing an organization for a new system design, the designer should perform a similar analysis using specifications of available components in order to make realistic decisions of cost versus performance.

System 1: This system was equivalent to that shown in figure 18. It was a non-pipelined organization and test conditions were based upon results of operations performed on the previous microcycle. A fixed microcycle period of 225 nanoseconds was used; this period was necessitated by the multiply instruction.

System 2: This evaluation was based on a "pipelined" system organization similar to that shown in figure 20. Test conditions were based upon results of previous microcycles and a fixed microcycle time of 172 nanoseconds was used. The pipelined organization allows the microcycle period to be reduced by 48 nanoseconds less than the cycle time for System 1.

System 3: This system was the same as System 2 except that test conditions based upon results of the current microcycle were used and the technique of predicting test condition results was utilized. The microcycle period was fixed at 172 nanoseconds. The time necessary for the result of the current operation to propagate through the test condition multiplexer and determine whether an extended cycle was needed did not require a longer period than the 172 nanoseconds established by the operation needed by the multiply instruction. An extended cycle adds 86 nanoseconds (one half microcycle) to the normal microcycle period.

System 4: This system was the same as System 2 except that a variable microcycle period was used. Test conditions were based upon the results from the current microcycle; however, no prediction of test conditions with an extended cycle for incorrect prediction was performed. Instead, those microinstructions which required more time to allow for propagation of the result through the test condition multiplexer and sequence controller were simply programmed to be of

longer duration. Microcycle periods of either 103, 137, 172, or 206 nanoseconds could be used depending upon the needs of each microinstruction. A conditional branch based upon the result of an arithmetic operation requires 235 nanoseconds with this system organization. This time exceeds the period of the longest available microcycle (206 nanoseconds). However, the conditional branch may be executed with adequate time margin by repeating the arithmetic operation on two successive microcycles: one of 130 nanoseconds followed by one of 137 nanoseconds – a total of 240 nanoseconds. Although this approach of repeating the arithmetic operation may require more microcode locations, it does offer even greater flexibility in tailoring the microcycle period to the needs of the operation being performed.

System 5: This system combines the techniques used in Systems 3 and 4. Variable length microcycles (103, 137, 172, or 206 nanoseconds) could be used. The technique of predicting test condition results was used and, when the cycle was extended due to an incorrect prediction, an additional 86 nanoseconds were added.

Table 2 shows the instructions typically used in a minicomputer that is configured in one of the foregoing system organizations. The execution times specified in table 2 for each instruction type were derived by using the execution time of System 1 as a baseline reference. The relative execution speed for each of the five systems can best be appreciated by examining the data given in table 3.

The instructions (described below) were chosen for a variety of reasons:

1. LD, JMP, and ST (Load, Jump, and Store) were chosen because they are among the most frequently used instructions, and thus are ones for which execution time optimization is quite important. Since these instructions do not involve test conditions based upon results of ALU operations, note that the technique of prediction does not improve the execution time.
2. JSR and BOC (Jump to Subroutine and Branch on Condition) are frequently used instructions. They were chosen in order to illustrate the advantages of prediction of test condition results. For JSR, it was assumed that the test condition result was always predicted correctly (i.e., no stack out of bounds occurs). For BOC, it was assumed that the test condition result was predicted correctly 50% of the time. The two values given for BOC correspond to the cases where: (a) there is no branch and (b) the branch occurs.
3. ADD and MOVE were chosen primarily because they are used by some as a figure-of-merit for machine performance. The figure shown for MOVE is the time needed for each pass through the loop which reads data from one location in memory and stores it in a second location. The advantage of the technique of prediction of current test conditions from previous microcycles does not show up in the figures shown by JSR and MOVE. This is because it was possible to

Table 2. Instruction Execution Time (ns) with Various System Organizations

System Organization	Instruction Type				
	LD, JMP, & ST	JSR	BOC	ADD	Loop for MOVE
System 1 – non-pipelined; test condition from previous μcycle	920	1610	920 or 1150	920	920N
System 2 – pipelined; no prediction; test condition from previous μcycle	688	1204	688 or 860	688	688N
System 3 – pipelined with prediction; test condition from current μcycle	688	1204	559 or 731	688	688N
System 4 – pipelined; no prediction; variable length μcycle; test condition from current μcycle	480	960	482 or 619	549	617
System 5 – pipelined with prediction and variable μcycle length	480	892	412 or 549	549	549N

Note: The reason JSR & Loop for MOVE don't improve with System 3 is that a way was found to write a code without an extra cycle.

Table 3. Relative Instruction Execution Rate with Various System Organizations (Execution speed as a speed improvement factor of System I)

System Organization	Instruction Type				
	LD, JMP, & ST	JSR	BOC	ADD	Loop for MOVE
System 1 – non-pipelined; test condition from previous μcycle	1.0	1.0	1.0 or 1.0	1.0	1.0
System 2 – pipelined; no prediction; test condition from previous μcycle	1.34	1.34	1.34 or 1.34	1.34	1.34
System 3 – pipelined with prediction; test condition from current μcycle	1.34	1.34	1.64 or 1.57	1.34	1.34
System 4 – pipelined; no prediction; variable length μcycle; test condition from current μcycle	1.91	1.67	1.91 or 1.85	1.67	1.49
System 5 – pipelined with prediction and variable μcycle length	1.91	1.80	2.23 or 2.09	1.67	1.67

write the microprogram with the same number of microinstructions for both systems. This was not the case with BOC, where an additional microinstruction was needed in order to conform to the requirement that test conditions be based upon results of the previous microcycle with System 1 and System 2.

Conclusions

Execution time calculations were made for a system where the macro-level instructions and data are stored in a (main) memory with very fast access time. Thus, it is assumed that it is not necessary to extend the clock cycle when reading from main memory. Although this is frequently not a valid assumption, it was necessary in order to simplify the presentation of results. If the memory access time is significant (say, greater than 200 nanoseconds), the relative improvement which can be obtained with the system organizations described here is somewhat less impressive. This is because the main memory access time may be overlapped to a greater extent with the system organizations having longer microcycle times. The overlapping is particularly important for those instructions which make multiple memory references, that is, LD and ST instructions require two memory reads, whereas the JMP instruction requires only one memory read. Conclusions may be drawn based upon a study of the results presented in table 3. Observe that the technique of using a variable microcycle period provides an impressive improvement in performance. Of course, this is a direct result of the fairly wide range of time intervals required for the various micro-operations presented in table 1. When the micro-operations which are performed most frequently can use the short execution cycle, the performance gained from the variable microcycle period has the most impact on overall throughput of the machine. When designing a machine with variable microcycle periods, the clever designer will concentrate his efforts toward speed optimization for the most frequently performed micro-operations. It may be possible to save hardware costs by allowing the microcycle time required for the infrequently performed operations to be longer. Thus, the variable-length microcycle approach to design offers design freedom which can possibly reduce costs as well as improve performance.

Timing Generator Design Example

A timing generator which has been designed to meet the general objectives discussed in the preceding paragraphs is shown in figure 21. This circuit generates one of two clock intervals (oscillator period x 4 or x 6) under microprogram control. A variation of this basic idea but providing a choice of four clock periods (4, 5, 6, or 7 times the basic oscillator period) is shown in figure 22. The circuit also provides for comparing the output of the test condition multiplexer with a predicted value (from the microprogram ROM). If the actual test multiplexer output does not match the predicted value, the clock period is extended (by 3 oscillator periods) and an alternate set of inputs to the sequencer logic is provided.

The key element of the circuit is a 74S195 shift register. Use of Schottky circuits allows operation at an oscillator frequency up to 33 MHz. This permits the generation of a microcycle period of 120 ns with programmable increments of 30 ns (for the clock generator which provides four programmable clock intervals, this would allow clock periods of 120, 150, 180, and 210 nanoseconds).

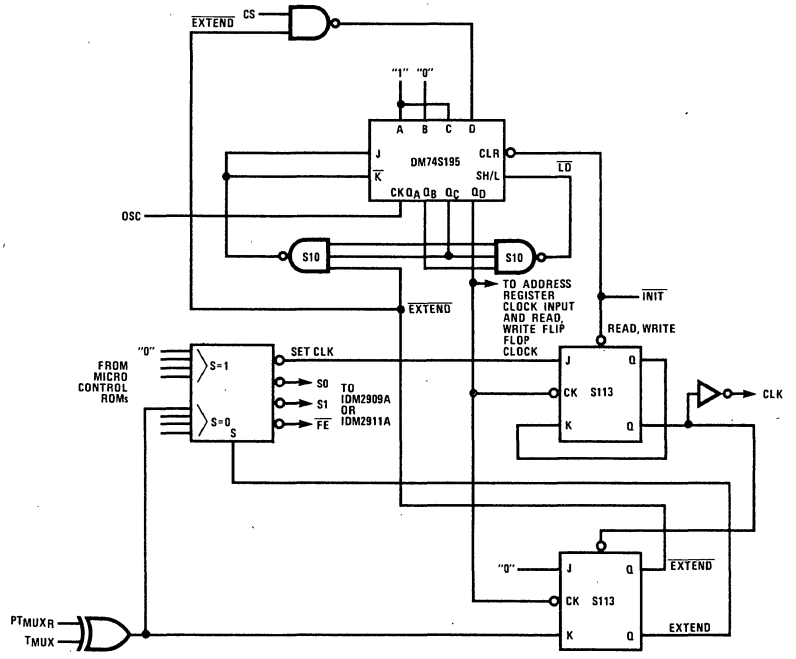


Figure 21. Two-Interval Programmable Timing Generator

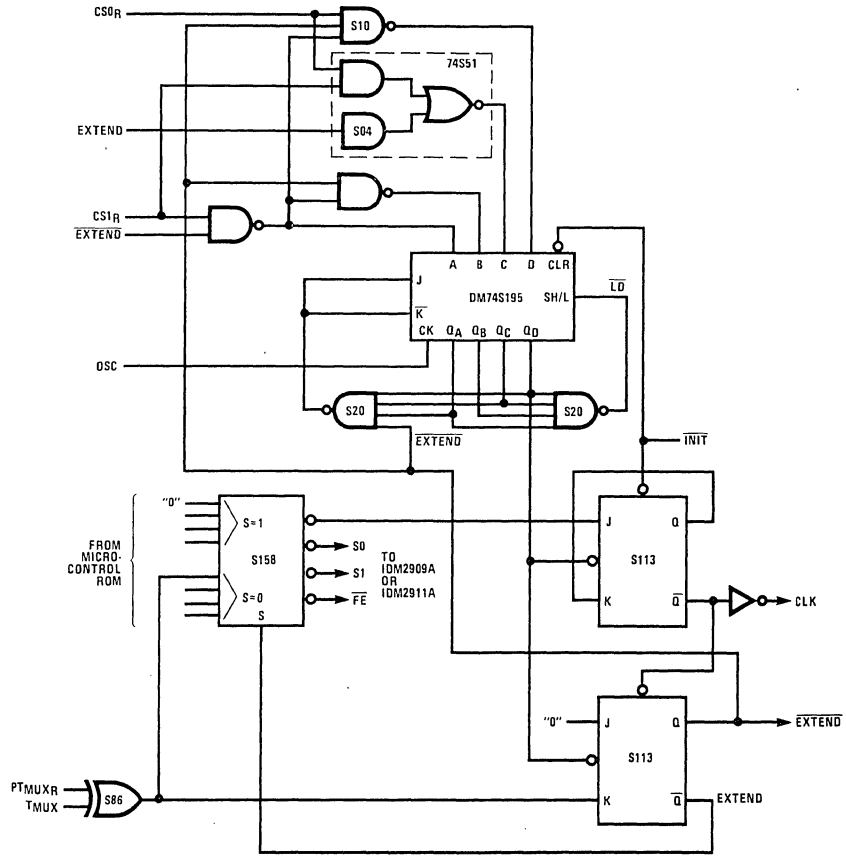


Figure 22. Four-Interval Programmable Timing Generator

The operation of the timing generator is best understood by reference to the state diagram shown in figure 23. Transitions from one state to another are made on each rising edge of OSC. The state of the shift register ($Q_A Q_B Q_C Q_D$) along with the state of CLK (the system clock) is specified in the state diagram. Assume that the clock (CLK) has just made a 0-to-1 transition indicating the start of a new microcycle (1110, CLK=1). EXTEND is a logic 0. The new outputs of the microprogram register then become valid resulting in the new values for Cycle Select (CS). (CS is a 1-bit value for the 2-interval circuit and a 2-bit value for the 4-interval circuit.) Cycle Select (CS) determines the state transition after CLK has been high for almost two OSC periods and thereby programs the duration of CLK. This is achieved by parallel loading the shift register with the desired value. State transitions then occur as determined by shifting the DM74S195. The clock input to the flip-flop which generates CLK is provided by the Q_D output of the DM74S195. CLK goes low when the DM74S195 reaches the 1010 state. On the next negative-going transition of Q_D, after CLK has been low for almost two OSC periods, the SETCLK output of the DM74S158 2:1 multiplexer determines whether CLK is set (the case when TMUX, the output of the test condition multiplexer is the same as PTMUX, the predicted value of TMUX) or CLK remains reset (corresponding to the case where TMUX is different from PTMUX). If CLK is set at this time, the sequence which was described above repeats in the same fashion. On the other hand, if TMUX was not predicted correctly, CLK will remain reset, and EXTEND will go to a logic 1. This causes the DM74S158 multiplexer to select the alternate set of inputs to the micro-sequencer logic (S_0, S_1, and FE) and causes SET CLK to go to a logic 1. After EXTEND has been active for three OSC periods (thus providing time to allow for propagation through the sequencer logic and microprogram ROM access), Q_D will make another negative-going transition, and CLK will be set, which in turn causes EXTEND to return to its logic 0 condition.

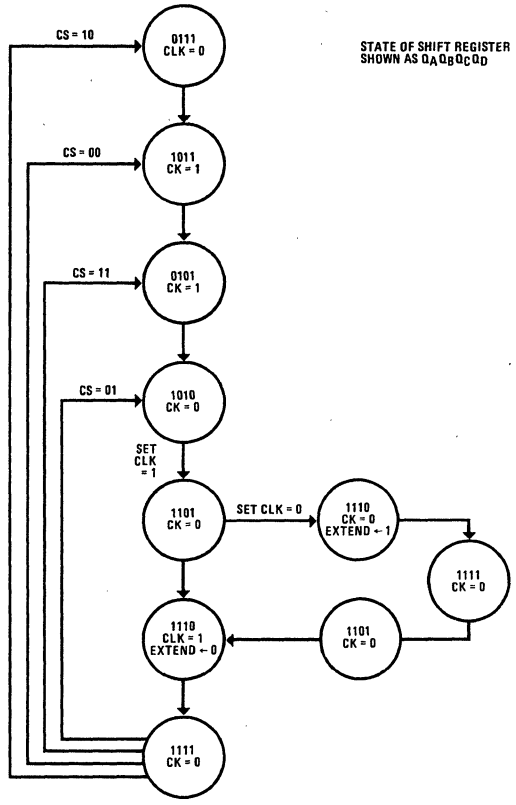


Figure 23. State Diagram for Four-Interval Programmable Timing Generator

Bit-Slice Microprocessor Design Takes a Giant Step Forward with "Schottky-Coupled-Logic" Circuits

National Semiconductor
Application Note 203
July 1978

A new four-bit slice "Schottky-coupled-logic" design combines the flexibility of the industry standard 2900 microprocessor architecture with advanced LSI processing. It implements low-power Schottky TTL circuitry on the same devices as a proprietary TRI-STATE™* emitter coupled logic design to achieve a 30 to 50 percent improvement in speed with no increase in power dissipation. It also allows the use of advanced "pipeline prediction" techniques in microprogram control design to significantly reduce microcycle times.

In most computer applications, cost, speed, power consumption and utility are the key factors. In some applications cost is the dominant consideration. In others it is speed or power consumption.

In bipolar four-bit slice microprocessor-based systems, this is particularly true. To date, however, designers have had to make a choice between the high speed of emitter coupled logic or the low power consumption and low cost of low power Schottky TTL four-bit designs such as the industry standard 2900 series.

But with current approaches it has not been very practical to have both.

If the designer chose an ECL design, he paid a price for the high speed with higher power consumption and loss of board design flexibility. If one of the LS bipolar 2900 designs currently available was chosen, low power could be achieved, but only at the price of considerably reduced system throughput.

Now, however, computer system designers can have both ECL-type speeds and LS bipolar power consumption. Using a new advanced "Schottky-coupled-logic" technique that combines low power Schottky circuitry on the same die as proprietary low power TRI-STATE ECL circuitry, the IDM2900 series of four-bit slice microprocessor components has been developed by National Semiconductor Corporation.

With this patented "SCL" technique, devices have been fabricated which are 30 to 50 percent faster than comparable 2900 designs now available. At the same time power consumption is slightly less than that for present LS bipolar designs and one third of that required for ECL-based designs.

The substantially increased system throughput made possible by this new series of SCL implemented IDM2900 parts means a number of advanced computer designs can be considered which were not possible before. For example, advanced "pipeline prediction" techniques in microprogram control design can be used to significantly reduce microcycle times.

An interesting byproduct of this approach is that this is the first ECL-based four-bit slice family to meet the military requirements over the military temperature range. Indeed, the new series shows even less performance degradation over the military temperature range than some of the standard LS bipolar parts now available.

A 60 Nanosecond Slice

The process and circuit improvement that have been achieved are the most apparent in the IDM2901 , which boasts an average microcycle time of only 60 to 70 nanoseconds, a 100% improvement over existing LS bipolar designs. Power consumption, however, is about the same, only 800 milliwatts for the entire device. Also available is an even faster version — the IDM2901A-1 — with a microcycle time of only 50 to 60 ns, and no increase in power consumption.

As with other implementations of the 2900 architecture, the IDM2901 is the key element in this high speed family of four-bit slice components. Designed as a high speed cascadable element intended for use in CPUs, peripheral controllers, programmable microprocessors and numerous other applications, the IDM2901 consists of a 16-word by 4-bit two-port random access memory, a high speed arithmetic logic unit and the associated shifting, decoding, and multiplexing circuitry. (See figure 1.)

Indeed, except for that most important parameter — speed — the IDM2901 is plug compatible with any LS bipolar implementation of the same architecture now on the market. But plug in replacement and raw speed improvements are just part of the story. As can be seen from tables 1 and 2, the IDM2901 , for example, has improved significantly almost every timing parameter possible. The read/modify/write cycle is 42 percent less, the maximum clock frequency 68 percent greater. Execution time for a typical operation, such as an add and shift (multiply) is 95ns maximum and 60ns typical, a significant gain over previous 2900 implementations. (See table 3.) Used in a typical design, system microcycle time is in the 100 to 150ns range, about one half to two thirds that of previous LS bit slice implementations.

These circuit and process improvements have been implemented in many of the standard components needed to build a system based on the 2900 bit slice architecture. In addition to the IDM2901 , nine other standard parts have already been introduced. These will allow system designers to take advantage of the increased speed.

*A trademark of National Semiconductor Corporation.

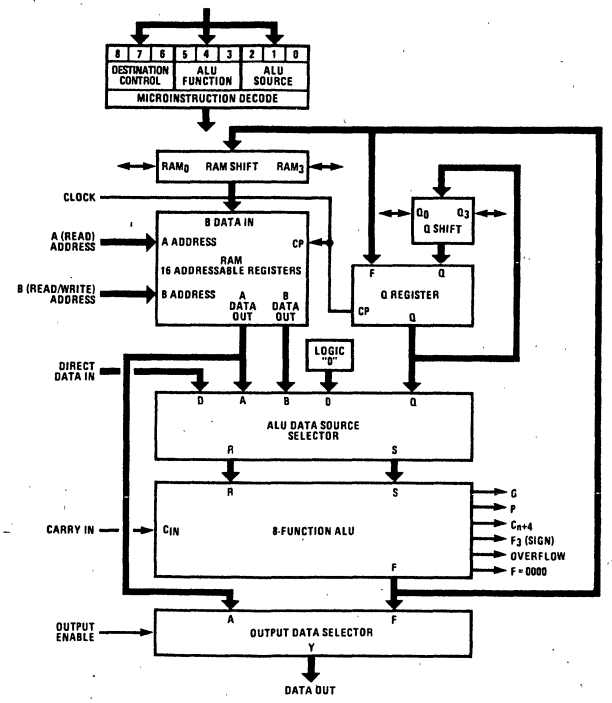


Figure 1. Block Diagram

Using some of the standard parts in the IDM2900 family, a typical 16-bit controller function can be implemented with a system microcycle time of about 140ns. This represents about a 30 percent improvement over that achieved with LS bipolar devices. Using the high speed IDM2901A-1, system throughput can be reduced to about 120ns. Using the proprietary parts added to the family, the same functions can be done in even less time, about 120 and 100ns, respectively.

Figure 2 shows a very simple, very fast state sequencing controller designed using IDM2900 family parts. It has no arithmetic capability, but 80ns clock intervals can be used. A less complex controller is shown in figure 3. It utilizes the IDM2901 for its data storage and arithmetic or logic generation. The IDM2911A is used as the state sequencer for this controller since its speed and subroutine stack can be used to advantage in the application.

LS + ECL = SCL

To achieve this combination of ECL speeds and LS bipolar power consumption, several techniques are used. One is to use low power Schottky circuitry in the periphery of the chip for input/output and interfacing to external TTL levels and the ECL internally — a technique commonly used in some bipolar memories. (See figure 4.)

Traditionally, ECL to TTL translators are slow unless considerable power is applied. In the IDM2900 family, however, the ECL speeds are retained, but at no cost in additional power, thanks to a TRI-STATE translator circuit technique that transforms the 0.7 volt ECL levels to 5 volt Schottky levels. This technique eliminates the slow and power consuming buffer transistors that usually do the job, and the translators can drop off to one third their active power with no loss in speed. Using this TRI-STATE translator technique, the extra 60 to 65 percent in power that would have been consumed is pumped instead into the portions of the device that require it; specifically, the ECL core circuitry.

Table 1. Percentage Improvement in Cycle Time and Clock Characteristics

Time	IDM2901A
Read-Modify-Write Cycle	40% less
Maximum Clock Frequency	6%
Minimum Clock Low Time	same
Minimum Clock High Time	same
Minimum Clock Period	40% less

Table 2.
Percentage Improvement
in Maximum Combinational Propagation Delays for IDM2901A and IDM2901A-1*

from Input \ to Output	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F = 0 R_L = 470	OVR	Shift Output RAM_0 RAM_3	Shift Output O_0 O_3
A, B	19 (38)	19 (38)	13 (33)	8 (31)	22 (50)	24 (30)	26 (42)	
D (arith mode)	11 (29)	11 (29)	11 (29)	0 (14)	8 (47)	18 (27)	23 (46)	
D (I = x37)	0 (20)	0 (20)			0 (42)		17 (36)	
C_n	0 (17)	0 (27)	0 (20)		20 (40)	0 (17)	30 (30)	
$I_{2,1,0}$	0 (27)	9 (55)	0 (30)	0 (33)	14 (43)	23 (62)	20 (40)	
$I_{5,4,3}$	9 (30)	9 (30)	9 (30)	10 (36)	21 (43)	23 (31)	33 (40)	
$I_{8,7,6}$	0 (17)						0 (0)	0 (0)
$\overline{OE}$ Enable/Disable	14/0 (43/20)							
A Bypassing ALU (I = 2xx)	11 (11)							
Clock ↗	0 (17)	0 (25)	0 (25)	0 (20)	20 (33)	27 (27)	25 (31)	0 (0)

*2901A-1 in parentheses.

The output translators use both linear and digital techniques. Differential ECL signals are translated using a differential current amplifier where the differential output voltage is changed to a differential current and then back to an output voltage. This drives a phase splitting transistor used to, in turn, drive the output circuitry in the periphery. Key to the operation of these translators is the use of an improved TRI-STATE logic buffer circuit characterized by a current mirror transistor having its base and emitter, respectively, connected to the base and emitter of the phase splitter transistor, and its collector connected to the voltage supply terminal. (See figure 5.) The emitter size on the current mirror transistor is about twice that of the emitter size of the phase splitter transistor.

The current mirror transistor supplements the drive current that is provided by the phase splitter transistor to the pull-down output transistor. This permits a higher resistance to be connected between the voltage supply terminal and the collector of the phase splitte transistor without diminishing the drive current to the pull-down output transistor. By connecting a higher resistance, the power for the circuit is reduced when the output is in its disabled state.

An additional advantage realized as a result of the current mirror transistor base and emitter connected, respectively, to the base and emitter of the phase splitter, and its collector to the supply voltage terminal, is a faster dynamic response in the conduction state of the pull-down output transistor to a change in the level of the digital data input signal. This occurs due to the selective use of the Miller feedback effect to cause a beneficial ratio change in the current mirror pair during a dynamic transition. Miller feedback occurs on the phase splitter transistor because its collector is coupled to the voltage supply through a resistance, and is absent on the current mirror transistor because its collector is directly connected to the voltage supply terminal. As a result, with the onset of the transition in the digital data input signal, as received from the collector of the input transistor, the current ratio between the current mirror and phase splitter transistors is even greater than the ratio of the respective emitter sizes.

Internally, the ECL logic has level translators on each input. This necessary circuitry achieves not only the level translation, but also has a very desirable input level sensitivity. As can be seen in figure 6, the translator is similar to a differential amplifier whose internal reference is stable. The result is very abrupt transfer characteristics on all input signals, and, thus, very fast switching speeds.

Improved Computer Design

The substantially increased system throughput made possible by this new series of SCL-implemented IDM2900 components means a number of improved bit slice processor designs can be considered which were not possible before.

Compared to simple control applications, there are a number of other factors to be considered when using IDM2900 series devices in more complex processor systems. The general changes which take place relate to special handling of data and address outputs and data inputs. The IDM2901 's register and ALU elements are no longer sufficient, especially when data and address word lengths grow from 8 to 16 bits or greater. Special functional elements are generally added, and include: input and output data or addressing registers, sign extend of

Table 3.
Maximum Throughput Comparisons for Add and Shift

Function	IDM 2901A-1	IDM 2901A	AMD 2901A	AMD 2901
A or B → $\overline{G}$ or $\overline{P}$	45	60	65	80
74S182 Delay	10.5	10.5	10.5	10.5
C_{IN} → RAM_0	35	35	50	55
RAM Setup Time	15	20	25	55
Total	105.5	125.5	150.5	175.5
Percent Change	40%	28%	14%	0%

data, and instruction decode, as well as shift and rotate control, and multiply functions. Also, special processor status registers are quite often added, as well as the unique controls for these elements.

Some special thought applied to these areas can reduce the parts count considerably and improve processor performance when using IDM2900 components.

The sign extend function is a good example of what can be done. Sign extension of a data word can be accomplished in a number of ways. But what the designer of the processor would prefer is to implement the function with the fewest possible parts and at the fastest data inputs. The first solution that comes to mind is the use of multiplexers, as shown in figure 7, which allows data to be fed through the multiplexer to D inputs of the IDM2901' s. The control function which steers the data to the D input representing the bit which needs to be extended normally comes from the microprogram store. The added delay using this path is 12ns or more if parts slower than the DM74S157 are used. For each 4 bits of data to be modified an additional component is required; 2 parts for 8 bits, 3 parts for 12 bits and 4 parts for 16 bits.

The IDM2900 family, however, allows consideration of a number of other ways to do sign extension that require fewer parts and are less expensive and faster.

One is to use the carry input to accomplish a sign extend. But to use this input one must subtract "1" from "0" conditionally if the sign bit is a "1" and the opposite if it is a "0." But the problem arises as to how to obtain a value "0" in a register, an impossibility.

But the same effect can be achieved if the same address location is placed upon both the A and B address inputs. The source code is then used to select A and B and the function code for subtract. Now, if a carry input is a "1" the result is a "0" and if the carry input is a "0" the result is an all "1s" sign extend result. This technique can propagate for as many packages as necessary since the carry logic is necessary for other functions and is already included.

An easy method of inserting the conditional carry with the IDM2901 is to use the IDM2902 in a manner that is different from standard LS bipolar designs. Instead of connecting the carry input of the 2902 to the microcontrol carry from ROM, it is connected to the carry out of the least significant IDM2901 package. Note that this is just as fast as the previously suggested connections since the G and P are only slightly faster than the carry out of the least significant IDM2901 . Doing this allows one free G and P input to be available at the second level, as indicated in figure 8.

It is only necessary to connect an AND gate to the input and sign extend is accomplished. The lower bits which want to be entered without modification need only be applied to the D inputs and a source code selected to perform a D minus 0 transferred to B. The most significant package group produces A minus B where A and B are as described before. An all-1s or all-0s result is obtained dependent upon the value of the data bit to be extended. The result is a sign extension with three fourths of a package for any sign extend, achieved at no loss in normal cycle time. This is because a carry input change can occur later in a cycle than a change of D.

Performing a Multiply

Most of the time the name of the game in computer processor design is speed. Nowhere is this more true than when it is necessary to perform a multiply. This is because the multiply determines the longest cycle time if performed in the normal manner. This is because more than one path through the 2901 is utilized. Passage through several external components is usually required and this must also be added to the solution time. However, with the use of high speed components in the IDM2900 family it is possible to circumvent and shorten this path, and thus shorten the multiply cycle time.

How this is done is clearly understood only by referring to a specific example. Let's assume the problem is to perform a multiply of two signed 16-bit values.

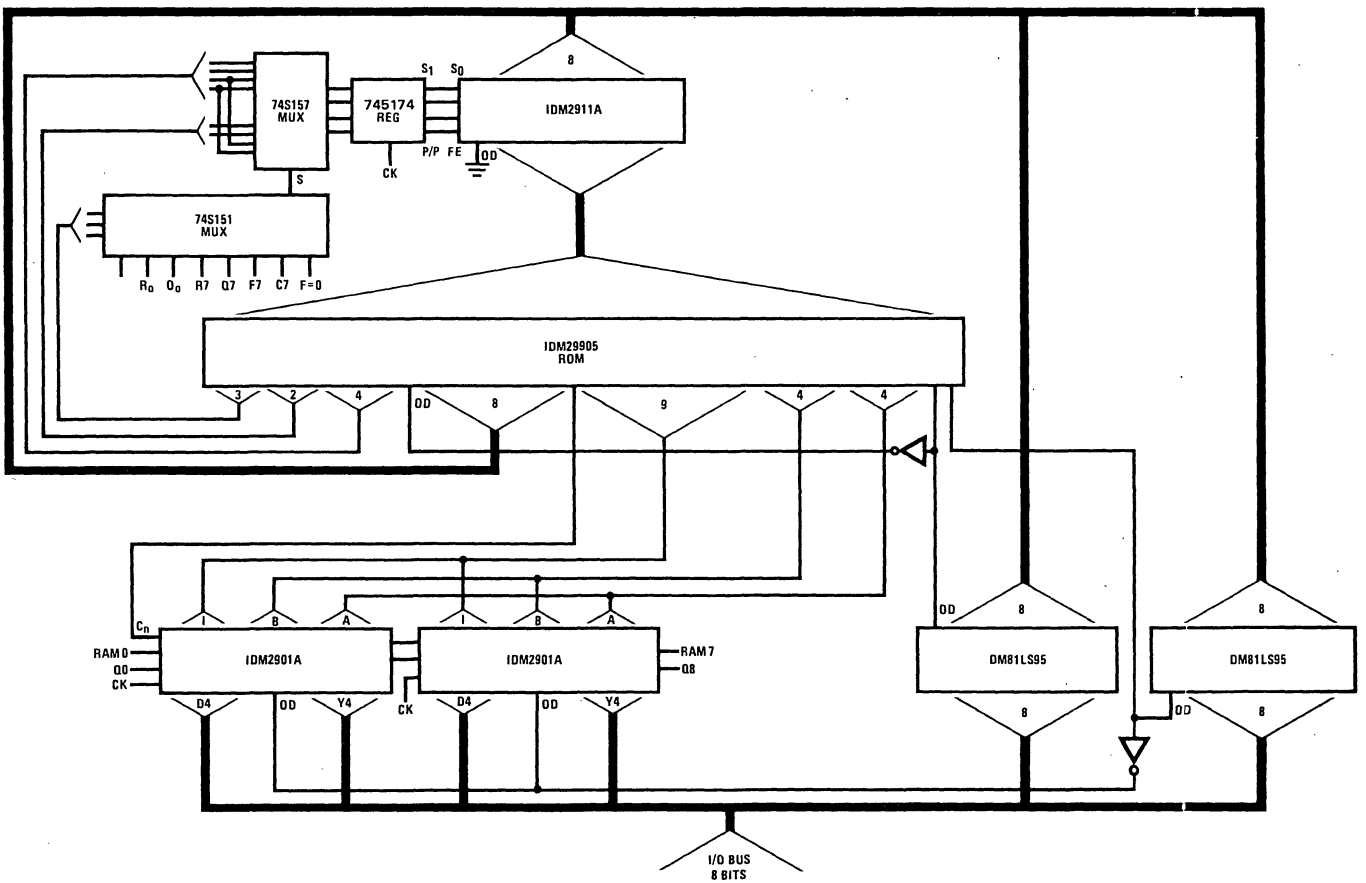


Figure 2. Very Fast State Sequencing Controller

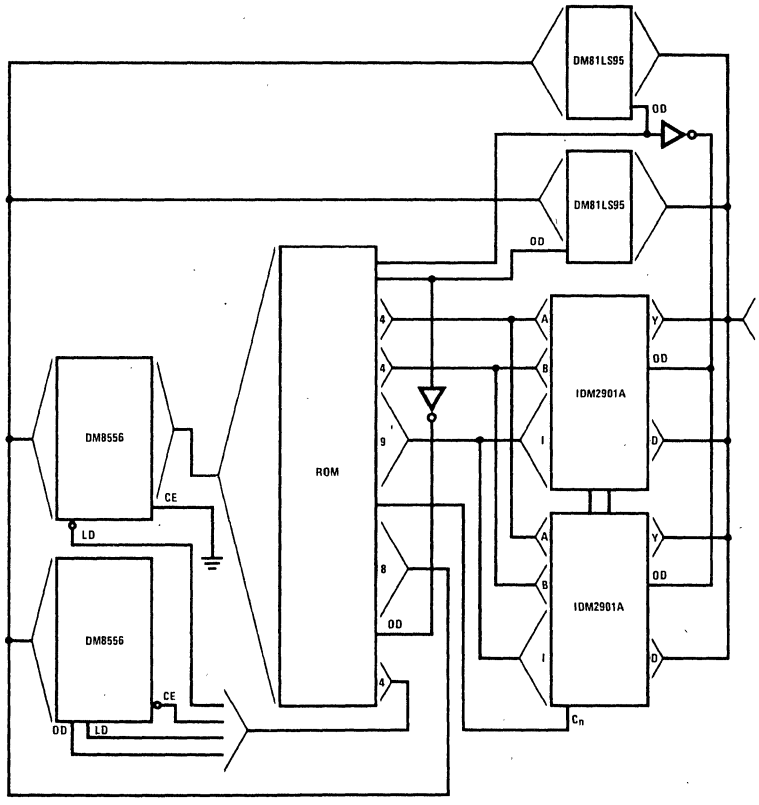


Figure 3. Small High Speed 8-Bit Controller with One Level of Subroutine Capability. This solution can run at 100ns cycles.

Figure 8 is the circuit as implemented using IDM2900 devices with the two multiplexers (74S253) and a D flip-flop (74S74). Using IDM2900 components and this technique, the multiply is performed 30 to 70 nanoseconds faster per cycle than with standard LS bipolar bit slice parts. This is a total speed improvement of 480 to 1,120ns.

An additional significance to the design is that special multiply cycle time intervals are not required. This operation, therefore, makes possible a processor or controller with a less complicated clock control circuit.

Note that in figure 8 there is an extra stage of register storage in the Q register (D type flip-flop), compared to traditional designs. It is therefore necessary to shift Q one time without shifting the file register.

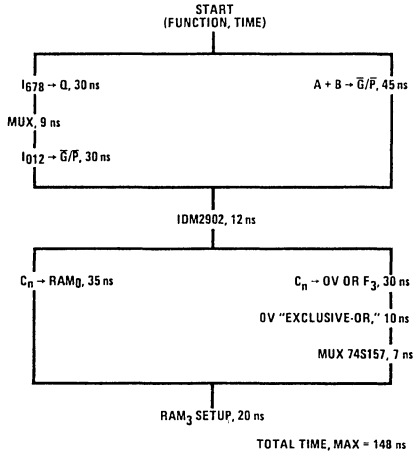
Since it is necessary to clear the partial product register, the Q register is shifted the first time so as to get the least significant bit into the extra storage location.

After this, the A and B register file addresses do not change and therefore do not enter into the timing equations. The much faster response time of an added D flip-flop saves a great deal of time in each microcycle of the multiply add and shift operation.

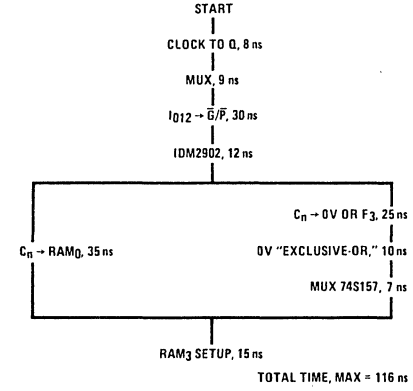
Since the A and B inputs do not change the critical path is from the D register output into the I_{012} inputs and through the IDM2901As in a normal add and shift operation. Using the Q flip-flop, 20ns is saved, and using the I_{012} input, 10ns is saved in each of the 16 cycles of the 16-by-16 multiply. This is all that is necessary for a positive signed multiplicand. But if a negative result is required, an additional path must be added.

The two possible paths in the most significant IDM2901A package are from C_n to RAM_0 output or from C_n to Overflow or F_3 and through the additional exclusive-OR gate and multiplexer input to the RAM_3 input. The maximum time delay path is 20ns from overflow and F_3 outputs back to the RAM_3 input for the most significant 2901A package.

Using standard techniques common to previous 2900 designs, only 15 conditional adds, followed by a shift and one conditional subtract and then a shift, are required to do a signed multiply in 2s complement notation. The resultant data paths required for this solution are as follows:



But if the circuit described in figure 8 is used, and the A and B address lines are set up one cycle ahead of the multiply sequence, the following timing comparison, using IDM2901A-1s instead of IDM2901As, prevails:



A net savings of 32ns per microcycle is thus achieved with this change. It can now be seen that sometimes it pays to add a flip-flop in certain locations to achieve higher performance so as to achieve a simpler solution in other areas. Here, a 20 percent reduction in cycle time was achieved.

Improving Microcycle Times with Pipeline Prediction

Perhaps the most important aspect of National's IDM2900 family of high speed, low power SCL components is the impact on how microprogram state sequencing is implemented in bit slice designs. The ultimate result will be further improvements in microcycle times beyond anything now possible with present 2900 bit slice families.

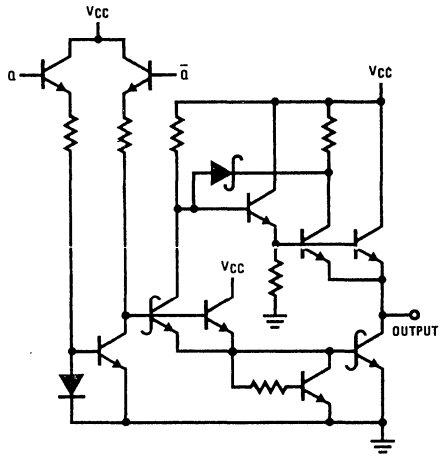


Figure 4.

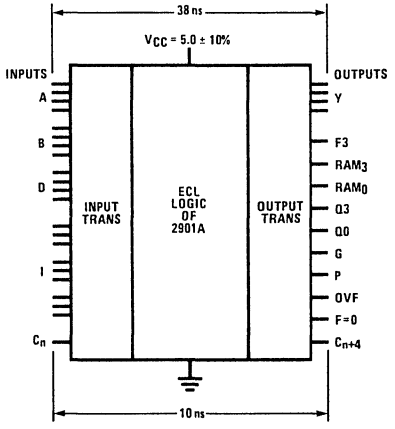


Figure 5.

In the very earliest use of state sequencing — in minicomputers and larger systems — operations were performed in series, one after the other, and the microcycle was defined as the sum of the operations. (See figure 9.) Still in use in some designs today, in this approach a state sequencer increments to the next state or branches to a next state depending on the logic level of the test input. In this solution the controller timing is from the clock edge of the controller register/counter through microcontrol storage (ROM) and the processing elements (2901s), then back through the next state decision tree to the controller-register counter.

The second approach is called "pipeline microcoding," and is an approach commonly used in bit slice systems such as the standard LS bipolar 2900 family. (See figure 10.) In this solution the microcontroller loop timing is operating in parallel with the execution of the processing component section.

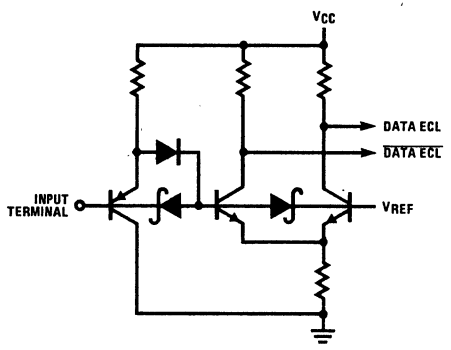


Figure 6.

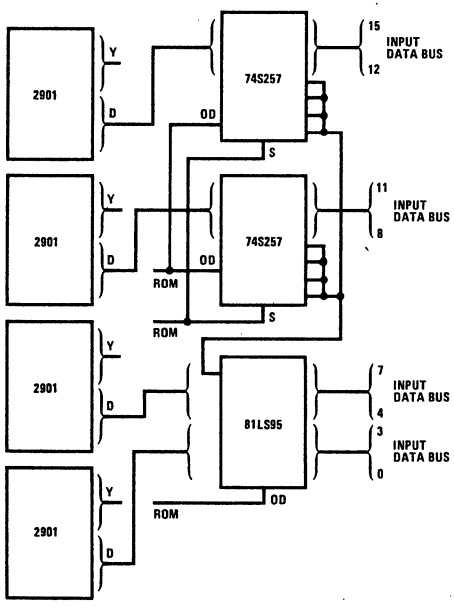


Figure 7. Sign Extend Using Multiplexers

During the time an arithmetic operation is being performed, the next microcontrol word is being set up for use by the microcode. The microcode for the present register/ALU operation occurs during the previous operation. The use of the register between the output of the microcontrol store and the 2901s allows the two sections to function with overlapped timing. The result of this type of micro-sequence control is a faster machine cycle time than used in the totally serial mode of operation.

Also required in this mode of operation is the absolute knowledge of the next state control one cycle before the execution of the 2901 cycle. It is therefore difficult to implement a number of successive conditional next state decisions. This type of microcontroller is said to be operating in a "pipeline" mode in that the next state microcontrol is being obtained during the time the previous one is being executed.

Using SCL-implemented IDM2900 components instead of LS bipolar bit slice devices in this approach results in a 65 to 75 percent reduction in the register/ALU portion of the microcycle. In spite of this, total microcycle time may be reduced only 40 to 50 percent. This is because the microcycle time is determined by the length of the longest operation, which in this case can be the delay in the microcode portion.

To get the full benefit of the high speeds inherent in National's SCL family therefore means abandoning the traditional approach to pipelining used in previous 2900 bit slice designs. What can be used instead is a different technique — pipeline prediction — which allows a reduction in the microcode portion of the microcycle so that it is equal to or less than the register/ALU setup time. The relative timing comparisons between these four approaches are shown in figures 11A through 11D.

The "pipeline prediction" controller functions in much the same way as the standard pipeline configuration except that it can also accept any number of successive conditional next state decisions in a row. This microcontroller "pipelines" microcontrol sequences in much the same manner as the previous design and for the same reasons. But shorter microcycles can be obtained due to the fact that during any microcycle the most predictable next cycle is being set up. But should the test of the next state decision be different from the one predicted, then the alternate state is conditioned and the microcontroller and the data system pass through a correction interval.

This design makes next state decisions within the same cycle as microcontrol of the IDM2901 . Figure 12 shows a "pipeline prediction" technique where the next state is a choice between two states. This means one state is predicted, and if incorrect the second choice is used. The microcycle is either delayed or an additional cycle is inserted.

There is no real reason why the design must be limited only to two next state conditons. Any number may exist. It is only necessary to predict the most probable next state and correct it if necessary. Most next state decisions are known to a high probability of occurrence. The additional cycle time added for the few times an incorrect prediction is made is extremely small compared to the total microcycle time saved. Additional speed is obtained with this technique since it minimizes the number of states through a control sequence.

Finally, pipeline prediction requires no increase in the number of components to achieve these increases.

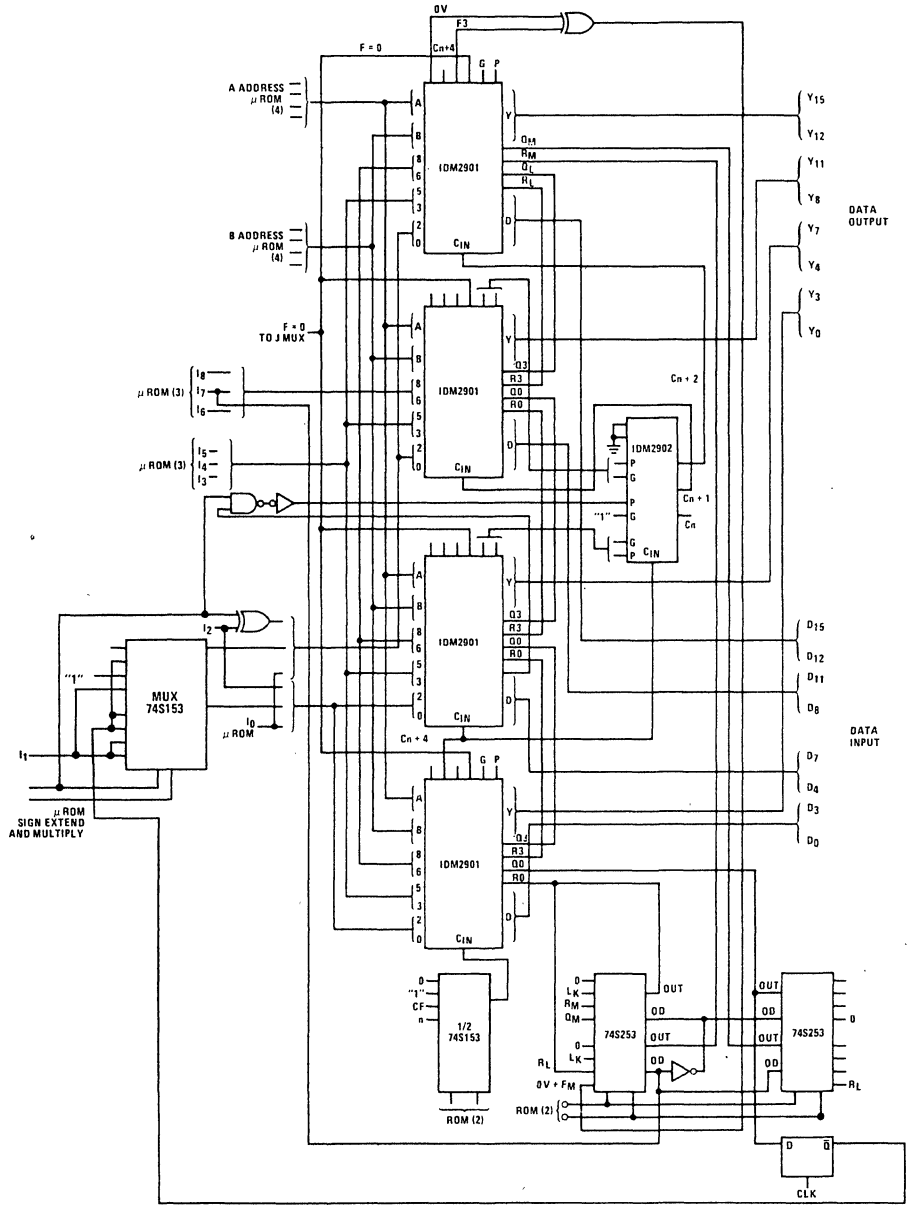


Figure 8. 16-Bit Register/ALU Design

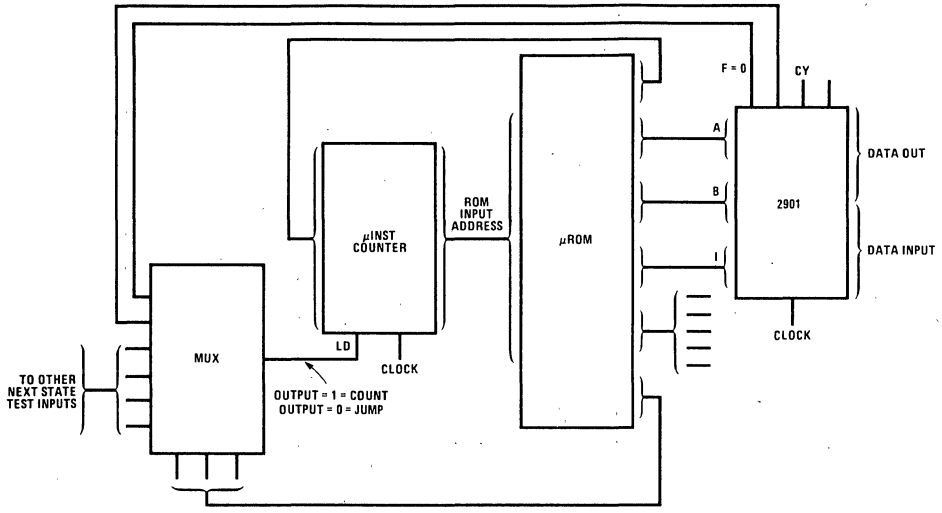


Figure 9. The Simple Microcontroller

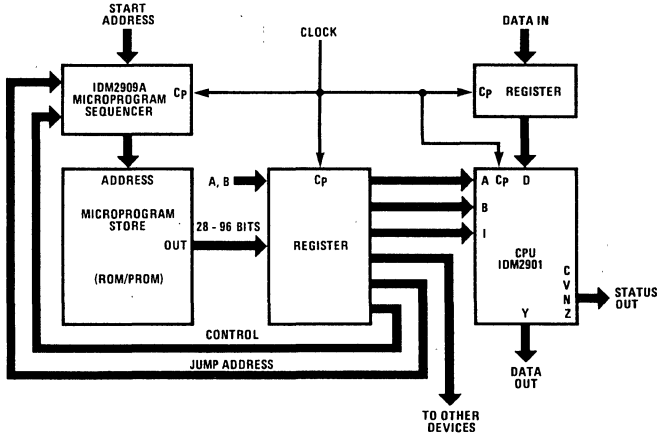


Figure 10. Microprogrammed Architecture Around IDM2901s

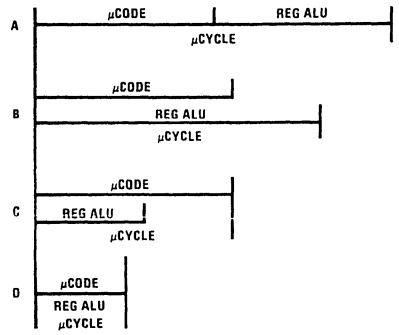


Figure 11. History of the Microcycle

Future Trends

By using higher speed parts such as the IDM2901A-1, greater improvements in throughput are possible.

And in the future there is the possibility of even further improvements, particularly on the chip processing level. The present components in National's IDM2900 SCL family have been designed with exceedingly liberal design rules. In spite of that, the chip area on the IDM2901 , for example, is equal to or less than that of some of its LS bipolar counterparts.

What this means is that there is inherent in the SCL technique the possibility of further improvements in density and integration — combining of many bit slice functions onto fewer and fewer chips — while maintaining speed.

It's not unreasonable to expect speeds on SCL-type bit slice 2901A parts to be in the 40 to 50ns range by the end of the decade and system throughput figures to be in the 80 to 90ns range. Even though SCL microcycle times at the component level may not match pure ECL-implemented parts, the system improvements allowed by the lower power may ultimately result in the design of systems with throughputs far in excess of what is possible with emitter coupled logic — at much lower power and cost.

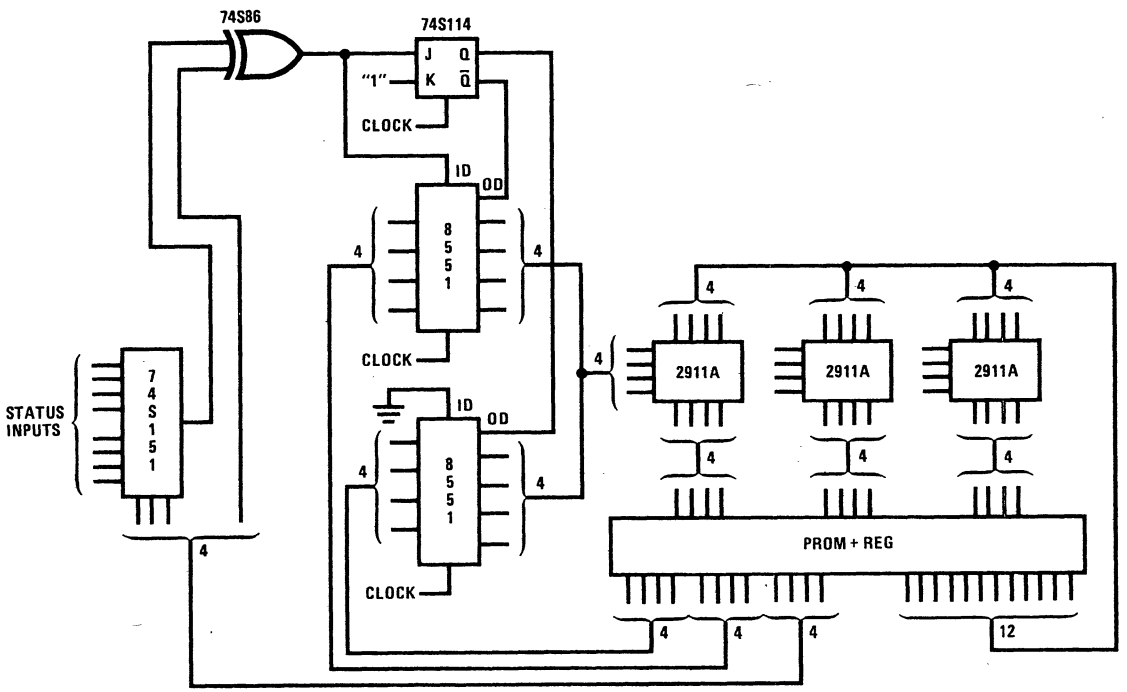


Figure 12. Microsequencer Controller for Pipeline Prediction

National Semiconductor

National Semiconductor
Application Note 217
May 1979

High-Speed Bit Slice Microsequencing Design

With the advent of higher speed versions of the industry standard 2900 bit slice microprocessor family, numerous options are now available to the system designer.

Using traditional approaches to bit slice system design, even the simple replacement of low speed, low power Schottky devices with a higher speed part, such as the IDM2901A-1, means an improvement in system throughput of 30% to 50% (Tables 1A and 1B). More importantly, these high speed parts mean a number of advanced computer designs can be considered, resulting in greater flexibility in making design tradeoffs between speed and parts count.

Table 1a. Maximum Cycle Time to STATUS Outputs*

Function	IDM2901A-1	IDM2901A
2901A A or B to $\overline{G}$ or $\overline{P}$	45ns	60ns
74S182 $\overline{G}$ or $\overline{P}$ to Carry Out	7ns	7ns
2901A C_{in} to F0, F3, C4 or OVR	30ns	40ns
Total	82ns	107ns

*Add applicable pipeline register timing.

Table 1b. Maximum Dedicated Signed Multiple Cycle (Conditional Signed Add and Shift)

Function	IDM2901A-1	IDM2901A
74S74 Clock to Out*	9ns	9ns
2901A I1 to $\overline{G}$ or $\overline{P}$	30ns	45ns
74S182 $\overline{G}$ or $\overline{P}$ to C Out	7ns	7ns
2901A C_{in} to F3 or OVR	25ns	30ns
74S86 Propagation Delay	10.5ns	10.5ns
2901A RAM Setup	15ns	20ns
Total	96.5ns	121.5ns

*Use a 74S74 as Q0 output, then connect inverted 74S74 output to I1 to realize a 19ns saving.

To take advantage of these high speed parts, an equally fast microcontrol loop is required, so that this portion of the system is a help and not a hindrance in increasing total throughput.

A number of microcontroller loop circuit configurations have been developed to take full advantage of these high speed parts. The choices are by no means exhaustive. Their purpose is to serve as an example for the designer; a starting point from which new designs can be developed.

MICROCONTROL AND THE MICROCYCLE

The object of the microcontrol portion of a processor or controller is to access the next control word to be used by the register/arithmetic-logic unit. The microcontrol portion includes a microstore of control words and a next state sequencer. Control words are fetched from microstore addresses as selected by the next state sequencer. Microstore addresses may be generated by incrementing, branching, etc., the next state sequencer being directed by a portion of the control word and by the logic level of a test input.

The microcontrol portion has to set up the next control word as quickly as possible, but otherwise stay out of the way, allowing the register/ALU portion to run at its maximum speed.

Today, this is not as easy as it was in the past. With LSI register/ALU units, such as the IDM2901A-1 or the IDM2901 , capable of speeds in the 100 to 125 nanosecond range, even the most complicated operations, such as multiply and devide, are fast enough to push most present day microcontroller designs approaches to their limits. Therefore other, higher speed approaches must be considered to take full advantage of the higher speed register/ALU's.

The first approach to microprogrammed system design — the very earliest use of state sequencing was utilized in early minicomputers and even some larger systems. Operations were performed in series, one after another (Figure 1 Phase I), with the microcycle being defined as the sum of the separate sequencer and register/ALU operations.

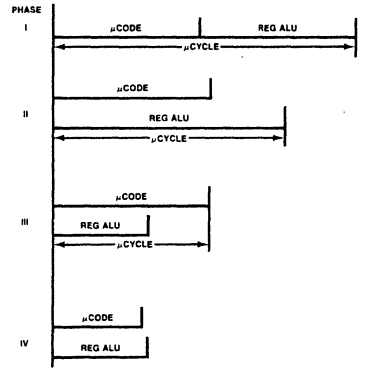


Figure 1. History of the μCycle

This solution, still in use today in some designs, routed controller timing from the clock edge of the controller register/counter through microcontrol storage, through the processing elements, then back through the next state decision tree to the controller register/counter.

The second approach, called pipeline microcoding, is an approach commonly used in bit slice systems. In this solution the microcontroller loop timing operates in parallel with the execution of the processing component section (Figure 1 Phase II). During the time an arithmetic/logic operation is performed, the next microcontrol word is being accessed. The microcontrol word for the present register/ALU operation had been selected and accessed during the previous microcycle, and is currently held in a pipeline register.

This type of microsequence control results in a faster machine cycle than is achievable in the totally serial mode employed in the first approach. It may not however, achieve machine cycle times consistent with the register/ALU cycle times available with today's higher speed register/ALU elements. For example, using highspeed components, such as the IDM2900 family, results in a 65 to 70 percent improvement in the register/ALU path. In spite of this, the resultant total microcycle time may be reduced only 30 to 50 percent because the microcycle is determined by the duration of the longest operation, which, in this case, is the delay required by the microcontrol portion (Figure 1 Phase III). Circuits optimized to approach the register/ALU cycle time (Figure 1 Phase IV) are required.

Another problem associated with pipelining is that it also requires absolute knowledge of the next state control one cycle before the execution of the current register/ALU cycle. Therefore, it is difficult to implement successive conditional next state decisions which require a test of current register/ALU results. This problem will also be considered.

As will be shown, different circuits may be configured to minimize microcontrol delay while retaining the benefits of bit slice use. While the pipelining approach will be used throughout, the circuits will differ in the manner in which conditional branch control is achieved. Speed and parts count are traded off, while retaining the same microsequencing instruction set.

Three modes of executing conditional branches are covered:

1. Overlapping the conditional branch propagation with the execution of a next unconditional microinstruction and using a NOP microcycle whenever useful work cannot be done in parallel (a NOP is a No OPeration microcycle during which the register/ALU is prevented from changing its contents). Conditional and unconditional microcycle times are equal.

2. Using the same sequences as above but employing different microcycle durations; a shorter one for unconditional microinstructions and a longer one to allow for the propagation of conditionals.

3. The pipelining prediction mode, where the conditional branch test is overlapped with the propagation of its statistically most likely outcome. Should this prediction prove to be true, the sequence continues; if false, a "pipeflushing" (NOP) one-cycle time delay is employed, during which the correct control word is allowed to propagate to the microcontrol output.

BASIC CIRCUIT ASSUMPTIONS

In all cases it is assumed that the machine has a 16-bit register/ALU and a 12-bit microaddress. Changing these parameters may increase or decrease the relative value of a given circuit.

The following constant time delays will be assumed in all circuits:

1. Microstore Time Delays

A microstore access time of 50 ns and a pipeline register setup time of 5 ns are assumed. (This is the minimum time required between microaddress validation and clocking the pipeline register).

2. Microsequencer Time Delays

The "select address" propagation time of the microsequencer is the time interval begining when the select lines become valid and ending when the desired microaddress is available at the microsequencer's outputs. Using the high speed IDM2909/11A, a select time of 30 ns is guaranteed along with a 45 ns clock to output (from file) time.

Thus, the longest total path for the microstore plus the microsequencer is:

$$50 + 5 + 45 = 100\,\text{ns}$$

This delay represents the calculated limit of the minimum time required to perform any unconditional sequence.

The setup time required by the microsequencer's internal registers is easily met in a 12-bit configuration, since it calls for a delay time of

$$(S_0S_1 \text{ to } C_{n+4}) + (C_n \text{ to } C_{n+4}) + (C_n \text{setup}) = 68\,\text{ns}$$

which is overlapped by the delay required between S_0S_1 and the next system clock.

The condition-test time delay is circuit dependent and will determine how fast, or how slow, the circuit will go.

This delay includes: 1. the time required for the pipeline register to become valid from clock; 2. the selection or propagation of the status bit under test; 3. the negation or assertion of its polarity, and; 4. the translation of the test result and conditional branch data to code compatible with driving the microsequencer.

Since the choices in selecting fast microsequencers and microstores are severely limited, the condition-test circuitry becomes the prime candidate for user optimized logic designs, because it is simple and inexpensive, etc. The following circuits attempt to minimize, in different ways, the "delay" overhead caused by the next state decision. To gain a measure of their relative speeds, the delays are compared to the calculated minimum for unconditional sequencing,

which is 100ns. A figure of merit is derived by dividing the total time delay by 100ns minimum (Table 2).

Table 2. Microcontrol Circuits Comparison

Circuit	Dynamic Performance	Figure of Merit	Parts Count	Relative Cost
I	158ns	58%	6¼	1.00
II	(Note 1)	(Note 1)	3¼	1.72
III	117/166ns	17%/66%	7¼	1.12
IV	114/135ns	14%/35%	7¼	1.10
V	133ns	33%	7⅔	0.96
VI	108ns	8%	5¾	0.90
VII	108ns	8%	6¼	0.97
VIII	108ns	8%	7	1.06

Note 1: The presently (October 1978) available 2910 has a published guarantee of 100ns from clock to Y output on instructions 8, 9 and 15.

The longest data path has not been released. It occurs where prior instructions were 4 or 12 or RLD was low.

The currently available 2910 will need a 207ns cycle when used in Circuit II in order to accommodate its longest data path (using calculated guarantees based on lab measurements performed on a number of parts). The corresponding figure of merit is 107%.

National Semiconductor's IDM2910A will need a 133ns cycle in the same circuit for its longest data path. The figure of merit will be 33%.

The IDM2910A will become available during the third quarter of 1983.

CIRCUIT I

This circuit is the traditional approach to the implementation of the microcontrol loop in a pipelined configuration. Status outputs of the last register/ALU operation determine the micro-control word to be used for the next register/ALU operation.

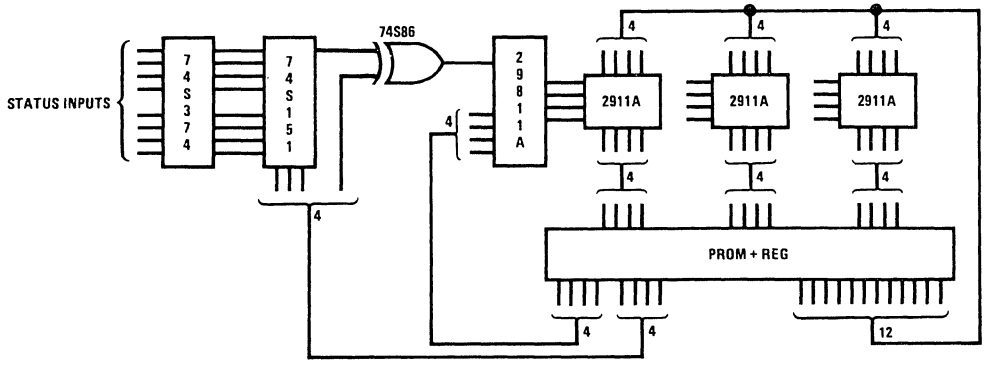
An IDM29811A next address controller is used to apply next address control to the IDM2911A four-bit microprogram sequencers. The IDM29811A is controlled by four pipeline register bits and one test input. The line to be tested is selected by a 74S151 eight-bit MUX as determined by the pipeline register. The pipeline register also determines whether negation or assertion should be performed by the 74S86 XOR gate to make it compatible with 29811 logical requirements.

The lines to be tested (inputs to the MUX) may be the results of a varity of functions internal or external to the controller. One line is generally tied to a permanent logic "1" or "0" so that by selecting it, the pipeline register may generate unconditional control of the 2911A. Some of the tested lines may carry data generated towards the end of the microcycle, such as ALU status. These data are stored in a 74S374 TRI-STATE® octal D type flip-flop since it has to be used in the next microcycle.

Conditional microcycles may be either overlapped with useful work (microprogram permitting) or may be waited out by means of a NOP. Total microcycle length required by this microsequencer is 158ns and the figure of merit is

$$\frac{158 - 100}{100} = 58\%$$

A comparison between this microcycle time (158ns) and the register/ALU loop time of 125ns or 105ns for the IDM2901 or IDM2901A-1, respectively, reveals that the machine's speed is limited by the microcontrol circuit. In short, even though the fastest microsequencer component (IDM2911A) was used, this traditional approach to microsequencer design is not compatible with higher speed, state-of-the-art ALUs.



Microcontroller, Circuit I

CIRCUIT II

One immediate "solution" to the problem outlined above, that has been suggested by some manufacturers, is going to a higher level of device integration, such as the 2910, which is a 12-bit microprogram sequencer designed to replace the 2911A and 29811A.

Conditional microprogramming is achieved here in the same way as in Circuit I and the parts count is reduced by 50%. However, the longest delay path is the one from the clock through the register/counter load to output — a guaranteed value of about 100ns. Microcycle time of this circuit is 207ns,* its figure of merit is 107% which is worse than the circuit it was designed to replace. The reduction in parts count, however, may be beneficial in those applications where operating speed is less important.

CIRCUIT III

This circuit utilizes two different clock cycle periods: a short one for unconditional sequencing and a longer one for conditional sequencing. A 74S157 quad two to one MUX and one additional pipeline register bit are used in order to provide faster, unconditional next address control for the 2911As. When conditional control is required, the path selected by the 74S157 will go through the 29811A. The four pipeline register lines will switch from carrying 2911A code (unconditional) to carrying code needed for the 29811A. Conditional microcycles need to be achieved by a clock extended microcycle which can either be overlapped with useful work or waited out with a NOP.

Total unconditional microcycle time is 117ns and the figure of merit is 17%. For the conditional microcycle mode, total time is 166ns and the figure of merit is 66%.

The overall figure of merit can be determined by weighting the calculated percentages according to the relative dynamic frequency of conditionals.

CIRCUIT IV

Similar to Circuit III, this circuit differs only in the replacement of the 29811A and the 74S157 with two 74S158 quad two line to one line multiplexers. Inverting outputs have been chosen to gain speed.

Two 4-bit pipeline register fields are supplied to the condition selected 74S158, one of which is used in unconditional microsequencing by the 74S158 that drives the 2911A.

This solution produces cycle times of 114ns and 146ns and figures of merit of 14% and 46% respectively, for the unconditional and conditional next state cycles.

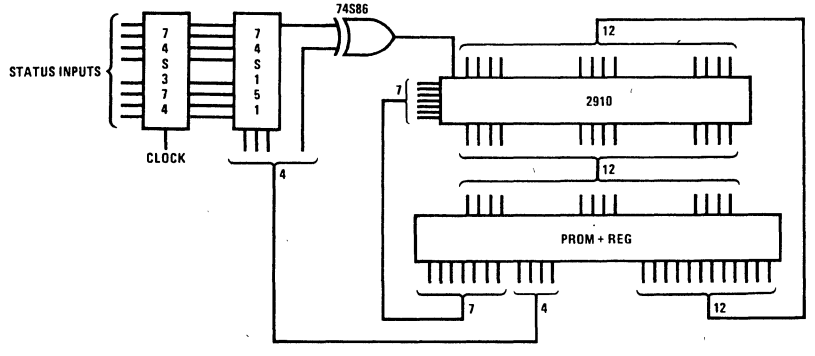
Now, by positioning the contents of the two 4-bit pipeline fields according to the logic level expected on the line under test, it is possible to remove the 74S86, eliminate one pipeline register bit to save 11ns on the conditional next state cycle. This reduces the time to 135ns and the conditional figure of merit to 35%. The unconditional figure of merit is unchanged (14%). Microprogramming is similar to that of Circuit III.

Another variation of this circuit is possible by removing the 74S158 driving the 2911A and connecting the outputs of the remaining 74S158 to the 2911A. The 74S86 may also be removed since the two, 4-bit pipeline register fields can be positioned to anticipate the desired result. Unconditional microcontrol is achieved by placing the same data on both sides of the 74S158. Total microcycle time is 129ns for both conditionals and unconditionals and the figure of merit is 29% (Compare this to the constant-microcycle time Circuit I and II). Microprogramming is the same as in Circuit I.

CIRCUIT V

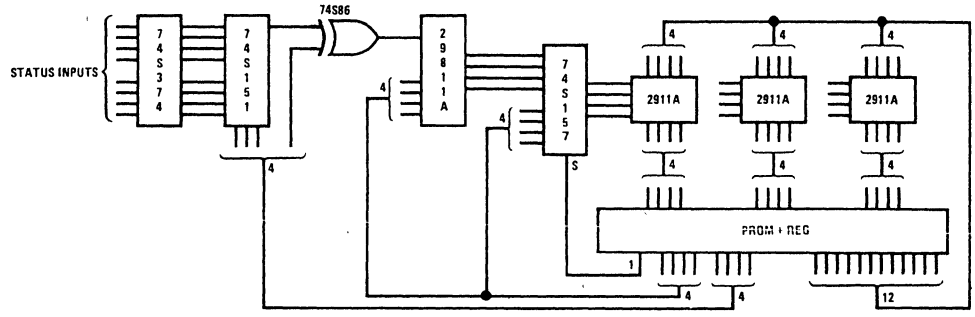
This circuit illustrates in yet another way the flexibility and advantages obtained by mixing MSI and SSI, in this case replacing the 74S158's used in previous circuits with 74S151's. Total timing needed is 133ns with a figure of merit of 33%.

This circuit is included to demonstrate a principle: sometimes a faster dynamic performance can be obtained by not using more complex circuits, in this case PROMs (29811A) and multiplexers. This occurs because less complex circuits allow greater freedom of design as well as being faster. Complex circuits may be slower and they frequently "force" design solutions to fit their own logical structure. Compare this circuit to Circuits, I, II and III.

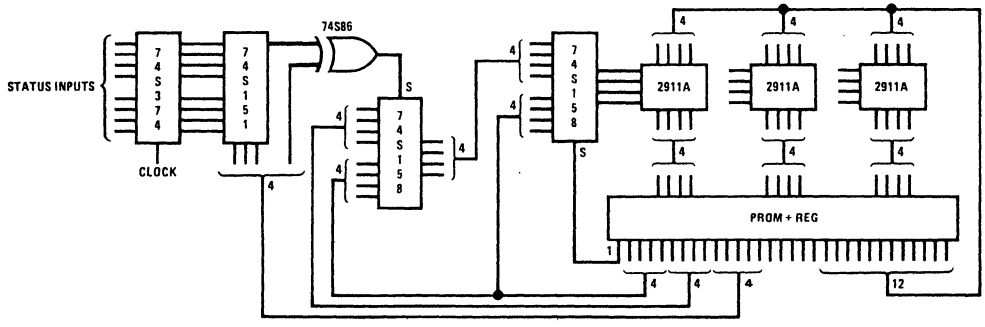


Note: Calculated guarantee based on lab measurements performed on a number of presently (October 1978) available parts. National Semiconductor's IDM2910A will show a significant speed improvement. (See Table 2.)

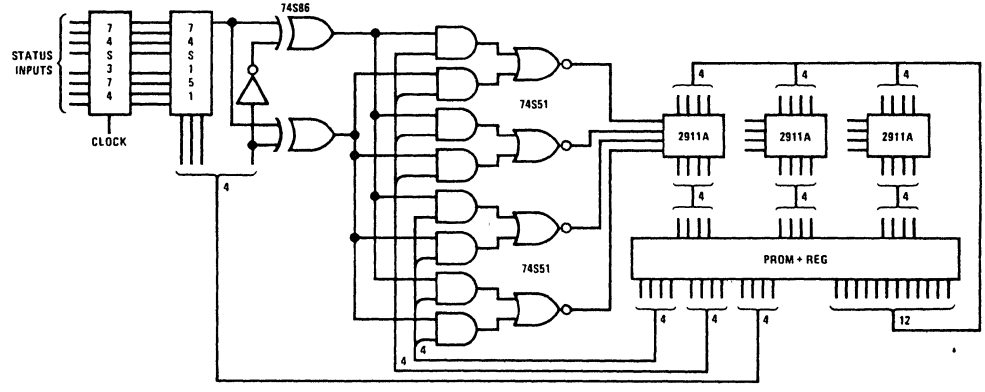
Microcontroller, Circuit II



Microcontroller, Circuit III



Microcontroller, Circuit IV



Microcontroller, Circuit V

CIRCUIT VI

This circuit represents a conceptual departure from the previous circuits. Although it functions in the same manner as the other circuits, here register/ALU performance is traded off in favor of the microcontroller loop. In other words, certain control loop time delays have been shifted over to the register/ALU loop. The status line to be tested is selected on the same microcycle that originated the status. One 74S74 edge triggered FF is used instead of the 74S374's which appear in the previous circuits.

In effect, the status register is now only one Flip-Flop of a faster varity than the 74S374's and less expensive relative to package count. If unconditionals are performed by setting the two 4-bit pipeline register fields to be identical to each other, the 74S86 may be removed as in Circuit IV.

Microcycle time is 108ns and the figure of merit is 8% for both conditional and unconditional sequences. It should be remembered, however, that 15ns has been inserted into the register/ALU loop. Using the 2901A-1, this 15ns must be added to the status valid time for a 16-bit addition of 82ns plus a 9ns clock-to-output pipeline register on the file addresses. This gives a total register/ALU microcycle time of:

$$82 + 9 + 15 = 106\,\text{ns}$$

which is compatible with the 108ns required for the microcontroller portion.

If the overall solution can be improved by moving time from one loop to another, the designer should do it.

Microprogramming this circuit is slightly different than the previous circuits since status generation and selection must be made during the same microcycle. Overlapping conditionals with useful work can be accomplished, or NOPs could be employed.

CIRCUIT VII

This circuit employs pipeline prediction to enhance speed in performing conditional microsequences.

Since in the other circuits outlined, the results of a register/ALU operation cannot be used to direct the operation immediately following it, it becomes necessary to insert fill-in words or NOPs. Pipeline prediction will minimize the number of NOPs required.

The term "prediction" refers to selecting and propagating the statistically most likely outcome. Should this prediction come true, the machine will continue at the unconditional microinstruction speed. If, however, the prediction turns out to be wrong, the predicted microcycle is converted to a NOP while waiting for propagation of the correct conditional outcome. During this waiting period the system will ignore the false microcontrol output word.

In this circuit, the prediction (and its correction, if necessary) are controlled by a 74S114 J-K edge triggered flip-flop. A logical zero result at the 74S86 output leaves the 74S114 in the "predict" position; a logical "one" causes the device to toggle and to apply to the 2911A the other choice of control code. This code is found in the 74S374, which is used as a one microcycle delay in order to preserve the initial code during NOP execution. Microcode forces a zero logic level at the output of the 74S86 whenever unconditional microinstructions are used. This logic level, in turn, causes the 74S114 to remain in its "predict" state, which is also used to generate unconditionals.

With this design, it is possible to stack any number of conditional states next to one another without confusing the controller. If all the predictions are correct, the machine operates in half the number of cycle times than with the previous technique. If all the first choices were incorrect, the design still breaks even with the previous solutions.

Generally, a net savings of cycles will result, having the same effect as an additional microcycle time speedup. This, together with the employed single length clock, makes this a very attractive circuit.

Microprogramming this circuit resembles Circuit VI, except that a jump (JMP) may not be predicted if the other choice is a continue (CONT). Such a prediction would cause an irreversible change in the microprogram counter/register. Other changes that may occur in the 2911A stack or address register can be inhibited by using the "one" logic level at the 74S86 output as a means to inhibit the RE and FE lines.

Total microcontroller cycle time is 108ns and the figure of merit is 8%.

CIRCUIT VIII

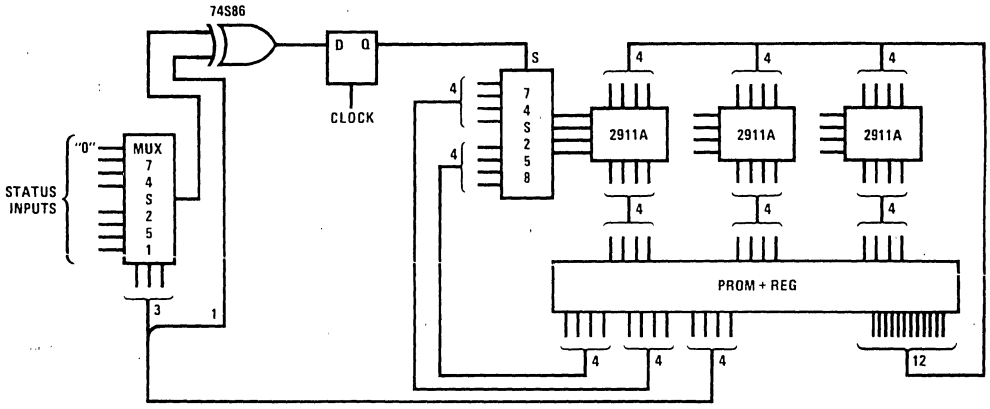
This circuit is essentially the equivalent of Circuit VII. Two 74S251 TRI-STATE® multiplexers have been used to decrease the propagation delay on the register/ALU side by eliminating the 74S86. Total time and overhead are unchanged (108ns and 8%).

CONCLUSION

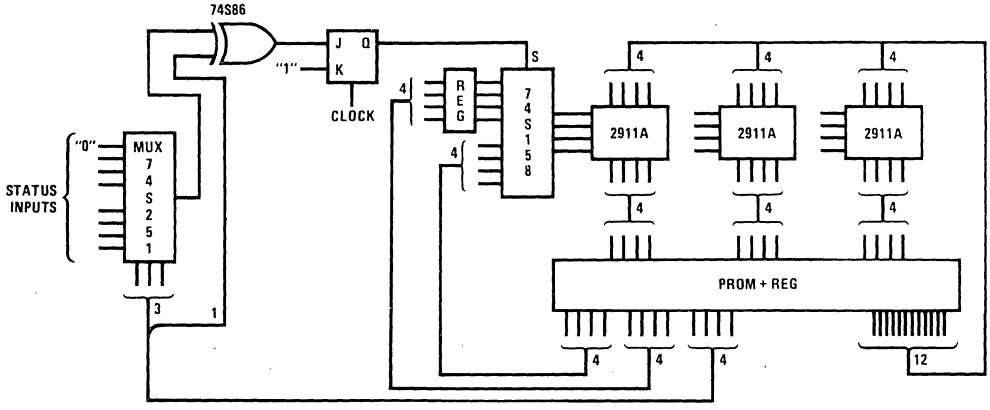
In less than two years, the 2900 bit-slice family has improved microcomputer speeds by 50% to 70%. The IDM2901A-1, the fastest part available, allows controlling and number-crunching CPU designs demanding less than 100ns per microcycle.

Faster microcontrol loops are required in order to take full advantage of ALU bit-slices like the IDM2901A and the IDM2901A-1.

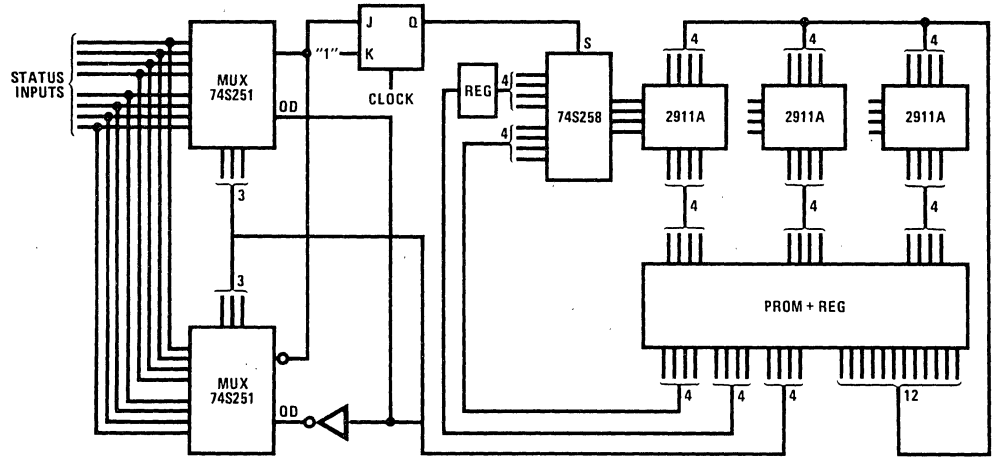
A few fast microcontrol loop designs have been explored, using the versatile IDM2909A/2911A microsequencer. These circuits are offered as basic suggestions, and as starting points for specific designs. Since, among other things, the data word width, the instruction repertoire and microstore size of a CPU will strongly influence the choice of which microcontrol loop design is best suited to yield the desired speed, price, microprogramming features, etc., the final choice must be made by the designer of a specific system.



Microcontroller, Circuit VI



Microcontroller, Circuit VII



Microcontroller, Circuit VIII

Fine Tuning the ALU Carry Path

National Semiconductor
Application Note 230
Harry Holt
May 1979

Most applications information for the IDM2902 Look-Ahead Carry Generator Family show three standard connections for 16-, 32-, and 64-bit Arithmetic Logic Units (ALUs). The three methods are shown in Figure 1.

With ALU cycle times in the 200 ns area, the standard connections shown in Figure 1 were quite adequate. A 5 to 10 ns overall savings did not warrant the time spent to examine alternative look-ahead carry methods. However, with the introduction in 1978 of the IDM2901A-1, cycle times began to approach 100 ns. This was further reduced to less than 80 ns (for a 16-bit ALU) with the introduction of the IDM2901A-2 in 1979. Now, obviously, a 5 to 10 ns savings is significant and well worth a new look at look-ahead carry techniques. The purpose of this application note is to do just that and, as will be shown, some of the results do not favor the standard approaches.

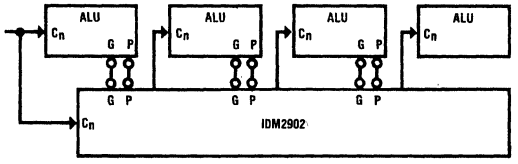


Figure 1(a). Conventional 16-Bit

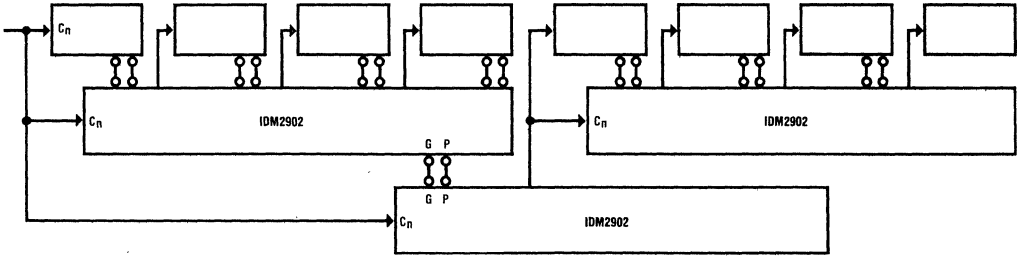


Figure 1(b). Conventional 32-Bit

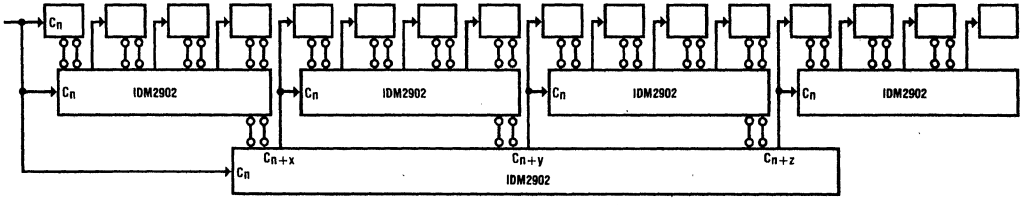


Figure 1(c). Conventional 64-Bit

BASIC METHODS

The basic methods examined in this application note can be divided into four categories:

1. Ripple Carry
2. Conventional Single Level
3. Multi-Level
4. Shifted

Ripple carry is generally considered to be slow, but at 8 bits it turns out to be the fastest method. Also, it will be shown that ripple carry can be used in combination with other methods to eliminate parts while adding very little to system cycle time. In most cases, the various methods will result in tradeoffs between parts count and system speed. It will be shown that some solutions, however, generate the highest performance with the *fewest* parts!

Single-level will be used to describe a system with a single layer of look-ahead carry even though technically this is a multi-level solution since the ALU itself looks across four bits. An example of a single-level approach is the 16-bit solution of Figure 1(a).

The conventional 32-bit connection [Figure 1(b)] is an example of multi-level look-ahead. In this approach, the carry-in is connected to two IDM2902s.

The least well known of the four methods is the shifted approach shown in Figure 2. Although this results in a slightly slower method in the 16-bit solution shown, there are word sizes where it can be the fastest method. Furthermore, freeing a set of G, P pins on the IDM2902 can have advantages in certain applications where sign-extension is required. (See Reference 1.)

As alluded to above, the various methods can be combined in a number of ways. The following is a list of the various combinations that were examined in this study. Almost all were applied to ALU sizes from 4 to 64 bits to identify the advantages and disadvantages of each. These will be summarized later.

Table I. Look-Ahead Carry Methods

1. Ripple
2. C_n
3. Shifted
4. Chained
5. Shifted Chain
6. Two Level
7. Two Level with Helpers
8. Shifted Two Level
9. Shifted Two Level with Helpers
10. Double Shifted Two Level
11. Double Shifted Two Level with Helpers
12. Three Level
13. Shifted Three Level
14. Double Shifted Three Level

FACTORS AFFECTING CHOICE

Before applying the look-ahead carry methods to the various word length ALUs, it may be worthwhile to look at some of the factors — other than raw speed — that could affect the choice of method. Some of these are:

1. parts count
2. board-to-board considerations
3. board space
4. sign extend
5. sequencer cycle time
6. board layout
7. word length expansion
8. different system architectures
9. current spiking

While parts count, board space, and board layout are more or less obvious considerations, the others deserve a brief comment:

A. Board-to-board considerations refer to those systems where half of the ALU is on one board and half is on another. Obviously all methods would not be readily adaptable to this situation if a sufficient number of connector pins is not available.

B. Sign-extend requirements may favor the method that frees a G,P input on one of the look-ahead carry circuits. This is explained more fully in Reference 1.

C. Sequencer cycle time, in a pipelined system, may be the limiting factor in overall system speed. Thus, saving a few nanoseconds in the ALU may not be worthwhile.

D. Future word length expansion is a consideration if several models of the same basic system are required. For example, 16 bits of address can address 64K words; twenty bits can address 1M words. If the ALU is used to compute addresses, the carry method optimized for 20 bits may be desirable.

E. The architecture that was assumed for this study will not be used in every system. Thus, the availability and timing of input signals, worst-case delay paths, and added components will affect the results shown in the following section. Thus, each design could require a separate study to achieve optimized results.

F. Current spiking is a consideration when one method causes several ALUs to change output states within a few nanoseconds of each other. If this causes system noise problems, perhaps an alternate method would be desirable.

APPLYING THE VARIOUS METHODS

In the following discussion, the IDM2901A-1 timing is used for the register-ALU elements. Because several different choices of pipeline register are available, the times shown do *not* include the clock-to-register output delay. Finally, the comparisons are based on the time required to add two registers and obtain a valid output, i.e., A + B → Y.

4, 8 Bits: Ripple carry is clearly the best from all considerations and thus no further discussion is necessary. Register-to-register add time for 8 bits is 75ns.

12 Bits: At present, the conventional single-level method is best (77 ns). However, if future bit-slices feature A, B → C_{n+4} as fast as A, B → $\overline{G}, \overline{P}$ and C_n → C_{n+4} as fast as the IDM2902's $\overline{G}, \overline{P} \rightarrow C_{n+y}$, ripple carry can be just as fast. (This illustrates the need for designers to continually rethink the problem as new parts become available.)

16 Bits: Without considering sign extend, the conventional approach [Figure 1(a)] is optimum (75 ns). The shifted method (Figure 2) is 8.5 ns slower under the assumptions made above, but if sign extend is required, it may well be as fast, in addition to eliminating multiplexers. (See Reference 1.) (This illustrates the fact that two parts of a system optimized independently may result in an overall slower system.)

20 Bits: As word width increases above 16 bits, some of the less conventional approaches begin to have some advantage. First, consider the more obvious approaches; the single level and chained approaches are shown in Figures 3(a) and 3(b). Another solution can be obtained by deleting parts from the conventional 32-bit solution of Figure 1(b). This is shown in Figure 3(c).

Note: In the figures that follow, connecting lines are simplified and terminal labels are eliminated for clarity.

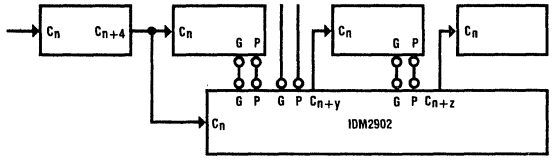


Figure 2. 16-Bit Shifted Look-Ahead

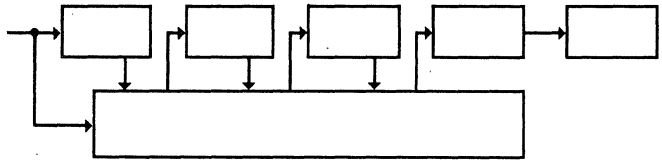


Figure 3(a). 20-Bit, Single-Level Method

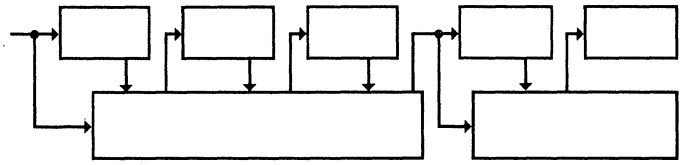


Figure 3(b). 20-Bit, Chained

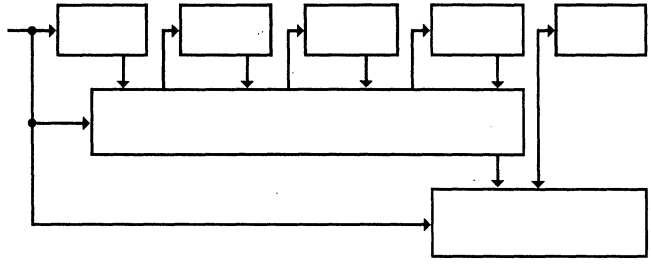


Figure 3(c). 20-Bit, Two-Level

From a timing standpoint, (b) and (c) of Figure 4 are both 87.5ns compared to 93ns for (a). The single-level method [Figure 3(a)] is superior from a parts count standpoint, requiring a single look-ahead carry rather than two. A closer look at Figure 3(c), however, reveals that only a small portion of the second look-ahead carry circuit is used. Furthermore, this portion can be replaced by a circuit consisting of 1/6 of a 74S04 and 1/2 of a 74S51 as shown in Figure 4. In addition to a lower power, lower cost solution, the replacement of the second look-ahead carry circuit actually saves 1.5ns!

Even more surprising is the fact that the shifted method shown in Figure 5 not only has the fewest parts, but also runs faster (85.5ns) than the other methods shown. Here is a situation where the speed-cost tradeoffs BOTH favor the same solution!

24, 28 Bits: Using the conventional 32-bit solution (deleting one or two ALUs) yields identical times (98ns) for both 24 and 28 bits. The shifted chain (Figure 6), however, uses fewer parts and is faster (96ns). With the same parts count, the chained and two-level methods yield the fastest times (87.5ns) for both 24- and 28-bit ALUs.

32 Bits: The conventional approach for 32 bits shown in Figure 1(b) is an example of the two-level with helpers method. For 32 bits, the register-to-register add time is 98ns for this method. This is a faster approach than the chained and two-level methods (103.5ns) that were optimum for 24 and 28 bits. Another method — the shifted two-level — again uses fewer parts and is considerably faster than the conventional approach (87.5ns). This is illustrated in Figure 7.

36, 40, 44 Bits: A 98ns solution can be obtained for 36-bit ALUs by simply deleting parts from the 64-bit solution of Figure 1(c). A word of caution: this is *not* the path to the most significant slice (MSS). It turns out that this path is only 87.5ns. The 98ns path is to the output of the second MSS. The shifted two-level with helper method (Figure 8) will also produce a 98ns result, but if the "helper" is replaced by the circuit of Figure 4, the result is 96.5ns.

Another solution, requiring only two parts, is shown in Figure 9. This solution — the double shifted two-level method — turns out to be the best two-part solution for all word sizes from 36 to 64 bits. Speed for this method is 101.5ns.

The shifted two-level with helper and double-shifted two-level methods turn out to be the optimum three-part and two-part solutions for 40- and 44-bit ALUs also.

48 Bits: As mentioned above, the double shifted two-level method shown in Figure 9 is also the optimum two-part solution for 48 bits. Three-part solutions are shown in Figure 10. The shifted three-level solution of Figure 10(a) results in a 114ns system. The double shifted three-level solution is 101.5ns. Note how the worst-case path varies between the two solutions. This points out the fact that several paths must be evaluated to ensure that the longest one has been found.

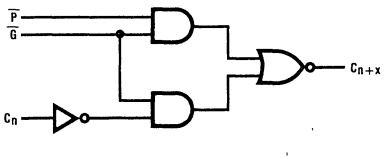


Figure 4. Partial Look-Ahead Carry Circuit

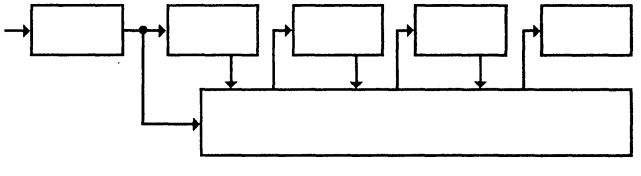


Figure 5. 20-Bit, Shifted

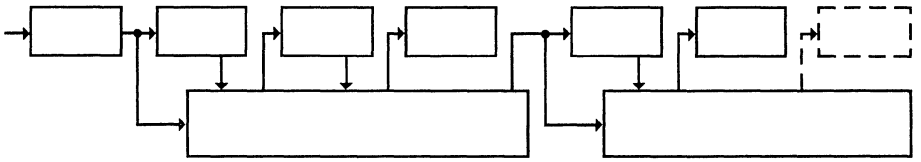


Figure 6. 24-, 28-Bit, Shifted Chain

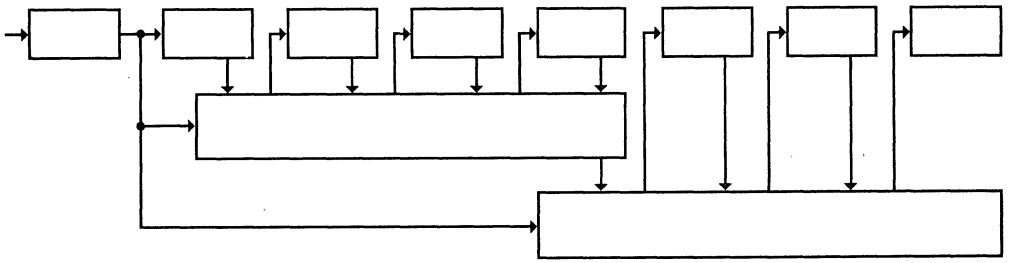


Figure 7. 32-Bit, Shifted Two-Level

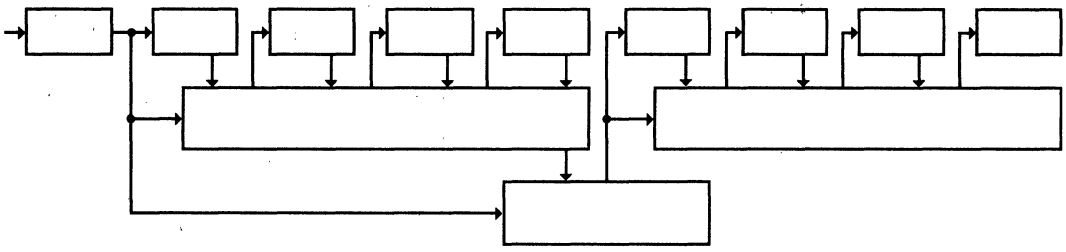


Figure 8. 36-Bit, Shifted Two-Level with Helper

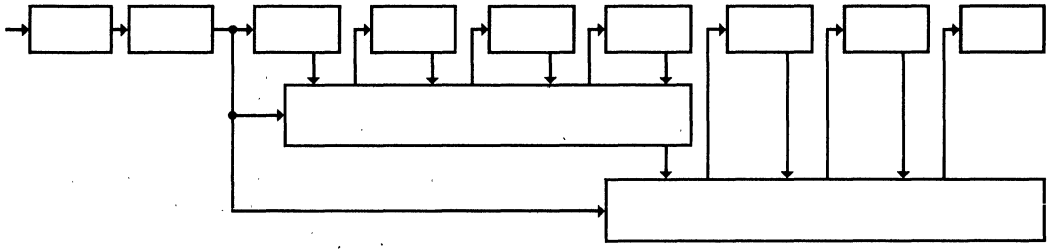


Figure 9. 36-Bit, Double-Shifted, Two-Level

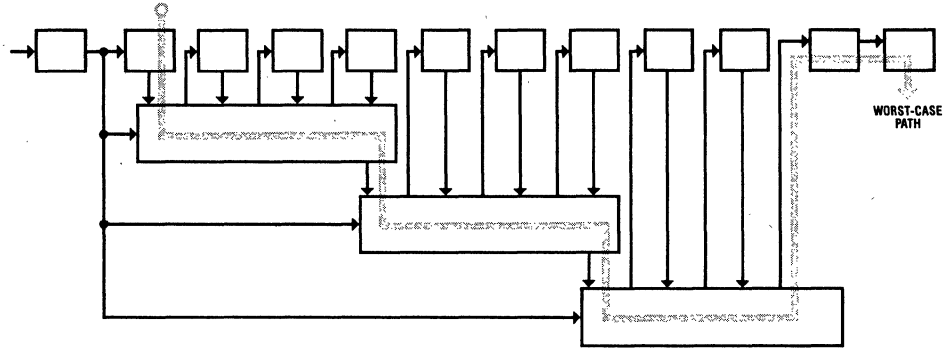


Figure 10(a). 48-Bit, Shifted, Three-Level

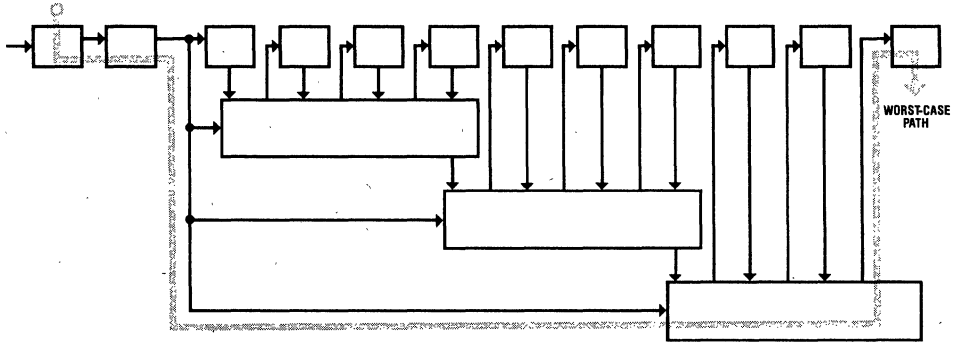


Figure 10(b). 48-Bit, Double Shifted, Three-Level

The four-part system of Figure 11 improves performance slightly (98ns) and may not be worth the additional expense. It is, however, the best four-part choice from 48 to 60 bits. This method is referred to as shifted two-level with helpers.

52 Bits: Not a particularly popular ALU size, the 52-bit system nevertheless provides an opportunity to demonstrate another look-ahead carry method — the double-shifted, two-level with helpers. This also turns out to be the fastest three-part method for word widths from 52 to 64 bits. This method, illustrated in Figure 12, results in 117.5ns for 52-bit systems.

56 Bits: ALUs of 56 bits are becoming common in floating point systems using 56 bits of mantissa and 8 bits of exponent. Deleting components from the conventional 64-bit approach [Figure 1(c)] results in a 98ns solution. This same speed, however, can be achieved with four parts using the shifted two-level with helper method of Figure 13.

60 Bits: The fastest 60-bit solution is the conventional approach for 64 bits [Figure 1(c)] with one alu deleted. This results in a 98ns solution. The shifted two-level with helper method (Figures 11 and 13) is a four-part solution that results in 103.5ns.

64 Bits: Again, the fastest 64-bit solution (98ns) is the conventional approach of Figure 1(c). The fastest four-part solution is a double-shifted two-level with helper method (117.5ns) illustrated in Figure 14.

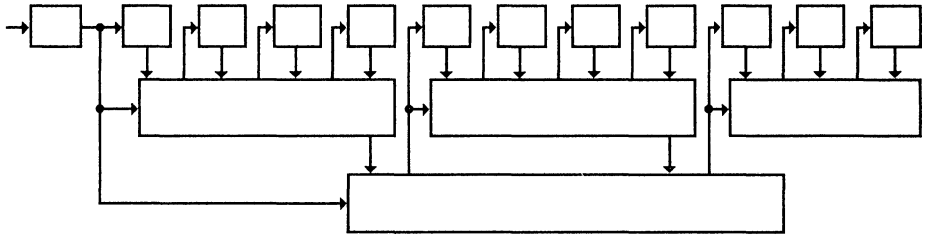


Figure 11. 48-Bit, Shifted Two-Level with Helpers

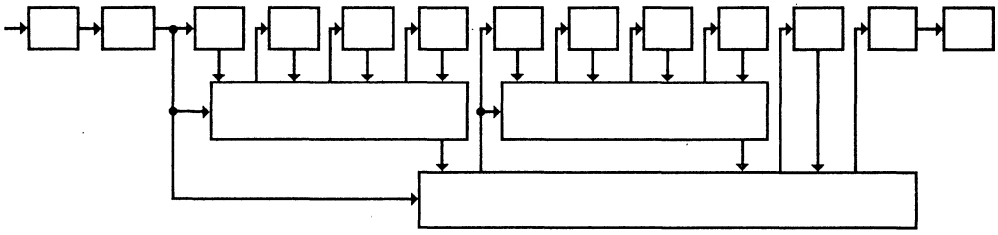


Figure 12. 52-Bit, Double-Shifted, Two-Level with Helpers

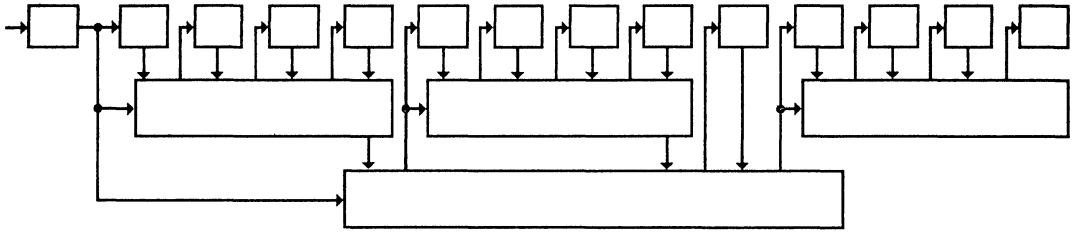


Figure 13. 56-Bit, Shifted, Two-Level with Helper

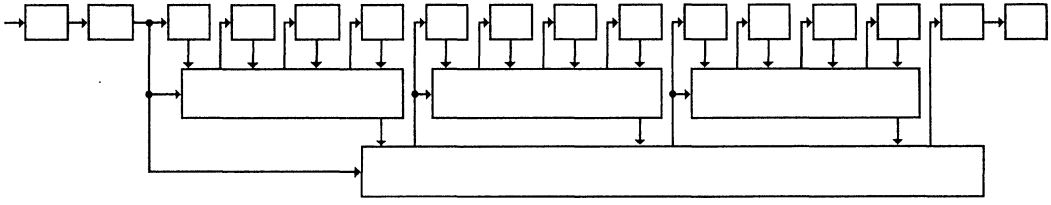


Figure 14. 64-Bit, Double Shifted, Two-Level with Helper

Table II is a summary of the data generated from this study. It lists, for each word size, the fastest solution for look-ahead carry parts count from 0 to 5. The number under the "Method" column corresponds to the numbered list of Table I. The fastest solution for each word size is shaded.

Table II. Optimum Speed for 4-64-Bit ALUs

Word Size	Number of IDM2902s											
	0		1		2		3		4		5	
	Method	Time	Method	Time	Method	Time	Method	Time	Method	Time	Method	Time
4	1	50										
8	1	75										
12	1	91	2	77								
16	1	107	2	77								
20	1	123	3	85.5	4	87.5						
24	1	139	3	101.5	4, 6, 8	87.5	7	98				
28	1	155	3	117.5	4, 6, 8	87.5	9	98				
32	1	171	3	133.5	8	87.5	9	98				
36	1	187	3	149.5	10	101.5	7, 9, 12	98				
40	1	203	3	165.5	10	117.5	4, 7, 9, 12	98				
44	1	219	3	181.5	10	133.5	9, 13	98				
48	1	235	3	197.5	10	149.5	14	101.5	7, 9	98		
52	1	251	3	213.5	10	165.5	11	117.5	7, 9	98		
56	1	267	3	229.5	10	181.5	11	133.5	9, 13	98	7	98
60	1	283	3	245.5	10	197.5	11	149.5	9	103.5	7, 9	98
64	1	299	3	261.5	10	213.5	11	165.5	11	117.5	7, 9	98

CONCLUSIONS

It may appear that a lot of time was spent investigating alternate look-ahead carry schemes that save "a few nanoseconds" in overall speed. While this is certainly true for systems with ALU cycle times in the 200ns range, it has been shown that with the more recent 2900 components from National Semiconductor, ALU cycle times in the 100ns region are certainly feasible, and here those same few nanoseconds could become significant. This will be even more apparent with the introduction of the IDM2901A-2, which will improve the register/ALU times listed in Table III by another 20-25%.

It has also been shown that no one solution is "best" for all applications. Even the "fastest" solution may not be optimum for a specific system when parts count, system wiring, board space, etc., are considered.

Table III. Delay Times Used to Calculate Cycle Time

IDM2901A-1:		IDM2902:	
$AB \rightarrow Y$	50ns	$\overline{G}, \overline{P} \rightarrow \overline{G}, \overline{P}$	10.5ns
$AB \rightarrow \overline{G}, \overline{P}$	45ns	$C_n \rightarrow C_{n+x,y,z}$	10.5ns
$AB \rightarrow C_{n+4}$	50ns	$\overline{G}, \overline{P} \rightarrow C_{n+x,y,z}$	7.0ns
$C_n \rightarrow C_{n+4}$	16ns		
$C_n \rightarrow Y$	25ns		

Finally, the entire study will soon be obsolete as new components with different (albeit faster) specifications are introduced. Therefore, the only conclusion that seems legitimate is that each application should be considered individually with the requirements of the system, the devices available, and sound engineering judgement determining the optimum solution. It is hoped that the information contained in this application note will provide some guidelines for finding that solution.

REFERENCES

1. AN-203, Bit-Slice Microprocessor Design Takes a Giant Step Forward with "Schottky-Coupled-Logic" Circuits.
2. AN-217, High Speed Bit-Slice Microsequencing Design.

Section 24
Programmable Logic

24

Introduction And General Description

What is a PAL?

A PAL is a user-programmable array of logic gates which allows the equivalent of a number of SSI and MSI (small- and medium-scale integration) packages to be implemented on a single chip. NSC's PAL series are Schottky TTL (transistor-transistor logic) components, and hence offer both speed and easy interfacing. Combinations of registers, flip-flops, and random logic are all easily implemented using PALs.

Why Should You Use A PAL?

Reduced board space

PALs typically implement the equivalent of from 4 to 12 SSI and MSI packages in a single 20-pin DIP. If the amount of space on your PCB is insufficient for your needs, you should seriously consider using PALs in your design.

Cost Effectiveness

The total manufacturing cost of a circuit implemented with PALs is frequently less than that of standard ICs. Only 25 to 50 per cent of the cost of utilizing an SSI or MSI chip is normally its purchase price; the remaining 50 to 75 per cent is tied up in the cost of the PCB area, assembly, and testing associated with that chip. Hence, as the PAL replaces more and more chips, its usage quickly becomes justified on a cost basis alone.

Fast System Design

Because of PALs' programmability and flexibility, the time needed to design and implement a system can be cut in half. Breadboards can be built quickly to test out new ideas without long waiting.

Design Flexibility

PALs offer the design engineer greater flexibility than standard, off-the-shelf parts. If a desired function is not readily available with standard components, an awkward assortment of chips may be needed to implement the function. With PALs, the engineer simply chooses what he wants instead of taking what he can get.

Easy Design Changes

PALs offer the designer the ability to reprogram an IC instead of redesigning other hardware and laying out a new PCB when the function of the card changes.

High Speed

PALs are built using Schottky technology. Register PALs clock at 40 MHz, with faster parts on the way.

Easy Field Programming

Unlike gate arrays and other approaches to custom logic design, the PAL is user-programmable, which minimizes turnaround time. The PAL can be programmed quickly and easily using standard PROM programmers with appropriate personality cards. Conversion of logic functions into the PAL format is accomplished quickly and easily using a software tool called PALASM™

Small Inventory

The PAL family can be used to replace up to 90 per cent of TTL components with just 15 different parts. This considerably lowers inventory costs.

What Is The Impact Of PAL On Logic Design?

Logic designers are noticing an apparent "complexity gap" between TTL and LSI. Products designed using discrete TTL devices would consume unacceptable amounts of physical space and electrical power. Software programmable LSI devices (microprocessors) offer high density and need relatively little power to do almost anything imaginable, but the designer pays a high price in software development and still has to use discretes to interface them to the outside world. Until recently, there has been no device that provides a really effective way of bridging this gap. National Semiconductor Company has seen this need, and now offers the designer a family of PAL (Programmable Array Logic) devices to fill it. PALs offer powerful capabilities for

creating cost-effective new products or for improving the effectiveness of existing logic designs. PAL devices save time and money by solving many of the system partitioning and interface problems not otherwise effectively solved by today's semiconductor device technology.

LSI (Large scale integration) offers many advantages, but advances have been made at the expense of either device flexibility or software complexity. LSI technology has been and still is leading to larger and larger standard logic functions. LSI offers high functional density and low power consumption; single ICs now perform functions that formerly required complete circuit cards. However, most LSI devices don't interface with user systems without large numbers of support devices. Designers are still forced to turn to random logic for many applications. LSI is slow, and it is rigidly partitioned. For all its capability to perform varied and complex tasks, the microprocessor is a slow and expensive way of doing simple, repetitive tasks when the necessary interface and other support devices are added, and when the time, money, and memory required for software development are considered.

TTL provides speed, and you could say its flexibility is infinite, but its price is high power consumption, large parts count, and low space utilization.

Custom IC's can be effective design solutions if the product is of low-to-medium complexity, its logic function is well defined, and its market is high volume. Its design cycle is typically long, and its cost can be prohibitive. This tends to discourage its use.

Fuse-programmable devices of various kinds have been invented to try to overcome the above-mentioned disadvantages. All but PAL require external interface logic, and all but PAL have disadvantages, to wit:

PROM: Requires careful design to avoid undesirable data transitions. Also limited on the number of input variables it can accommodate.

FPLA: Is expensive, difficult to program, and hard to understand.

FPGA: Isn't widely available, and lacks flexibility.

PMUX: Is available in only a few types.

The PAL—A New Extension of Fusible-Link Technology

The diode matrix was the first programmable integrated-circuit logic device, introduced in the early 1960's. This device contained only a diode-logic OR matrix, each crosspoint of which had a fusible link.

The programmable read-only memory (PROM) extended the programmable logic concept considerably by allowing input variables to be encoded, by reducing the number of pins required per input variable, and by providing TTL compatibility. The PROM is an AND-OR logic element with fixed AND matrix and programmable OR.

One advantage of using PROMS is that they are produced in high volume because they are used in many applications. Also, the PROM is a universal logic solution; in other words, all the product terms of the input variables are generated, making it possible to implement any AND-OR function of these variables.

The Field-Programmable Logic Array (FPLA) has a second fuse matrix (an AND matrix), so allows the designer to select and program only those product terms used in each specific function. These product terms are then combined in the OR fuse array to form an AND-OR logic equation. More about these later.

How It Works (See Figure 1-1.)

In the PAL concept, an AND fuse array allows the designer to specify the product terms required, and connect them to an OR matrix chosen to perform the required combination of AND-OR logic functions. PALs are offered in a number of different part types that vary the OR-gate configuration. Specifying the OR-gate connection therefore becomes a task of device selection rather than of programming, as with the FPLA. With this approach, PALs eliminate the need for a second fuse matrix with little loss in overall flexibility. Figure 1 is a schematic diagram that shows how a typical PAL circuit processes a two-input, one-output logic segment. The general logic equation for this segment is:

$$\text{Output} = (I_1 \cdot f_1 + /f_1)(/I_1 \cdot f_2 + /f_2)(I_2 \cdot f_3 + /f_3)(/I_2 \cdot f_4 + /f_4) + (I_1 \cdot f_5 + /f_5)(/I_1 \cdot f_6 + /f_6)(I_2 \cdot f_7 + /f_7 + /f_7)(I_2 \cdot f_8 + /f_8)$$

where the "f" terms represent the states of the fuse links in the PAL's AND array. In the above equation, an intact fuse is represented by f = 1, and a blown fuse by f = 0.

Although logic equations are convenient for simple functions, they become progressively less tractable as the functions become more complex. In large systems, the logic diagram, or schematic, and the truth table are the methods more commonly used to describe

logic networks. For simplicity, PAL logic is described in this book using the symbolic notation shown at right in Figure 1-2. The conventional, combinational logic diagram of the same expression is shown at left. In the figure, an X represents an intact fuse which, in conjunction with the series diode (not shown schematically), performs the logical AND function.

The two-input, one-output example shown in Figure 1-1, redrawn using the new logic notation, is depicted in Figure 1-3.

Figure 1-4 is the normal combinational logic diagram of an example whose transfer function is as follows:

$$\text{Output} = I_1 \bullet /I_2 + /I_1 \bullet I_2$$

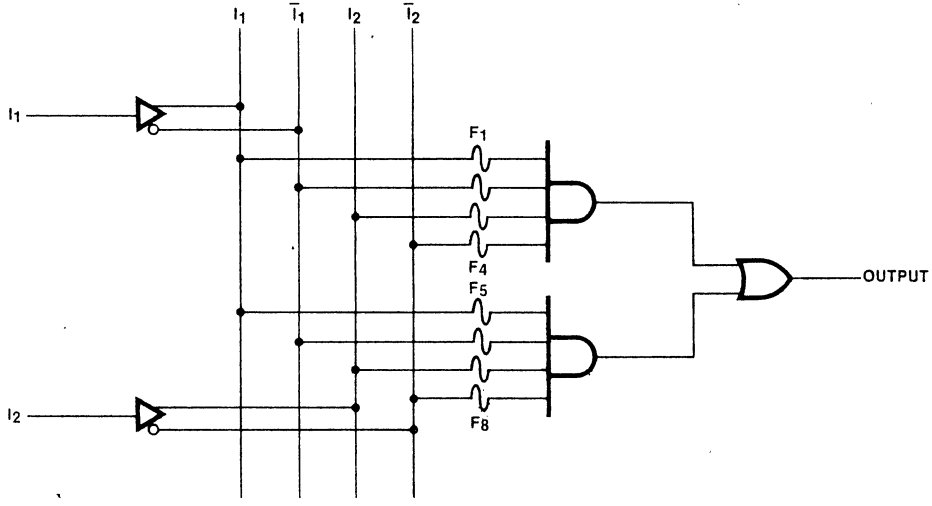


FIGURE 1-1. Partial Logic Diagram of a PAL®

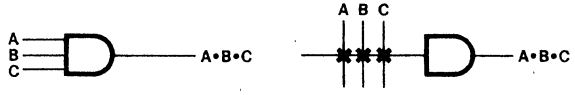


FIGURE 1-2. Conventional and PAL Logic Notation.

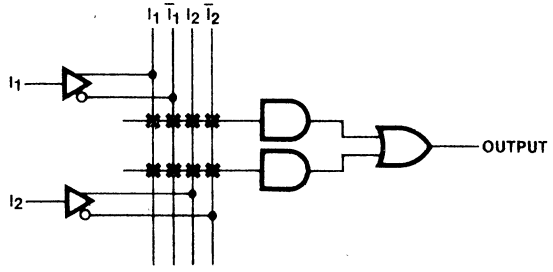


FIGURE 1-3. Two-input, One-output PALCircuit, Unprogrammed.

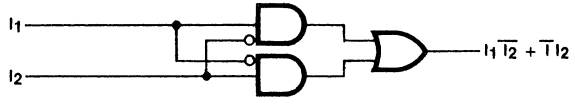


FIGURE 1-4. Logic Diagram of the Expression Shown Above

As can be seen from the expression and diagram, this is a two-input, one-output circuit; hence, the circuit of Figure 1-3 appears to be a good candidate to solve this problem. Removing the Xs from the junctions that do not represent terms of the example Boolean expression results in the diagram shown in Figure 1-5, which is the same PAL circuit shown in Figure 1-3, except that the appropriate fuses are blown.

Using the symbology described here not only displays the attributes of a logic diagram, but also those of the truth table for the same expression diagrammed. With this technique, it is possible to compare the structure of the PAL with those of the familiar PROM and PLA.

Comparison

To illustrate the differences among the three field-programmable logic concepts, each of the approaches is shown as an AND matrix, followed by an OR matrix. The basic logic implemented by the PROM is AND-OR, with the AND gates all preconnected on the chip, making this portion fixed, while the OR matrix is implemented with diode-fuse interconnections, making it programmable. Thus, the PROM is an AND-OR logic element with fixed AND matrix and programmable OR. The PROM solution in Figure 1-6 requires a 64-fuse matrix. There are many advantages to using PROMs as logic devices. One is that because they are used in many applications, they are produced in high volume. Also, the PROM is a universal logic solution; in other words, all the product terms of the input variables are generated, making it possible to implement any AND-OR function of these variables. However, PROMs cannot accommodate large numbers of variables; the maximum number of input variables currently being realized is 11.

The Field-Programmable Logic Array (FPLA) has a second fuse matrix (an AND matrix), allowing the designer to select and program only those product terms used in each specific function. (See Figure 1-7.) These product terms are then combined in the OR fuse array to form an AND-OR logic equation.

The typical FPLA implementation has less than 2^n terms available (with n as the number of input variables). This allows the FPLA to accommodate larger values of n, i.e., more inputs, in contrast with the PROM, where the number of product terms is always equal to 2^n. Although the FPLA usually requires fewer fuses to implement a given logic function, additional circuitry is required to select and program these fuses—circuitry that is not used in the final logic solution, but which is paid for in die area. This "chip overhead" cost becomes significant for simple applications that leave logic unused.

The basic logic structure of the PAL, consisting of a programmable AND array whose outputs feed a fixed OR array, is shown in Figure 1-8. The PAL is low in cost and easy to program, like the PROM, but also is more flexible, like the FPLA. Table 1-1 lists the characteristics of the three principal families of devices described here, and also others, for comparison.

Table 1-1.
Programmable Logic Device Summary

Device	AND	OR	Output Options
PROM	Fixed	Prog	TS,OC
FPLA	Prog	Prog	TS,OC,Fusible Polarity
FPGA	Prog	None	TS,OC,Fusible Polarity
PMUX	Fix/Prog	Fixed	TS
PAL	Prog	Fixed	TS,Registers,Feedback,I/O

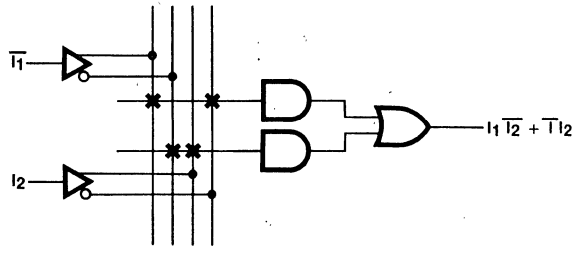


FIGURE 1-5. Blown Junctions Make the PAL Useful.

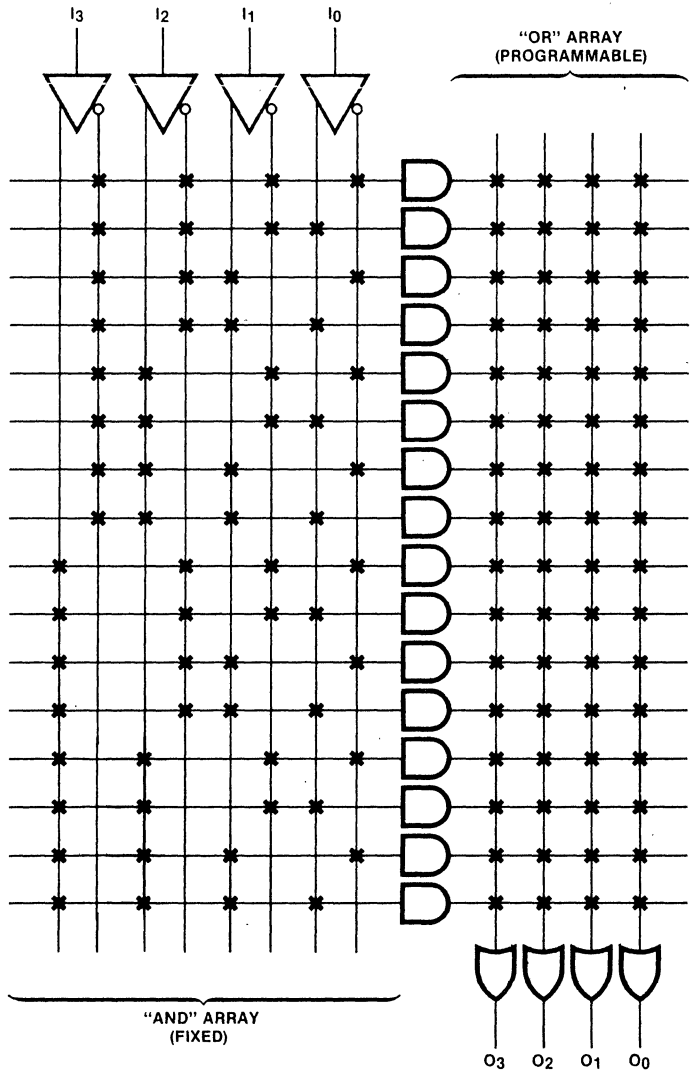


FIGURE 1-6. PROM Having 16 Words x 4 Bits.

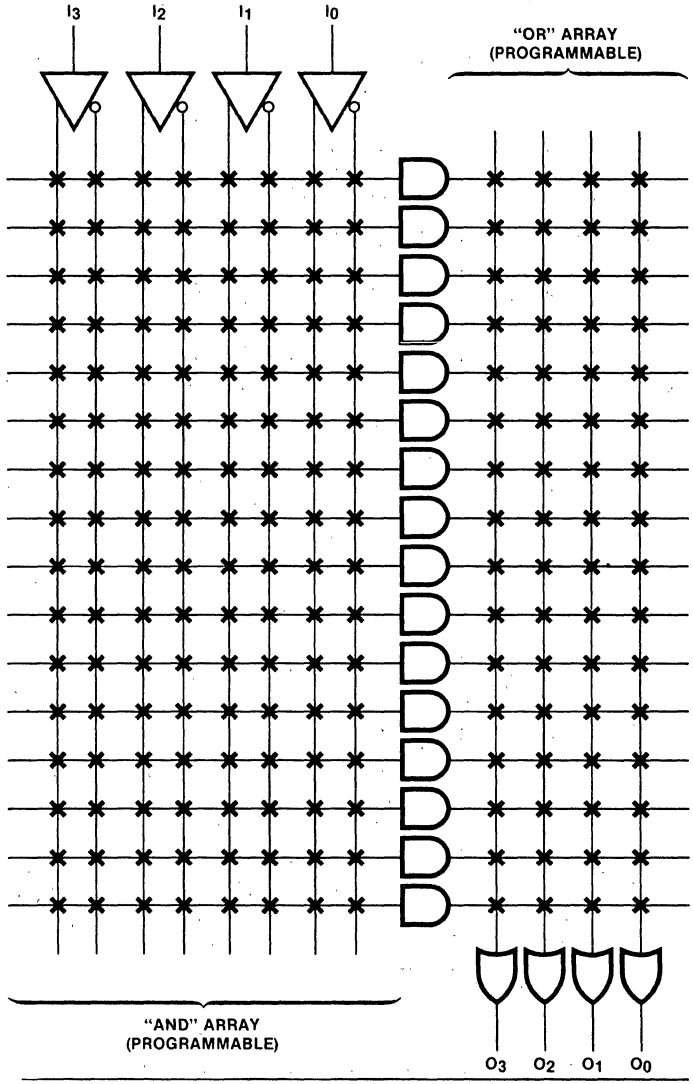


FIGURE 1-7. FPLA Having 4 Inputs, 4 Outputs, and 16 Products.

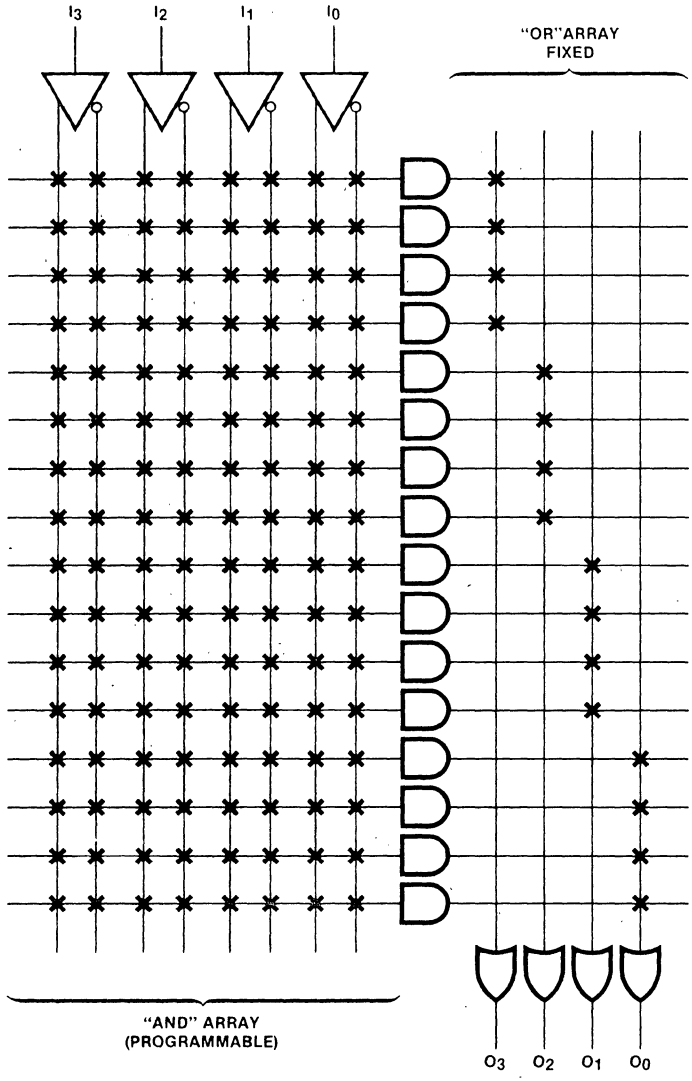


FIGURE 1-8. PAL Having 4 Inputs, 4 Outputs, and 16 Products.

TABLE 1-2. THE PROGRAMMABLE ARRAY LOGIC (PAL®) FAMILY

Std (35 ns)	High Speed (25 ns)	Pkg Pin	Description
10H8	10H8A	20	10 input, 8 output AND-OR array
12H6	12H6A	20	12 input, 6 output AND-OR array
14H4	14H4A	20	14 input, 4 output AND-OR array
16H2	16H2A	20	16 input, 2 output AND-OR array
10L8	10L8A	20	10 input, 8 output AND-OR array
12L6	12L6A	20	12 input, 6 output AND-OR array
14L4	14L4A	20	14 input, 4 output AND-OR array
16L2	16L2A	20	16 input, 2 output AND-OR array
16C1	16C1A	20	16 input, 1 output AND-OR/NOR array
16L8	16L8A	20	16 input, 8 output AND-OR-invert array
16R8	16R8A	20	16 input, 8 output AND-OR-register array
16R6	16R6A	20	16 input, 6 output AND-OR-register array
16R4	16R4A	20	16 input, 4 output AND-OR-register array
16X4		20	16 input, 4 output AND-OR-XOR-register array
16A4		20	16 input, 4 output AND-CARRY-OR-XOR register
12L10		24	12 input, 10 output AND-OR invert array
14L8		24	14 input, 8 output AND-OR-invert array
16L6		24	16 input, 6 output AND-OR-invert array
18L4		24	18 input, 4 output AND-OR-invert array
20L2		24	20 input, 2 output AND-OR-invert array
20C1		24	20 input, 1 output AND-OR/NOR array
20L10		24	20 input, 10 output AND-OR-invert array
20X10		24	20 input, 10 output AND-OR-XOR-register array
20X8		24	20 input, 8 output AND-OR-XOR-register array
20X4		24	20 input, 4 output AND-OR-XOR-register array

PALs For Every Task

The members of the PAL family are listed in Table 1-2. They are designed to cover the spectrum of logic functions at lower cost and lower package count. This allows you to select the PAL that best fits your application. PALs come in four basic configurations:

- Gates
- Register Outputs With Feedback
- Programmable I/O
- Arithmetic Functions

Gates

For 20/20A series, PALs are available in sizes from 10 × 8 (10 inputs 8 outputs) to 16 × 2, with either active-high or active-low output configurations. For 24 series, PALs are available in sizes from 12 × 10 to 20 × 2 with active-low output configurations. One part has complementary outputs with both series. This wide variety of input/output formats allows the PAL to replace many different-sized blocks of combinational logic with single packages.

Register Outputs With Feedback

High-end members of the PAL family feature latched data outputs with register feedback. Each sum or product term is stored in a D flip-flop on the rising edge of the system clock. (See Figure 1-9.) The Q output of the flip-flop can then be gated to the output pin by enabling the active-low TRI-STATE® buffer.

In addition to being available for transmission, the Q output is also fed back into the PAL array as an input term. This feedback allows the PAL to "remember" its prior state, and it can alter its function based upon that state. This allows you to configure the PAL as a state machine that can be programmed to execute elementary functions such as count up, count down, skip, shift, and branch.

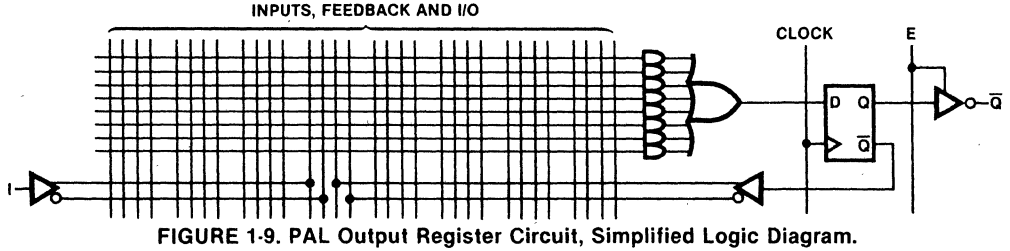


FIGURE 1-9. PAL Output Register Circuit, Simplified Logic Diagram.

Programmable I/O

Another feature of the high-end members of the PAL family is programmable input/output. This allows the product terms to directly control the outputs of the PAL. (See Figure 1-10.) One product term is used to enable the TRISTATE® buffer, which in turn gates the summation term to the output pin. The output is also fed back into the PAL array as an input. Thus, the PAL drives the I/O pin when the TRISTATE® gate is enabled; the I/O pin is an input to the PAL array when the TRISTATE® gate is disabled. This feature can be used to allocate available pins for I/O functions or to provide bidirectional output pins for operations such as shifting and rotating serial data.

Arithmetic Functions

The arithmetic functions add, subtract, greater than, and less than are implemented by two additional features of the register PAL. (See Figure 1-11.) First, the sums that are XORed at the input of a D flip-flop. This allows carries from previous operations to be XORed with current sums generated by the PAL array. Second, the Q output of the flip-flop is ORed with an input to form the terms I + Q, I + /Q, I + Q, and /I + /Q, which are then fed back into the PAL matrix. This option provides for versatile operations on two variables and facilitates the parallel generation of carries necessary for fast arithmetic operations. Figure 1-12 shows a PAL array, programmed to combine the available terms to form 16 logical products in an ALU or controller application.

Technology

National Semiconductor PALs are manufactured using the same high-volume technology used in the manufacture of PROMs. This includes state-of-the-art Schottky processing, dual-layer metal, and highly reliable titanium-tungsten fuses. NPN emitter followers make up the programmable AND array. The inputs are PNP transistors whose input impedance imposes a current drain of not more than 0.25 mA on the source. All outputs are standard TTL drivers with internal active-pullup transistors. Typical PAL propagation delay is 25 ns for the standard version.

Packaging

All PAL versions are supplied in the space-saving 20 and 24-pin, 0.3-in. "thin-dip" package. This package offers one of the best pin-count-to-area ratios available.

PALS also utilize National's copper-lead-frame plastic package design that combines the low cost of plastic with the thermal characteristics of CERDIP to provide highly reliable, cost-effective components.

Programming PALs are designed to be programmed using standard, commercially available PROM programmers with the addition of the proper personality module and socket adapters. Some programmers with PAL programming capability are listed in the PAL Design section.

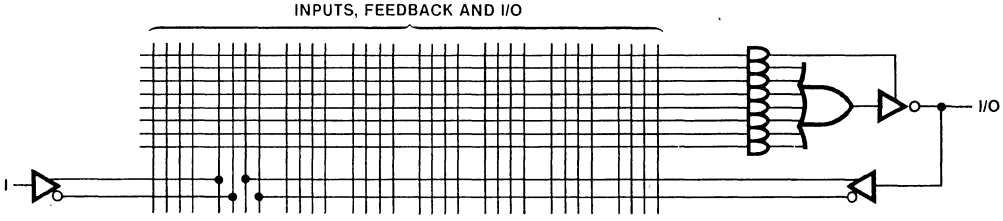


FIGURE 1-10. PAL Bidirectional Circuit, Logic Diagram.

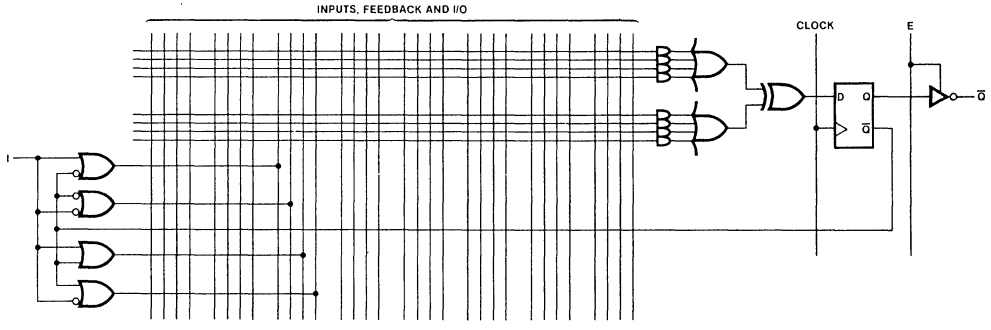


FIGURE 1-11. Logic Structure of an Arithmetic PAL.

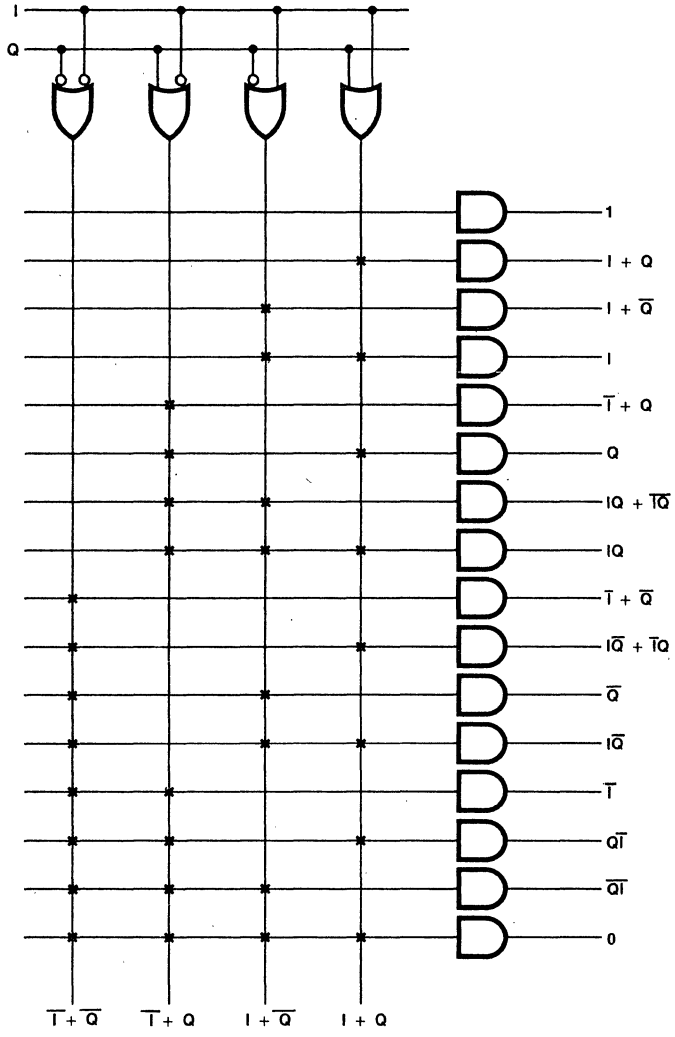


FIGURE 1-12. PAL Coding to Perform Typical ALU Functions.

PAL Part Numbers

The PAL part number reveals the logic operation the part performs. (See Figure 1-13.) The example shown, the DMPAL16L2NC, is a device that accommodates 16 input terms and generates 2 active-low output terms, is contained in a 20-pin plastic dual-inline package, and meets commercial temperature-range specifications.

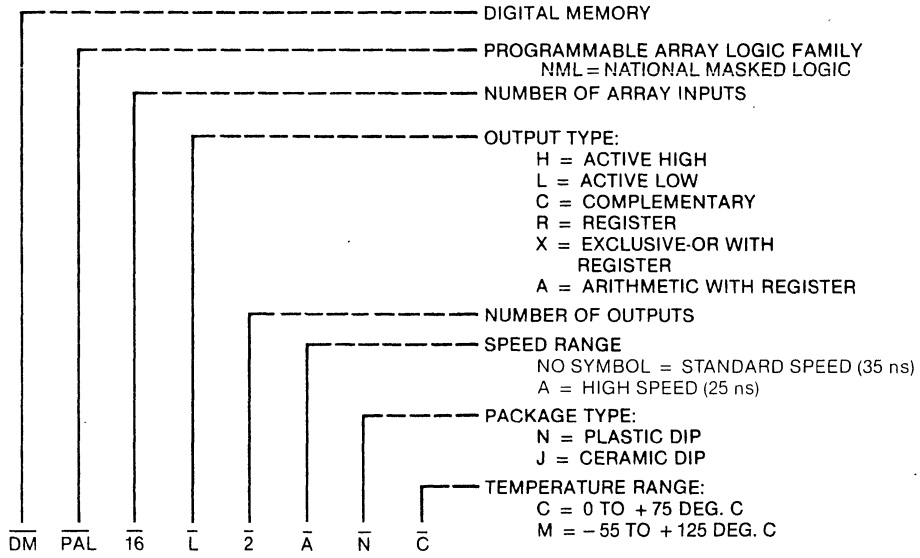


FIGURE 1-13. Meaning of PAL Part Number Code

PAL Logic Symbols

The logic symbols for each of the individual PAL devices gives a concise functional description of that device. Figure 1-14 shows a typical logic symbol, that of the 10H8 gate array.

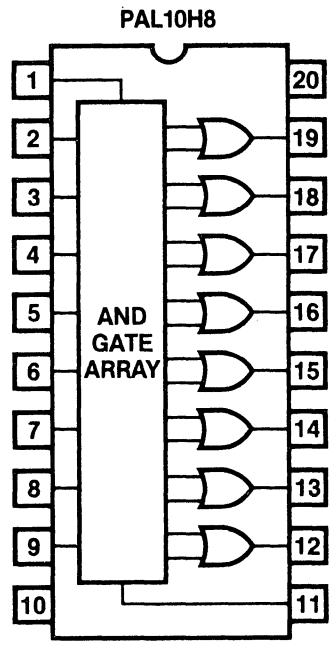
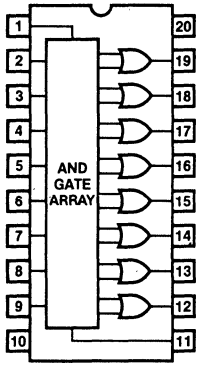


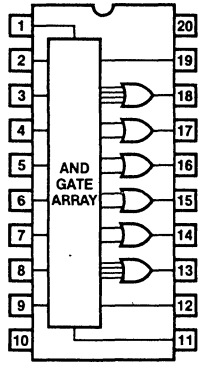
FIGURE 1-14. Logic Symbol, DMPAL10H8.

PAL Logic Symbols — Series 20

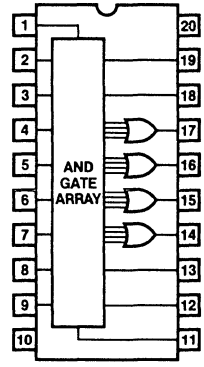
DMPAL10H8



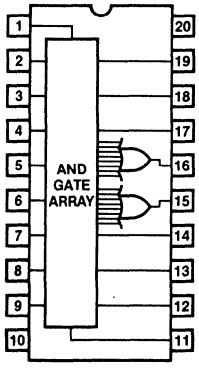
DMPAL12H6



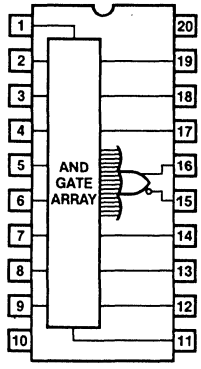
DMPAL14H4



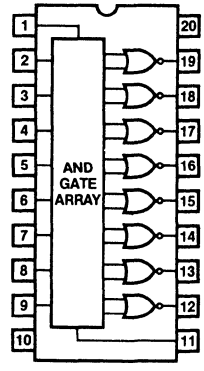
DMPAL16H2



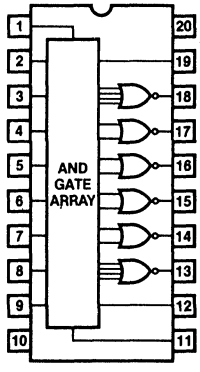
DMPAL16C1



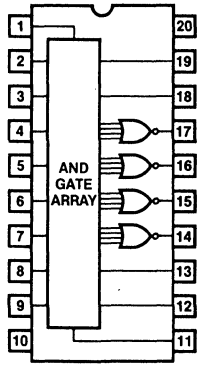
DMPAL10L8



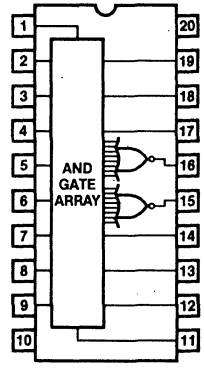
DMPAL12L6



DMPAL14L4

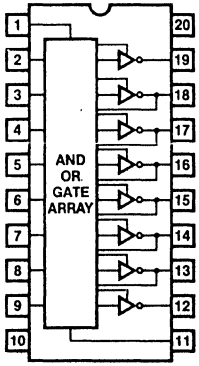


DMPAL16L2

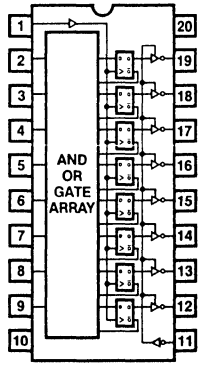


PAL Logic Symbols - Series 20 (Contd.)

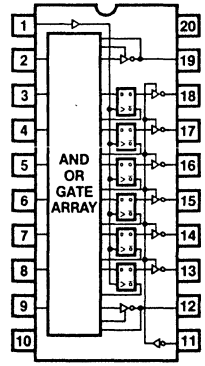
DMPAL16L8



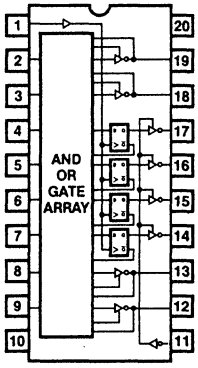
DMPAL16R8



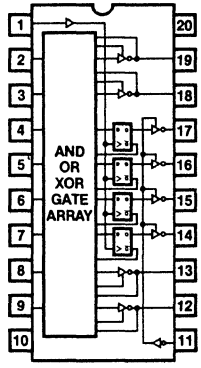
DMPAL16R6



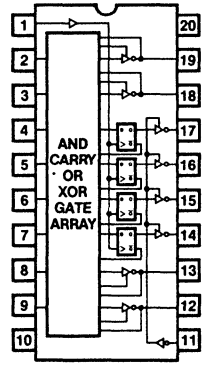
DMPAL16R4



DMPAL16X4

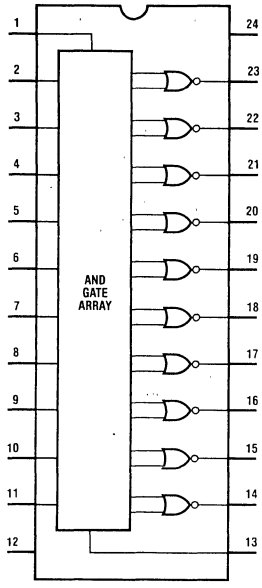


DMPAL16A4

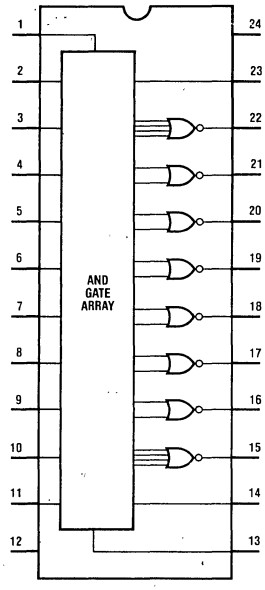


PAL Logic Symbols - Series 24

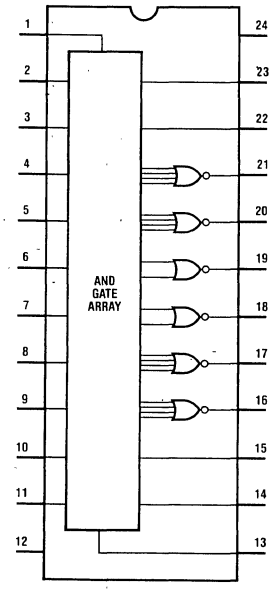
PAL12L10



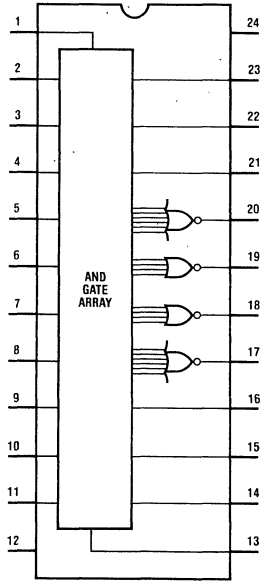
PAL14L8



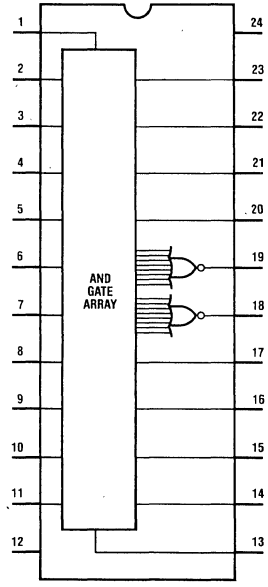
PAL16L6



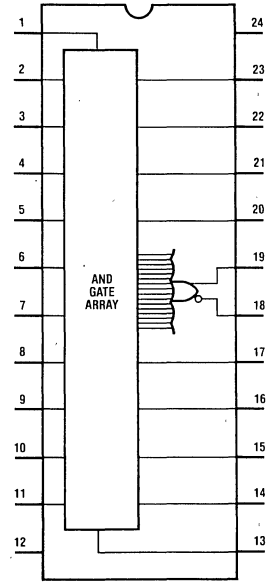
PAL18L4



PAL20L2

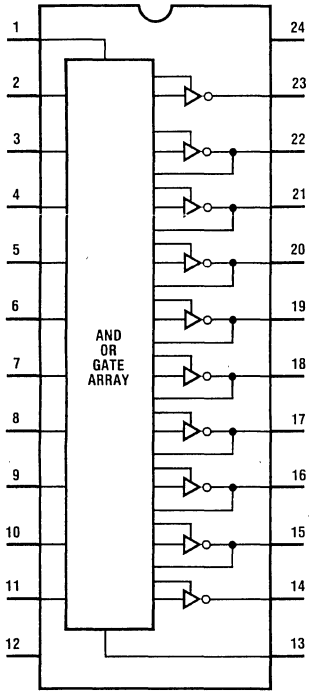


PAL20C1

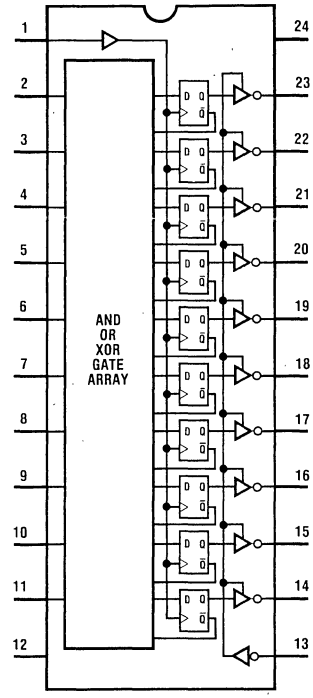


PAL Logic Symbols · Series 24 (Contd.)

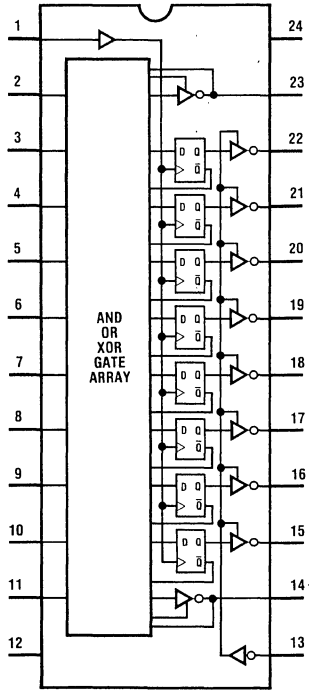
PAL20L10



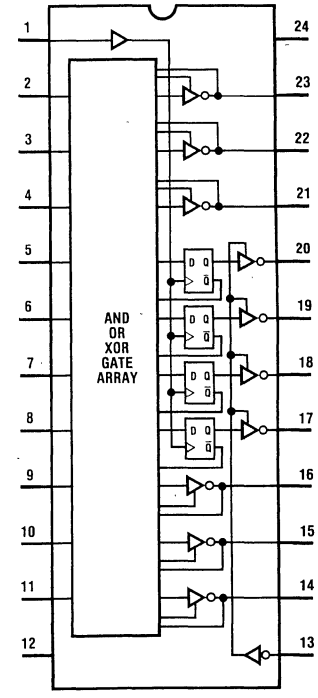
PAL20X10



PAL20X8



PAL20X4



National Semiconductor

DATA SHEETS

Programmable Array Logic (PAL®) Series 20/20A

Description

The PAL® family utilizes National Semiconductor's Schottky TTL process and bipolar PROM fusible-link technology to provide user-programmable logic to replace conventional SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PALs is greater than 4:1.

The family lets the systems engineer customize his chip by opening fusible links to configure AND and OR gates to perform his desired logic functions. Complex interconnections that previously required timeconsuming layout are thus transferred from PC board to silicon where they can be easily modified during prototype checkout or production.

The PAL transfer function is the familiar sum of products with a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array. (The PROM is a fixed AND array driving a programmable OR array.) In addition, the PAL family offers these options:

- Variable input/output in ratio.
- Programmable TRISTATE® outputs.
- Registers and feedback.

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops that are loaded on the low-to-high transition of the clock. PAL logic diagrams are shown with all fuses blown, enabling the designer to use the diagrams as coding sheets.

The entire PAL family is programmed on conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to make verification difficult. This feature gives the user a proprietary circuit that is very difficult to copy.

Features

- Programmable replacement for conventional TTL logic.
- Simplifies prototyping and board layout.
- Thin DIP packages.
- Reliable titanium-tungsten fuses.
- Available in standard and high speed versions.
- 25 ns max propagation delay for high speed versions (20A series)

Table 2-1. Part Types

Part Number	Description
PAL10H8	OCTAL 10 INPUT AND-OR GATE ARRAY
PAL 12H6	HEX 12 INPUT AND-OR GATE ARRAY
PAL 14H4	QUAD 14 INPUT AND-OR GATE ARRAY
PAL 16H2	DUAL 16 INPUT AND-OR GATE ARRAY
PAL 16C1	16 INPUT AND-OR/AND-OR-INVERT GATE ARRAY
PAL 10L8	OCTAL 10 INPUT AND-OR-INVERT GATE ARRAY
PAL 12L6	HEX 12 INPUT AND-OR-INVERT GATE ARRAY
PAL 14L4	QUAD 14 INPUT AND-OR-INVERT GATE ARRAY
PAL 16L2	DUAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL 16L8	OCTAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL 16R8	OCTAL 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL 16R6	HEX 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL 16R4	QUAD 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL 16X4	QUAD 16 INPUT REGISTERED AND-OR-XOR GATE ARRAY
PAL 16A4	QUAD 16 INPUT REGISTERED AND-CARRY-OR-XOR GATE ARRAY

Part Number	Description
PAL10H8A	OCTAL 10 INPUT AND-OR GATE ARRAY
PAL12H6A	HEX 12 INPUT AND-OR GATE ARRAY
PAL14H4A	QUAD 14 INPUT AND-OR GATE ARRAY
PAL16H2A	DUAL 16 INPUT AND-OR GATE ARRAY
PAL16C1A	16 INPUT AND-OR/AND-OR-INVERT GATE ARRAY
PAL10L8A	OCTAL 10 INPUT AND-OR INVERT GATE ARRAY
PAL12L6A	HEX 12 INPUT AND-OR-INVERT GATE ARRAY
PAL14L4A	QUAD 14 INPUT AND-OR-INVERT GATE ARRAY
PAL16L2A	DUAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL16L8A	OCTAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL16R8A	OCTAL 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16R6A	HEX 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16R4A	QUAD 16 INPUT REGISTERED AND-OR GATE ARRAY

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	7.0 V	12 V
Input voltage	5.5 V	12 V
Off-state output voltage	5.5 V	12 V
Storage temperature range	−65°C to	150°C

10H8, 12H6, 14H4, 16H2, 16C1, 10L8, 12L6, 14L4, 16L2

Electrical Characteristics

Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = MIN I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX V_I = 5.5 V			1.0	mA
I_{IH}	High-level input current	V_{CC} = MAX V_I = 2.4V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX V_I = 0.4V			−250	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX V_O = 0V	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX		55	90	mA

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Unit
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			−2.0			−3.2	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free air temperature	−55		125	0		75	°C

Switching Characteristics

Over Recommended Ranges of Temperature and V_{CC}

Symbol	Parameter	Test Conditions†† R1 = 560Ω R2 = 1.1 kΩ	Military T_A = −55° to +125°C V_{CC} = 5.0V ±10%			Commercial T_A = 0° to 75°C V_{CC} = 5.0V ± 5%			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{PD}	From any input to any output	C_L = 15pF		25	45		25	35	ns

16L8, 16R8, 16R6, 16R4, 16X4, 16A4
Electrical Characteristics
Over Recommended Operating Temperature Range

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage		V_{CC} = MIN I_I = -18 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN V_{IH} = 2V V_{IL} = 0.8V I_{OL} = MAX			0.5	V
I_{OZH}	Off-state output current high-level voltage applied		V_{CC} = MAX, V_{IH} = 2V, V_O = 2.4V, VIL = 0.8V			100	μA
I_{OZL}	Off-state output current low-level voltage applied		V_{CC} = MAX, V_{IH} = 2V V_O = 0.4V, VIL = 0.8V			−100	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX V_I = 5.5 V			1.0	mA
I_{IH}	High-level input current		V_{CC} MAX V_I = 2.4V			25	μA
I_{IL}	Low-level input current		V_{CC} MAX V_I = 0.4V			−250	μA
I_{OS}	Short-circuit output current		V_{CC} = MAX V_O = 0V	−30		−130	mA
I_{CC}	Supply Current	16L8	V_{CC} = MAX		140	180	mA
		16R4,16R6,16R8			150	180	

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Unit
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			−2.0			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free air temperature	−55		125*	0		75	°C

*Operating Case Temperature only, T_C = 125°C

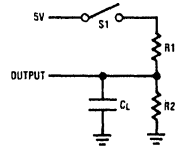
Switching Characteristics

Over Recommended Ranges of Temperature and V_{CC}

Symbol	Parameter		Test Conditions†† R1, R2	Military T_A = −55° to +125°C V_{CC} = 5.0V ±10% Min	Typ	Max	Commercial T_A = 0° to 75°C V_{CC} = 5.0V ± 5% Min	Typ	Max	Unit
t_{PD}	Input to output		C_L = 50pF		25	45		25	35	ns
t_{PD}	Clock to output				15	25		15	25	ns
t_{PZX}	Pin 11 to output enable				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable		C_L = 5pF		15	25		15	25	ns
t_{PZX}	Input to output enable		C_L = 50pF		25	45		25	35	ns
t_{PXZ}	Input to output disable		C_L = 5pF		25	45		25	35	ns
t_w	Width of clock	High		25			25			ns
		Low		25			25			
t_{su}	Setup time	16R8,16R6,16R4		45			35			ns
		16X4,16A4								
t_h	Hold time			0		−15	0		−15	ns

††See Standard Test Load and Definition of Waveforms

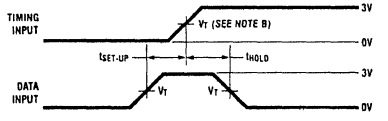
Standard Test Load



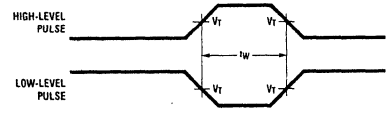
MEDPAL		SMPAL
MIL	COM'L	
R1 = 390	R1 = 200	R1 = 560
R2 = 750	R2 = 390	R2 = 1.1k

Test Waveforms

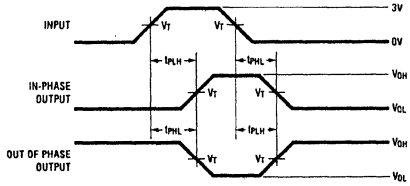
Set-Up and Hold



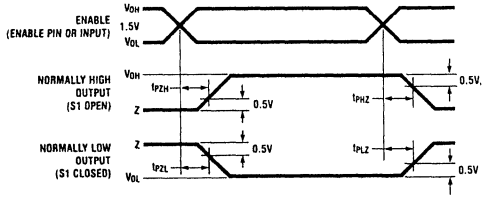
Pulse Width



Propagation Delay



Enable and Disable



Note A: C_L includes probe and jig capacitance.

Note B: V_T = 1.5V.

Note C: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Note D: All input pulses are supplied by generators having the following characteristics: PRR = 1 MHz, Z_{OUT} = 50Ω.

Absolute Maximum Ratings

	Operating	Programming
Supply Voltage, V_{CC}	7V	12V
Input Voltage	5.5V	12V
Off-State Output Voltage	5.5V	12V
Storage Temperature Range	−65°C to +150°C	

10H8A, 12H6A, 14H4A, 16H2A, 16C1A, 10L8A, 12L6A, 14L4A, 16L2A

Recommended Operating Conditions

Symbol	Parameter	Military			Commercial			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High Level Output Current			−2			−3.2	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Operating Free-Air Temperature				0		75	°C

Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_I = −18mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min., V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = Max.	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min., V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = Max.			0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max., V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max., V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max., V_I = 0.4V			−0.25	μA
I_{OS}	Short Circuit Output Current	V_{CC} = 5V	−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max.	55		90	mA

Switching Characteristics Over Recommended Ranges of Temperature and V_{CC}

Military: T_A = −55°C to +125°C, V_{CC} = 5V ±10%
Commercial: T_A = 0 to 75°C, V_{CC} = 5V ±5%

Symbol	Parameter	Test Conditions	Military			Commercial			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD}	From any Input to any Output	C_L = 15pF		15	30		15	25	ns

16L8A, 16R8A, 16R6A, 16R4A, 16X4A, 16A4A

Recommended Operating Conditions

Symbol	Parameter		Military			Commercial			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of Clock	Low	20	10		15	10		ns
		High	20	10		15	10		
t_{su}	Setup Time from Input or Feedback to Clock	16R8A, 16R6A, 16R4A	30	16		25	16		ns
t_h	Hold Time		0	−10		0	−10		ns
T_A	Operating Free-Air Temperature		−55			0	25	75	°C
T_C	Operating Case Temperature				125				°C

Electrical Characteristics Over Recommended Operating Temperature Range

Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage						0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min., I_I = −18mA				−0.8	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min., V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2mA	MIL	2.4	2.8		V
			I_{OH} = −3.2mA	COM				
V_{OL}	Low Level Output Voltage	V_{CC} = Min., V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 12mA	MIL		0.3	0.5	V
			I_{OL} = 24mA***	COM				
I_{OZH}	Off-state Output Current	V_{CC} = Max., V_{IL} = 0.8V, V_{IH} = 2V	V_O = 2.4V				100	µA
I_{OZL}			V_O = 0.4V				−100	µA
I_I	Maximum Input Current	V_{CC} = Max., V_I = 5.5V					1	mA
I_{IH}	High Level Input Current	V_{CC} = Max., V_I = 2.4V					25	µA
I_{IL}	Low Level Input Current	V_{CC} = Max., V_I = 0.4V				−0.02	−0.25	mA
I_{OS}	Output Short-Circuit Current**	V_{CC} = 5V	V_O = 0V		−30	−70	−130	mA
I_{CC}	Supply Current †	V_{CC} = Max.				120	180	mA

Switching Characteristics Over Recommended Ranges of Temperature and V_{CC}

Military: T_A = −55°C to +125°C*, V_{CC} = 5V ±10%
Commercial: T_A = 0 to 75°C, V_{CC} = 5V ±5%

Symbol	Parameter	Test Conditions†† R1, R2	Military			Commercial			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD}	Input or Feedback to Output	CL = 50pF		15	30		15	25	ns
t_{CLK}	Clock to Output or Feedback			10	20		10	15	ns
t_{PZX}	Pin 11 to Output Enable			10	25		10	20	ns
t_{PXZ}	Pin 11 to Output Disable	C_L = 5pF		11	25		11	20	ns
t_{PZX}	Input to Output Enable	C_L = 50pF		10	30		10	25	ns
t_{PXZ}	Input to Output Disable	C_L = 5pF		13	30		13	25	ns
f_{MAX}	Maximum Frequency		20	30		25	30		ns

† I_{CC} = Max. at minimum temperature.
††See Waveforms, Test Load on pg. 24-21.

Table 2-2. $T_A = 25°C$

Symbol	Parameter		Limits Min	Typ	Max	Units
V_{IHH}	Program-level input voltage		11.5	11.75	12.0	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD,L/R			25	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	μs
t_d	Delay time		100			ns
	Program Pulse duty cycle				25	%
V_P	Program/Verify-Protect-input voltage $5.5V \leq V_{CC} \leq 6V$		18	18.5	19	V
I_P	Program/Verify-Protect-input current				400	mA
t_{dv}	Delay Time to Verify		100			μs

Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all 15 PAL types. The array is divided into two groups, products 0 through 31 and products 32 through 63, for which pin identifications are shown in Figure 2-2. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

1. Raise Output Disable, OD, to V_{IHH}.
2. Select an input line by specifying I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, and L/R as shown in Table 12.
3. Select a product line by specifying A_0, A_1, and A_2 one-of-eight select as shown in Table 2-10.
4. Raise V_{CC} (pin 20) to V_{IHH}.
5. Program the fuse by pulsing the output pins O_n of the selected product group to V_{PH} as shown in Table 2-4.
6. Lower V_{CC} (pin 20) to 6.0 V.
7. Pulse the CLOCK pin and verify output pins O_n to be Low for active Low PAL types or High for active High PAL types.
8. Lower V_{CC}(pin 20) to 4.5 V and repeat step 7.
9. Should the output not verify, repeat steps 1 through 8 up to five (5) times.

Repeat this procedure for all fuses to be blown. (See Figure 2-3.)

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to 18.5 volts for 10 ms-1 sec. with V_{CC} at 6.0 volts.

Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = 10 k Ohms to 5.0 V.

Table 2-3. Input Line Select

Input Line Number	Pin Identification								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	R
25	HH	H	HH	HH	HH	HH	HH	HH	R
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	Z
29	H	HH	HH	HH	HH	HH	HH	HH	Z
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

Table 2-4. Product Line Select

Product Line Number	Pin Identification						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0,32	Z	Z	Z	HH	Z	Z	Z
1,33	Z	Z	Z	HH	Z	Z	HH
2,34	Z	Z	Z	HH	Z	HH	Z
3,35	Z	Z	Z	HH	Z	HH	HH
4,36	Z	Z	Z	HH	HH	Z	Z
5,37	Z	Z	Z	HH	HH	Z	HH
6,38	Z	Z	Z	HH	HH	HH	Z
7,39	Z	Z	Z	HH	HH	HH	HH
8,40	Z	Z	HH	Z	Z	Z	Z
9,41	Z	Z	HH	Z	Z	Z	HH
10,42	Z	Z	HH	Z	Z	HH	Z
11,43	Z	Z	HH	Z	Z	HH	HH
12,44	Z	Z	HH	Z	HH	Z	Z
13,45	Z	Z	HH	Z	HH	Z	HH
14,46	Z	Z	HH	Z	HH	HH	Z
15,47	Z	Z	HH	Z	HH	HH	HH
16,48	Z	HH	Z	Z	Z	Z	Z
17,49	Z	HH	Z	Z	Z	Z	HH
18,50	Z	HH	Z	Z	Z	HH	Z
19,51	Z	HH	Z	Z	Z	HH	HH
20,52	Z	HH	Z	Z	HH	Z	Z
21,53	Z	HH	Z	Z	HH	Z	HH
22,54	Z	HH	Z	Z	HH	HH	Z
23,55	Z	HH	Z	Z	HH	HH	HH
24,56	HH	Z	Z	Z	Z	Z	Z
25,57	HH	Z	Z	Z	Z	Z	HH
26,58	HH	Z	Z	Z	Z	HH	Z
27,59	HH	Z	Z	Z	Z	HH	HH
28,60	HH	Z	Z	Z	HH	Z	Z
29,61	HH	Z	Z	Z	HH	Z	HH
30,62	HH	Z	Z	Z	HH	HH	Z
31,63	HH	Z	Z	Z	HH	HH	HH

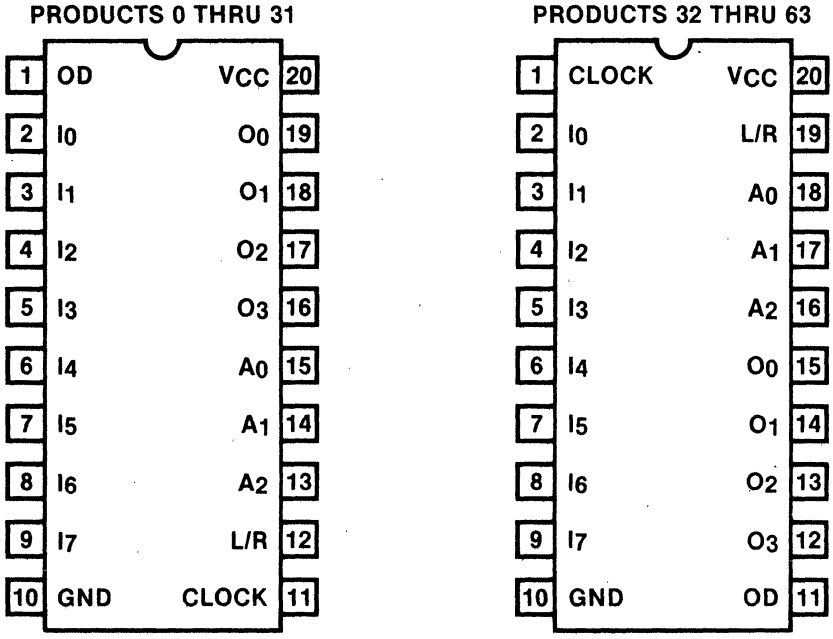


FIGURE 2-2. Pin Identification

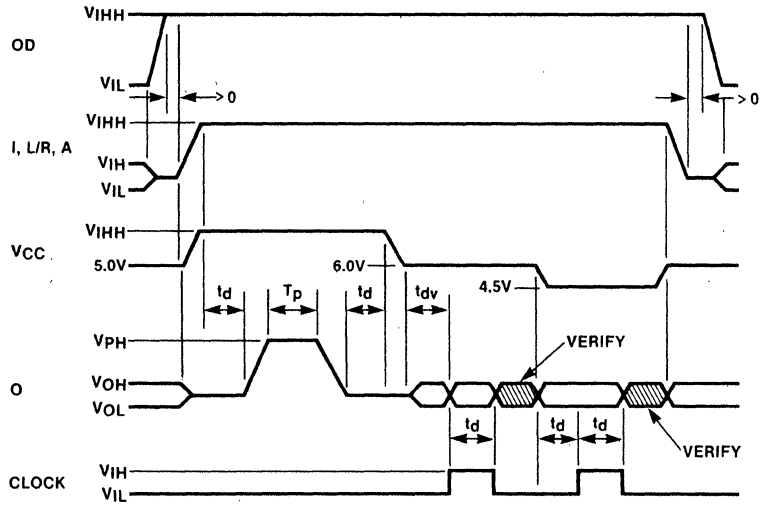


FIGURE 2-3. Programming Waveforms

Programmable Array Logic Series 24

General Description

The PAL® Series 24 family compliments the PAL Series 20 family by providing two additional inputs and two additional outputs, allowing more complex functions in a single package. This new family is made feasible by the new 300 Mil-wide, 24-pin package.

In addition to providing more logic functions per chip, 24 pins allow for many natural functions which were previously unavailable in 20-pin packages. Examples include:

- 8-bit parallel-in parallel-out counters
- 8-bit parallel-in parallel-out shift registers
- 16-Line-to-1-Line Multiplexers
- Dual 8-Line-to-1-Line Multiplexers
- Quad 4-Line-to-1-Line Multiplexers

These natural functions provide twice the density of traditional 16-pin packages.

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production. This often simplifies not only the PC board layout, but also the board itself.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality cards and socket adapters. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Features

- Programmable replacement for conventional TTL logic.
- Reduces IC inventories substantially and simplifies their control.
- Reduces chip count by 5 to 1, typically.
- Expedites and simplifies prototyping and board layout.
- Saves space with 300 Mil-wide, 24-pin DIP packages.
- Programmed on standard PROM programmers.
- Programmable three-state outputs.
- Last fuse reduces possibility of copying by competitors.

PAL is a registered trademark of and used under license with Monolithic Memories, Inc.

Table 2-5. Part Types

Part Number	Description
DMPAL12L10	DECA 12 Input AND-OR-INVERT Gate Array
DMPAL14L8	OCTAL 14 Input AND-OR-INVERT Gate Array
DMPAL16L6	HEX 16 Input AND-OR-INVERT Gate Array
DMPAL18L4	QUAD 18 input AND-OR-INVERT Gate Array
DMPAL20L10	DECA 20 Input AND-OR-Invert Gate Array
DMPAL20X10	DECA 20 Input Registered AND-OR-XOR Gate Array
DMPAL20X8	OCTAL 20 Input Registered AND-OR-XOR Gate Array
DMPAL20X4	QUAD 20 Input Registered AND-OR-XOR Gate Array
DMPAL20L2	DUAL 20 Input AND-OR-INVERT Array
DMPAL20C1	SINGLE 20 Input AND-OR-INVERT Array

Absolute Maximum Ratings

	Operating	Programming
Supply Voltage, V_{CC}	7V	12V
Input Voltage	5.5V	12V*
Off-state Output Voltage	5.5V	12V
Storage Temperature		−65°C to +150°C

Operating Conditions

Symbol	Parameter	Military			Commercial			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-air Temperature				0		75	°C
T_C	Operating Case Temperature	−55		125				°C

Electrical Characteristics Over Operating Conditions

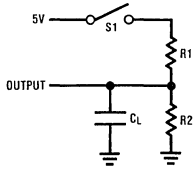
Symbol	Parameter	Test Conditions			Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage						0.8	V
V_{IH}	High Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min.	I_I = −18mA				−1.5	V
I_{IL}	Low Level Input Current †	V_{CC} = Max.	V_I = 0.4V				−0.25	mA
I_{IH}	High Level Input Current †	V_{CC} = Max.	V_I = 2.4V				25	μA
I_I	Maximum Input Current	V_{CC} = Max.	V_I = 5.5V				1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min. V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 12 mA	MIL			0.5	V
			I_{OL} = 24 mA	COM				
V_{OH}	High Level Output Voltage	V_{CC} = Min. V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −2 mA	MIL	2.4			V
			I_{OH} = −3.2mA	COM				
I_{OZL}	Off-state Output Current †	V_{CC} = Max. V_{IL} = 0.8V V_{IH} = 2V	V_O = 0.4V				−100	μA
I_{OZH}			V_O = 2.4V				100	μA
I_{OS}	Output Short-Circuit Current**	V_{CC} = Max.	V_O = 0V		−30		−130	mA
I_{CC}	Supply Current	V_{CC} = Max.	20X4, 20X8, 20X10			120	180	mA
			20L10			90	165	

† I/O pin leakage is the worst case of I_{OZX} or I_{IX}, e.g. I_{IL} and I_{OZH}.
* Pins 1 and 13 may be raised to 22V max.
** Only one output shorted at a time.

Switching Characteristics Over Operating Conditions

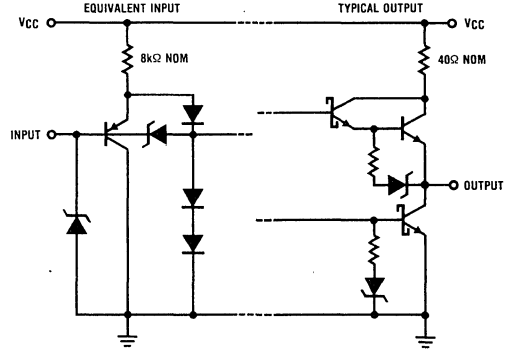
Symbol	Parameter		Test Conditions R1, R2	Military			Commercial			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PD}	Input or Feedback to Output		20L10, 20X10 20X8, 20X4 $C_L = 50$ pF		35	60		35	50	ns
t_{PD}	Input or Feedback to Output		12L10, 14L8, 16L6 18L4, 20L2, 20C1 $C_L = 50$ pF		25	45		25	40	ns
t_{CLK}	Clock to Output or Feedback		$C_L = 50$ pF		20	40		20	30	ns
t_{PZX}	Pin 13 to Output Enable		$C_L = 50$ pF		20	45		20	35	ns
t_{PXZ}	Pin 13 to Output Disable		$C_L = 5$ pF		20	45		20	35	ns
t_{PZX}	Input to Output Enable		$C_L = 50$ pF		35	55		35	45	ns
t_{PXZ}	Input to Output Disable		$C_L = 5$ pF		35	55		35	45	ns
t_W	Width of Clock	Low		30			25			ns
		High		40			35			ns
t_{SU}	Set-Up Time from Input or Feedback			60			50			ns
t_h	Hold Time			0	– 15		0	– 15		ns
f_{MAX}	Maximum Frequency			10.0			12.5			MHz

Test Load



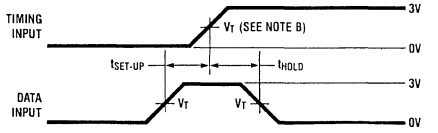
MIL	COM'L
R1 = 390	R1 = 200
R2 = 750	R2 = 390

Schematic of Inputs and Outputs

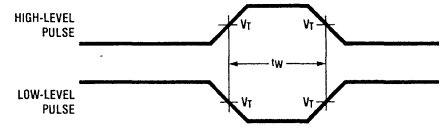


Test Waveforms

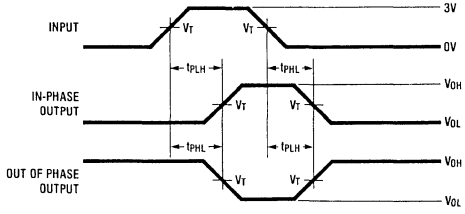
Set-Up and Hold



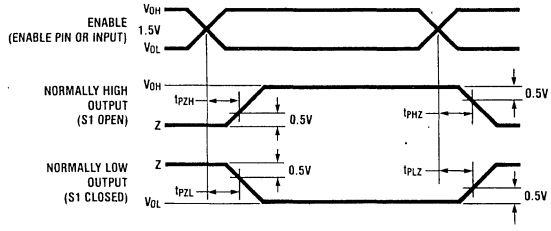
Pulse Width



Propagation Delay



Enable and Disable



Note A: C_L includes probe and jig capacitance.

Note B: $V_T = 1.5$V.

Note C: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Note D: All input pulses are supplied by generators having the following characteristics: PRR = 1 MHz, $Z_{OUT} = 50\Omega$.

Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all PAL types. The array is divided into two groups, products 0 thru 39 and products 40 thru 79, for which pin identifications are shown in Pin Configurations below. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Disable, OD, to V_{IHH}.

Step 2 Select an input line by specifying I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7, I_8, I_9 and L/R as shown in Table 2-6.

Step 3 Select a product line by specifying A_0 and A_1 one-of-four select as shown in Table 2-7.

Step 4 Raise V_{CC} (pin 24) to V_{IHH}.

Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to V_{IHH} as shown in Programming Waveform.

Step 6 Lower V_{CC} (pin 24) to 6.0 V.

Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.

Step 8 Lower V_{CC} (pin 24) to 4.5 V and repeat Step 7.

Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see Programming Waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 13 to 18.5 volts with V_{CC} at 6.0 volts.

Voltage Legend

L = Low Level Input Voltage, V_{IL}
H = High Level Input Voltage, V_{IH}
HH = High Level Program Voltage, V_{IHH}
Z = High Impedance (e.g. 10k Ω to 5.0V)

Table 2-6. Input Line Select

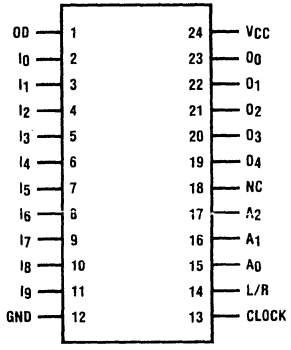
Input Line Number	Pin Identification										
	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	Z
1	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	Z
2	HH	HH	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	Z
5	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	Z
6	HH	HH	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	Z
9	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	Z
10	HH	HH	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	Z
13	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	Z
14	HH	HH	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	Z
17	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	Z
18	HH	HH	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	Z
21	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	Z
22	HH	HH	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	Z
25	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	Z
26	HH	HH	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	HH	HH	H	HH	HH	HH	HH	HH	HH	HH
28	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	Z
29	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	Z
30	HH	HH	L	HH	HH	HH	HH	HH	HH	HH	HH
31	HH	HH	H	HH	HH	HH	HH	HH	HH	HH	HH
32	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	Z
33	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	Z
34	HH	L	HH	HH	HH	HH	HH	HH	HH	HH	HH
35	HH	H	HH	HH	HH	HH	HH	HH	HH	HH	HH
36	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
37	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	Z
38	L	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH
39	H	HH	HH	HH	HH	HH	HH	HH	HH	HH	HH

Table 2-7. Product Line Select

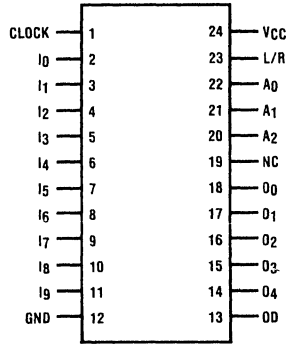
Product Line Number	Pin Identification							
	O_4	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 40	Z	Z	Z	Z	HH	Z	Z	Z
1, 41	Z	Z	Z	Z	HH	Z	Z	HH
2, 42	Z	Z	Z	Z	HH	Z	HH	Z
3, 43	Z	Z	Z	Z	HH	Z	HH	HH
8, 48	Z	Z	Z	HH	Z	Z	Z	Z
9, 49	Z	Z	Z	HH	Z	Z	Z	HH
10, 50	Z	Z	Z	HH	Z	Z	HH	Z
11, 51	Z	Z	Z	HH	Z	Z	HH	HH
16, 56	Z	Z	HH	Z	Z	Z	Z	Z
17, 57	Z	Z	HH	Z	Z	Z	Z	HH
18, 58	Z	Z	HH	Z	Z	Z	HH	Z
19, 59	Z	Z	HH	Z	Z	Z	HH	HH
24, 64	Z	HH	Z	Z	Z	Z	Z	Z
25, 65	Z	HH	Z	Z	Z	Z	Z	HH
26, 66	Z	HH	Z	Z	Z	Z	HH	Z
27, 67	Z	HH	Z	Z	Z	Z	HH	HH
32, 72	HH	Z	Z	Z	Z	Z	Z	Z
33, 73	HH	Z	Z	Z	Z	Z	Z	HH
34, 74	HH	Z	Z	Z	Z	Z	HH	Z
35, 75	HH	Z	Z	Z	Z	Z	HH	HH
36, 76	HH	Z	Z	Z	Z	HH	Z	Z
37, 77	HH	Z	Z	Z	Z	HH	Z	HH
38, 78	HH	Z	Z	Z	Z	HH	HH	Z
39, 79	HH	Z	Z	Z	Z	HH	HH	HH

Pin Configurations

PRODUCTS 0 THRU 39



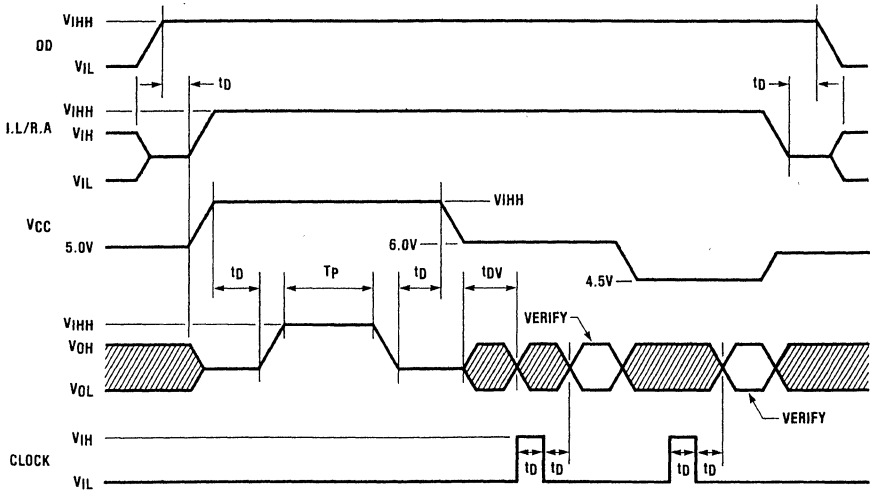
PRODUCTS 40 THRU 79



Programming Parameters $T_A = 25°C$

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{IHH}	Program-level Input Voltage		11.5	11.75	12.0	V
I_{IHH}	Program-level Input Current	Output Program Pulse			50	mA
		OD, L/R			50	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	μs
t_D	Delay Time		100			ns
t_{DV}	Delay Time to Verify		100			μs
	Program Pulse Duty Cycle				25	%
V_P	Verify-Protect Input Voltage $5.5V \leq V_{CC} \leq 6.0V$		18	18.5	19	V
I_P	Verify-Protect Input Current				400	mA
T_{PP}	Verify-Protect Pulse Width		20		50	ms

Programming Waveforms



National Semiconductor

PAL Design

Selecting the Right PAL

PAL part types come in small, medium, and large sizes, offering a wide range of complexities. The small PALs are also referred to as combinational because they just do logic functions. Four of these small PALs have active-high outputs (the "H" series), and four have active-low outputs (the "L" series), with a variety of input/output pin ratios. The one small PAL left over is the 16C1, which has complementary outputs. The small PAL types can replace random SSI gate functions at about a 4-to-1 chip-count reduction. This group is designed to provide low-power Schottky (LS) fan-out and fan-in characteristics of 8 mA output sink (I_{OL}) for totem-pole outputs and 0.25 mA input loading (I_{IL}).

The simplest medium PAL, the 16L8, is logically the same as the 10L8, with six added inputs that are shared with output pins. The 16 in its type number thus refers to the number of input variables to its AND matrix. Its unique logic is shown in Figure 3-2. Its TRI-STATE® outputs are controlled by lines from the AND matrix, so can be acted upon by input variables. These pins therefore serve as I/O in a bus-oriented environment.

Other medium PALs are the R (Register) devices. Figure 3-3 is a simplified diagram showing the logic embodied in the R series. The unique feature of the Register PAL is the D-type register element following each OR gate. A common clock input latches data into all register elements simultaneously on the rising edge of the clock pulse. The register outputs are connected to TRI-STATE buffers, controlled by a common enable input.

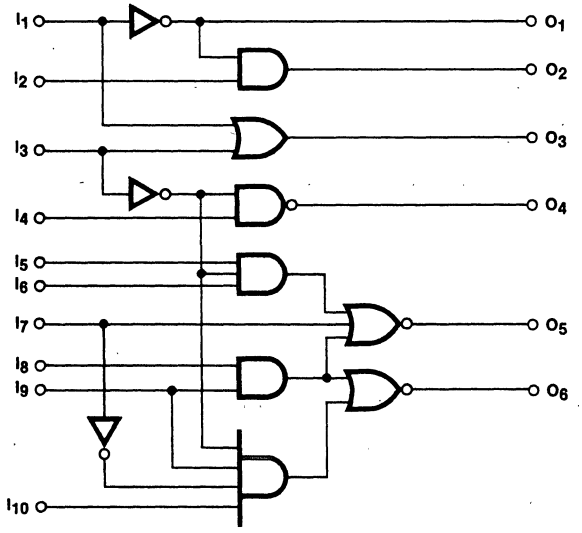


FIGURE 3-1. Typical Combinational Logic Application.

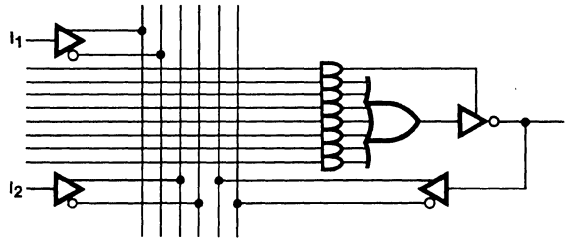


FIGURE 3-2. Simplified Logic Diagram of the 16L8 PAL®

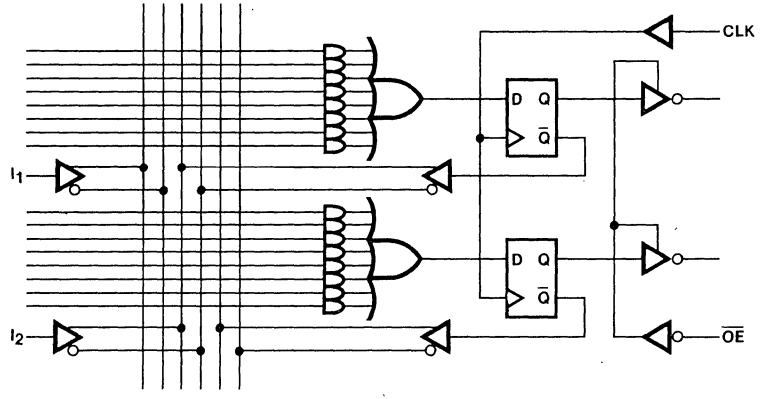


FIGURE 3-3. Logic of the R Series PAL®

A significant feature of the register PALs is the register feedback path to the AND matrix. This feedback path allows the PALs to be used in state-machine applications in which the feedback loops are all on-chip. These devices are especially useful in the design of custom registers, shifters, and counters.

The three register PALs are the 16R8, 16R6, and 16R4, which have eight, six, and four register elements, respectively. Each has eight outputs; those not serving the register elements are of the I/O variety, like those on the 16L8, above. Their outputs are bus drivers that will deliver the standard LS output sink of 24 mA (I_{OL}).

Two members of the PAL family (16x4 and 16A4) are referred to as large PALs. These two devices facilitate the arithmetic functions, add, subtract, greater than, and less than, by means of the two additional features shown in Figure 3-4. The sum of the products (OR outputs) is segmented into two, which are then XOR'd to the D flip-flop input. This allows carries from previous operations to be XOR'd with the two variable sums generated by the AND array.

A second feature is the gating of the register feedback path and inputs, forming the terms I + Q, I + /Q, /I + Q, and /I + /Q. This provides versatile operations on two variables and facilitates the parallel generation of carries. These two parts also have bus-driver outputs. You can expect "compression ratios" (package count reductions) of up to 12:1 by comparison with existing combinations of MSI and discretes. You can also invent new and unique LSI functions with these parts, and implement them without having to spend huge sums on masks or tooling.

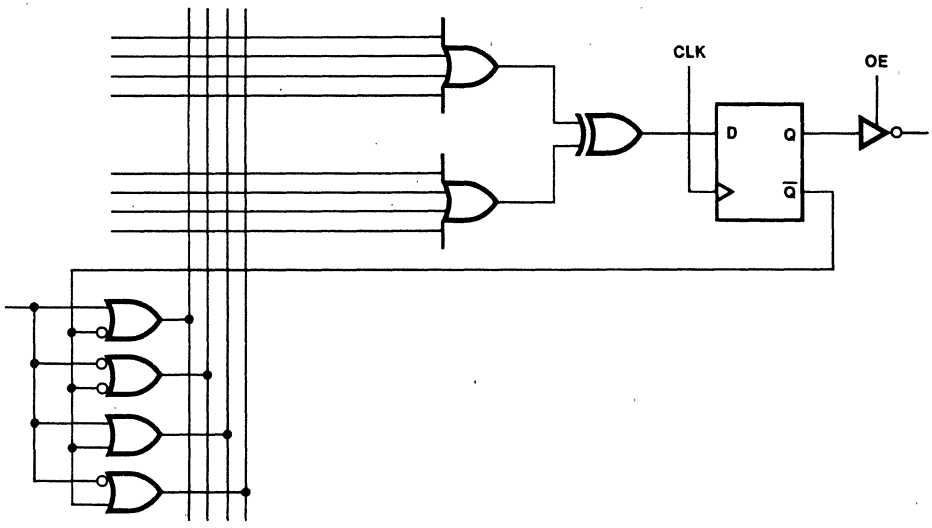


FIGURE 3-4. Logic of the Large PAL®

Designing the PAL Once a particular PAL device is selected, it is time to generate the PAL design. This can be done either manually or through the use of a software tool called PALASM™, described on page 24-41.

The coding conventions adopted to describe PAL programming are described in Figure 3-20. The arbitrary circuit of Figure 3-21 is used as a design example for selecting and coding a PAL. Since no registers are called for, the device to implement this function may be selected from among the H, L, and C types. Since the lower part of the diagram displays AND-OR-INVERT functions, the L series is most likely.

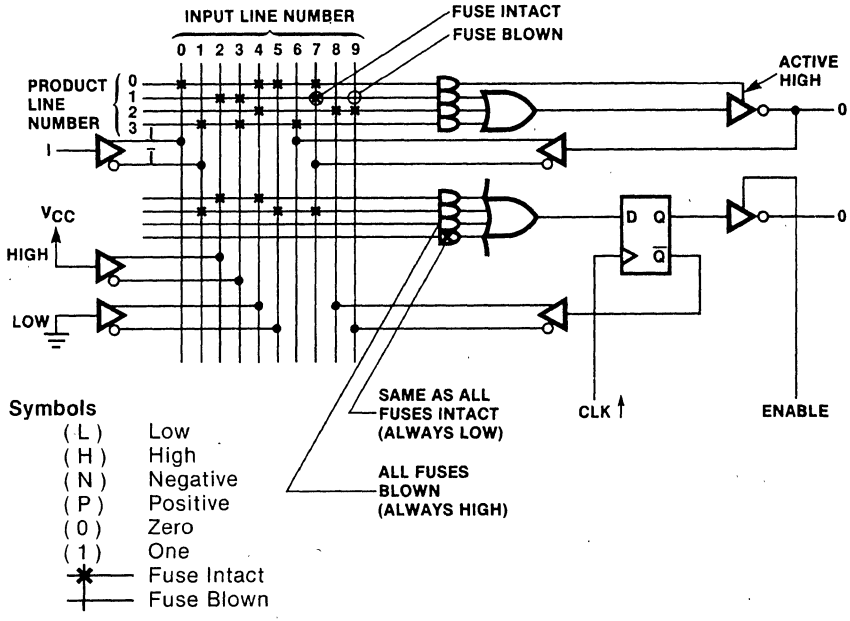


FIGURE 3-20. Coding Conventions.

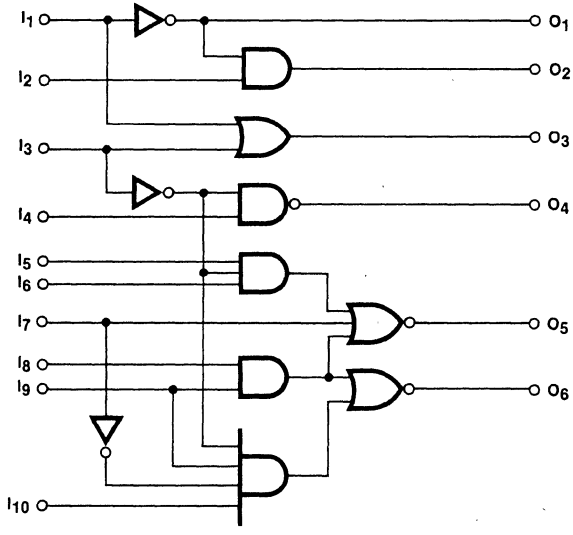


FIGURE 3-21. Design Example, Logic Diagram.

The next step: the number of inputs (10) and the number of outputs (6) indicates that a 10L8, 12L6, or 16LB could accommodate the entire circuit. Since the 10L8 and 12L6 are "small" PALs and hence less costly than the 16L8 "medium" device, the choice should be made between these two if possible. A review of the 10L8's logic diagram shows that all of its NOR gates are two-input gates, and the design example requires a three-input gate. On the other hand, the 12L6 has two 4-input gates which will accommodate the three-input requirement. It, therefore, is selected. Having chosen an inverting type of PAL, you apply DeMorgan's theorem to handle the inversion at the NOR gates feeding all of its outputs. Demorgan's theorem can be used to convert any logic form to the AND-OR/AND-NOR PAL format. This has been done in the equations below; the PAL AND-NOR format shown on the right.

$$O_1 = /I_1 \quad \cong \quad /O_1 = I_1 \ (1)$$

$$O_2 = /I_1 \bullet I_2 \quad \cong \quad /O_2 = I_1 + /I_2 \ (2)$$

$$O_3 = I_1 + I_3 \quad \cong \quad /O_3 = /I_1 \bullet /I_3 \ (3)$$

$$O_4 = /(/I_3 \bullet I_4) \quad \cong \quad /O_4 = /I_3 \bullet I_4 \ (4)$$

$$O_5 = /(/I_3 \bullet I_5 \bullet I_6 + I_7 + I_8 \bullet I_9)$$

$$\cong$$

$$/O_5 = /I_3 \bullet I_5 \bullet I_6 + I_7 + I_8 \bullet I_9 \ (5)$$

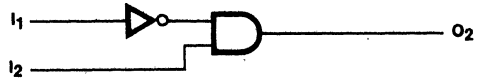
$$O_6 = /(I_8 \bullet I_a + /I_3 \bullet /I_7 \bullet I_9 \bullet I_{10})$$

$$\cong$$

$$/O_6 = I_8 \bullet I_9 + /I_3 \bullet /I_7 \bullet I_9 \bullet I_{10} \ (6)$$

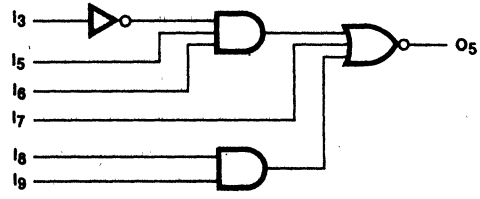
Assuming that there are no board layout constraints, input I_1 through I_{10} may be assigned to pins 1 through 11. (Pin 10 is ground.) The only constraint on output pin assignment is that O_5 must be assigned to pin 13 or 18 to take advantage of one of the 4-input NOR gates.

O_1 is assigned to pin 18. To make this output the inverse of I_1, leave input line 2 connected (not blown) to product line 8 and blow all the remaining fuses on that product line. This is indicated by the X on the intersection of input line 2 and product line 8 in Figure 3-24.



$$O_2 = \overline{I_1} \cdot I_2$$

FIGURE 3-22. The Logic Diagram and Expression for Output 2.



$$O_5 = \overline{I_3 I_5 I_6 + I_7 + I_8 I_9}$$

FIGURE 3-23. The Logic Diagram and Expression for Output 5.

As the other three inputs to NOR gate 1 are not used, they are forced to zero by leaving all fuses intact on product lines 9,10, and 11. (As shown in Figure 3-20, instead of confusing the diagram with many Xs, the unused inputs are indicated by Xs in the small AND symbols at the NOR gate inputs.)

The next output, O_2, is the AND function of $/I_1$ and I_2 (Figure 3-22). In the L series, the AND gates cannot be brought to outputs without inversion, but by DeMorgan's theorem, the equivalent function can be constructed by taking the complements of the two inputs, ORing them, and inverting the result. Equation (2), on Page 24-36 shows the form that can be coded directly into the 12L6. The coding of this expression, using pin 1 and the complement of pin 2 as inputs 1 and 2, respectively, and pin 17 as output 2, is marked with Xs on product lines 1 and 2 in Figure 3-24.

Output O_3 is the OR of I_1 and I_3. Again, the output inversion of the L series suggests the double-inversion application of DeMorgan's theorem, as shown in Equation (3). To do this, connect input lines 3 (I_1) and 5 (I_3) to product line 24. Since no other input is needed to NOR gate 3, its other input is forced low by leaving all its fuses intact. The X at the unused gate input shows this on the diagram.

Output O_4 is the NAND function of $/I_3$ and I_4. This is accomplished by ANDing input line 5 ($/I_3$) and input line 8 (I_4) on product line 32, which produces $/(/I_3 \bullet I_4)$ at the output of NOR gate 4, with its unused input tied to 0 (all fuses intact).

Output O_5 is generated by ANDing $/I_3$, I_5, and I_6 on product line 48, ANDing I_8 and I_9 on line 50, connecting I_7 to product line 49, and leaving unused line 51 grounded. (See Figures 3-23 and 3-24.)

Output O_6 is generated by ANDing I_8 and I_9 on product line 40 and $/I_3$, $/I_7$, I_9, and I_{10} on product line 41, which, inverted by NOR gate 5, results in $/O_6$. [See Equation (6).]

The coding for a completed PAL design must be transformed into a format more readily interpreted for execution on commercially available PROM programming devices. A form for doing this is shown in Figure 3-25. The numbers along the top of the figure correspond with the input line numbers that appear across the top of the logic diagram (Figure 3-24). The product term line numbers along the left side of these two illustrations correspond also.

Note that some of the boxes in Figure 3-25 are filled in with Gothic L's. These represent phantom fuses, which are fuse locations not accessible in the given device type but which must be accounted for to provide the programmer with the proper data for verification. For the present, these entries can be ignored. To fill in the remaining boxes, begin with the first X marked on the logic diagram, Figure 3-24. It is located at the intersection of input line 2 and product term 8. Since this is an intact fuse, an L (for Low) is entered in the corresponding box of Figure 3-25, as detailed below.

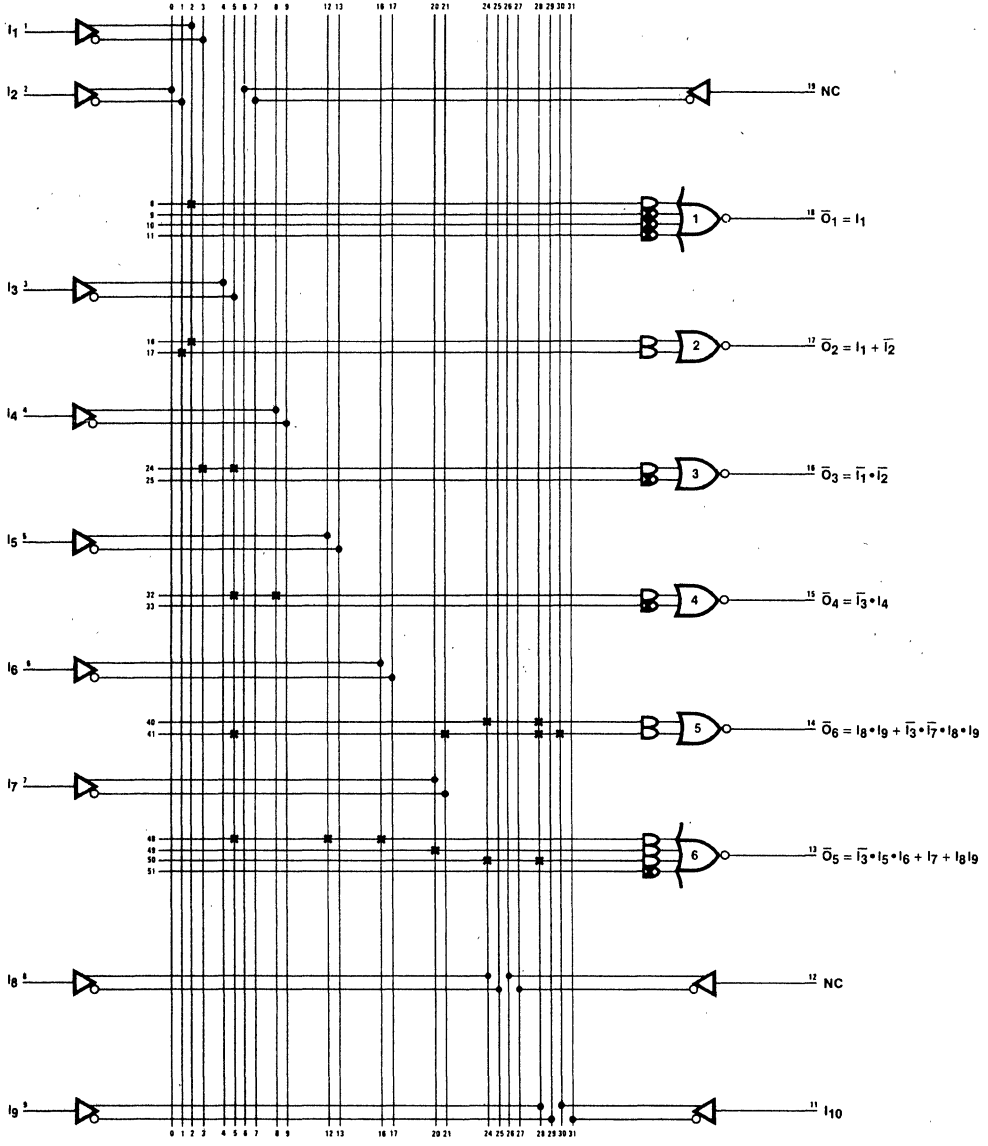
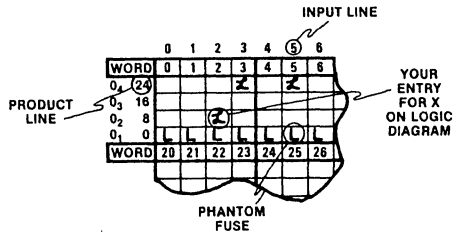
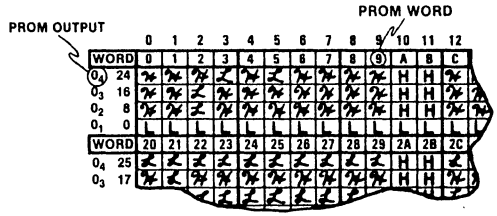


FIGURE 3-24. Logic Diagram of the National Type 12L6 PAL®





NOTE

Script L's (ℒ) are used to differentiate entries being programmed and entries already on the form. In practice, this is not necessary.

Next L's are entered in all of the blank spaces for product term 9 on the form (Fig. 3-25), since this is an unused line, as indicated by the X at the input to the NOR gate for this product term on the logic diagram. Similarly, complete lines of L's are entered for product terms 10 and 11. Every X on the logic diagram must be entered on the PAL programming form as an L or, in the case of the unused gate inputs, as a row of L's. Figure 3-25 is shown with all the necessary L's filled in.

Since all of the remaining fuses are to be blown, H's must be written into the remaining blanks. For clarity, this is not done in Figure 3-25, but a portion of the completed programming format is shown below.

Once the programming format is complete, the input line and product term numbers can be forgotten. What the format sheet does is translate these into their equivalent hexadecimal input words and outputs, in the form acceptable by a device that programs 512 x 4 PROMs. Thus, to program the example currently under discussion, insert the 12L6 PAL into the socket of a suitably configured programmer and enter the following:

Word No.	Output O_4 O_3 O_2 O_1
0	H H H L
1	H H H L
2	H L L L
3	L H H L
4	H H H L
5	L H H L
6	H H H L
•	•
•	•
•	•
1F	H H H L
20	L H L L
21	L L L L
22	L H L L
•	•
•	•
•	•
1FF	L L L L

After the PAL is programmed and verified, it must be tested logically in the PAL mode to eliminate defects which cannot be tested at the factory prior to programming.

Programming Format PAL 12L6

PATTERN: NAME:

PRODUCT TERMS (0-63)

DATE:

INPUTS (0-31)

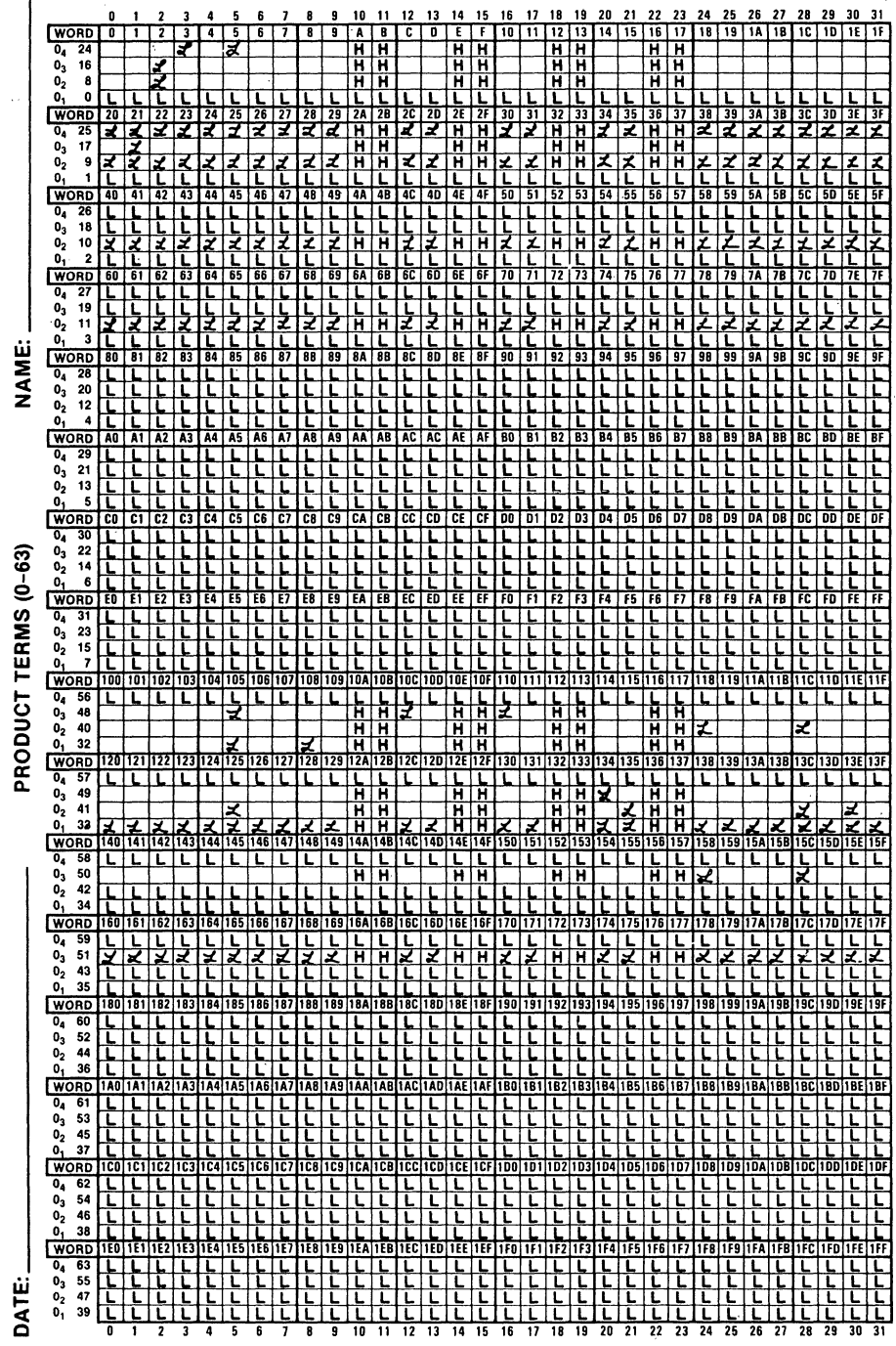


FIGURE 3-25. Programming Format Sheet for National Type 12L6 PAL.™

Executing this sequence programs a Type 12L6 PAL to implement the logic function shown in Figure 3-21. Programming format sheets and logic diagrams that show all fuse locations for all 15 of the PAL devices are shown later in this section.

Phantom Fuses

Phantom fuse locations are those locations where a fuse does not exist. These are revealed as missing outputs, missing product terms, or missing input lines in the logic diagrams, Figures 3-5 through 3-19. PALs with phantom fuse locations appear the same to the programming device as partially programmed 512 x 4 PROMs. As the programmer expects to verify all 2048 locations, the PAL programming format must provide the expected pattern for verifying nonexistent fuse nodes. When filling out the programming format, refer to Figure 3-26, the key to phantom fuse locations in the complete logic schematics that follow.

PALASM ™

Manual PAL coding, while practical for one or two designs, is far too tedious and error-prone for continual use. What is needed is a computer-aided design technique that automates the design process to the highest degree possible. One such design aid is a FORTRAN-IV-based software package called PALASM. This design aid allows PALs to be designed by writing logic equations to represent the desired logic function. The output of PALASM is a programming tape that can be used as a data input by most PROM programmers that have PAL personality cards. Its output format can be BHLF, BPNF, or Hexadecimal.

The simplest way to describe PALASM is with a design example. The same arbitrary sample function that is described on the previous pages is "designed" using PALASM in the discussion that follows. The logic diagram is shown in Figure 3-21. Figure 3-27 shows the logic operators recognized by the assembler. Figure 3-28 is the input to PALASM that is compiled by the program and generates the code for the programming device.

=	Equal
:=	Replaced by, following clock
/	Complement
★	AND, PRODUCT
+	OR, SUM
:+:	XOR
:★:	XNOR
( )	Conditional TRI-STATE IF statement, arithmetic

FIGURE 3-27. PALASM Operators

	Active High Logic		Active Low Logic	
	(PAL 10H8, 12H6, 14H4, 16H2)	LEGEND	(PAL 10L8, 12L6, 14L4, 16L2)	LEGEND
1) Missing Output	H (P,1)	⊡	L (N,O)	⊙
2) Missing product	L (N,O)	⊙	L (N,O)	⊙
3) Missing input lines	H (P,1)	⊡	H (P,1)	⊡

Note 1: Missing product term overrides missing input line.

Note 2: For PAL 16C1, first half of the array (product terms 0-31) acts as active high logic and the second half of the array (product terms 32-63) acts as active low logic device.

FIGURE 3-26. PAL Phantom Fuse Symbology.

The PALASM program is instructed to generate code with which to program the 12L6 by keying the sequence shown in Figure 3-28 into its host computer as follows:

Line 1: At the left margin, the PAL device is specified. For this example, the 12L6 remains the best solution. "PAL DESIGN SPECIFICATION" is entered at the right.

Line 2: A unique pattern number for this PAL design is entered at the left margin on line 2, followed by designer's name and date.

Line 3: The name or description of the device or function is entered. If this runs over one line, Line 4 may be used to complete it.

Line 4: If not used to complete line 3, this line is skipped.

Line 5, 6, and 7: These lines are used for pin assignments. All 20 of the pins on the PAL are assigned symbolic names, usually corresponding to the symbols used on the logic diagram. (Note that GND and V_{CC} must be included.) Assignment starts at pin 1 and proceeds sequentially, through pin 20. (See Figure 3-24 for sample pinouts.)

Line 8: Beginning on line 8, the logic equations that describe the required functions are written using the symbols defined in lines 5, 6, and 7, in the format applicable to the PAL selected. For example, the output of the 12L6 is low for the selected product term; therefore, the logic equations must be of the form $/0_X = f(I_1, I_2,...)$. The symbology used must be that shown in Figure 3-27.

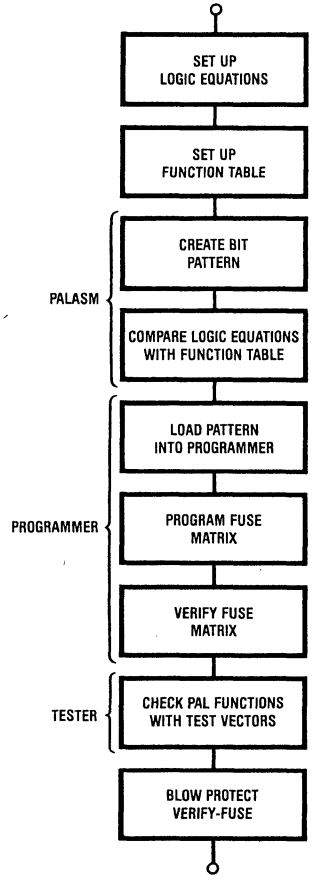
Line 1	PAL 12L6	PAL Design Specification
Line 2	PAT 1476	Bob Jones 5/10/81
Line 3	PAL Design Example	
Line 4		
Line 5	$I_1\ I_2\ I_3\ I_4\ I_5\ I_6\ I_7\ I_8\ I_9$ GND I_{10} NC O_5	
Line 6	$O_6\ O_4\ O_3 O_2\ O_1$ NC V_{CC}	
Line 7		
Line 8	$/O_1 = I_1$	
Line 9	$/O_2 = I_1 + /I_2$	
Line 10	$/O_3 = /I_1 * /I_3$	
Line 11	$/O_4 = /I_3 * I_4$	
Line 12	$/O_6 = I_8 * I_9 + /I_9 + I_3 * /I_7 * I_9 * I_{10}$	
Line 13	$/0_5 = /I_3 * I_5 * I_6 + I_7 + I_8 * I_9$	
Line 14		
Line 15	Description	
Line 16		
Line 17	This program is a design example describing	
Line 18	the use of PALASM as a PAL design aid.	

An additional design example using PALASM is shown on page 24-46. This is followed by the complete PALASM listing.

FIGURE 3-28. Example of PALASM (TM) Program Input

PAL Programming Procedure

The entire procedure for programming a PAL is shown in the block diagram below. The first step is to generate the logic equations and function table and then, using PALASM, to create bit pattern and compare logic equations with the function table. The third step is to load the bit pattern into a PAL programmer* to program and verify the fuse matrix. The fourth step is functionally testing the PAL with test vectors on a functional tester. The last step, blowing the protect verify fuse, is optional.



*See next page for details of PAL programmers.

PAL Programmers

Manufacturer	Basic Equipment	PAL-Modul	Adapters	PAL Design-Software Included	Performs Logic Simulation	Storage Media for Bit Pattern	Storage Media for Test Vectors	Programs 20-Pin	Programs 24-Pin	Blows Security Fuses
Data I/O	Model 17, 19, 29A or 100A	1427	1428-1 -2 -3	no	no	Master PAL	—	yes	no	no
Digelec	μP 803	FAM 51	20 + 24 pin socket	yes	no	Master PAL	—	yes	yes	yes
Kontron	EPP 80 or MPP 80S	MOD 21	SA 27 + SA 27 – 1	no	no	Master PAL	—	yes	yes	yes
Prolog	Progr. 910 or 980 or NSC Starplex™	PM9068	S 1 2 3	no	no	Master PAL	—	yes	no	yes
Stag	PPX	PM 202 + BRAL	AM10H8 • • • AM16C1	yes	no	Master PAL	—	yes	no	yes

All these systems program and verify the PALs in the PROM mode, they *do not perform a logic simulation* in the PAL mode 1. Additional (external) circuitry for logic simulation should be used if PALs go into volume production—otherwise a small percentage of the PALs will show failures when testing the complete PC board! OK for prototype-making.

PAL Development Systems

Manufacturer	Basic Equipment	PAL-Modul	Adapters	PAL Design-Software Included	Performs Logic Simulation	Storage Media for Bit Pattern	Storage Media for Test Vectors	Programs 20-Pin	Programs 24-Pin	Blows Security Fuses
Data I/O	Model 17, 19, 29A or 100 and any terminal	Logic-Pack	Design ad. and Progr. ad	yes	Yes, automatic or manual generation of test vectors	Master PAL	external	yes	yes	yes
Digelec	μP 803	FAM 52	20 and 24-pin adapter	yes	Yes, automatic or manual generation of test vectors	Master PAL	external	yes	yes	yes
Stag	—	ZL 30	—	yes	Yes, automatic or manual generation of test vectors	Master PAL	external	yes	yes	yes
Structured Design	any terminal	SD20/24	—	yes	Yes, manual generation of test vectors	Master PAL or on wafertape	external or internal	yes	yes	no

All these systems allow software supported PAL design. They perform a *fuse-verify* in the PROM mode and can do a *logic simulation* in the PAL mode!
All 5 programmers and 4 development systems can be connected with a host computer to run more sophisticated design software and/or for storage use.

PAL Legend

Constants

LOW (L)	NEGATIVE (N)	ZERO (0)	GND	FALSE	×	FUSE NOT BLOWN
HIGH (H)	POSITIVE (P)	ONE (1)	V_{CC}	TRUE	–	FUSE BLOWN

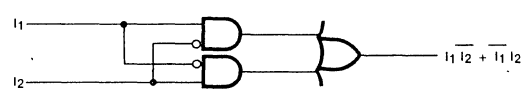
Operators

```
 =   EQUAL
:=   REPLACED BY FOLLOWING CLOCK
 /   COMPLEMENT
 *   AND, PRODUCT
 +   OR, SUM
:+:  XOR
:*:  XNOR
( )  CONDITIONAL THREE STATE, IF STATEMENT, ARITHMETIC
```

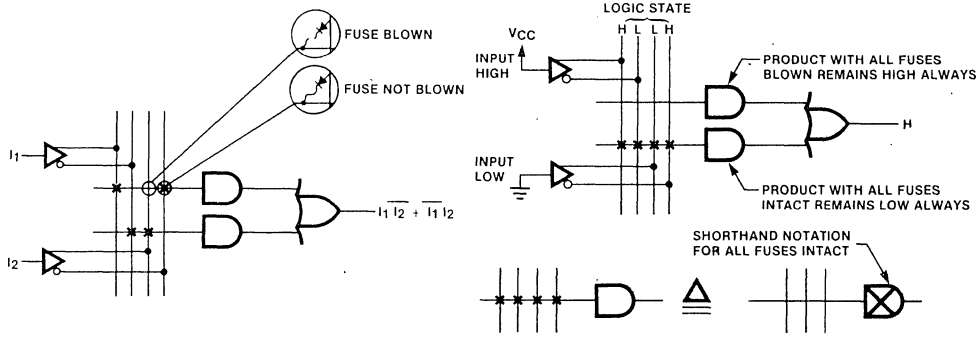
Equations

Standard	$Q_1 = I_1 \overline{I_2} + \overline{I_1} I_2$
PALASM	`O1 = I1*/I2 + /I1*I2`

Conventional Symbology



PAL Symbology



PAL Logic Diagram

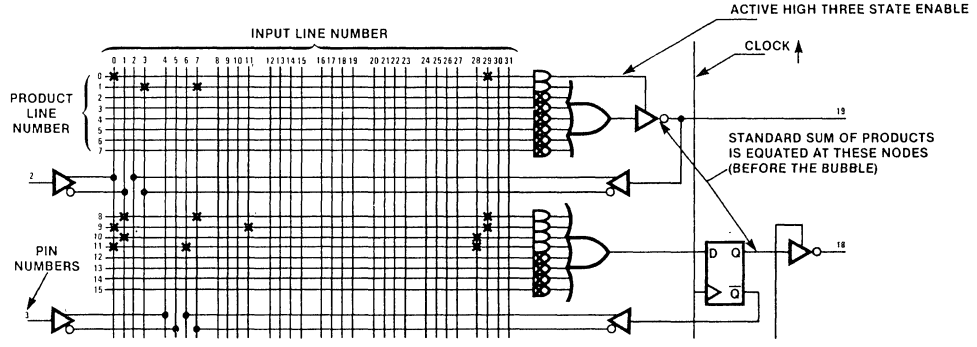


FIGURE 3-29. PAL Legend

Sample PAL Design Specification

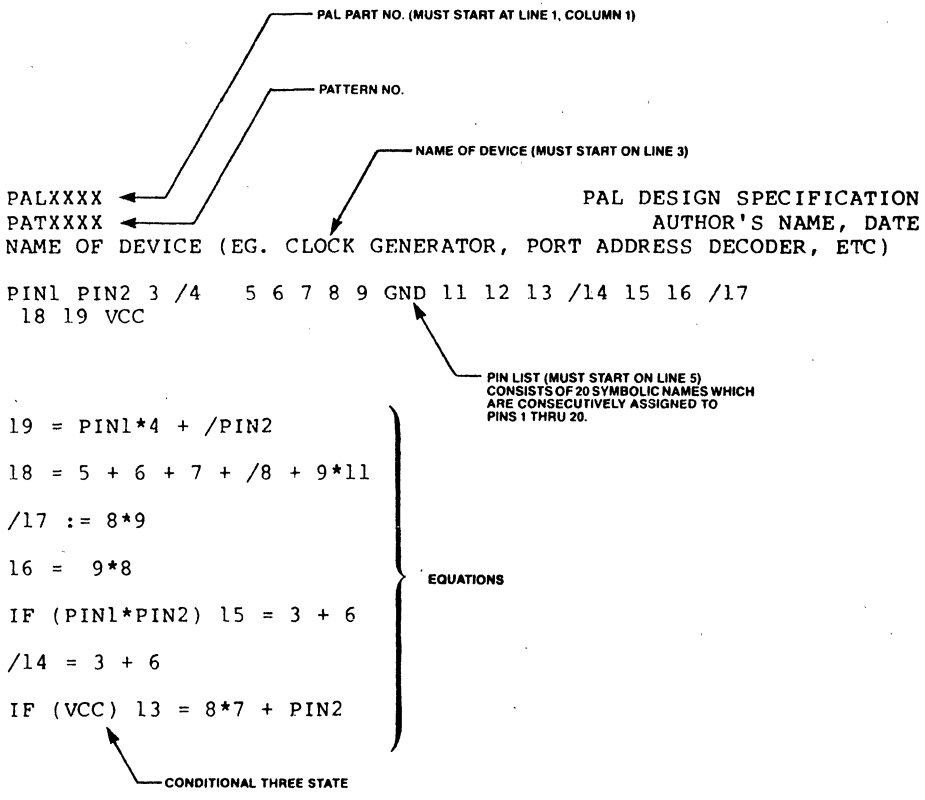


FIGURE 3-30. Sample PAL Design Specification.

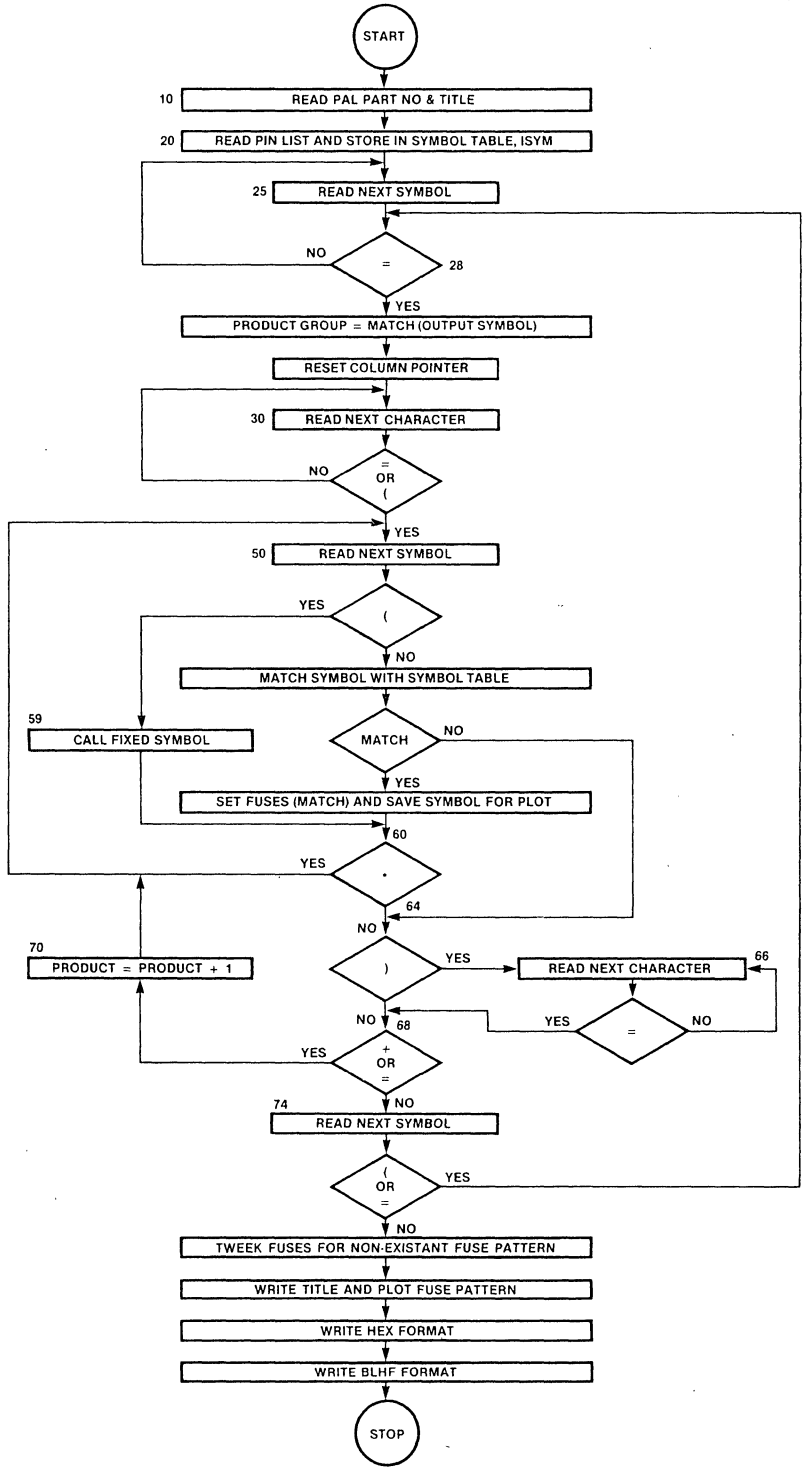


FIGURE 3-31. PALASM™ Flow Chart.

Listing 1. PALASM Source Code for 20 Series

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0


C***PALASM20**PALASM20**PALASM20**PALASM20**PALASM20**PALASM20**PALASM20PAL00010
C                                                                       PAL00020
C  P A L A S M  2 0  -  TRANSLATES SYMBOLIC EQUATIONS INTO PAL OBJECT   PAL00030
C                       CODE.  FORMATTED FOR DIRECT INPUT TO STANDARD   PAL00040
C                       PROM PROGRAMMERS.                               PAL00050
C                                                                       PAL00060
C                       INPUT:        PAL DESIGN SPECIFICATION ASSIGNED PAL00070
C                                     TO RPD(1).  OPERATION CODES ARE   PAL00080
C                                     ASSIGNED TO ROP(5).               PAL00090
C                                                                       PAL00100
C                       OUTPUT:       ECHO, SIMULATION, AND FUSE PATTERN PAL00110
C                                     ARE ASSIGNED TO PDF(6).  HEX AND  PAL00120
C                                     BINARY PROGRAMMING FORMATS ARE    PAL00130
C                                     ASSIGNED TO PDF(6).  PROMPTS AND  PAL00140
C                                     ERROR MESSAGES ARE ASSIGNED TO    PAL00150
C                                     PMS(0).                           PAL00160
C                                                                       PAL00170
C                       PART NUMBER:  THE PAL PART NUMBER MUST APPEAR   PAL00180
C                                     IN COLUMN ONE OF LINE ONE.        PAL00190
C                                                                       PAL00200
C                       PIN LIST:     20 SYMBOLIC PIN NAMES MUST APPEAR PAL00210
C                                     STARTING ON LINE FIVE.            PAL00220
C                                                                       PAL00230
C                       EQUATIONS:    STARTING FIRST LINE AFTER THE     PAL00240
C                                     PIN LIST IN THE FOLLOWING FORMS:  PAL00250
C                                                                       PAL00260
C                                        A = B*C + D                    PAL00270
C                                                                       PAL00280
C                                        A := B*C + D                   PAL00290
C                                                                       PAL00300
C                                        IF( A*B )  C = D + E           PAL00310
C                                                                       PAL00320
C                                        A2 := (A1:*:B1) + /C           PAL00330
C                                                                       PAL00340
C                                     ALL CHARACTERS FOLLOWING ';' ARE  PAL00350
C                                     IGNORED UNTIL THE NEXT LINE.      PAL00360
C                                                                       PAL00370
C                                     BLANKS ARE IGNORED.               PAL00380
C                                                                       PAL00390
C                       OPERATORS:    ( IN HIERARCHY OF EVALUATION )    PAL00400
C                                                                       PAL00410
C                                      ;     COMMENT FOLLOWS            PAL00420
C                                      /     COMPLEMENT                 PAL00430
C                                      *     AND (PRODUCT)              PAL00440
C                                      +     OR (SUM)                   PAL00450
C                                     :+:    XOR (EXCLUSIVE OR)         PAL00460
C                                     :*:    XNOR (EXCLUSIVE NOR)       PAL00470
C                                     ( )    CONDITIONAL THREE-STATE    PAL00480
C                                            OR FIXED SYMBOL            PAL00490
C                                      =     EQUALITY                   PAL00500
C                                     :=     REPLACED BY (AFTER CLOCK)  PAL00510
C                                                                       PAL00520
C                       FIXED SYMBOLS                                   PAL00530
C                       FOR PAL16X4                                     PAL00540
C                       AND PAL16A4                                     PAL00550
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

C                        ONLY:          (AN+/BN)       WHERE N = 0,1,2,3      PAL00560
C                                       (AN+BN)        FOR OUTPUT PINS        PAL00570
C                                       (AN)           17,16,15,14, RESP      PAL00580
C                                       (/AN+/BN)      A IS OUTPUT            PAL00590
C                                       (/BN)          B IS INPUT             PAL00600
C                                       (AN:+:BN)                             PAL00610
C                                       (AN*/BN)                              PAL00620
C                                       (/AN+BN)                              PAL00630
C                                       (AN:*:BN)                             PAL00640
C                                       (BN)                                  PAL00650
C                                       (AN*BN)                               PAL00660
C                                       (/AN)                                 PAL00670
C                                       (/AN*/BN)                             PAL00680
C                                       (/AN*BN)                              PAL00690
C                                                                             PAL00700
C                        FUNCTION       L, H, X, Z, AND C ARE VALID           PAL00710
C                          TABLE:       FUNCTION TABLE VECTOR ENTRIES.        PAL00720
C                                                                             PAL00730
C                        REFERENCE:     A COMPLETE USERS GUIDE TO             PAL00740
C                                       DESIGNING WITH PALS USING PALASM      PAL00750
C                                       IS PROVIDED IN THE MONOLITHIC         PAL00760
C                                       MEMORIES PAL HANDBOOK.                PAL00770
C                                                                             PAL00780
C                        SUBROUTINES:   INITLZ,SETSYM,INCR,MATCH,FIXSYM,      PAL00790
C                                       IXLATE,ECHO,CAT,PINOUT,PLOT,TWEEK,    PAL00800
C                                       BINR,HEX,SLIP,FANTOM,IODC2,IODC4,     PAL00810
C                                       TEST,FIXTST                           PAL00820
C                                                                             PAL00830
C                        REV LEVEL:     02/12/82 (VAX/VMS VERSION)            PAL00840
C                                       09/14/82 (GAI/SAO FAULT TESTING)      PAL00850
C                                       10/15/82 (JEDEC FORMAT)               PAL00860
C                                       By:Imtiyaz Bengali                    PAL00870
C                                                                             PAL00880
C                        AUTHORS:       JOHN BIRKNER AND VINCENT COLI         PAL00890
C                                       MONOLITHIC MEMORIES INC.              PAL00900
C                                       1165 EAST ARQUES AVENUE               PAL00910
C                                       SUNNYVALE, CALIFORNIA 94043           PAL00920
C                                       (408) 739-3535                        PAL00930
C                                                                             PAL00940
C                        FINE PRINT:    MONOLITHIC MEMORIES TAKES NO          PAL00950
C                                       RESPONSIBILITY FOR THE OPERATION      PAL00960
C                                       OR MAINTENANCE OF THIS PROGRAM.       PAL00970
C                                       THE SOURCE CODE AS PRINTED HERE       PAL00980
C                                       PRODUCED THE OBJECT CODE OF THE       PAL00990
C                                       EXAMPLES IN THE APPLICATIONS          PAL01000
C                                       SECTION ON A VAX/VMS 11/780           PAL01010
C                                       COMPUTER AND A NATIONAL CSS IBM       PAL01020
C                                       SYSTEM/370 FORTRAN IV(G).             PAL01030
C                                                                             PAL01040
C*****************************************************************************PAL01050
C                                                                             PAL01060
C                                                                             PAL01070
C*****************************************************************************PAL01080
C                                                                             PAL01090
C                                                                             PAL01100
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

C       MAIN PROGRAM                                                    PAL01110
C                                                                       PAL01120
        IMPLICIT INTEGER (A-Z)                                          PAL01130
        INTEGER IPAL(4),REST(73),PATNUM(80),TITLE(80),COMP(80),         PAL01140
       1        ISYM(8,20),IBUF(8,20)                                   PAL01150
        LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR,  PAL01160
       1        LFIX,LFIRST,LMATCH,LFUSES(32,64),LPHASE(20),LBUF(20),   PAL01170
       2        LPROD(80),LSAME,LACT,LOPERR,LINP,LPRD,LERR,LSA11,LSA01  PAL01180
        INTEGER   BEL                                                   PAL01190
        COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR   PAL01200
        COMMON /PGE/ IPAGE(80,200)                                      PAL01210
        COMMON /LFUSES/LFUSES                                           PAL01220
        COMMON /LUNIT/ PMS,POF,PDF                                      PAL01230
        COMMON /FTEST/ IFUNCT,IDESC,IEND                                PAL01240
        DATA E/'E'/,O/'O'/,T/'T'/,P/'P'/,B/'B'/,H/'H'/,S/'S'/,L/'L'/,   PAL01250
       1     N/'N'/,C/'C'/,Q/'Q'/,U/'U'/,F/'F'/,R/'R'/,A/'A'/,I/'I'/,   PAL01260
       2     J/'J'/                                                     PAL01270
        DATA BB/'B'/,CC/'C'/,DD/'D'/,EE/'E'/,FF/'F'/,II/'I'/,JJ/'J'/,   PAL01280
       1     NN/'N'/,OO/'O'/,PP/'P'/,RR/'R'/,SS/'S'/,TT/'T'/,UU/'U'/    PAL01290
        DATA BEL/Z07000000/                                             PAL01300
C                                                                       PAL01310
C                                                                       PAL01320
C       ASSIGNMENT OF DATA SET REFERENCES                               PAL01330
C       RPD - PAL DESIGN SPECIFICATION (INPUT)                          PAL01340
C       ROC - OPERATION CODE (INPUT)                                    PAL01350
C       POF - ECHO, PINOUT, TEST, AND PLOT (OUTPUT)                     PAL01360
C       PDF - HEX AND BINARY FORMAT PROGRAM TAPES (OUTPUT)              PAL01370
C       PMS - PROMPTS AND ERROR MESSAGES (OUTPUT)                       PAL01380
        WRITE(6,3)                                                      PAL01390
    3   FORMAT(/,' PALASM VERSION 1.5')                                 PAL01400
        WRITE(6,1)                                                      PAL01410
    1   FORMAT(/,' WHAT IS THE LOGICAL UNIT NUMBER FOR OUTPUT(6)?: ')   PAL01420
        READ(5,2) LUN                                                   PAL01430
    2   FORMAT(I4)                                                      PAL01440
        RPD=1                                                           PAL01450
        ROC=5                                                           PAL01460
        POF=6                                                           PAL01470
        PDF=6                                                           PAL01480
        PMS=10                                                          PAL01490
        IFUNCT=0                                                        PAL01500
        IDESC=0                                                         PAL01510
C       INITIALIZE LSAME AND LACT TO FALSE (ACTIVE HIGH/LOW ERROR)      PAL01520
        LSAME=.FALSE.                                                   PAL01530
        LACT=.FALSE.                                                    PAL01540
C       INITIALIZE LOPERR TO FALSE (OUTPUT PIN ERROR)                   PAL01550
        LOPERR=.FALSE.                                                  PAL01560
C       INITIALIZE LINP TO FALSE (INPUT PIN ERROR)                      PAL01570
        LINP=.FALSE.                                                    PAL01580
C       INITIALIZE LPRD TO FALSE (PRODUCT LINE ERROR)                   PAL01590
        LPRD=.FALSE.                                                    PAL01600
C       READ IN FIRST 4 LINES OF THE PAL DESIGN SPECIFICATION           PAL01610
        READ(RPD,10) IPAL,INOAI,IOT,INOO,REST,PATNUM,TITLE,COMP         PAL01620
   10   FORMAT(4A1,A1,A1,A1,73A1,/,80A1,/,80A1,/,80A1)                  PAL01630
C       READ IN PIN LIST (LINE 5) THROUGH THE END OF THE PAL DESIGN     PAL01640
C        SPECIFICATION                                                  PAL01650
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      DO 15 J=1,200                                                      PAL01660
         READ(RPD,11,END=16) (IPAGE(I,J),I=1,80)                         PAL01670
   11    FORMAT(80A1)                                                    PAL01680
C     CHECK FOR 'FUNCTION TABLE' AND SAVE ITS LINE NUMBER                PAL01690
      IF(      IFUNCT.EQ.0 .AND.IPAGE(1,J).EQ.FF.AND.                    PAL01700
     1    IPAGE(2,J).EQ.UU.AND.IPAGE(3,J).EQ.NN.AND.                     PAL01710
     2    IPAGE(4,J).EQ.CC.AND.IPAGE(5,J).EQ.TT.AND.                     PAL01720
     3    IPAGE(6,J).EQ.II.AND.IPAGE(7,J).EQ.OO.AND.                     PAL01730
     4    IPAGE(8,J).EQ.NN.AND.IPAGE(10,J).EQ.TT.AND.                    PAL01740
     5    IPAGE(12,J).EQ.BB.AND.IPAGE(14,J).EQ.EE ) IFUNCT=J             PAL01750
C     CHECK FOR 'DESCRIPTION' AND SAVE ITS LINE NUMBER                   PAL01760
      IF(      IDESC.EQ.0 .AND.IPAGE(1,J).EQ.DD.AND.                     PAL01770
     1    IPAGE(2,J).EQ.EE.AND.IPAGE(3,J).EQ.SS.AND.                     PAL01780
     2    IPAGE(4,J).EQ.CC.AND.IPAGE(5,J).EQ.RR.AND.                     PAL01790
     3    IPAGE(6,J).EQ.II.AND.IPAGE(7,J).EQ.PP.AND.                     PAL01800
     4    IPAGE(8,J).EQ.TT.AND.IPAGE(9,J).EQ.II.AND.                     PAL01810
     5    IPAGE(10,J).EQ.OO.AND.IPAGE(11,J).EQ.NN ) IDESC=J              PAL01820
   15 CONTINUE                                                           PAL01830
C     SAVE THE LAST LINE NUMBER OF THE PAL DESIGN SPECIFICATION          PAL01840
   16 IEND=J-1                                                           PAL01850
      CALL INITL2(INOAI,IOT,INOO,ITYPE,LFUSES,IC,IL,IBLOW,LFIX,IPCIR)   PAL01860
      ILE=IL+1                                                          PAL01870
C     PRINT ERROR MESSAGE FOR INVALID PAL PART TYPE                      PAL01880
      IF(ITYPE.NE.0) GO TO 17                                           PAL01890
         WRITE(PMS,18) IPAL,INOAI,IOT,INOO                              PAL01900
   18    FORMAT(/,' PAL PART TYPE ',4A1,A1,A1,A1,' IS INCORRECT')       PAL01910
         STOP                                                           PAL01920
C     GET 20 PIN NAMES                                                  PAL01930
   17 DO 20 J=1,20                                                      PAL01940
   20    CALL GETSYM(LPHASE,ISYM,J,IC,IL,LFIX)                          PAL01950
         IF(.NOT.(LEQUAL.OR.LLEFT.OR.LAND.OR.LOR.OR.LRIGHT)) GO TO 24   PAL01960
            WRITE(PMS,23)                                               PAL01970
   23       FORMAT(/,' LESS THAN 20 PIN NAMES IN PIN LIST')             PAL01980
            STOP                                                        PAL01990
   24 ILE=IL                                                            PAL02000
C     BYPASS FUSE PLOT ASSEMBLY IF HAL (H IN COLUMN 1, LINE 1)          PAL02010
      IF( IPAL(1).EQ.H ) GO TO 108                                      PAL02020
   25 CALL GETSYM(LBUF,IBUF,1,IC,IL,LFIX)                               PAL02030
   28    IF(.NOT.LEQUAL) GO TO 25                                       PAL02040
         COUNT=0                                                        PAL02050
         ILL=IL                                                         PAL02060
         CALL MATCH(IMATCH,IBUF,ISYM)                                   PAL02070
         IF( IMATCH.EQ.0 ) GO TO 100                                    PAL02080
         IPRD=IMATCH                                                    PAL02090
C        CHECK FOR VALID POLARITY                                       PAL02100
         LSAME = ( (     LPHASE(IMATCH)).AND.(     LBUF(1)).OR.        PAL02110
     1             (.NOT.LPHASE(IMATCH)).AND.(.NOT.LBUF(1)) )           PAL02120
         IF( IOT.EQ.H.AND.(.NOT.LSAME) )                    LACT=.TRUE.  PAL02130
         IF( (.NOT.(IOT.EQ.H.OR.IOT.EQ.C)).AND.(LSAME) ) LACT=.TRUE.    PAL02140
C        CHECK FOR VALID OUTPUT PIN                                     PAL02150
         IF( (ITYPE.EQ.1.OR.ITYPE.EQ.5.OR.ITYPE.EQ.6).AND.IOT.NE.A.     PAL02160
     1   AND.(IMATCH.LT.12.OR.IMATCH.GT.19) ) LOPERR=.TRUE.             PAL02170
         IF(  ITYPE.EQ.2.AND.(IMATCH.LT.13.OR.IMATCH.GT.18) )           PAL02180
     1                                        LOPERR=.TRUE.             PAL02190
         IF(  ITYPE.EQ.3.AND.(IMATCH.LT.14.OR.IMATCH.GT.17) )           PAL02200
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

     1                                                 LOPERR=.TRUE.                PAL02210
          IF(  ITYPE.EQ.4.AND.(IMATCH.LT.15.OR.IMATCH.GT.16) )                       PAL02220
     1                                                 LOPERR=.TRUE.                PAL02230
          IF( (LACT).OR.(LOPERR) ) GO TO 100                                         PAL02240
          I88PRO=(19-IMATCH)*8 + 1                                                   PAL02250
C         START PAL16C1 ON PRODUCT LINE 24 (I88PRO=25)                               PAL02260
          IF(IOT.EQ.C) I88PRO=25                                                     PAL02270
          IC=0                                                                       PAL02280
    30      CALL INCR(IC,IL,LFIX)                                                    PAL02290
            IF( .NOT.(LEQUAL.OR.LLEFT) ) GO TO 30                                    PAL02300
            LPROD(I88PRO)=.TRUE.                                                     PAL02310
            IF( (.NOT.LLEFT).AND.(REST(3).NE.PP) ) CALL SLIP(LFUSES,                 PAL02320
     1         I88PRO,INOAI,IOT,IBOD,IBLOW)                                          PAL02330
          DO 70 I8PRO=1,16                                                           PAL02340
              COUNT = COUNT + 1                                                      PAL02350
              IF( (LXOR).AND.I8PRO.NE.5 ) GO TO 70                                   PAL02360
              IPROD = I88PRO + I8PRO - 1                                             PAL02370
              LPROD(IPROD)=.TRUE.                                                    PAL02380
              LFIRST=.TRUE.                                                          PAL02390
    50          ILL=IL                                                             PAL02400
                CALL GETSYM(LBUF,IBUF,1,IC,IL,LFIX)                                PAL02410
              IF( (ITYPE.EQ.1.OR.ITYPE.EQ.2.AND.IPRD.GT.13                         PAL02420
     1             .AND.IPRD.LT.18).AND.COUNT.GT.2 ) LPRD=.TRUE.                   PAL02430
              IF( (ITYPE.EQ.3.OR.ITYPE.EQ.2.AND.(IPRD.EQ.13.OR.                    PAL02440
     1             IPRD.EQ.18)).AND.COUNT.GT.4 ) LPRD=.TRUE.                       PAL02450
              IF( IOT.NE.A.AND.IOT.NE.C.AND.COUNT.GT.8 ) LPRD=.TRUE.               PAL02460
              IF( .NOT.LPRD ) GO TO 69                                             PAL02470
              IF(IL.NE.IFUNCT.AND.IL.NE.IDESC) ILL=IL                              PAL02480
              IPROD = IPROD - 1                                                    PAL02490
              GO TO 118                                                            PAL02500
    69          IF(LFIX) GO TO 59                                                  PAL02510
                CALL MATCH(IMATCH,IBUF,ISYM)                                       PAL02520
C               CHECK FOR INVALID INPUT PIN                                        PAL02530
                IF( ITYPE.EQ.1.AND.(IMATCH.GE.12.AND.IMATCH.LE.19) )               PAL02540
     1              LINP=.TRUE.                                                    PAL02550
                IF( ITYPE.EQ.2.AND.(IMATCH.GE.13.AND.IMATCH.LE.18) )               PAL02560
     1              LINP=.TRUE.                                                    PAL02570
                IF( ITYPE.EQ.3.AND.(IMATCH.GE.14.AND.IMATCH.LE.17) )               PAL02580
     1              LINP=.TRUE.                                                    PAL02590
                IF( ITYPE.EQ.4.AND.(IMATCH.EQ.15.OR.IMATCH.EQ.16) )                PAL02600
     1              LINP=.TRUE.                                                    PAL02610
                IF( ITYPE.EQ.5.AND.(IMATCH.EQ.12.OR.IMATCH.EQ.19) )                PAL02620
     1              LINP=.TRUE.                                                    PAL02630
                IF( ITYPE.EQ.6.AND.(IMATCH.EQ.1.OR.IMATCH.EQ.11) )                 PAL02640
     1              LINP=.TRUE.                                                    PAL02650
                ILL=IL                                                             PAL02660
                IF(LINP) GO TO 100                                                 PAL02670
                IF( IMATCH.EQ.0 ) GO TO 100                                        PAL02680
                IF( IMATCH.EQ.10.OR.IMATCH.EQ.99 ) GO TO 64                        PAL02690
                IF(.NOT.LFIRST) GO TO 58                                           PAL02700
                    LFIRST=.FALSE.                                                 PAL02710
                    DO 56 I=1,32                                                   PAL02720
                        IBLOW = IBLOW + 1                                          PAL02730
    56                  LFUSES(I,IPROD)=.TRUE.                                     PAL02740
    58          CALL IXLATE(IINPUT,IMATCH,LPHASE,LBUF,ITYPE)                       PAL02750
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

                IF(IINPUT.GE.0) GO TO 60                                        PAL02760
                IBLOW = IBLOW - 1                                               PAL02770
                LFUSES(IINPUT,IPROD)=.FALSE.                                    PAL02780
                CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.FALSE.,ITYPE,           PAL02790
     |                    LPROD,IOUT,IBLOW,IPCTR)                               PAL02800
                GO TO 60                                                        PAL02810
   59           CALL FIXSYM(LBUF,IBUF,IC,IL,LFIRST,LFUSES,IBLOW,                PAL02820
     |                      IPROD,LFIX)                                         PAL02830
   60           IF(LAND) GO TO 50                                               PAL02840
   64         IF(.NOT.LRIGHT) GO TO 68                                          PAL02850
   66           CALL INCR(IC,IL,LFIX)                                           PAL02860
                IF(.NOT.LEQUAL)  GO TO 66                                       PAL02870
   68         IF( .NOT.(LOR.OR.LEQUAL) ) GO TO 74                               PAL02880
   70         CONTINUE                                                         PAL02890
   74      ILL=IL                                                              PAL02900
           CALL GETSYM(LBUF,IBUF,1,IC,IL,LFIX)                                 PAL02910
           IF(LLEFT.OR.LEQUAL) GO TO 28                                        PAL02920
  100 IF( ILL.EQ.IFUNCT.OR.ILL.EQ.IDESC ) GO TO 102                            PAL02930
C     PRINT AN ERROR MESSAGE IF UNRECOGNIZABLE SYMBOL                          PAL02940
      ILERR=ILL+4                                                             PAL02950
      WRITE(PMS,99) BEL                                                       PAL02960
   99 FORMAT(' ',A1)                                                          PAL02970
      WRITE(PMS,101) (IBUF(I,1),I=1,8),ILERR,(IPAGE(I,ILL),I=1,80)            PAL02980
  101 FORMAT(/,' ERROR SYMBOL = ',8A1,'       IN LINE NUMBER ',I3,           PAL02990
     |       /,' ',80A1)                                                       PAL03000
C     PRINT AN ERROR MESSAGE FOR ACTIVE HIGH/LOW PART                          PAL03010
      IF( (LACT).AND.(     LSAME).AND.(.NOT.LOPERR) )                         PAL03020
     |          WRITE(PMS,103) IPAL,INOAI,IOT,INOO                            PAL03030
  103 FORMAT(' OUTPUT MUST BE INVERTED SINCE ',4A1,A1,A1,A1,                   PAL03040
     |       ' IS AN ACTIVE LOW DEVICE')                                       PAL03050
      IF( (LACT).AND.(.NOT.LSAME).AND.(.NOT.LOPERR) )                         PAL03060
     |          WRITE(PMS,109) IPAL,INOAI,IOT,INOO                            PAL03070
  109 FORMAT(' OUTPUT CANNOT BE INVERTED SINCE ',4A1,A1,A1,A1,                 PAL03080
     |       ' IS AN ACTIVE HIGH DEVICE')                                      PAL03090
C     PRINT AN ERROR MESSAGE FOR AN INVALID OUTPUT PIN                         PAL03100
      IF( (LOPERR).AND.IMATCH.NE.0 )                                          PAL03110
     |          WRITE(PMS,105) IMATCH,IPAL,INOAI,IOT,INOO                     PAL03120
  105 FORMAT(' THIS PIN NUMBER ',I2,' IS AN INVALID OUTPUT PIN',               PAL03130
     |       ' FOR ',4A1,A1,A1,A1)                                             PAL03140
C     PRINT AN ERROR MESSAGE FOR AN INVALID INPUT PIN                          PAL03150
      IF(LINP) WRITE(PMS,115) IMATCH,IPAL,INOAI,IOT,INOO                      PAL03160
  115 FORMAT(' THIS PIN NUMBER ',I2,' IS AN INVALID INPUT PIN',                PAL03170
     |       ' FOR ',4A1,A1,A1,A1)                                             PAL03180
C     PRINT AN ERROR MESSAGE FOR INVALID PRODUCT LINE                          PAL03190
  118 ILERR=ILL+4                                                             PAL03200
      IF(LPRD) WRITE(PMS,119)                                                 PAL03210
     | (ISYM(I,IPRD),I=1,8),IPRD,ILERR,(IPAGE(I,ILL),I=1,80)                   PAL03220
  119 FORMAT(/,' OUTPUT PIN NAME = ',8A1,'  OUTPUT PIN NUMBER = ',I2,          PAL03230
     |       /,' MINTERM IN LINE NUMBER ',I3,/,' ',80A1)                       PAL03240
      IF( LPRD.AND.COUNT.LT.8 )                                               PAL03250
     |          WRITE(PMS,116) IPROD,IPAL,INOAI,IOT,INOO                      PAL03260
  116 FORMAT(' THIS PRODUCT LINE NUMBER ',I2,' IS NOT VALID',                  PAL03270
     |       ' FOR ',4A1,A1,A1,A1)                                             PAL03280
      IF( LPRD.AND.COUNT.GT.8 )                                               PAL03290
     |          WRITE(PMS,117) IPAL,INOAI,IOT,INOO                            PAL03300
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

  117 FORMAT(' MAXIUM OF 8 PRODUCT LINES ARE VALID FOR ',4A1,A1,A1,A1,   PAL03310
     1     /,' TOO MANY MINTERMS ARE SPECIFIED IN THIS EQUATION')        PAL03320
      STOP                                                              PAL03330
  102 IF(ITYPE.LE.4) CALL TWEEK(ITYPE,IOT,LFUSES)                       PAL03340
  108 WRITE(6,106)                                                      PAL03350
  106 FORMAT(/,' OPERATION CODES:')                                     PAL03360
      WRITE(6,107)                                                      PAL03370
  107 FORMAT(/,' E=ECHO INPUT  O=PINOUT  T=SIMULATE  P=PLOT  B=BRIEF',  PAL03380
     1       /,' H=HEX  S=SHORT  L=BHLF  N=BNPF  C=CATALOG  Q=QUIT',    PAL03390
     2       /,' F=FAULT TESTING  J=JEDEC FORMAT')                      PAL03400
      WRITE(6,110)                                                      PAL03410
  110 FORMAT(/,' ENTER OPERATION CODE: ')                               PAL03420
      READ(ROC,120) IOP                                                 PAL03430
  120 FORMAT(A1)                                                        PAL03440
C     CALL IODC2                                                        PAL03450
      IF(POF.NE.6) WRITE(POF,125)                                       PAL03460
  125 FORMAT('1')                                                       PAL03470
      IF(IOP.EQ.E) CALL ECHO(IPAL,INOAI,IOT,INOO,REST,PATNUM,TITLE,     PAL03480
     1                       COMP)                                      PAL03490
      IF(IOP.EQ.O) CALL PINOUT(IPAL,INOAI,IOT,INOO,TITLE)               PAL03500
      IF(IOP.EQ.T) CALL TEST(LPHASE,LBUF,TITLE,IC,IL,ILE,ISYM,IBUF,     PAL03510
     1                       ITYPE,INOO,LFIX,IPCTR,LERR,ISAF,IPCTR1,    PAL03520
     2                       .FALSE.,.FALSE.)                           PAL03530
C     INITIALIZING THE TOTAL FAULTS, CALLING FOR SA1/SA0 TEST           PAL03540
      ISAF=0                                                            PAL03550
      IF(IOP.EQ.F) GO TO 200                                            PAL03560
      IF(IOP.EQ.JJ) CALL PLOTF                                          PAL03570
  135 IF(IOP.EQ.P) CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.TRUE.,ITYPE, PAL03580
     1                       LPROD,IOP,IBLOW,IPCTR0)                    PAL03590
      IF(IOP.EQ.B) CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.TRUE.,ITYPE, PAL03600
     1                       LPROD,IOP,IBLOW,IPCTR0)                    PAL03610
      IF(IOP.EQ.H) CALL HEX(LFUSES,H)                                   PAL03620
      IF(IOP.EQ.S) CALL HEX(LFUSES,S)                                   PAL03630
      IF(IOP.EQ.L) CALL BINR(LFUSES,H,L)                                PAL03640
      IF(IOP.EQ.N) CALL BINR(LFUSES,P,N)                                PAL03650
      IF(IOP.EQ.C) CALL CAT                                             PAL03660
C     CALL IODC4                                                        PAL03670
      IF(IOP.NE.Q ) GO TO 108                                           PAL03680
      STOP                                                              PAL03690
C                                                                       PAL03700
C     SETTING THE PARAMETERS FOR SA1/SA0 TESTS                          PAL03710
  200 IPCTR=0                                                           PAL03720
      CALL TEST(LPHASE,LBUF,TITLE,IC,IL,ILE,ISYM,IBUF,ITYPE,            PAL03730
     1          INOO,IFIX,IPCTR,LERR,ISAF,IPCTR1,.FALSE.,.FALSE.)       PAL03740
      IPCTR0=IPCTR                                                      PAL03750
C     LOOPING FOR SA1 TEST                                              PAL03760
      DO 210 IPCTR1=1,IPCTR0                                            PAL03770
      LSA11=.TRUE.                                                      PAL03780
      CALL TEST(LPHASE,LBUF,TITLE,IC,IL,ILE,ISYM,IBUF,ITYPE,            PAL03790
     1          INOO,IFIX,IPCTR,LERR,ISAF,IPCTR1,LSA11,.FALSE.)         PAL03800
  210 CONTINUE                                                          PAL03810
      ISA1=ISAF                                                         PAL03820
C     LOOPING FOR SA0 TEST                                              PAL03830
      DO 215 IPCTR1=1,IPCTR0                                            PAL03840
      LSA01=.TRUE.                                                      PAL03850
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      CALL TEST(LPHASE,LBUF,TITLE,IC,IL,ILE,ISYM,IBUF,ITYPE,              PAL03860
     1          INOO,IFIX,IPCTR,LERR,ISAF,IPCTR1,.FALSE.,LSA01)           PAL03870
  215 CONTINUE                                                            PAL03880
      ISA0=ISAF-ISA1                                                      PAL03890
      IFAULT=(ISAF*100)/(IPCTR0*2)                                        PAL03900
      WRITE(POF,220) ISA1                                                 PAL03910
  220 FORMAT(/,' NUMBER OF STUCK AT ONE (SA1)  FAULTS ARE =' I3)          PAL03920
      WRITE(POF,225) ISA0                                                 PAL03930
  225 FORMAT(/,' NUMBER OF STUCK AT ZERO (SA0) FAULTS ARE =' I3)          PAL03940
      WRITE(POF,230) IFAULT                                               PAL03950
  230 FORMAT(/,' PRODUCT  TERM   COVERAGE                 =' I3,'%',//)   PAL03960
      GO TO 135                                                           PAL03970
C                                                                         PAL03980
      END                                                                 PAL03990
C                                                                         PAL04000
C  ************THIS SUBROUTINE IS ADDED FOR JEDEC FORMAT**********       PAL04010
C  THE FOLLOWING SUBROUTINE GIVES JEDEC FORMATTED OUTPUT FOR              PAL04020
C  PROGRAMMING COMPATIBILITY WITH DATA I/O PROGRAMMERS                    PAL04030
      SUBROUTINE PLOTF                                                    PAL04040
      IMPLICIT INTEGER (A-Z)                                              PAL04050
      LOGICAL  LFUSES (32,64)                                             PAL04060
      INTEGER IPBUF(32),ZERO,ONE                                          PAL04070
      INTEGER ISUM(4),IADR,STX,ETX,IDEC(4),IPT,IINP,J1,J2                 PAL04080
      INTEGER IDECIO(4),ISUMV(4),ISUMIO(4),BUFIO(32)                      PAL04090
      COMMON  /LUNIT/ PMS,POF,PDF                                         PAL04100
      COMMON  /IPT/ IPT                                                   PAL04110
      COMMON  /LFUSES/ LFUSES                                             PAL04120
      COMMON  /SUM/ ISUM,IDEC,IPBUF,BUFIO                                 PAL04130
      DATA    ZERO/'0'/, ONE/'1'/                                         PAL04140
      IADR=0                                                              PAL04150
      STX=2                                                               PAL04160
      ETX=3                                                               PAL04170
      ISUM(2)=0                                                           PAL04180
      ISUM(4)=230                                                         PAL04190
      WRITE(PDF,10) STX                                                   PAL04200
   10 FORMAT(' ',A1,'*F0*')                                               PAL04210
      DO 300 IPT=1,64                                                     PAL04220
      DO 50  IINP=1,32                                                    PAL04230
      IF(LFUSES(IINP,IPT)) IPBUF(IINP)=ONE                                PAL04240
      IF(.NOT.(LFUSES(IINP,IPT))) IPBUF(IINP)=ZERO                        PAL04250
   50 CONTINUE                                                            PAL04260
      IF(LFUSES(1,IPT)) GO TO 100                                         PAL04270
      IF(.NOT.LFUSES(2,IPT)) GO TO 250                                    PAL04280
  100 IDEC(4)=IADR                                                        PAL04290
      DO 150 J=1,3                                                        PAL04300
      J1=5-J                                                              PAL04310
      J2=4-J                                                              PAL04320
      IDEC(J2)=IDEC(J1)/10                                                PAL04330
      IDEC(J1)=IDEC(J1)-10*IDEC(J2)                                       PAL04340
      IDECIO(J1)=ICONV(IDEC(J1))                                          PAL04350
  150 CONTINUE                                                            PAL04360
      IDECIO(1)=ICONV(IDEC(1))                                            PAL04370
      CALL SUMCHK                                                         PAL04380
      WRITE(PDF,201)IDECIO,IPBUF                                          PAL04390
  201 FORMAT(' L',4A1,' ',8(4A1,' '),'*')                                 PAL04400
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0


  250 IADR=IADR+32                                                      PAL04410
  300 CONTINUE                                                          PAL04420
      ISUMIO(1)=ICONV(ISUM(2)/16)                                       PAL04430
      ISUM(2)=MOD(ISUM(2),16)                                           PAL04440
      ISUMIO(2)=ICONV(ISUM(2))                                          PAL04450
      ISUMIO(3)=ICONV(ISUM(4)/16)                                       PAL04460
      ISUM(4)=MOD(ISUM(4),16)                                           PAL04470
      ISUMIO(4)=ICONV(ISUM(4))                                          PAL04480
      WRITE(PDF,400) ETX,ISUMIO                                         PAL04490
  400 FORMAT(' *',A1,4A1,'*',/)                                         PAL04500
      RETURN                                                            PAL04510
      END                                                               PAL04520
C                                                                       PAL04530
C*********************************************************************** PAL04540
C                                                                       PAL04550
C THIS  SUBROUTINE CALCULATES THE SUMCHECK                              PAL04560
      SUBROUTINE SUMCHK                                                 PAL04570
      IMPLICIT INTEGER (A-Z)                                            PAL04580
      LOGICAL LFUSES(32,64)                                             PAL04590
      INTEGER IPBUF(32), BUFIO(32)                                      PAL04600
      INTEGER ISUM(4),IDEC(4)                                           PAL04610
      COMMON /IPT/ IPT                                                  PAL04620
      COMMON /LFUSES/ LFUSES                                            PAL04630
      COMMON/SUM/ ISUM,IDEC,IPBUF,BUFIO                                 PAL04640
      DO 50 J=1,32                                                      PAL04650
      IF(LFUSES(J,IPT)) BUFIO(J)=49                                     PAL04660
      IF(.NOT.LFUSES(J,IPT)) BUFIO(J)=48                                PAL04670
      ISUM(4)=ISUM(4)+BUFIO(J)                                          PAL04680
      IF(ISUM(4).GE.256) ISUM(2)=ISUM(2)+1                              PAL04690
      ISUM(4)=MOD(ISUM(4),256)                                          PAL04700
   50 CONTINUE                                                          PAL04710
      DO 100 J=1,4                                                      PAL04720
      ISUM(4)=ISUM(4)+IDEC(J)+48                                        PAL04730
      IF(ISUM(4).GE.256) ISUM(2)=ISUM(2)+1                              PAL04740
      ISUM(4)=MOD(ISUM(4),256)                                          PAL04750
  100 CONTINUE                                                          PAL04760
      ISUM(4)=ISUM(4)+173                                               PAL04770
      ISUM(2)=ISUM(2)+1                                                 PAL04780
      IF(ISUM(4).GE.256) ISUM(2)=ISUM(2)+1                              PAL04790
      ISUM(4)=MOD(ISUM(4),256)                                          PAL04800
      RETURN                                                            PAL04810
      END                                                               PAL04820
C*************************************************                      PAL04830
C                                                                       PAL04840
C                                                                       PAL04850
      INTEGER FUNCTION ICONV(K)                                         PAL04860
      IMPLICIT INTEGER (A-Z)                                            PAL04870
      DATA A/'0'/,B/'1'/,C/'2'/,D/'3'/,E/'4'/,F/'5'/,G/'6'/,H/'7'/      PAL04880
      DATA I/'8'/,J/'9'/,X/'A'/,L/'B'/,M/'C'/,N/'D'/,O/'E'/,P/'F'/      PAL04890
      IF(K.EQ.0)  ICONV=A                                               PAL04900
      IF(K.EQ.1)  ICONV=B                                               PAL04910
      IF(K.EQ.2)  ICONV=C                                               PAL04920
      IF(K.EQ.3)  ICONV=D                                               PAL04930
      IF(K.EQ.4)  ICONV=E                                               PAL04940
      IF(K.EQ.5)  ICONV=F                                               PAL04950
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      IF(K.EQ.6) ICONV=G                                                    PAL04960
      IF(K.EQ.7) ICONV=H                                                    PAL04970
      IF(K.EQ.8) ICONV=I                                                    PAL04980
      IF(K.EQ.9) ICONV=J                                                    PAL04990
      IF(K.EQ.10)ICONV=X                                                    PAL05000
      IF(K.EQ.11)ICONV=L                                                    PAL05010
      IF(K.EQ.12)ICONV=M                                                    PAL05020
      IF(K.EQ.13)ICONV=N                                                    PAL05030
      IF(K.EQ.14)ICONV=O                                                    PAL05040
      IF(K.EQ.15)ICONV=P                                                    PAL05050
      RETURN                                                                PAL05060
      END                                                                   PAL05070
C                                                                           PAL05080
C                                                                           PAL05090
C*************************************************************************PAL05100
C                                                                           PAL05110
      SUBROUTINE INITLZ(INOAI,IOT,INOO,ITYPE,LFUSES,IC,IL,IBLOW,LFIX,       PAL05120
     1                  IPCTR)                                            PAL05130
C     THIS SUBROUTINE INITIALIZES VARIABLES AND MATCHES PAL PART            PAL05140
C     NUMBER WITH ITYPE                                                     PAL05150
      IMPLICIT INTEGER (A-Z)                                                PAL05160
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR,        PAL05170
     1        LFIX,LFUSES(32,64)                                            PAL05180
      COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR         PAL05190
      COMMON /PGE/ IPAGE(80,200)                                            PAL05200
      DATA H/'H'/,L/'L'/,C/'C'/,R/'R'/,X/'X'/,A/'A'/,                       PAL05210
     1     I0/'0'/,I2/'2'/,I4/'4'/,I6/'6'/,I8/'8'/                          PAL05220
C     INITIALIZE LFUSES ARRAY (FUSE ARRAY)                                  PAL05230
      DO 20 J=1,64                                                          PAL05240
         DO 20 I=1,32                                                       PAL05250
   20       LFUSES(I,J)=.FALSE.                                             PAL05260
C     INITIALIZE IBLOW (NUMBER OF FUSES BLOWN)                              PAL05270
      IBLOW=0                                                               PAL05280
C     INITIALIZE IPCTR (NUMBER OF PRODUCT TERMS)                            PAL05290
      IPCTR=0                                                               PAL05300
C     INITIALIZE IC AND IL (COLUMN AND LINE POINTERS)                       PAL05310
      IC=0                                                                  PAL05320
      IL=1                                                                  PAL05330
C     INITIALIZE ITYPE (PAL PART TYPE)                                      PAL05340
      ITYPE=0                                                               PAL05350
C     ITYPE IS ASSIGNED THE FOLLOWING VALUES FOR THESE PAL TYPES:           PAL05360
C          PAL10H8,PAL10L8                          ITYPE=1                 PAL05370
C          PAL12H6,PAL12L6                          ITYPE=2                 PAL05380
C          PAL14H4,PAL14L4                          ITYPE=3                 PAL05390
C          PAL16H2,PAL16L2,PAL16C1                  ITYPE=4                 PAL05400
C          PAL16L8                                  ITYPE=5                 PAL05410
C          PAL16R4,PAL16R6,PAL16R8,PAL16X4,PAL16A4  ITYPE=6                 PAL05420
C     DETERMINE ITYPE                                                       PAL05430
      IF(  INOAI.EQ.I0 )                            ITYPE=1                 PAL05440
      IF(  INOAI.EQ.I2 )                            ITYPE=2                 PAL05450
      IF(  INOAI.EQ.I4 )                            ITYPE=3                 PAL05460
      IF( (INOAI.EQ.I6) )                           ITYPE=4                 PAL05470
      IF( (INOAI.EQ.I6).AND.(INOO.EQ.I8) )          ITYPE=5                 PAL05480
      IF( (IOT.EQ.R).OR.(IOT.EQ.X).OR.(IOT.EQ.A) )  ITYPE=6                 PAL05490
      IF( .NOT.(IOT.EQ.H.OR.IOT.EQ.L.OR.IOT.EQ.C                            PAL05500
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

     1       .OR.IOT.EQ.R.OR.IOT.EQ.X.OR.IOT.EQ.A) ) ITYPE=0                PAL05510
      CALL INCR(IC,IL,LFIX)                                                 PAL05520
      RETURN                                                                PAL05530
      END                                                                   PAL05540
C                                                                           PAL05550
C*************************************************************************PAL05560
C                                                                           PAL05570
      SUBROUTINE GETSYM(LPHASE,ISYM,J,IC,IL,LFIX)                           PAL05580
C     THIS SUBROUTINE GETS THE PIN NAME, / IF COMPLEMENT LOGIC, AND         PAL05590
C      THE FOLLOWING OPERATION SYMBOL IF ANY                                PAL05600
      IMPLICIT INTEGER (A-Z)                                                PAL05610
      INTEGER ISYM(8,20)                                                    PAL05620
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR,        PAL05630
     1        LFIX,LPHASE(20)                                               PAL05640
      COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR         PAL05650
      COMMON /PGE/ IPAGE(80,200)                                            PAL05660
      DATA IBLANK/' '/                                                      PAL05670
      LFIX=.FALSE.                                                          PAL05680
      IF( .NOT.(LLEFT.OR.LAND.OR.LOR.OR.LEQUAL.OR.LRIGHT) ) GO TO 10        PAL05690
      CALL INCR(IC,IL,LFIX)                                                 PAL05700
      IF(LLEFT) GO TO 60                                                    PAL05710
   10 LPHASE(J)=( .NOT.LSLASH )                                             PAL05720
      IF(LPHASE(J)) GO TO 15                                                PAL05730
      CALL INCR(IC,IL,LFIX)                                                 PAL05740
   15 DO 20 I=1,8                                                           PAL05750
   20      ISYM(I,J)=IBLANK                                                 PAL05760
   25 DO 30 I=1,7                                                           PAL05770
   30      ISYM(I,J)=ISYM(I+1,J)                                            PAL05780
      ISYM(8,J)=IPAGE(IC,IL)                                                PAL05790
      CALL INCR(IC,IL,LFIX)                                                 PAL05800
      IF( LLEFT.OR.LBLANK.OR.LAND.OR.LOR.OR.LRIGHT.OR.LEQUAL ) RETURN       PAL05810
      GO TO 25                                                              PAL05820
   60 LFIX=.TRUE.                                                           PAL05830
      RETURN                                                                PAL05840
      END                                                                   PAL05850
C                                                                           PAL05860
C*************************************************************************PAL05870
C                                                                           PAL05880
      SUBROUTINE INCR(IC,IL,LFIX)                                           PAL05890
C     THIS SUBROUTINE INCREMENTS COLUMN AND LINE POINTERS                   PAL05900
C      BLANKS AND CHARACTERS AFTER ';' ARE IGNORED                          PAL05910
      IMPLICIT INTEGER (A-Z)                                                PAL05920
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR,        PAL05930
     1        LFIX,LX1                                                      PAL05940
      COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR         PAL05950
      COMMON /PGE/ IPAGE(80,200)                                            PAL05960
      COMMON /LUNIT/ PMS,POF,PDF                                            PAL05970
      DATA IBLANK/' '/,ILEFT/'('/,IAND/'*'/,IOR/'+'/,COMENT/';'/,           PAL05980
     1     ISLASH/'/'/,IEQUAL/'='/,IRIGHT/')'/,ICOLON/':'/                  PAL05990
      LBLANK=.FALSE.                                                        PAL06000
      LXOR=.FALSE.                                                          PAL06010
      LXNOR=.FALSE.                                                         PAL06020
      LX1=.FALSE.                                                           PAL06030
      LRIGHT=.FALSE.                                                        PAL06040
   10 IC=IC+1                                                               PAL06050
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      IF(IC .LE.79 .AND. IPAGE(IC,IL).NE.COMENT) GO TO 30                PAL06060
      IL=IL+1                                                            PAL06070
      IF(IL.LE.200) GO TO 20                                             PAL06080
          WRITE(PMS,15)                                                  PAL06090
   15     FORMAT(/,' SOURCE FILE EXCEEDS 200 LINES OR MISSING',          PAL06100
     1            ' DESCRIPTION OR FUNCTION TABLE KEY WORD')             PAL06110
          STOP                                                           PAL06120
   20 IC=0                                                               PAL06130
      GO TO 10                                                           PAL06140
   30 IF( IPAGE(IC,IL).EQ.ICOLON.AND.(LFIX) ) RETURN                     PAL06150
      IF( IPAGE(IC,IL).NE.IBLANK ) GO TO 31                              PAL06160
          LBLANK=.TRUE.                                                  PAL06170
          GO TO 10                                                       PAL06180
   31 IF( IPAGE(IC,IL).NE.ICOLON ) GO TO 32                              PAL06190
      IF( (LXOR).OR.(LXNOR) )  GO TO 33                                  PAL06200
      LX1=.TRUE.                                                         PAL06210
      GO TO 10                                                           PAL06220
   33 IF(LXOR)  LOR=.TRUE.                                               PAL06230
      IF(LXNOR) LAND=.TRUE.                                              PAL06240
      RETURN                                                             PAL06250
   32 IF( .NOT.(LX1.AND.(IPAGE(IC,IL).EQ.IOR.OR.IPAGE(IC,IL).EQ.IAND)) )PAL06260
     1     GO TO 34                                                      PAL06270
      IF( IPAGE(IC,IL).EQ.IOR  ) LXOR=.TRUE.                             PAL06280
      IF( IPAGE(IC,IL).EQ.IAND ) LXNOR=.TRUE.                            PAL06290
      GO TO 10                                                           PAL06300
   34 LLEFT =( IPAGE(IC,IL).EQ.ILEFT  )                                  PAL06310
      LAND  =( IPAGE(IC,IL).EQ.IAND   )                                  PAL06320
      LOR   =( IPAGE(IC,IL).EQ. IOR   )                                  PAL06330
      LSLASH=( IPAGE(IC,IL).EQ.ISLASH )                                  PAL06340
      LEQUAL=( IPAGE(IC,IL).EQ.IEQUAL )                                  PAL06350
      LRIGHT=( IPAGE(IC,IL).EQ.IRIGHT )                                  PAL06360
      RETURN                                                             PAL06370
      END                                                                PAL06380
C                                                                        PAL06390
C*************************************************************************PAL06400
C                                                                        PAL06410
      SUBROUTINE MATCH(IMATCH,IBUF,ISYM)                                 PAL06420
C     THIS SUBROUTINE FINDS A MATCH BETWEEN THE PIN NAME IN THE EQUATIONPAL06430
C      AND THE PIN NAME IN THE PIN LIST OR FUNCTION TABLE PIN LIST       PAL06440
      IMPLICIT INTEGER (A-Z)                                             PAL06450
      INTEGER IBUF(8,20),ISYM(8,20)                                      PAL06460
      LOGICAL LMATCH                                                     PAL06470
      DATA C/'C'/,A/'A'/,R/'R'/,Y/'Y'/                                   PAL06480
      IMATCH=0                                                           PAL06490
      DO 20 J=1,20                                                       PAL06500
          LMATCH=.TRUE.                                                  PAL06510
          DO 10 I=1,8                                                    PAL06520
   10         LMATCH=LMATCH.AND.(IBUF(I,1).EQ.ISYM(I,J))                 PAL06530
          IF(LMATCH) IMATCH=J                                            PAL06540
   20     CONTINUE                                                       PAL06550
C     MATCH CARRY WHICH IS FOUND IN THE PAL16A4                          PAL06560
      IF( IBUF(3,1).EQ.C.AND.IBUF(4,1).EQ.A.AND.IBUF(5,1).EQ.R.AND.      PAL06570
     1    IBUF(6,1).EQ.R.AND.IBUF(7,1).EQ.Y ) IMATCH=99                  PAL06580
      RETURN                                                             PAL06590
      END                                                                PAL06600
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0


C                                                                               PAL06610
C*******************************************************************************PAL06620
C                                                                               PAL06630
      SUBROUTINE IXLATE(IINPUT,IMATCH,LPHASE,LBUF,ITYPE)                        PAL06640
C     THIS SUBROUTINE FINDS A MATCH BETWEEN THE INPUT PIN NUMBER AND            PAL06650
C      THE INPUT LINE NUMBER FOR A SPECIFIC PAL.  ADD 1 TO THE INPUT            PAL06660
C      LINE NUMBER IF THE PIN IS A COMPLEMENT                                   PAL06670
      IMPLICIT INTEGER (A-Z)                                                    PAL06680
      INTEGER ITABLE(20,6)                                                      PAL06690
      LOGICAL LPHASE(20),LBUF(20)                                               PAL06700
      DATA    ITABLE/                                                           PAL06710
     1   3, 1, 5, 9,13,17,21,25,29,-10,31,-1,-1,-1,-1,-1,-1,-1,-20,            PAL06720
     2   3, 1, 5, 9,13,17,21,25,29,-10,31,27,-1,-1,-1,-1,-1, 7,-20,            PAL06730
     3   3, 1, 5, 9,13,17,21,25,29,-10,31,27,23,-1,-1,-1,-1,11, 7,-20,         PAL06740
     4   3, 1, 5, 9,13,17,21,25,29,-10,31,27,23,19,-1,-1,15,11, 7,-20,         PAL06750
     5   3, 1, 5, 9,13,17,21,25,29,-10,31,-1,27,23,19,15,11, 7,-1,-20,         PAL06760
     6  -1, 1, 5, 9,13,17,21,25,29,-10,-1,31,27,23,19,15,11, 7, 3,-20/         PAL06770
      IINPUT=0                                                                  PAL06780
      IBUBL=0                                                                   PAL06790
      IF(((     LPHASE(IMATCH)).AND.(.NOT.LBUF(1))).OR.                         PAL06800
     1   ((.NOT.LPHASE(IMATCH)).AND.(     LBUF(1)))) IBUBL=1                   PAL06810
      IF( ITABLE(IMATCH,ITYPE).GT.0 ) IINPUT=ITABLE(IMATCH,ITYPE)+IBUBL         PAL06820
      RETURN                                                                    PAL06830
      END                                                                       PAL06840
C                                                                               PAL06850
C*******************************************************************************PAL06860
C                                                                               PAL06870
      SUBROUTINE FIXSYM(LBUF,IBUF,IC,IL,LFIRST,LFUSES,IBLOW,IPROD,LFIX)         PAL06880
C     THIS SUBROUTINE EVALUATES THE FIXED SYMBOLS FOUND IN THE                  PAL06890
C      PAL16X4 AND PAL16A4                                                      PAL06900
      IMPLICIT INTEGER (A-Z)                                                    PAL06910
      LOGICAL LBUF(20),LFUSES(32,64),LFIRST,LMATCH,LFIX                         PAL06920
      INTEGER IBUF(8,20),FIXBUF(8),TABLE(5,14)                                  PAL06930
      COMMON /PGE/ IPAGE(80,200)                                                PAL06940
      DATA A/'A'/,B/'B'/,ISLASH/'/'/,IOR/'+'/,IBLANK/' '/,IRIGHT/')'/,          PAL06950
     1        IAND/'*'/,N/'N'/,Q/'Q'/,NO/'0'/,N1/'1'/,N2/'2'/,N3/'3'/,          PAL06960
     2       ICOLON/':'/,                                                       PAL06970
     3        TABLE      /      ' ','A',' ','/','B',' ',' ','A',' ','B',PAL06980
     4       ' ',' ',' ',' ','A','/','A',' ','/','B',' ',' ',' ',' ','/','B',PAL06990
     5       'A',':',' ','B',' ','A','*','/','B',' ',' ','/','A',' ','B',PAL07000
     6       'A',':',' ','*',':','B',' ',' ',' ',' ','B',' ',' ',' ','A',' ','*','B',PAL07010
     7       ' ',' ',' ','/','A','/','A','*','/','B',' ','/','A','*','B'/PAL07020
      IINPUT=0                                                                  PAL07030
      DO 20 I=1,6                                                               PAL07040
         IBUF(I,1)=IBLANK                                                       PAL07050
   20    FIXBUF(I)=IBLANK                                                       PAL07060
   21 CALL INCR(IC,IL,LFIX)                                                     PAL07070
      I=IPAGE(IC,IL)                                                            PAL07080
      IF(I.EQ.IRIGHT) GO TO 40                                                  PAL07090
      IF(I.EQ.NO) IINPUT=8                                                      PAL07100
      IF(I.EQ.N1) IINPUT=12                                                     PAL07110
      IF(I.EQ.N2) IINPUT=16                                                     PAL07120
      IF(I.EQ.N3) IINPUT=20                                                     PAL07130
      DO 24 J=1,7                                                               PAL07140
   24    IBUF(J,1)=IBUF(J+1,1)                                                  PAL07150
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      IBUF(8,1)=I                                                        PAL07160
      IF(.NOT. ( (I.EQ.A).OR.(I.EQ.B).OR.(I.EQ.ISLASH).OR.(I.EQ.IOR)     PAL07170
     1       .OR.(I.EQ.IAND).OR.(I.EQ.ICOLON) ) )  GO TO 21              PAL07180
      DO 30 I=1,4                                                        PAL07190
   30     FIXBUF(I)=FIXBUF(I+1)                                          PAL07200
      FIXBUF(5)=IPAGE(IC,IL)                                             PAL07210
      GO TO 21                                                           PAL07220
   40 IMATCH=0                                                           PAL07230
      DO 60 J=1,14                                                       PAL07240
         LMATCH=.TRUE.                                                   PAL07250
         DO 50 I=1,5                                                     PAL07260
   50       LMATCH=LMATCH .AND. ( FIXBUF(I).EQ.TABLE(I,J) )             PAL07270
   60    IF(LMATCH) IMATCH=J                                            PAL07280
      IF(IMATCH.EQ.0) GO TO 100                                          PAL07290
      IF(.NOT.LFIRST) GO TO 85                                           PAL07300
         LFIRST=.FALSE.                                                  PAL07310
         DO 80 I=1,32                                                    PAL07320
            LFUSES(I,IPROD)=.TRUE.                                       PAL07330
   80       IBLOW = IBLOW + 1                                           PAL07340
   85 DO 90 I=1,4                                                        PAL07350
         IF( (IMATCH-7).LE.0 ) GO TO 90                                  PAL07360
         ISUM1=11NPUT+I                                                  PAL07370
         LFUSES(ISUM1,IPROD)=.FALSE.                                     PAL07380
         IBLOW = IBLOW - 1                                               PAL07390
         IMATCH=IMATCH-8                                                 PAL07400
   90 IMATCH=IMATCH+IMATCH                                               PAL07410
      LBUF(1)=.TRUE.                                                     PAL07420
      CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.FALSE.,ITYPE,              PAL07430
     1          LPROD,IOP,IBLOW,IPCTR)                                   PAL07440
  100 LFIX=.FALSE.                                                       PAL07450
      CALL INCR(IC,IL,LFIX)                                              PAL07460
      RETURN                                                             PAL07470
      END                                                                PAL07480
C                                                                        PAL07490
C************************************************************************PAL07500
C                                                                        PAL07510
      SUBROUTINE ECHO(IPAL,INOAI,IOT,INOO,REST,PATNUM,TITLE,COMP)        PAL07520
C     THIS SUBROUTINE PRINTS THE PAL DESIGN SPECIFICATION INPUT FILE     PAL07530
      IMPLICIT INTEGER (A-Z)                                             PAL07540
      INTEGER IPAL(4),REST(73),PATNUM(60),TITLE(80),COMP(80)             PAL07550
      COMMON /PGE/ IPAGE(80,200)                                         PAL07560
      COMMON /LUNIT/ PMS,POF,PDF                                         PAL07570
      COMMON /TTEST/ IFUNCT,IDESC,IEND                                   PAL07580
      DATA IBLANK/' '/                                                   PAL07590
      WRITE(POF,5) IPAL,INOAI,IOT,INOO,REST,PATNUM,TITLE,COMP            PAL07600
    5 FORMAT(/,' ',4A1,A1,A1,A1,73A1,/,' ',80A1,/,' ',80A1,/,' ',80A1)   PAL07610
      DO 20 IL=1,IEND                                                    PAL07620
         IC=81                                                           PAL07630
   10    IC=IC-1                                                        PAL07640
         IF( IPAGE(IC,IL).EQ.IBLANK.AND.IC.GT.1 ) GO TO 10               PAL07650
         WRITE(POF,15) (IPAGE(I,IL),I=1,IC)                              PAL07660
   15    FORMAT(' ',80A1)                                               PAL07670
   20 CONTINUE                                                           PAL07680
      RETURN                                                             PAL07690
      END                                                                PAL07700
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0


C                                                                              PAL07710
C*******************************************************************************PAL07720
C                                                                              PAL07730
      SUBROUTINE CAT                                                           PAL07740
C     THIS SUBROUTINE PRINTS THE PALASM CATOLOG                                PAL07750
      IMPLICIT INTEGER (A-Z)                                                   PAL07760
      COMMON /LUNIT/ PMS,POF,PDF                                               PAL07770
      WRITE(PMS,10)                                                            PAL07780
   10 FORMAT(/,' THIS PALASM AIDS THE USER IN THE DESIGN AND',                 PAL07790
     1          ' PROGRAMMING OF THE',/,' SERIES 20 PAL FAMILY.  THE',        PAL07800
     2          ' FOLLOWING OPTIONS ARE PROVIDED:',                           PAL07810
     3       //,'    ECHO (E)      - PRINTS THE PAL DESIGN',                  PAL07820
     4          ' SPECIFICATION',                                             PAL07830
     5       //,'    PINOUT (O)    - PRINTS THE PINOUT OF THE PAL',           PAL07840
     6       //,'    SIMULATE (T) - EXERCISES THE FUNCTION TABLE',            PAL07850
     7          ' VECTORS IN THE LOGIC',/,'                    ',            PAL07860
     8          ' EQUATIONS AND GENERATES TEST VECTORS',                      PAL07870
     9       //,'    PLOT (P)      - PRINTS THE ENTIRE FUSE PLOT')            PAL07880
      WRITE(PMS,20)                                                            PAL07890
   20 FORMAT(/,'    BRIEF (B)     - PRINTS ONLY THE USED PRODUCT LINES',       PAL07900
     1          ' OF THE FUSE PLOT',/,'                      PHANTOM',       PAL07910
     2          ' FUSES ARE OMITTED',                                         PAL07920
     3       //,'    HEX (H)       - GENERATES HEX PROGRAMMING FORMAT',       PAL07930
     4       //,'    SHORT (S)     - GENERATES HEX PROGRAMMING FORMAT',       PAL07940
     5       //,'    BHLF (L)      - GENERATES BHLF PROGRAMMING FORMAT',      PAL07950
     6       //,'    BNPF (N)      - GENERATES BNPF PROGRAMMING FORMAT',      PAL07960
     7       //,'    CATALOG (C)   - PRINTS THE PALASM CATALOG',              PAL07970
     8       //,'    QUIT (Q)      - EXIT PALASM',                            PAL07980
     9       //,'    JEDEC (Y)     - JEDEC FORMAT FOR DATA I/O PROGRAMMER'    PAL07990
     A       //,'    FAULT (F)     - FAULT TESTING ')                         PAL08000
      RETURN                                                                   PAL08010
      END                                                                      PAL08020
C                                                                              PAL08030
C*******************************************************************************PAL08040
C                                                                              PAL08050
      SUBROUTINE PINOUT(IPAL,INOAI,IOT,INOO,TITLE)                             PAL08060
C     THIS SUBROUTINE PRINTS THE PINOUT OF THE PAL                             PAL08070
      IMPLICIT INTEGER (A-Z)                                                   PAL08080
      INTEGER IPAL(4),TITLE(80),PIN(12,20),IIN(7,2)                            PAL08090
      COMMON /PGE/ IPAGE(80,200)                                               PAL08100
      COMMON /LUNIT/ PMS,POF,PDF                                               PAL08110
      DATA IBLANK/' '/,ISTAR/'*'/                                              PAL08120
      DO 10 J=1,20                                                             PAL08130
          DO 5 I=1,12                                                          PAL08140
    5        PIN(I,J)=IBLANK                                                   PAL08150
   10 CONTINUE                                                                 PAL08160
   15 DO 25 J=1,2                                                              PAL08170
          DO 20 I=1,7                                                          PAL08180
   20        IIN(I,J)=IBLANK                                                   PAL08190
   25 CONTINUE                                                                 PAL08200
      IIN(2,1)=IPAL(1)                                                         PAL08210
      IIN(4,1)=IPAL(2)                                                         PAL08220
      IIN(6,1)=IPAL(3)                                                         PAL08230
      IIN(1,2)=IPAL(4)                                                         PAL08240
      IIN(3,2)=INOAI                                                           PAL08250
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      IIN(5,2)=IOT                                                          PAL08260
      IIN(7,2)=INOO                                                         PAL08270
      J=0                                                                   PAL08280
      IL=0                                                                  PAL08290
   30 IC=0                                                                  PAL08300
      IL=IL+1                                                               PAL08310
   35 IC=IC+1                                                               PAL08320
   40 IF( IC.GT.80 ) GO TO 30                                               PAL08330
      IF( IPAGE(IC,IL).EQ.IBLANK ) GO TO 35                                 PAL08340
      J=J+1                                                                 PAL08350
      IF(J.GT.20) GO TO 60                                                  PAL08360
      DO 55 I=1,12                                                          PAL08370
           PIN(I,J)=IPAGE(IC,IL)                                            PAL08380
           IC=IC+1                                                          PAL08390
           IF( IC.GT.80 ) GO TO 40                                          PAL08400
           IF( IPAGE(IC,IL).EQ.IBLANK ) GO TO 40                            PAL08410
   55 CONTINUE                                                              PAL08420
   60 DO 75 J=1,10                                                          PAL08430
           II=0                                                             PAL08440
   65      II=II+1                                                          PAL08450
           IF(II.EQ.13) GO TO 75                                            PAL08460
           IF( PIN(II,J).NE.IBLANK ) GO TO 65                               PAL08470
           I=13                                                             PAL08480
   70      I=I-1                                                            PAL08490
           II=II-1                                                          PAL08500
           PIN(I,J)=PIN(II,J)                                               PAL08510
           PIN(II,J)=IBLANK                                                 PAL08520
           IF(II.NE.1) GO TO 70                                             PAL08530
   75 CONTINUE                                                              PAL08540
      WRITE(POF,76) TITLE                                                   PAL08550
   76 FORMAT(/,' ',80A1)                                                    PAL08560
      WRITE(POF,78) ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,       PAL08570
     1              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,       PAL08580
     2              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,       PAL08590
     3              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR        PAL08600
   78 FORMAT(/,' ',18X,14A1,3X,14A1,                                        PAL08610
     1       /,' ',18X,A1,13X,A1,1X,A1,13X,A1)                              PAL08620
      JJ=20                                                                 PAL08630
      DO 88 J=1,10                                                          PAL08640
           WRITE(POF,80) ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR    PAL08650
   80      FORMAT(' ',15X,4A1,29X,4A1)                                      PAL08660
           WRITE(POF,81) (PIN(I,J),I=1,12),ISTAR,J,ISTAR,                   PAL08670
     1          (IIN(I,1),I=1,7),ISTAR,JJ,ISTAR,(PIN(I,JJ),I=1,12)         PAL08680
   81      FORMAT(' ',12A1,3X,A1,I2,A1,11X,7A1,11X,A1,I2,A1,3X,12A1)        PAL08690
           WRITE(POF,82) ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR    PAL08700
   82      FORMAT(' ',15X,4A1,29X,4A1)                                      PAL08710
           WRITE(POF,84) ISTAR,(IIN(I,2),I=1,7),ISTAR                       PAL08720
   84      FORMAT(' ',18X,A1,11X,7A1,11X,A1)                                PAL08730
           DO 86 II=1,2                                                     PAL08740
                DO 85 I=1,7                                                 PAL08750
   85                IIN(I,II)=IBLANK                                      PAL08760
   86      CONTINUE                                                         PAL08770
           JJ=JJ-1                                                          PAL08780
   88 CONTINUE                                                              PAL08790
      WRITE(POF,90) ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,       PAL08800
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

     1              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,     PAL08810
     2              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,     PAL08820
     3              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR            PAL08830
  90 FORMAT(' ',18X,31A1)                                                PAL08840
     RETURN                                                              PAL08850
     END                                                                 PAL08860
C                                                                        PAL08870
C*******************************************************************************PAL08880
C                                                                        PAL08890
     SUBROUTINE PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,LDUMP,ITYPE,           PAL08900
     1               LPROD,IOP,IBLOW,IPCTR0)                             PAL08910
C    THIS THIS SUBROUTINE PRODUCES THE FUSE PLOT                         PAL08920
     IMPLICIT INTEGER (A-Z)                                              PAL08930
     INTEGER IBUF(8,20),IOUT(64),ISAVE(64,32),TITLE(80)                  PAL08940
     LOGICAL LBUF(20),LFUSES(32,64),LDUMP,LPROD(80)                      PAL08950
     COMMON /LUNIT/ PMS,POF,PDF                                          PAL08960
     DATA ISAVE/2048*' '/,IAND/'*'/,IOR/'+'/,ISLASH/'/'/,                PAL08970
    1     IDASH/'-'/,X/'X'/,IBLANK/' '/,P/'P'/,B/'B'/,                   PAL08980
    2     MIFANT/'0'/                                                    PAL08990
     IF(LDUMP) GO TO 60                                                  PAL09000
     IF(ISAVE(IPROD,1).NE.IBLANK) RETURN                                 PAL09010
     IF( LBUF(1) ) GO TO 5                                               PAL09020
     DO 30 J=1,31                                                        PAL09030
  30     ISAVE(IPROD,J)=ISAVE(IPROD,J+1)                                 PAL09040
     ISAVE(IPROD,32)=ISLASH                                              PAL09050
   5 DO 20 I=1,8                                                         PAL09060
         IF( ISAVE(IPROD,1).NE.IBLANK ) RETURN                           PAL09070
         IF( IBUF(I,1).EQ.IBLANK ) GO TO 20                              PAL09080
         DO 10 J=1,31                                                    PAL09090
  10         ISAVE(IPROD,J)=ISAVE(IPROD,J+1)                             PAL09100
        ISAVE(IPROD,32)=IBUF(I,1)                                        PAL09110
  20     CONTINUE                                                        PAL09120
     IF(ISAVE(IPROD,1).NE.IBLANK) RETURN                                 PAL09130
  40 DO 50 J=1,31                                                        PAL09140
  50     ISAVE(IPROD,J)=ISAVE(IPROD,J+1)                                 PAL09150
     ISAVE(IPROD,32)=IAND                                                PAL09160
     RETURN                                                              PAL09170
C    PRINT FUSE PLOT                                                     PAL09180
  60 WRITE(POF,62) TITLE                                                 PAL09190
  62 FORMAT(/,' ',80A1,//,                                               PAL09200
    1 '                 11 1111 1111 2222 2222 2233',/,                  PAL09210
    2 '     0123 4567 8901 2345 6789 0123 4567 8901',/)                  PAL09220
     DO 100 I88PRO=1,57,8                                                PAL09230
         DO 94 I8PRO=1,8                                                 PAL09240
             IPROD=I88PRO+I8PRO-1                                        PAL09250
             ISAVE(IPROD,32)=IBLANK                                      PAL09260
             DO 70 I=1,32                                                PAL09270
                 IF( ISAVE(IPROD,1).NE.IBLANK ) GO TO 70                 PAL09280
                 DO 65 J=1,31                                            PAL09290
                     ISAVE(IPROD,J)=ISAVE(IPROD,J+1)                     PAL09300
  65                 CONTINUE                                            PAL09310
                 ISAVE(IPROD,32)=IBLANK                                  PAL09320
  70         CONTINUE                                                    PAL09330
             DO 80 I=1,32                                                PAL09340
                 IOUT(I)=X                                               PAL09350
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

                    IF( LFUSES(I,IPROD) ) IOUT(I)=IDASH                    PAL09360
                    IOUT(I+32)=ISAVE(IPROD,I)                              PAL09370
   80           CONTINUE                                                   PAL09380
                IF(ITYPE.LE.4) CALL FANTOM(ITYPE,IOUT,IPROD,IBPRO)         PAL09390
                IPROD=IPROD-1                                              PAL09400
                DO 85 J=1,32                                               PAL09410
                    IF( IOP.EQ.B.AND.IOUT(J).EQ.HIFANT ) IOUT(J)=IBLANK    PAL09420
   85           CONTINUE                                                   PAL09430
                IF( (IOP.EQ.P).OR.(IOP.EQ.B.AND.(LPROD(IPROD+1))) )        PAL09440
     1          WRITE(POF,90) IPROD,IOUT                                   PAL09450
   90           FORMAT(' ',I2,8(' ',4A1),' ',32A1)                         PAL09460
   94           CONTINUE                                                   PAL09470
            WRITE(POF,96)                                                  PAL09480
   96       FORMAT(1X)                                                     PAL09490
  100       CONTINUE                                                       PAL09500
        WRITE(POF,110)                                                     PAL09510
  110 FORMAT(/,                                                            PAL09520
     1' LEGEND:  X : FUSE NOT BLOWN (L,N,O)    - : FUSE BLOWN    (H,P,I)')PAL09530
        IF( IOP.EQ.P.AND.ITYPE.LE.4 ) WRITE(POF,111)                       PAL09540
  111 FORMAT(                                                              PAL09550
     1'           O : PHANTOM FUSE    (L,N,O)    O : PHANTOM FUSE (H,P,I)')PAL09560
        WRITE(POF,112) IBLOW                                               PAL09570
  112 FORMAT(/,' NUMBER OF FUSES BLOWN = ',I4)                             PAL09580
        RETURN                                                             PAL09590
        END                                                                PAL09600
C                                                                          PAL09610
C*************************************************************************PAL09620
C                                                                          PAL09630
      SUBROUTINE HEX(LFUSES,IOP)                                           PAL09640
C     THIS SUBROUTINE GENERATES HEX PROGRAMMING FORMATS                    PAL09650
      IMPLICIT INTEGER (A-Z)                                               PAL09660
      INTEGER ITABLE(16),ITEMP(64),ZCSUM(4)                                PAL09670
      LOGICAL LFUSES(32,64)                                                PAL09680
      INTEGER   SOH,STX,ETX,BEL                                            PAL09690
      COMMON /LUNIT/ PMS,POF,PDF                                           PAL09700
      DATA H/'H'/,S/'S'/,IBLANK/' '/,                                      PAL09710
     1    ITABLE/'0','1','2','3','4','5','6','7',                         PAL09720
     2           '8','9','A','B','C','D','E','F'/                         PAL09730
      DATA SOH /Z01000000/ , STX /Z02000000/ ,                             PAL09740
     +          ETX/Z03000000/ , BEL /Z07000000/                           PAL09750
      CSUM=0                                                               PAL09760
      IF(IOP.EQ.H) WRITE(PDF,10)                                           PAL09770
   10 FORMAT(//,'                                          .',//)          PAL09780
C***** NOTE: SOME PROM PROGRAMMERS NEED A START CHARACTER.                 PAL09790
C*****       THIS PROGRAM OUTPUTS AN STX FOR THE DATA I/O MODEL 9          PAL09800
C*****         (USE SOH FOR MODEL 5)                                       PAL09810
      WRITE(PDF,5) BEL,BEL,BEL,BEL,BEL,BEL,BEL,STX,SOH                     PAL09820
    5 FORMAT(' ',9A1)                                                      PAL09830
      DO 40 I=1,33,32                                                      PAL09840
      INC=I-1                                                              PAL09850
        DO 40 IPROD=1,7,2                                                  PAL09860
          DO 20 J=1,2                                                      PAL09870
              DO 20 IINPUT=1,32                                            PAL09880
              IHEX=0                                                       PAL09890
              ISUM2=IPROD + J-1 + INC                                      PAL09900
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

               IF(LFUSES(IINPUT,ISUM2 + 0 )) IHEX=IHEX+1                PAL09910
               IF(LFUSES(IINPUT,ISUM2 + 8 )) IHEX=IHEX+2                PAL09920
               IF(LFUSES(IINPUT,ISUM2 + 16 )) IHEX=IHEX+4               PAL09930
               IF(LFUSES(IINPUT,ISUM2 + 24 )) IHEX=IHEX+8               PAL09940
               CSUM=CSUM+IHEX                                           PAL09950
               ISUMX=IINPUT+(32*(J-1))                                  PAL09960
   20          ITEMP(ISUMX)=ZTABLE(IHEX+1)                              PAL09970
           IF(IOP.EQ.H) WRITE(PDF,30) ITEMP                             PAL09980
   30      FORMAT(' ',32(A1,' '),'.',/,' ',32(A1,' '),'.')              PAL09990
   40      IF(IOP.EQ.S) WRITE(PDF,50) ITEMP                             PAL10000
   50      FORMAT(' ',64A1)                                             PAL10010
           IF(IOP.EQ.H) WRITE(PDF,70)                                   PAL10020
   70 FORMAT(' ',//,'                                          .',//)   PAL10030
           WRITE(PDF,80) ETX                                            PAL10040
   80 FORMAT(' ',A1)                                                    PAL10050
C      CONVERT DECIMAL CHECK SUM INTO HEX CHECK SUM                     PAL10060
       DO 85 I=1,4                                                      PAL10070
            ZTEMP=CSUM-16*(CSUM/16)                                     PAL10080
            ZCSUM(5-I)=ZTABLE(ZTEMP+1)                                  PAL10090
            CSUM=CSUM/16                                                PAL10100
   85  CONTINUE                                                         PAL10110
       IF(ZCSUM(1).EQ.ZTABLE(1)) ZCSUM(1)=IBLANK                        PAL10120
       WRITE(PMS,90) ZCSUM(1),ZCSUM(2),ZCSUM(3),ZCSUM(4)                PAL10130
   90  FORMAT(/' HEX CHECK SUM = ',4A1)                                 PAL10140
       RETURN                                                           PAL10150
       END                                                              PAL10160
C                                                                       PAL10170
C***********************************************************************PAL10180
C                                                                       PAL10190
       SUBROUTINE TWEEK(ITYPE,IOT,LFUSES)                               PAL10200
C      THIS SUBROUTINE TWEEKS LFUSES (THE PROGRAMMING FUSE PLOT)        PAL10210
C       FOR HIGH AND LOW PHANTOM FUSES                                  PAL10220
       IMPLICIT INTEGER (A-Z)                                           PAL10230
       LOGICAL LFUSES(32,64)                                            PAL10240
       DATA L/'L'/,C/'C'/                                               PAL10250
       IF(ITYPE.GE.4) GO TO 20                                          PAL10260
       DO 10 IPROD=1,64                                                 PAL10270
            LFUSES(15,IPROD)=.TRUE.                                     PAL10280
            LFUSES(16,IPROD)=.TRUE.                                     PAL10290
            LFUSES(19,IPROD)=.TRUE.                                     PAL10300
            LFUSES(20,IPROD)=.TRUE.                                     PAL10310
            IF(ITYPE.GE.3) GO TO 10                                     PAL10320
            LFUSES(11,IPROD)=.TRUE.                                     PAL10330
            LFUSES(12,IPROD)=.TRUE.                                     PAL10340
            LFUSES(23,IPROD)=.TRUE.                                     PAL10350
            LFUSES(24,IPROD)=.TRUE.                                     PAL10360
            IF(ITYPE.GE.2) GO TO 10                                     PAL10370
            LFUSES( 7,IPROD)=.TRUE.                                     PAL10380
            LFUSES( 8,IPROD)=.TRUE.                                     PAL10390
            LFUSES(27,IPROD)=.TRUE.                                     PAL10400
            LFUSES(28,IPROD)=.TRUE.                                     PAL10410
   10       CONTINUE                                                    PAL10420
       DO 18 IINPUT=7,28                                                PAL10430
            DO 12 IPROD=1,57,8                                          PAL10440
                 LFUSES(IINPUT,IPROD+4)=.FALSE.                         PAL10450
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

                LFUSES(IINPUT,IPROD+5)=.FALSE.                                  PAL10460
                LFUSES(IINPUT,IPROD+6)=.FALSE.                                  PAL10470
   12           LFUSES(IINPUT,IPROD+7)=.FALSE.                                  PAL10480
           IF(ITYPE.GE.3) GO TO 18                                              PAL10490
           DO 14 IPROD=17,41,8                                                  PAL10500
                LFUSES(IINPUT,IPROD+2)=.FALSE.                                  PAL10510
   14           LFUSES(IINPUT,IPROD+3)=.FALSE.                                  PAL10520
           IF(ITYPE.GE.2) GO TO 16                                              PAL10530
           DO 16 IPROD=1,57,8                                                   PAL10540
                LFUSES(IINPUT,IPROD+2)=.FALSE.                                  PAL10550
   16           LFUSES(IINPUT,IPROD+3)=.FALSE.                                  PAL10560
   18 CONTINUE                                                                  PAL10570
   20 IF( (ITYPE.EQ.1) .OR. ((ITYPE.EQ.4).AND.(IOT.EQ.L)) ) RETURN              PAL10580
      DO 99 IINPUT=1,32                                                         PAL10590
           DO 30 IPROD=1,8                                                      PAL10600
                LFUSES(IINPUT,IPROD+ 0)= (IOT.NE.L)                             PAL10610
   30           IF(IOT.NE.C) LFUSES(IINPUT,IPROD+56)= (IOT.NE.L)                PAL10620
           IF(ITYPE.LE.2) GO TO 99                                              PAL10630
           DO 40 IPROD=1,8                                                      PAL10640
                LFUSES(IINPUT,IPROD+ 8)= (IOT.NE.L)                             PAL10650
   40           IF(IOT.NE.C) LFUSES(IINPUT,IPROD+48)= (IOT.NE.L)                PAL10660
           IF(ITYPE.LE.3) GO TO 99                                              PAL10670
           DO 50 IPROD=1,8                                                      PAL10680
                LFUSES(IINPUT,IPROD+16)= (IOT.NE.L)                             PAL10690
   50           IF(IOT.NE.C) LFUSES(IINPUT,IPROD+40)= (IOT.NE.L)                PAL10700
   99      CONTINUE                                                             PAL10710
      RETURN                                                                    PAL10720
      END                                                                       PAL10730
C                                                                               PAL10740
C*******************************************************************************PAL10750
C                                                                               PAL10760
      SUBROUTINE BINR(LFUSES,H,L)                                               PAL10770
C     THIS SUBROUTINE GENERATES BINARY PROGRAMMING FORMATS                      PAL10780
      IMPLICIT INTEGER (A-Z)                                                    PAL10790
      INTEGER ITEMP(4,8)                                                        PAL10800
      LOGICAL LFUSES(32,64)                                                     PAL10810
      COMMON /LUNIT/ PMS,POF,PDF                                                PAL10820
      WRITE(POF,10)                                                             PAL10830
   10 FORMAT(//,'                                        .',//)                 PAL10840
      DO 20 I=1,33,32                                                           PAL10850
      INC=I-1                                                                   PAL10860
        DO 20 IPROD=1,8                                                         PAL10870
           DO 20 J=1,25,8                                                       PAL10880
             DO 15 K=1,8                                                        PAL10890
               IINPUT=J+K-1                                                     PAL10900
               ITEMP(1,K)=L                                                     PAL10910
               ITEMP(2,K)=L                                                     PAL10920
               ITEMP(3,K)=L                                                     PAL10930
               ITEMP(4,K)=L                                                     PAL10940
               ISUM3=IPROD+INC                                                  PAL10950
               IF(LFUSES(IINPUT,ISUM3 +  0 )) ITEMP(4,K)=H                      PAL10960
               IF(LFUSES(IINPUT,ISUM3 +  8 )) ITEMP(3,K)=H                      PAL10970
               IF(LFUSES(IINPUT,ISUM3 + 16 )) ITEMP(2,K)=H                      PAL10980
               IF(LFUSES(IINPUT,ISUM3 + 24 )) ITEMP(1,K)=H                      PAL10990
   15          CONTINUE                                                         PAL11000
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0


   20          WRITE(PDF,30) ITEMP                                          PAL11010
   30          FORMAT(' ',8('B',4A1,'F '))                                  PAL11020
      WRITE(PDF,10)                                                         PAL11030
      RETURN                                                                PAL11040
      END                                                                   PAL11050
C                                                                           PAL11060
C*************************************************************************PAL11070
C                                                                           PAL11080
      SUBROUTINE SLIP(LFUSES,I88PRO,INOAI,IOT,INOO,IBLOW)                   PAL11090
C     THIS SUBROUTINE WILL BLOW THE ENTIRE CONDITIONAL THREE-STATE          PAL11100
C      PRODUCT LINE WHEN 'IF(VCC)' CONDITION IS USED FOR THE                PAL11110
C      CORRESPONDING OUTPUT PIN                                             PAL11120
      IMPLICIT INTEGER (A-Z)                                                PAL11130
      LOGICAL LFUSES(32,64)                                                 PAL11140
      DATA R/'R'/,I1/'1'/,I2/'2'/,I4/'4'/,I6/'6'/,I8/'8'/                   PAL11150
      IF( (INOAI.NE.I6) .OR. (INOO.EQ.I1) .OR.  (INOO.EQ.I2) .OR.          PAL11160
     1     ( (IOT.EQ.R).AND.(INOO.EQ.I8) ) .OR.                           PAL11170
     2     ( (I88PRO.GE. 9).AND.(I88PRO.LE.49).AND.(INOO.EQ.I6) ) .OR.    PAL11180
     3     ( (I88PRO.GE.17).AND.(I88PRO.LE.41).AND.(INOO.EQ.I4)) ) RETURNPAL11190
      DO 10 I=1,32                                                          PAL11200
      IBLOW = IBLOW + 1                                                     PAL11210
   10 LFUSES(I,I88PRO) = .TRUE.                                             PAL11220
      I88PRO = I88PRO + 1                                                   PAL11230
      RETURN                                                                PAL11240
      END                                                                   PAL11250
C                                                                           PAL11260
C*************************************************************************PAL11270
C                                                                           PAL11280
      SUBROUTINE FANTOM(ITYPE,IOUT,IPROD,I8PRO)                             PAL11290
C     THIS SUBROUTINE UPDATES IOUT (THE PRINTED FUSE PLOT)                  PAL11300
C      FOR HIGH AND LOW PHANTOM FUSES                                       PAL11310
      IMPLICIT INTEGER (A-Z)                                                PAL11320
      INTEGER IOUT(64)                                                      PAL11330
      DATA X/'X'/,IDASH/'-'/,LOFANT/'0'/,HIFANT/'O'/                        PAL11340
      DO 10 I=1,32                                                          PAL11350
          IF( IOUT(I).EQ.IDASH ) IOUT(I)=HIFANT                             PAL11360
          IF( IOUT(I).EQ.X )     IOUT(I)=LOFANT                             PAL11370
   10 CONTINUE                                                              PAL11380
      IF((ITYPE.EQ.4).AND.((IPROD.LE.24).OR.(IPROD.GE.41))) RETURN          PAL11390
      IF((ITYPE.EQ.3).AND.((IPROD.LE.16).OR.(IPROD.GE.45))) RETURN          PAL11400
      IF((ITYPE.EQ.2).AND.((IPROD.LE. 8).OR.(IPROD.GE.53))) RETURN          PAL11410
      IF((ITYPE.LE.3).AND.(I8PRO.GE.5)) RETURN                              PAL11420
      IF((ITYPE.LE.2).AND.(IPROD.GE.19).AND.(IPROD.LE.48).AND.              PAL11430
     1    (I8PRO.GE.3)) RETURN                                              PAL11440
      IF((ITYPE.EQ.1).AND.(I8PRO.GE.3)) RETURN                              PAL11450
      DO 50 I=1,32                                                          PAL11460
        IF(((I.EQ.15).OR.(I.EQ.16).OR.(I.EQ.19).OR.(I.EQ.20)).AND.          PAL11470
     1    (ITYPE.LE.3)) GO TO 50                                            PAL11480
        IF(((I.EQ.11).OR.(I.EQ.12).OR.(I.EQ.23).OR.(I.EQ.24)).AND.          PAL11490
     1    (ITYPE.LE.2)) GO TO 50                                            PAL11500
        IF(((I.EQ. 7).OR.(I.EQ. 8).OR.(I.EQ.27).OR.(I.EQ.28)).AND.          PAL11510
     1    (ITYPE.LE.1)) GO TO 50                                            PAL11520
        IF( IOUT(I).EQ.HIFANT ) IOUT(I)=IDASH                               PAL11530
        IF( IOUT(I).EQ.LOFANT ) IOUT(I)=X                                   PAL11540
   50 CONTINUE                                                              PAL11550
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      RETURN                                                            PAL11560
      END                                                               PAL11570
C                                                                       PAL11580
C***********************************************************************PAL11590
C                                                                       PAL11600
      SUBROUTINE IODC2                                                  PAL11610
C***** THIS ROUTINE IS OPTIONAL, IT MAY BE USED TO TURN PERIPHERALS ON   PAL11620
      IMPLICIT INTEGER (A-Z)                                            PAL11630
      INTEGER   BEL,DC2,ESC,FF,NUL                                      PAL11640
      COMMON /LUNIT/ PMS,POF,PDF                                        PAL11650
      DATA BEL /Z07000000/ , DC2 /Z22000000/                            PAL11660
      WRITE(PDF,10) DC2,BEL                                             PAL11670
   10 FORMAT(' ',2A1)                                                   PAL11680
      RETURN                                                            PAL11690
      END                                                               PAL11700
C                                                                       PAL11710
C***********************************************************************PAL11720
C                                                                       PAL11730
      SUBROUTINE IODC4                                                  PAL11740
C***** THIS ROUTINE IS OPTIONAL, IT MAY BE USED TO TURN PERIPHERALS OFF  PAL11750
      IMPLICIT INTEGER (A-Z)                                            PAL11760
      INTEGER   BEL,DC3,DC4                                             PAL11770
      COMMON /LUNIT/ PMS,POF,PDF                                        PAL11780
      DATA BEL/Z07000000/,DC3/Z23000000/,DC4/Z24000000/                 PAL11790
      WRITE(PDF,10) BEL,DC3,DC4                                         PAL11800
   10 FORMAT(' ',3A1)                                                   PAL11810
      RETURN                                                            PAL11820
      END                                                               PAL11830
C                                                                       PAL11840
C***********************************************************************PAL11850
C                                                                       PAL11860
      SUBROUTINE TEST(LPHASE,LBUF,TITLE,IC,IL,ILE,ISYM,IBUF,ITYPE,      PAL11870
     1                INOO,LFIX,IPCTR,LERR,ISAF,IPCTR1,LSA11,LSA01)     PAL11880
C     THIS SUBROUTINE PERFORMS THE FUNCTION TABLE SIMULATION            PAL11890
C      AND GENERATES TEST VECTORS                                       PAL11900
      IMPLICIT INTEGER (A-Z)                                            PAL11910
      INTEGER ISYM(8,20),ISYM1(8,20),IBUF(8,20),IVECT(20),IVECTP(20),   PAL11920
     1        ISTATE(20),ISTATT(20),IPIN(20),TITLE(80),IPCTR             PAL11930
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR,    PAL11940
     1        LFIX,LSAME,XORFND,LERR,LPHASE(20),LPHAS1(20),LBUF(20),     PAL11950
     2        LOUT(20),LOUTP(20),LCLOCK,LPTRST,LCTRST,LENABL(20),NREG,   PAL11960
     3        LSA11,LSA12,LSA01                                         PAL11970
      INTEGER   BEL                                                     PAL11980
      COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR     PAL11990
      COMMON /PGE/ IPAGE(80,200)                                        PAL12000
      COMMON /LUNIT/ PMS,POF,PDF                                        PAL12010
      COMMON /FTEST/ IFUNCT,IDESC,IEND                                  PAL12020
      DATA IDASH/'-'/,L/'L'/,H/'H'/,X/'X'/,C/'C'/,Z/'Z'/,N0/'0'/,       PAL12030
     1     N1/'1'/,ERR/'?'/,IBLANK/' '/,COMENT/';'/,I4/'4'/,I6/'6'/,    PAL12040
     2     I8/'8'/                                                      PAL12050
      DATA BEL/Z07000000/                                               PAL12060
C     PRINT AN ERROR MESSAGE IF NO FUNCTION TABLE IS SUPPLIED           PAL12070
      IF(IFUNCT.NE.0) GO TO 3                                           PAL12080
      WRITE(PMS,2)                                                      PAL12090
    2 FORMAT(/,' FUNCTION TABLE MUST BE SUPPLIED IN ORDER TO PERFORM',  PAL12100
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

     1          ' SIMULATION')                                          PAL12110
      RETURN                                                           PAL12120
C     PRINT TITLE                                                      PAL12130
    3 IF((.NOT.LSA11).AND.(.NOT.LSA01)) WRITE(POF,4) TITLE             PAL12140
    4 FORMAT(/,' ',80A1,/)                                             PAL12150
C     INITIALIZE LERR (FUNCTION TABLE ERROR FLAG) TO NO ERROR          PAL12160
      LERR=.FALSE.                                                     PAL12170
C     INITIALIZE NERR (NUMBER OF FUNCTION TABLE ERRORS) TO NO ERRORS   PAL12180
      NERR=0                                                           PAL12190
C     INITIALIZE ITRST (THREE-STATE ENABLE FUNCTION TABLE PIN NUMBER)  PAL12200
      ITRST=0                                                          PAL12210
C     SET THE STARTING POINT OF THE FUNCTION TABLE TO COLUMN 0         PAL12220
C     AND IFUNCT + 1                                                   PAL12230
      IC=0                                                             PAL12240
      IL=IFUNCT + 1                                                    PAL12250
C     INITIALIZE SA1/SA0 PARAMETERS                                    PAL12260
      IPCTR3=0                                                         PAL12270
      IEQN=0                                                           PAL12280
      IPCTR=0                                                          PAL12290
C                                                                      PAL12300
C     MAKE A DUMMY CALL TO INCR                                        PAL12310
      CALL INCR(IC,IL,LFIX)                                            PAL12320
C     GET THE FUNCTION TABLE PIN LIST (UP TO 18)                       PAL12330
C      GO ONE MORE THAN MAX TO LOOK FOR DASHED LINE                    PAL12340
      DO 10 I=1,19                                                     PAL12350
      CALL GETSYM(LPHAS1,ISYM1,I,IC,IL,LFIX)                           PAL12360
         DO 5 J=1,8                                                    PAL12370
    5    IBUF(J,1)=ISYM1(J,1)                                          PAL12380
      IF(IBUF(8,1).EQ.IDASH) GO TO 12                                  PAL12390
      CALL MATCH(IMATCH,IBUF,ISYM)                                     PAL12400
      IF(IMATCH.NE.0) GO TO 7                                          PAL12410
      WRITE(PMS,6) (IBUF(J,1),J=1,8)                                   PAL12420
    6 FORMAT(/,' FUNCTION TABLE PIN LIST ERROR AT', 8A1)               PAL12430
      RETURN                                                           PAL12440
    7 LOUT(I)=.FALSE.                                                  PAL12450
      ISTATT(I)=X                                                      PAL12460
      IVECTP(I)=X                                                      PAL12470
C     IF APPROPIATE PAL TYPE, REMEMBER LOCATION OF CLOCK AND THREE-STATEPAL12480
C      ENABLE PIN IN FUNCTION TABLE PIN LIST                           PAL12490
      IF(ITYPE.NE.6) GO TO 10                                          PAL12500
      IF(IMATCH.EQ.1)  ICLOCK=I                                        PAL12510
      IF(IMATCH.EQ.11) ITRST=I                                         PAL12520
   10 IPIN(I)=IMATCH                                                   PAL12530
C     ALL SIGNAL NAMES FOR THE FUNCTIONAL TEST HAVE BEEN READ IN       PAL12540
C      ADJUST COUNT                                                    PAL12550
   12 IMAX=I-1                                                         PAL12560
      NVECT=0                                                          PAL12570
C                                                                      PAL12580
C*****START OF MAIN LOOP FOR SIMULATION*****                          PAL12590
C                                                                      PAL12600
C                                                                      PAL12610
C     INITIALLY THERE ARE NO FAULTS. IPCTR2 IS THE POINTER FOR         PAL12620
C     TOTAL NUMBER OF PRODUCT TERMS. IEQN IS EQUATION COUNT.           PAL12630
C     IPCTR3 IS THE PRODUCT TERM POINTER IN A PARTICULAR EQN.          PAL12640
   90 IPCTR2=0                                                         PAL12650
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      IEQN=0                                                            PAL12660
      IPCTR3=0                                                          PAL12670
      LSA12=.FALSE.                                                     PAL12680
      LSA02=.FALSE.                                                     PAL12690
C                                                                       PAL12700
      NVECT=NVECT+1                                                     PAL12710
      IC1=0                                                             PAL12720
      IL1=ILE                                                           PAL12730
C     GO PASSED COMMENT LINES                                           PAL12740
   23 IF(IPAGE(1,IL).NE.COMENT) GO TO 24                                PAL12750
      IL=IL+1                                                           PAL12760
      GO TO 23                                                          PAL12770
   24 CONTINUE                                                          PAL12780
C     GETS VECTORS FROM FUNCTION TABLE                                  PAL12790
      DO 20 I=1,IMAX                                                    PAL12800
        IF(IPAGE(IC,IL).EQ.IBLANK) GO TO 21                             PAL12810
        GO TO 22                                                        PAL12820
   21   IC=IC+1                                                         PAL12830
        IF(IPAGE(IC,IL).EQ.IBLANK) GO TO 21                             PAL12840
   22   IVECT(I)=IPAGE(IC,IL)                                           PAL12850
        IC=IC+1                                                         PAL12860
   20 CONTINUE                                                          PAL12870
C     ADVANCE LINE COUNT TO SKIP FUNCTION TABLE COMMENTS                PAL12880
      IL=IL+1                                                           PAL12890
      IC=1                                                              PAL12900
      IF(IVECT(1).EQ.IDASH) GO TO 95                                    PAL12910
C     CHECK FOR VALID FUNCTION TABLE VALUES (L,H,X,Z,C)                 PAL12920
      DO 11 I=1,IMAX                                                    PAL12930
        IF( IVECT(I).EQ.L.OR.IVECT(I).EQ.H.OR.IVECT(I).EQ.X.OR.         PAL12940
     1      IVECT(I).EQ.Z.OR.IVECT(I).EQ.C) GO TO 11                    PAL12950
        WRITE(PMS,8) IVECT(I),NVECT                                     PAL12960
    8   FORMAT(/,' ',A1,' IS NOT AN ALLOWED FUNCTION TABLE ENTRY',      PAL12970
     1         ' IN VECTOR ',I3)                                        PAL12980
        RETURN                                                          PAL12990
   11 CONTINUE                                                          PAL13000
C     INITIALIZE CLOCK AND THREE-STATE ENABLE FLAGS                     PAL13010
      LCLOCK=.FALSE.                                                    PAL13020
      LCTRST=.TRUE.                                                     PAL13030
      LPTRST=.TRUE.                                                     PAL13040
      DO 13 I=1,IMAX                                                    PAL13050
   13   LENABL(I)=.TRUE.                                                PAL13060
C     INITIALIZE NREG (NOT REGISTERED OUTPUT) TO FALSE                  PAL13070
      NREG=.FALSE.                                                      PAL13080
C     INITIALIZE ISTATE ARRAY TO ALL X'S                                PAL13090
      DO 15 I=1,20                                                      PAL13100
   15 ISTATE(I)=X                                                       PAL13110
C     CHECK IF THIS PAL TYPE HAS REGISTERS                              PAL13120
      IF(ITYPE.NE.6) GO TO 25                                           PAL13130
C     CHECK CLOCK AND THREE-STATE ENABLE PINS AND CHANGE FLAG IF NEEDED PAL13140
      IF(IVECT(ICLOCK).EQ.C) LCLOCK=.TRUE.                              PAL13150
      IF(ITRST.EQ.0) GO TO 25                                           PAL13160
      LSAME=( (     LPHASE(11)).AND.(     LPHAS1(ITRST)).OR.          PAL13170
     1        (.NOT.LPHASE(11)).AND.(.NOT.LPHAS1(ITRST)) )             PAL13180
      IF( IVECT(ITRST).EQ.L.AND.(.NOT.LSAME).OR.                        PAL13190
     1    IVECT(ITRST).EQ.H.AND.(     LSAME) ) LPTRST=.FALSE.          PAL13200
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0


      IF(LPIRST) GO TO 25                                                    PAL13210
C     DISABLE REGISTERED OUTPUTS IF APPROPRIATE                              PAL13220
      DO 46 I=1,IMAX                                                         PAL13230
         J=IPIN(I)                                                           PAL13240
         IF(J.EQ.14.OR.J.EQ.15.OR.J.EQ.16.OR.J.EQ.17) LENABL(I)=.FALSE.      PAL13250
         IF( INOO.EQ.I6.AND.(J.EQ.13.OR.J.EQ.18) )    LENABL(I)=.FALSE.      PAL13260
         IF( INOO.EQ.I8.AND.(J.EQ.12.OR.J.EQ.13                              PAL13270
     1                    .OR.J.EQ.18.OR.J.EQ.19) )    LENABL(I)=.FALSE.    PAL13280
   46 CONTINUE                                                               PAL13290
C                                                                            PAL13300
C*****SCAN THROUGH THE LOGIC EQUATIONS*****                                  PAL13310
C                                                                            PAL13320
C     MAKE A DUMMY CALL TO INCR                                              PAL13330
   25 CALL INCR(IC1,IL1,LFIX)                                                PAL13340
   26 CALL GETSYM(LBUF,IBUF,1,IC1,IL1,LFIX)                                  PAL13350
      IF(LLEFT) GO TO 29                                                     PAL13360
   27 IF(.NOT.LEQUAL) GO TO 26                                               PAL13370
C                                                                            PAL13380
      IF(LEQUAL) IEQN=IEQN+1                                                 PAL13390
C                                                                            PAL13400
C     EVALUATE CONDITIONAL THREE-STATE PRODUCT LINE                          PAL13410
   29 IF(LEQUAL) GO TO 35                                                    PAL13420
      NREG=.TRUE.                                                            PAL13430
   33 CALL GETSYM(LBUF,IBUF,1,IC1,IL1,LFIX)                                  PAL13440
      CALL MATCH(IINP,IBUF,ISYM1)                                            PAL13450
C     CHECK FOR GND, VCC, /GND, OR /VCC IN CONDITIONAL THREE-STATE           PAL13460
C      PRODUCT LINE                                                          PAL13470
      IF(IINP.NE.0) GO TO 32                                                 PAL13480
      CALL MATCH(IMATCH,IBUF,ISYM)                                           PAL13490
      ILL=IL1                                                                PAL13500
      IF( IINP.EQ.0.AND.IMATCH.NE.10.AND.IMATCH.NE.20 ) GO TO 100            PAL13510
      IF( IMATCH.EQ.10.AND.(LBUF(1)).OR.                                     PAL13520
     1    IMATCH.EQ.20.AND.(.NOT.LBUF(1)) ) LCTRST=.FALSE.                   PAL13530
      GO TO 34                                                               PAL13540
   32 ITEST=IVECT(IINP)                                                      PAL13550
      IF(  ITEST.EQ.L.AND.(     LPHAS1(IINP)).AND.(     LBUF(1))             PAL13560
     1.OR. ITEST.EQ.H.AND.(     LPHAS1(IINP)).AND.(.NOT.LBUF(1))             PAL13570
     2.OR. ITEST.EQ.H.AND.(.NOT.LPHAS1(IINP)).AND.(     LBUF(1))             PAL13580
     3.OR. ITEST.EQ.L.AND.(.NOT.LPHAS1(IINP)).AND.(.NOT.LBUF(1))             PAL13590
     4  )  LCTRST=.FALSE.                                                    PAL13600
      IF(ITEST.EQ.X.OR.ITEST.EQ.Z) LCTRST=.FALSE.                            PAL13610
   34 IF(LAND) GO TO 33                                                      PAL13620
      GO TO 27                                                               PAL13630
C                                                                            PAL13640
C     EVALUATE THE LOGIC EQUATION                                            PAL13650
C                                                                            PAL13660
C     FIND THE PIN NUMBER OF THE OUTPUT VECTORS                              PAL13670
C                                                                            PAL13680
   35  IPCTR3=0                                                              PAL13690
C                                                                            PAL13700
      CALL MATCH(IOUTP,IBUF,ISYM1)                                           PAL13710
C     FLAG UNREGISTERED OUTPUTS                                              PAL13720
      CALL MATCH(IOUT,IBUF,ISYM)                                             PAL13730
      IF(ITYPE.LE.5) NREG=.TRUE.                                             PAL13740
      IF( (INOO.EQ.I4.OR.INOO.EQ.I6).AND.(IOUT.EQ.12.OR.IOUT.EQ.19) )        PAL13750
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

     1      NREG=.TRUE.                                                    PAL13760
      IF( (INOO.EQ.I4).AND.(IOUT.EQ.13.OR.IOUT.EQ.18) ) NREG=.TRUE.       PAL13770
      ILL=ILI                                                            PAL13780
      IF(IOUTP.EQ.0) GO TO 100                                           PAL13790
      IF(NREG) LENABL(IOUTP)=LCTRST                                      PAL13800
      LOUT(IOUTP)=.TRUE.                                                 PAL13810
      IF( .NOT.LCTRST ) LOUT(IOUTP)=.FALSE.                              PAL13820
      LCTRST=.TRUE.                                                      PAL13830
      LOUTP(IOUTP)=LBUF(1)                                               PAL13840
C     DETERMINE PRODUCT TERM AND EVENTUALLY SUM FOR OUTPUT KEEPING       PAL13850
C      TRACK TO SEE IF AN XOR (EXCLUSIVE OR) HAS BEEN FOUND              PAL13860
      XORSUM=H                                                           PAL13870
      XORFND=.FALSE.                                                     PAL13880
      ISUM=L                                                             PAL13890
C                                                                        PAL13900
   28 IPCTR2=IPCTR2+1                                                    PAL13910
      IPCTR3=IPCTR3+1                                                    PAL13920
C                                                                        PAL13930
      IPCTR=IPCTR+1                                                      PAL13940
      IPROD=H                                                            PAL13950
   30 ILL=ILI                                                            PAL13960
      CALL GETSYM(LBUF,IBUF,1,IC1,IL1,LFIX)                              PAL13970
      IF( .NOT.LFIX ) GO TO 39                                           PAL13980
C     EVALUATE THE FIXED SYMBOLS FOUND IN THE PAL16X4 AND PAL16A4        PAL13990
          LFIX=.FALSE.                                                   PAL14000
          CALL FIXTST(LPHAS1,LBUF,IC1,IL1,ISYM,ISYM1,IBUF,               PAL14010
     1                IVECT,IVECTP,ITEST,LCLOCK,NREG,LFIX)               PAL14020
          IF(IPROD.EQ.H) IPROD=ITEST                                     PAL14030
          GO TO 38                                                       PAL14040
   39 CALL MATCH(IINP,IBUF,ISYM1)                                        PAL14050
      IF(IINP.NE.0) GO TO 47                                             PAL14060
      CALL MATCH(IMATCH,IBUF,ISYM)                                       PAL14070
      IF(IMATCH.NE.10.AND.IMATCH.NE.20) GO TO 100                        PAL14080
C     TWEEK FOR GND AND VCC IN PRODUCT LINE                              PAL14090
      IF(IMATCH.EQ.10) ITEST=L                                           PAL14100
      IF(IMATCH.EQ.20) ITEST=H                                           PAL14110
      IINP=19                                                            PAL14120
      LPHAS1(19)=.TRUE.                                                  PAL14130
      GO TO 37                                                           PAL14140
   47 ITEST=IVECT(IINP)                                                  PAL14150
C     GET REGISTERED FEED BACK VALUES                                    PAL14160
      IF(NREG) GO TO 37                                                  PAL14170
      CALL MATCH(IIFB,IBUF,ISYM)                                         PAL14180
      IF( (INOO.EQ.I4.OR.INOO.EQ.I6.OR.INOO.EQ.I8).AND.                  PAL14190
     1    (IIFB.EQ.14.OR.IIFB.EQ.15.OR.IIFB.EQ.16.OR.IIFB.EQ.17) )       PAL14200
     2     ITEST=IVECTP(IINP)                                            PAL14210
      IF( (INOO.EQ.I6.OR.INOO.EQ.I8).AND.(IIFB.EQ.13.OR.IIFB.EQ.18) )    PAL14220
     1     ITEST=IVECTP(IINP)                                            PAL14230
      IF(  INOO.EQ.I8.AND.(IIFB.EQ.12.OR.IIFB.EQ.19) )                   PAL14240
     1     ITEST=IVECTP(IINP)                                            PAL14250
   37 IF( ITEST.EQ.X.OR.ITEST.EQ.Z ) ITEST=L                             PAL14260
      IF(  ITEST.EQ.L.AND.(     LPHAS1(IINP)).AND.(     LBUF(1))         PAL14270
     1.OR. ITEST.EQ.H.AND.(     LPHAS1(IINP)).AND.(.NOT.LBUF(1))         PAL14280
     2.OR. ITEST.EQ.H.AND.(.NOT.LPHAS1(IINP)).AND.(     LBUF(1))         PAL14290
     3.OR. ITEST.EQ.L.AND.(.NOT.LPHAS1(IINP)).AND.(.NOT.LBUF(1))         PAL14300
```

```
     4  )  IPROD=L                                                          PAL14310
C                                                                           PAL14320
C      CHECK FOR A PARTICULAR PRODUCT TERM AND GO FOR SA1 TEST              PAL14330
       IF((IPCTR2.EQ.IPCTR1).AND.(LSA11))GO TO 110                          PAL14340
C                                                                           PAL14350
    38 IF(LRIGHT) CALL INCR(IC1,IL1,LFIX)                                   PAL14360
       IF(LAND) GO TO 30                                                    PAL14370
C                                                                           PAL14380
C      CHECK FOR A PARTICULAR PRODUCT TERM AND GO FOR SA0 TEST              PAL14390
       IF((IPCTR2.EQ.IPCTR1).AND.(LSA01))GO TO 120                          PAL14400
C                                                                           PAL14410
   121 IF(ISUM.EQ.L.AND.IPROD.EQ.X) ISUM=X                                  PAL14420
       IF( (ISUM.NE.H).AND.IPROD.EQ.H ) ISUM=H                              PAL14430
C      CHECK FOR XOR (EXCLUSIVE OR) AND SAVE INTERMEDIATE VALUE             PAL14440
       IF(.NOT.LXOR) GO TO 31                                               PAL14450
       XORSUM=ISUM                                                          PAL14460
       XORFND=.TRUE.                                                        PAL14470
       ISUM=L                                                               PAL14480
       GO TO 28                                                             PAL14490
    31 IF(LOR) GO TO 28                                                     PAL14500
       IPCTR3=0                                                             PAL14510
C      IF END OF EQUATION HAS BEEN FOUND, DETERMINE FINAL SUM AND SAVE ITPAL14520
       IF(.NOT.XORFND)     ISTATT(IOUTP)=ISUM                               PAL14530
       IF( (XORFND).AND.((ISUM.EQ.L.AND.XORSUM.EQ.L).OR.                    PAL14540
      1                  (ISUM.EQ.H.AND.XORSUM.EQ.H)) ) ISTATT(IOUTP)=L    PAL14550
       IF( (XORFND).AND.((ISUM.EQ.H.AND.XORSUM.EQ.L).OR.                    PAL14560
      1                  (ISUM.EQ.L.AND.XORSUM.EQ.H)) ) ISTATT(IOUTP)=H    PAL14570
       IF( (XORFND).AND. (ISUM.EQ.X.OR. XORSUM.EQ.X) )  ISTATT(IOUTP)=X     PAL14580
C      REGISTER DOES NOT CHANGE STATE IF NO CLOCK PULSE IS RECEIVED         PAL14590
       IF( (LCLOCK).OR.(NREG) ) GO TO 36                                    PAL14600
       LSAME = ( (     LOUTP(IOUTP)).AND.(     LPHAS1(IOUTP)).OR.         PAL14610
      1          (.NOT.LOUTP(IOUTP)).AND.(.NOT.LPHAS1(IOUTP)) )            PAL14620
       IF( IVECTP(IOUTP).EQ.L.AND.(     LSAME) ) ISTATT(IOUTP)=L           PAL14630
       IF( IVECTP(IOUTP).EQ.H.AND.(     LSAME) ) ISTATT(IOUTP)=H           PAL14640
       IF( IVECTP(IOUTP).EQ.L.AND.(.NOT.LSAME) ) ISTATT(IOUTP)=H           PAL14650
       IF( IVECTP(IOUTP).EQ.H.AND.(.NOT.LSAME) ) ISTATT(IOUTP)=L           PAL14660
    36 NREG=.FALSE.                                                         PAL14670
C      CHECK IF ALL EQUATIONS HAVE BEEN PROCESSED BY COMPARING CURRENT      PAL14680
C       LINE NUMBER WITH FUNCTION TABLE LINE NUMBER                         PAL14690
        IF(IDESC.NE.0.AND.IL1.LT.IFUNCT.AND.IL1.LT.IDESC.OR.                PAL14700
      1   IDESC.EQ.0.AND.IL1.LT.IFUNCT) GO TO 27                            PAL14710
C      DETERMINE OUTPUT LOGIC VALUES                                        PAL14720
C       COMPARE OUTPUTS TO SEE IF VECTOR AGREES WITH RESULTS                PAL14730
       DO 50 I=1,IMAX                                                       PAL14740
       IF( .NOT.LOUT(I) ) GO TO 50                                          PAL14750
       IF( ISTATT(I).EQ.X.AND.IVECT(I).EQ.X ) GO TO 50                      PAL14760
       LSAME = ( (     LOUTP(I)).AND.(     LPHAS1(I)).OR.                   PAL14770
      1          (.NOT.LOUTP(I)).AND.(.NOT.LPHAS1(I)) )                    PAL14780
       IMESS=40                                                             PAL14790
       IF(ISTATT(I).EQ.L.AND.IVECT(I).EQ.L.AND.(.NOT.LSAME)) IMESS=41       PAL14800
       IF(ISTATT(I).EQ.H.AND.IVECT(I).EQ.H.AND.(.NOT.LSAME)) IMESS=42       PAL14810
       IF(ISTATT(I).EQ.L.AND.IVECT(I).EQ.H.AND.(     LSAME)) IMESS=42       PAL14820
       IF(ISTATT(I).EQ.H.AND.IVECT(I).EQ.L.AND.(     LSAME)) IMESS=41       PAL14830
       IF( (     LENABL(I)).AND.IVECT(I).EQ.Z )              IMESS=43       PAL14840
       IF( (.NOT.LENABL(I)).AND.(LOUT(I)).AND.IVECT(I).NE.Z) IMESS=44       PAL14850
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      IF(IMESS.NE.40) LERR=.TRUE.                                          PAL14860
C                                                                          PAL14870
C     IF NO FAULT GO FOR NEXT VECTOR ELSE GET OUT OF SIMULATION AND        PAL14880
C     START SIMULATION FOR THE NEXT PRODUCT TERM.                          PAL14890
      IF((.NOT.LERR).AND.((LSA11).OR.(LSA01))) GO TO 50                    PAL14900
      IF((LERR).AND.((LSA11).OR.(LSA01))) GO TO 115                        PAL14910
C                                                                          PAL14920
      IF(IMESS.EQ.41) WRITE(PMS,41) NVECT,(ISYM1(J,I),J=1,8)               PAL14930
   41 FORMAT(/,' FUNCTION TABLE ERROR IN VECTOR',I3,'  PIN =',8A1,         PAL14940
     1          '  EXPECT = H  ACTUAL = L')                               PAL14950
      IF(IMESS.EQ.42) WRITE(PMS,42) NVECT,(ISYM1(J,I),J=1,8)               PAL14960
   42 FORMAT(/,' FUNCTION TABLE ERROR IN VECTOR',I3,'  PIN =',8A1,         PAL14970
     1          '  EXPECT = L  ACTUAL = H')                               PAL14980
      IF(IMESS.EQ.43) WRITE(PMS,43) NVECT,(ISYM1(J,I),J=1,8)               PAL14990
   43 FORMAT(/,' FUNCTION TABLE ERROR IN VECTOR',I3,'  PIN =',8A1,         PAL15000
     1       /,'  EXPECT  = OUTPUT ENABLE  ACTUAL = Z')                   PAL15010
      IF(IMESS.EQ.44) WRITE(PMS,44) NVECT,(ISYM1(J,I),J=1,8),IVECT(I)      PAL15020
   44 FORMAT(/,' FUNCTION TABLE ERROR IN VECTOR',I3,'  PIN =',8A1,         PAL15030
     1          '  EXPECT = Z  ACTUAL = ',A1)                             PAL15040
      IF( (IMESS.NE.40).AND.(PMS.EQ.6) ) WRITE(PMS,45) BEL                 PAL15050
   45 FORMAT(' ',A1)                                                       PAL15060
      IF(IMESS.NE.40) IVECT(I)=ERR                                         PAL15070
      IF(IMESS.NE.40) NERR=NERR+1                                          PAL15080
   50 CONTINUE                                                             PAL15090
C     CHANGE THE ORDER OF VECTORS FROM THE ORDER OF APPEARANCE IN THE      PAL15100
C      FUNCTION TABLE TO THAT OF THE PIN LIST AND TWEEK FOR OUTPUT         PAL15110
      DO 65 I=1,20                                                         PAL15120
         DO 55 J=1,IMAX                                                    PAL15130
         IF(IPIN(J).NE.I) GO TO 55                                         PAL15140
         IF( IVECT(J).EQ.L.OR.IVECT(J).EQ.H ) GO TO 51                     PAL15150
         ISTATE(I)=IVECT(J)                                                PAL15160
         GO TO 65                                                          PAL15170
   51    LSAME=( (      LPHASE(I)).AND.(      LPHAS1(J)).OR.              PAL15180
     1           (.NOT.LPHASE(I)).AND.(.NOT.LPHAS1(J)) )                   PAL15190
         IF( INOO.EQ.N1.AND.(I.EQ.15.OR.I.EQ.16) )  LOUT(J)=.TRUE.         PAL15200
         IF( (.NOT.LOUT(J)).AND.(      LSAME).AND.                         PAL15210
     1          IVECT(J).EQ.L )                          ISTATE(I)=NO      PAL15220
         IF( (.NOT.LOUT(J)).AND.(      LSAME).AND.                         PAL15230
     1          IVECT(J).EQ.H )                          ISTATE(I)=N1      PAL15240
         IF( (.NOT.LOUT(J)).AND.(.NOT.LSAME).AND.                          PAL15250
     1          IVECT(J).EQ.L )                          ISTATE(I)=N1      PAL15260
         IF( (.NOT.LOUT(J)).AND.(.NOT.LSAME).AND.                          PAL15270
     1          IVECT(J).EQ.H ).                         ISTATE(I)=NO      PAL15280
         IF( (      LOUT(J)).AND.(      LSAME).AND.                        PAL15290
     1          IVECT(J).EQ.L.AND.(      LENABL(J)) )  ISTATE(I)=L        PAL15300
         IF( (      LOUT(J)).AND.(      LSAME).AND.                        PAL15310
     1          IVECT(J).EQ.H.AND.(      LENABL(J)) )  ISTATE(I)=H        PAL15320
         IF( (      LOUT(J)).AND.(.NOT.LSAME).AND.                         PAL15330
     1          IVECT(J).EQ.L.AND.(      LENABL(J)) )  ISTATE(I)=H        PAL15340
         IF( (      LOUT(J)).AND.(.NOT.LSAME).AND.                         PAL15350
     1          IVECT(J).EQ.H.AND.(      LENABL(J)) )  ISTATE(I)=L        PAL15360
         IF( IVECT(J).EQ.ERR )                          ISTATE(I)=ERR     PAL15370
         GO TO 65                                                          PAL15380
   55 CONTINUE                                                             PAL15390
C     SAVE PRESENT VECTORS FOR FEED BACK USED WITH NEXT SET OF VECTORS     PAL15400
```

```
FILE: PAL20     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

C       IF CLOCK PULSE AND NOT Z (HI-Z IS ASYNCHRONOUS)                  PAL15410
   65 IF( (LCLOCK).AND.IVECT(J).NE.Z ) IVECTP(J)=IVECT(J)                PAL15420
C       ASSIGN X TO GROUND PIN AND 1 TO VCC PIN                          PAL15430
        ISTATE(10)=X                                                     PAL15440
        ISTATE(20)=N1                                                    PAL15450
C       PRINT TEST VECTORS                                               PAL15460
        IF((.NOT.LSA11).AND.(.NOT.LSA01))WRITE(POF,60)                   PAL15470
       1 NVECT,(ISTATE(I),I=1,20)                                        PAL15480
   60 FORMAT(' ',I3,' ',20A1)                                            PAL15490
        GO TO 90                                                         PAL15500
C       TERMINATE SIMULATION                                             PAL15510
C                                                                        PAL15520
   95 IF((.NOT.LERR).AND.(LSA11))WRITE(POF,150) IPCTR4,IEQN1             PAL15530
  150 FORMAT(' ',' PRODUCT: ',I3,' OF ','EQUATION.',I3,'                 PAL15540
       1 UNTESTED(SA1)FAULT')                                            PAL15550
        IF((.NOT.LERR).AND.(LSA01)) WRITE(POF,155) IPCTR4,IEQN1          PAL15560
  155 FORMAT(' ',' PRODUCT: ',I3,' OF ','EQUATION.',I3,'                 PAL15570
       1 UNTESTED(SA0)FAULT')                                            PAL15580
C                                                                        PAL15590
        IF((.NOT.LERR).AND.((.NOT.LSA11).AND.(.NOT.LSA01))) WRITE(POF,67) PAL15600
   67 FORMAT(/,' PASS SIMULATION')                                       PAL15610
        IPCTR=IPCTR/(NVECT-1)                                            PAL15620
        IF((     LERR).AND.((.NOT.LSA11).AND.(.NOT.LSA01)))              PAL15630
       1WRITE(POF,68) NERR                                               PAL15640
   68 FORMAT(/,' NUMBER OF FUNCTION TABLE ERRORS =',I3)                  PAL15650
        RETURN                                                           PAL15660
C       PRINT AN ERROR MESSAGE FOR AN UNDEFINED PIN NAME                 PAL15670
  100 ILERR=ILL+4                                                        PAL15680
        WRITE(PMS,101) (IBUF(I,1),I=1,8),ILERR,(IPAGE(I,ILL),I=1,80)     PAL15690
  101 FORMAT(/,' ERROR SYMBOL = ',8A1,'      IN LINE NUMBER ',I3,        PAL15700
       1       /,' ',80A1,/,' THIS PIN NAME IS NOT DEFINED IN THE',      PAL15710
       2                  ' FUNCTION TABLE PIN LIST')                   PAL15720
        RETURN                                                           PAL15730
C                                                                        PAL15740
C       THE PRODUCT TERM IS PULLED HIGH AND THE PRODUCT NUMBER           PAL15750
C       AND EQN NUMBER IS REMEMBERED                                     PAL15760
  110 IPROD=H                                                            PAL15770
        LSA12=.TRUE.                                                     PAL15780
        IEQN1=IEQN                                                       PAL15790
        IPCTR4=IPCTR3                                                    PAL15800
        GO TO 38                                                         PAL15810
C                                                                        PAL15820
C                                                                        PAL15830
C                                                                        PAL15840
C       THE PRODUCT TERM IS TESTED FOR SA0 FAULT AND ALSO REMEMBERED     PAL15850
  120 IPROD=L                                                            PAL15860
        LSA02=.TRUE.                                                     PAL15870
        IEQN1=IEQN                                                       PAL15880
        IPCTR4=IPCTR3                                                    PAL15890
        GO TO 121                                                        PAL15900
C                                                                        PAL15910
C                                                                        PAL15920
C                                                                        PAL15930
C       IF NO FAULT THEN NEXT PRODUCT TERM                               PAL15940
  115 ISAF=ISAF+1                                                        PAL15950
```

```
FILE: PAL20     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      LERR=.FALSE.                                                      PAL15960
      RETURN                                                            PAL15970
C                                                                       PAL15980
      END                                                               PAL15990
C                                                                       PAL16000
C*****************************************************************************PAL16010
C                                                                       PAL16020
      SUBROUTINE FIXIST(LPHAS1,LBUF,IC1,IL1,ISYM,ISYM1,IBUF,            PAL16030
     1                  IVECT,IVECTP,ITEST,LCLOCK,NREG,LFIX)            PAL16040
C     THIS SUBROUTINE EVALUATES THE FIXED SYMBOLS FOUND IN THE          PAL16050
C      PAL16A4 AND PAL16A4 FOR THE FUNCTION TABLE                       PAL16060
      IMPLICIT INTEGER (A-Z)                                            PAL16070
      INTEGER ISYM(8,20),ISYM1(8,20),IBUF(8,20),IVECT(20),IVECTP(20)    PAL16080
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR,    PAL16090
     1        LFIX,LPHAS1(20),LBUF(20),LCLOCK,NREG,TOR,TXOR,TXNOR,TAND, PAL16100
     2        LPHASA,LPHASB                                             PAL16110
      COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXNOR     PAL16120
      COMMON /PGE/ IPAGE(80,200)                                        PAL16130
      DATA L/'L'/,H/'H'/,X/'X'/,Z/'Z'/                                  PAL16140
C     GET OUTPUT PIN AN (WHERE N=0,1,2,3)                               PAL16150
      CALL GETSYM(LBUF,IBUF,1,IC1,IL1,LFIX)                             PAL16160
      CALL MATCH(IINP,IBUF,ISYM1)                                       PAL16170
      ITESTA=IVECT(IINP)                                                PAL16180
      LPHASA = ( (      LBUF(1)).AND.(      LPHAS1(IINP)).OR.           PAL16190
     1           (.NOT.LBUF(1)).AND.(.NOT.LPHAS1(IINP)) )               PAL16200
C     GET REGISTERED FEED BACK VALUES                                   PAL16210
      IF(NREG) GO TO 5                                                  PAL16220
      CALL MATCH(IIFB,IBUF,ISYM)                                        PAL16230
      IF( IIFB.EQ.14.OR.IIFB.EQ.15.OR.IIFB.EQ.16.OR.IIFB.EQ.17 )        PAL16240
     1    ITESTA=IVECTP(IINP)                                           PAL16250
    5 IF( (.NOT.LPHASA).AND.ITESTA.EQ.L ) GO TO 10                      PAL16260
      IF( (.NOT.LPHASA).AND.ITESTA.EQ.H ) GO TO 15                      PAL16270
      GO TO 20                                                          PAL16280
   10 ITESTA=H                                                          PAL16290
      GO TO 20                                                          PAL16300
   15 ITESTA=L                                                          PAL16310
   20 IF( .NOT.LRIGHT ) GO TO 25                                        PAL16320
         ITEST=ITESTA                                                   PAL16330
         RETURN                                                         PAL16340
C     SAVE THE FIXED SYMBOL OPERATORS                                   PAL16350
   25 TOR   = (LOR.AND.(.NOT.LXOR))                                     PAL16360
      TXOR  = (LXOR)                                                    PAL16370
      TXNOR = (LXNOR)                                                   PAL16380
      TAND  = (LAND.AND.(.NOT.LXNOR))                                   PAL16390
C     GET INPUT BN (WHERE N=0,1,2,3)                                    PAL16400
      CALL GETSYM(LBUF,IBUF,1,IC1,IL1,LFIX)                             PAL16410
      CALL MATCH(IINP,IBUF,ISYM1)                                       PAL16420
      ITESTB=IVECT(IINP)                                                PAL16430
      LPHASB = ( (      LBUF(1)).AND.(      LPHAS1(IINP)).OR.           PAL16440
     1           (.NOT.LBUF(1)).AND.(.NOT.LPHAS1(IINP)) )               PAL16450
      IF( (.NOT.LPHASB).AND.ITESTB.EQ.L ) GO TO 30                      PAL16460
      IF( (.NOT.LPHASB).AND.ITESTB.EQ.H ) GO TO 35                      PAL16470
      GO TO 40                                                          PAL16480
   30 ITESTB=H                                                          PAL16490
      GO TO 40                                                          PAL16500
```

FILE: PAL20 FORTRAN -A NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

```
   35 ITESTB=L                                                                  PAL16510
C     EVALUATE THE FIXED SYMBOL EXPRESSION                                      PAL16520
   40 ITEST=L                                                                   PAL16530
      IF(    (TOR).AND.(ITESTA.EQ.H.OR. ITESTB.EQ.H) )       ITEST=H           PAL16540
      IF(   (TXOR).AND.((ITESTA.EQ.H.AND.ITESTB.NE.H).OR.                       PAL16550
     1                  (ITESTA.NE.H.AND.ITESTB.EQ.H) ))    ITEST=H           PAL16560
      IF( (TXNOR).AND.((ITESTA.EQ.ITESTB).OR.                                   PAL16570
     1                  (ITESTA.EQ.X.OR.ITESTB.EQ.X) ))     ITEST=H           PAL16580
      IF(   (TAND).AND.(ITESTA.NE.L.AND.ITESTB.NE.L) )      ITEST=H           PAL16590
      IF( (ITESTA.EQ.X.OR.ITESTA.EQ.Z).AND.(ITESTB.EQ.X) )  ITEST=X           PAL16600
      RETURN                                                                    PAL16610
      END                                                                       PAL16620
```

Listing 2. PALASM Source Code for 24 Series

```
FILE: PAL24     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0


C**PALASM24**PALASM24**PALASM24**PALASM24**PALASM24**PALASM24**PALASM24*PAL00010
C                                                                       PAL00020
C  P A L A S M  2 4  -  TRANSLATES SYMBOLIC EQUATIONS INTO PAL OBJECT    PAL00030
C                       CODE  FORMATTED FOR DIRECT INPUT TO STANDARD    PAL00040
C                       PROM PROGRAMMERS.                               PAL00050
C                                                                       PAL00060
C                       INPUT:        PAL DESIGN SPECIFICATION ASSIGNED PAL00070
C                                     TO RPD(1).  OPERATION CODES ARE   PAL00080
C                                     ASSIGNED TO ROP(5).               PAL00090
C                                                                       PAL00100
C                       OUTPUT:       ECHO, SIMULATION, AND FUSE PATTERN PAL00110
C                                     ARE ASSIGNED TO POF(6).  HEX AND  PAL00120
C                                     BINARY PROGRAMMING FORMATS ARE    PAL00130
C                                     ASSIGNED TO PDF(6).  PROMPTS AND  PAL00140
C                                     ERROR MESSAGES ARE ASSIGNED TO    PAL00150
C                                     PMS(6).                           PAL00160
C                                                                       PAL00170
C                       PART NUMBER:  THE PAL PART NUMBER MUST APPEAR   PAL00180
C                                     IN COLUMN ONE OF LINE ONE.        PAL00190
C                                                                       PAL00200
C                       PIN LIST:     24 SYMBOLIC PIN NAMES MUST APPEAR PAL00210
C                                     STARTING ON LINE FIVE.            PAL00220
C                                                                       PAL00230
C                       EQUATIONS:    STARTING FIRST LINE AFTER THE     PAL00240
C                                     PIN LIST IN THE FOLLOWING FORMS:  PAL00250
C                                                                       PAL00260
C                                        A = B*C + D                    PAL00270
C                                                                       PAL00280
C                                        A := B*C + D                   PAL00290
C                                                                       PAL00300
C                                        IF( A*B )  C = D + E           PAL00310
C                                                                       PAL00320
C                                     ALL CHARACTERS FOLLOWING ';' ARE  PAL00330
C                                     IGNORED UNTIL THE NEXT LINE.      PAL00340
C                                                                       PAL00350
C                                     BLANKS ARE IGNORED.               PAL00360
C                                                                       PAL00370
C                       OPERATORS:    ( IN HIERARCHY OF EVALUATION )    PAL00380
C                                                                       PAL00390
C                                      ;     COMMENT FOLLOWS            PAL00400
C                                      /     COMPLEMENT                 PAL00410
C                                      *     AND (PRODUCT)              PAL00420
C                                      +     OR (SUM)                   PAL00430
C                                     :+:    XOR (EXCLUSIVE OR)         PAL00440
C                                     ( )    CONDITIONAL THREE-STATE    PAL00450
C                                      =     EQUALITY                   PAL00460
C                                     :=     REPLACED BY (AFTER CLOCK)  PAL00470
C                                                                       PAL00480
C                       FUNCTION      L, H, X, Z, AND C ARE VALID       PAL00490
C                         TABLE:      FUNCTION TABLE VECTOR ENTRIES.    PAL00500
C                                                                       PAL00510
C                       REFERENCE:    A COMPLETE USERS GUIDE TO         PAL00520
C                                     DESIGNING WITH PALS USING PALASM  PAL00530
C                                     IS PROVIDED IN THE MONOLITHIC     PAL00540
C                                     MEMORIES PAL HANDBOOK.            PAL00550
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

C                                                                       PAL00560
C                       SUBROUTINES: INITL2,GETSYM,INCR,MATCH,IXLATE,   PAL00570
C                                    ECHO,CAT,PINOUT,PLOT,HEX,TWEEK,    PAL00580
C                                    BINR,SLIP,FANTOM,IODC2,IODC4,TEST, PAL00590
C                                    PLOTF,SUMCHK                       PAL00600
C                                                                       PAL00610
C                       REV LEVEL:   02/12/82 (VAX/VMS VERSION)         PAL00620
C                                    10/13/82 FAULT TESTING             PAL00630
C                                    10/15/82 JEDEC FORMAT              PAL00640
C                                    BY:I.M.BENGALI                     PAL00650
C                                                                       PAL00660
C                       AUTHORS:     JOHN BIRKNER AND VINCENT COLI      PAL00670
C                                    MONOLITHIC MEMORIES INC.           PAL00680
C                                    1165 EAST ARQUES AVENUE            PAL00690
C                                    SUNNYVALE, CALIFORNIA 94043        PAL00700
C                                    (408) 739-3535                     PAL00710
C                                                                       PAL00720
C                       FINE PRINT:  MONOLITHIC MEMORIES TAKES NO       PAL00730
C                                    RESPONSIBILITY FOR THE OPERATION   PAL00740
C                                    OR MAINTENANCE OF THIS PROGRAM.    PAL00750
C                                    THE SOURCE CODE AS PRINTED HERE    PAL00760
C                                    PRODUCED THE OBJECT CODE OF THE    PAL00770
C                                    EXAMPLES IN THE APPLICATIONS       PAL00780
C                                    SECTION ON A VAX/VMS 11/780        PAL00790
C                                    COMPUTER AND A NATIONAL CSS IBM    PAL00800
C                                    SYSTEM/370 FORTRAN IV(G).          PAL00810
C                                                                       PAL00820
C***********************************************************************PAL00830
C                                                                       PAL00840
C                                                                       PAL00850
C***********************************************************************PAL00860
C                                                                       PAL00870
C                                                                       PAL00880
C     MAIN PROGRAM                                                      PAL00890
C                                                                       PAL00900
      IMPLICIT INTEGER (A-Z)                                            PAL00910
      INTEGER IPAL(3),INAME(5),REST(72),PATNUM(80),TITLE(80),COMP(80),  PAL00920
     1        ISYM(8,24),IBUF(8,24),JPROD(80)                           PAL00930
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LFIRST,   PAL00940
     1        LMATCH,LFUSES(40,80),LPHASE(24),LBUF(24),LPROD(80),       PAL00950
     2        LSAME,LACT,LOPERR,LINP,LERR,LSA11,LSA01                   PAL00960
      INTEGER   BEL                                                     PAL00970
      COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR           PAL00980
      COMMON /PGE/ IPAGE(80,200)                                        PAL00990
      COMMON /LFUSES/LFUSES                                             PAL01000
      COMMON /FTEST/ IFUNCT,IDESC,IEND                                  PAL01010
      COMMON /LUNIT/ PMS,POF,PDF                                        PAL01020
      DATA E/'E'/,O/'O'/,T/'T'/,P/'P'/,B/'B'/,D/'D'/,H/'H'/,S/'S'/,     PAL01030
     1     L/'L'/,N/'N'/,C/'C'/,Q/'Q'/,U/'U'/,F/'F'/,Y/'Y'/           PAL01040
      DATA BB/'B'/,CC/'C'/,DD/'D'/,EE/'E'/,FF/'F'/,II/'I'/,NN/'N'/,     PAL01050
     1     OO/'O'/,PP/'P'/,RR/'R'/,SS/'S'/,TT/'T'/,UU/'U'/,JJ/'J'/    PAL01060
      DATA BEL/Z07000000/                                               PAL01070
C                                                                       PAL01080
C                                                                       PAL01090
C     ASSIGNMENT OF DATA SET REFERENCES                                 PAL01100
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

C       RPD - PAL DESIGN SPECIFICATION (INPUT)                          PAL01110
C       ROC - OPERATION CODE (INPUT)                                    PAL01120
C       POF - ECHO, PINOUT, TEST, AND PLOT (OUTPUT)                     PAL01130
C       PDF - HEX AND BINARY FORMAT PROGRAM TAPES (OUTPUT)              PAL01140
C       PMS - PROMPTS AND ERROR MESSAGES (OUTPUT)                       PAL01150
        WRITE(6,3)                                                      PAL01160
      3 FORMAT(/,' PALASM VERSION 1.5 ' )                               PAL01170
        WRITE(6,1)                                                      PAL01180
      1 FORMAT(/,' WHAT IS THE LOGICAL UNIT NUMBER FOR OUTPUT(6)?: ')   PAL01190
        READ(5,2) LUN                                                   PAL01200
      2 FORMAT(I4)                                                      PAL01210
        RPD=1                                                           PAL01220
        ROC=5                                                           PAL01230
        POF=6                                                           PAL01240
        PDF=6                                                           PAL01250
        PMS=10                                                          PAL01260
        IFUNCT=0                                                        PAL01270
        IDESC=0                                                         PAL01280
C       INITIALIZE LSAME AND LACT TO FALSE (ACTIVE HIGH/LOW ERROR)      PAL01290
        LSAME=.FALSE.                                                   PAL01300
        LACT=.FALSE.                                                    PAL01310
C       INITIALIZE LOPERR TO FALSE (OUTPUT PIN ERROR)                   PAL01320
        LOPERR=.FALSE.                                                  PAL01330
C       READ IN FIRST 4 LINES OF PAL DESIGN SPECIFICATION               PAL01340
        READ(RPD,10) IPAL,INAME,BEST,PATNUM,TITLE,COMP                  PAL01350
     10 FORMAT(3A1,5A1,72A1,/,80A1,/,80A1,/,80A1)                       PAL01360
C       READ IN PIN LIST (LINE 5) THROUGH THE END OF THE PAL DESIGN     PAL01370
C        SPECIFICATION                                                  PAL01380
        DO 15 J=1,200                                                   PAL01390
           READ(RPD,11,END=16) (IPAGE(I,J),I=1,80)                      PAL01400
     11    FORMAT(80A1)                                                 PAL01410
C          CHECK FOR 'FUNCTION TABLE' AND SAVE ITS LINE NUMBER          PAL01420
           IF(      IFUNCT.EQ.0 .AND.IPAGE(1,J).EQ.FF.AND.              PAL01430
     1          IPAGE(2,J).EQ.UU.AND.IPAGE(3,J).EQ.NN.AND.              PAL01440
     2          IPAGE(4,J).EQ.CC.AND.IPAGE(5,J).EQ.TT.AND.              PAL01450
     3          IPAGE(6,J).EQ.II.AND.IPAGE(7,J).EQ.OO.AND.              PAL01460
     4          IPAGE(8,J).EQ.NN.AND.IPAGE(10,J).EQ.TT.AND.             PAL01470
     5          IPAGE(12,J).EQ.BB.AND.IPAGE(14,J).EQ.EE ) IFUNCT=J      PAL01480
C          CHECK FOR 'DESCRIPTION' AND SAVE ITS LINE NUMBER             PAL01490
           IF(      IDESC.EQ.0 .AND.IPAGE(1,J).EQ.DD.AND.               PAL01500
     1          IPAGE(2,J).EQ.EE.AND.IPAGE(3,J).EQ.SS.AND.              PAL01510
     2          IPAGE(4,J).EQ.CC.AND.IPAGE(5,J).EQ.RR.AND.              PAL01520
     3          IPAGE(6,J).EQ.II.AND.IPAGE(7,J).EQ.PP.AND.              PAL01530
     4          IPAGE(8,J).EQ.TT.AND.IPAGE(9,J).EQ.II.AND.              PAL01540
     5          IPAGE(10,J).EQ.OO.AND.IPAGE(11,J).EQ.NN ) IDESC=J       PAL01550
     15 CONTINUE                                                        PAL01560
C       SAVE THE LAST LINE NUMBER OF THE PAL DESIGN SPECIFICATION       PAL01570
     16 IEND=J-1                                                        PAL01580
        CALL INITLZ(INAME,ITYPE,LFUSES,IC,IL,IBLOW,IPCTR)               PAL01590
C       PRINT ERROR MESSAGE FOR INVALID PAL PART TYPE                   PAL01600
        IF(ITYPE.NE.0) GO TO 17                                         PAL01610
        WRITE(PMS,18) IPAL,INAME                                        PAL01620
     18 FORMAT(/,' PAL PART TYPE ',3A1,5A1,' IS INCORRECT')             PAL01630
        STOP                                                            PAL01640
C       GET 24 PIN NAMES                                                PAL01650
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0


   17 DO 20 J=1,24                                                          PAL01660
   20      CALL GETSYM(LPHASE,ISYM,J,IC,IL)                                 PAL01670
           IF(.NOT.(LEQUAL.OR.LLEFT.OR.LAND.OR.LOR.OR.LRIGHT)) GO TO 24     PAL01680
               WRITE(PMS,23)                                                PAL01690
   23          FORMAT(/,' LESS THAN 24 PIN NAMES IN PIN LIST')              PAL01700
               STOP                                                         PAL01710
   24 ILE=IL                                                                PAL01720
C     BYPASS FUSE PLOT ASSEMBLY IF HAL (H IN LINE 1, COLUMN 1)              PAL01730
      IF( IPAL(1).EQ.H ) GO TO 106                                          PAL01740
   25 CALL GETSYM(LBUF,IBUF,1,IC,IL)                                        PAL01750
   28      IF(.NOT.LEQUAL) GO TO 25                                         PAL01760
           ILL=IL                                                           PAL01770
           CALL MATCH(IMATCH,IBUF,ISYM)                                     PAL01780
           IF( IMATCH.EQ.0 ) GO TO 100                                      PAL01790
C          CHECK FOR VALID POLARITY (ACTIVE LOW)                           PAL01800
           LSAME = ( (     LPHASE(IMATCH)).AND.(     LBUF(1)).OR.         PAL01810
     1               (.NOT.LPHASE(IMATCH)).AND.(.NOT.LBUF(1)) )           PAL01820
           IF( ITYPE.NE.6.AND.(LSAME) ) LACT=.TRUE.                         PAL01830
C          CHECK FOR VALID OUTPUT PIN                                      PAL01840
   29      IF( (ITYPE.EQ.1.OR.ITYPE.EQ.7.OR.ITYPE.EQ.8.OR.ITYPE.EQ.9.OR.   PAL01850
     1          ITYPE.EQ.10).AND.(IMATCH.LT.14.OR.IMATCH.GT.23) )          PAL01860
     2          LOPERR=.TRUE.                                              PAL01870
           IF( (ITYPE.EQ.2.OR.ITYPE.EQ.11.OR.ITYPE.EQ.12.OR.ITYPE.EQ.13     PAL01880
     1          .OR.ITYPE.EQ.14).AND.(IMATCH.LT.15.OR.IMATCH.GT.22) )       PAL01890
     2          LOPERR=.TRUE.                                              PAL01900
           IF(  ITYPE.EQ.3.AND.(IMATCH.LT.16.OR.IMATCH.GT.21) )             PAL01910
     1          LOPERR=.TRUE.                                              PAL01920
           IF(  ITYPE.EQ.4.AND.(IMATCH.LT.17.OR.IMATCH.GT.20) )             PAL01930
     1          LOPERR=.TRUE.                                              PAL01940
           IF( (ITYPE.EQ.5.OR.ITYPE.EQ.6).AND.                              PAL01950
     1         (IMATCH.LT.18.OR.IMATCH.GT.19) ) LOPERR=.TRUE.             PAL01960
           IF( (LACT).OR.(LOPERR) ) GO TO 100                               PAL01970
           I88PRO=(23-IMATCH)*8 + 1                                         PAL01980
C          START PAL20C1 ON PRODUCT LINE 32 (I88PRO=33)                    PAL01990
           IF(INAME(3).EQ.C) I88PRO=33                                      PAL02000
           IC=0                                                             PAL02010
   30        CALL INCR(IC,IL)                                               PAL02020
             IF( .NOT.(LEQUAL.OR.LLEFT) ) GO TO 30                          PAL02030
             LPROD(I88PRO)=.TRUE.                                           PAL02040
             IF(.NOT.LLEFT) CALL SLIP(LFUSES,I88PRO,ITYPE,IBLOW)            PAL02050
           DO 70 I8PRO=1,16                                                 PAL02060
               IF( (LXOR).AND.I8PRO.NE.3 ) GO TO 70                         PAL02070
               IPROD = I88PRO + I8PRO - 1                                   PAL02080
               LPROD(IPROD)=.TRUE.                                          PAL02090
               LFIRST=.TRUE.                                                PAL02100
   50            ILL=IL                                                     PAL02110
                 CALL GETSYM(LBUF,IBUF,1,IC,IL)                             PAL02120
                 CALL MATCH(IMATCH,IBUF,ISYM)                               PAL02130
C                CHECK FOR INVALID INPUT PIN                                PAL02140
                 IF( ITYPE.EQ.1.AND.(IMATCH.GE.14.AND.IMATCH.LE.23) )       PAL02150
     1               LINP=.TRUE.                                            PAL02160
                 IF( ITYPE.EQ.2.AND.(IMATCH.GE.15.AND.IMATCH.LE.22) )       PAL02170
     1               LINP=.TRUE.                                            PAL02180
                 IF( ITYPE.EQ.3.AND.(IMATCH.GE.16.AND.IMATCH.LE.21) )       PAL02190
     1               LINP=.TRUE.                                            PAL02200
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

                IF( ITYPE.EQ.4.AND.(IMATCH.GE.17.AND.IMATCH.LE.20) )      PAL02210
     1              LINP=.TRUE.                                           PAL02220
                IF( ITYPE.EQ.5.AND.(IMATCH.EQ.18.OR.IMATCH.EQ.19) )       PAL02230
     1              LINP=.TRUE.                                           PAL02240
                IF( ITYPE.EQ.6.AND.(IMATCH.EQ.18.OR.IMATCH.EQ.19) )       PAL02250
     1              LINP=.TRUE.                                           PAL02260
                IF( ITYPE.EQ.7.AND.(IMATCH.EQ.14.OR.IMATCH.EQ.23) )       PAL02270
     1              LINP=.TRUE.                                           PAL02280
                IF( ITYPE.EQ.8..AND.(IMATCH.EQ.1.OR.IMATCH.EQ.13) )       PAL02290
     1              LINP=.TRUE.                                           PAL02300
                IF( ITYPE.EQ.9..AND.(IMATCH.EQ.1.OR.IMATCH.EQ.13) )       PAL02310
     1              LINP=.TRUE.                                           PAL02320
                IF( ITYPE.EQ.10..AND.(IMATCH.EQ.1.OR.IMATCH.EQ.13) )      PAL02330
     1              LINP=.TRUE.                                           PAL02340
                IF( ITYPE.EQ.11.AND.(IMATCH.EQ.15.OR.IMATCH.EQ.22) )      PAL02350
     1              LINP=.TRUE.                                           PAL02360
                IF( ITYPE.GE.12.AND.(IMATCH.EQ.1.OR.IMATCH.EQ.13) )       PAL02370
     1              LINP=.TRUE.                                           PAL02380
                ILL=IL                                                    PAL02390
                IF(LINP) GO TO 100                                        PAL02400
                IF(IMATCH.EQ.0) GO TO 100                                 PAL02410
                IF(IMATCH.EQ.12) GO TO 64                                 PAL02420
                IF(.NOT.LFIRST) GO TO 58                                  PAL02430
                    LFIRST=.FALSE.                                        PAL02440
                    DO 56 I=1,40                                          PAL02450
                        IBLOW = IBLOW + 1                                 PAL02460
   56               LFUSES(I,IPROD)=.TRUE.                                PAL02470
   58           CALL IXLATE(IINPUT,LPHASE,IMATCH,LBUF,ITYPE)              PAL02480
                IF(IINPUT.LE.0) GO TO 60                                  PAL02490
                IBLOW = IBLOW - 1                                         PAL02500
                LFUSES(IINPUT,IPROD)=.FALSE.                              PAL02510
                CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.FALSE.,ITYPE,     PAL02520
     1                    LPROD,IOP,IBLOW)                                PAL02530
   60           IF(LAND) GO TO 50                                         PAL02540
   64           IF(.NOT.LRIGHT) GO TO 68                                  PAL02550
   66           CALL INCR(IC,IL)                                          PAL02560
                IF(.NOT.LEQUAL) GO TO 66                                  PAL02570
   68          IF( .NOT.(LOR.OR.LEQUAL) ) GO TO 74                       PAL02580
   70          CONTINUE                                                  PAL02590
   74       ILL=IL                                                       PAL02600
            CALL GETSYM(LBUF,IBUF,1,IC,IL)                               PAL02610
            IF(LLEFT.OR.LEQUAL) GO TO 28                                 PAL02620
  100 IF( ILL.EQ.IFUNCT.OR.ILL.EQ.IDESC.OR.ILL.EQ.IEND ) GO TO 102       PAL02630
C       PRINT AN ERROR MESSAGE FOR AN UNRECOGNIZABLE SYMBOL              PAL02640
        ILERR=ILL+4                                                      PAL02650
        WRITE(PMS,99) BEL                                                PAL02660
   99   FORMAT(' ',A1)                                                   PAL02670
        WRITE(PMS,101) (IBUF(I,1),I=1,8),ILERR,(IPAGE(I,ILL),I=1,80)     PAL02680
  101   FORMAT(/,' ERROR SYMBOL =  ',8A1,'       IN LINE NUMBER ',I3,   PAL02690
     1         /,' ',80A1)                                               PAL02700
C       PRINT AN ERROR MESSAGE FOR ACTIVE HIGH/LOW ERRORS                PAL02710
        IF( (LACT).AND.(.NOT.LOPERR) ) WRITE(PMS,103) IPAL,INAME         PAL02720
  103   FORMAT(' OUTPUT MUST BE INVERTED SINCE ',3A1,5A1,                PAL02730
     1         ' IS AN ACTIVE LOW DEVICE')                               PAL02740
C       PRINT AN ERROR MESSAGE FOR AN INVALID OUTPUT PIN                 PAL02750
```

```
FILE: PAL24     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      IF( (LOPERR).AND.IMATCH.NE.0 ) WRITE(PMS,105) IMATCH,IPAL,INAME   PAL02760
  105 FORMAT(' THIS PIN, NUMBER ',I2,' IS AN INVALID OUTPUT PIN',       PAL02770
     1       ' FOR ',3A1,5A1)                                           PAL02780
C     PRINT AN ERROR MESSAGE FOR AN INVALID INPUT PIN                   PAL02790
      IF(LINP) WRITE(PMS,115) IMATCH,IPAL,INAME                         PAL02800
  115 FORMAT(' THIS PIN NUMBER ',I2,' IS AN INVALID INPUT PIN',         PAL02810
     1       ' FOR ',3A1,5A1)                                           PAL02820
      STOP                                                              PAL02830
  102 CALL TWEEK(ITYPE,LFUSES)                                          PAL02840
  108 WRITE(6,106)                                                      PAL02850
  106 FORMAT(/,' OPERATION CODES:')                                     PAL02860
      WRITE(6,107)                                                      PAL02870
  107 FORMAT(/,' E=ECHO INPUT  O=PINOUT  T=SIMULATE  P=PLOT  B=BRIEF',  PAL02880
     1       /,' C=CATALOG  H=HEX  S=SHORT  L=BHLF  N=BNPF ',          PAL02890
     2       /,' Q=QUIT F=FAULT TESTING  J=JEDEC FORMAT')              PAL02900
      WRITE(6,110)                                                      PAL02910
  110 FORMAT(/,' ENTER OPERATION CODE: ')                               PAL02920
      READ(ROC,120) IOP                                                 PAL02930
  120 FORMAT(A1)                                                        PAL02940
C     CALL IODC2                                                        PAL02950
      IF(POF.NE.6) WRITE(POF,125)                                       PAL02960
  125 FORMAT('1')                                                       PAL02970
      IF(IOP.EQ.E) CALL ECHO(IPAL,INAME,REST,PATNUM,TITLE,COMP)         PAL02980
      IF(IOP.EQ.O) CALL PINOUT(IPAL,INAME,TITLE)                        PAL02990
      IF(IOP.EQ.T) CALL TEST(LPHASE,LBUF,TITLE,IC,IL,ILE,ISYM,IBUF,     PAL03000
     1                ITYPE,IPCTR,LERR,ISAF,IPCTR1,.FALSE.,.FALSE.)     PAL03010
      IF(IOP.EQ.JJ) CALL PLOTF                                          PAL03020
C                                                                       PAL03030
      ISAF=0                                                            PAL03040
      IF(IOP.EQ.F) GO TO 200                                            PAL03050
C                                                                       PAL03060
  135 IF(IOP.EQ.P) CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.TRUE.,ITYPE, PAL03070
     1                       LPROD,IOP,IBLOW,IPCTR0)                    PAL03080
      IF(IOP.EQ.B) CALL PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,.TRUE.,ITYPE, PAL03090
     1                       LPROD,IOP,IBLOW,IPCTR0)                    PAL03100
      IF(IOP.EQ.H) CALL HEX(LFUSES,H)                                   PAL03110
      IF(IOP.EQ.S) CALL HEX(LFUSES,S)                                   PAL03120
      IF(IOP.EQ.L) CALL BINR(LFUSES,H,L)                                PAL03130
      IF(IOP.EQ.N) CALL BINR(LFUSES,P,N)                                PAL03140
      IF(IOP.EQ.C) CALL CAT                                             PAL03150
C     CALL IODC4                                                        PAL03160
      IF(IOP.NE.Q ) GO TO 108                                           PAL03170
      STOP                                                              PAL03180
C                                                                       PAL03190
C  SETTING THE PARAMETERS FOR THE SA0/SA1 TESTS                         PAL03200
  200 IPCTR=0                                                           PAL03210
      CALL TEST(LPHASE,LBUF,TITLE,IC,IL,ILE,ISYM,IBUF,ITYPE,IPCTR,      PAL03220
     1          LERR,ISAF,IPCTR1,.FALSE.,.FALSE.)                       PAL03230
      IPCTR0=IPCTR                                                      PAL03240
C  LOOPING FOR SA1 TEST                                                 PAL03250
      DO 210 IPCTR1=1,IPCTR0                                            PAL03260
      LSA11=.TRUE.                                                      PAL03270
      CALL TEST(LPHASE,LBUF,TITLE,IC,IL,ILE,ISYM,IBUF,ITYPE,IPCTR,      PAL03280
     1          LERR,ISAF,IPCTR1,LSA11,.FALSE.)                         PAL03290
  210 CONTINUE                                                          PAL03300
```

FILE: PAL24 FORTRAN A NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

```
      ISA1=ISAF                                                          PAL03310
C   LOOPING FOR SA0 TEST                                                 PAL03320
      DO 215 IPCTR1=1,IPCTR0                                             PAL03330
      LSA01=.TRUE.                                                       PAL03340
      CALL TEST(LPHASE,LBUF,TITILE,IC,IL,ILE,ISYM,IBUF,ITYPE,IPCTR,      PAL03350
     1          LERR,ISAF,IPCTR1,.FALSE.,LSA01)                          PAL03360
  215 CONTINUE                                                           PAL03370
      ISA0=ISAF-ISA1                                                     PAL03380
      IFAULT=(ISAF*100)/(2*IPCTR0)                                       PAL03390
      WRITE(POF,220) ISA1                                                PAL03400
  220 FORMAT(/,' NUMBER OF STUCK AT ONE  (SA1) FAULTS ARE =', I3)        PAL03410
      WRITE(POF,225) ISA0                                                PAL03420
  225 FORMAT(/,' NUMBER OF STUCK AT ZERO (SA0) FAULTS ARE =', I3)        PAL03430
      WRITE(POF,230)IFAULT                                               PAL03440
  230 FORMAT(/,' PRODUCT   TERM   COVERAGE                =' I3,'%',//)  PAL03450
      GO TO 135                                                          PAL03460
C                                                                        PAL03470
      END                                                                PAL03480
C                                                                        PAL03490
C************************************************************************PAL03500
C                                                                        PAL03510
C                                                                        PAL03520
C THIS SUBROUTINE GENERATES JEDEC FORMATTED OUTPUT FOR INTERFACING       PAL03530
C WITH DATA I/O PROGRAMMER                                               PAL03540
      SUBROUTINE PLOTF                                                   PAL03550
      IMPLICIT INTEGER (A-Z)                                             PAL03560
      LOGICAL LFUSES(40,80)                                              PAL03570
      INTEGER IPBUF(40),ZERO,ONE                                         PAL03580
      INTEGER ISUM(4),IADR,STX,ETX,IDEC(4),IPT,IINP,J1,J2                PAL03590
      INTEGER IDECIO(4),ISUMV(4),ISUMIO(4),BUFIO(40)                     PAL03600
      COMMON /LUNIT/PMS,POF,PDF                                          PAL03610
      COMMON /IPT/IPT                                                    PAL03620
      COMMON /LFUSES/LFUSES                                              PAL03630
      COMMON /SUM/ISUM,IDEC,IPBUF,BUFIO                                  PAL03640
      DATA ZERO/'0'/,ONE/'1'/                                            PAL03650
      IADR=0                                                             PAL03660
      STX=2                                                              PAL03670
      ETX=3                                                              PAL03680
      ISUM(2)=0                                                          PAL03690
      ISUM(4)=230                                                        PAL03700
      WRITE(PDF,10) STX                                                  PAL03710
   10 FORMAT(' ',A1,'*F0*')                                              PAL03720
      DO 300 IPT=1,80                                                    PAL03730
      DO 50 IINP=1,40                                                    PAL03740
      IF(LFUSES(IINP,IPT)) IPBUF(IINP)=ONE                               PAL03750
      IF(.NOT.(LFUSES(IINP,IPT))) IPBUF(IINP)=ZERO                       PAL03760
   50 CONTINUE                                                           PAL03770
      IF(LFUSES(1,IPT)) GO TO 100                                        PAL03780
      IF(.NOT.LFUSES(2,IPT)) GO TO 250                                   PAL03790
  100 IDEC(4)=IADR                                                       PAL03800
      DO 150 J=1,3                                                       PAL03810
      J1=5-J                                                             PAL03820
      J2=4-J                                                             PAL03830
      IDEC(J2)=IDEC(J1)/10                                               PAL03840
      IDEC(J1)=IDEC(J1)-10*IDEC(J2)                                      PAL03850
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      IDECIO(J1)=ICONV(IDEC(J1))                                        PAL03860
  150 CONTINUE                                                          PAL03870
      IDECIO(1)=ICONV(IDEC(1))                                          PAL03880
      CALL SUMCHK                                                       PAL03890
      WRITE(PDF,201) IDECIO,IPBUF                                       PAL03900
  201 FORMAT(' L',4A1,' ',10(4A1,' '),'*')                              PAL03910
  250 IADR=IADR+40                                                      PAL03920
  300 CONTINUE                                                          PAL03930
      ISUMIO(1)=ICONV(ISUM(2)/16)                                       PAL03940
      ISUM(2)=MOD(ISUM(2),16)                                           PAL03950
      ISUMIO(2)=ICONV(ISUM(2))                                          PAL03960
      ISUMIO(3)=ICONV(ISUM(4)/16)                                       PAL03970
      ISUM(4)=MOD(ISUM(4),16)                                           PAL03980
      ISUMIO(4)=ICONV(ISUM(4))                                          PAL03990
      WRITE(PDF,400) ETX,ISUMIO                                         PAL04000
  400 FORMAT(' *',A1,4A1,'*',/)                                         PAL04010
      RETURN                                                            PAL04020
      END                                                               PAL04030
C                                                                       PAL04040
C                                                                       PAL04050
C                                                                       PAL04060
      SUBROUTINE SUMCHK                                                 PAL04070
      IMPLICIT INTEGER(A-Z)                                             PAL04080
      LOGICAL LFUSES(40,80)                                             PAL04090
      INTEGER IPBUF(40), BUFIO(40)                                      PAL04100
      INTEGER ISUM(4), IDEC(4)                                          PAL04110
      COMMON /IPT/IPT                                                   PAL04120
      COMMON /LFUSES/ LFUSES                                            PAL04130
      COMMON /SUM/ ISUM, IDEC,IPBUF,BUFIO                               PAL04140
      DO 50 J=1,40                                                      PAL04150
      IF(LFUSES(J,IPT)) BUFIO(J)=49                                     PAL04160
      IF(.NOT.LFUSES(J,IPT)) BUFIO(J)=46                                PAL04170
      ISUM(4)=ISUM(4)+BUFIO(J)                                          PAL04180
      IF(ISUM(4).GE.256) ISUM(2)=ISUM(2)+1                              PAL04190
      ISUM(4)=MOD(ISUM(4),256)                                          PAL04200
   50 CONTINUE                                                          PAL04210
      DO 100 J=1,4                                                      PAL04220
      ISUM(4)=ISUM(4)+IDEC(J)+48                                        PAL04230
      IF(ISUM(4).GE.256) ISUM(2)=ISUM(2)+1                              PAL04240
      ISUM(4)=MOD(ISUM(4),256)                                          PAL04250
  100 CONTINUE                                                          PAL04260
      ISUM(4)=ISUM(4)+173                                               PAL04270
      ISUM(2)=ISUM(2)+1                                                 PAL04280
      IF(ISUM(4).GE.256) ISUM(2)=ISUM(2)+1                              PAL04290
      ISUM(4)=MOD(ISUM(4),256)                                          PAL04300
      RETURN                                                            PAL04310
      END                                                               PAL04320
C*************************************************                      PAL04330
C                                                                       PAL04340
      INTEGER FUNCTION ICONV(K)                                         PAL04350
      IMPLICIT INTEGER (A-Z)                                            PAL04360
      DATA A/'0'/,B/'1'/,C/'2'/,D/'3'/,E/'4'/,F/'5'/,G/'6'/,H/'7'/      PAL04370
      DATA I/'8'/,J/'9'/,X/'A'/,L/'B'/,M/'C'/,N/'D'/,O/'E'/,P/'F'/      PAL04380
      IF(K.EQ.0) ICONV=A                                                PAL04390
      IF(K.EQ.1) ICONV=B                                                PAL04400
```

```
      IF(K.EQ.2) ICONV=C                                                PAL04410
      IF(K.EQ.3) ICONV=L                                                PAL04420
      IF(K.EQ.4) ICONV=E                                                PAL04430
      IF(K.EQ.5) ICONV=F                                                PAL04440
      IF(K.EQ.6) ICONV=G                                                PAL04450
      IF(K.EQ.7) ICONV=H                                                PAL04460
      IF(K.EQ.8) ICONV=I                                                PAL04470
      IF(K.EQ.9) ICONV=J                                                PAL04480
      IF(K.EQ.10)ICONV=X                                                PAL04490
      IF(K.EQ.11)ICONV=L                                                PAL04500
      IF(K.EQ.12)ICONV=M                                                PAL04510
      IF(K.EQ.13)ICONV=N                                                PAL04520
      IF(K.EQ.14)ICONV=O                                                PAL04530
      IF(K.EQ.15)ICONV=P                                                PAL04540
      RETURN                                                            PAL04550
      END                                                               PAL04560
C*****************************************************                PAL04570
C                                                                       PAL04580
C                                                                       PAL04590
      SUBROUTINE INITLZ(INAME,ITYPE,LFUSES,IC,IL,IBLOW,IPCTR)           PAL04600
C     THIS SUBROUTINE INITIALIZIES VARIABLES AND MATCHES PAL PART       PAL04610
C      NUMBER WITH ITYPE                                                PAL04620
      IMPLICIT INTEGER (A-Z)                                            PAL04630
      INTEGER INAME(5),INFO(6,14)                                       PAL04640
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LFUSES(40,80), PAL04650
     1        LMATCH,LXOR                                               PAL04660
      COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR           PAL04670
      COMMON /PGE/ IPAGE(80,200)                                        PAL04680
      DATA INFO/                                                        PAL04690
     1     '1','2','L','1','0',1,                                       PAL04700
     2     '1','4','L','8',' ',2,                                       PAL04710
     3     '1','6','L','6',' ',3,                                       PAL04720
     4     '1','8','L','4',' ',4,                                       PAL04730
     5     '2','0','L','2',' ',5,                                       PAL04740
     6     '2','0','C','1',' ',6,                                       PAL04750
     7     '2','0','L','1','0',7,                                       PAL04760
     8     '2','0','X','1','0',8,                                       PAL04770
     9     '2','0','X','8',' ',9,                                       PAL04780
     A     '2','0','X','4',' ',10,                                      PAL04790
     B     '2','0','L','8',' ',11,                                      PAL04800
     C     '2','0','R','8',' ',12,                                      PAL04810
     D     '2','0','R','6',' ',13,                                      PAL04820
     E     '2','0','R','4',' ',14/                                      PAL04830
C     INITIALIZE LFUSES ARRAY (FUSE ARRAY)                              PAL04840
      DO 20 J=1,80                                                      PAL04850
         DO 20 I=1,40                                                   PAL04860
   20       LFUSES(I,J)=.FALSE.                                         PAL04870
C     INITIALIZE IBLOW (NUMBER OF FUSES BLOWN)                          PAL04880
      IBLOW=0                                                           PAL04890
      IPCTR=0                                                           PAL04900
C     INITIALIZE IC AND IL (COLUMN AND LINE POINTERS)                   PAL04910
      IC=0                                                              PAL04920
      IL=1                                                              PAL04930
C     INITIALIZE ITYPE (PAL PART TYPE)                                  PAL04940
      ITYPE=0                                                           PAL04950
```

```
FILE: PAL24     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

C      ITYPE IS ASSIGNED THE FOLLOWING VALUES FOR THESE PAL TYPES:          PAL04960
C      PAL12L10 =  1    PAL14L8  =  2    PAL16L6  =  3    PAL18L4  =  4    PAL04970
C      PAL20L2  =  5    PAL20C1  =  6    PAL20L10 =  7    PAL20X10 =  8    PAL04980
C      PAL20X8  =  9    PAL20X4  = 10    PAL20L8  = 11    PAL20R8  = 12    PAL04990
C      PAL20R6  = 13    PAL20R4  = 14                                      PAL05000
       DO 40 J=1,14                                                        PAL05010
          LMATCH=.TRUE.                                                    PAL05020
          DO 30 I=1,4                                                      PAL05030
   30        IF(INAME(I).NE.INFO(I,J)) LMATCH=.FALSE.                      PAL05040
          IF(LMATCH) ITYPE=INFO(6,J)                                       PAL05050
          IF (LMATCH) GO TO 50                                             PAL05060
   40  CONTINUE                                                            PAL05070
       IF(ITYPE.EQ.0) RETURN                                               PAL05080
   50  CALL INCR(IC,IL)                                                    PAL05090
       RETURN                                                              PAL05100
       END                                                                 PAL05110
C                                                                          PAL05120
C*************************************************************************PAL05130
C                                                                          PAL05140
       SUBROUTINE GETSYM(LPHASE,ISYM,J,IC,IL)                              PAL05150
C      THIS SUBROUTINE GETS THE PIN NAME, / IF COMPLEMENT LOGIC, AND       PAL05160
C       THE FOLLOWING OPERATION SYMBOL IF ANY                              PAL05170
       IMPLICIT INTEGER (A-Z)                                              PAL05180
       INTEGER ISYM(8,24)                                                  PAL05190
       LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LPHASE(24)  PAL05200
       COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR             PAL05210
       COMMON /PGE/ IPAGE(80,200)                                          PAL05220
       DATA IBLANK/' '/                                                    PAL05230
       IF( .NOT.(LLEFT.OR.LAND.OR.LOR.OR.LEQUAL.OR.LRIGHT) )  GO TO 10     PAL05240
       CALL INCR(IC,IL)                                                    PAL05250
   10  LPHASE(J)=(.NOT.LSLASH)                                             PAL05260
       IF(LPHASE(J)) GO TO 15                                              PAL05270
       CALL INCR(IC,IL)                                                    PAL05280
   15  DO 20 I=1,8                                                         PAL05290
   20      ISYM(I,J)=IBLANK                                                PAL05300
   25  DO 30 I=1,7                                                         PAL05310
   30      ISYM(I,J)=ISYM(I+1,J)                                           PAL05320
       ISYM(8,J)=IPAGE(IC,IL)                                              PAL05330
       CALL INCR(IC,IL)                                                    PAL05340
       IF( LLEFT.OR.LBLANK.OR.LAND.OR.LOR.OR.LRIGHT.OR.LEQUAL ) RETURN     PAL05350
       GO TO 25                                                            PAL05360
       END                                                                 PAL05370
C                                                                          PAL05380
C*************************************************************************PAL05390
C                                                                          PAL05400
       SUBROUTINE INCR(IC,IL)                                              PAL05410
C      THIS SUBROUTINE INCREMENTS COLUMN AND LINE POINTERS                 PAL05420
C       BLANKS AND CHARACTERS AFTER ';' ARE IGNORED                        PAL05430
       IMPLICIT INTEGER (A-Z)                                              PAL05440
       LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LXOR1       PAL05450
       COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR             PAL05460
       COMMON /PGE/ IPAGE(80,200)                                          PAL05470
       COMMON /LUNIT/ PMS,POF,PDF                                          PAL05480
       DATA IBLANK/' '/,ILEFT/'('/,IAND/'*'/,IOR/'+'/,COMENT/';'/,         PAL05490
      1         ISLASH/'/'/,IEQUAL/'='/,IRIGHT/')'/,ICOLON/':'/           PAL05500
```

```
FILE: PAL24     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      LBLANK=.FALSE.                                                    PAL05510
      LXOR=.FALSE.                                                      PAL05520
      LXOR1=.FALSE.                                                     PAL05530
   10 IC=IC+1                                                           PAL05540
      IF( IC.LE.79.AND.IPAGE(IC,IL).NE.COMENT ) GO TO 30                PAL05550
      IL=IL+1                                                           PAL05560
      IF(IL.LE.200) GO TO 20                                            PAL05570
          WRITE(PMS,15)                                                 PAL05580
   15     FORMAT(/,' SOURCE FILE EXCEEDS 200 LINES OR MISSING',         PAL05590
     1             ' DESCRIPTION OR FUNCTION TABLE KEY WORD')           PAL05600
          STOP                                                          PAL05610
   20 IC=0                                                              PAL05620
      GO TO 10                                                          PAL05630
   30 IF(IPAGE(IC,IL).NE.IBLANK) GO TO 31                               PAL05640
      LBLANK=.TRUE.                                                     PAL05650
      GO TO 10                                                          PAL05660
   31 IF(IPAGE(IC,IL).NE.ICOLON) GO TO 32                               PAL05670
      IF(LXOR) GO TO 33                                                 PAL05680
      LXOR1=.TRUE.                                                      PAL05690
      GO TO 10                                                          PAL05700
   33 LOR=.TRUE.                                                        PAL05710
      RETURN                                                            PAL05720
   32 IF( .NOT.(IPAGE(IC,IL).EQ.IOR.AND.(LXOR1)) ) GO TO 34             PAL05730
      LXOR=.TRUE.                                                       PAL05740
      GO TO 10                                                          PAL05750
   34 LLEFT =(IPAGE(IC,IL).EQ.ILEFT)                                    PAL05760
      LAND  =(IPAGE(IC,IL).EQ.IAND)                                     PAL05770
      LOR   =(IPAGE(IC,IL).EQ.IOR)                                      PAL05780
      LSLASH=(IPAGE(IC,IL).EQ.ISLASH)                                   PAL05790
      LEQUAL=(IPAGE(IC,IL).EQ.IEQUAL)                                   PAL05800
      LRIGHT=(IPAGE(IC,IL).EQ.IRIGHT)                                   PAL05810
      RETURN                                                            PAL05820
      END                                                               PAL05830
C                                                                       PAL05840
C*************************************************************************PAL05850
C                                                                       PAL05860
      SUBROUTINE MATCH(IMATCH,IBUF,ISYM)                                PAL05870
C     THIS SUBROUTINE FINDS A MATCH BETWEEN THE PIN NAME IN THE EQUATIONPAL05880
C      AND THE PIN NAME IN THE PIN LIST OR FUNCTION TABLE PIN LIST      PAL05890
      IMPLICIT INTEGER (A-Z)                                            PAL05900
      INTEGER IBUF(8,24),ISYM(8,24)                                     PAL05910
      LOGICAL LMATCH                                                    PAL05920
      IMATCH=0                                                          PAL05930
      DO 20 J=1,24                                                      PAL05940
          LMATCH=.TRUE.                                                 PAL05950
          DO 10 I=1,8                                                   PAL05960
   10         LMATCH=LMATCH.AND.(IBUF(I,1).EQ.ISYM(I,J))                PAL05970
          IF(LMATCH) IMATCH=J                                           PAL05980
   20     CONTINUE                                                      PAL05990
      RETURN                                                            PAL06000
      END                                                               PAL06010
C                                                                       PAL06020
C*************************************************************************PAL06030
C                                                                       PAL06040
      SUBROUTINE IXLATE(IINPUT,LPHASE,IMATCH,LBUF,ITYPE)                PAL06050
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

C      THIS SUBROUTINE FINDS A MATCH BETWEEN INPUT PIN NUMBER AND          PAL06060
C       THE INPUT LINE NUMBER FOR A SPECIFIC PAL.  ADD 1 TO THE INPUT      PAL06070
C       LINE NUMBER IF THE PIN IS A COMPLEMENT                             PAL06080
       IMPLICIT INTEGER (A-Z)                                             PAL06090
       INTEGER ITABLE(24,14)                                              PAL06100
       LOGICAL LPHASE(24),LBUF(24)                                        PAL06110
       DATA    ITABLE/                                                    PAL06120
      1 3,1,5,9,13,17,21,25,29,33,37,0,39, 0, 0, 0, 0, 0, 0, 0, 0,0,0,PAL06130
      2 3,1,5,9,13,17,21,25,29,33,37,0,39,35, 0, 0, 0, 0, 0, 0, 0, 0,7,0,PAL06140
      3 3,1,5,9,13,17,21,25,29,33,37,0,39,35,31, 0, 0, 0, 0, 0, 0,11,7,0,PAL06150
      4 3,1,5,9,13,17,21,25,29,33,37,0,39,35,31,27, 0, 0, 0, 0,15,11,7,0,PAL06160
      5 3,1,5,9,13,17,21,25,29,33,37,0,39,35,31,27,23, 0, 0,19,15,11,7,0,PAL06170
      6 3,1,5,9,13,17,21,25,29,33,37,0,39,35,31,27,23, 0, 0,19,15,11,7,0,PAL06180
      7 3,1,5,9,13,17,21,25,29,33,37,0,39, 0,35,31,27,23,19,15,11, 7,0,0,PAL06190
      8 0,1,5,9,13,17,21,25,29,33,37,0, 0,39,35,31,27,23,19,15,11, 7,3,0,PAL06200
      9 0,1,5,9,13,17,21,25,29,33,37,0, 0,39,35,31,27,23,19,15,11, 7,3,0,PAL06210
      A 0,1,5,9,13,17,21,25,29,33,37,0, 0,39,35,31,27,23,19,15,11, 7,3,0,PAL06220
      B 3,1,5,9,13,17,21,25,29,33,37,0,39,35, 0,31,27,23,19,15,11, 0,7,0,PAL06230
      C 0,1,5,9,13,17,21,25,29,33,37,0, 0,39,35,31,27,23,19,15,11, 7,3,0,PAL06240
      D 0,1,5,9,13,17,21,25,29,33,37,0, 0,39,35,31,27,23,19,15,11, 7,3,0,PAL06250
      E 0,1,5,9,13,17,21,25,29,33,37,0, 0,39,35,31,27,23,19,15,11, 7,3,0/PAL06260
       IBUBL=0                                                           PAL06270
       IF( ((     LPHASE(IMATCH)).AND.(.NOT.LBUF(1))).OR.               PAL06280
      1    ((.NOT.LPHASE(IMATCH)).AND.(     LBUF(1))) ) IBUBL=1         PAL06290
       IINPUT=ITABLE(IMATCH,ITYPE)+IBUBL                                 PAL06300
       RETURN                                                            PAL06310
       END                                                               PAL06320
C                                                                        PAL06330
C************************************************************************PAL06340
C                                                                        PAL06350
       SUBROUTINE ECHO(IPAL,INAME,REST,PATNUM,TITLE,COMP)                PAL06360
C      THIS SUBROUTINE PRINTS THE PAL DESIGN SPECIFICATION INPUT FILE    PAL06370
       IMPLICIT INTEGER (A-Z)                                            PAL06380
       INTEGER IPAL(3),INAME(5),REST(72),PATNUM(80),TITLE(80),COMP(80)   PAL06390
       COMMON /PGE/ IPAGE(80,200)                                        PAL06400
       COMMON /LUNIT/ PMS,POF,PDF                                        PAL06410
       COMMON /FTEST/ IFUNCT,IDESC,IEND                                  PAL06420
       DATA IBLANK/' '/                                                  PAL06430
       WRITE(POF,5) IPAL,INAME,REST,PATNUM,TITLE,COMP                    PAL06440
     5 FORMAT(/,' ',3A1,5A1,72A1,/,' ',80A1,/,' ',80A1,/,' ',80A1)       PAL06450
       DO 20 IL=1,IEND                                                   PAL06460
          IC=81                                                          PAL06470
    10    IC=IC-1                                                       PAL06480
          IF( IPAGE(IC,IL).EQ.IBLANK.AND.IC.GT.1 ) GO TO 10             PAL06490
          WRITE(POF,15) (IPAGE(I,IL),I=1,IC)                            PAL06500
    15    FORMAT(' ',80A1)                                              PAL06510
    20 CONTINUE                                                         PAL06520
       RETURN                                                           PAL06530
       END                                                              PAL06540
C                                                                       PAL06550
C************************************************************************PAL06560
C                                                                       PAL06570
       SUBROUTINE CAT                                                   PAL06580
C      THIS SUBROUTINE PRINTS THE PALASM CATALOG                        PAL06590
       IMPLICIT INTEGER (A-Z)                                           PAL06600
```

```
FILE: PAL24     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      COMMON /LUNIT/ PMS,POF,PDF                                        PAL06610
      WRITE(PMS,10)                                                     PAL06620
   10 FORMAT(/,' THIS PALASM AIDS THE USER IN THE DESIGN AND',          PAL06630
     1          ' PROGRAMMING OF THE',/,' SERIES 24 PAL FAMILY.  THE',  PAL06640
     2          ' FOLLOWING OPTIONS ARE PROVIDED:',                     PAL06650
     3        /,'     ECHO (E)      - PRINTS THE PAL DESIGN',          PAL06660
     4          ' SPECIFICATION',                                       PAL06670
     5       //,'     PINOUT (O)    - PRINTS THE PINOUT OF THE PAL',    PAL06680
     6       //,'     SIMULATE (T) - EXERCISES THE FUNCTION TABLE',     PAL06690
     7          ' VECTORS IN THE LOGIC',/,'                    ',      PAL06700
     8          ' EQUATIONS AND GENERATES TEST VECTORS',                PAL06710
     9       //,'     PLOT (P)      - PRINTS THE ENTIRE FUSE PLOT')     PAL06720
      WRITE(PMS,20)                                                     PAL06730
   20 FORMAT(/,'     BRIEF (B)     - PRINTS ONLY THE USED PRODUCT LINES', PAL06740
     1          ' OF THE FUSE PLOT',/,'                    PHANTOM',   PAL06750
     2          ' FUSES ARE OMITTED',                                   PAL06760
     3       //,'     JEDEC (J)     - GENERATES FUSE OUTPUT FOR DATA I/O', PAL06770
     4          ' PROGRAMMERS',                                         PAL06780
     5       //,'     HEX (H)       - GENERATES HEX PROGRAMMING FORMAT',  PAL06790
     6       //,'     SHORT (S)     - GENERATES HEX PROGRAMMING FORMAT',  PAL06800
     7       //,'     BHLF (L)      - GENERATES BHLF PROGRAMMING FORMAT', PAL06810
     8       //,'     BNPF (N)      - GENERATES BNPF PROGRAMMING FORMAT', PAL06820
     9       //,'     CATALOG (C)   - PRINTS THE PALASM CATALOG',       PAL06830
     A       //,'     QUIT (Q)      - EXIT PALASM',                     PAL06840
     B       //,'     FAULT (F)     - FAULT TESTING')                   PAL06850
      RETURN                                                            PAL06860
      END                                                               PAL06870
C                                                                       PAL06880
C***********************************************************************PAL06890
C                                                                       PAL06900
      SUBROUTINE PINOUT(IPAL,INAME,TITLE)                               PAL06910
C     THIS SUBROUTINE PRINTS THE PINOUT OF THE PAL                      PAL06920
      IMPLICIT INTEGER (A-Z)                                            PAL06930
      INTEGER IPAL(3),INAME(5),TITLE(80),PIN(12,24),IIN(8,2)            PAL06940
      COMMON /PGE/ IPAGE(80,200)                                        PAL06950
      COMMON /LUNIT/ PMS,POF,PDF                                        PAL06960
      DATA IBLANK/' '/,ISTAR/'*'/                                       PAL06970
      DO 10 J=1,24                                                      PAL06980
         DO 5 I=1,12                                                    PAL06990
    5       PIN(I,J)=IBLANK                                             PAL07000
   10 CONTINUE                                                          PAL07010
   15 DO 25 J=1,2                                                       PAL07020
         DO 20 I=1,8                                                    PAL07030
   20       IIN(I,J)=IBLANK                                            PAL07040
   25 CONTINUE                                                          PAL07050
      IIN(2,1)=IPAL(1)                                                  PAL07060
      IIN(4,1)=IPAL(2)                                                  PAL07070
      IIN(6,1)=IPAL(3)                                                  PAL07080
      IIN(1,2)=INAME(1)                                                 PAL07090
      IIN(3,2)=INAME(2)                                                 PAL07100
      IIN(5,2)=INAME(3)                                                 PAL07110
      IIN(7,2)=INAME(4)                                                 PAL07120
      IIN(8,2)=INAME(5)                                                 PAL07130
      J=0                                                               PAL07140
      IL=0                                                              PAL07150
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

   30 IC=0                                                                  PAL07160
      IL=IL+1                                                               PAL07170
   35 IC=IC+1                                                               PAL07180
   40 IF( IC.GT.80 ) GO TO 30                                               PAL07190
      IF( IPAGE(IC,IL).EQ.IBLANK ) GO TO 35                                 PAL07200
      J=J+1                                                                 PAL07210
      IF(J.GT.24) GO TO 60                                                  PAL07220
      DO 55 I=1,12                                                          PAL07230
           PIN(I,J)=IPAGE(IC,IL)                                            PAL07240
           IC=IC+1                                                          PAL07250
           IF( IC.GT.80 ) GO TO 40                                          PAL07260
           IF( IPAGE(IC,IL).EQ.IBLANK ) GO TO 40                            PAL07270
   55      CONTINUE                                                         PAL07280
   60 DO 75 J=1,12                                                          PAL07290
           II=0                                                             PAL07300
   65      II=II+1                                                          PAL07310
           IF(II.EQ.13) GO TO 75                                            PAL07320
           IF( PIN(II,J).NE.IBLANK ) GO TO 65                               PAL07330
           I=13                                                             PAL07340
   70      I=I-1                                                            PAL07350
           II=II-1                                                          PAL07360
           PIN(I,J)=PIN(II,J)                                               PAL07370
           PIN(II,J)=IBLANK                                                 PAL07380
           IF(II.NE.1) GO TO 70                                             PAL07390
   75 CONTINUE                                                              PAL07400
      WRITE(POF,76) TITLE                                                   PAL07410
   76 FORMAT(/,' ',80A1)                                                    PAL07420
      WRITE(POF,78) ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,       PAL07430
     1              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,       PAL07440
     2              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,       PAL07450
     3              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR        PAL07460
   78 FORMAT(/,' ',18X,14A1,3X,14A1,                                        PAL07470
     1       /,' ',18X,A1,13X,A1,1X,A1,13X,A1)                              PAL07480
      JJ=24                                                                 PAL07490
      DO 88 J=1,12                                                          PAL07500
           WRITE(POF,80) ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR    PAL07510
   80      FORMAT(' ',15X,4A1,29X,4A1)                                      PAL07520
           WRITE(POF,81) (PIN(I,J),I=1,12),ISTAR,J,ISTAR,                   PAL07530
     1          (IIN(I,1),I=1,8),ISTAR,JJ,ISTAR,(PIN(I,JJ),I=1,12)         PAL07540
   81      FORMAT(' ',12A1,3X,A1,I2,A1,11X,8A1,10X,A1,I2,A1,3X,12A1)        PAL07550
           WRITE(POF,82) ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR    PAL07560
   82      FORMAT(' ',15X,4A1,29X,4A1)                                      PAL07570
           WRITE(POF,84) ISTAR,(IIN(I,2),I=1,8),ISTAR                       PAL07580
   84      FORMAT(' ',18X,A1,11X,8A1,10X,A1)                                PAL07590
           DO 86 II=1,2                                                     PAL07600
                DO 85 I=1,8                                                 PAL07610
   85                IIN(I,II)=IBLANK                                      PAL07620
   86      CONTINUE                                                         PAL07630
           JJ=JJ-1                                                          PAL07640
   88 CONTINUE                                                              PAL07650
      WRITE(POF,90) ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,       PAL07660
     1              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,       PAL07670
     2              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,       PAL07680
     3              ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR,ISTAR              PAL07690
   90 FORMAT(' ',18X,31A1)                                                  PAL07700
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      RETURN                                                            PAL07710
      END                                                               PAL07720
C                                                                       PAL07730
C*************************************************************************PAL07740
C                                                                       PAL07750
      SUBROUTINE PLOT(LBUF,IBUF,LFUSES,IPROD,TITLE,LDUMP,ITYPE,LPROD,   PAL07760
     1                IOP,IBLOW)                                       PAL07770
C     THIS SUBROUTINE PRODUCES THE FUSE PLOT                            PAL07780
      IMPLICIT INTEGER (A-Z)-                                           PAL07790
      INTEGER IBUF(8,24),IOUT(64),ISAVE(80,40),TITLE(80),IDATA(40)      PAL07800
      LOGICAL LBUF(24),LFUSES(40,80),LDUMP,LPROD(80)                    PAL07810
      INTEGER   STX,ETX                                                 PAL07820
      COMMON /LUNIT/ PMS,POF,PDF                                        PAL07830
      DATA ISAVE/3200*' '/,IAND/'*'/,IOR/'+'/,ISLASH/'/'/,              PAL07840
     1     IDASH/'-'/,X/'X'/,IBLANK/' '/,P/'P'/,B/'B'/,                 PAL07850
     2     D/'D'/,ZERO/'0'/,ONE/'1'/,FX/'0'/,FIDASH/'0'/                PAL07860
      DATA STX/Z02000000/,ETX/Z03000000/                                PAL07870
      IF(LDUMP) GO TO 58                                                PAL07880
      IF(ISAVE(IPROD,1).NE.IBLANK) RETURN                               PAL07890
      IF(LBUF(1)) GO TO 5                                               PAL07900
      DO 30 J=1,39                                                      PAL07910
   30      ISAVE(IPROD,J)=ISAVE(IPROD,J+1)                              PAL07920
      ISAVE(IPROD,40)=ISLASH                                            PAL07930
    5 DO 20 I=1,8                                                       PAL07940
          IF( ISAVE(IPROD,1).NE.IBLANK ) RETURN                         PAL07950
          IF( IBUF(I,1).EQ.IBLANK ) GO TO 20                            PAL07960
          DO 10 J=1,39                                                  PAL07970
   10         ISAVE(IPROD,J)=ISAVE(IPROD,J+1)                          PAL07980
          ISAVE(IPROD,40)=IBUF(I,1)                                     PAL07990
   20     CONTINUE                                                      PAL08000
      IF(ISAVE(IPROD,1).NE.IBLANK) RETURN                               PAL08010
   40 DO 50 J=1,39                                                      PAL08020
   50     ISAVE(IPROD,J)=ISAVE(IPROD,J+1)                              PAL08030
      ISAVE(IPROD,40)=IAND                                              PAL08040
      RETURN                                                            PAL08050
C     PRINT FUSE PLOT                                                   PAL08060
   58 IF(IOP.EQ.D) GO TO 62                                             PAL08070
      WRITE(POF,61) TITLE                                               PAL08080
   61 FORMAT(/,' ',80A1,//,                                             PAL08090
     1 '                    11 1111 1111 2222 2222 2233 3333 3333',/,   PAL08100
     2 '    0123 4567 8901 2345 6789 0123 4567 8901 2345 6789',/)       PAL08110
      GO TO 64                                                          PAL08120
C***** STX DETERMINES THE STARTING CHARACTER FOR DATA I/O FORMAT         PAL08130
   62 WRITE(PDF,63) STX                                                 PAL08140
   63 FORMAT(' ',A1,'*L0000'/)                                          PAL08150
   64 DO 100 I88PRO=1,73,8                                              PAL08160
          DO 94 I8PRO=1,8                                               PAL08170
              IPROD=I88PRO+I8PRO-1                                      PAL08180
              ISAVE(IPROD,40)=IBLANK                                    PAL08190
              DO 70 I=1,40                                              PAL08200
                  IF( ISAVE(IPROD,1).NE.IBLANK ) GO TO 70               PAL08210
                  DO 65 J=1,39                                          PAL08220
   65                 ISAVE(IPROD,J)=ISAVE(IPROD,J+1)                  PAL08230
                  ISAVE(IPROD,40)=IBLANK                                PAL08240
   70             CONTINUE                                              PAL08250
```

```
FILE: PAL24     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

              DO 75 I=1,24                                                    PAL08260
                 IOUT(I+40)=ISAVE(IPROD,I)                                    PAL08270
   75         CONTINUE                                                        PAL08280
              IF( ISAVE(IPROD,25).NE.IBLANK ) IOUT(64)=IDASH                  PAL08290
              DO 80 I=1,40                                                    PAL08300
                 IOUT(I)=X                                                    PAL08310
                 IF(LFUSES(I,IPROD)) IOUT(I)=IDASH                            PAL08320
   80         CONTINUE                                                        PAL08330
              CALL FANTOM(ITYPE,IOP,IOUT,IPROD,I8PRO)                         PAL08340
              IF(IOP.NE.D) GO TO 85                                           PAL08350
              K=0                                                             PAL08360
   81         DO 82 I=1,40                                                    PAL08370
                 IF((IOUT(I).EQ.FX).OR.(IOUT(I).EQ.FIDASH)) GO TO 82          PAL08380
                 K=K+1                                                        PAL08390
                 IF(IOUT(I).EQ.X)      IDATA(K)=ZERO                          PAL08400
                 IF(IOUT(I).EQ.IDASH) IDATA(K)=ONE                            PAL08410
   82         CONTINUE                                                        PAL08420
              DO 83 I=1,40                                                    PAL08430
                 IF( (IOUT(I).EQ.X).OR.(IOUT(I).EQ.IDASH) ) GO TO 86          PAL08440
   83         CONTINUE                                                        PAL08450
              GO TO 94                                                        PAL08460
   86         WRITE(PDF,84) IDATA                                             PAL08470
   84         FORMAT(' ',40(A1,' '))                                          PAL08480
              GO TO 94                                                        PAL08490
   85         IPROD=IPROD-1                                                   PAL08500
              IF( (IOP.EQ.P).OR.(IOP.EQ.B.AND.(LPROD(IPROD+1))) )             PAL08510
     1        WRITE(POF,90) IPROD,IOUT                                        PAL08520
   90         FORMAT(' ',I2,10(' ',4A1),' ',24A1)                             PAL08530
   94         CONTINUE                                                        PAL08540
            WRITE(POF,96)                                                     PAL08550
   96       FORMAT(1X)                                                       PAL08560
  100       CONTINUE                                                        PAL08570
        IF(IOP.NE.D) GO TO 105                                                PAL08580
        WRITE(PDF,101) ETX                                                    PAL08590
  101   FORMAT(' ',A1)                                                       PAL08600
        RETURN                                                                PAL08610
  105   WRITE(POF,110)                                                       PAL08620
  110   FORMAT(/,                                                            PAL08630
       1' LEGEND:  X : FUSE NOT BLOWN (L,N,0)    - : FUSE BLOWN    (H,P,1)')PAL08640
        IF(IOP.EQ.P) WRITE(POF,111)                                           PAL08650
  111   FORMAT(                                                              PAL08660
       1'           0 : PHANTOM FUSE    (L,N,0)    O : PHANTOM FUSE (H,P,1)')PAL08670
        WRITE(POF,112) IBLOW                                                  PAL08680
  112   FORMAT(/,' NUMBER OF FUSES BLOW = ',I4)                              PAL08690
        WRITE(POF,113)                                                        PAL08700
  113   FORMAT(//)                                                           PAL08710
        RETURN                                                                PAL08720
        END                                                                   PAL08730
C                                                                             PAL08740
C*****************************************************************************PAL08750
C                                                                             PAL08760
      SUBROUTINE HEX(LFUSES,IOP)                                              PAL08770
C     THIS SUBROUTINE GENERATES HEX PROGRAMMING FORMATS                       PAL08780
      IMPLICIT INTEGER (A-Z)                                                  PAL08790
      INTEGER ITEMP(80),ZTABL1(32),ZTABL2(16),ZCSUM(4)                        PAL08800
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      LOGICAL LFUSES(40,80)                                              PAL08810
      INTEGER   SOH,STX,ETX,BEL                                          PAL08820
      COMMON /LUNIT/PMS,POF,PDF                                          PAL08830
      DATA H/'H'/,S/'S'/,IBLANK/' '/,                                    PAL08840
     1     ZTABL1/'00','01','02','03','04','05','06','07',              PAL08850
     2            '08','09','0A','0B','0C','0D','0E','0F',              PAL08860
     3            '10','11','12','13','14','15','16','17',              PAL08870
     4            '18','19','1A','1B','1C','1D','1E','1F'/,             PAL08880
     5     ZTABL2/'0','1','2','3','4','5','6','7',                      PAL08890
     6            '8','9','A','B','C','D','E','F'/                      PAL08900
      DATA SOH/Z01000000/,STX/Z02000000/,                                PAL08910
     +   ETX/Z03000000/,BEL/Z07000000/                                   PAL08920
      CSUM=0                                                             PAL08930
      IF(IOP.EQ.H) WRITE(PDF,10)                                         PAL08940
   10 FORMAT(//,80(' '),///)                                             PAL08950
C***** NOTE: SOME PROM PROGRAMMERS NEED A START CHARACTER.               PAL08960
C*****       THIS PROGRAM OUTPUTS AN STX FOR THE DATA I/O MODEL 9       PAL08970
C*****         (USE SOH FOR MODEL 5)                                    PAL08980
      WRITE(PDF,5) BEL,BEL,BEL,BEL,BEL,BEL,BEL,STX,SOH                   PAL08990
    5 FORMAT(' ',9A1)                                                    PAL09000
      DO 40 I=1,41,40                                                    PAL09010
      INC=I-1                                                            PAL09020
        DO 40 IPROD=1,7,2                                                PAL09030
          DO 20 J=1,2                                                    PAL09040
              DO 20 IINPUT=1,40                                          PAL09050
              IHEX=0                                                     PAL09060
              ISUM2=IPROD + J-1 + INC                                    PAL09070
              IF(LFUSES(IINPUT,ISUM2 +  0 )) IHEX=IHEX+1                 PAL09080
              IF(LFUSES(IINPUT,ISUM2 +  8 )) IHEX=IHEX+2                 PAL09090
              IF(LFUSES(IINPUT,ISUM2 + 16 )) IHEX=IHEX+4                 PAL09100
              IF(LFUSES(IINPUT,ISUM2 + 24 )) IHEX=IHEX+8                 PAL09110
              IF(LFUSES(IINPUT,ISUM2 + 32 )) IHEX=IHEX+16                PAL09120
              CSUM=CSUM+IHEX                                             PAL09130
              ISUMX=IINPUT+(40*(J-1))                                    PAL09140
   20         ITEMP(ISUMX)=ZTABL1(IHEX+1)                                PAL09150
        IF(IOP.EQ.H) WRITE(PDF,60) ITEMP                                 PAL09160
   60   FORMAT(4(' ',20(A2,' '),',',/))                                  PAL09170
   40   IF(IOP.EQ.S) WRITE(PDF,61) ITEMP                                 PAL09180
   61   FORMAT(4(' ',20A2,',',/))                                        PAL09190
      IF(IOP.EQ.H) WRITE(PDF,70)                                         PAL09200
   70 FORMAT(//,80(' '),///)                                             PAL09210
      WRITE(PDF,80) ETX                                                  PAL09220
   80 FORMAT(' ',A1)                                                     PAL09230
C     CONVERT DECIMAL CHECK SUM INTO HEX CHECK SUM                       PAL09240
      DO 85 I=1,4                                                        PAL09250
           ZTEMP=CSUM-16*(CSUM/16)                                       PAL09260
           ZCSUM(5-I)=ZTABL2(ZTEMP+1)                                    PAL09270
           CSUM=CSUM/16                                                  PAL09280
   85 CONTINUE                                                           PAL09290
     / IF(ZCSUM(1).EQ.ZTABL2(1)) ZCSUM(1)=IBLANK                         PAL09300
      WRITE(PMS,90) ZCSUM(1),ZCSUM(2),ZCSUM(3),ZCSUM(4)                  PAL09310
   90 FORMAT(/,' HEX CHECK SUM = ',4A1)                                  PAL09320
      RETURN                                                             PAL09330
      END                                                                PAL09340
C                                                                        PAL09350
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

C*************************************************************************PAL09360
C                                                                         PAL09370
      BLOCK DATA                                                          PAL09380
      IMPLICIT INTEGER (A-Z)                                              PAL09390
      COMMON /BLK/ PR8X10(10,14),PROD8(8,11),PRODLN(40,7)                 PAL09400
      DATA PR8X10/                                                        PAL09410
     1      4, 4, 4, 4, 4, 4, 4, 4, 4, 4,                                 PAL09420
     2      3, 6, 5, 5, 5, 5, 5, 5, 6, 3,                                 PAL09430
     3      3, 3, 7, 7, 8, 8, 7, 7, 3, 3,                                 PAL09440
     4      3, 3, 3, 9,10,10, 9, 3, 3, 3,                                 PAL09450
     5      3, 3, 3, 3, 1, 1, 3, 3, 3, 3,                                 PAL09460
     6      2, 2, 2, 2, 1, 1, 3, 3, 3, 3,                                 PAL09470
     7     11,11,11,11,11,11,11,11,11,11,                                 PAL09480
     8     11,11,11,11,11,11,11,11,11,11,                                 PAL09490
     9     11,11,11,11,11,11,11,11,11,11,                                 PAL09500
     A     11,11,11,11,11,11,11,11,11,11,                                 PAL09510
     B      3, 1, 1, 1, 1, 1, 1, 1, 1, 3,                                 PAL09520
     C      3, 1, 1, 1, 1, 1, 1, 1, 1, 3,                                 PAL09530
     D      3, 1, 1, 1, 1, 1, 1, 1, 1, 3,                                 PAL09540
     E      3, 1, 1, 1, 1, 1, 1, 1, 1, 3/                                 PAL09550
      DATA PROD8/                                                         PAL09560
     1     1,1,1,1,1,1,1,1,                                              PAL09570
     2     2,2,2,2,2,2,2,2,                                              PAL09580
     3     3,3,3,3,3,3,3,3,                                              PAL09590
     4     4,4,3,3,3,3,3,3,                                              PAL09600
     5     5,5,3,3,3,3,3,3,                                              PAL09610
     6     5,5,5,5,3,3,3,3,                                              PAL09620
     7     6,6,6,6,3,3,3,3,                                              PAL09630
     8     6,6,3,3,3,3,3,3,                                              PAL09640
     9     7,7,7,7,7,7,3,3,                                              PAL09650
     A     7,7,7,7,3,3,3,3,                                              PAL09660
     B     1,1,1,1,3,3,3,3/                                              PAL09670
      DATA PRODLN/                                                        PAL09680
     1     40*1HX,                                                       PAL09690
     2     40*1HP,                                                       PAL09700
     3     40*1HN,                                                       PAL09710
     4     6*1HX,2*1HP,2*1HX,2*1HP,2*1HX,2*1HP,2*1HX,                    PAL09720
     4     2*1HP,2*1HX,2*1HP,2*1HX,2*1HP,2*1HX,2*1HP,                    PAL09730
     4     2*1HX,2*1HP,4*1HX,                                            PAL09740
     5     10*1HX,2*1HP,2*1HX,2*1HP,2*1HX,2*1HP,2*1HX,                   PAL09750
     5     2*1HP,2*1HX,2*1HP,2*1HX,2*1HP,8*1HX,                          PAL09760
     6     14*1HX,2*1HP,2*1HX,2*1HP,2*1HX,2*1HP,2*1HX,                   PAL09770
     6     2*1HP,12*1HX,                                                 PAL09780
     7     18*1HX,2*1HP,2*1HX,2*1HP,16*1HX/                              PAL09790
      END                                                                 PAL09800
C                                                                         PAL09810
C*************************************************************************PAL09820
C                                                                         PAL09830
      SUBROUTINE TWEEK(ITYPE,LFUSES)                                      PAL09840
C     THIS SUBROUTINE TWEEKS LFUSES (THE PROGRAMMING FUSE PLOT)           PAL09850
C      FOR HIGH AND LOW PHANTOM FUSES                                     PAL09860
      IMPLICIT INTEGER (A-Z)                                              PAL09870
      LOGICAL LFUSES(40,80),LBLANK,LLEFT,LAND,LOR,LSLASH,                 PAL09880
     1        LEQUAL,LRIGHT,LXOR                                          PAL09890
      COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR             PAL09900
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      COMMON /BLK/ PR8X10(10,14),PROD8(8,11),PRODLN(40,7)                PAL09910
      DATA P/'P'/,N/'N'/                                                 PAL09920
      FUSPTR=1                                                           PAL09930
      DO 30 OUTPUT=1,10                                                  PAL09940
         GRTYPE=PR8X10(OUTPUT,ITYPE)                                     PAL09950
         DO 30 PRLINE=1,8                                                PAL09960
            LNTYPE=PROD8(PRLINE,GRTYPE)                                  PAL09970
            DO 20 COL=1,40                                               PAL09980
               IF(PRODLN(COL,LNTYPE).EQ.P)                               PAL09990
     1            LFUSES(COL,FUSPTR)=.TRUE.                             PAL10000
               IF(PRODLN(COL,LNTYPE).EQ.N)                               PAL10010
     1            LFUSES(COL,FUSPTR)=.FALSE.                            PAL10020
   20       CONTINUE                                                     PAL10030
            FUSPTR=FUSPTR+1                                              PAL10040
   30 CONTINUE                                                          PAL10050
      RETURN                                                             PAL10060
      END                                                                PAL10070
C                                                                        PAL10080
C*************************************************************************PAL10090
C                                                                        PAL10100
      SUBROUTINE BINR(LFUSES,H,L)                                        PAL10110
C     THIS SUBROUTINE GENERATES BINARY PROGRAMMING FORMATS               PAL10120
      IMPLICIT INTEGER (A-Z)                                             PAL10130
      INTEGER ITEMP(5,10)                                                PAL10140
      LOGICAL LFUSES(40,80)                                              PAL10150
      COMMON /LUNIT/ PMS,PDF,PDF                                         PAL10160
      WRITE(PDF,10)                                                      PAL10170
   10 FORMAT(//,'                                        .',//)          PAL10180
      DO 20 I=1,41,40                                                    PAL10190
      INC=I-1                                                            PAL10200
        DO 20 IPROD=1,8                                                  PAL10210
           DO 20 J=1,31,10                                               PAL10220
             DO 15 K=1,10                                                PAL10230
               IINPUT=J+K-1                                              PAL10240
               ITEMP(1,K)=L                                              PAL10250
               ITEMP(2,K)=L                                              PAL10260
               ITEMP(3,K)=L                                              PAL10270
               ITEMP(4,K)=L                                              PAL10280
               ITEMP(5,K)=L                                              PAL10290
               ISUM3=IPROD+INC                                           PAL10300
               IF(LFUSES(IINPUT,ISUM3 +  0 )) ITEMP(5,K)=H               PAL10310
               IF(LFUSES(IINPUT,ISUM3 +  8 )) ITEMP(4,K)=H               PAL10320
               IF(LFUSES(IINPUT,ISUM3 + 16 )) ITEMP(3,K)=H               PAL10330
               IF(LFUSES(IINPUT,ISUM3 + 24 )) ITEMP(2,K)=H               PAL10340
               IF(LFUSES(IINPUT,ISUM3 + 32 )) ITEMP(1,K)=H               PAL10350
   15          CONTINUE                                                  PAL10360
   20        WRITE(PDF,30) ITEMP                                         PAL10370
   30        FORMAT(' ',10('B',5A1,'F '))                                PAL10380
      WRITE(PDF,10)                                                      PAL10390
      RETURN                                                             PAL10400
      END                                                                PAL10410
C                                                                        PAL10420
C*************************************************************************PAL10430
C                                                                        PAL10440
      SUBROUTINE SLIP(LFUSES,I88PRO,ITYPE,IBLOW)                         PAL10450
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0


C      THIS SUBROUTINE WILL BLOW THE ENTIRE CONDITIONAL THREE-STATE       PAL10460
C       PRODUCT LINE WHEN 'IF(VCC)' CONDITION IS USED FOR THE             PAL10470
C       CORRESPONDING OUTPUT PIN                                          PAL10480
       IMPLICIT INTEGER (A-Z)                                             PAL10490
       INTEGER IENABL(10,14)                                              PAL10500
       LOGICAL LFUSES(40,80)                                              PAL10510
C      1=ENABLED OUTPUT.    0=ANYTHING ELSE FOR THAT OUTPUT               PAL10520
       DATA IENABL/                                                       PAL10530
      1      0,0,0,0,0,0,0,0,0,0,                                         PAL10540
      2      0,0,0,0,0,0,0,0,0,0,                                         PAL10550
      3      0,0,0,0,0,0,0,0,0,0,                                         PAL10560
      4      0,0,0,0,0,0,0,0,0,0,                                         PAL10570
      5      0,0,0,0,0,0,0,0,0,0,                                         PAL10580
      6      0,0,0,0,0,0,0,0,0,0,                                         PAL10590
      7      1,1,1,1,1,1,1,1,1,1,                                         PAL10600
      8      0,0,0,0,0,0,0,0,0,0,                                         PAL10610
      9      1,0,0,0,0,0,0,0,0,1,                                         PAL10620
      A      1,1,1,0,0,0,0,1,1,1,                                         PAL10630
      B      0,1,1,1,1,1,1,1,1,0,                                         PAL10640
      C      0,0,0,0,0,0,0,0,0,0,                                         PAL10650
      D      0,1,0,0,0,0,0,0,1,0,                                         PAL10660
      E      0,1,1,0,0,0,0,1,1,0/                                         PAL10670
       IOUT=(I88PRO-1)/8+1                                              PAL10680
       IF(IENABL(IOUT,ITYPE).EQ.0) RETURN                               PAL10690
       DO 10 I=1,40                                                     PAL10700
       IBLOW = IBLOW + 1                                                PAL10710
   10  LFUSES(I,I88PRO) = .TRUE.                                        PAL10720
       I88PRO = I88PRO + 1                                              PAL10730
       RETURN                                                           PAL10740
       END                                                              PAL10750
C                                                                       PAL10760
C***********************************************************************PAL10770
C                                                                       PAL10780
       SUBROUTINE FANTOM(ITYPE,IOP,IOUT,IPROD,I8PRO)                    PAL10790
C      THIS SUBROUTINE UPDATES IOUT (THE PRINTED FUSE PLOT)             PAL10800
C       FOR HIGH AND LOW PHANTOM FUSES                                  PAL10810
       IMPLICIT INTEGER (A-Z)                                           PAL10820
       INTEGER IOUT(64)                                                 PAL10830
       LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR          PAL10840
       COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR          PAL10850
       COMMON /BLK/ PR8X10(10,14),PROD8(8,11),PRODLN(40,7)              PAL10860
       DATA B/'B'/,N/'N'/,P/'P'/,LOFANT/'0'/,HIFANT/'0'/,IBLANK/' '/    PAL10870
C      GET OUTPUT GROUPING                                              PAL10880
       OUTPUT=(IPROD-1)/8+1                                             PAL10890
       GRTYPE=PR8X10(OUTPUT,ITYPE)                                      PAL10900
       LNTYPE=PROD8(I8PRO,GRTYPE)                                       PAL10910
       DO 10 COL=1,40                                                   PAL10920
          IF( PRODLN(COL,LNTYPE).EQ.P.AND.IOP.EQ.P )  IOUT(COL)=HIFANT  PAL10930
          IF( PRODLN(COL,LNTYPE).EQ.P.AND.IOP.EQ.B )  IOUT(COL)=IBLANK  PAL10940
          IF( PRODLN(COL,LNTYPE).EQ.N )               IOUT(COL)=LOFANT  PAL10950
   10  CONTINUE                                                         PAL10960
       RETURN                                                           PAL10970
       END                                                              PAL10980
C                                                                       PAL10990
C***********************************************************************PAL11000
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

C                                                                       PAL11010
      SUBROUTINE IODC2                                                  PAL11020
C***** THIS ROUTINE IS OPTIONAL, IT MAY BE USED TO TURN PERIPHERALS ON   PAL11030
      IMPLICIT INTEGER (A-Z)                                            PAL11040
      INTEGER   BEL,DC2                                                 PAL11050
      COMMON /LUNIT/ PMS,POF,PDF                                        PAL11060
      DATA BEL/Z07000000/,DC2/Z22000000/                                PAL11070
      WRITE(PDF,10) DC2,BEL                                             PAL11080
   10 FORMAT(' ',2A1)                                                   PAL11090
      RETURN                                                            PAL11100
      END                                                               PAL11110
C                                                                       PAL11120
C***********************************************************************PAL11130
C                                                                       PAL11140
      SUBROUTINE IODC4                                                  PAL11150
C***** THIS ROUTINE IS OPTIONAL, IT MAY BE USED TO TURN PERIPHERALS OFF  PAL11160
      IMPLICIT INTEGER (A-Z)                                            PAL11170
      INTEGER   BEL,DC3,DC4                                             PAL11180
      DATA BEL/Z07000000/,DC3/Z23000000/,DC4/Z24000000/                 PAL11190
      WRITE(PDF,10) BEL,DC3,DC4                                         PAL11200
   10 FORMAT(' ',3A1)                                                   PAL11210
      RETURN                                                            PAL11220
      END                                                               PAL11230
C                                                                       PAL11240
C***********************************************************************PAL11250
C                                                                       PAL11260
      SUBROUTINE TEST(LPHASE,LBUF,TITLE,IC,IL,ILE,ISYM,IBUF,ITYPE,      PAL11270
     1                IPCTR,LERR,ISAF,IPCTR1,LSA11,LSA01)               PAL11280
C     THIS SUBROUTINE PERFORMS THE FUNCTION TABLE SIMULATION            PAL11290
C      AND GENERATES TEST VECTORS                                       PAL11300
      IMPLICIT INTEGER (A-Z)                                            PAL11310
      INTEGER ISYM(8,24),ISYM1(8,24),IBUF(8,24),IVECT(24),IVECTP(24),   PAL11320
     1        ISTATE(24),ISTATT(24),IPIN(24),TITLE(80),IPCTR             PAL11330
      LOGICAL LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR,LSAME,    PAL11340
     1        XORFND,LERR,LPHASE(24),LPHAS1(24),LBUF(24),LOUT(24),      PAL11350
     2        LOUTP(24),LCLOCK,LPTRST,LCTRST,LENABL(24),NREG,           PAL11360
     3        LSA11,LSA12,LSA01,LSA02                                   PAL11370
      INTEGER   BEL                                                     PAL11380
      COMMON  LBLANK,LLEFT,LAND,LOR,LSLASH,LEQUAL,LRIGHT,LXOR           PAL11390
      COMMON /PGE/ IPAGE(80,200)                                        PAL11400
      COMMON /LUNIT/ PMS,POF,PDF                                        PAL11410
      COMMON /FTEST/ IFUNCT,IDESC,IEND                                  PAL11420
      DATA IDASH/'-'/,L/'L'/,H/'H'/,X/'X'/,C/'C'/,Z/'Z'/,NO/'0'/,       PAL11430
     1     N1/'1'/,ERR/'?'/,IBLANK/' '/,COMENT/';'/                     PAL11440
      DATA BEL/Z07000000/                                               PAL11450
C     PRINT AN ERROR MESSAGE IF NO FUNCTION TABLE IS SUPPLIED           PAL11460
      IF(IFUNCT.NE.0) GO TO 3                                           PAL11470
      WRITE(PMS,2)                                                      PAL11480
    2 FORMAT(/,' FUNCTION TABLE MUST BE SUPPLIED IN ORDER TO PERFORM',  PAL11490
     1        ' SIMULATION')                                           PAL11500
      RETURN                                                            PAL11510
C     PRINT TITLE                                                       PAL11520
    3 IF((.NOT.LSA11).AND.(.NOT.LSA01)) WRITE(POF,4) TITLE              PAL11530
    4 FORMAT(/,' ',80A1,/)                                              PAL11540
C     INITIALIZE LERR (FUNCTION TABLE ERROR FLAG) TO NO ERROR           PAL11550
```

```
FILE: PAL24     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      LERR=.FALSE.                                                      PAL11560
C     INITIALIZE NERR (NUMBER OF FUNCTION TABLE ERRORS) TO NO ERROR     PAL11570
      NERR=0                                                            PAL11580
C     SET THE STARTING POINT OF THE FUNCTION TABLE TO COLUMN 0          PAL11590
C      AND IFUNCT + 1                                                   PAL11600
      IC=0                                                              PAL11610
      IL=IFUNCT + 1                                                     PAL11620
C     INITIALISE SA1/SA0 PARAMETERS                                     PAL11630
      IPCTR3=0                                                          PAL11640
      IEQN=0                                                            PAL11650
      IPCTR=0                                                           PAL11660
C     INITIALIZE ITRST (THREE-STATE ENABLE FUNCTION TABLE PIN NUMBER)   PAL11670
      ITRST=0                                                           PAL11680
C     MAKE A DUMMY CALL TO INCR                                         PAL11690
      CALL INCR(IC,IL)                                                  PAL11700
C     GET THE FUNCTION TABLE PIN LIST (UP TO 22)                        PAL11710
C      GO ONE MORE THAN MAX TO LOOK FOR DASHED LINE                     PAL11720
      DO 10 I=1,23                                                      PAL11730
      CALL GETSYM(LPHAS1,ISYM1,I,IC,IL)                                 PAL11740
         DO 5 J=1,8                                                     PAL11750
    5    IBUF(J,1)=ISYM1(J,I)                                           PAL11760
      IF(IBUF(8,1).EQ.IDASH) GO TO 12                                   PAL11770
      CALL MATCH(IMATCH,IBUF,ISYM)                                      PAL11780
      IF(IMATCH.NE.0) GO TO 7                                           PAL11790
      WRITE(PMS,6) (IBUF(J,1),J=1,8)                                    PAL11800
    6 FORMAT(/,' FUNCTION TABLE PIN LIST ERROR AT', 8A1)                PAL11810
      RETURN                                                            PAL11820
    7 LOUT(I)=.FALSE.                                                   PAL11830
      ISTATT(I)=X                                                       PAL11840
      IVECTP(I)=X                                                       PAL11850
C     IF APPROPIATE PAL TYPE, REMEMBER LOCATION OF CLOCK AND THREE-STATEPAL11860
C      ENABLE PIN IN FUNCTION TABLE PIN LIST                            PAL11870
      IF( .NOT.(ITYPE.EQ.8.OR.ITYPE.EQ.9.OR.ITYPE.EQ.10.OR.             PAL11880
     1          ITYPE.EQ.12.OR.ITYPE.EQ.13.OR.ITYPE.EQ.14) ) GO TO 10   PAL11890
      IF(IMATCH.EQ.1)  ICLOCK=I                                         PAL11900
      IF(IMATCH.EQ.13) ITRST=I                                          PAL11910
   10 IPIN(I)=IMATCH                                                    PAL11920
C     ALL SIGNAL NAMES FOR THE FUNCTIONAL TEST HAVE BEEN READ IN        PAL11930
C      ADJUST COUNT                                                     PAL11940
   12 IMAX=I-1                                                          PAL11950
      NVECT=0                                                           PAL11960
C                                                                       PAL11970
C*****START OF MAIN LOOP FOR SIMULATION*****                           PAL11980
C                                                                       PAL11990
C                                                                       PAL12000
   90 IPCTR2=0                                                          PAL12010
      IEQN=0                                                            PAL12020
      IPCTR3=0                                                          PAL12030
      LSA12=.FALSE.                                                     PAL12040
      LSA02=.FALSE.                                                     PAL12050
C                                                                       PAL12060
      NVECT=NVECT+1                                                     PAL12070
      IC1=0                                                             PAL12080
      IL1=ILE                                                           PAL12090
C     GO PASSED COMMENT LINES                                           PAL12100
```

```
FILE: PAL24    FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

   23 IF(IPAGE(1,IL).NE.COMENT) GO TO 24                                PAL12110
      IL=IL+1                                                           PAL12120
      GO TO 23                                                          PAL12130
   24 CONTINUE                                                          PAL12140
C     GETS VECTORS FROM FUNCTION TABLE                                  PAL12150
      DO 20 I=1,IMAX                                                    PAL12160
        IF(IPAGE(IC,IL).EQ.IBLANK) GO TO 21                             PAL12170
        GO TO 22                                                        PAL12180
   21   IC=IC+1                                                         PAL12190
        IF(IPAGE(IC,IL).EQ.IBLANK) GO TO 21                             PAL12200
   22   IVECT(I)=IPAGE(IC,IL)                                           PAL12210
        IC=IC+1                                                         PAL12220
   20 CONTINUE                                                          PAL12230
C     ADVANCE LINE COUNT TO SKIP FUNCTION TABLE COMMENTS                PAL12240
      IL=IL+1                                                           PAL12250
      IC=1                                                              PAL12260
      IF(IVECT(1).EQ.IDASH) GO TO 95                                    PAL12270
C     CHECK FOR VALID FUNCTION TABLE VALUES (L,H,X,Z,C)                 PAL12280
      DO 11 I=1,IMAX                                                    PAL12290
         IF( IVECT(I).EQ.L.OR.IVECT(I).EQ.H.OR.IVECT(I).EQ.X.OR.        PAL12300
     1       IVECT(I).EQ.Z.OR.IVECT(I).EQ.C) GO TO 11                   PAL12310
         WRITE(PMS,8) IVECT(I),NVECT                                    PAL12320
    8    FORMAT(/,' ',A1,' IS NOT AN ALLOWED FUNCTION TABLE ENTRY',     PAL12330
     1                 ' IN VECTOR ',I3)                               PAL12340
         RETURN                                                         PAL12350
   11 CONTINUE                                                          PAL12360
C     INITIALIZE CLOCK AND THREE-STATE ENABLE FLAGS                     PAL12370
      LCLOCK=.FALSE.                                                    PAL12380
      LCTRST=.TRUE.                                                     PAL12390
      LPTRST=.TRUE.                                                     PAL12400
      DO 13 I=1,IMAX                                                    PAL12410
   13    LENABL(I)=.TRUE.                                             PAL12420
C     INITIALIZE NREG (NOT REGISTERED OUTPUT) TO FALSE                  PAL12430
      NREG=.FALSE.                                                      PAL12440
C     INITIALIZE ISTATE ARRAY TO ALL X'S                                PAL12450
      DO 15 I=1,24                                                      PAL12460
   15 ISTATE(I)=X                                                       PAL12470
C     CHECK IF THIS PAL TYPE HAS REGISTERS                              PAL12480
      IF( .NOT.(ITYPE.EQ.8.OR.ITYPE.EQ.9.OR.ITYPE.EQ.10.OR.             PAL12490
     1          ITYPE.EQ.12.OR.ITYPE.EQ.13.OR.ITYPE.EQ.14) ) GO TO 25   PAL12500
C     CHECK CLOCK AND THREE-STATE ENABLE PINS AND CHANGE FLAG IF NEEDED PAL12510
      IF(IVECT(ICLOCK).EQ.C) LCLOCK=.TRUE.                              PAL12520
      IF(ITRST.EQ.0) GO TO 25                                           PAL12530
      LSAME=( (     LPHASE(13)).AND.(     LPHASE(ITRST)).OR.          PAL12540
     1        (.NOT.LPHASE(13)).AND.(.NOT.LPHASE(ITRST)) )              PAL12550
      IF( IVECT(ITRST).EQ.L.AND.(.NOT.LSAME).OR.                        PAL12560
     1    IVECT(ITRST).EQ.H.AND.(     LSAME) ) LPTRST=.FALSE.           PAL12570
      IF(LPTRST) GO TO 25                                               PAL12580
C     DISABLE REGISTERED OUTPUTS IF APPROPRIATE                         PAL12590
      DO 46 I=1,IMAX                                                    PAL12600
         J=IPIN(I)                                                      PAL12610
         IF(J.EQ.17.OR.J.EQ.18.OR.J.EQ.19.OR.J.EQ.20) LENABL(I)=.FALSE. PAL12620
         IF( (ITYPE.EQ.8.OR.ITYPE.EQ.9.OR.ITYPE.EQ.12.OR.               PAL12630
     1        ITYPE.EQ.13).AND.(J.EQ.16.OR.J.EQ.21) ) LENABL(I)=.FALSE. PAL12640
         IF( (ITYPE.EQ.8.OR.ITYPE.EQ.9.OR.ITYPE.EQ.12).AND.             PAL12650
```

```
FILE: PAL24     FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

     1       (J.EQ.15.OR.J.EQ.22) )                          LENABL(I)=.FALSE.  PAL12660
          IF(  ITYPE.EQ.8.AND.(J.EQ.14.OR.J.EQ.23) )         LENABL(I)=.FALSE.  PAL12670
   46 CONTINUE                                                                   PAL12680
C                                                                                PAL12690
C*****SCAN THROUGH THE LOGIC EQUATIONS*****                                      PAL12700
C                                                                                PAL12710
C      MAKE A DUMMY CALL TO INCR                                                 PAL12720
   25 CALL INCR(IC1,IL1)                                                         PAL12730
   26 CALL GETSYM(LBUF,IBUF,1,IC1,IL1)                                           PAL12740
      IF(LLEFT) GO TO 29                                                         PAL12750
   27 IF(.NOT.LEQUAL) GO TO 26                                                   PAL12760
C                                                                                PAL12770
      IF(LEQUAL) IEQN=IEQN+1                                                     PAL12780
C                                                                                PAL12790
C      EVALUATE CONDITIONAL THREE-STATE PRODUCT LINE                             PAL12800
   29 IF(LEQUAL) GO TO 35                                                        PAL12810
      NREG=.TRUE.                                                                PAL12820
   33 CALL GETSYM(LBUF,IBUF,1,IC1,IL1)                                           PAL12830
      CALL MATCH(IINP,IBUF,ISYM1)                                                PAL12840
C      CHECK FOR GND, VCC, /GND, OR /VCC IN CONDITIONAL THREE-STATE              PAL12850
C      PRODUCT LINE                                                              PAL12860
      IF(IINP.NE.0) GO TO 32                                                     PAL12870
      CALL MATCH(IMATCH,IBUF,ISYM)                                               PAL12880
      ILL=IL1                                                                    PAL12890
      IF( IMATCH.EQ.12.AND.(LBUF(1)).OR.                                         PAL12900
     1    IMATCH.EQ.24.AND.(.NOT.LBUF(1)) ) LCTRST=.FALSE.                       PAL12910
      IF( IINP.EQ.0.AND.IMATCH.NE.12.AND.IMATCH.NE.24 ) GO TO 100                PAL12920
      GO TO 34                                                                   PAL12930
   32 ITEST=IVECT(IINP)                                                          PAL12940
      IF(  ITEST.EQ.L.AND.(     LPHAS1(IINP)).AND.(     LBUF(1))                 PAL12950
     1.OR. ITEST.EQ.H.AND.(     LPHAS1(IINP)).AND.(.NOT.LBUF(1))                 PAL12960
     2.OR. ITEST.EQ.H.AND.(.NOT.LPHAS1(IINP)).AND.(     LBUF(1))                 PAL12970
     3.OR. ITEST.EQ.L.AND.(.NOT.LPHAS1(IINP)).AND.(.NOT.LBUF(1))                 PAL12980
     4  )  LCTRST=.FALSE.                                                       PAL12990
      IF(ITEST.EQ.X.OR.ITEST.EQ.Z) LCTRST=.FALSE.                                PAL13000
   34 IF(LAND) GO TO 33                                                          PAL13010
      GO TO 27                                                                   PAL13020
C                                                                                PAL13030
C      EVALUATE THE LOGIC EQUATION                                               PAL13040
C                                                                                PAL13050
C      FIND PIN NUMBER OF THE OUTPUT VECTORS                                     PAL13060
C                                                                                PAL13070
   35 IPCTR3=0                                                                   PAL13080
C                                                                                PAL13090
      CALL MATCH(IOUTP,IBUF,ISYM1)                                               PAL13100
C      FLAG FOR UNREGISTERED OUTPUTS                                             PAL13110
      CALL MATCH(IOUT,IBUF,ISYM)                                                 PAL13120
      IF(ITYPE.LE.7.OR.ITYPE.EQ.11) NREG=.TRUE.                                  PAL13130
      IF( (ITYPE.EQ.9.OR.ITYPE.EQ.10).AND.(IOUT.EQ.14.OR.IOUT.EQ.23) )           PAL13140
     1    NREG=.TRUE.                                                           PAL13150
      IF( (ITYPE.EQ.10.OR.ITYPE.EQ.13.OR.ITYPE.EQ.14).AND.                       PAL13160
     1    (IOUT.EQ.15.OR.IOUT.EQ.22) ) NREG=.TRUE.                              PAL13170
      IF( (ITYPE.EQ.10.OR.ITYPE.EQ.14).AND.(IOUT.EQ.16.OR.IOUT.EQ.21) )          PAL13180
     1    NREG=.TRUE.                                                           PAL13190
      ILL=IL1                                                                    PAL13200
```

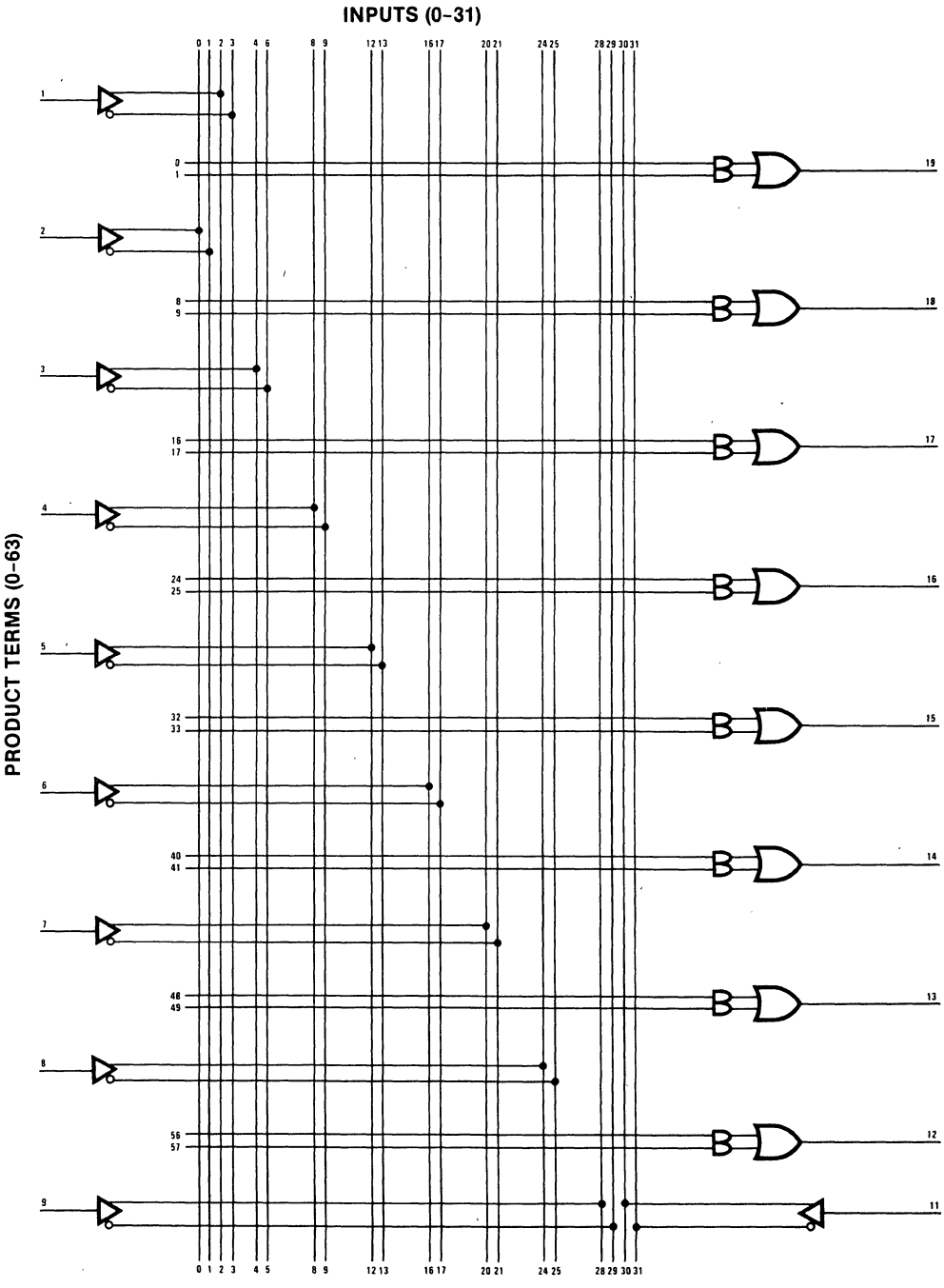
```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      IF(IOUTP.EQ.0) GO TO 100                                          PAL13210
      IF(NREG) LENABL(IOUTP)=LCTRST                                     PAL13220
      LOUT(IOUTP)=.TRUE.                                                PAL13230
      IF( .NOT.LCTRST ) LOUT(IOUTP)=.FALSE.                             PAL13240
      LCTRST=.TRUE.                                                     PAL13250
      LOUTP(IOUTP)=LBUF(1)                                              PAL13260
C     DETERMINE PRODUCT TERM AND EVENTUALLY SUM FOR OUTPUT KEEPING      PAL13270
C      TRACK TO SEE IF AN XOR (EXCLUSIVE OR) HAS BEEN FOUND             PAL13280
      XORSUM=H                                                          PAL13290
      XORFND=.FALSE.                                                    PAL13300
      ISUM=L                                                            PAL13310
C                                                                       PAL13320
   28 IPCTR2=IPCTR2+1                                                   PAL13330
      IPCTR3=IPCTR3+1                                                   PAL13340
      IPCTR=IPCTR+1                                                     PAL13350
C                                                                       PAL13360
      IPROD=H                                                           PAL13370
   30 ILL=ILI                                                           PAL13380
      CALL GETSYM(LBUF,IBUF,1,IC1,ILI)                                  PAL13390
      CALL MATCH(IINP,IBUF,ISYM1)                                       PAL13400
      IF(IINP.NE.0) GO TO 47                                            PAL13410
      CALL MATCH(IMATCH,IBUF,ISYM)                                      PAL13420
      IF(IMATCH.NE.12.AND.IMATCH.NE.24) GO TO 100                       PAL13430
C     TWEEK FOR GND AND VCC IN PRODUCT LINE                             PAL13440
      IF(IMATCH.EQ.12) ITEST=L                                          PAL13450
      IF(IMATCH.EQ.24) ITEST=H                                          PAL13460
      IINP=23                                                           PAL13470
      LPHAS1(23)=.TRUE.                                                 PAL13480
      GO TO 37                                                          PAL13490
   47 ITEST=IVECT(IINP)                                                 PAL13500
C     GET REGISTERED FEED BACK VALUES                                   PAL13510
      IF(NREG) GO TO 37                                                 PAL13520
      CALL MATCH(IIFB,IBUF,ISYM)                                        PAL13530
      IF( (ITYPE.EQ.8.OR.ITYPE.EQ.9.OR.ITYPE.EQ.10.OR.ITYPE.EQ.12.OR.   PAL13540
     1     ITYPE.EQ.13.OR.ITYPE.EQ.14).AND.(IIFB.EQ.17.OR.IIFB.EQ.18.OR.PAL13550
     2     IIFB.EQ.19.OR.IIFB.EQ.20) ) ITEST=IVECTP(IINP)               PAL13560
      IF( (ITYPE.EQ.8.OR.ITYPE.EQ.9.OR.ITYPE.EQ.12.OR.ITYPE.EQ.13).AND. PAL13570
     1    (IIFB.EQ.16.OR.IIFB.EQ.21) ) ITEST=IVECTP(IINP)               PAL13580
      IF( (ITYPE.EQ.8.OR.ITYPE.EQ.9.OR.ITYPE.EQ.12).AND.                PAL13590
     1    (IIFB.EQ.15.OR.IIFB.EQ.22) ) ITEST=IVECTP(IINP)               PAL13600
      IF( ITYPE.EQ.8.AND.(IIFB.EQ.14.OR.IIFB.EQ.23) )                   PAL13610
     1                              ITEST=IVECTP(IINP)                  PAL13620
   37 IF(ITEST.EQ.X.OR.ITEST.EQ.Z) ITEST=L                              PAL13630
      IF(  ITEST.EQ.L.AND.(     LPHAS1(IINP)).AND.(     LBUF(1))       PAL13640
     1.OR. ITEST.EQ.H.AND.(     LPHAS1(IINP)).AND.(.NOT.LBUF(1))       PAL13650
     2.OR. ITEST.EQ.H.AND.(.NOT.LPHAS1(IINP)).AND.(     LBUF(1))       PAL13660
     3.OR. ITEST.EQ.L.AND.(.NOT.LPHAS1(IINP)).AND.(.NOT.LBUF(1))       PAL13670
     4  )  IPROD=L                                                     PAL13680
C                                                                       PAL13690
      IF((IPCTR2.EQ.IPCTR1).AND.(LSA11)) GO TO 110                      PAL13700
C                                                                       PAL13710
   38 IF(LAND) GO TO 30                                                 PAL13720
C                                                                       PAL13730
      IF ((IPCTR2.EQ.IPCTR1).AND.(LSA01)) GO TO 120                     PAL13740
C                                                                       PAL13750
```

```
FILE: PAL24     FORTRAN  A    NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

  121 IF(ISUM.EQ.L.AND.IPROD.EQ.X) ISUM=X                                PAL13760
      IF( (ISUM.NE.H).AND.IPROD.EQ.H ) ISUM=H                            PAL13770
C     CHECK FOR XOR (EXCLUSIVE OR) AND SAVE INTERMEDIATE VALUE           PAL13780
      IF(.NOT.LXOR) GO TO 31                                             PAL13790
      XORSUM=ISUM                                                        PAL13800
      XORFND=.TRUE.                                                      PAL13810
      ISUM=L                                                             PAL13820
      GO TO 28                                                           PAL13830
   31 IF(LOR) GO TO 28                                                   PAL13840
      IPCTR3=0                                                           PAL13850
C     IF END OF EQUATION HAS BEEN FOUND, DETERMINE FINAL SUM AND SAVE IT PAL13860
      IF(.NOT.XORFND)     ISTAT1(IOUTP)=ISUM                             PAL13870
      IF( (XORFND).AND.((ISUM.EQ.L.AND.XORSUM.EQ.L).OR.                  PAL13880
     1                  (ISUM.EQ.H.AND.XORSUM.EQ.H)) ) ISTATT(IOUTP)=L  PAL13890
      IF( (XORFND).AND.((ISUM.EQ.H.AND.XORSUM.EQ.L).OR.                  PAL13900
     1                  (ISUM.EQ.L.AND.XORSUM.EQ.H)) ) ISTATT(IOUTP)=H  PAL13910
      IF( (XORFND).AND. (ISUM.EQ.X.OR. XORSUM.EQ.X) )  ISTATT(IOUTP)=X   PAL13920
C     REGISTER DOES NOT CHANGE STATE IF NO CLOCK PULSE IS RECEIVED       PAL13930
      IF( (LCLOCK).OR.(NREG) ) GO TO 36                                  PAL13940
      LSAME = ( (      LOUTP(IOUTP)).AND.(      LPHAS1(IOUTP)).OR.        PAL13950
     1          (.NOT.LOUTP(IOUTP)).AND.(.NOT.LPHAS1(IOUTP)) )          PAL13960
      IF( IVECTP(IOUTP).EQ.L.AND.(      LSAME) ) ISTATT(IOUTP)=L         PAL13970
      IF( IVECTP(IOUTP).EQ.H.AND.(      LSAME) ) ISTATT(IOUTP)=H         PAL13980
      IF( IVECTP(IOUTP).EQ.L.AND.(.NOT.LSAME) ) ISTATT(IOUTP)=H          PAL13990
      IF( IVECTP(IOUTP).EQ.H.AND.(.NOT.LSAME) ) ISTATT(IOUTP)=L          PAL14000
   36 NREG=.FALSE.                                                       PAL14010
C     CHECK IF ALL EQUATIONS HAVE BEEN PROCESSED BY COMPARING CURRENT    PAL14020
C      LINE NUMBER WITH FUNCTION TABLE LINE NUMBER                       PAL14030
      IF(IDESC.NE.0.AND.IL1.LT.IFUNCT.AND.IL1.LT.IDESC.OR.               PAL14040
     1   IDESC.EQ.0.AND.IL1.LT.IFUNCT) GO TO 27                          PAL14050
C     DETERMINE OUTPUT LOGIC VALUES                                      PAL14060
C      COMPARE OUTPUTS TO SEE IF VECTOR AGREES WITH RESULTS              PAL14070
      DO 50 I=1,IMAX                                                     PAL14080
      IF(.NOT.LOUT(I)) GO TO 50                                          PAL14090
      IF(ISTATT(I).EQ.X.AND.IVECT(I).EQ.X) GO TO 50                      PAL14100
      LSAME = ( (      LOUTP(I)).AND.(      LPHAS1(I)).OR.             PAL14110
     1          (.NOT.LOUTP(I)).AND.(.NOT.LPHAS1(I)) )                  PAL14120
      IMESS=40                                                           PAL14130
      IF(ISTATT(I).EQ.L.AND.IVECT(I).EQ.L.AND.(.NOT.LSAME))  IMESS=41    PAL14140
      IF(ISTATT(I).EQ.H.AND.IVECT(I).EQ.H.AND.(.NOT.LSAME))  IMESS=42    PAL14150
      IF(ISTATT(I).EQ.L.AND.IVECT(I).EQ.H.AND.(      LSAME))  IMESS=42    PAL14160
      IF(ISTATT(I).EQ.H.AND.IVECT(I).EQ.L.AND.(      LSAME))  IMESS=41    PAL14170
      IF( (      LENABL(I)).AND.IVECT(I).EQ.Z )               IMESS=43    PAL14180
      IF( (.NOT.LENABL(I)).AND.(LOUT(I)).AND.IVECT(I).NE.Z )  IMESS=44    PAL14190
      IF(IMESS.NE.40) LERR=.TRUE.                                        PAL14200
C                                                                        PAL14210
      IF((.NOT.LERR).AND.((LSA11).OR.(LSA01))) GO TO 50                  PAL14220
      IF((LERR).AND.((LSA11).OR.(LSA01))) GO TO 115                      PAL14230
C                                                                        PAL14240
      IF(IMESS.EQ.41) WRITE(PMS,41) NVECT,(ISYM1(J,I),J=1,8)             PAL14250
   41 FORMAT(/,' FUNCTION TABLE ERROR IN VECTOR',I3,'  PIN =',8A1,       PAL14260
     1          '  EXPECT = H  ACTUAL = L')                             PAL14270
      IF(IMESS.EQ.42) WRITE(PMS,42) NVECT,(ISYM1(J,I),J=1,8)             PAL14280
   42 FORMAT(/,' FUNCTION TABLE ERROR IN VECTOR',I3,'  PIN =',8A1,       PAL14290
     1          '  EXPECT = L  ACTUAL = H')                             PAL14300
```

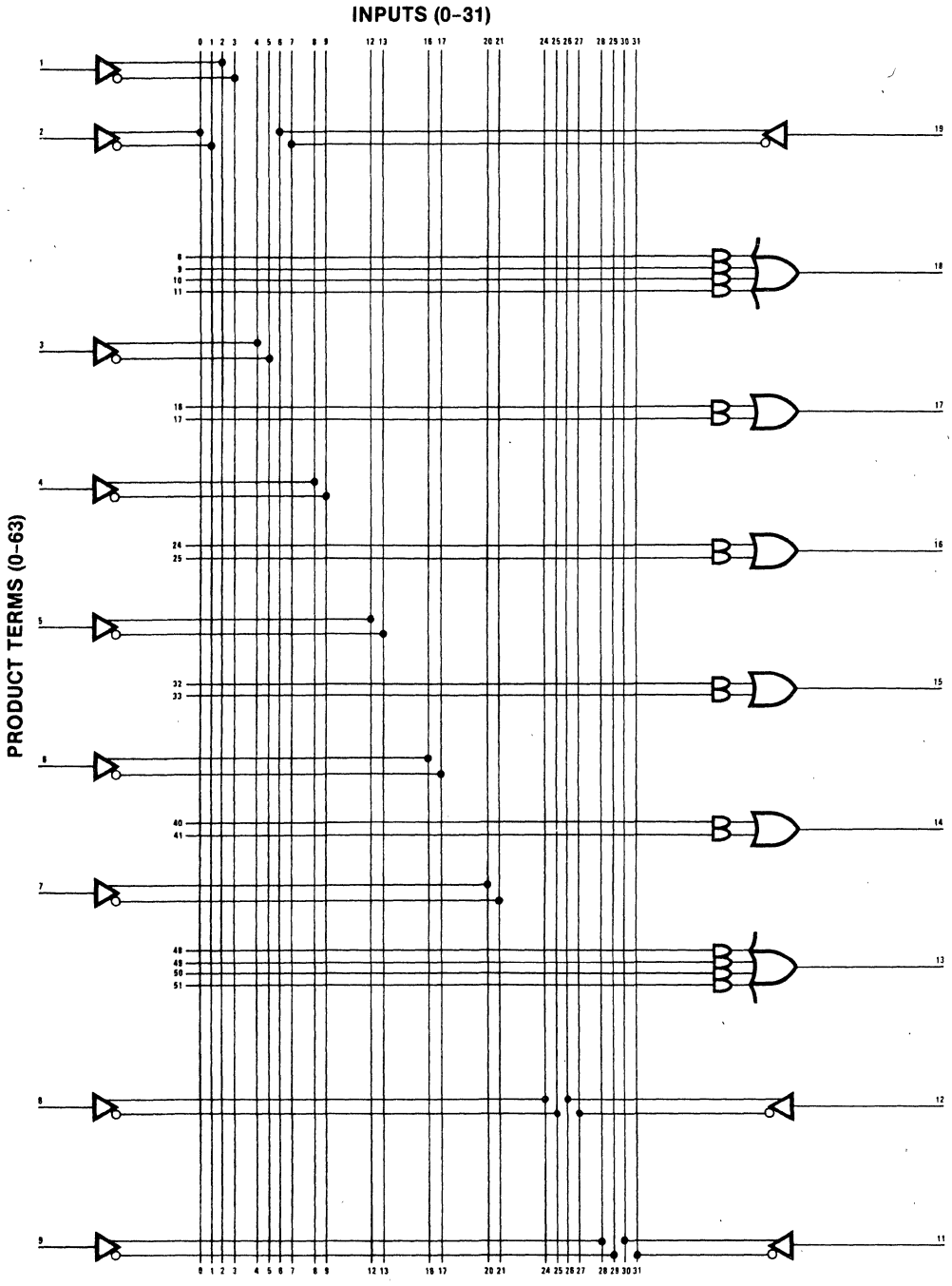
```
FILE: PAL24    FORTRAN  A   NSC TIME SHARING SERVICES VM/SP RELEASE 2.0

      IF(IMESS.EQ.43) WRITE(PMS,43) NVECT,(ISYM1(J,I),J=1,8)                PAL14310
   43 FORMAT(/,' FUNCTION TABLE ERROR IN VECTOR',I3,'  PIN =',8A1,          PAL14320
     1       /,'  EXPECT  = OUTPUT ENABLE  ACTUAL = Z')                     PAL14330
      IF(IMESS.EQ.44) WRITE(PMS,44) NVECT,(ISYM1(J,I),J=1,8),IVECT(I)       PAL14340
   44 FORMAT(/,' FUNCTION TABLE ERROR IN VECTOR',I3,'  PIN =',8A1,          PAL14350
     1         '  EXPECT = Z  ACTUAL = ',A1)                               PAL14360
      IF( (IMESS.NE.40).AND.(PMS.EQ.6) ) WRITE(PMS,45) BEL                  PAL14370
   45 FORMAT(' ',A1)                                                        PAL14380
      IF(IMESS.NE.40) IVECT(I)=ERR                                          PAL14390
      IF(IMESS.NE.40) NERR=NERR+1                                           PAL14400
   50 CONTINUE                                                              PAL14410
C     CHANGE THE ORDER OF VECTORS FROM THE ORDER OF APPEARANCE IN THE       PAL14420
C      FUNCTION TABLE TO THAT OF THE PIN LIST AND TWEEK FOR OUTPUT          PAL14430
      DO 65 I=1,24                                                          PAL14440
         DO 55 J=1,IMAX                                                     PAL14450
         IF(IPIN(J).NE.I) GO TO 55                                          PAL14460
         IF( IVECT(J).EQ.L.OR.IVECT(J).EQ.H ) GO TO 51                      PAL14470
         ISTATE(I)=IVECT(J)                                                 PAL14480
         GO TO 65                                                           PAL14490
   51    LSAME=( (      LPHASE(I)).AND.(      LPHAS1(J)).OR.               PAL14500
     1           (.NOT.LPHASE(1)).AND.(.NOT.LPHAS1(J)) )                    PAL14510
         IF( (ITYPE.EQ.5.AND.(I.EQ.18.OR.I.EQ.19) )  LOUT(J)=.TRUE.         PAL14520
         IF( (.NOT.LOUT(J)).AND.(      LSAME).AND.                          PAL14530
     1         IVECT(J).EQ.L )                          ISTATE(I)=NO        PAL14540
         IF( (.NOT.LOUT(J)).AND.(      LSAME).AND.                          PAL14550
     1         IVECT(J).EQ.H )                          ISTATE(I)=N1        PAL14560
         IF( (.NOT.LOUT(J)).AND.(.NOT.LSAME).AND.                           PAL14570
     1         IVECT(J).EQ.L )                          ISTATE(I)=N1        PAL14580
         IF( (.NOT.LOUT(J)).AND.(.NOT.LSAME).AND.                           PAL14590
     1         IVECT(J).EQ.H )                          ISTATE(I)=NO        PAL14600
         IF( (      LOUT(J)).AND.(      LSAME).AND.                       PAL14610
     1         IVECT(J).EQ.L.AND.(      LENABL(J)) )  ISTATE(I)=L          PAL14620
         IF( (      LOUT(J)).AND.(      LSAME).AND.                       PAL14630
     1         IVECT(J).EQ.H.AND.(      LENABL(J)) )  ISTATE(I)=H          PAL14640
         IF( (      LOUT(J)).AND.(.NOT.LSAME).AND.                        PAL14650
     1         IVECT(J).EQ.L.AND.(      LENABL(J)) )  ISTATE(I)=H          PAL14660
         IF( (      LOUT(J)).AND.(.NOT.LSAME).AND.                        PAL14670
     1         IVECT(J).EQ.H.AND.(      LENABL(J)) )  ISTATE(I)=L          PAL14680
         IF( IVECT(J).EQ.ERR )                        ISTATE(I)=ERR       PAL14690
         GO TO 65                                                           PAL14700
   55 CONTINUE                                                              PAL14710
C     SAVE PRESENT VECTORS FOR FEED BACK USED WITH NEXT SET OF VECTORS      PAL14720
C      IF CLOCK PULSE AND NOT Z (HI-Z IS ASYNCHRONOUS)                      PAL14730
   65 IF( (LCLOCK).AND.IVECT(J).NE.Z ) IVECTP(J)=IVECT(J)                   PAL14740
C     ASSIGN X TO GROUND PIN AND 1 TO VCC PIN                               PAL14750
      ISTATE(12)=X                                                          PAL14760
      ISTATE(24)=N1                                                         PAL14770
C     PRINT TEST VECTORS                                                    PAL14780
      IF((.NOT.LSA11).AND.(.NOT.LSA01))WRITE(POF,60)                        PAL14790
     1                          NVECT,(ISTATE(I),I=1,24)                   PAL14800
   60 FORMAT(' ',I3,' ',24A1)                                               PAL14810
      GO TO 90                                                              PAL14820
C     TERMINATE SIMULATION                                                  PAL14830
C                                                                           PAL14840
   95 IF((.NOT.LERR).AND.(LSA11)) WRITE(POF,150) IPCTR4,IEQN1               PAL14850
```

```
  150 FORMAT(' ',' PRODUCT: ',I3,' OF ','EQUATION',I3,'                    PAL14860
     1 UNTESTED(SA1) FAULT')                                               PAL14870
      IF((.NOT.LERR).AND.(LSA01)) WRITE(POF,155) IPCTR4,IEQN1              PAL14880
  155 FORMAT(' ',' PRODUCT: ',I3,' OF ','EQUATION',I3,'                    PAL14890
     1 UNTESTED(SA0) FAULT')                                               PAL14900
C                                                                          PAL14910
      IF((.NOT.LERR).AND.((.NOT.LSA11).AND.(.NOT.LSA01))) WRITE(POF,67)    PAL14920
   67 FORMAT(/,' PASS SIMULATION')                                         PAL14930
      IPCTR=IPCTR/(NVECT-1)                                                PAL14940
      IF((      LERR).AND.((.NOT.LSA11).AND.(.NOT.LSA01)))                 PAL14950
     1WRITE(POF,68) NERR                                                   PAL14960
   68 FORMAT(/,' NUMBER OF FUNCTION TABLE ERRORS =',I3)                    PAL14970
      RETURN                                                               PAL14980
C     PRINT AN ERROR MESSAGE FOR AN UNDEFINED PIN NAME                     PAL14990
  100 ILERR=ILL+4                                                          PAL15000
      WRITE(PMS,101) (IBUF(I,1),I=1,8),ILERR,(IPAGE(I,ILL),I=1,80)         PAL15010
  101 FORMAT(/,' ERROR SYMBOL =  ',8A1,'      IN LINE NUMBER ',I3,         PAL15020
     1       /,' ',80A1,/,' THIS PIN NAME IS NOT DEFINED IN THE',          PAL15030
     2                 ' FUNCTION TABLE PIN LIST')                         PAL15040
      RETURN                                                               PAL15050
C                                                                          PAL15060
  110 IPROD=H                                                              PAL15070
      LSA12=.TRUE.                                                         PAL15080
      IEQN1=IEQN                                                           PAL15090
      IPCTR4=IPCTR3                                                        PAL15100
      GO TO 38                                                             PAL15110
C                                                                          PAL15120
C                                                                          PAL15130
C                                                                          PAL15140
  120 IPROD=L                                                              PAL15150
      LSA02=.TRUE.                                                         PAL15160
      IEQN1=IEQN                                                           PAL15170
      IPCTR4=IPCTR3                                                        PAL15180
      GO TO    121                                                         PAL15190
C                                                                          PAL15200
C                                                                          PAL15210
C                                                                          PAL15220
  115 ISAF=ISAF+1                                                          PAL15230
      LERR=.FALSE.                                                         PAL15240
      RETURN                                                               PAL15250
C                                                                          PAL15260
      END                                                                  PAL15270
```

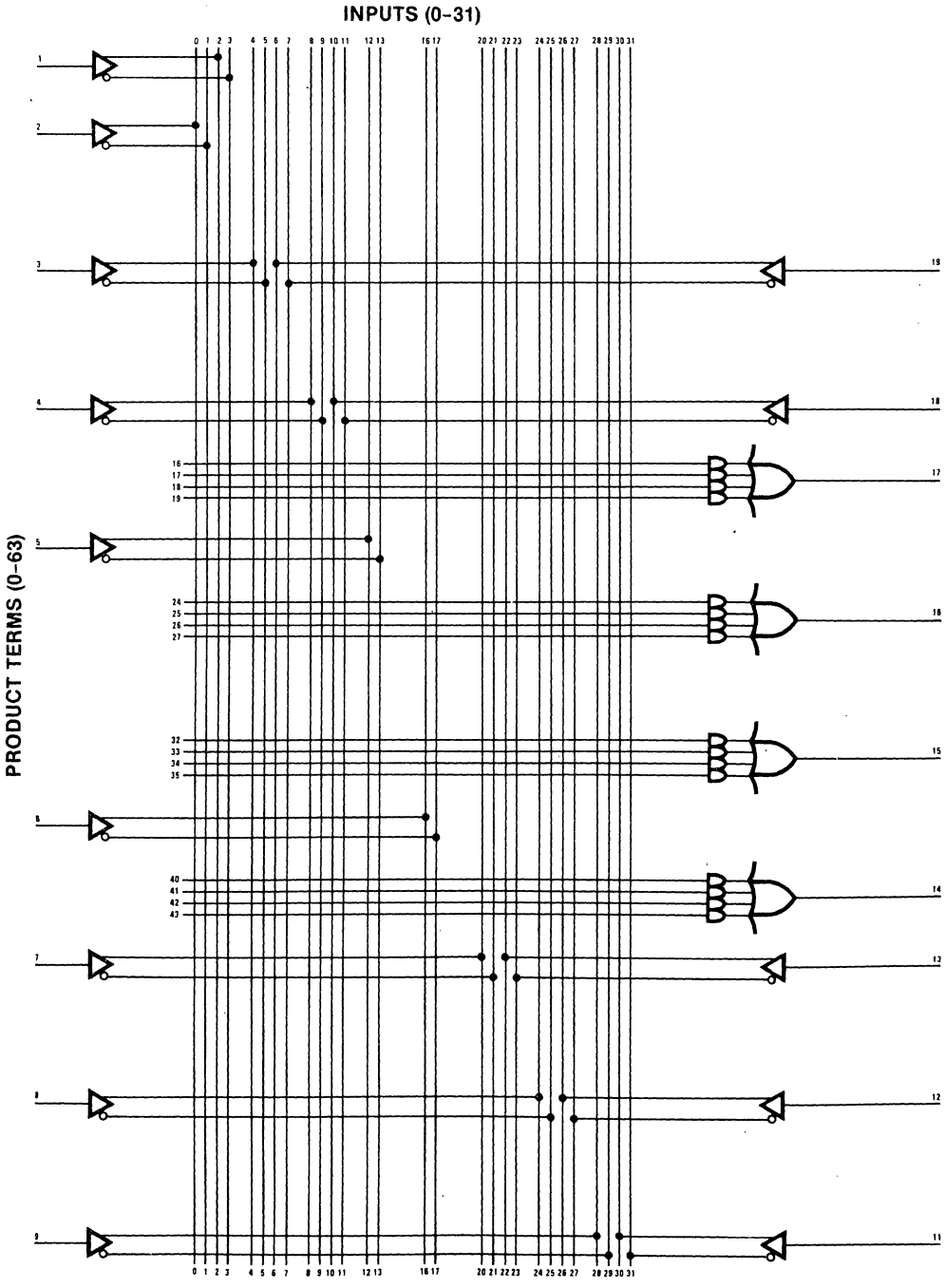
Logic Diagram PAL10H8



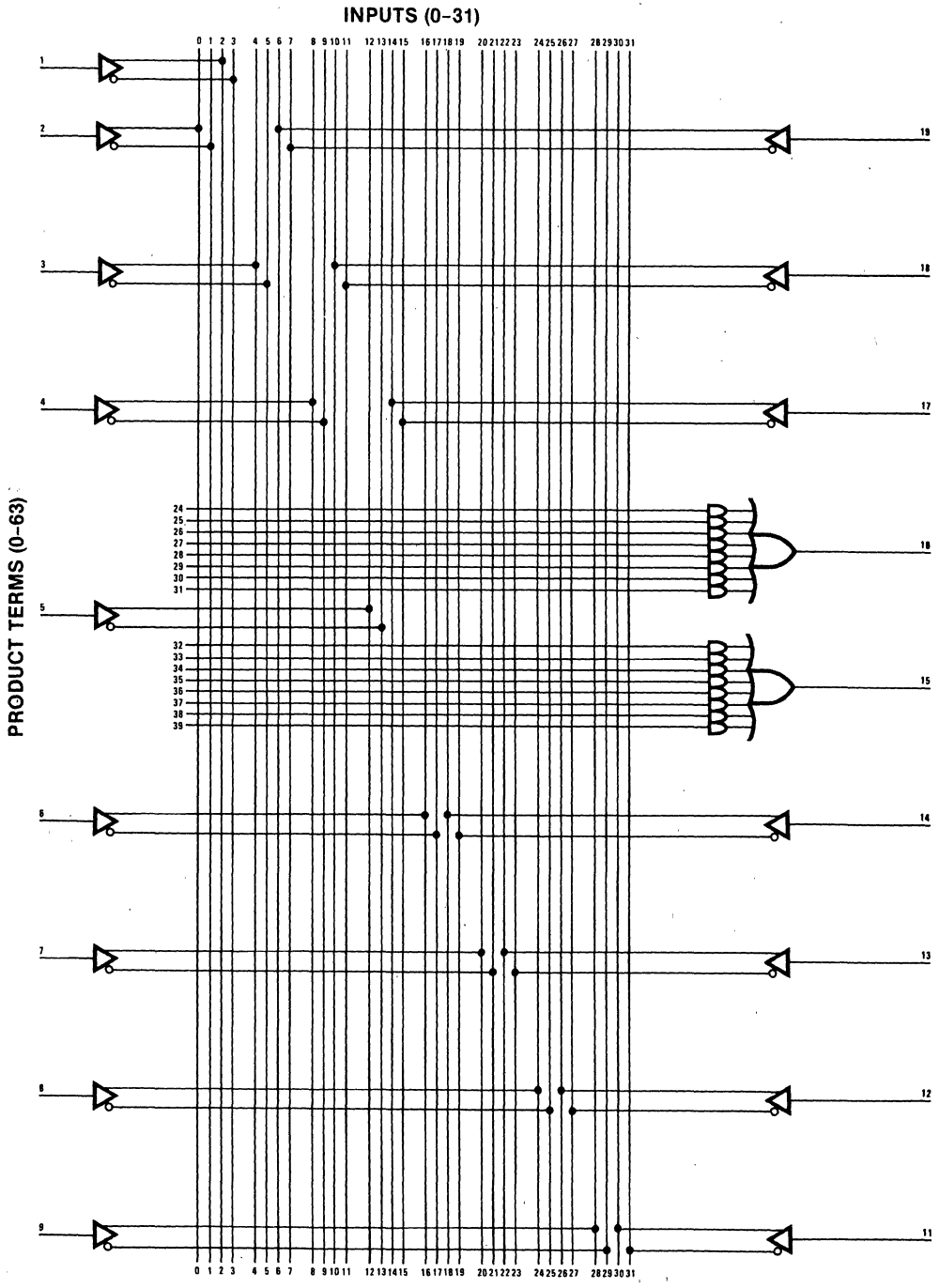
Logic Diagram PAL12H6



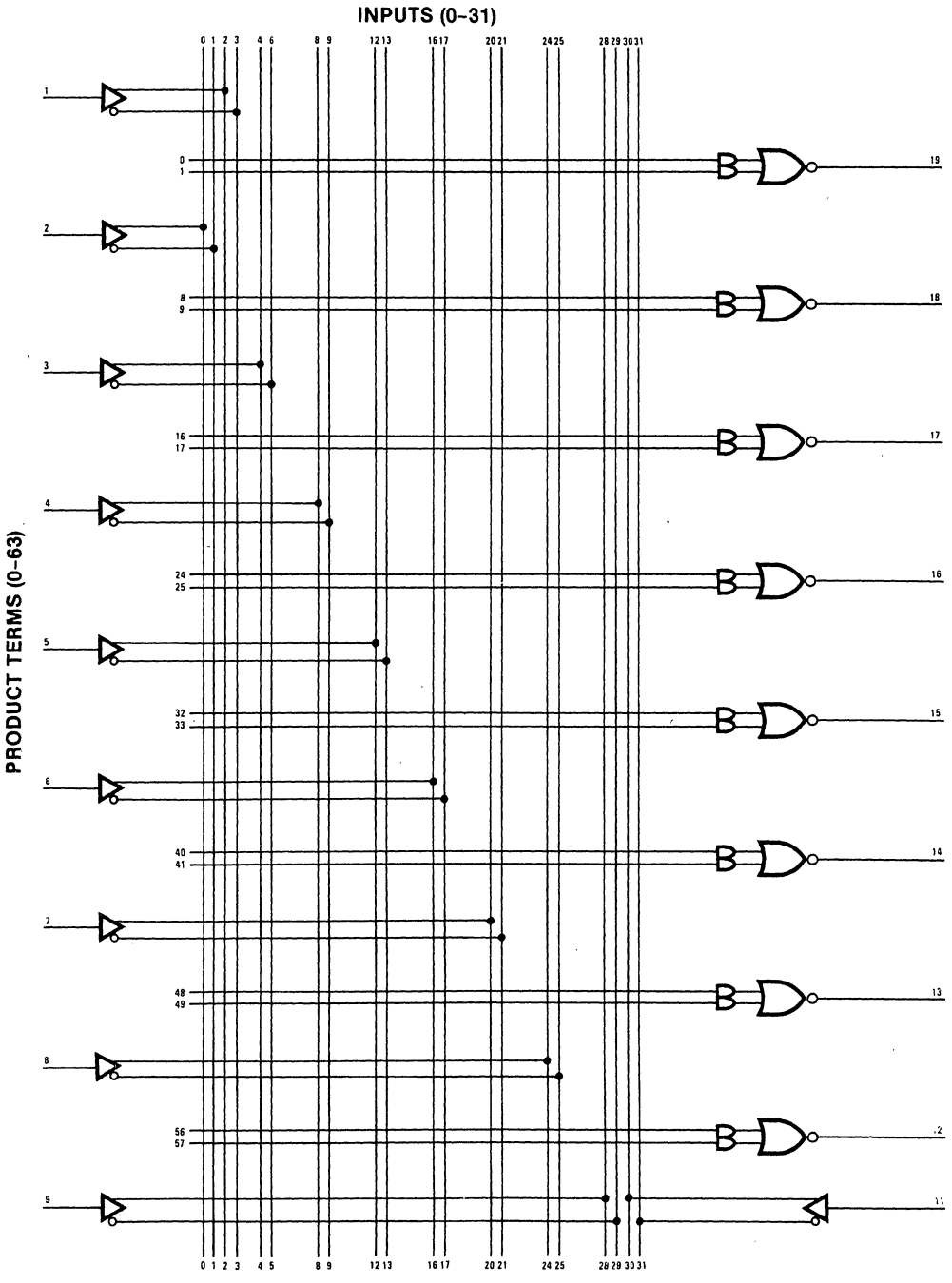
Logic Diagram PAL14H4



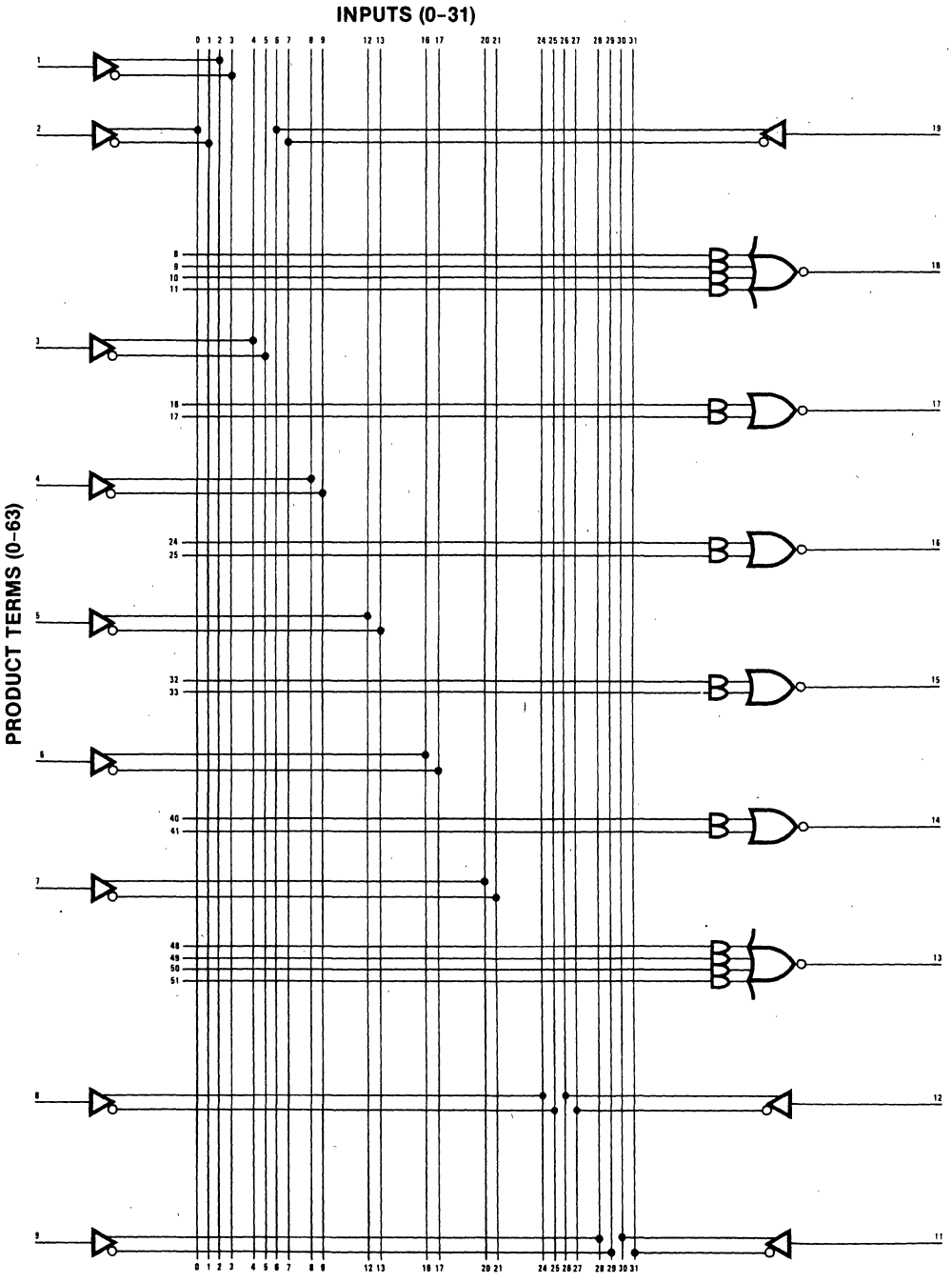
Logic Diagram PAL16H2



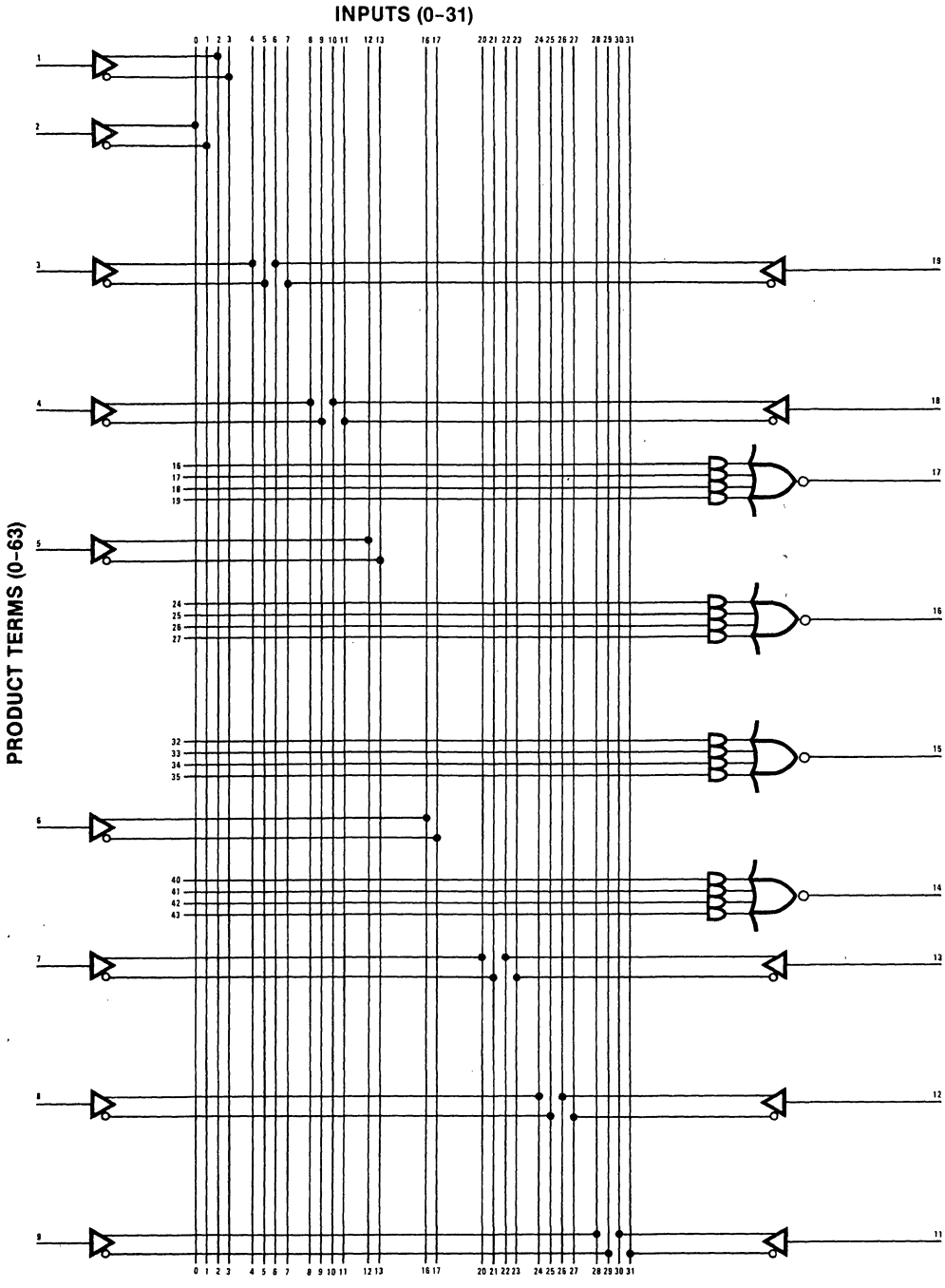
Logic Diagram PAL10L8



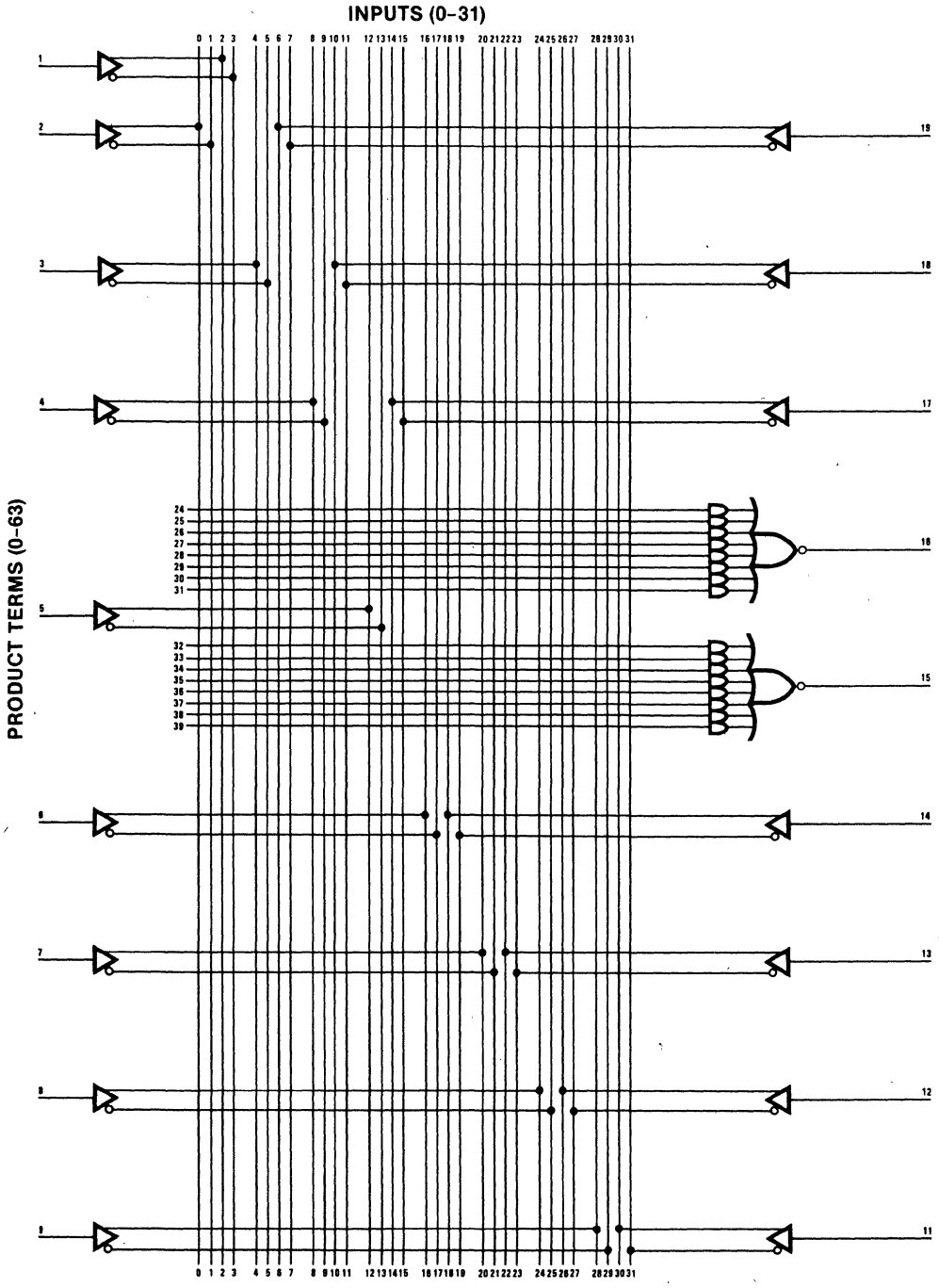
Logic Diagram PAL 12L6



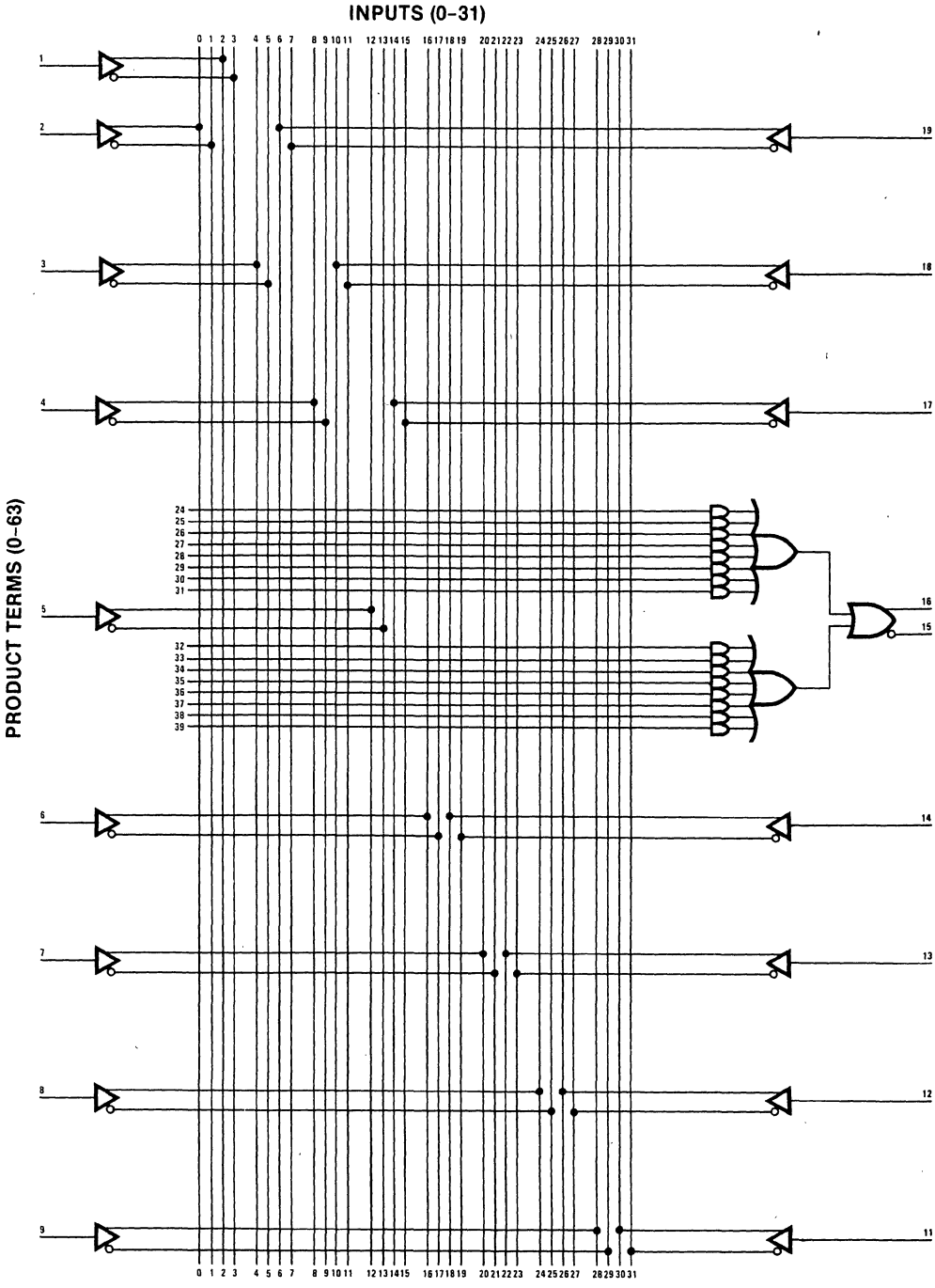
Logic Diagram PAL14L4



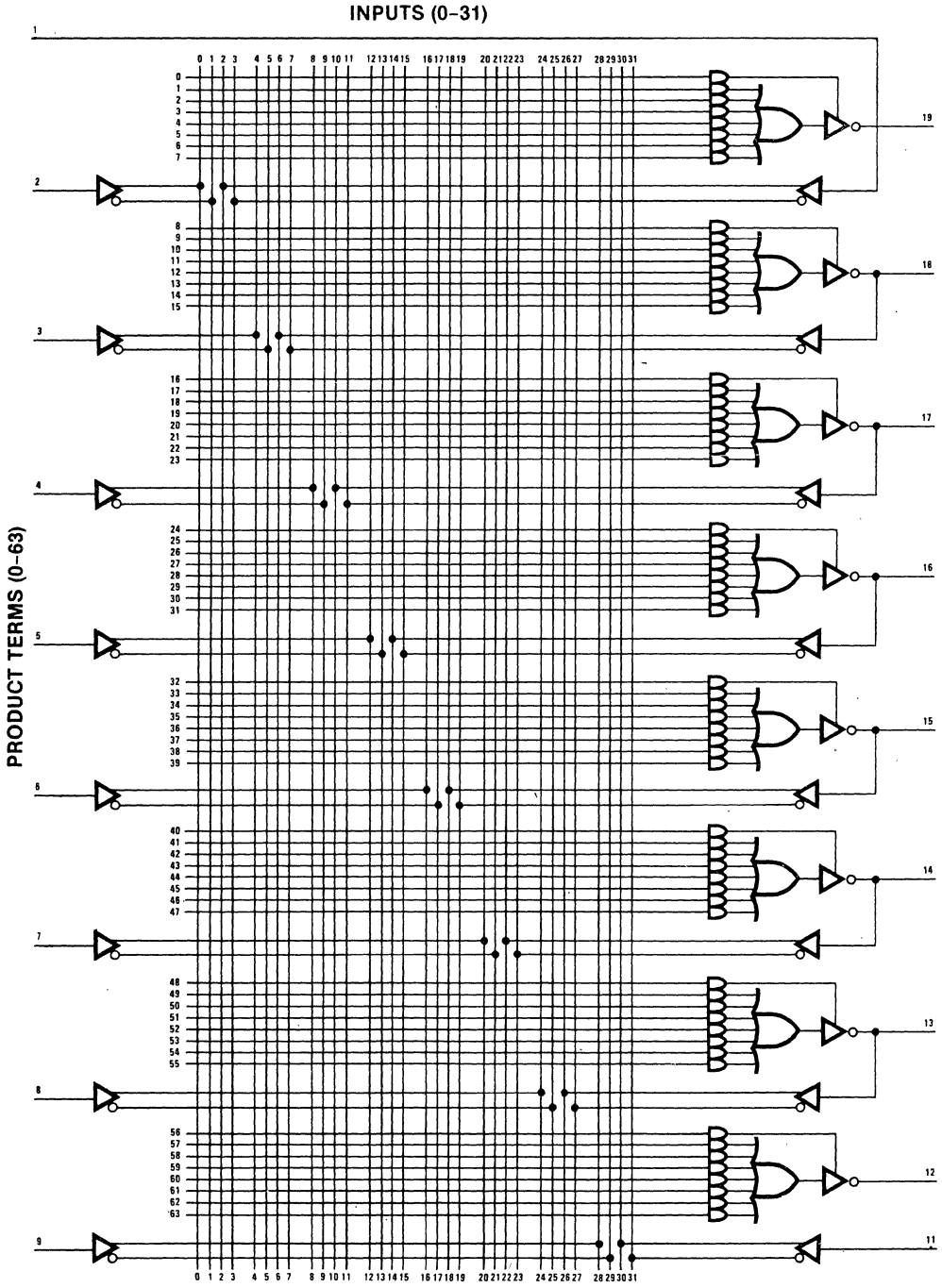
Logic Diagram PAL16L2



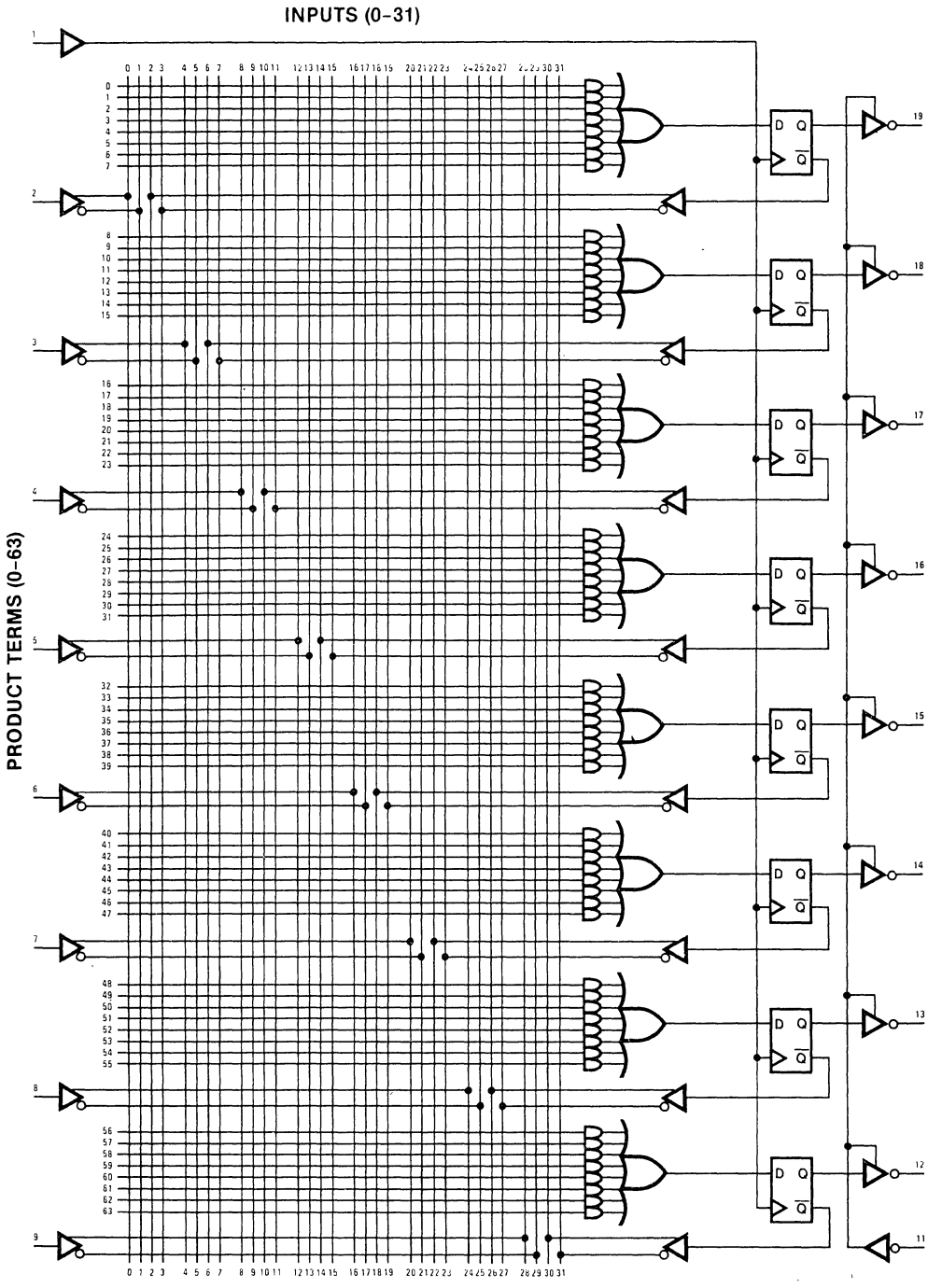
Logic Diagram PAL16C1



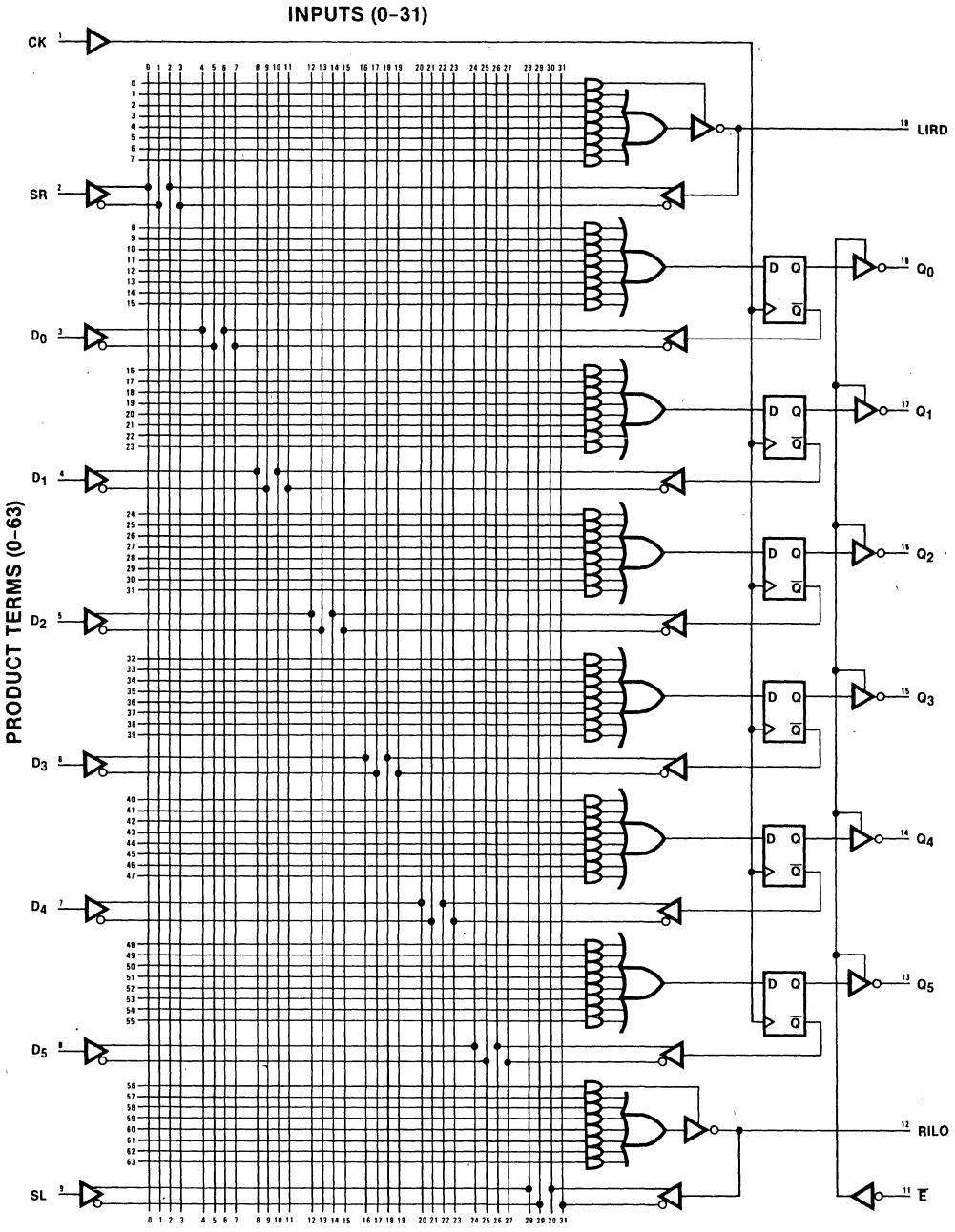
Logic Diagram PAL16L8



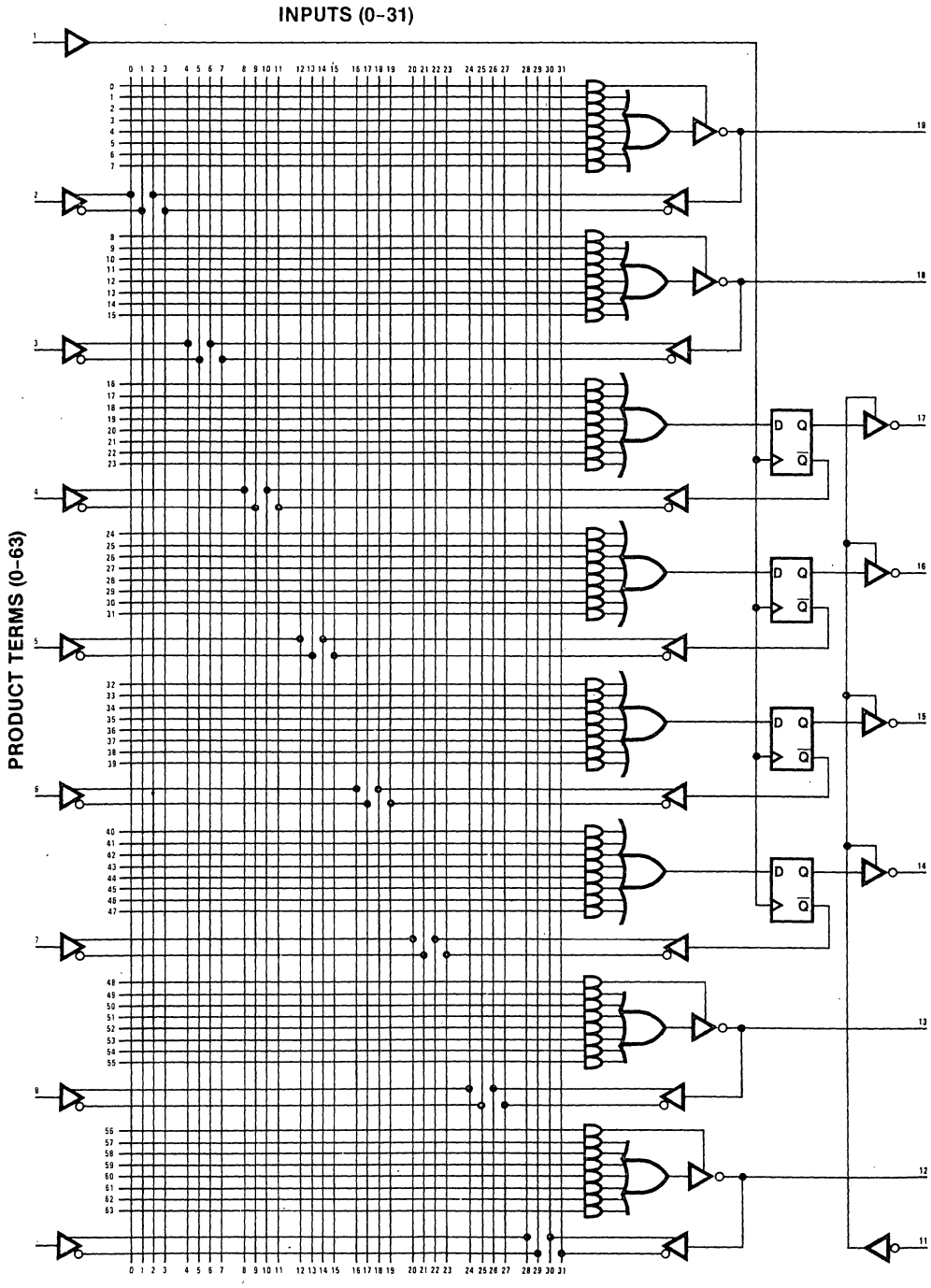
Logic Diagram PAL16R8



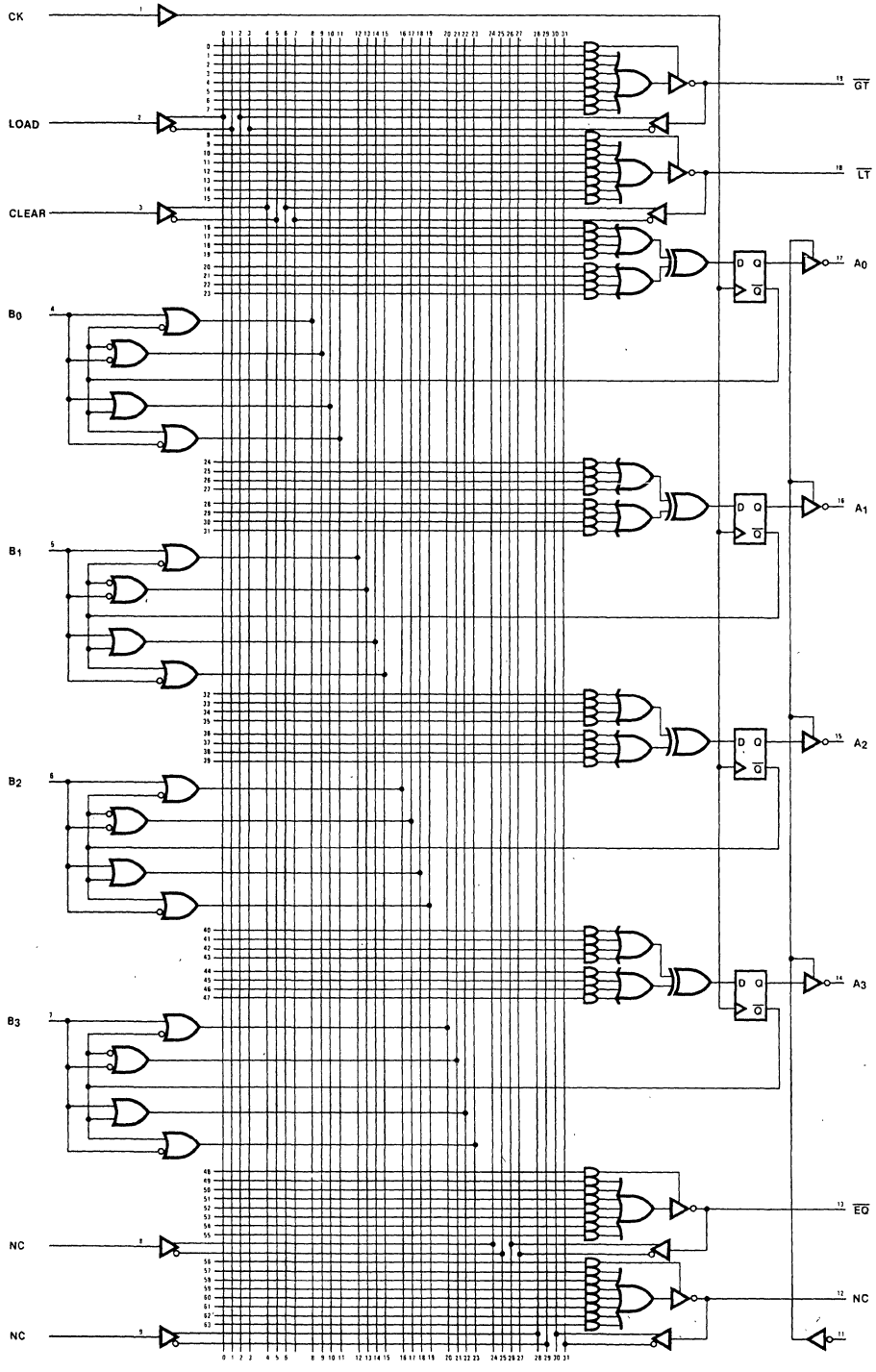
Logic Diagram PAL16R6



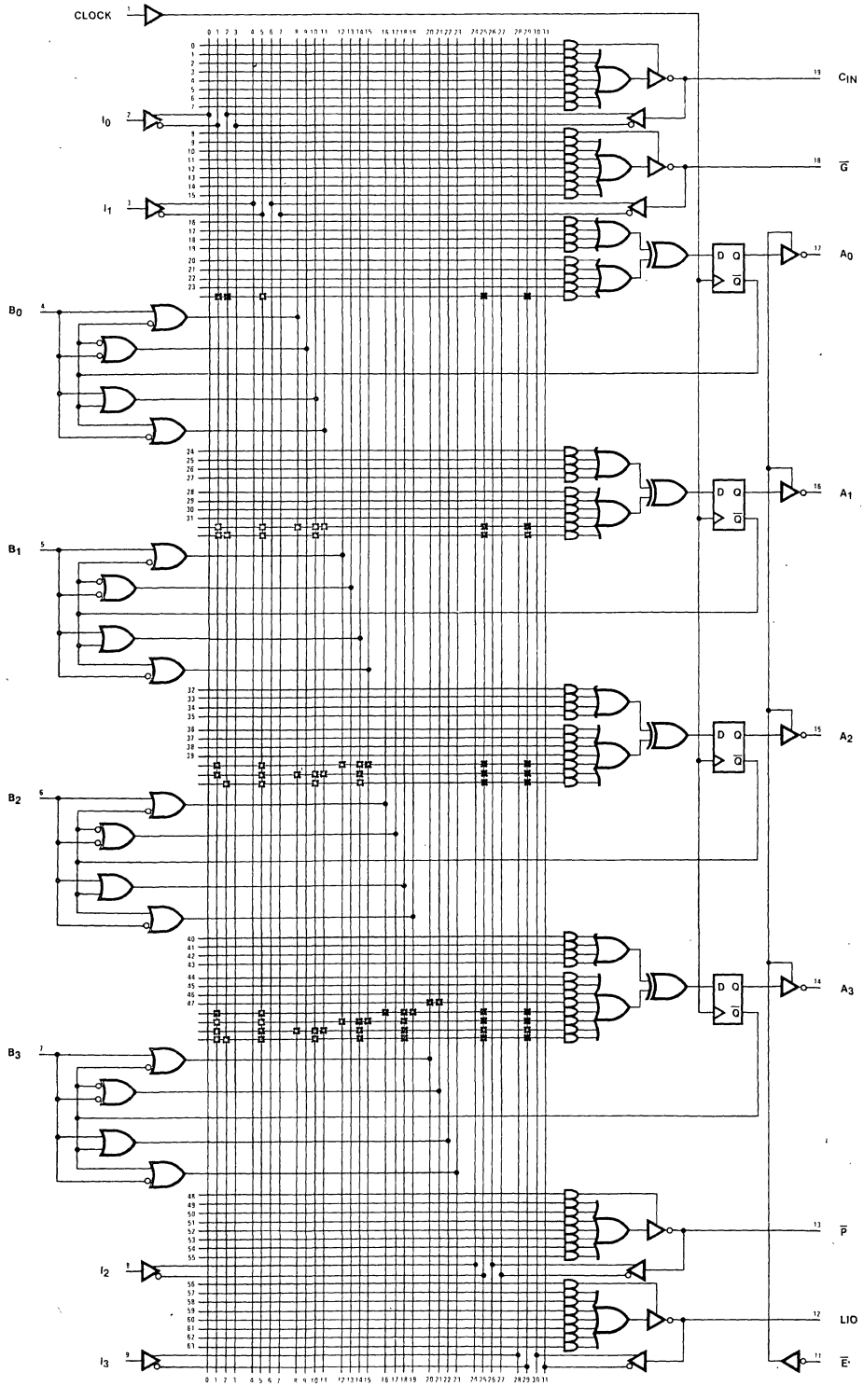
Logic Diagram PAL16R4



Logic Diagram PAL16X4

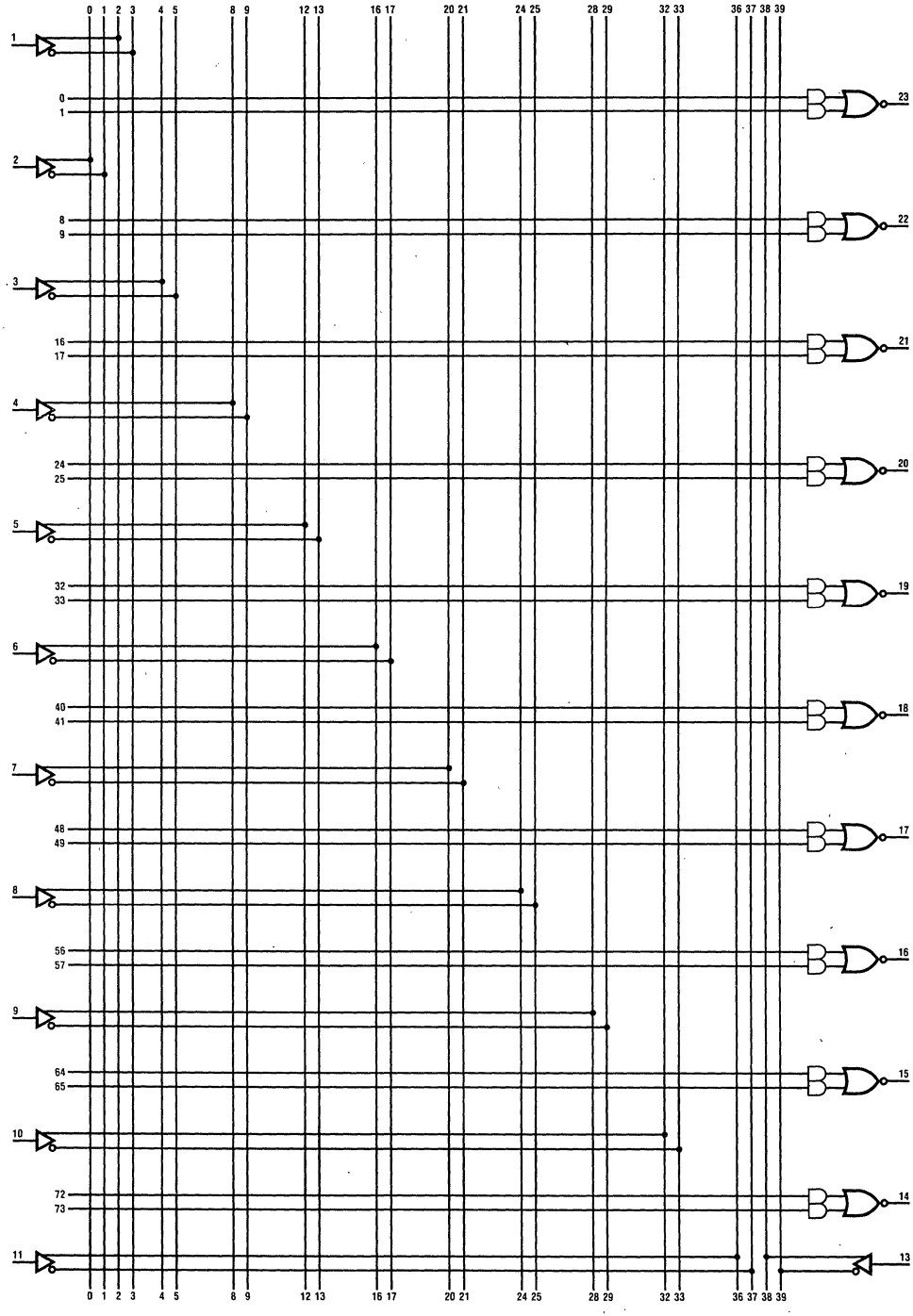


Logic Diagram PAL16A4



Logic Diagram

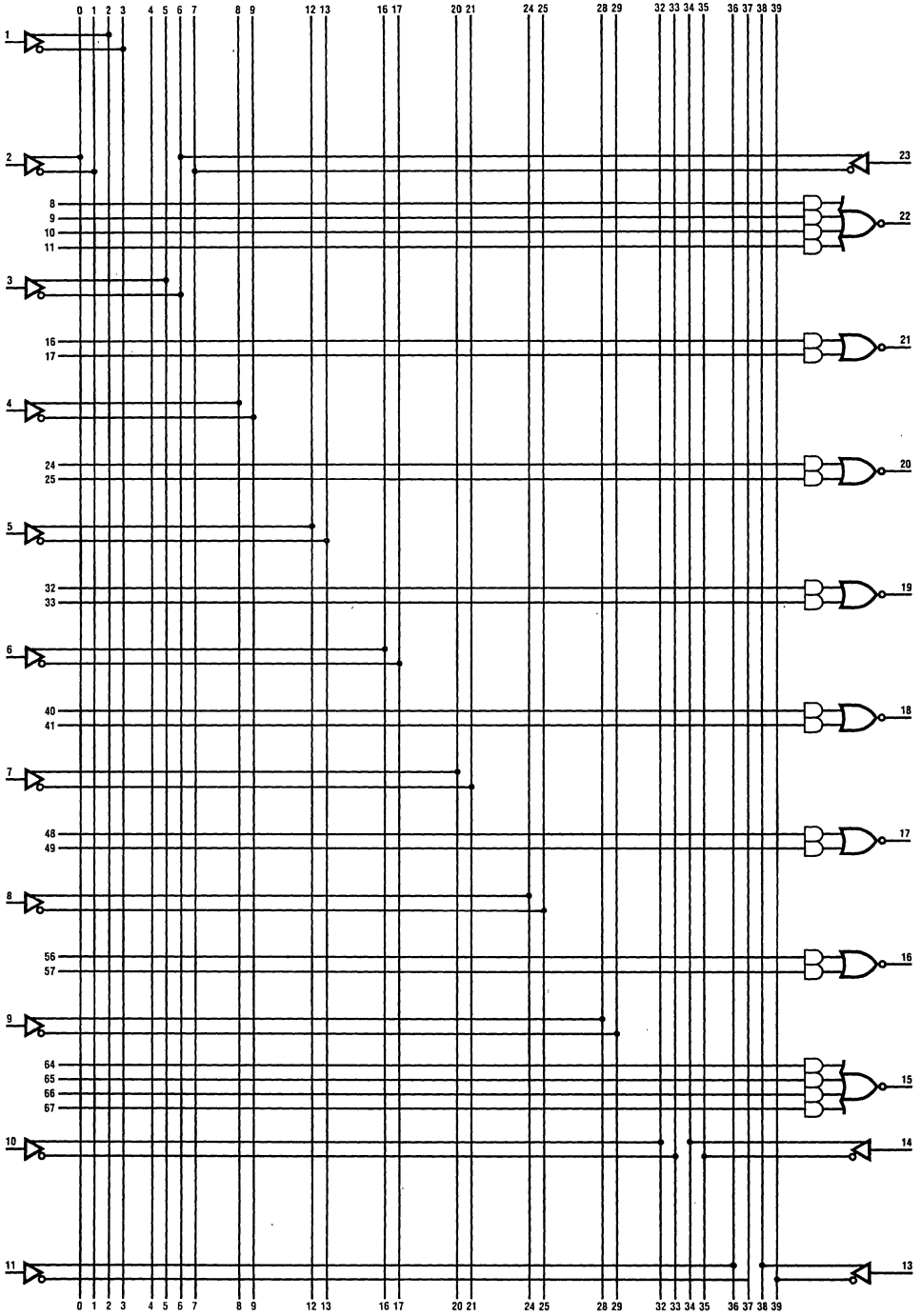
DMPAL12L10



Logic Diagram

DMPAL14L8

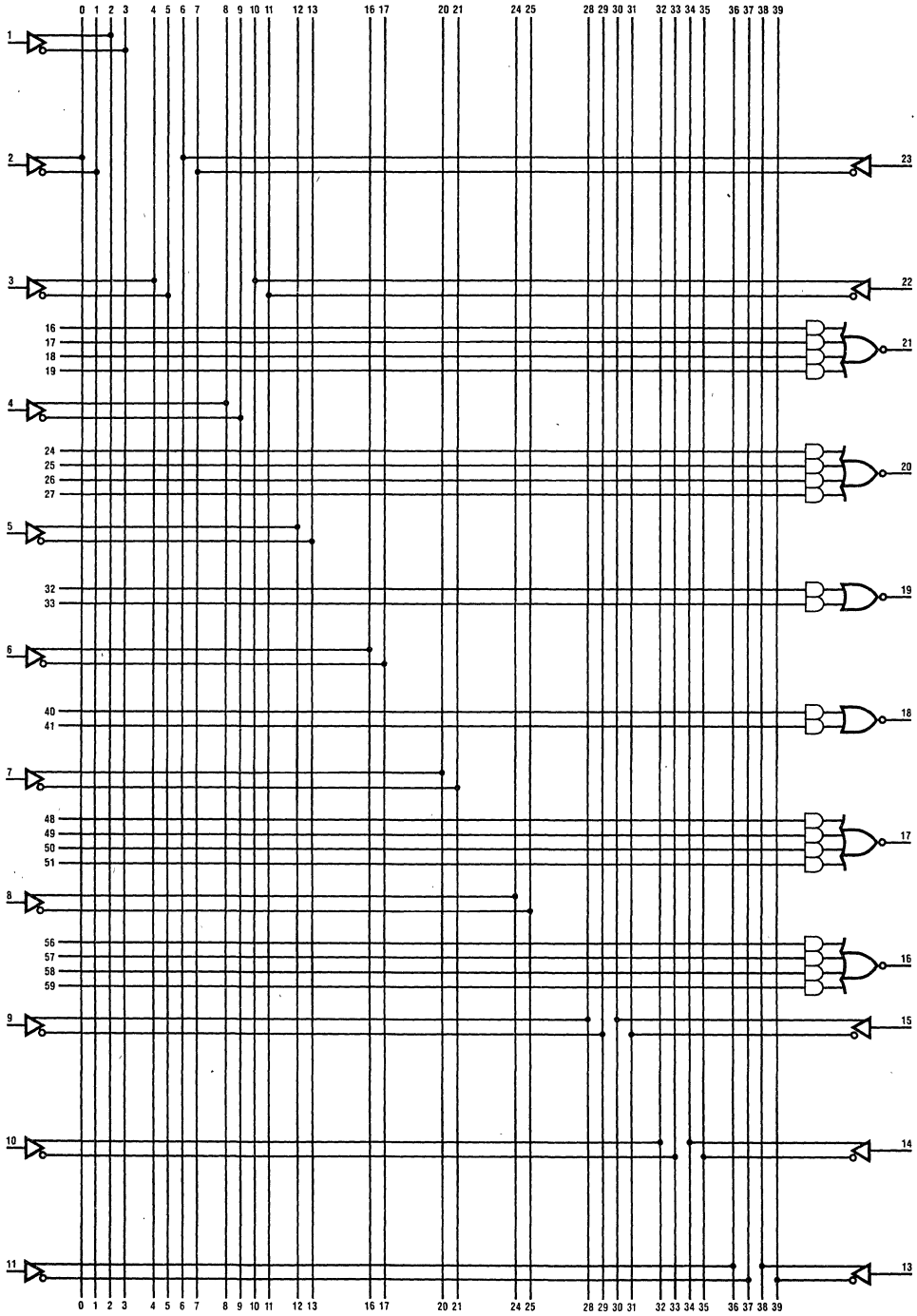
Inputs (0–39)



Logic Diagram

DMPAL16L6

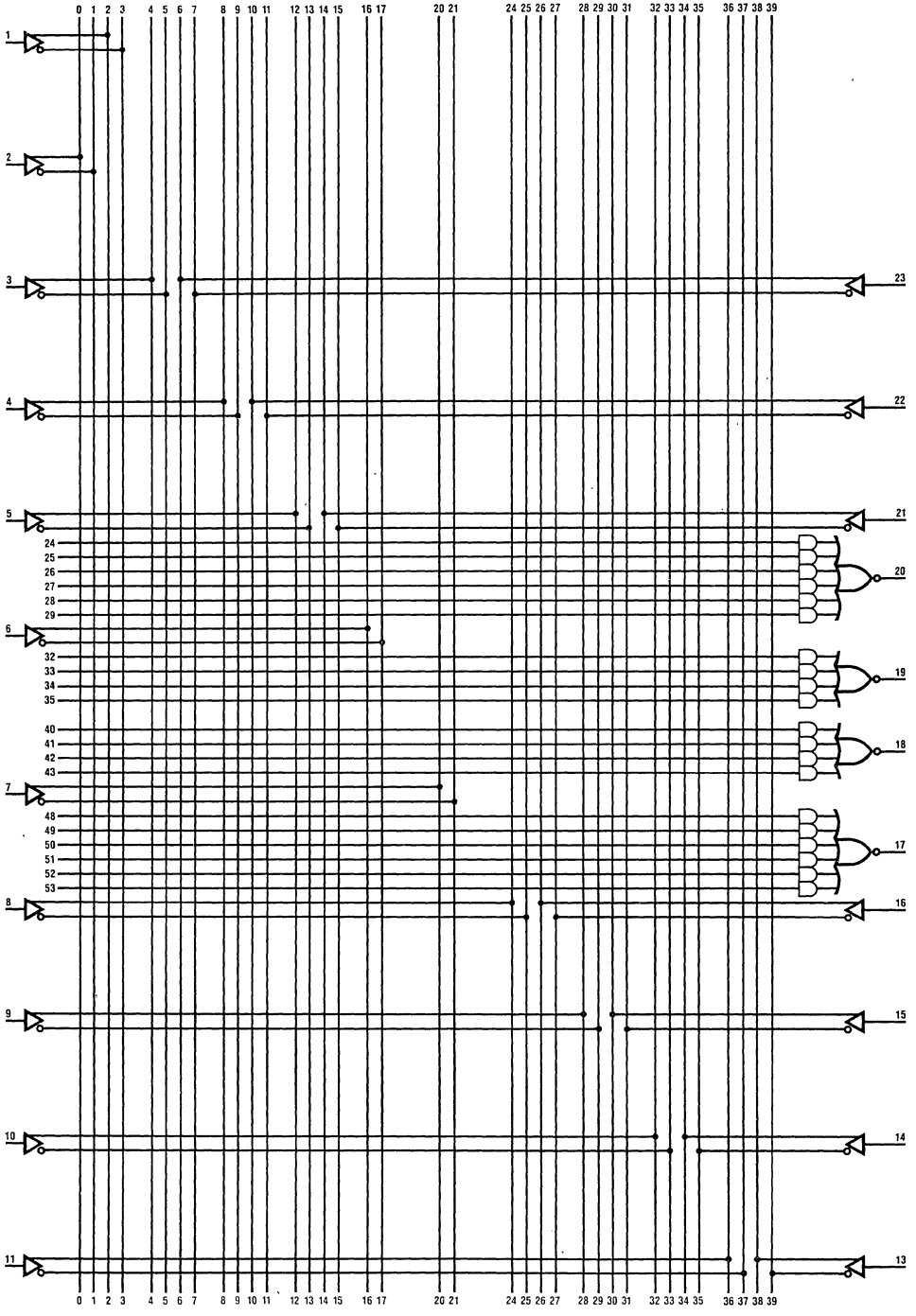
Inputs (0–39)



Logic Diagram

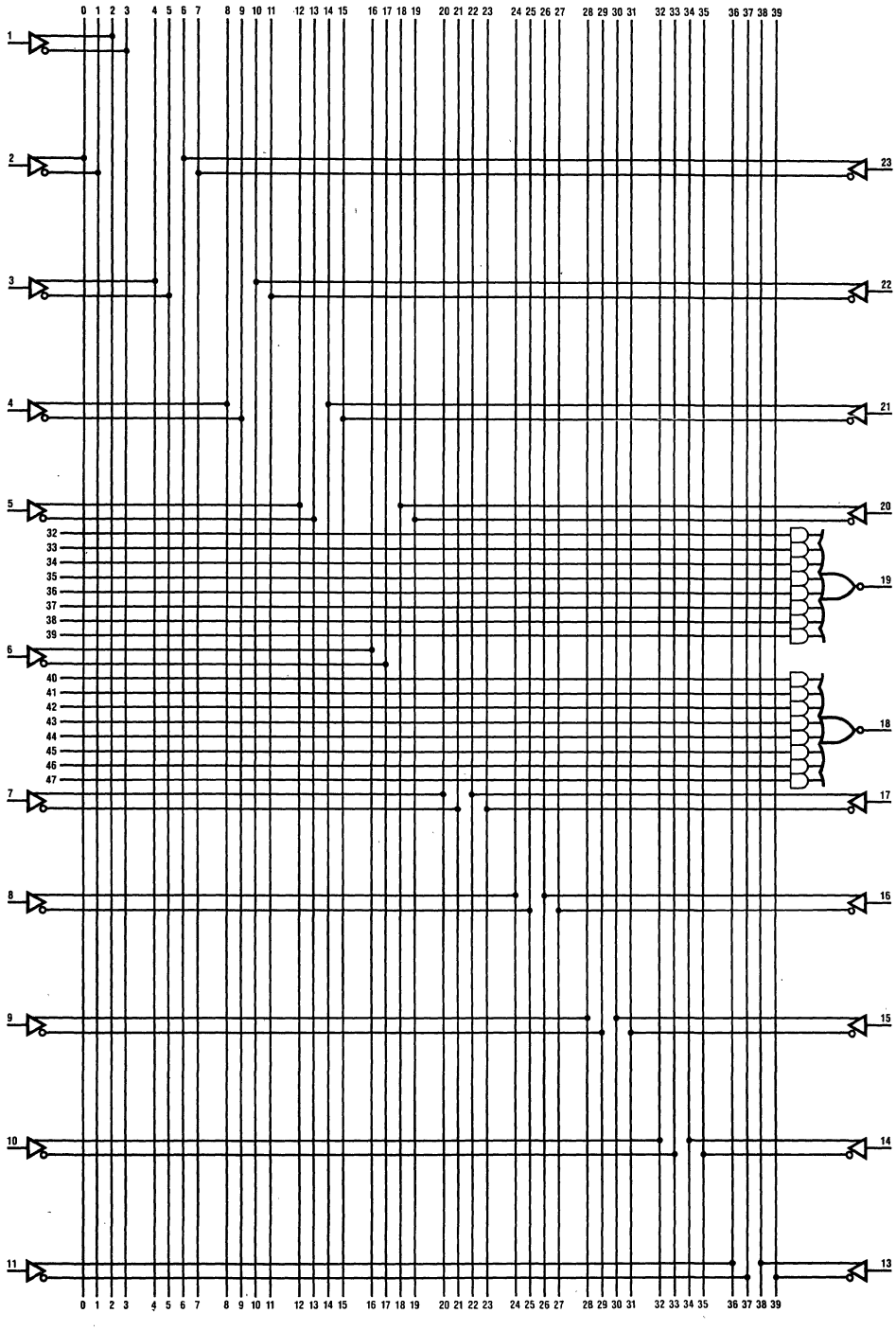
DMPAL18L4

Inputs (0-39)



Logic Diagram

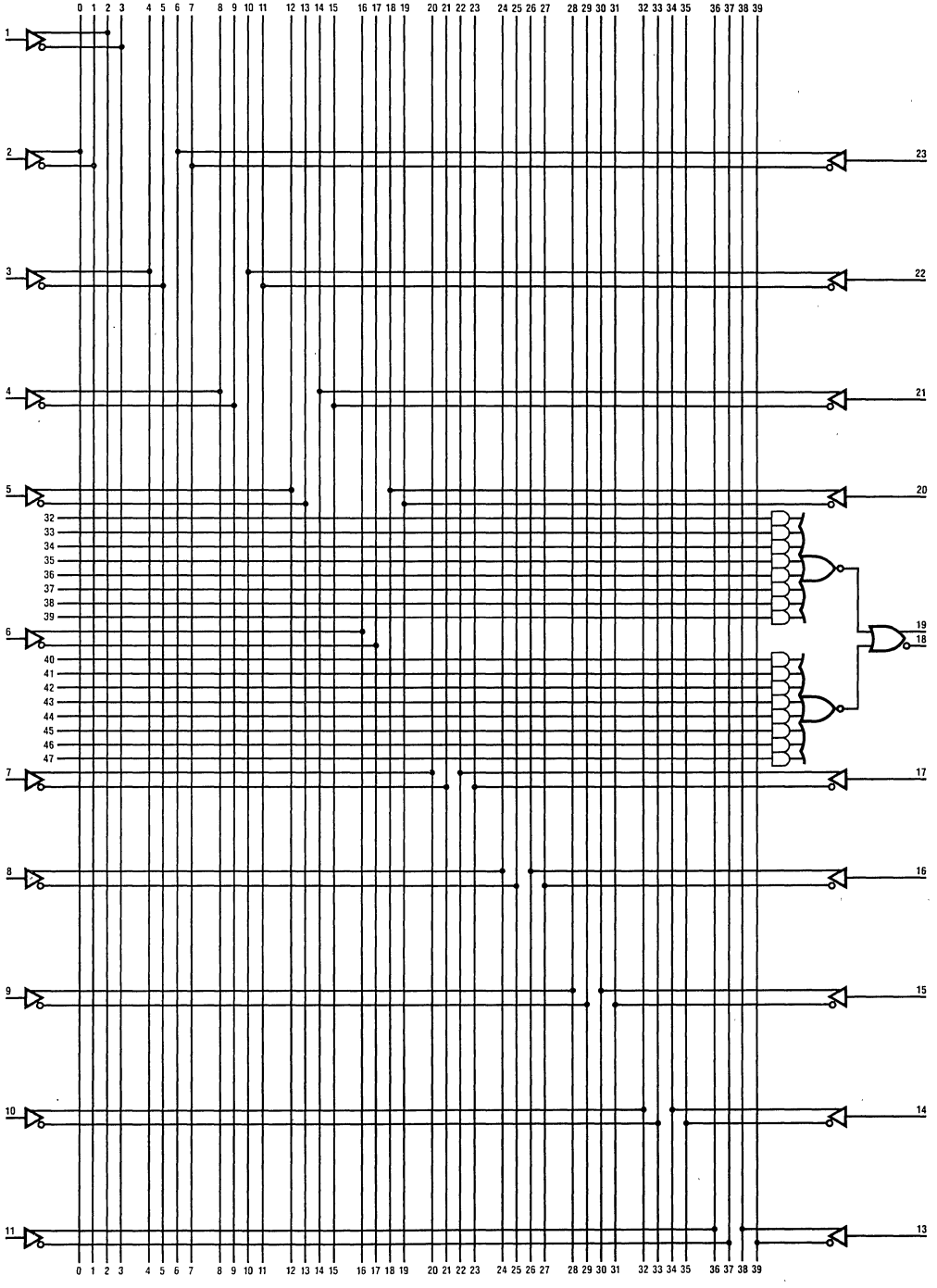
DMPAL20L2



Logic Diagram

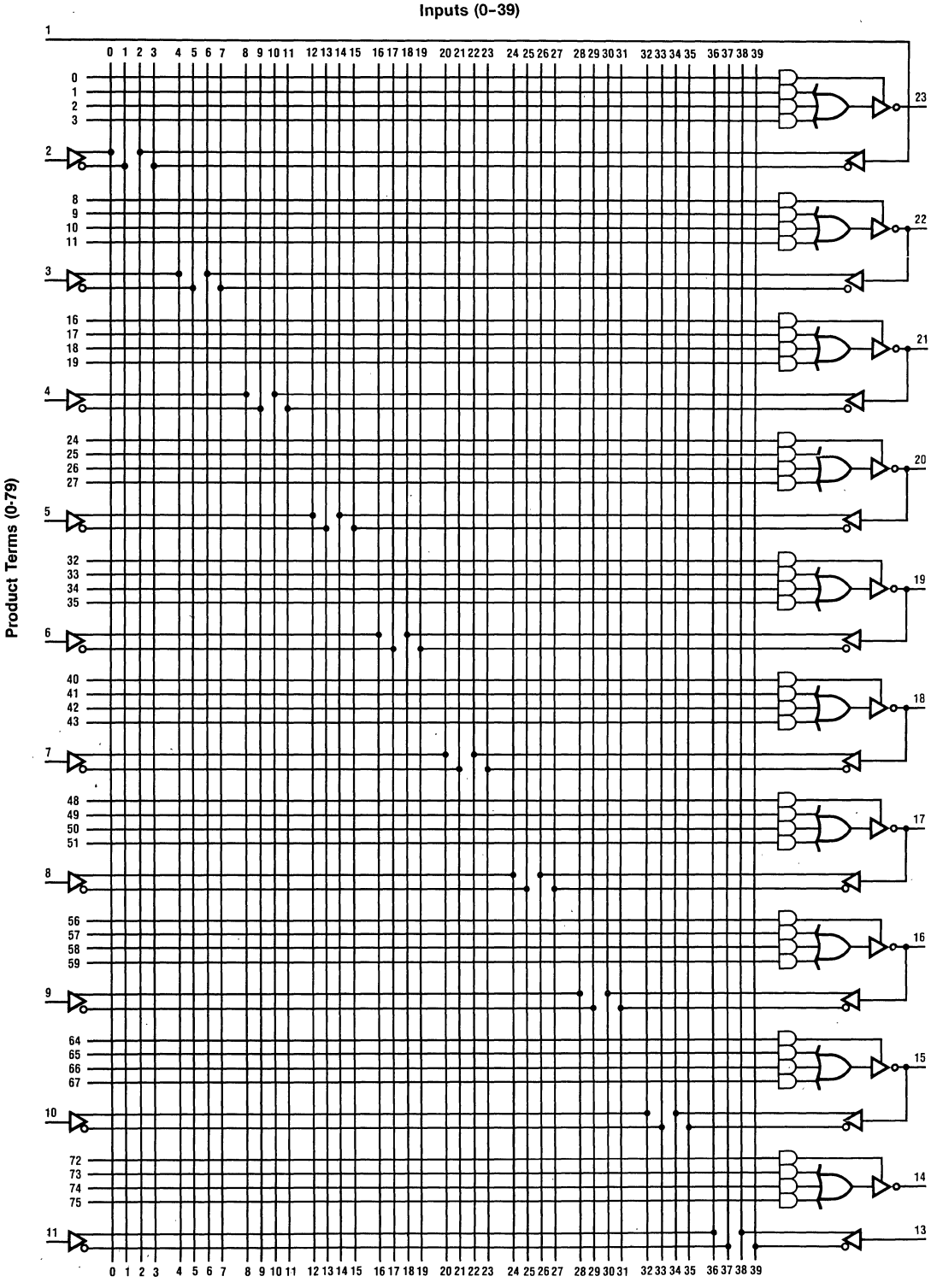
DMPAL20C1

Inputs (0-39)



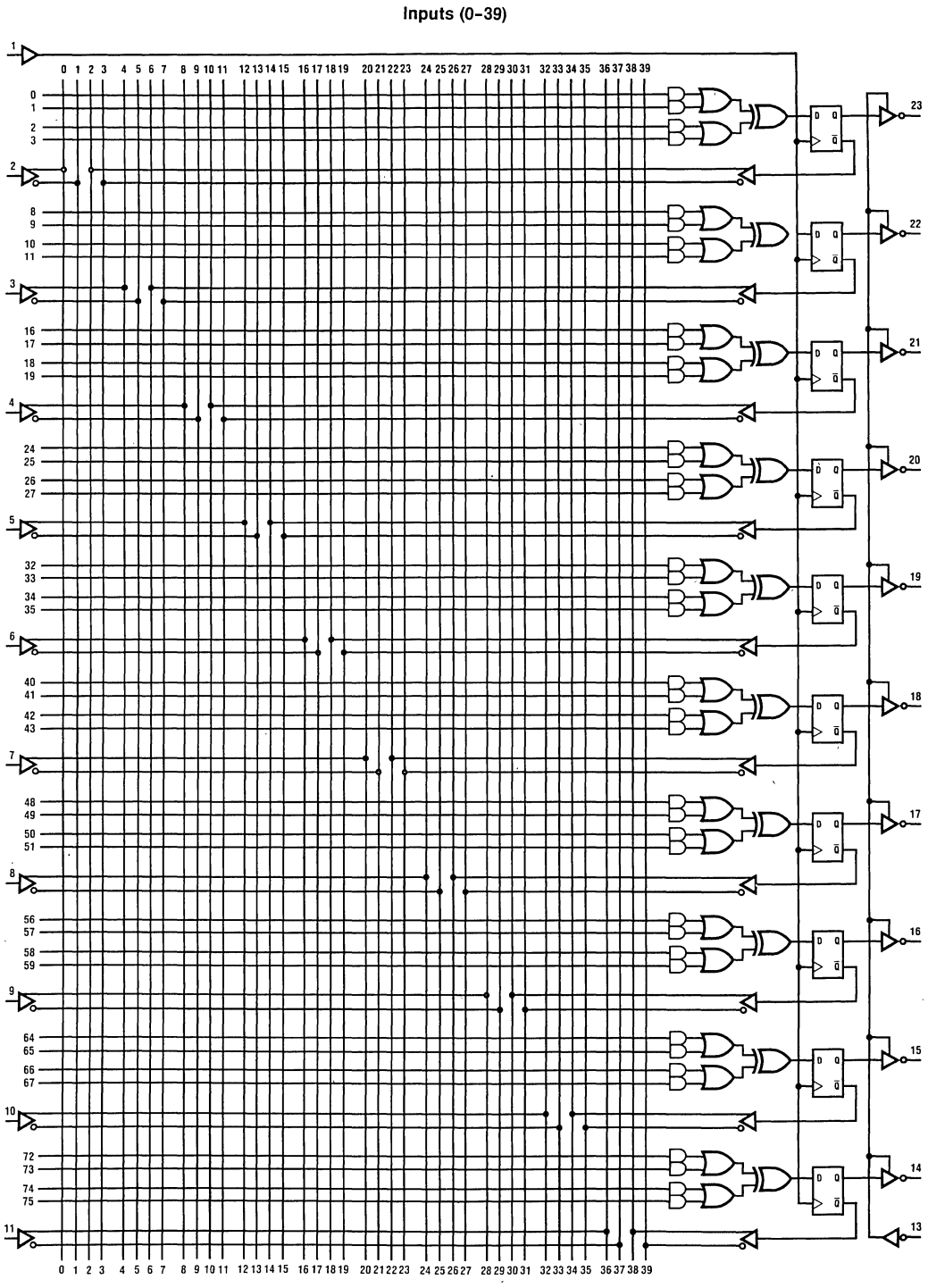
Logic Diagram

DMPAL20L10



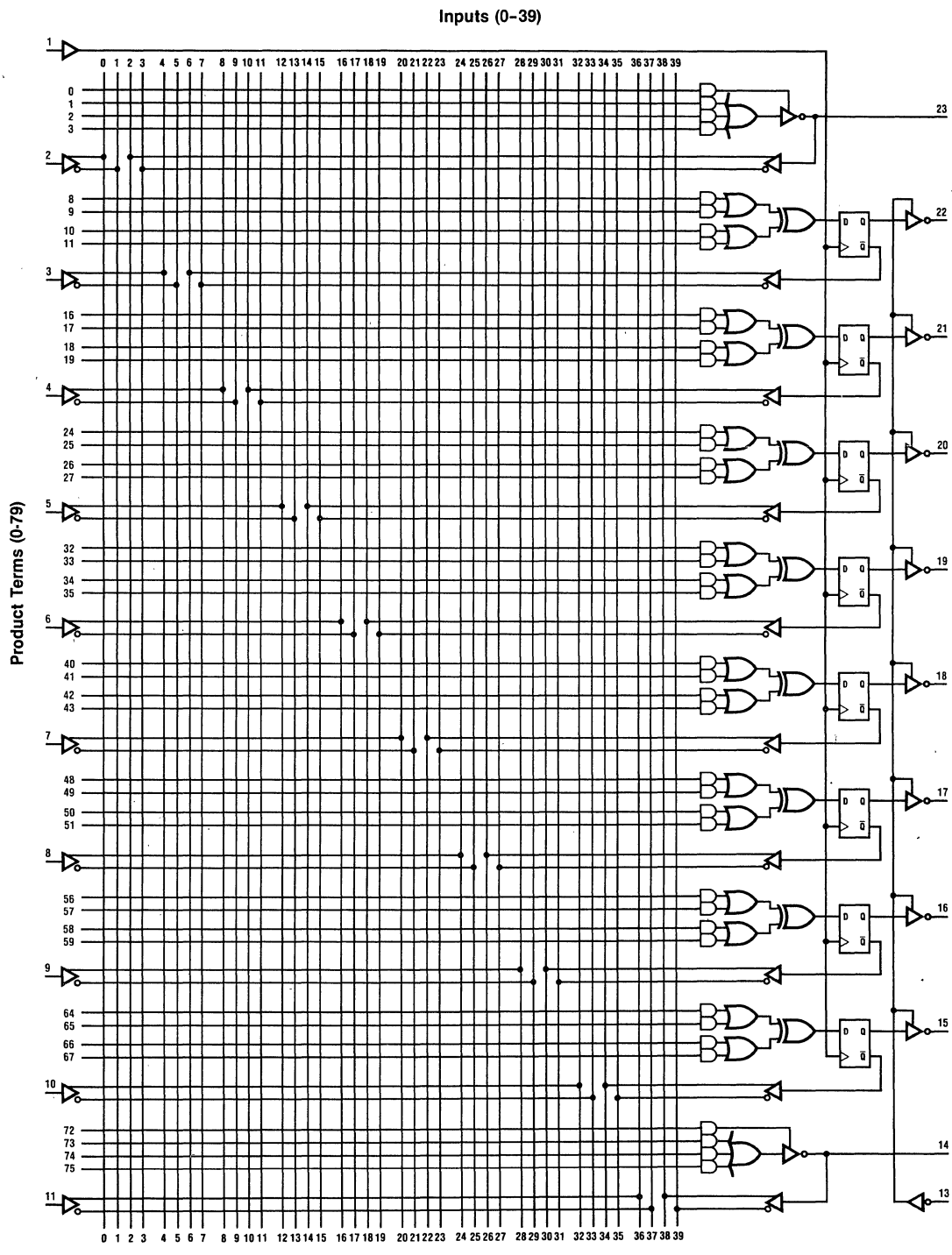
Logic Diagram

DMPAL20X10



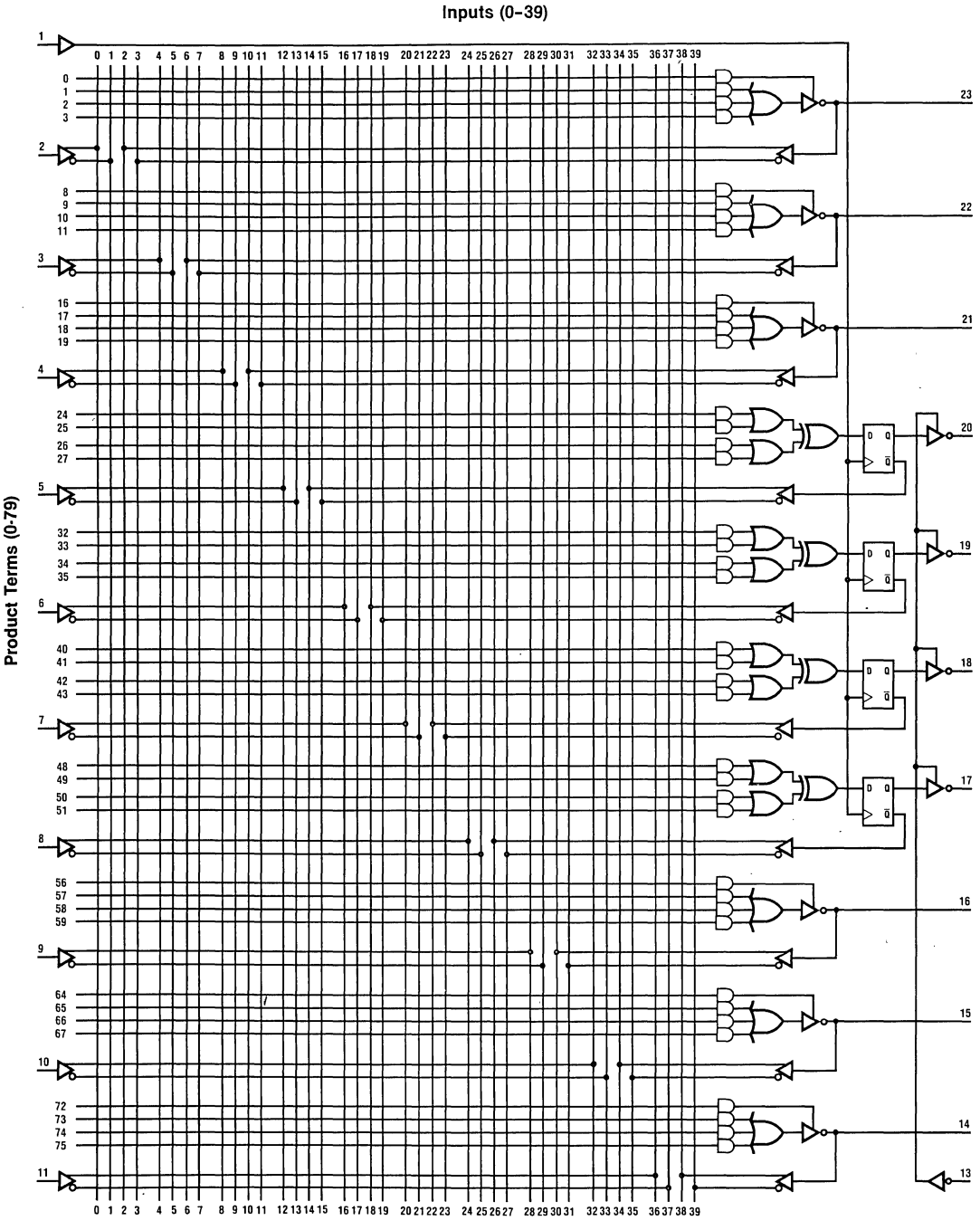
Logic Diagram

DMPAL20X8



Logic Diagram

DMPAL20X4



PAL LOGIC DIAGRAMS AND PROGRAMMING FORMAT CODING SHEETS FOR PAL 20 SERIES

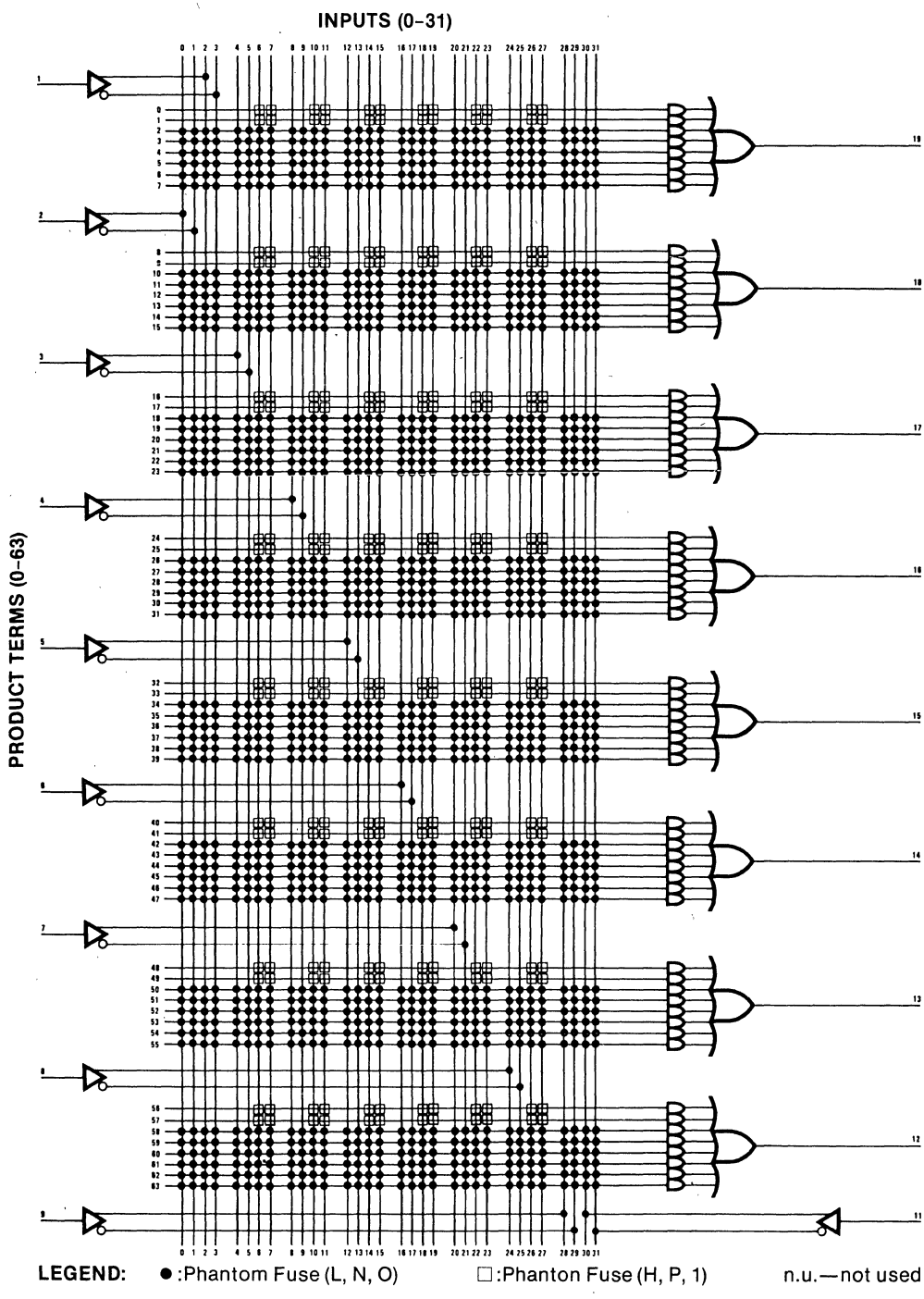


FIGURE 3-32. Logic Diagram, PAL10H8.

Programming Format PAL10H8

PATTERN: _____ NAME: _____

DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0_4 24							H	H			H	H			H	H			H	H			H	H			H	H				
0_3 16							H	H			H	H			H	H			H	H			H	H			H	H				
0_2 8							H	H			H	H			H	H			H	H			H	H			H	H				
0_1 0							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
0_4 25							H	H			H	H			H	H			H	H			H	H			H	H				
0_3 17							H	H			H	H			H	H			H	H			H	H			H	H				
0_2 9							H	H			H	H			H	H			H	H			H	H			H	H				
0_1 1							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
0_4 26	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 18	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 10	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
0_4 27	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 19	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 11	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 3	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
0_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
0_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
0_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 6	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 7	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
0_4 56							H	H			H	H			H	H			H	H			H	H			H	H				
0_3 48							H	H			H	H			H	H			H	H			H	H			H	H				
0_2 40							H	H			H	H			H	H			H	H			H	H			H	H				
0_1 32							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
0_4 57							H	H			H	H			H	H			H	H			H	H			H	H				
0_3 49							H	H			H	H			H	H			H	H			H	H			H	H				
0_2 41							H	H			H	H			H	H			H	H			H	H			H	H				
0_1 33							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
0_4 58	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 50	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 42	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 34	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
0_4 59	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 51	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 43	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 35	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
0_4 60	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
0_4 61	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
0_4 62	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
0_4 63	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-33. Programming Format Sheet, PAL10H8.

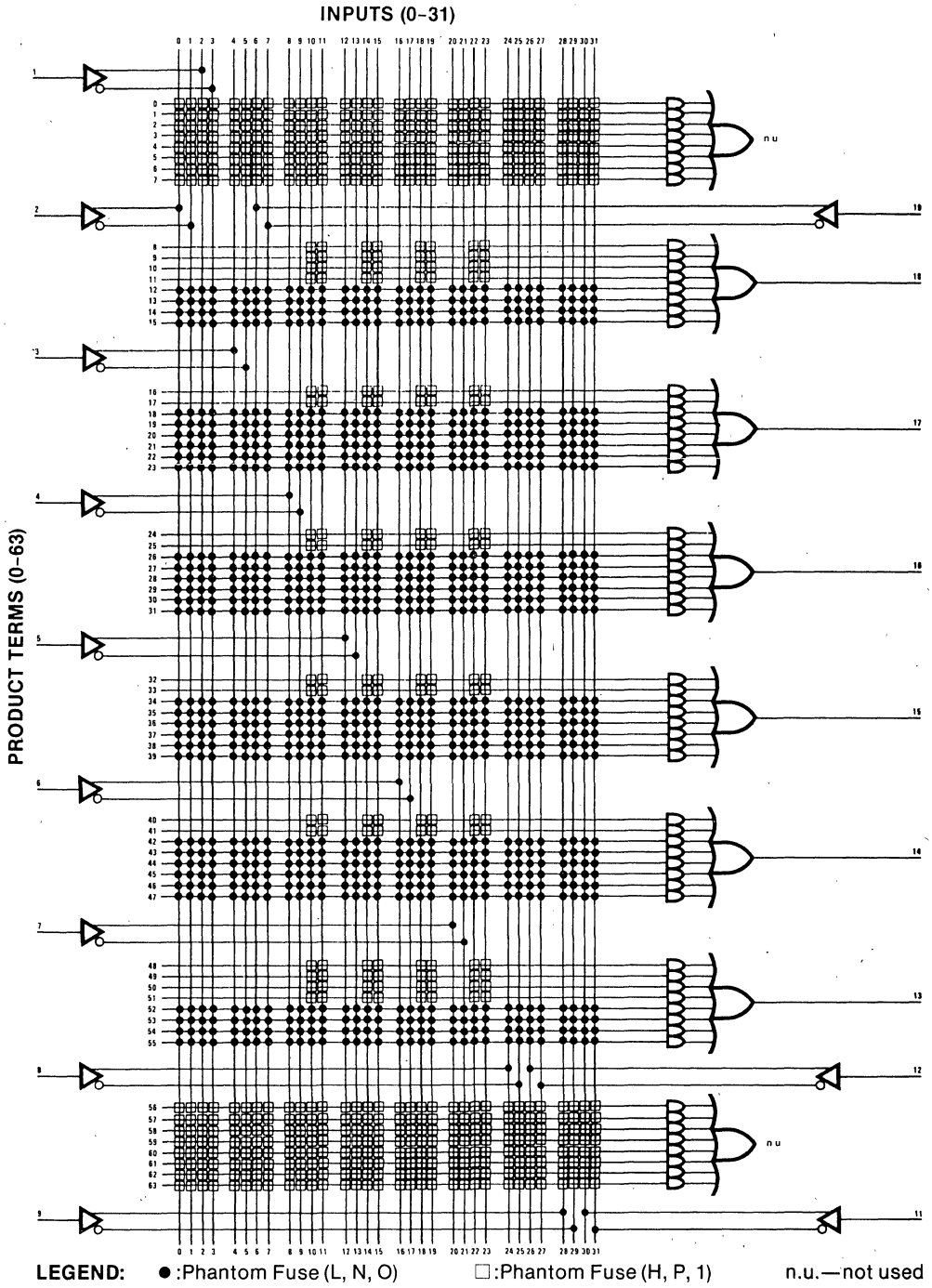


FIGURE 3-34. Logic Diagram, PAL12H6.

Programming Format PAL12H6

PATTERN: _____ NAME: _____

DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

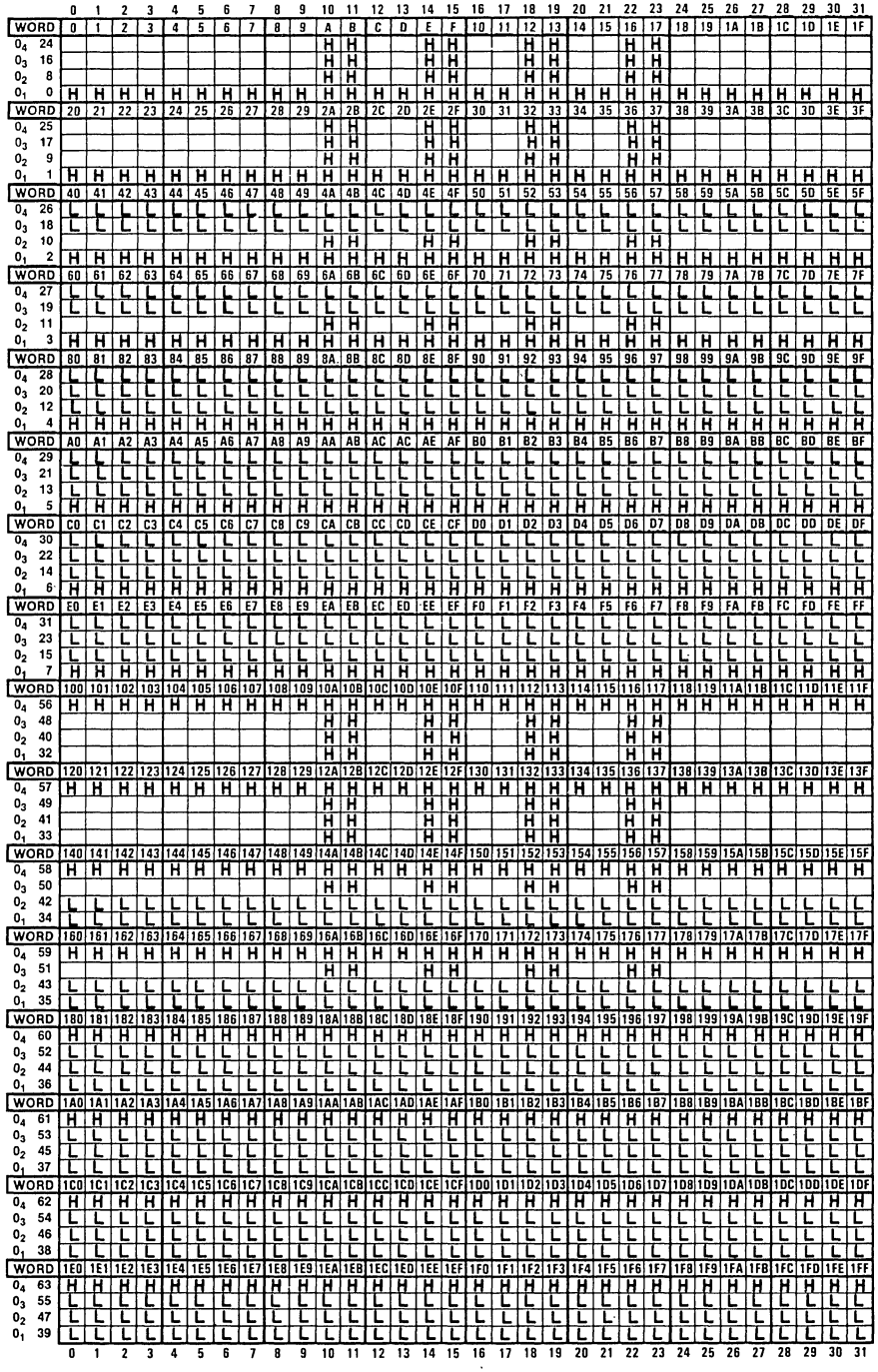


FIGURE 3-35. Programming Format Sheet, PAL12H6.

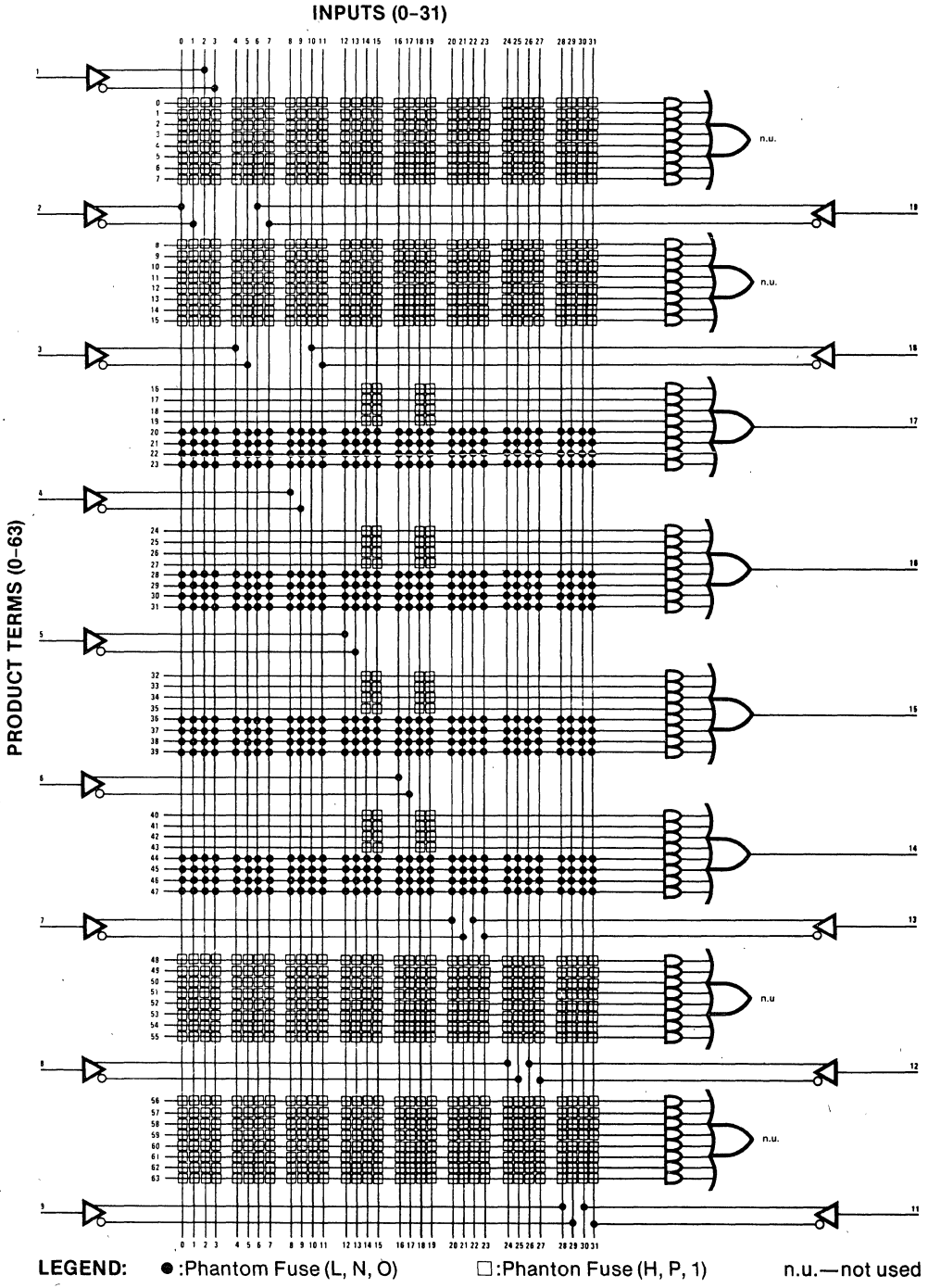


FIGURE 3-36. Logic Diagram, PAL14H4.

Programming Format PAL14H4

PATTERN: _____ NAME: _____

DATE: _____ PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24															H	H			H	H												
O_3 16															H	H			H	H												
O_2 8	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25															H	H			H	H												
O_3 17															H	H			H	H												
O_2 9	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26															H	H			H	H												
O_3 18															H	H			H	H												
O_2 10	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 2	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27															H	H			H	H												
O_3 19															H	H			H	H												
O_2 11	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 3	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 12	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 4	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 13	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 5	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 14	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 6	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_2 15	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_1 7	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 48	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 40															H	H			H	H												
O_1 32															H	H			H	H												
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 49	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 41															H	H			H	H												
O_1 33															H	H			H	H												
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 50	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 42															H	H			H	H												
O_1 34															H	H			H	H												
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 51	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 43															H	H			H	H												
O_1 35															H	H			H	H												
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 52	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 53	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 54	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_3 55	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
O_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
O_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-37. Programming Format Sheet, PAL14H4.

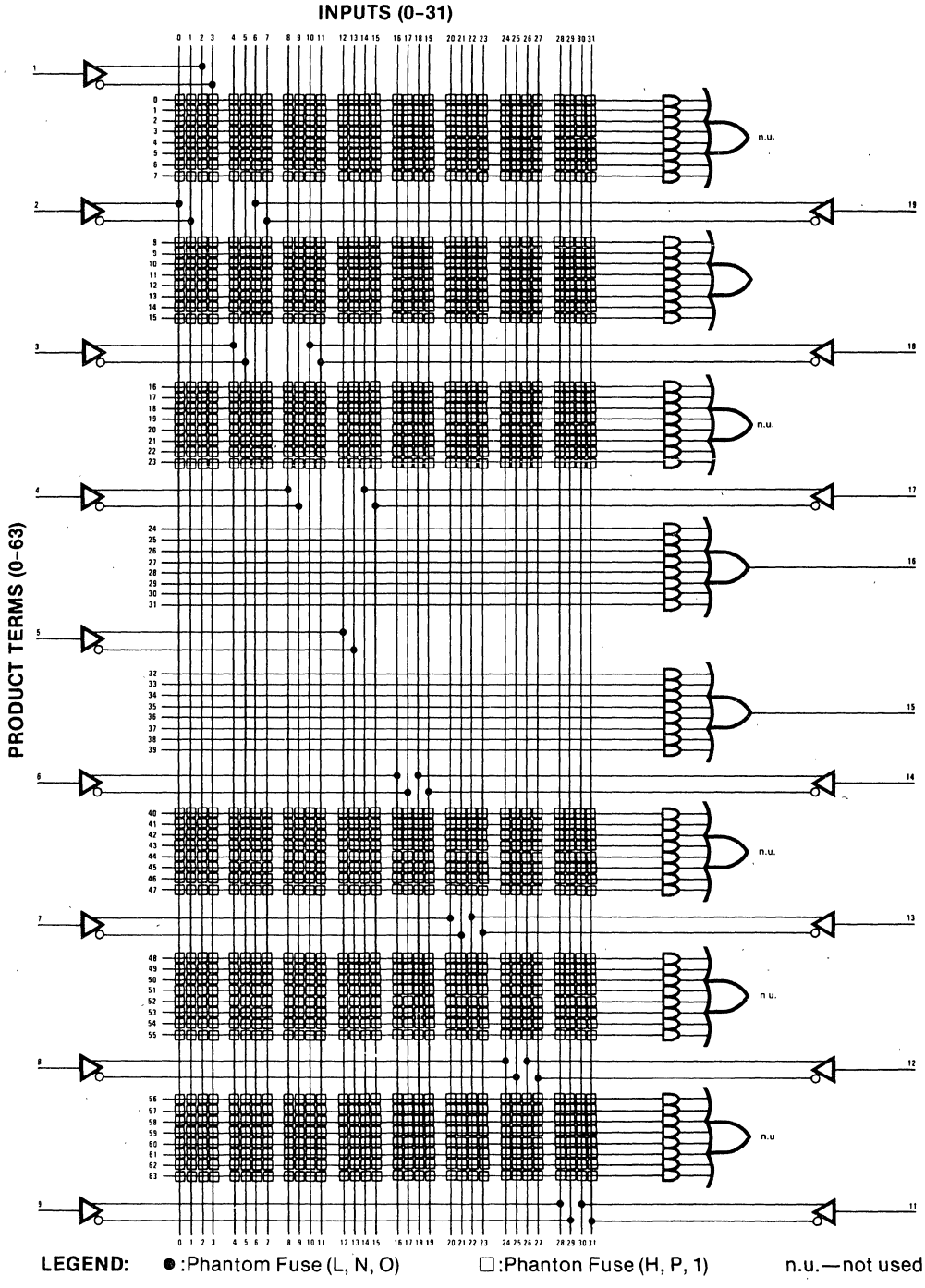


FIGURE 3-38. Logic Diagram, PAL16H2.

Programming Format PAL16H2

PATTERN: _____ NAME: _____

DATE: _____

INPUTS (0–31)

PRODUCT TERMS (0–63)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0_4 24																																
0_3 16	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 8	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
0_4 25																																
0_3 17	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 9	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
0_4 26																																
0_3 18	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 10	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 2	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
0_4 27																																
0_3 19	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 11	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 3	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
0_4 28																																
0_3 20	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 12	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 4	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
0_4 29																																
0_3 21	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 13	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 5	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
0_4 30																																
0_3 22	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 14	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 6	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0_4 31																																
0_3 23	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 15	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 7	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
0_4 56	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 48	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 40	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
0_4 57	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 49	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 41	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
0_4 58	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 50	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 42	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
0_4 59	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 51	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 43	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
0_4 60	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 52	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 44	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1A0	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
0_4 61	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 53	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 45	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
0_4 62	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 54	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 46	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
0_4 63	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 55	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_2 47	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-39. Programming Format Sheet, PAL16H2.

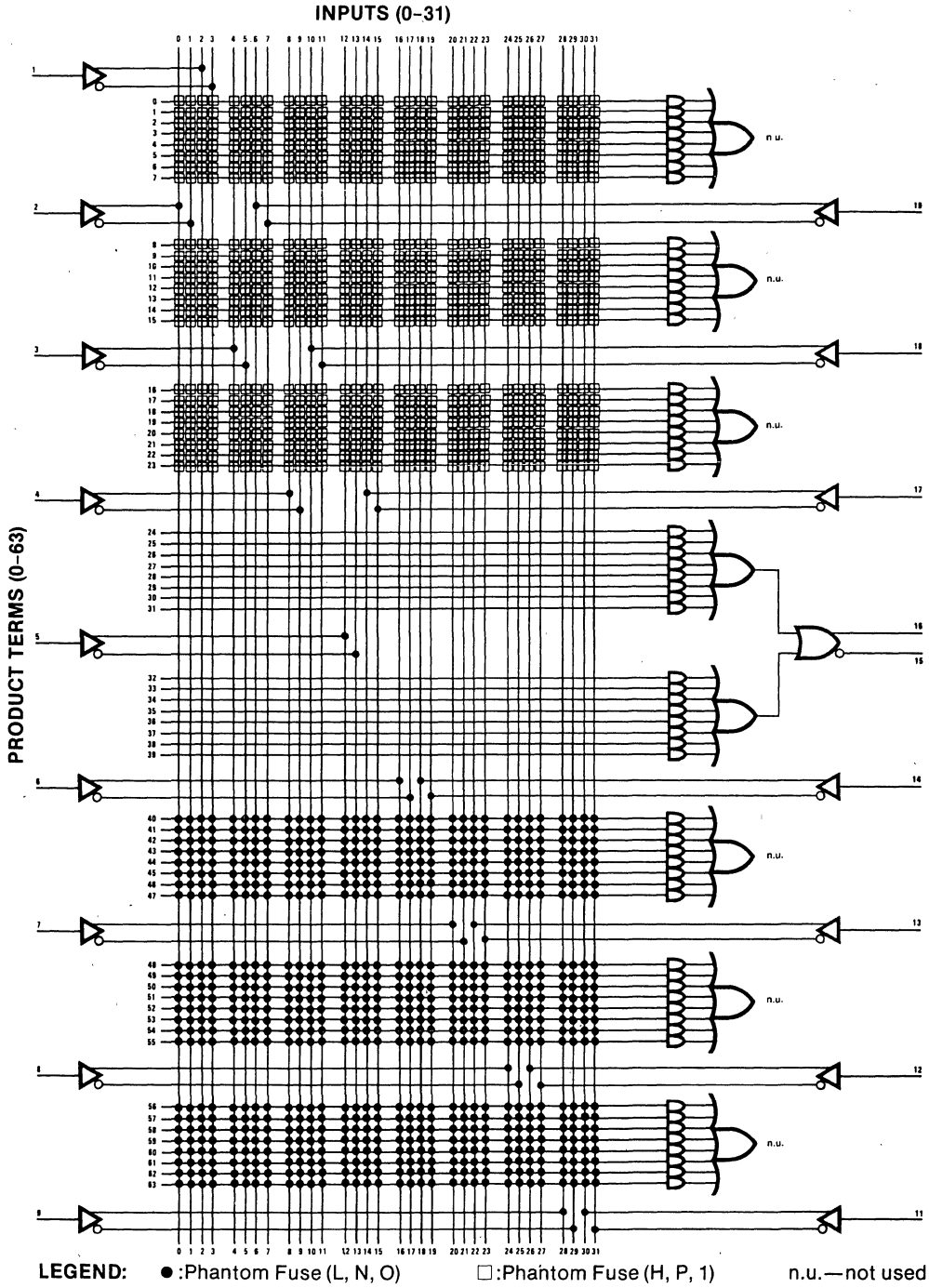


FIGURE 3-40. Logic Diagram, PAL16C1.

Programming Format PAL16C1

PATTERN: _____ NAME: _____

DATE: _____

PRODUCT TERMS (0–63)

INPUTS (0–31)

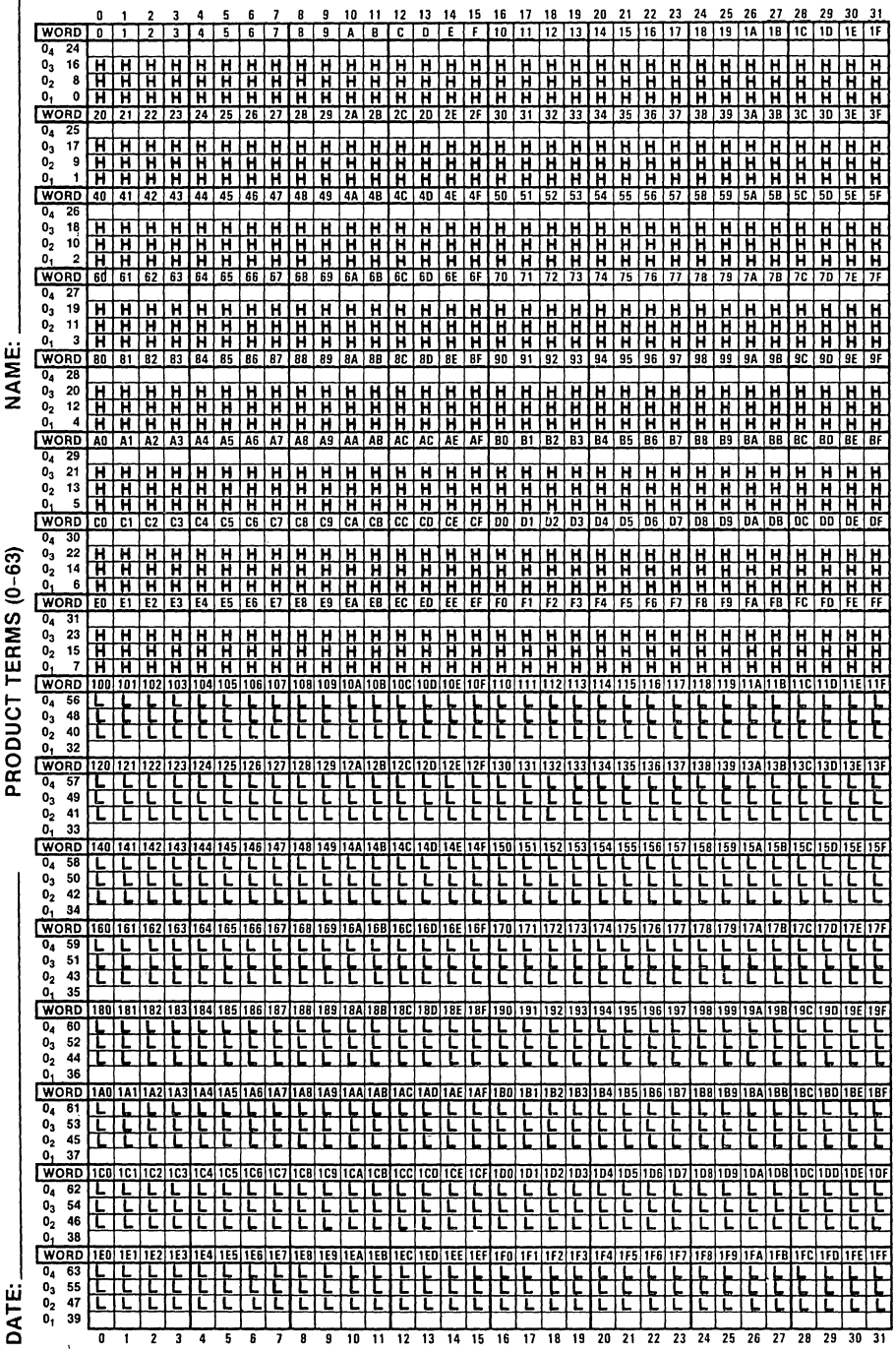


FIGURE 3-41. Programming Format Sheet, PAL16C1.

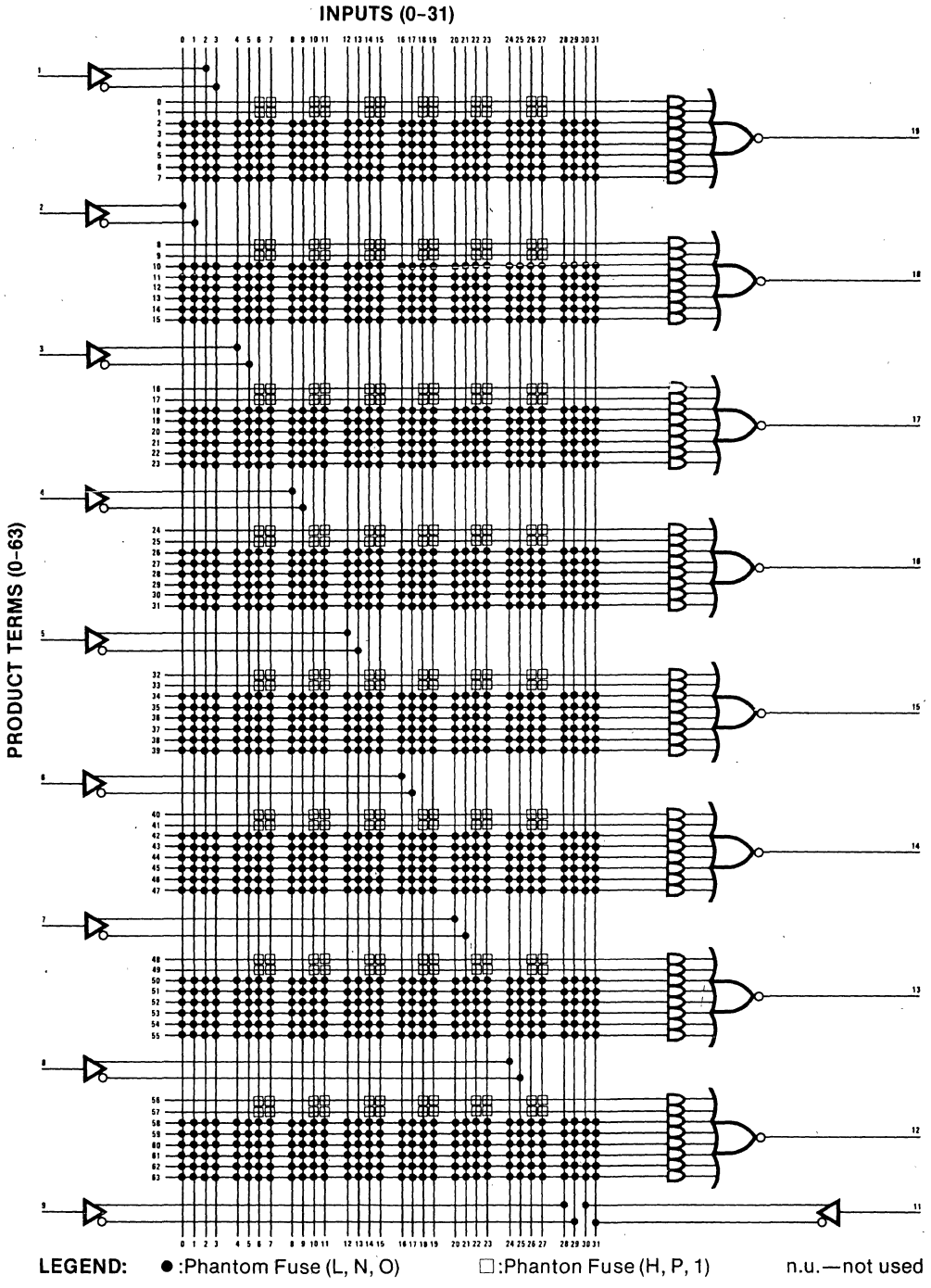


FIGURE 3-42. Logic Diagram, PAL10L8.

Programming Format **PAL10L8**

PATTERN: _____ NAME: _____

DATE: _____

PRODUCT TERMS (0–63)

INPUTS (0–31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0_4 24							H	H			H	H			H	H			H	H			H	H			H	H				
0_3 16							H	H			H	H			H	H			H	H			H	H			H	H				
0_2 8							H	H			H	H			H	H			H	H			H	H			H	H				
0_1 0							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
0_4 25							H	H			H	H			H	H			H	H			H	H			H	H				
0_3 17							H	H			H	H			H	H			H	H			H	H			H	H				
0_2 9							H	H			H	H			H	H			H	H			H	H			H	H				
0_1 1							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
0_4 26	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 18	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 10	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
0_4 27	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 19	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 11	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 3	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
0_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
0_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
0_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 6	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 7	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
0_4 56							H	H			H	H			H	H			H	H			H	H			H	H				
0_3 48							H	H			H	H			H	H			H	H			H	H			H	H				
0_2 40							H	H			H	H			H	H			H	H			H	H			H	H				
0_1 32							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
0_4 57							H	H			H	H			H	H			H	H			H	H			H	H				
0_3 49							H	H			H	H			H	H			H	H			H	H			H	H				
0_2 41							H	H			H	H			H	H			H	H			H	H			H	H				
0_1 33							H	H			H	H			H	H			H	H			H	H			H	H				
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
0_4 58	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 50	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 42	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 34	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
0_4 59	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 51	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 43	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 35	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
0_4 60	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
0_4 61	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
0_4 62	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
0_4 63	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-43. Programming Format Sheet, PAL10L8.

Logic Diagram PAL12L6

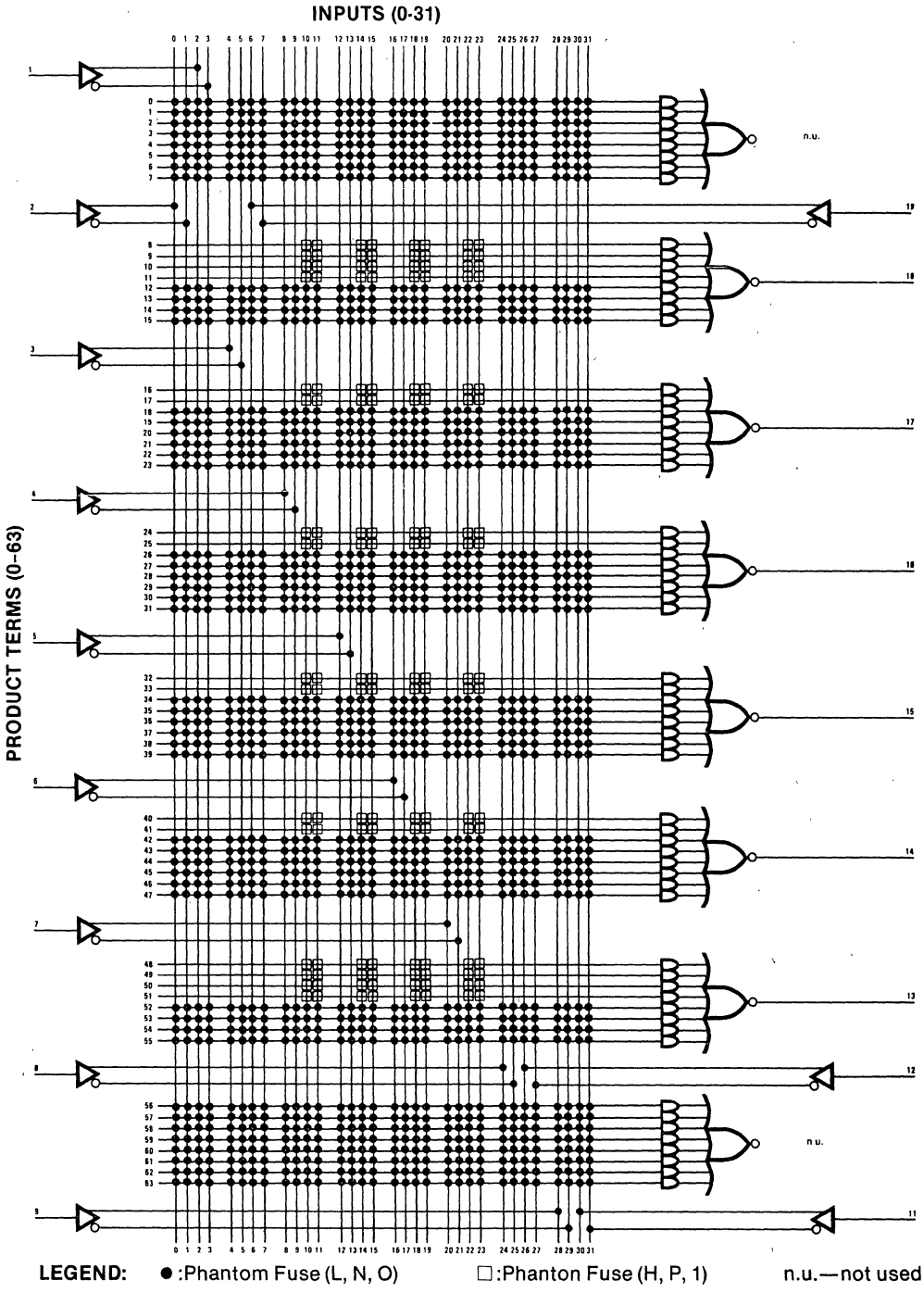


FIGURE 3-44. Logic Diagram, PAL12L6.

Programming Format PAL12L6

PATTERN: _____ NAME: _____

DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

WORD	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0_4 24											H	H			H	H			H	H			H	H								
0_3 16											H	H			H	H			H	H			H	H								
0_2 8											H	H			H	H			H	H			H	H								
0_1 0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
0_4 25											H	H			H	H			H	H			H	H								
0_3 17											H	H			H	H			H	H			H	H								
0_2 9											H	H			H	H			H	H			H	H								
0_1 1	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
0_4 26	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 18	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 10											H	H			H	H			H	H			H	H								
0_1 2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
0_4 27	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 19	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 11											H	H			H	H			H	H			H	H								
0_1 3	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
0_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
0_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
0_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 6	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 7	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	100	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
0_4 56	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 48											H	H			H	H			H	H			H	H								
0_2 40											H	H			H	H			H	H			H	H								
0_1 32											H	H			H	H			H	H			H	H								
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
0_4 57	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 49											H	H			H	H			H	H			H	H								
0_2 41											H	H			H	H			H	H			H	H								
0_1 33											H	H			H	H			H	H			H	H								
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
0_4 58	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 50											H	H			H	H			H	H			H	H								
0_2 42	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 34	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
0_4 59	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 51											H	H			H	H			H	H			H	H								
0_2 43	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 35	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
0_4 60	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
0_4 61	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	100	101	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
0_4 62	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
0_4 63	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-45. Programming Format Sheet, PAL12L6.

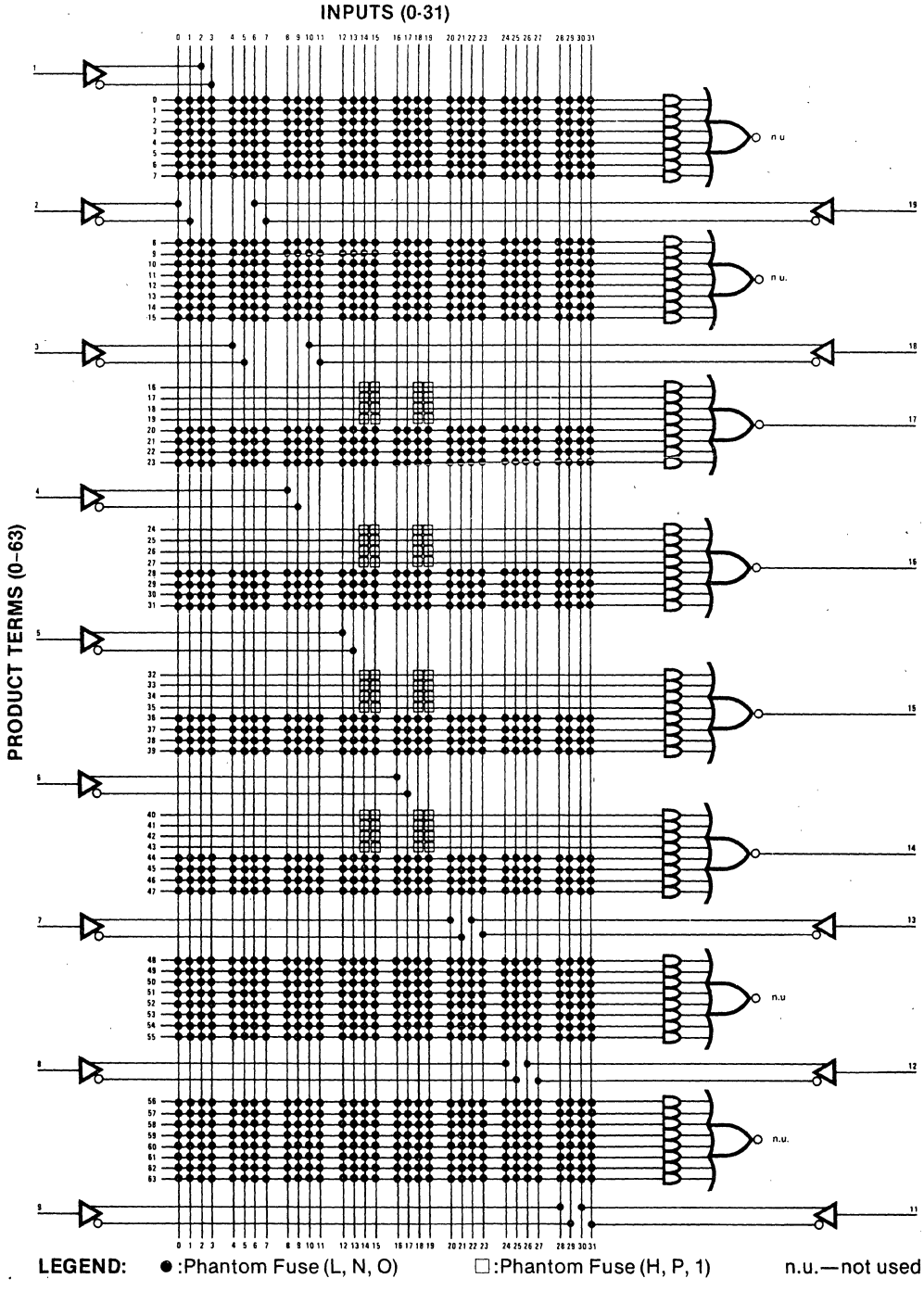


FIGURE 3-46. Logic Diagram, PAL14L4.

Programming Format PAL14L4

NAME: _____ PATTERN: _____ DATE: _____

PRODUCT TERMS (0–63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0_4 24															H	H			H	H												
0_3 16															H	H			H	H												
0_2 8	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 0	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
0_4 25															H	H			H	H												
0_3 17															H	H			H	H												
0_2 9	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 1	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
0_4 26															H	H			H	H												
0_3 18															H	H			H	H												
0_2 10	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 2	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
0_4 27															H	H			H	H												
0_3 19															H	H			H	H												
0_2 11	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 3	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
0_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 4	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
0_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 5	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
0_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 6	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 7	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
0_4 56	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 48	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 40															H	H			H	H												
0_1 32															H	H			H	H												
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
0_4 57	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 49	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 41															H	H			H	H												
0_1 33															H	H			H	H												
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
0_4 58	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 50	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 42															H	H			H	H												
0_1 34															H	H			H	H												
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
0_4 59	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 51	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 43															H	H			H	H												
0_1 35															H	H			H	H												
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
0_4 60	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
0_4 61	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
0_4 62	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
0_4 63	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-47. Programming Format Sheet, PAL14L4.

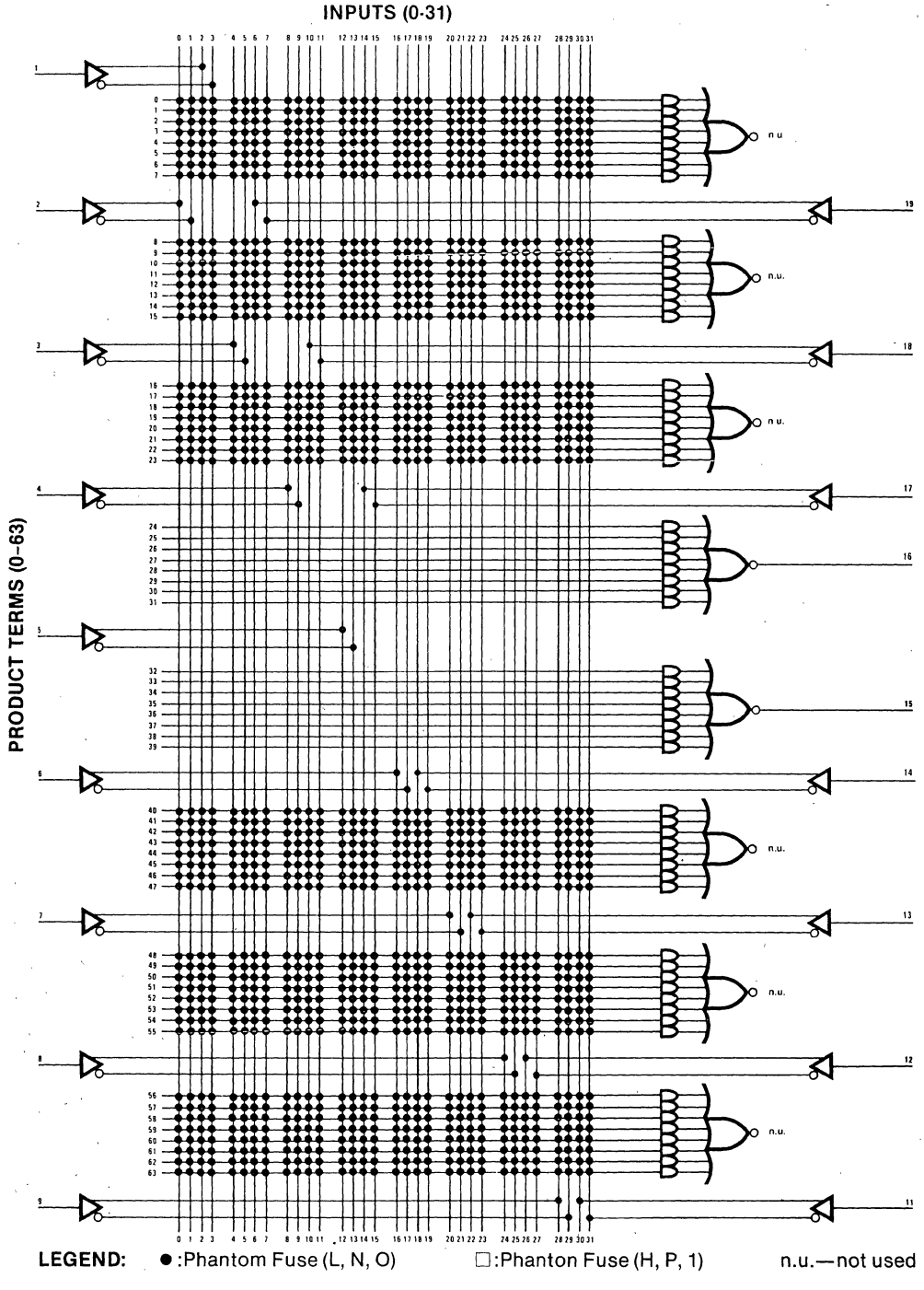


FIGURE 3-48. Logic Diagram, PAL16L2.

Programming Format

PAL16L2

PATTERN: _____

NAME: _____

DATE: _____

INPUTS (0-31)

PRODUCT TERMS (0-63)

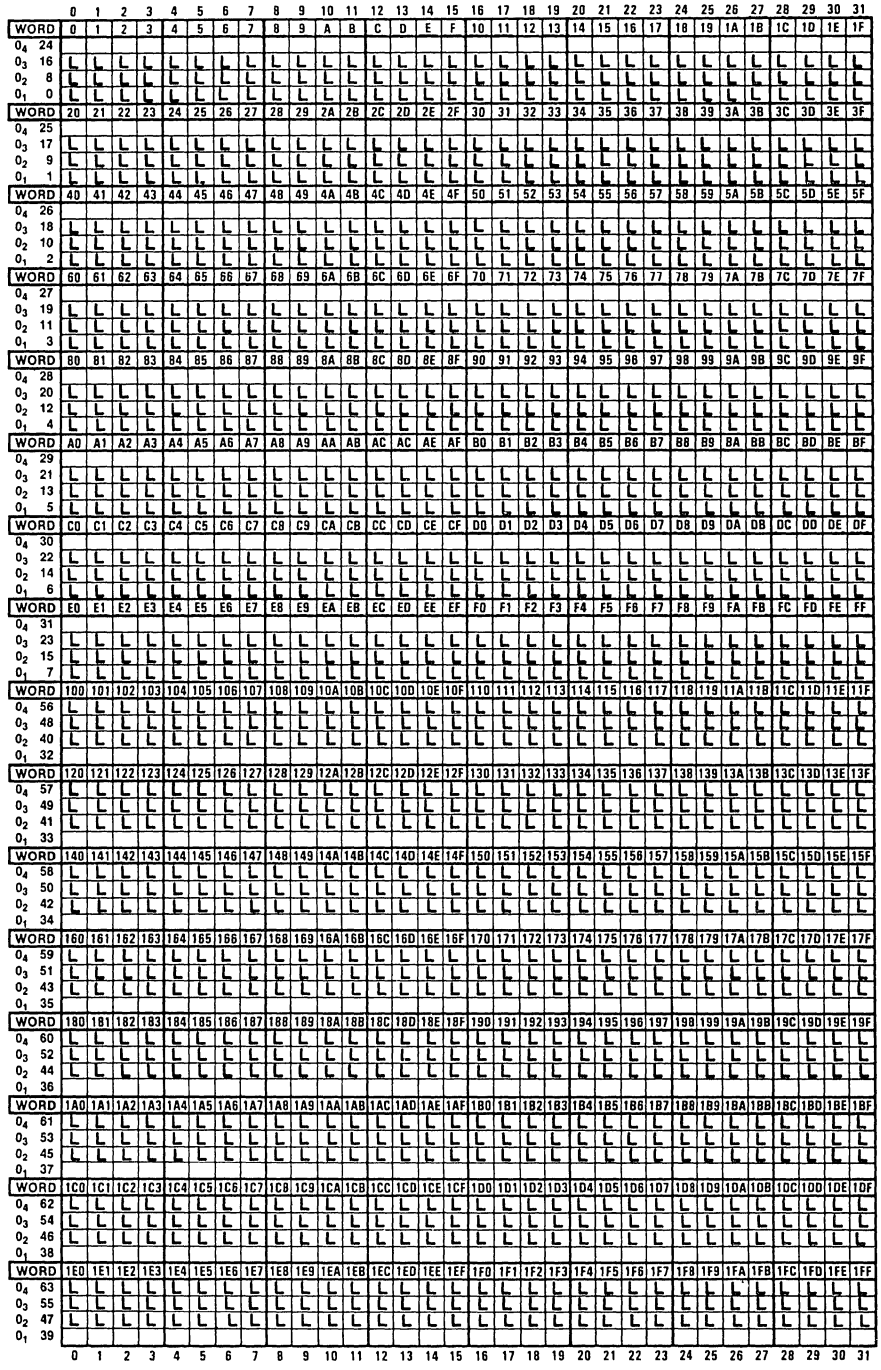


FIGURE 3-49. Programming Format Sheet, PAL16L2.

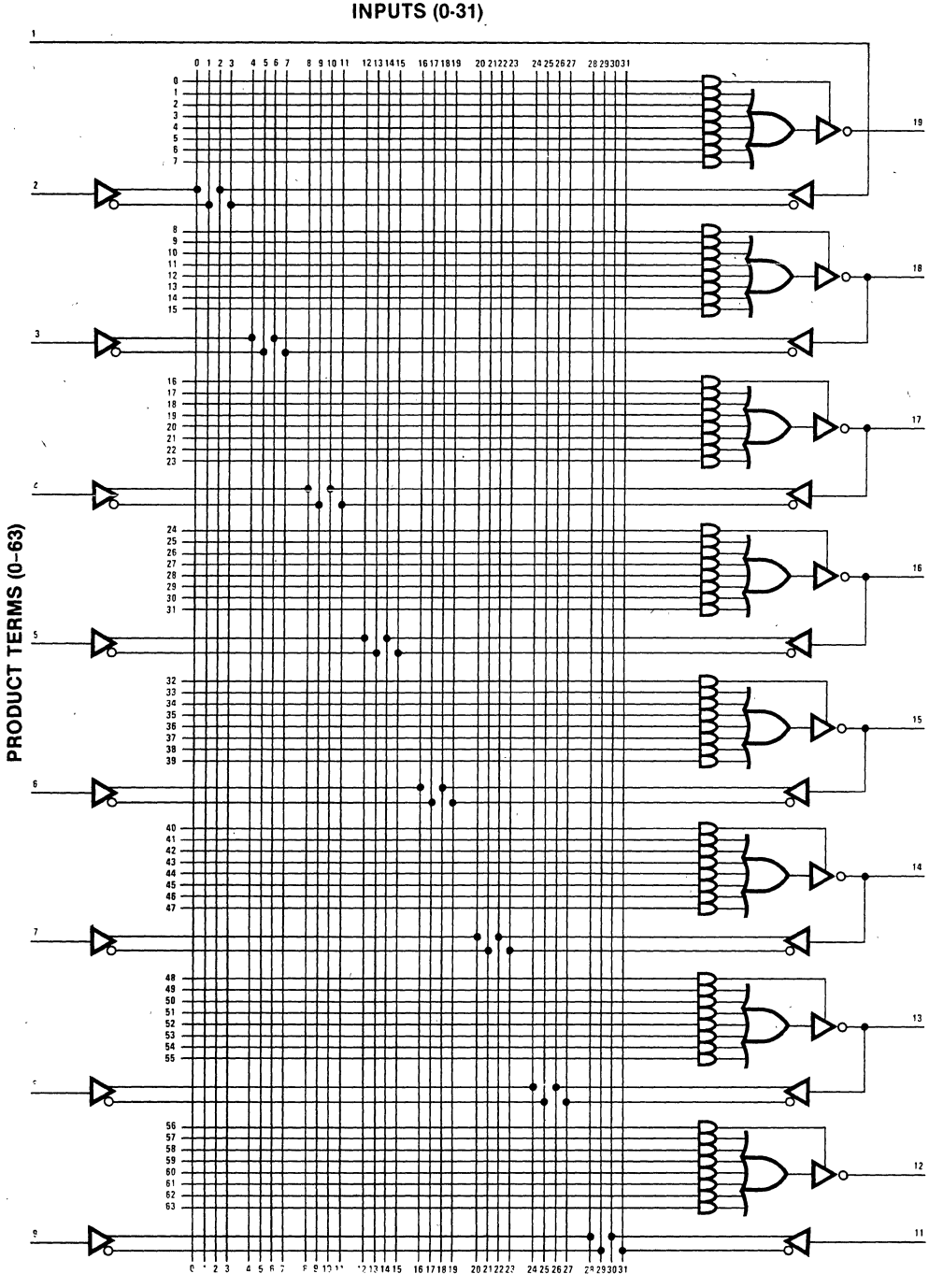


FIGURE 3-50. Logic Diagram, PAL16L8.

Programming Format PAL16L8

PATTERN: _____ NAME: _____ DATE: _____

INPUTS (0-31)

PRODUCT TERMS (0–63)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0_4 24																																
0_3 16																																
0_2 8																																
0_1 0																																
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
0_4 25																																
0_3 17																																
0_2 9																																
0_1 1																																
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
0_4 26																																
0_3 18																																
0_2 10																																
0_1 2																																
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
0_4 27																																
0_3 19																																
0_2 11																																
0_1 3																																
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
0_4 28																																
0_3 20																																
0_2 12																																
0_1 4																																
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
0_4 29																																
0_3 21																																
0_2 13																																
0_1 5																																
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
0_4 30																																
0_3 22																																
0_2 14																																
0_1 6																																
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0_4 31																																
0_3 23																																
0_2 15																																
0_1 7																																
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
0_4 56																																
0_3 48																																
0_2 40																																
0_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
0_4 57																																
0_3 49																																
0_2 41																																
0_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
0_4 58																																
0_3 50																																
0_2 42																																
0_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
0_4 59																																
0_3 51																																
0_2 43																																
0_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
0_4 60																																
0_3 52																																
0_2 44																																
0_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
0_4 61																																
0_3 53																																
0_2 45																																
0_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
0_4 62																																
0_3 54																																
0_2 46																																
0_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
0_4 63																																
0_3 55																																
0_2 47																																
0_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-51. Programming Format Sheet, PAL16L8.

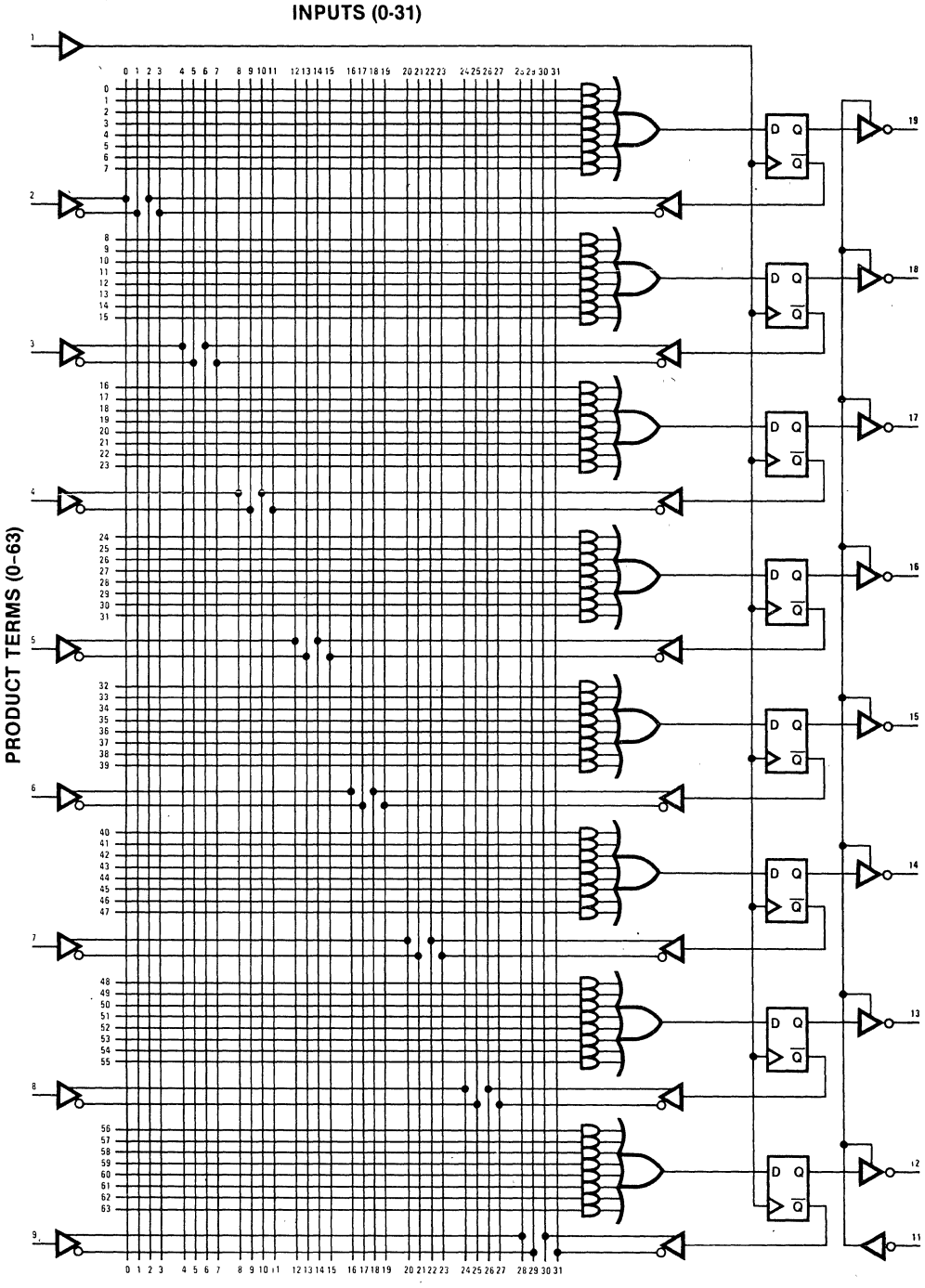


FIGURE 3-52. Logic Diagram, PAL16R8.

Programming Format PAL16R8

PATTERN: _____ NAME: _____ DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0_4 24																																
0_3 16																																
0_2 8																																
0_1 0																																
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
0_4 25																																
0_3 17																																
0_2 9																																
0_1 1																																
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
0_4 26																																
0_3 18																																
0_2 10																																
0_1 2																																
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
0_4 27																																
0_3 19																																
0_2 11																																
0_1 3																																
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
0_4 28																																
0_3 20																																
0_2 12																																
0_1 4																																
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
0_4 29																																
0_3 21																																
0_2 13																																
0_1 5																																
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
0_4 30																																
0_3 22																																
0_2 14																																
0_1 6																																
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0_4 31																																
0_3 23																																
0_2 15																																
0_1 7																																
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
0_4 56																																
0_3 48																																
0_2 40																																
0_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
0_4 57																																
0_3 49																																
0_2 41																																
0_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
0_4 58																																
0_3 50																																
0_2 42																																
0_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
0_4 59																																
0_3 51																																
0_2 43																																
0_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
0_4 60																																
0_3 52																																
0_2 44																																
0_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
0_4 61																																
0_3 53																																
0_2 45																																
0_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
0_4 62																																
0_3 54																																
0_2 46																																
0_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
0_4 63																																
0_3 55																																
0_2 47																																
0_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-53. Programming Format Sheet, PAL16R8.

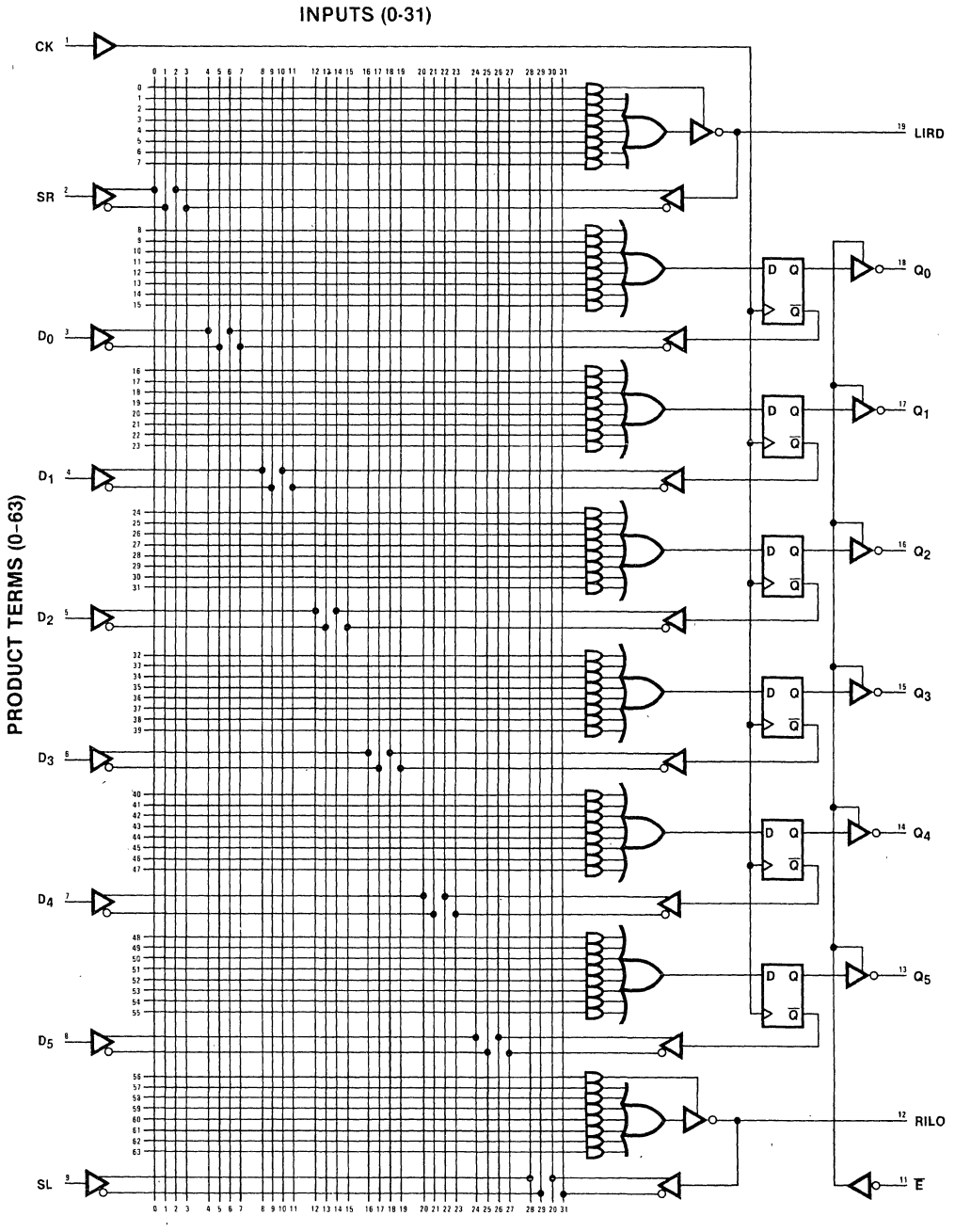


FIGURE 3-54. Logic Diagram, PAL16R6.

Programming Format PAL16R6

PATTERN: _____

NAME: _____

DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0_4 24																																
0_3 16																																
0_2 8																																
0_1 0																																
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
0_4 25																																
0_3 17																																
0_2 9																																
0_1 1																																
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
0_4 26																																
0_3 18																																
0_2 10																																
0_1 2																																
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
0_4 27																																
0_3 19																																
0_2 11																																
0_1 3																																
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
0_4 28																																
0_3 20																																
0_2 12																																
0_1 4																																
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
0_4 29																																
0_3 21																																
0_2 13																																
0_1 5																																
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
0_4 30																																
0_3 22																																
0_2 14																																
0_1 6																																
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0_4 31																																
0_3 23																																
0_2 15																																
0_1 7																																
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
0_4 56																																
0_3 48																																
0_2 40																																
0_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
0_4 57																																
0_3 49																																
0_2 41																																
0_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
0_4 58																																
0_3 50																																
0_2 42																																
0_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
0_4 59																																
0_3 51																																
0_2 43																																
0_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
0_4 60																																
0_3 52																																
0_2 44																																
0_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
0_4 61																																
0_3 53																																
0_2 45																																
0_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
0_4 62																																
0_3 54																																
0_2 46																																
0_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
0_4 63																																
0_3 55																																
0_2 47																																
0_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-55. Programming Format Sheet, PAL16R6.

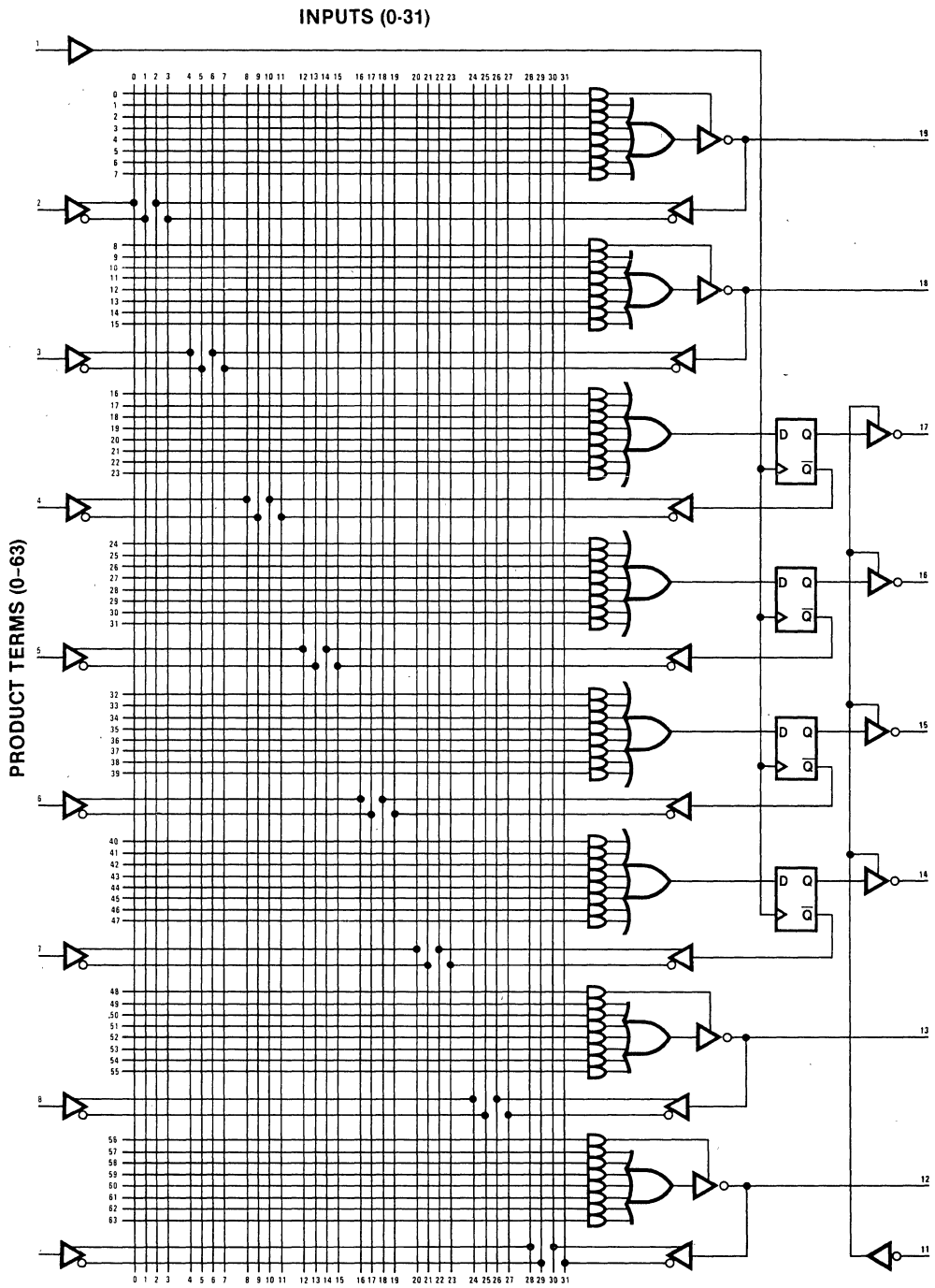


FIGURE 3-56. Logic Diagram, PAL16R4.

Programming Format PAL16R4

PATTERN: _____

NAME: _____

DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
O_4 24																																
O_3 16																																
O_2 8																																
O_1 0																																
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
O_4 25																																
O_3 17																																
O_2 9																																
O_1 1																																
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
O_4 26																																
O_3 18																																
O_2 10																																
O_1 2																																
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
O_4 27																																
O_3 19																																
O_2 11																																
O_1 3																																
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
O_4 28																																
O_3 20																																
O_2 12																																
O_1 4																																
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
O_4 29																																
O_3 21																																
O_2 13																																
O_1 5																																
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
O_4 30																																
O_3 22																																
O_2 14																																
O_1 6																																
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
O_4 31																																
O_3 23																																
O_2 15																																
O_1 7																																
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
O_4 56																																
O_3 48																																
O_2 40																																
O_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
O_4 57																																
O_3 49																																
O_2 41																																
O_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
O_4 58																																
O_3 50																																
O_2 42																																
O_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
O_4 59																																
O_3 51																																
O_2 43																																
O_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
O_4 60																																
O_3 52																																
O_2 44																																
O_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
O_4 61																																
O_3 53																																
O_2 45																																
O_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
O_4 62																																
O_3 54																																
O_2 46																																
O_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
O_4 63																																
O_3 55																																
O_2 47																																
O_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-57. Programming Format Sheet, PAL16R4.

Logic Diagram PAL16X4

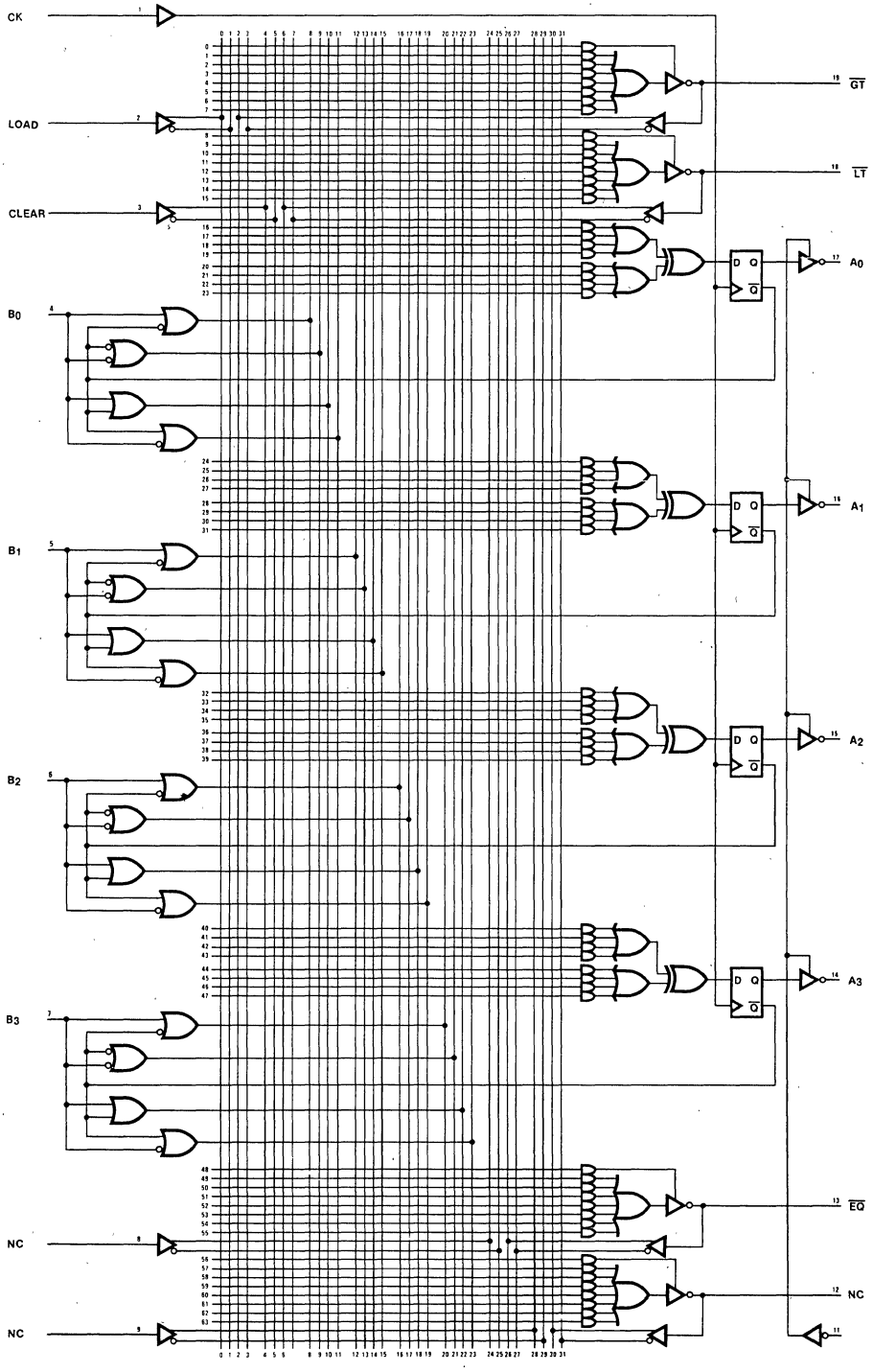


FIGURE 3-58. Logic Diagram, PAL16X4.

Programming Format PAL16R4

PATTERN: _____

NAME: _____

DATE: _____

PRODUCT TERMS (0-63)

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0_4 24																																
0_3 16																																
0_2 8																																
0_1 0																																
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
0_4 25																																
0_3 17																																
0_2 9																																
0_1 1																																
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
0_4 26																																
0_3 18																																
0_2 10																																
0_1 2																																
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
0_4 27																																
0_3 19																																
0_2 11																																
0_1 3																																
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
0_4 28																																
0_3 20																																
0_2 12																																
0_1 4																																
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
0_4 29																																
0_3 21																																
0_2 13																																
0_1 5																																
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
0_4 30																																
0_3 22																																
0_2 14																																
0_1 6																																
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0_4 31																																
0_3 23																																
0_2 15																																
0_1 7																																
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
0_4 56																																
0_3 48																																
0_2 40																																
0_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
0_4 57																																
0_3 49																																
0_2 41																																
0_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
0_4 58																																
0_3 50																																
0_2 42																																
0_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
0_4 59																																
0_3 51																																
0_2 43																																
0_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
0_4 60																																
0_3 52																																
0_2 44																																
0_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
0_4 61																																
0_3 53																																
0_2 45																																
0_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
0_4 62																																
0_3 54																																
0_2 46																																
0_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
0_4 63																																
0_3 55																																
0_2 47																																
0_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-59. Programming Format Sheet, PAL16X4.

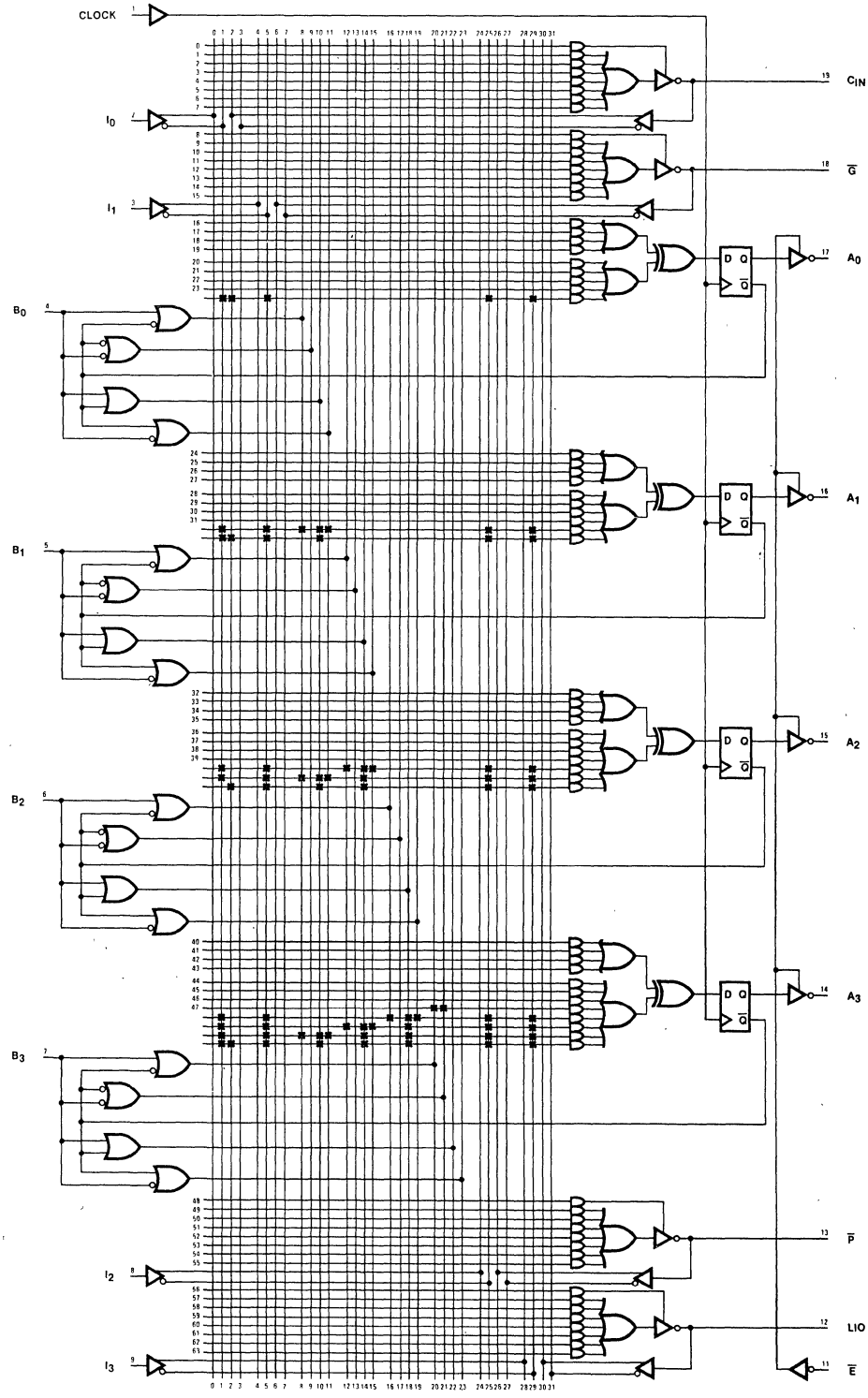


FIGURE 3-60. Logic Diagram, PAL16A4.

Programming Format PAL16R4

PATTERN: _____ NAME: _____

PRODUCT TERMS (0-63)

DATE: _____

INPUTS (0-31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0_4 24																																
0_3 16																																
0_2 8																																
0_1 0																																
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
0_4 25																																
0_3 17																																
0_2 9																																
0_1 1																																
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
0_4 26																																
0_3 18																																
0_2 10																																
0_1 2																																
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
0_4 27																																
0_3 19																																
0_2 11																																
0_1 3																																
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
0_4 28																																
0_3 20																																
0_2 12																																
0_1 4																																
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
0_4 29																																
0_3 21																																
0_2 13																																
0_1 5																																
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
0_4 30																																
0_3 22																																
0_2 14																																
0_1 6																																
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0_4 31																																
0_3 23																																
0_2 15																																
0_1 7																																
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
0_4 56																																
0_3 48																																
0_2 40																																
0_1 32																																
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
0_4 57																																
0_3 49																																
0_2 41																																
0_1 33																																
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
0_4 58																																
0_3 50																																
0_2 42																																
0_1 34																																
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
0_4 59																																
0_3 51																																
0_2 43																																
0_1 35																																
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
0_4 60																																
0_3 52																																
0_2 44																																
0_1 36																																
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
0_4 61																																
0_3 53																																
0_2 45																																
0_1 37																																
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
0_4 62																																
0_3 54																																
0_2 46																																
0_1 38																																
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
0_4 63																																
0_3 55																																
0_2 47																																
0_1 39																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

FIGURE 3-61. Programming Format Sheet, PAL16A4.

National Semiconductor

Application Suggestions

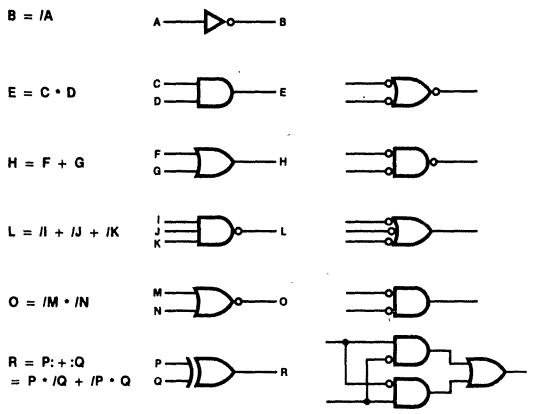
Using PALs, you may not only replace conventional logic in existing products but also optimize the design of new products. The other chapters of the book discuss the PAL concept and provide information on the advantages gained and the techniques used when designing with PALs. This section shows practical applications that range from simple logic gate replacements to complex control sequencers.

Each example is presented as a complete PAL design, carried through step by step, from the selection of the best PAL to solve the problem to the writing of the logic equations in PALASM notation. In most cases, manual coding is shown as well. This makes the examples complete enough for you to incorporate into your own system designs.

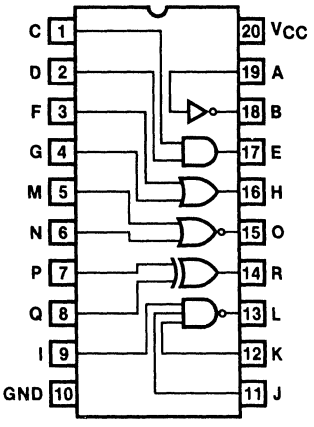
The uses to which PALS can be put are virtually limitless. Let your imagination run wild!

Here is a list of the design ideas you'll find in the ensuing pages:

EXAMPLE 1: BASIC GATES

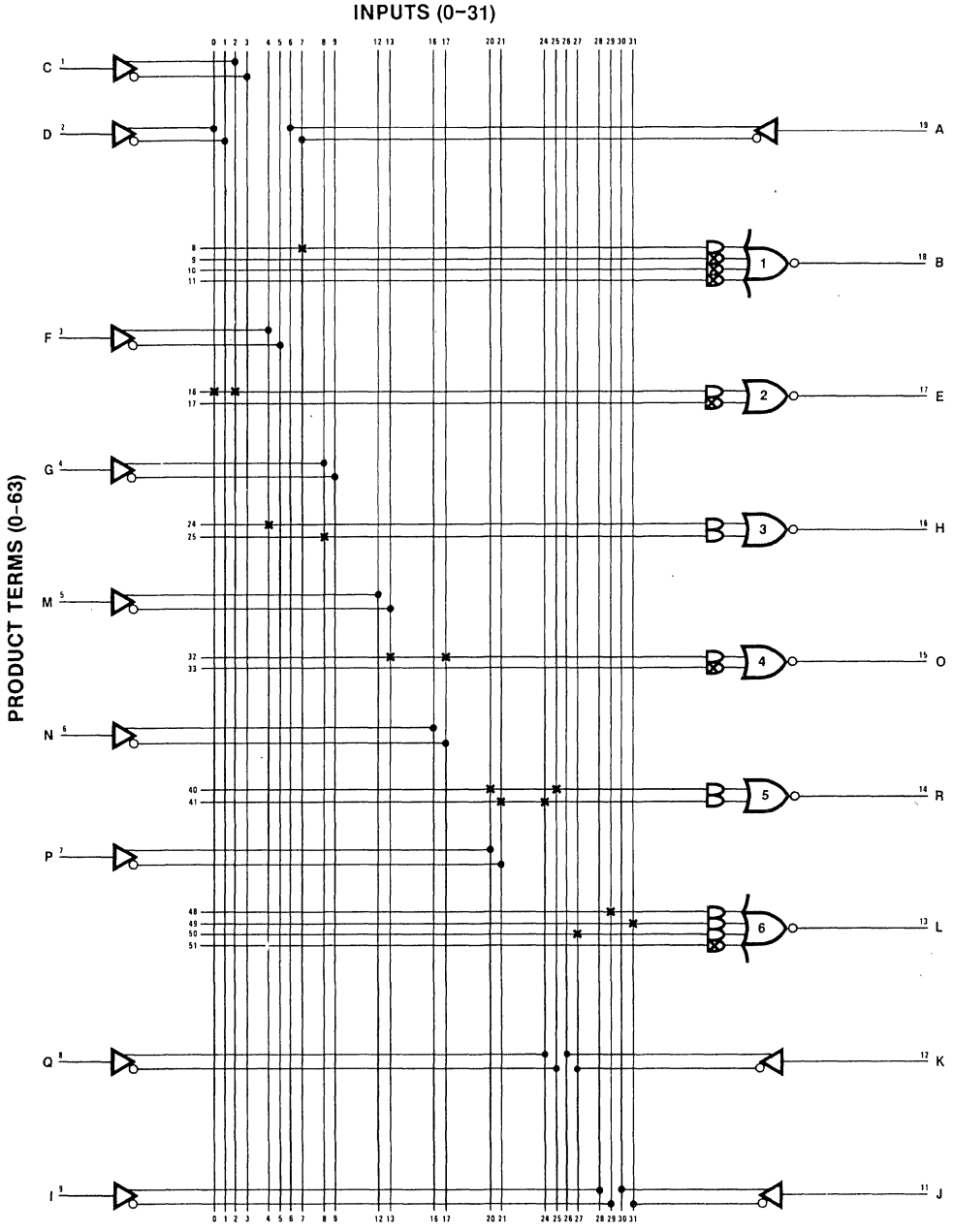


PAL 12H6



This example demonstrates how fusable logic can implement the basic inverter, AND, OR, NAND, NOR, and exclusive-OR functions. Note the one to one correspondence between conventional logic symbology and PAL logic symbology. The PAL12H6 is selected because it has 12 inputs and 6 outputs. For this this example, the fuse pattern is generated using

a) PALASM
b) Manual Programming Format (BHLF) Manual Coding


INPUTS (0–31)
PRODUCT TERMS (0–63)
0 1 2 3 4 5 6 7 8 9 12 13 16 17 20 21 24 25 26 27 28 29 30 31
C 1
D 2
F 3
G 4
M 5
N 6
P 7
Q 8
I 9
8 9 10 11
16 17
24 25
32 33
40 41
48 49 50 51
1
2
3
4
5
6
19 A
18 B
17 E
16 H
15 O
14 R
13 L
12 K
11 J

Manual Coding Basic Gates

Programming Format **PAL12H6**

PATTERN: _____ NAME: _____

DATE: _____

PRODUCT TERMS (0–63)

INPUTS (0–31)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
WORD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
0_4 24	X	X	X	X	L	X	X	X	X	X	H	H	X	X	H	H	X	X	H	H	X	X	H	H	X	X	X	X	X	X	X	X
0_3 16	L	X	L	X	X	X	X	L	X	X	H	H	X	X	H	H	X	X	H	H	X	X	H	H	X	X	X	X	X	X	X	X
0_2 8	X	X	X	X	X	X	X	L	X	X	H	H	X	X	H	H	X	X	H	H	X	X	H	H	X	X	X	X	X	X	X	X
0_1 0	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
0_4 25	X	X	X	X	X	X	X	X	L	X	H	H	X	X	H	H	X	X	H	H	X	X	H	H	X	X	X	X	X	X	X	X
0_3 17	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L
0_2 9	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L
0_1 1	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F
0_4 26	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 18	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 10	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L
0_1 2	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	60	61	62	63	64	65	66	67	68	69	6A	6B	6C	6D	6E	6F	70	71	72	73	74	75	76	77	78	79	7A	7B	7C	7D	7E	7F
0_4 27	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 19	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 11	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L
0_1 3	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
0_4 28	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 20	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 12	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 4	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	AA	AB	AC	AC	AE	AF	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	BA	BB	BC	BD	BE	BF
0_4 29	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 21	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 13	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 5	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF
0_4 30	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 22	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 14	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 6	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	EA	EB	EC	ED	EE	EF	F0	F1	F2	F3	F4	F5	F6	F7	F8	F9	FA	FB	FC	FD	FE	FF
0_4 31	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_3 23	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 15	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 7	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
WORD	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	111	112	113	114	115	116	117	118	119	11A	11B	11C	11D	11E	11F
0_4 56	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 48	X	X	X	X	X	X	X	X	X	X	H	H	X	X	H	H	X	X	H	H	X	X	H	H	X	X	X	L	X	X	X	X
0_2 40	X	X	X	X	X	X	X	X	X	X	H	H	X	X	H	H	X	X	H	H	L	X	H	H	X	L	X	X	X	X	X	X
0_1 32	X	X	X	X	X	X	X	X	X	X	H	H	X	L	H	H	X	L	H	H	X	X	H	H	X	X	X	X	X	X	X	X
WORD	120	121	122	123	124	125	126	127	128	129	12A	12B	12C	12D	12E	12F	130	131	132	133	134	135	136	137	138	139	13A	13B	13C	13D	13E	13F
0_4 57	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 49	X	X	X	X	X	X	X	X	X	X	H	H	X	X	H	H	X	X	H	H	X	X	H	H	X	X	X	X	X	X	L	X
0_2 41	X	X	X	X	X	X	X	L	X	X	H	H	X	X	H	H	X	X	H	H	X	L	H	H	L	X	X	X	X	L	X	X
0_1 33	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L
WORD	140	141	142	143	144	145	146	147	148	149	14A	14B	14C	14D	14E	14F	150	151	152	153	154	155	156	157	158	159	15A	15B	15C	15D	15E	15F
0_4 58	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 50	X	X	X	X	X	X	X	X	X	X	H	H	X	X	H	H	X	X	H	H	X	X	H	H	X	X	X	X	X	X	X	X
0_2 42	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 34	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	160	161	162	163	164	165	166	167	168	169	16A	16B	16C	16D	16E	16F	170	171	172	173	174	175	176	177	178	179	17A	17B	17C	17D	17E	17F
0_4 59	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 51	L	L	L	L	L	L	L	L	L	L	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L	L	L	L	L	L	L
0_2 43	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 35	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	180	181	182	183	184	185	186	187	188	189	18A	18B	18C	18D	18E	18F	190	191	192	193	194	195	196	197	198	199	19A	19B	19C	19D	19E	19F
0_4 60	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 52	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 44	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 36	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF
0_4 61	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 53	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 45	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 37	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1C0	1C1	1C2	1C3	1C4	1C5	1C6	1C7	1C8	1C9	1CA	1CB	1CC	1CD	1CE	1CF	1D0	1D1	1D2	1D3	1D4	1D5	1D6	1D7	1D8	1D9	1DA	1DB	1DC	1DD	1DE	1DF
0_4 62	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 54	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 46	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 38	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
WORD	1E0	1E1	1E2	1E3	1E4	1E5	1E6	1E7	1E8	1E9	1EA	1EB	1EC	1ED	1EE	1EF	1F0	1F1	1F2	1F3	1F4	1F5	1F6	1F7	1F8	1F9	1FA	1FB	1FC	1FD	1FE	1FF
0_4 63	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
0_3 55	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_2 47	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
0_1 39	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

```
PAL12H6                                    PAL DESIGN SPECIFICATION
P0055A
BASIC GATES EXAMPLE
S.V. CA
C D F G M N  P Q I GND J K L R O H E B A VCC

 B=/A
 E=C*D
 H=F+G
 O=/M*/N
 R=P*/Q+/P*Q
 L=/I+/J+/K

DESCRIPTION: THIS EXAMPLE ILLUSTRATES THE USE OF FUSIBLE LOGIC TO
             IMPLEMENT THE BASIC GATES.

NUMBER OF FUSES BLOWN =  306
```

PALASM Output HEX FORMAT

```
B F B F 7 F F D F F F F F F F F F F F F F F F F F F F F F F .
9 9 9 9 9 9 9 1 9 F F 9 9 F F 9 9 F F 9 9 F F 9 9 9 9 9 9 9 .
1 1 1 1 1 1 1 1 1 1 3 3 1 1 3 3 1 1 3 3 1 1 3 3 1 1 1 1 1 1 1 .
1 1 1 1 1 1 1 1 1 1 3 3 1 1 3 3 1 1 3 3 1 1 3 3 1 1 1 1 1 1 1 .
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 .
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 .
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 .
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 .
F F F F F F F F F F F F E F F F E F F D F F F F D F F F B F F .
E E E E E E E E E F F E E F F E E F F E C F F C E E E E E E A .
C C C C C C C C C C C C C C C C C C C C C C C C C C 8 C C C C .
8 8 8 8 8 8 8 8 8 8 C C 8 8 C C 8 8 C C 8 8 C C 8 8 8 8 8 8 8 .
8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 .
8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 .
8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 .
8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 8 .
```

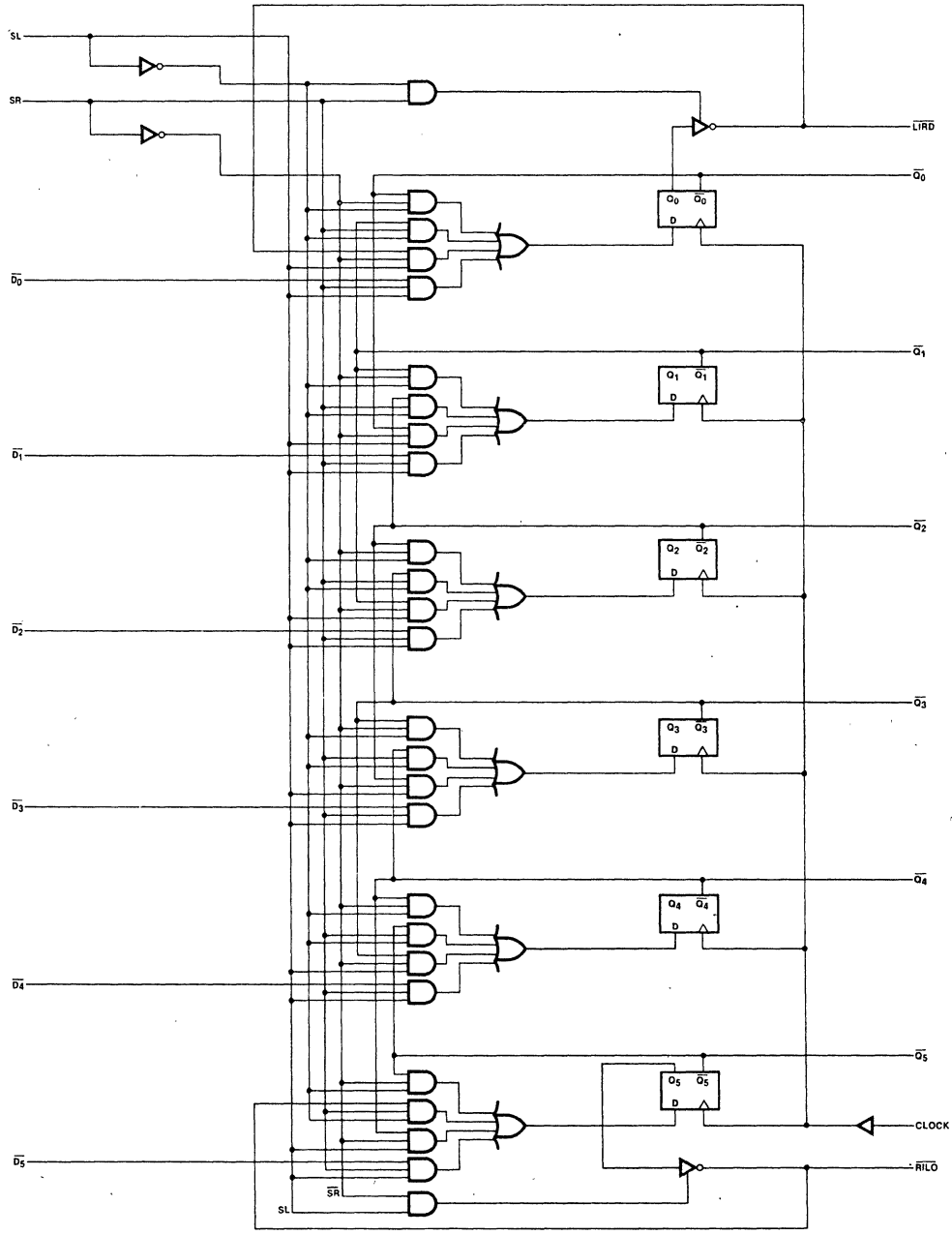
PALASM Output: Basic Gates

BHLF Format PAL12H6

```
BHLHHF BHHHHF BHLHHF BHHHHF BLHHHF BHHHHF BHHHHF BHHLHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF
BLLLHF BHLLHF BHHHHF BHHHHF BHLLHF BHLLHF BHHHHF BHHHHF
BHLLHF BHLLHF BHHHHF BHHHHF BHLLHF BHLLHF BHHHHF BHHHHF
BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF BHLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLHHF BLLHHF BLLLHF BLLLHF BLLHHF BLLHHF
BLLLHF BLLLHF BLLHHF BLLHHF BLLLHF BLLLHF BLLHHF BLLHHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLHHF BLLHHF BLLLHF BLLLHF BLLHHF BLLHHF
BLLLHF BLLLHF BLLHHF BLLHHF BLLLHF BLLLHF BLLHHF BLLHHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF BLLLHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHLF BHHHHF BHHHHF
BHHHHF BHHHLF BHHHHF BHHHHF BHHLHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHLHF BHHHHF BHHHHF BHHHHF BHLHHF BHHHHF BHHHHF
BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF
BHHHLF BHHHLF BHHHHF BHHHHF BHHHLF BHHHLF BHHHHF BHHHHF
BHHHLF BHHHLF BHHHHF BHHHHF BHHHLF BHHLLF BHHHHF BHHHHF
BHHLLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHLHLF
BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF
BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF
BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF BHHLLF
BHHLLF BHHLLF BHHLLF BHLLLF BHHLLF BHHLLF BHHLLF BHHLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHHLLF BHHLLF BHLLLF BHLLLF BHHLLF BHHLLF
BHLLLF BHLLLF BHHLLF BHHLLF BHLLLF BHLLLF BHHLLF BHHLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF BHLLLF
```

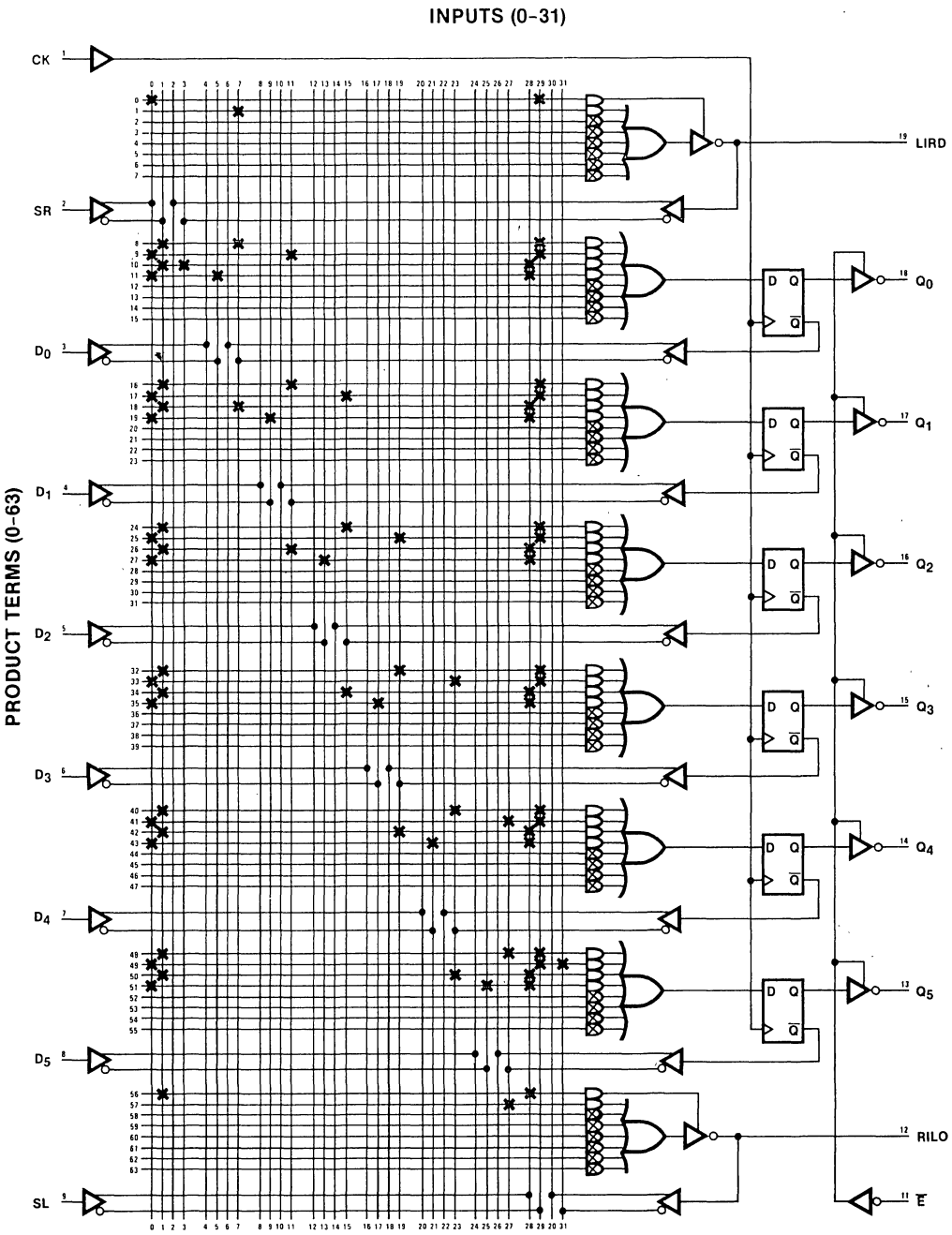
```
                    11 1111 1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0 0000 0000 0000 0000 0000 0000 0000 0000
 1 0000 0000 0000 0000 0000 0000 0000 0000
 2 0000 0000 0000 0000 0000 0000 0000 0000
 3 0000 0000 0000 0000 0000 0000 0000 0000
 4 0000 0000 0000 0000 0000 0000 0000 0000
 5 0000 0000 0000 0000 0000 0000 0000 0000
 6 0000 0000 0000 0000 0000 0000 0000 0000
 7 0000 0000 0000 0000 0000 0000 0000 0000

 8 ---- ---X --00 --00 --00 --00 ---- ---- /A
 9 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
10 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
11 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
12 0000 0000 0000 0000 0000 0000 0000 0000
13 0000 0000 0000 0000 0000 0000 0000 0000
14 0000 0000 0000 0000 0000 0000 0000 0000
15 0000 0000 0000 0000 0000 0000 0000 0000

16 X-X- ---- --00 --00 --00 --00 ---- ---- C*D
17 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
18 0000 0000 0000 0000 0000 0000 0000 0000
19 0000 0000 0000 0000 0000 0000 0000 0000
20 0000 0000 0000 0000 0000 0000 0000 0000
21 0000 0000 0000 0000 0000 0000 0000 0000
22 0000 0000 0000 0000 0000 0000 0000 0000
23 0000 0000 0000 0000 0000 0000 0000 0000

24 ---- X--- --00 --00 --00 --00 ---- ---- F
25 ---- ---- X-00 --00 --00 --00 ---- ---- G
26 0000 0000 0000 0000 0000 0000 0000 0000
27 0000 0000 0000 0000 0000 0000 0000 0000
28 0000 0000 0000 0000 0000 0000 0000 0000
29 0000 0000 0000 0000 0000 0000 0000 0000
30 0000 0000 0000 0000 0000 0000 0000 0000
31 0000 0000 0000 0000 0000 0000 0000 0000

32 ---- ---- --00 -XOO -XOO --00 ---- ---- /M*/N
33 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
34 0000 0000 0000 0000 0000 0000 0000 0000
35 0000 0000 0000 0000 0000 0000 0000 0000
36 0000 0000 0000 0000 0000 0000 0000 0000
37 0000 0000 0000 0000 0000 0000 0000 0000
38 0000 0000 0000 0000 0000 0000 0000 0000
39 0000 0000 0000 0000 0000 0000 0000 0000

40 ---- ---- --00 --00 --00 X-00 -X-- ---- P*/Q
41 ---- ---- --00 --00 --00 -XOO X--- ---- /P*Q
42 0000 0000 0000 0000 0000 0000 0000 0000
43 0000 0000 0000 0000 0000 0000 0000 0000
44 0000 0000 0000 0000 0000 0000 0000 0000
45 0000 0000 0000 0000 0000 0000 0000 0000
46 0000 0000 0000 0000 0000 0000 0000 0000
47 0000 0000 0000 0000 0000 0000 0000 0000

48 ---- ---- --00 --00 --00 --00 ---- -X-- /I
49 ---- ---- --00 --00 --00 --00 ---- ---X /J
50 ---- ---- --00 --00 --00 --00 ---X ---- /K
51 XXXX XXXX XXOO XXOO XXOO XXOO XXXX XXXX
52 0000 0000 0000 0000 0000 0000 0000 0000
53 0000 0000 0000 0000 0000 0000 0000 0000
54 0000 0000 0000 0000 0000 0000 0000 0000
55 0000 0000 0000 0000 0000 0000 0000 0000

56 0000 0000 0000 0000 0000 0000 0000 0000
57 0000 0000 0000 0000 0000 0000 0000 0000
58 0000 0000 0000 0000 0000 0000 0000 0000
59 0000 0000 0000 0000 0000 0000 0000 0000
60 0000 0000 0000 0000 0000 0000 0000 0000
61 0000 0000 0000 0000 0000 0000 0000 0000
62 0000 0000 0000 0000 0000 0000 0000 0000
63 0000 0000 0000 0000 0000 0000 0000 0000


LEGEND:  X : FUSE NOT BLOWN (L,N,0)    - : FUSE BLOWN    (H,P,1)
         0 : PHANTOM FUSE   (L,N,0)    O : PHANTOM FUSE (H,P,1)
```

EXAMPLE 2:
6-BIT SHIFT REGISTER WITH THREE-STATE OUTPUTS



Manual Coding: 6-Bit Shift Register with Three-State Outputs

Logic Diagram PAL16R6



Manual Coding: 6-Bit Shift Register with Three-State Outputs

Programming Format **PAL12H6**

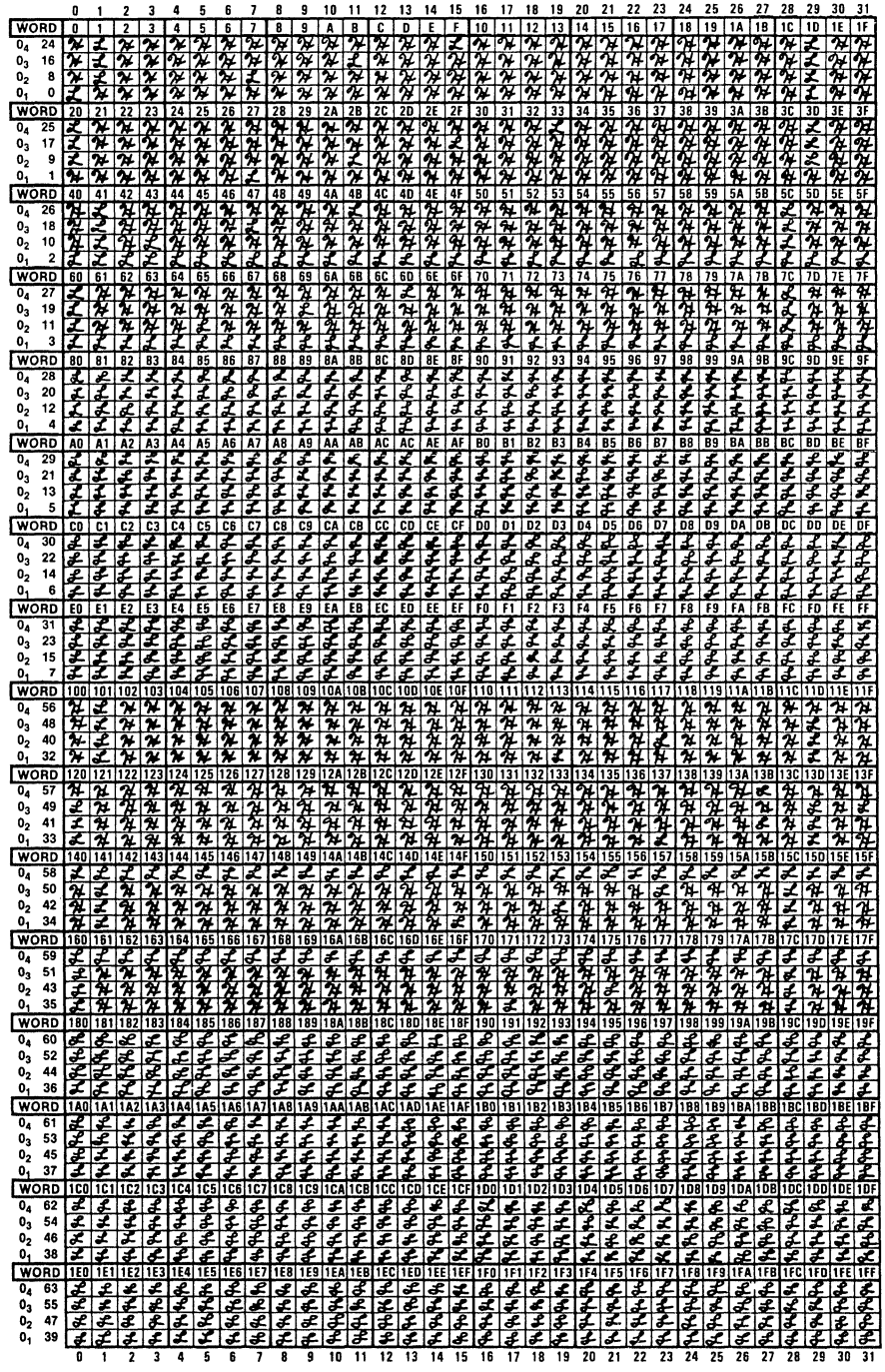
PATTERN: _____

NAME: _____

DATE: _____

PRODUCT TERMS (0–63)

INPUTS (0–31)



PALASM Output: 6-Bit Shift Register with Three-State Outputs

Design Specification PAL16R6

```
PAL16R6                                          PAL DESIGN SPECIFICATION
PAT0005
6-BIT SHIFT REGISTER WITH THREE-STATE OUTPUTS
MMI,SV
CK SR D0 D1 D2 D3 D4 D5 SL GND /E RILO Q5 Q4 Q3 Q2 Q1 Q0 LIRO VCC

IF(SR*/SL) /LIRO=/Q0
/Q0 := /SR*/SL*/Q0 + SR*/SL*/Q1 + /SR*SL*/LIRO + SR*SL*/D0
/Q1 := /SR*/SL*/Q1 + SR*/SL*/Q2 + /SR*SL*/Q0 + SR*SL*/D1
/Q2 := /SR*/SL*/Q2 + SR*/SL*/Q3 + /SR*SL*/Q1 + SR*SL*/D2
/Q3 := /SR*/SL*/Q3 + SR*/SL*/Q4 + /SR*SL*/Q2 + SR*SL*/D3
/Q4 := /SR*/SL*/Q4 + SR*/SL*/Q5 + /SR*SL*/Q3 + SR*SL*/D4
/Q5 := /SR*/SL*/Q5 + SR*/SL*/RILO + /SR*SL*/Q4 + SR*SL*/D5
IF(/SR*SL) /RILO=/Q5

DESCRIPTION:
THE 6-BIT SHIFT REGISTER WILL HOLD , SHIFT RIGHT, SHIFT LEFT, OR LOAD
ON THE RISING EDGE OF THE CLOCK (CK).
THE THREE STATE OUTPUTS ARE HIGH-Z WHEN THE ENABLE LINE (/E) IS HIGH AND
ENABLED WHEN ENABLE LINE (/E) IS LOW.
```

INPUTS					OUTPUTS							
SL	SR	RILO	LIRO	CLOCK	RILO	Q5	Q4	Q3	Q2	Q1	Q0	LIRO	OPERATION
L	L	X	X	L-H	Z	Q5	Q4	Q3	Q2	Q1	Q0	Z	HOLD
L	H	RI	X	L-H	Z	RI	Q5	Q4	Q3	Q2	Q1	Q1	RIGHT SHFT
H	L	X	LI	L-H	Q4	Q4	Q3	Q2	Q1	Q0	LI	Z	LEFT SHFT
H	H	X	X	L-H	Z	D5	D4	D3	D2	D1	D0	Z	LOAD D

```
NUMBER OF FUSES BLOWN =  818
```

PALASM Output

HEX FORMAT

```
E 1 F F F F F D F F F B F F F 7 F F F F F F F F F F F F 0 F F .
1 F F F F F F E F F F D F F F B F F F 7 F F F F F F F F 1 F F .
E 0 E C E E E A E E E 6 E E E E E E E E E E E E E E E 0 E E E .
0 E E E E C E E E A E E E 6 E E E E E E E E E E E E 0 E E E .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
F 0 F F F F F F F F F F F F F F F F F F F F F F F F B 7 8 F F .
8 F F F F F F F F F F F F F F F F F F F F E F F F 5 F 8 F B .
7 0 7 7 7 7 7 7 7 7 7 7 7 7 6 7 7 7 5 7 7 7 3 7 7 7 7 0 7 7 7 .
0 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 6 7 7 7 5 7 7 7 3 7 7 0 7 7 7 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 .
```

PALASM Output: 6-Bit Shift Register with Three-State Outputs

BHLF Format PAL16R6

```
BHHHLF BLLLHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHLHF
BHHHHF BHHHHF BHHHHF BHLHHF BHHHHF BHHHHF BHHHHF BLHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BLLLLF BHHHHF BHHHHF
BLLLHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHLF
BHHHHF BHHHHF BHHHHF BHHLHF BHHHHF BHHHHF BHHHHF BHLHHF
BHHHHF BHHHHF BHHHHF BLHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BLLLHF BHHHHF BHHHHF
BHHHLF BLLLLF BHHHLF BHHLLF BHHHLF BHHHLF BHHHLF BHLHLF
BHHHLF BHHHLF BHHHLF BLHHLF BHHHLF BHHHLF BHHHLF BHHHLF
BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF
BHHHLF BHHHLF BHHHLF BHHHLF BLLLLF BHHHLF BHHHLF BHHHLF
BLLLLF BHHHLF BHHHLF BHHHLF BHHHLF BHHLLF BHHHLF BHHHLF
BHHHLF BHLHLF BHHHLF BHHHLF BHHHLF BLHHLF BHHHLF BHHHLF
BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF BHHHLF
BHHHLF BHHHLF BHHHLF BHHHLF BLLLLF BHHHLF BHHHLF BHHHLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BHHHHF BLLLLF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHLF BHHHHF BHHHHF BHHHHF BHHLHF
BHHHHF BHHHHF BHHHHF BHLHHF BLHHHF BHLLLF BHHHHF BHHHHF
BHLLLF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF
BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHHF BHHHLF
BHHHHF BHHHHF BHHHHF BLHLHF BHHHHF BHLLLF BHHHHF BHLHHF
BLHHHF BLLLLF BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF
BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF BLHHLF
BLHHHF BLHHHF BLHHHF BLHLHF BLHHHF BLHHHF BLHHHF BLLHHF
BLHHHF BLHHHF BLHHHF BLHHHF BLLLLF BLHHHF BLHHHF BLHHHF
BLLLLF BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF
BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF BLHHHF
BLHHHF BLHHLF BLHHHF BLHHHF BLHHHF BLHLHF BLHHHF BLHHHF
BLHHHF BLLHHF BLHHHF BLHHHF BLLLLF BLHHHF BLHHHF BLHHHF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF BLLLLF
```

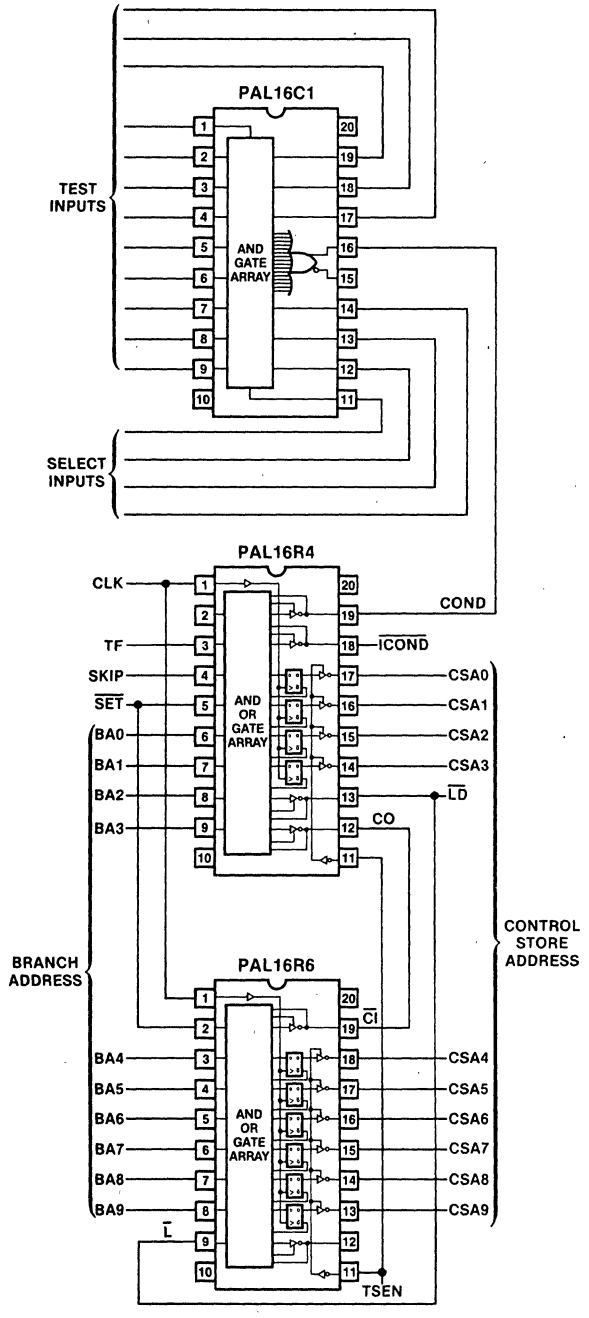
PALASM Output: 6-Bit Shift Register with Three-State Outputs

Fuse Plot PAL16R6

```
                    11 111  1111 2222 2222 2233
    0123 4567 8901 2345 6789 0123 4567 8901

 0  X--- ---- ---- ---- ---- ---- ---- -X-- SR*/SL
 1  ---- ---X ---- ---- ---- ---- ---- ---- /Q0
 2  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 3  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 4  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 5  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 6  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
 7  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

 8  -X-- ---X ---- ---- ---- ---- ---- -X-- /SR*/SL*/Q0
 9  X--- ---- ---X ---- ---- ---- ---- -X-- SR*/SL*/Q1
10  -X-X ---- ---- ---- ---- ---- ---- X--- /SR*SL*/LIRO
11  X--- -X-- ---- ---- ---- ---- ---- X--- SR*SL*/D0
12  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
13  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
14  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
15  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

16  -X-- ---- ---X ---- ---- ---- ---- -X-- /SR*/SL*/Q1
17  X--- ---- ---- ---X ---- ---- ---- -X-- SR*/SL*/Q2
18  -X-- ---X ---- ---- ---- ---- ---- X--- /SR*SL*/Q0
19  X--- ---- -X-- ---- ---- ---- ---- X--- SR*SL*/D1
20  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
21  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
22  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
23  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

24  -X-- ---- ---- ---X ---- ---- ---- -X-- /SR*/SL*/Q2
25  X--- ---- ---- ---- ---X ---- ---- -X-- SR*/SL*/Q3
26  -X-- ---- ---X ---- ---- ---- ---- X--- /SR*SL*/Q1
27  X--- ---- ---- -X-- ---- ---- ---- X--- SR*SL*/D2
28  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
29  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
30  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
31  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

32  -X-- ---- ---- ---- ---X ---- ---- -X-- /SR*/SL*/Q3
33  X--- ---- ---- ---- ---- ---X ---- -X-- SR*/SL*/Q4
34  -X-- ---- ---- ---X ---- ---- ---- X--- /SR*SL*/Q2
35  X--- ---- ---- ---- -X-- ---- ---- X--- SR*SL*/D3
36  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
37  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
38  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
39  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

40  -X-- ---- ---- ---- ---- ---X ---- -X-- /SR*/SL*/Q4
41  X--- ---- ---- ---- ---- ---- ---X -X-- SR*/SL*/Q5
42  -X-- ---- ---- ---- ---X ---- ---- X--- /SR*SL*/Q3
43  X--- ---- ---- ---- ---- -X-- ---- X--- SR*SL*/D4
44  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
45  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
46  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
47  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

48  -X-- ---- ---- ---- ---- ---- ---X -X-- /SR*/SL*/Q5
49  X--- ---- ---- ---- ---- ---- ---- -X-X SR*/SL*/RILO
50  -X-- ---- ---- ---- ---- ---X ---- X--- /SR*SL*/Q4
51  X--- ---- ---- ---- ---- ---- -X-- X--- SR*SL*/D5
52  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
53  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
54  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
55  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

56  -X-- ---- ---- ---- ---- ---- ---- X--- /SR*SL
57  ---- ---- ---- ---- ---- ---- ---X ---- /Q5
58  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
59  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
60  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
61  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
62  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX
63  XXXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX

LEGEND:  X : FUSE NOT BLOWN (L,N,0)    - : FUSE BLOWN    (H,P,1)
```

CONTROL STORE SEQUENCER

Solutions to control store sequencing are as varied as the problems that are solved by microprogrammed hardware. The traditional approach tends to be horizontally structured, whereas the application described here is designed for use with a vertical control store structure. The vertical control store has narrow control fields and may share field functions to increase efficiency. It is fast.



Control Store Sequencer Logic Schematic.

How It Works

This control store sequencer is designed to use a minimum of control bits while providing sufficient sequencing flexibility. Only three bits are required for the basic sequencer control. They make three things happen:

CSA = CSA + 1	Increment control store address
CSA = CSA + 2	A sort of branch instruction
CSA = BA	Load a branch address

The three control bits are SKIP, COND, and TF.

Skip defines whether the sequencer will skip or load.

Cond is the condition that is tested to see if the sequencer executed the operation defined by Skip.

TF defines whether Cond is tested true or false.

Table below lists all of the states the sequencer can assume.

Sequencer States

Skip	Cond	TF	Operation
0	0	0	Load
0	0	1	Increment
0	1	0	Increment
0	1	1	Load
1	0	0	Skip
1	0	1	Increment
1	1	0	Increment
1	1	1	Skip

There are two additional control bits, whose use is left to your discretion. They are /SET and /TSEN.

/Set is a synchronous preset that is usually used as a power-on reset; however, it may also be used as a one-bit vector to the last addressable location during normal operation.

/Tsen is the enable for the TRI-STATE™ outputs. This has several possible uses, one of which might be testing the hardware by the method of disabling the outputs, then supplying a test address from an external source.

The sequencer generates ten bits, which are divided into two parts. The least-significant four bits are constructed from a PAL16R4, and control the skip operation. During a skip, the state of the LSB is maintained and the next three bits function as a three-bit binary counter. During an increment, all four least-significant bits function as a binary counter. Carry out (/CO) is generated during skip when CSA_1 through CSA_3 = 1, and during increment when CSA_0 through CSA_3 = 1. Load (/LD) is also generated by the least-significant part, as a function of COND and TF. (See table below.)

/LD States

TF	Cond	/LD
0	0	0
0	1	1
1	0	1
1	1	0

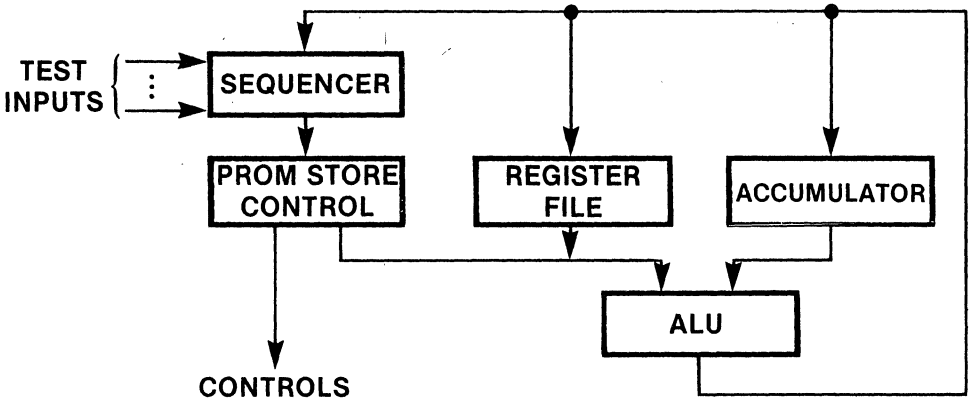
The most-significant six bits are constructed using a PAL16R6, functioning as a six-bit binary counter with carry-in (CI), synchronous load (/LD), and synchronous set (/SET). There is an extra pin that can be used to generate carry-out if you need more than ten bits.

System Integration

One of the first features that is desirable from a system standpoint is the expansion of the COND input to accommodate more than one condition for testing. The can be done nicely by using a 16C1 as a multiplexer. In this scheme, four terms are used as input selects. This leaves 12 terms to be used as condition inputs. This might seem wasteful at first, as 4 select terms could decode 16 inputs. Using the PAL, however, it is only a superficial waste, and the trade-off is the greater design flexibility you have by comparison with a standard multiplexer.

One COND output should be either true or false in order to generate unconditional increments, skips, or branches. The true or false state needs only to be a function of the four select terms, and doesn't require a condition input to be grounded or pulled up. Other functions, such as AND, OR, or XOR, can be performed on the condition inputs internally, too--functions a multiplexer would force you to design in external logic.

The following Figure shows how the sequencer design described here can be integrated into a system that provides subroutine capability. In the figure, the same control-store field is used to generate literals and branch addresses. Subroutining is accomplished by loading the return address into the register file before the subroutine jump is taken and then reading the return address out of the file when the subroutine's return executes.



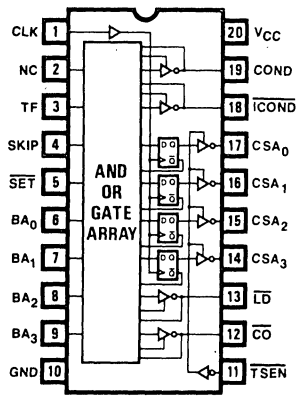
System Implementation of Sequencer

Control Store Sequencer, Most Significant Stage

Design Specification PAL16R4

```
PAL16R4                                                PAL DESIGN SPECIFICATION
PAT0028
CONTROL STORE SEQUENCER, LEAST SIGNIFICANT STAGE

CLK NC TF SKIP /SET BA0 BA1 BA2 BA3 GND /TSEN /CO /LD
CSA3 CSA2 CSA1 CSA0 /ICOND COND VCC

/CSA0 := /SET*/ICOND*CSA0 + /SET*ICOND*SKIP*/CSA0 + /SET*ICOND*/SKIP*/BA0

/CSA1 := /SET*CSA0*CSA1*/ICOND + /SET*/ICOND*/CSA0*/CSA1
       + /SET*ICOND*SKIP*CSA1 + /SET*ICOND*/SKIP*/BA2

/CSA2 := /SET*/ICOND*CSA0*CSA1*CSA2 + /SET*/ICOND*/CSA0*/CSA2
       + /SET*/LD*/CSA1*/CSA2 + /SET*/ICOND*SKIP*CSA1*CSA2
       + /SET*ICOND*/SKIP*/BA2

/CSA3 := /SET*/ICOND*CSA0*CSA1*CSA2*CSA3
       + /SET*/ICOND*/CSA0*/CSA3 + /SET*/LD*/CSA1*/CSA3
       + /SET*/LD*/CSA2*/CSA3 + /SET*ICOND*SKIP*CSA1*CSA2*CSA3
       + /SET*ICOND*/SKIP*/BA3

IF(VCC)  CO = CSA0*CSA1*CSA2*CSA3
            + TF*COND*SKIP*CSA1*CSA2*CSA3
            + /TF*/COND*SKIP*CSA1*CSA2*CSA3

IF(VCC)  ICOND = TF*COND + /TF*/COND

IF(VCC)  LD = TF*COND*/SKIP + /TF*/COND*/SKIP

DESCRIPTION:  SEE TEXT
```

PAL16R4



Logic Symbol

Control Store Sequencer, Least Significant Stage, Design Specification.

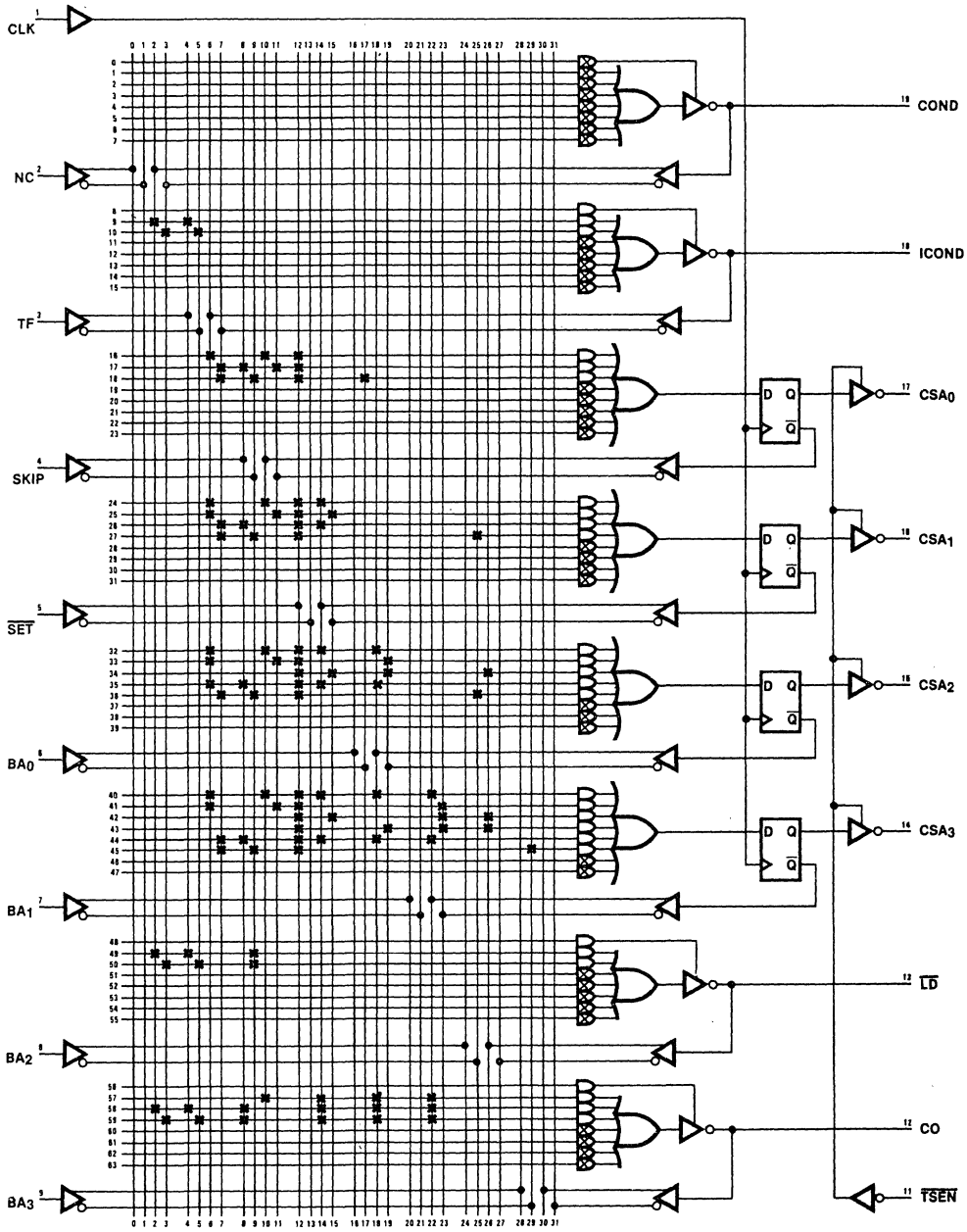
Control Store Sequencer, Most Significant Stage

Fuse Pattern PAL16R4

Control Store Sequencer, Least Significant Stage, Fuse Pattern.

Control Store Sequencer, Most Significant Stage

Logic Diagram PAL16R4



Control Store Sequencer, Least Significant State, Logic Diagram.

Control Store Sequencer, Most Significant Stage

Design Specification PAL16R6

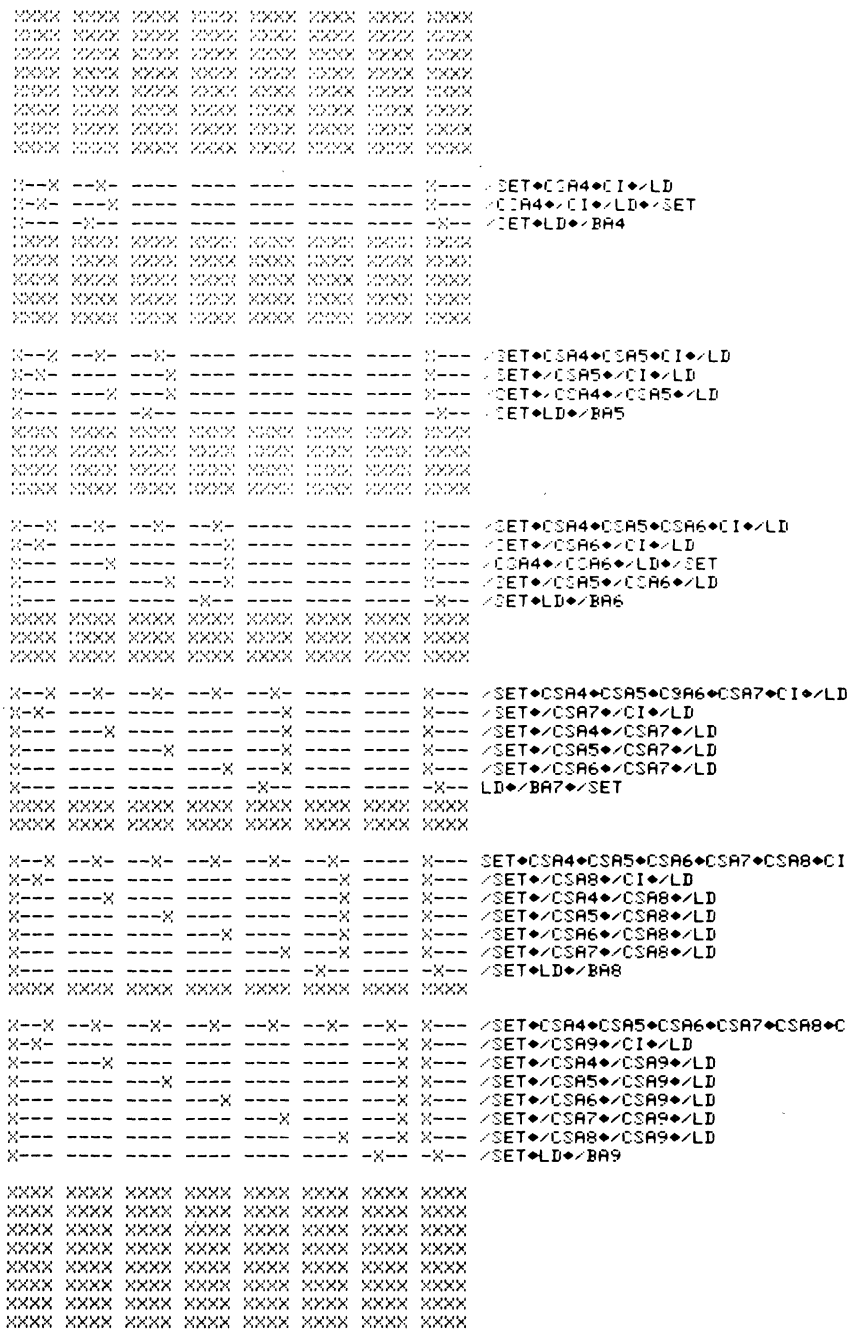
```
PAL16R6                                                PAL DESIGN SPECIFICATION
PAT0029
CONTROL STORE SEQUENCER, MOST SIGNIFICANT STAGE

CLK /SET BA4 BA5 BA6 BA7 BA8 BA9 /LD GND /TSEN NC CSA9 CSA8 CSA7 CSA6
CSA5 CSA4 /CI VCC


/CSA4 := /SET*CSA4*CI*/LD + /CSA4*/CI*/LD*/SET + /SET*LD*/BA4


/CSA5 := /SET*CSA4*CSA5*CI*/LD + /SET*/CSA5*/CI*/LD
       + /SET*/CSA4*/CSA5*/LD + /SET*LD*/BA5


/CSA6 := /SET*CSA4*CSA5*CSA6*CI*/LD + /SET*/CSA6*/CI*/LD
       + /CSA4*/CSA6*/LD*/SET + /SET*/CSA5*/CSA6*/LD
       + /SET*LD*/BA6


/CSA7 := /SET*CSA4*CSA5*CSA6*CSA7*CI*/LD
       + /SET*/CSA7*/CI*/LD + /SET*/CSA4*/CSA7*/LD
       + /SET*/CSA5*/CSA7*/LD + /SET*/CSA6*/CSA7*/LD
       + LD*/BA7*/SET


/CSA8 := /SET*CSA4*CSA5*CSA6*CSA7*CSA8*CI*/LD
       + /SET*/CSA8*/CI*/LD + /SET*/CSA4*/CSA8*/LD
       + /SET*/CSA5*/CSA8*/LD + /SET*/CSA6*/CSA8*/LD
       + /SET*/CSA7*/CSA8*/LD + /SET*LD*/BA8


/CSA9 := /SET*CSA4*CSA5*CSA6*CSA7*CSA8*CSA9*CI*/LD
       + /SET*/CSA9*/CI*/LD + /SET*/CSA4*/CSA9*/LD
       + /SET*/CSA5*/CSA9*/LD + /SET*/CSA6*/CSA9*/LD
       + /SET*/CSA7*/CSA9*/LD + /SET*/CSA8*/CSA9*/LD
       + /SET*LD*/BA9



DESCRIPTION:

THE 6-BIT COUNTER INCREMENTS WHEN THE /LD LINE IS HIGH
IF CARRY AND /SET.  THE OUTPUTS ARE ENABLED WHEN /TSEN IS LOW.
```

/SET	CI	/LD	CLK	CSA	OPERATION
L	X	X	L-H	ALL HIGH	SET
H	X	L	L-H	BA	LD
H	H	H	L-H	CSA	NOP
H	L	H	L-H	CSA PLUS 1	INCR

Control Store Sequencer, Most Significant Stage, Design Specification.

Control Store Sequencer, Most Significant Stage

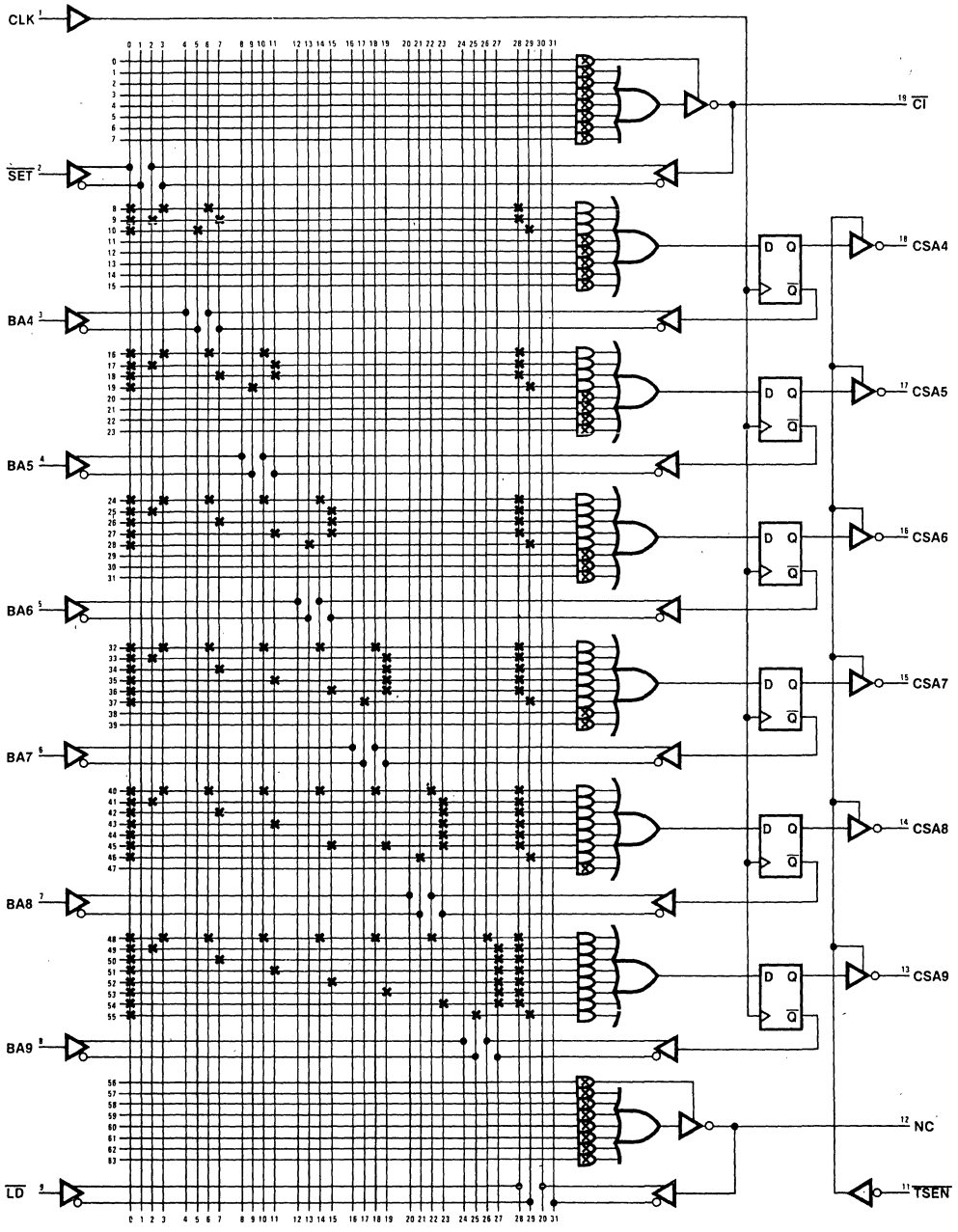
Fuse Pattern PAL16R6



Control Store Sequencer, Most Significant Stage, Fuse Pattern.

Control Store Sequencer, Most Significant Stage

Logic Diagram PAL16R6



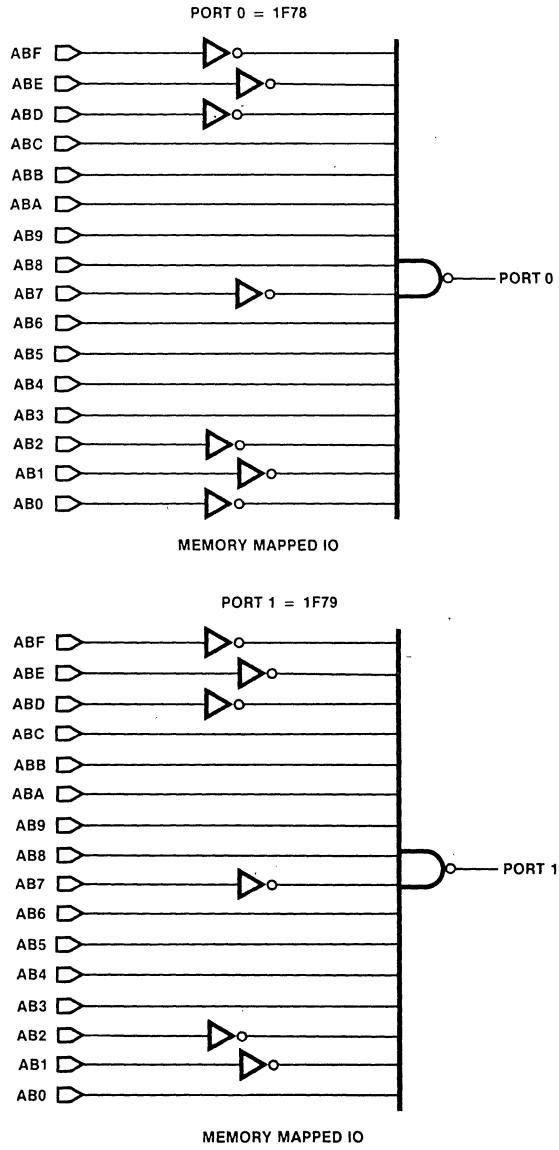
Control Store Sequencer, Most Significant Stage, Logic Diagram.

MEMORY-MAPPED I/O

Memory-mapped I/O is an interface technique that treats I/O devices' physical addresses as undifferentiated from memory address space. That is, no Memory-I/O decoding is required. Furthermore, most computers have more instructions to manipulate the contents of memory than they have I/O instructions. Therefore, the use of memory mapping can make I/O control much more flexible. PALs can be used to make memory-mapped I/O implementation easy, even if changes in memory addresses are required.

Functional Description

The figure below shows a circuit that is typical of those found in memory-mapped I/O applications. The inputs to the decode logic are the system memory address lines, A_0-A_F. The logic shown compares the address on the memory bus with the programmed comparison address. When an address on the bus matches, the corresponding I/O port enable signal is set. In conjunction with other system control signals, this enable can be used to transfer data to and from the system data bus.



Memory-Mapped I/O Logic Diagram

PAL Design

One PAL16L2 can be used to monitor a 16-bit address bus, fully decode addresses, and furnish enables to two ports, each of which could be anywhere within 64K of address space. Partial decoding for a larger number of ports could be done using other members of the PAL family.

Typical logic equations for the memory-mapped I/O logic are as follows:

Port 0 = /AB0 • /AB1 • /AB2 • AB3 • AB4 •
AB5 • AB6 • AB7 • AB8 • AB9 •
= ABA • ABB • ABC • /ABD • /ABE • /ABF •
[Note: source data incorrect]

Port 1 = AB0 • /AB1 • /AB2 • AB3 • AB4 •
AB5 • AB6 • /AB7 • AB8 • AB9 • ABA
• ABB • ABC • /ABD • /ABE •
/ABF•

The above example shows address decoding for memory locations $1F78_H$ and $1F79_H$. The equation terms could be changed to accommodate any 16-bit address.

Memory Mapped I/O

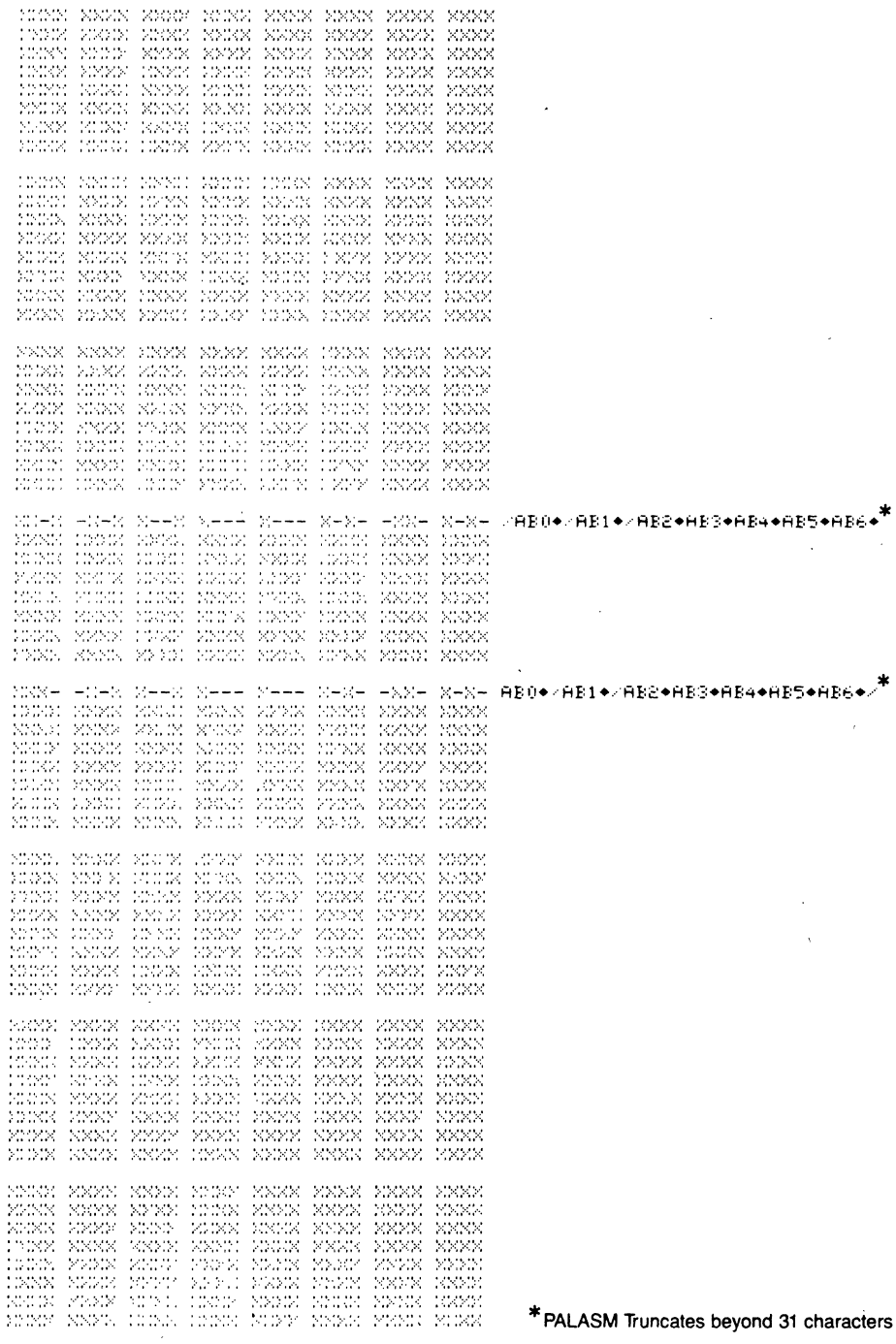
Design Specification PAL16L2

```
PAL16L2                                          PAL DESIGN SPECIFICATION
PAT0008
MEMORY MAPPED I/O

AB0 AB1 AB2 AB3 AB4 AB5 AB6 AB7 AB8 GND AB9 ABA ABB ABC
/PORT1 /PORT0 ABD ABE ABF VCC


PORT0   =   /AB0*/AB1*/AB2*AB3*AB4*AB5*AB6* AB7*AB8*AB9*ABA*ABB*ABC*
            /ABD*/ABE*/ABF

PORT1   =    AB0*/AB1*/AB2*AB3*AB4*AB5*AB6*/AB7*AB8*AB9*ABA*ABB*ABC*
            /ABD*/ABE*/ABF


DESCRIPTION:

THE PAL DECODES THE SPECIFIED MEMORY ADDRESS WORD TO PRODUCE A PORT
ENABLE FOR PORT0 AND PORT1 AS FOLLOWS:
```

PAL16L2 Memory-mapped I/O Decoder Design Specification.

Memory Mapped I/O

Fuse Pattern PAL16L2

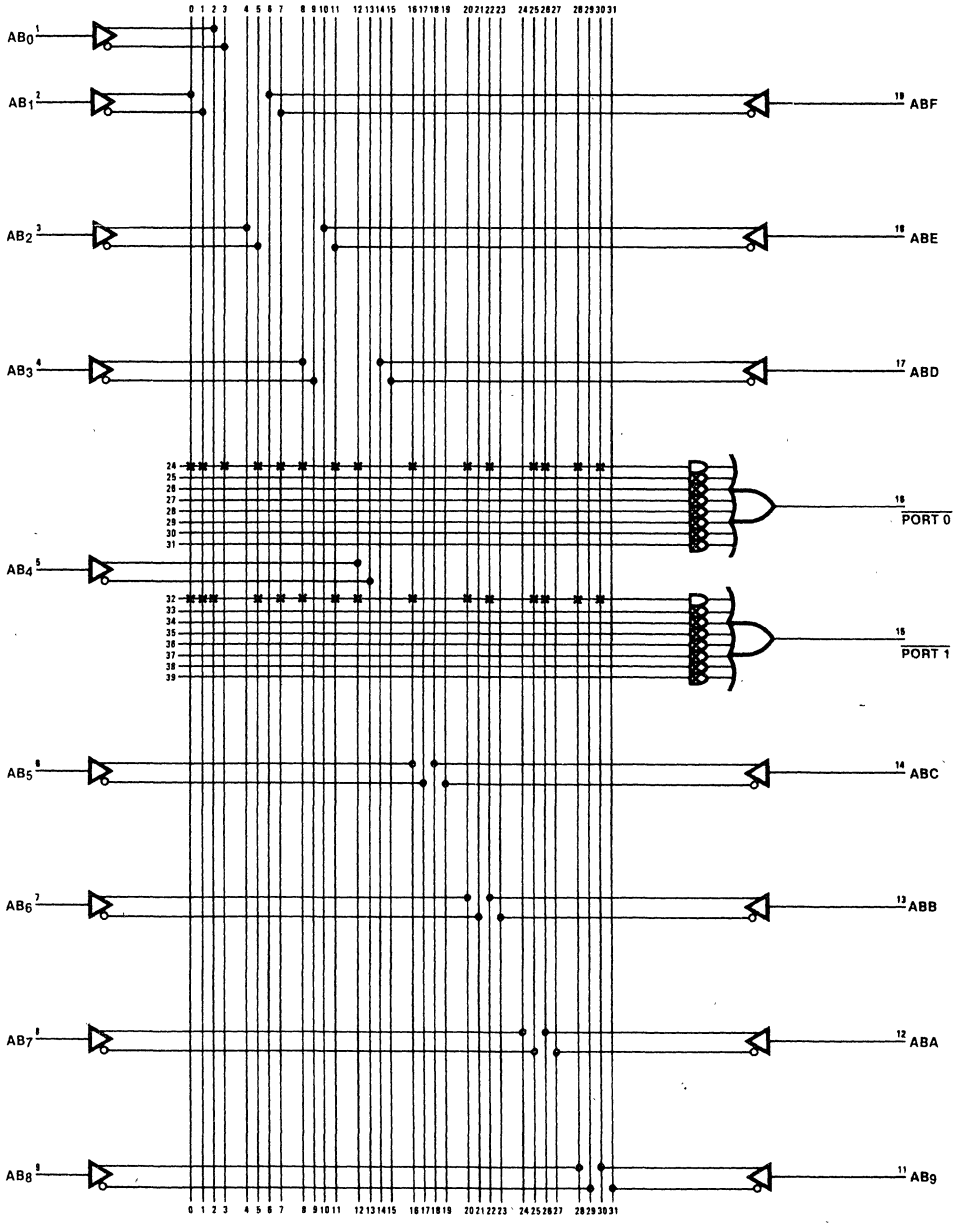


*PALASM Truncates beyond 31 characters

PAL16L2 Memory-mapped I/O Decoder Fuse Pattern.

Memory Mapped I/O

Logic Diagram PAL16L2

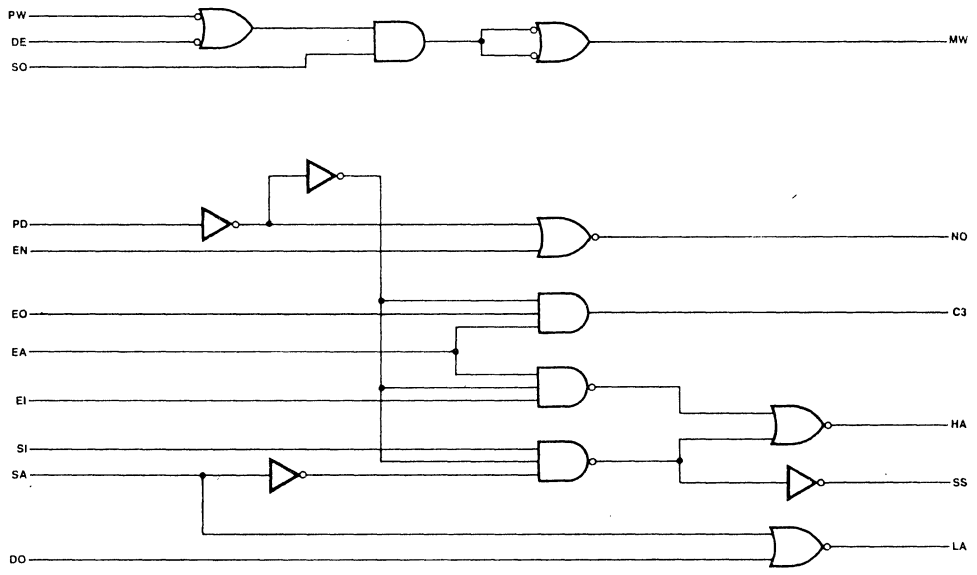


PAL16L2 Memory-mapped I/O Decoder Logic Diagram.

CONTROL LOGIC FOR 8080 CPU BOARD

The 8080 is one of the most widely-used of all current microprocessor designs. However, using it in a system requires that you decode and supply a fairly complex set of control signals.

With the rapid decline in 8080 prices, the logic required to perform this control decoding has become more expensive than the 8080 itself. This application note shows how a PAL can be used to eliminate much of this costly support logic on an 8080 CPU board.



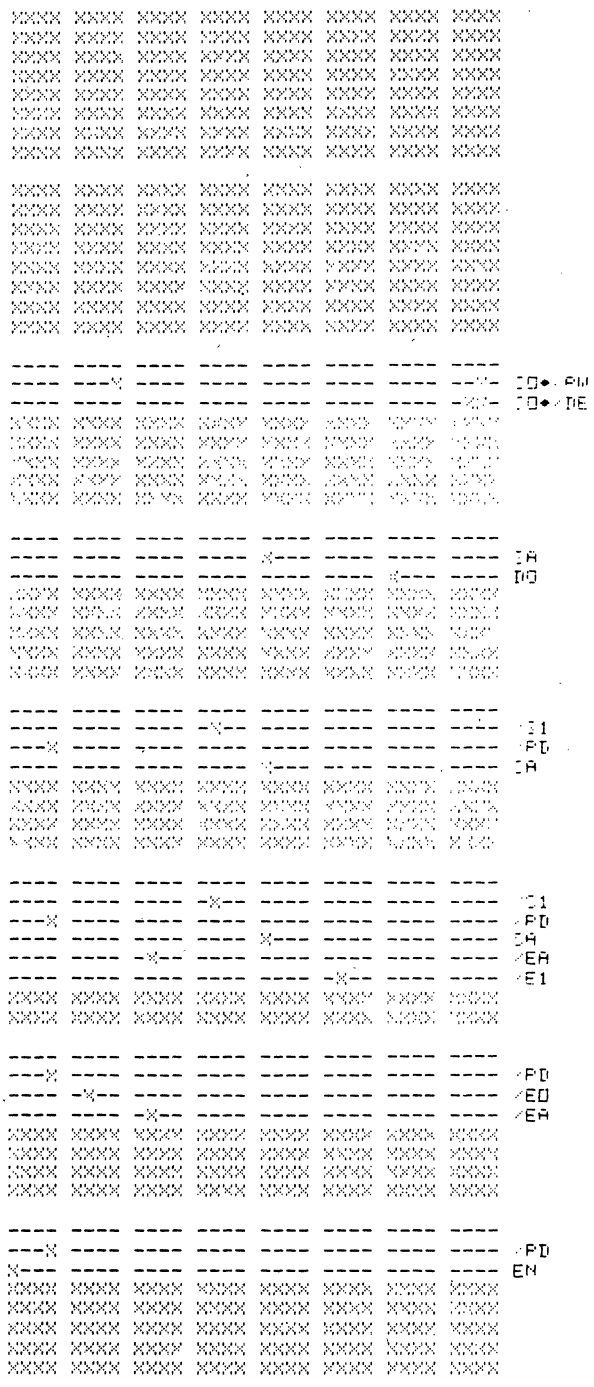
PAL16L8 Control Logic for 8080 CPU Board, Combinatorial Logic Diagram.

```
DESCRIPTION:
  PORTION OF LOGIC FROM 8080 CPU BOARD


PAL16L8                                                PAL DESIGN SPECIFICATION
PAT0012
PORTION OF RANDOM CONTROL LOGIC FOR 8080 CPU BOARD

PD EN EO EA S1 SA E1 DO DE GND SO NO C3 HA SS LA MW PW NC3 VCC


IF(/VCC) /MW= SO*/PW + SO*/DE

IF(/VCC) /LA= SA + DO

IF(/VCC) /SS= /S1 + /PD + SA

IF(/VCC) /HA= /S1 +/PD + SA + /EA + /E1

IF(/VCC) /C3= /PD + /EO + /EA

IF(/VCC) /NO= /PD + EN
```

PAL16L8 Control Logic for 8080 CPU Board, Design Specification.

Portion of Random Control Logic for 8080 CPU Board

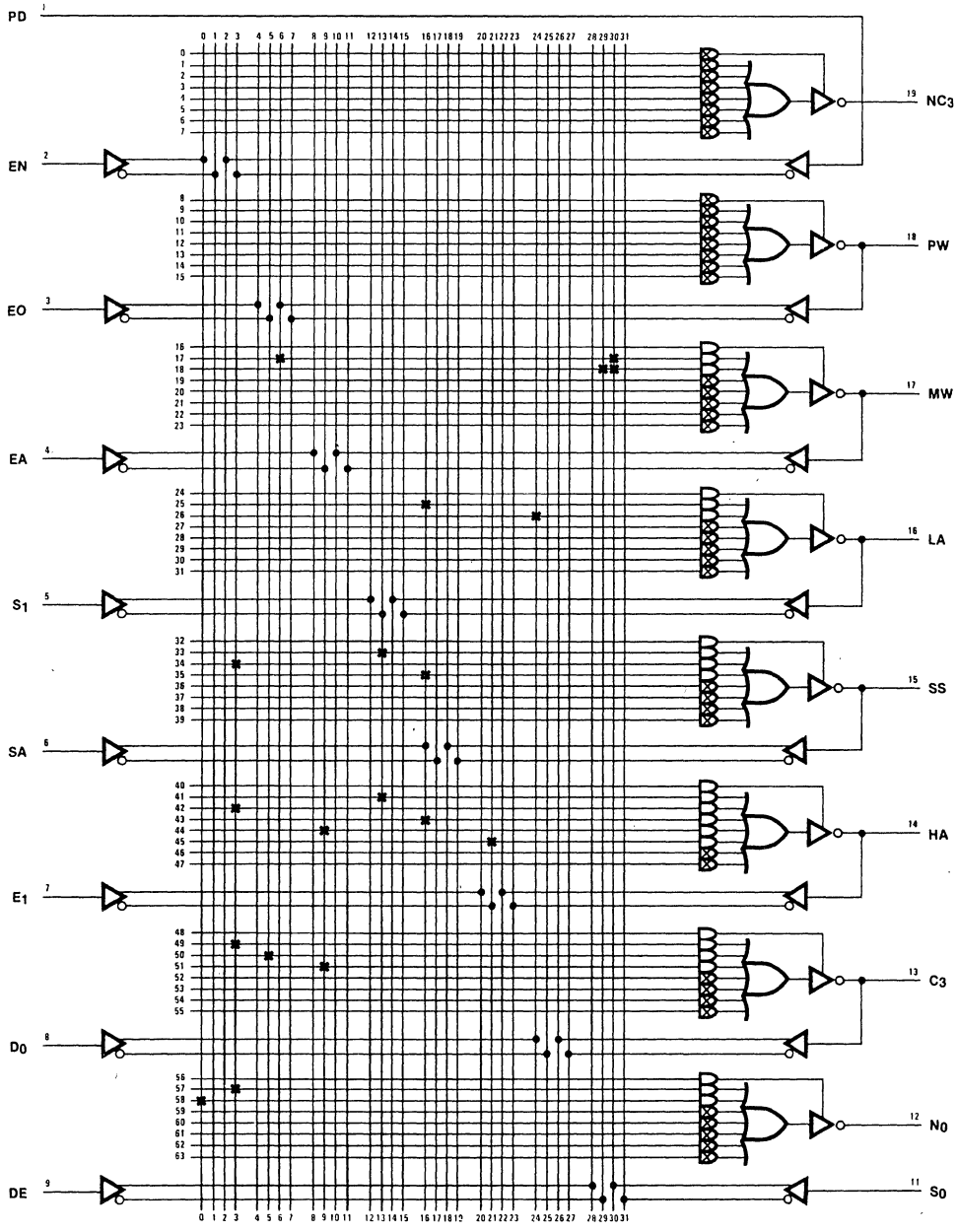
Fuse Pattern PAL16L8



PAL16L8 Control Logic for 8080 CPU Board, Fuse Pattern.

Portion of Random Control Logic for 8080 CPU Board

Logic Diagram PAL16L8



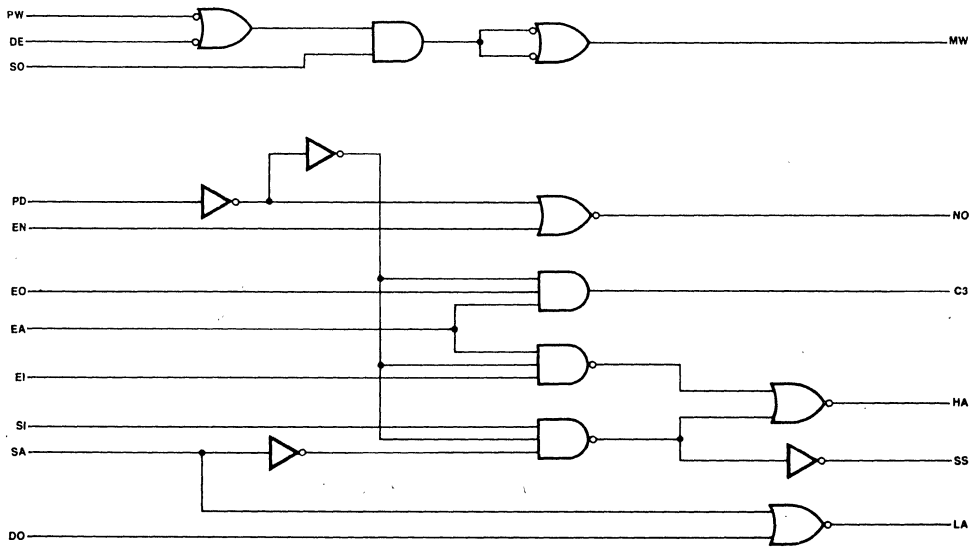
PAL16L8 Control Logic for 8080 CPU Board, Coded PAL Logic Diagram.

Portion of Random Control Logic for 8080 CPU Board (Improved Design)

Design Specification PAL12H6

```
PAL12H6                                                    PAL DESIGN SPECIFICATION
PAT0013
PORTION OF RANDOM CONTROL LOGIC FOR 8080 CPU BOARD

PD EN EO EA S1 SA E1 DO DE GND SO NC3 NO C3 HA SS LA MW PW VCC


MW = /SO + PW*DE

LA = /SA*/DO

SS = S1*PD*/SA

HA = S1*PD*/SA*EA*E1

C3 = PD*EO*EA

NO = PD*/EN


DESCRIPTION:
  PORTION OF LOGIC FROM 8080 CPU BOARD

NOTE:  THIS DESIGN IS IMPROVED OVER THE PREVIOUS EXAMPLE AS WE WERE
ABLE TO IMPLEMENT THE SAME EQUATIONS IN A SMALLER PAL.  THIS WAS
ACCOMPLISHED BY INVERTING THE EQUATIONS, THUS, REDUCING THE NUMBER OF
PRODUCTS PER OUTPUT TO A MAXIMUM OF TWO.
```

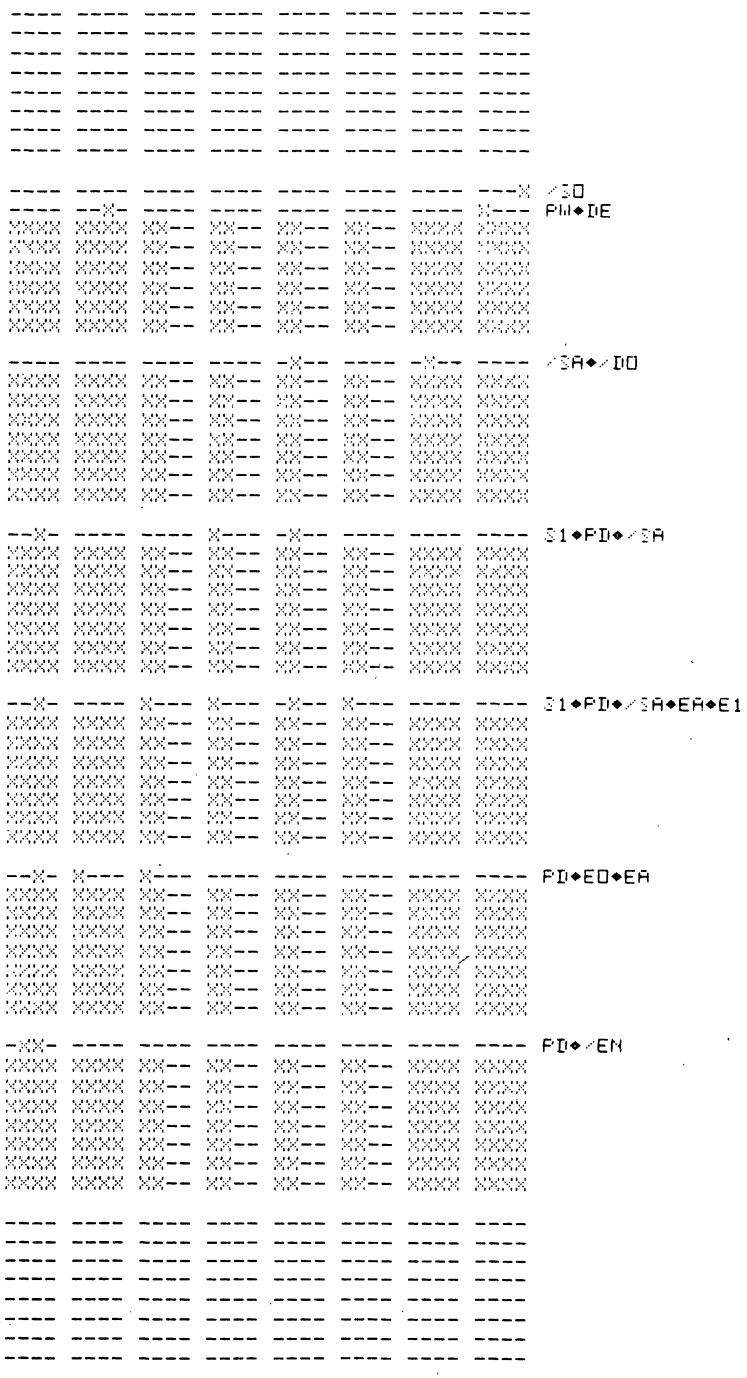
PAL12H6 Control Logic for 8080 CPU Board, Design Specification.



PAL12H6 Control Logic for 8080 CPU Board, Combinatorial Logic Diagram.

Portion of Random Control Logic for 8080 CPU Board (Improved Design)

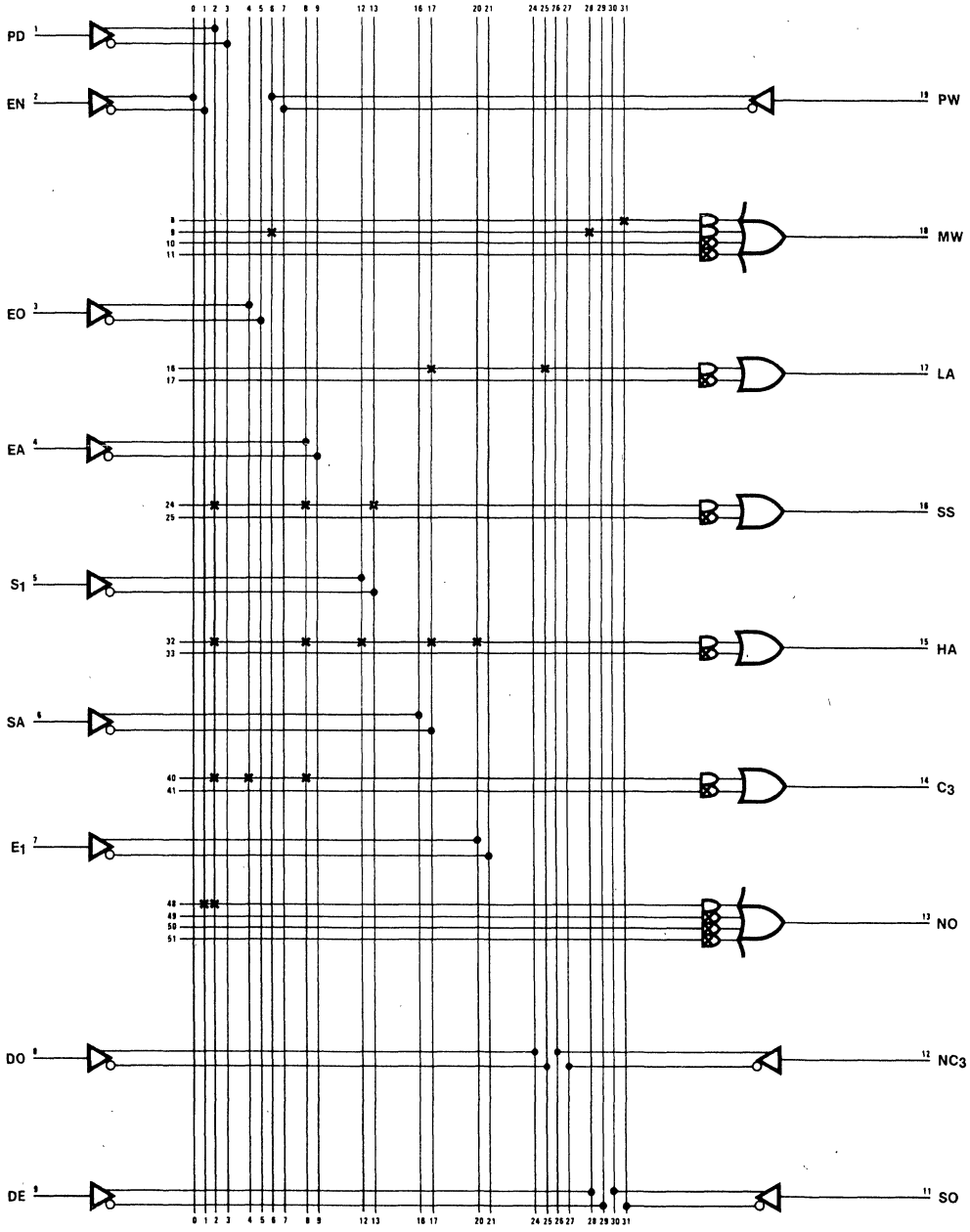
Fuse Pattern PAL12H6



PAL12H6 Control Logic for 8080 CPU Board, Fuse Pattern.

Portion of Random Control Logic for 8080 CPU Board (Improved Design)

Logic Diagram PAL12H6



PAL12H6 Control Logic for 8080 CPU Board, Coded PAL Logic Diagram.

HEXADECIMAL DECODER/LAMP DRIVER

The increasing use of microcomputers has led to an increased need to display numbers in hexadecimal format (0-9, A-F). Standard drivers for this function are not available, so most applications are forced to use several packages to decode each digit of the display. Since 6 to 12 digits are often being displayed, this approach can become very expensive. This example demonstrates how the hexadecimal display format can be both decoded and the LED indicators driven using a single PAL for each digit of the display.

Functional Description

A hex decoder/lamp driver accepts a four-bit hex digit, converts it to its corresponding seven-segment display code, and activates the appropriate segments on the display. These drivers can be used in both direct-drive and multiplexed display applications. A single PAL can provide both the basic decode/drive functions, and additional useful features as well.

Circuit Description

The figure shows three digits of a display system that uses three PALs to implement the complete decoding and display-driving functions. The inputs to each section are a hex code on pins D_0-D_3, a ripple blanking signal, an intensity control signal, and a lamp test signal.

The hex codes are decoded to form the seven-segment patterns shown in the figure. The input codes, digit, represented, and segments driven are as follows:

D_3	D_2	D_1	D_0	Digit	Segments
0	0	0	0	0	ABCDEF
0	0	0	1	1	BC
0	0	1	0	2	ABDEG
0	0	1	1	3	ABCDG
0	1	0	0	4	BCFG
0	1	0	1	5	ACDF
0	1	1	0	6	ACDEF
0	1	1	1	7	ABC
1	0	0	0	8	ABCDEFG
1	0	0	1	9	ABCFG
1	0	1	0	A	ABCEFG
1	0	1	1	B	CDEFG
1	1	0	0	C	ADEF
1	1	0	1	D	BCDEG
1	1	1	0	E	ADEFG
1	1	1	1	F	AEFG

Ripple-blanking input RBI is used to suppress leading zeroes in the display. The signal is propagated from the most significant digit to the least significant digit. If the digit input is zero and RBI is low (indicating that the previous digit is also zero), all segments are left blank and this digit position's ripple-blanking output RBO is set low.

Intensity control signal IC controls the duty cycle of the display driver. When IC is high, all segment drivers are turned off. Pulsing this pin with a duty-cycled signal allows the adjustment of the display's apparent brightness.

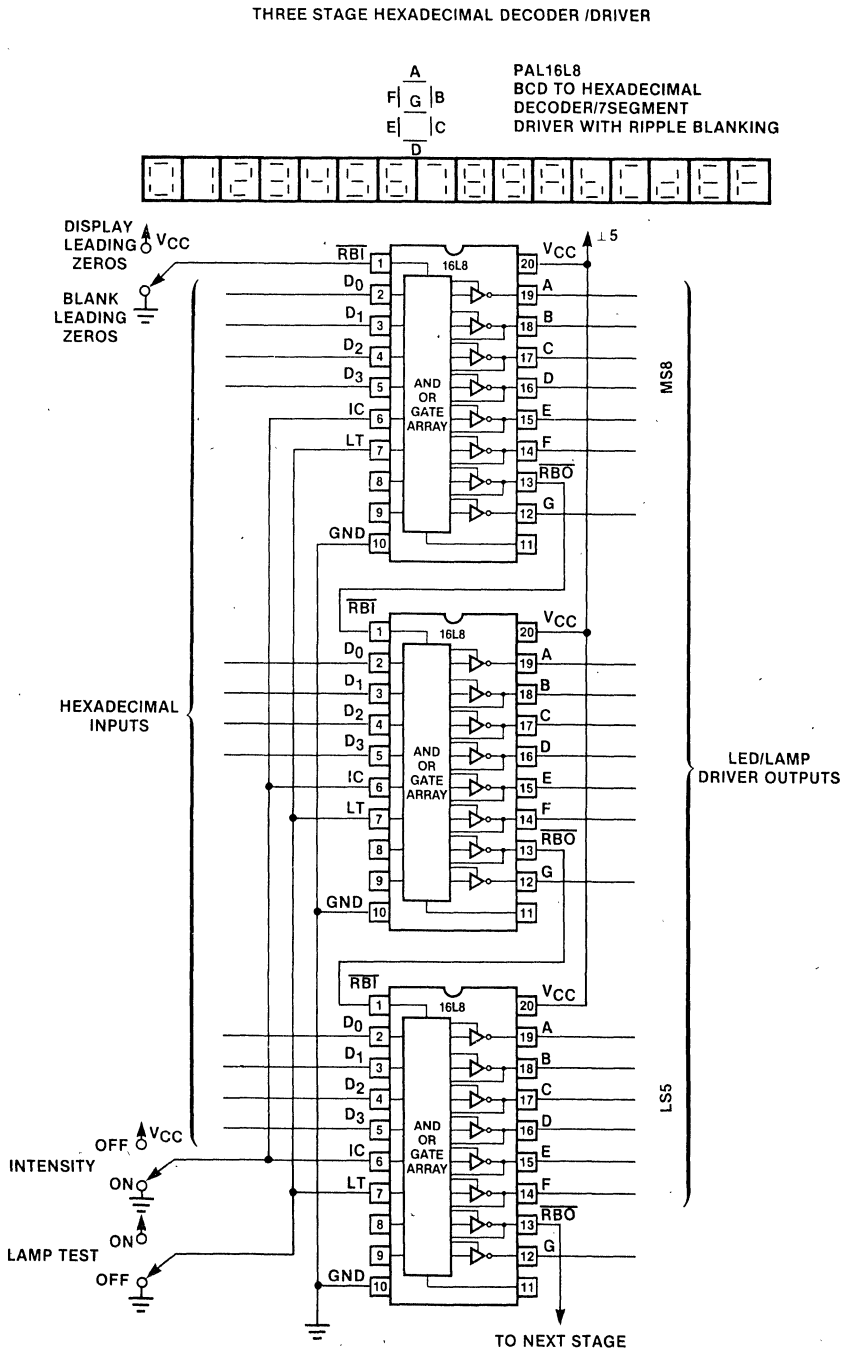
Lamp test signal LT lets you check to see if all LED segments are energized.

PAL Implementation

The PAL16L8 has both the required I/O pins and the drive current capability to perform as the complete display decoder-driver circuit with seven inputs and eight outputs. The logic equations for this circuits are shown in the listing. One PAL drives each digit; they may be cascaded without limit. With minor changes, the same logical structure could be used with multiplexer logic to allow a single PAL to decode and drive multiple digits.

Hex Decoder/7 Seg. Driver w/Ripple Blanking, Intensity Con., & Lamp Test

Logic Schematic



Hex Display Decoder-Driver, Combinatorial Logic Diagram.

Hex Decoder/7 Seg. Drive w/Ripple Blanking, Intensity Con., & Lamp Test

Design Specification PAL16L8

```
PAL16L8                                                    PAL DESIGN SPECIFICATION
PAT0007
HEX DECODER/7SEG. DRIVER W/RIPPLE BLANKING, INTENSITY CON., & LAMP TEST

/RBI D0 D1 D2 D3 IC LT NC NC GND NC G /RBO F E D C B A VCC



IF (/IC) /A = /RBO*/D0*/D2 + /RBO*D0*D3 + /RBO*D1*D2 +
              /RBO*D1*/D2*/D3 + /RBO*D0*D2*/D3 + /RBO*/D1*/D2*D3 + LT

IF (/IC) /B = /RBO*/D2*/D3 + /RBO*/D0*/D2 + /RBO*/D0*/D1*/D3 +
              /RBO*D0*D1*/D3 + /RBO*D0*/D1*D3 + LT

IF (/IC) /C = /RBO*D0*/D1 + /RBO*D0*/D2 + /RBO*/D1*/D2 +
              /RBO*D2*/D3 + /RBO*/D2*D3 + LT

IF (/IC) /D = /RBO*/D1*D3 + /RBO*/D0*/D2*/D3 +
              /RBO*D0*D1*/D2 + /RBO*/D0*D1*D2 + /RBO*D0*/D1*D2 + LT

IF (/IC) /E = /RBO*/D0*/D2 + /RBO*D2*D3 + /RBO*/D0*D1 +
              /RBO*D1*D3 + LT

IF (/IC) /F = /RBO*/D0*/D1 + /RBO*/D2*D3 + /RBO*D1*D3 +
              /RBO*/D0*D2 + /RBO*/D1*D2*/D3 + LT

IF (VCC)  RBO = /D0*/D1*/D2*/D3*/RBI

IF (/IC) /G = /RBO*D1*/D2 + /RBO*D0*D3 + /RBO*/D2*D3 +
              /RBO*/D0*D1 + /RBO*/D1*D2*/D3 + LT
```

DESCRIPTION:
THE HEXFDECIMAL DECODER/7-SEGMENT DRIVER FEATURES ACTIVE LOW OUTPUTS FOR DRIVING DISPLAY DIRECTLY.

IF DATA INPUT IS ZERO AND RIPPLE BLANKING INPUT (/RBI) IS LOW THAT DIGIT WILL BE BLANKED AND RIPPLE BLANKING OUTPUT WILL BE LOW.

THE RIPPLE BLANKING OUTPUT (/RBO) PROVIDES BLANKING INFORMATION FOR THE NEXT LEAST SIGNIFICANT STAGE. IT PROVIDES A LOW IF /RBI IS LOW AND THE DATA IN IS ZERO.

WHEN HIGH THE INTENSITY CONTROL (IC) WILL TURN OFF THE ENTIRE DISPLAY. IC MAY BE PULSED TO VARY THE INTENSITY OF THE DISPLAY.

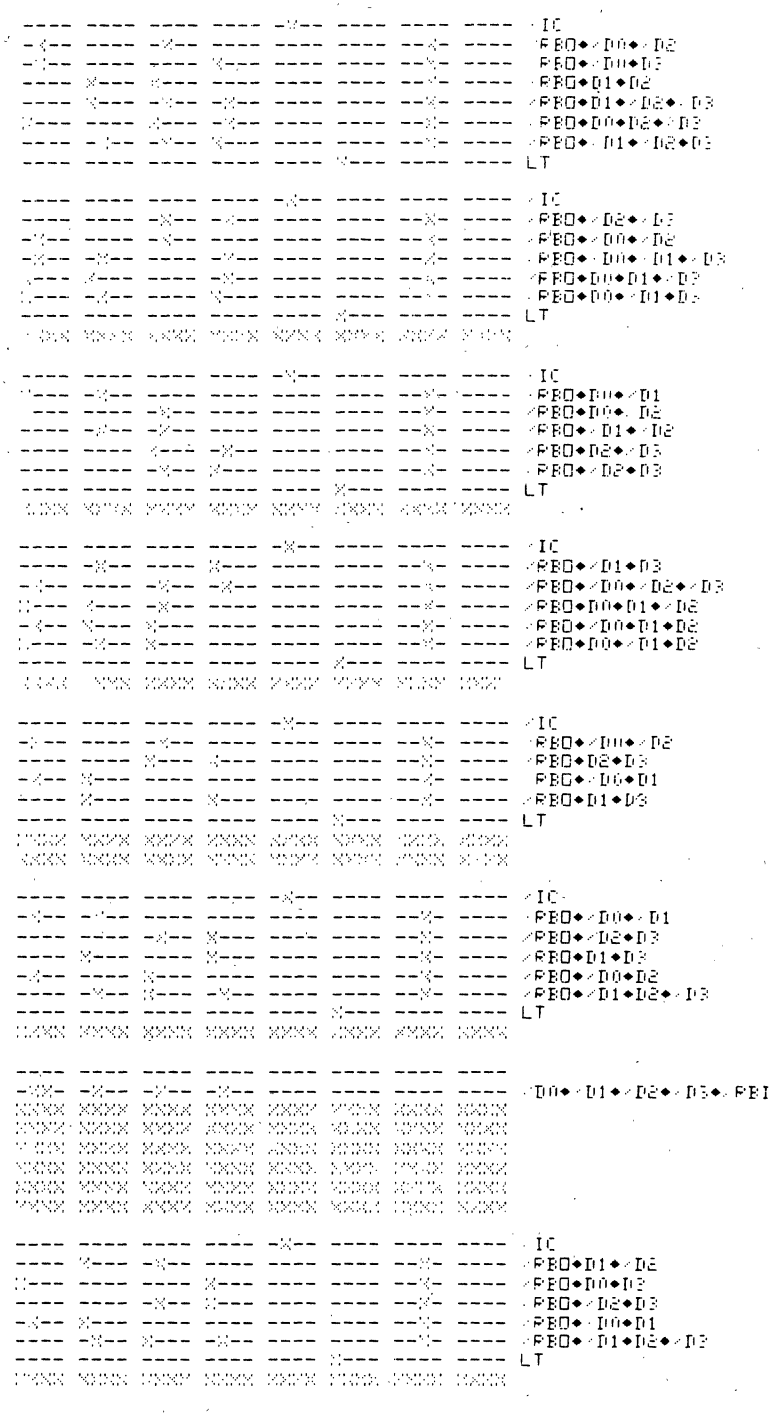
WHEN HIGH THE LAMP TEST INPUT (LT) WILL TURN ON THE DISPLAY.

INPUTS							OUTPUTS							
LT	IC	/RBI	D0	D1	D2	D3	A	B	C	D	E	F	G	/RBO
L	H	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	X
L	L	H	L	L	L	L	L	L	L	L	L	L	H	L
L	L	L	L	L	L	L	H	H	H	H	H	H	H	L
H	L	X	X	X	X	X	L	L	L	L	L	L	L	X

Hex Display Decoder-Driver, Design Specification.

Hex Decoder/7 Seg. Driver w/Ripple Blanking, Intensity Con., & Lamp Test

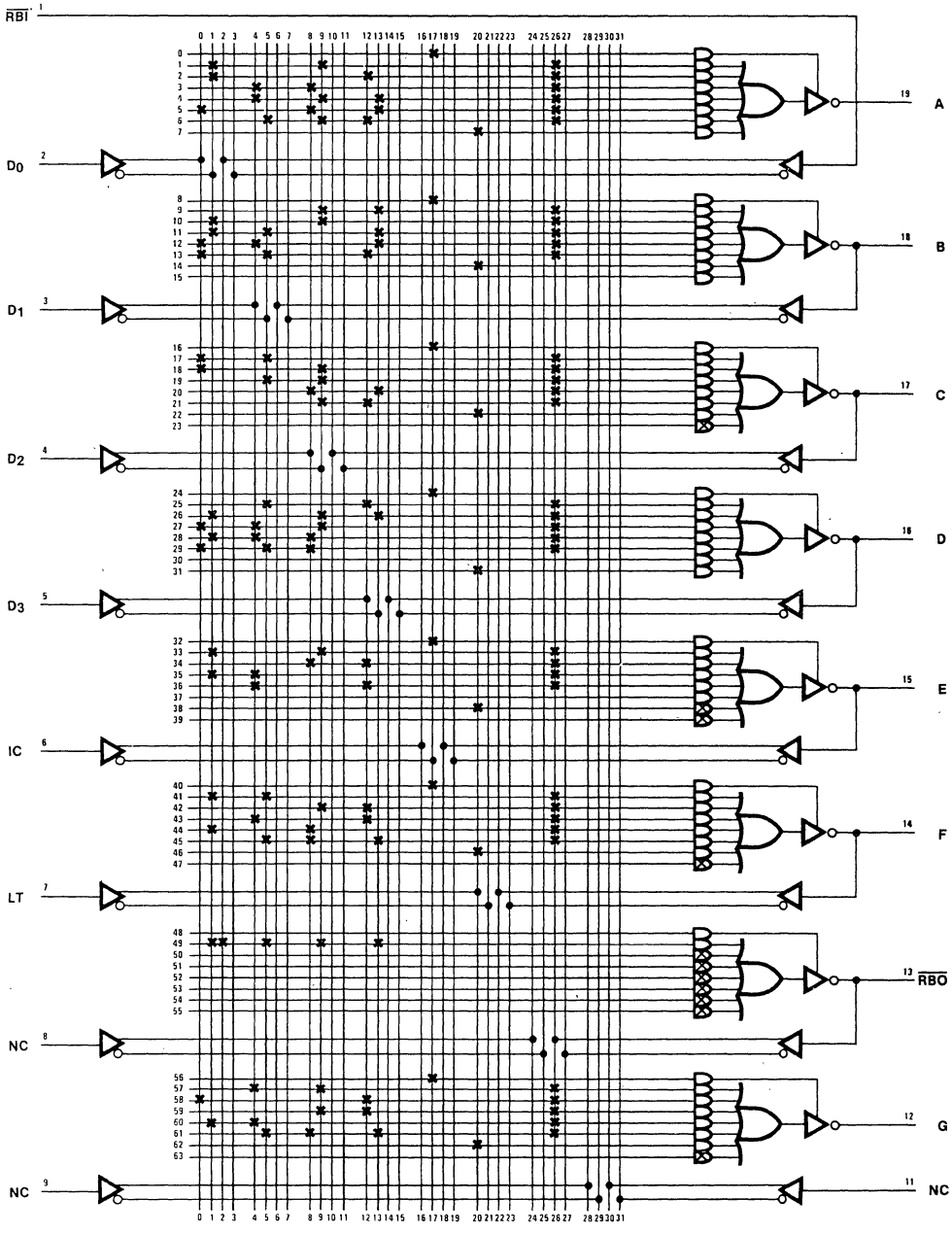
Fuse Pattern PAL16L8



Hex Display Decoder-Driver, Fuse Return

Hex Decoder/7 Seg. Driver w/Ripple Blanking, Intensity Con., & Lamp Test

Logic Diagram PAL16L8



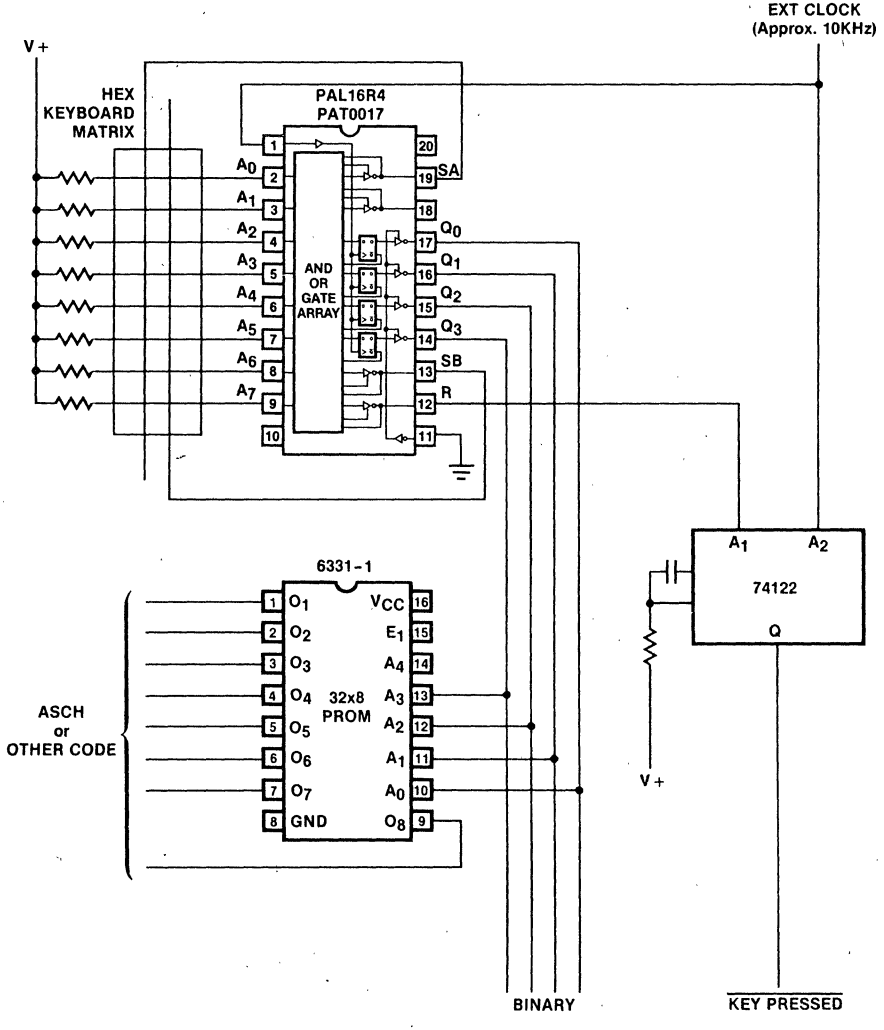
Hex Display Decoder-Driver, Coded PAL Logic Diagram.

HEXADECIMAL KEYBOARD SCANNER

The popularity of pocket calculators and home computers has created a large market for low-cost keyboards. The logic required to scan small keyboards is typically implemented either in SSI/MSI logic or in a computer-generated software scan. In the first case, the logic may be rather expensive; in the second case, if the microcomputer system is a busy one, the software scan may be unacceptably slow. A single PAL and just a few inexpensive parts can do the task.

Hex Keyboard Scanner

Logic Diagram PAL16L8

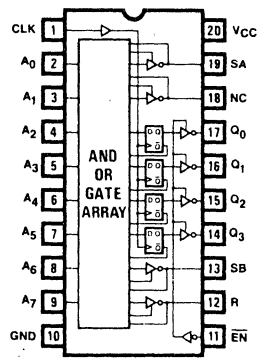


Hex Keyboard Scanner, Combinatorial Logic Diagram.

Hex Keyboard Scanner — Design Specification PAL16R4

```
PAL16R4                                                    PAL DESIGN SPECIFICATION
PAT0017
HEX KEYBOARD SCANNER

CLK A0 A1 A2 A3 A4 A5 A6 A7 GND /EN R SB Q3 Q2 Q1 Q0 NC SA VCC


IF ( VCC ) /SA = /Q3


IF ( VCC ) /NC  = /A0*/Q0*/Q1*/Q2 + /A1*Q0*/Q1*/Q2 +
                  /A2*/Q0*Q1*/Q2 + /A3*Q0*Q1*/Q2 +
                  /A4*/Q0*/Q1*Q2 + /A5*Q0*/Q1*Q2 +
                  /A6*/Q0*Q1*Q2

/Q0 := Q0*R + /Q0*/R

/Q1 := Q0*Q1*R + /Q0*/Q1*R + /Q1*/R

/Q2 := Q0*Q1*Q2*R+/Q0*/Q2*R + /Q1*/Q2*R + /Q2*/R

/Q3 := Q0*Q1*Q2*Q3*R + /Q0*/Q3*R + /Q1*/Q3*R + /Q2*/Q3*R + /Q3*/R

IF ( VCC ) /SB = Q3

IF ( VCC )  /R = /NC + /A7*Q0*Q1*Q2


DESCRIPTION:

    THE KEYBOARD SCANNER WILL SCAN A 16 KEY KEYBOARD ARRANGED IN A
2X8 MATRIX.  THE SCANNER WORKS BY SELECTING ONE ROW OF 8 SWITCHES
AND THEN SCANNING THE 8 INPUTS.  A LOW ON ANY INPUT WILL DISABLE THE CLOCK
GOING INTO THE ONE-SHOT.  THE ONE-SHOT IS USED AS A DELAY TO ALLOW THE
SWITCH BOUNCE TO SETTLE OUT.  AT THE END OF THE TIME DELAY (10MS), KEYPRESSED
WILL GO LOW.  THE OUTPUTS WILL THEN GIVE THE BINARY CODE FOR THE SWITCH
SELECTED.  WHEN THE SWITCH IS RELEASED, KEYPRESSED WILL GO HIGH, AND
SCANNING WILL CONTINUE.  WHEN THE END OF THE ROW IS REACHED, THE
SCANNER SWITCHES TO THE OTHER ROW AND CONTINUES SCANNING.
    THE EXTERNAL CLOCK SHOULD RUN IN THE RANGE OF 10 KHZ.
IF ASCII OR OTHER CODED CHARACTERS ARE DESIRED, THE BINARY CAN BE
 CONVERTED USING A PROM.
```

PAL16R4



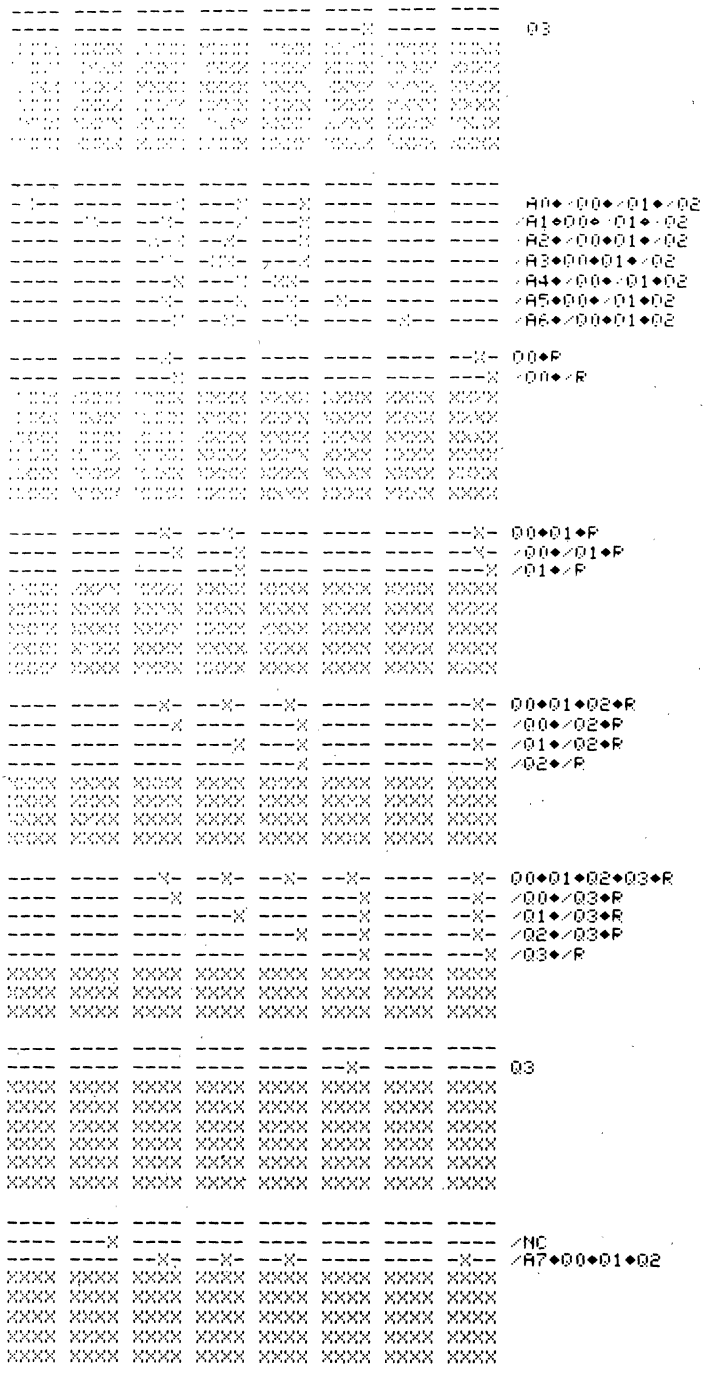
Logic Symbol

Hex Keyboard Scanner, Design Specification.

24

Hex Keyboard Scanner

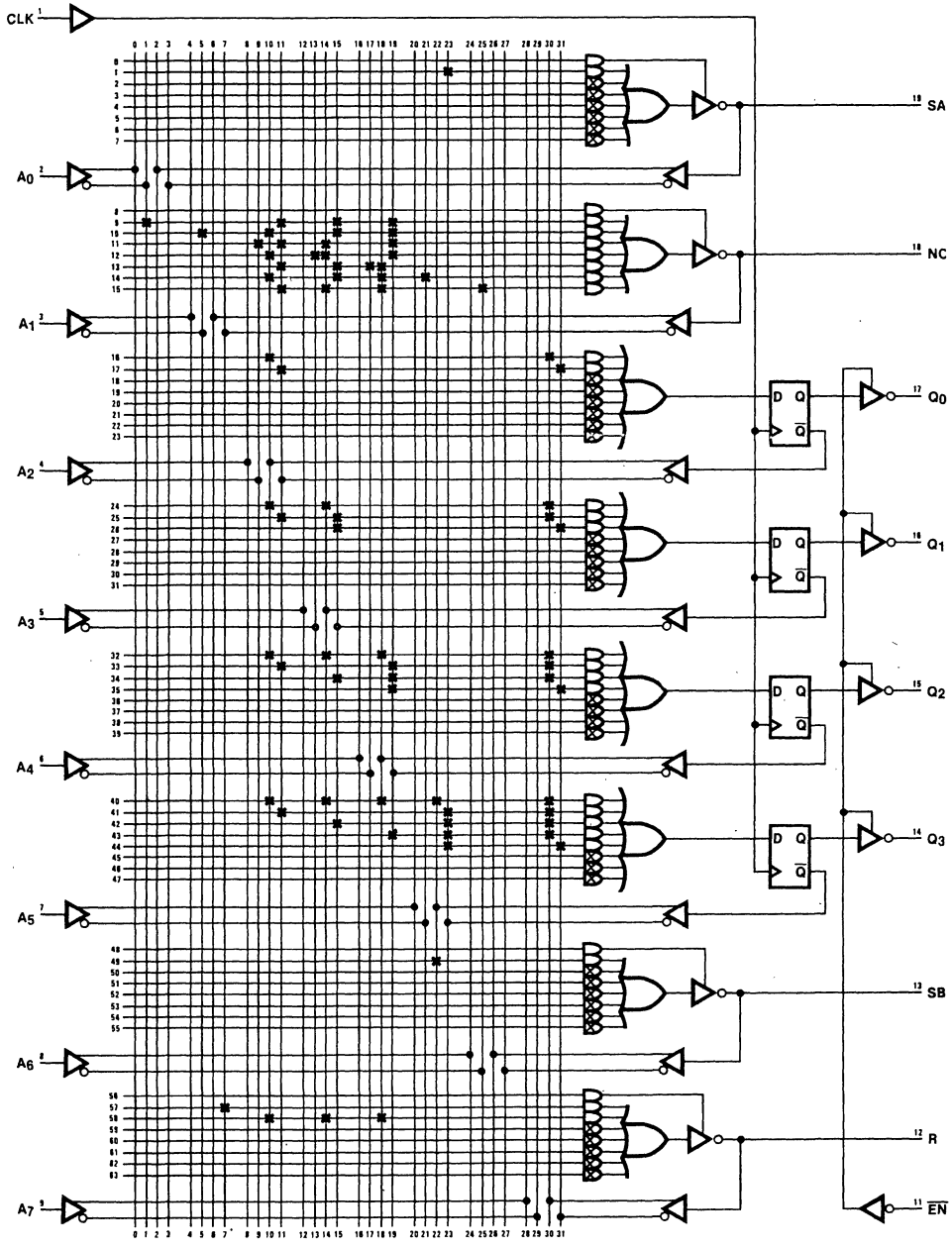
Fuse Pattern PAL16R4



Hex Keyboard Scanner, Fuse Return

Hex Keyboard Scanner

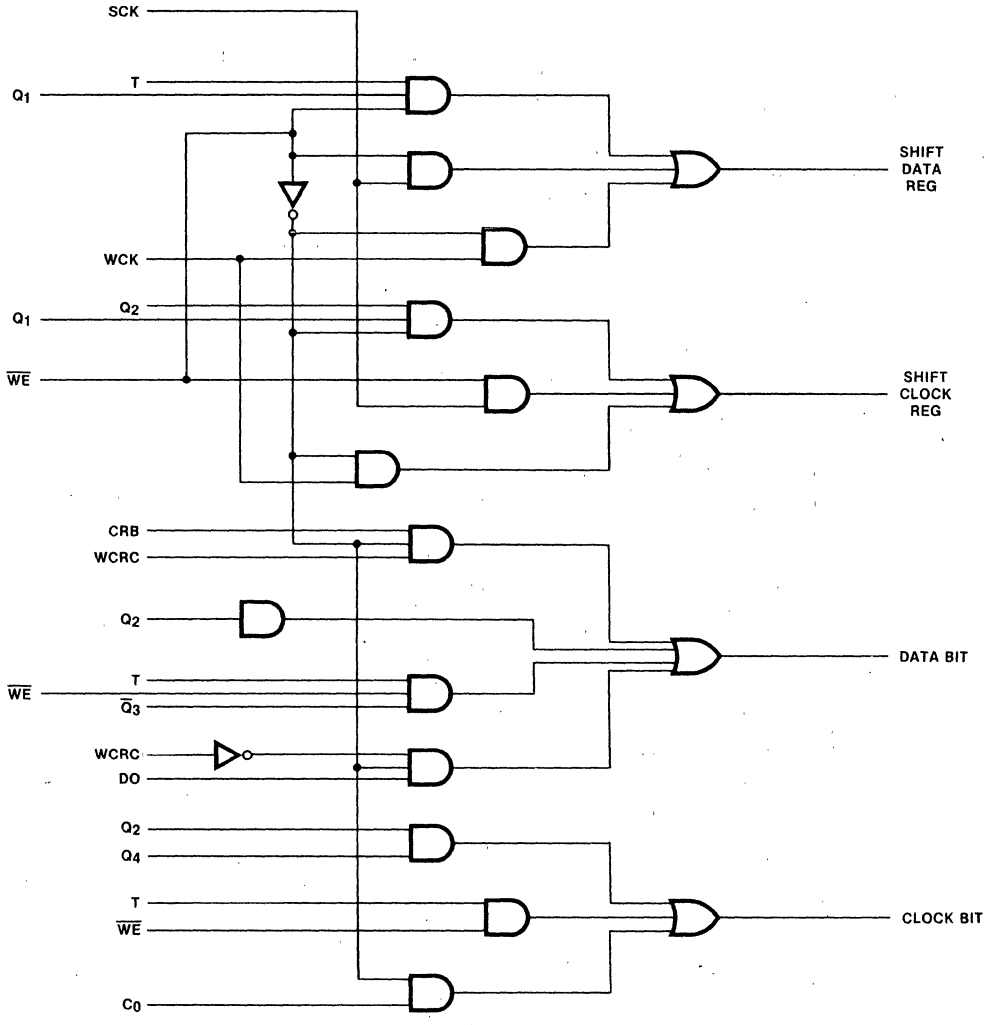
Logic Diagram PAL16R4



Hex Keyboard Scanner, Coded PAL Logic Diagram.

MINIDISKETTE CONTROL LOGIC

The flexible diskette (floppy), and its smaller brother, the minidiskette, are very popular as mass storage on small systems. Most of these small systems are destined for high-volume applications, so all possible production economies should be explored. The disk controller is the most complicated (and expensive) part of the disk subsystem; this example shows how a PAL can reduce the size and cost of the controller for a minidiskette-drive controller.



Minidiskette Control Logic Diagram.

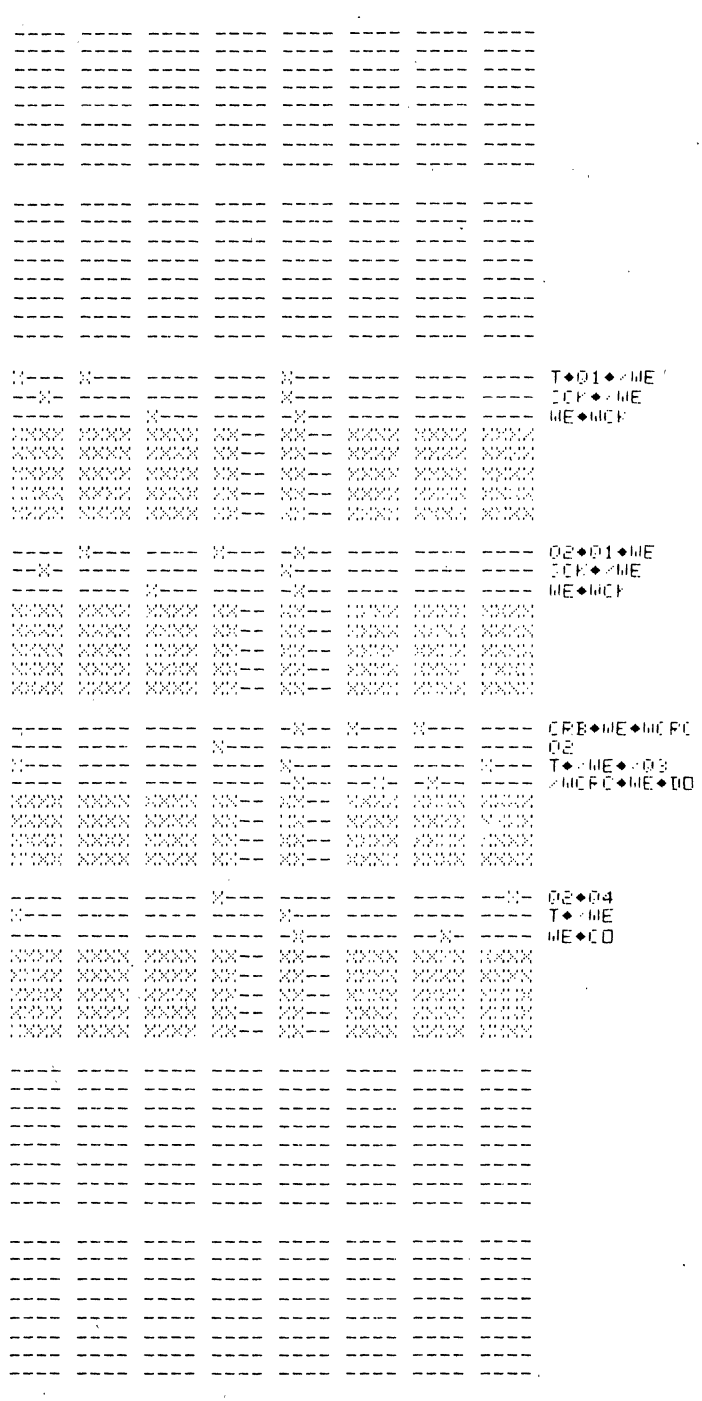
Portion of Micro Floppy Control Logic — Design Specification PAL14H4

```
PAL14H4                                                    PAL DESIGN SPECIFICATION
PAT0024
PORTION OF MICRO FLOPPY CONTROL LOGIC

SCK T 01 WCK 02 /WE CRB WCRC /03 GND 04 CO DO CKB DATABT SCREG SDREG NC 11 VCC


SDREG= T*01*/WE + SCK*/WE + WE*WCK

SCREG= 02*01*WE + SCK*/WE + WE*WCK

DATABT= CRB*WE*WCRC + 02 + T*/WE*/03 + /WCRC*WE*DO

CKB= 02*04 + T*/WE + WE*CO


DESCRIPTION:

   PORTION OF FLOPPY DISC CONTROL LOGIC
```

Minidiskette Control Logic Design Specification.

Portion of Micro Floppy Control Logic

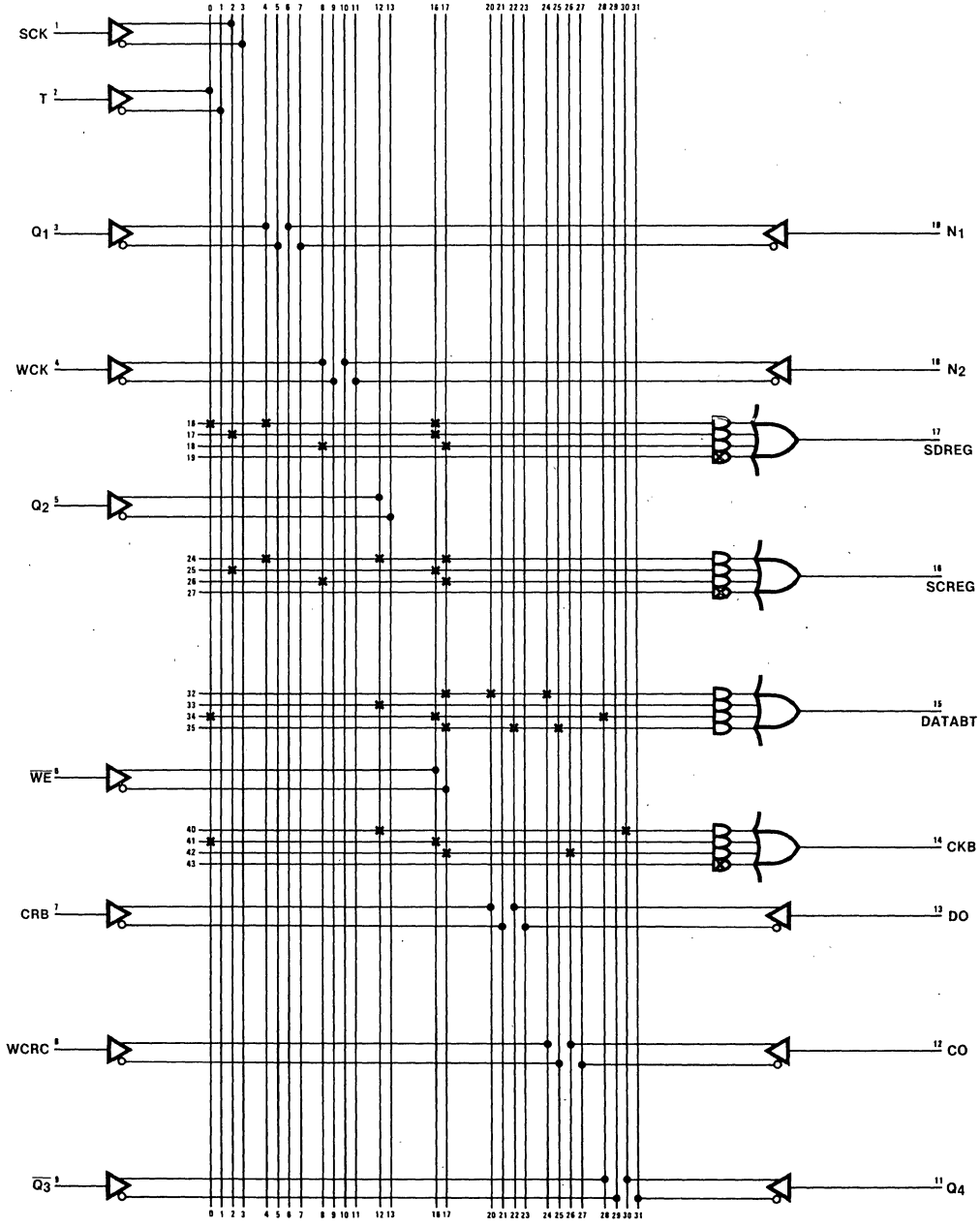
Fuse Pattern PAL14H4



Minidiskette Control Logic, 14H4 Fuse Pattern.

Portion of Micro Floppy Control Logic

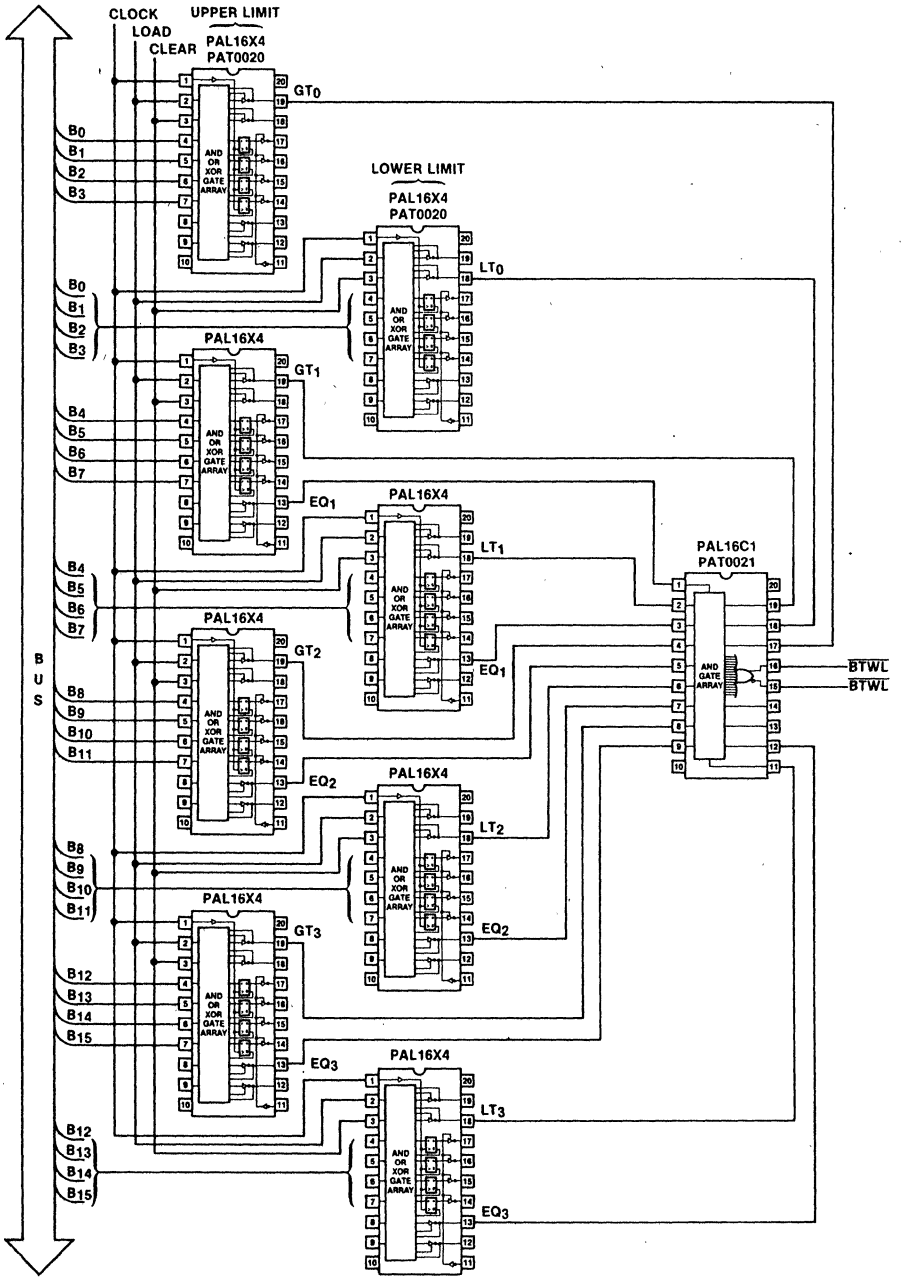
Logic Diagram PAL14H4



Minidiskette Control Logic, Coded 14H4 PAL Logic Diagram.

BETWEEN LIMITS COMPARATOR/ REGISTER

It is often needed to keep data between limits as it is processed, or to halt a process when limits are reached. This may be done for system security, or as a means of self-checking. The checker described here might search for a specific value, search for missing values: values either in or out of a certain range. The sample circuit shown monitors a 16-bit bus, using two PAL types, and latches a complementary pair of BTWL status signals into its output registers.

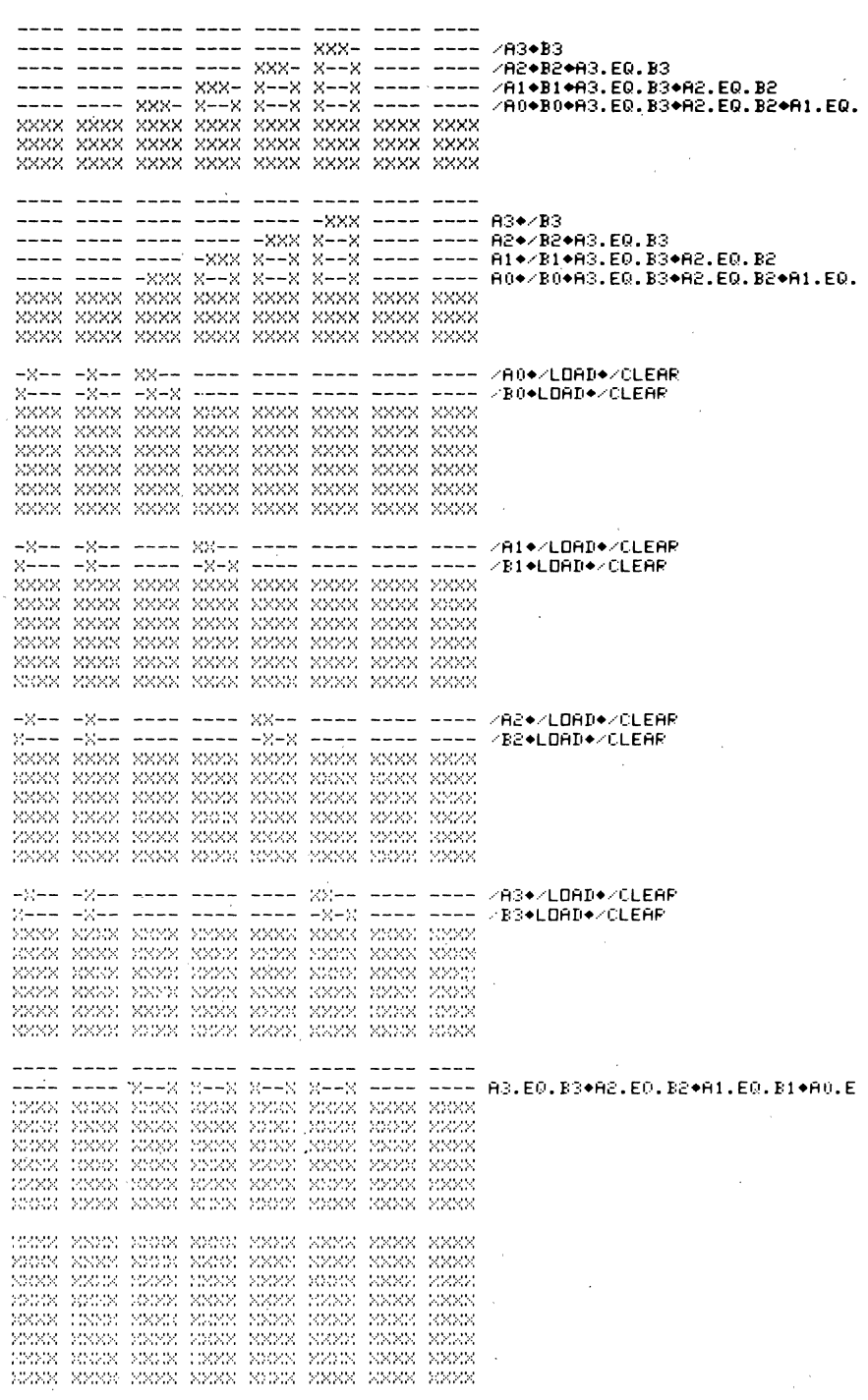


Limit Checker Combinatorial Logic Diagram.

```
PAL16X4                                          PAL DESIGN SPECIFICATION
PATTERN
BETWEEN LIMITS COMPARATOR   REGISTER

CK LOAD CLEAR B0 B1 B2 B3 NC NC GND /E NC /EO A3 A2 A1 A0 /LT /GT VCC


IF(VCC) LT = (A3*/B3) +
             (A2* B2) * (A3.EO.B3) +
             (A1* B1) * (A3.EO.B3) * (A2.EO.B2) +
             (A0*/B0) * (A3.EO.B3) * (A2.EO.B2) * (A1.EO.B1)

IF(VCC) GT = (/A3*B3) +
             (/A2*B2) * (A3.EO.B3) +
             (/A1*B1) * (A3.EO.B3) * (A2.EO.B2) +
             (/A0*B0) * (A3.EO.B3) * (A2.EO.B2) * (A1.EO.B1)



        A0 := (/A0* LOAD* CLEAR + (/B0*LOAD*/CLEAR

        A1 := (/A1*/LOAD*/CLEAR + (/B1*LOAD*/CLEAR

        A2 := (/A2*/LOAD*/CLEAR + (/B2*LOAD*/CLEAR

        A3 := (/A3*/LOAD*/CLEAR + (/B3*LOAD*/CLEAR



IF(VCC) EO = (A3.EO.B3) * (A2.EO.B2) * (A1.EO.B1) * (A0.EO.B0)



DESCRIPTION:

THE DEVICE CONTINUOUSLY COMPARES THE VALUE OF BUS, B, WITH THE VALUE OF
REGISTER A AND REPORTS THE STATUS ON OUTPUTS GT, LT, AND EQ.  GT INDICATES
THAT B IS GTEATER THAN A.  LT INDICATES THAT B IS LESS THAN A.  EQ
INDICATES THAT A IS EQUAL TO B.  THE VALUE OF REGISTER A
MAY READ BY LOWERING ENABLE LINE, /E.  REGISTER A IS LOADED
WITH THE VALUE ON BUS, B, WHEN THE LOAD LINE IS HIGH AND THE CLEAR LINE
IS LOW ON THE LOW TO HIGH TRANSITION OF THE CLOCK.


-------------------------------------------------
! LOAD ! CLEAR ! CLOCK ! REGISTER A ! OPERATION !
-------------------------------------------------
!   L  !   L   !  L-H  !      A      ! NOP       !
!   X  !   H   !  L-H  !   ALL HIGH  ! CLEAR     !
!   H  !   L   !  L-H  !      B      ! LOAD B    !
-------------------------------------------------
```

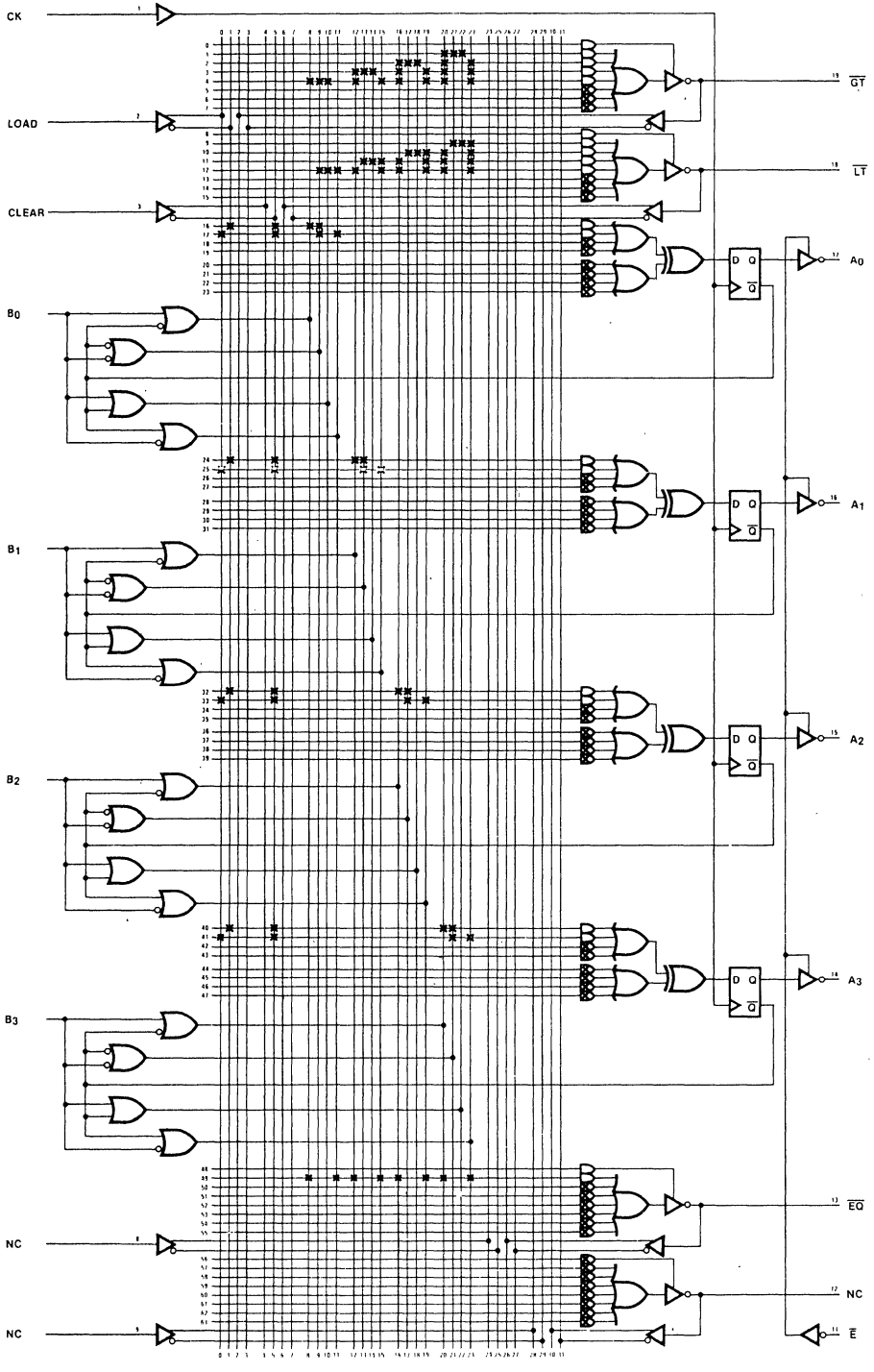
PAL16X4 Limit Checker Design Specification.

Between Limits Comparator/Register — Fuse Pattern PAL16X4



PAL16X4 Limit Checker Fuse Pattern.

Between Limits Comparator/Register — Logic Diagram PAL16X4

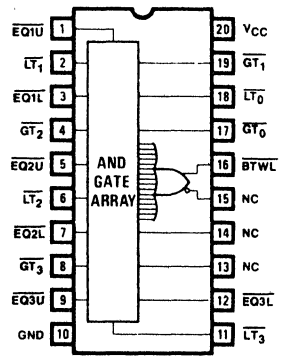


PAL16X4 Limit Checker Coded Logic Diagram.

Between Limits Comparator/Logic — Design Specification PAL16C1

```
PAL16C1                                                PAL DESIGN SPECIFICATION
PAT0021
BETWEEN LIMITS COMPARATOR / LOGIC

/EQ1U /LT1 /EQ1L /GT2 /EQ2U /LT2 /EQ2L /GT3 /EQ3U GND
/LT3 /EQ3L NC NC NC /BTWL /GT0 /LT0 /GT1 VCC


/BTWL = GT3 + GT2*EQ3U + GT1*EQ3U*EQ2U + GT0*EQ3U*EQ2U*EQ1U +

        LT3 + LT2*EQ3L + LT1*EQ3L*EQ2L + LT0*EQ3L*EQ2L*EQ1L


DESCRIPTION:

THE BETWEEN LIMITS LOGIC DETERMINES THE BTWL STATUS AS
A FUNCTION OF THE GT, LT AND EQ STATUS FROM THE COMPARATOR
REGISTERS.
```

PAL16C1

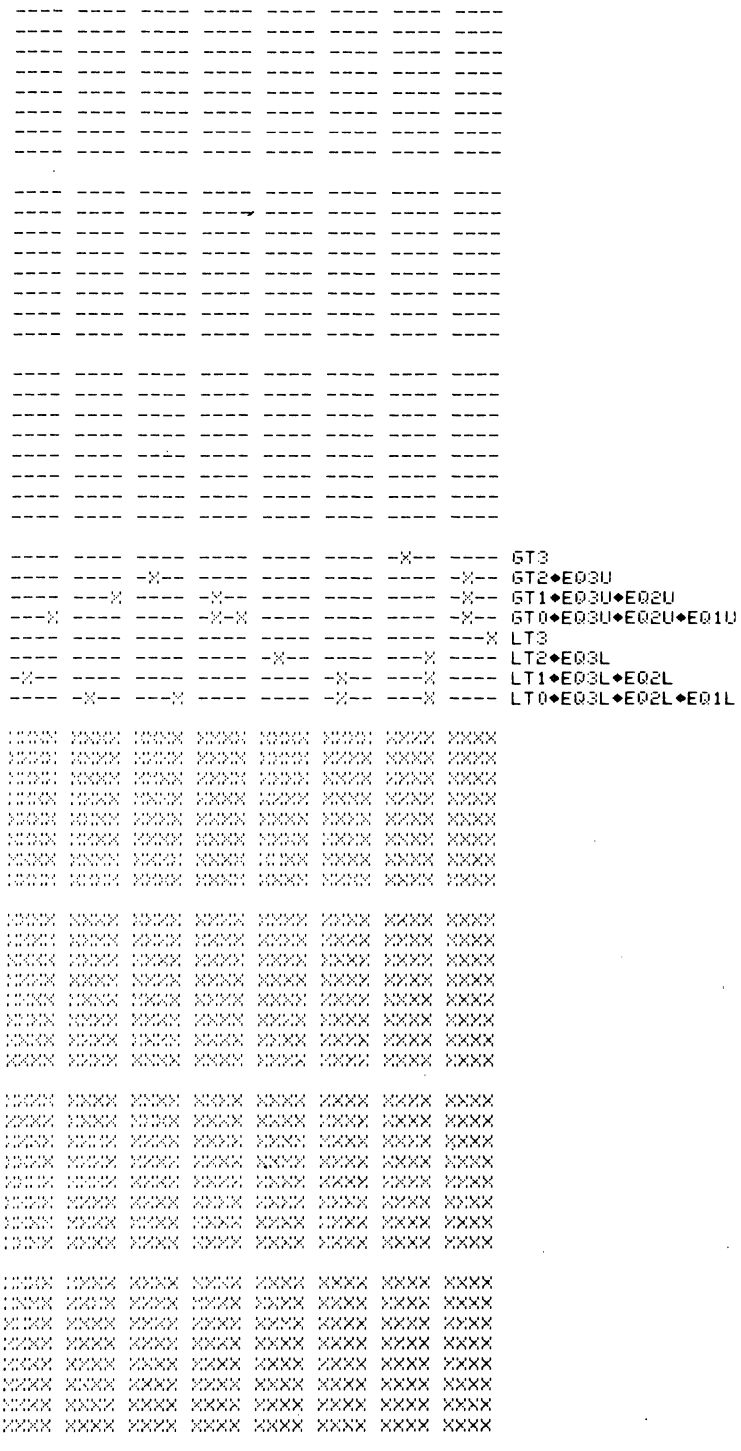


Logic Symbol

PAL16C1 Limit Checker Design Specification.

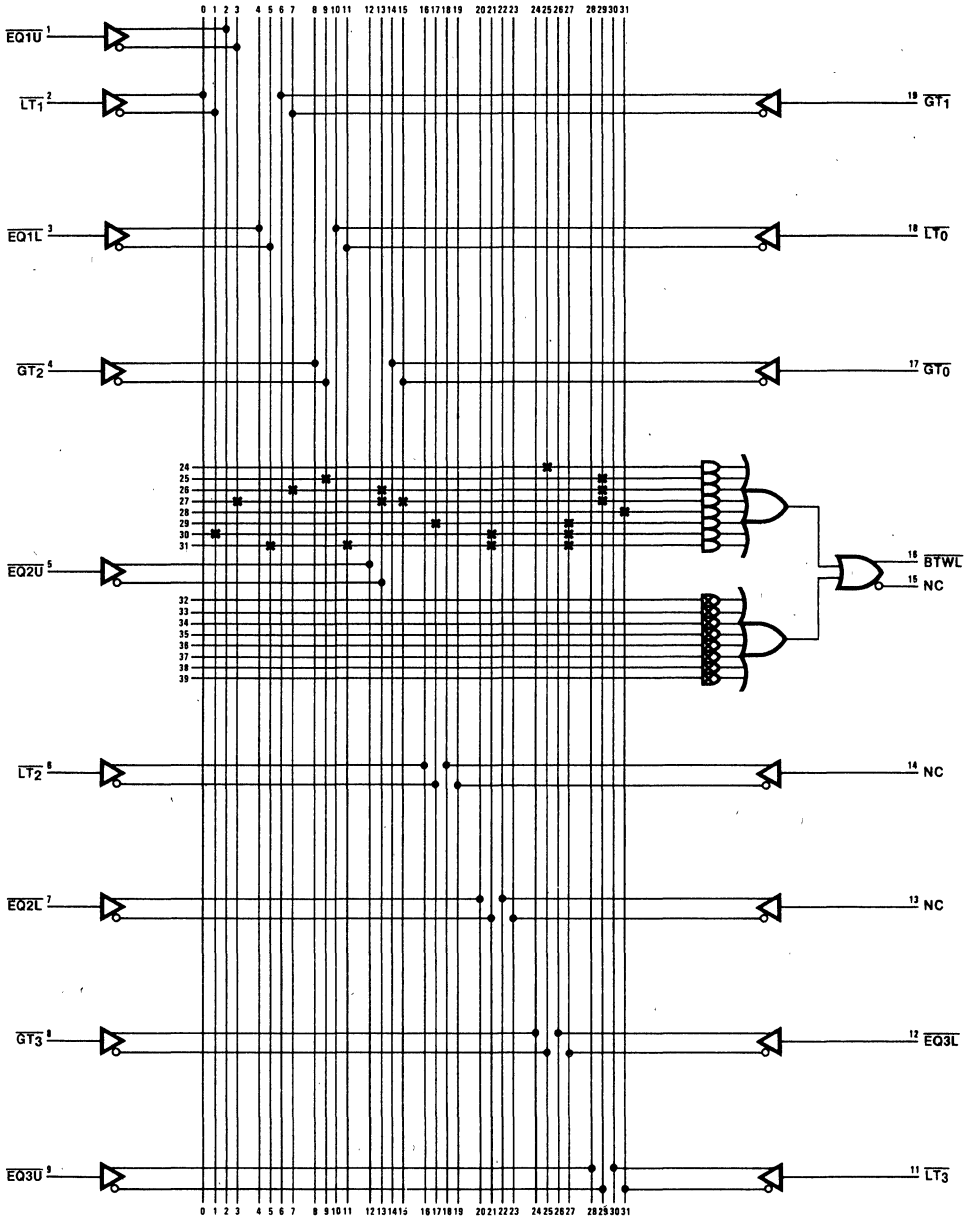
Between Limits/Comparator/Logic

Fuse Pattern PAL16C1



PAL16C1 Limit Checker Fuse Pattern.

Between Limits Comparator/Logic — Logic Diagram PAL16C1



PAL16C1 Limit Checker Coded Logic Diagram.

8-BIT I/O PRIORITY INTERRUPT ENCODER WITH REGISTERS

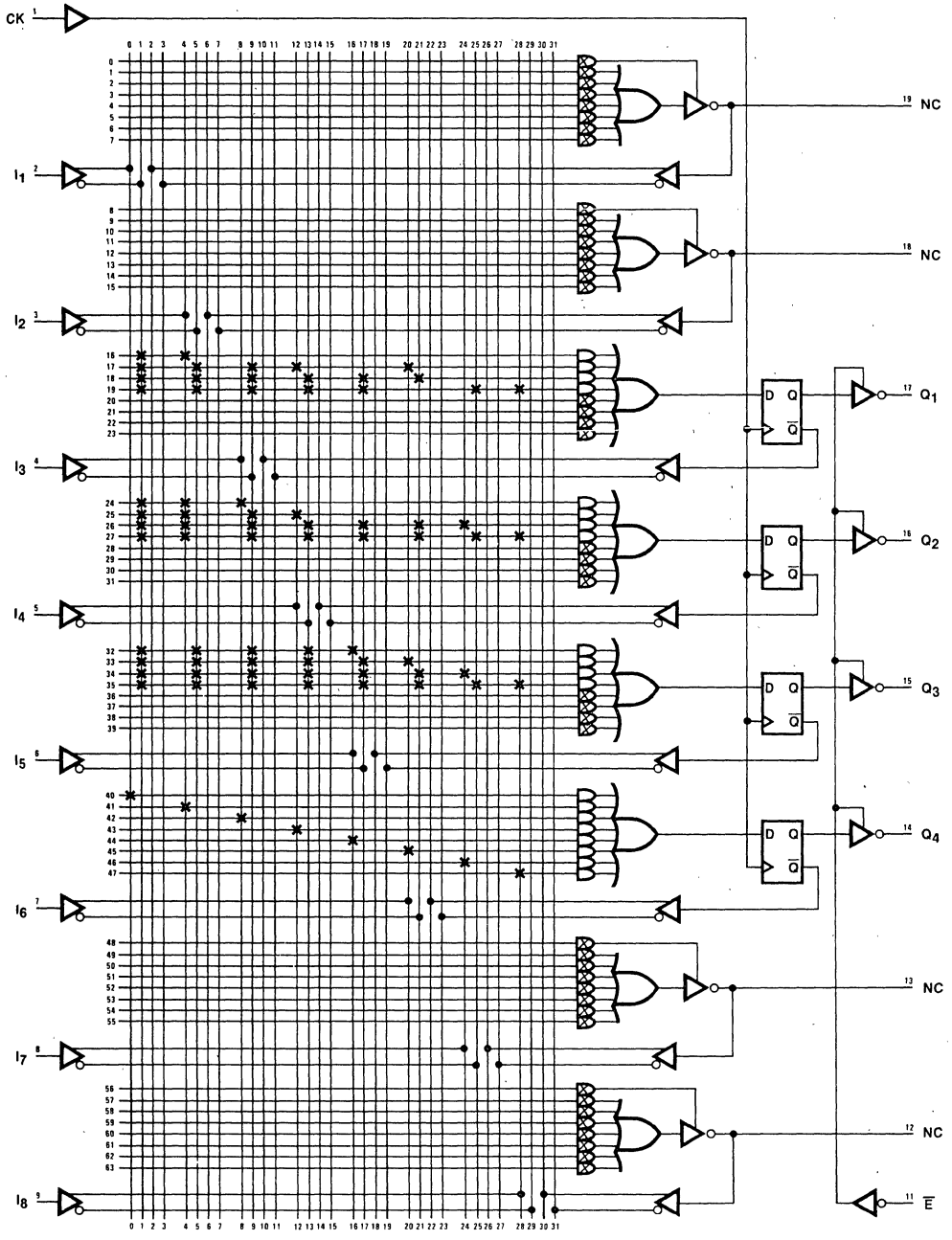
Design Specification PAL16R4

```
PAL16R4                                                PAL DESIGN SPECIFICATION
PAT0005
8 BIT I/O PRIORITY INTERRUPT ENCODER WITH REGISTERS

CK I1 I2 I3 I4 I5 I6 I7 I8 GND /E NC NC 04 03 02 01 NC NC VCC


/01 := /I1*I2 + /I1*/I2*/I3*I4 + /I1*/I2*/I3*/I4*/I5*I6 +
       /I1*/I2*/I3*/I4*/I5*/I6*/I7*I8

/02 := /I1*/I2*I3 + /I1*/I2*/I3*I4 + /I1*/I2*/I3*/I4*/I5*/I6*I7 +
       /I1*/I2*/I3*/I4*/I5*/I6*/I7*I8

/03 := /I1*/I2*/I3*/I4*I5 + /I1*/I2*/I3*/I4*/I5*I6 +
       /I1*/I2*/I3*/I4*/I5*/I6*I7 + /I1*/I2*/I3*/I4*/I5*/I6*/I7*I8

/04 := I1+I2+I3+I4+I5+I6+I7+I8


DESCRIPTION:
    THE I/O PRIORITY INTERRUPT ENCODER PRIORITIZES 8 I/O LINES
(I1 THRU I8) OUTPUTING 111 (03,02,01 RESPECTIVELY) FOR THE HIGHEST
PRIORITY I/O DEVICE (I1) AND 000 FOR AN INTERRUPT FROM THE LOWEST
PRIORITY I/O DEVICE (I8).  OUTPUT 04 SERVES AS THE INTERRUPT FLAG
AND GOES LOW WHEN ANY OF THE 8 I/O INPUTS GO HIGH.  THE PRIORITY
INTERRUPT ENCODER REGISTERS ARE UPDATED ON THE RISING EDGE OF THE
CLOCK INPUT (CK).  THE 3-STATE OUTPUTS ARE HIGH-Z WHEN THE ENABLE
LINE (/E) IS HIGH AND ENABLED WHEN THE ENABLED LINE (/E) IS LOW.


 TRUTH TABLE

 ----------------------------
 /  I  I  I  I  I  I  I  I    0  0  0  0
 E  8  7  6  5  4  3  2  1    4  3  2  1
 ----------------------------
 H  X  X  X  X  X  X  X  X    Z  Z  Z  Z
 L  X  X  X  X  X  X  X  H    L  H  H  H
 L  X  X  X  X  X  X  H  L    L  H  H  L
 L  X  X  X  X  X  H  L  L    L  H  L  H
 L  X  X  X  X  H  L  L  L    L  H  L  L
 L  X  X  X  H  L  L  L  L    L  L  H  H
 L  X  X  H  L  L  L  L  L    L  L  H  L
 L  X  H  L  L  L  L  L  L    L  L  L  H
 L  H  L  L  L  L  L  L  L    L  L  L  L
 L  L  L  L  L  L  L  L  L    H  H  H  H
```

Eight-Bit Priority Interrupt Encoder with Registers, Designs Specification.

8 Bit I/O Priority Interrupt Encoder with Registers

Design Specification PAL16R4



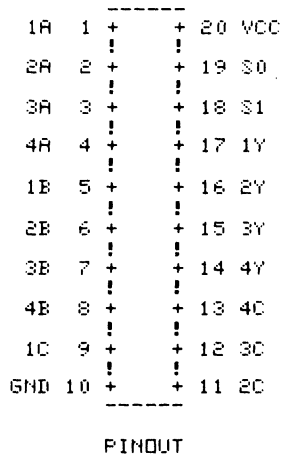
PAL16R4 Eight-Bit Priority Interrupt Encoder with Registers, Coded Logic Diagram.

QUADRUPLE 3-LINE/1-LINE DATA SELECTOR MULTIPLEXER

Design Specification PAL14H4

```
PAL14H4                                              PAL DESIGN SPECIFICATION
PAT0016
QUADRUPLE 3-LINE-TO-1-LINE DATA SELECTOR MULTIPLEXER

1A 2A 3A 4A 1B 2B 3B 4B 1C GND 2C 3C 4C 4Y 3Y 2Y 1Y S1 S0 VCC



 1Y = 1A*/S0*/S1 + 1B*S0*/S1 + 1C*/S0*S1

 2Y = 2A*/S0*/S1 + 2B*S0*/S1 + 2C*/S0*S1

 3Y = 3A*/S0*/S1 + 3B*S0*/S1 + 3C*/S0*S1

 4Y = 4A*/S0*/S1 + 4B*S0*/S1 + 4C*/S0*S1


DESCRIPTION:

    A 4-BIT WORD IS SELECTED FROM ONE OF THREE SOURCES AND IS ROUTED
TO THE FOUR OUTPUTS.  TRUE DATA IS PRESENTED AT THE OUTPUTS.  IF
INVERTED DATA IS DESIRED, USE THE SAME EQUATIONS WITH THE PAL14L4.
```

S0	S1	OUTPUTS
L	L	A DATA
H	L	B DATA
L	H	C DATA
H	H	LOW

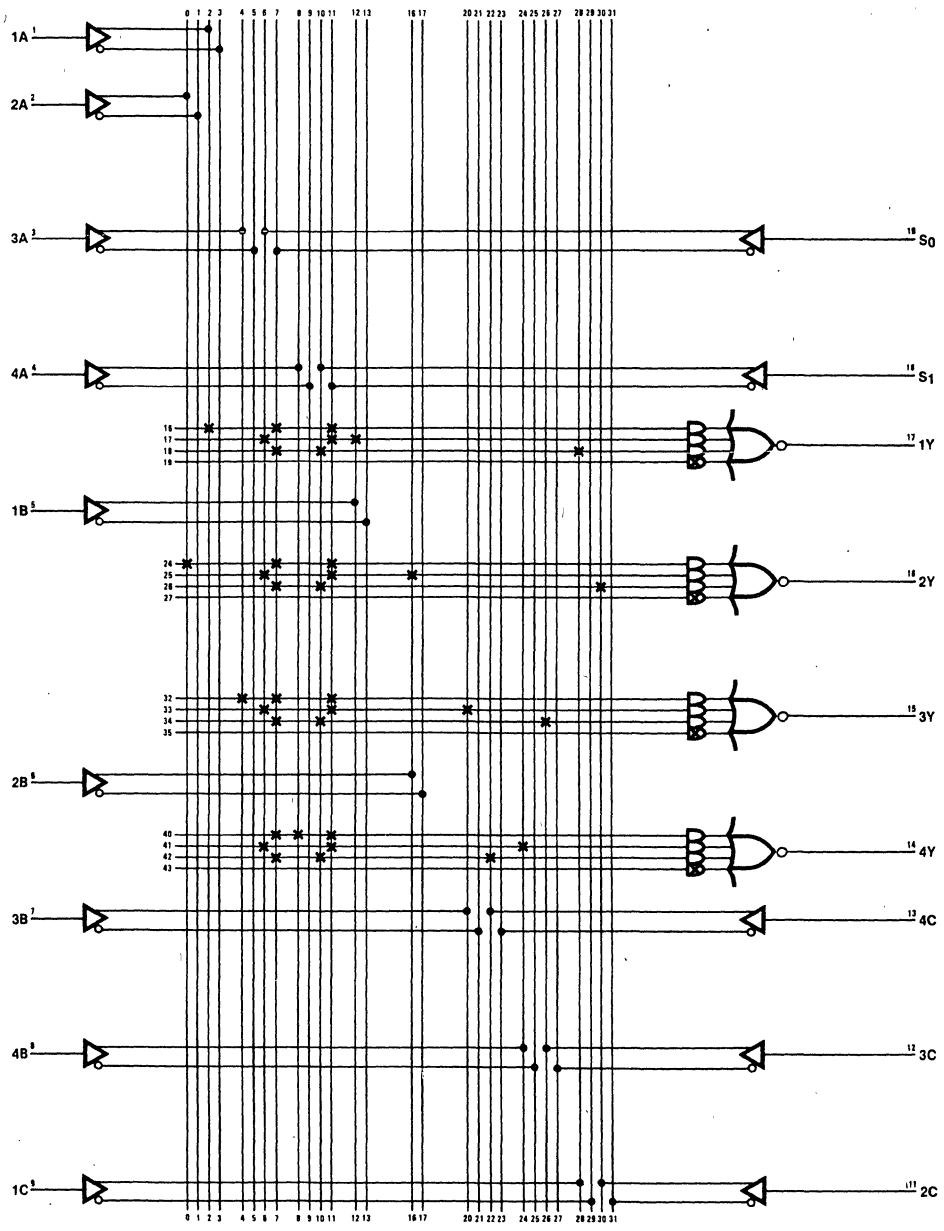


PINOUT

Quad 3-to-1 Data Selector-Multiplexer, Design Specification.

Quadruple 3-Line/1-Line Data Selector Multiplexer

Logic Diagram PAL14H4



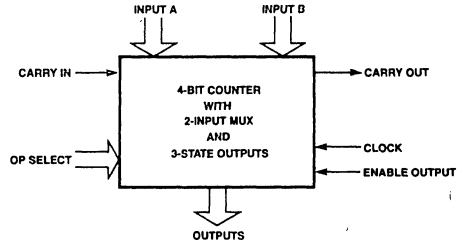
PAL14H4 Quad 3-to-1 Data Selector Multiplexer, Coded Logic Diagram

4-BIT COUNTER WITH 2 INPUT MUX

Design Specification PAL16R4

```
PAL16R4                                                    PAL DESIGN SPECIFICATION
PAT0034
4-BIT COUNTER WITH 2 INPUT MUX

CLOCK A0 A1 A2 A3 B0 B1 B2 B3 GND /E COUT I1 03 02 01 00 I0 CIN VCC


/Q0 := /I1*/I0*/Q0 + /I1*I0*/A0 + I1*/I0*/B0 +  I1*I0*/CIN*/Q0 +
       I1*I0*CIN*Q0

/Q1 := /I1*/I0*/Q1 + /I1*I0*/A1 + I1*/I0*/B1 +  I1*I0*/CIN*/Q1 +
       I1*I0*CIN*Q1*Q0 + I1*I0*/Q1*/Q0

/Q2 := /I1*/I0*/Q2 + /I1*I0*/A2 + I1*/I0*/B2 +  I1*I0*/CIN*/Q2 +
       I1*I0*CIN*Q2*Q1*Q0 + I1*I0*/Q2*/Q1 +I1*I0*/Q2*/Q0

/Q3 := /I1*/I0*/Q3 + /I1*I0*/A3 + I1*/I0*/B3 +  I1*I0*/CIN*/Q3 +
       I1*I0*CIN*Q3*Q2*Q1*Q0 + I1*I0*/Q3*/Q2 + I1*I0*/Q3*/Q1 + I1*I0*/Q3*/Q0


IF(VCC) /COUT = /CIN + /Q3 + /Q2 + /Q1 + /Q0


DESCRIPTION:

THE 4-BIT COUNTER LOADS A OR B FROM THE MUX, OR COUNTS UP.
THE THREE STATE OUTPUTS ARE ACTIVE WHEN /E IS LOW.
```

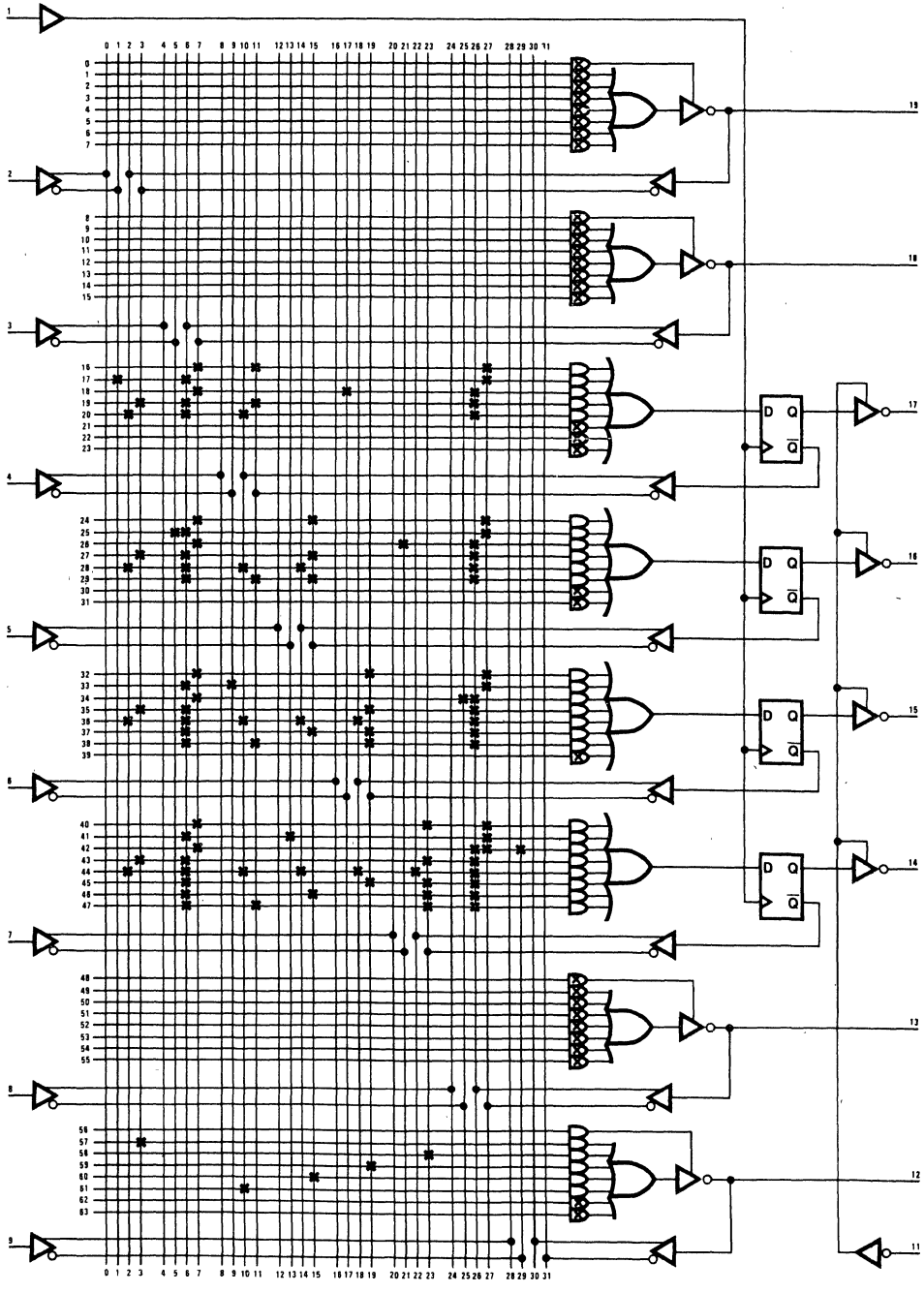
/E	I1	I0	CIN	CLOCK	OUTPUT Q	OPERATION
L	L	L	X	L-H	Q	NOP
L	L	H	X	L-H	A	LOAD A
L	H	L	X	L-H	B	LOAD B
L	H	H	L	L-H	Q	NOP
L	H	H	H	L-H	Q PLUS 1	INCREMENT



Four-Bit Counter with Two-Input Multiplex, Design Specification.

4-Bit Counter with 2 Input Mux

Logic Diagram PAL16R4



PAL16R4 Four-bit Counter with Two-Input Multiplex, Coded Logic Diagram.

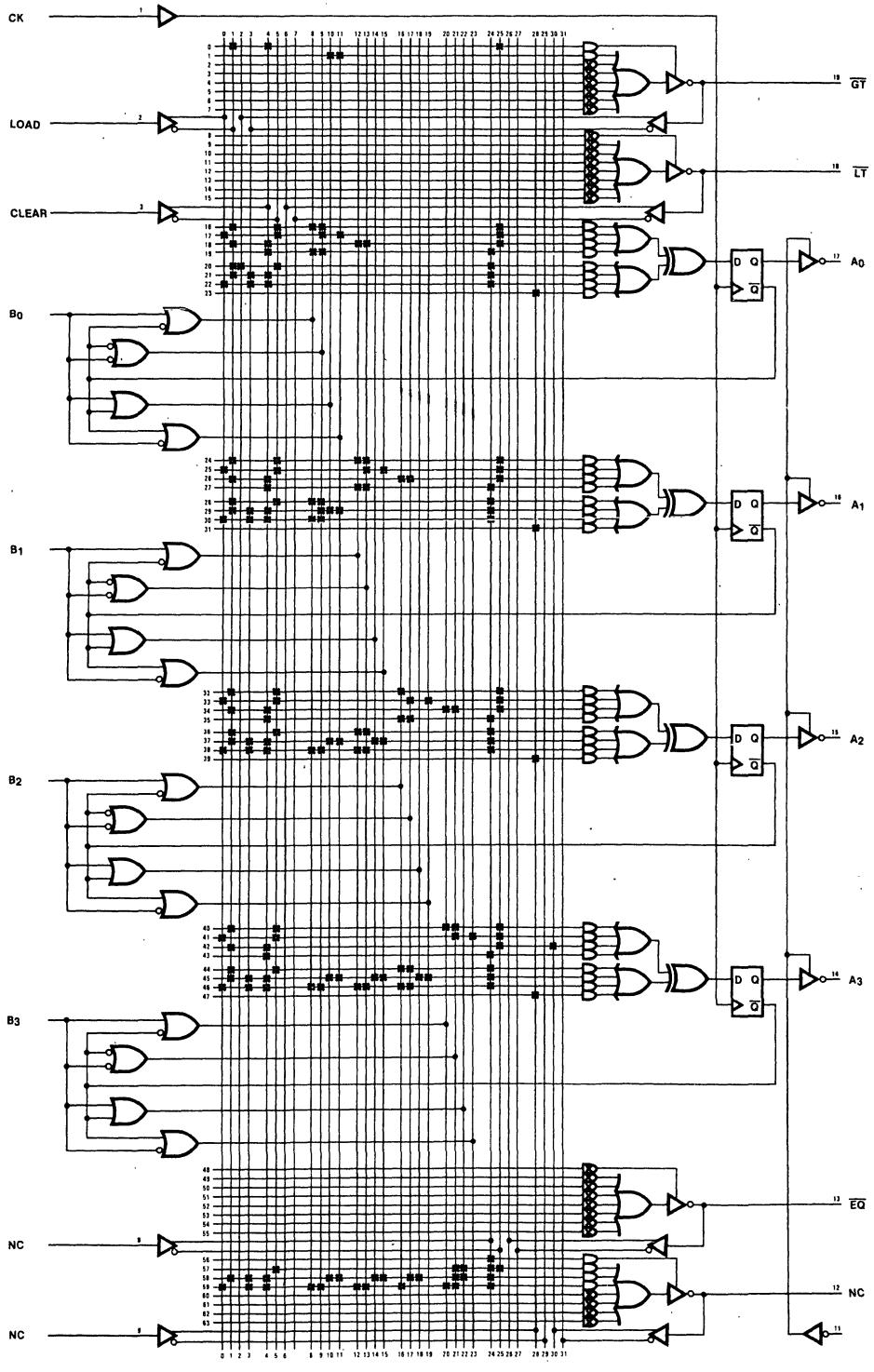
4-BIT UP/DOWN COUNTER WITH SHIFT AND THREE-STATE OUTPUTS

Design Specification PAL16X4

```
PAL16X4                                                    PAL DESIGN SPECIFICATION
PAT0026
4 BIT UP/DOWN COUNTER WITH SHIFT AND THREE-STATE OUTPUTS

CLOCK I0 I1 B0 B1 B2 B3 I2 CLEAR GND /E /LIO NC A3 A2 A1 A0 NC  RIO VCC


IF( /I2*I1*/I0 + RIO = /A0)


/A0 := (/A0)*/I2*/I1*/I0 + (/B0)*/I2*/I1*I0 + (/A1)*/I2*I1*/I0 + (/A0)*I2*I1
      :+: /RIO*I2*/I1*/I0 +
          RIO*I2*I1*/I0 +
          RIO*I2*I1* I0 + CLEAR


/A1 := (/A1)*/I2*/I1*/I0 + (/B1)*/I2*/I1*I0 + (/A2)*/I2*I1*/I0 + (/A1)*I2*I1
      :+: (/A0)*I2*/I1*/I0 +
          ( A0)*RIO*I2*I1*/I0 +
          (/A0)*RIO*I2*I1* I0 + CLEAR


/A2 := (/A2)*/I2*/I1*/I0 + (/B2)*/I2*/I1*I0 + (/A3)*/I2*I1*/I0 + (/A2)*I2*I1
      :+: (/A1)*I2*/I1*/I0 +
          ( A1)*( A0)*RIO*I2*I1*/I0 +
          (/A1)*(/A0)*RIO*I2*I1* I0 + CLEAR


/A3 := (/A3)*/I2*/I1*/I0 + (/B3)*/I2*/I1*I0 + /LIO*/I2*I1*/I0 + (/A3)*I2*I1
      :+: (/A2)*I2*/I1*/I0 +
          ( A2)*( A1)*( A0)*RIO*I2*I1*/I0 +
          (/A2)*(/A1)*(/A0)*RIO*I2*I1* I0 + CLEAR


IF( I2 )  LIO = (A3)*I2*/I1*/I2 + ( A3)*( A2)*( A1)*( A0)*RIO*I2*I1*/I0 +
                                  (/A3)*(/A2)*(/A1)*(/A0)*RIO*I2*I1* I0


DESCRIPTION:
THE UP/DOWN COUNTER WITH SHIFT WILL LOAD, SHIFT, COUNT UP, COUNT DOWN,
CLEAR OR NOP ON THE RISING EDGE OF THE CLOCK AS SPECIFIED BY THE
INSTRUCTION, I.  SHIFT I/O, CARRY AND BORROW SHARE THE SAME I/O LINES
(LIO AND RIO).  ACTIVE HIGH OUTPUTS, A, ARE ENABLED WHEN /E IS
LOW.  NOTE:  THE IMPLIED EXCLUSIVE OR, :+: , MUST BE PLACED BETWEEN
THE FOURTH AND FIFTH PRODUCT TERMS.
```

INPUTS							OUTPUTS						
CLEAR	I2	I1	I0	LIO	RIO	CLOCK	LIO	A3 A2 A1 A0				RIO	OPERATION
L	L	L	L	X	X	L-H	Z	A3	A2	A1	A0	Z	NOP
L	L	L	H	X	X	L-H	Z	B3	B2	B1	B0	Z	LOAD B
L	L	H	L	RI	Z	L-H	Z	RI	A3	A2	A1	A1	SHIFT RT
L	L	H	H	X	X	L-H	Z	ALL HIGH				Z	SET
L	H	L	L	Z	LI	L-H	A2	A2	A1	A0	LI	Z	SHIFT LT
L	H	L	H	Z	X	L-H	L	ALL HIGH				Z	SET
L	H	H	L	Z	CIN	L-H	COUT	A PLUS ONE				Z	INC IF CIN
L	H	H	H	Z	BIN	L-H	BOUT	A MINUS ONE				Z	DEC IF BIN
H	X	X	X	X	X	L-H	Z	ALL LOW				Z	CLEAR

Four-Bit Up/Down Counter with Shift and TRI-STATE (R) Outputs, Design Specification.



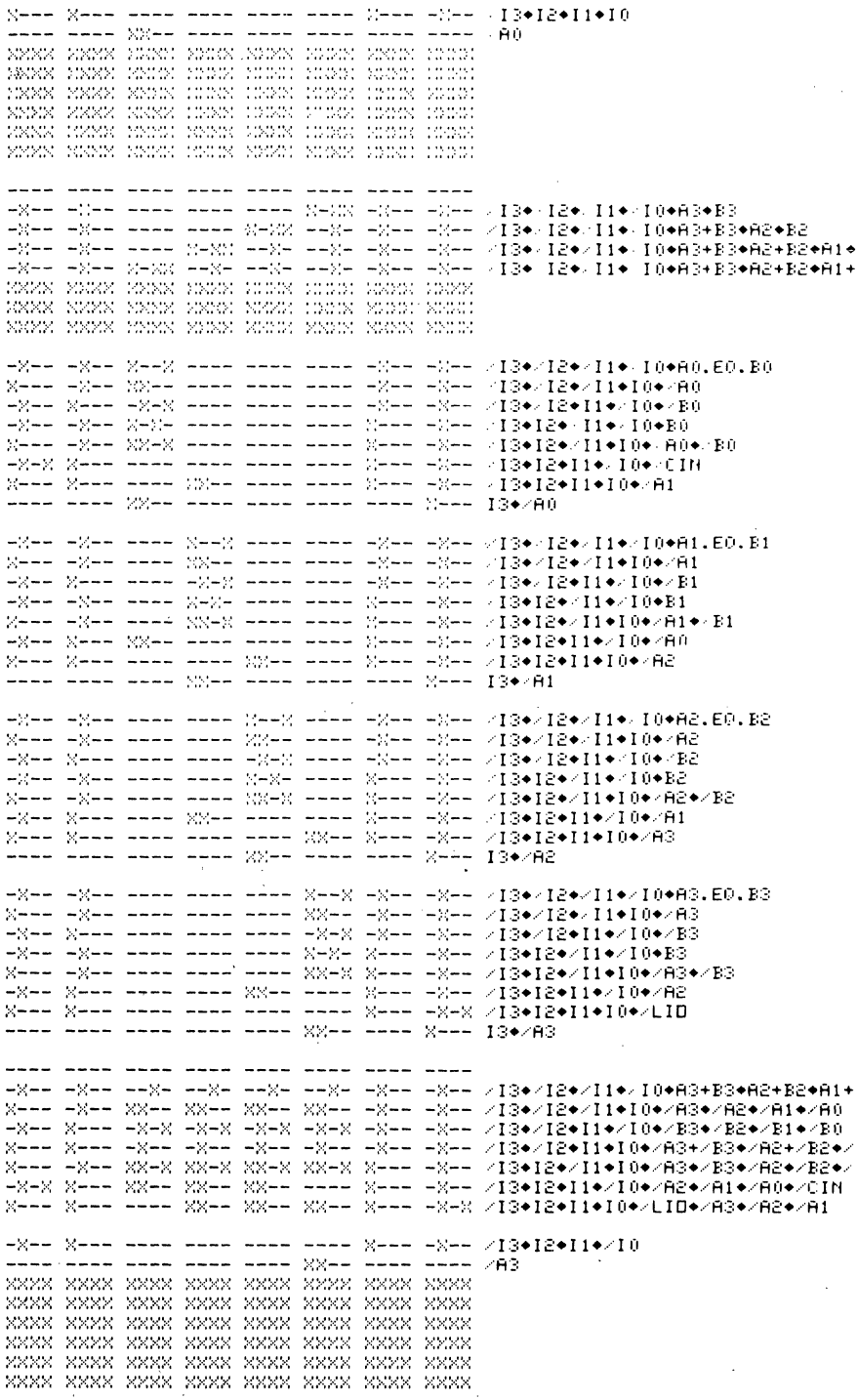
PAL16X4 Four-Bit Up/Down Counter with Shift and TRI-STATE (R) Outputs, Coded Logic Diagram.

```
PAL16A4                                  PAL DESIGN SPECIFICATION
PAT0026
ALU ACCUMULATOR

CLOCK  I0 I1 B0 B1 B2 B3 I2 I3 GND  E LIO  P A3 A2 A1 A0  G CIN VCC

 A0:=   I3* I2* I1* I0*/A0.E0.B0/ +  I3* I2* I1*I0*/ A0/ +  I3* I2*I1* I0*/ B0/+
        I3*I2* I1* I0*/B0/ :+:  I3*I2* I1*I0*/ A0* B0/ +
        I3*I2*I1* I0* CIN   +  I3*I2*I1*I0*/ A1/ + I3*/ A0/ + CARRY0

 A1:=   I3* I2* I1* I0*/A1.E0.B1/ +  I3* I2* I1*I0*/ A1/ +  I3* I2*I1* I0*/ B1/+
        I3*I2* I1* I0*/B1/ :+:  I3*I2* I1*I0*/ A1*/B1/ +
        I3*I2*I1* I0*/ A0/ +  I3*I2*I1*I0*/ A2/ + I3*/ A1/ + CARRY1

 A2:=   I3* I2* I1* I0*/A2.E0.B2/ +  I3* I2* I1*I0*/ A2/ +  I3* I2*I1*/I0*/ B2/+
        I3*I2* I1* I0*/B2/ :+:  I3*I2* I1*I0*/ A2*/B2/ +
        I3*I2*I1* I0*/ A1/ +  I3*I2*I1*I0*/ A3/ + I3*/ A2/ + CARRY2

 A3:=   I3* I2* I1* I0*/A3.E0.B3/ +  I3* I2* I1*I0*/ A3/ +  I3* I2*I1*/I0*/ B3/+
        I3*I2* I1* I0*/B3/ :+:  I3*I2* I1*I0*/ A3* B3/ +
        I3*I2*I1* I0*/ A2/ +  I3*I2*I1*I0* LIO   + I3*/ A3/ + CARRY3

IF/VCC/ G =  I3* I2* I1* I0 * /A3*B3/+
             I3*/I2* I1*/I0 * /A3+B3/*/A2*B2/+
             I3* I2* I1* I0 * /A3+B3/*/A2+B2/*/A1*B1/+
             I3* I2* I1* I0 * /A3+B3/*/A2+B2/*/A1+B1/*/A0*B0/

IF/VCC/ P =  I3* I2* I1* I0 * /A3+B3/*/A2+B2/*/A1+B1/*/A0+B0/ +
             I3* I2* I1*I0  * / A3/*/ A2/*/ A1/*/ A0/ +
             I3* I2*I1* I0  * / B3/*/ B2/*/ B1/*/ B0/ +
             I3* I2*I1*I0   * / A3+ B3/*/ A2+ B2/*/ A1+ B1/*/ A0+ B0/ +
             I3*I2* I1*I0   * / A3* B3/*/ A2* B2/*/ A1* B1/*/ A0* B0/ +
             I3*I2*I1* I0   * / A2/*/ A1/*/ A0/*/ CIN +
             I3*I2*I1*I0    *  LIO*/ A3/*/ A2/*/ A1/

IF/  I3*I2*I1* I0 /  LIO = / A3/

IF/  I3*I2*I1*I0  /  CIN = / A0/

NOTE:      CARRY0 =  I3* I2* I1* I0 * CIN

           CARRY1 =  I3* I2* I1* I0 * /A0*B0/+
                     I3* I2* I1* I0 * /A0+B0/*CIN

           CARRY2 =  I3* I2* I1* I0 * /A1*B1/+
                     I3* I2* I1* I0 * /A1+B1/*/A0*B0/+
                     I3* I2* I1* I0 * /A1+B1/*/A0+B0/*CIN

           CARRY3 =  I3* I2* I1* I0 * /A2*B2/+
                     I3* I2* I1* I0 * /A2+B2/*/A1*B1/+
                     I3* I2* I1* I0 * /A2+B2/*/A1+B1/*/A0*B0/+
                     I3* I2* I1* I0 * /A2+B2/*/A1+B1/*/A0+B0/*CIN

DESCRIPTION:
THE ALU ACCUMULATOR LOADS THE A-REGISTER WITH ONE OF EIGHT OPERANDS ON
THE RISING EDGE OF THE CLOCK. G AND P OUTPUT GENERATE AND PROPAGATE
ON THE ADD INSTRUCTION. P OUTPUT IS ZERO ON INSTRUCTIONS 1,2,3,5,6,7.

-------------------------------------------------------------------------------
!         INPUTS          !          OUTPUTS          !                      !
-------------------------------------------------------------      OPERATION      !
! I3 I2 I1 I0 ! LIO CIN ! LIO ! A3 A2 A1 A0 ! CIN !                      !
-------------------------------------------------------------------------------
!  L  L  L  L !  X   L  !  Z  ! A PLUS B    !  Z  ! ADD       A:=A PLUS B    !
!  L  L  L  L !  X   H  !  Z  ! A PL B PL 1  !  Z  ! ADD       A:=APLUSBPLUS1 !
!  L  L  L  H !  X   X  !  Z  ! A3 A2 A1 A0  !  Z  ! NOP       A:=A           !
!  L  L  H  L !  X   X  !  Z  ! B3 B2 B1 B0  !  Z  ! LOAD      A:=B           !
!  L  L  H  H !  X   X  !  Z  !   A AND B    !  Z  ! AND       A:=A*B         !
!  L  H  L  L !  X   X  !  Z  ! /B3 B2 B1 B0 !  Z  ! LOADCOMP  A:=/B          !
!  L  H  L  H !  X   X  !  Z  !   A OR B     !  Z  ! OR        A:=A+B         !
!  L  H  H  L !  X   LI !  A2 ! A2 A1 A0 LI  !  Z  ! SHIFT LEFT              !
!  L  H  H  H !  PI  X  !  Z  ! PI A3 A2 A1  !  A1 ! SHIFT RIGHT             !
!  H  X  X  X !  X   X  !  Z  ! A3 A2 A1 A0  !  Z  ! NOP       A:=A           !
-------------------------------------------------------------------------------
```

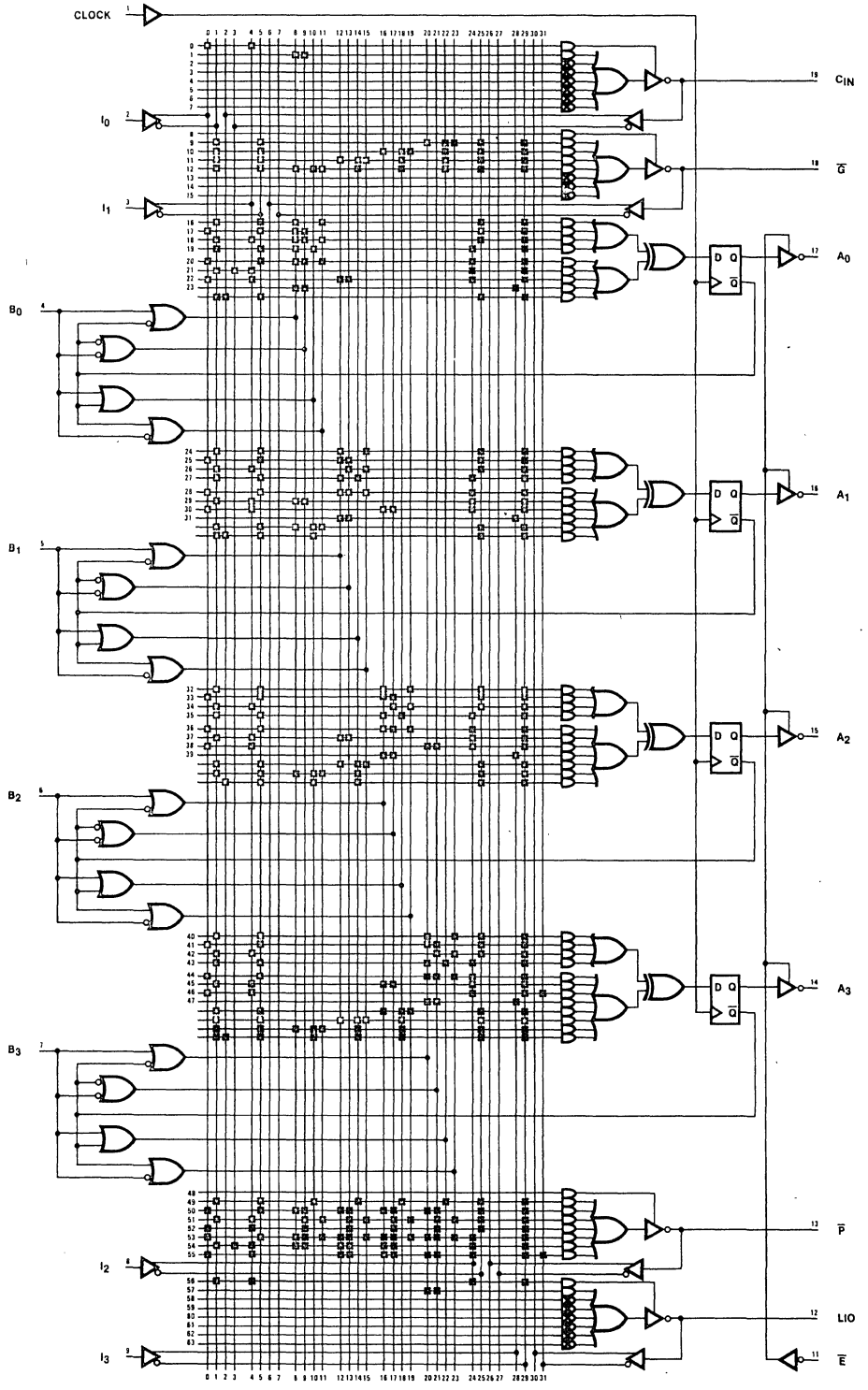
ALU Accumulator, Design Specification.

ALU Accumulator

Fuse Pattern PAL16A4



ALU Accumulator, PAL16A4 Fuse Pattern.



PAL16A4 ALU Accumulator, Coded Logic Diagram.

PACKAGES

Dual-In-Line Packages

(N) Devices ordered with "N" suffix are supplied in plastic molded dual-in-line packages. Molding material is a highly reliable compound suitable for military as well as commercial temperature range applications. Lead material is copper or alloy 42 with a hot solder dipped surface to allow ease of solderability.

(J) Devices ordered with the "J" suffix are supplied in a CERDIP package (ceramic lid and base sealed with high temperature vitreous glass). Lead material is solder dipped alloy 42.

(D) Devices ordered with the "D" suffix are supplied in side brazed, multi-layer, ceramic dual-in-line packages. The leads are Kovar or alloy 42 and either tin-plated, gold-plated, or solder-plated.

(Q) Devices ordered with the "Q" suffix are supplied in either a "D" or "J" package, but with a UV window.

Metal Can Packages

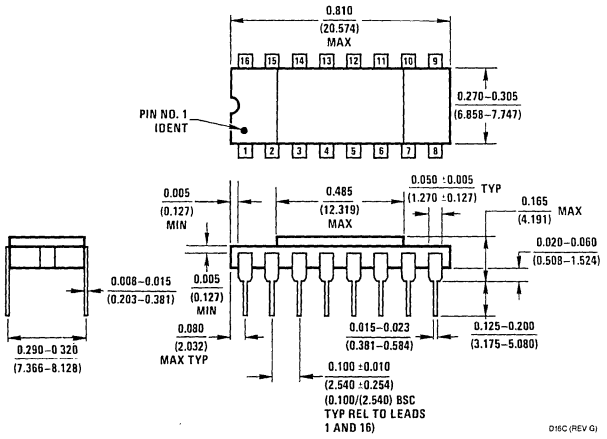
(H) Devices ordered with the "H" suffix are supplied in a metal can package. The cap is nickel finish and the leads are gold-plated Kovar. Gold free construction using epoxy D/A is also available, with a tin-plated finish.

Flat Packages

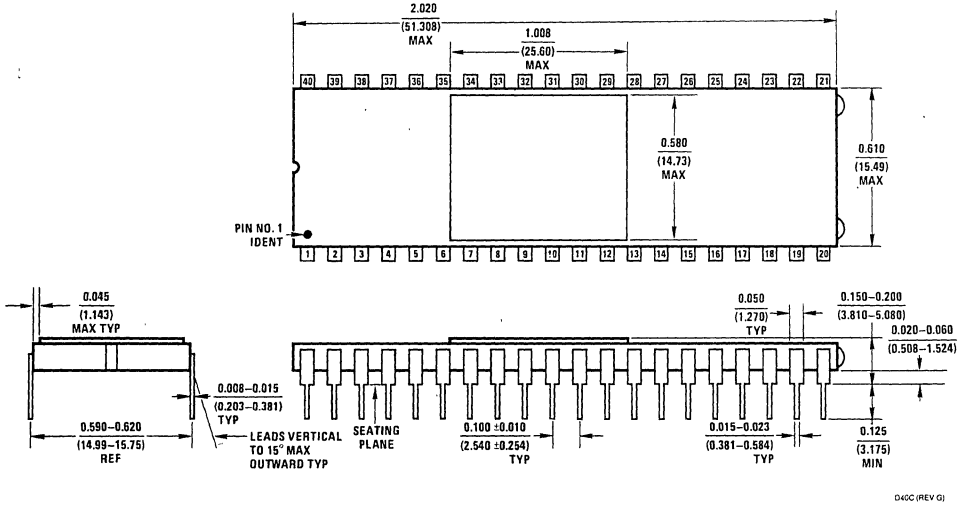
(F) Devices ordered with the "F" suffix are supplied in a multi-layer, ceramic bottom brazed flat package. The lid is plated alloy 42, and leads are gold-plated, tin-plated, or solder-plated alloy 42 or Kovar.

(W) Devices ordered with the "W" suffix are supplied in a low-temperature ceramic flat package.

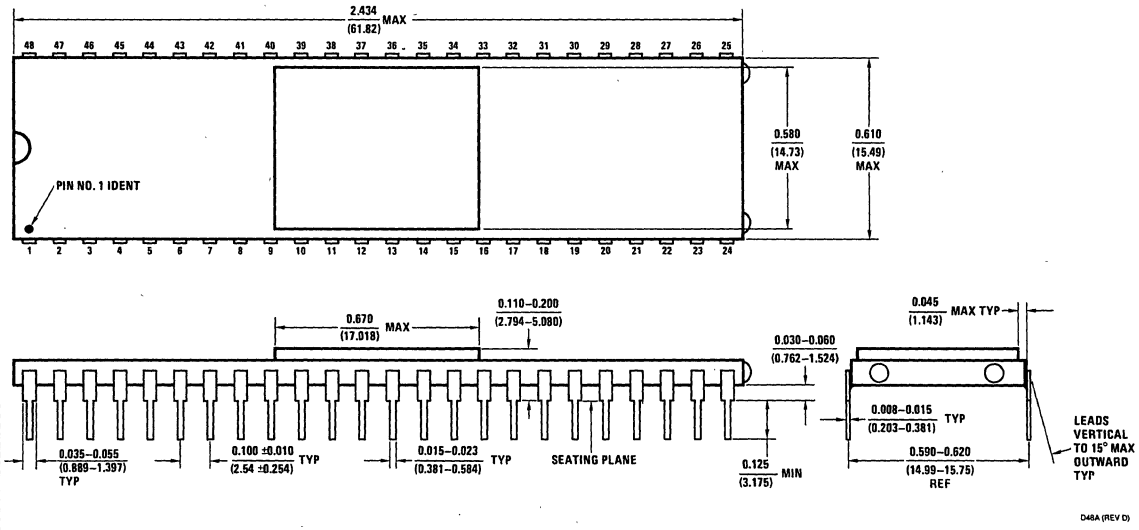
D16A package is replaced by D16C package.



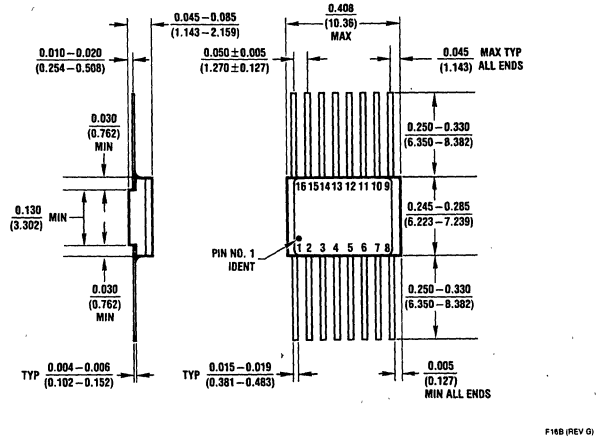
NS Package D16C
16-Lead Cavity DIP (D)



NS Package D40C
40-Lead Cavity DIP (D)

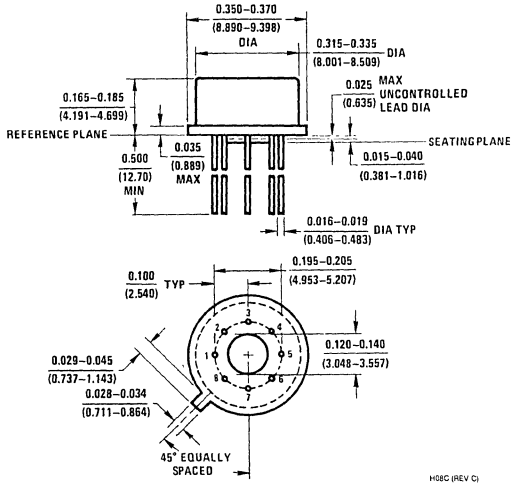


NS Package D48A
48-Lead Cavity DIP (D)

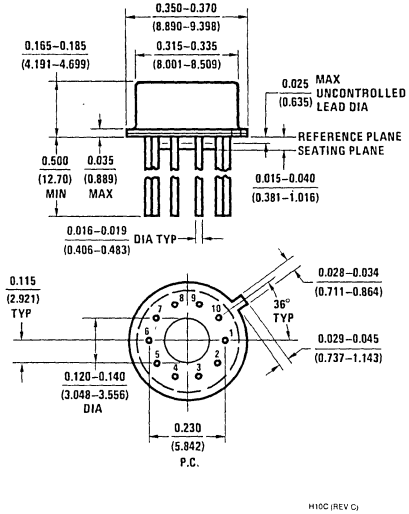


NS Package F16B
16-Lead Flat Package (F)

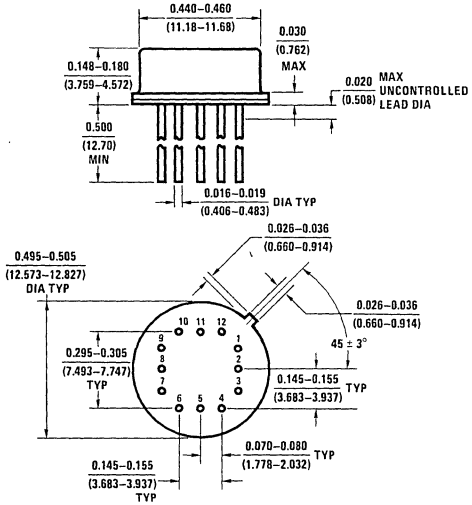
G12C package is replaced by H12C package.



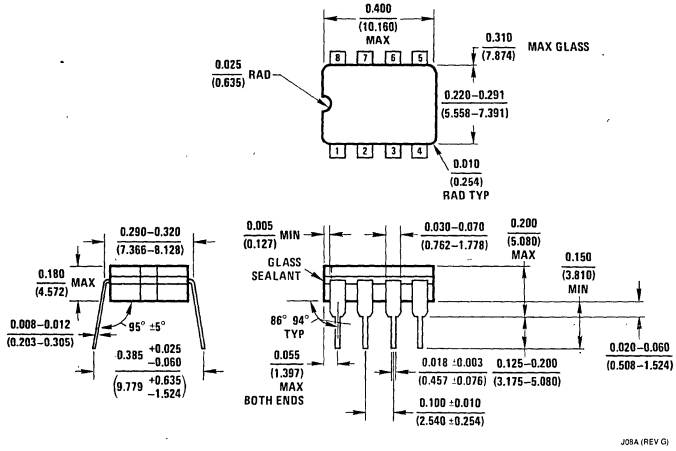
NS Package H08C
8-Lead TO-5 Metal Can Package (H)



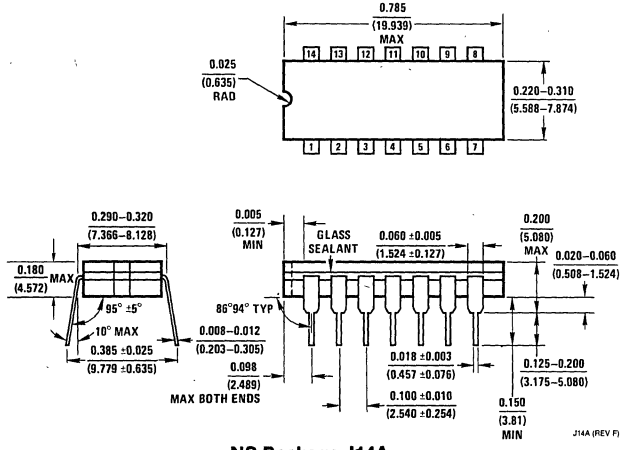
NS Package H10C
10-Lead TO-5 Metal Can Package (H)
(Low Profile)



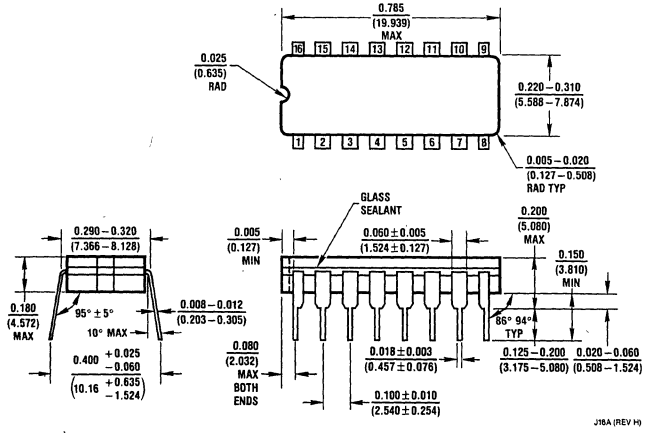
NS Package H12C
12-Lead TO-8 Metal Can Package (H)



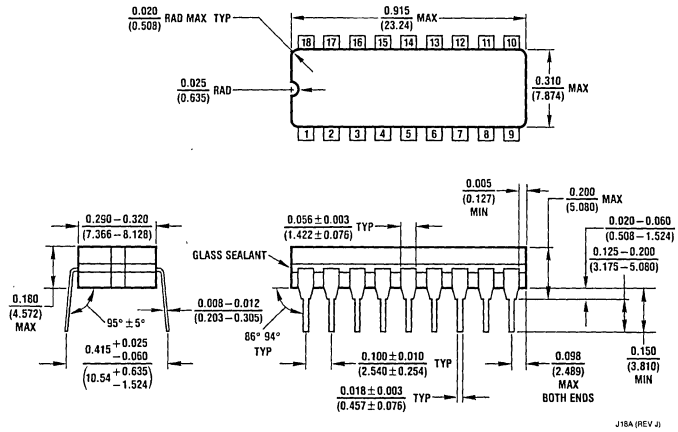
NS Package J08A
8-Lead Cavity DIP (J)



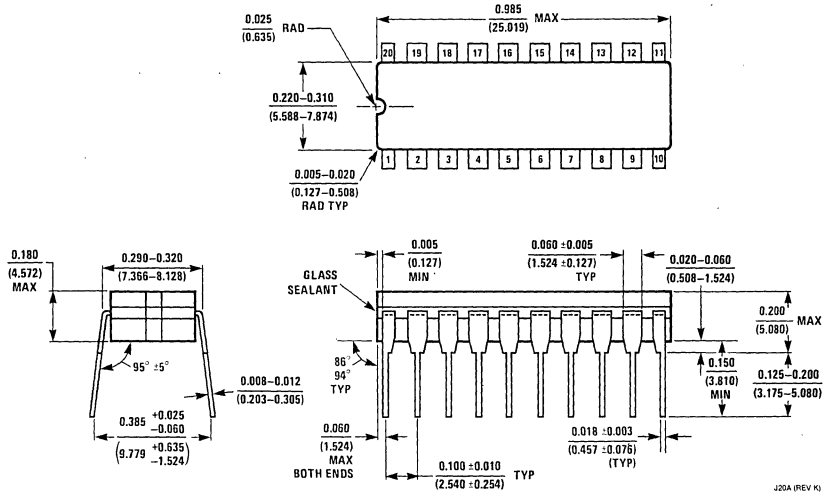
NS Package J14A
14-Lead Cavity DIP (J)



NS Package J16A
16-Lead Cavity DIP (J)

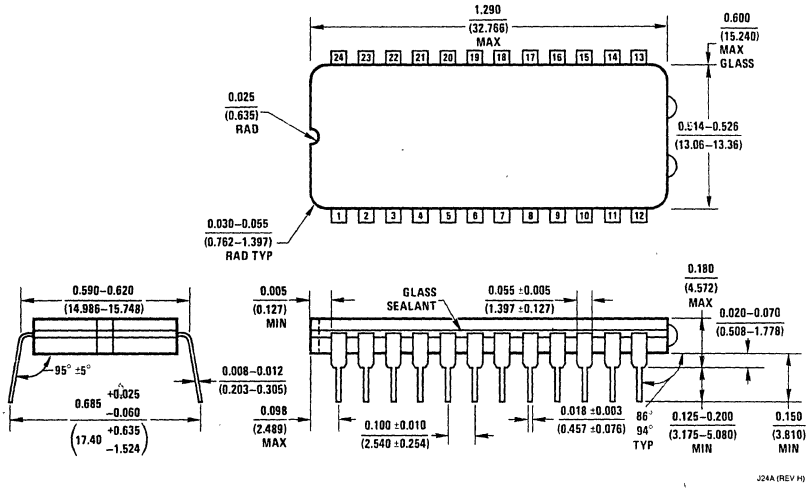


NS Package J18A
18-Lead Cavity DIP (J)



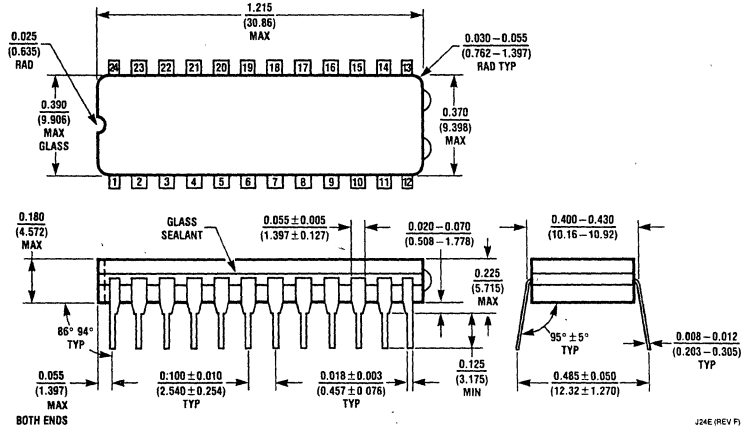
NS Package J20A
20-Lead Cavity DIP (J)

J20B package is replaced by J20A package.

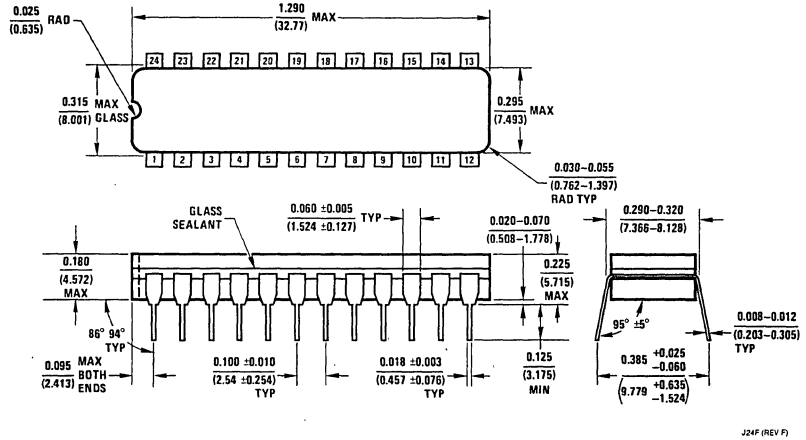


NS Package J24A
24-Lead Cavity DIP (J)

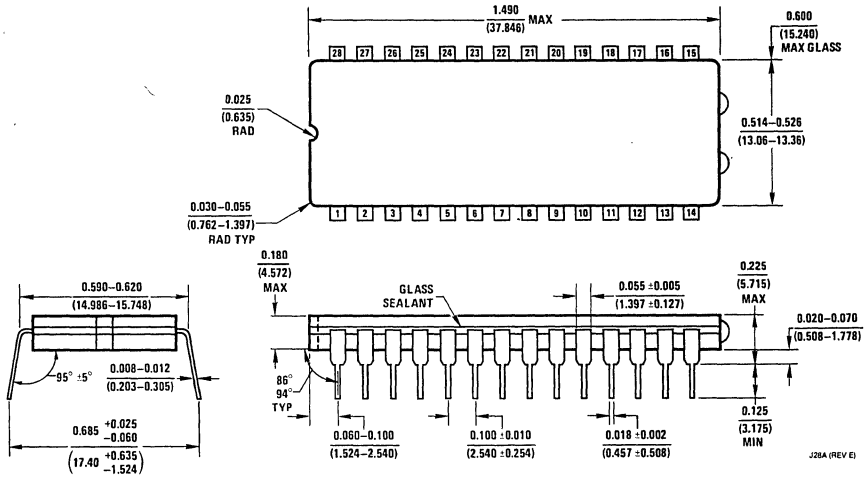
J24C package is replaced by J24A package.



NS Package J24E
24-Lead Cavity DIP (J)

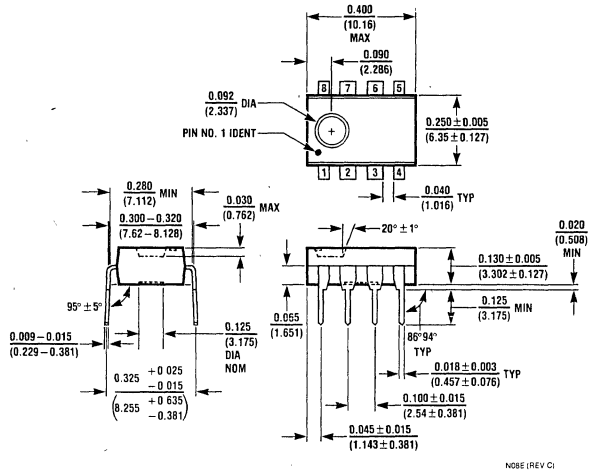


NS Package J24F
24-Lead Cavity DIP (J)

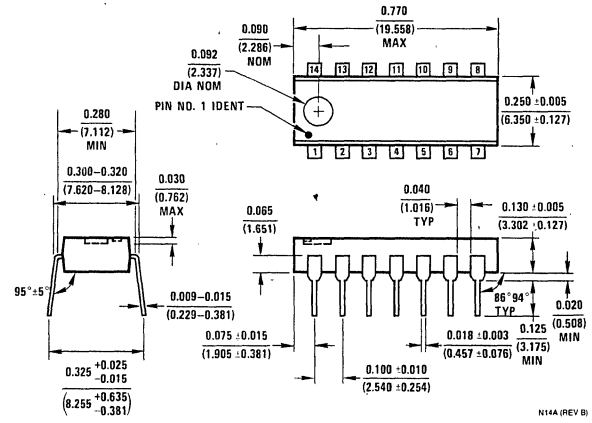


NS Package J28A
28-Lead Cavity DIP (J)

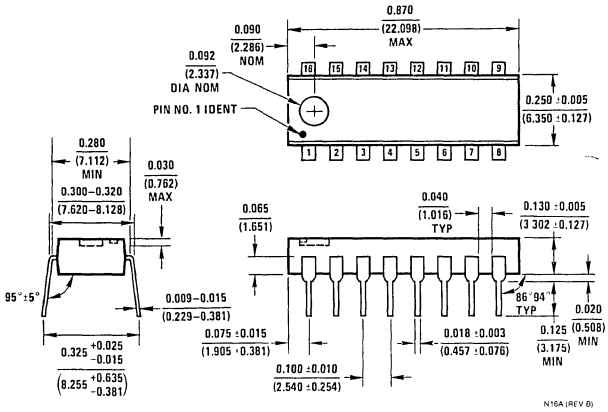
N08A package is replaced by N08E package.



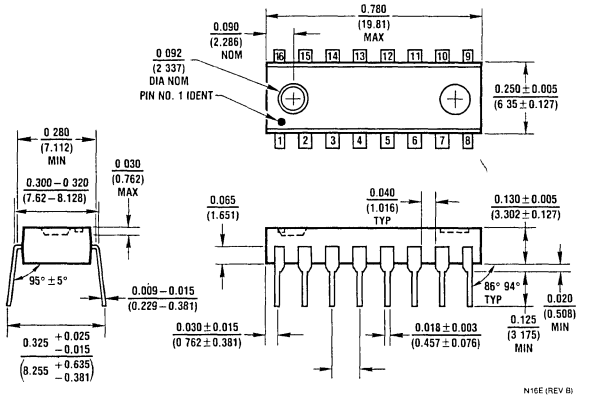
NS Package N08E
8-Lead Molded DIP (N)



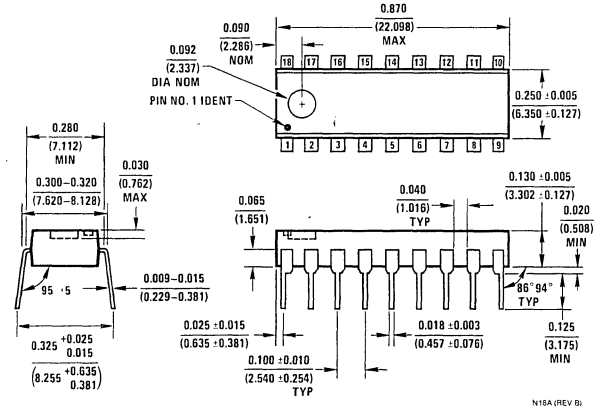
NS Package N14A
14-Lead Molded DIP (N)



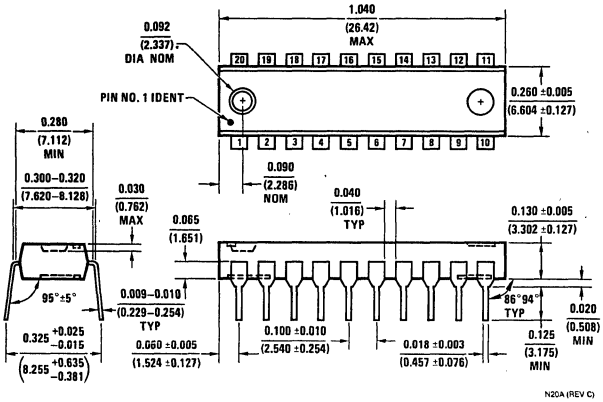
NS Package N16A
16-Lead Molded DIP (N)
(N16E may be substituted)



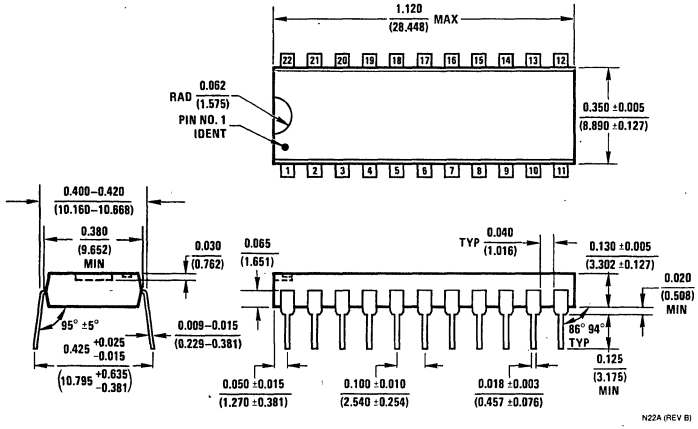
NS Package N16E
16-Lead Molded DIP (N)
(Substitute for N16A)



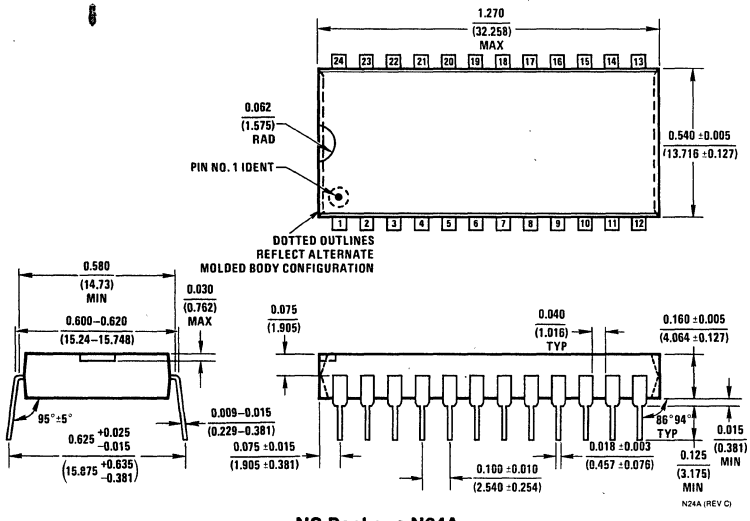
NS Package N18A
18-Lead Molded DIP (N)



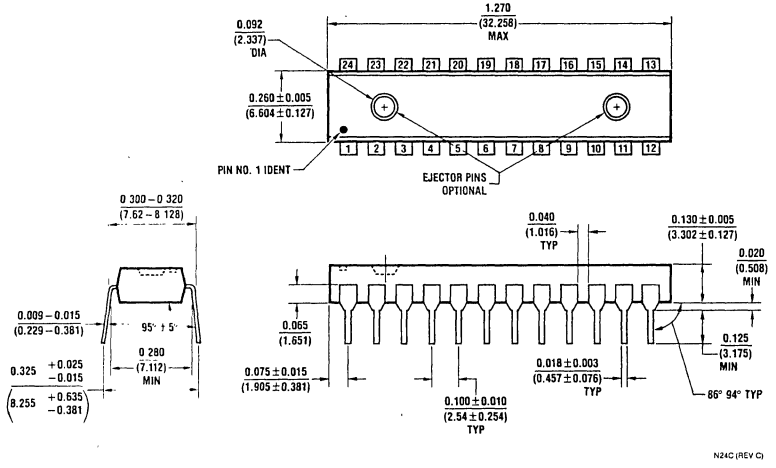
NS Package N20A
20-Lead Molded DIP (N)



NS Package N22A
22-Lead Molded DIP (N)

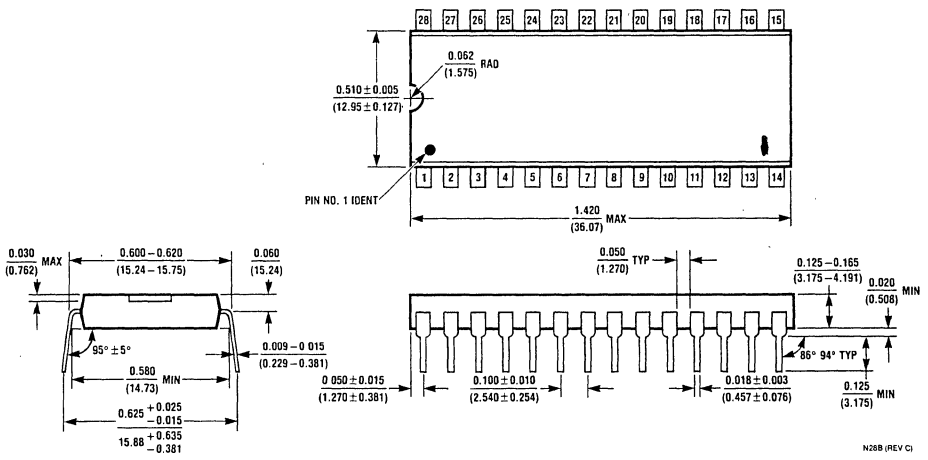


NS Package N24A
24-Lead Molded DIP (N)

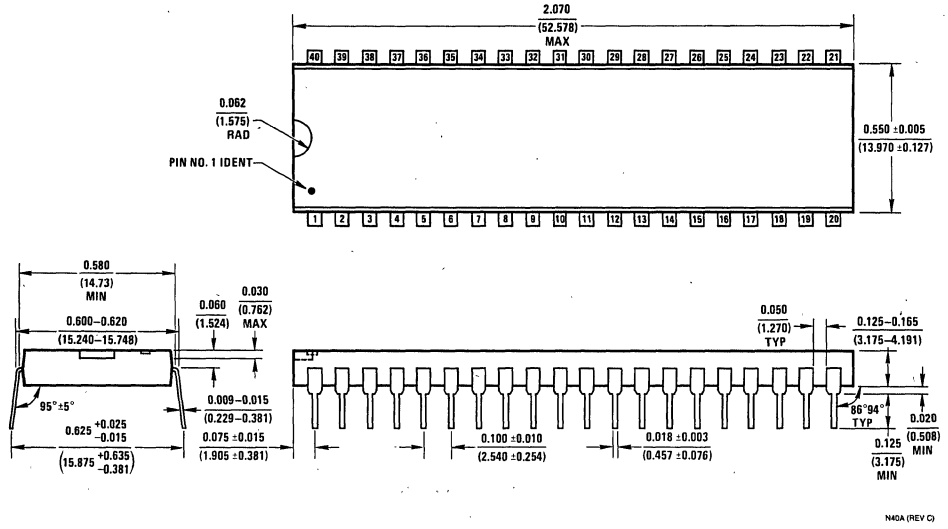


NS Package N24C
24-Lead Molded DIP (N)

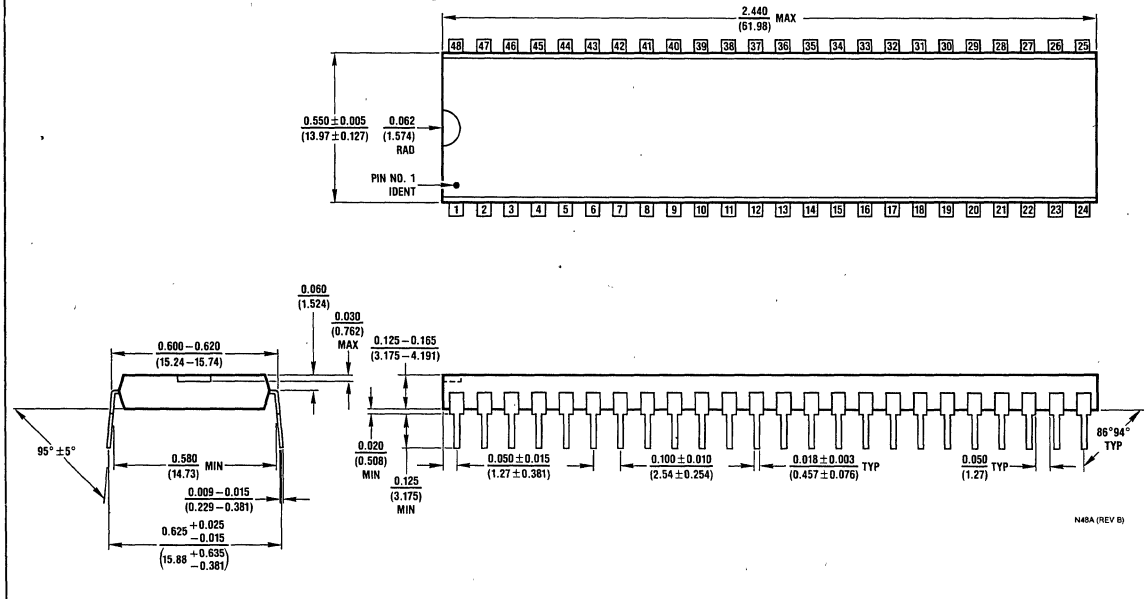
N28A package is replaced by N28B package.



NS Package N28B
28-Lead Molded DIP (N)

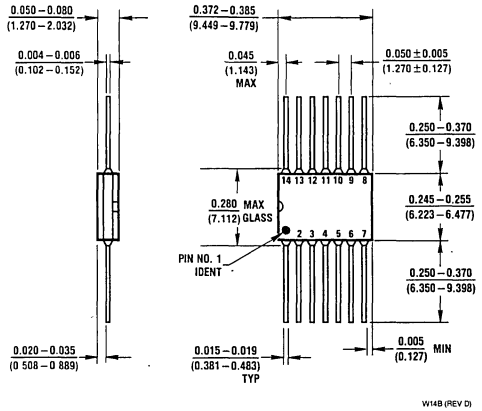


NS Package N40A
40-Lead Molded DIP (N)



NS Package N48A
48-Lead Molded DIP (N)

W14A package is replaced by W14B package.



NS Package W14B
14-Lead Flat Package (W)

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
Tel: (408) 721-5000
TWX: (910) 339-9240

Electronica NSC de Mexico SA
Hegel No. 153-204
Mexico 5 D.F. Mexico
Tel: (905) 531-1689, 531-0569, 531-8204
Telex: 017-73559

National Semiconductores Do Brasil Ltda.
Avda Brigadeiro Faria Lima 830
8 ANDAR
01452 Sao Paulo, Brasil
Tel: 212-1181
Telex: 1131931 NSBR

National Semiconductor GmbH
Furstenriederstrasse Nr.5
D-8000 Munchen 21
West Germany
Tel: (089) 5 60 12-0
Telex: 522772

National Semiconductor (UK) Ltd.
301 Harpur Centre
Horne Lane
Bedford MK40 1TR
United Kingdom
Tel: 0234-47147
Telex: 826 209

National Semiconductor Benelux
Ave. Charles Quint 545
B-1080 Bruxelles
Belgium
Tel: (02) 4661807
Telex: 61007

National Semiconductor (UK) Ltd.
1, Bianco Lunos Alle
DK-1868 Copenhagen V
Denmark
Tel: (01) 213211
Telex: 15179

National Semiconductor
Expansion 10000
28, Rue de la Redoute
F-92 260 Fontenay-aux-Roses
France
Tel: (01) 660-8140
Telex: 250956

National Semiconductor S.p.A.
Via Solferino 19
20121 Milano
Italy
Tel: (02) 345-2046/7/8/9
Telex: 332835

National Semiconductor AB
Box 2016
Stensätravägen 4/11 TR
S-12702 Skaerholmen
Sweden
Tel: (08) 970190
Telex: 10731

National Semiconductor
Calle Nunez Morgado 9
(Esc. Dcha. 1-A)
E-Madrid 16
Spain
Tel: (01) 733-2954/733-2958
Telex: 46133

National Semiconductor Switzerland
Alte Winterhurerstrasse 53
Postfach 567
CH-8304 Wallisellen-Zurich
Tel: (01) 830-2727
Telex: 59000

National Semiconductor
Pasilanraitio 6C
SF-00240 Helsinki 24
Finland
Tel: (90) 14 03 44
Telex: 124854

NS Japan K.K.
POB 4152 Shinjuku Center Building
1-25-1 Nishishinjuku, Shinjuku-ku
Tokyo 160, Japan
Tel: (03) 349-0811
Telex: 232-2015 NSCJ-J

National Semiconductor (Hong Kong) Ltd.
1st Floor
Cheung Kong Electronic Bldg.
4 Hing Yip Street
Kwun Tong
Kowloon, Hong Kong
Tel: 3-899235
Telex: 43866 NSEHK HX
Cable: NATSEMI HX

NS Electronics Pty. Ltd.
Cnr. Stud Rd. & Mtn. Highway
Bayswater, Victoria 3153
Australia
Tel: 03-729-6333
Telex: 32096

National Semiconductor (PTE) Ltd.
10th Floor
Pub Building, Devonshire Wing
Somerset Road
Singapore 0923
Tel: 652700047
Telex: NAT SEMI RS 21402

National Semiconductor (Far East) Ltd. Taiwan Branch
P.O. Box 68-332 Taipei
3rd Flr. Apollo Bldg. No. 281-7
Chung HSIAO E. Rd., Sec. 4
Taipei, Taiwan R.O.C.
Tel: 7310393-4, 7310465-6
Telex: 22837 NSTW
Cable: NSTW TAIPEI

National Semiconductor (HK) Ltd. Korea Liaison Office
6th Floor, Kunwon Bldg.
2-1 GA Mookjung-Dong
Choong-Ku, Seoul
C.P.O. Box 7941 Seoul
Tel: 267-9473
Telex: K24942

 BF/2648 IM-RRD150M73/Printed in U.S.A.