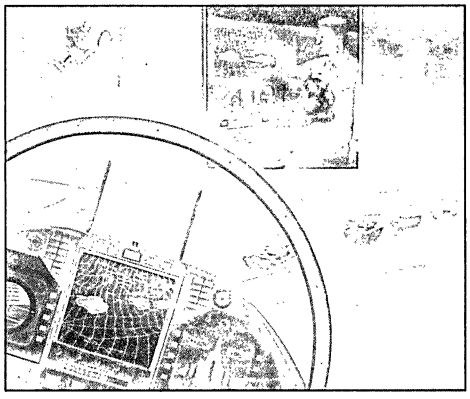
Military MECL
Family Data

MOTOROLA

MOTOROLA MILITARY MECL FAMILY

Q3/91
DL145



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MOTOROLA

MILITARY MECL INTEGRATED CIRCUITS

Prepared by
Military Products Operation
Strategic Marketing
and Technical Publications

This book presents technical data for a broad line of MECL (Military) integrated circuits. Complete specifications for the individual circuits are provided in the form of data sheets.

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First Edition
First Printing

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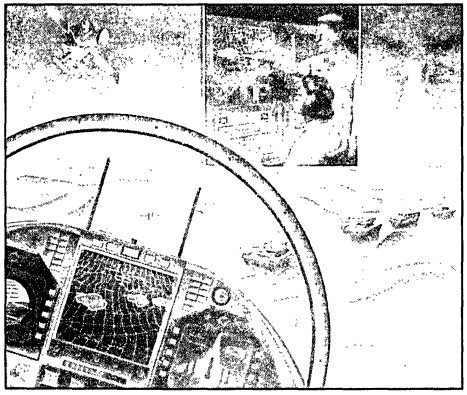


General Information

1

High Speed-Logic

1

High speed logic is used whenever improved system performance would increase a product's market value. For a given system design, high-speed logic is the most direct way to improve system performance and emitter-coupled logic (ECL) is today's fastest form of digital logic. Emitter-coupled logic offers both the logic speed and logic features to meet the market demands for higher performance systems.

MECL PRODUCTS

Motorola introduced the original monolithic emitter-coupled logic family with MECL I (1962) and followed this with MECL II (1966). These two families are now obsolete and have given way to the MECL III (1600 series), MECL 10K, PLL (12000 series) and MECL 10H families.

Chronologically the third family introduced, MECL III (1968) is a higher power, higher speed logic. Typical 1.0 ns edge speeds and propagation delays along with greater than 500 MHz flip-flop toggle rate, make MECL III useful for high-speed test and communication equipment. Also, this family is used in the high-speed sections and critical timing delays of larger systems. For more general purpose applications, however, trends in the large high-speed systems showed the need for easy-to-use logic family with propagation delays on the order of 2.0 ns. To match this requirement, the MECL 10,000 Series was introduced in 1971.

An important feature of the MECL 10K is its compatibility with MECL III to facilitate using both families in the same system. A second important feature is its significant power economy—MECL 10K gates use less than one-half the power of MECL III.

Motorola introduced the MECL 10H product family in 1981. This MECL family features 100% improvements in propagation delay and clock speeds while maintaining power supply currents equal to MECL 10K. MECL 10H is voltage compensated allowing guaranteed dc switching parameters over a ± 5.0% power supply range. Noise margins have been improved by 75% over the MECL 10K series.

Compatibility with MECL 10K and MECL III is a key element in allowing users to enhance existing systems by increasing the speed in critical timing areas. Also, many MECL 10H devices are pin out/functional duplications of the MECL 10K series devices. The emphasis of this new family will be placed on more powerful logic functions having more complexity and greater performance. With 1.0 ns propagation delays and 25 mW per gate, MECL 10H features the best speed-power product of any ECL logic family available today.

MECL IN PERSPECTIVE

In evaluating any logic line, speed and power requirements are the obvious primary considerations. Figure 1 provides the basic parameters of the MECL 10H, MECL 10K, and MECL III families. But they provide only the start of any comparative analysis, as there are a number of other important features that make MECL highly desirable for system implementation. Among these:

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces timing differential problems arising from the time delays introduced by inverters.

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

MECL FAMILY COMPARISON

Feature	MECL 10H	MECL 10K		MECL III
		10,100 Series	10,200 Series	
1. Gate Propagation Delay	1.0 ns	2.0 ns	1.5 ns	1.0 ns
2. Output Edge Speed *	1.0 ns	3.5 ns	2.5 ns	1.0 ns
3. Flip-Flop Toggle Speed	250 MHz min	125 MHz min	200 MHz min	300-500 MHz min
4. Gate Power	25 mW	25 mW	25 mW	60 mW
5. Speed Power Product	25pJ	50 pJ	37 pJ	60 pJ

* Output edge speed: MECL 10K/10H measured 20% to 80%, MECL III measured 10% to 90% of E out.

Figure 1. General Characteristics

Nearly Constant Power Supply Current Drain simplifies power-supply design and reduces costs.

Low Cross-Talk due to low-current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by Low power dissipation (particularly in MECL 10H and MECL 10K series). A basic MECL 10K gate consumes less than 8.0 mW in on-chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No "Line Drivers" are listed in MECL families, because every device is a line driver.

Wire-ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted-pair transmission lines as long as 1000 feet.

Wire-Wrap Capability is possible with the MECL 10K family because of the slow rise and fall time characteristic of the circuits.

Open Emitter-Follower Outputs are used for MECL outputs to simplify signal line drive. The outputs match any line impedance and the absence of internal pulldown resistors saves power.

Input Pulldown Resistor of approximately 50 kΩ permit unused inputs to remain unconnected for easier circuit board layout.

MECL APPLICATIONS

Motorola's MECL product lines are designed for a wide range of systems needs. Within the computer market, MECL 10K is used in systems ranging from special purpose peripheral controllers to large mainframe computers. Big growth areas in this market include disk and communication channel controllers for large systems and high performance minicomputers.

The industrial market primarily uses MECL for high performance test systems such as IC or PC board testers. However, the bandwidths of MECL 10H, MECL 10K, MECL III, and 12,000 are required for many frequency synthesizer systems using high speed phase lock loop networks. MECL will continue to grow in the industrial market through complex medical electronic products and high performance process control systems.

MECL 10K and MECL III have been accepted within the Federal market for numerous signal processors and navigation systems.

BASIC CONSIDERATIONS FOR HIGH-SPEED LOGIC DESIGN

High-speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium-speed systems, become highly important at state-of-the-art speeds.
2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.
3. The possibility of "crosstalk" between adjacent signal leads is proportionally increased in high-speed systems.
4. Electrical noise generation and pick-up are more determined at higher speeds.

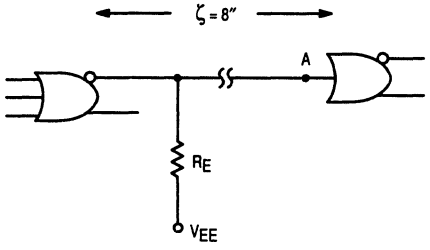
In general, these four characteristics are speed-and frequency-dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

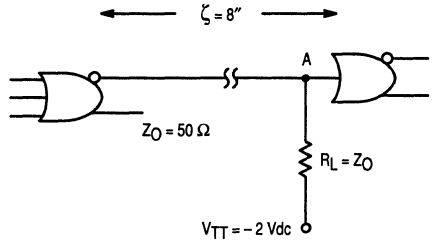
The interconnect-wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent "gate delay" is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip, the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. *MECL circuits, particularly those of the MECL 10K and MECL 10H Series are designed with a propensity toward complex functions to enhance overall system speed.*

Waveform distortion due to line reflections also becomes troublesome principally at state-of-the-art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At higher speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 2). The solution, as in RF technology, is to employ "transmission-line" practices and properly terminate each signal line with its characteristic impedance at the end of its run. *The low-impedance, emitter-follower outputs of MECL circuits facilitate transmission-line practices without upsetting the voltage levels of the system.*

The increase affinity for crosstalk in high-speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high-speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. *In the design of MECL 10K and MECL 10H, the rise and fall times have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.*

From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high-speed operation.





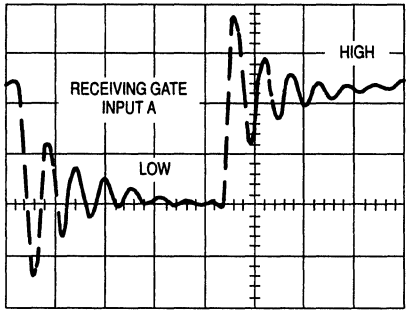


Figure 2a. Unterminated Transition Line (No Ground Plane Used)

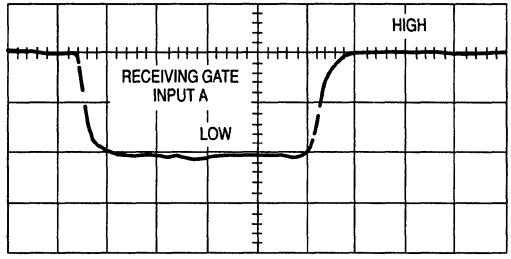


Figure 2b. Properly Terminated Transition Line (Ground Plane Added)

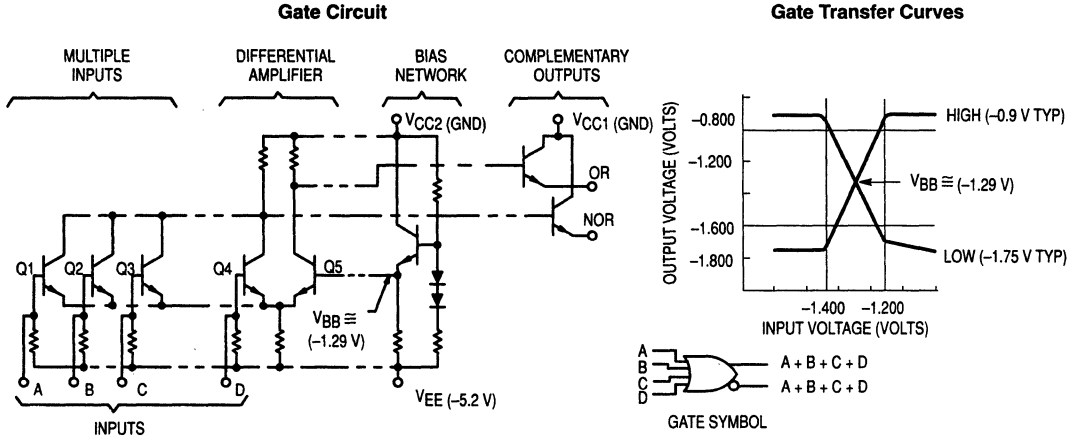


Figure 3. MECL 10K Gate Structure and Switching Behavior

CIRCUIT DESCRIPTION

The typical MECL 10K circuit, Figure 3, consists of a differential-amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower outputs to restore dc levels and provide buffering for transmission line driving. High fan-out operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter-follower outputs. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function. The design of the MECL 10H gate is unchanged, with two exceptions. The bias network has been replaced with a voltage regulator, and the differential amplifier source resistor has been replaced with a constant current source. (See section 2 for additional MECL 10H information.)

Power-Supply Connections — Any of the power supply levels, V_{TT}, V_{CC}, or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case: V_{CC} = 0, V_{TT} = - 2.0 V, V_{EE} = - 5.2 V.

System Logic Specifications — The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of V_{OL} = - 1.75 V to a HIGH state of V_{OH} = - 0.9 V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's." Then

"0" = - 1.75 V = LOW
"1" = 0.9 V = HIGH

Circuit Operation — Beginning with all logic inputs LOW (nominal - 1.75 V), assume that Q1 through Q4 are cut off because their P-N base-emitter junctions are not conducting, and the forward-biased Q5 is conducting. Under these conditions, with the base of Q5 held at - 1.29 V by the V_{BB} network, its emitter will be one diode drop (0.8 V) more negative than the base, or - 2.09 V. (The 0.8 V differential is a characteristic of this P-N junction.) The base-to-emitter differential across Q1–Q4 is then the difference between the common emitter voltage (- 2.09 V) and the LOW logic level (- 1.75 V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off.

When any one (or all) of the logic inputs are shifted upwards from the - 1.75 V LOW state to the - 0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common-emitter point rises from - 2.09 V to - 1.7 (one diode drop below the - 0.9 V base voltage of the input transistor), and since the base voltage of the fixed-bias transistor (Q5) is held at - 1.29 V, the base-emitter voltage Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 - Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1–Q4 and Q5 are transferred through the output emitter-follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

Current

I_{CC} Total power supply current drawn from the positive supply by a MECL unit under test.

I_{CBO} Leakage Current from input transistor on MECL devices without pulldown resistors when test voltage applied.

I_{CCH} Current drain from V_{CC} power supply with all inputs at logic HIGH level.

I_{CCL} Current drain from V_{CC} power supply with all inputs at logic LOW level.

I_E Total power supply current drawn from a MECL test unit by the negative power supply.

I_F Forward diode current drawn from an input of a saturated logic-to-MECL translator when that input is at ground potential.

I_{in} Current into the input of the test unit when a maximum logic HIGH (V_{IH}max) is applied at that input.

I_{INH} HIGH level input current into a node with a specified HIGH level (V_{IH}max) logic voltage applied to that node. (Same as I_{in} for positive logic).

I_{INL} LOW level input current, into a node with a specified LOW level (V_{IL}min) logic voltage applied to that node.

I_L Load current that is drawn from a MECL circuit output when measuring the output HIGH level voltage.

I_{OH} HIGH level output current: the current flowing into the output, at a specified HIGH level output voltage.

I_{OL} LOW level output current: the current flowing into the output, at a specified LOW level output voltage.

I_{OS} Output short circuit current.

I_{OUT} Output current (from a device or circuit, under such conditions mentioned in context).

I_R Reverse current drawn from a transistor input of a test unit when V_{EE} is applied at that input.

I_{SC} Short-circuit current drawn from a translator saturating output when that output is at ground potential.

Voltage

V_{BB} Reference bias supply voltage.

V_{BE} Base-to-emitter voltage drop of a transistor at specified collector and base currents.

V_{CB} Collector-to-base voltage drop of a transistor at specified collector and base currents.

V_{CC} General term for the most positive power supply voltage to a MECL device (usually ground, except for translator and interface circuits).

V_{CC1}	Most positive power supply voltage (output devices). (Usually ground for MECL devices.)
V_{CC2}	Most positive power supply voltage (current switches and bias driver). (Usually ground for MECL devices.)
V_{EE}	Most negative power supply voltage for a circuit. (Usually –5.2 V for MECL devices.)
V_F	Input voltage for measuring I_F on TTL interface circuits.
V_{IH}	Input logic HIGH voltage level (nominal value).
$V_{IH}max$	Maximum HIGH level input voltage: The most positive (least negative) value of high-level input voltage, for which operation of the logic element within specification limits is guaranteed.
V_{IHA}	Input logic HIGH threshold voltage level.
$V_{IHA}min$	Minimum input logic HIGH level (threshold) voltage for which performance is specified.
$V_{IH}min$	Minimum HIGH level input voltage: The least positive (most negative) value of HIGH level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{IL}	Input logic LOW voltage level (nominal value).
$V_{IL}max$	Maximum LOW level input voltage: The most positive (least negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{ILA}	Input logic LOW threshold voltage level.
$V_{ILA}max$	Maximum input logic LOW level (threshold) voltage for which performance is specified.
$V_{IL}min$	Minimum LOW level input voltage: The least positive (most negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{in}	Input voltage (to a circuit or device).
V_{max}	Maximum (most positive) supply voltage, permitted under a specified set of conditions.
V_{OH}	Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current, with the specified conditions applied to establish a HIGH level at the output.
V_{OHA}	Output logic HIGH threshold voltage level.
$V_{OHA}min$	Minimum output HIGH threshold voltage level for which performance is specified.
$V_{OH}max$	Maximum output HIGH or high-level voltage for given inputs.
$V_{OH}min$	Minimum output HIGH or high-level voltage for given inputs.
V_{OL}	Output logic LOW voltage level: The voltage level at the output terminal for a specified output current, with the specified conditions applied to establish a LOW level at the output.
V_{OLA}	Output logic LOW threshold voltage level.
$V_{OLA}max$	Maximum output LOW threshold voltage level for which performance is specified.
$V_{OL}max$	Maximum output LOW level voltage for given inputs.
$V_{OL}min$	Minimum output LOW level voltage for given inputs.
V_{TT}	Line load-resistor terminating voltage for outputs from a MECL device.
V_{OLS1}	Output logic LOW level on MECL 10,000 line receiver devices with all inputs at V_{EE} voltage level.
V_{OLS2}	Output logic LOW level on MECL 10,000 line receiver devices with all inputs open.

Time Parameters

t+	Waveform rise time (LOW to HIGH), 10% to 90%, or 20% to 80%, as specified.
t–	Waveform fall time (HIGH to LOW), 10% to 90%, or 20% to 80%, as specified.
t_r	Same as t+
t_f	Same as t–
t+ –	Propagation Delay, see Figure 9.
t– +	Propagation Delay, see Figure 9.
t_{pd}	Propagation Delay, input to output from the 50% point of the input waveform at pin x.
$t_{X\pm Y\pm}$	(Falling edge noted by – or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by – or rising edge noted by +). (Cf Figure 9.)
t_{X+}	Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x, with input conditions as specified.
t_{X-}	Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x, with input conditions as specified.
f_{Tog}	Toggle frequency of a flip-flop or counter device.
f_{shift}	Shift rate for a shift register.

Read Mode (Memories):

t_{ACS}	Chip Select Access Time
t_{RCS}	Chip Select Recovery Time
t_{AA}	Address Access Time

Write Mode (Memories):

t_W	Write Pulse Width
t_{WSD}	Data Setup Time Prior to Write
t_{WHD}	Data Hold Time After Write
t_{WSA}	Address Setup Time Prior to Write
t_{WHA}	Address Hold Time After Write
t_{WSCS}	Chip Select Setup Time Prior to Write
t_{WHCS}	Chip Select Hold Time After Write
t_{WS}	Write Disable Time
t_{WR}	Write Recovery Time

CIRCUIT DESCRIPTION (continued)

Temperature:

T_{stg}	Maximum temperature at which device may be stored without damage or performance degradation.
T_J	Junction (or die) temperature of an integrated circuit device.
T_A	Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit device package.
$\overline{\varnothing}_{JA}$	Thermal resistance of an IC package, junction to ambient.
$\overline{\varnothing}_{JC}$	Thermal resistance of an IC package, junction to case.
lfpm	Linear feet per minute.
$\overline{\varnothing}_{CA}$	Thermal resistance of an IC package, case to ambient.

Miscellaneous:

e_g	Signal generator inputs to a test circuit.
TP_{in}	Test point at input of unit under test.
TP_{out}	Test point at output of unit under test.
D.U.T.	Device Under Test.
C_{in}	Input capacitance.
C_{out}	Output capacitance.
Z_{out}	Output impedance.
P_D	Total dc power applied to a device, not including any power delivered from the device to a load.
R_L	Load resistance.
R_T	Terminating (load) resistance.
R_P	An input pull-down resistor (i.e, connected to the most negative voltage).
P.U.T.	Pin Under Test.

MECL POSITIVE AND NEGATIVE LOGIC

INTRODUCTION

The increasing popularity and use of emitter coupled logic has created a dilemma for some logic designers. Saturated logic families such as TTL have traditionally been designed with the NAND function as the basic logic function, however, the basic ECL logic function is the NOR function (positive logic). Therefore, the designer may either design ECL systems with positive logic using the NOR, or design with negative logic using the NAND. Which is the more convenient? On the one hand the designer is familiar with positive logic levels and definitions, and on the other hand, he/she is familiar with implementing systems using NAND functions. Perhaps a presentation of the basic definitions and characteristics of positive and negative logic will clarify the situation and eliminate misunderstanding.

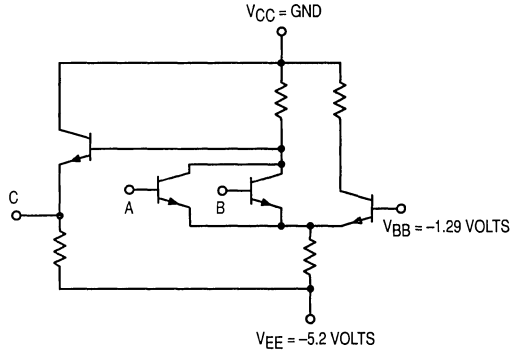


Figure 4.

Table 1.

Truth Table		
Inputs		Output
A	B	C
LO	LO	HI
LO	HI	LO
HI	LO	LO
HI	HI	LO

HI = –0.9 volts
LO = –1.7 volts

Table 2.

Negative Logic			Positive Logic		
Inputs		Output	Inputs		Output
A	B	C	A	B	C
1	1	0	0	0	1
1	0	1	0	1	0
0	1	1	1	0	0
0	0	1	1	1	0

Table 3.

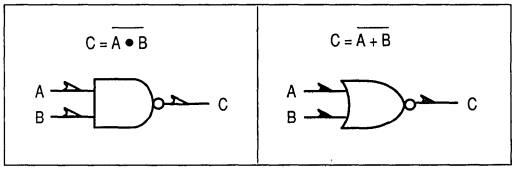


Figure 5a. Basic MECL Gate Circuit and Logic Function In Positive and Negative Nomenclature

LOGIC EQUIVALENCES

Binary logic must have two states to represent the binary 1 and 0. With ECL the typical states are a high level of - 0.9 volts and a low level of - 1.7 volts. Two choices are possible then to represent the binary 1 and 0. Positive logic defines the 1 or "true" state as the most positive voltage level, whereas negative logic defines the most negative voltage level as the 1 or "true" state. Because of the difference in definition of states, the basic ECL gate is a NOR function in positive logic and is a NAND function in negative logic.

Figure 5 more clearly shows the above comparison of functions. Table 1 lists the output voltage level as a function of the input voltage level of the MECL gate circuit shown Table 2 translates the voltage levels into the appropriate negative logic level which shows the function to be $C = \overline{A \times B}$; that is , the circuit performs the NAND function. Table 3 translates the equivalent positive logic function into $C = \overline{A + B}$, the NOR function.

Similar comparisons could be made for other positive logic functions. As an example, the positive OR function translates to the negative AND function. Figure 5b shows a comparison of several common logic functions.

Any function available in a logic family may be expressed in terms of positive or negative logic, bearing in mind the definition of logic levels. The choice of logic definition, as previously stated, is dependent on the designer. Motorola provides both positive and negative logic symbols on data sheets for the popular MECL 10,000 logic series.

SUMMARY

Conversion from one logic from to another or the use of a particular logic form need not be a complicated process. If the designer uses the logic form with which he is familiar and bears in mind the previously mentioned definition of levels, problems arising from definition of logic functions should be minimized.

REFERENCE

Y. Chu, Digital Computer Design Fundamentals
New York, McGraw-Hill, 1962

Inputs		Positive Logic					
A	**B**	**AND**	**OR**	**NAND**	**NOR**	**EXOR**	**COIN ***
LO	LO	LO	LO	HI	HI	LO	HI
LO	HI	LO	HI	HI	LO	HI	LO
HI	LO	LO	HI	HI	LO	HI	LO
HI	HI	HI	HI	LO	LO	LO	HI
A	**B**	**OR**	**AND**	**NOR**	**NAND**	**COIN ***	**EXOR**
Inputs		**Negative Logic**					

* Coincidence

Figure 5b. Comparative Positive and Negative Logic Functions

Technical Data

GENERAL CHARACTERISTICS AND SPECIFICATIONS

(See pages 1 - 5 through 1 - 7 for definitions of symbols and abbreviations.)

In subsequent sections of this Data Book, the important MECL parameters are identified and characterized, and complete data provided for each of the functions. To make this data as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as application information that applies to each family, are discussed in this section.

In general, the common characteristics of major importance are:

Maximum Ratings, including both dc and ac characteristics and temperature limits;

Transfer Characteristics, which define logic levels and switching thresholds;

DC Parameters, such as output levels, threshold levels, and forcing functions.

AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics. In addition, this section will discuss general layout and design guides that will help the designer in building and testing systems with MECL circuits.

LETTER SYMBOL AND ABBREVIATIONS

Throughout this section, and in the subsequent data sheets, letter symbols and abbreviations will be used in discussing electrical characteristics and specifications. The symbols used in this book, and their definitions, are listed on the preceding pages.

MAXIMUM RATINGS

The limit parameter beyond which the life of the devices may be impaired are given in Figure 6a. In addition, Figure 6b provides certain limits which, if exceeded, will not damage the devices, but could degrade the performance below that of the guaranteed specifications.

Characteristics	Symbol	Unit	MECL 10H	MECL 10K	MECL III
Power Supply	V_{EE}	Vdc	–8.0 to 0	–8.0 to 0	–8.0 to 0
Input Voltage (V_{CC} = 0)	V_{IN}	Vdc	0 to V_{EE}	0 to V_{EE}	0 to V_{EE}
Output Source Current Continuous	I_{OUT}	mAdc	50	50	40
Output Source Current Surge	I_{OUT}	mAdc	100	100	—
Storage Temperature	T_{sgt}	°C	–65 to + 150	–65 to + 150	–65 to + 150
Junction Temperature Ceramic Package (1)	T_J	°C	165	165	165 (2)
Junction Temperature Plastic Package (3)	T_J	°C	140	140	140

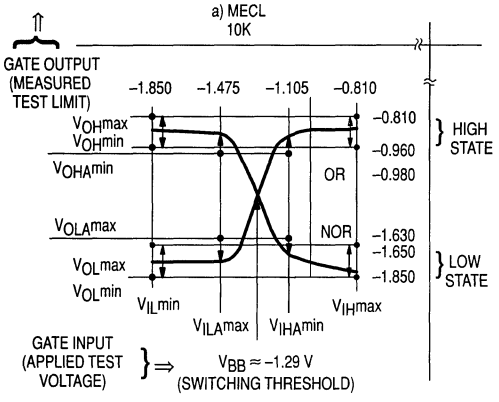
Figure 6a. Limits Beyond Which Device Life May Be Impaired

NOTES: 1. Maximum T_J may be exceeded (≤ 250°C) for short periods of time (≤ 240 hours) without significant reduction in device life.
2. Except 1670 which has a maximum junction temperature = 145°C.
3. For long term (≥ 10 yrs.) max T_J of 110°C required. Max T_J may be exceeded (≤ 175°C) for short periods of time (≤ 240 hours) without significant reduction in device life.

Characteristics	Symbol	Unit	MECL 10H	MECL 10K	MECL III
Operating Temperature Range Military (1)	T_A	°C	–55 to +125	–55 to +125	–55 to +125
Supply Voltage (V_{CC} = 0)	V_{EE}	Vdc	–4.94 to –5.46 (4)	–4.68 to –5.72 (2)	–4.68 to –5.72 (2)
Output Device Military	—	Ω	100 Ω to –2.0 Vdc	100 Ω to –2.0 Vdc	100 Ω to –2.0 Vdc (4)

Figure 6b. Limits Beyond Which Performance May Be Degraded

NOTES: 1. With airflow ≥ 500 lfpm.
2. Functionality only. Data sheet limits are specified for –5.2 V ± 5.0%.
3. Except 1648 which has an internal output pulldown resistor.
4. Functional and Data sheet limits.



TEST CONDITIONS: 25°C; V_{EE} = −5.2 V;
50 Ω MATCHED INPUTS AND OUTPUTS

Figure 7a. MECL 10K

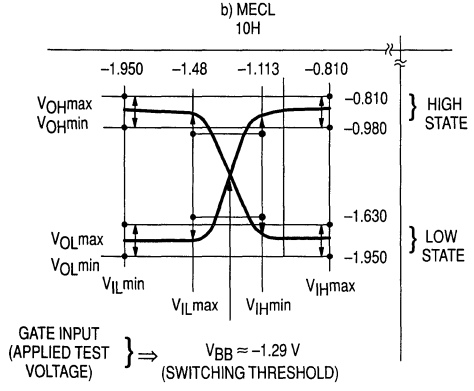


Figure 7b. MECL 10H

MECL TRANSFER CURVES

For MECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. Typical transfer curves and associated data for the MECL 10K/10H family are shown in Figures 7a and 7b respectively.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

The first set is obtained for 10K by applying test voltages, V_{IL}min and V_{IH}max (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between V_{OL}max and V_{OL}min, and V_{OH}max and V_{OH}min specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, V_{ILA}max, is applied to the gate and the NOR and OR output are measured to see that they are above V_{OHA}min and below the V_{OLA}max levels, respectively. Similar checks are made using the test input voltage V_{IHA}min.

The result of these specifications insures that:

a) The switching threshold (≈ V_{BB}) falls within the darkest rectangle; i.e. switching does not begin outside this rectangle;

b) Quiescent logic levels fall in the lightest shaded ranges;

c) Guaranteed noise immunity is met.

As shown in Figure 8, MECL 10K outputs rise with increasing ambient temperature. All circuits in each family have the same worst-case output level specifications regardless of power dissipation or junction temperature differences to reduce loss of noise margin due to thermal differences.

All of these specifications assume −5.2 V power supply operation. Operation at other power-supply voltages is possible, but will result in further transfer curve changes. Figure 9 gives rate of change of output voltages as a function of power supply.

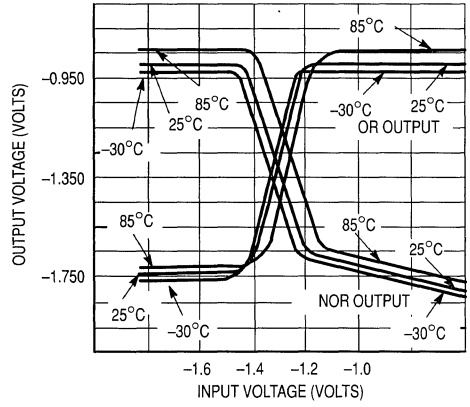


Figure 8. Typical Transfer Characteristics as a Function of Temperature (MECL 10K)

VOLTAGE	MECL 10H	MECL 10K	MECL III
$\Delta V_{OH}/\Delta V_{EE}$	0.008	0.016	0.033
$\Delta V_{OL}/\Delta V_{EE}$	0.020	0.250	0.270
$\Delta V_{BB}/\Delta V_{EE}$	0.010	0.148	0.140

Figure 9. Typical Level Change Rates

NOISE MARGIN

"Noise margin" is a measure of the logic circuit's resistance to undesired switching. MECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with the "A" subscript (V_{OHA}min, V_{OLA}max, V_{IHA}min, V_{ILA}max) in the transfer characteristic curves. MECL 10H is specified and tested with V_{OHA}min equal V_{OH}min, V_{OLA}max equal V_{OL}max, V_{IHA}min equal V_{IH}min and V_{ILA}max equal V_{IL}max. Guaranteed noise margin (NM) is defined as follows:

$NM_{HIGH\ LEVEL} = V_{OHA}\text{min} - V_{IHA}\text{min}$

$NM_{LOW\ LEVEL} = V_{ILA}\text{max} - V_{OLA}\text{max}$

To see how noise margin is computed, assume a MECL gate drives a similar MECL gate, Figure 10.

At a gate input (point B) equal to V_{ILA}max, MECL gate #2 can begin to enter the shaded transition region.

This is a "worst-case" condition, since the V_{OLA}max specification point guarantees that no device can enter the transition region before an input equal to V_{ILA}max is reached. Clearly then, V_{ILA}max is one critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, consider the output from MECL gate #1 (point A). What is the most positive value possible for this voltage (considering worst case specifications)? From Figure 10 it can be observed that the V_{OLA}max specification insures that the LOW state OR output from gate #1 can be no greater than V_{OLA}max.

Note that V_{OLA}max is more negative than V_{ILA}max.

Thus, with V_{OLA}max at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of V_{ILA}max on the transfer curve.)

In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input from V_{OLA}max to V_{ILA}max. This constitutes the "safety factor" known as noise margin. It can be calculated as the magnitude of the difference between the two specification voltages, or for the MECL 10K levels shown:

$NM_{LOW} = V_{ILA}\text{max} - V_{OLA}\text{max}$

$= -1.475\ V - (-1.630\ V)$

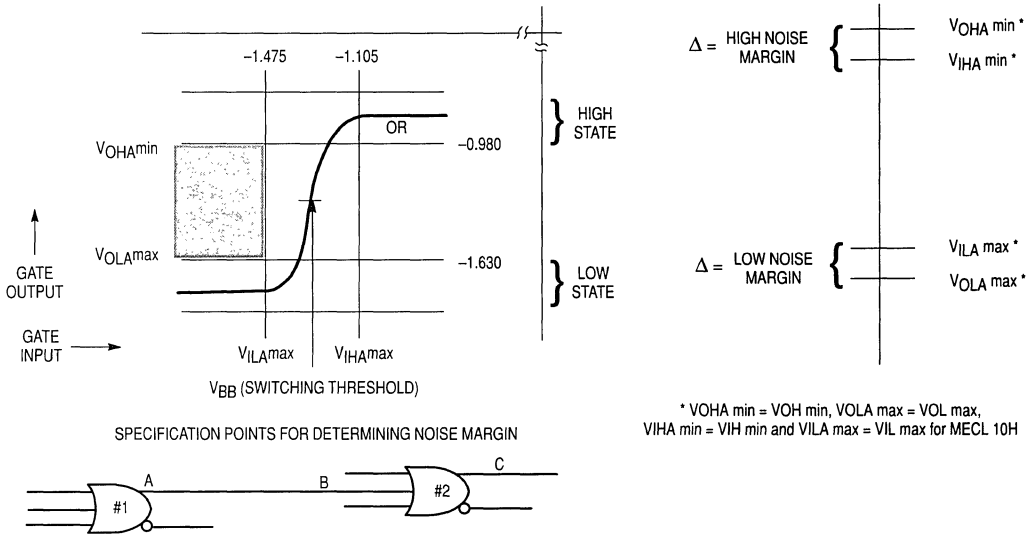
$= -155\ mV.$

Similarly, for a HIGH state:

$NM_{HIGH} = V_{OHA}\text{min} - V_{IHA}\text{min}$

$= -0.980\ V - (-1.105\ V)$

$= 125\ mV$



SPECIFICATION POINTS FOR DETERMINING NOISE MARGIN

* VOHA min = VOH min, VOLA max = VOL max, VIHA min = VIH min and VILA max = VIL max for MECL 10H

Figure 10. MECL Noise Margin Data

Analogous results are obtained when considering the "NOR" transfer data

Note that these noise margins are absolute worst case conditions. The lessor of the two noise margins is that for the HIGH state, 125 mV. This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances.

As shown in the table, typical noise margins are usually better than guaranteed – by about 75 mV. For MECL 10H the "noise margin" is 150 mV for NM low and NM high. (See Operational Data section of this chapter for details.)

Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on MECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise margin specifications, but also other circuit-related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state. In general, then, noise immunity involves line impedance, circuit output impedances, and propagation delay in addition to noise margin specifications. This subject to be discussed in greater detail in the MECL System Design Handbook HB205/D.

Family	Guaranteed Worst-Case dc Noise Margin (V)	Typical dc Noise Margin (V)
MECL 10H	0.150	0.270
MECL 10K	0.125	0.210
MECL III	0.115	0.200

Table 4. Noise Margin Computations

AC OR SWITCHING PARAMETERS

Time-dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit. They include the time delay involved in changing the output level from one logic state to another. In addition, they include the time required for the output of a circuit to respond to the input signal, designated as propagation delay, MECL waveform and propagation delay terminologies are depicted in Figure 11. Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent.

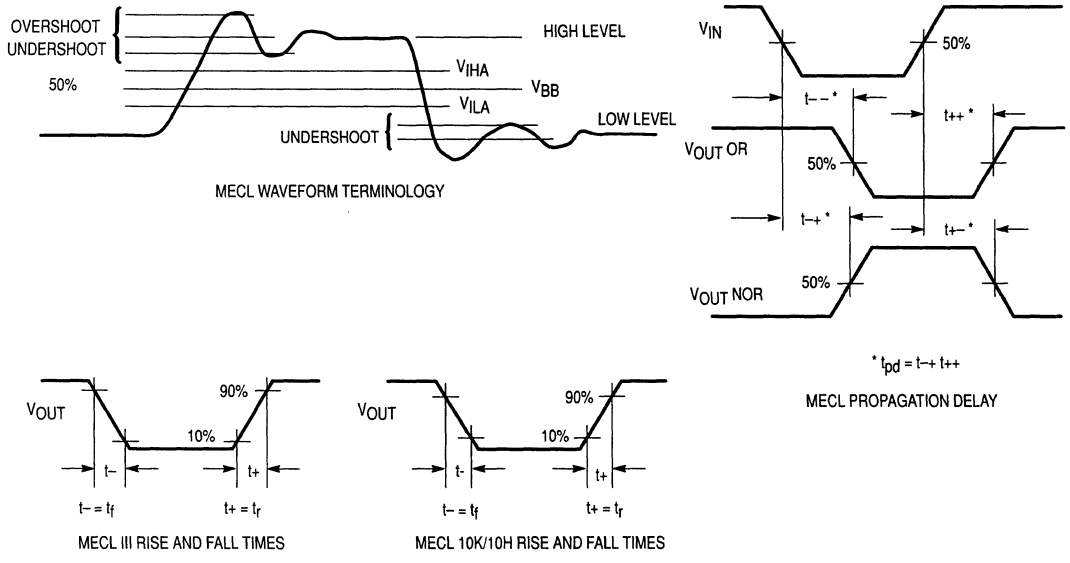


Figure 11. Typical Logic Waveforms

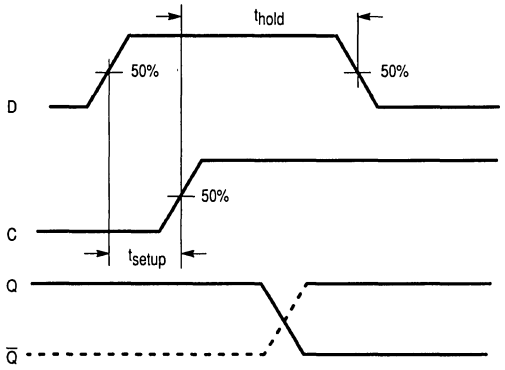


Figure 12. Setup and Hold Waveforms for MECL Logic Devices

SETUP AND HOLD TIMES

Setup and hold times are two ac parameters which can easily be confused unless clearly defined. For MECL logic devices, t_{setup} is the minimum time (50% – 50%) before the positive transition of the clock pulse (C) that information must be present at the Data input (D) to insure proper operation of the device. The t_{hold} is defined similarly as the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the Data input (D) to ensure proper operation. Setup and hold waveforms for logic devices are shown in Figure 12.

TESTING MECL 10H, MECL 10K AND MECL III

To obtain results correlating with Motorola circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 13.

This test circuit is the standard ac test configuration for most MECL devices. (Exceptions are shown with the device specifications.)

A solid ground plane is used in the test setup, and capacitors bypass V_{CC1}, V_{CC2}, and V_{EE} pins to ground. All power leads and signal leads are kept as short as possible.

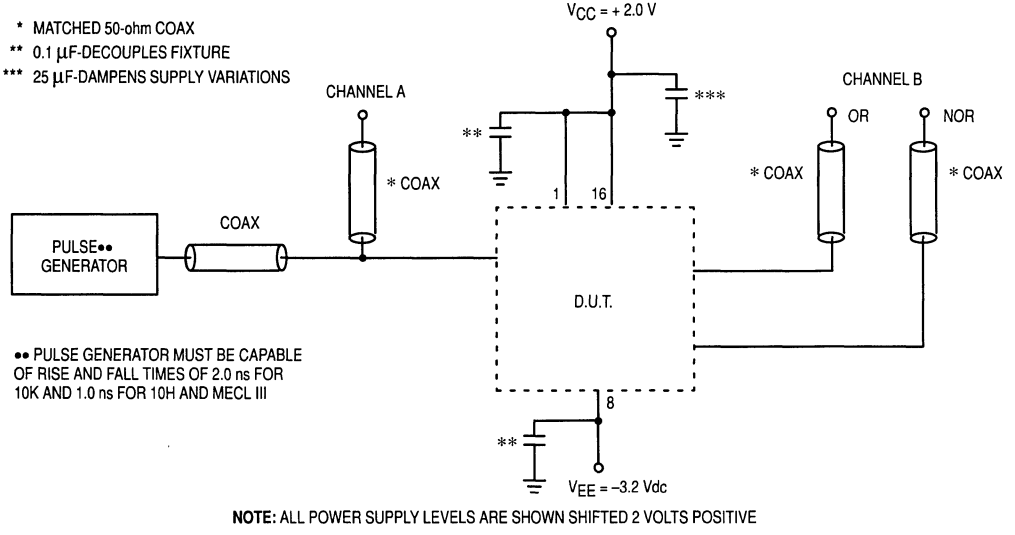
The sampling scope interface runs directly to the 50 ohm inputs of Channel A and B via 50-ohm coaxial cable. Equal-length coaxial cables must be used between the test set and the A and B scope inputs. A 50-ohm coax cable such as RG58/U or RG188A/U, is recommended.

Interconnect fittings should be 50-ohm GR, BNC, Selector Conhex, or equivalent. Wire length should be < 1/4 inch from T_{Pin} to input pin and T_{Pout} to output pin.

The pulse generator must be capable of 2.0 ns rise and fall times for MECL 10K and 1.5 ns for MECL 10H and MECL III. In addition, the generator voltage must have an offset to give MECL signal swings of ~ ±400 mV about a threshold of ~ + 0.7 V when V_{CC} = + 2.0 V and V_{EE} = –3.2 V for ac testing of logic devices.

The power supplies are shifted + 2.0 V, so that the device under test has only one resistor value to load into the precision 50-ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between Motorola and customer testing. Unused outputs loaded with a 100-ohm resistor. The positive supply (V_{CC}) should be decoupled from the test board by RF type 25 µF capacitors to ground. The V_{CC} pins are bypassed to ground with 0.1 µF, as is the V_{EE} pin.

Additional information on testing MECL 10K and understanding data sheets is found in Application Notes AN579/D and AN701/D.



NOTE: ALL POWER SUPPLY LEVELS ARE SHOWN SHIFTED 2 VOLTS POSITIVE

Figure 13. MECL Logic Switching Time Test Setup

1

POWER SUPPLY CONSIDERATIONS

MECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at – 5.2 V. While this MECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common-mode signal which is rejected by the differential action of the MECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity. Also, MECL 10H circuits may be operated with V_{EE} at – 4.5 V with negligible loss of noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The – 5.2 V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect. (Noise margins and performance specifications of MECL 10H are unaffected by variations in V_{EE} because of the internal voltage regulation.)

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by MECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0 μF and a 100 pF capacitor at the power entrance to the board, and a 0.01 μF low-inductance capacitor between ground and the –5.2 V line every four to six packages, are recommended.

Most MECL 10H, MECL 10K and MECL III circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross-coupling between individual circuits within a package when the outputs are driving heavy loads. Circuits with large drive capability, similar to the 10510, have two V_{CC1} pins. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

For further discussion of MECL power supply considerations to be made in system designing, see the MECL System Design Handbook.

POWER DISSIPATION

The power dissipation of MECL functional blocks is specified on their respective data sheets. This specification does not include power dissipation in the output devices due to output termination. The omission of the internal output pulldown resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

The table in Figure 14 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output-transistor power-dissipation value must be added to the specified package power dissipation for each external termination resistor used in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to – 2.0 Vdc	5.0	4.3
100 ohms to – 2.0 Vdc	7.5	6.5
75 ohms to – 2.0 Vdc	10	8.7
50 ohms to – 2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohm to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

Figure 14. Average Power Dissipation In Output Circuit External Terminating Resistors

LOADING CHARACTERISTICS

The differential input to MECL circuits offers several advantages. Its common-mode-rejection feature offers immunity against power-supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with MECL circuits does not normally present a design problem.

Graphs showing typical output voltage levels as a function of the load current for MECL 10H, MECL 10K and MECL III shown in Figure 15. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

MECL circuits typically have a 7 ohm output impedance and are relatively unaffected by capacitive loading on a positive-going output signal. However, the negative-going edge is dependent on the output pulldown or termination resistor. Loading close to a MECL output pin will cause an additional propagation delay of 0.1 ns per fanout load with a 50 ohm resistor to – 2.0 Vdc or 270 ohms to – 5.2 Vdc. A 100 ohm resistor to – 2.0 Vdc or 510 ohms to – 5.2 Vdc results in an additional 0.2 ns propagation delay per fanout load.

Terminated transmission line signal interconnections are used for best system performance. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are affected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{-1 + C_d/C_o}$. Here C_o is the normal intrinsic line capacitance, and C_d is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a MECL 10K transmission line vary with the line impedance. For example, with Z_O = 50 ohms, maximum stub length would be 4.5 inches (1.8 in. for MECL III). But when Z_O = 100 ohms, the maximum allowable stub length is decreased to 2.8 inches (1.0 in. for MECL III).

The input loading capacitance of a MECL 10H and MECL 10K gate is about 2.9 pF and 3.3 pF for MECL III. To allow for the IC connector or solder connection and a short stub length, 5 to 7 pF is commonly used in loading calculations.

UNUSED MECL INPUTS

The input impedance of a differential amplifier, as used in the typical MECL input circuit, is very high when the applied signal level is low. Under low-signal conditions, therefore, any leakage to the input capacitance of the gate could cause a gradual buildup of voltage on the input lead, thereby adversely affecting the switching characteristics at low repetition rates.

All single-ended input MECL logic circuits contain input pulldown resistors between the input transistor bases and V_{EE}. As a result, unused inputs may be left unconnected (the resistor provides a sink for I_{CBO} leakage currents, and inputs are held sufficiently negative that circuits will not trigger due to noise coupled into such inputs). Input pulldown resistors values are typically 50 kΩ and are not to be used as pulldown resistors for preceding open-emitter outputs.

Some MECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the V_{BB} pin provided and the other input goes to V_{EE}.

MECL circuits do not operate properly when inputs are connected to V_{CC} for a HIGH logic level. Proper design practice is to set a HIGH level as about – 0.9 volts below V_{CC} with a resistor divider, a diode drop, or an unused gate output.

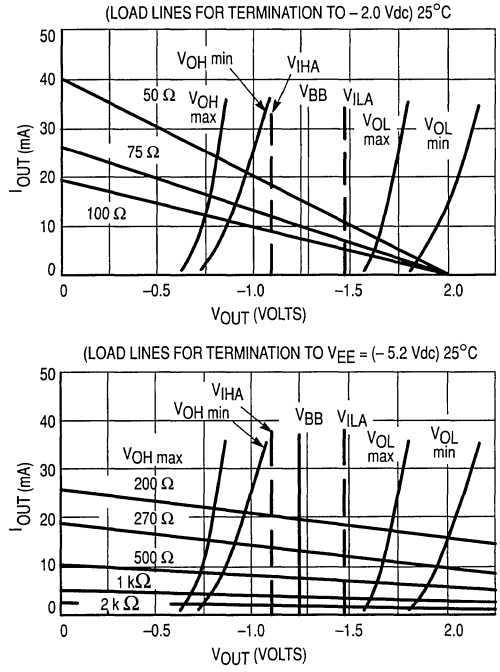


Figure 15. Output Voltage Levels versus DC Loading

1

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipation in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit – from the junction region to the ambient environment. The basic formula (a) for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\overline{\varnothing}_{JC} + \overline{\varnothing}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\overline{\varnothing}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature

T_A = maximum ambient temperature

P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation on Page 1-14).

$\overline{\varnothing}_{JC}$ = average thermal resistance, junction to case

$\overline{\varnothing}_{CA}$ = average thermal resistance, case to ambient

$\overline{\varnothing}_{JA}$ = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) MECL 10K devices.

Only two terms on the right side of the equation (1) can be varied by the user – the ambient temperature and the device case-to ambient thermal resistance, $\overline{\varnothing}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\overline{\varnothing}_{CA}$ thermal resistance term. $\overline{\varnothing}_{JC}$ is essentially independent of the air flow and external mounting method, but is sensitive to package material, die bonding method and die area.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D(\overline{\varnothing}_{JC}) \quad (3)$$

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Figure 16. In Figure 17, this basic data is converted into graphs showing maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in different packages, taking into account the maximum permissible operating junction temperature for long term life (≥ 100,000 hours for ceramic packages).

Thermal Resistance in Still Air										
Package Description							θ_{JA} (°C/Watt)		θ_{JC} (°C/Watt)	
No. Leads	Body Style	Body Material	Body WxL	Die Bond	Die Area (Sq. Mils)	Flag Area (Sq. Mils)	Avg.	Max.	Avg.	Max.
8	DIL	ALUMINA	1/4"x3/8"	SILVER/GLASS	2496	N/A	140	182	35	56
14	FLAT	ALUMINA	1/4"x1/4"	SILVER/GLASS	4096	N/A	165	215	28	45
14	DIL	ALUMINA	1/4"x3/4"	SILVER/GLASS	4096	N/A	100	130	25	40
16	FLAT	BEO	1/4"x3/8"	SILVER/GLASS	4096	N/A	88	114	13	21
16	FLAT	ALUMINA	1/4"x3/8"	SILVER/GLASS	4096	N/A	140	182	24	38
16	DIL	ALUMINA	1/4"x3/4"	SILVER/GLASS	4096	N/A	100	130	25	40
20	PLCC	EPOXY	0.035"x0.035"	EPOXY	4096	14,400	74	82	N/A	N/A
24	FLAT	BEO	3/8"x5/8"	SILVER/GLASS	8192	N/A	40	52	6	10
24	FLAT	ALUMINA	3/8"x5/8"	SILVER/GLASS	8192	N/A	64	83	11	18
24	DIL (6)	ALUMINA	1/2"x1-1/4"	SILVER/GLASS	8192	N/A	50	65	10	16
28	LCC	EPOXY	0.45"x0.45"	EPOXY	7134	28,900	65	68	N/A	N/A

Figure 16. Thermal Resistance Values For Standard MECL I/C Packages

AIR FLOW

The effect of air flow over the packages on $\overline{\varnothing}_{JA}$ (due to a decrease in $\overline{\varnothing}_{CA}$) is illustrated in the graphs of Figure 18. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual-in-line packaged MECL 10K quad OR/NOR gate (10501L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet per minute. From Figure 18, $\overline{\varnothing}_{JA}$ is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following maximum junction temperature results:

$T_J = P_D(\overline{\varnothing}_{JA}) + T_A$

$T_J = (0.195\ W)(50°C/W) + 25°C = 34.8°C$

Under the above operating conditions, the MECL 10K quad gate has its junction elevated above ambient temperature by only 9.8°C.

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperature as the air passes over the devices, or differences in ambient temperature between two devices.

The majority of MECL 10H, MECL 10K, and MECL III users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last package is a function of the air flow rate and individual package dissipation. Figure 19 provides gradient data at power levels of 200 mW, 250 mW, 300 mW, and 400 mW with air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual-in-line package as the air passes over each device. For higher rates of flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

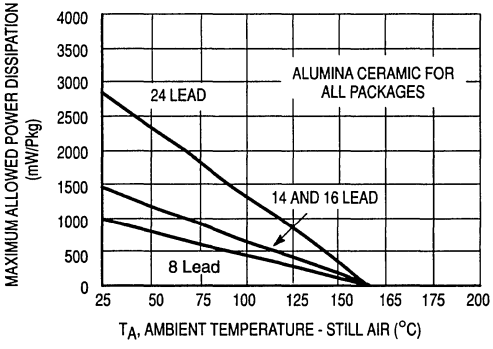


Figure 17a. Ambient Temperature Derating Curve (Ceramic Dual-in-Line Package)

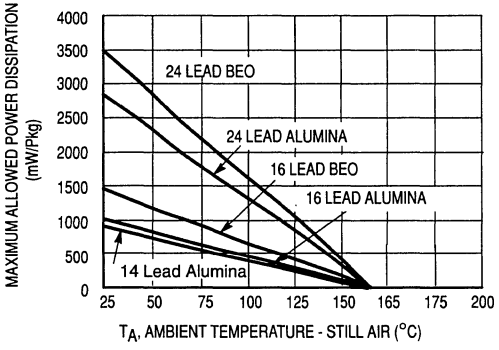


Figure 17b. Ambient Temperature Derating Curve (Ceramic Flat Package)

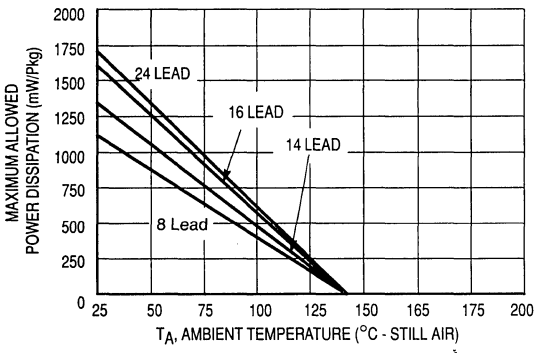


Figure 17c. Ambient Temperature Derating Curves (Plastic Dual-in-Line Package)

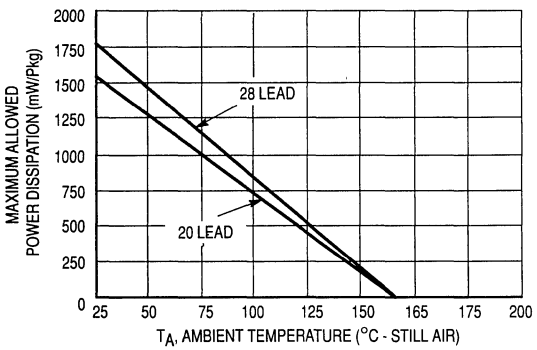


Figure 17d. Ambient Temperature Derating Curves (LCC Package)

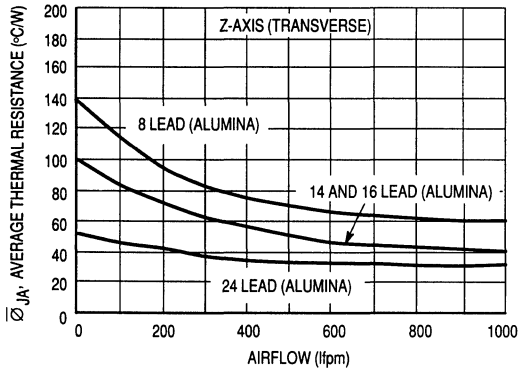


Figure 18a. Airflow versus Thermal Resistance (Ceramic Dual-in-Line Package)

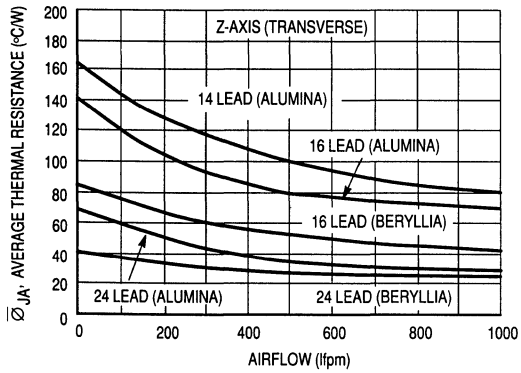


Figure 18b. Airflow versus Thermal Resistance (Ceramic Flat Package)

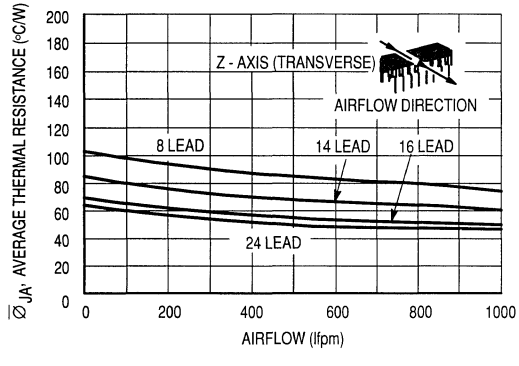


Figure 18c. Airflow versus Thermal Resistance (Plastic Dual-in-Line Package)

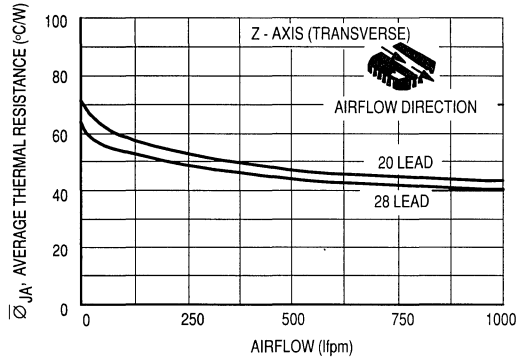


Figure 18d. Airflow versus Thermal Resistance (LCC Flat Package)

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Figure 19. Thermal Gradient of Junction Temperature (16 Pin MECL Dual-in-Line Package)

Devices mounted on 0.062" PC board with Z axis spacing of 0.5".
Air flow is 500 lfpm along Z axis.

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10K, 10H, and PLL devices are given for an operating temperature range from – 55°C to + 125°C. These values are based on having an air flow of 500 lfpm over the socket or P/C board mounted packages with no special heat sinking (i.e., dual-in-line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non-metallized area of P/C board).

The designer may want to use MECL devices under conditions other than those given above. The majority of the low-power device types may be used without air and with higher $\overline{\varnothing}_{JA}$. However, the designer must bear in mind that junction temperatures will be higher for higher $\overline{\varnothing}_{JA}$, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual-in-line ceramic device operated at $\overline{\varnothing}_{JA}$ = 100°C/W (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 lfpm air flow and a $\overline{\varnothing}_{JA}$ = 50°C/W. (Level shift = ΔT_J x 1.4 mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and $\overline{\varnothing}_{JA}$), noise margins are somewhat reduced. Therefore, the system designer must lay out the system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heat sinking are intended to provide the designer with sufficient information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEAT SINK SUGGESTIONS

With large high-speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer allows the use of microstrip line techniques to provide transmission line interconnections.

Two-sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal line must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time maybe used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two-ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 20, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug-in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

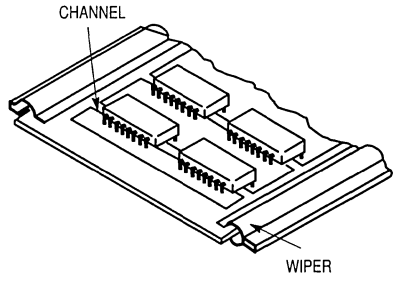


Figure 20. Channel/Wiper Heat Sinking on Double Layer Board

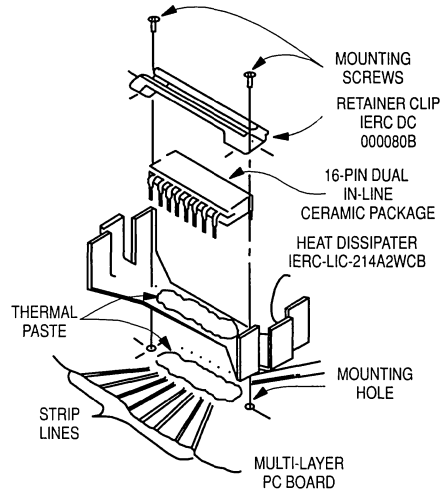


Figure 21. MECL High-power Dual-in-Line Package Mounting Method

For operating some of the higher power device types* in 16 lead dual-in-line packages in still air, requiring $\overline{\varnothing}_{JA}$ < 100°C/W, a suitable heat sink is the IERC-LIC-214A2WCB shown in Figure 21. This sink reduces the still air $\overline{\varnothing}_{JA}$ to around 55°C/W. By mounting this heat sink directly on a copper ground plane (using silicone paste) and passing 500 lfpm air over the packages, $\overline{\varnothing}_{JA}$ is reduced to approximately 35°C/W, permitting use at higher ambient temperatures or in lowering T_J for improved reliability.

It should be noted that the use of a heat sink on the top surface of the dual-in-line package is not very effective in lowering the $\overline{\varnothing}_{JA}$. This is due to the location of the die near the bottom surface of the package. Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wire.

*1654, 1678, 10536, 10537 and 10582, Max P_D >800 mW.

INTERFACING MECL TO SLOWER LOGIC TYPES

MECL circuits are interfacable with most other logic forms. For MECL/TTL/DTL interfaces, when MECL is operated at the recommended – 5.2 volts and TTL/DTL at + 5.0 V supply currently available translator circuits, such as the 10524 and 10525, may be used.

For systems where a dual supply (– 5.2 V and + 5.0 V) is not practical, the 10H750 includes four single supply MECL to TTL translators, or a discrete component translator can be designed. For details, see MECL System Design Handbook (HB205/D). Such circuits can easily be made fast enough for any available TTL.

MECL also interfaces readily with MOS. With CMOS operating at + 5.0 V any of the MECL to TTL translators work very well, currently available translator circuits such as the 10H751 and 10H752 may be used.

Specific circuitry for use in interfacing MECL families to other logic types is given in detail in the MECL System Design Handbook.

Complex MECL 10K devices are presently available for interfacing MECL with MOS logic, MOS memories, TTL three-state circuits, and IBM bus logic levels. See Application Note AN720/D for additional interfacing information.

CIRCUIT INTERCONNECTIONS

Through not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high-speed logic cards. Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages. This is particularly beneficial with MECL III which has relatively fast (1.0 ns) rise and fall times. Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for MECL III layouts and are justified when operating MECL 10H and MECL 10K at top circuit speed, when high-density packaging is a requirement, or when transmission line interconnects are used.

Point-to-point back-plane wiring without matched line terminations may be employed for MECL interconnections if line runs are kept short. At MECL 10K speeds, this applies to line runs up to 6 inches, for MECL 10H and MECL III up to 1 inch (Maximum open wire lengths for less than 100 mV undershoot). But, because of the open-emitter outputs of MECL 10H, MECL 10K and MECL III circuits, pull-down resistors are always required. Several ways of connecting such pull-down resistors are shown in Figure 22.

Resistor values for the connector in Figure 22a may range from 270 ohms to kΩ depending on power and load requirements. (See MECL System Design Handbook.) Power may be saved by connecting pull-down resistors in the range of 100 ohm to 150 ohms, to – 2.0 Vdc, as shown in Figure 23b. Use of a series damping resistor, Figure 23c, will extend permissible lengths of unmatched-impedance interconnections, with some loss of edge speed.

With proper choice of series damping resistor, line lengths can be extended to any length,** while limiting overshoot and undershoot to a predetermined amount. Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance. The open emitter-follower outputs of MECL 10H, MECL III and MECL 10K give the system designer all possible line driving options.

One major advantage of MECL over saturated logic is its capability for driving matched-impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The MECL 10H and MECL 10K emitter-follower output transistors will drive a 100 ohm termination line terminated to – 2.0 Vdc. This is the equivalent current load of 22 mA in the HIGH logic state and 6 mA in the LOW state.

Parallel termination of transmission lines can be done in two ways. One, as shown in Figure 23a, uses a single resistor whose value is equal to the impedance (Z_O) of the line. A terminating voltage (V_{TT}) of – 2.0 Vdc must be supplied to the terminating resistor.

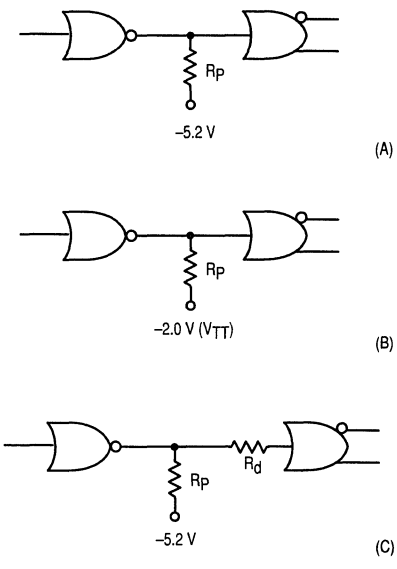


Figure 22. Pull-Down Resistor Techniques

Another method of parallel termination uses a pair of resistors, R_1 and R_2. Figure 23b illustrates this method. The following two equations are used to calculate the values of R_1 and R_2:

$R_1 = 1.6\ Z_O$

$R_2 = 2.6\ Z_O$

Another popular approach is the series-terminated transmission line (see Figure 24). This differs from parallel termination in that only one-half the swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

** Limited only by line attenuation and band-width characteristics.

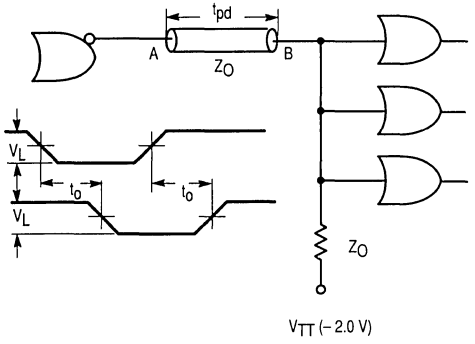


Figure 23a. Parallel Terminated Line

To maintain clean wave fronts, the input impedance of the driven gate must be greater than the characteristic impedance of the transmission line. This condition is satisfied by MECL circuits which have high impedance inputs. Using the appropriate terminating resistor (R_S) at point A (Figure 24), the reflections in the transmission line will be terminated.

The advantages of the series termination includes ease of driving multiple series-terminated lines, low power consumption, and low cross talk between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one-half logic swing present at intermediate points.

For board-to-board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantage of good noise immunity and low attenuation at high frequencies.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any MECL function may be connected to one end of the twisted pair line, and any MECL differential line receiver to the other as shown in the example, Figure 25. R_T is used to terminate the twisted pair line. The 1.0 to 1.5 V common-mode noise rejection of the line receiver ignores common-mode cross-talk, permitting multiple twisted pair lines to be tied into cables. MECL signals may be sent very long distances (> 1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made.

If timing is critical, parallel signals paths (shown in Figure 26) should be used when fanout to serve cards is required. This will eliminate distortion caused by long stub lengths off signal path.

Wire-wrapped connections can be used with MECL 10K. For MECL III and MECL 10H, the fast edge speeds (1.0 ns) create a mismatch at the wire-wrap connections which can cause reflections, thus reducing noise immunity. The mismatch occurs also with MECL 10K, but the distance between the wire-wrap connections and the end of the line is generally short enough so the reflections cause no problem.

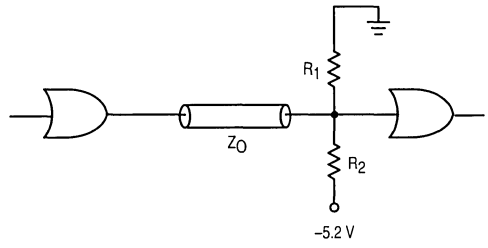


Figure 23b. Parallel Termination-Thevenin Equivalent

Series damping resistors may be used with wire-wrapped lines to extend permissible backplane wiring lengths. Twisted pair lines may be used for even longer distances across large wire-wrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single-ended, or differentially using a line receiver.

The recommended wire-wrapped circuit cards have a ground plane on one side and a voltage plane on the other side to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wire-wrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize cross talk between parallel paths in the signal lines. Point-to-point wire routing is recommended because cross talk will be minimized and line lengths will be shortest. Commercial wire-wrap boards designed for MECL 10K are available from several vendors.

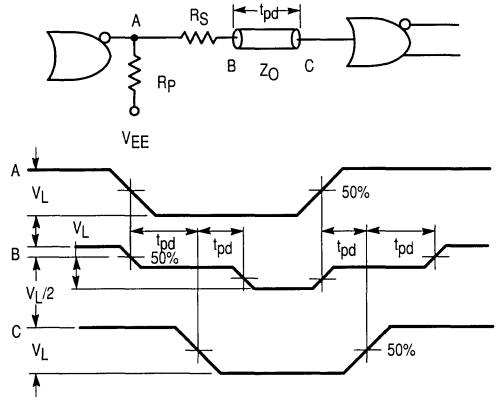


Figure 24. Series Terminated Line

MICROSTRIP AND STRIPLINE

Microstrip and stripline techniques are used with printed circuit boards to from transmission lines. Microstrip consists of a constant-width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 27). The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material.

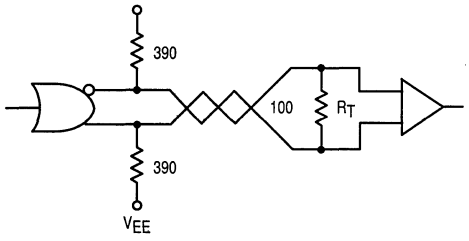


Figure 25. Twisted Pair Line Driver/Receiver

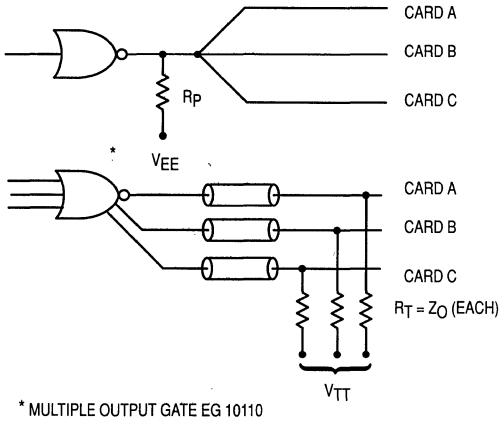


Figure 26. Parallel Fanout Techniques

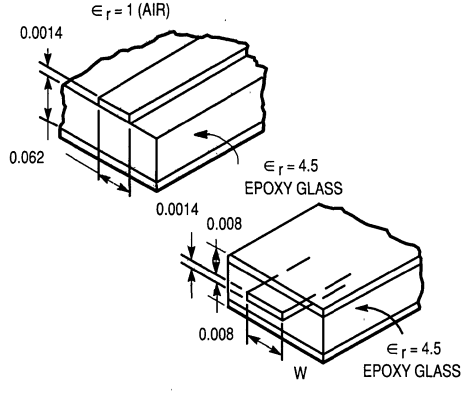


Figure 27. PC Interconnection Lines For Use With MECL

Stripline is used with multilayer circuit boards as shown in Figure 27. Stripline consists of a constant-width conductor between two ground planes.

Refer to MECL System Design Handbook for a full discussion of the properties and use of these.

CLOCK DISTRIBUTION

Clock distribution can be a system problem. At MECL 10K speeds, either coaxial cable or twisted pair line (using the 10501 and 10515) can be used to distribute clock signals throughout a system. Clock line lengths should be controlled and matched when timing could be critical. Once the clocking signals arrive on card, a tree distribution should be used for large-fanouts at high frequency. An example of this application technique is shown in Figure 28.

Because of the very high clock rates encountered in MECL III systems, rules for clocking are more rigorous than in slower systems.

The following guidelines should be followed for best results.

A. On-card Synchronous Clock Distribution via Transmission Line

1. Use the NOR output in developing clock chains or trees. Do not mix OR and NOR outputs in the chain.
2. Use balanced fanouts on the clock drivers.
3. Overshoot can be reduced by using two parallel drive lines in place of one drive line with twice the lumped load.
4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1.0 ns.
5. Parallel drive gates should be used when clocking repetition rates are high, or when high capacitance loads occur. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz bandwidth can be gained by paralleling two or three clock driver gates.
6. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid large lumped loads at the end of lines greater than 3 inches. A lumped load, if used, should be four or fewer loads.
7. For wire-OR (emitter dotting), two-way lines (busses) are recommended. To produce such lines, both ends of a transmission line are terminated with 100-ohms impedance. This method should be used when wire-OR connections exceed 1.0 inch apart on a drive line.

B. Off-Card Clock Distribution

1. The OR/NOR outputs of a 1660 may be used to drive into twisted pair lines or into flat, fixed-impedance ribbon cable. At the far end of the twisted pair a 1692 differential line receiver is used. The line should be terminated as shown in Figure 25. This method not only provides high speed, board-to-board clock distribution, but also provides system noise margin advantages. Since the line receiver operates independently of the V_{BB} reference voltage (differential inputs) the noise margin from board to board is also independent of temperature differentials.

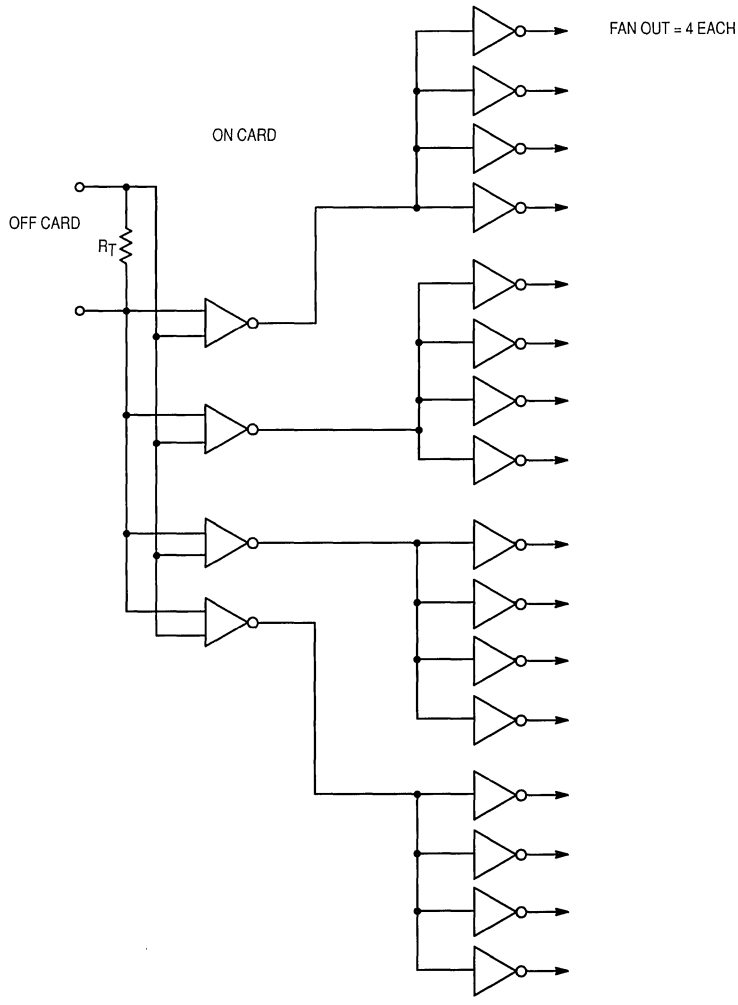


Figure 28. 64 Fanout Clock Distribution (Proper Termination Required)

LOGIC SHORTCUTS

MECL circuitry offers several logic design conveniences. Among these are:

1. **Wire-OR** (can be produced by wiring MECL output emitters together outside packages).
2. **Complementary Logic Outputs** (both OR and NOR are brought out to package pins in most cases).

An example of the use of these two features to reduce gate and package count is shown in Figure 29.

The connection shown saves several gate circuits over performing the same functions with non-ECL type logic. Also, the logic functions in Figure 29 are all accomplished with one gate propagation delay time for best system speed. Wire-ORing permits direct connections for MECL circuits to busses. (MECL System Design Handbook HB205/D and Application Note AN726/D).

Propagation delay is increased approximately 50 ps per wire-OR connection. In general, wire-OR should be limited to 6 MECL outputs to maintain a proper LOW logic level. The 10523 is an exception to this rule because it has a special V_{OL} level that allows very high fanout on a bus wire-OR line. The use of a single output pull-down resistor is recommended per wire-OR, to economize on power dissipation. However, two pull-down resistors per wire-OR can improve fall times and be used for double termination of busses.

Wire-OR should be done between gates in a package or nearby packages to avoid spikes due to line propagation delay. This does not apply to bus lines which activate only one driver at a time.

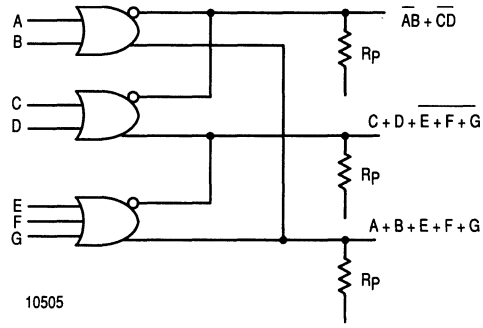


Figure 29. Use of Wire-OR and Complementary Outputs

System Considerations - A Summary of Recommendations

	MECL 10H	MECL 10K	MECL III
Power Supply Regulation	± 5.0% (1)	10% (2)	10% (2)
On-Card Temperature Gradient	20°C	Less Than 25°C	Less Than 25°C
Maximum Non-Transmission Line Length (No Damping Resistor)	1.0"	8.0"	1.0"
Unused Inputs	Leave Open (3)	Leave Open (3)	Leave Open (3)
PC Board	Multilayer	Standard 2-Sided or Multilayer	Multilayer
Cooling Requirements	500 lfpm Air	500 lfpm Air	500 lfpm Air
Bus Connection Capability	Yes (Wire-OR)	Yes (Wire-OR)	Yes (Wire-OR)
Maximum Twisted Pair Length (Differential Drive)	Limited By Cable Response Only, Usually >1000'	Limited By Cable Response Only, Usually >1000'	Limited By Cable Response Only, Usually >1000'
The Ground Plane to Occupy Percent Area of Card	>75%	>50%	>75%
Wire Wrap may be used	Not Recommended	Yes	Not Recommended
Compatible with MECL 10,000	Yes	–	Yes

(1) All dc and ac parameters guaranteed for $V_{EE} = -5.2\ V \pm 5.0\%$.
(2) At the devices (functional only).
(3) Except special functions without input pull-down resistors.

Family Overview

INTRODUCTION

Recent advances in bipolar processes have led to a proliferation of very high speed LSI and VLSI gate arrays in high end computer applications. The advent of these high speed arrays has created a need for a high speed logic family to tie or "glue" them together. Because arrays have a finite amount of circuitry and I/O pins, glue functions which are sensitive to either of these parameters may be better performed off the array. In addition glue functions which require very tight skew control may be difficult to perform on an array due to the inherent skew of the larger packages associated with large gate arrays. Therefore although the trend is to push more and more of the logic onto the array, there are design constraints which make performing some of the logic, such as clock distribution, multiplexing, decoding, latching, memory addressing and translating, in glue an attractive alternative.

The high end computer segment is not the only market segment pushing for higher performance logic parts. ATE, instrumentation and communication designs can have data rate requirements ranging from 300 MHz to as high as 2.5 GHz. Because large high speed arrays do not always lend themselves to the passing high frequency signals on and off chip, portions of the designs must be realized with discrete logic. The current bipolar logic families are not capable of operating at these high frequencies.

To answer the call for a very high speed bipolar logic family Motorola has designed and produced the ECLinPS (ECL in Pico Seconds) logic family. The family was designed to meet the most stringent of system requirements in speed, skew and board density as well as maintaining compatibility to existing ECL families.

ECL DESIGN BENEFITS

The speed benefits of an ECL design over those of alternative logic technologies are well documented, however there are a number of other important features that make ECL an attractive technology for system designs. The ECLinPS logic family as with other ECL families afford the following advantages:

COMPLEMENTARY OUTPUTS

Complimentary outputs are available on many functions with equal propagation delays between the two paths. This alleviates the need for external inverters and saves system power and board space while maintaining exceptional system timing.

TRANSMISSION LINE DRIVE CAPABILITY

The low output impedance, high input impedance and high current drive capability of ECL makes it an ideal technology for driving transmission lines. Regardless of the technology, as a system speeds increase, interconnect becomes more of a transmission line phenomenon. With ECL no special line driving devices are necessary as all ECL devices are line drivers.

CONSTANT POWER SUPPLY CURRENT DRAIN

Because of the differential amplifier design used for ECL circuits the current is not switched on and off but rather simply steered between two paths. Thus the current drain of an ECL device is independent of the logic state and the frequency of operation. Thus current stability greatly simplifies system power supply design.

INPUT PULLDOWN RESISTORS

ECL inputs have 50 kΩ-75 kΩ internal pulldown resistor which pull the input to V_{EE} (logic Low) when left open. This allows unused inputs to be left open and greatly simplifies logic design.

DIFFERENTIAL DRIVE CAPABILITY

Because of the presence of the high current drive complimentary outputs, ECL circuits are ideally suited for driving twisted pair lines or cables over long distances. With common mode noise rejection of 1 V or more ECL line receivers are less susceptible to common mode noise. In addition their differential inputs need only a few hundred millivolt voltage differences to correctly interpret the logic.

HIGH SPEED DESIGN PHILOSOPHY

Today a truly high speed logic family needs more than simply short propagation delays. The minimization of all types of skew as well as a level of logic density which affords a smaller amount of board space for equivalent function are also necessities of a high speed family. The following summary will outline the steps taken by Motorola to achieve these goals in the development of the ECLinPS logic family.

FAST PROPAGATION DELAYS

The ECLinPS family boasts 500 ps maximum packaged gate delays and typical flip-flop toggle frequencies of 1.4 GHz. Simple gate functions show typical propagation delays of 360 ps at 25 mW of power for a speed power product of only 9 pJ. For higher density devices internal gates run at 100 ps with 5 mW of power for a speed of power product of only 0.5 pJ.

INTERNAL DIFFERENTIAL INTERCONNECT

The propagation delay window size, skew between rising and falling inputs and susceptibility to noise are all phenomena which are exacerbated by V_{BB} switching reference variation. By extensively using differential interconnects internal to the chip the ECLinPS family has been able to achieve superior performance in these areas.

PROPAGATION DELAY TEMPERATURE INSENSITIVITY

The variation of propagation delay through an ECLinPS device across temperature is typically less than 50 ps. This stability allows for faster designs due to tighter delay windows across temperature.

INPUT IMPEDANCE AND LOADING CAPACITANCE

The input structures of the ECLinPS family show a positive real impedance across the applicable input frequency range. This ensures that the system will remain stable and operate as designed over a wide range of input frequencies. The input loading capacitance typically measures only 1.5 pF and is virtually independent of input fanout as the device capacitance is less than 5% of the total. Because the propagation delay of a signal down a transmission line is adversely affected by loading capacitance, the overall system speed is enhanced.

INPUT BUFFERS

To minimize propagation delays in a system environment, inputs with a large internal fanout are buffered to minimize the loading capacitance on the transmission line.

HIGH LEVEL OF INTEGRATION

28 pin designs allow for the design of 9 bit functions for implementation in byte plus parity applications. Full byte plus parity implementation reduces total package count and saves expensive board space.

SPACE EFFICIENT PACKAGE

The surface mount CERQUAD package affords a high level of integration with a minimum amount of required board space. Quad layout of the package equalizes pin lengths thus minimizing the skew between similar internal paths.

FLOW THROUGH PIN ASSIGNMENT

Input and output pins have been laid out in a flow through pattern with the inputs on one side of the package and the outputs on the other. This flow through pattern helps to simplify the PC board layout operation.

MULTIPLE V_{CCO} PINS

To minimize the noise generated in simultaneous switching situations, a minimum of three single ended outputs per V_{CCO} has been employed in the family. Optimum placement of these V_{CCO}s also results in superior output to output skew.

ADVANCED BIPOLAR PROCESSING

The ECLinPS logic family is fabricated using Motorola's MOSAIC III process, a process which is two generations ahead of the process used in the development of the 10H family. The small geometries and feature size of the MOSAIC III process enables the ECLinPS logic family to boast of a nearly three fold improvement in speed at less than half the power of the existing ECL logic families.

The MOSAIC III process is a double polysilicon process which uses a unique self-alignment scheme for device electrode and isolation definition. The process feature self aligned submicron emitters as well as polysilicon base, collector and emitter electrodes. In addition polysilicon resistors, diodes and capacitors are available to minimize the parasitic capacitance of an ECL gate. Figure 30 shows a cross section for an NPN device using the MOSAIC III process.

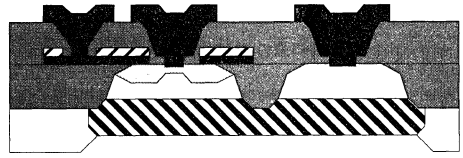


Figure 30. MOSAIC III Cross Section

By incorporating the use of polysilicon contacts and resistors through the MOSAIC III process, the parasitic capacitances of an ECLinPS gate are minimized, thus minimizing the time constants which comprise the switching delays of the gate. The resultant gates show delays of 100 ps for internal gates and 200 ps for output gates capable of driving 50 Ω loads. The small geometries of the process, nearly 350% reduction in device area compared to a 10H device, allow these internal gate delays to be achieved at only 800 μA of current.

UNIVERSAL COMPATIBILITY

Each member of the ECLinPS family is available in both of the existing ECL standards: 10 E series devices are compatible with the MECL 10H family; 100 E series devices are compatible with ECL 10K. In addition, to maintain compatibility with temperature compensated, three level series gated arrays, the 100 E devices are guaranteed to operate without degradation to a V_{EE} of –5.46 V.

The section below presents a comparison between the two standards in the new context of the ECLinPS family. The user is also referred to the Electrical Characteristics section of this book as well as appropriate family databooks and other literature for descriptive information on the earlier ECL families.

Because no supplier previous to Motorola has offered both ECL standards on an identical process, comparison of existing 10H and 10K style devices has some limitations. Comparison of the two standards fabricated with two different processes has sometimes led to the erroneous conclusion that there are inherent AC performance differences between them. In reality this is not the case. The only inherent difference between the two standards is the difference in the behavior of the DC characteristics with temperature.

AC PERFORMANCE

From an IC design standpoint, the only differences between a 10 E device and a 100 E device in the ECLinPS family are a small temperature compensation network in the 100 E output gate, and very minimal differences in the two bias generator networks. Therefore, one would expect that from an AC standpoint, the performance of the two standards in the ECLinPS family should be nearly identical; measurements prove this to be the case. There is no significant measurable difference in the rise/fall times, propagation delays or toggle frequencies when comparing a 10 E and a 100 E device. The minor difference between previous 10H and 10K designs is due to the fact that the two are fabricated on different processes, and in some cases are designed for operation at different power levels.

SUMMARY

Summarizing the above information; in general the two ECL design standards, although differing somewhat in DC parameters, are nearly identical when one compares the AC performance for a given device. There may be very small differences in the AC measurements due to the slightly smaller output swing of the 100E device. However, these differences are negligible when compared to the absolute value of the measurements. Therefore from an AC standpoint there is no real advantage in using one standard over the other, thus removing AC performance as a decision variable in high speed system design.

PACKAGING

During the definition phase of the ECLinPS family much attention was placed on the identification of a suitable package for the family. The package had to meet the criteria of minimum parasitics and propagation delays along with an attractive I/O versus board space relationship. Although the DIP package offered a level of familiarity and convenience, the performance of the package with a very high speed logic family was inadequate. In addition to the obvious parasitics and board space problems, the propagation delays through the DIP package were nearly twice as long as the delay through the silicon.

The 28 pin CERQUAD package emerged as the clear favorite both internally and with the high speed market in general. The package offers a quad layout to minimize both lead lengths and lead length differences. As a result, the parasitics and delays of the package are very well suited for a high speed logic family. In addition, the nearly matched lead lengths allow for tighter skew among similar paths through the chip.

The board density potential of the CERQUAD is also attractive in that it allows for a nearly 100% reduction in board space when compared to the DIP alternative. The package is approximately a half inch square with 50 mil spaced leads. More detailed measurements can be found in the package section of this databook.

Thermally the standard CERQUAD exhibits a θ_{JA} of 33.4°C per watt at 500 lfpm air flow. With this thermal resistance most 28 pin functions can be implemented with the MOSAIC III process without encountering any severe thermal problems.

Electrical Characteristics

PARAMETERS DEFINITIONS

The device data sheets in Chapter 5 contain specifications for the propagation delays for each of the devices in the ECLinPS family. In addition, where applicable, set-up/hold times and maximum toggle frequency (f_{max}) reset recovery and minimum pulse width specifications are also included. Table 5 in this section lists the rise/fall time specification for the family. The waveforms and terminologies used in describing the propagation delays and rise/fall times of the ECLinPS family are depicted in Figure 31.

Skew Times

In the design of high speed systems skew plays nearly as important a role as propagation delay. The majority of the devices in the ECLinPS family have the skew between outputs

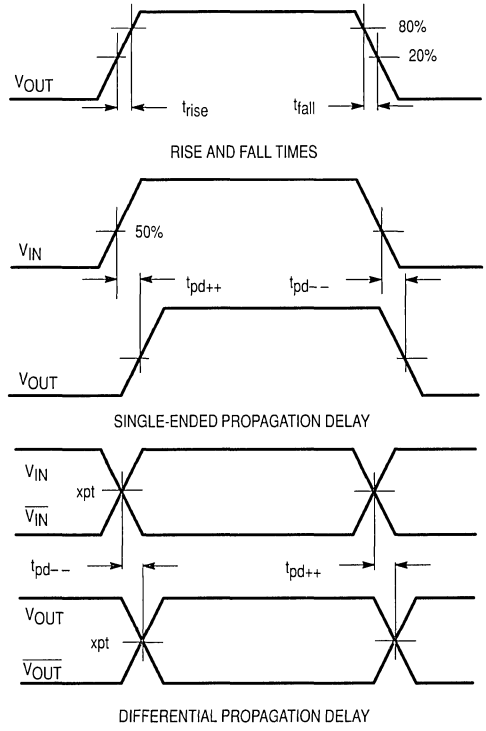


Figure 31. ECLinPS t_{pd} Measurement Waveforms

specified. This skew specification represents the typical difference between the dealys of similar paths on a single chip. No maximum value for skew is specified due to the difficulty in the production testing of this parameter. The user is encouraged to contact an ECLinPS application engineer to obtain actual evaluation data if this parameter is critical in their designs.

SET-UP AND HOLD TIMES

Propagation delays and rise/fall times are generally well understood parameters, however there is sometimes confusion surrounding the definition of the setup/hold and f_{max} parameters. Motorola defines the setup time of a device as the minimum time, prior to the transition of the clock, that an input must be stable to ensure that the device operates properly. The hold time, on the other hand, is defined as the minimum time that an input must remain stable after the transition of the clock to ensure that the device operates properly. Figure 32 illustrates the way in which Motorola defines setup and hold times.

Release Times

Release times are defined as the minimum amount of time an input must wait to be clocked after an enable, master reset or set signal is deactivated to ensure proper operation. Because more times than not this specification is in reference to a master reset operation this parameter is often called reset recovery time.

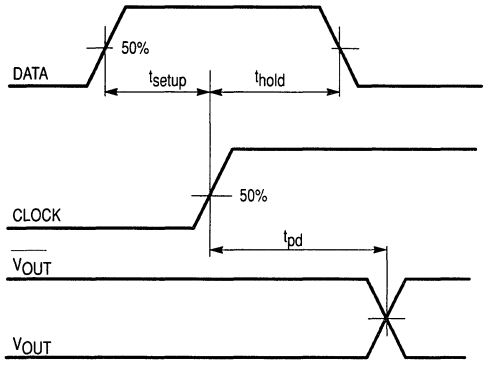


Figure 32. ECLinPS Set-Up and Hold Waveforms

f_{max} Measurement

In general f_{max} is measured in the manner shown in Figure 33 with the fail criterion being either a swing of 600 mV or less, or a miscount. However in some cases the feedback method of testing can lead to a pessimistic value of f_{max} because the feedback path delay is such that the setup times of the device are violated. If this is the case it is necessary to have two free running signal generators to ensure that the setup times are observed. This parameter, along with f_{shift} and f_{count}, represents the maximum frequency at which a particular flip flop, shift register or counter can be clocked with the divide, shift or count operation guaranteed. This number is generated from worst case operating conditions, thus under nominal operating conditions the maximum toggle frequency is higher.

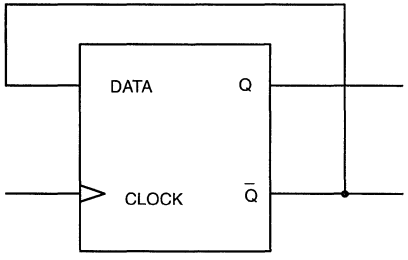


Figure 33. f_{max} Measurement

AC TESTING ECLinPS DEVICES

The introduction of the ECLinPS family raised the performance of silicon logic to a new domain. As the propagation delays of logic devices became ever faster the task of correlating between test setups becomes increasingly challenging. To obtain test results which correlate with Motorola, various testing techniques must be adhered to. A typical schematic for an ECLinPS test setup is illustrated in Figure 34. A solid ground plane is a must in the test setup, as the two power supplies are bypassed to this ground plane. A 20 μF capacitor from the two power supplies to ground is used to dampen any supply variations. An RF quality 0.01 μF capacitor from each power pin to ground is used to decouple the fixture.

These 0.01 μF capacitors should be located as close to the power pins as possible. In addition, all of the power leads should be kept as short as possible. The power supplies are shifted by + 2.0 V so that the load comprises only the precision 50 Ω input impedance of the oscilloscope. Use of this technique will assure that the customer and Motorola are terminating devices into equivalent loads and will improve test correlation. To further standardize testing, any unused outputs should be loaded with 50 Ω to ground.

Because the power supplies are shifted, the input levels must also be shifted by an equal amount. Table 5 gives the typical input levels for the ECLinPS family and their corresponding + 2.0 V shifted levels.

10 Exxx	Typical	Shifted
V_{IL}	– 1.75	+ 0.25
V_{IH}	– 1.90	+ 1.10
100 Exxx	**Typical**	**Shifted**
V_{IL}	– 1.70	+ 0.30
V_{IH}	– 0.95	+ 1.05

ECL Levels After Translating By +2.0 V

The test fixture should be in a controlled impedance 50 Ω environment, with any non-50 Ω interconnects, or stubs, kept as short as possible (< 1/4"). This controlled impedance environment will help to minimize overshoot and ringing, two phenomena which can lead to inaccuracies in AC measurements. To minimize degradation of the input and output edge rates, a 50 Ω coaxial cable with Teflon dielectric is recommended, however any other cable with a bandwidth of >5.0 GHz is adequate. In addition, the cables from the device under test (DUT) to the inputs of the scope should be matched in length to prevent any errors due to different path lengths from the DUT to the scope.

The interconnection fittings should be 50 Ω SMA straight or SMA launchers to minimize impedance mismatches at the interface of the coax and the test PC board. Although a Teflon laminate board is preferable, an FR4 laminate board is acceptable as long as the signal traces are kept to five inches or less. Longer traces will result in significant edge rate degradation of the input and output signals.

To make the board useful for incoming inspection or other volume testing the board needs to be fitted with a socket. Although not suitable for AC testing due to different pin lengths and large parasitics, there are through hole sockets which are adequate for CD testing of ECLinPS devices. For AC testing purposes a 28 pin surface mount socket is recommended.

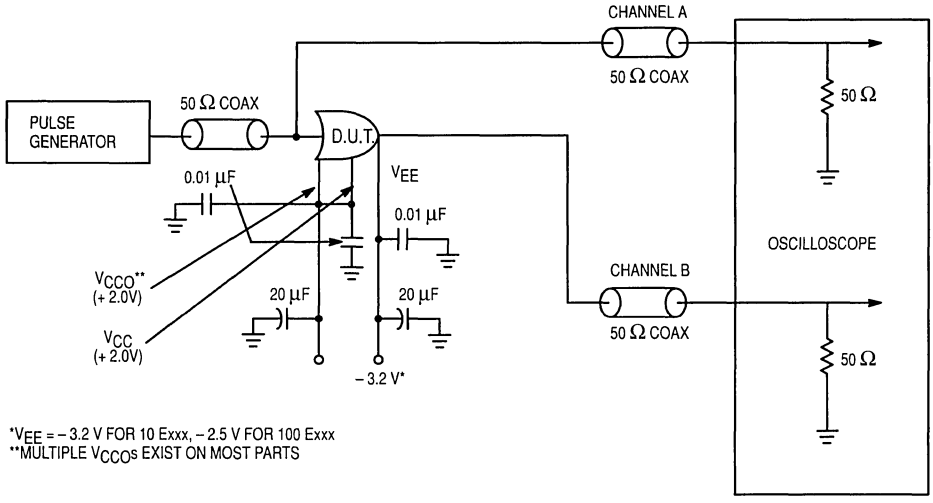


Figure 34. Typical ECLinPS Test Setup

Finally, to ensure correlation between Motorola and the customer, high performance state-of-the-art measuring equipment should be used. The pulse generator must be capable of producing the required input levels with rise and fall times of 500 ps. In addition, if f_{max} is going to be tested, a frequency of up to 1.5 GHz may be needed. The oscilloscope should also be of the utmost in performance with a minimum bandwidth of 5.0 GHz.

System Basics

POWER SUPPLY CONSIDERATIONS

The following text gives a brief description of the requirements and recommendation for treatment of power supplies in an ECLinPS system design. A more thorough narration on the general subject of power supplies can be found in the Motorola MECL System Design Handbook (HB205/D).

V_{CC} SUPPLY

As with all previous ECL families, the ECLinPS logic family is designed to operate with negative power supplies, in other words, with V_{CC} connected to ground. However ECLinPS circuits will work fine with positive power supplies as long as special care has been taken to ensure a stable, quiet V_{CC} supply. The output voltage levels for a positive supply system can be determined by simply subtracting the absolute value of the standard negative output levels from the desired V_{CC}.

To provide as small an AC impedance as possible, and minimize power bus IR drops, the V_{CC} supply should have a dedicated power plane. By providing a full ground plane in the system the designer ensures that the current return path for the signal traveling down a transmission line does not encounter any major obstructions. It is imperative that the noise and voltage drops be as small as possible on the V_{CC} plane as the internal switching references and output levels are all derived off of the V_{CC} power rail. Thus any perturbations on this rail could adversely affect the noise margins of a system.

$V_{EE} = V_{EE}$(min) to V_{EE}(max); $V_{CC} = V_{CCO}$ = GND											
		$T_A = 0°C$			$T_A = 25°C$			$T_A = 85°C$			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
t_r t_f	Output Rise/Fall Time (20 - 80%)	300		800	300		800	300		800	ps

Table 5. Family Output Edge Rate Specification

V_{EE} SUPPLY

To take advantage of increased logic density and temperature compensated outputs, many designers are building array options with both temperature compensated output levels and a –5.2 V V_{EE} supply. To alleviate any problems with interfacing these arrays to ECLinPS 100 E devices, Motorola has specified the operation of 100 E devices to include the standard 10H V_{EE} voltage range. Moreover, because of the superior voltage compensation of the bias network, this guarantee comes without any changes in the DC or AC specification limits. With the availability of both 10H and 10K compatible devices in the ECLinPS family there is generally no need to run 10 E devices at 10K voltage levels. If however this is desired, the 10 E devices will function at 100 E V_{EE} levels with, at worst, a small degradation in AC performance for a few devices due to soft saturation of the current source device.

Although both the 10 E and 100 E devices can tolerate variations in the V_{EE} supply without any detrimental effects, it is recommended that the V_{EE} supply also have a dedicated power plane. If this is not feasible, constraint care should be taken so that the IR drops of the V_{EE} bus do not create a V_{EE} voltage outside of the specification range. To provide the switching currents resulting from stray capacitances and asymmetric loading, the V_{EE} power supply in an ECL system needs to be bypassed. It is recommended that the V_{EE} supply be bypassed at each device with an RF quality .01μF capacitor to ground. In addition the supply should also be bypassed to ground with a 1 μF - 10 μF capacitor at the power inputs to a board. If a separate output termination plane is used, the V_{EE} supply will be of a static nature as the output switching current will return to ground via the V_{TT} supply, thus the bypassing of every device may be on the conservative side. If the design is going to include a liberal use of serial or Thevenin equivalent termination schemes a properly bypassed V_{EE} plane is essential.

V_{TT} SUPPLY

The output edge rates of the ECLinPS family necessitate an almost exclusive use of controlled impedance transmission lines for system interconnect (the details of this claim will be discussed in a latter section). Thus, unless Thevenin equivalent termination schemes are going to be used, a V_{TT} supply is a must in ECLinPS designs. The choice of using only Thevenin equivalent termination schemes to save a power supply should not be made lightly as the Thevenin scheme consumes up to ten times more power than the equivalent parallel termination to a –2.0V V_{TT} supply.

As was the case for the V_{EE} supply, a dedicated power plane, liberally bypassed as described above, should be used for the V_{TT} supply. In designs which rely heavily on parallel termination schemes the V_{TT} supply will be responsible for returning the switching current of the outputs to ground, therefore a low AC impedance is a must. For bypassing, many SIP resistor packs have bypass capacitors integrated in their design to supply the necessary bypassing of the supply. The use of SIP resistors will be discussed more thoroughly in a latter chapter.

HANDLING OF UNUSED INPUTS AND OUTPUTS

UNUSED INPUTS

All ECLinPS devices have internal 50 kΩ–75 kΩ pulldown resistors connected to V_{EE}. As a result, an input which is left open will be pulled to V_{EE} and thus set at a logic LOW. These internal pulldowns provide more than enough noise margin to keep the input from turning on if noise is coupled to the input, therefore there is no need to tie the inputs to V_{EE} external to the package.

In addition, by shorting the inputs to V_{EE} external to the package one removes the current limiting effect of the pulldown resistor and under extreme V_{EE} conditions the input transistor could be permanently damaged. If there are concerns about leaving sensitive inputs, such as clocks, open they should be tied low via an unused output or a quiet connection to V_{TT}.

Unless otherwise noted on the data sheets, the outputs to differential input devices will go to a defined state when the inputs are left open. This is accomplished via an internal clamp. Note that this clamp will only take over if the voltage at the inputs fall below ≈ – 2.5 V. Therefore if equal voltages of greater than – 2.5 V are placed on the inputs the outputs will attain an undefined midswing state.

Unlike saturating logic families, the inputs to an ECLinPS, or any ECL device, cannot be tied directly to V_{CC} to implement a logic HIGH level. Tying inputs to V_{CC} will saturate the input transistor and the AC and DC performance will be seriously impaired. A logic HIGH on an ECLinPS input should be tied to a level no higher than 600 mV below the V_{CC} rail and more typically no higher than the specified V_{IHmax} limit. A resistor or diode tree can be used to generate a logic HIGH level or more commonly an output of an unused gate can be used.

UNUSED OUTPUTS

The handling of unused outputs is guided by two criteria: power dissipation and noise generation. For single ended output devices it is highly recommended to leave unused outputs unterminated as there are no benefits in the alternative scheme. This not only saves the power associated with the output but also reduces the noise on the V_{CC} line by reducing the current being switched through the inductance of the V_{CC} pins. For the counters and shift registers of the family the count and shift frequencies will be maximized if the parallel outputs are left unterminated. Of course for applications where these parallel outputs are needed, this is not a viable alternative.

For the differential outputs, on the other hand, things are a little less cut and dry. If either of the outputs of a complimentary output pair is being used, both outputs of the pair should be terminated. This termination scheme minimizes the current being switched through the V_{CC} pin and thus minimizes the noise generated on V_{CC}. If, however, neither of the outputs of a complimentary pair are being used it makes most sense to leave these unterminated to save power. Note that the E511 device has special termination rules; these rules are outlined on the data sheet for the device.

MINIMIZING SIMULTANEOUS SWITCHING NOISE

A common occurrence among ECL families is the generation of crosstalk and other noise phenomena during simultaneous switching situations. Although the noise generated in ECL systems is minor compared to other technologies there are methods to even further minimize the problem.

Figure 35 illustrates the two output scenarios of an ECL device: differential outputs and single ended outputs. During switching, the current in the output device will change by ≈ 17 mA when loaded in the normal 50 Ω to – 2.0 V load. With differential outputs, as one output switches from a low to a high state, the other switches from high to a low state simultaneously thus the resultant current change through the V_{CCO} connection is zero. The current simply switches between the two outputs. However for the single ended output, the current change flows through the V_{CCO} connection of the output device. This current change through the V_{CCO} pin of the package causes a voltage spike due to the inductance of the pin.

Traditionally, manufacturers of ECL products have attempted to combat this problem by providing a separate V_{CC} pin for the output device (V_{CCO}, V_{CCA} etc.) and the internal circuitry. By doing this the noise generated on the V_{CCO} of the output devices would see a high impedance internal to the chip and not couple onto the the V_{CC} line which controls the output and internal bias levels. Unfortunately in practice the noise generated on the V_{CCO} would couple into the chip V_{CC} through the collector base capacitance of the output device, thus a large portion of the noise seen on the V_{CCO} line would also be seen on the V_{CC} line.

For the ECLinPS family and its associated edge speeds it was decided that multiple V_{CCO} pins would be necessary to minimize the inductance and the associated noise generation. A design rule was established so that there would be no more than three single ended outputs per V_{CCO} pin. Initially the V_{CC} and V_{CCO} pins were kept isolated from one another. However it was discovered that in certain applications the parasitics of the package and the output device would combine to produce an instability which resulted in the outputs going into an oscillatory state. To alleviate this oscillation problem it was necessary to make the V_{CC} and V_{CCO} metal common internal to the package. Subsequent evaluation showed that because of the liberal use of V_{CCO} pins the noise generated is equal to or less than that of previous ECL families.

To further reduce the noise generated there are some things that can be done at the system level. As mentioned above there should be adequate bypassing of the V_{CC} line and the guidelines for the handling of unused outputs should be followed. In addition, for wide single ended output devices an increase in the characteristic impedance of the transmission line interconnect will result in a smaller time rate of change of current; thus reducing the voltage glitch caused by the inductance of the package. This noise improvement should, of course, be weighed against the potential slowing of the higher impedance trace to optimize the performance of the entire system. In addition, the connection between the device V_{CC} pins and the ground plane should be as small as possible to minimize the inductance of the V_{CC} line. Note that a device mounted in a socket will exhibit a larger amount of V_{CC} noise due to the added inductance of the socket pins.

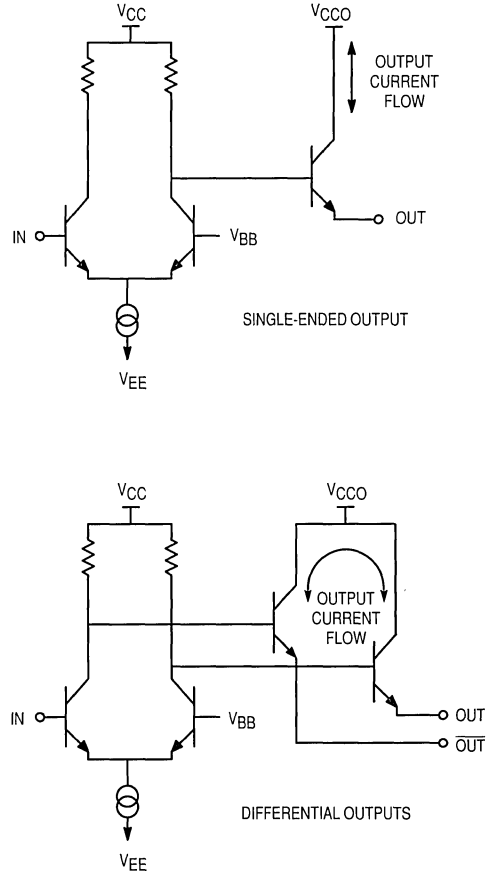


Figure 35. ECL Output Structures

EFFECTS OF CAPACITIVE LOADS

The issue of AC parametric shifts with load capacitance is a common concern especially with designers coming from the TTL and CMOS worlds. For ECLinPS type edge speeds wire interconnect starts acting like transmission lines for lengths greater than 1/2". Therefore in ECLinPS designs, for the majority of cases, the load on an output is seen by the transmission line and not the output of the driving device. The effects of load capacitance on transmission lines will be discussed in detail in the next section.

If the load is close to the driving output (<1/2"), the resulting degradation will be 15 - 25 ps/pF for both propagation delays and edge rates. In general, a capacitive load on an emitter follower has a greater impact on the falling edge than the rising edge. Therefore the upper end of the range given above represents the effect on fall times and the associated propagation delays while the lower end represents the effect on the rising output parameters. For ECLinPS devices the capacitive load produced by an input ranges from 1.2 pF to 2.0 pF. The majority (≈ 95%) of this capacitance is contributed by the package with very little added by the internal input circuitry. For this reason the range is generally a result of the difference between a corner and a center pin for the LCC package. A good typical capacitance value for a center pin is 1.4 pf and for a corner pin 1.7 pf. The capacitances for the other pins can be deduced through a linear interpolation.

WIRED-OR CONNECTIONS

The use of wired-or connections in ECL designs is a popular way to reduce total part count and optimize the speed performance of a system. The limitation of OR-tying ECL outputs has always been a combination of increased delay per OR-tie and the negative going disturbance seen at the output when one output switches from a high to a low while the rest of the outputs remain high. For high speed devices the latter problem is the primary limitation due to the increased sensitivity to this phenomena with decreasing output transition times. The following paragraph will attempt to describe the wire-OR glitch phenomena from a physical perspective.

Figure 36 illustrates a typical wire-OR situation. For simplicity the discussion will deal with only two outputs, however the argument could easily be expanded to include any number of outputs. If both the A and the B outputs start in the high state they will both supply equal amounts of current to the load. If the B output then transitions from a high to a low the line at the emitter of B will see a sudden decrease in the line voltage. This negative going transition on the line will continue downward at the natural fall time of the output until the A output responds to the voltage change and supplies the needed current to the load. This lag in the time it takes for A to correct the load current and return the line to a quiescent high level is comprised of three elements: the natural response time of the A output, the delay associated with the trace length between the two outputs and the time it takes for a signal to propagate through the package. The trace delay can be effectively forced to zero by OR-tying adjacent pins.

The resulting situation can then be considered "best case". In this best case situation, if the delay through the package is not a significant portion of the transition time of the output, the resulting negative going glitch will be relatively small (≈100 mV). A disturbance of this size will not propagate through a system. As the trace length between OR-tied outputs increases, the magnitude of the negative going disturbance will increase. Older ECL families specified the maximum delay allowed between OR-tied outputs to prevent the creation of a glitch which would propagate through a system.

As this glitch phenomena is a physical limitation, due to decreased edge rates, ECLinPS devices are susceptible to the problem to an even greater degree than previous slower ECL families. The package delay of even the 28-lead LCC is a significant portion of the transition times for an ECLinPS device. Therefore even in the best case situation described above one can expect an ≈ 200 mV glitch on the OR-tied line. A glitch of this magnitude will not propagate through the system but it is significantly worse than the best case situation of earlier ECL families. In fact as long as the distance between OR-tied outputs is kept less than 1/2" the resulting line disturbance will not be sufficient to propagate through most systems.

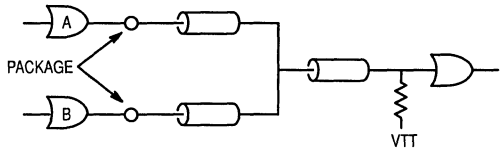


Figure 36. Typical Wire-OR Configuration

With this in mind the following recommendations are offered for OR-tying in ECLinPS designs. First OR-tying of clock lines should be avoided as even in the best case situation the disturbance on the line is significant and could cause false clocking in some situations. In addition wire ORed outputs should be from the same package and preferably should be adjacent pins. Non adjacent outputs should be within 1/2" of each other with the load resistor connection situated near the midpoint of the trace (Figure 36). By following these guidelines the practice of wire-ORing ECL outputs can be expanded to the ECLinPS family without encountering problems in the system.

A detailed discussion of wire-OR connections in the ECLinPS world of performance is beyond the scope of this text. For this reason a separate application note has been written which deals with this situation in a much more thorough manner. Anyone planning to use wire-OR connections in their ECLinPS design is encouraged to contact a Motorola representative to obtain this application note.

CLOCK DISTRIBUTION

Clock skew is a major contributor to the upper limit of operation of a high speed system, therefore any reduction in this parameter will enhance the overall performance of a system. Through the ECLinPS family and new offerings in the 10H family Motorola is providing devices uniquely designed to meet the demands of low skew clock distribution.

By far the largest contributor to system skew is the variation between different process lots of a given device. This variation is what defines the total delay window specified in the data sheets. This window can be minimized if the devices are fully differential due to the output level defined thresholds which ensure a "centered" input swing. The propagation delay windows of single ended ECL and other System Basics logic technologies are intimately tied to variations in the input thresholds. As illustrated in Figure 37 although the delays when measured from the threshold of the input to the 50% point of the output are equal; when measured from the specified 50% point of the input to the 50% point of the output the delays will vary with any

shift in the switching reference. Obviously the magnitude of the delay difference is also proportional to the edge rate of the input. In addition to increasing the size of the delay windows, this reference shift will cause the duty cycle of the output of a device to be different than that of the input. Unfortunately these thresholds are perhaps the most difficult aspects of a logic device to control.

As a result for the ultimate in low skew performance differential ECL devices are a must. A quick perusal of the ECLinPS portion of this databook will reveal a relatively large number of totally differential devices which will lend themselves nicely to very low skew applications such as clock distribution.

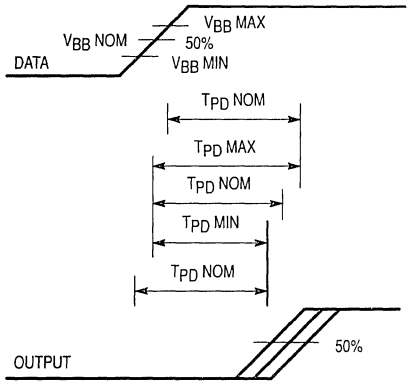


Figure 37. Delay versus Switching Reference Offset

In addition to these generic differential devices there are several devices which were designed exclusively for clock distribution systems. With past ECL families designers were forced to build clock distribution trees with devices which were compromises at best. The ECLinPS family, however, was built around the E511 clock distribution chip; a fully differential 1:9 fanout device which boasts within part skews as well as part to part skews unequaled in today's market.

Additionally, to further deskew clock lines the E595 programmable delay chip will be available. Although static delay lines can remove built in path length difference skew they can not compensate for variations in delays of the devices in the clock path. The E595 allows the user to delay a signal over a 2 ns range in 20 ps steps. Through the use of this device the designer can match skews between clocks to 20 ps.

Although these two devices satisfy the needs for many ECL designers they do overlook the needs of a special subset; the designer who mixes ECL and TTL technologies. When translating between ECL and TTL much of the skew performance gained through the E511 is lost when passed through the translator and distributed in TTL. To solve this problem a new set of translators have been introduced in the MECL 10H family. The 1041 and 1043 receive a differential ECL input and f an out nine TTL outputs with a guaranteed unparalleled skew between the TTL outputs. The 1040 and 1042 take differential ECL inputs and generate low skew TTL outputs which are ideal for driving clocks in 68030 and 68040 microprocessor systems. By using the ECL aspects of the E511 to distribute clock lines across the backplane to TTL cards and receiving and translating these signals with the 1040, 1041, 1042 or 1043 a TTL clock distribution tree can be designed with a performance level unheard of with past logic families.

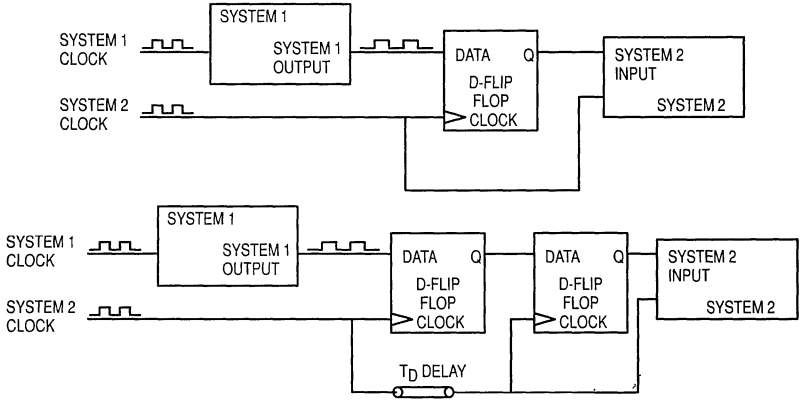


Figure 38. Clock Synchronization Schemes

Through the development of a library of differential devices, specialized low skew distribution chips and high resolution programmable delay chips Motorola has serviced the need for low skew clock distribution designs. These offerings open the door for even higher performance next generation machines.

METASTABILITY BEHAVIOR

The metastability behavior and measurement of a flip flop is a complicated subject and necessitates much more time than is available in this forum for a thorough explanation. As a result, the following description is of an overview nature. Anyone interested in a more thorough narration on the subject is encouraged to contact a Motorola representative to acquire the application note which contains a more detailed discussion on the subject.

In many designs occasions arise where an asynchronous signal needs to be synchronized to the system clock. Generally this task is accomplished with the use of a single or series of D flip-flops as pictured in Figure 38. Because the data signal and the clock signal are asynchronous the system designer cannot guarantee that the setup and hold specifications for the device will be met. This in and of itself would not cause a problem if it was not for the metastable behavior of a D flip-flop. The metastable behavior of a flip-flop is described by the outputs of a device attaining a non defined logic level or perhaps going into an oscillatory state when the data and the clock inputs to the flip flop switch simultaneously. It has been shown that this metastable behavior occurs across technology boundaries as well as across performance levels within a technology.

For ECL the characteristic of a flip-flop in a metastable state is a device whose outputs are in a non-defined state near the midpoint of a normal output swing. The output will return randomly to one of the two defined states some time later (Figure 39). The two parameters of importance when discussing metastability are the metastablity window; the window in time for which a transition on both the data and the clock will cause a metastable output, and the settling time; the time it takes for a metastable output to return to a defined state.

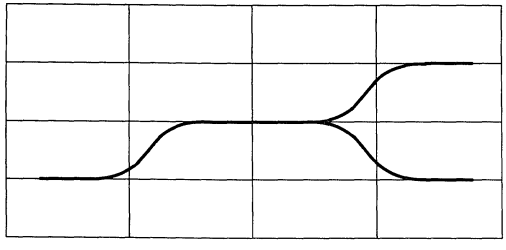


Figure 39. Metastable Behavior of an ECL Flip Flop

For the single flip flop design of Figure 37, the data being fed into system 2 will be in an undefined state and thus unusable if the synchronizing flip flop enters a metastable state. Because of this a more popular design incorporates multiple flip flop chains with cascading data inputs and clock inputs which are delayed with respect to each other. This redundancy of flip flops helps to reduce the probability that the data entering system 2 will be at an undefined level which could wreak havoc on the logic of that system. This reduction in probability relies on the fact that even if the preceding flip flop goes metastable it will settle to a defined state prior to the clocking of the following flip flop. Obviously, once the first flip flop goes metastable there is an even chance that it will settle in the wrong state and thus information will be lost. However, there are error detection and correction methods to circumvent this problem. The larger the flip flop chain the lower the probability of metastable data being fed into system 2.

Unfortunately for ECLinPS levels of performance both the window width and the settling time are difficult or impossible to measure directly. The metastable window for an ECLinPS flip flop is assuredly less than 5 ps and most likely less than 1 ps based on SPICE level simulation results. In either case, with today's measuring equipment it would be impossible to measure this window width directly. Although it is feasible to measure the settling time for a given occurrence, this parameter is not fixed but rather is of a variable length which makes it impossible to provide an absolute guarantee.

The challenge then becomes, how to characterize metastability behavior given the above circumstances. The standard method in the industry is to use Stoll's[1] equation, combined with the standard MTBF equation, to develop the following relationship:

$$MTFB = 1/(2 * f_C * f_D * T_P * 10^{-(\Delta t/\tau)})$$

where:

f_C: Clock Frequency
f_D: Data Frequency
T_P: FF Propagation Delay
Δt: Time Delay Between FF Clocks
τ: Time Delay Between FF Clocks

Note that the clock frequency, data frequency and time delay between flip flops are user defined parameters, thus it is up to Motorola to provide only the propagation delays and the resolution time constants for the ECLinPS flip flops.

The propagation delays are obviously already defined so this leaves only the resolution time constant yet to be determined. An evaluation fixture was fabricated and several ECLinPS flip flops were evaluated for resolution time constants. The results of the evaluation showed that the time constant was somewhat dependent on the part type as all the flip flops in the ECLinPS family do not use the same general design. The time constants range from 125 - 225 ps depending on the part type.

As an example, for a system with a 100 MHz clock and 75 MHz data rate the required delay between clock edges of a cascaded flip flop chain for the E551 register, assuming a τ of 200 ps, would be:

$$MTFB = 1/(2 * 100\ MHz * 75\ MHz * 800\ ps * 10^{-(\Delta t/200\ ps)})$$

where:

solving for an MTBF of 10 years yields:

Δt: = 3.1 ns therefore:

$T_D = \Delta t: + T_P = 3.9$ ns

So for an MTBF of 10 years, for the above situation, the second flip-flop should be clocked 3.9 ns after the first. Similar results can be found by applying the equation to different data and clock rates as well as different acceptable MTBF rates.

[1]Stoll, P. "How to Avoid Synchronization Problems," VLSI Design. November/December 1982. pp. 56 - 59.

System Interconnect

INTRODUCTION

As mentioned earlier, edge rates of the ECLinPS family are such that most interconnects must be treated as transmission lines. Thus, a controlled impedance environment is necessary to produce predictable interconnect delays as well as limiting the reflection phenomena of undershoot and overshoot. The three most common techniques for circuit and/or system interconnect at high data rates are microstrip, stripline and coaxial cable; both microstrip and stripline are printed circuit board methods whereas coaxial cable is most often used for interconnecting different parts of a system which are separated by relatively large distances. For slower speed applications (<300MHz) a twisted pair scheme also works well. The scope of writing will not include the twisted pair technique, however a detailed discussion of this topic can be found in the MECL System Design Handbook. Finally, wirewrap boards are not recommended for the ECLinPS family because the fast edge speeds exceed the capabilities of normal wirewrapped connections. Mismatches at the connections cause reflections which distort the fast signal, significantly reducing the noise immunity of the system and perhaps causing erroneous operation.

PRINTED CIRCUIT BOARDS

Printed circuit boards (PCB's) provide a reliable and economical means of interconnecting electrical signals between system components. Printed circuit boards consist of a dielectric substrate over which the conducting printed circuit material is placed. Three major categories of printed circuit boards exist:

1. Single-sided boards
2. Double-sided boards
3. Multilayer boards

The most common printed circuit board material used for digital designs is a glass-epoxy laminate. These boards use fiberglass dielectric with copper foils bonded to both sides of the dielectric material by an epoxy resin. Other substrate materials include fiberglass dielectric with a polyimide resin and fiberglass dielectric with a teflon resin. For multilayer boards the inner layers are separated by sheets of prepreg which acts as both a dielectric material and a bonding agent between layers.

The choice of substrate material depends on the function for which the board will be used, the environment in which the board is to operate, and costs. Table 6 lists several physical qualities which characterize several of the available PCB types. Each available substrate material has its own properties which makes it ideally suited for particular applications.

GLASS-EPOXY

Possesses good moisture absorption, chemical, and heat resistance properties as well as mechanical strength over standard humidity and temperature ranges. The most widely used versions are G10 and FR4, the fire resistant version of G10.

GLASS-POLYIMIDE

Good for elevated temperature operation because of its tight tolerance of the coefficient of thermal expansion. Very hard material, so it may damage drilling equipment when being drilled.

GLASS-TEFLON

Good for use when a low dielectric material is required. Very soft material, so it may be difficult to build features requiring precise geometries. Relatively expensive material.

MICROSTRIP

A microstrip line is the easiest printed circuit interconnect to fabricate because it consists simply of a ground plane and flat signal conductor separated by a dielectric (Figure 40)

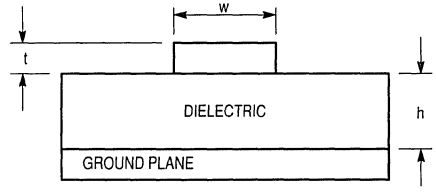


Figure 40. Microstrip Line

The characteristic impedance, Z_O, of a microstrip line is given by:

$$Z_O = \frac{87}{\sqrt{(\varepsilon_r + 1.41)}} \ln\left[\frac{(5.98 * h)}{(0.8w + t)}\right] \quad \text{(eqt. 1)}$$

where:

ε_r = Relative Dielectric Constant of the Substrate
w = Width of the Signal Trace
t = Thickness of Signal Trace
h = Thickness of the Dielectric

Equation 1 is accurate to within ±5% when:

$$0.1 < w/h < 3.0 \text{ and } 1 < \varepsilon_r < 15$$

Material	Dielectric Constant	Dissipation Factor	Thermal Coefficient of Expansion	Tensile Modulus
Glass-Epoxy	4.8 (1MHz)	0.022 (1MHz)	13 - 16 (10^{-6}/°C)	2.5
PTFE	2.1 (10GHz)	0.0004 (10GHz)	224 (10^{-6}/°C)	0.05
Glass-Polyimide	4.5 (1MHz)	0.10 (1MHz)	12 - 14 (10^{-6}/°C)	2.8

Table 6. Characteristics of Common PCB Materials

To mitigate the effects of electric field fringing, an additional constraint is that the width of the ground plane be such that it extends past each edge of the signal line by at least the width of the signal line.

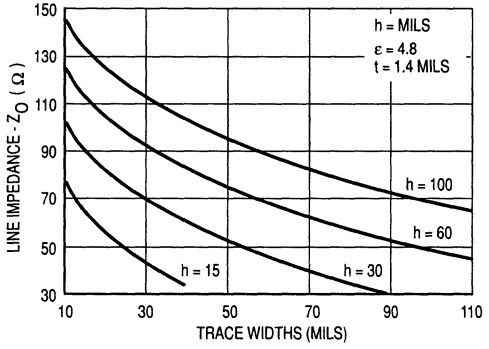
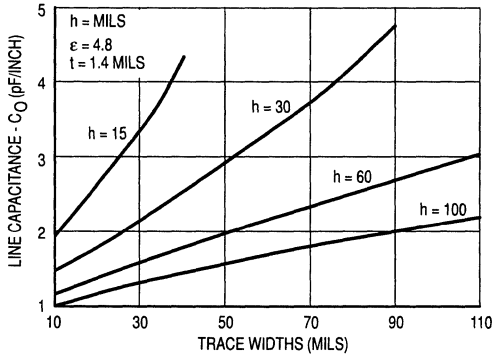


Figure 41. Microstrip Impedance versus Trace Width



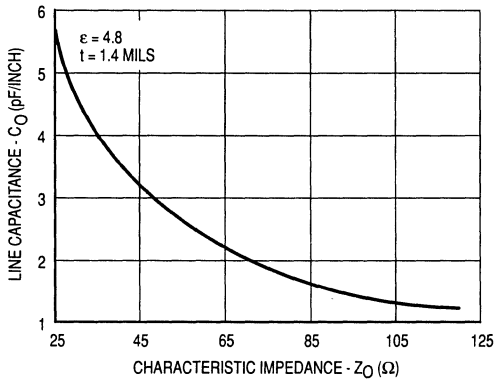


Figure 42. Line Capacitance versus Line Impedance and Trace Width

Figure 41 is a plot of characteristic impedance as a function of trace width and dielectric thickness for a dielectric constant of 4.8 and a trace thickness of 1.4 mils (1 ounce copper.) Using the equation for C_O developed in the previous chapter and Equation1 above the capacitance per unit length can be calculated for various trace widths. Figure 42 plots C_O versus trace width for several different dielectric thicknesses. In addition Figure 42 plots C_O versus the characteristic impedance for a microstrip line for the dielectric constant and trace thickness given above.

The propagation delay for a signal on a microstrip line is described by the following equation:

$$T_{PD} = 1.016\sqrt{(0.475 * \varepsilon_r + 0.67)}\ \text{ns/foot} \qquad \text{(eqt. 2)}$$

where:

ε_r = Dielectric Constant of the Board Material

Note that the propagation delay is dependent only on the dielectric constant of the PCB substrate. Figure 43 plots the propagation delay of a microstrip line versus the dielectric constant of the PCB.

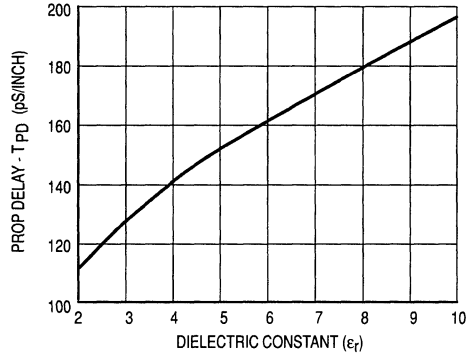


Figure 43. Propagation Delay versus Dielectric Constant

STRIPLINE

Stripline is a printed circuit board interconnect in which a signal conductor is placed in a dielectric medium which is "sandwiched" between two conducting layers (Figure 44)

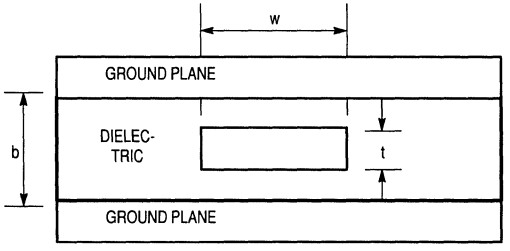


Figure 44. Stripline Structure

The characteristic impedance of the stripline is given by:

$$Z_O = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4b}{0.67\pi(0.8w + t)}\right] \quad \text{(eqt. 3)}$$

where:

ε_r = Relative Dielectric Constant of the Substrate
w = Width of the Stripline
t = Thickness of the Stripline
h = Distance Between the Two Ground Planes

Equation 3 is accurate for the following dimension ratios:

$w/(b - t) < 0.35$ and $t/b < 0.25$

Once again, using a fairly typical ε_r of 4.8 and a copper trace thickness of 1.4 mils, the characteristic impedance of a stripline interconnect can be plotted for various trace widths and dielectric thicknesses (Figure 45)

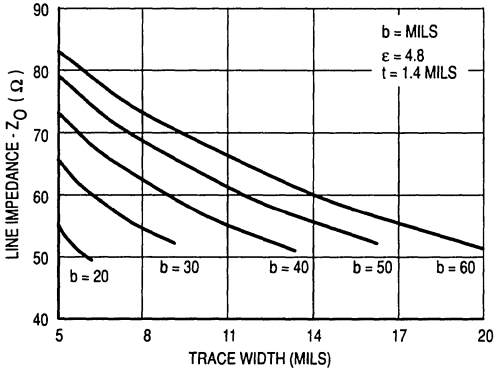


Figure 45. Stripline Impedance versus Trace Width

As was the case with a microstrip line the capacitance per unit length of a stripline trace can be calculated using $C_O = T_{pd}/Z_O$. The graphs of Figure 46 plot the capacitance of a stripline structure for a number of trace widths as well as the C_O versus the characteristic impedance of the line.

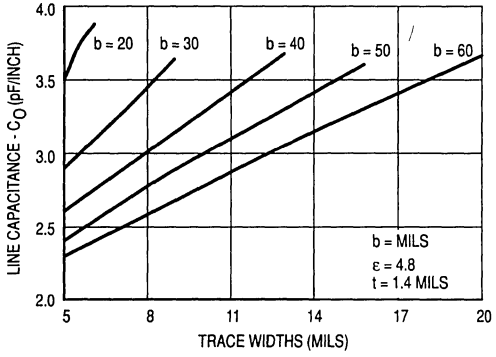
The propagation delay of a stripline trace is governed by the simple equation:

$$T_{PD} = 1.016\sqrt{\varepsilon_r} \text{ ns/ft} \quad \text{(eqt. 4)}$$

where:

ε_r = Dielectric Constant of the Board Material

Again the propagation delay of the trace is dependent only on the relative dielectric constant of the PCB substrate. Using Equation 4 the delay of the line can be plotted versus dielectric constant (Figure 47)



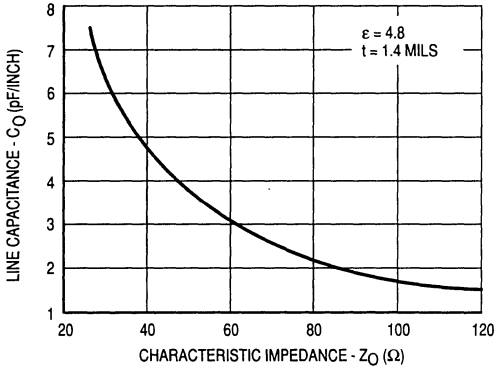


Figure 46. Stripline Capacitance versus Impedance and Trace Width

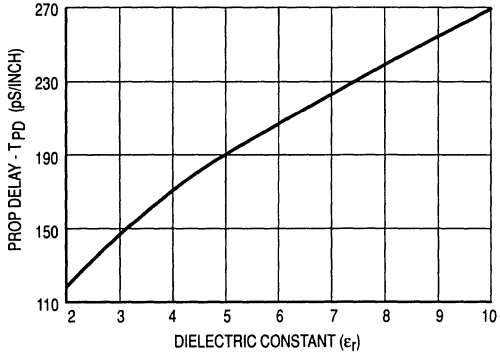


Figure 47. Stripline Propagation Delay versus Dielectric Constant

GENERAL INFORMATION

Since fiberglass-epoxy is by far the most widely used substrate in the industry two important considerations should be mentioned:

1. The propagation delay for microstrip is ≈145 ps per inch whereas that for stripline is ≈185 ps per inch. Since the propagation delay is governed by the dielectric of the substrate, a board material with a lower dielectric constant than glass-epoxy is required if a lower propagation delay is desired.
2. Cross coupled noise due to board geometries may require a substrate material with a lower dielectric constant. For example, the distance from the signal trace to the ground plane is a function of the substrate dielectric constant for a specified line characteristic impedance. Hence the switching energy coupled into adjacent traces on the same signal plane is also a function of the dielectric constant. If the dielectric thickness and trace width must be maintained for a given line impedance, the spacing between traces must be increased to maintain the noise margin. Since the dielectric constant of glass-epoxy is relatively large, the increase in spacing between the traces may be unacceptable. So, a substrate material with a lower dielectric constant may be desirable. Generally if the distance between traces is maintained at twice the distance to the ground plane, coupling between traces will be minimal.

Finally, printed circuit signal line shape variations play a significant role in modulating both the capacitance and inductance per unit length for a transmission line; in other words shape variations cause reflections. Bends in printed circuit traces cause an increase in the capacitance per unit length and a decrease in the inductance per unit length with a pronounced effect for angles of 90° or more. Two techniques available to compensate for shape changes are:

1. Maintain a uniform trace width.
2. Cut the corners of the trace such that the length of the diagonal cut is in the range of 1.6 to 2.0 times the trace width.

Figure 48 illustrates these two techniques.

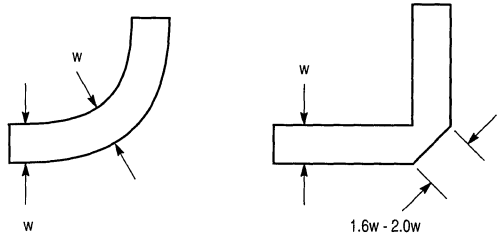


Figure 48. Compensation for Capacitive Effects of Trace Angles

COAXIAL CABLE

Coaxial cable is a two conductor transmission line consisting of a concentric inner conductor surrounded by a dielectric which in turn is surrounded by a tubular outer conductor (Figure 49). It is ideal for transmitting high frequency signals over long distances because of its well defined and uniform characteristic impedance. Moreover, crosstalk is minimized by the ground shield provided by the outer conductor.

The propagation delay is derived in the same way as a stripline interconnect and thus is described by Equation 4. Therefore as with stripline structures the delay is a function of only dielectric constant. The characteristic impedance and capacitance per unit length are parameters specified by the coaxial cable manufacturer, hence the designer should look to the cable manufacturer for these parameters.

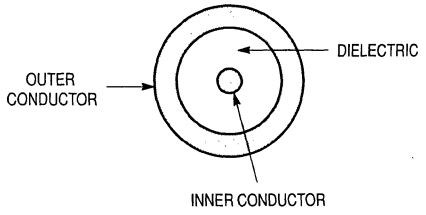


Figure 49. Cross Section of Coaxial Cable

COAXIAL CABLE LENGTHS

The ECLinPS family operates with rise times as fast as several hundred picoseconds, thus coaxial cable must be able to transmit these pulses without introducing a significant distortion. Viewing the ECLinPS output as a single time constant driver circuit terminated with a 50 Ω load, the required line bandwidth (f_C) can be calculated as follows.

$$f_C = 0.35/t_R \qquad \text{(eqt. 5)}$$

where:
t_R = 10% to 90% Rise Time

Converting the typical 20%-80% rise time value of 400 ps to an equivalent 10%-90% rise time value of 530 ps, and using Equation 5 yields a bandwidth value of f_C = 660MHz

Below 1 GHz the primary loss mechanism in transmission lines is skin effect, as dielectric losses for materials such as polyethylene and teflon are insignificant below this value. Since attenuation due to skin effect is proportional to the square root of frequency a log-log plot of attenuation versus frequency produces a linear result. The maximum coaxial cable lengths for the ECLinPS family can be derived from the plot in Figure 50.

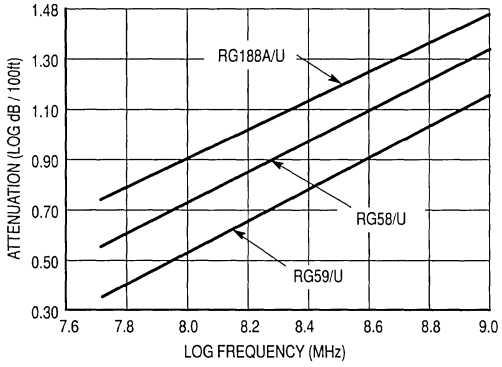


Figure 50. Coaxial Cable Attenuation versus Frequency

Typically for an ECL system the minimum peak to peak signal swing is 600 mV. The nominal peak to peak signal swing for the ECLinPS family is approximately 850 mV. Thus, the maximum permissible attenuation is:

$$\text{Loss (dB)} = 20 * \log (V_{IN}/V_O)$$
$$= 20 * \log (0.85/0.6) = 3.0 \text{ dB}$$

From Figure 50 the loss at 660MHz for RG58/U cable is 15 dB/100 feet. Therefore, the maximum length is

Max Length = 100 ft. * (3.0 dB/15 dB) = 20 ft.

Additional information concerning coaxial cable can be found in Motorola's MECL System Design Handbook (HB205/D).

SUMMARY OF VALUES

Table 7 is a compilation of propagation delays at nominal dielectric values for the three types of interconnects discussed.

Interconnect	T_{PD}	ε_r
Microstrip	145 ps/in	4.8
Stripline	185 ps/in	4.8
Coaxial Cable	123 ps/in	2.1

Table 7. Comparison of Interconnect Medium

TERMINATION TECHNIQUES

From transmission line theory, a signal propagating down the line is partially reflected back to the source if the line is not terminated in its characteristic impedance. The magnitude of the reflected voltage signal is governed by the load reflection coefficient, ρ_L.

$$\rho_L = (R_T - Z_O) / (R_T + Z_O) \qquad \text{(eqt. 6)}$$

where:
R_T = Load Impedance, and
Z_O = Characteristic Impedance of the Line

When the reflected signal arrives at the source it is re-reflected back toward the load with a magnitude dictated by the source reflection coefficient, ρ_S.

$$\rho_S = (R_S - Z_O) / (R_S + Z_O) \qquad \text{(eqt. 7)}$$

where:
R_S = Source Impedance
Z_O = Characteristic Impedance of the Line

The reflected signal continues to be re-reflected by the source and load impedances and is attenuated with each passage over the transmission line. The output response appears as a damped oscillation asymptotically approaching the steady state value. This phenomena is often referred to as ringing.

The importance of minimizing the reflected signals lies in their adverse affect on noise margin and the potential for driving the input transistors of the succeeding stage into saturation. Both of these phenomena can lead to less than ideal system performance. To minimize the potential hazards associated with reflections on transmission lines three basic termination techniques are available:

1. Minimizing Unterminated line lengths
2. Parallel Termination
3. Series Termination

UNTERMINATED LINES

Figure 51 illustrates an unterminated transmission line. This configuration is also referred to as a stub or an open line.

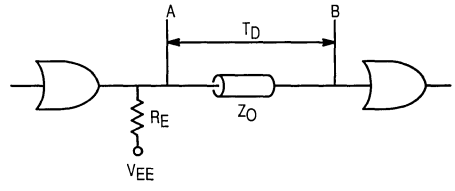


Figure 51. Unterminated Transmission Line

The function of R_E is to provide the drive current for a high to low transition at the driver output. Since the reflection coefficient at the load is of opposite polarity to that at the source, the signal will be reflected back and forth over the transmission line with the polarity changing after each reflection from the source impedance. Thus, steps appear at the input to the receiving gate. When R_E is too large steps appear in the trailing edge of the propagating signal that slows the edge speed of the input to the receiving gate, subsequently causing an increase in the net propagation delay. A reasonable negative-going signal swing at the input of the receiving gate results when the value of R_E is selected to produce an initial step of 600 mV at the driving gate. Hence:

$$I * Z_O > 0.6 \qquad \text{(eqt. 8)}$$

$$(V_{OH} - V_{EE})/(R_E + Z_O) * Z_O \geq 0.6$$

$$6.2Z_O \geq R_E \text{ (10E)}, \; 4.9Z_O \geq R_E \text{ (100E)} \qquad \text{(eqt. 9)}$$

Load resistors of less than 180 Ω should not be used because the heavy load may cause a reduction in noise immunity when the output is in the high state due to an increased output emitter-follower V_{BE} drop.

When the driver gate delivers a full ECL swing, the signal propagates from point A arriving at point B a time T_D later. At point B the signal is reflected as a function of ρ_L. The input impedance of the receiving gate is large relative to the line characteristic impedance, therefore:

$$\rho_L = (R_T - Z_O) / (R_T + Z_O) \approx 1 \qquad \text{(eqt. 10)}$$

A large positive reflection occurs resulting in overshoot. The reflected signal reaches point A at time $2T_D$, and a large negative reflection results because the output impedance of the driver gate is much less than the line characteristic impedance (i.e. $R_O << Z_O$). In this case the reflection coefficient is negative.

$$\rho_S = (R_O - Z_O) / (R_O + Z_O) \qquad \text{(eqt. 11)}$$

The signal is re-reflected back toward the load arriving at time $3T_D$ resulting in undershoot at point B. This re-reflection of signals continues between the source and load impedances causing ringing to appear on the output response.

The impetus in restricting interconnect lengths is to mitigate the effects of overshoot and undershoot. A handy rule of thumb is that the undershoot can be limited to less than 15% of the logic swing if the two way line delay is less than the rise time of the pulse. With an undershoot of <15% the physics of the situation will result in an overshoot which will not cause saturation problems at the receiving input. Thus, the maximum line length can be determined using Equation 12.

$$L_{max} < t_R/2*T_{PD} \text{ (unit length)} \qquad \text{(eqt. 12)}$$

where:
L = Line Length
t_R = Rise time
T_{PD} = Propagation Delay per unit Length

Further, the propagation delay increases with gate loading, thus the actual delay per unit length (T_{PD}') is given as:

$$T_{PD}' = T_{PD} * \sqrt{(1 + C_D / (L * C_O))}$$

Substitution of the modified delay per unit length into Equation 12 and rearranging yields Equation 13:

$$t_R \geq (2 * L) * T_{PD} * \sqrt{(1 + C_D / (L * C_O))} \qquad \text{(eqt. 13)}$$

Solving Equation 13 for the maximum line length produces:

$$L_{max} = 0.5 * (\sqrt{((C_D / C_O) ** 2 + (t_R/T_{PD}) ** 2)} - C_D/C_O \qquad \text{(eqt. 14)}$$

Assuming a worst case capacitance of 2 pF and a rise time of 200 ps for the ECLinPS family gives a value of 0.3 inches for the maximum open line length.

Table 8 shows maximum open line lengths derived from SPICE simulations for single and double gate loads, a maximum overshoot of 40% and undershoot of 20% was assumed. The simulation results indicate that for a 50 Ω line a stub length of ≤ 0.3 inches will limit the overshoot to less than 40%, and the undershoot to within 20% of the logic swing. Signal traces will most assuredly be larger than 0.3" for all but the simplest of interconnects, thus for most practical applications it will be necessary to use ECLinPS devices in a controlled impedance environment.

Z_O (Ω)	Microstrip		Stripline	
	Fanout = 1	Fanout = 2	Fanout = 1	Fanout = 2
	L_{max} (in)	L_{max} (in)	L_{max} (in)	L_{max} (in)
50	0.3	0.2	0.3	0.15
68	0.3	0.15	0.25	0.1
75	0.3	0.15	0.25	0.1
82	0.3	0.1	0.25	0.1
90	0.3	0.1	0.25	0.1
100	0.25	0.1	0.25	0.1

Table 8. SPICE Derived Maximum Open Line Lengths for ECLinPS Designs

PARALLEL TERMINATION

When the fastest circuit performance or the ability to drive distributed loads is desired, parallel termination is the method of choice. An important feature of the parallel termination scheme is the undistorted waveform along the full length of the line. A parallel terminated line is one in which the receiving end is terminated to a voltage (V_{TT}) through a resistor (R_T) with a value equal to the line characteristic impedance (Figure 52a). An advantage of this technique is that power consumption can be decreased by a judicious choice of V_{TT}. For 50 Ω systems the typical value of V_{TT} is negative two volts.

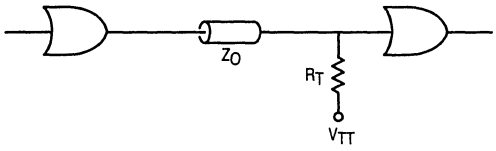


Figure 52a. Parallel Termination to VTT

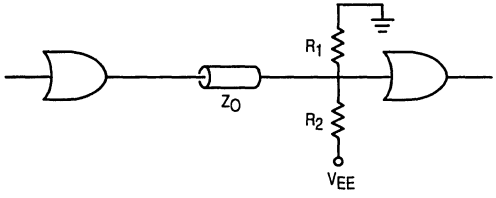


Figure 52b. Thevenin Equivalent Parallel Termination

Figure 52. Parallel Termination Schemes

Although the single resistor termination to V_{TT} conserves power, it offers the disadvantage of requiring an additional supply voltage. An alternate approach to using a single power supply is to use a resistor divider network as shown in Figure 52b. The Thevenin equivalent of the two resistors is a single resistor equal to the characteristic impedance of the line, and terminated to V_{TT}. The values for resistors R_1 and R_2 may be obtained from the following relationships:

$$R_2 = (V_{EE} / V_{TT}) * Z_O \quad \text{(eqt. 15)}$$
$$R_1 = (R_2 * V_{TT})/(V_{EE} - V_{TT}) \quad \text{(eqt. 16)}$$

For a nominal 10E supply voltage of –5.2V and V_{TT} of –2V:

$$R_2 = 2.6 * Z_O \quad \text{(eqt. 17)}$$
$$R_1 = R_2 / 1.6 \quad \text{(eqt. 18)}$$

For a nominal 100 E supply voltage of –4.5V and V_{TT} of –2V

$$R_2 = 2.25 * Z_O \quad \text{(eqt. 19)}$$
$$R_1 = R_2 / 1.25 \quad \text{(eqt. 20)}$$

Table 9 provides a reference of values for the resistor divider network of Figure 52b.

	10 E		100 E	
Z_O (Ω)	R_1 (Ω)	R_2 (Ω)	R_1 (Ω)	R_2 (Ω)
50	81	130	90	113
70	113	182	126	158
75	121	195	135	169
80	130	208	144	180
90	146	234	161	202
100	162	260	180	225
120	194	312	216	270
150	243	390	270	338

Table 9. Thevenin Termination Resistor Values

For both configurations, when the equivalent termination resistance matches the line impedance no reflection occurs because all the energy in the signal is absorbed by the termination. Hence, the primary tradeoff between the two types of termination schemes are power versus power supply requirements. As mentioned earlier, the V_{TT} scenario requires an extra power supply, however the Theveninization technique will consume 10 fold more DC power. Fortunately this extra power consumption will not be seen on the die, therefore both techniques will result in the same die junction temperatures.

ECLinPS output drivers consists of emitter followers designed to drive a 50 Ω load into a negative two volt supply (V_{TT}). Under these conditions the nominal 10 E output levels are –1.75 volts at 5 mA for the low state and –0.9 volts at 22 mA for the high state. For the 100 E devices the nominal output levels are –0.955 volts at 20.9 mA for the high state and –1.705 volts at 5.9 mA for the low state.

Figure 53 shows the nominal output characteristics for ECLinPS devices driving various load impedances returned to a negative two volt supply. This plot applies to both 10 E and 100 E versions of the ECLinPS family. The output resistances R_H (high state output resistance) and R_L (low state output resistance) are obtained from the reciprocal of the slope at the desired operating point. Many applications require loads other than 50 Ω, the resulting V_{OH} and V_{OL} levels can be estimated using the following technique.

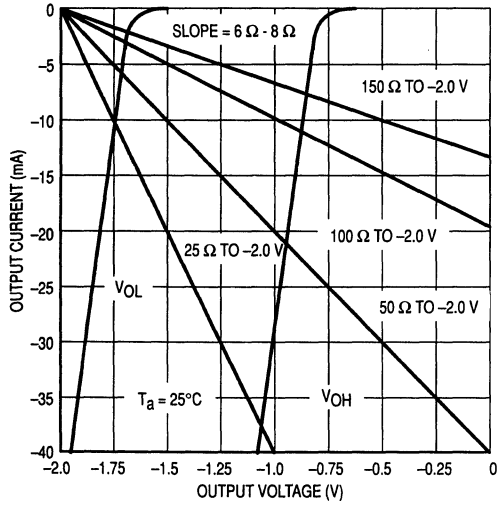


Figure 53. ECLinPS Output Characteristics

10 E DEVICES

The equivalent output circuit is shown in Figure 54. The output levels are estimated from Figure 54 as follows:

$$V_{OH} = -770\text{ mV} - 6*I_{HOUT} \quad \text{(eqt. 21)}$$

where:

$$I_{HOUT} = (-770\text{ mV} - V_{TT}) / (6\ \Omega + R_T)$$

and

$$V_{OL} = -1710\text{ mV} - 8*I_{LOUT} \quad \text{(eqt. 22)}$$

where:

$$I_{LOUT} = (-1710\text{ mV} - V_{TT}) / (8\ \Omega + R_T)$$

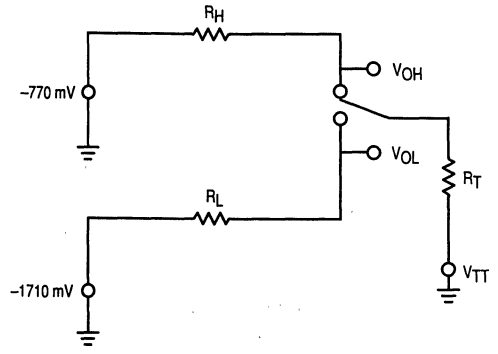


Figure 54. Equivalent Model for Calculating 10 E Output Levels

100 E DEVICES

The equivalent output circuit is shown in Figure 55. The output levels are estimated from Figure 55 as follows:

$$V_{OH} = -830\text{ mV} - 6*I_{HOUT} \quad \text{(eqt. 23)}$$

where:

$$I_{HOUT} = (-830\text{ mV} - V_{TT}) / (6\ \Omega + R_T)$$

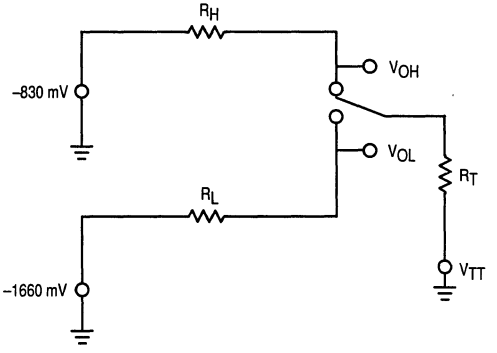


Figure 55. Equivalent Circuit for Calculating 100 E Output Levels

and

$$V_{OL} = -1660\text{ mV} - 8*I_{LOUT} \quad \text{(eqt. 24)}$$

where:

$$I_{LOUT} = (-1660\text{ mV} - V_{TT}) / (8\ \Omega + R_T)$$

SIP RESISTORS

The choice of resistor type for use as the termination resistor has several alternatives. Although the use of a discrete, preferably chip resistor, offers the best isolation and lowest parasitic additions there are SIP resistor packs which will work fine for ECLinPS designs. SIP resistors offer a level of density which is impossible to obtain using their discrete counterparts. However, there are some guidelines which the user should follow when using SIP resistor packs. Always terminate complimentary outputs in the same pack to minimize inductance effects on the SIP power pin. Noise generated on this pin will couple directly into all of the resistors in the pack. In addition, the SIP package should incorporate bypass capacitors in the design (Figure 56). These capacitors are necessary to help maintain a solid V_{TT} level within the package, again mitigating any potential crosstalk or feedthrough effects. A 10 pin SIP like the DALE CSRC-10B21-500J/103M, is suitable for providing 50 Ω terminations while maintaining a relatively noise free environment to non-switching inputs.

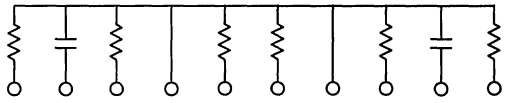


Figure 56. Standard ECL 10 pin SIP

SERIES TERMINATION TECHNIQUE

Series Damping is a technique in which a termination resistance is placed between the driver and the transmission line with no termination resistance placed at the receiving end of the line (Figure 57).

Series Termination is a special case of series damping in which the sum of the termination resistor (R_{ST}) and the output impedance of the driving gate (R_O) is equal to the line characteristic impedance.

$$R_{ST} + R_O = Z_O$$

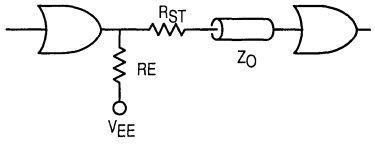


Figure 57. Series Termination

Series termination techniques are useful when the interconnect lengths are long or impedance discontinuities exist on the line. Additionally, the signal travels down the line at half amplitude minimizing problems associated with crosstalk. Unfortunately, a drawback with this technique is the possibility of a two step signal appearing when the driven inputs are far from the end of the transmission line. To avoid this problem the distance between the end of the transmission line and input gates should adhere to the guidelines specified in Table 8 from the section on unterminated lines.

SERIES TERMINATION THEORY

When the output of the series terminated driver gate switches, a change in voltage (ΔV_B) occurs at the input to the transmission line:

$$\Delta V_B = V_{IN} * (Z_O) / (R_{ST} + R_S + Z_O) \qquad \text{(eqt. 25)}$$

where:
V_{IN} = Internal Voltage Change
Z_O = Line Characteristic Impedance
R_S = Output Impedance of the Driver Gate
R_{ST} = Termination Resistance

Since $Z_O = R_{ST} + R_S$ substitution into Equation 25 yields:

$$\Delta V_B = V_{IN} / 2 \qquad \text{(eqt. 26)}$$

From Equation 26 an incident wave of half amplitude propagates down the transmission line. Since the transmission line is unterminated at the receiving end, the reflection coefficient at the load is approximately unity; therefore the reflection causes the voltage to double at the receiving end. When the reflected wave arrives at the source end its energy is absorbed by the series resistance producing no further reflections as the impedance is equal to the characteristic impedance of the line.

An extension of the series termination technique using parallel fanout eliminates the problem of lumped loading at the expense of extra transmission lines (Figure 58).

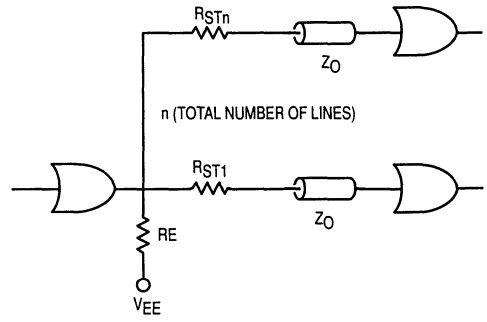


Figure 58. Parallel Fanout using Series Termination

CALCULATION OF R_E

R_E functions to establish V_{OH} and V_{OL} levels and to provide the negative going drive into R_{ST} and Z_O when the driver output switches to the low state. The value of R_E must be such that the required current is supplied to each transmission line while not allowing the output transistor to turn off when switching from a high to a low state. An appropriate model is to treat the output emitter follower as a simple switch (Figure 59).

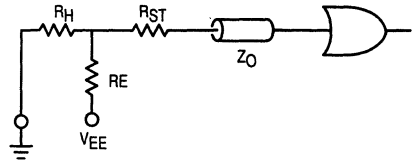


Figure 59. Equivalent Circuit for R_E Determination

The worst case scenario occurs when the driver output emitter follower is cutoff during a negative going transition. When this happens the switch can be considered opened, and at the instant it opens the line characteristic impedance behaves as a linear resistor returned to V_{OH}. The model becomes a simple series resistive network as shown in Figure 60.

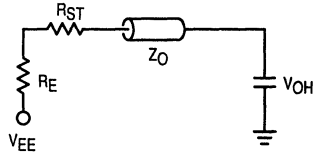


Figure 60. Equivalent Circuit with Output Cutoff

The maximum current occurs at the instant the switch opens and is given by Equation 27.

$$I_{MAX} = (V_{OH} - V_{EE}) / (R_E + R_{ST} + Z_O) \qquad \text{(eqt. 27)}$$

The initial current must be sufficient to generate a transient voltage equal to half of the logic swing since the voltage at the receiving end of the line doubles for the series terminated case. To insure the pull down current is large enough to handle reflections caused by discontinuities and load capacitances the transient voltage is increased by 25%. Therefore,

$$I_{INIT} = (1.25 * V_{SWING}/2) / Z_O \qquad \text{(eqt. 28)}$$

To satisfy the initial constraints $I_{MAX} > I_{INIT}$

$$(V_{OH} - V_{EE}) / (R_E + R_{ST} + Z_O) > (1.25 * V_{SWING}/2) / Z_O$$

For the 10 E series:

$V_{OH} = -0.9$ V, $V_{SWING} = 0.85$ V, $V_{EE} = -5.2$ V

$$[-0.9 - (-5.2)] / (R_{ST} + R_E + Z_O) \geq 0.531 / Z_O$$

$$7.10 * Z_O - R_{ST} \geq R_E \qquad \text{(eqt. 29)}$$

For the 100 E series:

$V_{OH} = -0.955$ V, $V_{SWING} = 0.75$, $V_{EE} = -4.5$ V

$$6.56 * Z_O - R_{ST} > R_E \qquad \text{(eqt. 30)}$$

Figure 58 showed a modification of the series termination scheme in which several series terminated lines are driven by a single ECL gate. The principle concern when applying this technique is to maintain the current in the output emitter follower below the maximum rated value. The value for R_E can be calculated by viewing the circuit in terms of conductances.

$$G_E > G_1 + G_2 + \ldots + G_n \qquad \text{(eqt. 31)}$$

For the 10 E series:

$$1 / R_E \geq 1 / (7.10 * Z_{O1} - R_{ST1}) + 1 / (7.10 * Z_{O2} - R_{ST2}) + 1 / (7.10 * Z_{O3} - R_{STn})$$

For the case where $Z_{O1}=Z_{O2}=\ldots=Z_{On}$ and $R_{ST1}=R_{ST2}=\ldots R_{STn}$

$$R_E \leq (7.10 * Z_O + R_{ST}) / n \qquad \text{(eqt. 32)}$$

where n is the number of parallel circuits.

For the 100 E series:

$$1 / R_E \geq 1 / (6.56 * Z_{O1} - R_{ST1}) + 1 / (6.56 * Z_{O2} - R_{ST2}) + 1 / (6.56 * Z_{O3} - R_{STn})$$

For the case where $Z_{O1}=Z_{O2}=\ldots=Z_{On}$ and $R_{ST1}=R_{ST2}=\ldots R_{STn}$

$$R_E \leq (6.56 * Z_O + R_{ST}) / n \qquad \text{(eqt. 33)}$$

where n is the number of parallel circuits.

When a series terminated line is driving more than a single ECL load the issue of maximum number of loads must be addressed. The factor limiting the number of loads is the voltage drop across the termination resistor caused by the input currents to the ECL loads when the loads are in the quiescent high state. A good rule of thumb is to determine if the loss in high state noise margin is acceptable. The loss in noise margin is given by

$$NM_{LOSS} = I_T * (R_{ST} + R_O) \qquad \text{(eqt. 34)}$$

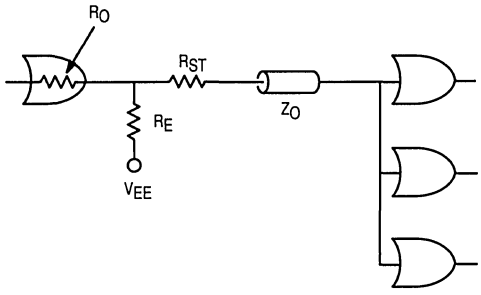


Figure 61. Noise Margin Loss Example

where:
I_T = Sum of I_{INH} Currents

For the majority of devices in the ECLinPS family the typical maximum value for quiescent high state input current is 150 μA. Thus for the circuit shown in Figure 61 in which three gate loads are present in a 50 Ω environment the loss in high state noise margin is calculated as:

$$NM_{LOSS} = 3 * 150\,\mu A * 50\,\Omega = 22.5\,mV$$

ECLinPS I/O SPICE MODELING KIT

Due to the heavier reliance on simulation tools for initial prototyping, Motorola has put together a SPICE modeling kit aimed at aiding the customer in modeling board interconnect behavior. The kit includes representative drivers and receivers as well as the necessary SPICE model parameters. In addition tips are provided for simulating a wide range of output conditions. The kit, in conjunction with todays CAD tools, can greatly simplify the design and characterization of critical nets in a design. Anyone interested in obtaining a copy is encouraged to contact an ECLinPS Application Engineer.

Interfacing With ECLinPS

INTERFACING TO EXISTING ECL FAMILIES

There currently exists two basic standards for high performance ECL logic devices: 10H and 10K. To maximize system flexibility each member of the ECLinPS family is available in both of the existing ECL standards: 10 E series devices are compatible with the MECL 10H family; 100 E series devices are compatible with ECL 10K.

The difference in the DC behavior of the outputs of the two different standards necessitates caution when mixing the two technologies into a single ended input design. As illustrated in Figures 62 and 63 and Table 10, there is no problem when a 10H device is used to drive a 10K device, however problems arise when the scenario is reversed.

For the case of a 10K device driving a 10H device the worst case noise margin is reduced to 35 mV, a noise margin which is unacceptable for most designs. Since the problems of interfacing are an output tracking rate versus a V_{BB} tracking rate problem if the system uses only differential interconnect between the two technologies there will be no loss of noise margin and the design will operate as desired.

Fortunately the ECLinPS family, by offering devices in both standards, allows the user to integrate higher performance technology into his design without having to battle these interface problems.

Another area of concern when interfacing to older slower logic families is the behavior of ECLinPS devices with slower input edge rates. Typically, other than clock inputs, the ECLinPS family will function properly for edge speeds of up to 20 ns. For edges significantly slower than 20 nS the Schmitt trigger circuit of Figure 64 can be used to sharpen the edge rates reliably.

Obviously a very slow edge rate will amplify differences in delay paths due to any offset of the V_{BB} switching reference. This extra delay should be included in speed calculations of a design. For calculation purposes a worst case ±200 ps/ns gate-gain delay (delay versus input edge rate) can be assumed or a more typical value of ±75 ps/ns can be used.

Drvr > Rcvr	NM - High	NM - Low
10H > 10H	150 mV	150 mV
10H > 10K	145 mV	125 mV
10K > 10K	130 mV	135 mV
10K > 10H	35 mV	130 mV

Table 10. Worst-Case Noise Margins of a Mixed 10H and 10K Design

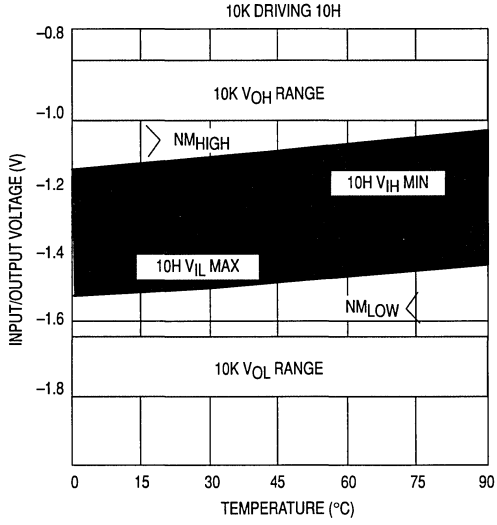


Figure 62. Interfacing 10H ECL and 10K ECL

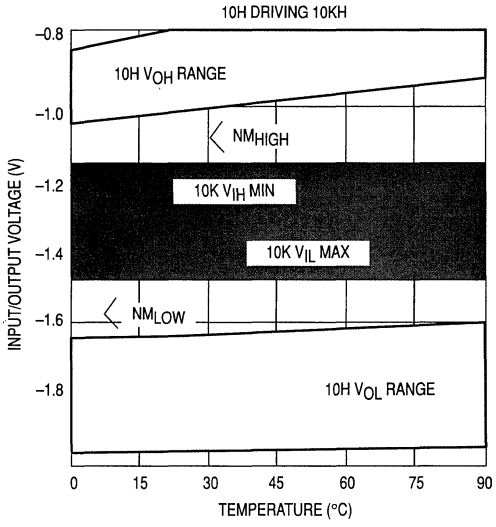


Figure 63. Interfacing 10H ECL and 10K ECL (continued)

Clock inputs on flip flop devices in the ECLinPS family are especially sensitive to slow edge rates. Flip flops have been successfully clocked in a noise free bench setup environment with edge rates of up to 20 ns. However in ATE systems where more noise is present, clocking problems arise with input edge rates of greater than 6 or 7 ns. To ensure reliable operation in a system with input clock edges slower than 7 ns it is recommended that the signals be buffered with an ECLinPS buffer circuit (E522, E516, E501 etc) or, for extreme conditions, the Schmitt trigger of Figure 64 to provide the gain necessary to sharpen the edges on the clock pulse.

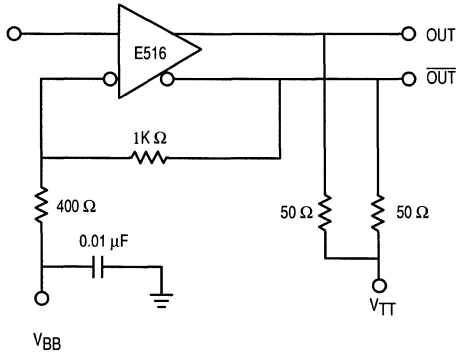


Figure 64. Schmitt Trigger w/ 100 mV of Hysteresis

INTERFACING TO TTL/CMOS LOGIC

To interface ECLinPS devices to TTL or CMOS subsystems there exists several new product offerings, as well as several existing devices, in the MECL 10H family which are ideally suited to the task. These translation devices are specially suited for clock distribution, DRAM driving as well as general purpose translation in both single supply and dual supply environments.

In mixed technology environments it is recommended that the noisy supplies of TTL and CMOS circuits be isolated from the ECL supplies. This can be done either through separate power planes in the board or a common plane with isolated ECL and TTL power sub-planes. The planes of common voltages (ie. ECL V_{CC} and TTL ground for split supply systems or common V_{CC} and ground for a single supply system) should then be connected to a common system ground or power supply through an appropriate edge connector.

INTERFACING TO GaAs LOGIC

In general, GaAs logic is designed to interface directly with ECL, however in some instances the worst case V_{OH} of a GaAs output can go as high as –0.3V. An ECLinPS device, depending on the input structure, may become saturated when driven with a –0.3V signal. It is recommended that if the designer is using a GaAs device which produces these –0.3V signals in an ECLinPS design he contact a Motorola Applications Engineer to determine if the ECLinPS device being driven will be susceptible to saturation.

AC COUPLING

In some cases it may be necessary to interface an ECLinPS design with a signal which lacks any DC offset. The differential devices in the ECLinPS family are ideally suited for this application. As pictured in Figure 65 the signal can be AC coupled and biased around the V_{BB} switching reference of the device. Note that this scheme only works for a data stream with no DC bias, for data streams such as RZ or unencoded NRZ DC restoration must be performed prior to AC coupling it to an ECLinPS device.

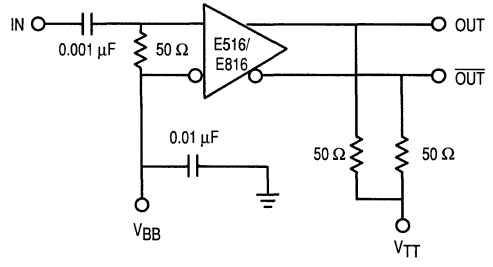


Figure 65. AC Couple Circuit

The 50 Ω resistor of Figure 65 provides the termination impedance while the V_{BB} pin provides the DC offset. The capacitor used to couple the signal must have an impedance of <<50 Ω for all frequency components of the input signal. Because large capacitors appear somewhat inductive at high frequencies it may be necessary to use a small capacitor in parallel with a larger one to achieve satisfactory operation. In addition it is important to bypass the V_{BB} line when used in this manner to minimize the noise coupled into the device.

Because the AC signal is biased around V_{BB}, the output of the ECLinPS device when AC coupled will have a duty cycle identical to the input. Thus this type of application is ideal for transforming high frequency sinusoidal waveforms from an oscillator into a square wave with a 50% duty cycle. The E816 device is a specialized line receiver with a much higher bandwidth than alternative ECLinPS devices, therefore for frequencies of >500MHz it is recommended that the designer use this device.

The above mentioned scenario will work fine as long as the input signal is present, however if the the inputs to the AC coupled device are left open problems may occur. With no input signal both inputs will go to V_{BB} and an undefined output, and perhaps an oscillating output, will result. If a defined output is necessary for an open input scenario, the circuit of Figure 66 can be used. The resistor tree between V_{CC} and V_{BB} creates an offset between the two inputs so that if the driving signal is lost a stable defined output will occur.

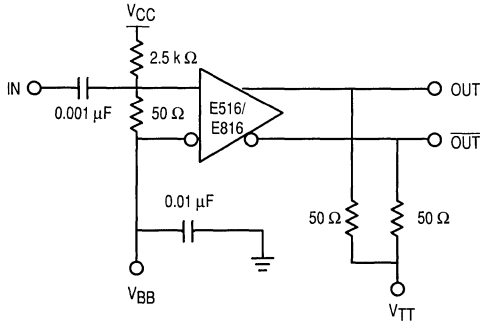


Figure 66. AC Couple Circuit with DC Offset

Unfortunately this configuration will adversely affect the duty cycle of the output. Depending on the frequency of the output, the duty cycle will change due to the longer distance to thresold on a rising edge as opposed to a falling edge. With this in mind, it becomes obvious that the smallest feasible offset would be the best solution. For stability a minimum of 25 mV is recommended, however this will not produce full ECL levels at the outputs of an E516 and thus another differential gate should be used to further amplify the signal. The gain of the E816 on the other hand is sufficient to produce acceptable levels at the outputs for DC input voltage differences of 25 mV. If a 150 mV offset is used full ECL levels will be seen at the outputs of the E516 however the price in duty cycle skew will be high. Of course if the signal is divided after it is received the duty cycle will be restored.

When using the circuit of Figure 66 care should be taken to limit the current sunk by the V_{BB} pin to a maximum of 0.5 mA. To achieve an offset of greater than 25 mV for the circuit of Figure 66 the DC current will necessarily need to be greater than 0.5 mA. To alleviate this dilemma one of the gates of the E516 can be configured as pictures in Figure 67 to generate a V_{BB} reference with the necessary current sinking capability. A single gate configured in this way will source or sink up to 10 mA without a significant shift in the generated V_{BB} level. If more current is needed several gates can be connected in parallel to provide the extra drive capability.

Note that the circuit pictured in Figure 66 will result in the Q outputs going high when the inputs are left open. If the opposite is desired the resistor to V_{CC} can be tied to the inverting input and V_{BB} to the non-inverting input.

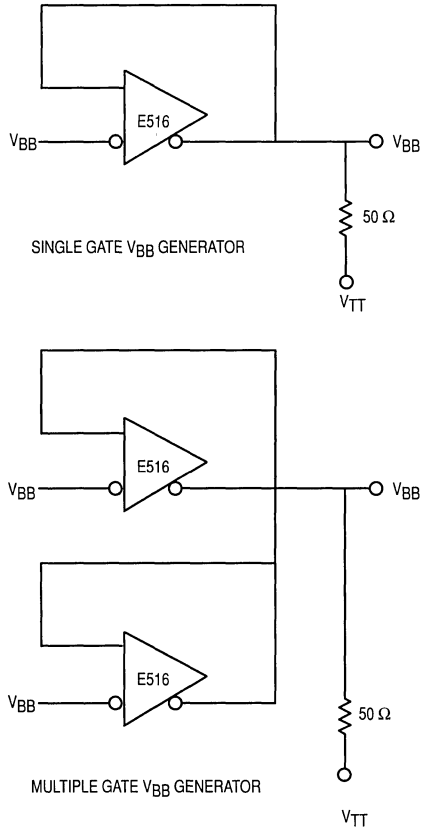
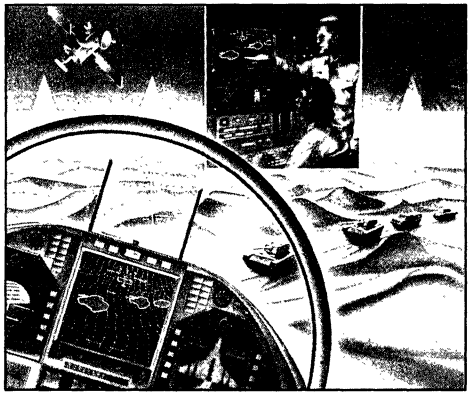


Figure 67. High Current V_{BB} Generator



MECL 10H

2

MOTOROLA

4-Bit Binary Counter

Military 10H416

ELECTRICALLY TESTED PER:
5962-8759001

The 10H416 is a high-speed synchronous, presettable, cascadable 4-bit binary counter. It is useful for a large number of conversion, counting and digital integration applications.

2

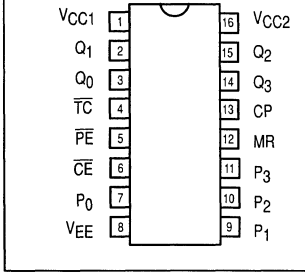
- Counting Frequency, 200 MHz Minimum
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8759001
3) 883: 10H416/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



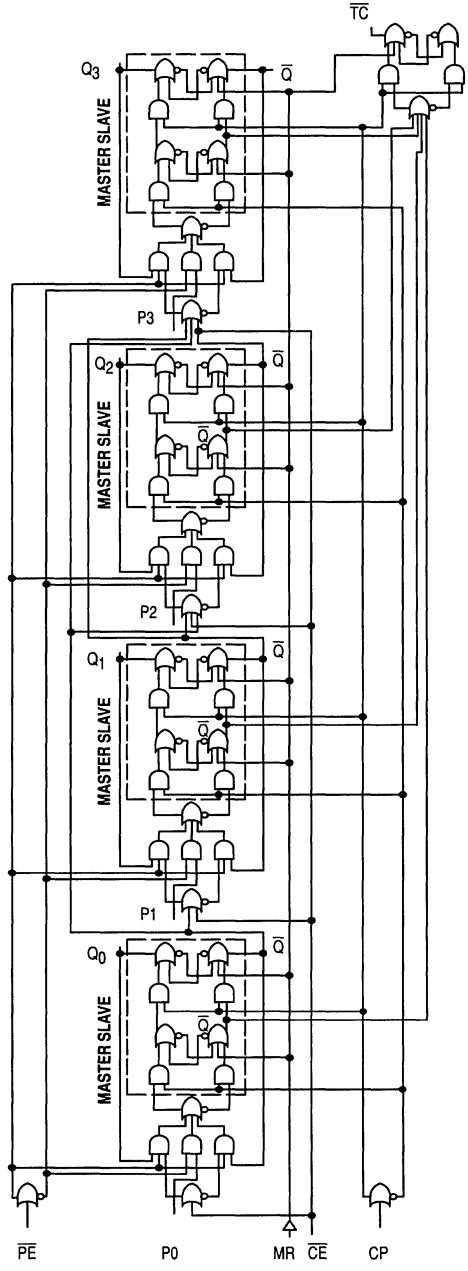
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω to V_{TT}
Q_0	3	7	4	51 Ω to V_{TT}
$\overline{TC}$	4	8	5	51 Ω to V_{TT}
$\overline{PE}$	5	9	7	OPEN
$\overline{CE}$	6	10	8	OPEN
P_0	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
P_1	9	13	12	GND
P_2	10	14	13	GND
P_3	11	15	14	GND
MR	12	16	15	OPEN
CP	13	1	17	CP1
Q_3	14	2	18	51 Ω to V_{TT}
Q_2	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

PIN NAMES

NAME	FUNCTION
$\overline{PE}$	Parallel Load Enable (Active Low)
P_n	Parallel Inputs
CP	Clock Inputs (Clocks on Positive Transition)
$\overline{CE}$	Count Enable (Low to Count)
MR	Master Reset (High forces all Q Outputs Low)
TC	Terminal Count (10010, Low at HLLH; 10016 Low at HHHH)
Q_n	Counter Outputs



NOTE: This diagram is provided for understanding of logic operation only. It should not be used for evaluation of propagation delays as many gate functions are achieved internally without incurring a full gate delay.

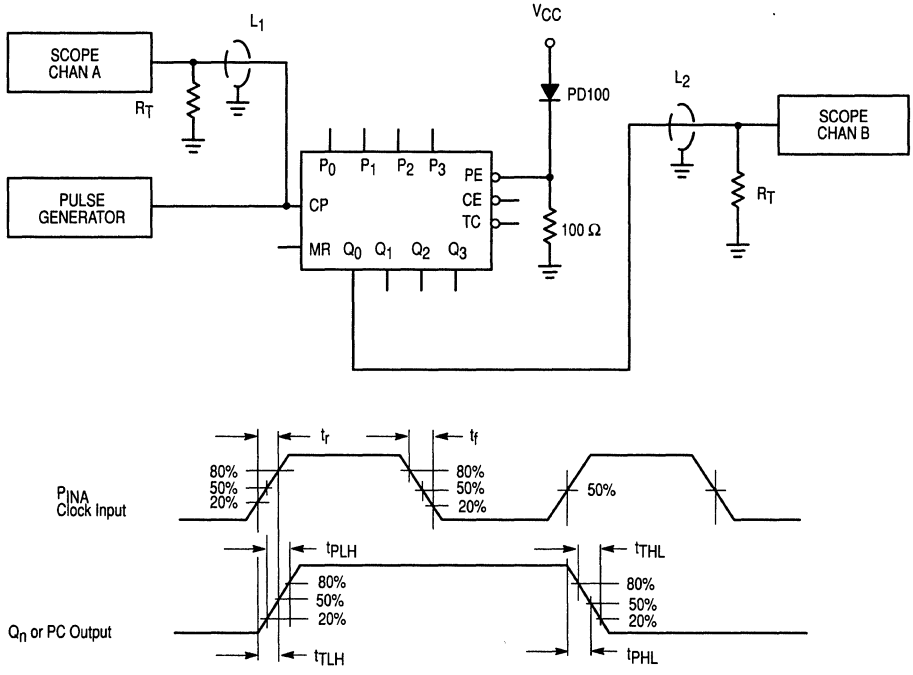
Figure 1. 4-Bit Binary Counter Logic Diagram

TRUTH TABLE

$\overline{CE}$	$\overline{PE}$	MR	CP	FUNCTION
L	L	L	Z	Load Parallel (P_n to Q_n)
H	L	L	Z	Load Parallel (P_n to Q_n)
L	H	L	Z	Count
H	H	L	Z	Hold
X	X	L	ZZ	Master Respond; Slave Hold
X	X	H	X	Reset (Q_n = Low, $\overline{TC}$ = High)

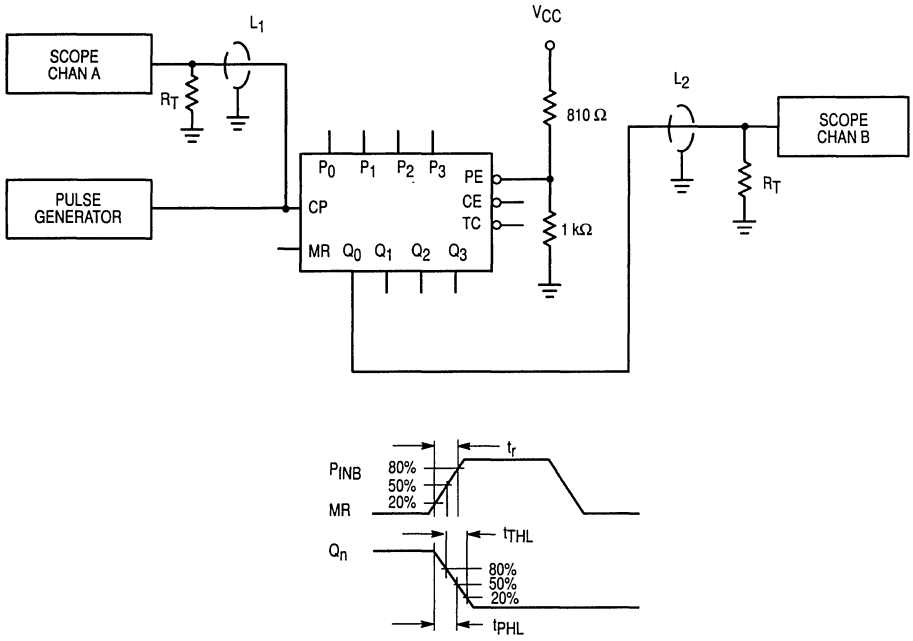
L = Low
H = High Voltage Level
X = Don't Care
Z = Clock Pulse (Low to High)
ZZ = Clock Pulse (High to Low)

Features include assertion inputs and outputs on each of the four master/slave counting flip-flops. Terminal count is generated internally in a manner that allows synchronous loading at nearly the speed of the basic counter.

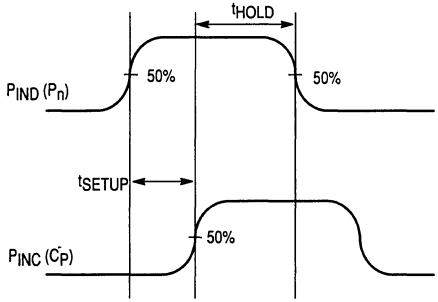


NOTES
1. L_1 and L_2 = equal length of 50 Ω impedance line, < 5.0 pF.
2. R_T = 50 Ω termination of scope.
3. Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}.
4. $V_{CC1} = V_{CC2} = 2.0$ V.
5. $V_{EE} = -3.2$ V.

Figure 2. Test Circuit and Waveforms (Clock to Output)



NOTES
1. L_1 and L_2 = equal length of 50 Ω impedance line.
2. R_T = 50 Ω termination of scope.
3. C_L = Jig and stray capacitance < 5.0 pF
3. Decoupling 0.1 µF from gnd to V_{EE} and V_{CC}.
4. $V_{CC1} = V_{CC2} = 2.0$ V.
5. $V_{EE} = -3.2$ V.



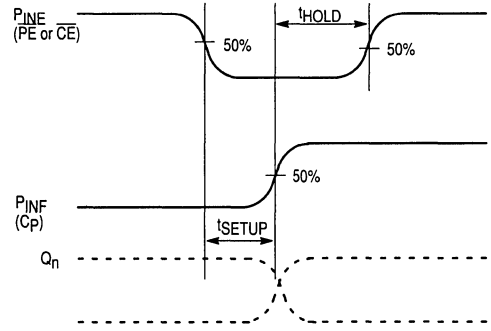


Figure 3. Test Circuit and Waveforms (Master Reset to Output)

10H416
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V	9 - 11, 7, 13	13	8		1, 16	2 - 4, 14, 15
V_{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	- 1.61	V	12, 13	13	8		1, 16	2 - 4, 14, 15
V_{OHA}	High Output Voltage	- 1.01	- 0.78	-0.65	- 0.65	- 1.06	- 0.84	V			8	8	1, 16	2 - 4, 14, 15
V_{OLA}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	-1.61	V			8	8	1, 16	2 - 4, 14, 15
I_{EE}	Power Supply Current	- 115		- 126		- 126		mA			8		1, 16	8
I_{IH}	Input Current High		265		450		450	µA	5 - 7, 9 - 11		8		1, 16	5 - 7, 9 - 11
I_{IH1}	Input Current High		700		1190		1190	µA	912		8		1, 16	12
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 9 - 13		8	1, 16	5 - 7, 9 - 13

10H416
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.780	-1.950	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.650	-1.950	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.840	-1.950	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	P_{S1}	P_{S2}	V_{CC}	V_{EEL}	Clk	P.U.T.
t_{TLH}	Rise Time	0.5	2.1	0.5	2.2	0.5	2.0	ns	5 - 13	4	9 - 11	7	1, 16	8		2, 3, 14, 15
t_{THL}	Fall Time	0.5	2.1	0.5	2.2	0.5	2.0	ns	5 - 13	4	9 - 11	7	1, 16	8		2, 3, 14, 15
t_{pd}	Propagation Delay															
	Clk to Q	1.0	2.6	1.0	2.9	1.0	2.5	ns	12, 13	14	7, 9 - 11	7	1, 16	8		2 - 4, 15
	Clk to TC	0.7	2.6	0.7	2.9	0.7	2.5	ns	12, 13	14	7, 9 - 11	7	1, 16	8		2 - 4, 15
	MR to Q	0.7	2.6	0.7	2.9	0.7	2.5	ns	12, 13	14	7, 9 - 11	7	1, 16	8		2 - 4, 15
t_{SET}	Setup Time															
	P_n to Clk	2.0		2.0		2.0		ns	5 - 7	3, 14	5, 7, 9 - 11		1, 16	8	13	3, 14
	CE or PE to Clk	2.5		2.5		2.5		ns	5 - 7	3, 14	5, 7, 9 - 11		1, 16	8	13	3, 14
t_{HOLD}	Hold Time															
	Clk to P_n	1.0		1.0		1.0		ns	5 - 7	3, 14	5, 7, 9 - 11		1, 16	8	13	3, 14
	Clk to PE or CE	0.5		0.5		0.5		ns	5 - 7	3, 14	5, 7, 9 - 11		1, 16	8	13	3, 14
f_{Count}	Count Frequency	200		200		200		MHz	13	3	9		1, 16	8		2, 4, 14, 15

Quad 2-Input NOR Gate with Strobe

Military 10H500

ELECTRICALLY TESTED PER:
MPG 10H500

The 10H500 is a quad 2 Input NOR gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

The MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply.

- Propagation Delay, 1.0 ns Typical
- 40 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10H500/BXAJC
X = CASE OUTLINE AS FOLLOWS:

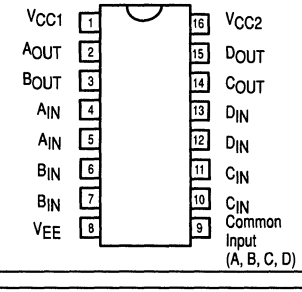
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

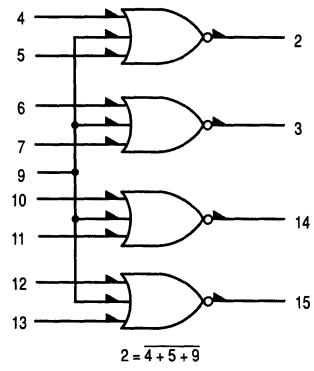
PIN ASSIGNMENTS

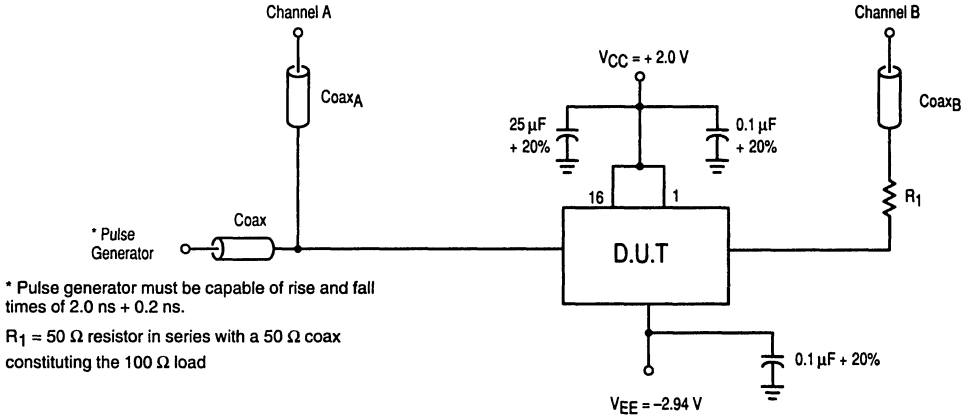
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	OPEN
A_{IN}	5	9	7	OPEN
B_{IN}	6	10	8	OPEN
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
Common Input	9	13	12	OPEN
C_{IN}	10	14	13	OPEN
C_{IN}	11	15	14	OPEN
D_{IN}	12	16	15	OPEN
D_{IN}	13	1	17	OPEN
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM



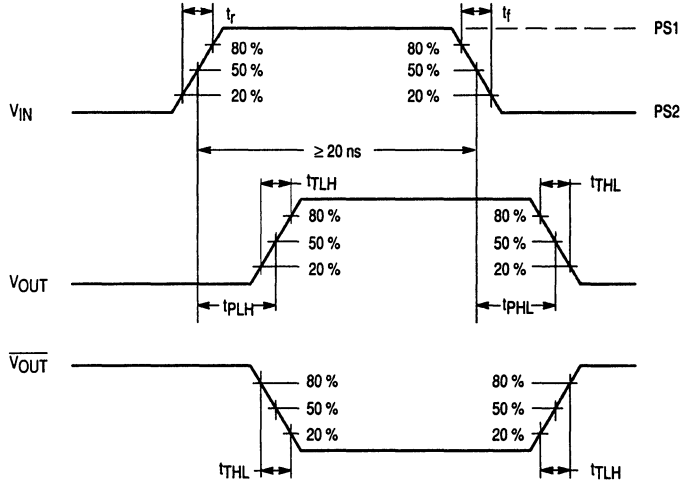


* Pulse generator must be capable of rise and fall times of 2.0 ns + 0.2 ns.

R_1 = 50 Ω resistor in series with a 50 Ω coax constituting the 100 Ω load

NOTES

1. Unused outputs should be loaded 100 Ω to GND.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 2.0 ns (20% - 80%) ± 0.2 ns.



NOTES

1. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.

Figure 1. Switching Test Circuit and Waveforms

10H500
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.11	-1.48	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IHA}	V_{ILA}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V		4, 5, 10, 11			8		1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	- 1.61	V	4-7, 9-13				8		1, 16	2, 3, 14, 15
V_{OHA}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V				4-7, 9-13	8	8	1, 16	2, 3, 14, 15
V_{OLA}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	-1.61	V			4-7, 9-13		8	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	- 26		- 29		- 29		mA					8		1, 16	8
I_{IH}	Input Current High		295		500		500	µA	4-7, 10-13				8		1, 16	4-7, 10-13
I_{IH1}	Input Current High		360		610		610	µA	9				8		1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4-7, 9-13			8		1, 16	4-7, 10-13

10H500
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.11	-1.48	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, All tests rferenced to Fig 1, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.5	1.8	0.66	2.34	0.6	2.1	ns	4, 6	2, 3	1, 16	8	2, 3, 14, 15
t_{THL}	Fall time	0.5	1.8	0.66	2.34	0.6	2.1	ns	4, 6	2, 3	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High	0.6	1.5	0.84	2.04	0.66	1.92	ns	10, 13	14, 15	1, 16	8	2, 3, 14
t_{PHL}	Propagation Delay High to Low	0.6	1.5	0.84	2.04	0.66	1.92	ns	10, 13	14, 15	1, 16	8	2, 3, 14

Quad OR/NOR Gate

Military 10H501

ELECTRICALLY TESTED PER:
5962-8750301

The 10H501 is a quad 2-input **OR/NOR** gate with one input from each gate common to pin 12.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

2

- Propagation Delay, 1.0 ns Typical
- 40 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8750301
3) 883: 10H501/BXAJC
X = CASE OUTLINE AS FOLLOWS:

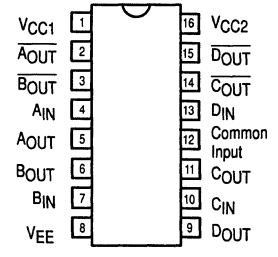
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

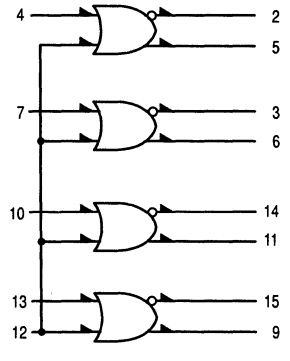
PIN ASSIGNMENTS

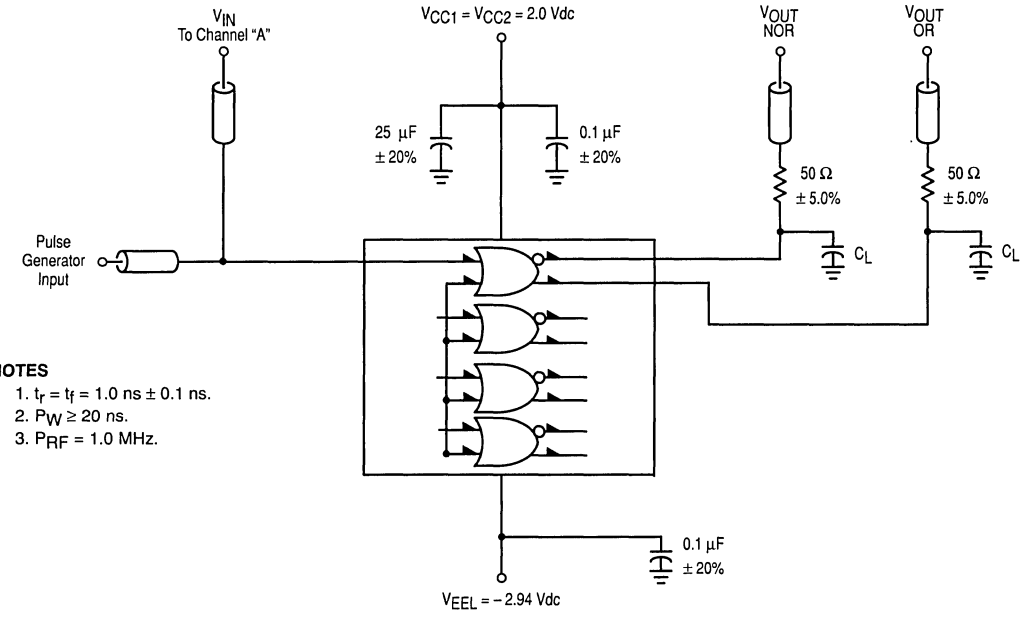
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{A_{OUT}}$	2	6	3	50 Ω to V_{TT}
$\overline{B_{OUT}}$	3	7	4	50 Ω to V_{TT}
A_{IN}	4	8	5	50 Ω to V_{TT}
A_{OUT}	5	9	7	50 Ω to V_{TT}
B_{OUT}	6	10	8	50 Ω to V_{TT}
B_{IN}	7	11	9	50 Ω to V_{TT}
V_{EE}	8	12	10	V_{EE}
D_{OUT}	9	13	12	510 Ω to V_{TT}
C_{IN}	10	14	13	510 Ω to V_{TT}
C_{OUT}	11	15	14	510 Ω to V_{TT}
Common Input	12	16	15	OPEN
D_{IN}	13	1	17	50 Ω to V_{TT}
$\overline{C_{OUT}}$	14	2	18	50 Ω to V_{TT}
$\overline{D_{OUT}}$	15	3	19	50 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM





NOTES

1. $t_r = t_f = 1.0$ ns ± 0.1 ns.
2. $P_W \geq 20$ ns.
3. $P_{RF} = 1.0$ MHz.

NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 inches (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test should be connected to a 100 Ω resistor to ground.
3. C_L = (test jig) ≤ 5.0 pF.

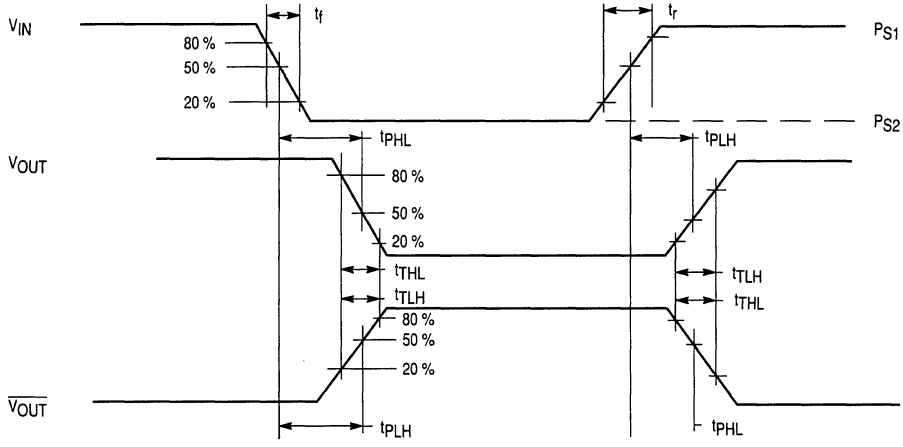


Figure 1. Switching Test Circuit and Waveforms

10H501
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V	4, 7, 10 12, 13	4, 7, 10 12, 13			8		1, 16	2, 3, 5, 6, 9, 11, 14, 15
V_{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	- 1.61	V	4, 7, 10 12, 13	4, 7, 10 12, 13			8		1, 16	2, 3, 5, 6, 9, 11, 14, 15
V_{OHA}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V			4, 7, 10 12, 13	4, 7, 10 12, 13	8	8	1, 16	2, 3, 5, 6, 9, 11, 14, 15
V_{OLA}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	-1.61	V			4, 7, 10 12, 13	4, 7, 10 12, 13	8	8	1, 16	2, 3, 5, 6, 9, 11, 14, 15
I_{EE}	Power Supply Current	- 26		- 29		- 29		mA					8		1, 16	8
I_{IH1}	Input Current High		265		425		425	µA	4, 7, 10, 13				8		1, 16	4, 7, 10, 13
I_{I2}	Input Current High		535		850		850	µA	12				8		1, 16	12
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4, 7, 10 12, 13				8	1, 16	4, 7, 10, 12, 13

10H501
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time (common)	0.4	1.65	0.4	1.7	0.4	1.65	ns	4	2, 5	1, 16	8	2
t_{THL}	Fall time (common)	0.4	1.65	0.4	1.7	0.4	1.65	ns	7	3	1, 16	8	2, 5
t_{PLH}	Propagation Delay Low to High (common)	0.5	1.6	0.5	1.8	0.5	1.6	ns	12	5	1, 16	8	2
t_{PHL}	Propagation Delay High to Low (common)	0.5	1.6	0.5	1.8	0.5	1.6	ns	12	15	1, 16	8	2, 5
t_{TLH}	Rise Time (others)	0.4	1.6	0.4	1.6	0.4	1.6	ns	4	2, 5	1, 16	8	2
t_{THL}	Fall time (others)	0.4	1.6	0.4	1.6	0.4	1.6	ns	7	3	1, 16	8	2, 5
t_{PLH}	Propagation Delay Low to High (others)	0.3	1.5	0.3	1.7	0.3	1.5	ns	12	5	1, 16	8	2
t_{PHL}	Propagation Delay High to Low (others)	0.3	1.5	0.3	1.7	0.3	1.5	ns	12	15	1, 16	8	2, 5

Quad 2-Input NOR Gate

ELECTRICALLY TESTED PER:
5962-8755701

The 10H502 is a quad 2-input **NOR** gate.The 10H502 provides one gate with **OR/NOR** outputs. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increases in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 40 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	OPEN
B_{IN}	6	10	8	51 Ω to V_{TT}
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$\overline{D_{OUT}}$	9	13	12	51 Ω to V_{TT}
C_{IN}	10	14	13	51 Ω to V_{TT}
C_{IN}	11	15	14	OPEN
D_{IN}	12	16	15	51 Ω to V_{TT}
D_{IN}	13	1	17	OPEN
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

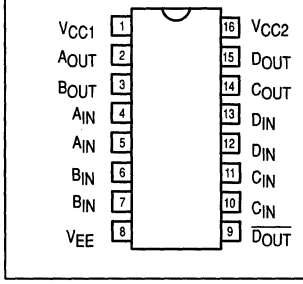
Military 10H502

AVAILABLE AS

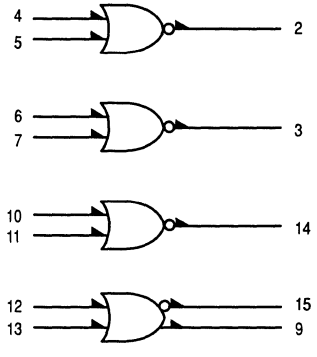
1) JAN: N/A
2) SMD: 5962-8755701
3) 883: 10H502/BXAJC
X = CASE OUTLINE AS FOLLOWS:

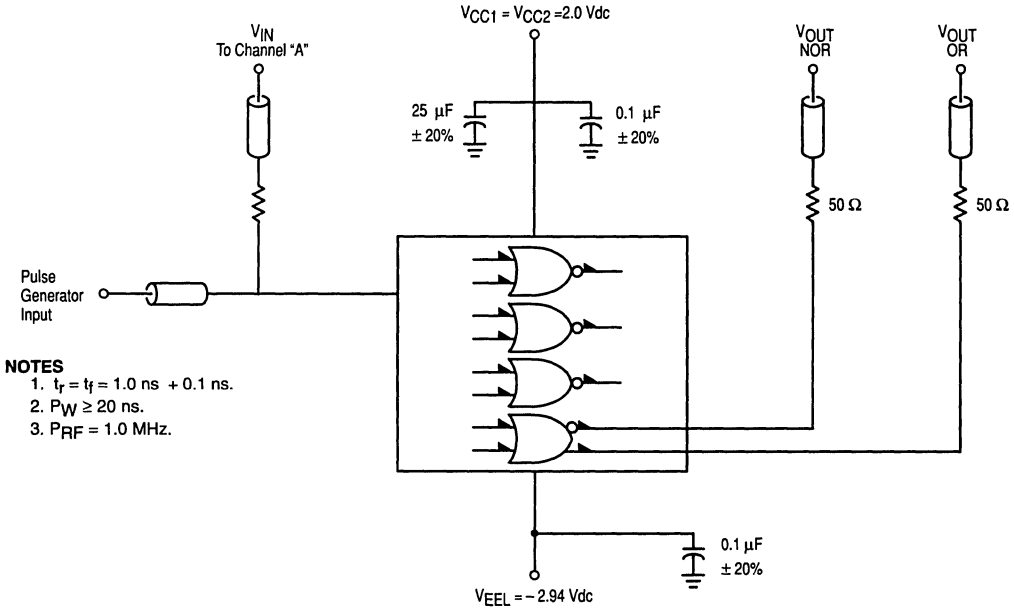
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES
1. $t_r = t_f = 1.0$ ns + 0.1 ns.
2. $P_W \geq 20$ ns.
3. $P_{RF} = 1.0$ MHz.

NOTES
1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 inches (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test should be connected to a 100 Ω resistor to ground.

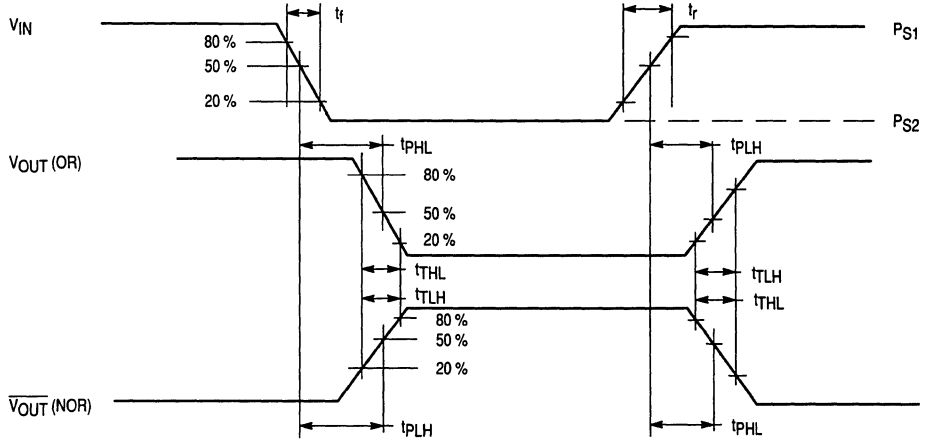


Figure 1. Switching Test Circuit and Waveforms

10H502
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = - 55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V	12, 13	4-7 12, 13			8		1, 16	2, 3, 9, 14, 15
V_{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	- 1.61	V	5-7 10-13	10-13			8		1, 16	2, 3, 9, 14, 15
V_{OH1}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V			12, 13	4, 6 10-13	8	8	1, 16	2, 9, 15
V_{OL1}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	-1.61	V			4-7 10-13	12, 13	8	8	1, 16	2, 9, 15
I_{EE}	Power Supply Current	- 26		- 29		- 29		mA					8		1, 16	8
I_{IH1}	Input Current High		265		425		425	µA	4, 7 10-13				8		1, 16	4, 7, 10-13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4-5 10-13			8		1, 16	4, 7, 10-13

10H502
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = - 55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.5	1.6	0.55	1.7	0.5	1.5	ns	5, 7, 11, 13	2, 3, 14, 9, 15	1, 16	8	2, 3, 9, 14, 15
t_{THL}	Fall time	0.5	1.6	0.55	1.7	0.5	1.5	ns	5, 7, 11, 13	2, 3, 14, 9, 15	1, 16	8	2, 3, 9, 14, 15
t_{PLH}	Propagation Delay Low to High	0.4	1.25	0.4	1.5	0.4	1.25	ns	5, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3, 9, 14, 15
t_{PHL}	Propagation Delay High to Low	0.4	1.25	0.4	1.5	0.4	1.25	ns	5, 7, 11, 13	2, 3, 14, 15	1, 16	8	2, 3, 9, 14, 15

MOTOROLA

Quad 2-Input OR Gate

Military 10H503

ELECTRICALLY TESTED PER:
5962-8756501

The 10H503 is a quad 2-input **OR** gate. The 10H503 provides one gate with **OR/NOR** outputs.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

2

- Propagation Delay, 1.0 ns Typical
- 40 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8756501
3) 883: 10H503/BXAJC
X = CASE OUTLINE AS FOLLOWS:

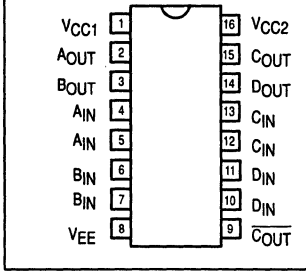
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

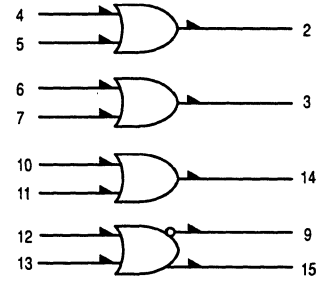
PIN ASSIGNMENTS

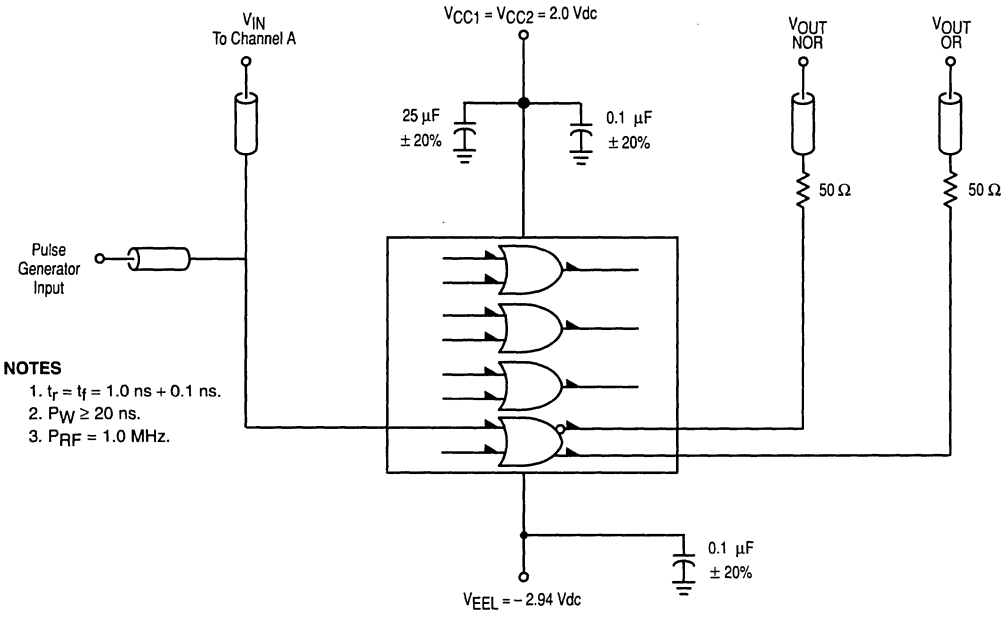
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	GND
A_{IN}	5	9	7	OPEN
B_{IN}	6	10	8	GND
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$\overline{C_{OUT}}$	9	13	12	51 Ω to V_{TT}
D_{IN}	10	14	13	GND
D_{IN}	11	15	14	OPEN
C_{IN}	12	16	15	GND
C_{IN}	13	1	17	OPEN
D_{OUT}	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM





NOTES

1. $t_r = t_f = 1.0$ ns + 0.1 ns.
2. $P_W \geq 20$ ns.
3. $P_{RF} = 1.0$ MHz.

NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 inches (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test should be connected to a 100 Ω resistor to ground.

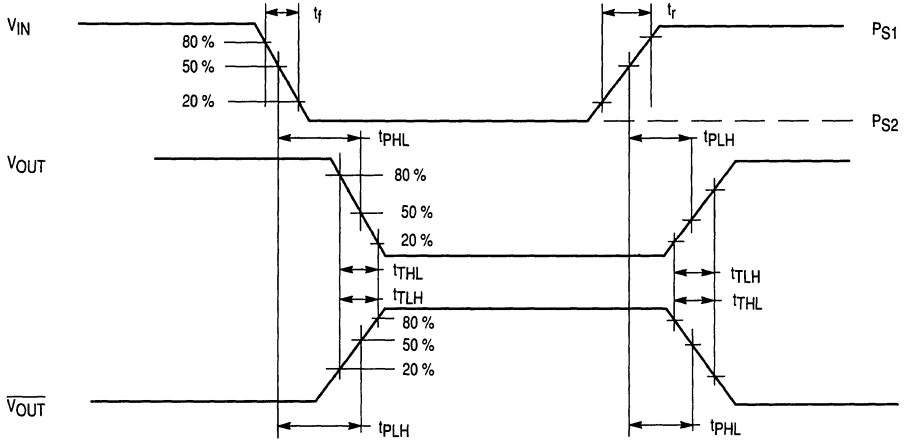


Figure 1. Switching Test Circuit and Waveforms

10H503
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V	4 - 7 10 - 13				8		1, 16	2, 3, 9, 14, 15
V_{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.363	- 1.95	- 1.61	V	12, 13	4 - 7 10 - 13			8		1, 16	2, 3, 9, 14, 15
V_{OH1}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V			4 - 7 10 - 13	12, 13	8	8	1, 16	2, 3, 9, 14, 15
V_{OL1}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.363	- 1.95	-1.61	V			12, 13	4 - 7 12, 13	8	8	1, 16	2, 3, 9, 14, 15
I_{EE}	Power Supply Current	- 26		- 29		- 29		mA					8		1, 16	8
I_{IH1}	Input Current High		265		425		425	µA	4 - 7 12, 13				8		1, 16	4 - 7, 10 - 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7 10 - 13				8	1, 16	4 - 7, 10 - 13

10H503
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.5	1.8	0.5	1.9	0.5	1.7	ns	5, 7, 11	2, 3, 14	1, 16	8	3, 9, 14, 15
t_{THL}	Fall time	0.5	1.8	0.5	1.9	0.5	1.7	ns	5, 7, 11	2, 3, 14	1, 16	8	3, 9, 14, 15
t_{PLH}	Propagation Delay Low to High	0.4	1.4	0.5	1.65	0.4	1.4	ns	13	9, 15	1, 16	8	2, 3, 9, 14
t_{PHL}	Propagation Delay High to Low	0.4	1.4	0.5	1.65	0.4	1.4	ns	13	9, 15	1, 16	8	2, 3, 14, 15

Quad 2-Input AND Gate

Military 10H504

ELECTRICALLY TESTED PER:
5962-8750401

The 10H504 is a quad 2-input **AND** gate. One of the gates has both **AND/NAND** outputs available.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 55 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

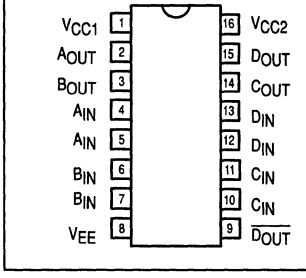
1) JAN: N/A
2) SMD: 5962-8750401
3) 883: 10H504/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

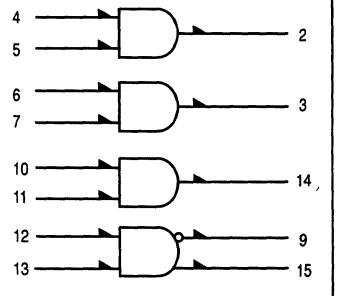
The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

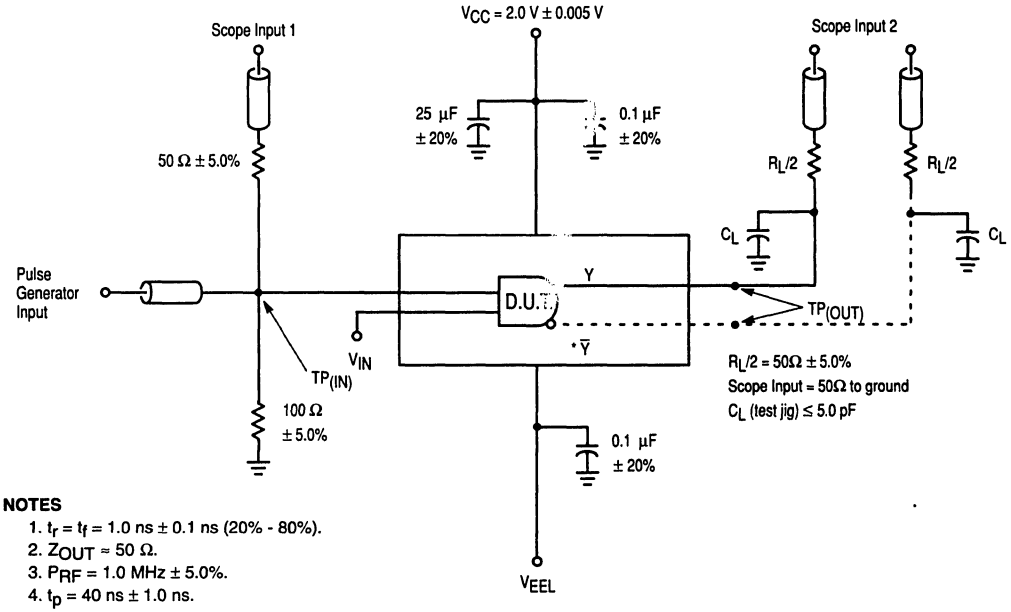
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	GND
A_{IN}	5	9	7	GND
B_{IN}	6	10	8	GND
B_{IN}	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
$\overline{D_{OUT}}$	9	13	12	51 Ω to V_{TT}
C_{IN}	10	14	13	GND
C_{IN}	11	15	14	GND
D_{IN}	12	16	15	GND
D_{IN}	13	1	17	GND
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



NOTES

1. $t_r = t_f$ = 1.0 ns ± 0.1 ns (20% - 80%).
2. $Z_{OUT} \approx$ 50 Ω.
3. P_{RF} = 1.0 MHz ± 5.0%.
4. t_p = 40 ns ± 1.0 ns.

NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 inches (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. * Applies to gate 4 only.

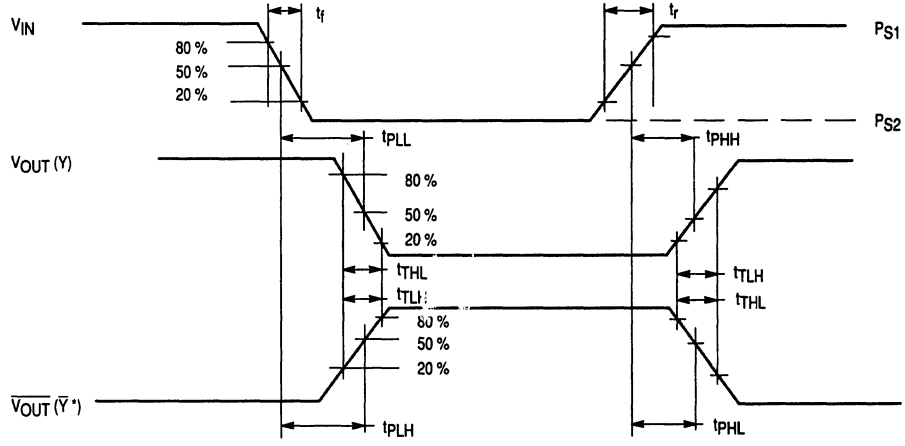


Figure 1. Switching Test Circuit and Waveforms

10H504
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.13	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V	4 - 7 10 - 13				8		1, 16	2, 3, 9, 14, 15
V_{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	- 1.61	V	4 - 7 10 - 13				8		1, 16	2, 3, 9, 14, 15
V_{OH1}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V	4 - 7 10 - 13		4 - 7 10 - 13	12, 13	8	8	1, 16	2, 3, 9, 14, 15
V_{OL1}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	-1.61	V	5 - 7 10 - 13		12, 13	4 - 7 10 - 13	8	8	1, 16	2, 3, 9, 14, 15
I_{EE}	Power Supply Current	- 35		- 39		- 39		mA					8		1, 16	8
I_{IH}	Input Current High		220		350		350	µA	5, 6 11, 12				8		1, 16	5, 6, 11, 12
I_{IH1}	Input Current High		265		425		425	µA	4, 7 10, 13				8		1, 16	4, 7, 10, 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4, 7, 10 12, 13				8	1, 16	4 - 7, 10 - 13

10H504
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.13	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{IH2}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.3	1.5	0.6	1.65	0.3	1.4	ns	4	2	5	1, 16	8	3, 9, 14, 15
t_{THL}	Fall time	0.3	1.5	0.6	1.65	0.3	1.4	ns	4	2	5	1, 16	8	3, 9, 14, 15
t_{PHL}	Propagation Delay High to Low	0.55	1.9	0.45	1.9	0.4	1.7	ns	4	2	5	1, 16	8	3, 9, 14, 15
t_{PHH}	Propagation Delay High to High	0.5	1.7	0.55	1.8	0.4	1.55	ns	4	2	5	1, 16	8	2, 3, 9,14
t_{PLL}	Propagation Delay Low to Low	0.4	1.6	0.45	1.75	0.4	1.6	ns	4	2	5	1, 16	8	2, 3, 9,14, 15
t_{PLH}	Propagation Delay Low to High	0.4	1.4	0.45	1.7	0.4	1.4	ns	13	9	12	1, 16	8	2, 3, 9,14, 15

Triple 2-3-2 Input OR/NOR Gate

ELECTRICALLY TESTED PER:
5962-8750701

The 10H505 is a triple 2-3-2 input **OR/NOR** gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

2

- Propagation Delay, 1.0 ns Typical
- 35 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	OPEN
A_{IN}	5	9	7	51 Ω to V_{TT}
$\overline{B_{OUT}}$	6	10	8	51 Ω to V_{TT}
B_{OUT}	7	11	9	51 Ω to V_{TT}
V_{EE}	8	12	10	V_{EE}
B_{IN}	9	13	12	51 Ω to V_{TT}
B_{IN}	10	14	13	OPEN
B_{IN}	11	15	14	OPEN
C_{IN}	12	16	15	OPEN
C_{IN}	13	1	17	51 Ω to V_{TT}
$\overline{C_{OUT}}$	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

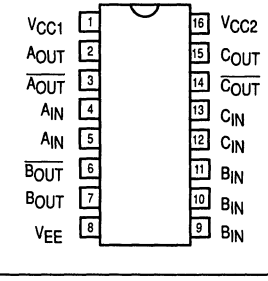
Military 10H505

AVAILABLE AS

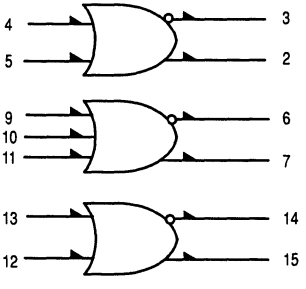
1) JAN: N/A
2) SMD: 5962-8750701
3) 883: 10H505/BXAJC
X = CASE OUTLINE AS FOLLOWS:

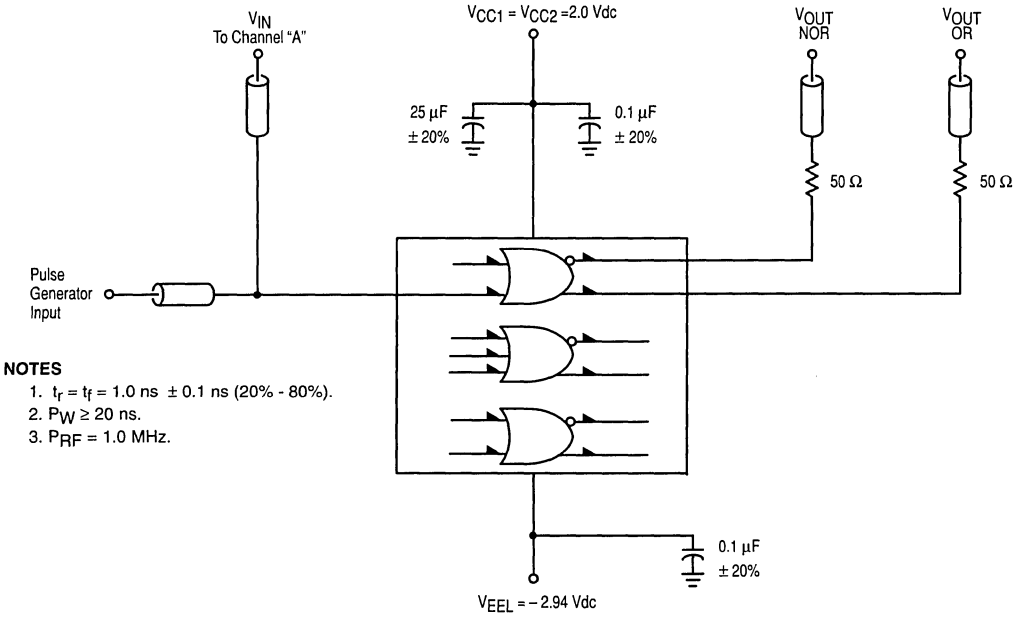
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. $t_r = t_f = 1.0$ ns ± 0.1 ns (20% - 80%).
2. $P_W \geq 20$ ns.
3. $P_{RF} = 1.0$ MHz.

NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 inches (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test should be connected to a 100 Ω resistor to ground.

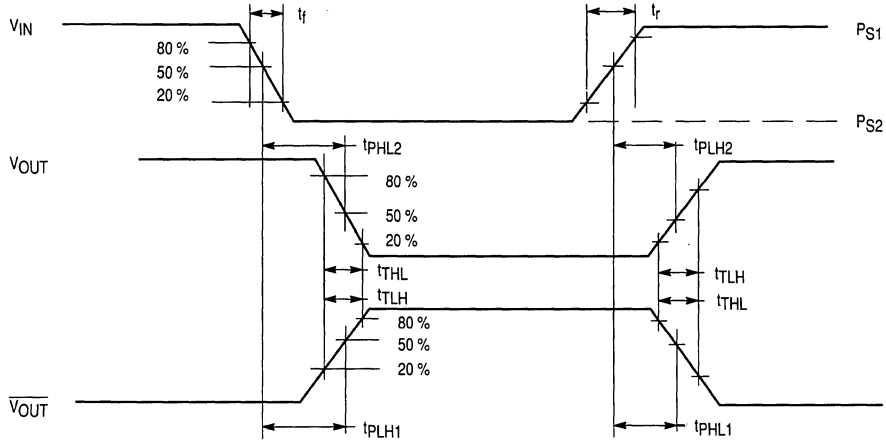


Figure 1. Switching Test Circuit and Waveforms

10H505
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = - 55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V	4, 5 9-13	4, 5 9-13			8		1, 16	2, 3, 6, 7, 14, 15
V_{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	- 1.61	V	4, 5 9-13	4, 5 9-13			8		1, 16	2, 3, 6, 7, 14, 15
V_{OH1}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V			4, 5 9-13	4, 5 9-13	8	8	1, 16	2, 3, 6, 7, 14, 15
V_{OL1}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	-1.61	V			4, 5 9-13	4, 5 9-13	8	8	1, 16	2, 3, 6, 7, 14, 15
I_{EE}	Power Supply Current	- 21		- 23		- 23		mA					8		1, 16	8
I_{IH1}	Input Current High		265		425		425	µA	4, 5 9-13				8		1, 16	4, 5 , 9 - 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4, 5 9-13				8	1, 16	4, 5, 9 - 13

10H505
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = - 55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{THL}	Fall Time	0.5	1.4	0.65	1.5	0.4	1.3	ns	4	3	1, 16	8	2, 6, 7, 14, 15
t_{TLH}	Rise Time	0.5	1.4	0.65	1.5	0.4	1.3	ns	4	3	1, 16	8	2, 3, 6, 7, 14, 15
t_{PHL1}	Propagation Delay High to Low	0.45	1.6	0.45	1.6	0.45	1.5	ns	4	2	1, 16	8	3, 6, 7, 14, 15
t_{PLH1}	Propagation Delay Low to High	0.4	1.4	0.4	1.6	0.4	1.2	ns	4	2	1, 16	8	3, 6, 7, 14, 15
t_{PHL2}	Propagation Delay High to Low	0.4	1.4	0.4	1.5	0.4	1.3	ns	4	2	1, 16	8	3, 6, 7, 14, 15
t_{PLH2}	Propagation Delay Low to High	0.45	1.4	0.45	1.6	0.45	1.5	ns	4	2	1, 16	8	3, 6, 7, 14, 15

Triple 4-3-3 Input NOR Gate

Military 10H506

ELECTRICALLY TESTED PER:
5962-8756401

The 10H506 is a Triple 4-3-3 input **NOR** gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply.

2

- Propagation Delay, 1.0 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8756401
3) 883: 10H506/BXAJC
X = CASE OUTLINE AS FOLLOWS:

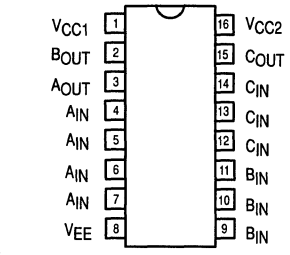
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

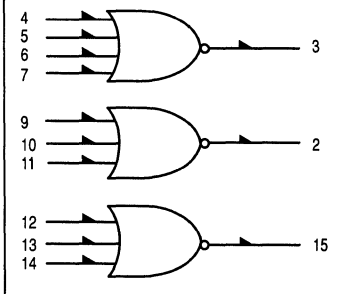
PIN ASSIGNMENTS

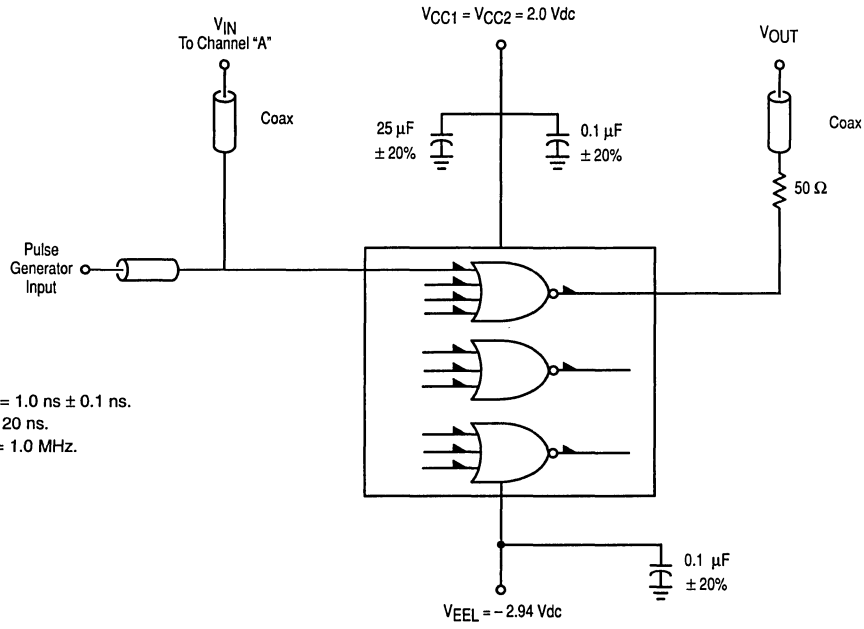
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
B_{OUT}	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	OPEN
A_{IN}	6	10	8	OPEN
A_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B_{IN}	9	13	12	OPEN
B_{IN}	10	14	13	51 Ω to V_{TT}
B_{IN}	11	15	14	OPEN
C_{IN}	12	16	15	OPEN
C_{IN}	13	1	17	OPEN
C_{IN}	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM





NOTES

1. $t_r = t_f = 1.0$ ns ± 0.1 ns.
2. $P_W \geq 20$ ns.
3. $P_{RF} = 1.0$ MHz.

NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test should be connected to a 100 Ω resistor to ground.

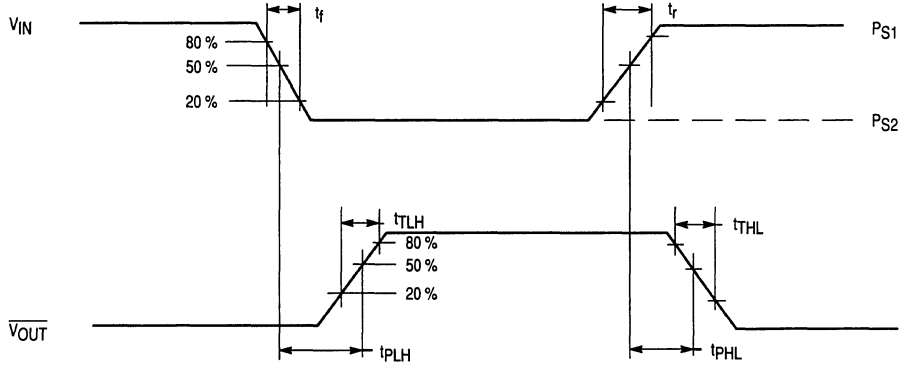


Figure 1. Switching Test Circuit and Waveforms

10H506
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V		4 - 7 9 - 14			8		1, 16	2, 3, 15
V_{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.363	- 1.95	- 1.61	V	4 - 7 9 - 14				8		1, 16	2, 3, 15
V_{OH1}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V				4 - 7 9 - 14	8	8	1, 16	2, 3, 15
V_{OL1}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.363	- 1.95	-1.61	V			4 - 7 9 - 14		8	8	1, 16	2, 3, 15
I_{EE}	Power Supply Current	- 21		- 23		- 23		mA					8		1, 16	8
I_{IH1}	Input Current High		310		500		500	µA	4 - 7 9 - 14				8		1, 16	4 - 7, 9 - 14
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7 9 - 14				8	1, 16	4 - 7, 9 - 14

10H506
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.6	1.8	0.55	1.9	0.5	1.7	ns	6	3	1, 16	8	2, 15
t_{THL}	Fall time	0.6	1.8	0.55	1.9	0.5	1.7	ns	10	2	1, 16	8	3, 15
t_{PHL}	Propagation Delay High to Low	0.5	1.75	0.55	1.8	0.5	1.7	ns	13	15	1, 16	8	2, 3
t_{PLH}	Propagation Delay Low to High	0.5	1.75	0.55	1.8	0.5	1.7	ns	13	15	1, 16	8	2, 3

Triple 2 Input Exclusive "OR"/Exclusive "NOR" Gate

Military 10H507

ELECTRICALLY TESTED PER:
5962-8772701

2

The 10H507 is a triple 2 input **Exclusive OR/NOR** gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 60 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8772701
3) 883: 10H507/BXAJC
X = CASE OUTLINE AS FOLLOWS:

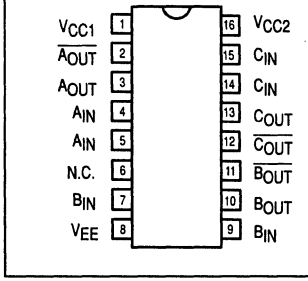
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

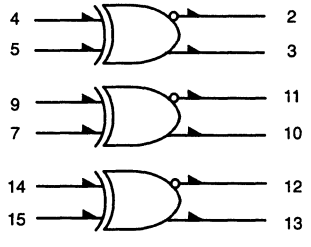
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{A_{OUT}}$	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	GND
A_{IN}	5	9	7	OPEN
N.C.	6	10	8	OPEN
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{CC}
B_{IN}	9	13	12	GND
B_{OUT}	10	14	13	51 Ω to V_{TT}
$\overline{B_{OUT}}$	11	15	14	51 Ω to V_{TT}
$\overline{C_{OUT}}$	12	16	15	51 Ω to V_{TT}
C_{OUT}	13	1	17	51 Ω to V_{TT}
C_{IN}	14	2	18	GND
C_{IN}	15	3	19	OPEN
V_{CC2}	16	4	20	GND

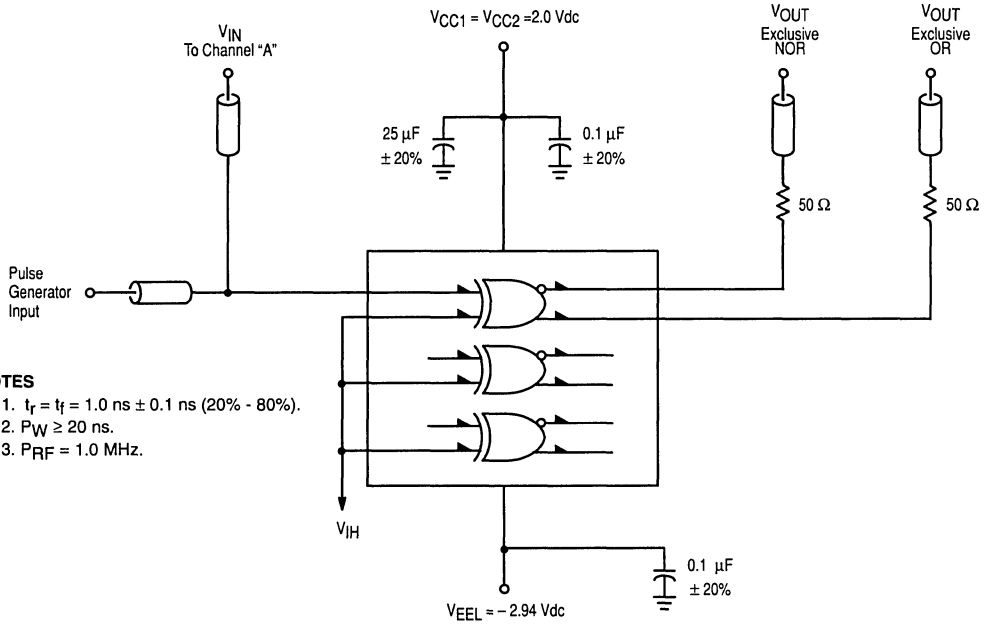
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM



$3 = (4 \bullet \overline{5}) + (\overline{4} \bullet 5)$
$2 = (\overline{4} \bullet \overline{5}) + (4 \bullet 5)$



NOTES

1. $t_r = t_f = 1.0$ ns ± 0.1 ns (20% - 80%).
2. $P_W \geq 20$ ns.
3. $P_{RF} = 1.0$ MHz.

NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 inches (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test should be connected to a 100 Ω resistor to ground.

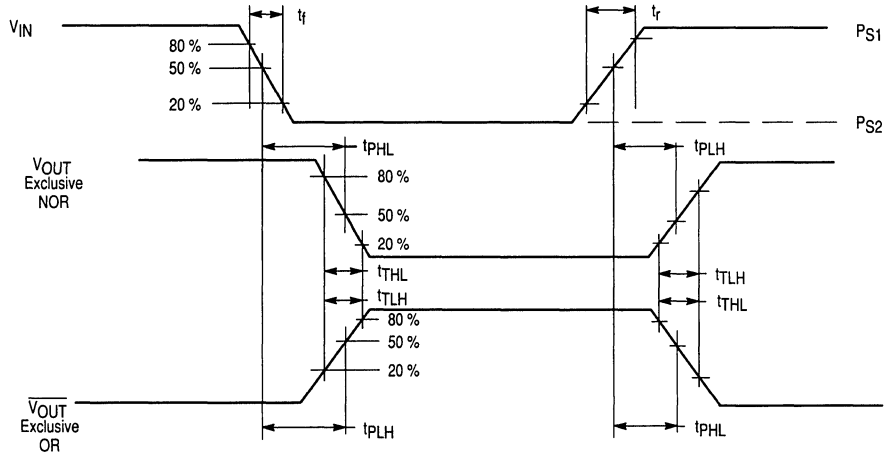


Figure 1. Switching Test Circuit and Waveforms

10H507
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	- 4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	- 4.94	-2.94
T_A = - 55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	- 4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V	4, 5, 7, 9, 14, 15	4, 5, 7, 9, 14, 15			8		1, 16	2, 3, 10-13
V_{OL}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	- 1.61	V	4, 5, 7, 9, 14, 15	4, 5, 7, 9, 14, 15			8		1, 16	2, 3, 10-13
V_{OH1}	High Output Voltage	- 1.01	- 0.78	-0.86	- 0.65	- 1.06	- 0.84	V		4, 7, 14	4, 5, 7, 9, 14, 15	4, 5, 7, 9, 14, 15	8	8	1, 16	2, 3, 10-13
V_{OL1}	Low Output Voltage	- 1.95	- 1.58	- 1.95	-1.565	- 1.95	-1.61	V	5, 9, 15		4, 5, 7, 9, 14, 15	4, 5, 7, 9, 14, 15	8	8	1, 16	2, 3, 10-13
I_{EE}	Power Supply Current	- 28		- 31		- 31		mA	5, 7, 15				8		1, 16	8
I_{IH}	Input Current High		220		425		425	µA	4, 9, 14				8		1, 16	4, 9, 14
I_{IH1}	Input Current High		265		425		425	µA	5, 7, 15				8		1, 16	5, 7, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4, 5, 7 9, 14, 15				8	1, 16	4, 5, 7, 9, 14, 15

10H507
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	- 4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	- 4.94	-2.94
T_A = - 55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	- 4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P.U.T.
t_{TLH}	Rise Time	0.5	1.6	0.5	1.9	0.5	1.5	ns	4	3	1, 16	8	5	5	2, 10-13
t_{THL}	Fall Time	0.5	1.6	0.5	1.9	0.5	1.5	ns	5	2	1, 16	8	5	5	3, 10-13
t_{PHL}	Propagation Delay High to Low	0.4	1.6	0.4	1.9	0.4	1.5	ns	7	11	1, 16	8	9	9	2, 3, 10, 12, 13
t_{PLH}	Propagation Delay Low to High	0.4	1.6	0.4	1.9	0.4	1.5	ns	14	13	1, 16	8	14	14	2, 3, 10-12

Dual 4-5 Input "OR/NOR" Gate

Military 10H509

ELECTRICALLY TESTED PER:
5962-8985601

2

The 10H509 is a dual 4-5 input **OR/NOR** gate. This MECL10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 40 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8985601
3) 883: 10H509/BXAJC
X = CASE OUTLINE AS FOLLOWS:

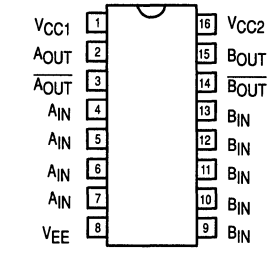
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

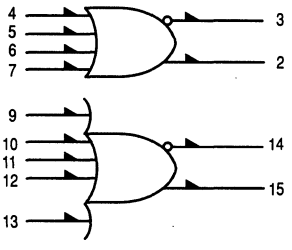
PIN ASSIGNMENTS

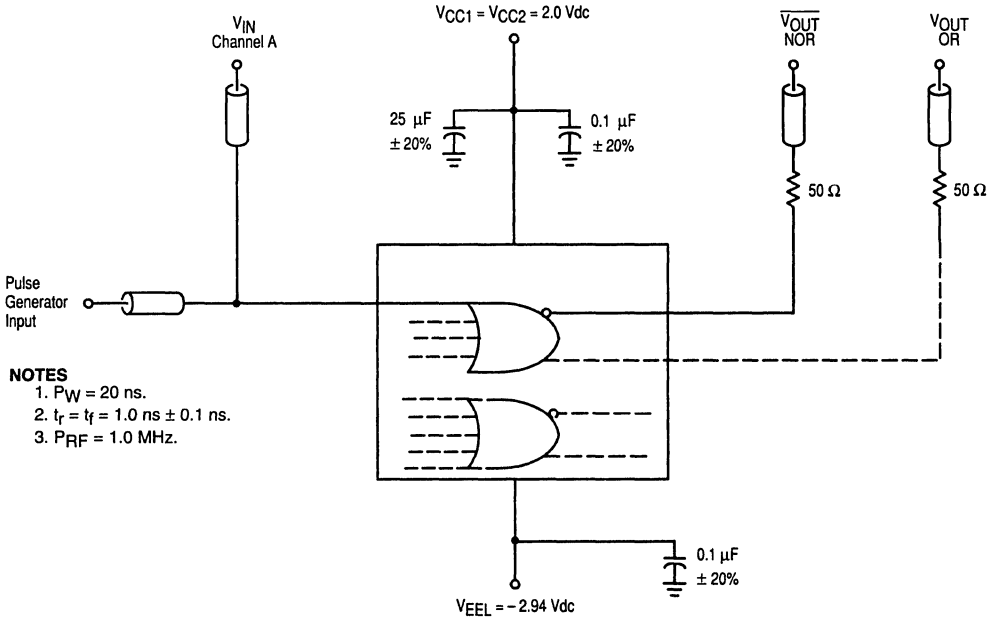
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	GND
A_{IN}	6	10	8	OPEN
A_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B_{IN}	9	13	12	OPEN
B_{IN}	10	14	13	OPEN
B_{IN}	11	15	14	OPEN
B_{IN}	12	16	15	GND
B_{IN}	13	1	17	51 Ω to V_{TT}
$\overline{B_{OUT}}$	14	2	18	51 Ω to V_{TT}
B_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



POSITIVE LOGIC DIAGRAM





NOTES
1. P_W = 20 ns.
2. $t_r = t_f$ = 1.0 ns ± 0.1 ns.
3. P_{RF} = 1.0 MHz.

NOTES
1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.

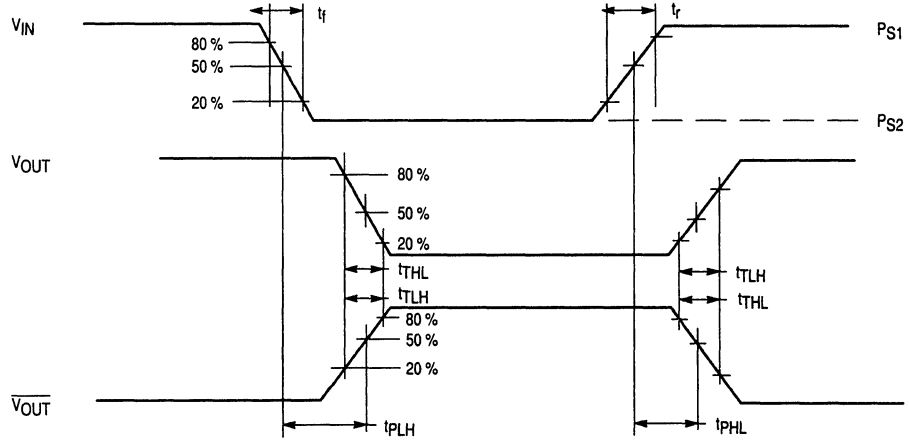


Figure 1. Switching Test Circuit and Waveforms

10H509
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}
T_A = 25 °C	–0.78	–1.95	–1.11	+0.31	–1.475	–1.105	0	–5.2
T_A = 125 °C	–0.65	–1.95	–0.96	+0.36	–1.400	–1.000	0	–5.2
T_A = –55 °C	–0.84	–1.95	–1.16	+0.28	–1.510	–1.255	0	–5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{CC}	V_{EE1}	P. U. T.
V_{OH}	High Output Voltage	–0.93	–0.78	–0.825	–0.63	–1.06	–0.88	v	4 – 7 9 – 13	4 – 7 9 – 13			1, 16	8	2, 3, 14, 15
V_{OL}	Low Output Voltage	–1.86	–1.62	–1.82	–1.545	–1.92	–1.655	V	4 – 7 9 – 13	4 – 7 9 – 13			1, 16	8	2, 3, 14, 15
V_{OTH}	High Output Voltage	–0.96		–0.845		–1.1		V			4 – 7 9 – 13	4 – 7 9 – 13	1, 16	8	2, 3, 14, 15
V_{OTL}	Low Output Voltage		–1.6		–1.525		–1.635	V			4 – 7 9 – 13	4 – 7 9 – 13	1, 16	8	2, 3, 14, 15
I_{EE}	Power Supply Current	–14		–16		– 16		mA					1, 16	8	8
I_{IH}	Input Current High		265		450		450	µA	4 – 7 9 – 13				1, 16	8	4 – 7, 9 – 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 – 7 9 – 13			1, 16	8	4 – 7, 9 – 13

10H509
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EEL}
T_A = 25 °C	–0.78	–1.85	–1.11	+0.31	–1.475	–1.105	0	–2.94
T_A = 125 °C	–0.63	–1.82	+1.24	+0.36	–1.400	–1.000	0	–2.94
T_A = –55 °C	–0.88	–1.92	+1.01	+0.28	–1.510	–1.255	0	–2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+25 °C		+125 °C		–55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.4	2.1	0.4	2.3	0.35	2.0	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	0.4	2.1	0.4	2.3	0.35	2.0	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High	0.3	1.3	0.45	1.6	0.25	1.3	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL}	Propagation Delay High to Low	0.3	1.3	0.45	1.6	0.25	1.3	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15

Quad Exclusive OR Gate

ELECTRICALLY TESTED PER:
5962-8755801

The 10H513 is a Quad Exclusive OR Gate with an enable common to all gates. The outputs may be wire-ORed together to perform a 4-bit comparison function (A = B). The enable is active LOW.

- 250 mW Max/Pkg (No Load)
- t_{pd} = 2.5 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	GND
A_{IN}	5	9	7	OPEN
B_{IN}	6	10	8	GND
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$\overline{Enable}$	9	13	12	OPEN
C_{IN}	10	14	13	GND
C_{IN}	11	15	14	OPEN
D_{IN}	12	16	15	GND
D_{IN}	13	1	17	OPEN
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Truth Table			
Input		$\overline{E}$	Output
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
Ø	Ø	H	L

Ø = Don't Care

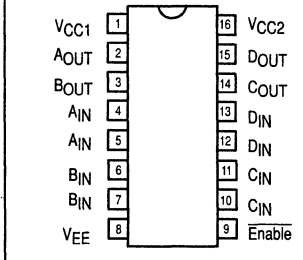
Military 10H513

AVAILABLE AS

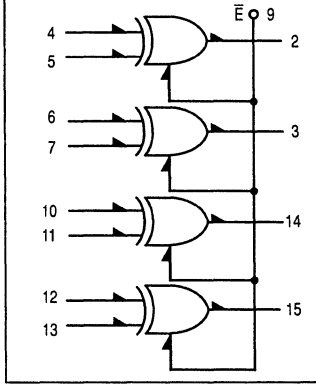
1) JAN: N/A
2) SMD: 5962-8755801
3) 883: 10H513/BXAJC
X = CASE OUTLINE AS FOLLOWS:

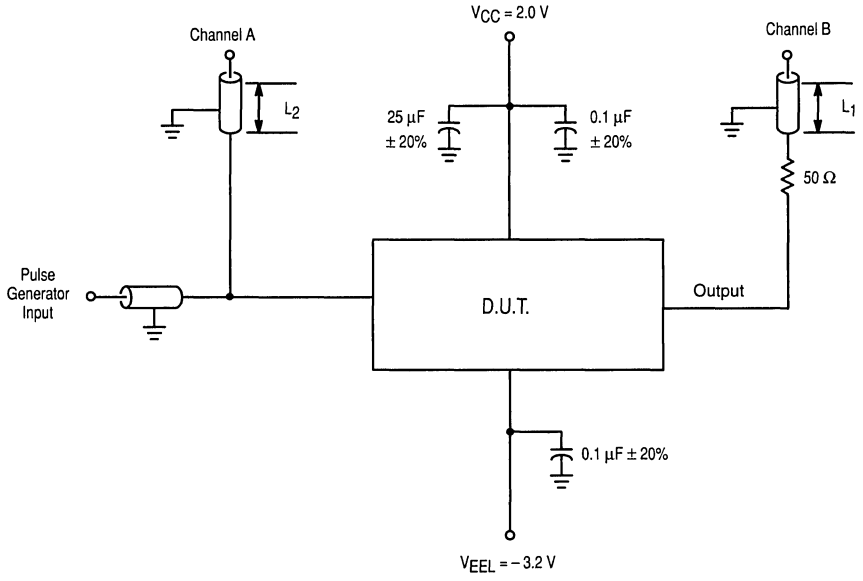
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



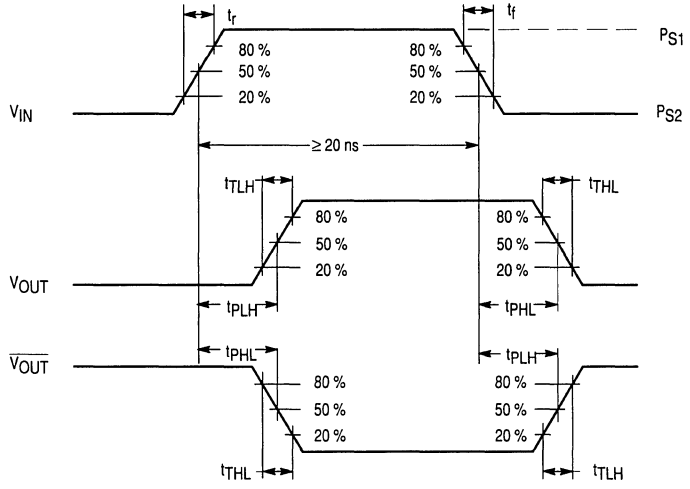
LOGIC DIAGRAM





NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. 2:1 divider may be used.
5. $L_1 = L_2$: Matched for equal time delays.



NOTES

1. $P_{IN} \geq 20$ ns.
2. f_{IN} = 1.0 MHz.
3. $t_r = t_f$ = 1.0 ns ± 0.1 ns

Figure 1. Switching Test Circuit and Waveforms

10H513
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{IL2}	V_{IH2}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	0	-5.46	-4.94
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	0	-5.46	-4.94
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	0	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	4 - 7 11, 13				8		1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V					8		1, 16	2, 3, 14, 15
V_{OHA}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	4 - 7 10 - 13		4 - 7 10 - 13	4 - 7 10 - 13		8	1, 16	2, 3, 14, 15
V_{OLA}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	4 - 7 10 - 13		4 - 7 10 - 13	4 - 7 10 - 13		8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	-42		-46		-46		mA					8		1, 16	8
I_{IH1}	Input Current High		320		510		510	µA	4, 6 10, 12				8		1, 16	4, 6, 10, 12
I_{H2}	Input Current High		270		430		430	µA	5, 7 11, 13				8		1, 16	5, 7, 11, 3
I_{H3}	Input Current High		740		1100		1100	µA	9				8		1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7 9 - 11 13, 14			8		1, 16	4 - 7, 9 - 13

10H513
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{IL2}	V_{IH2}	V_{CC}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	+2.0	-2.94
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	+2.0	-2.94
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	+2.0	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+25° C		+125° C		-55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P.U.T.
t_{TLH}	Rise Time	0.6	1.9	0.6	2.0	0.5	1.8	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15
t_{THL}	Fall Time	0.6	1.9	0.6	2.0	0.5	1.8	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15
t_{PLH} Data	Propagation Delay Low to High (A or B to Out)	0.4	1.8	0.5	1.9	0.4	1.7	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15
t_{PHL} Data	Propagation Delay High to Low (A or B to Out)	0.4	1.8	0.5	1.9	0.4	1.7	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15
t_{PLH} Enable	Propagation Delay Low to High (Enable to Out)	0.5	2.4	0.6	2.5	0.5	2.3	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15
t_{PHL} Enable	Propagation Delay High to Low (Enable to Out)	0.5	2.4	0.6	2.5	0.5	2.3	ns	4, 5	2	1, 16	8	4, 5	4, 5	3, 14, 15

Quad Line Receiver

Military 10H515

ELECTRICALLY TESTED PER:
5962-87501

2

The 10H515 is a quad differential amplifier designed for use in sensing differential signals over long lines. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in counting frequency, and no increase in power-supply current.

The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary. Active current sources provide the 10H515 with excellent common mode rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.

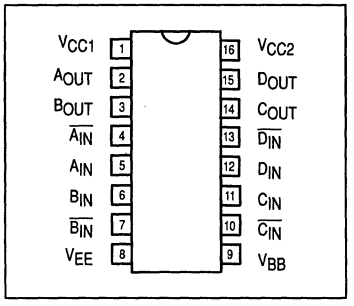
- Propagation Delay, 1.0 ns Typical
- 160 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-87501
3) 883: 10H515/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

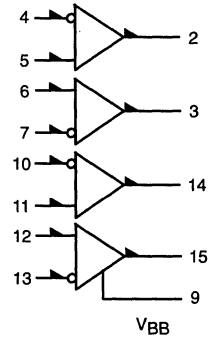
The letter "M" appears before the slash on LCC.



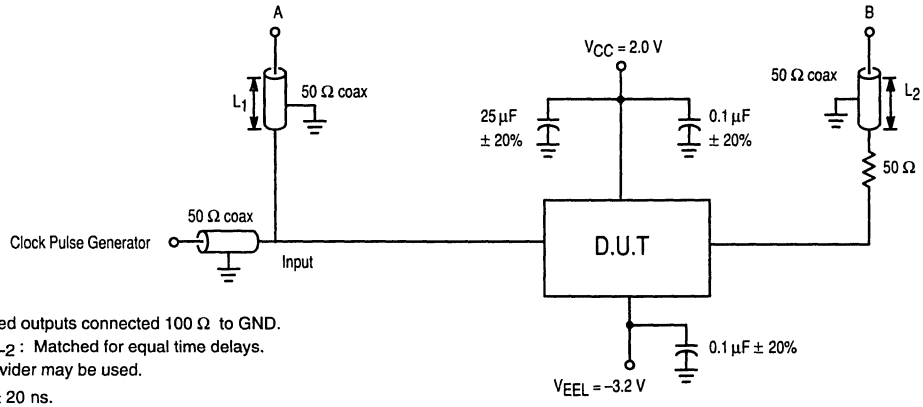
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
$\overline{A_{IN}}$	4	8	5	V_{BB}
A_{IN}	5	9	7	GND
B_{IN}	6	10	8	GND
$\overline{B_{IN}}$	7	11	9	V_{BB}
V_{EE}	8	12	10	V_{EE}
V_{BB}	9	13	12	V_{BB}
$\overline{C_{IN}}$	10	14	13	V_{BB}
C_{IN}	11	15	14	GND
D_{IN}	12	16	15	GND
$\overline{D_{IN}}$	13	1	17	V_{BB}
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN
V_{BB} = All pins designated for V_{BB} must be tied together, no external voltage applied.



NOTES

1. Unused outputs connected 100 Ω to GND.
2. $L_1 = L_2$: Matched for equal time delays.
3. 2:1 divider may be used.
4. $P_W \geq 20$ ns.
5. $P_{RF} = 1.0$ MHz.
6. $t_r = t_f = 1.0$ ns ± 0.1 ns measured at (20% - 80%).

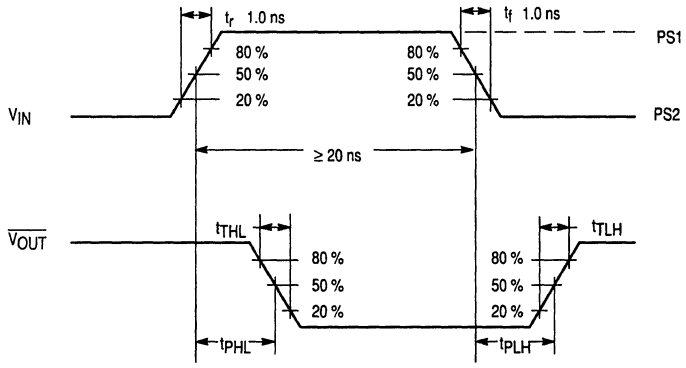


Figure 1. Switching Test Circuit and Waveforms

10H515
QUIESCENT LIMIT TABLE

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{CB}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-5.2
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-5.2
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V, V_{CB} = -5.2 V.								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	V_{BB}	(PUT) LD_1
V_{OH}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	** 5, 6, 11, 12	** 4, 7, 10, 13			8		1, 16		2, 3, 14, 15
V_{OL}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	** 4, 7, 10, 13	** 5, 6, 11, 12			8		1, 16		2, 3, 14, 15
V_{OH1}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V			** 5, 6, 11, 12	** 4, 7, 10, 13	8	8	1, 16		2, 3, 14, 15
V_{OL1}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V			** 4, 7, 10, 13	** 5, 6, 11, 12	8	8	1, 16		2, 3, 14, 15
V_{BB1}	Reference Voltage	–1.37	–1.25	–1.31	–1.19	–1.41	–1.27	V					8		1, 16		*** 9
I_{EE}	Power Supply Current	–26		–29		–29		mA					8		1, 16		8
I_{IH}	Input Current High		95		150		150	µA	4 – 7, 10 – 13				8		1, 16		4 – 7, 10 – 13
I_{CBO}	Input Current	–1.0		–1.0		–1.5		µA					8		1, 16	** 4 – 7, 10 – 13	4 – 7, 10 – 13

** connected to pin 9.
*** Measure voltage on pin 9, while it is connected to other pins.

10H515
QUIESCENT LIMIT TABLE

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-2.94	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-2.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.5	1.4	0.5	1.7	0.5	1.4	ns	4	2	1, 16	8	3, 14, 15
t_{THL}	Fall Time	0.5	1.4	0.5	1.7	0.5	1.4	ns	7	3	1, 16	8	2, 14, 15
t_{PHL}	Propagation Delay High to Low	0.45	1.2	0.5	1.8	0.45	1.2	ns	10	14	1, 16	8	2, 3, 15
t_{PLH}	Propagation Delay Low to High	0.45	1.2	0.5	1.4	0.45	1.2	ns	13	14	1, 16	8	2, 3, 14

MOTOROLA

Triple Line Receiver

ELECTRICALLY TESTED PER:
5962-8750201

The 10H516 is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 125 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{A_{OUT}}$	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
$\overline{A_{IN}}$	4	8	5	GND
A_{IN}	5	9	7	V_{BB}
$\overline{B_{OUT}}$	6	10	8	51 Ω to V_{TT}
B_{OUT}	7	11	9	51 Ω to V_{TT}
V_{EE}	8	12	10	V_{EE}
$\overline{B_{IN}}$	9	13	12	GND
B_{IN}	10	14	13	V_{BB}
V_{BB}	11	15	14	V_{BB}
$\overline{C_{IN}}$	12	16	15	GND
C_{IN}	13	1	17	V_{BB}
$\overline{C_{OUT}}$	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN
V_{BB} = All pins designated for V_{BB} must be tied together, no external voltage applied.

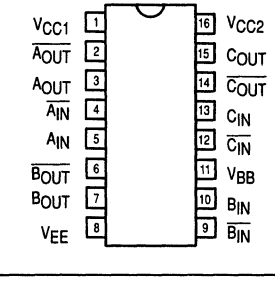
Military 10H516

AVAILABLE AS

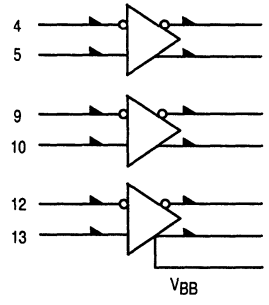
1) JAN: N/A
2) SMD: 5962-8750201
3) 883: 10H516/BXAJC
X = CASE OUTLINE AS FOLLOWS:

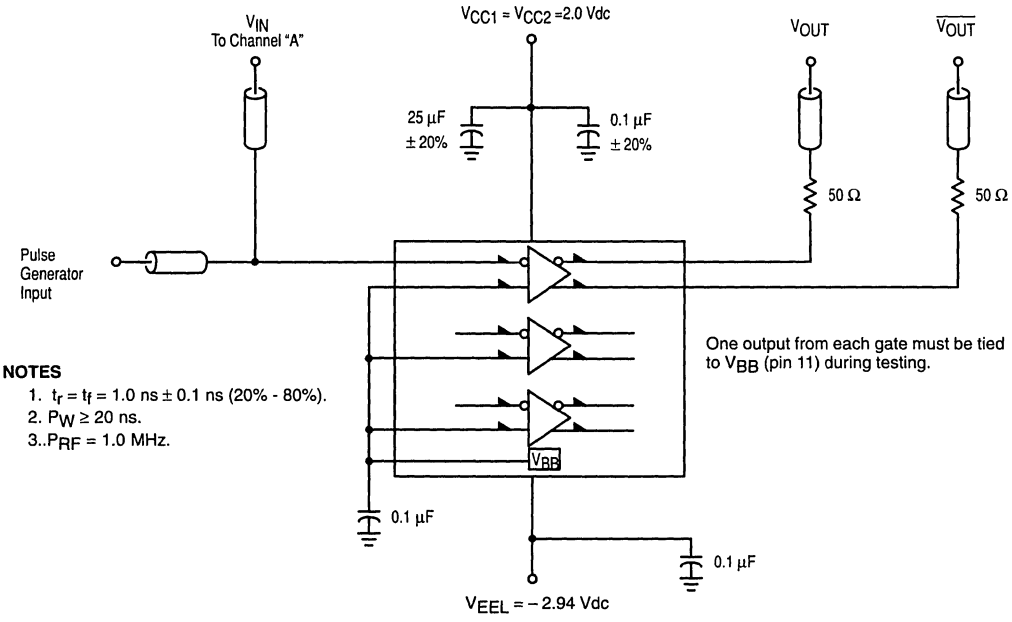
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. $t_r = t_f = 1.0$ ns ± 0.1 ns (20% - 80%).
2. $P_W \geq 20$ ns.
3. $P_{RF} = 1.0$ MHz.

NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 inches (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test should be connected to a 100 Ω resistor to ground.

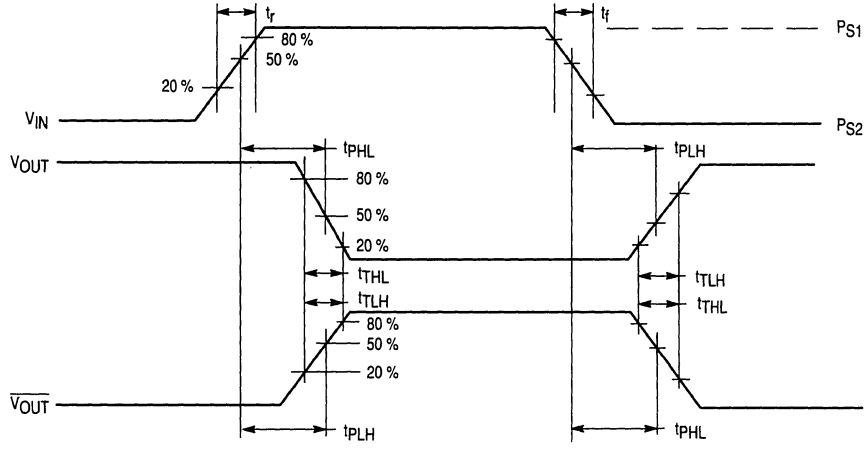


Figure 1. Switching Test Circuit and Waveforms

10H516
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 V.

Test Temperature	Test Voltage Values (Volts)									
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}	V_{CB}
T_A = 25°C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	-5.2
T_A = 125°C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	-5.2
T_A = -55°C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	V_{BB}	V_{CB}	P. U. T.
V_{OH}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13			8		1, 16			2, 3, 6, 7, 14, 15
V_{OL}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	4, 5, 9, 10, 12, 13, 14	4, 5, 9, 10, 12			8		1, 16			2, 3, 6, 7, 14, 15
V_{OH1}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 10, 13	8	8	1, 16	4, 5, 9, 11, 12		2, 3, 6, 7, 14, 15
V_{OL1}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 11, 12	4, 5, 9, 10, 13	8	8	1, 16	4, 5, 9, 11, 12		2, 3, 6, 7, 14, 15
V_{BB1}	Reference Voltage**	–1.37	–1.25	–1.31	–1.15	–1.41	–1.27	V						8	1, 16			11
I_{EE}	Power Supply Current	–21		–23		–23		mA	4, 9, 12	5, 10, 13			8		1, 16			8
I_{IH}	Input Current High		140		235		235	µA	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13			8		1, 16			4, 5, 9, 10, 12, 13
I_{CBO}	Input Leakage Current	–1.0		–1.0		–1.5		µA	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13				8	1, 16	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13

** For V_{BB1} connect pin 5, 10, 13 to pin 11.

10H516
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)									
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}	V_{CB}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94	-5.2
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94	-5.2
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE1}	P.U.T
t_{TLH}	Rise Time	0.4	1.35	0.4	1.5	0.4	1.25	ns	12	15	1, 16	8	2, 3, 6, 7, 14, 15
t_{THL}	Fall Time	0.4	1.35	0.4	1.5	0.4	1.25	ns	12	15	1, 16	8	2, 3, 6, 7, 14, 15
t_{PHL}	Propagation Delay	0.4	1.4	0.4	1.6	0.4	1.3	ns	4	2	1, 16	8	2, 3, 6, 7, 14, 15
t_{PLH}	Propagation Delay	0.4	1.4	0.4	1.6	0.4	1.3	ns	4	2	1, 16	8	2, 3, 6, 7, 14, 15

Dual 2-Wide 2-3-Input "OR-AND/OR-AND-INVERT" Gate

Military 10H517

ELECTRICALLY TESTED PER:
MPG 10H517

2

The 10H517 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates. This MECL 10H part is a functional pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 160 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

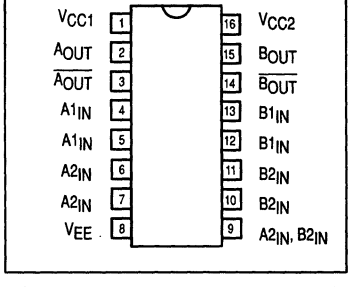
1) JAN: N/A
2) SMD: N/A
3) 883: 10H517/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

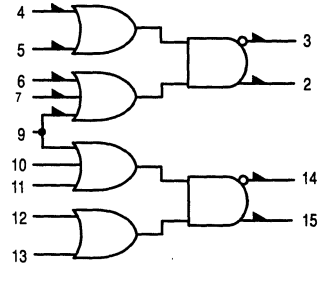
The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

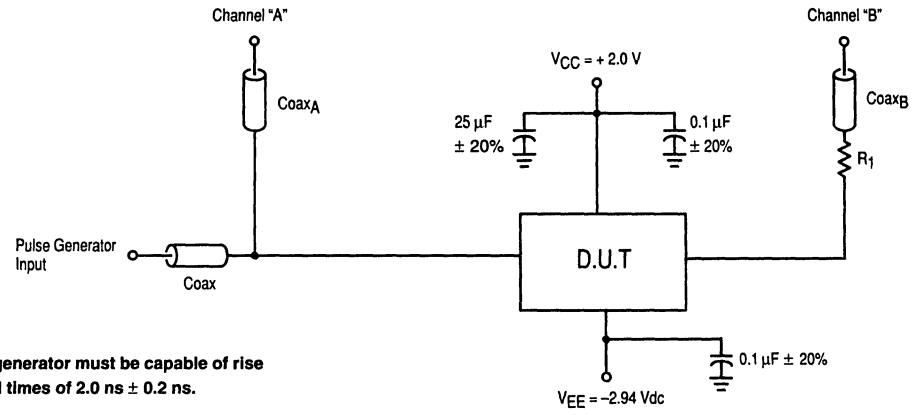
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V_{TT}
$A1_{IN}$	4	8	5	OPEN
$A1_{IN}$	5	9	7	OPEN
$A2_{IN}$	6	10	8	OPEN
$A2_{IN}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$A2_{IN}$, $B2_{IN}$	9	13	12	OPEN
$B2_{IN}$	10	14	13	OPEN
$B2_{IN}$	11	15	14	OPEN
$B1_{IN}$	12	16	15	OPEN
$B1_{IN}$	13	1	17	OPEN
$\overline{B_{OUT}}$	14	2	18	51 Ω to V_{TT}
B_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.

NOTES
1. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
2. Unused outputs should be loaded 100 Ω to ground.
3. 2:1 divider may be used.
4. $t_r = t_f = 1.0$ ns ± 0.1 ns measured at (20% - 80%).
5. $P_W \geq 20$ ns.
6. $P_{RF} = 1.00$ MHz.
7. $R_1 = 50$ Ω resistor in series with 50 Ω coax constituting the 100 Ω load.

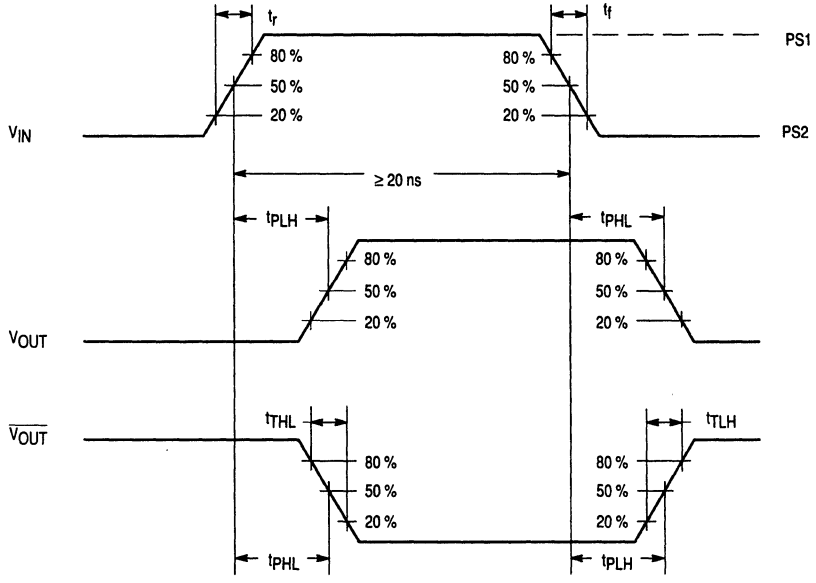


Figure 1. Switching Test Circuit and Waveforms

10H517
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.13	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.63	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125°C		- 55°C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	4 - 7 9 - 13				8		1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	4 - 7 9 - 13				8		1, 16	2, 3, 14, 15
V_{OHA}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	4 - 7 9 - 13		4 - 7 9 - 13	4 - 7 9 - 13	8	8	1, 16	2, 3, 14, 15
V_{OLA}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	4 - 7 9 - 13		4 - 7 9 - 13	4 - 7 9 - 13	8	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	-26		-29		-29		mA					8		1, 16	8
I_{IH1}	Input Current High		320		510		510	µA	4, 5, 12, 13				8		1, 16	4, 5, 12, 13
I_{IH2}	Input Current High		365		590		590	µA	6, 7 10, 11				8		1, 16	6, 7, 10, 11
I_{IH3}	Input Current High		460		755		755	µA	9				8		1, 16	9
I_{IL}	Input Current Low	0.3		0.3		0.5		µA		4 - 7 9 - 13			8		1, 16	7, 9 - 13

10H517
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.13	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.63	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T.
t_{TLH}	Rise Time	0.5	1.6	0.5	1.7	0.5	1.5	ns	4, 6, 11 12	2, 14, 15	1, 16	8	4, 6 11, 12	2, 3, 14, 15
t_{THL}	Fall Time	0.5	1.6	0.5	1.7	0.5	1.5	ns	4, 6, 11 12	2, 14, 15	1, 16	8	4, 6 11, 12	2, 3, 14, 15
t_{PHL}	Propagation Delay High to Low	0.54	1.62	0.6	1.8	0.54	1.62	ns	4, 6, 11 12	2, 14, 15	1, 16	8	4, 6 11, 12	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High	0.54	1.62	0.6	1.8	0.54	1.62	ns	4, 6, 11 12	2, 14, 15	1, 16	8	4, 6 11, 12	2, 3, 14, 15

Dual 2-Wide 3-Input "OR-AND" Gate

ELECTRICALLY TESTED PER:
5962-8755901

The 10H518 is a basic logic building block providing the **OR/AND** function, useful in data control and digital multiplexing applications.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 160 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$A1_{IN}$	3	7	4	OPEN
$A1_{IN}$	4	8	5	OPEN
$A1_{IN}$	5	9	7	GND
$A2_{IN}$	6	10	8	GND
$A2_{IN}$	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
$A2_{IN}$, $B2_{IN}$	9	13	12	GND
$B2_{IN}$	10	14	13	GND
$B2_{IN}$	11	15	14	OPEN
$B1_{IN}$	12	16	15	GND
$B1_{IN}$	13	1	17	OPEN
$B1_{IN}$	14	2	18	OPEN
B_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

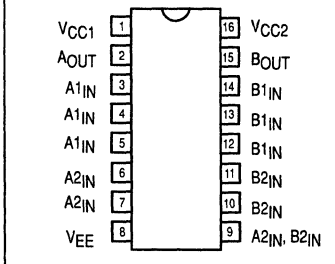
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

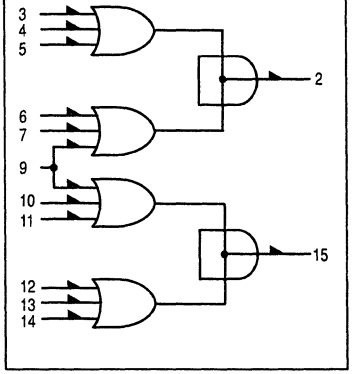
1) JAN: N/A
2) SMD: 5962-8755901
3) 883: 10H518/BXAJC
X = CASE OUTLINE AS FOLLOWS:

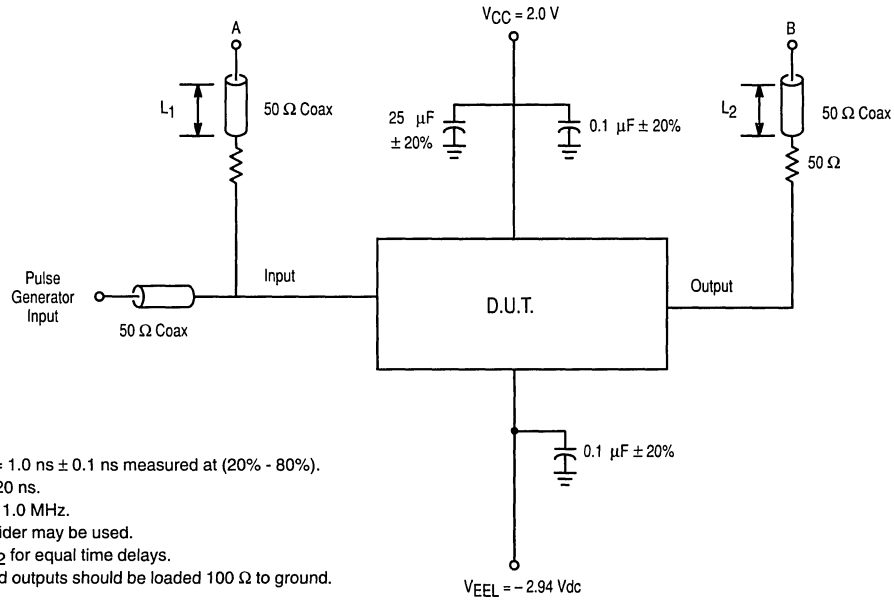
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. $t_r = t_f$ = 1.0 ns ± 0.1 ns measured at (20% - 80%).
2. $P_W \geq$ 20 ns.
3. P_{RF} = 1.0 MHz.
4. 2:1 divider may be used.
5. $L_1 = L_2$ for equal time delays.
6. Unused outputs should be loaded 100 Ω to ground.

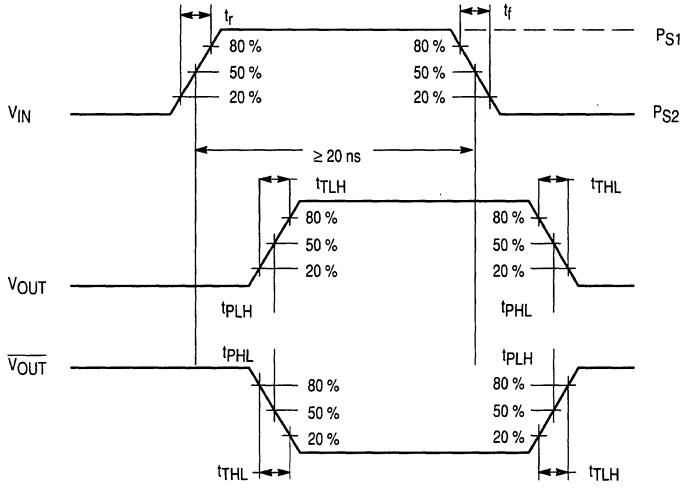


Figure 1. Switching Test Circuit and Waveforms

10H518
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.450	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 14				8		1, 16	2, 15
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	10, 13	3 - 7 9 - 14			8		1, 16	2, 15
V_{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 14	3 - 7 9 - 14	3 - 7 9 - 14		8	8	1, 16	2, 15
V_{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	3 - 7 9 - 14	3 - 7 9 - 14		3 - 7 9 - 14	8	8	1, 16	2, 15
I_{EE}	Power Supply Current	-26		-29		-29		mA					8		1, 16	8
I_{IH}	Input Current High		275		465		465	µA	3 - 5 12 - 14				8		1, 16	3 - 5, 12 - 14
I_{IH1}	Input Current High		320		545		545	µA	6, 7 10, 11				8		1, 16	6, 7, 10, 11
I_{IH2}	Input Current High		415		710		710	µA	9				8		1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 7 9 - 14				8	1, 16	3 - 7, 9 - 14

10H518
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.450	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T
t_{TLH}	Rise Time	0.5	1.6	0.5	1.7	0.5	1.5	ns	9	15	1, 16	8	5, 6, 14	2
t_{THL}	Fall Time	0.5	1.6	0.5	1.7	0.5	1.5	ns	9	15	1, 16	8	5, 6, 14	2
t_{PHL}	Propagation Delay	0.5	1.7	0.55	1.85	0.5	1.7	ns	4	2	1. 16	8	9, 13	15
t_{PLH}	Propagation Delay	0.5	1.7	0.55	1.85	0.5	1.7	ns	4	2	1. 16	8	9, 13	15

4-Wide 4-3-3-3 Input "OR-AND" Gate

Military 10H519

ELECTRICALLY TESTED PER:
5962-8772801

The 10H519 is a 4-wide 4-3-3-3 input **OR/AND** gate with one input from two gates common to pin 10.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 160 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8772801
3) 883: 10H519/BXAJC
X = CASE OUTLINE AS FOLLOWS:

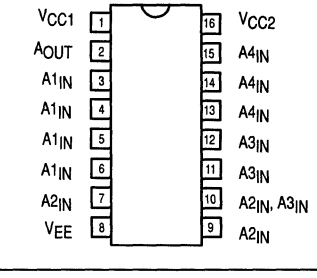
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

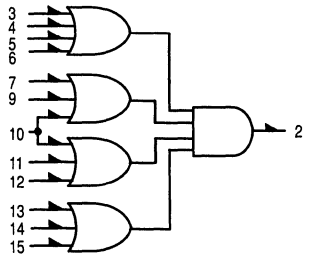
PIN ASSIGNMENTS

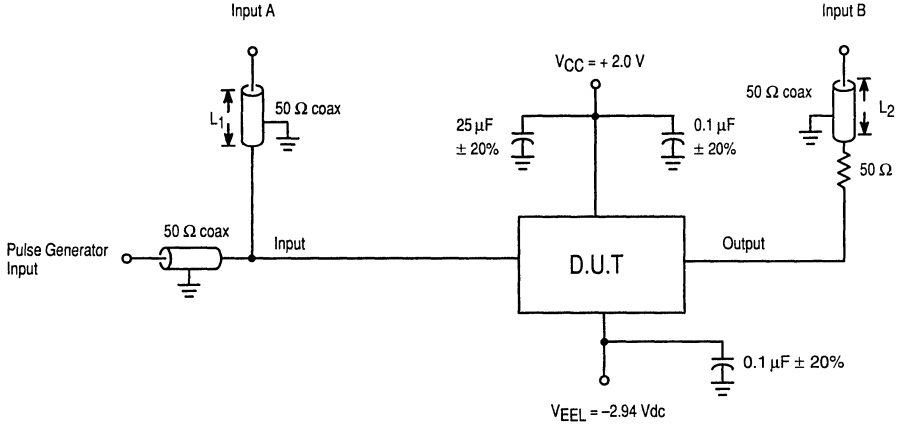
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$A1_{IN}$	3	7	4	GND
$A1_{IN}$	4	8	5	OPEN
$A1_{IN}$	5	9	7	OPEN
$A1_{IN}$	6	10	8	OPEN
$A2_{IN}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$A2_{IN}$	9	13	12	OPEN
$A2_{IN}$, $A3_{IN}$	10	14	13	GND
$A3_{IN}$	11	15	14	OPEN
$A3_{IN}$	12	16	15	OPEN
$A4_{IN}$	13	1	17	OPEN
$A4_{IN}$	14	2	18	OPEN
$A4_{IN}$	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM





NOTES

1. All other outputs loaded 100 Ω to GND.
2. $L_1 = L_2$: Matched for equal time delays.
3. $P_W \geq 20$ ns.
4. $P_{RF} = 1.0$ MHz.
5. $t_r = t_f = 1.0$ ns ± 0.1 ns.

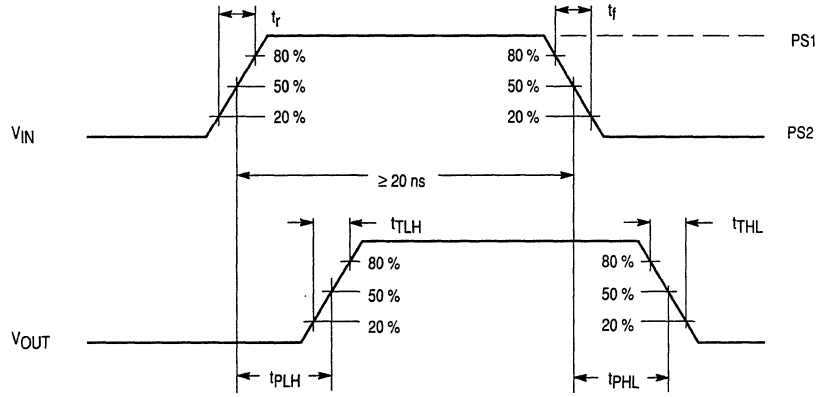


Figure 1. Switching Test Circuit and Waveforms

10H519
QUIESCENT LIMIT TABLE*

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-2.94	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-2.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	3 – 7 9 – 15				8		1, 16	2
V_{OL}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	3, 7, 10 11, 13	3 – 7 9 – 15			8		1, 16	2
V_{OH1}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	3 – 7 9 – 15	3 – 7 9 – 15	3 – 7 9 – 15		8	8	1, 16	2
V_{OL1}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	3 – 7 9 – 15	3 – 7 9 – 15		3 – 7 9 – 15	8	8	1, 16	2
I_{EE}	Power Supply Current	–26		–29		–29		mA					8		1, 16	8
I_{IH}	Input Current High		295		500		500	μA	3 – 7 9 – 15				8		1, 16	3 – 7 9 – 15
I_{IH1}	Input Current High		360		610		610	μA	10				8		1, 16	10
I_{IL}	Input Current Low	0.5		0.3		0.5		μA		3 – 7 9 – 15				8	1, 16	3 – 7 9 – 15

10H519
QUIESCENT LIMIT TABLE*

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-2.94	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-2.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T
t_{TLH}	Rise Time	0.8	2.0	0.8	2.3	0.8	1.9	ns	10	2	1, 16	8	4, 14	2
t_{THL}	Fall Time	0.8	2.0	0.8	2.3	0.8	1.9	ns	10	2	1, 16	8	4, 14	2
t_{PLH}	Propagation Delay Pin 10	0.75	2.25	0.8	2.55	0.75	2.2	ns	4	2	1. 16	8	7, 12, 13	2
t_{PHL}	Propagation Delay Pin 10	0.75	2.25	0.8	2.55	0.75	2.2	ns	4	2	1. 16	8	7, 12, 13	2
t_{PHL}	Propagation Delay Exclude Pin 10	0.75	2.5	0.8	2.8	0.75	2.4	ns	4	2	1. 16	8	7, 12, 13	2
t_{PLH}	Propagation Delay Exclude Pin 10	0.75	2.5	0.8	2.8	0.75	2.4	ns	4	2	1. 16	8	7, 12, 13	2

4-Wide "OR-AND/OR-AND-INVERT" Gate

Military 10H521

ELECTRICALLY TESTED PER:
5962-8773001

2

The 10H521 is a basic logic building block providing the simultaneous OR-AND/OR-AND-INVERT function, used in data control and digital multiplexing applications.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increases in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 40 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8773001
3) 883: 10H521/BXAJC
X = CASE OUTLINE AS FOLLOWS:

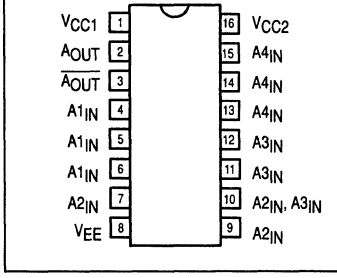
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

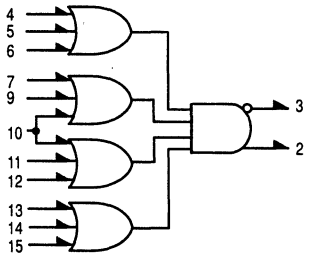
PIN ASSIGNMENTS

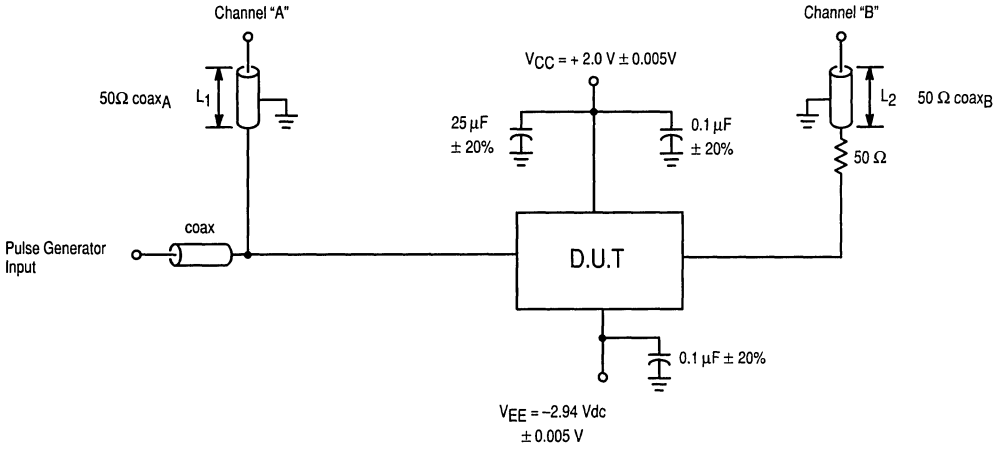
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	GND
$A1_{IN}$	4	8	5	OPEN
$A1_{IN}$	5	9	7	OPEN
$A1_{IN}$	6	10	8	OPEN
$A2_{IN}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$A2_{IN}$	9	13	12	OPEN
$A2_{IN}$, $A3_{IN}$	10	14	13	GND
$A3_{IN}$	11	15	14	OPEN
$A3_{IN}$	12	16	15	OPEN
$A4_{IN}$	13	1	17	OPEN
$A4_{IN}$	14	2	18	OPEN
$A4_{IN}$	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM





NOTES

1. All input and output cables to the scope are equal length of 50 Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test are connected to a 100 Ω resistor to ground.
3. $t_r = t_f = 1.0$ ns ± 0.1 ns.
4. $P_W \geq 20$ ns.
5. $P_{RF} = 1.00$ MHz.
6. 2:1 divider may be used.
7. $L_1 = L_2$ Matched for equal time delay.

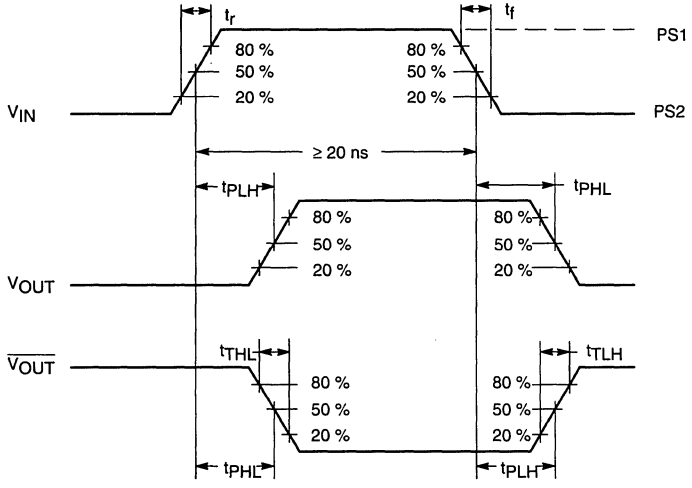


Figure 1. Switching Test Circuit and Waveforms

10H521
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10 H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.13	-1.480	+1.11	+0.31	-2.94	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-2.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	4 – 7 9 – 15	4 – 7 9 – 15			8		1, 16	2, 3
V_{OL}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	4 – 7 9 – 15	4 – 7 9 – 15			8		1, 16	2, 3
V_{OH1}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	4, 7 11, 13	4, 7 11, 13	4 – 7 9 – 15	4 – 7 9 – 15	8	8	1, 16	2, 3
V_{OL1}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	4, 7 11, 13		4 – 7 9 – 15	4 – 7 9 – 15	8	8	1, 16	2, 3
I_{EE}	Power Supply Current	–26		–29		–29		mA					8		1, 16	8
I_{IH}	Input Current High		295		500		500	µA	4 – 7, 9 11 – 15				8		1, 16	4 – 7, 9 11 – 15
I_{IH1}	Input Current High		360		610		610	µA	10				8		1, 16	10
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 – 7 9 – 15				8	1, 16	4 – 7, 9 – 15

10H521
QUIESCENT LIMIT TABLE*

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.13	-1.480	+1.11	+0.31	-2.94	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-2.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T
t_{TLH}	Rise Time	0.5	1.8	0.5	2.1	0.5	1.7	ns	5, 9, 10, 12, 15	2, 3	1, 16	8	5, 9, 10, 12, 15	2, 3
t_{THL}	Fall Time	0.5	1.8	0.5	2.1	0.5	1.7	ns	5, 9, 10, 12, 15	2, 3	1, 16	8	5, 9, 10, 12, 15	2, 3
t_{Pd}	Propagation Delay (Pin 10)	0.45	1.8	0.55	2.4	0.45	1.8	ns	5, 9, 10, 12, 15	2, 3	1. 16	8	5, 13	2, 3
t_{Pd}	Propagation Delay (Exclude Pin 10)	0.6	2.0	0.7	2.6	0.55	2.0	ns	5, 9, 10, 12, 15	2, 3	1. 16	8	5, 9, 12, 15	2, 3

Dual TTL-to-MECL Translator

Military 10H524

ELECTRICALLY TESTED PER:
5962-8756001

The 10H524 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems.

This 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8756001
3) 883: 10H524/BXAJC
X = CASE OUTLINE AS FOLLOWS:

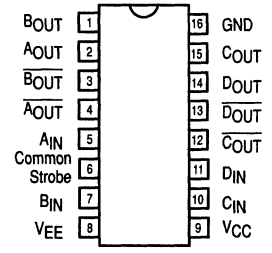
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

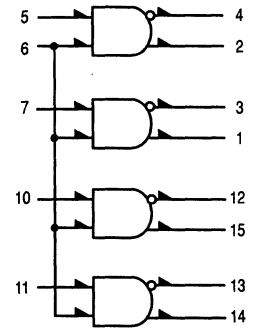
PIN ASSIGNMENTS

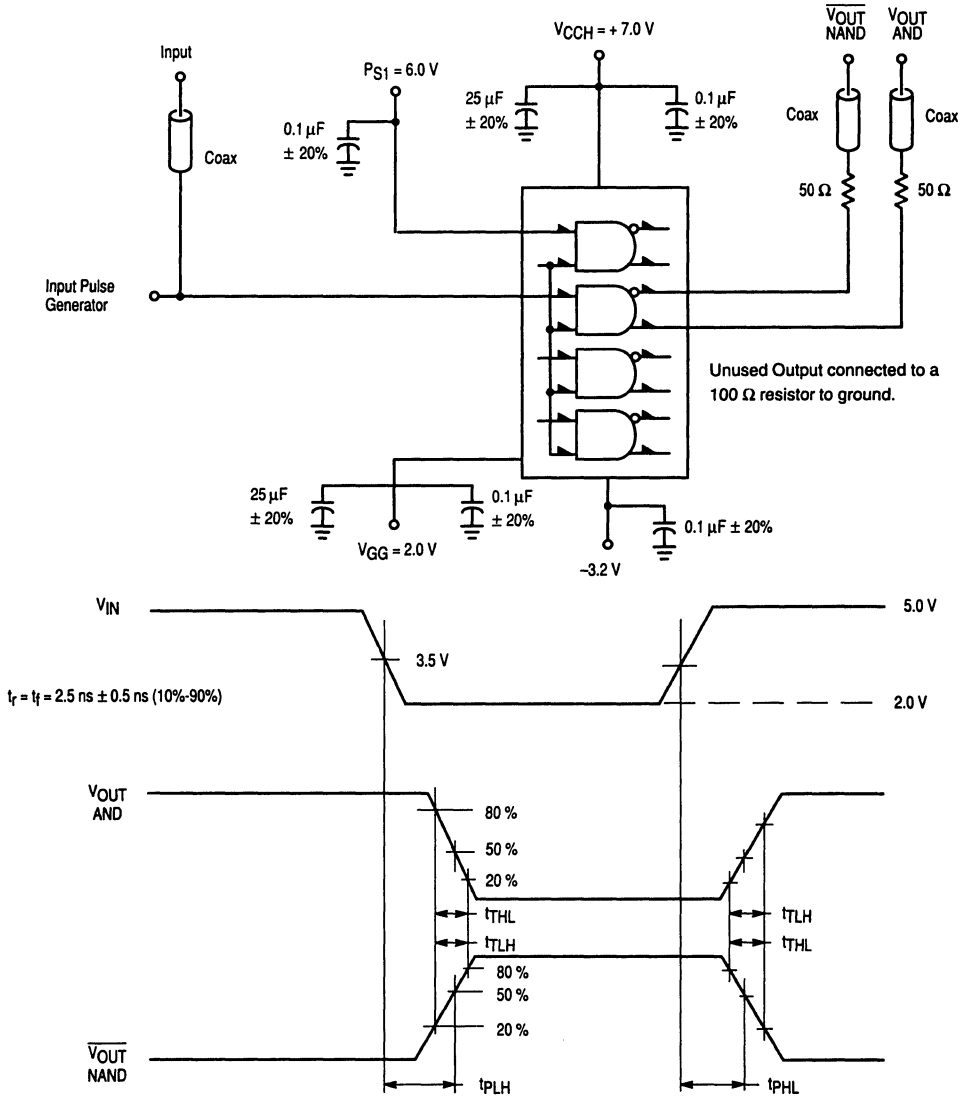
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
B_{OUT}	1	5	2	51 Ω to V_{TT}
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{B_{OUT}}$	3	7	4	51 Ω to V_{TT}
$\overline{A_{OUT}}$	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	V_{CC}
Common Strobe	6	10	8	V_{CC}
B_{IN}	7	11	9	V_{CC}
V_{EE}	8	12	10	V_{EE}
V_{CC}	9	13	12	V_{CC}
C_{IN}	10	14	13	V_{CC}
D_{IN}	11	15	14	V_{CC}
$\overline{C_{OUT}}$	12	16	15	51 Ω to V_{TT}
$\overline{D_{OUT}}$	13	1	17	51 Ω to V_{TT}
D_{OUT}	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
GND	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



POSITIVE LOGIC DIAGRAM





NOTES

1. 50 Ω termination to ground located in each scope channel input.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be < 164 inch from TP_{IN} to input pin and TP_{OUT} to output pin.

Figure 1. Switching Test Circuit and Waveforms

10H524
QUIESCENT LIMIT TABLE*

Test Temperature	Test Voltage Values (Volts)												
	V_{IH1}	V_{IL1}	V_{RH}	V_R	V_F	P_{S1}	V_{EEL}	V_{EE1}	V_{EE2}	B_{VIN}	V_{CC}	V_{CCH}	V_{GG}
T_A=25 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	–2.94	–5.46	–4.94	+5.5	+5.0	+7.0	+2.0
T_A=125 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	–2.94	–5.46	–4.94	+5.5	+5.0	+7.0	+2.0
T_A=55 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	–2.94	–5.46	–4.94	+5.5	+5.0	+7.0	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments I_{D1} = – 10 mA, I_{D2} = – 20 mA Output Load = 100 Ω to GND								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	GND	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V			5 – 7	10, 11	8		16	9	1 – 4 12 – 15
V_{OL}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V			5 – 7 10, 11	5, 7 10, 11	8		16	9	1 – 4 12 – 15
V_{OH1}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	5 – 7 10, 11	5 – 7 10, 11	5 – 7 10, 11		8	8	16	9	1 – 4 12 – 15
V_{OL1}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	5 – 7 10, 11	5 – 7 10, 11	5 – 7 10, 11	7	8	8	16	9	1 – 4 12 – 15
I_{EE}	Power Supply Current	–66		–72		–72		mA					8		16	9	8
I_{F1}	Forward Current		–3.2		–3.2		–3.2	mA			6	5, 7 10, 11		8	16	9	5, 7 10, 11
I_{F2}	Forward Current		–12.8		–12.8		–12.8	mA			5, 7 10, 11			8	16	9	6

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

10H524
QUIESCENT LIMIT TABLE*

Test Temperature	Test Voltage Values (Volts)												
	V_{IH1}	V_{IL1}	V_{RH}	V_R	V_F	P_{S1}	V_{EEL}	V_{EE1}	V_{EE2}	B_{VIN}	V_{CC}	V_{CCH}	V_{GG}
T_A=25 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	–2.94	–5.46	–4.94	+5.5	+5.0	+7.0	+2.0
T_A=125 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	–2.94	–5.46	–4.94	+5.5	+5.0	+7.0	+2.0
T_A=55 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	–2.94	–5.46	–4.94	+5.5	+5.0	+7.0	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments I_{D1} = – 10 mA, I_{D2} = – 20 mA Output Load = 100 Ω to –2.0 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_F	V_R	V_{RH}	B_{VIN}	I_{D1}	I_{D2}	V_{EE1}	GND	V_{CC}
V_{ID}	Input Clamp Voltage		–1.5		–1.5		–1.5	V					5, 7 10, 11	6	8	16	5, 7 10, 11
I_{CCL}	Positive Power Supply Current Drain		25		25		25	mA	10					8		16	9
I_{CCH}	Positive Power Supply Current Drain		16		18		16	mA			5 - 7 10, 11				8	16	9
I_{IN}	Input Current		1.0		1.0		1.0	mA	6			5 - 7 10, 11			8	16	5, 7 10, 11
I_{R1}	Reverse Current		50		50		50	µA	6	5, 7 10, 11					8	16	5, 7 10, 11
I_{R2}	Reverse Current		200		200		200	µA	5, 7 10, 11	6					8	16	6

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

10H524
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)												
	V_{IH1}	V_{IL1}	V_{RH}	V_R	V_F	P_{S1}	V_{EEL}	V_{EE1}	V_{EE2}	B_{VIN}	V_{CC}	V_{CCH}	V_{GG}
T_A=25 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	–2.94	–5.46	–4.94	+5.5	+5.0	+7.0	+2.0
T_A=125 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	–2.94	–5.46	–4.94	+5.5	+5.0	+7.0	+2.0
T_A=55 °C	+2.0	+0.8	+4.0	+2.4	+0.4	+6.0	–2.94	–5.46	–4.94	+5.5	+5.0	+7.0	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments I_{D1} = – 10 mA, I_{D2} = – 20 mA Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CCH}	V_{EEL}	V_{GG}	P_{S1}	P.U.T
t_r	Rise Time	0.45	2.0	0.5	2.5	0.4	1.8	ns	5	4	9	8	16	6	1 – 3, 12 – 15
t_f	Fall Time	0.45	2.0	0.5	2.5	0.4	1.8	ns	5	4	9	8	16	6	1 – 3, 12 – 15
t_{PHL}	Propagation Delay Pin 6	0.55	2.5	0.85	3.6	0.5	2.0	ns	10	12	9	8	16	6	1 – 4, 13 – 15
t_{PLH}	Propagation Delay Pin 6	0.55	2.5	0.85	3.6	0.5	2.0	ns	10	12	9	8	16	6	1 – 4, 13 – 15
t_{PHL}	Propagation Delay Pins 5, 7, 10, 11	0.55	2.4	0.85	3.5	0.55	2.1	ns	10	12	9	8	16	6	1 – 4, 13 – 15
t_{PLH}	Propagation Delay Pins 5, 7, 10, 11	0.55	2.4	0.85	3.5	0.55	2.1	ns	10	12	9	8	16	6	1 – 4, 13 – 15

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Dual MECL-to-TTL Translator

Military 10H525

ELECTRICALLY TESTED PER:
5962-8750801

The 10H525 is a quad translator for interfacing data and control signals between the MECL section and saturated logic section of digital systems.

This 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 2.5 ns Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8750801
3) 883: 10H525/BXAJC
X = CASE OUTLINE AS FOLLOWS:

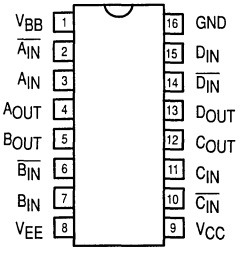
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

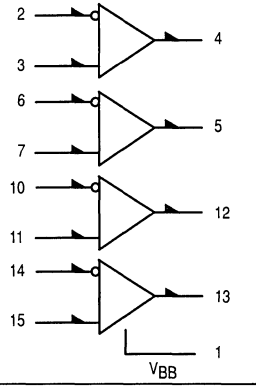
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{BB}	1	5	2	V_{BB}
$\overline{A_{IN}}$	2	6	3	2 K Ω to V_{EE}
A_{IN}	3	7	4	V_{BB}
A_{OUT}	4	8	5	360 Ω to V_{CC}
B_{OUT}	5	9	7	2 K Ω to V_{EE}
$\overline{B_{IN}}$	6	10	8	V_{BB}
B_{IN}	7	11	9	V_{CC}
V_{EE}	8	12	10	V_{EE}
V_{CC}	9	13	12	V_{CC}
$\overline{C_{IN}}$	10	14	13	V_{BB}
C_{IN}	11	15	14	2 K Ω to V_{EE}
C_{OUT}	12	16	15	360 Ω to V_{CC}
D_{OUT}	13	1	17	360 Ω to V_{CC}
$\overline{D_{IN}}$	14	2	18	V_{BB}
D_{IN}	15	3	19	2 K Ω to GND
GND	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



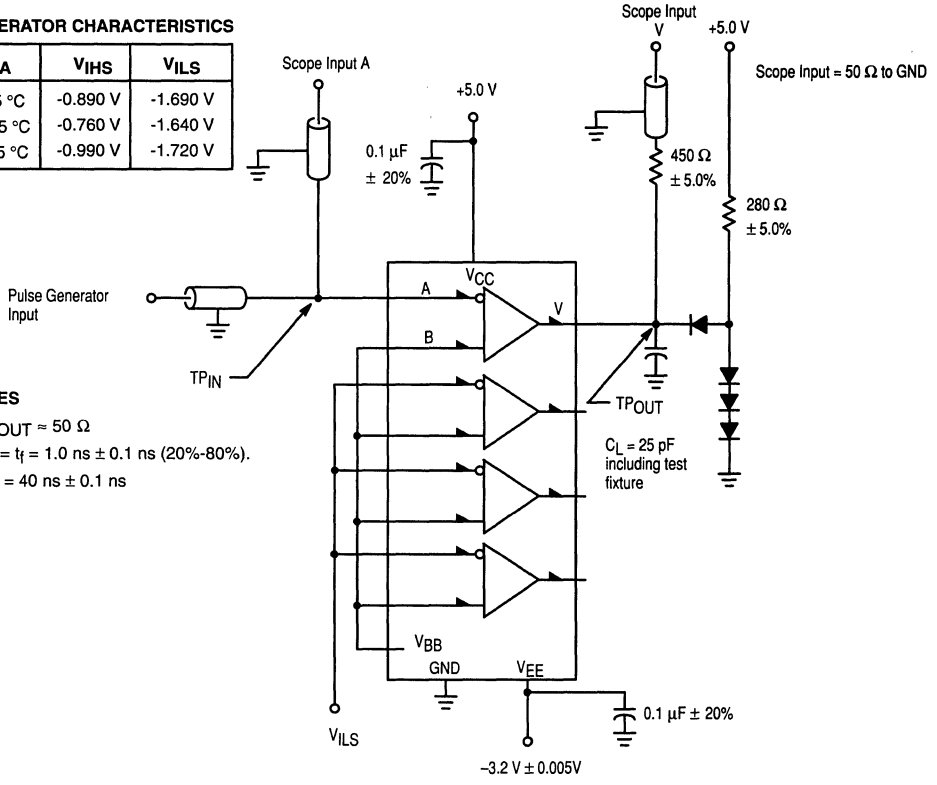
LOGIC DIAGRAM



2

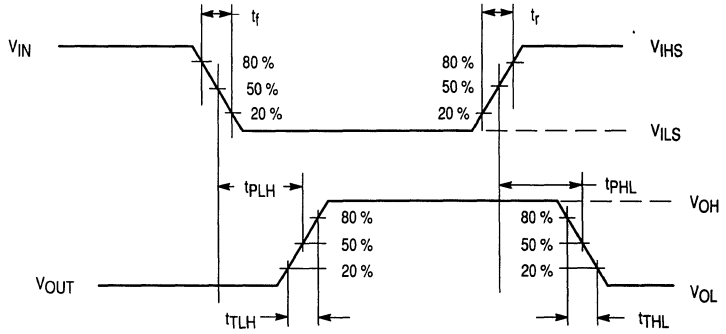
GENERATOR CHARACTERISTICS

T_A	V_{IHS}	V_{ILS}
25 °C	-0.890 V	-1.690 V
125 °C	-0.760 V	-1.640 V
-55 °C	-0.990 V	-1.720 V



NOTES

1. $Z_{OUT} \approx 50\ \Omega$
2. $t_r = t_f = 1.0$ ns ± 0.1 ns (20%-80%).
3. $t_p = 40$ ns ± 0.1 ns



NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cable. Wire length should be < 0.250 inch (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.Ω
3. All diodes are 1N3064 or equivalent.Ω

Figure 1. Switching Test Circuit and Waveforms

10H525
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)																Test Current (milliAmps)	
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE}	V_{EE1}	V_{EE2}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{CC}	V_{BB}	V_{IHS}	V_{ILS}	I_{OH}	I_{OL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.48	-0.89	-1.69	-5.2	-5.46	-4.94	+0.22	-0.95	-1.78	-2.95	+5.0	Pin 1	-0.89	-1.69	-2.0	+20
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	-0.76	-1.64	-5.2	-5.46	-4.94	+0.35	-0.95	-1.65	-2.95	+5.0	Pin 1	-0.76	-1.64	-2.0	+20
T_A = -55 °C	-0.84	-1.95	-1.16	-1.51	-0.99	-1.72	-5.2	-5.46	-4.94	+0.16	-0.95	-1.84	-2.95	+5.0	Pin 1	-0.99	-1.72	-2.0	+20

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
	Functional Parameters:	+ 25 °C Subgroup 1		+ 125 °C Subgroup 2		- 55 °C Subgroup 3			Pinouts referenced are for DIL package, check Pin Assignments GND = (Pin 16), Output Load = 100 Ω to GND									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IHH}	V_{IHL}	V_{IL}	V_{OL}	V_{ILL}	V_{ILH}	$V_{EE1/2}$	V_{OH}	P. U. T.
V_{OH}	High Output Voltage	2.5		2.5		2.5		V	3, 7 11, 15	3, 7 11, 15	3, 7 11, 15	2, 3, 6 7, 10, 11 14, 15		2, 6, 10, 11, 14	2, 6, 10, 14	8	4, 5 12, 13	4, 5 12, 13
V_{OL}	Low Output Voltage		0.5		0.5		0.5	V	2, 3, 6 7, 11 15	2, 6 10, 14	2, 3, 6 10, 14	3, 7 11, 15	4, 5 12, 13	3, 7 11, 15	3, 7 11, 15	8		4, 5 12, 13
V_{OLS}	Output Voltage		0.5		0.5		0.5	V					4, 5 12, 13			2, 3, 6 7, 8, 10, 11, 14, 15	4	4, 5 12, 13

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

10H525
QUIESCENT LIMIT TABLE*

Test Temperature	Test Voltage Values (Volts)																Test Current (milliAmps)
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE}	V_{EE1}	V_{EE2}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{CC}	V_{BB}	V_{IHS}	V_{ILS}	I_{OH}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.48	-0.89	-1.69	-5.2	-5.46	-4.94	+0.22	-0.95	-1.78	-2.95	+5.0	Pin 1	-0.89	-1.69	-2.0
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	-0.76	-1.64	-5.2	-5.46	-4.94	+0.35	-0.95	-1.65	-2.95	+5.0	Pin 1	-0.76	-1.64	-2.0
T_A = -55 °C	-0.84	-1.95	-1.16	-1.51	-0.99	-1.72	-5.2	-5.46	-4.94	+0.16	-0.95	-1.84	-2.95	+5.0	Pin 1	-0.99	-1.72	-2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
	Functional Parameters:	+ 25 °C Subgroup 1		+ 125 °C Subgroup 2		- 55 °C Subgroup 3			Pinouts referenced are for DIL package, check Pin Assignments GND = (Pin 16), Output Load = 100 Ω to GND									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IHA}	V_{IL}	V_{ILA}	V_{BB}	V_{EE}	$V_{EE1/2}$	I_{OH}	I_{OL}	P. U. T.
V_{OH1}	High Output Voltage	2.5		2.5		2.5		V			2, 6 10, 14	2, 6 10, 14	1, 3, 7 11, 15		8	4, 5 12, 13		4, 5 12, 13
V_{OL1}	Low Output Voltage		0.5		0.5		0.5	V		2, 6 10, 14	2, 6 10, 14		1, 3, 7 11, 15		8		4, 5 12, 13	4, 5 12, 13
V_{BB}	Reference Voltage	-1.37	-1.25	-1.31	-1.19	-1.41	-1.27	V					1, 3, 7 11, 15	8				1
I_{EE}	Power Supply Current	-40		-44		-44		mA					1, 3, 7 11, 15	2, 6 10, 14	8			8
I_{CCL}	Positive Power		40		40		40	mA					1, 3, 7 11, 15	2, 6 10, 14	8			9
I_{CCH}	Supply Drain Current		63		63		63	mA	2, 6 10, 14				1, 3, 7 11, 15		8			9
I_{CBO}	Input Leakage Current	-1.0		-1.0		-1.5		µA					1, 2, 3 6, 7, 10, 11, 14, 15		2, 3, 6 7, 8 10, 11 15			2, 3, 6, 7, 10, 11, 14, 15
I_{OS}	Short Circuit Current	-150	-60	-150	-60	-150	-60	mA			2, 6 10, 14		1, 3, 7 11, 15		8			4, 5, 12, 13
I_{INH}	Input Current		145		225		225	µA	2, 3, 6 7, 10 11, 14 15				1, 2, 3 6, 7, 10, 11, 14, 15		8			2, 3, 6, 7, 10, 11, 14, 15

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

10H525
QUIESCENT LIMIT TABLE*

Test Temperature	Test Voltage Values (Volts)																Test Current (milliAmps)
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE}	V_{EE1}	V_{EE2}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{CC}	V_{BB}	V_{IHS}	V_{ILS}	I_{OH}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.48	-0.89	-1.69	-5.2	-5.46	-4.94	+0.22	-0.95	-1.78	-2.95	+5.0	Pin 1	-0.89	-1.69	-2.0
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	-0.76	-1.64	-5.2	-5.46	-4.94	+0.35	-0.95	-1.65	-2.95	+5.0	Pin 1	-0.76	-1.64	-2.0
T_A = -55 °C	-0.84	-1.95	-1.16	-1.51	-0.99	-1.72	-5.2	-5.46	-4.94	+0.16	-0.95	-1.84	-2.95	+5.0	Pin 1	-0.99	-1.72	-2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments GND = (Pin 16), Output Load = (See Figure 1).						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{out}	V_{BB}	V_{EE2}	V_{ILS}	P_{S2}	P.U.T.
t_{TLH}	Rise Time	0.3	1.3	0.3	2.0	0.3	1.4	ns	2, 6, 10, 14	4, 5, 12, 13	1, 3, 7 11, 15	8	2, 6, 10, 14	10	4, 5, 12, 13
t_{THL}	Fall Time	0.3	1.3	0.3	2.0	0.3	1.4	ns	2, 6, 10, 14	4, 5, 12, 13	1, 3, 7 11, 15	8	2, 6, 10, 14	10	4, 5, 12, 13
$t_{PHL/PLH}$	Propagation Delay	0.85	3.2	0.9	3.5	0.8	2.9	ns	2, 6, 10, 14	4, 5, 12, 13	1, 3, 7 11, 15	8	2, 6, 10, 14	10	4, 5, 12, 13

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

MOTOROLA

Dual D Type Master-Slave Flip-Flop

Military 10H531

ELECTRICALLY TESTED PER:
5962-8756101

The 10H531 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

2

- Propagation Delay, 1.0 ns Typical
- 340 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8756101
3) 883: 10H531/BXAJC
X = CASE OUTLINE AS FOLLOWS:

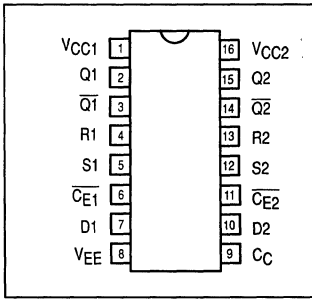
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

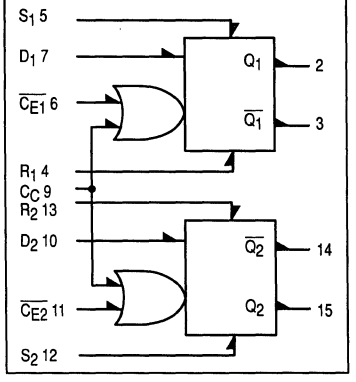
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω to V_{TT}
$\overline{Q_1}$	3	7	4	51 Ω to V_{TT}
R_1	4	8	5	51 Ω to V_{TT}
S_1	5	9	7	GND
$\overline{C_{E1}}$	6	10	8	OPEN
D_1	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
C_C	9	13	12	OPEN
D_2	10	14	13	OPEN
$\overline{C_{E2}}$	11	15	14	OPEN
S_2	12	16	15	GND
R_2	13	1	17	51 Ω to V_{TT}
$\overline{Q_2}$	14	2	18	51 Ω to V_{TT}
Q_2	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM

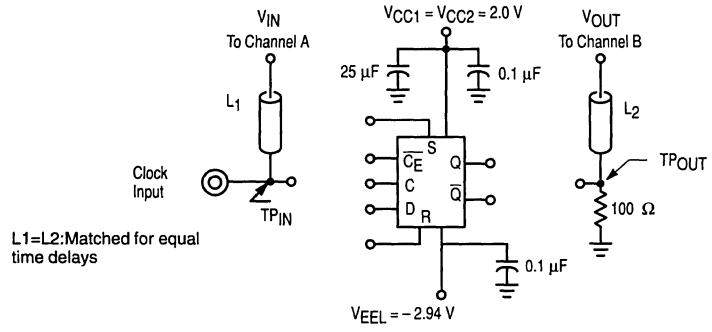


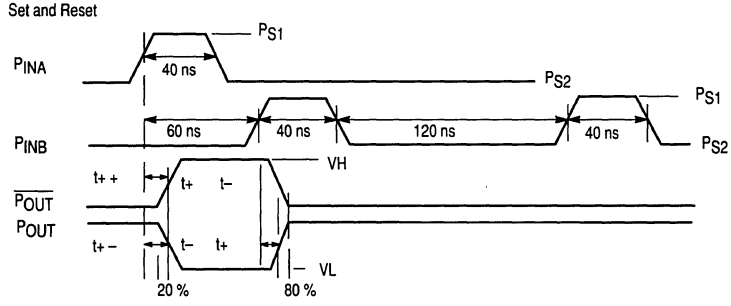
R-S Truth Table		
R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined
A clock H is a clock transition from a Low to High state

Clock Truth Table		
C	D	Q_{n+1}
L	Ø	Q_n
H	L	L
H	H	H

Ø = Don't Care
$C = \overline{CE} + CC$





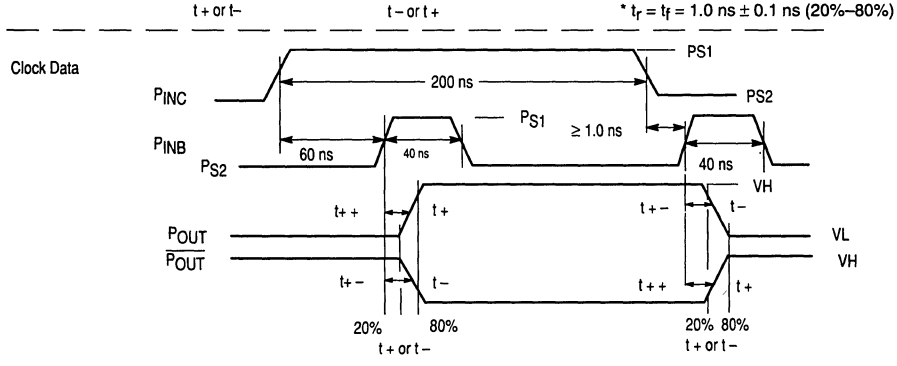


Figure 1. Switching Test Circuit and Waveforms

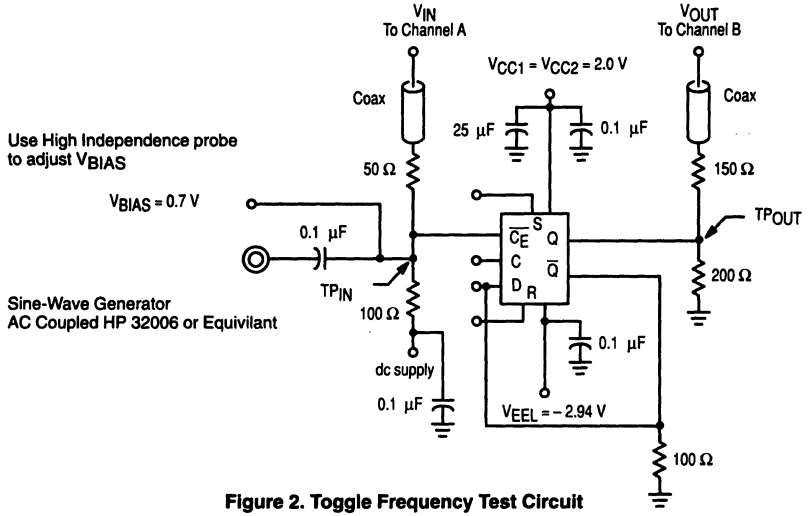
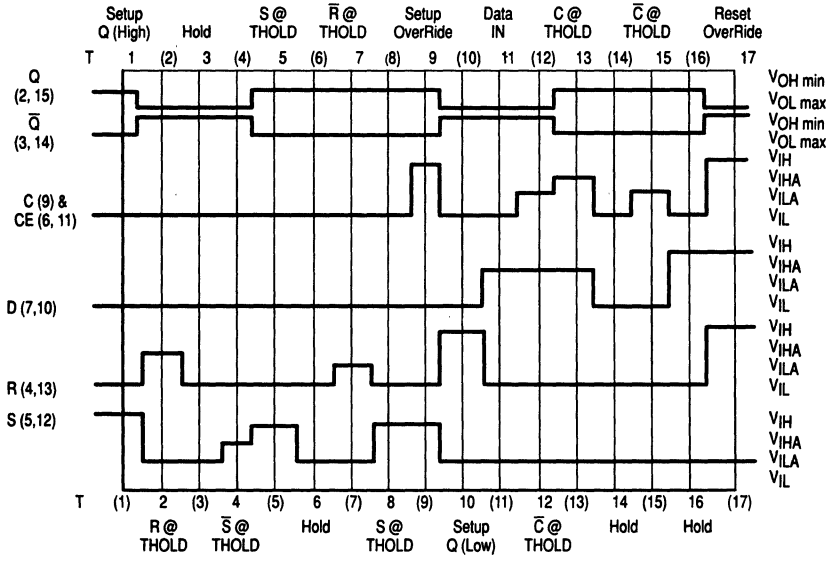
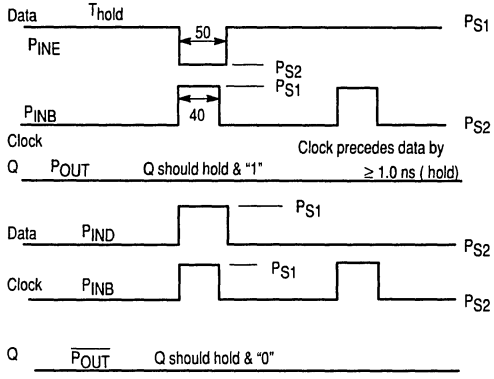


Figure 2. Toggle Frequency Test Circuit



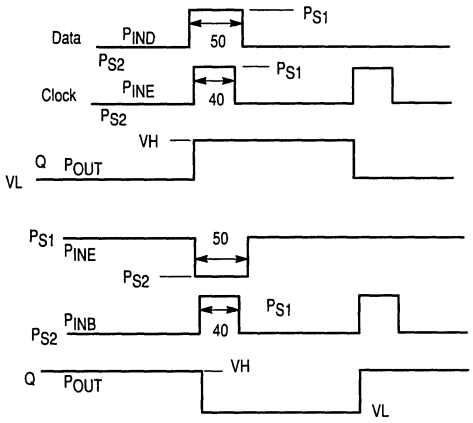
Note: Do not remove power during sequence of tests.

Figure 3. Timing Diagram



NOTES

1. t_{hold} is min. time after positive transition of the clock pulse that information must remain unchanged at the data input.
2. For all t_{hold} tests, pulse width should not be less than 20 ns.



NOTES

1. t_{setup} is the min. time before the positive transition of the clock information must be present at the data input.
2. For all setup tests, pulse widths should not be less than 20 ns.

Data precedes clock by ≤ 1.5 ns (setup)

Figure 4. T_{HOLD} Waveforms

10H531
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to –2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.780	-1.950	-1.110	-1.480	+1.11	+0.31	-2.94	-5.46	-4.94
T_A = 125 °C	-0.650	-1.950	-0.960	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
T_A = -55 °C	-0.840	-1.950	-1.160	-1.510	+1.01	+0.28	-2.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	4, 5 12, 13	4 – 7 9 – 13	8		1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	5, 12	4 – 7 9 – 13	8		1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V			8	8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V			8	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	–56		–62		–62		mA		6, 11	8		1, 16	8
I_{IH}	Input Current High		390		660		660	µA	9		8		1, 16	9
I_{IH1}	Input Current High		310		530		530	µA	6, 11		8		1, 16	6, 11
I_{IH2}	Input Current High		465		790		790	µA	4, 5 12, 13		8		1, 16	4, 5, 12, 13
I_{IH3}	Input Current High		285		485		486	µA	7, 10		8		1, 16	7, 10
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 – 7 9 – 13		8	1, 16	4 – 7, 9 – 13

10H531
QUIESCENT LIMIT TABLE*

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to –2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.780	-1.950	-1.110	-1.480	+1.11	+0.31	-2.94	-5.46	-4.94
T_A = 125 °C	-0.650	-1.950	-0.960	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
T_A = -55 °C	-0.840	-1.950	-1.160	-1.510	+1.01	+0.28	-2.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T
t_r	Rise Time	0.5	2.0	0.6	2.2	0.45	1.8	ns	4, 5	3	1, 16	8	2, 14, 15
t_f	Fall Time	0.5	2.0	0.6	2.2	0.45	1.8	ns	4, 5	3	1, 16	8	2, 14, 15
t_{pd}	Propagation Delay CLK, CE, Set, Reset	0.7	2.15	0.7	2.2	0.6	2.1	ns	10, 11	15	1. 16	8	2, 3, 14
t_{SET}	Set Up Time	0.7		0.7		0.7		ns	6, 7, 10, 11	2, 15	1. 16	8	2, 3, 14, 15
t_{HOLD}	Hold Time	0.8		0.8		0.8		ns	6, 7, 10, 11	2, 15	1, 16	8	2, 3, 14, 15
f_{tog}	Toggle Frequency	250		250		250		MHz					(See Fig. 2)

Dual J-K Master-Slave Flip-Flop

ELECTRICALLY TESTED PER:
5962-8750501

The 10H535 is a dual master-slave dc coupled J-K flip-flop. The device is provided with asynchronous set(s) and Reset (R). These set and reset inputs override the clock.

A common clock is provided with separate $\overline{J}$-$\overline{K}$ inputs. When the clock is static, the $\overline{J}$-$\overline{K}$ inputs do not effect the output.

The output states of the flip-flop change on the positive transition of the clock.

- Propagation Delay, 1.5 ns Typical
- 410 mW Max/Pkg (No Load)
- f_{Tog} = 250 MHz Max
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8750501
3) 883: 10H535/BXAJC
X = CASE OUTLINE AS FOLLOWS:

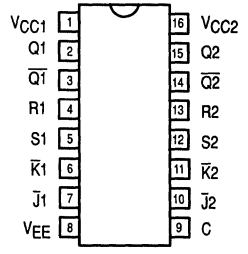
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

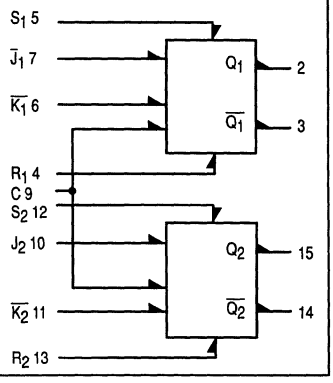
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω to V_{TT}
$\overline{Q_1}$	3	7	4	51 Ω to V_{TT}
R_1	4	8	5	51 Ω to V_{TT}
S_1	5	9	7	GND
$\overline{K_1}$	6	10	8	OPEN
$\overline{J_1}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
C	9	13	12	OPEN
$\overline{J_2}$	10	14	13	OPEN
$\overline{K_2}$	11	15	14	OPEN
S_2	12	16	15	GND
R_2	13	1	17	51 Ω to V_{TT}
$\overline{Q_2}$	14	2	18	51 Ω to V_{TT}
Q_2	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



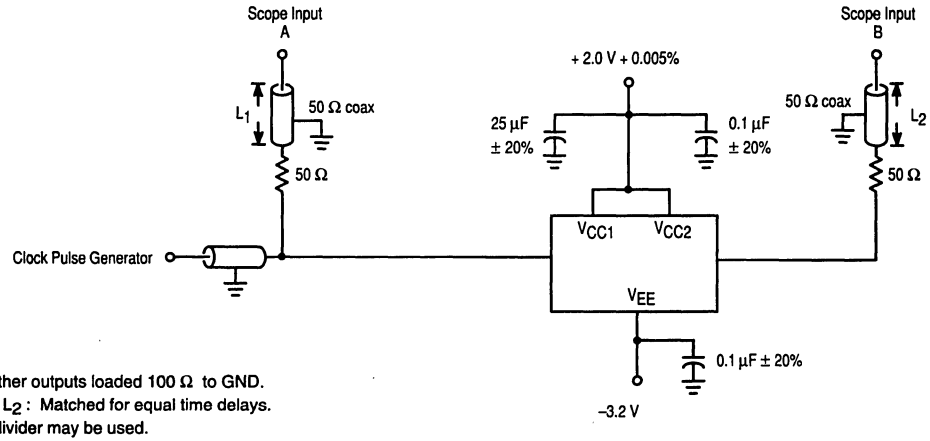
LOGIC DIAGRAM



R-S Truth Table		
R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

Clock Truth Table		
$\overline{J}$	$\overline{K}$	Q_{n+1}
L	L	$\overline{Q}_n$
H	L	L
L	H	H
H	H	Q_n

N.D. = Not Defined
A clock H is a clock transition from a Low to High state



NOTES

1. All other outputs loaded 100 Ω to GND.
2. $L_1 = L_2$: Matched for equal time delays.
3. 2:1 divider may be used.
4. $V_{IN} \geq 20$ ns.
5. $f_{IN} = 1.0$ MHz.
6. $t_r = t_f = 1.0$ ns ± 0.1 ns.

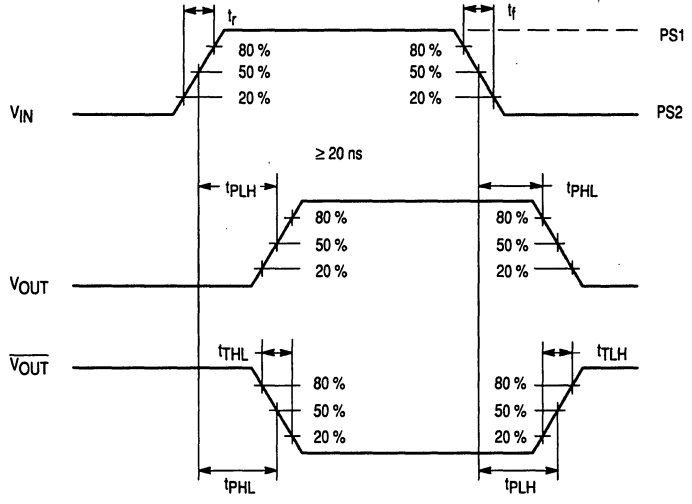
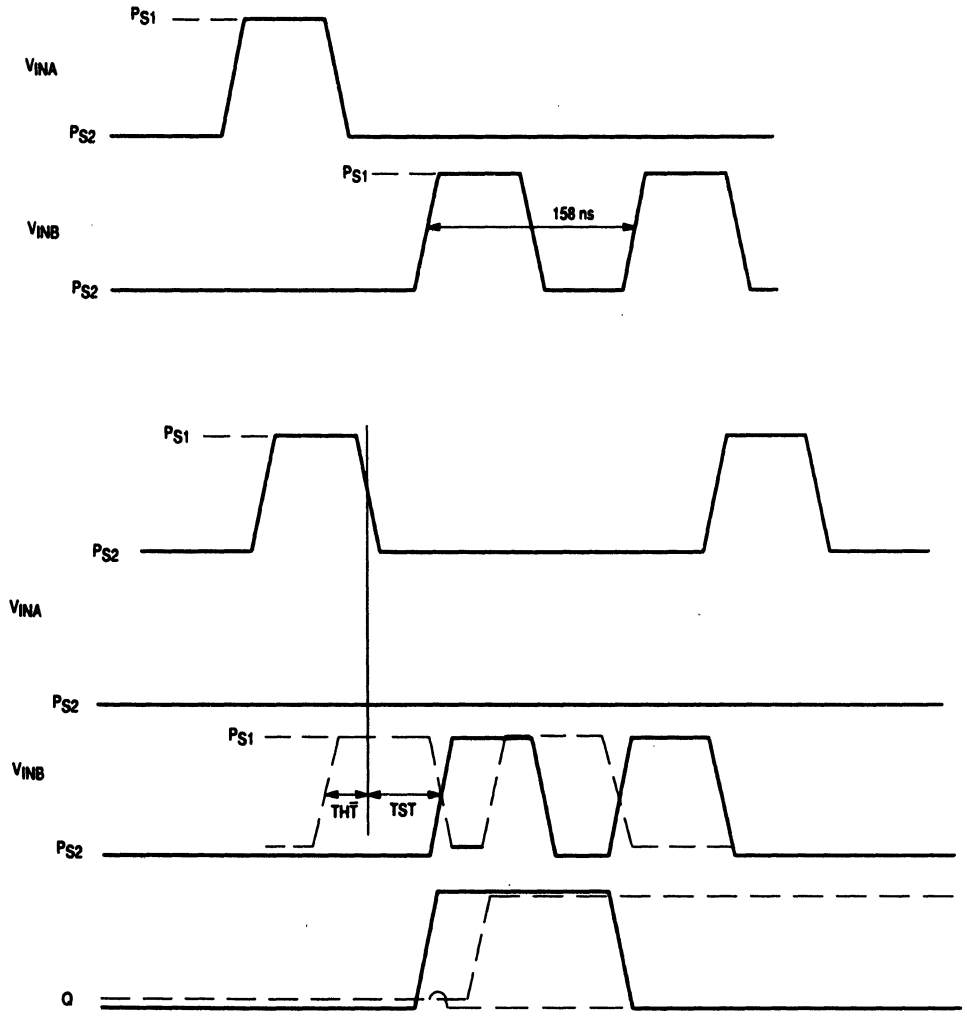


Figure 1. Switching Test Circuit and Waveforms



NOTES
1. TST = Minimum set up time for Toggle.
2. THT = Minimum hold time for Not Toggle.

Figure 2. Set, Reset and Toggle Waveforms

10H535
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to –2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EE2}
T_A = 25 °C	-0.780	-1.950	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.650	-1.950	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = - 55 °C	-0.840	-1.950	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE2}	V_{EE1}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	4, 5, 12, 13					8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	4, 5, 12, 13					8	1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	4, 5, 12, 13	4 – 7 9 – 13	4, 5, 12, 13	4 – 7 9 – 13	8	8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	4, 5, 12, 13	4 – 7 9 – 13	4, 5 12, 13	4 – 7 9 – 13	8	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	–68		–75		–75		mA						8	1, 16	8
I_{IH}	Input Current High		285		460		460	µA	6, 7, 10, 11					8	1, 16	6, 7, 10, 11
I_{IH1}	Input Current High		420		675		675	µA	9					8	1, 16	9
I_{IH2}	Input Current High		500		800		800	µA	4, 5, 12, 13					8	1, 16	4, 5, 12, 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 – 7 9 – 13			8		1, 16	4 – 7, 9 – 13

10H535
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to –2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EE2}
T_A = 25 °C	-0.780	-1.950	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.650	-1.950	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.840	-1.950	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		P_{S2}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH1} t_{TLH1}	Rise Time 1 or Fall Time 1	0.5	2.0	0.7	2.4	0.5	2.0	ns	6, 7, 10, 11	4, 5, 9, 14	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{TLH2} t_{TLH2}	Rise Time 2 or Fall Time 2	0.5	2.0	0.7	2.4	0.5	2.0	ns	6, 7, 10, 11	4, 5, 9, 14	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH1} t_{PLH1}	Propagation Delay 1 Set, Reset	0.7	2.3	0.7	2.6	0.5	2.3	ns	6, 7, 10, 11	4, 5, 9, 14	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH2} t_{PLH2}	Propagation Delay 2 Clock	0.7	2.3	0.7	2.6	0.5	2.3	ns	6, 7, 10, 11	4, 5, 9, 14	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{SETUP}	Setup Time	1.5		1.5		1.5		ns	6, 7, 10, 11	6, 7, 10, 11	3, 14	1, 16	8	3, 14
t_{HOLD}	Hold Time	1.0		1.0		1.0		ns	6, 7, 10, 11	6, 7, 10, 11	3, 14	1, 16	8	3, 14
f_{tog}	Toggle Frequency	250		250		250		MHz	6, 7, 10, 11	6, 7, 10 -11	3, 14	1, 16	8	3, 14

MOTOROLA

Universal Hexadecimal Counter

Military 10H536

ELECTRICALLY TESTED PER:
5962-870010101

The 10H536 is a high speed synchronous hexadecimal counter. This MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

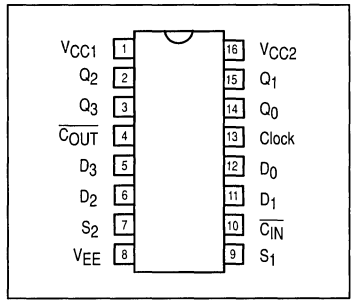
- Counting Frequency, 250 MHz Minimum
- 900 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8700101
3) 883: 10H536/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_2	2	6	3	51 Ω TO V_{TT}
Q_3	3	7	4	51 Ω TO V_{TT}
$\overline{C_{OUT}}$	4	8	5	51 Ω TO V_{TT}
D_3	5	9	7	GND
D_2	6	10	8	GND
S2	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
S1	9	13	12	OPEN
$\overline{C_{IN}}$	10	14	13	OPEN
D_1	11	15	14	GND
D_0	12	16	15	GND
CLK	13	1	17	CP1
Q_0	14	2	18	51 Ω TO V_{TT}
Q_1	15	3	19	51 Ω TO V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

FUNCTION SELECT TABLE

$\overline{C_{IN}}$	S_1	S_2	OPERATING MODE
Ø	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
Ø	H	H	Hold (Stop Count)

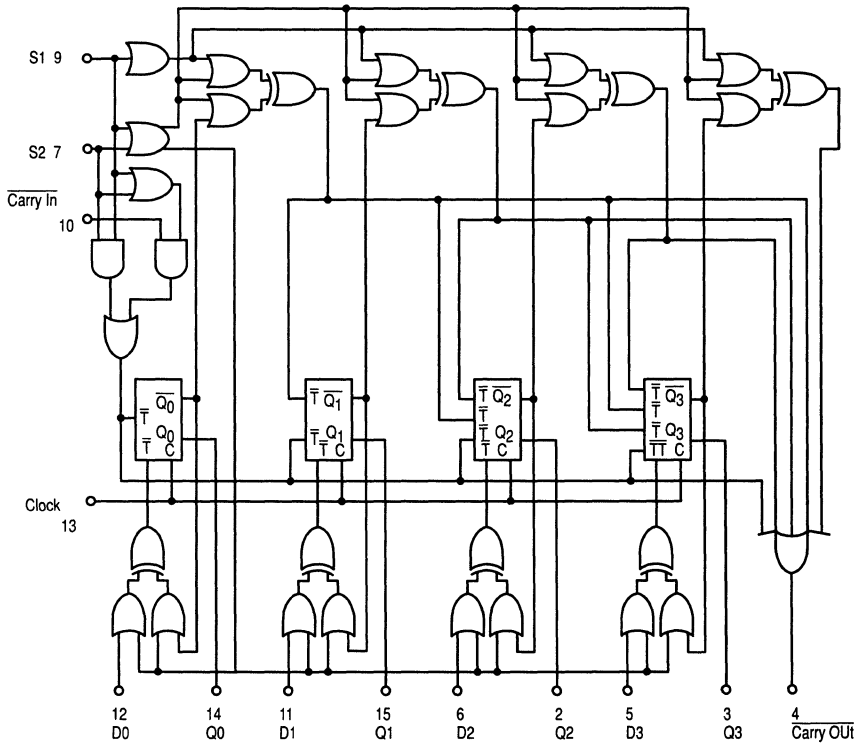
Ø = Don't Care

SEQUENTIAL TRUTH TABLE •												
S_1	S_2	D_0	D_1	D_2	D_3	$\overline{\text{Carry IN}}$	Clock ••	Q_0	Q_1	Q_2	Q_3	$\overline{\text{Carry OUT}}$
L	L	L	L	H	H	Ø	H	L	L	H	H	L
L	H	Ø	Ø	Ø	Ø	L	H	H	L	H	H	H
L	H	Ø	Ø	Ø	Ø	L	H	L	H	H	H	H
L	H	Ø	Ø	Ø	Ø	L	H	H	H	H	H	L
L	H	Ø	Ø	Ø	Ø	H	L	H	H	H	H	H
L	H	Ø	Ø	Ø	Ø	H	H	H	H	H	H	H
H	H	Ø	Ø	Ø	Ø	Ø	H	H	H	H	H	H
L	L	H	H	L	L	Ø	H	H	H	L	L	L
H	L	Ø	Ø	Ø	Ø	L	H	L	H	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	H	L	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	L	L	L	L	L
H	L	Ø	Ø	Ø	Ø	L	H	H	H	H	H	H

Ø = Don't Care

• Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

•• A clock H is defined as a clock input transition from a low to a high logic level.



NOTE
FLIP FLOPS WILL TOGGLE WHEN ALL $\overline{T}$ INPUTS ARE LOW.

Figure 1. Logic Diagram

10H536
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to –2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.780	-1.950	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.650	-1.950	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = - 55 °C	-0.840	-1.950	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{EE2}	V_{EE1}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	–1.046	–0.819	–0.899	–0.692	–1.099	–0.882	V	3 - 6, 11 - 14	13		8	1, 16	2, 3, 4, 14, 15
V_{OL}	Low Output Voltage	–1.95	–1.592	–1.95	–1.578	–1.95	–1.623	V	13	13		8	1, 16	2, 3, 4, 14, 15
V_{OH1}	High Output Voltage	–1.046	–0.819	–0.899	–0.692	–1.099	–0.882	V			8	8	1, 16	2, 3, 4, 14, 15
V_{OL1}	Low Output Voltage	–1.95	–1.592	–1.95	–1.578	–1.95	–1.623	V			8	8	1, 16	2, 3, 4, 14, 15
I_{EE}	Power Supply Current	–149		–164		–164		mA				8	1, 16	8
I_{IH}	Input Current High		225		365		365	µA	9			8	1, 16	9
I_{IH1}	Input Current High		260		415		415	µA	10			8	1, 16	10
I_{IH2}	Input Current High		320		520		520	µA	5, 6, 11 - 13			8	1, 16	5, 6, 11 - 13
I_{IH3}	Input Current High		405		655		655	µA	7			8	1, 16	7
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 10 - 13	8		1, 16	5, 6, 11 - 13

10H536
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to –2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EE2}
T_A = 25 °C	-0.780	-1.950	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.650	-1.950	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.840	-1.950	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	P_{S1}	P_{S2}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.7	2.1	0.7	2.3	0.7	2.3	ns	7, 13	4	11, 12	9, 10	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	0.7	2.1	0.7	2.3	0.7	2.3	ns	7, 13	4	11, 12	9, 10	1, 16	8	2, 3, 14, 15
t_{pd}	Propagation Delay														
	Clk to Q	0.7	3.2	0.7	3.5	0.7	3.5	ns	10	4	11, 12	9, 13	1, 16	8	2, 3, 14, 15
	Clk to $\overline{\text{Carry Out}}$	0.7	7.0	0.7	7.7	0.7	7.7	ns	10	4	11, 12	9, 13	1, 16	8	2, 3, 14, 15
	$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$	0.7	3.0	0.7	3.5	0.7	3.5	ns	10	4	11, 12	9, 13	1, 16	8	2, 3, 14, 15
t_{SET}	Setup Time														
	Data (D_0 to C)	2.0		2.0		2.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	Select (S to C)	3.5		3.5		3.5		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	Carry In ($\overline{C_{IN}}$ to C)	2.0		2.0		2.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	(C to $\overline{C_{IN}}$)	0.0		0.0		0.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
t_{HOLD}	Hold Time														
	Data (D_0 to C)	0.0		0.0		0.0		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	Select (S to C)	-0.5		-0.5		-0.5		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	Carry In ($\overline{C_{IN}}$ to C)	150		150		150		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
	(C to $\overline{C_{IN}}$)	2.0		2.2		2.2		ns	12, 13	14		7, 9	1, 16	8	2, 3, 14, 15
f_{Count}	Count Frequency	250		250		250		MHz	12	13	9		1, 16	8	3, 14

Four Bit Universal Shift Register

Military 10H541

ELECTRICALLY TESTED PER:
5962-8751101

The 10H541 is a four-bit universal shift register. This device is a functional/pin-out duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Shift frequency, 250 MHz min
- 610 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

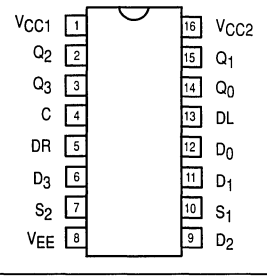
1) JAN: N/A
2) SMD: 5962-8751101
3) 883: 10H541/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_2	2	6	3	51 Ω to V_{TT}
Q_3	3	7	4	51 Ω to V_{TT}
C	4	8	5	CP1
DR	5	9	7	OPEN
D_3	6	10	8	GND
S_2	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
D_2	9	13	12	GND
S_1	10	14	13	OPEN
D_1	11	15	14	GND
D_0	12	16	15	GND
DL	13	1	17	OPEN
Q_0	14	2	18	51 Ω to V_{TT}
Q_1	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

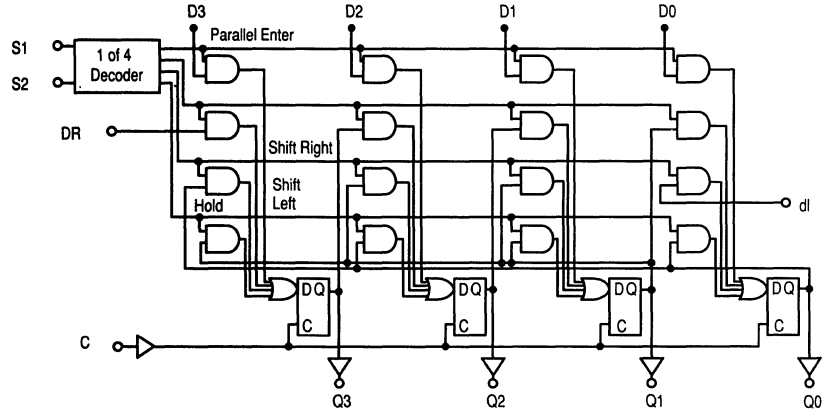
TRUTH TABLE

SELECT			OUTPUTS			
S_1	S_2	OPERATING MODE	Q_{0n+1}	Q_{1n+1}	Q_{2n+1}	Q_{3n+1}
L	L	Parallel Entry	D_0	D_1	D_2	D_3
L	H	Shift Right *	$Q1_n$	Q2n	Q3n	DR
H	L	Shift Left *	DL	Q0n	Q1n	Q2n
H	H	Stop Shift	$Q0_n$	Q1n	Q2n	Q3n

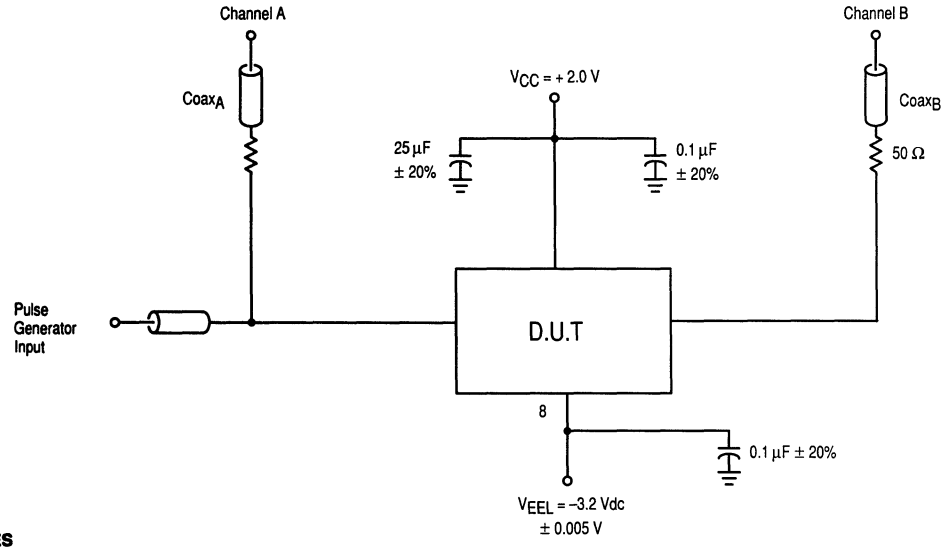
* Outputs as exist after pulse at "C" input conditions as shown,
(Pulse = Positive transition of the clock input.).

2

LOGIC DIAGRAM



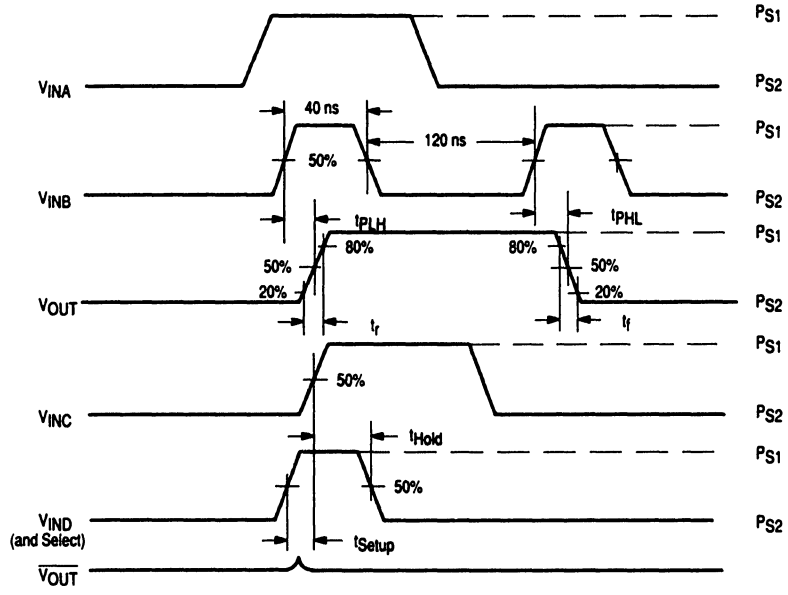
SWITCHING TEST CIRCUIT



NOTES

1. Unused outputs should be loaded 100 Ω to ground.
2. Length of Coax$_A$ and Coax$_B$ should be equal for equal time delay.
3. 2:1 divider maybe used.
4. $t_r = t_f = 1.0$ ns ± 0.1 ns (20% to 80%)

Figure 1. Switching Test Circuit and Waveforms



NOTES

1. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 2.0 MHz.
   c) t_r and t_f = 1.0 ns ± 0.1 ns (20% - 80%).

Figure 2. Switching Test Circuit Waveforms

10H541
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-2.94	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-2.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{EE2}	V_{EE1}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	4, 6, 9, 11, 12	4		8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	4	4, 6, 9, 11, 12		8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V			8	8	1, 16	2 - 4, 13 -15
V_{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V			8	8	1, 16	2 - 4, 13 -15
I_{IH1}	Input Current High		255		405		405	µA	5, 6, 9, 11 - 13			8	1, 16	5, 6, 9, 11 -13
I_{IH2}	Input Current High		260		415		415	µA	7, 10			8	1, 16	7, 10
I_{IH3}	Input Current High		320		510		510	µA	4			8	1, 16	4
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 13	8		1, 16	4 - 7, 9 - 14
I_{EE}	Power Supply	-102		-112		-112		mA			8		1, 16	8

10H541
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-2.94	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-2.94	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-2.94	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.7	2.0	0.7	2.2	0.7	1.7	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	0.7	2.0	0.7	2.2	0.7	1.7	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay	1.0	1.9	1.1	2.1	1.0	2.0	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL}	Propagation Delay	1.0	1.9	1.1	2.1	1.0	2.0	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{Setup}	Setup Time Data Inputs	1.5		1.5		1.5		ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{hold}	Hold Time Data Input	1.0		1.0		1.0		ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{Setup}	Setup Time Select Input	3.0		3.0		3.0		ns	4, 7, 10, 12	3, 14	1, 16	8	2, 3, 14, 15
t_{hold}	Hold Time Select Inputs	1.0		1.0		1.0		ns	4, 7, 10, 12	3, 14	1, 16	8	2, 3, 14, 15
f_{tog}	Toggle Frequency	250		250		250		MHz	4, 12	4	1, 16	8	14

Quad 2-Input Multiplexer (Non-Inverting)

Military 10H558

ELECTRICALLY TESTED PER:
5962-8756601

2

The 10H558 is a quad two channel multiplexer with common input select. A "high" level select enables input D00, D10, D20 and D30 and a "low" level select enables input D01, D11, D21 and D31.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.5 ns Typical
- 290 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

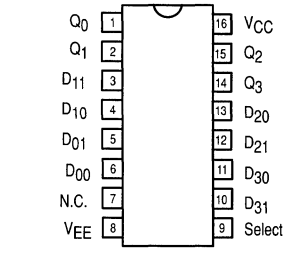
1) JAN: N/A
2) SMD: 5962-8756601
3) 883: 10H558/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

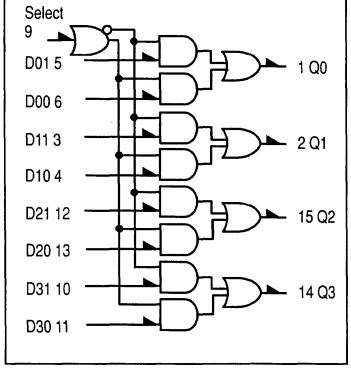
The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
Q0	1	5	2	51 Ω to V_{TT}
Q1	2	6	3	51 Ω to V_{TT}
D11	3	7	4	51 Ω to V_{TT}
D10	4	8	5	OPEN
D01	5	9	7	GND
D00	6	10	8	OPEN
NC	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
Select	9	13	12	OPEN
D31	10	14	13	GND
D30	11	15	14	OPEN
D21	12	16	15	GND
D20	13	1	17	OPEN
Q3	14	2	18	51 Ω to V_{TT}
Q2	15	3	19	51 Ω to V_{TT}
V_{CC}	16	4	20	GND



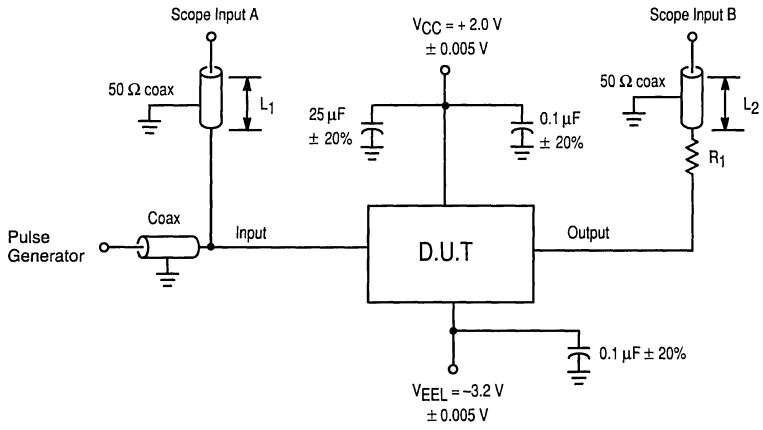
POSITIVE LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Truth Table			
Select	**D0**	**D1**	**Q**
L	Ø	L	L
L	Ø	H	H
H	L	Ø	L
H	H	Ø	H

Ø = Don't Care



NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Unused outputs connected to 100 Ω resistor to ground.
3. 2:1 divider may be used.
4. L1 = L2: Matched for equal time delay.
5. R_1 = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
6. $t_r = t_f$ = 1.0 ns ± 0.1 ns (20% - 80%).
7. $P_W \geq 20$ ns.
7. P_{RF} = 1.0 MHz.

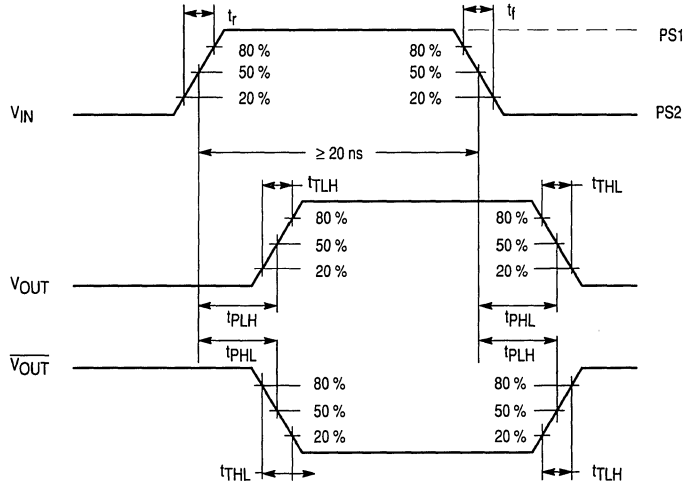


Figure 1. Switching Test Circuit and Waveforms

10H558
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25° C		+ 125° C		- 55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to GND							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3, 5, 10, 12				8		16	1, 2, 14, 15
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V					8		16	1, 2, 14, 15
V_{OH1}	High Output Voltage	-1.01	-1.78	-0.86	-0.65	-1.06	-0.84	V	3 - 6, 9 -13				8	8	16	1, 2, 13, 15
V_{OL1}	Low Output Voltage	-1.95	-0.58	-1.95	-1.565	-1.95	-1.61	V	3 - 6, 9 -13		3 - 6, 9 -13	9	8	8	16	1, 2, 14, 15
I_{EE}	Power Supply Current	-48		-53		-53		mA			9	3 - 6, 9 -13	8		16	8
I_{IH1}	Input Current High		295		475		475	µA	9				8		16	9
I_{IH2}	Input Current High		320		515		515	µA	3 - 6, 9 -13				8		16	3 - 6, 9 - 13
I_{IL}	Input Current	0.5		0.3		0.5		µA		3 - 6 9 - 13			8		16	3 - 6, 9 - 13

10H558
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.7	2.0	0.7	2.2	0.7	2.2	ns	3 - 6, 10 - 13	1, 2	16	8	1, 2, 14, 15
t_{THL}	Fall Time	0.7	2.0	0.7	2.2	0.7	2.2	ns	3 - 6, 10 - 13	1, 2	16	8	1, 2, 14, 15
t_{PLH}	Propagation Delay Data to Output	0.5	1.8	0.5	2.2	0.5	1.9	ns	3 - 6	1, 2, 10 - 13	16	8	1, 2, 14, 15
t_{PLH}	Propagation Delay Data to Output	0.5	1.8	0.5	2.2	0.5	1.9	ns	3 - 6	1, 2, 10 - 13	16	8	1, 2, 14, 15
t_{PHL}	Propagation Delay Select to Output	1.0	2.7	1.0	3.0	1.0	2.7	ns	3 - 6, 10 - 13	1, 2	16	8	1, 2, 14, 15
t_{PLH}	Propagation Delay Select to Output	1.0	2.7	1.0	3.0	1.0	2.7	ns	3 - 6, 10 - 13	1, 2	16	8	1, 2, 14, 15

12-Bit Parity Generator Checker

ELECTRICALLY TESTED PER:
5962-8756201

The 10H560 is a 12-bit parity generator-checker. The output goes high when an odd number of inputs are high providing the odd parity function. Unconnected inputs are pulled to a logic low allowing parity detection and generation for less than 12 bits.

The 10H560 is a functional pin duplication of the standard 10K family part with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 2.5 ns Typical
- 480 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

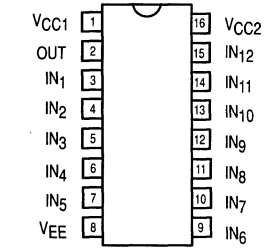
1) JAN: N/A
2) SMD: 5962-8756201
3) 883: 10H560/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

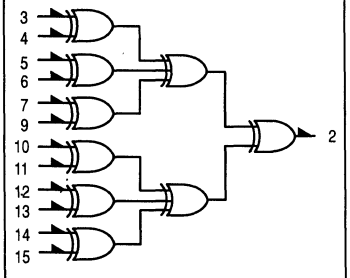
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Out	2	6	3	51 Ω to V_{TT}
IN_1	3	7	4	GND
IN_2	4	8	5	OPEN
IN_3	5	9	7	OPEN
IN_4	6	10	8	OPEN
IN_5	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
IN_6	9	13	12	OPEN
IN_7	10	14	13	GND
IN_8	11	15	14	OPEN
IN_9	12	16	15	OPEN
IN_{10}	13	1	17	OPEN
IN_{11}	14	2	18	OPEN
IN_{12}	15	3	19	GND
V_{CC2}	16	4	20	GND

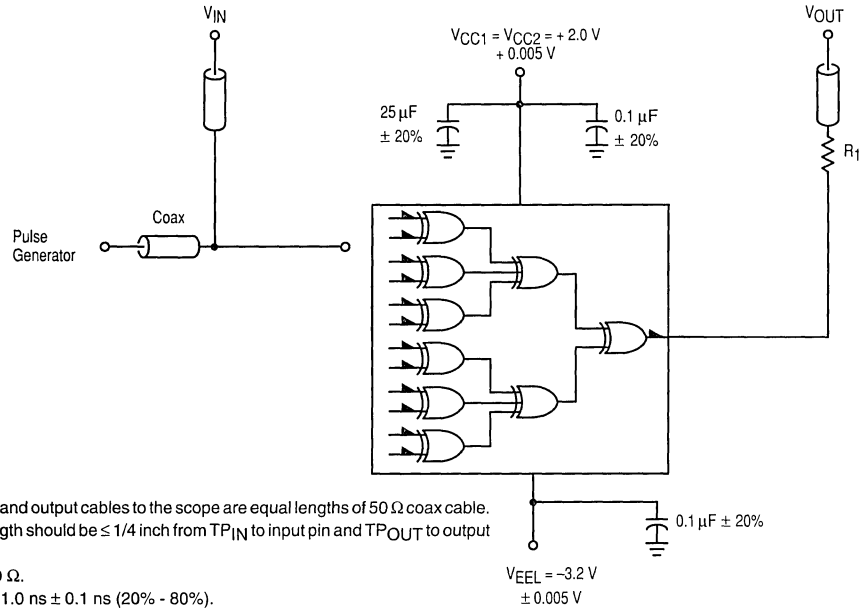


BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Truth Table	
Input	**Output**
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

POSITIVE LOGIC DIAGRAM





NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coax cable. Wire length should be ≤ 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. R_1 = 50 Ω.
3. $t_r = t_f$ = 1.0 ns ± 0.1 ns (20% - 80%).
4. P_W ≥ 20 ns.
5. P_{RR} = 1.0 MHz.

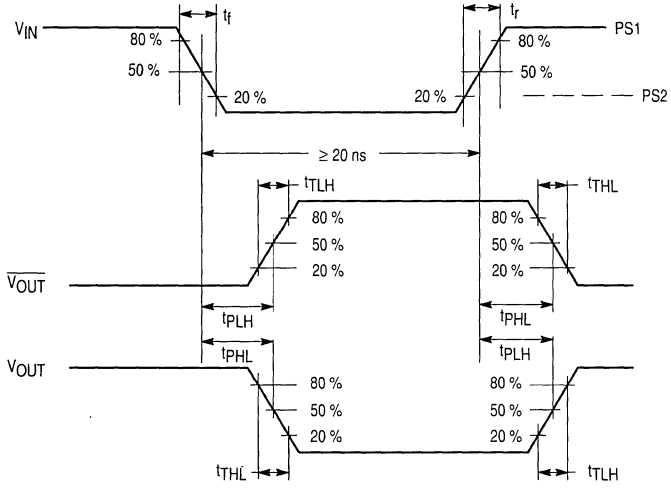


Figure 1. Switching Test Circuit and Waveforms

10H560
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE2}	V_{EE1}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 15	3 - 7				8	1, 16	2
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	3 - 7 9 - 15	3 - 7 9 - 15				8	1, 16	2
V_{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 11 13	4 - 7 9 -15	3, 5, 7 10, 12 14	12	8	8	1, 16	2
V_{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	3 - 7 9 - 14	4 - 7 9 -15	4, 6, 9 11, 13 15	3	8	8	1, 16	2
I_{EE}	Power Supply Current	-78		-88		-88		mA						8	1, 16	8
I_{IH}	Input Current High		245		390		390	µA	4, 5, 9 10, 13, 14					8	1, 16	4, 5, 9, 10, 13, 14
I_{IH1}	Input Current High		285		455		455	µA	3, 6, 7 11, 12 15					8	1, 16	3, 6, 7, 11, 12, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 7 9 - 15				8	1, 16	3 - 7, 9 - 15

10H560
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		P_{S2}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T.
t_{TLH}	Rise Time	0.55	1.8	0.75	1.9	0.55	1.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{THL}	Fall Time	0.55	1.8	0.75	1.9	0.55	1.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PLH1}	Propagation Delay (3, 5, 7, 10, 12, 14)	1.2	2.9	1.35	3.2	1.15	2.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PHL1}	Propagation Delay (3, 5, 7, 10, 12, 14)	1.45	3.0	1.7	3.4	1.4	2.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PHL2}	Propagation Delay (3, 5, 7, 10, 12, 14)	1.3	2.9	1.55	3.2	1.25	2.9	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PLH2}	Propagation Delay (3, 5, 7, 10, 12, 14)	1.4	3.2	1.55	3.6	1.35	2.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PLH1}	Propagation Delay (4, 6, 9, 11, 13, 15)	1.1	2.9	1.25	3.2	1.05	2.7	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PHL1}	Propagation Delay (4, 6, 9, 11, 13, 15)	1.15	2.7	1.35	3.2	1.1	2.6	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PHL2}	Propagation Delay (4, 6, 9, 11, 13, 15)	1.2	2.8	1.45	3.0	1.15	2.6	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1, 16	8	4 - 7, 9 - 15	2
t_{PLH2}	Propagation Delay (4, 6, 9, 11, 13, 15)	1.1	3.0	1.25	3.3	1.1	2.8	ns	4 - 7, 9 - 15	4 - 7, 9 - 15	2	1 ,16	8	4 - 7, 9 - 15	2

Binary to 1-8 Decoder (Low)

ELECTRICALLY TESTED PER:
5962-8756701

The 10H561 provides parallel decoding of a three bit binary word to one of eight lines. The 10H561 is useful in high-speed multiplexer/demultiplexer applications.

The 10H561 is designed to decode a three bit input word to one of eight output lines. The 10H561 output will be low when selected while all other outputs are high. The enable inputs, when either or both are high, force all outputs high.

The 10H561 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.

- Propagation Delay, 1.5 ns Typical
- 470 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

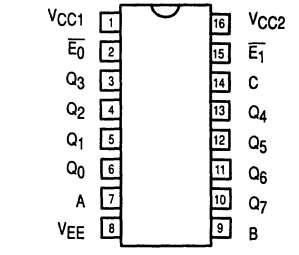
1) JAN: N/A
2) SMD: 5962-8756701
3) 883: 10H561/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

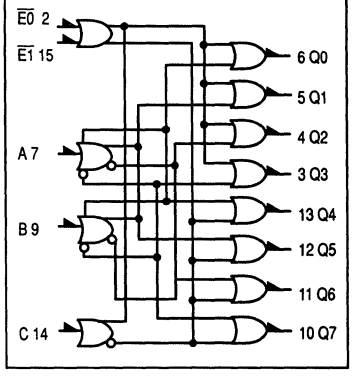
The letter "M" appears before the slash on LCC.

	PIN ASSIGNMENTS			
FUNCTION	**DIL**	**FLATS**	**LCC**	**BURN-IN (CONDITION C)**
V_{CC1}	1	5	2	GND
$\overline{E_0}$	2	6	3	GND
Q_3	3	7	4	V_{TT}
Q_2	4	8	5	V_{TT}
Q_1	5	9	7	V_{TT}
Q_0	6	10	8	V_{TT}
A	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B	9	13	12	OPEN
Q_7	10	14	13	V_{TT}
Q_6	11	15	14	V_{TT}
Q_5	12	16	15	V_{TT}
Q_4	13	1	17	V_{TT}
C	14	2	18	GND
$\overline{E_1}$	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



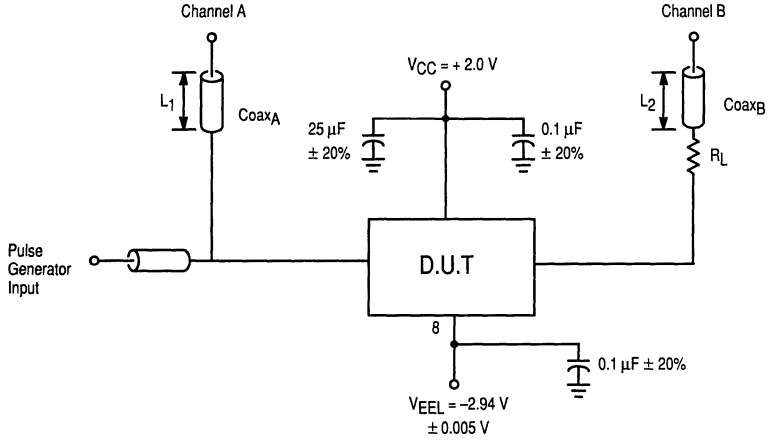
POSITIVE LOGIC DIAGRAM



TRUTH TABLE

Enable Inputs		Inputs			Outputs							
$\overline{E_1}$	$\overline{E_0}$	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	Ø	Ø	Ø	Ø	H	H	H	H	H	H	H	H
Ø	H	Ø	Ø	Ø	H	H	H	H	H	H	H	H

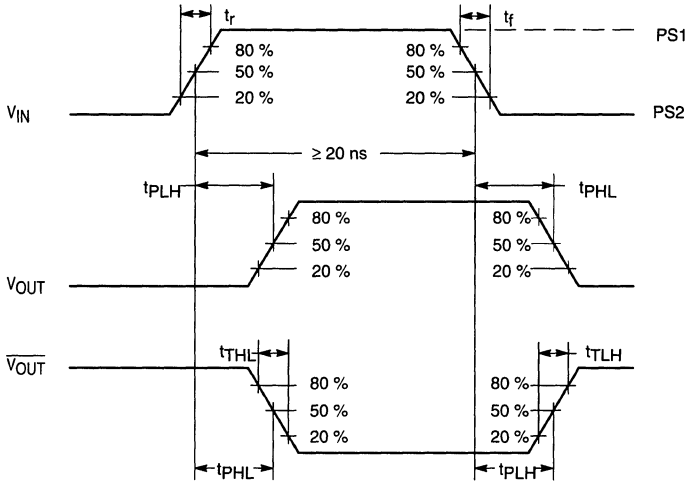
Ø = Don't Care



NOTES

1. All other outputs loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. $L_1 = L_2$: Matched for equal time delay.
4. R_L = 50 Ω.

Figure 1. Switching Test Circuit



NOTES
1. V_{IN} = 20 ns.
2. f_{IN} = 1.0 MHz.
3. $t_r = t_f$ = 1.0 ns ± 0.1 ns (20% - 80%).

Figure 2. Switching Test Circuit Waveforms

10H561
QUIESCENT LIMIT TABLE*

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	2, 7, 9				8		1, 16	3 - 6, 10 - 13
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.535	-1.95	-1.61	V	7, 9, 14				8		1, 16	3 - 6, 10 - 13
V_{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	7, 9, 14		2, 7, 9 14, 15	7, 9, 14	8	8	1, 16	3 - 6, 10 - 13
V_{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.535	-1.95	-1.61	V	7, 9, 14		7, 9, 14		8	8	1, 16	3 - 6, 10 - 13
I_{EE}	Power Supply Current	-76		-84		-84		mA	2, 7, 9, 14, 15				8		1, 16	8
I_{IH}	Input Current High		275		465		465	µA	2, 7, 9, 14, 15				8		1, 16	2, 7, 9, 14, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		2, 7, 9, 14, 15				8	1, 16	2, 7, 9, 14, 15

10H561
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		P_{S2}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T.
t_{TLH}	Rise Time	0.55	1.5	0.6	1.6	0.55	1.5	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{THL}	Fall Time	0.55	1.5	0.6	1.6	0.55	1.5	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PLH1}	Propagation Delay Data	0.85	2.1	1.05	2.3	0.8	1.9	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PHL1}	Propagation Delay Data	0.65	2.2	0.7	2.3	0.6	2.2	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PLH}	Rise Time for Pins Enable	1.25	2.3	1.4	2.6	1.15	2.2	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PHL}	Rise Time for Pins Enable	0.8	2.3	0.9	2.4	0.8	2.3	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PLH2}	Propagation Delay Data	0.75	2.1	0.85	2.3	0.7	2.0	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13
t_{PHL2}	Propagation Delay Data	0.8	2.2	1.0	2.4	0.75	2.2	ns	7, 9 14, 15	2, 7, 9, 14	3 - 6, 10 -13	1, 16	8	7, 9 14	3 - 6 10 - 13

Binary to 1-8 Decoder (High)

ELECTRICALLY TESTED PER:
MPG 10H562

The 10H562 provides parallel decoding of a three bit binary word to one of eight lines. The 10H562 is useful in high-speed multiplexer/demultiplexer applications.

The 10H562 is designed to decode a three bit input word to one of eight output lines. The 10H562 output will be low when selected while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

The 10H562 is a true parallel decoder. This eliminates unequal parallel path delay times found in other decoder designs. These devices are ideally suited for multiplexer/demultiplexer applications.

- Propagation Delay, 1.5 ns Typical
- 460 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

	PIN ASSIGNMENTS			
FUNCTION	**DIL**	**FLATS**	**LCC**	**BURN-IN (CONDITION C)**
V_{CC1}	1	5	2	GND
$\overline{E_0}$	2	6	3	OPEN
Q_3	3	7	4	V_{TT}
Q_2	4	8	5	V_{TT}
Q_1	5	9	7	V_{TT}
Q_0	6	10	8	V_{TT}
A	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
B	9	13	12	OPEN
Q_7	10	14	13	V_{TT}
Q_6	11	15	14	V_{TT}
Q_5	12	16	15	V_{TT}
Q_4	13	1	17	V_{TT}
C	14	2	18	OPEN
$\overline{E_1}$	15	3	19	OPEN
V_{CC2}	16	4	20	GND

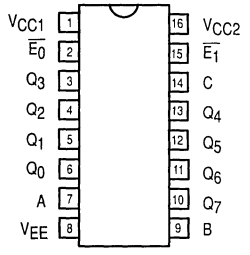
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

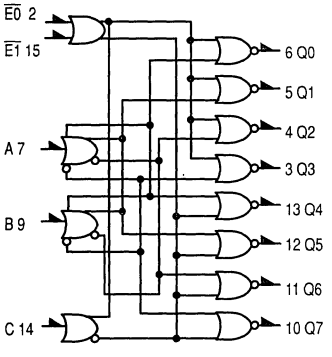
1) JAN: N/A
2) SMD: N/A
3) 883: 10H562/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



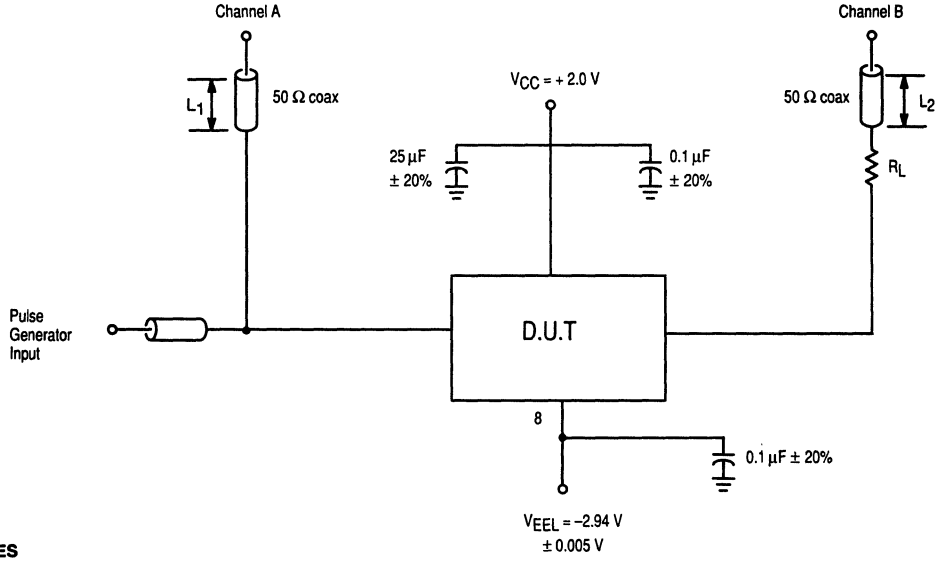
POSITIVE LOGIC DIAGRAM



10H562
TRUTH TABLE

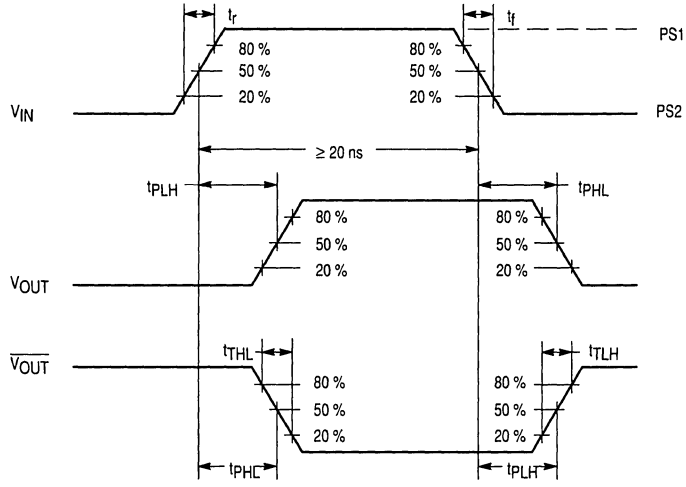
Enable Inputs		Inputs			Outputs							
$\overline{E_1}$	$\overline{E_0}$	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	Ø	Ø	Ø	Ø	L	L	L	L	L	L	L	L
Ø	H	Ø	Ø	Ø	L	L	L	L	L	L	L	L

Ø = Don't Care



NOTES
1. All other outputs loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. $L_1 = L_2$: Matched for equal time delay.
4. R_L = 50 Ω.

Figure 1. Switching Test Circuit



NOTES

V_{IN} has the following characteristics:

1. P_W = 20 ns.
2. f_{IN} = 1.0 MHz.
3. $t_r = t_f$ = 1.0 ns ± 0.1 ns (20% - 80%).

Figure 2. Switching Test Circuit Waveforms

10H562
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.780	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.735	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.840	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE2}	V_{EE1}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	7, 9, 14					8	1, 16	3 - 6, 10 - 13
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.363	-1.95	-1.61	V	2, 15					8	1, 16	3 - 6, 10 - 13
V_{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	7, 9, 14		2, 7, 9 14, 15	7, 9 14, 15	8	8	1, 16	3 - 6, 10 - 13
V_{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.363	-1.95	-1.61	V	7, 9, 14		7, 9, 14	2, 7, 9 14, 15	8	8	1, 16	3 - 6, 10 - 13
I_{EE}	Power Supply Current	-76		-84		-84		mA						8	1, 16	8
I_{IH}	Input Current High		275		465		465	µA	2, 7, 9 14, 15					8	1, 16	2, 7, 9, 14, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		2, 7, 9 14, 15			8		1, 16	2, 7, 9, 14, 15

10H562
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.780	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.735	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.840	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		P_{S2}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T.
t_{TLH}	Rise Time	0.6	1.9	0.6	2.0	0.6	1.8	ns	7, 9 14, 15	2, 7, 9,14	3 - 6, 10 - 13	1, 16	8	7, 9 14, 15	3 - 6, 10 - 13
t_{THL}	Fall Time	0.6	1.9	0.6	2.0	0.6	1.8	ns	7, 9 14, 15	2, 7, 9,14	3 - 6, 10 - 13	1, 16	8	7, 9 14, 15	3 - 6, 10 - 13
t_{PLH}	Propagation Delay	0.7	2.4	0.8	2.7	0.7	2.3	ns	7, 9 14, 15	2, 7, 9,14	3 - 6, 10 - 13	1, 16	8	7, 9 14, 15	3 - 6, 10 - 13
t_{PHL}	Propagation Delay	0.7	2.4	0.8	2.7	0.7	2.3	ns	7, 9 14, 15	2, 7, 9,14	3 - 6, 10 - 13	1, 16	8	7, 9 14, 15	3 - 6, 10 - 13

8-Line Multiplexer

Military 10H564

ELECTRICALLY TESTED PER:
5962-8772901

The 10H564 is a MECL 10H part which is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power supply current.

The 10H564 is designed to be used in data multiplexing and parallel to serial conversion applications. Full parallel gating provides equal delays through any data path. The 10H564 incorporates an output buffer, eight inputs and an enable. A high on the enable forces the output low. The open emitter output allows the 10H564 to be connected directly to a data bus. The enable line allows an easy means of expanding to more than 8 lines using additional 10H564's.

- Propagation Delay, 1.5 ns Typical
- 455 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8772901
3) 883: 10H564/BXAJC
X = CASE OUTLINE AS FOLLOWS:

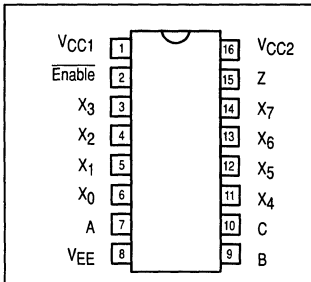
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

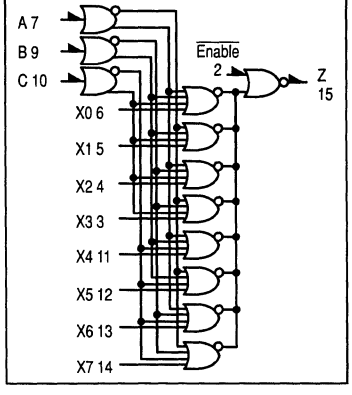
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{\text{Enable}}$	2	6	3	OPEN
X_3	3	7	4	OPEN
X_2	4	8	5	OPEN
X_1	5	9	7	OPEN
X_0	6	10	8	GND
A	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B	9	13	12	OPEN
C	10	14	13	OPEN
X_4	11	15	14	OPEN
X_5	12	16	15	OPEN
X_6	13	1	17	OPEN
X_7	14	2	18	OPEN
Z	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



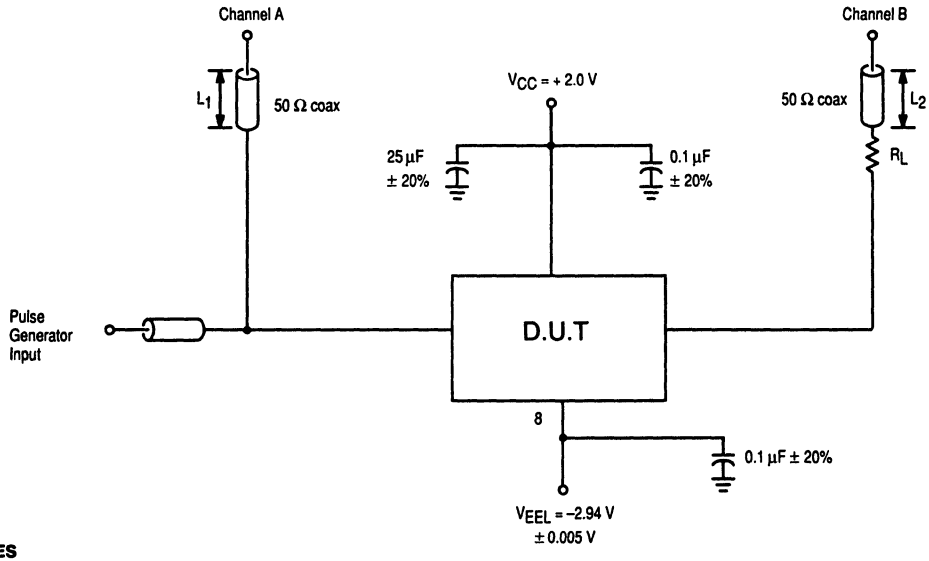
LOGIC DIAGRAM



TRUTH TABLE

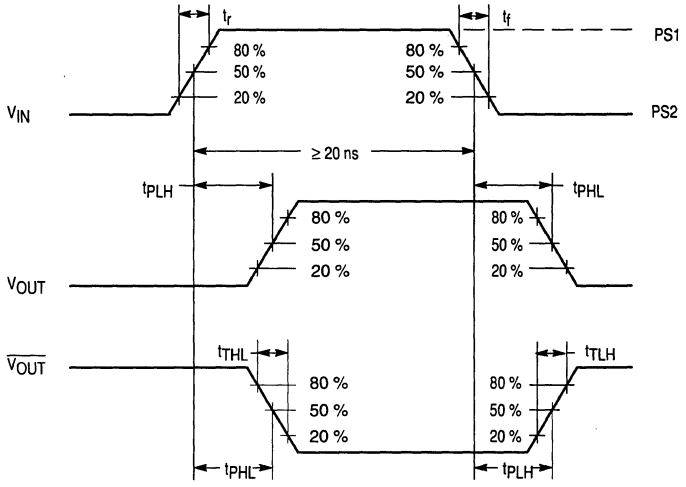
	ADDRESS INPUTS			
$\overline{\text{ENABLE}}$	C	B	A	Z
L	L	L	L	X_0
L	L	L	H	X_1
L	L	H	L	X_2
L	L	H	H	X_3
L	H	L	L	X_4
L	H	L	H	X_5
L	H	H	L	X_6
L	H	H	H	X_7
H	Ø	Ø	Ø	L

Ø = Don't Care



NOTES
1. All other outputs loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. $L_1 = L_2$: Matched for equal time delay.
4. $R_L = 50\ \Omega$.

Figure 1. Switching Test Circuit



NOTES

V_{IN} has the following characteristics:

1. P_W = 20 ns.
2. f_{IN} = 1.0 MHz.
3. $t_r = t_f$ = 1.0 ns ± 0.1 ns (20% - 80%).

Figure 2. Switching Test Circuit Waveforms

10H564
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE2}	V_{EE1}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 14	2, 9 10				8	1, 16	15
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	2, 7, 9 10, 14	2 - 7 9 - 14				8	1, 16	15
V_{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 13	2, 7, 9 10	3 - 5, 7 9 - 14	2, 7 9, 10	8	8	1, 16	15
V_{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	7, 9 10, 14	2, 7, 9 10	2	3 - 6 11 - 14	8	8	1, 16	15
I_{EE}	Power Supply Current	-75		-83		-83		mA						8	1, 16	8
I_{IH}	Input Current High		320		510		510	µA	2 - 7 9 - 14					8	1, 16	2 - 7, 9- 14
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		2 - 7 9 - 14			8		1, 16	2 - 7, 9 - 14

10H564
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		P_{S2}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T.
t_{TLH}	Rise Time	0.5	1.7	0.5	1.7	0.5	1.7	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{THL}	Fall Time	0.5	1.7	0.5	1.7	0.5	1.7	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PLH}	Propagation Delay Address to Output	1.45	2.7	1.6	3.2	1.4	2.6	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PHL}	Propagation Delay Address to Output	1.45	3.2	1.6	3.4	1.4	3.1	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PLH}	Propagation Delay Data to Output	1.0	2.3	1.15	2.6	1.0	2.2	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PHL}	Propagation Delay Data to Output	1.1	2.7	1.6	3.4	1.0	2.5	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PLH}	Propagation Delay Enable to Output	0.5	1.9	0.55	2.0	0.45	2.0	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15
t_{PHL}	Propagation Delay Enable to Output	0.66	2.0	0.7	2.0	0.55	2.0	ns	2 - 7 9 - 14	2 - 7 9 - 14	15	1, 16	8	2 - 7 9 - 14	15

Dual Binary to 1-4 Decoder (Low)

Military 10H571

ELECTRICALLY TESTED PER:
5962-8756801

The 10H571 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either $\overline{E_0}$ or $\overline{E_1}$ high, the corresponding selected 4 outputs are high. The common enable $\overline{E}$, when high, forces all outputs high.

- Propagation Delay, 2.0 ns Typical
- 460 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{E_1}$	2	6	3	GND
Q_{13}	3	7	4	51 Ω to V_{TT}
Q_{12}	4	8	5	51 Ω to V_{TT}
Q_{11}	5	9	7	51 Ω to V_{TT}
Q_{10}	6	10	8	51 Ω to V_{TT}
B	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
A	9	13	12	OPEN
Q_{03}	10	14	13	51 Ω to V_{TT}
Q_{02}	11	15	14	51 Ω to V_{TT}
Q_{01}	12	16	15	51 Ω to V_{TT}
Q_{00}	13	1	17	51 Ω to V_{TT}
$\overline{E_0}$	14	2	18	GND
$\overline{E}$	15	3	19	GND
V_{CC2}	16	4	20	GND

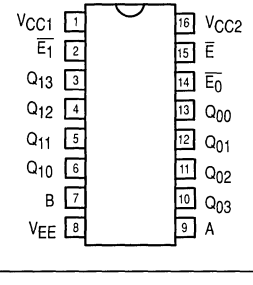
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

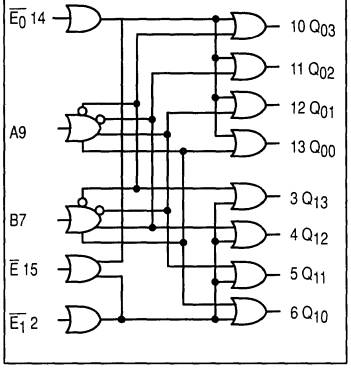
1) JAN: N/A
2) SMD: 5962-8756801
3) 883: 10H571/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



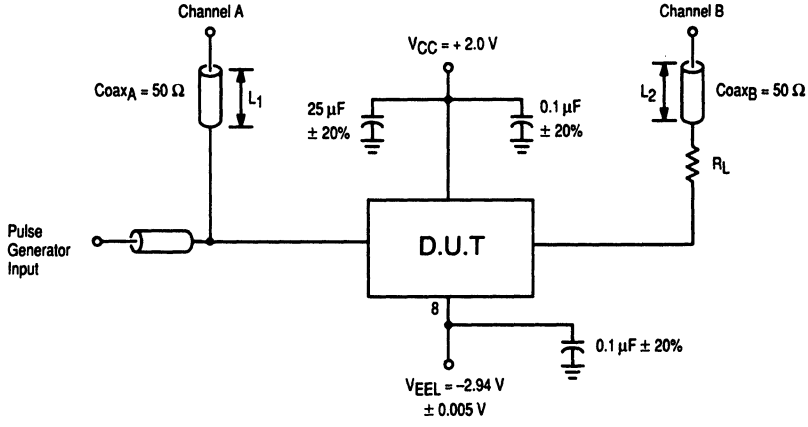
POSITIVE LOGIC DIAGRAM



TRUTH TABLE

Enable Inputs			Inputs		Outputs							
$\overline{E}$	$\overline{E_0}$	$\overline{E_1}$	A	B	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{00}	Q_{01}	Q_{02}	Q_{03}
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	Ø	Ø	Ø	Ø	H	H	H	H	H	H	H	H

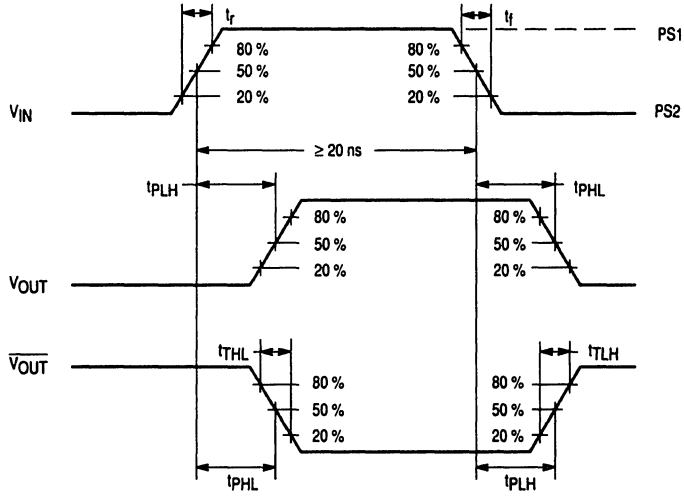
Ø = Don't Care



NOTES

1. All other outputs loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. $L_1 = L_2$: Matched for equal time delay.
4. R_L = 50 Ω.

Figure 1. Switching Test Circuit



NOTES
1. V_{IN} = 20 ns.
2. f_{IN} = 1.0 MHz.
3. $t_r = t_f$ = 1.0 ns ± 0.1 ns (20% - 80%).

Figure 2. Switching Test Circuit Waveforms

10H571
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-4.94	-2.94	-5.46
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-4.94	-2.94	-5.46
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-4.94	-2.94	-5.46

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C Subgroup 1		+ 125 °C Subgroup 2		- 55 °C Subgroup 3			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE2}	V_{EE1}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	15					8	1, 16	3 - 6, 10 - 13
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.363	-1.95	-1.61	V	7, 9					8	1, 16	3 - 6, 10 - 13
V_{OH1}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	7, 9		2, 7, 9 15	7, 9	8	8	1, 16	3 - 6, 10 - 13
V_{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.363	-1.95	-1.61	V	7, 9		7, 9	2, 7, 9 15	8	8	1, 16	3 - 6, 10 - 13
I_{EE}	Power Supply Current	-77		-85		-85		mA						8	1, 16	8
I_{IH}	Input Current High		275		465		465	μA	2, 7, 9 14, 15					8	1, 16	2 - 7, 9, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		μA		2, 7, 9 14, 15				8	1, 16	2 - 7, 9, 15

10H571
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-4.94	-2.94	-5.46
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-4.94	-2.94	-5.46
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-4.94	-2.94	-5.46

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T.
t_{TLH}	Rise Time	0.5	2.0	0.6	2.2	0.4	2.2	ns	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13
t_{THL}	Fall Time	0.5	2.0	0.6	2.2	0.4	2.2	ns	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13
t_{PLH}	Propagation Delay	0.5	3.0	0.5	3.2	0.5	3.2	ns	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13
t_{PHL}	Propagation Delay	0.5	3.0	0.5	3.2	0.5	3.2	ns	2, 7, 9, 14	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13

MOTOROLA

Dual 4 to 1 Multiplexer

Military 10H574

ELECTRICALLY TESTED PER:
5962-8750601

The 10H574 is a Dual 4-to-1 Multiplexer. This device is a functional/pinout duplication of the standard MECL 10K part, with 100% improvement in propagation delay and no increase in power supply current.

- Propagation Delay, 1.5 ns Typical
- 440 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_0	2	6	3	51 Ω to V_{TT}
DO0	3	7	4	OPEN
DO2	4	8	5	OPEN
DO1	5	9	7	GND
DO3	6	10	8	GND
A	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
B	9	13	12	GND
D13	10	14	13	GND
D11	11	15	14	OPEN
D12	12	16	15	GND
D10	13	1	17	OPEN
$\overline{\text{Enable}}$	14	2	18	OPEN
Q_1	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

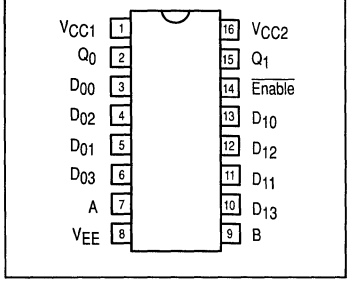
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

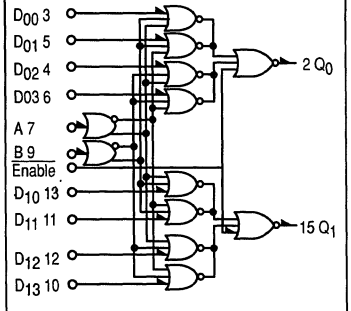
1) JAN: N/A
2) SMD: 5962-8750601
3) 883: 10H574/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



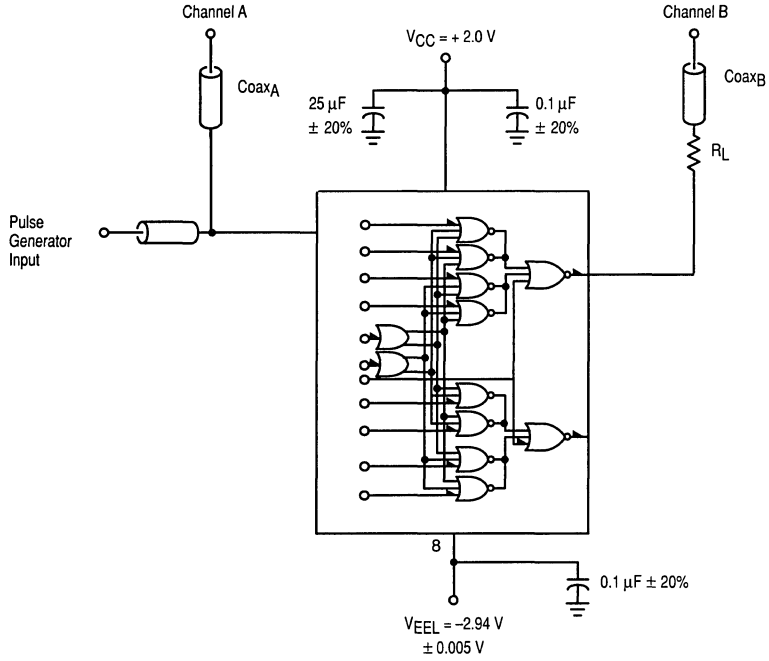
POSITIVE LOGIC DIAGRAM



TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Q_0	Q_1
H	Ø	Ø	L	L
L	L	L	D_{00}	D_{10}
L	L	H	D_{01}	D_{11}
L	H	L	D_{02}	D_{12}
L	H	H	D_{03}	D_{13}

Ø = Don't Care



NOTES

1. Unused outputs loaded 100 Ω to ground.
2. P_{RR} = 1.0 MHz.
3. $t_r = t_f$ = 1.0 ns ± 0.1 ns (20% - 80%).
4. R_L = 50 Ω.
5. P_W = 20 ns.

Figure 1. Switching Test Circuit

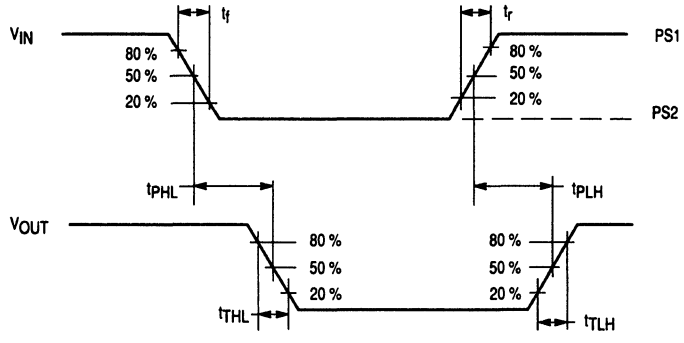


Figure 2. Switching Test Circuit Waveforms

10H574
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	-1.01	-0.78	-0.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 14	7, 9, 14			8		1, 16	2, 15
V_{OL}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	3, 7, 9, 13, 14	3 - 7 9 - 14			8		1, 16	2, 15
V_{OL1}	Low Output Voltage	-1.95	-1.58	-1.95	-1.565	-1.95	-1.61	V	7, 9, 14		7, 9, 14	3 - 7 9 - 13	8	8	1, 16	2 - 4 13 - 15
V_{OH1}	High Output Voltage	-1.01	-0.78	-1.86	-0.65	-1.06	-0.84	V	3 - 7 9 - 13		3 - 7 9 - 13	7, 9, 14	8	8	1, 16	2, 15
I_{IH}	Power Supply Current		300		475		475	µA	3 - 7 9 - 13				8		1, 16	3 - 7, 9 - 13
I_{IH1}	Input Current High		420		670		670	µA	14				8		1, 16	14
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 7 9 - 14			8		1, 16	3 - 7, 9 - 14
I_{EE}	Power Supply Drain Current	-73		-80		-80		mA					8		1, 16	8

10H574
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25° C		+ 125° C		- 55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P.U.T.
t_{TLH}	Rise Time	0.5	1.7	0.5	2.0	0.4	1.65	ns	3 - 7, 9 -14	2, 15	1, 16	8	3 - 5, 9, 11 - 13	2, 15
t_{THL}	Fall Time	0.5	1.7	0.5	2.0	0.4	1.65	ns	3 - 7, 9 -14	2, 15	1, 16	8	3 - 5, 9, 11 - 13	2, 15
t_{PLH} t_{PHL}	Propagation Delay (A & B) note 1	1.2	2.9	1.5	3.6	1.1	2.75	ns	3 - 7, 9 -14	2, 15	1, 16	8	3 - 5, 9, 11 - 13	2, 15
t_{PLH} t_{PHL}	Propagation Delay (Data X & Y) note 2	1.0	2.4	1.0	2.9	0.8	2.25	ns	3 - 7, 9 -14	2, 15	1, 16	8	3 - 5, 9, 11 - 13	2, 15
t_{PLH} t_{PHL}	Propagation Delay ($\overline{\text{Enable}}$) note 3	0.5	1.8	0.5	2.0	0.5	1.7	ns	3 - 7, 9 -14	2, 15	1, 16	8	3 - 5, 9, 11 - 13	2, 15

Notes
1. Pins 7, 9.
2. Pins 3 - 6, 10 - 13.
3. Pins 14.

Hex "D" Master-Slave Flip-Flop

Military 10H576

ELECTRICALLY TESTED PER:
5962-8751201

The 10H576 contains six master slave type "D" flip-flops with a common clock. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock frequency and propagation delay and no increase in power-supply current.

- Propagation Delay, 1.7 ns Typical
- 675 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

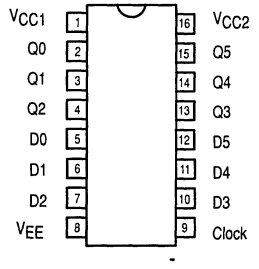
1) JAN: N/A
2) SMD: 5962-8751201
3) 883: 10H576/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

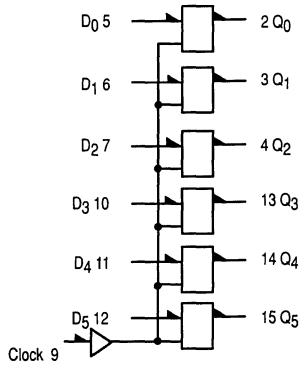
The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_0	2	6	3	51 Ω to V_{TT}
Q_1	3	7	4	51 Ω to V_{TT}
Q_2	4	8	5	51 Ω to V_{TT}
D0	5	9	7	GND
D_1	6	10	8	GND
D_2	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Clock	9	13	12	CP1
D_3	10	14	13	GND
D_4	11	15	14	GND
D_5	12	16	15	GND
Q_3	13	1	17	51 Ω to V_{TT}
Q_4	14	2	18	51 Ω to V_{TT}
Q_5	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



LOGIC DIAGRAM

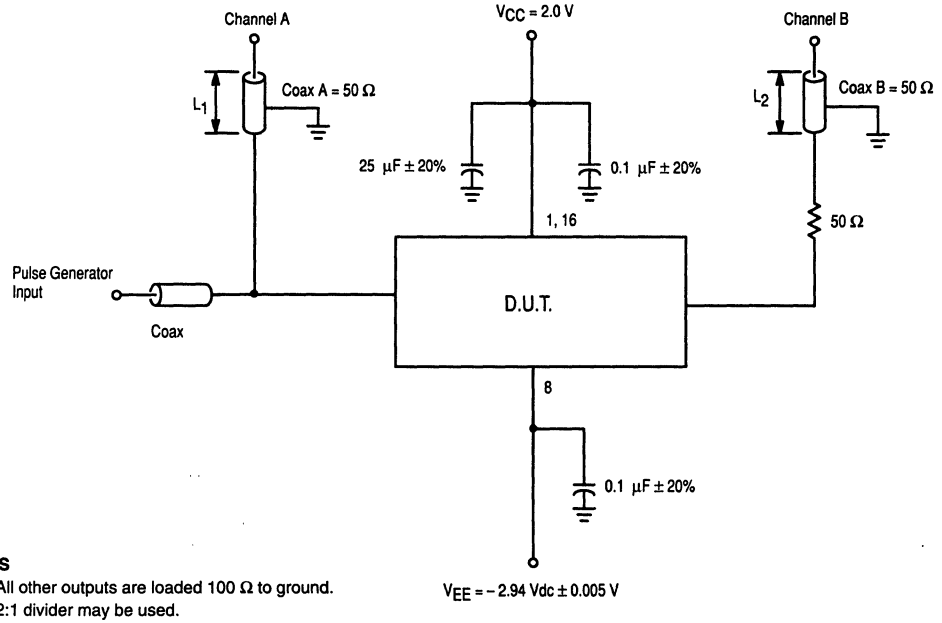


BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

CLOCK TRUTH TABLE		
C	D	Q_{n+1}
L	Ø	Q_n
H*	L	L
H*	H	H

Ø = Don't Care
* A clock H is a clock transition from a low to a high state

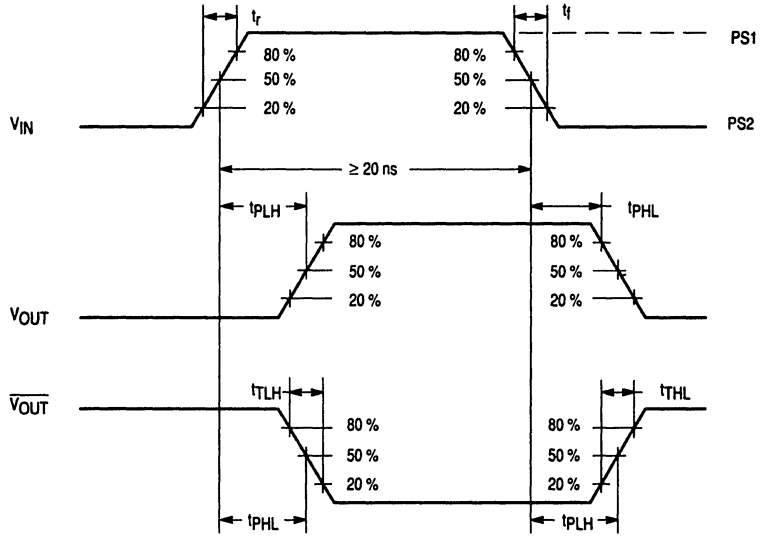
2



NOTES

1. All other outputs are loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. L_1: L_2: Matched for equal time delay.
4. V_{IN} = 20 ns.
5. f_{IN} = 1.0 MHz.
6. $t_r = t_f$ = 1.0 ns (20% - 80%) ± 0.1 ns.

Figure 1. Test Circuit



NOTES

1. All other outputs are loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. L_1: L_2: Matched for equal time delay.
4. V_{IN} = 20 ns.
5. f_{IN} = 1.0 MHz.
6. $t_r = t_f$ = 1.0 ns (20% - 80%) ± 0.1 ns.

Figure 2. Test Circuit Waveform

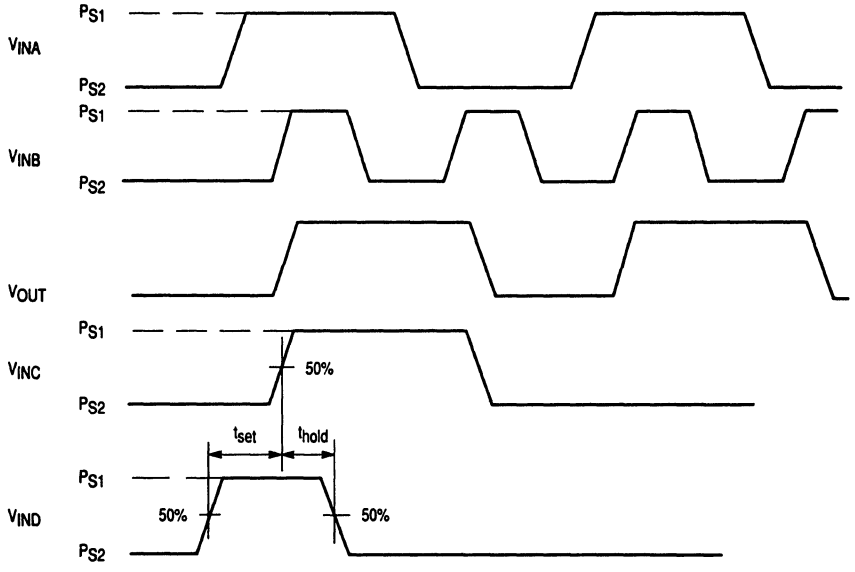


Figure 3. t_{SET} and t_{HOLD} Waveform

10H576
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE2}	V_{EE1}	V_{CC}	C_{P1}	P. U. T.
V_{OH}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	5 - 7 10 - 12					8	1, 16	9, P_1	2 - 4 13 - 15
V_{OL}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V		5 - 7 10 - 12				8	1, 16	9, P_1	2 - 4 13 - 15
V_{OH1}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	5 - 7 10 - 12	5 - 7 10 - 12	5 - 7 10 - 12		8	8	1, 16	9 P_1 –3	2 - 4 13 - 15
V_{OL1}	Low Output Voltage	– 1.96	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V	5 - 7 10 - 12	5 - 7 10 - 12		5 - 7 10 - 12	8	8	1, 16	9 P_1 –3	2 - 4 13 - 15
I_{EE}	Power Supply Current	– 112		– 123		– 123		mA						8	1, 16		8
I_{IH}	Input Current High		265		425		425	µA	5 - 7 10 - 12					8	1, 16		5 - 7 10 - 12
I_{IH1}	Input Current High		420		670		670	µA	9					8	1, 16		9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7 9 - 12			8		1, 16		5 - 7 10 - 12

NOTES

1. Hold power during all V_{OH} and V_{OL} tests.
2. P1) V_{IH} / V_{IL} P2) V_{IH} / V_{IH2} P3) V_{IH} / V_{IL2}

10H576
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	0.7	1.8	0.8	1.9	0.8	1.8	ns	5 - 7, 9 - 15	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
t_{THL}	Fall Time	0.7	1.8	0.8	1.9	0.8	1.8	ns	5 - 7, 9 - 15	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
t_{PLH}	Propagation Delay	1.0	2.7	1.0	3.0	1.0	2.9	ns	5 - 7, 9 - 15	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
t_{PHL}	Propagation Delay	1.0	2.7	1.0	3.0	1.0	2.9	ns	5 - 7, 9 - 15	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
t_{Setup}	Setup Time	1.5		1.5		1.5		ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
t_{Hold}	Hold Time	0.8		0.8		0.8		ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
f_{Toggle}	Toggle Frequency	250		250		250		MHz	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15

4-Bit Arithmetic Logic Unit/Function Generator

Military 10H581

ELECTRICALLY TESTED PER: MPG 10H581

2

The 10H581 is a high speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two 4-bit words. Full internal carry is incorporated for ripple-through operation. Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided allowing fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the 10579, full-carry look-ahead, as a second order look ahead block, the 10H581 provides high speed arithmetic operations on very long words.

This 10H part is a functional/pinout duplication of the standard MECL 10K family part with 100% improvement in propagation delay and not increase in power supply current.

- Improved Noise Margin, 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10H581/BXAJC
X = CASE OUTLINE AS FOLLOWS:

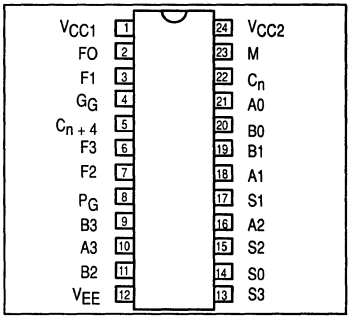
PACKAGE: CERDIP: K
CERFLAT: J

The letter "M" appears before the slash on LCC.

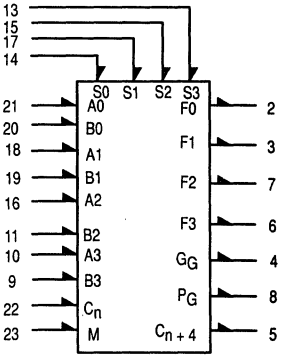
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CC1}	1	7	GND
F0	2	8	51 Ω to V_{TT}
F1	3	9	51 Ω to V_{TT}
G_G	4	10	51 Ω to V_{TT}
C_{n+4}	5	11	51 Ω to V_{TT}
F3	6	12	51 Ω to V_{TT}
F2	7	13	51 Ω to V_{TT}
P_G	8	14	51 Ω to V_{TT}
B3	9	15	50 Ω to V_{EE}
A3	10	16	GND
B2	11	17	50 Ω to V_{EE}
V_{EE}	12	18	V_{EE}
S3	13	19	50 Ω to V_{EE}
S0	14	20	GND
S2	15	21	50 Ω to V_{EE}
A2	16	22	GND
S1	17	23	GND
A1	18	24	50 Ω to V_{EE}
B1	19	1	V_{EE}
B0	20	2	50 Ω to V_{EE}
A0	21	3	GND
C_n	22	4	50 Ω to V_{EE}
M	23	5	GND
V_{CC2}	24	6	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM



ARITHMETIC/LOGIC FUNCTIONS

Function Select				Logic Function M is High C = D. C.	Arithmetic Operation M is Low C_n is low
S_3	S_2	S_1	S_0	F	F
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A} + \overline{B}$	F = A plus (A • $\overline{B}$)
L	L	H	L	$F = \overline{A} + B$	F = A plus (A • B)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A} \bullet B$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus (A • $\overline{B}$)
L	H	H	L	$F = A \ominus B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \bullet B$	F = (A + $\overline{B}$) plus 0
H	L	L	H	$F = A \oplus B$	F = A minus B minus 1
H	L	H	L	$F = B$	F = (A + $\overline{B}$) plus (A • B)
H	L	H	H	$F = A + B$	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$F = A \bullet \overline{B}$	F = (A • $\overline{B}$) minus 1
H	H	H	L	$F = A \bullet B$	F = (A • B) minus 1
H	H	H	H	F = A	F = minus 1

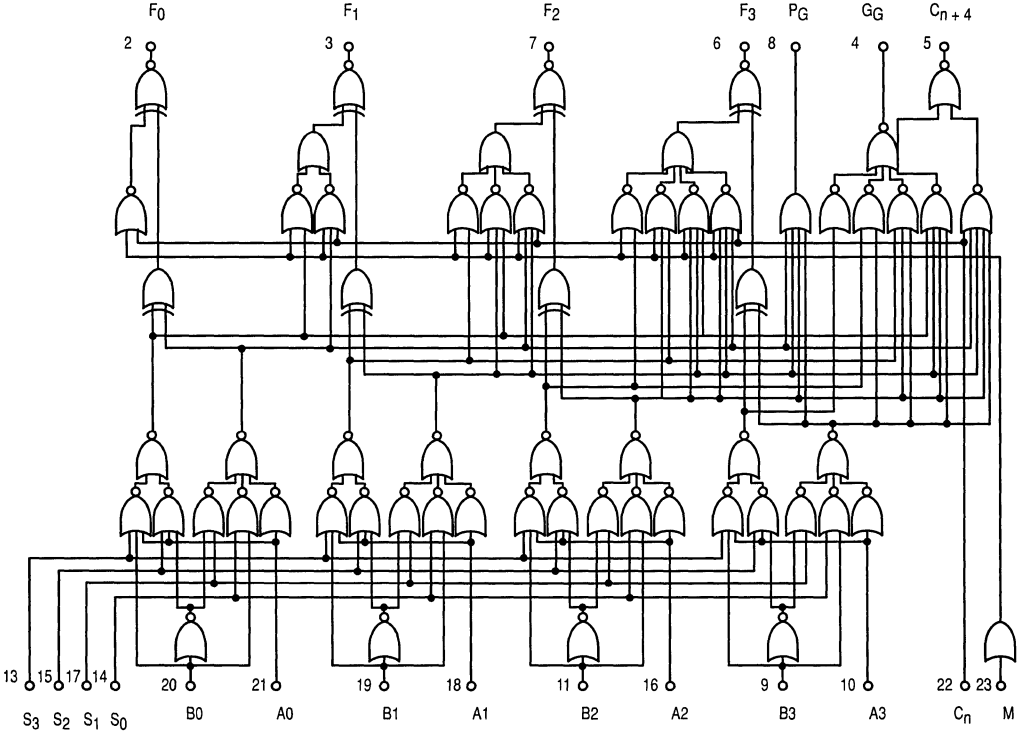
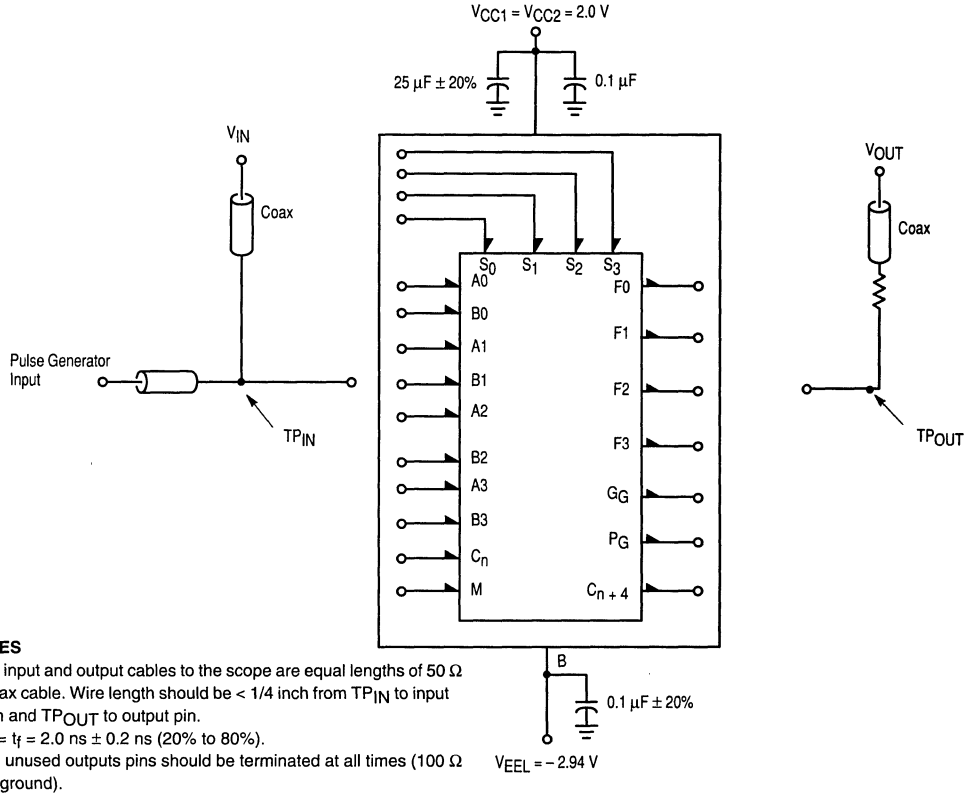


Figure 1. Logic Diagram



NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coax cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%).
3. All unused outputs pins should be terminated at all times (100 Ω to ground).
4. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) Frequency = 1.0 MHz.

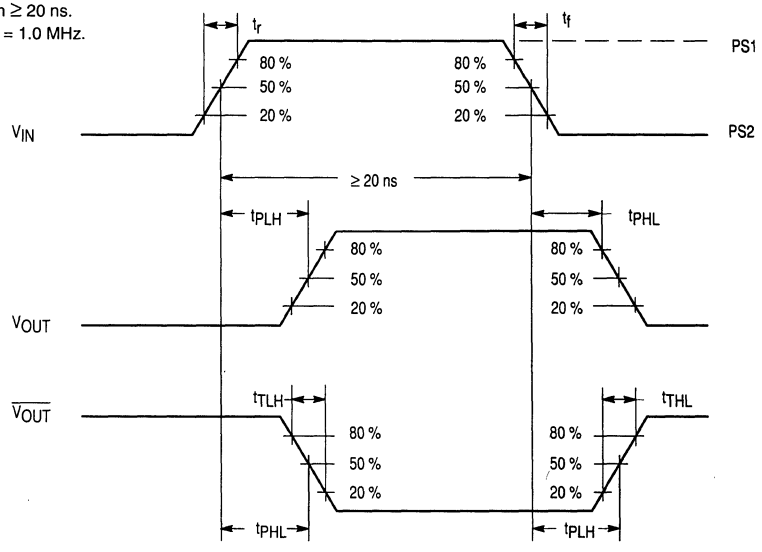


Figure 2. Switching Test Circuit and Waveforms

10H581
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.950	-1.105	-1.475	+1.11	+0.31	-5.46	-4.94
T_A = 125 °C	-0.65	-1.950	-1.000	-1.400	+1.24	+0.36	-5.46	-4.94
T_A = -55 °C	-0.88	-1.950	-1.255	-1.510	+1.01	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	$V_{EE1/2}$	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.09	– 0.88	V	9 - 11 16 - 23	13 - 15			12	1, 24	2 - 8
V_{OL1}	Low Output Voltage	– 1.85	– 1.620	– 1.82	– 1.545	– 1.92	– 1.655	V	9 - 11, 14, 16 18, 19, 21 - 23	9, 10, 13, 15 16, 17, 19, 21			12	1, 24	2, 3, 5 - 8
V_{OHA}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V	9 - 11, 13 16 - 23	13 - 23	16 - 23	13 - 15 22, 23	12	1, 24	2 - 8
V_{OLA}	Low Output Voltage	– 1.85	– 1.60	– 1.88	– 1.525	– 1.92	– 1.635	V		9 - 11, 13 - 23	14, 15	9 – 11 16 – 23	12	1, 24	2 - 8
V_{OL2}	Low Output Voltage	– 1.99	– 1.620	– 1.88	– 1.545	– 2.10	– 1.655	V	11, 14, 16, 18 20, 22, 23	9, 10, 13, 15 17, 19, 21	8		12	1, 24	4
I_{EE}	Power Supply Current	– 145		– 160		– 160		mA	9 - 11, 16 18 - 21				12	1, 24	12
I_{IH1}	Input Current High		200		340		340	µA	13, 23				12	1, 24	13, 23
I_{IH2}	Input Current High		220		375		375	µA	10, 16, 18 21				12	1, 24	10, 16, 18 21
I_{IH3}	Input Current High		245		415		415	µA	9, 11 19, 20				12	1, 24	9, 11, 19, 20
I_{IH4}	Input Current High		265		450		450	µA	14, 15, 17				12	1, 24	14, 15, 17
I_{IH5}	Input Current High		290		580		495	µA	22				12	1, 24	22
I_{IL}	Input Current Low	0.5		0.3		0.5		mA	9 - 11 13 - 23				1, 16		9 - 11, 13 - 23

10H581
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-4.94	-2.94
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-4.94	-2.94
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE1}	P_{S1}	P. U. T.
t_{TLH}/ t_{THL}	Rise & Fall Time	0.5	2.3	0.764	2.64	0.62	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay C_n to C_{n+4}	0.6	2.2	0.74	2.64	0.74	2.4	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.7	2.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay C_n to F	1.0	3.0	1.44	3.96	1.8	3.6	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.0	0.74	2.64	0.84	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay A to F	1.5	3.7	1.92	4.8	1.8	4.44	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.8	2.4	1.08	3.12	1.0	2.88	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay A to P_G	1.5	3.7	1.92	4.8	1.8	4.44	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.764	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay A to G_G	1.5	3.7	1.92	4.68	1.8	4.44	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.0	0.74	2.64	0.74	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay A to C_{n+4}	1.5	3.6	1.92	4.68	1.8	4.32	ns	"	"	"	"	"	"

10H581
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-4.94	-2.94
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-4.94	-2.94
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE1}	P_{S1}	P. U. T.
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.3	0.74	3.0	0.74	2.76	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay B to F	2.0	4.5	2.52	5.76	2.2	5.0	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.64	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay B to P_G	1.5	3.8	1.92	4.8	1.8	4.56	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.64	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay B to G_G	1.5	3.7	1.92	4.8	1.8	4.44	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.5	2.0	0.5	2.64	0.5	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay B to Cn + 4	2.0	4.0	2.52	5.16	2.4	4.8	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.7	2.3	0.86	3.0	0.86	2.76	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay M to F	1.5	4.2	1.92	5.4	1.8	5.04	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.0	0.74	2.64	0.74	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay S to F	1.5	4.5	1.92	5.76	1.8	5.4	ns	"	"	"	"	"	"

10H581
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-4.94	-2.94
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-4.94	-2.94
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE1}	P_{S1}	P. U. T.
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.4	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay S to P_G	1.5	4.0	1.92	5.16	1.8	4.8	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.6	2.2	0.74	2.88	0.74	2.64	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay S to C_{n+4}	1.5	4.1	1.92	5.28	1.8	4.92	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.5	3.2	0.5	4.0	0.5	3.84	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay S to G_G	1.3	4.5	1.68	5.76	1.56	5.4	ns	"	"	"	"	"	"

Hex "D" Master-Slave Flip-Flop with Reset

Military 10H586

ELECTRICALLY TESTED PER: 5962-8756301

The 10H586 is a hex D type flip-flop with common reset and clock lines. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in clock toggle frequency and propagation delay and no increase in power supply current.

- Propagation Delay, 1.7 ns Typical
- 660 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8756301
3) 883: 10H586/BXAJC
X = CASE OUTLINE AS FOLLOWS:

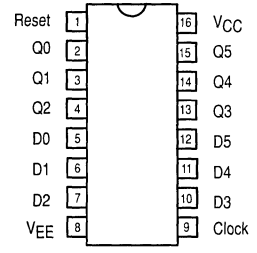
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

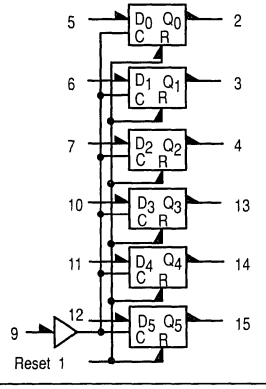
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_0	2	6	3	51 Ω to V_{TT}
Q_1	3	7	4	51 Ω to V_{TT}
Q_2	4	8	5	51 Ω to V_{TT}
D0	5	9	7	GND
D_1	6	10	8	GND
D_2	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Clock	9	13	12	CP1
D_3	10	14	13	GND
D_4	11	15	14	GND
D_5	12	16	15	GND
Q_3	13	1	17	51 Ω to V_{TT}
Q_4	14	2	18	51 Ω to V_{TT}
Q_5	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

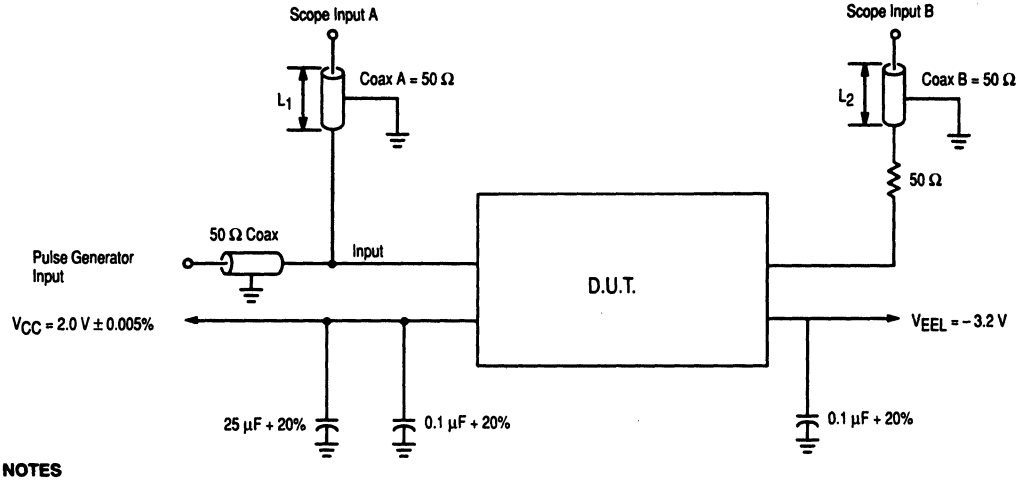


LOGIC DIAGRAM

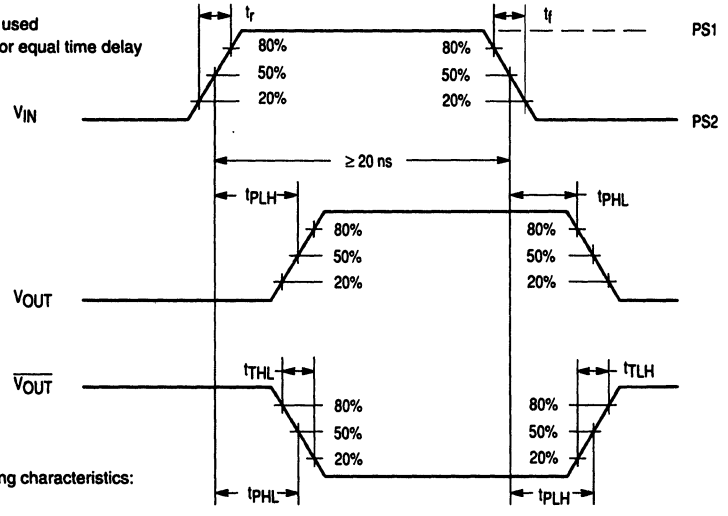


CLOCKED TRUTH TABLE			
R	C	Q	$Q_n + 1$
L	L	Ø	Q_n
L	H*	L	L
L	H*	H	H
H	L	Ø	L

Ø = Don't Care
* A clock H is a clock transition from a low to a high state



NOTES
1. Pulse generator must be capable of rise and fall time of 1.0 ns ± 0.1 ms
2. Unused outputs connected to 100 Ω resistor to ground
3. 2:1 divider may be used
4. L1 = L2: matched for equal time delay



NOTES
1. V_{IN} has the following characteristics:
   a) PW ≥ 20 ns
   b) f = 1.0 MHz

Figure 1. Switching Test Circuit and Waveforms

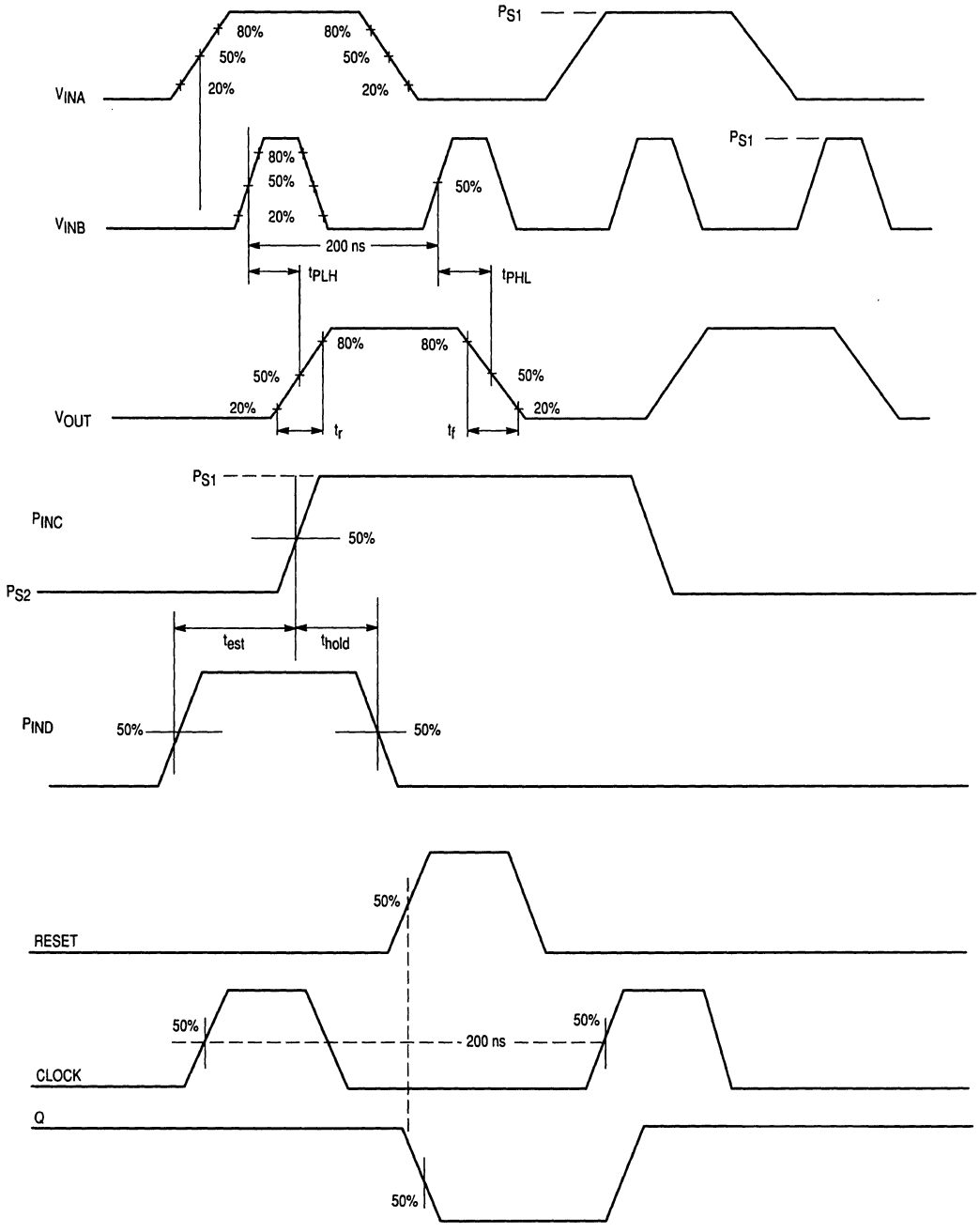


Figure 2. Switching Test Circuit and Waveforms

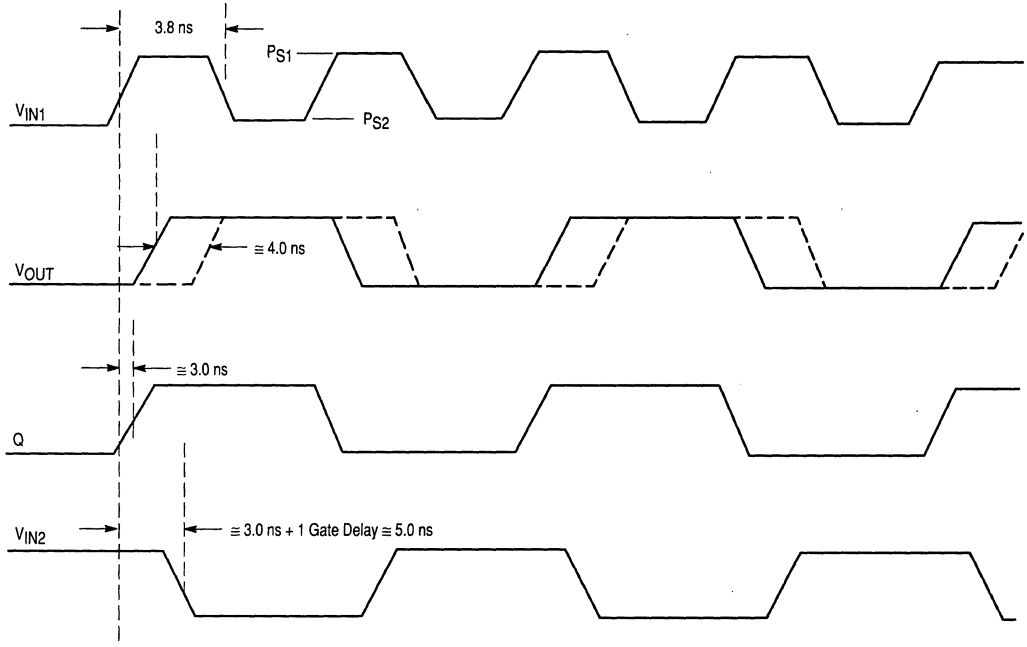


Figure 3. f_{TOGGLE} Waveforms

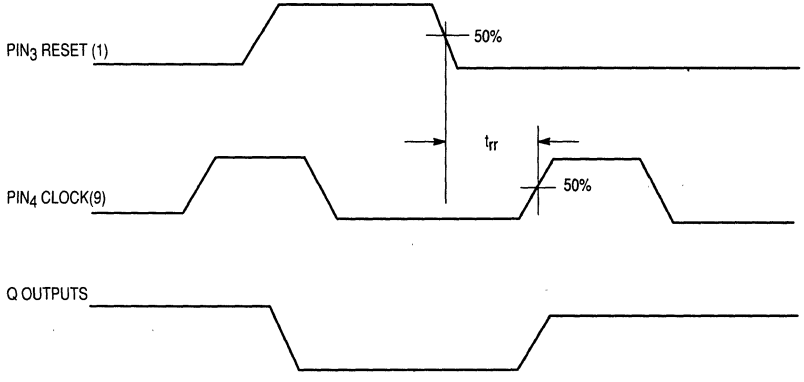


Figure 4. t_{rr} Waveforms

10H586
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	5 - 7 9 - 12	5 - 7 9 - 12			8		16	2 - 4, 13 - 15
V_{OL}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V	5 - 7 9 - 12	5 - 7 9 - 12			8		16	2 - 4, 13 - 15
V_{OH1}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	5 - 7 9 - 12	1, 5 - 7 10 - 12	5 - 7, 10 - 12	1	8	8	16	2 - 4, 13 - 15
V_{OL1}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V	5 - 7 10 - 12	1, 5 - 7 9 - 12	1	5 - 7, 10 - 12	8	8	16	2 - 4, 13 - 15
I_{EE}	Power Supply Current	– 110		– 121		– 121		mA					8		16	8
I_{IH}	Input Current High		420		670		670	µA	9				8		16	9
I_{IH1}	Input Current High		265		430		430	µA	5 - 7 10 - 12				8		16	5 - 7, 10 - 12
I_{IH2}	Input Current High		1200		1900		1900	µA	1				8		16	1
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		1, 5 - 7 9 - 12				8	16	1, 5 - 7, 9 - 12

NOTES

1. Hold power during all V_{OH} and V_{OL} tests.
2. P1) V_{IH} / V_{IL} P2) V_{IH} / V_{IH2} P3) V_{IH} / V_{IL2}

10H586
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		P_{S1}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	0.7	2.4	0.7	2.6	0.7	2.6	ns		5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{THL}	Fall Time	0.7	2.4	0.7	2.6	0.7	2.6	ns		5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{PLH}	Propagation Delay Clk or Reset to Q	0.7	2.7	0.7	3.0	0.7	3.0	ns	5 - 7 10 - 12	5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{PLH}	Propagation Delay Clk or Reset to Q	0.7	2.7	0.7	3.0	0.7	3.0	ns	5 - 7 10 - 12	5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{SET}	Setup Time	1.5		1.5		1.5		ns		5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{HOLD}	Hold Time	1.0		1.0		1.0		ns		5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
t_{RR}	Reset Recovery Time	3.0		3.0		3.0		ns	5 - 7 10 - 12	9	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15
f_{TOGGLE}	Toggle Frequency	250		250		250		MHz		5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	2 - 4, 13 - 15

Hex Buffer with Enable

Military 10H588

ELECTRICALLY TESTED PER:
5962-8750901

The 10H588 is a Hex Buffer with a common Enable input. When Enable is in the high state, all outputs are in the low-state. When Enable is in the low-state, the outputs take the same state as the inputs.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.3 ns Typical
- 250 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

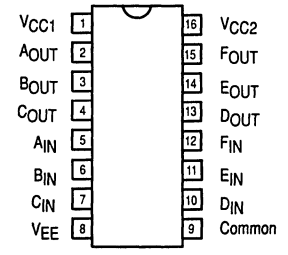
1) JAN: N/A
2) SMD: 5962-8750901
3) 883: 10H588/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

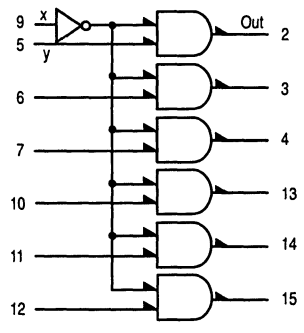
The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
C_{OUT}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	GND
B_{IN}	6	10	8	GND
C_{IN}	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Common	9	13	12	OPEN
D_{IN}	10	14	13	GND
E_{IN}	11	15	14	GND
F_{IN}	12	16	15	GND
D_{OUT}	13	1	17	51 Ω to V_{TT}
E_{OUT}	14	2	18	51 Ω to V_{TT}
F_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



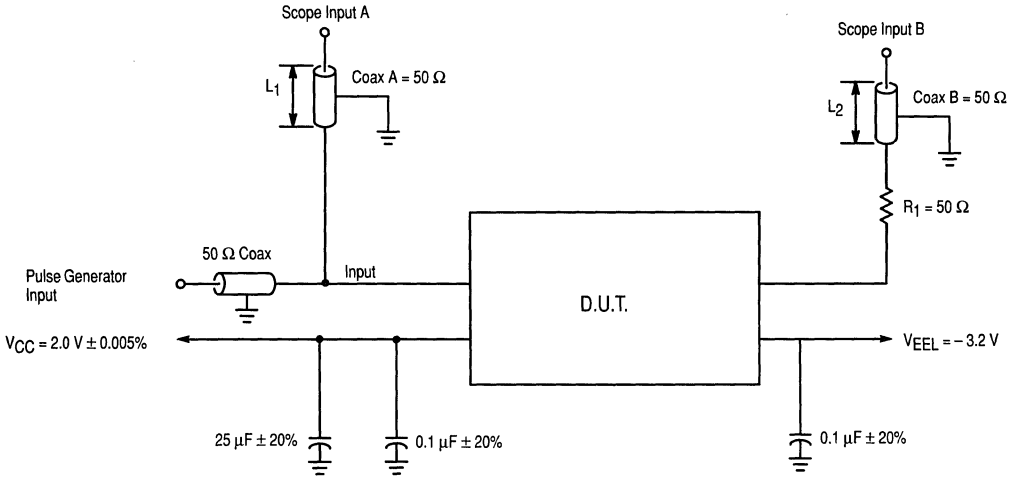
LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

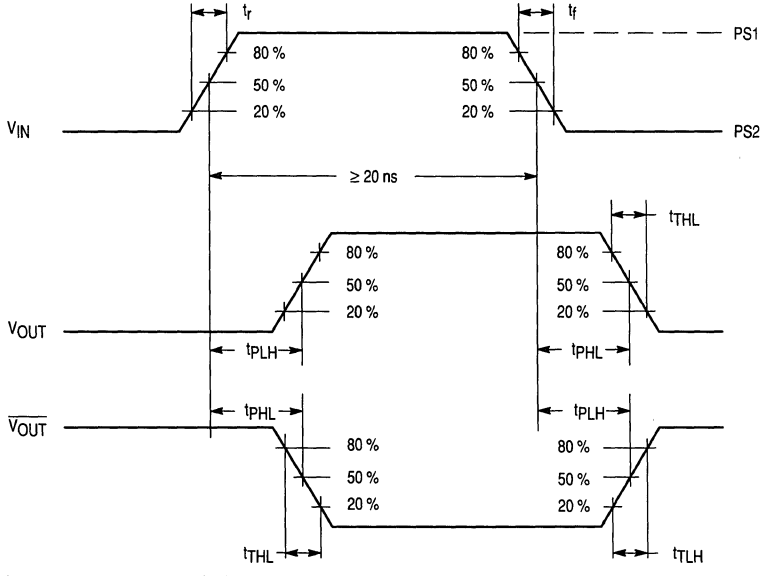
TRUTH TABLE		
Inputs		Output
X	Y	OUT
L	L	L
L	H	H
H	L	L
H	H	L

2



NOTES

1. Pulse generator must be capable of rise and fall time of 1.0 ns ± 0.1 ms
2. Unused outputs connected to 100 Ω resistor to ground
3. 2:1 divider may be used
4. L1 = L2: matched for equal time delay



NOTES

1. R_1 = 50 Ω in series with a 50 Ω coax constituting the 100 Ω load.
2. $t_r = t_f$ = 1.0 ns ± 0.1 ns.
3. PW ≥ 20 ns
4. f = 1.0 MHz.

Figure 1. Switching Test Circuit and Waveforms

10H588
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94
T_A = 125°C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	5 - 7 10 - 12		5 - 7 10 - 12	9	8		1, 16	2 - 4, 13 - 15
V_{OL}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V				9	8		1, 16	2 - 4, 13 - 15
V_{OH1}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	5 - 7 10 - 12			5 - 7 9 - 12	8	8	1, 16	2 - 4, 13 - 15
V_{OL1}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V	5 - 7 10 - 12		9	5 - 7 10 - 12	8	8	1, 16	2 - 4, 13 - 15
I_{EE}	Power Supply Current	– 42		– 46		– 46		mA					8		1, 16	8
I_{IH}	Input Current High		310		495		495	µA	5 - 7 9 - 12				8		1, 16	5 - 7, 9 - 12
I_{IL}	Input Current	0.5		0.3		0.5		µA		5 - 7 9 - 12				8	1, 16	5 - 7, 9 - 12

10H588
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.10	-1.480	+1.11	+0.31	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V				
		Subgroup 1		Subgroup 2		Subgroup 3							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	0.7	2.2	0.7	2.4	0.7	2.2	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
t_{THL}	Fall Time	0.7	2.2	0.7	2.4	0.7	2.2	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
t_{PHL} t_{PLH}	Propagation Delay Data	0.7	1.7	0.7	1.9	0.7	1.7	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15
t_{PLH} t_{PHL}	Propagation Delay Enable	0.7	2.6	0.7	2.8	0.7	2.5	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2 - 4, 13 - 15

Hex Inverter with Enable

ELECTRICALLY TESTED PER:
5962-8751001

The 10H589 is a Hex Inverter with a common Enable input. The hex inverting function is provided when Enable is in the low-state. When Enable is in the high-state, all outputs are low.

This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power-supply current.

- Propagation Delay, 1.3 ns Typical Data-to-Output
- 250 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
C_{OUT}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	GND
B_{IN}	6	10	8	GND
C_{IN}	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Common	9	13	12	OPEN
D_{IN}	10	14	13	GND
E_{IN}	11	15	14	GND
F_{IN}	12	16	15	GND
D_{OUT}	13	1	17	51 Ω to V_{TT}
E_{OUT}	14	2	18	51 Ω to V_{TT}
F_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

TRUTH TABLE

Inputs		Output
X	Y	OUT
L	L	H
L	H	L
H	L	L
H	H	L

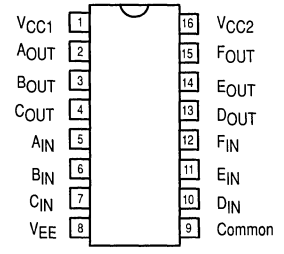
Military 10H589

AVAILABLE AS

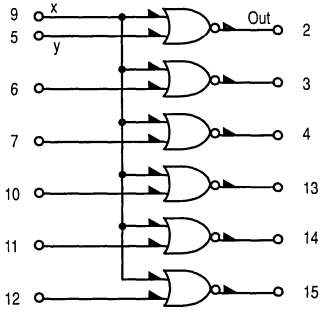
1) JAN: N/A
2) SMD: 5962-8751001
3) 883: 10H589/BXAJC
X = CASE OUTLINE AS FOLLOWS:

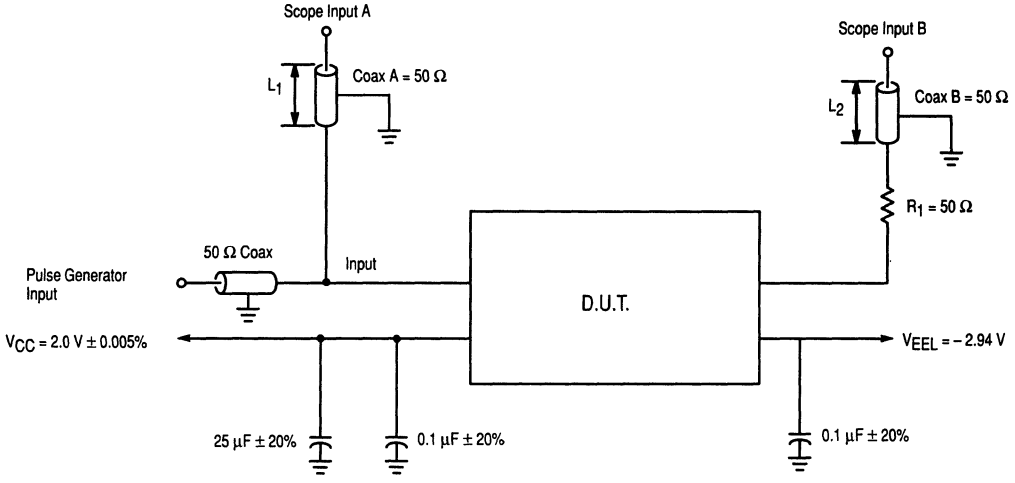
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



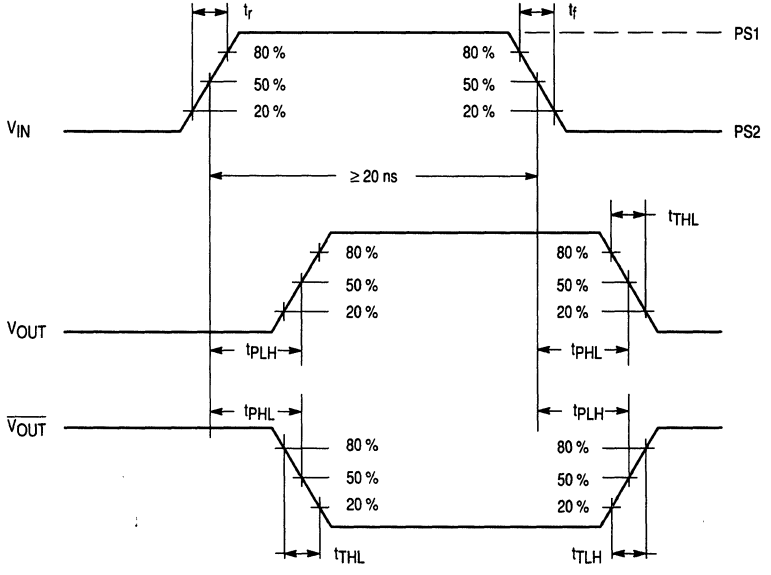
LOGIC DIAGRAM





NOTES

1. Pulse generator must be capable of rise and fall time of 1.0 ns ± 0.1 ms
2. Unused outputs connected to 100 Ω resistor to ground
3. 2:1 divider may be used
4. L1 = L2: matched for equal time delay



NOTES

1. R_1 = 50 Ω in series with a 50 Ω coax constituting the 100 Ω load.
2. $t_r = t_f$ = 1.0 ns ± 0.1 ns.
3. PW ≥ 20 ns
4. f = 1.0 MHz.

Figure 1. Switching Test Circuit and Waveforms

10H589
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to − 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	− 1.01	− 0.78	− 0.86	− 0.65	− 1.06	− 0.84	V		9			8		1, 16	2 - 4, 13 - 15
V_{OL}	Low Output Voltage	− 1.95	− 1.58	− 1.95	− 1.565	− 1.95	− 1.61	V			5 - 7 10 - 12		8		1, 16	2 - 4, 13 - 15
V_{OH1}	High Output Voltage	− 1.01	− 0.78	− 0.86	− 0.65	− 1.06	− 0.84	V				5 - 7 9 - 12	8	8	1, 16	2 - 4, 13 - 15
V_{OL1}	Low Output Voltage	− 1.95	− 1.58	− 1.95	− 1.565	− 1.95	− 1.61	V	9				8	8	1, 16	2 - 4, 13 - 15
I_{EE}	Power Supply Current	− 42		− 46		− 46		mA					8		1, 16	8
I_{IH}	Input Current High		310		495		495	µA	5 - 7 9 - 12				8		1, 16	5 - 7, 9 - 12
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7 9 - 12				8	1, 16	5 - 7, 9 - 12

10H589
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.780	-1.950	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94
T_A = 125 °C	-0.650	-1.950	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94
T_A = -55 °C	-0.840	-1.950	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to – 2.0 V, V_{EEL} = – 2.94 V				
		Subgroup 1		Subgroup 2		Subgroup 3							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	0.7	2.4	0.7	2.4	0.7	2.2	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2, 3, 4, 13, 14, 15
t_{THL}	Fall Time	0.7	2.4	0.7	2.4	0.7	2.2	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2, 3, 4, 13, 14, 15
t_{PLH}	Propagation Delay Data	0.7	1.8	0.7	1.9	0.7	1.9	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2, 3, 4, 13, 14, 15
t_{PHL}	Propagation Delay Data	0.7	1.8	0.7	1.9	0.7	1.9	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2, 3, 4, 13, 14, 15
t_{PHL}	Propagation Delay Enable	0.7	2.5	0.7	2.8	0.7	2.2	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2, 3, 4, 13, 14, 15
t_{PLH}	Propagation Delay Enable	0.7	2.5	0.7	2.8	0.7	2.2	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	1, 16	8	2, 3, 4, 13, 14, 15

Dual 4-5-Input OR/NOR Gate

ELECTRICALLY TESTED PER:
5962-8756901

The 10H609 is a Dual 4-5-input OR/NOR gate.

- Propagation Delay Average, 0.75 ns Typical
- 180 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	OPEN
A_{IN}	6	10	8	OPEN
A_{IN}	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
B_{IN}	9	13	12	GND
B_{IN}	10	14	13	GND
B_{IN}	11	15	14	GND
B_{IN}	12	16	15	OPEN
B_{IN}	13	1	17	CP1
B_{OUT}	14	2	18	51 Ω to V_{TT}
B_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

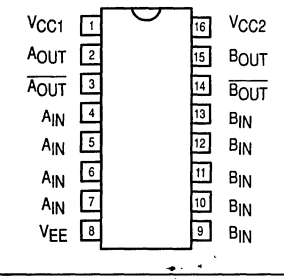
Military 10H609

AVAILABLE AS

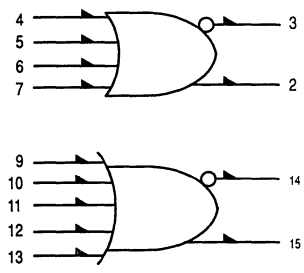
1) JAN: N/A
2) SMD: 5962-8756901
3) 883: 10H609/BXAJC
X = CASE OUTLINE AS FOLLOWS:

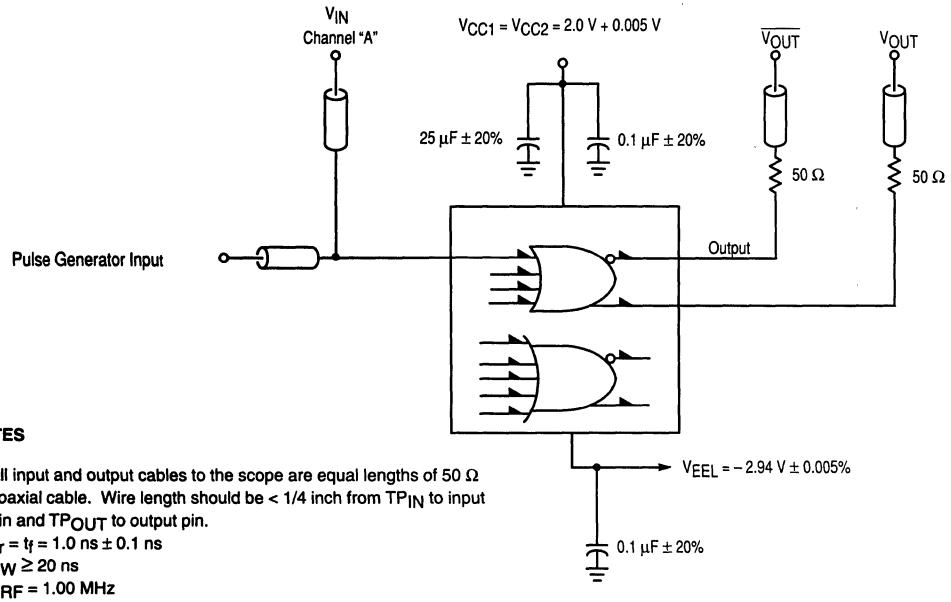
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. $t_r = t_f = 1.0$ ns ± 0.1 ns
3. $P_W \geq 20$ ns
4. $P_{RF} = 1.00$ MHz
5. Unused outputs connected to 100 Ω resistor to ground.

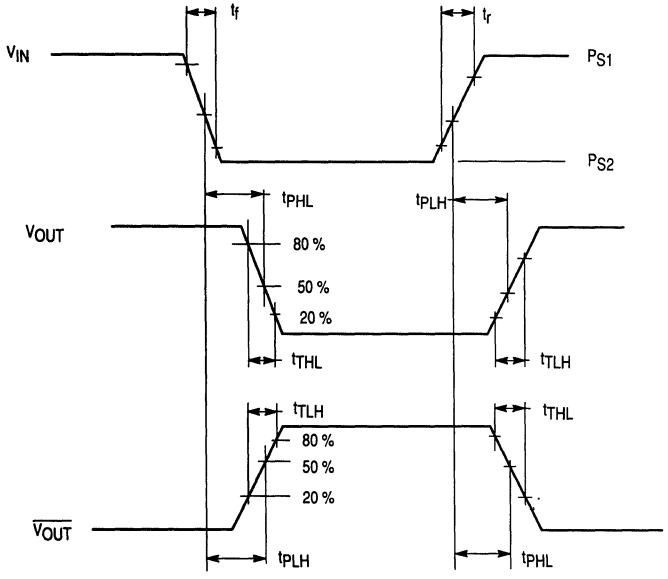


Figure 1. Switching Test Circuit and Waveforms

10H609
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.01	+0.31	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+0.28	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P.U.T.
V_{OH}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	4 - 7 9 - 13	4 - 7 9 - 13			8		1, 16	2, 3, 14, 159
V_{OL}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V			4 - 7 9 - 13	4 - 7 9 - 13	8		1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V			4 - 7 9 - 13	4 - 7 9 - 13	8	8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage	– 1.96	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V	4 - 7 9 - 13	4 - 7 9 - 13		5 - 7 10 - 12	8	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	– 30		– 33		– 33		mA					8		1, 16	8
I_{IH}	Input Current High		350		915		560	μA	4 - 7 9 - 13				8		1, 16	2, 3, 14, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		μA		4 - 7 9 - 13			8		1, 16	2, 3, 14, 15

10H609
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+1.01	+0.28	-5.46	-4.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to – 2.0 V, V_{EEL} = – 2.94 V				
		Subgroup 1		Subgroup 2		Subgroup 3							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.4	1.5	0.4	1.6	0.4	1.3	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	0.4	1.5	0.4	1.6	0.4	1.3	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL}	Propagation Delay Data	0.4	1.4	0.4	1.9	0.4	1.3	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Enable	0.4	1.4	0.4	1.9	0.4	1.3	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15

Dual 3-Input 3-Output "OR" Gate

ELECTRICALLY TESTED PER:
5962-8754101

The 10H610 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the 10H610 particularly useful in clock distribution applications where minimum clock skew is desired.

- Propagation Delay, 1.0 ns Typical
- 230 mW Max/Pkg (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
A_{OUT}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	OPEN
A_{IN}	6	10	8	GND
A_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B_{IN}	9	13	12	OPEN
B_{IN}	10	14	13	OPEN
B_{IN}	11	15	14	GND
B_{OUT}	12	16	15	51 Ω to V_{TT}
B_{OUT}	13	1	17	51 Ω to V_{TT}
B_{OUT}	14	2	18	51 Ω to V_{TT}
V_{CC1}	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

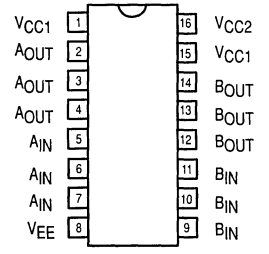
Military 10H610

AVAILABLE AS

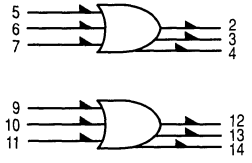
1) JAN: N/A
2) SMD: 5962-8754101
3) 883: 10H610/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

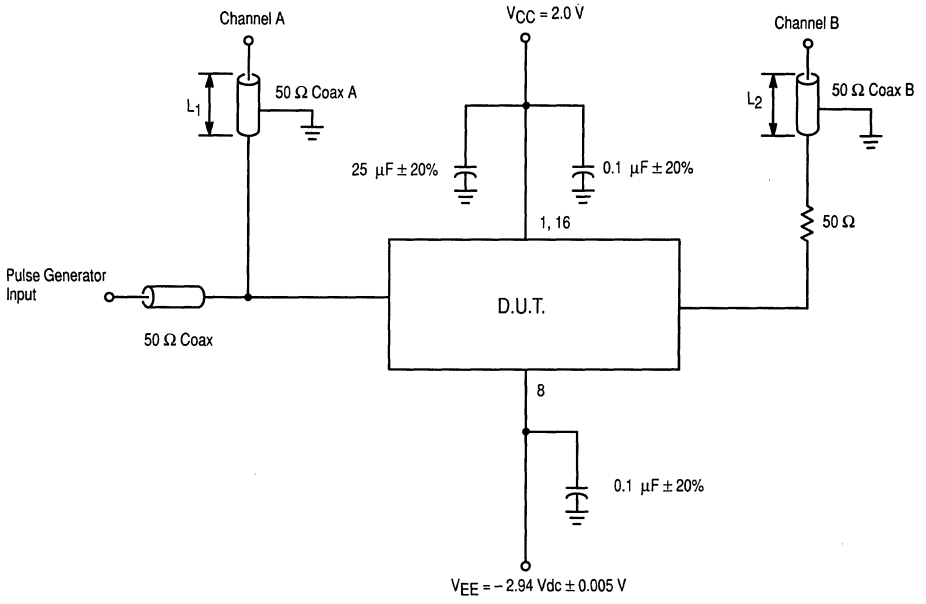
The letter "M" appears before the slash on LCC.

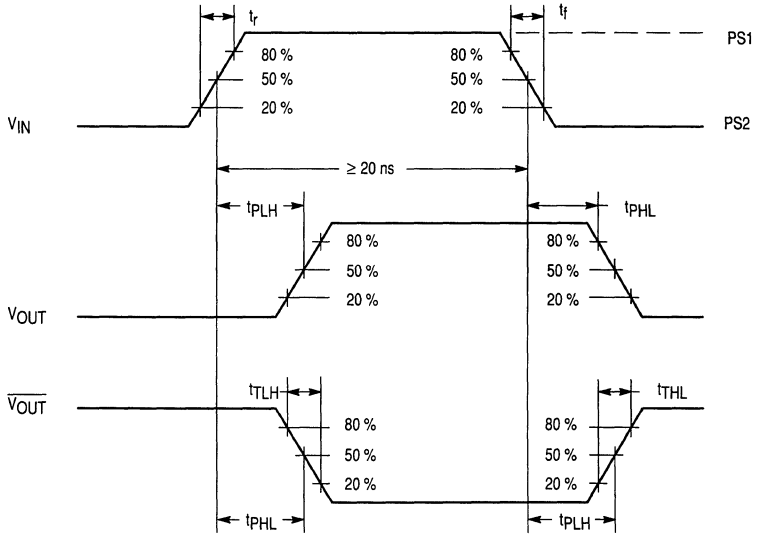


LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8





NOTES

1. All other outputs are loaded 100 Ω to ground.
2. 2:1 divider may be used.
3. L_1: L_2: Matched for equal time delay.
4. V_{IN} = has the following characteristics:
   a. pulse width = ≥ 20 ns.
   b. frequency = 1.0 MHz.
   c. $t_r = t_f$ = 1.0 ns (20% – 80%) + 0.1 ns.

Figure 1. Test Circuit

10H610
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+0.28	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE1}	V_{EE2}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V	5 - 7 9 - 11				8		1, 16, 5	2 - 4, 12 - 14
V_{OL}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V		5 - 7 9 - 11			8		1, 16, 5	2 - 4, 12 - 14
V_{OL1}	Low Output Voltage	– 1.95	– 1.58	– 1.95	– 1.565	– 1.95	– 1.61	V				5 - 7 9 - 11	8	8	1, 16, 5	2 - 4, 12 - 14
V_{OH1}	High Output Voltage	– 1.01	– 0.78	– 0.86	– 0.65	– 1.06	– 0.84	V			5 - 7 9 - 11		8	8	1, 16, 5	2 - 4, 12 - 14
I_{IH1}	Input Current High		450		720		720	µA	5 - 7 9 - 11				8		1, 16, 5	5 - 7, 9 - 11
I_{IL1}	Input Current Low	0.5		0.3		0.5		µA		5 - 7 9 - 11			8		1, 16, 5	5 - 7, 9 - 11
I_{EE}	Power Supply Drain Current	– 38		– 42		– 42		mA					8		1, 16, 5	8

10H610
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EEL}
T_A = 25 °C	-0.78	-1.95	-1.11	-1.480	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.65	-1.95	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = -55 °C	-0.84	-1.95	-1.16	-1.510	+0.28	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 1		Subgroup 2		Subgroup 3							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	0.75	1.8	0.7	1.9	0.65	1.75	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4 , 12 - 14
t_{THL}	Fall Time	0.75	1.8	0.7	1.9	0.65	1.75	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4 , 12 - 14
t_{PLH}	Propagation Delay	0.8	1.65	0.9	1.9	0.75	1.85	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4 , 12 - 14
t_{PHL}	Propagation Delay	0.55	1.7	0.6	1.95	0.5	1.6	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4 , 12 - 14

ECL to TTL Translator (+ 5.0 Vdc Power Supply)

ELECTRICALLY TESTED PER:
MPG 10H750

The 10H750 is a member of Motorola's 10H family of high performance ECL logic. It consists of 4 translator with differential inputs and TTL outputs. The 3-state outputs can be disabled by applying a HIGH TTL logic level on the common OE input.

The 10H750 is designed to be used primarily in systems incorporating both ECL and TTL logic operating off a common power supply. The separate V_{CC} power pins are not connected internally and thus isolate the noisy TTL V_{CC} runs from the relatively quiet ECL V_{CC} runs on the printed circuit board. The differential inputs allow the 10H750 to be used as an inverting or non-inverting translator, a differential line receiver or as a high performance comparator.

- Propagation Delay, 3.5 ns Typical
- MECL 10K-Compatible

	PIN ASSIGNMENTS			
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
ECL V_{CC}	1	5	2	V_{CC}
A_{OUT}	2	6	3	GND
A_{IN}	3	7	4	V_{CC}
$\overline{A_{IN}}$	4	8	5	GND
$\overline{B_{IN}}$	5	9	7	GND
B_{IN}	6	10	8	V_{CC}
B_{OUT}	7	11	9	GND
GND	8	12	10	GND
$\overline{OE}$	9	13	12	GND
D_{OUT}	10	14	13	GND
D_{IN}	11	15	14	V_{CC}
$\overline{D_{IN}}$	12	16	15	GND
$\overline{C_{IN}}$	13	1	17	GND
C_{IN}	14	2	18	V_{CC}
C_{OUT}	15	3	19	GND
TTL V_{CC}	16	4	20	V_{CC}

BURN - IN CONDITIONS:
V_{CC} = + 6.0 V MAX/ + 5.0 V MIN

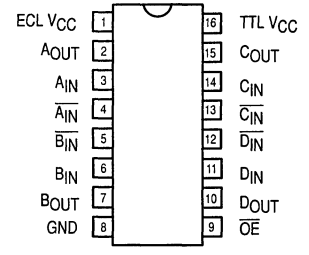
Military 10H750

AVAILABLE AS

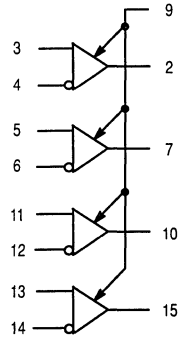
1) JAN: N/A
2) SMD: N/A
3) 883: 10H750/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



V_{CC} (+ 5.0 V) = Pins 1, and 16
GND = Pin 8

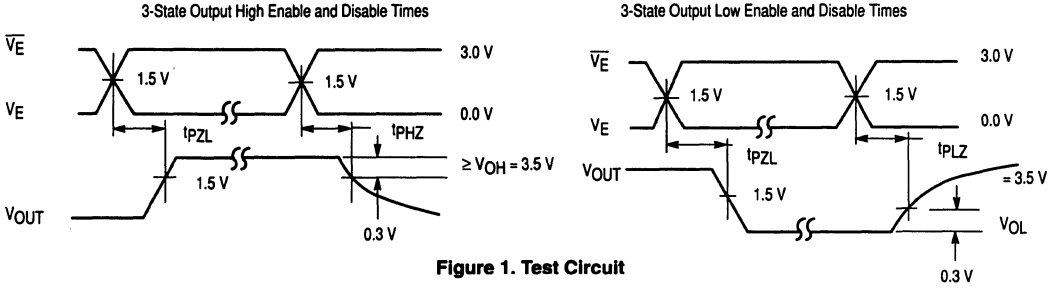


Figure 1. Test Circuit

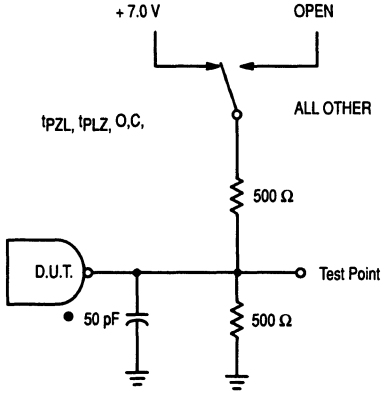


Figure 2. Test Load

• INCLUDES JIG AND PROBE CAPACITANCE

Application Note: Pin 9 is an $\overline{OE}$ and the 10H750 is disabled when $\overline{OE}$ is at V_{IH} or higher

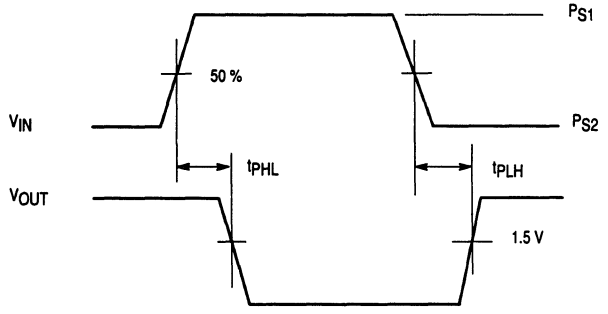


Figure 3. Inverting Waveform Functions

10H750
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts) (V_{DIFF} in milliVolts)															Test Current (milliAmps)	
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{CC}	V_{CC1}	V_{CC2}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_R	$V_{comm.mode}$	V_{DIFF}	I_{OH}	I_{OL}
T_A = 25 °C	+ 2.0	+ 0.8	+ 4.2	+ 3.15	+4.11	+3.31	+ 5.0	+ 5.5	+ 4.5	+ 5.0	+4.65	+3.15	+ 2.8	+3.71	+ 2.8 – + 5.0	+ 350	– 3.0	+ 20
T_A = 125 °C	+ 2.0	+ 0.8	+ 4.2	+ 3.15	+4.22	+3.345	+ 5.0	+ 5.5	+ 4.5	+ 5.0	+4.65	+3.15	+ 2.8	+3.82	+ 2.8 – + 5.0	+ 350	– 3.0	+ 20
T_A = 55 °C	+ 2.0	+ 0.8	+ 4.2	+ 3.15	+4.03	+3.285	+ 5.0	+ 5.5	+ 4.5	+ 5.0	+4.65	+3.15	+ 2.8	+3.63	+ 2.8 – + 5.0	+ 350	– 3.0	+ 20

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC1} & 2 = (Pin 1, 16), GND = (Pin 8), Output Load = See Figure 1.									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IHH}	V_{IHL}	V_{IL}	V_{ILL}	V_{ILH}	V_{CC2}	V_{CC1}	$I_{OH/L}$	P. U. T.
V_{OH}	High Output Voltage	2.5		2.5		2.5		V	3, 6 11, 14	3, 6 11, 14	3, 6 11, 14	4, 5 12, 13	4, 5 12, 13	4, 5 12, 13	1, 16	1, 16	2, 7 10, 15	2, 7 10, 15
V_{OL}	Low Output Voltage		0.5		0.5		0.5	V	2, 3	2	2	3		3	3	8	4	4, 5 12, 13
I_{OZH} I_{OZL}	Output Disable Current (High/ Low)	+ 50 –50		+ 50 –50		+ 50 –50		mA mA	2, 7 10, 15			2, 7 10, 15				1, 16		2, 7 10, 15
I_{CC1} I_{CC2}	Power Supply Current (TTL/ ECL)		20 12		20 12		20 12	mA mA		4, 5 12, 13		9		3, 6 11, 14		1, 16		1, 16
I_{CC}	Input Leakage Current		32		32		32	mA		4, 5 12, 13		9		3, 6 11, 14		1, 16		1, 16
I_{OS}	Short Circuit (**) Current	–60	–150	–60	–150	–60	–150	mA	3, 6 11, 14			4, 5, 9 12, 13				1, 16		2, 7 10, 15
I_{IH}	Input Current		20		20		20	µA	9							1, 16		9
I_{INH}	Input Current		50		50		50	µA		3 – 6 11 – 14				3, 6 11, 14		1, 16		3 – 6 11 – 14
I_{IL}	Input Current		– 0.6		– 0.6		– 0.6	µA				9				1, 16		9
I_{INL}	Input Current		50		50		50	µA		3 – 6 11 – 14				3, 6 11, 14		1, 16		3 – 6 11 – 14

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts. ** For I_{OS}: Pins 2, 7, 10, 15 = GND

10H750
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts) (V_{DIFF} in milliVolts)															Test Current (milliAmps)	
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{CC}	V_{CC1}	V_{CC2}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_R	$V_{comm.mode}$	V_{DIFF}	I_{OH}	I_{OL}
T_A = 25 °C	+ 2.0	+ 0.8	+ 4.2	+ 3.15	+4.11	+3.31	+ 5.0	+ 5.5	+ 4.5	+ 5.0	+4.65	+3.15	+ 2.8	+3.71	+ 2.8 – + 5.0	+ 350	– 3.0	+ 20
T_A = 125 °C	+ 2.0	+ 0.8	+ 4.2	+ 3.15	+4.22	+3.345	+ 5.0	+ 5.5	+ 4.5	+ 5.0	+4.65	+3.15	+ 2.8	+3.82	+ 2.8 – + 5.0	+ 350	– 3.0	+ 20
T_A = – 55 °C	+ 2.0	+ 0.8	+ 4.2	+ 3.15	+4.03	+3.285	+ 5.0	+ 5.5	+ 4.5	+ 5.0	+4.65	+3.15	+ 2.8	+3.63	+ 2.8 – + 5.0	+ 350	– 3.0	+ 20

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{out}	V_{CC}	V_R	P_{S1}	P_{S2}	P.U.T.
t_{pd}	Propagation Delay Data	1.5	5.0	1.5	5.2	1.5	5.0	ns	3, 4, 5 11 - 13	2, 7 10, 15	1, 16	3, 4, 5 11 - 13	3 - 6, 9 11 - 14	3 - 6, 9 11 - 14	2, 7, 10, 15
t_{pdHZ}	Outside Disable Time	2.0	6.0	2.0	6.2	2.0	6.0	ns	3, 4, 5 11 - 13	2, 7 10, 15	1, 16	3, 4, 5 11 - 13	3 - 6, 9 11 - 14	3 - 6, 9 11 - 14	2, 7, 10, 15
t_{pdHZ}	Outside Disable Time	2.0	6.0	2.0	6.2	2.0	6.0	ns	3, 4, 5 11 - 13	2, 7 10, 15	1, 16	3, 4, 5 11 - 13	3 - 6, 9 11 - 14	3 - 6, 9 11 - 14	2, 7, 10, 15
t_{pdZL}	Output Enable Time	2.0	8.0	2.0	8.2	2.0	8.0	ns	3, 4, 5 11 - 13	2, 7 10, 15	1, 16	3, 4, 5 11 - 13	3 - 6, 9 11 - 14	3 - 6, 9 11 - 14	2, 7, 10, 15
t_{pdZH}	Output Enable Time	2.0	8.0	2.0	8.2	2.0	8.0	ns	3, 4, 5 11 - 13	2, 7 10, 15	1, 16	3, 4, 5 11 - 13	3 - 6, 9 11 - 14	3 - 6, 9 11 - 14	2, 7, 10, 15

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Note

Subgroups A10 and A11, (AC testing) at –55°C and +125°C guaranteed, but not tested.

Military 10H751

Advance Information

Quad TTL/NMOS to MECL Translator

ELECTRICALLY TESTED PER:
MPG 10H751

The 10H751 is a quad translator for interfacing data between a saturated logic section and the MECL section of digital systems when only a + 5.0 Vdc power supply is available. The 10H751 has TTL/NMOS complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input at a low logic level, it forces all true outputs to the MECL low logic state (≈ +3.2 V) and all inverting outputs to the MECL high state (≈ + 4.1 V).

The 10H751 can also used with the 10H750 to transmit and receive TTL/NMOS information differentially via balanced twisted pair lines.

- Single + 5.0 V Power Supply
- All V_{CC} Pins Isolated On Chip
- Differentially Drive Balanced Lines
- t_{pd} = 1.3 ns typical

PIN ASSIGNMENTS

FUNCTION	DIL	BURN-IN (CONDITION C)
B_{OUT}	1	GND
$\overline{B_{OUT}}$	2	GND
NC	3	V_{CC}
A_{OUT}	4	GND
$\overline{A_{OUT}}$	5	GND
V_{CC}	6	V_{CC}
B_{IN}	7	GND
A_{IN}	8	GND
Common Strobe	9	GND
GND	10	GND
TTL V_{CC}	11	V_{CC}
D_{IN}	12	GND
NC	13	GND
C_{IN}	14	V_{CC}
V_{CC}^2	15	V_{CC}
$\overline{D_{OUT}}$	16	GND
D_{OUT}	17	GND
$\overline{C_{OUT}}$	18	GND
C_{OUT}	19	GND
TTL V_{CC}	20	V_{CC}

BURN - IN CONDITIONS:
V_{TT} = -2.0 V MAX/ -2.2 V MIN
V_{EE} = -5.7 V MAX/ -5.2 V MIN

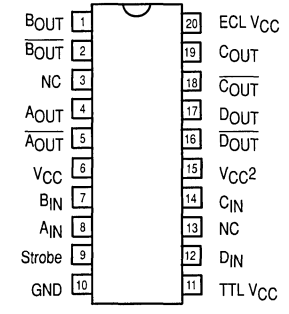
This document contains information on a new product. Specifications and information herein are subject to change without notice.

AVAILABLE AS

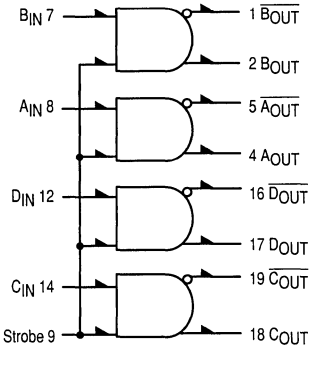
1) JAN: N/A
2) SMD: N/A
3) 883: 10H751/BXAJC
X = CASE OUTLINE AS FOLLOWS:

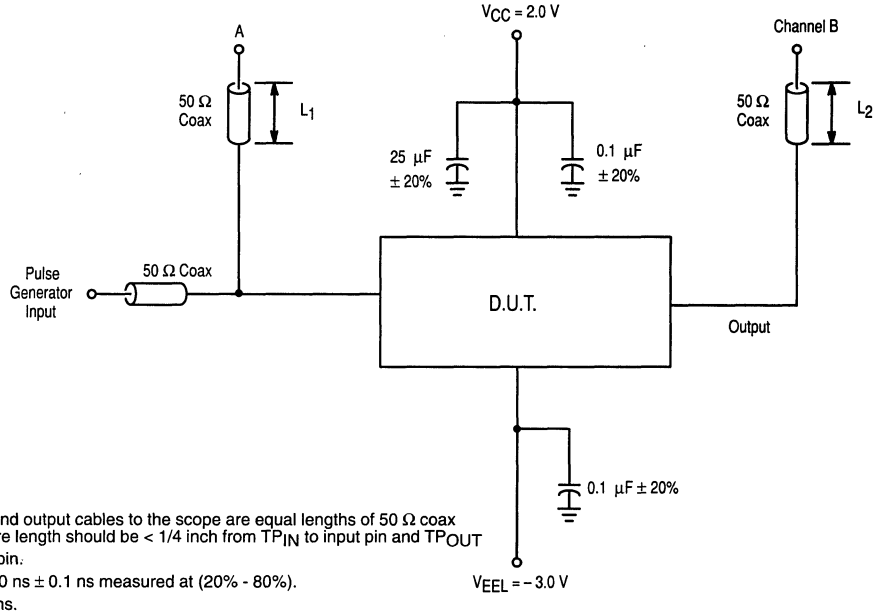
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coax cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. $t_r = t_f = 2.0$ ns ± 0.1 ns measured at (20% - 80%).
3. $P_W \geq 20$ ns.
4. $P_{RF} = 1.0$ MHz.
5. All unused outputs should be loaded 100 Ω to ground.
6. 2:1 divider may be used.
7. $L_1 = L_2$: Matched for equal time delay.

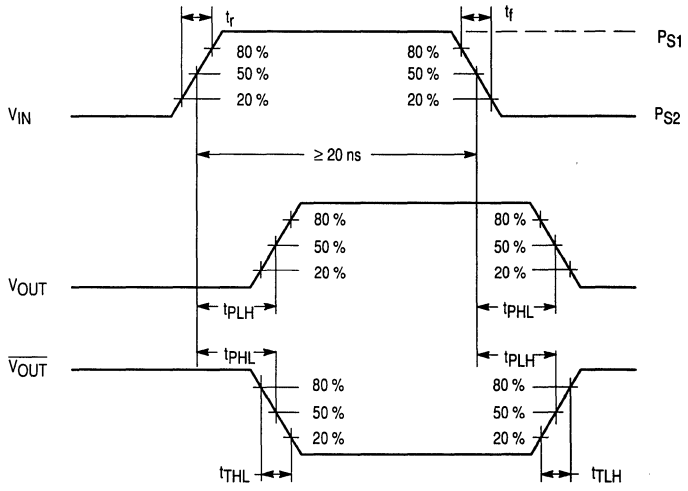


Figure 1. Switching Test Circuit and Waveforms

10H751
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to –2.0 volts.

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{CCL}	V_{CCH}
T_A = 25 °C	+2.7	+0.4	+2.0	+0.8	+5.0	+4.75	+5.25
T_A = 125 °C	+2.7	+0.4	+2.0	+0.8	+5.0	+4.75	+5.25
T_A = - 55 °C	+2.7	+0.4	+2.0	+0.8	+5.0	+4.75	+5.25

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to + 3.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	GND	V_{CC}	V_{CCL}	V_{CCH}	P. U. T.
V_{OH}	High Output Voltage	4.00	4.30	4.08	4.30	3.80	4.20	V	7 - 9, 12, 14			10	6, 11, 15, 20			1, 2, 4, 5, 16 - 19
V_{OL}	Low Output Voltage	3.00	3.40	3.05	3.40	3.05	3.37	V		7 - 9, 12, 14		10	6, 11, 15, 20			1, 2, 4, 5, 16 - 19
V_{OHH}	High Output Voltage	4.27	4.50	4.33	4.60	3.90	4.40	V				10			6, 11, 15, 20	1, 2, 4, 5, 16 - 19
V_{OLL}	Low Output Voltage	3.30	3.80	2.80	3.20	2.80	3.12	V		7 - 9, 12, 14		10		6, 11, 15, 20		1, 2, 4, 5, 16 - 19
V_{OLH}	Low Output Voltage	3.30	3.80	3.30	3.70	3.30	3.62	V				10			6, 11, 15, 20	1, 2, 4, 5, 16 - 19
V_{OHL}	High Output Voltage	3.77	4.20	3.83	4.10	3.50	3.91	V			7 - 9, 12, 14	10		6, 11, 15, 20		1, 2, 4, 5, 16 - 19
I_{CC}	Power Supply Current (ECL)		45		50		50	mA				10	6, 11, 15, 20			20
I_{CC}	Power Supply Current (TTL)		15		20		20	mA				10	6, 11, 15, 20			11
I_{INH1}	Input Current High		20		25		25	µA	7 - 9, 12, 14	7 - 9, 12, 14		10			6, 11, 15, 20	7, 8, 12, 14
I_{INH2}	Input Current High		80		100		100	µA	9	7 - 9, 12, 14		10			6, 11, 15, 20	9
I_{INL1}	Input Current Low		- 0.6		- 0.8		- 0.8	µA		7 - 9, 12, 14		10	7 - 9, 12, 14		6, 11, 15, 20	7, 8, 12, 14
I_{INL2}	Input Current Low		- 2.4		- 3.2		- 3.2	µA		9		10	7, 8, 12, 14		6, 11, 15, 20	9

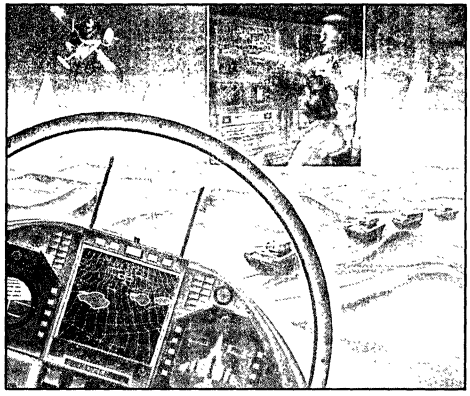
10H751
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to –2.0 volts.

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{CCL}	V_{CCH}
T_A = 25 °C	+2.7	+0.4	+2.0	+0.8	+5.0	+4.75	+5.25
T_A = 125 °C	+2.7	+0.4	+2.0	+0.8	+5.0	+4.75	+5.25
T_A = - 55 °C	+2.7	+0.4	+2.0	+0.8	+5.0	+4.75	+5.25

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW			
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND			
		Subgroup 9		Subgroup 10		Subgroup 11						
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	GND	P.U.T.
t_{TLH}/ t_{TLH}	Rise & Fall Time	0.6	1.7	0.9	1.8	0.5	1.7	ns	7, 8, 12, 14	1, 2, 4, 5, 16, 17, 18, 19	10	1, 2, 4, 5, 16, 17, 18, 19
t_{pd}	Propagation Delay	0.4	2.2	0.3	2.65	0.2	2.2	ns	7, 8, 12, 14	1, 2, 4, 5, 16, 17, 18, 19	10	1, 2, 4, 5, 16, 17, 18, 19



MECL 10K 3

Military 10500

Quad 2-Input NOR Gate with Strobe

ELECTRICALLY TESTED PER:
MPG 10500

The 10500 is a quad 2 input **NOR** gate. Each gate has 3 inputs, two of which are independent and one of which is tied common to all four gates.

- 40 mW Max/Gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10500/BXAJC
X = CASE OUTLINE AS FOLLOWS:

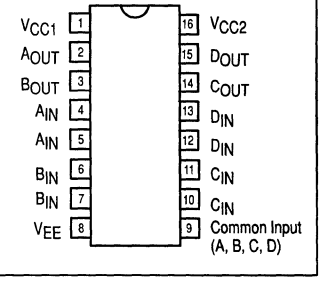
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

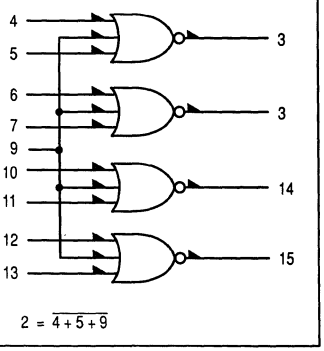
PIN ASSIGNMENTS

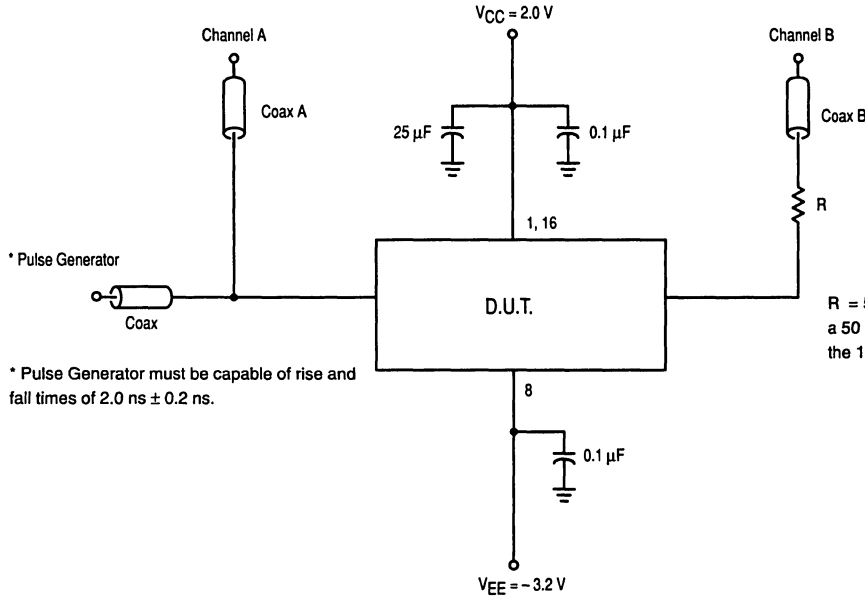
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	OPEN
A_{IN}	5	9	7	OPEN
B_{IN}	6	10	8	OPEN
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
Common Input	9	13	12	OPEN
C_{IN}	10	14	13	OPEN
C_{IN}	11	15	14	OPEN
D_{IN}	12	16	15	OPEN
D_{IN}	13	1	17	OPEN
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM





NOTES
1. Length of $Coax_A$ and $Coax_B$ should be of equal length for equal time delay.
2. Unused outputs should be loaded 100 Ω to ground.
3. 2:1 divider may be used.

NOTES
1. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

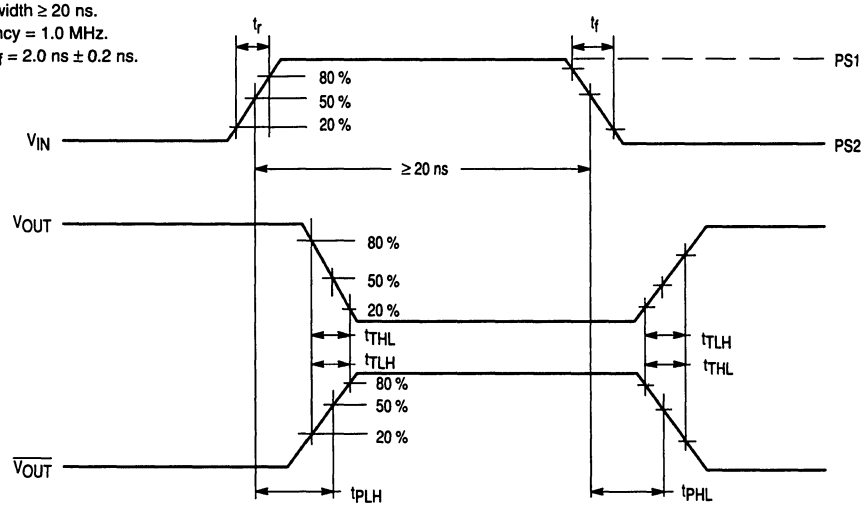


Figure 1. Switching Test Circuit and Waveforms

3

10500
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{CC}	V_{EEL}	V_{EE}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	+2.0	-2.94	-5.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.345	+2.0	-2.94	-5.2
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.03	+0.285	+2.0	-2.94	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	GND	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V		4, 5, 10, 11				8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.565	– 1.92	– 1.655	V	4 - 7, 9 - 13					8	1, 16	2, 3, 14, 15
V_{OHA}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V				4 - 7, 9 - 13		8	1, 16	2, 3, 14, 15
V_{OLA}	Low Output Voltage	– 1.85	– 1.60	– 1.82	– 1.565	– 1.92	– 1.635	V			4 - 7, 9 - 13			8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Drain Current	– 26	– 3.0	– 29	– 3.0	– 29	– 3.0	mA						8	1, 16	8
I_{IH}	Input Current High		245		415		415	µA	4 - 7, 9 - 13					8	1, 16	4 - 7, 10 - 13
I_{IH1}	Input Current High		470		800		800	µA	9					8	1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 13				8	1, 16	4 - 7, 10 - 13

10500
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{CC}	V_{EEL}	V_{EE}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	+2.0	-2.94	-5.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.345	+2.0	-2.94	-5.2
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.03	+0.285	+2.0	-2.94	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	4, 6	2, 3	1, 16	8	2, 3, 14, 15
t_{TLH}	Fall Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	4, 6	2, 3	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High	1.0	2.9	1.0	3.7	1.0	3.7	ns	10, 13	14, 15	1, 16	8	2, 3, 14
t_{PHL}	Propagation Delay High to Low	1.0	2.9	1.0	3.7	1.0	3.7	ns	10, 13	14, 15	1, 16	8	2, 3, 14

Quad OR/NOR Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/06001

The 10501 is a quad 2-input **OR/NOR** gate with one input from each gate common to pin 12.

- 40 mW Max/Gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{A_{OUT}}$	2	6	3	51 Ω to V_{TT}
$\overline{B_{OUT}}$	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	51 Ω to V_{TT}
A_{OUT}	5	9	7	51 Ω to V_{TT}
B_{OUT}	6	10	8	51 Ω to V_{TT}
B_{IN}	7	11	9	51 Ω to V_{TT}
V_{EE}	8	12	10	V_{EE}
D_{OUT}	9	13	12	51 Ω to V_{TT}
C_{IN}	10	14	13	51 Ω to V_{TT}
C_{OUT}	11	15	14	51 Ω to V_{TT}
Common Input	12	16	15	OPEN
D_{IN}	13	1	17	51 Ω to V_{TT}
$\overline{C_{OUT}}$	14	2	18	51 Ω to V_{TT}
$\overline{D_{OUT}}$	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

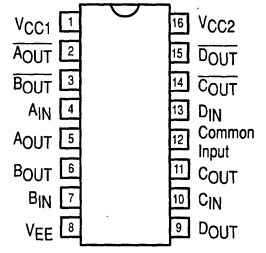
Military 10501

AVAILABLE AS

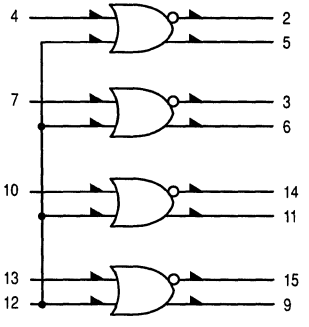
1) JAN: JM 38510/06001
2) SMD: N/A
3) 883: 10501/BXAJC
X = CASE OUTLINE AS FOLLOWS:

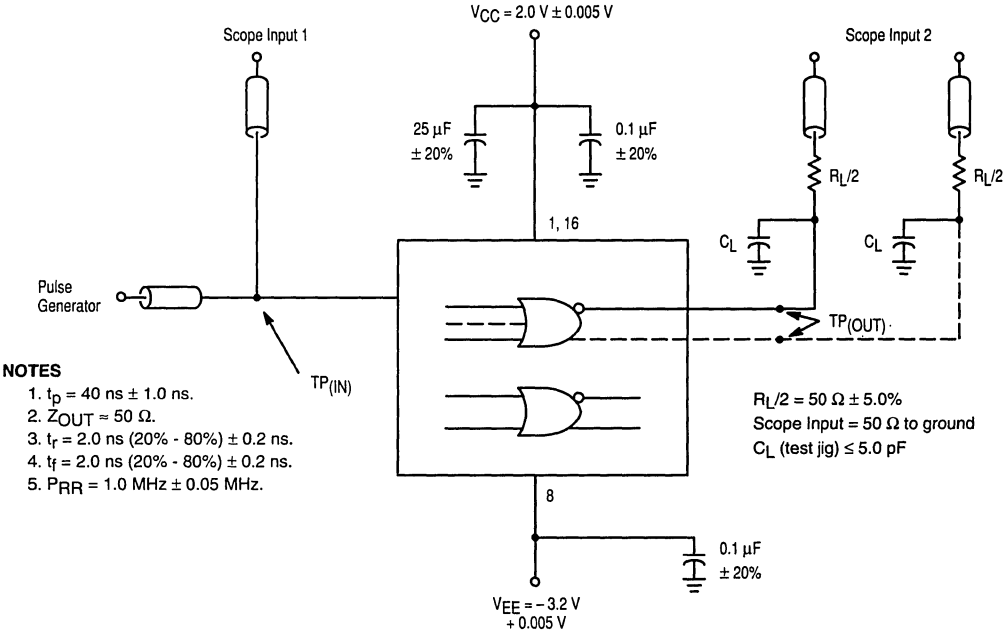
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. t_p = 40 ns ± 1.0 ns.
2. Z_{OUT} ≈ 50 Ω.
3. t_r = 2.0 ns (20% - 80%) ± 0.2 ns.
4. t_f = 2.0 ns (20% - 80%) ± 0.2 ns.
5. P_{RR} = 1.0 MHz ± 0.05 MHz.

NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.

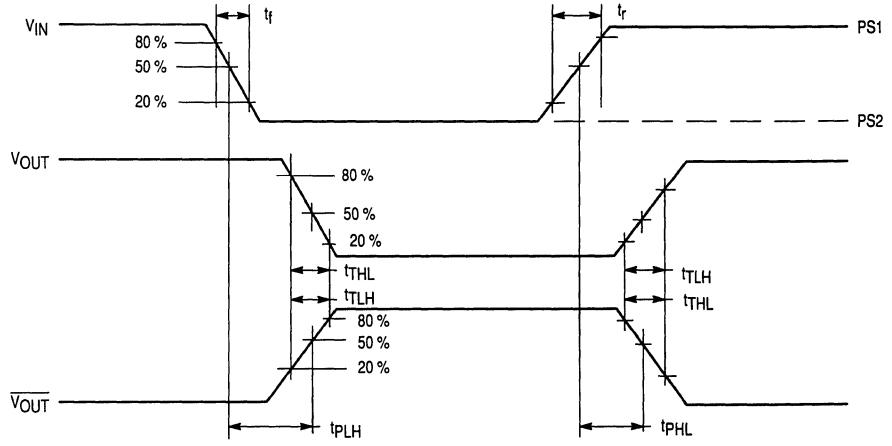


Figure 1. Switching Test Circuit and Waveforms

10501
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	P. U. T.
V_{OH}	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.08	-0.88	V	4, 7, 10 12, 13	4, 7, 10 12, 13			1, 16	8	2, 3, 5, 6, 9, 11 14, 15
V_{OL}	Low Output Voltage	-1.86	-1.62	-1.82	-1.545	-1.92	-1.655	V	4, 7, 10 12, 13	4, 7, 10 12, 13			1, 16	8	2, 3, 5, 6, 9, 11 14, 15
V_{OTH}	High Output Voltage	-0.96		-0.845		-1.1		V			4, 7, 10 12, 13	4, 7, 10 12, 13	1, 16	8	2, 3, 5, 6, 9, 11 14, 15
V_{OTL}	Low Output Voltage		-1.6		-1.525		-1.636	V			4, 7, 10 12, 13	4, 7, 10 12, 13	1, 16	8	2, 3, 5, 6, 9, 11 14, 15
I_{EE}	Power Supply Current	-26		-29		-29		mA					1, 16	8	8
I_{IH}	Input Current High		265		450		450	µA	4, 7, 10, 13				1, 16	8	4, 7, 10, 13
I_{IH1}	Input Current High		550		935		935	µA	12				1, 16	8	12
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4, 7, 10 12, 13			1, 16	8	4, 7, 10, 13

10501
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	+2.0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	+2.0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	+2.0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+ 25° C		+ 125 ° C		- 55 ° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	4, 7, 10, 13	2, 3, 5, 6, 9 11, 14, 15	1, 16	8	2, 3, 5, 6, 9, 11, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	4, 7, 10, 13	2, 3, 5, 6, 9 11, 14, 15	1, 16	8	2, 3, 5, 6, 9, 11, 14, 15
t_{PLH}	Propaganda Delay Low to High	1.0	2.9	1.0	3.7	1.0	3.7	ns	4, 7, 10, 13	2, 3, 5, 6, 9 11, 14, 15	1, 16	8	2, 3, 5, 6, 9, 11, 14, 15
t_{PHL}	Propaganda Delay High to Low	1.0	2.9	1.0	3.7	1.0	3.7	ns	4, 7, 10, 13	2, 3, 5, 6, 9 11, 14, 15	1, 16	8	2, 3, 5, 6, 9, 11, 14, 15

Quad 2-Input NOR Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/06002

The 10502 is a quad 2-input **NOR** gate.The 10502 provides one gate with **OR/NOR** outputs.

- 40 mW Max/Gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	51 Ω to V_{TT}
B_{IN}	6	10	8	51 Ω to V_{TT}
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$\overline{D_{OUT}}$	9	13	12	51 Ω to V_{TT}
C_{IN}	10	14	13	51 Ω to V_{TT}
C_{IN}	11	15	14	OPEN
D_{IN}	12	16	15	51 Ω to V_{TT}
D_{IN}	13	1	17	OPEN
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

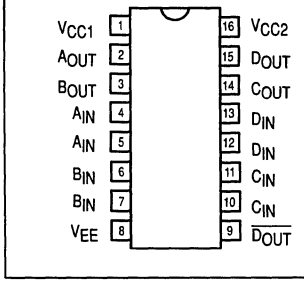
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

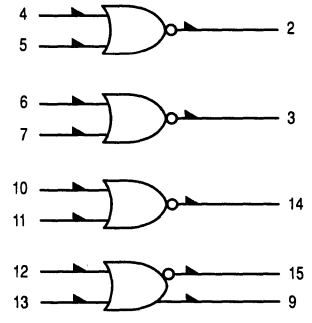
1) JAN: JM 38510/06002
2) SMD: N/A
3) 883: 10502/BXAJC
X = CASE OUTLINE AS FOLLOWS:

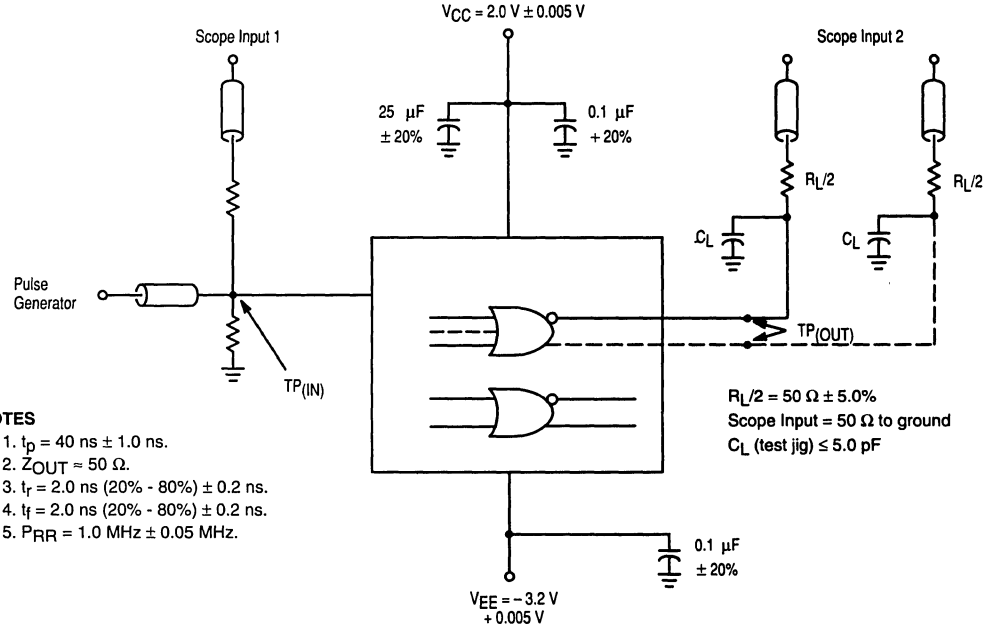
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. t_p = 40 ns ± 1.0 ns.
2. $Z_{OUT} \approx 50\ \Omega$.
3. t_r = 2.0 ns (20% - 80%) ± 0.2 ns.
4. t_f = 2.0 ns (20% - 80%) ± 0.2 ns.
5. P_{RR} = 1.0 MHz ± 0.05 MHz.

NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.

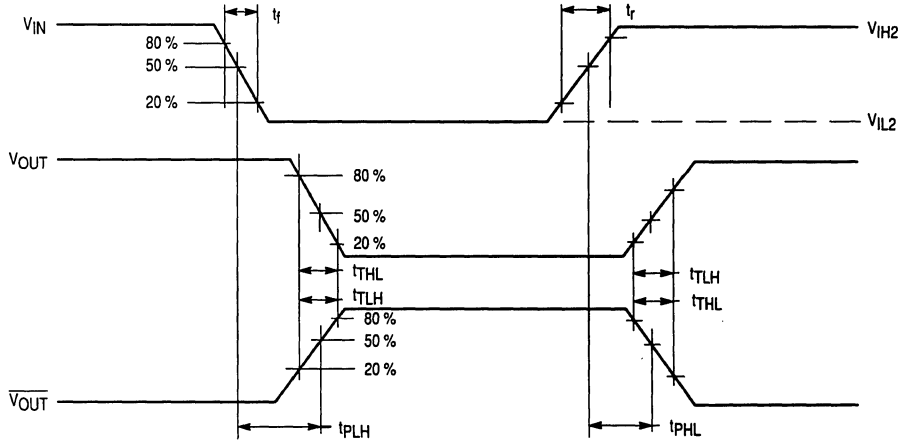


Figure 1. Switching Test Circuit and Waveforms

10502
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C Subgroup 1		+ 125 °C Subgroup 2		- 55 °C Subgroup 3			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	P. U. T.
V_{OH}	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.08	-0.88	V	12, 13	4 - 7 10 - 13			1, 16	8	2, 3, 9, 14, 15
V_{OL}	Low Output Voltage	-1.86	-1.62	-1.82	-1.545	-1.92	-1.655	V	4 - 7 10 - 13	12, 13			1, 16	8	2, 3, 9, 14, 15
V_{OTH}	High Output Voltage	-0.96		-0.845		-1.1		V			4 - 7 10 - 13	12, 13	1, 16	8	2, 3, 9, 14, 15
V_{OTL}	Low Output Voltage		-1.6		-1.525		-1.636	V			12, 13	4 - 7 10 - 13	1, 16	8	2, 3, 9, 14, 15
I_{EE}	Power Supply Current	-26		-29		-29		mA					1, 16	8	8
I_{IH}	Input Current High		265		450		450	µA	4 - 7 10 - 13				1, 16	8	4 - 7, 10 - 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7 10 - 13			1, 16	8	4 - 7, 10 - 13

10502
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	+2.0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	+2.0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	+2.0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+ 25° C		+ 125 ° C		- 55 ° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	5, 7, 11, 13	2, 3, 9 14, 15	1, 16	8	2, 3, 9, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	5, 7, 11, 13	2, 3, 9 14, 15	1, 16	8	2, 3, 9, 14, 15
t_{PLH}	Propaganda Delay Low to High	1.0	2.9	1.0	3.7	1.0	3.7	ns	5, 7, 11, 13	2, 3, 9 14, 15	1, 16	8	2, 3, 9, 14, 15
t_{PHL}	Propaganda Delay High to Low	1.0	2.9	1.0	3.7	1.0	3.7	ns	5, 7, 11, 13	2, 3, 9 14, 15	1, 16	8	2, 3, 9, 14, 15

Quad 2-Input OR Gate

ELECTRICALLY TESTED PER:
MPG 10503

The 10503 is a quad 2 input **OR** gate. The 10503 provides one gate with **OR/NOR** outputs.

- 40 mW Max/Gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	GND
A_{IN}	5	9	7	OPEN
B_{IN}	6	10	8	GND
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$\overline{C_{OUT}}$	9	13	12	51 Ω to V_{TT}
D_{IN}	10	14	13	GND
D_{IN}	11	15	14	OPEN
C_{IN}	12	16	15	GND
C_{IN}	13	1	17	OPEN
D_{OUT}	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

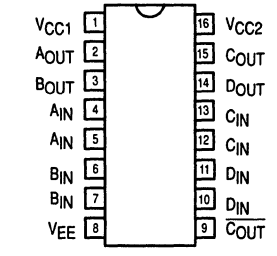
Military 10503

AVAILABLE AS

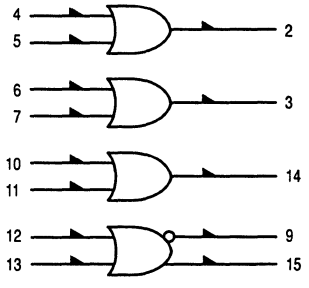
1) JAN: N/A
2) SMD: N/A
3) 883: 10503/BXAJC
X = CASE OUTLINE AS FOLLOWS:

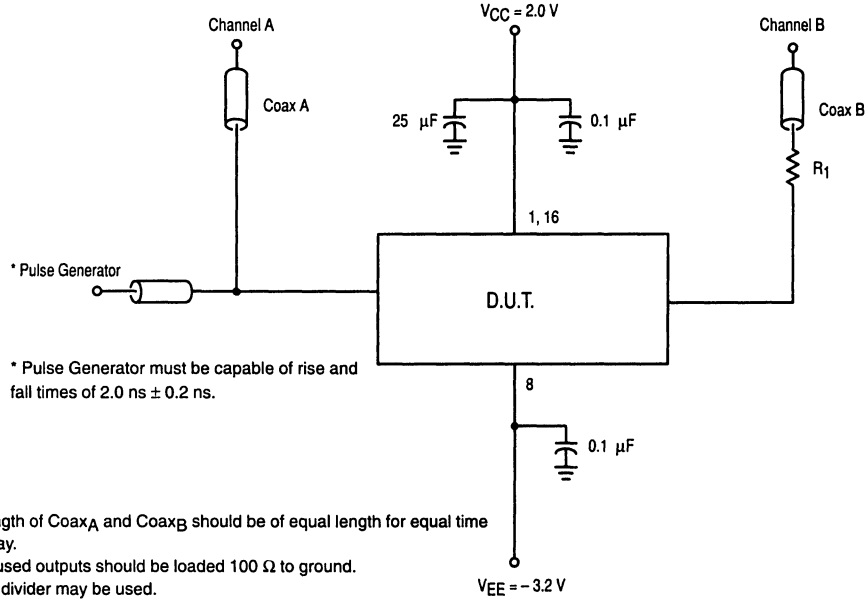
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





* Pulse Generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.

NOTES

1. Length of $Coax_A$ and $Coax_B$ should be of equal length for equal time delay.
2. Unused outputs should be loaded 100 Ω to ground.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 2.0 ns (20%-80%) ± 0.2 ns.
5. R_1 = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.

NOTES

1. V_{IN} has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

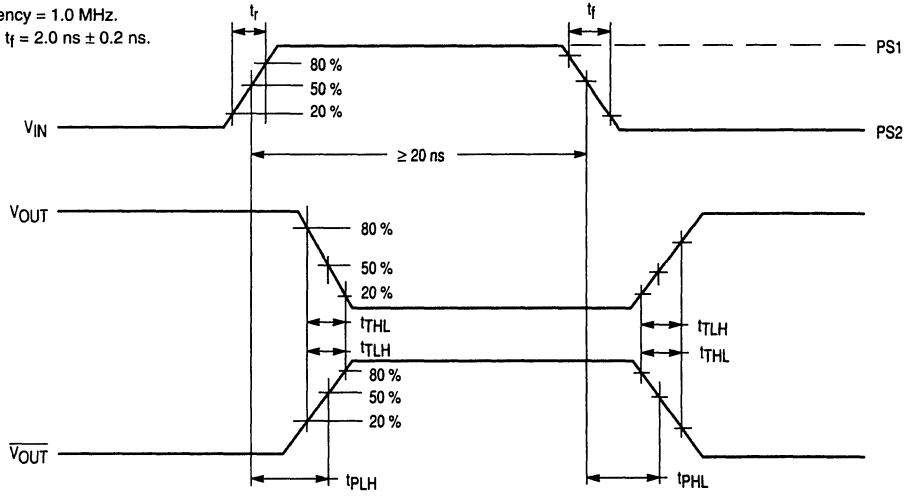


Figure 1. Switching Test Circuit and Waveforms

10503
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{CC}	V_{EEL}	V_{EE}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	0	-3.2	-5.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	0	-3.2	-5.2
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	0	-3.2	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to − 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	− 0.93	− 0.78	− 0.825	− 0.63	− 1.08	− 0.88	V	4 - 7, 10 - 13				8	1, 16	2, 3, 9, 14, 15
V_{OL}	Low Output Voltage	− 1.85	− 1.62	− 1.82	− 1.545	− 1.92	− 1.655	V	12, 13				8	1, 16	2, 3, 9, 14, 15
V_{OHA}	High Output Voltage	− 0.95	− 0.78	− 0.845	− 0.63	− 1.1	− 0.88	V			4 - 7, 10 - 13	12, 13	8	1, 16	2, 3, 9, 14, 15
V_{OLA}	Low Output Voltage	− 1.85	− 1.6	− 1.82	− 1.525	− 1.92	− 1.635	V			12, 13	4 - 7, 10 - 13	8	1, 16	2, 3, 9, 14, 15
I_{EE}	Power Supply Drain Current	− 26		− 29		− 29		mA					8	1, 16	8
I_{IH}	Input Current High		245		415		415	μA	4 - 7, 10 - 13				8	1, 16	4 - 7, 10 - 13
I_{IL}	Input Current Low	0.5		0.3		0.5		μA		4 - 7, 10 - 13			8	1, 16	4 - 7, 10 - 13

10503
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{CC}	V_{EEL}	V_{EE}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	+2.0	-3.2	-5.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	+2.0	-3.2	-5.2
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	+2.0	-3.2	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.1	4.0	1.1	4.0	ns	5, 7 11, 13	2, 3, 9, 14, 15	1, 16	8	2, 3, 9, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.1	4.0	1.1	4.0	ns	5, 7 11, 13	2, 3, 9, 14, 15	1, 16	8	2, 3, 9, 14, 15
t_{PLH}	Propagation Delay Low to High	1.0	2.9	1.0	3.7	1.0	3.7	ns	5, 7 11, 13	2, 3, 9, 14, 15	1, 16	8	2, 3, 9, 14, 15
t_{PHL}	Propagation Delay High to Low	1.0	2.9	1.0	3.7	1.0	3.7	ns	5, 7 11, 13	2, 3, 9, 14, 15	1, 16	8	2, 3, 9, 14, 15

Quad 2-Input AND Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/06201

The 10504 is a quad 2 input **AND** gate. One of the gates has **AND/NAND** outputs available.

- 50 mW Max/Gate (No Load)
- t_{pd} = 2.7 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	GND
A_{IN}	5	9	7	GND
B_{IN}	6	10	8	GND
B_{IN}	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
$\overline{D_{OUT}}$	9	13	12	51 Ω to V_{TT}
C_{IN}	10	14	13	GND
C_{IN}	11	15	14	GND
D_{IN}	12	16	15	GND
D_{IN}	13	1	17	GND
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

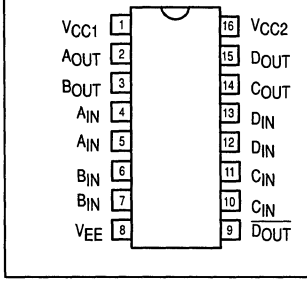
Military 10504

AVAILABLE AS

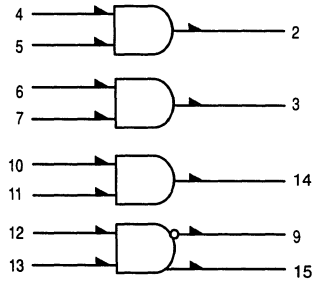
1) JAN: JM 38510/06201
2) SMD: N/A
3) 883: 10504/BXAJC
X = CASE OUTLINE AS FOLLOWS:

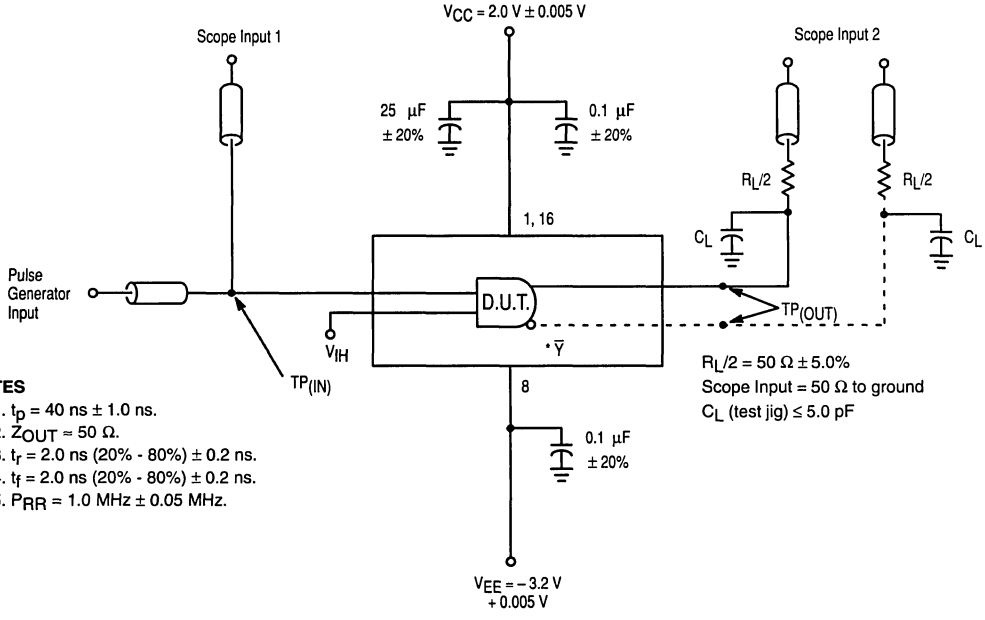
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. t_p = 40 ns ± 1.0 ns.
2. $Z_{OUT} \approx 50\ \Omega$.
3. t_r = 2.0 ns (20% - 80%) ± 0.2 ns.
4. t_f = 2.0 ns (20% - 80%) ± 0.2 ns.
5. P_{RR} = 1.0 MHz ± 0.05 MHz.

NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. *($\overline{Y}$) applies to gate 4 only.

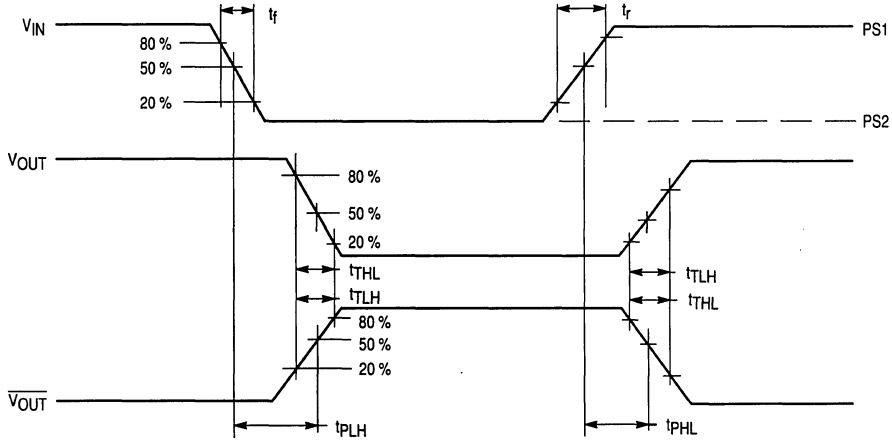


Figure 1. Switching Test Circuit and Waveforms

10504
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	V_{EE1}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	4 - 7, 10 - 13				8	1, 16	2, 3, 9, 14, 15
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.545	– 1.92	– 1.655	V	4 - 7, 10 - 13				8	1, 16	2, 3, 9, 14, 15
V_{OTH}	High Output Voltage	– 0.95		– 0.845		– 1.1		V	4 - 7, 10 - 13			4 - 7, 10 - 13	8	1, 16	2, 3, 9, 14, 15
V_{OTL}	Low Output Voltage		– 1.6		– 1.525		– 1.635	V	4 - 7, 10 - 13		4 - 7, 10 - 13		8	1, 16	2, 3, 9, 14, 15
I_{EE}	Power Supply Drain Current	– 35		– 39		– 39		mA					8	1, 16	8
I_{IH1}	Input Current High		265		450		450	µA	4 - 7, 10 - 13				8	1, 16	4 - 7, 10 - 13
I_{IH}	Input Current High		220		375		375	µA	5, 6, 11, 12				8	1, 16	5, 6, 11, 12
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 10 - 13			8	1, 16	4 - 7, 10 - 13

10504
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	2.0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	2.0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	2.0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IH2}	V_{IN}	V_{OUT}	V_{CC}	V_{EE2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.5	1.0	4.1	1.0	3.8	ns	4 - 7, 10 - 13	4 - 7, 10 - 13	2, 3, 9, 14, 15	1, 16	8	2, 3, 9, 14, 15
t_{THL}	Fall Time	1.1	3.5	1.0	4.1	1.0	3.8	ns	4 - 7, 10 - 13	4 - 7, 10 - 13	2, 3, 9, 14, 15	1, 16	8	2, 3, 9, 14, 15
t_{PLH}	Propagation Delay Low to High	1.0	4.0	1.0	4.7	1.0	4.3	ns	4 - 7, 10 - 13	4 - 7, 10 - 13	2, 3, 9, 14, 15	1, 16	8	2, 3, 9, 14, 15
t_{PHL}	Propagation Delay High to Low	1.0	4.0	1.0	4.7	1.0	4.3	ns	4 - 7, 10 - 13	4 - 7, 10 - 13	2, 3, 9, 14, 15	1, 16	8	2, 3, 9, 14, 15

Triple 2-3-2 OR/NOR Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/06003

The 10505 is a triple 2-3-2 input **OR/NOR** gate.

- 35 mW Max/Gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	OPEN
A_{IN}	5	9	7	51 Ω to V_{TT}
$\overline{B_{OUT}}$	6	10	8	51 Ω to V_{TT}
B_{OUT}	7	11	9	51 Ω to V_{TT}
V_{EE}	8	12	10	V_{EE}
B_{IN}	9	13	12	51 Ω to V_{TT}
B_{IN}	10	14	13	OPEN
B_{IN}	11	15	14	OPEN
C_{IN}	12	16	15	OPEN
C_{IN}	13	1	17	51 Ω to V_{TT}
$\overline{C_{OUT}}$	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

3

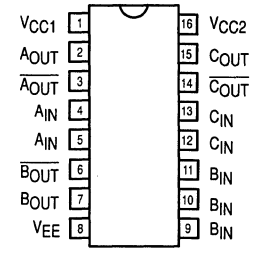
Military 10505

AVAILABLE AS

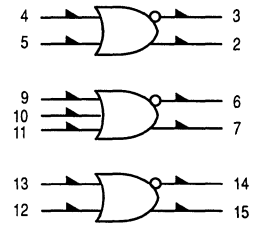
1) JAN: JM 38510/06003
2) SMD: N/A
3) 883: 10505/BXAJC
X = CASE OUTLINE AS FOLLOWS:

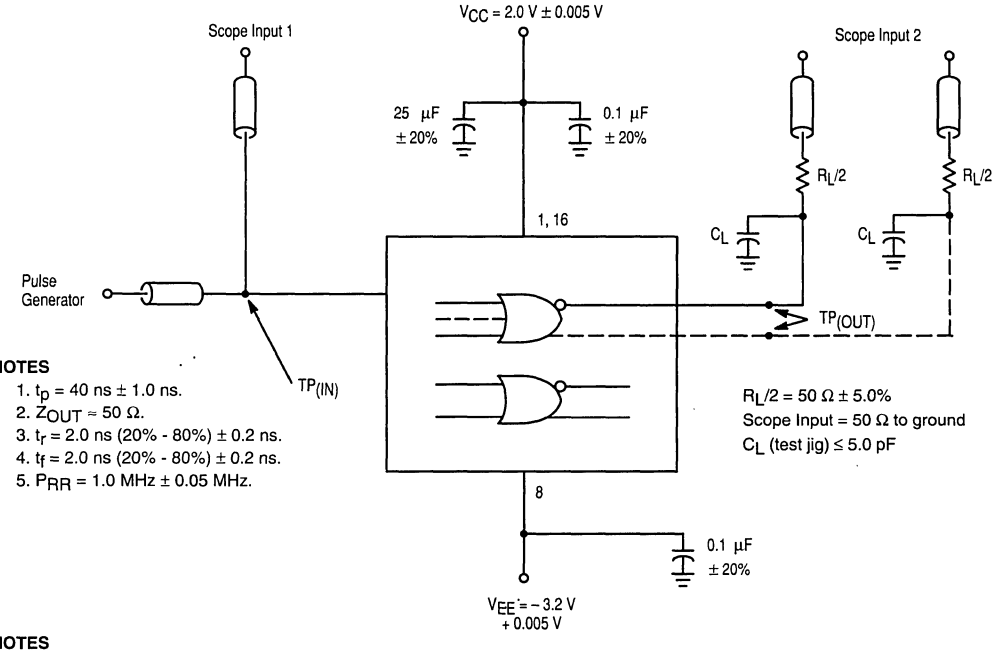
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. t_p = 40 ns ± 1.0 ns.
2. $Z_{OUT} \approx$ 50 Ω.
3. t_r = 2.0 ns (20% - 80%) ± 0.2 ns.
4. t_f = 2.0 ns (20% - 80%) ± 0.2 ns.
5. P_{RR} = 1.0 MHz ± 0.05 MHz.

NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.

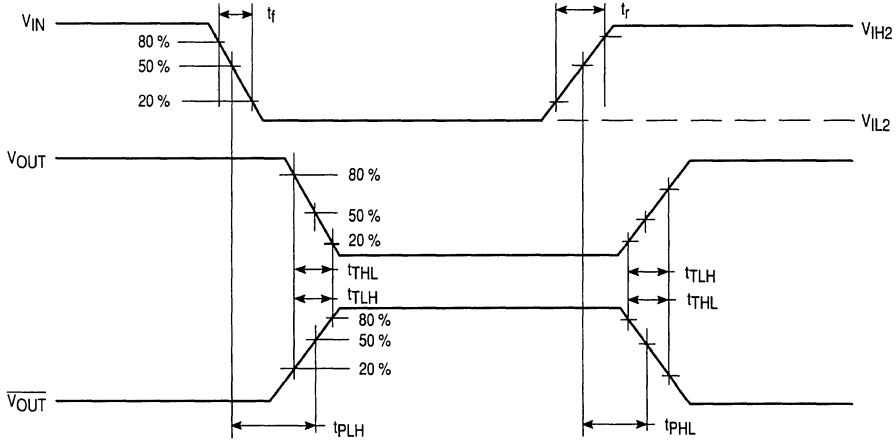


Figure 1. Switching Test Circuit and Waveforms

10505
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	P. U. T.
V_{OH}	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.08	-0.88	V	4, 5, 9 - 13	4, 5, 9 - 13			1, 16	8	2, 3, 6, 7 14, 15
V_{OL}	Low Output Voltage	-1.86	-1.62	-1.82	-1.545	-1.92	-1.655	V	4, 5, 9 - 13	4, 5, 9 - 13			1, 16	8	2, 3, 6, 7 14, 15
V_{OTH}	High Output Voltage	-0.95		-0.85		-1.1		V			4, 5, 9 - 13	4, 5, 9 - 13	1, 16	8	2, 3, 6, 7 14, 15
V_{OTL}	Low Output Voltage		-1.6		-1.525		-1.636	V			4, 5, 9 - 13	4, 5, 9 - 13	1, 16	8	2, 3, 6, 7 14, 15
I_{EE}	Power Supply Current	-21		-24		-24		mA					1, 16	8	8
I_{IH}	Input Current High		265		450		450	µA	4, 5, 9 - 13				1, 16	8	4, 5, 9 - 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4, 5, 9 - 13			1, 16	8	4, 5, 9 - 13

10505
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	+2.0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	+2.0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	+2.0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+ 25° C		+ 125 ° C		- 55 ° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	4, 9, 12	2, 3, 6, 7 14, 15	1, 16	8	2, 3, 6, 7, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	4, 9, 12	2, 3, 6, 7 14, 15	1, 16	8	2, 3, 6, 7, 14, 15
t_{PLH}	Propaganda Delay Low to High	1.0	2.9	1.0	3.7	1.0	3.7	ns	4, 9, 12	2, 3, 6, 7 14, 15	1, 16	8	2, 3, 6, 7, 14, 15
t_{PHL}	Propaganda Delay High to Low	1.0	2.9	1.0	3.7	1.0	3.7	ns	4, 9, 12	2, 3, 6, 7 14, 15	1, 16	8	2, 3, 6, 7, 14, 15

Triple 4-3-3 Input NOR Gate

Military 10506

ELECTRICALLY TESTED PER:
MIL-M-38510/06004

The 10506 is a triple 4-3-3 input NOR gate.

- 35 mW Max/Gate (No Load)
- t_{pd} = 2.8 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
B_{OUT}	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	OPEN
A_{IN}	6	10	8	OPEN
A_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B_{IN}	9	13	12	OPEN
B_{IN}	10	14	13	51 Ω to V_{TT}
B_{IN}	11	15	14	OPEN
C_{IN}	12	16	15	OPEN
C_{IN}	13	1	17	OPEN
C_{IN}	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

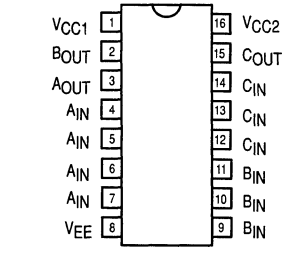
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

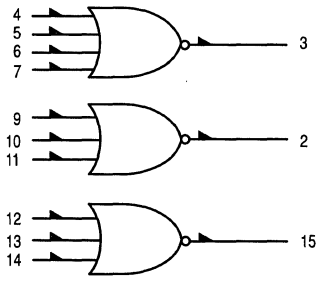
1) JAN: JM 38510/06004
2) SMD: N/A
3) 883: 10506/BXAJC
X = CASE OUTLINE AS FOLLOWS:

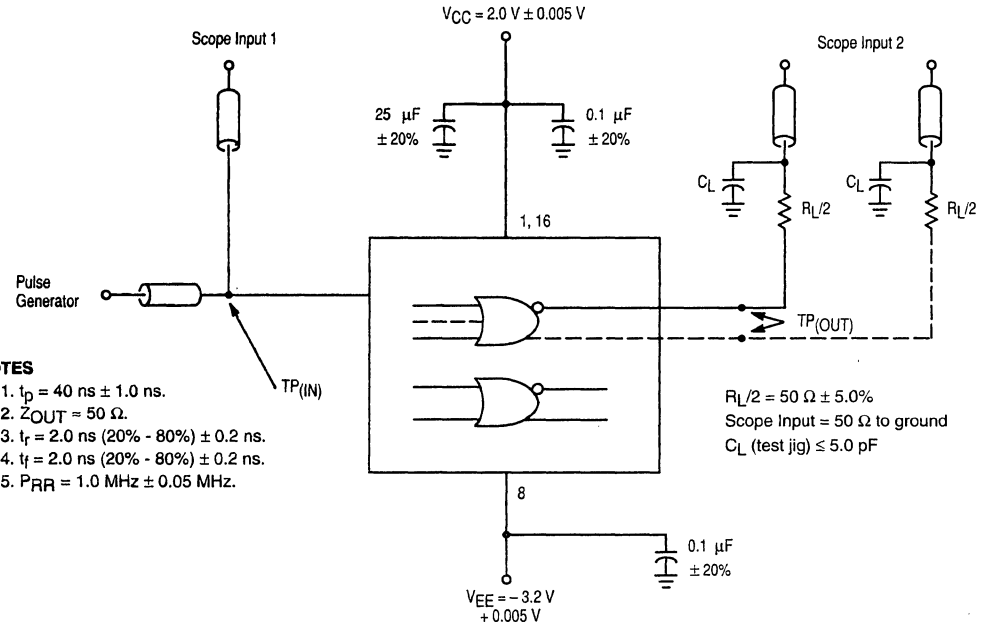
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. t_p = 40 ns ± 1.0 ns.
2. $Z_{OUT} \approx 50\ \Omega$.
3. t_r = 2.0 ns (20% - 80%) ± 0.2 ns.
4. t_f = 2.0 ns (20% - 80%) ± 0.2 ns.
5. P_{RR} = 1.0 MHz ± 0.05 MHz.

$R_L/2 = 50\ \Omega \pm 5.0\%$
Scope Input = 50 Ω to ground
C_L (test jig) ≤ 5.0 pF

NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.

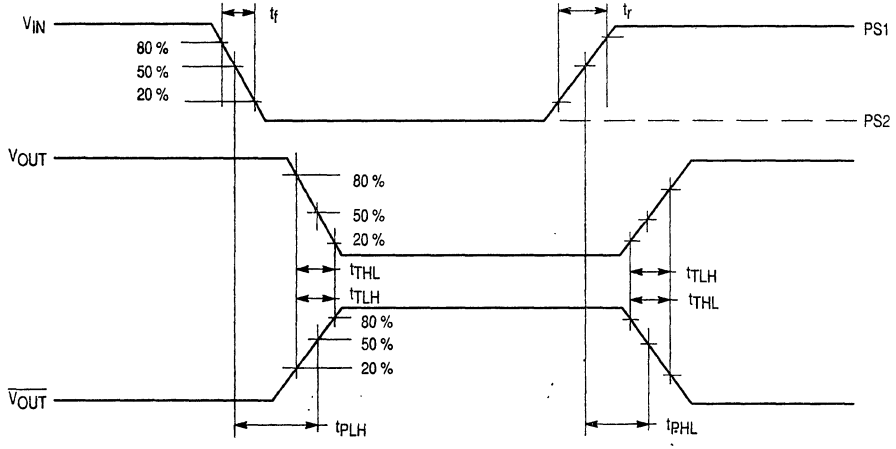


Figure 1. Switching Test Circuit and Waveforms

10506
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	+2.0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	+2.0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	+2.0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C Subgroup 1		+ 125 °C Subgroup 2		- 55 °C Subgroup 3			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	P. U. T.
V_{OH}	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.08	-0.88	V		4 - 7, 9 - 14			1, 16	8	2, 3, 15
V_{OL}	Low Output Voltage	-1.86	-1.62	-1.82	-1.545	-1.92	-1.656	V	4 - 7, 9 - 14				1, 16	8	2, 3, 15
V_{OTH}	High Output Voltage	-0.95		-0.845		-1.1		V			4 - 7, 9 - 14		1, 16	8	2, 3, 15
V_{OTL}	Low Output Voltage		-1.6		-1.525		-1.636	V				4 - 7, 9 - 14	1, 16	8	2, 3, 15
I_{EE}	Power Supply Current	-21		-24		-24		mA					1, 16	8	8
I_{IH}	Input Current High		265		450		450	µA	4 - 7, 9 - 14				1, 16	8	4 - 7, 9 - 14
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 14			1, 16	8	4 - 7, 9 - 14

10506
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	+2.0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	+2.0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	+2.0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+ 25° C Subgroup 9		+ 125 ° C Subgroup 10		- 55 ° C Subgroup 11			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	6, 10 12	2, 3, 15	1, 16	8	2, 3, 15
t_{THL}	Fall Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	6, 10	2, 3, 15	1, 16	8	2, 3, 15
t_{PLH}	Propaganda Delay Low to High	1.0	2.9	1.0	3.7	1.0	3.7	ns	6, 10	2, 3, 15	1, 16	8	2, 3, 15
t_{PHL}	Propaganda Delay High to Low	1.0	2.9	1.0	3.7	1.0	3.7	ns	6, 10	2, 3, 15	1, 16	8	2, 3, 15

Triple 2 Input Exclusive "OR"/Exclusive "NOR" Gate

Military 10507

ELECTRICALLY TESTED PER:
MIL-M-38510/06005

The 10507 is a triple 2 input exclusive **OR/NOR** gate.

- 40 mW Max/Gate (No Load)
- t_{pd} = 2.8 ns typ
- t_r, t_f = 2.5 ns typ (20% - 80%)

AVAILABLE AS

1) JAN: JM 38510/06005
2) SMD: N/A
3) 883: 10507/BXAJC
X = CASE OUTLINE AS FOLLOWS:

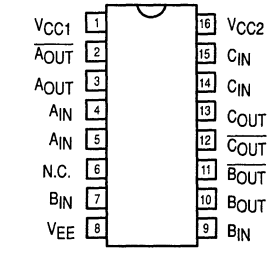
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

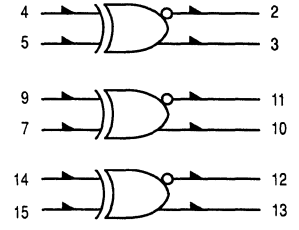
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{A_{OUT}}$	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	GND
A_{IN}	5	9	7	OPEN
N.C.	6	10	8	OPEN
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{CC}
B_{IN}	9	13	12	GND
B_{OUT}	10	14	13	51 Ω to V_{TT}
$\overline{B_{OUT}}$	11	15	14	51 Ω to V_{TT}
$\overline{C_{OUT}}$	12	16	15	51 Ω to V_{TT}
C_{OUT}	13	1	17	51 Ω to V_{TT}
C_{IN}	14	2	18	GND
C_{IN}	15	3	19	OPEN
V_{CC2}	16	4	20	GND

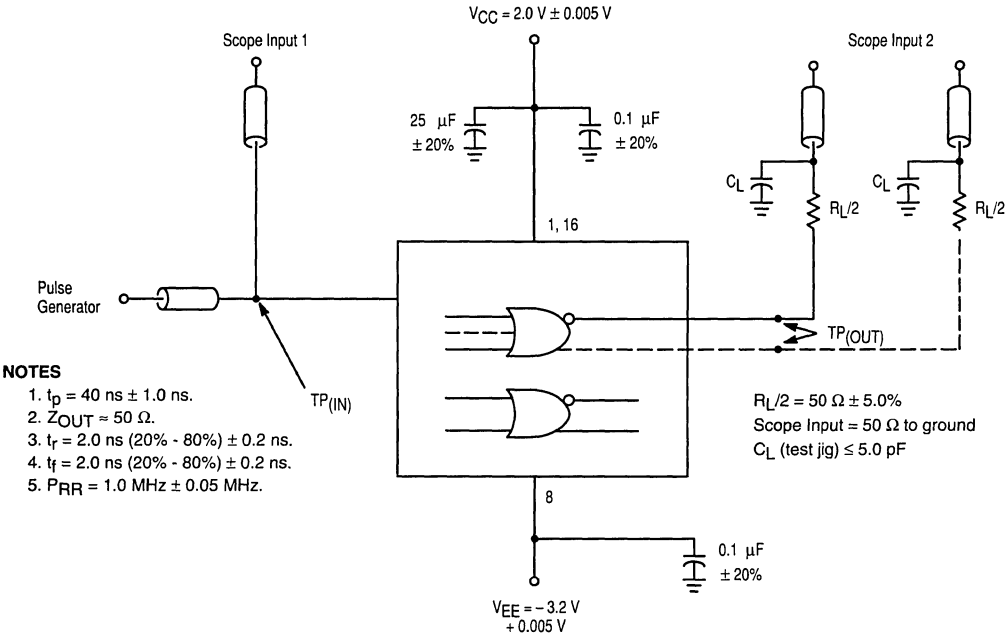
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM



$3 = (4 \bullet \overline{5}) + (\overline{4} \bullet 5)$
$2 = (\overline{4} \bullet \overline{5}) + (4 \bullet 5)$



NOTES
1. t_p = 40 ns ± 1.0 ns.
2. $Z_{OUT} \approx 50\ \Omega$.
3. t_r = 2.0 ns (20% - 80%) ± 0.2 ns.
4. t_f = 2.0 ns (20% - 80%) ± 0.2 ns.
5. P_{RR} = 1.0 MHz ± 0.05 MHz.

$R_L/2 = 50\ \Omega \pm 5.0\%$
Scope Input = 50 Ω to ground
C_L (test jig) ≤ 5.0 pF

NOTES
1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.

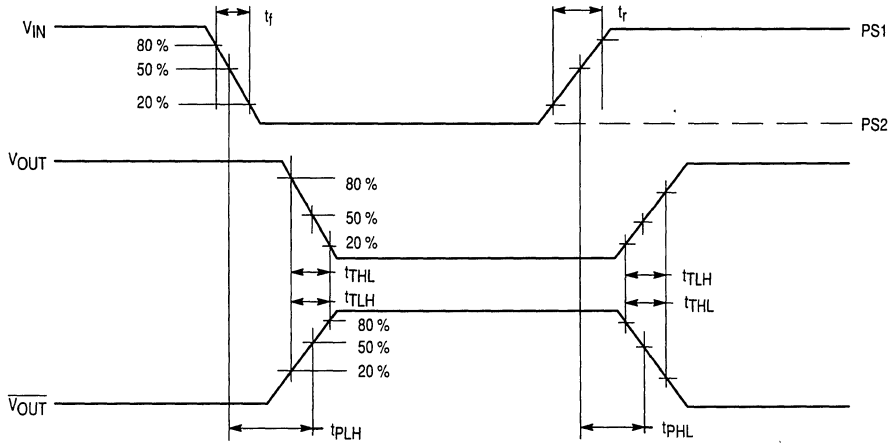


Figure 1. Switching Test Circuit and Waveforms

10507
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	P. U. T.
V_{OH}	High Output Voltage	–0.93	–0.78	–0.825	–0.63	–1.08	–0.88	V	All Inputs	All Inputs			1, 16	8	2, 3, 10 – 13
V_{OL}	Low Output Voltage	–1.86	–1.62	–1.82	–1.545	–1.92	–1.655	V	All Inputs	All Inputs			1, 16	8	2, 3, 10 – 13
V_{OTH}	High Output Voltage	–0.95		–0.845		–1.1		V		4, 9, 14	All Inputs	All Inputs	1, 16	8	2, 3, 10 – 13
V_{OTL}	Low Output Voltage		–1.6		–1.525		–1.635	V	5, 9, 14		All Inputs	All Inputs	1, 16	8	2, 3, 10 – 13
I_{EE}	Power Supply Current	–28		–31		–31		mA	4, 7, 15				1, 16	8	8
I_{IH1}	Input Current High		265		450		450	µA	4, 9, 14				1, 16	8	4, 9, 14
I_{IH2}	Input Current High		220		375		375	µA	5, 7, 15				1, 16	8	5, 7, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4, 5, 7, 9, 14,15			1, 16	8	4, 5, 7, 14, 15

10507
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	V_{EE2}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	+2.0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	+2.0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	+2.0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+25 °C		+125 °C		−55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	1.1	3.5	1.0	4.3	1.0	4.3	ns	4, 7, 14	2, 3, 10 – 13	1, 16	8	2, 3, 10 – 13
t_{THL}	Fall Time	1.1	3.5	1.0	4.3	1.0	4.3	ns	4, 7, 14	2, 3, 10 – 13	1, 16	8	2, 3, 10 – 13
t_{PLH}	Propagation Delay Low to High	1.1	3.7	1.0	4.5	1.0	4.5	ns	4, 7, 14	2, 3, 10 – 13	1, 16	8	2, 3, 10 – 13
t_{PHL}	Propagation Delay High to Low	1.1	3.7	1.0	4.5	1.0	4.5	ns	4, 7, 14	2, 3, 10 – 13	1, 16	8	2, 3, 10 – 13

Dual 4-5 Input "OR/NOR" Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/06006

The 10509 is a dual 4-5 input **OR/NOR** gate.

- 25 mW Max/Gate (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	GND
A_{IN}	6	10	8	OPEN
A_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B_{IN}	9	13	12	OPEN
B_{IN}	10	14	13	OPEN
B_{IN}	11	15	14	OPEN
B_{IN}	12	16	15	GND
B_{IN}	13	1	17	51 Ω to V_{TT}
$\overline{B_{OUT}}$	14	2	18	51 Ω to V_{TT}
B_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

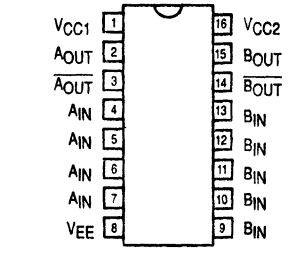
Military 10509

AVAILABLE AS

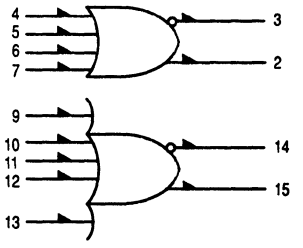
1) JAN: JM 38510/06006
2) SMD: N/A
3) 883: 10509/BXAJC
X = CASE OUTLINE AS FOLLOWS:

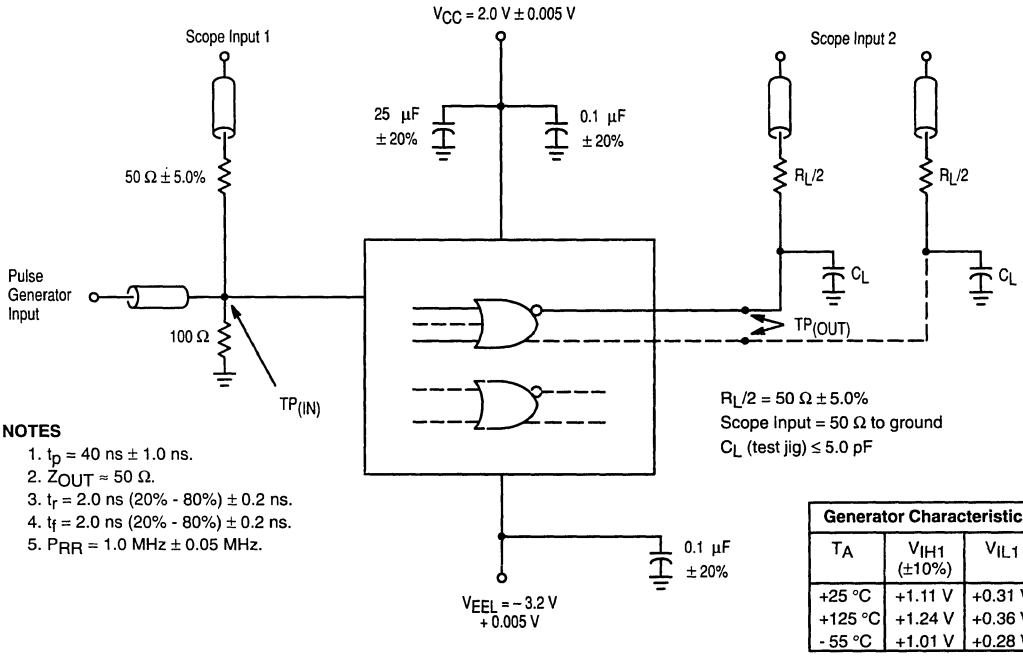
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. t_p = 40 ns ± 1.0 ns.
2. $Z_{OUT} \approx 50\ \Omega$.
3. t_r = 2.0 ns (20% - 80%) ± 0.2 ns.
4. t_f = 2.0 ns (20% - 80%) ± 0.2 ns.
5. P_{RR} = 1.0 MHz ± 0.05 MHz.

Generator Characteristics:		
T_A	V_{IH1} (±10%)	V_{IL1}
+25 °C	+1.11 V	+0.31 V
+125 °C	+1.24 V	+0.36 V
- 55 °C	+1.01 V	+0.28 V

NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.

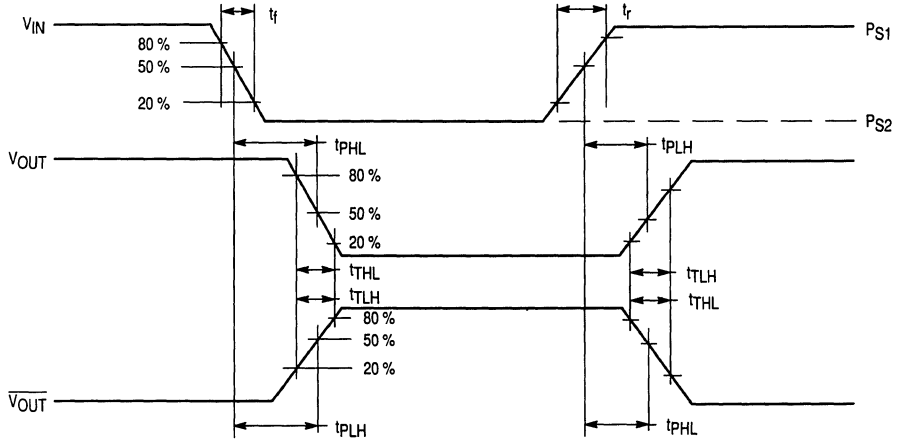


Figure 1. Switching Test Circuit and Waveforms

10509
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	0	-5.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	0	-5.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	0	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITL}	V_{ITH}	V_{CC}	V_{EE1}	P. U. T.
V_{OH}	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.06	-0.88	V	4 - 7, 9 - 13	4 - 7, 9 - 13			1, 16	8	2, 3, 14, 15
V_{OL}	Low Output Voltage	-1.86	-1.62	-1.82	-1.545	-1.92	-1.655	V	4 - 7, 9 - 13	4 - 7, 9 - 13			1, 16	8	2, 3, 14, 15
V_{OTH}	High Output Voltage	-0.96		-0.845		-1.1		V			4 - 7, 9 - 13	4 - 7, 9 - 13	1, 16	8	2, 3, 14, 15
V_{OTL}	Low Output Voltage		-1.6		-1.525		-1.635	V			4 - 7, 9 - 13	4 - 7, 9 - 13	1, 16	8	2, 3, 14, 15
I_{EE}	Power Supply Current	-14		-16		-16		mA					1, 16	8	8
I_{IH}	Input Current High		265		450		450	μA	4 - 7, 9 - 13				1, 16	8	4 - 7, 9 - 13
I_{IL}	Input Current Low	0.5		0.3		0.5		μA		4 - 7, 9 - 13			1, 16	8	4 - 7, 9 - 13

10509
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{CC}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	+1.11	+0.31	-1.475	-1.105	+2.0	-3.2
T_A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	+2.0	-3.2
T_A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	+2.0	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+ 25° C		+ 125 ° C		- 55 ° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	6, 11	2, 3, 14	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.0	4.0	1.0	4.0	ns	6, 11	2, 3, 14	1, 16	8	2, 3, 14, 15
t_{PLH}	Propaganda Delay Low to High	1.0	2.9	1.0	3.7	1.0	3.7	ns	6, 11	2, 3, 14	1, 16	8	2, 3, 14, 15
t_{PHL}	Propaganda Delay High to Low	1.0	2.9	1.0	3.7	1.0	3.7	ns	6, 11	2, 3, 14	1, 16	8	2, 3, 14, 15

MOTOROLA

Military 10513

Quad Exclusive OR Gate

ELECTRICALLY TESTED PER:
5962-8755801

The 10513 is a Quad Exclusive OR Gate with an enable common to all gates. The outputs may be wire-ORed together to perform a 4-bit comparison function (A = B). The enable is active Low.

- 240 mW Max/Pkg (No Load)
- t_{pd} = 2.5 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
A_{IN}	4	8	5	GND
A_{IN}	5	9	7	OPEN
B_{IN}	6	10	8	GND
B_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$\overline{Enable}$	9	13	12	OPEN
C_{IN}	10	14	13	GND
C_{IN}	11	15	14	OPEN
D_{IN}	12	16	15	GND
D_{IN}	13	1	17	OPEN
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Truth Table

Input		$\overline{E}$	Output
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
∅	∅	H	L

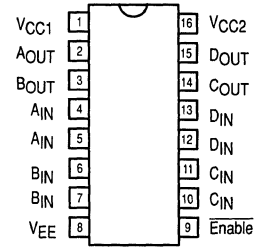
∅ = Don't Care

AVAILABLE AS

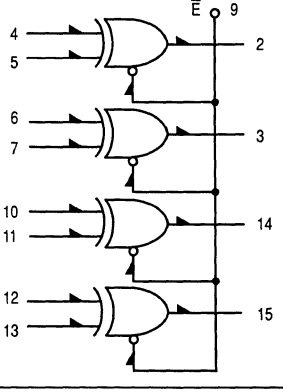
1) JAN: N/A
2) SMD: 5962-8755801
3) 883: 10513/BXAJC
X = CASE OUTLINE AS FOLLOWS:

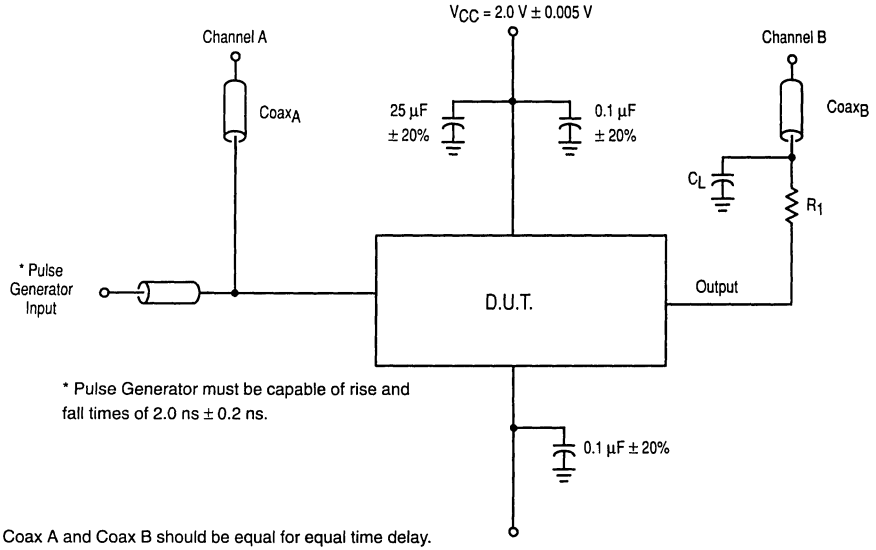
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

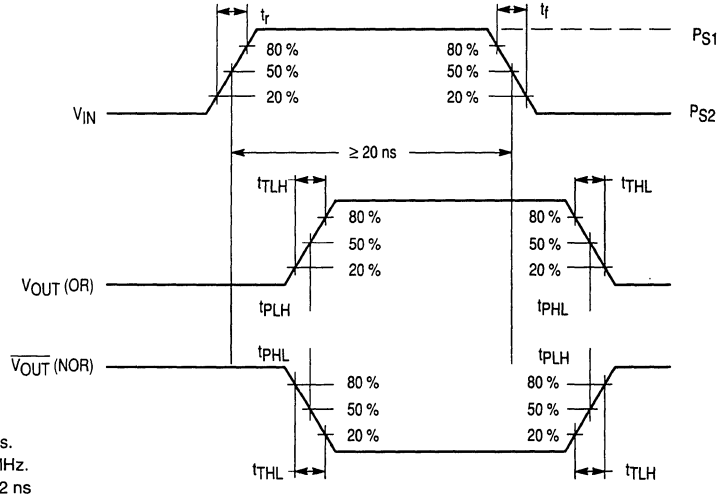


LOGIC DIAGRAM





NOTES
1. Length of Coax A and Coax B should be equal for equal time delay.
2. Unused outputs should be loaded 100 Ω to ground.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 2.0 ns ± 0.2 ns measured at (20% - 80%).
5. R_1 = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
6. $C_L \leq 5.0$ pF (including test jig).
7. $L_1 = L_2$: Matched for equal time delay. $P_W \geq 20$ ns.



NOTES
1. Pulse width ≥ 20 ns.
2. Frequency = 1.0 MHz.
3. $t_r = t_f$ = 2.0 ns ± 0.2 ns

Figure 1. Switching Test Circuit and Waveforms

10513
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{CC}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{CC}	V_{EE}	P. U. T.
V_{OH}	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.08	-0.88	V	4 - 7, 11, 14				1, 16	8	2, 3, 14, 15
V_{OL}	Low Output Voltage	-1.85	-1.62	-1.82	-1.545	-1.92	-1.655	V					1, 16	8	2, 3, 14, 15
V_{OHA}	High Output Voltage	-0.95		-0.845		-1.1		V	4 - 7, 11, 14		4 - 7, 11, 14	4 - 7, 11, 14	1, 16	8	2, 3, 14, 15
V_{OLA}	Low Output Voltage		-1.6		-1.525		-1.635	V	4 - 7, 11, 14		4 - 7, 11, 14	4 - 7, 11, 14	1, 16	8	2, 3, 14, 15
I_{EE}	Power Supply Current	-42		-46		-46		mA					1, 16	8	8
I_{IH1}	Input Current High		265		450		450	µA	4 - 7, 10, 13				1, 16	8	4, 7, 10, 13
I_{IH2}	Input Current High		220		375		375	µA	5, 6, 11, 12				1, 16	8	5, 6, 11, 12
I_{IH3}	Input Current High		545		925		925	µA	9				1, 16	8	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 13			1, 16	8	4 - 7, 9 - 13

10513
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{CC}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	+2.0	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	+2.0	-5.2	-3.2
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	+2.0	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+ 25° C		+ 125 ° C		- 55 ° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.9	1.1	4.4	1.1	4.2	ns	4, 5	2	1, 16	8	3, 14, 15
t_{THL}	Fall Time	1.1	3.9	1.1	4.4	1.1	4.2	ns	4, 5	2	1, 16	8	3, 14, 15
t_{PLH}	Propaganda Delay Low to High (A or B to Out)	1.3	4.5	1.3	5.0	1.1	4.7	ns	4, 5	2	1, 16	8	3, 14, 15
t_{PHL}	Propaganda Delay High to Low (A or B to Out)	1.3	4.5	1.3	5.0	1.1	4.7	ns	4, 5	2	1, 16	8	3, 14, 15
t_{PHL}	Propagation Delay High to Low (Enable to Out)	1.5	5.0	1.5	5.5	1.3	5.2	ns	4, 5	2	1, 16	8	3, 14, 15
t_{PLH}	Propagation Delay Low to High (Enable to Out)	1.5	5.0	1.5	5.5	1.3	5.2	ns	4, 5	2	1, 16	8	3, 14, 15

MOTOROLA

Triple Line Receiver

ELECTRICALLY TESTED PER:
MPG 10514

The 10514 is a triple line receiver designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

Another feature of the 10514 is that the OR outputs go to a logic low level whenever the inputs are left floating. The outputs are each capable of driving 50 ohm transmission lines.

This device is useful in high speed central processors, mini-computers, peripheral controllers, digital communication systems, testing and instrumentation systems. The 10514 can also be used for MOS to MECL interfacing and it is ideal as a sense amplifier for MOS RAM's.

A V_{BB} reference is provided which is useful in making the 10514 a Schmitt trigger, allowing single-ended driving of the inputs, or other applications where a stable reference voltage is necessary.

- P_D = 205 mW Max/Pkg (No Load)
- t_{pd} = 2.4 ns typ (Single-ended Input)
- t_{pd} = 2.0 ns typ (Differential Input)
- t_r, t_f = 2.1 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{A_{OUT}}$	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
$\overline{A_{IN}}$	4	8	5	GND
A_{IN}	5	9	7	V_{BB}
$\overline{B_{OUT}}$	6	10	8	51 Ω to V_{TT}
B_{OUT}	7	11	9	51 Ω to V_{TT}
V_{EE}	8	12	10	V_{EE}
$\overline{B_{IN}}$	9	13	12	GND
B_{IN}	10	14	13	V_{BB}
V_{BB}	11	15	14	V_{BB}
$\overline{C_{IN}}$	12	16	15	GND
C_{IN}	13	1	17	V_{BB}
$\overline{C_{OUT}}$	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN
V_{BB} = All pins designated for V_{BB} must be tied together, no external voltage applied.

NOTES

1. **V_{BB} to be used to supply bias to the 10514 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor.**
2. **When the input pin with the bubble goes positive, the output goes negative.**

Military 10514

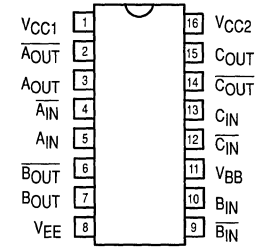
MPO

AVAILABLE AS

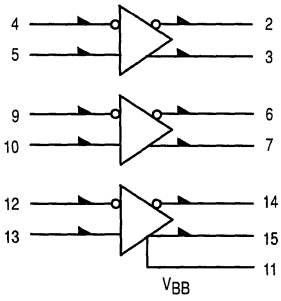
1) JAN: N/A
2) SMD: N/A
3) 883: 10514/BXAJC
X = CASE OUTLINE AS FOLLOWS:

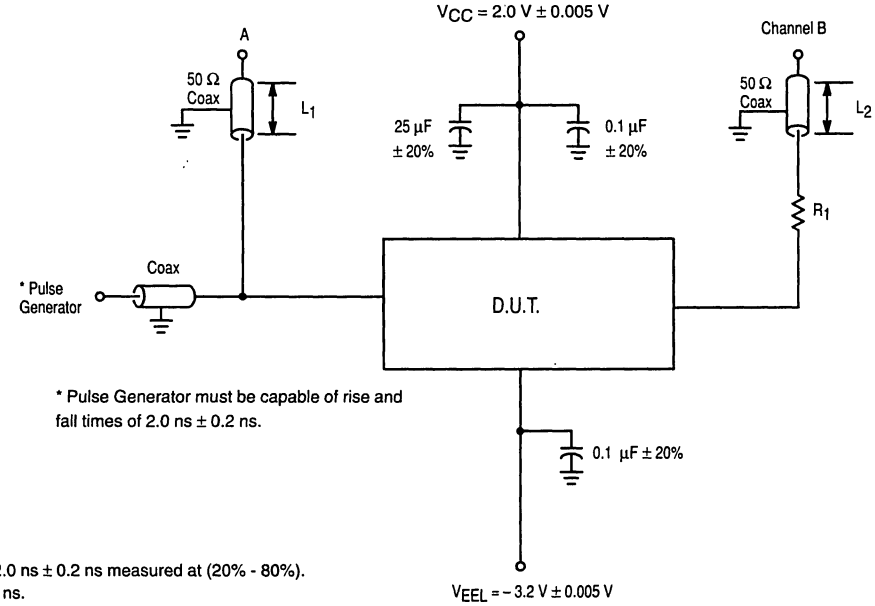
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. $t_r = t_f = 2.0$ ns ± 0.2 ns measured at (20% - 80%).
2. $P_W \geq 20$ ns.
3. $P_{RF} = 1.0$ MHz.
4. $R_1 = 50\ \Omega$ resistor in series with 50 Ω coax constituting the 100 Ω load.
5. Unused outputs should be loaded 100 Ω to ground.
6. 2:1 divider may be used.
7. $L_1 = L_2$: Matched for equal time delay.

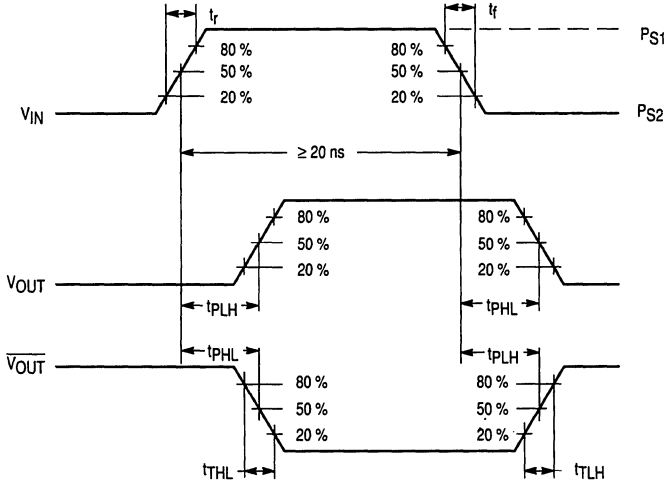


Figure 1. Switching Test Circuit and Waveforms

10514
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{IHT}	V_{ILT}	V_{IHL}	V_{ILH}
T_A = 25 °C	-0.78	-1.85	+0.22	-2.85	-1.105	-1.475	-1.78	-0.85
T_A = 125 °C	-0.63	-1.82	+0.37	-2.82	-1.000	-1.400	-1.63	-0.82
T_A = -55 °C	-0.88	-1.92	+0.12	-2.92	-1.255	-1.510	-1.88	-0.92

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V, V_{EE} = -5.2 V, V_{EEL} = -3.2 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{IHL}	V_{LH}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	–0.93	–0.78	–0.825	–0.63	–1.08	–0.88	V	4, 5, 9 10, 12 13	4, 5, 9 10, 12 13	4, 5, 9 10, 12 13		8		4, 5, 9 10, 12 13	1, 16	2, 3, 6, 7 14, 15
V_{OL}	Low Output Voltage	–1.85	–1.62	–1.82	–1.545	–1.92	–1.655	V	4, 5, 9 10, 12 13	4, 5, 9 10, 12 13		4, 5, 9 10, 12 13	8	4, 5, 9 10, 12 13		1, 16	2, 3, 6, 7 14, 15
V_{BB}	Reference Voltage	–1.35	–1.23	–1.24	–1.12	–1.44	–1.32	V					8			1, 16	11
I_{EE}	Power Supply Current	–35		–39		–39		mA					8			1, 16	8
I_{IH}	Input Current High		45		80		80	µA	4, 5, 9 10, 12 13	4, 5, 9 10, 12 13			8			1, 16	4, 5, 9, 10 12, 13
I_{CBO}	Input Leakage Current	–1.0		–1.0		–1.5		µA					4, 5, 8 9, 10, 12, 13			1, 16	4, 5, 9, 10 12, 13
V_{OH1}	High Output Voltage	–0.95		–0.845		–1.1		V	V_{ITH} 4, 5, 9, 10, 12, 13		V_{ITL} 4, 5, 9, 10, 12, 13		V_{EE} 8	** 4, 5, 9, 12		V_{CC} 1, 16	(PUT) LD_1 4, 5, 9, 12
V_{OL1}	Low Output Voltage		–1.6		–1.525		–1.635	V	4, 5, 9, 10, 12, 13		4, 5, 9, 10, 12, 13		8	4, 5, 9, 12		1, 16	4, 5, 9, 12

** Connected to pin 11

10514
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{IHT}	V_{ILT}	V_{IHL}	V_{ILH}
T_A = 25 °C	-0.78	-1.85	+0.22	-2.85	-1.105	-1.475	-1.78	-0.85
T_A = 125 °C	-0.63	-1.82	+0.37	-2.82	-1.000	-1.400	-1.63	-0.82
T_A = -55 °C	-0.88	-1.92	+0.12	-2.92	-1.255	-1.510	-1.88	-0.92

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND, V_{EE} = -5.2 V, V_{EEL} = -3.2 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		**	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.5	3.5	1.2	4.1	1.3	3.8	ns	5, 10, 13	4, 9, 12	2, 3, 6, 7, 14, 15	1, 16	8	2, 3, 6, 7, 14, 15
t_{THL}	Fall Time	1.5	3.5	1.2	4.1	1.3	3.8	ns	5, 10, 13	4, 9, 12	2, 3, 6, 7, 14, 15	1, 16	8	2, 3, 6, 7, 14, 15
t_{PHL}	Propagation Delay High to Low	1.0	4.0	1.0	4.7	1.0	4.3	ns	5, 10, 13	4, 9, 12	2, 3, 6, 7, 14, 15	1, 16	8	2, 3, 6, 7, 14, 15
t_{PLH}	Propagation Delay Low to High	1.0	4.0	1.0	4.7	1.0	4.3	ns	5, 10, 13	4, 9, 12	2, 3, 6, 7, 14, 15	1, 16	8	2, 3, 6, 7, 14, 15

** Connected to pin 11

Quad Line Receiver

Military 10515

ELECTRICALLY TESTED PER:
MPG 10515

The 10515 is a quad differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 9 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the 10515 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 9) to prevent upsetting the current source bias network.

- P_D = 150 mW Max/Pkg (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

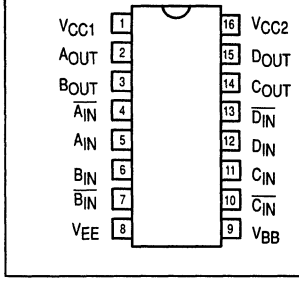
1) JAN: N/A
2) SMD: N/A
3) 883: 10515/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

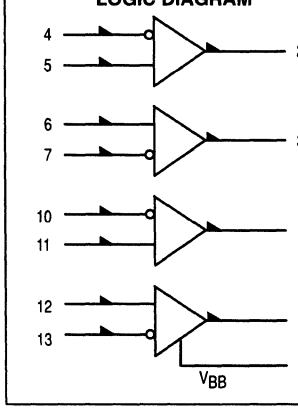
The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
$\overline{A_{IN}}$	4	8	5	V_{BB}
A_{IN}	5	9	7	GND
B_{IN}	6	10	8	GND
$\overline{B_{IN}}$	7	11	9	V_{BB}
V_{EE}	8	12	10	V_{EE}
V_{BB}	9	13	12	V_{BB}
C_{IN}	10	14	13	V_{BB}
C_{IN}	11	15	14	GND
D_{IN}	12	16	15	GND
$\overline{D_{IN}}$	13	1	17	V_{BB}
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



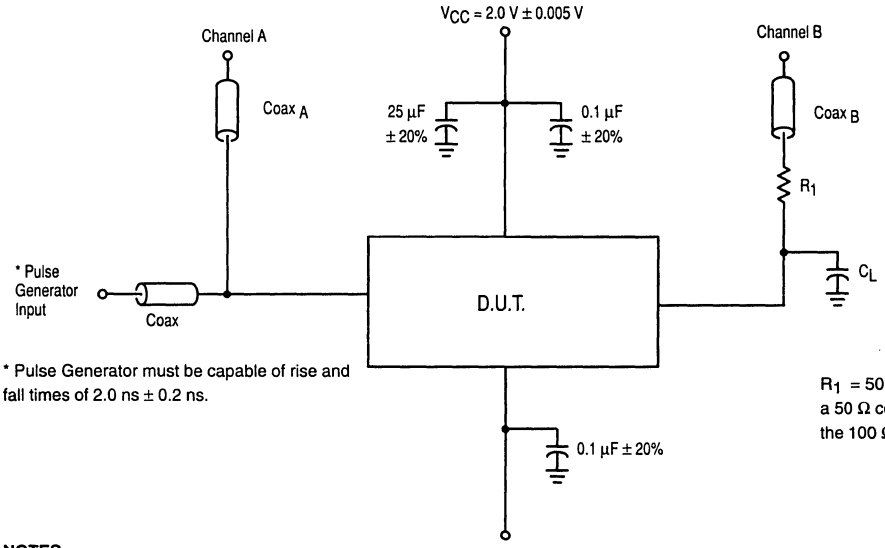
LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN
V_{BB} = All pins designated for V_{BB} must be tied together, no external voltage applied.

NOTES

1. **V_{BB} to be used to supply bias to the 10515 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor.**
2. **When the input pin with the bubble goes positive, the output goes negative.**



* Pulse Generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.

R_1 = 50 Ω resistor in series with a 50 Ω coax cable constituting the 100 Ω load.

3

NOTES
1. $t_r = t_f$ = 2.0 ns ± 0.2 ns measured at (20% - 80%).
2. $P_W \geq 20$ ns.
3. P_{RF} = 1.0 MHz.
4. R_1 = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
5. Unused outputs should be loaded 100 Ω to ground.
6. 2:1 divider may be used.

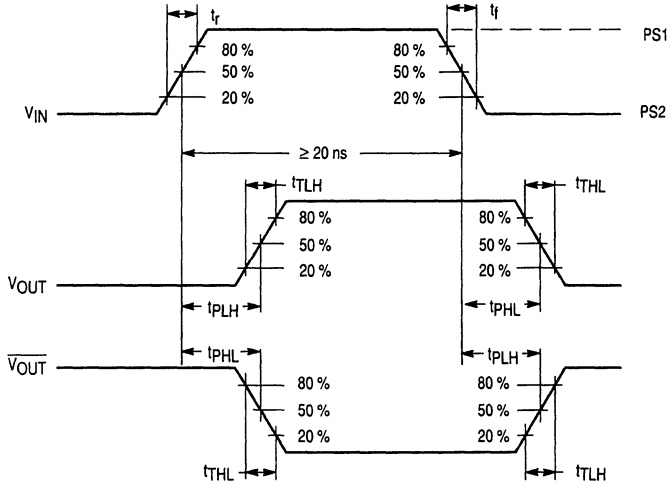


Figure 1. Switching Test Circuit and Waveforms

10515
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE}	V_{CB}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-3.2	-5.2	-5.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-3.2	-5.2	-5.2
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-3.2	-5.2	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	***	P. U. T.
V_{OH}	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.08	-0.88	V	5, 6, 11, 12	4, 7 10, 13			8	1, 16	4 - 7 11 - 13	2, 3, 14, 15
V_{OL}	Low Output Voltage	-1.85	-1.62	-1.82	-1.545	-1.92	-1.655	V	4, 7, 10, 13	5, 6 11, 12			8	1, 16	4 - 7 11 - 13	2, 3, 14, 15
V_{OH1}	High Output Voltage	-0.95	-0.78	-0.845	-0.63	-1.10	-0.88	V			5, 6 11, 12	4, 7 10, 13	8	1, 16	4 - 7 11 - 13	2, 3, 14, 15
V_{OL1}	Low Output Voltage	-1.85	-1.60	-1.82	-1.525	-1.92	-1.635	V			4, 7 10, 13	5, 6 11, 12	8	1, 16	4 - 7 11 - 13	2, 3, 14, 15
** V_{BB}	Reference Voltage	-1.35	-1.23	-1.24	-1.12	-1.44	-1.32	V					8	1, 16	5, 6 11, 12	9
I_{EE}	Power Supply Current	-26		-29		-29		mA					8	1, 16	5, 6 11, 12	8
I_{IH}	Input Current High		95		165		165	µA	4 - 7 10 - 13				8	1, 16		4 - 7 10 - 13
I_{CBO}	Input Leakage Current	-1.0		-1.0		-1.5		µA					8	1, 16	4 - 7 10 - 13	4 - 7 10 - 13

** Connected to pin 9.
*** Measure voltage on pin 9 while it is connected to other pins.

10515
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE}	V_{CB}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-3.2	-5.2	-5.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-3.2	-5.2	-5.2
T_A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-3.2	-5.2	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	4.4	1.0	3.9	ns	4, 7 11, 13	2, 3 14, 15	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.0	4.4	1.0	3.9	ns	4, 7 11, 13	2, 3 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL}	Propagation Delay High to Low	1.0	2.9	1.0	4.0	1.0	3.5	ns	4, 7 11, 13	2, 3 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High	1.0	2.9	1.0	4.0	1.0	3.5	ns	4, 7 11, 13	2, 3 14, 15	1, 16	8	2, 3, 14, 15

MOTOROLA

Triple Line Receiver

Military 10516

ELECTRICALLY TESTED PER:
5962-7800901

The 10516 is a triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide the 10516 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to complement outputs of the input logic function.

3

- P_D = 125 mW Max/Pkg (No Load)
- t_{pd} = 2.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

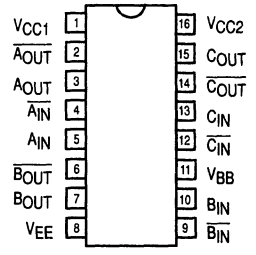
1) JAN: N/A
2) SMD: 5962-7800901
3) 883: 10516/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

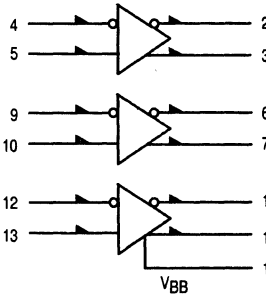
The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{A_{OUT}}$	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
$\overline{A_{IN}}$	4	8	5	GND
A_{IN}	5	9	7	V_{BB}
$\overline{B_{OUT}}$	6	10	8	51 Ω to V_{TT}
B_{OUT}	7	11	9	51 Ω to V_{TT}
V_{EE}	8	12	10	V_{EE}
$\overline{B_{IN}}$	9	13	12	GND
B_{IN}	10	14	13	V_{BB}
V_{BB}	11	15	14	V_{BB}
$\overline{C_{IN}}$	12	16	15	GND
C_{IN}	13	1	17	V_{BB}
$\overline{C_{OUT}}$	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



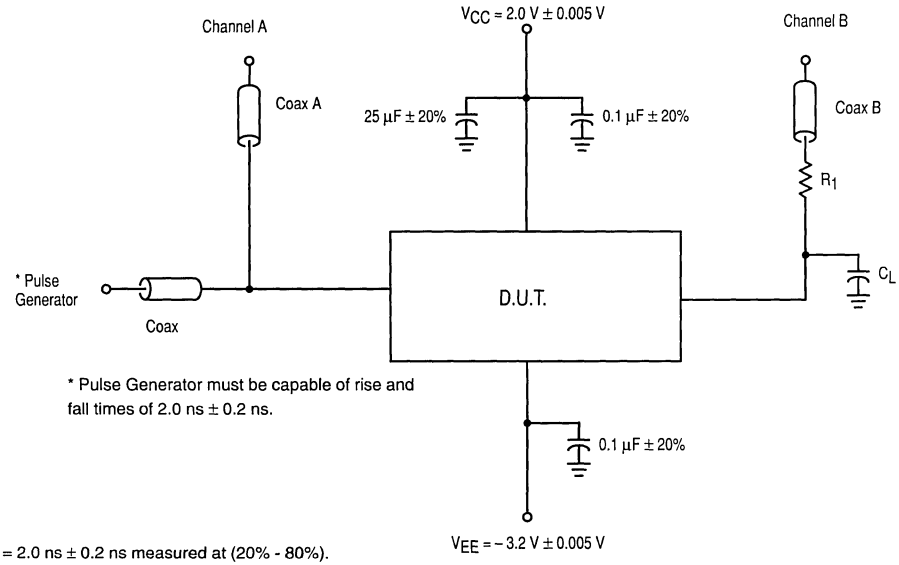
LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN
V_{BB} = All pins designated for V_{BB} must be tied together, no external voltage applied.

NOTES

1. **V_{BB} to be used to supply bias to the 10516 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor.**
2. **When the input pin with the bubble goes positive, the output goes negative.**



NOTES

1. $t_r = t_f$ = 2.0 ns ± 0.2 ns measured at (20% - 80%).
2. $P_W \geq 20$ ns.
3. P_{RF} = 1.0 MHz.
4. R1 = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
5. Unused outputs should be loaded 100 Ω to ground.
6. 2:1 divider may be used.
7. Length of $Coax_A$ and $Coax_B$ are matched 50 Ω.
8. $C_L \leq 5.0$ pF (including test jig).
9. Length of $Coax_A$ and $Coax_B$ should be matched for equal time delay.

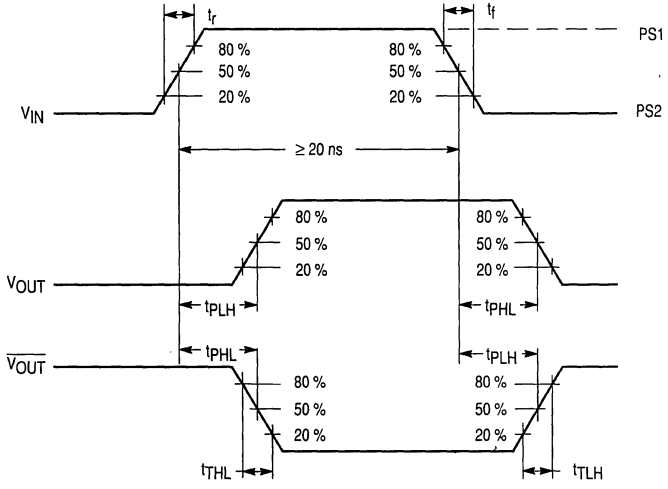


Figure 1. Switching Test Circuit and Waveforms

10516
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 3.2	- 5.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 3.2	- 5.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 3.2	- 5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V, V_{BB} = -5.2 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	V_{CB}	V_{BB}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13			8	1, 16			2, 3, 6, 7, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4, 5, 9, 10, 12, 13, 14	4, 5, 9, 10, 12, 13			8	1, 16			2, 3, 6, 7, 14, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.1	- 0.88	V	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13	8	1, 16		4, 5, 9, 10, 12, 13	2, 3, 6, 7, 14, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.6	- 1.82	- 1.525	- 1.92	- 1.635	V	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13	8	1, 16		4, 5, 9, 10, 12, 13	2, 3, 6, 7, 14, 15
**V_{BB1}	Reference Voltage	- 1.35	- 1.23	- 1.24	- 1.12	- 1.44	- 1.32	V						1, 16			11
I_{EE}	Power Supply Current	- 21		- 24		- 24		mA	4, 9, 12	5, 10, 13			8	1, 16			8
I_{IH}	Input Current High		95		165		165	µA	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13			8	1, 16			4, 5, 9, 10, 12, 13
I_{CBO}	Input Leakage Current	- 1.0		- 1.0		-1.5		µA	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13				1, 16	4, 5, 9, 10, 12, 13		4, 5, 9, 10, 12, 13

** Connect pins 5, 10, 13 to pin 11

10516
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EEL}	V_{EE1}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 3.2	- 5.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 3.2	- 5.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 3.2	- 5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, V_{BB} = -5.2 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{BB}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	4.4	1.0	3.9	ns	4, 9	2, 3	1, 16	5, 10, 13	8	2, 3, 7, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.0	4.4	1.0	3.9	ns	4, 9	2, 3	1, 16	5, 10, 13	8	2, 3, 7, 14, 15
t_{PHL}	Propagation Delay High to Low	1.0	2.9	1.0	4.0	1.0	3.5	ns	4, 9	2, 3	1, 16	5, 10	8	2, 3, 7, 14, 15
t_{PLH}	Propagation Delay Low to High	1.0	2.9	1.0	4.0	1.0	3.5	ns	4, 9	2, 3	1, 16	5, 10	8	2, 3, 7, 14, 15

MOTOROLA

Dual 2-Wide 2-3 Input "OR-AND/OR-AND-INVERT" Gate

ELECTRICALLY TESTED PER:
MPG 10517

The 10517 is a general purpose logic element designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates.

- 150 mW Max/Pkg (No Load)
- t_{pd} = 2.3 ns typ
- t_r, t_f = 2.2 ns typ (20% - 80%)

3

	PIN ASSIGNMENTS			
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V_{TT}
$A1_{IN}$	4	8	5	OPEN
$A1_{IN}$	5	9	7	OPEN
$A2_{IN}$	6	10	8	OPEN
$A2_{IN}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$A2_{IN}$, $B2_{IN}$	9	13	12	OPEN
$B2_{IN}$	10	14	13	OPEN
$B2_{IN}$	11	15	14	OPEN
$B1_{IN}$	12	16	15	OPEN
$B1_{IN}$	13	1	17	OPEN
$\overline{B_{OUT}}$	14	2	18	51 Ω to V_{TT}
B_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Military 10517

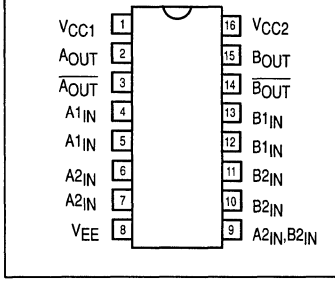
MPO

AVAILABLE AS

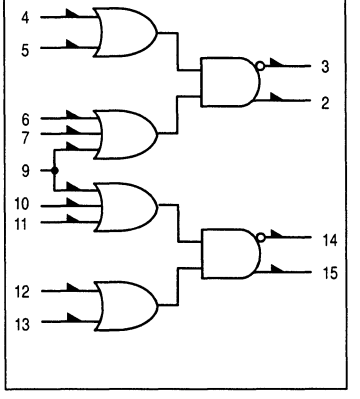
1) JAN: N/A
2) SMD: N/A
3) 883: 10517/BXAJC
X = CASE OUTLINE AS FOLLOWS:

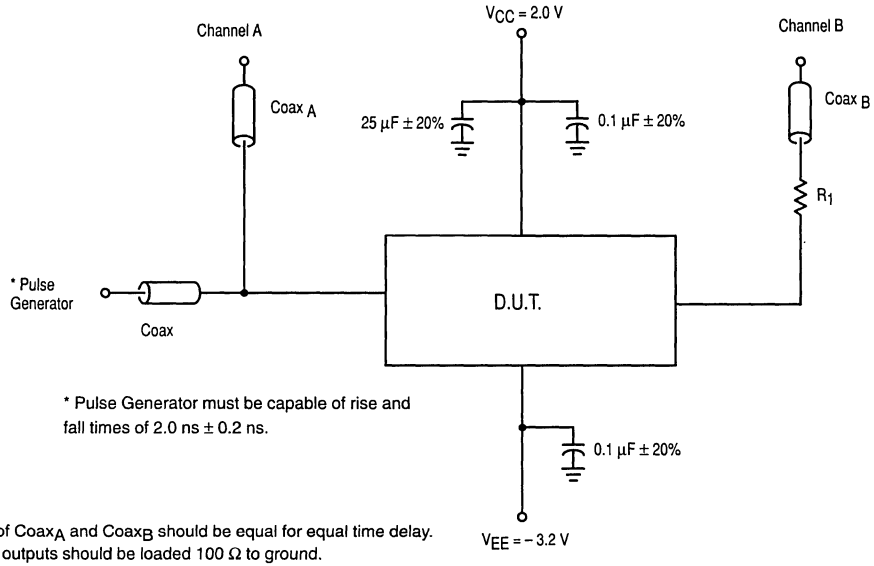
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES
1. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
2. Unused outputs should be loaded 100 Ω to ground.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns measured at (20% - 80%).
5. $P_W \geq 20$ ns.
6. $P_{RF} = 1.0$ MHz.
7. $R_1 = 50$ Ω resistor in series with 50 Ω coax constituting the 100 Ω load.

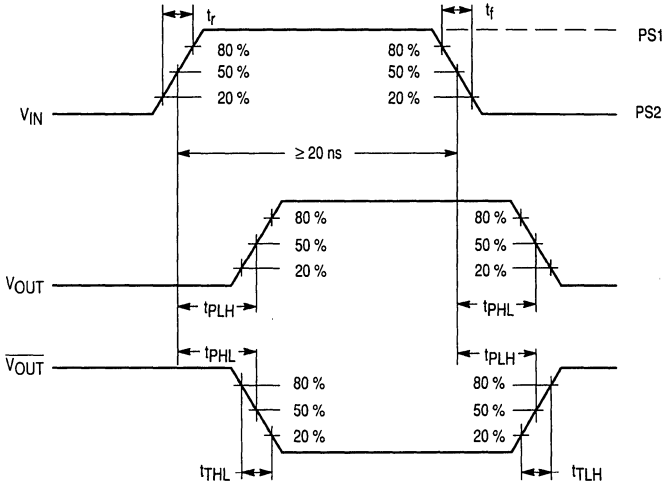


Figure 1. Switching Test Circuit and Waveforms

10517
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	-1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	-1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	-1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25° C		+ 125 ° C		- 55 ° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4 - 7 9 - 13				8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4 - 7 9 - 13				8	1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	4 - 7 9 - 13		4 - 7 9 - 13	4 - 7 9 - 13	8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	4 - 7 9 - 13		4 - 7 9 - 13	4 - 7 9 - 13	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	- 26		- 29		- 29		mA					8	1, 16	8
I_{IH}	Input Current High		245		415		415	μA	4, 5 12, 13				8	1, 16	4, 5, 12, 13
I_{IH1}	Input Current High		265		450		450	μA	6, 7 10, 11				8	1, 16	6, 7, 10, 11
I_{IH2}	Input Current High		350		595		595	μA	9				8	1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		μA		4 - 7 9 - 13			8	1, 16	7, 9 - 1

10517
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	-1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.66	- 1.82	- 1.000	-1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	-1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.0	4.0	0.9	4.0	1.0	4.1	ns	4, 6, 11, 12	2, 14, 15	1, 16	8	4, 6, 11, 12	2, 3, 14, 15
t_{THL}	Fall Time	1.0	4.0	0.9	4.0	1.0	4.1	ns	4, 6, 11, 12	2, 14, 15	1, 16	8	4, 6, 11, 12	2, 3, 14, 15
t_{PHL}	Propagation Delay High to Low	1.4	3.4	1.2	3.5	1.1	3.5	ns	4, 6, 11, 12	2, 14, 15	1, 16	8	4, 6, 11, 12	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High	1.4	3.4	1.2	3.5	1.1	3.5	ns	4, 6, 11, 12	2, 14, 15	1, 16	8	4, 6, 11, 12	2, 3, 14, 15

Dual 2-Wide 3-Input "OR-AND" Gate

ELECTRICALLY TESTED PER:
MPG 10518

The 10518 is a basic logic building block providing the OR/AND function, useful in data control and digital multiplexing applications.

- 150 mW Max/Pkg (No Load)
- t_{pd} = 2.3 ns typ
- t_r, t_f = 2.5 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$A1_{IN}$	3	7	4	OPEN
$A1_{IN}$	4	8	5	OPEN
$A1_{IN}$	5	9	7	GND
$A2_{IN}$	6	10	8	GND
$A2_{IN}$	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
$A2_{IN}$, $B2_{IN}$	9	13	12	GND
$B2_{IN}$	10	14	13	GND
$B2_{IN}$	11	15	14	OPEN
$B1_{IN}$	12	16	15	GND
$B1_{IN}$	13	1	17	OPEN
$B1_{IN}$	14	2	18	OPEN
B_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

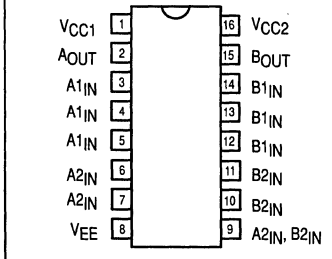
Military 10518

AVAILABLE AS

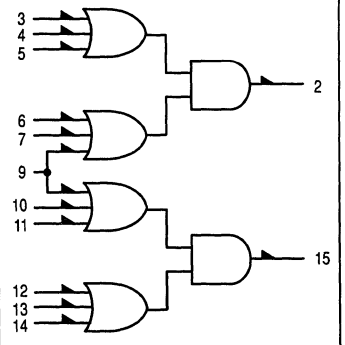
1) JAN: N/A
2) SMD: N/A
3) 883: 10518/BXAJC
X = CASE OUTLINE AS FOLLOWS:

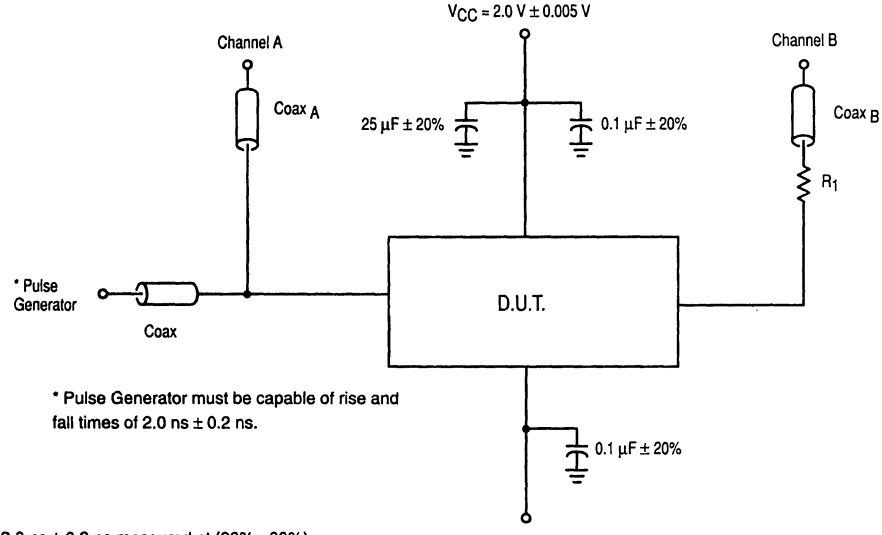
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. $t_r = t_f$ = 2.0 ns ± 0.2 ns measured at (20% - 80%).
2. $P_W \geq 20$ ns.
3. P_{RF} = 1.0 MHz.
4. 2:1 divider may be used.
5. R_1 = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground.
7. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
8. $Coax_A$ and $Coax_B$ are matched 50 Ω.

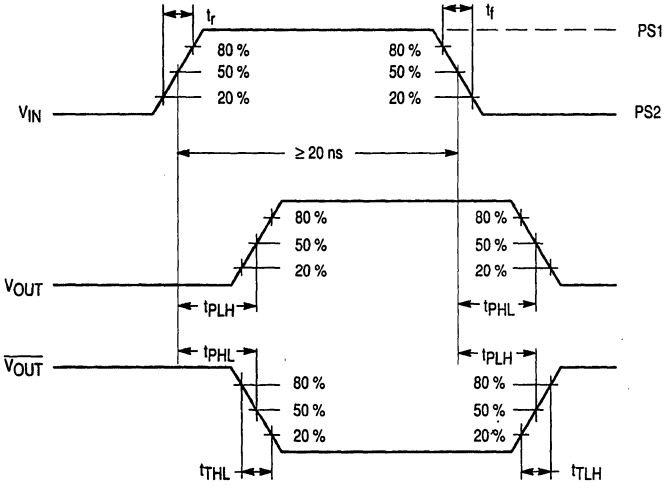


Figure 1. Switching Test Circuit and Waveforms

10518
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = -55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{EEL}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	3 - 7 9 - 14				8		1, 16	2, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	10, 13	3 - 7 9 - 14			8		1, 16	2, 15
V_{OH1}	High Output Voltage	- 0.95		- 0.845		- 1.1		V	3 - 7 9 - 14	3 - 7 9 - 14	3 - 7 9 - 14		8	8	1, 16	2, 15
V_{OL1}	Low Output Voltage		- 1.6		- 1.525		- 1.635	V	3 - 7 9 - 14	3 - 7 9 - 14		3 - 7 9 - 14	8	8	1, 16	2, 15
I_{EE}	Power Supply Current	- 26		- 29		- 29		mA					8		1, 16	8
I_{IH}	Input Current High		245		415		415	µA	3 - 5 12 - 14				8		1, 16	3 - 5, 12 - 14
I_{IH1}	Input Current High		265		450		450	µA	6, 7 10, 11				8		1, 16	6, 7, 10, 11
I_{IH2}	Input Current High		350		595		595	µA	9				8		1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 7 9 - 14			8		1, 16	3 - 7, 9 - 14

10518
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = -55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.3	4.0	1.0	4.0	1.1	4.1	ns	4, 10, 12	2, 15	1, 16	8	3, 5, 6, 9, 10, 12, 14	2, 15
t_{THL}	Fall Time	1.3	4.0	1.0	4.0	1.1	4.1	ns	4, 10, 12	2, 15	1, 16	8	3, 5, 6, 9, 10, 12, 14	2, 15
t_{PHL}	Propagation Delay High to Low	1.4	3.4	1.2	3.5	1.1	3.5	ns	4, 10, 12	2, 15	1, 16	8	3, 5, 6, 9, 10, 12, 14	2, 15
t_{PLH}	Propagation Delay Low to High	1.4	3.4	1.2	3.5	1.1	3.5	ns	4, 10, 12	2, 15	1, 16	8	3, 5, 6, 9, 10, 12, 14	2, 15

4-Wide 4-3-3-3 Input "OR-AND" Gate

Military 10519

ELECTRICALLY TESTED PER:
MPG 10519

The 10519 is a 4-wide 4-3-3-3 input **OR/AND** gate with one input from two gates common to pin 10.

- 150 mW Max/Pkg (No Load)
- t_{pd} = 2.3 ns typ
- t_r, t_f = 2.5 ns typ (20% - 80%)

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10519/BXAJC
X = CASE OUTLINE AS FOLLOWS:

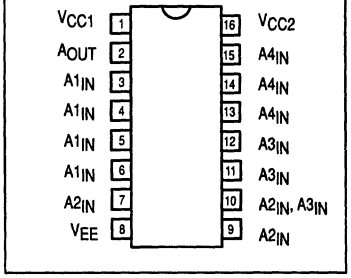
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

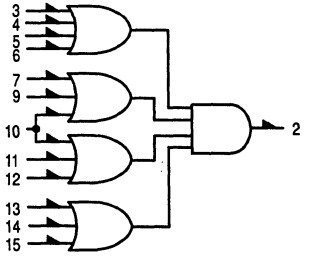
PIN ASSIGNMENTS

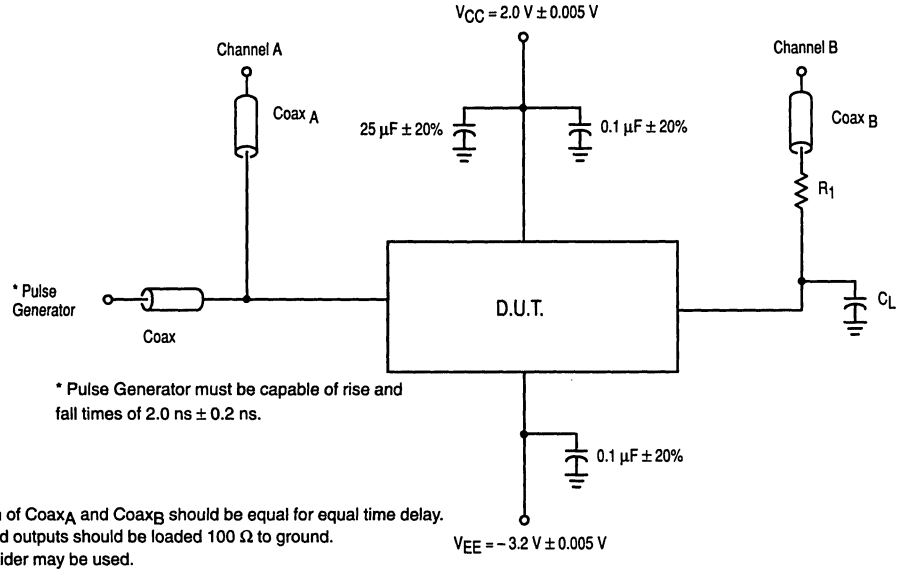
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$A1_{IN}$	3	7	4	GND
$A1_{IN}$	4	8	5	OPEN
$A1_{IN}$	5	9	7	OPEN
$A1_{IN}$	6	10	8	OPEN
$A2_{IN}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$A2_{IN}$	9	13	12	OPEN
$A2_{IN}$, $A3_{IN}$	10	14	13	GND
$A3_{IN}$	11	15	14	OPEN
$A3_{IN}$	12	16	15	OPEN
$A4_{IN}$	13	1	17	OPEN
$A4_{IN}$	14	2	18	OPEN
$A4_{IN}$	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM





NOTES

1. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
2. Unused outputs should be loaded 100 Ω to ground.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns measured at (20% - 80%).
5. $P_W \geq 20$ ns.
6. $P_{RF} = 1.0$ MHz.
7. $R_1 = 50$ Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
8. $C_L \leq 5.0$ pF (including test jig).

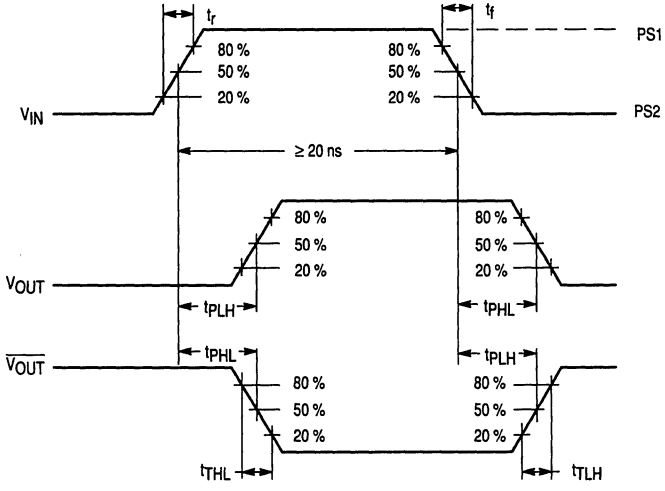


Figure 1. Switching Test Circuit and Waveforms

10519
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = -55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	3 - 7, 9, - 15				8	1, 16	2
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	3, 7, 10, 11, 13	3 - 7, 9 - 15			8	1, 16	2
V_{OH1}	High Output Voltage	- 0.95		- 0.845		- 1.10		V	3 - 7, 9 - 15	3 - 7, 9 - 15	3 - 7, 9 - 15		8	1, 16	2
V_{OL1}	Low Output Voltage		- 1.600		- 1.525		- 1.635	V	3 - 7, 9 - 15	3 - 7, 9 - 15		3 - 7, 9 - 15	8	1, 16	2
I_{EE}	Power Supply Current	- 26		- 29		- 29		mA					8	1, 16	8
I_{IH}	Input Current High		390		415		415	µA	3 - 7, 9, 11 - 15				8	1, 16	3 - 7, 9 - 15
I_{IH1}	Input Current High		495		525		525	µA	10				8	1, 16	10
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 7, 9 - 15			8	1, 16	3 - 7, 9 - 15

10519
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = -55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.5	4.0	1.2	4.3	1.3	4.1	ns	4, 7, 12, 14	2	1, 16	8	4, 7, 12, 14	2
t_{THL}	Fall Time	1.5	4.0	1.2	4.3	1.3	4.1	ns	4, 7, 12, 14	2	1, 16	8	4, 7, 12, 14	2
t_{PHL}	Propagation Delay High to Low	1.4	3.8	1.2	4.0	1.1	4.1	ns	4, 7, 12, 14	2	1, 16	8	4, 7, 12, 14	2
t_{PLH}	Propagation Delay Low to High	1.4	3.8	1.2	4.0	1.1	4.1	ns	4, 7, 12, 14	2	1, 16	8	4, 7, 12, 14	2

4-Wide "OR-AND/OR-AND-INVERT" Gate

ELECTRICALLY TESTED PER:
5962-8857701

The 10521 is a basic building block providing the simultaneous OR-AND/OR-AND-INVERT function, useful in data control and digital multiplexing applications.

- 150 mW Max/Pkg (No Load)
- t_{pd} = 2.3 ns typ
- t_r, t_f = 2.5 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V_{TT}
$A1_{IN}$	4	8	5	OPEN
$A1_{IN}$	5	9	7	OPEN
$A1_{IN}$	6	10	8	OPEN
$A2_{IN}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$A2_{IN}$	9	13	12	OPEN
$A2_{IN}$, $A3_{IN}$	10	14	13	OPEN
$A3_{IN}$	11	15	14	OPEN
$A3_{IN}$	12	16	15	OPEN
$A4_{IN}$	13	1	17	OPEN
$A4_{IN}$	14	2	18	OPEN
$A4_{IN}$	15	3	19	OPEN
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

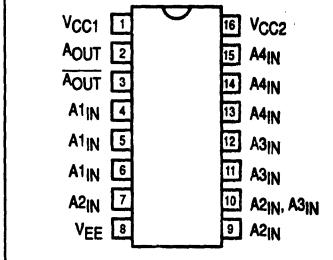
Military 10521

AVAILABLE AS

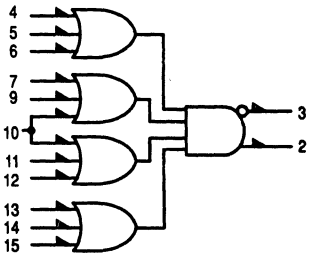
1) JAN: N/A
2) SMD: 5962-8857701
3) 883: 10521/BXAJC
X = CASE OUTLINE AS FOLLOWS:

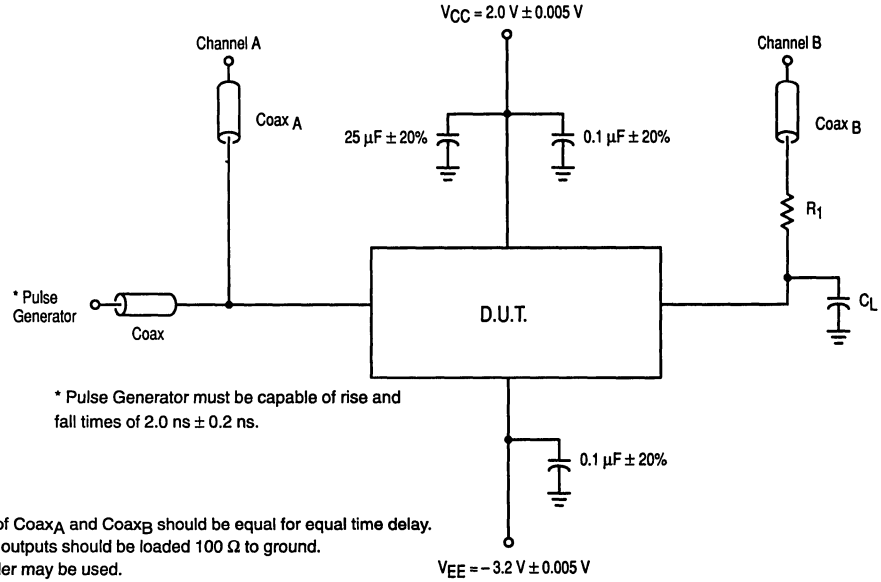
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
2. Unused outputs should be loaded 100 Ω to ground.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns measured at (20% - 80%).
5. $P_W \geq 20$ ns.
6. $P_{RF} = 1.0$ MHz.
7. $R_1 = 50$ Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
8. C_L = Jig and stray capacitance ≤ 5.0 pF.

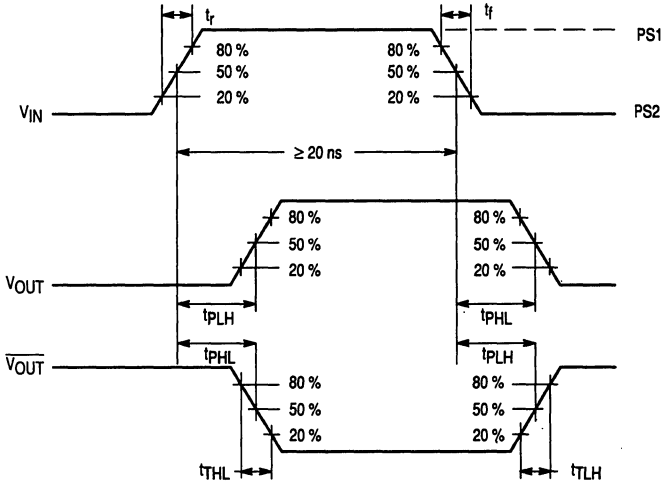


Figure 1. Switching Test Circuit and Waveforms

10521
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4 - 7, 9 - 15	4 - 7, 9 - 15			8	1, 16	2, 3
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4 - 7, 9 - 13	4 - 7, 9 - 15			8	1, 16	2, 3
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	4, 7, 11, 13	4, 7, 11, 13	4 - 7, 9 - 13	4 - 7, 9 - 13	8	1, 16	2, 3
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	4, 7, 11, 13		4 - 7, 9 - 13	4 - 7, 9 - 13	8	1, 16	2, 3
I_{EE}	Power Supply Current	- 26		- 29		- 29		mA					8	1, 16	8
I_{IH}	Input Current High		245		415		415	µA	4 - 7, 9, 11 - 15				8	1, 16	4 - 7, 9, 11 - 15
I_{IH1}	Input Current High		310		525		525	µA	10				8	1, 16	10
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 15			8	1, 16	4 - 7, 9 - 15

10521
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = -55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.1	4.0	0.9	4.4	1.0	4.5	ns	5, 9, 10 12, 15	3	1, 16	8	5, 9, 12, 15	2, 3
t_{THL}	Fall Time	1.1	4.0	0.9	4.4	1.0	4.5	ns	5, 9, 10 12, 15	3	1, 16	8	5, 9, 12, 15	2, 3
t_{PHL}	Propagation Delay High to Low	1.4	3.5	1.1	3.9	1.2	3.8	ns	5, 9, 10 12, 15	3	1, 16	8	5, 9, 12, 15	2, 3
t_{PLH}	Propagation Delay Low to High	1.4	3.5	1.1	3.9	1.2	3.8	ns	5, 9, 10 12, 15	3	1, 16	8	5, 9, 12, 15	2, 3

MOTOROLA

Triple 4-3-3 Input Bus Driver

Military 10523

ELECTRICALLY TESTED PER:
MPG 10523

The 10523 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with V_{OL} = - 2.1 Vdc so that the bus may be terminated to - 2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the 10523 are "turned-off". This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to - 2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the 10523, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 2.

3

- 435 mW Max/Pkg (No Load)
- t_{pd} = 3.0 ns typ (1.5 Vdc in to 50% out)
- t_r, t_f = 2.5 ns typ (20% - 80%)

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10523/BXAJC
X = CASE OUTLINE AS FOLLOWS:

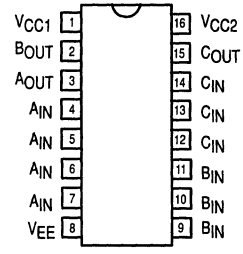
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

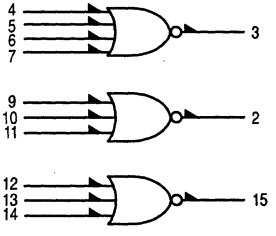
PIN ASSIGNMENTS

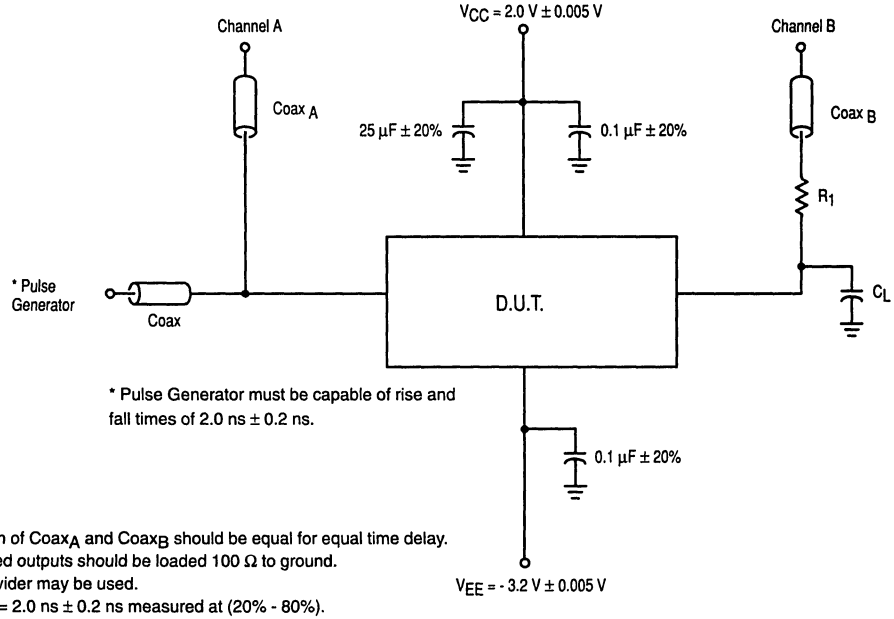
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
B_{OUT}	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	50 Ω to V_{TT}
A_{IN}	4	8	5	OPEN
A_{IN}	5	9	7	OPEN
A_{IN}	6	10	8	OPEN
A_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B_{IN}	9	13	12	OPEN
B_{IN}	10	14	13	OPEN
B_{IN}	11	15	14	OPEN
C_{IN}	12	16	15	OPEN
C_{IN}	13	1	17	OPEN
C_{IN}	14	2	18	OPEN
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN



LOGIC DIAGRAM





NOTES

1. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
2. Unused outputs should be loaded 100 Ω to ground.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 2.0 ns ± 0.2 ns measured at (20% - 80%).
5. $P_W \geq 20$ ns.
6. P_{RF} = 1.0 MHz.
7. R_1 = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
8. CL = Jig and stray capacitance ≤ 5.0 pF.

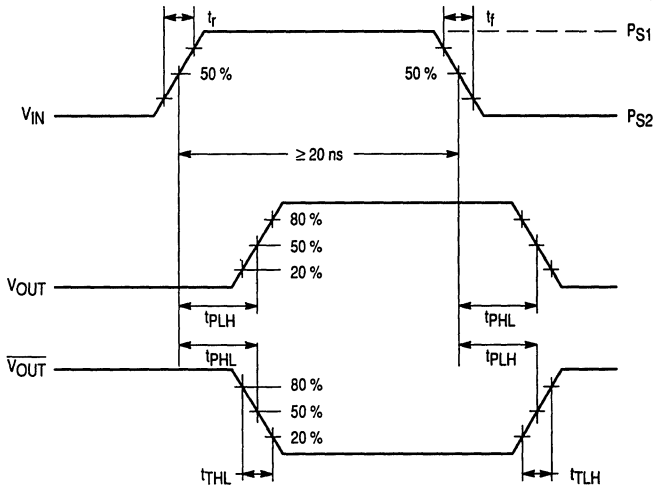


Figure 1. Switching Test Circuit and Waveforms

10523
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IL2}	V_{IH2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	– 0.78	– 1.85	– 1.475	– 1.105	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	– 0.63	– 1.82	– 1.400	– 1.000	+ 1.32	+ 0.445	- 5.2	- 3.2
T_A = - 55 °C	– 0.88	– 1.89	– 1.510	– 1.255	+ 1.30	+ 0.385	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V					8	1, 16	2, 3, 15
V_{OL}	Low Output Voltage	- 2.15	- 2.03	- 2.15	- 2.03	- 2.15	- 2.03	V	4 - 7, 9 - 15				8	1, 16	2, 3, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V				4 - 7, 9 - 15	8	1, 16	2, 3, 15
V_{OL1}	Low Output Voltage	- 2.15	- 1.60	- 2.15	- 1.525	- 2.15	- 1.635	V	4, 9, 12		4 - 7, 9 - 15		8	1, 16	2, 3, 15
I_{EE}	Power Supply Current	- 75		- 83		- 83		mA	4 - 7, 9 - 15				8	1, 16	8
I_{IH}	Input Current High		220		373		373	μA	4 - 7, 9 - 15				8	1, 16	4 - 7, 9 - 15
I_{IL}	Input Current Low	0.5		0.3		0.5		μA		4 - 7, 9 - 15			8	1, 16	4 - 7, 9 - 15

10523
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IL2}	V_{IH2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	− 0.78	− 1.85	− 1.475	− 1.105	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	− 0.63	− 1.82	− 1.400	− 1.000	+ 1.32	+ 0.445	- 5.2	- 3.2
T_A = - 55 °C	− 0.88	− 1.89	− 1.510	− 1.255	+ 1.30	+ 0.385	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW			
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = + 2.0 V, Output Load = 100 Ω to GND			
		Subgroup 9		Subgroup 10		Subgroup 11						
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.0	3.5	1.0	3.5	1.0	3.5	ns	4 - 7, 9 - 14	2, 3, 15	8	2, 3, 15
t_{THL}	Fall Time	1.0	3.5	1.0	3.5	1.0	3.5	ns	4 - 7, 9 - 14	2, 3, 15	8	2, 3, 15
t_{PHL}	Propagation Delay High to Low	1.2	4.4	1.2	6.0	1.2	4.4	ns	4 - 7, 9 - 14	2, 3, 15	8	2, 3, 15
t_{PLH}	Propagation Delay Low to High	1.2	4.4	1.2	6.0	1.2	4.4	ns	4 - 7, 9 - 14	2, 3, 15	8	2, 3, 15

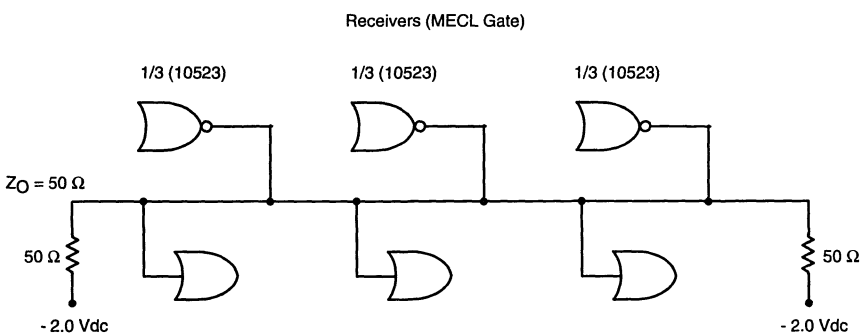


Figure 2. 50 Ohm Bus Driver

MOTOROLA

Quad TTL-to-MECL Translator

ELECTRICALLY TESTED PER:
MIL-M-38510/06301

The 10524 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The MECL 10524 has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the logic low level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, + 5.0 Volts, and – 5.2 Volts. Propagation delay of the 10524 is typically 3.5 ns. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by the 10515 or 10516 differential receivers. The 10524 is useful in computers, instrumentation, peripheral controllers, test equipment, and digital communication systems.

- 205 mW Max/Pkg (No Load)
- t_{pd} = 3.5 ns typ (1.5 Vdc in to 50% out)
- t_r, t_f = 2.5 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
B_{OUT}	1	5	2	50 Ω to V_{TT}
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{B_{OUT}}$	3	7	4	50 Ω to V_{TT}
$\overline{A_{OUT}}$	4	8	5	50 Ω to V_{TT}
A_{IN}	5	9	7	V_{CC}
Common Strobe	6	10	8	V_{CC}
B_{IN}	7	11	9	V_{CC}
V_{EE}	8	12	10	V_{EE}
V_{CC}	9	13	12	V_{CC}
C_{IN}	10	14	13	V_{CC}
D_{IN}	11	15	14	V_{CC}
$\overline{C_{OUT}}$	12	16	15	51 Ω to V_{TT}
$\overline{D_{OUT}}$	13	1	17	51 Ω to V_{TT}
D_{OUT}	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	GND
GND	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

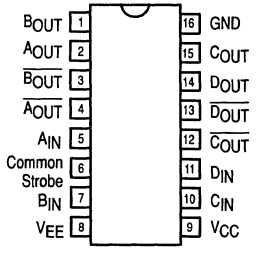
Military 10524

AVAILABLE AS

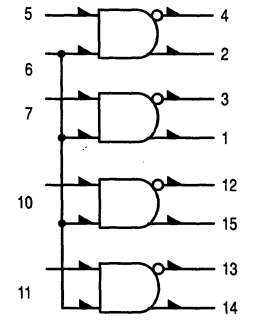
1) JAN: JM 38510/06301
2) SMD: N/A
3) 883: 10524/BXAJC
X = CASE OUTLINE AS FOLLOWS:

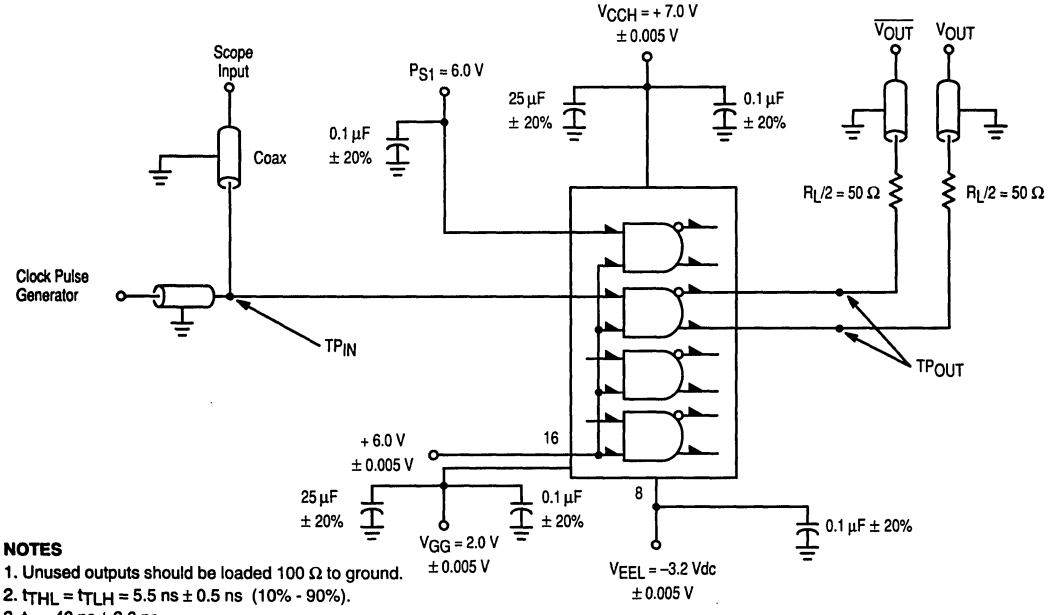
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. Unused outputs should be loaded 100 Ω to ground.
2. $t_{THL} = t_{TLH} = 5.5$ ns ± 0.5 ns (10% - 90%).
3. $t_p = 40$ ns ± 2.0 ns.
4. $Z_{OUT} \approx 50\ \Omega$.
5. C_L = Jig and stray capacitance ≤ 5.0 pF.

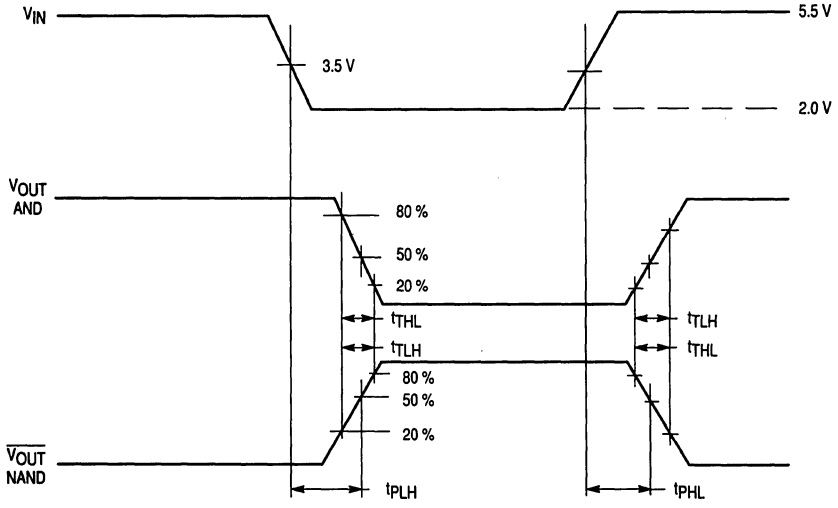


Figure 1. Switching Test Circuit and Waveforms

NOTES

1. 50 Ω termination to ground located in each scope channel input.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.

10524
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{ITL}	V_{ITH}	V_{CCH}	V_{GG}	V_{EE}	V_{EEL}
T_A = 25 °C	+ 2.4	+ 0.4	+ 1.10	+ 1.80	+ 7.0	+ 2.0	- 5.2	- 3.2
T_A = 125 °C	+ 2.4	+ 0.4	+ 0.80	+ 1.80	+ 7.0	+ 2.0	- 5.2	- 3.2
T_A = - 55 °C	+ 2.4	+ 0.4	+ 1.10	+ 2.00	+ 7.0	+ 2.0	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 5.0 V, I_{IN} = 10 mA, Output Load = 100 Ω to - 2.0 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	I_{IN}	GND	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.76	- 0.825	- 0.63	- 1.08	- 0.88	V	5, 6, 7, 10, 11	6				16	8	9	1 - 4, 12 - 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	5, 6, 7, 10, 11	6				16	8	9	1 - 4, 12 - 15
V_{OH1}	High Output Voltage	- 0.95		- 0.845		- 1.10		V	5, 6, 7, 10, 11		5, 6, 7, 10, 11	5, 6, 7, 10, 11		16	8	9	1 - 4, 12 - 15
V_{OL1}	Low Output Voltage		- 1.60		- 1.525		- 1.635	V	5, 6, 7, 10, 11		5, 6, 7, 10, 11	5, 6, 7, 10, 11		16	8	9	1 - 4, 12 - 15
I_{EE}	Power Supply Current	- 66		- 73		- 73		mA						16	8	9	8
I_{IH1}	Input Current High		50		85		85	µA	5, 7, 10, 11					6, 16	8	9	5, 7, 10, 11
I_{IL1}	Input Current Low	- 3.2		- 5.5		- 3.2		mA	6	5, 7, 10, 11				16	8	9	5, 7, 10, 11
I_{IH2}	Input Current High		200		340		340	µA	6					5, 7, 10, 11, 16	8	9	6
I_{IL2}	Input Current Low	- 12.8		- 22		- 12.8		mA		6				16	8	9	6
V_{IC}	Input Clamp Voltage	- 1.5						V					5 - 7 10, 11	16	8	9	5 - 7 10, 11

10524
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{ITL}	V_{ITH}	V_{CCH}	V_{GG}	V_{EE}	V_{EEL}
T_A = 25 °C	+ 2.4	+ 0.4	+ 1.10	+ 1.80	+ 7.0	+ 2.0	- 5.2	- 3.2
T_A = 125 °C	+ 2.4	+ 0.4	+ 0.80	+ 1.80	+ 7.0	+ 2.0	- 5.2	- 3.2
T_A = - 55 °C	+ 2.4	+ 0.4	+ 1.10	+ 2.00	+ 7.0	+ 2.0	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 5.0 V, I_{IN} = 1.0 mA, Output Load = 100 Ω to - 2.0 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	I_{IN}	GND	V_{EE}	V_{CC}	P. U. T.
I_{CCL} I_{CCH}	Positive Power Supply Current Drain		25 16		28 18		28 18	mA mA						5, 7, 10, 11, 16	8	5 - 7, 9, 10, 11	9
BV_{IN}	Input Breakdown Voltage	5.5		5.5		5.5		V		6			5 - 7 10, 11	16	8	9	5 - 7 10, 11

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 5.0 V, I_{IN} = - 10 mA or - 20 mA Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CCH}	V_{EEL}	V_{GG}	+ 6.0 V	P. U. T.
t_{TLH}	Rise Time	1.1	3.9	1.0	5.0	1.0	5.0	ns	5, 7, 10, 11	1 - 4 12 - 15	9	8	16	6	1 - 4 12 - 15
t_{THL}	Fall Time	1.1	3.9	1.0	5.0	1.0	5.0	ns	5, 7, 10, 11	1 - 4 12 - 15	9	8	16	6	1 - 4 12 - 15
t_{PHL}	Propagation Delay High to Low	1.0	6.0	1.0	8.0	1.0	8.0	ns	5, 7	1 - 4 10, 11	9, 12 - 15	8	16	6	1 - 4 12 - 15
t_{PLH}	Propagation Delay Low to High	1.0	6.0	1.0	8.0	1.0	8.0	ns	5, 7	1 - 4 10, 11	9, 12 - 15	8	16	6	1 - 4 12 - 15

Quad MECL-to-TTL Translator

Military 10525

ELECTRICALLY TESTED PER:
MIL-M-38510/06302

The 10525 is a quad translator for interfacing data and control signals between the MECL section and saturated logic section of digital systems. The 10525 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is available on pin 1 for use in single-ended input biasing. The outputs of the 10525 go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, + 5.0 Volts and – 5.2 Volts. Propagation delay of the 10525 is typically 4.5 ns. The 10525 has fanout of 10 TTL loads. The dc levels are MECL 10,000 in and Schottky TTL, or TTL out. This device has an input common mode noise rejection of ± 1.0 volt.

An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL logic from the noisy TTL environment. This device is useful in computers, instrumentation, peripheral controllers, test equipment and digital communications systems.

- 230 mW Max/Pkg (No Load)
- t_{pd} = 4.5 ns typ (50% to 1.5 Vdc out)
- t_r, t_f = 2.5 ns typ (1.0 V to 2.0V)

AVAILABLE AS

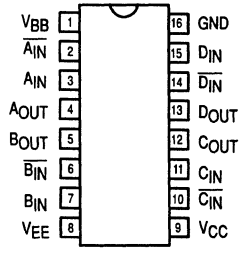
1) JAN: JM 38510/06302
2) SMD: N/A
3) 883: 10525/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

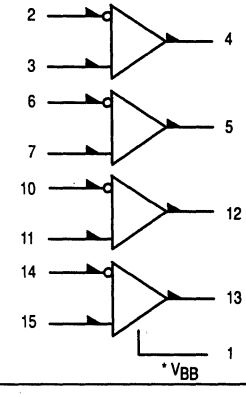
The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{BB}	1	5	2	V_{BB}
$\overline{A_{IN}}$	2	6	3	2 K Ω to V_{EE}
A_{IN}	3	7	4	V_{BB}
A_{OUT}	4	8	5	360 Ω to V_{CC}
B_{OUT}	5	9	7	360 Ω to V_{EE}
$\overline{B_{IN}}$	6	10	8	2 K Ω to V_{EE}
B_{IN}	7	11	9	V_{BB}
V_{EE}	8	12	10	V_{EE}
V_{CC}	9	13	12	V_{CC}
$\overline{C_{IN}}$	10	14	13	V_{BB}
C_{IN}	11	15	14	2 K Ω to V_{EE}
C_{OUT}	12	16	15	360 Ω to V_{EE}
D_{OUT}	13	1	17	360 Ω to V_{CC}
$\overline{D_{IN}}$	14	2	18	V_{BB}
D_{IN}	15	3	19	2 K Ω to GND
GND	16	4	20	GND



LOGIC DIAGRAM

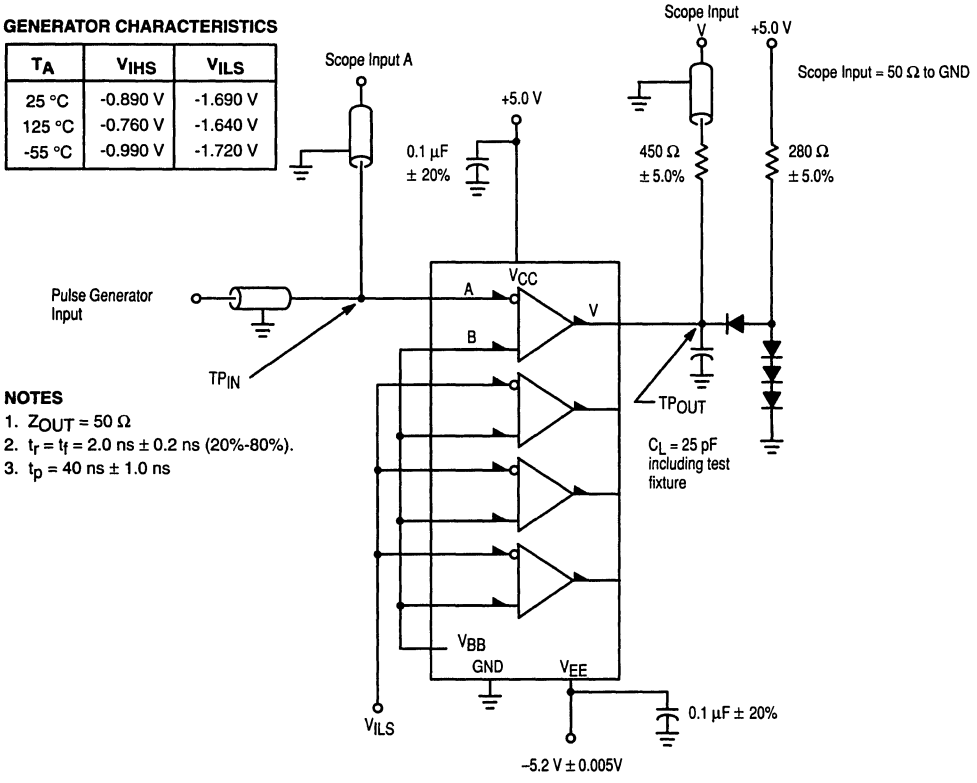


BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

*** V_{BB} to be used to supply bias to the 10525 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor.**
When the input pin with the bubble goes positive, the output goes negative.

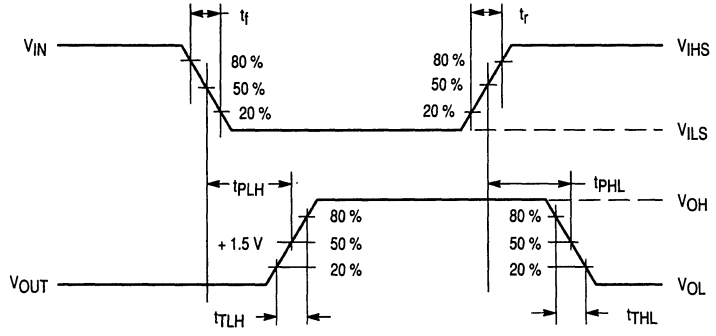
GENERATOR CHARACTERISTICS

T_A	V_{IHS}	V_{ILS}
25 °C	-0.890 V	-1.690 V
125 °C	-0.760 V	-1.640 V
-55 °C	-0.990 V	-1.720 V



NOTES

1. $Z_{OUT} = 50\ \Omega$
2. $t_r = t_f = 2.0$ ns ± 0.2 ns (20%-80%).
3. $t_p = 40$ ns ± 1.0 ns



NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cable. Wire length should be < 0.250 inch (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. All diodes are 1N3064 or equivalent.

Figure 1. Switching Test Circuit and Waveforms

10525
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)														Test Current Values (milliAmps)	
	V_{IH}	V_{IL}	V_{ITH}	V_{ITL}	V_{CB}	V_{EE}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{CC}	V_{BB}	V_{IHS}	V_{ILS}	I_{OH}	I_{OL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	- 5.2	- 5.2	+ 0.22	- 0.85	- 1.78	- 2.85	+ 5.0	Pin 1	- 0.89	- 1.69	- 2.0	+ 12.0
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	- 5.2	- 5.2	+ 0.37	- 0.82	- 1.63	- 2.82	+ 5.0	Pin 1	- 0.76	- 1.64	- 2.0	+ 12.0
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	- 5.2	- 5.2	+ 0.12	- 0.92	- 1.88	- 2.92	+ 5.0	Pin 1	- 0.99	- 1.72	- 2.0	+ 12.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW										
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments GND = Pin 16, Output Load = - 2.0 V										
		Subgroup 1		Subgroup 2		Subgroup 3													
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IHH}	V_{IHL}	V_{IL}	I_{OL}	I_{OH}	V_{ILL}	V_{ILH}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	2.5		2.5		2.5		V	3, 7, 11, 15	3, 7, 11, 15	3, 7, 11, 15	2, 3, 6, 7, 10, 11, 15		4, 5, 12, 13	2, 6, 10, 11, 14	2, 3, 6, 7, 10, 11, 14	8	9	4, 5, 12, 13
V_{OL}	Low Output Voltage		0.5		0.5		0.5	V	2, 3	2	2	3	4, 5, 12, 13		3	3	8	9	4, 5, 12, 13
V_{OLS}	Output Voltage		0.5		0.5		0.5	V					4, 5, 12, 13				2, 3, 6, 7, 8, 10, 11, 14	9	4, 5, 12, 13

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

10525
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)														Test Current Values (milliAmps)	
	V_{IH}	V_{IL}	V_{ITH}	V_{ITL}	V_{CB}	V_{EE}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{CC}	V_{BB}	V_{IHS}	V_{ILS}	I_{OH}	I_{OL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	- 5.2	- 5.2	+ 0.22	- 0.85	- 1.78	- 2.85	+ 5.0	Pin 1	- 0.89	- 1.69	- 2.0	+ 12.0
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	- 5.2	- 5.2	+ 0.37	- 0.82	- 1.63	- 2.82	+ 5.0	Pin 1	- 0.76	- 1.64	- 2.0	+ 12.0
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	- 5.2	- 5.2	+ 0.12	- 0.92	- 1.88	- 2.92	+ 5.0	Pin 1	- 0.99	- 1.72	- 2.0	+ 12.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = Pin 9, Output Load = - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{ITH}	V_{IL}	V_{ITL}	V_{BB}	V_{EE}	GND	I_{OL}	I_{OH}	P. U. T.
V_{OTH}	High Output Voltage	2.5		2.5		2.5		V		2, 6, 10, 14	2, 6, 10, 14	1, 3, 7, 11, 15	8	16		4, 5, 12, 13	4, 5, 12, 13
V_{OTL}	Low Output Voltage		0.5		0.5		0.5	V	2, 6, 10, 14	2, 6, 10, 14		1, 3, 7, 11, 15	8	16	4, 5, 12, 13		4, 5, 12, 13
V_{BB}	Reference Voltage	- 1.35	- 1.23	- 1.22	- 1.10	- 1.44	- 1.32	V				1, 3, 7, 11, 15	8	16			1
I_{EE}	Power Supply Current	- 40		- 44		- 40		mA				1, 3, 7, 11, 15	8	16			8
I_{CCL}	Positive Power Supply Drain Current		39		39		39	mA				1, 3, 7, 11, 15	8	16			9

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

10525
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)														Test Current Values (milliAmps)	
	V_{IH}	V_{IL}	V_{ITH}	V_{ITL}	V_{CB}	V_{EE}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{CC}	V_{BB}	V_{IHS}	V_{ILS}	I_{OH}	I_{OL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	- 5.2	- 5.2	+ 0.22	- 0.85	- 1.78	- 2.85	+ 5.0	Pin 1	- 0.89	- 1.69	- 2.0	+ 12.0
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	- 5.2	- 5.2	+ 0.37	- 0.82	- 1.63	- 2.82	+ 5.0	Pin 1	- 0.76	- 1.64	- 2.0	+ 12.0
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	- 5.2	- 5.2	+ 0.12	- 0.92	- 1.88	- 2.92	+ 5.0	Pin 1	- 0.99	- 1.72	- 2.0	+ 12.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = Pin 9, Output Load = - 2.0 V				
		Subgroup 1		Subgroup 2		Subgroup 3							
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{BB}	V_{EE}	GND	P. U. T.
I_{CCH}	Positive Power Supply Drain Current		52		52		52	mA	2, 6, 10, 14	1, 3, 7, 11, 15	8	16	9
I_{CBO}	Input Leakage Current	- 1.0		- 1.0		- 1.5		µA		1 - 3, 6, 7, 10, 11, 14, 15	2, 3, 6 - 8, 10, 11, 14, 15	16	2, 3, 6, 7, 10, 11, 14, 15
I_{OS}	Short Circuit Current	- 40	- 100	– 35	- 100	– 40	- 100	mA		1, 3, 7, 11, 15	8	4, 5, 12, 13	4, 5, 12, 13
I_{IH1}	Input Current High		115		196		196	µA	2, 3, 6, 7, 10, 11, 14, 15	1, 2, 3, 7, 10, 11, 14, 15		8, 16	2, 3, 6, 7, 10, 11, 14, 15

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

10525
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)														Test Current Values (milliAmps)	
	V_{IH}	V_{IL}	V_{ITH}	V_{ITL}	V_{CB}	V_{EE}	V_{IHH}	V_{ILH}	V_{IHL}	V_{ILL}	V_{CC}	V_{BB}	V_{IHS}	V_{ILS}	I_{OH}	I_{OL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	- 5.2	- 5.2	+ 0.22	- 0.85	- 1.78	- 2.85	+ 5.0	Pin 1	- 0.89	- 1.69	- 2.0	+ 12.0
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	- 5.2	- 5.2	+ 0.37	- 0.82	- 1.63	- 2.82	+ 5.0	Pin 1	- 0.76	- 1.64	- 2.0	+ 12.0
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	- 5.2	- 5.2	+ 0.12	- 0.92	- 1.88	- 2.92	+ 5.0	Pin 1	- 0.99	- 1.72	- 2.0	+ 12.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = Pin 9, GND = Pin 16, Output Load = See Figure 1.						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{BB}	P_{S2}	V_{EE}	V_{ILS}	P. U. T.
t_{TLH}	Rise Time		3.3		5.3		4.5	ns	2, 6, 10, 14	4, 5, 12, 13	1, 3, 7, 11, 15	10	8	2, 6, 10, 14	4, 5, 12, 13
t_{THL}	Fall Time		3.3		5.3		4.5	ns	2, 6, 10, 14	4, 5, 12, 13	1, 3, 7, 11, 15	10	8	2, 6, 10, 14	4, 5, 12, 13
t_{PHL}	Propagation Delay High to Low	1.0	6.0	1.0	7.0	1.0	6.5	ns	2, 6, 10, 14	4, 5, 12, 13	1, 3, 7, 11, 15	10	8	2, 6, 10, 14	4, 5, 12, 13
t_{PLH}	Propagation Delay Low to High	1.0	6.0	1.0	7.0	1.0	6.5	ns	2, 6, 10, 14	4, 5, 12, 13	1, 3, 7, 11, 15	10	8	2, 6, 10, 14	4, 5, 12, 13

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Dual Latch

ELECTRICALLY TESTED PER:
MPG 10530

The 10530 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the enable inputs for the clocking function. If the common clock is to be used to clock the latch, the Clock Enable ($\overline{C}_E$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\overline{C}$).

Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in information present at the data inputs will not affect the output information.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\overline{C}$ or $\overline{C}_E$ or both are high.

- 205 mW Max/Pkg (No Load)
- t_{pd} = 2.5 ns typ
- t_r, t_f = 2.7 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω TO V_{TT}
$\overline{Q_1}$	3	7	4	51 Ω TO V_{TT}
R_1	4	8	5	OPEN
S_1	5	9	7	OPEN
$\overline{C_{E1}}$	6	10	8	OPEN
D_1	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$\overline{C}$	9	13	12	OPEN
D_2	10	14	13	OPEN
$\overline{C_{E2}}$	11	15	14	OPEN
S_2	12	16	15	OPEN
R_2	13	1	17	OPEN
$\overline{Q_2}$	14	2	18	51 Ω TO V_{TT}
Q_2	15	3	19	51 Ω TO V_{TT}
V_{CC2}	16	4	20	GND

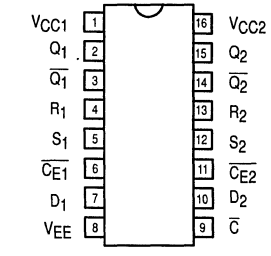
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

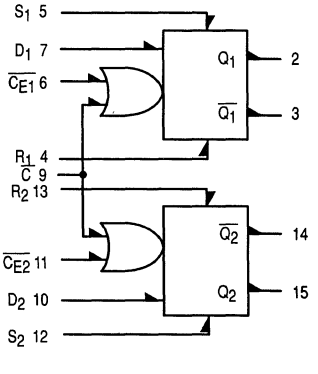
1) JAN: N/A
2) SMD: N/A
3) 883: 10530/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



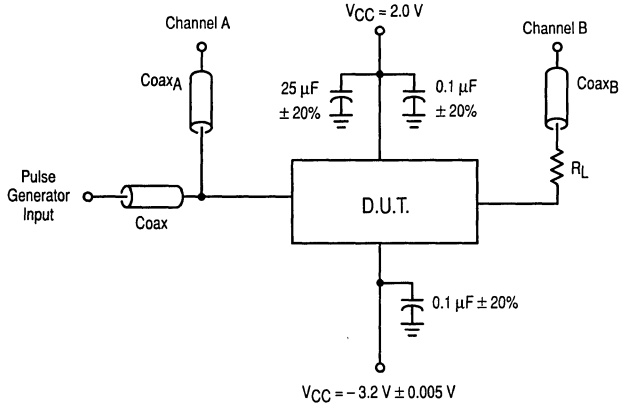
LOGIC DIAGRAM



TRUTH TABLE

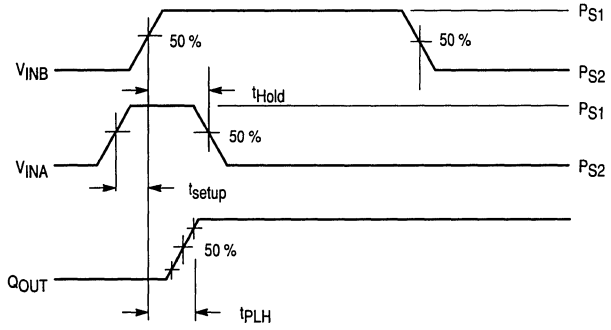
D	$\overline{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
Ø | L | H | Q_n |
Ø | H | L | Q_n |
Ø | H | H | Q_n |

Ø = Don't Care



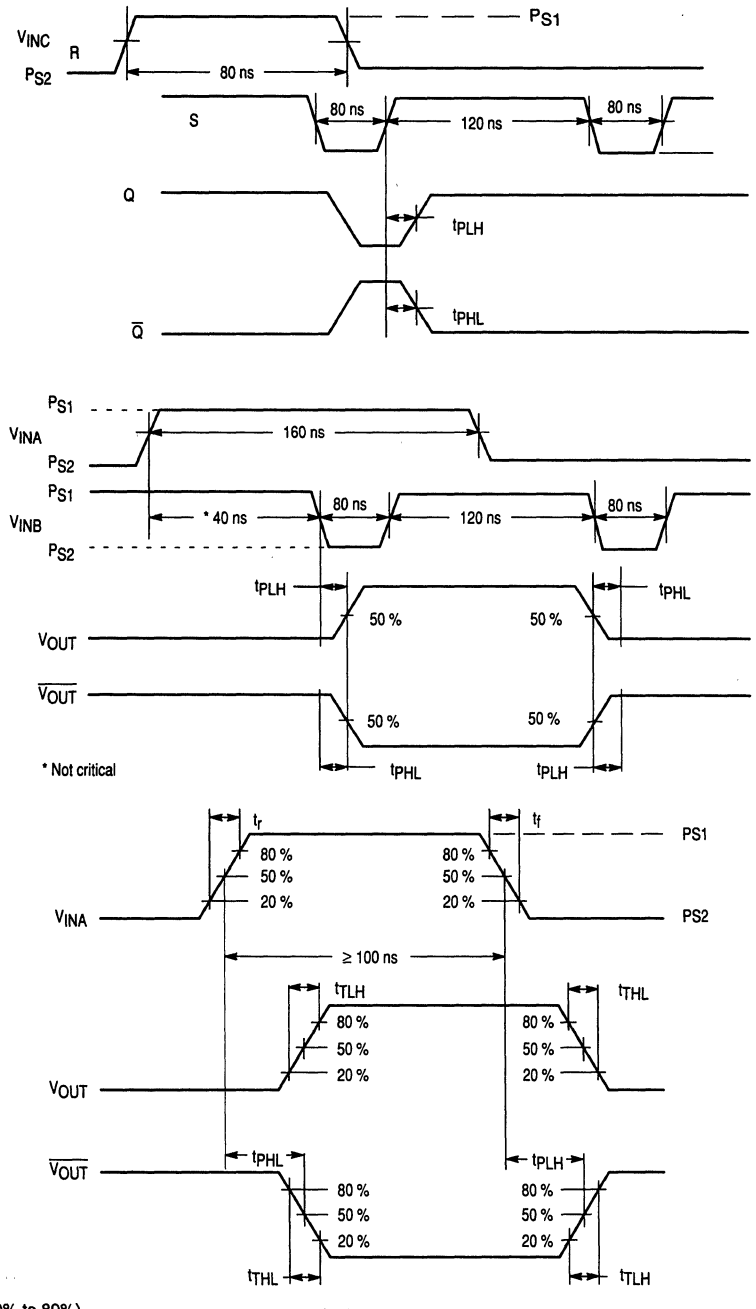
NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. 2:1 divider may be used.
5. R_L = 50 Ω resistor in series with a 50 Ω coax constitute the 100 Ω load.
6. Z_{OUT} = 50 Ω (20% to 80%).



t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).
t_{hold} is the minimum time before the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

Figure 1. Switching Test Circuit and Set/Reset Waveforms



NOTES
1. f = 2.0 MHz.
2. $t_r = t_f = 2.0$ ns (20% to 80%)

Figure 2. Switching Waveforms

10530
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4 - 7, 9 - 13	4 - 7, 9 - 13			8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4 - 7, 9 - 13	4 - 7, 9 - 13			8	1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	4, 5, 12, 13	4, 7, 9 - 13	4 - 7, 9 - 13	4 - 7, 9 - 13	8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	4, 7, 10, 13	4 - 7, 9 - 13	4 - 7, 9 - 13	4 - 7, 9 - 13	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	- 35		- 39		- 39		mA	9				8	1, 16	8
I_{IH}	Input Current High		220		375		375	µA	6, 11				8	1, 16	6, 11
I_{IH1}	Input Current High		265		450		450	µA	9				8	1, 16	9
I_{IH2}	Input Current High		285		485		485	µA	4 - 7, 10 - 13				8	1, 16	4 - 7, 10 - 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 13			8	1, 16	4 - 7, 9 - 13

10530
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.5	1.0	4.1	1.0	3.9	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	1.1	3.5	1.0	4.1	1.0	3.9	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{pd}	Propagation Delay Data to Output	1.0	3.5	1.0	4.1	1.0	3.9	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{pd}	Propagation Delay S/R to Output	1.0	3.5	1.0	4.1	1.0	3.9	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{pd}	Propagation Delay Clock to Output	1.0	4.0	1.0	4.7	1.0	4.3	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{set}	Setup Time	2.5		2.5		2.5		ns	6, 7, 10, 11	2, 15	1, 16	8	2, 15
t_{hold}	Hold Time	1.5		1.5		1.5		ns	6, 7, 10, 11	2, 15	1, 16	8	2, 15

MOTOROLA

Dual D Type Master Slave Flip-Flop

ELECTRICALLY TESTED PER:
MIL-M-38510/06101

The 10531 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable (C_E) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

- 325 mW Max/Pkg (No Load)
- f_{tog} = 125 MHz typ
- t_{pd} = 3.0 ns typ
- t_r, t_f = 2.5 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω TO V_{TT}
$\overline{Q_1}$	3	7	4	51 Ω TO V_{TT}
R_1	4	8	5	51 Ω TO V_{TT}
S_1	5	9	7	GND
$\overline{C_{E1}}$	6	10	8	OPEN
D_1	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
C_C	9	13	12	OPEN
D_2	10	14	13	OPEN
$\overline{C_{E2}}$	11	15	14	OPEN
S_2	12	16	15	GND
R_2	13	1	17	51 Ω TO V_{TT}
$\overline{Q_2}$	14	2	18	51 Ω TO V_{TT}
Q_2	15	3	19	51 Ω TO V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Military 10531

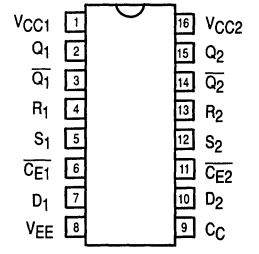
MPO

AVAILABLE AS

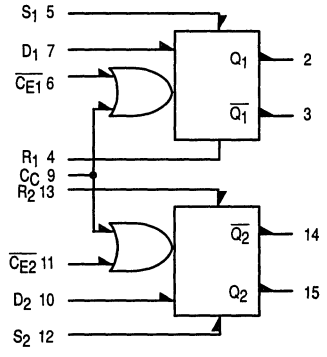
1) JAN: JM 38510/06101
2) SMD: N/A
3) 883: 10531/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



3

R-S TRUTH TABLE

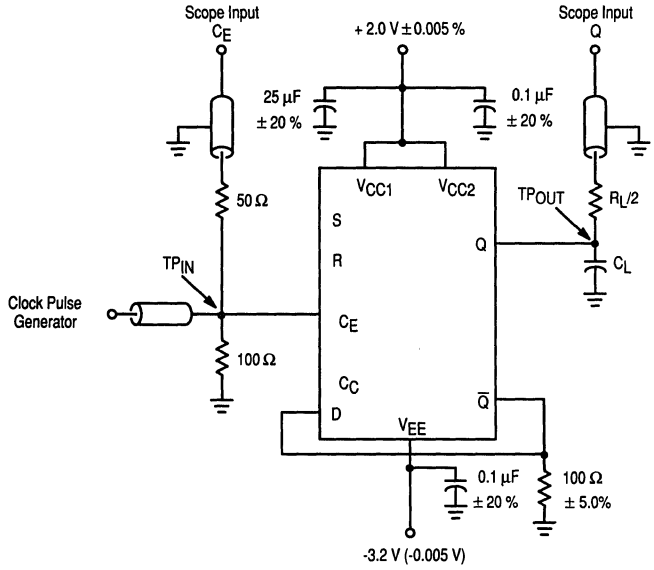
R	S	$Q_n + 1$
L	L	Q_n
L	H	H
H	L	L
H	H	N. D.

N. D. = Not Defined
A clock H is a clock transition from a Low to a High state

CLOCKED TRUTH TABLE

C	D	$Q_n + 1$
L	Ø	Q_n
H	L	L
H	H	H

Ø = Don't Care
$C = C_E + C_C$



NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2 = 50\ \Omega \pm 5.0\%$.
6. $t_r = t_f = 2.0$ ns (20% - 80%).
7. Scope Input = 50 Ω GND.
8. C_L (test Jig) ≤ 5.0 pF.

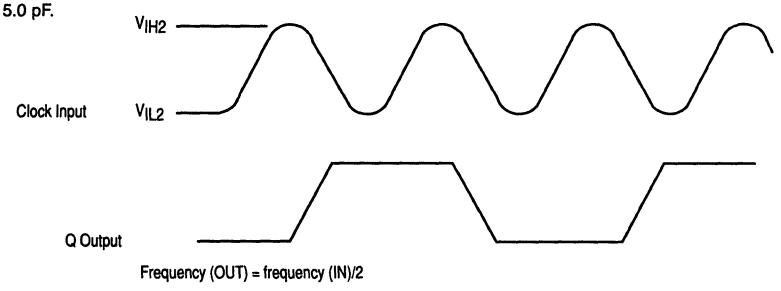
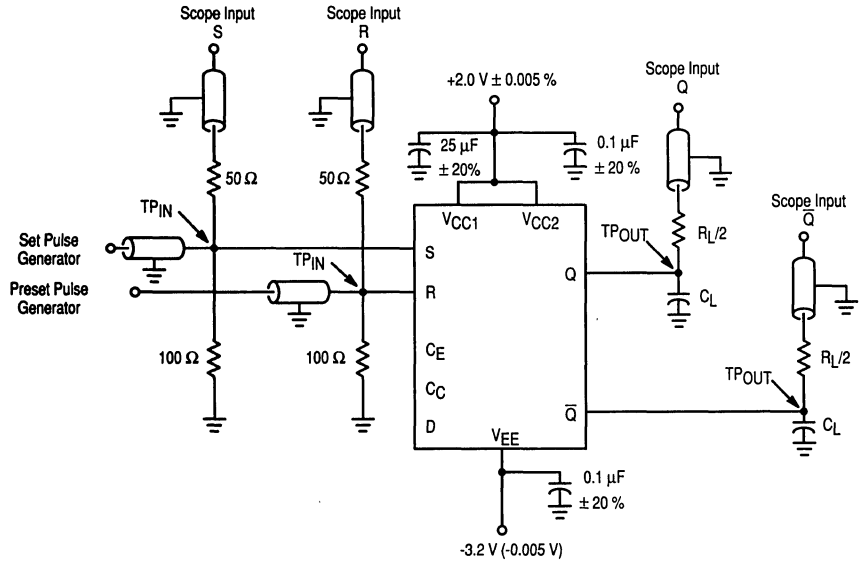
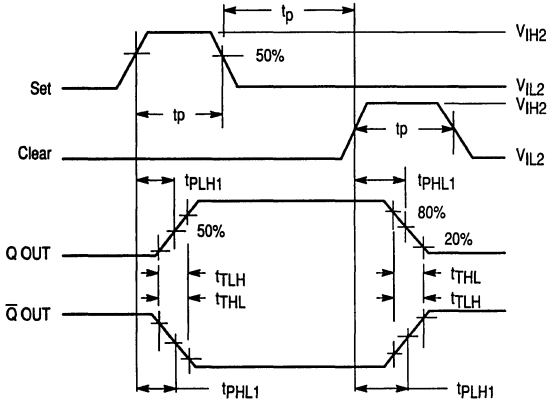


Figure 1. F_{MAX} Test Circuit and Clock Input Sinewave

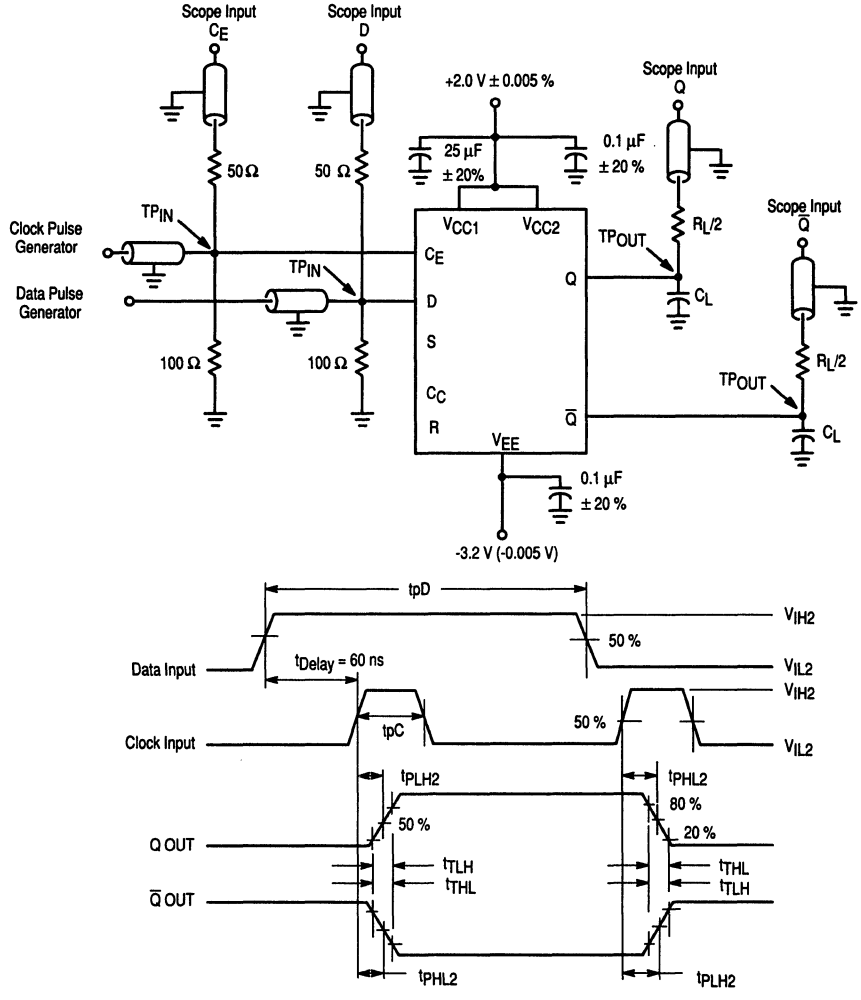




NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. Z_{OUT} = 50 Ω.
7. t_p (Set & Reset) = 40 ns.
8. PRR = 1.0 MHz.
9. Scope Input = 50 Ω to GND.
10. C_L (test Jig) ≤ 5.0 pF.

Figure 2. Set and Reset Switching Test Circuit



NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. Z_{OUT} = 50 Ω.
7. t_{pD}(Data) = 150 ns, t_{pC} (Clock) = 40 ns.
8. PRR = 1.0 MHz.
9. Scope Input = 50 Ω to GND.
10. C_L (test Jig) ≤ 5.0 pF.

Figure 3. Synchronous Switching Test Circuit and Waveform

10531
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{EE}	V_{EE1}
T_A = 25 °C	- 0.780	- 1.850	+ 1.11	+ 0.31	- 1.475	- 1.105	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	+ 1.24	+ 0.36	- 1.400	- 1.000	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	+ 1.01	+ 0.28	- 1.510	- 1.255	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4, 5, 12, 13	4 - 7, 9 - 13			8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4, 5, 12, 13	4 - 7, 9 - 13			8	1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	- 0.95		- 0.845		- 1.10		V	4, 5, 12, 13	4, 7, 9 - 13	4, 5, 12, 13	4 - 7, 9 - 13	8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage		- 1.60		- 1.525		- 1.635	V	4, 5, 12, 13	4 - 7, 9 - 13	4, 5, 12, 13	4 - 7, 9 - 13	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	- 56		- 62		- 62		mA					8	1, 16	8
I_{IH}	Input Current High		265		450		450	µA	9				8	1, 16	9
I_{IH1}	Input Current High		220		375		375	µA	6, 11				8	1, 16	6, 11
I_{IH2}	Input Current High		330		565		565	µA	4, 5, 12, 13				8	1, 16	4, 5, 12, 13
I_{IH3}	Input Current High		245		420		420	µA	7, 10				8	1, 16	7, 10
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 13			8	1, 16	4 - 7, 9 - 13

10531
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{EE}	V_{EE1}
T_A = 25 °C	- 0.780	- 1.850	+ 1.11	+ 0.31	- 1.475	- 1.105	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	+ 1.24	+ 0.36	- 1.400	- 1.000	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	+ 1.01	+ 0.28	- 1.510	- 1.255	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	4.5	1.1	4.9	1.0	4.6	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	1.1	4.5	1.1	4.9	1.0	4.6	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH1}	Propagation Delay	1.2	4.3	1.2	4.9	1.1	4.5	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH2}	Propagation Delay	1.5	4.5	1.5	5.0	1.4	4.6	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL1}	Propagation Delay	1.2	4.3	1.2	4.9	1.1	4.5	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL2}	Propagation Delay	1.5	4.5	1.5	5.0	1.4	4.6	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
f_{tog}	Toggle Frequency (max)	125		125		105		MHz	6, 11	2, 15	1, 16	8	2, 3, 14, 15

Quad Latch

ELECTRICALLY TESTED PER:
MPG 10533

The 10533 is a high speed, low power, quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on the negative going transition of the clock.

The outputs are gated when the output enable ($\overline{G}$) is low. All four latches may be clocked at one time with the common clock (C_C), or each half may be clocked separately with its clock enable ($\overline{CE}$).

- 435 mW Max/Pkg (No Load)
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_0	2	6	3	51 Ω TO V_{TT}
D0	3	7	4	GND
$\overline{CE}$	4	8	5	OPEN
$\overline{G0}$	5	9	7	OPEN
Q1	6	10	8	OPEN
D1	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
D	9	13	12	GND
$\overline{G1}$	10	14	13	OPEN
Q2	11	15	14	51 Ω TO V_{TT}
$\overline{CE}$	12	16	15	OPEN
C_C	13	1	17	GND
D3	14	2	18	GND
Q3	15	3	19	51 Ω TO V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	Ø	Ø	L
L	L	Ø	Q_n
L	H	L	L
L	H	H	H

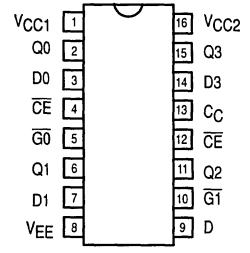
Ø = Don't Care
C = C_C + CE

AVAILABLE AS

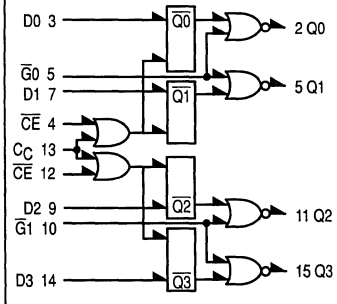
1) JAN: N/A
2) SMD: N/A
3) 883: 10533/BXAJC
X = CASE OUTLINE AS FOLLOWS:

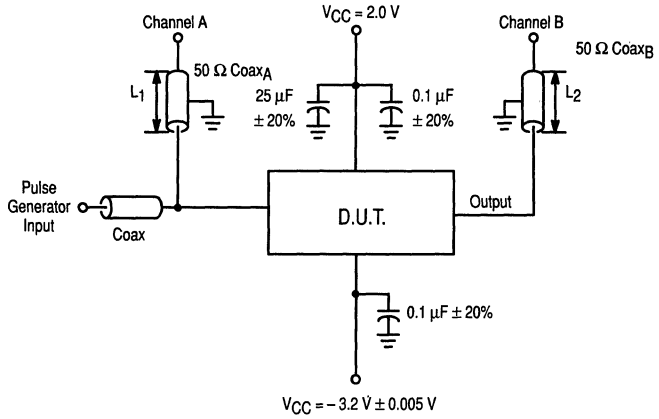
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





3

NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. 2:1 divider may be used.
3. L_1 = L_2 : Matched for equal time delays.
4. V_{IN} = has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.
5. Unused outputs should be loaded 100.Ω to Gnd.

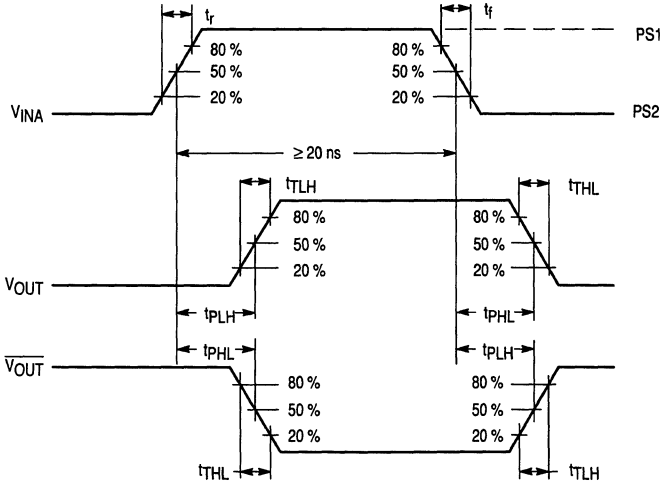
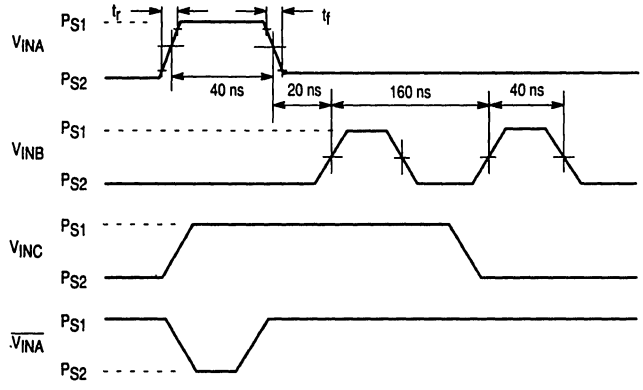
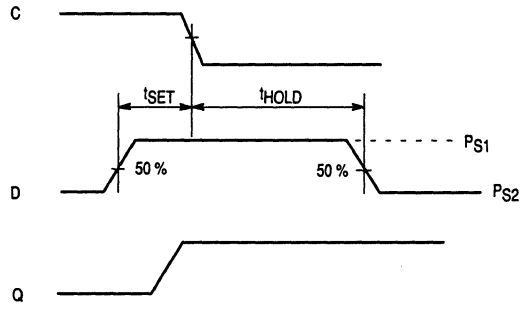


Figure 1. Switching Test Circuit and Set/Reset Waveforms

SWITCHING WAVEFORMS





NOTES

1. V_{IN} has the following characteristics:
   a) Pulse width ≥ 40 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns (20% to 80%)

Figure 2. t_{SETUP} and t_{HOLD} Waveforms

10533
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	3, 7, 9, 12 - 14				8	1, 16	2, 6, 11, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	3, 4, 5, 7, 9, 10, 12 - 14				8	1, 16	2, 6, 11, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	3, 4, 7, 9, 12, 14		5, 10	3, 7, 13, 14	8	1, 16	2, 6, 11, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	3, 4, 7, 9, 12, 14	3, 4, 7, 9, 12, 14	3, 4, 7, 9, 12, 14		8	1, 16	2, 6, 11, 15
I_{IH1}	Input Current High		350		595		595	µA	5, 10				8	1, 16	5, 10
I_{IH2}	Input Current High		245		415		415	µA	7, 9, 14				8	1, 16	7, 9, 14
I_{IH3}	Input Current High		265		450		450	µA	4, 12				8	1, 16	4, 12
I_{IH4}	Input Current High		350		595		595	µA	13				8	1, 16	13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 5, 7, 9, 10, 12 - 14			8	1, 16	3 - 5, 7, 9, 10, 12 - 14
I_{EE}	Power Supply Current	- 75	-7	- 83	-8	- 83	-8	mA		13			8	1, 16	8

10533
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.5	1.0	4.1	1.0	3.9	ns	3 - 5, 7, 9, 10, 12, 14	2, 6, 11, 15	1, 16	8	3, 9, 14	5, 10, 13	2, 6, 11, 15
t_{THL}	Fall Time	1.1	3.5	1.0	4.1	1.0	3.9	ns	3 - 5, 7, 9, 10, 12, 14	2, 6, 11, 15	1, 16	8	3, 9, 14	5, 10, 13	2, 6, 11, 15
t_{PLH}/ t_{PHL}	Propagation Delay Clock to Output	1.0	5.4	1.0	6.3	1.0	5.8	ns	3 - 5, 7, 9, 10, 12, 14	2, 6, 11, 15	1, 16	8	3, 9, 14	5, 10, 13	2, 6, 11, 15
t_{PLH}/ t_{PHL}	Propagation Delay Data to Output	1.0	5.4	1.0	6.3	1.0	5.8	ns	3 - 5, 7, 9, 10, 12, 14	2, 6, 11, 15	1, 16	8	3, 9, 14	5, 10, 13	2, 6, 11, 15
t_{PLH}/ t_{PHL}	Propagation Delay Gate to Output	1.0	3.1	1.0	3.6	1.0	3.3	ns	3 - 5, 7, 9, 10, 12, 14	2, 6, 11, 15	1, 16	8	3, 9, 14	5, 10, 13	2, 6, 11, 15
t_{set}	Setup Time	2.5		2.5		2.5		ns	3, 4, 7, 9, 12, 14	2, 6, 11	1, 16	8			2, 6, 11, 15
t_{hold}	Hold Time	1.5		1.5		1.5		ns	3, 4, 7, 9, 12, 14	2, 6, 11	1, 16	8			2, 6, 11, 15

MOTOROLA

Dual J-K Master Slave Flip-Flop

ELECTRICALLY TESTED PER:
MIL-M-38510/06104

The 10535 is a dual master-slave dc coupled J-K flip-flop. Asynchronous Set (S) and Reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate $\overline{J}$-$\overline{K}$ inputs. When the clock is static, the $\overline{J}$-$\overline{K}$ inputs do not effect the output.

The output states of the flip-flop change on the positive transition of the clock.

- 390 mW Max/Pkg (No Load)
- f_{tog} = 120 MHz typ
- t_{pd} = 3.0 ns typ
- t_r, t_f = 2.5 ns typ (20% - 80%)

3

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω TO V_{TT}
$\overline{Q_1}$	3	7	4	51 Ω TO V_{TT}
R_1	4	8	5	51 Ω TO V_{TT}
S_1	5	9	7	GND
$\overline{K_1}$	6	10	8	OPEN
$\overline{J_1}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
C	9	13	12	OPEN
$\overline{J_2}$	10	14	13	OPEN
$\overline{K_2}$	11	15	14	OPEN
S_2	12	16	15	GND
R_2	13	1	17	51 Ω TO V_{TT}
$\overline{Q_2}$	14	2	18	51 Ω TO V_{TT}
Q_2	15	3	19	51 Ω TO V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

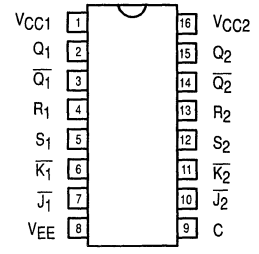
Military 10535

AVAILABLE AS

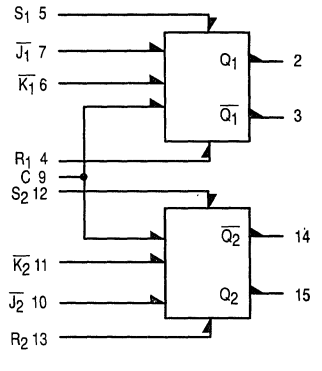
1) JAN: JM 38510/06104
2) SMD: N/A
3) 883: 10535/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



R-S TRUTH TABLE

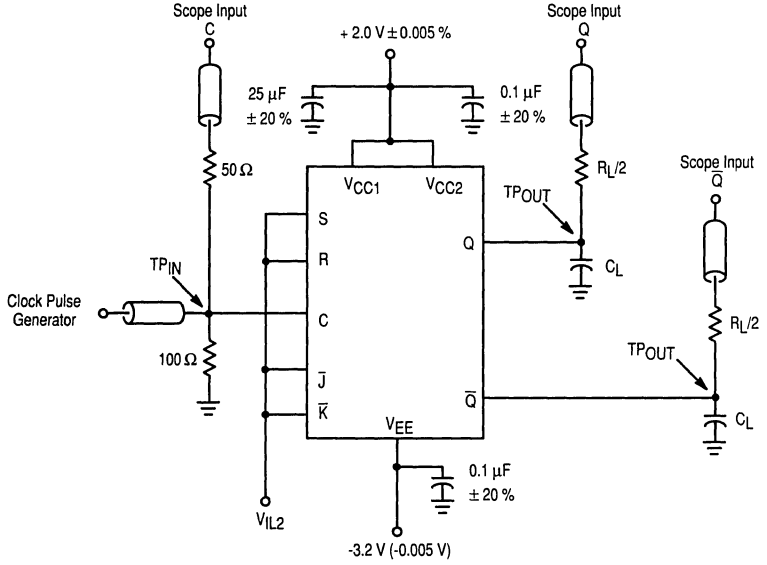
R	S	$Q_n + 1$
L	L	Q_n
L	H	H
H	L	L
H	H	N. D.

N. D. = Not Defined
A clock H is a clock transition from a Low to a High state

CLOCKED TRUTH TABLE *

$\overline{J}$	$\overline{K}$	$Q_n + 1$
L	L	Q_n
H	L	L
L	H	H
H	H	Q_n

* Output states change on positive transition of clock for $\overline{J}$-$\overline{K}$ input condition preset



NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables.
   Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. $t_r = t_f$ = 2.0 ns (20% - 80%).
7. Scope Input = 50 Ω GND.
8. C_L (test Jig) ≤ 5.0 pF.

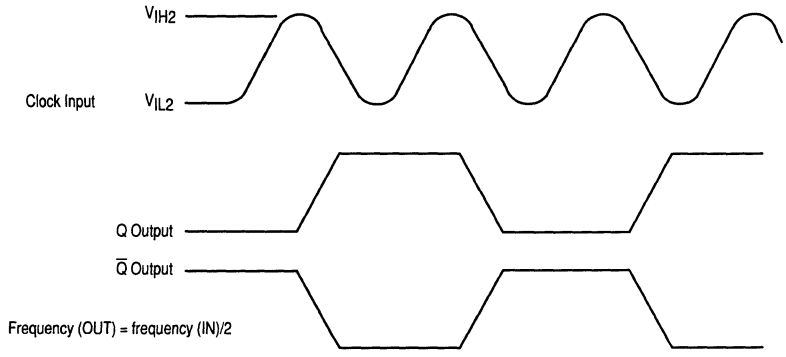
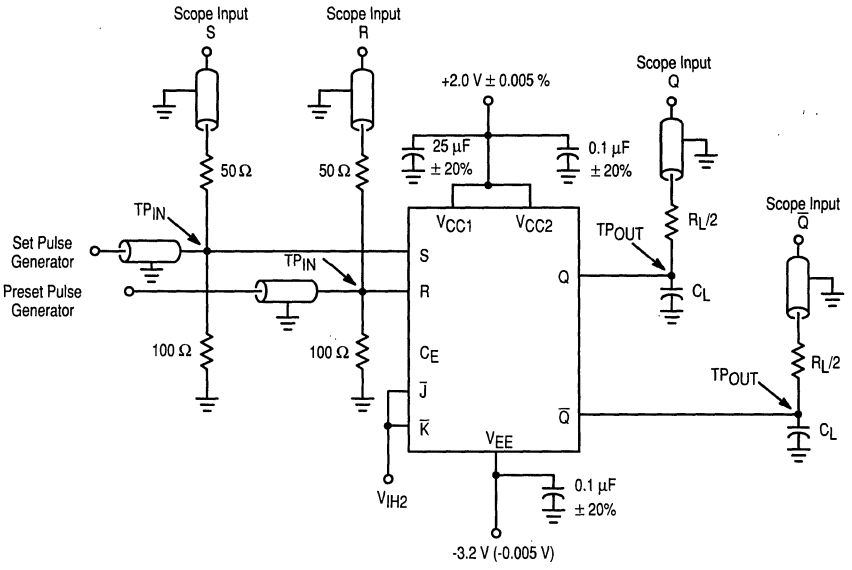
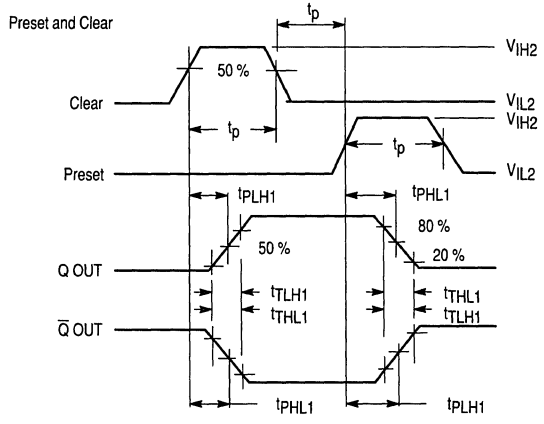


Figure 1. F_{MAX} Test Circuit and Clock Input Sinewave

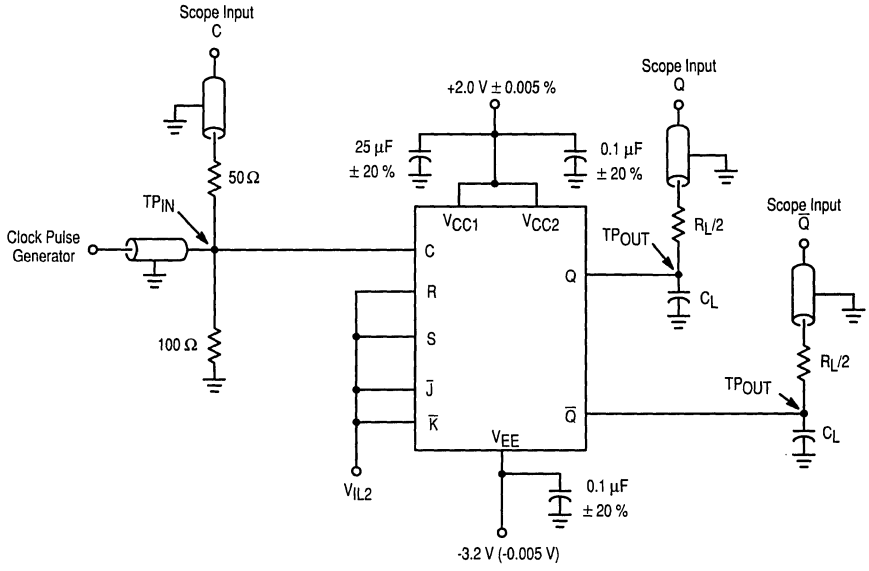


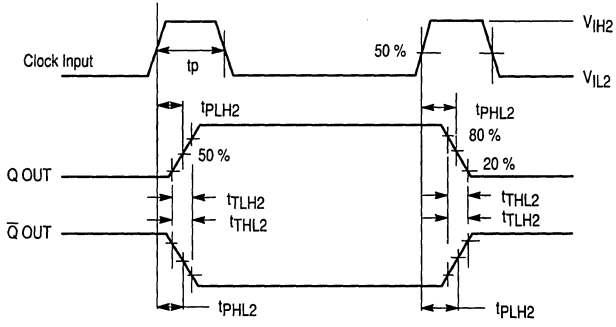


NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. Z_{OUT} = 50 Ω.
7. t_p (Set & Reset) = 40 ns.
8. PRR = 1.0 MHz.
9. $t_r = t_f$ = 2.0 ns (20% - 80%).
10. Scope Input = 50 Ω to GND.
11. C_L (test Jig) ≤ 5.0 pF.

Figure 2. Preset and Clear Switching Test Circuit

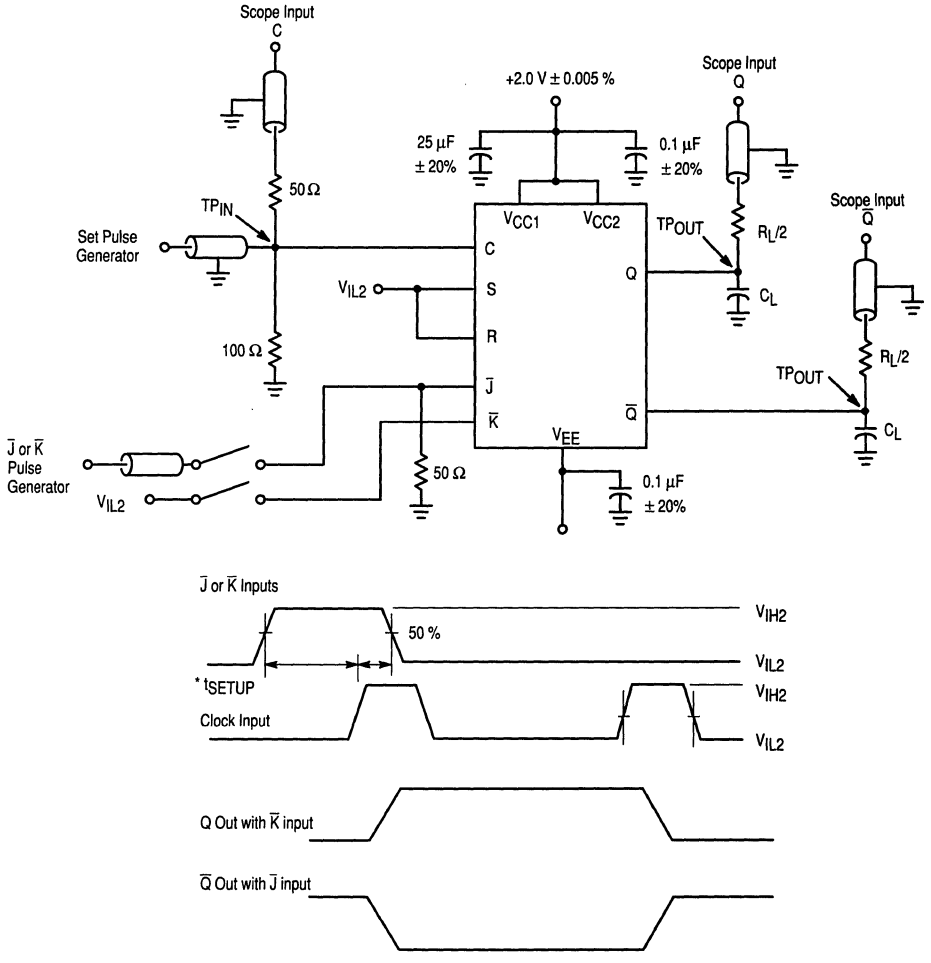




NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. Z_{OUT} = 50 Ω.
7. t_p (Clock) = 40 ns.
8. PRR = 1.0 MHz.
9. $t_r = t_f$ = 2.0 ns (20% - 80%).
10. Scope Input = 50 Ω to GND.
11. C_L (test Jig) ≤ 5.0 pF.

Figure 3. Synchronous Switching Test Circuit and Waveform



NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2 = 50\ \Omega \pm 5.0\%$.
6. $Z_{OUT} = 50\ \Omega$.
7. $t_{THL} = t_{TLH} = 2.0$ ns (20% - 80%).
8. Scope Input = 50 Ω to GND.
9. C_L (test Jig) ≤ 5.0 pF.
* 10. For information only; not tested: $t_{setup} \geq 1.0$ ns, $t_{hold} \geq 0.75$ ns.

Figure 4. Setup and Hold Test Circuit and Waveform

10535
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{EE}	V_{EE1}
T_A = 25 °C	- 0.780	- 1.850	+ 1.11	+ 0.31	- 1.475	- 1.105	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	+ 1.24	+ 0.36	- 1.400	- 1.000	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	+ 1.01	+ 0.28	- 1.510	- 1.255	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4, 5, 12, 13				8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4, 5, 12, 13				8	1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	- 0.95		- 0.845		- 1.10		V	4, 5, 12, 13	4, 7, 9 - 13	4, 5, 12, 13	4 - 7, 9 - 13	8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage		- 1.60		- 1.525		- 1.635	V	4, 5, 12, 13	4 - 7, 9 - 13	4, 5, 12, 13	4 - 7, 9 - 13	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	- 66		- 75		- 75		mA					8	1, 16	8
I_{IH}	Input Current High		265		450		450	µA	6, 7, 9 - 11				8	1, 16	6, 7, 9 - 11
I_{IH1}	Input Current High		390		665		665	µA	4, 5, 12, 13				8	1, 16	4, 5, 12, 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 13			8	1, 16	4 - 7, 9 - 13

10535
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{EE}	V_{EE1}
T_A = 25 °C	- 0.780	- 1.850	+ 1.11	+ 0.31	- 1.475	- 1.105	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	+ 1.24	+ 0.36	- 1.400	- 1.000	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	+ 1.01	+ 0.28	- 1.510	- 1.255	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IH2}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH1} t_{THL1}	Rise Time 1 or Fall Time 1	1.1	4.5	1.0	5.3	1.0	4.8	ns	6, 7	4, 5, 10, 11, 12, 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{TLH1} t_{THL1}	Rise Time 2 or Fall Time 2	1.1	4.5	1.0	5.3	1.0	4.8	ns		9	2, 3, 14, 15	1, 16	8	2, 3, 14, 15, 10 - 13
t_{PLH1}	Propagation Delay 1	1.01	5.0	1.0	5.9	1.0	5.4	ns	6, 7, 10, 11	4, 5, 12, 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL1}	Propagation Delay 1	1.01	5.0	1.0	5.9	1.0	5.4	ns	6, 7, 10, 11	4, 5, 12, 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH2}	Propagation Delay 2	1.0	4.5	1.0	5.3	1.0	4.8	ns	6, 7, 10, 11	4, 5, 12, 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL2}	Propagation Delay 2	1.0	4.5	1.0	5.3	1.0	4.8	ns	6, 7, 10, 11	4, 5, 12, 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
f_{tog}	Toggle Frequency	125		115		105		MHz		9	2, 15	1, 16	8	2, 15

MOTOROLA

Universal Hexadecimal Counter

ELECTRICALLY TESTED PER:
5962-8774501

The 10536 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the 10536 suitable for either computers or instrumentation.

Three control lines (S1, S2, and Carry In) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count, or when the counter is being preset.

This device is not designed for use with gated clocks, Control is via S1 and S2.

- 720 mW Typ/Pkg (No Load)
- f_{COUNT} = 120 MHz typ
- t_{pd} = 3.3 ns typ (C - Q)
  = 7.0 ns typ (C - C_{OUT})
  = 5.0 ns typ (C_{IN} - C_{OUT})

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_2	2	6	3	51 Ω TO V_{TT}
Q_3	3	7	4	51 Ω TO V_{TT}
$\overline{C_{OUT}}$	4	8	5	51 Ω TO V_{TT}
D_3	5	9	7	GND
D_2	6	10	8	GND
S2	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
S1	9	13	12	OPEN
$\overline{C_{IN}}$	10	14	13	OPEN
D_1	11	15	14	GND
D_0	12	16	15	GND
CLK	13	1	17	CP1
Q_0	14	2	18	51 Ω TO V_{TT}
Q_1	15	3	19	51 Ω TO V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

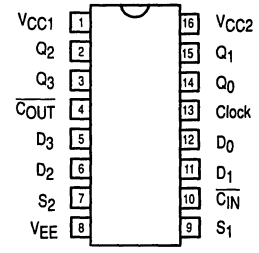
Military 10536

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8774501
3) 883: 10536/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



3

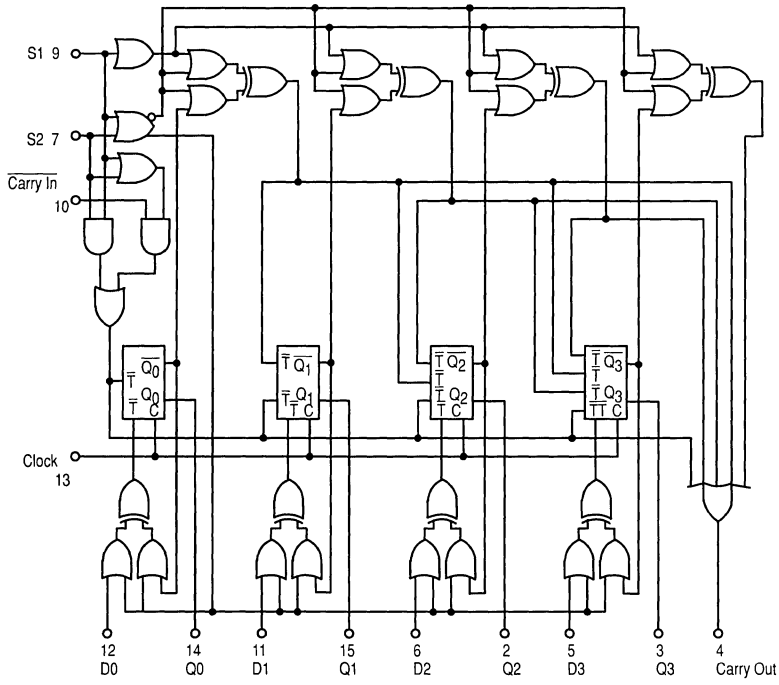
FUNCTION SELECT TABLE			
C_{IN}	S_1	S_2	OPERATING MODE
Ø	L	L	Preset (Program)
L	L	H	Increment (Count Up)
H	L	H	Hold Count
L	H	L	Decrement (Count Down)
H	H	L	Hold Count
Ø	H	H	Hold (Stop Count)

SEQUENTIAL TRUTH TABLE •												
S_1	S_2	D_0	D_1	D_2	D_3	$\overline{\text{Carry IN}}$	Clock ••	Q_0	Q_1	Q_2	Q_3	$\overline{\text{Carry OUT}}$
L	L	L	L	H	H	Ø	H	L	L	H	H	L
L	H	Ø	Ø	Ø	Ø	L	H	H	L	H	H	H
L	H	Ø	Ø	Ø	Ø	L	H	L	H	H	H	H
L	H	Ø	Ø	Ø	Ø	L	H	H	H	H	H	L
L	H	Ø	Ø	Ø	Ø	H	L	H	H	H	H	H
L	H	Ø	Ø	Ø	Ø	H	H	H	H	H	H	H
H	H	Ø	Ø	Ø	Ø	Ø	H	H	H	H	H	H
L	L	H	H	L	L	Ø	H	H	H	L	L	L
H	L	Ø	Ø	Ø	Ø	L	H	L	H	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	H	L	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	L	L	L	L	L
H	L	Ø	Ø	Ø	Ø	L	H	H	H	H	H	H

Ø = Don't Care

• Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

•• A clock H is defined as a clock input transition from a low to a high logic level.



NOTE:
FLIP FLOPS WILL TOGGLE WHEN
ALL $\overline{T}$ INPUTS ARE LOW.

Figure 1. Logic Diagram

10536
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	5 - 7, 9, 11 - 13	13			8	1, 16	2, 3, 4, 14, 15
V_{OL}	Low Output Voltage	- 1.93	- 1.62	- 1.90	- 1.545	- 2.00	- 1.655	V	13				8	1, 16	2, 3, 4, 14, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V					8	1, 16	2, 3, 4, 14, 15
V_{OL1}	Low Output Voltage	- 1.93	- 1.60	- 1.90	- 1.525	- 2.00	- 1.635	V					8	1, 16	2, 3, 4, 14, 15
I_{EE}	Power Supply Current	- 125		- 138		- 138		mA					8	1, 16	8
I_{IH}	Input Current High		220		375		375	µA	5, 6, 11, 12				8	1, 16	5, 6, 11, 12
I_{IH1}	Input Current High		245		415		415	µA	9, 10				8	1, 16	9, 10
I_{IH2}	Input Current High		265		450		450	µA	7				8	1, 16	7
I_{IH3}	Input Current High		290		495		495	µA	13				8	1, 16	13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 10 - 13			8	1, 16	5 - 7, 10 - 13

10536
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.2	3.7	0.9	3.3	ns	12, 13	4	1, 16	8	7	5, 6, 9 - 12	2, 3, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.2	3.7	0.9	3.3	ns	12, 13	4	1, 16	8	7	5, 6, 9 - 12	2, 3, 14, 15
t_{pd}	Propagation Delay CLK to Q CLK to Carry Out Carry In to Carry Out	1.0 2.5 1.6	4.5 10.5 6.9	1.4 2.4 1.9	5.2 12.6 7.6	0.8 2.0 1.6	4.6 11.0 7.1	ns ns ns	12, 13 12, 13 12, 13	4, 14 4, 14 4, 14	1, 16 1, 16 1, 16	8 8 8	6, 7 6, 7 6, 7	5 - 7, 9 - 11 5 - 7, 9 - 11 5 - 7, 9 - 11	2, 3, 14, 15 2, 3, 14, 15 2, 3, 14, 15
t_{set}	Setup Time Data (D_0 to C) Select (S to C) Carry In (C_{IN} to C) (C to $\overline{C_{IN}}$)	3.5 7.5 2.5 0		3.5 7.5 2.5 0		3.5 7.5 2.5 0		ns ns ns ns	10, 13 10, 13 10, 13 10, 13	14 14 14 14	1, 16 1, 16 1, 16 1, 16	8 8 8 8	7 7 7 7	5, 6, 9, 11, 12 5, 6, 9, 11, 12 5, 6, 9, 11, 12 5, 6, 9, 11, 12	2, 3, 14, 15 2, 3, 14, 15 2, 3, 14, 15 2, 3, 14, 15
t_{hold}	Hold Time Data (D_0 to C) Select (S to C) Carry In (C_{IN} to C) (C to $\overline{C_{IN}}$)	0 – 1.0 0 1.5		10 – 1.0 0 1.5		0 – 1.0 0 1.5		ns ns ps ns	10, 13 10, 13 10, 13 10, 13	14 14 14 14	1, 16 1, 16 1, 16 1, 16	8 8 8 8	7 7 7 7	5, 6, 9, 11, 12 5, 6, 9, 11, 12 5, 6, 9, 11, 12 5, 6, 9, 11, 12	2, 3, 14, 15 2, 3, 14, 15 2, 3, 14, 15 2, 3, 14, 15
f_{tog}	Toggle Frequency	125		115		115		MHz	13	14	1, 16	8	9	5, 6, 9 - 12	2, 3, 14, 15

MOTOROLA

Universal Decade Counter

Military 10537

ELECTRICALLY TESTED PER:
MPG 10537

The 10537 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications. The synchronous count feature makes the 10537 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter.

$\overline{\text{Carry out}}$ goes low on the terminal count. The $\overline{\text{Carry Out}}$ on the 10537 is partially decoded from Q1 and Q2 directly, so in the preset mode the condition of the $\overline{\text{Carry Out}}$ after Clock's positive excursion will depend on the condition of Q1 and/or Q2. The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is as shown in the State Diagrams.

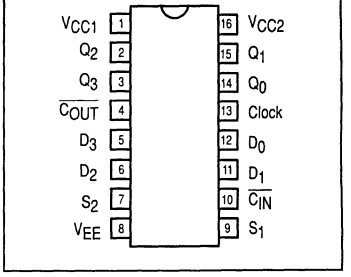
- 860 mW Typ/Pkg (No Load)
- f_{COUNT} = 150 MHz typ
- t_{pd} = 3.3 ns typ (C - Q)
  = 7.0 ns typ (C - $\overline{C_{OUT}}$)
  = 5.0 ns typ ($\overline{C_{IN}}$ - $\overline{C_{OUT}}$)

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10537/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



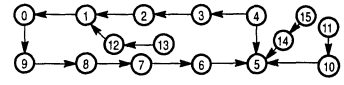
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_2	2	6	3	51 Ω TO V_{TT}
Q_3	3	7	4	51 Ω TO V_{TT}
$\overline{C_{OUT}}$	4	8	5	51 Ω TO V_{TT}
D_3	5	9	7	GND
D_2	6	10	8	GND
S2	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
S1	9	13	12	OPEN
$\overline{C_{IN}}$	10	14	13	OPEN
D_1	11	15	14	GND
D_0	12	16	15	GND
CLK	13	1	17	CP1
Q_0	14	2	18	51 Ω TO V_{TT}
Q_1	15	3	19	51 Ω TO V_{TT}
V_{CC2}	16	4	20	GND

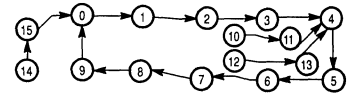
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

STATE DIAGRAMS

COUNTDOWN



COUNTUP



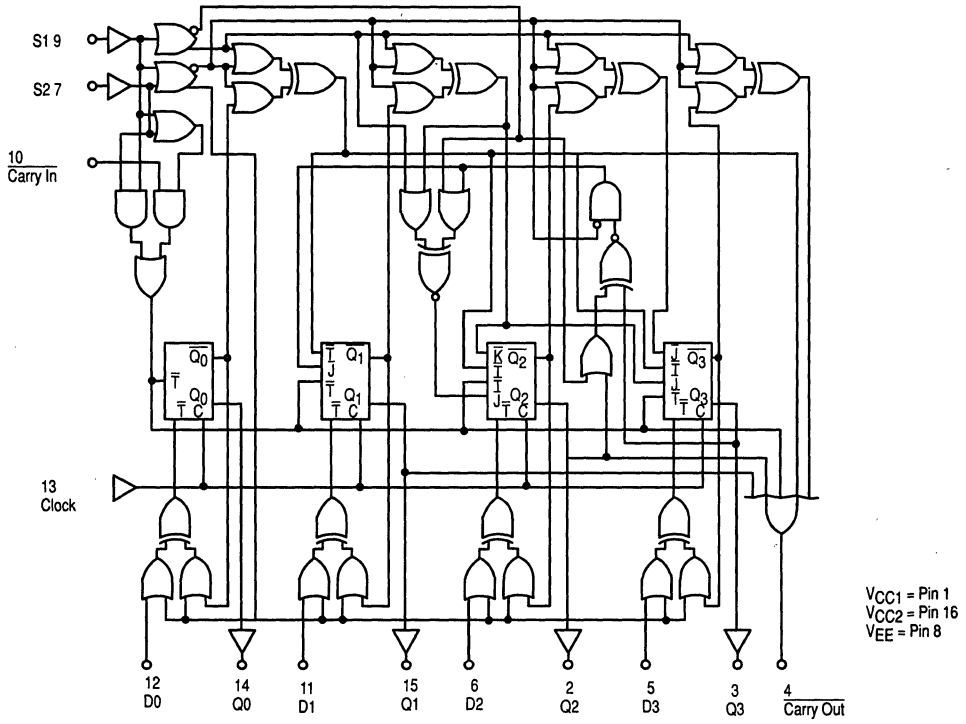
FUNCTION SELECT TABLE		
S_1	S_2	OPERATING MODE
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

SEQUENTIAL TRUTH TABLE •												
S_1	S_2	D_0	D_1	D_2	D_3	$\overline{\text{Carry}}$ IN	Clock ••	Q_0	Q_1	Q_2	Q_3	$\overline{\text{Carry}}$ OUT
L	L	H	H	H	L	Ø	H	H	H	H	L	H
L	H	Ø	Ø	Ø	Ø	L	H	L	L	L	H	H
L	H	Ø	Ø	Ø	Ø	L	H	H	L	L	H	L
L	H	Ø	Ø	Ø	Ø	L	H	L	L	L	L	H
L	H	Ø	Ø	Ø	Ø	L	H	H	L	L	L	H
L	H	Ø	Ø	Ø	Ø	H	L	H	L	L	L	H
L	H	Ø	Ø	Ø	Ø	H	H	H	L	L	L	H
H	H	Ø	Ø	Ø	Ø	Ø	H	H	L	L	L	H
L	L	H	H	L	L	Ø	H	H	H	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	L	H	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	H	L	L	L	H
H	L	Ø	Ø	Ø	Ø	L	H	L	L	L	L	L

Ø = Don't Care

• Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

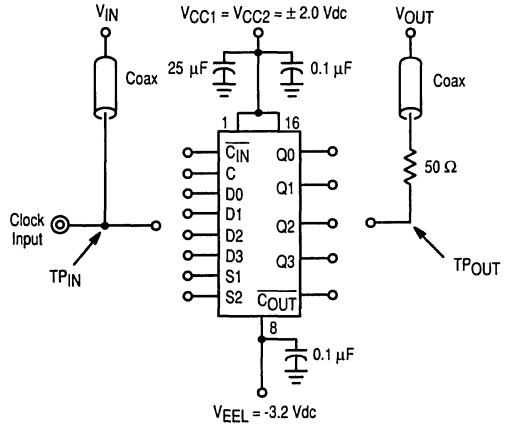
•• A clock H is defined as a clock input transition from a low to a high logic level.



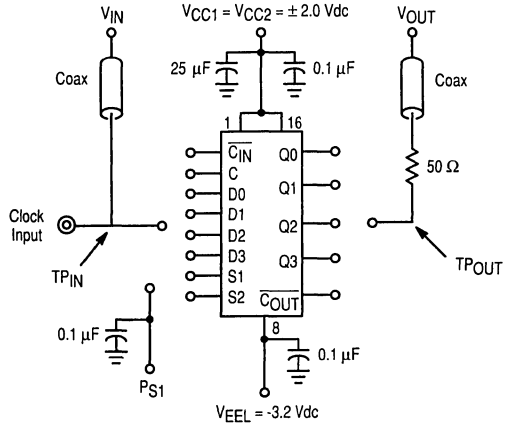
NOTE
FLIP FLOPS WILL TOGGLE WHEN
ALL $\overline{T}$ INPUTS ARE LOW.

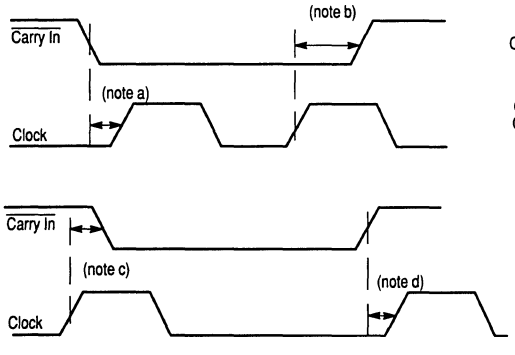
Figure 1. Logic Diagram

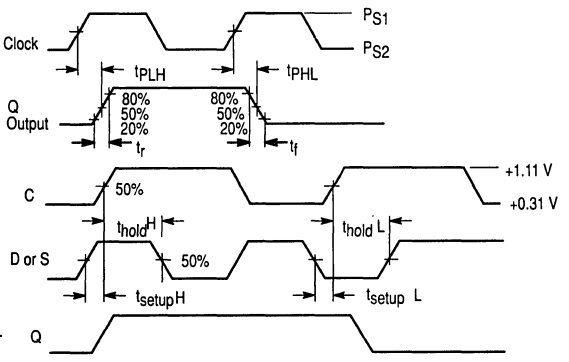
Switching Time Test Circuit



Counter Frequency Test Circuit







NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Unused outputs are connected to a 100 Ω resistor to ground.
3. 50 Ω termination located in each scope channel input.
4. PW ≥ 20 ns.
5. PRR = 1.0 MHz.
6. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%).

a) is the minimum time to wait after the counter has been enabled to clock it.
b) is the minimum time before the counter has been disabled that it may be clocked.
c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.
d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.
(b) and (c) may be negative numbers.
t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.
t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.

Figure 2. Test Circuits and Waveforms

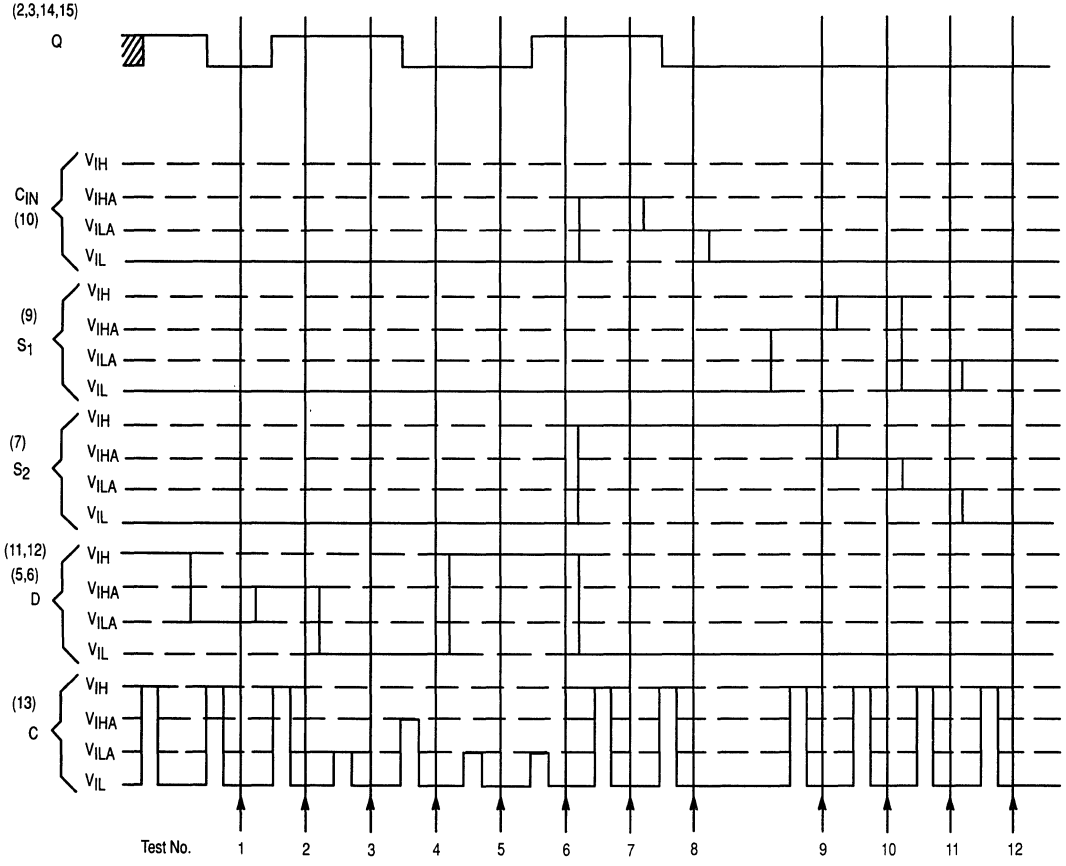


Figure 3. Threshold Sequence for V_{OLA}, V_{OHA} Tests

10537
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V				
		Subgroup 1		Subgroup 2		Subgroup 3							
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	5 - 7, 9, 11 - 13	13	8	1, 16	2, 3, 4, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	13	13	8	1, 16	2, 3, 4, 14, 15
V_{OH1}	High Output Voltage**	- 0.95		- 0.845		- 1.10		V			8	1, 16	2, 3, 4, 14, 15
V_{OL1}	Low Output Voltage**		- 1.60		- 1.525		- 1.635	V			8	1, 16	2, 3, 4, 14, 15
I_{EE}	Power Supply Current	- 150		- 165		- 165		mA			8	1, 16	8
I_{IH}	Input Current High		220		375		375	µA	5, 6, 11, 12		8	1, 16	5, 6, 11, 12
I_{IH1}	Input Current High		245		415		415	µA	9, 10		8	1, 16	9, 10
I_{IH2}	Input Current High		265		450		450	µA	7		8	1, 16	7
I_{IH3}	Input Current High		290		495		495	µA	13		8	1, 16	13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 10 - 14	8	1, 16	5 - 7, 10 - 14

** See Figure 3

10537
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max		CLK	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.2	3.7	0.9	3.3	ns		7, 10, 12, 13	4, 14	1, 16	8, 11, 12	5 - 7, 13	9, 10	4, 14
t_{THL}	Fall Time	1.1	3.3	1.2	3.7	0.9	3.3	ns		7, 10, 12, 13	4, 14	1, 16	8, 11, 12	5 - 7, 13	9, 10	4, 14
t_{pd}	Propagation Delay CLK to Q CLK to Carry Out Carry In to Carry Out	1.0 2.5 1.6	4.5 10.5 6.9	1.4 2.4 1.9	5.2 12.6 7.6	0.8 2.0 1.6	4.6 11.0 7.1	ns ns ns		7, 10, 12, 13 7, 10, 12, 13 7, 10, 12, 13	4, 14 4, 14 4, 14	1, 16 1, 16 1, 16	8, 11, 12 8, 11, 12 8, 11, 12	5 - 7, 13 5 - 7, 13 5 - 7, 13	9, 10 9, 10 9, 10	4, 14 4, 14 4, 14
t_{set}	Setup Time Data Inputs Select Inputs Carry In Input	3.5 7.5 7.5 3.7 -1.0		3.5 7.5 7.5 4.5 -1.0		3.5 7.5 7.5 4.5 -1.0		ns ns ns ns ns	13 13 13 13 13	7, 10, 12, 13 7, 10, 12, 13 7, 10, 12, 13 7, 10, 12, 13 7, 10, 12, 13	14 14 14 14 14	1, 16 1, 16 1, 16 1, 16 1, 16	8 8 8 8 8	7 7 7 7 7	7, 10 7, 10 7, 10 7, 10 7, 10	14 14 14 14 14
t_{hold}	Hold Time Data Inputs Select Inputs Carry In Inputs	0.0 – 2.5 – 1.6 3.1		0.0 – 2.5 – 1.6 4.0		0.0 – 2.5 – 1.6 4.0		ns ns ps ns	13 13 13 13	7, 10, 12, 13 7, 10, 12, 13 7, 10, 12, 13 7, 10, 12, 13	14 14 14 14	1, 16 1, 16 1, 16 1, 16	8 8 8 8	7 7 7 7	7, 10 7, 10 7, 10 7, 10	14 14 14 14
f_{count}	Counting Frequency	125		115		115		MHz		13	14	1, 16	8	7, 9		14

MOTOROLA

Bi-Quinary Counter

ELECTRICALLY TESTED PER:
MPG 10538

The 10538 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set-reset master-slave flip-flops. Clock inputs trigger on the positive going edge of the clock pulse.

Set or Reset input override the clock, allowing asynchronous "set" or "clear". Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits.

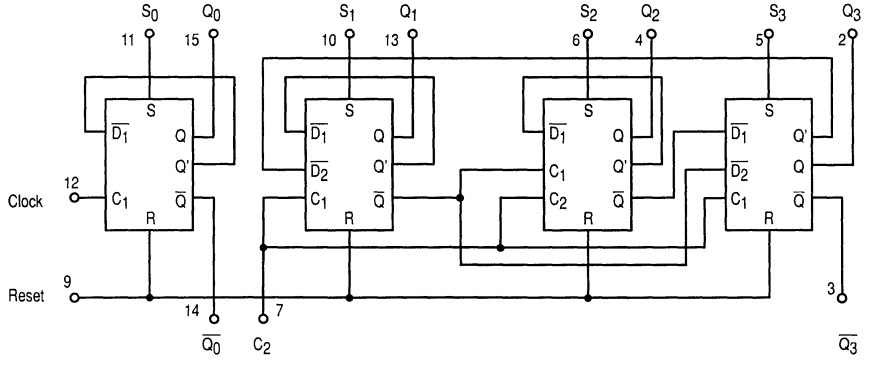
- 610 mW Max/Pkg (No Load)
- f_{tog} = 150 MHz typ
- t_{pd} = 2.5 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_3	2	6	3	51 Ω to V_{TT}
$\overline{Q_3}$	3	7	4	51 Ω to V_{TT}
Q_2	4	8	5	51 Ω to V_{TT}
S_3	5	9	7	GND
S_2	6	10	8	GND
C_2	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
Reset	9	13	12	OPEN
S_1	10	14	13	GND
S_0	11	15	14	GND
C_1	12	16	15	OPEN
Q_1	13	1	17	51 Ω to V_{TT}
Q_0	14	2	18	51 Ω to V_{TT}
$\overline{Q_0}$	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.2 V MIN/ - 2.0 V MAX
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

LOGIC DIAGRAM



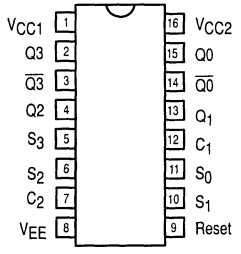
Military 10538

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10538/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



3

BI-QUINARY

(Clock connected to C2 and Q3 connected to C1)

COUNT	Q_1	Q_2	Q_3	Q_0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

BCD

(Clock connected to C1 and Q0 Connected to C2)

COUNT	Q_0	Q_1	Q_2	Q_0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

3

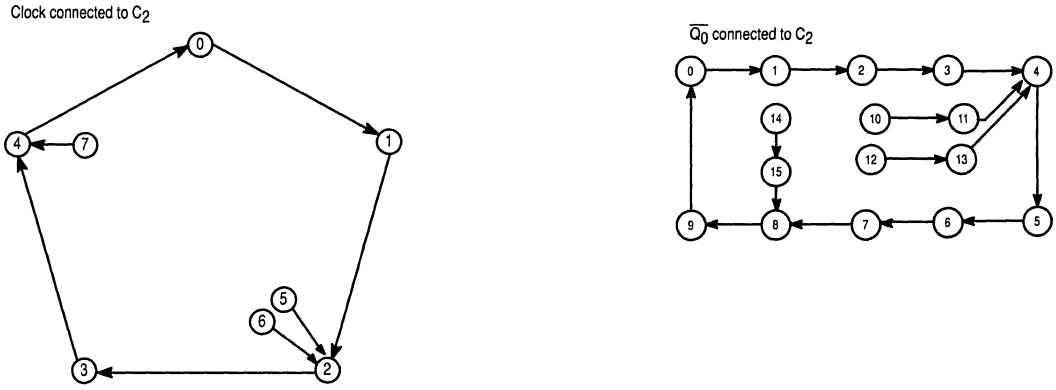


Figure 1. Counter State Diagram-Positive Logic

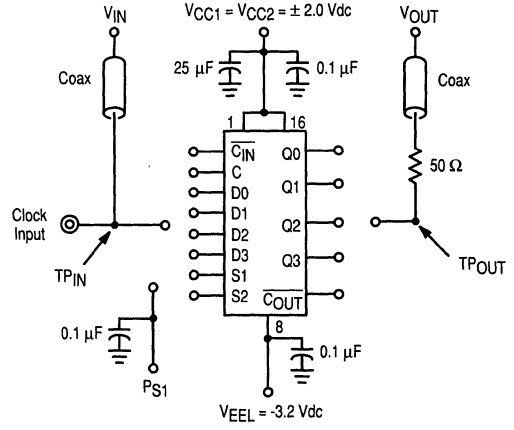
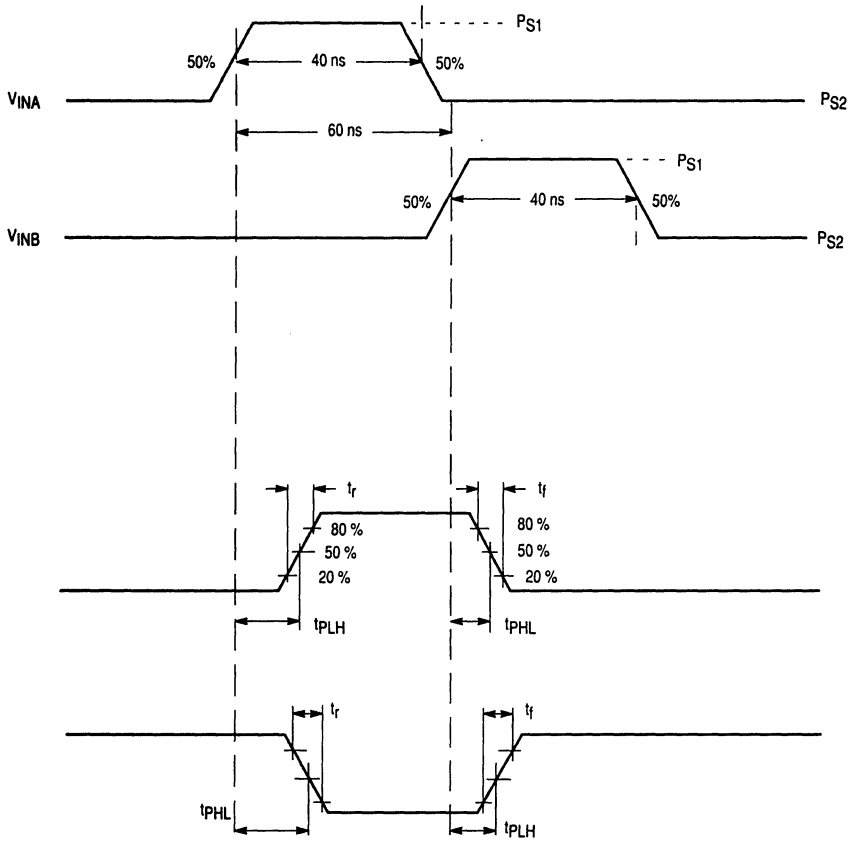


Figure 2. Test Circuit



NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Unused outputs are connected to a 100 Ω resistor to ground.
3. 50 Ω termination located in each scope channel input.
4. PW ≥ 20 ns.
5. PRR = 1.0 MHz.
6. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%).
7. Duty Cycle = 50%
8. 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.

Figure 3. Switching Test Circuit Waveforms

10538
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	$P_{1, 2, 3}$	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	5, 6, 9 - 11			8	1, 16	2, 3, 4, 13, 15
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.545	– 1.92	– 1.655	V	5, 6, 9 - 11			8	1, 16	2, 3, 4, 13, 15
V_{OH1}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V		5 - 7, 9 - 12	5 - 7, 9 - 12	8	1, 16	2, 3, 4, 13, 15
V_{OL1}	Low Output Voltage	– 1.85	– 1.60	– 1.82	– 1.525	– 1.92	– 1.635	V		5 - 7, 9 - 12	5 - 7, 9 - 12	8	1, 16	2, 3, 4, 13, 15
I_{EE}	Power Supply Drain Current	– 88		– 97		– 97		mA				8	1, 16	8
I_{IH}	Input Current High		220		375		375	µA	12			8	1, 16	12
I_{IH1}	Input Current High		245		415		415	µA	5, 6, 10, 11			8	1, 16	5, 6, 10, 11
I_{IH2}	Input Current High		290		495		495	µA	7			8	1, 16	7
I_{IH3}	Input Current High		410		700		700	µA	9			8	1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 9 - 12		8	1, 16	5 - 7, 9 - 12

10538
QUIESCENT LIMIT TABLE *

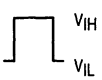
* ELECTRICAL CHARACTERISTICS

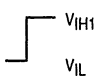
Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

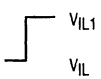
Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_r	Rise Time	1.1	4.5	1.1	5.0	1.1	4.7	ns	5, 7, 9, 10	2 - 4, 13 -15	1, 16	8	6, 10	9, 10	2 - 4, 13 -15
t_f	Fall Time	1.1	4.5	1.1	5.0	1.1	4.7	ns	5, 7, 9, 10	2 - 4, 13 -15	1, 16	8	6, 10	9, 10	2 - 4, 13 -15
t_{PHL}	Propagation Delay C to Q_1, Q_2, $\overline{Q_3}$	1.5	5.0	1.5	6.2	1.4	6.2	ns	5, 7, 9, 10	2 - 4, 13 -15	1, 16	8	6, 10	9, 10	2 - 4, 13 -15
t_{PLH}	Propagation Delay C to Q_0, $\overline{Q_0}$	1.5	4.8	1.5	5.5	1.4	5.5	ns	5, 7, 9, 10	2 - 4, 13 -15	1, 16	8	6, 10	9, 10	2 - 4, 13 -15
t_{PHL}	Propagation Delay S to Q	1.5	5.0	1.5	6.2	1.4	5.2	ns	5, 7, 9, 10	2 - 4, 13 -15	1, 16	8	6, 10	9, 10	2 - 4, 13 -15
t_{PLH}	Propagation Delay R to Q	1.5	5.0	1.5	6.2	1.4	5.5	ns	5, 7, 9, 10	2 - 4, 13 -15	1, 16	8	6, 10	9, 10	2 - 4, 13 -15
f_{Tog}	Toggle Frequency	125		125		125		MHz	7, 12	2, 14	1, 16	8		6, 7, 9 - 12	2, 14

NOTES:

P1) 

P2) 

P3) 

Four Bit Universal Shift Register

ELECTRICALLY TESTED PER:
5962-8855701

The 10541 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Input S_1 and S_2 control the four possible operations of the register without external gating of the clock.

The flip-flops shift information on the positive edge of the dock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs; four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

- 585 mW Max/Pkg (No Load)
- f_{Shift} = 200 MHz typ
- t_r, t_f = 1.5 ns typ (20% - 80%)

AVAILABLE AS

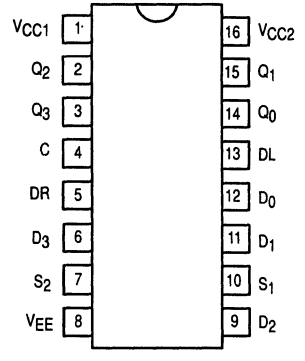
1) JAN: N/A
2) SMD: 5962-8855701
3) 883: 10541/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

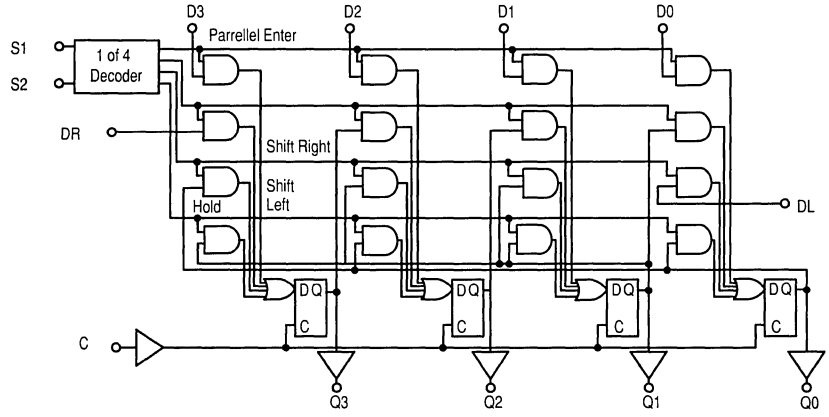
PIN ASSIGNMENTS

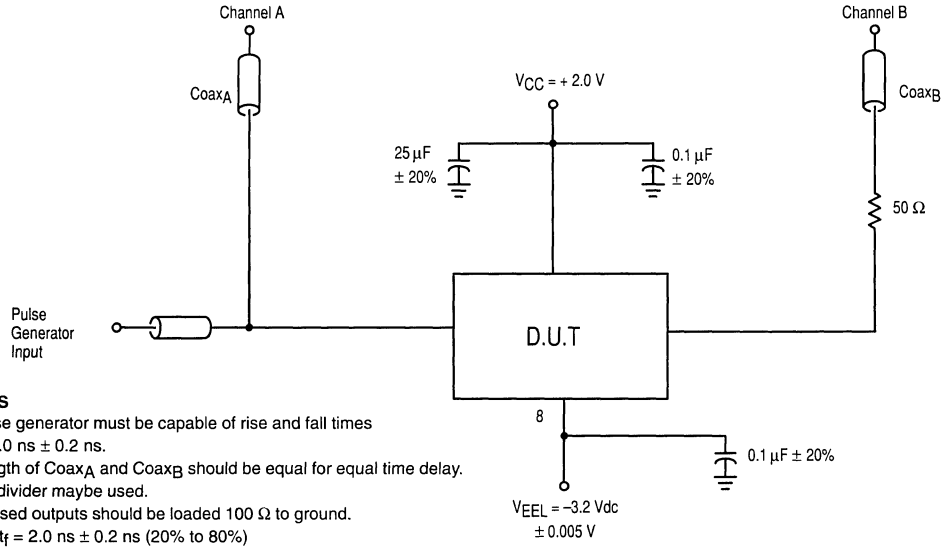
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_2	2	6	3	51 Ω to V_{TT}
Q_3	3	7	4	51 Ω to V_{TT}
C	4	8	5	CP1
DR	5	9	7	OPEN
D_3	6	10	8	GND
S_2	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
D_2	9	13	12	GND
S_1	10	14	13	OPEN
D_1	11	15	14	GND
D_0	12	16	15	GND
DL	13	1	17	OPEN
Q_0	14	2	18	51 Ω to V_{TT}
Q_1	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

LOGIC DIAGRAM





NOTES

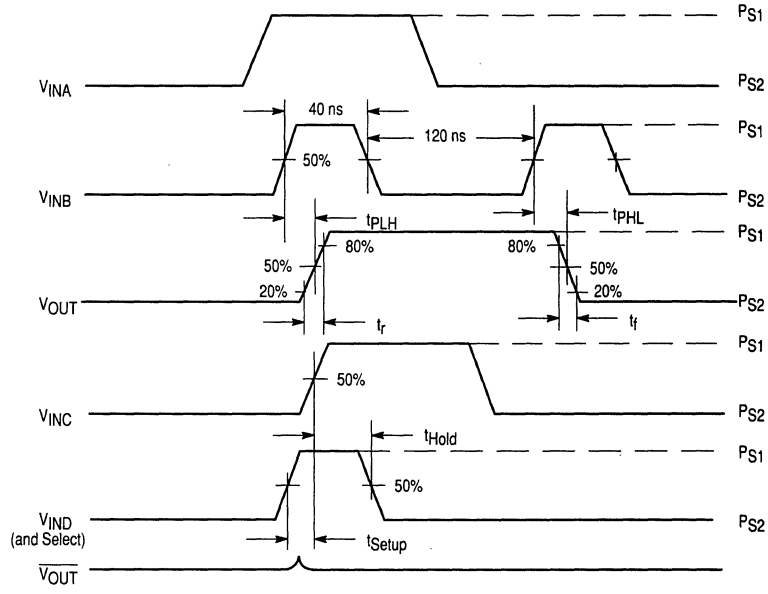
1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 3:1 divider maybe used.
4. Unused outputs should be loaded 100 Ω to ground.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)

Figure 1. Switching Test Circuit and Waveforms

TRUTH TABLE

SELECT		OPERATING MODE	OUTPUTS			
S_1	S_2		Q_{0n+1}	Q_{1n+1}	Q_{2n+1}	Q_{3n+1}
L	L	Parallel Entry	D_0	D_1	D_2	D_3
L	H	Shift Right *	$Q1_n$	Q2n	Q3n	DR
H	L	Shift Left *	DL	Q0n	Q1n	Q2n
H	H	Stop Shift	$Q0_n$	Q1n	Q2n	Q3n

* Outputs as exist after pulse at "C" input conditions as shown,
(Pulse = Positive transition of the clock input.).



NOTES

1. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 2.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

Figure 2. Switching Test Circuit Waveforms

10541
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4, 5, 9, 11, 12	4			8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4	4, 5, 9, 11, 12			8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	4 - 7, 9 - 13	4 - 7, 9 - 13	4 - 7, 9 - 13	4 - 7, 9 - 13	8	1, 16	2 - 4, 13 - 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	4 - 7, 9 - 13	4 - 7, 9 - 13	4 - 7, 9 - 13	4 - 7, 9 - 13	8	1, 16	2 - 4, 13 - 15
I_{IH1}	Input Current High		220		375		375	µA	5, 6, 9, 11 - 13				8	1, 16	5, 6, 9, 11 - 13
I_{IH2}	Input Current High		245		415		415	µA	7, 10				8	1, 16	7, 10
I_{IH3}	Input Current High		265		450		450	µA	4				8	1, 16	4
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 13			8	1, 16	4 - 7, 9 - 13
I_{EE}	Power Supply Drain Current	- 102		- 112		- 112		mA					8	1, 16	8

10541
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL}	Propagation Delay	1.8	3.8	2.0	4.5	1.7	4.1	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay	1.8	3.8	2.0	4.5	1.7	4.1	ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{Setup}	Setup Time Data Input	2.5		3.0		3.0		ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{hold}	Hold Time Data Input	1.5		1.5		1.5		ns	4, 6, 9, 11, 12	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{Setup}	Setup Time Select Inputs	5.0		7.0		7.0		ns	4, 6, 9, 11, 12	3, 14	1, 16	8	2, 3, 14, 15
t_{hold}	Hold Time Select Input	1.5		1.5		1.5		ns	4, 6, 9, 11, 12	3, 14	1, 16	8	2, 3, 14, 15
f_{tog}	Toggle Frequency	150		150		150		MHz	4, 6, 9, 11, 12	3, 14	1, 16	8	14
f_{shift}	Shift Frequency	150		150		150		MHz	4, 6, 9, 11, 12	3, 14	1, 16	8	14

Military 10553

Quad Latch

ELECTRICALLY TESTED PER:
MPG 10553

The 10553 is a high speed, low power, MECL quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs. Open emitters allow a large number of outputs to be wire-ORed together. Latch outputs are gated, allowing direct wiring to a bus. When the clock is low, outputs will follow D inputs. Information is latched on the positive going transition of the Clock. The 10553 provides the same logic function as the 10533, except for inversion of the clock.

- 435 mW Max/Pkg (No Load)
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

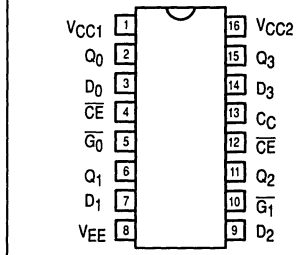
1) JAN: N/A
2) SMD: N/A
3) 883: 10553/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_0	2	6	3	51 Ω to V_{TT}
D_0	3	7	4	GND
$\overline{CE}$	4	8	5	OPEN
$\overline{G_0}$	5	9	7	OPEN
Q_1	6	10	8	51 Ω to V_{TT}
D_1	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
D_2	9	13	12	GND
$\overline{G_1}$	10	14	13	OPEN
Q_2	11	15	14	51 Ω to V_{TT}
$\overline{CE}$	12	16	15	OPEN
C_C	13	1	17	OPEN
D_3	14	2	18	GND
Q_3	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



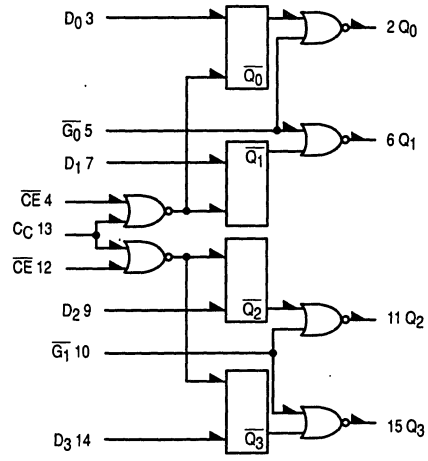
BURN - IN CONDITIONS:
V_{TT} = – 2.2 V MIN/ – 2.0 V MAX
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

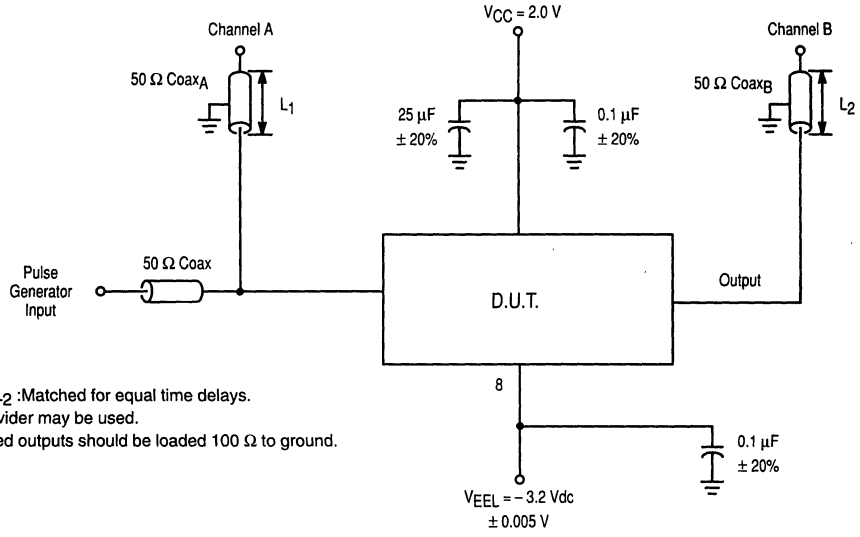
TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	∅	∅	L
L	H	∅	Q_n
L	L	L	L
L	L	H	H

∅ = Don't Care
$C = C_C + \overline{CE}$

LOGIC DIAGRAM

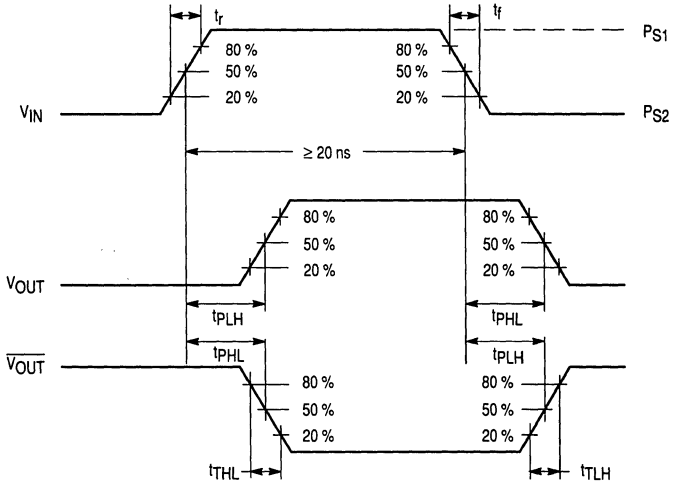




NOTES

1. $L_1 = L_2$:Matched for equal time delays.
2. 2:1 divider may be used.
3. Unused outputs should be loaded 100 Ω to ground.

Figure 1. Switching Test Circuit



NOTES

1. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

Figure 2. Switching Test Circuit Waveform

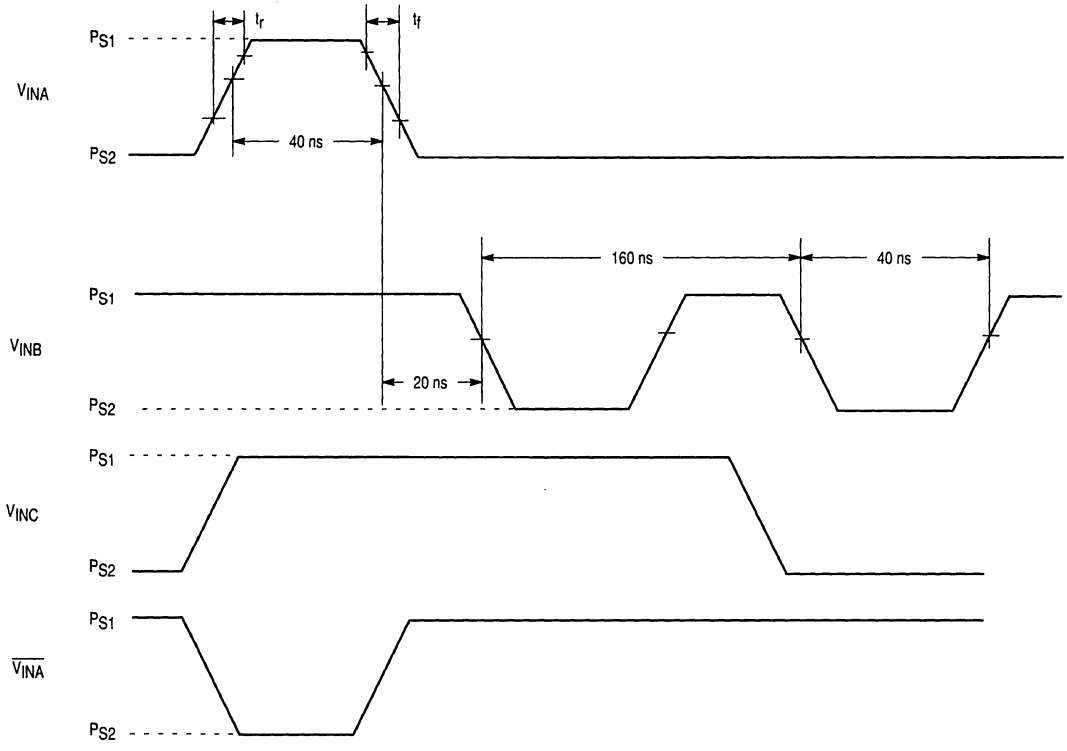


Figure 3. Switching Test Circuit (continued)

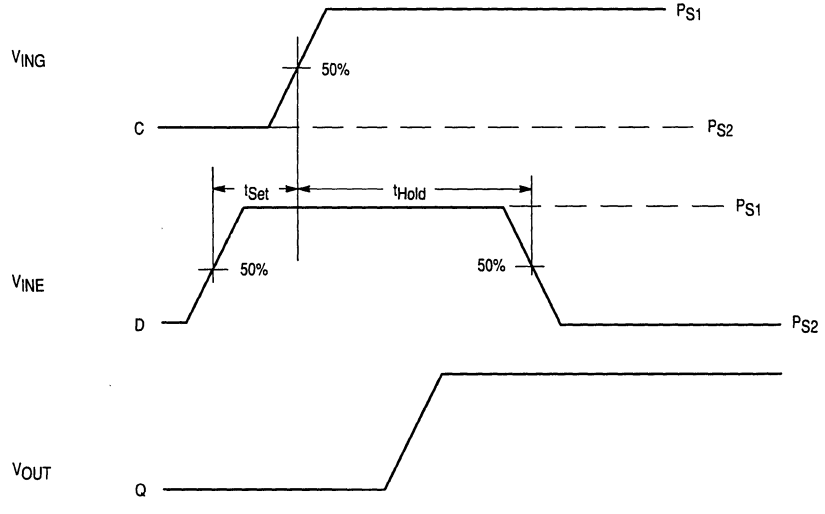


Figure 4. t_{Setup} and t_{Hold} Waveforms

10553
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	3, 7, 9, 13, 14				8	1, 16	2, 6, 11, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	3, 5, 7, 9, 10, 14				8	1, 16	2, 6, 11, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	3, 7, 9, 14		5, 10	5, 9, 14	8	1, 16	2, 6, 11, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	3, 7, 9, 14		3, 7, 9, 14	5, 10	8	1, 16	2, 6, 11, 15
I_{IH1}	Input Current High		290		495		495	µA	13				8	1, 16	13
I_{IH2}	Input Current High		245		420		420	µA	3, 4, 7, 9, 12, 14				8	1, 16	3, 4, 7, 9, 12, 14
I_{IH3}	Input Current High		350		595		595	µA	5, 10				8	1, 16	5, 10
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 5, 7, 9, 10, 12 - 14			8	1, 16	3 - 5, 7, 9, 10, 12 - 14
I_{EE}	Power Supply Drain Current	- 75		- 83		- 83		mA					8	1, 16	8

10553
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.5	1.0	4.1	1.0	3.9	ns	3 - 5, 7, 9, 10, 12, 14	2, 6, 11, 15	1, 16	8	3, 9, 14	5, 10, 13	2, 6, 11, 15
t_{THL}	Fall Time	1.1	3.5	1.0	4.1	1.0	3.9	ns	3 - 5, 7, 9, 10, 12, 14	2, 6, 11, 15	1, 16	8	3, 9, 14	5, 10, 13	2, 6, 11, 15
t_{PHL}/ t_{PLH}	Propagation Delay Clock to Output	1.0	5.6	1.0	6.6	1.0	6.1	ns	3 - 5, 7, 9, 10, 12, 14	2, 6, 11, 15	1, 16	8	3, 9, 14	5, 10, 13	2, 6, 11, 15
t_{PHL}/ t_{PLH}	Propagation Delay Data to Output	1.0	5.4	1.0	6.3	1.0	5.8	ns	3 - 5, 7, 9, 10, 12, 14	2, 6, 11, 15	1, 16	8	3, 9, 14	5, 10, 13	2, 6, 11, 15
t_{PHL}/ t_{PLH}	Propagation Delay Gate to Output	1.0	3.1	1.0	3.6	1.0	3.4	ns	3 - 5, 7, 9, 10, 12, 14	2, 6, 11, 15	1, 16	8	3, 9, 14	5, 10, 13	2, 6, 11, 15
t_S	Setup Time	2.5		2.5		2.5		ns	3, 7, 9, 11, 14	2, 6, 11, 15	1, 16	8			2, 6, 11, 15
t_H	Hold Time	1.5		1.5		1.5		ns	3, 4, 7, 9, 14	2, 6, 11, 15	1, 16	8			2, 6, 11, 15

MOTOROLA

Quad 2-Input Multiplexer (Non-Inverting)

ELECTRICALLY TESTED PER:
5962-8779201

The 10558 is a quad two channel multiplexer. A common select input determines which data inputs are enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D12, and D31.

- 280 mW Max/Pkg (No Load)
- t_{pd} = 2.5 ns typ (Data to Q)
  = 3.2 ns typ (Select to Q)
- t_r, t_f = 2.5 ns typ (20% - 80%)

3

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
Q0	1	5	2	51 Ω to V_{TT}
Q1	2	6	3	51 Ω to V_{TT}
D11	3	7	4	51 Ω to V_{TT}
D10	4	8	5	OPEN
D01	5	9	7	GND
D00	6	10	8	OPEN
NC	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
Select	9	13	12	OPEN
D31	10	14	13	GND
D30	11	15	14	OPEN
D21	12	16	15	GND
D20	13	1	17	OPEN
Q3	14	2	18	51 Ω to V_{TT}
Q2	15	3	19	51 Ω to V_{TT}
V_{CC}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

TRUTH TABLE

Select	D_0	D_1	Q
L	∅	L	L
L	∅	H	H
H	L	∅	L
H	H	∅	H

∅ = Don't Care

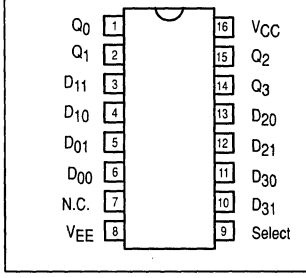
Military 10558

AVAILABLE AS

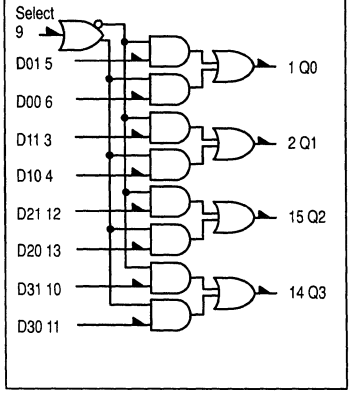
1) JAN: N/A
2) SMD: 5962-8779201
3) 883: 10558/BXAJC
X = CASE OUTLINE AS FOLLOWS:

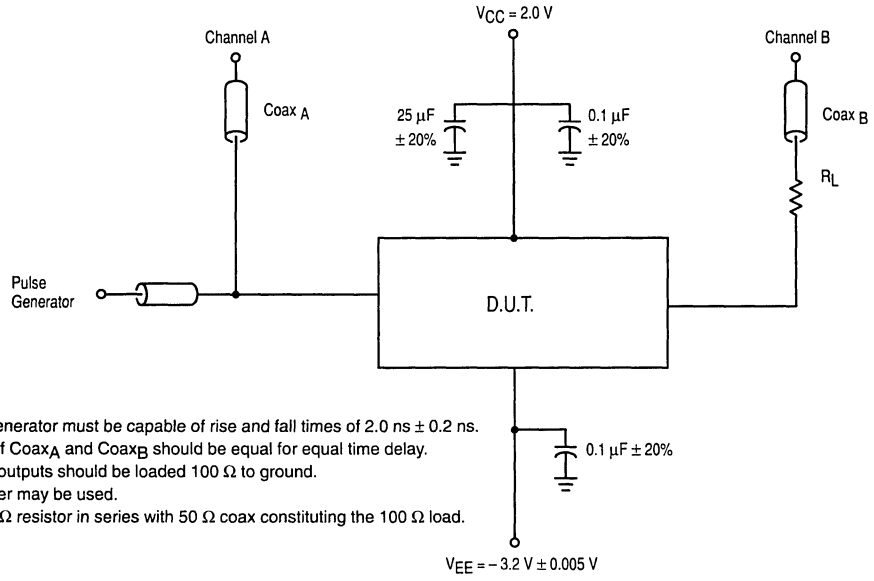
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



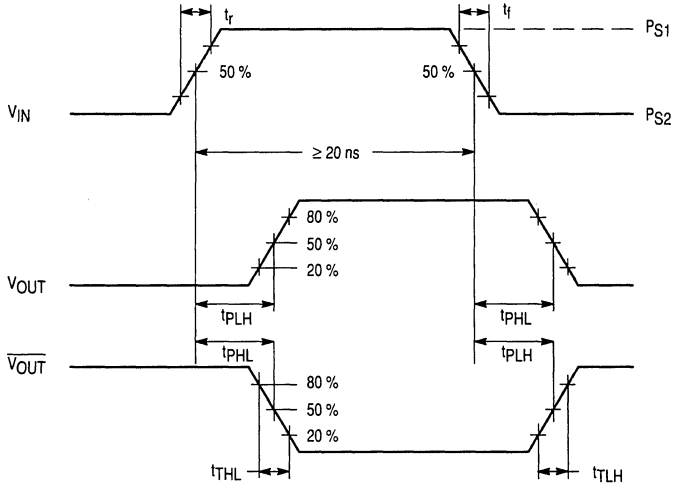
LOGIC DIAGRAM





NOTES
1. Pulse Generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. Unused outputs should be loaded 100 Ω to ground.
4. 2:1 divider may be used.
5. R_L = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.

Figure 1. Switching Test Circuit



NOTES
V_{IN} has the following characteristics:
1. $P_W \geq 20$ ns.
2. P_{RF} = 1.0 MHz.
3. $t_r = t_f = 2.0$ ns ± 0.2 ns measured at (20% - 80%).

Figure 2. Switching Test Circuit Waveforms

10558
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	3, 5, 10, 12				8	16	1, 2, 14, 15
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.545	– 1.92	– 1.655	V					8	16	1, 2, 14, 15
V_{OL1}	Low Output Voltage	– 1.85	– 1.60	– 1.82	– 1.525	– 1.92	– 1.635	V	3 - 6, 9 - 13			3 - 6, 9 - 13	8	16	1, 2, 14, 15
V_{OH1}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V	3 - 6, 9 - 13		3 - 6, 9 - 13		8	16	1, 2, 14, 15
I_{IH1}	Input Current High		225		385		385	µA	9				8	16	9
I_{IH2}	Input Current High		250		425		425	µA	3 - 6, 10 - 13				8	16	4, 5, 6, 10 - 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 6, 9 - 13			8	16	3 - 6, 9 - 13
I_{EE}	Power Supply Drain Current	– 48		– 53		– 53		mA					8	16	8

10558
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.5	3.3	1.6	3.5	1.6	3.5	ns	3 - 6, 9 - 13	1, 2, 14, 15	16	8	3 - 6, 9 - 13	1, 2, 14, 15
t_{THL}	Fall Time	1.5	3.3	1.6	3.5	1.6	3.5	ns	3 - 6, 9 - 13	1, 2, 14, 15	16	8	3 - 6, 9 - 13	1, 2, 14, 15
t_{PHL}/ t_{PLH}	Propagation Delay Data to Output	1.2	3.0	1.5	3.5	1.5	3.5	ns	3 - 6, 9 - 13	1, 2, 14, 15	16	8	3 - 6, 9 - 13	1, 2, 14, 15
t_{PHL}/ t_{PLH}	Propagation Delay Select to Output	2.4	4.5	2.5	5.0	2.5	5.0	ns	3 - 6, 9 - 13	1, 2, 14, 15	16	8	3 - 6, 9 - 13	1, 2, 14, 15

12-Bit Parity Generator-Checker

ELECTRICALLY TESTED PER:
MPG 10560

The 10560 consists of nine **EXCLUSIVE-OR** gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

- 450 mW Max/Pkg (No Load)
- t_{pd} = 5.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Out	2	6	3	51 Ω to V_{TT}
IN_1	3	7	4	GND
IN_2	4	8	5	OPEN
IN_3	5	9	7	OPEN
IN_4	6	10	8	OPEN
IN_5	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
IN_6	9	13	12	OPEN
IN_7	10	14	13	GND
IN_8	11	15	14	OPEN
IN_9	12	16	15	OPEN
IN_{10}	13	1	17	OPEN
IN_{11}	14	2	18	OPEN
IN_{12}	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.2 V MIN/ – 2.0 V MAX
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Input	Output
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High

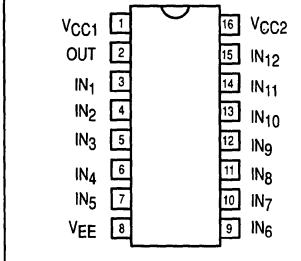
Military 10560

AVAILABLE AS

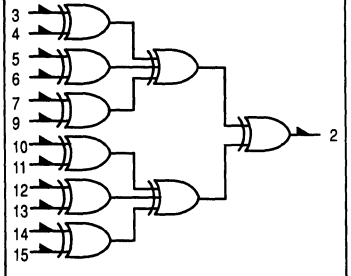
1) JAN: N/A
2) SMD: N/A
3) 883: 10560/BXAJC
X = CASE OUTLINE AS FOLLOWS:

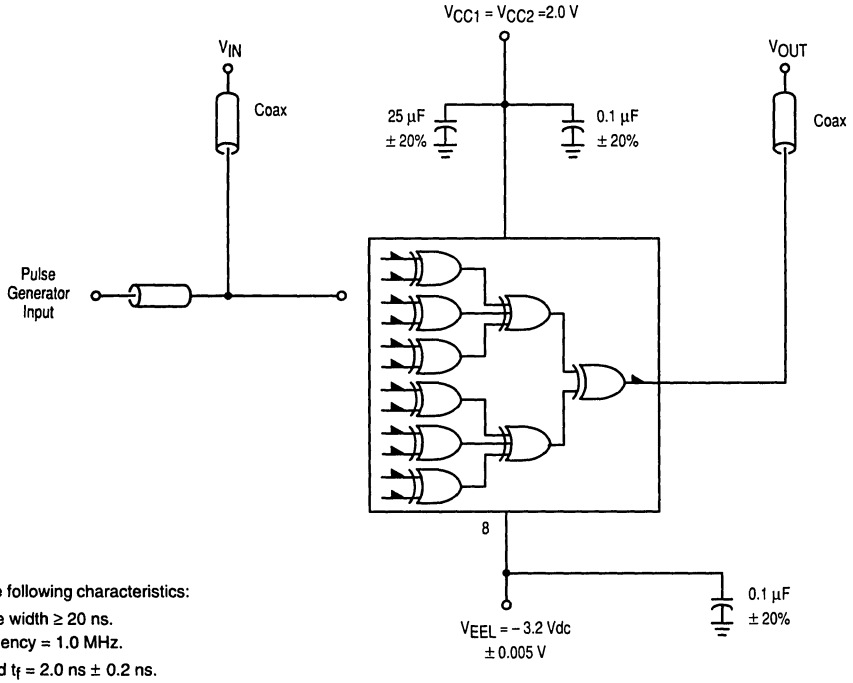
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be < 1.4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.

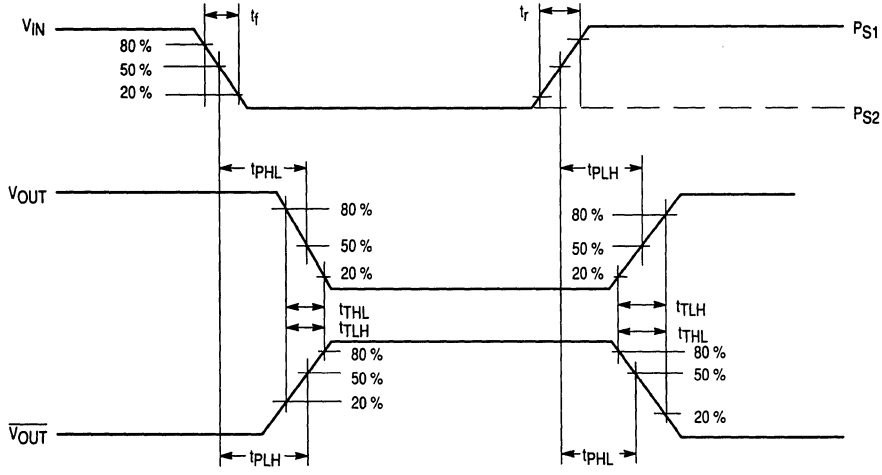


Figure 1. Switching Test Circuit and Waveforms

10560
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to − 2.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	− 0.93	− 0.78	− 0.825	− 0.63	− 1.08	− 0.88	V	3 - 7 9 - 15	3 - 7 9 - 15		8	1, 16	2
V_{OL}	Low Output Voltage	− 1.85	− 1.62	− 1.82	− 1.545	− 1.92	− 1.655	V	3 - 7 9 - 15	3 - 7 9 - 15		8	1, 16	2
V_{OL1}	Low Output Voltage	− 1.85	− 1.60	− 1.82	− 1.525	− 1.92	− 1.635	V	3 - 7 9 - 14	4 - 7 9 - 15	4, 7, 9 11, 13, 15	8	1, 16	2
V_{OH1}	High Output Voltage	− 0.95	− 0.78	− 0.845	− 0.63	− 1.10	− 0.88	V	3 - 7, 9 - 11, 13	4 - 7 9 - 15	3, 5, 7, 10, 12, 14	8	1, 16	2
I_{IH1}	Input Current High		265		450		450	µA	4, 5, 9, 12, 13, 14			8	1, 16	4, 5, 9, 10, 13, 14
I_{IH2}	Input Current High		220		375		375	µA	3, 6, 7, 11, 12, 15			8	1, 16	3, 6, 7, 11, 12, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 7 9 - 15		8	1, 16	3 - 7, 9 - 15
I_{EE}	Power Supply Drain Current	− 78		− 86		− 86		mA				8	1, 16	8

10560
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	0.9	3.4	1.0	3.4	ns	3 - 7 9 - 15	2	1, 16	8	3 - 7 9 - 15	3 - 7 9 - 15	2
t_{THL}	Fall Time	1.1	3.3	0.9	3.4	1.0	3.4	ns	3 - 7 9 - 15	2	1, 16	8	3 - 7 9 - 15	3 - 7 9 - 15	2
t_{PLH}	Propagation Delay	2.0	7.5	1.4	7.9	1.6	8.1	ns	3 - 7 9 - 15	2	1, 16	8	3 - 7 9 - 15	3 - 7 9 - 15	2
t_{PHL}	Propagation Delay	2.0	7.5	1.4	7.9	1.6	8.1	ns	3 - 7 9 - 15	2	1, 16	8	3 - 7 9 - 15	3 - 7 9 - 15	2

Military 10561

Binary to 1-8 Decoder (Low)

ELECTRICALLY TESTED PER:
MPG 10561

The 10561 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

The 10561 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This design provides the identical 4.0 ns delay from any address or enable input to any output.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the 10536 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the 10501s to send twisted-pair select data to the multiplexer/demultiplexer units.

- 440 mW Max/Pkg (No Load)
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10561/BXAJC
X = CASE OUTLINE AS FOLLOWS:

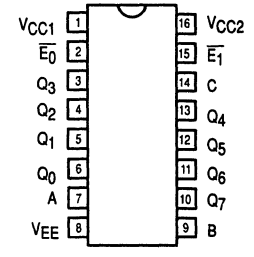
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

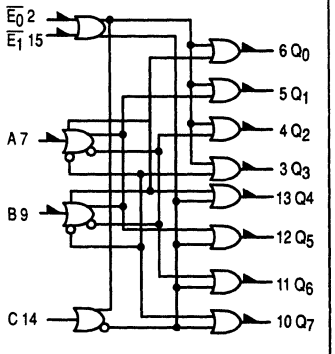
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{E_0}$	2	6	3	GND
Q_3	3	7	4	51 Ω to V_{TT}
Q_2	4	8	5	51 Ω to V_{TT}
Q_1	5	9	7	51 Ω to V_{TT}
Q_0	6	10	8	51 Ω to V_{TT}
A	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B	9	13	12	OPEN
Q_7	10	14	13	51 Ω to V_{TT}
Q_6	11	15	14	51 Ω to V_{TT}
Q_5	12	16	15	51 Ω to V_{TT}
Q_4	13	1	17	51 Ω to V_{TT}
C	14	2	18	GND
$\overline{E_1}$	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.2 V MIN/ – 2.0 V MAX
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



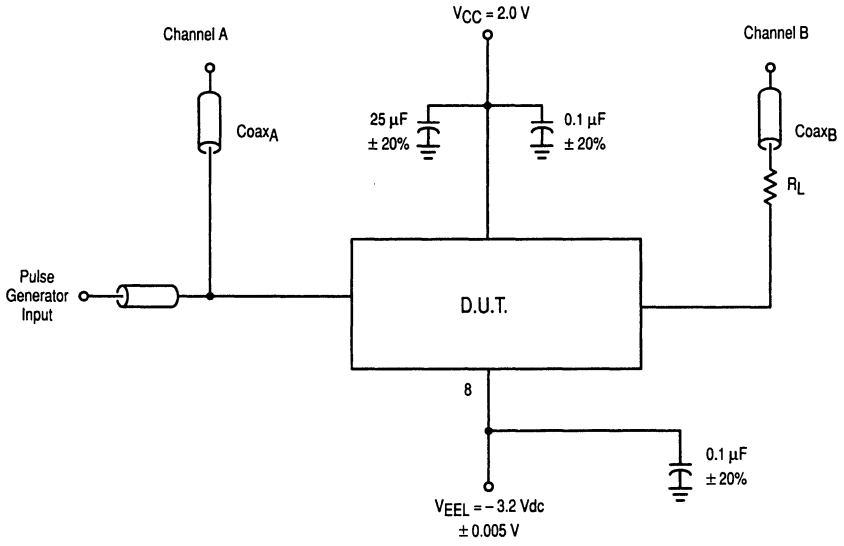
LOGIC DIAGRAM



TRUTH TABLE

ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E_1}$	$\overline{E_0}$	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	Ø	Ø	Ø	Ø	H	H	H	H	H	H	H	H
Ø	H	Ø	Ø	Ø	H	H	H	H	H	H	H	H

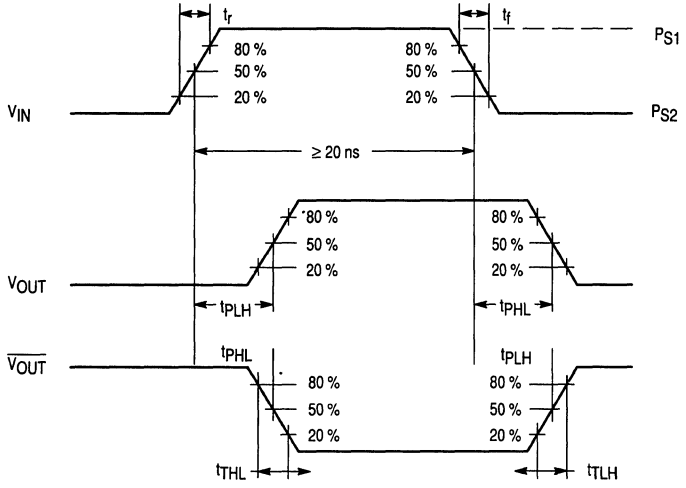
3



NOTES

1. The Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns
2. Length of $Coax_A$ and $Coax_B$ should be of equal lengths for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0$ ns (20% – 80%) + 0.2 ns.
5. $R_L = 50\ \Omega$ resistor in series with 50 Ω coax constituting 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground.

Figure 1. Switching Test Circuit



NOTES

1. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

Figure 2. Switching Test Circuit Waveforms

10561
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	2				8	1, 16	3 - 6, 10 - 13
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	7, 9, 14				8	1, 16	3 - 6, 10 - 13
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	7, 9, 14		7, 9, 14	2, 7, 9, 14	8	1, 16	3 - 6, 10 - 13
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	7, 9, 14		7, 9, 15	7, 9	8	1, 16	3 - 6, 10 - 13
I_{IH1}	Input Current High		220		375		375	µA	2, 7, 9, 14, 15				8	1, 16	2, 7, 9, 14, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		2, 7, 9 14, 15			8	1, 16	2, 7, 9, 14, 15
I_{EE}	Power Supply Drain Current	- 76		- 84		- 84		mA					8	1, 16	8

10561
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	2, 7, 9, 14	3, 4, 5, 10 - 13	1, 16	8	7, 9, 14	7, 9	3 - 6, 10 - 13
t_{THL}	Fall Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	2, 7, 9, 14	3, 4, 5, 10 - 13	1, 16	8	7, 9, 14	7, 9	3 - 6, 10 - 13
t_{PLH}	Propagation Delay	1.5	6.0	1.3	7.0	1.2	6.5	ns	2, 7, 9, 14	3, 4, 5, 10 - 13	1, 16	8	7, 9, 14	7, 9	3 - 6, 10 - 13
t_{PHL}	Propagation Delay	1.5	6.0	1.3	7.0	1.2	6.5	ns	2, 7, 9, 14	3, 4, 5, 10 - 13	1, 16	8	7, 9, 14	7, 9	3 - 6, 10 - 13

Binary to 1-8 Decoder (High)

Military 10562

ELECTRICALLY TESTED PER:
MPG 10562

The 10562 is designed to convert three lines of input data to a one of eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

The 10562 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This device is ideally suited for demultiplexer applications. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the 10536 control counters, has the capability of incrementing, decrementing or holding data channels. When both S_0 and S_1 are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the 10501s to send twisted-pair select data to the multiplexer/demultiplexer units.

- 440 mW Max/Gate (No Load)
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10562/BXAJC
X = CASE OUTLINE AS FOLLOWS:

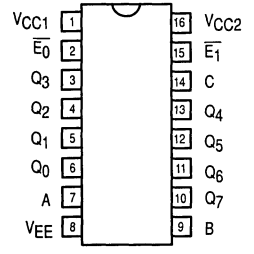
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

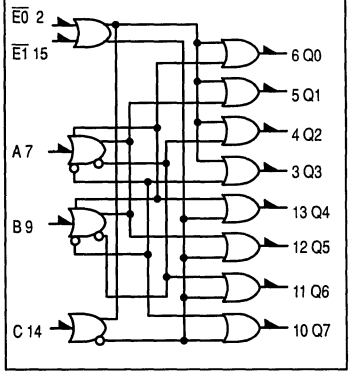
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{E_0}$	2	6	3	OPEN
Q_3	3	7	4	51 Ω to V_{TT}
Q_2	4	8	5	51 Ω to V_{TT}
Q_1	5	9	7	51 Ω to V_{TT}
Q_0	6	10	8	51 Ω to V_{TT}
A	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
B	9	13	12	OPEN
Q_7	10	14	13	51 Ω to V_{TT}
Q_6	11	15	14	51 Ω to V_{TT}
Q_5	12	16	15	51 Ω to V_{TT}
Q_4	13	1	17	51 Ω to V_{TT}
C	14	2	18	OPEN
$\overline{E_1}$	15	3	19	OPEN
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/– 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



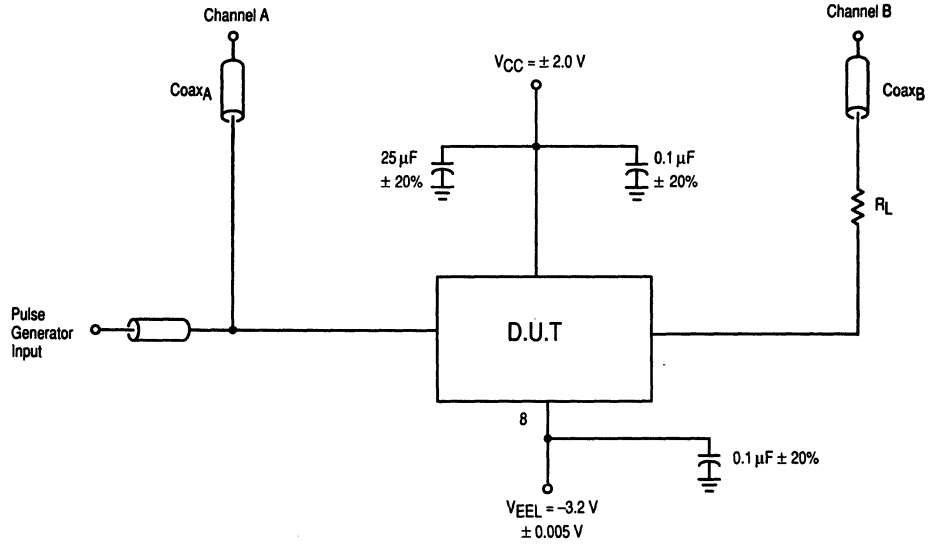
LOGIC DIAGRAM



TRUTH TABLE

Enable Inputs		Inputs			Outputs							
$\overline{E_1}$	$\overline{E_0}$	C	B	A	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	Ø	Ø	Ø	Ø	L	L	L	L	L	L	L	L
Ø	H	Ø	Ø	Ø	L	L	L	L	L	L	L	L

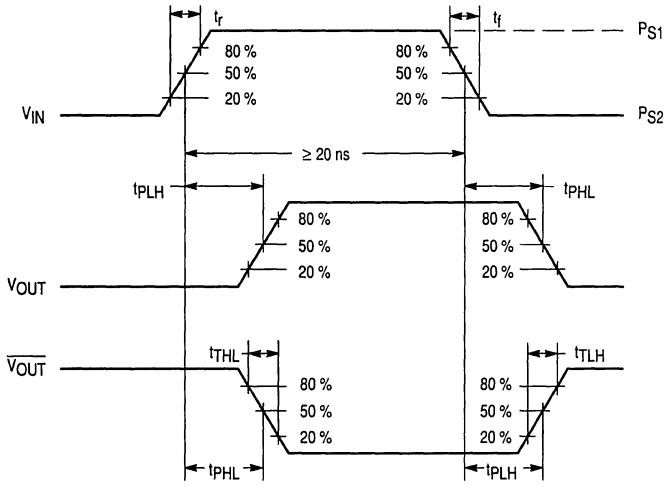
Ø = Don't Care



NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of Coax$_A$ and Coax$_B$ should be equal for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% - 80%).
5. R_L = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground.

Figure 1. Switching Test Circuit



NOTES
V_{IN} has the following characteristics:
1. P_W = 20 ns.
2. f_{IN} = 1.0 MHz.
3. $t_r = t_f$ = 2.0 ns ± 0.2 ns.

Figure 2. Switching Test Circuit Waveforms

3

10562
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	7, 9, 14				8	1, 16	3 - 6, 10 - 13
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.545	– 1.92	– 1.655	V	2, 15				8	1, 16	3 - 6, 10 - 13
V_{OL1}	Low Output Voltage	– 1.85	– 1.60	– 1.82	– 1.525	– 1.92	– 1.635	V	7, 9, 14		2, 7, 9, 14, 15	7, 9, 14	8	1, 16	3 - 6, 10 - 13
V_{OH1}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V	7, 9, 14		7, 9, 14	2, 7, 9 14, 15	8	1, 16	3 - 6, 10 - 13
I_{IH1}	Input Current High		220		375		375	µA	2, 7, 9 14, 15				8	1, 16	2, 7, 9, 14, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		2, 7, 9 14, 15			8	1, 16	2, 7, 9, 14, 15
I_{EE}	Power Supply Drain Current	– 76		– 84		– 84		mA					8	1, 16	8

10562
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	2, 7 9, 14	3 - 6, 10 -13	1, 16	8	7, 9, 14, 15	7, 9, 14, 15	3 - 6, 10 - 13
t_{THL}	Fall Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	2, 7 9, 14	3 - 6, 10 - 13	1, 16	8	7, 9, 14, 15	7, 9, 14, 15	3 - 6, 10 - 13
t_{PLH}	Propagation Delay	1.5	6.0	1.3	7.0	1.2	6.5	ns	2, 7 9, 14	3 - 6, 10 - 13	1, 16	8	7, 9, 14, 15	7, 9, 14, 15	3 - 6, 10 - 13
t_{PHL}	Propagation Delay	1.5	6.0	1.3	7.0	1.2	6.5	ns	2, 7 9, 14	3 - 6, 10 - 13	1, 16	8	7, 9, 14, 15	7, 9, 14, 15	3 - 6, 10 - 13

MOTOROLA

Error Detection-Correction Circuit

ELECTRICALLY TESTED PER:
MPG 10563

The 10563 is an error detection and correction circuit. It is a building block designed for use with memory systems. The 10563 offers economy in the design of the error detection/correction subsystems for mainframe and add-on memory systems.

For example, using eight 10563s together with eight 12-bit parity checkers (10560), single bit error detection/correction and double-bit error detection can be done on a word of 64-bit length. Only eight check bits (B_0-B_7) need be added to the word.

- 720 mW Max/Pkg (No Load)
- t_{pd} = 5.0 ns typ

3

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$P0_B$	2	6	3	51 Ω to V_{TT}
P_3	3	7	4	51 Ω to V_{TT}
B_5	4	8	5	OPEN
B_6	5	9	7	OPEN
B_2	6	10	8	GND
B_1	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
B_0	9	13	12	OPEN
B_3	10	14	13	GND
B_7	11	15	14	GND
B_4	12	16	15	OPEN
P_2	13	1	17	51 Ω to V_{TT}
P_1	14	2	18	51 Ω to V_{TT}
$P0_A$	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/– 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

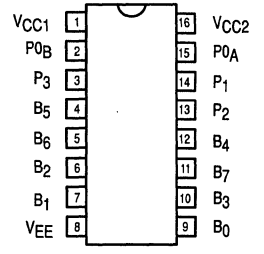
Military 10563

AVAILABLE AS

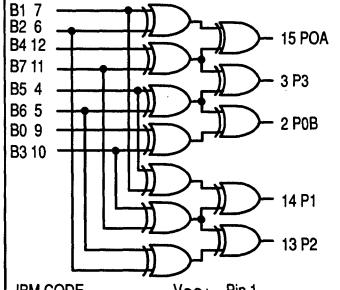
1) JAN: N/A
2) SMD: N/A
3) 883: 10563/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

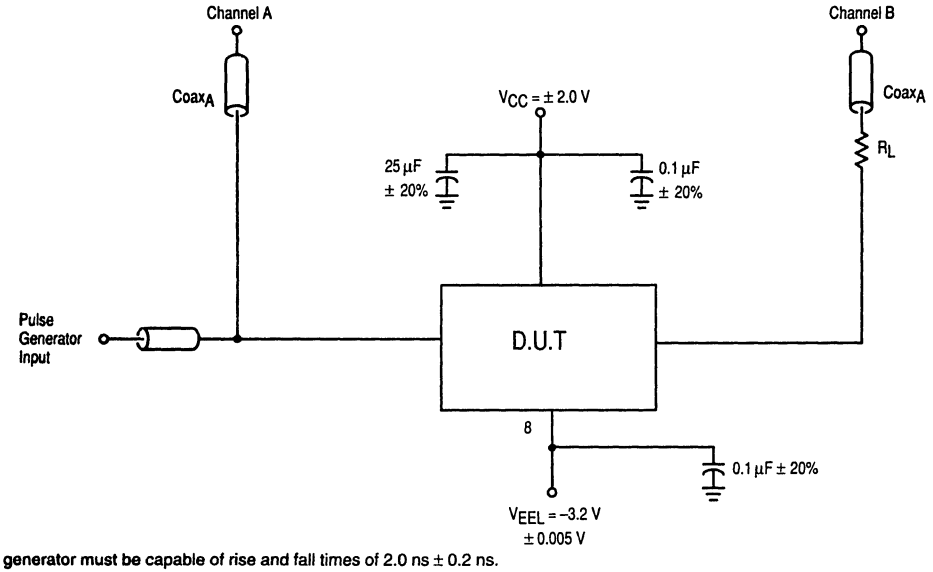


LOGIC DIAGRAM



IBM CODE
$P0_A$=B1,B2,B4,B7
$P0_B$=BO,B3,B5,B6
P1=B1,B3,B5,B7
P2=B2,B3,B6,B7
P3=B4,B5,B6,B7

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8



NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)
5. $R_L = 50\ \Omega$ resistor in series with 50 Ω coax constituting the 100 Ω load.
6. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
7. Unused outputs should be loaded 100 Ω to ground.

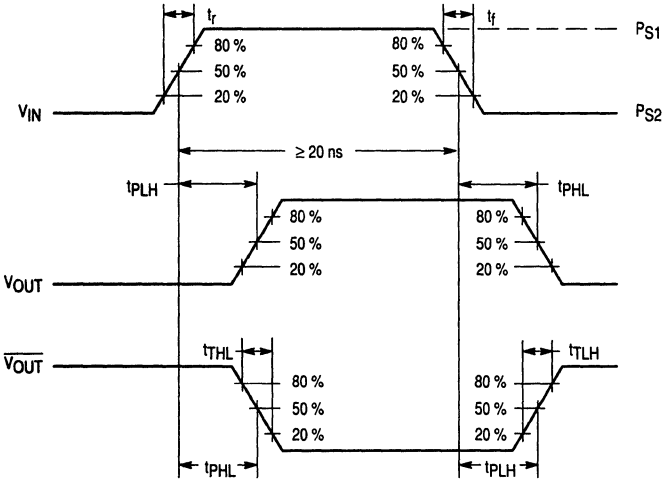


Figure 1. Switching Test Circuit and Waveforms

10563
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to − 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	− 0.93	− 0.78	− 0.825	− 0.63	− 1.08	− 0.88	V	4, 11				8	1, 16	2, 3, 13 - 15
V_{OL}	Low Output Voltage	− 1.85	− 1.62	− 1.82	− 1.545	− 1.92	− 1.655	V					8	1, 16	2, 3, 13 - 15
V_{OL1}	Low Output Voltage	− 1.85	− 1.60	− 1.82	− 1.525	− 1.92	− 1.635	V				4 - 7, 9 - 12	8	1, 16	2, 3, 13 - 15
V_{OH1}	High Output Voltage	− 0.95	− 0.78	− 0.845	− 0.63	− 1.10	− 0.88	V			4 - 7, 9 - 12		8	1, 16	2, 3, 13 - 15
I_{IH}	Input Current High		220		375		375	µA	4, 6, 10				8	1, 16	4, 6, 10
I_{IH1}	Input Current High		265		450		450	µA	5, 7, 9, 11, 12				8	16	5, 7, 9, 11 12
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 12			8	16	2, 7, 9, 14 15
I_{EE}	Power Supply Drain Current	− 125		− 138		− 138		mA					8	1, 16	8

10563
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.1	3.9	1.1	4.5	1.1	4.4	ns	4 - 7, 9 - 12	2, 3 13 -15	1, 16	8	7, 9, 14	2, 3, 13 - 15
t_{THL}	Fall Time	1.1	3.9	1.1	4.5	1.1	4.4	ns	4 - 7, 9 - 12	2, 3 13 - 15	1, 16	8	7, 9, 14	2, 3, 13 - 15
t_{PLH}	Propagation Delay	1.5	6.5	1.5	7.5	1.3	7.0	ns	4 - 7, 9 - 12	2, 3 13 - 15	1, 16	8	7, 9, 14	2, 3, 13 - 16
t_{PHL}	Propagation Delay	1.5	6.5	1.5	7.5	1.3	7.0	ns	4 - 7, 9 - 12	2, 3 13 - 15	1, 16	8	7, 9, 14	2, 3, 13 - 15

MOTOROLA

8-Line Multiplexer

ELECTRICALLY TESTED PER:
5962-8852701

The 10564 is high speed, low power eight-channel data selector which routes data preset at one-of-eight inputs to the output. The data is routed according to the three bit code present on the address inputs. An enable input is provided for easy bit expansion.

- 435 mW Max/Pkg (No Load)
- t_{pd} = 3.0 ns typ
- t_r,t_f = 2.0 ns typ (20% - 80%.)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{\text{Enable}}$	2	6	3	OPEN
X_3	3	7	4	OPEN
X_2	4	8	5	OPEN
X_1	5	9	7	OPEN
X_0	6	10	8	GND
A	7	11	9	OPEN
V_{EE}	8	12	10	VEE
B	9	13	12	OPEN
C	10	14	13	OPEN
X_4	11	15	14	OPEN
X_5	12	16	15	OPEN
X_6	13	1	17	OPEN
X_7	14	2	18	OPEN
Z	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/– 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Truth Table

	Address Input			
$\overline{\text{Enable}}$	C	B	A	Z
L	L	L	L	X_0
L	L	L	H	X_1
L	L	H	L	X_2
L	L	H	H	X_3
L	H	L	L	X_4
L	H	L	H	X_5
L	H	H	L	X_6
L	H	H	H	X_7
H	∅	∅	∅	L

∅ = Don't Care

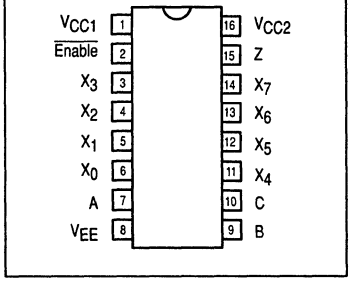
Military 10564

AVAILABLE AS

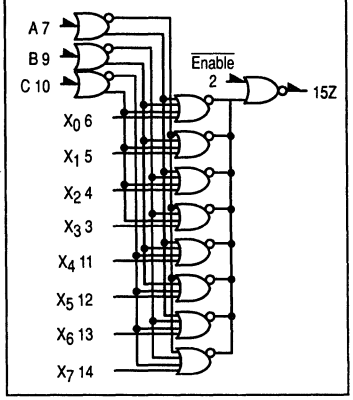
1) JAN: N/A
2) SMD: 5962-8852701
3) 883: 10564/BXAJC
X = CASE OUTLINE AS FOLLOWS:

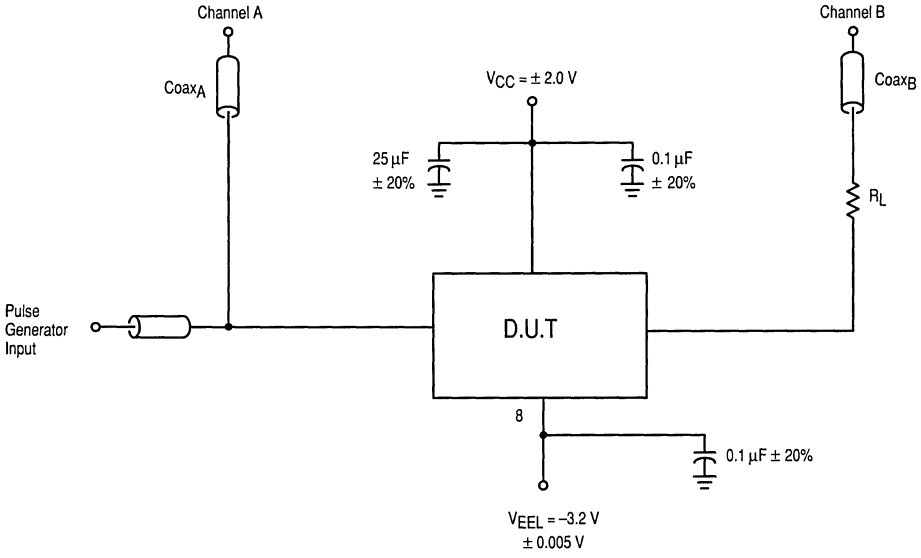
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

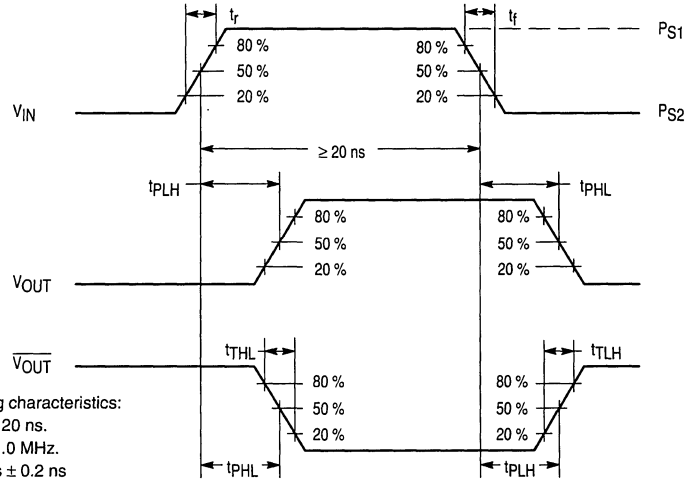


LOGIC DIAGRAM





NOTES
1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of Coax$_A$ and Coax$_B$ should be equal for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 2.0 ns ± 0.2 ns (20% to 80%)
5. R_L = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.



NOTES
1. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) $t_r = t_f$ = 2.0 ns ± 0.2 ns

Figure 1. Switching Test Circuit and Waveforms

10564
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	4 - 7, 9 - 14	2, 7, 9, 10			8	1, 16	15
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.545	– 1.92	– 1.655	V	2, 7, 9 - 14	2, 7, 9 - 14			8	1, 16	15
V_{OL1}	Low Output Voltage	– 1.85	– 1.60	– 1.82	– 1.525	– 1.92	– 1.635	V	7, 9	2, 7, 10, 14	2, 9, 10	3, 5, 6, 11 - 14	8	1, 16	15
V_{OH1}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V	3 - 7, 9 - 13	2, 7, 9, 10	7, 9, 15	3 - 7, 9 - 14	8	1, 16	15
I_{IH1}	Input Current High		265		450		450	µA	2 - 7, 9 - 11				8	1, 16	2 - 7, 9 - 11
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		2 - 7, 9 - 14			8	1, 16	2, 7, 9, 14, 15
I_{EE}	Power Supply Drain Current	– 75		– 83		– 83		mA					8	1, 16	8

10564
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	0.9	3.4	0.9	3.3	ns	2 - 5, 7, 9, 10	15	1, 16	8	2 - 7, 9 - 14	2 - 7, 9 - 14	15
t_{THL}	Fall Time	1.1	3.3	0.9	3.4	0.9	3.3	ns	2 - 5, 7, 9, 10	15	1, 16	8	2 - 7, 9 - 14	2 - 7, 9 - 14	15
t_{PLH}	Propagation Delay Enable to Output	1.0	3.1	0.9	3.1	0.9	3.2	ns	2 - 5, 7, 9, 10	15	1, 16	8	2 - 7, 9 - 14	2 - 7, 9 - 14	15
t_{PLH}	Propagation Delay A, B, C to Output	2.0	6.2	1.9	6.2	1.8	6.3	ns	2 - 5, 7, 9, 10	15	1, 16	8	2 - 7, 9 - 14	2 - 7, 9 - 14	15
t_{PHL}	Propagation Delay Data to Output	1.5	4.7	1.2	4.7	1.3	4.8	ns	2 - 5, 7, 9, 10	15	1, 16	8	2 - 7, 9 - 14	2 - 7, 9 - 14	15

Military 10565

8-Input Priority Decoder

ELECTRICALLY TESTED PER:
5962-9056101

The 10565 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the dock goes high. This device is very useful for a variety of applications in checking system status in control processors, peripheral controllers, and testing systems.

The input is active when high, (e. g., the three binary outputs are low when input DO is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary. The 10565 can also be used to develop binary codes from random logic inputs, for addressing ROMs, RAMs, or for multiplexing data.

- 750 mW Max/Pkg (No Load)
- t_{pd} = 4.5 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-9056101
3) 883: 10565/BXAJC
X = CASE OUTLINE AS FOLLOWS:

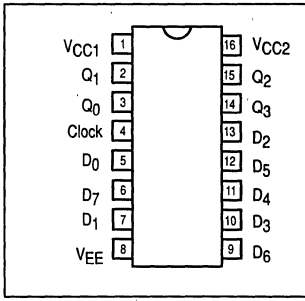
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

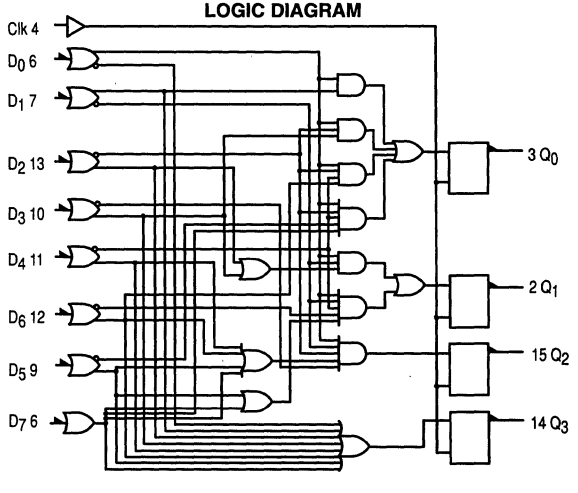
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω to V_{TT}
Q_0	3	7	4	51 Ω to V_{TT}
Clock	4	8	5	OPEN
D_0	5	9	7	OPEN
D_7	6	10	8	GND
D_1	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
D_6	9	13	12	OPEN
D_3	10	14	13	OPEN
D_4	11	15	14	OPEN
D_5	12	16	15	OPEN
D_2	13	1	17	OPEN
Q_3	14	2	18	51 Ω to V_{TT}
Q_2	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.2 V MIN/ – 2.0 V MAX
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



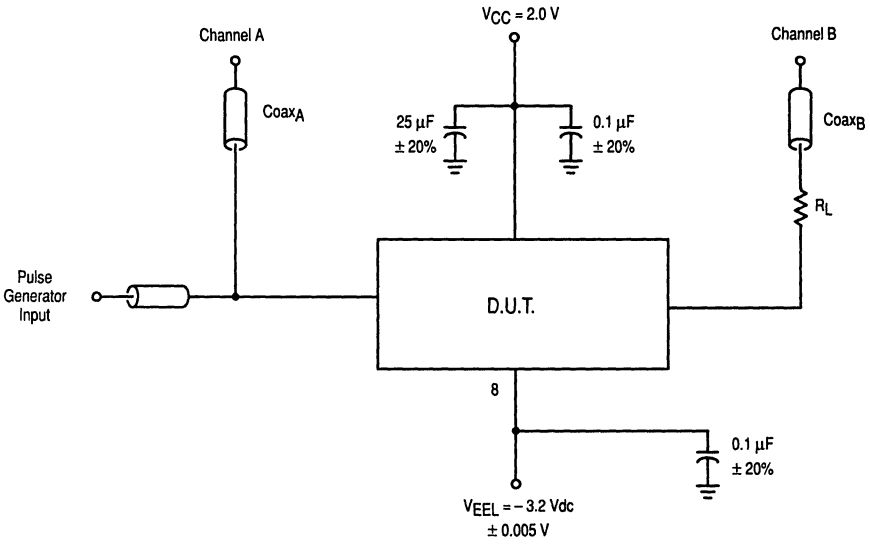
LOGIC DIAGRAM



TRUTH TABLE

DATA INPUTS								OUTPUTS			
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Q_3	Q_2	Q_1	Q_0
H	Ø	Ø	Ø	Ø	Ø	Ø	Ø	H	L	L	L
L	H	Ø	Ø	Ø	Ø	Ø	Ø	H	L	L	H
L	L	H	Ø	Ø	Ø	Ø	Ø	H	L	H	L
L	L	L	H	Ø	Ø	Ø	Ø	H	L	H	H
L	L	L	L	H	Ø	Ø	Ø	H	H	L	L
L	L	L	L	L	H	Ø	Ø	H	H	L	H
L	L	L	L	L	L	H	Ø	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

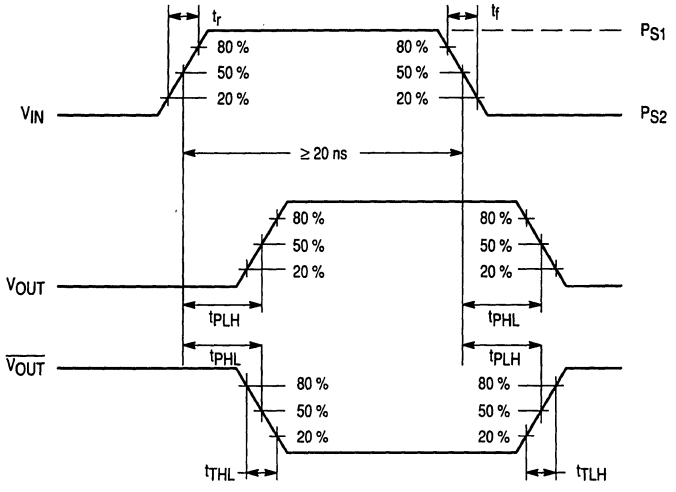
Ø = Don't Care

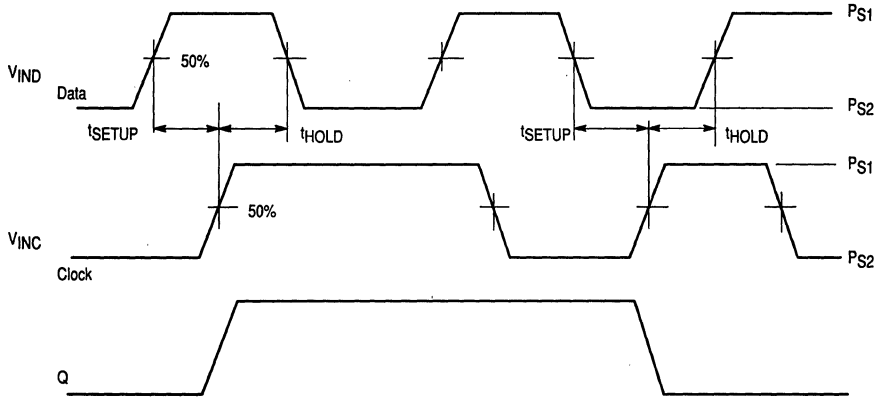


NOTES

1. The Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns
2. Length of $Coax_A$ and $Coax_B$ should be of equal lengths for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0$ ns (20% – 80%) ± 0.2 ns.
5. $R_L = 50\ \Omega$ resistor in series with 50 Ω coax constituting 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground.

Figure 1. Switching Test Circuit





NOTES

1. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

Figure 2. Switching Test Circuit Waveforms

10565
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to − 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	− 0.93	− 0.78	− 0.825	− 0.63	− 1.08	− 0.88	V	6				8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	− 1.85	− 1.62	− 1.82	− 1.545	− 1.92	− 1.655	V	6				8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage	− 1.85	− 1.60	− 1.82	− 1.525	− 1.92	− 1.635	V	6	4, 6	4, 5, 7, 9 - 13	4 - 7, 9 - 13	8	1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	− 0.95	− 0.78	− 0.845	− 0.63	− 1.10	− 0.88	V		4, 6	4 - 7, 9 - 13		8	1, 16	2, 3, 14, 15
I_{IH}	Input Current High		220		375		375	µA	5 - 7, 9 - 13				8	1, 16	2, 3, 14, 15
I_{IH1}	Input Current High		245		415		415	µA	4				8	1, 16	4
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 13			8	1, 16	4 - 7, 9 - 13
I_{EE}	Power Supply Drain Current	− 131		− 144		− 144		mA					8	1, 16	8

10565
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.1	4.5	1.1	3.8	ns	4 - 7, 9 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.1	4.5	1.1	3.8	ns	4 - 7, 9 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH}/ t_{PHL}	Propagation Delay Data to Output	2.0	7.0	2.0	8.5	2.0	7.5	ns	4 - 7, 9 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL}/ t_{PLH}	Propagation Delay Clock to Output	1.5	4.0	1.5	5.5	1.5	5.0	ns	4 - 7, 9 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{SET}	Setup Time	6.0		6.0		6.0		ns	4 - 7, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{HOLD}	Hold Time	1.0		1.0		1.0		ns	4 - 7, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15

Military 10566

5-Bit Magnitude Comparator

ELECTRICALLY TESTED PER:
MPG 10566

The 10566 is a high speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A < B and A > B. A = B can be obtained by NORing the two outputs with an additional gate. A high level on the enable function forces both outputs low. Multiple 10566s may be used for larger word comparisons.

- 610 mW Max/Pkg (No Load)
- t_{pd} = Data to Output 6.0 ns typ
  $\overline{E}$ to Output 2.5 ns typ

AVAILABLE AS

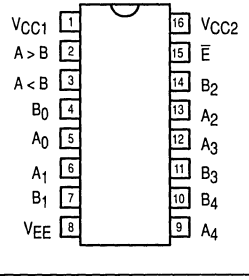
1) JAN: N/A
2) SMD: N/A
3) 883: 10566/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A > B	2	6	3	51 Ω to V_{TT}
A < B	3	7	4	51 Ω to V_{TT}
B_0	4	8	5	OPEN
A_0	5	9	7	OPEN
A_1	6	10	8	OPEN
B_1	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
A_4	9	13	12	OPEN
B_4	10	14	13	GND
B_3	11	15	14	OPEN
A_3	12	16	15	OPEN
A_2	13	1	17	OPEN
B_2	14	2	18	OPEN
$\overline{E}$	15	3	19	GND
V_{CC2}	16	4	20	GND

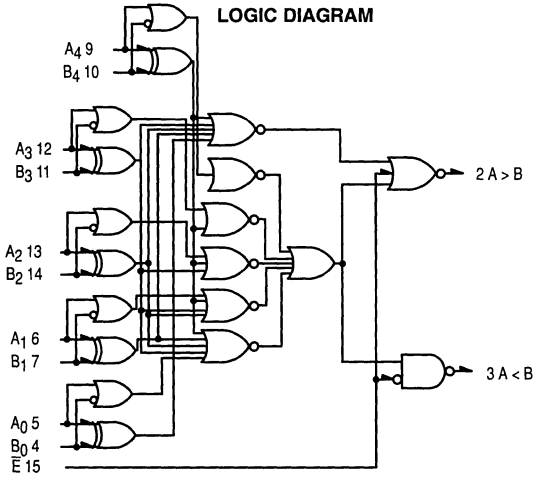


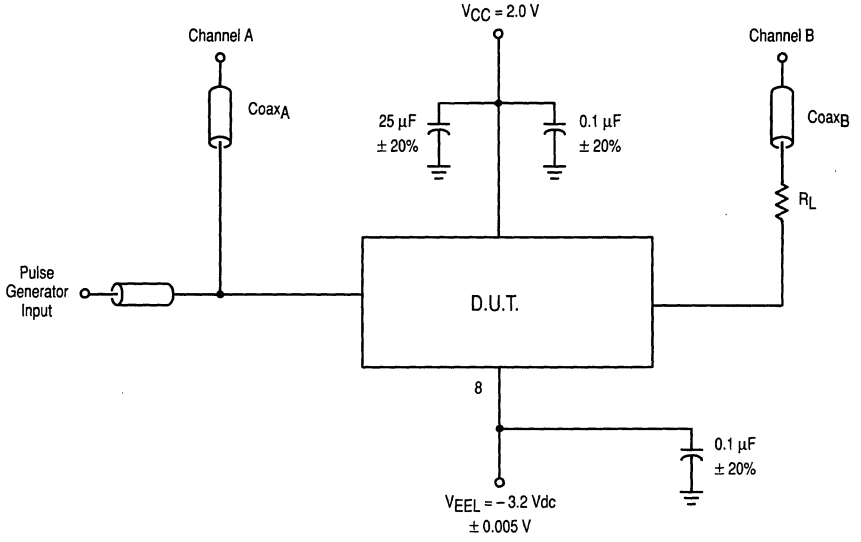
BURN - IN CONDITIONS:
V_{TT} = – 2.2 V MIN/ – 2.0 V MAX
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

TRUTH TABLE

Inputs			Outputs	
$\overline{E}$	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L

LOGIC DIAGRAM

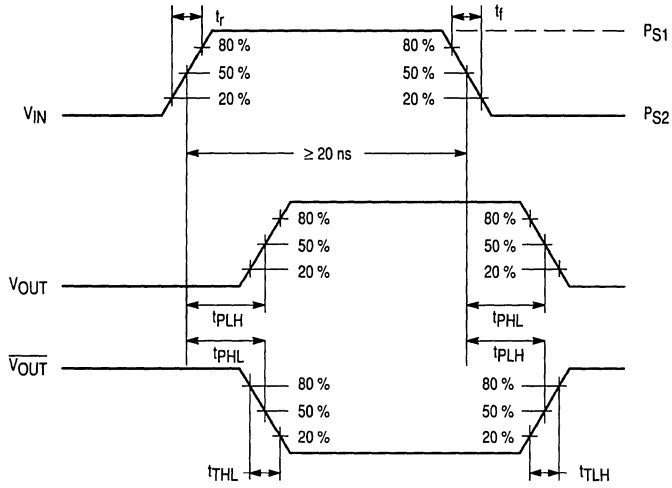




NOTES

1. The Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns
2. Length of $Coax_A$ and $Coax_B$ should be of equal lengths for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 2.0 ns (20% – 80%) ± 0.2 ns.
5. R_L = 50 Ω resistor in series with 50 Ω coax constituting 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground.

Figure 1. Switching Test Circuit



NOTES

1. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

Figure 2. Switching Test Circuit Waveforms

3

10566
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4, 5				8	1, 16	2, 3
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4, 5, 15				8	1, 16	2, 3
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	4, 5		15	4 - 7, 9 - 14	8	1, 16	2, 3
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	4, 5		4 - 7, 9 - 14		8	1, 16	2, 3
I_{IH}	Input Current High		220		375		375	µA	4 - 7, 9 - 15				8	1, 16	4 - 7, 9 - 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 15			8	1, 16	4 - 7, 9 - 15
I_{EE}	Power Supply Drain Current	- 106		- 117		- 117		mA					8	1, 16	8

10566
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.5	1.1	4.1	1.1	3.8	ns	2 - 5, 7, 9, 10	2, 3	1, 16	8	2, 3
t_{THL}	Fall Time	1.1	3.5	1.1	4.1	1.1	3.8	ns	2 - 5, 7, 9, 10	2, 3	1, 16	8	2, 3
t_{PLH}/ t_{PHL}	Propagation Delay Data to Output	1.0	3.6	1.0	4.2	1.0	3.9	ns	2 - 5, 7, 9, 10	2, 3	1, 16	8	2, 3
t_{PHL}/ t_{PLH}	Propagation Delay Clock to Output	1.0	7.6	1.0	8.9	1.0	8.2	ns	2 - 5, 7, 9, 10	2, 3	1, 16	8	2, 3

Military 10568

Quad Latch

ELECTRICALLY TESTED PER:
MPG 10568

The 10568 is a Quad Latch with common clocking to all four latches. Separate output enabling gates are provided for each latch, allowing direct wiring to a bus. When the clock is high, outputs will follow the D inputs. Information is latched on the negative-going transition of the clock.

- 435 mW Max/Pkg (No Load)
- $t_{pd} = \overline{G}$ to Q = 2.0 ns typ
  = D to Q = 3.0 ns typ
  = C to Q = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

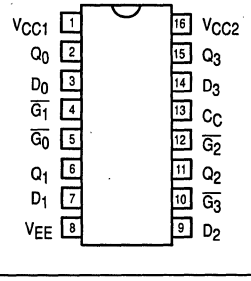
1) JAN: N/A
2) SMD: N/A
3) 883: 10568/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_0	2	6	3	51 Ω to V_{TT}
D_0	3	7	4	GND
$\overline{G_1}$	4	8	5	OPEN
$\overline{G_0}$	5	9	7	OPEN
Q_1	6	10	8	51 Ω to V_{TT}
D_1	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
D_2	9	13	12	GND
$\overline{G_3}$	10	14	13	OPEN
Q_2	11	15	14	51 Ω to V_{TT}
$\overline{G_2}$	12	16	15	OPEN
C_C	13	1	17	GND
D_3	14	2	18	GND
Q_3	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



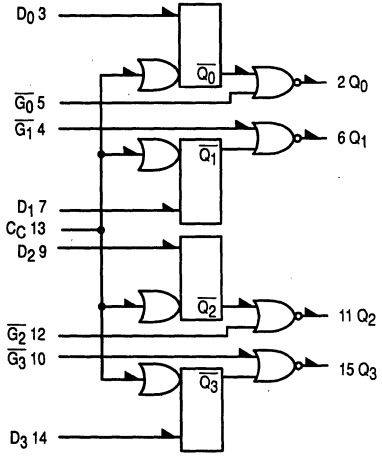
BURN - IN CONDITIONS:
V_{TT} = – 2.2 V MIN/ – 2.0 V MAX
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

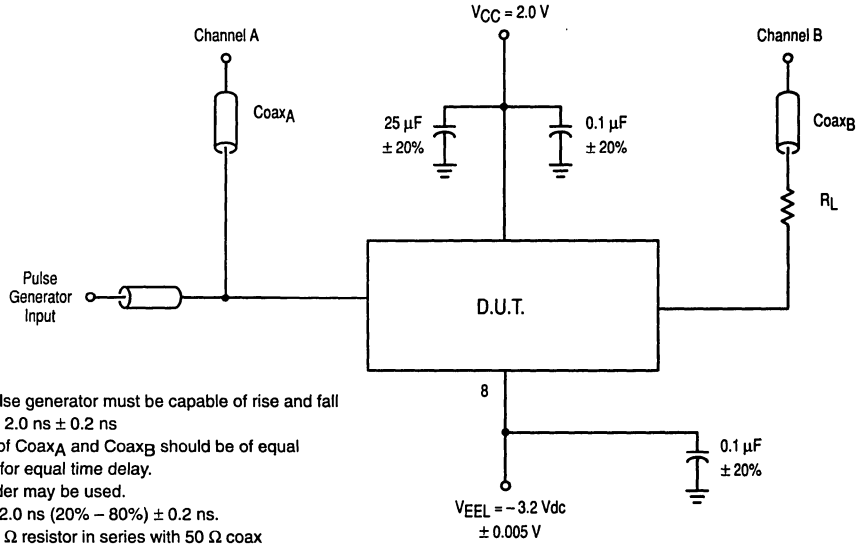
TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	Ø	Ø	L
L	L	Ø	Q_n
L	H	L	L
L	H	H	H

Ø = Don't Care

LOGIC DIAGRAM

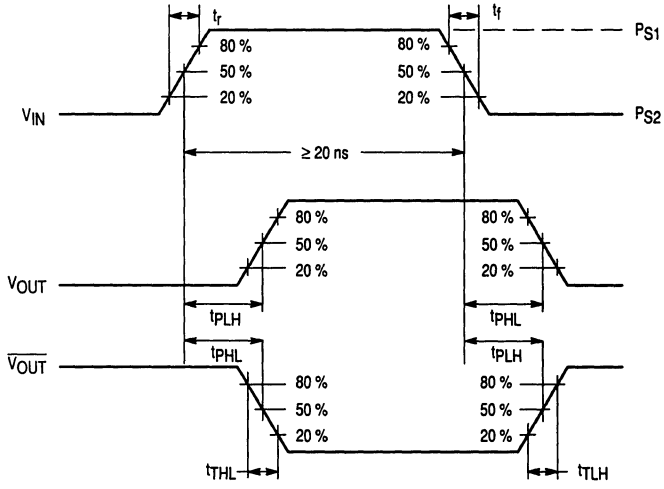




NOTES

1. The Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns
2. Length of Coax$_A$ and Coax$_B$ should be of equal lengths for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 2.0 ns (20% – 80%) ± 0.2 ns.
5. R_L = 50 Ω resistor in series with 50 Ω coax constituting 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground.

Figure 1. Switching Test Circuit



NOTES

1. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

Figure 2. Switching Test Circuit Waveform

10568
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to − 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	− 0.93	− 0.78	− 0.825	− 0.63	− 1.08	− 0.88	V	3, 7, 9, 13, 14				8	1, 16	2, 6, 11, 15
V_{OL}	Low Output Voltage	− 1.85	− 1.62	− 1.82	− 1.545	− 1.92	− 1.655	V	3 - 5, 7, 9, 10, 12 - 14				8	1, 16	2, 6, 11, 15
V_{OL1}	Low Output Voltage		− 1.60		− 1.525		− 1.635	V	3, 7, 9, 13, 14		4, 5, 10, 12	3, 7, 9, 14	8	1, 16	2, 6, 11, 15
V_{OH1}	High Output Voltage	− 0.95		− 0.845		− 1.10		V	3, 7, 9, 13, 14		3, 7, 9, 14	4, 5, 10, 12	8	1, 16	2, 6, 11, 15
I_{IH1}	Input Current High		290		495		495	µA	13				8	1, 16	13
I_{IH2}	Input Current High		245		415		415	µA	3, 7, 9, 14				8	1, 16	3, 7, 9, 14
I_{IH3}	Input Current High		265		450		450	µA	4, 5, 10, 12				8	1, 16	4, 5, 10, 12
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 5, 7, 9, 10, 12 - 14			8	1, 16	3 - 5, 7, 9, 10, 12 - 14
I_{EE}	Power Supply Drain Current	− 75		− 83		− 83		mA					8	1, 16	8

10568
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.5	1.0	4.0	1.0	3.9	ns	3 - 5, 7, 9, 10, 12 - 14	2, 6, 11, 15	1, 16	8			2, 6, 11, 15
t_{THL}	Fall Time	1.1	3.5	1.0	4.0	1.0	3.9	ns	3 - 5, 7, 9, 10, 12 - 14	2, 6, 11, 15	1, 16	8			2, 6, 11, 15
t_{PHL}/ t_{PLH}	Propagation Delay Clock to Output	1.0	5.6	1.0	6.6	1.0	6.1	ns	3 - 5, 7, 9, 10, 12 - 14	2, 6, 11, 15	1, 16	8		5, 10, 13	2, 6, 11, 15
t_{PHL}/ t_{PLH}	Propagation Delay Data to Output	1.0	5.4	1.0	6.3	1.0	5.8	ns	3 - 5, 7, 9, 10, 12 - 14	2, 6, 11, 15	1, 16	8		5, 10, 13	2, 6, 11, 15
t_{PHL}/ t_{PLH}	Propagation Delay Gate to Output	1.0	3.1	1.0	3.6	1.0	3.4	ns	3 - 5, 7, 9, 10, 12 - 14	2, 6, 11, 15	1, 16	8	7, 9, 14		2, 6, 11, 15
t_S	Setup Time	2.5		2.5		2.5		ns	3, 7, 9, 11, 14	2, 6, 11, 15	1, 16	8			2, 6, 11, 15
t_H	Hold Time	1.0		1.0		1.0		ns	3, 7, 9, 11, 14	2, 6, 11, 15	1, 16	8			2, 6, 11, 15

9 + 2-Bit Parity Generator-Checker

Military 10570

ELECTRICALLY TESTED PER:
MPG 10570

The 10570 is a 11-bit parity circuit, which is segmented into 9 data bits and 2 control bits. Output A generates odd parity on 9-bits; that is, Output A goes high for an odd number of high logic levels on the bit inputs in only 2 gate delays.

The control inputs can be used to expand parity to larger numbers of bits with minimal delay or can be used to generate even parity. To expand parity to larger words, the 10570 can be used with the 10560 or other 10570's. The 10570 can generate both even and odd parity.

- 410 mW Max/Pkg (No Load)
- t_{pd} = 2.5 ns typ (Control Inputs to B Output)
  = 4.0 ns typ (Data Inputs to A Output)
  = 6.0 ns typ (Data Inputs to B Output)
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

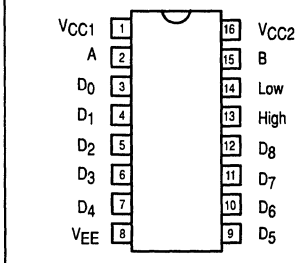
1) JAN: N/A
2) SMD: N/A
3) 883: 10570/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

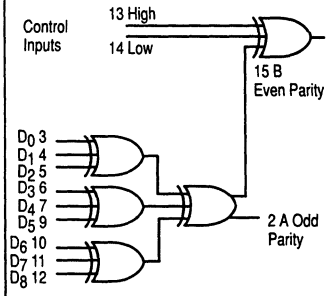
The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A	2	6	3	51 Ω to V_{TT}
D_0	3	7	4	GND
D_1	4	8	5	OPEN
D_2	5	9	7	OPEN
D_3	6	10	8	OPEN
D_4	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
D_5	9	13	12	OPEN
D_6	10	14	13	OPEN
D_7	11	15	14	OPEN
D_8	12	16	15	OPEN
High	13	1	17	OPEN
Low	14	2	18	OPEN
B	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Truth Table

Inputs	Outputs	
Sum of D Inputs at High Level	Odd Parity Output A	Even Parity Output B
Even	Low	High
Odd	High	Low

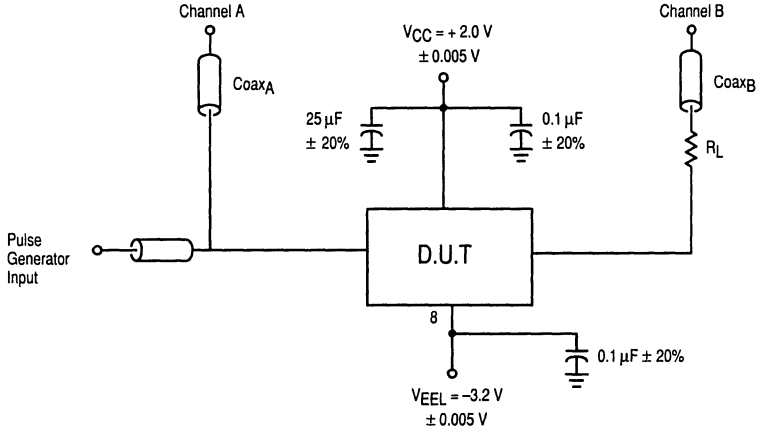
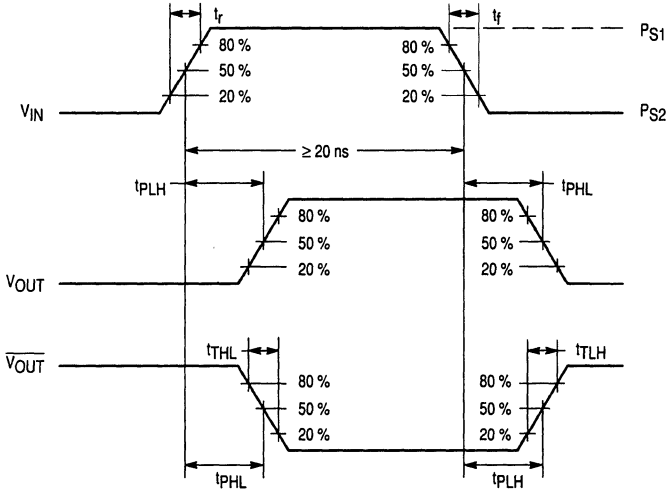


Figure 1. Switching Test Circuit and Waveforms



NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. 2:1 divider may be used.
3. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)
5. $R_L = 50\ \Omega$ resistor in series with 50 Ω coax constituting the 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground
7. PW ≥ 20 ns.
8. $f_{IN} = 1.0$ MHz.

Figure 2

10570
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	3 - 7, 9 - 14				8	1, 16	2, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	3 - 7, 9 - 14				8	1, 16	2, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 1.63	- 1.10	- 0.88	V			3 - 7, 9 - 14		8	1, 16	2, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 0.82	- 1.525	- 1.92	- 1.635	V				3 - 7, 9 - 14	8	1, 16	2, 15
I_{EE}	Power Supply Drain Current	- 71		- 78		- 78		mA					8	1, 16	8
I_{IH}	Input Current High		220		375		375	µA	3 - 7, 9 - 14				8	1, 16	3 - 7, 9 - 14
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 7, 9 - 14			8	1, 16	3 - 7, 9 - 14

10570
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	V_{EE}	P. U. T.
t_{TLH}	Rise Time	1.5	3.9	1.5	4.8	1.5	4.5	ns	3, 7, 11, 13	2, 15	1, 16	8	16	2, 15
t_{THL}	Fall Time	1.5	3.9	1.5	4.8	1.5	4.5	ns	3, 7, 11, 13	2, 15	1, 16	8	16	2, 15
t_{PLH}/ t_{PHL}	Propagation Delay Carry Input to B	1.5	4.0	1.5	4.8	1.5	4.6	ns	3, 7, 11, 13	2, 15	1, 16	8	16	2, 15
t_{PHL}/ t_{PLH}	Propagation Delay Other Inputs to A	2.0	6.0	2.0	8.0	2.0	7.5	ns	3, 7, 11, 13	2, 15	1, 16	8	16	2, 15
t_{pd}/t_{pd}	Propagation Delay Other Inputs to B	2.0	8.8	4.0	10.5	4.0	10.0	ns	3, 7, 11, 13	2, 15	1, 16	8	16	2, 15

Dual Binary to 1-4 Decoder (Low)

Military 10571

ELECTRICALLY TESTED PER:
MPG 10571

The 10571 is a binary coded 2 line to dual 4 line decoder with selected outputs low. With either $\overline{E0}$ or $\overline{E1}$ high, the corresponding selected 4 outputs are high. The common enable $\overline{E}$, when high, forces all outputs high.

- 445 mW Max/Pkg (No Load)
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{E_1}$	2	6	3	GND
Q13	3	7	4	51 Ω to V_{TT}
Q12	4	8	5	51 Ω to V_{TT}
Q11	5	9	7	51 Ω to V_{TT}
Q10	6	10	8	51 Ω to V_{TT}
B	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
A	9	13	12	OPEN
Q03	10	14	13	51 Ω to V_{TT}
Q02	11	15	14	51 Ω to V_{TT}
Q01	12	16	15	51 Ω to V_{TT}
Q00	13	1	17	51 Ω to V_{TT}
$\overline{E_0}$	14	2	18	GND
$\overline{E}$	15	3	19	GND
V_{CC2}	16	4	20	GND

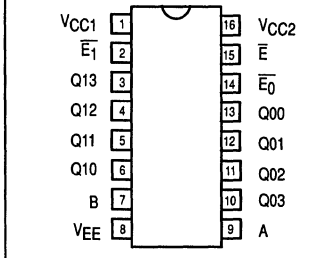
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

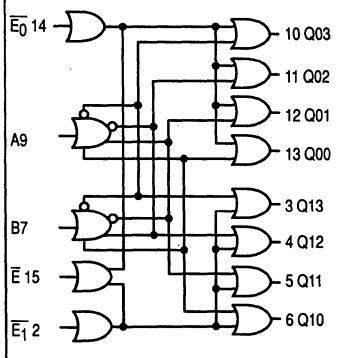
1) JAN: N/A
2) SMD: N/A
3) 883: 10571/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



TRUTH TABLE

Enable Inputs			Inputs		Outputs							
$\overline{E}$	$\overline{E_0}$	$\overline{E_1}$	A	B	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{00}	Q_{01}	Q_{02}	Q_{03}
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	Ø	Ø	Ø	Ø	H	H	H	H	H	H	H	H

Ø = Don't Care

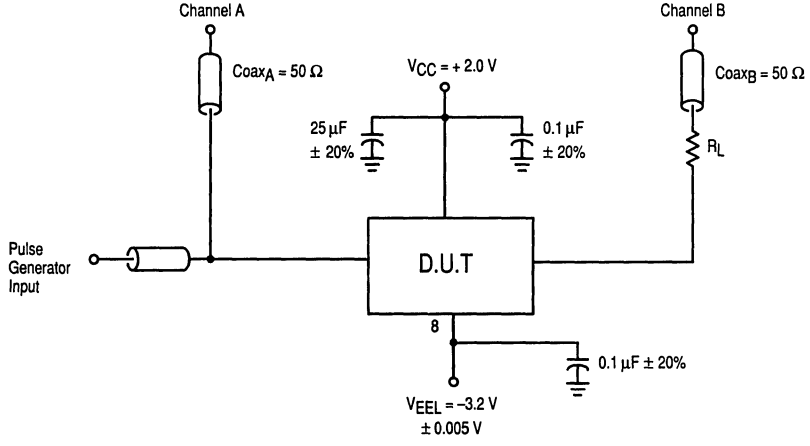
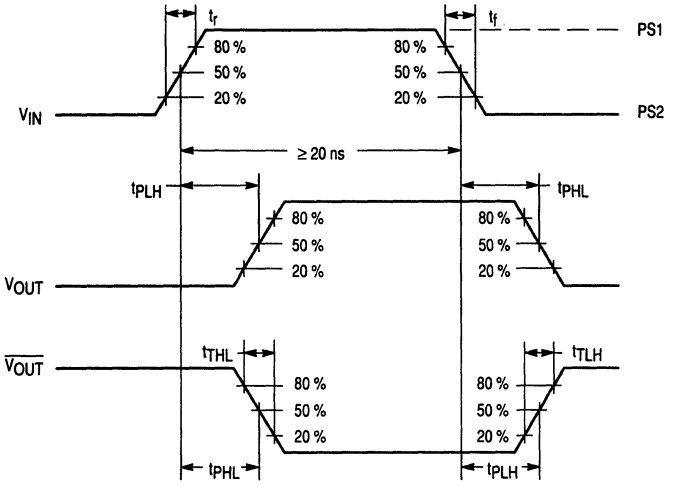


Figure 1. Switching Test Circuit



NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. 2:1 divider may be used.
3. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)
5. $R_L = 50\ \Omega$ resistor in series with 50 Ω coax constituting the 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground

NOTES

V_{IN} has the following characteristics:

a) PW ≥ 20 ns.
b) $f_{IN} = 1.0$ MHz.
c) t_r and $t_f = 2.0$ ns ± 0.2 ns. (20% - 80%)

Figure 2. Switching Test Circuit Waveforms

10571
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	15				8	1, 16	3 - 6, 10 - 13
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	7, 9				8	1, 16	3 - 6, 10 - 13
V_{OH1}	High Output Voltage		- 1.60		- 1.525		- 1.635	V	7, 9			4 - 7, 14, 15	8	1, 16	3 - 6, 10 - 13
V_{OL1}	Low Output Voltage	- 0.95		- 0.845		- 1.10		V	7, 9		4 - 7, 14, 15		8	1, 16	3 - 6, 10 - 13
I_{IH1}	Input Current High		220		375		375	µA	2, 7, 9, 14, 15				8	1, 16	2, 7, 9, 14, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		2, 7, 9, 14, 15	3 - 7, 9 - 13		8	1, 16	2, 7, 9, 14, 15
I_{EE}	Power Supply Drain Current	- 77		- 85		- 85		mA					8	1, 16	8

10571
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	2, 7, 9, 14, 15	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	1, 2, 14, 15
t_{THL}	Fall Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	2, 7, 9, 14, 15	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	1, 2, 14, 15
t_{PLH}	Propagation Delay	1.5	6.0	1.2	7.0	1.3	6.5	ns	2, 7, 9, 14, 15	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	1, 2, 14, 15
t_{PHL}	Propagation Delay	1.5	6.0	1.2	7.0	1.3	6.5	ns	2, 7, 9, 14, 15	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	1, 2, 14, 15

Dual Binary to 1-4 Decoder (High)

Military 10572

ELECTRICALLY TESTED PER:
MPG 10572

The 10572 is a binary coded 2 line to dual 4 line decoder with selected outputs high. With either $\overline{E}_0$ or $\overline{E}_1$ low, the corresponding selected 4 outputs are low. The common enable $\overline{E}$, when high, forces all outputs low.

- 445 mW Max/Pkg (No Load)
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10572/BXAJC
X = CASE OUTLINE AS FOLLOWS:

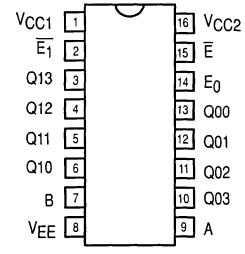
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

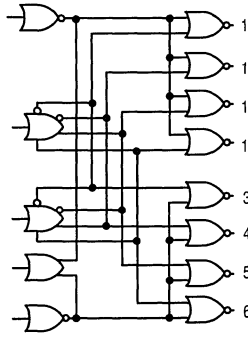
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{E_1}$	2	6	3	GND
Q13	3	7	4	51 Ω to V_{TT}
Q12	4	8	5	51 Ω to V_{TT}
Q11	5	9	7	51 Ω to V_{TT}
Q10	6	10	8	51 Ω to V_{TT}
B	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
A	9	13	12	OPEN
Q03	10	14	13	51 Ω to V_{TT}
Q02	11	15	14	51 Ω to V_{TT}
Q01	12	16	15	51 Ω to V_{TT}
Q00	13	1	17	51 Ω to V_{TT}
$\overline{E_0}$	14	2	18	GND
$\overline{E}$	15	3	19	OPEN
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM



TRUTH TABLE

Enable Inputs			Inputs		Outputs							
$\overline{E}$	$\overline{E_0}$	$\overline{E_1}$	A	B	Q_{10}	Q_{11}	Q_{12}	Q_{13}	Q_{00}	Q_{01}	Q_{02}	Q_{03}
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	Ø	Ø	Ø	Ø	L	L	L	L	L	L	L	L

Ø = Don't Care

3

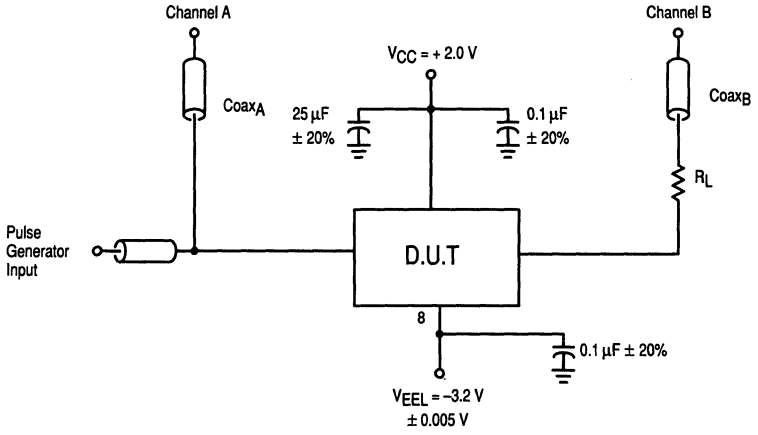
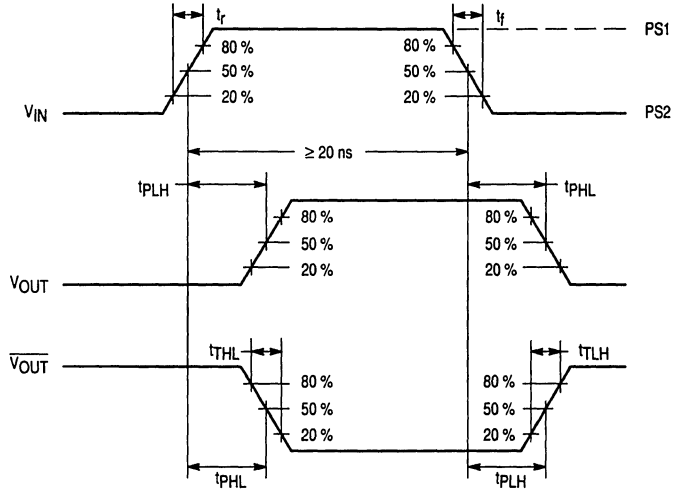


Figure 1. Switching Test Circuit



NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. 2:1 divider may be used.
3. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)
5. $R_L = 50\ \Omega$ resistor in series with 50 Ω coax constituting the 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground

NOTES

V_{IN} has the following characteristics:

a) PW ≥ 20 ns.
b) $f_{IN} = 1.0$ MHz.
c) t_r and $t_f = 2.0$ ns ± 0.2 ns. (20% - 80%)

Figure 2. Switching Test Circuit Waveforms

10572
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	2, 7, 9, 14				8	1, 16	3 - 6, 10 - 13
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.635	V	15				8	1, 16	3 - 6, 10 - 13
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	2, 7, 9, 14		2, 7, 9, 14		8	1, 16	3 - 6, 10 - 13
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	2, 7, 9, 14		2, 7, 9, 14	7, 15	8	1, 16	3 - 6, 10 - 13
I_{IH1}	Input Current High		220		375		375	µA	2, 7, 9, 14, 15				8	1, 16	2, 7, 9, 14, 15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		2, 7, 9, 14, 15			8	1, 16	2, 7, 9, 14, 15
I_{EE}	Power Supply Drain Current	- 77		- 85		- 85		mA					8	1, 16	8

10572
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	2, 7, 9, 14, 15	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13
t_{THL}	Fall Time	1.1	3.3	1.0	3.9	1.0	3.6	ns	2, 7, 9, 14, 15	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13
t_{PLH}	Propagation Delay	1.5	6.0	1.2	7.0	1.3	6.5	ns	2, 7, 9, 14, 15	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13
t_{PHL}	Propagation Delay	1.5	6.0	1.2	7.0	1.3	6.5	ns	2, 7, 9, 14, 15	3 - 6, 10 - 13	1, 16	8	2, 7, 9, 14	3 - 6, 10 - 13

Quad 2-Input Multiplexer/Latch

Military 10573

ELECTRICALLY TESTED PER:
MPG 10573

The 10573 is a quad two channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, and D31. Any change on the data input will be reflected at the outputs while the clock is low.

The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not effect the output information.

- 380 mW Max/Pkg (No Load)
- t_{pd} = 2.5 ns typ (All Output Loaded)
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
Q0	1	5	2	51 Ω to V_{TT}
Q1	2	6	3	51 Ω to V_{TT}
D11	3	7	4	GND
D10	4	8	5	OPEN
D01	5	9	7	GND
D00	6	10	8	OPEN
Clock	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
Select	9	13	12	OPEN
D31	10	14	13	GND
D30	11	15	14	OPEN
D21	12	16	15	GND
D20	13	1	17	OPEN
Q3	14	2	18	51 Ω to V_{TT}
Q2	15	3	19	51 Ω to V_{TT}
V_{CC}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

TRUTH TABLE

Inputs		Output
Select	Clock	$Q0_{n+1}$
H	L	D00
L	L	D01
Ø	L	$Q0_n$

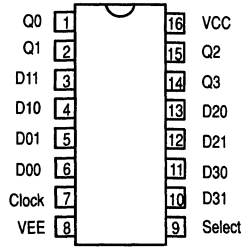
Ø = Don't Care

AVAILABLE AS

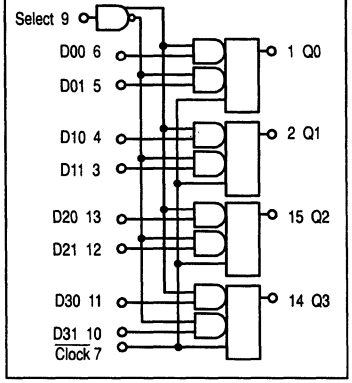
1) JAN: N/A
2) SMD: N/A
3) 883: 10573/BXAJC
X = CASE OUTLINE AS FOLLOWS:

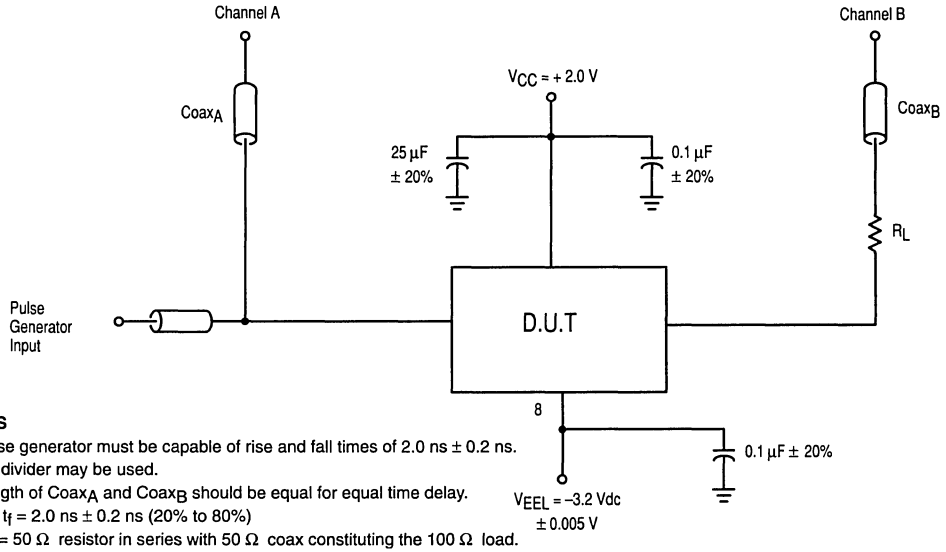
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. 2:1 divider may be used.
3. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
4. $t_r = t_f$ = 2.0 ns ± 0.2 ns (20% to 80%)
5. R_L = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground

NOTES

V_{IN} has the following characteristics:

a) PW ≥ 20 ns.
b) f_{IN} = 1.0 MHz.
c) t_r and t_f = 1.0 ns ± 0.1 ns. (20% - 80%)

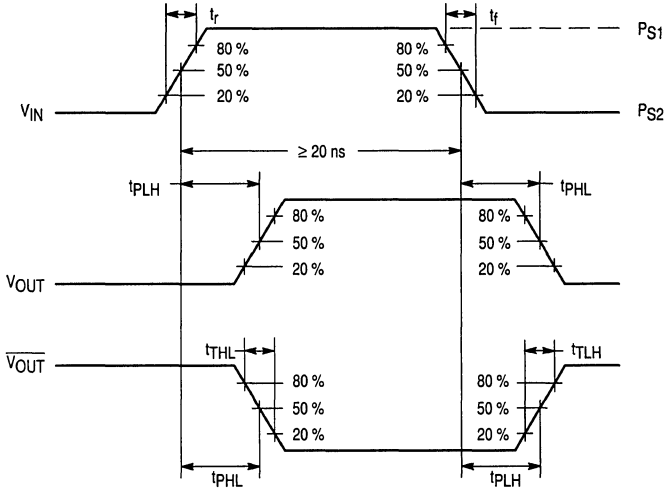


Figure 1. Switching Test Circuit and Waveforms

10573
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	3, 5, 10, 12				8	16	1, 2, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	3 - 7, 9 - 13	3, 5, 10, 12	7, 9	3 - 7, 9 - 13	8	16	1, 2, 14, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	3 - 7, 9 - 13	3, 5, 7, 10 - 13	3 - 7, 9 - 13	7, 9	8	16	1, 2, 14, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V					8	16	1, 2, 14, 15
I_{EE}	Power Supply Drain Current	- 66		- 73		- 73		mA					8	16	8
I_{IH}	Input Current High		250		425		425	µA	7, 9				8	16	7, 9
I_{IH1}	Input Current High		295		500		500	µA	3 - 6, 10 - 13				8	16	3 - 7, 10 - 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA			3 - 7, 9 - 13		8	16	3 - 7, 10 - 13

10573
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	V_{IH}	V_{IL}	P. U. T.
t_{TLH}	Rise Time	1.5	3.5	1.4	7.5	1.0	4.2	ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8	3, 5, 10, 12			1, 2, 14, 15
t_{THL}	Fall Time	1.5	3.5	1.4	7.5	1.0	4.2	ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8	3, 5, 10, 12			1, 2, 14, 15
t_{pd}	Propagation Delay Select to Q	1.3	5.7	1.2	7.0	1.0	6.5	ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8	3, 5, 10, 12			1, 2, 14, 15
t_{pd}	Propagation Delay Data to Q	1.0	3.5	1.1	5.5	0.8	3.9	ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8	3, 5, 10, 12			1, 2, 14, 15
t_{pd}	Propagation Delay Clock to Q	1.6	6.8	1.4	7.5	1.6	7.5	ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8	3, 5, 10, 12			1, 2, 14, 15
t_{set}	Setup Time Select to Q	3.0		3.0		4.0		ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8		9	9	1
t_{set}	Setup Time Data to Q	2.0		2.0		2.0		ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8		5, 6	5, 6	1
t_{hold}	Hold Time Data Input	2.5		2.5		2.5		ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8		9	9	1
t_{hold}	Hold Time Select Input	1.5		1.5		1.5		ns	3 - 7, 9 - 13	1, 2, 14, 15	16	8		5, 6	5, 6	1

Dual 4 to 1 Multiplexer

ELECTRICALLY TESTED PER:
MPG 10574

The 10574 is a high speed dual channel multiplexer with output enable capability. The select inputs determine one of four active data inputs for each multiplexer. An output enable forces both outputs low when in the high state.

- 420 mW Max/Pkg (No Load)
- t_{pd} = 3.5 ns typ (Data to Output)
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_0	2	6	3	51 Ω to V_{TT}
D00	3	7	4	OPEN
D02	4	8	5	OPEN
D01	5	9	7	GND
D03	6	10	8	GND
A	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
B	9	13	12	GND
D13	10	14	13	GND
D11	11	15	14	OPEN
D12	12	16	15	GND
D10	13	1	17	OPEN
$\overline{\text{Enable}}$	14	2	18	OPEN
Q_1	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

TRUTH TABLE

Enable	Address Inputs		Outputs	
$\overline{E}$	B	A	Q_0	Q_1
H	∅	∅	L	L
L	L	L	D00	D10
L	L	H	D01	D11
L	H	L	D02	D12
L	H	H	D03	D13

∅ = Don't Care

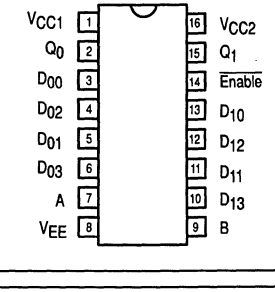
Military 10574

AVAILABLE AS

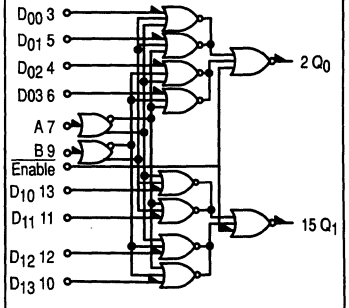
1) JAN: N/A
2) SMD: N/A
3) 883: 10574/BXAJC
X = CASE OUTLINE AS FOLLOWS:

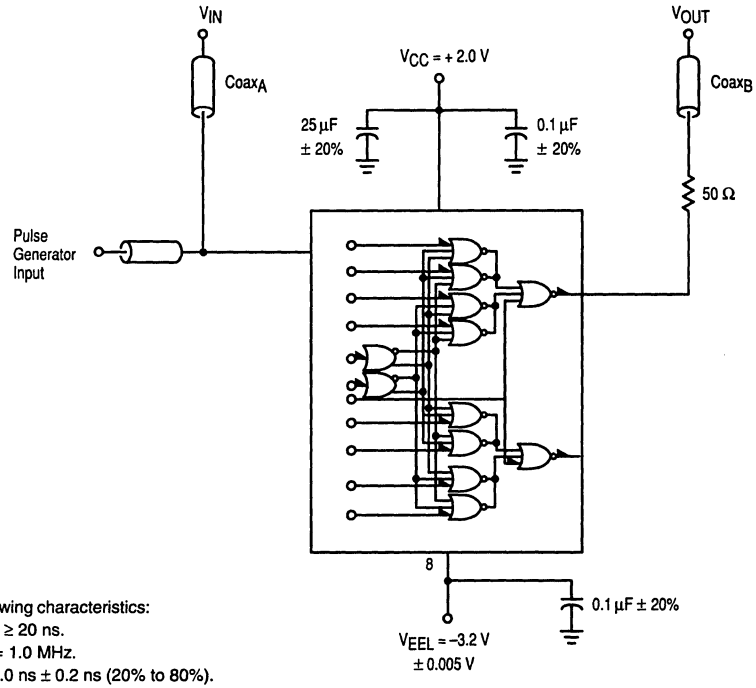
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns (20% to 80%).
2. All input and output cables to the scope are equal length of 50 Ω coaxial cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.

Figure 1. Switching Test Circuit

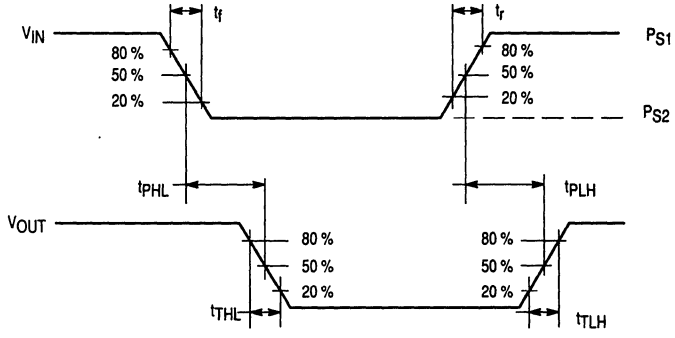


Figure 2. Switching Test Circuit Waveforms

10574
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	3 - 7, 9 - 13	7, 9, 14			8	1, 16	2, 15
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.545	– 1.92	– 1.655	V	3, 7, 9, 14	3 - 7	14	9 - 13	8	1, 16	2, 15
V_{OL1}	Low Output Voltage	– 1.85	– 1.60	– 1.82	– 1.525	– 1.92	– 1.635	V	3 - 7		3 - 7, 9 - 13	7, 9	8, 14	1, 16	2, 15
V_{OH1}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V	7, 9		7, 9, 14	3 - 7, 9 - 13	8	1, 16	2, 15
I_{IH1}	Input Current High		220		375		375	µA	3 - 7, 9 - 13				8	1, 16	3 - 7, 9 - 13
I_{IH2}	Input Current High		330		565		565	µA	14				8	1, 16	14
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 9 - 14			8	1, 16	3 - 7, 9 - 14
I_{EE}	Power Supply Drain Current	– 73		– 80		– 80		mA					8	1, 16	8

10574
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.1	3.3	0.9	3.4	0.9	3.3	ns	3 - 7, 9 - 13	2, 15	1, 16	8	3, 4, 5, 7, 9, 11, 12, 13	2, 15
t_{THL}	Fall Time	1.1	3.3	0.9	3.4	0.9	3.3	ns	3 - 7, 9 - 13	2, 15	1, 16	8	3, 4, 5, 7, 9, 11, 12, 13	2, 15
t_{PLH}/ t_{PHL}	Propagation Delay Address (Pin 7)	2.0	6.2	1.9	6.2	1.8	6.3	ns	3 - 7, 9 - 13	2, 15	1, 16	8	3, 4, 5, 7, 9, 11, 12, 13	2, 15
t_{PHL}/ t_{PLH}	Propagation Delay Enable (Pin 14)	1.0	3.1	0.9	3.1	0.9	3.2	ns	3 - 7, 9 - 13	2, 15	1, 16	8	3, 4, 5, 7, 9, 11, 12, 13	2, 15
t_{PLH}/ t_{PHL}	Propagation Delay	1.5	4.7	1.2	4.7	1.3	4.8	ns	3 - 7, 9 - 13	2, 15	1, 16	8	3, 4, 5, 7, 9, 11, 12, 13	2, 15

Military 10575

Quint Latch

ELECTRICALLY TESTED PER:
MPG 10575

The 10575 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not effect the output information. The reset input is enabled only when the clock is in the high state.

- 560 mW Max/Pkg (No Load)
- t_{pd} = 2.5 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_2	2	6	3	51 Ω to V_{TT}
Q_3	3	7	4	51 Ω to V_{TT}
Q_4	4	8	5	51 Ω to V_{TT}
D_4	5	9	7	GND
$\overline{C_0}$	6	10	8	OPEN
$\overline{C_1}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
D_3	9	13	12	GND
D_0	10	14	13	GND
Reset	11	15	14	OPEN
D_1	12	16	15	GND
D_2	13	1	17	GND
Q_0	14	2	18	51 Ω to V_{TT}
Q_1	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

TRUTH TABLE

D	$\overline{C_0}$	$\overline{C_1}$	Reset	Q_{n+1}
L	L	L	Ø	L
H	L	L	Ø	H
Ø	H	Ø	L	Q_n
Ø	Ø	H	L	Q_n
Ø	H	Ø	H	L
Ø	Ø	H	H	L

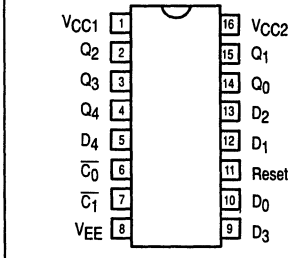
Ø = Don't Care

AVAILABLE AS

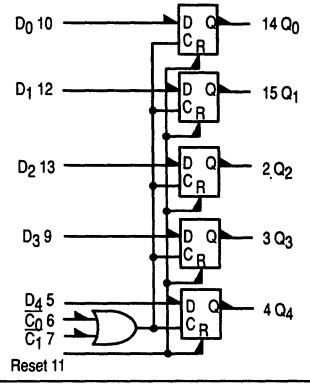
1) JAN: N/A
2) SMD: N/A
3) 883: 10575/BXAJC
X = CASE OUTLINE AS FOLLOWS:

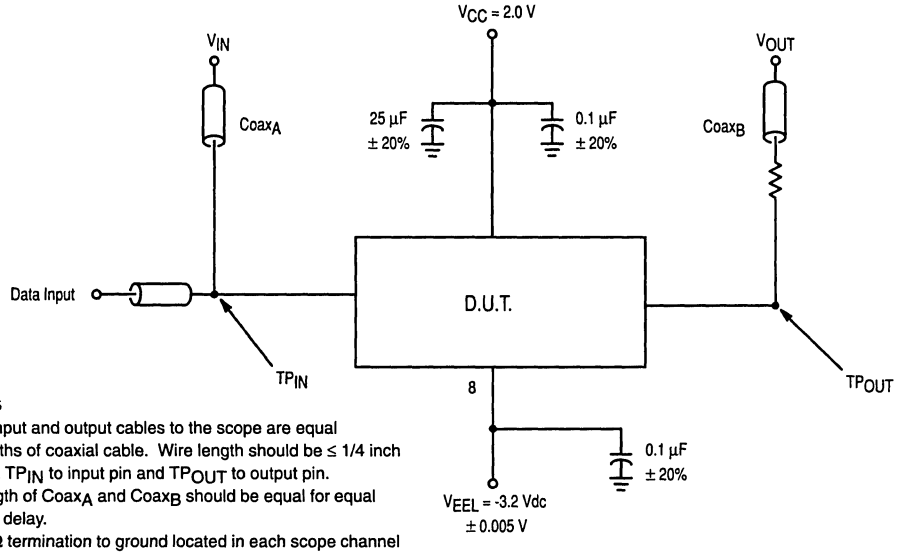
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. All input and output cables to the scope are equal lengths of coaxial cable. Wire length should be ≤ 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 50 Ω termination to ground located in each scope channel input.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)
5. Unused outputs should be loaded 100 Ω to ground.
6. frequency = 1.0 MHz.

Figure 1. Switching Test Circuit

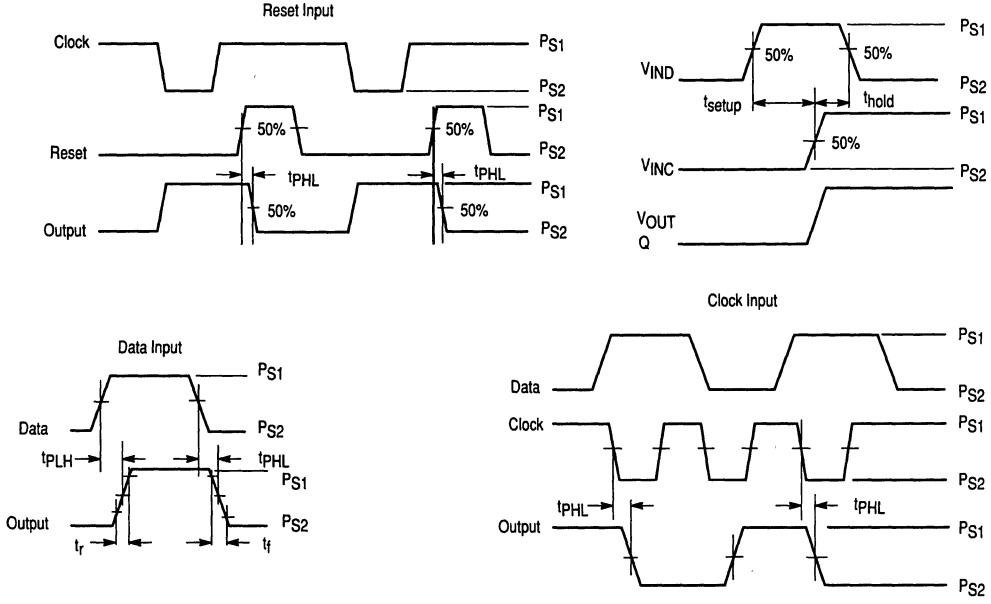


Figure 2. Switching Test Circuit Waveforms

10575
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	5, 9, 10, 12, 13				8	1, 16	2 - 4, 14, 15
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.545	– 1.92	– 1.655	V					8	1, 16	2 - 4, 14, 15
V_{OL1}	Low Output Voltage	– 1.85	– 1.60	– 1.82	– 1.525	– 1.92	– 1.635	V	5, 6, 9, 10, 11, 13	5, 9 - 13	11	5 - 7, 9, 10, 11, 13	8	1, 16	2 - 4, 14, 15
V_{OH1}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.62	– 1.10	– 0.88	V	5, 6, 9, 10, 11, 13	5, 6, 9, 10 - 13	5 - 7, 9, 10, 11, 13	11	8	1, 16	2 - 4, 14, 15
I_{IH1}	Input Current High		290		495		495	µA	5, 9, 10, 12, 13				8	1, 16	5, 9, 10, 12, 13
I_{IH2}	Input Current High		650		1100		1100	µA	11				8	1, 16	11
I_{IH3}	Input Current High		290		495		495	µA	6, 7				8	1, 16	6, 7
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 9 - 13			8	1, 16	5 - 7, 9 - 13
I_{EE}	Power Supply Drain Current	– 97		– 107		– 107		mA					8	1, 16	8

10575
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	3.5	1.0	4.1	1.0	3.8	ns	5, 6, 9 - 13	2 - 4, 14, 15	1, 16	8	2 - 4, 14, 15
t_{THL}	Fall Time	1.1	3.5	1.0	4.1	1.0	3.8	ns	5, 6, 9 - 13	2 - 4, 14, 15	1, 16	8	2 - 4, 14, 15
t_{pd}	Propagation Delay Reset to Q	1.0	3.9	1.0	4.6	1.0	4.2	ns	5, 6, 9 - 13	2 - 4, 14, 15	1, 16	8	2 - 4, 14, 15
t_{pd}	Propagation Delay Data to Q	1.0	3.5	1.0	4.1	1.0	3.8	ns	5, 6, 9 - 13	2 - 4, 14, 15	1, 16	8	2 - 4, 14, 15
t_{pd}	Propagation Delay Clock to Q	1.0	4.3	1.0	5.0	1.0	4.6	ns	5, 6, 9 - 13	2 - 4, 14, 15	1, 16	8	2 - 4, 14, 15
t_{SET}	Setup Time	2.5		2.5		2.5		ns	6, 10, 12, 13	2 - 4, 14, 15	1, 16	8	2 - 4, 14, 15
t_{HOLD}	Hold Time	1.5		1.5		1.5		ns	6, 10, 12, 13	2 - 4, 14, 15	1, 16	8	2 - 4, 14, 15

Hex "D" Master-Slave Flip-Flop

ELECTRICALLY TESTED PER:
JM 38510/06103

The 10576 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.

- 630 mW Max/Pkg (No Load)
- f_{toggle} = 150 MHz (typ)
- t_r, t_f = 2.0 ns typ (20% - 80%)

3

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_0	2	6	3	51 Ω to V_{TT}
Q_1	3	7	4	51 Ω to V_{TT}
Q_2	4	8	5	51 Ω to V_{TT}
D0	5	9	7	GND
D_1	6	10	8	GND
D_2	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Clock	9	13	12	CP1
D_3	10	14	13	GND
D_4	11	15	14	GND
D_5	12	16	15	GND
Q_3	13	1	17	51 Ω to V_{TT}
Q_4	14	2	18	51 Ω to V_{TT}
Q_5	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

TRUTH TABLE

C	D	Q_{n+1}
L	∅	Q_n
* H	L	L
* H	H	H

∅ = Don't Care
* A clock H is a clock transition from a Low to a High state

Military 10576

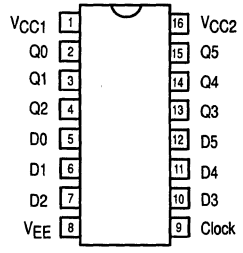
MPO

AVAILABLE AS

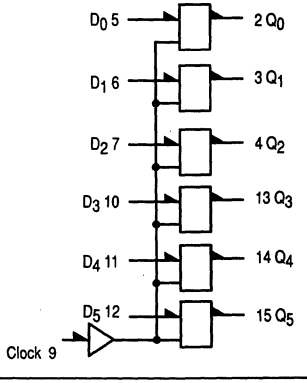
1) JAN: JM 38510/06103
2) SMD: N/A
3) 883: 10576/BXAJC
X = CASE OUTLINE AS FOLLOWS:

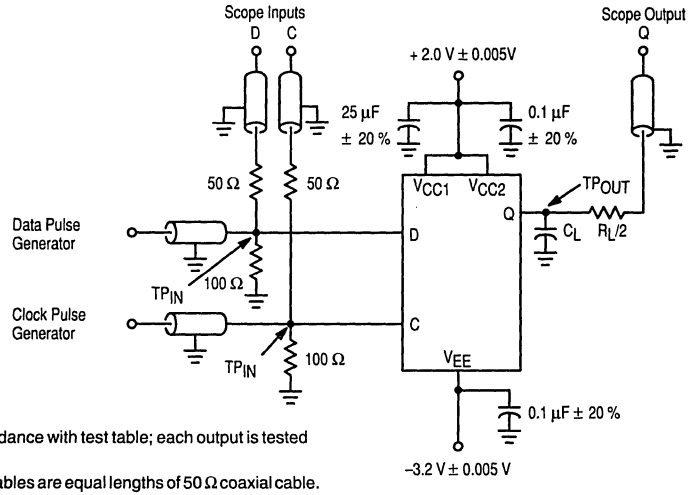
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM

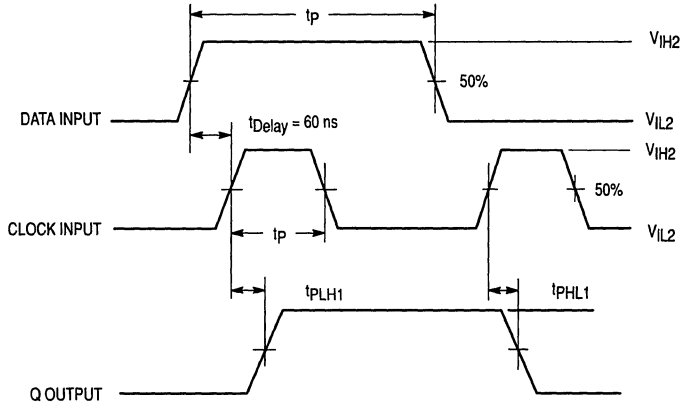




NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.25 inch (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Output not under test connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. Scope input = 50 Ω to ground.
7. C_L (test jig) ≤ 5.0 pF.
8. Z_{OUT} = 50 Ω.

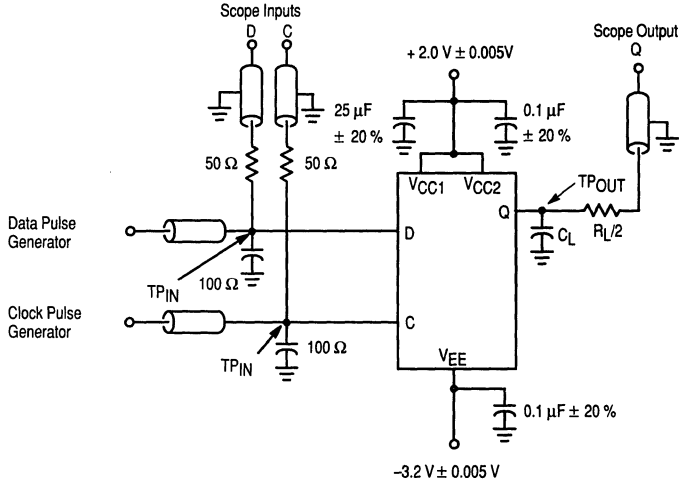
Figure 1. Synchronous Switching Test Circuit



NOTES

1. Note that observed pulse amplitude is attenuated by one half.
2. $t_{P(data)}$ = 150 ns.
3. $t_{P(clock)}$ = 40 ns.
4. PRR = 1.0 MHz.
5. $t_{THL} = t_{TLH}$ = 2.0 ns (20% to 80%).

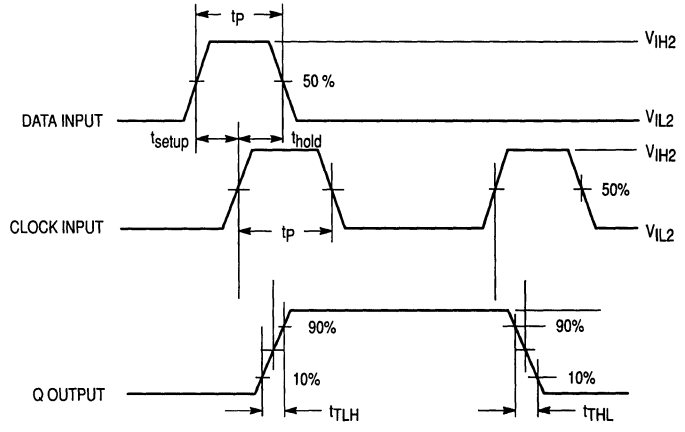
Figure 2. Synchronous Switching Test Circuit Waveforms



NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.25 inch (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to otuput pin.
3. Output not under test connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. Scope input = 50 Ω to ground.
7. C_L (test jig) ≤ 5.0 pF.
8. Z_{OUT} = 50 Ω.

Figure 3. Setup and Hold Test Circuit



NOTES

1. Note that observed pulse amplitude is attenuated by one half.
2. $t_{P(data)}$ = 40 ns.
3. $t_{P(clock)}$ = 40 ns.
4. PRR = 1.0 MHz.
5. $t_{THL} = t_{TLH}$ = 2.0 ns (20% to 80%).

Figure 4. t_{SETUP} and t_{HOLD} Waveforms

10576
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{ITH}	V_{ITL}	V_{IH1}	V_{IL1}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	Clk	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	5 - 7, 10 - 12				9	8	16	2 - 4, 13 - 15
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.545	– 1.92	– 1.655	V		5 - 7, 10 - 12				8	16	2 - 4, 13 - 15
V_{OTL}	Low Output Voltage		– 1.60		– 1.525		– 1.635	V	6, 7, 10 - 12	6, 7, 10 - 12	6, 7, 10 - 12	5 - 7, 10 - 12	9	8	16	2 - 4, 13 - 15
V_{OTH}	High Output Voltage	– 0.95		– 0.845		– 1.10		V	5 - 7, 10 - 12	5 - 7, 10 - 12		5 - 7, 10 - 12	9	8	16	2 - 4, 13 - 15
I_{IH1}	Input Current High		220		375		375	µA	5 - 7, 10 - 12					8	16	5 - 7, 10 - 12
I_{IH2}	Input Current High		310		527		527	µA	9					8	16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 10 - 12				8	16	5 - 7, 10 - 12
I_{EE}	Power Supply Drain Current	– 110		– 121		– 121		mA						8	16	8

10576
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{ITH}	V_{ITL}	V_{IH1}	V_{IL1}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	4.0	1.0	4.5	1.0	4.3	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12
t_{THL}	Fall Time	1.1	4.0	1.0	4.5	1.0	4.3	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12
t_{PLH}	Propagation Delay	1.5	4.5	1.3	5.3	1.2	4.9	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12
t_{PLH}	Propagation Delay	1.5	4.5	1.3	5.3	1.2	4.9	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12
f_{Toggle}	Toggle Frequency	125		125		115		MHz	5 - 7, 10 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12

Military 10578

Binary Counter

ELECTRICALLY TESTED PER:
MPG 10578

The 10578 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function. Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

- 505 mW Max/Pkg (No Load)
- f_{toggle} = 150 MHz (typ)
- t_r , t_f = 2.7 ns typ (20% - 80%)

AVAILABLE AS

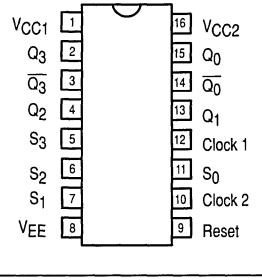
1) JAN: N/A
2) SMD: N/A
3) 883: 10578/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

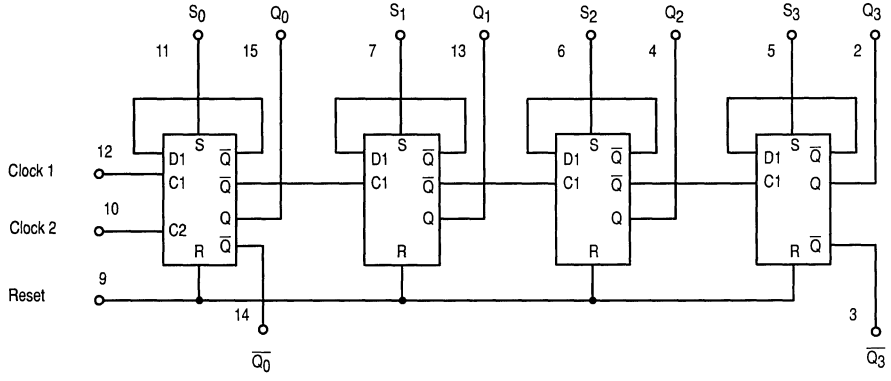
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q3	2	6	3	51 Ω to V_{TT}
$\overline{Q3}$	3	7	4	51 Ω to V_{TT}
Q2	4	8	5	51 Ω to V_{TT}
S3	5	9	7	GND
S2	6	10	8	GND
S1	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Reset	9	13	12	OPEN
Clock 2	10	14	13	OPEN
S0	11	15	14	GND
Clock 1	12	16	15	OPEN
Q1	13	1	17	51 Ω to V_{TT}
$\overline{Q0}$	14	2	18	51 Ω to V_{TT}
Q0	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND



BURN - IN CONDITIONS:
V_{TT} = – 2.2 V MIN/ – 2.0 V MAX
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

LOGIC DIAGRAM

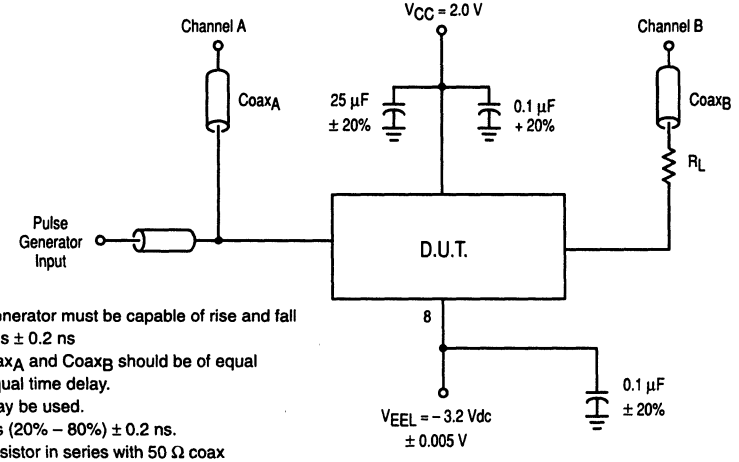


INPUTS							OUTOUTS			
R	S_0	S_1	S_2	S_3	C_1	C_2	Q_0	Q_1	Q_2	Q_3
H	L	L	L	L	φ	φ	L	L	L	L
L	H	H	H	H	φ	φ	H	H	H	H
L	L	L	L	L	H	φ	No Count			
L	L	L	L	L	φ	H	No Count			
L	L	L	L	L	••	••	L	L	L	L
L	L	L	L	L	••	••	H	L	L	L
L	L	L	L	L	••	••	L	H	L	L
L	L	L	L	L	••	••	H	H	L	L
L	L	L	L	L	••	••	L	L	H	L
L	L	L	L	L	••	••	H	L	H	L
L	L	L	L	L	••	••	L	H	H	L
L	L	L	L	L	••	••	H	H	H	L
L	L	L	L	L	••	••	L	L	L	H
L	L	L	L	L	••	••	H	L	L	H
L	L	L	L	L	••	••	L	H	L	H
L	L	L	L	L	••	••	H	H	L	H
L	L	L	L	L	••	••	L	L	H	H
L	L	L	L	L	••	••	H	L	H	H
L	L	L	L	L	••	••	L	H	H	H
L	L	L	L	L	••	••	H	H	H	H

Ø = Don't Care

•• V_{IH} / V_{IL}

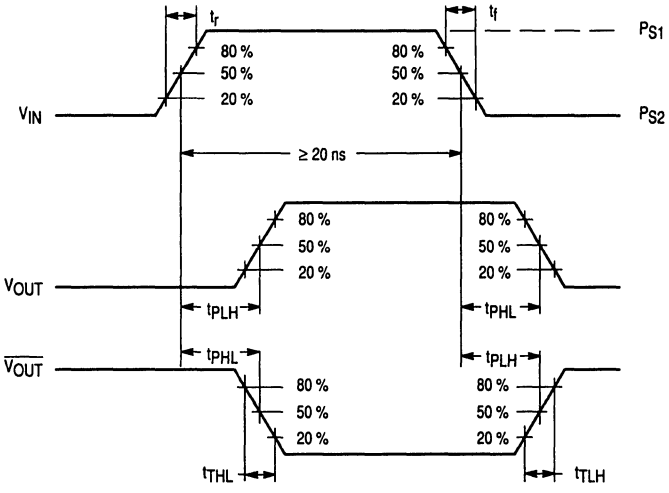
Clock transition from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.



NOTES

1. The Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns
2. Length of Coax$_A$ and Coax$_B$ should be of equal lengths for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 2.0 ns (20% – 80%) ± 0.2 ns.
5. R_L = 50 Ω resistor in series with 50 Ω coax constituting 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground.

Figure 1. Switching Test Circuit



NOTES

1. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

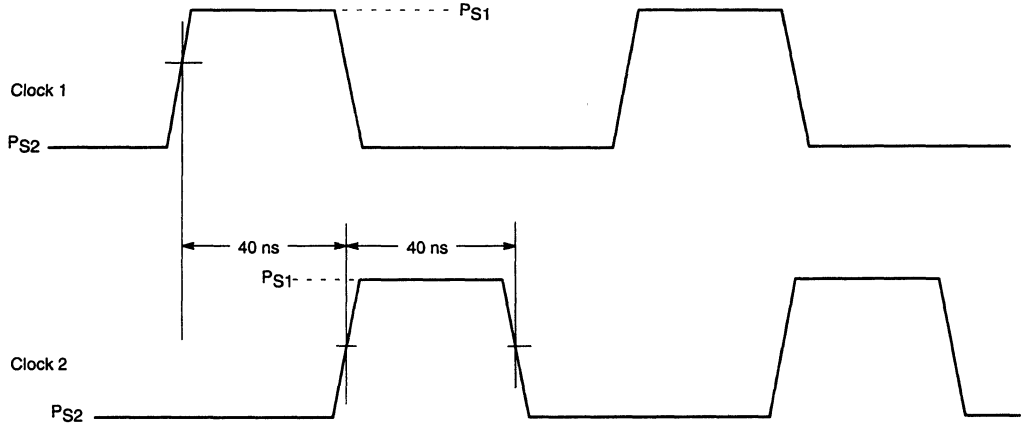


Figure 2. Switching Test Circuit Waveforms

10578
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	$P_{1, 2, 3}$	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	5 - 7, 9, 11			8	1, 16	2, 3, 4, 13, 14
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.545	– 1.92	– 1.655	V	5 - 7, 9, 11			8	1, 16	2, 3, 4, 13, 14
V_{OL1}	Low Output Voltage	– 1.85	– 1.60	– 1.82	– 1.525	– 1.92	– 1.635	V		5 - 7, 9 - 12	5 - 7, 9 - 12	8	1, 16	2, 3, 4, 13 - 15
V_{OH1}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V		5 - 7, 9 - 12		8	1, 16	2, 3, 4, 13 - 15
I_{IH}	Input Current High		245		415		415	µA	10, 12			8	1, 16	10, 12
I_{IH1}	Input Current High		220		375		375	µA	5 - 7, 11			8	1, 16	5 - 7, 11
I_{IH2}	Input Current High		410		700		700	µA	9			8	1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 9 - 12		8	1, 16	5 - 7, 9 - 12
I_{EE}	Power Supply Drain Current	– 88	- 10	– 97	- 10	– 97	- 10	mA				8	1, 16	8

NOTES

P1) V_{IH} / V_{IL} P2) V_{IH1} / V_{IL} P3) V_{IL1} / V_{IL}

10578
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	P_{S1}	P_{S2}	f_{max}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.1	4.5	1.1	5.3	1.1	4.9	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11			1, 16	8	2 - 4, 13 - 15
t_{THL}	Fall Time	1.1	4.5	1.1	5.3	1.1	4.9	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11			1, 16	8	2 - 4, 13 - 15
t_{pd}	Propagation Delay Clock to Q_0, $\overline{Q_0}$	1.5	4.8	1.5	5.6	1.4	5.0	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11			1, 16	8	2 - 4, 13 - 15
t_{pd}	Propagation Delay Clock to Q_1	2.0	9.2	2.0	10.8	1.9	9.9	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11			1, 16	8	2 - 4, 13 - 15
t_{pd}	Propagation Delay Clock to Q_2	3.0	12	3.0	14	2.9	13	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11			1, 16	8	2 - 4, 13 - 15
t_{pd}	Propagation Delay Clock to Q_3, $\overline{Q_3}$	4.0	14.5	4.0	17	3.9	16	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11			1, 16	8	2 - 4, 13 - 15
$t_{set/reset}$	Set/Rest Input	1.5	5.0	1.5	6.1	1.4	5.6	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11			1, 16	8	2 - 4, 13 - 15
f_{Tog}	Toggle Frequency	125		125		125		MHz		14, 15		6, 7, 9, 11	10, 12	1, 16	8	14, 15

MOTOROLA

Look-Ahead Carry Block

ELECTRICALLY TESTED PER:
5962-8774601

The 10579 is a high speed, low power, standard MECL complex function that is designed to perform the look-ahead carry function. This device can be used with the 10581 4-bit ALU directly, or with the 10580 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

When used with the 10581, the 10579 performs a second order or higher look-ahead. Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques. The 10579 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.

3

- 415 mW Max/Pkg (No Load)
- t_{pd} = 3.0 ns typ (Carry, Propagate)
  4.0 ns typ (Generate)
- t_r, t_f = 2.3 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
G_G	2	6	3	51 Ω to V_{TT}
C_{n+4}	3	7	4	51 Ω to V_{TT}
G0	4	8	5	OPEN
G3	5	9	7	GND
C_{n+2}	6	10	8	51 Ω to V_{TT}
G1	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
G2	9	13	12	OPEN
P1	10	14	13	GND
C_n	11	15	14	OPEN
P2	12	16	15	OPEN
P3	13	1	17	GND
P0	14	2	18	OPEN
P_G	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

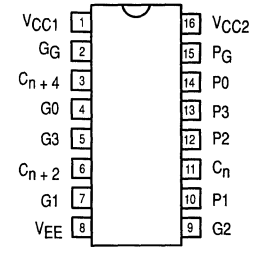
Military 10579

AVAILABLE AS

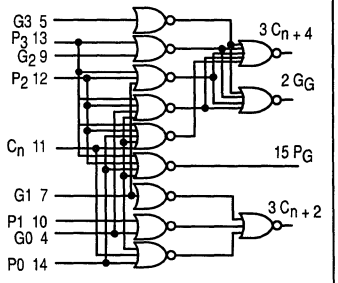
1) JAN: N/A
2) SMD: 5962-8774601
3) 883: 10579/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

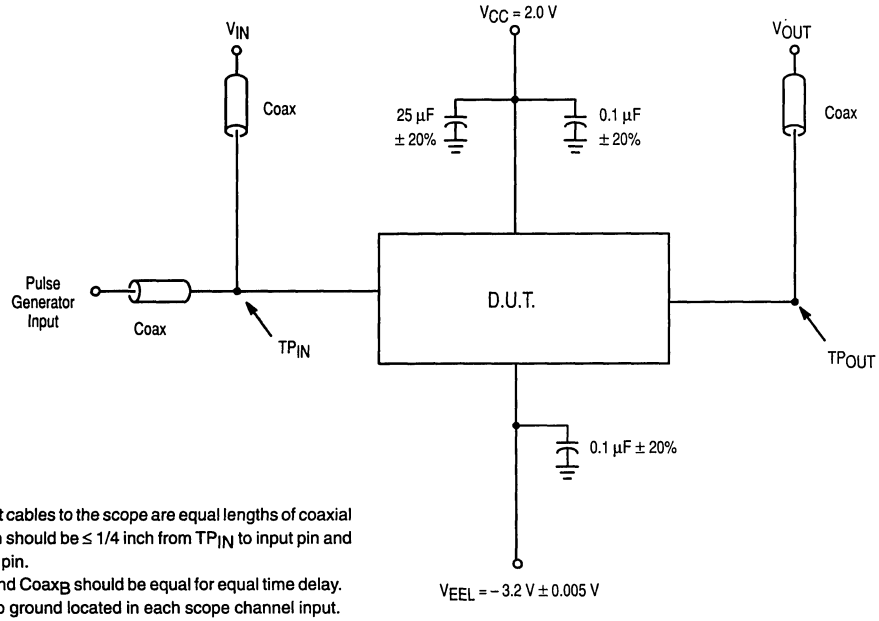
The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



$P_G = P_0 + P_1 + P_2 + P3$
$G_G = (G0 + P1 + P2 + P3)(G1 + P2 + P3)G3$
$C_{n+2} = (C_n + P0 + P1)(G0 + P1)\ G1$
$C_{n+4} = (C_n + P0 + P1 + P2 + P3)(G0 + P1 + P2 + P3)\ (G2 + P3)\ G3$



NOTES

1. All input and output cables to the scope are equal lengths of coaxial cable. Wire length should be ≤ 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 50 Ω termination to ground located in each scope channel input.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)
5. Unused outputs should be loaded 100 Ω to ground.
6. Frequency = 1.0 MHz.

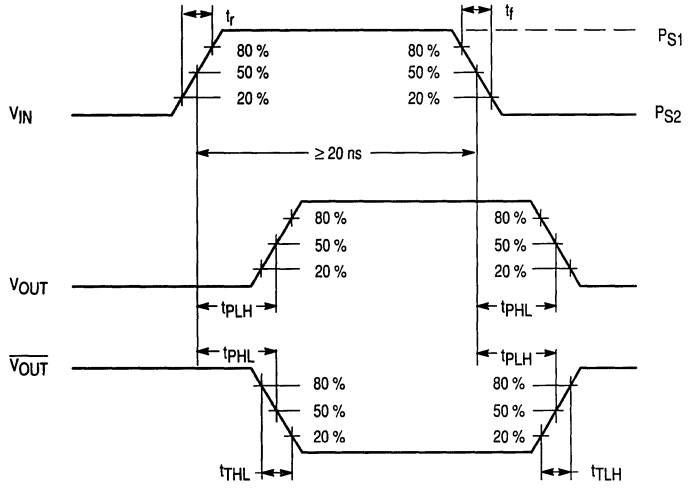


Figure 1. Switching Test Circuit and Waveforms

10579
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.950	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.650	- 1.950	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.09	- 0.88	V	4, 5, 7, 9, 14				8	1, 16	2, 3, 6, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V		4, 5, 7, 9, 14			8	1, 16	2, 3, 6, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	5, 7, 9, 10, 12, 13, 14	5, 7, 9 - 14			8	1, 16	2, 3, 6, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	4, 5, 7, 9, 10, 12 - 14		4, 5, 10 - 13		8	1, 16	2, 3, 6, 15
I_{IH1}	Input Current High		225		380		380	µA	5, 9				8	1, 16	5, 9
I_{IH2}	Input Current High		270		460		460	µA	4, 7, 11				8	1, 16	4, 7, 11
I_{IH3}	Input Current High		355		600		600	µA	14				8	1, 16	14
I_{IH4}	Input Current High		395		670		670	µA	12				8	1, 16	12
I_{IH5}	Input Current High		440		750		750	µA	10, 13				8	1, 16	10, 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4, 7, 9, 14			8	1, 16	4, 7, 9, 14
I_{EE}	Power Supply Current	- 72		- 79		- 79		mA					8	1, 16	8

10579
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.950	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.650	- 1.950	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.1	3.5	1.0	4.1	1.0	3.9	ns	5, 9, 10 11, 13	2, 3, 6, 15	1, 16	8	4, 5, 7, 9, 10, 12, 13	2, 3, 6, 15
t_{THL}	Fall Time	1.1	3.5	1.0	4.1	1.0	3.9	ns	5, 9, 10 11, 13	2, 3, 6, 15	1, 16	8	4, 5, 7, 9, 10, 12, 13	2, 3, 6, 15
t_{pd}	Propagation Delay G or C to Carry Out	1.0	5.5	1.0	6.4	1.0	5.9	ns	5, 9, 10 11, 13	2, 3, 6, 15	1, 16	8	4, 5, 7, 9, 10, 12, 13	2, 3, 6, 15
t_{pd}	Propagation Delay G to G_G	1.0	5.5	1.0	6.4	1.0	5.9	ns	5, 9, 10 11, 13	2, 3, 6, 15	1, 16	8	4, 5, 7, 9, 10, 12, 13	2, 3, 6, 15
t_{pd}	Propagation Delay P to P_G	1.0	3.5	1.0	4.1	1.0	3.9	ns	5, 9, 10 11, 13	2, 3, 6, 15	1, 16	8	4, 5, 7, 9, 10, 12, 13	2, 3, 6, 15
t_{pd}	Propagation Delay P ro G_G	1.0	5.5	1.0	6.4	1.0	5.9	ns	5, 9, 10 11, 13	2, 3, 6, 15	1, 16	8	4, 5, 7, 9, 10, 12, 13	2, 3, 6, 15

MOTOROLA

Dual 2-Bit Adder/Subtractor

ELECTRICALLY TESTED PER:
MPG 10580

The 10580 is a high speed, low power general-purpose adder/subtractor. It is designed to be used in special purpose adders/subtractors or in high speed multiplier arrays. The 10580 can be used in any piece of equipment where these operations are necessary.

Inputs for each adder are Carry-in, operand A, and operand B; outputs are Sum, $\overline{\text{Sum}}$, and Carry-out. The common Select inputs serve as a control line to invert A for subtract, and a control line to invert B.

- 495 mW Max/Pkg (No Load)
- C_{IN} to C_{OUT} = 2.0 ns
- A_0 to S_0 = 4.5 ns
- A_0 to C_{OUT} = 4.5 ns
- t_r, t_f = 2.4 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
$\overline{S_1}$	1	5	2	51 Ω to V_{TT}
$\overline{S_0}$	2	6	3	51 Ω to V_{TT}
C_{OUT}	3	7	4	51 Ω to V_{TT}
C_{IN}	4	8	5	OPEN
A_0	5	9	7	OPEN
B_0	6	10	8	OPEN
Sel_A	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
Sel_B	9	13	12	OPEN
B_1	10	14	13	OPEN
A_1	11	15	14	OPEN
C_{IN}	12	16	15	OPEN
C_{OUT}	13	1	17	51 Ω to V_{TT}
S_1	14	2	18	51 Ω to V_{TT}
S_0	15	3	19	51 Ω to V_{TT}
V_{CC}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Military 10580

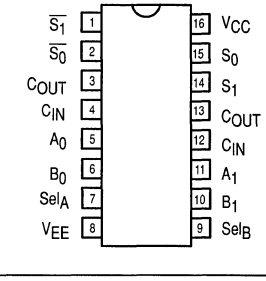
MPO

AVAILABLE AS

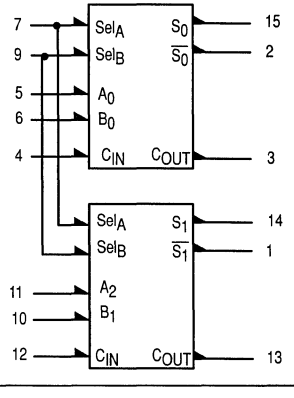
1) JAN: N/A
2) SMD: N/A
3) 883: 10580/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



TRUTH TABLE

Function	Inputs							
	Sel_A	Sel_B	A_0	B_0	C_{IN}	S_O	$\overline{S_O}$	C_{OUT}
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	L	H	L
	H	L	L	H	H	H	L	L
	H	L	H	L	L	L	H	H
	H	L	H	L	H	H	L	H
	H	L	H	H	L	H	L	L
	H	L	H	H	H	L	H	H
REVERSE SUBTRACT	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	L	H	H
	L	H	L	H	H	H	L	H
	L	H	H	L	L	L	H	L
	L	H	H	L	H	H	L	L
	L	H	H	H	L	H	L	L
	L	H	H	H	H	L	H	H
	L	L	L	L	L	L	H	H
	L	L	L	L	H	H	L	H
	L	L	L	H	L	H	L	L
	L	L	L	H	H	L	H	H
	L	L	H	L	L	H	L	L
	L	L	H	L	H	L	H	H
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

FUNCTION SELECT TABLE

Sel_A	Sel_B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

POSITIVE LOGIC ONLY

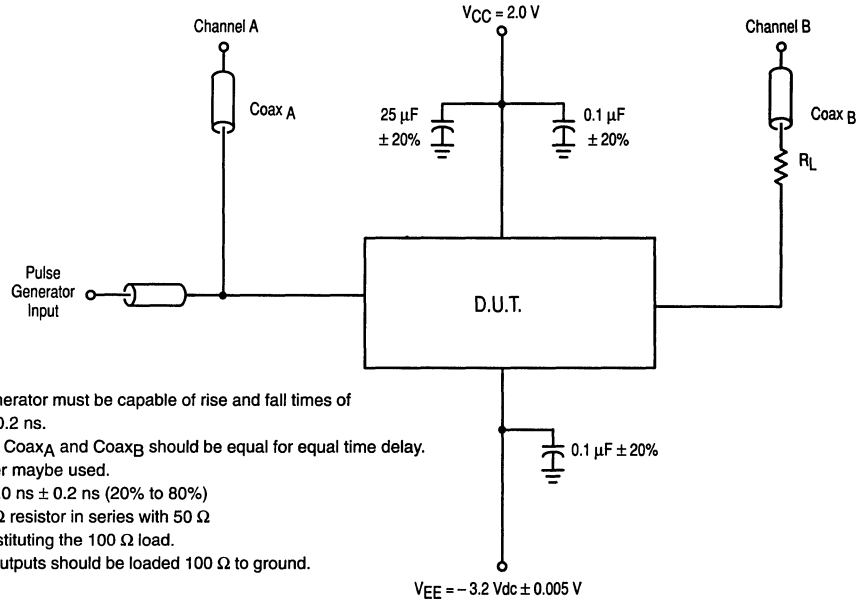
$A' = \overline{A \oplus Sel_A} = A \odot Sel_A$

$B' = \overline{B \oplus Sel_B} = B \odot Sel_B$

$S = \overline{C}_{IN}(\overline{A}'B' + A'\overline{B}') + C_{IN}(A'B' + \overline{A}'\overline{B}')$

$C_{OUT} = C_{IN}A' + C_{IN}B' + A'B'$

3



3

NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 2:1 divider maybe used.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)
5. $R_L = 50\ \Omega$ resistor in series with 50 Ω coax constituting the 100 Ω load.
6. Unused outputs should be loaded 100 Ω to ground.

NOTES

1. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

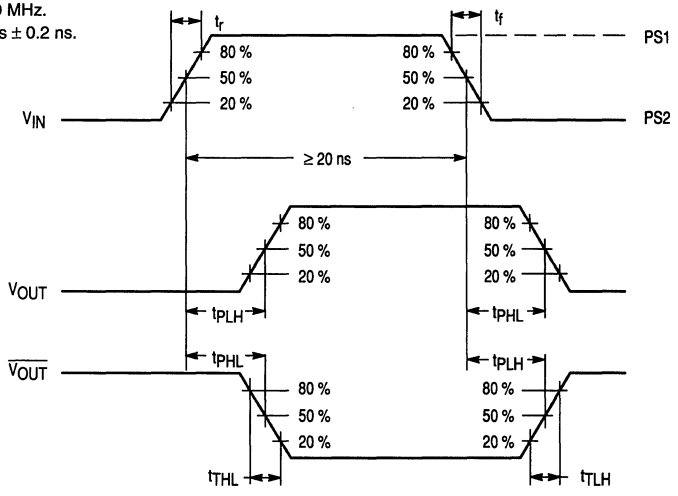


Figure 1. Switching Test Circuit and Waveforms

10580
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	-1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	-1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	-1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25° C		+ 125 ° C		- 55 ° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4, 5, 9, 11, 12				8	16	1 - 3, 13 - 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	5, 11				8	16	1 - 3, 13 - 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	4, 7, 9, 12		4 - 7 9 - 12	4 - 7 9 - 12	8	16	1 - 3, 13 - 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	4, 7, 9, 12		4 - 7 9 - 12	4 - 7 9 - 12	8	16	1 - 3, 13 - 15
I_{IH1}	Input Current High		370		630		630	µA	4, 12				8	16	4, 12
I_{IH2}	Input Current High		290		495		495	µA	7, 9				8	16	7, 9
I_{IH3}	Input Current High		220		375		375	µA	5, 6, 10, 11				8	16	5, 6, 10, 11
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7 9 - 12			8	16	4 - 7 , 9 - 12
I_{EE}	Power Supply Current	- 86		- 95		- 95		mA					8	16	8

10580
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	-1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.66	- 1.82	- 1.000	-1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	-1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.7	1.0	4.3	1.0	4.0	ns	4 - 7, 9 - 12	1 - 3, 13 - 15	16	8	4 - 7, 9 - 12	4 - 7, 9 - 12	2, 3, 15
t_{THL}	Fall Time	1.1	3.7	1.0	4.3	1.0	4.0	ns	4 - 7, 9 - 12	1 - 3, 13 - 15	16	8	4 - 7, 9 - 12	4 - 7, 9 - 12	2, 3, 15
t_{PHL}/t_{PLH}	Propagation Delay Select Input	1.3	5.4	1.0	6.3	1.0	5.8	ns	4 - 7, 9 - 12	1 - 3, 13 - 15	16	8	4 - 7, 9 - 12	4 - 7, 9 - 12	2, 3, 15
t_{PHL}/t_{PLH}	Propagation Delay Carry Input	1.0	3.3	1.0	3.9	1.0	3.6	ns	4 - 7, 9 - 12	1 - 3, 13 - 15	16	8	4 - 7, 9 - 12	4 - 7, 9 - 12	2, 3, 15

MOTOROLA

4-Bit Arithmetic Logic Unit/Function Generator

Military 10581

ELECTRICALLY TESTED PER:
MPG 10581

The 10581 is a high speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two 4-bit words. Full internal carry is incorporated for ripple-through operation. Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 through S3) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look-ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the 10579, full-carry look-ahead, as a second order look ahead block, the 10581 provides high speed arithmetic operations on very long words.

- 600 mW typ/pkg (No load)
- t_{pd} (typ): A1 to F = 6.5 ns
  C_n to C_{n+4} = 3.1 ns
  A1 to P_G = 5.0 ns
  A1 to G_G = 4.5 ns
  A1 to C_{n+4} = 5.0 ns

AVAILABLE AS

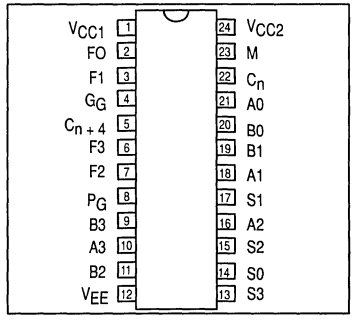
1) JAN: N/A
2) SMD: N/A
3) 883C: 10581/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: K
CERFLAT: J
LCC: 3

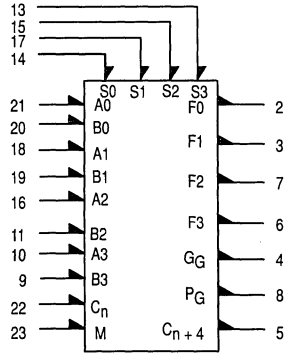
The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	7	2	GND
F0	2	8	3	51 Ω to V_{TT}
F1	3	9	4	51 Ω to V_{TT}
G_G	4	10	5	51 Ω to V_{TT}
C_{n+4}	5	11	6	51 Ω to V_{TT}
F3	6	12	7	51 Ω to V_{TT}
F2	7	13	9	51 Ω to V_{TT}
P_G	8	14	10	51 Ω to V_{TT}
B3	9	15	11	50 Ω to V_{EE}
A3	10	16	12	GND
B2	11	17	13	50 Ω to V_{EE}
V_{EE}	12	18	14	V_{EE}
S3	13	19	16	50 Ω to V_{EE}
S0	14	20	17	GND
S2	15	21	18	50 Ω to V_{EE}
A2	16	22	19	GND
S1	17	23	20	GND
A1	18	24	21	50 Ω to V_{EE}
B1	19	1	23	V_{EE}
B0	20	2	24	50 Ω to V_{EE}
A0	21	3	25	GND
C_n	22	4	26	50 Ω to V_{EE}
M	23	5	27	GND
V_{CC2}	24	6	28	GND



LOGIC DIAGRAM

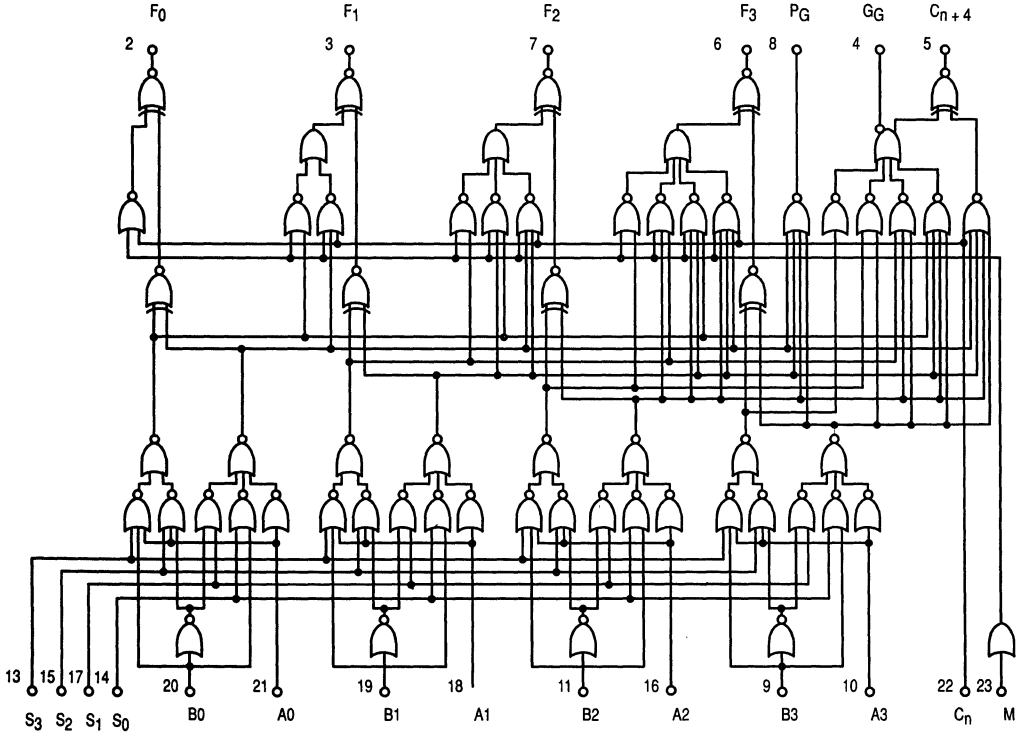


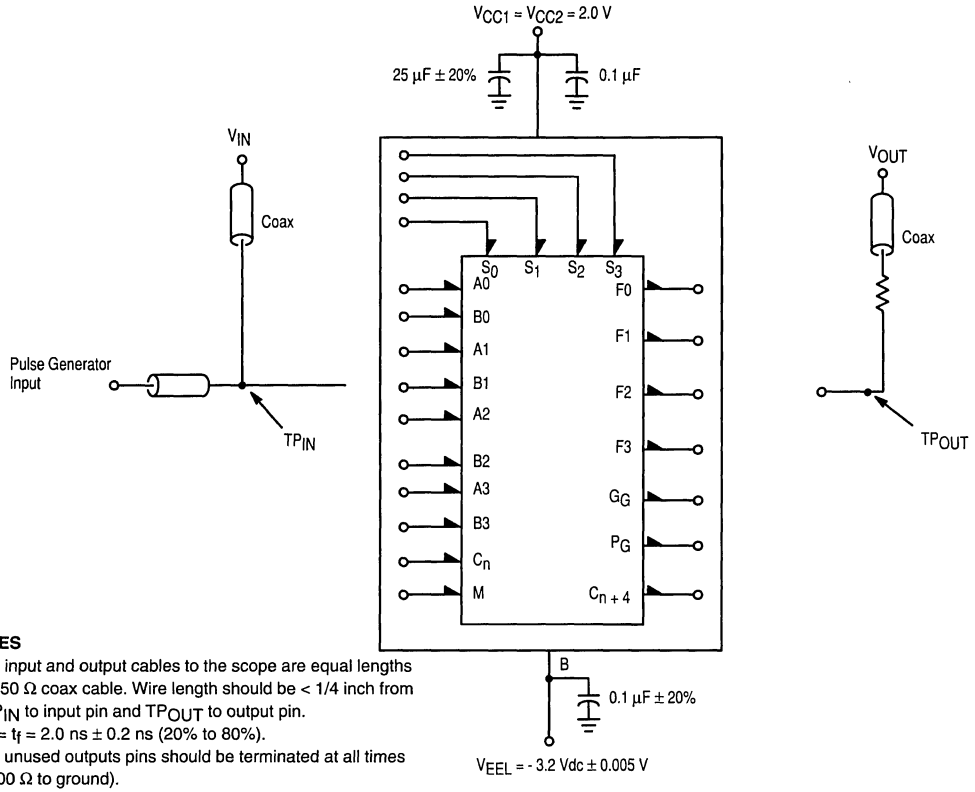
BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

Arithmetic/Logic Functions

Function Select				Logic Function M is High C = D. C.	Arithmetic Operation M is Low C_n is low
S_3	S_2	S_1	S_0	F	F
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A} + \overline{B}$	F = A plus $(A \bullet \overline{B})$
L	L	H	L	$F = \overline{A} + B$	F = A plus (A • B)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A} \bullet B$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus $(A \bullet \overline{B})$
L	H	H	L	$F = A \otimes B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \bullet B$	F = (A + $\overline{B}$) plus 0
H	L	L	H	$F = A \oplus B$	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) plus (A • B)
H	L	H	H	F = A + B	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	$F = A \bullet \overline{B}$	F = (A • $\overline{B}$) minus 1
H	H	H	L	F = A • B	F = (A • B) minus 1
H	H	H	H	F = A	F = minus 1

Logic Diagram





NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coax cable. Wire length should be < 1/4 inch from TP_{IN} to input pin and TP_{OUT} to output pin.
2. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%).
3. All unused outputs pins should be terminated at all times (100 Ω to ground).
4. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.

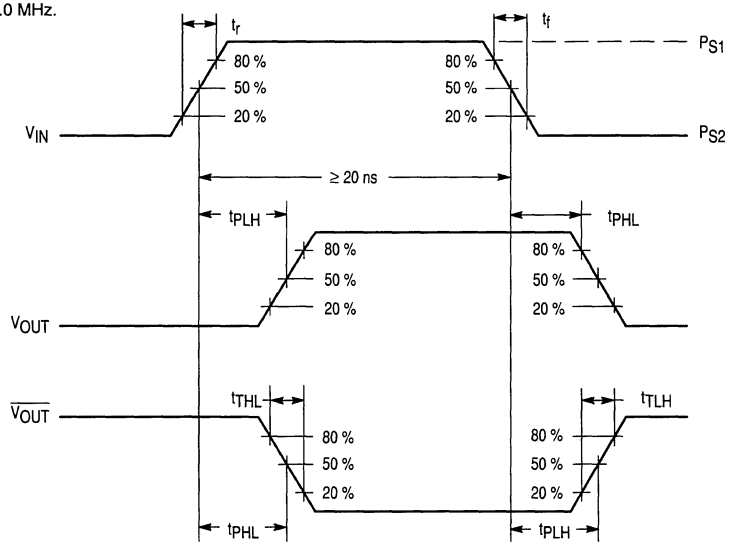


Figure 1. Switching Test Circuit and Waveforms

3

10581
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.850	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.820	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = -55 °C	-0.88	-1.920	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V	9 - 11 16 - 23	13 - 15			12	1, 24	2 - 8
V_{OL1}	Low Output Voltage	– 1.85	– 1.620	– 1.82	– 1.545	– 1.92	– 1.655	V	9 - 11, 14, 16 18, 19, 21 - 23	9, 10, 13, 15 16, 17, 19, 21			12	1, 24	2, 3, 5 - 8
V_{OLA}	Low Output Voltage	– 1.98	– 1.60	– 1.88	– 1.525	– 2.10	– 1.635	V		9 - 11, 13 - 23	14, 15	9 – 11 16 – 23	12	1, 24	2 - 8
V_{OHA}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V	9 - 11, 13 16 - 23	13 - 23	16 - 23	13 - 15 22, 23	12	1, 24	2 - 8
V_{OL2}	Low Output Voltage	– 1.99	– 1.620	– 1.88	– 1.545	– 2.10	– 1.655	V	11, 14, 16, 18 20, 22, 23	9, 10, 13, 15 17, 19, 21			12	1, 24	4
I_{IH1}	Input Current High		200		340		340	µA	13, 23				12	1, 24	13, 23
I_{IH2}	Input Current High		220		375		375	µA	10, 16, 18 21				12	1, 24	10, 16, 18 21
I_{IH3}	Input Current High		245		415		415	µA	9, 11 19, 20				12	1, 24	9, 11, 19, 20
I_{IH4}	Input Current High		265		450		450	µA	14, 15, 17				12	1, 24	14, 15, 17
I_{IH5}	Input Current High		290		495		495	µA	22				12	1, 24	22
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		9 - 11 13 - 23			12	1, 24	9 - 11 , 13 - 23
I_{EE}	Power Supply Current	– 145		– 160		– 160		mA	9 - 11, 16 18 - 21				12	1, 24	12

10581
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.850	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.820	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = -55 °C	-0.88	-1.920	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
		+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
	Functional Parameters:	Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}/ t_{THL}	Rise & Fall Time	1.0	3.0	0.8	3.1	0.9	3.1	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{C_n}$ to $\overline{C_n + 4}$	1.1	5.0	0.9	5.1	1.0	5.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.3	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{C_n}$ to $\overline{F}$	2.0	7.0	2.0	7.1	1.9	7.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{A}$ to $\overline{F}$	3.0	10	2.8	10.2	2.9	10.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	3.5	1.0	3.6	0.9	3.5	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{A}$ to $\overline{P_G}$	2.0	6.5	1.8	6.5	1.8	6.6	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{A}$ to $\overline{G_G}$	2.0	7.0	2.0	7.1	1.9	7.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.0	3.0	0.9	3.1	0.9	3.0	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{A}$ to $\overline{C_n + 4}$	2.0	7.0	1.9	7.5	2.0	7.1	ns	"	"	"	"	"	"

10581
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.850	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.820	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = -55 °C	-0.88	-1.920	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{B}$ to $\overline{F}$	3.0	11	2.7	11.2	2.9	11.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	3.5	0.9	3.5	1.0	3.5	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{B}$ to $\overline{P_G}$	2.0	7.5	1.6	7.6	1.8	7.6	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.0	1.0	5.0	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{B}$ to $\overline{G_G}$	2.0	8.0	2.0	8.1	1.9	8.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.0	3.0	0.9	3.0	0.9	3.0	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{B}$ to $\overline{C_{n+4}}$	2.0	8.0	1.9	8.5	1.9	8.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{M}$ to $\overline{F}$	3.0	10	2.8	10.2	2.3	10.3	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.2	1.0	5.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14, 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{S}$ to $\overline{F}$	3.0	10	2.6	10.2	2.7	10.2	ns	"	"	"	"	"	"

10581
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.850	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.820	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = -55 °C	-0.88	-1.920	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.1	1.0	5.1	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{S}$ to $\overline{P_G}$	2.0	8.0	1.8	8.1	1.9	8.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	1.1	5.0	1.0	5.1	1.0	5.1	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{S}$ to $\overline{C_{n+4}}$	2.0	9.0	1.8	9.1	1.9	9.1	ns	"	"	"	"	"	"
t_{TLH}/ t_{THL}	Rise & Fall Time	0.8	6.0	0.8	6.2	0.8	6.2	ns	9 - 11, 13 - 23	2 - 7	1, 24	12	9 - 11, 13, 14 16, 18, 19, 21 22	2 - 7
t_{pd}	Propagation Delay $\overline{S}$ to $\overline{G_G}$	2.0	9.0	1.7	9.1	1.7	9.2	ns	"	"	"	"	"	"

MOTOROLA

2-Bit Arithmetic Logic Unit/Function Generator

ELECTRICALLY TESTED PER:
MPG 10582

The 10582 is a high speed arithmetic logic unit capable of performing 4 logic operations and 4 arithmetic operations on two 2-bit words. Full internal carry is incorporated for arithmetic operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 and S1) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided for a second order look ahead carry using the 10579. The internal carry is enabled by applying a low level voltage to the mode control input (M).

The 10582 provides an alternate to the 10581 four-bit ALU for applications not requiring the extended functions of the 10581 or for applications requiring a 16-pin package. The 10582 also differs from the 10581 in that Word A and Word B are treated equally for addition and subtraction (A plus B, A minus B, B minus A).

- 795 mW Max/Pkg (No Load)
- t_{pd} (typ): A_1 to F = 7.5 ns
  C_n to C_{n+2} = 2.7 ns
  A_1 to P_G = 6.5 ns
  A_1 to G_G = 5.5 ns
  A_1 to C_{n+2} = 2.7 ns
- t_r, t_f = 2.4 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
C_{n+2}	2	6	3	51 Ω to V_{TT}
G_G	3	7	4	51 Ω to V_{TT}
F0	4	8	5	51 Ω to V_{TT}
A0	5	9	7	OPEN
B0	6	10	8	OPEN
M	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
S1	9	13	12	OPEN
S0	10	14	13	OPEN
B1	11	15	14	GND
A1	12	16	15	GND
C_n	13	1	17	OPEN
F1	14	2	18	51 Ω to V_{TT}
F_G	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

3

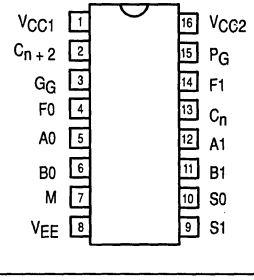
Military 10582

AVAILABLE AS

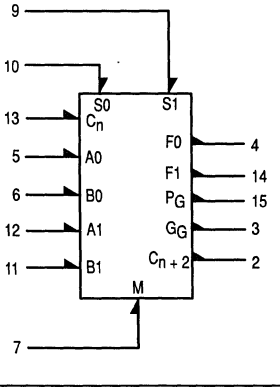
1) JAN: N/A
2) SMD: N/A
3) 883: 10582/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

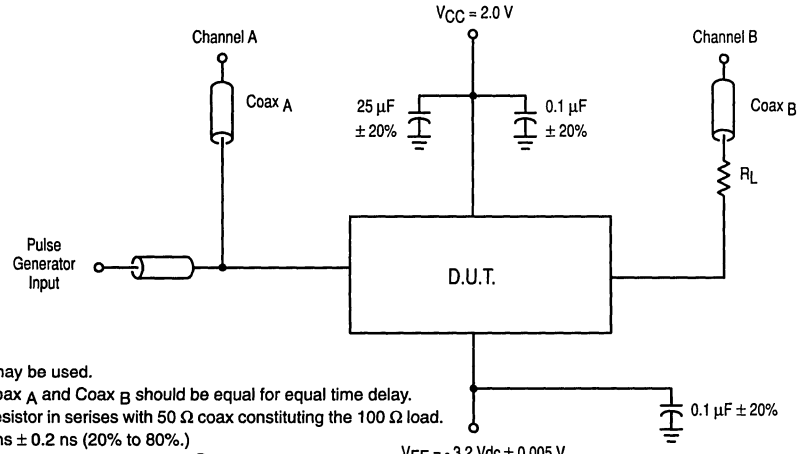


LOGIC DIAGRAM



ARITHMETIC/LOGIC FUNCTIONS

Function Select		POSITIVE LOGIC	
		Logic Function	Arithmetic Operation
		M is High	M is Low
S1	S0	F	F
L	L	F = A ⊗ B	F = A plus B plus Carry
L	H	F = A ⊕ B	F = $\overline{A}$ plus B plus Carry
H	L	F = A • B	F = A plus $\overline{B}$ plus Carry
H	H	F = A + B	F = A times 2



NOTES

1. 2:1 divider may be used.
2. Length of Coax A and Coax B should be equal for equal time delay.
3. R_L = 50 Ω resistor in serises with 50 Ω coax constituting the 100 Ω load.
4. $t_r = t_f$ = 2.0 ns ± 0.2 ns (20% to 80%.)
5. Unused outputs should be loaded 100 Ω to ground.
6. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
7. V_{IN} waveform has the following characteristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz

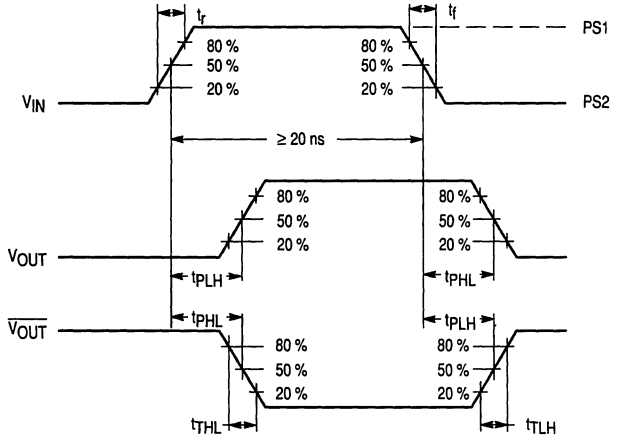


Figure 1. Switching Test Circuit and Waveform

10582
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	-1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	-1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	-1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25° C		+ 125 ° C		- 55 ° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	5, 6, 11 - 13			8	1, 16	2 - 4, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	7, 9, 10			8	1, 16	2 - 4, 14, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	5 - 7, 9 - 13	5 - 7, 9 - 13		8	1, 16	2 - 4, 14, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	5 - 7, 9 - 13		5 - 7, 9 - 13	8	1, 16	2 - 4, 14, 15
I_{IH1}	Input Current High		220		375		375	µA	7, 9, 10			8	1, 16	7, 9, 10
I_{IH2}	Input Current High		390		660		660	µA	5, 12			8	1, 16	5, 12
I_{IH3}	Input Current High		290		495		495	µA	6, 11			8	1, 16	6, 11
I_{IH4}	Input Current High		350		595		595	µA	13			8	1, 16	13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 9 - 13		8	1, 16	5 - 7, 9 - 13
I_{EE}	Power Supply Current	- 138		- 152		- 152		mA				8	1, 16	8

10582
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	-1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.66	- 1.82	- 1.000	-1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	-1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.5	4.5	1.6	5.3	1.5	4.9	ns	5 - 7, 9 - 13	2 - 4, 14, 15	1, 16	8	5 - 7, 9 - 13	2 - 4, 14, 15
t_{THL}	Fall Time	1.5	4.5	1.6	5.3	1.5	4.9	ns	5 - 7, 9 - 13	2 - 4, 14, 15	1, 16	8	5 - 7, 9 - 13	2 - 4, 14, 15
t_{pd}	Propagation Delay C_n to C_{n+2} or F	1.5	5.6	1.6	6.6	1.5	6.1	ns	5 - 7, 9 - 13	2 - 4, 14, 15	1, 16	8	5 - 7, 9 - 13	2 - 4, 14, 15
t_{pd}	Propagation Delay A0 or B0 to F	2.3	10.0	2.4	11.7	2.3	10.8	ns	5 - 7, 9 - 13	2 - 4, 14, 15	1, 16	8	5 - 7, 9 - 13	2 - 4, 14, 15
t_{pd}	Propagation Delay A1 or B1 to F_1	2.3	10.0	2.4	11.7	2.3	10.8	ns	5 - 7, 9 - 13	2 - 4, 14, 15	1, 16	8	5 - 7, 9 - 13	2 - 4, 14, 15
t_{pd}	Propagation Delay A0, B0, A1 to C_{n+2}	2.3	10.0	2.4	11.7	2.3	10.8	ns	5 - 7, 9 - 13	2 - 4, 14, 15	1, 16	8	5 - 7, 9 - 13	2 - 4, 14, 15
t_{pd}	Propagation Delay B1 to C_{n+2}	2.8	12.0	2.9	14.0	2.8	13.0	ns	5 - 7, 9 - 13	2 - 4, 14, 15	1, 16	8	5 - 7, 9 - 13	2 - 4, 14, 15
t_{pd}	Propagation Delay A or B to P_G or G_G	2.3	10.0	2.4	11.7	2.3	10.8	ns	5 - 7, 9 - 13	2 - 4, 14, 15	1, 16	8	5 - 7, 9 - 13	2 - 4, 14, 15
t_{pd}	Propagation Delay M or S to F	2.3	10.0	2.4	11.7	2.3	10.8	ns	5 - 7, 9 - 13	2 - 4, 14, 15	1, 16	8	5 - 7, 9 - 13	2 - 4, 14, 15

MOTOROLA

Hex "D" Master-Slave Flip-Flop with Reset

ELECTRICALLY TESTED PER:
5962-8779301

The 10586 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device. A common Reset is included in this circuit. Reset only functions when clock is low.

- 630 mW Max/Pkg (No Load)
- f_{Tog} = 150 MHz typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
Reset	1	5	2	OPEN
Q_0	2	6	3	51 Ω to V_{TT}
Q_1	3	7	4	51 Ω to V_{TT}
Q_2	4	8	5	51 Ω to V_{TT}
D0	5	9	7	GND
D_1	6	10	8	GND
D_2	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Clock	9	13	12	CP1
D_3	10	14	13	GND
D_4	11	15	14	GND
D_5	12	16	15	GND
Q_3	13	1	17	51 Ω to V_{TT}
Q_4	14	2	18	51 Ω to V_{TT}
Q_5	15	3	19	51 Ω to V_{TT}
V_{CC}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = - 2.0 V MAX/ - 2.2 V MIN
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

TRUTH TABLE

R	C	D	Q_{n+1}
L	L	∅	Q_n
L	H	L	L
L	H	H	H
H	L	∅	L

∅ = Don't Care
* A clock H is a clock transition from a Low to a High state

Military 10586

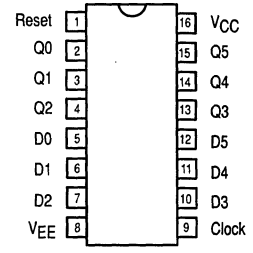
MPO

AVAILABLE AS

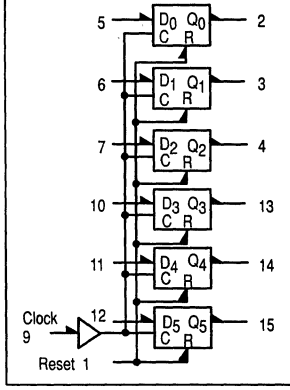
1) JAN: N/A
2) SMD: 5962-8779301
3) 883: 10586/BXAJC
X = CASE OUTLINE AS FOLLOWS:

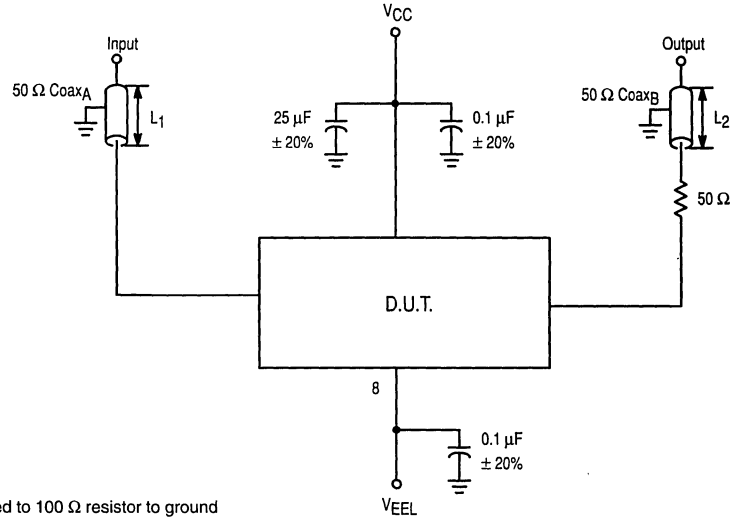
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



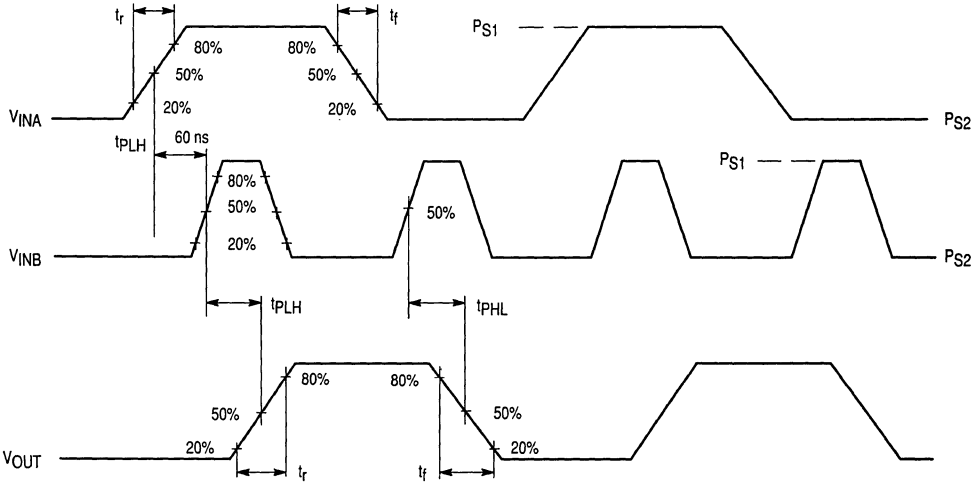
LOGIC DIAGRAM





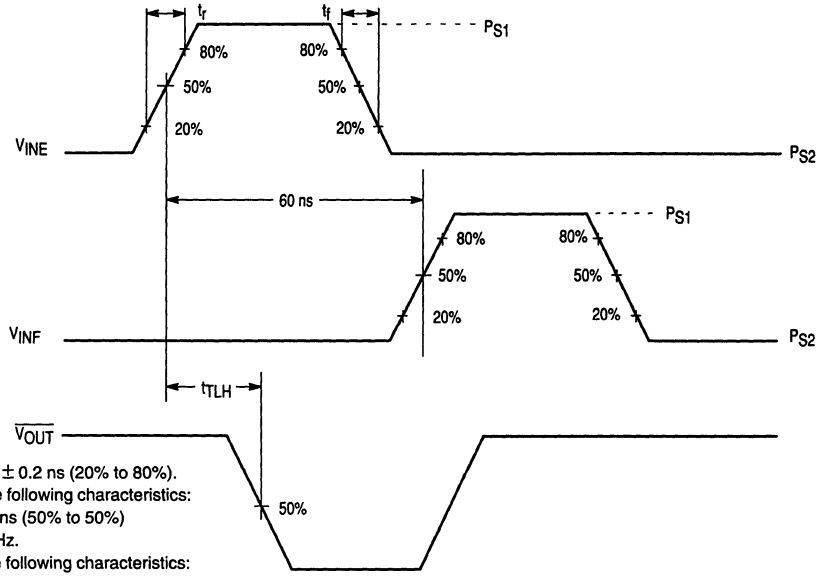
NOTES
1. Unused outputs connected to 100 Ω resistor to ground
2. 2:1 divider may be used
3. L1 = L2: matched for equal time delay

Figure 1. Switching Test Circuit



NOTES
1. $t_r = t_f$ 2.0 ns ± 0.2 ns (20% to 80%).
2. V_{INA} has the following characteristics:
   a) PW = 500 ns (50% to 50%)
   b) f = 1.0 MHz.
3. V_{INB} has the following characteristics:
   a) PW ≥ 40 ns (50% to 50%)
   b) f = 1.0 MHz.

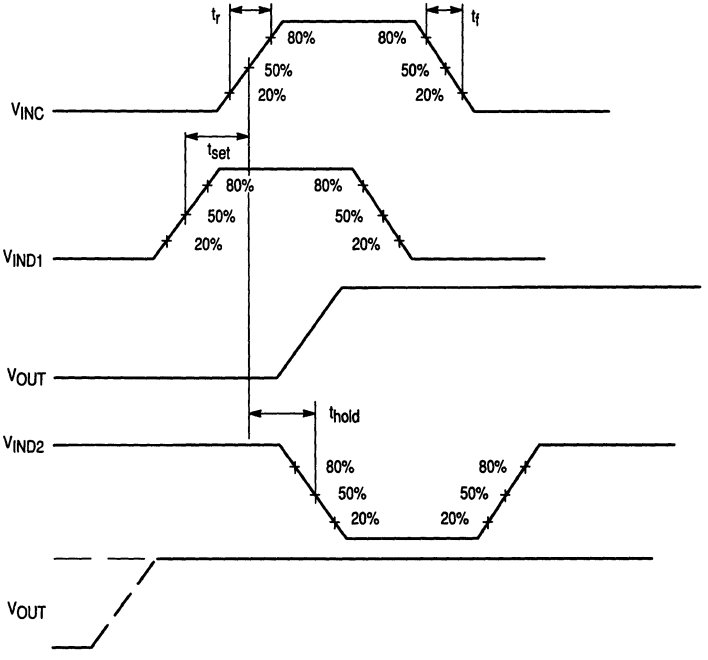
Figure 2. Switching Test Circuit Waveform



NOTES

1. $t_r = t_f$ 2.0 ns ± 0.2 ns (20% to 80%).
2. V_{INE} has the following characteristics:
   a) PW ≥ 40 ns (50% to 50%)
   b) f = 1.0 MHz.
3. V_{INF} has the following characteristics:
   a) PW ≥ 40 ns (50% to 50%)
   b) f = 1.0 MHz.

Figure 3. Switching Test Circuit Waveforms



NOTES

1. $t_r = t_f$ 2.0 ns ± 0.2 ns (20% to 80%).
2. V_{INC} has the following characteristics:
   a) PW ≥ 40 ns (50% to 50%)
   b) f = 1.0 MHz.
3. V_{IND} has the following characteristics:
   a) PW ≥ 40 ns (50% to 50%)
   b) f = 1.0 MHz.

Figure 4. t_{SET} and t_{HOLD} Waveforms

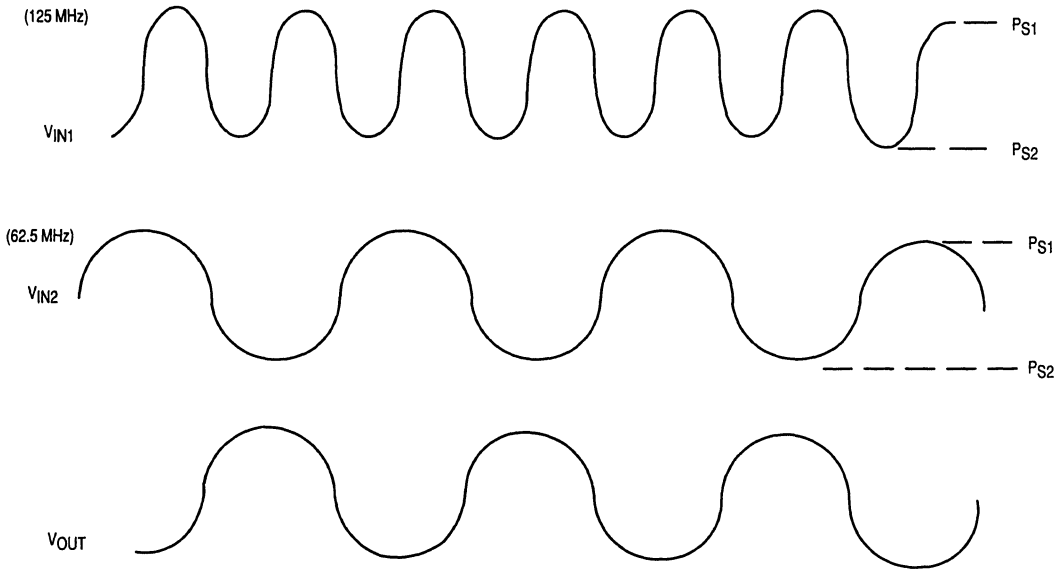


Figure 4. f_{Toggle} Waveforms

10586
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		− 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to − 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	− 0.93	− 0.78	− 0.825	− 0.63	− 1.08	− 0.88	V	5 - 7, 9 - 12	5 - 7, 9 - 12			8	16	2 - 4, 13 - 15
V_{OL}	Low Output Voltage	− 1.85	− 1.62	− 1.82	− 1.545	− 1.92	− 1.655	V	5 - 7, 9 - 12	5 - 7, 9 - 12			8	16	2 - 4, 13 - 15
V_{OH1}	High Output Voltage	− 0.95	− 0.78	− 0.845	− 0.63	− 1.10	− 0.88	V	5 - 7, 9 - 12	1, 5 - 7, 10 - 12	5 - 7, 10 - 12	1	8	16	2 - 4, 13 - 15
V_{OL1}	Low Output Voltage	− 1.85	− 1.60	− 1.82	− 1.525	− 1.92	− 1.635	V	5 - 7, 10 - 12	1, 5 - 7, 9 - 12	1	5 - 7, 10 - 12	8	16	2 - 4, 13 - 15
I_{EE}	Power Supply Drain Current	− 110		− 121		− 121		mA					8	16	8
I_{IH1}	Input Current High		220		375		375	µA	5 - 7, 10 - 12				8	16	5 - 7, 10 - 12
I_{IH2}	Input Current High		310		525		525	µA	9				8	16	9
I_{IH3}	Input Current High		575		975		975	µA	1				8	16	1
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		1, 5 - 7, 9 - 12			8	16	1, 5 - 7, 9 - 12

10586
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.1	4.0	1.0	4.7	1.0	4.3	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	16	8		2 - 4, 13 - 15
t_{THL}	Fall Time	1.1	4.0	1.0	4.7	1.0	4.3	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	16	8		2 - 4, 13 - 15
t_{PLH}	Propagation Delay Clk or Reset to Out	1.6	4.5	1.6	5.3	1.6	4.9	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12	2 - 4, 13 - 15
t_{PLH}	Propagation Delay Clk or Reset to Out	1.6	4.5	1.6	5.3	1.6	4.9	ns	5 - 7, 9 - 12	2 - 4, 13 - 15	16	8	5 - 7, 10 - 12	2 - 4, 13 - 15
t_{SET}	Setup Time	2.5		2.5		2.5		ns	5 - 7, 9 - 12	2 - 4, 13 - 15	16	8		2 - 4, 13 - 15
t_{HOLD}	Hold Time	1.5		1.5		1.5		ns	5 - 7, 9 - 12	2 - 4, 13 - 15	16	8		2 - 4, 13 - 15
f_{Toggle}	Toggle Frequency	125		125		125		MHz	5 - 7, 9 - 12	2 - 4, 13 - 15	16	8		2 - 4, 13 - 15

MOTOROLA

Quad MST to MECL 10K Translator

ELECTRICALLY TESTED PER:
MPG 10590

The 10590 is a quad translator for interfacing from IBM MST-type logic signals to standard MECL 10K logic levels. This circuit features differential inputs for high noise environments or may be used with single ended lines by tieing one of the inputs to ground.

Since the 10590 is designed to accept signals centered around ground, it is a useful interface element for many communication systems. When pin 9 is connected to V_{CC} the circuit becomes a line receiver for MECL signals. The outputs go to a low level whenever the inputs are left floating.

- 300 mW Max/Pkg (No Load)
- t_{pd} = 2.5 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

3

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω V_{TT}
B_{OUT}	3	7	4	51 Ω V_{TT}
$\overline{A_{IN}}$	4	8	5	51 Ω V_{TT}
A_{IN}	5	9	7	GND
B_{IN}	6	10	8	GND
$\overline{B_{in}}$	7	11	9	51 Ω to V_{TT}
V_{EE}	8	12	10	V_{EE}
V_{SS} or V_{CC}	9	13	12	GND
$\overline{C_{IN}}$	10	14	13	51 Ω to V_{TT}
C_{IN}	11	15	14	GND
D_{IN}	12	16	16	GND
$\overline{D_{IN}}$	13	1	17	51 Ω to V_{TT}
C_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

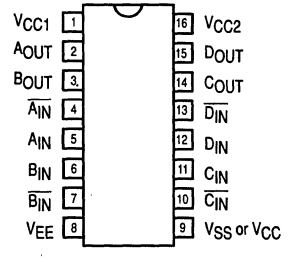
Military 10590

AVAILABLE AS

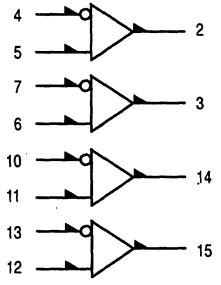
1) JAN: N/A
2) SMD: N/A
3) 883: 10590/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

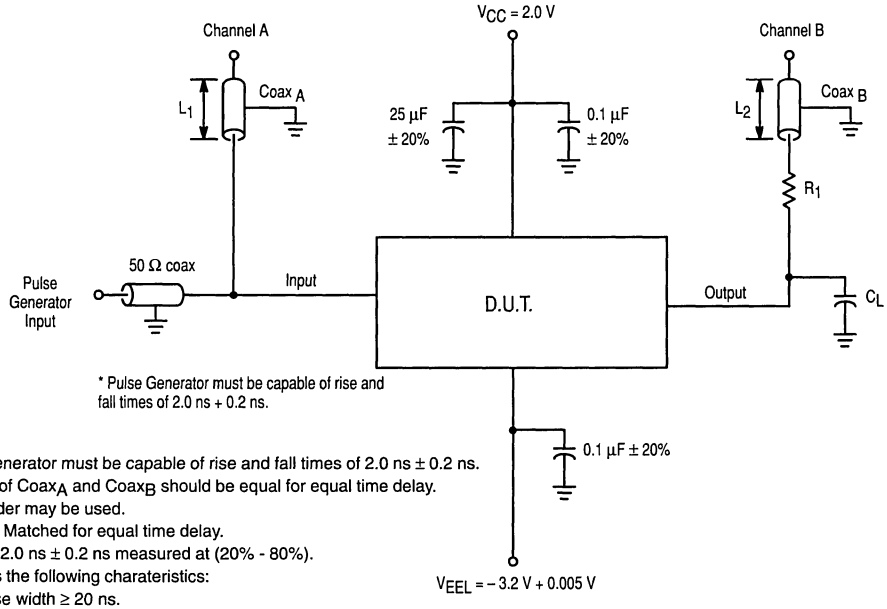
The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8
V_{SS} = Pin 9 Translator
V_{CC} = Pin 9 Receiver



NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 2:1 divider may be used.
5. $L_1 = L_2$ Matched for equal time delay.
5. $t_r = t_f$ = 2.0 ns ± 0.2 ns measured at (20% - 80%).
6. VIN has the following charateristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
7. All other outputs loaded 100 Ω to ground.

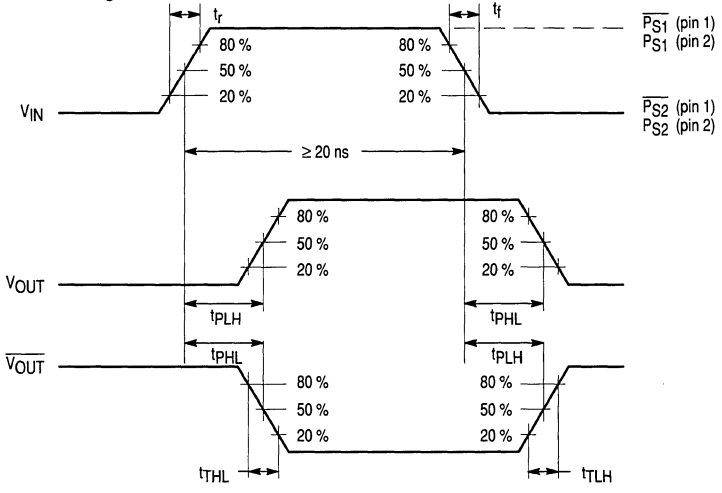


Figure 1. Switching Test Circuit and Waveforms

10590
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)												
	V_{IH}	V_{IL}	V_{IH2}	V_{IL2}	V_{SS}	V_{IHM}	V_{ILM}	V_{IHH}	V_{ILH}	V_{ILL}	V_{IHL}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.780	- 1.850	- 1.105	- 1.475	+1.25	+0.44	-0.49	+0.186	-0.85	-2.53	-1.486	- 5.2	- 3.2
T_A = 125 °C	- 0.630	- 1.820	- 1.000	- 1.400	+1.25	+0.62	-0.43	+0.186	-0.85	-2.53	-1.486	- 5.2	- 3.2
T_A = - 55 °C	- 0.880	- 1.920	- 1.255	- 1.510	+1.25	+0.344	-0.538	+0.186	-0.85	-2.53	-1.486	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	$V_{IHH}/V_{IHL}/V_{IHM}$	$V_{ILH}/V_{ILL}V_{ILM}$	V_{EE}	V_{CC}	V_{SS}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	5, 6, 11, 12	4, 7, 10, 13	5, 6, 11, 12	4, 7, 10, 13	8	1, 9, 16	9	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4, 7, 10, 13	5, 6, 11, 12	4, 7, 10, 13	5, 6, 11, 12	8	1, 9, 16	9	2, 3, 14, 15

									V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{SS}	V_{EE}	GND	P. U. T.
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	-1.635	V			4, 7, 10, 13	5, 6, 11, 12		8	1, 9, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	-0.88	V			5, 6, 11, 12	4, 7, 10, 13		8	1, 9, 16	2, 3, 14, 15
I_{IH1}	Input Current High		45		80		80	µA	4 - 7 10 - 13	4 - 7 10 - 13			9	8	1, 16	4 - 7 10 - 13
I_{CBO}	Reverse Leakage Current	- 1.0		- 1.0		- 1.5		µA					9	4 - 8 10 - 13	1, 16	4 - 7 10 - 13
I_{EE}	Power Supply Current	- 52		- 57		- 57		mA	4, 6 10, 12	5, 7 11, 13			9		1, 16	8
I_{CC}	Power Supply Drain Current		27		27		27	mA	4, 6 10, 12	5, 7 11, 13			9		1, 16	9

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

10590
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{SS1}	V_{RB}	$\overline{P_{S1}}$	$\overline{P_{S2}}$	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	+ 3.25	+ 0.71	+ 2.40	+ 1.60	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	+ 3.25	+ 0.71	+ 2.64	+ 1.85	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = -55 °C	+ 3.25	+ 0.71	+ 2.30	+ 1.44	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN1}	V_{IN2}	V_{OUT}	V_{CC}	V_{EEL}	V_{SS1}	P. U. T.
t_{TLH}	Rise Time	1.5	4.3	1.1	5.0	1.1	4.6	ns	5 - 7, 10 - 13	4 - 7, 10 - 13	2, 3, 14, 15	1, 4 - 7, 9 - 13	8	7, 9	2, 3, 14, 15
t_{THL}	Fall Time	1.5	4.3	1.1	5.0	1.1	4.6	ns	5 - 7, 10 - 13	4 - 7, 10 - 13	2, 3, 14, 15	1, 4 - 7, 9 - 13	8	7, 9	2, 3, 14, 15
t_{PHL}	Propagation Delay Input to Output	1.0	3.7	1.0	4.3	1.0	4.0	ns	5 - 7, 10 - 13	4 - 7, 10 - 13	2, 3, 14, 15	1, 4 - 7, 9 - 13	8	7, 9	2, 3, 14, 15
t_{PLH}	Propagation Delay Input to Output	1.0	3.7	1.0	4.3	1.0	4.0	ns	5 - 7, 10 - 13	4 - 7, 10 - 13	2, 3, 14, 15	1, 4 - 7, 9 - 13	8	7, 9	2, 3, 14, 15

Hex MECL 10K to MST Translator

Military 10591

ELECTRICALLY TESTED PER:
MPG 10591

The 10591 is a hex MECL to IBM MST type logic translator. A common enable (active low) is provided for gating. Open emitter outputs are provided for gating. Open emitter outputs are provided to permit direct transmission line driving.

The 10591 is useful for interfacing to both MST-II and MST-IV systems.

- 300 mW Max/Pkg (No Load)
- t_{pd} = 2.5 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 10591/BXAJC
X = CASE OUTLINE AS FOLLOWS:

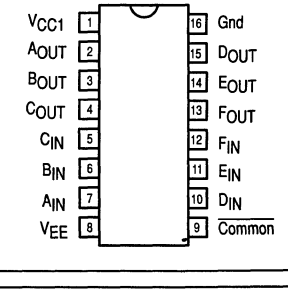
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

3

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	V_{CC}
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
C_{OUT}	4	8	5	51 Ω to V_{TT}
C_{IN}	5	9	7	OPEN
B_{IN}	6	10	8	OPEN
A_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	VEE
$\overline{\text{Common}}$	9	13	12	OPEN
D_{IN}	10	14	13	OPEN
E_{IN}	11	15	14	OPEN
F_{IN}	12	16	15	OPEN
F_{OUT}	13	1	17	51 Ω to V_{TT}
E_{OUT}	14	2	18	51 Ω to V_{TT}
D_{OUT}	15	3	19	51 Ω to V_{TT}
GND	16	4	20	GND

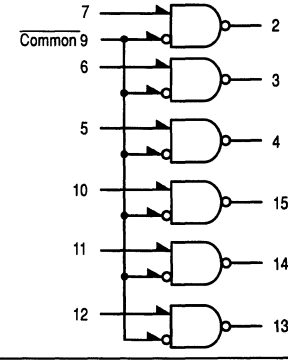


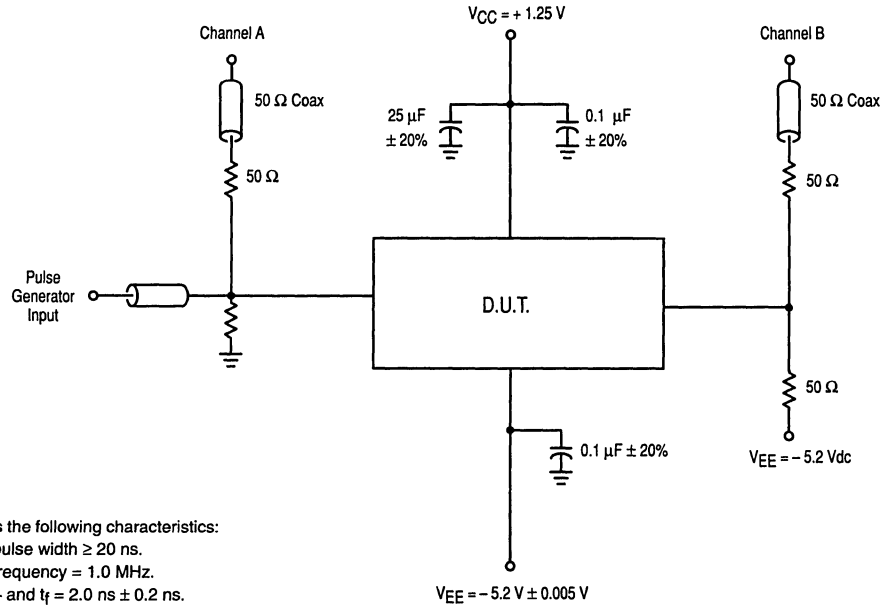
BURN - IN CONDITIONS:
V_{CC} = 1.25 VMIN/1.50 V MAX.
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

TRUTH TABLE

Data	$\overline{\text{Common}}$	Output
L	L	L
L	H	L
H	L	H
H	H	L

LOGIC DIAGRAM





NOTES

1. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

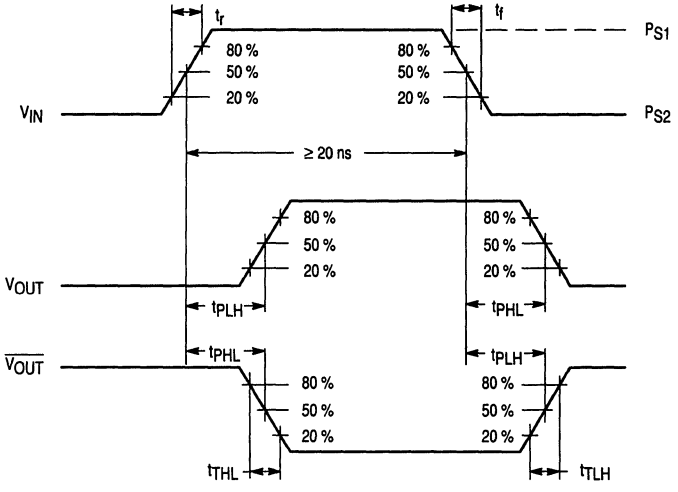


Figure 1. Switching Test Circuit and Waveforms

10591
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}
T_A = 25 °C	- 0.780	- 1.85	- 1.105	- 1.475	- 0.89	- 1.69	- 5.2
T_A = 125 °C	- 0.630	- 1.82	- 1.000	- 1.400	- 0.76	- 1.64	- 5.2
T_A = - 55 °C	- 0.880	- 1.92	- 1.255	- 1.510	- 0.99	- 1.72	- 5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 1.25 V, Output Load = 845 Ω to - 5.2 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	GND	P. U. T.
V_{OH}	High Output Voltage	+ 0.255	+ 0.44	+ 0.375	+ 0.62	+ 0.111	+ 0.344	V	5 - 7, 10 - 12				8	1	16	2 - 4, 13 - 15
V_{OL}	Low Output Voltage	- 0.49	- 0.29	- 0.43	- 0.23	- 0.538	- 0.338	V		9			8	1	16	2 - 4, 13 - 15
V_{OH1}	High Output Voltage	- 0.49	- 0.27	- 0.43	- 0.21	- 0.538	- 0.318	V	5 - 7, 10 - 12	9		5 - 7, 10 - 12	8	1	16	2 - 4, 13 - 15
V_{OL1}	Low Output Voltage	+ 0.235	+ 0.44	+ 0.355	+ 0.62	+ 0.091	+ 0.344	V	5 - 7, 10 - 12	9	5 - 7, 10 - 12	9	8	1	16	2 - 4, 13 - 15
I_{IH1}	Input Current High		245		415		415	µA	5 - 7, 10 - 12				8	1	16	2 - 4, 13 - 15
I_{IH2}	Input Current High		265		450		450	µA	9				8	1	16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 10 - 12			8	1	16	2 - 4, 13 - 15
I_{EE}	Power Supply Current	- 35	- 10	- 39	- 10	- 39	- 10	mA	9				8	1	16	8
I_{CC}	Power Supply Drain Current		23		23		23	µA	9				8	1	16	1

10591
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained.

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}
T_A = 25 °C	- 0.780	- 1.85	- 1.105	- 1.475	- 0.89	- 1.69	- 5.2
T_A = 125 °C	- 0.630	- 1.82	- 1.000	- 1.400	- 0.76	- 1.64	- 5.2
T_A = - 55 °C	- 0.880	- 1.92	- 1.255	- 1.510	- 0.99	- 1.72	- 5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 1.25 V, Output Load = 91 Ω to GND							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE}	P_{S1}	P_{S2}	GND	P. U. T.
t_{TLH}	Rise Time	1.1	4.3	1.0	5.0	1.0	4.6	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	1	8	5 - 7, 10 - 12	7, 9	16	2, 3, 14, 15
t_{THL}	Fall Time	1.1	4.3	1.0	5.0	1.0	4.6	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	1	8	5 - 7, 10 - 12	7, 9	16	2, 3, 14, 15
t_{PLH} t_{PHL}	Propagation Delay Data Input to Output	1.0	3.4	1.0	4.0	1.0	3.7	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	1	8	5 - 7, 10 - 12	7, 9	16	2, 3, 14, 15
t_{PLH} t_{PHL}	Propagation Delay Enable Input to Output	1.0	4.5	1.0	5.3	1.0	4.9	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	1	8	5 - 7, 10 - 12	7, 9	16	2, 3, 14, 15

MOTOROLA

Quad Bus Driver

Military 10592

ELECTRICALLY TESTED PER:
MPG 10592

The 10592 contains four line drivers with complementary outputs. Each driver has a Data (D) input and shares an Enable ($\overline{E}$) input with another driver. The two driver outputs are the uncommitted collectors of a pair of NPN transistors operating as a current switch. Each driver accepts 10K MECL input signals and provides a nominal signal swing of 800 mV across a 50 Ω load at each output collector.

Outputs can drive higher values of load resistance, provided that the combination of I_R drop and load return voltage V_{LR} does not cause an output collector to go more negative than -2.4 V with respect to V_{CC}. To avoid output transistor breakdown, the load return voltage should not be more positive than +5.5 V with respect to V_{CC}.

When the $\overline{E}$ input is high, both output transistors of a driver are nonconducting. When not used, the $\overline{E}$ inputs, as well as the D inputs, may be left open.

- Open Collector Outputs Drive Terminated Lines or Transformers
- 50 kΩ Input Pull-down Resistors on All Inputs (Unused Inputs May be left Open)
- 805 mW typ/pkg (No Load)
- Propagation Delay = 3.5 ns typ ($\overline{E}$-Output)
  = 3.0 ns typ (D-Output)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
Z_2	1	5	2	GND
$\overline{Z_2}$	2	6	3	GND
Z_1	3	7	4	GND
$\overline{Z_1}$	4	8	5	GND
D_1	5	9	7	OPEN
D_2	6	10	8	OPEN
$\overline{E_1}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
$\overline{E_2}$	9	13	12	OPEN
D_3	10	14	13	OPEN
D_4	11	15	14	OPEN
$\overline{Z_4}$	12	16	15	GND
Z_4	13	1	17	GND
$\overline{Z_3}$	14	2	18	GND
Z_3	15	3	19	GND
V_{CC}	16	4	20	GND

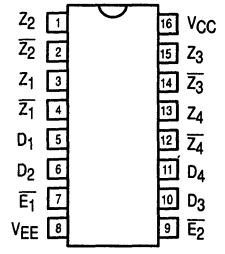
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

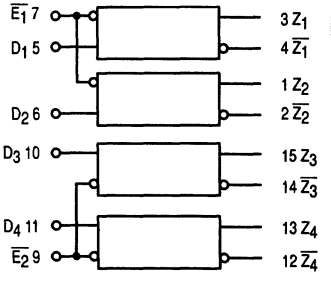
1) JAN: N/A
2) SMD: N/A
3) 883: 10592/BXAJC
X = CASE OUTLINE AS FOLLOWS:

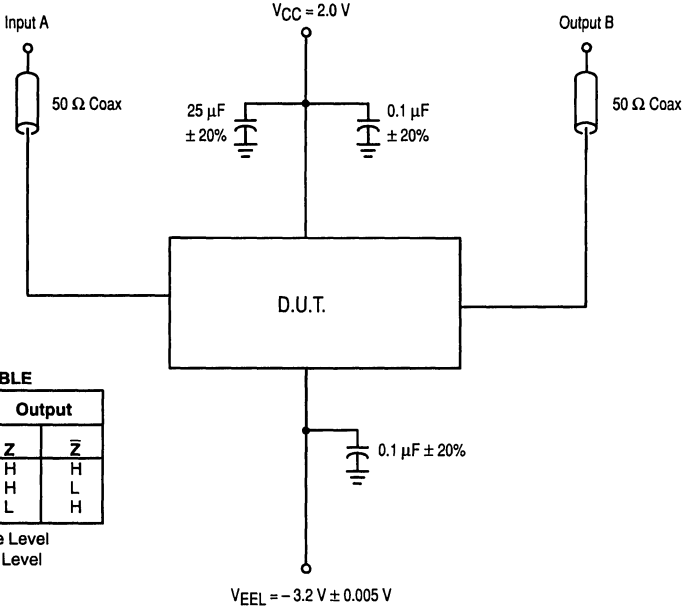
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM

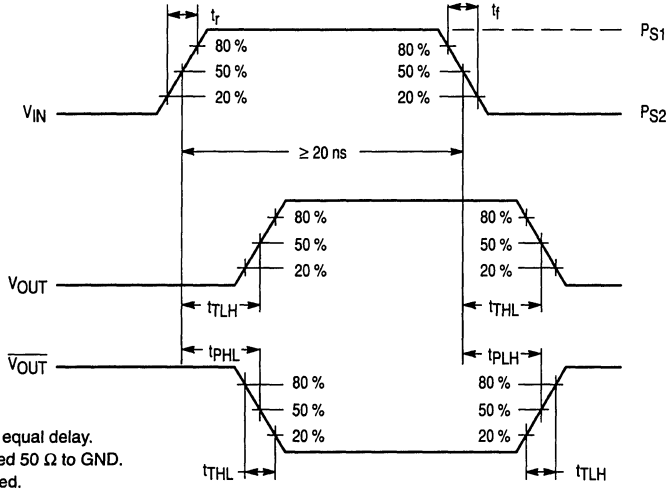




TRUTH TABLE

Inputs		Output	
$\overline{E}$	D	Z	$\overline{Z}$
H	X	H	H
L	H	H	L
L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care



NOTES
1. L1 = L2: Matched for equal delay.
2. All other outputs loaded 50 Ω to GND.
3. 2:1 divider may be used.
4. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 2.0 ns ± 0.2 ns.

Figure 1. Switching Test Circuit and Waveforms

10592
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)											
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE} (MIN)	V_{EE} (MAX)	V_{EE} (Nom)	B_{VO}	V_{LK}	V_{OLS}
T_A = 25 °C	- 0.780	- 1.85	- 1.105	- 1.475	- 0.89	- 1.69	- 5.72	- 4.68	- 5.2	+ 5.095	- 1.850	- 2.4
T_A = 125 °C	- 0.630	- 1.82	- 1.000	- 1.400	- 0.78	- 1.655	- 5.72	- 4.68	- 5.2	+ 4.960	- 1.825	- 2.4
T_A = - 55 °C	- 0.880	- 1.92	- 1.255	- 1.510	- 0.97	- 1.715	- 5.72	- 4.68	- 5.2	+ 4.960	- 1.89	- 2.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = GND, Output Load = 50 Ω to GND, V_{LR} = 270 Ω to + 5.5 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{LR}	V_{OLS}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.10	+ 0.10	- 0.10	+ 0.10	- 0.15	+ 0.05	V	5, 6, 10, 11	5, 6, 10, 11					8	16	1 - 4, 12 - 15
V_{OL}	Low Output Voltage	- 0.90	- 0.70	- 0.95	- 0.70	- 0.85	- 0.60	V	5, 6, 10, 11	5, 6, 10, 11					8	16	1 - 4, 12 - 15
V_{OLC}	Low Output Voltage	- 0.90	- 0.70	- 0.95	- 0.70	- 0.85	- 0.60	V			5, 6, 10, 11	5, 6, 10, 11			8	16	1 - 4, 12 - 15
V_{OHC}	High Output Voltage	- 0.10	+ 0.10	- 0.10	- 0.10	- 0.15	+ 0.05	V			5, 6, 10, 11	5, 6, 10, 11			8	16	1 - 4, 12 - 15
I_{IH1}	Input Current High		220		350		350	µA	5 - 7, 9 - 11						8	16	5 - 7, 9 - 11
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7, 9 - 11					8	16	5 - 7, 9 - 11
I_{OV}	Short Circuit Current (No Output Voltage)		104.4		102.2		102.2	mA	7, 9				1 - 4, 12 - 15		8	16	1 - 4, 12 - 15
I_{OS}	Output Short Circuit Current	34.1		34.7		- 34.7		mA		5, 6, 10, 11				1 - 4, 12 - 15	8	16	1 - 4, 12 - 15
I_{QOFF}	Open Collector Input Current		500		500		500	µA		2, 7, 9, 14, 15					8	16	2, 7, 9, 14, 15
I_{EE}	Power Supply Drain Current	- 140		- 154		- 154		mA							8	16	8

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to Gnd.

10592
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)											
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE} (MIN)	V_{EE} (MAX)	V_{EE} (Nom)	B_{VO}	V_{LK}	V_{OLS}
T_A = 25 °C	- 0.780	- 1.85	- 1.105	- 1.475	- 0.89	- 1.69	- 5.72	- 4.68	- 5.2	+ 5.095	- 1.850	- 2.4
T_A = 125 °C	- 0.630	- 1.82	- 1.000	- 1.400	- 0.78	- 1.655	- 5.72	- 4.68	- 5.2	+ 4.960	- 1.825	- 2.4
T_A = - 55 °C	- 0.880	- 1.92	- 1.255	- 1.510	- 0.97	- 1.715	- 5.72	- 4.68	- 5.2	+ 4.960	- 1.89	- 2.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = GND, Output Load = 50 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	0.5	3.3	0.5	4.7	0.5	3.8	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15
t_{THL}	Fall Time	0.5	3.3	0.5	4.7	0.5	3.8	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15
t_{PLH} t_{PHL}	Propagation Delay Data	1.5	4.5	1.5	5.6	1.5	5.3	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15
t_{PLH} t_{PHL}	Propagation Delay Enable	2.0	6.0	1.0	9.0	1.0	6.0	ns	6, 9, 10, 11	1 - 4, 12 - 15	16	8	10, 11	1 - 4, 12 - 15

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50 Ω resistor to Gnd.

Hex Inverter/Buffer

Military 10595

ELECTRICALLY TESTED PER:
MPG 10595

The 10595 is a Hex Buffer Inverter which is built using EXCLUSIVE NOR gates. There is a common input to these gates which when placed low or left open allows them to act as inverters.

With the common input connected to a high logic level the 10595 is a hex buffer, useful for high fanout clock driving and reducing stub lengths on long bus lines.

- 285 mW Max/Pkg (No Load)
- t_{pd} = 4.0 ns typ
- t_{pd} = 4.0 ns typ
- t_r, t_f = 2.0 ns typ (20% - 80%)

AVAILABLE AS

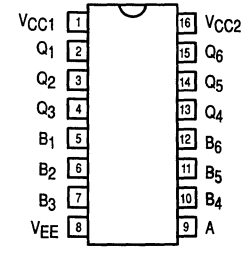
1) JAN: N/A
2) SMD: N/A
3) 883: 10595/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω to V_{TT}
Q_2	3	7	4	51 Ω to V_{TT}
Q_3	4	8	5	51 Ω to V_{TT}
B_1	5	9	7	OPEN
B_2	6	10	8	OPEN
B_3	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
A	9	13	12	OPEN
B_4	10	14	13	OPEN
B_5	11	15	14	OPEN
B_6	12	16	15	OPEN
Q_4	13	1	17	51 Ω to V_{TT}
Q_5	14	2	18	51 Ω to V_{TT}
Q_6	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

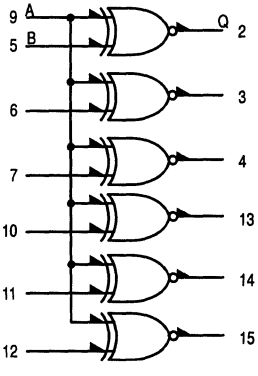


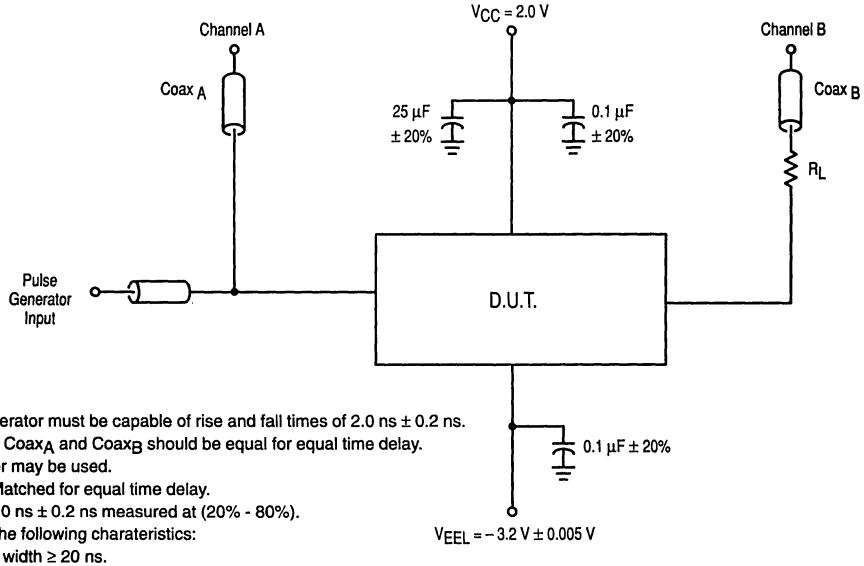
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

TRUTH TABLE

Inputs		Output
A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

LOGIC DIAGRAM





NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 2:1 divider may be used.
4. $L_1 = L_2$ Matched for equal time delay.
5. $t_r = t_f = 2.0$ ns ± 0.2 ns measured at (20% - 80%).
6. V_{IN} has the following charateristics:
   a) Pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
7. $R_L = 50\ \Omega$ resistor in series with 50 Ω coax constituting the 100 Ω load.
8. All other outputs loaded 100 Ω to ground.

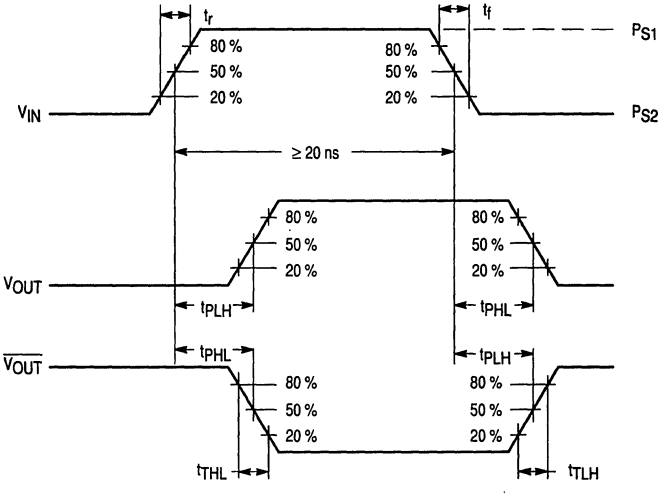


Figure 1. Switching Test Circuit and Waveforms

10595
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IIL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = -55 °C	- 0.88	- 1.92	- 1.170	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IH2}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	9				8	1, 16	2 - 4, 13 - 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V					8	1, 16	2 - 4, 13 - 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	-1.635	V			5 - 7 10 - 12		8	1, 16	2 - 4, 13 - 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	-0.88	V				5 - 7 10 - 12	8	1, 16	2 - 4, 13 - 15
I_{IH1}	Input Current High		265		450		450	µA	5 - 7 10 - 12				8	1, 16	5 - 7 10 - 12
I_{IH2}	Input Current High		290		495		495	µA	9				8	1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7 10 - 12			8	1, 16	2 - 4, 13 - 15
I_{EE}	Power Supply Drain Current	- 49		- 54		- 54		mA					8	1, 16	8

10595
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IILL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = -55 °C	- 0.88	- 1.92	- 1.170	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P. U. T.
t_{TLH}	Rise Time	1.1	4.5	1.0	5.3	1.0	4.9	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	1, 16	8		2 - 4, 13 - 15
t_{THL}	Fall Time	1.1	4.5	1.0	5.3	1.0	4.9	ns	5 - 7, 10 - 12	2 - 4, 13 - 15	1, 16	8		2 - 4, 13 - 15
t_{PLH} t_{PHL}	Propagation Delay B Inputs	1.1	4.0	1.0	4.7	1.0	4.3	ns	5 - 7, 11 - 13	2 - 4, 13 - 15	1, 16	8	9	2 - 4, 13 - 15
t_{PLH} t_{PHL}	Propagation Delay A Inputs	1.1	5.0	1.0	5.9	1.0	5.4	ns	5 - 7, 11 - 13	2 - 4, 13 - 15	1, 16	8	9	2 - 4, 13 - 15

MOTOROLA

Hex "AND" Gate

ELECTRICALLY TESTED PER:
MIL-M-38510/06202

The 10597 provides a high speed hex AND function with strobe capability.

- 285 mW Max/Pkg (No Load)
- t_{pd} = 2.8 ns typ (B - Q)
- t_{pd} = 3.8 ns typ (A - Q)
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
B_{OUT}	3	7	4	51 Ω to V_{TT}
C_{OUT}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	GND
B_{IN}	6	10	8	GND
C_{IN}	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Common	9	13	12	GND
D_{IN}	10	14	13	GND
E_{IN}	11	15	14	GND
F_{IN}	12	16	15	GND
D_{OUT}	13	1	17	51 Ω to V_{TT}
E_{OUT}	14	2	18	51 Ω to V_{TT}
F_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

TRUTH TABLE

Inputs		Output
A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H

Military 10597

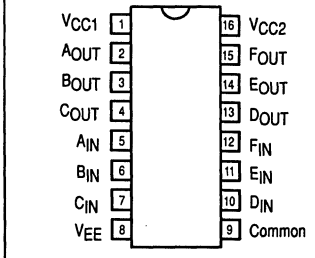
MPO

AVAILABLE AS:

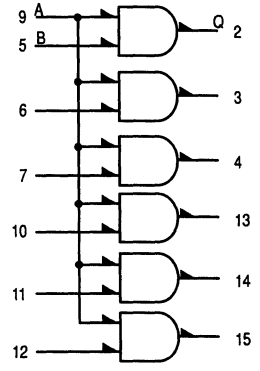
1) JAN: JM 38510/06202
2) SMD: N/A
3) 883C: 10597/BXAJC
X = CASE OUTLINE AS FOLLOWS:

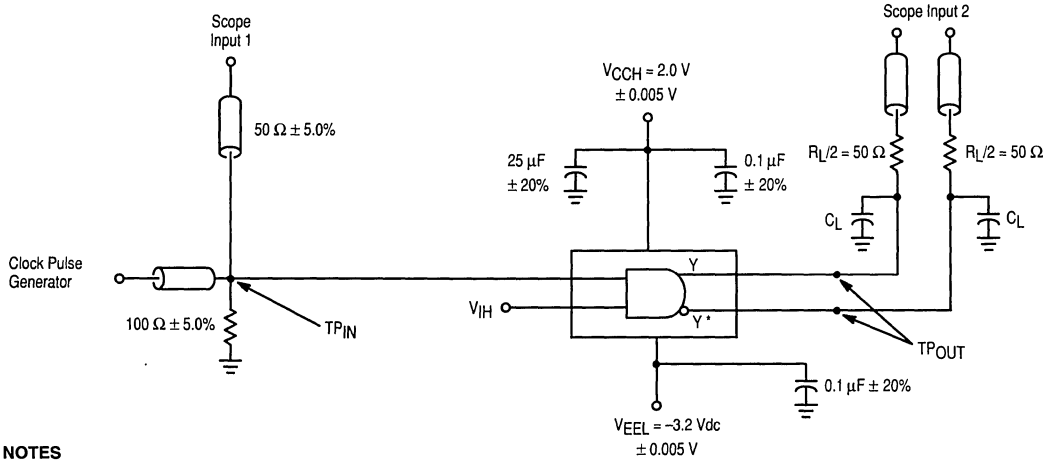
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≥ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. (*) applies to gate 4 only.
5. t_p = 40 ns ± 1.0 ns.
6. $Z_{OUT} \approx 50\ \Omega$.
7. $t_{THL} = t_{TLH}$ = 2.0 ns (200% - 80%) ± 0.2 ns.
8. PRR = 1.0 MHz ± 0.05 MHz.
9. Scope input = 50 Ω to ground.
10. C_L = 5.0 pF (including test jig).
11. $R_L/2$ = 50 Ω ± 5.0%

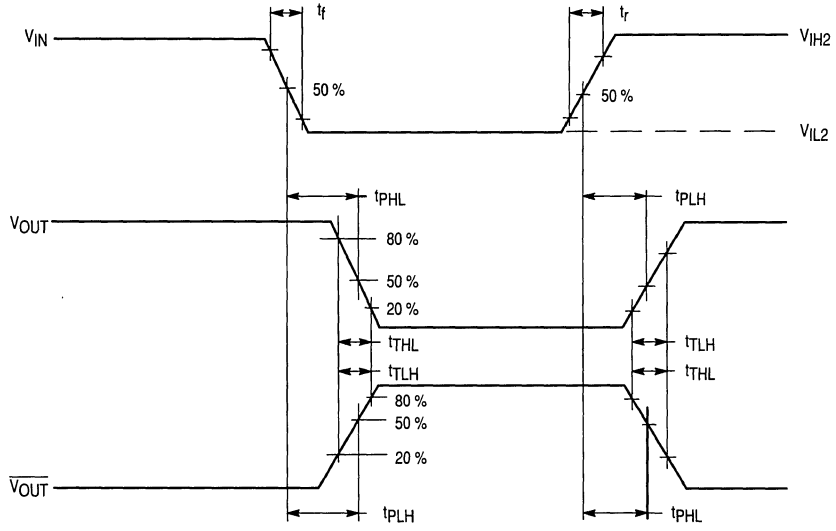


Figure 1. Switching Test Circuit and Waveforms

10597
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)						
	V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	V_{IH2}	V_{EE1}	V_{EE2}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	- 5.2	- 3.2
T_A = -55 °C	- 0.88	- 1.82	- 1.170	- 1.510	+ 1.01	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	V_{EE1}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	5 - 7 9 - 12				8	1, 16	2 - 4, 13 - 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V					8	1, 16	2 - 4, 13 - 15
V_{OL1}	Low Output Voltage		- 1.60		- 1.525		-1.635	V	5 - 7 9 - 12			5 - 7 9 - 12	8	1, 16	2 - 4, 13 - 15
V_{OH1}	High Output Voltage	- 0.95		- 0.845		- 1.10		V	5 - 7 9 - 12		5 - 7 9 - 12		8	1, 16	2 - 4, 13 - 15
I_{IH1}	Input Current High		265		450		450	µA	5 - 7 10 - 12				8	1, 16	7 - 9, 10 - 12
I_{IH2}	Input Current High		290		495		495	µA	9				8	1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7 9 - 12			8	1, 16	7 - 9, 10 - 12
I_{EE}	Power Supply Drain Current	- 49		- 54		- 54		mA					8	1, 16	8

10597
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)						
	V_{IH1}	V_{IL1}	V_{ITH}	V_{ITL}	V_{IH2}	V_{EE1}	V_{EE2}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	- 5.2	- 3.2
T_A = -55 °C	- 0.88	- 1.82	- 1.170	- 1.510	+ 1.01	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{IH2}	V_{CC}	V_{EE2}	P. U. T.
t_{TLH}	Rise Time	1.1	4.5	1.0	5.3	1.0	4.9	ns	5 - 7, 9 - 12	2 - 4, 13 - 15		1, 16	8	2 - 4, 13 - 15
t_{THL}	Fall Time	1.1	4.5	1.0	5.3	1.0	4.9	ns	5 - 7, 9 - 12	2 - 4, 13 - 15		1, 16	8	2 - 4, 13 - 15
t_{PLH1}	Propagation Delay	1.1	4.0	1.0	4.7	1.0	4.3	ns	5 - 7, 9 - 12	2 - 4, 13 - 15		1, 16	8	2 - 4, 13 - 15
t_{PLH2}	Propagation Delay	1.1	5.0	1.0	5.9	1.0	5.4	ns		2 - 4, 13 - 15	5 - 7, 9 - 12	1, 16	8	2 - 4, 13 - 15
t_{PHL1}	Propagation Delay	1.1	4.0	1.0	4.7	1.0	4.3	ns	5 - 7, 9 - 12	2 - 4, 13 - 15		1, 16	8	2 - 4, 13 - 15
t_{PHL2}	Propagation Delay	1.1	5.0	1.0	5.9	1.0	5.4	ns		2 - 4, 13 - 15	5 - 7, 9 - 12	1, 16	8	2 - 4, 13 - 15

Monostable Multivibrator

Military 10598

ELECTRICALLY TESTED PER:
5962-8777301

The 10598 is a retriggerable monostable multivibrator. Two enable inputs permit triggering on any combination of positive or negative edges as shown in the accompanying table. The trigger input is buffered by Schmitt triggers making it insensitive to input rise and fall times.

The pulse width is controlled by external capacitor and resistor. The resistor sets a current which is the linear discharge rate of the capacitor. Also, the pulse width can be controlled by the external current source or voltage

For high-speed response with minimum delay, a hi-speed input is also provided. This input bypasses the internal Schmitt triggers and the output responds within 2.0 nanoseconds typically.Output logic and threshold levels are standard MECL 10,000. Test conditions are per table 2. Each "Precondition" referred to in table 2 is per the sequence of table 1.

- 580 mW Max/Pkg (No Load)
- t_{pd} = 4.0 ns typ Trigger Input to Q
  = 2.0 ns typ Hi-Speed Input to Q

Min Timing Pulse Width	PW_{Qmin}	10 ns typ[1]
Max Timing Pulse Width	PW_{Qmax}	>10 ns typ[2]
Min Trigger Pulse Width	PW_T	2.0 ns typ
Min Hi-Speed Trigger Pulse Width	PW_{HS}	3.0 ns typ
Enable Setup Time	t_{set}	1.0 ns typ
Enable Hold Time	t_{hold}	1.0 ns typ

[1] C_{Ext} = 0 (Pin 4 open), R_{Ext} = 0 (Pin 6 to V_{EE})
[2] C_{Ext} = 10 µF, R_{Ext} = 2.7 kΩ

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{Q}$	2	6	3	51 Ω to V_{TT}
Q	3	7	4	51 Ω to V_{TT}
C_{EXT}	4	8	5	OPEN
$\overline{E_{Pos.}}$	5	9	7	OPEN
R_{EXT}	6	10	8	V_{EE}
Ext. Pulse Width Control	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
N.C.	9	13	12	OPEN
$\overline{E_{Neg.}}$	10	14	13	OPEN
N.C.	11	15	14	OPEN
N.C.	12	16	15	OPEN
Trigger Input	13	1	17	OPEN
N.C.	14	2	18	OPEN
Hi-Speed Input	15	3	19	OPEN
V_{CC2}	16	4	20	GND

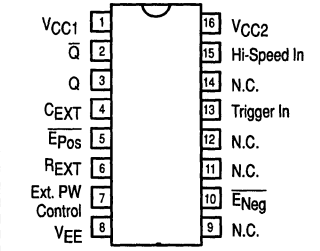
BURN - IN CONDITIONS:
V_{TT} = - 2.2 V MIN/ - 2.0 V MAX
V_{EE} = - 5.7 V MAX/ - 5.2 V MIN

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8777301
3) 883: 10598/BXAJC
X = CASE OUTLINE AS FOLLOWS:

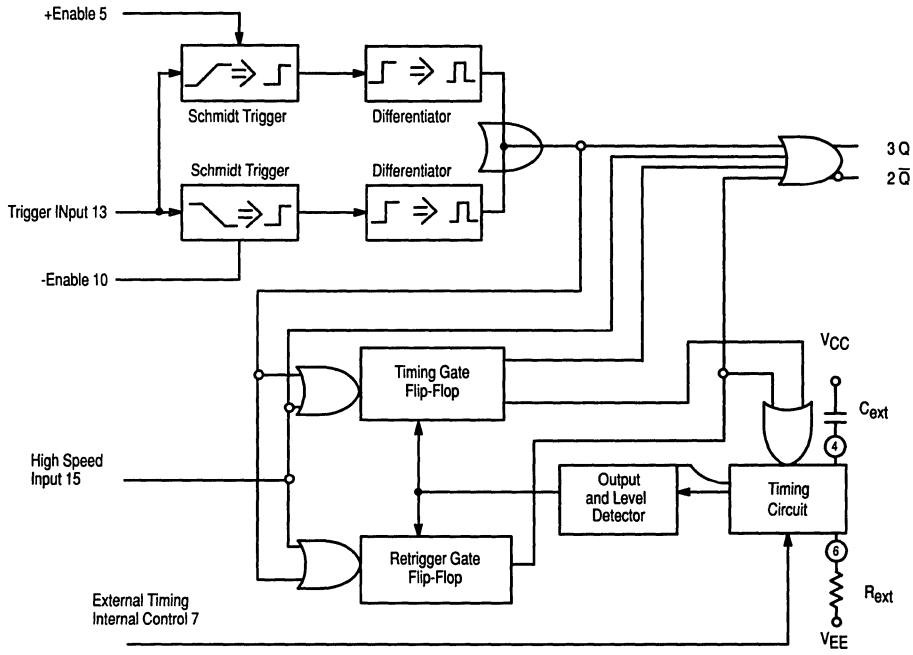
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

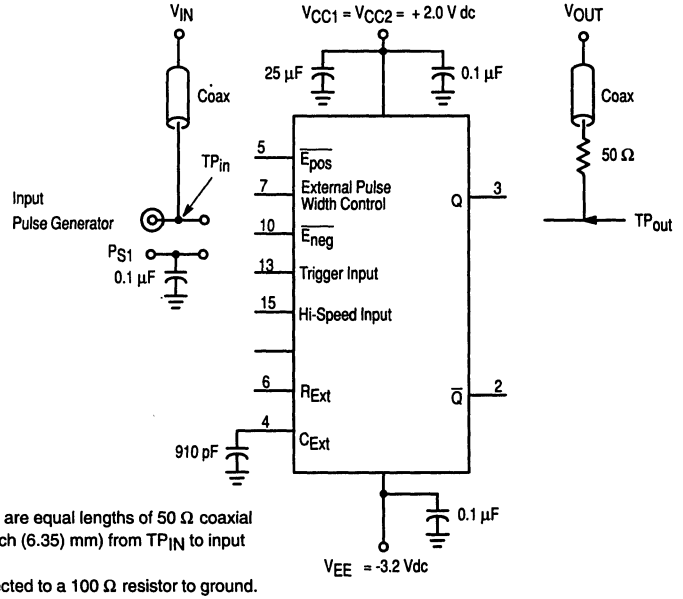


TRUTH TABLE

Inputs $\overline{E_{pos}}$	Inputs $\overline{E_{neg}}$	Output
L	L	Triggers on both positive and negative input slopes
L	H	Triggers on the positive input slope
H	L	Triggers on the negative input slope
H	H	Trigger disabled



Block Diagram

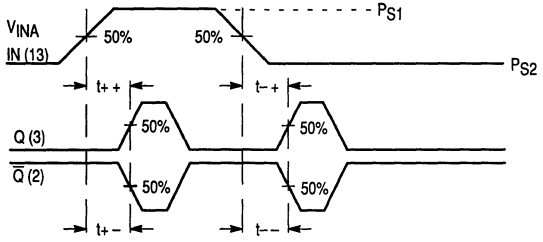


NOTES

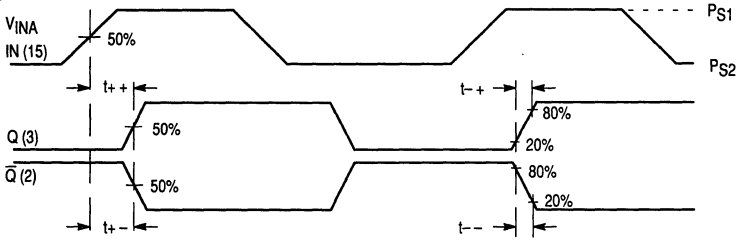
1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≥ 0.250 inch (6.35) mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
2. Outputs not under test should be connected to a 100 Ω resistor to ground.
3. $t_{THL} = t_{TLH} = 2.0 \pm$ ns (20% - 80%).
4. 50 Ω termination to ground located in each scope probe.

Figure 1. Switching Test Circuit

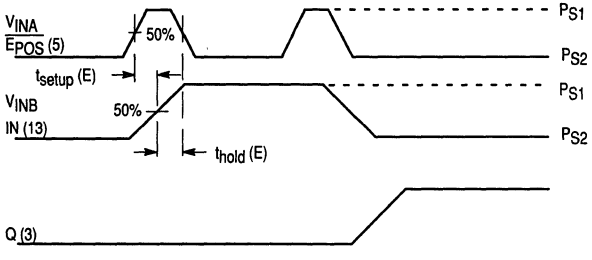
Trigger Delay Test

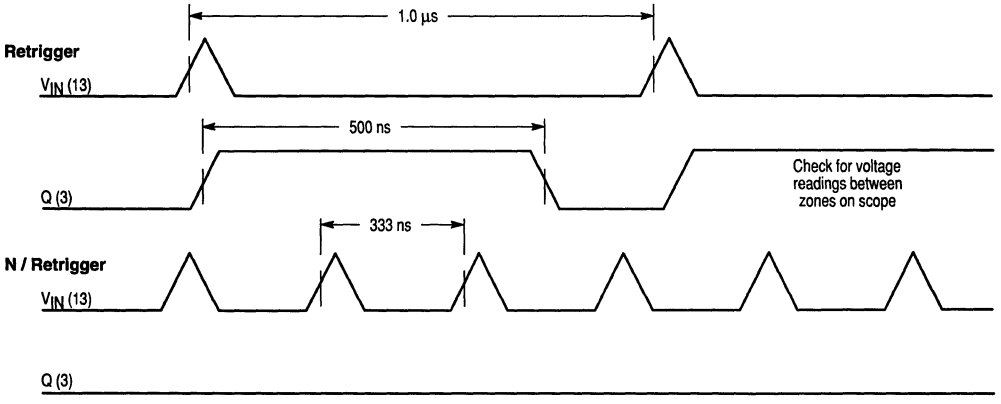


High Speed Trigger



t_{Setup} / t_{Hold} Tests

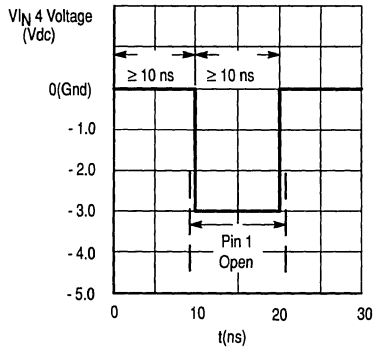




The output stays high so no voltage difference is measured on the scope. All zone markers are at the same level.

Figure 2. Switching Test Circuit Waveforms

Table 1. Precondition Sequence

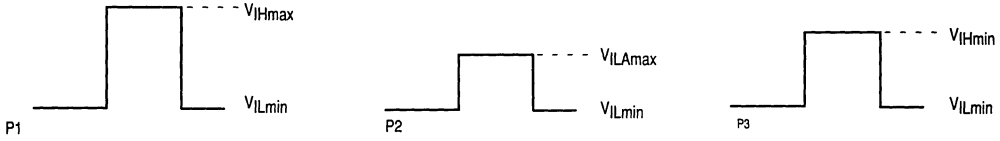


1. At t = 0
   a) Apply V_{IHmax} to Pin 5 and 10.
   b) Apply V_{ILmin} to Pin 15.
   c) Ground Pin 4.
2. At t ≥ 10 ns
   a) Open Pin 1.
   b) Apply - 3.0 Vdc to Pin 4.
   Hold these conditions for ≥ 10 ns.
3. Return Pin 4 to Ground and preform test as indicated in Table 2.

3

Table 2. Conditions for Testing Output Levels

(See Table 1 for Precondition Sequence)



Test P.U.T	Pin Condition 5	10	13	15
Precondition				
V_{OH} 2			V_{ILmin}	
V_{OH} 3			P1	
Precondition				
V_{OL} 3			V_{ILmin}	
V_{OL} 2			P1	
Precondition				
V_{OHA} 2				V_{ILAmax}
V_{OHA} 3				V_{IHAmin}
Precondition				
V_{OHA} 2			V_{ILmin}	
V_{OHA} 3			P3	
Precondition				
V_{OHA} 2			P2	
V_{OHA} 3			P3	
Precondition				
V_{OHA} 2		V_{IHmax}	P2	
V_{OHA} 3		V_{IHmax}	P3	
Precondition				
V_{OHA} 2		V_{IHmax}	P1	
V_{OHA} 3		V_{IHmax}	P1	

Test P.U.T	Pin Condition 5	10	13	15
Precondition				
V_{OHA} 2		V_{IHAmin}	P1	
V_{OHA} 3		V_{ILAmax}	P1	
Precondition				
V_{OLA} 3				V_{ILAmax}
V_{OLA} 2				V_{IHAmin}
Precondition				
V_{OLA} 2			V_{ILmin}	
V_{OLA} 3			V_{ILmin}	
Precondition				
V_{OLA} 3			P2	
V_{OLA} 2			P3	
Precondition				
V_{OLA} 3		V_{IHmax}	P2	
V_{OLA} 2		V_{IHmax}	P3	
Precondition				
V_{OLA} 3	V_{IHAmin}	V_{IHmax}	P1	
V_{OLA} 2	V_{ILAmax}	V_{IHmax}	P1	
Precondition				
V_{OLA} 3	V_{IHmax}	V_{IHAmin}	P1	
V_{OLA} 2	V_{IHmax}	V_{ILAmax}	P1	

10598
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)										
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}	V_{CC}	V_{T1}	V_{T2}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2	+2.0	-2.45	-3.0
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2	+2.0	-2.35	-2.9
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2	+2.0	-2.55	-3.09

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to – 2.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{CC}	P_{1-3}	$V_{T1, 2}$	GND	P. U. T.
V_{OH}	High Output Voltage	– 0.93	– 0.78	– 0.825	– 0.63	– 1.08	– 0.88	V		13			6, 8	1, 4, 16	13		4	2, 3
V_{OL}	Low Output Voltage	– 1.85	– 1.62	– 1.82	– 1.545	– 1.92	– 1.665	V		13			6, 8	1, 4, 16	13		4	2, 3
V_{OLA}	Low Output Voltage	– 1.85	– 1.60	– 1.82	– 1.525	– 1.92	– 1.635	V	10	13	10	10	6, 8	1, 4, 16	13	4	4	2, 3
V_{OHA}	High Output Voltage	– 0.95	– 0.78	– 0.845	– 0.63	– 1.10	– 0.88	V	10	13	10	10	6, 8	1, 4, 16	13	4	4	2, 3
I_{IH1}	Input Current High		220		375		375	µA	13				6, 8	1, 4, 16			4	13
I_{IH2}	Input Current High		260		450		450	µA	5, 10				6, 8	1, 4, 16			4	5, 10
I_{IH3}	Input Current High		350		595		595	µA	15				6, 8	1, 4, 16			4	15
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5, 10, 13, 15			6, 8	1, 4, 16			4	5, 10, 13, 15
V_{R4}	Bias Voltage	-4.16	-3.4	-4.16	-3.4	-4.16	-3.4	V					6, 8	1, 4, 16			4	7
I_{EE}	Power Supply Drain Current	– 100		– 111		– 111		mA					6, 8	1, 4, 16			4	8

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

10598
QUIESCENT LIMIT TABLE *

Test Temperature	Test Voltage Values (Volts)													
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}	V_{CC}	V_{T1}	V_{T2}	P_{S11}	P_{S12}	P_{S13}
T_A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2	+2.0	-2.45	-3.0	0.0	0.0	-3.2
T_A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2	+2.0	-2.35	-2.9	0.0	0.0	-3.2
T_A = - 55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2	+2.0	-2.55	-3.09	0.0	0.0	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S11}	P_{S12}	P. U. T.
t_{TLH}/t_{THL}	Rise Time/Fall Time High Speed Trigger Delay to Output	1.5	3.5	1.0	4.5	1.0	4.5	ns	13, 15	2, 3	1, 16	8	7		2, 3, 13, 15
t_{PHL}/t_{PLH}	Propagation Delay High Speed Trigger Delay to Output	1.5	2.8	1.0	4.0	1.0	4.0	ns	13, 15	2, 3	1, 16	8	7		2, 3, 13, 15
t_{PHL}/t_{PLH}	Propagation Delay Trigger Delay to Output	2.5	5.5	2.0	7.0	2.0	7.0	ns	13, 15	2, 3	1, 16	8	7		2, 3, 13, 15
t_{Setup} (E)	Enable Setup Time	3.5						ns	5, 13	3	1, 16	8	7		5, 13
t_{Hold} (E)	Enable Hold Time	3.5						ns	5, 13	3	1, 16	8	7		5, 13
$\overline{R_{Trig}}$	$\overline{\text{Retrigger}}$	–50	50					ns	5, 13	3	1, 16	8		7	3
R_{Trig}	Retrigger	0.15	1.0					ns	5, 13	3	1, 16	8		7	3

*** ELECTRICAL CHARACTERISTICS**

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

Dual 3-Input 3-Output "OR" Gate

ELECTRICALLY TESTED PER:
MPG 10610

The 10610 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the 10610 particularly useful in clock distribution applications where minimum clock skew is desired.

- 220 mW Max/Pkg (No Load)
- t_{pd} = 1.5 ns typ (All Output Loaded)
- t_r, t_f = 1.5 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
A_{OUT}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	OPEN
A_{IN}	6	10	8	GND
A_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	VEE
B_{IN}	9	13	12	OPEN
B_{IN}	10	14	13	OPEN
B_{IN}	11	15	14	GND
B_{OUT}	12	16	15	51 Ω to V_{TT}
B_{OUT}	13	1	17	51 Ω to V_{TT}
B_{OUT}	14	2	18	51 Ω to V_{TT}
V_{CC1}	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

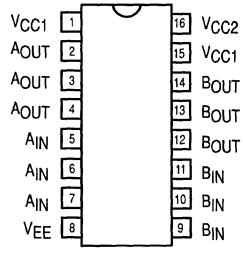
Military 10610

AVAILABLE AS:

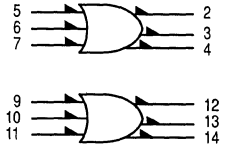
1) JAN: N/A
2) SMD: N/A
3) 883: 10610/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

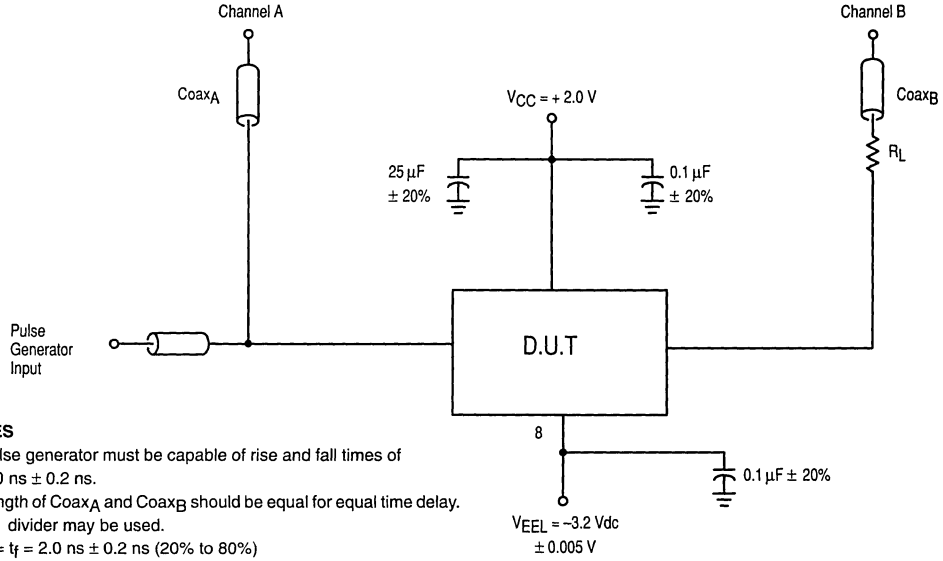
The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8



NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f$ = 2.0 ns ± 0.2 ns (20% to 80%)
5. R_L = 50 Ω resistor in series with 50 Ω coax constituting the 100 Ω load.
6. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
7. Unused outputs should be loaded 100 Ω to ground.

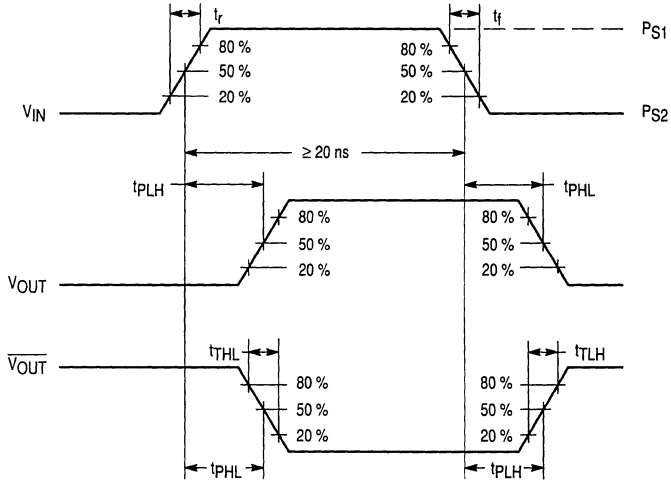


Figure 1. Switching Test Circuit and Waveforms

10610
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	5 - 7 9 - 11				8	1, 15, 16	2 - 4, 12 - 14
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V		5 - 7 9 - 11			8	1, 15, 16	2 - 4, 12 - 14
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V				5 - 7 9 - 11	8	1, 15, 16	2 - 4, 12 - 14
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V			5 - 7 9 - 11		8	1, 15, 16	2 - 4, 12 - 14
I_{IH1}	Input Current High		410		700		700	µA	5 - 7 9 - 11				8	1, 15, 16	5 - 7 9 - 11
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7 9 - 11			8	1, 15, 16	5 - 7 9 - 11
I_{EE}	Power Supply Drain Current	- 38		- 42		- 42		mA					8	1, 15, 16	8

10610
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.0	2.5	1.0	3.0	1.0	2.9	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 14
t_{THL}	Fall Time	1.0	2.5	1.0	3.0	1.0	2.9	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 14
t_{PHL}	Propagation Delay	1.0	2.9	1.0	3.4	1.0	3.3	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 14
t_{PLH}	Propagation Delay	1.0	2.9	1.0	3.4	1.0	3.3	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 14

MOTOROLA

Dual 3-Input 3-Output "NOR" Gate

ELECTRICALLY TESTED PER:
MPG 10611

The 10611 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the 10611 particularly useful in clock distribution applications where minimum clock skew is desired.

- 220 mW Max/Pkg (No Load)
- t_{pd} = 1.5 ns typ (All Output Loaded)
- t_r, t_f = 1.5 ns typ (20% - 80%)

3

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
A_{OUT}	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	OPEN
A_{IN}	6	10	8	OPEN
A_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	VEE
B_{IN}	9	13	12	OPEN
B_{IN}	10	14	13	OPEN
B_{IN}	11	15	14	OPEN
B_{OUT}	12	16	15	51 Ω to V_{TT}
B_{OUT}	13	1	17	51 Ω to V_{TT}
B_{OUT}	14	2	18	51 Ω to V_{TT}
V_{CC1}	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Military 10611

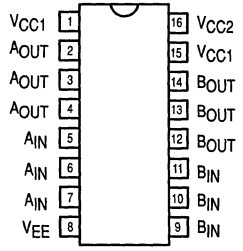
MPO

AVAILABLE AS:

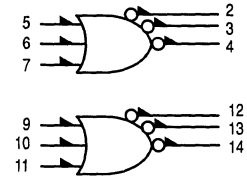
1) JAN: N/A
2) SMD: N/A
3) 883: 10611/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

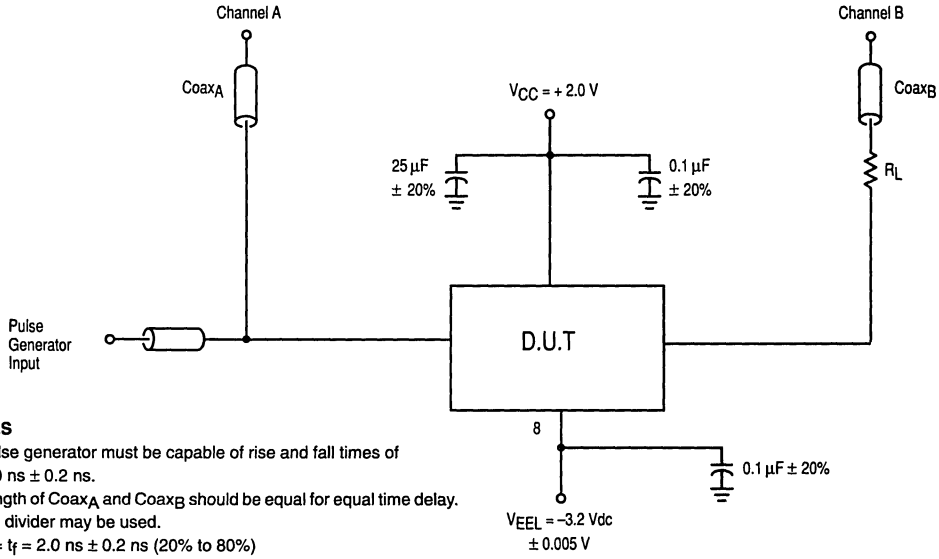
The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8



NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)
5. $R_L = 50\ \Omega$ resistor in series with 50 Ω coax constituting the 100 Ω load.
6. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
7. Unused outputs should be loaded 100 Ω to ground.

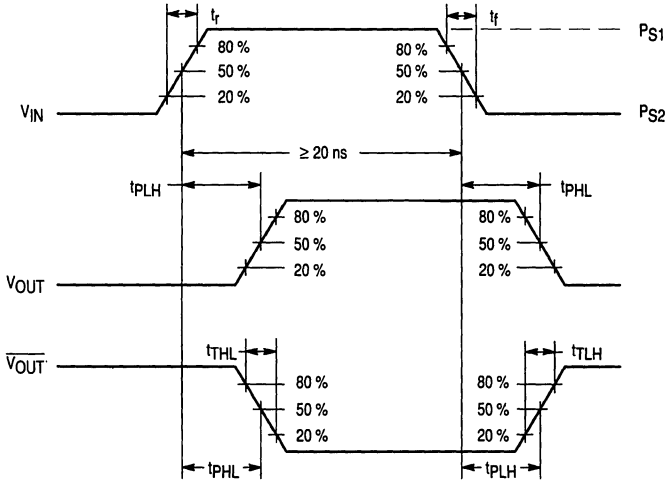


Figure 1. Switching Test Circuit and Waveforms

10611
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V		5 - 7 9 - 11			8	1, 15, 16	2 - 4, 12 - 14
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	5 - 7 9 - 11				8	1, 15, 16	2 - 4, 12 - 14
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V			5 - 7 9 - 11		8	1, 15, 16	2 - 4, 12 - 14
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V				5 - 7 9 - 11	8	1, 15, 16	2 - 4, 12 - 14
I_{IH1}	Input Current High		410		700		700	µA	5 - 7 9 - 11				8	1, 15, 16	5 - 7 9 - 11
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7 9 - 11			8	1, 15, 16	5 - 7 9 - 11
I_{EE}	Power Supply Drain Current	- 38		- 42		- 42		mA					8	1, 15, 16	8

10611
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.0	2.5	1.0	3.0	1.0	2.9	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 14
t_{THL}	Fall Time	1.0	2.5	1.0	3.0	1.0	2.9	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 14
t_{PHL}	Propagation Delay	1.0	2.9	1.0	3.0	1.0	2.9	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 14
t_{PLH}	Propagation Delay	1.0	2.9	1.0	3.0	1.0	2.9	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 14

High Speed Dual 3-Input 3-Output OR/NOR Gate

ELECTRICALLY TESTED PER:
5962-8775001

The 10611 is designed to drive up to six transmission lines simultaneously. The multiple outputs of this device also allow the wire "OR"-ing of several levels of gating for minimization of gate and package count.

The ability to control three parallel lines with minimum propagation delay from a single point makes the 10611 particularly useful in clock distribution applications where minimum clock skew is desired.

- 220 mW Max/Pkg (No Load)
- t_{pd} = 1.5 ns typ (All Output Loaded)
- t_r, t_f = 1.5 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
A_{OUT}	2	6	3	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	4	51 Ω to V_{TT}
$\overline{A_{OUT}}$	4	8	5	51 Ω to V_{TT}
A_{IN}	5	9	7	OPEN
A_{IN}	6	10	8	OPEN
A_{IN}	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
B_{IN}	9	13	12	OPEN
B_{IN}	10	14	13	OPEN
B_{IN}	11	15	14	OPEN
$\overline{B_{OUT}}$	12	16	15	51 Ω to V_{TT}
$\overline{B_{OUT}}$	13	1	17	51 Ω to V_{TT}
B_{OUT}	14	2	18	51 Ω to V_{TT}
V_{CC1}	15	3	19	GND
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

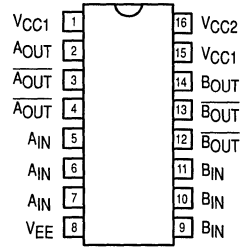
Military 10612

AVAILABLE AS:

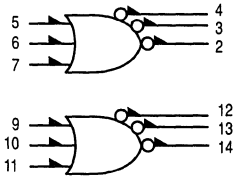
1) JAN: N/A
2) SMD: 5962-8775001
3) 883: 10612/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

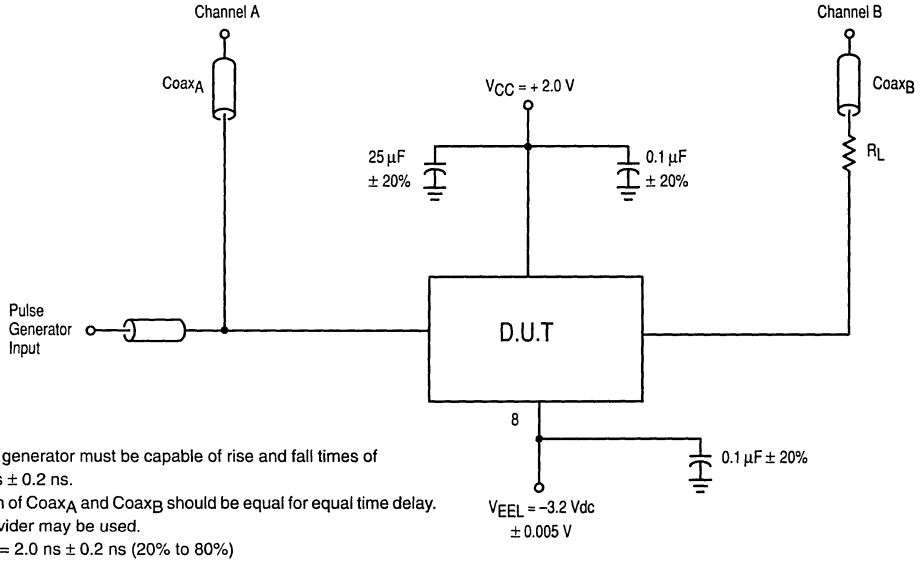
The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



V_{CC1} = Pin 1, 15
V_{CC2} = Pin 16
V_{EE} = Pin 8



NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)
5. $R_L = 50\ \Omega$ resistor in series with 50 Ω coax constituting the 100 Ω load.
6. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
7. Unused outputs should be loaded 100 Ω ground.

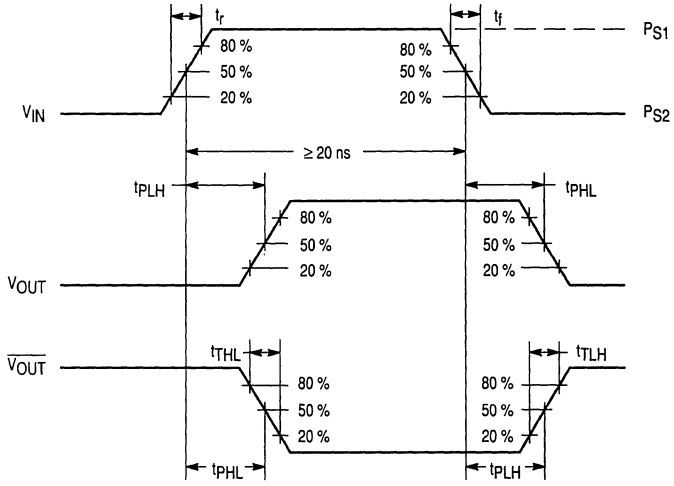


Figure 1. Switching Test Circuit and Waveforms

10612
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	5 - 7 9 - 11	5 - 7 9 - 11			8	1, 15, 16	2 - 4, 12 - 14
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	5 - 7 9 - 11	5 - 7 9 - 11			8	1, 15, 16	2 - 4, 12 - 14
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V			5 - 7 9 - 11	5 - 7 9 - 11	8	1, 15, 16	2 - 4, 12 - 14
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V			5 - 7 9 - 11	5 - 7 9 - 11	8	1, 15, 16	2 - 4, 12 - 14
I_{IH1}	Input Current High		410		700		700	µA	5 - 7 9 - 11				8	1, 15, 16	5 - 7 9 - 11
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		5 - 7 9 - 11			8	1, 15, 16	5 - 7 9 - 11
I_{EE}	Power Supply Drain Current	- 38		- 42		- 42		mA					8	1, 15, 16	8

10612
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.0	2.5	1.0	3.0	1.0	2.9	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 15
t_{THL}	Fall Time	1.0	2.5	1.0	3.0	1.0	2.9	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 15
t_{PHL}	Propagation Delay	1.0	2.5	1.0	3.0	1.0	2.9	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 15
t_{PLH}	Propagation Delay	1.0	2.5	1.0	3.0	1.0	2.9	ns	7, 9	2 - 4, 12 - 14	1, 15, 16	8	2 - 4, 12 - 15

MOTOROLA

Triple Line Receiver (High Speed)

ELECTRICALLY TESTED PER:
MPG 10616

The 10616 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The base bias supply (V_{BB}) is made available at pin 11 make the device useful as a Schmitt trigger, or in other application where a stable reference voltage is necessary.

Active current sources provide the 10616 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

Complementary outputs are provided to allow driving twisted pair lines, to enable cascading of several amplifiers in a chain, or simply to provide complement outputs of the input logic function.

3

- 150 mW Max/Pkg (No Load)
- t_{pd} = 2.0 ns typ (All Output Loaded)
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
$\overline{A_{OUT}}$	2	6	3	51 Ω to V_{TT}
A_{OUT}	3	7	4	51 Ω to V_{TT}
$\overline{A_{IN}}$	4	8	5	GND
A_{IN}	5	9	7	V_{BB}
$\overline{B_{OUT}}$	6	10	8	51 Ω to V_{TT}
B_{OUT}	7	11	9	51 Ω to V_{TT}
V_{EE}	8	12	10	V_{EE}
$\overline{B_{IN}}$	9	13	12	GND
B_{IN}	10	14	13	V_{BB}
V_{BB}	11	15	14	V_{BB}
$\overline{C_{IN}}$	12	16	15	GND
C_{IN}	13	1	17	V_{BB}
$\overline{C_{OUT}}$	14	2	18	51 Ω to V_{TT}
C_{OUT}	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

NOTES:
1. **V_{BB} to be used to supply bias to the 10616 only and bypassed (when used) with 0.01 μF to 0.1 μF capacitor.**
2. **When the input pin with the bubble goes positive, the output goes posittive.**

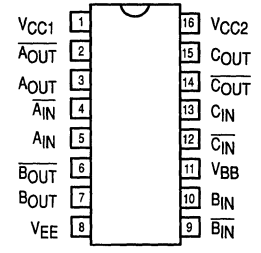
Military 10616

AVAILABLE AS:

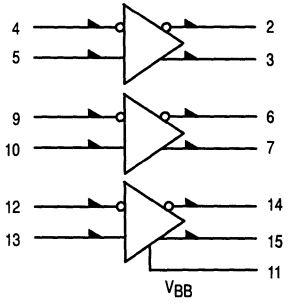
1) JAN: N/A
2) SMD: N/A
3) 883: 10616/BXAJC
X = CASE OUTLINE AS FOLLOWS:

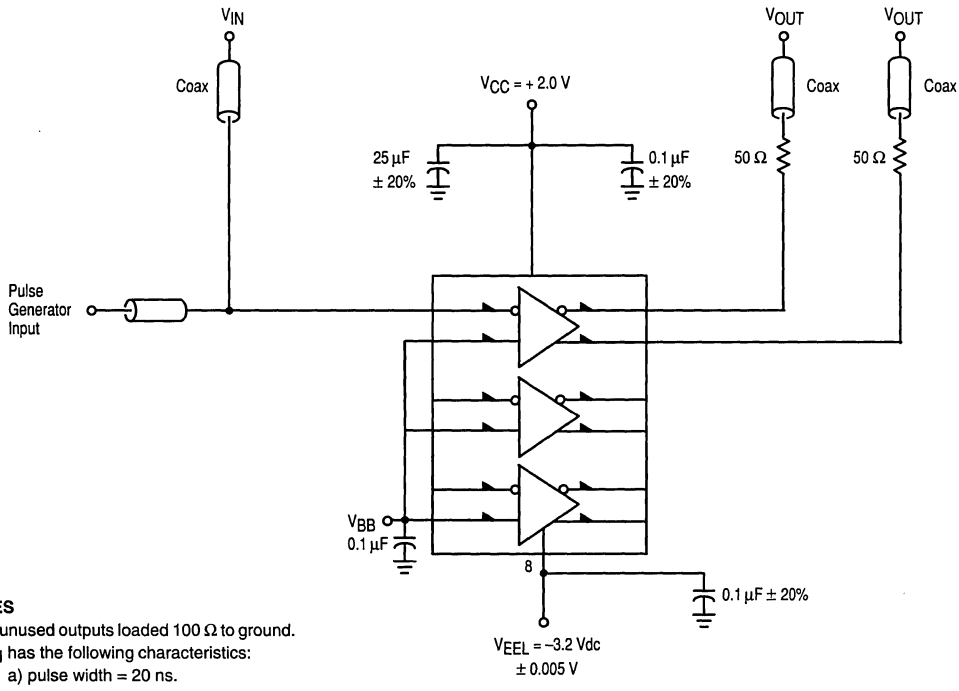
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM





NOTES

1. All unused outputs loaded 100 Ω to ground.
2. V_{IN} has the following characteristics:
   a) pulse width = 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and t_f = 1.5 ns ± 0.2 ns.

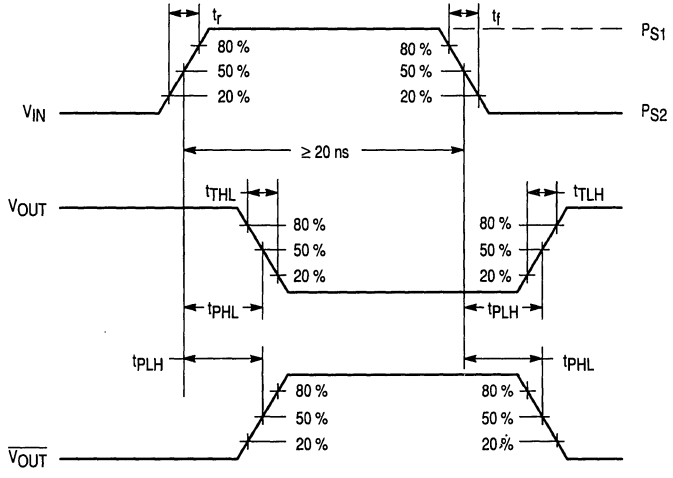


Figure 1. Switching Test Circuit and Waveforms

10616
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{CB}/V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{BB} to pin 11, V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{BB}	V_{CB}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4, 5, 9, 12, 13	4, 5, 9, 12, 13					8	1, 16	2, 3, 6, 7, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4, 5, 9, 12, 13	4, 5, 9, 12, 13					8	1, 16	2, 3, 6, 7, 14, 15
V_{OL1}	Low Output Voltage		- 1.60		- 1.525		- 1.635	V			4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13	4, 9, 13, 14		8	1, 16	2, 3, 6, 7, 14, 15
V_{OH1}	High Output Voltage	- 0.95		- 0.845		- 1.10		V			4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13	4, 9, 13, 14		8	1, 16	2, 3, 6, 7, 14, 15
V_{BB}	Reference Bias Supply Voltage	- 1.35	- 1.23	- 1.24	- 1.12	- 1.44	- 1.32	V	4, 9, 12	5, 10, 13					8	1, 16	11
I_{CBO}	Open Collector Input Current	- 1.0		- 1.0		- 1.5		μA	4, 7, 9, 12, 14					5, 10, 13	8	1, 16	4, 5, 9, 10, 12, 13
I_{IH}	Input Current High		115		195		195	μA	4, 5, 9, 10, 12, 13	4, 5, 9, 10, 12, 13					8	1, 16	4, 5, 9, 10, 12, 13
I_{EE}	Power Supply Drain Current	- 25		- 28		- 28		mA		5, 10, 13					8	1, 16	8

10616
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{CB}/V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{BB}	V_{CC}	V_{EEL}	P. U. T.
t_{TLH}	Rise Time	1.0	2.5	1.0	2.9	1.0	2.7	ns	4, 9, 12	2, 14	5, 10, 13	1, 16	8	2, 3, 6, 7, 14, 15
t_{THL}	Fall Time	1.0	2.5	1.0	2.9	1.0	2.7	ns	4, 9, 12	2, 14	5, 10, 13	1, 16	8	2, 3, 6, 7, 14, 15
t_{PHL}	Propagation Delay	1.0	2.5	1.0	2.9	1.0	2.7	ns	4, 9, 12	2, 14	5, 10, 13	1, 16	8	2, 3, 6, 7, 14, 15
t_{PLH}	Propagation Delay	1.0	2.5	1.0	2.9	1.0	2.7	ns	4, 9, 12	2, 14	5, 10, 13	1, 16	8	2, 3, 6, 7, 14, 15

High Speed Dual D Type Master Slave Flip-Flop

ELECTRICALLY TESTED PER:
MIL-M-38510/06102

The 10631 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\overline{C_E}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

- 375 mW Max/Pkg (No Load)
- f_{Tog} = 225 MHz typ
- t_{pd} = 2.0 ns typ (All Output Loaded)
- t_r, t_f = 2.0 ns typ (20% - 80%)

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω to V_{TT}
$\overline{Q_1}$	3	7	4	51 Ω to V_{TT}
R_1	4	8	5	51 Ω to V_{TT}
S_1	5	9	7	GND
$\overline{C_{E1}}$	6	10	8	OPEN
D_1	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
C_C	9	13	12	OPEN
D_2	10	14	13	OPEN
$\overline{C_{E2}}$	11	15	14	OPEN
S_2	12	16	15	GND
R_2	13	1	17	51 Ω to V_{TT}
$\overline{Q_2}$	14	2	18	51 Ω to V_{TT}
Q_2	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

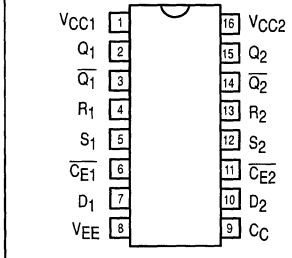
Military 10631

AVAILABLE AS:

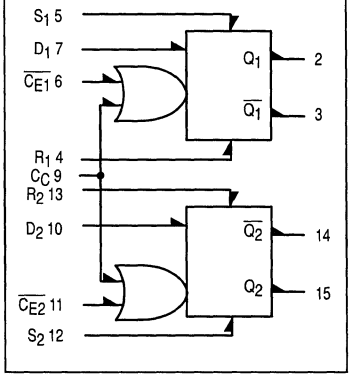
1) JAN: JM 38510/06102
2) SMD: N/A
3) 883: 10631/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



R-S TRUTH TABLE

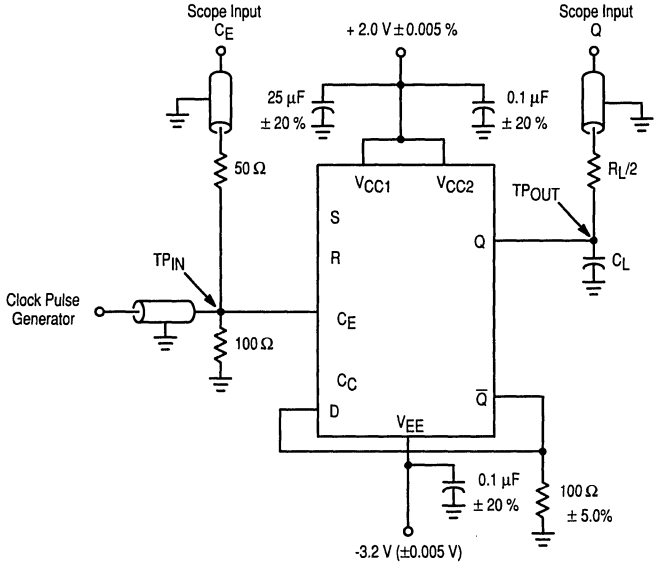
R	S	$Q_n + 1$
L	L	Q_n
L	H	H
H	L	L
H	H	N. D.

N.D. = Not Defined
A clock H is a clock transition from a Low to a High state

CLOCKED TRUTH TABLE

C	D	$Q_n + 1$
L	∅	Q_n
H	L	L
H	H	H

∅ = Don't Care
$C = C_E + C_C$



NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2 = 50\ \Omega \pm 5.0\%$.
6. $t_r = t_f = 2.0$ ns (20% - 80%).
7. Scope Input = 50 Ω GND.
8. C_L (test Jig) ≤ 5.0 pF.

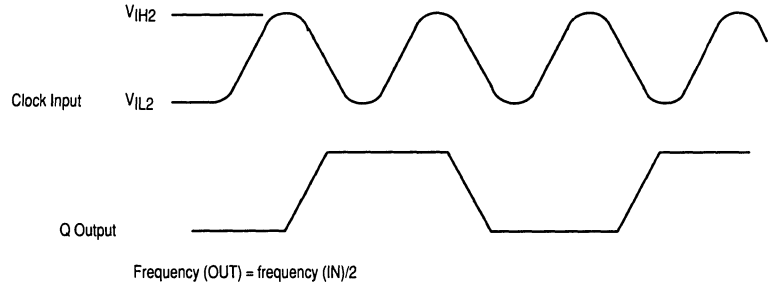
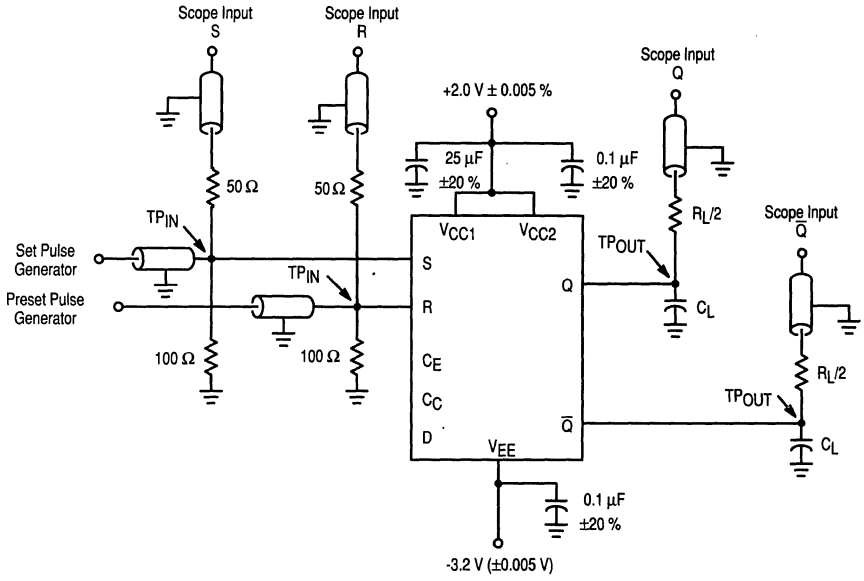
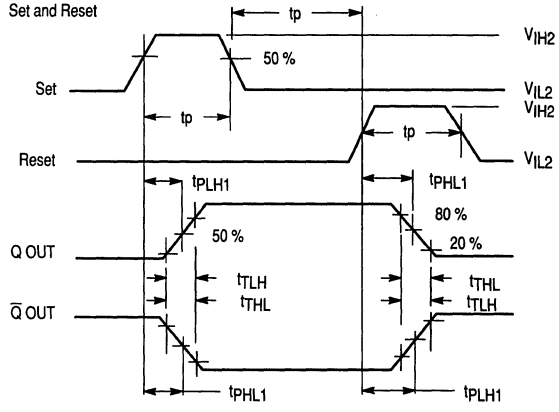


Figure 1. F_{MAX} Test Circuit and Clock Input Sinewave

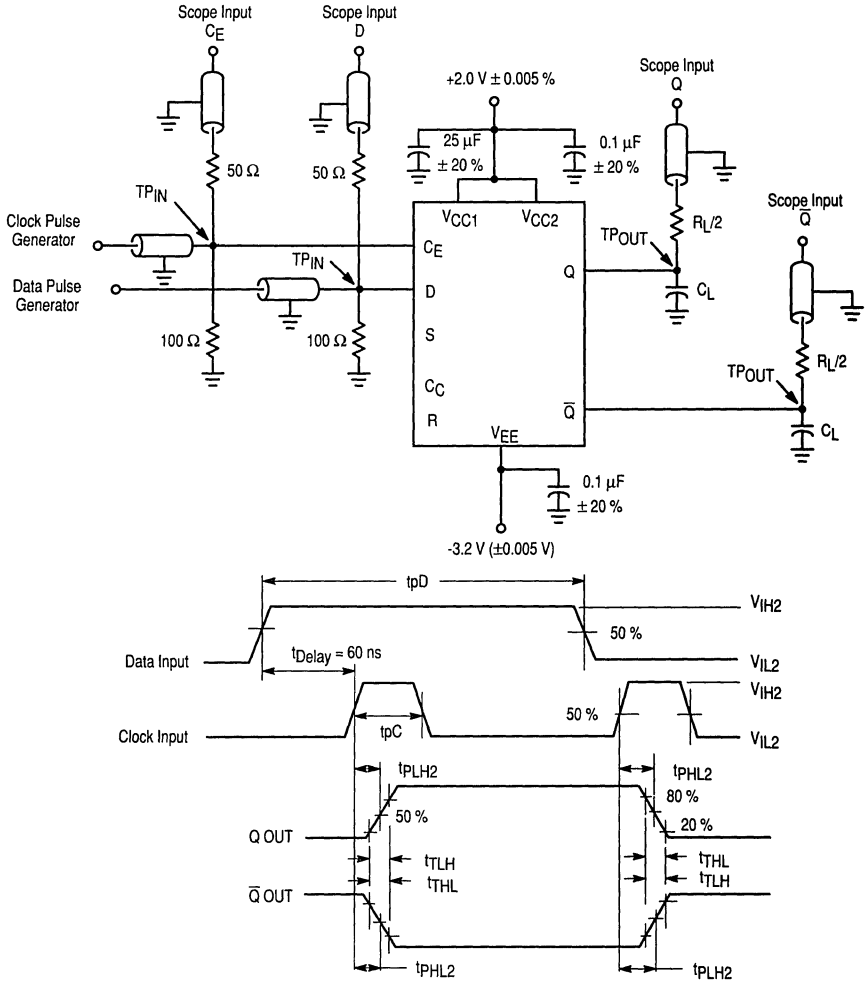




NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2 = 50\ \Omega \pm 5.0\%$.
6. $Z_{OUT} = 50\ \Omega$.
7. t_{REC} (Set & Reset) = 40 ns.
8. PRR = 1.0 MHz.
9. Scope Input = 50 Ω to GND.
10. C_L (test Jig) ≤ 5.0 pF.

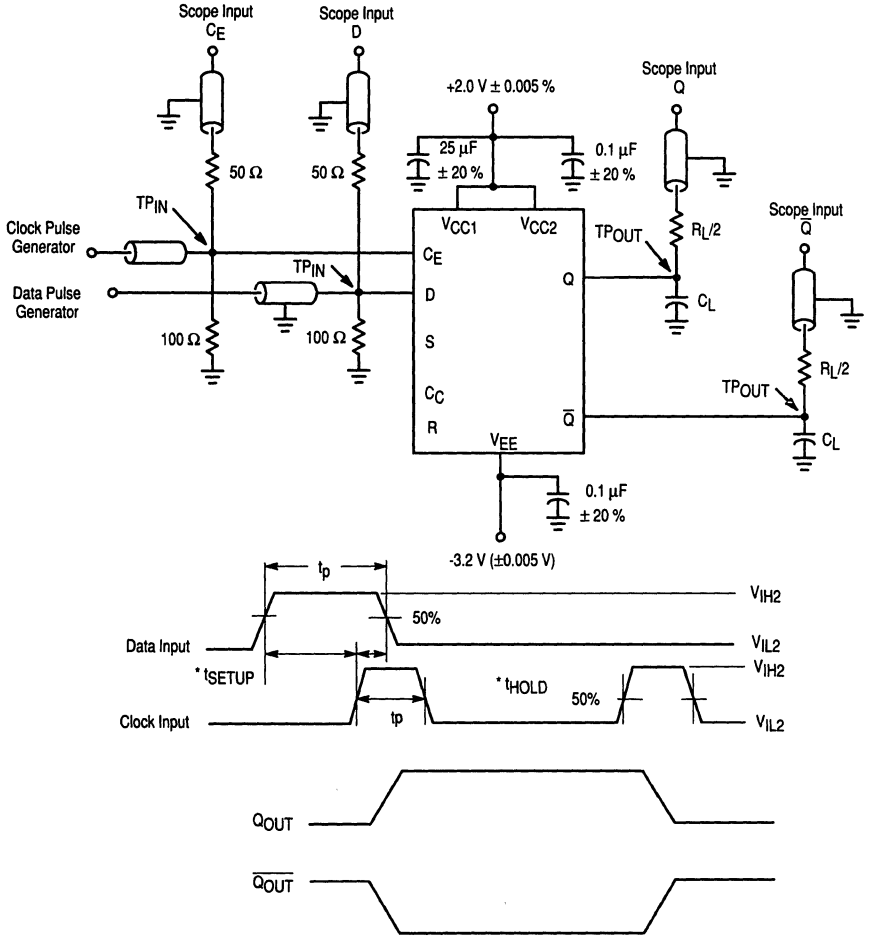
Figure 2. Set and Reset Switching Test Circuit



NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.35 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. Z_{OUT} = 50 Ω.
7. t_{pD}(Data) = 150 ns, t_{pC} (Clock) = 40 ns.
8. PRR = 1.0 MHz.
9. Scope Input = 50 Ω to GND.
10. C_L (test Jig) ≤ 5.0 pF.

Figure 3. Synchronous Switching Test Circuit and Waveform



NOTES

1. Perform test in accordance with test table: each output is tested separately.
2. All input and output cables are equal lengths of 50 Ω coaxial cables. Wire length should be ≤ 0.250 (6.36 mm) from tp in to input pin and tp out to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.
4. Note that observed pulse amplitude is attenuated by one half.
5. $R_L/2$ = 50 Ω ± 5.0%.
6. Z_{OUT} = 50 Ω.
7. t_p(Data & Clock) = 40 ns.
8. Scope Input = 50 Ω to GND.
9. C_L (test Jig) ≤ 5.0 pF.
* 10. For information only; not tested: t_{setup} ≥ 1.0 ns, t_{hold} ≥ 0.75 ns.

Figure 4. Setup and Hold Test Circuit and Waveform

10631
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{EE}	V_{EE1}
T_A = 25 °C	- 0.78	- 1.85	+ 1.11	+ 0.31	- 1.105	- 1.475	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	+ 1.24	+ 0.36	- 1.000	- 1.400	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	+ 1.01	+ 0.28	- 1.255	- 1.510	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	4, 5, 12, 13	4 - 7 9 - 13			8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	4, 5, 12, 13	4 - 7 9 - 13			8	1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	- 0.95		- 0.845		- 1.10		V	4, 5, 12, 13	4 - 7 9 - 13	4 - 7 9 - 13	4 - 7 9 - 13	8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage		- 1.60		- 1.525		- 1.635	V	4, 5, 12, 13	4 - 7 9 - 13	4 - 7 9 - 13	4 - 7 9 - 13	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Drain Current	- 65		- 72		- 72		mA					8	1, 16	8
I_{IH}	Input Current High		220		375		375	µA	6, 11				8	1, 16	6, 11
I_{IH1}	Input Current High		410		700		700	µA	4, 5, 12, 13				8	1, 16	4, 5, 12, 13
I_{IH2}	Input Current High		220		375		375	µA	7, 10				8	1, 16	7, 10
I_{IH3}	Input Current High		290		495		495	µA	9				8	1, 16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7 9 - 13			8	1, 16	4 - 7, 9 - 13

10631
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{ITL}	V_{ITH}	V_{EE}	V_{EE1}
T_A = 25 °C	- 0.78	- 1.85	+ 1.11	+ 0.31	- 1.105	- 1.475	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	+ 1.24	+ 0.36	- 1.000	- 1.400	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	+ 1.01	+ 0.28	- 1.255	- 1.510	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE1}	P. U. T.
t_{TLH}	Rise Time	1.0	3.1	1.1	3.6	0.9	3.4	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 6	8	2, 3, 14, 15
t_{THL}	Fall Time	1.0	3.1	1.1	3.6	0.9	3.4	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 6	8	2, 3, 14, 15
t_{PLH1}	Propagation Delay	1.1	3.3	1.0	3.9	1.0	3.7	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH2}	Propagation Delay	1.5	3.3	1.2	3.9	1.3	3.7	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL1}	Propagation Delay	1.1	3.3	1.0	3.9	1.0	3.7	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PHL2}	Propagation Delay	1.5	3.3	1.2	3.9	1.3	3.7	ns	4 - 7, 10 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
$f_{(max)}$	Toggle Frequency (max)	200		200		200		MHz	6, 11	2, 15	1, 16	8	2, 3, 14, 15

MOTOROLA

High Speed 2 x 1 Bit Array Multiplier Block

ELECTRICALLY TESTED PER:
MPG 10687

The 10687 is a dual high speed interactive multiplier. It is designed for use as an array multiplier block. Each device is a modified full adder/subtractor that forms a single-bit binary product at each operand input of the adder. Internal carry lookahead is employed for high speed operation.

An addition or subtraction is selected by mode controls (M_0, M_1). The mode controls are buffered such that they can be grounded or taken to a standard high logic level to accomplish subtraction. When left open or taken to a low logic level, M_0 and M_1 cause addition.

- 555 mW Max/Pkg (No Load)
- t_{pd} : (Outputs Loaded 1.0 kΩ to V_{EE})
  C_0 to C_2 = 1.7 ns typ
  a_0 to C_2 = 2.8 ns
  a_0 to S_0 = 2.7 ns
  b_0 to S_0 = 3.1 ns
  a_0 to S_1 = 3.9 ns
  b_0 to S_1 = 4.4 ns
  M_0 to S_1 = 8.7 ns

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
S_1	1	5	2	51 Ω to V_{TT}
S_0	2	6	3	51 Ω to V_{TT}
M_0	3	7	4	OPEN
b_0	4	8	5	GND
$\overline{b_0}$	5	9	7	OPEN
a_0	6	10	8	GND
$\overline{a_0}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
C_0	9	13	12	GND
$\overline{a_1}$	10	14	13	OPEN
a_1	11	15	14	GND
$\overline{b_1}$	12	16	15	OPEN
b_1	13	1	17	GND
M_1	14	2	18	51 Ω to V_{TT}
C_2	15	3	19	51 Ω to V_{TT}
V_{CC}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

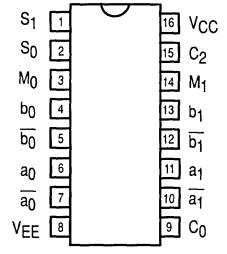
Military 10687

AVAILABLE AS:

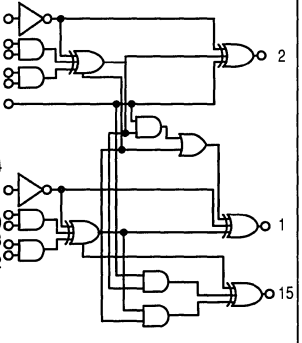
1) JAN: N/A
2) SMD: N/A
3) 883: 10687/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.



LOGIC DIAGRAM



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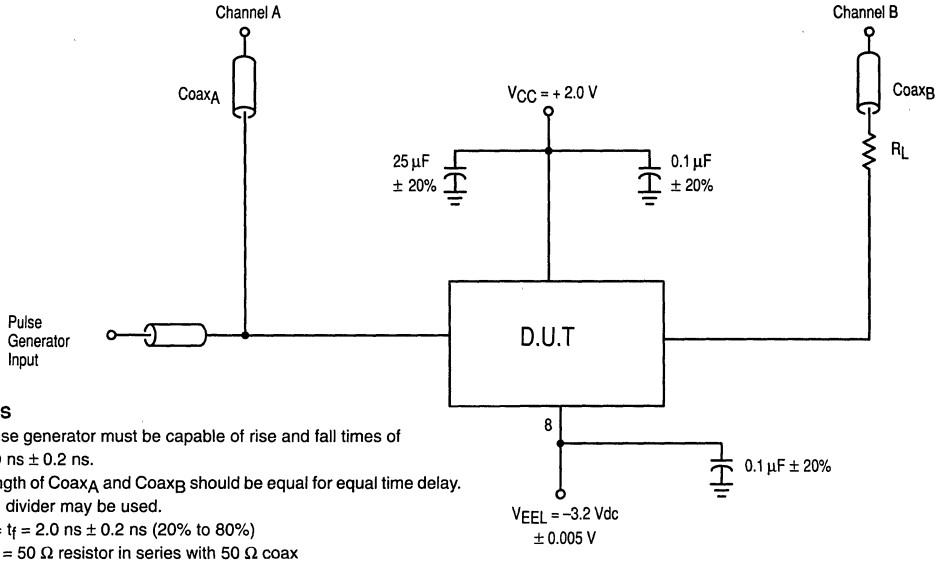


NOTES

1. Pulse generator must be capable of rise and fall times of 2.0 ns ± 0.2 ns.
2. Length of $Coax_A$ and $Coax_B$ should be equal for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0$ ns ± 0.2 ns (20% to 80%)
5. $R_L = 50\ \Omega$ resistor in series with 50 Ω coax constituting the 100 Ω load.
6. V_{IN} has the following characteristics:
   a) pulse width ≥ 20 ns.
   b) frequency = 1.0 MHz.
   c) t_r and $t_f = 2.0$ ns ± 0.2 ns.
7. Unused outputs should be loaded 100 Ω to ground.

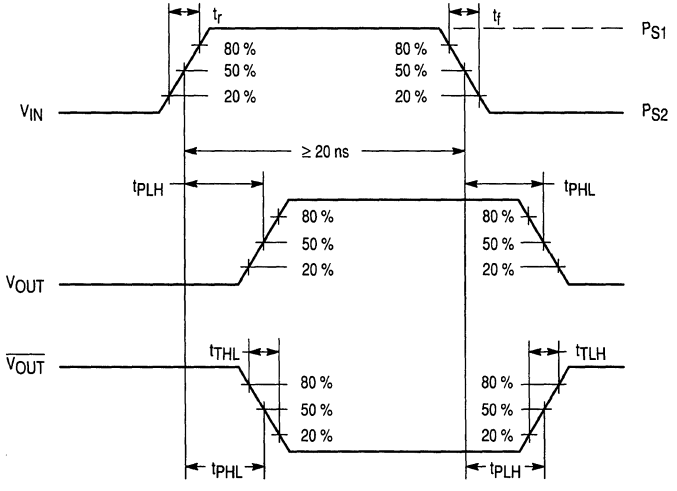


Figure 1. Switching Test Circuit and Waveforms

10687
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	V_{EE}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	5, 6, 9, 10				8	16	1, 2, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V					8	16	1, 2, 15
V_{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V	6, 7, 9 - 11			4 - 7 9 - 14	8	16	1, 2, 15
V_{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V	6, 7, 9 - 11		4 - 7 9 - 13		8	16	1, 2, 15
I_{IH1}	Input Current High		200		340		340	µA	3, 14				8	16	3, 14
I_{IH2}	Input Current High		220		375		375	µA	4, 5, 12, 13				8	16	4, 5, 12, 13
I_{IH3}	Input Current High		265		450		450	µA	6, 7, 10, 11				8	16	6, 7, 10, 11
I_{IH4}	Input Current High		410		700		700	µA	9				8	16	9
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		3 - 7 9 - 14			8	16	3 - 7 9 - 14
I_{EE}	Power Supply Drain Current	- 96		- 106		- 106		mA					8	16	8

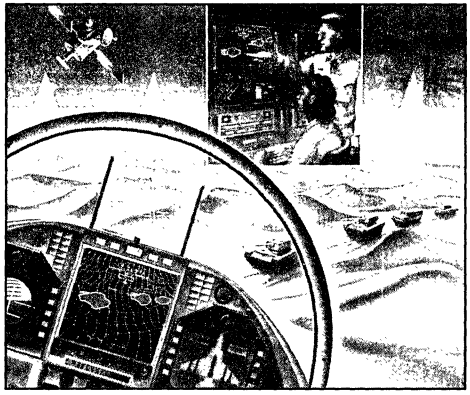
10687
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V_{IH}	V_{IL}	V_{IH1}	V_{IL1}	P_{S1}	P_{S2}	V_{EE}	V_{EEL}
T_A = 25 °C	- 0.78	- 1.85	- 1.105	- 1.475	+ 1.11	+ 0.31	- 5.2	- 3.2
T_A = 125 °C	- 0.63	- 1.82	- 1.000	- 1.400	+ 1.24	+ 0.36	- 5.2	- 3.2
T_A = - 55 °C	- 0.88	- 1.92	- 1.255	- 1.510	+ 1.01	+ 0.28	- 5.2	- 3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P_{S1}	P_{S2}	P. U. T.
t_{TLH}	Rise Time	1.1	3.1	1.0	3.6	1.1	3.4	ns	3 - 7, 9 - 14	1, 2, 15	1, 16	8	3 - 7, 9 - 14	3 - 7, 9 - 14	1, 2, 15
t_{THL}	Fall Time	1.1	3.1	1.0	3.6	1.1	3.4	ns	3 - 7, 9 - 14	1, 2, 15	1, 16	8	3 - 7, 9 - 14	3 - 7, 9 - 14	1, 2, 15
t_{PHL} / t_{PLH}	Propagation Delay C_0 to C_2 or S_0	1.1	3.4	1.1	4.2	1.1	4.0	ns	3 - 7, 9 - 14	1, 2, 15	1, 16	8	3 - 7, 9 - 14	3 - 7, 9 - 14	1, 2, 15
	C_0 to S_1	1.1	4.5	1.1	4.9	1.1	4.9	ns							
t_{PHL} / t_{PLH}	Propagation Delay A_0 to C_2 or S_0	1.1	4.7	1.1	7.0	1.1	5.0	ns	3 - 7, 9 - 14	1, 2, 15	1, 16	8	3 - 7, 9 - 14	3 - 7, 9 - 14	1, 2, 15
	A_0 to S_1	1.4	5.8	2.0	6.6	2.0	6.2	ns							
t_{PHL} / t_{PLH}	Propagation Delay B_0 to C_2 or S_0	1.1	4.7	1.1	7.0	1.1	5.0	ns	3 - 7, 9 - 14	1, 2, 15	1, 16	8	3 - 7, 9 - 14	3 - 7, 9 - 14	1, 2, 15
	B_0 to S_1	1.4	5.8	2.0	6.6	2.0	6.2	ns							
t_{PHL} / t_{PLH}	Propagation Delay A_1 or B_1 to S_1 or C_2	1.1	4.5	1.5	5.2	1.1	4.5	ns	3 - 7, 9 - 14	1, 2, 15	1, 16	8	3 - 7, 9 - 14	3 - 7, 9 - 14	1, 2, 15
t_{PHL} / t_{PLH}	Propagation Delay M_0 to S_1 or M_1 to C_2	3.0	12.5	3.0	14.5	3.0	14	ns	3 - 7, 9 - 14	1, 2, 15	1, 16	8	3 - 7, 9 - 14	3 - 7, 9 - 14	1, 2, 15
	M_0 to C_2	3.0	12.5	2.5	14.5	2.5	14	ns							



MECL III

4

Military 1648M

Voltage Controlled Oscillator

ELECTRICALLY TESTED PER:
MPG 1648M

The 1648M requires an external parallel tank circuit consisting of the inductor (L) capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). This device may be used in many applications requiring a fixed or variable frequency clock source of the high spectral purity. (See Test Circuit).

The 1648M may be operated from a + 5.0 Vdc supply or a – 5.2 Vdc supply, depending upon system requirements.

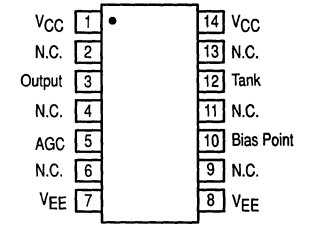
ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage (V_{CC} = 0)	V_{CC}	– 8.0	0	Vdc
Input Voltage @ (V_{EE} = – 5.2 Vdc)	V_{IN5} V_{IN12}	– 5.2 0	– 3.4 V_{EE}	Vdc Vdc
Output Source Current	I_O		< 40	mAdc
Storage Temperature Range	T_{stg}	– 55	+ 125	°C
Operating Temperature Range	T_A	– 55	+ 125	°C

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 1648M/BXAJC
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: C
CERFLAT: D
LCC: 2

The letter "M" appears before the slash on LCC.

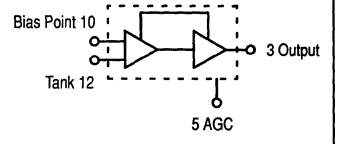


PIN ASSIGNMENTS

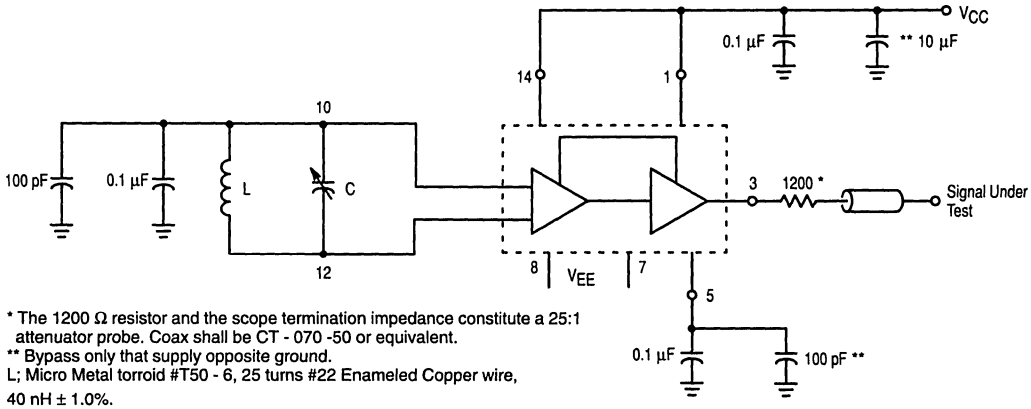
FUNCTION	DIL Case 692	FLATS Case 717	LCC Case 756A	BURN-IN (CONDITION C)
V_{CC}	1	1	2	GND
N.C.	2	2	3	OPEN
Output	3	3	4	51 Ω to V_{TT}
N.C.	4	4	6	OPEN
AGC	5	5	8	OPEN
N.C.	6	6	9	OPEN
V_{EE}	7	7	10	V_{EE}
V_{EE}	8	8	12	V_{EE}
N.C.	9	9	13	OPEN
Bias Point	10	10	14	OPEN
N.C.	11	11	16	OPEN
Tank	12	12	18	51 Ω to V_{TT}
N.C.	13	13	19	OPEN
V_{CC}	14	14	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

LOGIC DIAGRAM



Input Capacitance = 6.0 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 215 mW typ/pkg (+ 5.0 Vdc supply)
Maximum Output Frequency = 225 MHz typ



* The 1200 Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT - 070 -50 or equivalent.
** Bypass only that supply opposite ground.
L; Micro Metal torroid #T50 - 6, 25 turns #22 Enameled Copper wire, 40 nH ± 1.0%.
C = 10.0 pF ± 1.0%.

Figure 1. Test Circuit

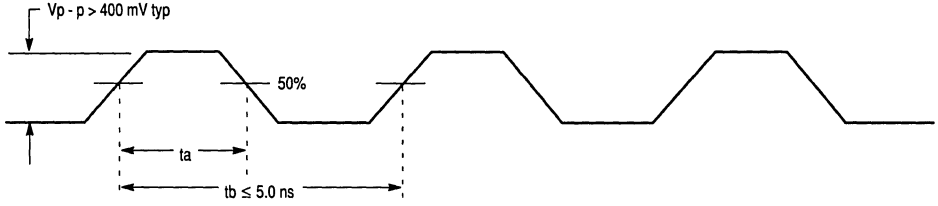


Figure 2. Test Circuit Waveforms

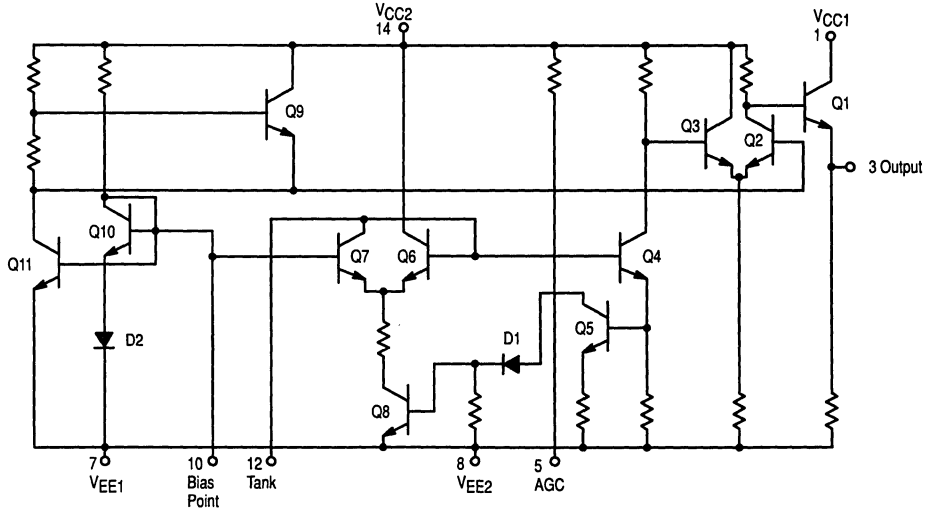


Figure 3. Circuit Schematic

1648M
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						Test Current Values (mA)
	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{EE}	V_{CC}	I_L
T_A = 25 °C	-3.35	-3.85	+1.85	+1.35	-5.2	+5.0	-5.0
T_A = 125 °C	-3.60	-4.10	+1.60	+1.10	-5.2	+5.0	-5.0
T_A = -55 °C	-3.13	-3.63	+2.07	+1.57	-5.2	+5.0	-5.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{CC}	V_{EE}	I_L	GND	P.U.T.
V_{THA}	High Internal Threshold Voltage	- 3.75	- 3.45	- 4.0	- 3.7	- 3.53	- 3.23	V		12				7, 8		1, 14	5, 10
V_{OHA}	High Output Voltage	- 0.96	- 0.75	- 0.84	- 0.60	- 1.08	- 0.87	V		12				7, 8	3	1, 14	3
V_{OLA}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.54	- 1.92	- 1.67	V	12					7, 8	3	1, 14	3
V_{THB}	High Internal Threshold Voltage	1.45	1.75	1.2	1.5	1.67	1.97	V				12	1, 14			7, 8	5, 10
V_{OHB}	High Output Voltage	4.04	4.25	4.16	4.4	3.92	4.13	V				12	1, 14		3	7, 8	3
V_{OLB}	Low Output Voltage	3.2	3.43	3.23	3.51	3.13	3.38	V			12		1, 14		3	7, 8	3
I_{CC}	Power Supply Current Off		40					mA								7, 8	1, 14
I_{EE}	Power Supply Drain Current	- 41						mA						7, 8		1, 14	7, 8

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW	
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND	
		Subgroup 9		Subgroup 10		Subgroup 11				
		Min	Max	Min	Max	Min	Max		V_{CC}	GND
* f_{Max}	Oscillation Frequency	200		200		190		MHz	1, 14	7, 8

* Frequency variations over temperature is a direct function of the ΔC/Δ Temperature and ΔL/Δ Temperature.

MOTOROLA

Dual A/D Converter

Military 1650

ELECTRICALLY TESTED PER:
MPG 1650 (– 30°C to + 85°C)

The 1650 is a very high speed comparator utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The 1650 provides high impedance Darlington inputs, while the 1651 is a lower impedance option, with higher input slew rate and higher speed capability.

The clock inputs ($\overline{C_a}$ and $\overline{C_b}$) operate from MECL III or MECL 10,000 digital levels. When $\overline{C_a}$ is at a logic high level, Q_0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q_0}$ is the logic complement of Q_0. When the clock input goes to a low logic level, the outputs are latched in their present state.

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ
- Input Slew Rate = 350 V/µs
- Differential Input Voltage Range: 5.0 V (– 30°C to 85°C)
- Common Mode Range: – 2.5 V to + 3.0 V (– 30°C to 85°C)
- Resolution: ≤ 20 mV (– 30°C to 85°C)
- Drives 50 Ω lines

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1650/BXA *
X = CASE OUTLINE AS FOLLOWS:

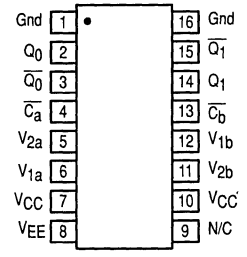
PACKAGE: CERDIP: E
CERFLAT: F

*** 883 Processing (Non-Compliant)**

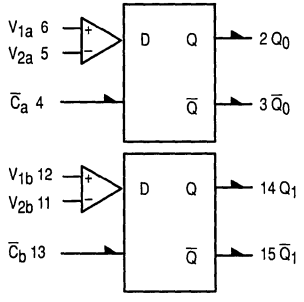
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
GND	1	5	GND
Q_0	2	6	51 Ω to V_{TT}
$\overline{Q_0}$	3	7	51 Ω to V_{TT}
$\overline{C_a}$	4	8	GND
V_{2a}	5	9	V_{TT}
V_{1a}	6	10	GND
V_{CC}	7	11	V_{CC}
V_{EE}	8	12	V_{EE}
N.C.	9	13	OPEN
V_{CC}	10	14	V_{CC}
V_{2b}	11	15	V_{TT}
V_{1b}	12	16	GND
$\overline{C_b}$	13	1	GND
Q_1	14	2	51 Ω to V_{TT}
$\overline{Q_1}$	15	3	51 Ω to V_{TT}
GND	16	4	GND

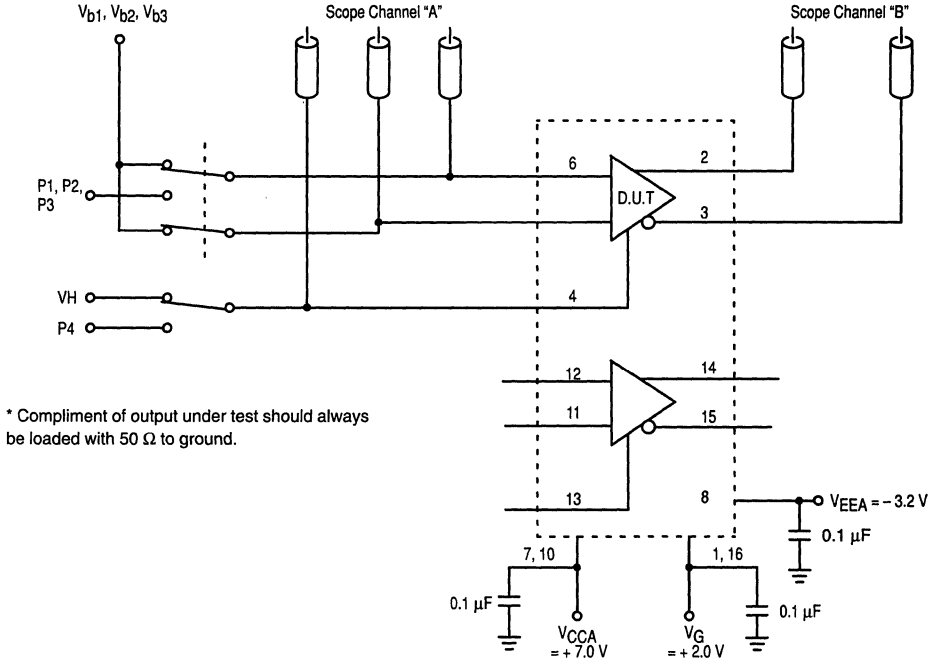
BURN - IN CONDITIONS:
V_{TT} = – 1.8 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 4.7 V MIN
V_{CC} = + 5.0 V MAX/ + 4.5 V MIN



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC} V_{EE}		+ 6.0 – 6.0	Vdc Vdc
Analog Input Voltage	V_{IN}		– 3.0 to + 3.0	Vdc
Gate Input Voltage	V_{IN}		0 to V_{EE}	Vdc
Storage Temperature Range	T_{stg}	– 55	+ 125	°C
Operating Temperature Range	T_A	– 30	+ 85	°C



* Compliment of output under test should always be loaded with 50 Ω to ground.

Figure 1. Circuit Schematic

TRUTH TABLE			
$\overline{C}$	V_1, V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q0}_n$

ϕ = Don't Care

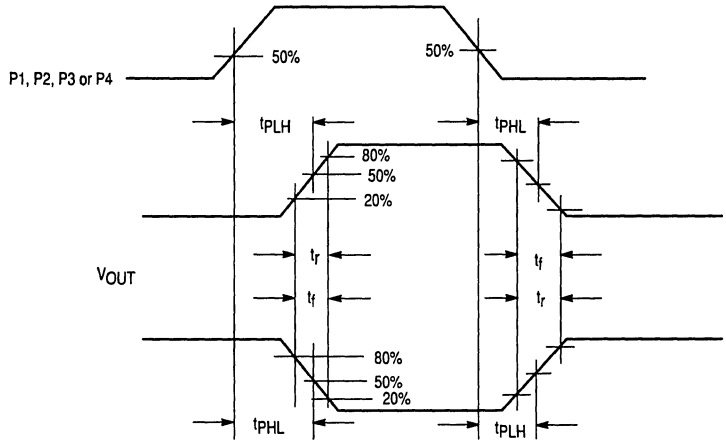
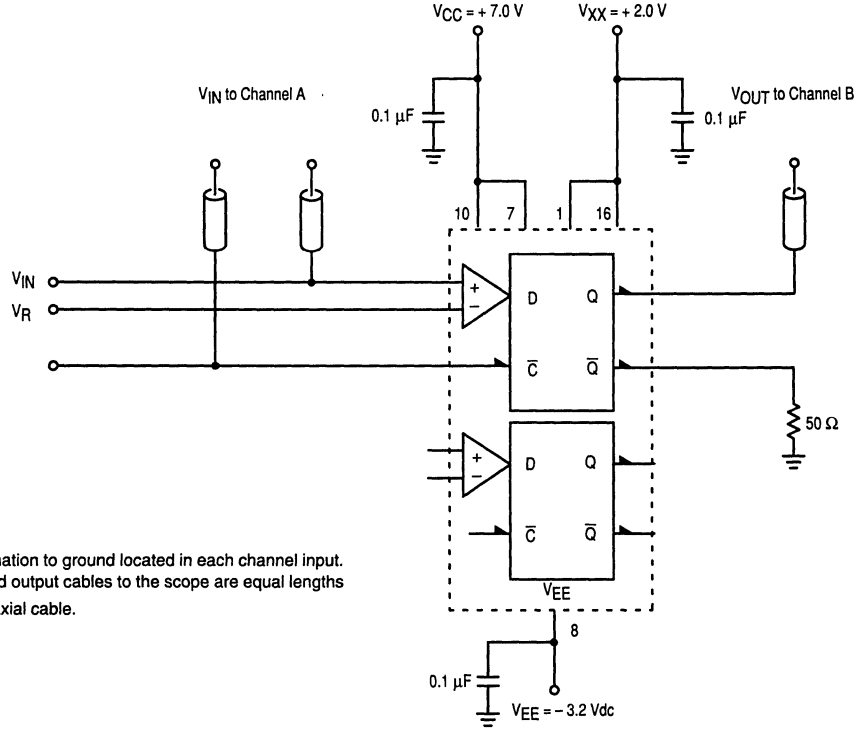


Figure 2. Test Circuit Waveforms



50 Ω termination to ground located in each channel input. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

Figure 3. Clock Enable Time Test Circuit

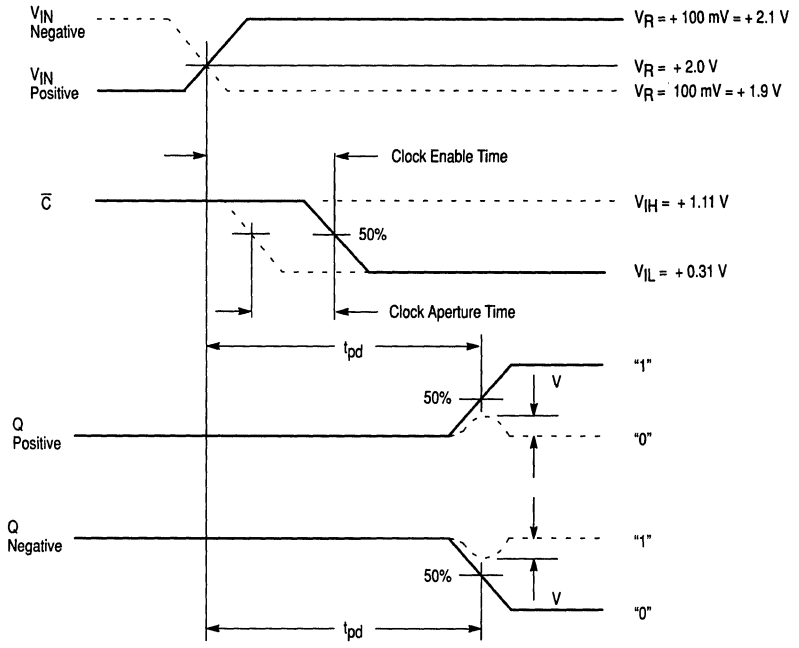


Figure 4. Analog Signal Positive and Negative Skew Case

Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 500 ps.

Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

NOTE: All power supply and logic levels are shown shifted 2.0 volts positive.

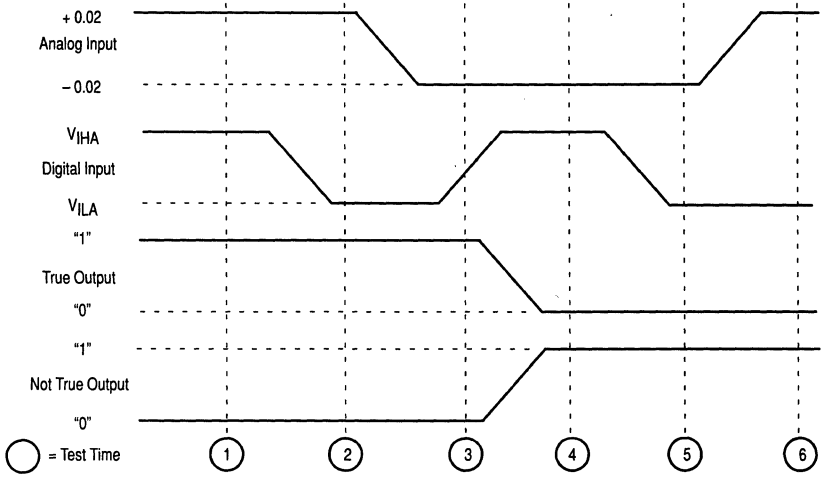


Figure 5. Threshold Pulse Diagram

1650
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)											
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{CC}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	+5.0	+0.02	-0.02	+3.0	+2.98	-2.5	-2.48
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	+5.0	+0.02	-0.02	+3.0	+2.98	-2.5	-2.48
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	+5.0	+0.02	-0.02	+3.0	+2.98	-2.5	-2.48

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to - 2.0 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EE}	V_{A1-6}	GND	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V	4, 13				7, 10	8	5, 6, 11, 12	1, 5, 6, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V	4, 13				7, 10	8	5, 6, 11, 12	1, 5, 6, 16	2, 3, 14, 15
V_{OHA}	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V		4, 6, 12, 13	4, 13	4, 13	7, 10	8	6, 12	1, 5, 6, 16	2, 3, 14, 15
V_{OLA}	Low Output Voltage	- 1.85	- 1.6	- 1.83	- 1.555	- 1.89	- 1.63	V		4, 6, 12, 13	4, 13	4, 13	7, 10	8	6, 12	1, 5, 6, 16	2, 3, 14, 15
I_{IN}	Input Current		10					µA	4, 13	4, 13			7, 10	8	5, 6, 11, 12	1, 5, 6, 11, 12, 16	5, 6, 11, 12
I_{INH}	Input Current High		350					µA	4, 13	4, 13			7, 10	8	5, 11	1, 6, 12, 16	4, 13
I_L	Leakage Current	- 7.0						µA	4, 13	4, 13			7, 10	8	5, 6, 11, 12	1, 5, 6, 11, 12, 16	5, 6, 11, 12

1650
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)											
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{CC}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	+5.0	+0.02	-0.02	+3.0	+2.98	-2.5	-2.48
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	+5.0	+0.02	-0.02	+3.0	+2.98	-2.5	-2.48
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	+5.0	+0.02	-0.02	+3.0	+2.98	-2.5	-2.48

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{CC}	V_{EE}	V_{A1-6}	GND	P.U.T.
I_{INL}	Leakage Current Low	0.5						µA	4, 13	4, 13	7, 10	8	5, 11	1, 6, 12, 16	4, 13
I_{EE}	Power Supply Drain Current	- 55						mA	4, 13		7, 10	8	6, 12	1, 5, 11, 16	8
* I_{CC}	Power Supply Drain Off		+25					mA		4, 13	7, 10	8	6, 12	1, 5, 11, 16	7, 10

* I_{CC} = Total current to pin 7 and 10 tied together.

1650
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)							Test Parameter	Test Voltage Values (Volts)		
	V_H	V_G	V_{B1}	V_{B2}	V_{B3}	V_{CCA}	V_{EEA}		P_1	P_2	P_3
T_A = 25 °C	+1.11	+2.0	-0.4	+2.0	+4.9	+7.0	-3.2	V_{IH}	+2.10	+5.0	-0.30
T_A = 85 °C	+1.19	+2.0	-0.4	+2.0	+4.9	+7.0	-3.2	V_R	+2.0	+4.9	-0.40
T_A = -30 °C	+1.04	+2.0	-0.4	+2.0	+4.9	+7.0	-3.2	V_{IL}	+1.9	+4.8	-0.50

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C Subgroup 9		+ 85 °C Subgroup 10		- 30 °C Subgroup 11			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND								
		Min	Max	Min	Max	Min	Max		V_H	V_G	V_{B1}	V_{B2}	V_{B3}	V_{CCA}	V_{EEA}	P_{1-3}	P.U.T./V_{OUT}
t_{TLH}	Rise Time	1.0	3.7	1.0	3.9	1.0	3.5	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
t_{THL}	Fall Time	1.0	3.0	1.0	3.3	1.0	3.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(1)}$	Propagation Delay	2.0	5.0	2.0	5.7	2.0	5.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(1)}$	Propagation Delay	2.0	5.0	2.0	5.7	2.0	5.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(2)}$	Propagation Delay	2.0	5.2	2.0	6.2	2.0	5.2	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(2)}$	Propagation Delay	2.0	5.2	2.0	6.2	2.0	5.2	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
t_{setup}	Setup Time	2.5		2.5		2.5		ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15

Dual A/D Converter

ELECTRICALLY TESTED PER:
MPG 1651 (– 30°C to + 85°C)

The 1651 is a very high speed comparator utilizing differential inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The 1651 is a lower impedance option to the 1650, with higher input slew rate and higher speed capability.

The clock inputs ($\overline{C}_a$ and $\overline{C}_b$) operate from MECL III or MECL 10,000 digital levels. When $\overline{C}_a$ is at a logic high level, Q_0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\overline{Q}_0$ is the logic complement of Q_0. When the clock input goes to a low level, the outputs are latched in their present state.

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ
- Input Slew Rate = 500 V/μs
- Differential Input Voltage Range: 5.0 V (– 30°C to 85°C)
- Common Mode Range: – 3.0 V to + 2.5 V (– 30°C to 85°C)
- Resolution: ≤ 20 mV (– 30°C to 85°C)
- Drives 51Ω lines

4

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
GND	1	5	GND
Q_0	2	6	51 Ω to V_{TT}
$\overline{Q_0}$	3	7	51 Ω to V_{TT}
$\overline{C_a}$	4	8	GND
V_{2a}	5	9	V_{TT}
V_{1a}	6	10	GND
V_{CC}	7	11	V_{CC}
V_{EE}	8	12	V_{EE}
N.C.	9	13	OPEN
V_{CC}	10	14	V_{CC}
V_{2b}	11	15	V_{TT}
V_{1b}	12	16	GND
$\overline{C_b}$	13	1	GND
Q_1	14	2	51 Ω to V_{TT}
$\overline{Q_1}$	15	3	51 Ω to V_{TT}
GND	16	4	GND

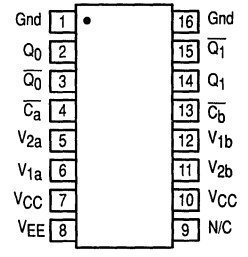
BURN - IN CONDITIONS:
V_{TT} = – 1.8 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 4.7 V MIN
V_{CC} = + 5.0 V MAX/ + 4.5 V MIN

AVAILABLE AS

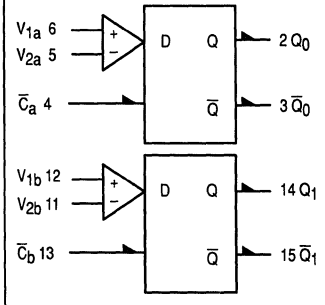
1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1651/BXA *
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F

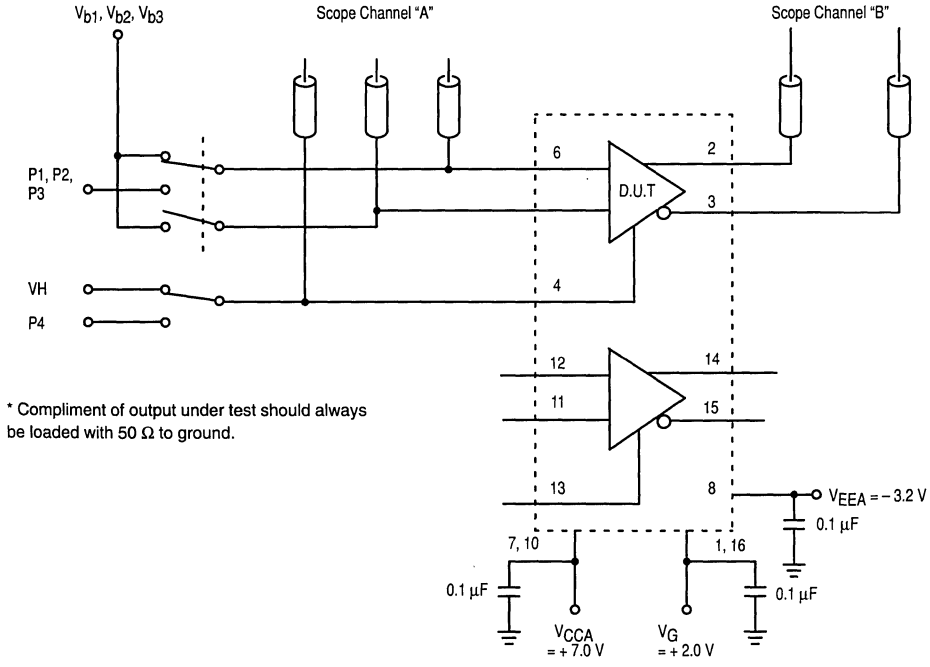
*** 883 Processing (Non-Compliant)**



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC} V_{EE}		+ 6.0 − 8.0	Vdc Vdc
Analog Input Voltage	V_{IN}		− 3.0 to + 3.0	Vdc
Gate Input Voltage	V_{IN}		0 to V_{EE}	Vdc
Storage Temperature Range	T_{stg}	− 55	+ 125	°C
Operating Temperature Range	T_A	− 30	+ 85	°C



* Compliment of output under test should always be loaded with 50 Ω to ground.

Figure 1. Circuit Schematic

TRUTH TABLE			
$\overline{C}$	V_1, V_2	$Q0_{n+1}$	$\overline{Q0}_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\overline{Q0}_n$

ϕ = Don't Care

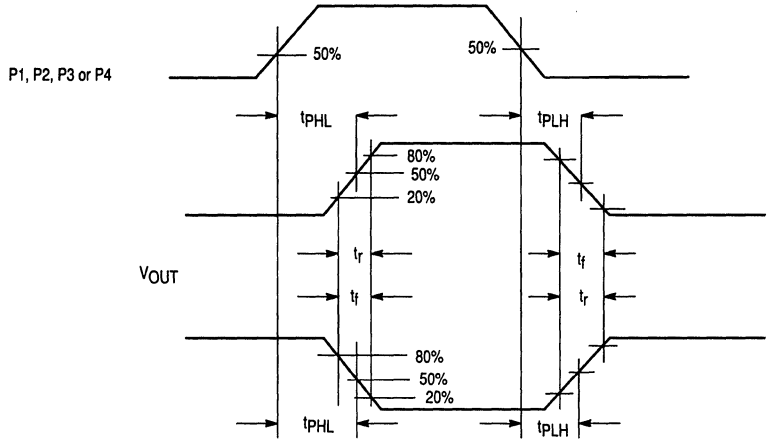
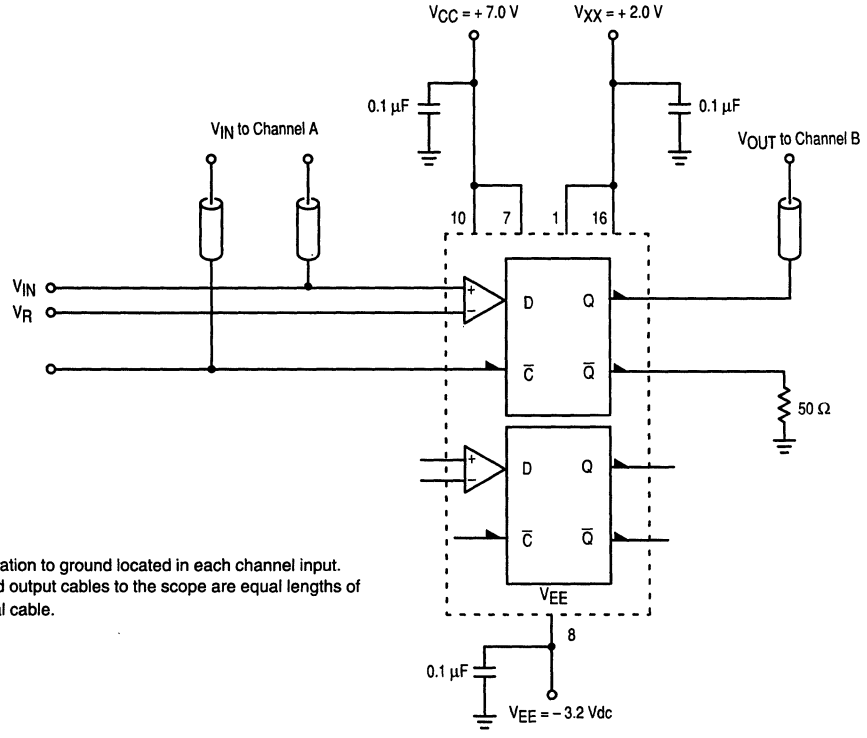


Figure 2. Test Circuit Waveforms



50 Ω termination to ground located in each channel input.
All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

Figure 3. Clock Enable Time Test Circuit

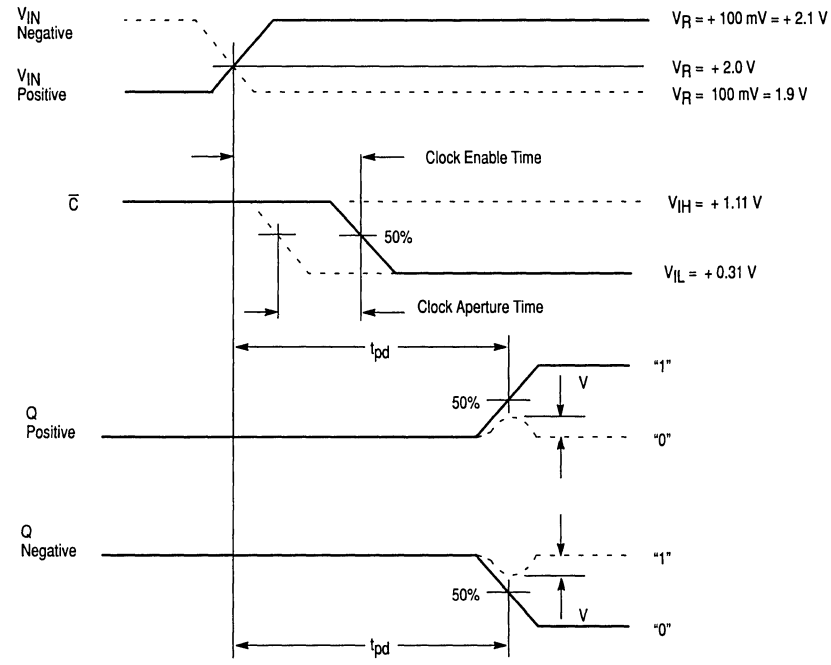


Figure 4. Analog Signal Positive and Negative Skew Case

——— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog Q) is not degraded by more than 500 ps.

- - - - - - Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

NOTE: All power supply and logic levels are shown shifted 2.0 volts positive.

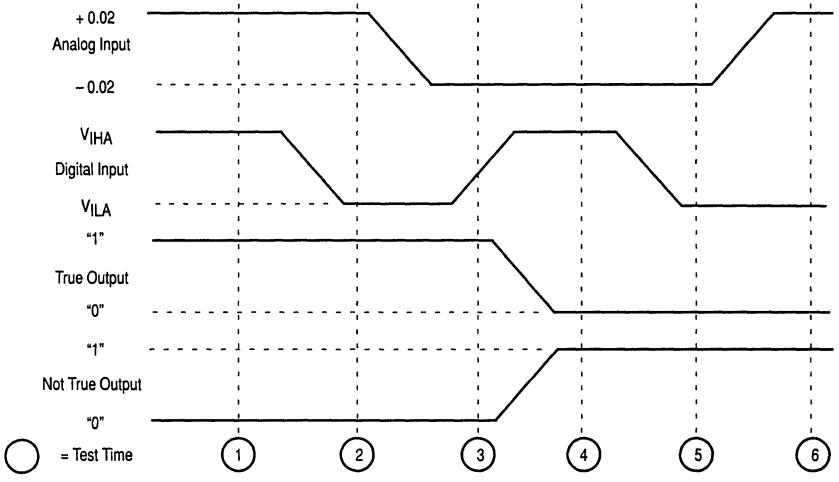


Figure 5. Threshold Pulse Diagram

4

1651
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)											
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{CC}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to - 2.0 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EE}	V_{A1-6}	GND	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V	4, 13				7, 10	8	5, 6, 11, 12	1, 5, 6, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V	4, 13				7, 10	8	5, 6, 11, 12	1, 5, 6, 16	2, 3, 14, 15
V_{OHA}	High Output Voltage	- 0.98	- 0.825	- 0.91	- 0.715	- 1.065	- 0.89	V		4, 6, 12, 13	4, 13	4, 13	7, 10	8	6, 12	1, 5, 6, 16	2, 3, 14, 15
V_{OLA}	Low Output Voltage	- 1.83	- 1.60	- 1.80	- 1.555	- 1.83	- 1.60	V		4, 6, 12, 13	4, 13	4, 13	7, 10	8	6, 12	1, 5, 6, 16	2, 3, 14, 15
I_{INH}	Input Current High		350					µA	4, 13	4, 13			7, 10	8	5, 11	1, 6, 12, 16	4, 13
I_L	Leakage Current	- 10						µA	4, 13	4, 13			7, 10	8	5, 6, 11, 12	1, 6, 12, 16	5, 6, 11, 12

1651
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)											
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{CC}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	+5.0	+0.02	-0.02	+2.5	+2.48	-3.0	-2.98

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C Subgroup 1		+ 85 °C Subgroup 2		- 30 °C Subgroup 3			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to - 2.0 V						
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{CC}	V_{EE}	V_{A1-6}	GND	P.U.T.
I_{INL}	Leakage Current Low	0.5						µA	4, 13	4, 13	7, 10	8	5, 6, 11, 12	1, 5, 6, 12, 16	5, 6, 11, 12
I_{EE}	Power Supply Drain Current	- 55						mA	4, 13		7, 10	8	5, 6, 11, 12	1, 5, 6, 12, 16	8
* I_{CC}	Power Supply Drain Off		+25					mA		4, 13	7, 10	8	5, 6, 11, 12	1, 5, 6, 12, 16	7, 10

* I_{CC} = Total current to pin 7 and 10 tied together.

1651
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)							Test Parameter	Test Voltage Values (Volts)		
	V_H	V_G	V_{B1}	V_{B2}	V_{B3}	V_{CCA}	V_{EEA}		P_1	P_2	P_3
T_A = 25 °C	+1.11	+2.0	-0.9	+2.0	+4.4	+7.0	-3.2	V_{IH}	+2.10	+4.5	-0.80
T_A = 85 °C	+1.19	+2.0	-0.9	+2.0	+4.4	+7.0	-3.2	V_R	+2.0	+4.4	-0.90
T_A = -30 °C	+1.04	+2.0	-0.9	+2.0	+4.4	+7.0	-3.2	V_{IL}	+1.9	+4.3	-1.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND								
		Subgroup 9		Subgroup 10		Subgroup 11											
		Min	Max	Min	Max	Min	Max		V_H	V_G	V_{B1}	V_{B2}	V_{B3}	V_{CCA}	V_{EEA}	P_{1-3}	P.U.T./V_{OUT}
t_{TLH}	Rise Time	1.0	3.5	1.0	3.8	1.0	3.5	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
t_{THL}	Fall Time	1.0	3.0	1.0	3.3	1.0	3.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(1)}$	Propagation Delay	2.0	5.0	2.0	5.7	2.0	5.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(1)}$	Propagation Delay	2.0	5.0	2.0	5.7	2.0	5.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(2)}$	Propagation Delay	2.0	5.0	2.0	5.2	2.0	5.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
$t_{pd(2)}$	Propagation Delay	2.0	5.0	2.0	5.2	2.0	5.0	ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15
t_{setup}	Setup Time	2.5		2.5		2.5		ns	4, 13	1, 16	5, 12	5, 12	5, 12	7, 10	8	4, 6, 11, 13	2, 3, 14, 15

MOTOROLA

Binary Counter

Military 1654

ELECTRICALLY TESTED PER:
MPG 1654 (– 30°C to + 85°C)

The 1654 is a 4-bit counter capable of divide-by-two, divide-by-four, divide-by-eight, or divide-by-16 functions. Clock inputs trigger on the positive going edge of the clock pulse.

Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all levels.

- Power Dissipation = 750 mW typ
- f_{Tog} = 325 MHz typ

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage (V_{CC} = 0)	V_{CC}	– 8.0	0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{IN}	0	V_{EE}	Vdc
Output Source Current Continuous	I_O		< 40	mAdc
Storage Temperature Range	T_{stg}	– 55	+ 125	°C
Operating Temperature Range	T_A	– 30	+ 85	°C

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1654/BXA *
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E

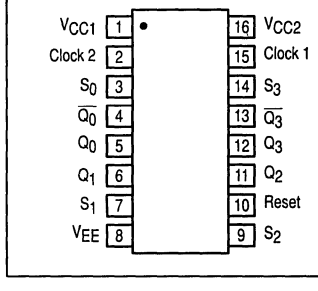
*** 883 Processing (Non-Compliant)**

4

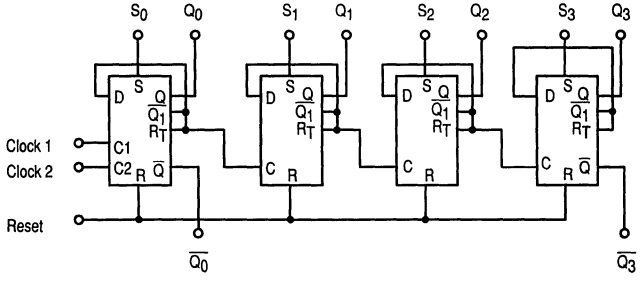
PIN ASSIGNMENTS

FUNCTION	DIL	BURN-IN (CONDITION C)
V_{CC1}	1	GND
Clock 2	2	OPEN
S_0	3	GND
$\overline{Q_0}$	4	51 Ω to V_{TT}
Q_0	5	51 Ω to V_{TT}
Q_1	6	51 Ω to V_{TT}
S_1	7	GND
V_{EE}	8	V_{EE}
S_2	9	GND
Reset	10	OPEN
Q_2	11	51 Ω to V_{TT}
Q_3	12	51 Ω to V_{TT}
$\overline{Q_3}$	13	51 Ω to V_{TT}
S_3	14	GND
Clock 1	15	OPEN
V_{CC2}	16	GND

BURN - IN CONDITIONS:
V_{TT} = – 1.8 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 4.7 V MIN



LOGIC DIAGRAM



TRUTH TABLE

Inputs							Outputs			
R	S_0	S_1	S_2	S_3	C_1	C_2	Q_0	Q_1	Q_2	Q_3
1	0	0	0	0	ϕ	ϕ	0	0	0	0
0	1	1	1	1	ϕ	ϕ	1	1	1	1
0	0	0	0	0	1	ϕ	No Count			
0	0	0	0	0	ϕ	1	No Count			
0	0	0	0	0	**	**	0	0	0	0
0	0	0	0	0	**	**	1	0	0	0
0	0	0	0	0	**	**	0	1	0	0
0	0	0	0	0	**	**	1	1	0	0
0	0	0	0	0	**	**	0	0	1	0
0	0	0	0	0	**	**	1	0	1	0
0	0	0	0	0	**	**	0	1	1	0
0	0	0	0	0	**	**	1	1	1	0
0	0	0	0	0	**	**	0	0	0	1
0	0	0	0	0	**	**	1	0	0	1
0	0	0	0	0	**	**	0	1	0	1
0	0	0	0	0	**	**	1	1	0	1
0	0	0	0	0	**	**	0	0	1	1
0	0	0	0	0	**	**	1	0	1	1
0	0	0	0	0	**	**	0	1	1	1
0	0	0	0	0	**	**	1	1	1	1

ϕ = Don't Care
** = V_{IH} Clock transition from V_{IL} to V_{IH}
V_{IL} may be applied to C_1 or C_2 or both for same effect

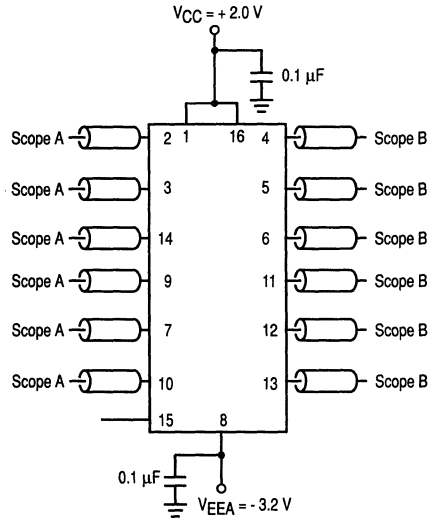


Figure 1. Test Circuit

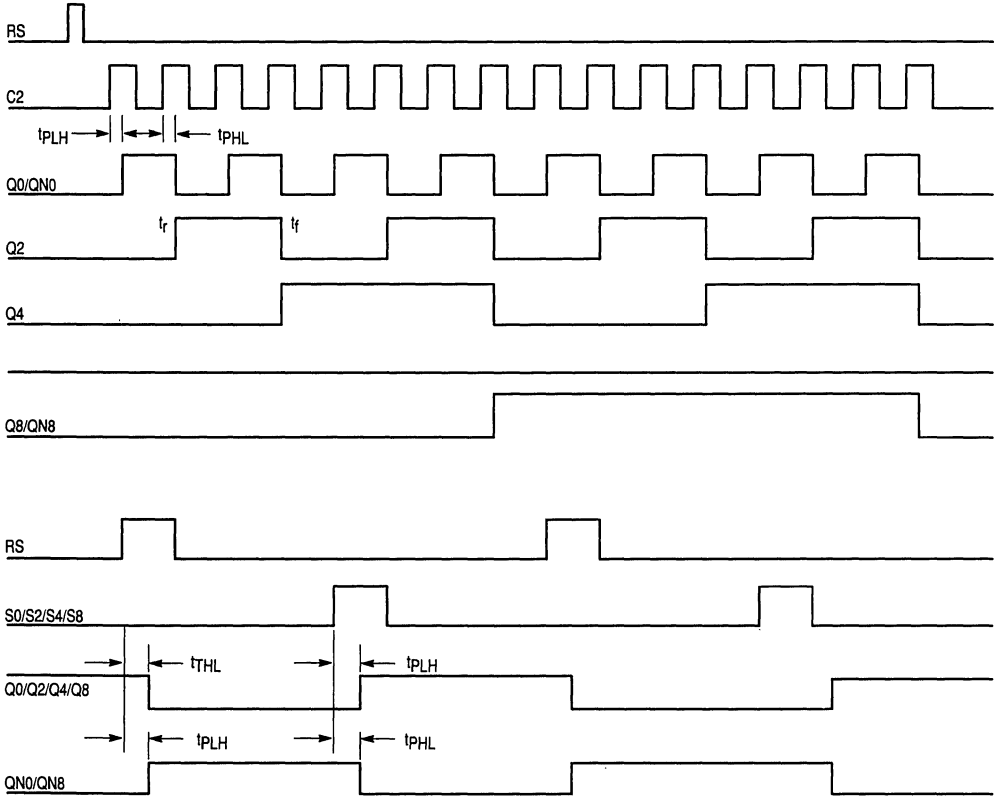


Figure 2. Test Circuit Waveforms

Temp.	25°C	85°C	−30°C
V_{ILL}	0.31 V	0.337 V	0.285 V
V_{IHH}	1.11 V	1.185 V	1.041 V
P_{IN}	1.0 MHz	1.0 MHz	1.0 MHz
t_r, t_f	1.5 ns	1.5 ns	1.5 ns

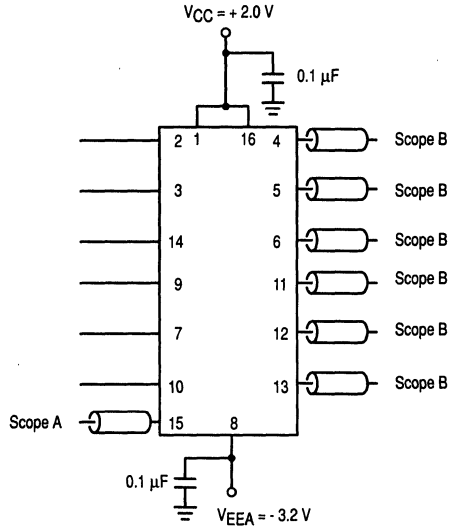


Figure 3. Toggle Test Circuit

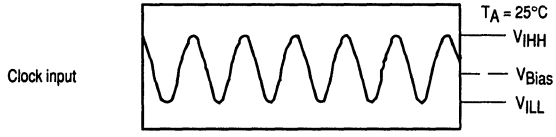


Figure 4. Toggle Waveform

Temp.	25°C	85°C	– 30°C
V_{ILL}	0.31 V	0.337 V	0.285 V
V_{IHH}	1.11 V	1.185 V	1.041 V
P_{IN}	300 MHz	260 MHz	260 MHz

1654
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0.0 V, Output Load = 50 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EE}	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V	3, 7, 9, 10, 14				1, 16	8	4 - 6, 11 - 13
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V	3, 10, 14				1, 16	8	4 - 6, 11 - 13
V_{OHA}	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V			3, 7, 9, 10, 14		1, 16	8	4 - 6, 11 - 13
V_{OLA}	Low Output Voltage	- 1.85	- 1.60	- 1.83	- 1.555	- 1.89	- 1.63	V	3, 7, 9, 10, 14			3, 7, 9, 10, 14	1, 16	8	4 - 6, 11 - 13
I_{EE}	Power Supply Drain Current	- 200						mA	2, 3, 7, 9, 10, 14, 15				1, 16	8	8
I_{INH1}	Input Current High		600					µA	2, 3, 7, 14, 15				1, 16	8	2, 3, 7, 14, 15
I_{INH2}	Input Current High		1.0					mA	10				1, 16	8	10
I_{INL}	Input Current Low	0.5						µA		2, 3, 7, 9, 10, 14, 15			1, 16	8	2, 3, 7, 9, 10, 14, 15

1654
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}	V_{CC}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+5.0
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+5.0
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+5.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{ILL}	V_{IN}	V_{OUT}	V_{CC}	V_{EEA}	C_{P1-3}	P.U.T.
t_{TLH}	Rise Time (Pins 4 - 6, 11 - 13)		2.7		3.1		2.9	ns	2, 3, 7, 9, 14	2, 3, 10	4 - 6, 6 - 13	1, 16	8		4 - 6, 6 - 13
t_{THL}	Fall Time (Pins 4 - 6, 11 - 13)		2.6		3.0		2.8	ns	2, 3, 7, 9, 14	2, 3, 10	4 - 6, 6 - 13	1, 16	8		4 - 6, 6 - 13
t_{pd}	Propagation Delay Clock (t2+5+, t2+4+) Reset		3.3 4.9		3.7 4.9		2.9 5.1	ns ns	2, 3, 7, 9, 14 2, 3, 7, 9, 14	2, 3, 10 2, 3, 10	4 - 6, 6 - 13 4 - 6, 6 - 13	1, 16 1, 16	8 8		4 - 6, 6 - 13 4 - 6, 6 - 13
f_{Tog}	Toggle Frequency	260		260		260		MHz			4 - 6, 6 - 13	1, 16	8	15	4 - 6, 6 - 13

MOTOROLA

Dual 4-Input OR/NOR Gate

Military 1660

ELECTRICALLY TESTED PER:
MPG 1660 (– 30°C to + 85°C)

- P_D = 120 mW typ/pkg
- t_{pd} = 0.9 ns typ (510 ohm load)
  = 1.1 ns typ (50 ohm load)
- Full Load Current, I_L = – 25 mAdc max

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage (V_{CC} = 0)	V_{CC}	– 8.0	0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{IN}	0	V_{EE}	Vdc
Output Source Current Continuous	I_O		< 40	mAdc
Storage Temperature Range	T_{stg}	– 55	+ 175	°C
Operating Temperature Range	T_A	– 30	+ 85	°C

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1660/BXA *
X = CASE OUTLINE AS FOLLOWS:

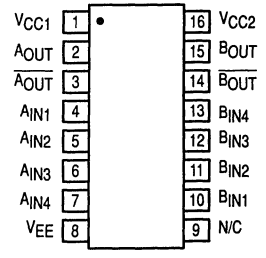
PACKAGE: CERDIP: E
CERFLAT: F

*** 883 Processing (Non-Compliant)**

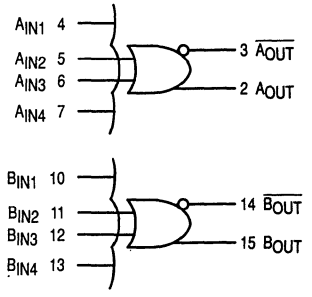
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CC1}	1	5	GND
A_{OUT}	2	6	51 Ω to V_{TT}
$\overline{A_{OUT}}$	3	7	51 Ω to V_{TT}
A_{IN1}	4	8	OPEN
A_{IN2}	5	9	OPEN
A_{IN3}	6	10	OPEN
A_{IN4}	7	11	OPEN
V_{EE}	8	12	V_{EE}
N.C.	9	13	OPEN
B_{IN1}	10	14	OPEN
B_{IN2}	11	15	GND
B_{IN3}	12	16	OPEN
B_{IN4}	13	1	GND
$\overline{B_{OUT}}$	14	2	51 Ω to V_{TT}
B_{OUT}	15	3	51 Ω to V_{TT}
V_{CC2}	16	4	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM



$\overline{OUT} = IN1 + IN2 + IN3 + IN4$
$OUT = \overline{IN1 + IN2 + IN3 + IN4}$

4

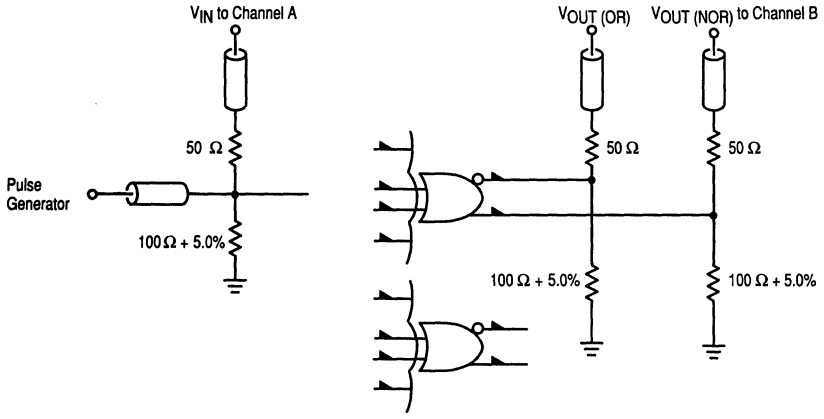


Figure 1. Test Circuit

4

NOTES

1. Pulse Amp. = 0.8 V.
2. $t_r = t_f = 1.5$ ns + 0.2 ns (measured between 10% and 90%).
3. PRR = 20 MHz, 50% duty cycle.
4. DC level = 0.71 V.
5. Unused outputs connected to a 100 Ω resistor to ground.

Temp.	25°C	85°C	– 30°C
V_{ILL}	0.31 V	0.337 V	0.285 V
V_{IHH}	1.11 V	1.185 V	1.04 1V

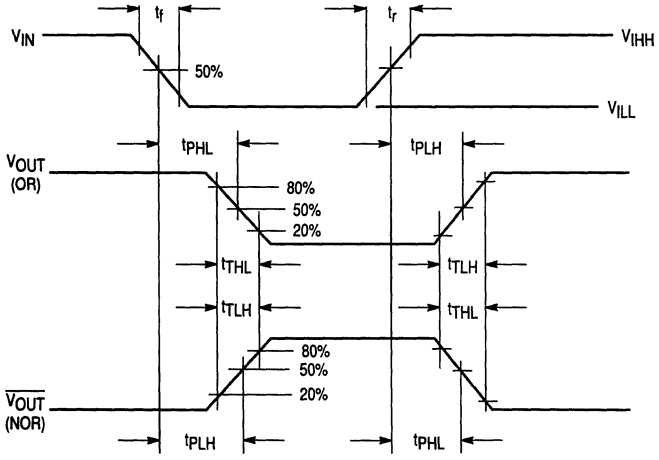


Figure 2. Test Circuit Waveforms

1660
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EE}	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V	4 - 7, 10 - 13	4 - 7, 10 - 13			1, 16	8	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V	4 - 7, 10 - 13	4 - 7, 10 - 13			1, 16	8	2, 3, 14, 15
V_{OHA}	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V		4 - 7, 10 - 13	4 - 7, 10 - 13	4 - 7, 10 - 13	1, 16	8	2, 3, 14, 15
V_{OLA}	Low Output Voltage	- 1.85	- 1.60	- 1.83	- 1.555	- 1.89	- 1.63	V		4 - 7, 10 - 13	4 - 7, 10 - 13	4 - 7, 10 - 13	1, 16	8	2, 3, 14, 15
I_{EE}	Power Supply Drain Current	-28		-28		-28		mA					1, 16	8	8
I_{INH}	Input Current High		350		350		350	µA	4 - 7, 10 - 13	4 - 7, 10 - 13			1, 16	8	4 - 7, 10 - 13
I_{INL}	Input Current Low	0.5		0.3		0.5		µA	4 - 7, 10 - 13	4 - 7, 10 - 13			1, 16	8	4 - 7, 10 - 13

1660
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}	V_{CC}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+2.0
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+2.0
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EE}	P.U.T.
t_{TLH}	Rise Time		2.1		2.3		2.2	ns	4, 11	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time		2.1		2.3		2.2	ns	4, 11	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{PHL}	Propagation Delay High to Low (NOR)		1.9		2.1		2.0	ns	4, 11	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High (NOR)		1.8		2.0		1.9	ns	4, 11	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{PHL}	Propagation Delay High to Low (OR)		1.7		1.9		1.8	ns	4, 11	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High (OR)		1.8		2.0		1.9	ns	4, 11	2, 3, 14, 16	1, 16	8	2, 3, 14, 15

MOTOROLA

Quad 2-Input NOR Gate

ELECTRICALLY TESTED PER:
MPG 1662 (– 30°C to + 85°C)

- P_D = 240 mW typ/pkg
- t_{pd} = 0.9 ns typ (510 ohm load)
  = 1.1 ns typ (50 ohm load)
- Full Load Current, I_L = – 25 mAdc max

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage (V_{CC} = 0)	V_{CC}	– 8.0	0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{IN}	0	V_{EE}	Vdc
Output Source Current Continuous	I_O		< 40	mAdc
Storage Temperature Range	T_{stg}	– 55	+ 125	°C
Operating Temperature Range	T_A	– 30	+ 85	°C

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CC1}	1	5	GND
A_{OUT}	2	6	51 Ω to V_{TT}
B_{OUT}	3	7	51 Ω to V_{TT}
A_{IN1}	4	8	OPEN
A_{IN2}	5	9	OPEN
B_{IN1}	6	10	OPEN
B_{IN2}	7	11	OPEN
V_{EE}	8	12	V_{EE}
N.C.	9	13	OPEN
C_{IN1}	10	14	OPEN
C_{IN2}	11	15	GND
D_{IN1}	12	16	OPEN
D_{IN2}	13	1	GND
C_{OUT}	14	2	51 Ω to V_{TT}
D_{OUT}	15	3	51 Ω to V_{TT}
V_{CC2}	16	4	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

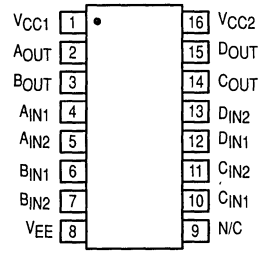
Military 1662

AVAILABLE AS

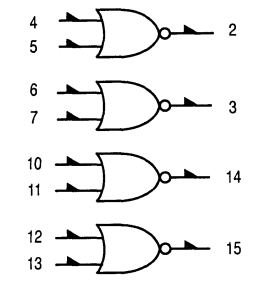
1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1662/BXA *
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F

*** 883 Processing (Non-Compliant)**



LOGIC DIAGRAM



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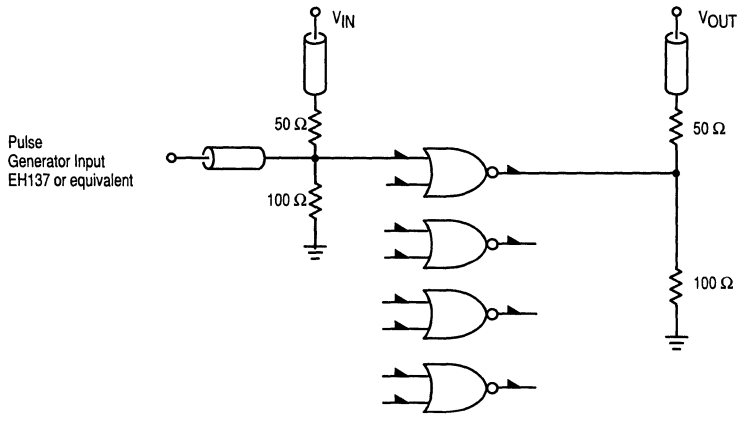


Figure 1. Test Circuit

4

NOTES

1. Coaxial cables (Equal lengths, typ 2 places) to scope.
2. $t_r = t_f = 1.5$ ns ± 0.2 ns.
3. PRR = 20 MHz, 50% duty cycle.
4. Unused outputs connected to a 50 Ω resistor to ground.

Temp.	25°C	85°C	– 30°C
V_{ILL}	0.31 V	0.34 V	0.28 V
V_{IHH}	1.11 V	1.19 V	1.04 V

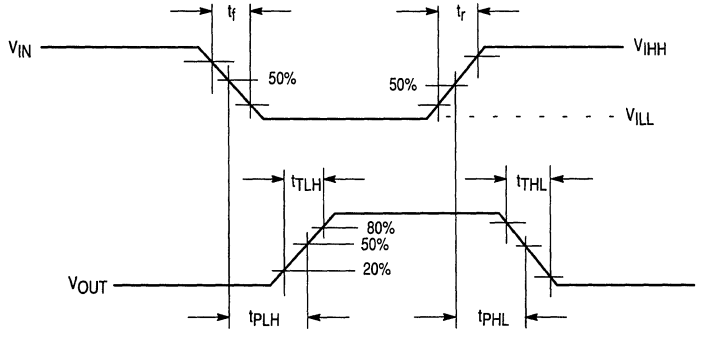


Figure 2. Test Circuit Waveforms

1662
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEL}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0.0 V, Output Load = 50 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EE}	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V		4 - 7, 10 - 13			1, 16	8	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V	4 - 7, 10 - 13				1, 16	8	2, 3, 14, 15
V_{OHA}	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V				4 - 7, 10 - 13	1, 16	8	2, 3, 14, 15
V_{OLA}	Low Output Voltage	- 1.85	- 1.60	- 1.83	- 1.555	- 1.89	- 1.63	V			4 - 7, 10 - 13		1, 16	8	2, 3, 14, 15
I_{EE}	Power Supply Drain Current	-56		-56		-56		mA					1, 16	8	8
I_{INH}	Input Current High		350		350		350	µA	4 - 7, 10 - 13				1, 16	8	4 - 7, 10 - 13
I_{INL}	Input Current Low	0.5		0.3		0.5		µA		4 - 7, 10 - 13			1, 16	8	4 - 7, 10 - 13

1662
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEL}	V_{CC}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+2.0
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+2.0
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time		2.1		2.3		2.2	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time		2.1		2.3		2.2	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{PHL}	Propagation Delay High to Low A, B and D		1.9		2.1		2.0	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High A, B and D		2.1		2.1		2.1	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{PHL}	Propagation Delay High to Low C		2.0		2.2		2.1	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High C		2.1		2.1		2.1	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15

MOTOROLA

Quad 2-Input OR Gate

ELECTRICALLY TESTED PER:
MPG 1664 (– 30°C to + 85°C)

- P_D = 240 mW typ/pkg
- t_{pd} = 0.9 ns typ (510 ohm load)
  = 1.1 ns typ (50 ohm load)
- Full Load Current, I_L = – 25 mAdc max

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage (V_{CC} = 0)	V_{CC}	– 8.0	0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{IN}	0	V_{EE}	Vdc
Output Source Current Continuous	I_O		< 40	mAdc
Storage Temperature Range	T_{stg}	– 55	+ 125	°C
Operating Temperature Range	T_A	– 30	+ 85	°C

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CC1}	1	5	GND
A_{OUT}	2	6	51 Ω to V_{TT}
B_{OUT}	3	7	51 Ω to V_{TT}
A_{IN1}	4	8	GND
A_{IN2}	5	9	OPEN
B_{IN1}	6	10	GND
B_{IN2}	7	11	OPEN
V_{EE}	8	12	V_{EE}
N.C.	9	13	OPEN
C_{IN1}	10	14	GND
C_{IN2}	11	15	OPEN
D_{IN1}	12	16	GND
D_{IN2}	13	1	OPEN
C_{OUT}	14	2	51 Ω to V_{TT}
D_{OUT}	15	3	51 Ω to V_{TT}
V_{CC2}	16	4	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

Military 1664

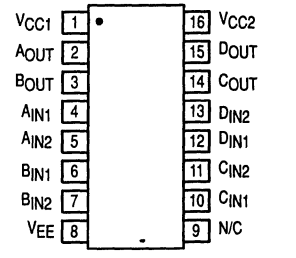
AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1664/BXA *
X = CASE OUTLINE AS FOLLOWS:

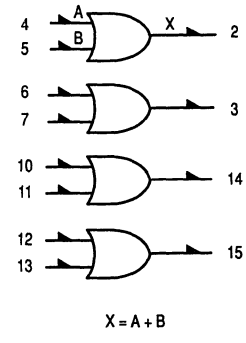
PACKAGE: CERDIP: E
CERFLAT: F

*** 883 Processing (Non-Compliant)**

4



LOGIC DIAGRAM



X = A + B

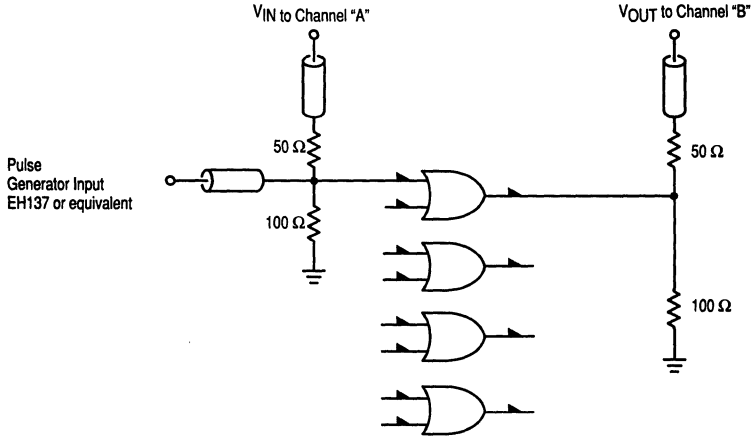


Figure 1. Test Circuit

4

NOTES

1. Coaxial cables (Equal lengths, typ 2 places) to scope.
2. $t_r = t_f = 1.5$ ns ± 0.2 ns.
3. PRR = 20 MHz, 50% duty cycle.
4. Unused outputs connected to a 50 Ω resistor to ground.

Temp.	25°C	85°C	– 30°C
V_{ILL}	0.31 V	0.337 V	0.285 V
V_{IHH}	1.11 V	1.185 V	1.041 V

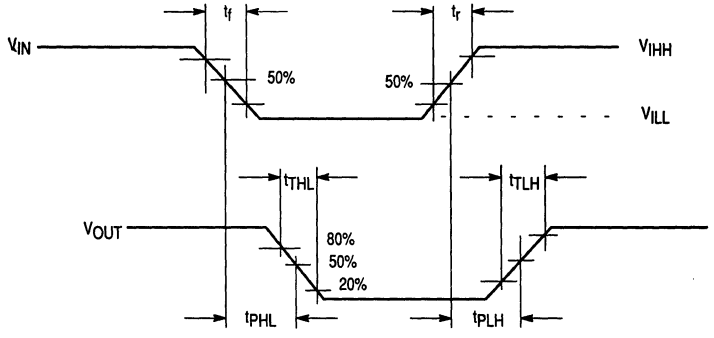


Figure 2. Test Circuit Waveforms

1664
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C Subgroup 1		+ 85 °C Subgroup 2		- 30 °C Subgroup 3			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0.0 V, Output Load = 50 Ω to - 2.0 V						
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EE}	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V	4 - 7, 10 - 13				1, 16	8	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V		4 - 7, 10 - 13			1, 16	8	2, 3, 14, 15
V_{OHA}	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V			4 - 7, 10 - 13		1, 16	8	2, 3, 14, 15
V_{OLA}	Low Output Voltage	- 1.85	- 1.60	- 1.83	- 1.555	- 1.89	- 1.63	V				4 - 7, 10 - 13	1, 16	8	2, 3, 14, 15
I_{EE}	Power Supply Drain Current	-56						mA					1, 16	8	8
I_{INH}	Input Current High		350					µA	4 - 7, 10 - 13				1, 16	8	4 - 7, 10 - 13
I_{INL}	Input Current Low	0.5						µA		4 - 7, 10 - 13			1, 16	8	4 - 7, 10 - 13

1664
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEL}	V_{CC}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+2.0
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+2.0
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEA}	P.U.T.
t_{TLH}	Rise Time		2.1		2.3		2.2	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time		2.1		2.3		2.2	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{PHL}	Propagation Delay High to Low	0.6	1.7	0.6	1.9	0.6	1.8	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15
t_{PLH}	Propagation Delay Low to High	0.6	1.5	0.6	1.7	0.6	1.6	ns	5, 6 11, 12	2, 3, 14, 16	1, 16	8	2, 3, 14, 15

MOTOROLA

Dual Clocked Latch

ELECTRICALLY TESTED PER:
MPG 1668 (– 30°C to + 85°C)

- P_D = 220 mW typ/pkg
- t_{pd} = 1.6 ns typ (510 ohm load)
  = 1.8 ns typ (50 ohm load)

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage (V_{CC} = 0)	V_{CC}	– 8.0	0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{IN}	0	V_{EE}	Vdc
Output Source Current Continuous	I_O		< 40	mAdc
Storage Temperature Range	T_{stg}	– 55	+ 125	°C
Operating Temperature Range	T_A	– 30	+ 85	°C

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CC1}	1	5	GND
Q_1	2	6	51 Ω to V_{TT}
$\overline{Q}_1$	3	7	51 Ω to V_{TT}
R_1	4	8	OPEN
S_1	5	9	GND
D_1	6	10	OPEN
C_1	7	11	OPEN
V_{EE}	8	12	VEE
C_2	9	13	OPEN
N.C.	10	14	OPEN
D_2	11	15	OPEN
S_2	12	16	GND
R_2	13	1	OPEN
$\overline{Q}_2$	14	2	51 Ω to V_{TT}
Q_2	15	3	51 Ω to V_{TT}
V_{CC2}	16	4	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

NOTICE: END OF LIFE — FINAL ORDERS MUST BE PLACED BY DECEMBER 31, 1991

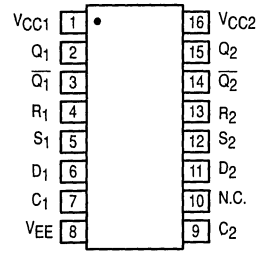
Military 1668

AVAILABLE AS

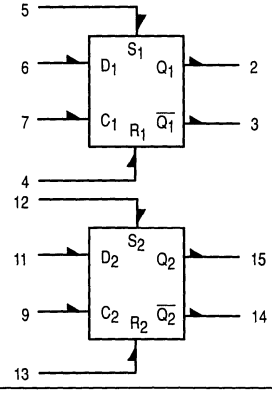
1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1668/BXA *
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F

*** 883 Processing (Non-Compliant)**



LOGIC DIAGRAM



4

TRUTH TABLE

S	R	D	C	Q_{n+1}
0	0	ϕ	0	Q_n
1	0	ϕ	0	1
0	1	ϕ	0	0
1	1	ϕ	0	**
ϕ	ϕ	0	1	0
ϕ	ϕ	1	1	1

** Output state not defined ϕ = Don't Care

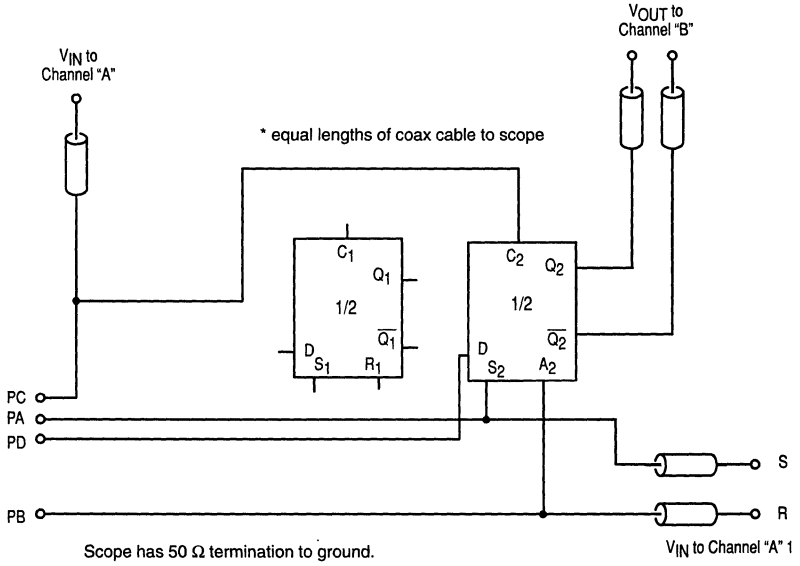
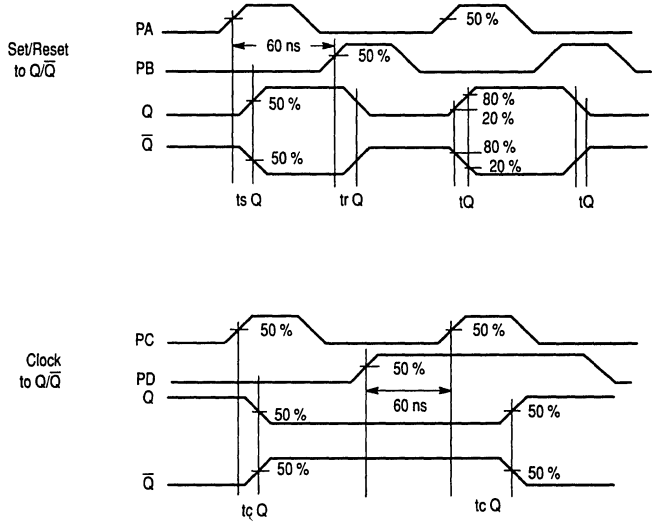


Figure 1. Set and Reset Switching Test Circuit

Temp.	25°C	85°C	– 30°C
V_{ILL}	0.31 V	0.337 V	0.285 V
V_{IHH}	1.11 V	1.185 V	1.041 V



NOTES

1. Input Pulse Characteristics:
   a) Frequency A, B, D = 1.0 MHz.
   b) Frequency C = 2.0 MHz.
   c) Duty Cycle = 50%.
2. $t_r = t_f = 2.0$ ns (20% – 80%).

Figure 2. Switching Waveforms

4

1668
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0.0 V, Output Load = 50 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EE}	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V	4 - 7, 9, 11 - 13	4 - 7, 9, 11 - 13			1, 16	8	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V	4 - 7, 9, 11 - 13	4 - 7, 9, 11 - 13			1, 16	8	2, 3, 14, 15
V_{OHA}	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V		4 - 7, 9, 11 - 13	4 - 7, 9, 11 - 13	4 - 7, 9, 11 - 13	1, 16	8	2, 3, 14, 15
V_{OLA}	Low Output Voltage	- 1.85	- 1.60	- 1.83	- 1.555	- 1.89	- 1.63	V		4 - 7, 9, 11 - 13	4, 5, 7, 12, 13	4 - 7, 9, 11 - 13	1, 16	8	2, 3, 14, 15
I_{EE}	Power Supply Drain Current	-55	-6					mA	7, 9				1, 16	8	8
I_{INH1}	Input Current High		370					µA	4 - 7, 9, 11 - 13				1, 16	8	4 - 6, 11 - 13
I_{INH2}	Input Current High		225					µA	7, 9				1, 16	8	7, 9
I_{INL}	Input Current Low	0.5						µA		4 - 7, 9, 11 - 13			1, 16	8	4 - 7, 9, 11 - 13

1668
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEL}	V_{CC}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+2.0
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+2.0
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEA}	P.U.T.
t_{TLH}	Rise Time	0.8	2.5	0.9	2.9	0.8	2.8	ns	4 - 7, 9, 11 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	0.5	2.2	0.5	2.6	0.5	2.4	ns	4 - 7, 9, 11 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{pd}	Propagation Delay Clock to Output	1.0	2.5	1.1	2.8	1.0	2.7	ns	4 - 7, 9, 11 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{pd}	Propagation Delay S/R to Output	1.0	2.3	1.1	2.7	1.0	2.5	ns	4 - 7, 9, 11 - 13	2, 3, 14, 15	1, 16	8	2, 3, 14, 15

MOTOROLA

Master-Slave Flip-Flop

Military 1670

ELECTRICALLY TESTED PER:
MPG 1670 (– 30°C to + 85°C)

Master slave construction renders the 1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when dock input (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled. Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) Inputs.

- P_D = 220 mW typ/pkg (No Load)
- f_{TOG} = 350 MHz typ

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage (V_{CC} = 0)	V_{CC}	– 8.0	0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{IN}	0	V_{EE}	Vdc
Output Source Current Continuous	I_O		< 40	mAdc
Storage Temperature Range	T_{stg}	– 55	+ 125	°C
Operating Temperature Range	T_A	– 30	+ 85	°C

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CC1}	1	5	GND
Q	2	6	51 Ω to V_{TT}
$\overline{Q}$	3	7	51 Ω to V_{TT}
Reset	4	8	OPEN
Set	5	9	GND
N.C.	6	10	OPEN
Clock 1	7	11	OPEN
V_{EE}	8	12	VEE
Clock 2	9	13	OPEN
N.C.	10	14	OPEN
Data	11	15	OPEN
N.C.	12	16	GND
N.C.	13	1	OPEN
N.C.	14	2	51 Ω to V_{TT}
N.C.	15	3	51 Ω to V_{TT}
V_{CC2}	16	4	GND

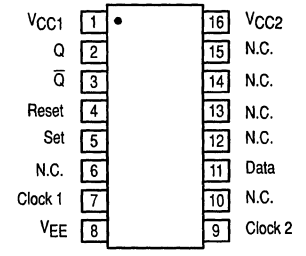
BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

AVAILABLE AS

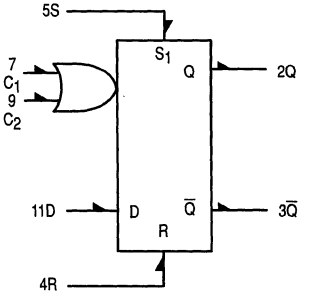
1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1670/BXA *
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F

*** 883 Processing (Non-Compliant)**



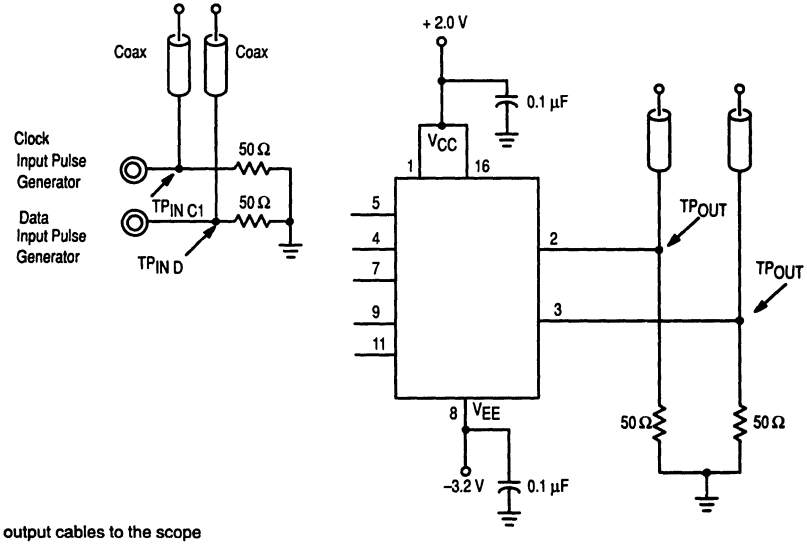
LOGIC DIAGRAM



TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	⌐	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	⌐	H
L	L	H	H	Q_n

N.D. = Not Defined
ϕ = Don't Care
.C = C1 + C2



NOTE
1. All input and output cables to the scope are equal lengths of 50 ohm coaxial cable

Figure 1. Switching Test Circuit

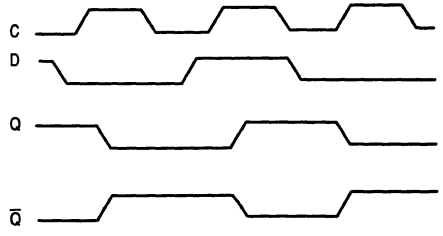


Figure 2. Timing Diagram

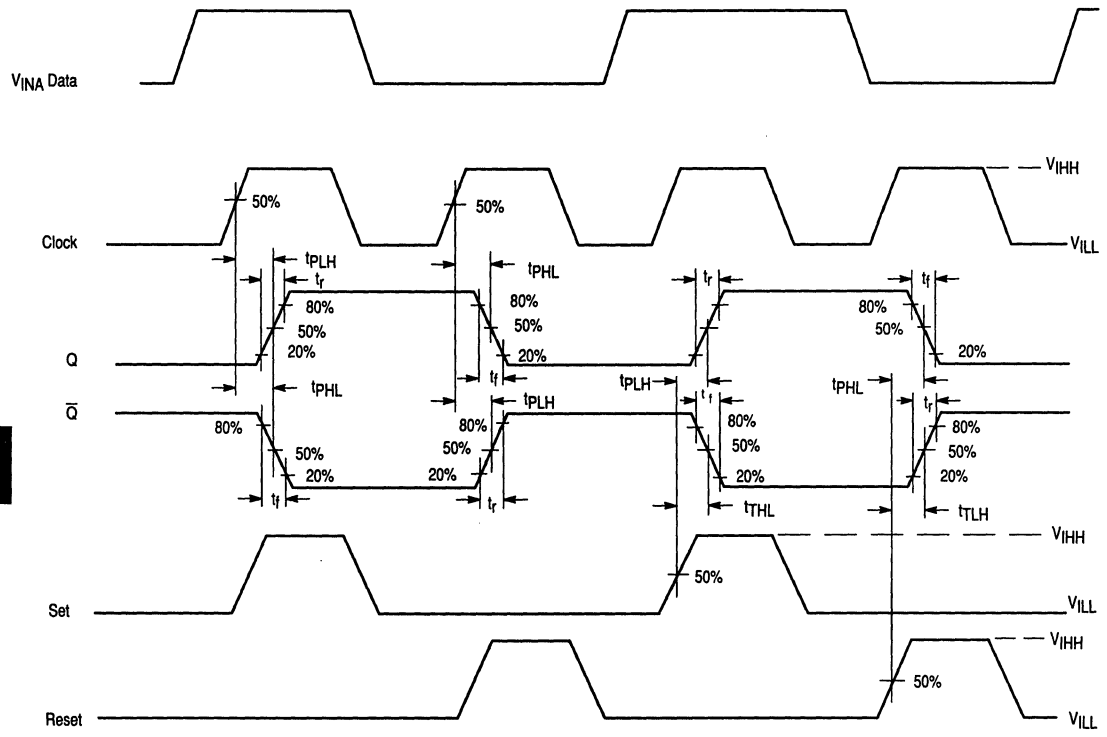
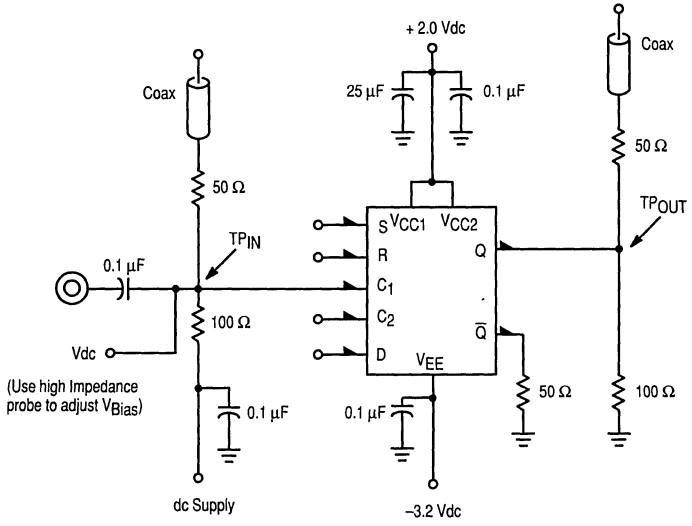


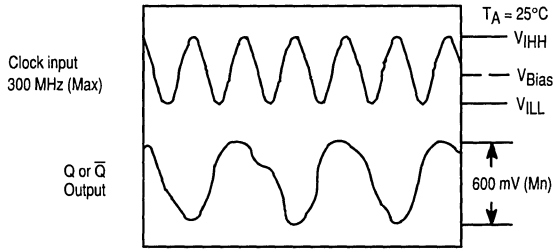
Figure 3. Switching Waveforms

Temp.	25°C	85°C	– 30°C
V_{IHH}	1.11 V	1.185 V	1.041 V
V_{ILL}	0.31 V	0.337 V	0.285 V



NOTE
All input and output cables to the scope are equal lengths of 50 ohm coaxial cable

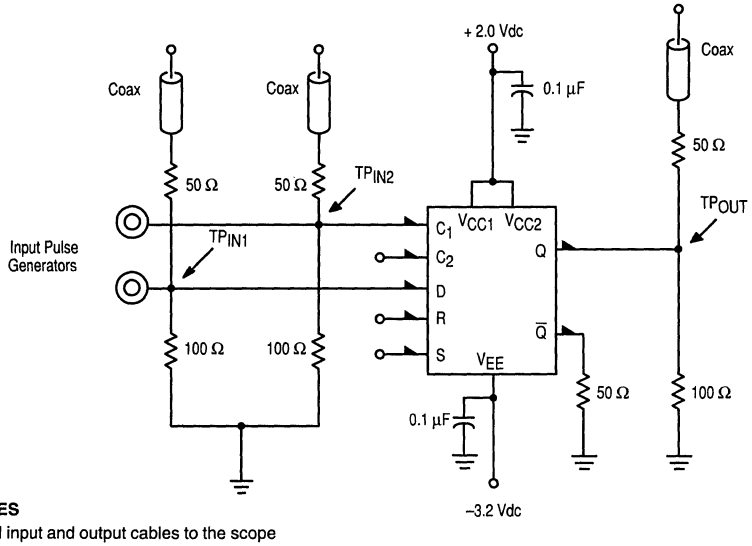
Figure 4. Toggle Frequency Test Circuit



NOTES
1. The maximum toggle frequency of the device has been exceed when either:
   a) The output peak to peak voltage swing falls below 600 mV, or
   b) The device ceases to toggle (devide by two).

Figure 5. Toggle Frequency Waveforms

Temp.	25°C	85°C	– 30°C
V_{IHH}	1.11 V	1.185 V	1.041 V
V_{ILL}	0.31 V	0.337 V	0.285 V
V_{Bias}	0.71 V	0.761 V	0.663 V



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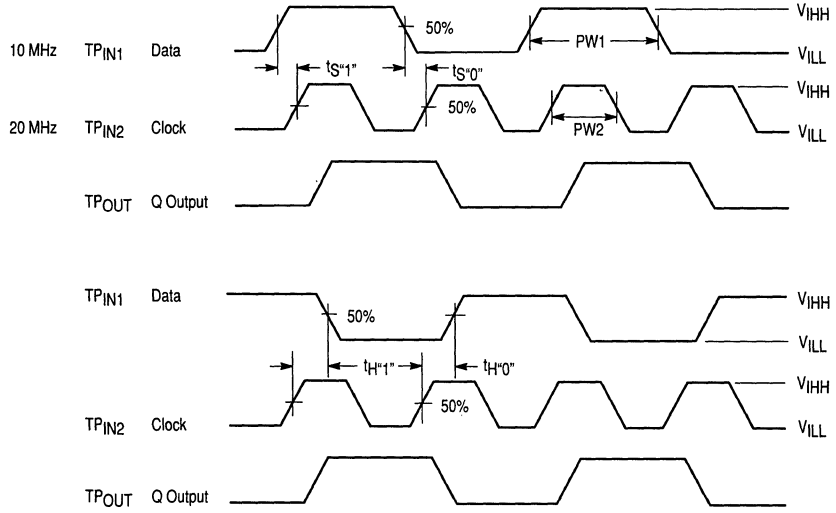
NOTES

1. All input and output cables to the scope are equal lengths of 50 ohm coaxial cable
2. $t_r = t_f = 1.5$ ns ± 0.2 ns (10% to 90%).

Figure 6. Setup and Hold Test Circuit



NOTES

1. Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.
2. Hold time is the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the data (D) input.

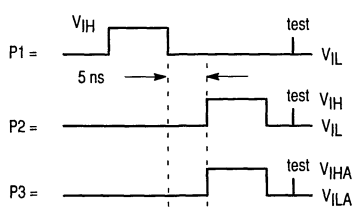
Figure 7. Setup Time and Hold Waveforms

Temp.	25°C	85°C	– 30°C
V_{IHH}	1.11 V	1.185 V	1.041 V
V_{ILL}	0.31 V	0.337 V	0.285 V

1670
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}	V_{CC}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+2.0
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+2.0
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	P_{1-3}	V_{CC}	V_{EE}	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V		4, 5, 7, 9, 11			4, 5	1, 16	8	2, 3
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V		4, 5, 7, 9, 11			4, 5	1, 16	8	2, 3
V_{OHA}	High Output Voltage	- 0.98	- 0.826	- 0.91	- 0.713	- 1.065	- 0.892	V	11	11	11	4, 5, 7, 9, 11	4, 5, 7, 9	1, 16	8	2, 3
V_{OLA}	Low Output Voltage	- 1.828	- 1.60	- 1.808	- 1.555	- 1.867	- 1.63	V			7, 11	4, 5, 7, 9, 11	4, 5, 7, 9	1, 16	8	2, 3
I_{EE}	Power Supply Drain Current	-48						mA	7, 9					1, 16	8	8
I_{INH1}	Input Current High		550					µA	4, 5					1, 16	8	4, 5
I_{INH2}	Input Current High		250					µA	7, 9					1, 16	8	7, 9
I_{INH3}	Input Current High		270					µA	11					1, 16	8	11
I_{INL}	Input Current Low	0.5						µA	7, 11	4, 5, 7, 9, 11				1, 16	8	4, 5, 7, 9, 11



1670
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEL}	V_{CC}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+2.0
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+2.0
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEA}	Data	P.U.T.
t_{TLH}	Rise Time	0.6	2.5	0.6	2.9	0.5	2.7	ns	4, 5, 9, 11	2, 3	1, 16	8		2, 3
t_{THL}	Fall Time	0.6	1.9	0.6	2.3	0.5	2.1	ns	4, 5, 9, 11	2, 3	1, 16	8		2, 3
t_{pd}	Propagation Delay High to Low	1.1	2.5	1.1	2.9	1.0	2.7	ns	4, 5, 9, 11	2, 3	1, 16	8		2, 3
t_{pd}	Propagation Delay Low to High	1.1	2.5	1.1	2.9	1.0	2.7	ns	4, 5, 9, 11	2, 3	1, 16	8		2, 3
f_{Tog}	Toggle Frequency	300		270		270		MHz	3	2	1, 16	8	11	2
t_s	Set-Up Time t_s"1" t_s"0"		0.4 0.5					ns ns	6 6	2 2	1, 16 1, 16	8 8	11 11	2 2
t_h	Hold Time t_s"1" t_s"0"		0.6 0.5					ns ns	6 6	2 2	1, 16 1, 16	8 8	11 11	2 2
t_{Reset}	Reset	1.1	3.0	1.1	3.4	1.0	3.2	ns	6	2	1, 16	8	11	2

* Temperature Limits are guaranteed but not tested.

MOTOROLA

Triple 2-Input Exclusive-OR Gate

Military 1672

ELECTRICALLY TESTED PER:
MPG 1672 (– 30°C to + 85°C)

- P_D = 220 mW typ/pkg
- t_{pd} = 1.1 ns typ (510 ohm load)
  = 1.3 ns typ (50 ohm load)
- Full Load Current, I_L = – 25 mAdc max

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage (V_{CC} = 0)	V_{CC}	– 8.0	0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{IN}	0	V_{EE}	Vdc
Output Source Current Continuous	I_O		< 40	mAdc
Storage Temperature Range	T_{stg}	– 55	+ 125	°C
Operating Temperature Range	T_A	– 30	+ 85	°C

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1672/BXA *
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F

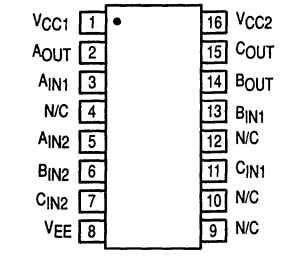
*** 883 Processing (Non-Compliant)**

4

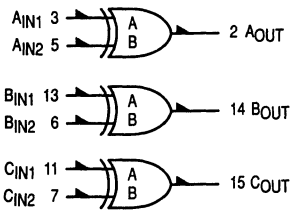
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CC1}	1	5	GND
A_{OUT}	2	6	51 Ω to V_{TT}
A_{IN1}	3	7	GND
N.C.	4	8	OPEN
A_{IN2}	5	9	OPEN
B_{IN2}	6	10	OPEN
C_{IN2}	7	11	OPEN
V_{EE}	8	12	VEE
N.C.	9	13	OPEN
N.C.	10	14	OPEN
C_{IN1}	11	15	GND
N.C.	12	16	OPEN
B_{IN1}	13	1	GND
B_{OUT}	14	2	51 Ω to V_{TT}
C_{OUT}	15	3	51 Ω to V_{TT}
V_{CC2}	16	4	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM



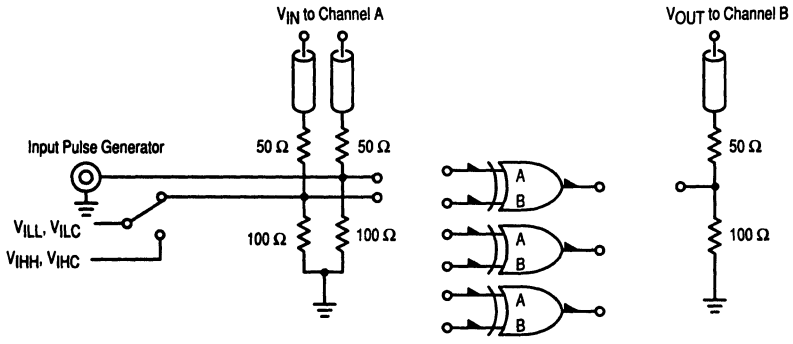


Figure 1. Test Circuit

NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
2. $t_r = t_f = 1.5$ ns (measured between 10% and 90%).
3. Frequency = 20 MHz.
4. 50% duty cycle.
5. For V_{OUT},1 apply V_{IN} to input A and V_{ILL} to input B.
6. For V_{OUT},2 apply V_{IN} to input A and V_{IHH} to input B.
7. Unused outputs connected to a 50 Ω resistor to ground.

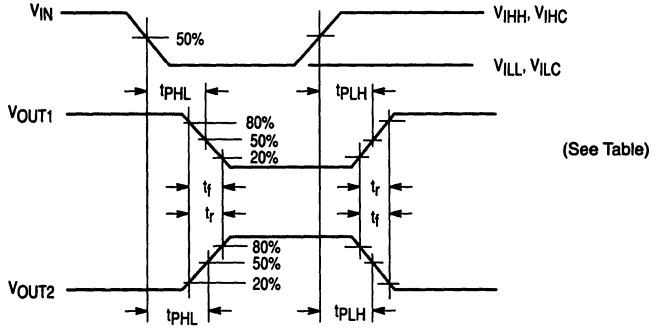


Figure 2. Test Circuit Waveforms

Temp.	25°C	85°C	– 30°C
V_{ILL}	0.31 V	0.337 V	0.285 V
V_{IHH}	1.11 V	1.185 V	1.041 V

1672
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0.0 V, Output Load = 50 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EE}	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V	8 - 11, 14, 16	8 - 11, 14, 16			1, 16	8	2, 3, 6
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V	8 - 11, 14, 16	8 - 11, 14, 16			1, 16	8	2, 3, 6
V_{OHA}	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V			8 - 11, 14, 16	8 - 11, 14, 16	1, 16	8	2, 3, 6
V_{OLA}	Low Output Voltage	- 1.85	- 1.60	- 1.83	- 1.555	- 1.89	- 1.63	V			8 - 11, 14, 16	8 - 11, 14, 16	1, 16	8	2, 3, 6
I_{EE}	Power Supply Drain Current	-55		-61		-61		mA	8 - 11, 14, 16				1, 16	8	2
I_{INH1}	Input Current High		350		590		590	µA	8, 14, 16				1, 16	8	8, 14, 16
I_{INH2}	Input Current High		270		460		460	µA	10, 11				1, 16	8	10, 11
I_{INL}	Input Current Low	0.5		0.3		0.5		µA		8 - 11, 14, 16			1, 16	8	8 - 11, 14, 16

NOTE This table is for DIL only.

1672
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEL}	V_{CC}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+2.0
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+2.0
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEA}	V_{IHC}	V_{ILC}	P.U.T.
t_{pd}	Propagation Delay (t3+2+), (t3+2-), (t13+14+)		1.9		2.4		2.1	ns	3, 13	2, 14	1, 16	8	5	5, 6	2, 14
t_{pd}	Propagation Delay (t3+2+), (t3+2-), t13-14-)(t11+15+) (t11+t15-)		2.0		2.5		2.2	ns	3, 11, 13	2, 14, 15	1, 16	8	5, 6, 7	5, 6, 7	2, 14, 15
t_{pd}	Propagation Delay (t5+2+)(t5+2-) (t16+14+)(t16+14-) (t11-15+)(t7+15+) (t7+15-)		2.3		2.8		2.5	ns	5, 6, 7, 11	2, 14, 15	1, 16	8	3, 7, 11, 13	3, 11, 13	2, 14, 15
t_{pd}	Propagation Delay (t5-2+)		2.5		3.0		2.7	ns	5	2	1, 16	8	3		2
t_{pd}	Propagation Delay (t5-2-)(t6-14+)(t7-15-)		2.6		3.1		2.8	ns	5, 6, 7	2, 14, 15	1, 16	8	13	3, 11	2, 14, 15
t_{pd}	Propagation Delay (t13-14+)(t11-15-)		2.1		2.6		2.3	ns	11, 13	14, 15	1, 16	8	6	7	14, 15
t_{pd}	Propagation Delay (t6-14-)		2.7		3.2		2.9	ns	6	14	1, 16	8		13	14
t_{pd}	Propagation Delay (t7-15-)		2.6		3.1		2.7	ns	7	15	1, 16	8	11		15

NOTE This table is for DIL only.

MOTOROLA

Bi-Quinary Counter

Military 1678

ELECTRICALLY TESTED PER:
MPG 1678 (– 30°C to + 85°C)

The 1678 is a 4-bit counter capable of divide-by-two, divide-by-five, or divide-by-10 function. When used independently, the divide-by-two section will toggle at 350 MHz typically, while the divide-by-five section will toggle at 325 MHz typically. Clock inputs trigger on the positive going edge of the clock pulse.

Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

- DC Input Factor
  - R 2.40
  - Clk 0.77
  - C2 1.23
  - S 1.00
- Power Dissipation = 750 mW typ
- f_{Tog} = 350 MHz typ

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1678/BXA *
X = CASE OUTLINE AS FOLLOWS:

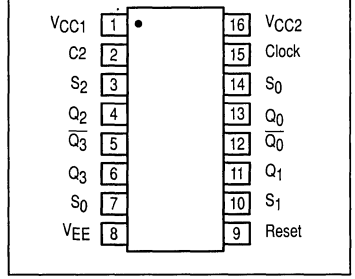
PACKAGE: CERDIP: E

*** 883 Processing (Non-Compliant)**

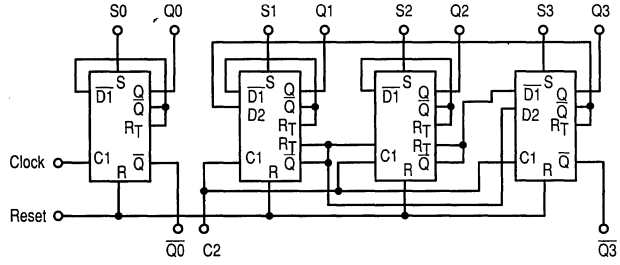
ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage (V_{CC} = 0)	V_{CC}	– 8.0	0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{IN}	0	V_{EE}	Vdc
Storage Temperature Range	T_{stg}	– 55	+ 125	°C
Operating Temperature Range	T_A	– 30	+ 85	°C

PIN ASSIGNMENTS

FUNCTION	DIL	BURN-IN (CONDITION C)
V_{CC1}	1	GND
C2	2	OPEN
S_2	3	GND
Q_2	4	51 Ω to V_{TT}
$\overline{Q_3}$	5	51 Ω to V_{TT}
Q_3	6	51 Ω to V_{TT}
S_3	7	GND
V_{EE}	8	V_{EE}
Reset	9	OPEN
S_1	10	GND
Q_1	11	51 Ω to V_{TT}
Q_0	12	51 Ω to V_{TT}
$\overline{Q_0}$	13	51 Ω to V_{TT}
S_0	14	GND
Clock	15	OPEN
V_{CC2}	16	GND



LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

TRUTH TABLE

$\overline{D}$	C	S	R	Q	$\overline{Q}$
0	0	0	0	Q_{n+1}	$\overline{Q}_{n+1}$
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	•	•
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	•	•
1	0	0	0	Q_{n+1}	$\overline{Q}_{n+1}$
1	0	0	1	0	1
1	0	1	0	1	0
1	0	1	1	•	•
1	1	0	0	0	1
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	•	•

• Output State Undefined

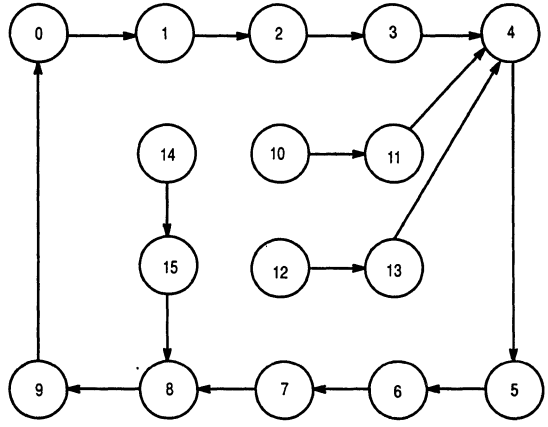
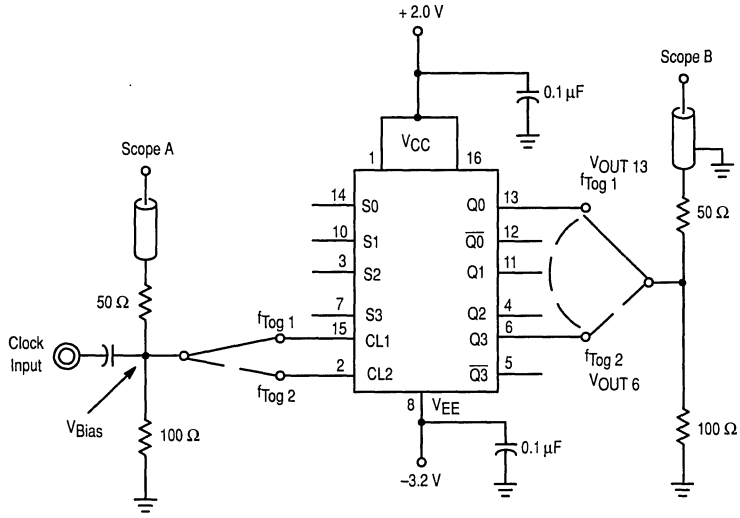


Figure 1. State Diagram



NOTES
1. Sine Wave generator AC coupled HP3200B or equivalent.
2. V_{OUT} = 600 mV min. peak to peak. Output at scope will be ½ actual at V_{IN}.
3. CP = Sine Wave

Figure 2. Toggle Frequency Test Circuit

Temp.	25°C	85°C	– 30°C
V_{OUT} 13	150	135	135
V_{OUT} 6	55	50	50

All in MHz min.

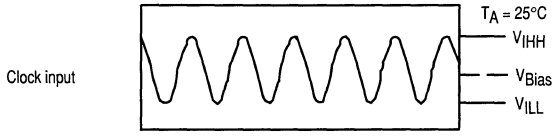


Figure 3. Toggle Frequency Waveform

Temp.	25°C	85°C	– 30°C
V_{IHH}	1.11 V	1.185 V	1.041 V
V_{ILL}	0.31 V	0.337 V	0.285 V
V_{BIAS}	0.70 V	0.76 V	0.65 V

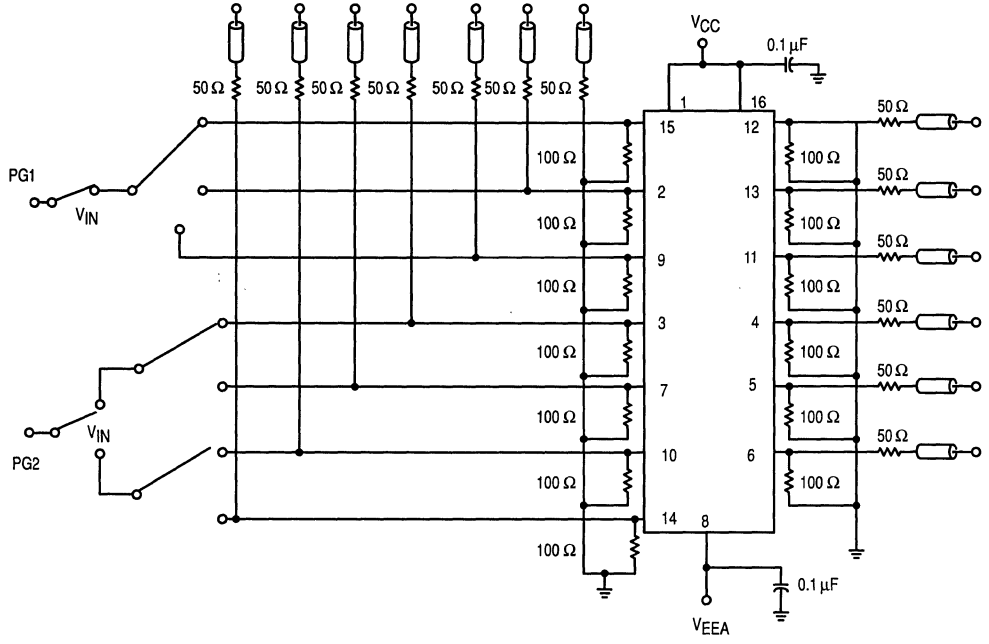
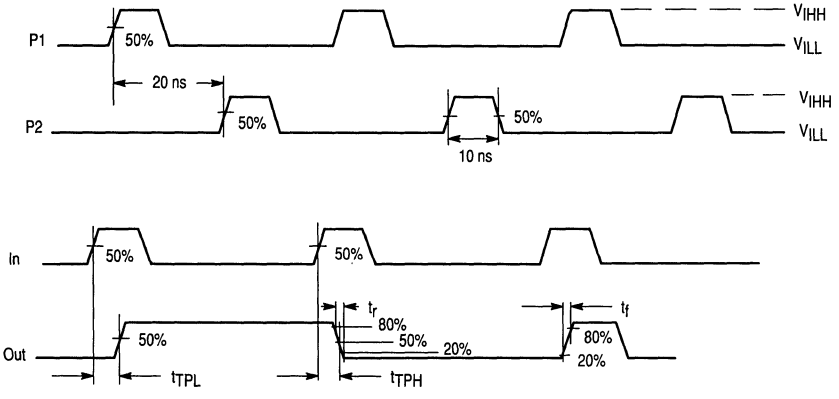


Figure 4. Switching Test Circuit



NOTES

1. $t_r = t_f = 1.5$ ns ± 0.2 ns.
2. $f_{req} = 25$ MHz.

Figure 5. Setup and Hold Waveforms

Temp.	25°C	85°C	– 30°C
V_{IHH}	1.11 V	1.185 V	1.04 1V
V_{ILL}	0.31 V	0.337 V	0.285 V

1678
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0.0 V, Output Load = 50 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_R	V_{CC}	V_{EE}	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V	3, 7, 9, 10, 14				4 - 6, 11 - 13	1, 16	8	4 - 6, 11 - 13
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V	7, 9, 10, 14				4 - 6, 11 - 13	1, 16	8	4 - 6, 11 - 13
V_{OHA}	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V	10		3, 7, 9, 10, 14	7, 9, 14	4 - 6, 11 - 13	1, 16	8	4 - 6, 11 - 13
V_{OLA}	Low Output Voltage	- 1.85	- 1.60	- 1.83	- 1.555	- 1.89	- 1.63	V	10		7, 9, 14	3, 7, 9, 10, 14	4 - 6	1, 16	8	4 - 6
I_{EE}	Power Supply Drain Current	- 200						mA	2, 3, 7, 9, 10, 14, 15					1, 16	8	8
I_{INH1}	Input Current High		450					µA	3, 7, 10, 14, 15					1, 16	8	3, 7, 9, 10, 14, 15
I_{INH2}	Input Current High		700					µA	2					1, 16	8	2
I_{INH3}	Input Current High		1.0					mA	9					1, 16	8	9
I_{INL}	Input Current Low	0.5						µA		2, 3, 7, 9, 10, 14, 15				1, 16	8	2, 3, 7, 9, 10, 14, 15

CAUTION: This device dissipates 750 to 900 mW of power. Use heat sink if operating over 50 seconds at $T_A \geq 25°C$.

1678
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}	V_{CC}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+5.0
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+5.0
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+5.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEA}	C_{P1-2}	P.U.T.
t_{TLH}	Rise Time		2.7		3.1		2.9	ns	14	12, 13	1, 16	8		12, 13
t_{THL}	Fall Time		2.6		3.0		2.8	ns	14	12, 13	1, 16	8		12, 13
t_{pd}	Propagation Delay C1 Limits		2.7		3.1		2.9	ns	14	12, 13	1, 16	8		12, 13
t_{pd}	Propagation Delay C2 Limits		3.0		3.4		3.2	ns	2	4, 5, 6, 11	1, 16	8		4, 5, 6, 11
t_{Set}	Set Limits		3.7		4.1		3.9	ns	3, 7, 9, 10, 14	4 - 6, 6 - 13	1, 16	8		4 - 6, 6 - 13
t_{Reset}	Reset Limits		4.5		4.9		3.9	ns	3, 7, 9, 10, 14	4 - 6, 6 - 13	1, 16	8		4 - 6, 6 - 13
f_{Tog1}	Toggle Frequency ÷by 2	300		270		260		MHz			1, 16	8	15	
f_{Tog2}	Toggle Frequency ÷by 5	275		250		250		MHz			1, 16	8	3	

* Temperature limits are guaranteed but not tested.

MOTOROLA

UHF Prescaler Type D Flip-Flop

ELECTRICALLY TESTED PER:
MPG 1690 (– 30°C to + 85°C)

- P_D = 220 mW typ/pkg (No Load)
- f_{Tog} = 500 MHz min.

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage (V_{CC} = 0)	V_{CC}	– 8.0	0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{IN}	0	V_{EE}	Vdc
Output Source Current Continuous	I_O		< 40	mAdc
Storage Temperature Range	T_{stg}	– 55	+ 125	°C
Operating Temperature Range	T_A	– 30	+ 85	°C

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CC1}	1	5	GND
Q	2	6	51 Ω to V_{TT}
$\overline{Q}$	3	7	51 Ω to V_{TT}
NC	4	8	OPEN
NC	5	9	OPEN
NC	6	10	OPEN
C_1	7	11	OPEN
V_{EE}	8	12	V_{EE}
C_2	9	13	OPEN
NC	10	14	OPEN
D_1	11	15	OPEN
D_2	12	16	OPEN
NC	13	1	OPEN
NC	14	2	OPEN
NC	15	3	OPEN
V_{CC2}	16	4	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

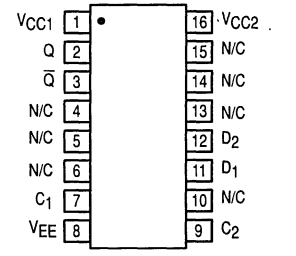
Military 1690

AVAILABLE AS

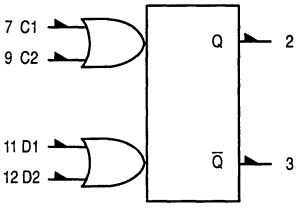
1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1690/BXA *
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F

*** 883 Processing (Non-Compliant)**



LOGIC DIAGRAM

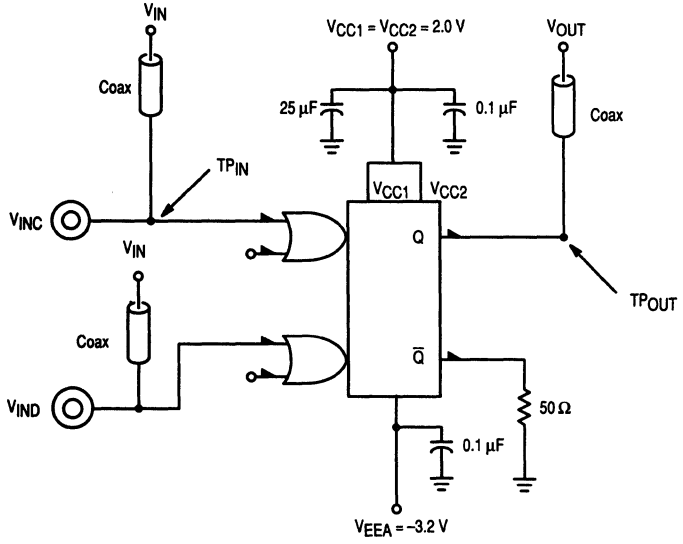


4

TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	ϕ	Q_n
⌐	L	L
⌐	H	H

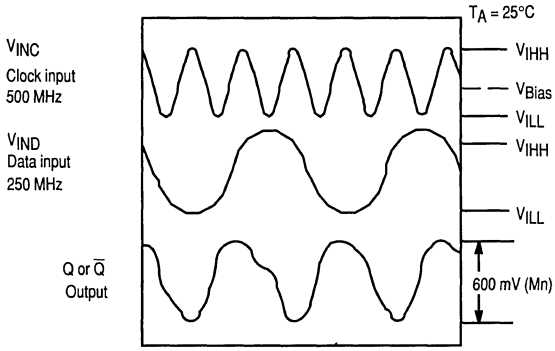
C = C1 + C2
D = D1 + D2
ϕ = Don't Care



NOTES
1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
2. 50 Ω termination to ground located in each scope channel.

Figure 1. Toggle Frequency Test Circuit

Temp.	25°C	85°C	−30°C
V_{ILL}	0.31 V	0.337 V	0.285 V
V_{IHH}	1.11 V	1.185 V	1.041 V



NOTES

1. The maximum toggle frequency of the device has be exceeded when either:
   a) The output peak to peak voltage swing falls below 600 mV, or
   b) The device ceases to toggle (divide by two).

Figure 2. Toggle Frequency Waveforms

4

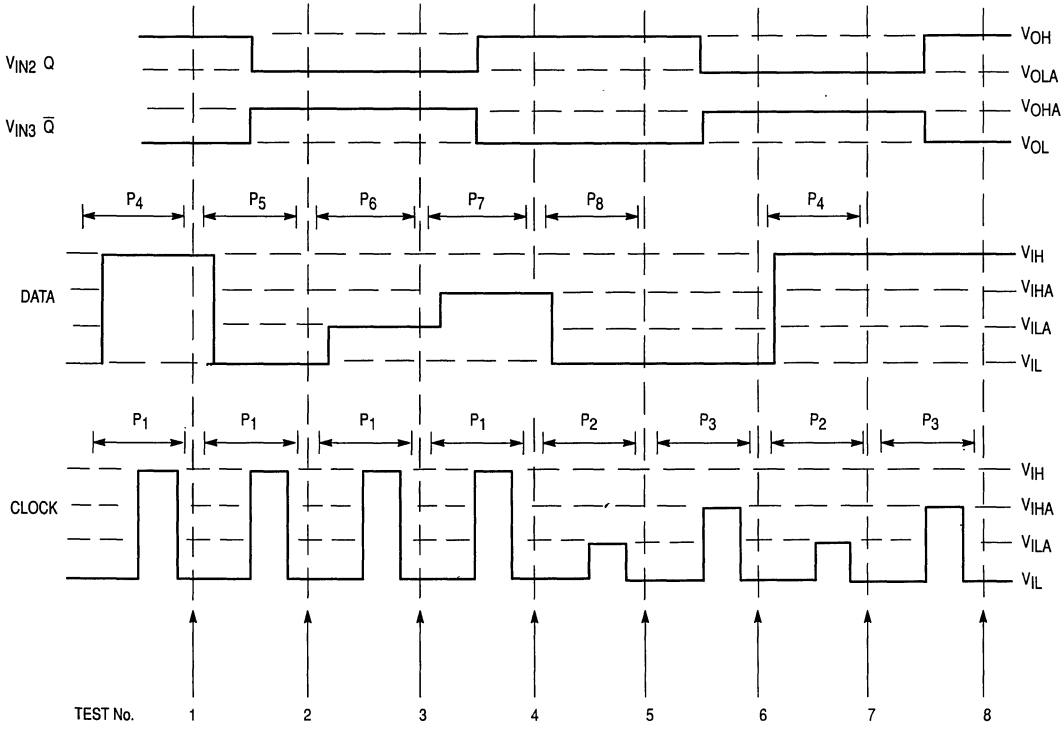


Figure 3. Clocking Sequence

1690
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}
T_A = 25 °C	-0.81	-1.95	-1.13	-1.48	-5.2	-3.2
T_A = 85 °C	-0.70	-1.95	-1.07	-1.44	-5.2	-3.2
T_A = -30 °C	-0.875	-1.95	-1.17	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0.0 V, Output Load = 50 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	P_A	P_{1-8}	V_{CC}	V_{EE}	P.U.T.
V_{OH}	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V	7, 11	12	7		1, 16	8	2, 3
V_{OL}	Low Output Voltage	- 1.95	- 1.63	- 1.95	- 1.60	- 1.95	- 1.63	V	9, 12	12	9		1, 16	8	2, 3
V_{OHA}	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V	11	11		7, 11	1, 16	8	2, 3
V_{OLA}	Low Output Voltage	- 1.95	- 1.63	- 1.95	- 1.60	- 1.95	- 1.63	V	12	12		9, 12	1, 16	8	2, 3
I_{EE}	Power Supply Drain Current	-59		-65		-65		mA	7, 9, 11, 12				1, 16	8	8
I_{INH1}	Input Current High		260		400		400	µA	7, 9				1, 16	8	7, 9
I_{INH2}	Input Current High		280		435		435	µA	11, 12				1, 16	8	11, 12
I_{INL}	Input Current Low	0.5		0.3		0.5		µA		7, 9, 11, 12			1, 16	8	7, 9, 11, 12

* For P1 - P8 refer to figure 3.

1690
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}
T_A = 25 °C	-0.81	-1.95	-1.13	-1.48	-5.2	-3.2
T_A = 85 °C	-0.70	-1.95	-1.07	-1.44	-5.2	-3.2
T_A = -30 °C	-0.875	-1.95	-1.17	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{CC}	V_{EEA}	P.U.T.
t_{TLH}	Rise Time		1.3					ns	7, 11	2	1, 16	8	2
t_{THL}	Fall Time		1.3					ns	7, 11	2	1, 16	8	2
t_{pd}	Propagation Delay		1.5					ns	7, 11	2	1, 16	8	2
t_{setup}	Setup Time		0.3					ns	7, 11	2	1, 16	8	2
t_{Hold}	Hold Time		0.3					ns	7, 11	2	1, 16	8	2
f_{Tog}	Toggle Frequency	500		500		500		MHz	7, 11	2	1, 16	8	2

MOTOROLA

Quad Line Receiver with Bias Driver

Military 1692

ELECTRICALLY TESTED PER:
MPG 1692 (– 30°C to + 85°C)

- P_D = 220 mW typ/pkg
- t_{pd} = 0.9 ns typ (510 ohm load)
  = 1.1 ns typ (50 ohm load)
- Full Load Current, I_L = – 25 mAdc max

ABSOLUTE MAXIMUM RATINGS:	Symbol	Min	Max	Unit
Power Supply Voltage (V_{CC} = 0)	V_{CC}	– 8.0	0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{IN}	0	V_{EE}	Vdc
Output Source Current Continuous	I_O		< 40	mAdc
Storage Temperature Range	T_{stg}	– 65	+ 165	°C
Operating Temperature Range	T_A	– 30	+ 85	°C

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: N/A
4) 1692/BXA *
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F

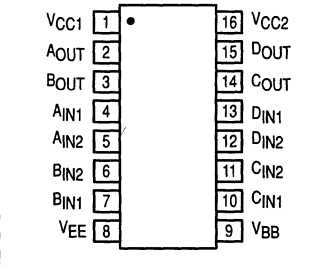
*** 883 Processing (Non-Compliant)**

4

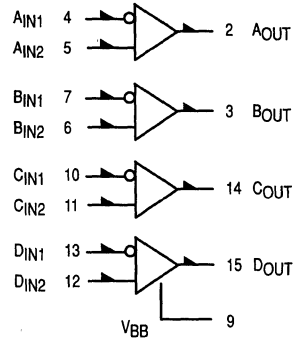
PIN ASSIGNMENTS

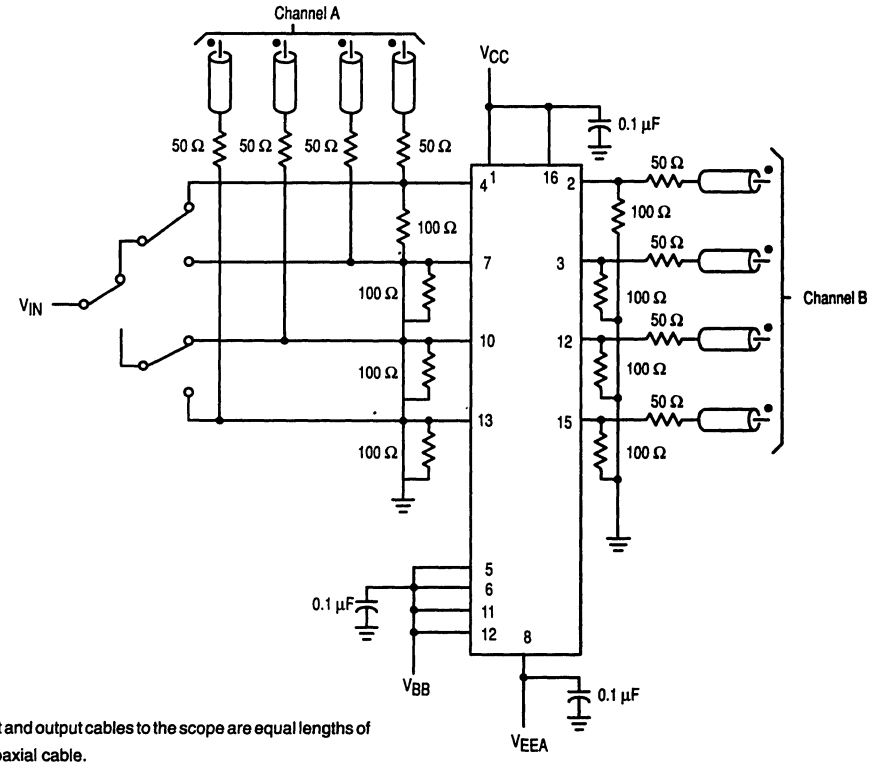
FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CC1}	1	5	GND
A_{OUT}	2	6	51 Ω to V_{TT}
B_{OUT}	3	7	51 Ω to V_{TT}
A_{IN1}	4	8	V_{BB}
A_{IN2}	5	9	GND
B_{IN2}	6	10	GND
B_{IN1}	7	11	V_{BB}
V_{EE}	8	12	V_{EE}
V_{BB}	9	13	V_{BB}
C_{IN1}	10	14	V_{BB}
C_{IN2}	11	15	GND
D_{IN2}	12	16	GND
D_{IN1}	13	1	V_{BB}
C_{OUT}	14	2	51 Ω to V_{TT}
D_{OUT}	15	3	51 Ω to V_{TT}
V_{CC2}	16	4	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



LOGIC DIAGRAM





NOTES

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
2. Input Generator = EH137 or equivalent.
3. $t_r = t_f = 1.5$ ns ± 0.2 ns.
4. Frequency = 20 MHz.
5. 50% duty cycle.
6. Pulse Amp. = 0.8 Vdc.
7. DC level = + 0.71 Vdc.

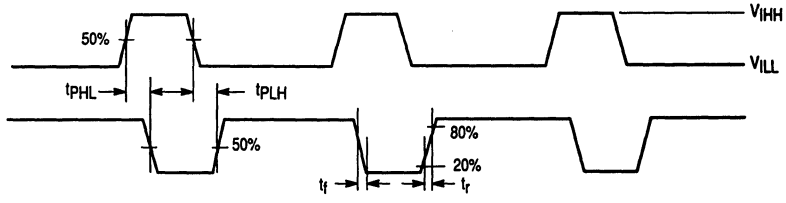


Figure 1. Test Circuit and Waveforms

Temp.	25°C	85°C	– 30°C
V_{ILL}	0.31 V	0.337 V	0.285 V
V_{IHH}	1.11 V	1.185 V	1.041 V

1692
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEA}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0.0 V, Output Load = 50 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{BB}	V_{CC}	V_{EE}	P.U.T.
V_{OH}	High Output Voltage	- 0.96	- 0.81	- 0.89	- 0.7	- 1.045	- 0.875	V	4, 7, 10, 13	4, 7, 10, 13			5, 6, 11, 12	1, 16	8	2, 3, 14, 15
V_{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.83	- 1.575	- 1.89	- 1.65	V	4, 7, 10, 13	4, 7, 10, 13			5, 6, 11, 12	1, 16	8	2, 3, 14, 15
V_{OHA}	High Output Voltage	- 0.98	- 0.81	- 0.91	- 0.7	- 1.065	- 0.875	V		4, 7, 10, 13		4, 7, 10, 13	5, 6, 11, 12	1, 16	8	2, 3, 14, 15
V_{OLA}	Low Output Voltage	- 1.85	- 1.60	- 1.83	- 1.555	- 1.89	- 1.63	V		4, 7, 10, 13	4, 7, 10, 13		5, 6, 11, 12	1, 16	8	2, 3, 14, 15
V_{BB1}	Reference Voltage	- 1.35	- 1.25	- 1.295	- 1.95	- 1.4	- 1.3	V					5, 6, 11, 12	1, 16	8	9
I_{EE}	Power Supply Drain Current	- 50						mA		4, 7, 10, 13			5, 6, 11, 12	1, 16	8	8
I_{IN}	Input Current High		250					µA	4, 7, 10, 13	4, 7, 10, 13			4 - 7, 10 - 13	1, 16	8	4 - 7, 10 - 13
I_R	Input Current High	- 100	100					µA		4, 7, 10, 13			4 - 7, 10 - 13	1, 16	8	4 - 7, 10 - 13

1692
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)						
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{EE}	V_{EEL}	V_{CC}
T_A = 25 °C	-0.81	-1.85	-1.095	-1.485	-5.2	-3.2	+2.0
T_A = 85 °C	-0.70	-1.83	-1.025	-1.440	-5.2	-3.2	+2.0
T_A = -30 °C	-0.875	-1.89	-1.180	-1.515	-5.2	-3.2	+2.0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 85 °C		- 30 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{IN}	V_{OUT}	V_{BB}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH}	Rise Time	0.6	2.1	0.6	2.3	0.6	2.2	ns	4 - 7, 10, 13	2, 3, 14, 15	5, 6, 11, 12	1, 16	8	2, 3, 14, 15
t_{THL}	Fall Time	0.6	2.1	0.6	2.3	0.6	2.2	ns	4 - 7, 10, 13	2, 3, 14, 15	5, 6, 11, 12	1, 16	8	2, 3, 14, 15
t_{pd}	Propagation Delay High to Low	0.6	1.7	0.6	1.9	0.6	1.8	ns	4 - 7, 10, 13	2, 3, 14, 15	5, 6, 11, 12	1, 16	8	2, 3, 14, 15
t_{pd}	Propagation Delay Low to High	0.6	1.5	0.6	1.7	0.6	1.6	ns	4 - 7, 10, 13	2, 3, 14, 15	5, 6, 11, 12	1, 16	8	2, 3, 14, 15

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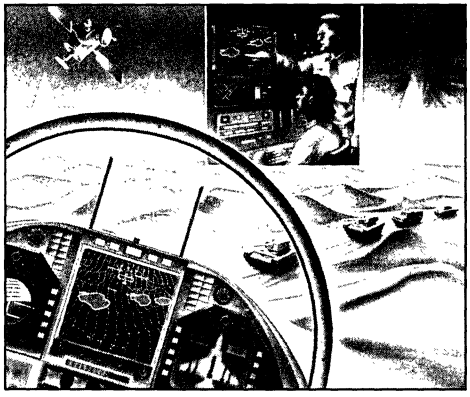


ECLinPS 5

MOTOROLA

8-Bit Synchronous Binary Up Counter

Military 10E416

Product Preview

ELECTRICALLY TESTED PER:
10E416

The 10E416 is a high-speed synchronous, presettable, cascadable 8-bit binary counter. Architecture and operation are the same as the 10H416 in the MECL 10H family, extended to 8-bits, as shown in the logic diagram.

The counter features internal feedback of $\overline{TC}$, gated by the TCLD (terminal count load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with TC going LOW to indicate an all-one state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically reload upon $\overline{TC}$ = LOW, thus functioning as a programmable counter.

- 700 MHz Min. Count Frequency
- 1000 ps CLK to Q, $\overline{TC}$
- Internal $\overline{TC}$ Feedback (Gated)
- 8-Bit
- Fully Synchronous Counting and $\overline{TC}$ Generation
- Asynchronous Master Reset
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

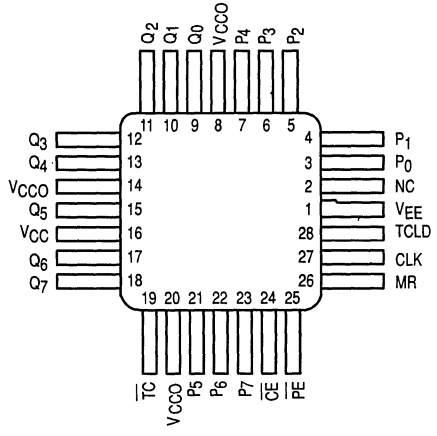
1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: F

5

PIN NAME

Pin	Function
P_0 - P_7	Parallel Data (Preset) Data
Q_0 - Q_7	Data Outputs
$\overline{CE}$	Count Enable Control Input
$\overline{PE}$	Parallel Load Enable Control Input
MR	Master Reset
CLK	Clock
$\overline{TC}$	Terminal Count Output
TCLD	TC - Load Control Input



FUNCTION TABLE

$\overline{CE}$	$\overline{PE}$	TCLD	MR	CLK	Function
X	L	X	L	⌐	Load Parallel (P_n to Q_n)
L	H	L	L	⌐	Continuous Count
L	H	H	L	⌐	Count: Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	⌐	Hold
X	X	X	L	⌙	Master Respond, Slaves Hold
X	X	X	H	⌐	Reset (Q_n: = LOW, $\overline{TC}$: = HIGH)

⌐ = clock pulse (low to high)
⌙ = clock pulse (high to low)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; $V_{CC} = V_{CCO}$ = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input Current High		150		150		150	µA	
I_{EE}	Power Supply Current		181		181		181	mA	

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AC CHARACTERISTICS: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{count}	Maximum Count Frequency	700		700		700		MHz	
t_{PLH}	Propagation Delay to Output								
t_{PHL}	CLK to Q	600	1000	600	1000	600	1000	ps	
	MR to Q	600	1000	600	1000	600	1000	ps	
	CLK to $\overline{TC}$ (Q's loaded)	550	1050	550	1050	550	1050	ps	(Note 1)
	CLK to $\overline{TC}$ (Q's unloaded)	550	900	550	900	550	900	ps	(Note 1)
	MR to $\overline{TC}$	625	1000	625	1000	625	1000	ps	
t_S	Setup Time								
	Pn	150		150		150		ps	
	CE	600		600		600		ps	
	PE	600		600		600		ps	
	TCLD	500		500		500		ps	
t_H	Hold Time								
	Pn	250		250		250		ps	
	CE	0		0		0		ps	
	PE	0		0		0		ps	
	TCLD	100		100		100		ps	
t_{RR}	Reset Recovery Time	900		900		900		ps	
t_{PW}	Minimum Pulse Width								
	CLK, MR	400		400		400		ps	
t_r t_f	Rise/Fall Times 20 - 80%	300	800	300	800	300	800	ps	

1. CLK to $\overline{TC}$ propagation delay is dependent on the loading of the Q outputs. With all of the Q outputs loaded the noise generated in going from a IIII IIII state to a 0000 0000 state causes the CLK to $\overline{TC}$+ delay to increase.

5

MOTOROLA

4-Input Quad OR/NOR Gate

Product Preview

ELECTRICALLY TESTED PER:
10E501

The 10E501 is a quad 4-Input **OR/NOR** gate.

- 500 ps Max. Propagation Delay
- 75 kΩ Input Pulldown Resistors

PIN NAME

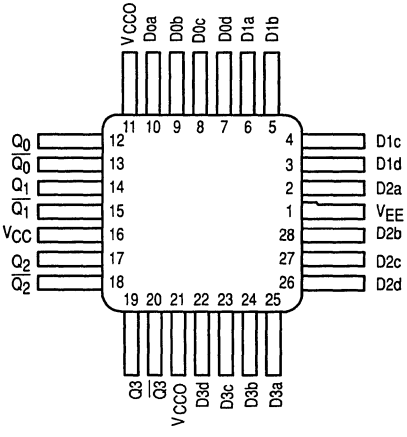
Pin	Function
D_{0a} - D_{3d}	Data Inputs
Q_0 - Q_3	True Outputs
$\overline{Q_0}$ - $\overline{Q_3}$	Inverting Outputs

Military 10E501

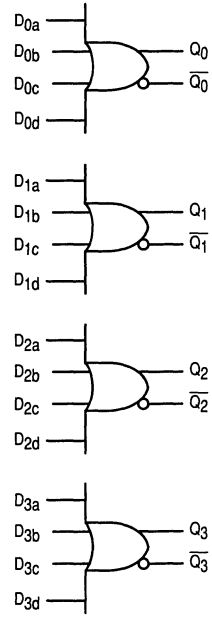
AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X



LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input Current High D		150		150		150	µA	
I_{EE}	Power Supply Current		36		36		36	mA	

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AC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	200	500	200	500	200	500	ps	
t_{Skew}	Within-device Skew		50		50		50	ps	(Note 1)
t_{Skew}	Within-Gate Skew		25		25		25	ps	(Note 2)
t_r t_f	Rise/Fall Times 20 - 80%	300	575	300	575	300	575	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Within-gate skew is defined as the variation in propagation delays of a gate when driven from its different inputs.

MOTOROLA

Quint 2-Input AND/NAND Gate

Military 10E504

Product Preview

ELECTRICALLY TESTED PER:
10E504

The 10E504 is a quint 2-input **AND/NAND** gate. The function output F is the OR of all five AND gate outputs, while $\overline{F}$ is the NOR. The Q outputs need not be terminated if only the F outputs are to be used.

- 600 ps Max. Propagation Delay
- OR/NOR Function Outputs
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

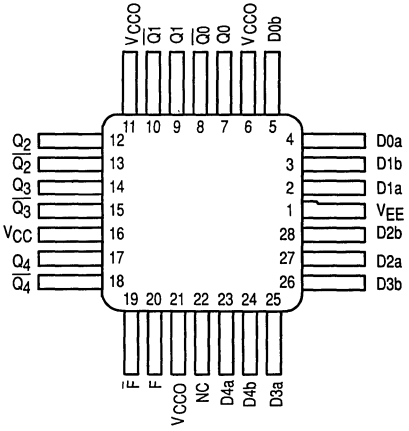
PIN NAME

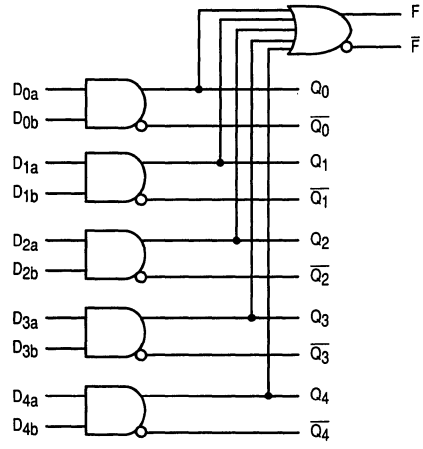
Pin	Function
D_{0a} - D_{4b}	Data Inputs
Q_0 - Q_4	AND Outputs
$\overline{Q_0}$ - $\overline{Q_4}$	NAND Outputs
F	OR Output
$\overline{F}$	NOR Output

FUNCTION OUTPUTS

$$F = (D_{0a} \bullet D_{0b}) + (D_{1a} \bullet D_{1b}) + (D_{2a} \bullet D_{2b}) + (D_{3a} \bullet D_{3b}) + (D_{4a} \bullet D_{4b})$$

LOGIC DIAGRAM





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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		200		200		200	µA	
I_{EE}	Power Supply Current		46		46		46	mA	

5

AC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D to Q	225	600	225	600	225	600	ps	
	D to F	500	1000	500	1000	500	1000	ps	
t_{Skew}	Within-device Skew								
	D to Q	75		75		75		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%								
	Q	275	700	275	700	275	700	ps	
	F	300	700	300	700	300	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

MOTOROLA

Quint 2-Input XOR/XNOR Gate

Military 10E507

Product Preview

ELECTRICALLY TESTED PER:
10E507

The 10E507 is a quint 2-input **XOR/XNOR** gate. The function output F is the OR of all five XOR outputs, while $\overline{F}$ is the NOR. The Q outputs need not be terminated if only the F outputs are to be used.

- 600 ps Max. Propagation Delay
- OR/NOR Function Outputs
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

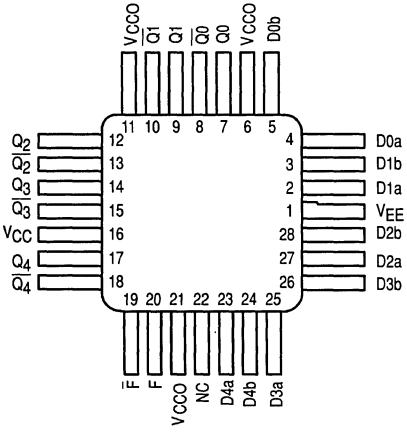
PACKAGE: NON-Compliant
QFP: X

PIN NAME

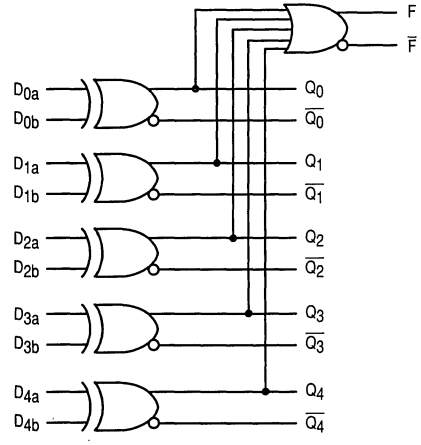
Pin	Function
D_{0a} - D_{4b}	Data Inputs
Q_0 - Q_4	XOR Outputs
$\overline{Q_0}$ - $\overline{Q_4}$	XNOR Outputs
F	OR Output
$\overline{F}$	NOR Output

FUNCTION OUTPUTS

$$F = (D_{0a} \oplus D_{0b}) + (D_{1a} \oplus D_{1b}) + (D_{2a} \oplus D_{2b}) + (D_{3a} \oplus D_{3b}) + (D_{4a} \oplus D_{4b})$$



LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		200		200		200	µA	
I_{EE}	Power Supply Current		50		50		50	mA	

AC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D to Q	250	600	250	600	250	600	ps	
	D to F	500	1000	500	1000	500	1000	ps	
t_{Skew}	Within-device Skew								
	D to Q	75		75		75		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%								
	Q	275	700	275	700	275	700	ps	
	F	300	700	300	700	300	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

MOTOROLA

1:9 Differential Clock Driver

Product Preview

ELECTRICALLY TESTED PER:
10E511

Military 10E511

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: F

The 10E511 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. It accepts one signal input, which can be either differential or else single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs. An enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

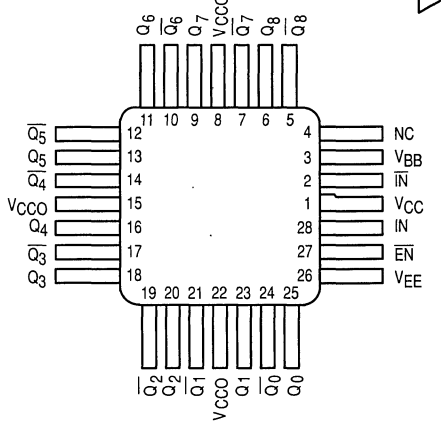
To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i. e. sharing the same V_{CCO}) as the pairs(s) being used on the same side, in order to maintain minimum skew. Failure to do this will result in small degradation of propagation delay (on the order of 10-20 ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When used for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01 μF capacitor.

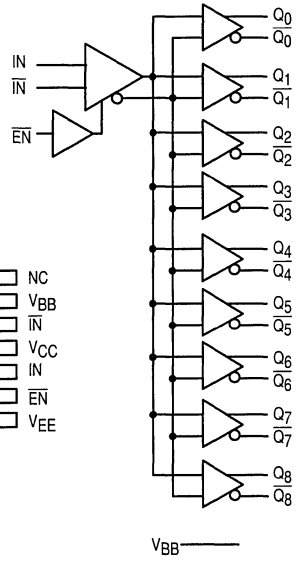
- Low Skew
- Guaranteed Skew Spec
- Differential Design
- V_{BB} output
- Enable
- 75 kΩ Input Pulldown Resistors

PIN NAME

Pin	Function
IN, $\overline{IN}$	Differential Input Pair
En	Enable
Q_0, $\overline{Q_0}$ - Q_8, $\overline{Q_8}$	Differential Outputs
V_{BB}	V_{BB} Outputs



LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; $V_{CC} = V_{CCO}$ = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
V_{BB}	Output Reference Voltage	-1.35	-1.25	-1.31	-1.19	-1.38	-1.27	V	V_{IL} = Open, V_{IH} = Open, R_L = 50Ω to – 2.0 V.
I_{IH}	Input Current High		150		150		150	µA	V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.
I_{EE}	Power Supply Current		60		60		60	mA	V_{EE} (MAX), V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.

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AC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay to Output								
t_{PHL}	IN (differential)	430	630	430	630	430	630	ps	(Note 1)
	IN (Single-ended)	330	730	330	730	330	730	ps	(Note 2)
	Enable	450	850	450	850	450	850	ps	(Note 3)
	Disable	450	850	450	850	450	850	ps	(Note 3)
t_{Skew}	Within-Device Skew		50		50		50	ps	(Note 4)
t_S	Setup Time $\overline{En}$ to IN	200		200		200		ps	(Note 5)
t_H	Hold Time IN to $\overline{En}$	0		0		0		ps	(Note 6)
t_R	Release Time $\overline{En}$ to IN	300		300		300		ps	(Note 7)
V_{PP}	Minimum Input Swing	250		250		250		mV	(Note 8)
V_{CMR}	Common Mode Range	-1.6	-0.4	-1.6	-0.4	-1.6	-0.4	V	(Note 9)
t_r t_f	Rise/Fall Times 20 - 80%	275	600	275	600	275	600	ps	

See Notes on following page.

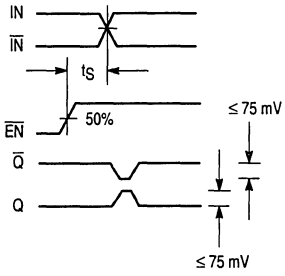

Figure 1. Setup Time

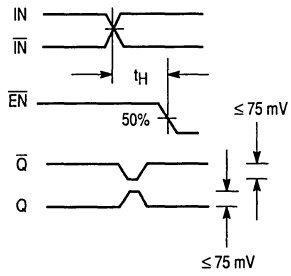

Figure 2. Hold Time

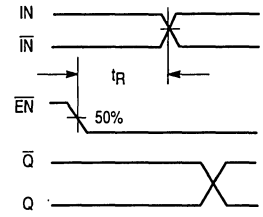

Figure 3. Release Time

Notes

1. The differential propagation is defined as the delay from the crossing points of the differential input signals to the crossing point of differential output signals. (See *Definitions and testing ECLinPS AC Parameters* in Section 1.)
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. (See *Definitions and testing ECLinPS AC Parameters* in Section 1.)
3. Enable is defined as the propagation delay from 50% point of the **negative** transition $\overline{EN}$ to the 50% point of the **positive** transition on Q (or a negative transition on $\overline{Q}$). Disable is defined as the propagation delay from 50% point of the **positive** transition on $\overline{EN}$ to the 50% point of the **negative** transition on Q (or a negative transition on $\overline{Q}$).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ± 75 mV to that IN/$\overline{IN}$ transition (see Figure 1).
6. The hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or a positive going $\overline{IN}$ to prevent an output response greater than ± 75 mV to that IN/$\overline{IN}$ transition (see Figure 2).
7. The release time is the minimum time that $\overline{EN}$ must be de-asserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. V_{PP} (min) is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min) is AC limited for the E511, a differential input as low as 50 mV will still produce full ECL levels at the output.
9. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP} (min). Measured output voltages must fall within the specified limits of V_{OH} and V_{OL} (V_{OH} = - 0.880 V max, - 1.090 V min, V_{OL} = - 1.580 V max, - 1.810 V min).

MOTOROLA

Quad Driver

Military 10E512

Product Preview

ELECTRICALLY TESTED PER:
10E512

The 10E512 is a quad driver with two pairs of OR/NOR outputs form each gate, and a common, buffered enable input. Using the data inputs the device can serve as an ECL memory address fan-out driver. Using just the enable input, the device serves as a clock driver, although the 10E511 is designed specifically for this purpose, and offers lower skew than the E512.

- 600 ps Max. Propagation Delay
- Common Enable Input
- 75 kΩ Input Pulldown Resistors

PIN NAME

Pin	Function
D_0 - D_3	Data Inputs
$\overline{EN}$	Enable Inputs
Q_{na} - Qnb	True Outputs
$\overline{Q_{na}}$ - $\overline{Qnb}$	Inverting Outputs

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

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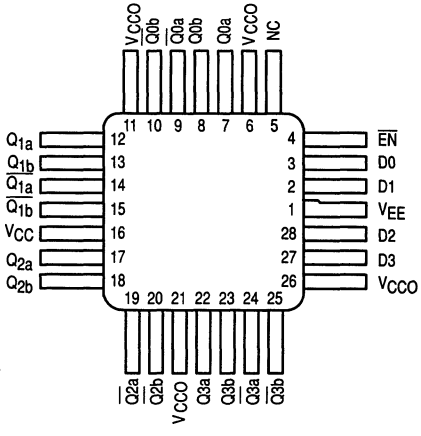
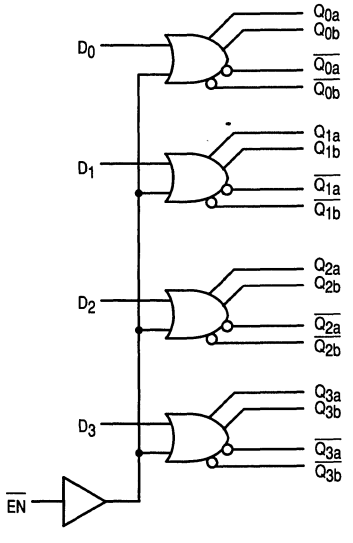


LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current								
	D		200		200		200	µA	
	$\overline{EN}$		150		150		150	µA	
I_{EE}	Power Supply Current		56		56		56	mA	

AC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D	200	600	200	600	200	600	ps	
	$\overline{EN}$	275	675	275	675	275	675	ps	
t_{Skew}	Within-device Skew								
	Dn to Qn, $\overline{Qn}$	80		80		80		ps	(Note 1)
	Dna to Qnb	40		40		40		ps	(Note 2)
t_r t_f	Rise/Fall Times 20 - 80%	275	700	275	700	275	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Skew defined between common OR or common NOR outputs of a single gate.

5

MOTOROLA

Quint Differential Line Receiver

Military 10E516

Product Preview

ELECTRICALLY TESTED PER:
10E516

The 10E516 is a quint differential line receiver with emitter-follower outputs. An internally generated reference supply (V_{BB}) is available for single-ended reception.

Active current sources plus a deep collector feature of the MOSAIC III process provide the receivers with excellent common-mode noise rejection. Each receiver has a dedicated V_{CCO} supply lead, providing optimum symmetry and stability.

The receiver design features clamp circuity to cause a defined state if both the inverting and non-inverting inputs are left open; in this case the Q output goes LOW, while the $\overline{Q}$ output goes HIGH. This feature makes the device ideal for twisted pair applications.

If both inverting and non-inverting inputs are at equal potential > -2.5 V, the receiver does not go to a defined state, but rather current-shares in normal differential amplifier fashion, producing output voltage levels midway between HIGH and LOW, or the device may even oscillate.

The device V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01μF capacitor.

The 10E516 features input pull-down resistors, as does the rest of the ECLinPS family.

AVAILABLE AS

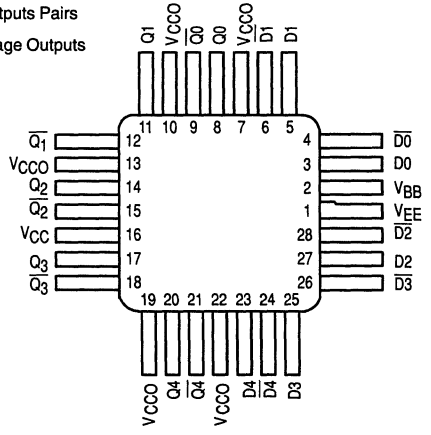
1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

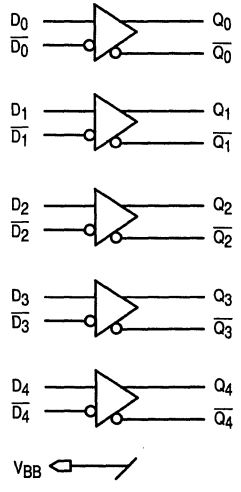
- 500 ps Max. Propagation Delay
- V_{BB} Supply Output
- Dedicated V_{CCO} Pin for Each Receiver
- 75 kΩ Input Pulldown Resistors

PIN NAME

Pin	Function
D_0, $\overline{D_0}$ - D_4, $\overline{D_4}$	Differential Inputs Pairs
Q_0, $\overline{Q_0}$ - Q_4, $\overline{Q_4}$	Differential Outputs Pairs
V_{BB}	Reference Voltage Outputs



LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; $V_{CC} = V_{CCO}$ = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		− 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
V_{BB}	Output Reference Voltage	-1.35	-1.25	-1.31	-1.19	-1.38	-1.27	V	
I_{IH}	Input High Current		200		200		200	µA	
I_{EE}	Power Supply Current		35		35		35	mA	
$V_{PP(DC)}$	Input Seneitivity	150		150		150		mV	(Note 1)
V_{CMR}	Common Mode Range	-2.0	-0.6	-2.0	-0.6	-2.0	-0.6	V	(Note 2)

1. V_{PP} is the minimum differential input voltage required to assure full ECL levels are present at the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing is greater than V_{PPMIN} and < 1.0 V.

AC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D	200	450	200	450	200	450	ps	
	D (SE)	150	500	150	500	150	500	ps	
$V_{PP(AC)}$	Minimum Input Swing	150		150		150		mV	(Note 1)
t_{Skew}	Within-device Skew								
	Dn to Qn, $\overline{Qn}$	50		50		50		ps	(Note 2)
t_{Skew}	Duty Cycle Skew								
	t_{PLH} - t_{PHL}	± 10		± 10		± 10		ps	(Note 3)
t_r t_f	Rise/Fall Times 20 - 80%	275	575	275	575	275	575	ps	

1. Minimum input swing for which AC parameters are guaranteed.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross points of the outputs.

5

MOTOROLA

4-Bit D Flip-Flop

Military 10E531

Product Preview

ELECTRICALLY TESTED PER:
10E531

The 10E531 is a quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock (C_C) LOW and using the Clock Enable ($\overline{CE}$) inputs for clocking. Common clocking is achieved by holding the $\overline{CE}$ inputs LOW and using C_C to clock all four flip-flops. In this case, the $\overline{CE}$ inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both C_C and $\overline{CE}$ are LOW, and transfers to the slave when either C_C or $\overline{CE}$ (or both) go HIGH.

- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

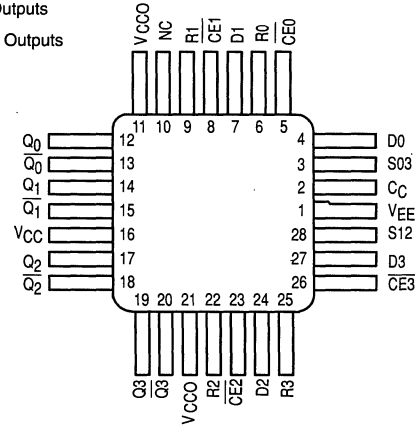
1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

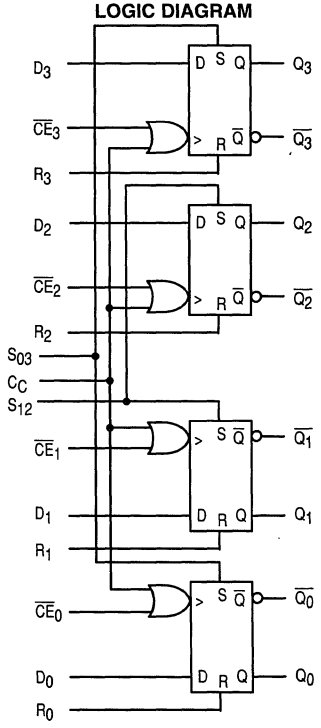
5

PIN NAME

Pin	Function
D_0 - D_3	Data Inputs
$\overline{CE_0}$ - $\overline{CE_3}$	Clock Enables (Individual)
R_0 - R_3	Resets
C_C	Common Clock
S_{03}, S_{12}	Sets (Paired)
Q_0 - Q_3	True Outputs
$\overline{Q_0}$ - $\overline{Q_3}$	Inverting Outputs



LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current							µA	
	C_C		350		350		350		
	S		450		450		450		
	R		300		300		300		
	$\overline{CE}$		300		300		300		
	D		150		150		150		
I_{EE}	Power Supply Current		70		70		70	mA	

5

AC CHARACTERISTICS: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Max. Toggle Frequency	1100		1100		1100		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output								
	$\overline{CE}$	360	700	360	700	360	700	ps	
	C_C	325	675	325	675	325	675	ps	
	R	350	725	350	725	350	725	ps	
	S	350	725	350	725	350	725	ps	
t_S	Setup Time								
	D	150		150		150		ps	(Note 2)
t_H	Hold Time								
	D	175		175		175		ps	(Note 2)
t_{RR}	Reset Recovery Time	400		400		400		ps	
t_{Skew}	Within-device Skew	60		60		60		ps	(Note 1)
t_{PW}	Minimum Pulse Width								
	Clk, S, R	400		400		400		ps	
t_r t_f	Rise/Fall Times 20 - 80%	300	675	300	675	300	675	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Setup/hold time guaranteed for both C_C & $\overline{CE}$.

5

MOTOROLA

8-Bit Shift Register

Military 10E541

Product Preview

ELECTRICALLY TESTED PER:
10E541

The 10E541 is an 8-bit full-function shift register. The 10E541 performs serial/parallel in and serial/parallel out, shifting in either direction. The eight inputs D_0-D_7 accept parallel input data, while DL/DR accept serial input data for left/right shifting.

The select pins, SEL0 and SEL1, select one of four modes of operation: Load, Hold, Shift Left, Shift Right, according to the Function Table.

Input data is accepted a set-up time before the positive clock edge. A HIGH on the Master Reset (MR) pin asynchronously resets all the registers to zero.

- 700 MHz Min. Shift Frequency
- 8-Bits
- Full-Function, Bi-directional
- Asynchronous Master Reset
- 75 kΩ Input Pulldown Resistors

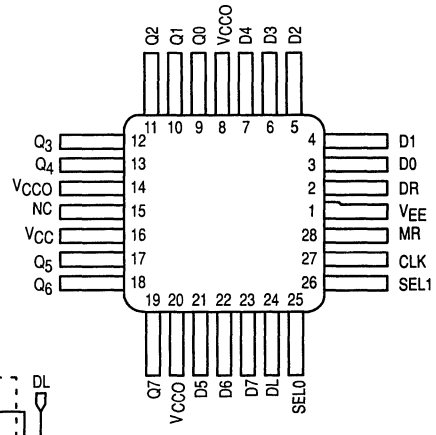
AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

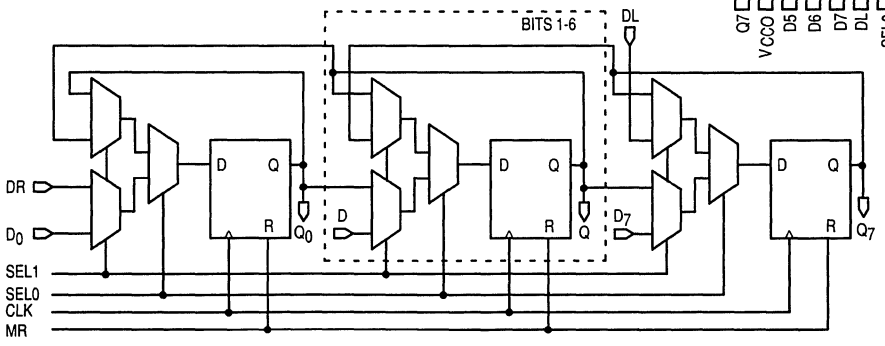
PACKAGE: NON-Compliant
QFP: X

PIN NAME

Pin	Function
D_0 - D_7	Parallel Data Inputs
DL, DR	Serial Data Inputs
SEL0, SEL1	Mode Select Inputs
CLK	Clock
Q_0 - Q_7	Data Outputs
MR	Master Reset



LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

Function Table		
SEL0	SEL1	Function
L	L	Load
L	H	Shift Right (Dn to D_{n+1})
H	L	Shift Left (Dn to D_{n-1})
H	H	Hold

Expanded Function Table														
Function	DL	DR	SEL0	SEL1	MR	CLK	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Load	X	X	L	L	L	Z	D0	D1	D2	D3	D4	D5	D6	D7
Shift Right	X	L	L	H	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	Q6
	X	H	L	H	L	Z	H	L	Q0	Q1	Q2	Q3	Q4	Q5
Shift Left	L	X	H	L	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	L
	H	X	H	L	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Hold	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Reset	X	X	X	X	H	X	L	L	L	L	L	L	L	L

5

DC CHARACTERISTICS: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		150		150		150	µA	
I_{EE}	Power Supply Current		157		157		157	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{Shift}	Max. Shift Frequency	700		700		700		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output								
	Clk	625	975	625	975	625	975	ps	
	MR	600	975	600	975	600	975	ps	
t_S	Setup Time								
	D	175		175		175		ps	
	SEL0	350		350		350		ps	
	SEL1	300		300		300		ps	
t_H	Hold Time								
	D	200		200		200		ps	
	SEL0	100		100		100		ps	
	SEL1	100		100		100		ps	
t_{RR}	Reset Recovery Time	900		900		900		ps	
t_{PW}	Minimum Pulse Width								
	Clk, MR	400		400		400		ps	
t_{Skew}	Within-device Skew	60		60		60		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	300	800	300	800	300	800	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

5

MOTOROLA

9-Bit Shift Register

Military 10E542

Product Preview

ELECTRICALLY TESTED PER:
10E542

The 10E542 is a 9-bit shift register, designed with byte-parity applications in mind. The 10E542 performs serial/parallel in and serial/parallel out, shifting in one direction. The nine inputs D_0-D_8 accept parallel input data, while S-IN accepts serial input data.

The SEL (Select) input pin is used to switch between the two modes of operation –SHIFT and LOAD. The shift direction is from bit 0 to bit 8. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

- 700 MHz Min. Shift Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

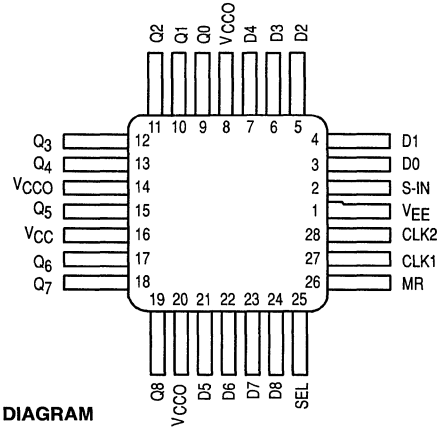
5

PIN NAME

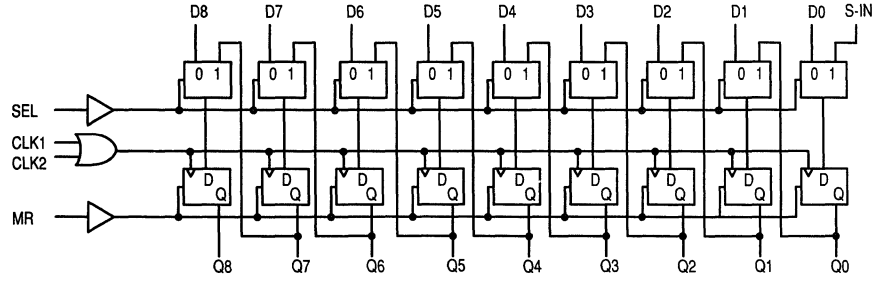
Pin	Function
D_0 - D_8	Parallel Data Inputs
S-IN	Serial Data Input
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q_0 - Q_8	Data Outputs

Function Table

SEL	Mode
L	LOAD
H	SHIFT



LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; $V_{CC} = V_{CCO}$ = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		150		150		150	µA	
I_{EE}	Power Supply Current		145		145		145	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{SHIFT}	Max. Shift Frequency	700		700		700		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output								
	Clk	600	1000	600	1000	600	1000	ps	
	MR	600	1000	600	1000	600	1000	ps	
t_S	Setup Time								
	D	50		50		50		ps	
	SEL	300		300		300		ps	
t_H	Hold Time								
	D	300		300		300		ps	
	SEL	75		75		75		ps	
t_{RR}	Reset Recovery Time	900		900		900		ps	
t_{PW}	Minimum Pulse Width								
	Clk, MR	400		400		400		ps	
t_{Skew}	Within-device Skew	75		75		75		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	300	800	300	800	300	800	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

5

MOTOROLA

9-Bit Hold Register

Military 10E543

Product Preview

ELECTRICALLY TESTED PER:
10E543

The 10E543 is a 9-bit holding register, designed with byte-parity applications in mind. The 10E543 holds current data or loads new data, with the nine inputs D_0-D_8 accepting parallel input data.

The SEL (Select) input pin is used to switch between the two modes of operation –HOLD and LOAD. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

- 700 MHz Min. Operating Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

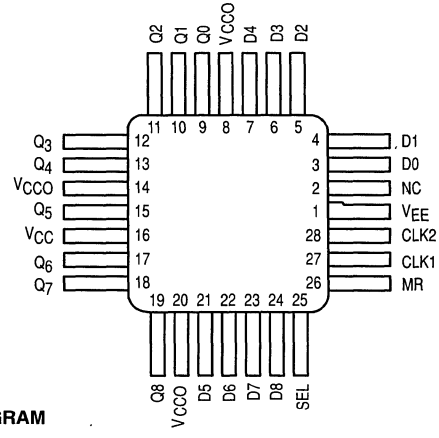
PACKAGE: NON-Compliant
QFP: X

PIN NAME

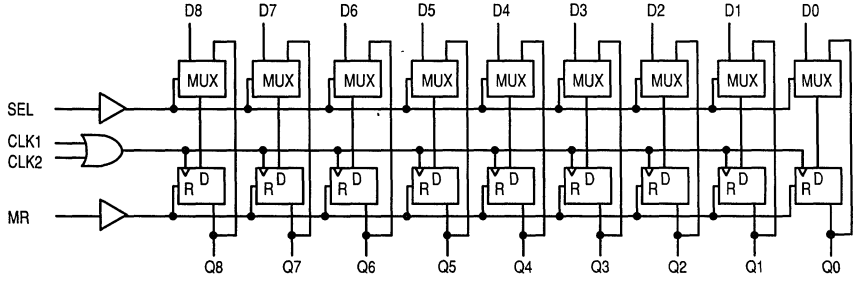
Pin	Function
D_0 - D_8	Parallel Data Inputs
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q_0 - Q_8	Data Outputs
NC	No Connection

Function Table

SEL	Mode
L	LOAD
H	HOLD



LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; $V_{CC} = V_{CCO}$ = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		150		150		150	µA	
I_{EE}	Power Supply Current		145		145		145	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{SHIFT}	Max. Toggle Frequency	700		700		700		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output								
	Clk	600	1000	600	1000	600	1000	ps	
	MR	600	1000	600	1000	600	1000	ps	
t_S	Setup Time								
	D	50		50		50		ps	
	SEL	300		300		300		ps	
t_H	Hold Time								
	D	300		300		300		ps	
	SEL	75		75		75		ps	
t_{RR}	Reset Recovery Time	900		900		900		ps	
t_{PW}	Minimum Pulse Width								
	Clk, MR	400		400		400		ps	
t_{Skew}	Within-device Skew	75		75		75		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	300	800	300	800	300	800	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

5

MOTOROLA

6-Bit D Register

Military 10E551

Product Preview

ELECTRICALLY TESTED PER:
10E551

The 10E551 contains 6 D-type, edge-triggered, master-slave flip-flops with differential outputs. Data enters the master when both Clk1 and Clk2 are Low, and is transferred to the slave when Clk 1 or Clk2 (or both) go High. The asynchronous Master Reset (MR) makes Q outputs go Low.

- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Asynchronous Master Reset
- Dual Clocks
- 75 kΩ Input Pulldown Resistors

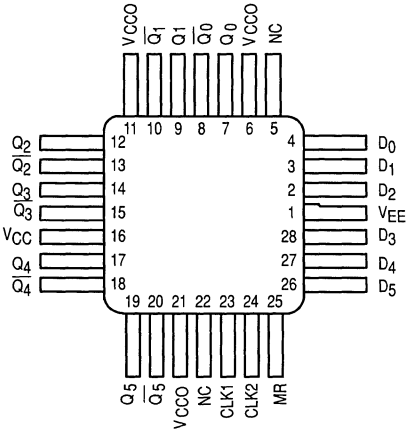
AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

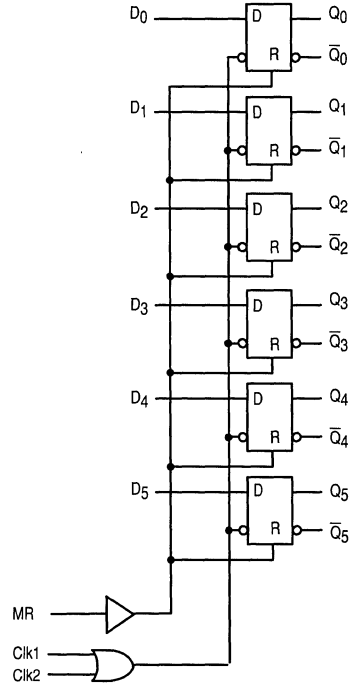
PACKAGE: NON-Compliant
QFP: X

PIN NAME

Pin	Function
D_0 - D_5	Data Inputs
Clk1, Clk2	Clock Inputs
MR	Master Reset
Q_0 - Q_5	True Outputs
$\overline{Q}_0$ - $\overline{Q}_5$	Inverted Outputs



LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; $V_{CC} = V_{CCO}$ = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		150		150		150	µA	V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.
I_{EE}	Power Supply Current		78		78		78	mA	V_{EE} (MAX), V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.

AC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Toggle Frequency	1100		1100		1100		MHz	V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
t_{PLH}	Propagation Delay to Output								V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
t_{PHL}	MR	475	800	475	800	475	800	ps	
	CLK	475	850	475	850	475	850	ps	
t_S	Setup Time, D	0		0		0		ps	V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
t_H	Hold Time, D	350		350		350		ps	V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
t_{RR}	Reset Recovery Time	750		750		750		ps	V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
t_{PW}	Minimum Pulse Width								
	CLK, MR	400		400		400		ps	
t_{Skew}	Within-device Skew	65		65		65		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	300	700	300	700	300	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

5

MOTOROLA

3-Bit 4:1 Mux-Latch

Military 10E556

Product Preview

ELECTRICALLY TESTED PER:
10E556

The 10E556 contains three 4:1 multiplexers followed by transparent latches with differential outputs. When both latch Enables (LEN1, LEN2) are Low, the latch is transparent, and output data is controlled by the multiplexer select controls (SEL0, SEL1). A logic High on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs Low.

- 950 ps Max. D to Output
- 850 ps Max. LEN to Output
- Differential Outputs
- Asynchronous Master Slave
- Dual Latch-Enable
- 75 kΩ Input Pulldown Resistors

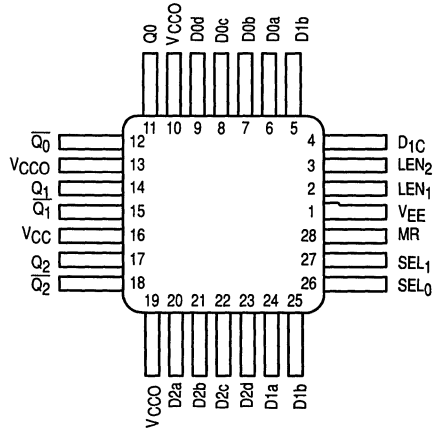
AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

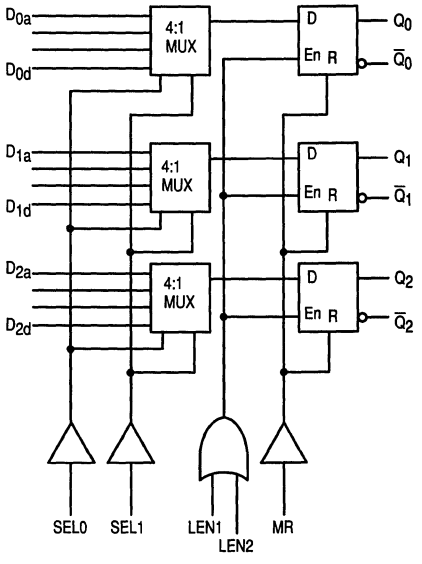
PACKAGE: NON-Compliant
QFP: X

PIN NAME

Pin	Function
D_0x- D_3x	Input Data
SEL0, SEL1	Select Inputs
LEN1, LEN2	Latch Enable
MR	Master Reset
Q_0 - Q_5	True Outputs
$\overline{Q}_0$ - $\overline{Q}_5$	Inverted Outputs



LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; $V_{CC} = V_{CCO}$ = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input Current High		150		150		150	µA	V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.
I_{EE}	Power Supply Current		90		90		90	mA	V_{EE} (MAX), V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.

FUNCTION TABLE		
SEL0	SEL1	Data
L	L	a
H	L	b
L	H	c
H	H	d

FUNCTION TABLE		
LEN1	LEN2	Latch
L	L	Transp.
H	X	Latch
X	H	Latch

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AC CHARACTERISTICS: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
	D	400	900	400	900	400	900	ps	
	SEL0	550	1050	550	1050	550	1050	ps	
	SEL1	450	900	450	900	450	900	ps	
	LEN	350	800	350	900	350	800	ps	
	MR	350	825	350	825	350	825	ps	
t_S	Setup Time								V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
	D	400		400		400		ps	
	SEL0	700		700		700		ps	
	SEL1	600		600		600		ps	
t_H	Hold Time								V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
	D	300		300		300		ps	
	SEL0	100		100		100		ps	
	SEL1	200		200		200		ps	
t_{RR}	Reset Recovery Time	800		800		800		ps	
t_{PW}	Minimum Pulse Width MR	400		400		400		ps	
t_{Skew}	Within-device Skew	50		50		50		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	275	700	275	700	275	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

5

MOTOROLA

5-Bit 2:1 Multiplexer

Military 10E558

Product Preview

ELECTRICALLY TESTED PER:
10E558

The 10E558 contains five 2:1 multiplexers with differential outputs. The output data are controlled by the Select input (SEL).

- 600 ps Max. D to Output
- 800 ps Max. SEL to Output
- Differential Outputs
- One V_{CCO} Pin Per Output Pair
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

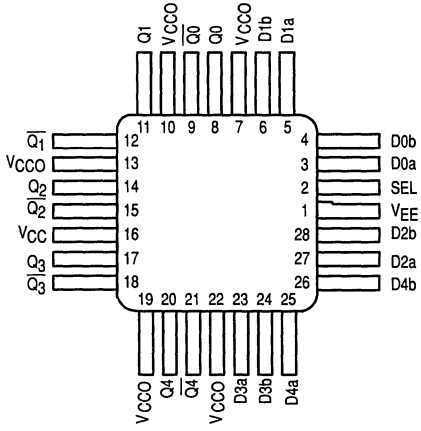
PACKAGE: NON-Compliant
QFP: X

PIN NAME

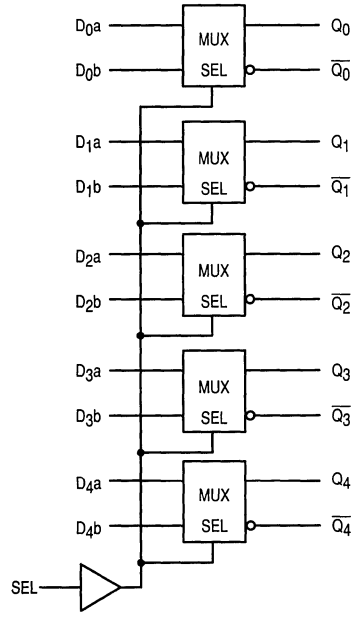
Pin	Function
D_0a - D_4a	Inputs Data a
D_0b - D_4b	Inputs Data b
SEL	Select Input
Q_0 - Q_4	True Outputs
$\overline{Q_0}$ - $\overline{Q_4}$	Inverted Outputs

Function Table

SEL	Data
H	a
L	b



LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; V_{CC} = V_{CCO} = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current							µA	
	D		200		200		200		
	SEL		150		150		150		
I_{EE}	Power Supply Current		40		40		40	mA	

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AC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D	225	550	225	550	225	550	ps	
	SEL	400	775	400	775	400	775	ps	
t_{Skew}	Within-device Skew	60		60		60		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	275	650	275	650	275	650	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

MOTOROLA

6-Bit D Register Differential Data And Clock

Product Preview

ELECTRICALLY TESTED PER:
10E851

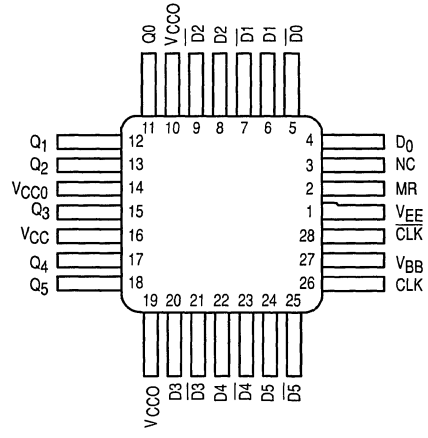
The 10E851 contains 6 D-type flip-flops with single-ended outputs and differential data inputs. The common clock input is also differential. The registers are triggered by a positive transition of the positive clock (Clk) input.

A High on the Master Reset (MR) input resets all Q outputs to Low. The V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When used for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01 μF capacitor.

- Differential Inputs: Data and Clock
- V_{BB} Outputs
- 1100 MHz Min. Toggle Frequency
- Asynchronous Master Reset
- 75 kΩ Input Pulldown Resistors

PIN NAME

Pin	Function
D_0 - D_5	+ Data Inputs
$\overline{D_0}$ - $\overline{D_5}$	- Data Inputs
CLK	+ Clock Inputs
$\overline{CLK}$	- Clock Inputs
MR	Master Reset
V_{BB}	V_{BB} Output
Q_0 - Q_5	Data Outputs



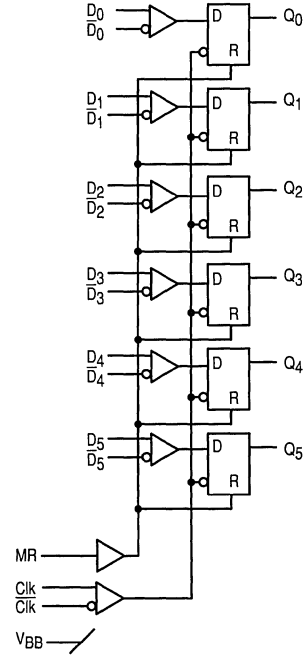
Military 10E851

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

LOGIC DIAGRAM



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10E Series DC CHARACTERISTICS: V_{EE} = -5.2 V ± 5%; $V_{CC} = V_{CCO}$ = GND[1]

Symbol	Parameter	Limits						Units
		+ 25° C		+ 125° C		– 55° C		
		Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	-980	-810	TBA		TBA		mV
V_{OL}	Output LOW Voltage	-1950	-1630	TBA		TBA		mV
V_{IH}	Input HIGH Voltage	-1130	-810	TBA		TBA		mV
V_{IL}	Input LOW Voltage	-1950	-1480	TBA		TBA		mV
I_{IL}	Input LOW Current	0.5		TBA		TBA		µA

1. 10E series circuits are designed to meet the dc specifications shown in the table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0 volts, except bus outputs where specified, are terminated into 25Ω.

DC CHARACTERISTICS: $V_{EE} = V_{EE}$(min) to V_{EE}(max), $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
V_{BB}	Output Reference Voltage	-1.35	-1.25	-1.31	-1.19	-1.38	-1.27	V	V_{IL} = Open, V_{IH} = Open, R_L = 50Ω to – 2.0 V.
I_{IH}	Input Current High		150		150		150	µA	V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.
I_{EE}	Power Supply Current		101		101		101	mA	V_{EE} (MAX), V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.
V_{CMR}	Common Mode Range	-2.0	-0.4	-2.0	-0.4	-2.0	-0.4	V	(Note 1)

1. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operations obtained when the "HIGH" input is within the V_{CMR} range and the input swing is greater than V_{PPMIN} and < 1.0 V.

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AC CHARACTERISTICS: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Toggle Frequency	1100		1100		1100		MHz	V_{IL} = 0.295 V, V_{IH} = 1.045 V, Dn = 0.670 V, $\overline{Clk}$ = 0.670 V, R_L = 50Ω to Gnd.
t_{PLH} t_{PHL}	Propagation Delay to Output								V_{IL} = 0.295 V, V_{IH} = 1,045 V, Dn = 0.670 V, $\overline{Clk}$ = 0.670 V, R_L = 50Ω to Gnd.
	CLK (Diff)	475	800	475	800	475	800	ps	
	CLK (SE)	425	850	425	850	425	850	ps	
	MR	425	850	425	850	425	850	ps	
t_S	Setup Time, D	150		150		150		ps	V_{IL} = 0.295 V, V_{IH} = 1.045 V, Dn = 0.670 V, $\overline{Clk}$ = 0.670 V, R_L = 50Ω to Gnd.
t_H	Hold Time, D	250		250		250		ps	V_{IL} = 0.295 V, V_{IH} = 1.045 V, Dn = 0.670 V, $\overline{Clk}$ = 0.670 V, R_L = 50Ω to Gnd.
$V_{PP(AC)}$	Minimum Input Swing	150		150		150		mV	(Note 1)
t_{RR}	Reset Recovery Time	750		750		750		ps	
t_{PW}	Minimum Pulse Width CLK, MR	400		400		400		ps	
t_{Skew}	Within-device Skew	100		100		100		ps	(Note 2)
t_r t_f	Rise/Fall Times 20 - 80%	275	800	275	800	275	800	ps	

1. Minimum input voltage for AC parameters are guaranteed.
2. Within-device skew is defined as identical transitions on similar paths through a device.

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MOTOROLA

8-Bit Synchronous Binary Up Counter

Military 100E416

Product Preview

ELECTRICALLY TESTED PER:
100E416

The 100E416 is a high-speed synchronous, presettable, cascadable 8-bit binary counter. Architecture and operation are the same as the 10H416 in the MECL 10H family, extended to 8-bits, as shown in the logic diagram.

The counter features internal feedback of $\overline{TC}$, gated by the TCLD (terminal count load) pin. When TCLD is LOW (or left open, in which case it is pulled LOW by the internal pull-downs), the $\overline{TC}$ feedback is disabled, and counting proceeds continuously, with TC going LOW to indicate an all-one state. When TCLD is HIGH, the $\overline{TC}$ feedback causes the counter to automatically re-load upon $\overline{TC}$ = LOW, thus functioning as a programmable counter

- 700 MHz Min. Count Frequency
- 1000 ps CLK to Q, $\overline{TC}$
- Internal $\overline{TC}$ Feedback (Gated)
- 8-Bit
- Fully Synchronous Counting and $\overline{TC}$ Generation
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: F

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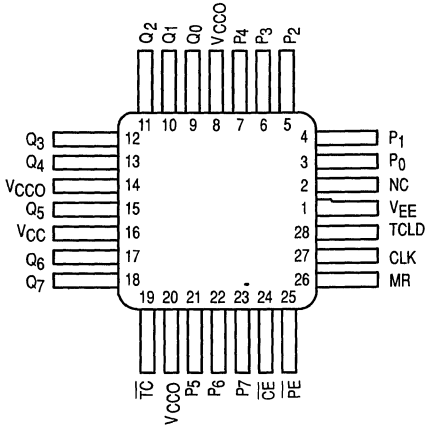
PIN NAME

Pin	Function
P_0 - P_7	Parallel Data (Preset) Data
Q_0 - Q_7	Data Outputs
$\overline{CE}$	Count Enable Control Input
$\overline{PE}$	Parallel Load Enable Control Input
MR	Master Reset
CLK	Clock
$\overline{TC}$	Terminal Count Output
TCLD	TC - Load Control Input



FUNCTION TABLE

$\overline{CE}$	$\overline{PE}$	TCLD	MR	CLK	Function
X	L	X	L	⌐	Load Parallel (P_n to Q_n)
L	H	L	L	⌐	Continuous Count
L	H	H	L	⌐	Count: Load Parallel on $\overline{TC}$ = LOW
H	H	X	L	⌐	Hold
X	X	X	L	⌙	Master Respond, Slaves Hold
X	X	X	H	⌐	Reset (Q_n: = LOW, $\overline{TC}$: = HIGH)

⌐ = clock pulse (low to high)
⌙ = clock pulse (high to low)

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, V_{CC} = V_{CCO} = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	V_{IN} = $V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or V_{IN} = $V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	V_{IN} = $V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or V_{IN} = $V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	V_{IN} = $V_{IL(min)}$	

DC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input Current High		150		150		150	µA	
I_{EE}	Power Supply Current		181		208		181	mA	

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AC CHARACTERISTICS: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
f_{count}	Maximum Count Frequency	700		700		700		MHz	
t_{PLH}	Propagation Delay to Output								
t_{PHL}	CLK to Q	600	1000	600	1000	600	1000	ps	
	MR to Q	600	1000	600	1000	600	1000	ps	
	CLK to $\overline{TC}$ (Q's loaded)	550	1050	550	1050	550	1050	ps	(Note 1)
	CLK to $\overline{TC}$ (Q's unloaded)	550	900	550	900	550	900	ps	(Note 1)
	MR to $\overline{TC}$	625	1000	625	1000	625	1000	ps	
t_S	Setup Time								
	Pn	150		150		150		ps	
	CE	600		600		600		ps	
	PE	600		600		600		ps	
	TCLD	500		500		500		ps	
t_H	Hold Time								
	Pn	250		250		250		ps	
	CE	0		0		0		ps	
	PE	0		0		0		ps	
	TCLD	100		100		100		ps	
t_{RR}	Reset Recovery Time	900		900		900		ps	
t_{PW}	Minimum Pulse Width								
	CLK, MR	400		400		400		ps	
t_r t_f	Rise/Fall Times 20 - 80%	300	800	300	800	300	800	ps	

1. CLK to $\overline{TC}$ propagation delay is dependent on the loading of the Q outputs. With all of the Q outputs loaded the noise generated in going from a IIII IIII state to a 0000 0000 state causes the CLK to $\overline{TC}$+ delay to increase.

5

MOTOROLA

4-Input Quad OR/NOR Gate

Product Preview

ELECTRICALLY TESTED PER:
100E501

The 100E501 is a quad 4-Input **OR/NOR** gate.

- 500 ps Max. Propagation Delay
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

PIN NAME

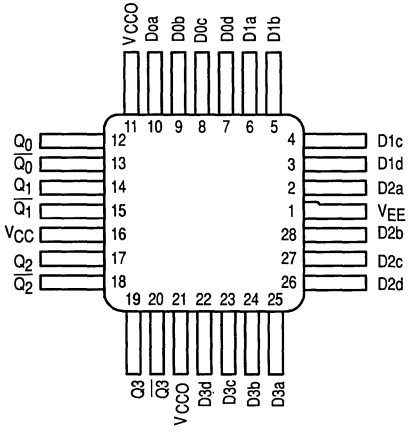
Pin	Function
D_{0a} - D_{3d}	Data Inputs
Q_0 - Q_3	True Outputs
$\overline{Q_0}$ - $\overline{Q_3}$	Inverting Outputs

Military 100E501

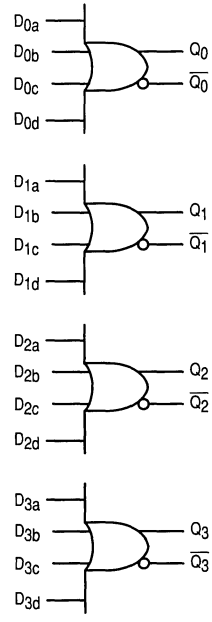
AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X



LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input Current High		150		150		150	µA	
I_{EE}	Power Supply Current		36		42		36	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q	200	500	200	500	200	500	ps	
t_{Skew}	Within-device Skew		50		50		50	ps	(Note 1)
t_{Skew}	Within-gate Skew		25		25		25	ps	(Note 2)
t_r t_f	Rise/Fall Times 20 - 80%	300	575	300	575	300	575	ps	

1. Within-device skew is defined as identical transitions on similar paths trough a device.
2. Within-gate skew is defined as the variation in propagation delays of a gate when driven from its different inputs.

5

MOTOROLA

Quint 2-Input AND/NAND Gate

Product Preview

ELECTRICALLY TESTED PER:
100E504

The 100E504 is a quint 2-input **AND/NAND** gate. The function output F is the OR of all five AND gate outputs, while $\overline{F}$ is the NOR. The Q outputs need not be terminated if only the F outputs are to be used.

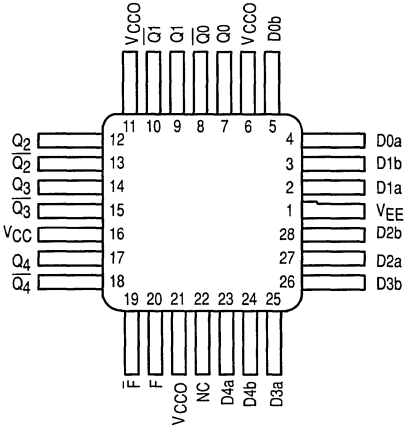
- 600 ps Max. Propagation Delay
- OR/NOR Function Outputs
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

PIN NAME

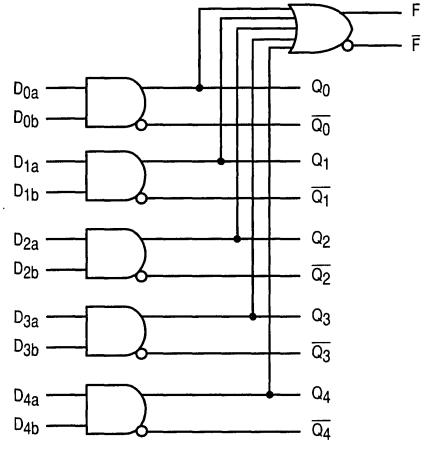
Pin	Function
D_{0a} - D_{4b}	Data Inputs
Q_0 - Q_4	AND Outputs
$\overline{Q_0}$ - $\overline{Q_4}$	NAND Outputs
F	OR Output
$\overline{F}$	NOR Output

FUNCTION OUTPUTS

$F = (D_{0a} \bullet D_{0b}) + (D_{1a} \bullet D_{1b}) + (D_{2a} \bullet D_{2b}) + (D_{3a} \bullet D_{3b}) + (D_{4a} \bullet D_{4b})$



LOGIC DIAGRAM



Military 100E504

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		200		200		200	µA	
I_{EE}	Power Supply Current		46		53		46	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D to Q	225	600	225	600	225	600	ps	
	D to F	500	1000	500	1000	500	1000	ps	
t_{Skew}	Within-device Skew								
	D to Q	75		75		75		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%								
	Q	275	700	275	700	275	700	ps	
	F	300	700	300	700	300	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

5

MOTOROLA

Quint 2-Input XOR/XNOR Gate

Product Preview

ELECTRICALLY TESTED PER:
100E507

Military 100E507

The 100E507 is a quint 2-input **XOR/XNOR** gate. The function output F is the OR of all five XOR outputs, while $\overline{F}$ is the NOR. The Q outputs need not be terminated if only the F outputs are to be used.

- 600 ps Max. Propagation Delay
- OR/NOR Function Outputs
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

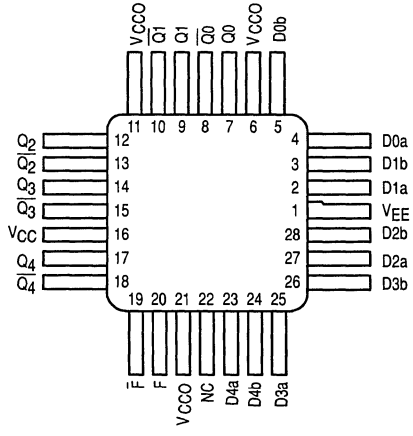
PIN NAME

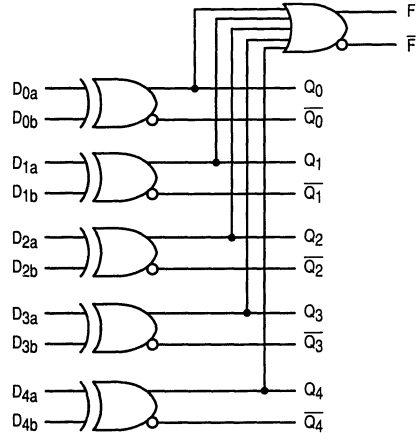
Pin	Function
D_{0a} - D_{4b}	Data Inputs
Q_0 - Q_4	XOR Outputs
$\overline{Q_0}$ - $\overline{Q_4}$	XNOR Outputs
F	OR Output
$\overline{F}$	NOR Output

FUNCTION OUTPUTS

$$F = (D_{0a} \oplus D_{0b}) + (D_{1a} \oplus D_{1b}) + (D_{2a} \oplus D_{2b}) + (D_{3a} \oplus D_{3b}) + (D_{4a} \oplus D4_b)$$

LOGIC DIAGRAM





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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		200		200		200	µA	
I_{EE}	Power Supply Current		50		58		50	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D to Q	250	600	250	600	250	600	ps	
	D to F	500	1000	500	1000	500	1000	ps	
t_{Skew}	Within-device Skew								
	D to Q	75		75		75		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%								
	Q	275	700	275	700	275	700	ps	
	F	300	700	300	700	300	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

5

MOTOROLA

1:9 Differential Clock Driver

Product Preview

ELECTRICALLY TESTED PER:
100E511

Military 100E511

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: F

The 100E511 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. It accepts one signal input, which can be either differential or else single-ended if the V_{BB} output is used. The signal is fanned out to 9 identical differential outputs. An enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all $\overline{Q}$ outputs HIGH.

The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within device, and empirical modeling is used to determine process control limits that ensure consistent t_{pd} distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

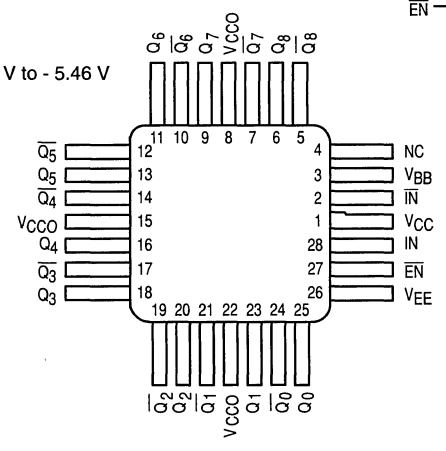
To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into 50Ω, even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i. e. sharing the same V_{CCO}) as the pairs(s) being used on the same side, in order to maintain minimum skew. Failure to do this will result in small degradation of propagation delay (on the order of 10-20 ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

The V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When used for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01 μF capacitor.

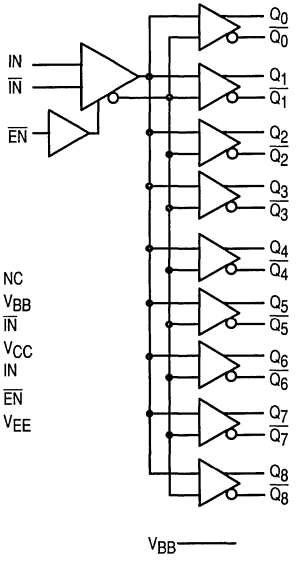
- Low Skew
- Guaranteed Skew Spec
- Differential Design
- V_{BB} output
- Enable
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

PIN NAME

Pin	Function
IN, $\overline{IN}$	Differential Input Pair
En	Enable
Q_0, $\overline{Q_0}$ - Q_8, $\overline{Q_8}$	Differential Outputs
V_{BB}	V_{BB} Outputs



LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		μA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
V_{BB}	Output Reference Voltage	-1.38	-1.26	-1.38	-1.26	-1.38	-1.26	V	V_{IL} = Open, V_{IH} = Open, R_L = 50Ω to – 2.0 V.
I_{IH}	Input Current High		150		150		150	μA	V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.
I_{EE}	Power Supply Current		60		69		60	mA	V_{EE} (MAX), V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

5

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay to Output								
t_{PHL}	IN (Differential)	430	630	430	630	430	630	ps	(Note 1)
	IN (Single-ended)	330	730	330	730	330	730	ps	(Note 2)
	Enable	450	850	450	850	450	850	ps	(Note 3)
	Disable	450	850	450	850	450	850	ps	(Note 3)
t_{Skew}	Within-Device Skew		50		50		50	ps	(Note 4)
t_S	Setup Time $\overline{En}$ to IN	200		200		200		ps	(Note 5)
t_H	Hold Time IN to $\overline{En}$	0		0		0		ps	(Note 6)
t_R	Release Time $\overline{En}$ to IN	300		300		300		ps	(Note 7)
V_{PP}	Minimum Input Swing	250		250		250		mV	(Note 8)
V_{CMR}	Common Mode Range	-1.6	-0.4	-1.6	-0.4	-1.6	-0.4	V	(Note 9)
t_r t_f	Rise/Fall Times 20 - 80%	275	600	275	600	275	600	ps	

See Notes on the following page.

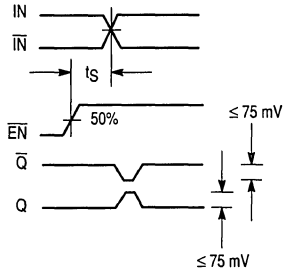

Figure 1. Setup Time

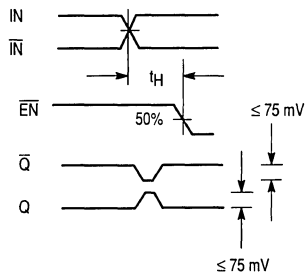

Figure 2. Hold Time

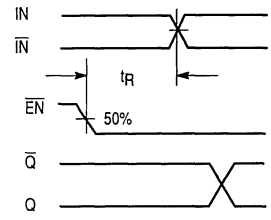

Figure 3. Release Time

Notes

1. The differential propagation is defined as the delay from the crossing points of the differential input signals to the crossing point of differential output signals. (See *Definitions and testing ECLinPS AC Parameters* in Section 1.)
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. (See *Definitions and testing ECLinPS AC Parameters* in Section 1.)
3. Enable is defined as the propagation delay from 50% point of the **negative** transition $\overline{EN}$ to the 50% point of the **positive** transition on Q (or a negative transition on $\overline{Q}$). Disable is defined as the propagation delay from 50% point of the **positive** transition on $\overline{EN}$ to the 50% point of the **negative** transition on Q (or a negative transition on $\overline{Q}$).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The setup time is the minimum time that $\overline{EN}$ must be asserted prior to the next transition of IN/$\overline{IN}$ to prevent an output response greater than ± 75 mV to that IN/$\overline{IN}$ transition (see Figure 1).
6. The hold time is the minimum time that $\overline{EN}$ must remain asserted after a negative going IN or a positive going $\overline{IN}$ to prevent an output response greater than ± 75 mV to that IN/$\overline{IN}$ transition (see Figure 2).
7. The release time is the minimum time that $\overline{EN}$ must be deasserted prior to the next IN/$\overline{IN}$ transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. V_{PP} (min) is defined as the *minimum* input differential voltage which will cause no increase in the propagation delay. The V_{PP} (min) is AC limited for the E511, a differential input as low as 50 mV will still produce full ECL levels at the output.
9. V_{CMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V_{PP} (min). Measured output voltages must fall within the specified limits of V_{OH} and V_{OL} (V_{OH} = - 0.880 V max, - 1.090 V min, V_{OL} = - 1.580 V max, - 1.810 V min).

5

MOTOROLA

Quad Driver

Military 100E512

Product Preview

ELECTRICALLY TESTED PER:
100E512

The 100E512 is a quad driver with two pairs of OR/NOR outputs form each gate, and a common, buffered enable input. Using the data inputs the device can serve as an ECL memory address fan-out driver. Using just the enable input, the device serves as a clock driver, although the 100E511 is designed specifically for this purpose, and offers lower skew than the E512.

- 600 ps Max. Propagation Delay
- Common Enable Input
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

PIN NAME

Pin	Function
D_0 - D_3	Data Inputs
$\overline{EN}$	Enable Inputs
Q_{na} - Qnb	True Outputs
$\overline{Q_{na}}$ - $\overline{Qnb}$	Inverting Outputs

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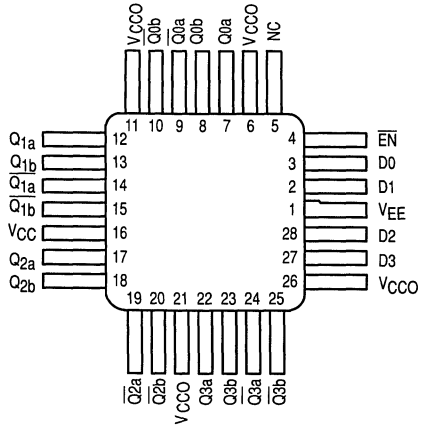
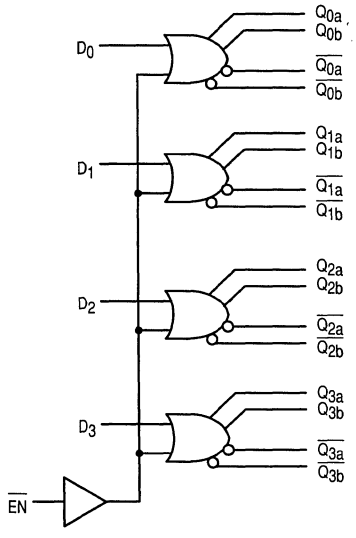


LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current							µA	
	D		200		200		200		
	$\overline{EN}$		150		150		150		
I_{EE}	Power Supply Current	47	56	54	65	47	56	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D	200	600	200	600	200	600	ps	
	$\overline{EN}$	275	675	275	675	275	675	ps	
t_{Skew}	Within-device Skew								
	Dn to Qn, $\overline{Qn}$	80		80		80		ps	(Note 1)
	Dna to Qnb	40		40		40		ps	(Note 2)
t_r t_f	Rise/Fall Times 20 - 80%	275	700	275	700	275	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Skew defined between common OR or common NOR outputs of a single gate.

5

MOTOROLA

Quint Differential Line Receiver

Military 100E516

Product Preview

ELECTRICALLY TESTED PER:
100E516

The 100E516 is a quint differential line receiver with emitter-follower outputs. An internally generated reference supply (V_{BB}) is available for single-ended reception.

Active current sources plus a deep collector feature of the MOSAIC III process provide the receivers with excellent common-mode noise rejection. Each receiver has a dedicated V_{CCO} supply lead, providing optimum symmetry and stability.

The receiver design features clamp circuity to cause a defined state if both the inverting and non-inverting inputs are left open; in this case the Q output goes LOW, while the $\overline{Q}$ output goes HIGH. This feature makes the device ideal for twisted pair applications.

If both inverting and non-inverting inputs are at equal potential > -2.5 V, the receiver does not go to a defined state, but rather current-shares in normal differential amplifier fashion, producing output voltage levels midway between HIGH and LOW, or the device may even oscillate.

The device V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When using for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01μF capacitor.

The 100E516 features input pull-down resistors, as does the rest of the ECLinPS family.

AVAILABLE AS

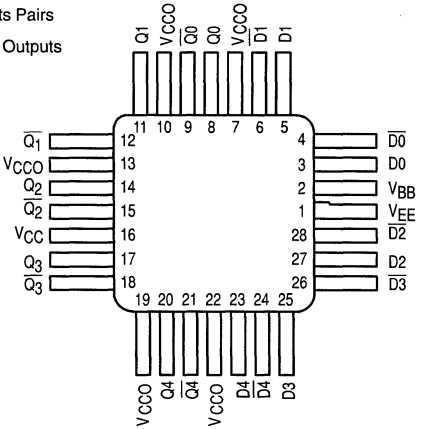
1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

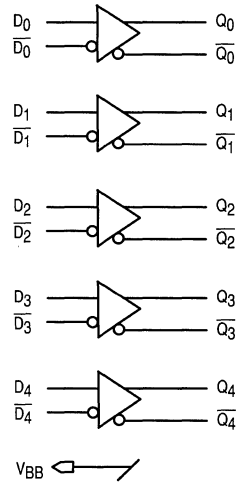
- 500 ps Max. Propagation Delay
- V_{BB} Supply Output
- Dedicated V_{CCO} Pin for Each Receiver
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

PIN NAME

Pin	Function
D_0, $\overline{D_0}$ - D_4, $\overline{D_4}$	Differential Inputs Pairs
Q_0, $\overline{Q_0}$ - Q_4, $\overline{Q_4}$	Differential Outputs Pairs
V_{BB}	Reference Voltage Outputs



LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, V_{CC} = V_{CCO} = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	V_{IN} = $V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or V_{IN} = $V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	V_{IN} = $V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or V_{IN} = $V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	V_{IN} = $V_{IL(min)}$	

DC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
V_{BB}	Output Reference Voltage	-1.38	-1.26	-1.38	-1.26	-1.38	-1.26	V	
I_{IH}	Input High Current		200		200		200	µA	
I_{EE}	Power Supply Current	29	35	33	40	29	35	mA	
$V_{PP(DC)}$	Input Seneitivity	150		150		150		mV	(Note 1)
V_{CMR}	Common Mode Range	-2.0	-0.6	-2.0	-0.6	-2.0	-0.6	V	(Note 2)

1. V_{PP} is the minimum differential input voltage required to assure full ECL levels are present at the outputs.
2. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operation is obtained when the "HIGH" input is within the V_{CMR} range and the input swing is greater than V_{PPMIN} and < 1.0 V.

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AC CHARACTERISTICS: V_{EE} = V_{EE}(min) to V_{EE}(max), V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D	200	450	200	450	200	450	ps	
	D (SE)	150	500	150	500	150	500	ps	
$V_{PP(AC)}$	Minimum Input Swing	150		150		150		mV	(Note 1)
t_{Skew}	Within-device Skew								
	Dn to Qn, $\overline{Qn}$	50		50		50		ps	(Note 2)
t_{Skew}	Duty Cycle Skew								
	t_{PLH} - t_{PHL}	± 10		± 10		± 10		ps	(Note 3)
t_r t_f	Rise/Fall Times 20 - 80%	275	575	275	575	275	575	ps	

1. Minimum input swing for which AC parameters are guaranteed.
2. Within-device skew is defined as identical transitions on similar paths through a device.
3. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross points of the outputs.

MOTOROLA

4-Bit D Flip-Flop

Military 100E531

Product Preview

ELECTRICALLY TESTED PER:
100E531

The 100E531 is a quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock (C_C) LOW and using the Clock Enable ($\overline{CE}$) inputs for clocking. Common clocking is achieved by holding the $\overline{CE}$ inputs LOW and using C_C to clock all four flip-flops. In this case, the $\overline{CE}$ inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both C_C and $\overline{CE}$ are LOW, and transfers to the slave when either C_C or $\overline{CE}$ (or both) go HIGH.

- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

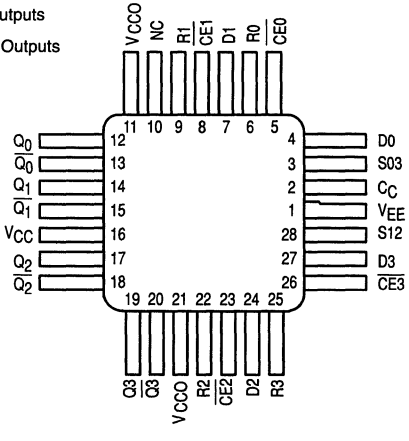
1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

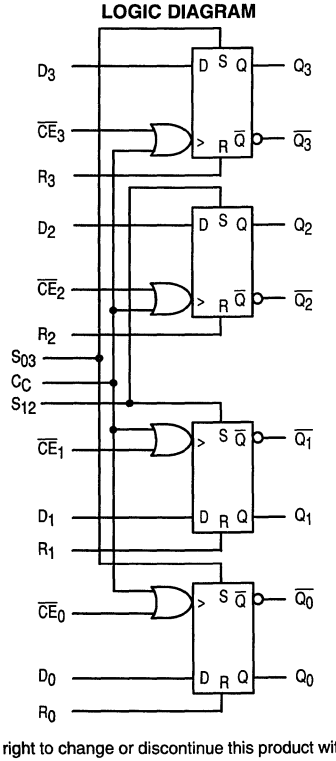
5

PIN NAME

Pin	Function
D_0 - D_3	Data Inputs
$\overline{CE_0}$ - $\overline{CE_3}$	Clock Enables (Individual)
R_0 - R_3	Resets
C_C	Common Clock
S_{03}, S_{12}	Sets (Paired)
Q_0 - Q_3	True Outputs
$\overline{Q_0}$ - $\overline{Q_3}$	Inverting Outputs



LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current							µA	
	C_C		350		350		350		
	S		450		450		450		
	R		300		300		300		
	$\overline{CE}$		300		300		300		
	D		150		150		150		
I_{EE}	Power Supply Current		70		81		70	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Max. Toggle Frequency	1100		1100		1100		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output								
	$\overline{CE}$	360	700	360	700	360	700	ps	
	C_C	325	675	325	675	325	675	ps	
	R	350	725	350	725	350	725	ps	
	S	350	725	350	725	350	725	ps	
t_S	Setup Time								
	D	150		150		150		ps	(Note 2)
t_H	Hold Time								
	D	175		175		175		ps	(Note 2)
t_{RR}	Reset Recovery Time	400		400		400		ps	
t_{Skew}	Within-device Skew	60		60		60		ps	(Note 1)
t_{PW}	Minimum Pulse Width								
	Clk, S, R	400		400		400		ps	
t_r t_f	Rise/Fall Times 20 - 80%	300	675	300	675	300	675	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Setup/hold time guaranteed for both C_C & $\overline{CE}$.

5

MOTOROLA

8-Bit Shift Register

Military 100E541

Product Preview

ELECTRICALLY TESTED PER:
100E541

The 100E541 is an 8-bit full-function shift register. The 100E541 performs serial/parallel in and serial/parallel out, shifting in either direction. The eight inputs D_0-D_7 accept parallel input data, while DL/DR accept serial input data for left/right shifting.

The select pins, SEL0 and SEL1, select one of four modes of operation: Load, Hold, Shift Left, Shift Right, according to the Function Table.

Input data is accepted a set-up time before the positive clock edge. A HIGH on the Master Reset (MR) pin asynchronously resets all the registers to zero.

- 700 MHz Min. Shift Frequency
- 8-Bits
- Full-Function, Bi-directional
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

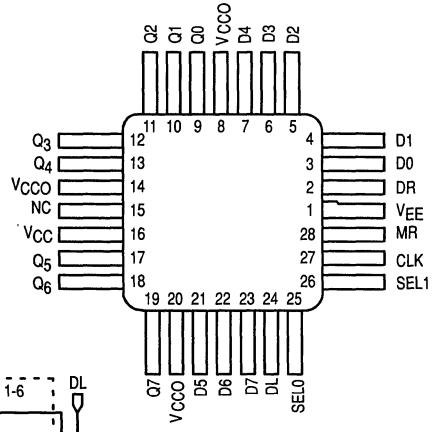
AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

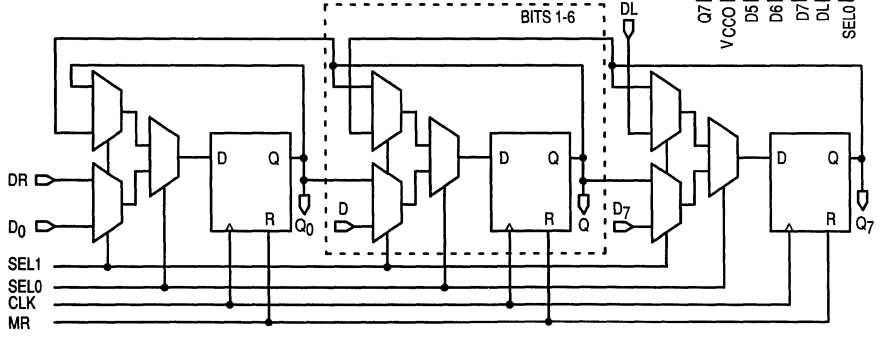
PACKAGE: NON-Compliant
QFP: X

PIN NAME

Pin	Function
D_0 - D_7	Parallel Data Inputs
DL, DR	Serial Data Inputs
SEL0, SEL1	Mode Select Inputs
CLK	Clock
Q_0 - Q_7	Data Outputs
MR	Master Reset



LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	$V_{IN} = V_{IL(min)}$	

Function Table

SEL0	SEL1	Function
L	L	Load
L	H	Shift Right (Dn to D_{n+1})
H	L	Shift Left (Dn to D_{n-1})
H	H	Hold

Expanded Function Table

Function	DL	DR	SEL0	SEL1	MR	CLK	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Load	X	X	L	L	L	Z	D0	D1	D2	D3	D4	D5	D6	D7
Shift Right	X	L	L	H	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	Q6
	X	H	L	H	L	Z	H	L	Q0	Q1	Q2	Q3	Q4	Q5
Shift Left	L	X	H	L	L	Z	L	Q0	Q1	Q2	Q3	Q4	Q5	L
	H	X	H	L	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Hold	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
	X	X	H	H	L	Z	Q0	Q1	Q2	Q3	Q4	Q5	L	H
Reset	X	X	X	X	H	X	L	L	L	L	L	L	L	L

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DC CHARACTERISTICS: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		150		150		150	µA	
I_{EE}	Power Supply Current		157		181		157	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{Shift}	Max. Shift Frequency	700		700		700		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output								
	Clk	625	975	625	975	625	975	ps	
	MR	600	975	600	975	600	975	ps	
t_S	Setup Time								
	D	175		175		175		ps	
	SEL0	350		350		350		ps	
	SEL1	300		300		300		ps	
t_H	Hold Time								
	D	200		200		200		ps	
	SEL0	100		100		100		ps	
	SEL1	100		100		100		ps	
t_{RR}	Reset Recovery Time	900		900		900		ps	
t_{PW}	Minimum Pulse Width								
	Clk, MR	400		400		400		ps	
t_{Skew}	Within-device Skew	60		60		60		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	300	800	300	800	300	800	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

5

MOTOROLA

9-Bit Shift Register

Military 100E542

Product Preview

ELECTRICALLY TESTED PER:
100E542

The 100E542 is a 9-bit shift register, designed with byte-parity applications in mind. The 100E542 performs serial/parallel in and serial/parallel out, shifting in one direction. The nine inputs D_0-D_8 accept parallel input data, while S-IN accepts serial input data.

The SEL (Select) input pin is used to switch between the two modes of operation –SHIFT and LOAD. The shift direction is from bit 0 to bit 8. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2; shifting is also accomplished on the positive clock edge. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

- 700 MHz Min. Shift Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

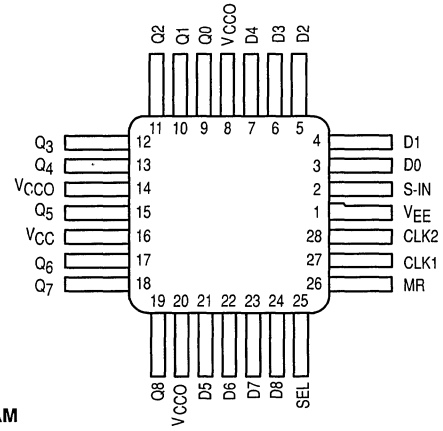
PACKAGE: NON-Compliant
QFP: X

PIN NAME

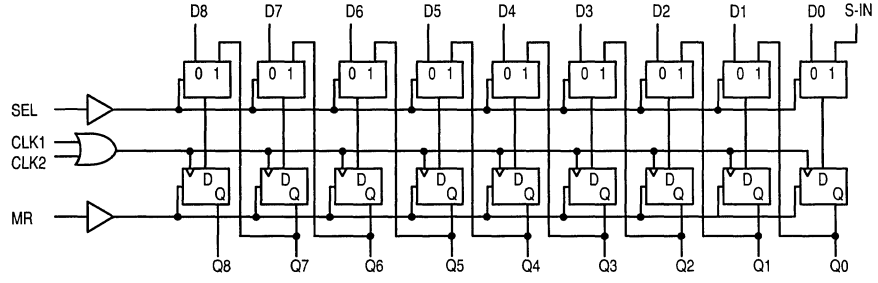
Pin	Function
D_0 - D_8	Parallel Data Inputs
S-IN	Serial Data Input
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q_0 - Q_8	Data Outputs

Function Table

SEL	Mode
L	LOAD
H	SHIFT



LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		μA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		150		150		150	μA	
I_{EE}	Power Supply Current		145		165		145	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{SHIFT}	Max. Shift Frequency	700		700		700		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output								
	Clk	600	1000	600	1000	600	1000	ps	
	MR	600	1000	600	1000	600	1000	ps	
t_S	Setup Time								
	D	50		50		50		ps	
	SEL	300		300		300		ps	
t_H	Hold Time								
	D	300		300		300		ps	
	SEL	75		75		75		ps	
t_{RR}	Reset Recovery Time	900		900		900		ps	
t_{PW}	Minimum Pulse Width								
	Clk, MR	400		400		400		ps	
t_{Skew}	Within-device Skew	75		75		75		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	300	800	300	800	300	800	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

5

MOTOROLA

9-Bit Hold Register

Military 100E543

Product Preview

ELECTRICALLY TESTED PER:
100E543

The 100E543 is a 9-bit holding register, designed with byte-parity applications in mind. The 100E543 holds current data or loads new data, with the nine inputs D_0-D_8 accepting parallel input data.

The SEL (Select) input pin is used to switch between the two modes of operation –HOLD and LOAD. Input data is accepted by the registers a set-up time before the positive going edge of CLK1 or CLK2. A HIGH on the Master Reset pin (MR) asynchronously resets all the registers to zero.

- 700 MHz Min. Operating Frequency
- 9-Bit for Byte-Parity Applications
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

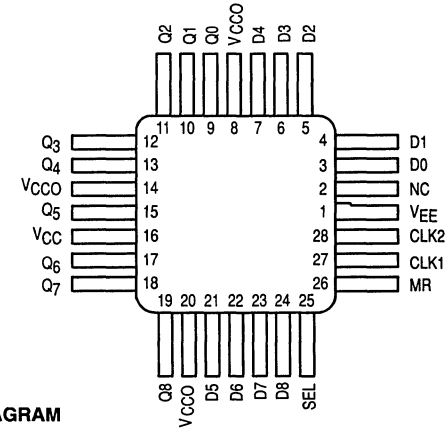
PACKAGE: NON-Compliant
QFP: X

PIN NAME

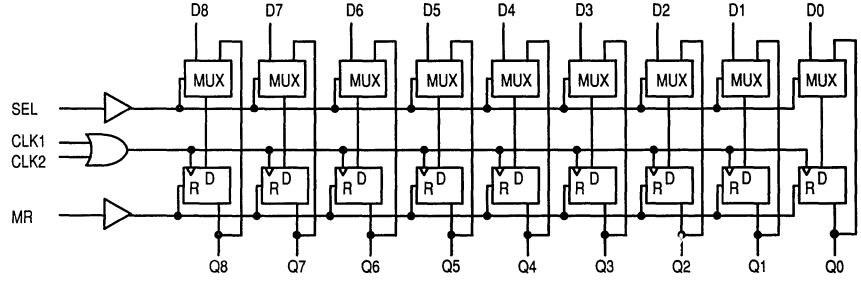
Pin	Function
D_0 - D_8	Parallel Data Inputs
SEL	Mode Select Input
CLK1, CLK2	Clock Inputs
MR	Master Reset
Q_0 - Q_8	Data Outputs
NC	No Connection

Function Table

SEL	Mode
L	LOAD
H	HOLD



LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, V_{CC} = V_{CCO} = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	V_{IN} = $V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or V_{IN} = $V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	V_{IN} = $V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or V_{IN} = $V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	V_{IN} = $V_{IL(min)}$	

DC CHARACTERISTICS: V_{EE} = $V_{EE(min)}$ to $V_{EE(max)}$, V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		150		150		150	µA	
I_{EE}	Power Supply Current		145		165		145	mA	

AC CHARACTERISTICS: V_{EE} = $V_{EE(min)}$ to $V_{EE(max)}$, V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{SHIFT}	Max. Toggle Frequency	700		700		700		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output								
	Clk	600	1000	600	1000	600	1000	ps	
	MR	600	1000	600	1000	600	1000	ps	
t_S	Setup Time								
	D	50		50		50		ps	
	SEL	300		300		300		ps	
t_H	Hold Time								
	D	300		300		300		ps	
	SEL	75		75		75		ps	
t_{RR}	Reset Recovery Time	900		900		900		ps	
t_{PW}	Minimum Pulse Width								
	Clk, MR	400		400		400		ps	
t_{Skew}	Within-device Skew	75		75		75		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	300	800	300	800	300	800	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

MOTOROLA

6-Bit D Register

Military 100E551

Product Preview

ELECTRICALLY TESTED PER:
100E551

The 100E551 contains 6 D-type, edge-triggered, master-slave flip-flops with differential outputs. Data enters the master when both Clk1 and Clk2 are Low, and is transferred to the slave when Clk 1 or Clk2 (or both) go High. The asynchronous Master Reset (MR) makes Q outputs go Low.

- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Asynchronous Master Reset
- Dual Clocks
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46V
- 75 kΩ Input Pulldown Resistors

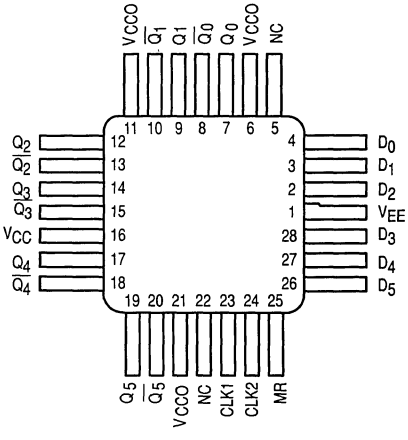
AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

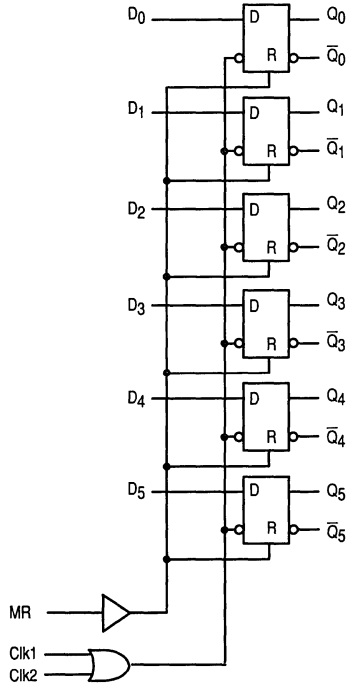
PACKAGE: NON-Compliant
QFP: X

PIN NAME

Pin	Function
D_0 - D_5	Data Inputs
Clk1, Clk2	Clock Inputs
MR	Master Reset
Q_0 - Q_5	True Outputs
$\overline{Q}_0$ - $\overline{Q}_5$	Inverted Outputs



LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		μA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		150		150		150	μA	V_{IL} = − 1.810 V, V_{IH} = − 0.880 V, R_L = 50Ω to − 2.0 V.
I_{EE}	Power Supply Current		78		90		78	mA	V_{EE} (MAX), V_{IL} = − 1.810 V, V_{IH} = − 0.880 V, R_L = 50Ω to − 2.0 V.

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Toggle Frequency	1100		1100		1100		MHz	V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
t_{PLH}	Propagation Delay to Output								V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
t_{PHL}	MR	475	800	475	800	475	800	ps	
	CLK	475	850	475	850	475	850	ps	
t_S	Setup Time, D	0		0		0		ps	V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
t_H	Hold Time, D	350		350		350		ps	V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
t_{RR}	Reset Recovery Time	750		750		750		ps	V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
t_{PW}	Minimum Pulse Width								
	CLK, MR	400		400		400		ps	
t_{Skew}	Within-device Skew	65		65		65		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	300	700	300	700	300	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

MOTOROLA

3-Bit 4:1 Mux-Latch

Product Preview

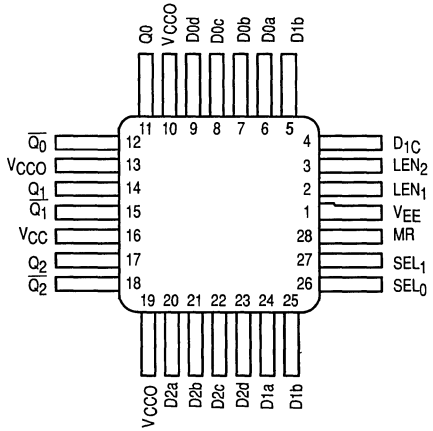
ELECTRICALLY TESTED PER:
100E556

The 100E556 contains three 4:1 multiplexers followed by transparent latches with differential outputs. When both latch Enables (LEN1, LEN2) are Low, the latch is transparent, and output data is controlled by the multiplexer select controls (SEL0, SEL1). A logic High on either LEN1 or LEN2 (or both) latches the outputs. The Master Reset (MR) overrides all other controls to set the Q outputs Low.

- 950 ps Max. D to Output
- 850 ps Max. LEN to Output
- Differential Outputs
- Asynchronous Master Slave
- Dual Latch-Enable
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

PIN NAME

Pin	Function
D_0x- D_3x	Input Data
SEL0, SEL1	Select Inputs
LEN1, LEN2	Latch Enable
MR	Master Reset
Q_0 - Q_5	True Outputs
$\overline{Q}_0$ - $\overline{Q}_5$	Inverted Outputs



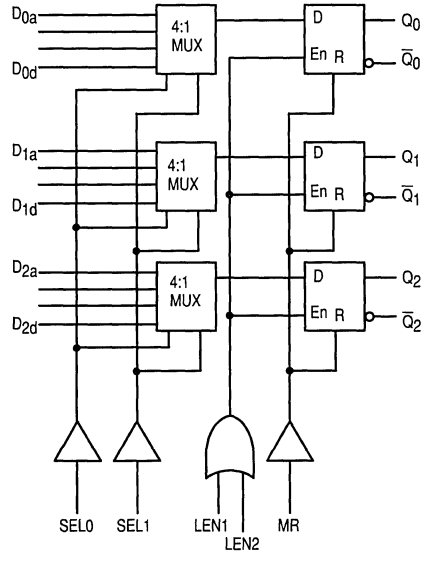
Military 100E556

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		μA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input Current High		150		150		150	μA	V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.
I_{EE}	Power Supply Current		90		103		90	mA	V_{EE} (MAX), V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.

5

FUNCTION TABLE		
SEL0	SEL1	Data
L	L	a
H	L	b
L	H	c
H	H	d

FUNCTION TABLE		
LEN1	LEN2	Latch
L	L	Transp.
H	X	Latch
X	H	Latch

AC CHARACTERISTICS: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
	D	400	900	400	900	400	900	ps	
	SEL0	550	1050	550	1050	550	1050	ps	
	SEL1	450	900	450	900	450	900	ps	
	LEN	350	800	350	900	350	800	ps	
	MR	350	825	350	825	350	825	ps	
t_S	Setup Time								V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
	D	400		400		400		ps	
	SEL0	700		700		700		ps	
	SEL1	600		600		600		ps	
t_H	Hold Time								V_{IL} = 0.295 V, V_{IH} = 1.045 V, R_L = 50Ω to Gnd.
	D	300		300		300		ps	
	SEL0	100		100		100		ps	
	SEL1	200		200		200		ps	
t_{RR}	Reset Recovery Time	800		800		800		ps	
t_{PW}	Minimum Pulse Width MR	400		400		400		ps	
t_{Skew}	Within-device Skew	50		50		50		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	275	700	275	700	275	700	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

5

MOTOROLA

5-Bit 2:1 Multiplexer

Military 100E558

Product Preview

ELECTRICALLY TESTED PER:
100E558

The 100E558 contains five 2:1 multiplexers with differential outputs. The output data are controlled by the Select input (SEL).

- 600 ps Max. D to Output
- 800 ps Max. SEL to Output
- Differential Outputs
- One V_{CCO} Pin Per Output Pair
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

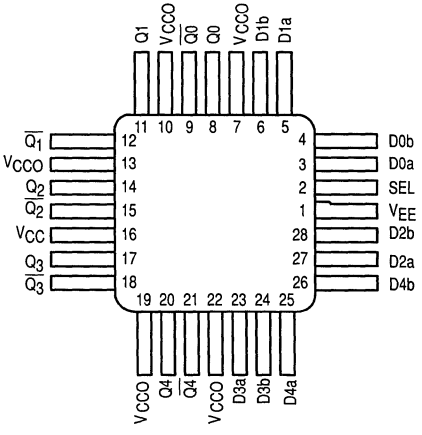
PIN NAME

Pin	Function
D_0a - D_4a	Inputs Data a
D_0b - D_4b	Inputs Data b
SEL	Select Input
Q_0 - Q_4	True Outputs
$\overline{Q_0}$ - $\overline{Q_4}$	Inverted Outputs

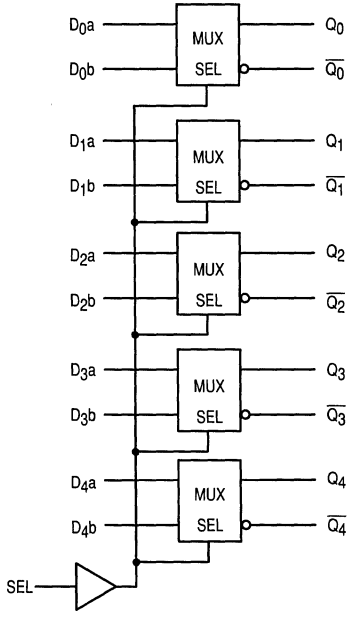
5

Function Table

SEL	Data
H	a
L	b



LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current							µA	
	D		200		200		200		
	SEL		150		150		150		
I_{EE}	Power Supply Current		40		46		40	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output								
	D	225	550	225	550	225	550	ps	
	SEL	400	775	400	775	400	775	ps	
t_{Skew}	Within-device Skew		60		60		60	ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80%	275	650	275	650	275	650	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.

5

MOTOROLA

6-Bit D Register Differential Data & Clock

Military 100E851

Product Preview

ELECTRICALLY TESTED PER:
100E851

The 100E851 contains 6 D-type flip-flops with single-ended outputs and differential data inputs. The common clock input is also differential. The registers are triggered by a positive transition of the positive clock (Clk) input.

A High on the Master Reset (MR) input resets all Q outputs to Low. The V_{BB} output is intended for use as a reference voltage for single-ended reception of ECL signals to that device only. When used for this purpose, it is recommended that V_{BB} is decoupled to V_{CC} via a 0.01 μF capacitor.

- Differential Inputs: Data and Clock
- V_{BB} Outputs
- 1100 MHz Min. Toggle Frequency
- Asynchronous Master Reset
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

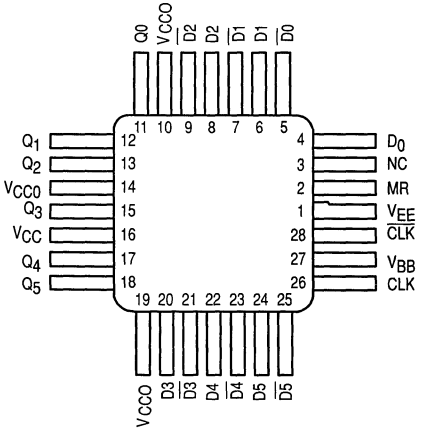
AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

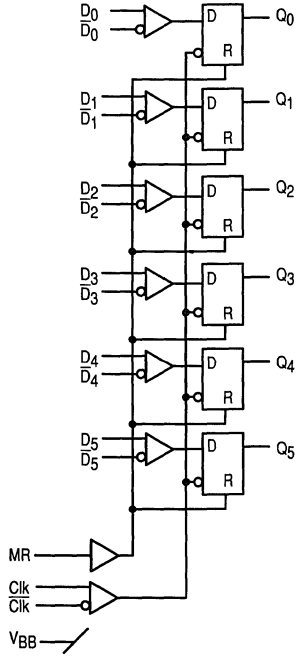
PACKAGE: NON-Compliant
QFP: X

PIN NAME

Pin	Function
D_0 - D_5	+ Data Inputs
$\overline{D_0}$ - $\overline{D_5}$	- Data Inputs
CLK	+ Clock Inputs
$\overline{CLK}$	- Clock Inputs
MR	Master Reset
V_{BB}	V_{BB} Output
Q_0 - Q_5	Data Outputs



LOGIC DIAGRAM



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100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, V_{CC} = V_{CCO} = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	V_{IN} = $V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or V_{IN} = $V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	V_{IN} = $V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or V_{IN} = $V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	V_{IN} = $V_{IL(min)}$	

DC CHARACTERISTICS: V_{EE} = $V_{EE(min)}$ to $V_{EE(max)}$, V_{CC} = V_{CCO} = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
V_{BB}	Output Reference Voltage	-1.38	-1.26	-1.38	-1.26	-1.38	-1.26	V	V_{IL} = Open, V_{IH} = Open, R_L = 50Ω to – 2.0 V.
I_{IH}	Input Current High		150		150		150	µA	V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.
I_{EE}	Power Supply Current		101		116		101	mA	V_{EE} (MAX), V_{IL} = – 1.810 V, V_{IH} = – 0.880 V, R_L = 50Ω to – 2.0 V.
V_{CMR}	Common Mode Range	-2.0	-0.4	-2.0	-0.4	-2.0	-0.4	V	(Note 1)

1. V_{CMR} is referenced to the most positive side of the differential input signal. Normal operations obtained when the "HIGH" input is within the V_{CMR} range and the input swing is greater than V_{PPMIN} and < 1.0 V.

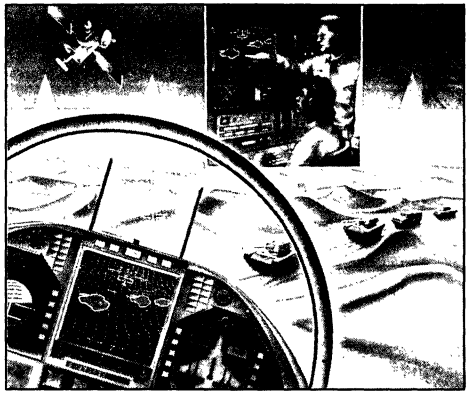
5

AC CHARACTERISTICS: $V_{EE} = V_{EE}(min)$ to $V_{EE}(max)$, $V_{CC} = V_{CCO} = GND$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Toggle Frequency	1100		1100		1100		MHz	V_{IL} = 0.295 V, V_{IH} = 1.045 V, Dn = 0.670 V, $\overline{Clk}$ = 0.670 V, R_L = 50Ω to Gnd.
t_{PLH} t_{PHL}	Propagation Delay to Output								V_{IL} = 0.295 V, V_{IH} = 1.045 V, Dn = 0.670 V, $\overline{Clk}$ = 0.670 V, R_L = 50Ω to Gnd.
	CLK (Diff)	475	800	475	800	475	800	ps	
	CLK (SE)	425	850	425	850	425	850	ps	
	MR	425	850	425	850	425	850	ps	
t_S	Setup Time, D	150		150		150		ps	V_{IL} = 0.295 V, V_{IH} = 1.045 V, Dn = 0.670 V, $\overline{Clk}$ = 0.670 V, R_L = 50Ω to Gnd.
t_H	Hold Time, D	250		250		250		ps	V_{IL} = 0.295 V, V_{IH} = 1.045 V, Dn = 0.670 V, $\overline{Clk}$ = 0.670 V, R_L = 50Ω to Gnd.
$V_{PP}(AC)$	Minimum Input Swing	150		159		150		mV	(Note 1)
t_{RR}	Reset Recovery Time	750		750		750		ps	
t_{PW}	Minimum Pulse Width CLK, MR	400		400		400		ps	
t_{Skew}	Within-device Skew	100		100		100		ps	(Note 2)
t_r t_f	Rise/Fall Times 20 - 80%	275	800	275	800	275	800	ps	

5

1. Minimum input voltage for AC parameters are guaranteed.
2. Within-device skew is defined as identical transitions on similar paths through a device.



Phase-Locked Loop 6

Analog Mixer

Military 12502

ELECTRICALLY TESTED PER:
MPG 12502

The 12502 is a double balanced analog mixer, including an input amplifier feeding the mixer carrier port and a temperature compensated bias regulator. The input circuits for both the amplifier and mixer are differential amplifier circuits. The on-chip regulator provides all of the required biasing.

This circuit is designed for use as a balanced mixer in high-frequency wideband circuits. Other typical applications include suppressed carrier and amplitude modulation, synchronous AM detection, FM detection, phase detection, and frequency doubling, at frequencies up to UHF.

AVAILABLE AS

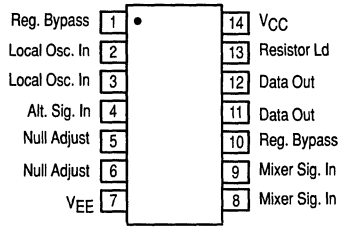
1) JAN: N/A
2) SMD: N/A
3) 883: 12502/BXAJC

X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: C

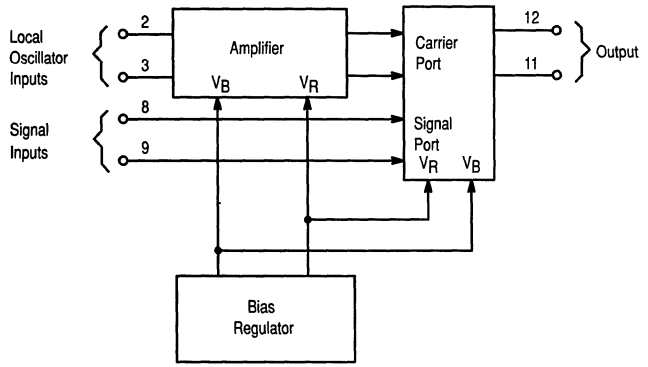
PIN ASSIGNMENTS

FUNCTION	DIL	BURN-IN (CONDITION C)
Reg. Bypass	1	V_{CC}
Local Osc. In	2	OPEN
Local Osc. In	3	OPEN
Alt. Sig. In	4	OPEN
Null Adjust	5	OPEN
Null Adjust	6	OPEN
V_{EE}	7	OPEN
Mixer Sig. In	8	GND
Mixer Sig. In	9	GND
Reg. Bypass	10	V_{CC}
Data Out	11	V_{CC}
Data Out	12	OPEN
Resistor Load	13	OPEN
V_{CC}	14	OPEN

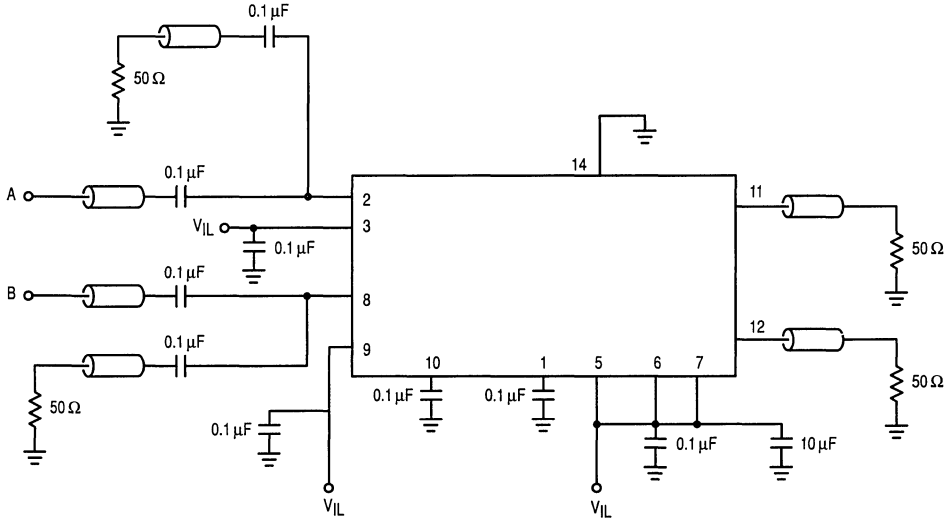


BURN - IN CONDITIONS:
V_{CC} = +6.0 V MAX/ +5.0 V MIN

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		+ 7.0	Vdc
Output Voltage	V_{OUT}		+ 5.5	Vdc
Input Voltage	V_{IN}		+ 5.5	Vdc
Operating Temperature Range	T_A	− 55	+ 125	°C
Storage Temperature Range	T_{stg}	− 65	+ 175	°C



NOTES

1. V_{IL} = − 3.0 V on pin 3 when pin 8 is under test.
   V_{IL} = − 3.0 V on pin 9 when pin 2 is under test.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
3. All unused cables to the scope must be terminated with a 50 Ω ± 1.0% resistor.
4. f = 100 MHz.
5. Signal A = 30 mVp-p.
   Signal B = 300 mVp-p.

Figure 1. Test Circuit

6

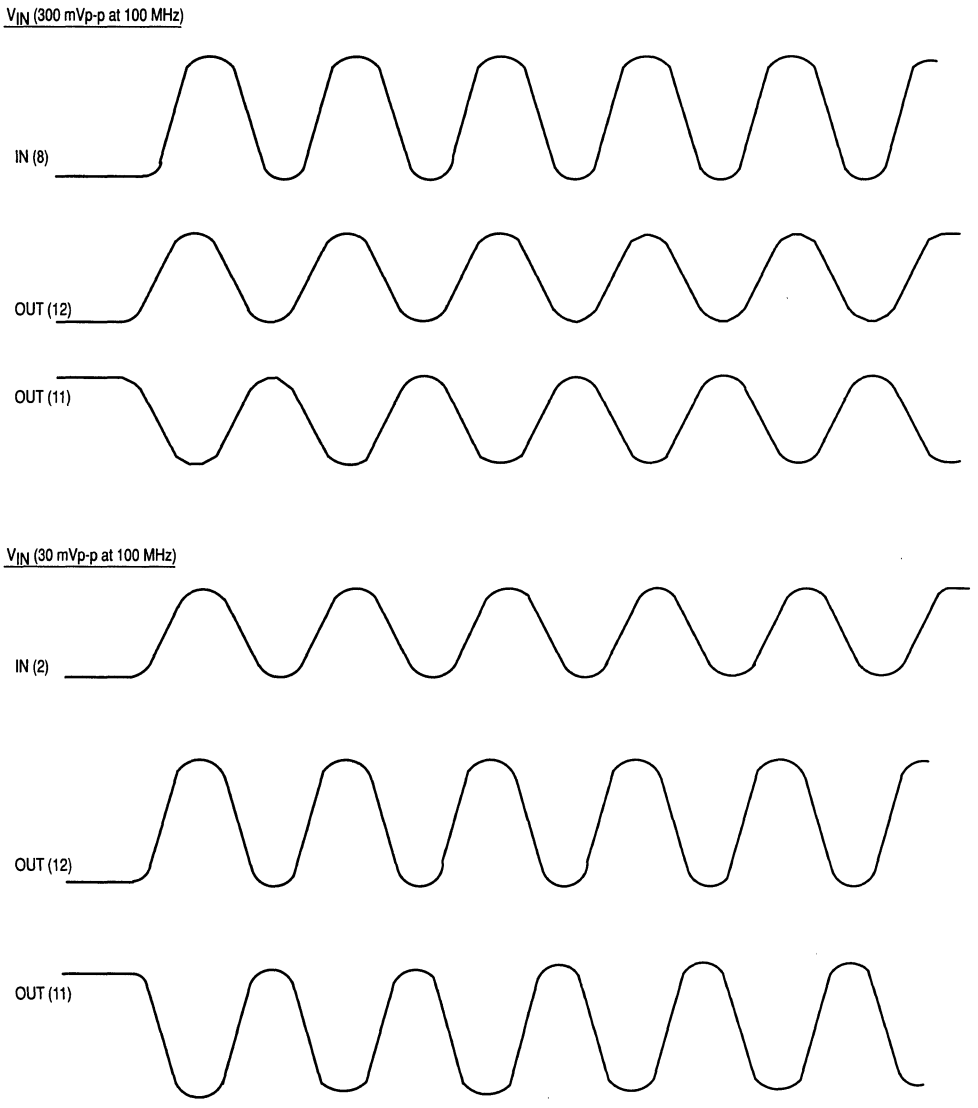


Figure 2. Frequency Diagram

12502
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)				
	V_{IH}	V_{IL}	V_{ILX}	V_{CC}	V_{EE}
T_A = 25 °C	+ 2.9	+ 2.0	-3.0	+ 5.0	-5.0
T_A = 125 °C	+ 2.9	+ 2.0		+ 5.0	
T_A = -55 °C	+ 2.9	+ 2.0		+ 5.0	

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to Gnd				
		Subgroup 1		Subgroup 2		Subgroup 3							
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{CC}	V_{EE}	P.U.T.
$V_{Bias\ 1}$	Bias Voltage	2.32	2.52	2.29	2.49	2.34	2.54	V			11, 12, 14	5 - 7	1
$V_{Bias\ 4}$	Bias Voltage	400	600	420	620	390	590	mV			11, 12, 14	5 - 7	4
$V_{Bias\ 5}$	Bias Voltage	285	425	305	445	275	415	mV			11, 12, 14	5 - 7	5
$V_{Bias\ 6}$	Bias Voltage	285	425	305	445	275	415	mV			11, 12, 14	5 - 7	6
$V_{Bias\ 10}$	Bias Voltage	1.185	1.385	1.05	1.25	1.3	1.5	V			11, 12, 14	5 - 7	10
I_{CC1}	Power Supply Drain Current	0.7	1.3					mA			11, 12, 14	5 - 7	11, 12
ΔI_{CC1}	Differential Current	- 50	50					µA			11, 12, 14	5 - 7	11, 12
I_{CC2}	Power Supply Drain Current	2.1	3.9					mA			11, 12, 14	5 - 7	11, 12
ΔI_{CC2}	Differential Current	- 100	100					µA			11, 12, 14	5 - 7	11, 12
I_{CC3}	Power Supply Drain Current		16.0					mA			11, 12, 14	5 - 7	14
I_{INH}	Input Current High		0.75					mA	2, 3, 8, 9		11, 12, 14	5 - 7	2, 3, 8, 9
I_{INL}	Input Current Low	- 0.7						mA		2, 3, 8, 9	11, 12, 14	5 - 7	2, 3, 8, 9
I_{OUT}	Output Current	4.2	7.8					mA	2, 3, 8, 9		11, 12, 14	2, 3, 8, 9	11, 12

12502
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)				
	V_{IH}	V_{IL}	V_{ILX}	V_{CC}	V_{EE}
T_A = 25 °C	+ 2.9	+ 2.0	-3.0	+ 5.0	-5.0
T_A = 125 °C	+ 2.9	+ 2.0		+ 5.0	
T_A = -55 °C	+ 2.9	+ 2.0		+ 5.0	

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 50 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{ILX}	V_{IN}	V_{OUT}	V_{CC}	V_{EE}	P.U.T.
A_{V1}	AC Gain	180						mV	9	2	11, 12	14	7	11, 12
A_{V2}	AC Gain	100						mV	3	8	11, 12	14	7	11, 12

NOTE: AC Gain is a function of the collecter impedance.

Two Modulus Prescaler

Military 12509

ELECTRICALLY TESTED PER:
5962-8774801

The 12509 is a two-modulus prescaler which will divide by 5 and 6. A MECL-to-MTTL translator is provided to interface with the 12514 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

- 600 MHz (Typ) Toggle Frequency
- 12509 (÷ 5/6)
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- + 5.0 or – 5.2 V Operation *
- Buffered Clock Input — Series-Input RC Typ, 20 Ohms and 4.0 pF
- V_{BB} Reference Voltage
- 460 mW Max/Pkg (No Load)

AVAILABLE AS

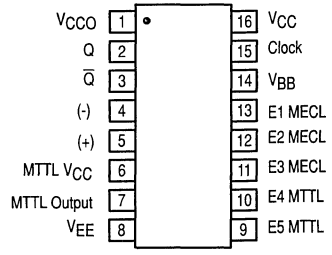
1) JAN: N/A
2) SMD: 5962-8774801
3) 883: 12509/BXAJC

X = CASE OUTLINE AS FOLLOWS:

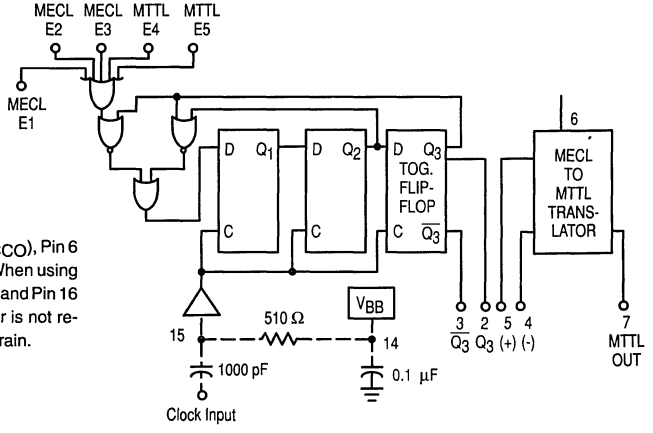
PACKAGE: CERDIP: E

PIN ASSIGNMENTS

FUNCTION	DIL	BURN-IN (CONDITION C)
V_{CCO}	1	GND
Q	2	51 Ω to V_{TT}
$\overline{Q}$	3	51 Ω to V_{TT}
(-)	4	51 Ω to V_{TT}
(+)	5	GND
MTTL V_{CC}	6	GND
MTTL Output	7	51 Ω to V_{TT}
V_{EE}	8	V_{EE}
E5 MTTL	9	GND
E4 MTTL	10	GND
E3 MECL	11	51 Ω to V_{TT}
E2 MECL	12	51 Ω to V_{TT}
E1 MECL	13	51 Ω to V_{TT}
V_{BB}	14	OPEN
Clock	15	51 Ω to V_{TT}
V_{CC}	16	GND



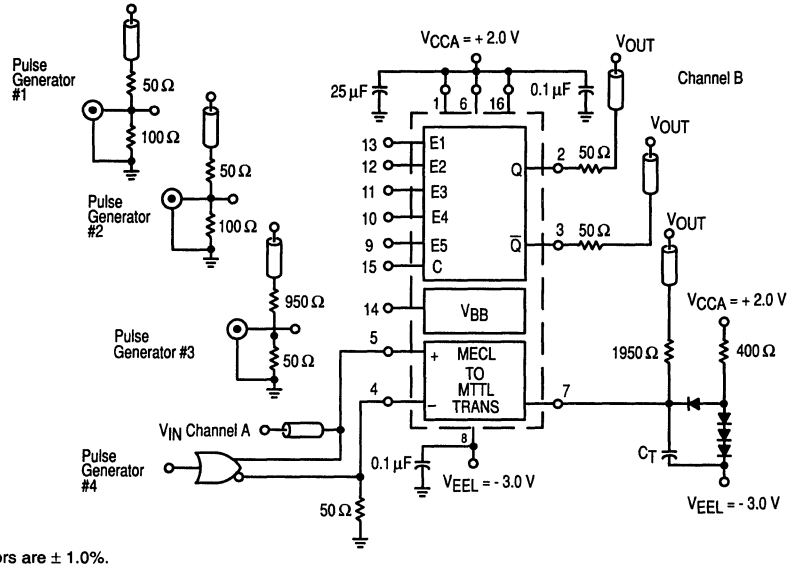
LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

* When using a + 5.0 V supply, apply + 5.0 V to Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), Pin 16 (V_{CC}), and ground Pin 8 (V_{EE}). When using –5.2 V supply, ground Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), and Pin 16 (V_{CC}) and apply 5.2 V to Pin 8 (V_{EE}). If the translator is not required, Pin 6 may be left open to conserve dc power drain.

ABSOLUTE MAXIMUM RATINGS	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		+ 7.0	Vdc
Output Voltage	V_{OUT}		+ 5.5	Vdc
Input Voltage	V_{IN}		+ 5.5	Vdc
Operating Temperature Range	T_A	− 55	+ 125	°C
Storage Temperature Range	T_{stg}	− 65	+ 165	°C



NOTES

1. All resistors are ± 1.0%.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
3. The 1950 Ω resistor at pin 7 and the scope termination impedance constitute a 40:1 attenuator probe.
4. All unused outputs must be terminated with 100 Ω to ground.
5. Pulse generator 1, 2, and 4 have the following characteristics:
   a) PRF = 10 MHz.
   b) PW = 50% duty cycle.
   c) $t_r = t_f = 2.0$ ns ± 0.2 ns.
6. Pulse generator 3 has the following characteristics:
   a) PRF = 2.0 MHz.
   b) PW = 50% duty cycle.
   c) $t_r = t_f = 5.0$ ns ± 0.5 ns.

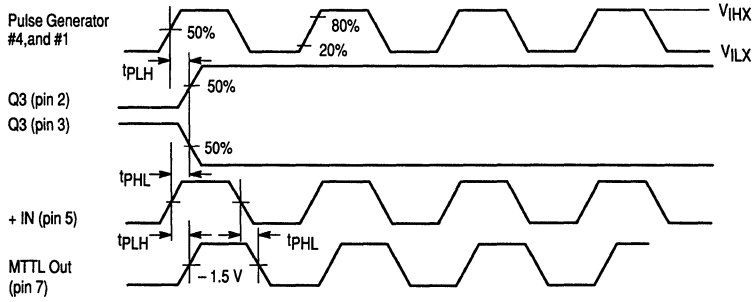


Figure 1. Switching Test Circuit and Waveforms

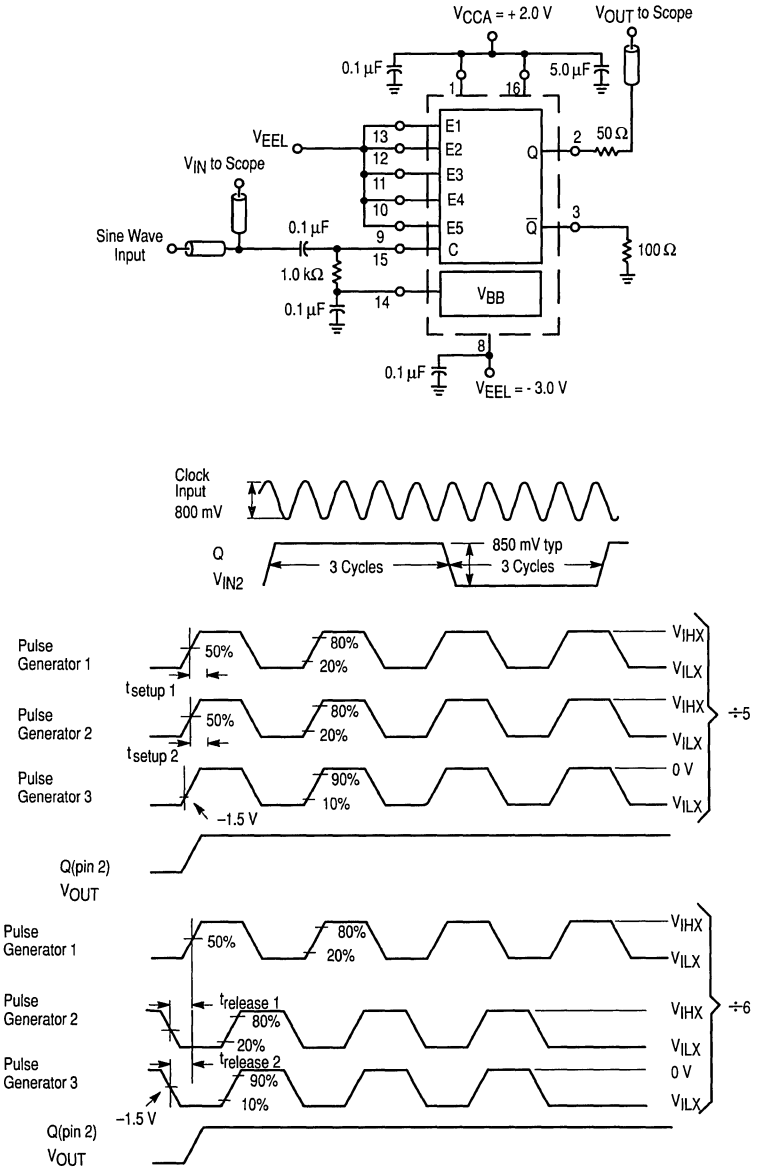


Figure 2. Switching Test Circuit and Waveforms

6

Sequence Table 1

(Use with V_{OH1}, V_{OL1}, V_{OHA}, V_{OLA} tests)

ENABLE INPUTS						
TTL 9	TTL 10	ECL 10	ECL 12	ECL 13	ECL 15	
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	+6
V_{IH}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	+5
V_{IL}	V_{IH}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	+5
V_{IL}	V_{IL}	V_{IHB}	V_{ILB}	V_{ILB}	C_{P1}	+5
V_{IL}	V_{IL}	V_{ILB}	V_{IHB}	V_{ILB}	C_{P1}	+5
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{IHB}	C_{P1}	+5

Sequence Table 2

(Use with V_{OH1}, V_{OL1}, V_{OHA}, V_{OLA} tests)

ENABLE INPUTS						
TTL 9	TTL 10	ECL 11	ECL 12	ECL 13	ECL 15	
V_{ILT}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	6
V_{IL}	V_{ILT}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	6
V_{IL}	V_{IL}	V_{ILA}	V_{ILB}	V_{ILB}	C_{P1}	6
V_{IL}	V_{IL}	V_{ILB}	V_{ILA}	V_{ILB}	C_{P1}	6
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILA}	C_{P1}	6
V_{IHT}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	5
V_{IL}	V_{IHT}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}	5
V_{IL}	V_{IL}	V_{IHA}	V_{ILB}	V_{ILB}	C_{P1}	5
V_{IL}	VIL	V_{ILB}	V_{IHA}	V_{ILB}	C_{P1}	5
V_{IL}	VIL	V_{ILB}	V_{ILB}	V_{IHA}	C_{P1}	5

State Diagram

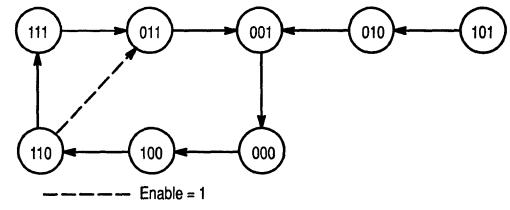
6

Enable = 0

Q_1	Q_2	Q_3
1	1	1
0	1	1
0	0	1
0	0	0
1	0	0
1	1	0

Enable = 1

NOTE: The state of the enable is important only for the positive clock transition when the counter is in the state 110.



12509
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)															Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{IHT}	V_{ILT}	V_{EE}	V_{CC}	V_{IHX}	V_{ILX}	V_{ILL}	V_{EEL}	V_{CCA}	I_L	I_{OL}	I_{OH}
T_A = 25 °C	+ 2.4	+ 0.5	+ 3.895	+ 3.525	+ 4.22	+ 3.11	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.15	+ 0.215	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = -55 °C	+ 2.4	+ 0.5	+ 3.745	+ 3.5	+ 4.12	+ 3.04	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.02	+ 0.165	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C Subgroup 1		+ 125 °C Subgroup 2		- 55 °C Subgroup 3			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 3.0 V								
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	$V_{IHA/B}$	$V_{ILA/B}$	V_{CC}	V_{EE}	C_{P1}	$I_{OH/OL}$	P.U.T.
V_{OH1}	Output Voltage High	4.03	4.22	4.135	4.37	3.88	4.12	V	9, 10	[1]9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 2)
V_{OH2}	Output Voltage High	2.70	4.22	3.00	4.37	2.40	4.12	V			5	4	6	8		7 I_{OH}	7
V_{OL1}	Output Voltage Low	3.11	3.44	3.14	3.515	3.04	3.405	V	9, 10	9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 2)
V_{OL2}	Output Voltage Low	0.10	0.80	0.10	0.66	0.10	1.00	V			4	5	6	8		7 I_{OL}	7
V_{OHA}	Output Voltage High	4.01	4.22	4.115	4.37	3.86	4.12	V		9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 3)
V_{OLA}	Output Voltage Low	3.11	3.46	3.14	3.535	3.04	3.425	V		9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 3)
V_{BB1}	Reference Bias Supply Voltage	3.67	3.87					V					1, 16	8		14	14
I_{OS}	Output Short Circuit Current	- 65	- 20	- 65	- 20	- 65	- 20	mA		7	5	5	6	8			7
I_{CC1}	Power Supply Current	- 80	- 10	- 80	- 10	- 88	- 10	mA					1, 16	8			8
I_{CC2}	Power Supply Current	0.5	5.2	0.5	5.2	0.5	5.2	mA			4	4	6	8			6

1. Power Supply Voltage = 5.0 V, Power Supply Voltage = - 5.2 V is guaranteed but not tested.
2. See sequence table 1.
3. See sequence table 2.

12509
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)															Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{IHT}	V_{ILT}	V_{EE}	V_{CC}	V_{IHX}	V_{ILX}	V_{ILL}	V_{EEL}	V_{CCA}	I_L	I_{OL}	I_{OH}
T_A = 25 °C	+ 2.4	+ 0.5	+ 3.895	+ 3.525	+ 4.22	+ 3.11	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.15	+ 0.215	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = -55 °C	+ 2.4	+ 0.5	+ 3.745	+ 3.5	+ 4.12	+ 3.04	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.02	+ 0.165	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 3.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	$V_{IHA/B}$	$V_{ILA/B}$	V_{CC}	V_{EE}	P.U.T.
I_{INH1}	Input Current High		250		400		400	µA		9, 10	11 - 13, 15		1, 16	8	11, 12, 13, 15
I_{INH2}	Input Current High	2.0	6.0	2.0	6.4	1.7	6.0	mA			4, 5	4, 5	6	8	4, 5
I_{INH3}	Input Current High	1.0	3.0	1.0	3.6	0.7	3.0	mA			5	5	6	8	5
I_{INH4}	Input Current High		100		100		100	µA	9, 10				1, 16	8	9, 10
I_{INI1}	Input Current Low	- 10		- 10		- 10		µA					1, 16	8, 15, 11 - 13	11, 12, 13, 15
I_{INI1}	Input Current Low	- 1.6		- 1.6		- 1.6		mA		9, 10			1, 16	8	9, 10

1. Power Supply Voltage = 5.0 V, Power Supply Voltage = - 5.2 V is guaranteed but not tested.

* **ELECTRICAL CHARACTERISTICS**: This device is designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100 Ω resistor to + 3.0 V.

12509
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)															Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{IHT}	V_{ILT}	V_{EE}	V_{CC}	V_{IHX}	V_{ILX}	V_{ILL}	V_{EEL}	V_{CCA}	I_L	I_{OL}	I_{OH}
T_A = 25 °C	+ 2.4	+ 0.5	+ 3.895	+ 3.525	+ 4.22	+ 3.11	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.15	+ 0.215	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = -55 °C	+ 2.4	+ 0.5	+ 3.745	+ 3.5	+ 4.12	+ 3.04	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.02	+ 0.165	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 0.0 V						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}	V_{CCA}	V_{EEL}	P.U.T.
t_{PLH}	Propagation Delay	4.8	8.1		9.4		8.1	ns	9, 10	11 - 13	15	2, 3	1, 16	8	2, 3
t_{PHL}	Propagation Delay	4.8	7.5		8.7		7.5	ns	9, 10	11 - 13	15	2, 3	1, 16	8	2, 3
t_{PLH}	Propagation Delay	3.4	8.1		9.4		8.1	ns	9, 10	11 - 13	15	2, 3	1, 16	8	7
t_{PHL}	Propagation Delay	3.0	6.5		7.6		6.5	ns	9, 10	11 - 13	15	2, 3	1, 16	8	7
		Min	Typ	Min	Max	Min	Max		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}	V_{CCA}	V_{EEL}	P.U.T.
$t_{Setup\ 1}$	Setup Time MECL	5.0	2.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
$t_{Setup\ 2}$	Setup Time MTTL	5.0	3.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
$t_{Rel\ 1}$	Release Time MECL	5.0	2.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
$t_{Rel\ 2}$	Release Time MTTL	5.0	3.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
		Min	Typ	Min	Typ	Min	Typ		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}	V_{CCA}	V_{EEL}	P.U.T.
$f_{max} \div 6$	Toggle Frequency	480	520	420	440	420	500	MHz			15	2	1, 6, 16	8 - 13	2

Two Modulus Prescaler

Military 12511

ELECTRICALLY TESTED PER:
MPG 12511

The 12511 is a two-modulus prescaler which will divide by 8 and 9. A MECL-to-MTTL translator is provided to interface with the 12514 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

- 600 MHz (Typ) Toggle Frequency
- 12511 (÷ 8/9)
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- + 5.0 or – 5.2 V Operation *
- Buffered Clock Input Series Input RC Typ, 20 Ohms and 4.0 pF
- V_{BB} Reference Voltage
- 460 mW Max/Pkg (No Load)

AVAILABLE AS

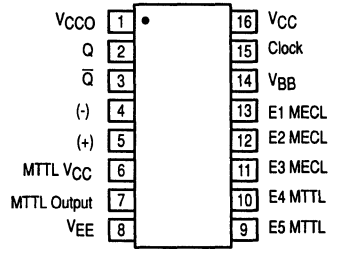
1) JAN: N/A
2) SMD: N/A
3) 883: 12511/BXAJC

X = CASE OUTLINE AS FOLLOWS:

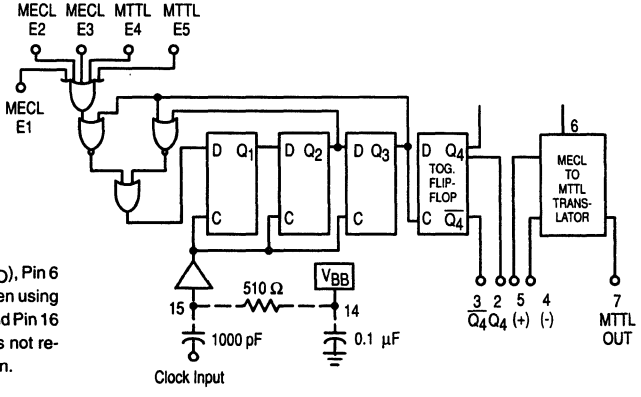
PACKAGE: CERDIP: E
CERFLAT: F

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CCO}	1	1	GND
Q	2	2	51 Ω to V_{TT}
$\overline{Q}$	3	3	51 Ω to V_{TT}
(–)	4	4	51 Ω to V_{TT}
(+)	5	5	GND
MTTL V_{CC}	6	6	GND
MTTL Output	7	7	51 Ω to V_{TT}
V_{EE}	8	8	V_{EE}
E5 MTTL	9	9	GND
E4 MTTL	10	10	GND
E3 MECL	11	11	51 Ω to V_{TT}
E2 MECL	12	12	51 Ω to V_{TT}
E1 MECL	13	13	51 Ω to V_{TT}
V_{BB}	14	14	OPEN
Clock	15	15	51 Ω to V_{TT}
V_{CC}	16	16	GND



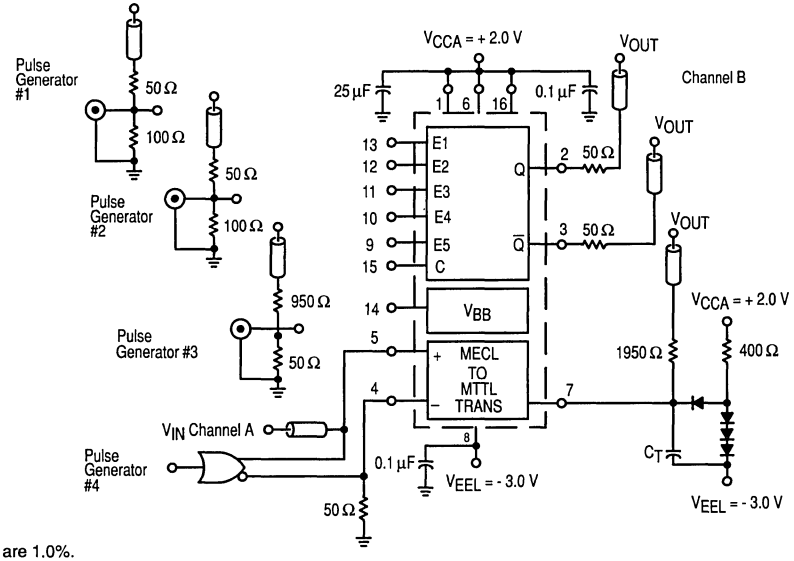
LOGIC DIAGRAM



BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

* When using a + 5.0 V supply, apply + 5.0 V to Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), Pin 16 (V_{CC}), and ground Pin 8 (V_{EE}). When using –5.2 V supply, ground Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), and Pin 16 (V_{CC}) and apply 5.2 V to Pin 8 (V_{EE}). If the translator is not required, Pin 6 may be left open to conserve dc power drain.

ABSOLUTE MAXIMUM RATINGS	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		+ 7.0	Vdc
Output Voltage	V_{OUT}		+ 5.5	Vdc
Input Voltage	V_{IN}		+ 5.5	Vdc
Operating Temperature Range	T_A	− 55	+ 125	°C
Storage Temperature Range	T_{stg}	− 65	+ 175	°C



NOTES

1. All resistors are 1.0%.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
3. The 1950 Ω resistor at pin 7 and the scope termination impedance constitute a 40:1 attenuator probe.
4. All unused outputs must be terminated with 100 Ω to ground.
5. Pulse generator 1, 2, and 4 have the following characteristics:
   a) PRF = 10 MHz.
   b) PW = 50% duty cycle.
   c) $t_r = t_f = 2.0$ ns ± 0.2 ns.
6. Pulse generator 3 has the following characteristics:
   a) PRF = 2.0 MHz.
   b) PW = 50% duty cycle.
   c) $t_r = t_f = 5.0$ ns ± 0.5 ns.

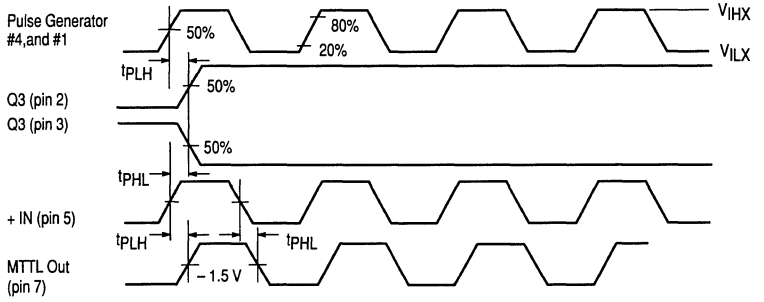


Figure 1. Switching Test Circuit and Waveforms

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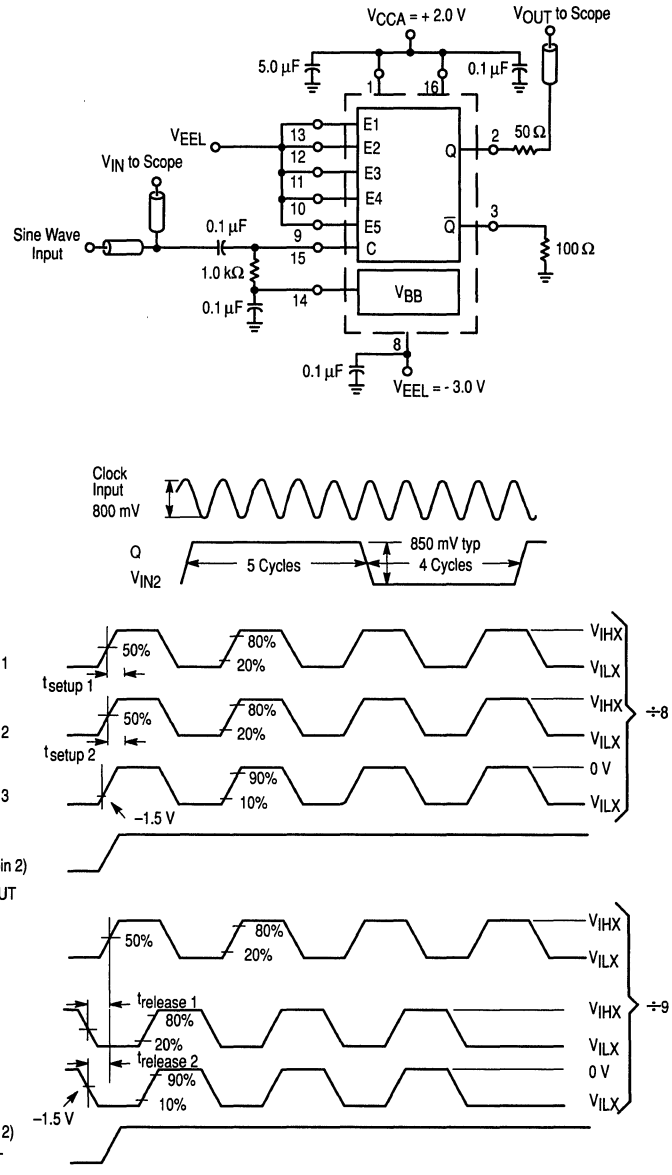


Figure 2. Switching Test Circuit and Waveforms

Sequence Table 1

(Use with V_{OH1}, V_{OL1}, V_{OHA}, V_{OLA} tests)

ENABLE INPUTS					
TTL 9	TTL 10	ECL 10	ECL 12	ECL 13	ECL 15
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IH}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IH}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{IHB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{ILB}	V_{IHB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{IHB}	C_{P1}

Sequence Table 2

(Use with V_{OH1}, V_{OL1}, V_{OHA}, V_{OLA} tests)

ENABLE INPUTS					
TTL 9	TTL 10	ECL 11	ECL 12	ECL 13	ECL 15
V_{ILT}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{ILT}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{ILA}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{ILB}	V_{ILA}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILA}	C_{P1}
V_{IHT}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IHT}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{IHA}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	VIL	V_{ILB}	V_{IHA}	V_{ILB}	C_{P1}
V_{IL}	VIL	V_{ILB}	V_{ILB}	V_{IHA}	C_{P1}

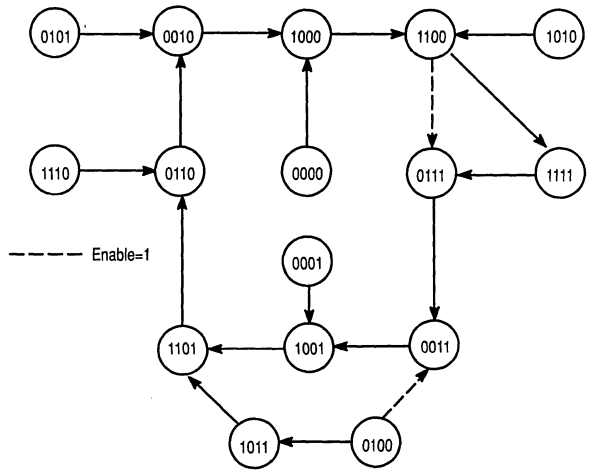
State Diagram

Q_1	Q_2	Q_3	Q_4
1	1	1	1
0	1	1	1
0	0	1	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
1	0	0	0
1	1	0	0

Enable = 1

Enable = 0

NOTE: The state of the enable is important only for the positive clock transition when the counter is in the state 1100.



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12511
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)															Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{IHT}	V_{ILT}	V_{EE}	V_{CC}	V_{IHX}	V_{ILX}	V_{ILL}	V_{EEL}	V_{CCA}	I_L	I_{OL}	I_{OH}
T_A = 25 °C	+ 2.4	+ 0.5	+ 3.895	+ 3.525	+ 4.22	+ 3.11	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.15	+ 0.215	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = -55 °C	+ 2.4	+ 0.5	+ 3.745	+ 3.5	+ 4.12	+ 3.04	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.02	+ 0.165	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 3.0 V								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	$V_{IHA/B}$	$V_{ILA/B}$	V_{CC}	V_{EE}	C_{P1}	$I_{OH/OL}$	P.U.T.
V_{OH1}	Output Voltage High	4.03	4.22	4.135	4.37	3.88	4.12	V	9, 10	9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 2)
V_{OH2}	Output Voltage High	2.70	4.22	3.00	4.37	2.40	4.12	V			4	5	6	8		7 I_{OH}	7
V_{OL1}	Output Voltage Low	3.11	3.44	3.14	3.515	3.04	3.405	V	9, 10	9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 2)
V_{OL2}	Output Voltage Low	0.10	0.80	0.10	0.66	0.10	1.00	V			4	5	6	8		7 I_{OL}	7
V_{OHA}	Output Voltage High	4.01	4.22	4.115	4.37	3.86	4.12	V		9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 3)
V_{OLA}	Output Voltage Low	3.11	3.46	3.14	3.535	3.04	3.425	V		9, 10	11 - 13	11 - 13	1, 16	8	15		2, 3 (Note 3)
V_{BB1}	Reference Bias Supply Voltage	3.67	3.87					V					1, 16	8		14	14
I_{OS}	Output Short Circuit Current	- 65	- 20	- 65	- 20	- 65	- 20	mA		7	5	4	6	8			7
I_{CC1}	Power Supply Current	- 80		- 80		- 88		mA					1, 16	8			8
I_{CC2}	Power Supply Current		5.2		5.2		5.2	mA			4	5	6	8			6

1. Power Supply Voltage = 5.0 V, Power Supply Voltage = - 5.2 V is guaranteed but not tested.
2. See sequence table 1.
3. See sequence table 2.

12511
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)															Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{IHT}	V_{ILT}	V_{EE}	V_{CC}	V_{IHX}	V_{ILX}	V_{ILL}	V_{EEL}	V_{CCA}	I_L	I_{OL}	I_{OH}
T_A = 25 °C	+ 2.4	+ 0.5	+ 3.895	+ 3.525	+ 4.22	+ 3.11	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.15	+ 0.215	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = -55 °C	+ 2.4	+ 0.5	+ 3.745	+ 3.5	+ 4.12	+ 3.04	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.02	+ 0.165	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C Subgroup 1		+ 125 °C Subgroup 2		- 55 °C Subgroup 3			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 3.0 V						
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	$V_{IHA/B}$	$V_{ILA/B}$	V_{CC}	V_{EE}	P.U.T.
I_{INH1}	Input Current High		250		400		400	µA		9, 10	11 - 13, 15		1, 16	8	11, 12, 13, 15
I_{INH2}	Input Current High	2.0	6.0	2.0	6.4	1.7	6.0	mA			4, 5	4, 5	6	8	4, 5
I_{INH3}	Input Current High	1.0	3.0	1.0	3.6	0.7	3.0	mA			4	5	6	8	5
I_{INH4}	Input Current High		100		100		100	µA	9, 10				1, 16	8	9, 10
I_{INI1}	Input Current Low	- 10		- 10		- 10		µA					1, 16	8, 15, 11 - 13	11, 12, 13, 15
I_{INI1}	Input Current Low	- 1.6		- 1.6		- 1.6		mA		9, 10			1, 16	8	9, 10

1. Power Supply Voltage = 5.0 V, Power Supply Voltage = - 5.2 V is guaranteed but not tested.

* **ELECTRICAL CHARACTERISTICS:** This device is designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100Ω resistor to + 3.0 V.

12511
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)															Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{IHT}	V_{ILT}	V_{EE}	V_{CC}	V_{IHX}	V_{ILX}	V_{ILL}	V_{EEL}	V_{CCA}	I_L	I_{OL}	I_{OH}
T_A = 25 °C	+ 2.4	+ 0.5	+ 3.895	+ 3.525	+ 4.22	+ 3.11	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.15	+ 0.215	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = -55 °C	+ 2.4	+ 0.5	+ 3.745	+ 3.5	+ 4.12	+ 3.04	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.02	+ 0.165	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to 0.0 V							
		Subgroup 9		Subgroup 10		Subgroup 11										
		Min	Max	Min	Max	Min	Max		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}	*	V_{CCA}	V_{EEL}	P.U.T.
t_{PHH}	Propagation Delay (15+ 2+)	4.8	8.1		9.4		8.1	ns	9, 10	11 - 13	15	2, 3	4, 5	1, 6, 16	8	2, 3
t_{PHH}	Propagation Delay (5+ 7+)	3.4	8.1		9.4		8.1	ns	9, 10	11 - 13	15	2, 3	4, 5	1, 6, 16	8	2, 3
t_{PLL}	Propagation Delay (15+ 2-)	4.8	7.5		8.7		7.5	ns	9, 10	11 - 13	15	2, 3	4, 5	1, 6, 16	8	7
t_{PLL}	Propagation Delay (5- 7-)	3.0	6.5		7.6		6.5	ns	9, 10	11 - 13	15	2, 3	4, 5	1, 6, 16	8	7
		Min	Typ	Min	Max	Min	Max		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}		V_{CCA}	V_{EEL}	P.U.T.
$t_{Setup\ 1}$	Setup Time MECL	5.0	2.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13			1, 6, 16	8	9 - 13
$t_{Setup\ 2}$	Setup Time MTTL	5.0	3.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13			1, 6, 16	8	9 - 13
$t_{Rel\ 1}$	Release Time MECL	5.0	2.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13			1, 6, 16	8	9 - 13
$t_{Rel\ 2}$	Release Time MTTL	5.0	3.0	5.0		5.0		ns	9, 10	11 - 13	9 - 13			1, 6, 16	8	9 - 13
		Min	Typ	Min	Typ	Min	Typ		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}		V_{CCA}	V_{EEL}	P.U.T.
f_{max} ÷9	Toggle Frequency	500	550	500	550	500	550	MHz			15	2		1, 6, 16	8 - 13	2

* See Figure 2.

MOTOROLA

Two Modulus Prescaler

Military 12513

ELECTRICALLY TESTED PER:
MPG 12513

The 12513 is a two-modulus prescaler which will divide by 10 and 11. A MECL-to-MTTL translator is provided to interface with the 12514 Counter Control Logic. In addition, there is a buffered clock input and MECL bias voltage source.

- 600 MHz (Typ) Toggle Frequency
- 12513 (+ 10/11)
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- + 5.0 or – 5.2 V Operation *
- Buffered Clock Input Series Input RC Typ, 20 Ohms and 4.0 pF
- V_{BB} Reference Voltage
- 460 mW Max/Pkg (No Load)

AVAILABLE AS

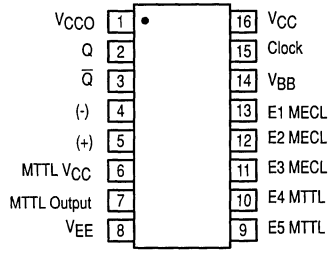
1) JAN: N/A
2) SMD: N/A
3) 883: 12513/BXAJC

X = CASE OUTLINE AS FOLLOWS:

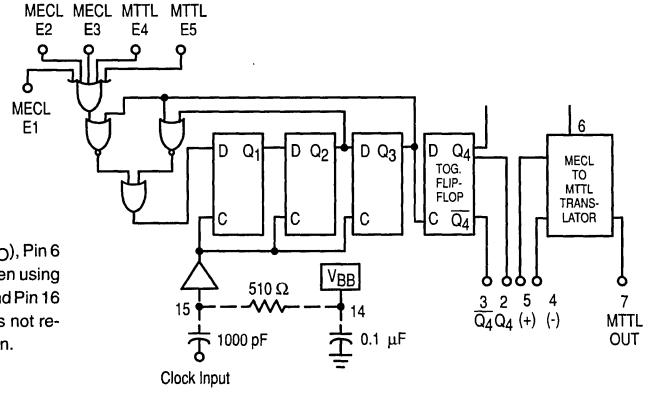
PACKAGE: CERDIP: E
CERFLAT: F

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	BURN-IN (CONDITION C)
V_{CCO}	1	1	GND
Q	2	2	51 Ω to V_{TT}
$\overline{Q}$	3	3	51 Ω to V_{TT}
(–)	4	4	51 Ω to V_{TT}
(+)	5	5	GND
MTTL V_{CC}	6	6	GND
MTTL Output	7	7	51 Ω to V_{TT}
V_{EE}	8	8	V_{EE}
E5 MTTL	9	9	GND
E4 MTTL	10	10	GND
E3 MECL	11	11	51 Ω to V_{TT}
E2 MECL	12	12	51 Ω to V_{TT}
E1 MECL	13	13	51 Ω to V_{TT}
V_{BB}	14	14	OPEN
Clock	15	15	51 Ω to V_{TT}
V_{CC}	16	16	GND



LOGIC DIAGRAM

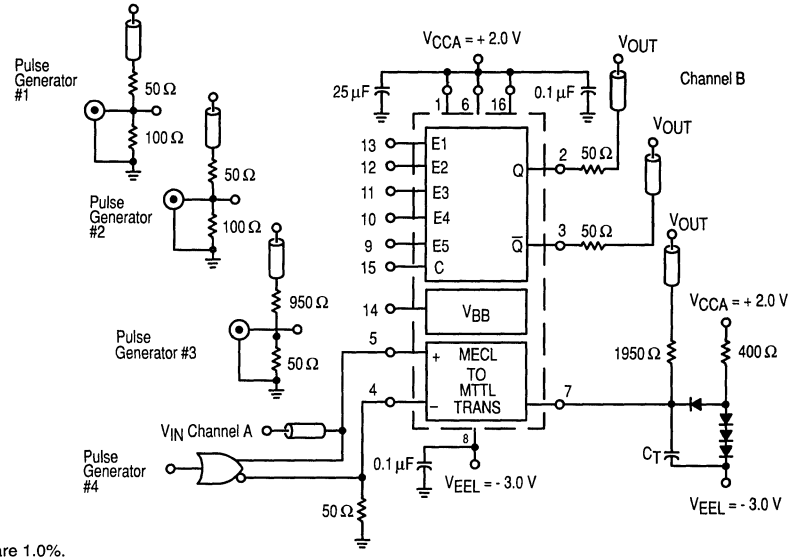


BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN

* When using a + 5.0 V supply, apply + 5.0 V to Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), Pin 16 (V_{CC}), and ground Pin 8 (V_{EE}). When using –5.2 V supply, ground Pin 1 (V_{CCO}), Pin 6 (MTTL V_{CC}), and Pin 16 (V_{CC}) and apply 5.2 V to Pin 8 (V_{EE}). If the translator is not required, Pin 6 may be left open to conserve dc power drain.

6

ABSOLUTE MAXIMUM RATINGS	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		+ 7.0	Vdc
Output Voltage	V_{OUT}		+ 5.5	Vdc
Input Voltage	V_{IN}		+ 5.5	Vdc
Operating Temperature Range	T_A	− 55	+ 125	°C
Storage Temperature Range	T_{stg}	− 65	+ 175	°C



NOTES

1. All resistors are 1.0%.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
3. The 1950 Ω resistor at pin 7 and the scope termination impedance constitute a 40:1 attenuator probe.
4. All unused outputs must be terminated with 100 Ω to ground.
5. Pulse generator 1, 2, and 4 have the following characteristics:
   a) PRF = 10 MHz.
   b) PW = 50% duty cycle.
   c) $t_r = t_f = 2.0$ ns ± 0.2 ns.
6. Pulse generator 3 has the following characteristics:
   a) PRF = 2.0 MHz.
   b) PW = 50% duty cycle.
   c) $t_r = t_f = 5.0$ ns ± 0.5 ns.

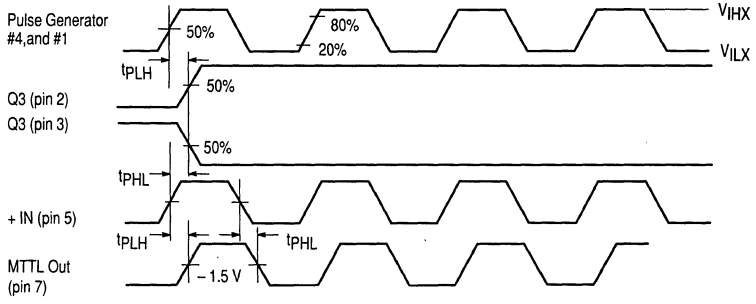


Figure 1. Switching Test Circuit and Waveforms

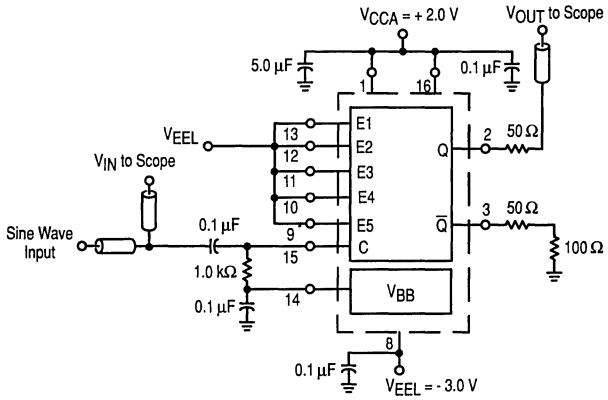


Figure 2. Switching Test Circuit and Waveforms

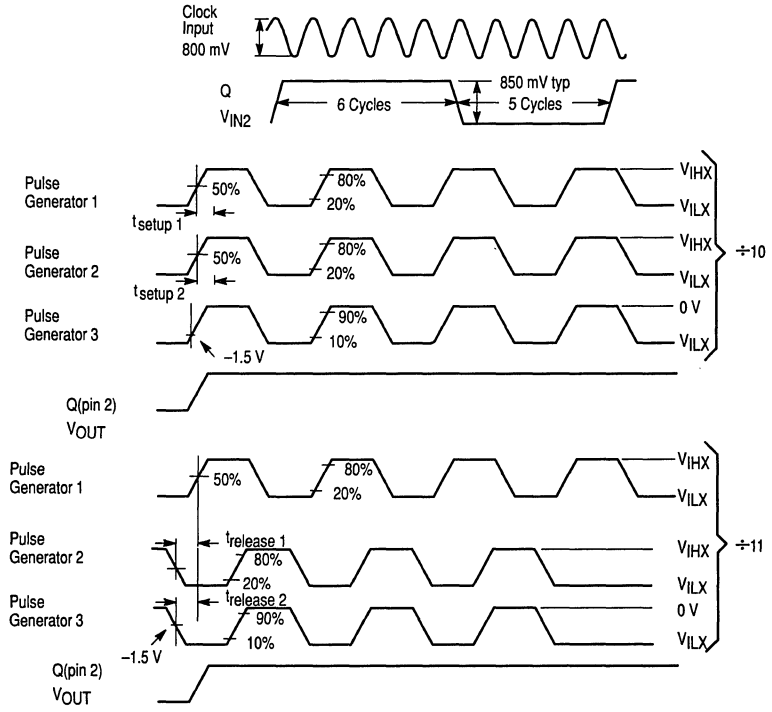


Figure 3. Maximum Frequency Test Circuit

6

Sequence Table 1

(Use with V_{OH1}, V_{OL1}, V_{OHA}, V_{OLA} tests)

ENABLE INPUTS					
TTL 9	TTL 10	ECL 11	ECL 12	ECL 13	ECL 15
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IH}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IH}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{IHB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{ILB}	V_{IHB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{IHB}	C_{P1}

Sequence Table 2

(Use with V_{OH1}, V_{OL1}, V_{OHA}, V_{OLA} tests)

ENABLE INPUTS					
TTL 9	TTL 10	ECL 11	ECL 12	ECL 13	ECL 15
V_{ILT}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{ILT}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{ILA}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{ILB}	V_{ILA}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILA}	C_{P1}
V_{IHT}	V_{IL}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IHT}	V_{ILB}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	V_{IL}	V_{ILA}	V_{ILB}	V_{ILB}	C_{P1}
V_{IL}	VIL	V_{ILB}	V_{ILA}	V_{ILB}	C_{P1}
V_{IL}	VIL	V_{ILB}	V_{ILB}	V_{ILA}	C_{P1}

6

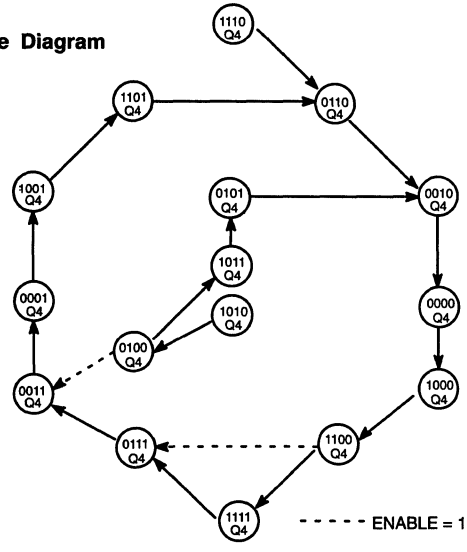
State Diagram

Q_1	Q_2	Q_3	Q_4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

Enable = 1

Enable = 0

NOTE: The state of the enable is important only for the positive clock transition when the counter is in the state 1100.



12513
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)															Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{IHT}	V_{ILT}	V_{EE}	V_{CC}	V_{IHX}	V_{ILX}	V_{ILL}	V_{EEL}	V_{CCA}	I_L	I_{OL}	I_{OH}
T_A = 25 °C	+ 2.4	+ 0.5	+ 3.895	+ 3.525	+ 4.22	+ 3.11	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.15	+ 0.215	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = -55 °C	+ 2.4	+ 0.5	+ 3.745	+ 3.5	+ 4.12	+ 3.04	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.02	+ 0.165	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW									
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 3.0 V									
		Subgroup 1		Subgroup 2		Subgroup 3												
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	$V_{IHA/B}$	$V_{ILA/B}$	V_{CC}	V_{EE}	C_{P1}	$I_{OH/OL}$	I_L	P.U.T.
V_{OH1}	Output Voltage High	4.03	4.22	4.135	4.37	3.88	4.12	V	9, 10	9, 10	11 - 13	11 - 13	1, 16	8	15			2, 3 (Note 2)
V_{OH2}	Output Voltage High	2.70	4.5	3.00	4.5	2.40	4.5	V			5	4	6	8		7 I_{OH}		7
V_{OL1}	Output Voltage Low	3.11	3.44	3.14	3.515	3.04	3.405	V	9, 10	9, 10	11 - 13	11 - 13	1, 16	8	15			2, 3 (Note 2)
V_{OL2}	Output Voltage Low	0.10	0.80	0.10	0.66	0.10	1.00	V			4	5	6	8		7 I_{OL}		7
V_{OHA}	Output Voltage High	4.01	4.5	4.115	4.5	3.86	4.5	V		9, 10	11 - 13	11 - 13	1, 16	8	15			2, 3 (Note 3)
V_{OLA}	Output Voltage Low	3.11	3.46	3.14	3.535	3.04	3.425	V		9, 10	11 - 13	11 - 13	1, 16	8	15			2, 3 (Note 3)
V_{BB1}	Reference Bias Supply Voltage	3.67	3.87					V					1, 16	8			14	14
I_{OS}	Output Short Circuit Current	- 65	- 20	- 65	- 20	- 65	- 20	mA		7	5	4	6	8				7
I_{CC1}	Power Supply Current	- 80		- 80		- 88		mA					1, 16	8				8
I_{CC2}	Power Supply Current		5.2		5.2		5.2	mA			4	5	6	8				6

1. Power Supply Voltage = 5.0 V, Power Supply Voltage = - 5.2 V is guaranteed but not tested.
2. See Sequence Table 1.
3. See Sequence Table 2.

12513
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)															Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{IHT}	V_{ILT}	V_{EE}	V_{CC}	V_{IHX}	V_{ILX}	V_{ILL}	V_{EEL}	V_{CCA}	I_L	I_{OL}	I_{OH}
T_A = 25 °C	+ 2.4	+ 0.5	+ 3.895	+ 3.525	+ 4.22	+ 3.11	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.15	+ 0.215	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = -55 °C	+ 2.4	+ 0.5	+ 3.745	+ 3.5	+ 4.12	+ 3.04	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.02	+ 0.165	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C Subgroup 1		+ 125 °C Subgroup 2		- 55 °C Subgroup 3			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 3.0 V						
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	$V_{IHA/B}$	$V_{ILA/B}$	V_{CC}	V_{EE}	P.U.T.
I_{INH1}	Input Current High		250		400		400	µA		9, 10	11 - 13, 15		1, 16	8	11, 12, 13, 15
I_{INH2}	Input Current High	2.0	6.0	2.0	6.4	1.7	6.0	mA			4, 5	4, 5	6	8	4, 5
I_{INH3}	Input Current High	1.0	3.0	1.0	3.6	0.7	3.0	mA			4	5	6	8	5
I_{INH4}	Input Current High		100		100		100	µA	9, 10				1, 16	8	9, 10
I_{INI1}	Input Current Low	- 10		- 10		- 10		µA					1, 16	8, 15, 11 - 13	11, 12, 13, 15
I_{INI1}	Input Current Low	- 1.6		- 1.6		- 1.6		mA		9, 10			1, 16	8	9, 10

1. Power Supply Voltage = 5.0 V, Power Supply Voltage = - 5.2 V is guaranteed but not tested.

* **ELECTRICAL CHARACTERISTICS**: This device is designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100 Ω resistor to + 3.0 V.

12513
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)															Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{IHT}	V_{ILT}	V_{EE}	V_{CC}	V_{IHX}	V_{ILX}	V_{ILL}	V_{EEL}	V_{CCA}	I_L	I_{OL}	I_{OH}
T_A = 25 °C	+ 2.4	+ 0.5	+ 3.895	+ 3.525	+ 4.22	+ 3.11	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.15	+ 0.215	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = 125 °C	+ 2.4	+ 0.5	+ 4.0	+ 3.6	+ 4.37	+ 3.14	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.27	+ 0.26	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4
T_A = -55 °C	+ 2.4	+ 0.5	+ 3.745	+ 3.5	+ 4.12	+ 3.04	+ 2.0	+ 0.8	0.0	+ 5.0	+ 1.02	+ 0.165	- 3.0	- 3.0	+ 2.0	- 0.25	+ 16	- 0.4

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 3.0 V						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}	V_{CCA}	V_{EEL}	P.U.T.
t_{PHH}	Propagation Delay (15+2+)		8.1		9.4		8.1	ns	9, 10	11 - 13	15	2, 3	1, 6, 16	8	2, 3
t_{PHH}	Propagation Delay (5+ 7+)		8.1		9.4		8.1	ns	9, 10	11 - 13	15	2, 3	1, 6, 16	8	2, 3
t_{PLL}	Propagation Delay (15+ 2-)		7.5		8.7		7.5	ns	9, 10	11 - 13	15	2, 3	1, 6, 16	8	7
t_{PLL}	Propagation Delay (5- 7-)		6.5		7.6		6.5	ns	9, 10	11 - 13	15	2, 3	1, 6, 16	8	7
		Min	Typ	Min	Max	Min	Max		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}	V_{CCA}	V_{EEL}	P.U.T.
$t_{Setup\ 1}$	Setup Time MECL	5.0		5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
$t_{Setup\ 2}$	Setup Time MTTL	5.0		5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
$t_{Rel\ 1}$	Release Time MECL	5.0		5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
$t_{Rel\ 2}$	Release Time MTTL	5.0		5.0		5.0		ns	9, 10	11 - 13	9 - 13		1, 6, 16	8	9 - 13
		Min	Typ	Min	Typ	Min	Typ		V_{ILL}	V_{ILX}	V_{IN}	V_{OUT}	V_{CCA}	V_{EEL}	P.U.T.
f_{max} ÷11	Toggle Frequency	550	600	500	540	500	600	MHz			15	2	1, 6, 16	8 - 13	2

Military 12514

Counter Control Logic

ELECTRICALLY TESTED PER:
MPG 12514

The 12514 monolithic counter control logic unit is designed for use with the 12513 Two Modulus Prescaler and the 4016 Programmable Counter to accomplish direct high-frequency programming. The 12514 consists of a zero detector which controls the modulus of the 12513, and an early decode function which controls the 4016. The early decode feature also increases the useful frequency range of the 4016 from 8.0 MHz to 25 MHz.

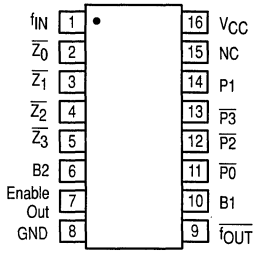
ABSOLUTE MAXIMUM RATINGS	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		+7.0	V_{dc}
Output Voltage	V_{OUT}		+5.5	V_{dc}
Input Voltage	V_{IN}		+5.5	V_{dc}
Operating Temperature Range	T_A	-55	+125	°C
Storage Temperature Range	T_{stg}	-65	+175	°C

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 12514/BXAJC

X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E

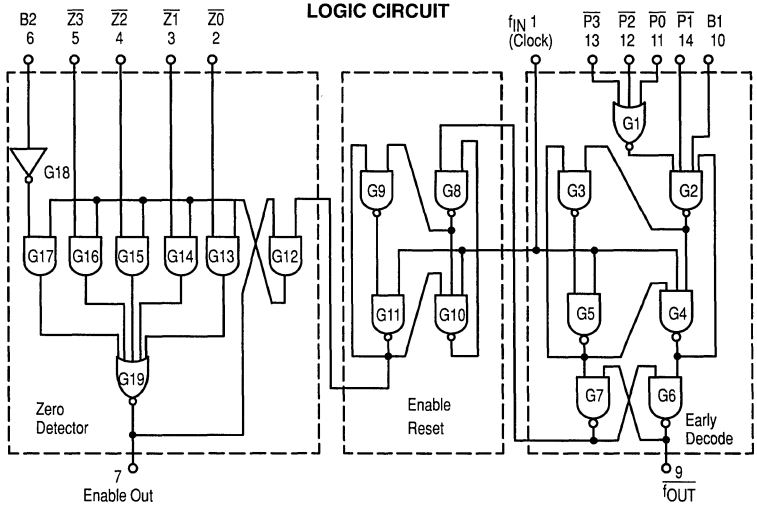


PIN ASSIGNMENTS

FUNCTION	DIL	BURN-IN (CONDITION C)
f_{IN}	1	V_{CC}
$\overline{Z_0}$	2	GND
$\overline{Z_1}$	3	GND
$\overline{Z_2}$	4	GND
$\overline{Z_3}$	5	GND
B2	6	V_{CC}
Enable Out	7	V_{CC}
GND	8	V_{CC}
$\overline{f_{OUT}}$	9	GND
B1	10	V_{CC}
$\overline{P0}$	11	V_{CC}
$\overline{P2}$	12	V_{CC}
$\overline{P3}$	13	V_{CC}
P1	14	V_{CC}
NC	15	OPEN
V_{CC}	16	V_{CC}

BURN - IN CONDITIONS:
V_{CC} = 6.0 V MAX/ 5.0 V MIN

LOGIC CIRCUIT



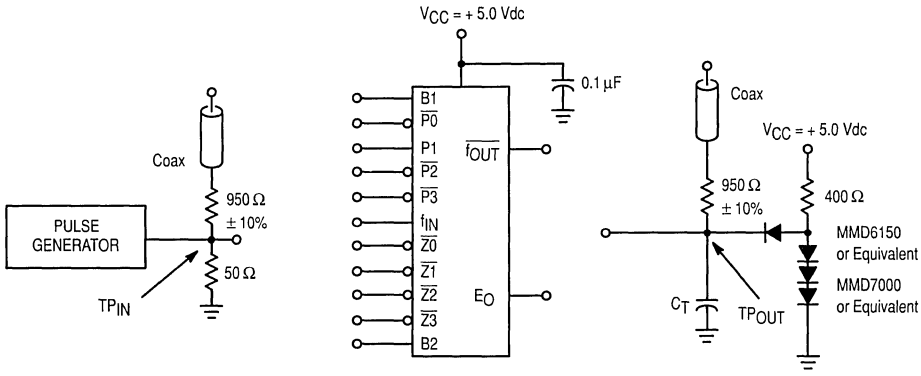


Figure 1. Switching Test Circuit

NOTES

1. Two pulse generators are required and must be slaved together to provide the waveforms shown.
2. C_T = 15.0 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.
3. The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.
4. A load is connected to each output during testing.

PRF = 1.0 MHz double pulsed for waveform A; 1.0 MHz for waveform B.

$t_r = t_f$ = 5.0 ns (10% to 90% points).

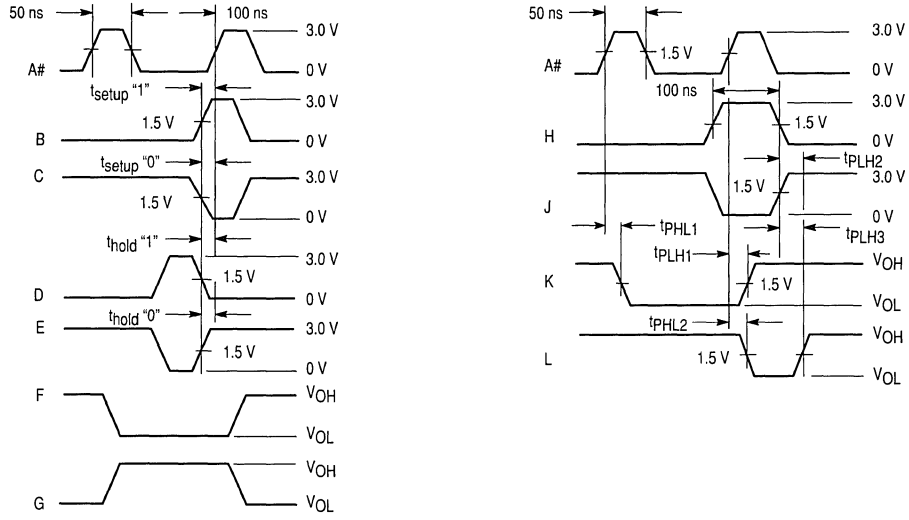


Figure 2. Setup and Hold Times

12514
QUIESCENT LIMIT TABLE *

*** ELECTRICAL CHARACTERISTICS:**

Test procedures are shown for the f_{IN}, $\overline{Z_O}$, B_1 and P_1 inputs. All other inputs are tested in the same manner as the $\overline{Z_O}$ input.

Test Temperature	Test Voltage Values (Volts)							Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{RH}	V_{IHH}	V_{CC}	V_{CCL}	V_{CCH}	I_{OL}	I_{OH}	I_{IC}
T_A = 25 °C	+2.4	+0.5	+4.5	+5.0	+5.0	+4.5	+5.5	+16	-0.4	-10
T_A = 125 °C	+2.4	+0.5	+4.5	+5.0	+5.0	+4.5	+5.5	+16	-0.4	-10
T_A = -55 °C	+2.4	+0.5	+4.5	+5.0	+5.0	+4.5	+5.5	+16	-0.4	-10

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C Subgroup 1		+ 125 °C Subgroup 2		- 55 °C Subgroup 3			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 Ω to + 5.0 V								
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{IL}	V_{RH}	V_{IHH}	$V_{CC/L/H}$	GND	$C_{P1/2}$	$I_{OH}/I_{OL}/I_{IC}$	P.U.T.
V_{OH}	High Voltage Output	2.4		2.4		2.4		V		2 - 5	6, 11 - 13		16 (V_{CCL})	8	1 (C_{P1})	7, 9 (I_{OH})	7, 9
V_{OL}	Low Voltage Output		0.5		0.5		0.5	V		11 - 13	2 - 5, 10, 14		16 (V_{CCL})	8	1 (C_{P2})	7, 9 (I_{OL})	7, 9
V_{IC}	Input Clamping Voltage		- 1.2		- 1.2		- 1.2	V					16 (V_{CCL})	8		1 - 6, 10 - 14 (I_{IC})	1 - 6, 10 - 14
** I_{INH1}	Input Current High		40		40		80	µA	2 - 6, 10 - 14				16 (V_{CCH})	1, 6, 8, 11 - 13			2 - 6, 10 - 14
I_{INH2}	Input Current High		160		160		420	µA					16 (V_{CCH})	8, 10			1
I_{INH3}	Input Current High		1.0		1.0		1.0	mA				1 - 6, 10 - 14	16 (V_{CCH})	1, 6, 8, 10 - 13			1 - 6, 10 - 14
** I_{INL1}	Input Current Low		- 1.6		- 1.6		- 1.6	mA		2 - 5, 10 - 14			16 (V_{CCH})	1, 6, 8, 10 - 13			2 - 6, 10 - 14
I_{INL}	Input Current Low		- 6.4		- 6.4		- 6.4	mA		1	6, 11 - 13		16 (V_{CCH})	8, 10			1
I_{os}	Short Circuit Current	- 20	- 65	- 20	- 65	- 20	- 65	µA		2 - 5			16 (V_{CC})	7, 8, 9	1 (C_{P2})		7, 9
*** I_{CC}	Power Supply Drain Current		35		35		35	mA					16 (V_{CC})	6, 8, 10			16

** Momentary Gnd to pin 7 prior to test.

*** Measure current after CP1 applied to pin 1.

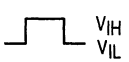
12514
QUIESCENT LIMIT TABLE

*** ELECTRICAL CHARACTERISTICS:**

Test procedures are shown for the f_{IN}, $\overline{Z_O}$, B_1 and P_1 inputs. All other inputs are tested in the same manner as the $\overline{Z_O}$ input.

Test Temperature	Test Voltage Values (Volts)							Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{RH}	V_{IHH}	V_{CC}	V_{CCL}	V_{CCH}	I_{OL}	I_{OH}	I_{IC}
T_A = 25 °C	+2.4	+0.5	+4.5	+5.0	+5.0	+4.5	+5.5	+16	-0.4	-10
T_A = 125 °C	+2.4	+0.5	+4.5	+5.0	+5.0	+4.5	+5.5	+16	-0.4	-10
T_A = -55 °C	+2.4	+0.5	+4.5	+5.0	+5.0	+4.5	+5.5	+16	-0.4	-10

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{OUT}	V_{IL}	V_{IN}	V_{IH}	V_{CC}	V_{EE}	P.U.T.
t_{PLH1}	Propagation Delay		15		19		16	ns	9	11 - 13	1, 10	14	16	8	9
t_{PHL1}	Propagation Delay		16		18		17	ns	9	11 - 13	1, 10	14	16	8	9
t_{PLH2}	Propagation Delay		12		17		12	ns	7	2 - 5, 11 - 13	1 - 6	10, 14	16	8	7
t_{PHL2}	Propagation Delay		16		19		17	ns	7	2 - 5, 11 - 13	1 - 6	10, 14	16	8	7
t_{PLH3}	Propagation Delay		16		20		17	ns	7	2 - 5, 11 - 13	1, 6	10, 14	16	8	7
t_{Set1}	Setup Time (Pins 10, 14)		2.0					ns	9	11 - 13	1, 10 - 14	10, 14	16	8	10 - 14
t_{Set1}	Setup Time (Pins 11 - 13)		12					ns	9	11 - 13	1, 10 - 14	10, 14	16	8	10 - 14
t_{Set0}	Setup Time (Pins 10, 14)		8.0					ns	9	11 - 13	1, 10 - 14	10, 14	16	8	10 - 14
t_{Set0}	Setup Time (Pins 11 - 13)		9.0					ns	9	11 - 13	1, 10 - 14	10, 14	16	8	10 - 14

CP1 

CP2 

12514
QUIESCENT LIMIT TABLE

*** ELECTRICAL CHARACTERISTICS:**

Test procedures are shown for the f_{IN}, $\overline{Z_O}$, B_1 and P_1 inputs. All other inputs are tested in the same manner as the $\overline{Z_O}$ input.

Test Temperature	Test Voltage Values (Volts)							Test Current Values (mA)		
	V_{IH}	V_{IL}	V_{RH}	V_{IHH}	V_{CC}	V_{CCL}	V_{CCH}	I_{OL}	I_{OH}	I_{IC}
T_A = 25 °C	+2.4	+0.5	+4.5	+5.0	+5.0	+4.5	+5.5	+16	-0.4	-10
T_A = 125 °C	+2.4	+0.5	+4.5	+5.0	+5.0	+4.5	+5.5	+16	-0.4	-10
T_A = -55 °C	+2.4	+0.5	+4.5	+5.0	+5.0	+4.5	+5.5	+16	-0.4	-10

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{OUT}	V_{IL}	V_{IN}	V_{IH}	V_{CC}	V_{EE}	P.U.T.
t_{Hold1}	Hold Time (Pins 10, 14)		8.0					ns	9	11 - 13	1, 10 - 14	10, 14	16	8	10 - 14
t_{Hold1}	Hold Time (Pins 11 - 13)		10					ns	9	11 - 13	1, 10 - 14	10, 14	16	8	10 - 14
t_{Hold0}	Hold Time (Pins 10, 14)		2.0					ns	9	11 - 13	1, 10 - 14	10, 14	16	8	10 - 14
t_{Hold0}	Hold Time (Pins 11 - 13)		14					ns	9	11 - 13	1, 10 - 14	10, 14	16	8	10 - 14

Low-Power Two Modulus Prescaler

Military 12515

ELECTRICALLY TESTED PER:
MPG 12515

The 12515 is a two-modulus prescaler which will divide by 32 and 33. An internal regulator is provided to allow this device to be used over a wide range of power-supply voltages. This device may be operated by applying a supply voltage of 5.0 Vdc ± 10% at pin 7 or by applying an unregulated voltage from 5.5 Vdc to 9.5 Vdc to pin 8.

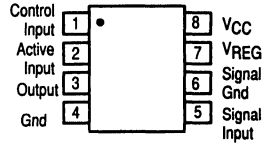
- 225 MHz Toggle Frequency
- Low-Power — 7.5 mA Max at 6.8 V
- Control Input and Output are Compatible with Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5 V to 9.5 V

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 12515/BXAJC

X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: P



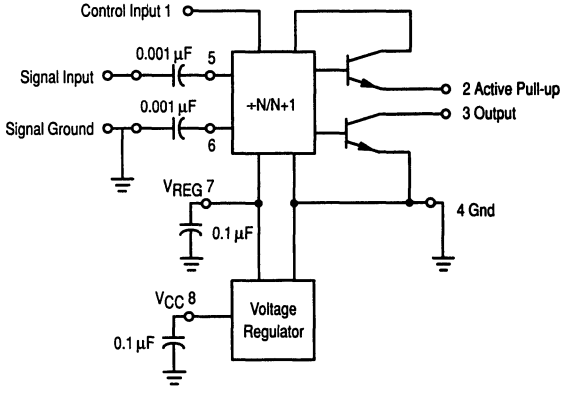
ABSOLUTE MAXIMUM RATINGS	Symbol	Min.	Max.	Units
Regulated Voltage, Pin 7	V_{REG}		+8.0	V_{dc}
Power Supply Voltage, Pin 8	V_{CC}		+10	V_{dc}
Input Voltage	V_{IN}		+2.0	V_{dc}
Operating Temperature Range	T_A	-55	+125	°C
Storage Temperature Range	T_{stg}	-65	+175	°C

PIN ASSIGNMENTS

FUNCTION	DIL	BURN-IN (CONDITION C)
Control Input	1	V_{CC}
Active Pullup	2	3.01 kΩ to V_{CC}
Output	3	3.01 kΩ to V_{CC}
Gnd	4	GND
Signal Input	5	6.19 kΩ to V_{CC}
Signal Gnd	6	OPEN
V_{REG}	7	OPEN
V_{CC}	8	V_{CC}

BURN - IN CONDITIONS:
V_{CC} = 6.5 V MAX/ 5.5 V MIN

LOGIC DIAGRAM



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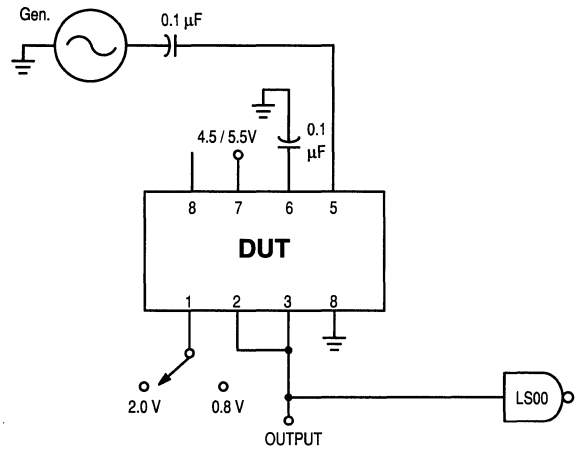


Figure 1. Minimum/Maximum Amp., Maximum/Minimum Frequency

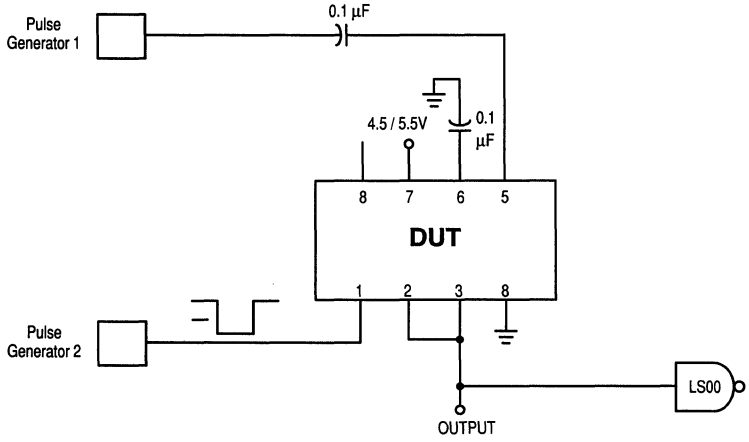


Figure 2. Setup and Hold Control Modulus, Clock to Output Delay (Information Only)

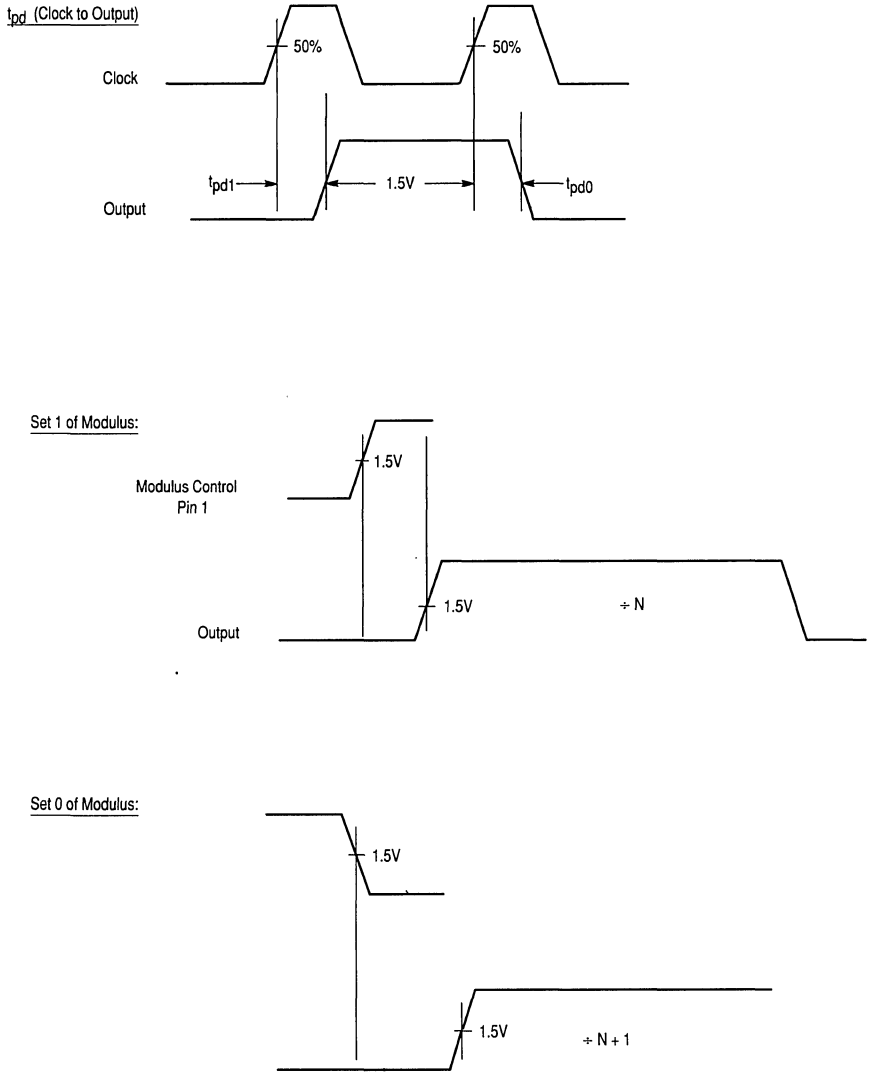
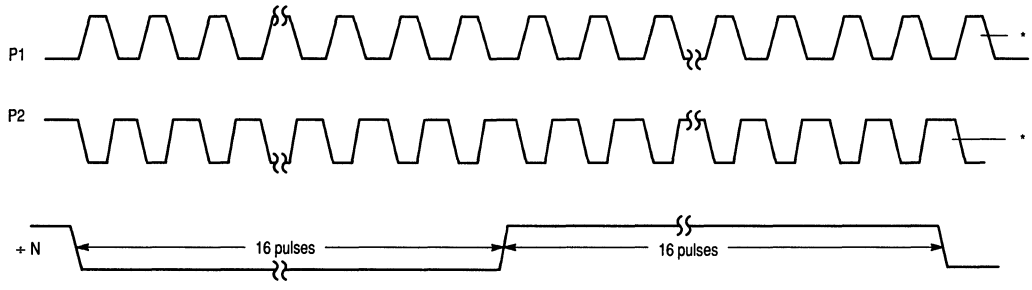
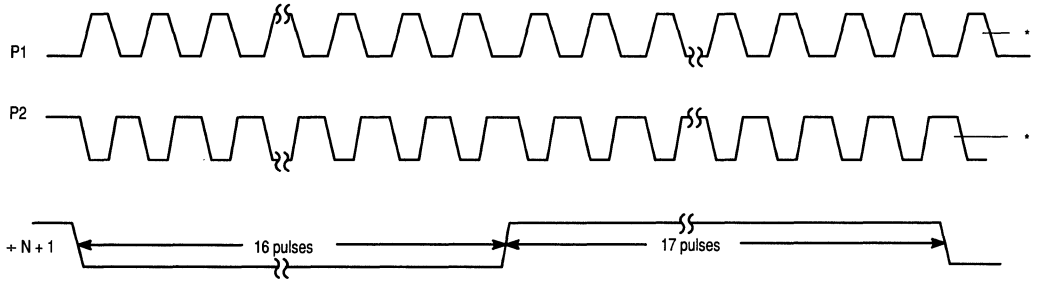


Figure 3. Test Circuit Waveforms (Information Only)

6



P1 = 400 mV above and below * point (for static testing only). Rise and Fall times of test waveforms must be less than 20 ns.
* Device internal bias point.



P1 = 400 mV above and below * point (for static testing only). Rise and Fall times of test waveforms must be less than 20 ns.
* Device internal bias point.

6

Figure 4. Test Waveforms

12515
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)									Test Current Values		Divide by Function	
	V_{IH}	V_{IL}	V_{IR}	V_{LL}	$V_{CH/CM1}$	$V_{IM/CM2}$	V_{CL}	V_{CC}	GND	I_{OL}	I_{CH}	÷N	÷N + 1
T_A = 25 °C	+2.0	+0.8	+2.7	+0.4	+5.5	+9.5	+4.5	+5.0	0	+2.0 mA	-100 µA	+32	+33
T_A = 125 °C	+2.0	+0.8	+2.7	+0.4	+5.5	+9.5	+4.5	+5.0	0	+2.0 mA	-100 µA	+32	+33
T_A = -55 °C	+2.0	+0.8	+2.7	+0.4	+5.5	+9.5	+4.5	+5.0	0	+2.0 mA	-100 µA	+32	+33

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments P1 per figure 4, Output Load = 0.1 µF to Gnd								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_{IH}	V_{CH}	$V_{IM/CM2}$	V_{CL}	C1	P1	I_{OH}/I_{OL}	GND	P.U.T.
** V_{OH}	High Voltage Output	2.5		2.5		2.5		V	1			7	6	5	2, 3 (I_{OH})	4	2, 3
* V_{OL}	Low Voltage Output		0.5		0.5		0.5	V	1			7	6	5	2, 3 (I_{OL})	4	2, 3
** I_{SC}	Short Circuit Current	-5.0	-16.5	-5.0	-16.5	-5.0	-16.5	mA	1	7			6	5		2, 3, 4	2, 3
* I_{IM}	Input Current High		0.1		0.1		0.1	mA			1	7, 8	6	5		4	1
* I_{CH}	Power Supply Current		7.2		7.2		7.2	mA	1	7			6	5		4	7
* I_{CM}	Power Supply Current		7.8		7.8		7.8	mA	1		8 (V_{CM2})		6	5		4	8

* Precondition Low, Pins 2 and 3 wired together.

** Precondition High, Pins 2 and 3 wired together.

12515
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)									Test Current Values		Divide by Function	
	V_{IH}	V_{IL}	V_{IR}	V_{LL}	$V_{CH/CM1}$	$V_{IM/CM2}$	V_{CL}	V_{CC}	GND	I_{OL}	I_{CH}	÷N	÷N + 1
T_A = 25 °C	+2.0	+0.8	+2.7	+0.4	+5.5	+9.5	+4.5	+5.0	0	+2.0 mA	-100 µA	+32	+33
T_A = 125 °C	+2.0	+0.8	+2.7	+0.4	+5.5	+9.5	+4.5	+5.0	0	+2.0 mA	-100 µA	+32	+33
T_A = -55 °C	+2.0	+0.8	+2.7	+0.4	+5.5	+9.5	+4.5	+5.0	0	+2.0 mA	-100 µA	+32	+33

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments P1 per figure 4, Output Load = 0.1 µF to Gnd								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		V_R	V_{R2}	V_{CH}	V_{IR}	V_{ILL}	C1	P1	GND	P.U.T.
V_R	High Voltage Output	3.5	4.5	3.5	4.5	4.0	5.0	V	7		8 (V_{CH1})						7
V_{R2}	Low Voltage Output	4.0	4.5	3.3	4.5	4.0	5.0	V		7	8 (V_{CH2})						7
* I_{IR}	Short Circuit Current	-5.0	-16.5	-5.0	-16.5	-5.0	-16.5	mA			7, 8	1		6	5	4	1
* I_{IL}	Input Current High		0.1		0.1		0.1	mA			7, 8		1	6	5	4	1

* Precondition Low, Pins 2 and 3 wired together.

12515
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)									Test Current Values		Divide by Function	
	V_{IH}	V_{IL}	V_{IR}	V_{LL}	$V_{CH/CM1}$	$V_{IM/CM2}$	V_{CL}	V_{CC}	GND	I_{OL}	I_{CH}	÷N	÷N + 1
T_A = 25 °C	+2.0	+0.8	+2.7	+0.4	+5.5	+9.5	+4.5	+5.0	0	+2.0 mA	-100 µA	+32	+33
T_A = 125 °C	+2.0	+0.8	+2.7	+0.4	+5.5	+9.5	+4.5	+5.0	0	+2.0 mA	-100 µA	+32	+33
T_A = -55 °C	+2.0	+0.8	+2.7	+0.4	+5.5	+9.5	+4.5	+5.0	0	+2.0 mA	-100 µA	+32	+33

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW				
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max		V_{OUT}	V_{IN}	V_{CC}	V_{EEL}	P.U.T.
t_{pd}	Propagation Delay (Note 1)		50		50		50	ns	(See Figure 1 - 4)				
* **Clk1** (min)	Clock Input 1 (Note 2)	400	800	400	800	400	800	mVp-p	(See Figure 1 - 4)				
* **Clk2** (min)	Clock Input 2 (Note 2)	200	800	200	800	200	800	mVp-p	(See Figure 1 - 4)				
* **Clk** (max)	Clock Maximum (Note 2)	200	800	200	800	200	800	mVp-p	(See Figure 1 - 4)				
t_{SET0}	Setup Time (Note 1)		6.0		6.0		6.0	ns	(See Figure 1 - 4)				
t_{SET1}	Setup Time (Note 1)		6.0		6.0		6.0	ns	(See Figure 1 - 4)				
f_{max}	Toggle Frequency (Note 3)	225		225		225		MHz	(See Figure 1 - 4)				
f_{min}	Toggle Frequency		35		35		35	MHz	(See Figure 1 - 4)				

1. These parameters guaranteed by those marked with a single asterisk *, therefore are not tested.
2. Measure Clock 1 (min) at 35 MHz, Clock 2 (min) at 50 MHz, and Clock (max) at f_{MAX}.
3. 275 MHz for 12515A.

Military 12540

Phase-Frequency Detector

ELECTRICALLY TESTED PER:
5962-8775201

The 12540 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the 1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of the Phase Detector #1 of the 4044.

- Operating Frequency = 80 MHz typical

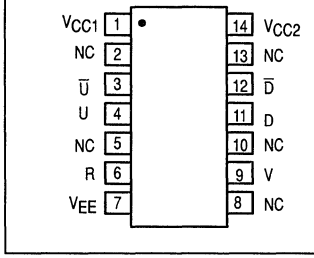
ABSOLUTE MAXIMUM RATINGS	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		+7.0	V_{dc}
Output Voltage	V_{OUT}		+5.5	V_{dc}
Input Voltage	V_{IN}		+5.5	V_{dc}
Operating Temperature Range	T_A	-55	+125	°C
Storage Temperature Range	T_{stg}	-65	+175	°C

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8775207
3) 883: 12540/BXAJC

X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: C

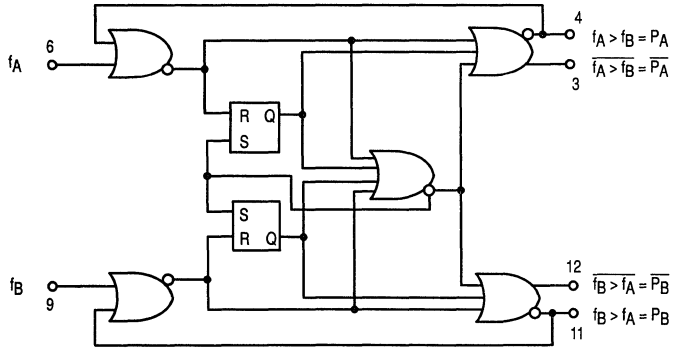


PIN ASSIGNMENTS

FUNCTION	DIL	BURN-IN (CONDITION C)
V_{CC1}	1	GND
NC	2	OPEN
$\overline{U}$	3	51Ω to V_{TT}
U	4	51Ω to V_{TT}
NC	5	OPEN
R	6	2 kΩ to V_{TT}
V_{EE}	7	V_{CC}
NC	8	OPEN
V	9	2 kΩ to V_{TT}
NC	10	OPEN
D	11	51Ω to V_{TT}
$\overline{D}$	12	51Ω to V_{TT}
NC	13	OPEN
V_{CC2}	14	GND

BURN - IN CONDITIONS:
V_{CC} = 6.0 V MAX/ 5.0 V MIN

LOGIC DIAGRAM



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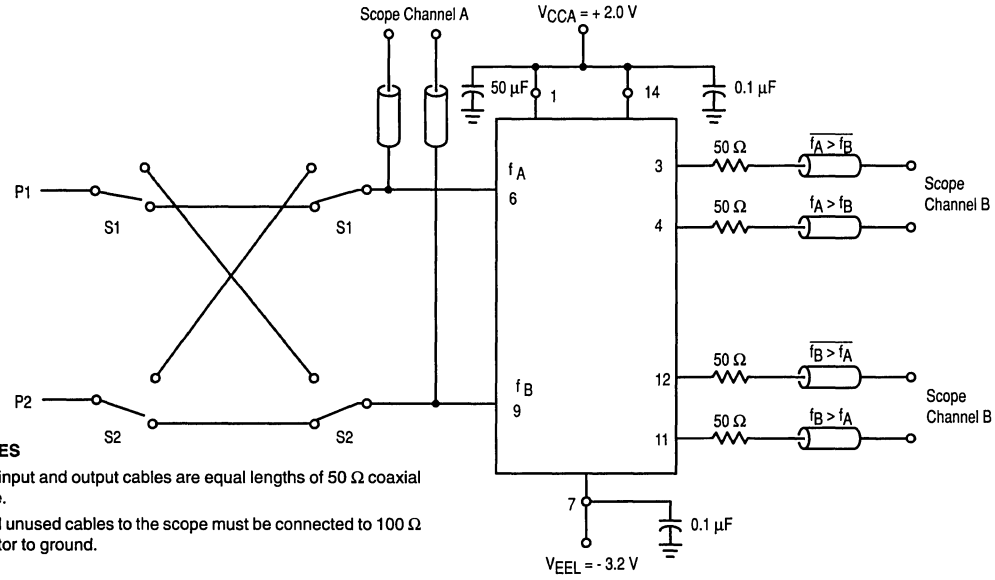


NOTES

1 All input and output cables are equal lengths of 50 Ω coaxial cable.

2. All unused cables to the scope must be connected to 100 Ω resistor to ground.

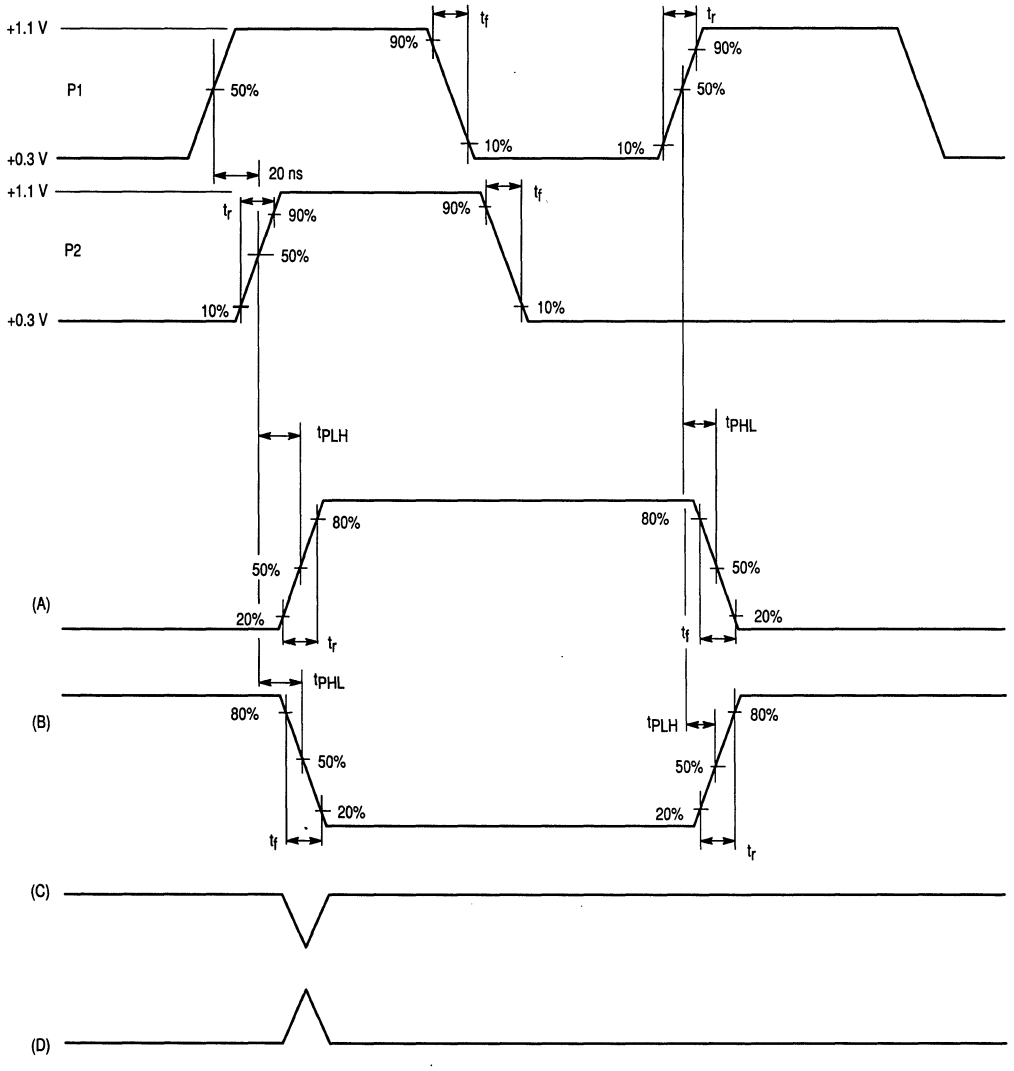
Figure 1. Switching Test Circuit

Functional Truth Table

INPUT		OUTPUT			
f_A	f_B	$f_A > f_B$	$f_B > f_A$	$\overline{f_A > f_B}$	$\overline{f_B > f_A}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1

X = DON'T CARE

6



NOTES

1. P1, P2:
   a) PRF = 5.0 MHz.
   b) Duty Cycle 50%.
   c) $t_r = t_f = 1.5$ ns ± 0.2 ns (10% to 90%)

Figure 2. Test Circuit Waveforms

12540
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EE}
T_A = 25 °C	+ 4.22	+3.21	+3.895	+3.525	+5.0	0
T_A = 125 °C	+ 4.37	+3.24	+4.000	+3.600	+5.0	0
T_A = -55 °C	+4.12	+3.14	+3.745	+3.490	+5.0	0

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 kΩ to + 3.0 V					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		V_{IH}	R - 1	V_{EE}	*	V_{CC}	P.U.T.
V_{OH}	High Voltage Output	4.07	4.22	4.175	4.37	3.92	4.12	V		3, 4, 11, 12	7	6, 9	1, 14	3, 4, 11, 12
V_{OL}	Low Voltage Output	3.21	3.44	3.24	3.515	3.14	3.405	V		3, 4, 11, 12	7	7, 9	1, 14	3, 4, 11, 12
V_{OHA}	Threshold Voltage High	4.05	4.22	4.155	4.37	3.90	4.12	V		3, 4, 11, 12	7	7, 9	1, 14	3, 4, 11, 12
V_{OLA}	Threshold Voltage Low	3.21	3.46	3.24	3.535	3.14	3.425	V		3, 4, 11, 12	7	7, 9	1, 14	3, 4, 11, 12
I_{INH}	Input Current High		350					μA	6, 9		7		1, 14	6, 9
I_E	Total Power Supply Current	-115	-60					μA			7		1, 14	7

NOTE: (This device will meet standard MECL logic levels using V_{EE} = - 5.2 Vdc and V_{CC} = 0V).
1. The outputs of the device must be tested by sequencing through the truth table for V_{OH}, V_{OL} tests.
2. The outputs of the device must be tested by sequencing through the truth table for V_{OHA}, V_{OLA} tests.
All input, power supply, and ground voltages must be maintained between tests.
3. Preconditioning for AC tests is accomplished by applying P1 for a minimum of two pulses prior to P2.
* = Per truth table.

12540
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)					
	V_{IH}	V_{IL}	V_{IHA}	V_{ILA}	V_{CC}	V_{EEL}
T_A = 25 °C	+ 4.22	+ 3.21	+ 3.895	+ 3.525	+ 2.0	-3.0 or -3.2
T_A = 125 °C	+ 4.37	+ 3.24	+ 4.000	+ 3.600	+ 2.0	-3.0 or -3.2
T_A = -55 °C	+ 4.12	+ 3.14	+ 3.745	+ 3.490	+ 2.0	-3.0 or -3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 100 kΩ to 0.0 V					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		V_{OUT}	V_{CCA}	P_1	P_2	V_{EEL}	P.U.T.
t_r	Rise Time		3.4		3.8		3.4	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_f	Fall Time		3.4		3.8		3.4	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t6+4+)	0	4.6	0	5.0	0	4.6	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t6+12+)	0	6.0	0	6.6	0	6.0	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t6+3-)	0	4.5	0	4.9	0	4.5	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t6+11-)	0	6.4	0	7.0	0	6.4	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t9+11+)	0	4.6	0	5.0	0	4.6	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t9+3+)	0	6.0	0	6.6	0	6.0	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t9+12-)	0	4.5	0	4.9	0	4.5	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12
t_{pd}	Propagation Delay (t9+4+)	0	6.4	0	7.0	0	6.4	ns	3, 4, 11, 12	1, 14	8, 9	8, 9	7	3, 4, 11, 12

MOTOROLA

Military 12561

Crystal Oscillator

ELECTRICALLY TESTED PER:
MPG 12561

The 12561 is for use with an external crystal to form a crystal controlled oscillator. In addition to the fundamental series mode crystal, two bypass capacitors are required (plus usual power supply pin bypass capacitors). Translators are provided internally for MECL and TTL outputs.

- Frequency Range = 2.0 MHz to 20 MHz
- Single Supply Operation: + 5.0 Vdc or - 5.2 Vdc
- Three Outputs Available:
  1. Complementary Sine Wave (600 mVp-p)
  2. Complementary MECL
  3. Single Ended TTL

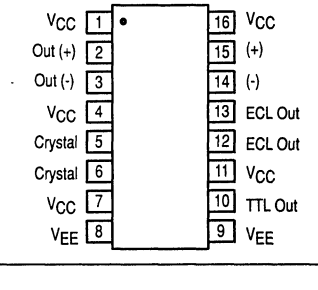
ABSOLUTE MAXIMUM RATINGS	Symbol	Min.	Max.	Units
Supply Voltage	V_{CC}		+7.0	V_{dc}
Output Voltage	V_{OUT}		+5.5	V_{dc}
Input Voltage	V_{IN}		+5.5	V_{dc}
Operating Temperature Range	T_A	-55	+125	°C
Storage Temperature Range	T_{stg}	-65	+150	°C

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: 12561/BXAJC

X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E

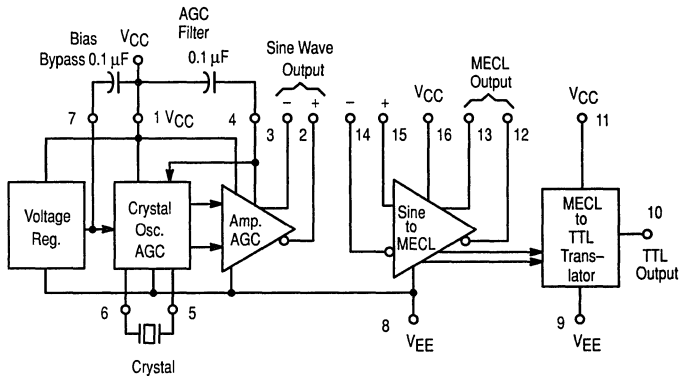


PIN ASSIGNMENTS

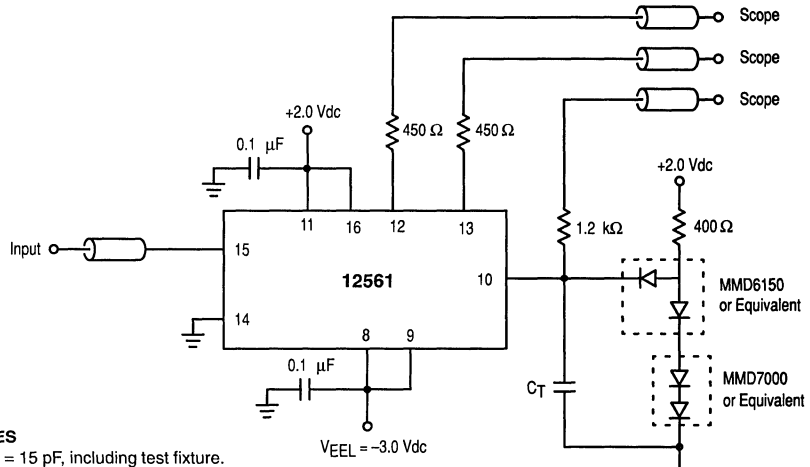
FUNCTION	DIL	BURN-IN (CONDITION C)
V_{CC}	1	V_{CC}
Sine Wave Out -	2	OPEN
Sine Wave Out +	3	OPEN
V_{CC}	4	OPEN
Crystal	5	OPEN
Crystal	6	OPEN
V_{CC}	7	OPEN
V_{EE}	8	GND
V_{EE}	9	GND
TTL Out	10	V_{CC}
V_{CC}	11	V_{CC}
ECL Out	12	OPEN
ECL Out	13	OPEN
(-)	14	OPEN
(+)	15	V_{CC}
V_{CC}	16	V_{CC}

BURN - IN CONDITIONS:
V_{CC} = 6.0 V MAX/ 5.0 V MIN

LOGIC DIAGRAM



6



NOTES
1. C_T = 15 pF, including test fixture.
2. All input and output cables are equal lengths of 50 Ω coaxial cable.
3. All unused cables to the scope must be terminated with a 50 Ω ± 1.0% resistor.
4. $t_r = t_f$ = 2.0 ns ± 0.2 ns.
5. f = 2.0 MHz.
6. EH model 137 pulse generator or equivalent.

Figure 1. AC Test Circuit

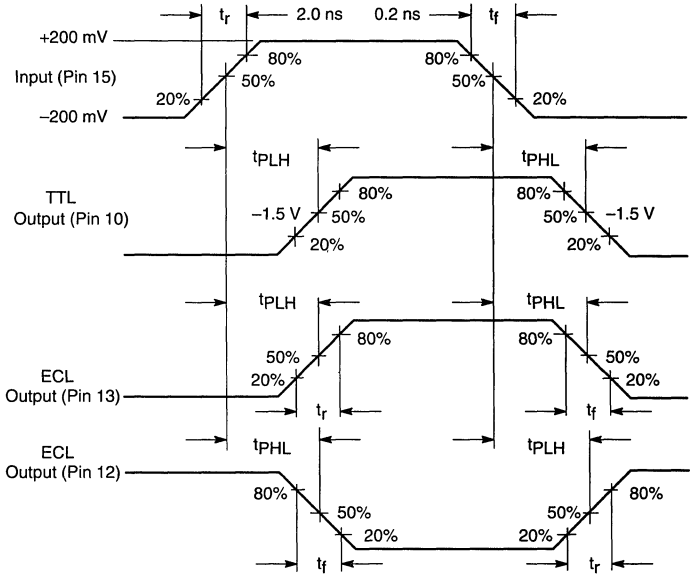


Figure 2. AC Test Circuit Waveforms

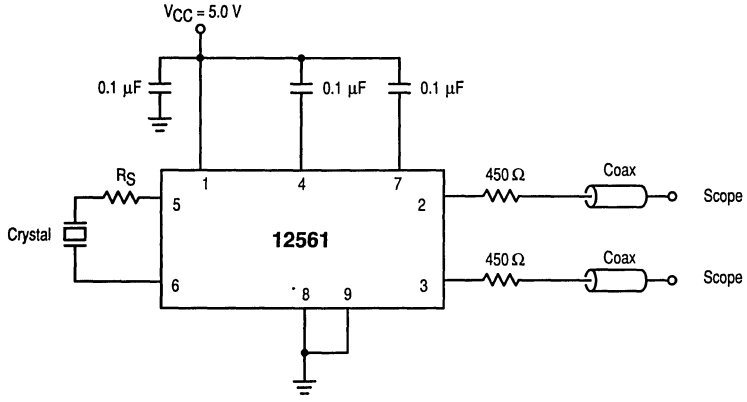


Figure 3. Test Circuit #2

NOTES

1. Crystal: Reeves Hoffman series mode, A element f = 10.0 MHz; R_E = 5 Ω,
Series R minimum at Fundamental
2. R_S = 150 kΩ
3. The purpose of the series resistor, R_S, in the test circuit is to guarantee oscillation using crystals having an R_E as large as 155 Ω.
4. All output cables to the scope are equal lengths of 50 Ω coaxial cables. All unused cables must be terminated with a 50 Ω ± 1.0% resistor. A 50 Ω termination to ground is located in each channel input. The 450 Ω series resistor in conjunction with the 50 Ω termination constitutes a 10:1 attenuator.

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12561
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)											Test Current Values (mA)		
	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{CC}	V_{CCL}	V_{CCH}	V_{CCA}	V_{EEL}	V_{EE}	V_{TH}	I_{OL}	I_{OH}	I_L
T_A = 25 °C	+3.90	+3.52	+4.19	+3.21	+5.0	+4.5	+5.5	+2.0	-3.0	0	+4.0	+16	-0.4	-2.5
T_A = 125 °C	+4.03	+3.60	+4.37	+3.25	+5.0	+4.5	+5.5	+2.0	-3.0	0	+4.0	+16	-0.4	-2.5
T_A = -55 °C	+3.78	+3.49	+4.07	+3.18	+5.0	+4.5	+5.5	+2.0	-3.0	0	+4.0	+16	-0.4	-2.5

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW								
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 0.1 µF from Pins 4, 7 to V_{CC}								
		Subgroup 1		Subgroup 2		Subgroup 3											
		Min	Max	Min	Max	Min	Max		$V_{IHA/B}$	$V_{ILA/B}$	V_{TH}	V_{CC}	V_{CCH}	V_{EE}	V_{CCL}	$I_{OH/OL/L}$	P.U.T.
V_{OH1}	High Voltage Output	4.03	4.22	3.16	4.37	3.91	4.17	V	14, 15	14, 15		16		8		12, 13 (I_L)	12, 13
V_{OH2}	High Voltage Output	2.4	4.22	2.39	4.0	2.39	4.0	V	15	14				8, 9	11, 16	10 (I_{OH})	10
V_{OL1}	Low Voltage Output	3.0	3.44	3.04	3.5	2.97	3.39	V	14, 15	14, 15		16		8		12, 13 (I_L)	12, 13
V_{OL2}	Low Voltage Output	0.0	0.5	0.0	0.5	0.0	0.5	V	14, 15	14, 15			11, 16	8, 9	11, 16	10 (I_{OL})	10
V_{OHA}	Threshold Voltage High	4.01	4.22	4.14	4.37	3.89	4.17	V	14, 15	14, 15		16		8		12, 13 (I_L)	12, 13
V_{OLA}	Threshold Voltage Low	3.0	3.46	3.04	3.52	2.97	3.41	V	14, 15	14, 15		16		8		12, 13 (I_L)	12, 13
ΔV	Differential Offset Voltage (4 - 7)	40	325					mV			5, 6	1		8			4 - 7
ΔV	Differential Offset Voltage (2 - 3)	-150	150					mV			4	1, 11, 16		8, 9			2 - 3
I_{INH}	Input Current High		250					µA	14, 15	14, 15		16		8			14, 15
I_{INL}	Input Current Low		-1.0					µA	14, 15			16		8, 14, 15			14, 15

NOTE: This device will meet standard MECL logic levels using V_{EE} = - 5.2 Vdc and V_{CC} = 0 V.

12561
QUIESCENT LIMIT TABLE

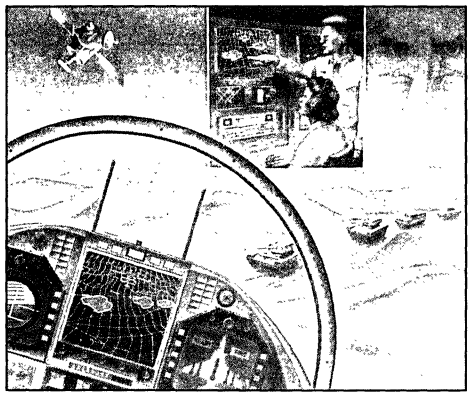
Test Temperature	Test Voltage Values (Volts)											Test Current Values (mA)		
	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{CC}	V_{CCL}	V_{CCH}	V_{CCA}	V_{EEL}	V_{EE}	V_{TH}	I_{OL}	I_{OH}	I_L
T_A = 25 °C	+3.90	+3.52	+4.19	+3.21	+5.0	+4.5	+5.5	+2.0	-3.0	0	+4.0	+16	-0.4	-2.5
T_A = 125 °C	+4.03	+3.60	+4.37	+3.25	+5.0	+4.5	+5.5	+2.0	-3.0	0	+4.0	+16	-0.4	-2.5
T_A = -55 °C	+3.78	+3.49	+4.07	+3.18	+5.0	+4.5	+5.5	+2.0	-3.0	0	+4.0	+16	-0.4	-2.5

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 0.1 µF from Pins 4, 7 to V_{CC}					
		Subgroup 1		Subgroup 2		Subgroup 3								
		Min	Max	Min	Max	Min	Max		$V_{IHA/B}$	$V_{ILA/B}$	V_{CC}	V_{EE}	V_{CCL}	P.U.T.
I_{OS}	Short Circuit Current	-20	-60	-20	-60	-20	-60	mA	15	14		8, 9, 10	11, 16	10
I_{CC1}	Power Supply Drain Current	18.0	28.0					mA			1	8		1
I_{CC2}	Power Supply Drain Current		4.0					mA	14	15		8, 9	11, 16	11
I_{CC3}	Power Supply Drain Current	13.0	19.0					mA			16	8		16

12561
QUIESCENT LIMIT TABLE

Test Temperature	Test Voltage Values (Volts)											Test Current Values (mA)		
	V_{IHA}	V_{ILA}	V_{IHB}	V_{ILB}	V_{CC}	V_{CCL}	V_{CCH}	V_{CCA}	V_{EEL}	V_{EE}	V_{TH}	I_{OL}	I_{OH}	I_L
T_A = 25 °C	+3.90	+3.52	+4.19	+3.21	+5.0	+4.5	+5.5	+2.0	-3.0	0	+4.0	+16	-0.4	-2.5
T_A = 125 °C	+4.03	+3.60	+4.37	+3.25	+5.0	+4.5	+5.5	+2.0	-3.0	0	+4.0	+16	-0.4	-2.5
T_A = -55 °C	+3.78	+3.49	+4.07	+3.18	+5.0	+4.5	+5.5	+2.0	-3.0	0	+4.0	+16	-0.4	-2.5

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments Output Load = 0.1 μF from Pins 4, 7 to V_{CC}						
		Subgroup 9		Subgroup 10		Subgroup 11									
		Min	Max	Min	Max	Min	Max		V_{OUT}	V_{CCA}	V_{IN}	XTAL	V_{EEL}	GND	P.U.T.
t_r	Rise Time	1.1	4.0	1.1	4.5	1.1	3.8	ns	12, 13	11, 16	15		9, 10	14	12, 13
t_f	Fall Time	1.1	4.0	1.1	5.0	1.1	3.8	ns	12, 13	11, 16	15		9, 10	14	12, 13
t_{pd}	Propagation Delay (t15+10+)	1.1	25	1.1	30	1.1	30	ns	10	11, 16	15		9, 10	14	10
t_{pd}	Propagation Delay (t15-10-)	1.1	18	1.1	22	1.1	22	ns	10	11, 16	15		9, 10	14	10
t_{pd}	Propagation Delay (t15+12-)	1.1	5.5	1.1	6.0	1.1	5.0	ns	12	11, 16	15		9, 10	14	2
t_{pd}	Propagation Delay (t15+12+)	1.1	5.2	1.1	5.5	1.1	4.8	ns	12	11, 16	15		9, 10	14	12
t_{pd}	Propagation Delay (t15+13+)	1.1	5.0	1.1	5.4	1.1	4.6	ns	13	11, 16	15		9, 10	14	12
t_{pd}	Propagation Delay (t15-13-)	1.1	5.0	1.1	5.2	1.1	5.0	ns	13	11, 16	15		9, 10	14	13
V_{S2}	Sine Wave Amplitude	700						mV	2	1		5, 6	8, 9		2
V_{S3}	Sine Wave Amplitude	700						mV	3	1		5, 6	8, 9		3

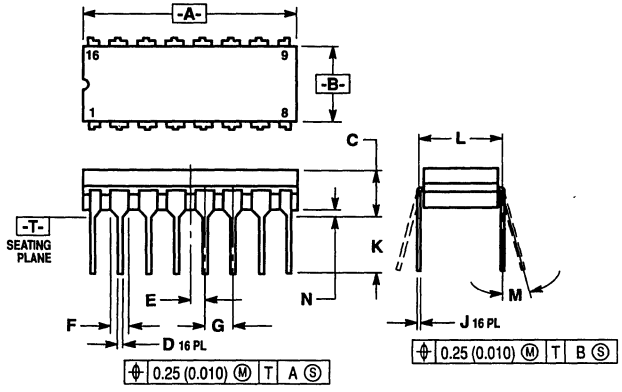


Package Outlines and Mechanical Data

7

Package Outlines and Mechanical Data

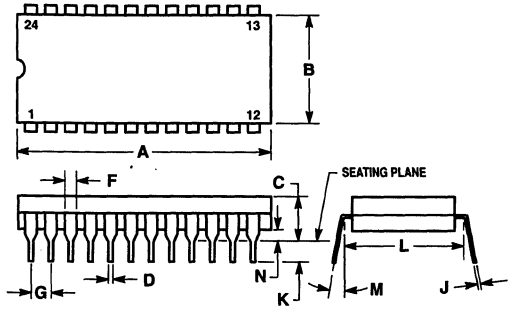
Dual-In-Line (DIL) Packages



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.93	0.750	0.785
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.39	0.50	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

CASE 620-10



NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

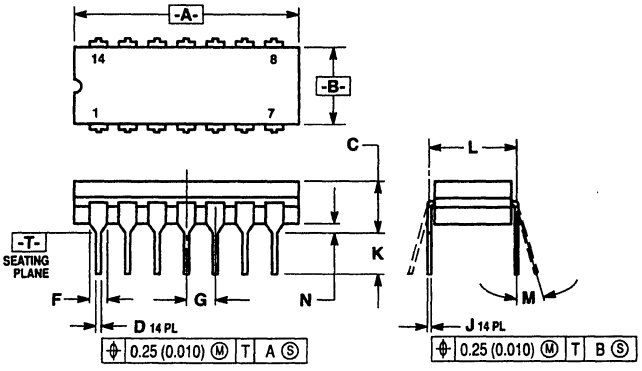
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

CASE 623-05

7

Package Outlines and Mechanical Data

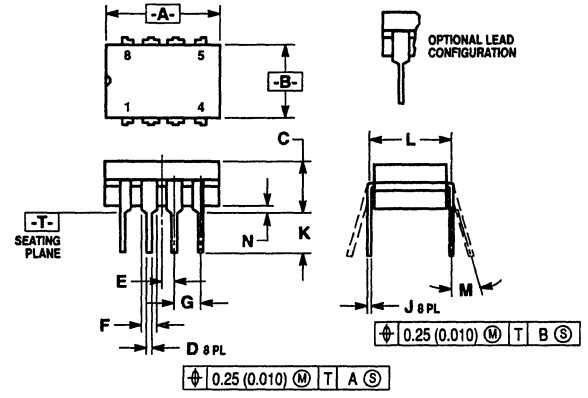
Dual-In-Line (DIL) Packages



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

CASE 632-08



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS AT LEAD POSITIONS 1, 4, 5, AND 8.
5. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

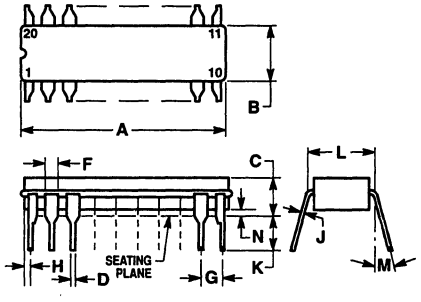
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.98	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
E	1.27 BSC		0.050 BSC	
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 693-03

7

Package Outlines and Mechanical Data

Dual-In-Line (DIL) Packages



NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

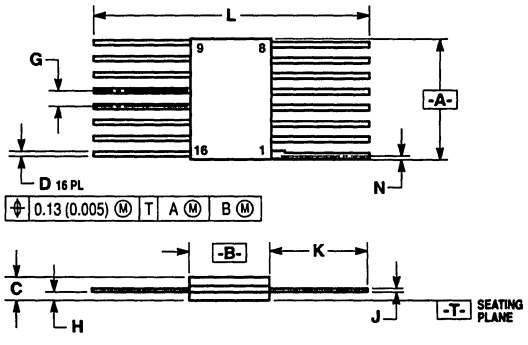
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

CASE 732-03

7

Package Outlines and Mechanical Data

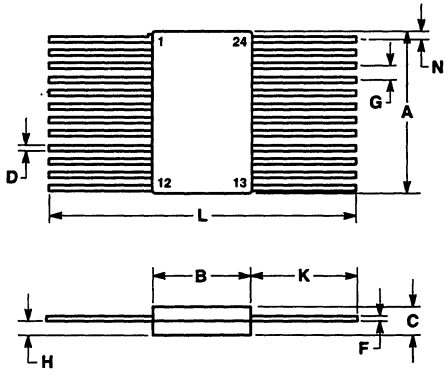
Flat Pack (FP)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "A" AND "B" ALLOW FOR LID MISALIGNMENT, AND GLASS MINISCUS.
4. DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
5. LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
6. DIMENSION "J" INCLUDES SOLDER LEAD FINISH.
7. LEAD NUMBERS SHOWN FOR REFERENCE ONLY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	9.90	0.370	0.390
B	6.23	6.60	0.245	0.260
C	1.53	2.15	0.060	0.085
D	0.36	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	0.01	0.025	0.040
J	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	0.50	—	0.020

CASE 650-05



NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

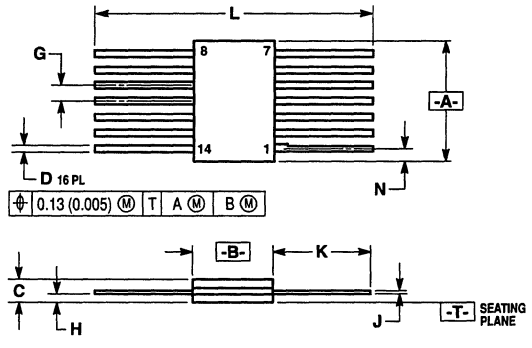
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	—	0.865	—
N	0.25	0.63	0.010	0.025

CASE 652-02

7

Package Outlines and Mechanical Data

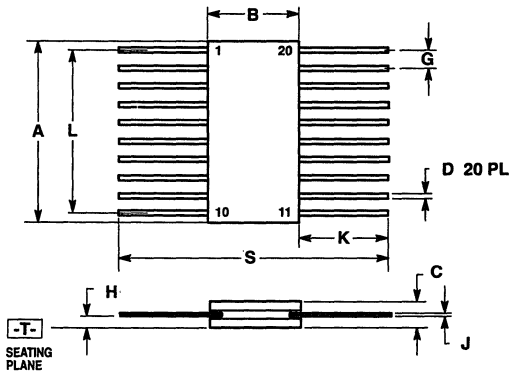
Flat Pack (FP)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "A" AND "B" ALLOW FOR LID MISALIGNMENT, AND GLASS MINISCUS.
4. DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
5. LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
6. DIMENSION "J" INCLUDES SOLDER LEAD FINISH.
7. LEAD NUMBERS SHOWN FOR REFERENCE ONLY.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	9.90	0.370	0.390
B	6.23	6.60	0.245	0.260
C	1.53	2.15	0.060	0.085
D	0.36	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	1.01	0.025	0.040
J	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	1.14	—	0.045

CASE 717-04



0.13 (0.005) M T A M

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "A" AND "B" ALLOW FOR LID MISALIGNMENT, AND GLASS MINISCUS.
4. DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
5. LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
6. DIMENSION "J" INCLUDES SOLDER LEAD FINISH.
7. LEAD NUMBERS SHOWN FOR REFERENCE ONLY.

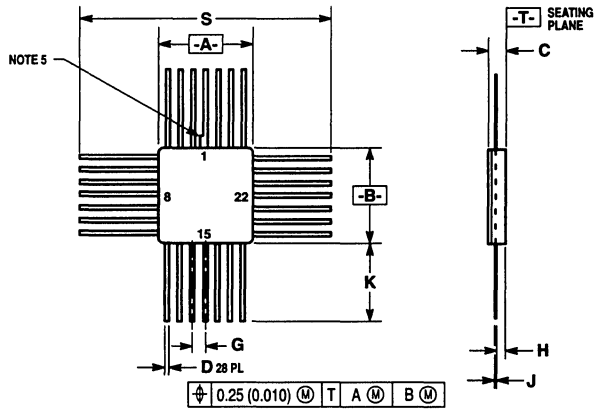
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.32	13.08	0.485	0.515
B	5.84	7.11	0.230	0.280
C	1.52	2.16	0.060	0.085
D	0.38	0.48	0.015	0.019
G	1.27 BSC		0.050 BSC	
H	0.64	1.02	0.025	0.040
J	0.10	0.18	0.004	0.007
K	6.35	9.39	0.250	0.370
L	11.43 BSC		0.450 BSC	
S	18.54	—	0.730	—

CASE 737-03

7

Package Outlines and Mechanical Data

Flat Pack (FP)



NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A AND B ALLOW FOR LID MISALIGNMENT, AND GLASS MINISCUS.
4. DIMENSION H SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
5. LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD.
6. DIMENSION J INCLUDES SOLDER LEAD FINISH.
7. LEAD NUMBERS SHOWN FOR REFERENCE ONLY.

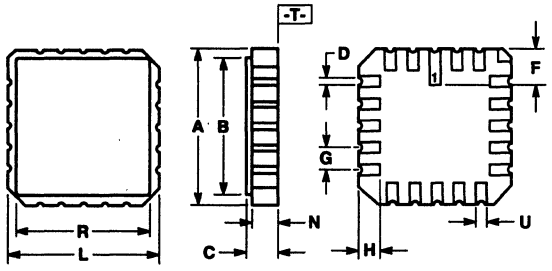
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.89	10.16	0.350	0.400
B	8.89	10.16	0.350	0.400
C	1.52	2.03	0.060	0.080
D	0.36	0.48	0.014	0.019
G	1.27 BSC		0.050 BSC	
H	0.89	1.09	0.035	0.043
J	0.10	0.18	0.004	0.007
K	7.49	8.38	0.295	0.330
S	23.88	25.65	0.940	1.010

CASE 865-01

7

Package Outlines and Mechanical Data

Leadless Ceramic Chip Carrier (LCCC) Package



NOTES:
1. DIMENSIONS A, AND L ARE DATUMS.
2. -T- IS A GAUGE PLANE.
3. POSITIONAL TOLERANCE FOR TERMINALS (D): 20 PLACES.

⌖	ϕ 0.25 (0.010) Ⓜ	T	A Ⓢ	L Ⓢ

4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
5. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.68	9.09	0.342	0.358
B	7.49	7.75	0.295	0.305
C	—	1.90	—	0.075
D	0.30	0.50	0.012	0.020
F	1.91	2.41	0.075	0.095
G	1.27 BSC		0.050 BSC	
H	1.07	1.47	0.042	0.058
L	8.68	9.09	0.342	0.358
N	1.27	1.52	0.050	0.060
R	7.49	7.74	0.295	0.305
U	0.55	0.71	0.022	0.028

CASE 756A-02

7

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33027-0 Printed in USA 7/91 EVANS PRESS EMTR 2009 25,000 BIP MIL YDACAA

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