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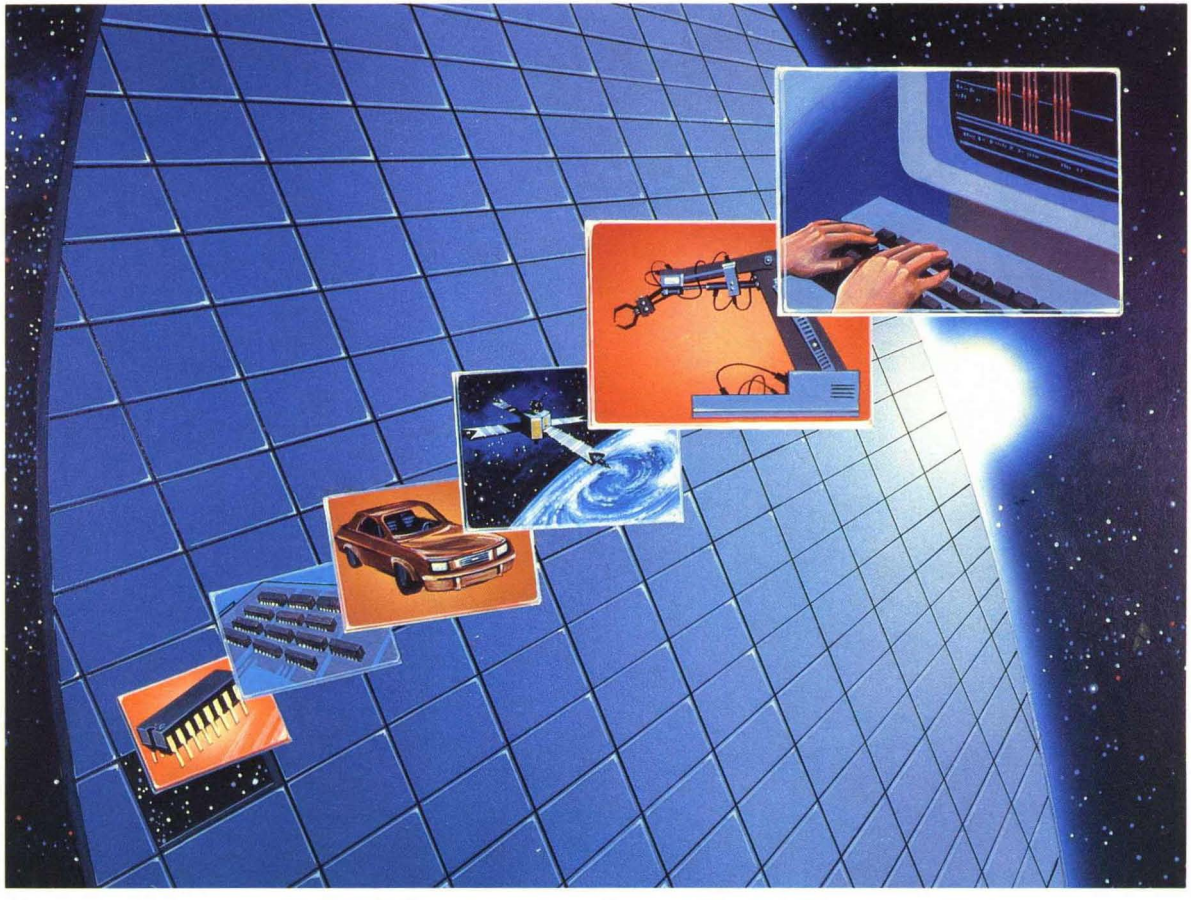
MOTOROLA



MEMORY DATA

MOTOROLA MEMORY DATA

DATA CLASSIFICATION

Product Preview

This heading on a data sheet indicates that the device is in the formative stages or in design (under development). The disclaimer at the bottom of the first page reads: "This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice."

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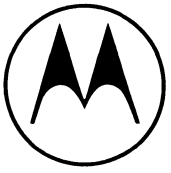

MOTOROLA

MEMORIES

Prepared by
Technical Information Center

Motorola has developed a broad range of reliable memories for virtually any digital data processing system application. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, a selector guide is included to simplify the task of choosing the best combination of circuits for optimum system architecture.

The information in this book has been carefully checked; no responsibility, however, is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent rights of the manufacturer.

New Motorola memories are being introduced continually. For the latest releases, and additional technical information or pricing, contact your nearest authorized Motorola distributor or Motorola sales office.

Series E

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Selector Guide and Cross Reference

1

MOS/CMOS

MOS Dynamic RAMs

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
64K × 4	MCM41464AP10 (P)	100	18
	MCM41464AP12 (P)	120	18
	MCM41464AP15 (P)	150	18
256K × 1	MCM6256BP10 (P)	100	16
	MCM6256BP12 (P)	120	16
	MCM6256BP15 (P)	150	16
	MCM6257BP10 (N)	100	16
	MCM6257BP12 (N)	120	16
	MCM6257BP15 (N)	150	16
256K × 4	MCM514256P85 (P)	85	20
	MCM514256P10 (P)	100	20
	MCM514256P12 (P)	120	20
	MCM514256J85 (P)	85	20/26
	MCM514256J10 (P)	100	20/26
	MCM514256J12 (P)	120	20/26
	MCM514258P85 (S)	85	20
	MCM514258P10 (S)	100	20
	MCM514258P12 (S)	120	20
	MCM514258J85 (S)	85	20/26
	MCM514258J10 (S)	100	20/26
	MCM514258J12 (S)	120	20/26
1M × 1	MCM511000P85 (P)	85	18
	MCM511000P10 (P)	100	18
	MCM511000P12 (P)	120	18
	MCM511000J85 (P)	85	20/26
	MCM511000J10 (P)	100	20/26
	MCM511000J12 (P)	120	20/26
	MCM511001P85 (N)	85	18
	MCM511001P10 (N)	100	18
	MCM511001P12 (N)	120	18
	MCM511001J85 (N)	85	20/26
	MCM511001J10 (N)	100	20/26
	MCM511001J12 (N)	120	20/26
	MCM511002P85 (S)	85	18
	MCM511002P10 (S)	100	18
	MCM511002P12 (S)	120	18
	MCM511002J85 (S)	85	20/26
	MCM511002J10 (S)	100	20/26
	MCM511002J12 (S)	120	20/26

(P) Page Mode
(N) Nibble Mode
(S) Static Column

MOS Static RAMs

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
2K × 8	MCM2016HN45 (1)	45	24
	MCM2016HN55 (1)	55	24
	MCM2016HN70 (1)	70	24
	MCM2018N35 (1)	35	24
	MCM2018N45 (1)	45	24

CMOS Static RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Access Time (ns max)	Pins
4K × 4	MCM1423P45	40	20
	IMS1423P-45	40	20
	MCM6168P45	45	20
	MCM6168P55	55	20
	MCM6168P70	70	20
	MCM6268P25	25	20
	MCM6268P35	35	20
	MCM6269P25* (2)	25	20
	MCM6269P35 (2)	35	20
8K × 8	MCM6064P10	100	28
	MCM6064P12	120	28
	MCM6064P15	150	28
	MCM60L64P10	100	28
	MCM60L64P12	120	28
	MCM60L64P15	150	28
	MCM6164C45	45	28
	MCM6164C55	55	28
	MCM61L64C45	45	28
	MCM61L64C55	55	28
	MCM6164P45*	45	28
	MCM6164P55*	55	28
	MCM61L64P45*	45	28
	MCM61L64P55*	55	28
	MCM6164J45*	45	28
	MCM6164J55*	55	28
	MCM61L64J45*	45	28
	MCM61L64J55*	55	28
	MCM6164CC55 (3)	55	28
	MCM6164CC70 (3)	70	28
	MCM6264P35*	35	28
	MCM6264P45*	45	28
	MCM6264J35*	35	28
	MCM6264J45*	45	28
16K × 4	MCM6288P25	25	22
	MCM6288P30	30	22
	MCM6288P35	35	22
	MCM6290P25* (4)	25	24
	MCM6290P30* (4)	30	24
	MCM6290P35* (4)	35	24
	MCM6290J25* (4)	25	24
	MCM6290J30* (4)	30	24
	MCM6290J35* (4)	35	24
64K × 1	MCM6287P25	25	22
	MCM6287P35	35	22
	MCM6287J25	25	24
	MCM6287J35	35	24

(Continued)

*To be introduced
(1) 300 mil package
(2) Chip select version
(3) Industrial temperature range, −40 to 85°C
(4) Output enable version

CMOS Static RAMs (Continued)

Organization	Part Number	Access Time (ns max)	Pins
32K × 8	MCM60256P85	85	28
	MCM60256P10	100	28
	MCM60256P12	120	28
	MCM60L256P85	85	28
	MCM60L256P10	100	28
	MCM60L256P12	120	28
	MCM6206P45*	45	28
	MCM6206P55*	55	28
	MCM6206P70*	70	28
	MCM6206J45*	45	28
	MCM6206J55*	55	28
	MCM6206J70*	70	28
64K × 4	MCM6208P25*	25	24
	MCM6208P35*	35	24
	MCM6208L25*	25	24
	MCM6208L35*	35	24
	MCM6208J25*	25	24
	MCM6208J35*	35	24
256K × 1	MCM6207P25*	25	24
	MCM6207P35*	35	24
	MCM6207L25*	25	24
	MCM6207L35*	35	24
	MCM6207J25*	25	24
	MCM6207J35*	35	24

Cache Tag RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Address to Match Time (ns max)	Pins
4K × 4	MCM62350P22	22	24
	MCM62350P25	25	24
	MCM62350P30	30	24
	MCM62350J22	22	24
	MCM62350J25	25	24
	MCM62350J30	30	24
	MCM62351P22	22	24
	MCM62351P25	25	24
	MCM62351P30	30	24
	MCM62351J22	22	24
	MCM62351J25	25	24
	MCM62351J30	30	24
	MCM4180P22	22	22
	MCM4180P25	25	22
	MCM4180P30	30	22

Synchronous Static RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Access Time (ns max)	Pins
16K × 4	MCM6292C25	25	28
	MCM6292C30	30	28
	MCM6292C35	35	28
	MCM6292J25	25	28
	MCM6292J30	30	28
	MCM6292J35	35	28
	MCM6293P25	25	28
	MCM6293P30	30	28
	MCM6293P35	35	28
	MCM6293J25	25	28
	MCM6293J30	30	28
	MCM6293J35	35	28
	MCM6294P25	25	28
	MCM6294P30	30	28
	MCM6294P35	35	28
	MCM6294J25	25	28
	MCM6294J30	30	28
	MCM6294J35	35	28
	MCM6295C25	25	28
	MCM6295C30	30	28
	MCM6295C35	35	28
	MCM6295J25	25	28
	MCM6295J30	30	28
	MCM6295J35	35	28

MOS Dual Port RAM

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
256 × 8	MCM68HC34L	240	40
	MCM68HC34P	240	40

MOS EEPROMs

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (μs)	Pins
16 × 16	MCM2801P	1	14
32 × 32	MCM2802P	1, 3	14
256 × 8	MCM2814P	3.5	8

MECL

RAMs

(0 to 75°C)

Organization	Part Number	Access Time (ns max)	Pins
8 × 2	MCM10143	15.3	24
16 × 4	MCM10145	15	16
16 × 4	MC10H145	6	16
64 × 1	MCM10148	15	16
128 × 1	MCM10147	15	16
256 × 1	MCM10144	26	16
256 × 1	MCM10152	15	16
1024 × 1	MCM10146	29	16
1024 × 1	MCM10415-15	15	16
1024 × 1	MCM10415-20	20	16

PROMs

(0 to 75°C)

Organization	Part Number	Access Time (ns max)	Pins
32 × 8	MCM10139	20	16
256 × 4	MCM10149-10	10	16
256 × 4	MCM10149-25	25	16

MILITARY PRODUCTS

CMOS Static RAMs

(+5 V, −55 to 125°C)

Organization	Part Number	Access Time (ns max)	Pins
4K × 4	6168-55/BRAJC	55	20
	6168-55/BYAJC	55	20
	6168-55/BUAJC	55	20
	6168-70/BRAJC	70	20
	6168-70/BYAJC	70	20
	6168-70/BUAJC	70	20
	6268-35/BRAJC	35	20
	6268-35/BYAJC	35	20
	6268-35/BUAJC	35	20
	6268-45/BRAJC	45	20
	6268-45/BYAJC	45	20
	6268-45/BUAJC	45	20
8K × 8	6164-55/BXAJC	55	28
	6164-55/BUAJC	55	32
	6164-70/BXAJC	70	28
	6164-70/BUAJC	70	32
16K × 4	6288-35/BXAJC	35	22
	6288-35/BUAJC	35	22
	6288-45/BXAJC	45	22
	6288-45/BUAJC	45	22
64K × 1	6287-35/BXAJC	35	22
	6287-35/BUAJC	35	22
	6287-45/BXAJC	45	22
	6287-45/BUAJC	45	22

CROSS REFERENCE

The part numbers in the first column are arranged in alphanumeric sequence. The "Motorola Part Number" denotes what is believed to be the functional equivalent by pin function, except for differences in select/enable functions.

NOTE: The user must verify speed, power, and package interchangeability based on detailed specifications.

Motorola does not assume any liability arising out of the application or use of any product listed.

MOS Dynamic RAM Cross Reference

Competition Part Number	Motorola Part Number	Organization
AM90C255	**MCM6256B**	256K × 1
AM90C256	**MCM6256B**	256K × 1
AM90C257	**MCM6257B**	256K × 1
HM50464	**MCM41464**	64K × 4
HM511000	**MCM511000**	1M × 1
HM511001	**MCM511001**	1M × 1
HM511002	**MCM511002**	1M × 1
HM51256	**MCM6256B**	256K × 1
HM51256L	**MCM6256B**	256K × 1
HY51C100	**MCM511000**	1M × 1
HY51C256	**MCM6256B**	256K × 1
HY51C464	**MCM41464**	64K × 4
HY51256L	**MCM6256B**	256K × 1
HY51464	**MCM41464**	64K × 4
KM41256	**MCM6256B**	256K × 1
KM41257	**MCM6257B**	256K × 1
LH21256	**MCM6256B**	256K × 1
LH21257	**MCM6257B**	256K × 1
LH2464	**MCM41464**	64K × 4
LH2465	**MCM41464**	64K × 4
LH64256	**MCM514256**	256K × 4
LH65257	**MCM514258**	256K × 4
M41256N	**MCM6256B**	256K × 1
M41256P	**MCM6256B**	256K × 1
M441024K	**MCM514258**	256K × 4
M441024P	**MCM514256**	256K × 4
M5M4C1000	**MCM511000**	1M × 1
M5M4C1001	**MCM511001**	1M × 1
M5M4C1002	**MCM511002**	1M × 1
M5M44C256	**MCM514256**	256K × 4
M5M44C258	**MCM514258**	256K × 4
M5M4464	**MCM41464**	64K × 4
MB81256	**MCM6256B**	256K × 1
MB81257	**MCM6257B**	256K × 1
MB81464	**MCM41464**	64K × 4
MN41256	**MCM6256B**	256K × 1
MSM41000	**MCM511000**	1M × 1
MSM41001	**MCM511001**	1M × 1
MSM41004	**MCM514256**	256K × 4
MSM41005	**MCM514258**	256K × 4
MSM41256	**MCM6256B**	256K × 1
MSM41257A	**MCM6257B**	256K × 1
MSM41464	**MCM41464**	64K × 4
MT1256	**MCM6256B**	256K × 1
MT4064	**MCM41464**	64K × 4

MOS DRAMs (Continued)

Competition Part Number	Motorola Part Number	Organization
TC511000	**MCM511000**	1M × 1
TC511001	**MCM511001**	1M × 1
TC511002	**MCM511002**	1M × 1
TMM41256	**MCM6256B**	256K × 1
TMM41464	**MCM41464**	64K × 4
TMS4256	**MCM6256B**	256K × 1
TMS4257	**MCM6257B**	256K × 1
TMS4C1024	**MCM511000**	1M × 1
TMS4C1025	**MCM511001**	1M × 1
TMS4C1027	**MCM511002**	1M × 1
TMS44C256	**MCM514256**	256K × 4
TMS44C257	**MCM514258**	256K × 4
TMS4464	**MCM41464**	64K × 4
μPD41256	**MCM6256B**	256K × 1
μPD41257	**MCM6257B**	256K × 1
μPD41464	**MCM41464**	64K × 4
μPD421000	**MCM511000**	1M × 1
μPD421001	**MCM511001**	1M × 1
μPD421002	**MCM511002**	1M × 1

MOS Static RAM Cross Reference

Part Number	Motorola Part Number	Organization
Am2168	**MCM1423/6168/6268/IMS1423**	4K × 4
Am2169	**MCM6269**	4K × 4
Am91L14	**MCM2114/21L14**	1K × 4
Am91L24	**MCM2114/21L14**	1K × 4
Am9114	**MCM2114/21L14**	1K × 4
Am9124	**MCM2114/21L14**	1K × 4
Am9128	**MCM2016H**	2K × 8
Am99C164	**MCM6288**	16K × 4
Am99C165	**MCM6290**	16K × 4
Am99C641	**MCM6287**	64K × 1
Am99C68	**MCM1423/6168/6268/IMS1423**	4K × 4
Am99C88	**MCM6164/61L64**	8K × 8
Am99C88	**MCM6064/60L64**	8K × 8
Am99C88L	**MCM6164/61L64**	8K × 8
Am99L68	**MCM1423/6168/6268/IMS1423**	4K × 4
CDM62256	**MCM60256/60L256**	32K × 8
CDM6264	**MCM6164/61L64/6064/60L64**	8K × 8
CXK5464	**MCM6288**	16K × 4
CXK5814	**MCM2016H**	2K × 8
CXK5864	**MCM6164/61L64**	8K × 8

Continued

MOS SRAMs (Continued)

Part Number	Motorola Part Number	Organization
CY7C128	**MCM2016H**	2K × 8
CY7C164	**MCM6288**	16K × 4
CY7C166	**MCM6290**	16K × 4
CY7C168	**MCM1423/6168/6268/IMS1423**	4K × 4
CY7C169	**MCM6269**	4K × 4
CY7C185	**MCM6164/61L64**	8K × 8
CYC7186	**MCM6164/61L64**	8K × 8
CY7C187	**MCM6287**	64K × 1
F1600	**MCM6287**	64K × 1
F1620/F1621	**MCM6288**	16K × 4
F1622	**MCM6290**	16K × 4
GM76C88	**MCM6064/60L64**	8K × 8
HM4334	**MCM2114/21L14**	1K × 4
HM4334L	**MCM2114/21L14**	1K × 4
HM472114	**MCM2114/21L14**	1K × 4
HM472114A	**MCM2114/21L14**	1K × 4
HM6168H	**MCM1423/6168/6268/IMS1423**	4K × 4
HM6168HL	**MCM1423/6168/6268/IMS1423**	4K × 4
HM62256	**MCM60256/60L256**	32K × 8
HM6264	**MCM6164/61L64/6064**	8K × 8
HM6264L	**MCM6164/61L64/60L64**	8K × 8
HM6268	**MCM1423/6168/6268/IMS1423**	4K × 4
HM6268L	**MCM1423/6168/6268/IMS1423**	4K × 4
HM6287	**MCM6287**	64K × 1
HM6287L	**MCM6287**	64K × 1
HM-6514	**MCM2114/21L14**	1K × 4
HM-6516	**MCM2016H**	2K × 8
HM-65162	**MCM2016H**	2K × 8
HM-65172	**MCM2016H**	2K × 8
HM65681	**MCM1423/6168/6268/IMS1423**	4K × 4
HM65768	**MCM1423/6168/6268/IMS1423**	4K × 4
HM6788	**MCM6288**	16K × 4
HM8832	**MCM60256**	32K × 8
HY2116	**MCM2016H**	2K × 8
HY61C16	**MCM2016H**	2K × 8
HY61C68	**MCM1423/6168/6268/IMS1423**	4K × 4
HY61C68L	**MCM1423/6168/6268/IMS1423**	4K × 4
HY6116	**MCM2016H**	2K × 8
HY62C64	**MCM6164/61L64**	8K × 8
HY62C87	**MCM6287**	64K × 1
HY62C88	**MCM6288**	16K × 4
IDT6116L	**MCM2016H**	2K × 8
IDT6116S	**MCM2016H**	2K × 8
IDT6168L	**MCM1423/6168/IMS1423**	4K × 4
IDT6168LA	**MCM6268**	4K × 4
IDT6168S	**MCM1423/6168/IMS1423**	4K × 4
IDT6168SA	**MCM6268**	4K × 4
IDT71256L	**MCM60L256**	32K × 8
IDT71256S	**MCM60256**	32K × 8
IDT7164L	**MCM61L64/60L64**	8K × 8
IDT7164S	**MCM6164/6064**	8K × 8
IDT7187L	**MCM6287**	64K × 1
IDT7187S	**MCM6287**	64K × 1
IDT7188L	**MCM6288**	16K × 4
IDT7188S	**MCM6288**	16K × 4
IDT7198L	**MCM6290**	16K × 4
IDT7198S	**MCM6290**	16K × 4
IDT8M864L	**MCM60L64**	8K × 8
IMS1420	**MCM1423/6168/6268/IMS1423**	4K × 4
IMS1420L	**MCM1423/6168/6268/IMS1423**	4K × 4

Part Number	Motorola Part Number	Organization
IMS1421	**MCM6269**	4K × 4
IMS1423	**MCM1423/6168/6268/IMS1423**	4K × 4
IMS1600	**MCM6287**	64K × 1
IMS1601	**MCM6287**	64K × 1
IMS1620	**MCM6288**	16K × 4
IMS1624	**MCM6290**	16K × 4
IMS1630	**MCM6164/61L64**	8K × 8
KM6264	**MCM6064**	8K × 8
LH5114	**MCM2114/21L14**	1K × 4
M2114	**MCM2114/21L14**	1K × 4
M2114L	**MCM2114/21L14**	1K × 4
MB81C68	**MCM1423/6168/6268/IMS1423**	4K × 4
MB81C68A	**MCM6268**	4K × 4
MB81C68W	**MCM1423/6168/6268/IMS1423**	4K × 4
MB81C69A	**MCM6269**	4K × 4
MB81C71	**MCM6287**	64K × 1
MB81C74	**MCM6288**	16K × 4
MB81C78	**MCM6164/61L64**	8K × 8
MB8114	**MCM2114/21L14**	1K × 4
MB8128	**MCM2016H**	2K × 8
MB8168	**MCM1423/6168/6268/IMS1423**	4K × 4
MB8171	**MCM6287**	64K × 1
MB8416A	**MCM2016H**	2K × 8
MB8416A-L	**MCM2016H**	2K × 8
MB8417A	**MCM2016H**	2K × 8
MB8417A-L	**MCM2016H**	2K × 8
MB8418A	**MCM2016H**	2K × 8
MB8418A-L	**MCM2016H**	2K × 8
MB84256	**MCM60256**	32K × 8
MB8464	**MCM6164/61L64/6064/60L64**	8K × 8
MB8464-L	**MCM6164/61L64/60L64**	8K × 8
MK41H68	**MCM1423/6168/6268/IMS1423**	4K × 4
MK41H69	**MCM6269**	4K × 4
MK4802	**MCM2016H**	2K × 8
MM2114	**MCM2114/21L14**	1K × 4
MM2114L	**MCM2114/21L14**	1K × 4
MSM2114L	**MCM2114/21L14**	1K × 4
MSM2128	**MCM2016H**	2K × 8
MSM5114	**MCM2114/21L14**	1K × 4
MSM5115	**MCM2114/21L14**	1K × 4
MSM5128	**MCM2016H**	2K × 8
MSM5165	**MCM6164/61L64/6064/60L64**	8K × 8
MSM5165L	**MCM6164/61L64/6064/60L64**	8K × 8
MWS5114	**MCM2114/21L14**	1K × 4
M5M2168	**MCM1423/6168/6268/IMS1423**	4K × 4
M5M5116	**MCM2016H**	2K × 8
M5M5117	**MCM2016H**	2K × 8
M5M5118	**MCM2016H**	2K × 8
M5M5165	**MCM6164/61L64**	8K × 8
M5M5165-L	**MCM6164/61L64**	8K × 8
M5M5187	**MCM6287**	64K × 1
M5M5188	**MCM6288**	16K × 4
M58981	**MCM2114/21L14**	1K × 4
NMC2114A	**MCM2114/21L14**	1K × 4
NMC2114AP	**MCM2114/21L14**	1K × 4
NMC2116	**MCM2016H**	2K × 8
NMC6164	**MCM6164/61L64**	8K × 8
NMC6164L	**MCM6164/61L64**	8K × 8
NMC6504	**MCM6147A/61L47A**	4K × 1
P4C187	**MCM6287**	64K × 1

MOS SRAMs (Continued)

Part Number	Motorola Part Number	Organization
P4C188	**MCM6288**	16K × 4
PS6168	**MCM1423/6168/6268/IMS1423**	4K × 4
SCM21C14	**MCM2114/21L14**	1K × 4
SCM21C16	**MCM2016H**	2K × 8
SCM2114AL	**MCM2114/21L14**	1K × 4
SCM6116	**MCM2016H**	2K × 8
SCM6116L	**MCM2016H**	2K × 8
SMJ5517	**MCM2016H**	2K × 8
SRM2016	**MCM2016H**	2K × 8
SRM20256	**MCM60256**	32K × 8
SRM2064	**MCM6164/61L64/6064/60L64**	8K × 8
SRM2114	**MCM2114/21L14**	1K × 4
SRM2261	**MCM6287**	64K × 1
SRM2264	**MCM6164/61L64/6064/60L64**	8K × 8
SRM2268	**MCM1423/6168/6268/IMS1423**	4K × 4
SRM2274	**MCM6288**	16K × 4
SRM2275H	**MCM6290**	16K × 4
SRM6514	**MCM2114/21L14**	1K × 4
SR16K4	**MCM1423/6168/6268/IMS1423**	4K × 4
SR64E4	**MCM6290**	16K × 4
SR64K1	**MCM6287**	64K × 1
SR64K4	**MCM6288**	16K × 4
SR64K8	**MCM6164/61L64**	8K × 8
STC2168	**MCM1423/6168/6268/IMS1423**	4K × 4
STC2168L	**MCM1423/6168/6268/IMS1423**	4K × 4
STC2168M	**MCM1423/6168/6268/IMS1423**	4K × 4
STC6264	**MCM6064/60L64**	8K × 8
S6514	**MCM2114/21L14**	1K × 4
S6516	**MCM2016H**	2K × 8
TC5513A	**MCM2114/21L14**	1K × 4
TC5513A-L	**MCM2114/21L14**	1K × 4
TC5514	**MCM2114/21L14**	1K × 4
TC5514A	**MCM2114/21L14**	1K × 4
TC5514A-L	**MCM2114/21L14**	1K × 4
TC5517B	**MCM2016H**	2K × 8
TC5517B-L	**MCM2016H**	2K × 8
TC5518C	**MCM2016H**	2K × 8
TC5518C-L	**MCM2016H**	2K × 8
TC55257	**MCM60256**	32K × 8
TC55257L	**MCM60L256**	32K × 8
TC55416	**MCM6288**	16K × 4
TC5561	**MCM6287**	64K × 1
TC5562	**MCM6287**	64K × 1
TC5564	**MCM6164/61L64/6064/60L64**	8K × 8
TC5564-L	**MCM6164/61L64/6064/60L64**	8K × 8

Part Number	Motorola Part Number	Organization
TC5565	**MCM6164/61L64/6064/60L64**	8K × 8
TC5565-L	**MCM6164/61L64/6064/60L64**	8K × 8
TMM2015A	**MCM2016H**	2K × 8
TMM2016	**MCM2016H**	2K × 8
TMM2016A	**MCM2016H**	2K × 8
TMM2018	**MCM2016H/2018**	2K × 8
TMM2019	**MCM2016H/2018**	2K × 8
TMM2063	**MCM6164/61L64/6064/60L64**	8K × 8
TMM2064	**MCM6164/61L64/6064/60L64**	8K × 8
TMM2068	**MCM1423/6168/6268/IMS1423**	4K × 4
TMM2114A	**MCM2114/21L14**	1K × 4
TMM314A	**MCM2114/21L14**	1K × 4
TMM314A-L	**MCM2114/21L14**	1K × 4
TMS2114	**MCM2114/21L14**	1K × 4
TMS2114L	**MCM2114/21L14**	1K × 4
TMS4016	**MCM2016H**	2K × 8
UM2128	**MCM2016H**	2K × 8
UM2129	**MCM2016H**	2K × 8
UM6104	**MCM2114/21L14**	1K × 4
UM6116	**MCM2016H**	2K × 8
UM6168	**MCM1423/6168/6268/IMS1423**	4K × 4
μPD4016	**MCM2016H**	2K × 8
μPD4168	**MCM6064**	8K × 8
μPD42832	**MCM60256**	32K × 8
μPD4314	**MCM1423/6168/6268/IMS1423**	4K × 4
μPD43256	**MCM60256**	32K × 8
μPD43257-L	**MCM60L256**	32K × 8
μPD4361	**MCM6287**	64K × 1
μPD4362	**MCM6288**	16K × 4
μPD4364	**MCM6164/61L64**	8K × 8
μPD4364L	**MCM6164/61L64/6064/60L64**	8K × 8
μPD446	**MCM2016H**	2K × 8
μPD4464	**MCM6164/61L64/6064/60L64**	8K × 8
μPD449	**MCM2016H**	2K × 8
VT20C68	**MCM1423/6168/6268/IMS1423**	4K × 4
VT20C69	**MCM6269**	4K × 4
VT64KS4	**MCM6288**	16K × 4
VT65KS4	**MCM6290**	16K × 4
2114A	**MCM2114/21L14**	1K × 4
2114AL	**MCM2114/21L14**	1K × 4
51C68	**MCM1423/6168/6268/IMS1423**	4K × 4
51C69	**MCM6269**	4K × 4
8808CL	**MCM60L64**	8K × 8
8832C	**MCM60256**	32K × 8

MOS Dynamic RAMs

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MOS Dynamic RAMs

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
64K × 4	MCM41464AP10 (P)	100	18
	MCM41464AP12 (P)	120	18
	MCM41464AP15 (P)	150	18
256K × 1	MCM6256BP10 (P)	100	16
	MCM6256BP12 (P)	120	16
	MCM6256BP15 (P)	150	16
	MCM6257BP10 (N)	100	16
	MCM6257BP12 (N)	120	16
	MCM6257BP15 (N)	150	16
256K × 4	MCM514256P85 (P)	85	20
	MCM514256P10 (P)	100	20
	MCM514256P12 (P)	120	20
	MCM514256J85 (P)	85	20/26
	MCM514256J10 (P)	100	20/26
	MCM514256J12 (P)	120	20/26
	MCM514258P85 (S)	85	20
	MCM514258P10 (S)	100	20
	MCM514258P12 (S)	120	20
	MCM514258J85 (S)	85	20/26
	MCM514258J10 (S)	100	20/26
	MCM514258J12 (S)	120	20/26
1M × 1	MCM511000P85 (P)	85	18
	MCM511000P10 (P)	100	18
	MCM511000P12 (P)	120	18
	MCM511000J85 (P)	85	20/26
	MCM511000J10 (P)	100	20/26
	MCM511000J12 (P)	120	20/26
	MCM511001P85 (N)	85	18
	MCM511001P10 (N)	100	18
	MCM511001P12 (N)	120	18
	MCM511001J85 (N)	85	20/26
	MCM511001J10 (N)	100	20/26
	MCM511001J12 (N)	120	20/26
	MCM511002P85 (S)	85	18
	MCM511002P10 (S)	100	18
	MCM511002P12 (S)	120	18
	MCM511002J85 (S)	85	20/26
	MCM511002J10 (S)	100	20/26
	MCM511002J12 (S)	120	20/26

(P) Page Mode
(N) Nibble Mode
(S) Static Column

MCM6256B

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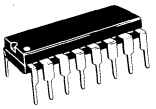
Advance Information

256K-Bit Dynamic RAM



P PACKAGE
PLASTIC
CASE 648

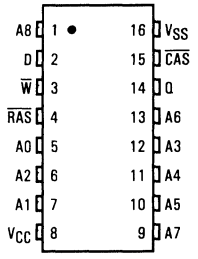
The MCM6256B is a 262,144 bit, high-speed, dynamic random access memory. Organized as 262,144 one-bit words and fabricated using N-channel silicon-gate MOS technology, this single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. All inputs and outputs are fully TTL compatible.

By multiplexing row and column address inputs, the MCM6256B requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{CAS}$ allowing greater system flexibility.

The MCM6256B features "page mode" which allows random column accesses of the 512 bits within the selected row.

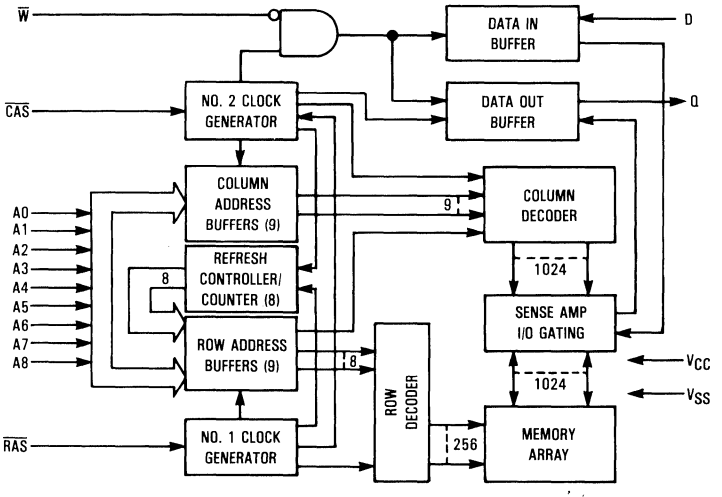
- Organized as 262,144 Words of 1 Bit
- Single +5 Volt Operation (±10%)
- Maximum Access Time: MCM6256B-10 = 100 ns
  MCM6256B-12 = 120 ns
  MCM6256B-15 = 150 ns
- Low Power Dissipation: MCM6256B-10 = 440 mW Maximum (Active)
  MCM6256B-12 = 396 mW Maximum (Active)
  MCM6256B-15 = 358 mW Maximum (Active)
  28 mW Maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{RAS}$-Only Refresh Mode
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- Page Mode Capability

PIN ASSIGNMENT



PIN NAMES	
A0-A8	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic 0 Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM6256B-10, t_{RC} = 190 ns		—	80		
MCM6256B-12, t_{RC} = 220 ns		—	72		
MCM6256B-15, t_{RC} = 260 ns		—	65		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	5.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	2
MCM6256B-10, t_{RC} = 190 ns		—	70		
MCM6256B-12, t_{RC} = 220 ns		—	62		
MCM6256B-15, t_{RC} = 260 ns		—	55		
V_{CC} Power Supply Current During Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM6256B-10, t_{PC} = 100 ns		—	60		
MCM6256B-12, t_{PC} = 120 ns		—	55		
MCM6256B-15, t_{PC} = 145 ns		—	50		
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh	I_{CC5}			mA	2
MCM6256B-10, t_{RC} = 190 ns		—	70		
MCM6256B-12, t_{RC} = 220 ns		—	62		
MCM6256B-15, t_{RC} = 260 ns		—	55		
Input Leakage Current (V_{SS} < V_{in} < V_{CC})	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, V_{SS} < V_{out} < V_{CC})	$I_{lkg(O)}$	−10	10	μA	
Output Logic 1 Voltage (I_{out} = −5 mA)	V_{OH}	2.4	—	V	
Output Logic 0 Voltage (I_{out} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit	Notes
Input Capacitance	A0-A8, D	C_{in}	—	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		—	7	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	—	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 5)

Parameter	Symbol		MCM6256B-10		MCM6256B-12		MCM6256B-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	190	–	220	–	260	–	ns	4, 5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	200	–	240	–	265	–	ns	4, 5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	220	–	260	–	310	–	ns	4, 5
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	100	–	120	–	150	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	50	–	60	–	75	ns	7, 8
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	5	25	5	30	5	35	ns	9
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	80	–	90	–	100	–	ns	–
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	–
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	–
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	50	25	60	25	75	ns	10
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RELAX}	t_{RAH}	15	–	15	–	15	–	ns	–
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	–	25	–	30	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	70	–	85	–	105	–	ns	–
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	–
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	11
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	10	–	15	–	20	–	ns	11
Write Command Hold Time	t_{CELWH}	t_{WCH}	20	–	25	–	30	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	70	–	85	–	105	–	ns	–
Write Command Pulse Width	t_{WLWH}	t_{WP}	20	–	25	–	30	–	ns	–
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	25	–	35	–	45	–	ns	–
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	25	–	35	–	45	–	ns	–
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	12
Data in Hold Time	t_{CELDX}	t_{DH}	20	–	25	–	30	–	ns	12
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	70	–	85	–	105	–	ns	–
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	–	10	–	10	–	ns	–
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	50	–	60	–	75	–	ns	–
Refresh Period	t_{RVRV}	t_{RFSH}	–	4	–	4	–	4	ms	–

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
5. AC measurements t_T = 5.0 ns.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

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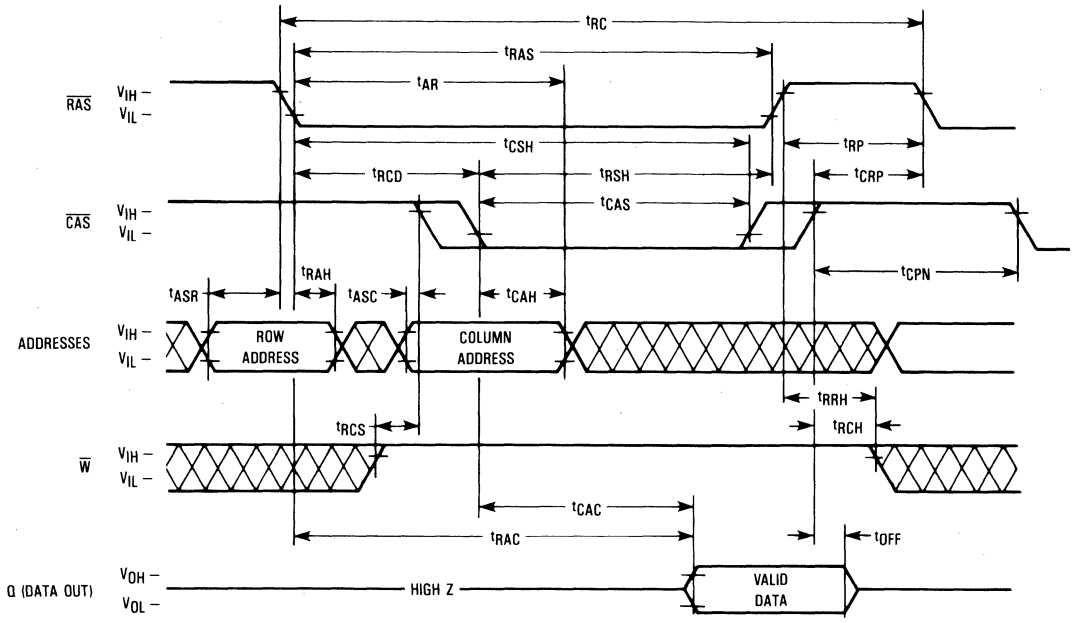
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM6256B-10		MCM6256B-12		MCM6256B-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	30	–	40	–	50	–	ns	13
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	80	–	100	–	125	–	ns	13
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	100	–	120	–	150	–	ns	–
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	15	–	20	–	25	–	ns	–
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	40	–	50	–	60	–	ns	–
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	100	–	120	–	145	–	ns	–
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	110	–	140	–	170	–	ns	–
Page Mode Read-Modify-Write Cycle Time	t_{CELCEL}	t_{PRMW}	130	–	160	–	195	–	ns	–
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	–
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	–
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	–
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	50	–	60	–	ns	–

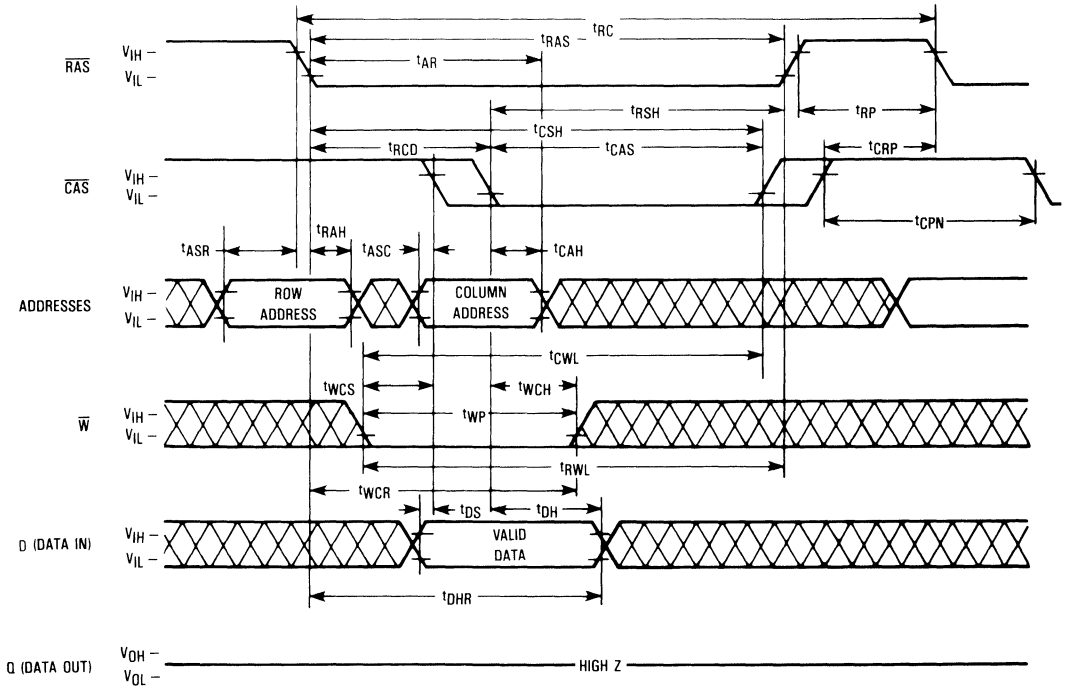
NOTES:

13. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

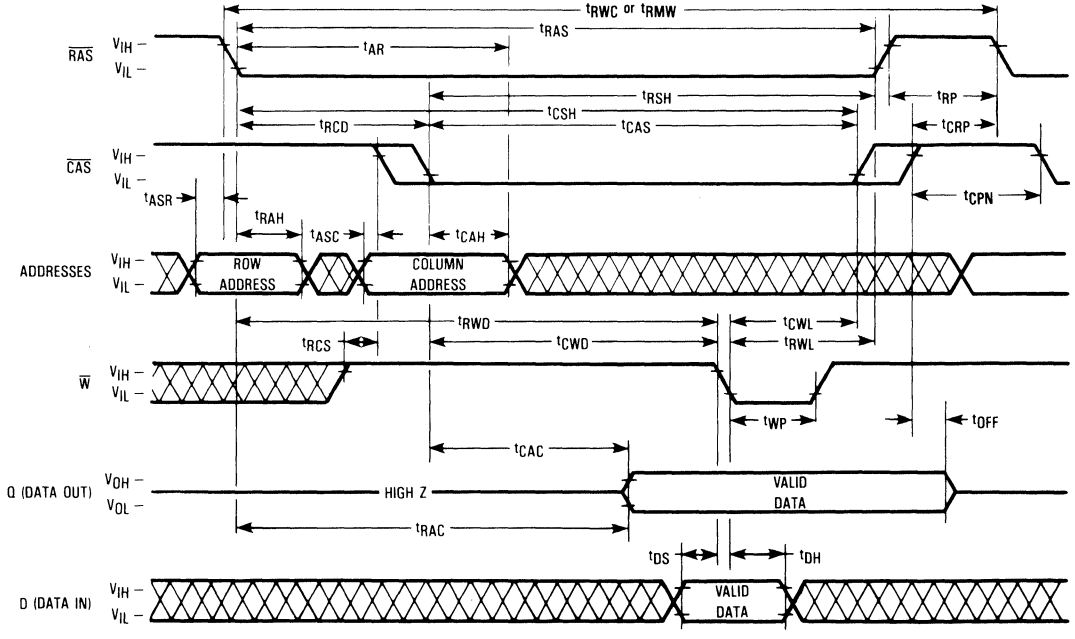
READ CYCLE TIMING



WRITE CYCLE TIMING

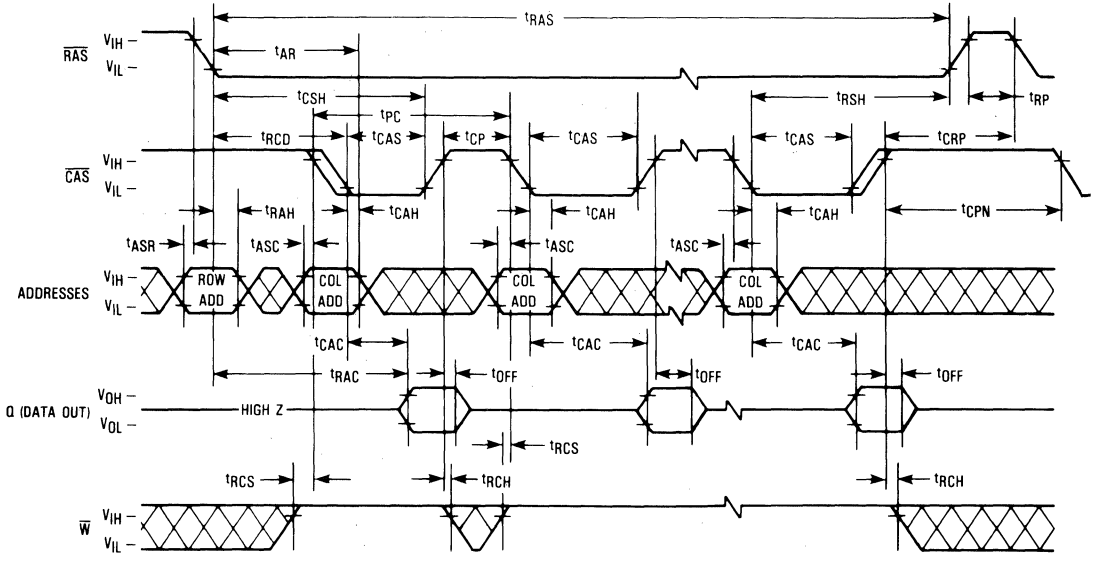


READ-WRITE/READ-MODIFY-WRITE CYCLE

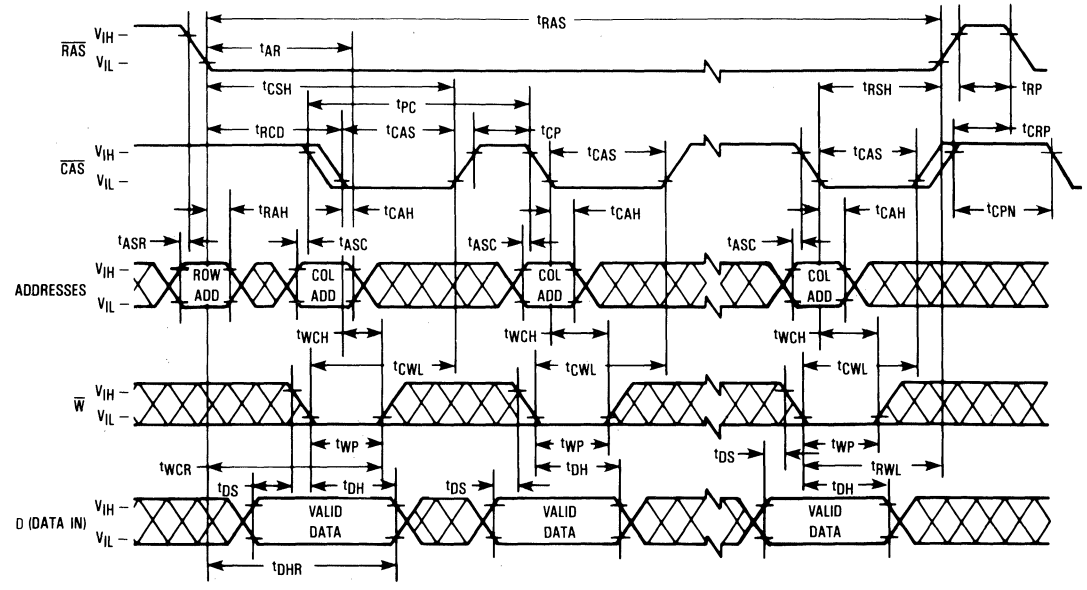


2

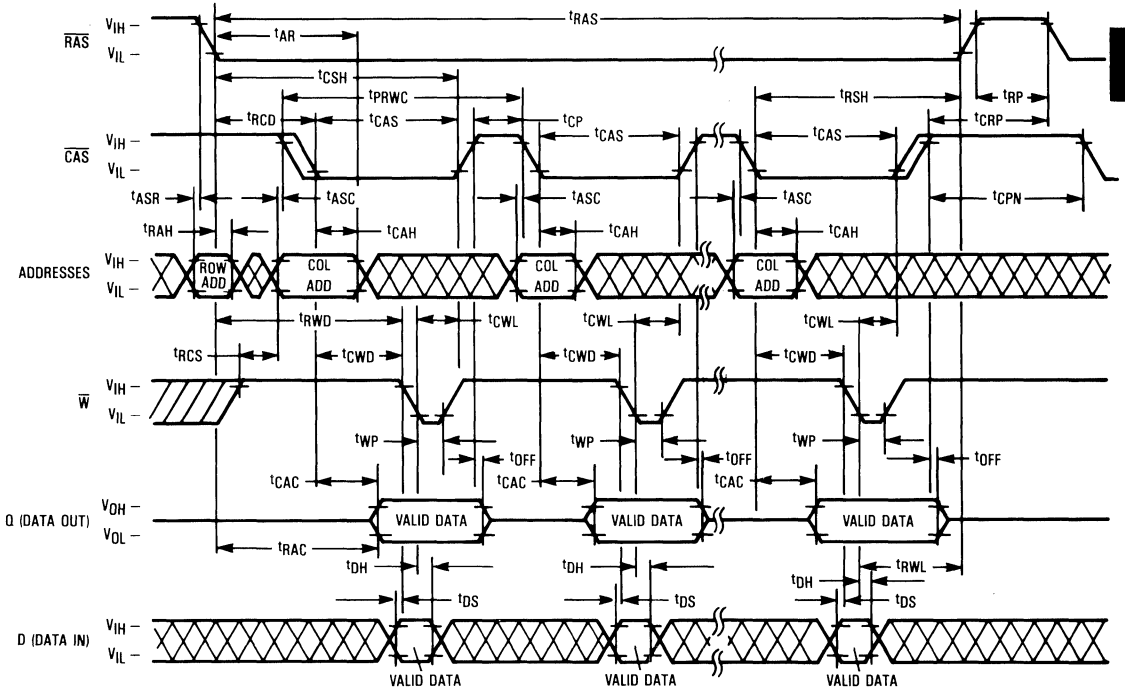
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE

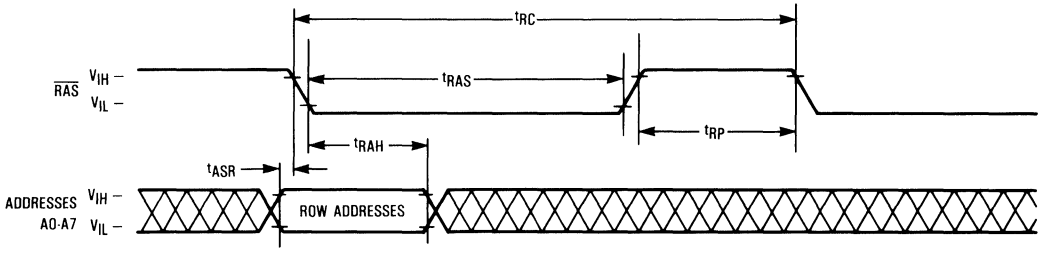


PAGE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



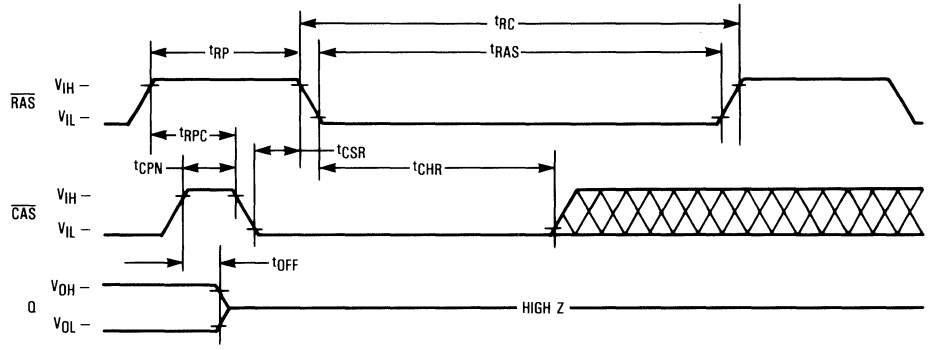
RAS-ONLY REFRESH CYCLE

(D, W, and A8 are Don't Care, CAS is High)



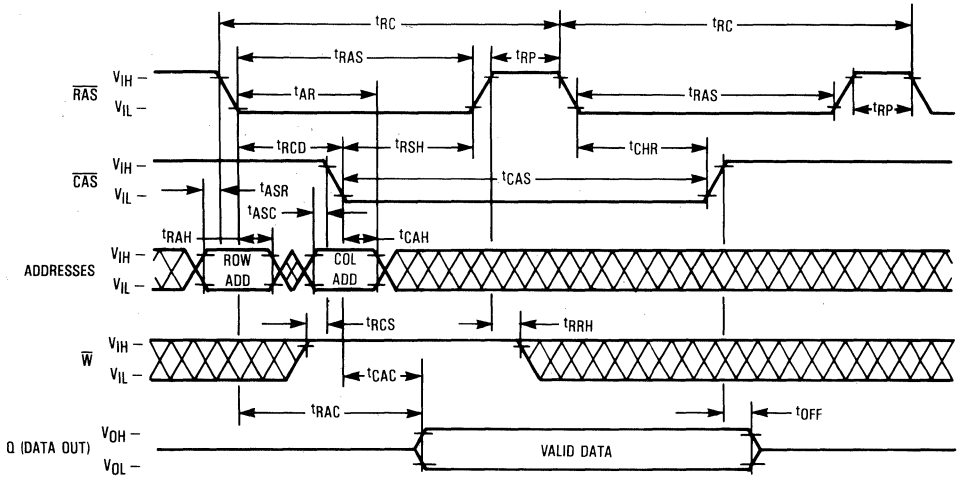
CAS-BEFORE RAS REFRESH CYCLE

(W, D, and A0-A8 are Don't Care)

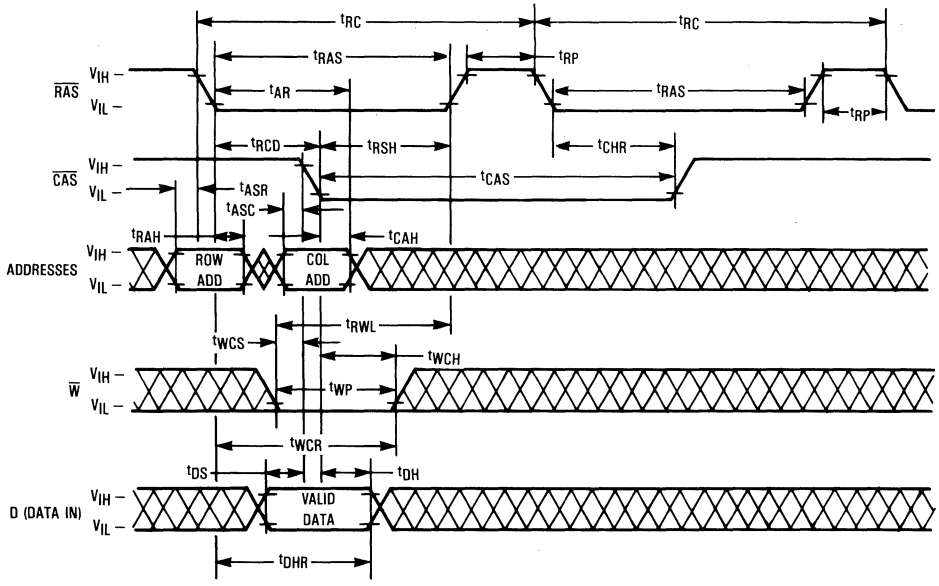


2

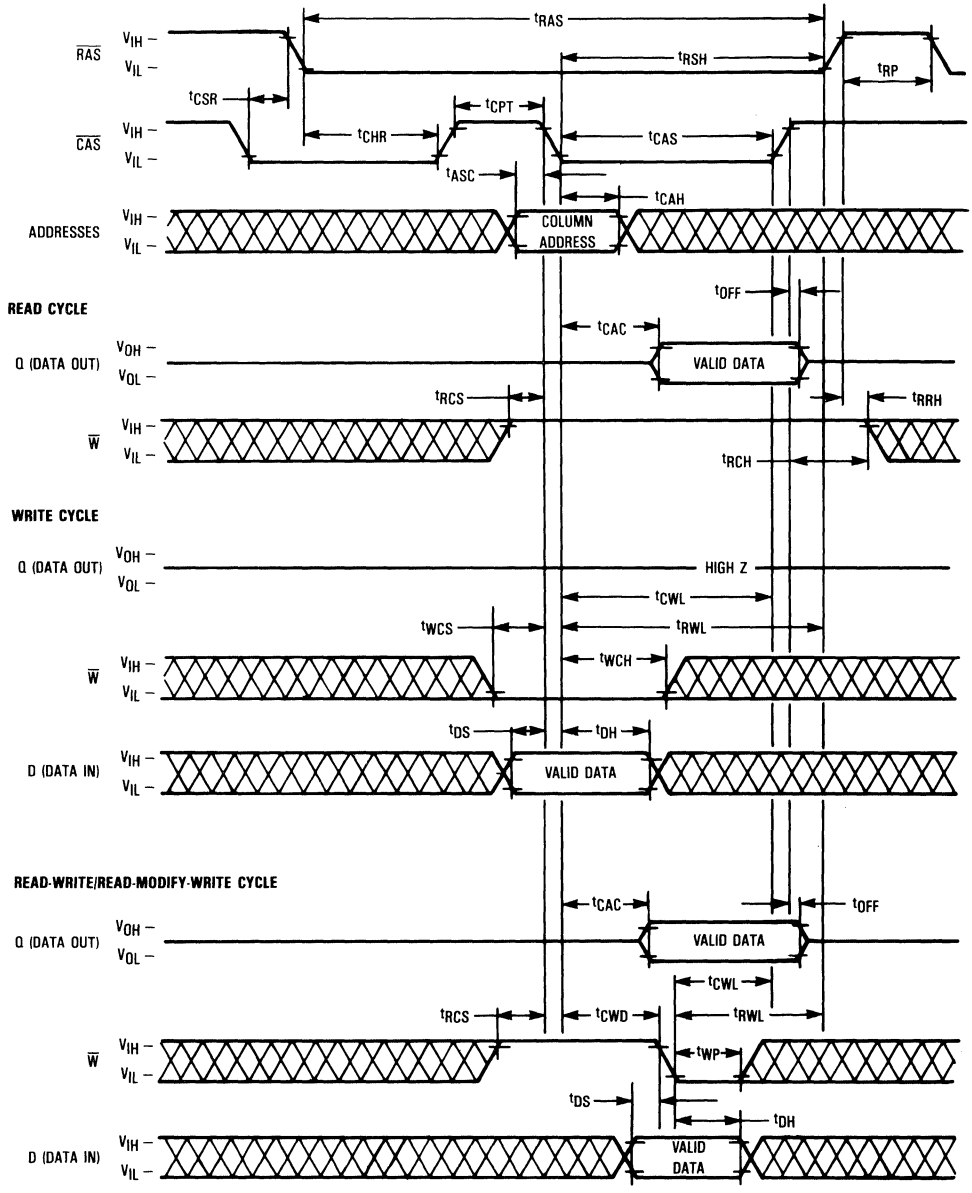
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 256K RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where an 8-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A8 (pin 1) is not required for refresh. The other variation, which is called page mode, allows the user to column access the 512 bits within a selected row. (See **PAGE-MODE CYCLES** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds $-$ $[t_{RWL} + t_{RP} + 2t_T]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out

occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at the 512 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 256K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 9-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 milliseconds. This is accomplished by sequentially cycling through the 256 row address locations every 4 milliseconds, (i.e., at least one row every 15.6 microseconds like the 64K dynamic RAM). A normal read or write operation to the RAM will serve to refresh all the bits (1024) associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 256 row addresses every 4 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM6256B can be tested by $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

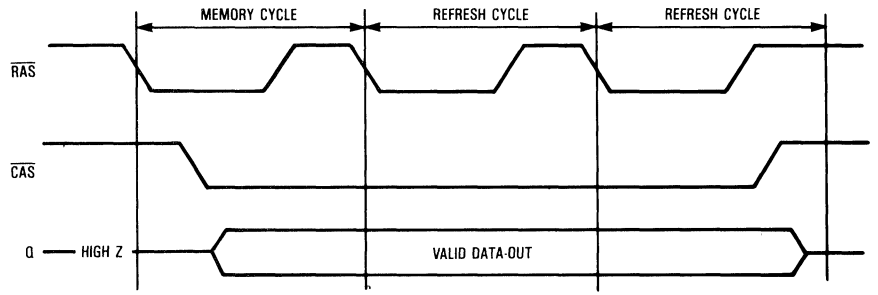
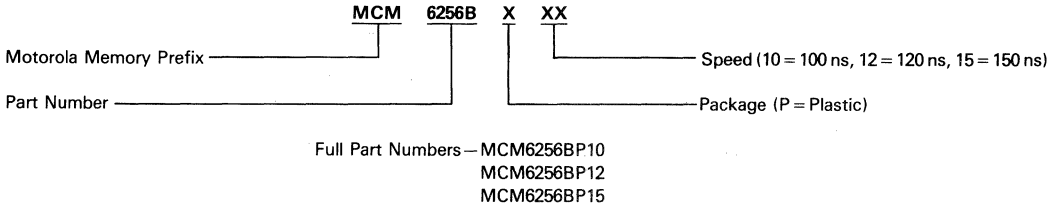


Figure 1. Hidden Refresh Cycle

2

ORDERING INFORMATION
(Order by Full Part Number)



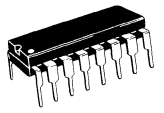
Full Part Numbers — MCM6256BP10
MCM6256BP12
MCM6256BP15

MCM6257B

2

Advance Information

256K x 1 Nibble Mode Dynamic RAM



P PACKAGE
PLASTIC
CASE 648

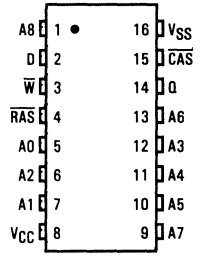
The MCM6257B is a 262,144 bit, high-speed, dynamic random access memory. Organized as 262,144 one-bit words and fabricated using N-channel silicon-gate MOS technology, this single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability. All inputs and outputs are fully TTL compatible.

By multiplexing row and column address inputs, the MCM6257B requires only nine address lines and permits packaging in standard 16-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated. Data out (Q) is controlled by $\overline{CAS}$ allowing greater system flexibility.

The MCM6257B features "nibble mode" which allows serial access of 4 bits of data at a high data rate.

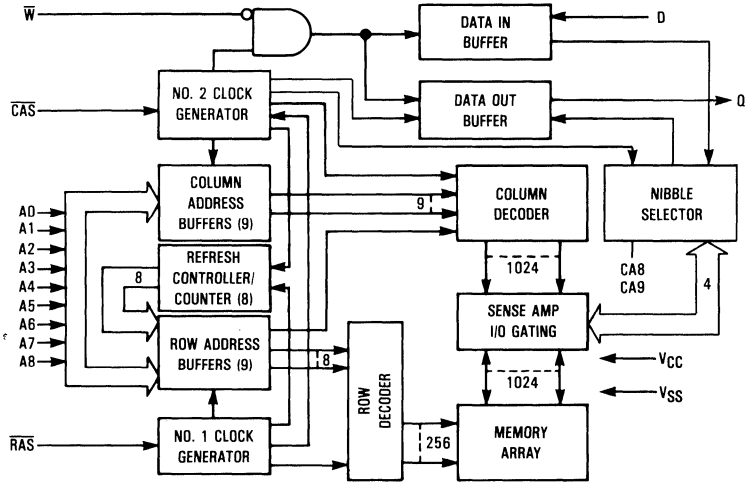
- Single +5 Volt Operation (±10%)
- Maximum Access Time: MCM6257B-10 = 100 ns
  MCM6257B-12 = 120 ns
  MCM6257B-15 = 150 ns
- Low Power Dissipation: MCM6257B-10 = 440 mW Maximum (Active)
  MCM6257B-12 = 396 mW Maximum (Active)
  MCM6257B-15 = 358 mW Maximum (Active)
  28 mW Maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ and $\overline{RAS}$-Only Refresh Modes
- Hidden Refresh
- Fast Nibble Mode Access and Cycle Time (MCM6257B-10) = 25 ns Access Time
  50 ns Cycle Time

PIN ASSIGNMENT



PIN NAMES	
A0-A8	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Input High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM6257B-10, t_{RC} = 190 ns		—	80		
MCM6257B-12, t_{RC} = 220 ns		—	72		
MCM6257B-15, t_{RC} = 260 ns		—	65		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	5.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	2
MCM6257B-10, t_{RC} = 190 ns		—	70		
MCM6257B-12, t_{RC} = 220 ns		—	62		
MCM6257B-15, t_{RC} = 260 ns		—	55		
V_{CC} Power Supply Current During Nibble Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM6257B-10, t_{NC} = 50 ns		—	50		
MCM6257B-12, t_{NC} = 60 ns		—	45		
MCM6257B-15, t_{NC} = 70 ns		—	40		
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh	I_{CC5}			mA	2
MCM6257B-10, t_{RC} = 190 ns		—	70		
MCM6257B-12, t_{RC} = 220 ns		—	62		
MCM6257B-15, t_{RC} = 260 ns		—	55		
Input Leakage Current (V_{SS} < V_{in} < V_{CC})	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, V_{SS} < V_{out} < V_{CC})	$I_{lkg(O)}$	−10	10	μA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Typ	Max	Unit	Notes
Input Capacitance	A0-A8, D	C_{in}	—	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		—	7	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q	C_{out}	—	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 5)

Parameter	Symbol		MCM6257B-10		MCM6257B-12		MCM6257B-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	190	–	220	–	260	–	ns	4, 5
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	200	–	240	–	285	–	ns	4, 5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	220	–	260	–	310	–	ns	4, 5
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	100	–	120	–	150	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	50	–	60	–	75	ns	7, 8
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	5	25	5	30	5	35	ns	9
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	80	–	90	–	100	–	ns	–
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	–
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	50	10,000	60	10,000	75	10,000	ns	–
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	50	25	60	25	75	ns	10
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RELAX}	t_{RAH}	15	–	15	–	15	–	ns	–
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	–	25	–	30	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	70	–	85	–	105	–	ns	–
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	–
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	11
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	10	–	15	–	20	–	ns	11
Write Command Hold Time	t_{CELWH}	t_{WCH}	20	–	25	–	30	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	70	–	85	–	105	–	ns	–
Write Command Pulse Width	t_{WLWH}	t_{WP}	20	–	25	–	30	–	ns	–
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	25	–	35	–	45	–	ns	–
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	25	–	35	–	45	–	ns	–
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	12
Data in Hold Time	t_{CELDX}	t_{DH}	20	–	25	–	30	–	ns	12
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	70	–	85	–	105	–	ns	–
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	–	10	–	10	–	ns	–
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	50	–	60	–	75	–	ns	–
Refresh Period	t_{RVRV}	t_{RFSH}	–	4	–	4	–	4	ms	–

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
5. AC measurements t_T = 5.0 ns.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

2

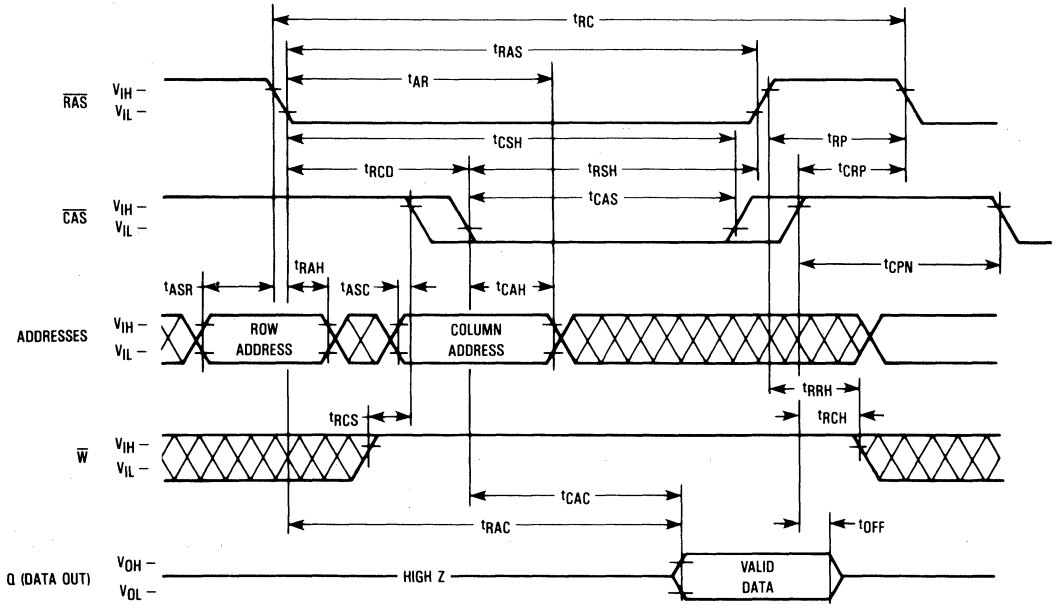
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM6257B-10		MCM6257B-12		MCM6257B-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	30	–	40	–	50	–	ns	13
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	80	–	100	–	125	–	ns	13
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	100	–	120	–	150	–	ns	–
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	15	–	20	–	25	–	ns	–
Nibble Mode Cycle Time	t_{CEHCEH}	t_{NC}	50	–	60	–	70	–	ns	–
Nibble Mode Read-Write/Read-Modify-Write Cycle Time	t_{CEHCEH}	t_{NRWC}	75	–	90	–	105	–	ns	–
Nibble Mode Access Time	t_{CELQV}	t_{NCAC}	25	–	30	–	40	–	ns	–
Nibble Mode $\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{NCAS}	25	–	30	–	40	–	ns	–
Nibble Mode $\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{NCP}	15	–	20	–	20	–	ns	–
Nibble Mode $\overline{RAS}$ Hold Time (Read)	t_{CELREH}	t_{NRRSH}	20	–	25	–	30	–	ns	–
Nibble Mode $\overline{RAS}$ Hold Time (Write)	t_{CELREH}	t_{NWRSH}	40	–	45	–	50	–	ns	–
Nibble Mode $\overline{CAS}$ to Write Delay Time	t_{CELWH}	t_{NCWD}	25	–	30	–	40	–	ns	–
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{NCWL}	20	–	25	–	30	–	ns	–
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	–
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	–
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	–
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	40	–	50	–	60	–	ns	–

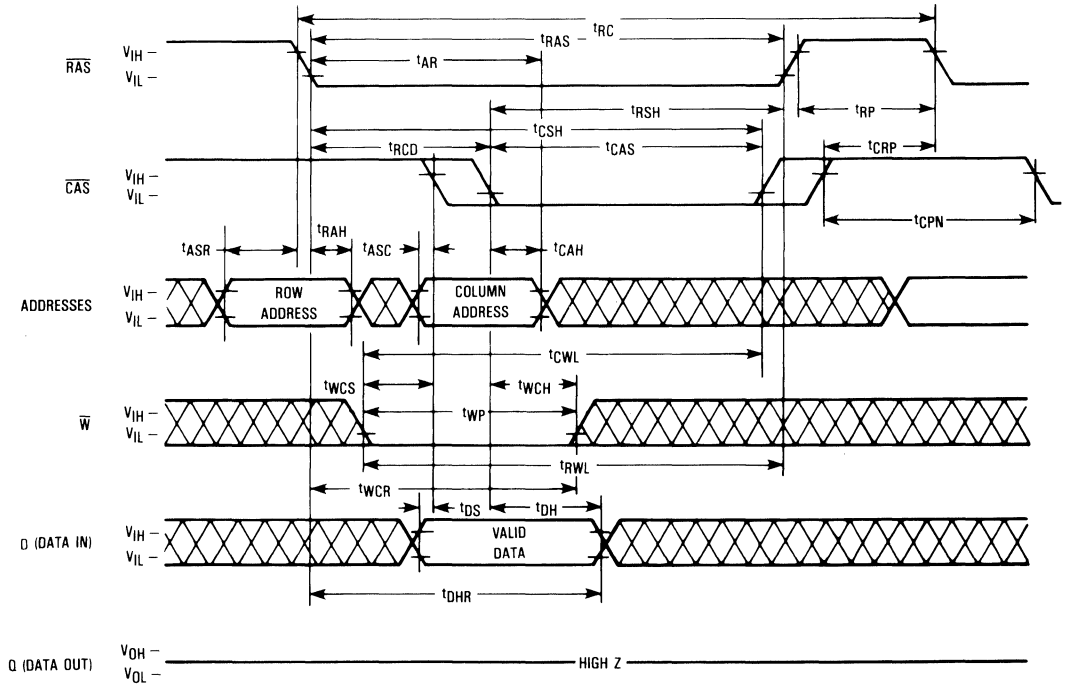
NOTES:

13. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

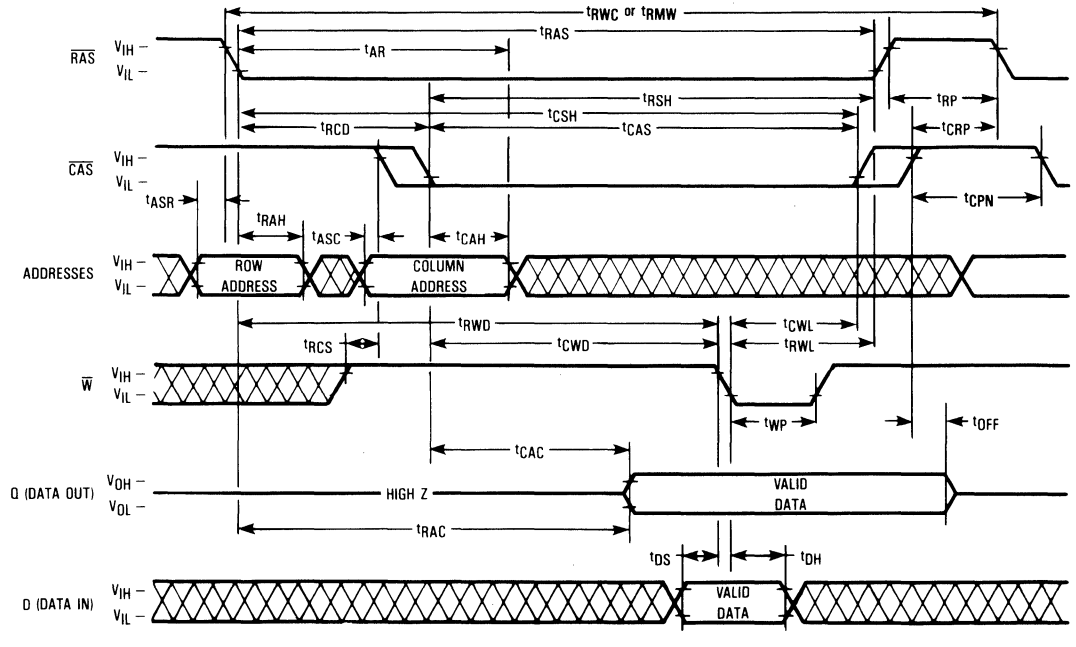
READ CYCLE TIMING



WRITE CYCLE TIMING

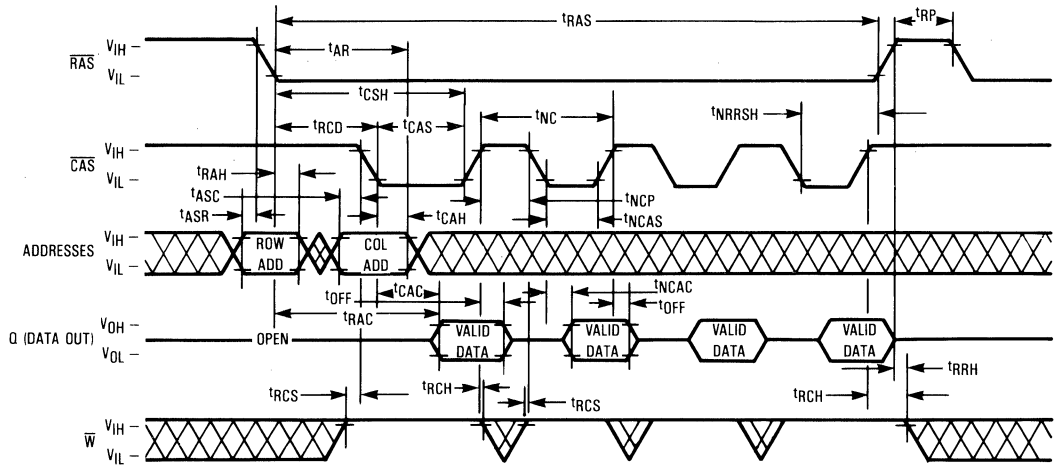


READ-WRITE/READ-MODIFY-WRITE CYCLE

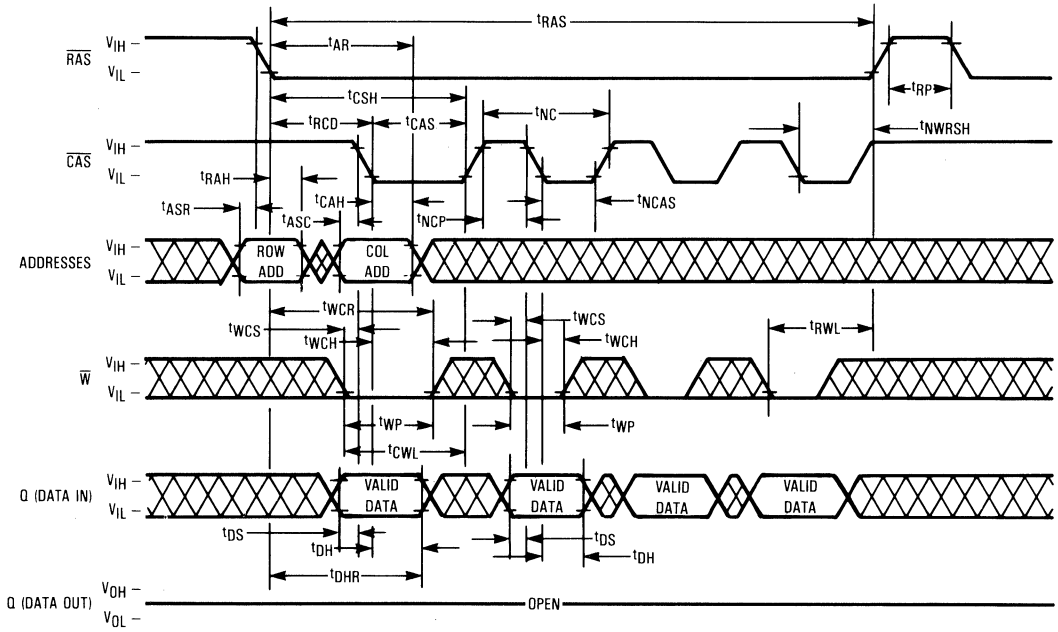


2

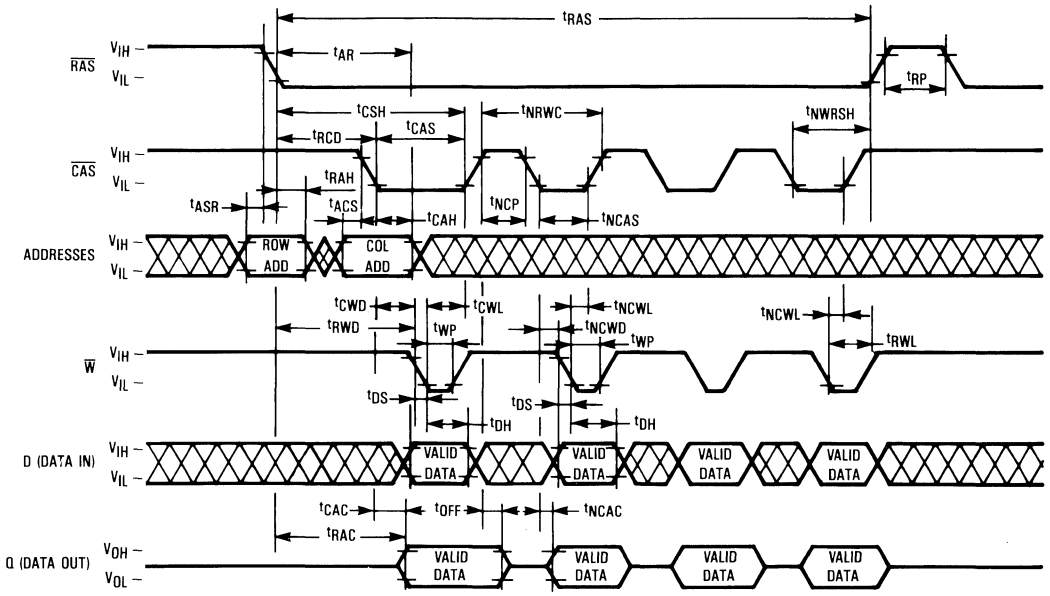
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE (EARLY WRITE)

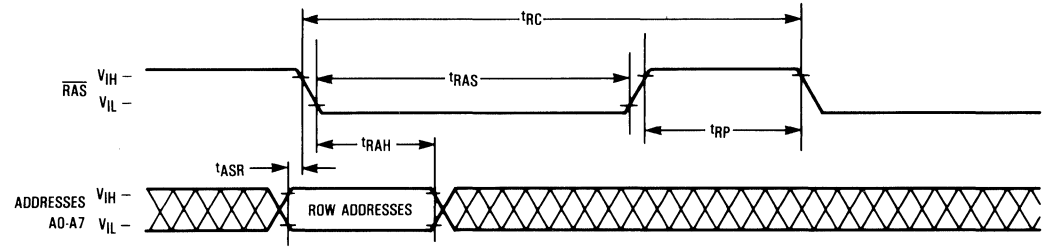


NIBBLE MODE READ-WRITE/READY-MODIFY-WRITE CYCLE



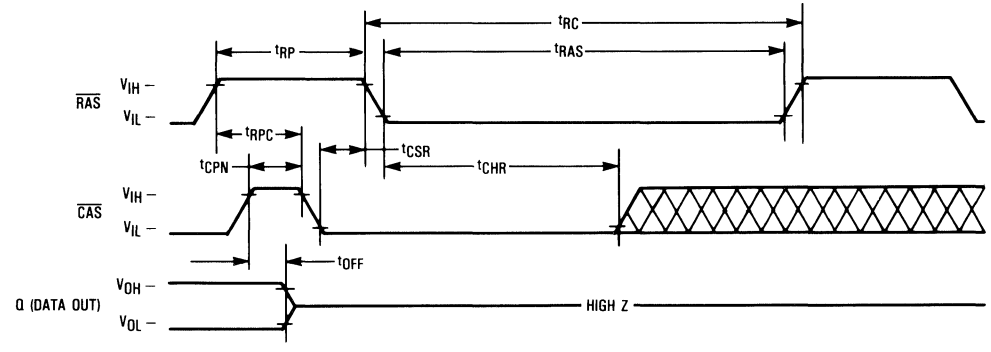
RAS-ONLY REFRESH CYCLE

(D, W, and A8 are Don't Care, CAS is High)



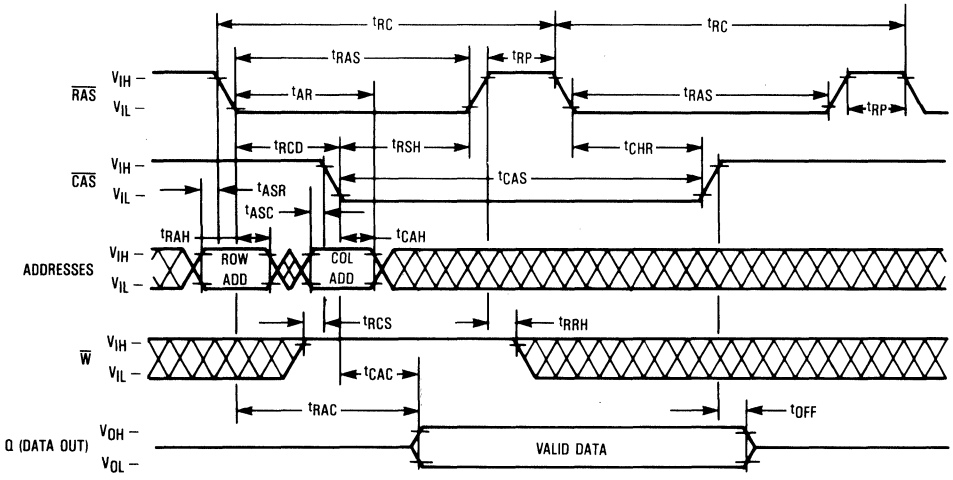
CAS-BEFORE RAS REFRESH CYCLE

(W, D, and A0-A8 are Don't Care)

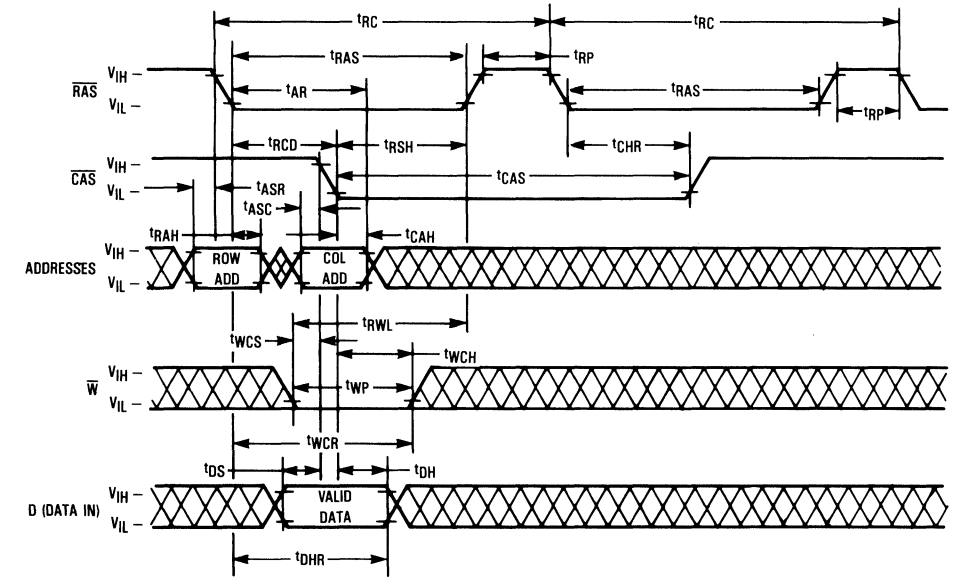


2

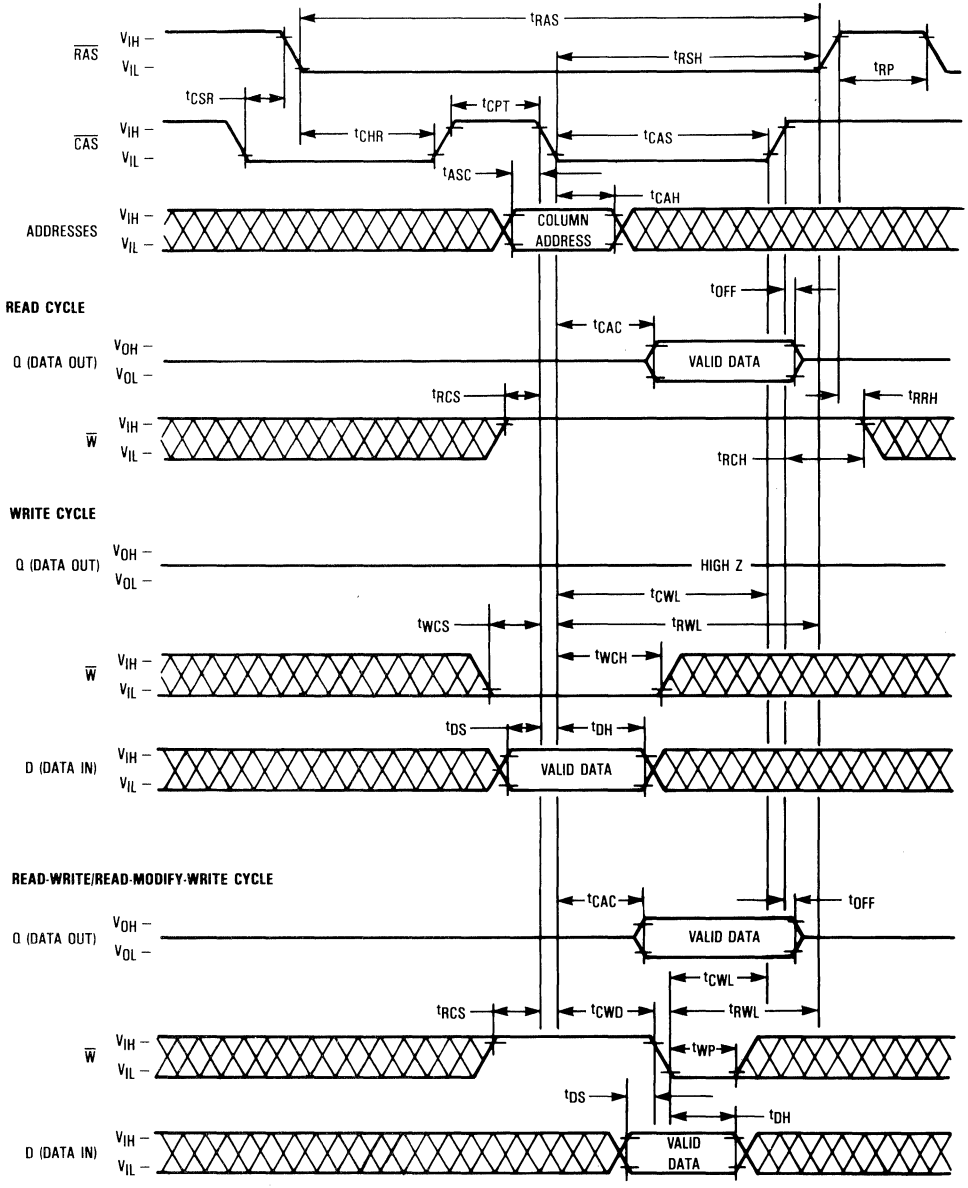
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of eighteen address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 256K RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where an 8-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A8 (pin 1) is not required for refresh. The other variation, which is called nibble mode, allows the user to access 4 bits serially. (See **NIBBLE MODE** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important

role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

NIBBLE MODE

Nibble mode allows high speed serial read, write, or read-modify-write access of 2, 3, or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA8, RA8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA8 and CA8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access.

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 milliseconds. This is accomplished by sequentially cycling through the 256 row address locations every 4 milliseconds, (i.e., at least one row every 15.6 microseconds like the 64K dynamic RAM). A normal read or write operation to the RAM will serve to refresh all the bits (1024) associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 256 row addresses every 4 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM6257B can be tested by $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

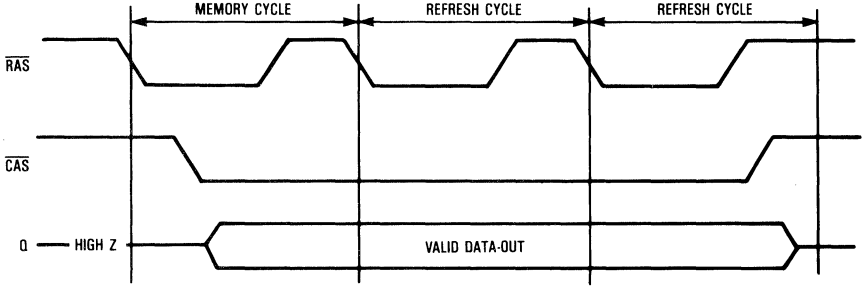
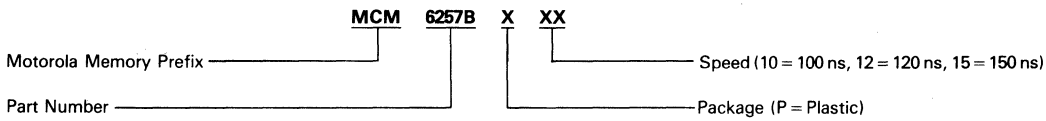


Figure 1. Hidden Refresh Cycle

2

ORDERING INFORMATION
(Order by Full Part Number)



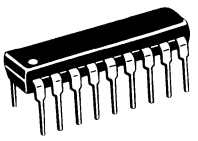
Full Part Numbers—MCM6257BP10
MCM6257BP12
MCM6257BP15

MCM41464A

2

Advance Information

64K x 4 Dynamic RAM



P PACKAGE
PLASTIC
CASE 707

The MCM41464A is a 262,144 bit, high-speed, dynamic random access memory. Organized as 65,536 words of 4 bits, and fabricated using N-channel silicon-gate MOS technology, this new single +5 volt supply dynamic RAM combines high performance with low cost and improved reliability.

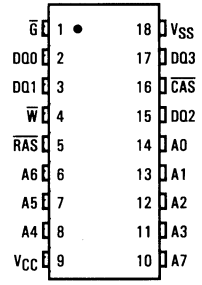
By multiplexing row and column address inputs, the MCM41464A requires only eight address lines and permits packaging in standard 18-pin 300 mil wide dual-in-line packages. Complete address decoding is done on-chip with address latches incorporated.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM41464A incorporates a one transistor cell design and dynamic storage techniques.

The MCM41464A features "page mode" which allows random column accesses of the 256 bits within the selected row.

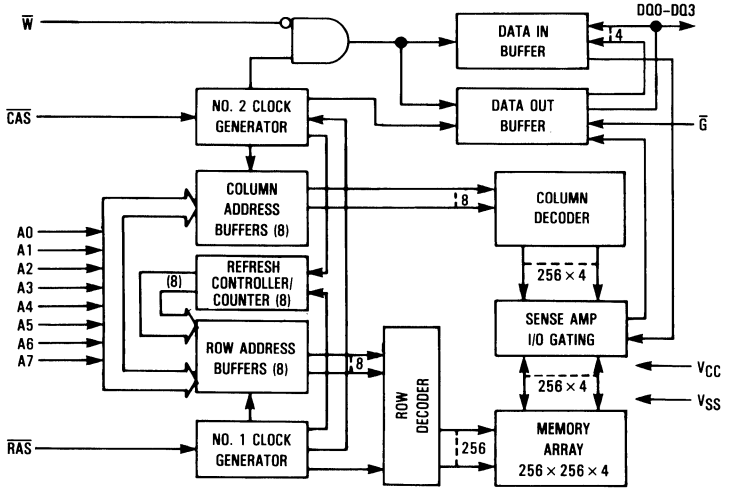
- Organized as 65,536 Words of 4 Bits
- Single +5 Volt Operation (±10%)
- Maximum Access Time: MCM41464A-10 = 100 ns
  MCM41464A-12 = 120 ns
  MCM41464A-15 = 150 ns
- Low Power Dissipation: MCM41464A-10 = 440 mW
  MCM41464A-12 = 396 mW Maximum (Active)
  MCM41464A-15 = 358 mW Maximum (Active)
  28 mW Maximum (Standby)
- Three-State Data Output
- Early-Write Common I/O Capability
- 256 Cycle, 4 ms Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh Mode
- Hidden Refresh
- $\overline{RAS}$-Only Refresh Mode
- Page Mode Capability

PIN ASSIGNMENT



PIN NAMES	
A0-A7	Address Input
DQ0-DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1
Input High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Input Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM41464A-10, t_{RC} = 190 ns		–	80		
MCM41464A-12, t_{RC} = 220 ns		–	72		
MCM41464A-15, t_{RC} = 260 ns		–	65		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	–	5.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS} = V_{IH}$)	I_{CC3}			mA	2
MCM41464A-10, t_{RC} = 190 ns		–	70		
MCM41464A-12, t_{RC} = 220 ns		–	62		
MCM41464A-15, t_{RC} = 260 ns		–	55		
V_{CC} Power Supply Current During Page Mode Cycle ($\overline{RAS} = V_{IL}$)	I_{CC4}			mA	2
MCM41464A-10, t_{PC} = 100 ns		–	70		
MCM41464A-12, t_{PC} = 120 ns		–	55		
MCM41464A-15, t_{PC} = 145 ns		–	50		
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh	I_{CC5}			mA	2
MCM41464A-10, t_{RC} = 190 ns		–	70		
MCM41464A-12, t_{RC} = 220 ns		–	62		
MCM41464A-15, t_{RC} = 260 ns		–	55		
Input Leakage Current ($V_{SS} < V_{in} < V_{CC}$)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} < V_{out} < V_{CC}$)	$I_{lkg(O)}$	−10	10	μA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A7, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	pF	3
Output Capacitance ($\overline{CAS} = V_{IH}$ to Disable Output)	Q	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 5)

Parameter	Symbol		MCM41464A-10		MCM41464A-12		MCM41464A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	190	—	220	—	260	—	ns	4, 5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	260	—	300	—	355	—	ns	4, 5
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	100	—	120	—	150	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	50	—	60	—	75	ns	7, 8
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	30	0	35	0	40	ns	9
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	80	—	90	—	100	—	ns	—
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	100	10,000	120	10,000	150	10,000	ns	—
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	50	10,000	50	10,000	75	10,000	ns	—
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	50	25	60	25	75	ns	10
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	—
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	15	—	15	—	ns	—
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	—
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	—	25	—	35	—	ns	—
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	70	—	85	—	110	—	ns	—
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	—
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	—
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	11
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	10	—	15	—	20	—	ns	11
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	30	—	35	—	45	—	ns	—
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	80	—	95	—	120	—	ns	—
Write Command Pulse Width	t_{WLWH}	t_{WP}	30	—	35	—	45	—	ns	—
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	30	—	35	—	45	—	ns	—
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	30	—	35	—	45	—	ns	—
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	12
Data in Hold Time	t_{CELDX}	t_{DH}	30	—	35	—	45	—	ns	12
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	80	—	95	—	120	—	ns	—
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	10	—	ns	—
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	50	—	60	—	75	—	ns	—
Refresh Period	t_{RVRV}	t_{RFSH}	—	4	—	4	—	4	ms	—

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
5. AC measurements t_T = 5.0 ns.
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
10. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
11. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
12. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

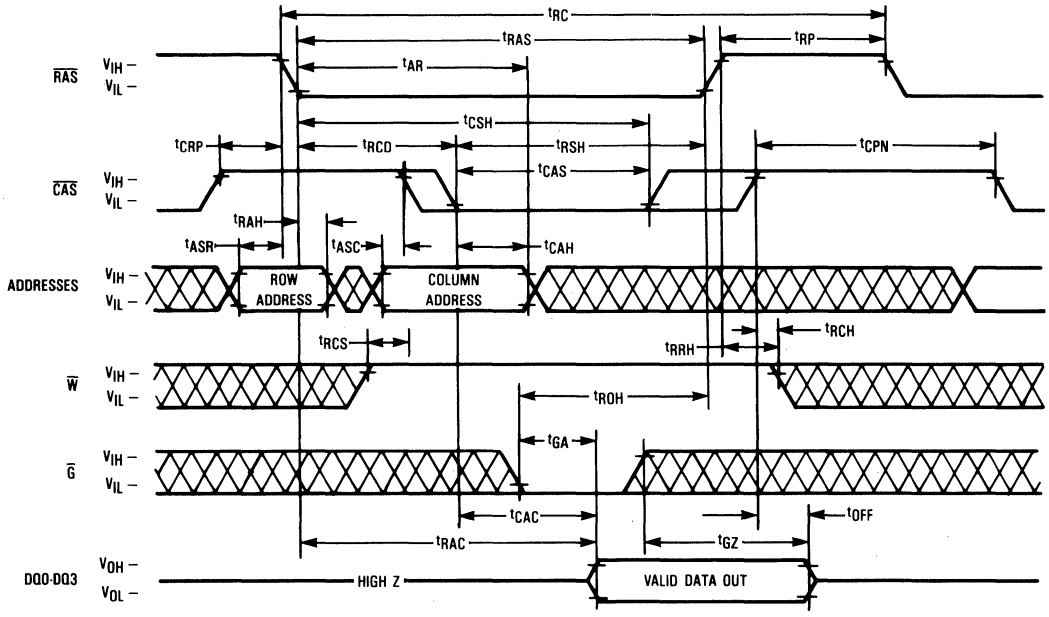
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM41464A-10		MCM41464A-12		MCM41464A-15		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	13
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	85	–	100	–	120	–	ns	13
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	135	–	160	–	195	–	ns	13
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	100	–	120	–	150	–	ns	–
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	20	–	20	–	25	–	ns	–
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	40	–	50	–	60	–	ns	–
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	100	–	120	–	145	–	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	–	25	–	30	–	40	ns	–
$\overline{G}$ to Data Delay	t_{GHDX}	t_{GD}	25	–	30	–	40	–	ns	–
Output Buffer Turn-off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	25	0	30	0	40	ns	–
$\overline{G}$ Command Hold Time	t_{WLGH}	t_{GH}	25	–	30	–	40	–	ns	–
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	–	10	–	10	–	ns	–
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	–
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	–
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	–
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	20	–	50	–	60	–	ns	–

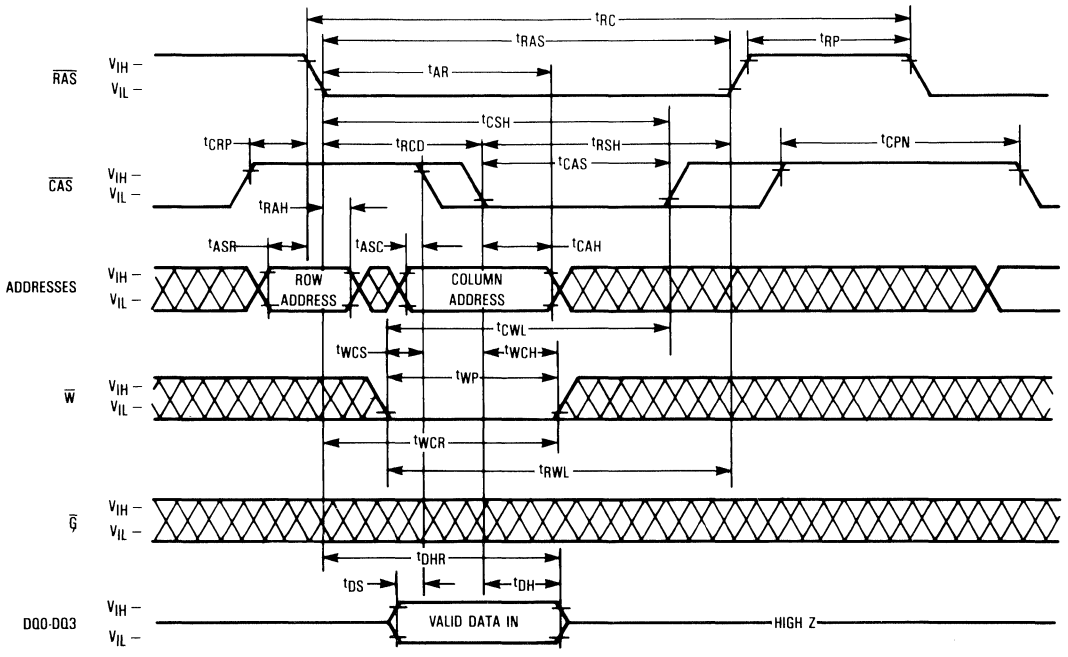
NOTES:

13. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

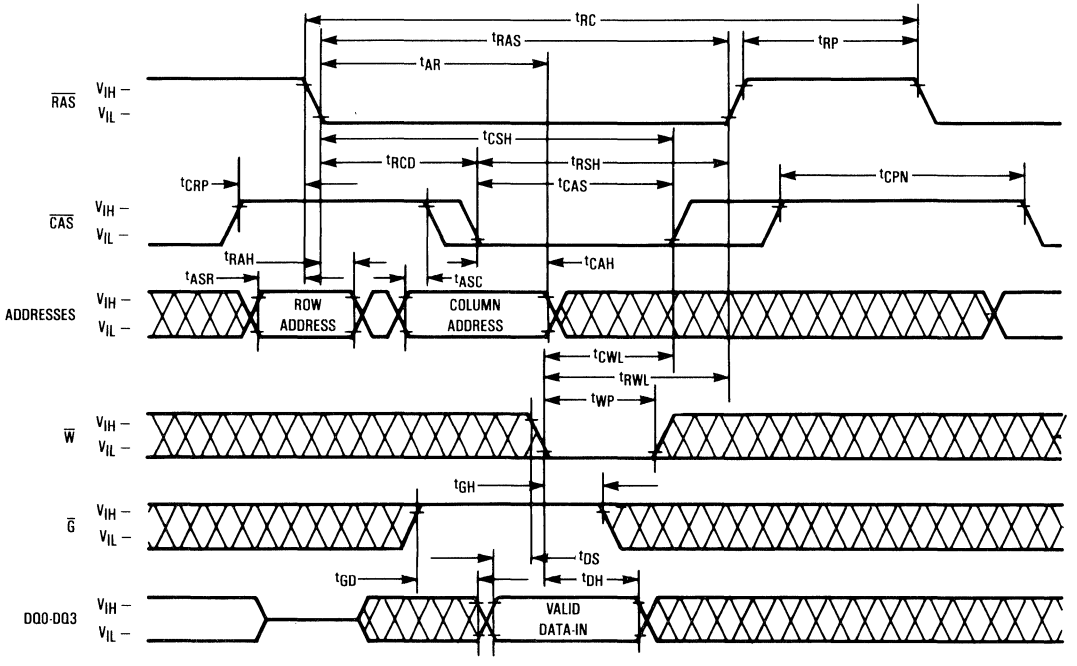
READ CYCLE



WRITE CYCLE (EARLY WRITE)

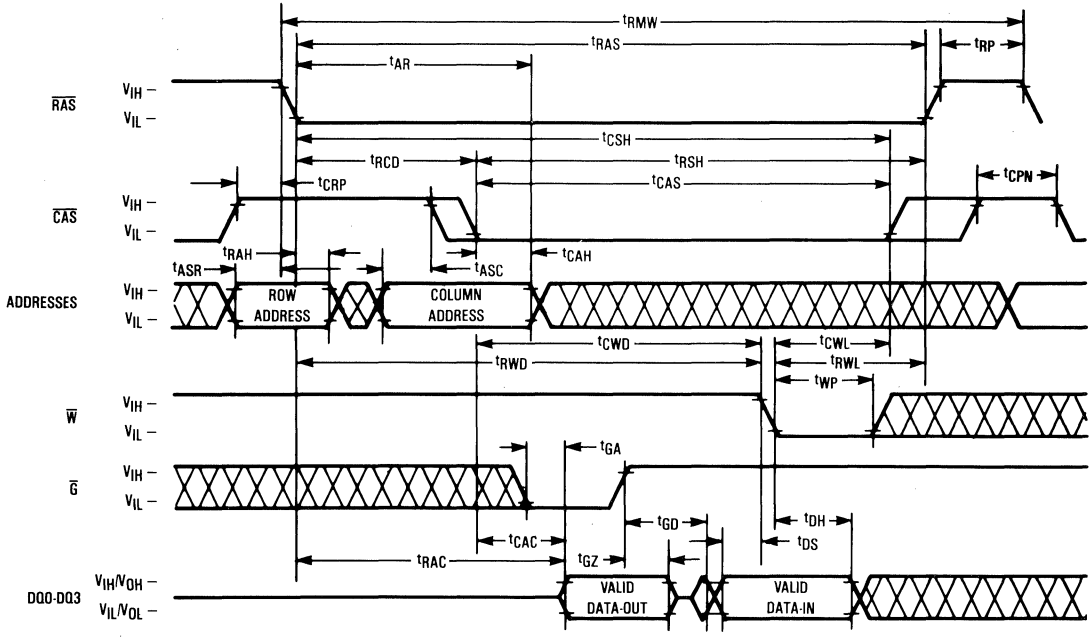


WRITE CYCLE (G CONTROLLED WRITE)

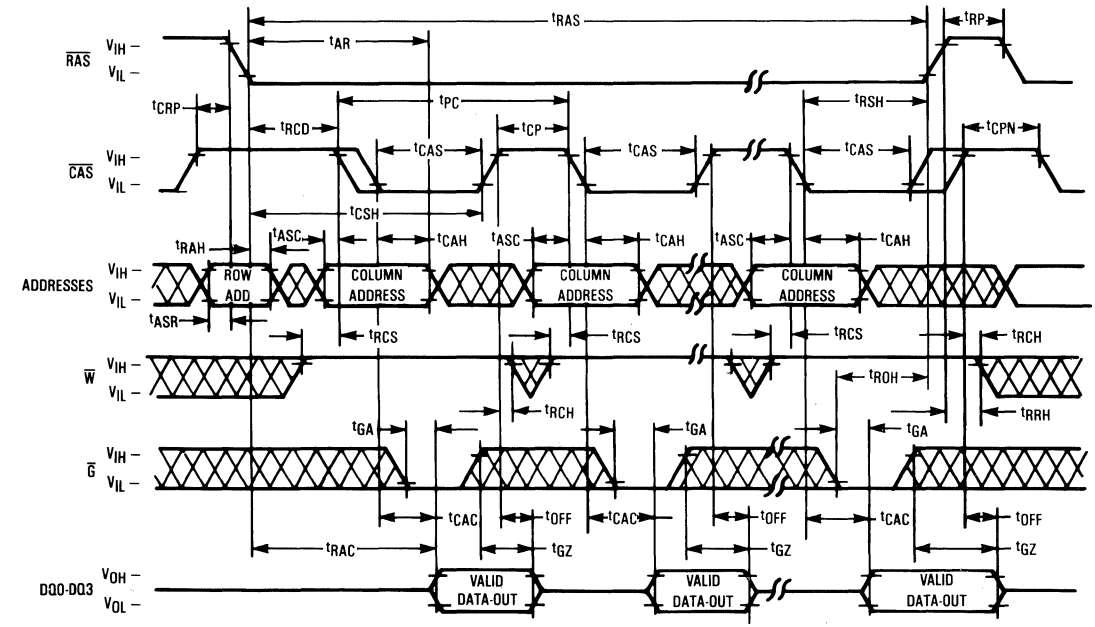


2

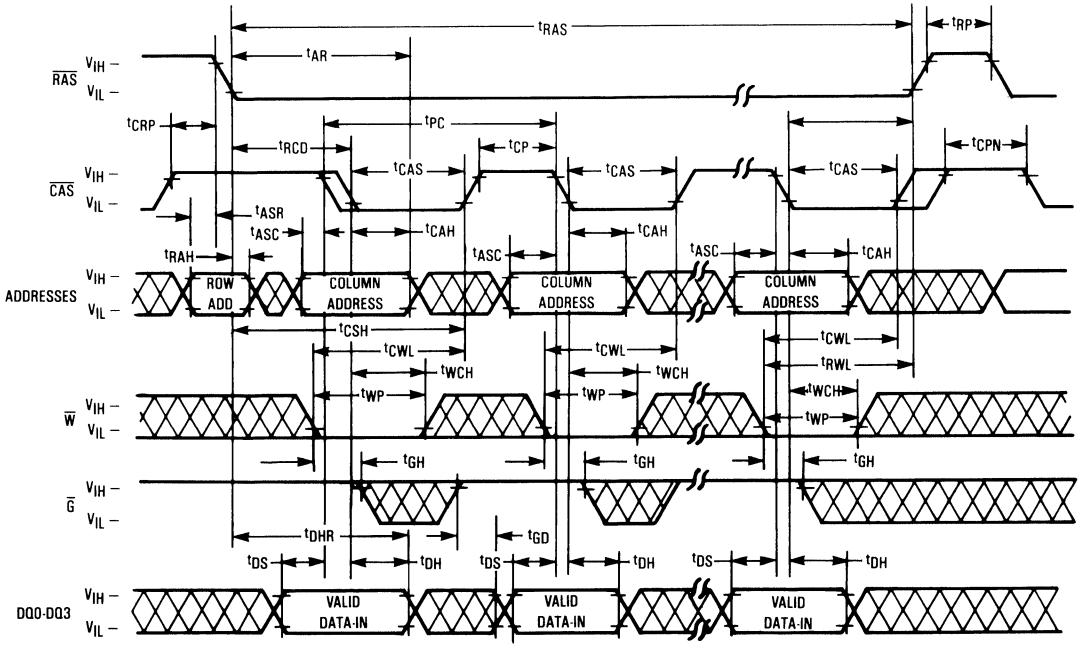
READ-MODIFY-WRITE CYCLE



PAGE MODE READ CYCLE

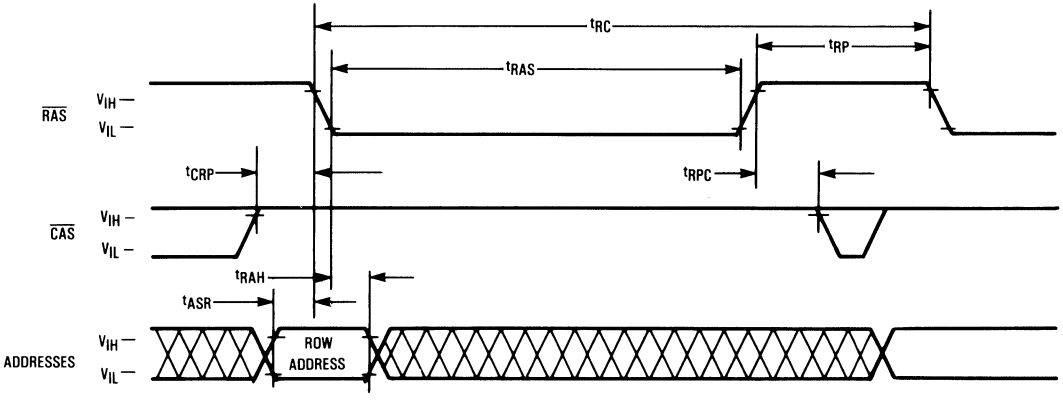


PAGE MODE WRITE CYCLE



RAS ONLY REFRESH CYCLE

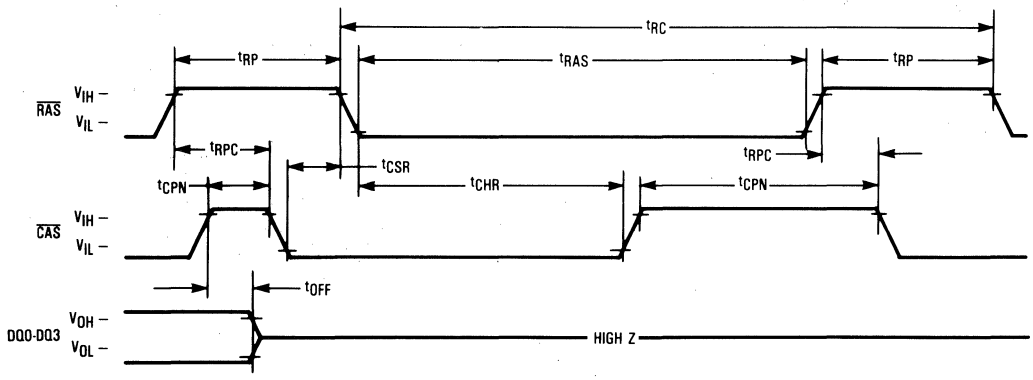
(W and G are Don't Care)



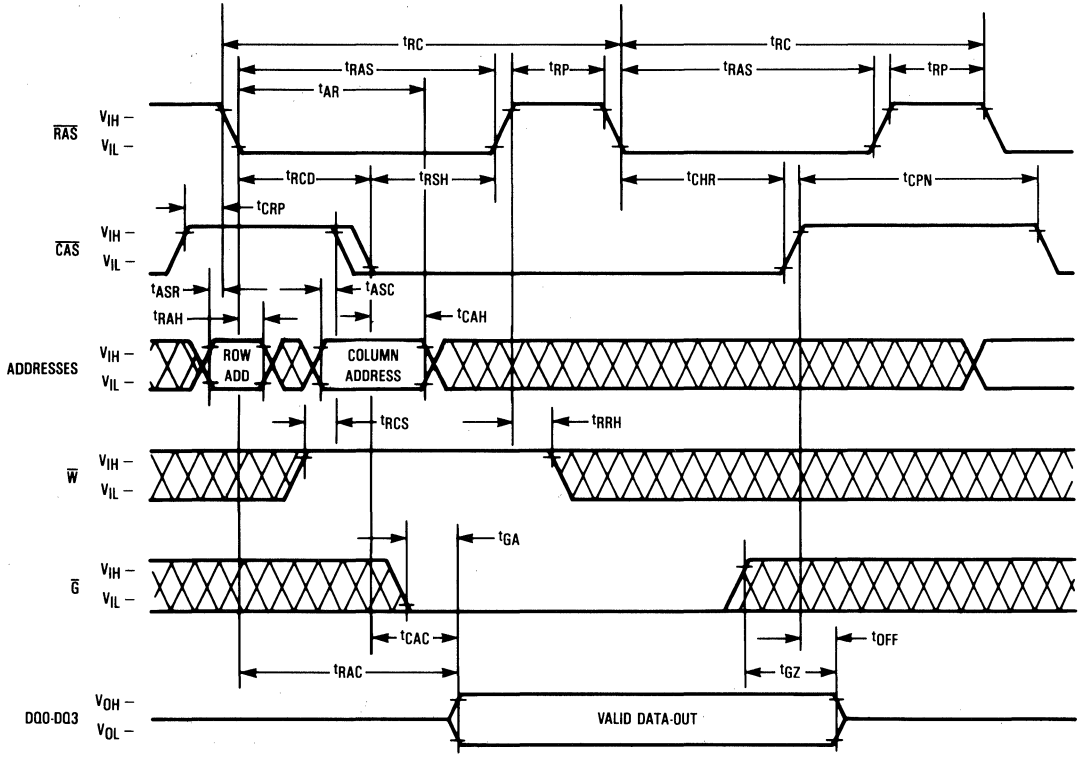
2

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

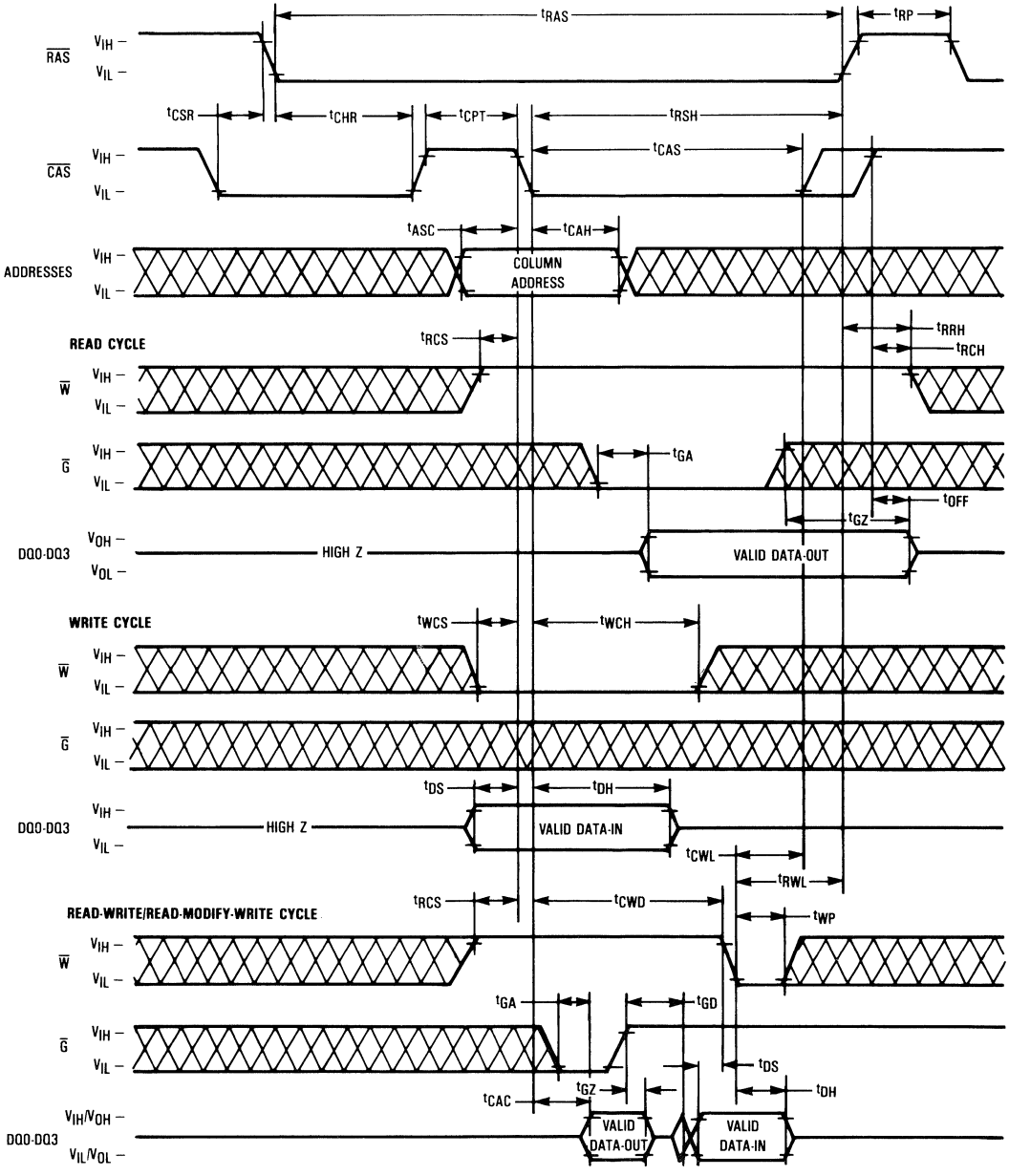
($\overline{W}$, $\overline{G}$, and A0-A7 are Don't Care)



HIDDEN REFRESH CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of 16 address bits will decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, other variations in addressing the RAM, the refresh modes ($\overline{RAS}$ only refresh; $\overline{CAS}$ before $\overline{RAS}$ refresh; hidden refresh), another mode called page mode allows the user to column access the 256 bits within a selected row. The refresh mode and page mode operations are described in more detail later on.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ and $\overline{G}$ clocks are active; the output will switch to the three-state mode when either the $\overline{CAS}$ or $\overline{G}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

In a late write or a ready-modify-write cycle, $\overline{G}$ must be at the V_{IH} level to bring the output buffers to high impedance prior to data-in being valid.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE CYCLE

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at the 256 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 256K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 8-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write cycle, the conditions normal to that mode of operation will apply in the page mode also. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 milliseconds. This is accomplished by sequentially cycling through the 256 row address locations every 4 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will serve to refresh all the bits associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 256 row addresses every 4 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MCM41464A offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh

An optional feature of the MCM41464A is that refresh cycle may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure 1 below)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM41464A can be tested by $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 256 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

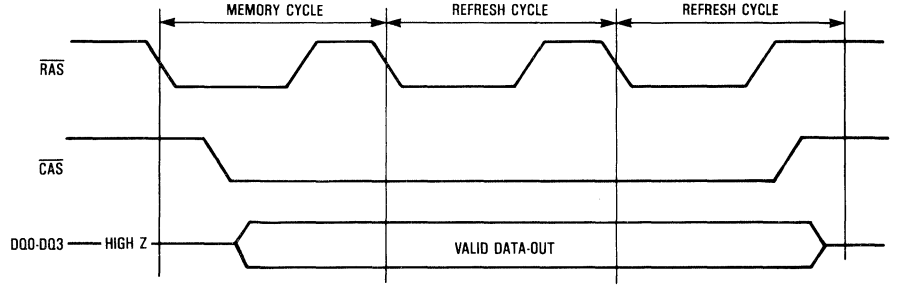
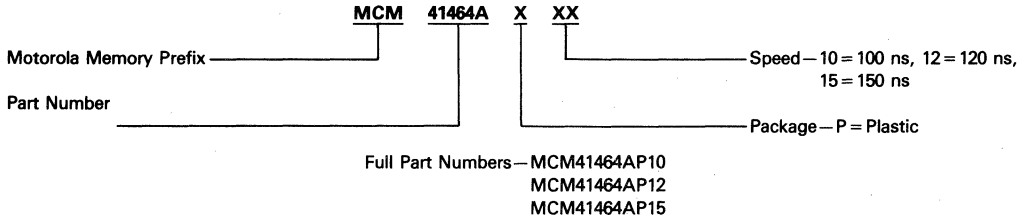


Figure 1. Hidden Refresh Cycle

2

ORDERING INFORMATION
(Order by Full Part Number)



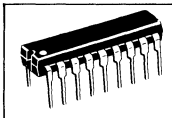
Full Part Numbers — MCM41464AP10
MCM41464AP12
MCM41464AP15

MCM511000

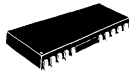
2

Advance Information

1M x 1 CMOS Dynamic RAM



P PACKAGE
PLASTIC
CASE 707A



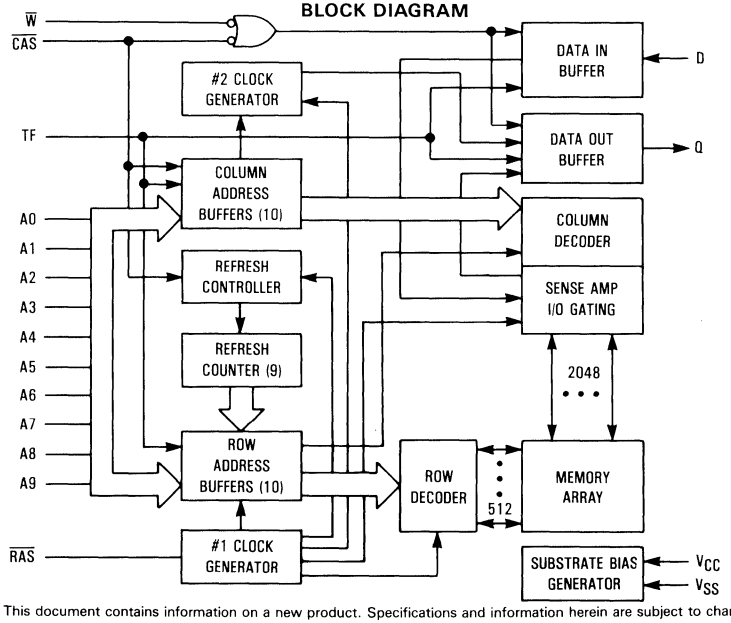
J PACKAGE
SMALL OUTLINE
CASE 822

The MCM511000 is a 1.2μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

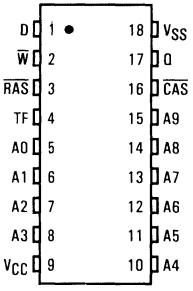
The MCM511000 requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in standard 300 mil wide packages: dual-in-line package (DIP) and J-lead small outline package.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- Test Mode Capability
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM511000-85 = 85 ns (Maximum)
  MCM511000-10 = 100 ns (Maximum)
  MCM511000-12 = 120 ns (Maximum)
- Low Active Power Dissipation: MCM511000-85 = 385 mW (Maximum)
  MCM511000-10 = 330 mW (Maximum)
  MCM511000-12 = 275 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)

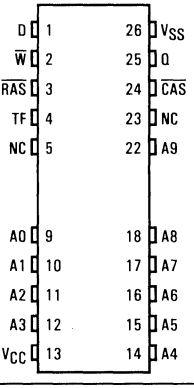
BLOCK DIAGRAM



PIN ASSIGNMENT
DUAL-IN-LINE



SMALL OUTLINE



PIN NAMES	
A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1
Test Function Input High Voltage	$V_{IH\ (TF)}$	V_{CC} + 4.5	—	10.5	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511000-85, t_{RC} = 165 ns		—	70		
MCM511000-10, t_{RC} = 190 ns		—	60		
MCM511000-12, t_{RC} = 220 ns		—	50		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS} = V_{IH}$)	I_{CC3}			mA	2
MCM511000-85, t_{RC} = 165 ns		—	70		
MCM511000-10, t_{RC} = 190 ns		—	60		
MCM511000-12, t_{RC} = 220 ns		—	50		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS} = V_{IL}$)	I_{CC4}			mA	2
MCM511000-85, t_{PC} = 50 ns		—	50		
MCM511000-10, t_{PC} = 55 ns		—	40		
MCM511000-12, t_{PC} = 70 ns		—	30		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511000-85, t_{RC} = 165 ns		—	70		
MCM511000-10, t_{RC} = 190 ns		—	60		
MCM511000-12, t_{RC} = 220 ns		—	50		
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Input Leakage Current (TF) (0 V ≤ $V_{in(TF)}$ ≤ 0.8 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS} = V_{IH}$, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Test Function Input Current (V_{CC} + 4.5 V ≤ $V_{in(TF)}$ ≤ 10.5 V)	$I_{in(TF)}$	—	1	mA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	pF	3
Output Capacitance ($\overline{CAS} = V_{IH}$ to Disable Output)	Q	C_{out}	7	pF	3

NOTES: 1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511000-85		MCM511000-10		MCM511000-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	165	—	190	—	220	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	190	—	220	—	255	—	ns	6
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	—	55	—	70	—	ns	
Page Mode Read-Write Cycle Time	t_{CELCEL}	t_{PRWC}	75	—	85	—	105	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	85	—	100	—	120	ns	7, 8
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	25	—	25	—	30	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	—	45	—	50	—	60	ns	7, 10
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	45	—	50	—	65	ns	7
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	5	—	5	—	5	—	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	30	0	30	0	35	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	85	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	85	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	60	25	75	25	90	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	15	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	15	—	15	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	—	20	—	25	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	65	—	75	—	90	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	45	—	50	—	60	—	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

2

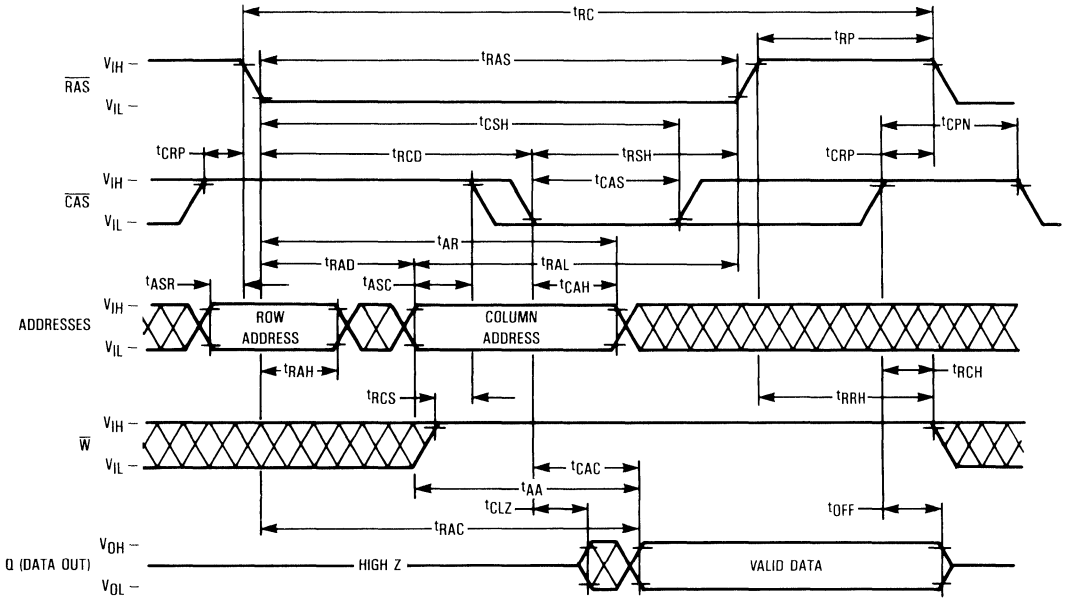
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511000-85		MCM511000-10		MCM511000-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	20	–	20	–	25	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	65	–	75	–	90	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	20	–	20	–	25	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	25	–	30	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	25	–	30	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{CELDX}	t_{DH}	20	–	20	–	25	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	65	–	75	–	90	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	16
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	25	–	25	–	30	–	ns	16
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	85	–	100	–	120	–	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	45	–	50	–	60	–	ns	16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{CAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	50	–	50	–	60	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	15	–	15	–	20	–	ns	
Test Mode Enable Setup Time Referenced to $\overline{RAS}$	t_{TEHREL}	t_{TES}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{RAS}$	t_{REHTEL}	t_{TEH}	0	–	0	–	0	–	ns	

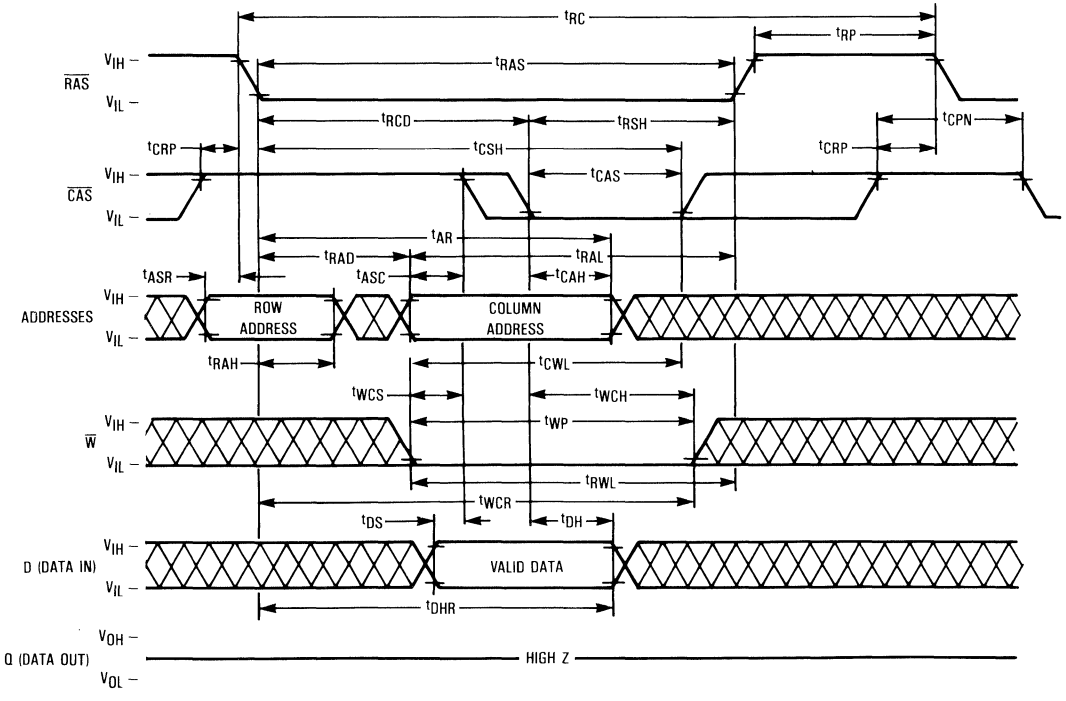
NOTES:

14. Enter t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



EARLY WRITE CYCLE



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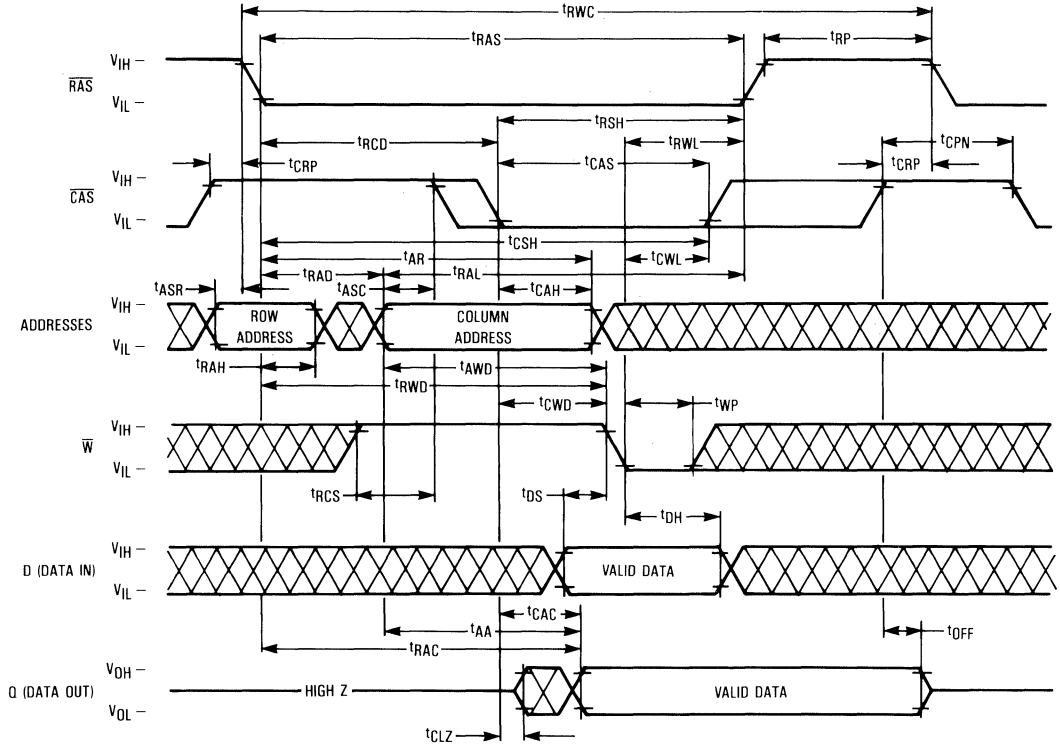
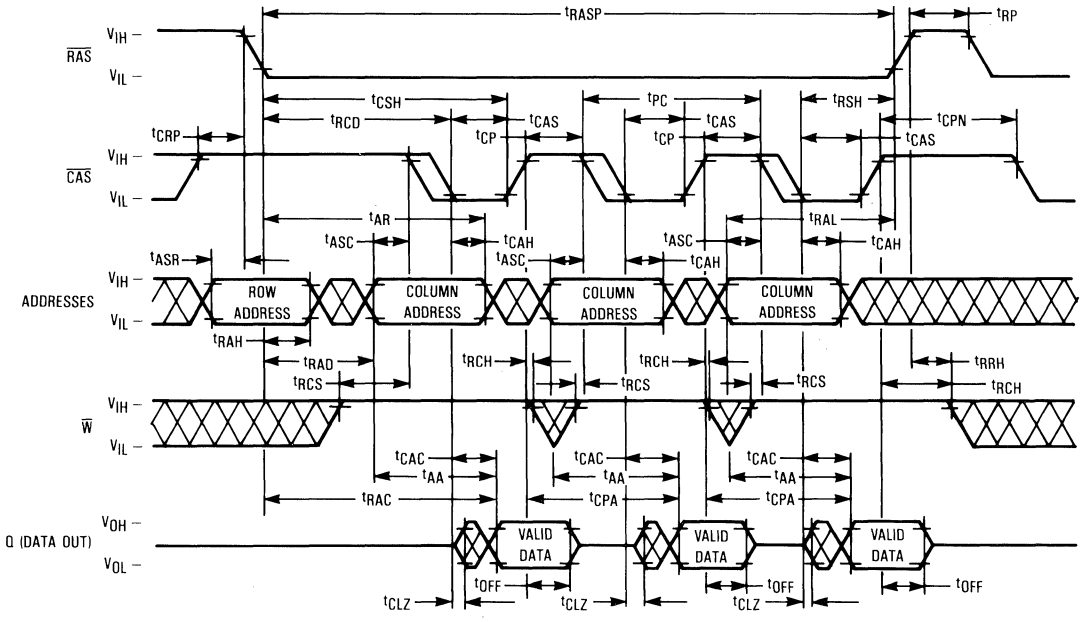
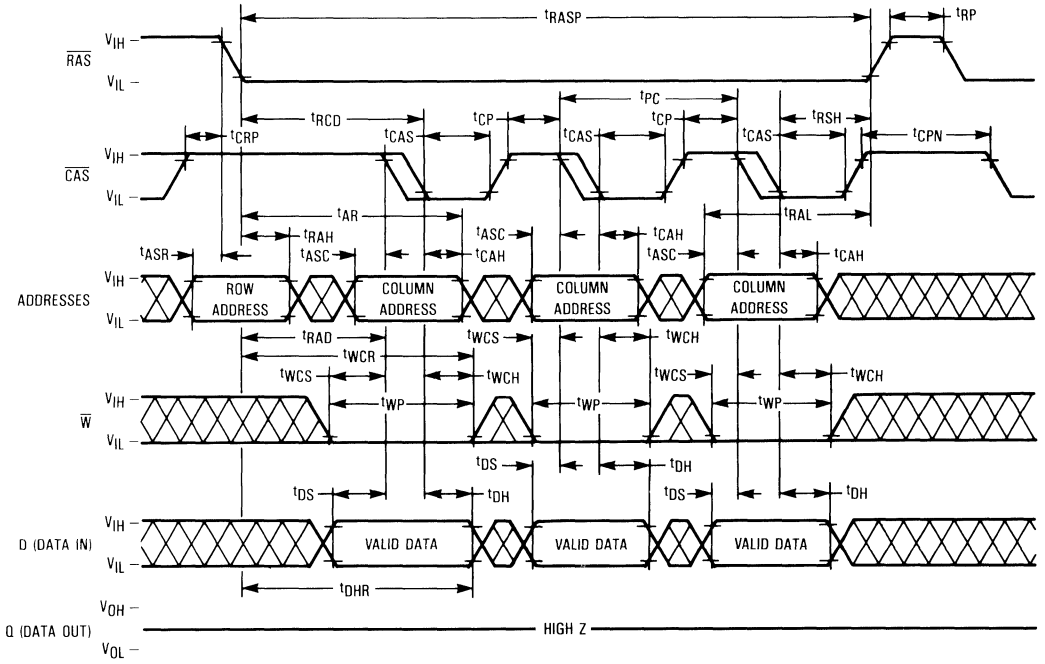
READ-WRITE CYCLE



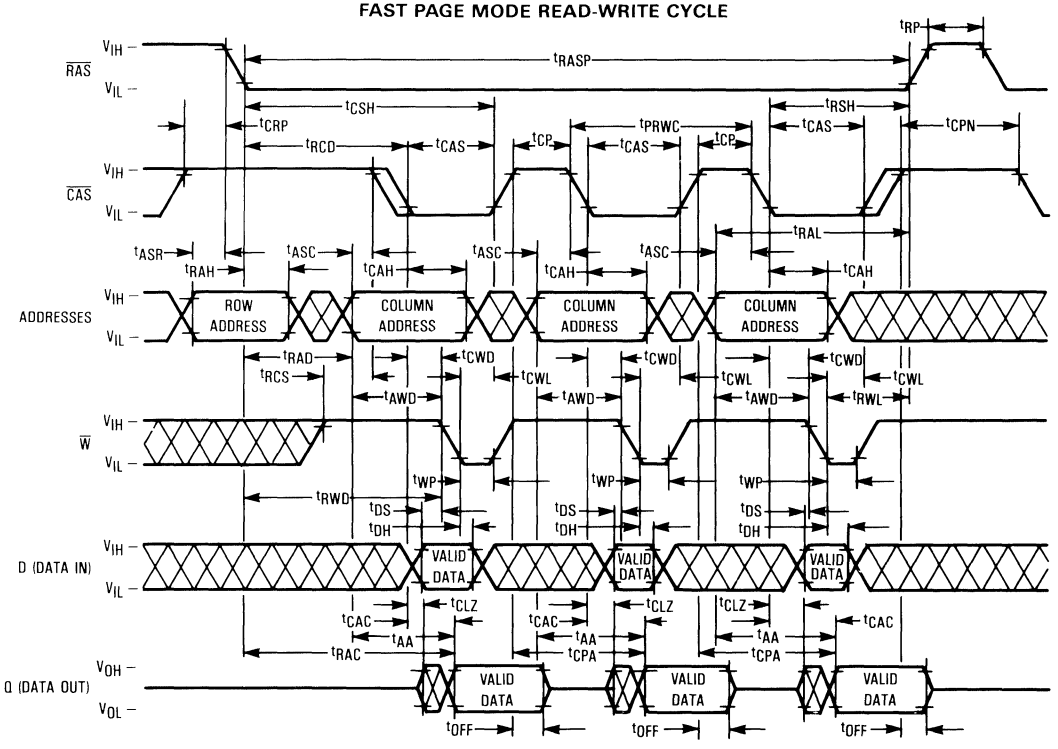
FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



FAST PAGE MODE READ-WRITE CYCLE



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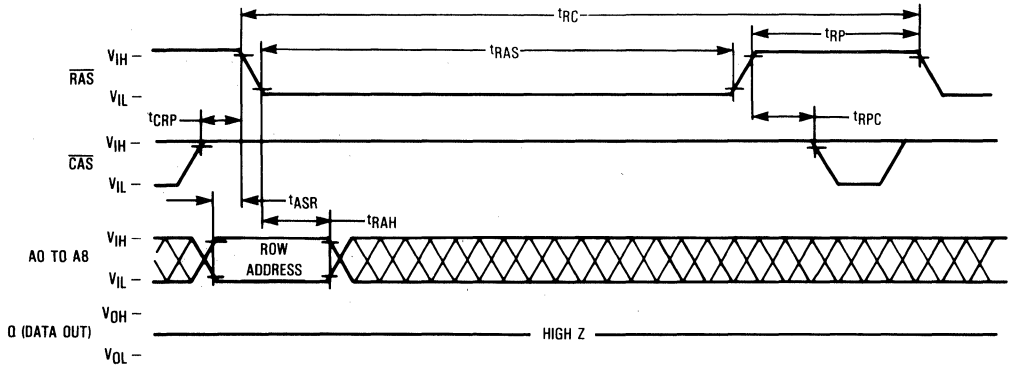
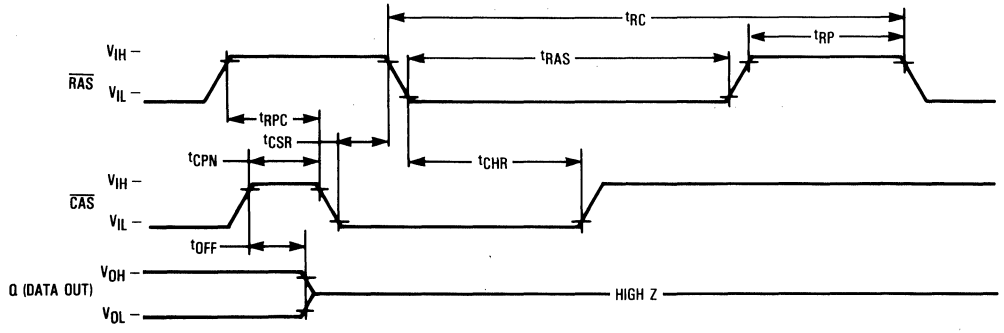
$\overline{RAS}$ ONLY REFRESH CYCLE

($\overline{W}$ and A9 are Don't Care)

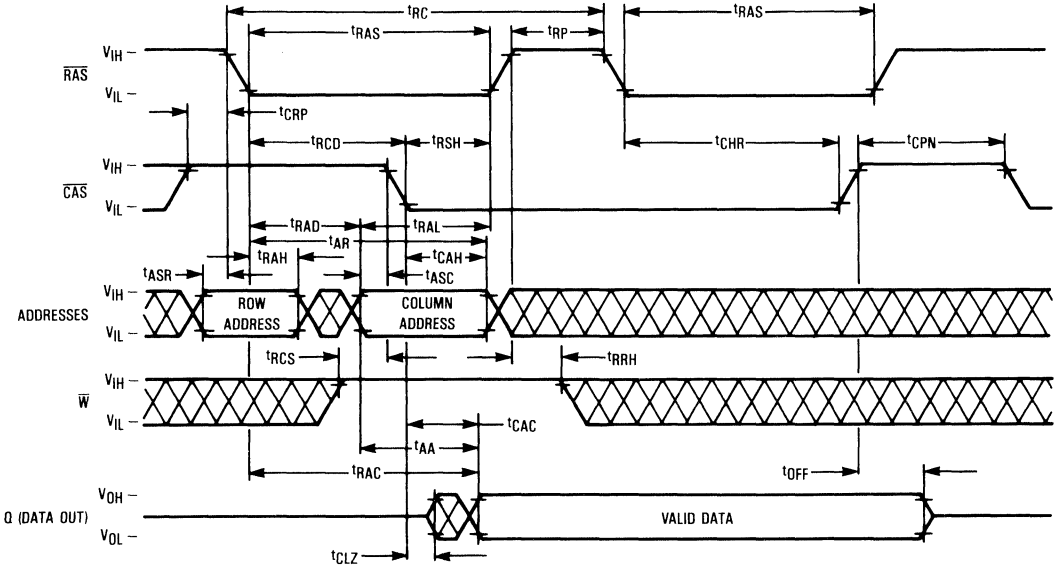


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

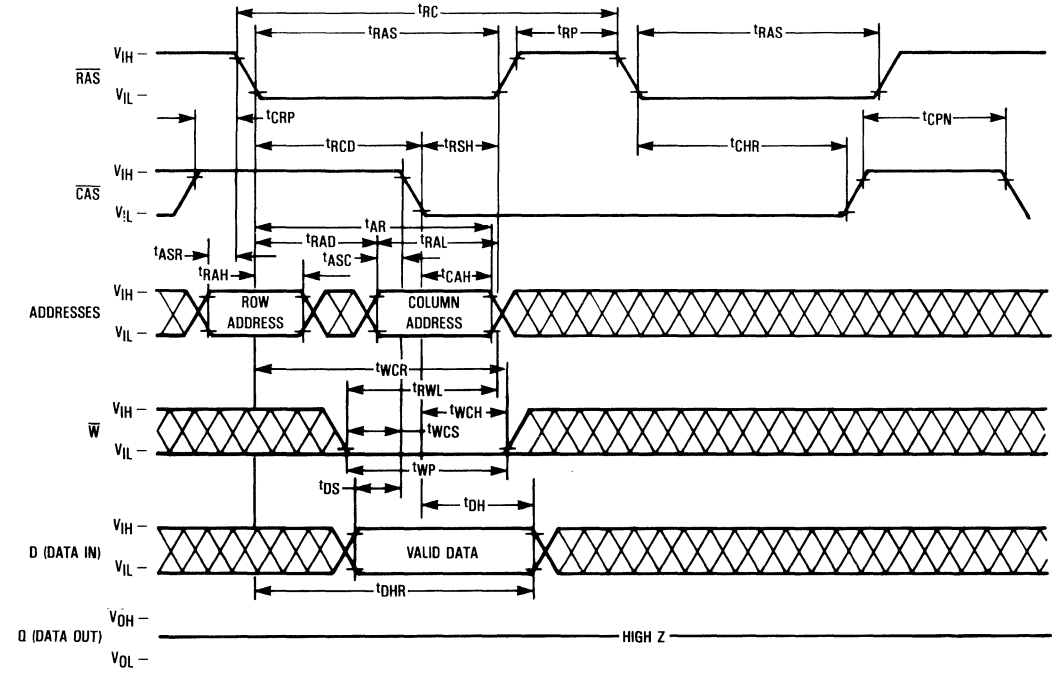
($\overline{W}$ and A0 to A9 are Don't Care)



HIDDEN REFRESH CYCLE (READ)

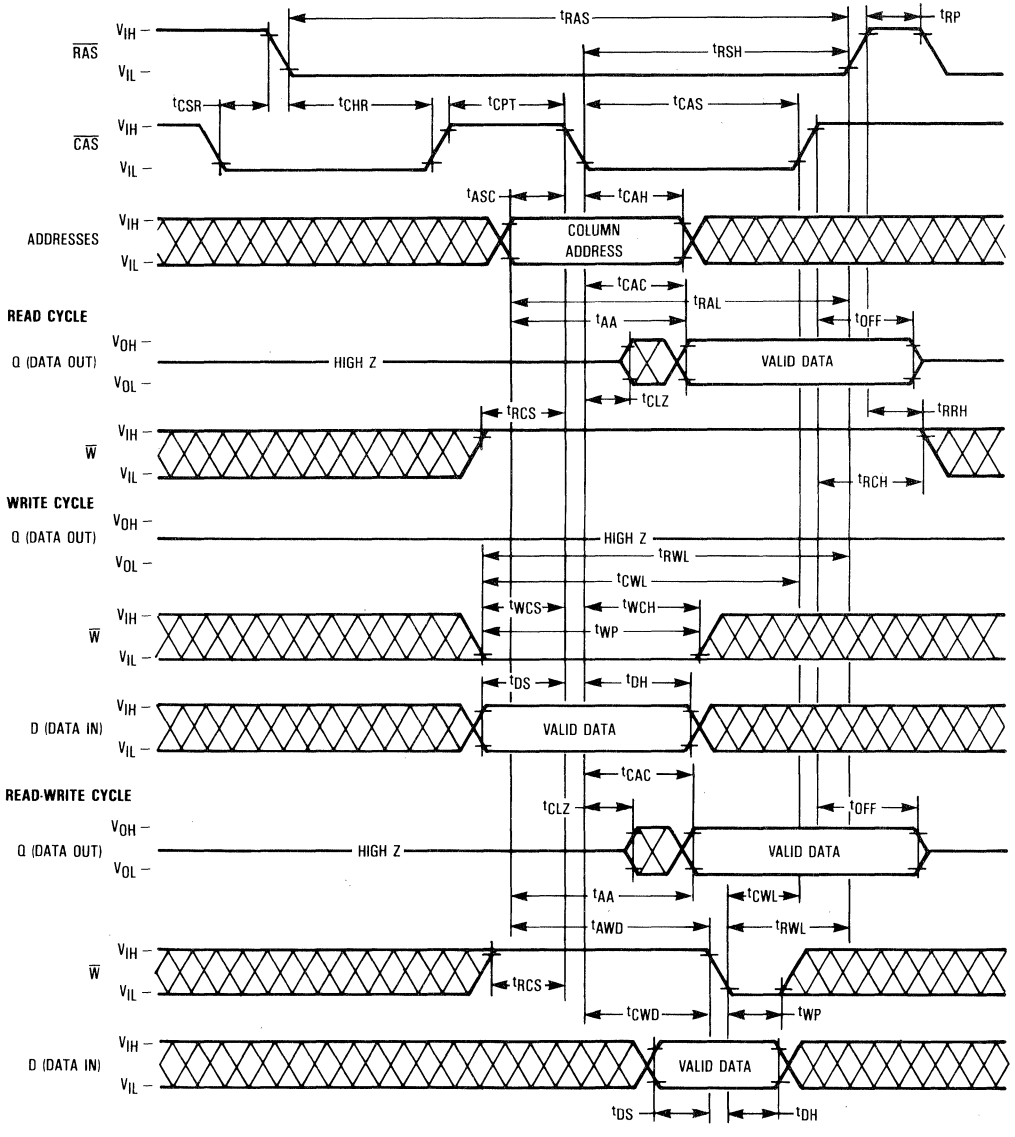


HIDDEN REFRESH CYCLE (WRITE)



2

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of twenty address bits will decode one of the 1,048,576 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 1M RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, which is called page mode, allows the user to column access the 2048 bits within a selected row. (See **PAGE-MODE CYCLES** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out

occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at the 1024 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 10-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will serve to refresh all the bits (2048) associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM511000 can be tested by $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

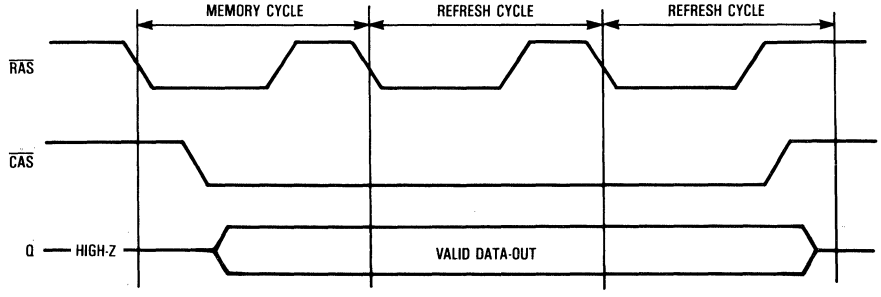


Figure 1. Hidden Refresh Cycle

TEST MODE

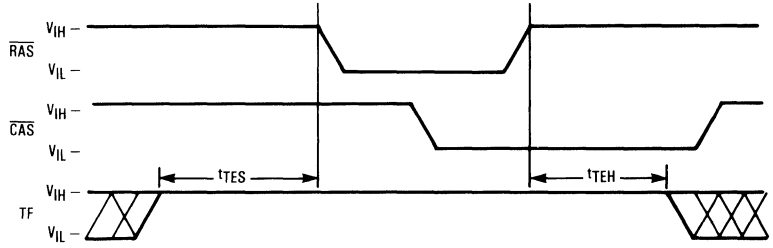
Internal organization of the device of 256K × 4 allows the device to be tested as if it were a 256K × 1 DRAM. In the test mode, data is written into 4 sectors in parallel and retrieved the same way. If all 4 bits are equal on a read, data out indicates the same data at all bits. If all 4 bits are not equal, the data out will indicate a high impedance state. See truth table and block diagram below.

The test mode function is performed on any of the timing cycles, including fast page mode, when the TF pin is held on "super voltage" (V_{CC} + 4.5 V), where (4.5 V ≤ V_{CC} ≤ 5.5 V), maximum voltage = 10.5 V, for the specified period (t_{TES}, t_{TEH}; see test mode cycle). A9 is ignored in the test mode. Normal operation requires the TF pin to either be connected to V_{IL}, or remain open.

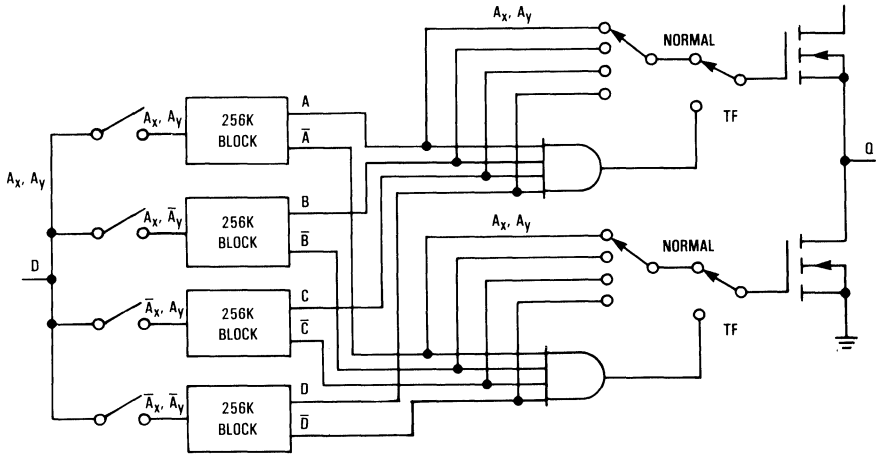
Test Mode Truth Table

A	B	C	D	Q
0	0	0	0	0
1	1	1	1	1
Any Other				High-Z

TEST MODE CYCLE

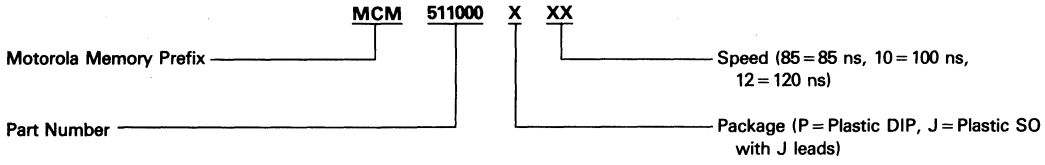


TEST FUNCTION BLOCK DIAGRAM



2

ORDERING INFORMATION
(Order by Full Part Number)



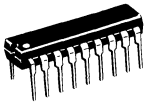
Full Part Numbers—	MCM511000P85	MCM511000J85
	MCM511000P10	MCM511000J10
	MCM511000P12	MCM511000J12

MCM511001

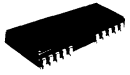
2

Advance Information

1M x 1 CMOS Dynamic RAM



P PACKAGE
PLASTIC
CASE 707A



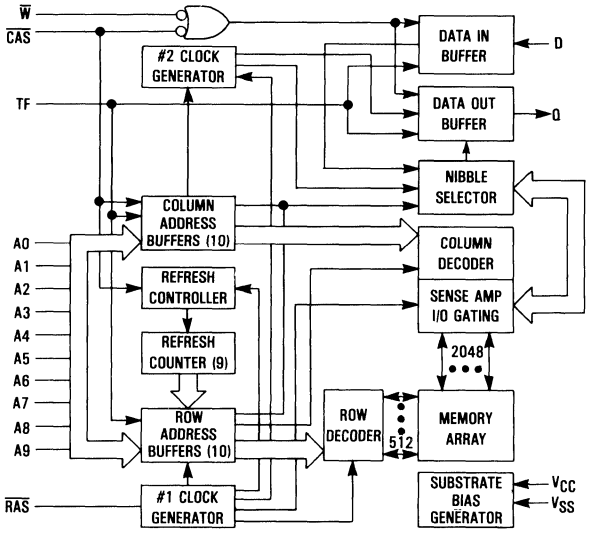
J PACKAGE
SMALL OUTLINE
CASE 822

The MCM511001 is a 1.2μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The fast nibble mode feature allows high-speed serial access of up to 4 bits of data.

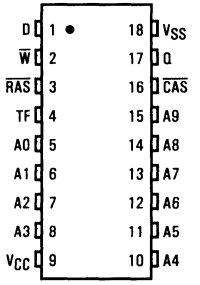
The MCM511001 requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in standard 300 mil wide packages: dual-in-line package (DIP) and J-lead small outline package.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Nibble Mode Capability
- Test Mode Capability
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM511001-85 = 85 ns (Maximum)
  MCM511001-10 = 100 ns (Maximum)
  MCM511001-12 = 120 ns (Maximum)
- Low Active Power Dissipation: MCM511001-85 = 385 mW (Maximum)
  MCM511001-10 = 330 mW (Maximum)
  MCM511001-12 = 275 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)

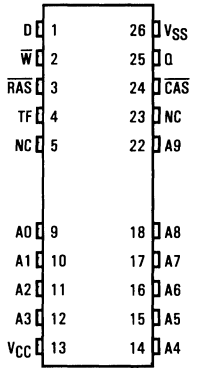
BLOCK DIAGRAM



PIN ASSIGNMENT
DUAL-IN-LINE



SMALL OUTLINE



PIN NAMES	
A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	–	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	–	0.8	V	1
Test Function Input High Voltage	$V_{IH(TF)}$	V_{CC}+4.5	–	10.5	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511001-85, t_{RC} = 165 ns		–	70		
MCM511001-10, t_{RC} = 190 ns		–	60		
MCM511001-12, t_{RC} = 220 ns		–	50		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	–	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS} = V_{IH}$)	I_{CC3}			mA	2
MCM511001-85, t_{RC} = 165 ns		–	70		
MCM511001-10, t_{RC} = 190 ns		–	60		
MCM511001-12, t_{RC} = 220 ns		–	50		
V_{CC} Power Supply Current During Nibble Mode Cycle ($\overline{RAS} = V_{IL}$)	I_{CC4}			mA	2
MCM511001-85, t_{NC} = 40 ns		–	50		
MCM511001-10, t_{NC} = 40 ns		–	40		
MCM511001-12, t_{NC} = 50 ns		–	30		
V_{CC} Power Supply Current (Standby) ($\overline{RAS} = \overline{CAS} = V_{CC}$ − 0.2 V)	I_{CC5}	–	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511001-85, t_{RC} = 165 ns		–	70		
MCM511001-10, t_{RC} = 190 ns		–	60		
MCM511001-12, t_{RC} = 220 ns		–	50		
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Input Leakage Current (TF) (0 V ≤ $V_{in(TF)}$ ≤ 0.8 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS} = V_{IH}$, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Test Function Input Current (V_{CC} + 4.5 V ≤ $V_{in(TF)}$ ≤ 10.5 V)	$I_{in(TF)}$	–	1	mA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	–	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	–	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, TF		7	pF	3
Output Capacitance ($\overline{CAS} = V_{IH}$ to Disable Output)	Q	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511001-85		MCM511001-10		MCM511001-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	165	—	190	—	220	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	190	—	220	—	255	—	ns	6
Nibble Mode Cycle Time	t_{CEHCEH}	t_{NC}	40	—	40	—	50	—	ns	
Nibble Mode Read-Write Cycle Time	t_{CEHCEH}	t_{NRMW}	65	—	65	—	80	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	85	—	100	—	120	ns	7, 8
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	30	—	35	—	40	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	—	45	—	50	—	60	ns	7, 10
Nibble Mode Access Time	t_{CELQV}	t_{NCAC}	—	20	—	20	—	25	ns	7
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	5	—	5	—	5	—	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	30	0	30	0	35	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	85	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	30	—	35	—	40	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	30	10,000	35	10,000	40	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	55	25	65	25	80	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	20	40	20	50	20	60	ns	13
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	15	—	15	—	20	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	15	—	15	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	—	20	—	25	—	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	65	—	75	—	90	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	45	—	50	—	60	—	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

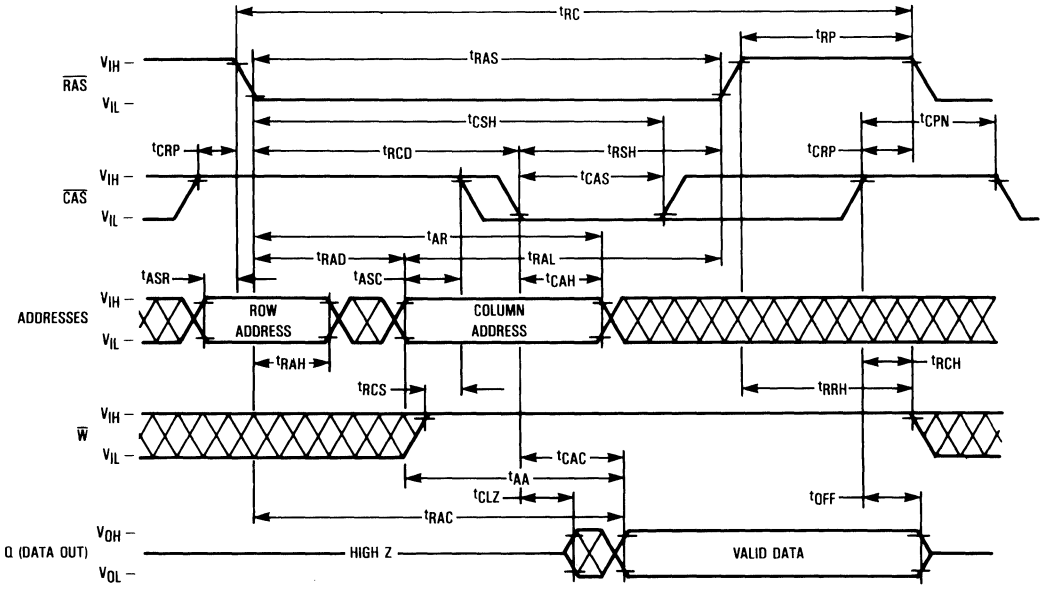
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511001-85		MCM511001-10		MCM511001-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	20	–	20	–	25	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	65	–	75	–	90	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	20	–	20	–	25	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	25	–	30	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	25	–	30	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{CELDX}	t_{DH}	20	–	20	–	25	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	65	–	75	–	90	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	16
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	30	–	35	–	45	–	ns	16
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	85	–	100	–	120	–	ns	16
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	45	–	50	–	60	–	ns	16
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	50	–	50	–	60	–	ns	
Nibble Mode Pulse Width	t_{CELCEH}	t_{NCAS}	20	–	20	–	25	–	ns	
Nibble Mode $\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{NCP}	10	–	10	–	15	–	ns	
Nibble Mode $\overline{RAS}$ Hold Time	t_{CELREH}	t_{NRSH}	20	–	20	–	25	–	ns	
Nibble Mode $\overline{CAS}$ to Write Delay Time	t_{CELWL}	t_{NCWD}	20	–	20	–	25	–	ns	
Nibble Mode Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{NRWL}	20	–	20	–	25	–	ns	
Nibble Mode Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{NCWL}	20	–	20	–	25	–	ns	
Test Mode Enable Setup Time Referenced to $\overline{RAS}$	t_{TEHREL}	t_{TES}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{RAS}$	t_{REHTEL}	t_{TEH}	0	–	0	–	0	–	ns	

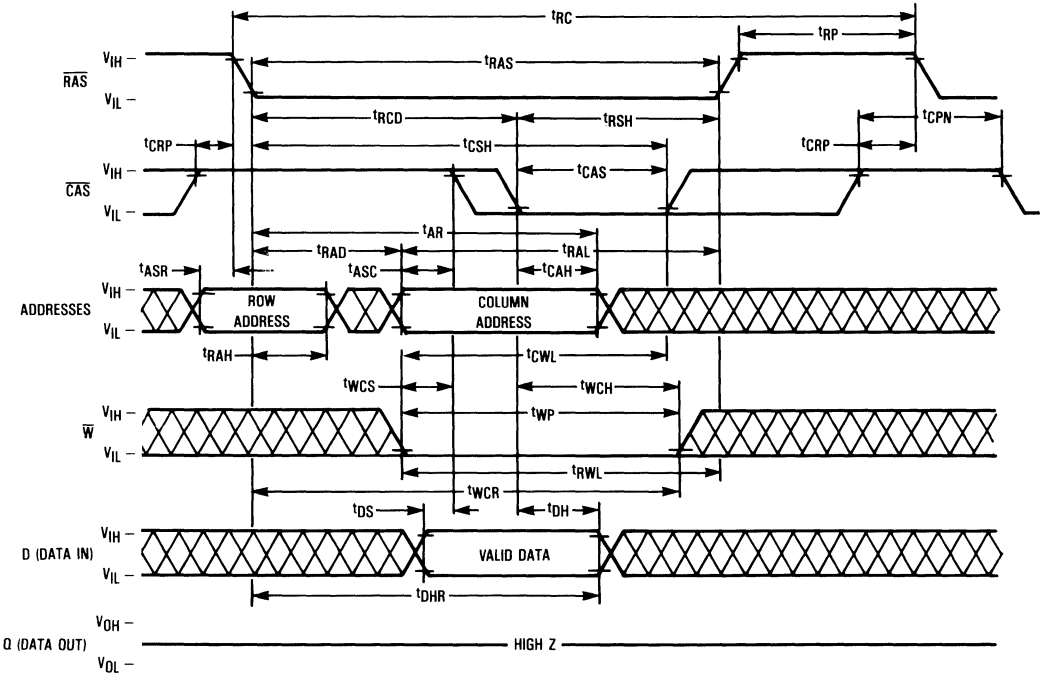
NOTES:

14. Enter t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE

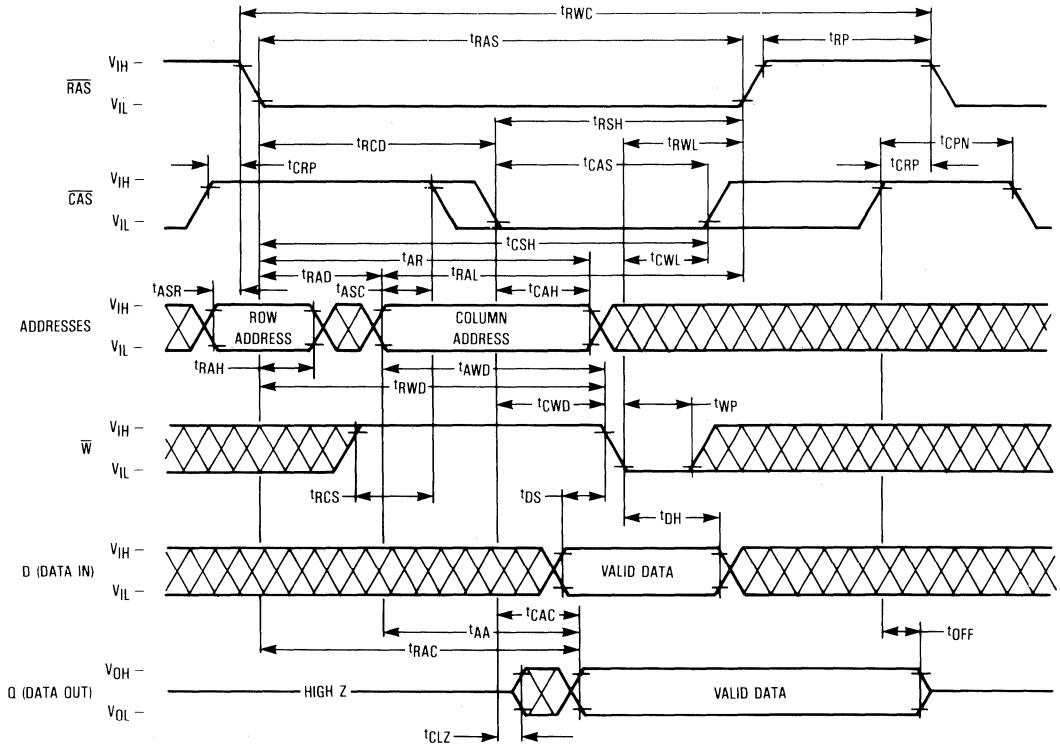


EARLY WRITE CYCLE

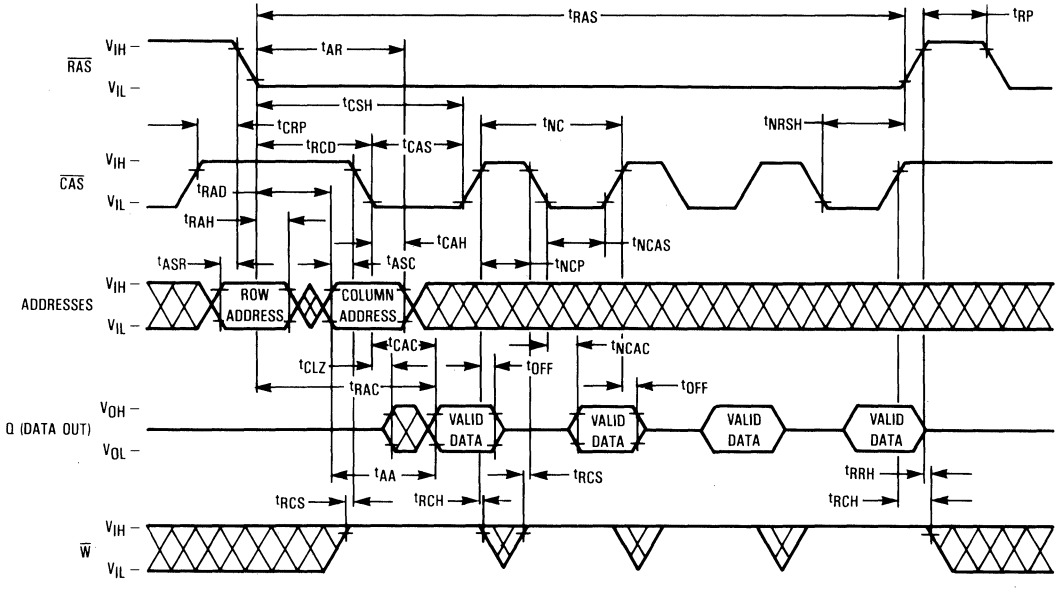


2

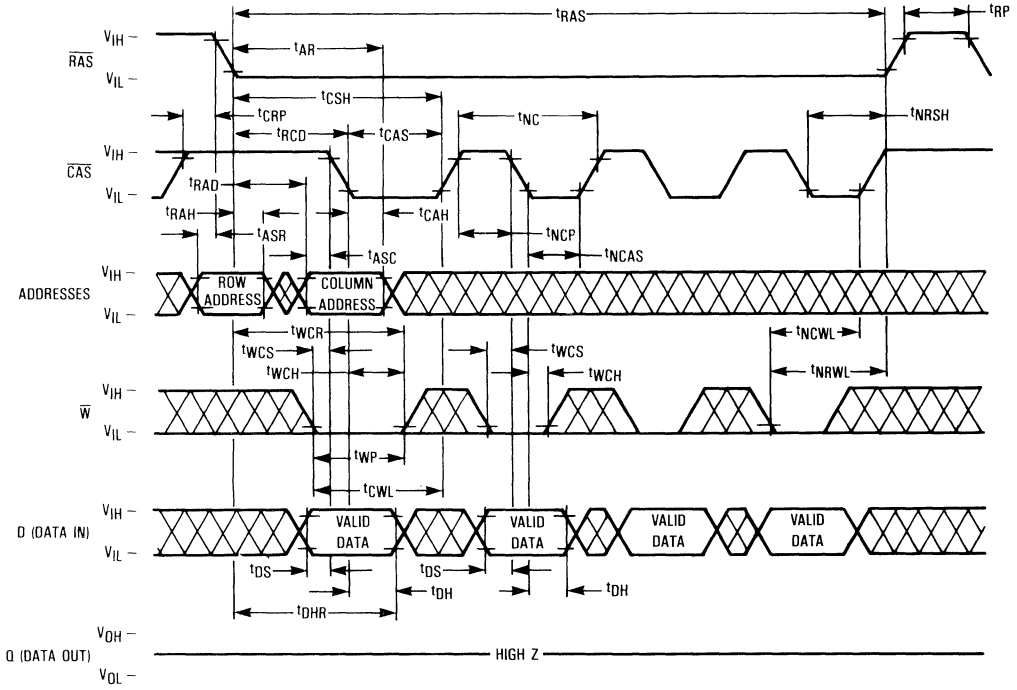
READ-WRITE CYCLE



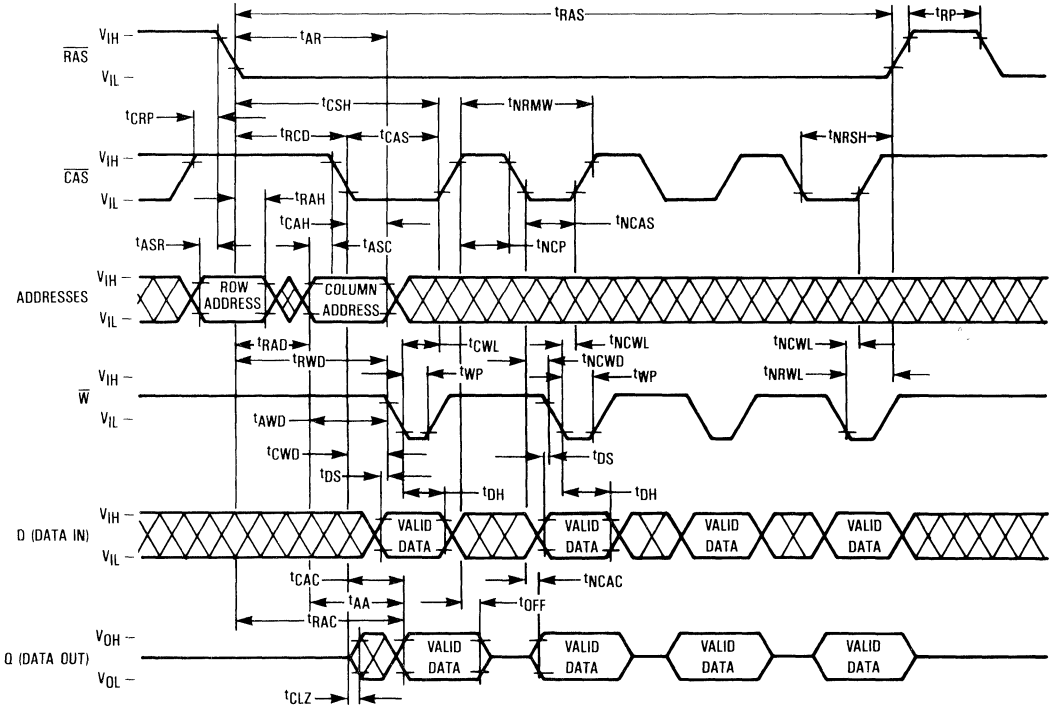
NIBBLE MODE READ CYCLE



NIBBLE MODE WRITE CYCLE (EARLY WRITE)



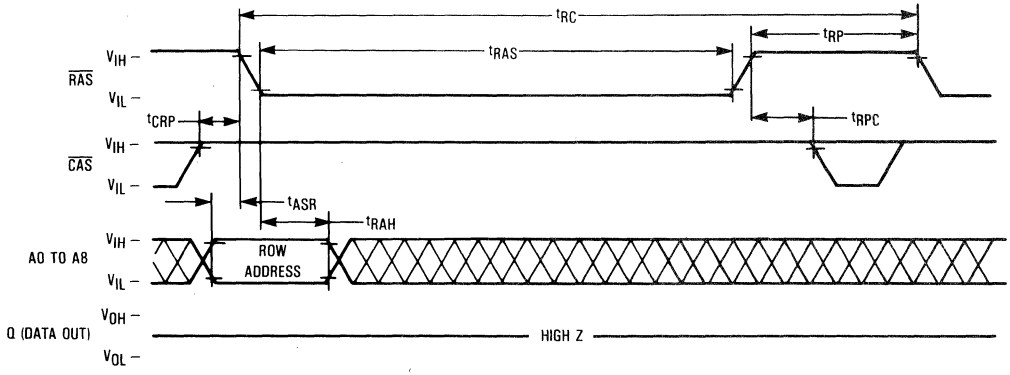
NIBBLE MODE READ-WRITE CYCLE



2

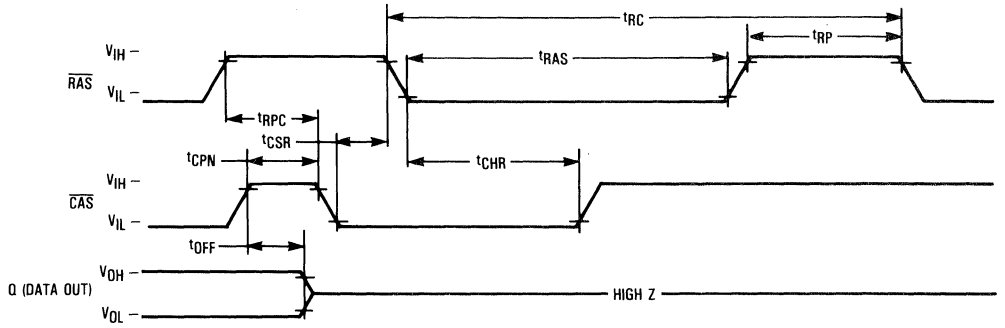
$\overline{RAS}$ ONLY REFRESH CYCLE

($\overline{W}$ and A9 are Don't Care)

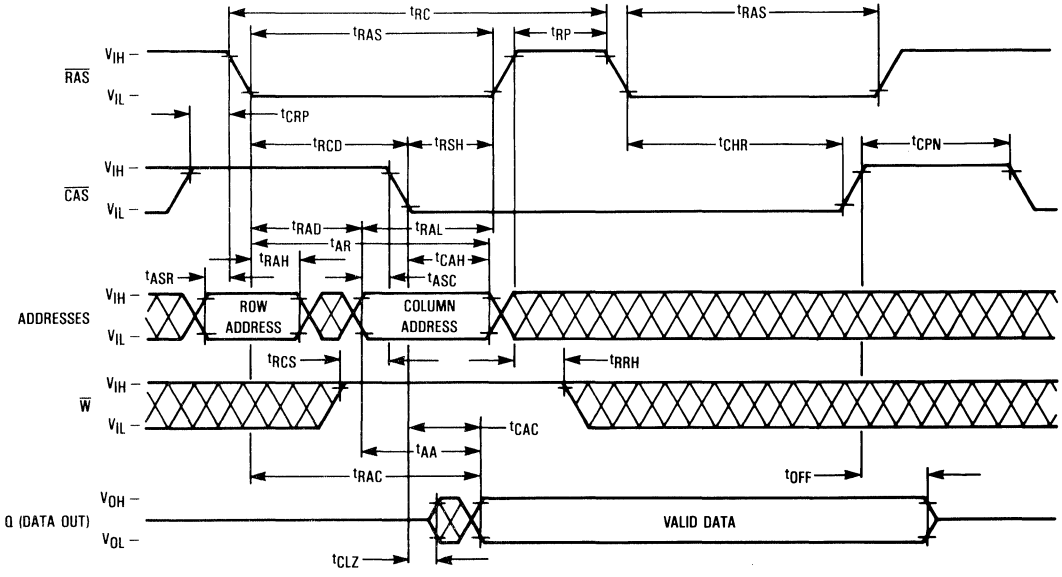


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

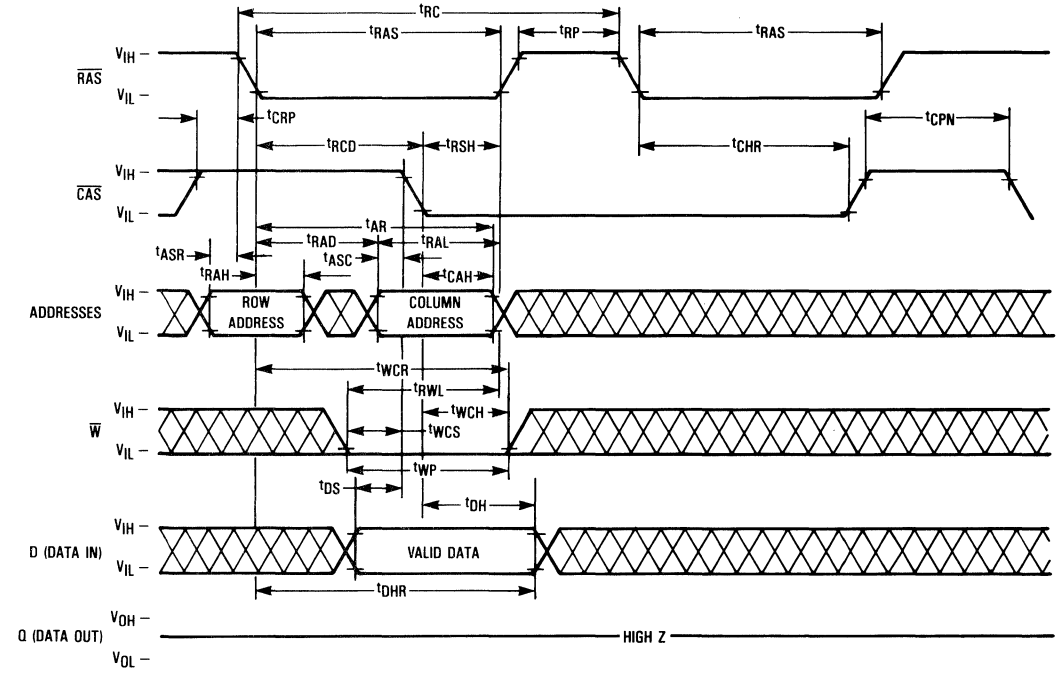
($\overline{W}$ and A0 to A9 are Don't Care)



HIDDEN REFRESH CYCLE (READ)

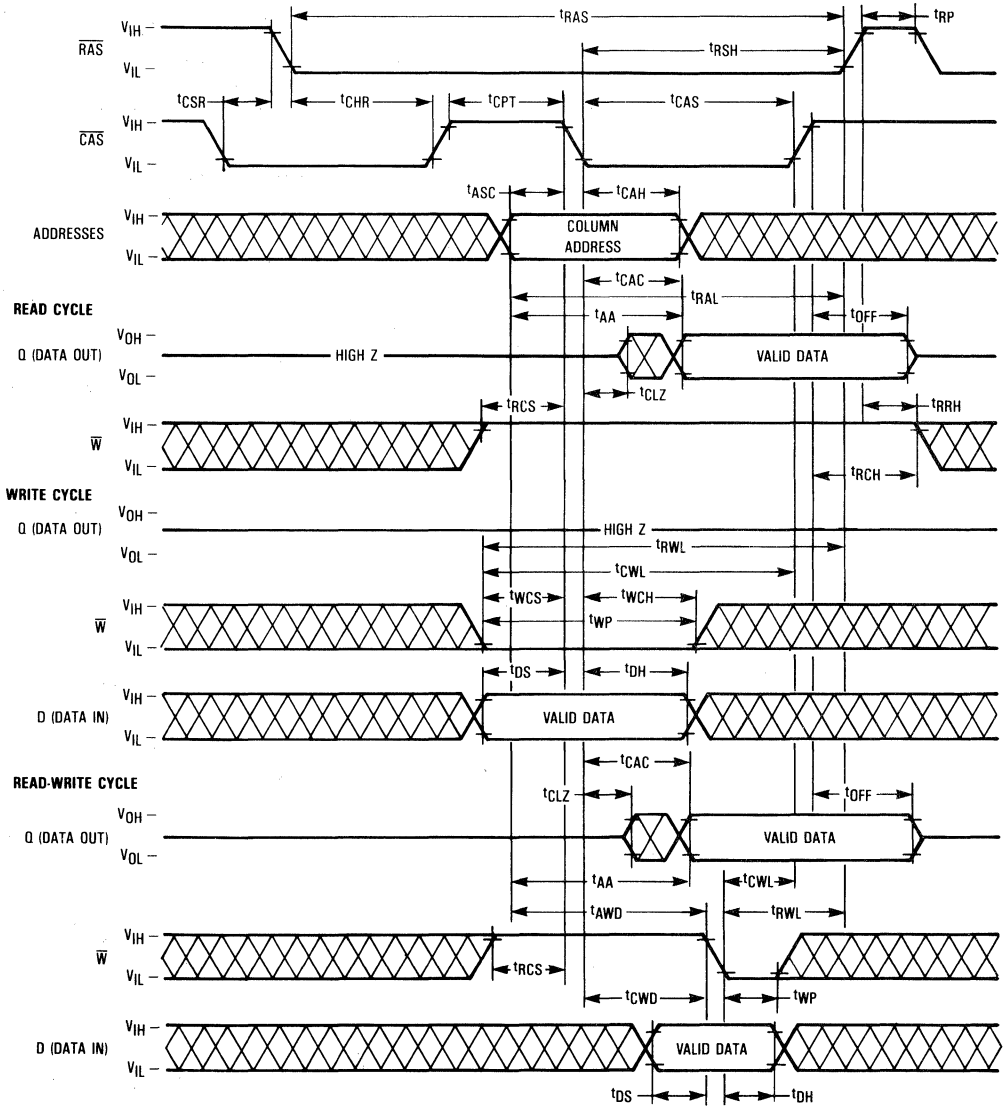


HIDDEN REFRESH CYCLE (WRITE)



2

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of twenty address bits will decode one of the 1,048,576 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 1M RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, which is called nibble mode, allows the user to access 4 bits serially. (See **NIBBLE MODE** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important

role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

NIBBLE MODE

Nibble mode allows high speed serial read, write, or read-modify-write access of 2, 3, or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 9 row addresses and the 9 column addresses. The 2 bits of addresses (CA9, RA9) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by the normal mode, the remaining nibble bits may be accessed by toggling $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA9 and CA9 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access.

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation is executed again on subsequent access, the new data will be written into the selected cell location.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will serve to refresh all the bits (2048) associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CAS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM511001 can be tested by $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

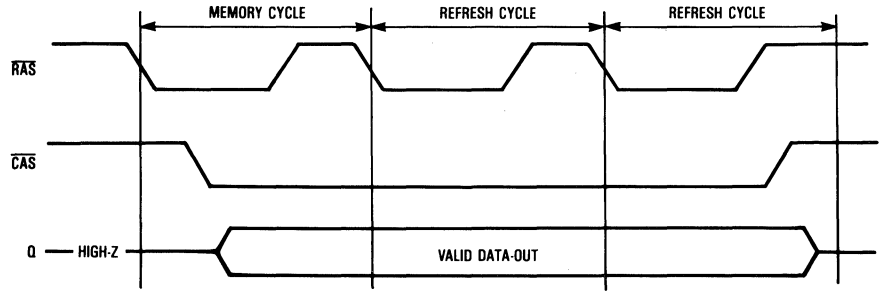


Figure 1. Hidden Refresh Cycle

TEST MODE

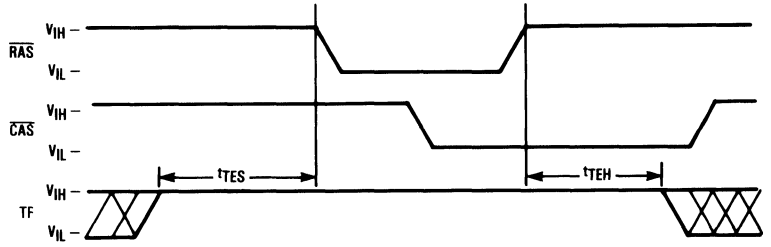
Internal organization of the device of 256K × 4 allows the device to be tested as if it were a 256K × 1 DRAM. In the test mode, data is written into 4 sectors in parallel and retrieved the same way. If all 4 bits are equal on a read, data out indicates the same data at all bits. If all 4 bits are not equal, the data out will indicate a high impedance state. See truth table and block diagram below.

The test mode function is performed on any of the timing cycles, including fast page mode, when the TF pin is held on "super voltage" (V_{CC} + 4.5 V), where (4.5 V ≤ V_{CC} ≤ 5.5 V), maximum voltage = 10.5 V, for the specified period (t_{TES}, t_{TEH}; see test mode cycle). A9 is ignored in the test mode. Normal operation requires the TF pin to either be connected to V_{IL}, or remain open.

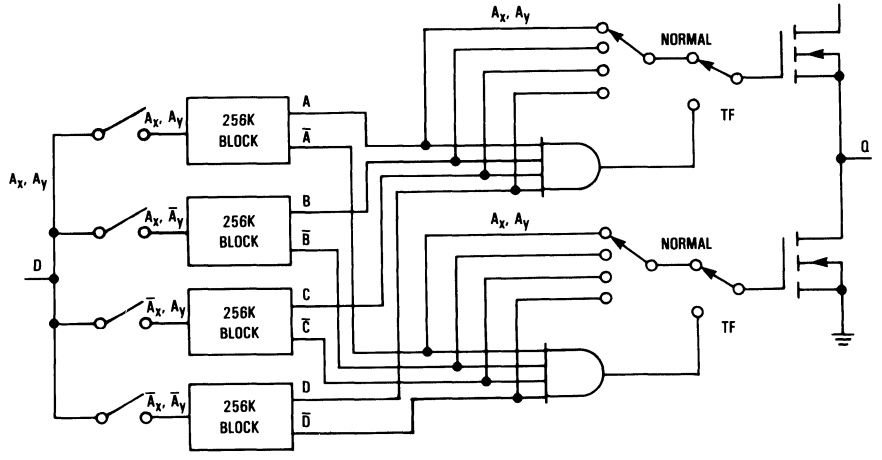
Test Mode Truth Table

A	B	C	D	Q
0	0	0	0	0
1	1	1	1	1
Any Other				High-Z

TEST MODE CYCLE

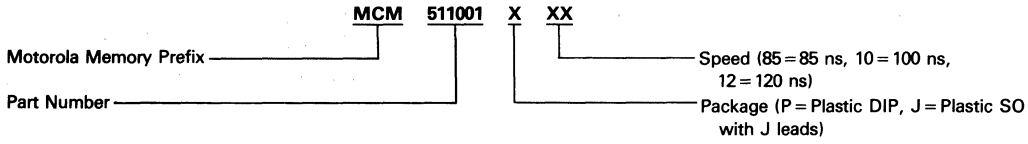


TEST FUNCTION BLOCK DIAGRAM



2

ORDERING INFORMATION
(Order by Full Part Number)



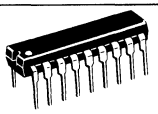
Full Part Numbers—		
	MCM511001P85	MCM511001J85
	MCM511001P10	MCM511001J10
	MCM511001P12	MCM511001J12

MCM511002

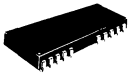
2

Advance Information

1M x 1 CMOS Dynamic RAM



P PACKAGE
PLASTIC
CASE 707A



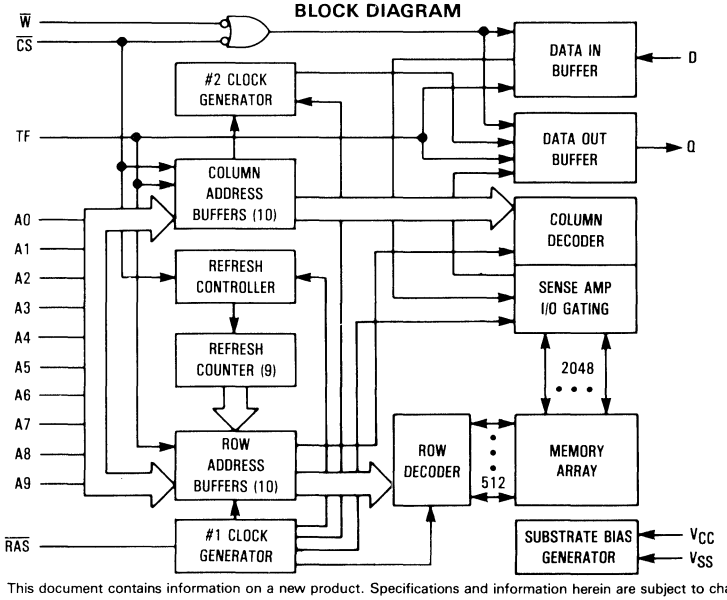
J PACKAGE
SMALL OUTLINE
CASE 822

The MCM511002 is a 1.2μ CMOS high-speed, dynamic random access memory. It is organized as 1,048,576 one-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost. The static column mode feature allows column data to be accessed upon the column address transition when $\overline{RAS}$ and $\overline{CS}$ are held low, similar to static RAM operation.

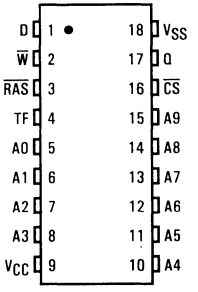
The MCM511002 requires only 10 address lines; row and column address inputs are multiplexed.

- Three-State Data Output
- Early-Write Common I/O Capability
- Static Column Mode Capability
- Test Mode Capability
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM511002-85 = 85 ns (Maximum)
  MCM511002-10 = 100 ns (Maximum)
  MCM511002-12 = 120 ns (Maximum)
- Low Active Power Dissipation: MCM511002-85 = 385 mW (Maximum)
  MCM511002-10 = 330 mW (Maximum)
  MCM511002-12 = 275 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)

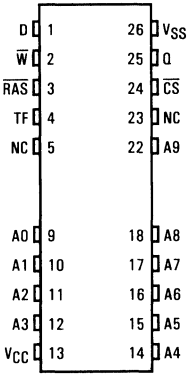
BLOCK DIAGRAM



PIN ASSIGNMENT
DUAL-IN-LINE



SMALL OUTLINE



PIN NAMES	
A0-A9	Address Input
D	Data Input
Q	Data Output
$\overline{W}$	Read/Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
V_{CC}	Power (+5 V)
V_{SS}	Ground
TF	Test Function Enable
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Test Function Input Voltage	$V_{in(TF)}$	−1 to +10.5	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1
Test Function Input High Voltage	$V_{IH\ (TF)}$	V_{CC}+4.5	—	10.5	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM511002-85, t_{RC} = 165 ns		—	70		
MCM511002-10, t_{RC} = 190 ns		—	60		
MCM511002-12, t_{RC} = 220 ns		—	50		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CS}$ = V_{IH})	I_{CC3}			mA	2
MCM511002-85, t_{RC} = 165 ns		—	70		
MCM511002-10, t_{RC} = 190 ns		—	60		
MCM511002-12, t_{RC} = 220 ns		—	50		
V_{CC} Power Supply Current During Static Column Mode Cycle ($\overline{RAS}$ = $\overline{CS}$ = V_{IL})	I_{CC4}			mA	2
MCM511002-85, t_{SC} = 50 ns		—	50		
MCM511002-10, t_{SC} = 55 ns		—	40		
MCM511002-12, t_{SC} = 70 ns		—	30		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} − 0.2 V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM511002-85, t_{RC} = 165 ns		—	70		
MCM511002-10, t_{RC} = 190 ns		—	60		
MCM511002-12, t_{RC} = 220 ns		—	50		
Input Leakage Current (Except TF) (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Input Leakage Current (TF) (0 V ≤ $V_{in(TF)}$ ≤ 0.8 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Test Function Input Current (V_{CC} + 4.5 V ≤ $V_{in(TF)}$ ≤ 10.5 V)	$I_{in(TF)}$	—	1	mA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A9, D	C_{in}	5	pF	3
	$\overline{RAS}$, $\overline{CS}$, $\overline{W}$, TF		7	pF	3
Output Capacitance ($\overline{CS}$ = V_{IH} to Disable Output)	Q	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM511002-85		MCM511002-10		MCM511002-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	165	—	190	—	220	—	ns	6
Read-Write Cycle Time	t_{RELREL}	t_{RWC}	190	—	220	—	255	—	ns	6
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	50	—	55	—	65	—	ns	
Static Column Mode Read-Write Cycle Time	t_{AVAV}	t_{SRWC}	90	—	100	—	120	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	85	—	100	—	120	ns	7, 8
Access Time from $\overline{CS}$	t_{CELQV}	t_{CAC}	—	25	—	25	—	30	ns	7, 9
Access Time from Column Address	t_{AVQV}	t_{AA}	—	45	—	50	—	60	ns	7, 10
Access Time from Last Write	t_{WLQV}	t_{ALW}	—	85	—	95	—	115	ns	7, 11
$\overline{CS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	5	—	5	—	5	—	ns	7
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	30	0	30	0	35	ns	12
Data Out Hold from Address Change	t_{AXQX}	t_{AOH}	5	—	5	—	5	—	ns	
Data Out Enable from Write	t_{WHQV}	t_{OW}	—	30	—	30	—	35	ns	
Data Out Hold from Write	t_{WHQX}	t_{WOH}	0	—	0	—	0	—	ns	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	70	—	80	—	90	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	85	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	85	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	25	—	25	—	30	—	ns	
$\overline{CS}$ Hold Time	t_{RELCEH}	t_{CSH}	85	—	100	—	120	—	ns	
$\overline{CS}$ Pulse Width	t_{CELCEH}	t_{CS}	25	10,000	25	10,000	30	10,000	ns	
$\overline{CS}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	25	100,000	25	100,000	30	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	60	25	75	25	90	ns	13
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	20	40	20	50	20	60	ns	14
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	—	10	—	10	—	ns	
$\overline{CS}$ Precharge Time (Static Column Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	15	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	15	—	15	—	15	—	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. TF pin must be at V_{IL} or open if not used.
6. The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
7. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max), and/or $t_{LWAD} \geq t_{LWAD}$ (max).
11. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max).
12. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

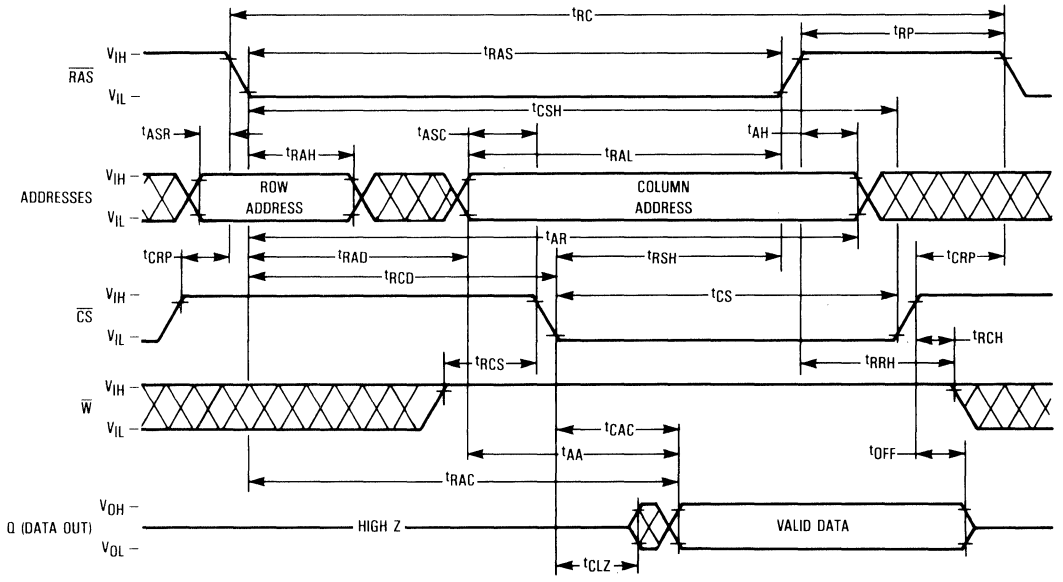
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM511002-85		MCM511002-10		MCM511002-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	–	20	–	25	–	ns	
Write Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AWR}	65	–	75	–	90	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	100	–	115	–	140	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	45	–	50	–	60	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$ High	t_{REHAX}	t_{AH}	10	–	10	–	15	–	ns	15
Write Command to $\overline{CS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	25	–	30	–	ns	
Last Write to Column Address Delay Time	t_{WLAV}	t_{LWAD}	25	40	25	45	30	55	ns	16
Last Write to Column Address Hold Time	t_{WLAX}	t_{AHLW}	85	–	95	–	115	–	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	17
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	17
Write Hold Time	t_{CELWH}	t_{WH}	0	–	0	–	0	–	ns	18
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	65	–	75	–	90	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	20	–	20	–	25	–	ns	
Write Command Inactive Time	t_{WHWL}	t_{WI}	10	–	10	–	15	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	25	–	30	–	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	19
Data In Hold Time	t_{CELDX}	t_{DH}	20	–	20	–	25	–	ns	19
Data In Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	65	–	75	–	90	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time (Output Data Disable)	t_{WLCEL}	t_{WS}	0	–	0	–	0	–	ns	18
$\overline{CS}$ to Write Delay	t_{CELWL}	t_{CWD}	25	–	25	–	30	–	ns	18
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	85	–	100	–	120	–	ns	18
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	45	–	50	–	60	–	ns	18
$\overline{CS}$ Setup Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CS}$ Hold Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{CS}$ Precharge to $\overline{CS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CS}$ Precharge Time for $\overline{CS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	50	–	50	–	60	–	ns	
$\overline{CS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	15	–	15	–	20	–	ns	
Test Mode Enable Setup Time Referenced to $\overline{RAS}$	t_{TEHREL}	t_{TES}	0	–	0	–	0	–	ns	
Test Mode Enable Hold Time Referenced to $\overline{RAS}$	t_{REHTEL}	t_{TEH}	0	–	0	–	0	–	ns	

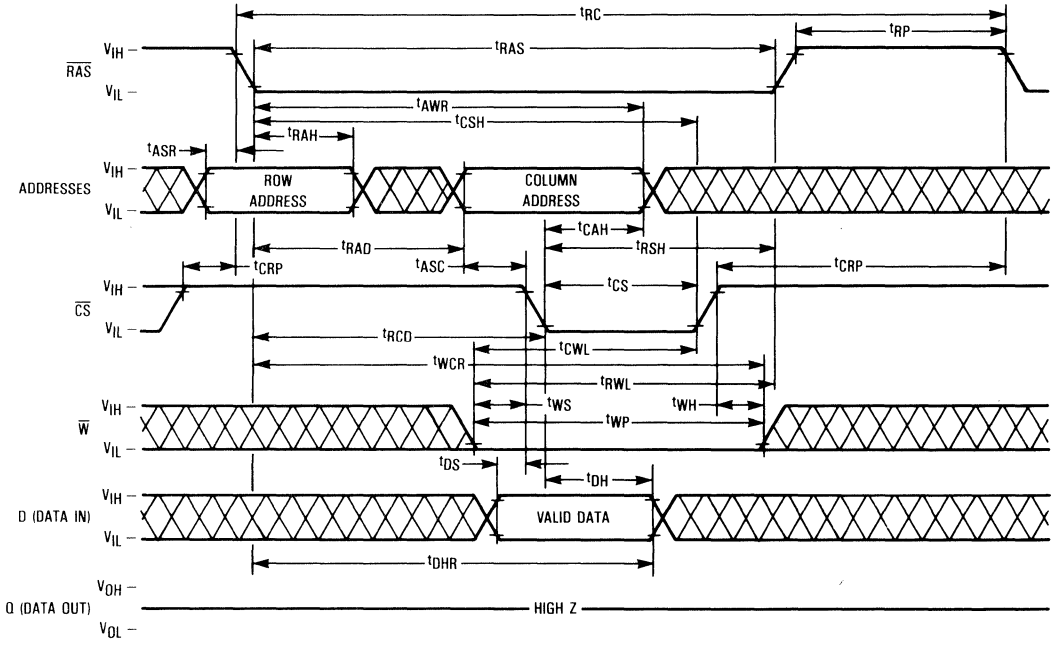
NOTES:

15. t_{AH} is time required to latch column address.
16. Operation within the t_{LWAD} limit ensures that t_{ALW} can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
17. Enter t_{RRH} or t_{RCH} must be satisfied for a read cycle.
18. t_{WS}, t_{WH}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
19. These parameters are referenced to $\overline{CS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.

READ CYCLE



EARLY WRITE CYCLE



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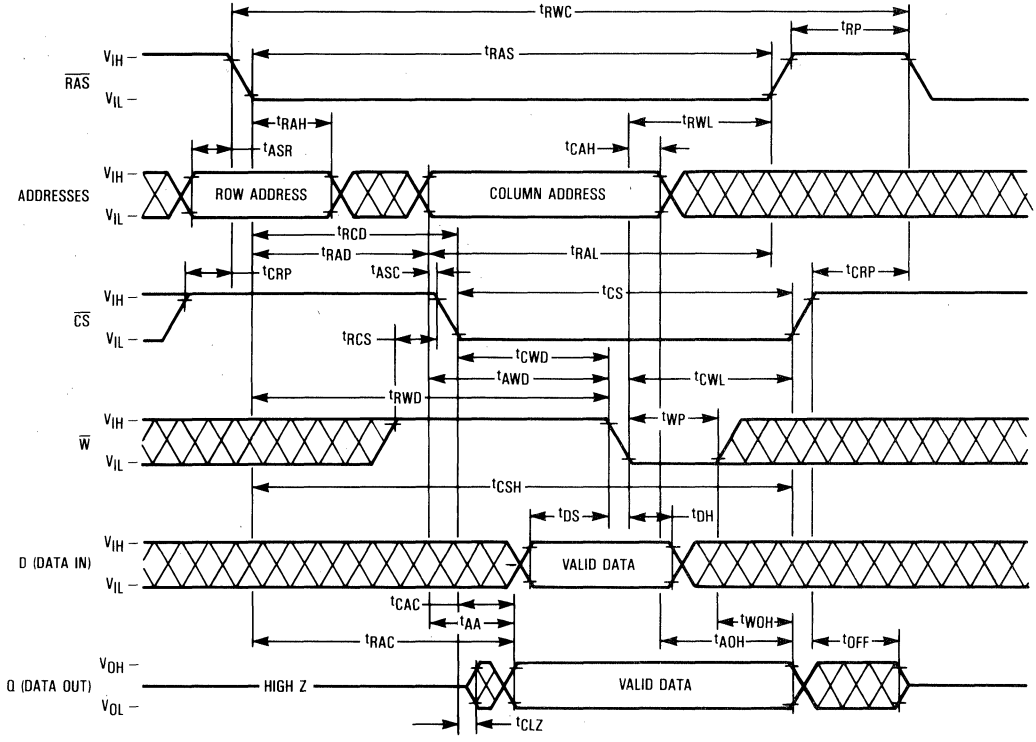
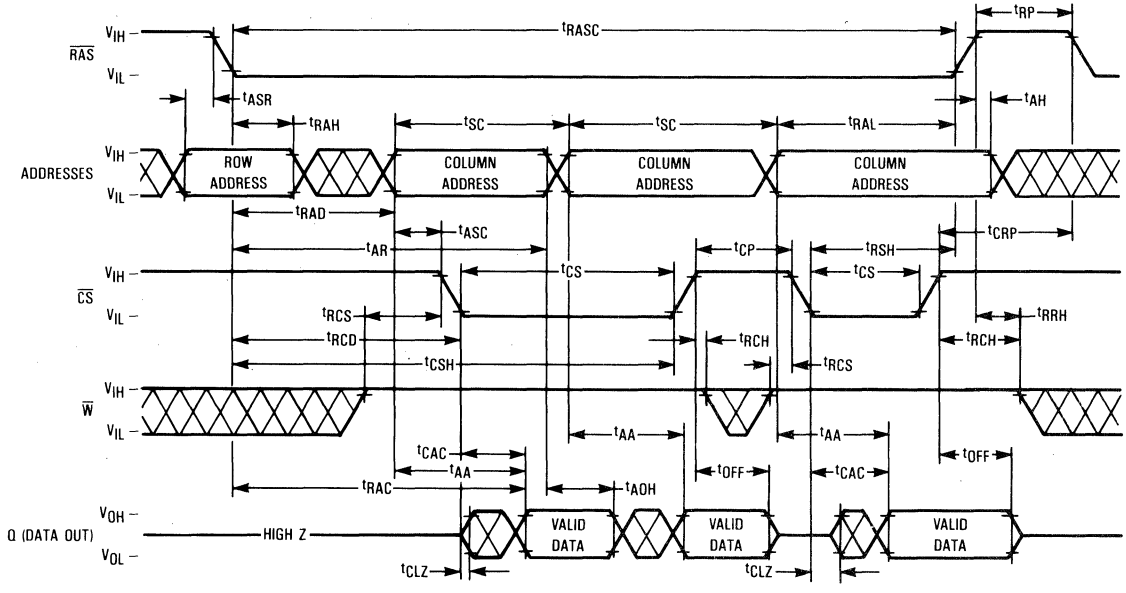
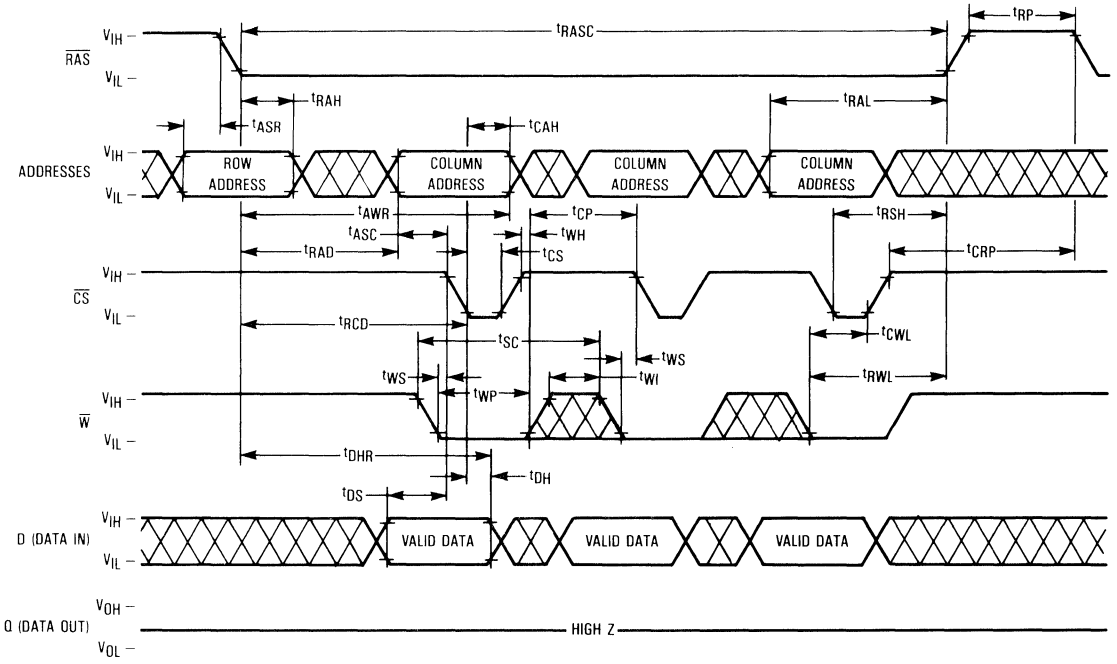
READ-WRITE CYCLE



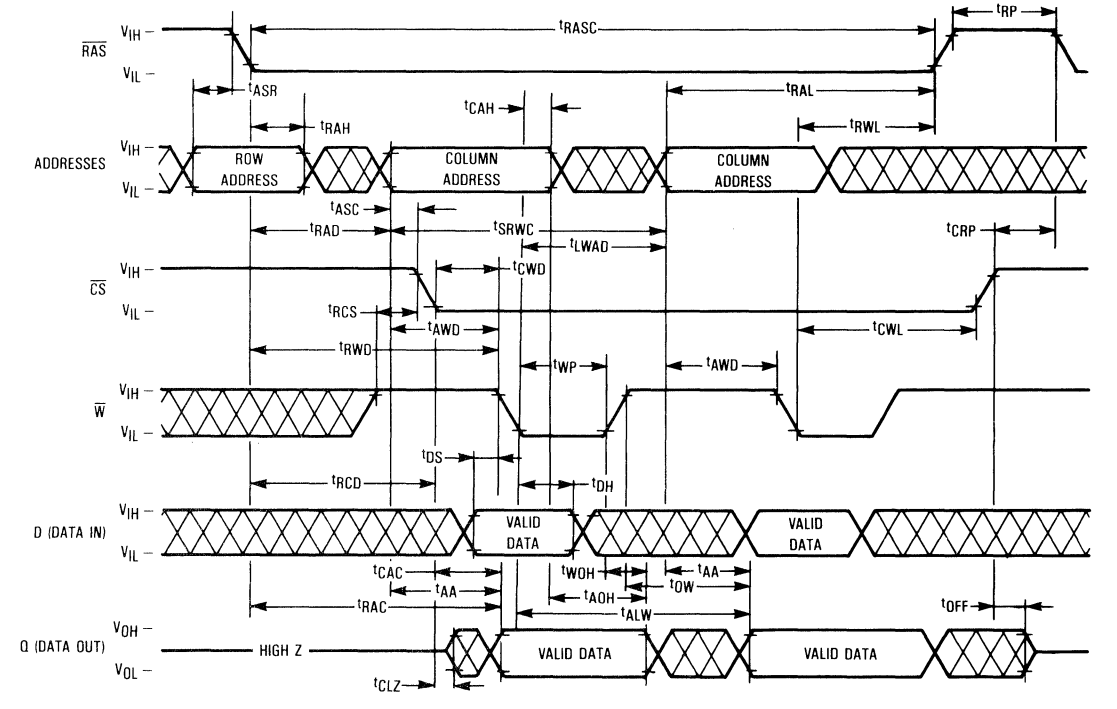
STATIC COLUMN MODE READ CYCLE



STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



STATIC COLUMN MODE READ-WRITE CYCLE



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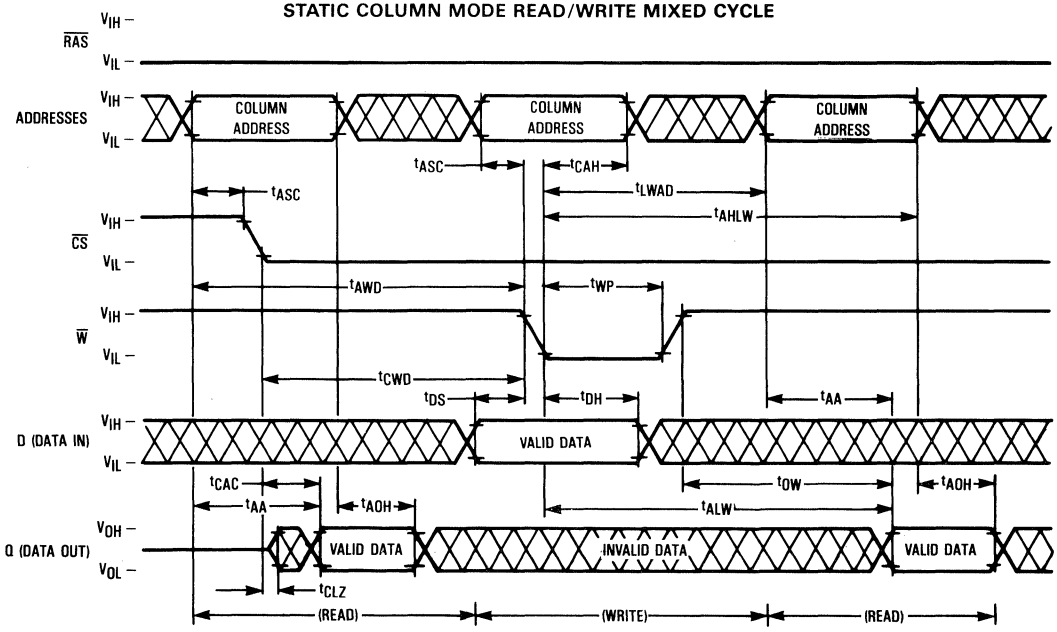
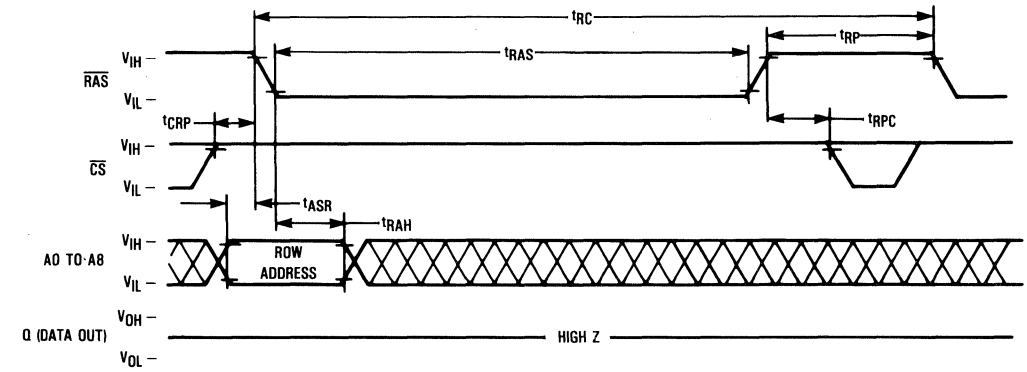
STATIC COLUMN MODE READ/WRITE MIXED CYCLE



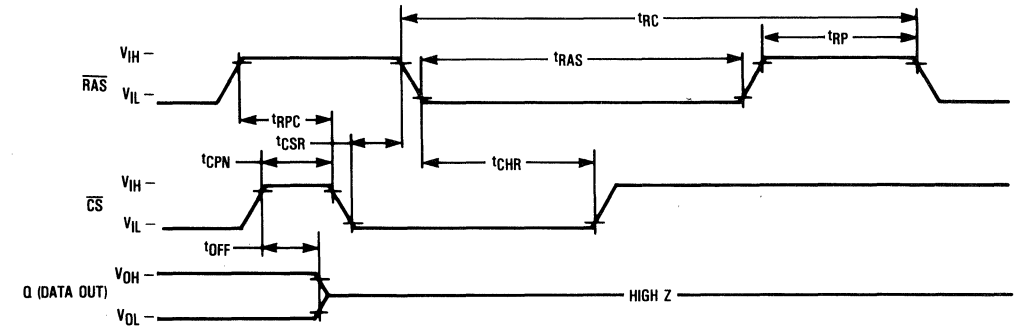
RAS ONLY REFRESH CYCLE

(W and A9 are Don't Care)

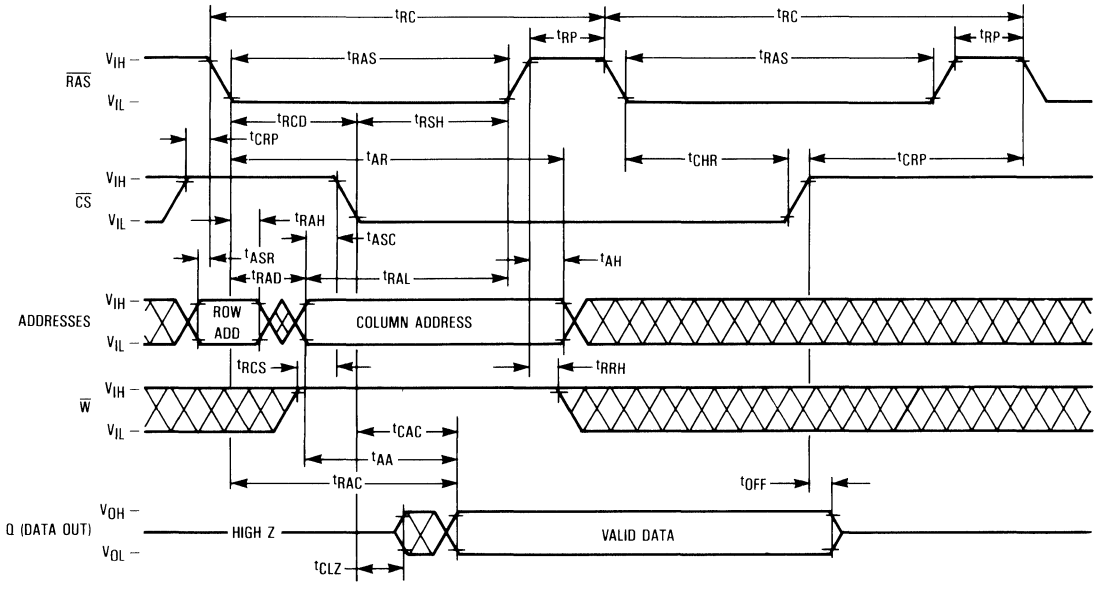


CS BEFORE RAS REFRESH CYCLE

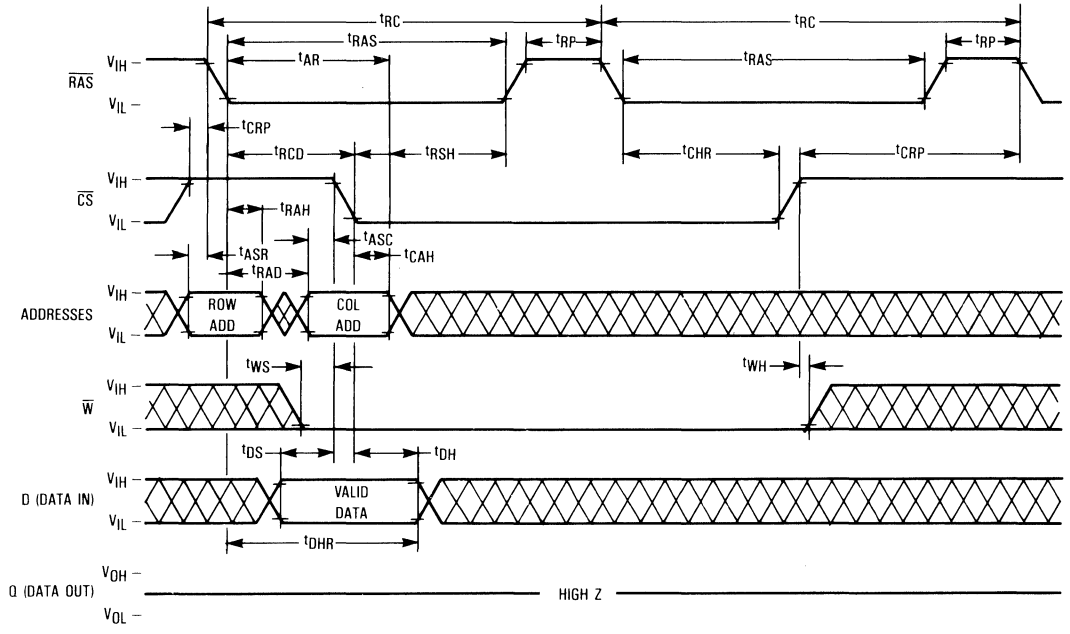
(W and A0 to A9 are Don't Care)



HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



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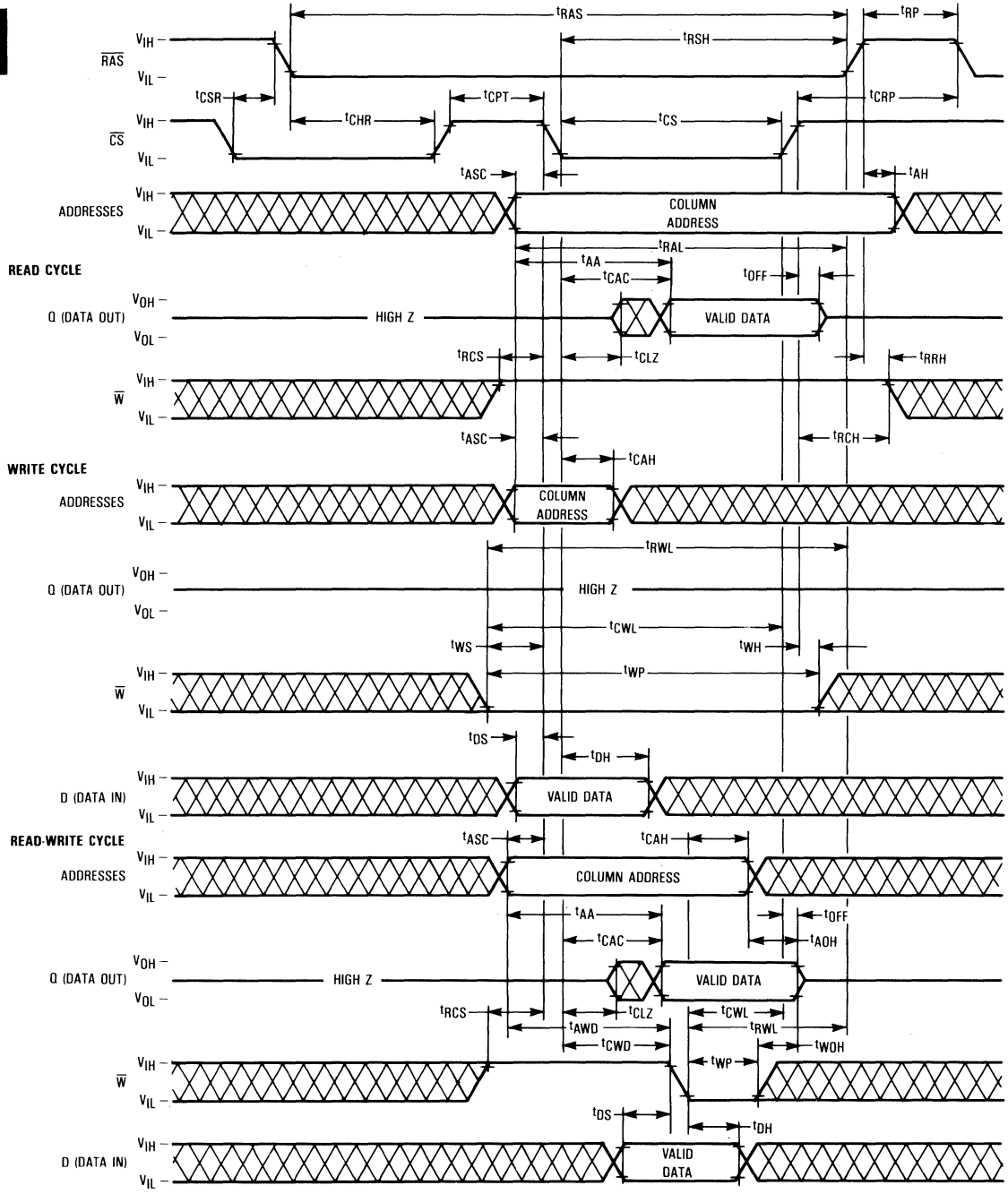
$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed with two separate 10-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and chip select ($\overline{CS}$). A total of twenty address bits will decode one of the 1,048,576 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 1M RAM, one is called the $\overline{RAS}$ only refresh cycle (described later) where a 9-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. The most significant bit on Row Address A9 is not required for refresh. The other variation, which is called static column, allows the user to column access the 2048 bits within a selected row. (See **STATIC COLUMN CYCLES** section.)

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CS}$ clock active transition will determine read access time. The external $\overline{CS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CS}$ clock will allow the external $\overline{CS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CS}) period for the $\overline{CS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CS}$ clock is active; the output will switch to the three-state mode when the $\overline{CS}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYCLES

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, t_{CWD} plays an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

2

STATIC COLUMN CYCLES

Static column operation allows fast successive data operations at the 1024 column locations within a row. Access time is typically half the regular $\overline{RAS}$ clock access (t_{RAC}). Static column operation is achieved by holding both $\overline{RAS}$ and $\overline{CS}$ low, and selecting the column location determined by the 10-bit column address field.

The static column cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by a column address and $\overline{CS}$ clock, as in a normal read or write cycle. Subsequent column addresses are accessed at a higher speed (t_{AA}, t_{ALW}, t_{OW}, or t_{CAC}, depending on the previous and intended operation), as the column address field is changed. Read, write, and read-write operations can be performed and mixed in any order when the device is in the static column mode.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will serve to refresh all the bits (2048) associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CS}$ Before $\overline{RAS}$ Refresh

This refresh cycle is initiated when $\overline{RAS}$ falls, after $\overline{CS}$ has been low (by t_{CSR}). This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CS}$ is held active (hidden refresh).

Hidden Refresh

The hidden refresh method allows refresh cycles to be performed while maintaining valid data at the output pin. Hidden refresh is performed by holding $\overline{CS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle. (See Figure 1.)

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM511000 can be tested by $\overline{CS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

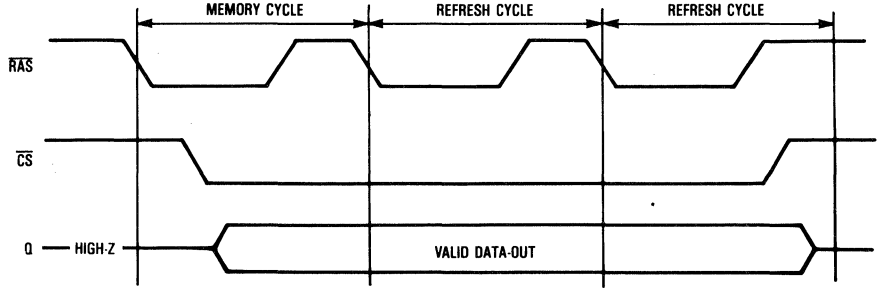


Figure 1. Hidden Refresh Cycle

TEST MODE

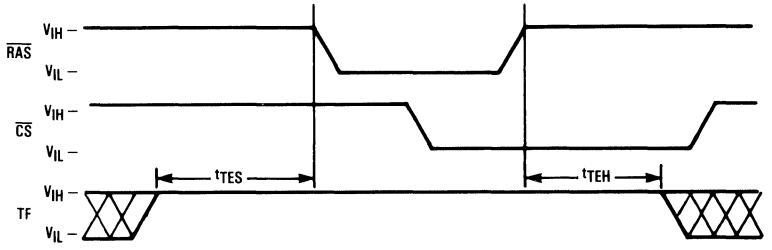
Internal organization of the device of 256K × 4 allows the device to be tested as if it were a 256K × 1 DRAM. In the test mode, data is written into 4 sectors in parallel and retrieved the same way. If all 4 bits are equal on a read, data out indicates the same data at all bits. If all 4 bits are not equal, the data out will indicate a high impedance state. See truth table and block diagram below.

The test mode function is performed on any of the timing cycles, including fast page mode, when the TF pin is held on "super voltage" (V_{CC} + 4.5 V), where (4.5 V ≤ V_{CC} ≤ 5.5 V), maximum voltage = 10.5 V, for the specified period (t_{TES}, t_{TEH}; see test mode cycle). A9 is ignored in the test mode. Normal operation requires the TF pin to either be connected to V_{IL}, or remain open.

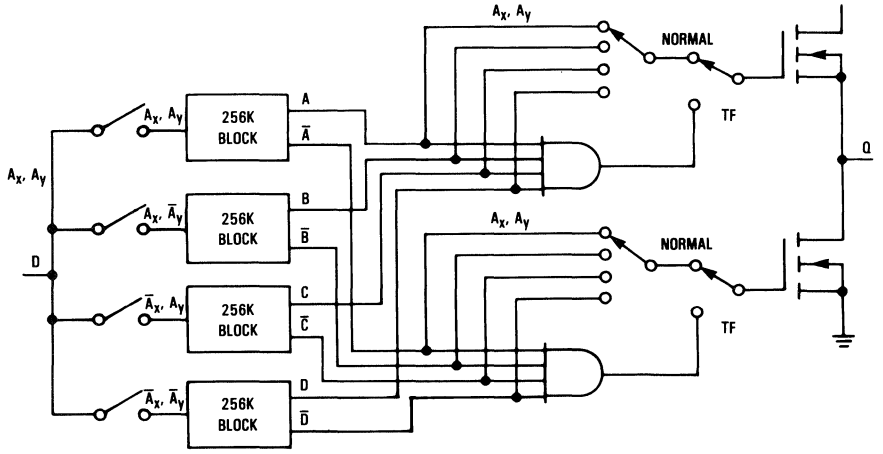
Test Mode Truth Table

A	B	C	D	Q
0	0	0	0	0
1	1	1	1	1
Any Other				High-Z

TEST MODE CYCLE

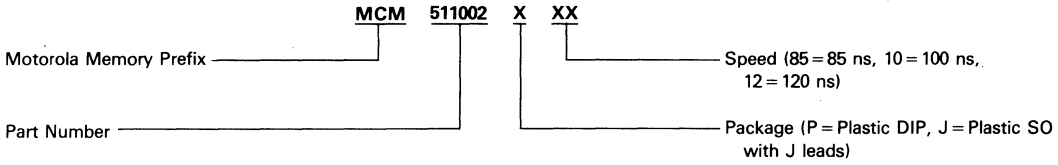


TEST FUNCTION BLOCK DIAGRAM



2

ORDERING INFORMATION
(Order by Full Part Number)



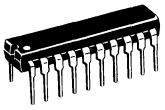
Full Part Numbers—MCM511002P85 MCM511002J85
MCM511002P10 MCM511002J10
MCM511002P12 MCM511002J12

MCM514256

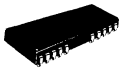
2

Advance Information

256K x 4 CMOS Dynamic RAM



P PACKAGE
PLASTIC
CASE 738A



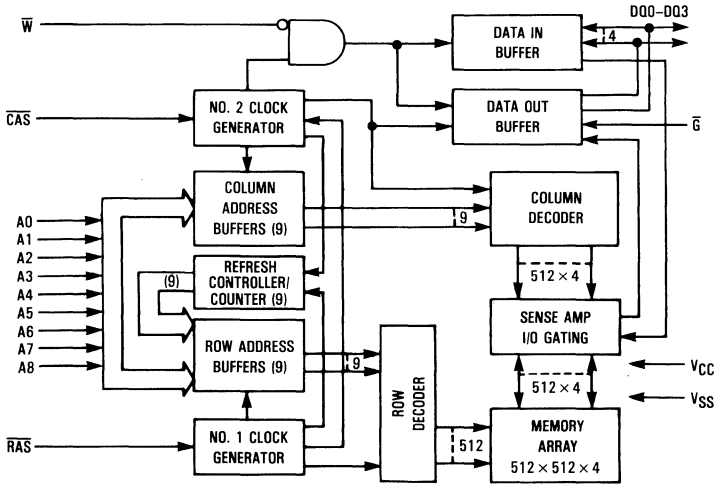
J PACKAGE
SMALL OUTLINE
CASE 822

The MCM514256 is a 1.2μ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

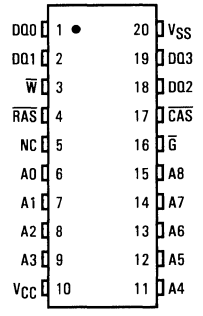
The MCM514256 requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in standard 300 mil wide packages: dual-in-line package (DIP) and J-lead small outline package.

- Three-State Data Output
- Fast Page Mode Capability
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM514256-85 = 85 ns (Maximum)
  MCM514256-10 = 100 ns (Maximum)
  MCM514256-12 = 120 ns (Maximum)
- Low Active Power Dissipation: MCM514256-85 = 413 mW (Maximum)
  MCM514256-10 = 358 mW (Maximum)
  MCM514256-12 = 303 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)

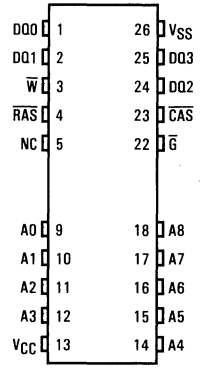
BLOCK DIAGRAM



PIN ASSIGNMENT
DUAL-IN-LINE



SMALL OUTLINE



PIN NAMES	
A0-A8	Address Input
DQ0-DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

2

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM514256-85, t_{RC} = 165 ns		—	75		
MCM514256-10, t_{RC} = 190 ns		—	65		
MCM514256-12, t_{RC} = 220 ns		—	55		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CAS}$ = V_{IH})	I_{CC3}			mA	2
MCM514256-85, t_{RC} = 165 ns		—	75		
MCM514256-10, t_{RC} = 190 ns		—	65		
MCM514256-12, t_{RC} = 220 ns		—	55		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM514256-85, t_{PC} = 50 ns		—	55		
MCM514256-10, t_{PC} = 55 ns		—	45		
MCM514256-12, t_{PC} = 70 ns		—	35		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} − 0.2 V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM514256-85, t_{RC} = 165 ns		—	75		
MCM514256-10, t_{RC} = 190 ns		—	65		
MCM514256-12, t_{RC} = 220 ns		—	55		
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CAS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A8	C_{in}	5	pF	3
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7	pF	3
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0-DQ3	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514256-85		MCM514256-10		MCM514256-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	165	–	190	–	220	–	ns	5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	225	–	255	–	295	–	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	50	–	55	–	70	–	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{CELCEL}	t_{PRMW}	110	–	115	–	140	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	85	–	100	–	120	ns	6, 7
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	–	30	–	30	–	35	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	–	45	–	50	–	60	ns	6, 9
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	–	45	–	50	–	65	ns	6
$\overline{CAS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	5	–	5	–	5	–	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	30	0	30	0	35	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	85	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	85	100,000	100	100,000	120	100,000	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	30	–	30	–	35	–	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	85	–	100	–	120	–	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	30	10,000	30	10,000	35	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	55	25	70	25	85	ns	11
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	20	40	20	50	20	60	ns	12
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	15	–	15	–	20	–	ns	
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CEHCEL}	t_{CP}	10	–	10	–	15	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	15	–	15	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	–	20	–	25	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	65	–	75	–	90	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	45	–	50	–	60	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

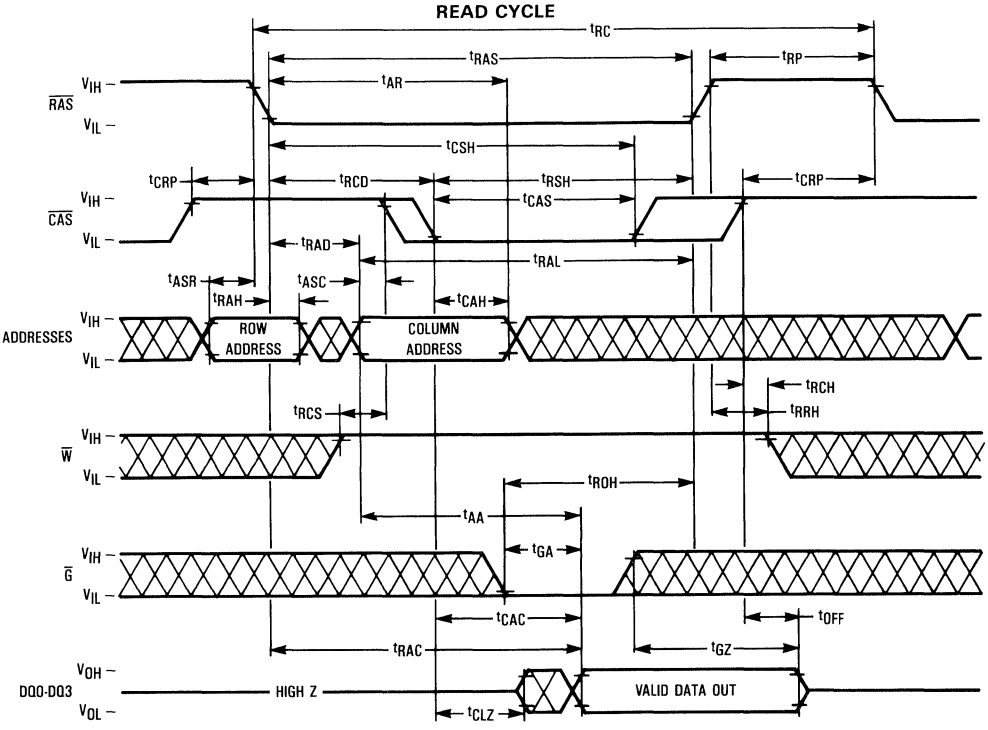
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM514256-85		MCM514256-10		MCM514256-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	13
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	13
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	20	–	20	–	25	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	65	–	75	–	90	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	20	–	20	–	25	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	25	–	30	–	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	25	–	30	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	20	–	20	–	25	–	ns	14
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	65	–	75	–	90	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	–	0	–	0	–	ns	15
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	65	–	65	–	75	–	ns	15
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	120	–	135	–	160	–	ns	15
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	80	–	85	–	100	–	ns	15
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	50	–	50	–	60	–	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	20	–	20	–	20	–	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	–	25	–	25	–	30	ns	
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	25	–	25	–	30	–	ns	
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	25	0	25	0	30	ns	
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	25	–	25	–	30	–	ns	

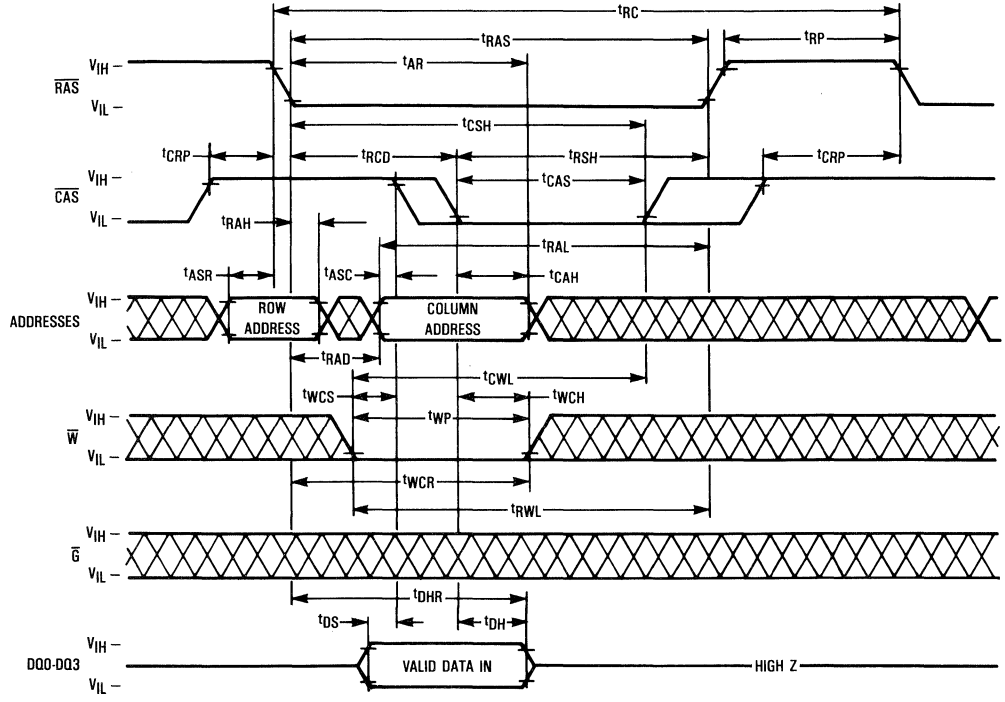
NOTES:

13. Enter t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

READ CYCLE



WRITE CYCLE (EARLY WRITE)



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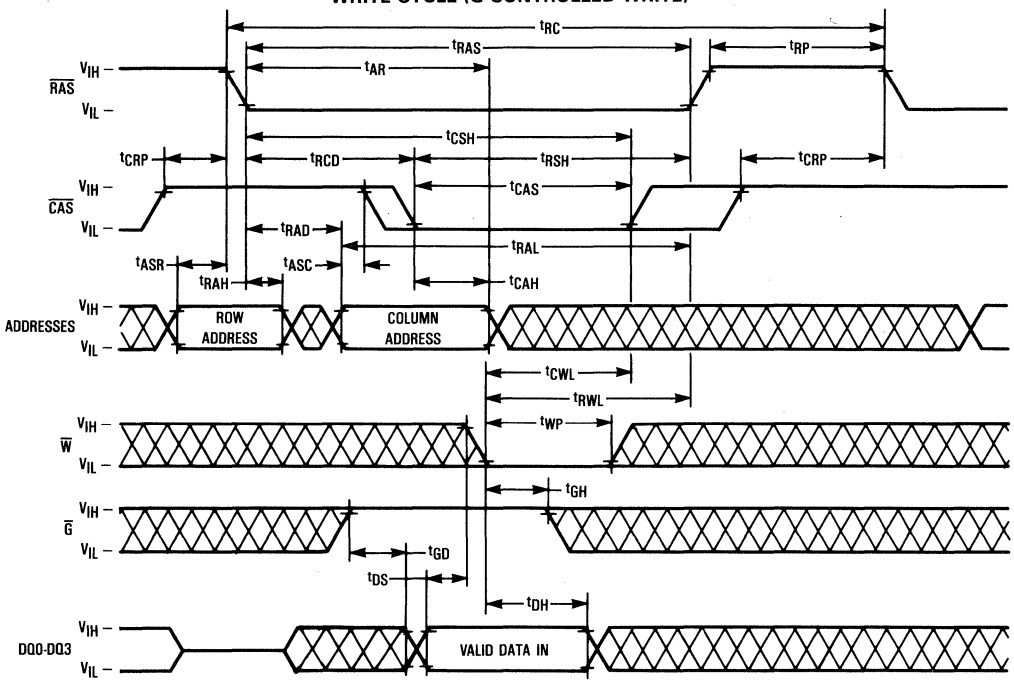
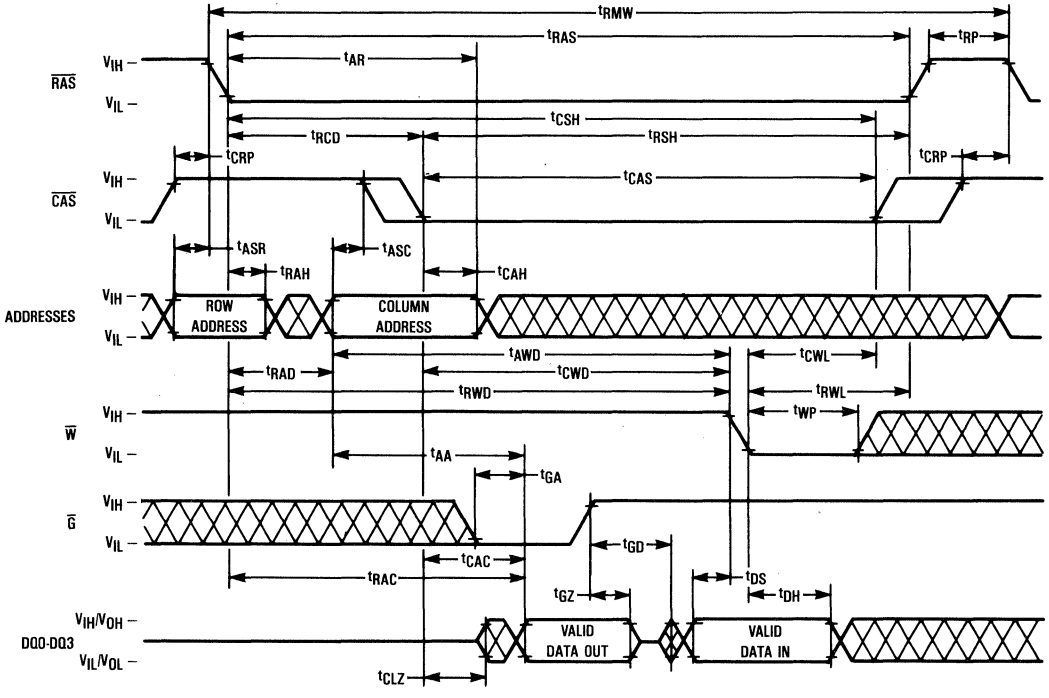
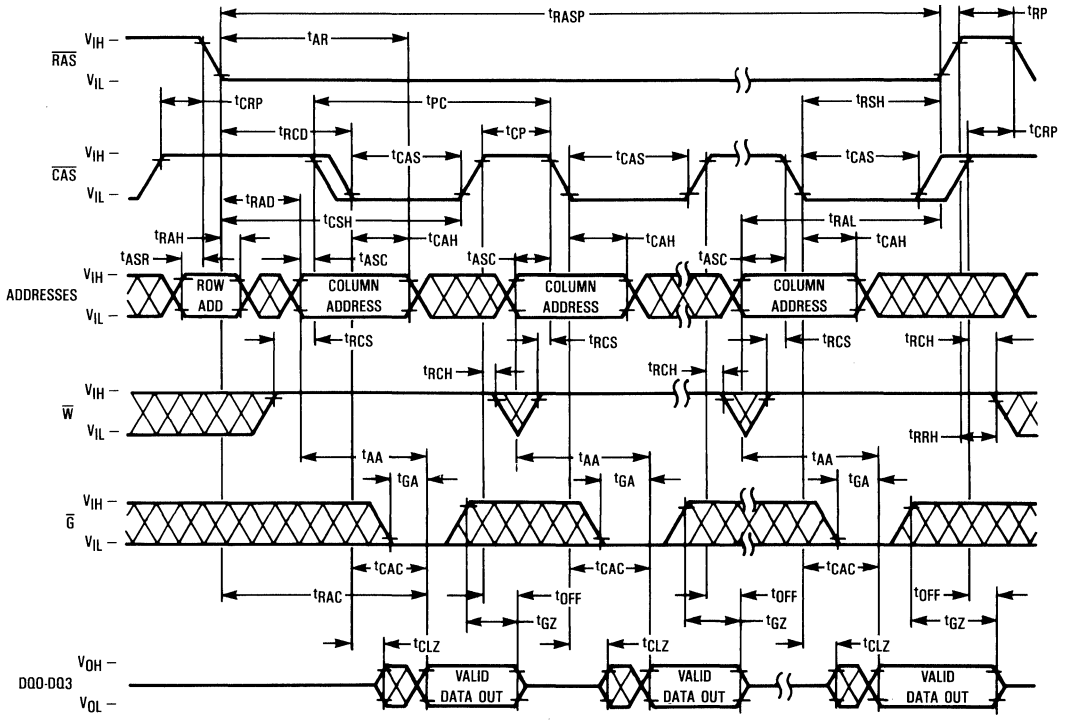
WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



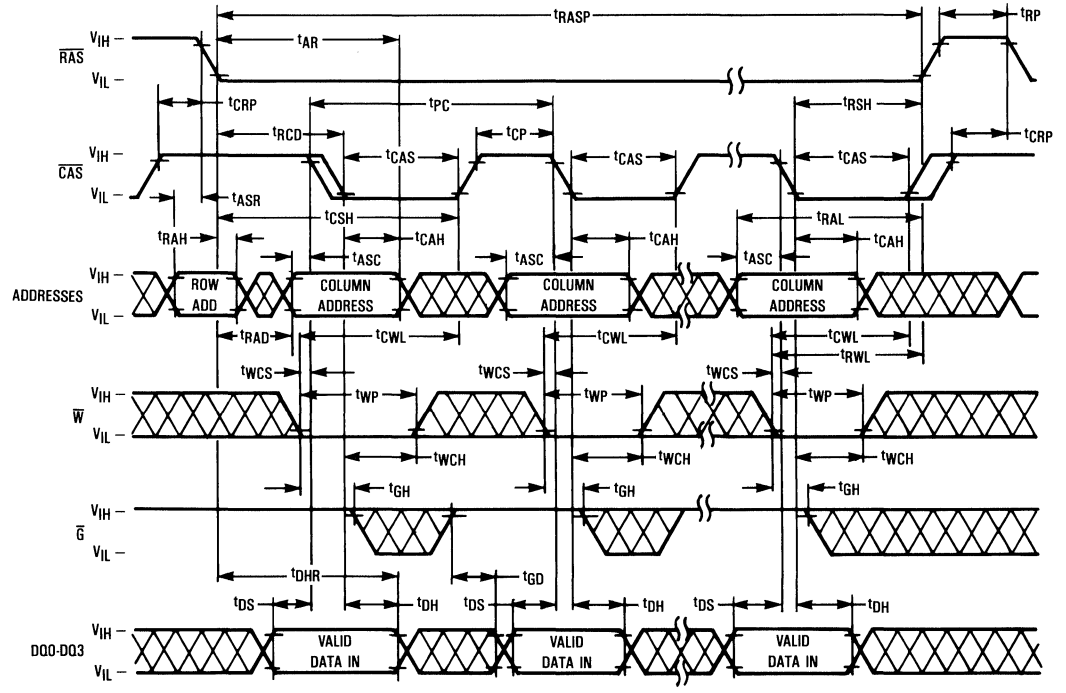
READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE



FAST PAGE MODE WRITE CYCLE



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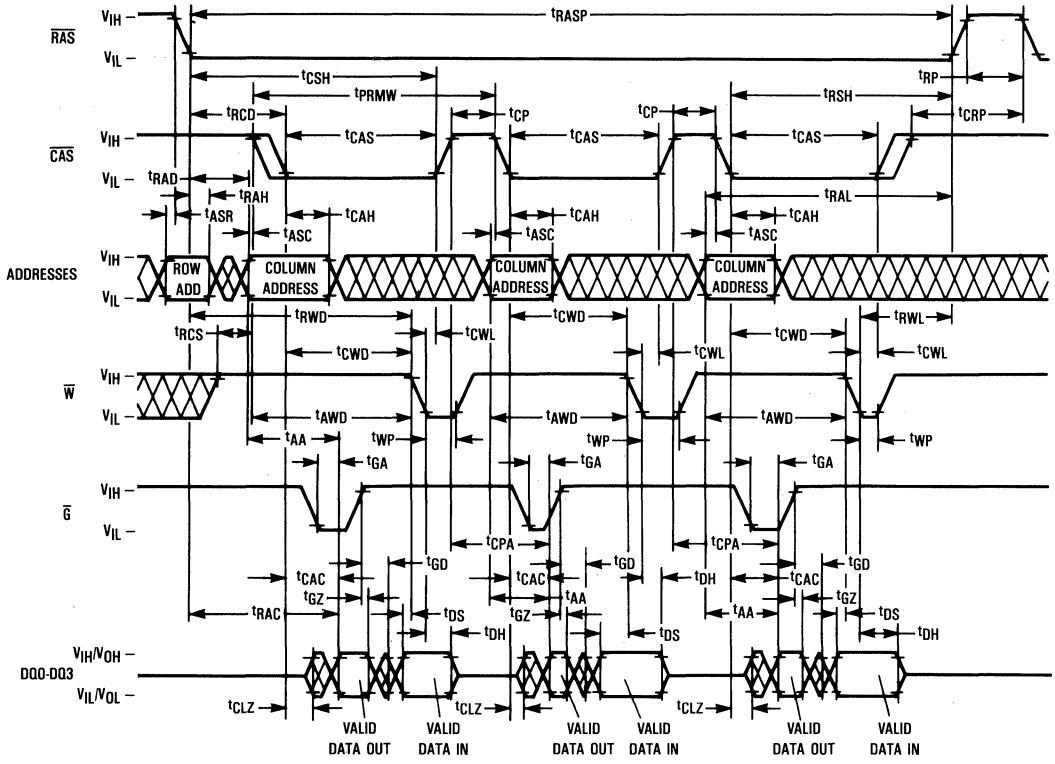
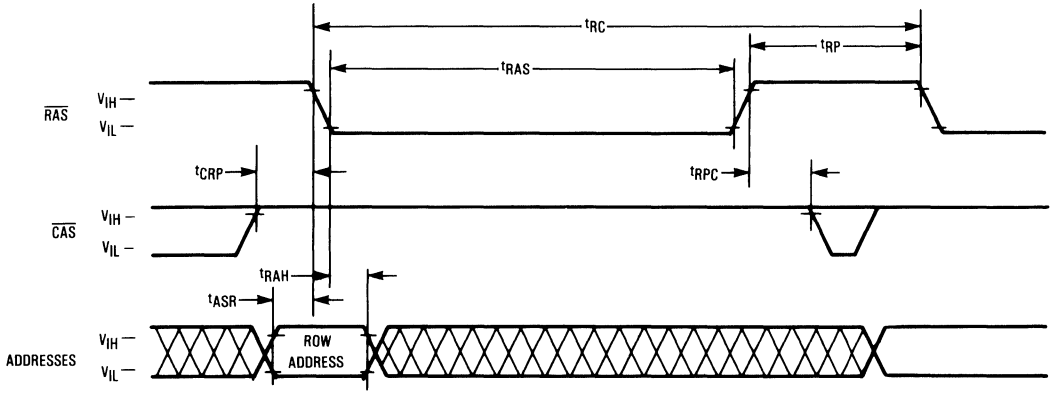
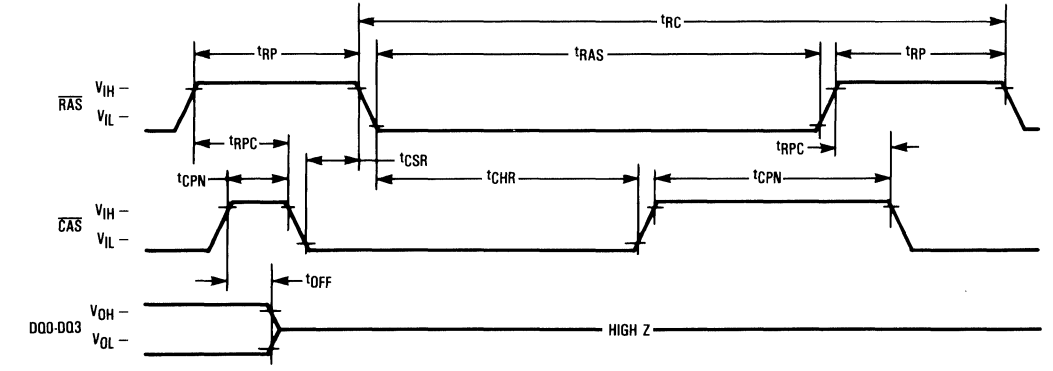
FAST PAGE MODE READ-MODIFY-WRITE CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and $\overline{G}$ are Don't Care)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$, $\overline{G}$, and A0-A8 are Don't Care)



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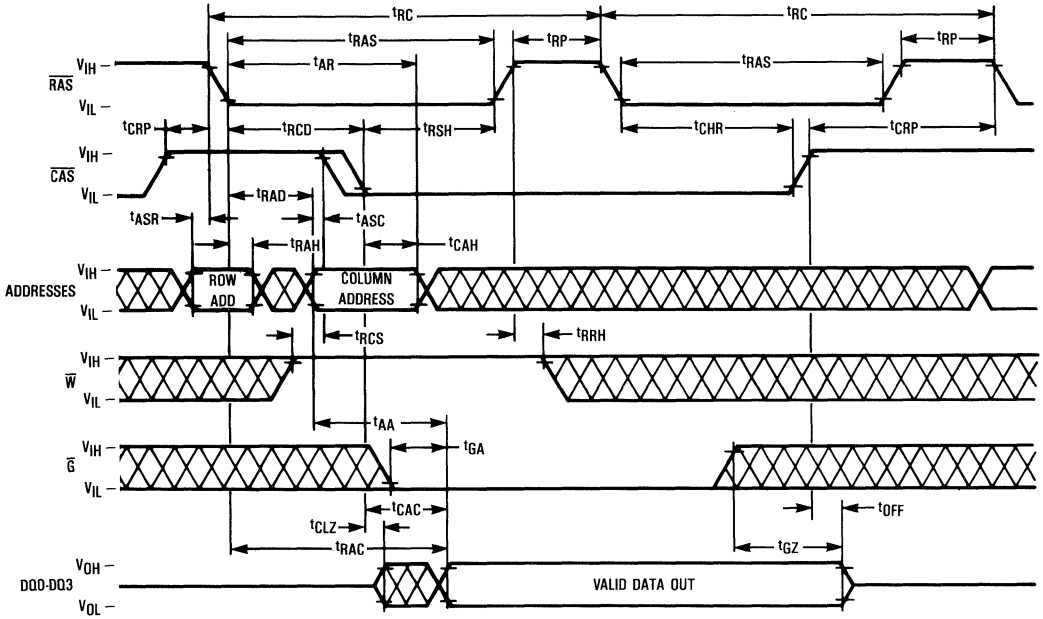
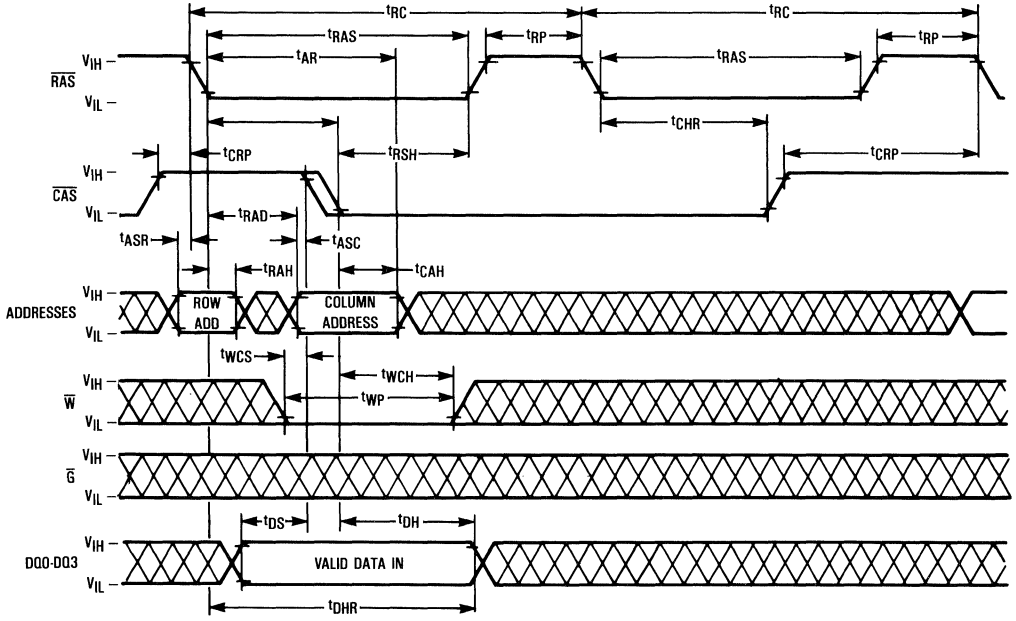
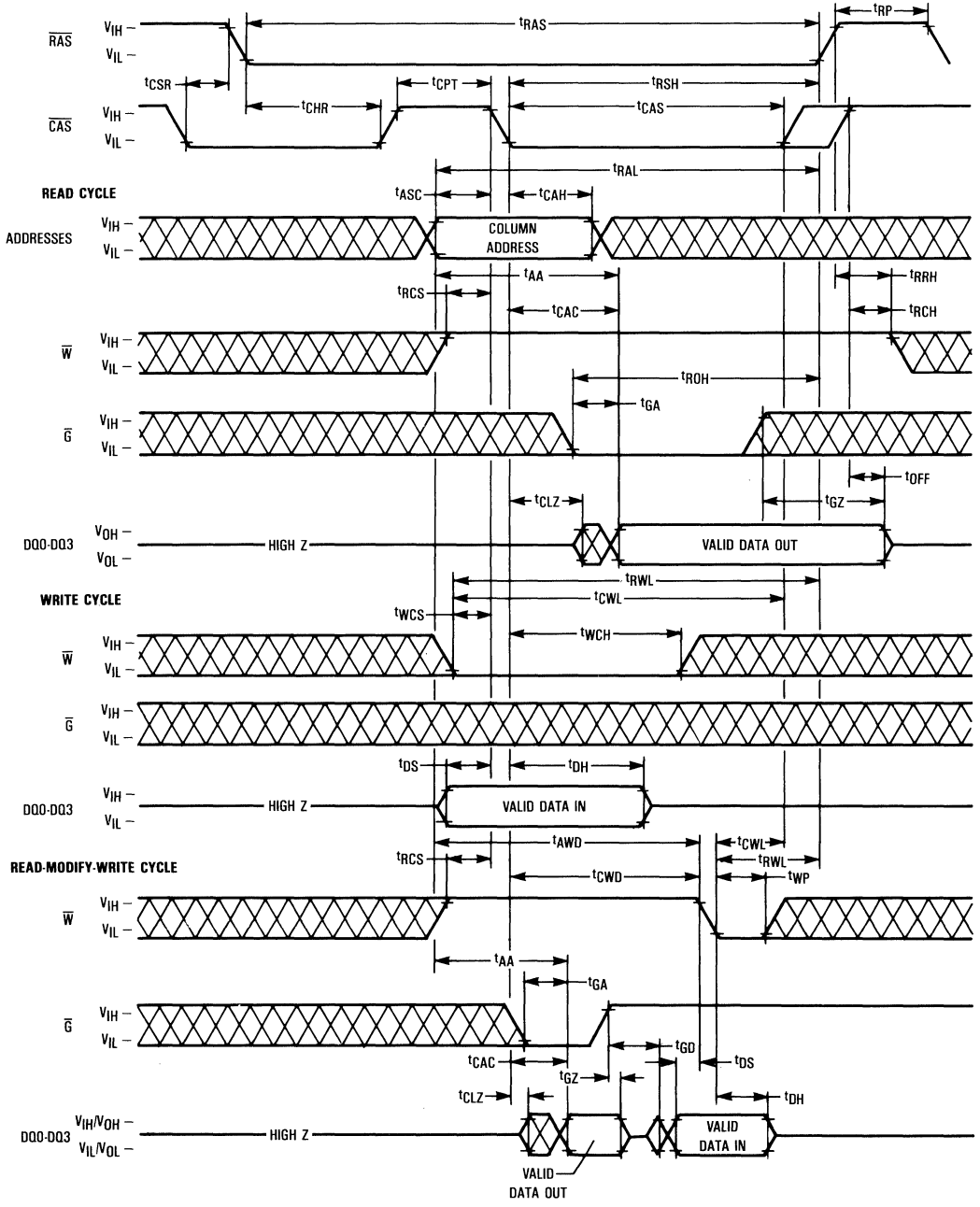
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



2

DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CAS}$). A total of 18 address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, other variations in addressing the RAM, the refresh modes ($\overline{RAS}$ only refresh; $\overline{CAS}$ before $\overline{RAS}$ refresh; hidden refresh), another mode called page mode allows the user to column access the 512 bits within a selected row. The refresh mode and page mode operations are described in more detail later on.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a page mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ and $\overline{G}$ clocks are active; the output will switch to the three-state mode when either the $\overline{CAS}$ or $\overline{G}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds — $[t_{RWL} + t_{RP} + 2t_T]$.

In a late write or a ready-modify-write cycle, $\overline{G}$ must be at the V_{IH} level to bring the output buffers to high impedance prior to data-in being valid.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE CYCLE

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

PAGE-MODE CYCLES

Page mode operation allows fast successive data operations at the 512 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 1M dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 9-bit column address field.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write cycle, the conditions normal to that mode of operation will apply in the page mode also. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will serve to refresh all the bits associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MCM514256 offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh

An optional feature of the MCM514256 is that refresh cycle may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CAS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. (see Figure 1 below)

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM514256 can be tested by $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

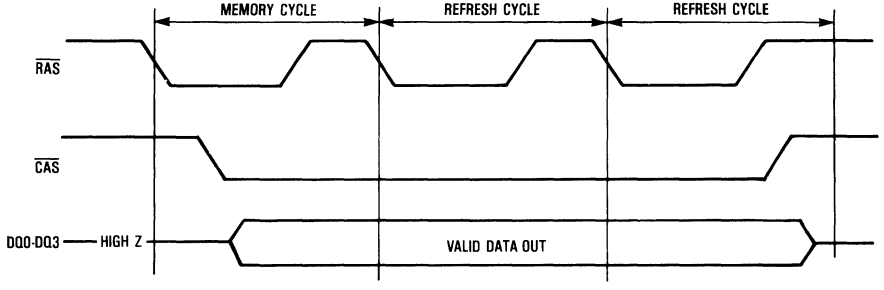


Figure 1. Hidden Refresh Cycle

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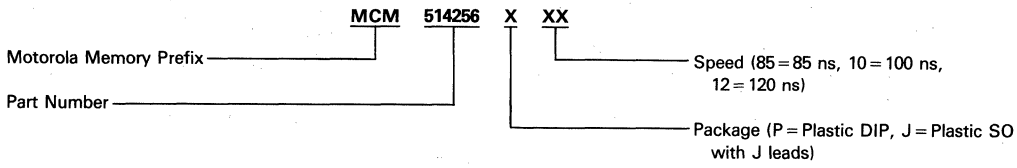
ORDERING INFORMATION
(Order by Full Part Number)



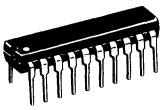
Full Part Numbers—MCM514256P85 MCM514256J85
MCM514256P10 MCM514256J10
MCM514256P12 MCM514256J12

MCM514258

2

Advance Information

256K × 4 CMOS Dynamic RAM



P PACKAGE
PLASTIC
CASE 738A

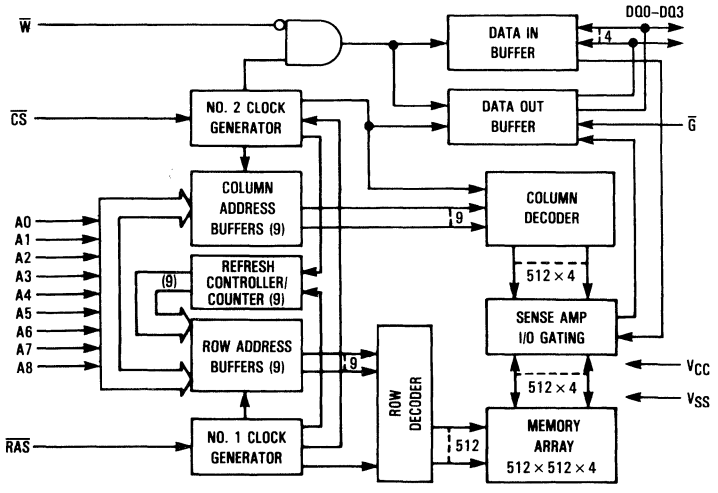
J PACKAGE
SMALL OUTLINE
CASE 822

The MCM514258 is a 1.2μ CMOS high-speed, dynamic random access memory. It is organized as 262,144 four-bit words and fabricated with CMOS silicon-gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

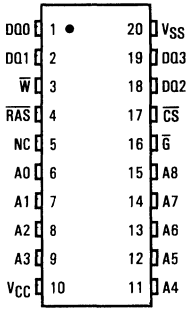
The MCM514258 requires only nine address lines; row and column address inputs are multiplexed. The device is packaged in standard 300 mil wide packages: dual-in-line package (DIP) and J-lead small outline package.

- Three-State Data Output
- Static Column Mode Capability
- TTL-Compatible Inputs and Output
- $\overline{RAS}$ Only Refresh
- $\overline{CS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 512 Cycle, 8 ms Refresh
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM514258-85 = 85 ns (Maximum)
  MCM514258-10 = 100 ns (Maximum)
  MCM514258-12 = 120 ns (Maximum)
- Low Active Power Dissipation: MCM514258-85 = 413 mW (Maximum)
  MCM514258-10 = 358 mW (Maximum)
  MCM514258-12 = 303 mW (Maximum)
- Low Standby Power Dissipation: 11 mW (Maximum, TTL Levels)
  5.5 mW (Maximum, CMOS Levels)

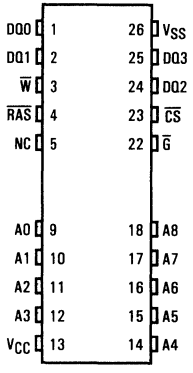
BLOCK DIAGRAM



PIN ASSIGNMENT
DUAL-IN-LINE



SMALL OUTLINE



PIN NAMES	
A0-A8	Address Input
DQ0-DQ3	Data Input/Output
$\overline{G}$	Output Enable
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−1 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−1 to +7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0		
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V	1
Logic Low Voltage, All Inputs	V_{IL}	−1.0	—	0.8	V	1

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	2
MCM514258-85, t_{RC} = 165 ns		—	75		
MCM514258-10, t_{RC} = 190 ns		—	65		
MCM514258-12, t_{RC} = 220 ns		—	55		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{IH})	I_{CC2}	—	2.0	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles ($\overline{CS}$ = V_{IH})	I_{CC3}			mA	2
MCM514258-85, t_{RC} = 165 ns		—	75		
MCM514258-10, t_{RC} = 190 ns		—	65		
MCM514258-12, t_{RC} = 220 ns		—	55		
V_{CC} Power Supply Current During Static Column Mode Cycle ($\overline{RAS}$ = V_{IL})	I_{CC4}			mA	2
MCM514258-85, t_{SC} = 50 ns		—	75		
MCM514258-10, t_{SC} = 55 ns		—	65		
MCM514258-12, t_{SC} = 70 ns		—	55		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CS}$ = V_{CC} − 0.2 V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CS}$ Before $\overline{RAS}$ Refresh Cycle	I_{CC6}			mA	2
MCM514258-85, t_{RC} = 165 ns		—	75		
MCM514258-10, t_{RC} = 190 ns		—	65		
MCM514258-12, t_{RC} = 220 ns		—	55		
Input Leakage Current (0 V ≤ V_{in} ≤ 6.5 V)	$I_{lkg(I)}$	−10	10	μA	
Output Leakage Current ($\overline{CS}$ = V_{IH}, 0 V ≤ V_{out} ≤ 5.5 V)	$I_{lkg(O)}$	−10	10	μA	
Output High Voltage (I_{OH} = −5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit	Notes
Input Capacitance	A0-A8	C_{in}	5	pF	3
	$\overline{G}$, $\overline{RAS}$, $\overline{CS}$, $\overline{W}$		7	pF	3
Output Capacitance ($\overline{CS}$ = V_{IH} to Disable Output)	DQ0-DQ3	C_{out}	7	pF	3

NOTES:
1. All voltages referenced to V_{SS}.
2. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
3. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ-MODIFY-WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM514258-85		MCM514258-10		MCM514258-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	165	–	190	–	220	–	ns	5
Read-Modify-Write Cycle Time	t_{RELREL}	t_{RMW}	225	–	255	–	295	–	ns	5
Static Column Mode Cycle Time	t_{AVAV}	t_{SC}	50	–	55	–	65	–	ns	
Static Column Mode Read-Modify-Write Cycle Time	t_{AVAV}	t_{SRMW}	110	–	115	–	135	–	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	–	85	–	100	–	120	ns	6, 7
Access Time from $\overline{CS}$	t_{CELQV}	t_{CAC}	–	30	–	30	–	35	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	–	45	–	50	–	60	ns	6, 9
Access Time from Last Write	t_{WLQV}	t_{ALW}	–	85	–	95	–	115	ns	6, 10
$\overline{CS}$ to Output in Low-Z	t_{CELQX}	t_{CLZ}	5	–	5	–	5	–	ns	6
Output Buffer and Turn-Off Delay	t_{CEHQZ}	t_{OFF}	0	30	0	30	0	35	ns	11
Output Data Hold Time from Column Address	t_{AXQX}	t_{AOH}	5	–	5	–	5	–	ns	
Output Data Enable Time from Write	t_{WHQV}	t_{OW}	–	30	–	30	–	35	ns	
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	70	–	80	–	90	–	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	85	10,000	100	10,000	120	10,000	ns	
$\overline{RAS}$ Pulse Width (Static Column Mode)	t_{RELREH}	t_{RASC}	85	100,000	100	100,000	120	100,000	ns	
$\overline{CS}$ to $\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	30	–	30	–	35	–	ns	
$\overline{RAS}$ to $\overline{CS}$ Hold Time	t_{RELCEH}	t_{CSH}	85	–	100	–	120	–	ns	
$\overline{CS}$ Pulse Width	t_{CELCEH}	t_{CS}	30	10,000	30	10,000	35	10,000	ns	
$\overline{CS}$ Pulse Width (Static Column Mode)	t_{CELCEH}	t_{CSC}	30	100,000	30	100,000	35	100,000	ns	
$\overline{RAS}$ to $\overline{CS}$ Delay Time	t_{RELCEL}	t_{RCD}	25	55	25	70	25	85	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	20	40	20	50	20	60	ns	13
$\overline{CS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	10	–	10	–	10	–	ns	
$\overline{CS}$ Precharge Time	t_{CEHCEL}	t_{CPN}	15	–	15	–	20	–	ns	
$\overline{CS}$ Precharge Time (Static Column Mode)	t_{CEHCEL}	t_{CP}	10	–	10	–	15	–	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	15	–	15	–	15	–	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	20	–	20	–	25	–	ns	
Write Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AWR}	65	–	75	–	90	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{RELAX}	t_{AR}	100	–	115	–	140	–	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	45	–	50	–	60	–	ns	

(continued)

NOTES:

1. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.
6. Measured with a current load equivalent to 2 TTL (−200 µA, +4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. Assumes that $t_{LWAD} \leq t_{LWAD}$ (max).
11. t_{OFF} (max) and/or t_{GZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

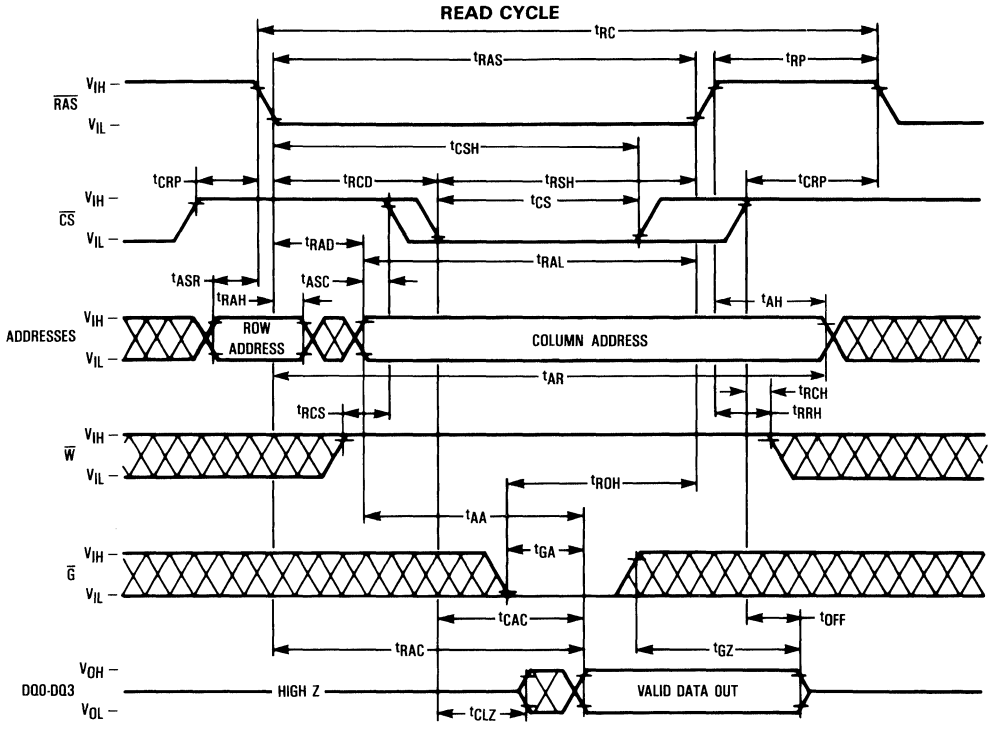
READ, WRITE, AND READ-MODIFY-WRITE CYCLES (Continued)

Parameter	Symbol		MCM514258-85		MCM514258-10		MCM514258-12		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Column Address Hold Time Referenced to $\overline{RAS}$	t_{REHAX}	t_{AH}	10	–	10	–	15	–	ns	14
Last Write to Column Address Delay Time	t_{WLAV}	t_{LWAD}	25	40	25	45	30	55	ns	15
Last Write to Column Address Hold Time	t_{WLAX}	t_{AHLW}	85	–	95	–	115	–	ns	
Read Command Setup Time Referenced to $\overline{CS}$	t_{WHCEL}	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time Referenced to $\overline{CS}$	t_{CEHWX}	t_{RCH}	0	–	0	–	0	–	ns	16
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	–	0	–	0	–	ns	16
Write Command Hold Time (Output Data Disable)	t_{CEHWH}	t_{WH}	0	–	0	–	0	–	ns	17
Write Command Hold Time Referenced to $\overline{RAS}$	t_{RELWH}	t_{WCR}	65	–	75	–	90	–	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	20	–	20	–	25	–	ns	
Write Inactive Time	t_{WHWL}	t_{WI}	10	–	10	–	15	–	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	20	–	25	–	30	–	ns	
Write Command to $\overline{CS}$ Lead Time	t_{WLCEH}	t_{CWL}	20	–	25	–	30	–	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	–	0	–	0	–	ns	18
Data in Hold Time	t_{CELDX}	t_{DH}	20	–	20	–	25	–	ns	18
Data in Hold Time Referenced to $\overline{RAS}$	t_{RELDX}	t_{DHR}	65	–	75	–	90	–	ns	
Refresh Period	t_{RVRV}	t_{RFSH}	–	8	–	8	–	8	ms	
Write Command Setup Time (Output Data Disable)	t_{WLCEL}	t_{WS}	0	–	0	–	0	–	ns	17
$\overline{CS}$ to Write Delay (RMW Cycle)	t_{CELWL}	t_{CWD}	65	–	65	–	75	–	ns	17
$\overline{RAS}$ to Write Delay (RMW Cycle)	t_{RELWL}	t_{RWD}	120	–	135	–	160	–	ns	17
Column Address to Write Delay Time	t_{AVWL}	t_{AWD}	80	–	85	–	100	–	ns	17
$\overline{CS}$ Setup Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{CELREL}	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{CS}$ Hold Time for $\overline{CS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	30	–	30	–	30	–	ns	
$\overline{RAS}$ Precharge to $\overline{CS}$ Active Time	t_{REHCEL}	t_{RPC}	0	–	0	–	0	–	ns	
$\overline{CS}$ Precharge Time for $\overline{CS}$ Before $\overline{RAS}$ Counter Test	t_{CEHCEL}	t_{CPT}	50	–	50	–	60	–	ns	
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	20	–	20	–	20	–	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	–	30	–	30	–	35	ns	
$\overline{G}$ to Data Delay	t_{GHDX}	t_{GD}	25	–	25	–	30	–	ns	
Output Buffer Turn-Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	25	0	25	0	30	ns	11
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	25	–	25	–	30	–	ns	

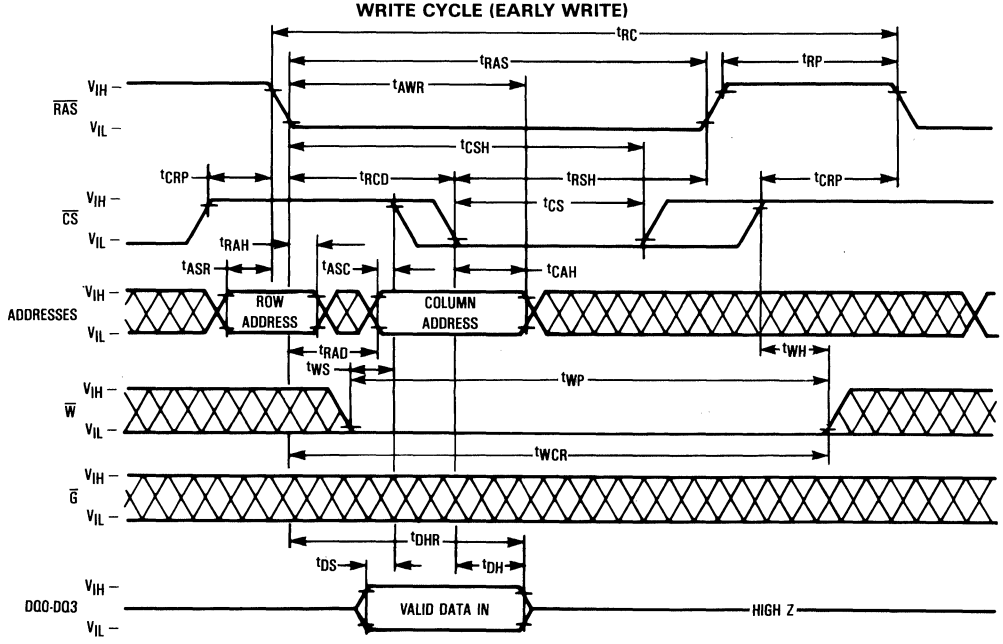
NOTES:

14. t_{AH} is the condition to latch the column address when $\overline{RAS}$ transitions from low to high.
15. Operation within the specified t_{LWAD} (max) limit ensures that t_{ALW} (max) can be met. t_{LWAD} (max) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max) limit, then access time is controlled exclusively by t_{AA}.
16. Enter t_{RRH} or t_{RCH} must be satisfied for a read cycle.
17. t_{WH}, t_{WS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WS} \geq t_{WS}$ (min) and $t_{WH} \geq t_{WH}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
18. These parameters are referenced to $\overline{CS}$ leading edge in random write cycles and to $\overline{W}$ leading edge in delayed write or read-modify-write cycles.

READ CYCLE

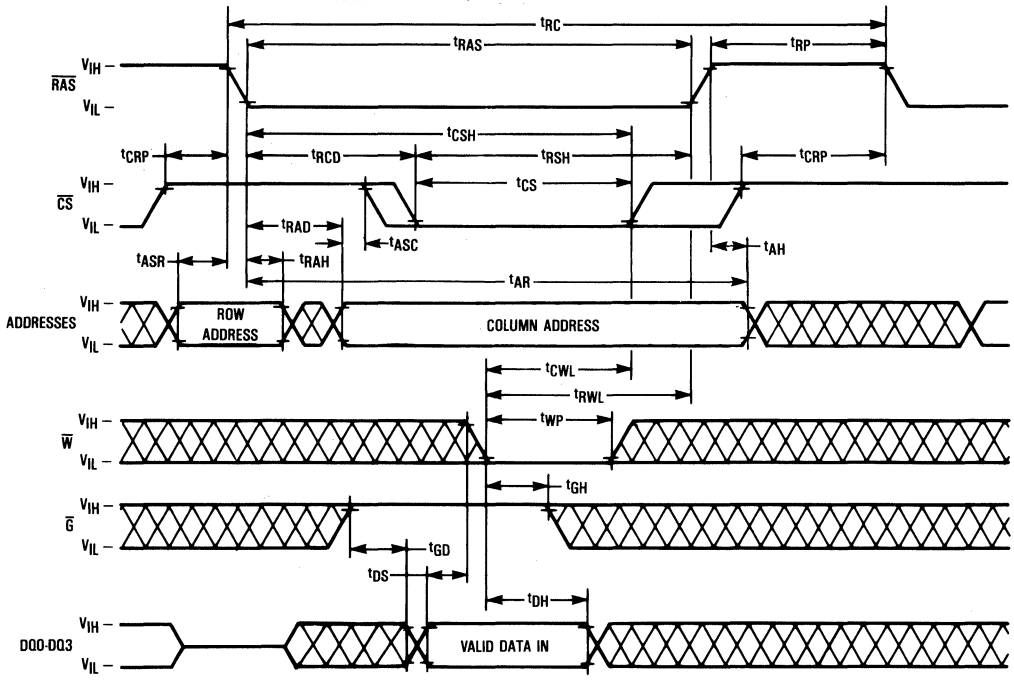


WRITE CYCLE (EARLY WRITE)

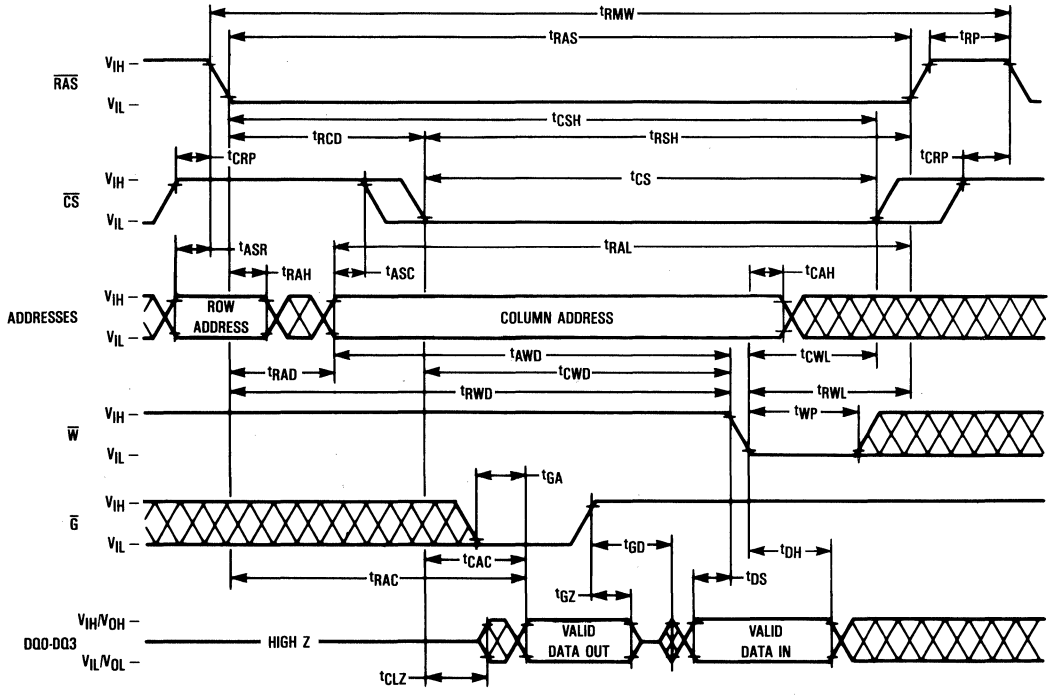


2

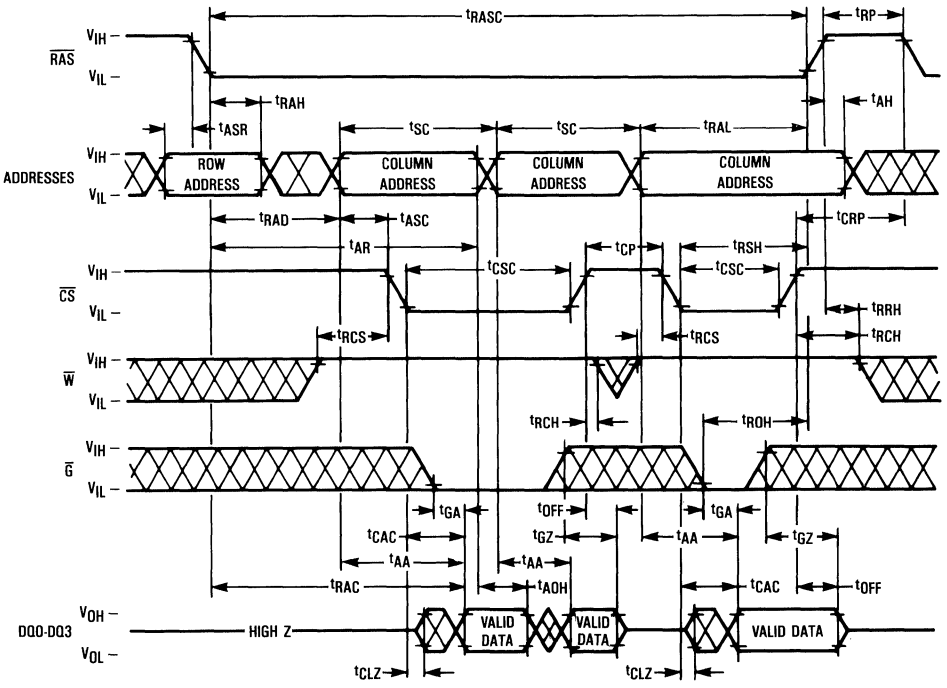
WRITE CYCLE ($\overline{G}$ CONTROLLED WRITE)



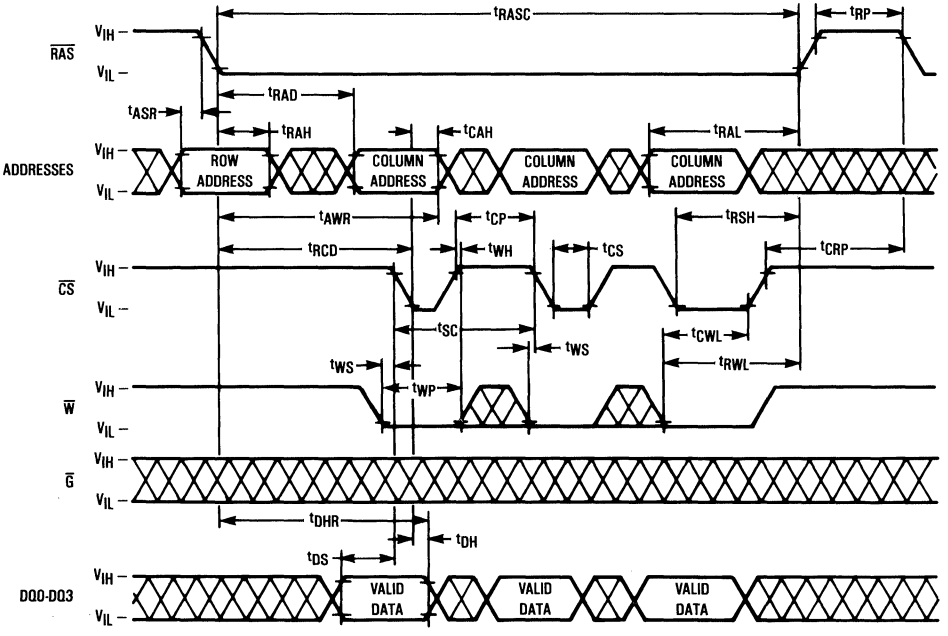
READ-MODIFY-WRITE CYCLE



STATIC COLUMN MODE READ CYCLE

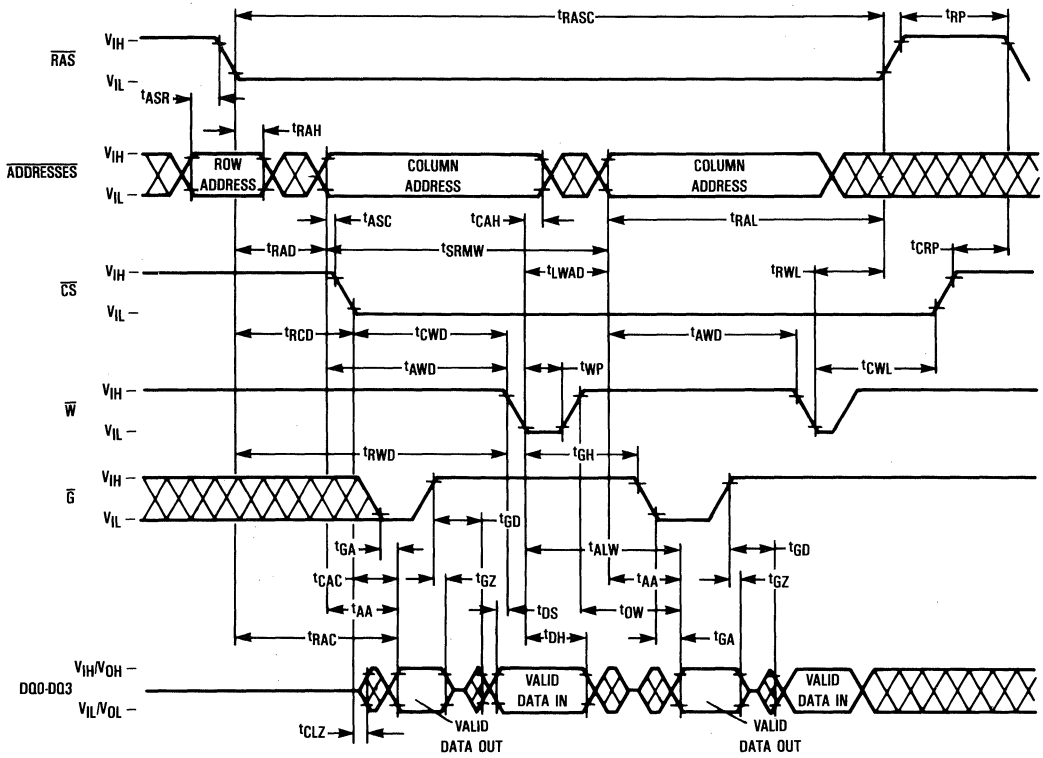


STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

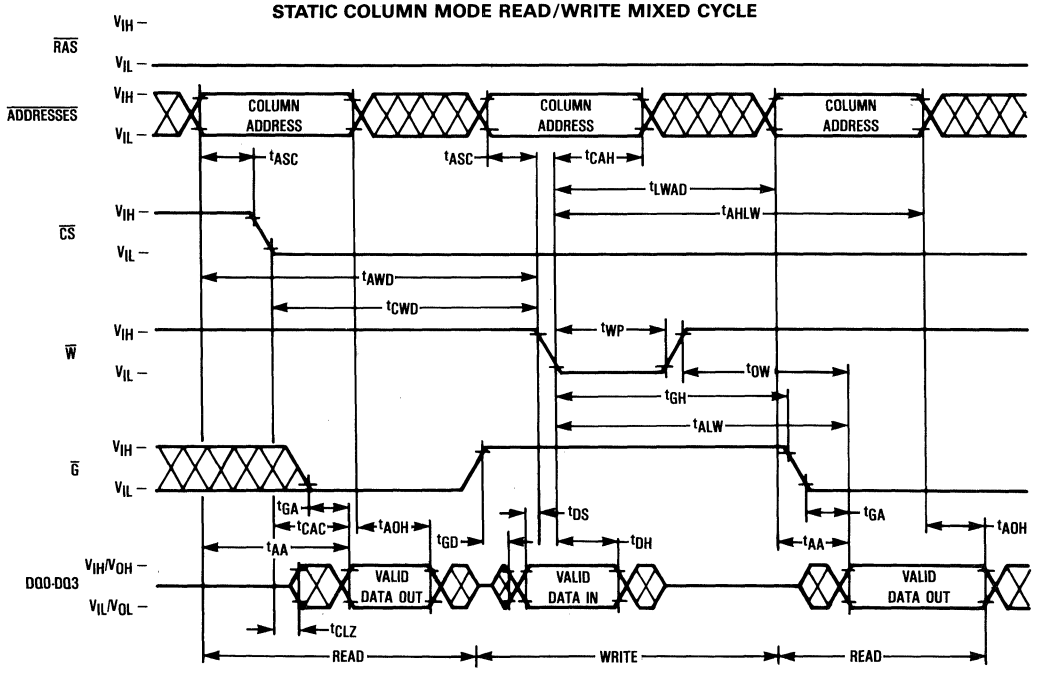


2

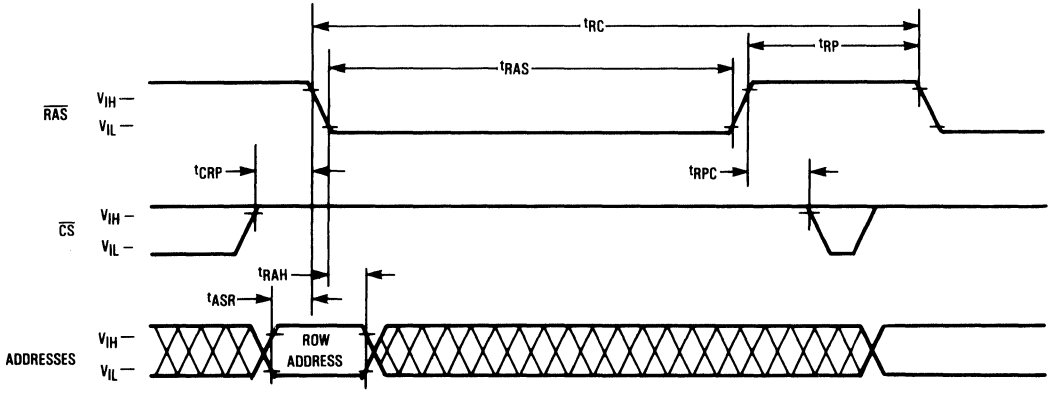
STATIC COLUMN MODE READ-MODIFY-WRITE CYCLE



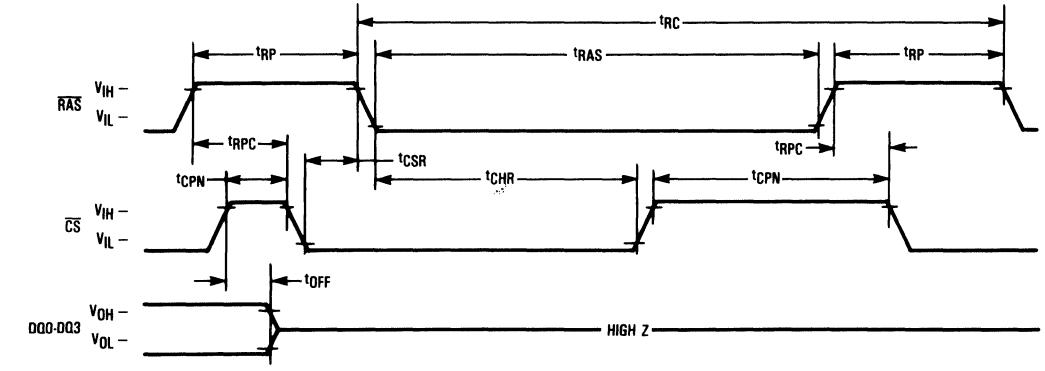
STATIC COLUMN MODE READ/WRITE MIXED CYCLE



$\overline{RAS}$ ONLY REFRESH CYCLE
($\overline{W}$ and $\overline{G}$ are Don't Care)

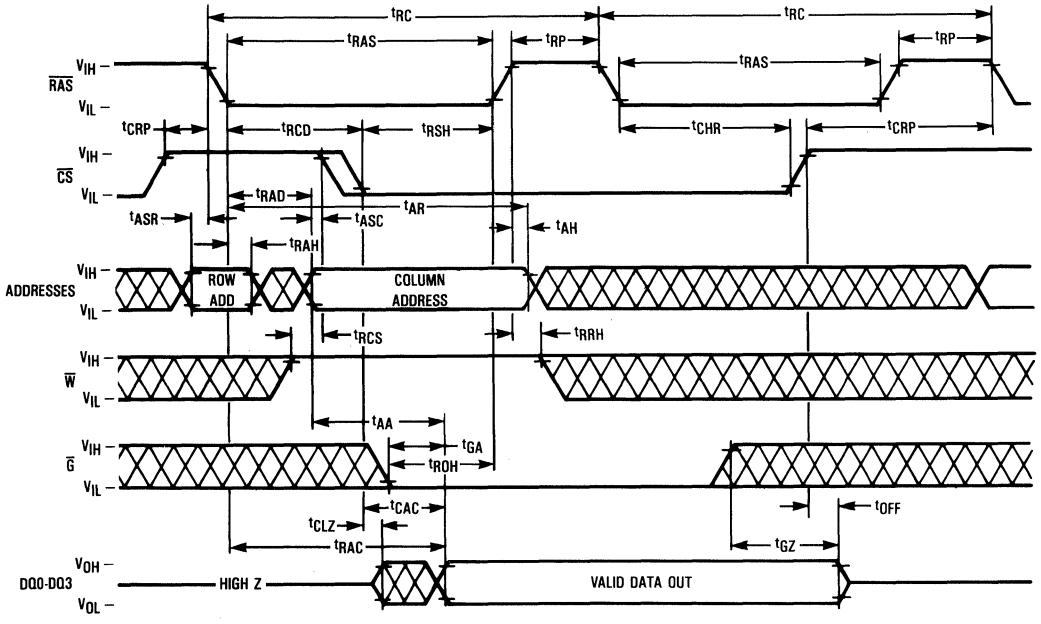


$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE
($\overline{W}$, $\overline{G}$, and A0-A8 are Don't Care)

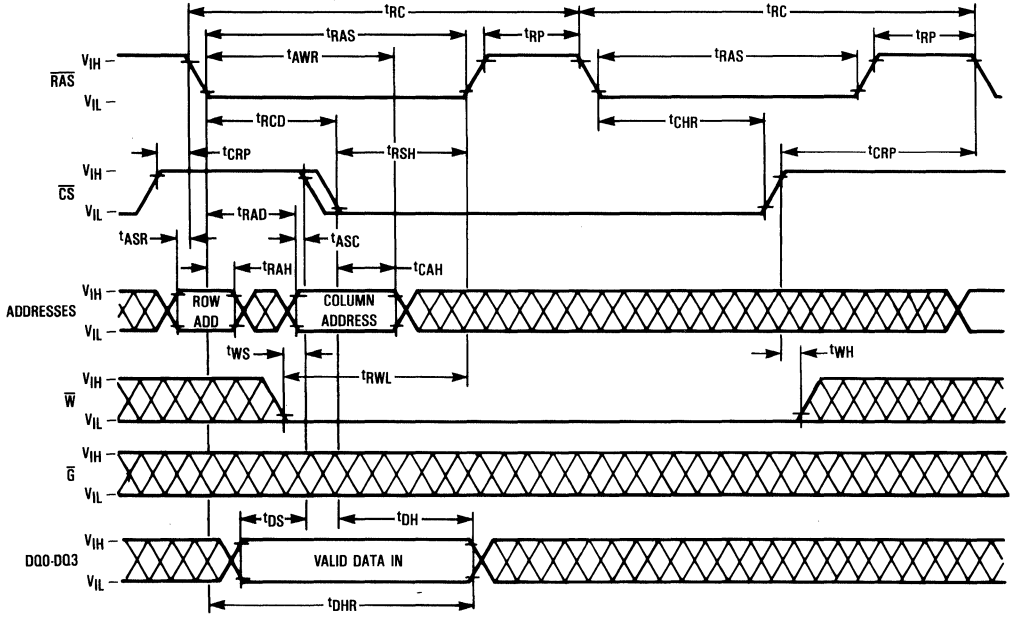


2

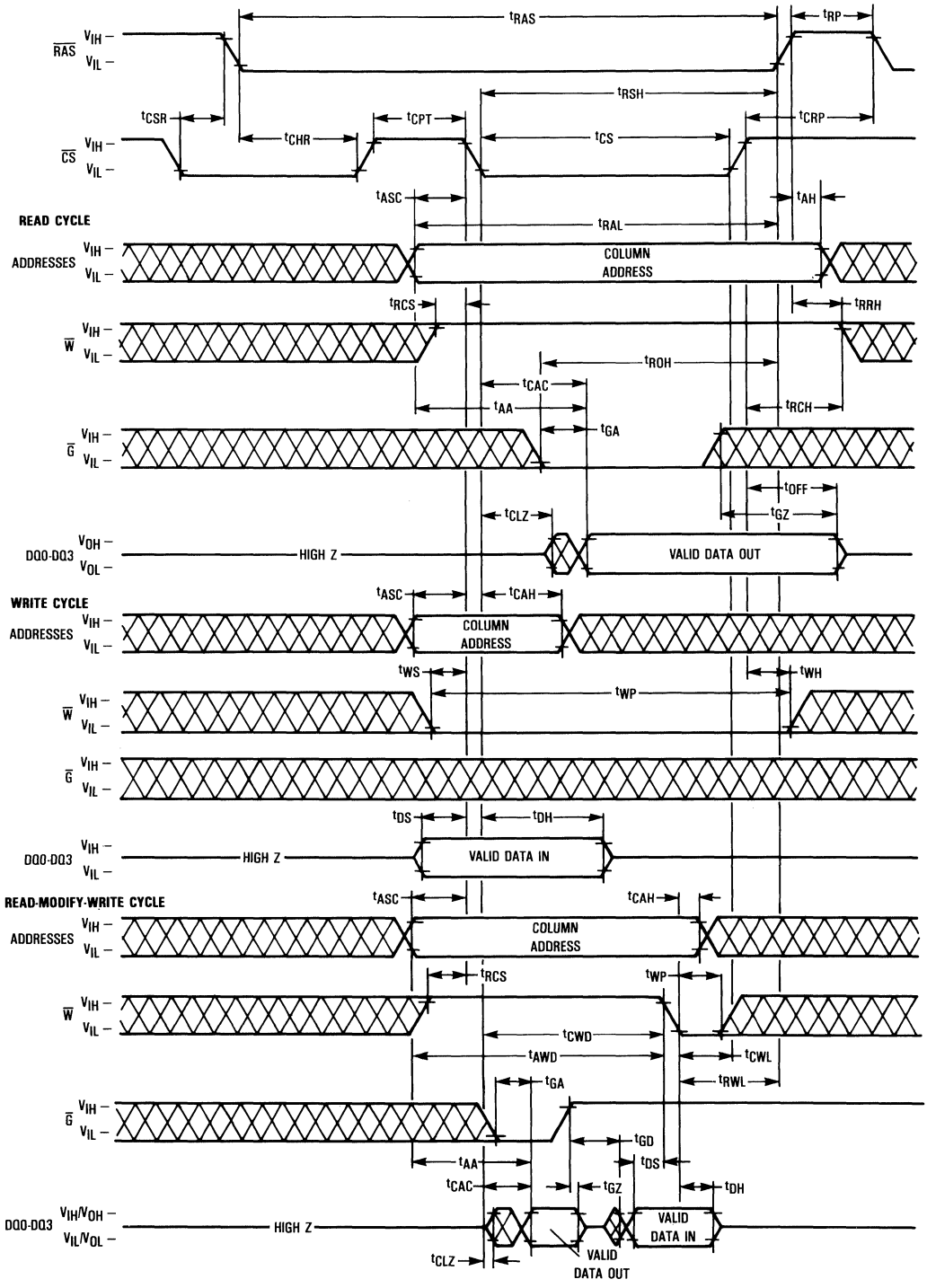
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power-up an initial pause of 200 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 4 milliseconds with device powered up), the wake up sequence (8 active cycles) will be necessary to assure proper device operation.

ADDRESSING THE RAM

The nine address pins on the device are time multiplexed with two separate 9-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe ($\overline{RAS}$) and the column address strobe ($\overline{CS}$). A total of 18 address bits will decode one of the 262,144 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, other variations in addressing the RAM, the refresh modes ($\overline{RAS}$ only refresh; $\overline{CS}$ before $\overline{RAS}$ refresh; hidden refresh), another mode called static column mode allows the user to column access the 512 bits within a selected row. The refresh mode and static column mode operations are described in more detail later on.

READ CYCLE

A read cycle is referred to as a normal read cycle to differentiate it from a static column mode read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CS}$ clock must be active before or at the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CS}$ clock active transition will determine read access time. The external $\overline{CS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This gating feature on the $\overline{CS}$ clock will allow the external $\overline{CS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CS}) period for the $\overline{CS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CS}$ and $\overline{G}$ clocks are active; the output will switch to the three-state mode when either the $\overline{CS}$ or $\overline{G}$ clock goes inactive. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as an early write cycle. In an early write cycle, the write clock and the data in are referenced to the active transition of the $\overline{CS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisfied before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CS}$ clock. This time could be as long as 10 microseconds—$[t_{RWL} + t_{RP} + 2t_T]$.

In a late write or a ready-modify-write cycle, $\overline{G}$ must be at the V_{IH} level to bring the output buffers to high impedance prior to data-in being valid.

At the start of an early write cycle, the data out is in a high impedance condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CS}$ clock from enabling the data-out buffers. The three-state condition (high impedance) of the data out pin during a write cycle can be effectively utilized in systems that have a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE CYCLE

As the name implies, both a read and a write cycle are accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

STATIC COLUMN MODE CYCLES

Output buffers are always on when the device is in the static column mode and $\overline{CS}$ clock is not cycled, resulting in fewer transients and simpler operation. The static column mode allows faster access (t_{AA}) to any of the 512 column addresses on a given row, typically at half the standard (t_{RAC}) rate for randomly performed operations. Static column mode operation consists of changing column addresses while holding the $\overline{RAS}$ and $\overline{CS}$ clocks active. A new column location can be accessed with each static column cycle (t_{SC}).

Static column mode operation is initiated with a standard read or write cycle. The row address is latched by the $\overline{RAS}$ clock transition to active, followed by column addresses and $\overline{CS}$ clock. Performing an address cycle (t_{SC}) while $\overline{RAS}$ and $\overline{CS}$ clocks remain active constitutes the first static column cycle. Subsequent static column cycles can be performed as long as the $\overline{RAS}$ and $\overline{CS}$ clocks are held active. The first access (data out) occurs at the standard (t_{RAC}) rate. All of the read operations in static column mode following the initial operation are measured at the faster rate (t_{AA}), provided all other timing minimums are maintained. Static column cycle time determines how fast successive bits are read.

Any combination of read, write, or read-modify-write operations can be performed in the static column mode. The conditions normal to each operation apply when the device is operated in this mode.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 8 milliseconds. This is accomplished by sequentially cycling through the 512 row address locations every 8 milliseconds, (i.e., at least one row every 15.6 microseconds). A normal read or write operation to the RAM will serve to refresh all the bits associated with the particular rows decoded.

$\overline{RAS}$-Only Refresh

In this refresh method, the system must perform a $\overline{RAS}$-only cycle on 512 row addresses every 8 milliseconds. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CS}$ clock is not required and must be inactive or at a V_{IH} level.

$\overline{CS}$ Before $\overline{RAS}$ Refresh

$\overline{CS}$ before $\overline{RAS}$ refreshing available on the MCM514258 offers an alternate refresh method. If $\overline{CS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place.

After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh

An optional feature of the MCM514258 is that refresh cycle may be performed while maintaining valid data at the output pin. This is referred to as Hidden Refresh. Hidden Refresh is performed by holding $\overline{CS}$ at V_{IL} and taking $\overline{RAS}$ high and after a specified precharge period (t_{RP}), executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle. (see Figure 1 below)

$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh operation of MCM514258 can be tested by $\overline{CS}$ before $\overline{RAS}$ refresh counter test. This cycle performs read/write operation taking the internal counter address as row address and the input address as column address.

The test is performed after a minimum of 8 $\overline{CS}$ before $\overline{RAS}$ cycles as initialization cycles. The test procedure is as follows.

1. Write a "0" into all memory cells.
2. Select any column address and read the "0"s written in step 1. Write a "1" into each cell of the selected column by performing $\overline{CS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
3. Read the "1"s (use a normal read mode) written in step 2.
4. Select the same column address as step 2, read the "1"s and write a "0" into each cell by performing $\overline{CS}$ before $\overline{RAS}$ Refresh Counter Test Read-Write Cycle (see timing diagram). Repeat 512 times.
5. Read the "0"s (use a normal read mode) written in step 4.
6. Repeat steps 1 through 5 using complement data.

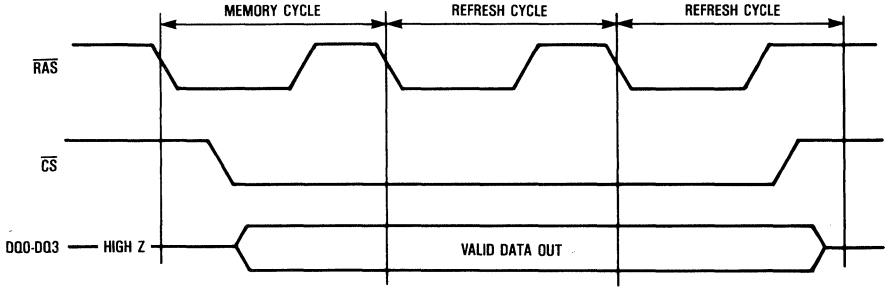
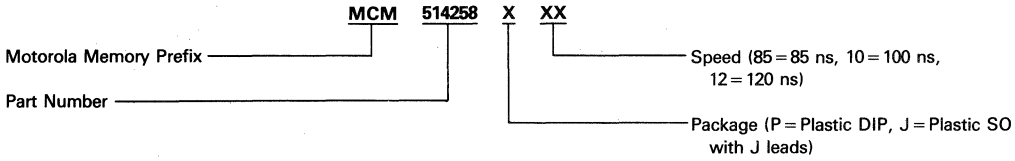


Figure 1. Hidden Refresh Cycle

2

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—MCM514258P85 MCM514258J85
MCM514258P10 MCM514258J10
MCM514258P12 MCM514258J12

General MOS Static RAMs 3

MOS Static RAMs

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
2K × 8	MCM2016HN45 (1)	45	24
	MCM2016HN55 (1)	55	24
	MCM2016HN70 (1)	70	24
	MCM2018N35 (1)	35	24
	MCM2018N45 (1)	45	24

(1) 300 mil package.

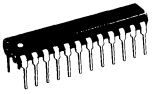
CMOS Static RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Access Time (ns max)	Pins
8K × 8	MCM6064P10	100	28
	MCM6064P12	120	28
	MCM6064P15	150	28
	MCM60L64P10	100	28
	MCM60L64P12	120	28
	MCM60L64P15	150	28
32K × 8	MCM60256P85	85	28
	MCM60256P10	100	28
	MCM60256P12	120	28
	MCM60L256P85	85	28
	MCM60L256P10	100	28
	MCM60L256P12	120	28

MCM2016H

Fast 16K Bit Static RAM



N PACKAGE
PLASTIC
CASE 724

3

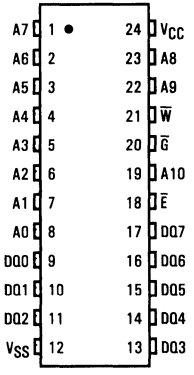
The MCM2016H is a 16,384 bit static random access memory organized as 2048 words by 8 bits, fabricated using Motorola's high-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are longer than access times. Perfect for cache and sub-100 ns buffer memory systems, this high speed static RAM is intended for applications that demand superior performance and reliability.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings.

The MCM2016H is in a 24-pin dual-in-line 300 mil wide plastic package with the industry standard JEDEC approved pinout.

- Single +5 V Operation, ±10%
- Fully Static: No Clock or Timing Strobe Required
- Fast Access Time: MCM2016H-45 = 45 ns (Maximum)
  MCM2016H-55 = 55 ns (Maximum)
  MCM2016H-70 = 70 ns (Maximum)
- Power Supply Current: 135 mA Maximum (Active)
  20 mA Maximum (Standby)
- Three-State Output

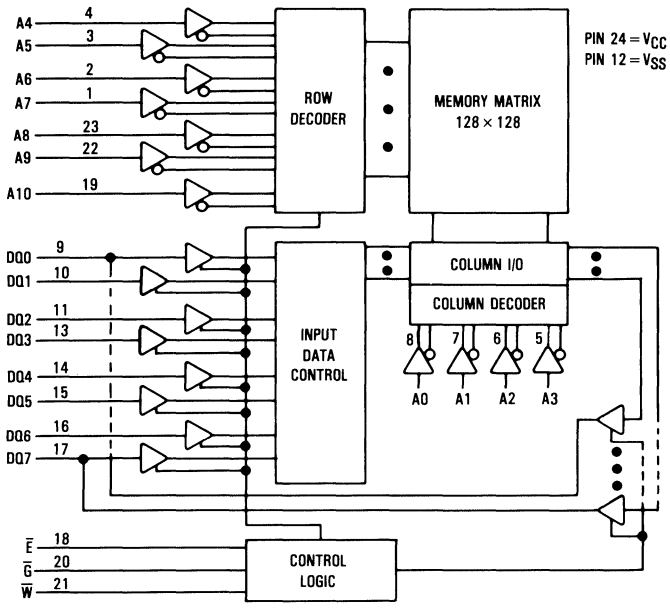
PIN ASSIGNMENT



PIN NAMES

A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



MODE SELECTION

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	V_{CC} Current	DQ
Standby	H	X	X	I_{SB}	High Z
Read	L	L	H	I_{CC}	Q
Write Cycle	L	X	L	I_{CC}	D

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage on Any Pin With Respect to V_{SS}	V_{in}, V_{out}	−0.5 to +7.0	V
DC Output Current	I_{out}	±20	mA
Power Dissipation	P_D	1.1	Watt
Temperature Under Bias	T_{bias}	−10 to +80	°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage (50 ns Maximum Address Rise and Fall Times, while the chip is selected)	V_{IH}	2.2	3.0	6.0	V
	V_{IL}	−0.5*	0	0.8	V

*The device will withstand undershoots to the −2.5 volt level with a maximum pulse width of 50 ns. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{CC} = 5.5 V, V_{in} = GND to V_{CC})	$I_{lkg(I)}$	−1.0	1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC})	$I_{lkg(O)}$	−1.0	1.0	μA
Operating Power Supply Current ($\overline{E}$ = V_{IL}, $I_{I/O}$ = 0 mA)	I_{CC}	—	135	mA
Standby Power Supply Current ($\overline{E}$ = V_{IH})	I_{SB}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$ and DQ	C_{in}	3	5	pF
	$\overline{E}$		5	7	
I/O Capacitance	DQ	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

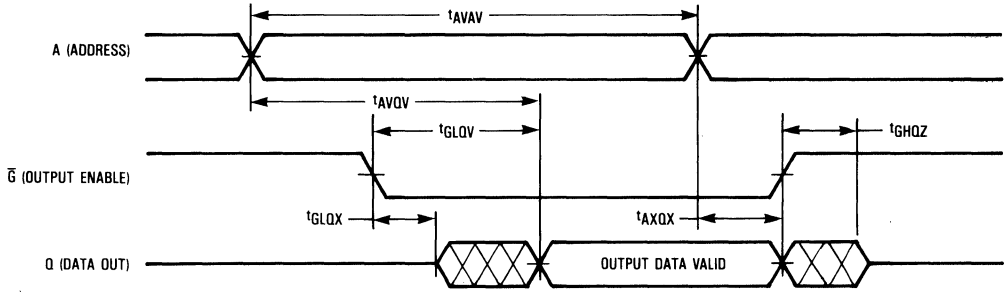
Input Pulse Levels . . . . . 0 and 3.0 V
Input Rise and Fall Times . . . . . 5 ns
Input and Output Timing Measurement Reference Levels . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

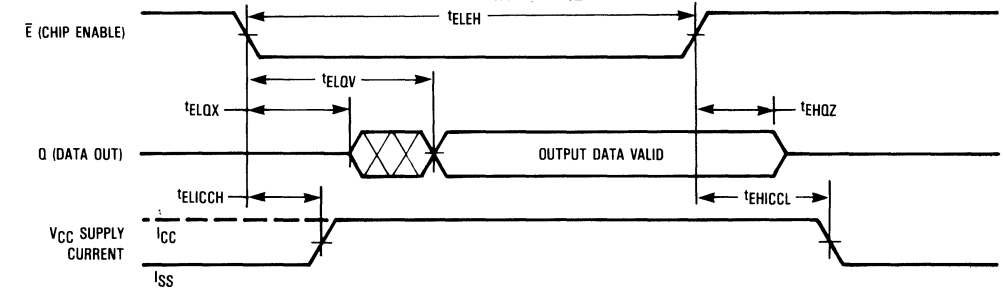
Parameter	Symbol		MCM2016H-45		MCM2016H-55		MCM2016H-70		Units	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Address Valid to Address Valid (Read Cycle Time)	t_{AVAV}	t_{RC}	45	–	55	–	70	–	ns	
Address Valid to Output Valid (Address Access Time)	t_{AVQV}	t_{AC}	–	45	–	55	–	70	ns	
Chip Enable Low to Chip Enable High (Read Cycle Time)	t_{ELEH}	t_{RC}	45	–	55	–	70	–	ns	
Chip Enable Low to Output Valid (Chip Enable Access Time)	t_{ELQV}	t_{ACS}	–	45	–	55	–	70	ns	
Output Enable Low to Output Valid (Output Enable Access Time)	t_{GLQV}	t_{OE}	–	20	–	25	–	30	ns	
Chip Enable Low to Output Invalid (Chip Enable to Output Active)	t_{ELQX}	t_{CLZ}	5	–	5	–	5	–	ns	2
Chip Enable High to Output High Z (Chip Disable to Output Disable)	t_{EHQZ}	t_{CHZ}	0	20	0	20	0	20	ns	2
Output Enable Low to Output Invalid (Output Enable to Output Active)	t_{GLQX}	t_{OLZ}	0	–	0	–	0	–	ns	2
Output Enable High to Output High Z (Output Disable to Output Disable)	t_{GHQZ}	t_{OHZ}	0	20	0	20	0	20	ns	2
Address Invalid to Output Invalid (Output Hold Time)	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns	
Chip Enable Low to Power Up	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	ns	
Chip Enable High to Power Down	t_{EHICCL}	t_{PD}	–	20	–	20	–	20	ns	

NOTES:
1. Transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
2. Transition is measured ±200 mV from the steady state output voltage with the output loading specified in Figure 1.
3. In read cycle 2, all addresses are valid prior to or coincident with chip enable ($\overline{E}$) transition low.

READ CYCLE 1 ($\overline{W} = V_{IH}$, $\overline{E} = V_{IL}$)



READ CYCLE 2 ($\overline{W} = V_{IH}$, $\overline{G} = V_{IL}$; See Note 3 Above)

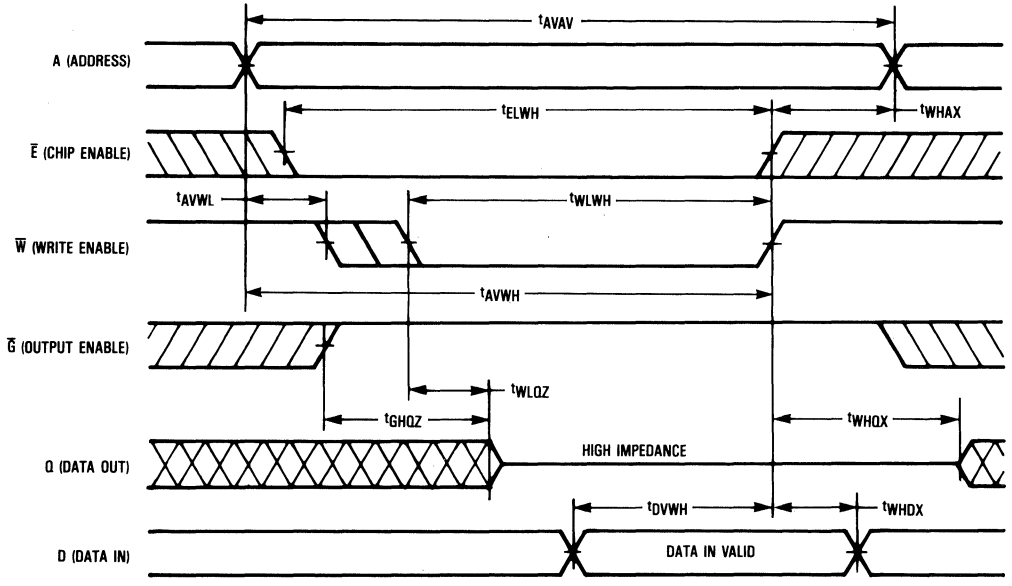


WRITE CYCLE (See Notes 1 and 2)

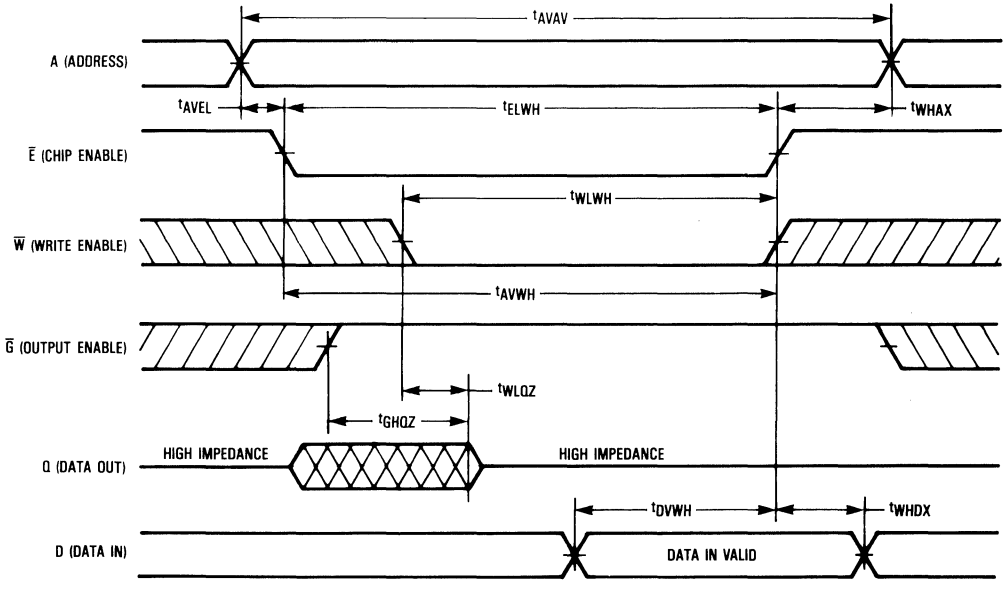
Parameter	Symbol		MCM2016H-45		MCM2016H-55		MCM2016H-70		Units	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	45	–	55	–	70	–	ns	
Chip Enable Low to Write High (Chip Enable to End of Write)	t_{ELWH}	t_{EW}	40	–	50	–	65	–	ns	
Address Valid to Chip Enable Low (Address Setup to Chip Enable)	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to Write Low (Address Setup to Write)	t_{AVWL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to Write High	t_{AVWH}	t_{AW}	40	–	50	–	65	–	ns	3
Write Low to Write High (Write Pulse Width)	t_{WLWH}	t_{WP}	35	–	40	–	40	–	ns	
Write High to Address Don't Care (Address Hold After End of Write)	t_{WHAX}	t_{WR}	0	–	0	–	0	–	ns	4
Write High to Output Don't Care (Output Active After End of Write)	t_{WHQX}	t_{WLZ}	0	–	0	–	0	–	ns	5
Write Low to Output High Z (Write Enable to Output Disable)	t_{WLQZ}	t_{WHZ}	0	20	0	20	0	20	ns	5
Data Valid to Write High (Data Setup to End of Write)	t_{DVWH}	t_{DS}	20	–	25	–	30	–	ns	3
Write High to Data Don't Care (Data Hold After End of Write)	t_{WHDX}	t_{DH}	0	–	0	–	0	–	ns	3, 5
Output Enable High to Output High Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	0	20	ns	

NOTES:
1. Write enable ($\overline{W}$) must be high during all address transitions.
2. If the chip enable ($\overline{E}$) low transition occurs simultaneously with the write enable ($\overline{W}$) transition, the output remains in a high impedance state.
3. Both chip enable ($\overline{E}$) and write enable ($\overline{W}$) must be active (low) to write data into the memory. Either signal can terminate the write cycle by going high. Data in setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
4. t_{WHAX} is measured from the earlier of, chip enable ($\overline{E}$) or write enable ($\overline{W}$) going high to the end of write cycle.
5. Output enable ($\overline{G}$) can be either low or high during a write cycle. If chip enable ($\overline{E}$) and $\overline{G}$ are both low during this period then the data input/output (DQ) pins are in the output state. Under these conditions input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{E}$ Controlled)



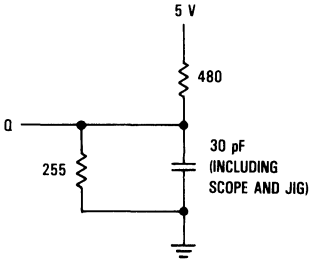
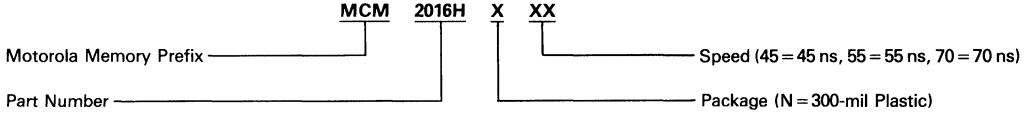


Figure 1. Output Load

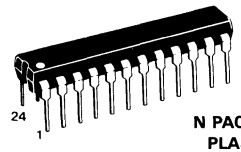
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM2016HN45 MCM2016HN55 MCM2016HN70

MCM2018

Fast 16K Bit Static RAM



N PACKAGE
PLASTIC
CASE 724

3

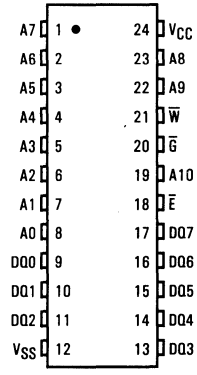
The MCM2018 is a 16,384 bit static random access memory organized as 2048 words by 8 bits, fabricated using Motorola's high-performance silicon-gate MOS (HMOS) technology. It uses an innovative design approach which combines the ease-of-use features of fully static operation (no external clocks or timing strobes required) with the reduced standby power dissipation associated with clocked memories. To the user this means low standby power dissipation without the need for address setup and hold times, nor reduced data rates due to cycle times that are longer than access times. Perfect for cache and sub-100 ns buffer memory systems, this high speed static RAM is intended for applications that demand superior performance and reliability.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings.

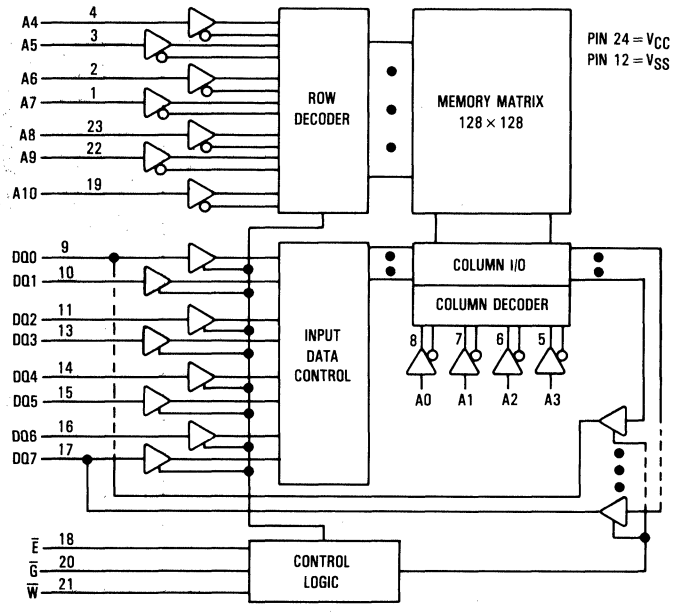
The MCM2018 is in a 24-pin dual-in-line 300 mil wide package with the industry standard JEDEC approved pinout.

- Single +5 V Operation, ±10%
- Fully Static: No Clock or Timing Strobe Required
- Fast Access Time: MCM2018-35 = 35 ns (Maximum)
  MCM2018-45 = 45 ns (Maximum)
- Power Supply Current: 135 mA Maximum (Active)
  20 mA Maximum (Standby)
- Three-State Output

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A10	Address Input
DQ0-DQ7	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
V_{CC}	+5 V Power Supply
V_{SS}	Ground

MODE SELECTION

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	V_{CC} Current	DQ
Standby	H	X	X	I_{SB}	High Z
Read	L	L	H	I_{CC}	Q
Write Cycle	L	X	L	I_{CC}	D

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

3

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage on Any Pin With Respect to V_{SS}	V_{in}, V_{out}	−0.5 to +7.0	V
DC Output Current	I_{out}	±20	mA
Power Dissipation	P_D	1.1	Watt
Temperature Under Bias	T_{bias}	−10 to +80	°C
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage (50 ns Maximum Address Rise and Fall Times, While the Chip is Selected)	V_{IH}	2.0	3.0	6.0	V
	V_{IL}	−0.5*	0	0.8	V

*The device will withstand undershoots to the −2.5 volt level with a maximum pulse width of 50 ns. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (V_{CC} = 5.5 V, V_{in} = GND to V_{CC})	$I_{lkg(I)}$	−1.0	1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, $V_{I/O}$ = GND to V_{CC})	$I_{lkg(O)}$	−1.0	1.0	μA
Operating Power Supply Current ($\overline{E}$ = V_{IL}, $I_{I/O}$ = 0 mA)	I_{CC}	—	135	mA
Standby Power Supply Current ($\overline{E}$ = V_{IH})	I_{SB}	—	20	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$ and DQ	C_{in}	3	5	pF
	$\overline{E}$		5	7	
I/O Capacitance	DQ	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

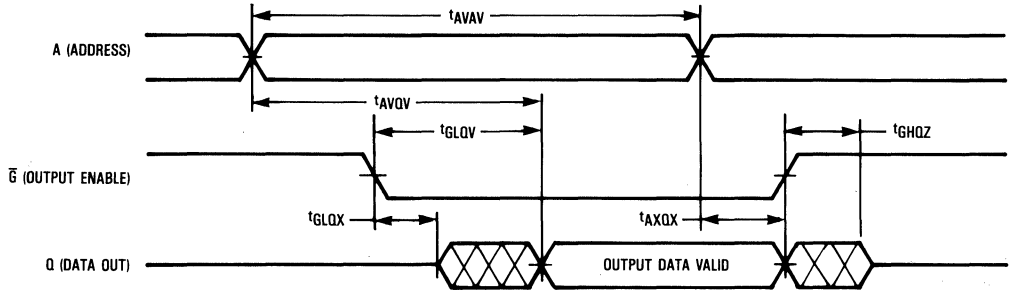
Input Pulse Levels . . . . . 0 and 3.0 V
Input Rise and Fall Times . . . . . 5 ns
Input and Output Timing Measurement Reference Levels . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

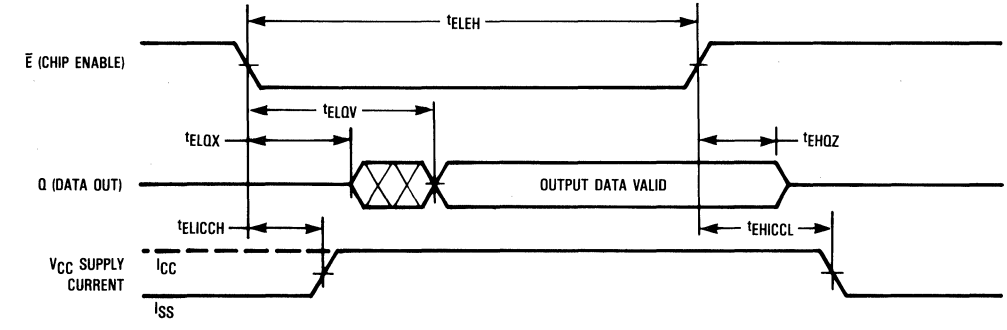
Parameter	Symbol		MCM2018-35		MCM2018-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Address Valid to Address Valid (Read Cycle Time)	t_{AVAV}	t_{RC}	35	–	45	–	ns	
Address Valid to Output Valid (Address Access Time)	t_{AVQV}	t_{AC}	–	35	–	45	ns	
Chip Enable Low to Chip Enable High (Read Cycle Time)	t_{ELEH}	t_{RC}	35	–	45	–	ns	
Chip Enable Low to Output Valid (Chip Enable Access Time)	t_{ELQV}	t_{ACS}	–	35	–	45	ns	
Output Enable Low to Output Valid (Output Enable Access Time)	t_{GLQV}	t_{OE}	–	20	–	20	ns	
Chip Enable Low to Output Invalid (Chip Enable to Output Active)	t_{ELQX}	t_{CLZ}	5	–	5	–	ns	2
Chip Enable High to Output High Z (Chip Disable to Output Disable)	t_{EHQZ}	t_{CHZ}	0	20	0	20	ns	2
Output Enable Low to Output Invalid (Output Enable to Output Active)	t_{GLQX}	t_{OLZ}	0	–	0	–	ns	2
Output Enable High to Output High Z (Output Disable to Output Disable)	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	2
Address Invalid to Output Invalid (Output Hold Time)	t_{AXQX}	t_{OH}	5	–	5	–	ns	
Chip Enable Low to Power Up	t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Chip Enable High to Power Down	t_{EHICCL}	t_{PD}	–	20	–	20	ns	

NOTES:
1. Transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IL} and V_{IH} (or between V_{IH} and V_{IL}) in a monotonic manner.
2. Transition is measured ±200 mV from the steady state output voltage with the output loading specified in Figure 1.
3. In read cycle 2, all addresses are valid prior to or coincident with chip enable ($\overline{E}$) transition low.

READ CYCLE 1 ($\overline{W} = V_{IH}$, $\overline{E} = V_{IL}$)



READ CYCLE 2 ($\overline{W} = V_{IH}$, $\overline{G} = V_{IL}$; See Note 3 Above)

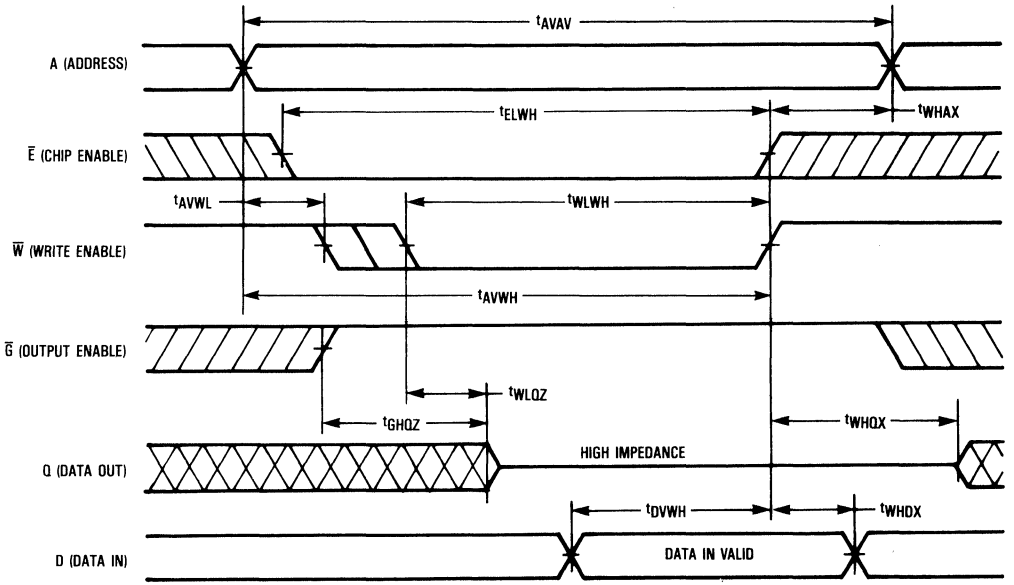


WRITE CYCLE (See Notes 1 and 2)

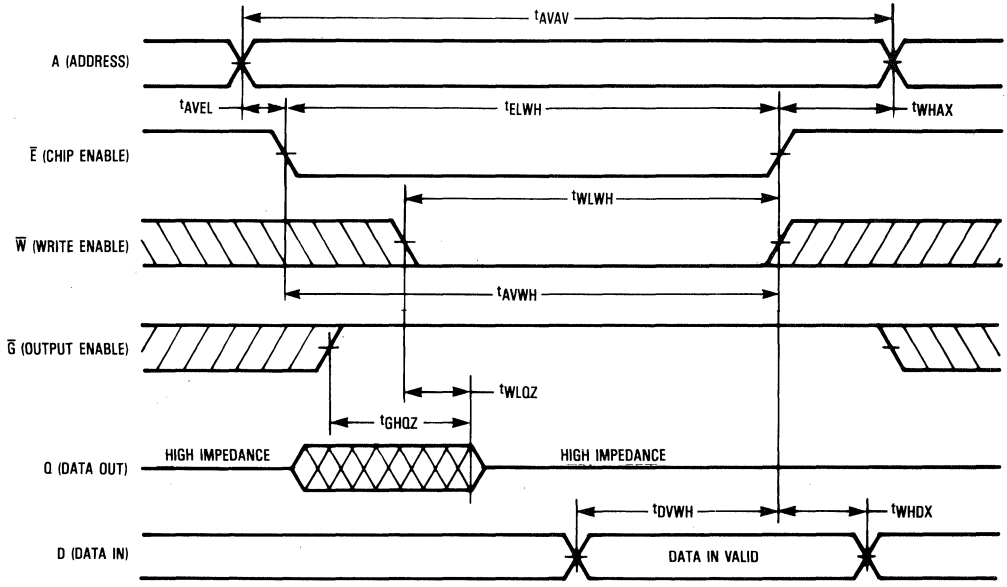
Parameter	Symbol		MCM2018-35		MCM2018-45		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Address Valid to Address Valid (Write Cycle Time)	t_{AVAV}	t_{WC}	35	–	45	–	ns	
Chip Enable Low to Write High (Chip Enable to End of Write)	t_{ELWH}	t_{EW}	30	–	40	–	ns	
Address Valid to Chip Enable Low (Address Setup to Chip Enable)	t_{AVEL}	t_{AS}	0	–	0	–	ns	
Address Valid to Write Low (Address Setup to Write)	t_{AVWL}	t_{AS}	0	–	0	–	ns	
Address Valid to Write High	t_{AVWH}	t_{AW}	30	–	40	–	ns	3
Write Low to Write High (Write Pulse Width)	t_{WLWH}	t_{WP}	30	–	35	–	ns	
Write High to Address Don't Care (Address Hold After End of Write)	t_{WHAX}	t_{WR}	0	–	0	–	ns	4
Write High to Output Don't Care (Output Active After End of Write)	t_{WHQX}	t_{WLZ}	0	–	0	–	ns	5
Write Low to Output High Z (Write Enable to Output Disable)	t_{WLQZ}	t_{WHZ}	0	20	0	20	ns	5
Data Valid to Write High (Data Setup to End of Write)	t_{DVWH}	t_{DS}	15	–	20	–	ns	3
Write High to Data Don't Care (Data Hold After End of Write)	t_{WHDX}	t_{DH}	0	–	0	–	ns	3, 5
Output Enable High to Output High Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	

NOTES:
1. Write enable ($\overline{W}$) must be high during all address transitions.
2. If the chip enable ($\overline{E}$) low transition occurs simultaneously with the write enable ($\overline{W}$) transition, the output remains in a high impedance state.
3. Both chip enable ($\overline{E}$) and write enable ($\overline{W}$) must be active (low) to write data into the memory. Either signal can terminate the write cycle by going high. Data in setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
4. t_{WHAX} is measured from the earlier of, chip enable ($\overline{E}$) or write enable ($\overline{W}$) going high to the end of write cycle.
5. Output enable ($\overline{G}$) can be either low or high during a write cycle. If chip enable ($\overline{E}$) and $\overline{G}$ are both low during this period then the data input/output (DQ) pins are in the output state. Under these conditions input signals of opposite phase to the outputs must not be applied.

WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{E}$ Controlled)



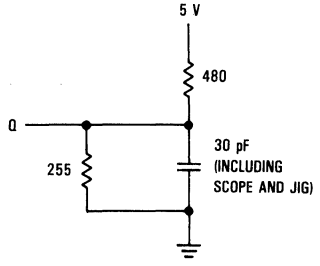
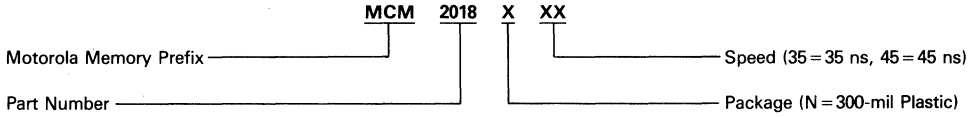


Figure 1. Output Load

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM2018N35
MCM2018N45

MCM6064
MCM60L64

Advance Information

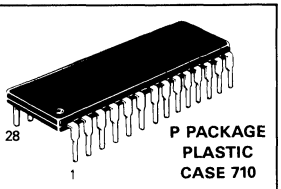
8K x 8 Bit CMOS Static Random Access Memory

The MCM6064 is a 65,536 bit low-power static random access memory organized as 8192 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The maximum operating current is 5 mA/MHz and corresponding maximum power consumption is 27.5 mW/MHz.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. For MCM6064 typical standby current is 3 μA, with a maximum of 100 μA. For MCM60L64 typical standby current is 0.6 μA, with maximum of 1.0 μA at 25°C. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

The MCM6064 is available in a 600 mil, 28 pin plastic dual-in-line package.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—248 mW (Maximum Active)
- Two Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (MCM60L64)
- Data Retention Supply Voltage = 2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Pin Compatible with 2764 EPROM Family
- Three State Outputs
- Fast Access Times: MCM6064-10 and MCM60L64-10 = 100 ns (Max)
  MCM6064-12 and MCM60L64-12 = 120 ns (Max)
  MCM6064-15 and MCM60L64-15 = 150 ns (Max)



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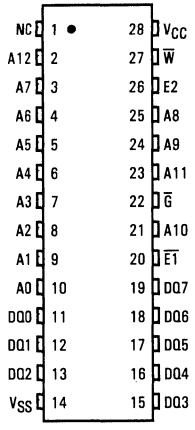
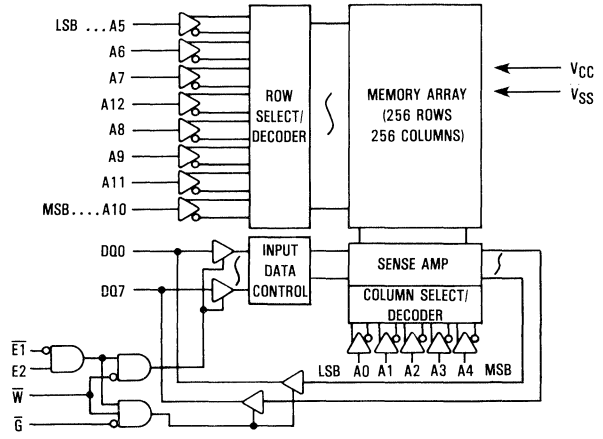
3

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	7	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC} + 0.5	V
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	<0.01	±1.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	<0.01	±1.0	μA
DC Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{in} = V_{IH} or V_{IL})	I_{CC}	—	—	10	mA
AC Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{in} = V_{IH} or V_{IL}, I_{out} = 0)	I_{CCA}				mA
MCM6064-10: t_{AVAV} = 100 ns		—	—	45	
MCM6064-12: t_{AVAV} = 120 ns		—	—	40	
MCM6064-15: t_{AVAV} = 150 ns		—	—	35	
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})	I_{SB1}	—	—	3.0	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 or E2 ≤ 0.2 V) MCM6064	I_{SB2}	—	3	100	μA
MCM60L64, T_A = 25°C		—	0.6	1.0	
T_A = 0 to 70°C		—	—	30	
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	—	—	V

CAPACITANCE (Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	—	6	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	—	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6064-10 MCM60L64-10		MCM6064-12 MCM60L64-12		MCM6064-15 MCM60L64-15		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	100	—	120	—	150	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	100	—	120	—	150	ns	—
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	—	100	—	120	—	150	ns	—
E2 Access Time	t_{E2HQV}	t_{AC2}	—	100	—	120	—	150	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	50	—	60	—	70	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	20	—	20	—	20	—	ns	—
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	10	—	10	—	15	—	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	—	5	—	5	—	ns	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	35	0	40	0	50	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	35	0	40	0	50	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

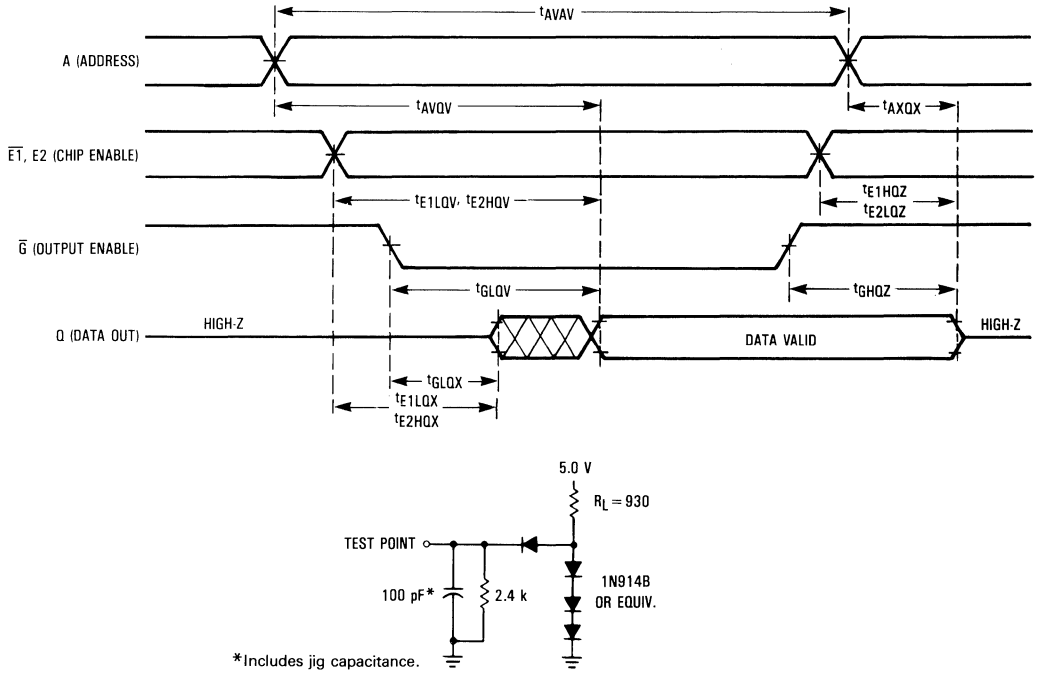
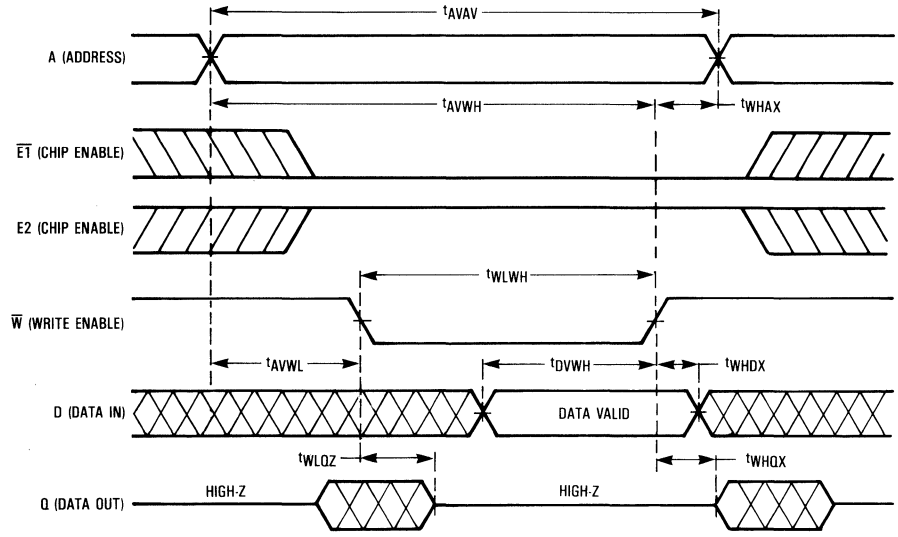


Figure 1. AC Test Load

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6064-10 MCM60L64-10		MCM6064-12 MCM60L64-12		MCM6064-15 MCM60L64-15		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	100	—	120	—	150	—	ns	—
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	—
Address Valid to End of Write	t_{AVWH}	t_{AW}	80	—	85	—	100	—	ns	—
Write Pulse Width	t_{WLWH}	t_{WP}	60	—	70	—	90	—	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	40	—	50	—	60	—	ns	—
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	35	0	40	0	50	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	—	5	—	10	—	ns	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	—

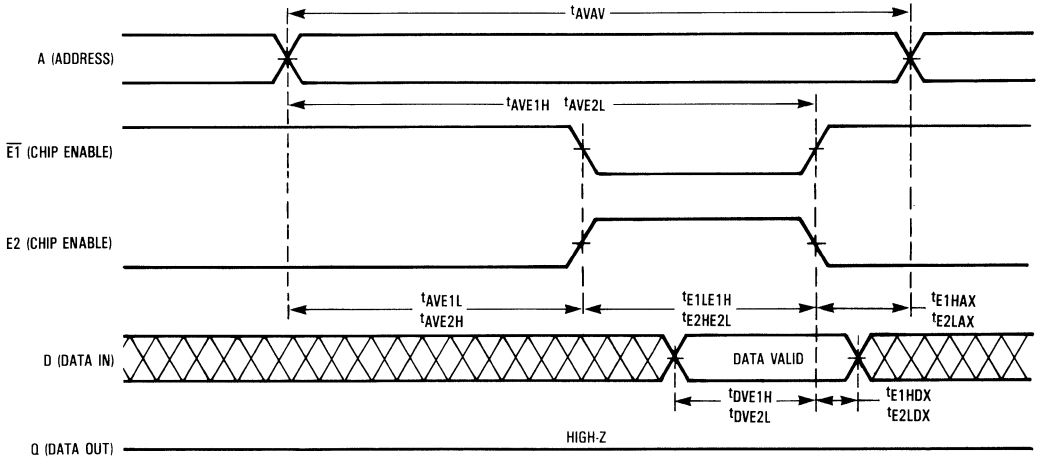
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are periodically sampled and not 100% tested.



WRITE CYCLE 2 ($\overline{E1}$, E2 CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6064-10 MCM60L64-10		MCM6064-12 MCM60L64-12		MCM6064-15 MCM60L64-15		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	100	—	120	—	150	—	ns	—
Address Setup Time	t_{AVE1L}, t_{AVE2H}	t_{AS}	0	—	0	—	0	—	ns	2
Address Valid to End of Write	t_{AVE1H}, t_{AVE2L}	t_{AW}	80	—	85	—	100	—	ns	2
Chip Enable to End of Write	t_{E1LE1H}, t_{E2HE2L}	t_{CW}	80	—	85	—	100	—	ns	2, 3
Data Valid to End of Write	t_{DVE1H}, t_{DVE2L}	t_{DW}	40	—	50	—	60	—	ns	2
Data Hold Time	t_{E1HDX}, t_{E2LDX}	t_{DH}	0	—	0	—	0	—	ns	2, 4
Write Recovery Time	t_{E1HAX}, t_{E2LAX}	t_{WR}	0	—	0	—	0	—	ns	2, 5

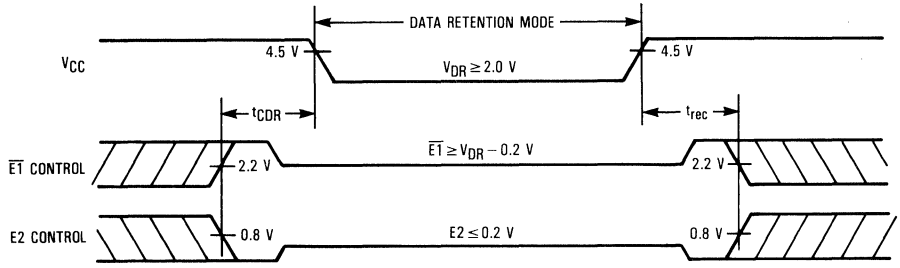
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
5. $\overline{W}$ must be high during all address transitions.



DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E1} \geq V_{CC} - 0.2$ V or E2 ≤ 0.2 V)	V_{DR}	2.0	—	5.5	V
Data Retention Current ($\overline{E1} \geq V_{CC} - 0.2$ or E2 ≤ 0.2 V)	I_{CCDR}				μA
MCM6064: V_{CC} = 3.0 V		—	—	50	
V_{CC} = 5.5 V		—	—	100	
MCM60L64: V_{CC} = 3.0 V		—	—	15	
V_{CC} = 5.5 V		—	—	30	
Chip Disable to Data Retention Time	t_{CDR}	0	—	—	ns
Operation Recovery Time	t_{rec}	t_{AVAV}*	—	—	ns

*t_{AVAV} = Read Cycle Time



ORDERING INFORMATION
(Order by Full Part Number)

MCM **6064 or 60L64** X XX

Motorola Memory Prefix

Part Number
(With L = Low Power Version)

Speed (10 = 100 ns, 12 = 120 ns, 15 = 150 ns)

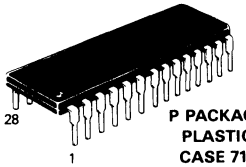
Package (P = Plastic)

Full Part Numbers — MCM6064P10, MCM6064P12, MCM6064P15, MCM60L64P10, MCM60L64P12, MCM60L64P15

MCM60256
MCM60L256

Advance Information

32K x 8 Bit CMOS Static Random Access Memory



P PACKAGE
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CASE 710

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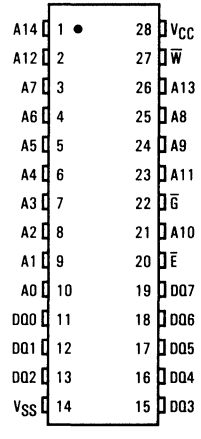
The MCM60256 is a 262,144 bit low-power static random access memory organized as 32,768 words of 8 bits, fabricated using silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. The operating current is 5 mA/MHz (typ) and the minimum cycle time is 85 ns.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. When $\overline{E}$ is a logic high, the part is placed in low power standby mode. The typical standby current for MCM60L256 is 2 μA. Chip enable also controls the data retention mode. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 40 ns (MCM60256-85). Thus the MCM60256 is suitable for use in various microprocessor application systems where high speed, low power, and battery backup are required.

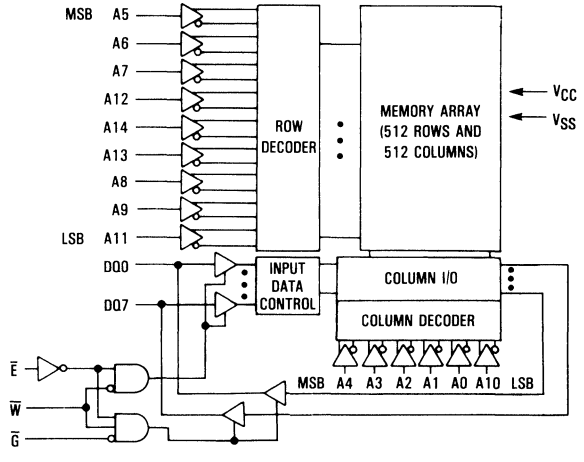
The MCM60256 is offered in a 600 mil, 28 pin plastic dual-in-line package.

- Single 5 V Supply, ± 10%
- 32K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Low Power Dissipation—27.5 mW/MHz (Typical Active)
- Two Chip Enable Inputs for More System Design Flexibility and Low Power Standby Mode
- Battery Backup Capability (MCM60L256)
- Data Retention Supply Voltage = 2.0 V to 5.5 V
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM60256-85 and MCM60L256-85 = 85 ns (Max)
  MCM60256-10 and MCM60L256-10 = 100 ns (Max)
  MCM60256-12 and MCM60L256-12 = 120 ns (Max)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.3 to 7.0	V
Voltage to Any Pin with Respect to V_{SS}	V_{in}, V_{out}	−0.5 to V_{CC} + 0.5	V
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤50 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	<0.01	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	<0.01	±1.0	μA
Operating Current (Read Cycle) ($\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IH}, Other Input = V_{IH}/V_{IL}, I_{out} = 0 mA)	I_{CCA1}				mA
MCM60256: t_{AVQV} = 1 μs		—	10	—	
MCM60256-85: t_{AVQV} = 85 ns		—	—	70	
MCM60256-10: t_{AVQV} = 100 ns		—	—	70	
MCM60256-12: t_{AVQV} = 120 ns		—	—	70	
($\overline{E}$ = 0.2 V, $\overline{W}$ = V_{CC} − 0.2 V, Other Input = V_{CC} − 0.2 V/0.2 V, I_{out} = 0 mA)	I_{CCA2}				
MCM60256: t_{AVQV} = 1 μs		—	5	—	
MCM60256-85: t_{AVQV} = 85 ns		—	—	60	
MCM60256-10: t_{AVQV} = 100 ns		—	—	60	
MCM60256-12: t_{AVQV} = 120 ns		—	—	60	
Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	—	—	3.0	mA
Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{CC} = 2.0 to 5.5 V) MCM60256	I_{SB2}	—	—	1.0	mA
MCM60L256		—	2	100	μA
Output Low Voltage (I_{OL} = 4.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	—	—	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance (V_{in} = 0 V)	All Inputs Except DQ	C_{in}	—	10	pF
I/O Capacitance ($V_{I/O}$ = 0 V)	DQ	$C_{I/O}$	—	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

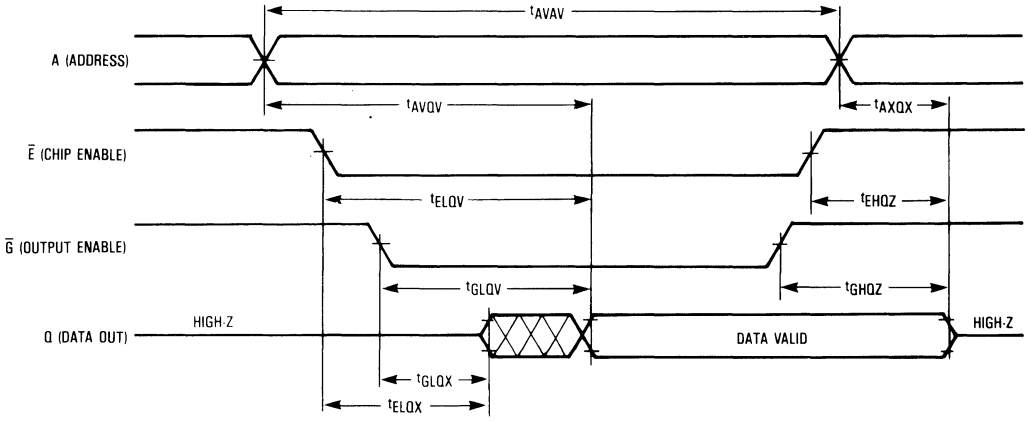
(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0.6 V, 2.4 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . .0.8 and 2.2 V
Output Load . . . . . See Figure 1

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM60256-85 MCM60L256-85		MCM60256-10 MCM60L256-10		MCM60256-12 MCM60L256-12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	85	—	100	—	120	—	ns	—
Address Access Time	t_{AVQV}	t_{AA}	—	85	—	100	—	120	ns	—
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	—	85	—	100	—	120	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	40	—	50	—	60	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	10	—	10	—	ns	—
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	—	10	—	10	—	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	—	5	—	5	—	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	30	0	50	0	60	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	30	0	40	0	50	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.



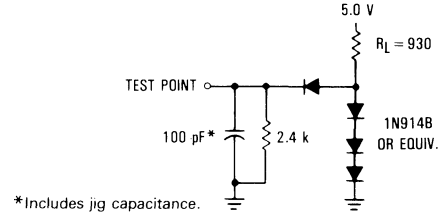


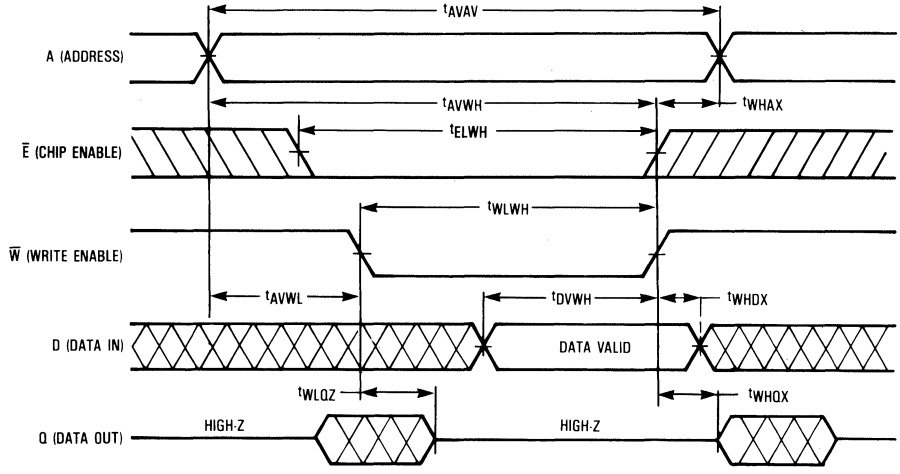
Figure 1. AC Test Load

WRITE CYCLE 1 AND 2 (See Note 1)

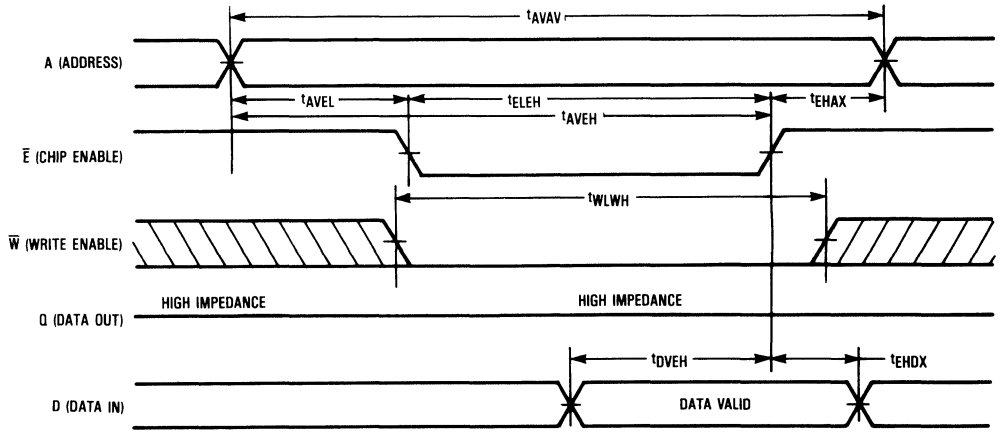
Parameter	Symbol	Alt Symbol	MCM60256-85 MCM60L256-85		MCM60256-10 MCM60L256-10		MCM60256-12 MCM60L256-12		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	85	–	100	–	120	–	ns	–
Address Setup Time	t_{AVWL}/t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}/t_{AVEH}	t_{AW}	75	–	90	–	100	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	60	–	70	–	80	–	ns	2
Data Valid to End of Write	t_{DVWH}/t_{DVEH}	t_{DW}	40	–	40	–	50	–	ns	–
Data Hold Time	t_{WHDX}/t_{EHOX}	t_{DH}	0	–	0	–	0	–	ns	–
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	30	0	50	0	60	ns	3, 4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	10	–	10	–	10	–	ns	3, 4
Write Recovery Time	t_{WHAX}/t_{EHAX}	t_{WR}	10	–	10	–	10	–	ns	5
Chip Enable to End of Write	t_{ELWH}/t_{ELEH}	t_{CW}	65	–	90	–	100	–	ns	–

NOTES:
1. Outputs are in high impedance state if $\overline{G}$ is high during Write Cycle.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{E}$ and a low $\overline{W}$. If $\overline{W}$ goes low prior to $\overline{E}$ low then outputs will remain in a high impedance state.
3. All high-Z and low-Z parameters are considered in a high or low impedance state when the outputs have made a 500 mV transition from the previous steady state voltage.
4. These parameters are periodically sampled and not 100% tested.
5. t_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of write cycle.

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED)



WRITE CYCLE 2 ($\overline{E}$ Controlled)

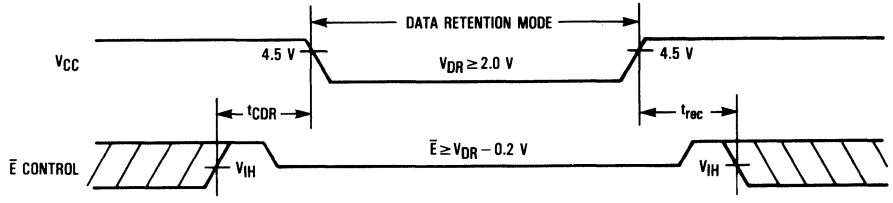


DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

Parameter		Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E} \geq V_{CC} - 0.2$ V)		V_{DR}	2.0	–	5.5	V
Data Retention Current ($\overline{E} \geq V_{CC} - 0.2$ V)	MCM60256	I_{CCDR}	–	–	1.0	mA
	MCM60L256: V_{CC} = 3.0 V		–	–	50	μA
	V_{CC} = 5.5 V		–	–	100	μA
Chip Disable to Data Retention Time		t_{CDR}	0	–	–	ns
Operation Recovery Time		t_{rec}	t_{AVAV}*	–	–	ns

*t_{AVAV} = Read Cycle Time

DATA RETENTION MODE



NOTE: If the V_{IH} of $\overline{E}$ is 2.4 V in operation, I_{SB1} current flows during the period that the V_{CC} voltage is decreasing from 4.5 V to 2.4 V.

ORDERING INFORMATION
(Order by Full Part Number)

MCM 60256 or 60L256 X XX

- MCM — Motorola Memory Prefix
- 60256 or 60L256 — Part Number (With L = Low Power Version)
- X — Package (P = Plastic)
- XX — Speed (85 = 85 ns, 10 = 100 ns, 12 = 120 ns)

Full Part Numbers — MCM60256P85, MCM60256P10, MCM60256P12, MCM60L256P85, MCM60L256P10, MCM60L256P12

CMOS Fast Static RAMs

4

CMOS Fast Static RAMs

(+5 V, 0 to 70°C unless otherwise noted)

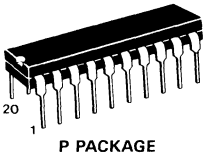
Organization	Part Number	Access Time (ns max)	Pins
4K × 4	MCM1423P45	40	20
	IMS1423P-45	40	20
	MCM6168P45	45	20
	MCM6168P55	55	20
	MCM6168P70	70	20
	MCM6268P25	25	20
	MCM6268P35	35	20
	MCM6269P25* (2)	25	20
	MCM6269P35 (2)	35	20
8K × 8	MCM6164C45	45	28
	MCM6164C55	55	28
	MCM61L64C45	45	28
	MCM61L64C55	55	28
	MCM6164P45*	45	28
	MCM6164P55*	55	28
	MCM61L64P45*	45	28
	MCM61L64P55*	55	28
	MCM6164J45*	45	28
	MCM6164J55*	55	28
	MCM61L64J45*	45	28
	MCM61L64J55*	55	28
	MCM6164CC55 (3)	55	28
	MCM6164CC70 (3)	70	28
	MCM6264P35*	35	28
	MCM6264P45*	45	28
	MCM6264J35*	35	28
	MCM6264J45*	45	28

*To be introduced
(2) Chip select version
(3) Industrial temperature range, −40 to 85°C
(4) Output enable version

Organization	Part Number	Access Time (ns max)	Pins
16K × 4	MCM6288P25	25	22
	MCM6288P30	30	22
	MCM6288P35	35	22
	MCM6290P25* (4)	25	24
	MCM6290P30* (4)	30	24
	MCM6290P35* (4)	35	24
	MCM6290J25* (4)	25	24
	MCM6290J30* (4)	30	24
	MCM6290J35* (4)	35	24
64K × 1	MCM6287P25	25	22
	MCM6287P35	35	22
	MCM6287J25	25	24
	MCM6287J35	35	24
32K × 8	MCM6206P45*	45	28
	MCM6206P55*	55	28
	MCM6206P70*	70	28
	MCM6206J45*	45	28
	MCM6206J55*	55	28
	MCM6206J70*	70	28
64K × 4	MCM6208P25*	25	24
	MCM6208P35*	35	24
	MCM6208L25*	25	24
	MCM6208L35*	35	24
	MCM6208J25*	25	24
	MCM6208J35*	35	24
256K × 1	MCM6207P25*	25	24
	MCM6207P35*	35	24
	MCM6207L25*	25	24
	MCM6207L35*	35	24
	MCM6207J25*	25	24
	MCM6207J35*	35	24

MCM1423*

4K x 4 Bit Static Random Access Memory



P PACKAGE
PLASTIC
CASE 738

4

The MCM1423 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption, provides greater reliability, and provides protection against soft errors caused by alpha particles. Fast access time makes this device suitable for cache and other sub-50 ns applications, especially those requiring just a little faster address access time (40 ns).

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature reduces system power requirements without degrading access performance.

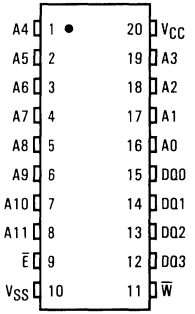
The MCM1423 is available in a 300 mil, 20 pin plastic dual in-line package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 4K x 4 Bit Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Protects Against Soft Errors Caused by Alpha Particles
- Fast Access Time (Maximum):

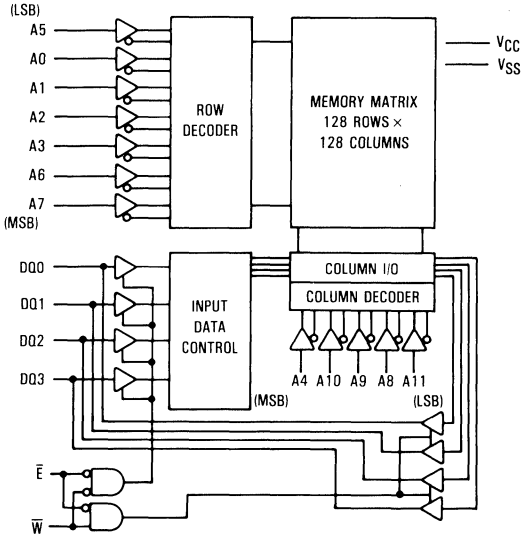
Address	Chip Enable
40 ns	45 ns

- Low Power Operation: 80 mA Max (Active)
  20 mA Max (Standby—TTL Levels)
  2 mA Max (Standby—Full Rail)

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

*This device may also be ordered as IMS1423P-45.

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	Not Selected	I_{SB}	High-Z
L	H	Read	I_{CC}	D_{out}
L	L	Write	I_{CC}	D_{in}

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Value	Unit
Power Supply Voltage (V_{CC})	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	±20	mA
Power Dissipation	1.0	W
Operating Temperature	0 to +70	°C
Storage Temperature	−55 to +125	°C
Temperature Under Bias	−10 to +85	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage (See note below)	V_{IH}	2.0	—	V_{CC} + 0.3 V	V
Input Low Voltage (See note below)	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

NOTE: Address rise and fall times while the chip is selected are 50 ns maximum.

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to 5.5 V)	I_{IL}	—	—	1.0	μA
Output Leakage Current ($\overline{E} = V_{IH}$ or $\overline{W} = V_{IL}$; V_{out} = 0 to V_{CC})**	I_{OL}	—	—	2.0	μA
Power Supply Current ($\overline{E} = V_{IL}$; $V_{in} = V_{IL}$ or V_{IH}, I_{out} = 0 mA)**	I_{CC}	—	—	80	mA
Standby Current ($\overline{E} = V_{IH}$)	I_{SB1}	—	—	20	mA
Standby Current ($\overline{E} \geq V_{CC}$ − 0.2 V) (0.2 V ≥ $V_{in} \geq V_{CC}$ − 0.2 V)	I_{SB2}	—	—	2	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	—	V

**Input levels less than −0.3 V or greater than V_{CC} + 0.3 V will cause I/O and power supply currents to exceed maximum rating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	—	3	5	pF
	$\overline{E}$		—	5	7	
I/O Capacitance		$C_{I/O}$	—	5	7	pF

AC TEST LOADS

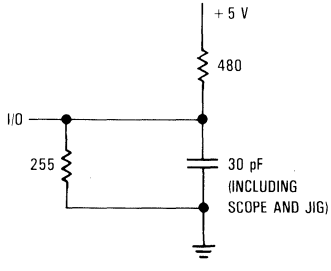


Figure 1A

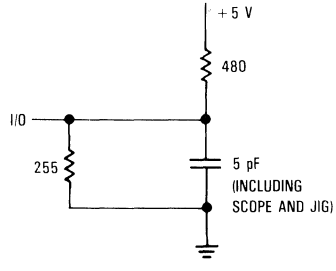


Figure 1B

AC OPERATING CONDITIONS AND CHARACTERISTICS

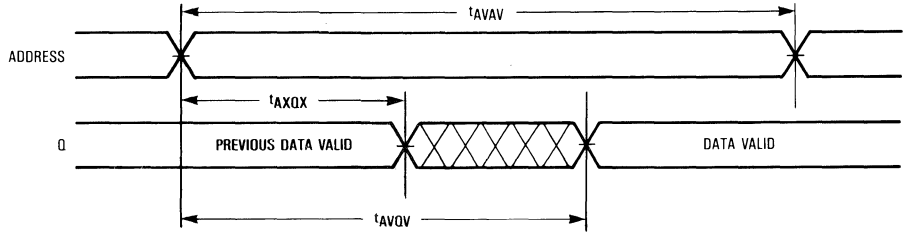
(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Mesurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A

READ CYCLE 1 ($\overline{E}$ = V_{IL})

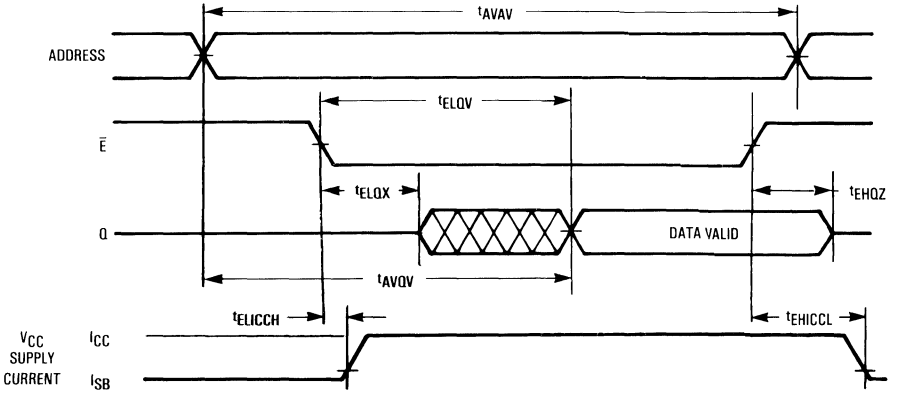
Parameter	Symbol		MCM1423P45		Unit
	Standard	Alternate	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	40	—	ns
Address Access Time	t_{AVQV}	t_{AA}	—	40	ns
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	ns



READ CYCLE 2 ($\overline{E}$ is Clocked)

Parameter	Symbol		MCM1423P45		Unit	Notes
	Standard	Alternate	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	40	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	40	ns	
$\overline{E}$ Access Time	t_{ELQV}	t_{ACS}	—	45	ns	
$\overline{E}$ Low to Output Active	t_{ELQX}	t_{LZ}	5	—	ns	1
$\overline{E}$ High to Output High-Z	t_{EHQZ}	t_{HZ}	0	20	ns	1
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	ns	
Power Up Time	t_{ELICCH}	t_{PU}	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	45	ns	

NOTE:
1. Measured with ac load of Figure 1B. Parameter is sampled and not 100% tested. Transition measured ±500 mV from steady-state voltage.

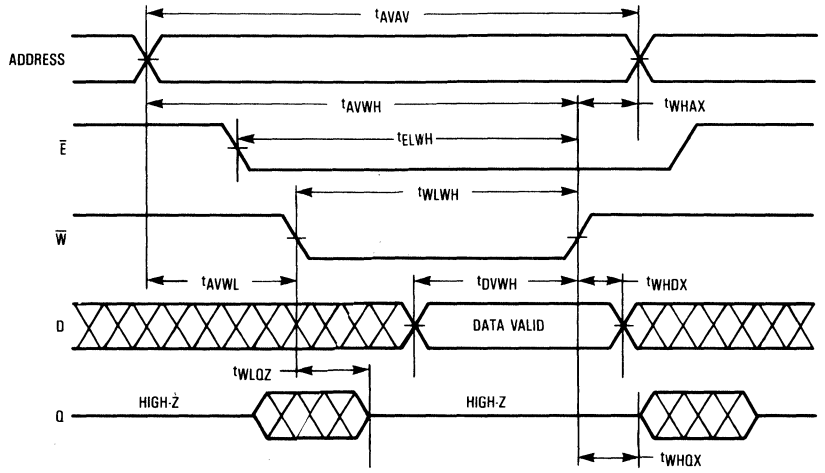


WRITE CYCLE 1 ($\overline{W}$ Controlled) (See Note 1)

Parameter	Symbol		MCM1423P45		Unit	Notes
	Standard	Alternate	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	40	–	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	35	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	35	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	5	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	20	ns	2, 3
Write High to Output Active	t_{WHQX}	t_{OW}	6	–	ns	2, 3
Write Recovery Time	t_{WHAX}	t_{WR}	5	–	ns	
$\overline{E}$ Low to End of Write	t_{ELWH}	t_{CW}	35	–	ns	

4

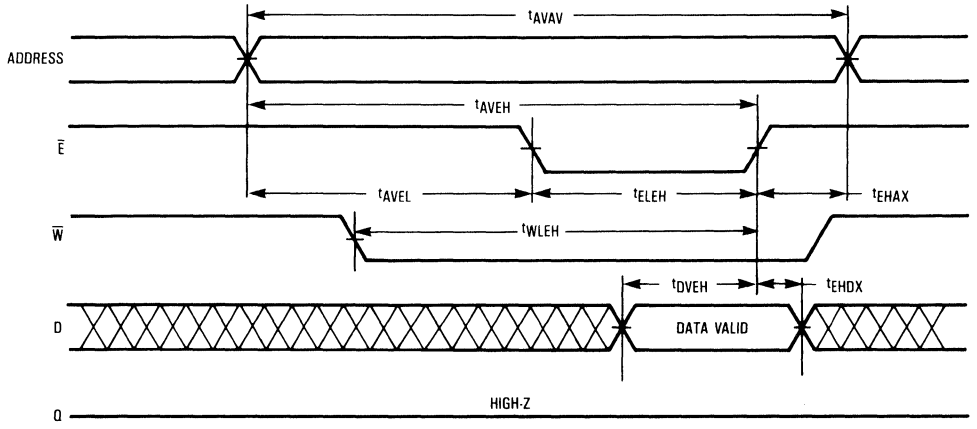
NOTES:
1. A Write occurs during the overlap of a low $\overline{W}$ and a low $\overline{E}$.
2. Measured with the ac load of Figure 1B. Parameter is sampled and not 100% tested. Transition measured ±500 mV from steady-state voltage.
3. When the outputs are active, data of opposite logic level to an output must not be applied.



WRITE CYCLE 2 ($\overline{E}$ Controlled) (See Note 1)

Parameter	Symbol		MCM1423P45		Unit
	Standard	Alternate	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	40	—	ns
Address Setup Time	t_{AVEL}	t_{AS}	0	—	ns
Address Valid to End of Write	t_{AVEH}	t_{AW}	35	—	ns
Write Pulse Width	t_{ELEH}	t_{EW}	35	—	ns
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	—	ns
Data Hold Time	t_{EHDX}	t_{DH}	5	—	ns
Write Recovery Time	t_{EHAX}	t_{WR}	5	—	ns
Write Low to End of Write	t_{WLEH}	t_{WP}	35	—	ns

NOTE:
1. If $\overline{E}$ goes low coincident with or after $\overline{W}$ low, and $\overline{E}$ goes high before or coincident with $\overline{W}$ high, the I/O will remain in a high impedance condition.



TIMING PARAMETER ABBREVIATIONS

t X X X X

signal name from which interval is defined
transition direction for first signal
signal name to which interval is defined
transition direction for second signal

The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

ORDERING INFORMATION
(Order by Full Part Number)

MCM 1423 X XX

- MCM — Motorola Memory Prefix
- 1423 — Part Number
- X — Package (P = Plastic DIP)
- XX — Speed (45 = 45 ns)

Full Part Number — MCM1423P45

NOTE: This device may also be ordered as IMS1423P-45.

MCM6164
MCM61L64

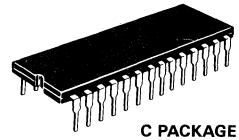
8K x 8 Bit Fast Static Random Access Memory

The MCM6164/MCM61L64 is a 65,536 bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

The MCM6164/MCM61L64 is available in a 600 mil, 28 pin ceramic dual-in-line package, with JEDEC standard pinout.

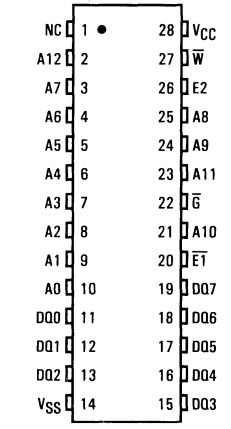
- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time — 45, 55 ns (Maximum)
- Low Power Dissipation — 495, 440 mW (Maximum, Active)
- Low Power/Data Retention Version (MCM61L64)
- Fully TTL Compatible
- Three State Data Outputs
- Also Available in Industrial Temperature Range (−40 to 85°C) as MCM6164C



C PACKAGE
CERAMIC
CASE 733

For Plastic DIP or SOJ package, consult your Motorola representative.

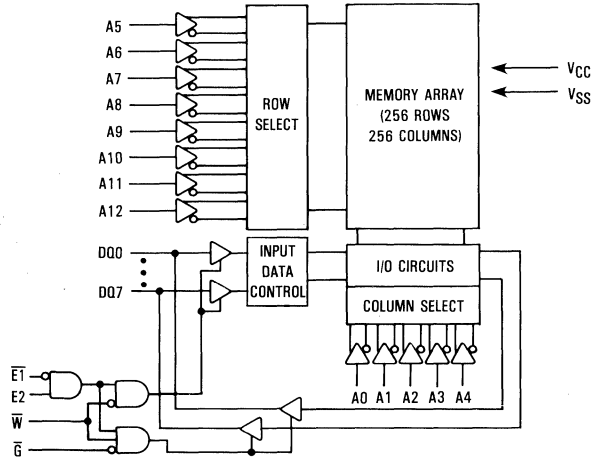
PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc, V_{IL} (min) = −3.0 V (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic		Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	–	<0.01	±1.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	–	<0.01	±1.0	μA
Power Supply Current ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{in} = V_{IH} or V_{IL}, I_{out} = 0)	t_{AVAV} = 45 ns t_{AVAV} = 55 ns	I_{CC}	– –	50 40	90 80	mA
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})		I_{SB1}	–	1.3	3.0	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ 0.2 V)	MCM6164 MCM61L64	I_{SB2}	– –	– 5	1.0 50	mA μA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	–	0.15	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	3.0	–	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	6	pF
Input/Output Capacitance	DQ	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

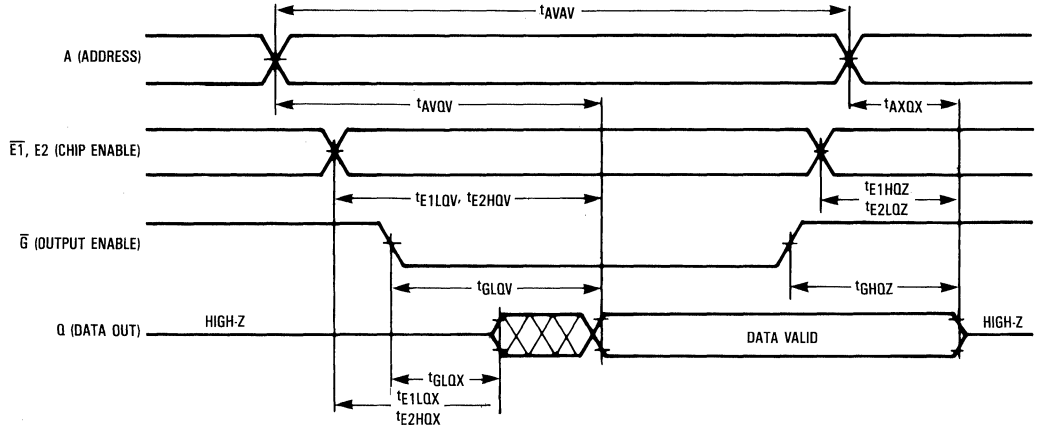
Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . 0.8 V and 2.0 V
Output Load . . . . . Figure 1

READ CYCLE (See Note 1)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	45	–	55	–	ns	–
Address Cycle Time	t_{AVQV}	t_{AA}	–	45	–	55	ns	–
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	–	45	–	55	ns	–
E2 Access Time	t_{E2HQV}	t_{AC2}	–	45	–	55	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	20	–	25	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	ns	–
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5	–	5	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	ns	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	20	0	20	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. Periodically sampled rather than 100% tested.



TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

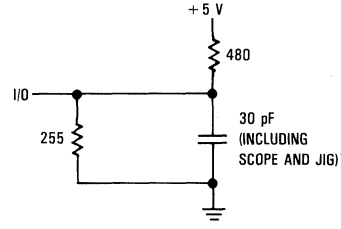
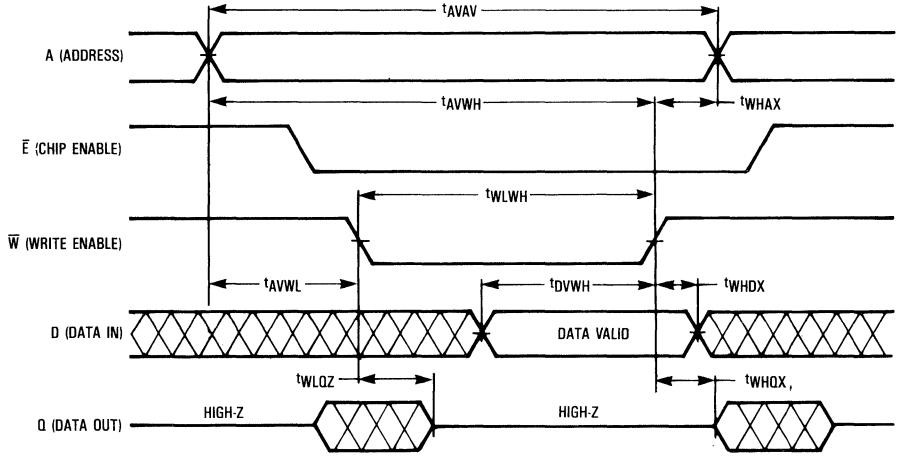


Figure 1. Test Load

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	–	55	–	ns	–
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}	t_{AW}	40	–	50	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	25	–	30	–	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	20	–	25	–	ns	–
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	20	0	20	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	–	5	–	ns	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	–

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. Periodically sampled rather than 100% tested.



TYPICAL CHARACTERISTICS

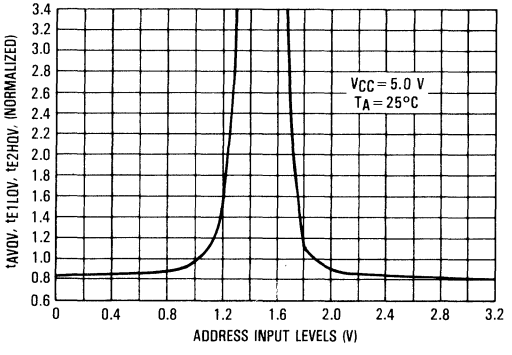
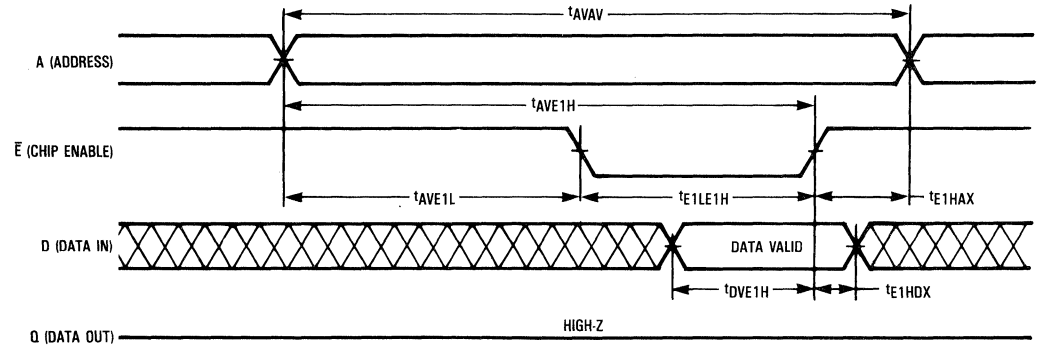


Figure 2. Access Time Versus Address Input Levels

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Notes 1 and 2)

Characteristic	Symbol	Alt Symbol	MCM6164-45 MCM61L64-45		MCM6164-55 MCM61L64-55		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	—	55	—	ns	—
Address Setup Time	t_{AVE1L}	t_{AS}	0	—	0	—	ns	—
Address Valid to End of Write	t_{AVE1H}	t_{AW}	40	—	50	—	ns	—
Chip Enable to End of Write	t_{E1LE1H}	t_{CW}	40	—	50	—	ns	3
Data Valid to End of Write	t_{DVE1H}	t_{DW}	20	—	25	—	ns	—
Data Hold Time	t_{E1HDX}	t_{DH}	0	—	0	—	ns	4
Write Recovery Time	t_{E1HAX}	t_{WR}	0	—	0	—	ns	5

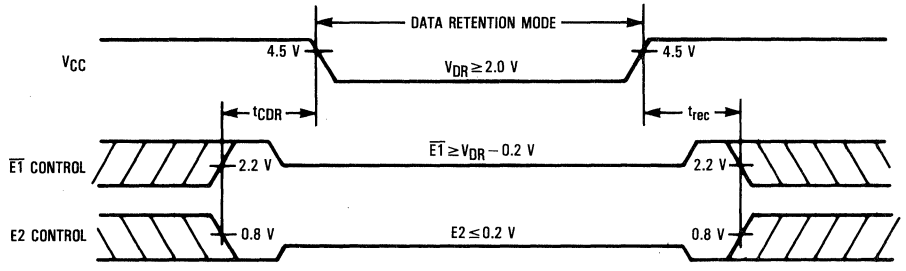
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
5. $\overline{W}$ must be high during all address transitions.



LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C) (MCM61L64 Only)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{CC} for Data Retention ($\overline{E1} \geq V_{CC} - 0.2$ V or E2 ≤ 0.2 V, $V_{in} \geq V_{CC} - 0.2$ V or $V_{in} \leq 0.2$ V)	V_{DR}	2.0	1.0	7.0	V
Data Retention Current (V_{CC} = 3.0 V, $\overline{E1} \geq 2.8$ V or E2 ≤ 0.2 V, $V_{in} \geq 2.8$ V or $V_{in} \leq 0.2$ V)	I_{CCDR}	—	10	30	μA
Chip Disable to Data Retention Time (see waveform below)	t_{CDR}	0	—	—	ns
Operation Recovery Time (see waveform below)	t_{rec}	t_{AVAV}*	—	—	ns

*t_{AVAV} = Read Cycle Time



TYPICAL CHARACTERISTICS
(Continued)

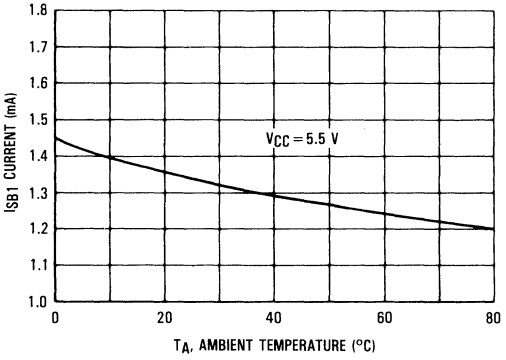


Figure 3. Standby Current Versus Temperature

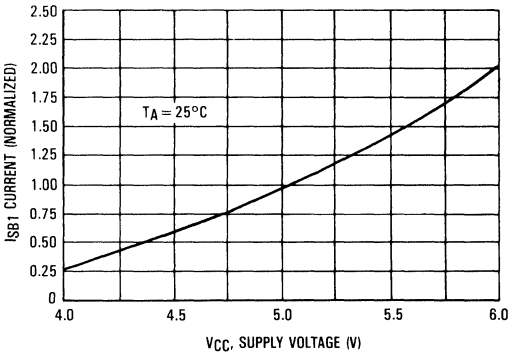


Figure 4. Standby Current Versus Supply Voltage

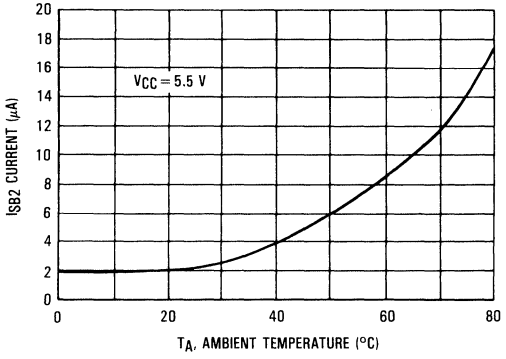


Figure 5. Standby Current Versus Temperature

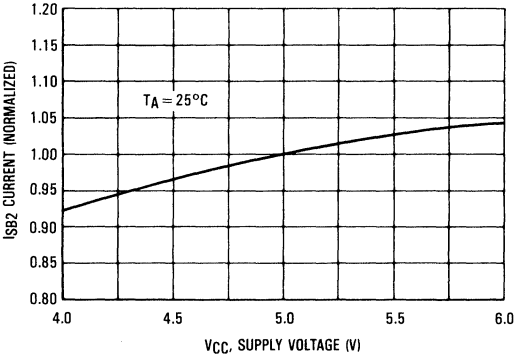


Figure 6. Standby Current Versus Supply Voltage

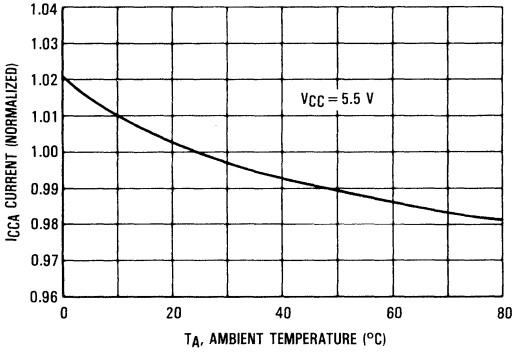


Figure 7. Supply Current Versus Temperature

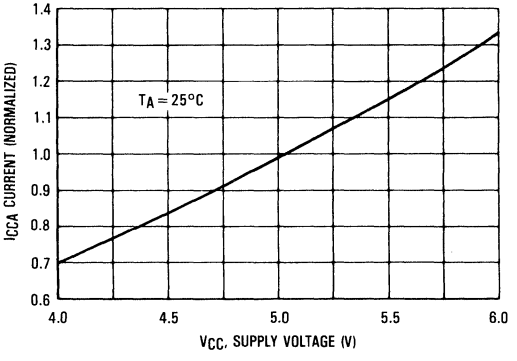


Figure 8. Supply Current Versus Supply Voltage

TYPICAL CHARACTERISTICS
(Continued)

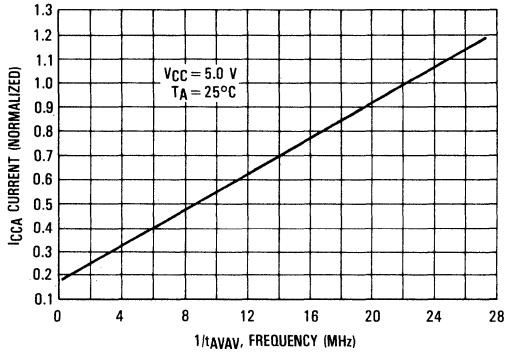


Figure 9. Supply Current Versus Frequency

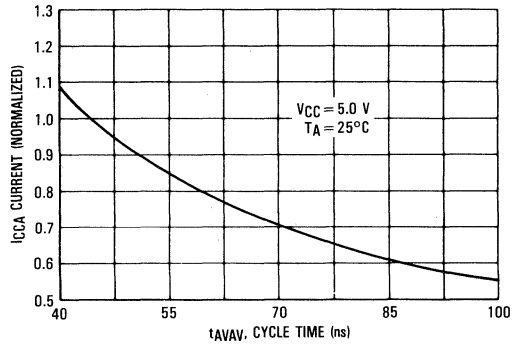


Figure 10. Supply Current Versus Cycle Time

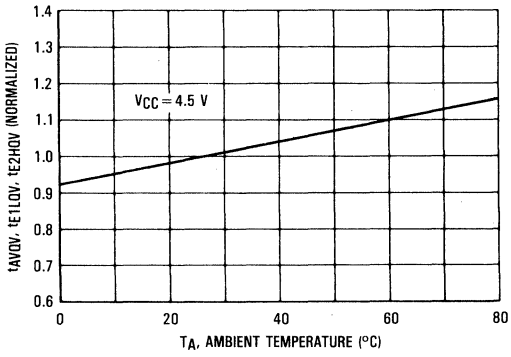


Figure 11. Access Time Versus Temperature

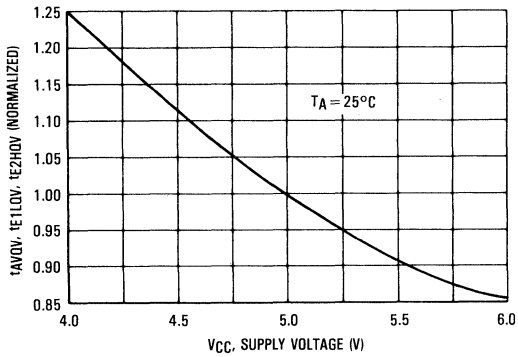


Figure 12. Access Time Versus Supply Voltage

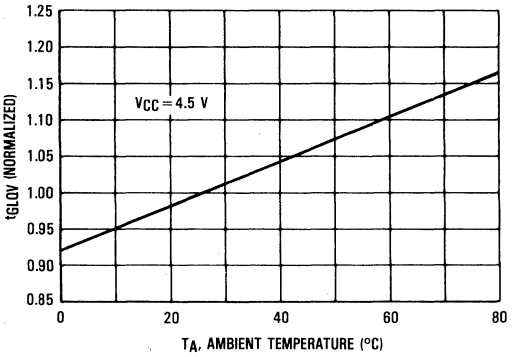


Figure 13. Access Time Versus Temperature

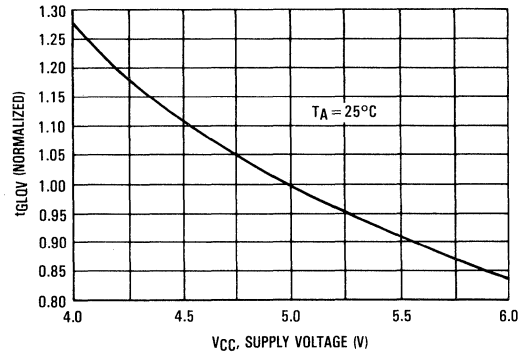
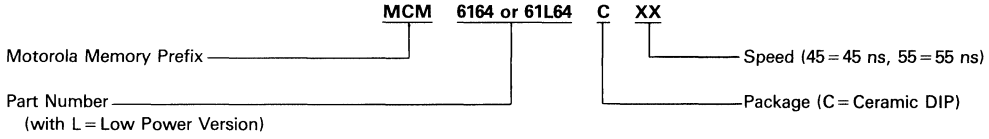


Figure 14. Access Time Versus Supply Voltage

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6164C45 MCM6164C55 MCM61L64C45 MCM61L64C55

For Plastic DIP or SOJ package, consult your Motorola representative.

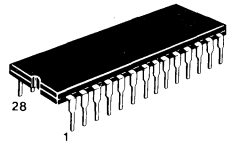
4

MCM6164C

Advance Information

8K x 8 Bit Fast Static Random Access Memory

Industrial Temperature Range: −40 to 85°C



C PACKAGE
CERAMIC
CASE 733

4

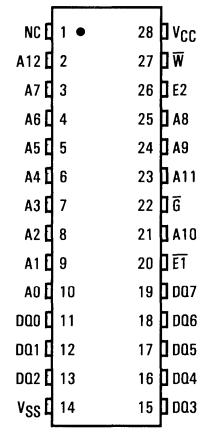
The MCM6164C is a 65,536 bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. With its operating temperature range of −40°C to +85°C and hermetic package, the MCM6164C is ideally suited for harsh industrial type environments.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

The MCM6164C is available in a 600 mil, 28 pin ceramic dual-in-line package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—55 or 70 ns (Maximum)
- Low Power Dissipation—440 or 385 mW (Maximum, Active)
- Fully TTL Compatible
- Three State Data Outputs
- Also Available in Commercial Temperature Range (0 to 70°C) as MCM6164/MCM61L64

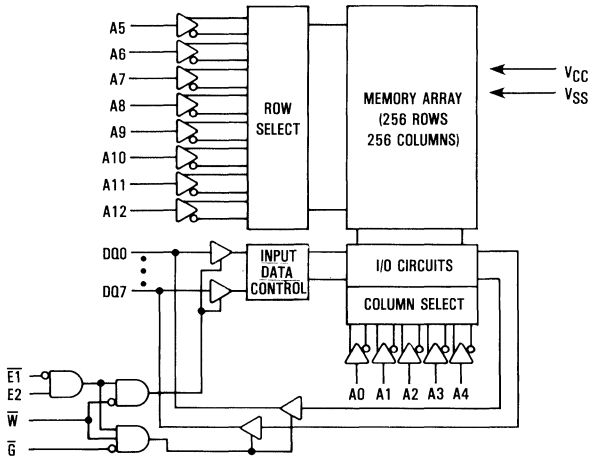
PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	−40 to +85	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = −40 to 85°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc, V_{IL} (min) = −3.0 V (pulse width ≤20 ns)

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	<0.01	±2.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	<0.01	±2.0	μA
Power Supply Current t_{AVAV} = 55 ns	I_{CC}	—	40	80	mA
($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{in} = V_{IH} or V_{IL}, I_{out} = 0) t_{AVAV} = 70 ns		—	35	70	
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})	I_{SB1}	—	1.3	3.0	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ 0.2 V)	I_{SB2}	—	0.005	1.0	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.15	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	3.0	—	V

Typical values are referenced to T_A = 25°C and V_{CC} = 5.0 V

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	6	pF
Input/Output Capacitance	DQ	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −40 to +85°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Output Timing Measurement Reference Level . . . 0.8 V and 2.0 V
Output Load . . . . . Figure 1

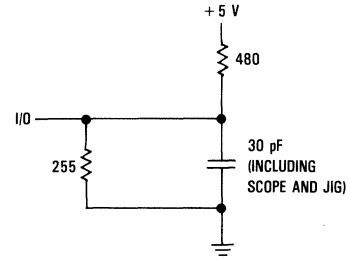


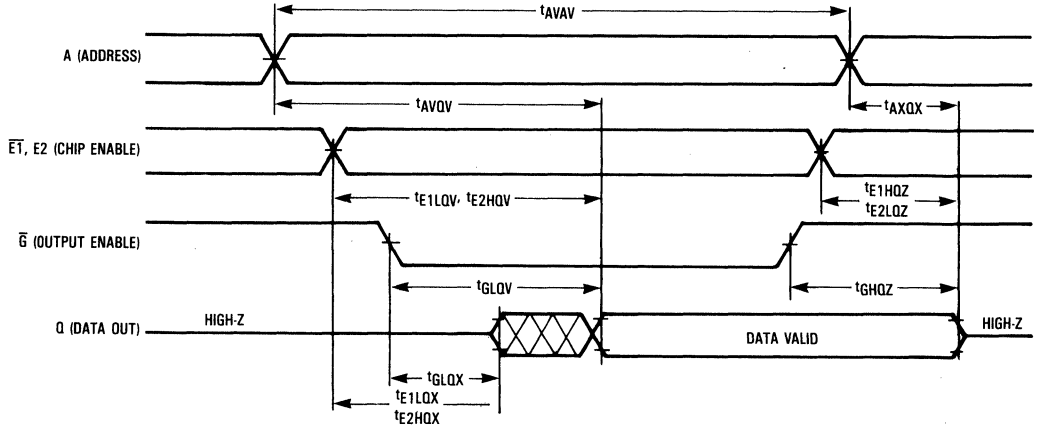
Figure 1. Test Load

4

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6164CC55		MCM6164CC70		Notes
			Min	Max	Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	55	–	70	–	–
Address Cycle Time	t_{AVQV}	t_{AA}	–	55	–	70	–
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	–	55	–	70	–
E2 Access Time	t_{E2HQV}	t_{AC2}	–	55	–	70	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	25	–	30	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	–
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5	–	5	–	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	20	0	20	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	2, 3

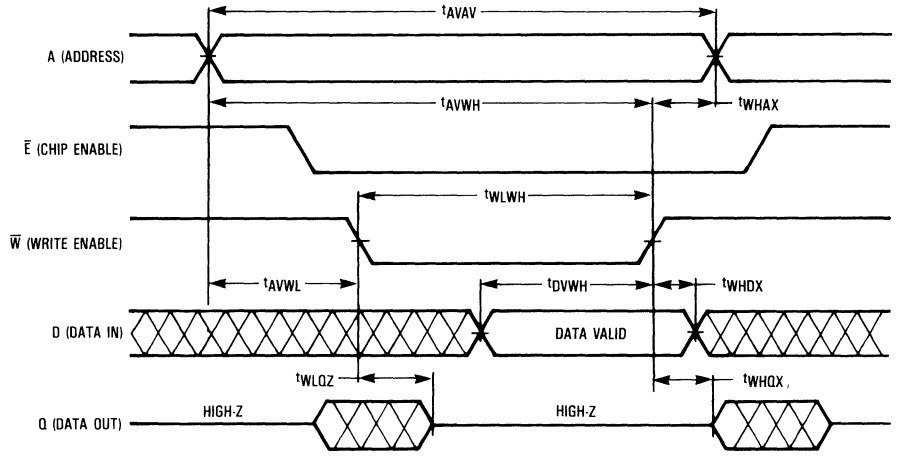
NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. Periodically sampled rather than 100% tested.



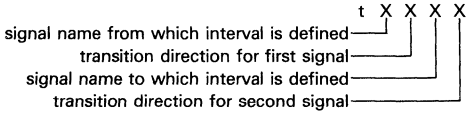
WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6164CC55		MCM6164CC70		Notes
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	55	–	70	–	–
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	–
Address Valid to End of Write	t_{AVWH}	t_{AW}	50	–	60	–	–
Write Pulse Width	t_{WLWH}	t_{WP}	30	–	40	–	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	25	–	30	–	–
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	20	0	20	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	–	5	–	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	–

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. Periodically sampled rather than 100% tested.



TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

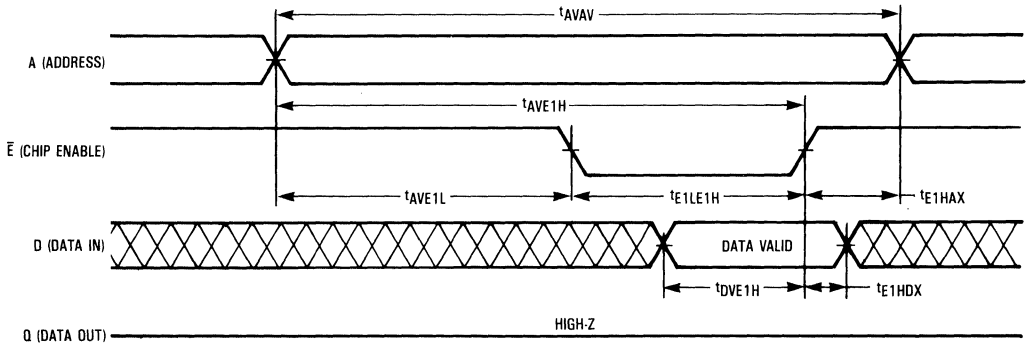
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Notes 1 and 2)

Parameter	Symbol	Alt Symbol	MCM6164CC55		MCM6164CC70		Notes
			Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	55	–	70	–	–
Address Setup Time	t_{AVE1L}	t_{AS}	0	–	0	–	–
Address Valid to End of Write	t_{AVE1H}	t_{AW}	50	–	60	–	–
Chip Enable to End of Write	t_{E1LE1H}	t_{CW}	50	–	60	–	3
Data Valid to End of Write	t_{DVE1H}	t_{DW}	25	–	30	–	–
Data Hold Time	t_{E1HDX}	t_{DH}	0	–	0	–	4
Write Recovery Time	t_{E1HAX}	t_{WR}	0	–	0	–	5

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.
3. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
4. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
5. $\overline{W}$ must be high during all address transitions.



TYPICAL CHARACTERISTICS

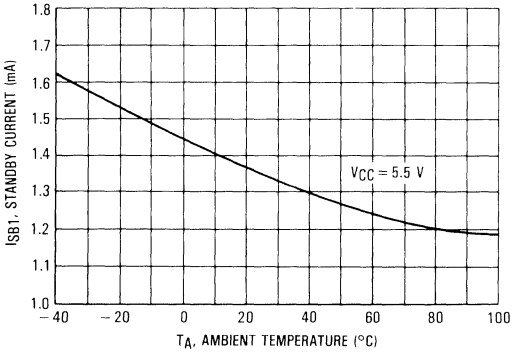


Figure 2. Standby Current Versus Temperature

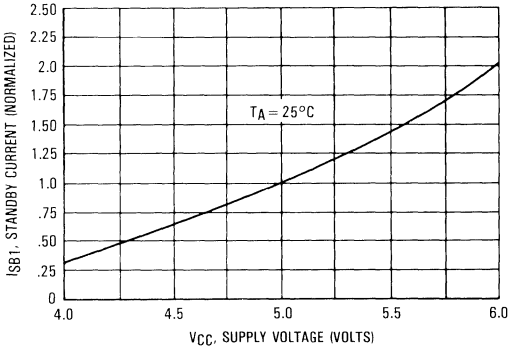


Figure 3. Standby Current Versus Supply Voltage

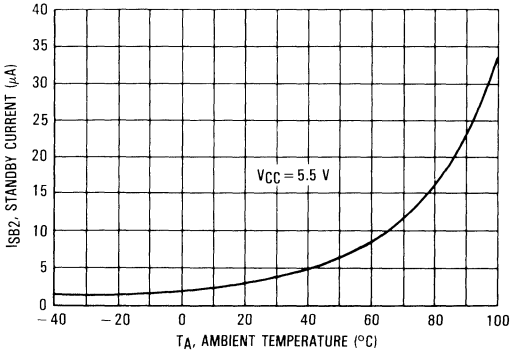


Figure 4. Standby Current Versus Temperature

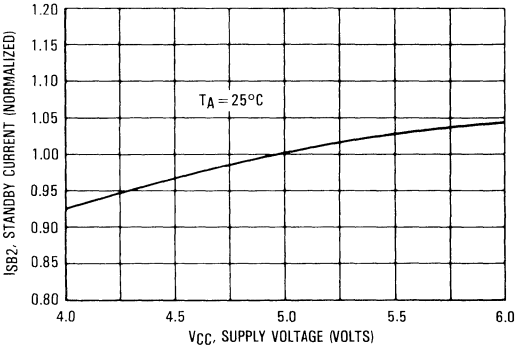


Figure 5. Standby Current Versus Supply Voltage

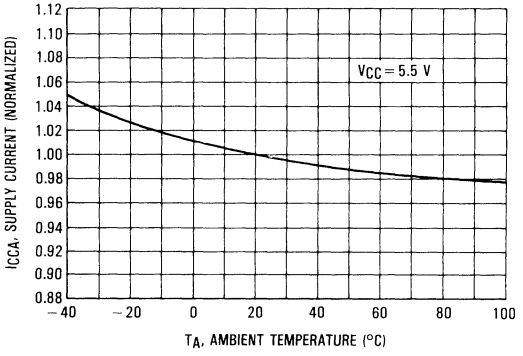


Figure 6. Supply Current Versus Temperature

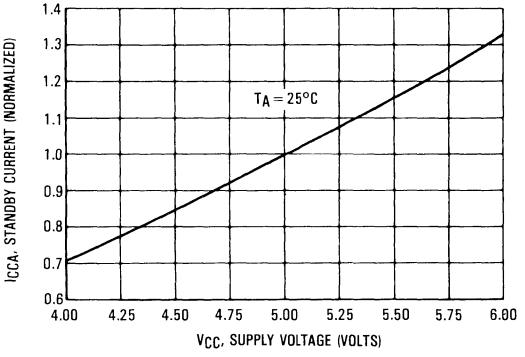


Figure 7. Supply Current Versus Supply Voltage

TYPICAL CHARACTERISTICS
(Continued)

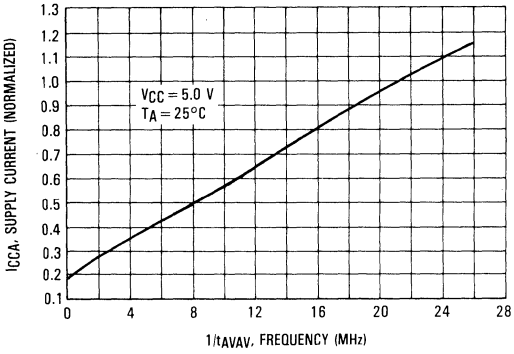


Figure 8. Supply Current Versus Frequency

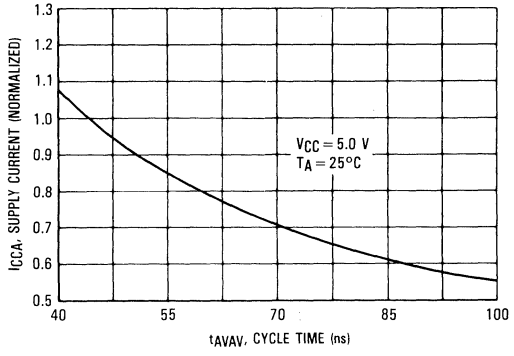


Figure 9. Supply Current Versus Cycle Time

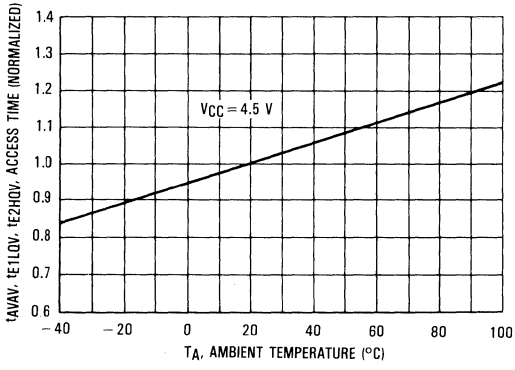


Figure 10. Access Time Versus Temperature

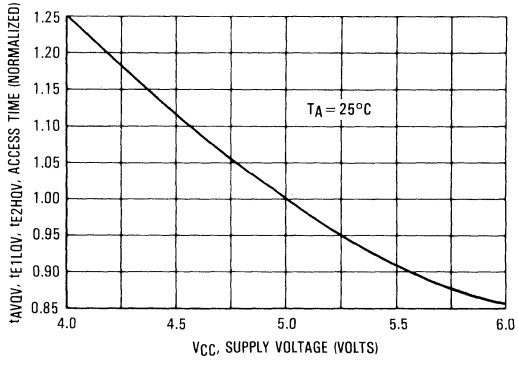


Figure 11. Access Time Versus Supply Voltage

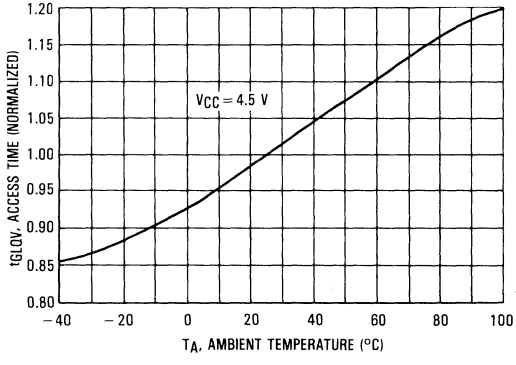


Figure 12. Access Time Versus Temperature

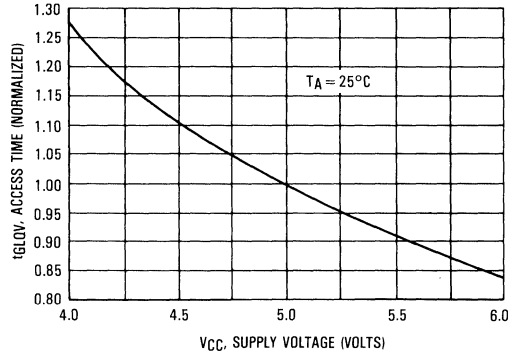


Figure 13. Access Time Versus Supply Voltage

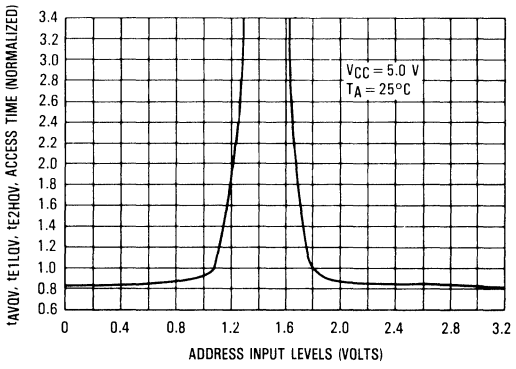
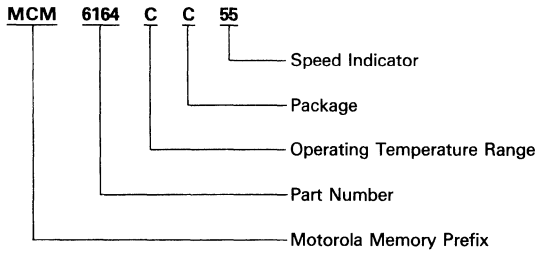


Figure 14. Access Time Versus Address Input Levels

4

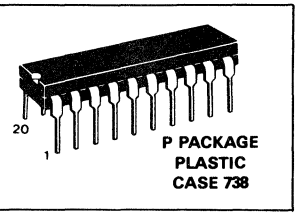
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Number—MCM6164CC55 or MCM6164CC70

MCM6168

4K x 4 Bit Static Random Access Memory



P PACKAGE
PLASTIC
CASE 738

The MCM6168 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other high speed applications.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature provides reduced system power requirements without degrading access time performance.

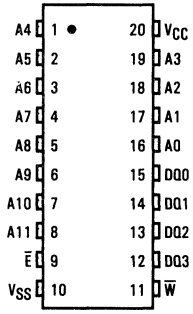
The MCM6168 is available in a 300 mil, 20 lead plastic dual-in-line package with the standard JEDEC pinout.

- Single 5 V Supply, ±10%
- 4K x 4 Bit Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Three State Output
- Fast Access Time (Maximum):

	Address	Chip Enable
MCM6168-45	45 ns	45 ns
MCM6168-55	50 ns	55 ns
MCM6168-70	60 ns	70 ns

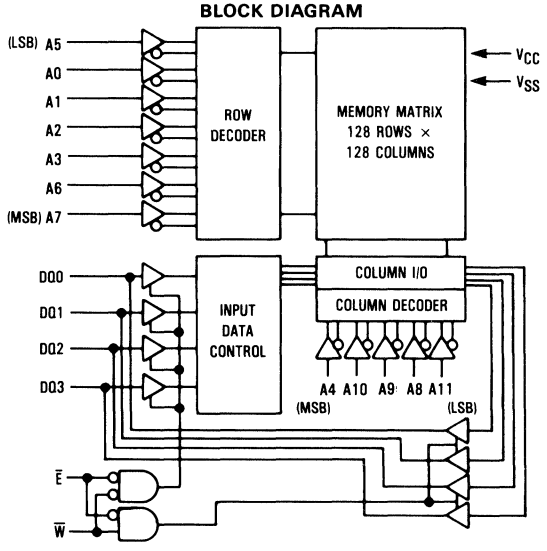
- Low Power Operation: 80 mA Max (Active)
  20 mA Max (Standby—TTL Levels)
  2 mA Max (Standby—CMOS Levels)
- Fully TTL Compatible

PIN ASSIGNMENT



PIN NAMES	
A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin
H	X	Not Selected	ISB1, ISB2	High-Z
L	H	Read	I_{CC}	D_{out}
L	L	Write	I_{CC}	D_{in}

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V	1
Input Low Voltage	V_{IL}	−0.3	—	0.8	V	1, 2

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA	
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±2.0	μA	3
Power Supply Current ($\overline{E}$ = V_{IL}, V_{in} = V_{IL} or V_{IH}, I_{out} = 0 mA)	I_{CC}	—	80	mA	3
TTL Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	—	20	mA	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ 0.2 V or ≥ V_{CC} − 0.2 V)	I_{SB2}	—	2	mA	
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V	

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	3	5	pF
	$\overline{E}$		5	7	
I/O Capacitance		$C_{I/O}$	5	7	pF

NOTES:
1. Address rise and fall times while the chip is selected are 50 ns maximum.
2. V_{IL}(min) = −0.3 V dc; V_{IL}(min) = −3.0 V ac (pulse width ≤ 20 ns).
3. Input levels less than −0.3 V or greater than V_{CC} + 0.3 V will cause I/O and power supply currents to exceed maximum rating.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

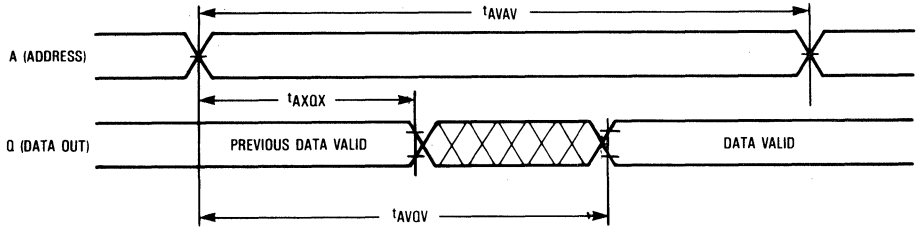
Output Timing Measurement Reference Level . . . . .0.8 and 2.0 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

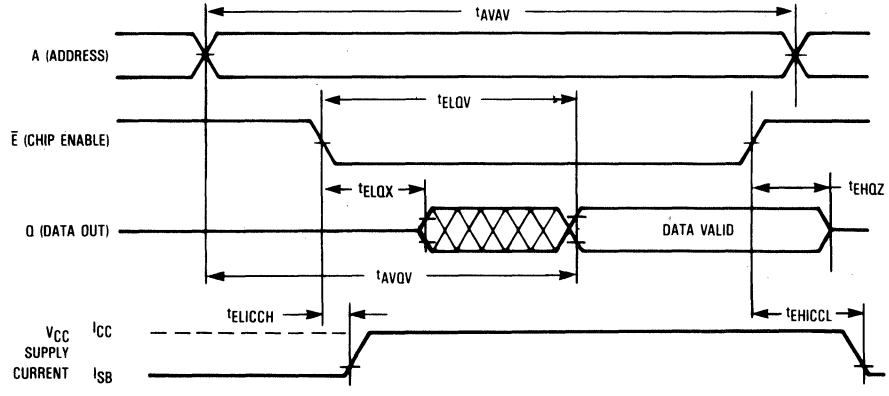
Parameter	Symbol		MCM6168-45		MCM6168-55		MCM6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	45	–	55	–	70	–	ns	
Address Access Time	t_{AVQV}	t_{AA}	–	45	–	50	–	60	ns	
$\overline{E}$ Access Time	t_{ELQV}	t_{ACS}	–	45	–	55	–	70	ns	
$\overline{E}$ Low to Output Active	t_{ELQX}	t_{LZ}	10	–	10	–	10	–	ns	2, 3
$\overline{E}$ High to Output High-Z	t_{EHQZ}	t_{HZ}	0	15	0	20	0	25	ns	2, 3
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns	
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	45	–	55	–	70	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
3. This parameter is sampled and not 100% tested.
4. Device is continuously selected ($\overline{E} = V_{IL}$).
5. Addresses valid prior to or coincident with $\overline{E}$ going low.

READ CYCLE 1 (See Note 4 Above)



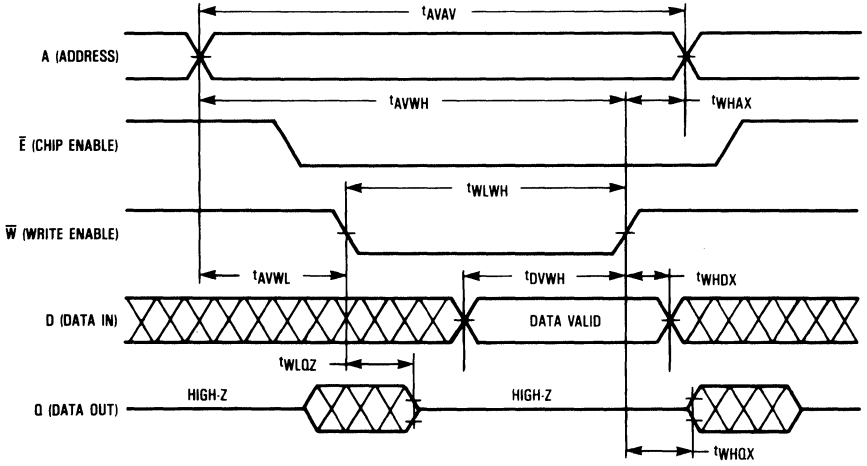
READ CYCLE 2 (See Note 5 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled; See Note 1)

Parameter	Symbol		MCM6168-45		MCM6168-55		MCM6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	40	–	50	–	60	–	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	35	–	45	–	55	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	35	–	45	–	55	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	–	20	–	25	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	3	–	3	–	3	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	–	20	–	25	–	30	ns	2, 3
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	5	–	ns	2, 3
Write Recovery Time	t_{WHAX}	t_{WR}	5	–	5	–	5	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
3. Parameter is sampled and not 100% tested.



AC TEST LOADS

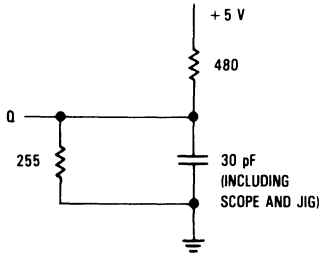


Figure 1A

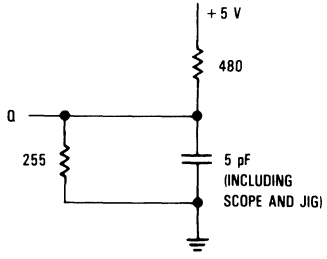


Figure 1B

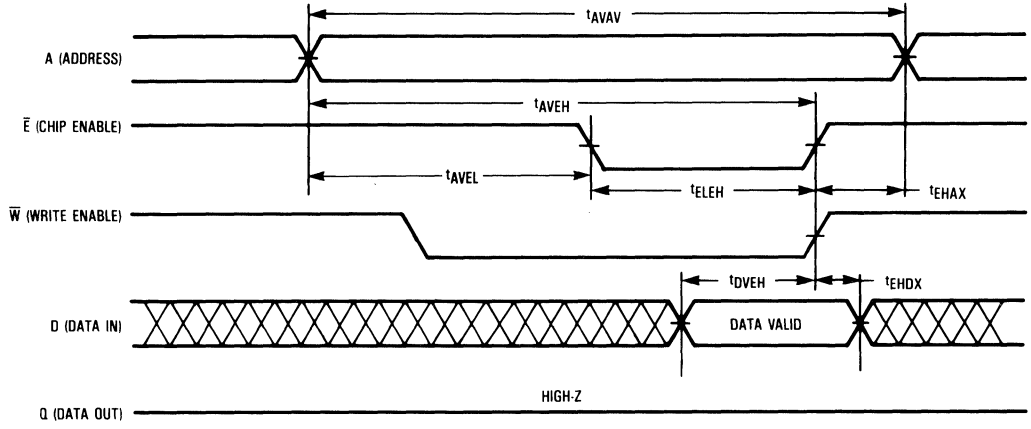
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

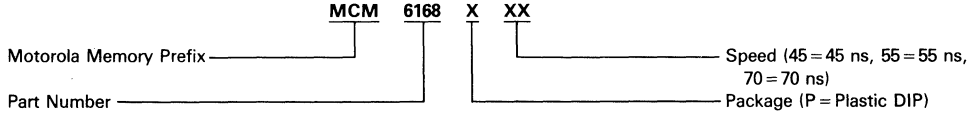
WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		MCM6168-45		MCM6168-55		MCM6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	40	–	50	–	60	–	ns	
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	35	–	45	–	55	–	ns	
Write Pulse Width	t_{ELEH}	t_{CW}	35	–	45	–	55	–	ns	2, 3
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	–	20	–	25	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	3	–	3	–	3	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	5	–	5	–	5	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
3. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

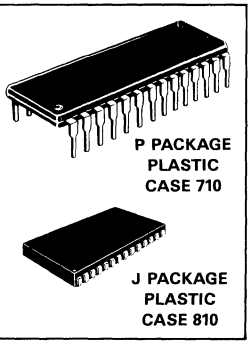


Full Part Numbers – MCM6168P45
MCM6168P55
MCM6168P70

MCM6206

Product Preview

32K x 8 Bit Fast Static Random Access Memory



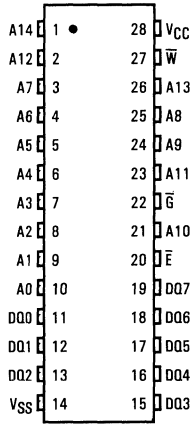
The MCM6206 is a 262,144 bit static random access memory organized as 32,768 words of 8 bits, fabricated using Motorola's third-generation high-performance silicon-gate CMOS (HCMOS IV) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

Chip enable ($\overline{E}$) controls the power-down feature. It is not a clock but rather a chip control that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature provides significant system-level power savings. Another control feature, output enable ($\overline{G}$) allows access to the memory contents as fast as 20 ns (MCM6206-45).

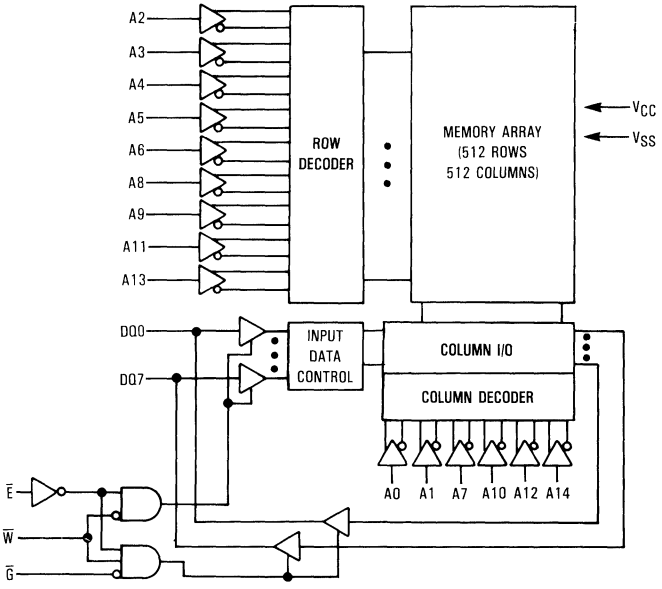
The MCM6206 is packaged in a 600 mil, 28 pin plastic dual-in-line package or a 28 lead 400 mil plastic SOJ package with the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—45, 55, or 70 ns (Maximum)
- Low Power Dissipation
- Two Chip Controls; $\overline{E}$ for Automatic Power Down
  $\overline{G}$ for Fast Access to Data
- Three State Outputs
- Fully TTL Compatible

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A14	Address
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	Not Selected	I_{SB}	High Z
L	H	H	Output Disabled	I_{CC}	High Z
L	L	H	Read	I_{CC}	D_{out}
L	X	L	Write	I_{CC}	D_{in}

X—Don't Care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	—	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg}(I)$	—	±1.0	μA
Output Leakage Current ($\overline{E}=V_{IH}$, or $\overline{G}=V_{IH}$, V_{out}=0 to 5.5 V)		$I_{lkg}(O)$	—	±1.0	μA
Power Supply Current ($\overline{E}=V_{IL}$, $V_{in}=V_{IH}$ or V_{IL}, I_{out}=0)	(t_{AVAV}=45 ns)	I_{CC}	—	120	mA
	(t_{AVAV}=55 ns)	I_{CC}	—	110	mA
	(t_{AVAV}=70 ns)	I_{CC}	—	100	mA
Standby Current ($\overline{E}=V_{IH}$) (TTL Levels)		I_{SB1}	—	TBD	mA
Standby Current ($\overline{E} \geq V_{CC}-0.2$ V) (CMOS Levels)		I_{SB2}	—	TBD	mA
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, T_A=25°C, periodically sampled and not 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

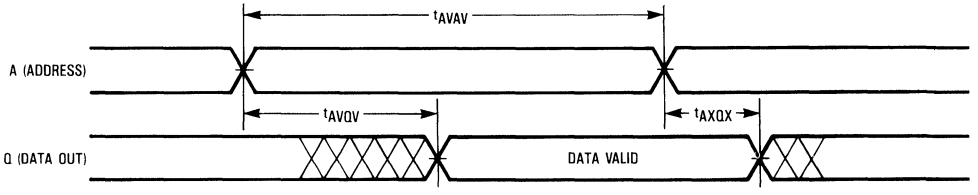
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . . 1.5 V
Output Load . . . . . See Figure 1

READ CYCLE 1 & 2 (See Note 1)

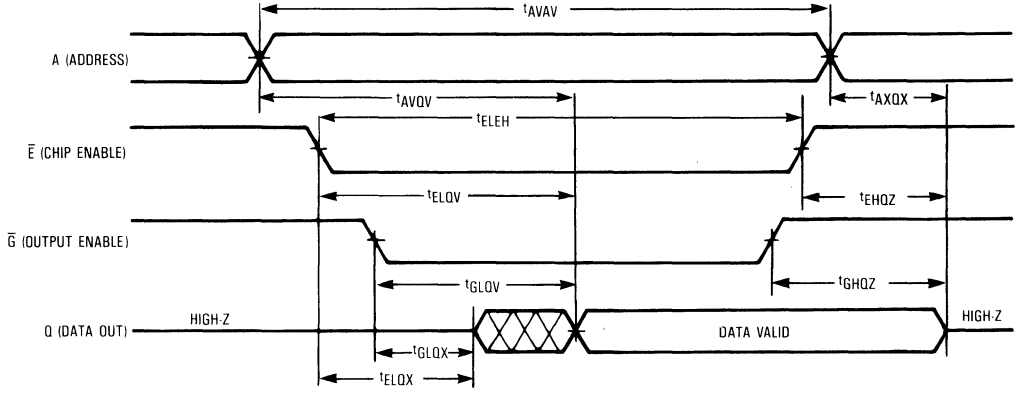
Parameter	Symbol	Alt Symbol	MCM6206-45		MCM6206-55		MCM6206-70		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	45	–	55	–	70	–	ns	–
Address Access Time	t_{AVQV}	t_{AA}	–	45	–	55	–	70	ns	–
$\overline{E}$ Access Time	t_{ELQV}	t_{AC}	–	45	–	55	–	70	ns	–
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	–	20	–	25	–	30	ns	–
Enable Low to Enable High	t_{ELEH}	t_{CW}	45	–	55	–	70	–	ns	–
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns	2
Chip Enable to Output Low-Z	t_{ELQX}	t_{CLZ}	10	–	10	–	10	–	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	–	0	–	0	–	ns	2, 3
Chip Enable to Output High-Z	t_{EHQZ}	t_{CHZ}	0	20	0	20	0	20	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	20	0	20	0	20	ns	2, 3

NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.

READ CYCLE 1 ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL})



READ CYCLE 2



WRITE CYCLE 1 & 2 (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6206-45		MCM6206-55		MCM6206-70		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	45	—	55	—	70	—	ns	—
Address Setup to Write Low Address Setup to Enable Low	t_{AVWL} t_{AVEL}	t_{AS}	0	—	0	—	0	—	ns	2
Address Valid to Write High Address Valid to Enable High	t_{AVWH} t_{AVEH}	t_{AW}	35	—	45	—	55	—	ns	—
Data Valid to Write High Data Valid to Enable High	t_{DVWH} t_{DVEH}	t_{DW}	20	—	25	—	30	—	ns	—
Data Hold From Write High Data Hold From Enable High	t_{WHDX} t_{EHDX}	t_{DH}	0	—	0	—	0	—	ns	3
Write Recovery Time Enable Recovery Time	t_{WHAX} t_{EHAX}	t_{WR}	0	—	0	—	0	—	ns	2
Chip Enable to End of Write Enable Low to Enable High	t_{ELWH} t_{ELEH}	t_{CW}	35	—	45	—	55	—	ns	1
Write Pulse Width	t_{WLWH}	t_{WP}	25	—	30	—	35	—	ns	—
Write Low to Output High-Z	t_{WLQZ}	t_{WHZ}	0	20	0	20	0	20	ns	4
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	—	5	—	5	—	ns	4

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E}$ or low $\overline{W}$. A write cycle ends at the earliest transition of a high $\overline{E}$ or high $\overline{W}$.
2. $\overline{W}$ must be high during all address transitions.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mv transition from the previous steady state voltage.

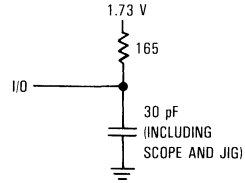
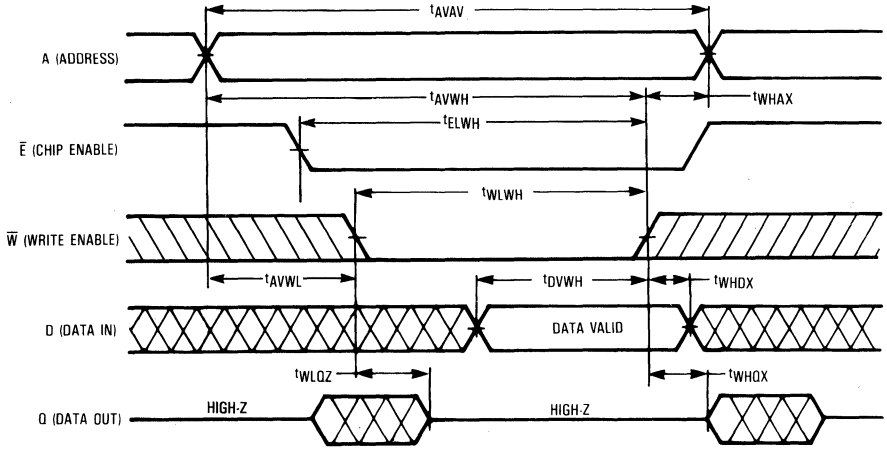
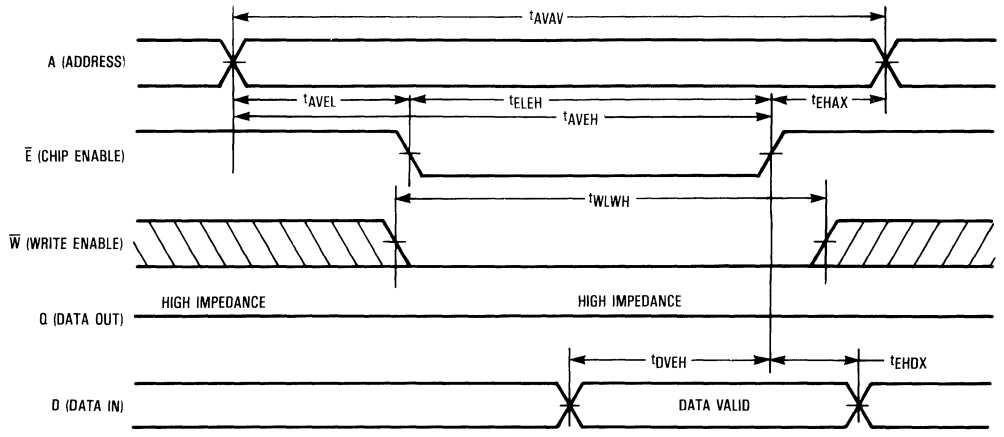


Figure 1. Test Load

WRITE CYCLE 1 ($\overline{W}$ Controlled)



WRITE CYCLE 2 ($\overline{E}$ Controlled)



4

ORDERING INFORMATION
(Order by Full Part Number)

MCM 6206 X XX

Motorola Memory Prefix

Part Number

Speed (45 = 45 ns, 55 = 55 ns, 70 = 70 ns)

Package (P = Plastic DIP, J = Plastic SOJ)

Full Part Numbers — MCM6206P45 MCM6206P55 MCM6206P70
MCM6206J45 MCM6206J55 MCM6206J70

MCM6207

Product Preview

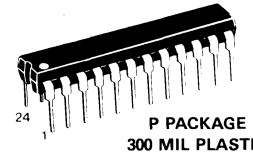
256K x 1 Bit Static Random Access Memory

The MCM6207 is a 262,144 bit static random access memory organized as 262,144 words of 1 bit, fabricated using Motorola's third-generation high-performance silicon-gate CMOS (HCMOS IV) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

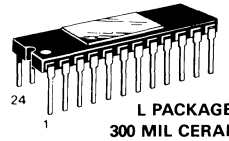
The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

The MCM6207 is available in a 300 mil, 24 lead ceramic sidebraze or plastic DIP, and will also be available in a 300 mil, surface-mount SOJ package.

- Single 5 V ±10% Power Supply
- Fast Access Time: 25/35 ns
- Equal Address and Chip Enable Access Time
- Separate Data Input and Three State Output
- Fully TTL Compatible
- Low Power Operation: 120/110 mA Maximum, Active AC
- High Board Density SOJ Package to be Available



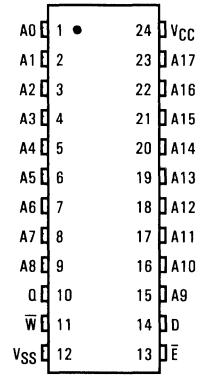
P PACKAGE
300 MIL PLASTIC
CASE 724



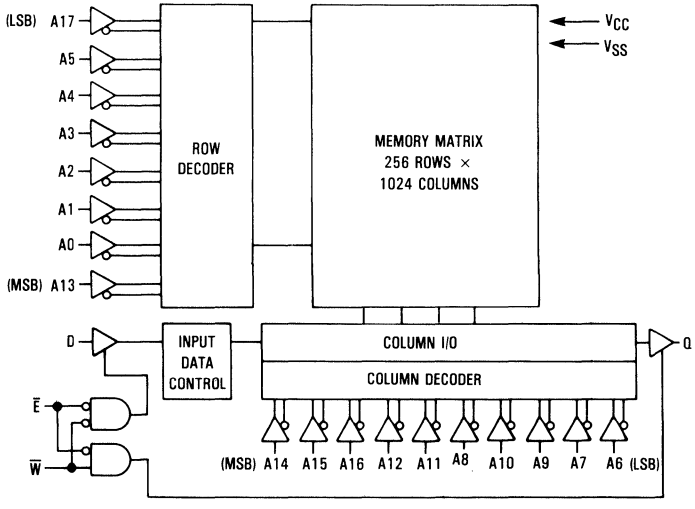
L PACKAGE
300 MIL CERAMIC
CASE 716

WILL BE AVAILABLE IN
24-LEAD, 300-MIL,
SURFACE MOUNT SOJ PACKAGE

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A17	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current	I_{out}	±20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias (T_A = 25°C)	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic Ceramic	T_{stg}	−55 to +125 −65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out} = 0 mA) MCM6207-25: t_{AVAV} = 25 ns	I_{CCA}	—	120	mA
MCM6207-35: t_{AVAV} = 35 ns		—	110	
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	TBD	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	TBD	mA
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance All Inputs Except $\overline{E}$	C_{in}	4	6	pF
$\overline{E}$		5	7	
Output Capacitance	C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

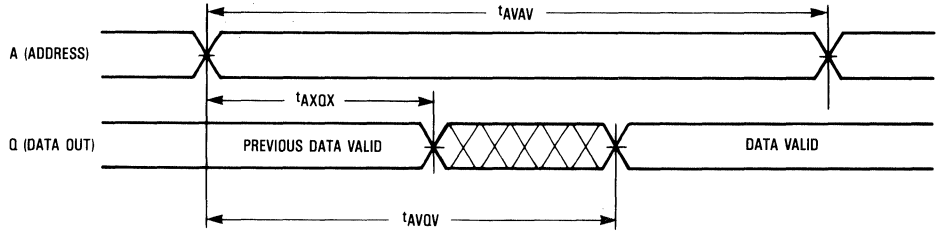
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A

READ CYCLE (See Note 1)

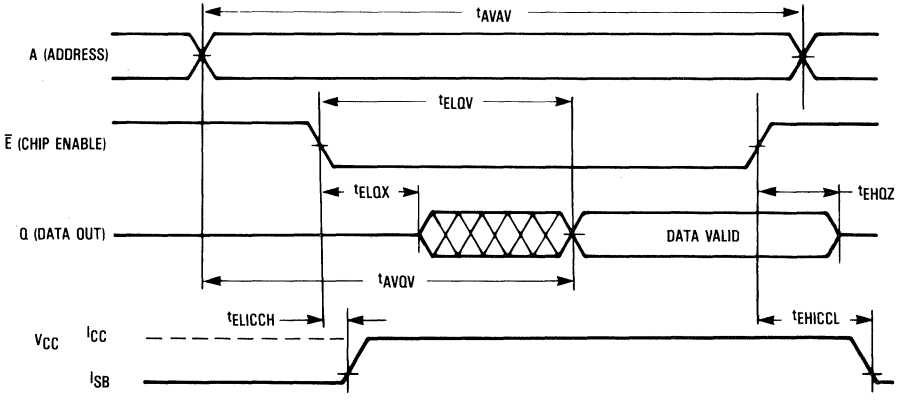
Parameter	Symbol		MCM6207-25		MCM6207-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	–	35	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	25	–	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	–	25	–	35	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	–	5	–	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	15	0	15	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	25	–	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E} = V_{IL}$).

READ CYCLE 1 (See Note 7 Above)



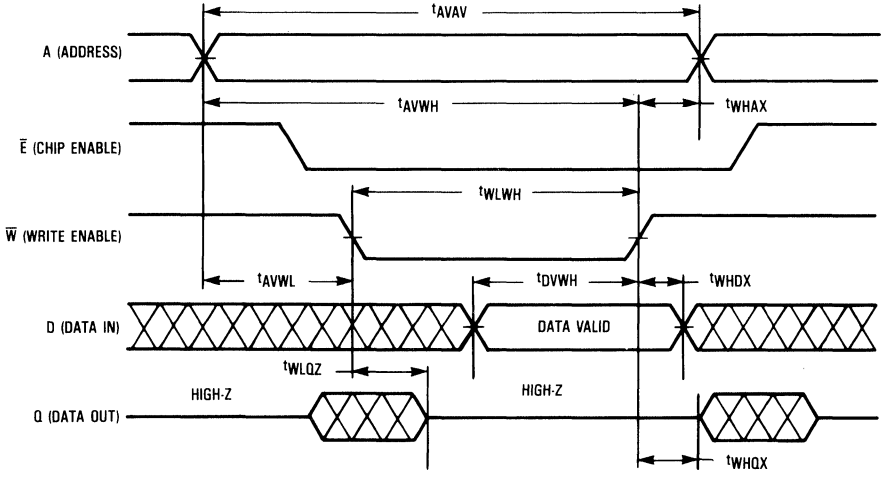
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6207-25		MCM6207-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	35	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	–	25	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	–	20	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	–	15	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	15	0	15	ns	3,4
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	ns	3,4
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.



AC TEST LOADS

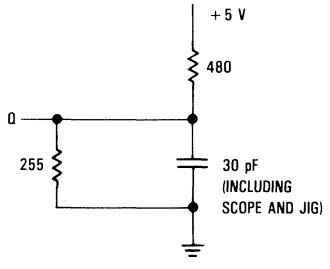


Figure 1A

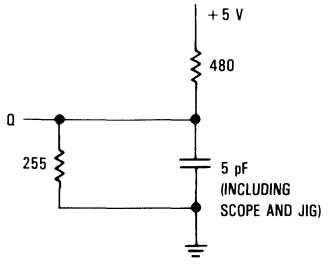


Figure 1B

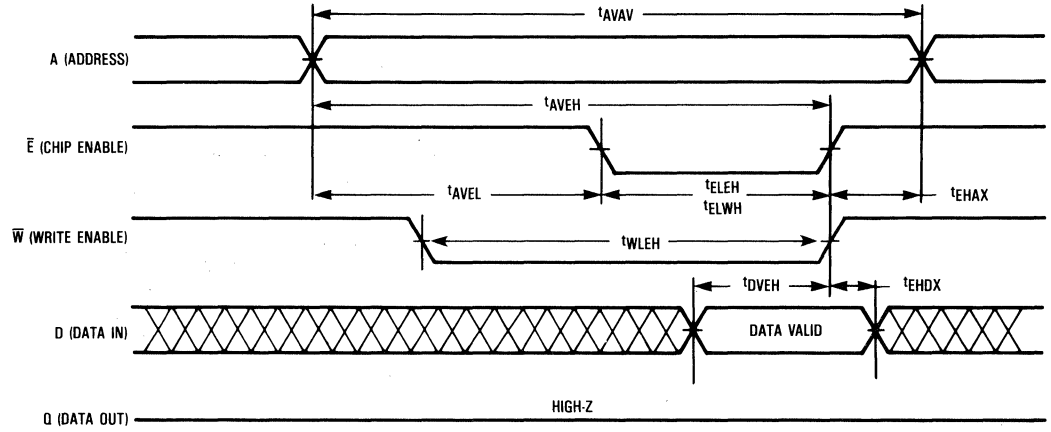
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6207-25		MCM6207-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20	—	25	—	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	20	—	25	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	20	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6207 X XX

- MCM — Motorola Memory Prefix
- 6207 — Part Number
- X — Package (P = Plastic DIP, L = Ceramic Sidebraze DIP, J = Plastic SOJ)
- XX — Speed (25 = 25 ns, 35 = 35 ns)

Full Part Numbers — MCM6207P25, MCM6207P35, MCM6207L25, MCM6207L35, MCM6207J25, MCM6207J35

MCM6208

Product Preview

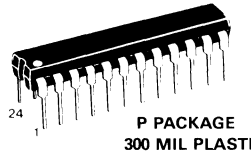
64K x 4 Bit Static Random Access Memory

The MCM6208 is a 262,144 bit static random access memory organized as 65,536 words of 4 bits, fabricated using Motorola's third-generation high-performance silicon-gate CMOS (HCMOS IV) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

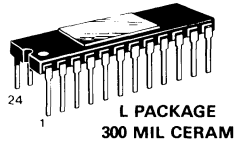
The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features reduce system power requirements without degrading access time performance.

The MCM6208 is available in a 300 mil, 24 lead ceramic sidebraze or plastic DIP, and will also be available in a 300 mil, 24 lead plastic surface-mount SOJ package.

- Single 5 V ±10% Power Supply
- Fast Access Time: 25/35 ns
- Equal Address and Chip Enable Access Time
- Three State Outputs
- Fully TTL Compatible
- Low Power Operation: 120/110 mA Maximum, Active AC
- High Board Density SOJ Package to be Available



P PACKAGE
300 MIL PLASTIC
CASE 724

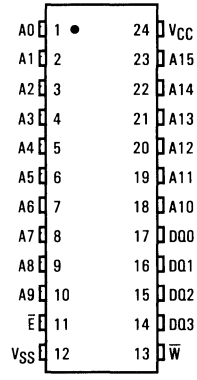


L PACKAGE
300 MIL CERAMIC
CASE 716

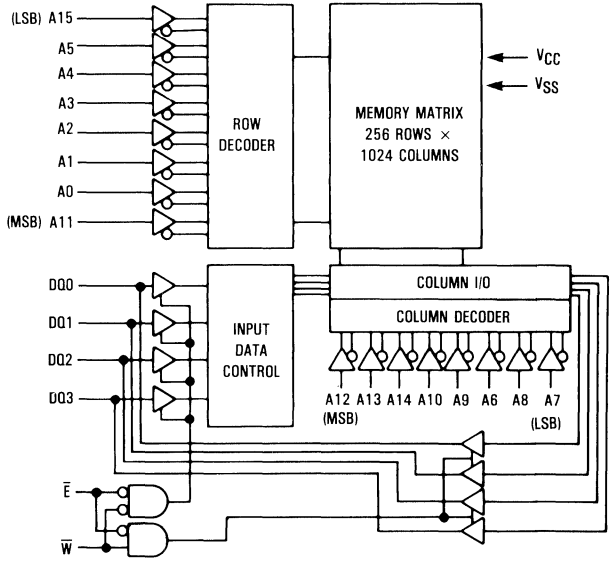
WILL BE AVAILABLE IN 24-LEAD, 300-MIL, SURFACE MOUNT SOJ PACKAGE

4

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES	
A0-A15	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic Ceramic	T_{stg}	−55 to +125 −65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out} = 0 mA)	MCM6208-25: t_{AVAV} = 25 ns	I_{CCA}	—	120	mA
	MCM6208-35: t_{AVAV} = 35 ns		—	110	
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	—	TBD	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} −0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	TBD	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$ and DQ	C_{in}	4	6	pF
	$\overline{E}$		5	7	
I/O Capacitance	DQ	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

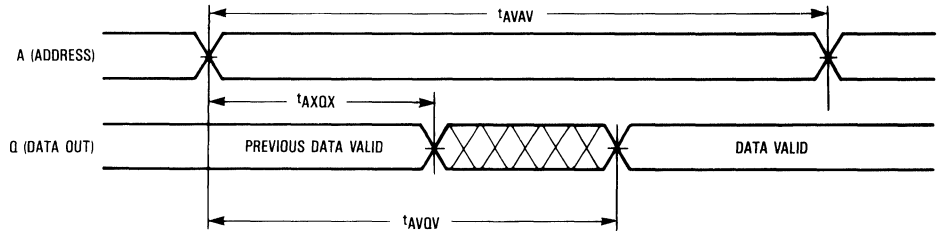
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . See Figure 1A

READ CYCLE (See Note 1)

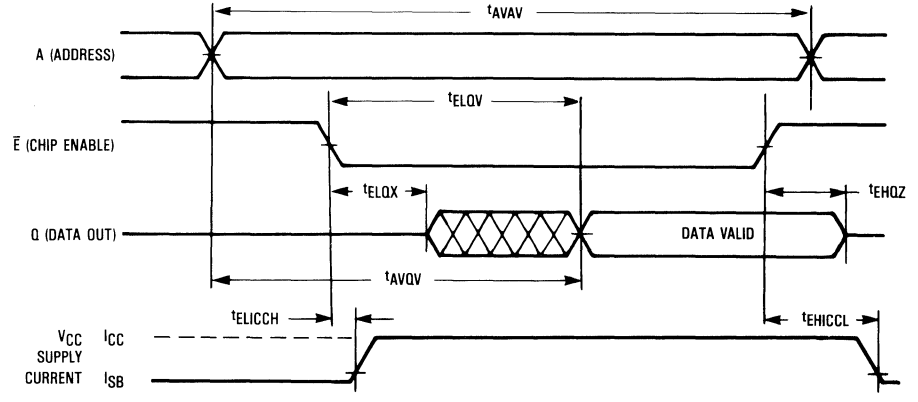
Parameter	Symbol		MCM6208-25		MCM6208-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	–	35	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	25	–	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	–	25	–	35	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	–	10	–	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	10	0	15	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	25	–	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E} = V_{IL}$).

READ CYCLE 1 (See Note 7 Above)



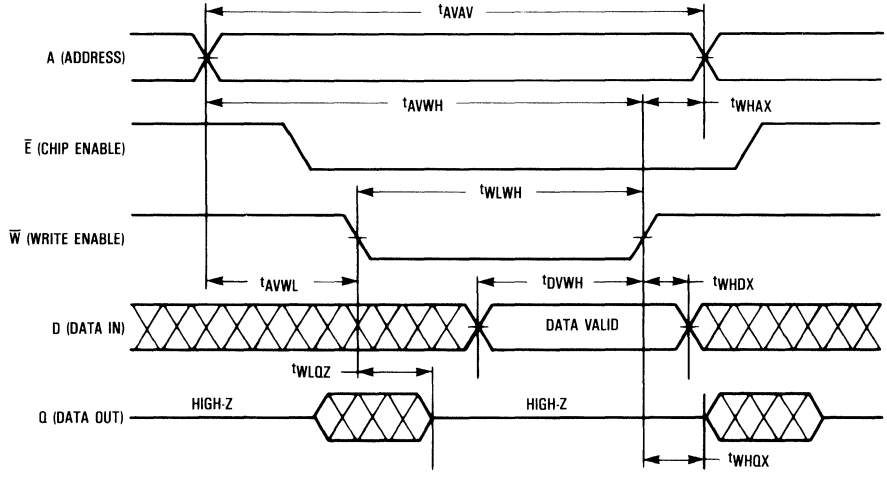
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6208-25		MCM6208-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	30	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	10	0	15	ns	3,4,5
Write High to Outut Active	t_{WHQX}	t_{OW}	5	—	10	—	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.



AC TEST LOADS

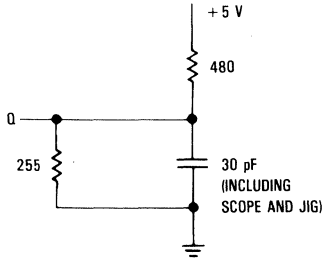


Figure 1A

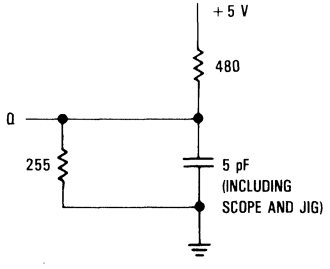


Figure 1B

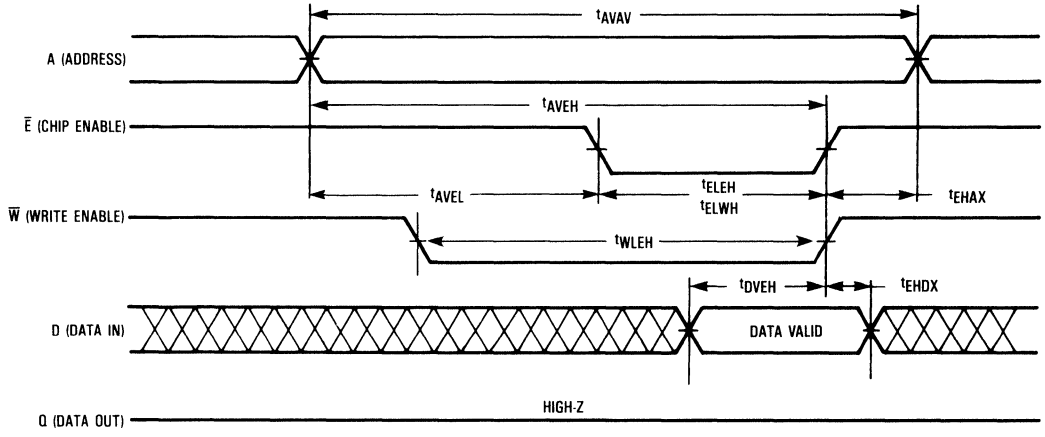
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6208-25		MCM6208-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	35	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	–	30	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20	–	30	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	20	–	30	–	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	20	–	30	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	–	15	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6208 X XX

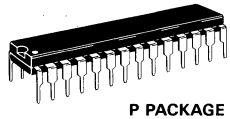
- MCM — Motorola Memory Prefix
- 6208 — Part Number
- X — Package (P = Plastic DIP, L = Ceramic Sidebraze DIP, J = Plastic SOJ)
- XX — Speed (25 = 25 ns, 35 = 35 ns)

Full Part Numbers — MCM6208P25, MCM6208P35, MCM6208L25, MCM6208L35, MCM6208J25, MCM6208J35

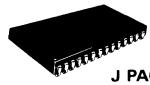
MCM6264

Product Preview

8K x 8 Bit Fast Static RAM



P PACKAGE
300 MIL PLASTIC



J PACKAGE
PLASTIC
CASE 810

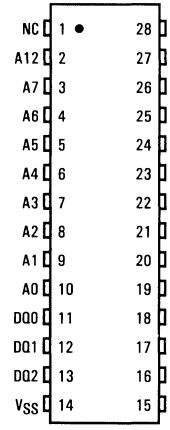
The MCM6264 is a 65,536 bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption which provides greater reliability.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

The MCM6264 is available in a 300 mil, 28 pin plastic dual-in-line package and a 400 mil, 28 pin plastic SOJ package. Both packages feature the JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Fast Access Time—35, 45 ns (Maximum)
- Low Power Operation—110/100 mA (Maximum, Active)
- Three State Outputs
- All Inputs and Outputs are TTL Compatible
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems

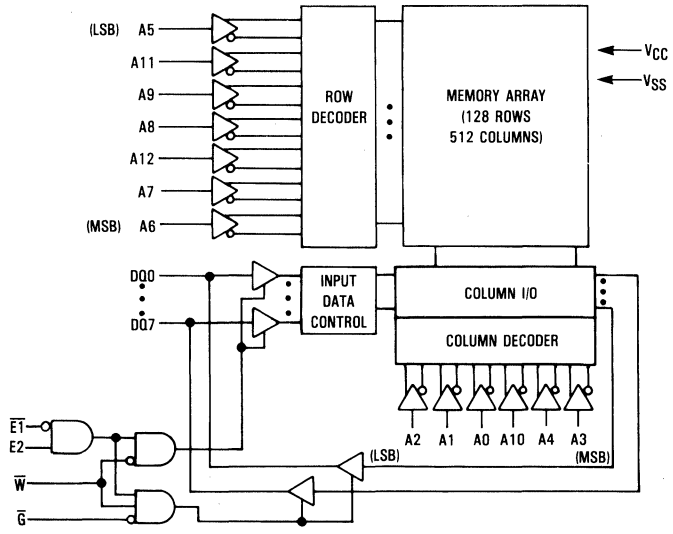
PIN ASSIGNMENT



PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

BLOCK DIAGRAM



This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	–	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	–	0.8	V

*V_{IL} (min) = −0.3 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	–	±1.0	μA
Power Supply Current	(t_{AVAV} = 35 ns)	I_{CC}	–	110	mA
($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{in} = V_{IH} or V_{IL}, I_{out} = 0)	(t_{AVAV} = 45 ns)		–	100	
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})		I_{SB1}	–	20	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ 0.2 V, V_{in} = V_{IH} or V_{in} = V_{IL})		I_{SB2}	–	15	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	6	pF
I/O Capacitance	DQ	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Input Timing Measurement Reference Levels . . . . . 1.5 V
Output Timing Measurement Reference Levels . . . . 0.8 and 2.0 V
Output Load . . . . . See Figure 1

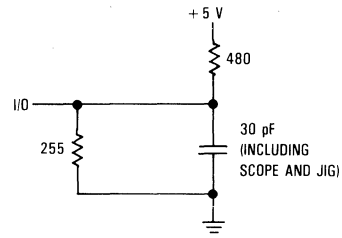


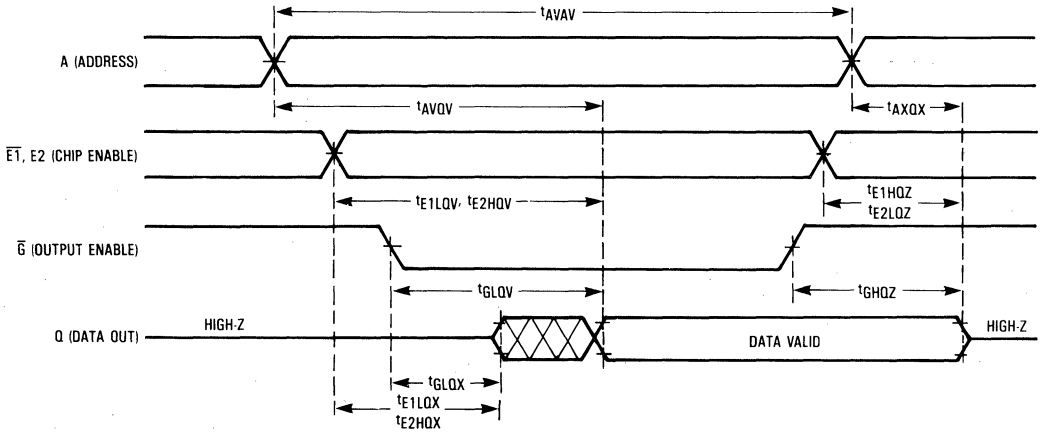
Figure 1. Test Load

4

READ CYCLE (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6264-35		MCM6264-45		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	35	—	45	—	ns	—
Address Cycle Time	t_{AVQV}	t_{AA}	—	35	—	45	ns	—
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	—	35	—	45	ns	—
E2 Access Time	t_{E2HQV}	t_{AC2}	—	35	—	45	ns	—
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	15	—	20	ns	—
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	—
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	5	—	5	—	ns	2, 3
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	0	—	0	—	ns	2, 3
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	0	15	0	20	ns	2, 3
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	0	15	0	20	ns	2, 3

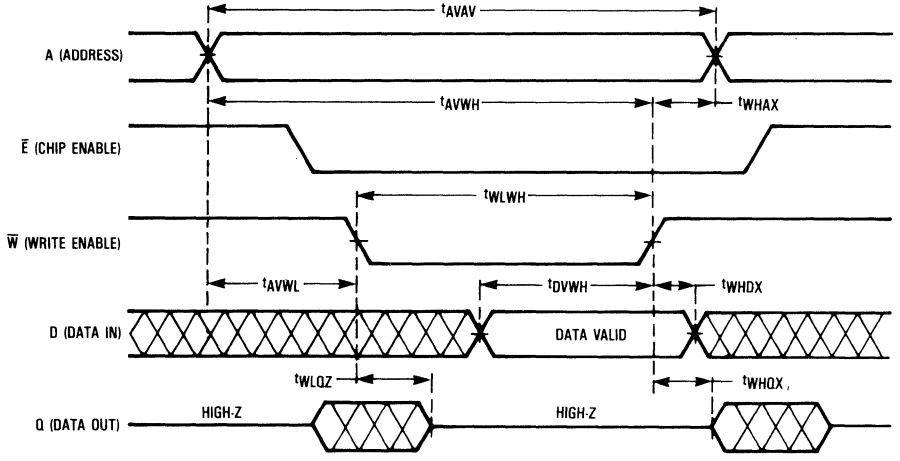
NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
3. These parameters are periodically sampled and not 100% tested.



WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6264-35		MCM6264-45		Unit	Notes
			Min	Max	Min	Max.		
Write Cycle Time	t_{AVAV}	t_{WC}	35	–	45	–	ns	–
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	–
Address Valid to End of Write	t_{AVWH}	t_{AW}	30	–	35	–	ns	–
Write Pulse Width	t_{WLWH}	t_{WP}	30	–	35	–	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	–	20	–	ns	–
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	3
Write Low to Output in High-Z	t_{WLQZ}	t_{WHZ}	0	15	0	20	ns	4, 5
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	–	5	–	ns	4, 5
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	–

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$, or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$, or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.
5. These parameters are periodically sampled and not 100% tested.



TIMING PARAMETER ABBREVIATIONS

t X X X X

- signal name from which interval is defined
- transition direction for first signal
- signal name to which interval is defined
- transition direction for second signal

The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

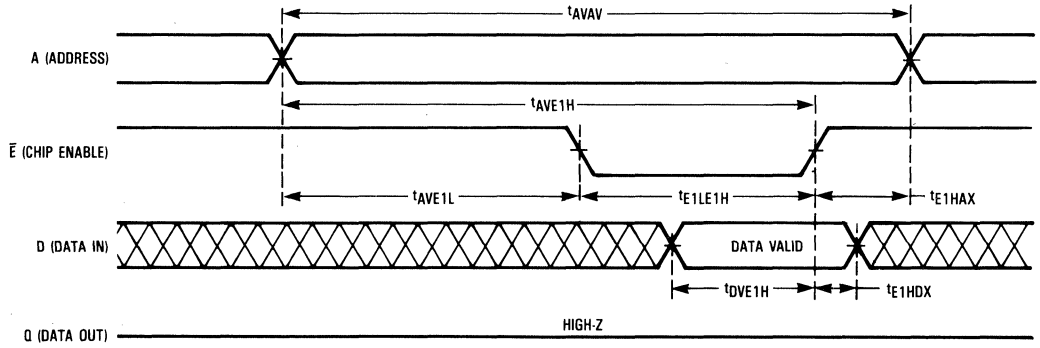
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Note 1)

Parameter	Symbol	Alt Symbol	MCM6264-35		MCM6264-45		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	35	–	45	–	ns	–
Address Setup Time	t_{AVE1L}	t_{AS}	0	–	0	–	ns	5
Address Valid to End of Write	t_{AVE1H}	t_{AW}	30	–	35	–	ns	5
Chip Enable to End of Write	t_{E1LE1H}	t_{CW}	30	–	35	–	ns	2, 5
Data Valid to End of Write	t_{DVE1H}	t_{DW}	15	–	20	–	ns	5
Data Hold Time	t_{E1HDX}	t_{DH}	0	–	0	–	ns	3, 5
Write Recovery Time	t_{E1HAX}	t_{WR}	0	–	0	–	ns	4, 5

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$, or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$, or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. $\overline{W}$ must be high during all address transitions.
5. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.



ORDERING INFORMATION
(Order by Full Part Number)

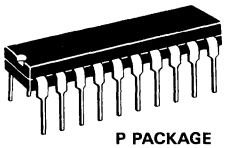
MCM 6264 X XX

- MCM — Motorola Memory Prefix
- 6264 — Part Number
- X — Package (P = Plastic DIP, J = Plastic SOJ)
- XX — Speed (35 = 35 ns, 45 = 45 ns)

Full Part Numbers — MCM6264P35, MCM6264P45, MCM6264J35, MCM6264J45

MCM6268

4K × 4 Bit Static Random Access Memory



P PACKAGE
PLASTIC
CASE 738

The MCM6268 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other sub-50 ns applications.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

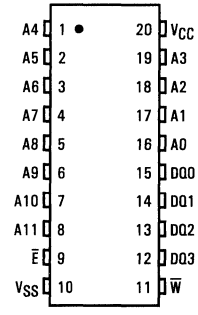
The MCM6268 is available in a 20 lead plastic dual-in-line package and features the standard JEDEC pinout.

- Single 5 V Supply, ±10%
- 4K × 4 Bit Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Three State Output
- Fully TTL Compatible
- Fast Access Time (Maximum):

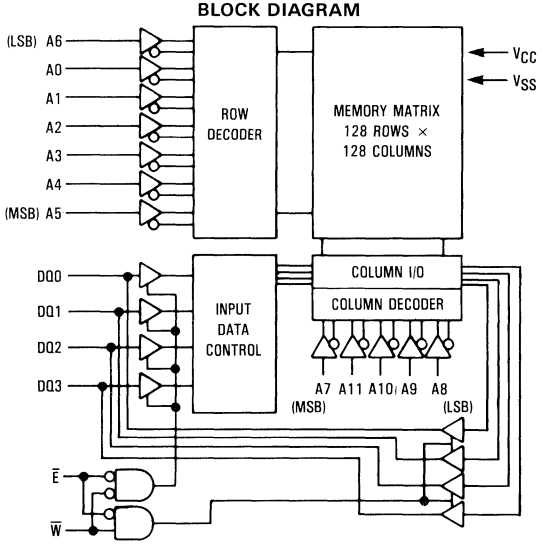
	Address	Chip Enable
MCM6268P25	25 ns	25 ns
MCM6268P35	35 ns	35 ns

- Low Power Operation: 120/110 mA Maximum, Active AC

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH}, V_{out}=0 to V_{CC})		$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out}=0 mA)	MCM6268-25: t_{AVAV}=25 ns	I_{CCA}	—	120	mA
	MCM6268-35: t_{AVAV}=35 ns		—	110	
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	15	mA
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	—	4	6	pF
	$\overline{E}$		—	5	7	
I/O Capacitance		$C_{I/O}$	—	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

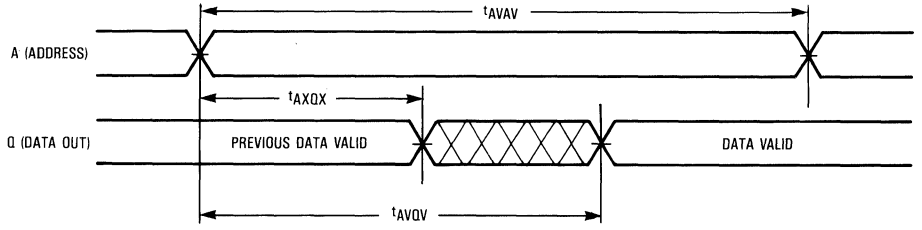
Input Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns
Output Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

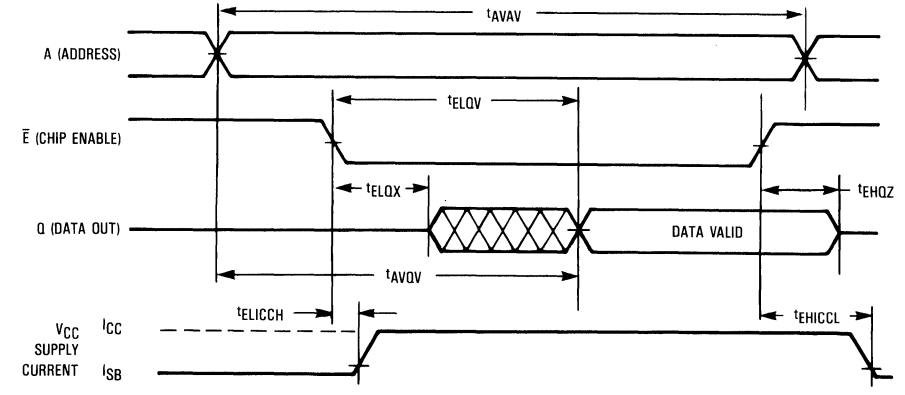
Parameter	Symbol		MCM6268P25		MCM6268P35		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	–	35	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	25	–	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	–	25	–	35	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	–	10	–	ns	3,4,5
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	10	0	15	ns	3,4,5
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	20	–	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{E} = V_{IL}$).
7. Addresses valid prior to or coincident with $\overline{E}$ going low.

READ CYCLE 1 (See Note 6 Above)



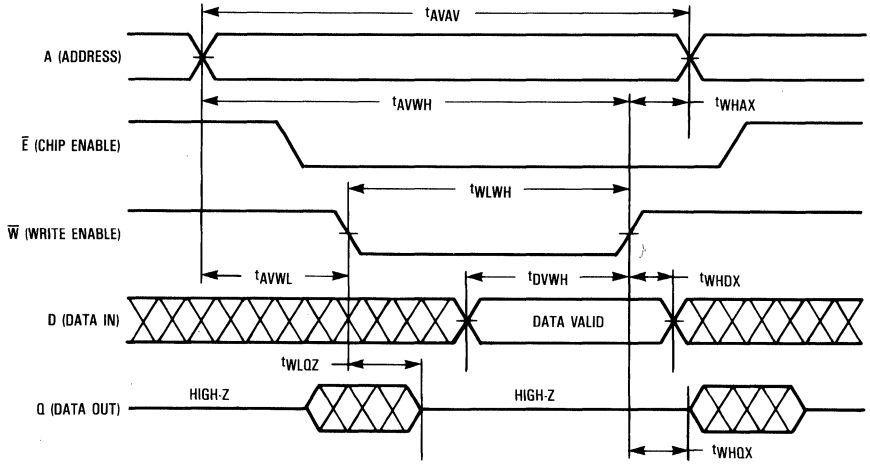
READ CYCLE 2 (See Note 7 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6268P25		MCM6268P35		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	30	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	10	0	15	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	10	—	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max, is less than t_{WHQX} min, both for a given device and from device to device.



AC TEST LOADS

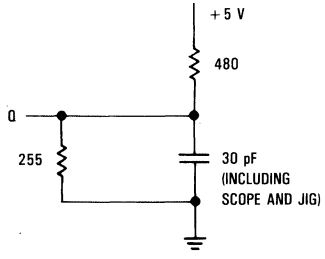


Figure 1A

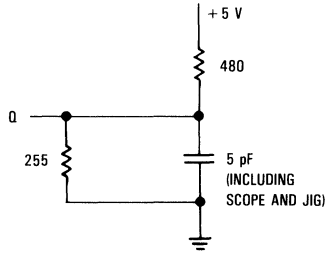


Figure 1B

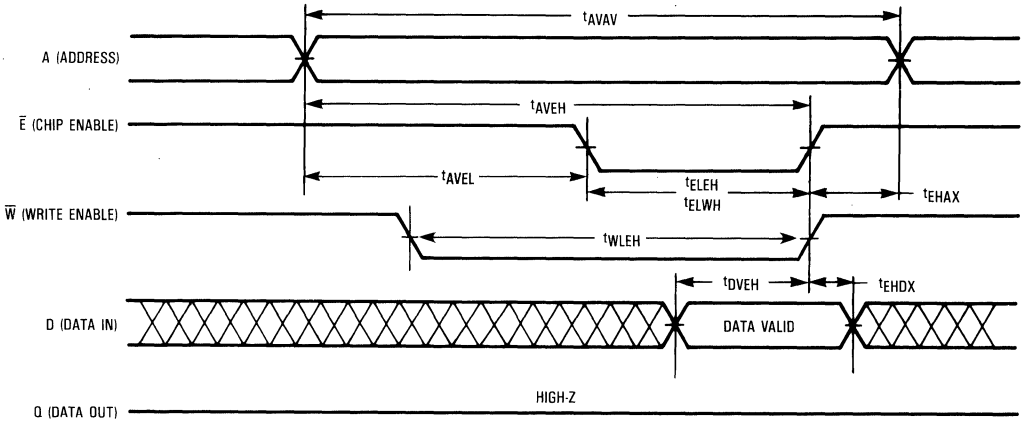
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

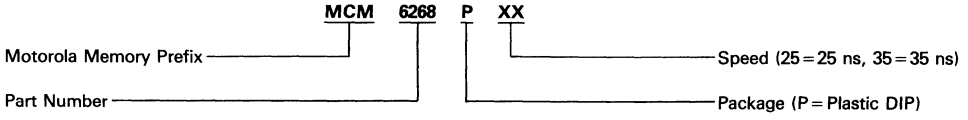
WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		MCM6268P25		MCM6268P35		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	—	30	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20	—	30	—	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	20	—	30	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	20	—	30	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

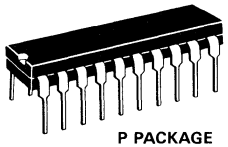


Full Part Numbers — MCM6268P25 MCM6268P35

MCM6269

Advance Information

4K x 4 Bit Static Random Access Memory



P PACKAGE
PLASTIC
CASE 738

4

The MCM6269 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other sub-50 ns applications.

Similar in design to the Motorola MCM6268, the MCM6269 features an enhanced chip select circuit allowing access to data in as little as 12 ns.

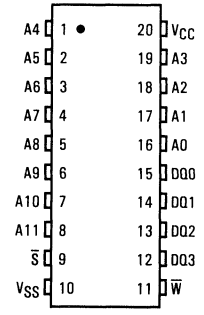
The MCM6269 is available in either a 20 lead plastic dual-in-line package or a ceramic leadless chip carrier; both feature the standard JEDEC pinout.

- Single 5 V Supply, ±10%
- 4K x 4 Bit Organization
- Fully Static—No Clock or Timing Strobes Necessary
- Three State Output
- Fully TTL Compatible
- Fast Access Time (Maximum):

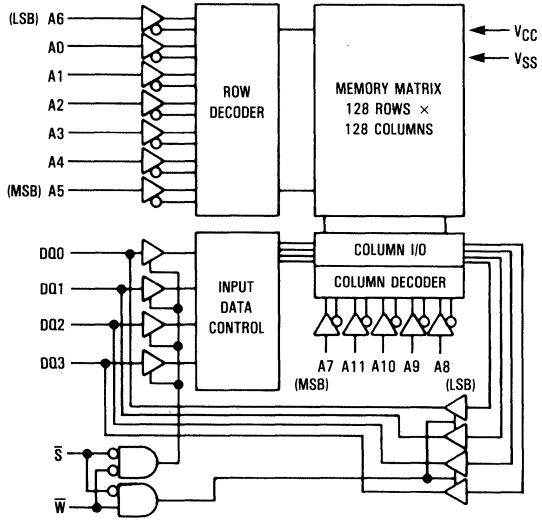
	Address	Chip Select
MCM6269P25	25 ns	12 ns
MCM6269P35	35 ns	15 ns

- Low Power Operation: 120/110 mA Maximum, Active AC

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A11	Address Input
W	Write Enable
S	Chip Select
DQ0-DQ3	Data Input/Output
VCC	+5 V Power Supply
VSS	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{S}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	Not Selected	I_{CCA}	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{S}$=V_{IH}, V_{out}=0 to V_{CC})		$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out}=0 mA)	MCM6269-25: t_{AVAV}=25 ns	I_{CCA}	—	120	mA
	MCM6269-35: t_{AVAV}=35 ns		—	110	
CMOS Standby Current ($\overline{S}$≥V_{CC}−0.2 V, V_{in}≤0.2 V, or ≥V_{CC}−0.2 V)		I_{SB}	—	15	mA
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{S}$	C_{in}	4	6	pF
	$\overline{S}$		5	7	
I/O Capacitance		$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

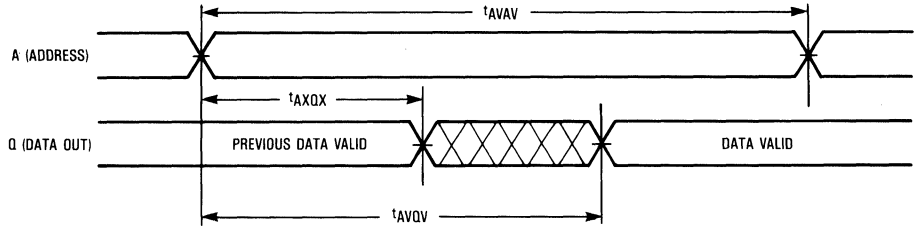
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

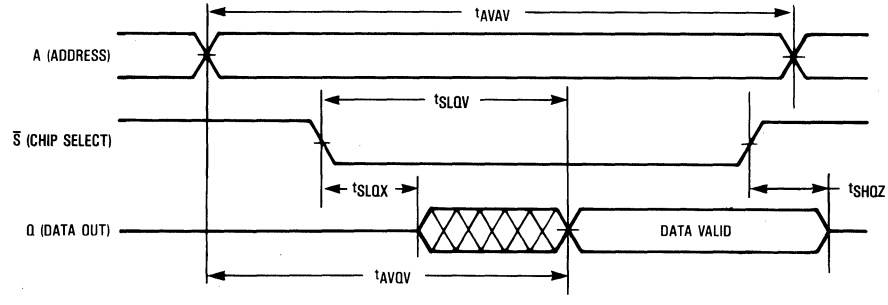
Parameter	Symbol		MCM6269P25		MCM6269P35		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	35	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	35	ns	
Select Access Time	t_{SLQV}	t_{ACS}	—	12	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	
Select Low to Output Active	t_{SLQX}	t_{LZ}	5	—	5	—	ns	3,4,5
Select High to Output High-Z	t_{SHQZ}	t_{HZ}	0	10	0	15	ns	3,4,5

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{SHQZ} max, is less than t_{SLQX} min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{S} = V_{IL}$).
7. Addresses valid prior to or coincident with $\overline{S}$ going low.

READ CYCLE 1 (See Note 6 Above)



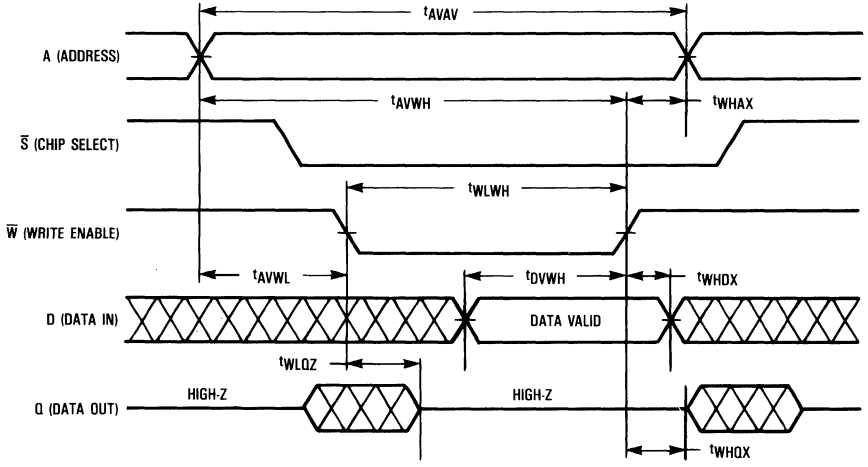
READ CYCLE 2 (See Note 7 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6269P25		MCM6269P35		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	30	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	30	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	10	0	15	ns	3,4,5
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	10	—	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ± 500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max, is less than t_{WHQX} min, both for a given device and from device to device.



AC TEST LOADS

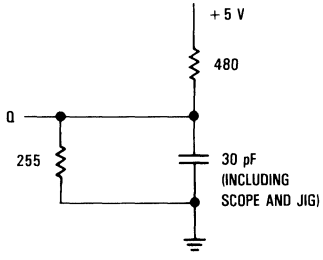


Figure 1A

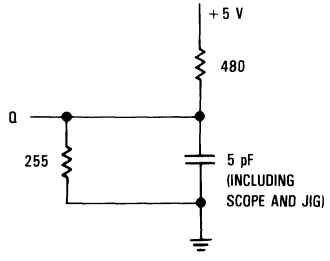


Figure 1B

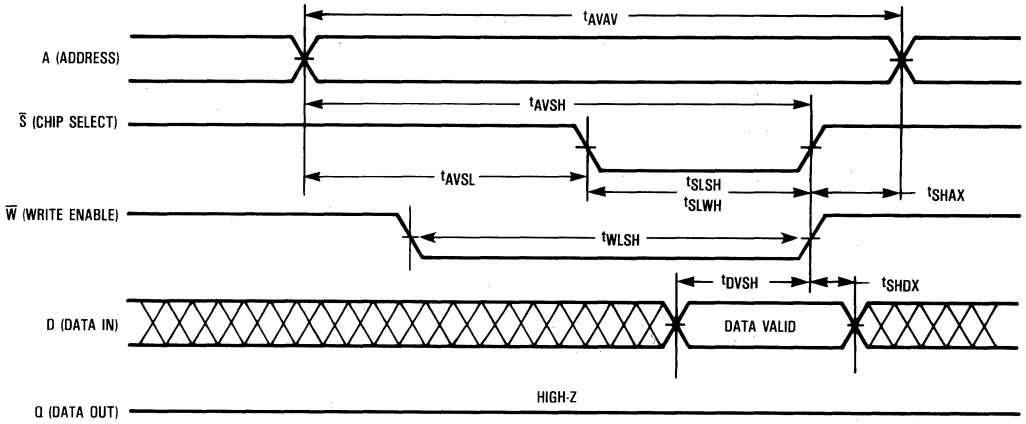
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{S}$ Controlled; See Note 1)

Parameter	Symbol		MCM6269P25		MCM6269P35		Units	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	ns	2
Address Setup Time	t_{AVSL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVSH}	t_{AW}	20	—	30	—	ns	
Select to End of Write	t_{SLSH}	t_{CW}	20	—	30	—	ns	3,4
Select to End of Write	t_{SLWH}	t_{CW}	20	—	30	—	ns	
Write Pulse Width	t_{WLSH}	t_{WP}	20	—	30	—	ns	
Data Valid to End of Write	t_{DVSH}	t_{DW}	10	—	15	—	ns	
Data Hold Time	t_{SHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{SHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{S}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{S}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{S}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6269 P XX

- MCM — Motorola Memory Prefix
- 6269 — Part Number
- P — Package (P = Plastic DIP)
- XX — Speed (25 = 25 ns, 35 = 35 ns)

Full Part Numbers — MCM6269P25 MCM6269P35

MCM6287

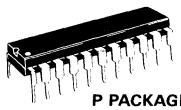
64K x 1 Bit Static Random Access Memory

The MCM6287 is a 65,536 bit static random access memory organized as 65,536 words of 1 bit, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

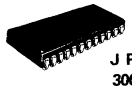
The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

The MCM6287 is available in a 300 mil, 22 lead plastic DIP or a ceramic leadless chip carrier measuring 290 x 490 mils, and will be available in a 24 lead, 300 mil, surface-mount SOJ package. All feature JEDEC standard pinout.

- Single 5 V ±10% Power Supply
- Fast Access Time: 25/35 ns
- Equal Address and Chip Enable Access Time
- Low Power Operation: 120/110 mA Maximum, Active AC
- High Board Density SOJ and Ceramic Leadless Chip Carrier (LCC) Available
- Three State Data Output
- Fully TTL Compatible



P PACKAGE
PLASTIC
CASE 736A



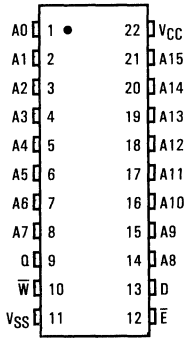
J PACKAGE
300 MIL SO
CASE 810A

Z PACKAGE
CERAMIC LCC

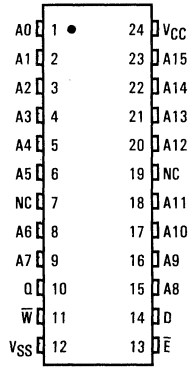
PIN NAMES	
A0-A15	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No Connection

PIN ASSIGNMENT

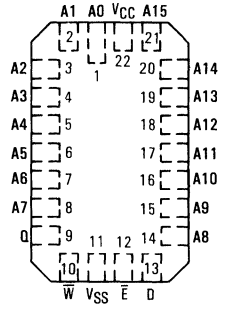
DUAL-IN-LINE



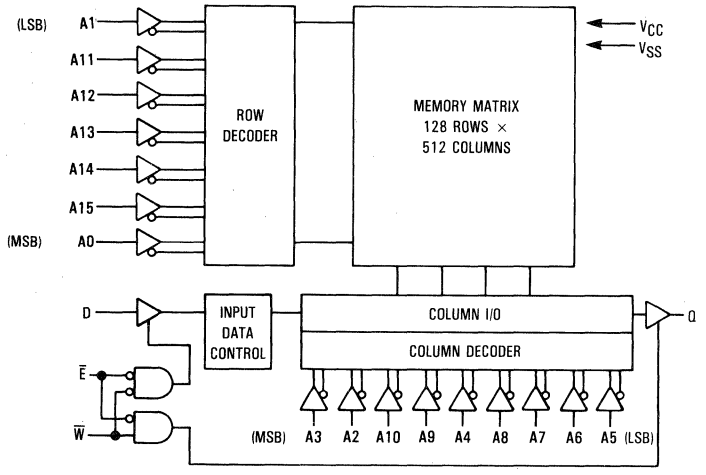
SMALL OUTLINE



CHIP CARRIER



BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature—Plastic Ceramic	T_{stg}	−55 to +125 −65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current (I_{out} = 0 mA)	MCM6287-25: t_{AVAV} = 25 ns	I_{CCA}	–	120	mA
	MCM6287-35: t_{AVAV} = 35 ns	I_{CCA}	–	110	
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	–	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} −0.2 V, No Restrictions on Other Inputs)		I_{SB2}	–	15	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
Output Capacitance		C_{out}	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

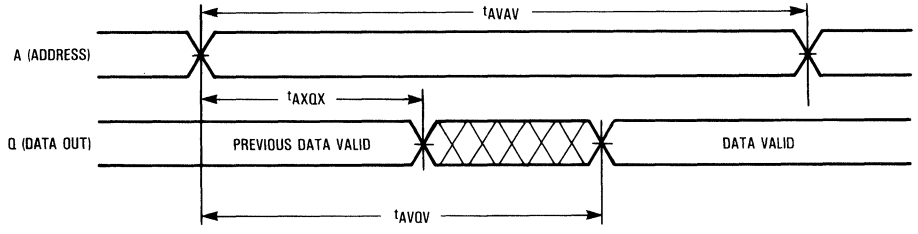
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

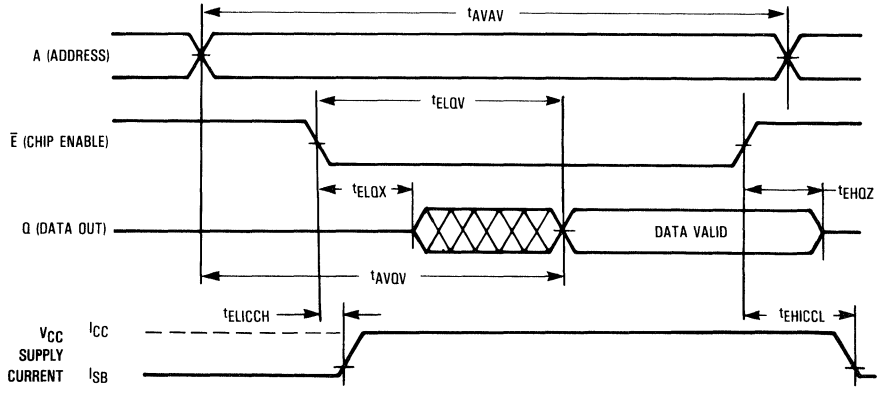
Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	35	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	25	—	35	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	15	0	15	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	25	—	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E} = V_{IL}$).

READ CYCLE 1 (See Note 7 Above)



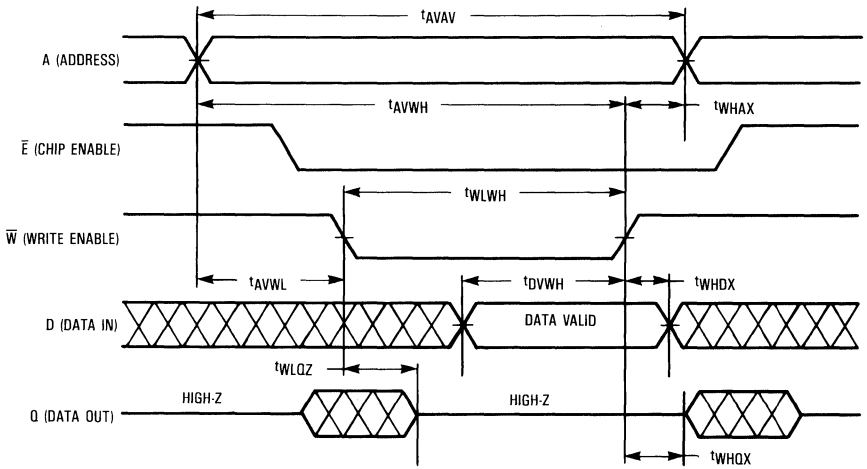
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	35	–	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	–	0	–	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	–	25	–	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	–	20	–	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	–	15	–	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	–	0	–	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	15	0	15	ns	3,4
Write High to Output Active	t_{WHQX}	t_{OW}	5	–	5	–	ns	3,4
Write Recovery Time	t_{WHAX}	t_{WR}	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.



AC TEST LOADS

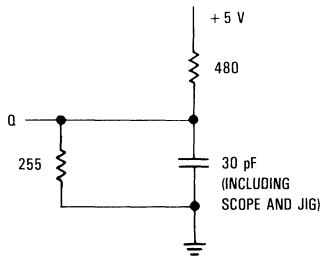


Figure 1A

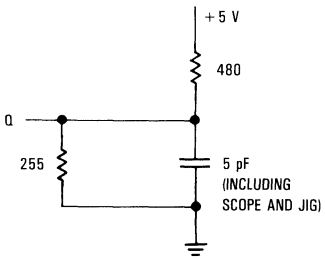


Figure 1B

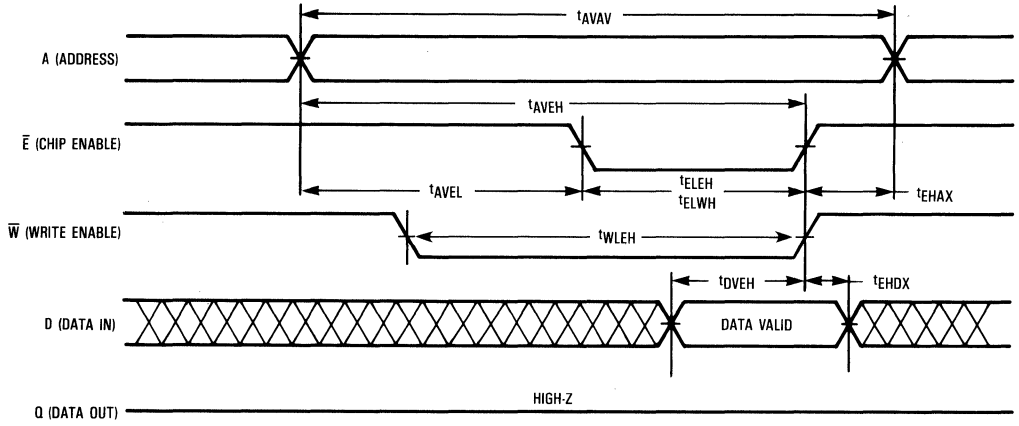
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6287-25		MCM6287-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	35	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	—	25	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20	—	25	—	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	20	—	25	—	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	20	—	20	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



TYPICAL CHARACTERISTICS

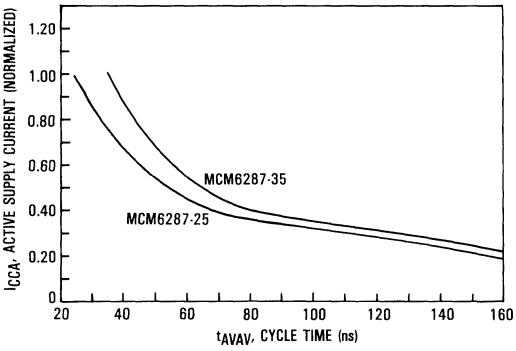


Figure 2. Relative Power versus Cycle Time

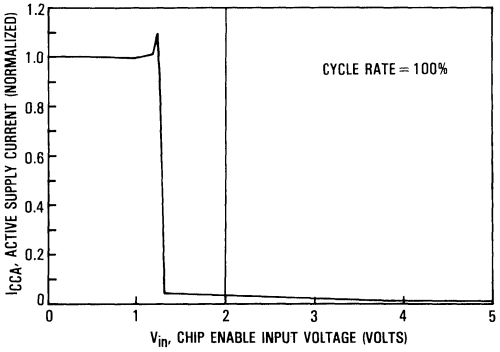


Figure 3. Active Supply Current versus Chip Enable Input Voltage

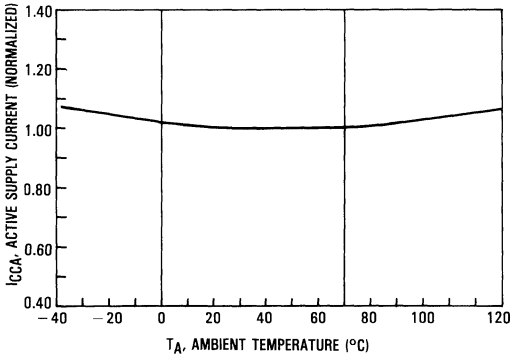


Figure 4. Active Supply Current versus Temperature

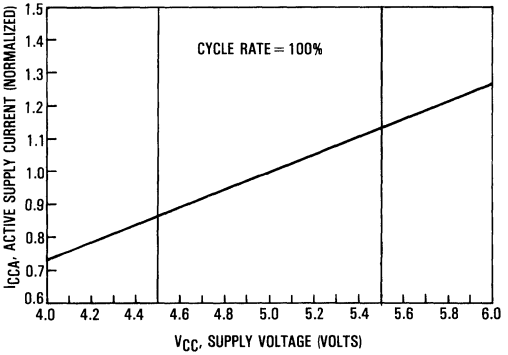


Figure 5. Active Supply Current versus Supply Voltage

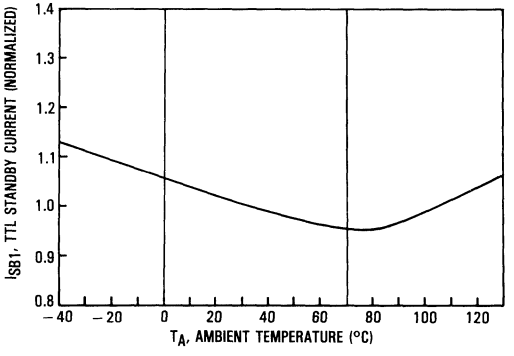


Figure 6. Standby Supply Current versus Temperature

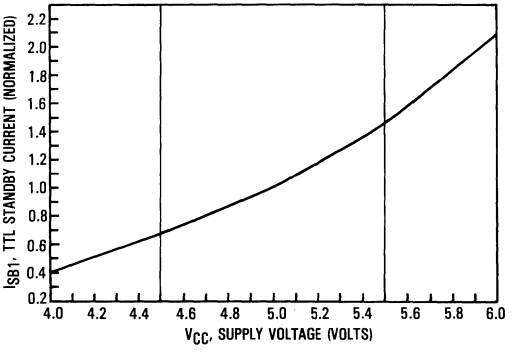


Figure 7. Standby Supply Current versus Supply Voltage

TYPICAL CHARACTERISTICS (Continued)

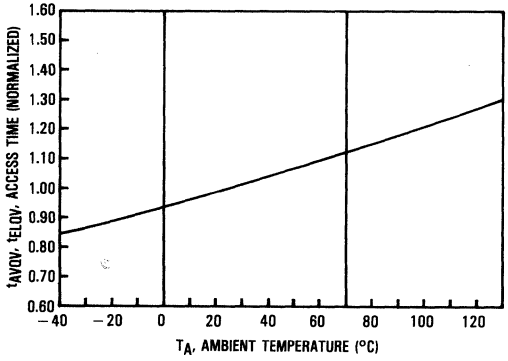


Figure 8. Address and Enable Access Times versus Temperature

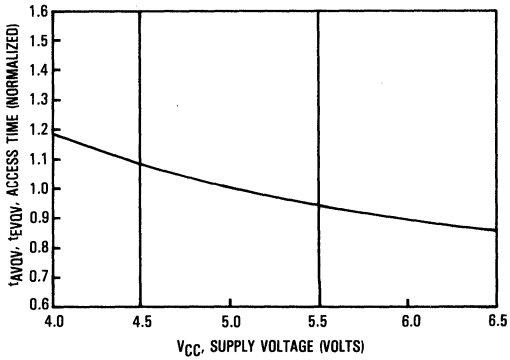


Figure 9. Address and Enable Access Times versus Supply Voltage

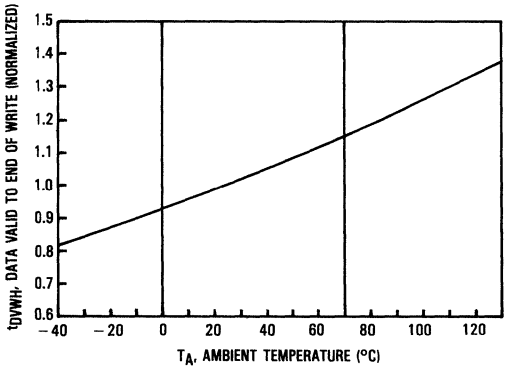


Figure 10. Data Setup Time versus Temperature

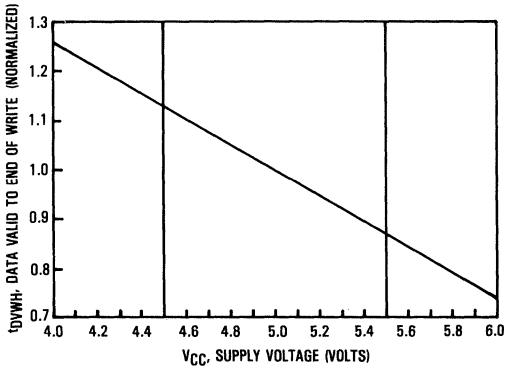


Figure 11. Data Setup Time versus Supply Voltage

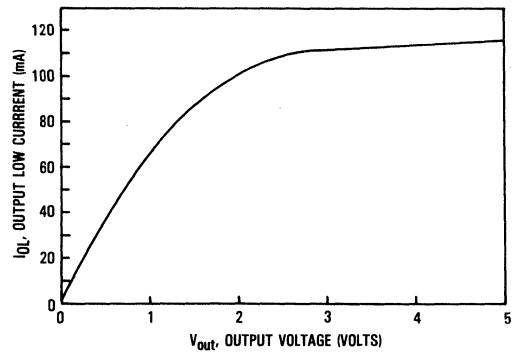


Figure 12. Output Sink Current versus Output Voltage

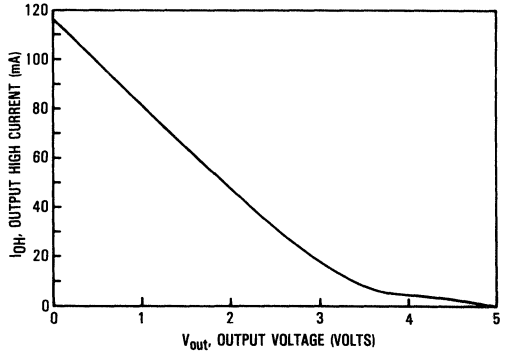
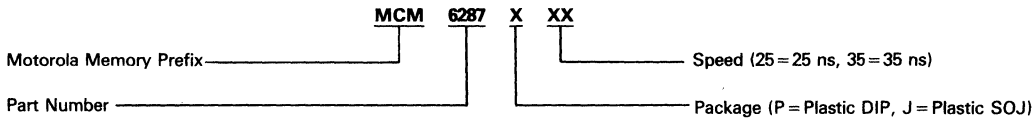


Figure 13. Output Source Current versus Output Voltage

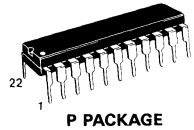
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6287P25 MCM6287P35
MCM6287J25 MCM6287J35

MCM6288

16K x 4 Bit Static Random Access Memory



P PACKAGE
PLASTIC
CASE 736A

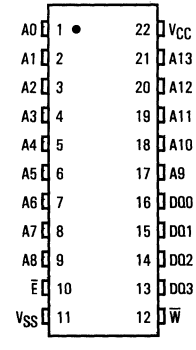
The MCM6288 is a 65,536 bit static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features reduce system power requirements without degrading access time performance.

The MCM6288 is available in a 300 mil, 22 lead plastic DIP, with JEDEC standard pinout. Also available is a 24-lead version, MCM6290, with fast output enable access times of 12 ns and 15 ns.

- Single 5 V ±10% Power Supply
- Fast Access Time: 25/30/35 ns
- Equal Address and Chip Enable Access Time
- Low Power Operation: 120/110 mA Maximum, Active AC
- Fully TTL Compatible
- Three-State Data Output

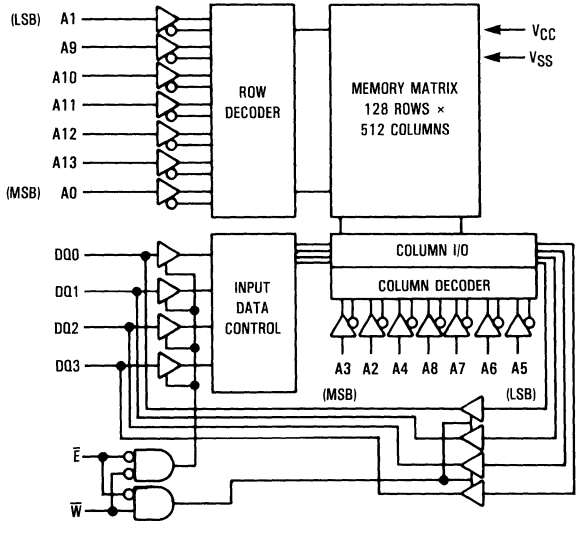
PIN ASSIGNMENT



PIN NAMES

A0-A13	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

BLOCK DIAGRAM



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	–
L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	L	Write	I_{CCA}	High-Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})		$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})		$I_{lkg(O)}$	–	±1.0	μA
AC Supply Current (I_{out} = 0 mA)	MCM6288-25: t_{AVAV} = 25 ns	I_{CCA}	–	120	mA
	MCM6288-30: t_{AVAV} = 30 ns		–	120	
	MCM6288-35: t_{AVAV} = 35 ns		–	110	
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	–	20	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} −0.2 V, No Restrictions on Other Inputs)		I_{SB2}	–	15	mA
Output Low Voltage (I_{OL} = 8.0 mA)		V_{OL}	–	0.4	V
Output High Voltage (I_{OH} = −4.0 mA)		V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
I/O Capacitance		$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

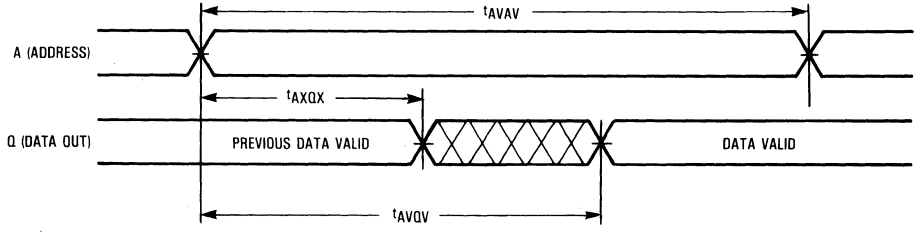
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

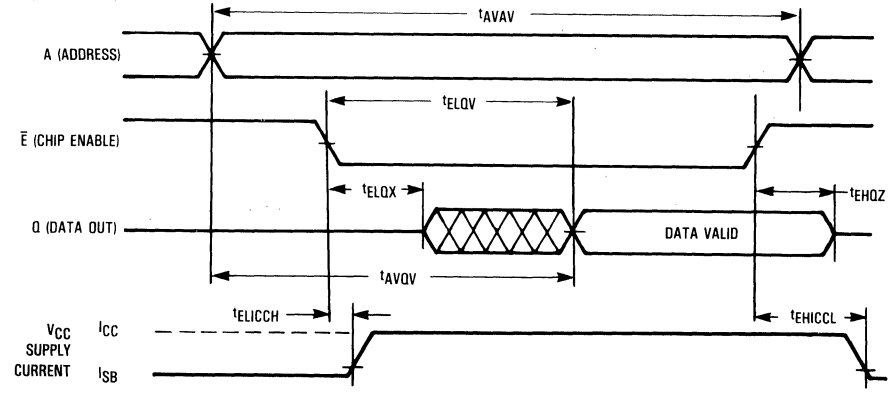
Parameter	Symbol		MCM6288P25		MCM6288P30		MCM6288P35		Units	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	–	30	–	35	–	ns	2
Address Access Time	t_{AVQV}	t_{AA}	–	25	–	30	–	35	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	–	25	–	30	–	35	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	–	7	–	10	–	ns	4,5,6
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	10	0	12	0	15	ns	4,5,6
Power Up Time	t_{ELICCH}	t_{PU}	0	–	0	–	0	–	ns	
Power Down Time	t_{EHICCL}	t_{PD}	–	25	–	30	–	30	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}).

READ CYCLE 1 (See Note 7 Above)



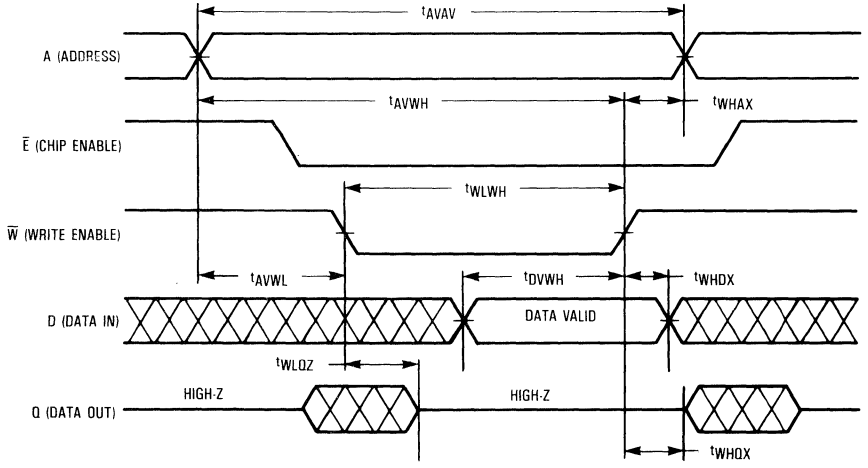
READ CYCLE 2 (See Note 3 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)

Parameter	Symbol		MCM6288P25		MCM6288P30		MCM6288P35		Units	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	30	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	25	—	30	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	12	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	10	0	12	0	15	ns	3,4,5
Write High to Outut Active	t_{WHQX}	t_{OW}	5	—	7	—	10	—	ns	3,4,5
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. Parameter is sampled and not 100% tested.
5. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.



AC TEST LOADS

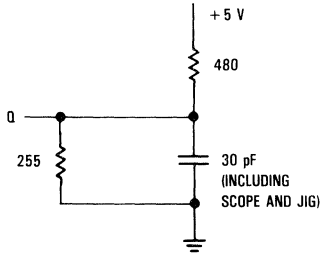


Figure 1A

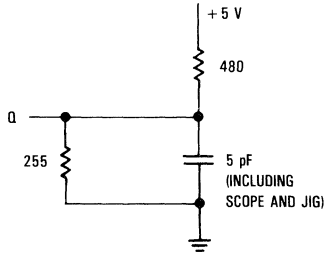


Figure 1B

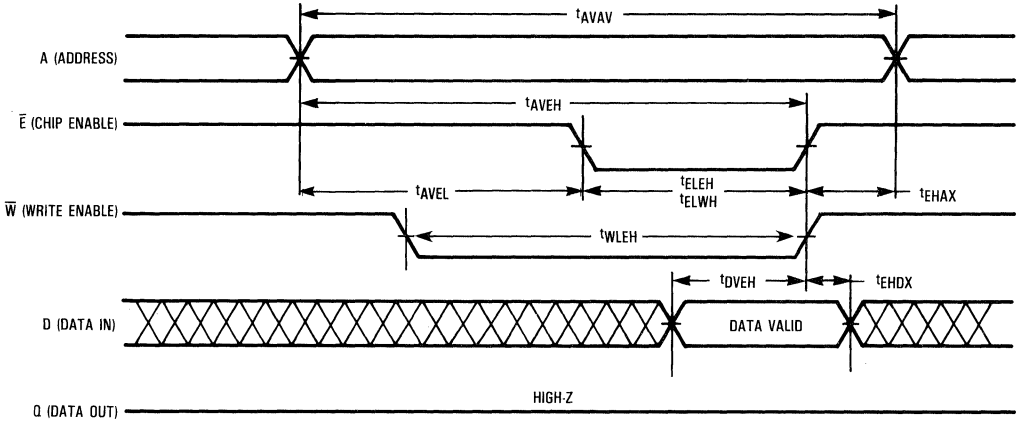
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled, See Note 1)

Parameter	Symbol		MCM6288P25		MCM6288P30		MCM6288P35		Units	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	30	–	35	–	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	–	25	–	30	–	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	20	–	25	–	30	–	ns	3,4
Enable to End of Write	t_{ELWH}	t_{CW}	20	–	25	–	30	–	ns	
Write Pulse Width	t_{WLEH}	t_{WP}	20	–	25	–	30	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	–	12	–	15	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



TYPICAL CHARACTERISTICS

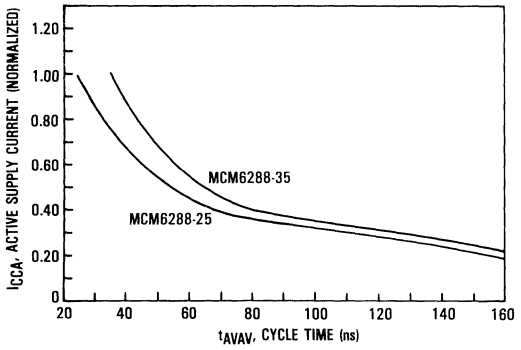


Figure 2. Relative Power versus Cycle Time

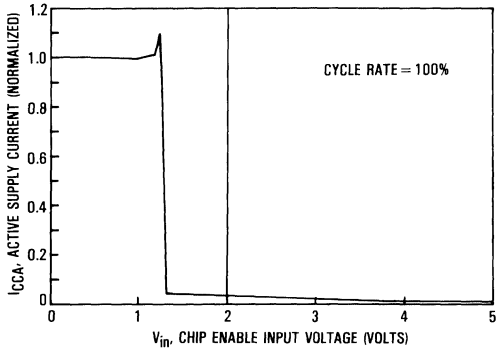


Figure 3. Active Supply Current versus Chip Enable Input Voltage

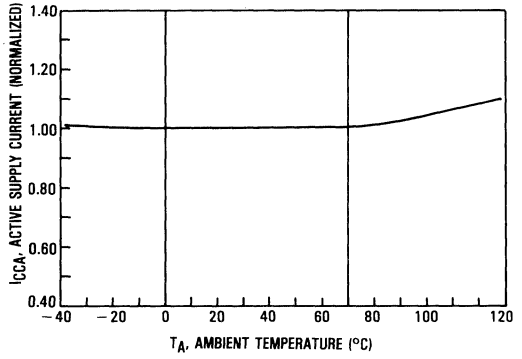


Figure 4. Active Supply Current versus Temperature

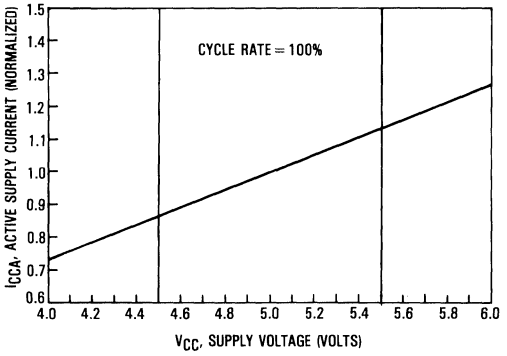


Figure 5. Active Supply Current versus Supply Voltage

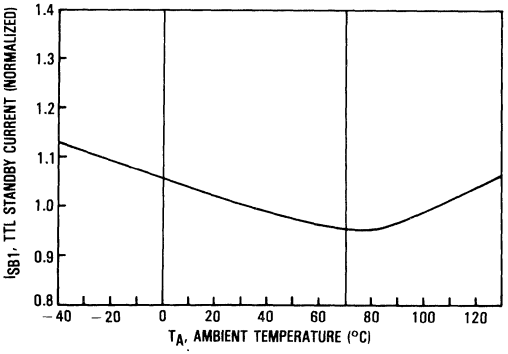


Figure 6. Standby Supply Current versus Temperature

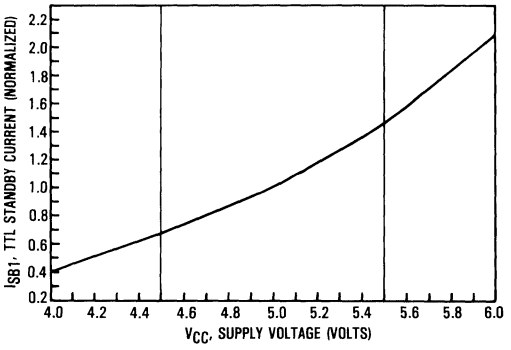


Figure 7. Standby Supply Current versus Supply Voltage

TYPICAL CHARACTERISTICS (Continued)

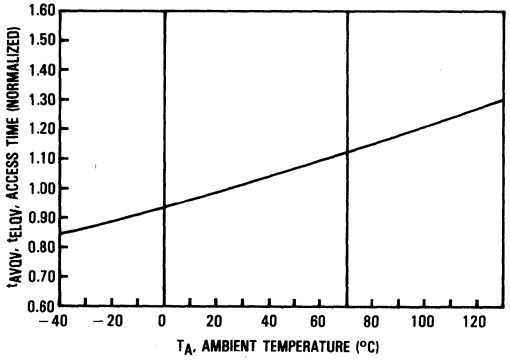


Figure 8. Address and Enable Access Times versus Temperature

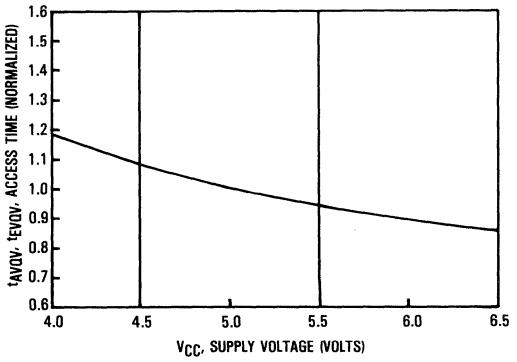


Figure 9. Address and Enable Access Times versus Supply Voltage

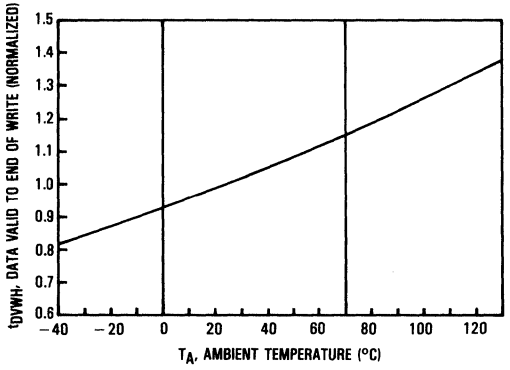


Figure 10. Data Setup Time versus Temperature

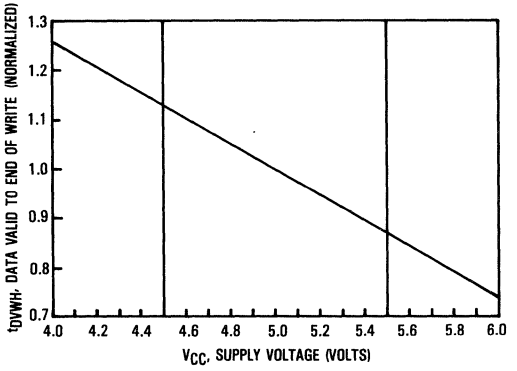


Figure 11. Data Setup Time versus Supply Voltage

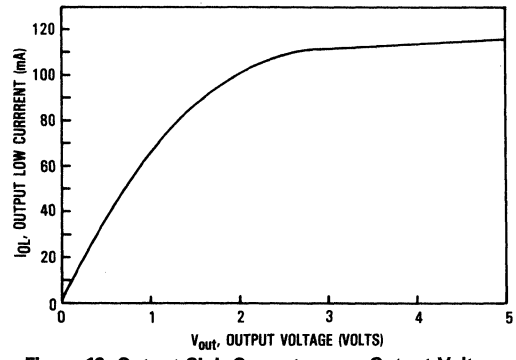


Figure 12. Output Sink Current versus Output Voltage

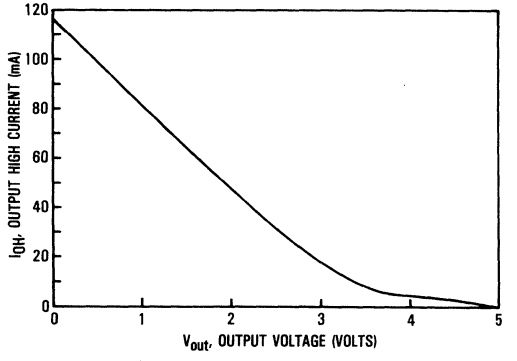
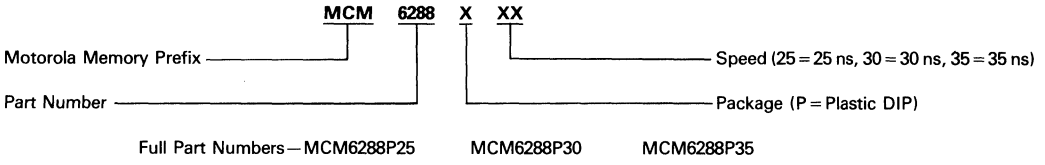


Figure 13. Output Source Current versus Output Voltage

ORDERING INFORMATION
(Order by Full Part Number)

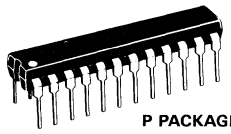


Full Part Numbers — MCM6288P25 MCM6288P30 MCM6288P35

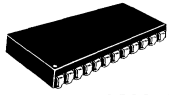
MCM6290

Advance Information

16K x 4 Bit Static Random Access Memory



P PACKAGE
300 MIL PLASTIC
CASE 724



J PACKAGE
300 MIL SOJ
CASE 810A

4

The MCM6290 is a 65,536 bit static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

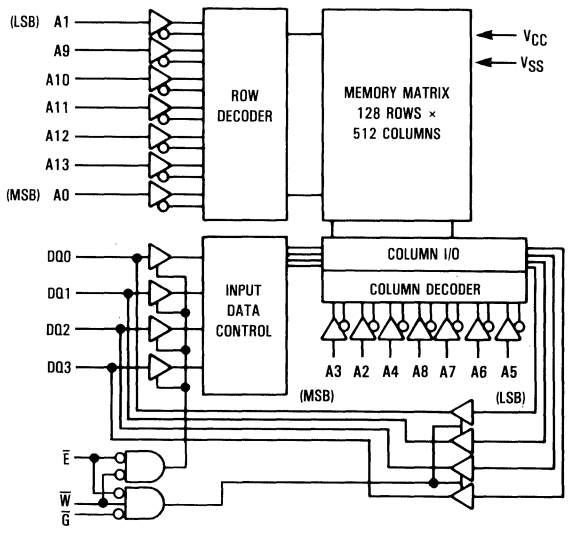
The MCM6290 is equipped with both chip enable ($\overline{E}$) and output enable ($\overline{G}$) inputs, allowing for greater system flexibility. Either input, when high, will force the outputs to high impedance.

- Single 5 V Supply, ±10%
- Fully Static—No Clock or Timing Strobes Necessary
- Three-State Outputs
- Fully TTL Compatible
- Fast Access Time (Maximum):

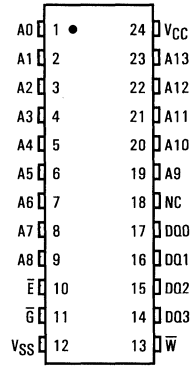
	Address	Chip Enable	Output Enable
MCM6290-25	25 ns	25 ns	12 ns
MCM6290-30	30 ns	30 ns	15 ns
MCM6290-35	35 ns	35 ns	15 ns

- Low Power Operation: 120/110 mA Maximum, Active AC
- Output Enable ($\overline{G}$) Feature for Increased System Flexibility and to Eliminate Bus Contention Problems

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
A0-A13	Address Input
DQ0-DQ3	Data Input/Output
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{E}$	Chip Enable
NC	No Connect
V_{CC}	+5 V Power Supply
V_{SS}	Ground

This document contains information on a new product. Specifications and information herein are subject to change without notice.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	X	Not Selected	I_{SB}	High-Z	—
L	H	H	Read	I_{CCA}	High-Z	—
L	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	X	L	Write	I_{CCA}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC})	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (+25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

4

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC}=5.0 V ±10%, T_A=0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter		Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in}=0 to V_{CC})		$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{E}$=V_{IH} or $\overline{G}$=V_{IH} or $\overline{W}$=V_{IL}, V_{out}=0 to V_{CC})		$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current (I_{out}=0 mA)	MCM6290-25: t_{AVAV}=25 ns	I_{CCA}	—	120	mA
	MCM6290-30: t_{AVAV}=30 ns		—	120	
	MCM6290-35: t_{AVAV}=35 ns		—	110	
TTL Standby Current ($\overline{E}$=V_{IH}, No Restrictions on Other Inputs)		I_{SB1}	—	20	mA
CMOS Standby Current ($\overline{E}$≥V_{CC}−0.2 V, No Restrictions on Other Inputs)		I_{SB2}	—	15	mA
Output Low Voltage (I_{OL}=8.0 mA)		V_{OL}	—	0.4	V
Output High Voltage (I_{OH}=−4.0 mA)		V_{OH}	2.4	—	V

CAPACITANCE (f=1.0 MHz, dV=3.0 V, T_A=25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	4	6	pF
	$\overline{E}$		5	7	
I/O Capacitance	DQ	$C_{I/O}$	5	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . 0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

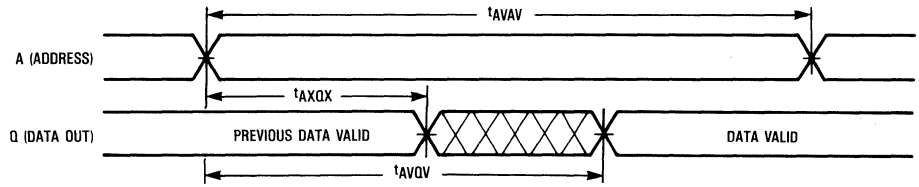
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

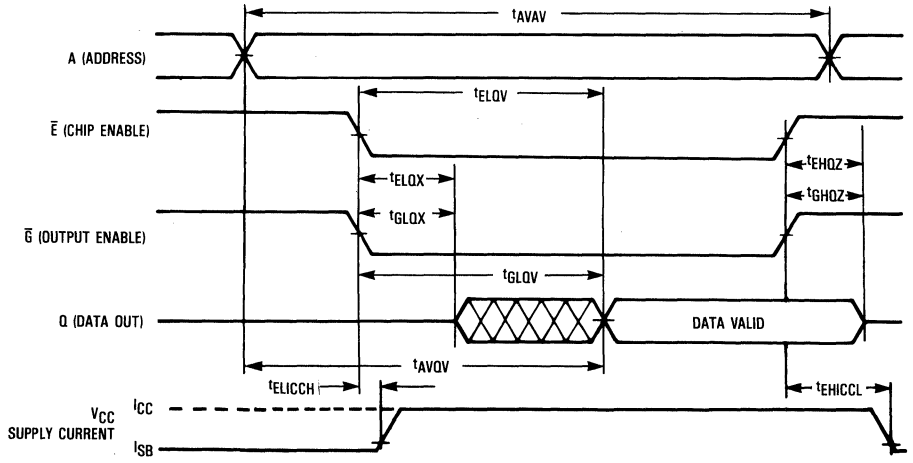
Parameter	Symbol		MCM6290-25		MCM6290-30		MCM6290-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	30	—	35	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	30	—	35	ns	
Chip Enable Access Time	t_{ELQV}	t_{ACS}	—	25	—	30	—	35	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	12	—	15	—	15	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	5	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	7	—	10	—	ns	3,4,5
Chip Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	10	0	12	0	15	ns	3,4,5
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	5	—	8	—	10	—	ns	3,4,5
Output Enable High to Output High-Z	t_{GHQZ}	t_{HZ}	0	10	0	12	0	15	ns	3,4,5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	25	—	30	—	30	ns	

NOTES: 1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. Device is continuously selected ($\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}).
7. Addresses valid prior to or coincident with $\overline{E}$ going low.

READ CYCLE 1 (See Note 6 Above)



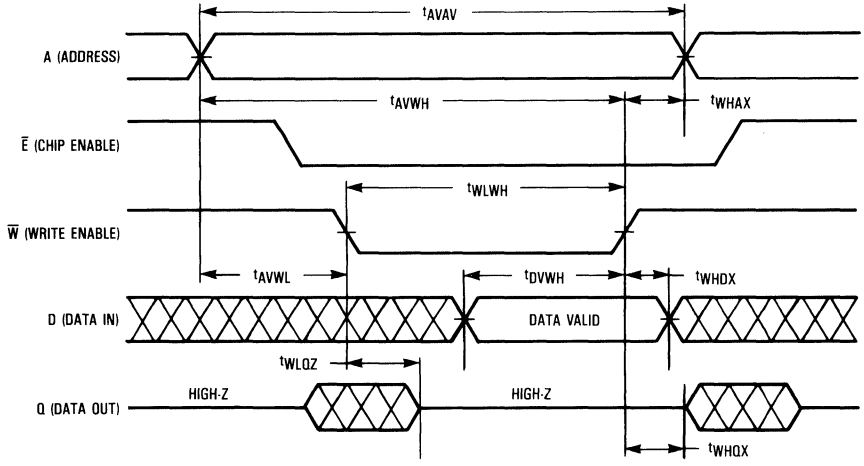
READ CYCLE 2 (See Note 7 Above)



WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM6290-25		MCM6290-30		MCM6290-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	30	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	25	—	30	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	12	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	10	0	12	0	15	ns	4,5,6
Write High to Output Active	t_{WHQX}	t_{OW}	5	—	8	—	10	—	ns	4,5,6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
5. Parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max, is less than t_{WHQX} min, both for a given device and from device to device.



AC TEST LOADS

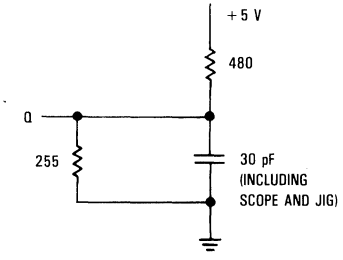


Figure 1A

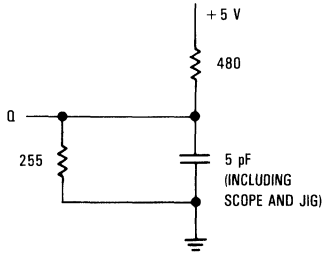
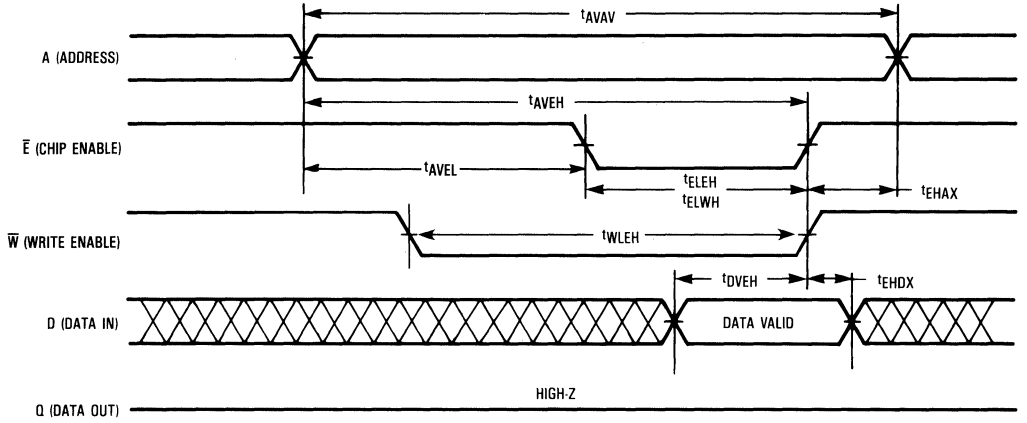


Figure 1B

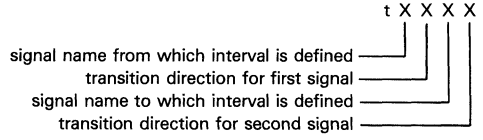
WRITE CYCLE 2 ($\overline{E}$ Controlled; See Notes 1 and 2)

Parameter	Symbol		MCM6290-25		MCM6290-30		MCM6290-35		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	–	30	–	35	–	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	–	0	–	0	–	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	20	–	25	–	30	–	ns	
Chip Enable to End of Write	t_{ELEH}	t_{CW}	20	–	25	–	30	–	ns	4,5
Chip Enable to End of Write	t_{ELWH}	t_{CW}	20	–	25	–	30	–	ns	4,5
Write Pulse Width	t_{WLEH}	t_{WP}	20	–	25	–	30	–	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	10	–	12	–	15	–	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	–	0	–	0	–	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	–	0	–	0	–	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{G}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance state.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

TYPICAL CHARACTERISTICS

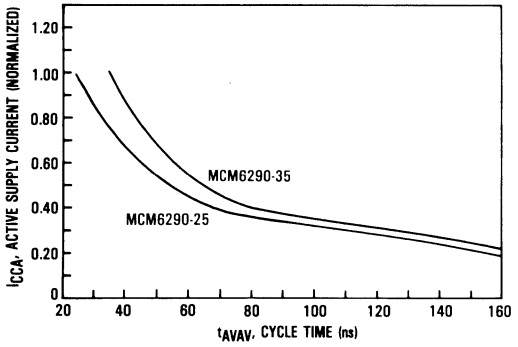


Figure 2. Relative Power versus Cycle Time

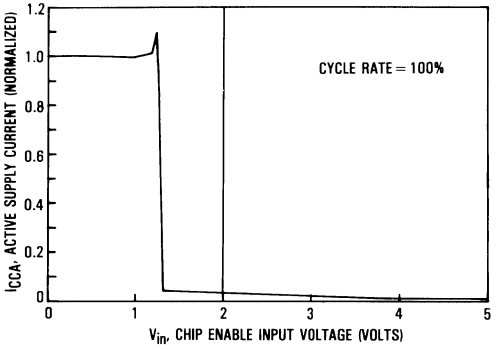


Figure 3. Active Supply Current versus Chip Enable Input Voltage

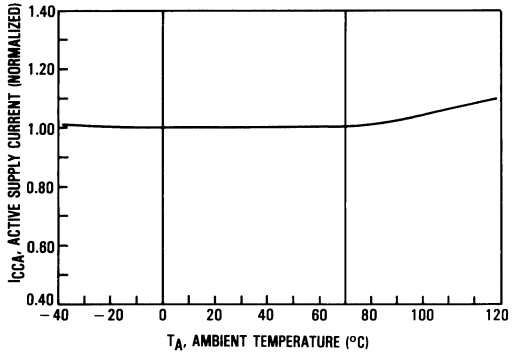


Figure 4. Active Supply Current versus Temperature

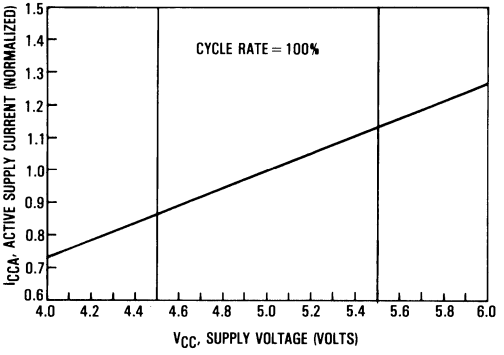


Figure 5. Active Supply Current versus Supply Voltage

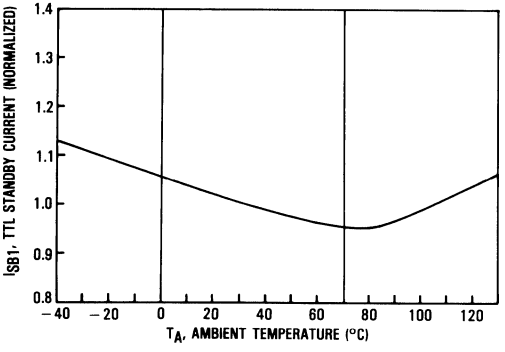


Figure 6. Standby Supply Current versus Temperature

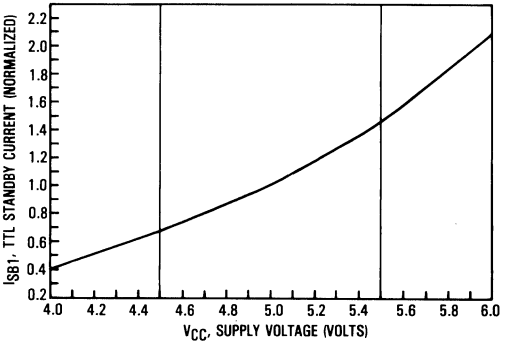


Figure 7. Standby Supply Current versus Supply Voltage

TYPICAL CHARACTERISTICS (Continued)

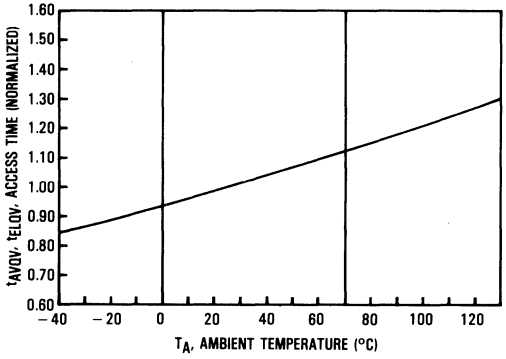


Figure 8. Address and Enable Access Times versus Temperature

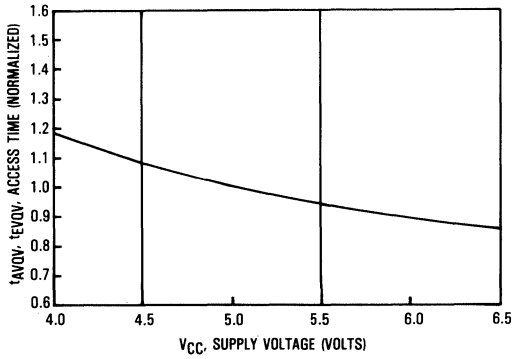


Figure 9. Address and Enable Access Times versus Supply Voltage

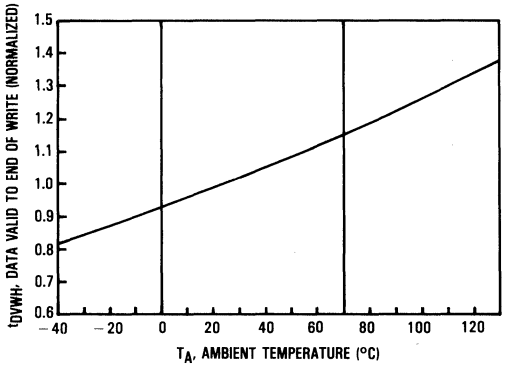


Figure 10. Data Setup Time versus Temperature

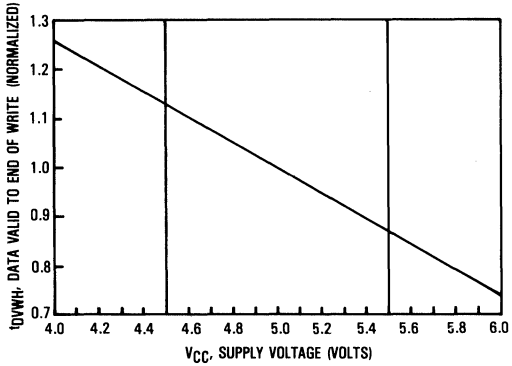


Figure 11. Data Setup Time versus Supply Voltage

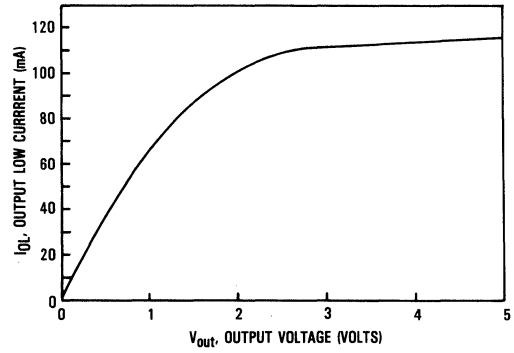


Figure 12. Output Sink Current versus Output Voltage

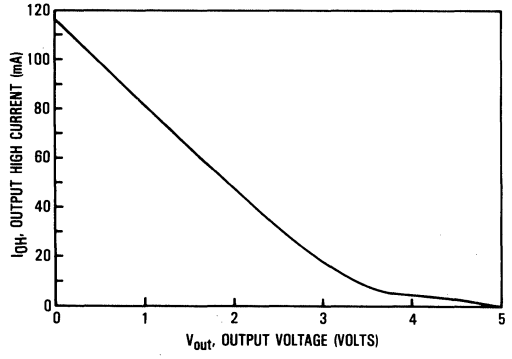
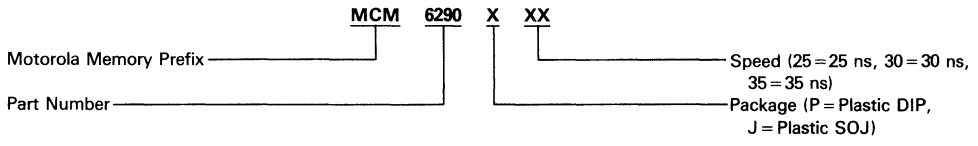


Figure 13. Output Source Current versus Output Voltage

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM6290P25	MCM6290P30	MCM6290P35
	MCM6290J25	MCM6290J30	MCM6290J35

4

Special Application MOS Static RAMs

5

5

Cache Tag RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Address to Match Time (ns max)	Pins
4K × 4	MCM62350P22	22	24
	MCM62350P25	25	24
	MCM62350P30	30	24
	MCM62350J22	22	24
	MCM62350J25	25	24
	MCM62350J30	30	24
	MCM62351P22	22	24
	MCM62351P25	25	24
	MCM62351P30	30	24
	MCM62351J22	22	24
	MCM62351J25	25	24
	MCM62351J30	30	24
	MCM4180P22	22	22
	MCM4180P25	25	22
	MCM4180P30	30	22

MOS Dual Port RAM

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (ns max)	Pins
256 × 8	MCM68HC34L	240	40
	MCM68HC34P	240	40

Synchronous Static RAMs

(+5 V, 0 to 70°C unless otherwise noted)

Organization	Part Number	Access Time (ns max)	Pins
16K × 4	MCM6292C25	25	28
	MCM6292C30	30	28
	MCM6292C35	35	28
	MCM6292J25	25	28
	MCM6292J30	30	28
	MCM6292J35	35	28
	MCM6293P25	25	28
	MCM6293P30	30	28
	MCM6293P35	35	28
	MCM6293J25	25	28
	MCM6293J30	30	28
	MCM6293J35	35	28
	MCM6294P25	25	28
	MCM6294P30	30	28
	MCM6294P35	35	28
	MCM6294J25	25	28
	MCM6294J30	30	28
	MCM6294J35	35	28
	MCM6295C25	25	28
	MCM6295C30	30	28
	MCM6295C35	35	28
	MCM6295J25	25	28
	MCM6295J30	30	28
	MCM6295J35	35	28

MCM68HC34

Advance Information

HCMOS
(HIGH DENSITY CMOS SILICON-GATE)

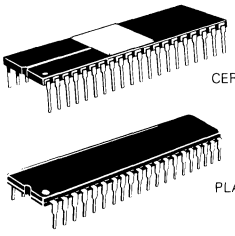
DUAL-PORT RAM
MEMORY UNIT

DUAL-PORT RAM MEMORY UNIT

The MCM68HC34 is a dual-port RAM memory (DPM) unit which enables two processors, arbitrarily referred to as "A" and "B", operating on two separate buses to exchange data without interfering with devices on the other bus. It contains 256 bytes of dual-port RAM which is the medium actually used for the interchange of data.

The dual-port memory unit contains six semaphore registers that provide a means for controlling access to the dual-port RAM or any other shared resources. It also contains interrupt registers which provide a means for the processors to interrupt each other.

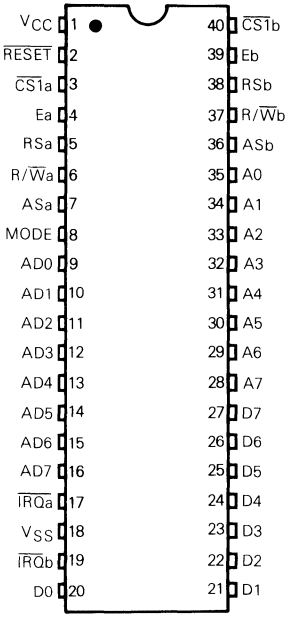
- High-Speed CMOS (HCMOS) Structure
- Six Read/Write Semaphore Registers
- 256 Bytes of Dual-Port RAM
- Eight Address Lines



L SUFFIX
CERAMIC PACKAGE
CASE 715

P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN ASSIGNMENT



ORDERING INFORMATION (T_A = 0° to 70°C)

Package Type	Order Number
Ceramic L Suffix	MCM68HC34L
Plastic P Suffix	MCM68HC34P

This document contains information on a new product. Specifications and information herein are subject to change without notice.

5

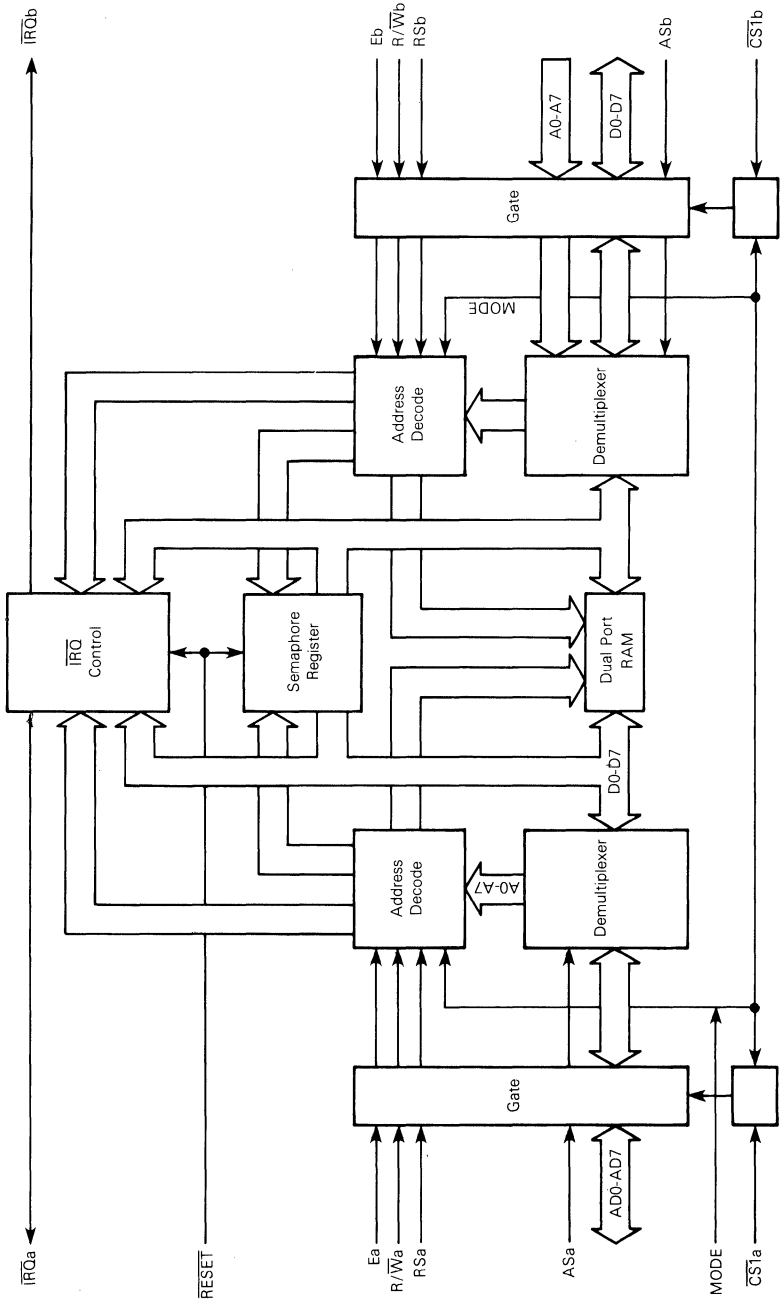


FIGURE 1 — BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

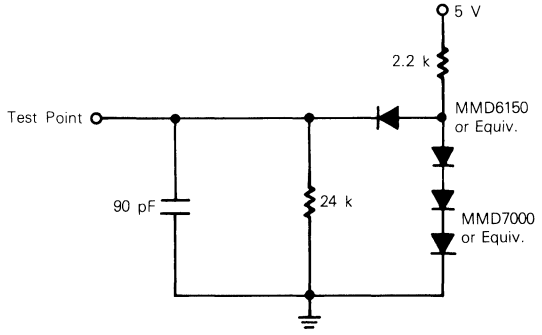
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to 7.0	V
Input Voltage, All Inputs	V_{in}	V_{SS}−0.3 to V_{CC}+0.5	V
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance Ceramic Plastic	θ_{JA}	 50 100	°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. Unused inputs must be tied to an appropriate logic level (either V_{CC} or V_{SS}) to reduce leakage currents and increase reliablity.

FIGURE 2 — BUS TIMING LOAD



DC ELECTRICAL CHARACTERISTCS (V_{CC} = 5.0 Vdc ±5%, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise noted)

Characteristics	Symbol	Min	Max	Unit
Input High Voltage (see Note 1)	V_{IH}	2.0	V_{CC}+0.3	V
Input Low Voltage (see Note 2)	V_{IL}	V_{SS}−0.3	0.8	V
Input Current (V_{in}=0 to V_{CC})	I_{in}	−	1.0	μA
Output Leakage Current	I_{OZ}	−	10.0	μA
Output High Voltage (I_{Load}= −100 μA) (I_{Load}= <10.0 μA)	V_{OH}	2.4 V_{CC}−0.1	− −	V
Output Low Voltage (I_{Load}=1.6 mA) (I_{Load}= <10.0 μA)	V_{OL}	− −	0.4 0.1	V
Current Drain — Outputs Unloaded Operating — Ea, Eb=1 MHz, Both Sides Active	I_{DD}	−	30	mA
Input Capacitance	C_{in}	−	10	pF
Output Capacitance (AD0-AD7 and D0-D7)	C_{out}	−	12	pF

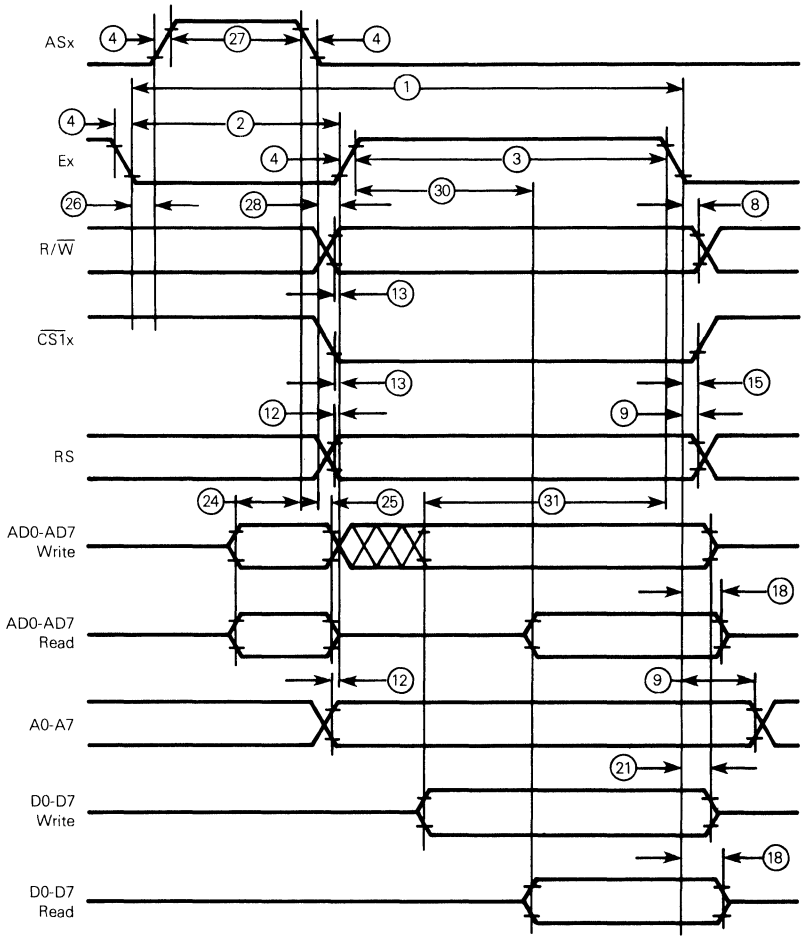
NOTES:
1. Input high voltage as stated is for all inputs except MODE. In the case of MODE, input high voltage is tied to V_{CC}.
2. Input low voltage as stated is for all inputs except MODE. In the case of MODE, input low voltage is tied to V_{SS} or is floating. If floating, the voltage will be internally pulled to V_{SS}.

BUS TIMING (See Notes 1 and 2 and Figure 2)

Ident Number	Characteristics	Symbol	Min	Max	Unit
1	Cycle Time	t_{cyc}	800	–	ns
2	Pulse Width, E Low	P_{WEL}	300	–	ns
3	Pulse Width, E High	P_{WEH}	325	–	ns
4	Input Rise and Fall Time	t_r, t_f	–	30	ns
8	Read/Write Hold Time	t_{RWH}	10	–	ns
9	Non-Multiplexed Address, RS Hold Time	t_{AH}	10	–	ns
12	Non-Multiplexed Address, RS Valid Time to Eb	t_{AV}	20	–	ns
13	R/$\overline{W}$, Chip Select Setup Time	t_{RWS}	20	–	ns
15	Chip Select Hold Time	t_{CH}	0	–	ns
18	Read Data Hold Time	t_{DHR}	20	75	ns
21	Write Data Hold Time	t_{DHW}	10	–	ns
24	Address Setup Time for Latch	t_{ASL}	20	–	ns
25	Address Hold Time for Latch	t_{AHL}	20	–	ns
26	Delay Time E to AS Rise	t_{ASD}	60	–	ns
27	Pulse Width, AS High	PW_{ASH}	110	–	ns
28	Address Strobe to E Delay	t_{ASED}	20	–	ns
30	Read Data Delay Time	t_{DDR}	–	240	ns
31	Write Data Setup Time	t_{DSW}	100	–	ns

NOTES:
1. Timing numbers relative to one side only. No numbers are intended to be cross-referenced from one side to the other.
2. Measurement points shown for ac timing are 0.8 V and 2.0 V, unless otherwise specified.

BUS TIMING DIAGRAMS



SIGNAL DESCRIPTION

The following paragraphs contain a brief description of the input and output signals.

V_{CC} AND V_{SS}

These pins supply power to the DPM. V_{CC} is +5 volts ±5% and V_{SS} is 0 volts or ground.

E CLOCK INPUTS (Ea AND Eb)

These are the input clocks from the respective processors and are positive during the latter portion of the bus cycle.

REGISTER SELECT INPUTS (RSa AND RSb)

These inputs function as register select inputs. A high on the RSa for side A or RSb for side B input allows selection of the semaphore and interrupt registers respectively for side A and side B by the lower three address bits. A low on RSa or RSb selects 256 bytes of RAM from side A or side B respectively.

5

CHIP SELECT INPUTS ($\overline{CS1}$a AND $\overline{CS1}$b)

These inputs function as chip select inputs for their respective sides. $\overline{CS1}$a must be low to select side A and $\overline{CS1}$b must be low to select side B. If $\overline{CS1}$a is high, side A is deselected. If $\overline{CS1}$b is high, side B is deselected.

MODE SELECT (MODE)

In normal operation, this pin should always be connected to V_{CC} (MODE = 1). Each side has three states controlled by RSa and $\overline{CS1}$a for side A and RSb and $\overline{CS1}$b for side B.

If $\overline{CS1}$a is high, side A cannot be accessed. If $\overline{CS1}$a is low, side A accesses either 256 bytes of RAM or the six semaphore registers and the two interrupt registers depending on the level of RSa. If RSa is low, 256 bytes of RAM are accessed and if RSa is high, the six semaphores and two interrupt registers are accessed.

The six semaphore and two interrupt registers are redundantly mapped in the 256 byte mode. That is, only the low order three bits select one of eight registers and the upper five bits of address are not decoded. Refer to Table 1.

TABLE 1 — SIDE A CONTROL SIGNAL OPERATION

Mode	$\overline{CS1}$a	RSa	Operation
1	0	0	Access 256 Byte RAM Side A
1	0	1	Access Semaphore/$\overline{IRQ}$ Side A on Lower Three Bits of Address
1	1	X	Side A Not Selected

The three states for side B in the 256 byte mode are controlled in the manner as side A using RSb and $\overline{CS1}$b except that side B uses separated address and data inputs. Refer to Table 2.

TABLE 2 — SIDE B CONTROL SIGNAL OPERATION

Mode	$\overline{CS1}$b	RSb	Operation
1	0	0	Access 256 Byte RAM Side B
1	0	1	Access Semaphore/$\overline{IRQ}$ Side B on Lower Three Bits of Address
1	1	X	Side B Not Selected

INTERRUPT REQUEST OUTPUTS ($\overline{IRQ}$a AND $\overline{IRQ}$b)

These pins are active low open-drain outputs. A write to address F9 from one side asserts an interrupt, if not masked on the other side. A write to address F9 sets this pin low.

B SIDE ADDRESS BUS INPUTS (A0-A7) AND B SIDE BIDIRECTIONAL DATA BUS (D0-D7)

When the B side is run from a multiplexed bus processor, the B side address pins are connected to the B side data pins, respectively (A0 to D0, A1 to D1, etc.).

SYSTEM RESET INPUT ($\overline{RESET}$)

A low level on this input causes the semaphore registers to be set to the states shown in Table 5 under **SEMAPHORE REGISTERS** and clears both bits of both $\overline{IRQ}$ registers to zeros. The RAM data is unaffected by $\overline{RESET}$.

ADDRESS STROBE INPUTS (ASa AND ASb)

The ASa input demultiplexes the eight low order address lines from the data lines on the A side. The falling edge of ASa latches the A side address within the DPM. The ASb input is used in the same manner when the B side is connected to a multiplexed bus. It must be connected to a high level when the B side is connected to a non-multiplexed bus.

A SIDE MULTIPLEXED ADDRESS/ BIDIRECTIONAL DATA BUS (AD0-AD7)

The A side can only be used with a multiplexed address/data bus. The A side addresses are on these lines during the time ASa is high. The lines are used as bidirectional data lines during the time Ea is high.

DUAL-PORT RAM

The dual-port memory unit contains 256 bytes of dual-port RAM that is accessed from either processor. It is selected in either case by eight address lines, register select, and chip select inputs. The direction of data transfer is controlled by the respective read/write (R/$\overline{W}$a or R/$\overline{W}$b) line. The dual-port RAM enables the processors to exchange data without interfering with devices on the other bus.

Simultaneous accesses by both sides of different locations of dual-port RAM will cause no ambiguities. Simultaneous reads by both sides of the same dual-port RAM location gives the proper data to both sides. On a simultaneous write and read of the same location, the data written is put into RAM but the data read is undefined. Simultaneous writes to

the same RAM location result in undefined data being stored. Thus, simultaneous writes and simultaneous write and read to the same location should be avoided. The semaphore registers provide a tool for determining when the shared RAM is available.

SEMAPHORE REGISTERS

The dual-port memory unit contains six read/write semaphore registers. Only two bits of each register are used. Bit 7 is the semaphore (SEM) bit and bit 6 is the ownership (OWN) bit. The remaining six bits will read all zeros.

Each semaphore register is able to arbitrate simultaneous accesses to it. The semaphore register bits provide a mechanism for controlling accesses to the shared RAM but there are no hardware controls of the dual-port RAM by the semaphore registers.

Table 3 is the truth table for when a semaphore register is accessed by one of the processors. When a semaphore register is written, the actual data written is disregarded but the SEM bit is set to zero. When the register is read, the resulting SEM bit is one (for the next read). The data obtained from the read is interpreted as: SEM bit equals zero — resource available, SEM bit equals one — resource not available.

TABLE 3 — ONE PROCESSOR SEMAPHORE BIT TRUTH TABLE

Original SEM Bit	R/$\overline{W}$	Data Read	Resulting SEM Bit
0	R	0*	1
1	R	1*	1
0	$\overline{W}$	—	0
1	$\overline{W}$	—	0

*0 = Resource Available
1 = Resource Not Available

Table 4 shows the truth table if both processors read or read and write the same semaphore register at the same time. The A processor always reads the actual SEM bit. The B processor reads the SEM bit except during the simultaneous read of a clear SEM bit. This insures that during a simultaneous read, only the A processor reads a clear SEM bit and therefore has priority to the shared RAM.

TABLE 4 — SIMULTANEOUS ACCESS OF OF SEMAPHORE REGISTER TRUTH TABLE

Original	A Processor		B Processor		Resulting
SEM Bit	R/$\overline{W}$	Data Read	R/$\overline{W}$	Data Read	SEM Bit
0	R	0*	R	1*	1
1	R	1*	$\overline{W}$	—	0
1	$\overline{W}$	—	R	1*	0
1	R	1*	R	1*	1

*0 = Resource Available
1 = Resource Not Available

The ownership bit is a read-only bit that indicates which processor last set the SEM bit. The OWN bit is set to a one whenever the SEM bit is set from zero to one. The OWN bit as read by one processor is the complement of the bit read by the other processor.

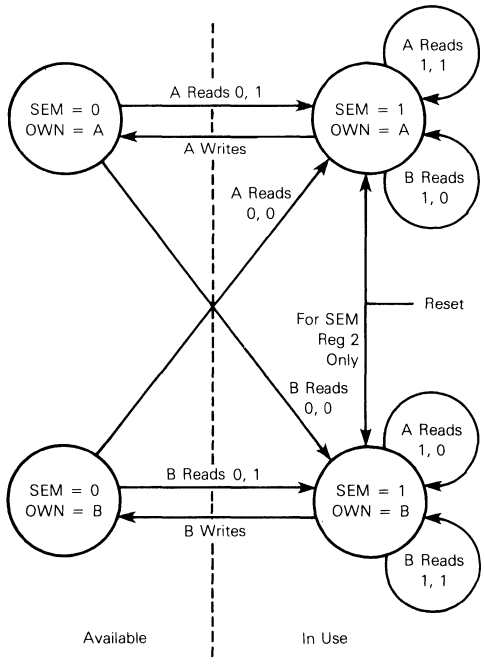
The reset state of the semaphore registers is defined in Table 5. The A processor owns all of the semaphore registers except the second semaphore register which is owned by the B processor.

TABLE 5 — RESET STATE OF SEMAPHORE REGISTERS

Semaphore Register Number	A Processor		B Processor	
	SEM Bit	OWN Bit	SEM Bit	OWN Bit
1	1	1	1	0
2	1	0	1	1
3	1	1	1	0
4	1	1	1	0
5	1	1	1	0
6	1	1	1	0

A state diagram for a semaphore register is shown in Figure 3.

FIGURE 3 — STATE DIAGRAM FOR SEMAPHORE REGISTER



NOTES:
1. Writes to a semaphore register are valid only if SEM = 1 and OWN = 1.
2. When A and B simultaneously read a semaphore register, the hardware handles it as a read by A followed by a read by B.

INTERRUPT REGISTERS

The dual-port memory unit contains two addressable locations at F8 and F9 on both sides that control the interrupt ($\overline{IRQ}$) operation between the processors. Although there is only one hardware register for each side, for purposes of explanation the register accessed at location F8 is referred to

as the IRQX status register and the register accessed at location F9 is referred to as the IRQX control register (refer to Table 6). The registers each consisting of two bits have identical bit arrangements. Bit 6 is the enable bit and bit 7 is the flag bit. The other six bits are not used and always read as zero. When $\overline{\text{RESET}}$ is asserted, both bits are cleared to zero.

Table 7 summarizes the bits involved when reading or writing to the status or control registers at F8 or F9. The enable bits on either side (A or B) track the data that is written into the status register from that side. Writes to the control register do not alter data. The actual data written is disregarded but the action sets the flag bit in the other side's register and asserts an interrupt signal if enabled.

The following describes how the B side interrupt is asserted from the A side. The A side interrupt is controlled in a similar manner.

When the enable bit in the IRQb status register is set (bit 6 = 1), a write to IRQa control register sets the flag bit in the IRQb status register (bit 7 = 1) and causes an interrupt on the B side by setting the IRQb pin low. Reading the IRQb status register reads the state of the B side enable and flag bits. Reading the IRQb control register also reads the enable and flag bits but in addition, clears the B side flag bit (bit 7 = 0) and clears the B side interrupt by removing the low condition on the IRQb pin.

The enable bit in the IRQb status register (bit 6) is changed by writing the proper data to bit 6 of the IRQb status register. If the B side enable bit is zero, interrupts are prevented on the B side. However, a write to the IRQa control register still sets the B side flag bit.

INTERNAL REGISTER ADDRESSES

Table 8 shows the address of the RAM, $\overline{\text{IRQ}}$, and semaphore registers. The addresses to these registers are the same whether accessed from the A or B side. The address and data buses are multiplexed on the A side. The B side has separate address and data buses. The B side can be used on a multiplexed bus by connecting the corresponding address and data bit pins together (A0 to D0, A1 to D1, etc.) and using the B side address strobe input pin.

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TABLE 6 — IRQ REGISTERS

Location	Register Name	Bit 7	Bit 6	Bits 5 to 0
A Side F8	IRQa Status	Flag	Enable	Not Used
A Side F9	IRQa Control	Flag	Enable	Not Used
B Side F8	IRQb Status	Flag	Enable	Not Used
B Side F9	IRQb Control	Flag	Enable	Not Used

TABLE 7 — INTERRUPT OPERATION

Operation	Action Taken
A Reads IRQa Status at F8	Read EA and FA
A Writes IRQa Status at F8	Writes to EA
A Reads IRQa Control at F9	Read EA and FA; Clear FA
A Writes IRQa Control at F9	Set FB; Assert IRQB if Enabled
B Reads IRQb Status at F8	Read EB and FB
B Writes IRQb Status at F8	Writes to EB
B Reads IRb Control at F9	Read EB and FB; Clear FB
B Writes IRQb Control at F9	Set FA; Assert IRQA if Enabled

F8 and F9 are Address Locations
EA and FA are A Side Enable and Flag Bits
EB and FB are B Side Enable and Flag Bits

TABLE 8 — REGISTER LOCATIONS

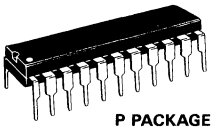
RS	Address	Register Name
0	00-FF	Dual Ported RAM
1	00-07	IRQ and Semaphore
1	08-0F	IRQ and Semaphore
1	10-17	IRQ and Semaphore
1	18-1F	IRQ and Semaphore
1	•	IRQ and Semaphore
	•	
	•	
1	E0-E7	IRQ and Semaphore
1	E8-EF	IRQ and Semaphore
1	F0-F7	IRQ and Semaphore
1	F8-FF	IRQ and Semaphore

Where:
X is 0 through F of the upper four bits of the address (note that only the lower three bits of the address are decoded):
X0 and X8 IRQa or IRQb Status
X1 and X9 IRQa or IRQb Control
X2 and XA Semaphore 1
X3 and XB Semaphore 2
X4 and XC Semaphore 3
X5 and XD Semaphore 4
X6 and XE Semaphore 5
X7 and XF Semaphore 6

MCM4180

Product Preview

4K x 4 Bit Cache Address Tag Comparator



P PACKAGE
PLASTIC
CASE 736A

The MCM4180 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's second generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates a 4K x 4 SRAM core with an on-board comparator for efficient implementation of a cache memory.

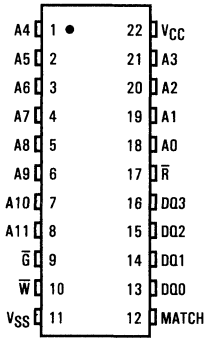
The device has a $\overline{R}$ pin for flash clear of the RAM, useful for system initialization.

The MCM4180 compares RAM contents with current input data. The result is either an active high match level for a cache hit, or an active low level for a cache miss.

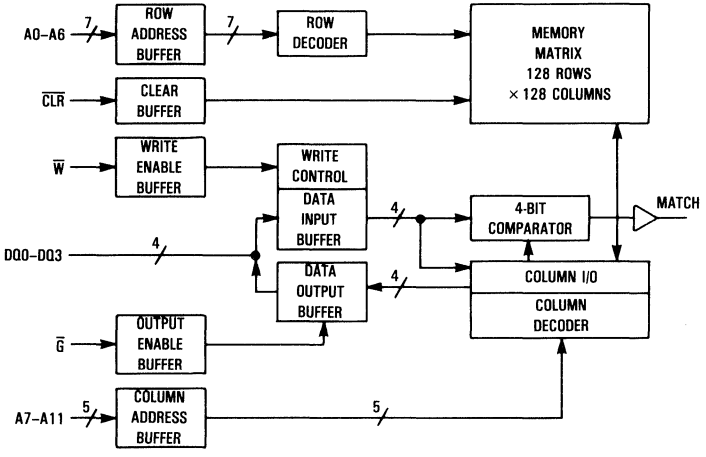
The MCM4180 will be available in a 22 lead plastic DIP.

- Single 5 V ±10% Power Supply
- Fast Address to Match Time: 22/25/30 ns max
- Fast Data to Match Time: 10/12/15 ns max
- Fast Read of Tag RAM Contents: 25/30/35 ns max
- Flash Clear of the Tag RAM ($\overline{R}$ Pin)
- Pin and Function Compatible with the MK41H80

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
$\overline{R}$	Flash Clear Input
MATCH	Match (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

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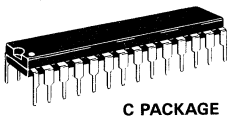
This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MCM6292

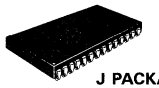
Product Preview

16K x 4 Bit Synchronous Static RAM

with Transparent Outputs



C PACKAGE
CERAMIC
CASE 733B



J PACKAGE
PLASTIC
CASE 810

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The MCM6292 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output latching onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A13), data (D0-D3), write ($\overline{W}$), and chip select ($\overline{S}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

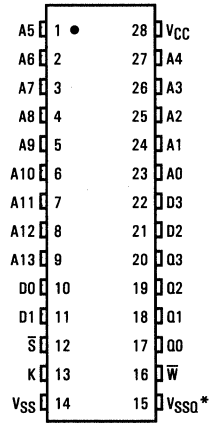
The MC6292 provides transparent output operation when K is low for access of RAM data within the same cycle (output data is latched when K is high).

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM6292 will be available in a 300-mil, 28-pin ceramic DIP as well as a 400-mil, 28-pin plastic SOJ package.

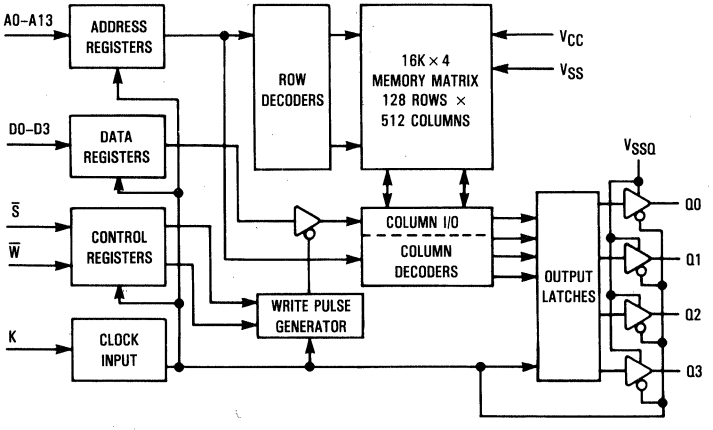
- Single 5 V ±10% Power Supply
- Fast Access and Cycle Times: 25/30/35 ns Max
- Address, Data Input, $\overline{S}$, and $\overline{W}$ Registers On-Chip
- Transparent Output Latch for Access Within the Same Cycle
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

PIN ASSIGNMENT



*For minimum cycle/low noise applications, V_{SSQ} should be isolated from V_{SS}.

BLOCK DIAGRAM



PIN NAMES	
A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

TRUTH TABLE

$\overline{S}$	$\overline{W}$	Operation	Q0-Q3
L	L	Write	High Z
L	H	Read	D_{out}
H	X	Not Selected	High Z

NOTE: The values of $\overline{S}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A = 25°C$)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature Plastic Ceramic	T_{stg}	−55 to +125 −65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0$ V ±10%, $T_A = 0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{S} = V_{IH}$, $V_{out} = 0$ to V_{CC})	$I_{lkg(O)}$	–	±1.0	μA
DC Supply Current ($\overline{S} = V_{IL}$, $V_{in} = V_{IL}$ or V_{IH}, $I_{out} = 0$)	I_{CC}	–	20	mA
AC Supply Current ($\overline{S} = V_{IL}$, $I_{out} = 0$ mA)	I_{CCA}	–	120	mA
Output Low Voltage ($I_{OL} = 12.0$ mA)	V_{OL}	–	0.4	V
Output High Voltage ($I_{OH} = -10.0$ mA)	V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A = 25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter		Symbol	MCM6292-25		MCM6292-30		MCM6292-35		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time		t_{KHKH}	25	–	30	–	35	–	ns	2
Clock Access Time		t_{KHQV}	–	25	–	30	–	35	ns	4, 6
Data Valid from Clock Low		t_{KLQV}	–	10	–	13	–	15	ns	5, 6
Output Hold from Clock Low		t_{KLQX}	0	–	0	–	0	–	ns	3, 6
Clock Low to Q High Z ($\overline{S}=V_{IH}$)		t_{KLQZ}	–	10	–	13	–	15	ns	3, 6
Clock Low Pulse Width		t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width		t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for:	$\overline{S}$	t_{SVKH}	5	–	5	–	5	–	ns	
	A	t_{AVKH}								
	$\overline{W}$	t_{WHKH}								
Hold Times for:	$\overline{S}$	t_{KHSX}	3	–	3	–	3	–	ns	
	A	t_{KHAX}								
	$\overline{W}$	t_{KHWX}								

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{S}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested.
4. For Read Cycle 1 timing, clock high pulse width $<(t_{KHQV}-t_{KLQV})$.
5. For Read Cycle 2 timing, clock high pulse width $\geq(t_{KHQV}-t_{KLQV})$.
6. K must be at a low level for outputs to transition.

AC TEST LOADS

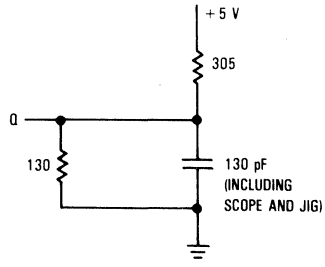


Figure 1A

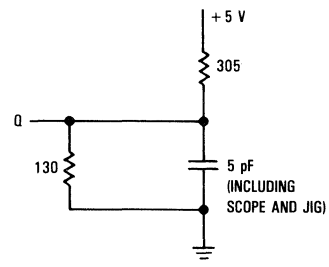
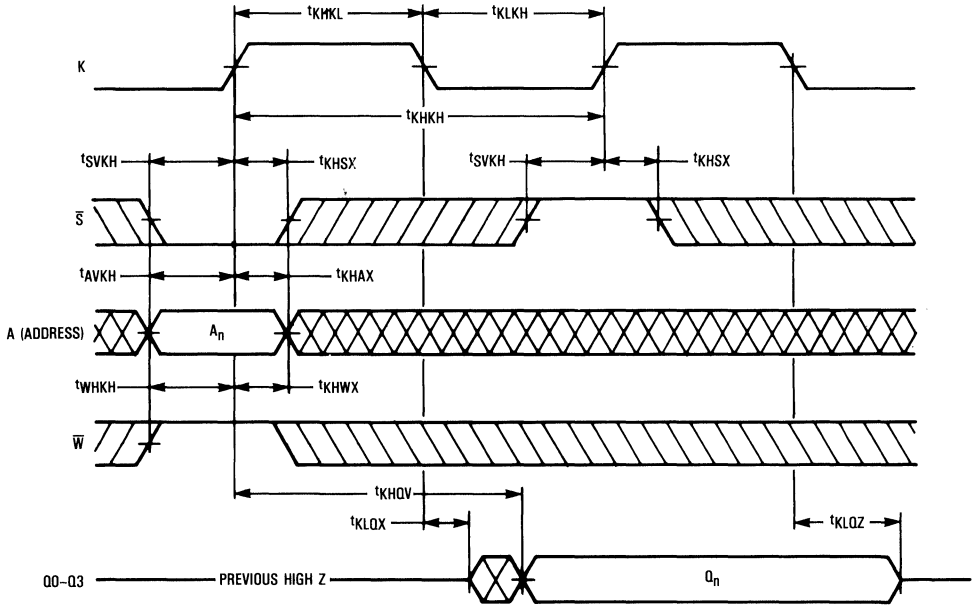
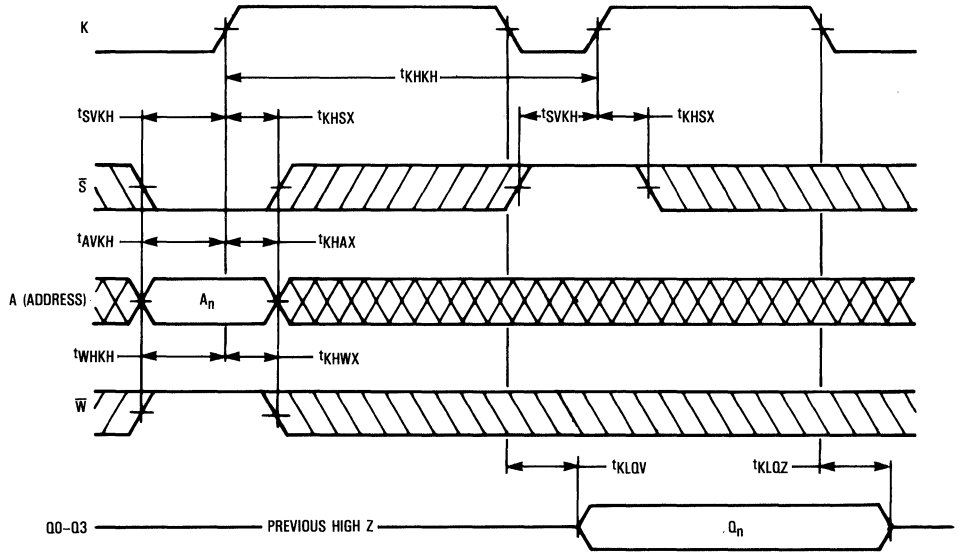


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 2)



NOTES:
1. For Read Cycle 1 timing, clock high pulse width $<(t_{KHQV} - t_{KLQV})$.
2. For Read Cycle 2 timing, clock high pulse width $\geq(t_{KHQV} - t_{KLQV})$.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6292-25		MCM6292-30		MCM6292-35		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	25	—	30	—	35	—	ns	2
Clock Low to Output High Z		t_{KLQZ}	—	10	—	13	—	15	ns	3
Setup Times for:	$\overline{S}$	t_{SVKH}	5	—	5	—	5	—	ns	
	A	t_{AVKH}								
	$\overline{W}$	t_{WLKH}								
	D	t_{DVKH}								
Hold Times for:	$\overline{S}$	t_{KHSX}	3	—	3	—	3	—	ns	
	A	t_{KHAX}								
	$\overline{W}$	t_{KHWX}								
	D	t_{KHDX}								

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{S}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. K must be at a low level for outputs to transition.

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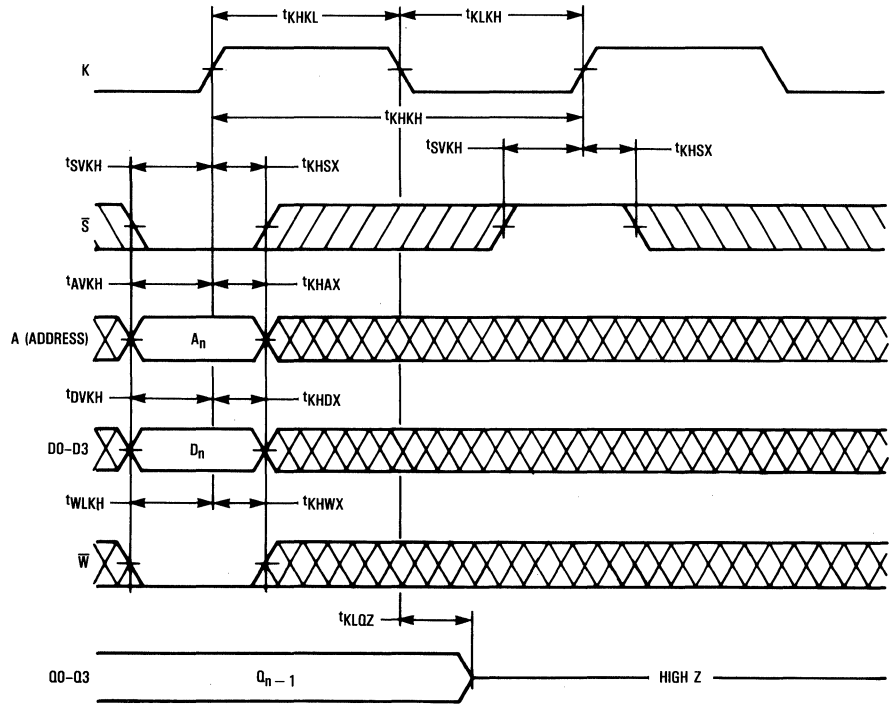


APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Latches on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output latches, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6292 offers transparent output operation, which allows output data access within the same t_{KHKH} cycle. This feature lends itself well to applications requiring RAM data to be set up on the system bus prior to the next rising clock edge. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next falling clock edge. When the clock (K) signal is low, the output is allowed to transition relative to the most recent rising clock (K) edge.

Figure 2 shows a typical system configuration using four MCM6292 chips. The system addresses are tied to the MCM6292s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6292. The clock (K) signal is a logical derivation of the system clock.

Figure 3 shows typical bus timing for the configuration of Figure 2. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

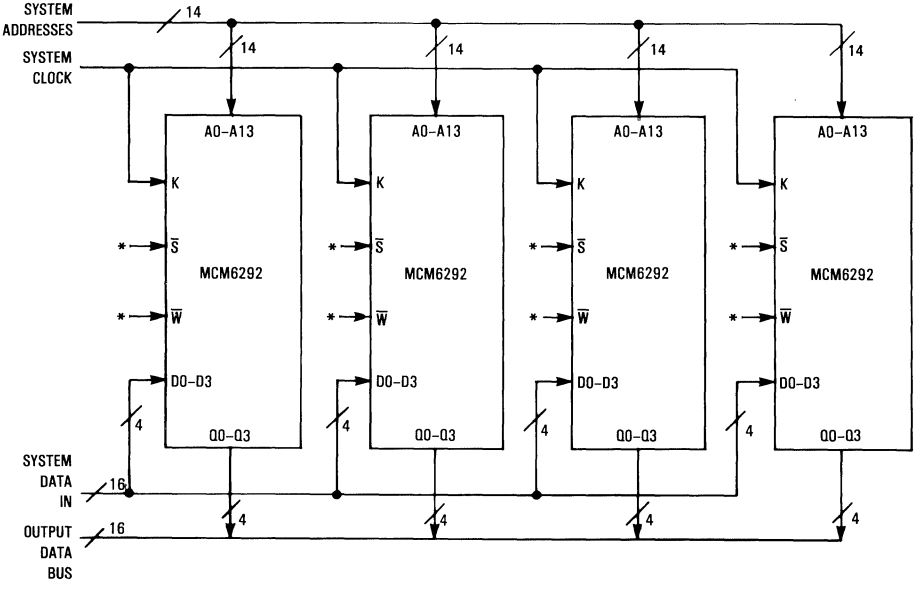
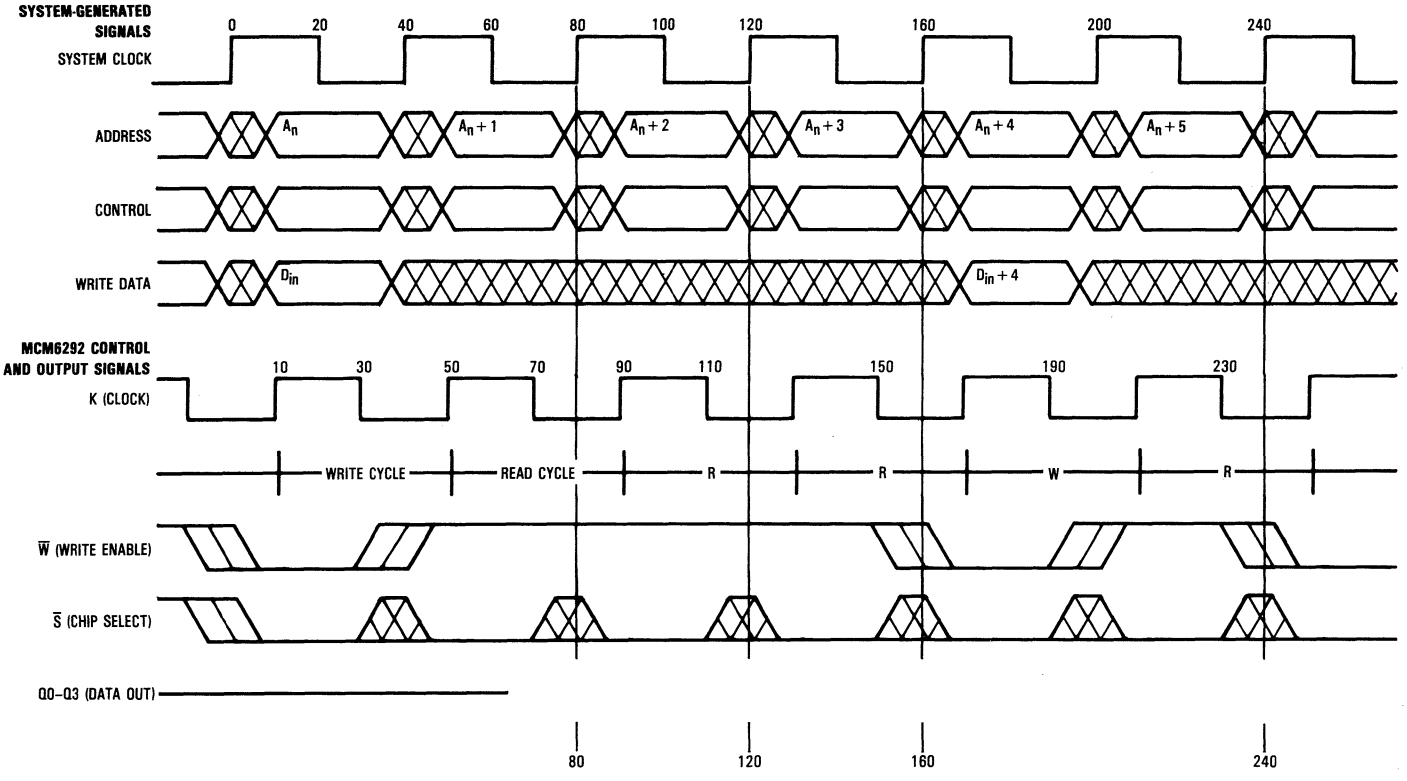


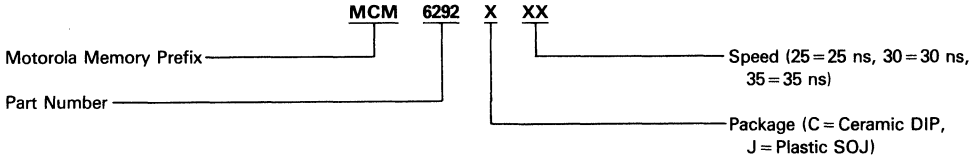
Figure 2. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 3. Nonpipeline System Timing

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—	MCM6292C25	MCM6292J25
	MCM6292C30	MCM6292J30
	MCM6292C35	MCM6292J35

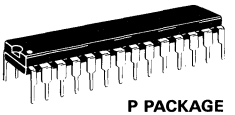
5

MCM6293

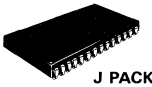
Product Preview

16K x 4 Bit Synchronous Static RAM

with Output Registers



P PACKAGE
300 MIL PLASTIC
CASE TBD



J PACKAGE
PLASTIC
CASE 810

5

The MCM6293 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications.

Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A13), data (D0-D3), write ($\overline{W}$), and chip select ($\overline{S}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

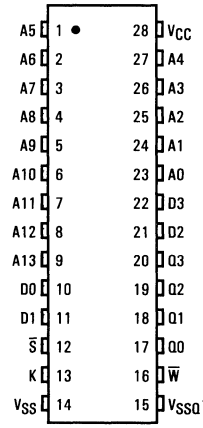
The MC6293 provides output register operation. At the rising edge of K, the RAM data from the previous K high cycle is presented. This function is well suited to fully pipelined applications.

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

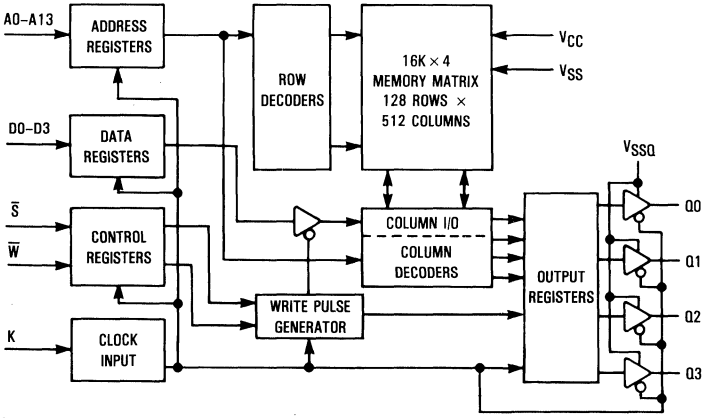
The MCM6293 will be available in a 300-mil, 28-pin plastic DIP as well as a 400-mil, 28-pin plastic SOJ package.

- Single 5 V ±10% Power Supply
- Fast Cycle Times: 25/30/35 ns Max
- Fast Clock (K) Access Times: 10/13/15 ns Max
- Address, Data Input, $\overline{S}$, and $\overline{W}$ Registers On-Chip
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

PIN ASSIGNMENT



*For minimum cycle/low noise applications, V_{SSQ} should be isolated from V_{SS}.



PIN NAMES

A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

TRUTH TABLE

$\overline{S}$	$\overline{W}$	Operation	Q0-Q3
L	L	Write	High Z
L	H	Read	D_{out}
H	X	Not Selected	High Z

NOTE: The values of $\overline{S}$ and $\overline{W}$ are valid inputs for the setup and hold times relative to the K rising edge.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A = 25°C$)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature Plastic Ceramic	T_{stg}	−55 to +125 −65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0$ V ±10%, $T_A = 0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{S} = V_{IH}$, $V_{out} = 0$ to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{S} = V_{IL}$, $I_{out} = 0$ mA, Cycle Time = t_{KHKH} min)	I_{CCA}	—	120	mA
Output Low Voltage ($I_{OL} = 12.0$ mA)	V_{OL}	—	0.4	V
Output High Voltage ($I_{OH} = -10.0$ mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A = 25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM6293-25		MCM6293-30		MCM6293-35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	25	—	30	—	35	—	ns	2
Clock Access Time	t_{KHQV}	—	10	—	13	—	15	ns	3
Output Active from Clock High	t_{KHQX}	0	—	0	—	0	—	ns	4
Clock High to Q High Z ($\overline{S}$ = V_{IH})	t_{KHQZ}	—	10	—	13	—	15	ns	4
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	5	—	ns	
Setup Times for: $\overline{S}$	t_{SVKH}	5	—	5	—	5	—	ns	
A	t_{AVKH}								
$\overline{W}$	t_{WHKH}								
Hold Times for: $\overline{S}$	t_{KHSX}	3	—	3	—	3	—	ns	
A	t_{KHAX}								
$\overline{W}$	t_{KHWX}								

NOTES:
1. A read is defined by $\overline{W}$ high and $\overline{S}$ low for the setup and hold times.
2. All read cycle timing is referenced from K.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.

AC TEST LOADS

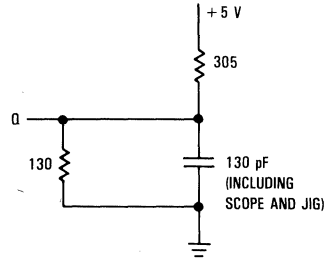


Figure 1A

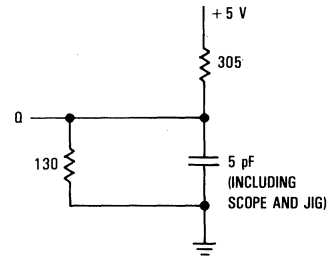
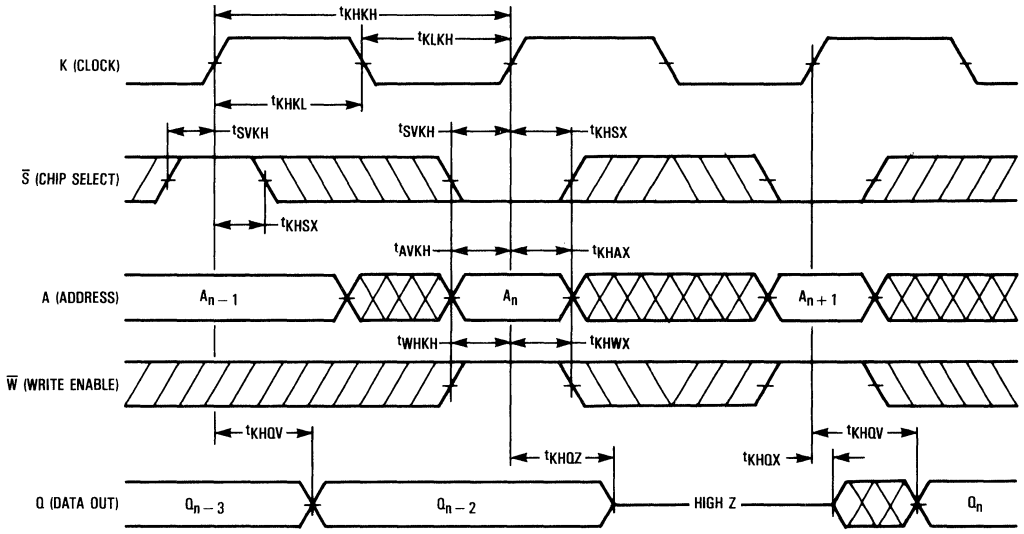
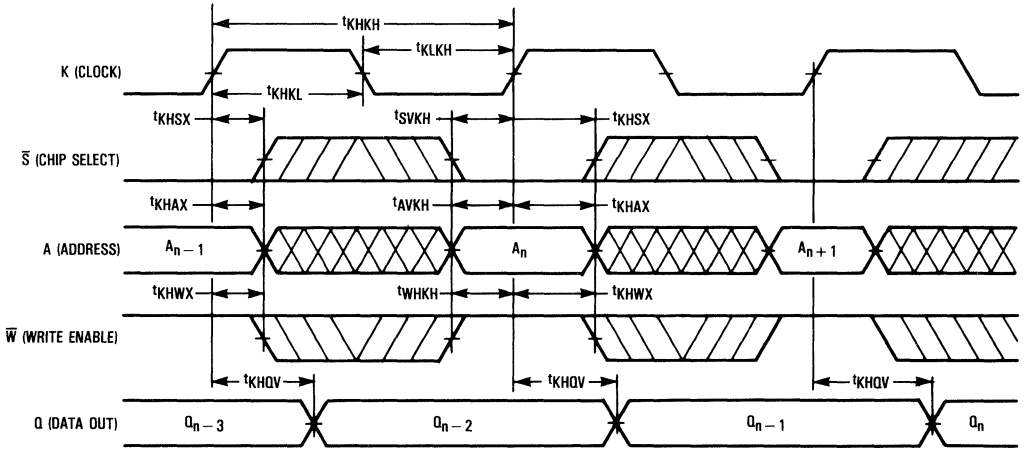


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles where $\overline{W} = V_{IH}$ and $\overline{S} = V_{IL}$ for those cycles.

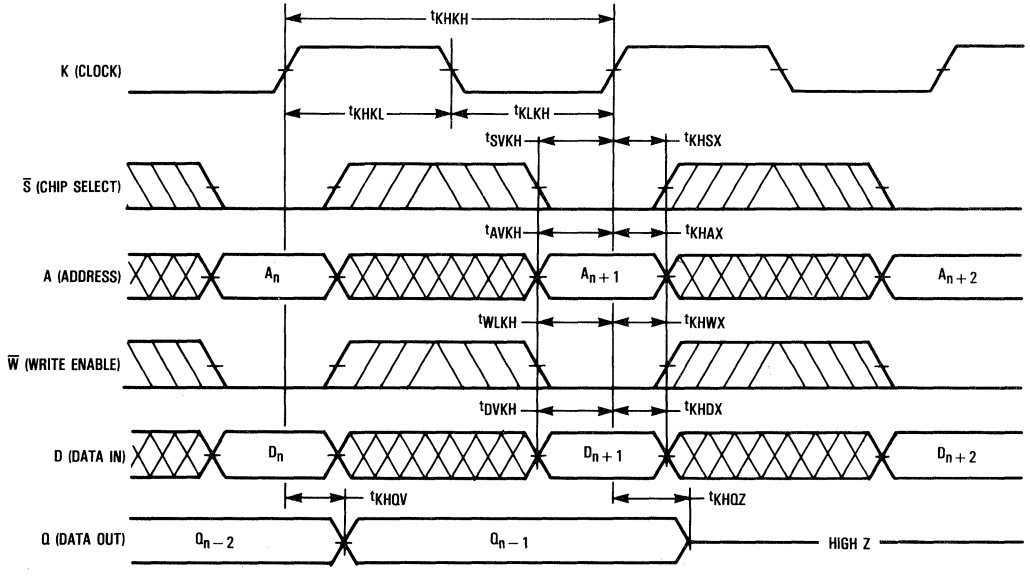
WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6293-25		MCM6293-30		MCM6293-35		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	25	—	30	—	35	—	ns	2
Clock High to Output High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	—	10	—	13	—	15	ns	3
Setup Times for:	$\overline{S}$	t_{SVKH}	5	—	5	—	5	—	ns	
	A	t_{AVKH}								
	$\overline{W}$	t_{WLKH}								
	D	t_{DVKH}								
Hold Times for:	$\overline{S}$	t_{KHSX}	3	—	3	—	3	—	ns	
	A	t_{KHAX}								
	$\overline{W}$	t_{KHWX}								
	D	t_{KHDX}								

NOTES:
1. A write is performed when $\overline{W}$ and $\overline{S}$ are both low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.

5

WRITE CYCLE



APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Registers on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output registers, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6293 offers registered output operation. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next rising clock edge.

Figure 2 shows a typical system configuration using four MCM6293 chips. The system addresses are tied to the MCM6293s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6293. The clock (K) signal is a logical derivation of the system clock.

Figure 3 shows typical bus timing for the configuration of Figure 2. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

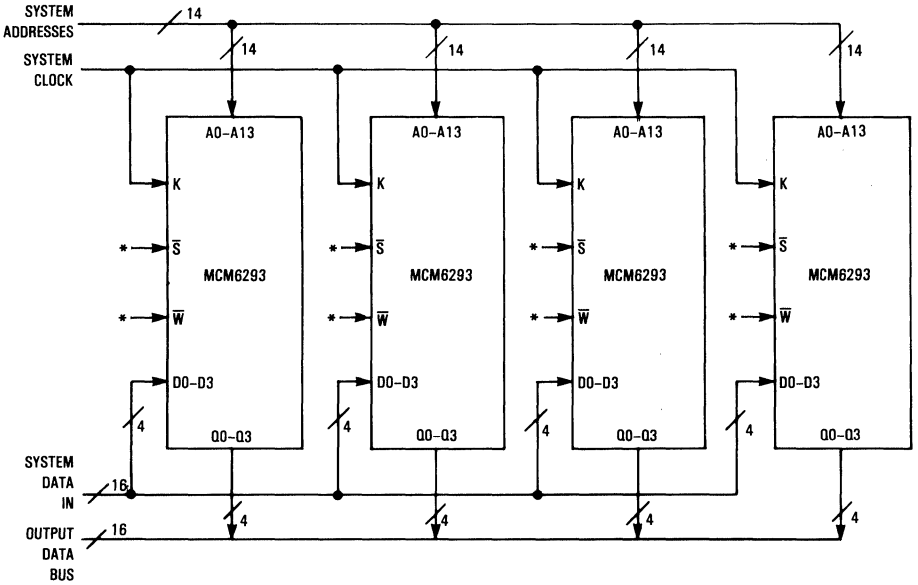
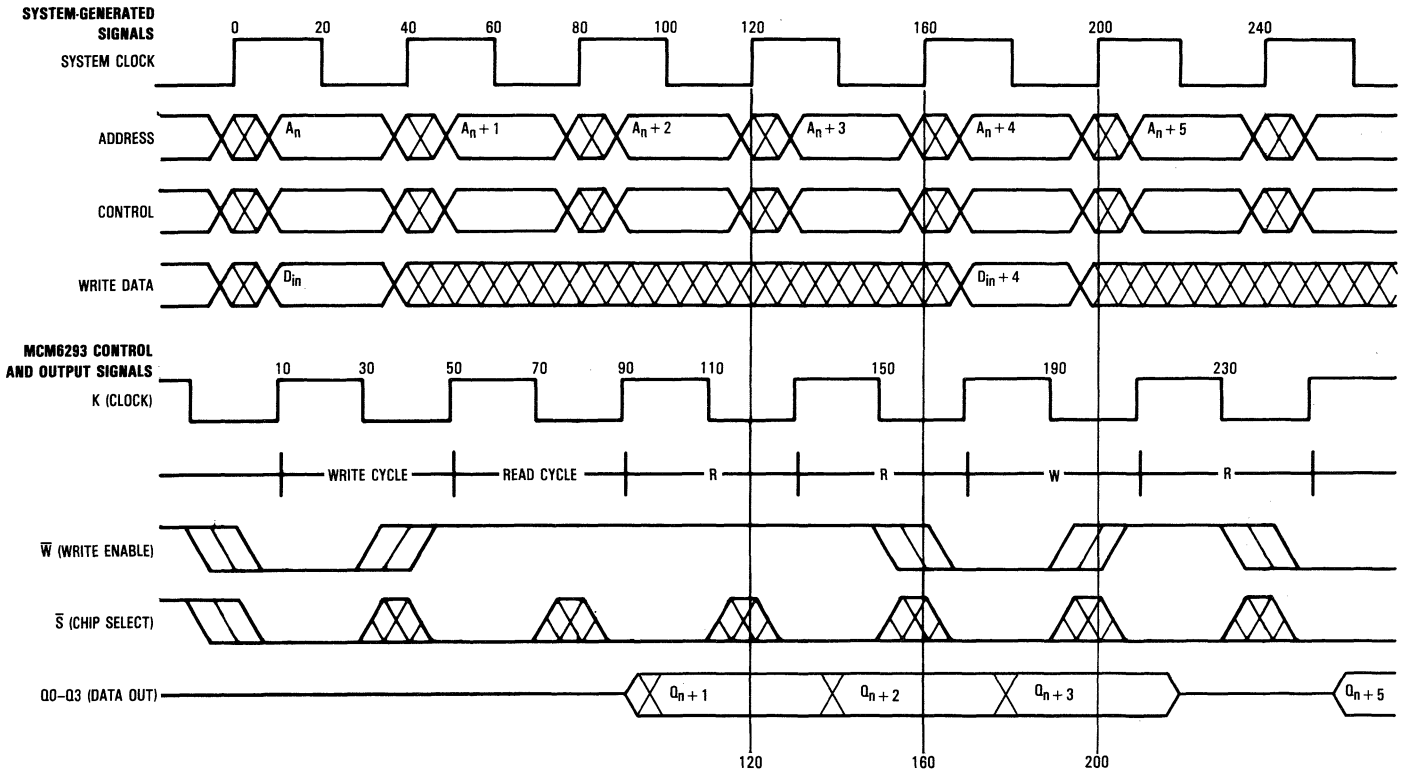


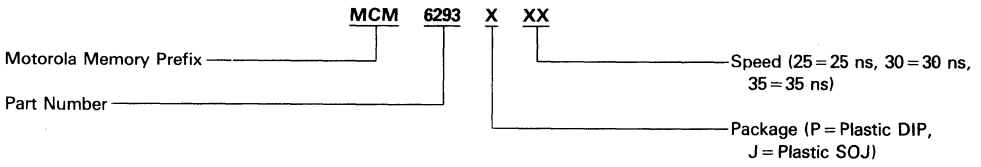
Figure 2. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 3. Pipeline System Timing

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—MCM6293P25 MCM6293J25
MCM6293P30 MCM6293J30
MCM6293P35 MCM6293J35

5

MCM6294

Product Preview

16K x 4 Bit Synchronous Static RAM

with Output Registers and Output Enable

P PACKAGE
300 MIL PLASTIC
CASE TBD

J PACKAGE
PLASTIC
CASE 810

5

The MCM6294 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output registers onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications. Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A13), data (D0-D3), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

The MC6294 provides output register operation. At the rising edge of K, the RAM data from the previous K high cycle is presented. This function is well suited to fully pipelined applications.

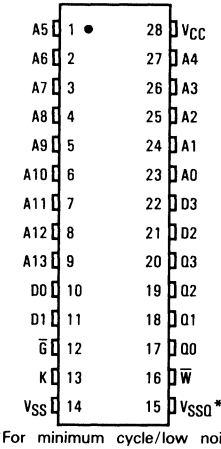
The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM6294 will be available in a 300-mil, 28-pin plastic DIP as well as a 400-mil, 28-pin plastic SOJ package.

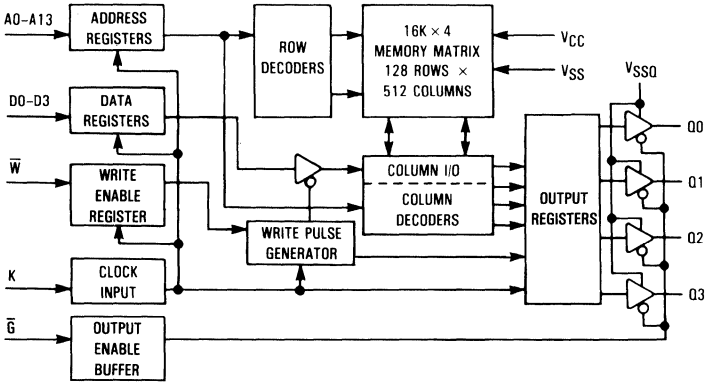
- Single 5 V ±10% Power Supply
- Fast Cycle Times: 25/30/35 ns Max
- Fast Clock (K) Access Times: 10/13/15 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Output Enable for Asynchronous Bus Control
- Output Registers for Fully Pipelined Applications
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

PIN ASSIGNMENT



*For minimum cycle/low noise applications, V_{SSQ} should be isolated from V_{SS}.

BLOCK DIAGRAM



PIN NAMES

A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

TRUTH TABLE

$\overline{W}$	Operation	Q0-Q3
L	Write	High Z
H	Read	D_{out}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A = 25°C$)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature Plastic Ceramic	T_{stg}	−55 to +125 −65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0$ V ±10%, $T_A = 0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	—	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	—	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	—	±1.0	μA
Output Leakage Current ($\overline{S} = V_{IH}$, $V_{out} = 0$ to V_{CC})	$I_{lkg(O)}$	—	±1.0	μA
AC Supply Current ($\overline{G} = V_{IL}$, $I_{out} = 0$ mA, Cycle Time = t_{KHKH} min)	I_{CCA}	—	120	mA
Output Low Voltage ($I_{OL} = 12.0$ mA)	V_{OL}	—	0.4	V
Output High Voltage ($I_{OH} = -10.0$ mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A = 25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM6294-25		MCM6294-30		MCM6294-35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	25	–	30	–	35	–	ns	2
Clock Access Time	t_{KHQV}	–	10	–	13	–	15	ns	3
Output Active from Clock High	t_{KHQX}	0	–	0	–	0	–	ns	4
Clock Low Pulse Width	t_{KLKH}	5	–	5	–	5	–	ns	
Clock High Pulse Width	t_{KHKL}	5	–	5	–	5	–	ns	
Setup Times for: A	t_{AVKH}	5	–	5	–	5	–	ns	
Setup Times for: $\overline{W}$	t_{WHKH}								
Hold Times for: A	t_{KHAX}	3	–	3	–	3	–	ns	
Hold Times for: $\overline{W}$	t_{KHWX}								
$\overline{G}$ High to Q High Z	t_{GHQZ}	–	10	–	13	–	15	ns	4, 5
$\overline{G}$ Low to Q Active	t_{GLQX}	0	–	0	–	0	–	ns	4, 5
$\overline{G}$ Low to Q Valid	t_{GLQV}	–	10	–	13	–	15	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K or from $\overline{G}$.
3. Valid data from K high will be the data stored at the address of the last valid read cycle.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested.
5. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min for a given device.

5

AC TEST LOADS

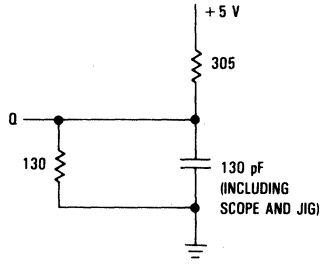


Figure 1A

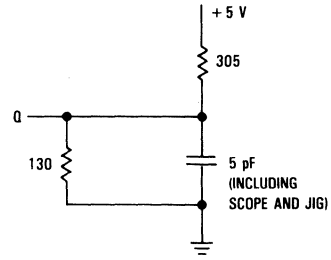
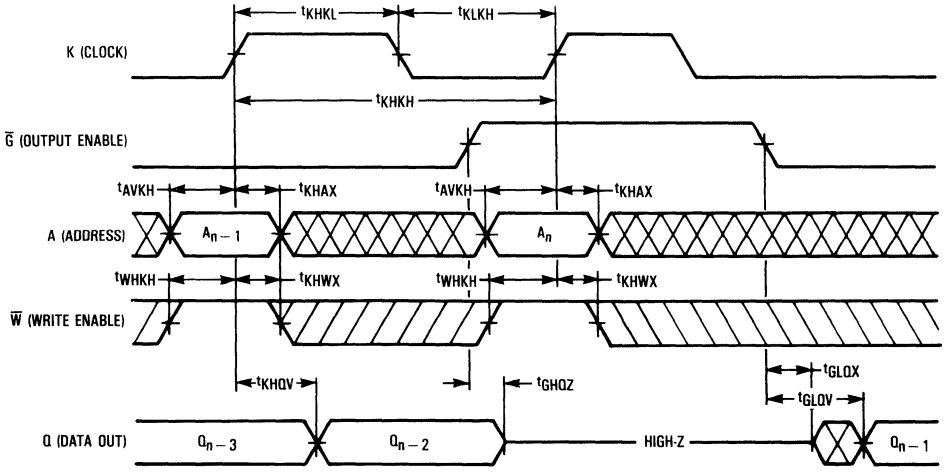
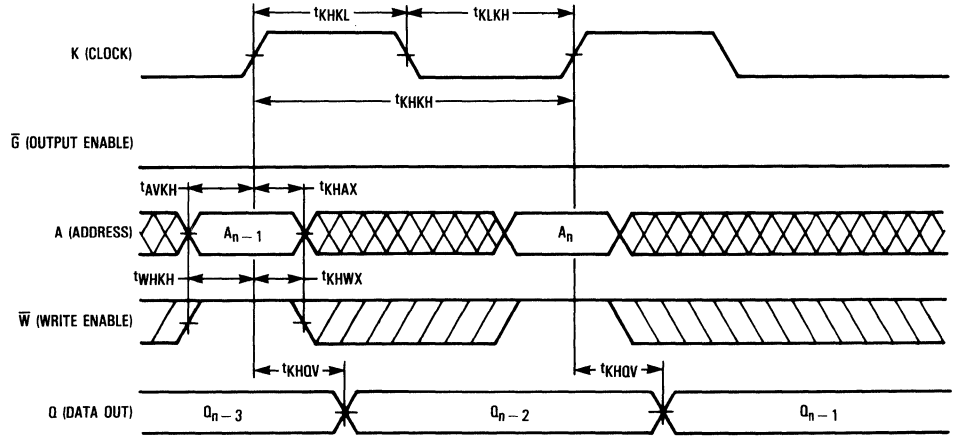


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 1)



NOTE:
1. The outputs Q_{n-3} and Q_{n-2} are derived from two previous read cycles, where $\overline{W} = V_{IH}$ for those cycles.

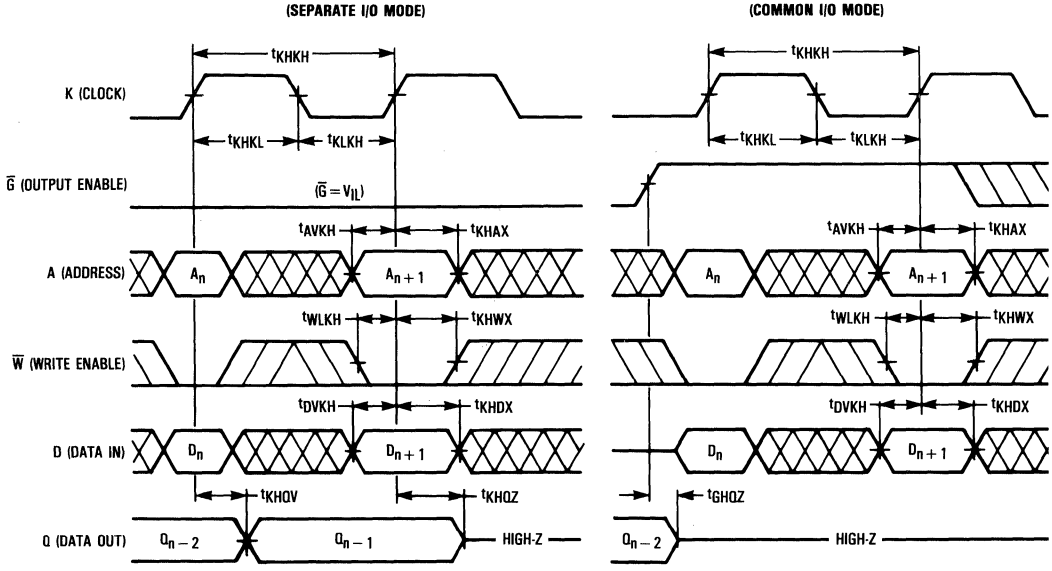
WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6294-25		MCM6294-30		MCM6294-35		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	25	–	30	–	35	–	ns	2
Clock High to Output High Z ($\overline{W}=V_{IL}$)		t_{KHQZ}	–	10	–	13	–	15	ns	3
$\overline{G}$ High to Q High Z		t_{GHQZ}	–	10	–	13	–	15	ns	4
Setup Times for:	A	t_{AVKH}	5	–	5	–	5	–	ns	
	$\overline{W}$	t_{WLKH}								
	D	t_{DVKH}								
Hold Times for:	A	t_{KHAX}	3	–	3	–	3	–	ns	
	$\overline{W}$	t_{KHWX}								
	D	t_{KHDX}								

NOTES:
1. A write is performed when $\overline{W}$ is low for the specified setup and hold times.
2. All write cycle timing is referenced from K or from $\overline{G}$.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. At any given voltage and temperature, t_{KHQZ} max is less than t_{KHQX} min for a given device.
4. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.

5

WRITE CYCLE 1



APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Registers on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output registers, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6294 offers registered output operation. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next rising clock edge.

Figure 2 shows a typical system configuration using four MCM6294 chips. The system addresses are tied to the MCM6294s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6294. The clock (K) signal is a logical derivation of the system clock.

Figure 3 shows typical bus timing for the configuration of Figure 2. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

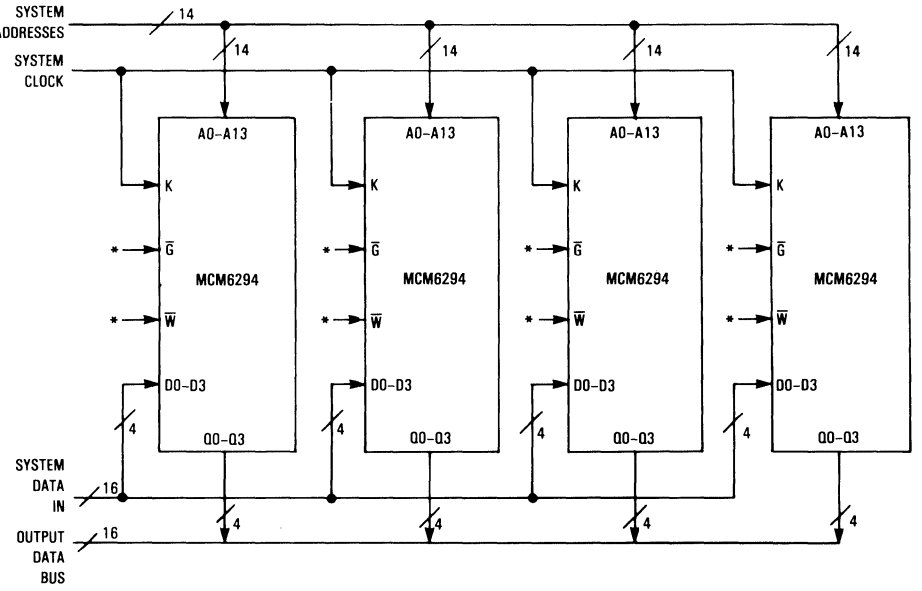
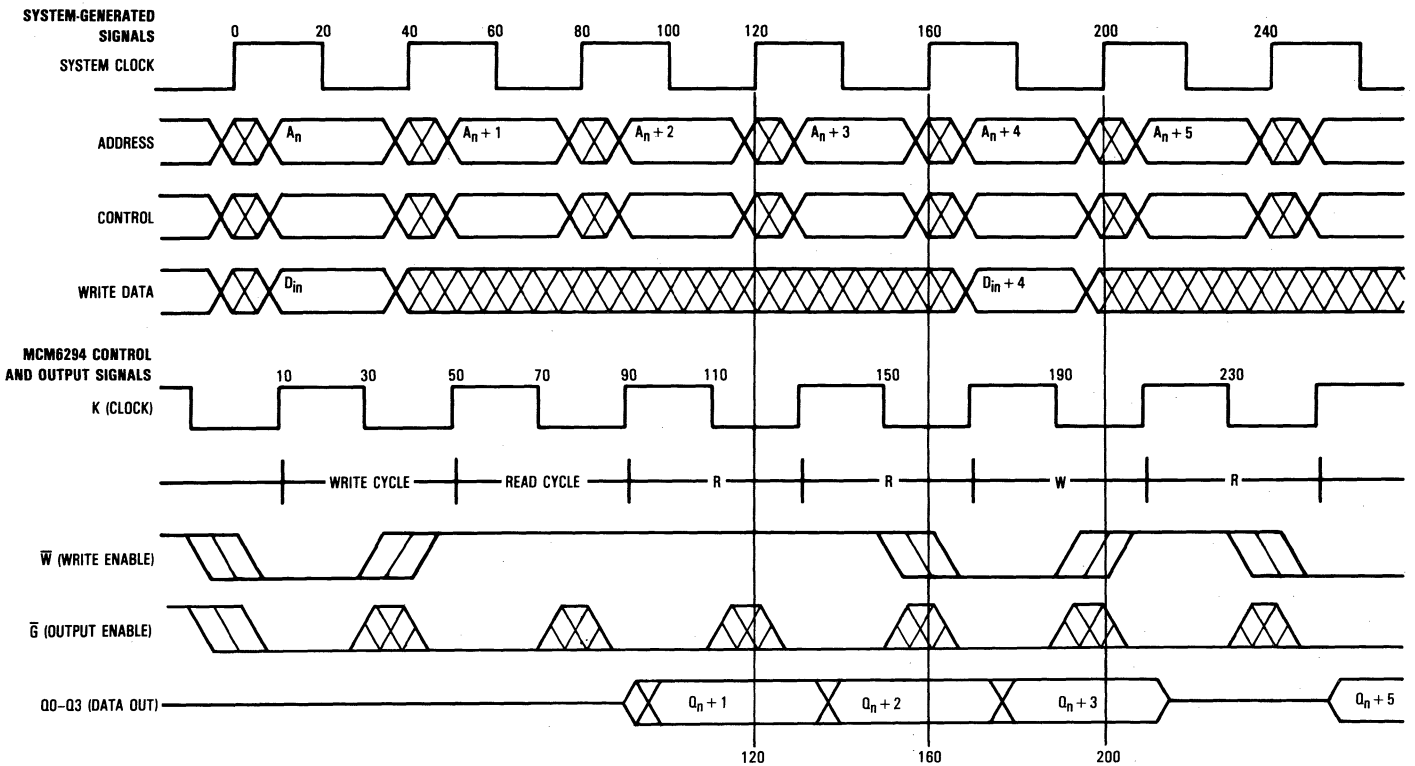


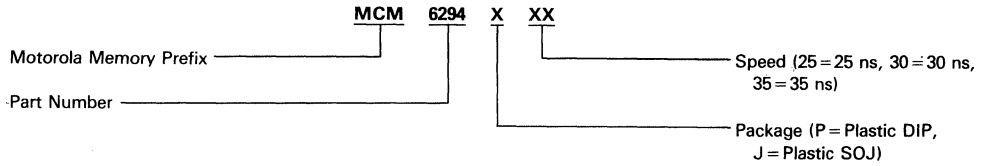
Figure 2. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 3. Pipeline System Timing

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM6294P25 MCM6294J25
MCM6294P30 MCM6294J30
MCM6294P35 MCM6294J35

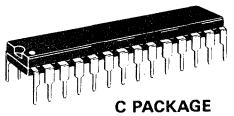
5

MCM6295

Product Preview

16K x 4 Bit Synchronous Static RAM

with Transparent Outputs and Output Enable



C PACKAGE
CERAMIC
CASE 733B

J PACKAGE
PLASTIC
CASE 810

The MCM6295 is a 65,536 bit synchronous static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates input registers, high speed SRAM, and high-drive capability output latching onto a single monolithic circuit for reduced parts count implementation of cache data RAM and writeable control store applications. Synchronous design allows precise cycle control with the use of an external clock (K), while CMOS circuitry reduces the overall power consumption of the integrated functions for greater reliability.

The address (A0-A13), data (D0-D3), and write ($\overline{W}$) inputs are all clock (K) controlled, positive-edge-triggered, noninverting registers.

The MC6295 provides transparent output operation when K is low for access of RAM data within the same cycle (output data is latched when K is high).

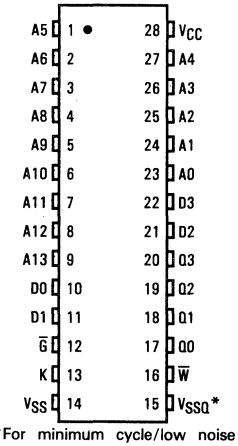
The output enable ($\overline{G}$) provides asynchronous bus control for common I/O or bank switch applications.

Write operations are internally self-timed and initiated by the rising edge of the K input. This feature eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The MCM6295 will be available in a 300-mil, 28-pin ceramic DIP as well as a 400-mil, 28-pin plastic SOJ package.

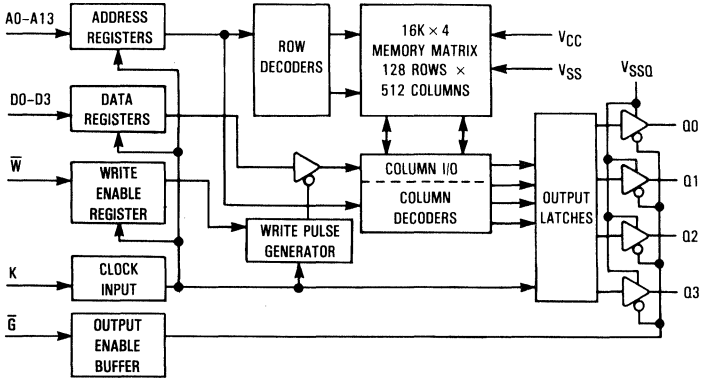
- Single 5 V ±10% Power Supply
- Fast Access and Cycle Times: 25/30/35 ns Max
- Address, Data Input, and $\overline{W}$ Registers On-Chip
- Transparent Output Latch for Access Within the Same Cycle
- Output Enable for Asynchronous Bus Control
- High Output Drive Capability
- Internally Self-Timed Write Pulse Generation
- Separate Data Input and Data Output Pins
- High Board Density SOJ Package Available
- Typical Applications: General-Purpose Buffer Storage, Writeable Control Store, Data Cache, or Cache Tag

PIN ASSIGNMENT



*For minimum cycle/low noise applications, V_{SSQ} should be isolated from V_{SS}.

BLOCK DIAGRAM



PIN NAMES

A0-A13	Address Inputs
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
D0-D3	Data Inputs
Q0-Q3	Data Outputs
K	Clock Input
V_{CC}	+5 V Power Supply
V_{SS}	Ground
V_{SSQ}	Output Buffer Ground

TRUTH TABLE

$\overline{W}$	Operation	Q0-Q3
L	Write	High Z
H	Read	D_{out}

NOTE: The value $\overline{W}$ is a valid input for the setup and hold times relative to the K rising edge.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS}/V_{SSQ} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation ($T_A = 25°C$)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−10 to +85	°C
Operating Temperature	T_A	0 to +70	°C
Storage Temperature Plastic Ceramic	T_{stg}	−55 to +125 −65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

5

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0$ V ±10%, $T_A = 0$ to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to $V_{SS} = V_{SSQ} = 0$ V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.0	–	V_{CC} +0.3	V
Input Low Voltage	V_{IL}	−0.5*	–	0.8	V

*V_{IL} (min) = −0.5 V dc; V_{IL} (min) = −3.0 V ac (pulse width ≤20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{lkg(I)}$	–	±1.0	μA
Output Leakage Current ($\overline{G} = V_{IH}$, $V_{out} = 0$ to V_{CC})	$I_{lkg(O)}$	–	±1.0	μA
DC Supply Current ($\overline{G} = V_{IL}$, $V_{in} = V_{IL}$ or V_{IH}, $I_{out} = 0$)	I_{CC}	–	20	mA
AC Supply Current ($\overline{G} = V_{IL}$, $I_{out} = 0$ mA)	I_{CCA}	–	120	mA
Output Low Voltage ($I_{OL} = 12.0$ mA)	V_{OL}	–	0.4	V
Output High Voltage ($I_{OH} = -10.0$ mA)	V_{OH}	2.4	–	V

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, $T_A = 25°C$, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	4	6	pF
Output Capacitance	C_{out}	7	10	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load. . . . . .See Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

Parameter	Symbol	MCM6295-25		MCM6295-30		MCM6295-35		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{KHKH}	25	—	30	—	35	—	ns	2
Clock Access Time	t_{KHQV}	—	25	—	30	—	35	ns	4, 6
Data Valid from Clock Low	t_{KLQV}	—	10	—	13	—	15	ns	5, 6
Output Hold from Clock Low	t_{KLQX}	0	—	0	—	0	—	ns	3, 6
Clock Low Pulse Width	t_{KLKH}	5	—	5	—	5	—	ns	
Clock High Pulse Width	t_{KHKL}	5	—	5	—	5	—	ns	
Setup Times for: A	t_{AVKH}	5	—	5	—	5	—	ns	
Setup Times for: $\overline{W}$	t_{WHKH}								
Hold Times for: A	t_{KHAX}	3	—	3	—	3	—	ns	
Hold Times for: $\overline{W}$	t_{KHWX}								
$\overline{G}$ High to Q High Z	t_{GHQZ}	—	10	—	13	—	15	ns	7
$\overline{G}$ Low to Q Active	t_{GLQX}	0	—	0	—	0	—	ns	7
$\overline{G}$ Low to Q Valid	t_{GLQV}	—	10	—	13	—	15	ns	

NOTES:
1. A read is defined by $\overline{W}$ high for the setup and hold times.
2. All read cycle timing is referenced from K or from $\overline{G}$.
3. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B. This parameter is sampled not 100% tested.
4. For Read Cycle 1 timing, clock high pulse width $< (t_{KHQV} - t_{KLQV})$.
5. For Read Cycle 2 timing, clock high pulse width $\geq (t_{KHQV} - t_{KLQV})$.
6. K must be at a low level for outputs to transition.
7. At any given voltage and temperature, t_{GHQZ} max is less than t_{GLQX} min, both for a given device and from device to device.

AC TEST LOADS

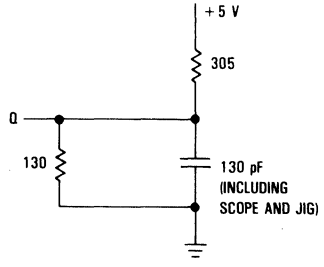


Figure 1A

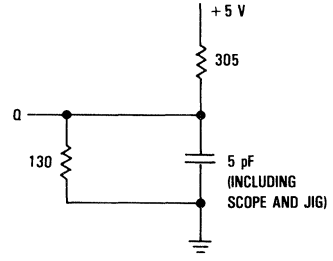
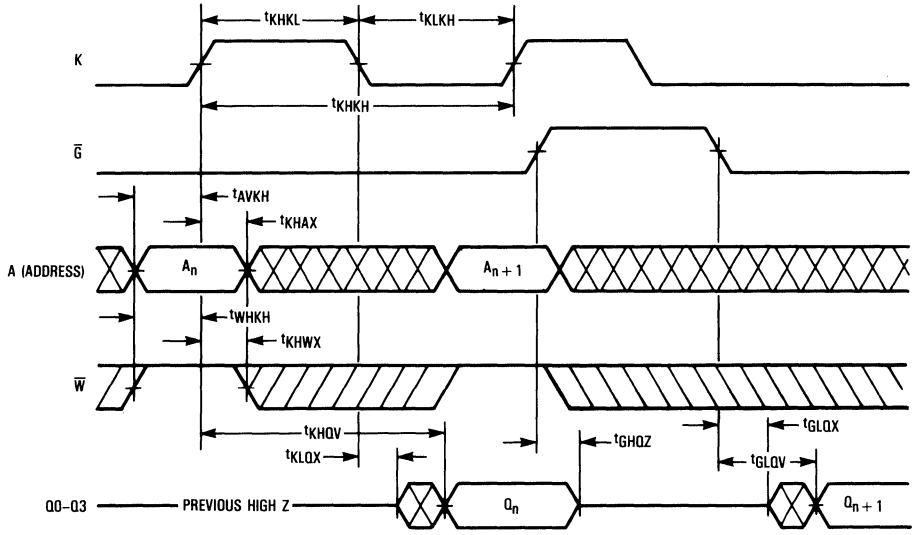
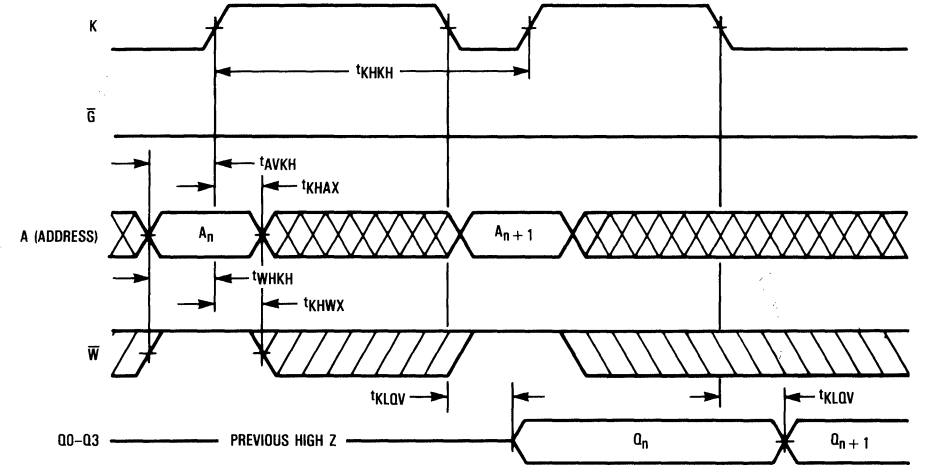


Figure 1B

READ CYCLE 1 (See Note 1)



READ CYCLE 2 (See Note 2)



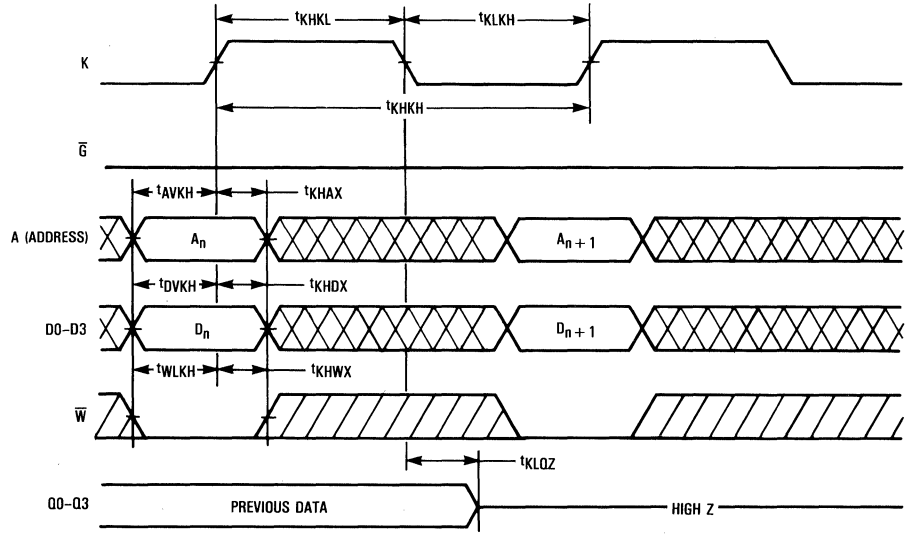
NOTES:
1. For Read Cycle 1 timing, clock high pulse width $< (t_{KHQV} - t_{KLQV})$.
2. For Read Cycle 2 timing, clock high pulse width $\geq (t_{KHQV} - t_{KLQV})$.

WRITE CYCLE ($\overline{W}$ Controlled, See Note 1)

Parameter		Symbol	MCM6295-25		MCM6295-30		MCM6295-35		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time		t_{KHKH}	25	–	30	–	35	–	ns	2
Clock Low to Output High Z ($\overline{W}=V_{IL}$)		t_{KLQZ}	–	10	–	13	–	15	ns	3
$\overline{G}$ High to Q High Z		t_{GHQZ}	–	10	–	13	–	15	ns	4
Setup Times for:	A	t_{AVKH}	5	–	5	–	5	–	ns	
	$\overline{W}$	t_{WLKH}								
	D	t_{DVKH}								
Hold Times for:	A	t_{KHAX}	3	–	3	–	3	–	ns	
	$\overline{W}$	t_{KHWX}								
	D	t_{KHDX}								

NOTES:
1. A write is performed when $\overline{W}$ is low for the specified setup and hold times.
2. All write cycle timing is referenced from K.
3. K must be at a low level for outputs to transition.
4. $\overline{G}$ becomes a don't care signal for successive writes after the first write cycle.

5



APPLICATIONS INFORMATION

The Motorola family of synchronous SRAMs is designed to provide a performance and parts count advantage in applications such as writeable control stores, memory mapping, and cache memory. The on-board input registers eliminate the need for external latch chips in systems where addresses and data are not on the bus long enough to satisfy standard SRAM setup and hold times. Latches on the output port provide extended hold times independent of address or other device input changes to better meet system access requirements. The clock (K) input controls the operation of the input registers and output latches, and provides a direct means of synchronizing the SRAM to a system clock.

The MCM6295 offers transparent output operation, which allows output data access within the same t_{KHKH} cycle. This feature lends itself well to applications requiring RAM data to be set up on the system bus prior to the next rising clock edge. On the rising edge of the clock (K) signal, the output data for the previous cycle is latched until the next falling clock edge. When the clock (K) signal is low, the output is allowed to transition relative to the most recent rising clock (K) edge.

Figure 2 shows a typical system configuration using four MCM6295 chips. The system addresses are tied to the MCM6295s in parallel, while system data is distributed among the four input data ports of 4 bits each. Output data is tied to a separate output data bus to exploit the separate I/O configuration of the MCM6295. The clock (K) signal is a logical derivation of the system clock.

Figure 3 shows typical bus timing for the configuration of Figure 2. The system bus supplies address, data, and control signals, while accepting data from the memory on rising clock edges. In some applications, the clock (K) signal may need to be a delayed system clock to allow adequate address and data setup times.

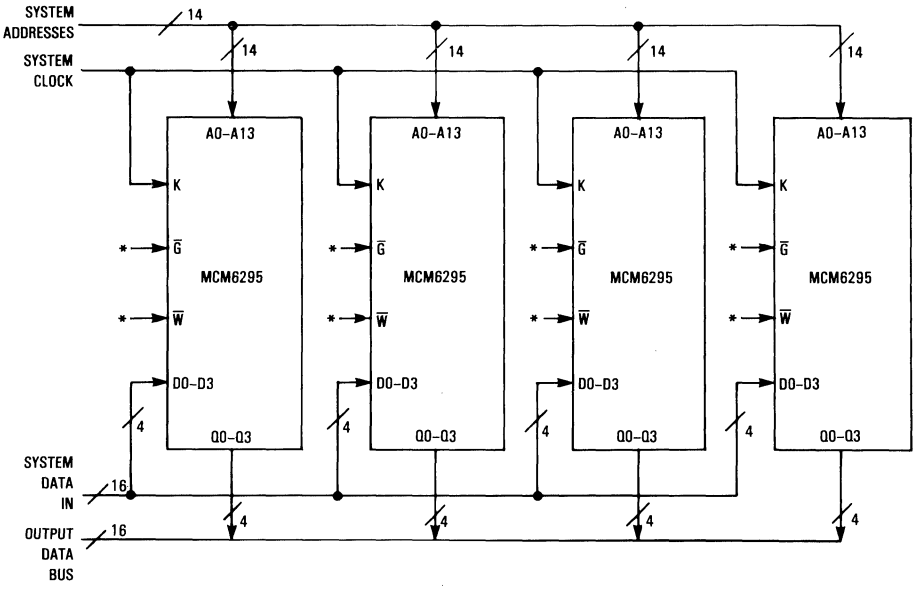
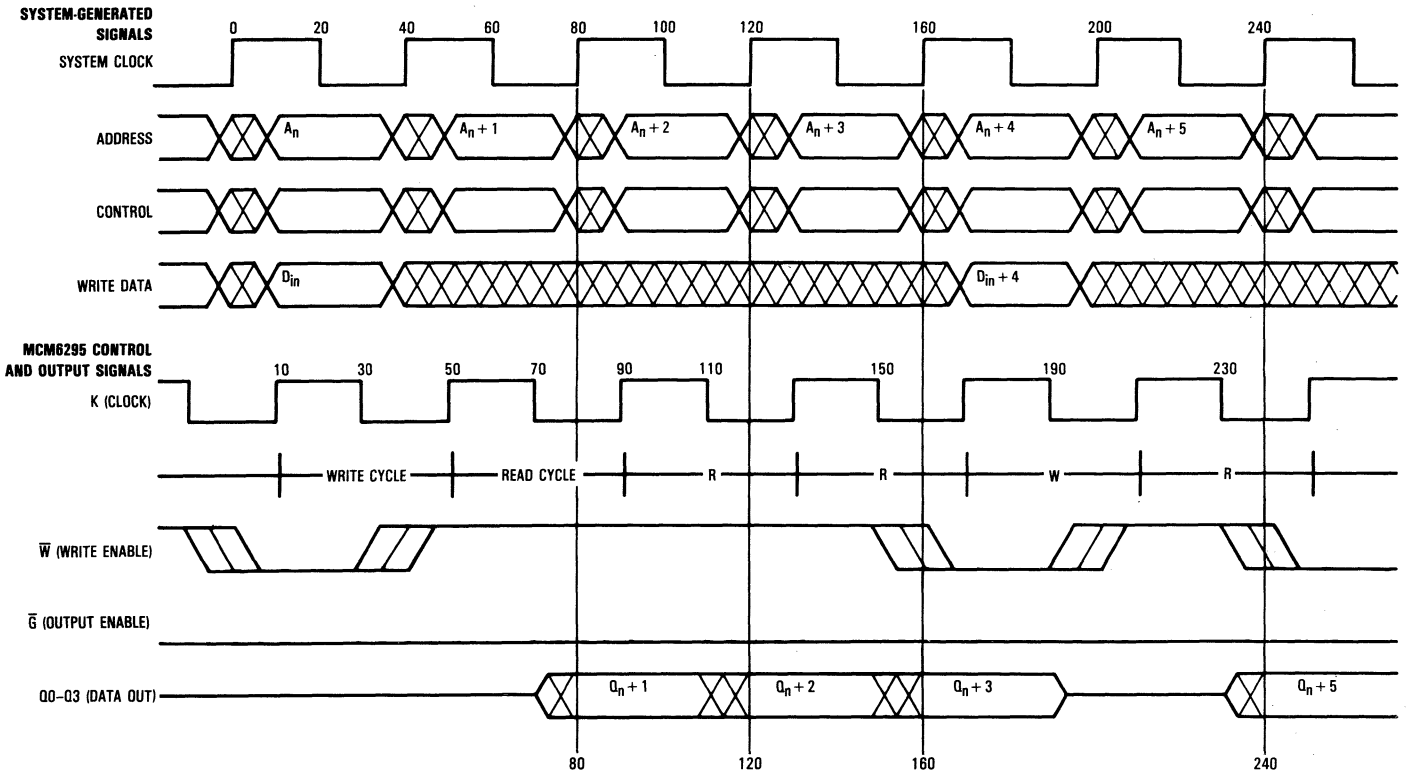


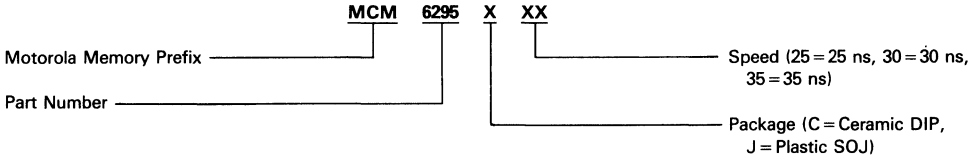
Figure 2. Typical Configuration for a 16-Bit Bus



NOTES:
1. The system supplies address, data, and control information and accepts data from memory on the rising edge of the system clock.
2. The memory clock is delayed 10 ns (for this example) to allow input information to propagate to the memory chips.

Figure 3. Nonpipeline System Timing

ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers—MCM6295C25 MCM6295J25
MCM6295C30 MCM6295J30
MCM6295C35 MCM6295J35

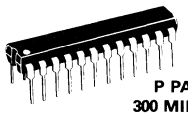
5

MCM62350

Product Preview

4K × 4 Bit Cache Address Tag Comparator

with System Status Bit Functions



P PACKAGE
300 MIL PLASTIC
CASE 724

J PACKAGE
300 MIL SOJ
CASE 810A

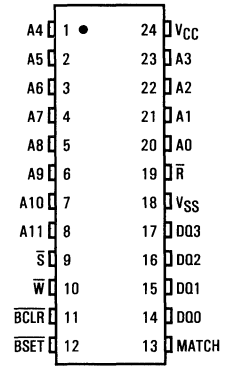
The MCM62350 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's second generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates a 4K × 4 SRAM core, an on-board comparator, and special pin functions for tag valid and system status bit applications. These functions allow easy interface to the MC68020 and MC68030 microprocessors, or any other environment where efficient implementation of external cache memory is required.

The device has a reset ($\overline{R}$) pin for flash clear of the RAM within two minimum cycles. This function is useful for system initialization. Individual bits within a tag can be set or cleared via the $\overline{BSET}$ and $\overline{BCLR}$ control input pins for valid bit updates.

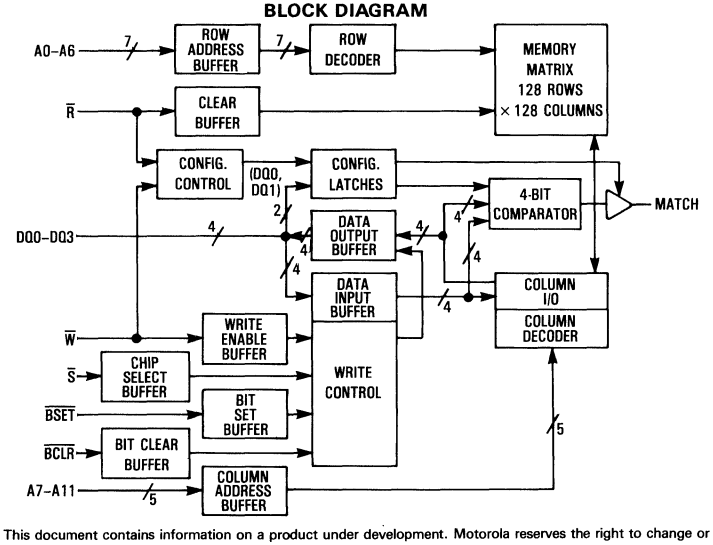
The MCM62350 has two configurable comparator modes. The comparator can be configured as standard XNOR (exclusive NOR) for address tag comparison, or AOI (AND-OR-Invert) for determining whether specific bits in the 4-bit word are set (for system status applications). In addition, the match output can be programmed as true high or true low for potential logic delay savings. The configuration of these modes is accomplished by performing a write cycle with the $\overline{R}$ pin held low.

- Single 5 V ± 10% Power Supply
- Fast Address to Match Time; 22/25/30 ns max
- Fast Data to Match Time; 10/12/15 ns max
- Fast Read of Tag RAM Contents; 25/30/35 ns max
- Flash Clear of the Tag RAM; 50/60/70 ns max
- Programmable Active Output Level of Match
- Bit Manipulation of Tags via $\overline{BSET}$ and $\overline{BCLR}$ Writes
- Configurable Comparator Modes: XNOR Mode for Address Tag Comparison
  AOI Mode for System Valid Bit Comparison

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{BCLR}$	Bit Clear Control Input
$\overline{BSET}$	Bit Set Control Input
$\overline{R}$	Reset (Flash Clear) Input
MATCH	Match (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

MCM62351

Product Preview

4K x 4 Bit Cache Address Tag Comparator

with System Status Bit Functions

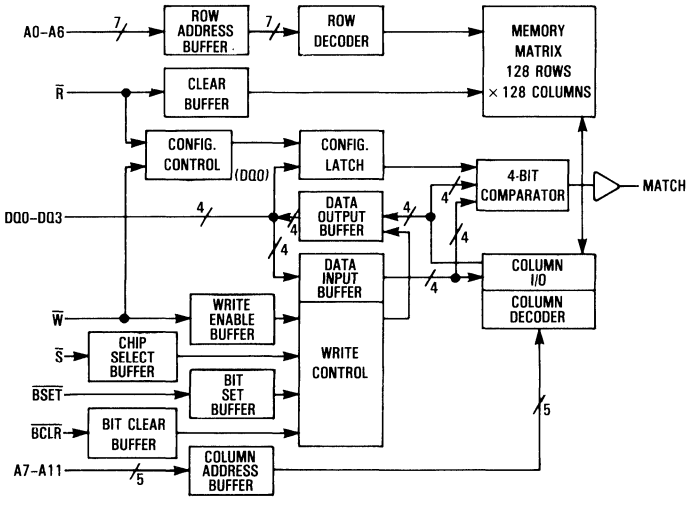
The MCM62351 is a 16,384 bit cache address tag comparator organized as 4096 tags of 4 bits, fabricated using Motorola's second generation high-performance silicon-gate CMOS (HCMOS III) technology. The device integrates a 4K x 4 SRAM core, an on-board comparator, and special pin functions for tag valid and system status bit applications. These functions allow easy interface to the MC68020 and MC68030 microprocessors, or any other environment where efficient implementation of external cache memory is required.

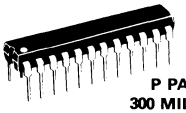
The device has a reset ($\overline{R}$) pin for flash clear of the RAM within two minimum cycles. This function is useful for system initialization. Individual bits within a tag can be set or cleared via the $\overline{BSET}$ and $\overline{BCLR}$ control input pins for valid bit updates.

The MCM62351 has two configurable comparator modes. The comparator can be configured as standard XNOR (exclusive NOR) for address tag comparison, or AOI (AND-OR-Invert) for determining whether specific bits in the 4-bit word are set (for system status applications). The configuration of the comparator is accomplished by performing a write cycle with the $\overline{R}$ pin held low. The match output is open drain, allowing efficient combination of multiple match outputs using a wired-OR connection.

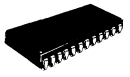
- Single 5 V ±10% Power Supply
- Fast Address to Match Time; 22/25/30 ns max
- Fast Data to Match Time; 10/12/15 ns max
- Fast Read of Tag RAM Contents; 25/30/35 ns max
- Flash Clear of the Tag RAM; 50/60/70 ns max
- Open Drain Match Output
- Bit Manipulation of Tags via $\overline{BSET}$ and $\overline{BCLR}$ Writes
- Configurable Comparator Modes: XNOR Mode for Address Tag Comparison
  AOI Mode for System Valid Bit Comparison

BLOCK DIAGRAM



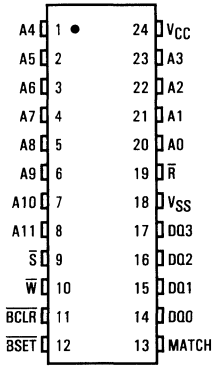


P PACKAGE
300 MIL PLASTIC
CASE 724



J PACKAGE
300 MIL SOJ
CASE 810A

PIN ASSIGNMENT



PIN NAMES	
A0-A11	Address Inputs
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
$\overline{BCLR}$	Bit Clear Control Input
$\overline{BSET}$	Bit Set Control Input
$\overline{R}$	Reset (Flash Clear) Input
MATCH	Match (Hit) Output
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MOS EEPROMs 6

MOS EEPROMs

(+5 V, 0 to 70°C)

Organization	Part Number	Access Time (μs)	Pins
16 × 16	MCM2801P	1	14
32 × 32	MCM2802P	1, 3	14
256 × 8	MCM2814P	3.5	8

MCM2801

Advance Information

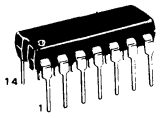
16 x 16-BIT SERIAL ELECTRICALLY ERASABLE PROM

The MCM2801 is a 256-bit serial Electrically Erasable PROM designed for handling small amounts of data in applications requiring both non-volatile memory and in-system information updates.

The MCM2801 offers in-system erase and reprogram capability. It has external control of timing functions and serial format for data and address. The MCM2801 is fabricated in floating gate technology for high reliability and producibility.

- Single +5 V power supply
- Organized as 16 words of 16 bits
- MPU Bus compatible
- Single + 25 V power supply for erase and program
- In-System program/erase capability
- Both word and whole array erasable
- 100,000 write/erase cycles

MOS
(N-CHANNEL, SILICON GATE)
16 × 16 BIT
ELECTRICALLY ERASABLE
PROGRAMMABLE READ
ONLY MEMORY



PLASTIC PACKAGE
CASE 646

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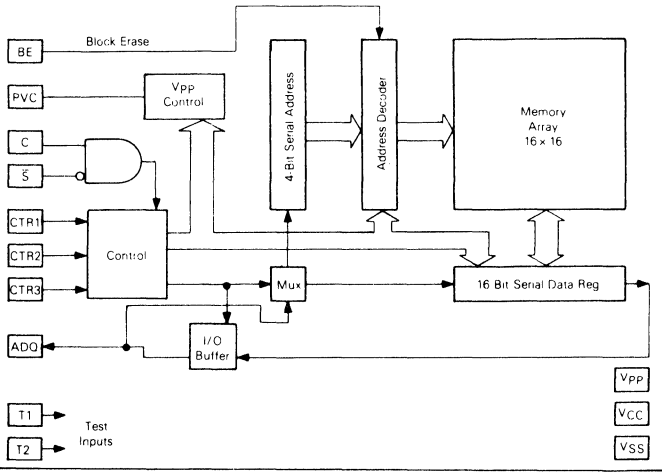
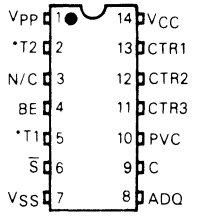
BLOCK DIAGRAM



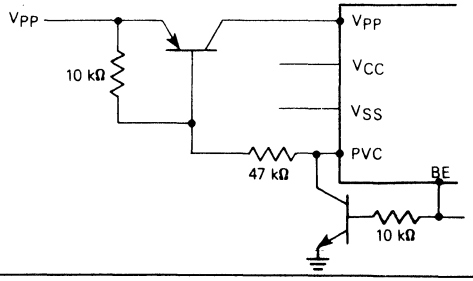
PIN ASSIGNMENT



*For normal operation, these inputs should be hardwired to V_{SS}.

PIN NAMES	
ADQ	Multiplexed Address/ Data-In/Data-Out
C	Clock
PVC	Program Voltage Control
CTR1, 2, 3	Control
BE	Block Erase
$\overline{S}$	Chip Select
T1, T2	Test Pins

FIGURE 1 - TYPICAL V_{PP} CONTROL
(See AC CONDITIONS AND CHARACTERISTICS - NOTE 2)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This is advance information and specifications are subject to change without notice.

MODE SELECTION

Mode	Pin Number						
	1 V_{PP}	6 $\overline{S}$	7 V_{SS}	11 CTR3	12 CTR2	13 CTR1	14 V_{CC}
Standby	V_{SS} or V_{CC}	V_{IH}	V_{SS}	V_{IH}	V_{IH}	V_{IH}	V_{CC}
Word Erase	V_{PP}	V_{IL}	V_{SS}	V_{IH}	V_{IL}	V_{IL}	V_{CC}
Write	V_{PP}	V_{IL}	V_{SS}	V_{IL}	V_{IH}	V_{IL}	V_{CC}
Serial Data Out	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IH}	V_{IH}	V_{IL}	V_{CC}
Serial Address In	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IL}	V_{IL}	V_{IH}	V_{CC}
Serial Data In	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IH}	V_{IL}	V_{IH}	V_{CC}
Read	V_{SS} or V_{CC}	V_{IL}	V_{SS}	V_{IL}	V_{IH}	V_{IH}	V_{CC}
Standby	V_{SS} or V_{CC}	V_{IH}	V_{SS}	V_{IL}	V_{IL}	V_{IL}	V_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Rating	Value	Unit
Temperature Under Bias	−40 to +85	°C
Operating Temperature Range	0 to +70	°C
Storage Temperature	−55 to +150	°C
All Input or Output Voltages with Respect to V_{SS} (Except PVC)	+8 to −0.5	V
V_{PP} Supply Voltage with Respect to V_{SS}	+28 to −0.5	V
PVC Voltage with Respect to V_{SS}	+28 to −0.5	V

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

6

RECOMMENDED DC OPERATING CONDITIONS (Full operating voltage and temperature range unless otherwise noted.)

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC} V_{PP}	4.5 24.0	5.0 25	5.5 26.0	V
Input High Voltage	V_{IH}	2.4	–	V_{CC} + 1.0	V
Input Low Voltage	V_{IL}	−0.1	–	0.8	V

OPERATING DC CHARACTERISTICS

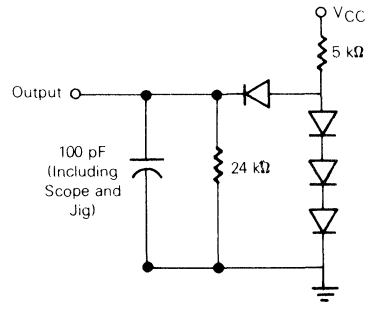
Characteristic	Condition	Symbol	Min	Typ	Max	Units
Input Sink Current	$0 < V_{in} < V_{CC}$	I_{in}	–	–	10	μA
V_{CC} Supply Current	$V_{CC} = 5.5$ V	I_{CC}	–	–	30	mA
V_{PP} Supply Current	$V_{PP} = 26.0$ V	I_{PP}	–	–	4.0	mA
Output Low Voltage	$I_{OL} = 1.0$ mA	V_{OL}	–	–	0.5	V
Output High Voltage	$I_{OH} = -0.1$ mA	V_{OH}	2.4	–	–	V
PVC Current (Write or Word Erase)	PVCL = 1 V	PVC_{ON}	200	–	–	μA
PVC Leakage	PVCH = 26 V	PVC_{OFF}	–	–	5	μA

CAPACITANCE (f = 1.0 MHz, $T_A = 25°C$, $V_{CC} = +5$ V, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance ($V_{in} = 0$ V)	C_{in}	–	6.0	pF
Output Capacitance ($V_{out} = 0$ V)	C_{out}	–	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\Delta_t/\Delta V$.

FIGURE 2 — OUTPUT LOAD



AC OPERATING CONDITIONS AND CHARACTERISTICS

Input Pulse Levels ..... 0.65 Volts and 2.6 Volts
Input Rise and Fall Times ..... 20 ns
Input Timing Levels ..... 1.0 Volt and 3.8 Volts
Output Timing Levels ..... 1.0 Volt and 2 Volts
Output Load ..... See Figure 2

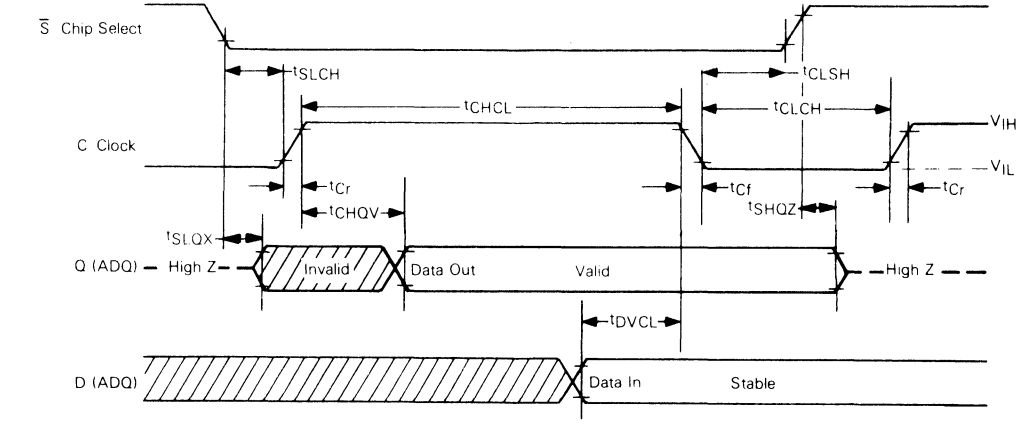
Characteristic	Symbol	Min	Max	Unit
Erase Time	t_{ERASE}	100	–	ms
Write Time	t_{WRITE}	10	–	ms
Clock High Level Hold Time	t_{CHCL}	4	10	μs
Clock Low Level Hold Time	t_{CLCH}	4	–	μs
Clock Rise Time	t_{Cr}	5	1000	ns
Clock Fall Time	t_{Cf}	5	1000	ns
Chip Select Setup	t_{SLCH}	1	–	μs
Chip Select Hold	t_{CLSH}	1	–	μs
Data Out Delay	t_{CHQV}	–	1	μs
Address In Setup	t_{AVCL}	1	–	μs
Data In Setup	t_{DVCL}	1		μs
Control Setup Time	t_{CtrVCH}	1	–	μs
Control Hold Time	t_{CtrX}	50	–	ns
Data-Off Time (from the Clock)	t_{CHQZ}	–	3.0	μs
Chip Select Low to Output Active Time	t_{SLQX}	–	2.0	μs
Data-Off Time (from Chip Select)	t_{SHQZ}	–	2.0	μs

NOTE 2: During application of V_{PP}, a 1 μF ceramic capacitor is recommended between V_{PP} and Ground to suppress any voltage transients which might damage the device.

6

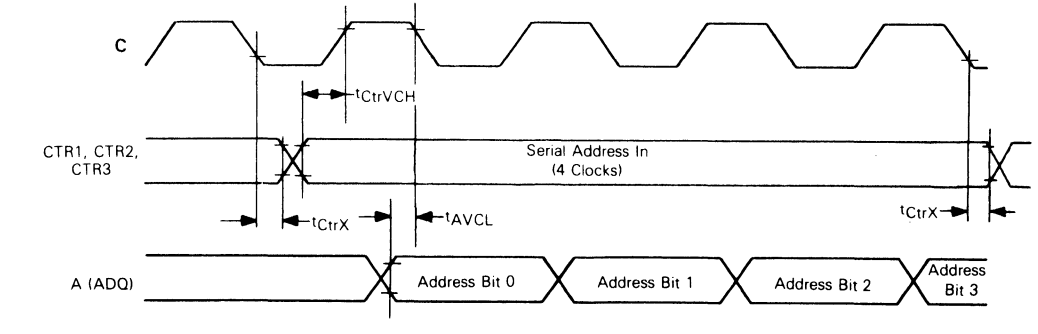
TIMING DIAGRAMS

Clock Cycle Detail

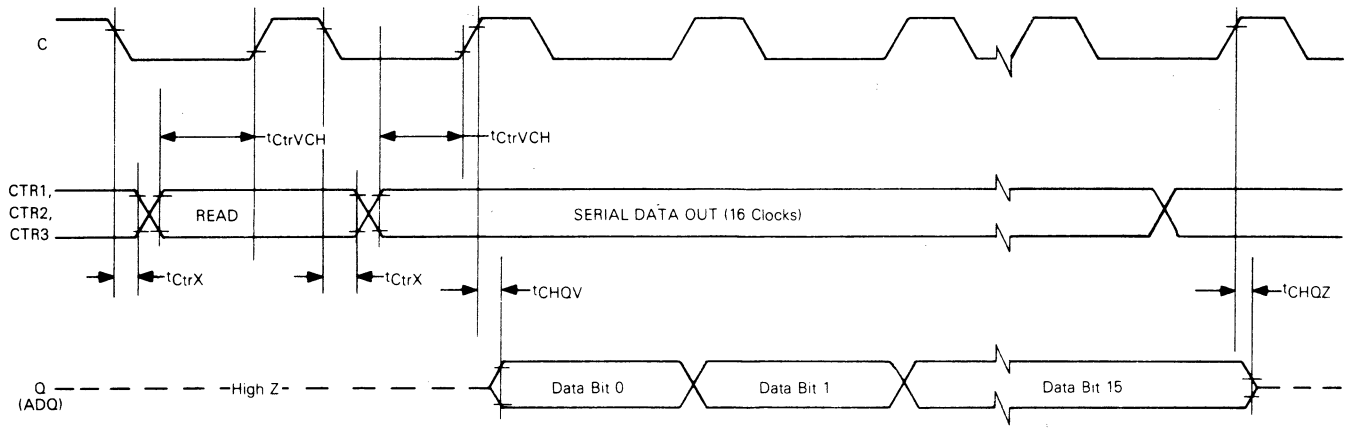


All times defined at 10% or 90% points.

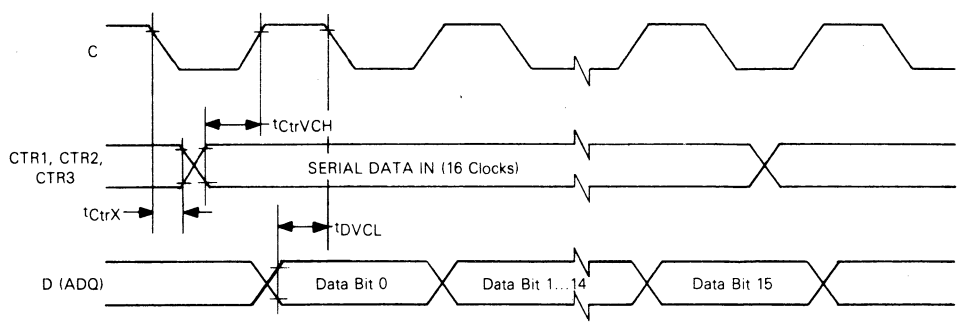
Serial Address In



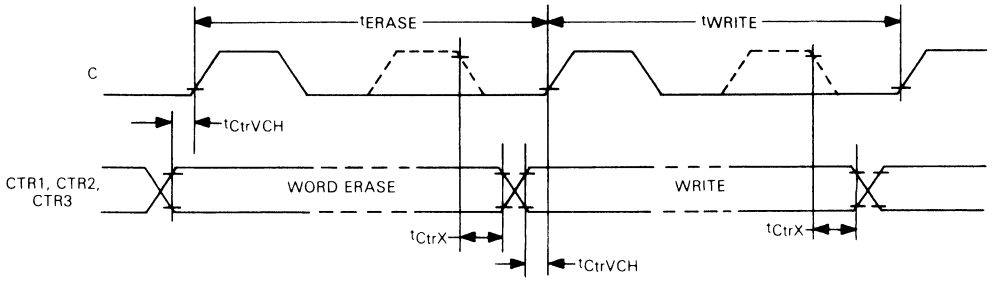
READ AND SERIAL DATA OUT



SERIAL DATA IN



ERASE-WRITE SEQUENCE



NOTE: One clock pulse is sufficient to load a new control code.

FUNCTIONAL DESCRIPTION

The memory stores sixteen words, each of sixteen bits. All functions are selected by a 3-bit parallel control code. The clock line is used to strobe these codes and to serially shift data and addresses.

Read-Out

1. The 4-bit serial address is shifted on the ADQ line while the SERIAL ADDRESS-IN code is applied on the three control pins.
2. The READ instruction is strobed with one clock pulse. This reads the word from the new address in the memory array and parallel loads it into the data register.
3. While the SERIAL DATA-OUT code is being applied, data is shifted out on the ADQ pin with 16 clock pulses. In this mode, the ADQ pin output buffer is active.

Writing

1. The address is changed, if necessary, in the same manner as in the readout.
2. While the SERIAL DATA-IN code is being applied, data is shifted in on the ADQ pin with 16 clock pulses. If the data to be written has already been shifted into the data register, it is not necessary to re-enter the 16 bits, so this step may be omitted.
3. The WORD ERASE code is strobed in with one clock pulse. After the specified ERASE time, the addressed word is erased.
4. The WRITE code is strobed in with one clock pulse. After the specified WRITE time, a STANDBY code can be strobed in to stop writing. Data will be programmed at the specified address.

   It is also possible to change the sequence by erasing a memory location before starting a write sequence.

Standby

Either of the two STANDBY codes, when strobed in with a clock pulse, puts the memory in a quiescent state. The output is then in the high-impedance state and the absence or presence of the clock will not affect the device.

Pin Description

The active high clock signal (C) is used for shifting addresses and data into or out of the chip. It is also used for strobing control codes.

The I/O pin (ADQ) is used for entering addresses and data in. It is in the output state only for shifting output data.

The active low Chip Select pin (S) is only used to block the clock and put the ADQ buffer into the high-impedance mode. It has no influence on the operating status of the device and does not force a standby condition.

The programming voltage control pin (PVC) is an open-drain output that is active when a WORD ERASE or WRITE control code is strobed in. As shown in Figure 1, it can be used to control the V_{PP} supply applied to the circuit. The BLOCK ERASE (BE) pin can be used to clear the whole array. As the PVC output is not active in this state, the programming voltage should be directly applied to the V_{PP} pin for the specified erase time.

The Test inputs (TEST1) and TEST2) are provided for testing purpose only and should be connected to V_{SS} in any application.

Data Protection

When V_{PP} is turned off, data stored in the array is protected. The programming voltage should not be applied to the V_{PP} pin if V_{CC} is not present. Therefore, use of the PVC control output, which is controlled by the V_{CC} supply is recommended. Using this feature, V_{PP} and V_{CC} can be turned on or off in any sequence without disturbing data in the array. However, to avoid spurious control codes being strobed into the device, all inputs should be stable when V_{PP} is on.

General Comments

The erased state corresponds to a logical zero at the ADQ output.

WRITE (for any address) must be preceded by an ERASE at the same address.

V_{PP} is necessary for WRITE, WORD ERASE or BLOCK ERASE. In all other cases, it can be switched to high impedance, V_{CC} or V_{SS}.

MCM2802

32x32 BIT SERIAL ELECTRICALLY ERASABLE PROM

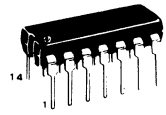
The MCM2802 is a 1K-bit serial Electrically Erasable PROM designed for applications requiring both non-volatile memory and in-system information updates. In digital tuning systems, it provides storage for up to 32 channels. It has external control of timing functions and serial format for data and address.

- Single 5V supply in Read mode
- Organised as 32 Words of 32 Bits
- 5V and 25V supply for Erase and Program
- In-System Program/Erase Capability
- 0–100 kHz clock rate
- Floating gate process
- Expandable to 16K-bit systems
- Word and Array erasable
- 100,000 Write/Erase Cycles

MOS

(N-CHANNEL, SILICON GATE)

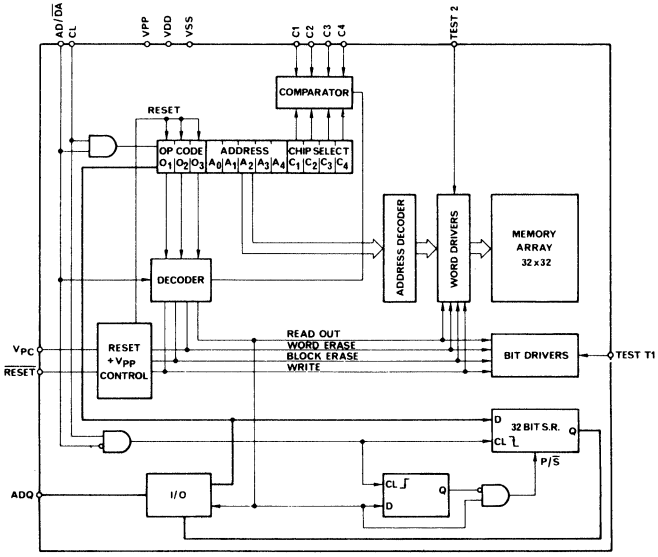
32 × 32 BIT
ELECTRICALLY ERASABLE PROM



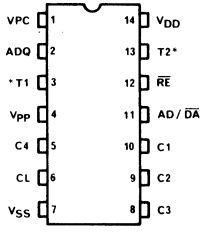
P SUFFIX
PLASTIC PACKAGE
CASE 646

6

FIGURE 1 – BLOCK DIAGRAM



PIN ASSIGNMENT



*For normal operation, hardwired to V_{SS}

PIN NAMES

VPC . . . . . Program Voltage Control
ADQ . . . Address Input + Data Input/Output
T1, T2 . . . . . Margin Testing
C1, C2, C3, C4 . . . . . Chip Address 1 to 4
CL . . . . . Clock
$\overline{RE}$ . . . . . Reset
AD/$\overline{DA}$ . . . . . Shift Register Select

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (Voltages referred to V_{SS})

Rating	Symbol	Min.	Max.	Unit
DC Supply Voltage	V_{DD}	- 0.5	8	Vdc
Programming Voltage	V_{PP}	- 0.5	28	Vdc
Input Voltage	V_{IN}	- 0.5	8	Vdc
VP Control Output	V_{PC}	- 0.5	28	Vdc
Operating Temperature Range	T_A	0	70	°C
Storage Temperature Range	T_{STG}	- 55	150	°C

NOTE – Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

SWITCHING CHARACTERISTICS (T_A = 0... 70°C, V_{DD} = 5V ± 10%, V_{PP} = 25V ± 1V)

Pin	Symbol	Parameter	Fig. No.	Min.	Max.	Unit
	t_{ER}	Erase time		100		ms
	t_{WR}	Write time		10		ms
CL	F_{CL}	Clock Frequency $F_{CL} = 1/T_{CL}$	2		100	kHz
CL	t_{CLH}	Clock High Level Hold Time	2	4		µs
CL	t_{CLL}	Clock Low Level Hold Time	2	4		µs
CL	t_{CLRF}	Clock Fall Time and Rise Time	2		1	µs
AD/DA	$t_{AD/DA}$	Register Control to Clock				
		Delay Time except for t_{READ}	2	1		µs
	t_{READ}	After READ opcode only	3	2	100	µs
ADQ	t_{DSUP}	Address/Data In Set-Up	2, 3	2		µs
	t_{DH}	Address/Data In Hold	2, 3	2.0		µs
ADQ	t_{DOUTS}	Data Out Serial Delay	3		1	µs.
	t_{DOUTP}	Data Out Parallel Delay	3		3	µs
	C_{out}	Output Capacitance (V_{out} = 0 V)			12	pF
	C_{in}	Input Capacitance (V_{in} = 0 V)			12	pF

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DC CHARACTERISTICS (T_A = 0... 70°C, V_{DD} = 5V ± 10%, V_{PP} = 25V ± 1V)

Pin	Characteristic	Condition	Symbol	Min.	Max.	Unit
V_{PP}	Supply Current		I_{PP}		3	mA
V_{DD}	Supply Current		I_{DD}		20	mA
ADQ	Tristate Input/Output	V_{OH} = 2.4V	I_{OH}	- 0.1		mA
		V_{OL} = 0.5V	I_{OL}	1.6		mA
		Tristate	I_{IN}		10	µA
All Inputs Except ADQ	Input Leakage		I_{IN}		10	µA
V_{PC}	VP Control	V_{ON} = 1V	I_{ON}	0.7		mA
	Pull down device	OFF state	V_{MAX}		V_{PP}	V
		V_{OFF} = VP	I_{OFF}		10	µA
All Inputs	Input Low Voltage	V_{IL}		0.1	0.8	V
	Input High Voltage	V_{IH}		2.4	5.5	V

FIGURE 2 – GENERAL TIMINGS

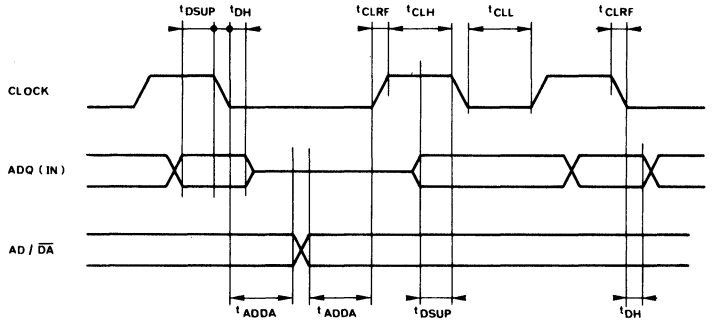


FIGURE 3 – READOUT TIMINGS

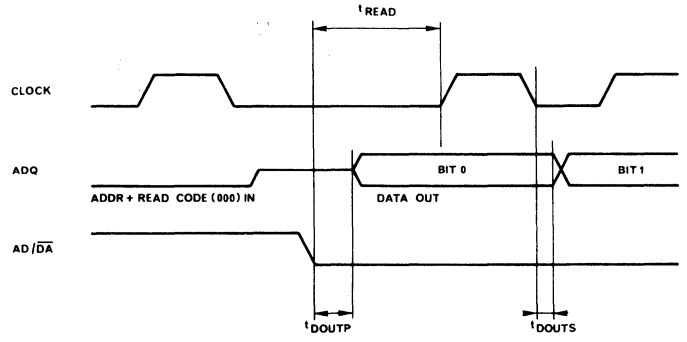


FIGURE 4 – READOUT SEQUENCE

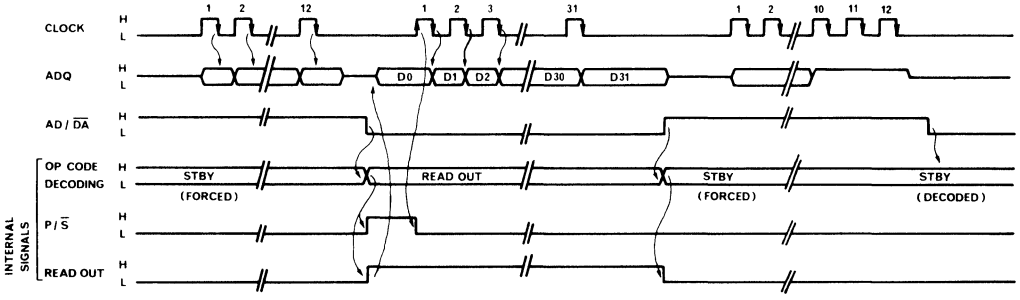


FIGURE 5 – WRITE SEQUENCE

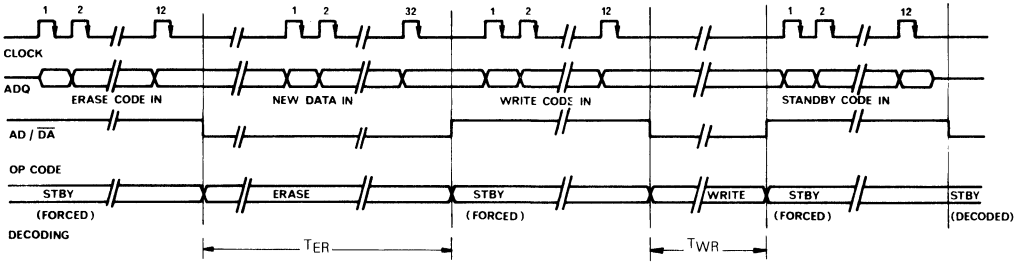
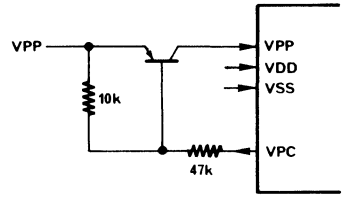
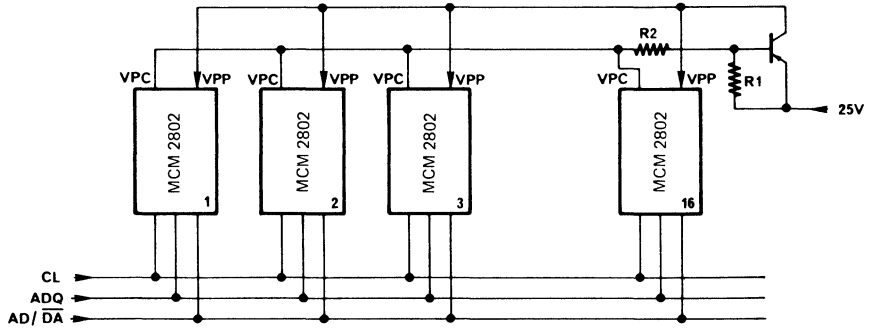


FIGURE 6 – Vpp CONTROL AND MULTICHIP SETUP





FUNCTIONAL DESCRIPTION

The circuit accepts 12 bits of Address/Op code in the address register and 32 bits of data in the data register (see figure 1: Block diagram).

ADDRESS/OP CODE FORMAT (figure 1)

The four shifted bits C1 to C4 are used as chip select word in multichip systems. The chip address is defined by hardwiring the C1 to C4 pins. These bits are adjacent to the address field, so that no software modification is required in a program designed for a multi-1K memory application.

The five following A1 to A5 bits select one of the word addresses. The last 3 bits 01 to 03 control the operating modes.

Function	01	02	03
Read	0	0	0
Word Erase	0	1	0
Block Erase	1	1	0
Write	1	0	0
Standby	X	X	1

6

READ OPERATION (figure 4)

1) The ADDRESS/OP CODE is loaded. The address selecting the word to be read and the op code bits being the READ code.

2) The AD/$\overline{DA}$ is switched to the data mode, thus initiating the parallel transfer from the core to the shift register. First bit of data is present at the output.

3) As soon as the first of the 31 data out clock pulses is applied, the parallel transfer is stopped and data is shifted at the output. Data is recirculated in the data register.

4) The output buffer is turned on only when READ is internally decoded, AD/$\overline{DA}$ is low and chip is selected by C1 and C4. Otherwise it is in the high impedance state.
Addresses and data are clocked in and out with the falling edge of clock.
An erased bit corresponds to a low level output.

WRITING (figure 5)

1) ADDRESS/OP CODE is shifted in, the op code being either BLOCK ERASE or WORD ERASE.

2) Switching the AD/$\overline{DA}$ line low for t = t_{ERASE} initiates the erase process. During this period of time, a data word can be shifted into the data register.

3) Then the WRITE code and the same address is loaded to the address register.

4) The AD/$\overline{DA}$ line is switched low again for a t = t_{WRITE}, during which the selected word is programmed.

5) At the end of the WRITE operation it is recommended to load op code STANDBY and to return input AD/$\overline{DA}$ to the low state.

ERASE

Both BLOCK ERASE and WORD ERASE are provided and are controlled by the op code. VPP has to be applied for BLOCK ERASE, WORD ERASE and for WRITE. For all other conditions it can be switched off to high impedance or V_{DD} or V_{SS}.

STANDBY

When AD/$\overline{DA}$ is high, the instruction decoder is disabled and hence STANDBY is forced. By shifting the STANDBY op code into the address register STANDBY will be recognized independently of the state of AD/DA.

CLOCK

The active high clock is only used for shifting data and addresses. This shift occurs on the clock falling edge.

CHIP SELECTION

The ADDRESS/DATA line can be used as a chip select in a system having other serial I/O devices. DATA and CLOCK lines being shared the non-volatile memory is only activated when the AD/$\overline{DA}$ line is low. Shifting information to the data register has no effect to the core while the chip is deselected.
In a multi-memory arrangement, all the lines including ADDRESS/DATA, CLOCK and DATA, are shared, with the exception of C1 to C4 which are hardwired to V_{DD} or V_{SS}, thus defining the circuit address. All V_P control outputs of the memory circuits can be combined in a wired OR configuration.

DATA PROTECTION

When V_{PP} is turned off, data stored in the array is always protected. A V_{PP} control output is provided for switching the V_{PP} supply. It consists of a pull down device to V_{SS}. This device is turned on only when: V_{DD} is present, a WRITE or ERASE code has been loaded in the address register and AD/$\overline{DA}$ is low.
Schematics for this external V_{PP} control are proposed in figure 6.

RESET

V_{PP} and V_{DD} may be turned on or off in any sequence without disturbing data in the NVM array. During power up, the op code is preset to the standby mode. The $\overline{RESET}$ input can be connected to the system $\overline{RESET}$.

MCM2814

Advance Information

256x8 BIT SERIAL EEPROM

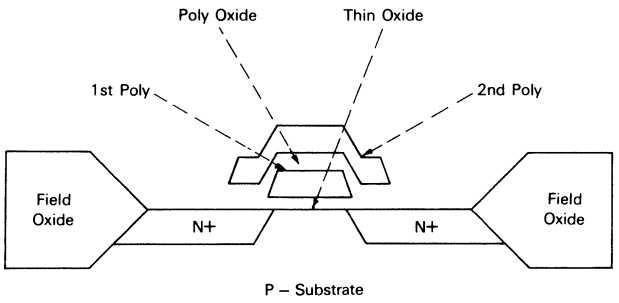
The MCM2814 is a 2048-bit serial electrically erasable PROM. Designed for handling data in applications requiring both non-volatile memory and in-system information updates.

The MCM2814 is fabricated in an 8-pin DIL package using floating-gate HCMOS EEPROM technology.

Features:

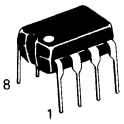
- 8-pin DIP, in HCMOS for low consumption.
- 2048 bits organised as 256 bytes.
- Byte programmable.
- 3 – 6 V supply during read operations.
- On-chip Programming Voltage Generator.
- Two programming modes: two-wire serial access, M-bus/four-wire serial access SPI.
- Data protection of ¼, ½, or ¾ array with EEPROM bits.
- Simultaneous programming of 1 to 4 bytes.
- Automatic byte address increment in Read mode.
- Chip selection with separate pin.
- Single 4.5 V to 6 V supply during programming.
- Digital filtering on Clock and Data inputs.
- Bit program operation: no byte erase necessary.
- Data protection after Reset.
- Write/Erase endurance: 10000 cycles.
- Data retention: 10 years.

FETMOS
(Floating-Gate Electron Tunnelling MOS)



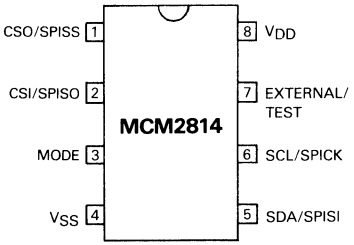
This document contains information on a new product. Specifications and information herein are subject to change without notice.

HCMOS
(FLOATING-GATE TECHNOLOGY)
256 x 8 BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY



P SUFFIX
PLASTIC PACKAGE
CASE 626-04

PIN ASSIGNMENT



PIN DESCRIPTION

V_{DD}:	Power Supply
V_{SS}:	Ground (Ref)
External/ Test	Connected to on-chip Voltage Multiplier output
Mode =	0 M-bus
CS0	Chip Select (Hardwired)
CS1	Chip Select (Hardwired)
SDA	Serial Date I/O
SCL	Serial Clock Input
Mode =	1 SPI
SPISS	Slave Select Input
SPISO	Serial Data Output
SPISI	Serial Data Input
SPICK	Serial Clock Input

6

SECTION 1. PIN DESCRIPTION

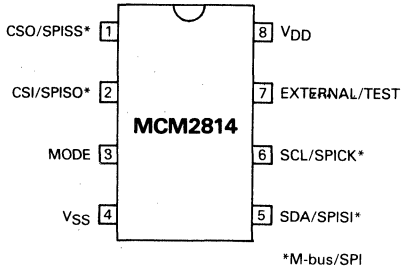


Figure 1 Pinout

1.1 V_{SS}/V_{DD} (Pins 4/8)

V_{DD} and V_{SS} are used to power the circuit. In read mode this supply voltage must be comprised in the V_{DDR} range. (See **5.2 Electrical Characteristics**). In program mode this supply range is limited to V_{DDP}.

1.2 External/Test (Pin 7)

This pin is used for testing the on-chip voltage multiplier that generates the programming voltage required for a program operation, and should be left open for 5 Volt only operation.
An external capacitor (Low leakage) on this pin might have a positive impact on the programming endurance, as the V_{PP} rise time will be increased.
Recommendations will be issued after the characterisation. As this on-chip generator has a high impedance, an external supply can be connected to this pin. This also allows to block any inadvertant programming by maintaining this pin at V_{DD}.

1.3 Mode (Pin 3)

This pin is used to select one of two modes of operation: M-bus mode at the low logic level or SPI mode at high level.
This pin is usually hardwired to V_{SS} or V_{DD}. It should only be changed if the circuit is internally in a standby state.
This pin is high impedance when V_{DD} is at V_{SS} level.

1.4 CS1 / SPISO (Pin 2)

In M-bus mode, this pin is used for selecting multiple identical chips on the same serial bus. The chip address is formed by 5 bits predefined for this chip, followed by 2 additional chip select bits. These last two bits must correspond to the CS1 / CS0 code for proper chip selection. Up to four MCM 2814 can be connected on the same SCL and SDA lines. (See **Figure 4**).

In SPI mode this pin is a push-pull slave data output (SPISO). It will shift-out byte addresses and data as described in Section 4.
This pin is usually connected to the data input pin of a SPI master (MISO).
This pin can not be pulled higher than 0.5 V above V_{DD}, even if V_{DD} is at V_{SS} level.

1.5 CSO / SPISS (Pin 1)

In M-bus mode this pin is used in conjunction with CS1 for chip selection. (See **above**).

In SPI mode this pin is a Slave Select input. In this mode the serial access is deselected when the SPISS input is high, and the SPISO data output pin is forced high impedance. Multiple chips using the same SPICK, SPISI and SPISO lines, can be selected via this pin as described in Figure 10.
After powering up the device, a falling edge of the SPISS line is required to start the SPI serial access.

This pin is high impedance when V_{DD} is at V_{SS} level.

1.6 SCL / SPICK (Pin 6)

The serial clock is supplied on pin SCL / SPICK. This pin is an input only, therefore the chip can only operate as a slave under the control of a serial bus master.
The clock input rising edge is used to shift in data present on the SDA/SPISI pin, and the falling edge is used to shift out data on the SDA or SPISO pin.

This pin is high impedance when V_{DD} is at V_{SS} level.

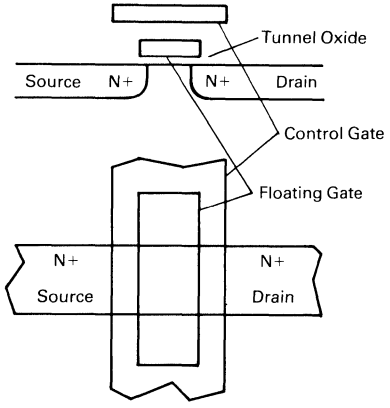
1.7 SDA / SPISI (Pin 5)

In M-bus mode, SDA pin is used to transmit data serially in the memory (Receiver) or from the memory (Transmitter). Data transmitted via this pin includes chip addresses, byte addresses, byte data, Read/Write and acknowledge bits. When SDA is in output, it operates as a pull-down only device (Open-drain). The protocol of this transmission is described in Figures 5 and 6.

In SPI mode, this pin is a Slave data Input (SPISI) only and is used to receive opcodes, byte addresses and byte data. It is usually connected to the data output pin of a SPI master. (MOSI).

This pin is high impedance when V_{DD} is at V_{SS} level.

SECTION 2. EEPROM



	CG	D	S
READ	0V	VDD	0V
PROG 1	0V	VPP	OPEN
PROG 0	VPP	0V	0V

Figure 2 EEPROM Transistor

256 Bytes of EEPROM memory are implemented in a floating gate double poly-silicon process. A Byte Address register is used to select one of the bytes. Three basic state of operation can be distinguished :

- Standby state.
- Read state
- Program state

2.1 EEPROM Operation

2.1.1 Standby State

In this state, neither a programming, nor a serial transmission occurs, and the power consumption is minimum. (See **3.4.1** and **4.5**).

2.1.2 Read State

In read state the data of the selected byte is transferred from the memory array to the data shift register used for the serial transmission. This state is active during a serial transmission.

2.1.3 Program State

In this state, a programming voltage higher than V_{DD} is necessary. This voltage is generated by the on-chip voltage multiplier or can be supplied externally. During programming V_{DD} must be within the V_{DDP} range. (See **5.2**).

In M-bus mode, the programming starts at the end of a write command, when a STOP or a new START condition occurs. The programming is enabled at this time, as well as the on-chip voltage multiplier. If there is a capacitive load on the V_{PP} pin, the V_{PP} rise time should be added to the minimum program time t_{PROG}.

In SPI mode, programming could start when a write serial transmission is ended with an SPISS rising edge. Actual programming will only happen if enabled by a V_{PP} enable serial command. This command can be transmitted before or after the write sequence.

2.2 EEPROM Data Protection

Some circuitry has been included to prevent unwanted modification of EEPROM data, and is described below. However, a noisy serial link is very often the cause of bad data or data written to the wrong address. Besides measures to reduce this noise on the board, the serial clock and data inputs (SCL/SDA) have Schmitt triggers and digital filters to reject some of the noise.

2.2.1 Power Up Reset

Immediately after power is applied, programming is inhibited to prevent EEPROM data loss during the system power up.

In both modes this condition is removed when a READ is performed.
In M-bus mode, the read bit with a valid chip address gives the control to the MCM2814. Therefore another 8 bits read without master acknowledge is necessary to stop the read sequence.
In SPI mode, it is sufficient to send the READ opcode before a new V_{PP} enable command and the write sequence.

At Reset the following circuitry is initialised:

- The circuit is in standby state.
- In M-bus mode, it is waiting for a start condition.
- In SPI mode, it is waiting for a high to low SPISS transition.
- The data outputs are high impedance (SDA, SPISO).
- The programming is disabled.
- The on-chip V_{PP} generator is off.
- The byte address register is cleared ($00).

2.2.2 Programming Voltage Enable

In SPI mode only, an internal programming voltage enable flip-flop can be set or cleared with two separate opcodes, thus reducing the risk of unwanted EEPROM programming.

2.2.3 Array Write Protect

In both modes, byte address 255 ($FF) contains EEPROM bits with a special function. When one or two bits of this address are programmed at once, the programming of EEPROM sections is inhibited according to the following table:

Data at ADDR $FF		Protected Addresses	No. of Bytes Protected
XXXX	00XX	No Write Prot.	-
XXXX	01XX	$C0 – $FB	60
XXXX	10XX	$80 – $FB	124
XXXX	11XX	$40 – $FB	188

X = Don't care

Table 1 EEPROM Write Protect

This protection is reversible as address 255 ($FF) can be modified at any time.

2.3 EEPROM Properties

NO ERASE : Unlike most EEPROM's it is not necessary to erase a byte before writing new data to it.
The program operation takes t_{PROG} and must be externally timed.

CUMULATIVE : As the programming operation is under external control, it can be done at once or at various time frames as long as the total programming time exceeds the specified minimum t_{PROG} value.
t_{PROG} is defined with V_{PP} at its programming level.

SELF LIMITING : Excess pogramming has no positive effect, as programmed EEPROM thresholds will asymptotically reach their nominal values. Programming durations above the recommended maximum t_{PROG} have negative impacts on the EEPROM programming endurance.

2.4 EEPROM Reliability

Reliability figures are statistical in nature. Therefore no minimum or maximum specifications can be applied. The result of reliability tests will be published instead. These tests are conducted on a regular basis during the production life of a circuit and reports are available upon request.

2.4.1 Data Retention

Typical data retention should exceed 10 years for the specified operating temperature range. Data retention is usually tested with the device under bias, but without accessing the EEPROM array.

2.4.2 Read Stress

Unlike some non-volatile memories, there should be no disturbance of the stored data under continuous read of EEPROM bytes. The life limit under continuous read condition should therefore be similar to the normal operating life of the device.

2.4.3 Program Endurance

As for all EEPROM's, there is a wearout mechanism associated with the programming mechanism of the non volatile memory. More than 10,000 programming cycles should be possible per memory bit, for the specified operating temperature range. A programming cycle is defined as a 0 to 1 to 0 programming. Unlike most EEPROM's where the whole byte is erased before being re-programmed, if just one bit is modified in a byte, only this bit will see the programming stress.
Some endurance experiments have shown that the number of programming cycles can be increased if the V_{PP} rise time is increased. This can be achieved with an external capacitor on V_{PP} when the on-chip V_{PP} generator is used. In SPI mode, the V_{PP} should be enabled after the write command has been transmitted.
If an external V_{PP} is provided, it should be ramped up only after the write command is transmitted. In this case, a V_{PP} above the maximum value has also a neagtive impact on the endurance.

2.5 Vpp Voltage Multiplier

In M-bus mode, the on-chip V_{PP} generator is turned on or off automatically during a program sequence.

In SPI mode, it is switched on only after a serial V_{PP} enable command has been issued, independently of write or read commands.

SECTION 3. M-BUS OPERATING MODE

The MODE pin can be hardwired to V_{DD} or V_{SS} to select two different modes of operation. Differences are at the serial transmission level and in the EEPROM operation. They are called M-bus mode and SPI mode.

3.1 M-bus Mode

Only two wires are needed to control the device operation. The serial transmission of this mode is similar to the IIC (*) serial communication standard. It features :

- Up to 4 identical chips on the same 2 wire bus.
- CS1 / CS0 pins for chip selection.
- SCL clock line, input only.
- SDA line used as Input and Output.
- Data acknowledge bit generated.
- Auto programming after reception of new data.
- Programming time under external control.
- Write inhibit after reset.

*IIC is a trademark of Philips

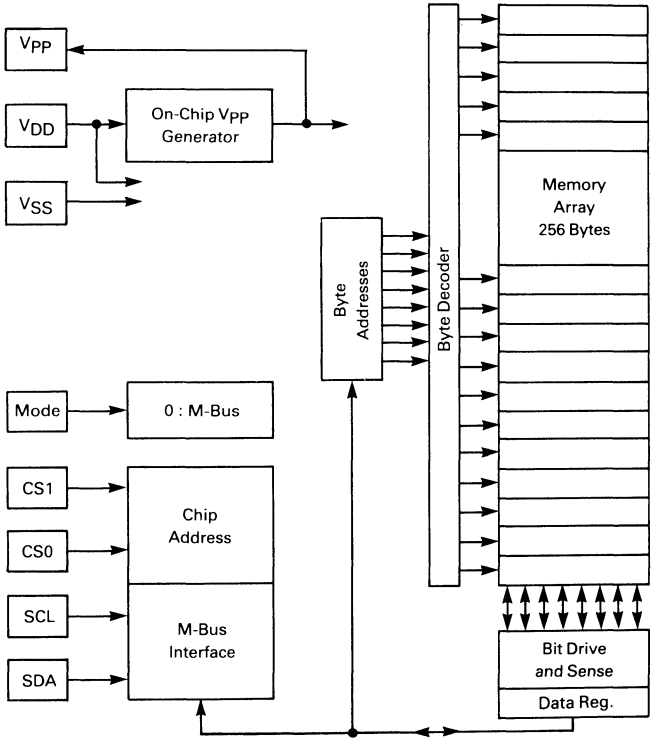


Figure 3 M-bus Block Diagram

3.2 Lexicon

This lexicon will describe some terms used in this serial interface description.

MASTER : The device that initiates the serial transmission is designated as master. In general, it is the device generating the clock. This memory can never function as a master.

SLAVE : This memory always operates as a slave.

TRANSMITTER : The device with its SDA pin in output is a data transmitter. In the case of multiple devices in output, the device sending a low level will win due to the Open-Drain connection.

RECEIVER : A device that has been properly selected by a chip address followed by a write bit is a receiver, and will

shift data present on the SDA pin in internal registers.

MSB : The Most Significant Bit is the first bit transmitted and received.

START CONDITION : The start condition is defined as a 1 to 0 transition of SDA when SCL is high. The first byte of data following a start condition includes the chip address followed by the R/W bit. All devices connected on the same bus receive this data to check if they are addressed.

STOP CONDITION : The stop condition is defined as a 0 to 1 transition of SDA when SCL is high. In this circuit, the stop condition is never mandatory. An EEPROM programming can be initiated by the STOP or also by any following START condition.
A STOP after a serial read sequence will put the device in standby state.

CHIP ADDRESS : The first byte transmitted after a START contains the chip address followed by the Read/Write bit. The 7 bit chip address is formed of 5 fixed bits followed by 2 chip select bits.
Fixed bits are 1010X for this device (X is a don't care bit).

The 2 chip select bits must correspond to the 2 chip select inputs for proper chip selection. By this means, up to 4 identical chips can be connected on the same SDA / SCL lines, in order to form a memory bank of up to 8 KBits.

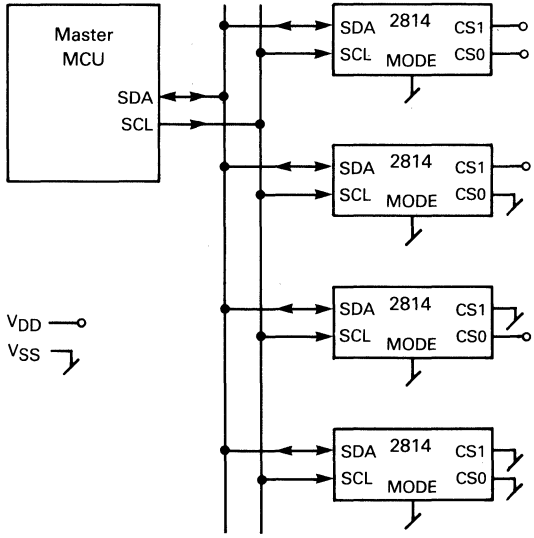
READ/WRITE BIT : The 8th bit transmitted by the master after the 7 bit chip address will indicate the direction of transfer for the next bytes. (Until a new start or stop). If low, the following bytes are transmitted by the master. If high, the following bytes are transmitted by the MCM 2814.

BYTE ADDRESS : The first byte of data received by the memory after the chip address, will be latched in the byte address register and is used to select one of the 256 EEPROM bytes.

ACKNOWLEDGE BIT : This bit is sent by the selected receiver on the data line after a byte reception. Due to the open drain structure, a valid acknowledge bit corresponds to a low level. While operating as a transmitter, sending a sequence of data bits, this device will check the acknowledge bit generated by the master. The absence of this bit will stop the transmission of data.

3.3 Chip Selection

The 2 chip select bits transmitted in the chip address must match the status of CS1 and CS0 inputs.



Pin Status			Chip Address Transmitted
Mode	CS1	CS0	
0	1	1	1010 X11
0	1	0	1010 X10
0	0	1	1010 X01
0	0	0	1010 X00

X = Don't care

Figure 4 M-bus Chip Selection

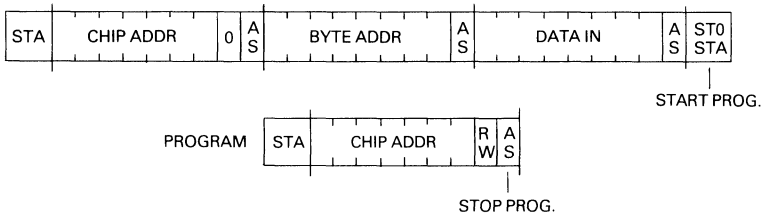
3.4 Protocol

At the protocol level, the transmission of data is defined in the form of sequences of Start (STA), Stop (STO) conditions, and bytes followed by acknowledge bits.

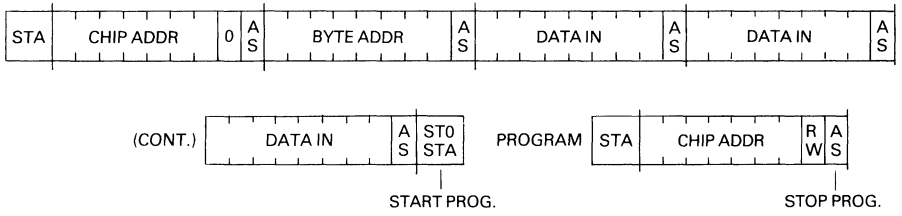
3.4.1 Standby State

When no serial transmission and no programming are made, the circuit is in standby. A STOP condition following a read sequence or a write byte address sequence (without data write), will put the circuit in standby. A new START condition will wake up the device, to get the chip address. If the chip address is not valid, the device will return in standby.
The power consumption is minimum in standby.

Write One Byte



Write up to 4 Bytes



STA: Start Condition
STO: Stop Condition
R/W BIT: 1 = Read/0 = Write
INC: Increment Byte Address
AS: Slave Acknowledge (2814)
AM: Master Acknowledge

Figure 5 M-bus Write Protocol

3.4.2 Write Sequence

The serial write to the memory includes a serial transmission of the byte address and the data to be written. When this is completed by a stop or a new start condition, the programming sequence is initiated.

Programming is under control of the master. It is initiated by the write sequence just described, and stopped by any new valid selection of the chip.
Therefore, the t_{PROG} time is defined as the time between these two operations, and is defined by the master.

Bad chip addresses or chip addresses for other chips on the same bus do not suspend the programming.

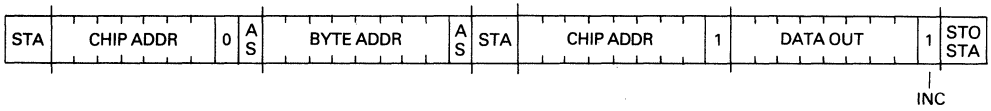
The on-chip V_{PP} generator is automatically turned on or off when needed. If an external V_{PP} is applied, the programming voltage is only allowed into the array during the above defined t_{PROG} time.

It is possible to program simultaneously up to 4 bytes, provided the 6 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.

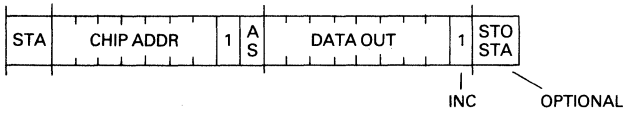
3.4.3 Read Sequence

Reading data from the memory is made in two steps. First the byte address must be loaded in the byte address register. Then data can be read out of the memory. The first step is only required to define the byte address. If this address was predefined from a previous read this step can be skipped.
The byte address is automatically incremented after each data byte transmitted.
This is also valid after the last byte of a transmission.
Therefore, the next read sequence without any byte address specified, will transmit data of the next byte. A read sequence will transmit data bytes of successive addresses until the absence of the acknowledge bit from the master. In this case the SDA output driver will switch off and the circuit will go to standby.

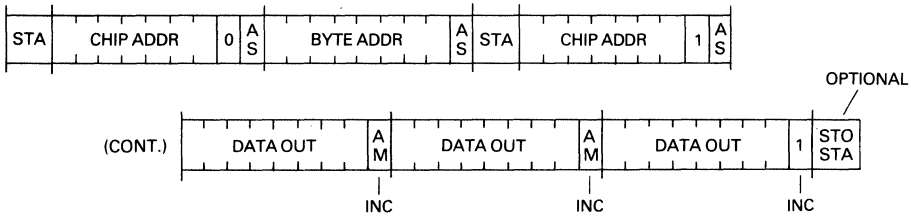
Read One Byte. (Inc. Write Byte Address)



Read One More Byte. (Byte Address Defined)



Read Many Bytes



STA: Start Condition R/W BIT: 1 = Read/0 = Write AS: Slave Acknowledge (2814)
STO: Stop Condition INC: Increment Byte Address AM: Master Acknowledge

Figure 6 M-bus Read Protocol

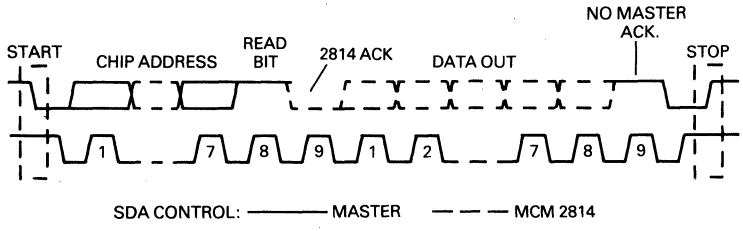


Figure 7 M-bus Read Detail

3.4.4 Signal Levels

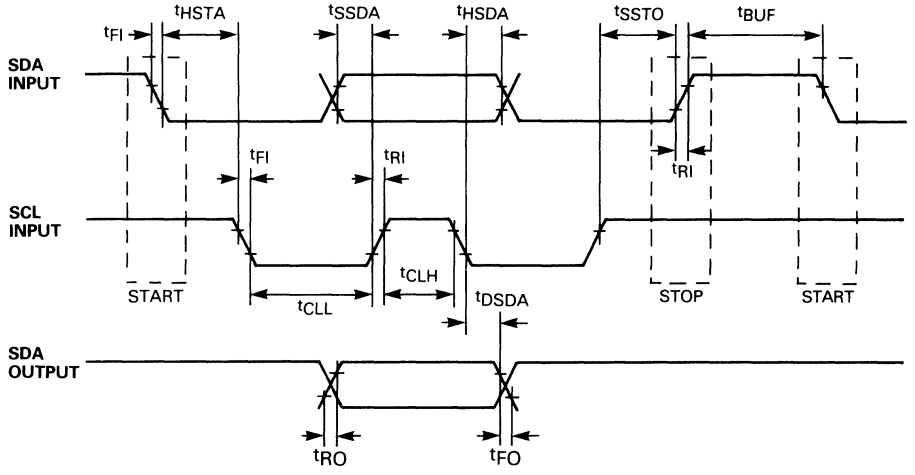


Figure 8 M-bus Timings

Electrical and switching characteristics are described in Section 5.
During a transmission, SDA line transitions must occur when SCL is low. A negative transition of SDA with SCL high is recognised as a START condition, the positive transition as a STOP condition.

The acknowledge bit is provided by the device receiving data. Therefore, during this time the data transmitter must leave the SDA line at high impedance.
As this memory has an open drain SDA output, an external pull-up resistor to V_{DD} should be included on SDA line.

SECTION 4. SPI OPERATING MODE

The serial transmission of this mode requires 4 wires to control the device operation. It features:

- Multiple chips on same 3 wire bus with separate chip select lines.
- SPISS chip selection.
- SPICK clock line, Input only.
- SPISI line used as Input only.
- SPISO line used as Output only.
- No acknowledge bit.
- Programming under control of the master via serial opcodes.
- Programming time under external control.
- Write inhibit after reset.
- Write enable/disable via serial opcodes.
- Byte address output for transparency.

This SPI mode can be used with the SPI of Motorola Microprocessor MC6805S2/S3, MC6805K2/L3/L8, MC68HC05C4 and MC68HC11.

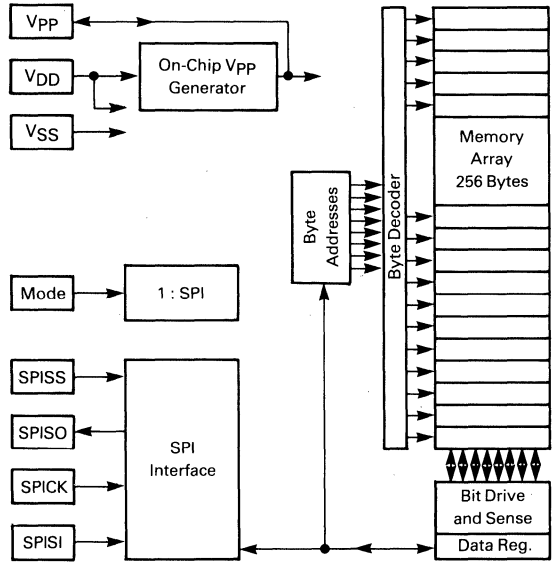


Figure 9 SPI Block Diagram

6

4.1 SPI Serial Interface

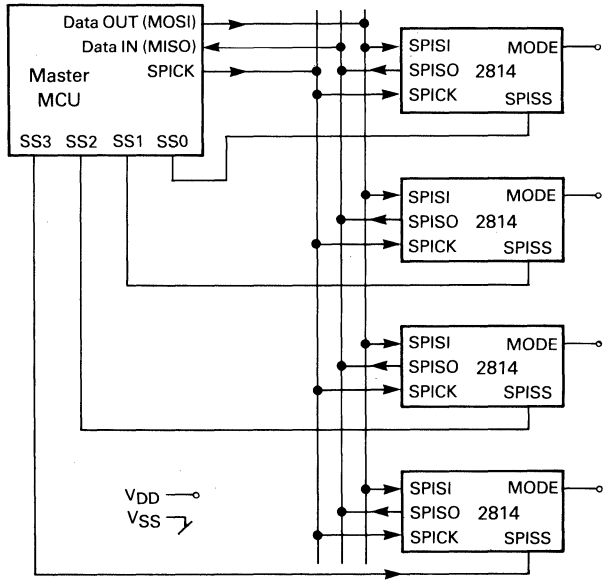


Figure 10 SPI Chip Selection

The serial interface via pins SPICL, SPISI and SPISO is compatible with the SPI standard when the MODE pin is high.

4.2 Lexicon

This lexicon will describe some terms used in this serial interface description.

MASTER : The device that generates the serial clock on SPICK is designated as master. This memory can never function as a master.

SLAVE : This memory always operate as a slave as the SPICK pin is always an input.

TRANSMITTER / RECEIVER : This device has separate pins for data transmission (SPISO) and reception (SPISI). Simultaneous data input and output can therefore occur when the chip is selected with SPISS and is clocked (SPICK).

MSB : The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT : The chip is selected when pin SPISS is low. When the chip is not selected, no data will be input from pin SPISI, and output pin SPISO is high impedance.

4.3 Serial Op-Code

The first byte transmitted after the chip is selected with SPISS going low, contains the opcode that defines the operation to be performed.

Data Transmitted	Operation
1010 0111	Read byte address followed by data.
1010 0110	Program enable. Vpp generator ON.
1010 0100	Program disable. Vpp generator OFF.
1010 0010	Write (Program) data.

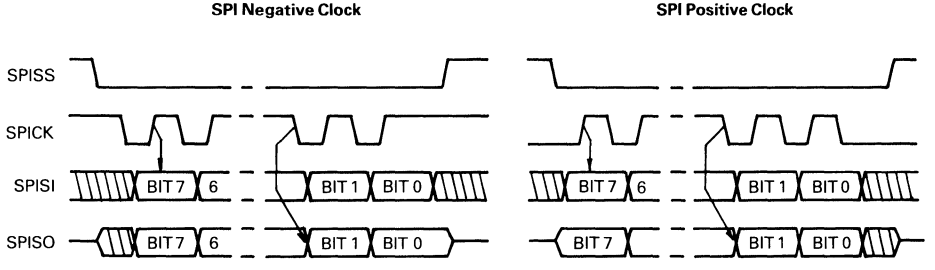
Table 2 SPI Opcodes

All other codes are invalid. After an invalid code is received, no data is shifted in the MCM 2814 and the SPISO data output is high impedance until a new SPISS falling edge re-initialises the serial communication.

4.4 Protocol

The MCM2814 SPI interface accepts both a negative or positive clock.
The SPI protocol for this device defines the bytes transmitted on the SPISI and SPISO data lines for proper chip operation.

6



Positive Clock Edge: Shift IN
Negative Clock Edge: Data OUT

Figure 11 SPI Clock Phase and Polarity

4.5 Standby State

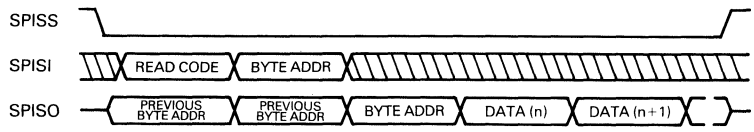
The circuit is in standby when no serial transmission takes place, when no write is waiting for the Vpp enable command and when the Vpp generator is off.
When SPISS is high, standby state will follow:

- A power up reset.
- A Vpp disable command.
- A Read, providing no Vpp enable command has been issued previously.

The power consumption is minimum in standby.

4.6 Read Sequence

Read One or More Bytes



Invalid Opcodes

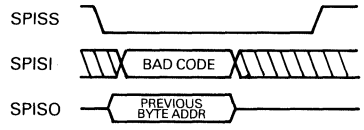


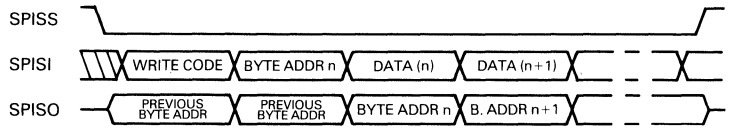
Figure 12 SPI Read

Reading the memory via the serial SPI link requires the following sequence. The SPISS line is pulled low to select the device. The read opcode is transmitted on the SPISI line followed by the byte address. When this is done, data on the SPISI line has no more influence on the memory. At the beginning of an SPI transaction, the SPISO buffer is turned on and will shift out the current byte address. This can be used for a relative addressing of the byte address. The new byte address is then transmitted followed by corresponding data. If just one byte is read, SPISS can be pulled back to the high level. It is possible to continue the read sequence, as the byte address is automatically incremented. The byte address is shifted out only once, in the beginning of a transmission.

6

4.7 Program Sequence

Write One to Four Bytes



V_{PP} Enable/Disable

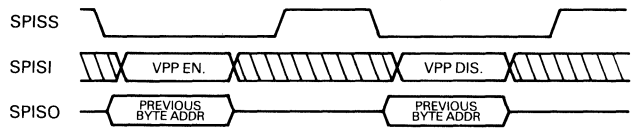


Figure 13 SPI Program

To program a byte, two separate conditions must be simultaneously present. The program must be enabled via the V_{PP} enable command, and a serial write must be done. The V_{PP} enable will also turn on the on-chip V_{PP} generator. At this time, the chip is obviously not in standby, even if SPISS is high. The program disable command will stop the on-chip V_{PP} supply and protect the EEPROM data against unwanted modifications. An external V_{PP} supply will also be internally enabled or disabled by this mechanism.

A write serial sequence includes an SPISS high to low transition, followed by the write code on the SPISI line. The byte address followed by the corresponding data to be written are then shifted through the SPISI pin. At the

beginning of an SPI transaction, the SPISO buffer is turned on and will shift out the current byte address. This can be used for a relative addressing of the byte to be programmed. The new byte address is also echoed for possible checking by the master. If Vpp is enabled, the programming will start after the SPISS line goes back to a high level. It is also possible to issue the Vpp enable command after the write sequence.
If the Vpp enable command is issued after the serial write, no Read or invalid code should be transmitted in between as this would clear the programming latch containing the data to be programmed.
The programming is suspended when a new chip selection with SPISS low occurs. It is then possible to send a new write command to program new data. A Vpp enable or a Read command will stop the programming.

It is possible to program simultaneously up to 4 bytes, provided the 6 most significant bits of their addresses are identical. The byte address is incremented after each new data byte shifted in.

4.8 Signal Levels

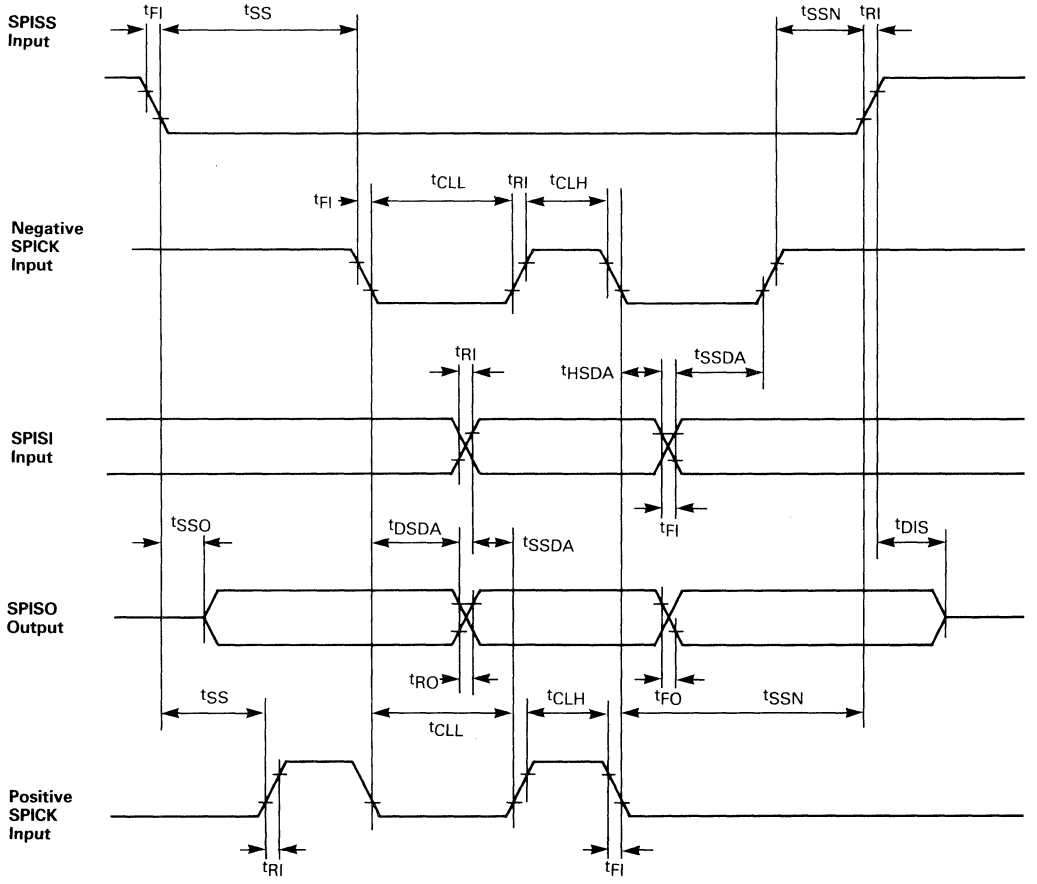


Figure 14 SPI Timings

Electrical and switching characteristics are described in **Section 5**.

SECTION 5. CHARACTERISTICS

V_{SS} = 0 V

5.1 Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +7.0	Vdc
Input voltage pins 1, 3, 5, 6	V_{in}	−0.3 to +7.0	Vdc
Input voltage pin 2	V_{in}	−0.3 to V_{DD} +0.3	Vdc
Current on any Input	I_{in}	0.1	mA
Sink current SDA	ISDAL	10	mA
Sink current SPISO	ISOL	10	mA
Source current SPISO	ISOH	10	mA
Operating temperature	T_A	0 to 70*	°C
Storage temperature	T_S	−55 to 125**	°C
Junction Temperature	T_j	150**	°C
Thermal resistance	Th_{ja}	200	°C/W

*Specification over the temperature range, −40 to +85°C to be determined.

6

Stresses above those listed under 'Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum operating conditions for extended periods may affect reliability.

**In particular, continuous high temperature application may cause leakage of stored charge in EEPROM, resulting in data loss.

5.2 Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage STANDBY	V_{DDS}	-	-	6.0	Vdc
Supply current STANDBY*	I_{DDS}	-	1	TBD	μA
Supply voltage READ	V_{DDR}	3.0	-	6.0	Vdc
Supply current READ*	I_{DDR}	-	0.3	1.5	mA
Supply voltage PROG	V_{DDP}	4.5**	-	6.0	Vdc
Supply current PROG*	I_{DDP}	-	0.5	3.0	mA

*Inputs at V_{SS} or V_{DD}.
**Programmability at 3 V V_{DDP} (min) is still to be determined.

5.3 Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
SCL, SDA, SPISS, SPISI Inputs					
Input low voltage	V_{IL}	−0.3	-	$0.3*V_{DD}$	Vdc
Input high voltage	V_{IH}	$0.7*V_{DD}$	-	$V_{DD}+0.3$	Vdc
Input leakage	I_{IN}	-	-	±10	μA
SDA/SPISO Pull down Outputs					
Output low I_{OL} <10μA	V_{OL}	-	-	0.1	Vdc
Output high leakage	I_{OH}	-	-	±10	μA
Output low I_{OL} = 3 mA V_{DD} = 5 V	V_{OL}	-	-	0.4	Vdc
Output low I_{OL} = 1 mA V_{DD} = 3 V	V_{OL}	-	-	0.4	Vdc
SPISO Pull up Output					
Output high I_{OH} = 1.6 mA V_{DD} = 5 V	V_{OH}	$V_{DD}-0.8$	-	-	Vdc
Output high I_{OH} = 0.4 mA V_{DD} = 3 V	V_{OH}	$V_{DD}-0.3$	-	-	Vdc
MODE, CS1, CS0 Inputs					
Input low voltage	V_{ILV}	−0.3	-	$0.3*V_{DD}$	Vdc
Input high voltage	V_{IH}	$0.7*V_{DD}$	-	$V_{DD}+0.3$	Vdc
Input leakage	I_{IN}	-	-	±10	μA
Input capacitance	C_{IN}	-	10	-	pF

5.4 SWITCHING PARAMETERS

5.4.1 General

Characteristic	Symbol	Min	Typ	Max	Unit
Programming time 1 byte	t_{PROG}	10	-	t_{BD}	mS
Programming time 4 bytes	t_{PROG}	20	-	t_{BD}	mS

5.4.2 Serial Bus Input

Characteristic	Symbol	Min	Typ	Max	Unit
SDA/SPISI, SCL/SPICK, SPISS Inputs					
Clock frequency	F_{SCL}	0.0	-	125	kHz
Clock High time	t_{CLH}	4.0	-	-	µS
Clock Low time	t_{CLL}	4.0	-	-	µS
Stop to Start delay	t_{BUF}	4.0	-	-	µS
Start hold time	t_{HSTA}	4.0	-	-	µS
Data hold time	t_{HSDA}	0.0	-	-	µS
Data set-up time	t_{SSDA}	250	-	-	nS
Input Rise time	t_{RI}	-	-	1.0	µS
Input Fall time	t_{FI}	-	-	300	nS
Stop set-up time	t_{SSTO}	4.0	-	-	µS
SPISS Lead time	t_{SS}	4.0	-	-	µS
SPISS Lag time	t_{SSN}	4.0	-	-	µS

All values refer to V_{IH} and V_{IL} levels.

5.4.3 Serial Bus Output

V_{DD} = 5 Vdc ±10%. T_A = 0 to 70°C. C_L = 200 pF.

Characteristic	Symbol	Min	Typ	Max	Unit
SDA/SPISO Outputs					
Data delay	t_{DSDA}	-	1.5	3.5	µS
Rise time SDA	t_{RO}	-	-	*	nS
Rise time SPISO	t_{RO}	-	-	100	nS
Fall time	t_{FO}	-	-	100	nS
SPI select time	t_{SSO}	-	-	1.2	µS
Disable time	t_{DIS}	-	1.5	3.5	µS

V_{DD} = 3.3 Vdc ± 10%. T_A = 0 to 70°C. C_L = 200 pF.

Characteristic	Symbol	Min	Typ	Max	Unit
SDA/SPISO Outputs					
Data delay	t_{DSDA}	-	2.0	3.5	µS
Rise time SDA	t_{RO}	-	-	*	nS
Rise time SPISO	t_{RO}	-	-	200	nS
Fall time	t_{FO}	-	-	200	nS
SPI select time	t_{SSO}	-	-	1.5	µS
Disable time	t_{DIS}	-	2.0	3.5	µS

All values referred to V_{IH} and V_{IL} levels.
*Depends on external pull-up resistor value.

MECL RAMs 7

MECL RAMs

(0 to 75°C)

Organization	Part Number	Access Time (ns max)	Pins
8 × 2	MCM10143	15.3	24
16 × 4	MCM10145	15	16
16 × 4	MC10H145	6	16
64 × 1	MCM10148	15	16
128 × 1	MCM10147	15	16
256 × 1	MCM10144	26	16
256 × 1	MCM10152	15	16
1024 × 1	MCM10146	29	16
1024 × 1	MCM10415-15	15	16
1024 × 1	MCM10415-20	20	16

MC10H145

Advance Information

MECL 10KH

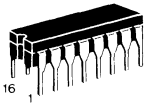
16 × 4 BIT REGISTER FILE

MECL 10KH HIGH-SPEED EMITTER-COUPLED LOGIC

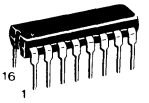
The MC10H145 is a 16 x 4 bit register file. The active-low chip select allows easy expansion.

The operating mode of the register file is controlled by the $\overline{WE}$ input. When $\overline{WE}$ is "low" the device is in the write mode, the outputs are "low" and the data present at D_n input is stored at the selected address, when $\overline{WE}$ is "high," the device is in the read mode — the data state at the selected location is present at the Q_n outputs.

- Address Access Time, 3.5 ns Typical
- Power Dissipation, 700 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

FN SUFFIX
PLCC
CASE 775

MAXIMUM RATINGS

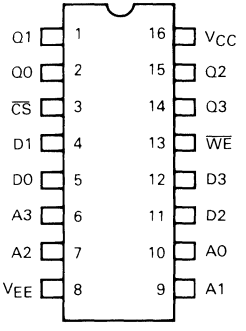
Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	-8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	-55 to +150 -55 to +165	°C

ELECTRICAL CHARACTERISTICS (V_{EE} = -5.2 V ± 5%) (See Note)

Characteristic	Symbol	0°		25°		75°		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Current	I_E	—	165	—	150	—	165	mA
Input Current High	I_{inH}	—	375	—	220	—	220	μA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	μA
High Output Voltage	V_{OH}	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
Low Output Voltage	V_{OL}	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
High Input Voltage	V_{IH}	-1.17	-0.84	-1.13	-0.81	-1.07	-0.735	Vdc
Low Input Voltage	V_{IL}	-1.95	-1.48	-1.95	-1.48	-1.95	-1.45	Vdc

NOTE:
Each MECL 10KH series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

PIN ASSIGNMENT



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care

Q-State of Addressed Cell

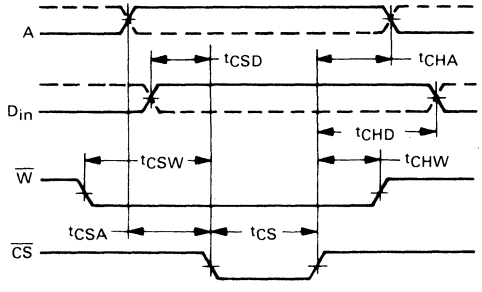
AC PARAMETERS

Characteristics	Symbol	MC10H145 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ±5% Min	Max	Unit	Conditions
Read Mode				ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	0	3.0		
Chip Select Recovery Time	t_{RCS}	0	3.0		
Address Access Time	t_{AA}	0	6.0		
Write Mode				ns	t_{WSA} = 3.5 ns
Write Pulse Width	t_W	6.0	—		Measured at 50% of input to 50% of output. t_W = 4.0 ns.
Data Setup Time Prior to Write	t_{WSD}	0	—		
Data Hold Time After Write	t_{WHD}	1.5	—		
Address Setup Time Prior to Write	t_{WSA}	3.5	—		
Address Hold Time After Write	t_{WHA}	1.5	—		
Chip Select Setup Time Prior to Write	t_{WSCS}	0	—		
Chip Select Hold Time After Write	t_{WHCS}	1.5	—		
Write Disable Time	t_{WS}	1.0	4.0		
Write Recovery Time	t_{WR}	1.0	4.0		
Chip Enable Strobe Mode				ns	Guaranteed but not tested on standard product. See Figure 1.
Data Setup Prior to Chip Select	t_{CSD}	0	—		
Write Enable Setup Prior to Chip Select	t_{CSW}	0	—		
Address Setup Prior to Chip Select	t_{CSA}	0	—		
Data Hold Time After Chip Select	t_{CHD}	1.0	—		
Write Enable Hold Time After Chip Select	t_{CHW}	0	—		
Address Hold Time After Chip Select	t_{CHA}	2.0	—		
Chip Select Minimum Pulse Width	t_{CS}	4.0	—		
Rise and Fall Time	t_r, t_f			ns	Measured between 20% and 80% points.
Address to Output		0.6	2.5		
CS to Output		0.6	2.5		
Capacitance				pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	6.0		
Output Capacitance	C_{out}	—	8.0		

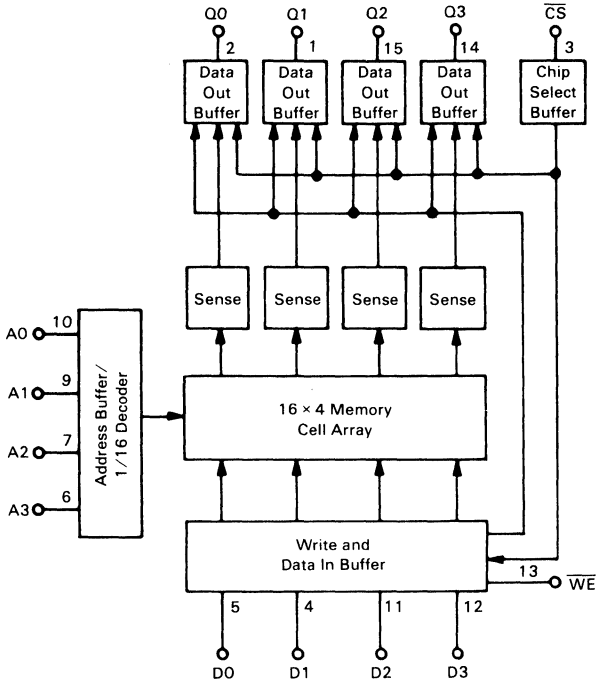
NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MC10H145. $C_L \leq$ 5.0 pF (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
3. For proper use of MECL in a system environment, consult MECL System Design Handbook.

7

FIGURE 1 — CHIP ENABLE STROBE MODE



16 × 4 Bit Register File

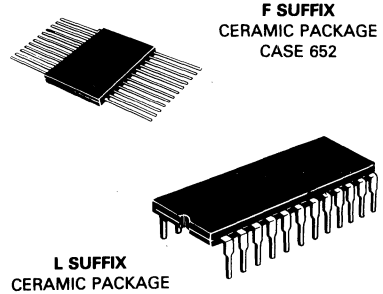


7

MCM10143

MECL

8 x 2 MULTIPORT REGISTER FILE (RAM)



F SUFFIX
CERAMIC PACKAGE
CASE 652

L SUFFIX
CERAMIC PACKAGE
CASE 623

8 x 2 MULTIPORT REGISTER FILE (RAM)

The MC10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE

A write occurs on the positive to negative transition of the clock. Data is enabled by having the write enable (of each bit to be written) low when the clock transition is made. The written information is seen at the output on the negative to positive clock transition provided the read enable (of each bit) is at a low level. To inhibit a bit from being written, the write enable of that bit must be at a high level when the clock goes to a low state and must remain high until clock goes high. The operation of the clock and write enables can be reversed. While the clock is low, a positive to negative transition of the write enable will write into the bit addressed by A_0–A_2. The data is seen at the output on the negative to positive transition of the clock, provided the read enable is low.

READ

When the clock is high any two words may be read out simultaneously, as selected by addresses B_0–B_2 and C_0–C_2, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates (B_0–B_1), (C_0–C_1).

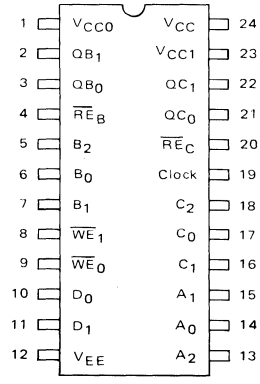
t_{pd}:
CLock to Data out = 5 ns (typ)
(Read Selected)
Address to Data out = 10 ns (typ)
(Clock High)
$\overline{\text{Read Enable}}$ to Data out = 2.8 ns (typ)
(Clock high, Addresses present)
P_D = 610 mW/pkg (typ no load)

TRUTH TABLE

*MODE	INPUT							OUTPUT			
	**Clock	$\overline{WE}_0$	$\overline{WE}_1$	D_0	D_1	$\overline{RE}_B$	$\overline{RE}_C$	QB_0	QB_1	QC_0	QC_1
Write	L→H	L	L	H	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	H→L	ϕ	ϕ	ϕ	ϕ	L	L	H	H	H	H
Read	L→H→L	H	H	ϕ	ϕ	L	L	H	H	H	H
Write	L→H	L	L	L	H	H	H	L	L	L	L
Read	H	ϕ	ϕ	ϕ	ϕ	L	L	L	H	L	H

**Note: Clock occurs sequentially through Truth Table
*Note: A0-A2, B0-B2, and C0-C2 are all set to same address location throughout Table.
ϕ = Don't Care

PIN ASSIGNMENT



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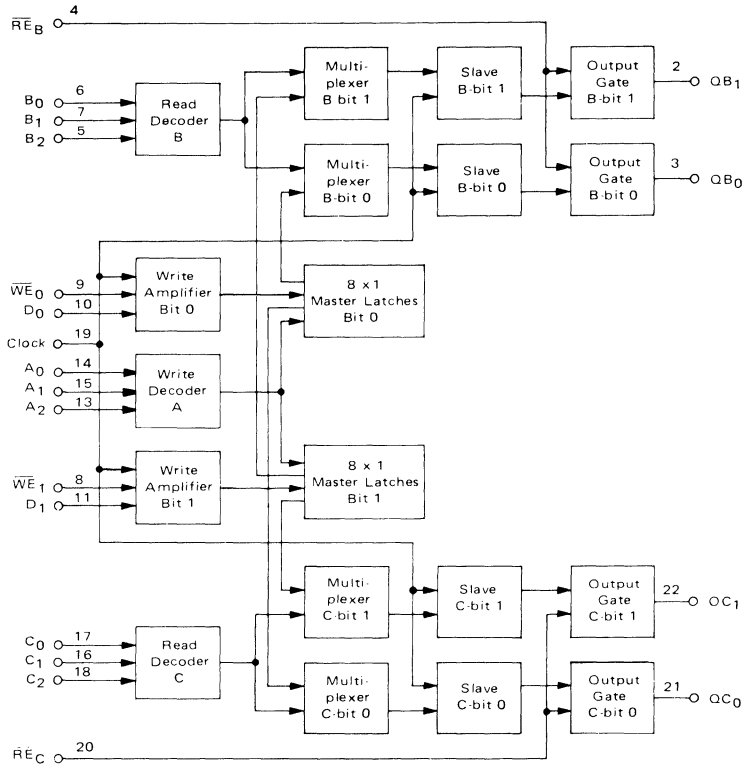
BLOCK DIAGRAM



7

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

ELECTRICAL CHARACTERISTICS

Test Temperature	DC TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = −5.2 Vdc ± 5%)

Characteristics	Symbol	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit
Power Supply Drain Current	I_E	–	150	–	118	150	–	150	mAdc
Input Current	I_{inH}								μAdc
Pins 10, 11, 19		–	245	–	–	245	–	245	
All other pins		–	200	–	–	200	–	200	
Switching Times ①									ns
Read Mode									
Address Input	$t_{B\pm QB\pm}$	4.0	15.3	4.5	10	14.5	4.5	15.5	
Read Enable	$t_{\overline{RE}-QB+}$	1.1	5.3	1.2	3.5	5.0	1.2	5.5	
Data	$t_{Clock+QB-}$	1.7	7.3	2.0	5.0	7.0	2.0	7.6	
Setup									
Address	$t_{setup(B-Clock-)}$	–	–	8.5	5.5	–	–	–	
Hold									
Address	$t_{hold(Clock-B+)}$	–	–	-1.5	-4.5	–	–	–	
Write Mode									
Setup									
Write Enable	$t_{setup(\overline{WE}-Clock+)}$	–	–	7.0	4.0	–	–	–	
Write Disable	$t_{setup(\overline{WE}+Clock-)}$	–	–	1.0	-2.0	–	–	–	
Address	$t_{setup(A-Clock+)}$	–	–	8.0	5.0	–	–	–	
Data	$t_{setup(D-Clock+)}$	–	–	5.0	2.0	–	–	–	
Hold									
Write Enable	$t_{hold(Clock-\overline{WE}+)}$	–	–	5.5	2.5	–	–	–	
Write Disable	$t_{hold(Clock+\overline{WE}-)}$	–	–	1.0	-2.0	–	–	–	
Address	$t_{hold(Clock+A+)}$	–	–	1.0	-3.0	–	–	–	
Data	$t_{hold(Clock+D+)}$	–	–	1.0	-2.0	–	–	–	
Write Pulse Width	$PW_{\overline{WE}}$	–	–	8.0	5.0	–	–	–	
Rise Time, Fall Time (20% to 80%)	t_r, t_f	1.1	4.2	1.1	2.5	4.0	1.1	4.5	

① AC timing figures do not show all the necessary presetting conditions.

READ TIMING DIAGRAMS

Access (Clock High)

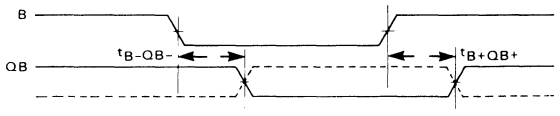


FIGURE 1

Enable

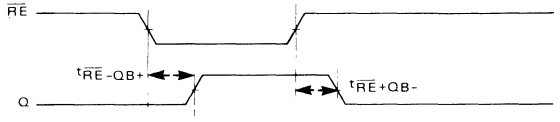


FIGURE 2

Data
(Address Selected)

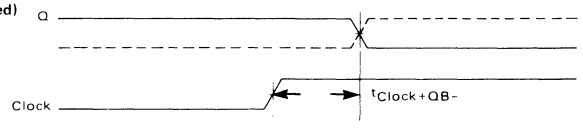


FIGURE 3

Setup and Hold

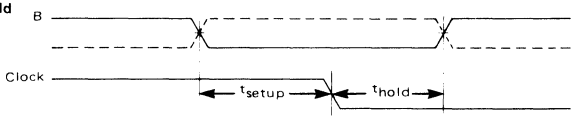


FIGURE 4

WRITE TIMING DIAGRAM

Enable Setup

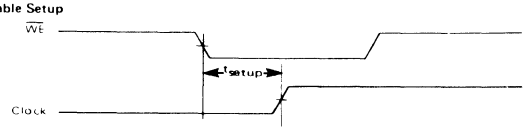


FIGURE 5

Enable Hold

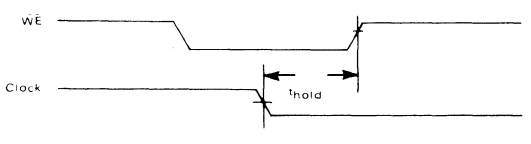


FIGURE 6

Disable

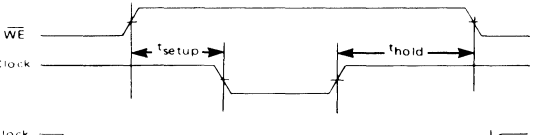


FIGURE 7

Pulse Width

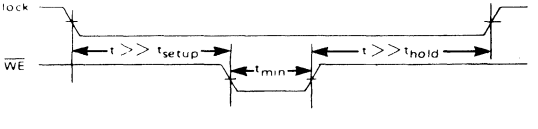


FIGURE 8

Address

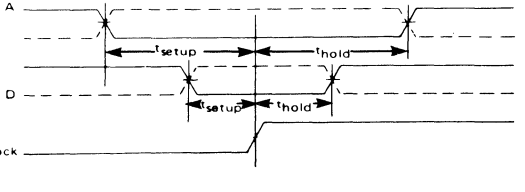


FIGURE 9

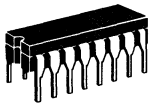
7

MCM10144

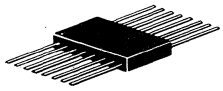
256 x 1-BIT RANDOM ACCESS MEMORY

The MCM10144 is a 256 word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of an 8-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 3 active-low chip select lines. It has a typical access time of 17 ns and is designed for high-speed scratch pad, control, cache, and buffer storage applications.

- Typical Address Access Time = 17 ns
- Typical Chip Select Access Time = 4.0 ns
- Operating Temperature Range = 0° to +75°C
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on Chip Select
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family
- Pin-for-Pin Replacement for F10410



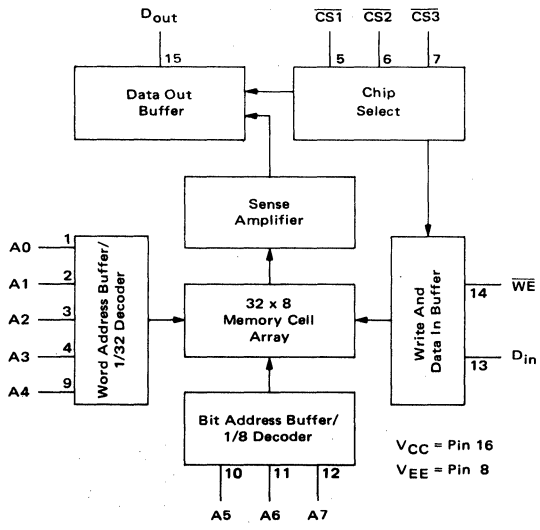
L SUFFIX
CERAMIC PACKAGE
CASE 620



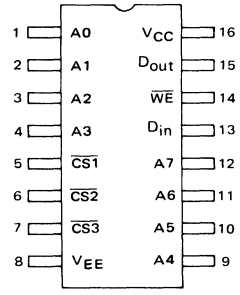
F SUFFIX
CERAMIC PACKAGE
CASE 650

7

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A7	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM10144 is a 256 word x 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 thru A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

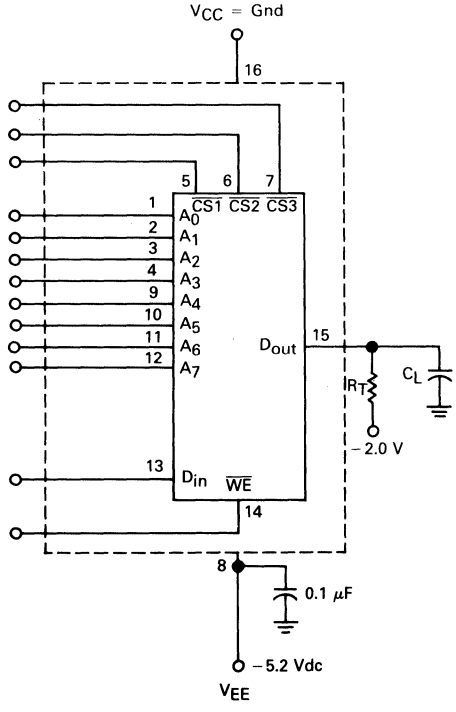
		MCM10144 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	130	–	125	–	120	mAdc	Typ I_{EE} @ 25°C = 90 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

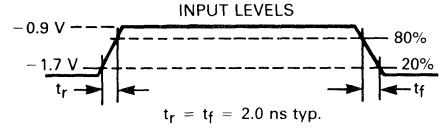
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	10	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	4.0	10	ns	output. See Note 2.
Address Access Time	t_{AA}	7.0	17	26	ns	
Write Mode						
Write Pulse Width	t_W	25	6.0	–	ns	t_{WSA} = 8.0 ns
Data Setup Time Prior to Write	t_{WSD}	2.0	-3.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	2.0	-3.0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	8.0	0	–	ns	t_W = 25 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	0.0	-4.0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	-3.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	2.0	-3.0	–	ns	
Write Disable Time	t_{WS}	2.5	5.0	10	ns	
Write Recovery Time	t_{WR}	2.5	5.0	10	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	7.0	ns	When driven from Address inputs.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF

FIGURE 2 – CHIP SELECT ACCESS TIME

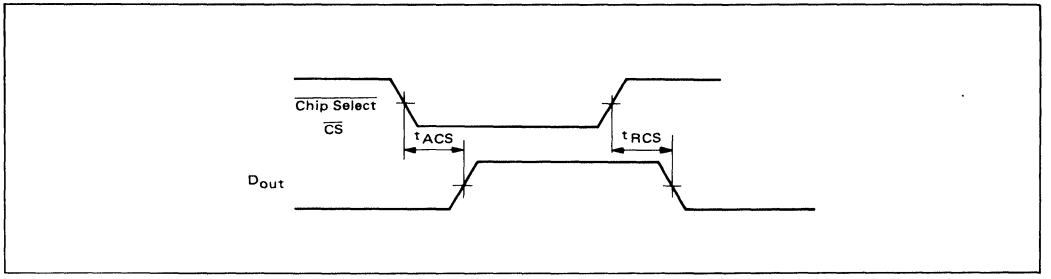


FIGURE 3 – ADDRESS ACCESS TIME

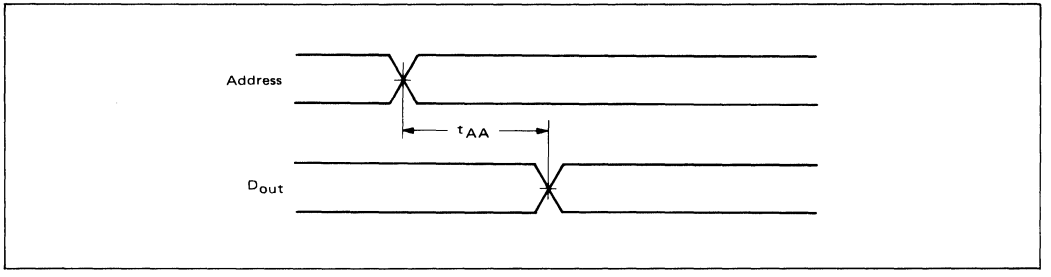
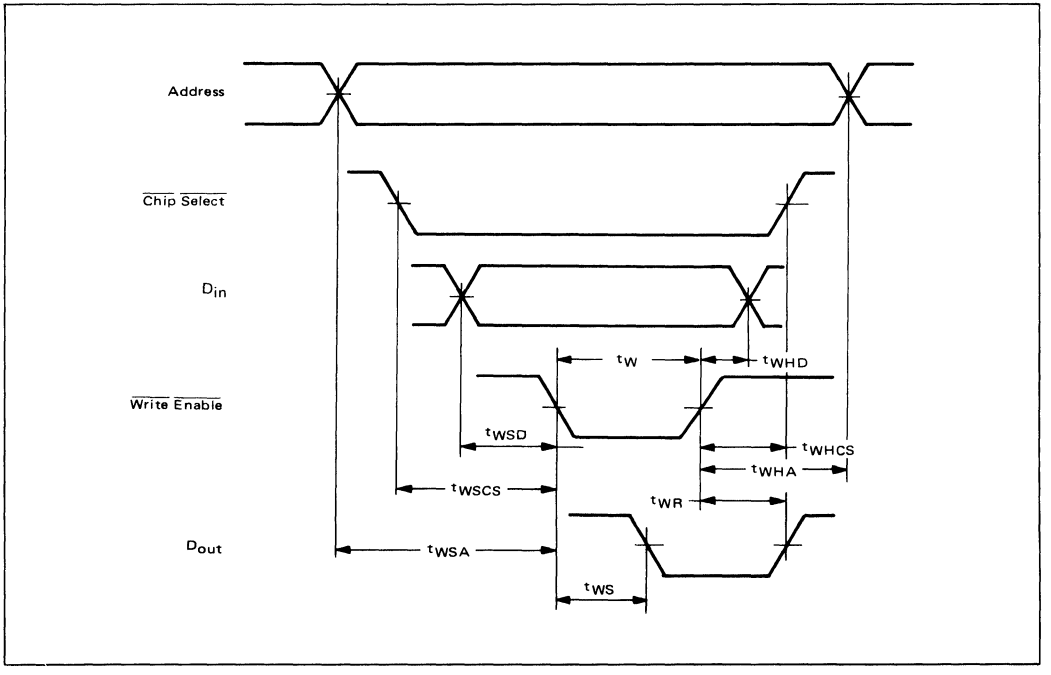


FIGURE 4 – WRITE MODE



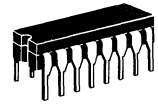
7

MCM10145

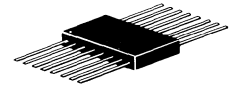
64-BIT REGISTER FILE (RAM)

The MCM10145 is a 64-Bit RAM organized as a 16 x 4 array. This organization and the high speed make the MCM10145 particularly useful in register file or small scratch pad applications. Fully decoded inputs, together with a chip enable, provide expansion of memory capacity. The $\overline{\text{Write Enable}}$ input, when low, allows data to be entered; when high, disables the data inputs. The $\overline{\text{Chip Select}}$ input when low, allows full functional operation of the device; when high, all outputs go to a low logic state. The $\overline{\text{Chip Select}}$, together with open emitter outputs allow full wire-ORing and data bussing capability. On-chip input pulldown resistors allow unused inputs to remain open.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 4.5 ns
- Operating Temperature Range = 0^{o} to $+75^{o}C$
- 50 kΩ Pulldown Resistors on All Inputs
- Fully Compatible with MECL 10,000
- Pin-for-Pin Compatible with the F10145



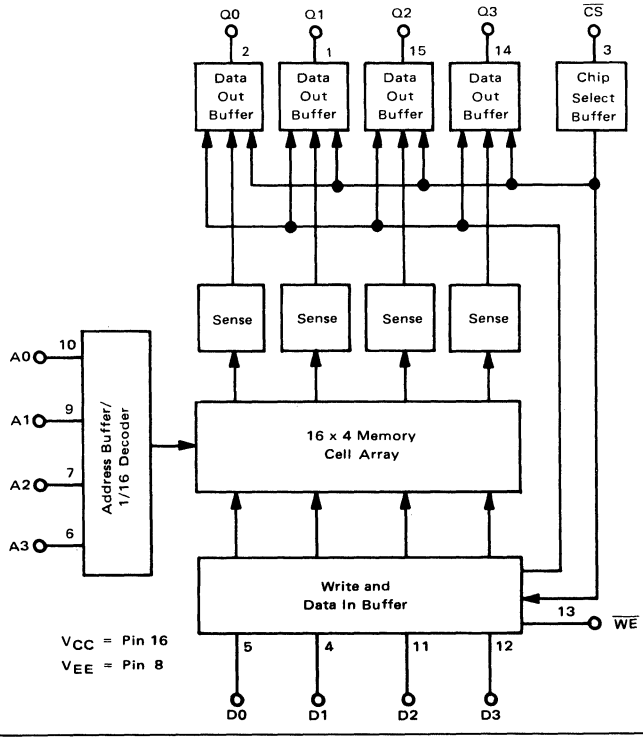
L SUFFIX
CERAMIC PACKAGE
CASE 620



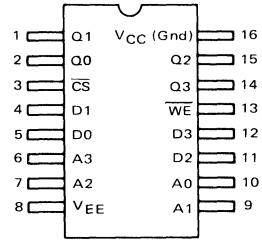
F SUFFIX
CERAMIC PACKAGE
CASE 650

7

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

$\overline{\text{CS}}$	Chip Select Input
A0 thru A3	Address Inputs
D0 thru D3	Data Inputs
Q0 thru Q3	Data Outputs
$\overline{\text{WE}}$	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{\text{CS}}$	$\overline{\text{WE}}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM10145 is a 16 word x 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 thru A3.

The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_n is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Q_n.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

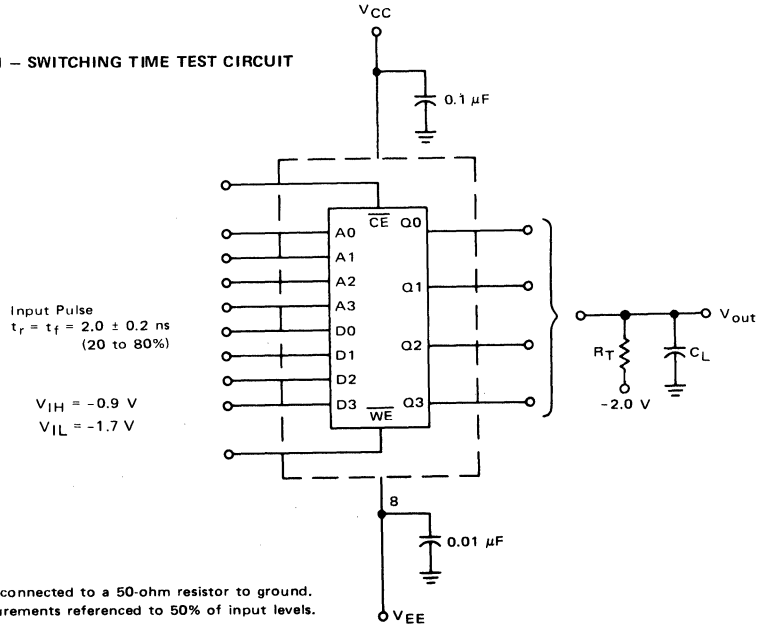
		MCM10145 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	130	–	125	–	120	mAdc	Typ I_{EE} @ 25°C = 90 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = −5.2 Vdc ±5°; Output Load see Figure 1; see Note 2.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.5	8.0	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	5.0	8.0	ns	output. See Note 1.
Address Access Time	t_{AA}	4.0	10	15	ns	
Write Mode						
Write Pulse Width	t_W	8.0	–	–	ns	t_{WSA} = 5 ns
Data Setup Time Prior to Write	t_{WSD}	0	-6.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	3.0	0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	5.0	1.0	–	ns	t_W = 8 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	1.0	-3.0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	0	-5.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	0	-6.0	–	ns	
Write Disable Time	t_{WS}	2.0	5.0	8.0	ns	
Write Recovery Time	t_{WR}	2.0	5.0	8.0	ns	
Chip Enable Strobe Mode						
Data Setup Prior to Chip Select	t_{CSD}	0	-6.0	–	ns	Guaranteed but not tested on standard
Write Enable Setup Prior to Chip Select	t_{CSW}	0	-3.0	–	ns	product. See Figure 5.
Address Setup Prior to Chip Select	t_{CSA}	0	-3.0	–	ns	
Data Hold Time After Chip Select	t_{CHD}	2.0	-1.0	–	ns	
Write Enable Hold Time After Chip Select	t_{CHW}	0	-6.0	–	ns	
Address Hold Time After Chip Select	t_{CHA}	4.0	-1.0	–	ns	
Chip Select Minimum Pulse Width	t_{CS}	18	12	–	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Address to Output	t_r, t_f	1.5	3.0	7.0	ns	
$\overline{CS}$ to Output	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	6.0	pF	
Output Capacitance	C_{out}	–	5.0	8.0	pF	

Notes:
1. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.
2. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

FIGURE 1 – SWITCHING TIME TEST CIRCUIT



Unused outputs connected to a 50-ohm resistor to ground.
All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (Including Jig and Stray Capacitance)
Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.

FIGURE 2 – CHIP SELECT ACCESS TIME

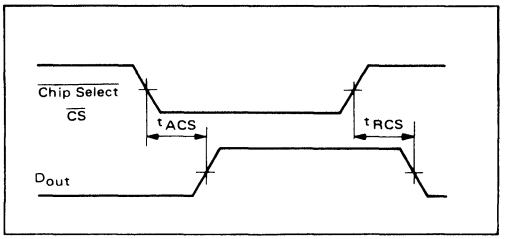


FIGURE 3 – ADDRESS ACCESS TIME

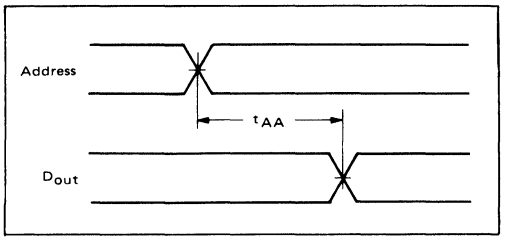


FIGURE 4 – WRITE MODE

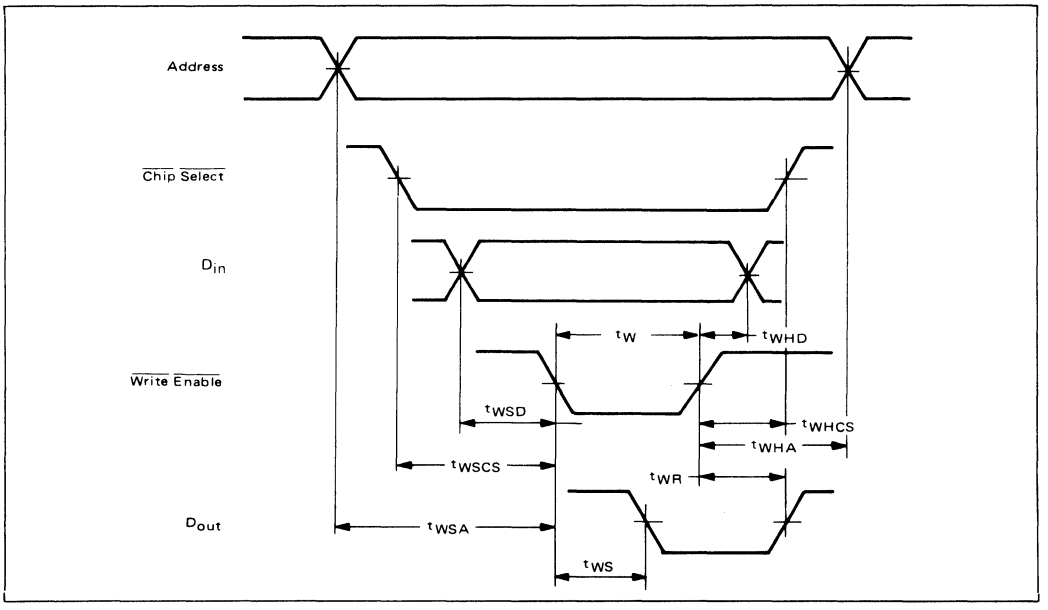
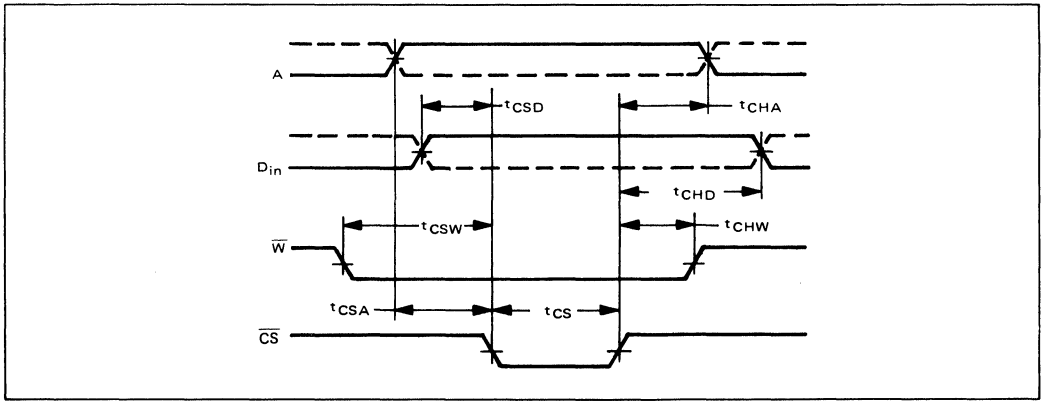


FIGURE 5 – CHIP ENABLE STROBE MODE



7

MCM10146

1024 x 1-BIT RANDOM ACCESS MEMORY

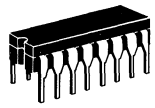
The MCM10146 is a 1024-bit Read/Write Random Access Memory organized 1024 words by 1 bit. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with a separate data in line, a non-inverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

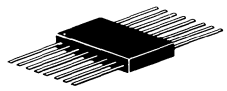
- Fully Compatible with MECL 10,000
- Temperature Range of 0° to 75°C (see note 1)
- Emitter-Follower Output Permits Full Wire-ORing (see note 3)
- Power Dissipation Decreases with Increasing Temperature
- Typical Address Access of 24 ns
- Typical Chip Select Access of 4.0 ns

PIN DESIGNATION

CS	Chip Select Input
A0 to A9	Address Inputs
D_{in}	Data Inputs
D_{out}	Data Output
WE	Write Enable Input



L SUFFIX
CERAMIC PACKAGE
CASE 620

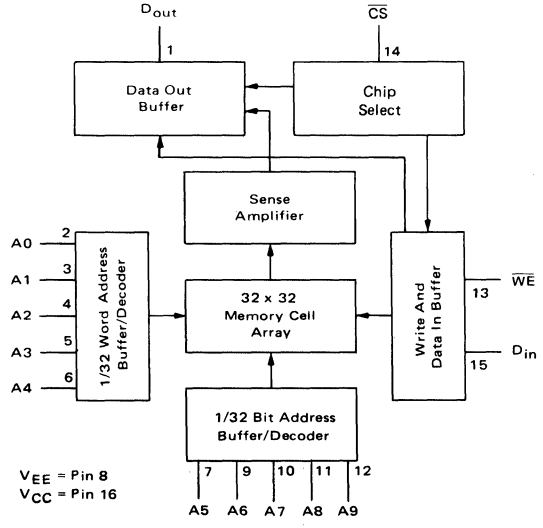


F SUFFIX
CERAMIC PACKAGE
CASE 650

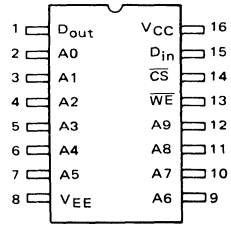
ORDERING INFORMATION

Suffix Denotes
MCM10146 – L Ceramic Dual-in-Line Package
– F Ceramic Flat Package

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

This device is a 1024 x 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM (CS input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table)

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

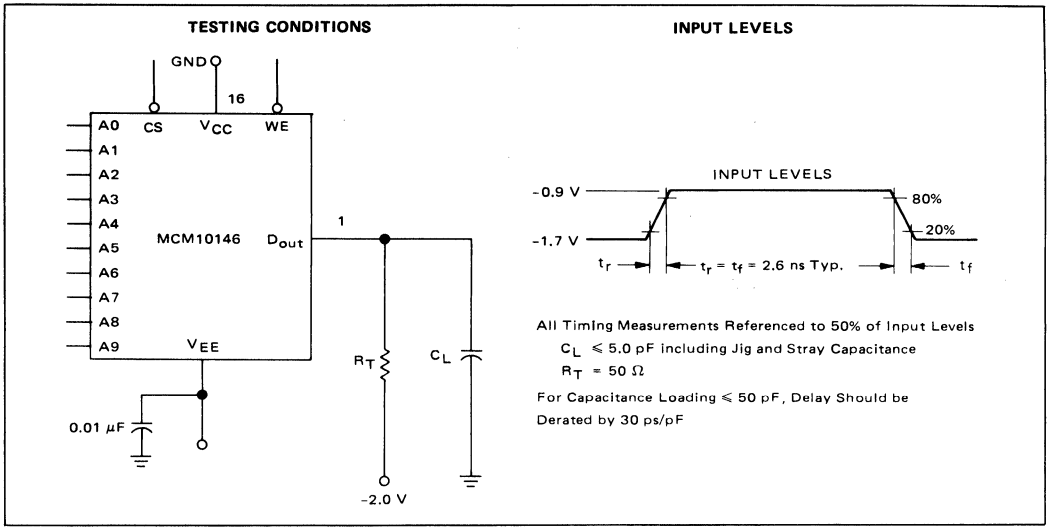
	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

DC Characteristics	Symbol	MCM10146 Test Limits 0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	150	–	145	–	125	mAdc	Typ I_{EE} @ 25°C = 100 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.920	-1.665	-1.900	-1.650	-1.880	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

FIGURE 1 – SWITCHING TEST CIRCUIT AND WAVEFORMS



Guaranteed with V_{EE} = -5.2 Vdc ± 5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10146 Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	7.0	ns	Measured at 50% of input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	4.0	7.0	ns	See Note 2.
Address Access Time	t_{AA}	8.0	24	29	ns	
Write Mode						See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	25	20	–	ns	t_{WSA} = 8.0 ns. Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	5.0	0	–	ns	
Data Hold Time After Write	t_{WHD}	5.0	0	–	ns	
Address Setup Time Prior to Write	t_{WSA}	8.0	0	–	ns	t_W = 25 ns
Address Hold Time After Write	t_{WHA}	2.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	5.0	0	–	ns	
Write Disable Time	t_{WS}	2.8	5.0	7.0	ns	
Write Recovery Time	t_{WR}	2.8	5.0	7.0	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	2.5	4.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Output Rise and Fall Time	t_r, t_f	1.5	4.0	8.0	ns	When driven from Address inputs.
Capacitance						Measured with a pulse technique.
Input Lead Capacitance	C_{in}	–	4.0	5.0	pF	
Output Lead Capacitance	C_{out}	–	7.0	8.0	pF	

Notes:

(1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.

(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

(4) Typical limits are at V_{EE} = -5.2 Vdc, T_A = 25°C and standard loading.

FIGURE 2 – CHIP SELECT ACCESS TIME

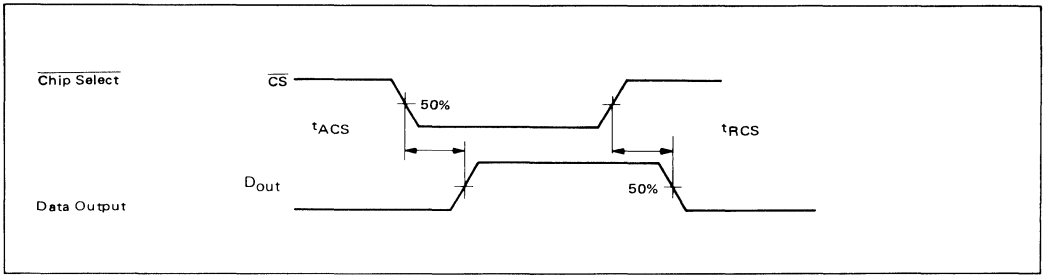


FIGURE 3 – ADDRESS ACCESS TIME

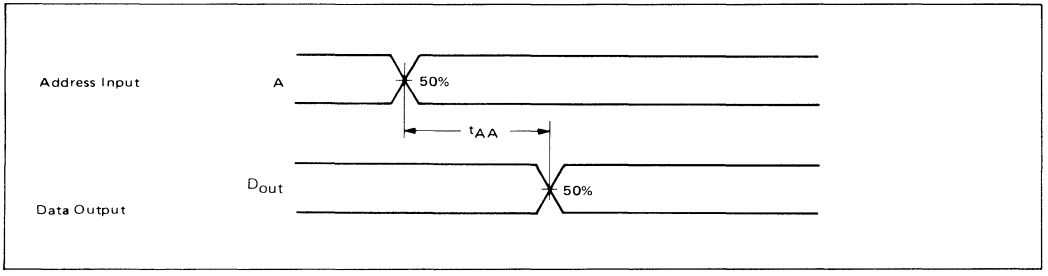
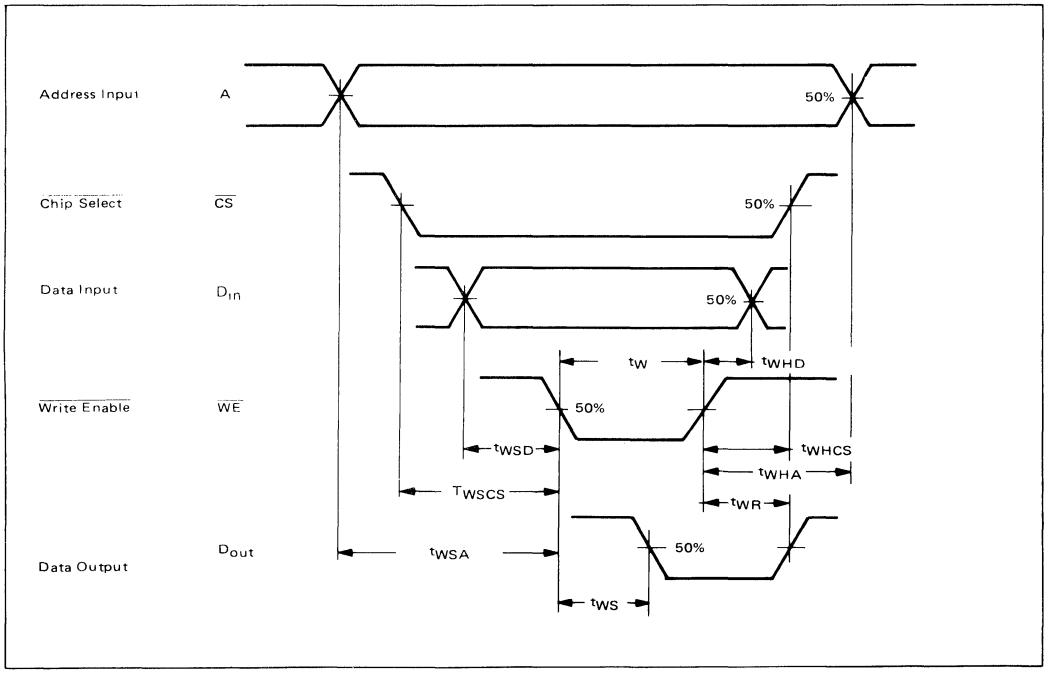


FIGURE 4 – WRITE STROBE MODE



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MCM10147

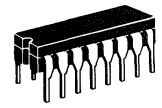
MECL

128-BIT RANDOM ACCESS MEMORY

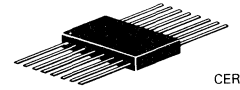
128 x 1-BIT RANDOM ACCESS MEMORY

The MCM10147 is a 128-word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of a 7-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 2 active-low chip select lines. It has a typical access time of 10 ns and is designed for high-speed scratch pads, control, cache, and buffer storage applications.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 5.0 ns
- Operating Temperature Range = 0^{o} to $+75^{o}C$
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family
- Similar to F10405.



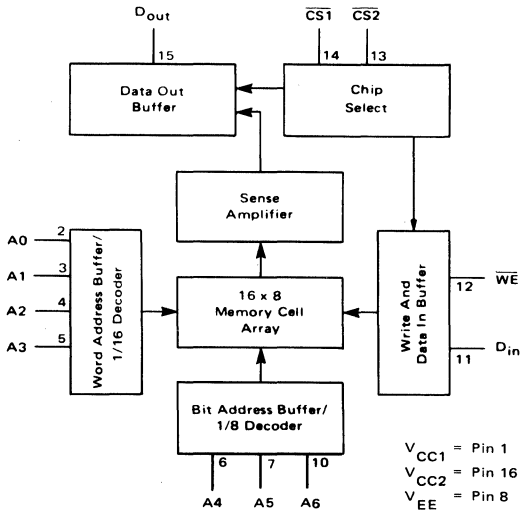
L SUFFIX
CERAMIC PACKAGE
CASE 620



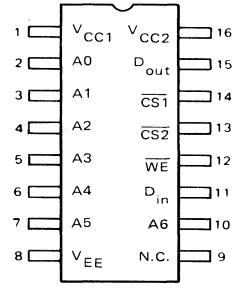
F SUFFIX
CERAMIC PACKAGE
CASE 650

7

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A6	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2}$ ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM 10147 is a 128 word x 1-bit RAM. Bit selection is achieved by means of a 7-bit address A0 thru A6.

The active-low chip select allows memory expansion up to 512 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

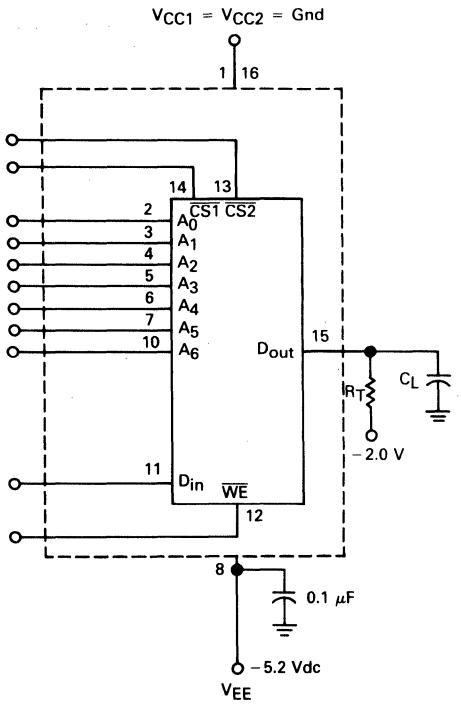
		MCM10144 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	105	–	100	–	95	mAdc	Typ I_{EE} @ 25°C = 80 mA All outputs and inputs open. Measure pin 8.
Input Current High	I_{inH}	–	220	–	220	–	220	µAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	I_{inL}	0.5	–	0.5	–	0.3	–	µAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

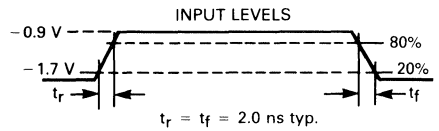
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	5.0	8.0	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	5.0	8.0	ns	output. See Note 2.
Address Access Time	t_{AA}	5.0	10	15	ns	
Write Mode						
Write Pulse Width	t_W	8.0	6.0	–	ns	t_{WSA} = 4.0 ns
Data Setup Time Prior to Write	t_{WSD}	1.0	-5.0	–	ns	
Data Hold Time After Write	t_{WHD}	3.0	-2.0	–	ns	
Address Setup Time Prior to Write	t_{WSA}	4.0	0	–	ns	t_W = 8.0 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	3.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	1.0	-5.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	1.0	-5.0	–	ns	
Write Disable Time	t_{WS}	2.0	5.0	8.0	ns	Measured at 50% of input to 50%
Write Recovery Time	t_{WR}	2.0	5.0	8.0	ns	of output.
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





$t_r = t_f$ = 2.0 ns typ.

All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF

FIGURE 2 – CHIP SELECT ACCESS TIME

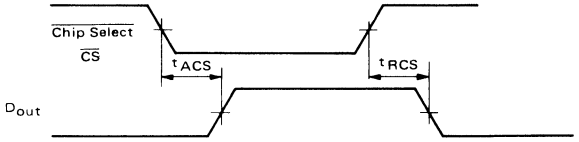


FIGURE 3 – ADDRESS ACCESS TIME

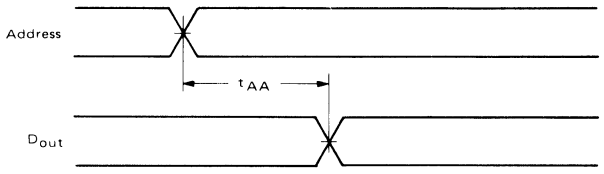
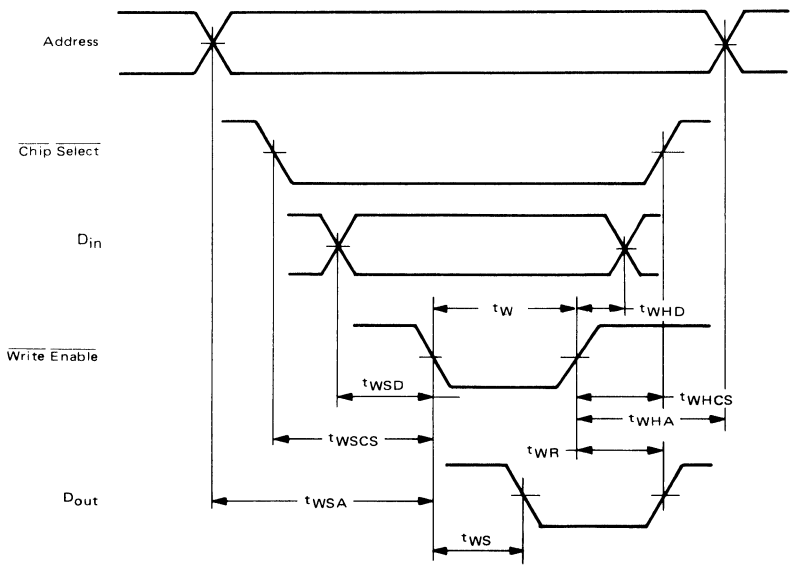


FIGURE 4 – WRITE MODE



7

MCM10148

MECL

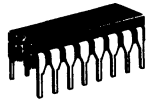
64 X 1-BIT
RANDOM ACCESS MEMORY

128 x 1-BIT RANDOM ACCESS MEMORY

The MCM10148 is a fast 64-word X 1-bit RAM. Bit selection is achieved by means of a 6-bit address, A0 through A5.

The active-low chip selects and fast chip select access time allow easy memory expansion up to 256 words without affecting system performance. The operating mode (CS inputs low) is controlled by the WE input. With WE low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With WE high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

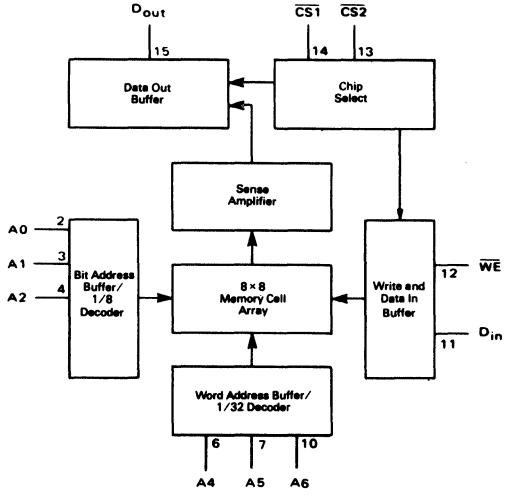
- Typical Address Access Time of 10 ns
- Typical Chip Select Access Time of 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (420 mW typ @ 25°C) Decreases with Increasing Temperature
- 50 kΩ Input Pulldown Resistors (420 mW typ) on All Inputs



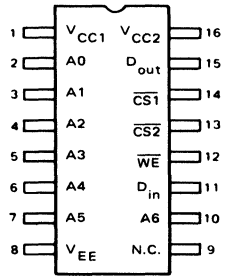
L SUFFIX
CERAMIC PACKAGE
CASE 620

7

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NOTATION

CS	Chip Select Input
A0 thru A6	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2}$

ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	0°C		+25°C		+75°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	—	105	—	100	—	95	mAdc
Input Current High	I_{inH}	—	220	—	220	—	220	μAdc

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10148 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ±5%		Unit	Conditions
		Min	Max		
Read Mode				ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	—	7.5		
Chip Select Recovery Time	t_{RCS}	—	7.5		
Address Access time	t_{AA}	—	15		
Write Mode				ns	t_{WSA} = 5.0 ns Measured at 50% of input to 50% of output. t_W = 8.0 ns.
Write Pulse Width	t_W	8.0	—		
Data Setup Time Prior to Write	t_{WSD}	3.0	—		
Data Hold Time After Write	t_{WHD}	2.0	—		
Address Setup Time Prior to Write	t_{WSA}	5.0	—		
Address Hold Time After Write	t_{WHA}	3.0	—		
Chip Select Setup Time Prior to Write	t_{WSCS}	3.0	—		
Chip Select Hold Time After Write	t_{WHCS}	0	—		
Write Disable Time	t_{WS}	2.0	7.5		
Write Recovery Time	t_{WR}	2.0	7.5		
Rise and Fall Time	t_r, t_f	1.5	5.0	ns	Measured between 20% and 80% points.
Capacitance				pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	5.0		
Output Capacitance	C_{out}	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50Ω, MCM10148.

$C_L \leq 5.0$ pF (including jig and stray capacitance)

Delay should be derated 30 ps/pF for capacitive load up to 50 pF.

2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

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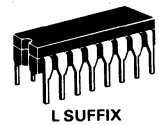
MCM10152

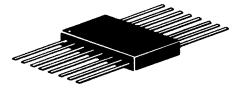
256 x 1-BIT RANDOM ACCESS MEMORY

The MCM10152 is a 256 word x 1-bit Read/Write Random Access Memory. Data is accessed or stored by means of an 8-bit address decoded on chip. It has a non-inverting data out, a separate data in line and 3 active-low chip select lines. It has a typical access time of 11 ns and is designed for high-speed scratch pad, control, cache, and buffer storage applications.

- Typical Address Access Time = 11 ns
- Typical Chip Select Access Time = 4.0 ns
- Operating Temperature Range = 0° to +75°C
- Open Emitter Output Permits Wired-OR for Easy Memory Expansion
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation Decreases with Increasing Temperature
- Fully Compatible with MECL 10,000 Logic Family

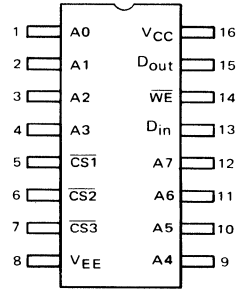


L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

PIN ASSIGNMENT

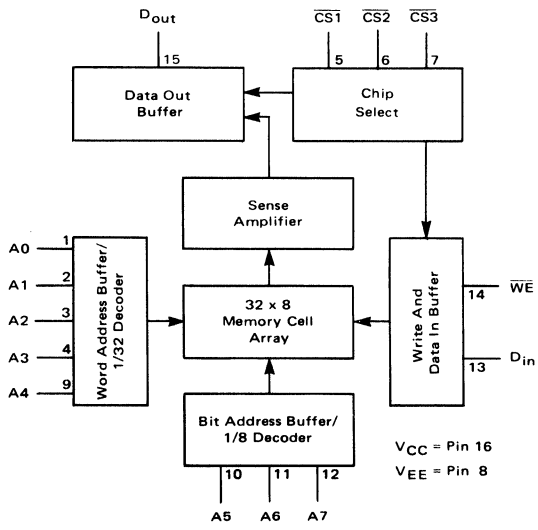


PIN NOTATION

CS	Chip Select Input
A0 thru A7	Address Inputs
D_{in}	Data Input
D_{out}	Data Output
WE	Write Enable Input

7

BLOCK DIAGRAM



TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.

FUNCTIONAL DESCRIPTION:

The MCM10152 is a 256 word x 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 thru A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	< 50 < 100	mAdc
Junction Operating Temperature	T_J	< 165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

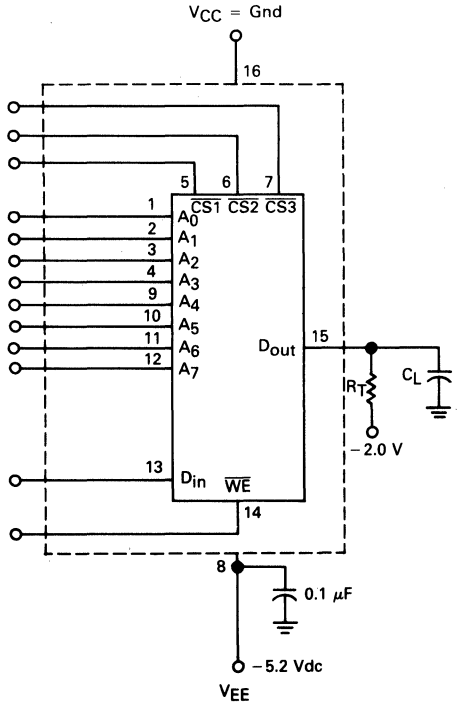
		MCM10152 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	–	135	–	130	–	125	mAdc	Typ I_{EE} @ 25°C = 110 mA All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	–	220	–	220	–	220	µAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	–	0.5	–	0.3	–	µAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V
Logic "0" Output Voltage	V_{OL}	-1.870	-1.665	-1.850	-1.650	-1.830	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	–	-0.980	–	-0.920	–	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to -2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	–	-1.645	–	-1.630	–	-1.605	Vdc	

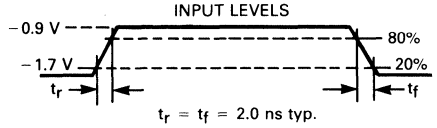
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ± 5%; Output Load see Figure 1; see Note 1 & 3.)

Characteristic	Symbol	Test Limits Min	Typ	Max	Unit	Conditions
Read Mode						See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	2.0	4.0	7.5	ns	Measured from 50% of input to 50% of
Chip Select Recovery Time	t_{RCS}	2.0	4.0	7.5	ns	output. See Note 2.
Address Access Time	t_{AA}	7.0	11	15	ns	
Write Mode						
Write Pulse Width	t_W	10	6.0	–	ns	t_{WSA} = 5.0 ns
Data Setup Time Prior to Write	t_{WSD}	2.0	-3.0	–	ns	Measured at 50% of input to 50% of
Data Hold Time After Write	t_{WHD}	2.0	-2.0	–	ns	output.
Address Setup Time Prior to Write	t_{WSA}	5.0	3.0	–	ns	t_W = 10 ns. See Figure 4.
Address Hold Time After Write	t_{WHA}	3.0	0	–	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	-3.0	–	ns	
Chip Select Hold Time After Write	t_{WHCS}	2.0	-3.0	–	ns	
Write Disable Time	t_{WS}	2.5	5.0	7.5	ns	
Write Recovery Time	t_{WR}	2.5	5.0	7.5	ns	
Rise and Fall Time						Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	3.0	5.0	ns	
Capacitance						
Input Capacitance	C_{in}	–	4.0	5.0	pF	
Output Capacitance	C_{out}	–	7.0	8.0	pF	

Notes: (1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a system environment, consult: "MECL System Design Handbook."

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





All timing measurements referenced to 50% of input levels.
R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF

FIGURE 2 – CHIP SELECT ACCESS TIME

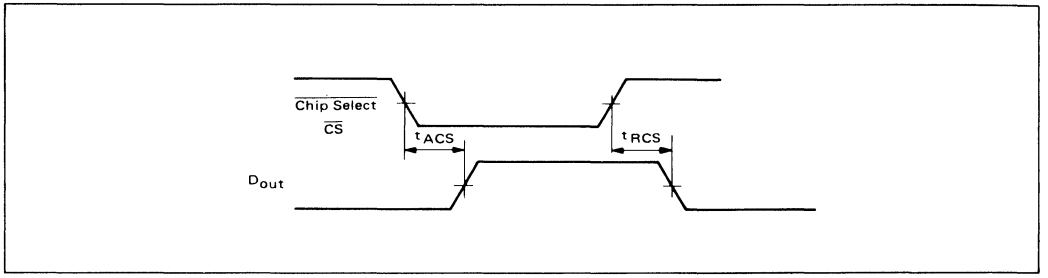


FIGURE 3 – ADDRESS ACCESS TIME

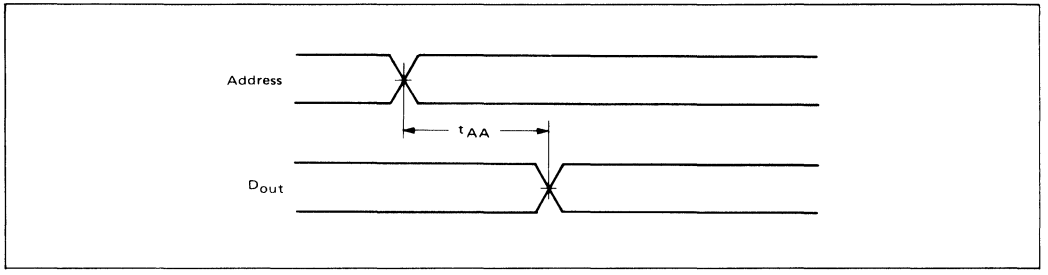
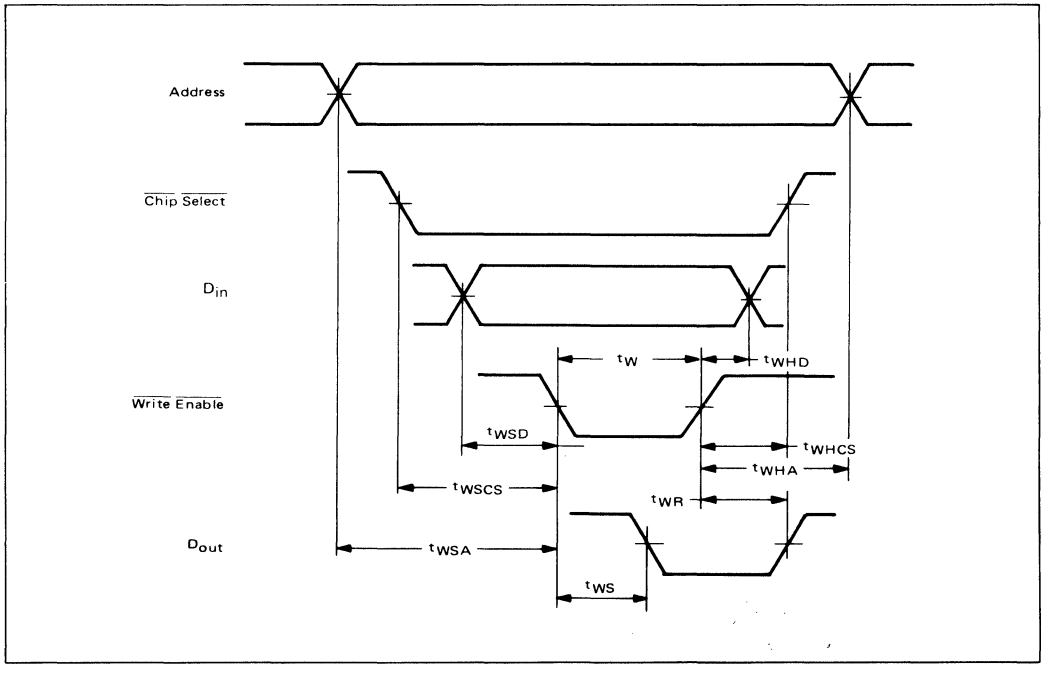


FIGURE 4 – WRITE MODE



7

MCM10415-15
MCM10415-20

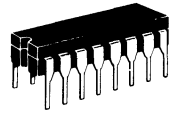
MECL
1024-BIT RANDOM
ACCESS MEMORY

1024 x 1-BIT RANDOM ACCESS MEMORY

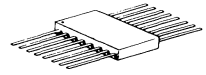
The MCM10415 is a 1024-bit Read/Write Random Access Memory organized 1024 words by 1 bit. Data is selected or stored by means of a 10-bit address (A0 through A9) decoded on the chip. The chip is designed with a separate data in line, a noninverting data output, and an active-low chip select.

This device is designed for use in high-speed scratch pad, control, cache and buffer storage applications.

- Address Access Time: MCM10415-20 20 ns (Max)
  MCM10415-15 15 ns (Max)
- Fully Compatible with MECL 10K/10KH
- Temperature Range of 0° to 75°C
- Emitter-Follower Output Permits Full Wire-ORing
- Power Dissipation Decreases with Increasing Temperature



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

ORDERING INFORMATION
Suffix Denotes
MCM10415L15 — Ceramic Dual-in-Line Package
MCM10415F15 — Ceramic Flat Package
MCM10415L20 — Ceramic Dual-in-Line Package
MCM10415F20 — Ceramic Flat Package

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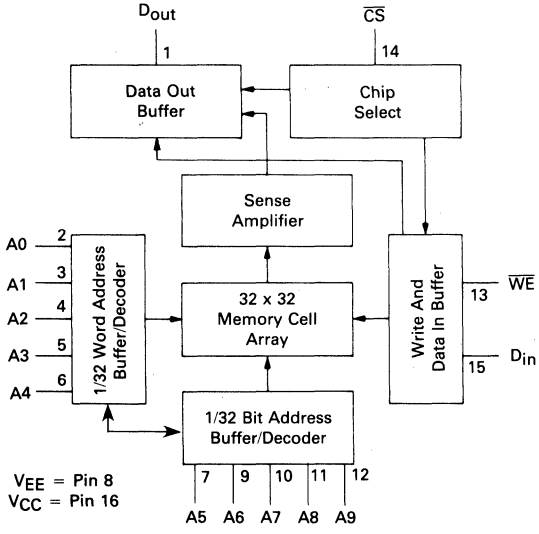
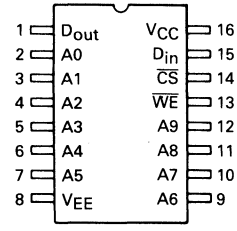
BLOCK DIAGRAM



PIN ASSIGNMENT



PIN DESIGNATION

$\overline{CS}$	Chip Select Input
A0 to A9	Address Inputs
D_{in}	Data Inputs
D_{out}	Data Output
$\overline{WE}$	Write Enable Input

FUNCTIONAL DESCRIPTION:

This device is a 1024 x 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM (CS input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented noninverted at D_{out}. (See Truth Table)

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	−8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	<50 <100	mAdc
Junction Operating Temperature	T_J	<165	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

	DC TEST VOLTAGE VALUES (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	−0.840	−1.870	−1.145	−1.490	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+75°C	−0.720	−1.830	−1.045	−1.450	−5.2

ELECTRICAL CHARACTERISTICS

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts.

		MCM10415 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	—	150	—	145	—	125	mAdc	Typ I_{EE} @ 25°C = 100 mA All outputs and inputs open. Measure Pin 8.
Input Current High	I_{inH}	—	220	—	220	—	220	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low ($\overline{CS}$ only) Input Curent Low (All Others)	I_{inL}	0.5 −50	—	0.5 −50	—	0.3 −50	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	Vdc	Load 50 Ω to −2.0 V
Logic "0" Output Voltage	V_{OL}	−1.870	−1.665	−1.850	−1.650	−1.830	−1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	−1.020	—	−0.980	—	−0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time. $V_{in} = V_{IHA}$ or V_{ILA}. Load 50 Ω to −2.0 V.
Logic "0" Threshold Voltage	V_{OLA}	—	−1.645	—	−1.630	—	−1.605	Vdc	

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Guaranteed with V_{EE} = −5.2 Vdc ±5.0%, T_A = 0°C to 75°C (see Note 1). Output Load see Figure 1.

Characteristic	Symbol	MCM10415-20 Min	MCM10415-20 Max	MCM10415-15 Min	MCM10415-15 Max	Unit	Conditions
Read Mode							See Figures 2 and 3.
Chip Select Access Time	t_{ACS}	—	8.0	—	7.0	ns	Measured at 50% of input to 50% of output.
Chip Select Recovery Time	t_{RCS}	—	8.0	—	7.0	ns	See Note 2.
Address Access Time	t_{AA}	—	20	—	15	ns	
Write Mode							See Figure 4.
Write Pulse Width (To guarantee writing)	t_W	14	—	12	—	ns	t_{WSA} = 3.0 ns — MCM10415-20 t_{WSA} = 2.0 ns — MCM10415-15 Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	3.0	—	2.0	—	ns	
Data Hold Time After Write	t_{WHD}	3.0	—	1.0	—	ns	
Address Setup Time Prior to Write	t_{WSA}	3.0	—	2.0	—	ns	t_W = 14 ns — MCM10415-20 t_W = 12 ns — MCM10415-15
Address Hold Time After Write	t_{WHA}	3.0	—	1.0	—	ns	
Chip Select Setup Time Prior to Write	t_{WSCS}	3.0	—	2.0	—	ns	
Chip Select Hold Time After Write	t_{WHCS}	3.0	—	1.0	—	ns	
Write Disable Time	t_{WS}	—	8.0	—	7.0	ns	
Write Recovery Time	t_{WR}	—	8.0	—	7.0	ns	
Rise and Fall Time							Measured between 20% and 80% points.
Output Rise and Fall Time	t_r, t_f	1.5	4.0	1.5	4.0	ns	When driven from $\overline{CS}$ or $\overline{WE}$ inputs.
Output Rise and Fall Time	t_r, t_f	1.5	8.0	1.5	8.0	ns	When driven from Address inputs.
Capacitance							Measured with a pulse technique. See Note 4.
Input Lead Capacitance	C_{in}	—	5.0	—	5.0	pF	
Output Lead Capacitance	C_{out}	—	8.0	—	8.0	pF	

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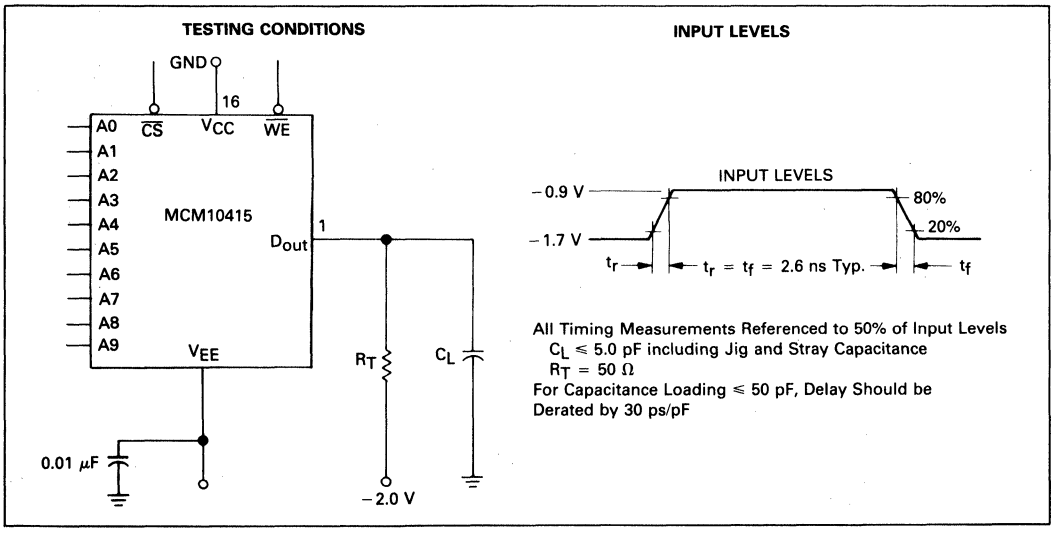
Notes:
(1) Contact your Motorola Sales Representative for details if extended temperature operation is desired.
(2) The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
(3) For proper use of MECL Memories in a System environment, consult: "MECL System Design Handbook."
(4) Typical ratings are 3.0 pF for C_{in} and 5.0 pF for C_{out}.

FIGURE 1 — SWITCHING TEST CIRCUIT AND WAVEFORMS



MECL PROMs 8

MECL PROMs

(0 to 75°C)

Organization	Part Number	Access Time (ns max)	Pins
32 × 8	MCM10139	20	16
256 × 4	MCM10149-10	10	16
256 × 4	MCM10149-25	25	16

MCM10139

MECL

32 X 8 BIT PROGRAMMABLE READ-ONLY MEMORY

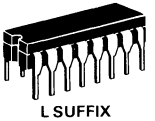
256-BIT PROGRAMMABLE READ ONLY MEMORY (PROM)

The MCM10139 is a 256-bit programmable read only memory (PROM). The circuit is organized as 32 words of 8 bits. Prior to programming, all stored bits are at logic 0 (low) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The MCM10139 has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

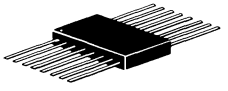
The MCM10139 is fully compatible with the MECL 10,000 logic family. It is designed for use in microprogramming, code conversion, logic simulation, and look-up table storage.

P_D = 520 mW typ/pkg (No Load)

t_{Access} = 15 ns typ (Address Inputs)

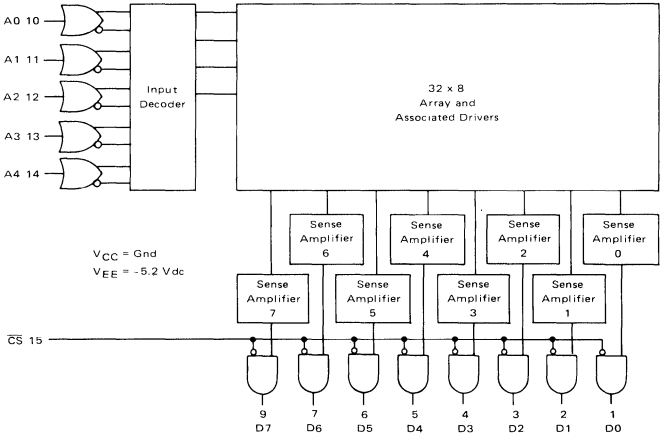


L SUFFIX
CERAMIC PACKAGE
CASE 620

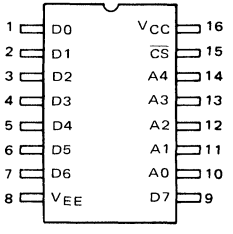


F SUFFIX
CERAMIC PACKAGE
CASE 650

LOGIC DIAGRAM



PIN ASSIGNMENT



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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8 to 0	Vdc
Base Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{EE}	Vdc
Output Source Current — Continuous — Surge	I_O	<50 <100	mAdc
Junction Operating Temperature	T_J	<165	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

ELECTRICAL CHARACTERISTICS

	DC Test Voltage Values (Volts)				
Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2
+75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Each MECL Memory circuit has been designed to meet the dc and ac specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts.

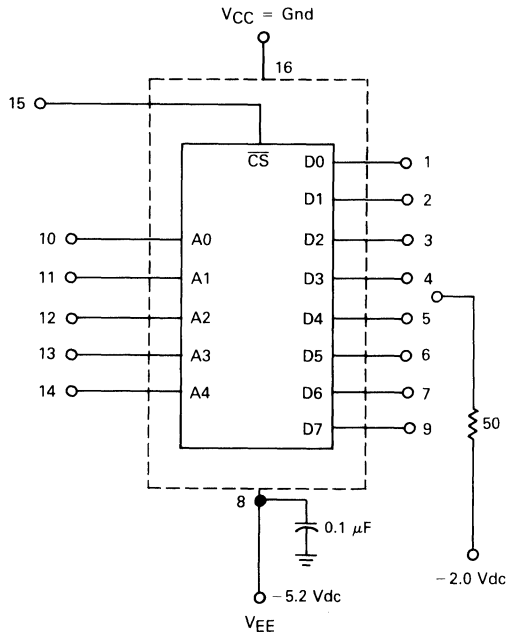
		MCM10139 Test Limits							
		0°C		+25°C		+75°C			
DC Characteristics	Symbol	Min	Max	Min	Max	Min	Max	Unit	Conditions
Power Supply Drain Current	I_{EE}	—	150	—	145	—	140	mAdc	Typ I_{EE} @ 25°C = 100 mA. All outputs and inputs open. Measure pin 8.
Input Current High	$I_{in}H$	—	265	—	265	—	265	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IH}$.
Input Current Low	$I_{in}L$	0.5	—	0.5	—	0.3	—	μAdc	Test one input at a time, all other inputs are open. $V_{in} = V_{IL}$.
Logic "1" Output Voltage	V_{OH}	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc	Load 50 Ω to -2.0 V.
Logic "0" Output Voltage	V_{OL}	-2.010	-1.665	-1.990	-1.650	-1.970	-1.625	Vdc	
Logic "1" Threshold Voltage	V_{OHA}	-1.020	—	-0.980	—	-0.920	—	Vdc	Threshold testing is performed and guaranteed on one input at a time.
Logic "0" Threshold Voltage	V_{OLA}	—	-1.645	—	-1.630	—	-1.605	Vdc	$V_{in} = V_{ILH}$ or V_{ILA}. Load 50 Ω to -2.0 V.

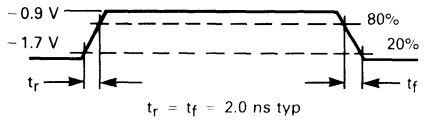
SWITCHING CHARACTERISTICS (T_A = 0° to +75°C, V_{EE} = -5.2 Vdc ±5%; Output Load—See Figure 1 and Note 1)

		Test Limits				
Characteristic	Symbol	Min	Typ	Max	Unit	Conditions
Chip Select Access Time	t_{ACS}	—	10	15	ns	See Figures 2 and 3.
Chip Select Recovery Time	t_{RCS}	—	10	15	ns	Measured from 50% of input to 50%
Address Access Time	t_{AA}	—	15	20	ns	of output. See Note 2.
Output Rise and Fall Time	t_r, t_f	—	3.0	—	ns	Measured between 20% and 80% points.
Input Capacitance	C_{in}	—	4.0	5.0	pF	
Output Capacitance	C_{out}	—	7.0	8.0	pF	

Notes: 1. Contact your Motorola Sales Representative for details if extended temperature operation is desired.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the memory.

FIGURE 1 — SWITCHING TIME TEST CIRCUIT





$t_r = t_f = 2.0$ ns typ

All timing measurements referenced to 50% of input levels.
All outputs loaded 50 ohms to −2.0 Vdc.

FIGURE 2 – CHIP SELECT ACCESS TIME

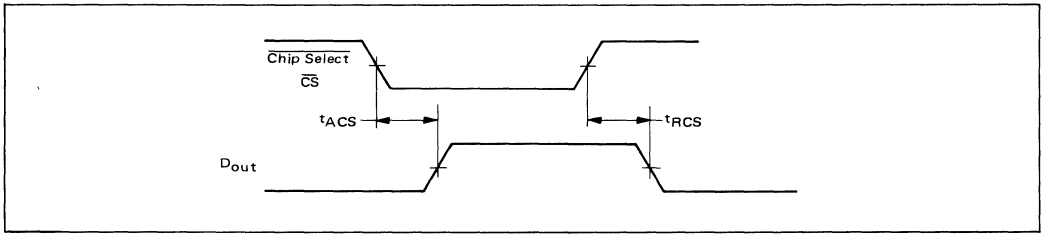
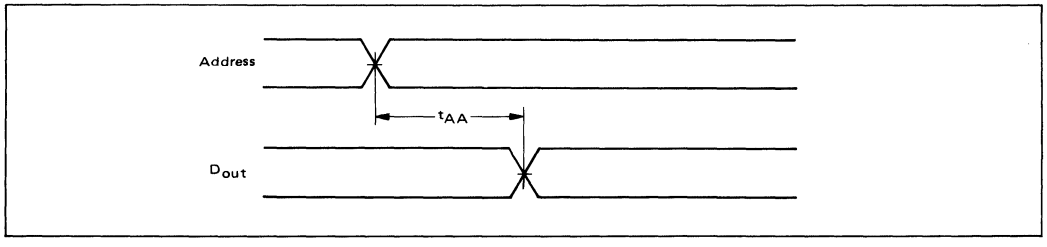


FIGURE 3 – ADDRESS ACCESS TIME



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RECOMMENDED PROGRAMMING PROCEDURE*

The MCM10139 is shipped with all bits at logical "0" (low). To write logical "1s", proceed as follows.

MANUAL (See Figure 4)

Step 1 Connect V_{EE} (Pin 8) to -5.2 V and V_{CC} (Pin 16) to 0.0 V. Address the word to be programmed by applying -1.2 to -0.6 volts for a logic "1" and -5.2 to -4.2 volts for a logic "0" to the appropriate address inputs.

Step 2 Raise V_{CC} (Pin 16) to +6.8 volts.

Step 3 After V_{CC} has stabilized at +6.8 volts (including any ringing which may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

Step 4 Return V_{CC} to 0.0 Volts.

CAUTION

To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at +6.8 volts for more than 1 second.

Step 5 Verify that the selected bit has programmed by connecting a 460 Ω resistor to -5.2 volts and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once. During verification V_{IH} should be -1.0 to -0.6 volts.

Step 6 If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (See Figure 5)

Step 1 Connect V_{EE} (Pin 8) to -5.2 volts and V_{CC} (Pin 16) to 0.0 volts. Apply the proper address data and raise V_{CC} (Pin 16) to +6.8 volts.

Step 2 After a minimum delay of 100 μs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.1 \leq PW \leq 1$ ms).

Step 3 Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time. The delay between output programming pulses should be equal to or less than 1.0 ms.)

Step 4 After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at +6.8 volts during the entire programming time.

Step 5 After stepping through all address words, return V_{CC} to 0.0 volts and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once. During verification V_{IH} should be -1.0 to -0.6 volts.

*NOTE: For devices that program incorrectly—return serialized units with individual truth tables. Noncompliance voids warranty.

PROGRAMMING SPECIFICATIONS

Characteristic	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
Power Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	Vdc	
To Program	V_{CCP}	+6.04	+6.8	+7.56	Vdc	
To Verify	V_{CCV}	0	0	0	Vdc	
Programming Supply Current	I_{CCP}	–	200	600	mA	V_{CC} = +6.8 Vdc
Address Voltage	V_{IH} Program	-1.2	–	-0.6	Vdc	
Logical "1"	V_{IH} Verify	-1.0	–	-0.6	Vdc	
Logical "0"	V_{IL}	-5.2	–	-4.2	Vdc	
Maximum Time at $V_{CC} = V_{CCP}$	–	--	–	1.0	sec	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mAdc	
Output Program Pulse Width	t_p	0.5	–	1.0	ms	
Output Pulse Rise Time	–	–	–	10	μs	
Programming Pulse Delay (1)						
Following V_{CC} change	t_d	0.1	–	1.0	ms	
Between Output Pulses	t_{d1}	0.01	–	1.0	ms	

NOTE 1. Maximum is specified to minimize the amount of time V_{CC} is at +6.8 volts.

FIGURE 4 – MANUAL PROGRAMMING CIRCUIT

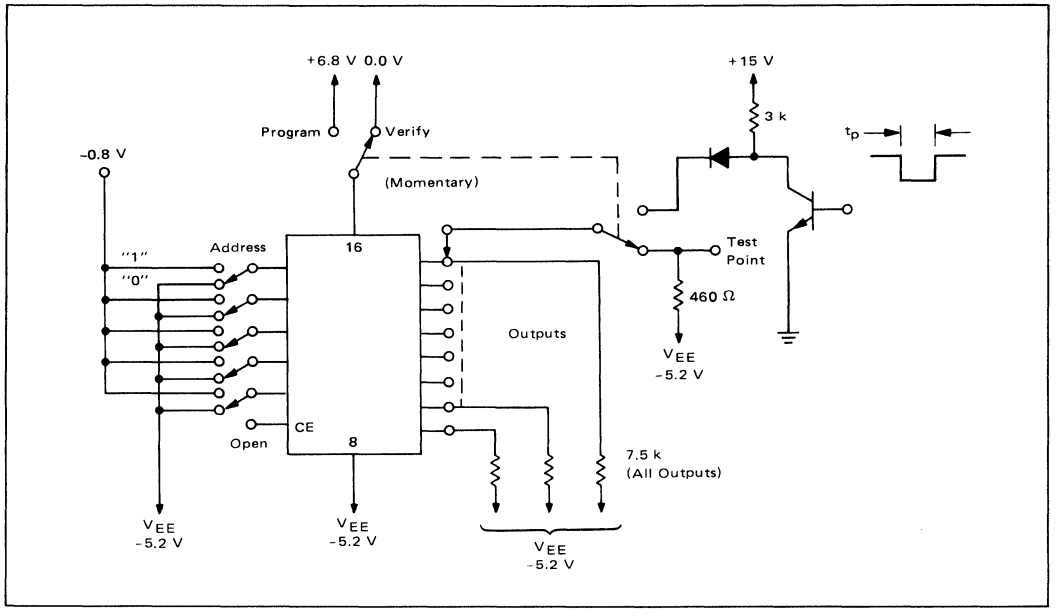
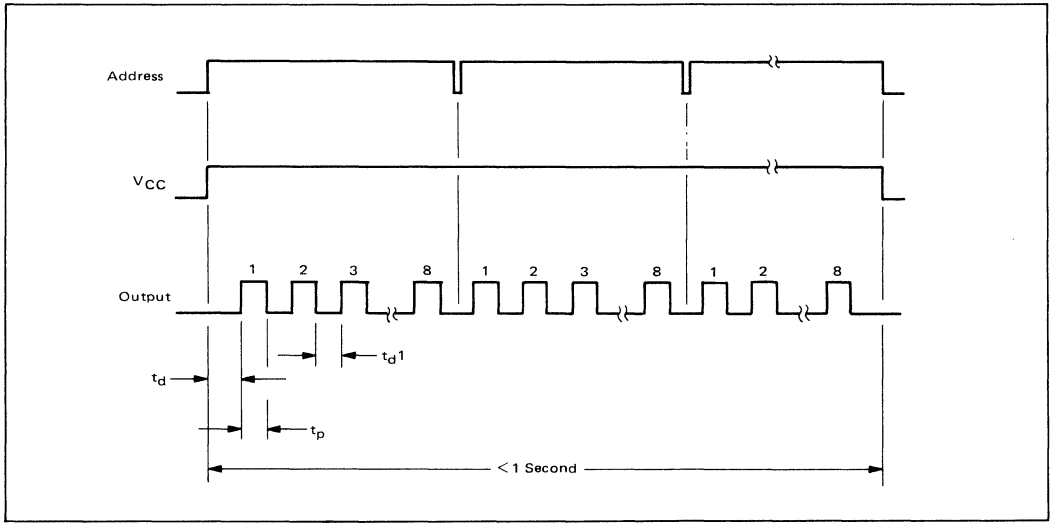


FIGURE 5 – AUTOMATIC PROGRAMMING CIRCUIT



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MCM10149*10

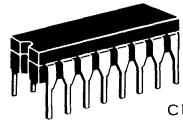
256 x 4-BIT PROGRAMMABLE READ-ONLY MEMORY

This device is a 256-word x 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

- Typical Address Access Time of 7.0 ns
- Typical Chip Select Access Time of 2.5 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (740 mW typ @ 25°C) Decreases with Increasing Temperature

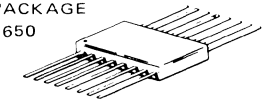
MECL

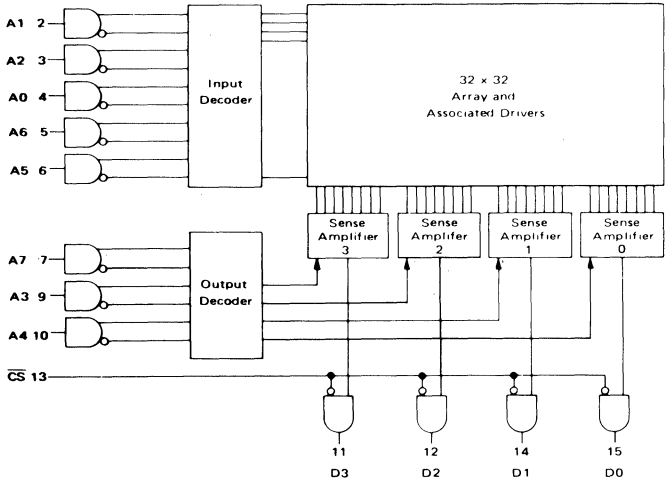
1024-BIT PROGRAMMABLE READ-ONLY MEMORY



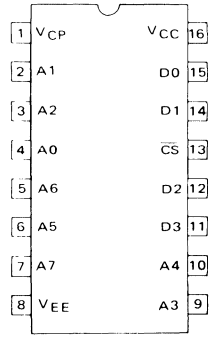
L SUFFIX
CERAMIC PACKAGE
CASE 620

F SUFFIX
CERAMIC PACKAGE
CASE 650





PIN ASSIGNMENT



8

ELECTRICAL CHARACTERISTICS①

Characteristic	Symbol	0°C		+25°C		+75°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	--	175	–	170	–	165	mAdc
Input Current High	I_{inH}	–	265	--	265	–	265	μAdc

Forcing Function	Parameter	0°C	25°C②	75°C②
V_{IHmax} =	V_{OHmax}	−0.840	−0.810	−0.720
	V_{OHmin}	−1.000	−0.960	−0.900
V_{IHAmin}	V_{OHAmin}	−1.020	−0.980	−0.920
		−1.130	−1.105	−1.045
V_{ILAmax}		−1.490	−1.475	−1.450
	V_{OLAmax}	−1.645	−1.630	−1.605
	V_{OLmax}	−1.665	−1.650	−1.625
V_{ILmin} =	V_{OLmin}	−1.870	−1.850	−1.830
V_{ILmin}	I_{NLmin}	0.5	0.5	0.3

NOTES: ① The MCM10149*10 is designed to meet the dc specifications in the electrical characteristics tables after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear FPM is maintained. Outputs are terminated through a 50 Ω resistor to −2.0 V.
② 0–75°C temperature range, 50 Ω to −2.0 V.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	T_A = 0 to 75°C, V_{EE} = −5.2 Vdc ±5%			Unit	Conditions
		Min	Typ	Max		
Read Mode					ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	1.0	3.0	5.0		
Chip Select Recovery Time	t_{RCS}	1.0	3.0	5.0		
Address Access Time	t_{AA}	3.0	7.0	10		
Rise and Fall Time	t_r, t_f	1.0	2.0	5.0	ns	Measured between 20% and 80% points.
Capacitance					pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	—	5.0		
Output Capacitance	C_{out}	—	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. V_{CP} = V_{CC} = Gnd for normal operation.

PROGRAMMING THE MCM10149*10

During programming of the MCM10149*10, input Pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input Pins 2, 3, 4, 5, and 6 are addressed with 0 V $\leq V_{IH} \leq$ +0.25 V and $V_{EE} \leq V_{IL} \leq$ −3.0 V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with V_{CP} = V_{CC} = 0 V and V_{EE} = −5.2 V ±5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to +10 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 15.2 V, +10 V − [− 5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1 − 10 μs range, while its pulse width (t_{W1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at +10 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of −5.2 V ±5%.

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Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresponding output pin to a voltage of +2.85 V ±5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor to −2.0 V. Current into the selected output is 5 mA maximum.

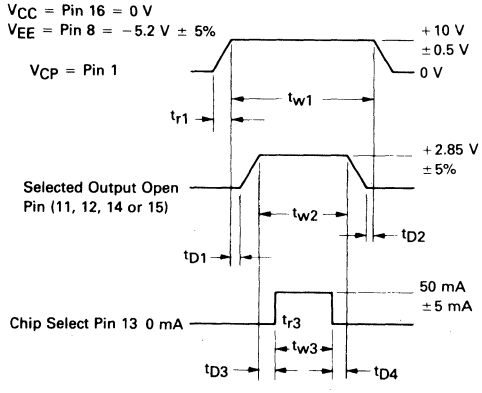
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. It pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ±5.0 mA. The voltage clamp on this current source is to be −6.0 V.

After the fusing current source has returned to 0 mA, the bit select pulse is returned to its initial level, i.e., the output is returned through its load to −2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Non compliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149*10.



The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of ≤ 15% is to be observed.

Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	≥ 1 μs
t_{w1}	Pulse Width, Programming Voltage	≥ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	≥ 0
t_{w2}	Pulse Width, Bit Select	≥ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	≥ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	≥ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	≥ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	≥ 1 μs

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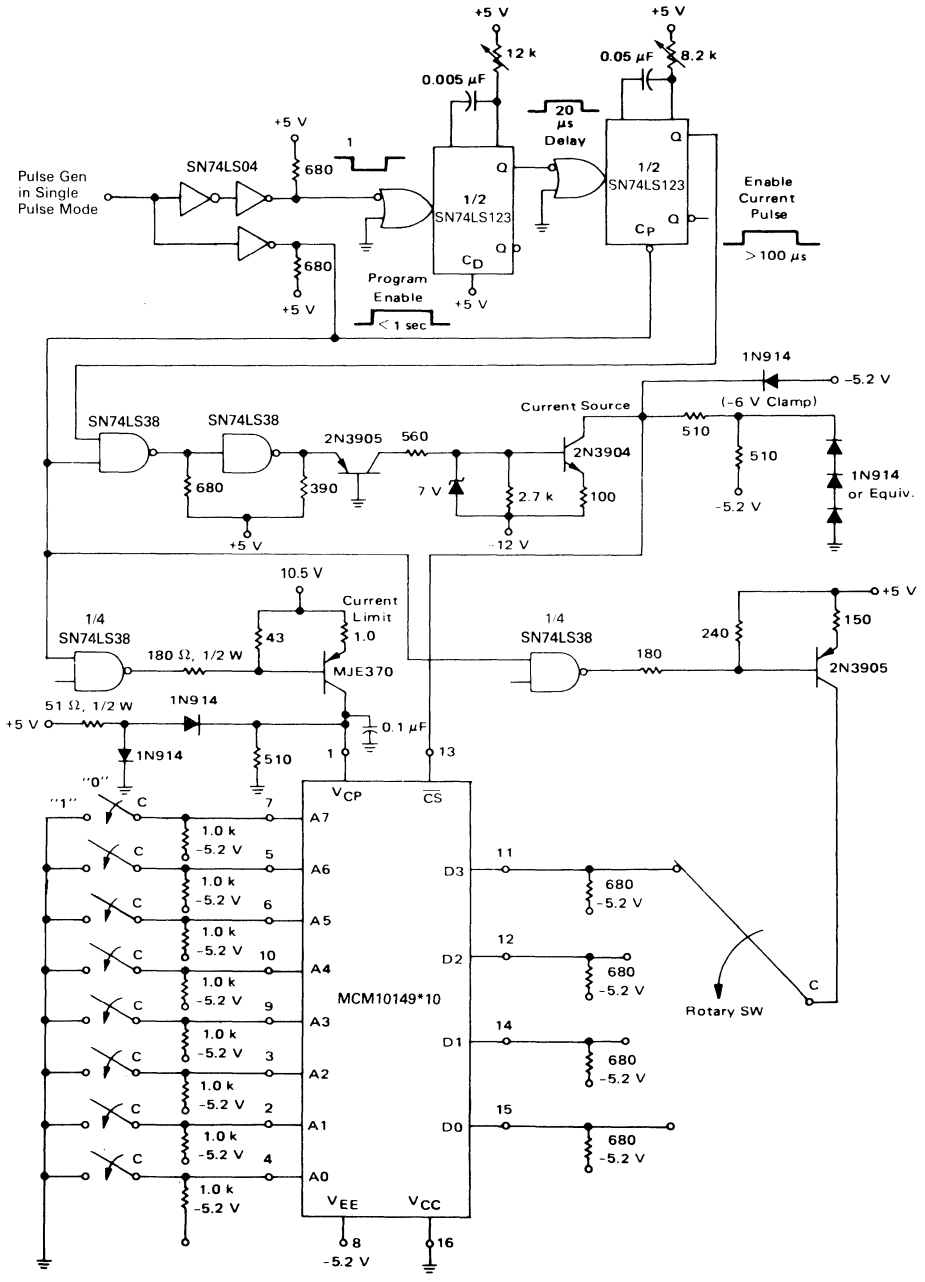
MANUAL PROGRAMMING CIRCUIT



MCM10149*25

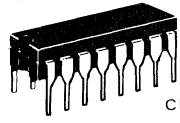
256 x 4-BIT PROGRAMMABLE READ-ONLY MEMORY

This device is a 256-word x 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

- Typical Address Access Time of 20 ns
- Typical Chip Select Access Time of 8.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @ 25°C) Decreases with Increasing Temperature

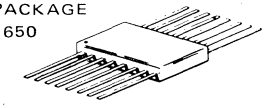
MECL

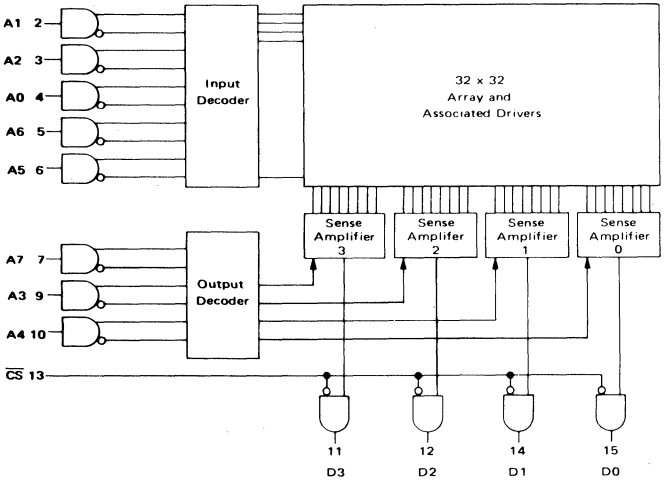
1024-BIT PROGRAMMABLE READ-ONLY MEMORY



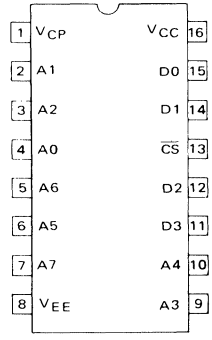
L SUFFIX
CERAMIC PACKAGE
CASE 620

F SUFFIX
CERAMIC PACKAGE
CASE 650





PIN ASSIGNMENT



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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	0°C		+25°C		+75°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	155	–	150	–	145	mAdc
Input Current High	I_{inH}	–	265	–	265	–	265	μAdc

Forcing Function	Parameter	0°C	25°C①	75°C①
V_{IHmax} =	V_{OHmax}	−0.840	−0.810	−0.720
	V_{OHmin}	−1.000	−0.960	−0.900
V_{IHAmin}	V_{OHAmin}	−1.020	−0.980	−0.920
		−1.130	−1.105	−1.045
V_{ILAmax}		−1.490	−1.475	−1.450
	V_{OLAmax}	−1.645	−1.630	−1.605
	V_{OLmax}	−1.665	−1.650	−1.625
V_{ILmin} =	V_{OLmin}	−1.870	−1.850	−1.830
V_{ILmin}	I_{NLmin}	0.5	0.5	0.3

NOTES: ① 0–75°C temperature range, 50Ω to −2.0V.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10149*25 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max		
Read Mode				ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	2.0	10		
Chip Select Recovery Time	t_{RCS}	2.0	10		
Address Access Time	t_{AA}	7.0	25		
Rise and Fall Time	t_r, t_f	1.5	7.0	ns	Measured between 20% and 80% points.
Capacitance				pF	Measured with a pulse technique.
Input Capacitance	C_{in}	—	5.0		
Output Capacitance	C_{out}	—	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10149;
$C_L \leq 5.0$ pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. $V_{CP} = V_{CC}$ = Gnd for normal operation.

*To be determined; contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 †

During programming of the MCM 10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with $0 V \leq V_{IH} \leq +0.25$ V and $V_{EE} \leq V_{IL} \leq -3.0$ V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with $V_{CP} = V_{CC}$ = 0 V and $V_{EE} = -5.2$ V ± 5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to + 12 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 17.2 V, + 12 V − [− 5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1 − 10 μs range, while its pulse width (t_{W1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at + 12 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be

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set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of − 5.2 V ± 5%.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresponding output pin to a voltage of + 2.85 V ± 5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor to − 2.0 into the selected

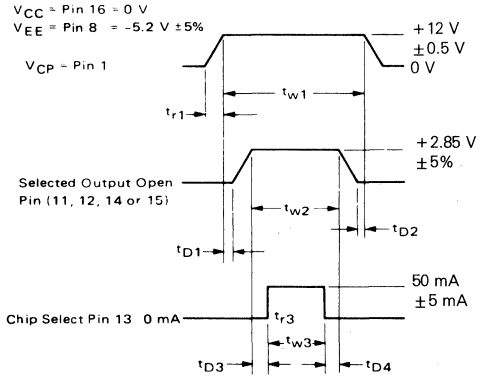
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. It pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ± 5.0 mA. The voltage clamp on this current source is to be − 6.0 V.

After the fusing current source has returned 0 mA, the bit select pulse is returned to it initial level, i.e., the output is returned through its load to − 2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Non compliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.



The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of ⩽ 15% is to be observed.

Definitions and values of timing symbols are as follows.

Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	⩾ 1 μs
t_{w1}	Pulse Width, Programming Voltage	⩾ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	⩾ 0
t_{w2}	Pulse Width, Bit Select	⩾ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	⩾ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	⩾ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	⩾ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	⩾ 1 μs

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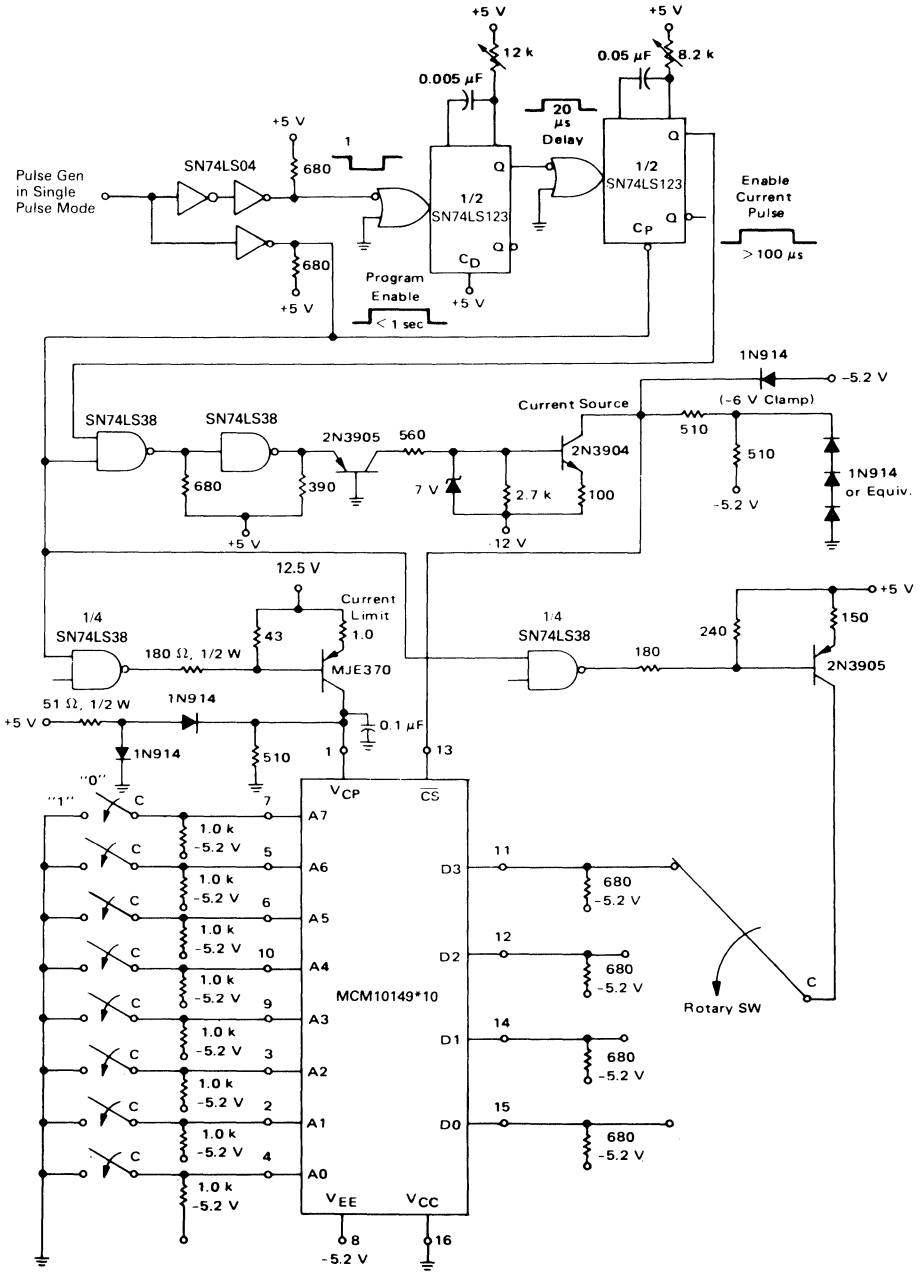
MANUAL PROGRAMMING CIRCUIT



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Military Products 9

Military CMOS Static RAMs

(+5 V, −55 to 125°C)

Organization	Part Number	Access Time (ns max)	Pins
4K × 4	6168-55/BRAJC	55	20
	6168-55/BYAJC	55	20
	6168-55/BUAJC	55	20
	6168-70/BRAJC	70	20
	6168-70/BYAJC	70	20
	6168-70/BUAJC	70	20
	6268-35/BRAJC	35	20
	6268-35/BYAJC	35	20
	6268-35/BUAJC	35	20
	6268-45/BRAJC	45	20
	6268-45/BYAJC	45	20
	6268-45/BUAJC	45	20
8K × 8	6164-55/BXAJC	55	28
	6164-55/BUAJC	55	32
	6164-70/BXAJC	70	28
	6164-70/BUAJC	70	32
16K × 4	6288-35/BXAJC	35	22
	6288-35/BUAJC	35	22
	6288-45/BXAJC	45	22
	6288-45/BUAJC	45	22
64K × 1	6287-35/BXAJC	35	22
	6287-35/BUAJC	35	22
	6287-45/BXAJC	45	22
	6287-45/BUAJC	45	22

Military 6164

8K x 8-Bit Fast Static Random Access Memory

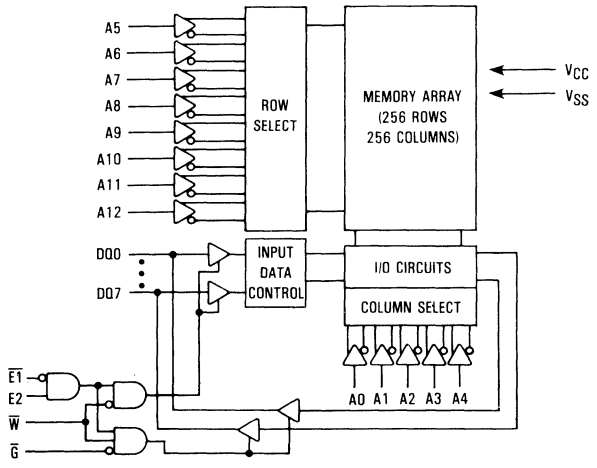
The 6164 is a 65,536-bit static random access memory organized as 8192 words of 8 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability.

The chip enable pins ($\overline{E1}$ and E2) are not clocks. Either pin, when asserted false, causes the part to enter a low power standby mode. The part will remain in standby mode until both pins are asserted true again. The availability of active high and active low chip enable pins provides more system design flexibility than single chip enable devices.

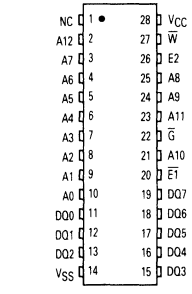
The 6164 is available in a 600 mil, 28-pin ceramic dual-in-line package, and a 32-terminal ceramic LCCC with JEDEC standard pinout.

- Single 5 V Supply, ±10%
- 8K x 8 Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Fast Access Time — 55, 70 ns (Maximum)
- Low Power Dissipation — 660, 495 mW (Maximum, Active)
- Fully TTL Compatible
- Three-State Data Outputs

BLOCK DIAGRAM

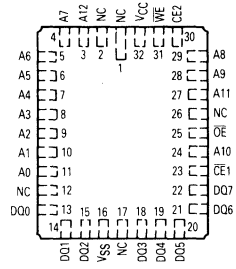


PIN ASSIGNMENT



CASE 733-04
CERAMIC

CHIP CARRIER



CASE 766A-01
CERAMIC

PIN NAMES

A0-A12	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0-DQ7	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground
NC	No Connection

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TRUTH TABLE

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	Supply Current	I/O Pin
H	X	X	X	Not Selected	I_{SB}	High Z
X	L	X	X	Not Selected	I_{SB}	High Z
L	H	H	H	Output Disabled	I_{CC}	High Z
L	H	L	H	Read	I_{CC}	D_{out}
L	H	X	L	Write	I_{CC}	D_{in}

X = don't care

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−55 to +125	°C
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.3*	0.8	V

*V_{IL} (min) = −0.5 Vdc; V_{IL} (min) = −3 Vac (pulse width ≤ 20 ns)

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DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	2	μA
Output Leakage Current ($\overline{E1}$ = V_{IH}, E2 = V_{IL}, or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	2	μA
Power Supply Current +25, +125°C ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, V_{in} = V_{IH} or V_{IL}, I_{out} = 0) −55°C	I_{CC}	— —	90 120	mA
Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL})	I_{SB1}	—	3	mA
Standby Current ($\overline{E1}$ ≥ V_{CC} − 0.2 V or E2 ≤ 0.2 V)	I_{SB2}	—	0.9	mA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1 MHz, T_A = 25°C, sampled at initial device qualification and major redesigns rather than 100% tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	All Inputs Except DQ	C_{in}	10	pF
Input/Output Capacitance	DQ	$C_{I/O}$	12	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

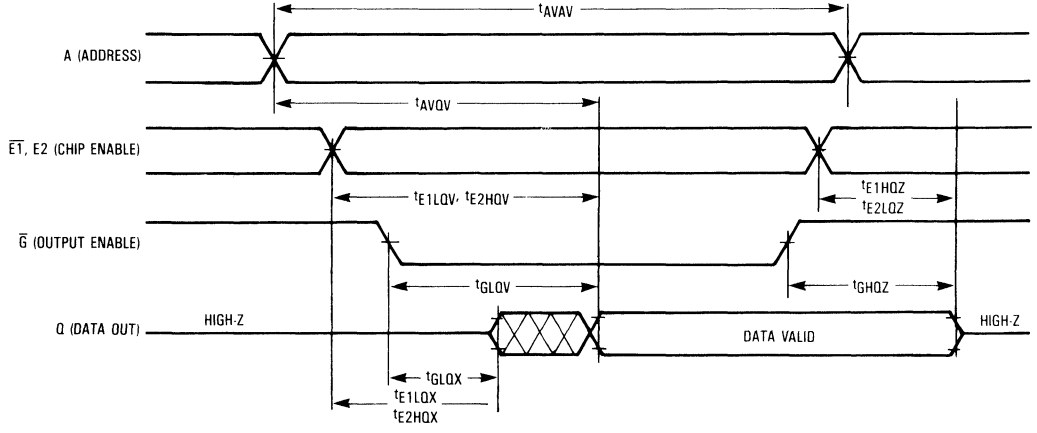
Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels. . . . . 0 to 3 V
Input Rise/Fall Time. . . . . 5 ns

Output Timing Measurement Reference Level . . 0.8 V and 2 V
Output Load . . . . . Figure 1

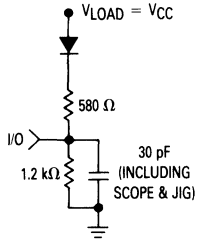
READ CYCLE (See Note 1)

Characteristic	Symbol	Alt Symbol	6164-55		6164-70		Unit	Notes
			Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	55	—	70	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	55	—	70	ns	
$\overline{E1}$ Access Time	t_{E1LQV}	t_{AC1}	—	55	—	70	ns	
E2 Access Time	t_{E2HQV}	t_{AC2}	—	55	—	70	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{OE}	—	50	—	50	ns	
Chip Enable to Output Low-Z	t_{E1LQX}, t_{E2HQX}	t_{CLZ}	10	—	10	—	ns	2
Output Enable to Output Low-Z	t_{GLQX}	t_{OLZ}	5	—	5	—	ns	2
Chip Enable to Output High-Z	t_{E1HQZ}, t_{E2LQZ}	t_{CHZ}	—	35	—	35	ns	2
Output Enable to Output High-Z	t_{GHQZ}	t_{OHZ}	—	35	—	35	ns	2

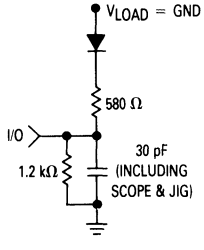
NOTES:
1. $\overline{W}$ is high at all times for read cycles.
2. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.



AC TEST LOADS



(Used for all propagation delay tests except for high to high Z transitions.)



(Used only for propagation tests involving high to high Z transitions or vice versa.)

TIMING LIMITS

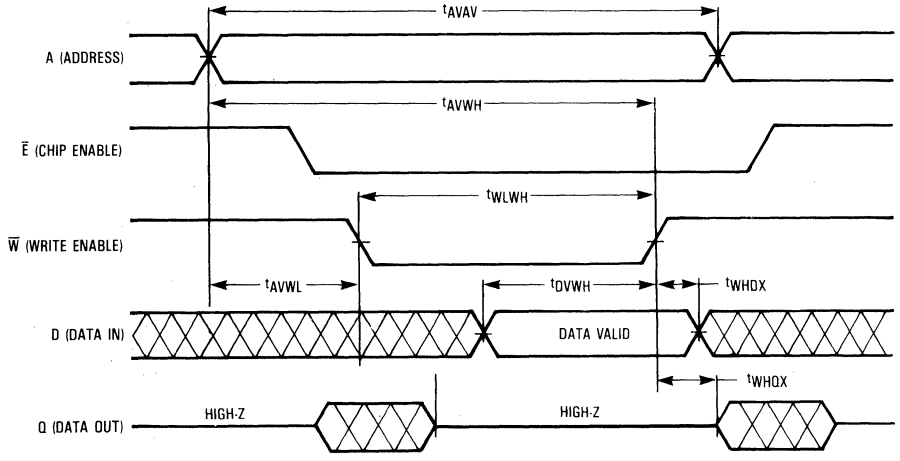
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

9

WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (See Note 1)

Characteristic	Symbol	Alt Symbol	6164-55		6164-70		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	55	—	70	—	ns	
Address Setup Time	t_{AVWL}	t_{AS}	15	—	15	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	50	—	70	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	45	—	60	—	ns	2
Data Valid to End of Write	t_{DVWH}	t_{DW}	30	—	40	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	10	—	10	—	ns	3
Write High to Output Low-Z	t_{WHQX}	t_{WLZ}	5	—	5	—	ns	4

NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. If $\overline{W}$ goes low coincident with or prior to $\overline{E1}$ low or E2 high then the outputs will remain in a high impedance state.
3. During this time the output pins may be in the output state. Signals of opposite phase to the outputs must not be applied at this time.
4. All high-Z and low-Z parameters are considered in a high or low impedance state when the output has made a 500 mV transition from the previous steady state voltage.



9

TYPICAL CHARACTERISTICS

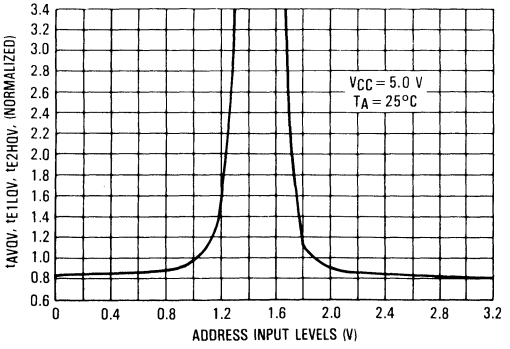
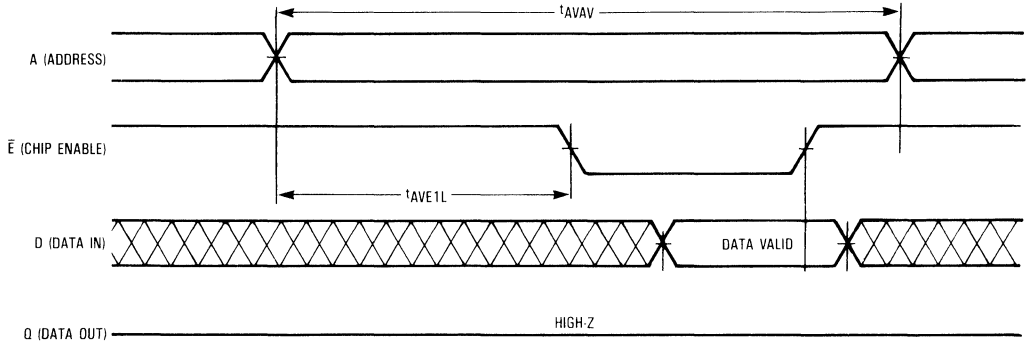


Figure 2. Access Time versus Address Input Levels

WRITE CYCLE 2 (ENABLE CONTROLLED) (See Notes 1 and 2)

Characteristic	Symbol	Alt Symbol	6164-55		6164-70		Unit	Notes
			Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	55	—	70	—	ns	
Address Setup Time	t_{AVE1L}	t_{AS}	0	—	0	—	ns	

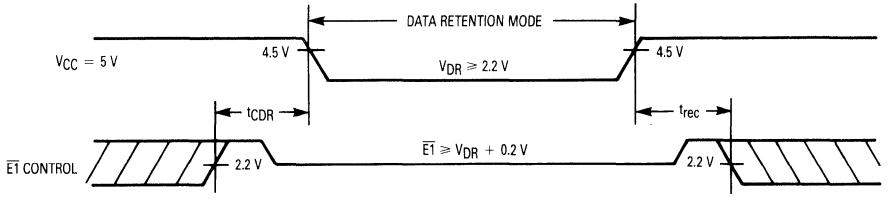
NOTES:
1. A write cycle starts at the latest transition of a low $\overline{E1}$, low $\overline{W}$ or high E2. A write cycle ends at the earliest transition of a high $\overline{E1}$, high $\overline{W}$ or low E2.
2. $\overline{E1}$ and E2 timings are identical when E2 signals are inverted.



LOW V_{CC} DATA RETENTION CHARACTERISTICS (T_A = −55 to +125°C)

Characteristic		Symbol	Min	Max	Unit
V_{CC} for Data Retention ($\overline{E1} \geq 2.2$ V, $V_{in} \geq 2.2$ V)		V_{DR}	2.2	7	V
Data Retention Current (V_{CC} = 2 V, $\overline{E1} \geq 2.2$ V, $V_{in} \geq 2.2$ V)	+25, −55°C +125°C	I_{CCDR}	— —	40 200	μA
Chip Disable to Data Retention Time (see waveform below)		t_{CDR}	0	—	ns
Operation Recovery Time (see waveform below)		t_{rec}	t_{AVAV}*	—	ns

*t_{AVAV} = Read Cycle Time



ORDERING INFORMATION
(Order by Full Part Number)

6164-55 / BXAJC

- Package Type
- Speed
- Part Number

Available Speeds	Available Packages
55 ns	X C-DIP 28 pin
70 ns	U LCCC 32 terminal

Military 6168

4K x 4-Bit Fast Static Random Access Memory

The 6168 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other high speed applications.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This feature provides reduced system power requirements without degrading access time performance.

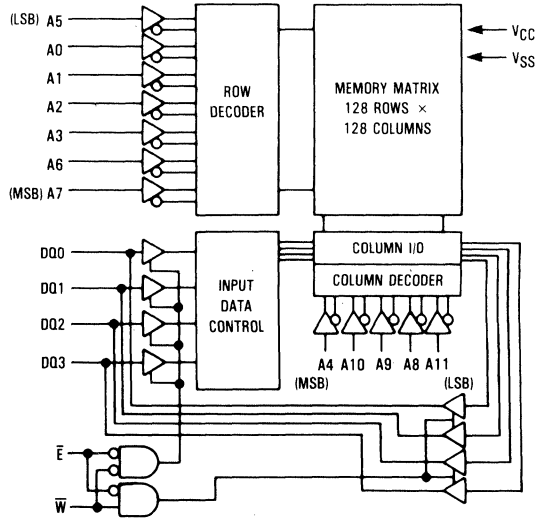
The 6168 is available in a 300 mil, 20 lead ceramic dual-in-line, 20 terminal, rectangular ceramic LCC, and 20-pin ceramic flat packages with the standard JEDEC pinout.

- Single 5 V Supply, ±10%
- 4K x 4 Bit Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Three State Output
- Fast Access Time (Maximum):

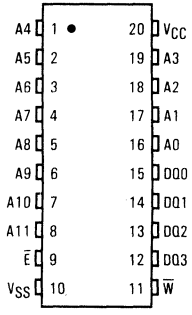
	Address	Chip Enable
6168-55	55 ns	40 ns
6168-70	70 ns	60 ns

- Low Power Operation @ 25°C: 120 mA Max (Active)
  20 mA Max (Standby — TTL Levels)
  0.9 mA Max (Standby — CMOS Levels)
- Fully TTL Compatible

BLOCK DIAGRAM



PIN ASSIGNMENT



CASE 732-03
CERAMIC

CASE 737-02
CERAMIC

CASE 756C-01
CERAMIC

PIN NAMES	
A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

9

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin
H	X	Not Selected	ISB1, ISB2	High-Z
L	H	Read	I_{CC}	D_{out}
L	L	Write	I_{CC}	D_{in}

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−55 to +125	°C
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V	
Input High Voltage	V_{IH}	2	V_{CC} + 0.3	V	1
Input Low Voltage	V_{IL}	−0.3	0.8	V	1, 2

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Notes
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±2.0	μA	
Output Leakage Current ($\overline{E}$ = V_{IH} or $\overline{W}$ = V_{IL}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±2.0	μA	3
Power Supply Current ($\overline{E}$ = V_{IL}, V_{in} = V_{IL} or V_{IH}, I_{out} = 0 mA)	I_{CC}	—	90	mA	3
TTL Standby Current ($\overline{E}$ = V_{IH})	I_{SB1}	—	20	mA	
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, V_{in} ≤ 0.2 V or ≥ V_{CC} − 0.2 V)	I_{SB2}	—	0.9	mA	
Output Low Voltage (I_{OL} = 8.0 mA)	V_{OL}	—	0.4	V	
Output High Voltage (I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V	

CAPACITANCE (f = 1 MHz, T_A = 25°C, sampled at initial device qualification and major redesigns rather than 100% tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	3	5	pF
	$\overline{E}$		5	7	
I/O Capacitance		$C_{I/O}$	5	7	pF

NOTES:
1. Address rise and fall times while the chip is selected are 50 ns maximum.
2. V_{IL}(min) = −0.3 V dc; V_{IL}(min) = −3.0 V ac (pulse width ≤ 20 ns).
3. Input levels less than −0.3 V or greater than V_{CC} + 0.3 V will cause I/O and power supply currents to exceed maximum rating.

9

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels . . . . . .0 to 3.0 V
Input Rise/Fall Time . . . . . 5 ns

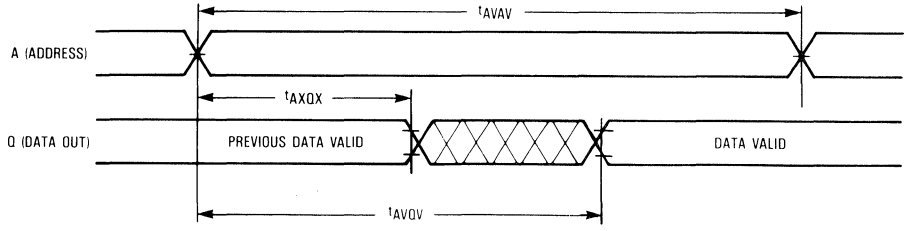
Output Timing Measurement Reference Level . . . . .0.8 and 2.0 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

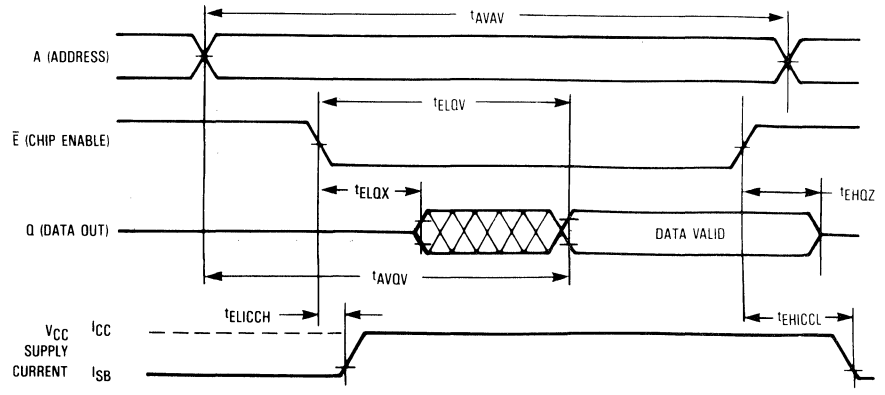
Parameter	Symbol		6168-55		6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	55	—	70	—	ns	
Address Access Time	t_{AVQV}	t_{AA}	—	55	—	70	ns	
$\overline{E}$ Access Time	t_{ELQV}	t_{ACS}	—	55	—	70	ns	
$\overline{E}$ Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	ns	2
$\overline{E}$ High to Output High-Z	t_{EHQZ}	t_{HZ}	0	85	0	30	ns	2
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	—	5	—	ns	
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	55	—	70	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
3. Device is continuously selected ($\overline{E}$ = V_{IL}).
4. Addresses valid prior to or coincident with $\overline{E}$ going low.

READ CYCLE 1 (See Note 3 Above)



READ CYCLE 2 (See Note 4 Above)

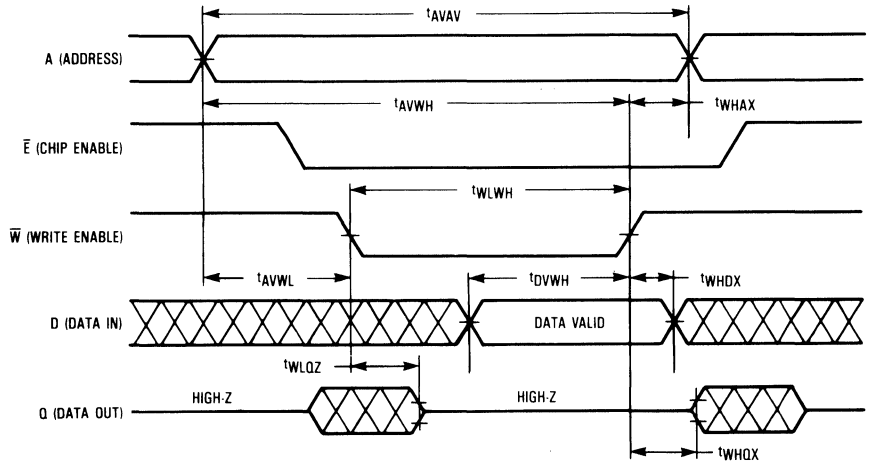


9

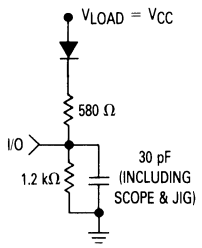
WRITE CYCLE 1 ($\overline{W}$ Controlled; See Note 1)

Parameter	Symbol		6168-55		6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	50	—	60	—	ns	
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	40	—	60	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	40	—	60	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	20	—	30	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	3	—	3	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	—	25	—	30	ns	2
Write High to Output Active	t_{WHQX}	t_{OW}	0	—	0	—	ns	2
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

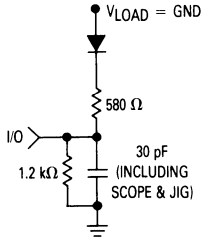
NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.



AC TEST LOADS



(Used for all propagation delay tests except for high to high Z transitions.)



(Used only for propagation tests involving high to high Z transitions or vice versa.)

TIMING LIMITS

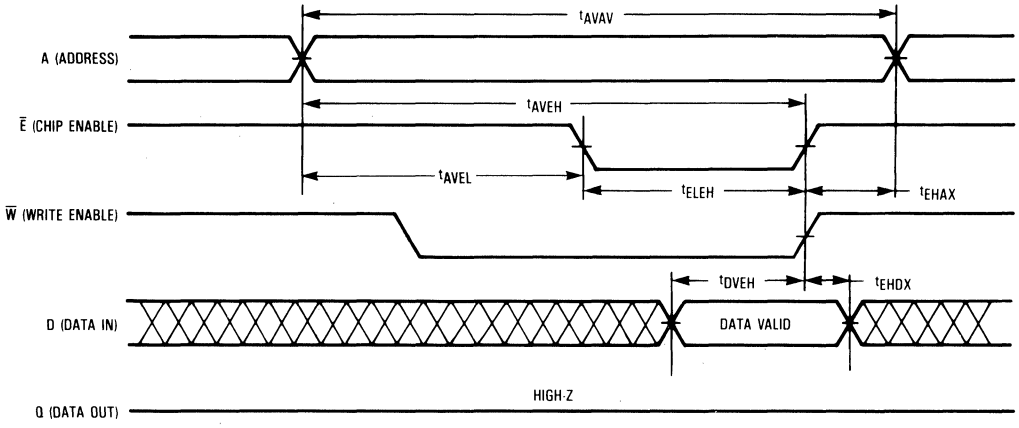
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

9

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		6168-55		6168-70		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	50	—	60	—	ns	
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	40	—	60	—	ns	
Write Pulse Width	t_{ELEH}	t_{CW}	45	—	60	—	ns	2, 3
Data Valid to End of Write	t_{DVEH}	t_{DW}	20	—	30	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	3	—	3	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
3. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



ORDERING INFORMATION
(Order by Full Part Number)

6168-55 / BRAJC

- Package Type
- Speed
- Part Number

Available Speeds	Available Packages
55 ns	R C-DIP 20 pin
70 ns	Y C-FLAT 20 pin
	U LCCC 20 terminal

Military 6268

4K x 4-Bit Fast Static Random Access Memory

The 6268 is a 16,384-bit static random access memory organized as 4096 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides greater reliability. Fast access time makes this device suitable for cache and other sub-50 ns applications.

The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

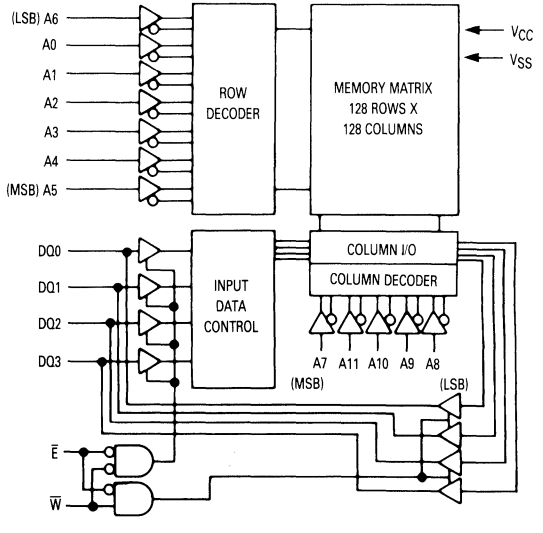
The 6268 is available in a 20-lead ceramic dual-in-line, 20-terminal ceramic LCCC, and a 20-pin ceramic flat package and features the standard JEDEC pinout.

- Single 5 V Supply, ±10%
- 4K x 4 Bit Organization
- Fully Static — No Clock or Timing Strobes Necessary
- Three State Output
- Fully TTL Compatible
- Fast Access Time (Maximum):

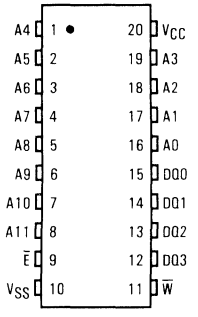
	Address	Chip Enable
6268-35	35 ns	35 ns
6268-45	45 ns	45 ns

- Low Power Operation: 120 mA Maximum, Active AC
  5 mA Maximum, Standby (TTL Levels)
  2 mA Maximum, Standby (Full Rail)

BLOCK DIAGRAM



PIN ASSIGNMENT



CASE 732-03
CERAMIC

CASE 737-02
CERAMIC

CASE 756C-01
CERAMIC

PIN NAMES	
A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
DQ0-DQ3	Data Input/Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

9

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	I/O Pin	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	D_{in}	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1	W
Temperature Under Bias	T_{bias}	−55 to +125	°C
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	0.8	V

*V_{IL} (min) = −0.5 Vdc; V_{IL} (min) = −3 Vac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	2	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	2	μA
AC Supply Current (I_{out} = 0 mA)	I_{CCA}	—	120	mA
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	5	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	2	mA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1 MHz, T_A = 25°C, sampled at initial device qualification and major redesigns rather than 100% tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	—	6	pF
	$\overline{E}$		—	6	
I/O Capacitance		$C_{I/O}$	—	7	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

Input Reference Level . . . . . 1.5 V
Input Pulse Levels. . . . . 0 to 3 V
Input Rise/Fall Time. . . . . 5 ns

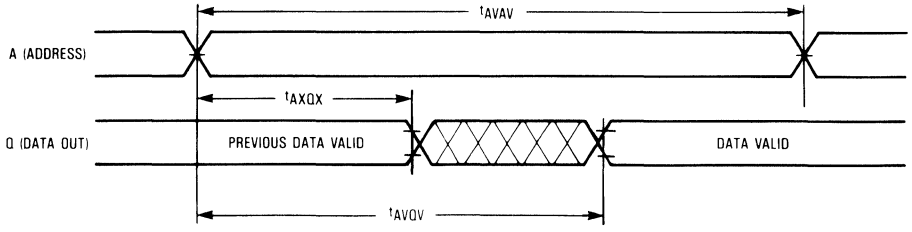
Output Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

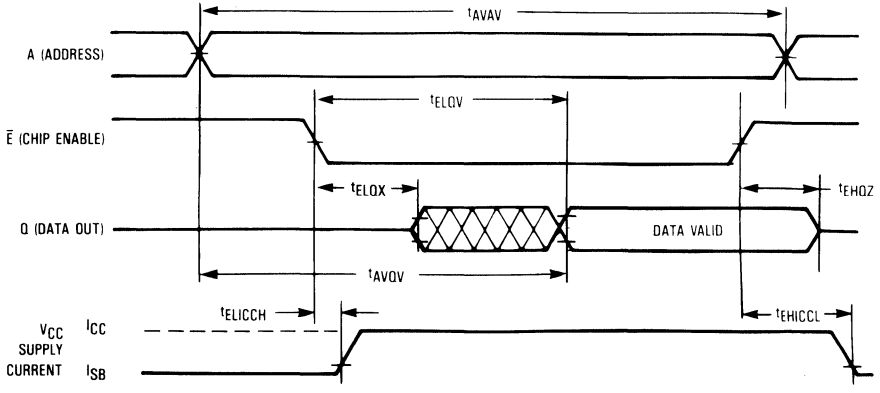
Parameter	Symbol		6268-35		6268-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	35	—	45	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	35	—	45	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	ns	3,4
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	15	0	20	ns	3,4
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	35	—	45	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
4. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
5. Device is continuously selected ($\overline{E}$ = V_{IL}).
6. Addresses valid prior to or coincident with $\overline{E}$ going low.

READ CYCLE 1 (See Note 5 Above)



READ CYCLE 2 (See Note 6 Above)



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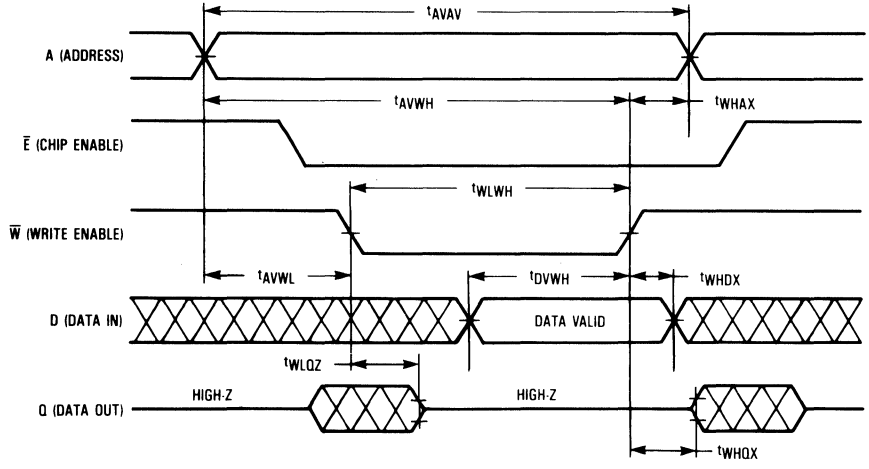
WRITE CYCLE 1 ($\overline{W}$ Controlled; See Note 1)

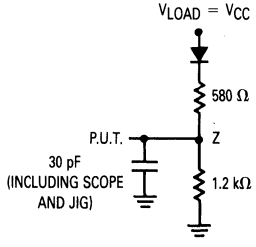
Parameter	Symbol		6268-35		6268-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	30	—	35	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	30	—	30	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	3	—	3	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	—	15	—	20	ns	3,4
Write High to Output Active	t_{WHQX}	t_{OW}	0	—	0	—	ns	3,4
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. At any given voltage and temperature, t_{WLQZ} max, is less than t_{WHQX} min, both for a given device and from device to device.

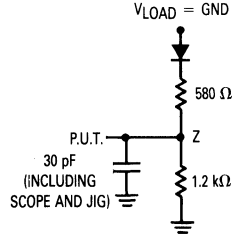


9

AC TEST LOADS



a) Test circuit used for propagation delay tests except for V_{OH} to high-Z transitions.



b) Use only for V_{OH} to high-Z and high-Z to V_{OH} transitions.

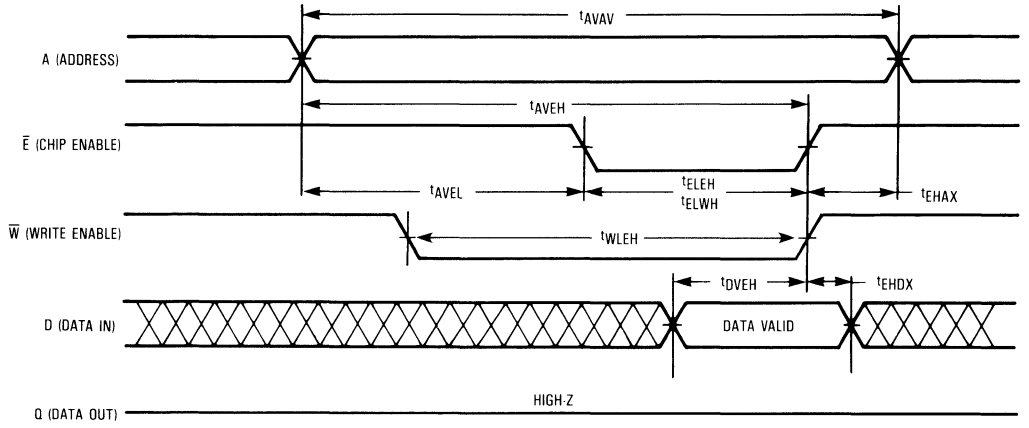
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		6268-35		6268-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	30	—	35	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	30	—	35	—	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	30	—	30	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	3	—	3	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



9

ORDERING INFORMATION
(Order by Full Part Number)

6268-35 / BRAJC

- Package Type
- Speed
- Part Number

Available Speeds	Available Packages
35 ns	R C-DIP 20 pin
45 ns	Y C-FLAT 20 pin
	U LCCC 20 terminal

Military 6287

64K x 1-Bit Fast Static Random Access Memory

The 6287 is a 65,536-bit static random access memory organized as 65,536 words of 1 bit, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

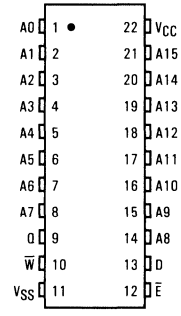
The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features provide reduced system power requirements without degrading access time performance.

The 6287 is available in a 300 mil, 22-pin sidebraze, and a 22-terminal ceramic leadless chip carrier measuring 290 x 490 mils. All feature JEDEC standard pinouts.

- Single 5 V ±10% Power Supply
- Fast Access Time: 35/45 ns
- Equal Address and Chip Enable Access Time
- Low Power Operation: 120 mA Maximum, Active AC
  5 mA Maximum, Standby (TTL Levels)
  2 mA Maximum, Standby (Full Rail)
- Fully TTL Compatible
- Three-State Data Output

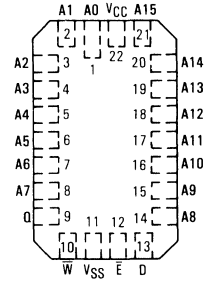
PIN ASSIGNMENT

SIDEBRAZE



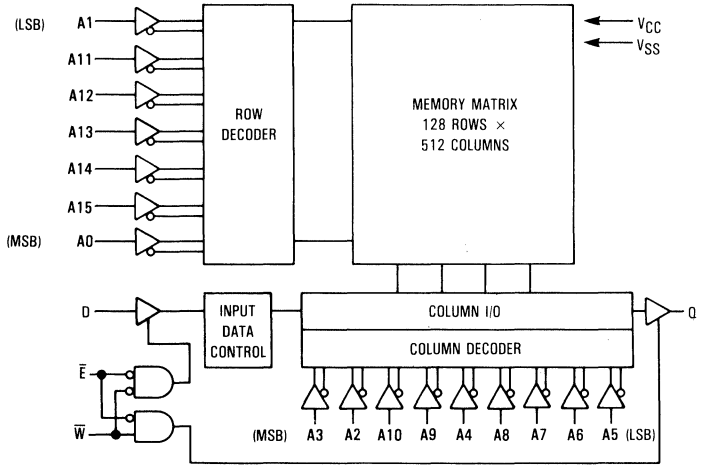
CASE 736-05
CERAMIC

CHIP CARRIER



CASE 800-02
CERAMIC

BLOCK DIAGRAM



PIN NAMES	
A0–A15	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

9

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC} +0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A = 25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−55 to +125	°C
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature—Ceramic	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	0.8	V

*V_{IL} (min) = −0.5 Vdc; V_{IL} (min) = −3 Vac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	±1	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	±1	μA
AC Supply Current (I_{out} = 0 mA)	I_{CCA}	—	120	mA
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	5	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	2	mA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, sampled at initial device qualification and major redesigns rather than 100% tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	—	6	pF
	$\overline{E}$		—	7	
Output Capacitance		C_{out}	—	7	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels. . . . . 0 to 3 V
Input Rise/Fall Time. . . . . 5 ns

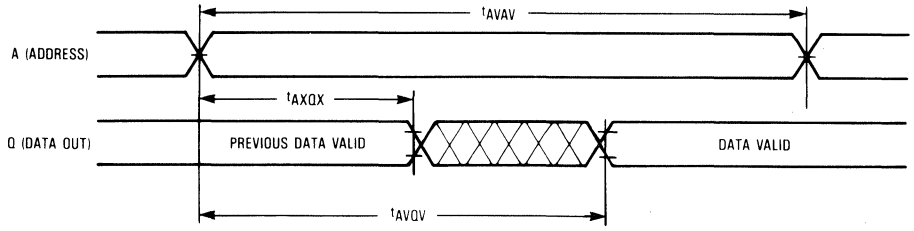
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

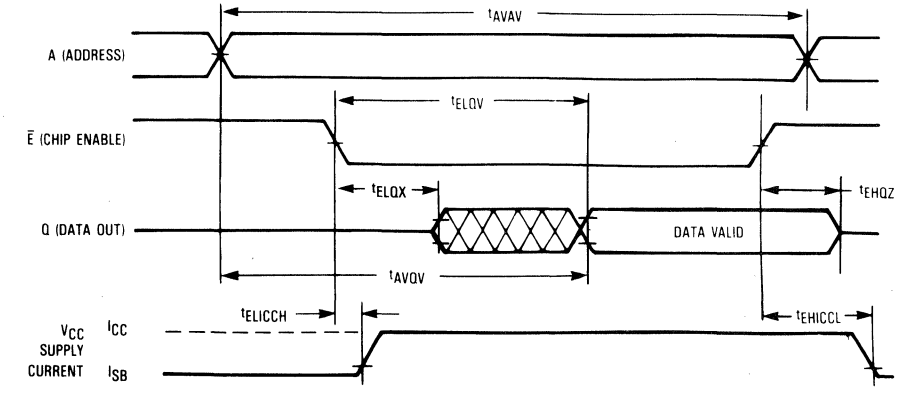
Parameter	Symbol		6287-35		6287-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	35	—	45	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	35	—	45	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	ns	4,5
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	15	0	20	ns	4,5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	35	—	45	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. Device is continuously selected ($\overline{E}$ = V_{IL}).

READ CYCLE 1 (See Note 6 Above)



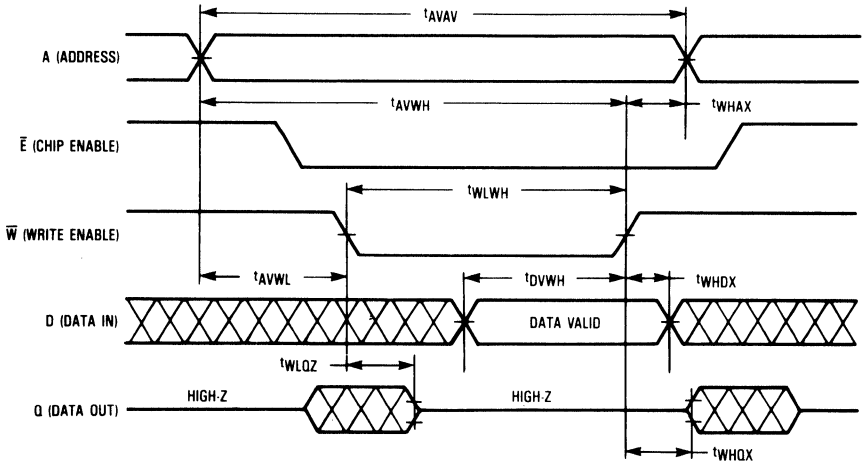
READ CYCLE 2 (See Note 3 Above)



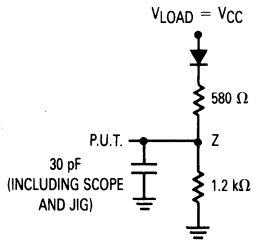
WRITE CYCLE 1 ($\overline{W}$ Controlled; See Note 1)

Parameter	Symbol		6287-35		6287-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	30	—	35	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	30	—	30	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	3	—	3	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	15	0	20	ns	3
Write High to Output Active	t_{WHQX}	t_{OW}	0	—	0	—	ns	3
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

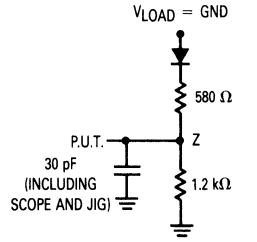
NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.



AC TEST LOADS



a) Test circuit used for propagation delay tests except for V_{OH} to high-Z transitions.



b) Use only for V_{OH} to high-Z and high-Z to V_{OH} transitions.

TIMING LIMITS

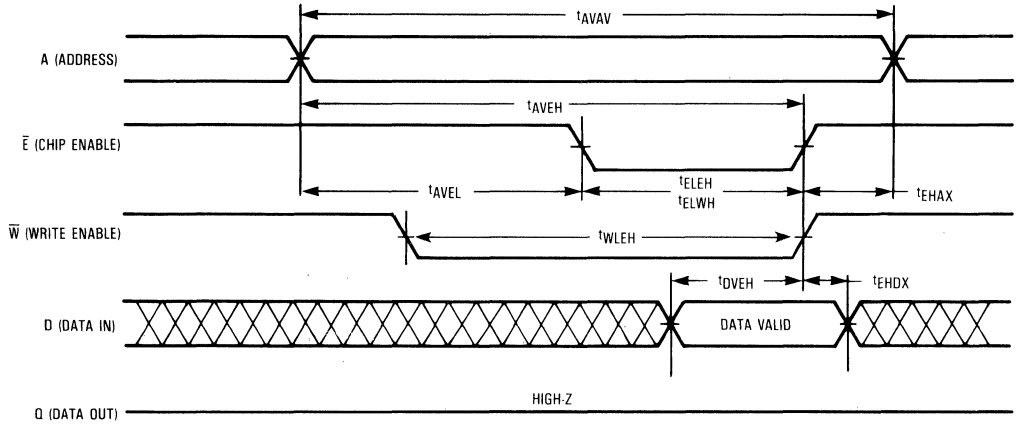
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

9

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		6287-35		6287-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	30	—	35	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	30	—	35	—	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	30	—	30	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	3	—	3	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



9

ORDERING INFORMATION
(Order by Full Part Number)

6287-35 / BXAJC

- Package Type
- Speed
- Part Number

Available Speeds	Available Packages		
35 ns	X	Sidebraze	22 pin
45 ns	U	LCCC	22 terminal

Military 6288

16K x 4-Bit Fast Static Random Access Memory

The 6288 is a 65,536-bit static random access memory organized as 16,384 words of 4 bits, fabricated using Motorola's second-generation high-performance silicon-gate CMOS (HCMOS III) technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption for greater reliability.

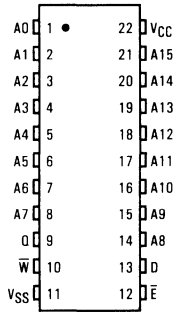
The chip enable ($\overline{E}$) pin is not a clock. In less than a cycle time after $\overline{E}$ goes high, the part enters a low-power standby mode, remaining in that state until $\overline{E}$ goes low again. This device also incorporates internal power down circuitry that will reduce active current for less than 100% duty cycle applications. These features reduce system power requirements without degrading access time performance.

The 6288 is available in a 300 mil, 22-pin sidebraze, and a 22-terminal ceramic leadless chip carrier measuring 290 x 490 mils. All feature JEDEC standard pinouts.

- Single 5 V ±10% Power Supply
- Fast Access Time: 35/45 ns
- Equal Address and Chip Enable Access Time
- Low Power Operation: 120 mA Maximum, Active AC
  5 mA Maximum, Standby (TTL Levels)
  2 mA Maximum, Standby (Full Rail)
- Fully TTL Compatible
- Three-State Data Output

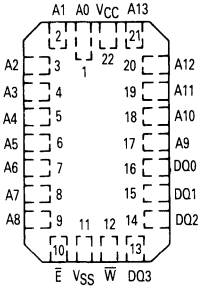
PIN ASSIGNMENT

SIDEBRAZE



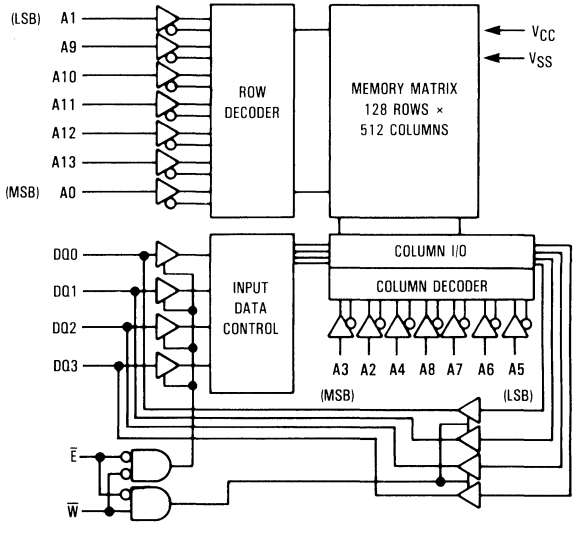
CASE 736-05
CERAMIC

CHIP CARRIER



CASE 800-02
CERAMIC

BLOCK DIAGRAM



PIN NAMES	
A0–A15	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	+5 V Power Supply
V_{SS}	Ground

9

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	Not Selected	ISB1, ISB2	High-Z	—
L	H	Read	I_{CC}	D_{out}	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	−0.5 to +7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	−0.5 to V_{CC}+0.5	V
Output Current (per I/O)	I_{out}	±20	mA
Power Dissipation (T_A=25°C)	P_D	1.0	W
Temperature Under Bias	T_{bias}	−55 to +125	°C
Operating Temperature	T_A	−55 to +125	°C
Storage Temperature	T_{stg}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	−0.5*	0.8	V

*V_{IL} (min) = −0.5 Vdc; V_{IL} (min) = −3 Vac (pulse width ≤ 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	2	μA
Output Leakage Current ($\overline{E}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	2	μA
AC Supply Current (I_{out} = 0 mA)	I_{CCA}	—	120	mA
TTL Standby Current ($\overline{E}$ = V_{IH}, No Restrictions on Other Inputs)	I_{SB1}	—	5	mA
CMOS Standby Current ($\overline{E}$ ≥ V_{CC} − 0.2 V, No Restrictions on Other Inputs)	I_{SB2}	—	2	mA
Output Low Voltage (I_{OL} = 8 mA)	V_{OL}	—	0.4	V
Output High Voltage (I_{OH} = −4 mA)	V_{OH}	2.4	—	V

CAPACITANCE (f = 1 MHz, dV = 3 V, T_A = 25°C, sampled at initial device qualification and major redesigns rather than 100% tested)

Characteristic		Symbol	Min	Max	Unit
Input Capacitance	All Inputs Except $\overline{E}$	C_{in}	—	6	pF
	$\overline{E}$		—	7	
I/O Capacitance		$C_{I/O}$	—	7	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5 V ±10%, T_A = −55 to +125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level . . . . . 1.5 V
Input Pulse Levels. . . . . 0 to 3 V
Input Rise/Fall Time. . . . . 5 ns

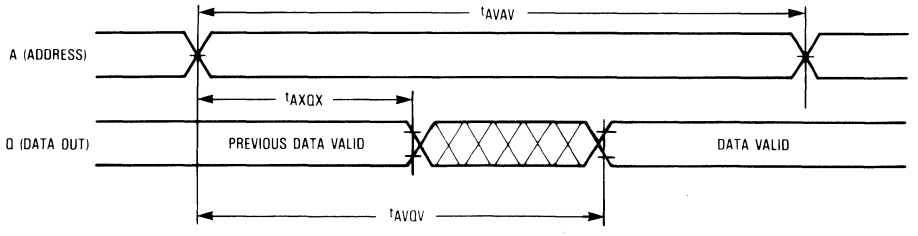
Output Timing Measurement Reference Level . . . . . 1.5 V
Output Load . . . . . Figure 1A Unless Otherwise Noted

READ CYCLE (See Note 1)

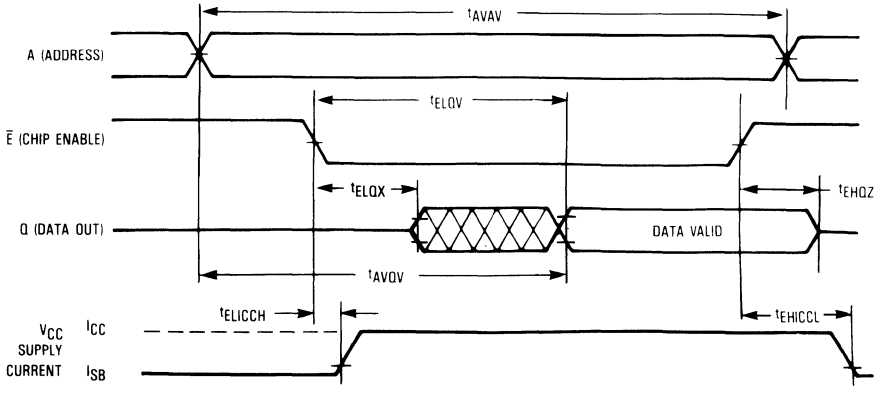
Parameter	Symbol		6288-35		6288-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	35	—	45	—	ns	2
Address Access Time	t_{AVQV}	t_{AA}	—	35	—	45	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	35	—	45	ns	3
Output Hold from Address Change	t_{AXQX}	t_{OH}	3	—	3	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	—	5	—	ns	4,5
Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	15	0	20	ns	4,5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	35	—	45	ns	

NOTES:
1. $\overline{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{E}$ going low.
4. At any given voltage and temperature, t_{EHQZ} max, is less than t_{ELQX} min, both for a given device and from device to device.
5. Transition is measured ±500 mV from steady-state voltage with load of Figure 1B.
6. Device is continuously selected ($\overline{E}$ = V_{IL}).

READ CYCLE 1 (See Note 6 Above)



READ CYCLE 2 (See Note 3 Above)



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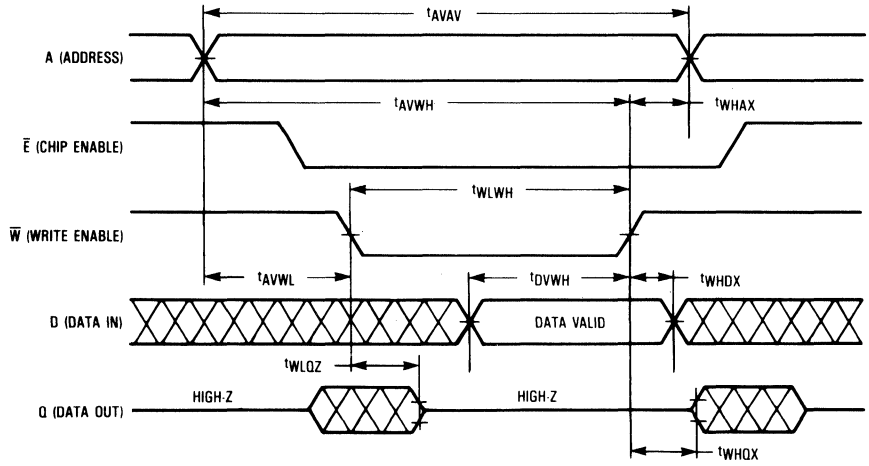
WRITE CYCLE 1 ($\overline{W}$ Controlled; See Note 1)

Parameter	Symbol		6288-35		6288-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	30	—	35	—	ns	
Write Pulse Width	t_{WLWH}	t_{WP}	30	—	30	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	15	—	15	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	3	—	3	—	ns	
Write Low to Output High-Z	t_{WLQZ}	t_{WZ}	0	15	0	20	ns	3,4
Write High to Output Active	t_{WHQX}	t_{OW}	0	—	0	—	ns	3,4
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady-state voltage with load in Figure 1B.
4. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.



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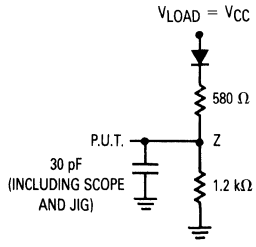
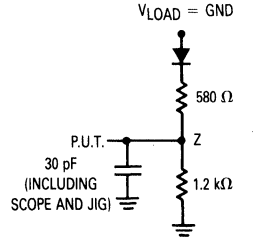
AC TEST LOADS



a) Test circuit used for propagation delay tests except for V_{OH} to high-Z transitions.



b) Use only for V_{OH} to high-Z and high-Z to V_{OH} transitions.

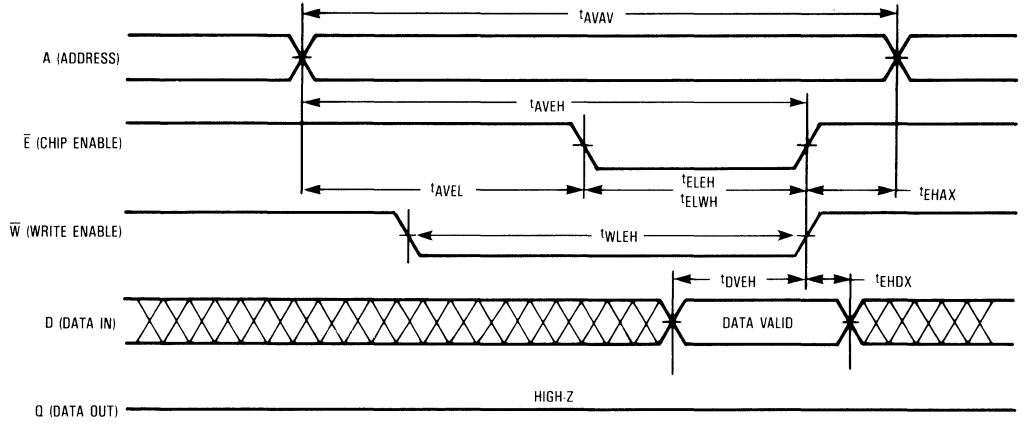
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WRITE CYCLE 2 ($\overline{E}$ Controlled; See Note 1)

Parameter	Symbol		6288-35		6288-45		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	30	—	40	—	ns	2
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	30	—	35	—	ns	
Enable to End of Write	t_{ELEH}	t_{CW}	30	—	35	—	ns	3,4
Write Pulse Width	t_{WLEH}	t_{WP}	30	—	30	—	ns	
Data Valid to End of Write	t_{DVEH}	t_{DW}	15	—	15	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	3	—	3	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
4. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.



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ORDERING INFORMATION
(Order by Full Part Number)

6288-35 / BXAJC

- Package Type
- Speed
- Part Number

Available Speeds	Available Packages		
35 ns	X	Sidebraze	22 pin
45 ns	U	LCCC	22 terminal

Reliability Information 10

CORPORATE QUALITY STATEMENT

MOTOROLA CORPORATE QUALITY GOAL

IMPROVE PRODUCT AND SERVICES QUALITY TEN TIMES BY 1989
AND AT LEAST ONE HUNDRED FOLD BY 1991.

ACHIEVE SIX SIGMA CAPABILITY BY 1992.

With a deep sense of urgency, spread dedication to quality to every facet of the corporation and achieve a culture of continual improvement to ASSURE TOTAL CUSTOMER SATISFACTION. There is only one ultimate goal: zero defects in everything we do.

signed:

BOB GALVIN
Chairman

BILL WEISZ
Vice Chairman

JOHN MITCHELL
President

GEORGE FISHER
Deputy to Chief
Executive Office

GARY TOOKER
Chief to Corporate
Staff Officer

JACK GERMAIN
Motorola Director
of Quality

JIM LINCICOME
Government Electronics
Group

CARL LINDHOLM
International
Operations

LEVY KATZIR
New Enterprises

JIM NORLING
Semiconductor Products
Sector

STEVE LEVY
Japanese Operations

DON JONES
Chief Financial
Officer

JIM DONNELLY
Personnel

RAY FARMER
Communications Sector

ED STAIANO
General Systems
Group

GERHARD SCHULMEYER
Automotive & Industrial
Electronics Group

DIVISION QUALITY STATEMENT

MOTOROLA MOS MEMORY PRODUCTS DIVISION

COMMITMENT TO SIX SIGMA
WORLD CLASS

The Memory Products Division staff are pleased to announce our commitment to be a World Class MOS Memory supplier. This means more bullet proof designs which can tolerate handling, processes at the limit and beyond, and outstanding control of the manufacturing processes such that a product design which is marginal will still yield consistent quality performance.

Memory Products Division fully endorses the Motorola Corporate goal of improving product and service quality ten times by 1989 and one hundred fold by 1991.

Through our quality improvement process using SIX SIGMA we can and will accomplish being the best memory supplier through WORLD CLASS product margins and services in their truest sense.

ENDORSEMENTS:

Jim George | Bud Broeker | Bill Bowers | Jim Eachus

Weldon Knape | Roger Kung | Bill Lane | Jon Rodgers

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SIX SIGMA

MOTOROLA

OUR SIX SIGMA CHALLENGE

WHAT IS SIX SIGMA?

Six Sigma is the required capability level to approach the Standard. The Standard is Zero Defects. Our goal is to be best-in-class in Product, Sales, and Service.

WHY SIX SIGMA?

The performance of a product is determined by how much margin exists between the design requirements of its characteristics (and those of its parts/steps), and the actual value of those characteristics. These characteristics are produced by processes in the factory, and at the suppliers.

Each process attempts to reproduce its characteristics identically from unit to unit, but within each process some variation does occur. For some processes, such as those which use real-time feedback to control the outcome, the variation is quite small, and for others it may be quite large.

Variation of the process is measured in Standard Deviations (Sigma) from the Mean. The normal variation, defined as process width, is ±3 Sigma about the mean.

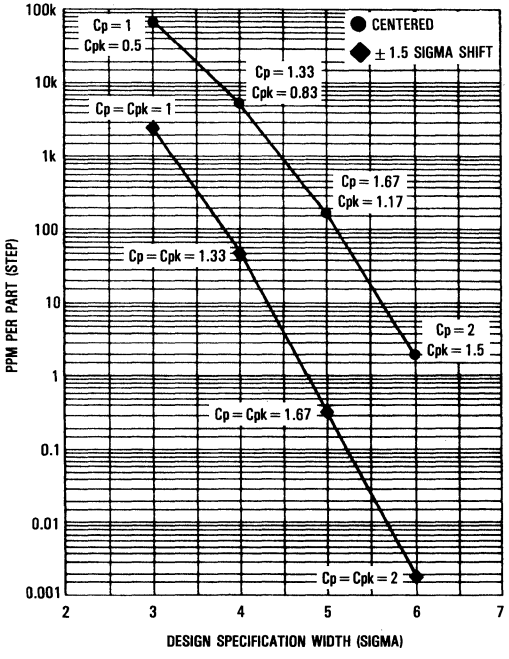

Figure 1. Standard Deviations from Mean

Approximately 2,700 parts per million parts/steps will fall outside the normal variation of ±3 Sigma, see Figure 1. This, by itself, does not appear disconcerting. However, when we build a product containing 1,200 parts/steps, we can expect 3.24 defects per unit (1200 × 0.0027), on an average. This would result in a rolled yield of less than 4%, which means fewer than 4 units out of every hundred would go through the entire manufacturing process without a defect, see Table 1.

Thus, we can see that for a product to be built virtually defect-free, it must be designed to accept characteristics that are significantly more than ±3 Sigma away from the Mean.

It can be shown that a design that can accept **twice the normal variation** of the process, or ±6 Sigma, can be expected to have no more than 3.4 parts per million defective for each characteristic, even if the process mean were to shift by as much as ±1.5 Sigma, see Figure 1. To quantify this, Capability Index (Cp) is used, where:

$$Cp = \frac{\text{design specification width}}{\text{process width}}$$

Table 1. Rolled Yield

TOTAL DEFECTS PER UNIT	ROLLED THROUGHPUT YIELD (%)
5.3	0.5
4.6	1.0
3.9	2.0
3.5	3.0
3.2	4.0
3.0	5.0
2.3	10
1.9	15
1.6	20
1.4	25
1.2	30
1.0	37
0.9	40
0.8	45
0.7	50
0.6	55
0.51	60
0.43	65
0.36	70
0.29	75
0.22	80
0.16	85
0.10	90
0.05	95
0.00	100

ROLLED THROUGHPUT YIELD (%) = $100\ e^{-d/u}$

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A design specification width of ±6 Sigma and a process width of ±3 Sigma yields a Cp of 12/6 = 2. However, as shown in Figure 2, the process mean can shift. When the process mean is shifted with respect to the design mean, the Capability Index is adjusted with a factor k, and becomes Cpk. Cpk = Cp(1 − k), where:

$$k = \frac{\text{process shift}}{\text{design specification width/2}}$$

The k factor for ±6 Sigma design with a 1.5 Sigma process shift = 1.5/(12/2) = 0.25, and the Cpk = 2(1 − 0.25) = 1.5.

In the same case of a product containing 1,200 parts/steps, we would now expect only 0.0041 defects per unit (1200 × 0.0000034). This would mean that 996 units out of 1,000 would go through the entire manufacturing process without a defect (see Table 2).

It is, therefore, our five year goal to achieve ±6 Sigma capability in Product, Sales, and Service.

Table 2. Overall Yield vs Sigma (Distribution Shifted ±1.5 σ)

NUMBER OF PARTS (STEPS)	±3 σ (%)	±4 σ (%)	±5 σ (%)	±6 σ (%)
1	93.32	99.379	99.9767	99.99966
7	61.63	95.733	99.839	99.9976
10	50.08	93.96	99.768	99.9966
20	25.08	88.29	99.536	99.9932
40	6.29	77.94	99.074	99.9864
60	1.58	68.81	98.614	99.9796
80	0.40	60.75	98.156	99.9728
100	0.10	53.64	97.70	99.966
150	–	39.38	96.61	99.949
200	–	28.77	95.45	99.932
300	–	15.43	93.26	99.898
400	–	8.28	91.11	99.864
500	–	4.44	89.02	99.830
600	–	2.38	86.97	99.796
700	–	1.28	84.97	99.762
800	–	0.69	83.02	99.729
900	–	0.37	81.11	99.695
1000	–	0.20	79.24	99.661
1200	–	0.06	75.88	99.593
3000	–	–	50.15	98.985
17000	–	–	0.02	94.384
38000	–	–	–	87.880
70000	–	–	–	78.820
150000	–	–	–	60.000

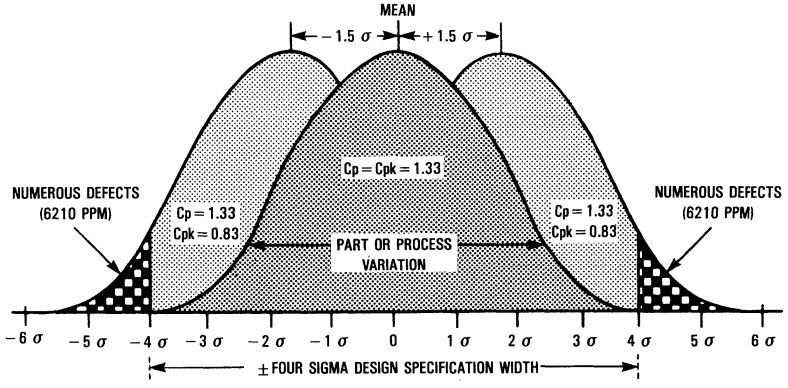

Figure 2a. Four Sigma Capability

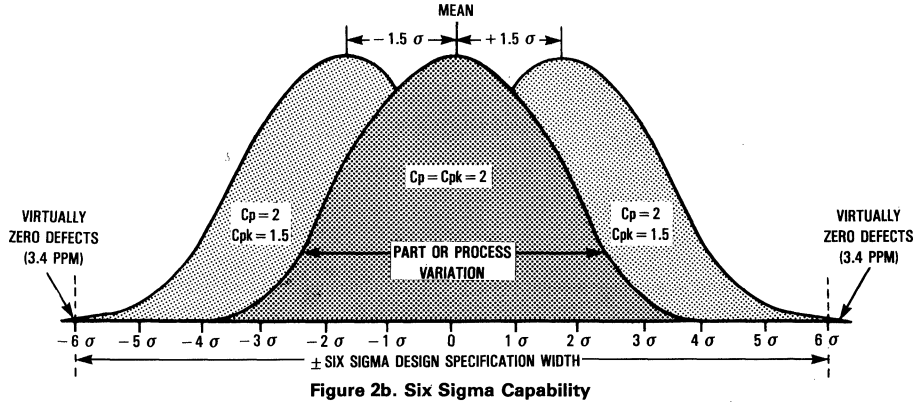

Figure 2b. Six Sigma Capability

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QUALITY MONITORING

Average Outgoing Quality (AOQ) refers to the number of devices per million that are outside specification limits at the time of shipment. Motorola has continually improved its outgoing quality, and has established a goal of zero PPM (parts per million) AOQ. This level of quality will lead to vendor certification programs with many of our customers. The program ensures a certain level of quality, thus allowing a customer to either reduce or eliminate the need for incoming inspections.

By paying strict attention to quality at an early stage, the possibility of failures occurring further down the line is greatly minimized. Motorola's electrical parametric testing eliminates devices that do not conform to electrical specification. Additional parametric testing on a sample basis provides data for continued improvement.

AVERAGE OUTGOING QUALITY (AOQ) CALCULATION

$$\text{AOQ in PPM} = (\text{Process Average}) \cdot (\text{Lot Acceptance Rate}) \cdot (10^6)$$

$$\text{Process Average} = \frac{\text{Total Projected Reject Devices}^*}{\text{Total Number of Devices}}$$

$$\text{Projected Reject Devices} = \frac{\text{Defects in Sample}}{\text{Sample Size}} \cdot \text{Lot Size}$$

$$\text{Total Number of Devices} = \text{Sum of all the units in each submitted lot}$$

$$\text{Lot Acceptance Rate} = 1 - \frac{\text{Number of Lots Rejected}}{\text{Number of Lots Tested}}$$

10^6 = Conversion to parts per million (PPM)

MARKING PERMANENCY, HERMETICITY, AND SOLDERABILITY MONITORS

Marking permanency testing is performed per Motorola specification. The procedure involves soaking the device in various solvents, brushing the markings, and then inspecting the markings for legibility.

Hermeticity monitoring includes tests for both fine and gross leaks in the hermetic package seal.

Solderability testing is used to ensure that device leads can be soldered without voids, discoloration, flaking, dewetting, or bridging. Typically, the test specifies steam preconditioning followed by a 235° to 260°C solder dip and microscope inspection of the leads.

RELIABILITY MONITORING

Motorola recognizes the need to monitor established MOS Memory products to maintain the level of quality and reliability demonstrated through the internal and joint qualification processes. Motorola maintains a system of monitor programs that provide monthly feedback on the extensive matrix of Motorola fabrication, assembly, and testing technologies that produce our products. As with qualification activity, great care is taken to assure the accuracy and quality of the data generated.

*All rejects: visual, mechanical, and electrical (dc, ac, and high/low temperature).

RELIABILITY STRESS TESTS

The following summary gives brief descriptions of the various reliability tests included in both reliability qualification and monitor programs. Not all of the tests listed are performed by each program and other tests can be performed when appropriate. Refer to Table 3.

Table 3. Stresses and Typical Stress Conditions

Stress	Typical Stress Condition
High Temperature Operating Life, Dynamic or Static	125°C, 6.0 V
Temperature Cycle	−65°C to +150°C Air to Air
Thermal Shock	−65°C to +150°C Liquid to Liquid
Temperature Humidity Bias	85°C, 85% RH, 5.0 V
Autoclave	121°C, 100% RH, 15 psig
Pressure Temperature Humidity Bias	148°C, 90% RH, 44 psig, 5.0 V
Low Temperature Operating Life	0°C/25°C, 6.0 V

HIGH TEMPERATURE OPERATING LIFE

High temperature operating life (HTOL or HTRB) testing is performed to accelerate failure mechanisms that are thermally activated through the application of extreme temperatures and the use of biased operating conditions. The temperature and voltage conditions used in the stress will vary with the product being stressed. However, the typical stress ambient is 125°C with the bias applied equal to or greater than the data sheet nominal value. All devices used in the HTOL test are sampled directly after final electrical test with no prior burn-in or other prescreening unless called out in the normal production flow. Testing can either be performed with dynamic signals applied to the device or in a static bias configuration.

TEMPERATURE CYCLE

Temperature cycle testing accelerates the effects of thermal expansion mismatch among the different components within a specific die and packaging system. This test is typically performed per MIL-STD-883 or MIL-STD-750 with the minimum and maximum temperatures being −65°C and +150°C. During temperature cycle testing, devices are inserted into a cycling system and held at the cold dwell temperature for at least ten minutes. Following this cold dwell, the devices are heated to the hot dwell where they remain for another ten minute minimum time period. The system employs a circulating air environment to assure rapid stabilization at the specified temperature. The dwell at each extreme, plus the two transition times of five minutes each (one up to the hot dwell temperature, another down to the cold dwell temperature), constitute one cycle. Test duration for this test will vary with device and packaging system employed.

THERMAL SHOCK

The objective of thermal shock testing is the same as that for temperature cycle testing—to emphasize differences in expansion coefficients for components of the packaging system. However, thermal shock provides additional stress in that

the device is exposed to a sudden change in temperature due to the transfer time of ten seconds maximum as well as the increased thermal conductivity of a liquid ambient. This test is typically performed per MIL-STD-883 or MIL-STD-750 with the minimum and maximum temperatures being −65°C and +150°C. Devices are placed in a fluorocarbon bath and cooled to minimum specified temperature. After being held in the cold chamber for five minutes minimum, the devices are transferred to an adjacent chamber filled with fluorocarbon at the maximum specified temperature for an equivalent time. Two five-minute dwells plus two ten-second transitions constitute one cycle.

TEMPERATURE HUMIDITY BIAS

Temperature humidity bias (THB or H^3TRB) is an environmental test performed at a temperature of 85°C and a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated circuits. A nominal static bias is applied to the device to create the electrolytic cells necessary to accelerate corrosion of the metallization.

AUTOCLAVE

Autoclave is an environmental test which measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Conditions employed during the test include 121°C, 100% relative humidity, and 15 psig. Corrosion of the die is the expected failure mechanism. Autoclave is a highly accelerated and destructive test.

PTHB (PRESSURE-TEMPERATURE-HUMIDITY-BIAS)

This test is performed to accelerate the effects of moisture penetration with the dominant effect being corrosion. The test detects similar failure mechanisms as THB but at a greatly accelerated rate. Conditions usually employed during the test are a temperature of 148°C, pressure of 44 psig or greater, a relative humidity of 90 (PTHB), and a bias level which is the nominal rating of the device.

LOW TEMPERATURE OPERATING LIFE

This test is performed primarily to accelerate hot carrier injection effects in semiconductor devices by exposing them to room ambient or colder temperatures with the use of biased operating conditions. Threshold shifts or parametric changes are typically the basis for failure. The length of this test will vary with temperature and bias conditions employed.

SYSTEM SOFT ERROR

System soft error is designed to detect errors caused by impact ionization of silicon by high energy particles. This stress is performed on a system level basis. The system is operated for millions of device hours to obtain an accurate measure of actual system soft error performance.

MECHANICAL SHOCK

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand a sudden change in mechanical stress typically due to abrupt changes in motion as seen in handling, transportation, or actual use. The typical test condition would be as follows: acceleration = 1500 g, orientation = Y1 plane, t = 0.5 ms, and number of pulses = 5.

VARIABLE FREQUENCY VIBRATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to examine the ability of the device to withstand deterioration due to mechanical resonance. The typical test condition is: peak acceleration = 20 g, frequency range = 20 Hz to 20 kHz, and t = 48 minutes.

CONSTANT ACCELERATION

This test is typically performed per MIL-STD-883 or MIL-STD-750 and is used to indicate structural or mechanical weaknesses in a device/packaging system by applying a severe mechanical stress. A typical test condition used is as follows: stress level = 30 kg, orientation = Y1 plane, and t = 1 minute.

QUALITY SYSTEMS

A Global Quality System is key to achieving our goal of "Best In Class". Quality systems are implemented in wafer fabrication, assembly, final test, and distribution world wide. Figure 3 depicts Quality Assurance involvement and the techniques applied in the general flow of product and Figure 4 shows Memory Manufacturing locations world wide.

	QUALITY ASSURANCE TECHNIQUES			
	SAMPLING	SPC	MONITOR	AUDIT
INCOMING (WAFERS, CHEMICALS, ETC.)	X	X	X	X
WAFER FAB	X	X	X	X
ASSEMBLY	X	X	X	X
BURN-IN/TEST	X	X	X	X
DISTRIBUTION	X	X	X	X

Figure 3. General Product Flow

Direct Customer interaction ensures that they are receiving product that meets all of their requirements 100% of the time. In fact, the MOS Memories Reliability and Quality Assurance department has devised a customer advocate list that assigns key Reliability and Quality Assurance personnel to specific customers in order to facilitate any inquiry a particular customer may have with regard to quality, reliability, or any other issue they may want to discuss.

All processes and activities that relate to the manufacturing of MOS Memories are fully documented, and regular audits are performed to ensure continuous adherence to proper procedures. We are always striving to produce and reproduce the highest quality product available throughout the world.

MOS Memory Products Division promotes the concept of statistical process controls throughout the entire manufacturing process. This is exemplified by our commitment to in-depth statistical process control training programs for everyone—from the line operator to upper management. Favorable results have already been realized from the initial phases of implementation, with much more to follow.

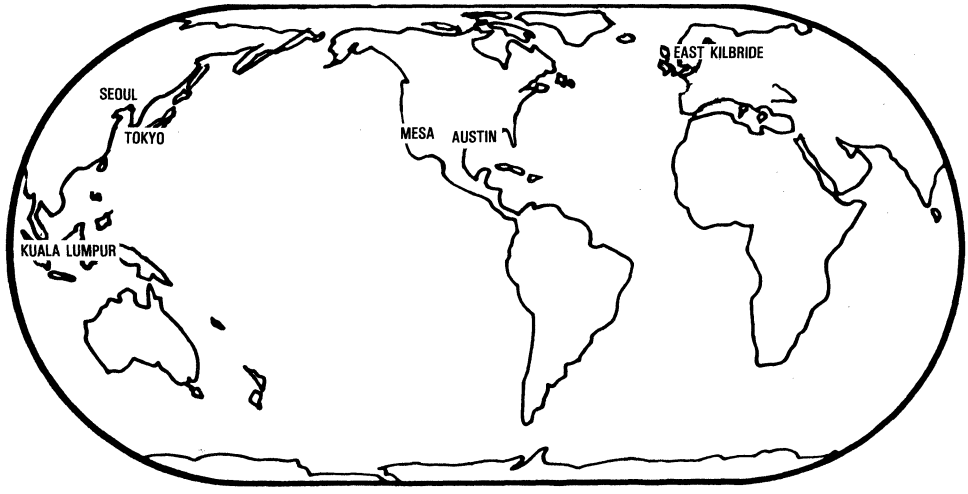

Figure 4. Wafer Fab/Assembly/Final Test Locations

MOS Memory Products Division maintains a World Wide Quality Assurance system that is second to none. Daily status reports are received from remote locations, and any problems that arise are tackled on real-time basis. MOS Memory Products Division is also a leader in accurate and efficient methods of quality data collection and reporting.

Every unit that MOS Memory Products Division produces is coded so that complete traceability is maintained, including visibility to the wafer and assembly lot level. The Quality System ensures that we can provide any specific processing information to our customers on request.

INTERNAL QUALIFICATION DISCIPLINE

Motorola recognizes the need to establish that all MOS Memory devices, both new products as well as existing ones, reach and maintain a level of quality and reliability that is unsurpassed in the electronics marketplace. To ensure this, internal qualification requirements, procedures, and methods as well as vendor qualification specifications have been developed. These activities are intended to provide a consistent, comprehensive, and methodical approach to device qualification and to improve our customer's understanding of Motorola's qualification results and their subsequent application implications.

For qualification results to be valid and acceptable, the collected data must be proved accurate to the highest possible confidence level. Therefore, a complete device history and data log is kept with any lost or missing data potentially leading to test results that are unusable for qualification purposes. Testing conditions and pass/fail criteria are established before stressing begins. Strict adherence to this and the use of control devices insure that the test results are valid and meaningful.

New MOS Memory devices which are under development or in the prototype stage are subject to requirements defined for the three levels of the development cycle. These levels are the alpha, beta, and introductory phases of device development. Each phase contains guidelines and controls concerning issues such as device labeling, number of customers, sample quantities, pricing and stocking levels, and open-order-entry timing. Decisions regarding these items are made jointly by marketing, product, and reliability personnel.

JOINT QUALIFICATION

As a result of the rigorous discipline used for internal qualification of Motorola MOS Memory products, our customers can benefit from joint qualification type activities. Motorola's clearly defined qualification procedures improve the customer's ability to comprehend Motorola's qualification results in an effective manner which aides in their qualification decision making process. Through parallel qualification activities between Motorola and its customers, this procedure can cut qualification costs by reducing duplication of effort, improving resource utilization, and shortening introduction cycle time. This helps to ensure competitive edge advantages for our customers.

Joint Qualification activities result in a partnership type of interaction between Motorola and its customers on an engineering level. This assists our customers in two critical areas. First, it allows them to understand more clearly the strengths and weaknesses of Motorola's products. Secondly, our customers can make clear decisions concerning which stresses they need to concentrate on during their internal qualification activities.

HISTORICAL PERFORMANCE

Over the course of the last five years, significant achievements have been made on quality and delivery performance. The ± SIX SIGMA capability process will assist the MOS Memory Products Division in pursuit of our standard of zero defects and 100% on time delivery.

Figure 5 indicates the product Average Outgoing Quality performance as measured in parts per million. Figure 6 is the delivery performance as measured against the internal Motorola schedule date.

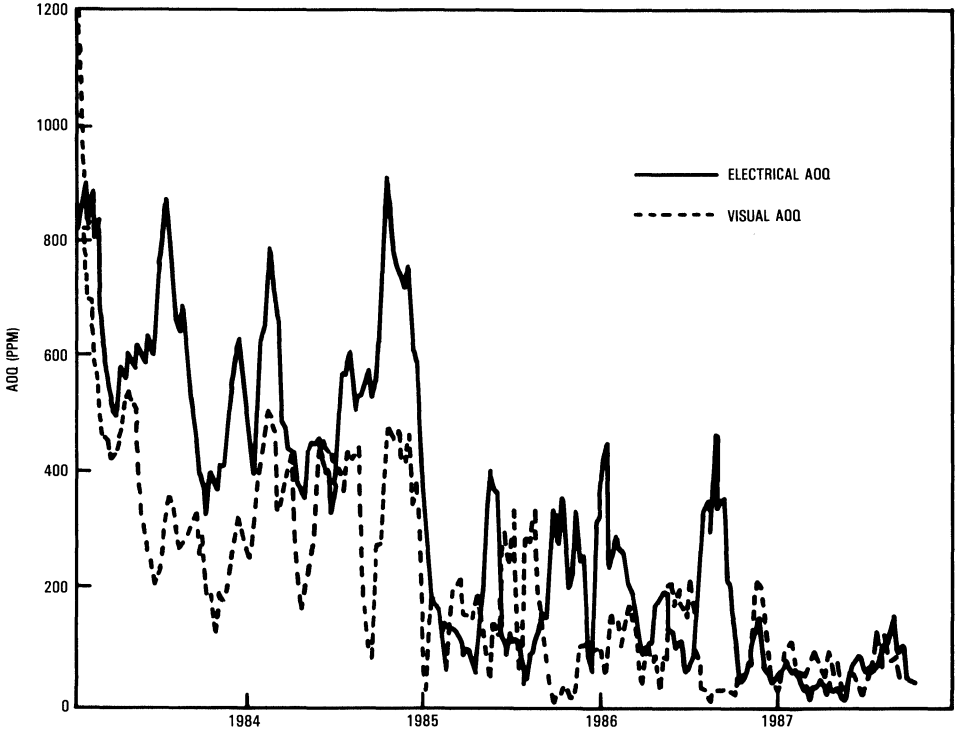

Figure 5. Motorola MOS Memory Products Division Average Outgoing Quality—4 Week Average World Memory

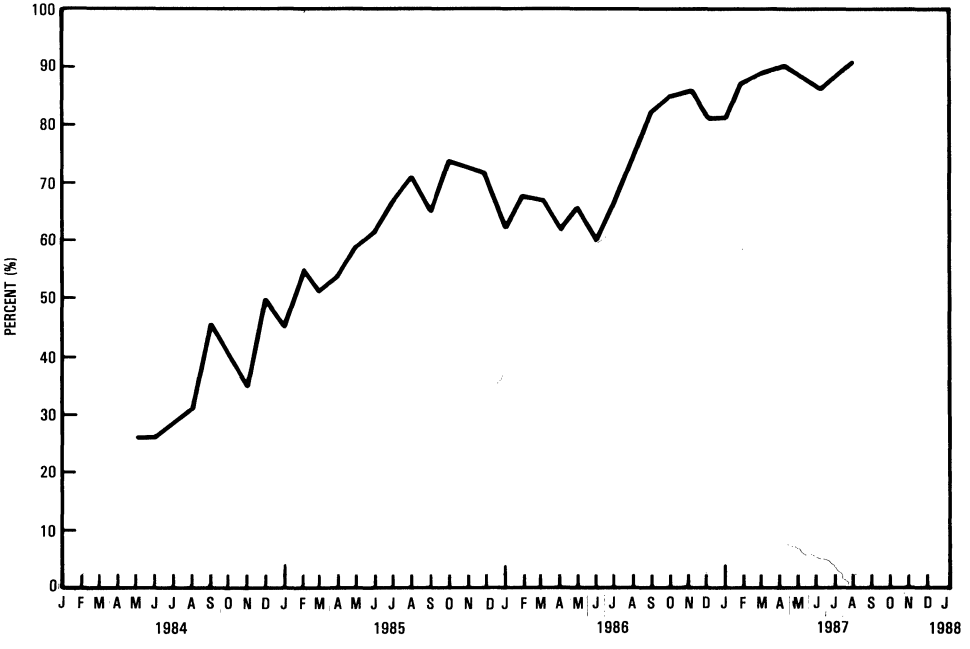

Figure 6. MOS Memory Products Division On-Time Delivery

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Applications Information 11

AN987

DRAM Refresh Modes

DRAMs offer the lowest cost per bit of any memory, and for that reason are enormously popular in a wide range of applications. This low cost per bit is achieved with a very simple bit cell design, among other things, but rooted in this simplicity are some inherent drawbacks. One major limitation is the need to refresh each memory bit at regular intervals. This note discusses what refresh is, the reasons refresh is required for DRAM operation, and the various types of refresh available on the Motorola 1M × 1 and 256K × 4 DRAMs. Specific comments refer to the 1M × 1 85-ns DRAM. Refer to specific device data sheets for analogous information on other devices.

The heart of any memory device is the bit cell. A 1M DRAM has 1,048,576 of these cells in the memory array. Each cell holds a single bit of information in the form of a high or low voltage, where high voltage = a binary "1" and low voltage = a binary "0". The DRAM bit cell consists of one transistor and one capacitor. The transistor acts as a switch, regulating when the capacitor will charge and discharge, while the capacitor stores a high or low voltage charge.

All capacitors leak over time, slowly losing the charge stored in them, regardless of how carefully they are constructed. Junction and dielectric leakage are two capacitor discharge paths that are characteristic of the DRAM bit cell, and both are affected by temperature. The capacitor in the bit cell can hold a small charge, on the order of 35-125 fF ($fF = 1 \times 10^{-15}$ farads). As this charge dissipates through leakage paths, the small difference between a "1" and a "0" diminishes. If nothing is done to restore the charge on the capacitor to its initial value, the sensing circuitry on the DRAM will eventually be unable to detect a charge difference and will read the cell as a "0".

Thus, all the capacitors in the memory array must be periodically recharged, or refreshed. Refresh is accomplished by accessing each row in the array, one row at a time. When a row is accessed, it is turned on, and voltage is applied to the row, recharging each capacitor on the row to its initial value. Specified refresh time on the 1M × 1 DRAM is 8 milliseconds; every row must be recharged every 8 milliseconds. This is a vast improvement over refresh times required for earlier generations of DRAMs. The 16K × 1 DRAM required refresh every 2 milliseconds, the 256K × 1 DRAM requires a refresh every 4 milliseconds. Longer refresh times mean more time available for access to memory, and less time required to refresh the device.

Design and operation of the DRAM allow only one row to be refreshed at a time; 512 refresh cycles are required to refresh the entire 1M × 1 memory array. The array is actually 1024 rows by 1024 columns, but it operates electrically like two half arrays of 512 rows by 1024 columns. During refresh, every row is treated as if it runs through both halves of the array, refreshing 2048 column locations (bit cells) per row. This design results in fewer refresh cycles required to recharge the entire array, since only 512 rows need to be accessed, rather than 1024.

Refresh can be performed in either a single **burst** of 512 consecutive refresh cycles (one cycle per row) every 8 milliseconds, or **distributed** over time, one refresh cycle every 15 microseconds (8 milliseconds per 512 rows = 15.6 microseconds per row) on average, or some combination of these two extremes. As long as every row is refreshed within 8 milliseconds, the actual method used is best determined by system use of the DRAM. The burst takes 84 microseconds to complete (165 nanoseconds per row × 512 rows for 85 nanoseconds per device). During this burst refresh time, no memory operations can be performed on the device. Distributed refresh disables memory access for 165 nanoseconds every 15 microseconds.

The 1M × 1 DRAM can be refreshed in three ways: $\overline{RAS}$ only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, and hidden refresh. In addition, any normal read or write refreshes all 2048 bit cells on the row accessed. Regardless of the refresh method used, the time required to refresh one row is the random read or write ($\overline{RAS}$) cycle time (t_{RC}). When operating the device in page, nibble, or static column mode, only the row being accessed is refreshed. The device must be in normal random mode to utilize any of these specific refresh methods.

$\overline{RAS}$ only refresh requires external row counters, to ensure all rows are refreshed within the specified time, and externally-supplied row addresses. $\overline{CAS}$ before $\overline{RAS}$ relies on internal row counters and internally generates the address of the next row to be refreshed. Hidden refresh is a variation on $\overline{CAS}$ before $\overline{RAS}$ refresh that holds valid data at the output while refresh is occurring. Whenever the device is in a refresh cycle, neither a read nor a write operation can be performed. Hidden refresh allows the device to be read ahead of refresh, then holds the valid data at the output while refresh cycles are in progress. It appears that the refresh is hidden among data cycles because valid data is maintained at the output.

$\overline{RAS}$ only refresh is performed by supplying row addresses A0-A8 and completing a $\overline{RAS}$ cycle (t_{RC}); switching $\overline{RAS}$ from inactive (high) to active (low), holding $\overline{RAS}$ low (t_{RAS}), then switching back to high, and holding $\overline{RAS}$ high (t_{RP}). A9 is ignored during $\overline{RAS}$ only refresh, since this address normally determines which half of the array is to be accessed. $\overline{CAS}$ must be held high through this $\overline{RAS}$ cycle, hence the name $\overline{RAS}$ only refresh. An external row counter is required for this refresh method. See Figure 1.

$\overline{CAS}$ before $\overline{RAS}$ refresh is performed by switching $\overline{CAS}$ from high to low while $\overline{RAS}$ is high, then switching $\overline{RAS}$ low (t_{CSR}). This reversal of the usual clock order activates an internal row counter that generates addresses to be refreshed; external addresses are ignored in this cycle. $\overline{CAS}$ must be held low (t_{CHR}) after $\overline{RAS}$ transitions to low. After that time it can either be held low or switched to high. See Figure 2. The $\overline{CAS}$ before $\overline{RAS}$ refresh counter test, specified on all DRAM data sheets that offer this type of refresh, is used to check for proper operation of the internal row counters and correct address generation.

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Hidden refresh is a $\overline{CAS}$ before $\overline{RAS}$ refresh that has been initiated during a read or write operation. At the end of a typical read cycle, $\overline{CAS}$ would be switched to high before $\overline{RAS}$, turning off the output. In a hidden refresh cycle, $\overline{RAS}$ is switched to high, concluding the $\overline{RAS}$ cycle (t_{RC}), while $\overline{CAS}$ is held low. $\overline{RAS}$ is held high (t_{RP}), then switched low, beginning another $\overline{RAS}$ cycle. As long as $\overline{CAS}$ is held low, data is valid at the output, resulting in a long read cycle. Since data can be read while the device is being refreshed, the refresh operation(s) appears to be hidden by the read cycle. The same refresh can be performed after a write cycle is initiated. This method of refresh allows refresh cycles to be mixed within read and write cycles. During the refresh cycle, a write operation cannot be performed. See Figure 3.

Refresh is an integral and necessary part of DRAM operation. Substantial improvement has been made in increasing the time between refresh cycles, but as long as the bit cell design utilizes a capacitor, periodic recharging will be required. Three methods of refresh are available on the 1M × 1 DRAM: $\overline{RAS}$ only, $\overline{CAS}$ before $\overline{RAS}$, and hidden refresh. The Motorola 1M × 1 and 256K × 4 will work in virtually all systems as a result of flexibility provided by this assortment of refresh methods.

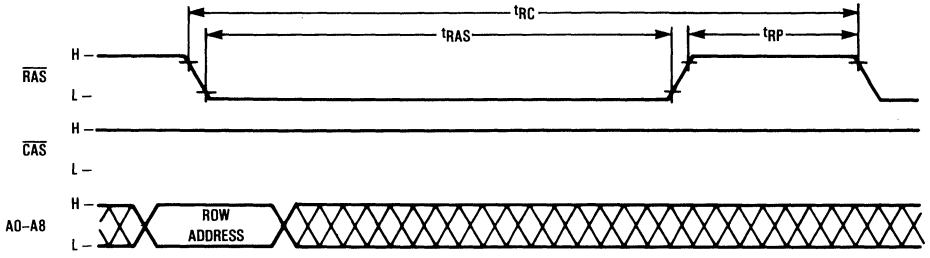

Figure 1. $\overline{RAS}$ Only Refresh Cycle

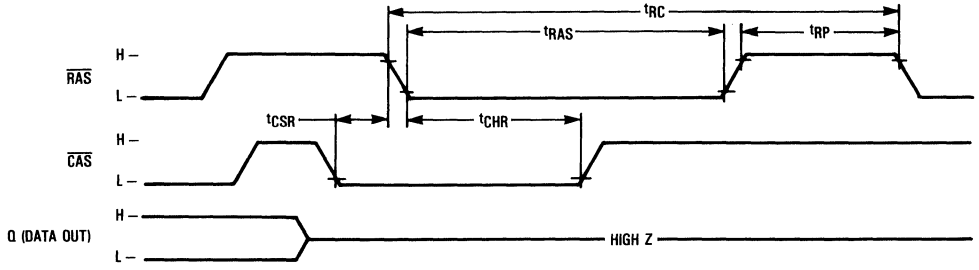

Figure 2. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

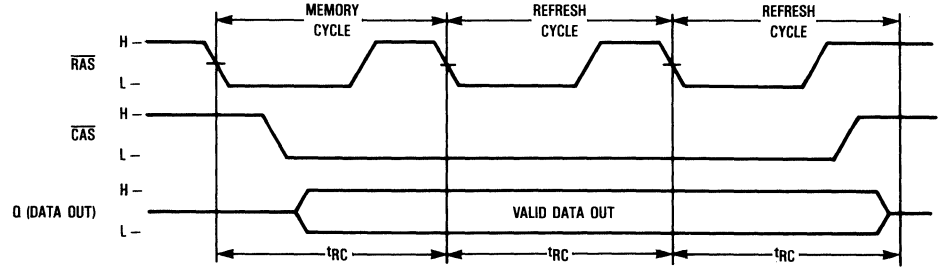

Figure 3. Hidden Refresh Cycle

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Page, Nibble, and Static Column Modes: High-Speed, Serial-Access Options on 1M-Bit + DRAMs

The 1M-bit and higher density DRAMs offered by Motorola, in addition to operating in a standard mode at advertised access times, have special operating modes that will significantly decrease access time. These are page, nibble, and static column modes. All three modes are available in the 1M × 1 configuration; page and static column modes are also available on the 256K × 4 configuration. Read, write, and read-write operations can be mixed and performed in any order while these devices are operating in either random or special mode.

The comments that follow refer specifically to successive read operations for page, nibble, and static column modes on the 1M × 1 device. The read operation is chosen for sake of simplicity in illustrating these special operating modes. However, decreased access times will occur for all operations, performed in any order, when the device is operated in any of these modes. General operating comments apply to the 256K × 4 device as well.

All of these special operating modes are useful in applications that require high-speed serial access. Typical examples include video bit map graphics monitors or RAM disks. Page mode is the standard, available since the days of the 16K × 1 DRAM. Static column is the latest mode to be made available on DRAMs, and nibble mode first appeared somewhere in between. Page and static column offer the same column location access, but operate somewhat differently. Nibble is unlike either of the other modes, but faster than both in its niche. All modes are initiated after a standard read or write is performed.

Page and static column modes allow access to any of 1024 column locations on a specific row, while nibble allows access to a maximum of four bits. The location of the first bit in nibble mode determines the other bits to be accessed. Nibble mode allows the fastest access of the three devices (t_{NCAC}), all other parameters held equal, at about 1/4 the standard (t_{RAC}) rate. Page and static column access times (t_{CAC}, t_{AA}) are, respectively, about 1/3 and 1/2 the standard rate.

Cycle time is a better indicator of relative speed improvement, since it measures the minimum time between any two successive reads. Cycle time is approximately 1/4 for nibble and 1/3 for page and static column modes, with respect to a

Table 1. Operating Characteristic Comparison

Parameter		Page	Nibble	Static Column	Random
Access Time (ns)*	t_{CAC}	25	—	—	—
	t_{NCAC}	—	20	—	—
	t_{AA}	—	—	45	—
	t_{RAC}	—	—	—	85
Cycle Time (ns)*	t_{PC}	50	—	—	—
	t_{NC}	—	40	—	—
	t_{SC}	—	—	50	—
	t_{RC}	—	—	—	165
Accessible Bits		1024	4	1024	All
Order of Accessible Bits		Random	Fixed	Random	Random
Conditions	$\overline{RAS}$	Active	Active	Active	Cycle
	$\overline{CAS}$ or $\overline{CS}$**	Cycle	Cycle	Active	Cycle
	Addresses	Cycle	N/A	Cycle	Cycle
	Outputs	Cycle	Cycle	Active	Cycle
Time to Read 4 Bits (ns)*		235	205	235	660
Time to Read 1024 Unique Bits (ns)*		51,235	70,400	51,235	168,960

*Values for a 1M × 1 85-ns device.

**$\overline{CS}$ on Static Column.

Page:
4 bit read = $t_{RAC} + 3t_{PC}$
1024 bit read = $t_{RAC} + 1023t_{PC}$

Nibble:
4 bit read = $t_{RAC} + 3t_{NC}$
1024 bit read = $256 \cdot (t_{RAC} + 3t_{NC} + t_{RP})$

Static Column:
4 bit read = $t_{RAC} + 3t_{SC}$
1024 bit read = $t_{RAC} + 1023t_{SC}$

Random:
4 bit read = $4t_{RC}$
1024 bit read = $1024t_{RC}$

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random cycle time of 165 nanoseconds. When operated in these high-speed modes, users will typically access most or all of the bits available to that mode, once the mode has been initiated. Thus the best measure of speed for nibble mode is the rate at which four bits are read, while the rate at which 1024 bits are read is the best measure of page or static column mode. When the actual operating conditions are considered, as described elsewhere, the difference between t_{CAC}, t_{NCAC}, and t_{AA} measurements hold relatively little significance.

Page mode is slightly more difficult to interface in a system than static column mode due to extra $\overline{CAS}$ pulses that are required in page mode. Static column generates less noise than page mode, because output buffers and $\overline{CS}$ are always active in this mode. Noise transients, generated every time $\overline{CAS}$ is cycled from inactive to active, are thus eliminated in the static column mode.

PAGE MODE

Page mode allows faster access to any of the 1024 column locations on a given row, typically at one third the standard (t_{RAC}) rate for randomly-performed operations. Page mode consists of cycling the $\overline{CAS}$ clock from active (low) to inactive (high) and back, and providing a column address, while holding the $\overline{RAS}$ clock active (low). A new column location can be accessed with each $\overline{CAS}$ cycle (t_{PC}).

Page mode is initiated with a standard read or write operation. Row address is latched by the $\overline{RAS}$ clock transition to active, followed by column address and $\overline{CAS}$ clock active. Performing a $\overline{CAS}$ cycle (t_{PC}) and supplying a column address while $\overline{RAS}$ clock remains active constitutes the first page mode cycle. Subsequent page mode cycles can be performed as long as $\overline{RAS}$ clock is active. The first access (data valid) occurs at the standard rate (t_{RAC}). All of the read operations in page mode following the initial operation are measured at the faster rate (t_{CAC}), provided all other timing minimums are maintained (see Figure 1a). Page mode cycle time determines how fast successive bits are read (see Figure 1b).

NIBBLE MODE

Nibble mode allows serial access to two, three, or four bits of data at a much higher rate than random operations (t_{RAC}). Nibble mode consists of cycling the $\overline{CAS}$ clock while holding the $\overline{RAS}$ clock active, like page mode. Internal row and column address counters increment at each $\overline{CAS}$ cycle, thus no external column addresses are required (unlike page or static column modes). After cycling $\overline{CAS}$ three times in nibble mode, the address sequence repeats and the same four bits are accessed again, in serial order, upon subsequent cycles of $\overline{CAS}$:

00, 01, 10, 11, 00, 01, 10, 11, . . .

Nibble mode operation is initiated with a standard read or write cycle. Row address is latched by $\overline{RAS}$ clock transition to active, followed by column addresses and $\overline{CAS}$ clock. Performing a $\overline{CAS}$ cycle (t_{NC}) while $\overline{RAS}$ clock remains active constitutes the first nibble mode cycle. Subsequent nibble mode cycles can be performed as long as the $\overline{RAS}$ clock is held active. The first access (data out) occurs at the standard rate (t_{RAC}). All of the read operations in nibble mode following the initial operation are measured at the faster rate (t_{NCAC}), provided all other timing minimums are maintained (see Figure 2a). Nibble mode cycle time determines how fast successive bits are read (see Figure 2b).

STATIC COLUMN MODE

This mode is useful in applications that require less noise than page mode. Output buffers are always on when the device is in this mode and $\overline{CS}$ clock is not cycled, resulting in fewer transients and simpler operation. It allows faster access to any of the 1024 column addresses on a given row, typically at half the standard (t_{RAC}) rate for randomly performed operations. Static column consists of changing column addresses while holding the $\overline{RAS}$ and $\overline{CS}$ clocks active. A new column location can be accessed with each static column cycle (t_{SC}).

Static column mode operation is initiated with a standard read or write cycle. Row address is latched by $\overline{RAS}$ clock transition to active, followed by column addresses and $\overline{CS}$ clock. Performing an address cycle (t_{SC}) while $\overline{RAS}$ and $\overline{CS}$ clocks remain active constitutes the first static column cycle. Subsequent static column cycles can be performed as long as the $\overline{RAS}$ and $\overline{CS}$ clocks are held active. The first access (data out) occurs at the standard (t_{RAC}) rate. All of the read operations in static column following the initial operation are measured at the faster rate (t_{AA}), provided all other timing minimums are maintained (see Figure 3a). Static column cycle time determines how fast successive bits are read (see Figure 3b).

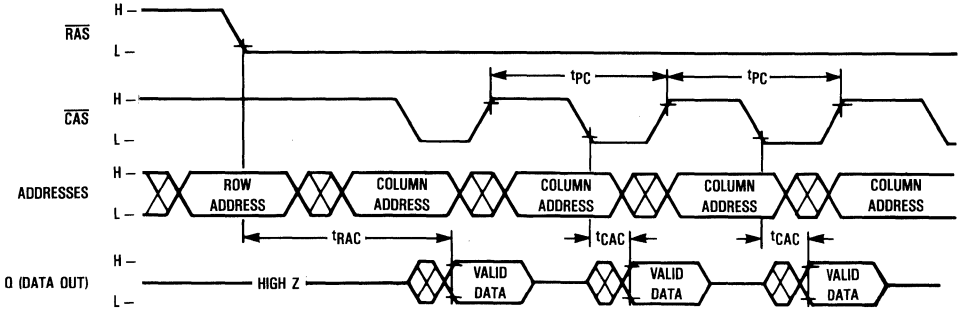

Figure 1a. Page Mode Read Cycle

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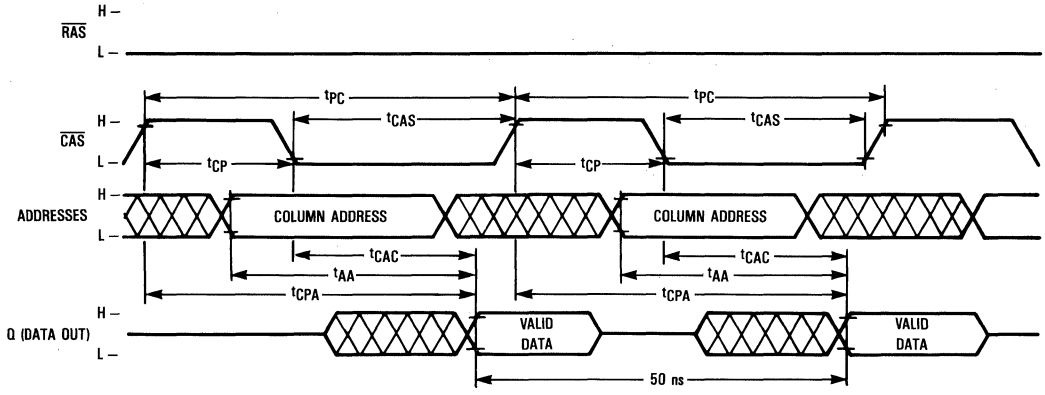

Figure 1b. Page Mode Cycle Minimum Timing

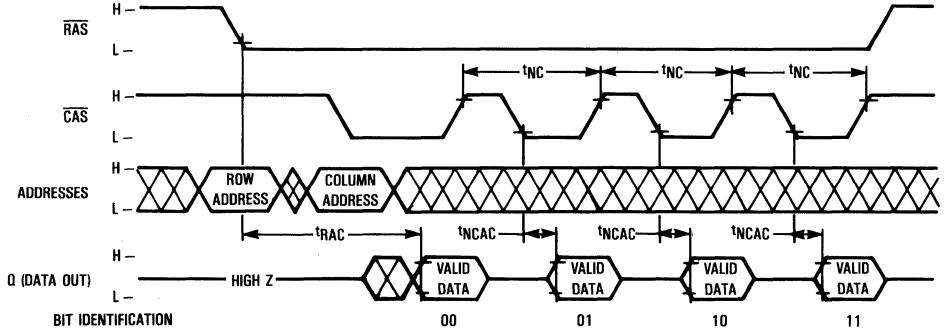

Figure 2a. Nibble Mode Read Cycle

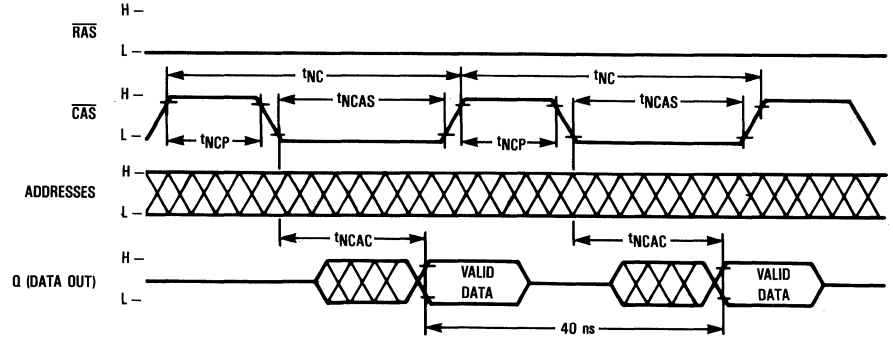

Figure 2b. Nibble Mode Cycle Minimum Timing

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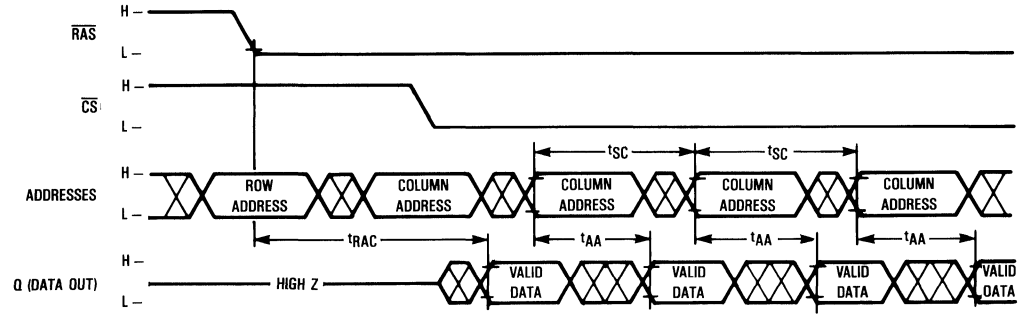

Figure 3a. Static Column Mode Read Cycle

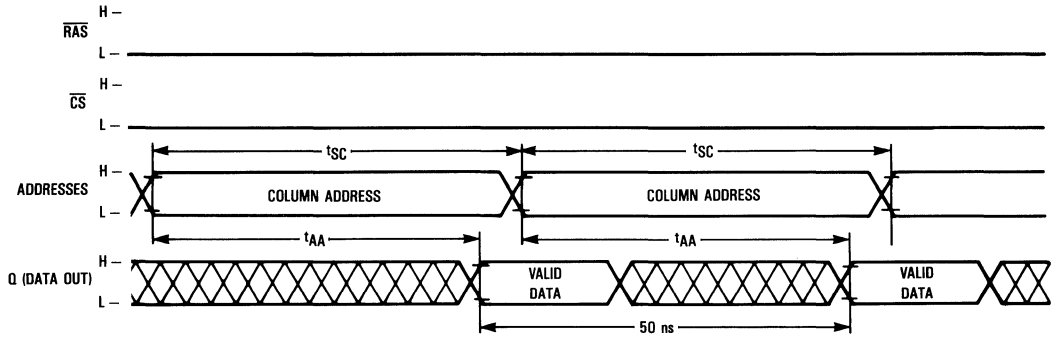

Figure 3b. Static Column Mode Cycle Minimum Timing

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Avoiding Bus Contention in Fast Access RAM Designs

INTRODUCTION

When designing a bus oriented system, the possibility of bus contention must be taken into consideration. Bus contention occurs when two or more devices try to output opposite logic levels on the same common bus line.

This application note points out common causes of bus contention when designing with fast static random access memories and describes ways to eliminate or reduce contention.

WHAT CAUSES BUS CONTENTION?

The most common form of bus contention occurs when one device has not completely turned off (output in a high-impedance state) before another device is turned on (output active). Basically, contention is a timing overlap problem that results in large, transient current spikes. These large current spikes not only generate system noise, but can also affect the long term reliability of the devices on the bus (see Figure 1).

BUS CONTENTION AND FAST STATIC RAMs

Since memory devices are primarily used in bus oriented systems, care must be taken to avoid bus contention in memory designs. Fast static RAMs with common I/O data lines (or any high frequency device with common I/O pins) are the most likely candidates to encounter bus contention. This is due to the tight timing requirements that are needed to achieve high-speed operation. If timing control is not well maintained, bus contention will occur. The most common form of bus contention for memories occurs when switching from a read mode to a write mode or vice versa.

SWITCHING FROM A READ TO WRITE MODE

With $\overline{E}$ low (device selected), on the falling edge of $\overline{W}$ (write asserted) the RAM output driver begins to turn off (high-impedance state). Depending on the input and output logic levels, if sufficient time is not allowed for the output to fully turn off before an input driver turns on, bus contention will occur (see Figure 2a).

Figure 2a shows an example of a RAM trying to drive a bus line low while an input driver is trying to drive the line high. If the situation were reversed (RAM output high and the input driver low), bus contention would still exist.

Of course the obvious way to avoid this type of bus contention is to make sure that the input buffer is not enabled until the write low to output high-impedance (t_{WLQZ}) time is satisfied (see Figure 2b). This specification is usually given on most manufacturers' data sheets.

Another method to eliminate bus contention would be to use $\overline{E}$ to deselect the RAM before asserting $\overline{W}$ (low). This allows the RAM output extra time to go into high-impedance state before the input driver is enabled. $\overline{E}$ and $\overline{W}$ are later asserted low to begin a write cycle (see Figure 2c).

SWITCHING FROM A WRITE TO A READ MODE

With $\overline{E}$ set low (device selected), on the rising edge of $\overline{W}$ (write terminated) the address or data-in changes before the device has had a chance to terminate the write mode. If this should occur, and depending on the input and output logic levels, a bus contention situation could exist (see Figure 3). To avoid address changing type bus contention requires that the address not change till the write recovery specification (t_{WHAX}) is satisfied. To avoid bus contention caused by data changing requires that the data-in remains stable for the duration of the data hold specification (t_{WHDX}). Most of

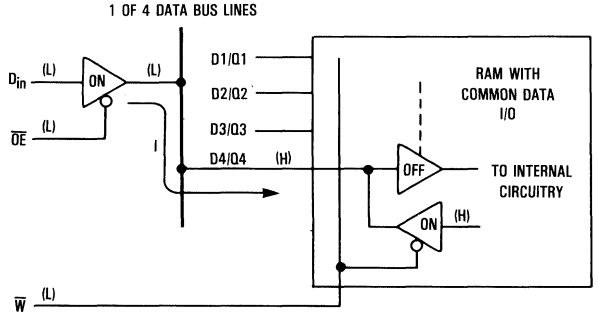

Figure 1. Common I/O Bus Contention

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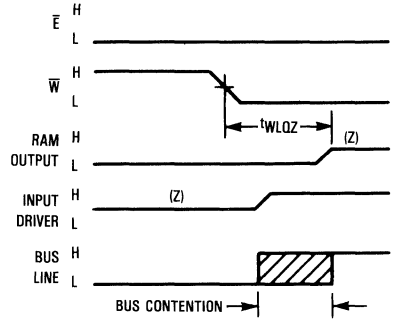

Figure 2a. Input Driver Enabled Prior to Disabling RAM Output

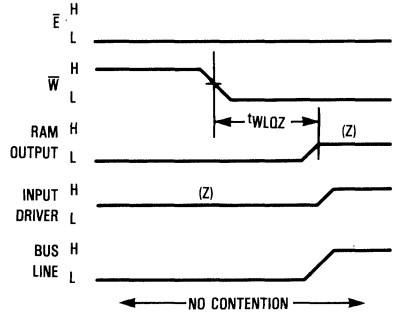

Figure 2b. Input Driver Disabled Prior to Enabling RAM Output

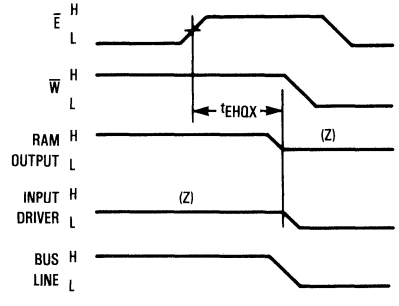

Figure 2c. Using $\overline{E}$ to Avoid Bus Contention

Motorola's fast static RAMs specify write recovery and data hold times of 0 ns. However, it is always a good practice to allow some margin to take care of possible race conditions.

Both of these types of contention could also be avoided by taking $\overline{E}$ high prior to taking $\overline{W}$ high. This will give the RAM output driver time to go to a high-impedance state before $\overline{W}$ goes high. In this case $\overline{E}$ is used to terminate the write cycle instead of $\overline{W}$ (see Figure 3c).

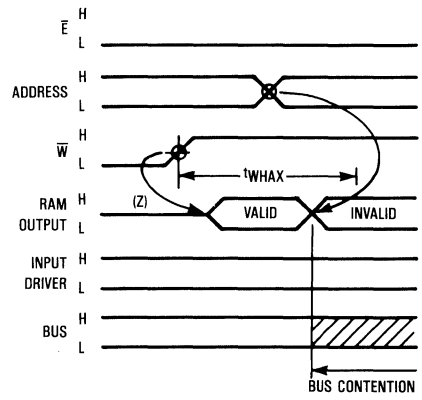

Figure 3a. Data Setup Time Violation

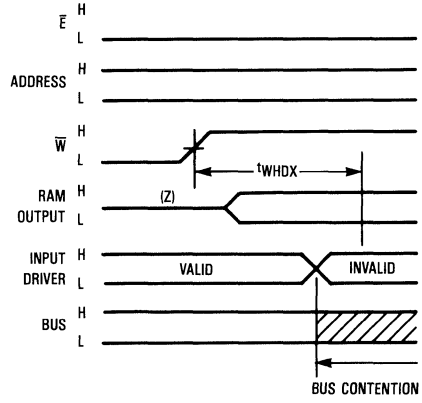

Figure 3b. Data Hold Time Violation

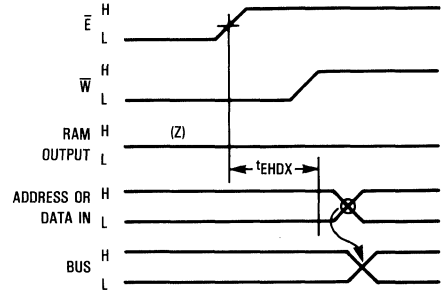

Figure 3c. Using $\overline{E}$ to Avoid Bus Contention

OTHER WAYS TO ELIMINATE BUS CONTENTION

If the RAM has an output enable pin ($\overline{G}$), synchronizing schemes can be incorporated to help eliminate bus contention. Taking $\overline{G}$ high will ensure that even when the RAM is in a read mode the output will be in a high-impedance state. This will allow the input driver to be enabled longer.

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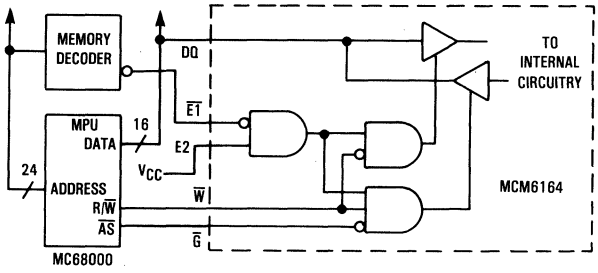

Figure 4a. Using $\overline{G}$ to Avoid Bus Contention

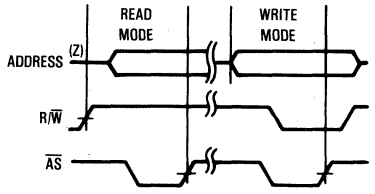

Figure 4b. Timing Diagram of the MC68000

Most advanced microprocessors, such as the MC68000 and MC68020, have asynchronous bus control signals that take advantage of fast memory devices with output enable pins. Figure 4 shows one way to avoid bus contention using a Motorola MC68000 interfaced to a Motorola 45-ns MCM6164.

A more obvious way to eliminate bus contention is to use slow memory devices. Slow memories have loose timing requirements that allow devices to fully turn off before another device turns on. Of course this defeats the whole purpose of fast static memory devices.

Another obvious way to eliminate bus contention is to use memory devices that have separate data I/O pins. In this way the R/$\overline{W}$ signal from the microprocessor can control a buffer device to eliminate bus contention (see Figure 5). However, the industry is demanding RAM with common I/O because these devices cost less and save system real estate.

Common I/O devices reduce package size since fewer pins are needed. Smaller packages result in less PCB space requirement. Common I/O devices also eliminate the need for an extra buffer with its associated expense and space requirement. In general fast static RAMs configured greater than a X1 will have common data I/O pins.

Another popular way to reduce bus contention is to put a current limiting series resistor on each bus line (see Figure 6). The series resistor does not eliminate bus contention, but it helps reduce the large transient currents associated with bus contention. However, series resistors increase access time as well as increasing component count. The added access time depends on the total bus capacitance (including the capacitance of the devices on the bus) and the total bus resistance. The added delay should be added on to the point at which bus contention ceases. The following formulas can be used to determine the added access delay.

$$t_{HL} = R_L \cdot C_L \cdot \ln \frac{V_{in}(\text{initial}) - V_{in}(\text{final})}{V_{IL}(\text{max}) - V_{in}(\text{final})}$$

$$t_{LH} = R_L \cdot C_L \cdot \ln \frac{V_{in}(\text{final}) - V_{in}(\text{initial})}{V_{in}(\text{final}) - V_{IH}(\text{min})}$$

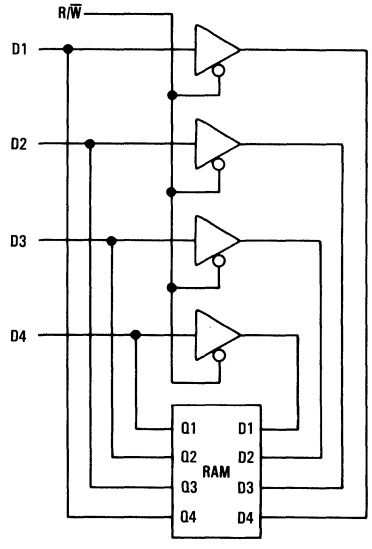

Figure 5. Separate I/O Buffer

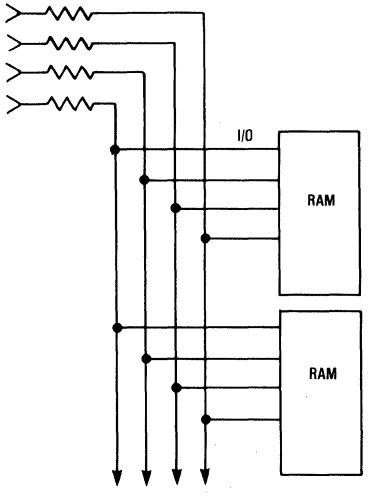

Figure 6. Using Series Terminating Resistors

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Generally the value of the resistor should be around 100 ohms. The larger the resistor the less the transient current generated, but the greater the delay. Using a 150-ohm resistor will limit the current flow to less than 20 milliamperes while adding approximately 3 nanoseconds extra access time. However, note that even with series resistors bus contention duty cycle must be minimized to reduce EMI and bus ringing.

Although it is very important to reduce bus contention, CMOS memories can tolerate more bus noise generated by bus contention than can bipolar memories, due to the excellent noise immunity advantage of CMOS over bipolar technology. However, even when using CMOS memories, large destructive transient currents generated by bus contention can still occur.

CONCLUSION

Bus contention must be taken into consideration in most bus-oriented system design. The occurrence of bus contention generates large transient currents that produce system noise and could also affect the system's long term reliability.

Fast random access memories with common data I/O pins are very susceptible to bus contention due to tight timing requirements. Although it is almost impossible to totally eliminate bus contention, it must be the goal of the system designer to minimize bus contention.

AN973

Avoiding Data Errors with Fast Static RAMs

Microprocessors are now capable of 20-25 MHz. This places a great demand on SRAMs to supply super-fast access times. Today's sub-100-nanosecond SRAMs in production are rapidly moving to sub-50 nanoseconds as yesterday's prototypes ramp into production, and sub-25 nanoseconds is just on the horizon. This need for high-speed SRAMs is amplified by the fact that setup, hold times, and cycle edge accuracies do not usually improve at the same rate as the clock frequency. There is help on the way in terms of application specific SRAMs that put on chip some of the "glue" features that eliminate gate delays caused by decoders, drivers, or clock signals; but for now, the main burden will fall upon SRAM designers to make up for the "lost time" in the shorter cycles. Some of the tools of the SRAM designer are improved processes, tighter design rules, and improved circuit techniques such as address transition detection. When you combine all of these features into a high performance SRAM, you no longer have the bistable flip-flop of yesterday but a highly tuned circuit that is more closely related to a DRAM. This is where the system designer can help. Although SRAM designers are doing everything possible to make the devices stable and noise immune, there is no substitute for a good solid system layout and design. The following discussion gives system designers some insight into potential trouble areas from a component engineering viewpoint.

CHARACTERISTICS OF HIGH-SPEED BUSES

When data is transmitted over long distances, the line on which the data travels has to be considered a transmission line. A long distance is relative to the rate at which data is being toggled. Address and data buses associated with high-throughput microprocessors (e.g., M68000 family) must also be thought of as transmission lines, since it is not uncommon for these processors to run bus cycles of 40-nanosecond periods or less.

Other features of high-end microprocessor buses are that they tend to operate in harsh, noisy-type environments, and most of these buses are unterminated. A high-impedance, unterminated bus line acts just like an antenna. It not only radiates EMI, it can also receive EMI. This can result in bus ringing, crosstalk, and various other noise associated problems. The more transmission lines a bus has, the more antennas to pick up and radiate noise. Of course, the best way to reduce this EMI is to ensure that the bus is properly terminated into a low-impedance load. This low-impedance load could be in the form of a pull-up or pull-down resistor tied to each bus line. Ideally, the termination resistor should be equal to the characteristic impedance of the bus line. A transmission line terminated into its own characteristic impedance has the best incident wave switching as well as the least amount of reflection.

Since an unterminated bus looks almost entirely like a capacitive load, the larger the resistor value the slower the rate at which data can be presented to the receiving device. This is due to the time it takes to charge and discharge this capacitive line through the termination resistor. If a small value resistor is used, the charging/discharging time delay can be minimized (t=RC). However, the smaller the resistor the greater the power consumption through the resistor. Also, if the resistor value is too small, its value will approach that of the source resistance of the transmitting device, which could lead to a degradation of noise margin to the receiving devices. A resistor value between 1 kilohm and 10 kilohms is usually adequate. The actual value should be optimized through experimentation (see Figure 1).

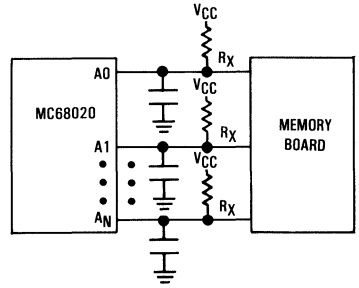

Figure 1. Microprocessor Address Bus with Pull-Up Resistors

HIGH SPEED SRAM DESIGN TECHNIQUES

In order to speed up access times of high-speed RAMs, many new design techniques have surfaced. One of the most innovative techniques to emerge is known as address transition detection (ATD) circuitry. Since row address access times are typically slower than column address access times, this circuitry originally used the row addresses to trigger a clocking sequence that restored bit lines, shorted data lines, equalized sense amplifiers, and threestated the output as the output buffers were equalized. This meant that many of the internal transistions could be completed by the time that the signals were decoded and propagated through the device seeking the proper cell and outputting data. This then made row and column access times much more equal and eliminated one of the speed bottlenecks. This scheme also has the added advantage of reducing power consumption because the static bit line loads can be reduced in size by utilizing a parallel equalization that is also generated at the ATD initiation and used to pull up the bit line 0 before selection of the new word line. Since

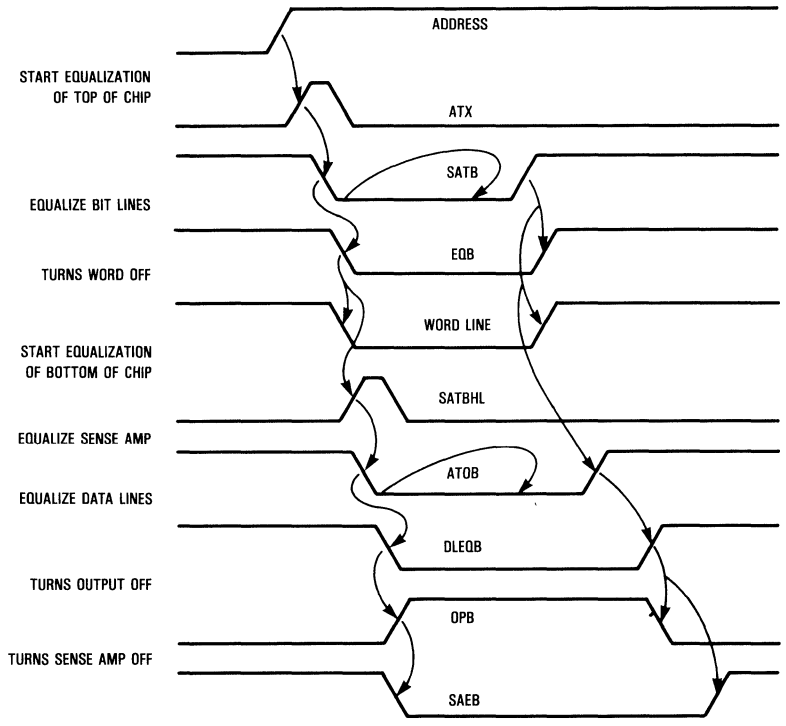

Figure 2. Address Transition Detection Timing Chain

its inception, ATD has been expanded and is now activated by all addresses and chip select pins instead of just row addresses. A typical timing chain, as shown in Figure 2, applies to Motorola's MCM6164 8K×8 SRAM and exemplifies the clock sequence dependency.

ATD has been shown to be very effective as a performance enhancer and will remain a valuable tool for designers, but it can be seen that we now essentially have a clock-activated part. What happens if addresses are floated or oscillate at a frequency greater than the ATD response? What happens if addresses are skewed, thereby getting successive ATD initiations? There is also the case of signals being gated from numerous sources, in which the address may start in one direction and then reverse several times before it finally seeks a valid high or low level. Circuit designers believe that these potential problems have been resolved over the last few years as testing techniques and circuit simulations have wrung out the infinite number of application variations. However, there is a simple, foolproof way that system designers can eliminate any potential for this type of a problem. Deselect the device during address transitions (see Figure 3).

Since new design techniques have made chip select access times equal to address access times, system designers can take advantage of this and improve reliabilty of their system by increasing overall immunity to a noisy environment. This can cover a host of potential board-induced problems from oscillating multiplexer or driver units, to spurious address glitches put out by MPUs.

Another design improvement is related to rise and fall times on the output levels, known by circuit designers as di/dt. This is the inductance associated with the changing current as loads are charging and discharging. This inductance is coupled back to the device, and through connections and bus resistance can cause the power supply or ground to change drastically. This is pushed to the limits as output drivers become more powerful, and is especially aggravated by multiple I/O devices like byte-wide SRAMs which may have all eight data lines switch from all 0s to all 1s or vice versa. These spurious noise spikes on the power lines can affect the data contents of the device, as well as any other device sharing the same power and ground buses (see Figure 4). Circuit designers have developed circuitry that has a feedback loop that controls the rise and fall time just enough to minimize overshoot, undershoot, and ringing. This di/dt is the inherent reason why byte-wide SRAMs are typically 4-5 nanoseconds slower than single output devices.

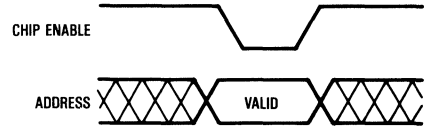

Figure 3. Deselection of Device During Address Transition

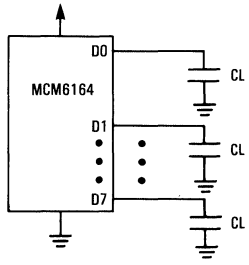

Figure 4a. MCM6164C Data Bus

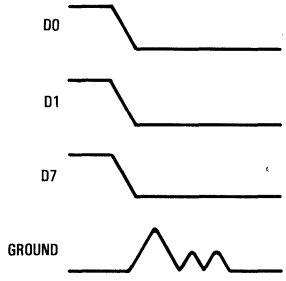

Figure 4b. Ground Bounce When Data Switches from All 1s to All 0s

PCB POWER FEED CONSIDERATIONS

Another source of noise can be inadequate power feeds and power supply decouplng. Large ground planes should be used to reduce both inductances and resistances. The resistances of the power supply lines should be less than 0.1 ohm. If the inductances or resistances of the power supply lines become significant, V_{CC} or ground bounce can occur. Since all inputs are referenced to ground, gate input thresholds could be exceeded, causing data errors to be generated. An excellent PCB design is one that incorporates a multilayer board. One layer should be entirely devoted to a ground plane.

The use of good-quality decoupling capacitors can help to keep noise off the power lines. A value between 0.01 microfarad and 0.1 microfarad (use 0.1 microfarad for $\times 8$ organizations) should be used for each RAM. This capacitor should be located as close to the RAM power pins as possible. When using IC sockets, it is recommended that sockets with gold-plated copper contacts and built-in decouplng capacitors be used.

A large value capacitor (≥ 1 microfarad) should be used on each V_{CC} line. The purpose of this capacitor is to provide for sudden current demand (current surges) from the power supply.

Figure 5 illustrates a typical memory board design.

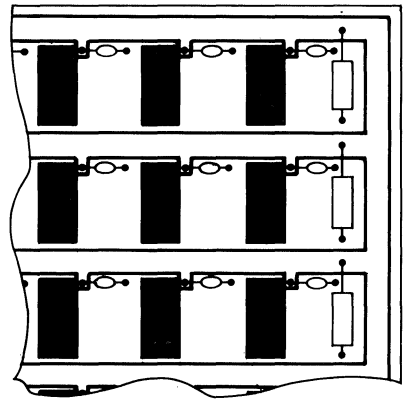

Figure 5. Typical Memory Board

SUMMARY

Digital transmission line theory must be taken into account when designing high-frequency buses. A high-impedance, unterminated bus behaves much like an antenna, receiving as well as transmitting EMI. The use of termination resistors on these buses can reduce EMI. Many innovative designs have evolved to speed up access times of fast static RAMs. One of the more innovative designs is that of address transition detection circuitry. Most high-speed RAMs today use this technique to decrease access time. Good PCB power feed design, as well as the judicious use of decoupling capacitors, is essential for optimum performance from fast static RAMs.

Much of the time, the problems caused by a marginal device, system layout, or pushing for the last nanosecond is an intermittent random type of problem that could result in either destroyed data or access time push-out. If you are having a problem, call Motorola MOS Memories in Austin, Texas, (512) 928-SRAM (928-7726). We are on your design team!

AN984

25 MHz Logical Cache for an MC68020

Prepared by:
Motorola — East Kilbride, Scotland

INTRODUCTION

As the speed of the MC68020 processor increases it becomes more difficult and more expensive to provide large amounts of no-wait states memory. The addition of a logical cache in a memory management based system then becomes a more viable alternative to the problem. For a typical 25 MHz MC68020 system the incorporation of a no-wait states cache is one of the most economical ways in which the true performance attainable from this particular processor can be achieved.

CACHE DESCRIPTION

The cache described in this application note is a 32K byte (8K long words) direct mapped logical cache. The cache is organized such that both supervisor and user, program and data accesses are stored. The entries are tagged appropriately with the function code lines. To avoid any stale data problems that may occur with the data the cache update logic includes a 'write through' mechanism that forces any data writes to update both the memory and the cache. The cache operates with no wait states with a 25 MHz MC68020.

BLOCK DIAGRAM DESCRIPTION

The cache can be broken down into several functional parts as follows:

- tag RAMs
- data RAMs
- control logic
- entry update mechanism

The cache is organized as 8K long word entries (see Figure 1) which are referenced by a 22 bit TAG field. This TAG is made up of the upper address lines (TA15–TA31), the function codes (TFC0-2) and the size pins (TSIZE0-1). By incorporating the size pins into the TAG field means that the data entry can be validated even if it were referenced as a misaligned data transfer. The function codes allow the entries to be referenced separately with respect to user/supervisor and program and data entries.

The cache mechanism will begin operation as soon as an address becomes valid on the logical address bus. This address accesses the TAG RAM within the cache and the corresponding entry is compared with the relevant section of the logical address bus (LA15-LA31) and the control bus (FC0-2, SIZE0-1).

If this comparison is valid then this gives an indication to the comparator logic that a valid entry may be present within the cache data RAMs.

To determine whether this data entry is indeed valid a simultaneous access is made to the VALID bit RAM with the lower section of the logical address bus (LA2-LA14). If the entry in this VALID RAM is a logic 0 then this indicates that the corresponding data entry at that cache address (LA2-LA14) is a valid entry.

Access to that data item can then be made on the condition of several control signals (e.g. R/W*, CACHE-E*, etc.) and the data buffers to the system data bus will be enabled. This is termed as a CACHE HIT.

Conversely, if the entry in the VALID bit RAM was a logic 1 then this would indicate that the corresponding data item was not a valid cache entry and so the isolation data buffers would not be enabled to the system bus. This is termed as a CACHE MISS.

When the cache detects a HIT then the bus cycle is completed from the data RAMs and the system operates with no wait states.

If on the other hand the cache detects a MISS then the processor has to fetch its data from external memory which by its nature will be slower and will incur wait states.

To facilitate the data fetch from external memory the cache mechanism forces the processor to do a RETRY of the MISSed bus cycle. This retried bus cycle will then go out to external memory and fetches the relevant data item which will be latched by the processor and also used to update the cache. Subsequent accesses to this address will then find the data resident in the cache.

To preserve data integrity a CACHE MISS is also generated by a data write cycle. On writing to an address the cache forces a MISS such that the data item will be written to the cache in addition to the external memory. Subsequent data reads at this location will find that the data item is resident and is the most recent version.

Forced CACHE MISSes are also generated when the logical

address is detected as being a peripheral access (e.g. serial I/O device) or when the processor is executing a CPU space cycle (e.g. interrupt acknowledge).

CACHE CONTROL MECHANISM

The cache hit signal (CHIT*) is generated as a result of the comparison of the TAG data, the VALID bit and various control signals. When the logical address from the processor becomes valid the cache TAG RAMs are enabled and the TAG data is produced for comparison.

These TAG RAMs are addressed as an 8K long word bank and so logical address lines LA2 to LA14 are used.

The TAG RAM itself contains information relating to the bus status of the cached item. This bus status consists of a section of the logical address bus (LA15-LA31) and some control signals (FC0-2, SIZE0-1). When these TAG RAMs are accessed this previous bus status is compared with the existing bus to detect if there is a match.

Comparators U215, U216 and U217 (see Figure 4) are used to compare this information and if there is a match the outputs Oa=b (pin 19) will be asserted.

The assertion of these three comparator outputs is then conditioned by various other factors to determine whether a cache hit signal should be generated.

While the TAG RAMs are being accessed by logical address lines LA2-LA14 a VALID bit RAM is also accessed. The information contained in this VALID bit determines whether or not the cache data is valid. When the cache is enabled all the entries in the VALID RAM are set to logic 1 to indicate that there are no valid entries in the cache.

Subsequent memory accesses then cause a cache miss which results in a cache entry being made. When this cache entry is made the status of the bus (LA15-31, FC0-2, SIZE0-1) is saved in the TAG RAM at the location pointed to by the cache index (LA2-14). The information on the data bus is then saved in the data RAMs at address with cache index LA2-14 and the corresponding VALID bit entry is also set (i.e. the cache entry is marked as being valid).

Subsequent accesses to that address will then cause the TAG address comparators to assert their outputs and the VALID bit to be set. The assertion of the cache hit signal (CHIT*) is then dependent upon the status of several other control signals such as cache enable (CACHE-E*), CPU space and peripheral access (IOEN*). Accesses to CPU space are not cached because of the problems that might arise when servicing interrupts or accessing coprocessors. In addition access to peripheral devices (indicated by the signal IOEN*) are not cached because of the read write nature of some peripheral device registers.

When these signals are taken into account the resultant assertion of the cache hit signal (CHIT*) will then cause the processor to complete the bus cycle with no wait states.

Control of the cache is facilitated by three hardware primitives: Cache Enable, Cache Disable and Cache Clear. These primitives are initiated by accessing a specific address within CPU space which is not used for any other CPU space functions.

On requesting a cache enable function the mechanism causes the VALID bit RAM to be set to logic 1's, indicating no valid cache entries, and then assert the CACHE-E* signal to the rest of the system.

The cache disable function simply negates this CACHE-E* signal.

The cache clear function is included to allow the support of multi-tasking software. On initiation of the cache clear function all entries in the VALID bit RAM are cleared so emptying the cache. This is useful where the software has to perform a context switch.

CACHE CONTROL LOGIC

The Cache control logic allows the software programmer to enable the cache, disable the cache and to clear the cache contents. Accesses to the control logic can only be done under CPU space. This prevents accidentally writing to the control logic during normal operation (the SFC and DFC registers are programmed for CPU space with the MOVEC instruction, and the MOVES is used in writing to the control logic). Hence only the supervisor mode of operation can control the cache.

The address lines LA24-LA26 are used to decode the cache control functions, these being inputs fed to an 74LS138 U241 (see Figure 3). In addition to these addresses in CPU space, the programmer should also select an area of memory that will not cause contention with the normal MC68020 CPU functions.

An example decode could be $1070000 ($ is used to represent a hexadecimal number) for clear cache, $2070000 for disable cache and $4070000 for enable cache.

Cache Enable

The cache is enabled by accessing to a CPU address similar to the one given above, the data being irrelevant. On enabling the cache all entries are made invalid. This ensures that no stale data problems are created from accesses when the cache was previously enabled.

The output from U118D (see Figure 3) is used to enable a sequencer consisting of three 4-bit binary counters: U246, U247 and U248. These counters are used to increment the address bus to set the valid bits to all 1's (entry is invalid). The addresses are presented to the valid RAM U259 via the latches U249 and U250, the outputs from these being enabled at the same time as a write to enable the cache. Also during this sequence the logical address bus to this RAM is tri-stated from the RAM's address bus by U243 and U244.

Under normal operation the latches U243 and U244 are enabled and U249, U250 are disabled allowing the valid RAM to be addressed from the logical address bus. The 12-bit sequence clears 4 K entries in the cache (each entry is a long word).

The sequence is repeated twice to clear the whole 8 K entry cache. The two D-type flip flops U251B and U251A are used to write first to the upper 4 K then the lower 4 K entries.

At the end of the cache clear sequence the cache is enabled via the S-R flip flop U257D and U118C. The CACHE.E* is then used in the comparator logic to indicate that the cache is enabled. In addition the DSACK0* and DSACK1* is returned to the MC68020.

As far as the processor is concerned the cache clear mechanism can be thought of as a long instruction. The valid

RAM latches data with respect to the sequencer clock (40 MHz for 25 ns SRAM's) and a logic 1 is latched on each falling edge of this clock.

A logic 1 is written into the valid RAM when: the sequencer is enabled; it is the falling edge of the 40 MHz clock and the WRITEN* signal from the entry update mechanism is high (U258C, U263A and U219D). This logic is also used to write a logic 0 into the valid RAM during normal operation.

To prevent external bus contention when the cache is being written to, a signal ADDBUFDIS* is generated which can be used to disable external address buffers. The CMISS signal should be used to disable the external address buffers during a cache hit.

Cache Clear

The cache clear mechanism is used to allow the operating system to perform a context switch. A cache clear command will produce the same output as the enable cache command.

Using the 40 MHz clock gives a context switch time of approximately 0.025 x 1024 x 8 = 205 us. If this is unacceptable the mechanism can be speeded up by using several valid bit RAMs of lower density in parallel, or using a RAM with a clear feature.

Cache Disable

This command produces an input into U240B to set the S-R flip flop to cache disable (CACHE.E* set to a logic 1). The reset signal is also fed into U240B to ensure that the cache is always disabled at reset.

ENTRY UPDATE MECHANISM

This section of logic (see Figure 2) is used to control the cache mechanism for updating entries in the cache. In addition, the logic will produce control signals used to latch data into the Tag and Data RAMs and control the isolation data buffers for the cache (U236 - U239 in Figure 5).

The mechanism used to update the entries in the cache is only enabled on a read cycle (R/W* signal into U261D) and when the cache is enabled (CACHE.E* signal into U261C).

The control logic is required to perform three distinct operations:

- On a write cycle the WRITEN* signal should be asserted to latch data into the RAMs to perform a write through operation. When the address is next accessed it will reside in the cache.
- On a read cycle that does not generate a cache hit, the logic needs to initiate a retry operation to enable the cache to latch the data which is being read by the MC68020.
- Thirdly, on a read cycle, which causes a cache hit, the bus cycle needs to be terminated to allow zero wait state operation at 25 MHz from the cache.

Write Cycles

Assuming the cache is enabled then on a write cycle the output from U240D produces logic 0 (the output from U261C will be logic 0). This output produces a signal INHIBIT* which prevents the cache returning DSACK0*, DSACK1*, HALT* and BERR* (U256A, B, C, D), used for read cycles (see Figure 2).

A signal FORCEW* is also generated via U258B and U219C to control the output enable of the cache isolation buffers to allow data to be routed to the cache data RAMs (see Figure 5).

The WRITEN* signal is finally generated from U258A to produce the W* enable for the TAG and DATA RAMs. WRITEN* is also used to enable the buffers: U212 - U214, to route the current logical address, function codes and size lines into the TAG RAMs (see Figure 4).

Two banks of RAMs are used to obtain an 8 K entry long word cache; the lower bank of RAMs are enabled with LA14* from U255C and the upper bank is enabled by LA14. This is needed to allow 25 MHz operation (25 ns SRAM - MCM6268-25 -are used as shown in Figure 4).

On the assertion of DSACK0*, DSACK1* from the external physical memory the two D-type flip-flops U235A and U253B (see Figure 2) are used to negate the WRITEN* just after the falling edge of the processor clock S4 (just after the MC68020 latches data). On the negation of WRITEN*, tag data is written into the tag field.

The information on the data bus is latched into the cache data RAM and the tag buffers and data isolation buffers isolate the cache from the system busses. This section together with the whole entry update mechanism must operate logically very quickly hence FAST logic is used throughout.

Read Cycle with a Cache Miss

Timing diagram 1 shows the cache sequence when a cache miss occurs. From this diagram it can be seen that the addresses on the address bus do not become stable until 5 ns into S1 worst case. At this point it will take 25 ns to obtain information from the TAG data RAMs (the RAMs are permanently enabled).

In addition to this there is a delay through two levels of comparator (U215 - U218). This gives an absolute maximum propagation delay time of 46 ns after the address bus is stable before a valid CHIT* signal is generated. With the above conditions a valid cache hit signal (CHIT*) should be asserted in the middle of S3 for a TAG match. The entry update mechanism uses this information to determine if there is going to be a cache miss or a cache hit.

In the case of a cache miss the following sequence of events are executed: DSACK0* and DSACK1* are asserted by the assertion of the MC68020 AS* (U255B) by U256A and U256B as shown in Figure 2. The INHIBIT is set to a logic 1 by U261C, U261D and U262A. U252A is then used to bring U252B out of RESET on the falling edge of S2. This D-type is then used to sample the CHIT* signal in the middle of S3. In the case of a cache miss the D input will still remain high, forcing the cache miss signal CMISS to go high. This is used to enable external data buffers for the MC68020. This causes the BERR* and HALT* signal to be asserted simultaneously to request a retry cycle (via U261B, U256C and U256D). This takes advantage of the MC68020's ability to recognize a late retry if spec 27A is satisfied. (Note that

68020 inserts an additional 3 clock cycles after S5 of this cycle).

On the termination of this bus cycle all signals are negated as shown in the timing diagram, with the exception of the INHIBIT. This is because on the rising edge of LAS* the output from Q* of U269A is fed back to the input to produce a low INHIBIT signal for the following retry cycle This low INHIBIT signal prevents the DSACK0*, DSACK1*, BERR* and HALT* lines from being asserted by the cache during the retry cycle.

Timing diagram 2 shows the retry cycle. The length of this cycle is determined by the actual physical device being read so it is shown as an unknown number of wait states. The same cycle is repeated as above, however, during this cycle INHIBIT has been asserted causing FORCEW* (force a write to the RAMs) and WRITEN* to be asserted. This has the effect of updating the cache on the read cycle by forcing the cache to latch the addresses, function code and size signals to the TAG RAM and the DATA bus contents into the data RAMs.

The buffers U236 - U239 are enabled by (CHIT*) ANDed with (FORCEW*) and the direction is controlled by CHIT*. In this case CHIT* is a logic 1 causing data to be written into the RAMs. The buffers U212 - U214 are enabled by the WRITEN* signal.

On return of the DSACK0*, DSACK1* from the physical system, the WRITEN* signal is negated (via U257A, U255C, U253A, U253B, U219B and U258A) to latch data into the RAMs just after the falling edge of S4.

In addition to this all the signals are negated at the end of the cycle and the INHIBIT signal returns to a logic 1 level on the negation of LAS* (U262A and U240D).

Read Cycle with a Cache Hit

When a read cycle occurs at an address which has a corresponding input in the cache, a cache hit will occur. This cycle is similar to the one above except the CHIT* signal from the comparators U215 - U218 is asserted by the middle of S3, setting CMISS inactive (output from Q of U252B is set to a logic low) and forcing the external data buffers to be disabled preventing data bus contention. The BERR* and HALT* are also prevented from being asserted by U261B so no late retry cycle is signalled to the MC68020.

Finally, the cache data RAM isolation buffers U236 - U239 are enabled and the direction is selected to be output from the RAMs to the data bus. As there is no bus activity which stops the recognition of DSACK0* and DSACK1*, this read cycle by the MC68020 from the cache is performed in zero wait states at 25 MHz.

At the end of the cycle all the signals are negated for the next bus cycle.

CONCLUSION

The design of a 25 MHz logical data cache to interface between the processor and an MMU involves the use of very fast logic and static RAMs for zero wait state operation. The RAM access speed required in this application is 25 nS to allow no wait states operation.

The control logic has been designed discretely with FAST Schottky TTL since the use of PLAs would have a serious effect on gate propagation delay times.

The MC68020 supports a late retry cycle recognition and this is used in the design to take corrective action in the case of a cache miss.

As greater performance is required from the MC68020 the move towards high frequency zero-wait state operation becomes a more important requirement. If an MMU is placed between the processor and memory this will have an effect on zero-wait operation at the higher frequencies.

If the logical data cache can be made large enough, so that a high hit rate can be achieved, then slower physical memory could be tolerated in the system.

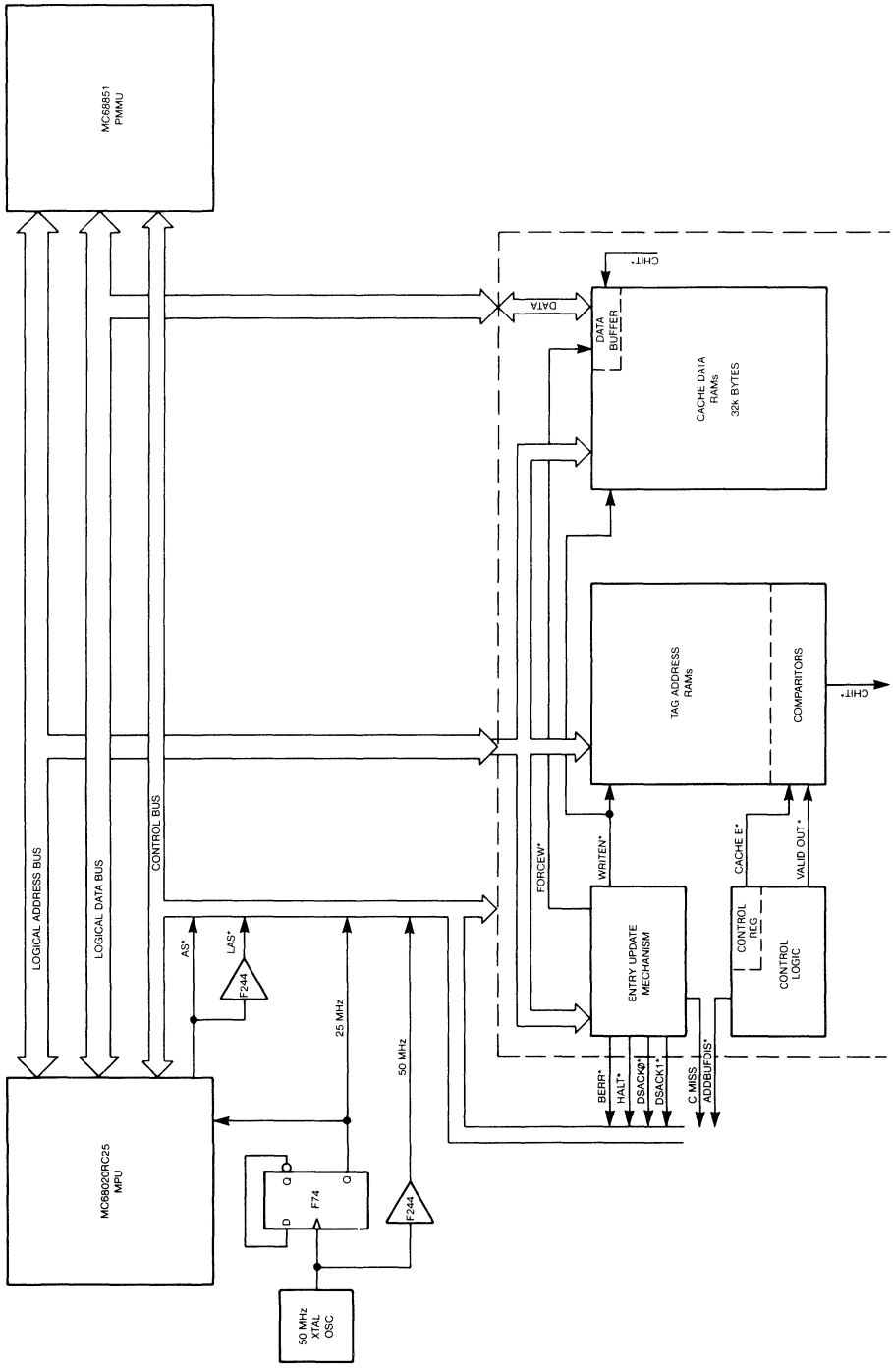

Figure 1: Block Diagram

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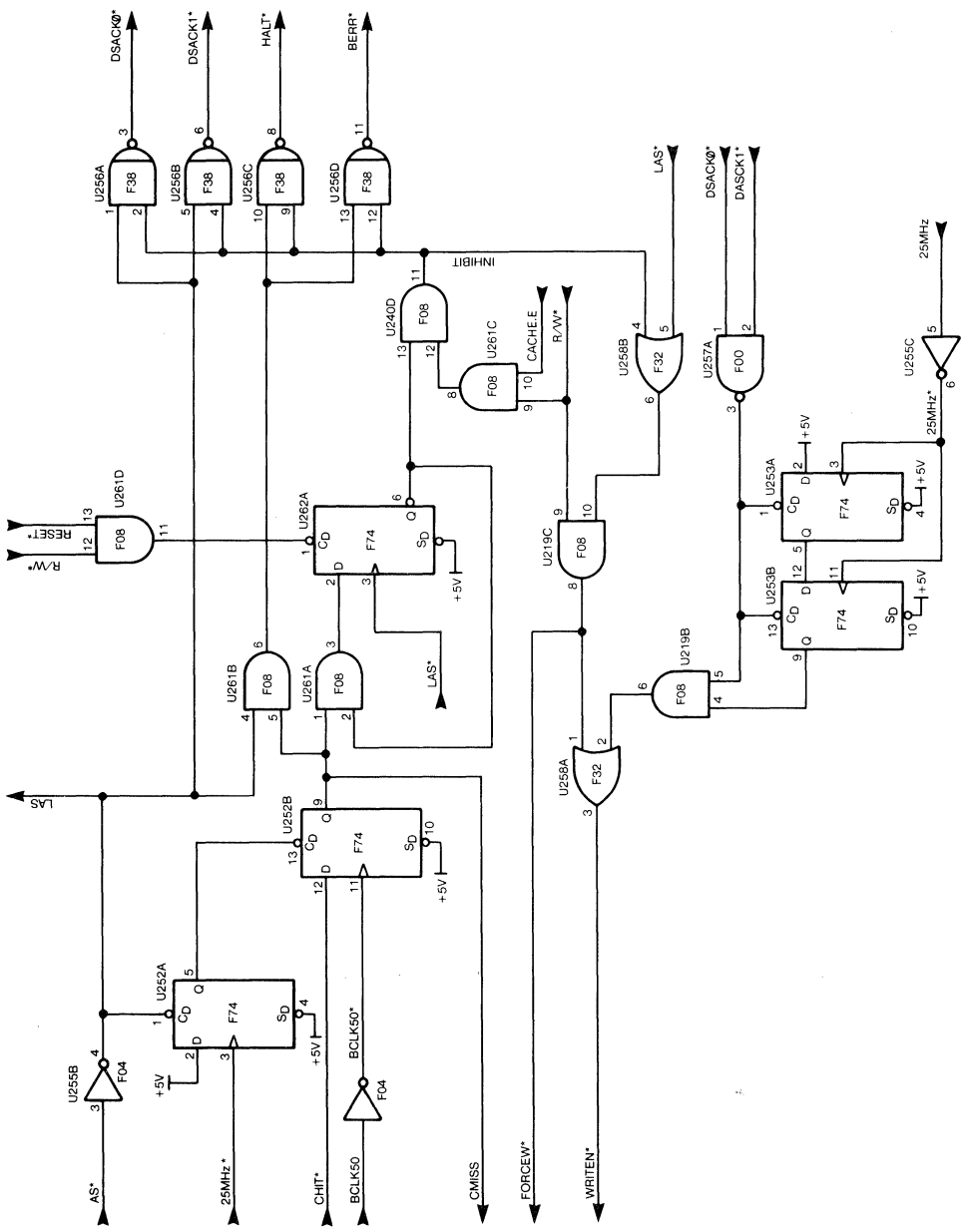

Figure 2: Entry Update Mechanism

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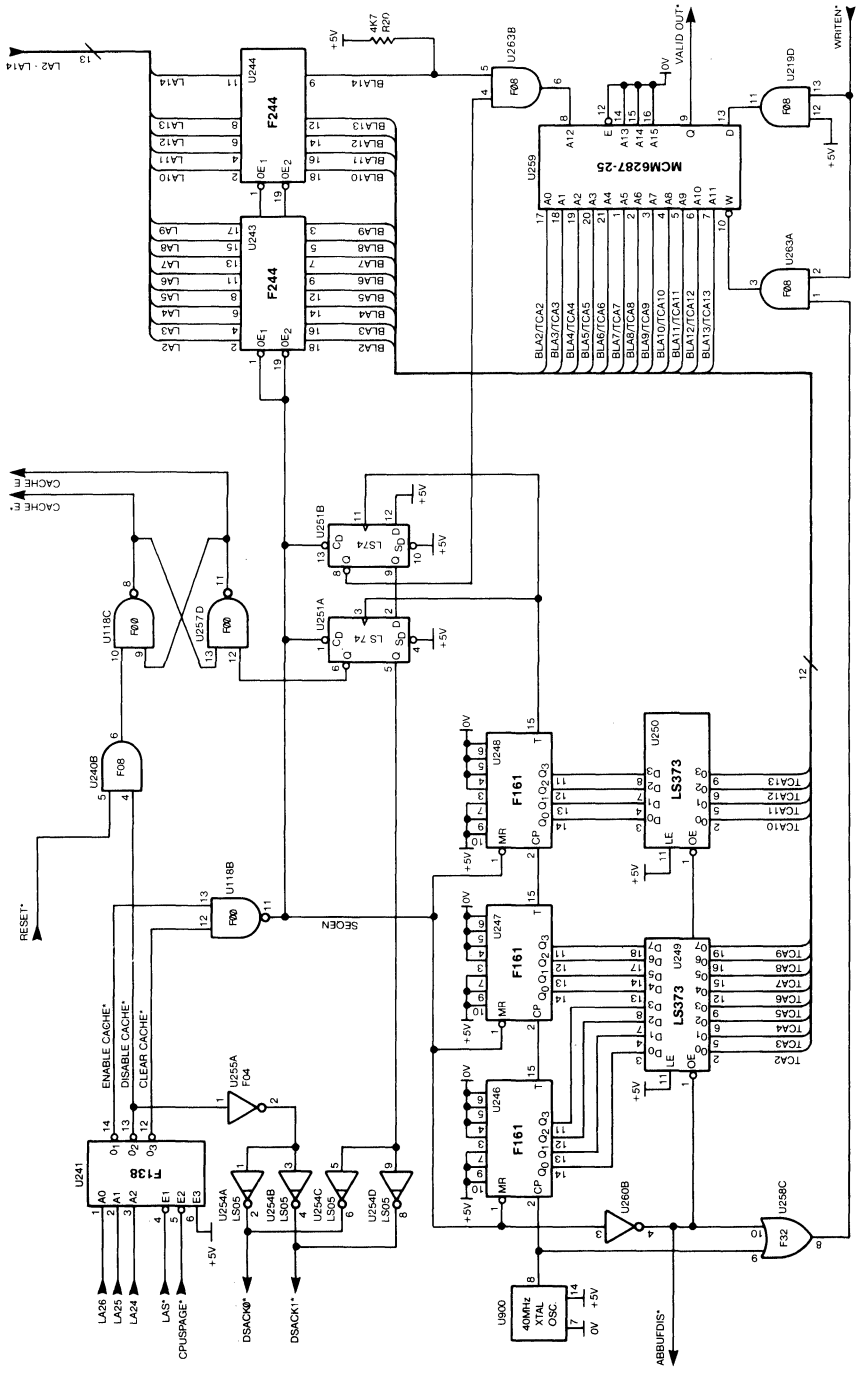

Figure 3: Control Logic

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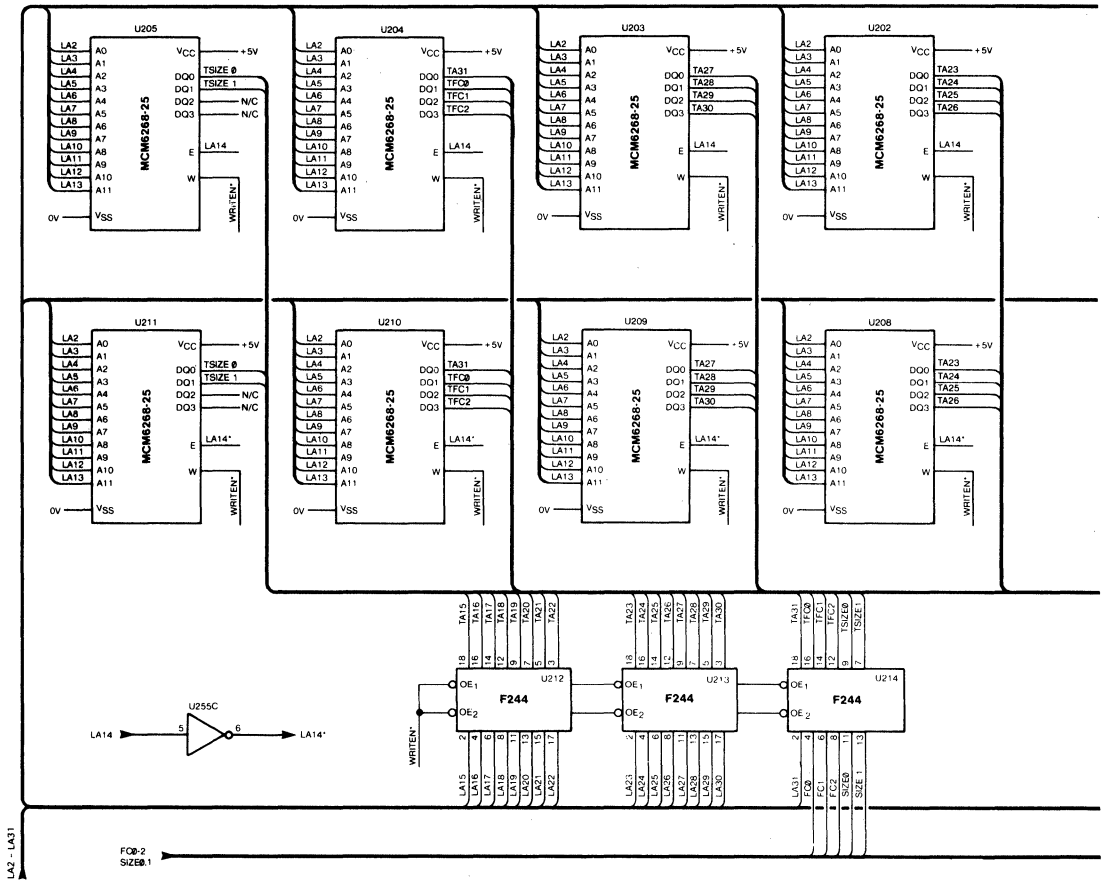
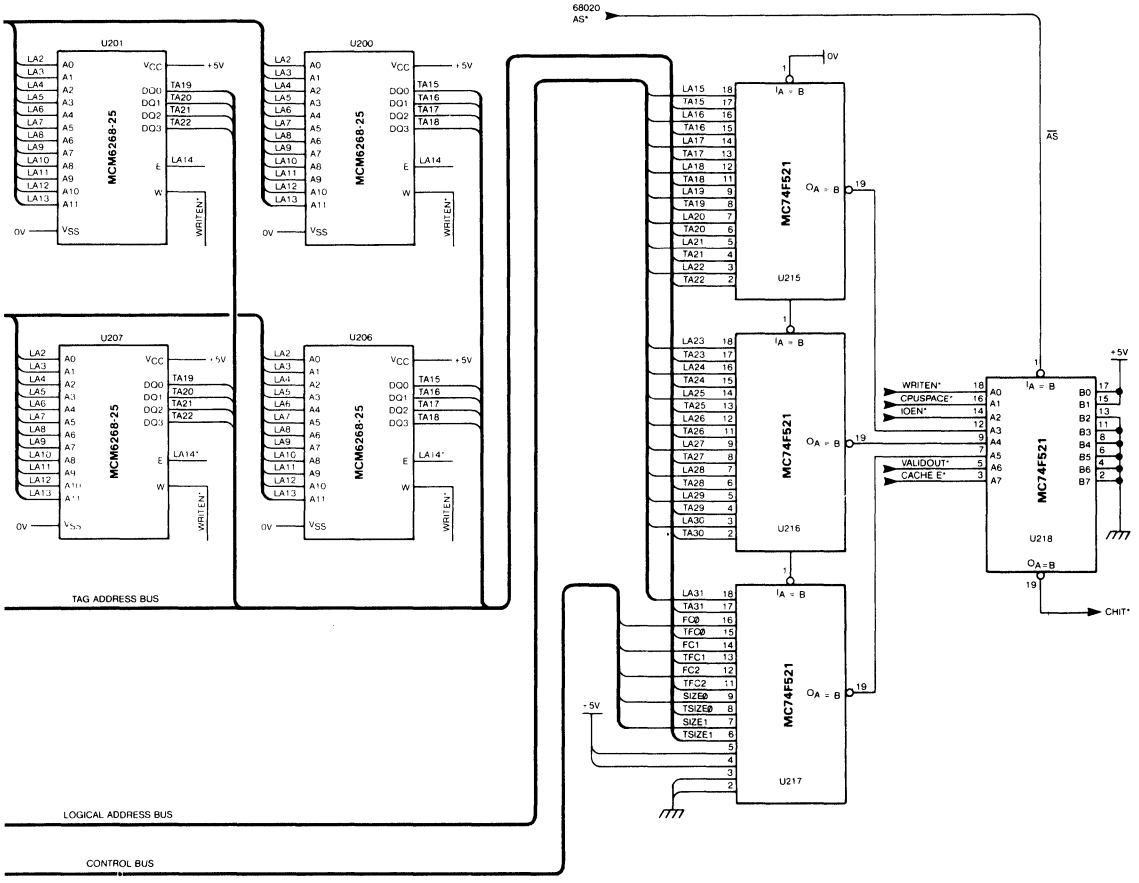


Figure 4: TAG Address RAMs


68020
AS*
U201
U200
U207
U206
MCM6268-25
+5V
0V
WRITEN*
LA14
LA14*
TA19
TA20
TA21
TA22
TA15
TA16
TA17
TA18
TAG ADDRESS BUS
U215
U216
U217
U218
MC74F521
WRITEN*
CPUSPACE*
IOEN*
VALIDOUT*
CACHE E*
CHIT*
LOGICAL ADDRESS BUS
CONTROL BUS

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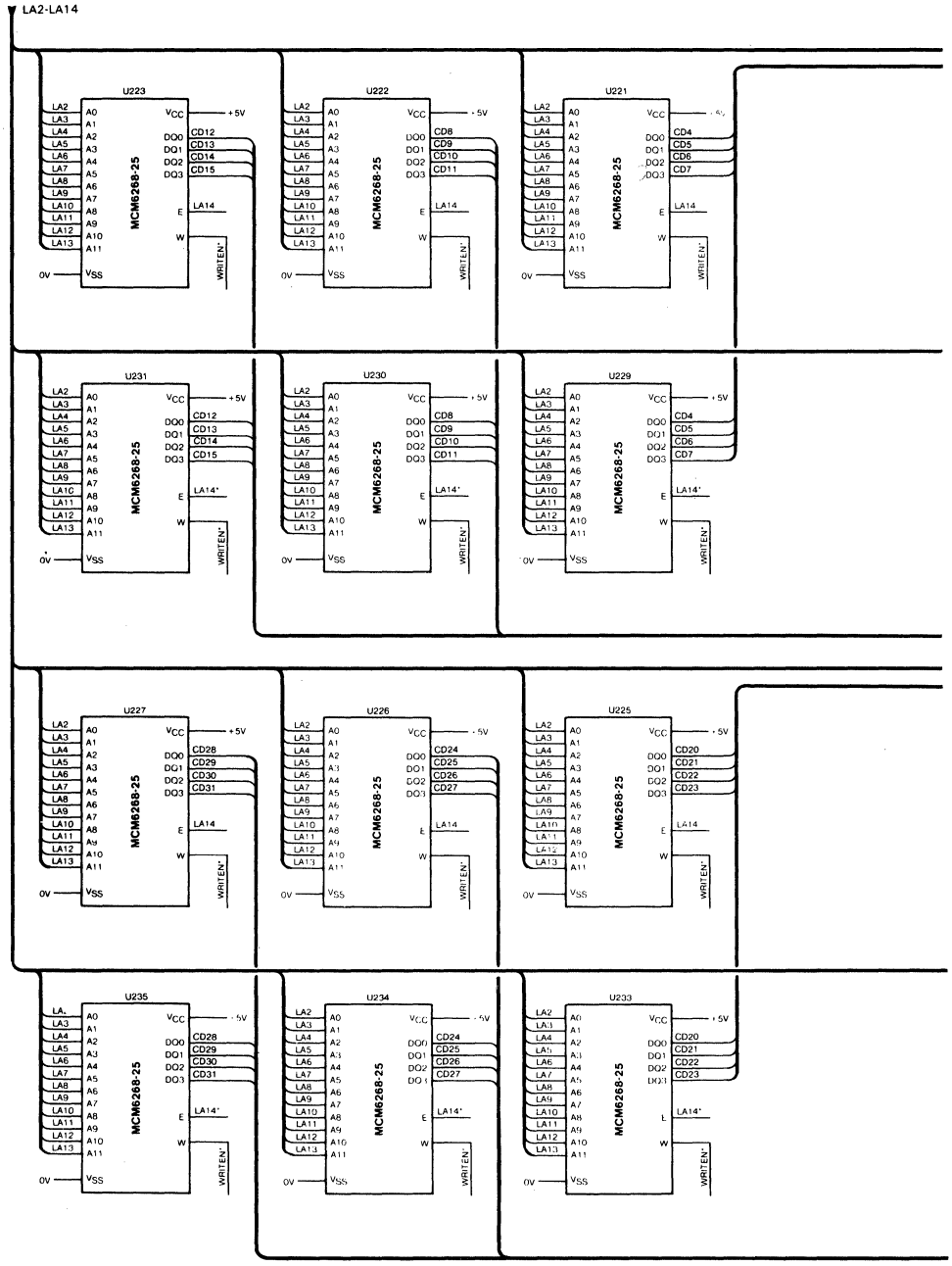

Figure 5: Cache Data RAMS

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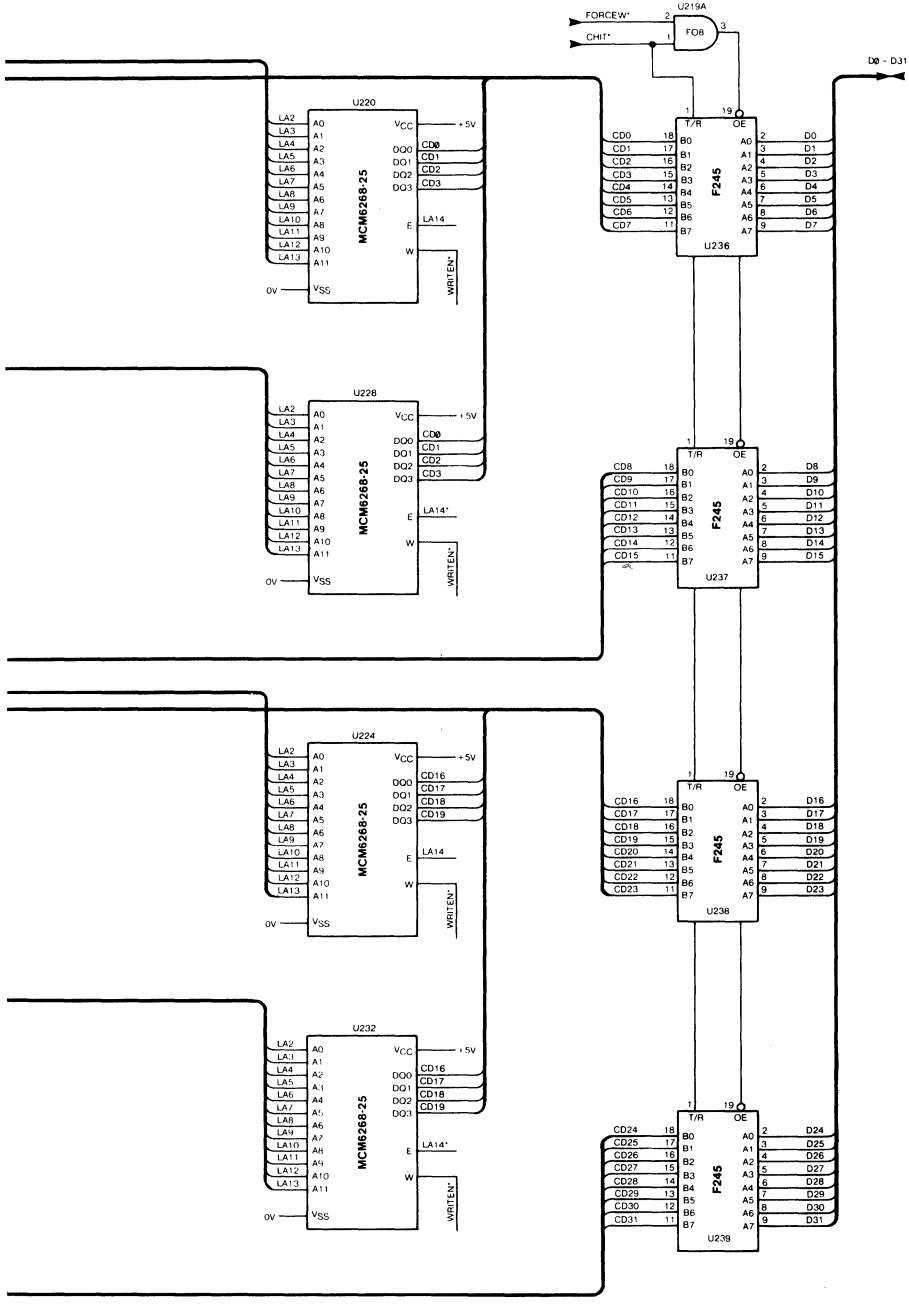
FORCEW*
CHIT*
U219A
FO8
D0 - D31
U220
U228
U224
U232
MCM6268-25
F245
U236
U237
U238
U239
LA2
LA3
LA4
LA5
LA6
LA7
LA8
LA9
LA10
LA11
LA12
LA13
+5V
0V
LA14
LA14*
WRITEN*
CD0
CD1
CD2
CD3
CD8
CD9
CD10
CD11
CD12
CD13
CD14
CD15
CD16
CD17
CD18
CD19
CD20
CD21
CD22
CD23
CD24
CD25
CD26
CD27
CD28
CD29
CD30
CD31
T/R
OE
D0
D1
D2
D3
D4
D5
D6
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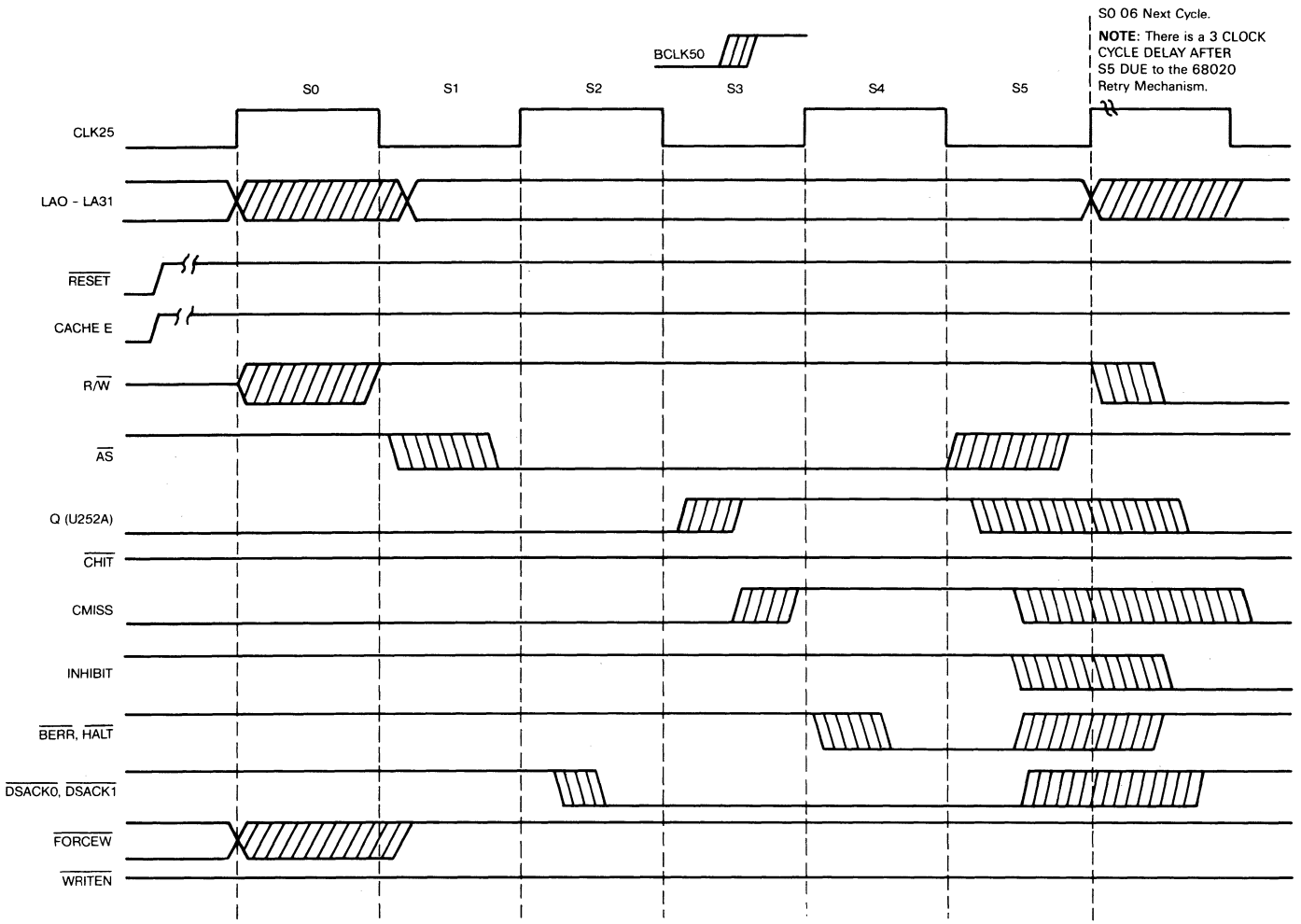
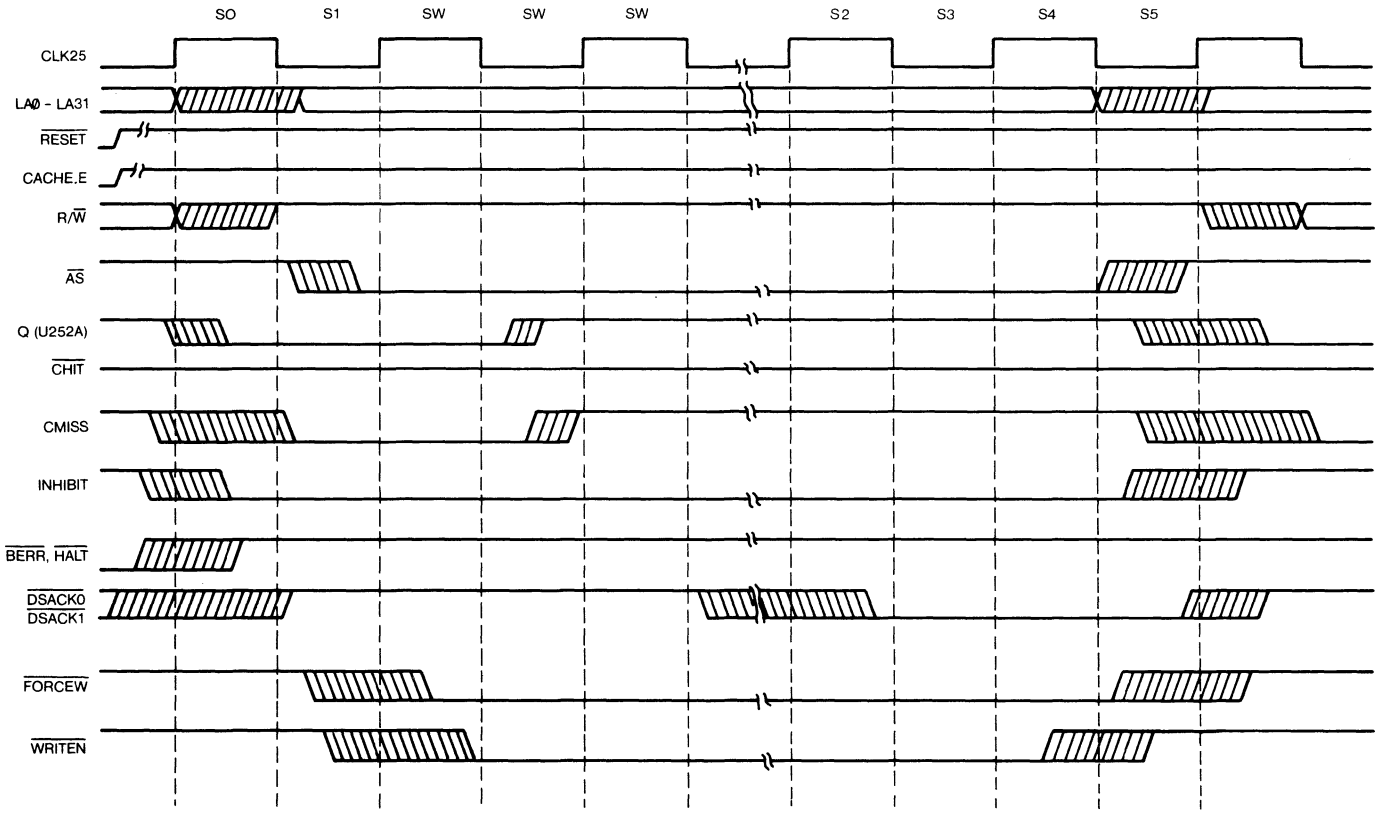
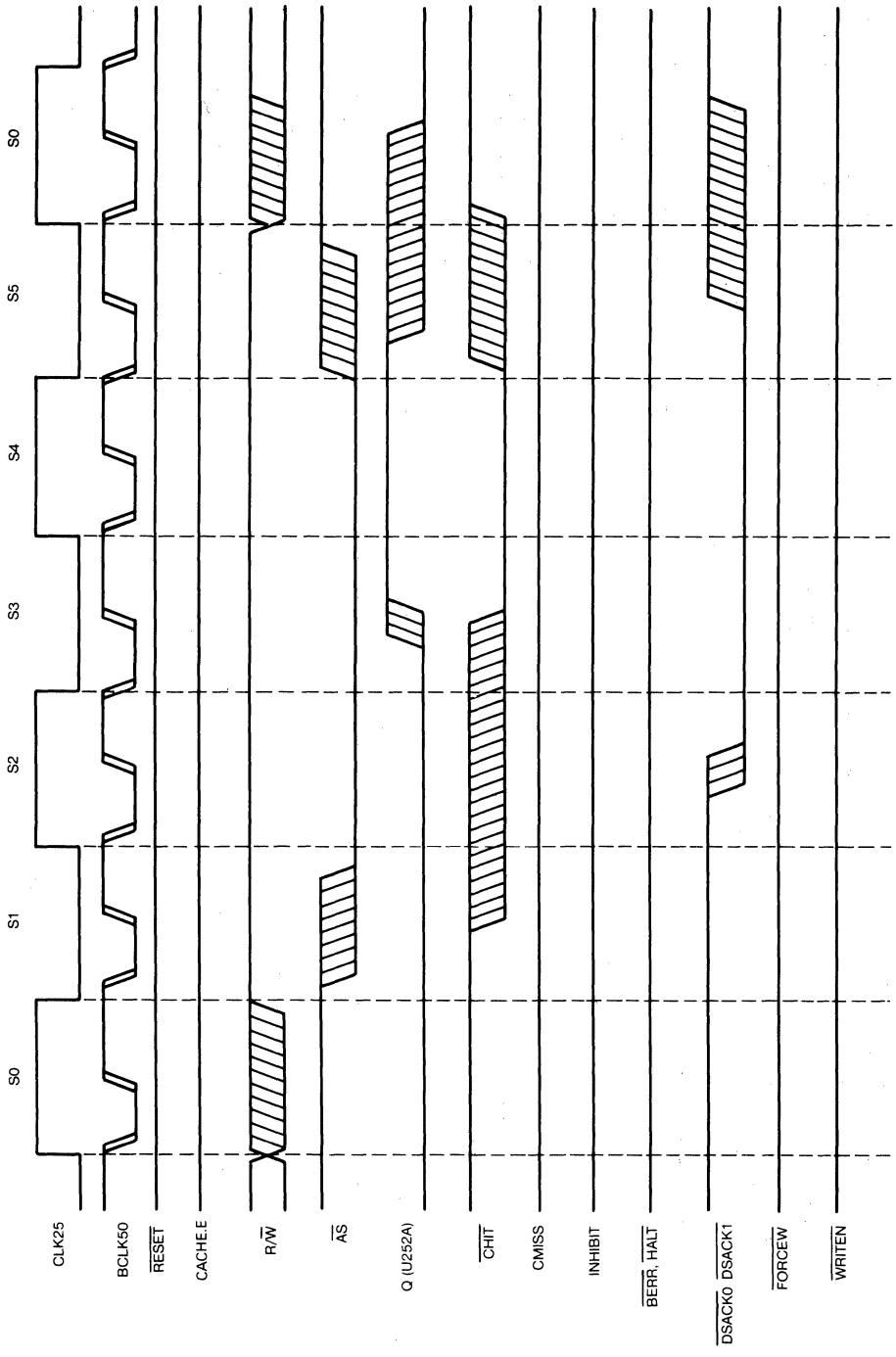


Timing Diagram 1 - Cache Miss



Timing Diagram 2 - Retry of the Cache Miss Cycle



Timing Diagram 3 – Cache Hit

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AR258

HIGH FREQUENCY SYSTEM OPERATION USING SYNCHRONOUS SRAMs

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INTRODUCTION

The market for semiconductor memory products suitable for today's high speed cache applications is changing dramatically as the demand for higher performance super mini, ASIC, and microprocessor based computers rapidly increases. This development has put heavy pressure on MOS memory suppliers for faster and faster static RAMs to support shorter and shorter processor cycle times. To utilize their full system performance, fast SRAMs require precise system control, long address hold times, and have tight write pulse requirements. They provide short data valid time, cause common I/O data contention, and offer low drive capability. Todays high performance processors themselves have similar I/O requirements. Therefore system designers have many concerns when designing a fast memory subsystem. They must use additional logic (latches, drivers, pulse generators, etc.) to allow the memory subsystem to interact efficiently with the processor at the fastest system cycle times.

A solution to get the memory and the processor to work well together at fast cycle and access times lies not only in faster components, but in minimizing the need for external glue logic and its associated delays. The Synchronous Static RAM is defined as having on chip latches for all its inputs and outputs, added drive capability, and a self timed write cycle all under the control of the system clock. This eliminates the need for most external logic chips and allows the memory to run at higher system speeds than standard SRAMs with comparable access times.

This paper outlines the basic architecture of a Synchronous SRAM that Motorola plans to introduce in the first half of 1988. We will highlight its advantages over standard SRAMs in high frequency computer system operation. This is followed by an application example for a MC68030 cache subsystem.

ARCHITECTURE AND OPERATION

ARCHITECTURE

A block diagram of the 16K × 4 Synchronous SRAM is shown in Figure 1. This diagram shows all inputs, outputs, and control signals ($\overline{W}$, $\overline{S}$, and K) to the part; addresses (A0-A13), data in (D0-D3), data out (Q0-Q3), clock (K), chip select ($\overline{S}$), and write enable ($\overline{W}$). All inputs, outputs, write enable, and chip select are latched by the clock.

The latches are one of two types, either positive edge triggered or transparent. The positive edge triggered latches are latched by the rising edge of clock (K). The transparent latches are frozen when the clock is in the high state and open when it is in the low state. Our parts feature two of the possible combinations of input and output latches. The first part, the MCM6292, features edge triggered latches on the inputs and transparent latches on the outputs. Our second part, the MCM6293, has edge triggered latches on both inputs and outputs, to aid in pipelining data.

The output buffers on all of our parts are capable of driving 130 pF loads. The output buffers were designed to drive this load because in some systems the latches that they replace would be required to drive a comparable size load. Due to the size of load that the output buffers must drive, and the speed at which the part operates, we have added an extra ground pin (V_{SSQ}). This pin is the ground connection for all of our output drivers, and allows us to drive our outputs harder and also gives us noise immunity on the ground bus.

For systems that require a common I/O configuration we expect to offer the MCM6295 and the MCM6294, which are the MCM6292 and the MCM6293 with an asynchronous output enable ($\overline{G}$) option. These parts, the MCM6294 and the MCM6295, replace the chip select ($\overline{S}$) buffer with an asynchronous output enable ($\overline{G}$) buffer.

OPERATION

The operation of these parts is much the same as a standard 16K × 4 SRAM except for the fact that the inputs and outputs are latched and the cycle begins with the low to high transition of the clock. The following examples will concentrate on a read and write cycle for both the MCM6292 and the MCM6293. The MCM6294 and MCM6295 read and write cycles are the same as the MCM6292 and the MCM6293 except that the outputs can be put into a high impedance state at any time by using output enable ($\overline{G}$).

During a read, see Figure 2, all inputs are latched into the part at the rising edge of the clock (K) in both the MCM6292 and the MCM6293. For the MCM6292, when clock goes high, the outputs become latched and are held in that state until the clock falls low. Since the output latches are transparent, during clock low time, there are two possible access times, t_{KHQV} and t_{KLQV}. These access times are dependent upon the high pulse width of the clock. If the high pulse width is less than the access time of the memory array the longer t_{KHQV} spec is the clock access time. However if the clock high pulse is longer than the memory array access time, the clock access time becomes t_{KLQV}. For the MCM6293 the

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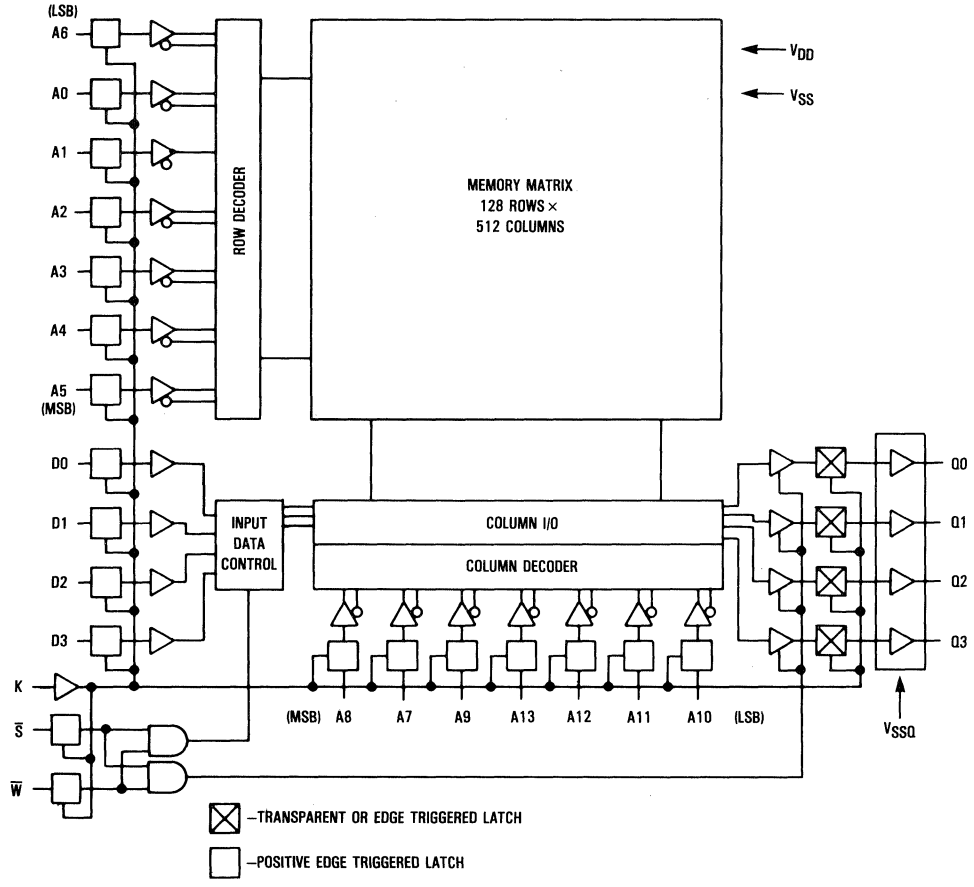


Figure 1. Synchronous SRAM Block Diagram

outputs transition only when the clock switches from low to high. The output data that is latched during the low to high transition of the clock is the data from the previous read cycle.

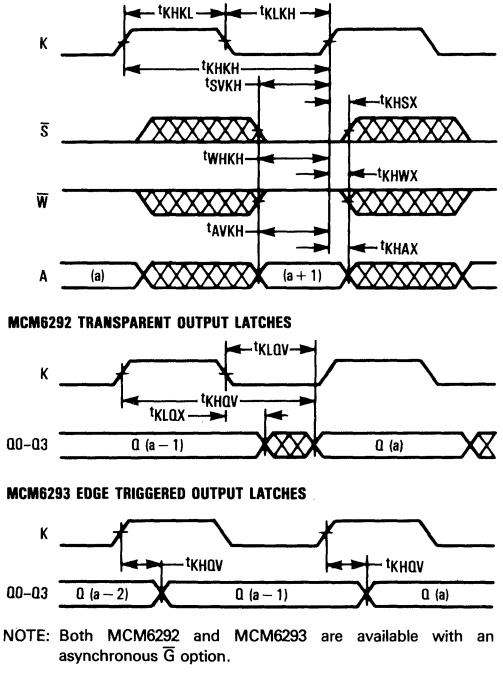
For the write cycle, see Figure 3, all inputs are handled in the same manner as in the read. Since both write enable and the input data are sampled on the rising edge of the clock the write becomes self timed. This eliminates the need for complex off chip write pulse generating circuitry. The outputs are put in a high impedance state t_{KLQZ} after the clock falls low for the MCM6292. In the MCM6293 the output buffers will not go into a high impedance state until the low to high transition of the clock at the beginning of the next cycle. The MCM6294 and the MCM6295 allow the user to put the output buffers into a high impedance state asynchronously by using the output enable input. This allows the user to put the output buffers into a high impedance state earlier in the cycle, which eases the data contention problem when the part is used in a common I/O system configuration.

SYSTEM ADVANTAGES (SRAM vs SSRAM)

SYSTEM DESCRIPTION AND TIMING

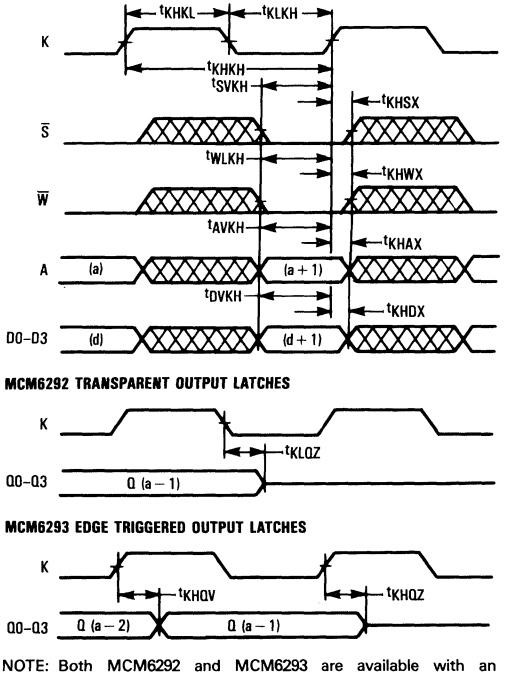
Figure 7 shows two examples of a 16K × 32 bit memory using standard parts. The systems shown require eighteen parts each, ten latches and eight 16K × 4 SRAMs, to implement the same function as eight synchronous SRAMs and no glue logic.

The functional equivalent of a MCM6292 is the standard 16K × 4 SRAM with edge triggered latches on the inputs and transparent latches on the outputs, as shown at the top of Figure 7. The parts used in this example are six 'F374 octal D-type flip flops, four 'F373 octal transparent latches, and eight 6288 16K × 4 SRAMs. The predicted timing diagram for the system is shown in Figure 4. This timing diagram compares the predicted system access with that of the MCM6292. In the timing diagrams an approximate skew of 5 ns was added to the address timing to allow for some propagation delay from the MPU or CPU. For the purpose of comparison, three timing



NOTE: Both MCM6292 and MCM6293 are available with an asynchronous $\overline{G}$ option.

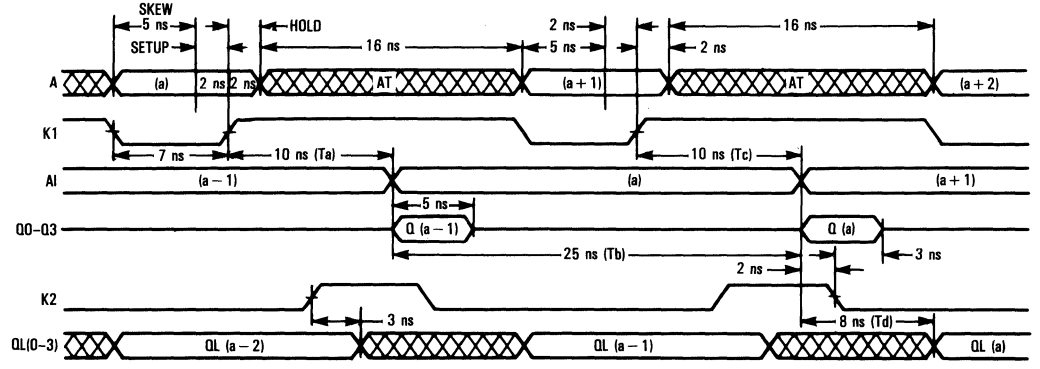
Figure 2. Read Cycle Comparison



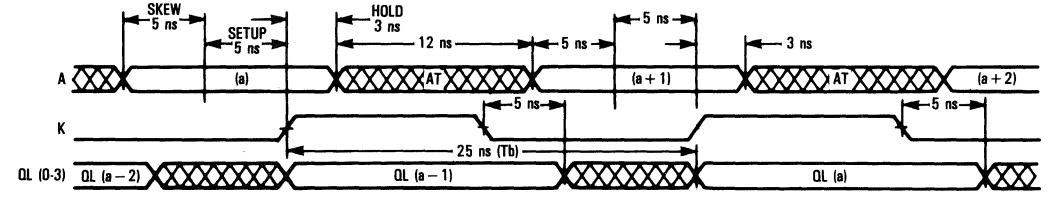
NOTE: Both MCM6292 and MCM6293 are available with an asynchronous $\overline{G}$ option.

Figure 3. Write Cycle Comparison

STANDARD SRAM WITH EDGE TRIGGERED LATCHES ON INPUTS AND TRANSPARENT LATCHES ON OUTPUTS (t_{AVQV} = 50 ns, t_{CYC} = 25 ns)



MCM6292 SYNCHRONOUS SRAM (t_{AVQV} = 35 ns, t_{CYC} = 25 ns)



NOTE: AT—Address generation and transition time.

Figure 4. Standard SRAM vs MCM6292 Timing Diagram

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parameters were calculated, t_{CYC} (cycle time), t_{AVQV} (address valid to data out valid time), and t_{KQV} (address clock valid to data out valid time). The equations used to calculate each of the timing parameters for the standard SRAMs are as follows:

$$t_{CYC} = Ta + Tb - Tc$$
$$t_{KQV} = Ta + Tb + Td$$
$$t_{AVQV} = skew + setup + Ta + Tb + Td \ .$$

The equivalent timing parameters for the MCM6292 can be determined as follows:

$$t_{CYC} = Tb$$
$$t_{KQV} = Tb$$
$$t_{AVQV} = skew + setup + Tb \ .$$

The equivalent circuit for the MCM6293, as shown at the bottom of Figure 7, is a 16K × 4 SRAM with positive edge triggered latches on both inputs and outputs. For this example the parts used are, eight 6288 16K × 4 SRAMs and ten 'F374 octal D-type flip flops. The timing diagrams for this example are shown in Figure 5. The equations for calculating the timing parameters are as follows:

Standard SRAMs:

$$t_{CYC} = Ta + Tb - Tc$$
$$t_{KQV} = Ta + Tb + Td + Te$$
$$t_{AVQV} = skew + setup + Ta + Tb + Td + Te$$

MCM6293:

$$t_{CYC} = Tb$$
$$t_{KQV} = Tb + Te$$
$$t_{AVQV} = skew + setup + Tb + Te$$

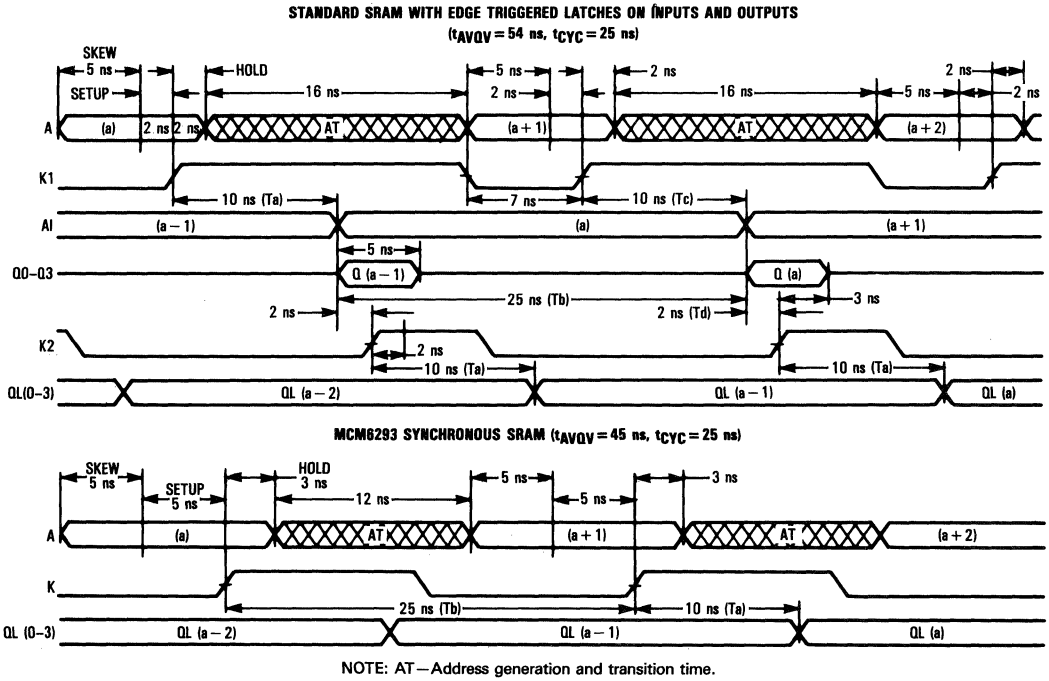
SYSTEM COMPARISONS

The timing parameters for the 25 ns 16K × 4 synchronous SRAMs and the equivalent circuits using 25 ns SRAMs are in Table 1. Also in Table 1 are timing parameters for other systems using progressively faster and more expensive SRAMs. From this table it can be determined that if either t_{AVQV} or t_{KQV} were the most important timing constraints a much faster SRAM would be needed to match the performance of the synchronous SRAM. For the performance of the system built with standard parts to match the performance of the 25 ns MCM6292, it would be necessary to use a 10 ns SRAM. Similarly, if the system used 25 ns MCM6293s the equivalent system made from standard parts would require 15 ns SRAMs.

Another important advantage of the synchronous parts over standard parts is the board level chip count; 18 parts are necessary when using standard SRAMs while only 8 parts are needed for the synchronous SRAM implementation. This is critical when board space is an important factor. Also, the fact that data and write enable are sampled on the rising edge of the clock, eliminates the need for complex write pulse generating circuitry. Finally, in order to get the high speed performance out of standard SRAMs, it requires precise timing and phase control of two clock signals (K1 and K2), while in the synchronous part only one clock (K) is needed.

APPLICATION: MC68030 CACHE SUBSYSTEM

The Synchronous SRAM combined with the Motorola MC68030 microprocessor illustrates the potential of this advanced memory architecture. The high frequency performance of microprocessors like the MC68030 can be impaired by having



NOTE: AT—Address generation and transition time.

Figure 5. Standard SRAM vs MCM6293 Timing Diagram

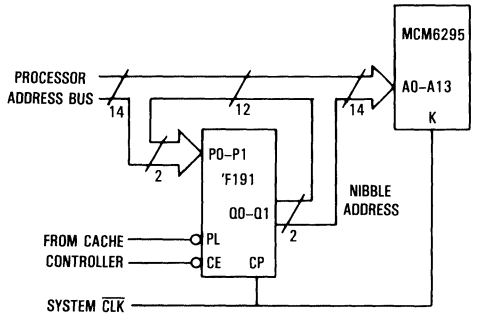


Figure 6. MC68030 Burst Read Addressing

to wait for slow memory to respond. For this example we will use a 16K by 32-bit cache system running at frequencies of up to 33-1/3 MHz. This does not mean that you can purchase MC68030 processors today at this speed, only that our 25 ns SSRAM will support this processor up to that speed. The MC68030 timings used for this example are extrapolated from the current 16.67 and 20 MHz specifications that exist today and are not intended to be the official specifications.

We will exploit the processor's burst read cycle which supports burst filling of its on-chip instruction and data caches, adding to the overall system performance. The on-chip caches are organized with a block size of four long words, so that there is only one tag for the four long words in a block. Since locality of reference is present to some degree in most programs, filling of all four entries when a single entry misses can be advantageous, especially if the time spent filling the additional entries is minimal. When the caches are burst-filled, data can be latched by the processor in as little as one clock for each 32 bits.[1]

The timing diagram shown in Figure 8 shows a burst read cycle (four 32-bit words read) in a 3-1-1-1 clock cycle configuration. The first word is read in 3 clock cycles and the remaining three words are read in one clock cycle each. The burst read cycle begins with a cache burst request ($\overline{\text{CBREQ}}$) from the processor followed by a cache burst acknowledge ($\overline{\text{CBACK}}$) from the memory controller. This means the processor is requesting a burst cycle and the accessed memory can comply. During the burst cycle the processor supplies the starting address in the normal synchronous fashion and holds it valid until all four long words are read. It does not provide the next three addresses required to complete the burst fill, so they must be generated off chip. For this example we used a 'F191 counter whose control signals, PL and $\overline{\text{CE}}$, are generated in a cache controller. The clock input, CP ($\overline{\text{CLK}}$), is the opposite phase of the system clock. The SSRAM operates with the same inverted system clock ($\overline{\text{CLK}}$) and receives its addresses from two sources; A2–A13 are supplied from the processor's address bus, and A0–A1 are supplied from the 'F191 counter to allow nibble counting as shown in Figure 6.

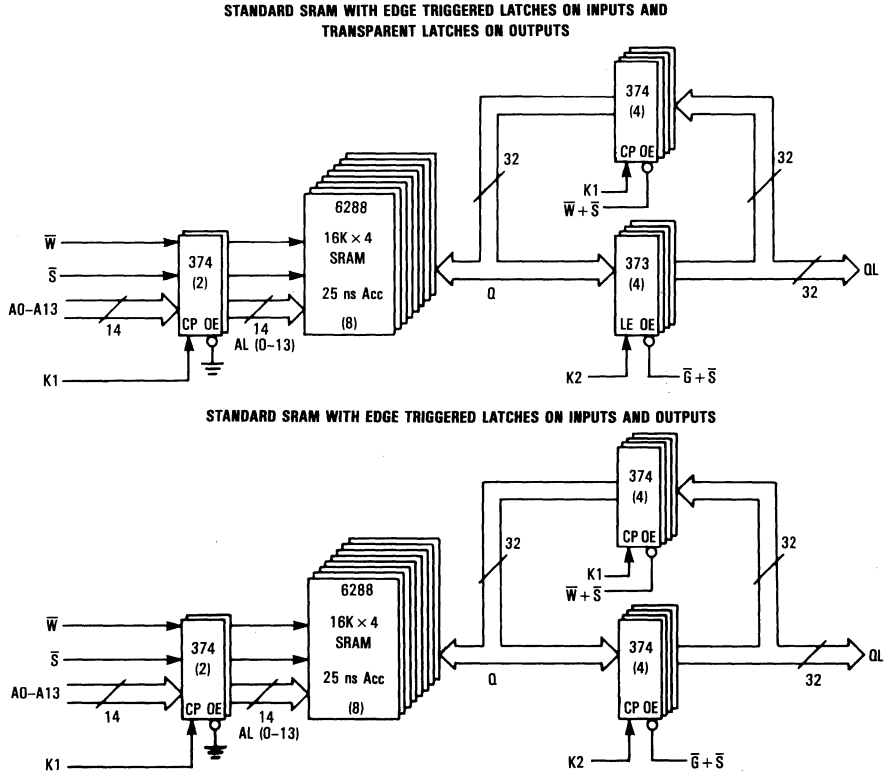
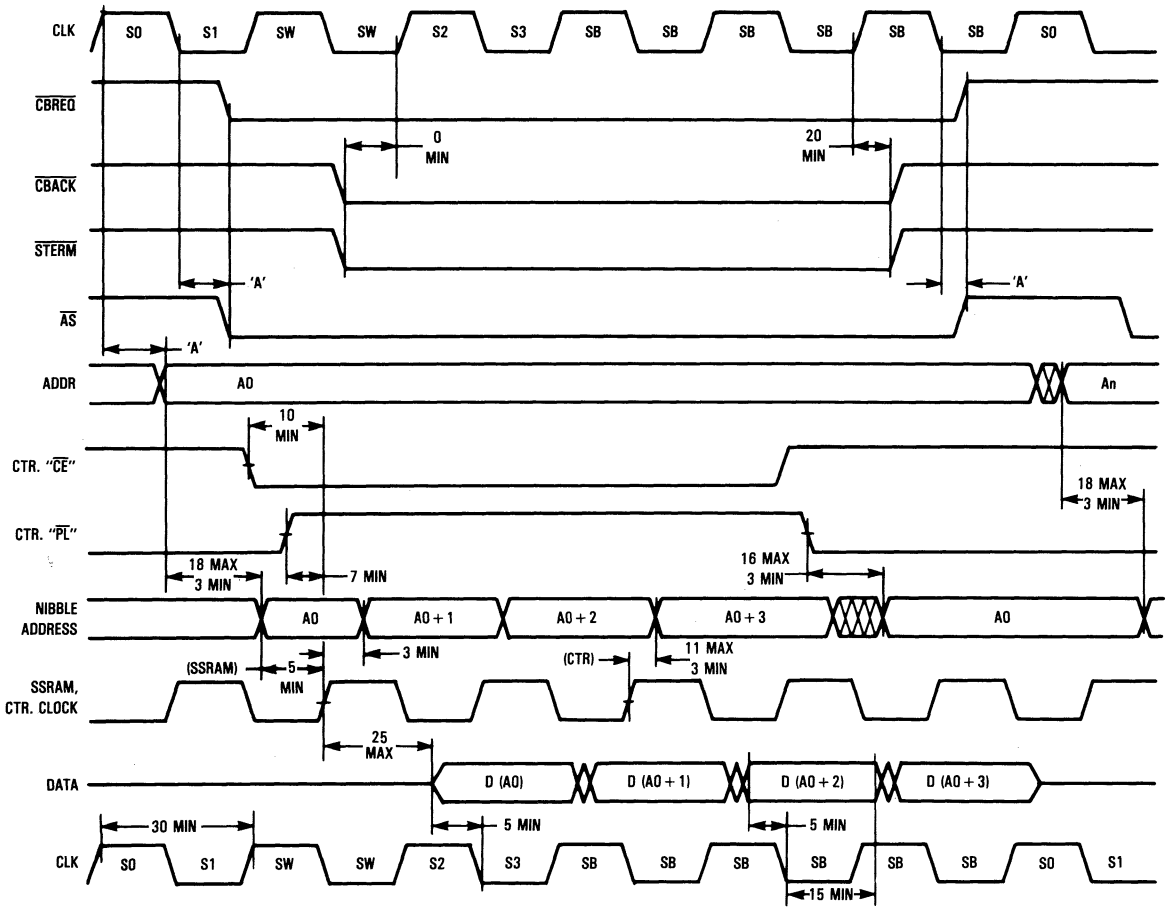


Figure 7. Standard SRAM Implementations

11



NOTES: 'A' ~ (minimum clock period)/2 CTR. = counter ('F191)

Figure 8. MC68030 Burst Fill Timing

Table 1. Timing Comparisons Between SSRAMs and SRAMs

Timings	25 ns SSRAM		25 ns SRAM		20 ns SRAM		15 ns SRAM		10 ns SRAM	
	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output	Trans. Output	Edge Trig. Output
t_{CYC}	25 ns	25 ns	25 ns	25 ns	20 ns	20 ns	15 ns	15 ns	10 ns	10 ns
t_{AVQV}	35 ns	45 ns	50 ns	54 ns	45 ns	49 ns	40 ns	44 ns	35 ns	39 ns
t_{KQV}	25 ns	35 ns	43 ns	43 ns	38 ns	38 ns	33 ns	33 ns	28 ns	28 ns

The timing begins with the request, the acknowledgment and the generation of the first address. This address is used to access one of the four long words. Two low order address signals from this address must also be loaded into the counter. At the beginning of the cycle the parallel load signal for the counter is enabled, the address is then loaded in and the PL signal can be disabled. The counter will provide the memory this first address a propagation delay later and then increment it on successive clock edges to supply the memory with the remaining three needed addresses. After receiving all four 32-bit words the processor is free to continue.

A similar system built using standard MCM6288 (16K × 4) type SRAMs would require the use of off-chip input and output latches ('F373 or 'F374 type) in addition to the counter. It would require four chips to perform the latching function for 32-bit data in, and four chips to latch the 32-bit data out, for a total of eight additional 20 pin packages added to the memory PC board. This standard SRAM cache system would also require additional logic in the cache controller to support the write pulse, associated write enable and data in timing for write cycles, and the generation of a second clock (LE or CP) to separately control the input and output latches. To attain the cache system speed of 33-1/3 MHz would require a SRAM access time of approximately one bin faster than the SSRAM. In addition the external glue logic would have to be faster than what is currently offered in the 74F series logic.

SUMMARY

There are many applications for high-speed Synchronous Static RAMs. The integration of latches, self timed writes, bus drive capability, and clock control greatly simplifies system level implementation and ease of use. These features will allow SSRAMs to continue to support higher frequency system operation. Depending on the application, Synchronous Static RAMs can provide up to a 10 to 15 ns improvement in system access time over SRAMs that spec the same chip speeds. They save precious board space by reducing the chip count, and simplify controller design for latch control and write cycles.

ACKNOWLEDGMENTS

The authors would like to thank Brian Branson and Bill Martino for their inputs and comments that helped complete this paper. And special thanks to Richard Crisp for his MC68030 cache system timing analysis.

REFERENCES

1. Motorola Semiconductor Technical Data: "Technical Summary: Second Generation 32-Bit Enhanced Microprocessor", 1986.
2. Motorola Semiconductor Technical Data: "Fast and LS TTL Data", 1986.

Motorola Inc. can provide the usual promotional and technical literature associated with the Synchronous Static RAM family.

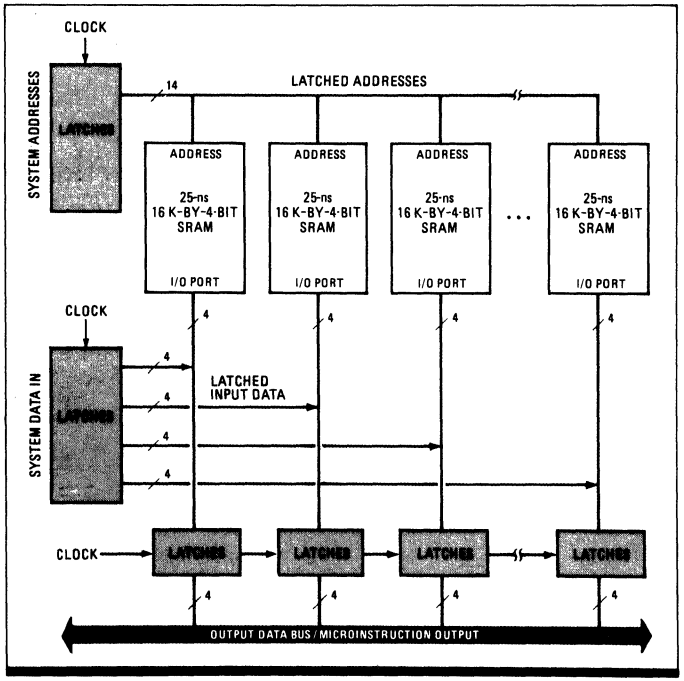
MOTOROLA'S RADICAL SRAM DESIGN SPEEDS SYSTEMS 40%

Key to higher throughput is a synchronous clocked architecture and on-chip I/O latches; the combination cuts interconnection delay by up to 20 ns

by Bernard C. Cole

Engineers at Motorola Inc.'s MOS Memory Products Division are taking a radically different approach from the current asynchronous architecture for static random-access memories. They are developing a synchronous architecture the company claims will improve system throughput by as much as 40% and will reduce system component count by as much as 50%.

The keys to the Austin, Texas, division's new architecture are: replacing the traditional self-clocked address-transition-detection circuitry, found in conventional asynchronous SRAMs, with a synchronous clocked architecture, and adding critical input and output latches on-chip. The combination of these features eliminates as much as 8 to 10 ns of interconnection delay on input and on output, says William Martino, the division's design manager for specialized memories. It also eliminates circuitry often required to make asynchronous devices appear synchronous in high-performance cache-memory systems, which depend heavily on the synchronization of critical timing parameters. Also incorporated on the chip are drive transistors capable of driving buses with capacitive loads of up to 130 pF without additional external circuitry. Motorola designers also enlarged the geometries to increase the inherent drive capability of the devices.



1. ASYNCHRONOUS. Using asynchronous SRAMs, designers of high-performance synchronous systems must incorporate latches on the inputs and outputs, adding 15 to 20 ns of delay.

The new architecture has been incorporated into four initial products that are members of a new family of 16-Kbit-by-4-bit SRAMs with cycle times ranging from 25 to 35 ns and access times in the 10 to 35 ns range. This equals that of comparably sized asynchronous SRAMs fabricated with the same 1.5-μm double-metal CMOS process [*Electronics*, Aug. 7, 1986, p. 81], says Frank Miller, synchronous SRAM project leader at the division. But Miller emphasizes that the elimination of as much as 20 ns of interconnection delay can almost double system-level performance.

Motorola expects to offer samples of the four clocked synchronous SRAM parts within about a month and plans to be in volume production by the end of the fourth quarter. Two of the devices, the MCM6292 and 6295, incorporate level-sensitive transparent latches,

whereas the MCM6293 and 6294 use positive-edge-triggered latches. Also the 6294 and 6295 each have an output enable pin that allows the user asynchronous control of the output buffers, allowing the parts to be used in common I/O at the board level. All the devices feature an active ac power dissipation of 600 mW and an active dc power of only 100 mW.

The advantages of Motorola's new family of synchronous SRAMs outweigh the advantages of asynchronous devices, Martino says. In asynchronous devices, great reliance is placed on address-transition detection, a self-clocking scheme that uses the address-signal transition, or edge, as a reference to synchronizing all operations on the chip to that signal. Martino says that asynchronous SRAMs are widely used because they allow and recognize address changes at any time. As a result, no external global clock is necessary to access data, making them easy to use. Also, compared with dynamic RAMs, asynchronous SRAMs take much less external circuitry, says Miller. Because they are free-running, the addresses can be changed whenever needed, and they are very easy to control.

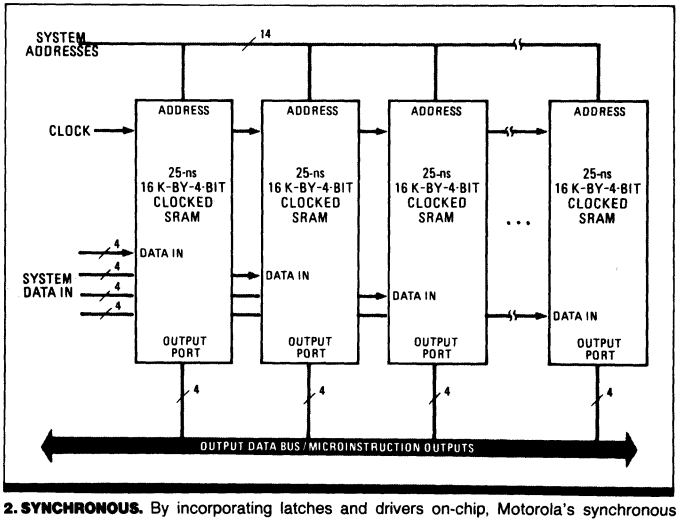
Although they are easy to use, asynchronous SRAMs must be surrounded by considerable external logic (see fig. 1) in many applications in high-performance processor systems such as writable control stores, data caches, and cache-tag memories [*Electronics*, June 11, 1987, p. 78] that require synchronous operation. The extra circuitry imposes a considerable performance penalty, and that can be a problem in cache applications in particular, says Martino, where the speed of memory typically must be at least an order of magnitude faster than main memory. Also, for a cache to work properly, critical timing relationships must be preserved so that a variety of simultaneous operations can be coordinated, such as searching the tag store, getting data out of cache, and replacing proper entries in the cache. The added delay of the external logic can make it difficult to preserve these relationships.

When system speeds were in the 200-ns range, Miller says, the additional 10-to-20-ns penalty of this external logic could be tolerated. "But with processor speeds improving so dramatically, now pushing below 100 ns toward 50 ns, this is a penalty that is critical, especially since the speed of the external logic has not kept pace with the improvements in speed at the chip level."

Depending on the type of register involved and the process used, the delay time, even with high-performance logic families, can be reduced to no more than 7 to 10 ns, says Martino. As a result, most speed improvements have come by pushing the speed of the memory chips themselves. But, as processors speed up, memories with sufficiently low access times are getting harder and harder to produce inexpensively, Martino says. Current 25-to-35-ns asynchronous SRAMs are barely adequate, he says. And newer processors will require a system throughput of no more than 35 to 40 ns. For such throughputs, SRAMs must be pushed to below 10 ns, only achievable now with bipolar and BiCMOS circuits, but at much higher power. "However, even if parts are pushed down to 1 ns and under, there is still that 10 ns on the input and another 10 ns on the output to deal with," says Martino.

The most important element in Motorola's new SRAM architecture (see fig. 2) is the incorporation of the external input and output latches necessary for synchronous operation on board. This design considerably simplifies system design and reduces interconnection delay. "By pulling all of that glue logic on board, it is no longer necessary to drive a large bus to TTL levels," says Martino. "It is now done on-chip, reducing the 10-ns delay down to picosecond levels. This allows the use of a 25-ns part for a 25-to-30-ns bus, rather than using more expensive, power-hungry 10- and 15-ns parts for the same chore."

The Motorola architecture uses address-input latches to hold the addresses so that the processor does not have to hold the addresses valid for the entire cycle. A similar function is served by the data latches on the input. The latches on the output, however, serve a dual function. First, they provide a longer setup and hold time over which the data is valid on the bus, necessary in most processing systems. With a



2. SYNCHRONOUS. By incorporating latches and drivers on-chip, Motorola's synchronous SRAM reduces chip count by more than 50% and reduces interconnection delay.

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standard SRAM at minimum cycle time, that time is about 5 ns without any external latching. This is not enough time for most systems, which require the data to be on the bus for at least 15 to 20 ns, for the processor to receive the valid data. The other function of the latches is to provide the extra drive needed to drive the buses with capacitive loads of up to 130 pF.

The designers of the new SRAMs have eliminated the address-detection-transition circuitry; now they use on-chip clock input for a synchronous clocking scheme

Also incorporated on-chip to support the synchronous operation of the latches is a clock input that controls when the latches are transparent and when they are brought into play. Usually this clock input is a derivative of the system clock; that is, the latches are controlled by the edge of the system clock.

The Motorola designers have eliminated the address-detection-transition circuitry in the new SRAMs. Instead, they use the on-chip clock input to incorporate a synchronous clocking scheme in which the necessary address, data, chip-select, and write-enable information previously brought on board the chip by the address-detection-transition circuitry is now accessed at the beginning of the cycle in reference to the external clock, rather than to the address edge as in the asynchronous scheme. The technique, says Martino, is similar to how a DRAM brings in its addresses with setup and hold times in relation to a read-access or column-access signal input. "Since this device employs a clock with a high-going edge at the beginning of each cycle, it is no longer necessary to detect address- transitions," he says. "The system will tell the chip when to supply the necessary information by providing the clock at the appropriate time."

To eliminate the external drive circuitry, the inherent drive capability of the devices was increased fourfold, says Miller. So Motorola designers enlarged the geometries used to fabricate the pull-up and pull-down transistors, typically on the order of 1,500 μm wide, compared with 400- to 600-μm widths on the standard 30-pF devices, and as small as 6 μm in the memory array and 80 μm in the peripheral circuitry. Moreover, to achieve higher speed in spite of the higher drive currents, n-channel devices, which are only output devices, were used rather than the slower p-channel devices. Furthermore, these output devices were speeded up by incorporating a separate ground-supply pin for the output drivers. "This allowed us to burn more current in the output drivers without corrupting the operation of the rest of the circuit," Miller says.

Although this required a substantial increase in the area devoted to the drive circuitry, the chip size, 146 by 404 mils, is not substantially larger than comparable 64-Kbit asynchronous SRAMs. The extra area required for the larger drivers and for the internal clocking circuitry is offset by the area eliminated by removal of the address-transition-detection circuitry required on asynchronous parts, Martino says. □

INGENIOUS SRAM DESIGN WAS DONE IN REMARKABLY SHORT TIME

For a memory device of such complexity and ingenious design, Motorola's new clocked synchronous static random-access-memory design was completed in a remarkably short time—only 12 months. Moreover, most of the work was done by a four-person design team: William Martino, design manager for specialized memories; Frank Miller, synchronous SRAM project leader; chip designer Scott Remington; and layout engineer Richard Southerland.

One reason for the fast turnaround was that the array and much of the peripheral circuitry is identical to what was used in the company's family of asynchronous 64-Kbit SRAMs, says Miller. "All we had to do was strip off those portions of the circuit relating to the asynchronous operation and replace them with new synchronous elements."

The team drew from two sources for the features incorporated into the synchronous design—including their cumulative design experience. Miller has seven years' experience in memory design. Remington, an eight-year Motorola veteran, worked on the company's 64-Kbit and 1- Mbit DRAMs. Southerland, a five-year Texas Instruments veteran, worked on most of Motorola's asynchronous SRAMs in his two years with the company.

EXPERTS. Miller, Southerland, and Remington, from left, are old hands at memory design.

The other source was extensive input from Motorola's customers. "We spent several months defining a variety of special-application memory devices, from dual-port SRAMs and video DRAMs to content-addressable memories," says Miller. "But when we started taking these designs around to customers for input, we found they were most concerned with ways to make standard parts work better. For designers of high-performance systems using cache architectures, one of the largest common denominators was complaints that they had to surround the asynchronous parts with a variety of glue logic to operate appropriately in a synchronous environment.

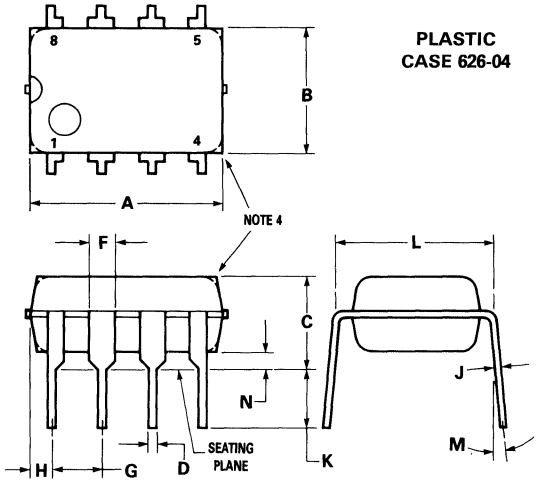
"The key is listening to the customers, finding out what their specific complaints are, and coming up with parts that satisfy those needs."

Mechanical Data 12

MECHANICAL DATA

Package availability and ordering information are given on the individual data sheets.

8-PIN PACKAGE

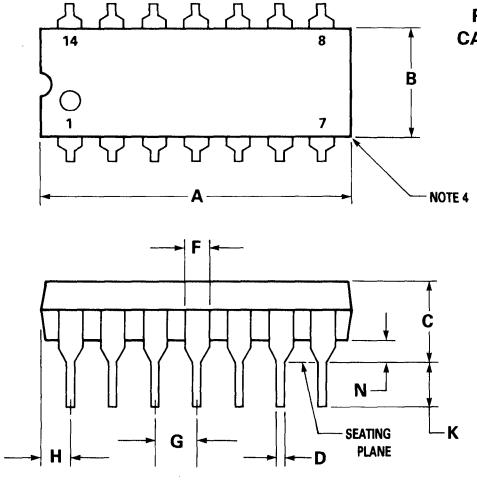


PLASTIC
CASE 626-04

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.51	0.76	0.020	0.030

NOTES:
1. LEAD POSITIONAL TOLERANCE:
   ϕ | ϕ 0.13 (0.005) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
4. DIMENSIONS A AND B ARE DATUMS.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

14-PIN PACKAGE

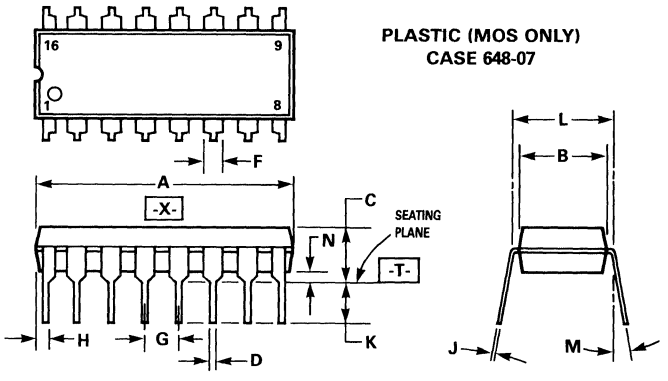


PLASTIC
CASE 646-06

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL; AS SHOWN IN PREVIOUS ISSUE.

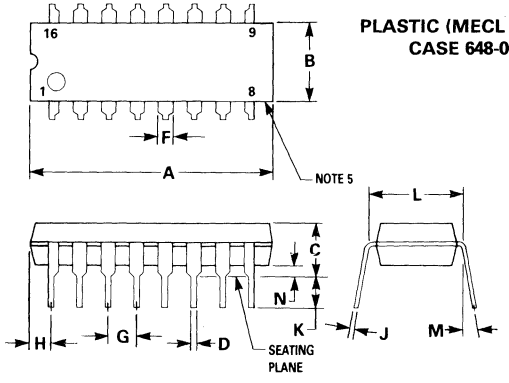
12



PLASTIC (MOS ONLY)
CASE 648-07

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76 REF		0.030 REF	
J	0.20	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.49	7.75	0.295	0.305
M	0°	10°	0°	10°
N	0.51	1.01	0.020	0.040

NOTES:
1. LEAD POSITIONAL TOLERANCE: ⌖ | 0.25 (0.010) Ⓜ | T | X Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. F DIMENSION IS FOR FULL LEADS.
5. ROUNDED CORNERS OPTIONAL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
7. CONTROLLING DIMENSION: INCH.

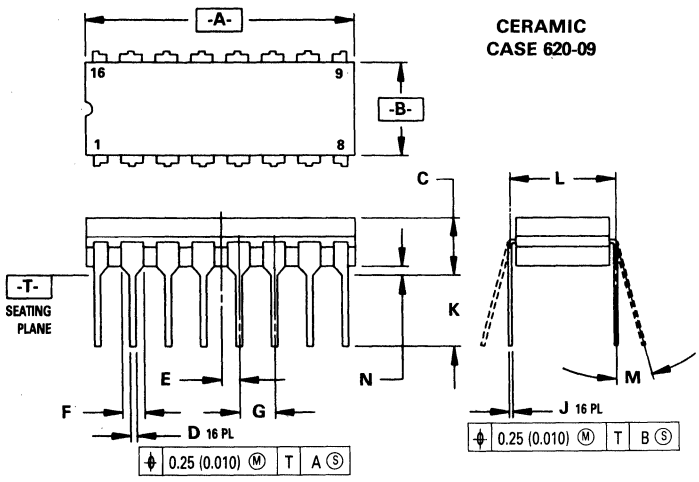


PLASTIC (MECL ONLY)
CASE 648-06

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	21.34	0.740	0.840
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.040

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL; AS SHOWN IN PREVIOUS ISSUE.

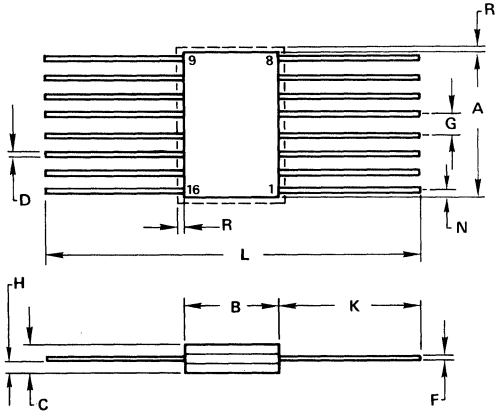
12



CERAMIC
CASE 620-09

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.55	0.750	0.770
B	6.10	7.36	0.240	0.290
C	—	4.19	—	0.165
D	0.39	0.53	0.015	0.021
E	1.27 BSC		0.050 BSC	
F	1.40	1.77	0.055	0.070
G	2.54 BSC		0.100 BSC	
J	0.23	0.27	0.009	0.011
K	—	5.08	—	0.200
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.39	0.88	0.015	0.035

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

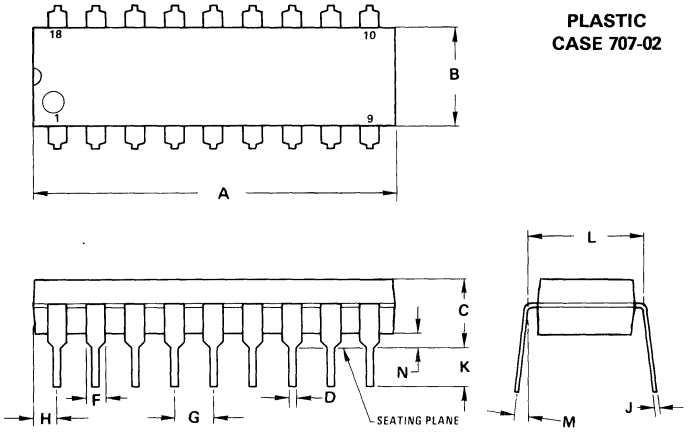


CERAMIC
CASE 650-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.40	10.16	0.370	0.400
B	6.22	7.24	0.245	0.285
C	1.52	2.03	0.060	0.080
D	0.41	0.48	0.016	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

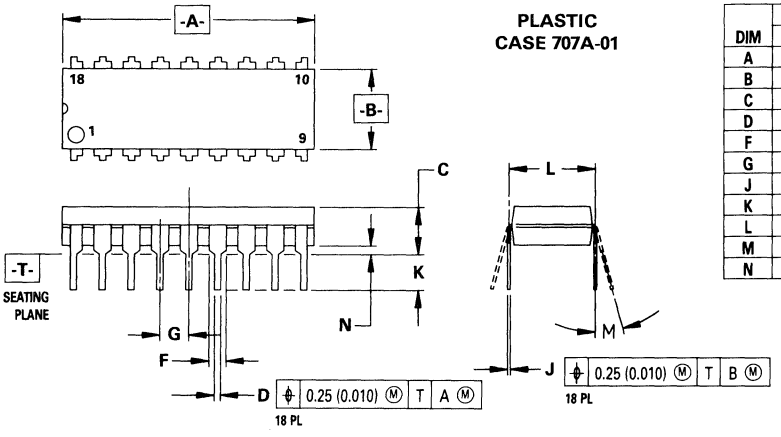
12



PLASTIC
CASE 707-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

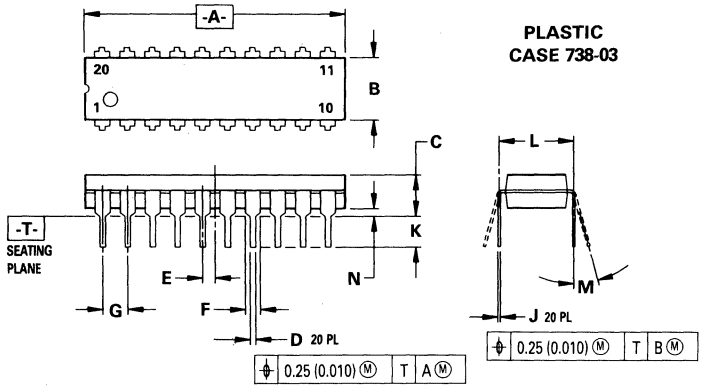


PLASTIC
CASE 707A-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	21.85	22.35	0.860	0.880
B	7.12	7.49	0.280	0.295
C	3.56	4.57	0.140	0.180
D	0.36	0.55	0.014	0.022
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	2.93	3.42	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

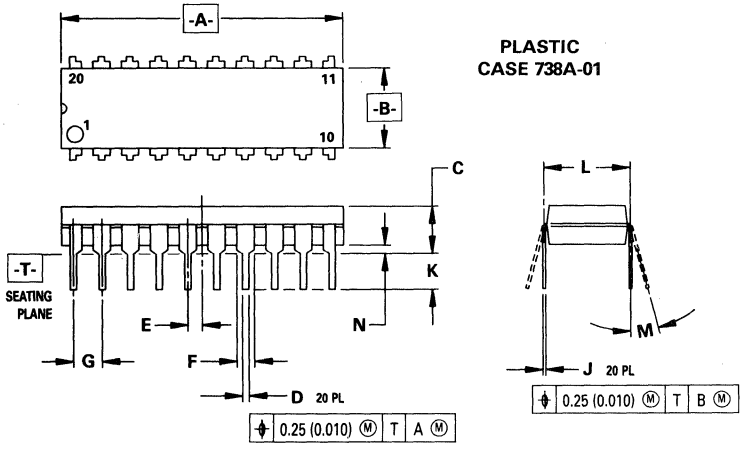
12



PLASTIC
CASE 738-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

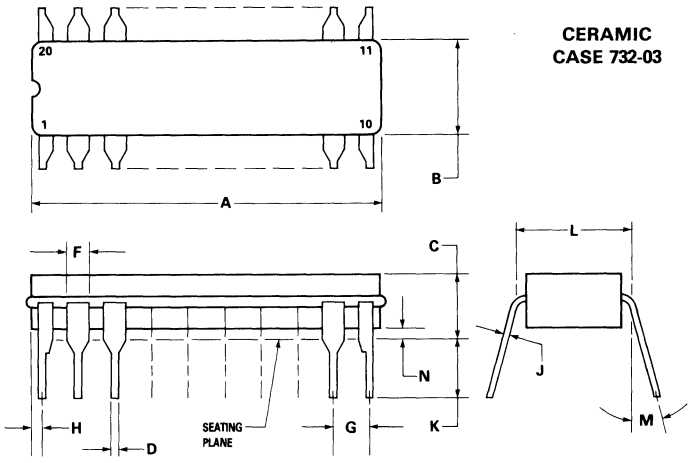


PLASTIC
CASE 738A-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.39	24.89	0.960	0.980
B	7.12	7.49	0.280	0.295
C	3.69	4.44	0.145	0.175
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.

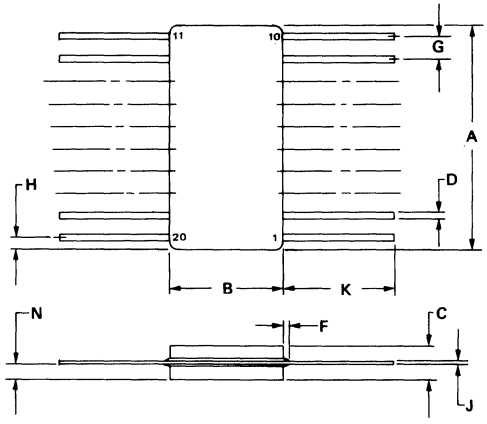
12



CERAMIC
CASE 732-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

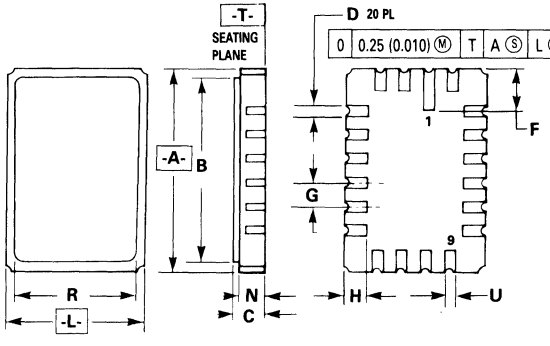
NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.



CERAMIC
CASE 737-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	13.08	–	0.515
B	5.84	7.11	0.230	0.280
C	1.52	2.16	0.060	0.085
D	0.41	0.46	0.016	0.018
F	–	0.25	–	0.010
G	1.27 BSC		0.050 BSC	
H	1.14	1.40	0.045	0.055
J	0.08	0.13	0.003	0.005
K	–	9.14	–	0.360
N	–	1.02	–	0.040

NOTE:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.



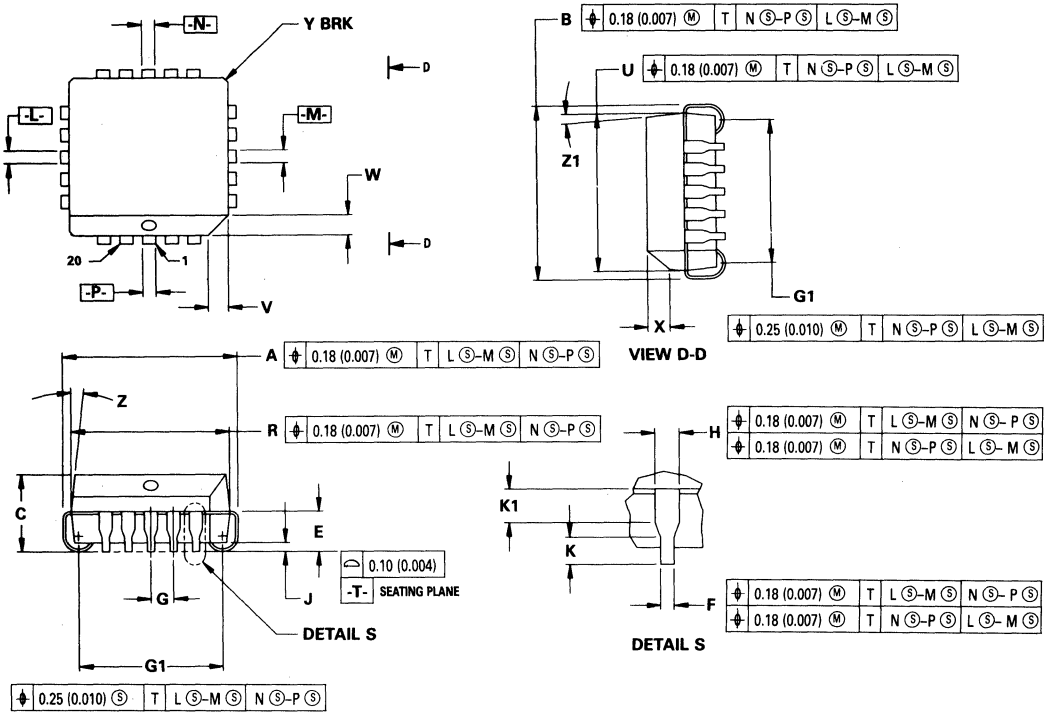
CERAMIC
CASE 756C-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	10.67	10.92	0.420	0.430
B	10.09	10.41	0.400	0.410
C	1.68	1.98	0.066	0.078
D	0.56	0.71	0.022	0.028
F	2.11	2.46	0.083	0.097
G	1.27 BSC		0.050 BSC	
H	1.07	1.21	0.042	0.048
L	7.24	7.49	0.285	0.295
N	1.40	1.65	0.055	0.065
R	6.61	6.85	0.260	0.270
U	0.28	0.53	0.011	0.021

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

12

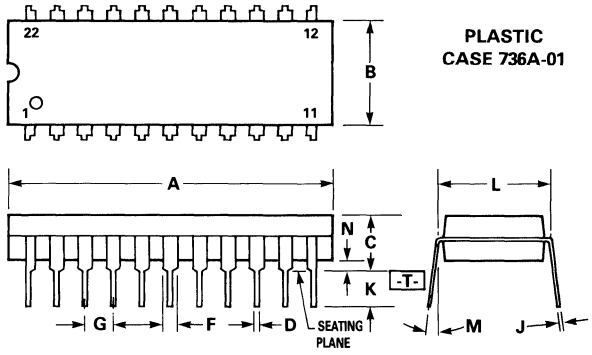
PLASTIC CHIP CARRIER
CASE 775-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51	—	0.020	—
K	0.64	—	0.025	—
R	8.89	9.04	0.350	0.356
U	8.89	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y	—	0.50	—	0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02	—	0.040	—
Z1	2°	10°	2°	10°

NOTES:
1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM GI, TRUE POSTION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

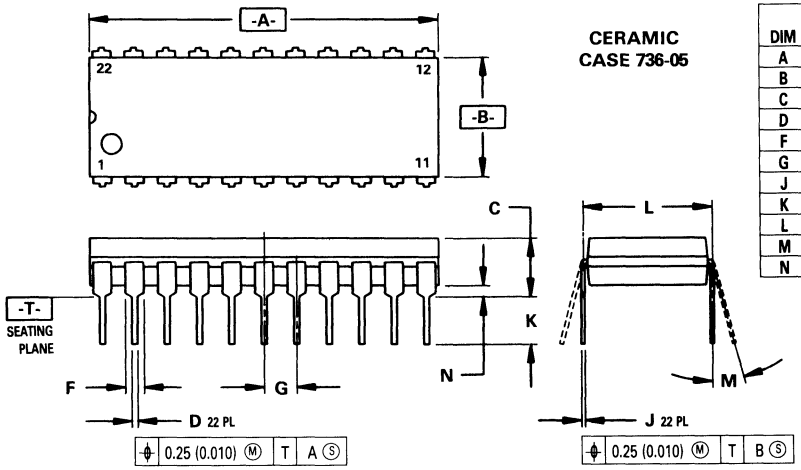
12



PLASTIC
CASE 736A-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	25.65	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.74	4.57	0.155	0.180
D	0.38	0.55	0.015	0.022
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.20	0.38	0.008	0.015
K	2.79	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. DIMENSION A IS A DATUM. T IS BOTH A DATUM AND A SEATING PLANE.
2. POSITIONAL TOLERANCE FOR D DIMENSION; 22 PL:
   ⌖ 0.25 (0.010) Ⓜ -T- A Ⓜ
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSIONING AND TOLERANCING PER Y14.5 M, 1982.
5. CONTROLLING DIMENSION: INCH.

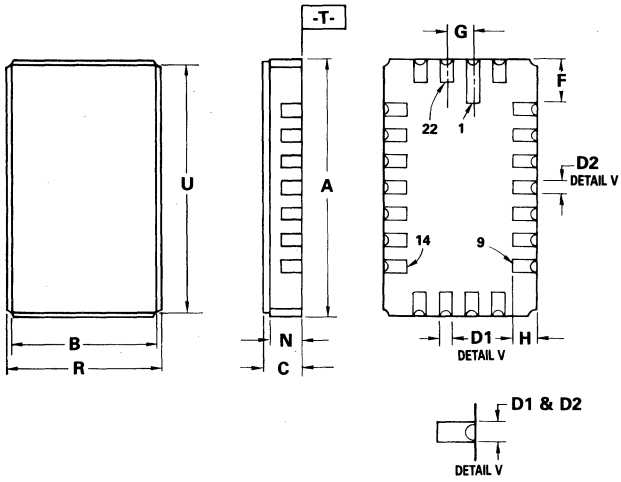


CERAMIC
CASE 736-05

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	26.93	27.81	1.060	1.095
B	9.15	9.90	0.360	0.390
C	3.81	5.46	0.150	0.215
D	0.39	0.53	0.015	0.021
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.39	0.008	0.015
K	3.18	4.31	0.125	0.170
L	10.16 BSC		0.400 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F FOR FULL LEADS. HALF LEADS OPTIONAL AT LEAD POSITIONS 1, 11, 12, AND 22.
5. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

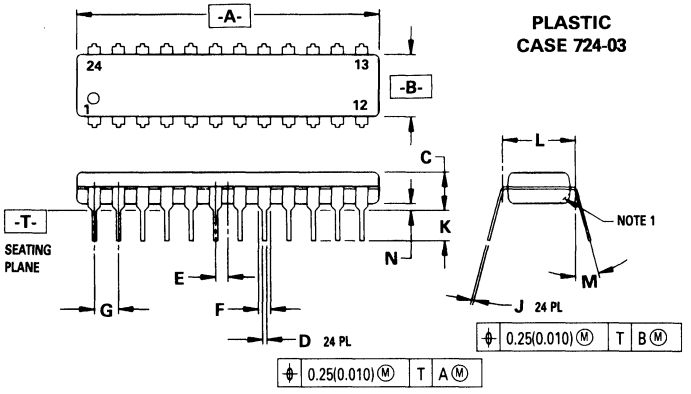
CERAMIC CHIP CARRIER
CASE 800-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.27	12.62	0.483	0.497
B	6.68	7.03	0.263	0.277
C	1.63	1.98	0.064	0.078
D	0.51	0.76	0.020	0.030
F	1.98	2.33	0.078	0.092
G	1.27 BSC		0.050 BSC	
H	0.97	1.32	0.038	0.052
N	1.27	1.62	0.050	0.064
R	7.19	7.54	0.283	0.297
U	11.76	12.11	0.463	0.477

NOTES:
1. DIMENSIONS A AND R ARE DATUMS AND T IS A GAUGE PLANE.
2. POSITIONAL TOLERANCE FOR TERMINALS D_2, 14 PLACES:
   ⌖ | 0.25 (0.010) Ⓜ | T | R Ⓢ | U Ⓢ
   TERMINALS D_1, 8 PLACES:
   ⌖ | 0.25 (0.010) Ⓜ | T | U Ⓢ | R Ⓢ
3. DIMENSIONING AND TOLERANCING PER Y14.5M, 1982.
4. CONTROLLING DIM: INCH.

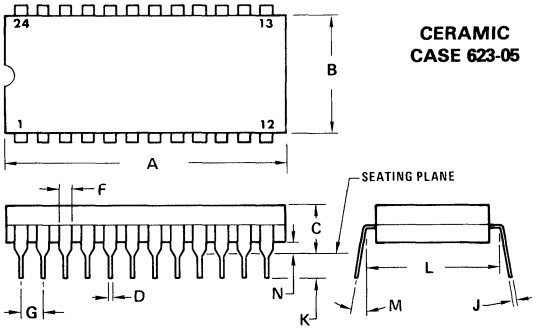
12



PLASTIC
CASE 724-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
J	0.18	0.30	0.007	0.012
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:
1. CHAMFERRED CONTOUR OPTIONAL.
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.

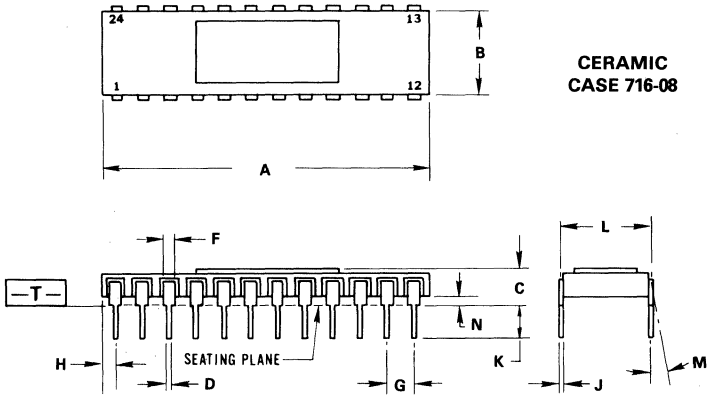


CERAMIC
CASE 623-05

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL).

12

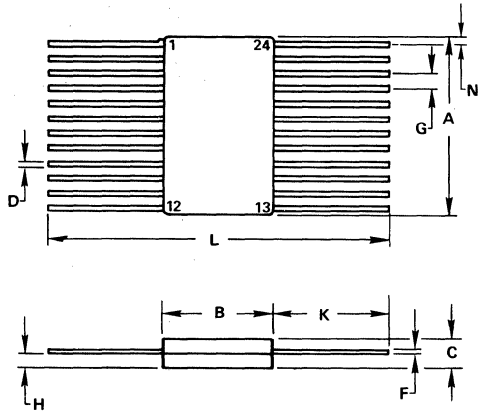


CERAMIC
CASE 716-08

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	27.63	30.98	1.088	1.220
B	7.16	7.74	0.282	0.305
C	2.66	4.31	0.105	0.170
D	0.38	0.53	0.015	0.021
F	1.14	1.39	0.045	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.77	0.030	0.070
J	0.20	0.30	0.008	0.012
K	3.17	5.08	0.125	0.200
L	7.62 BSC		0.300 BSC	
M	–	10^0	–	10^0
N	1.01	1.52	0.040	0.060

NOTES:
1. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ 0.25 (0.010) Ⓜ | T | A Ⓜ | B Ⓜ
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.
4. CONTROLLING DIMENSION: INCH.

CERAMIC
CASE 652-02

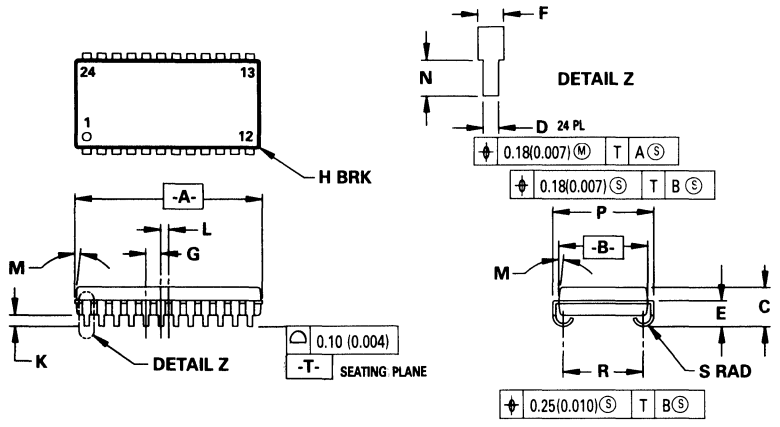


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.99	15.49	0.590	0.610
B	9.27	9.91	0.365	0.390
C	1.27	2.03	0.050	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.69	1.02	0.027	0.040
K	6.35	9.40	0.250	0.370
L	21.97	–	0.865	–
N	0.25	0.63	0.010	0.025

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

12

PLASTIC SOJ
CASE 810A-01

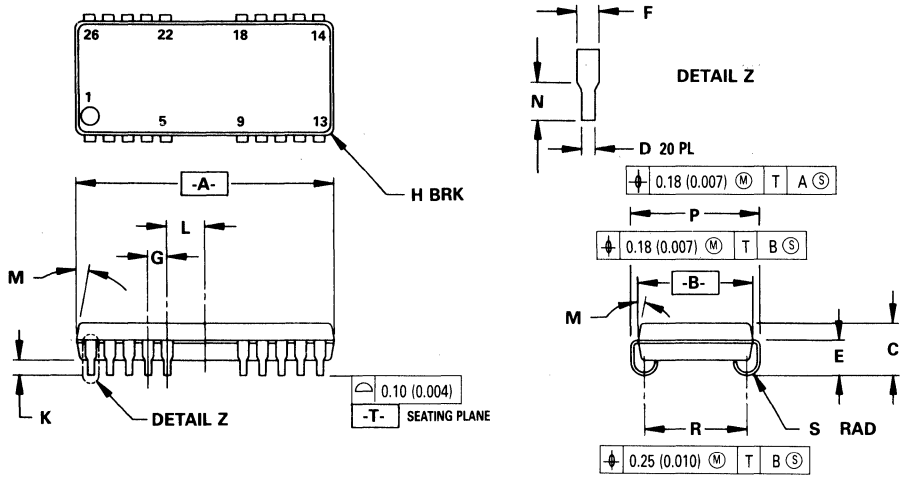


	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.75	16.00	0.620	0.630
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	5°	0°	5°
N	0.89	1.14	0.035	0.045
P	8.51	8.76	0.335	0.345
R	6.61	7.11	0.260	0.280
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM "R" TO BE DETERMINED AT DATUM -T-.

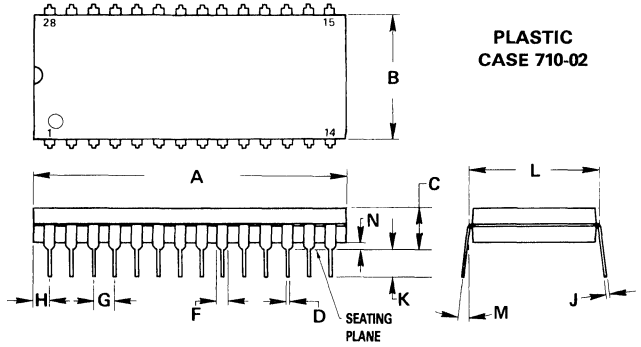
12

PLASTIC SOJ
CASE 822-02



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	17.02	17.27	0.670	0.680
B	7.50	7.74	0.295	0.305
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	2.54 BSC		0.100 BSC	
M	0°	5°	0°	5°
N	0.89	1.14	0.035	0.045
P	8.39	8.63	0.330	0.340
R	6.61	6.98	0.260	0.275
S	0.77	1.01	0.030	0.040

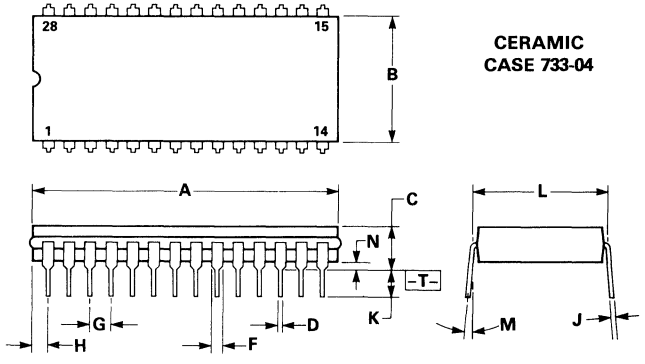
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIM R TO BE DETERMINED AT DATUM -T-.
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 6, 7, 8, 19, 20, & 21 ARE NOT USED.



PLASTIC
CASE 710-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



CERAMIC
CASE 733-04

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.84	1.435	1.490
B	12.70	15.36	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.55	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS: ϕ 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING & TOLERANCING PER Y14.5, 1982.
7. CONTROLLING DIM: INCH.

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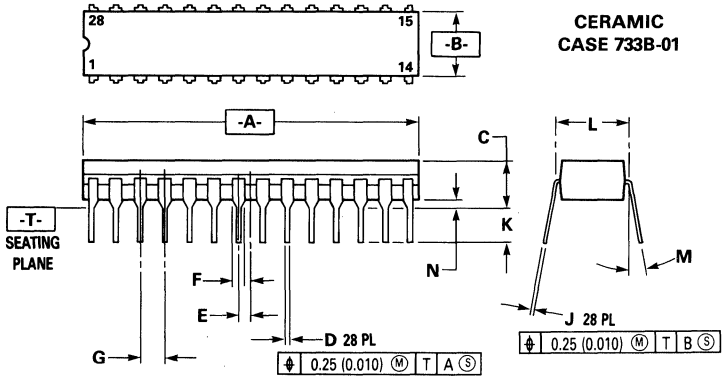
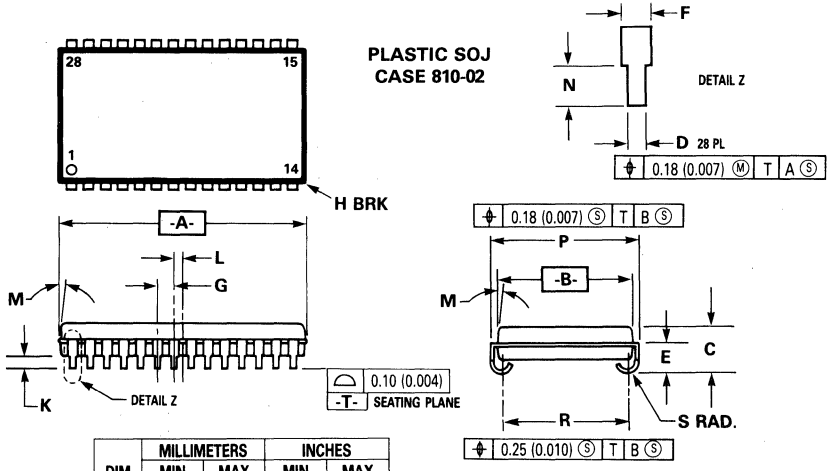


CERAMIC
CASE 733B-01

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	34.17	35.30	1.345	1.390
B	6.10	7.49	0.240	0.295
C	4.07	5.84	0.160	0.230
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM A AND B INCLUDES MENISCUS.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
4. CONTROLLING DIMENSION: INCH.



PLASTIC SOJ
CASE 810-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	18.29	18.54	0.720	0.730
B	10.04	10.28	0.395	0.405
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	5°	0°	5°
N	0.89	1.14	0.035	0.045
P	11.05	11.30	0.435	0.445
R	9.15	9.65	0.360	0.380
S	0.77	1.01	0.030	0.040

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM "R" TO BE DETERMINED AT DATUM -T-.

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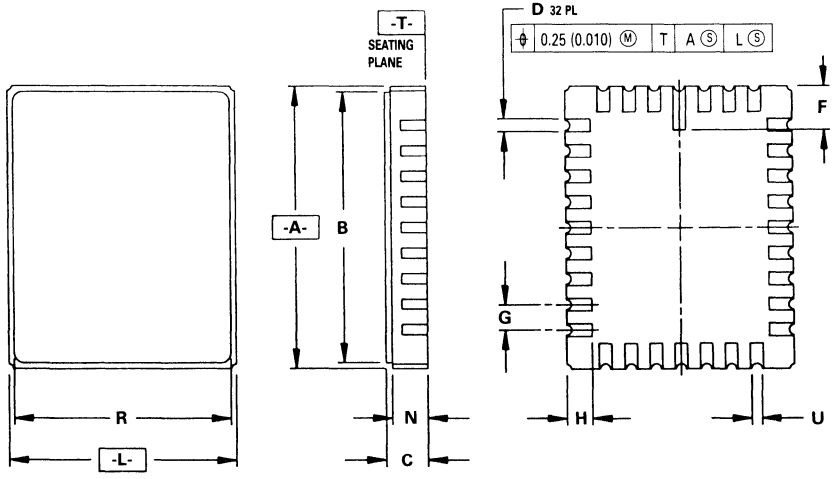
CERAMIC
CASE 766A-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	13.85	14.22	0.545	0.560
B	13.34	13.58	0.525	0.535
C	1.91	2.26	0.075	0.089
D	0.56	0.71	0.022	0.028
F	1.91	2.41	0.075	0.095
G	1.27 BSC		0.050 BSC	
H	1.07	1.47	0.042	0.058
L	11.31	11.63	0.445	0.458
N	1.63	1.93	0.064	0.076
R	10.80	11.04	0.425	0.435
U	—	0.50	—	0.020

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

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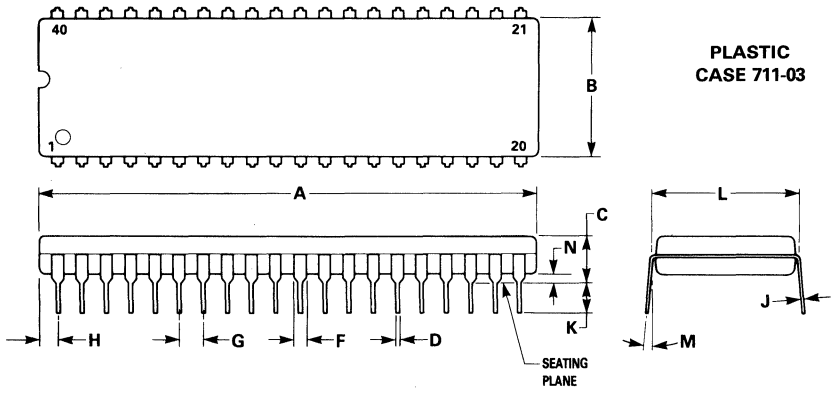
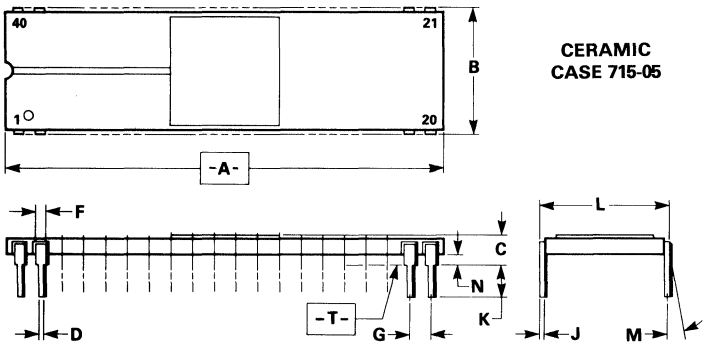


PLASTIC
CASE 711-03

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.



CERAMIC
CASE 715-05

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.63	15.49	0.576	0.610
C	2.79	4.32	0.110	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.57	0.100	0.180
L	14.99	15.65	0.590	0.616
M	—	10°	—	10°
N	1.02	1.52	0.040	0.060

NOTES:
1. DIMENSION -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS: ⌖ 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

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