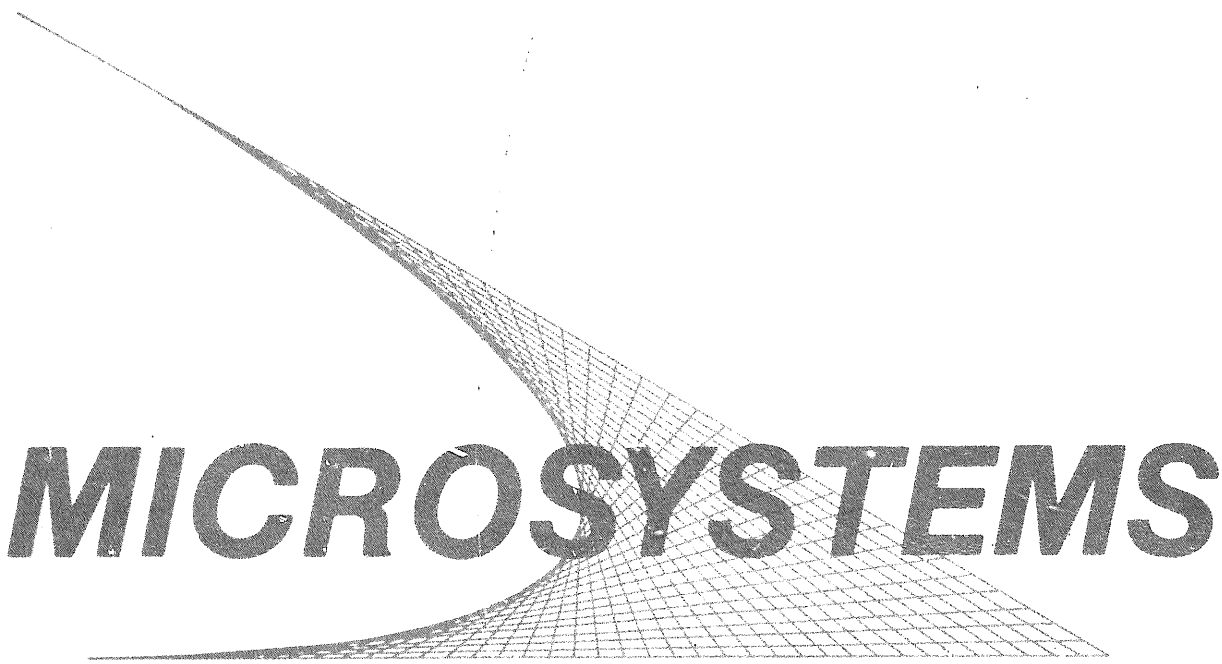
MOTOROLA

M68KVM12/D1

M68KVM12
1024K / 4096K Byte Dynamic RAM
User's Manual



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M68KVM12/D1

AUGUST 1984

M68KVM12

1024K/4096K BYTE DYNAMIC RAM

USER'S MANUAL

First Edition

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Microsystems Warranty and Repair for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

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PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

TABLE OF CONTENTS

TABLE OF CONTENTS (cont'd)

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1
GENERAL DESCRIPTION

CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual provides general information, hardware preparation and installation instructions, functional description, and support information for the M68KVM12 1024K/4096K Byte Dynamic RAM memory module. The module is shown in Figure 1-1. This memory module will be referred to as the VM12 throughout the remainder of this manual.

1.2 FEATURES

The features of the VM12 include:

- 1 megabyte, or 4 megabytes of dyanmic RAM
- Compatible with VERSAbus
- Control status register functions
- Byte parity error detection
- Battery backup capability

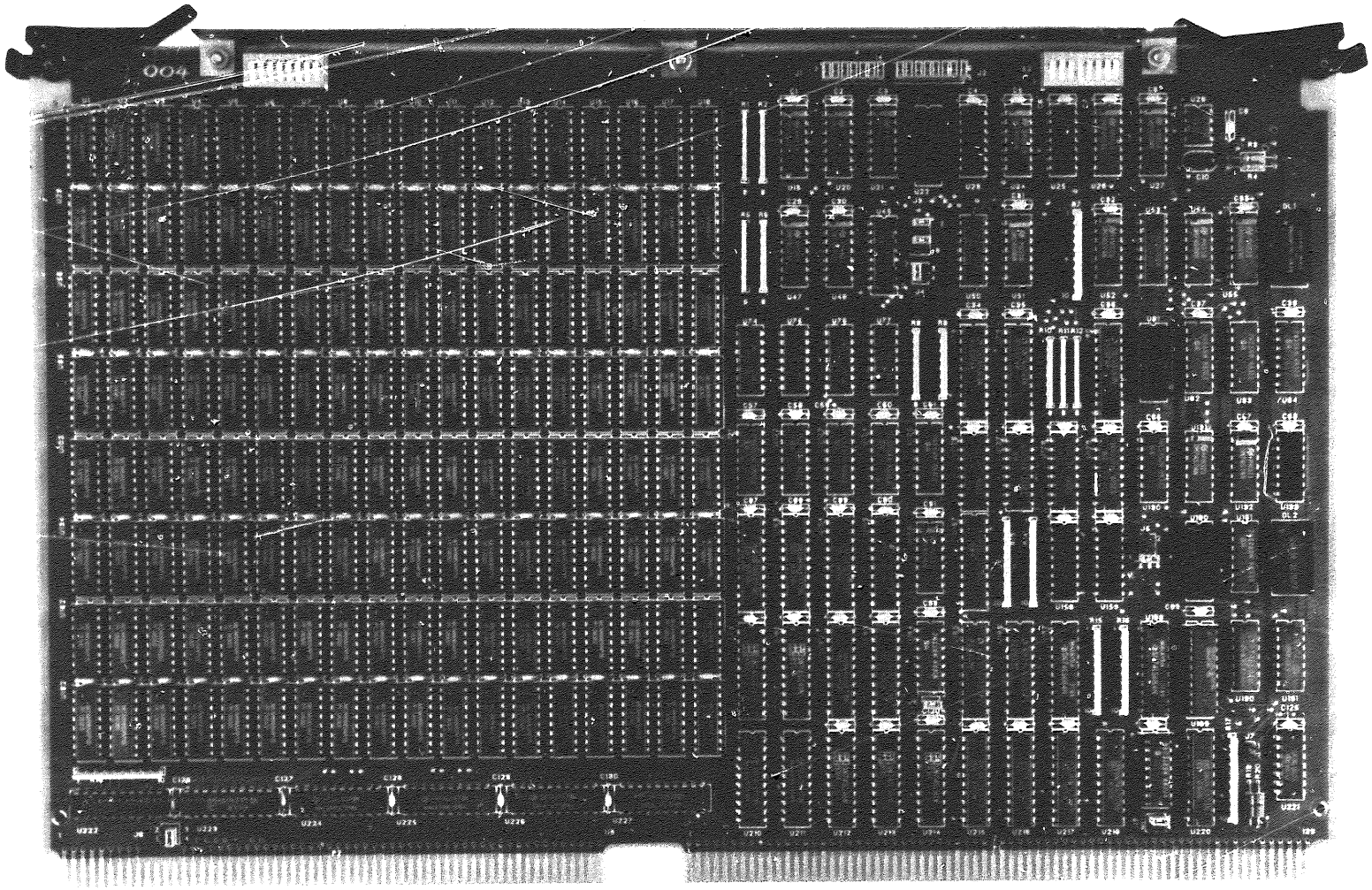

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FIGURE 1-1. VM12 Memory Module

SPECIFI-
CATIONS

1.3 SPECIFICATIONS

VM12 specifications are listed in Table 1-1.

TABLE 1-1. VM12 Specifications

CHARACTERISTICS	SPECIFICATIONS
Memory device type	HMOS dynamic RAM 64K x 1 (model B01) HMOS dynamic RAM, 256K x 1 (model B02)
Storage capacity	1 Mbyte (model B01) 4 Mbyte (model B02)
Word size	Byte (8 bits + 1 parity) Word (16 bits + 2 parity) Long word (32 bits + 4 parity)
Power requirements	
Normal operation	+5V @ 5A
Standby voltage	+5V @ 2A
Read access time	350 ns (maximum)
Write access time	180 ns (maximum)
Memory cycle time	420 ns (maximum)
Refresh cycle time	15 us (maximum)
Temperature	
Operating	0° to 70°C
Storage	-20° to 85°C
Relative Humidity	5% to 95% (non-condensing)
Physical Characteristics	
Height	9.25 in. (23.50 cm)
Width	14.50 in. (36.83 cm)
Thickness	0.66 in. (1.68 cm)

1.4 GENERAL DESCRIPTION

The VM12 provides mass semiconductor storage and is designed for use in high-speed memory applications. The module utilizes high-density 64K x 1 dynamic RAM devices on model B01, or 256K x 1 devices on model B02. Parity generation and detection circuitry, along with a Control/Status Register (CSR), allow error detection and memory diagnostics.

The memory array and refresh circuitry can be powered optionally by +5 Vdc or +5 Vdc standby supplies. When the latter option is employed, the VM12 is capable of retaining data indefinitely while consuming minimal current (2A, typically) from the +5 Vdc standby supply.

Because the VM12 is VERSAbus-compatible, it can be used in many products. Such products include Motorola's EXORmacs (development system for the MC68000 family of products), VMC 68/2, and similar VERSAmodule based systems.

1.5 RELATED DOCUMENTATION

The VERSAbus Specification Manual, M68KVBS, is applicable to the VM12.

CHAPTER 2 HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

CHAPTER 2

HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides unpacking instructions, hardware preparation procedures, and installation instructions for the VM12.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request carrier's agent be present during unpacking and inspection of the equipment.

Unpack module from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment.

2.3 HARDWARE PREPARATION

This section describes hardware preparation of the VM12 module prior to system installation. Observance of this description will ensure the user that his VM12 components are properly configured for system operation.

The VM12 has been factory tested for system operation and is shipped with factory-installed header jumpers. There are nine headers which are used to select the various functions and options of the module. Before the module is installed, the user should verify the jumper configuration of each header and alter, as required, for the user's particular system operation.

Two DIP-type switches (S1 and S2) on the edge of the module are provided for starting address selection. Refer to paragraph 2.3.9 for additional information regarding the use of these switches.

Figure 2-1 illustrates the location of the VM12 connectors, headers, and switches. Table 2-1 lists each header designation, the function of each header, and the factory-installed configuration. Figure 2-2 illustrates the pin arrangement of each header and shows the jumper configuration as-shipped from the factory for each one. A more detailed description of the headers is provided in the following paragraphs.

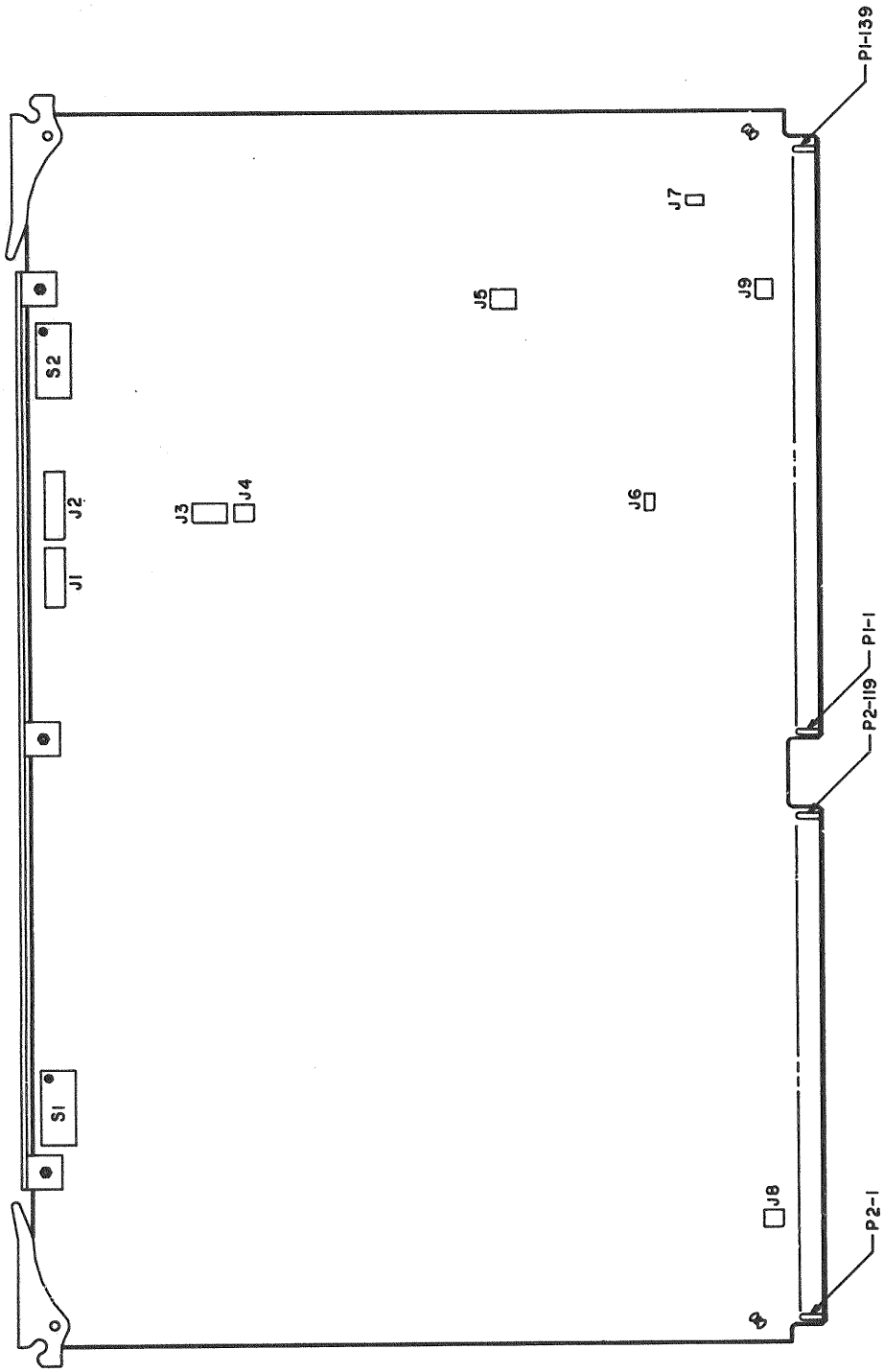
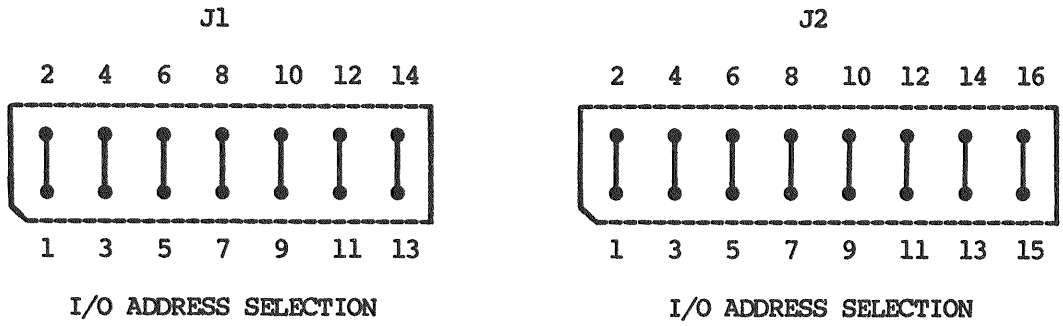
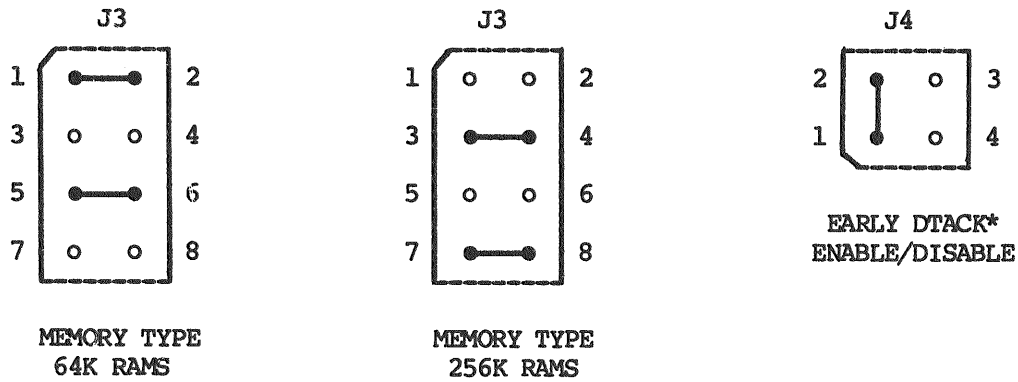


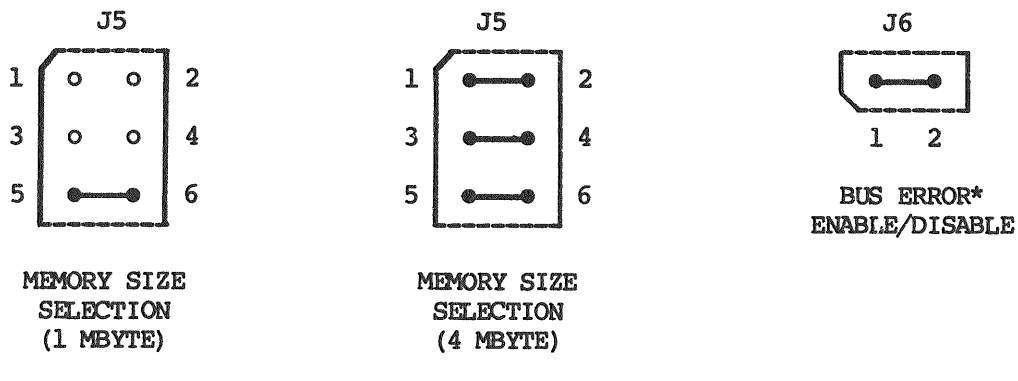
FIGURE 2-1. VM12 Connector and Header Location Diagram

TABLE 2-1. VM12 Headers

HEADER	FUNCTION	FACTORY-INSTALLED CONFIGURATION
J1	I/O address selection	(1-2), (3-4), (5-6), (7-8), (9-10), (11-12), (13-14)
J2	I/O address selection	(1-2), (3-4), (5-6), (7-8), (9-10), (11-12), (13-14), (15-16)
J3	Memory type selection	(1-2), (5-6) --- B01 model (3-4), (7,8) --- B02 model
J4	Early DTACK* enable/disable	(1-2)
J5	Memory size selection	(5-6) --- B01 model (1-2), (3-4), (5-6) --- B02 model
J6	BUS ERROR* enable/disable	(1-2)
J7	Parity error report enable/disable	Open (not jumpered)
J8	Extended address selection enable/disable	(3-4)
J9	Address modifier response selection	(1-2)







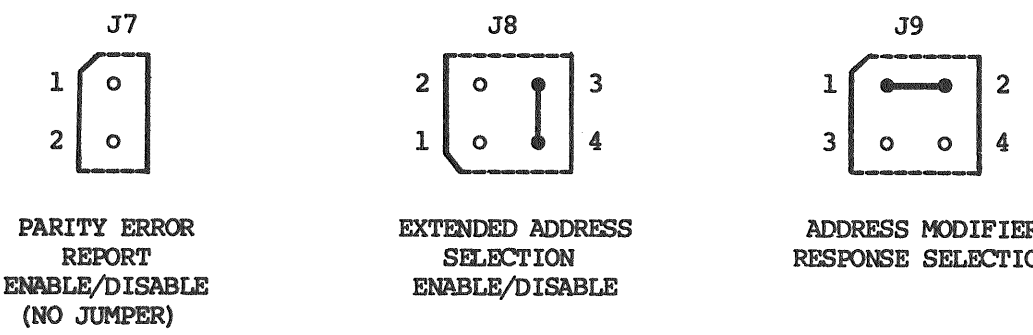


FIGURE 2-2. Header Pin Arrangements and As-Shipped Jumper Configurations

I/O ADDRESS SELECTION HEADER

2.3.1 I/O Address Selection Headers (J1, J2)

Headers J1 and J2 are used to select the I/O address which defines the location of the control/status word. The control/status word occupies only one word within the I/O space, FF0000-FFFFFF.

The VM12 is shipped with all jumpers installed on headers J1 and J2. This jumper configuration locates the control/status word at FFFFFE-FFFFFF. When J1 and J2 are left open (all jumpers removed), the control/status word is located at FF0000-FF0001. The J1 and J2 jumpers can be configured to set any location between these limits.

Table 2-2 gives jumper installation configurations for the various address lines.

TABLE 2-2. Headers J1 and J2 Configurations

ADDRESS LINE	HEADER J1 PINS JUMPERED	HEADER J2 PINS JUMPERED
1	1-2	--
2	3-4	--
3	5-6	--
4	7-8	--
5	9-10	--
6	11-12	--
7	13-14	--
8	--	1-2
9	--	3-4
10	--	5-6
11	--	7-8
12	--	9-10
13	--	11-12
14	--	13-14
15	--	15-16

MEMORY SIZE SELECTION HEADERS

2.3.2 Memory Type Selection Header (J3)

Header J3 is used to select the memory type on the VM12. When the VM12 is configured for a total memory capacity of one megabyte, 64K RAM's are used, and jumpers should be installed on pins 1 to 2 and 5 to 6 of header J3. When the VM12 is configured for a total memory capacity of four megabytes, 256K RAM's are used, and jumpers should be installed on pins 3 to 4 and 7 to 8 of header J3.

2.3.3 Early DTACK* Enable/Disable Header (J4)

Header J4 is provided to allow the DTACK* signal to be activated 270 ns (maximum) after DATA STROBE*, thus making possible faster memory operation.

NOTE

This feature option should be used with discretion, because parity errors would not be detected when using the early DTACK*.

The VM12 is shipped with pins 1-2 of J4 jumpered. This configuration is for normal VM12 operation (normal DTACK* time). If the early DTACK* operation is desired, remove the jumper from pins 1-2 and install it on pins 3-4 of J4.

2.3.4 Memory Size Selection Header (J5)

Header J5 is used to select the total memory size (capacity) of the VM12. The one megabyte VM12, which uses 64K RAM's, is selected by jumpering pins 5 to 6 on header J5. The four megabyte VM12, which uses 256K RAM's, is selected by jumpering pins 1 to 2, 3 to 4, and 5 to 6 on header J5.

2.3.5 Bus Error Enable/Disable Header (J6)

Header J6 provides the user with the option to enable or disable the issuing of the BUS ERROR* signal. For additional information, refer to the descriptions of the control/status register and parity error detection. To enable issuing the BUS ERROR*, install jumper on J6, pins 1-2. To disable issuing of the BUS ERROR*, remove the jumper on J6, pins 1-2. The VM12 is shipped with pins 1-2 jumpered.

2.3.6 Parity Error Report Enable/Disable (J7)

If a parity error is detected on a read cycle, and provided the parity error bit is set, bit 15 in the CSR will be set (refer to Chapter 4).

Header J7 determines which of the two modes of operation for parity error report will be used. If J7 is open (no jumper on pins 1-2), writing a logic 1 to bit 0 of the CSR enables parity error report. If a jumper is installed on pins 1-2 of J7, bit 0 of the CSR is a logic 0 at power-up, and parity error report is enabled. Writing a logic 1 to bit 0 of the CSR now disables parity error report.

NOTE

The user can "don't care" bit 0 of the CSR by removing the jumper on header J6. This disables the issuing of the BUS ERROR* signal (refer to header J6 description, paragraph 2.3.5).

2.3.7 Extended Address Selection Enable/Disable Header (J8)

Header J8, in conjunction with switch 1 (S1), is used to enable or disable the extended addresses of the VM12. For additional information, refer to the descriptions of switch 1 (S1) and switch 2 (S2) under paragraph 2.3.9 and in Figure 2-3. To enable the extended addresses, install a jumper on J8, pins 1-2. To disable the extended addresses, install a jumper on J8, pins 3-4. The VM12 is shipped with pins 3-4 jumpered.

2.3.8 Address Modifier Response Selection Header (J9)

The VM12 is designed so that the user can replace a PROM (82S129) at U219 to modify module response to address modifier (AM) codes. The memory portion of the module responds to AM codes for supervisor/user standard (24-bit address) mode or for supervisor/user extended (32-bit address) mode. Selection of these options is accomplished by the configuration of J9 jumpers. Table 2-3 lists the available options. The VM12 is shipped with J9 pins 1-2 jumpered.

TABLE 2-3. J9 Jumper Options

J9 PINS JUMPERED:	MODE OF OPERATION SELECTED	RESPONDS TO AM CODES:
1-2	Supervisor/user standard	01, 02, 05, 06, FF
3-4	Supervisor/user extended	F1, F2, F5, F6, FF

The I/O portion (control/status register) responds to AM code 15.

BACKUP BATTERY OPERATIONS

2.3.9 Address Select Options (S1, S2)

Two DIP-type switches (S1 and S2) are provided on the VM12 module (see Figure 2-1) for selecting the starting address. The VM12 memory section is configurable to begin on any 64K boundary within a selected 16-megabyte page. (Sixty-four such pages exist when the extended addressing mode is used.) The jumper option provided by header J8 allows the upper eight address select switches (contained on S1) to be disabled if the VM12 is used in systems limited to 24 address lines (refer to paragraph 2.3.7).

The ending address of the memory section is the sum of the starting address and the board population. An exception to this occurs if the memory is located within one megabyte of an upper page boundary. In this case the ending address is the page boundary.

Figure 2-3 shows the starting address boundaries selectable by S1 and S2.

2.3.10 Backup Battery Operation

The memory array and refresh circuitry on the VM12 can be powered optionally by +5 Vdc or by the +5 Vdc standby line. When powered by the +5 Vdc standby line, the VM12 is capable of retaining data indefinitely while using minimal current (2A, typically) from the +5 Vdc standby supply.

Battery backup (+5 Vdc standby) operation can be employed by removing (unsoldering or cutting) the zero-ohm jumper resistors, R19 and R20. This will allow the +5 Vdc standby power to be applied to the VM12 (refer to the schematic diagram, Figure 5-2).

	S1								S2							
Switch Position	8	7	6	5	4	3	2	1	8	7	6	5	4	3	2	1
Address Line	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Starting Address	2G	1G	512M	256M	128M	64M	32M	16M	8M	4M	2M	1M	512K	256K	128K	64K

FIGURE 2-3. Starting Address Selection Options

INSTAL-
LATION
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TIONS

2.4 INSTALLATION INSTRUCTIONS

When the VM12 module has been prepared for installation (configured by user) as desired, it is ready for system use and can now be installed.

The following general procedure is recommended for installing the VM12 module in a Motorola EXORmacs or VERSAmodule chassis, or other compatible system chassis:

WARNING

AC POWER MUST BE REMOVED TO AVOID ELECTRICAL SHOCK TO MAINTENANCE PERSONNEL.

a. Remove power from chassis in which VM12 is being installed.

CAUTION

INSERTING MODULES WHILE POWER IS APPLIED COULD RESULT IN DAMAGE TO MODULE COMPONENTS.

b. Obtain access to the card rack area of the chassis (refer to the appropriate chassis user's manual for location and directions).

CAUTION

AVOID TOUCHING AREAS OF MOS CIRCUITRY; STATIC DISCHARGE CAN DAMAGE INTEGRATED CIRCUITS.

c. Using a firm grip on the module, carefully align the pins on the module with the mating connectors of the chassis backplane. Use a firm, steady pushing motion to install the module snuggly in the connectors.

The VM12 can be installed in any available slot which is not reserved for a processor or other intelligent board.

CHAPTER 3
OPERATING INSTRUC-TIONS

PROGRAM-MING DESCRIPTION

CHAPTER 3

OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides a description of controls on the VM12 and other information pertaining to the operation of the module.

3.2 OPERATING CONTROLS

The only operating controls on the VM12 are two switches, S1 and S2. These switches are used to select the starting address of the VM12. For a description of these switches and their functions, refer to paragraph 2.3.9.

3.3 OPERATING PROCEDURES

The VM12 operating procedure consists only of configuring the module (according to information in Chapter 2) and inserting it into the VERSAbus connectors.

3.4 PROGRAMMING DESCRIPTION

This section provdes the necessary information to program the address modifier decoder U219 to respond to alternate modes of operation by means of address modifier codes.

The programmable address modifier decoder is a bipolar PROM designated U219. The device generic part number is an N82S129 made by Signetics. The structure is a 256 x 4, meaning there are eight address lines and four outputs (one output is not used and is not connected.) Following are the signals and the corresponding pins to which they are applied.

SIGNAL	U219 PIN NAME	U219 PIN NUMBER
AM0	A7	15
AM1	A6	1
AM2	A5	2
AM3	A4	3
AM4	A3	4
AM5	A2	7
AM6	A1	6
AM7	A0	5

This device may be programmed by the user such that the VM12 may respond to a number of different address modifier codes (AM0-AM7). The VM12 is shipped from the factory with the PROM programmed to respond to address modifier hexadecimal codes 01, 02, 05, 06, and FF for standard addressing, and F1, F2, F5, F6, and FF for extended addressing.

A partial truth table of the valid codes that cause the outputs of U219 to become active is given in Table 3-1.

TABLE 3-1. Address Modifier Codes

AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0		CODE
1	1	1	1	1	1	1	0	01	Supervisor/ User Standard
1	1	1	1	1	1	0	1	02	U219, Pin 11
1	1	1	1	1	0	1	0	05	
1	1	1	1	1	0	0	1	06	
0	0	0	0	0	0	0	0	FF	
0	0	0	0	1	1	1	0	F1	Supervisor/ User Extended
0	0	0	0	1	1	0	1	F2	U219, Pin 12
0	0	0	0	1	0	1	0	F5	
0	0	0	0	1	0	0	1	F6	
0	0	0	0	0	0	0	0	FF	
1	1	1	0	1	0	1	0	15	I/O U219, Pin 10

NOTE: AM0-AM7 correspond to address lines A7-A0, respectively, on the N82S129 PROM.

The user may desire to program U219 to respond in alternative modes. U219 can be programmed to respond to any combination of address modifier codes not already defined by the VMEbus specification and also for any combination of blocks to be enabled.

CHAPTER 4
FUNCTIONAL DESCRIPTION

READ CYCLE SEQUENCE

CHAPTER 4

FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter provides overall operational and block diagram level descriptions for the VM12 memory module.

4.2 VM12 MEMORY MODULE OPERATION

The VM12 operates in the following modes: byte write or read (8 bits + 1 parity), word write or read (16 bits + 2 parity), or longword write or read (32 bits + 4 parity). Data strobes DS0*, DS1*, A01*, and LWORD* determine whether the VM12 operates in a byte, word, or longword mode. The WRITE* signal controls write and read operations.

The following paragraphs briefly describe the write and read cycle sequences. See Figures 4-1 and 4-2 for VM12 module timing diagrams.

4.2.1 Write Cycle Sequence

The VM12 performs the write cycle sequence to store data into memory. A write cycle is initiated when the write data signal (WRITE*) and the data strobe signals (DS0* and DS1*) are activated on the VERSAbus. Next, the VM12 performs the address comparison and address modifier decode to generate the board select signal (BDSEL) and initiate the memory cycle. The DS0*, DS1*, A01*, and LWORD* signals determine the access mode (byte, word, or longword) for the write cycle, and data is then transferred into the specified location in memory. When the data is received, the VM12 activates the data acknowledge (DTACK*) signal which indicates to the requester that the write cycle has been completed.

4.2.2 Read Cycle Sequence

The VM12 performs the read cycle sequence to retrieve data from memory. A read cycle is initiated when the write data signal (WRITE*) is inactive. At that time, the data strobe signals (DS0* and DS1*) are activated on the VERSAbus. Next, the VM12 performs the address comparison and address modifier decode to generate the board select signal (BDSEL), and initiate the memory cycle. When this occurs, the address currently on the bus is latched into the VM12 module. The VM12 decoding circuitry decodes this address, and data at the specified addressed memory location is transferred to the VERSAbus. The VM12 then activates the DTACK* signal to indicate to the requester that the read cycle has been completed.

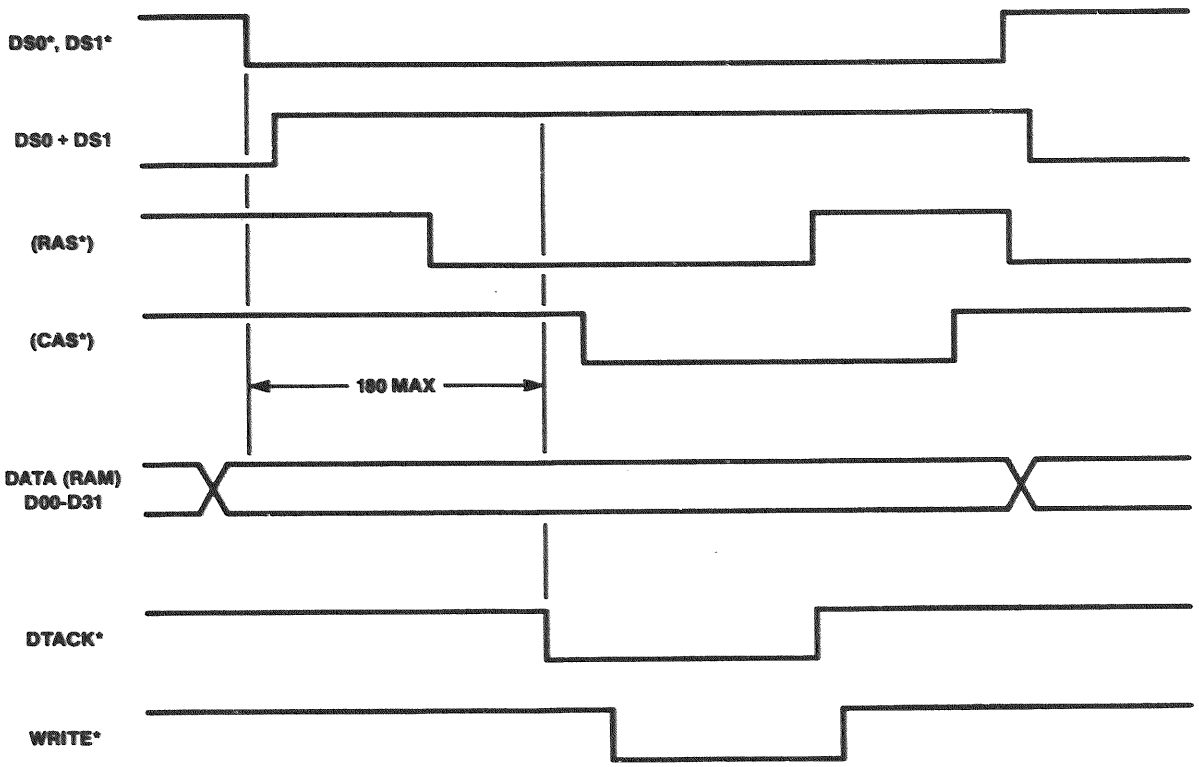


FIGURE 4-1. Memory Write Cycle Timing Diagram

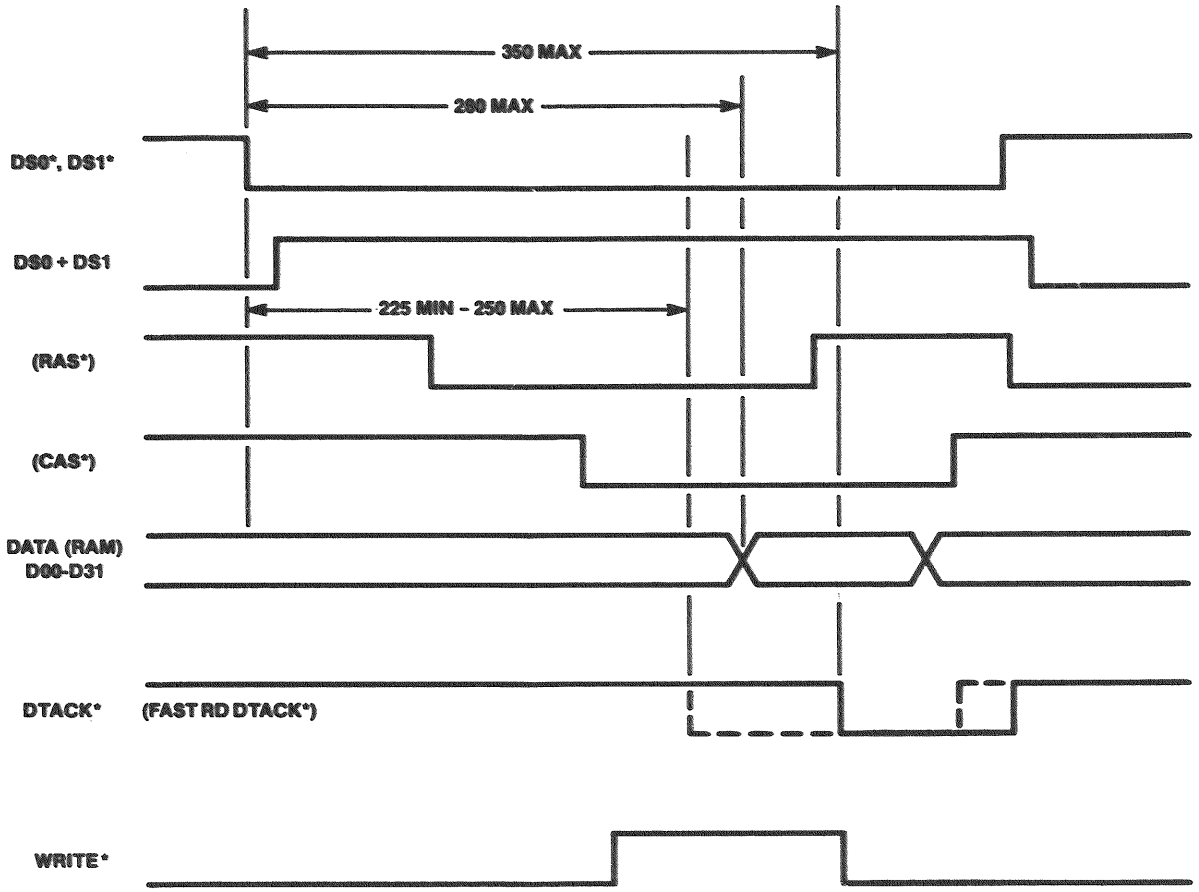


FIGURE 4-2. Memory Read Cycle Timing Diagram

4.2.3 Battery Backup Operation

The VM12 is designed with the option to operate on battery backup power in case of a power outage. Refer to Chapter 2 for information concerning battery operation.

NOTE

Battery operation merely allows data to be retained in memory during a power outage. Normal read and write operations cannot be performed when operating on battery power.

4.3 MODULE DESCRIPTION

The VM12 memory module performs data storage (write mode), data retrieval (read mode), and data retention (memory refreshing) operations. Figure 4-3 illustrates a simple functional block diagram of the VM12. The diagram illustrates the overall basic functional circuits of the memory module. For a more detailed diagram of the VM12, refer to the schematic diagram in Chapter 5.

The VM12 memory module consists of the following functional circuits:

a. I/O buffers and latches
b. Address decoding
c. Memory array
d. Data parity generation/checking
e. Control/status register (CSR)
f. Refresh and control

4.3.1 I/O Buffers and Latches

All signals entering and leaving the VM12 module pass through buffers and latches. The address buffers and latches are U215-U218 and U223. The data buffers and latches are U152-U155, U180-U183, U210-U213, U220, and U224-U227. These buffers and latches are activated/deactivated by internal and external signals.

Incoming data (write mode) is transferred to the module buffers/latches when the internal signals buffered data strobe (BDS0* and BDS1*), external signals WRITE*, LWORD* (if longword is selected), and A01* are active (low level). Data is transferred out of the module buffers (read mode) when these signals are active (low level); however, the WRITE* signal must be inactive (high level).

In the read mode of operation, the low order data bits (D00-D07) are gated out of the buffers when DS0* and BDS0* are active and WRITE* is inactive. The high-order data bits (D08-D15) are gated out when DS1* and BDS1* are active and WRITE* is inactive. When both DS0* and DS1* along with both BDS0* and BDS1* are active and WRITE* is inactive, all 16 data bits will be gated out of the module buffers. If a longword (32 bits) is being read out, the LWORD* signal must also be active.

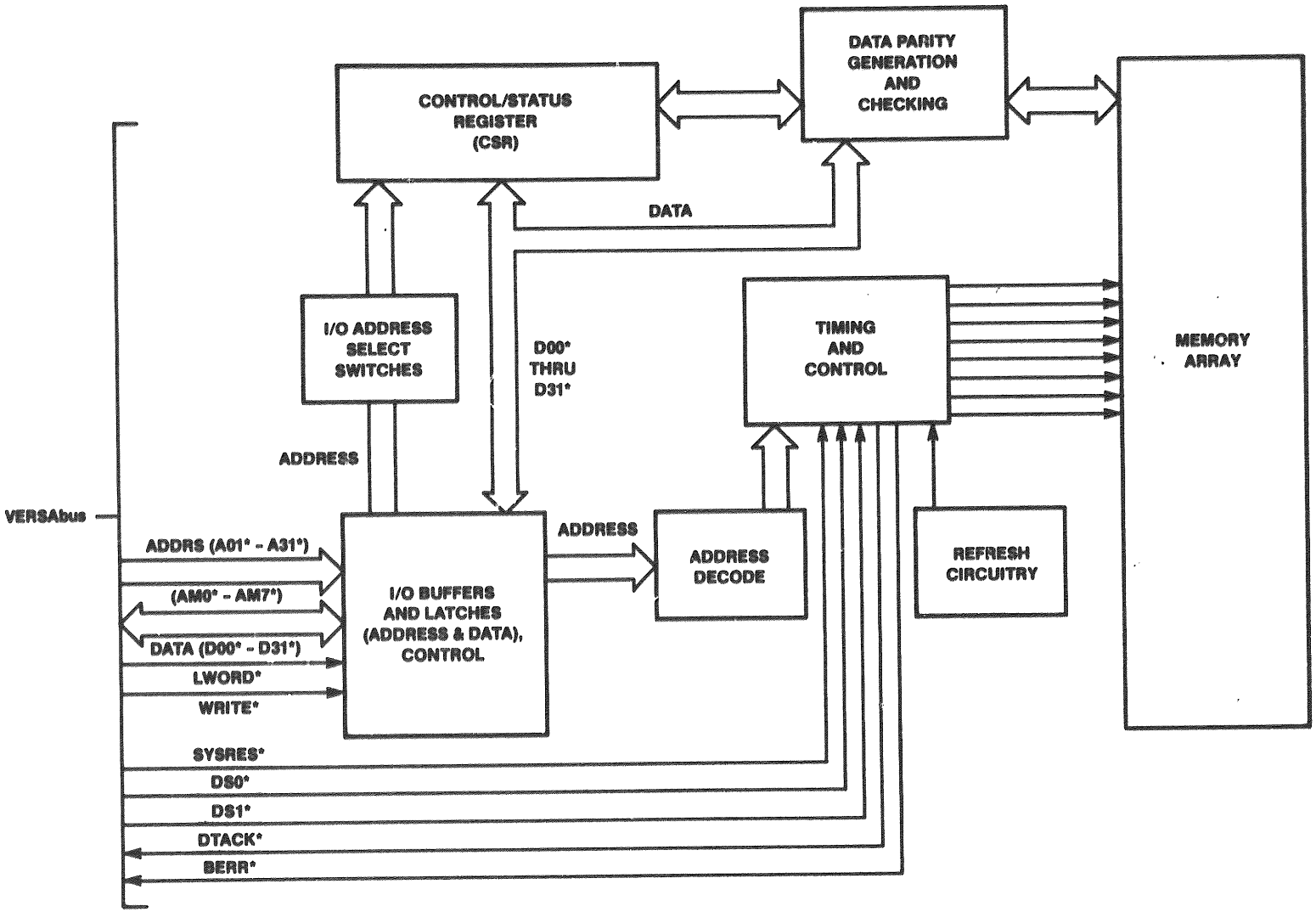


FIGURE 4-3. VM12 Functional Block Diagram

4.3.2 Address Decoding

The address lines (A02*-A31*), as well as address modifier lines (AM0*-AM7*), are connected to the module through address latches U215-U218 and U223. Address lines LA00*-LA31* are then routed through address comparators U222 and U187. Coming out of these address comparators, address lines LA16*-LA31* go to switch 1 (S1) and switch 2 (S2). The switch settings of these two switches determine the starting address of the VM12 module (refer to heading 2.3.9 and Figure 2-3 for more information regarding use of these switches). Address lines LA16*-LA23* are also routed through address comparators U158, U159, and U188. These address comparators and the jumper configuration on header J5 determine the size of the memory.

When the starting address is determined, the address decoder activates the main timing circuitry, buffered data strobe (BDS0*/BDS1*), BDSEL, and the row address select.

4.3.3 Memory Array

Memory storage on the VM12 module consists of a 144-device array that is physically arranged on the module in eight rows of 18 RAM's.

The VM12 uses 64K x 1 devices for a total capacity of 1 Megabyte (1,024,000 bytes), or 256K x 1 devices for a total capacity of 4 megabytes (4,096,000 bytes). The devices are physically arranged on the VM12 module such that in each row the first eight RAM's comprise the low-order data bits of the byte, the next eight RAM's comprise the upper-order data bits of the byte, and the last two devices in the row are the lower byte and upper byte parity bits, respectively.

Referring to Figure 4-4 and to the schematic diagrams, notice that ROW ADDRESS STROBE 0 (RAS0*) gates data bits D00*-D15* and associated parity bits to the first row of RAM devices. RAS1* gates data bits D00*-D15* and associated parity bits to the second row of RAM devices. RAS2* gates these bits to the third row, and RAS3* gates these bits to the fourth row. Then, this whole scheme is repeated on the next four rows of devices for data bits D16*-D31*.

4.3.4 Data Parity Generation And Checking

The VM12 generates a parity bit for each byte stored during a write cycle. Even parity is generated by the parity generator (U74-U77) and stored in the memory devices for the associated byte. Devices U74 and U75 generate the parity bits for the lower-order bytes, and U76 and U77 generate the parity bits for the higher-order bytes.

Parity checking is accomplished during read cycles. When a read cycle is performed data bytes are gated to the parity checker (U121-U124). Devices U121 and U122 check parity for the low-order bytes, and U123 and U124 check parity for the high-order bytes.

Parity checking is performed by routing the memory data bits plus previously stored parity bits to the inputs of the parity checker. Since even parity was generated during the write operation (when the data was stored into memory), even parity is checked when the data is read out of memory.

		BITS D00*-D07*	BITS D08*-D15*	PARITY	
ROW 1	RAS0* ----->	U1-U8	U9-U16	U17	U18
ROW 2	RAS1* ----->	U29-U36	U37-U44	U45	U46
ROW 3	RAS2* ----->	U56-U63	U64-U71	U72	U73
ROW 4	RAS3* ----->	U85-U92	U93-U100	U101	U102

		BITS D16*-D23*	BITS D24*-D31*	PARITY	
ROW 5	RAS0* ----->	U103-U110	U111-U118	U119	U120
ROW 6	RAS1* ----->	U134-U141	U142-U149	U150	U151
ROW 7	RAS2* ----->	U162-U169	U170-U177	U178	U179
ROW 8	RAS3* ----->	U192-U199	U200-U207	U208	U209

FIGURE 4-4. VM12 Memory Array Configuration

CONTROL/ STATUS REGISTER

If the output of the parity checker goes high, it indicates that parity is correct. If the output goes low, a parity error is indicated, and a BUS ERROR (BERR*) is activated on the bus if a jumper is installed on header J6. Also, when an error is detected, bit 15 in the control/status register (CSR) is set, provided ENABLE PARITY ERROR REPORT (EPER*) bit is set. Refer to heading 4.3.5 for a description of the CSR.

There are two modes of operation for Parity Error Report determined by header J7. If J7 is open (jumper is not installed) and a logical one is written to bit 0 of the CSR, Parity Error Report is enabled. If a jumper is installed on J7, bit 0 of the CSR is a logical zero at power up, and Parity Error Report is enabled. If a logical one is now written to bit 0 of CSR, Parity Error Report is disabled.

The user can "don't care" bit 0 of CSR by removing the J6 jumper. This prevents the VM12 from issuing a BERR* signal.

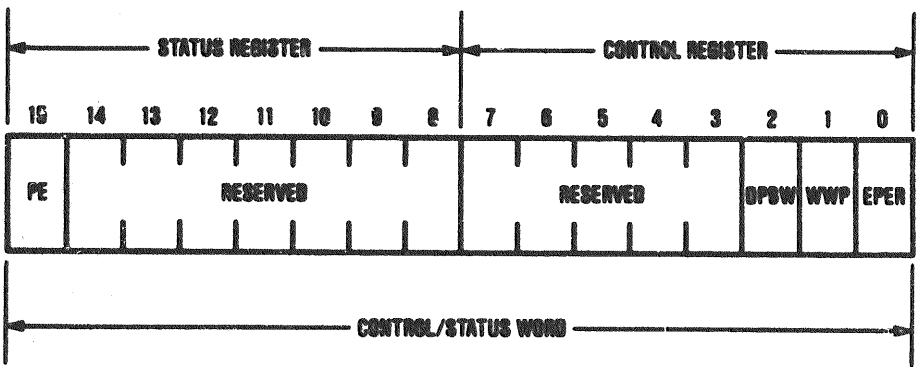
4

4.3.5 Control/Status Register

The VM12 Control/Status Register (CSR) is accessible as a 16-bit word, which provides parity error indication and software enabling/disabling control of parity generation, incorrect parity generation (for testing purposes), and the parity error checking circuitry. Hardware for the CSR includes:

- CSR address decoder (U185 and U186)
- I/O address selection headers (J1 and J2)
- BERR* enable/disable header (J7)
- Parity error status bit device (U131A)
- CSR register device (U157)

The Control/Status Word (CSW) is a 16-bit word which is formatted into two basic segments: (1) control register, and (2) status register. These items are described in the following paragraphs. See Figure 4-5.



BIT ASSIGNMENTS:

0	ENABLE PARITY ERROR REPORT (EPER)
1	WRITE WRONG PARITY (WWP)
2	DISABLE PARITY BIT WRITE (DPBW)
3-7	RESERVED
8-14	RESERVED
15	PARITY ERROR (PE)

FIGURE 4-5. Control/Status Word Bit Assignment

4.3.5.1 Control Register. The control register occupies three bits of the lower byte of the CSW. All three bits operate in normal read and write modes. Bits three through seven are undefined. The bits are automatically cleared when the SYSRESET* signal is a low level. All control/status bits are also cleared on power-up. The user may "don't care" bit 0 by removing the jumper on header J6.

Two bits in the control register (bits 1 and 2) can be used to facilitate memory testing under software control. Bit 2 can be set to inhibit the writing of the even parity value into the parity bit during a memory write cycle. Bit 1 can be set to enable the writing of the wrong parity value into a parity bit.

4.3.5.2 Status Register. The status register occupies one bit of the upper byte of the CSW. The bit operates in normal read and write modes. Bits 8-14 are undefined. Bit 15 will always set when a parity error is detected on a read access. A Buss Error (BERR*) is activated only if bit 0 is also set, and a jumper is installed on header J6.

Bit 15 is automatically cleared when the SYSRESET* signal is a low level. It may also be cleared by writing a logic zero to that location. All control/status bits are also cleared on power-up.

4.3.6 Refresh and Control

Memory refreshing is performed continuously to ensure that information is not lost. Each refresh cycle is initiated by the refresh oscillator (U28). If a memory cycle is in progress, the next refresh cycle will begin when the memory cycle is complete. The VM12 memory devices are refreshed every 15 microseconds.

Control circuits provide arbitration between the refresh memory and the I/O cycles. Refer to sheets 8 and 9 of the schematic diagrams for memory module timing and control circuits.

CHAPTER 5
SUPPORT INFORMATION

CONNECTOR SIGNAL DESCRIPTIONS

CHAPTER 5

SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides pin assignments and signal descriptions for the signals on the VERSAbus connectors, parts list and parts location diagram, and a schematic diagram for the VM12.

5.2 CONNECTOR SIGNAL DESCRIPTIONS

The VM12 has two interface connectors (P1 and P2) which are used for interfacing to the VERSAbus. These connectors are standard VERSAbus gold-plated edge connectors located at the bottom of the module (see Figure 5-1). Connector P1 has 140 pins, 70 on the component side and 70 on the solder side. Connector P2 has 120 pins, 60 on each side.

Table 5-1 lists the pins, signal mnemonic and names, and signal descriptions for connector P1. Table 5-2 gives the same categories of information for P2.

TABLE 5-1. Connector P1 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1,2	+5V	+5 Vdc POWER - Used by module logic circuits.
3,4,23,24,27, 28,31,32,61, 62,67,68,71, 72,119,120, 123,124,135-140	GND	GROUND - Used by logic circuits.
21,22,30,33, 64-66,69,70, 73,75-77,79, 80,82,87-93, 107-118,121, 122,125-128	N.C.	No connection.
5-20	D00*-D15*	DATA bus (bits 0-15) - 16 three-state bidirectional data lines that provide a data path between the VM12 module and all other modules connected to the VERSAbus.
25	DS0*	DATA STROBE 0 - Input signal which indicates a data transfer will occur on data bus lines D00*-D07* during byte and word transfers.
26	DS1*	DATA STROBE 1 - Input signal which indicates a data transfer will occur on data bus lines D08*-D15* during byte and word transfers.

TABLE 5-1. Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
29	DTACK*	DATA TRANSFER ACKNOWLEDGE - Output signal which indicates valid data is available to the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
34	WRITE*	WRITE - Input signal that determines whether the data transfer cycle in progress is a read (high) or write (low).
35	LWORD*	LONGWORD - Input signal that determines whether a cycle is a byte/word transfer (high) or longword transfer (low).
36-58	A01*-A23*	ADDRESS bus (bits 1-23) - 23 input signals used to selectively address the VM12. NOTE For extended addressing assignments, refer to Table 5-2 descriptions (Connector P2).
59	AM4*	ADDRESS MODIFIER (bit 4) - Input signal that provides additional address bus data such as size, cycle type, and DTB master identification.
60	AM7*	ADDRESS MODIFIER (bit 7) - Same as AM4* on pin 59.
63	AM3*	ADDRESS MODIFIER (bit 3) - Same as AM4* on pin 59.
74	SYSRES*	SYSTEM RESET - Input signal which, when low, will reset the system.
78	ACFAIL*	AC FAILURE - Input signal which indicates that ac input to system power supply is no longer being provided or that the required input voltage levels are not being met.
81	BERR*	BUS ERROR* - Output signal which indicates that an unrecoverable error has occurred and the bus cycle must be aborted.
83-86	AM0*,AM1* AM2*,AM6*	ADDRESS MODIFIER - (bits 0, 1, 2, and 6) - Same as AM4* on pin 59.
94	AM5*	ADDRESS MODIFIER (bit 5) - Same as AM4* on pin 59.

TABLE 5-1. Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
95-106 (2)		
129-132	+5V	+5 Vdc power - Used by module logic circuits.
133,134	+5VB	+5 Vdc battery (standby) power - Alternate +5 Vdc power source which can be used optionally by module logic circuits.

NOTE: 1. Odd pins are on component side of module. Even pins are on solder side of module.

(2) The following pin pairs on the VM12 module are shorted together so that these daisy-chained bus signals loop "in" and "out" of this board. This eliminates the need to jumper these signals on the chassis backplane. (See sheet 2 of schematic diagram, Figure 5-2.)

95,96 (ACKIN*, ACKOUT*)
97,98 (BG0IN*, BG0OUT*)
99,100 (BG1IN*, BG1OUT*)
101,102 (BG2IN*, BG2OUT*)
103,104 (BG3IN*, BG3OUT*)
105,106 (BG4IN*, BG4OUT*)

5

TABLE 5-2. Connector P2 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1-6,97,98, 101,102	GND	GROUND - Used by module logic circuits.
7-10	+5V	+5 Vdc power - Used by module logic circuits.
11-88,99,100, 103,104	N.C.	No connection.
89-96	A24*-A31*	ADDRESS bus (bits 24-31) - 8 input signals used, optionally, to select an extended address on the VM12. (Refer to Table 5-1 for other address lines used on the VM12.)
105-120 (2)	D16*-D31*	DATA bus (bits 16-31) - 16 three-state bidirectional data lines that provide a data path between the VM12 module and all other modules connected to the VERSAbus.

NOTES: 1. Odd pins are on component side of module. Even pins are on solder side of module.

(2) Pins 105-120 (D16*-D31*) are not bussed in VERSAmodule chassis backplane, in VMC 68/2 systems, or in slots A14 and A15 of EXORmacs chassis.

PARTS LIST

5.3 PARTS LIST

Table 5-3 lists the components of the VM12. This list reflects the latest issue of VM12 hardware at the time of printing. A parts location drawing is provided in Figure 5-1.

TABLE 5-3. VM12 Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
---	84-W8280B01	Printed wire board assembly, M68KVM12
C1-C9, C11-C130	21NW9632A03	Capacitor, ceramic, axial, .1 uf @ 50 Vdc, ±20%
C10	21NW9629A37	Capacitor, mica, 330 pF @ 100 Vdc, ±5%
DL1	01NW9804C24	Digital delay module, 200 ns
DL2	01NW9804C49	Digital delay module, 50 ns
J1	28NW9802C36	Header, double row, 14-pin
J2	28NW9802B34	Header, double row, 16-pin
J3	28NW9802C43	Header, double row, 8-pin
J4,J8, J9	28NW9802C29	Header, double row, 4-pin
J5	28NW9802B21	Header, double row, 6-pin
J6,J7	28NW9802D01	Header, double row, 2-pin
R1,R2,R5, R6,R8-R12	51NW9626A56	Resistor network, SIP, 8-pin, four 22-ohm
R3	06SW-124A73	Resistor, film, 10K ohm, 5%, 1/4W
R4	06SW-124A81	Resistor, film, 22K ohm, 5%, 1/4W
R7,R13-R18	51NW9626A41	Resistor network, SIP, 10-pin, nine 4.7K-ohm
R19-R20	29NW9805B46	Jumper, axial, insulated
S1,S2	40NW9801A34	Switch, DIP, SPST, 8-position
U1-U18, U29-U46, U56-U73, U85-U120, U134-U151, U162-U179, U192-U209	51NW9615M09 51NW9615P38	I.C. MCM6665AP15 (VM12-B01) I.C. HM50256-15 (VM12-B02)
U19-U21, U26,U47, U48, U55	51NW9615C94	I.C. SN74S00N

TABLE 5-3. VM12 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U23	51NW9615D32	I.C. SN74S02N
U24	51NW9615F31	I.C. SN74S51N
U25,U83	51NW9615E27	I.C. SN74S10N
U27,U51,U54	51NW9615C56	I.C. SN74S08N
U28	51NW9615B65	I.C. MC1455P1
U49	51NW9615D91	I.C. SN74S139N
U50,U190, U191	51NW9615C21	I.C. SN74LS04N
U52,U131, U132,U156	51NW9615C95	I.C. SN74S74N
U53	51NW9615E91	I.C. SN74LS00N
U74-U77	51NW9615F12	I.C. 74LS280N
U78,U79,U80	51NW9615F79	I.C. SN74S240N
U81	---	Not used (spare)
U82,U125	51NW9615G43	I.C. SN74S64N
U84	51NW9615C96	I.C. SN74S04N
U121-U124	51NW9615E35	I.C. DM74S280N
U126-U129	51NW9615F84	I.C. SN74S153N
U130	51NW9615F38	I.C. SN74LS393N
U133	51NW9615D90	I.C. SN74S11N
U152-U155, U182,U183, U215-U218, U220,U223	51NW9615G56	I.C. SN74S373N
U157	51NW9615J13	I.C. AM25LS2519PC
U158,U159	51NW9615J36	I.C. SN74LS283N
U160	51NW9615C58	I.C. SN74S86N

DIAGRAMS

TABLE 5-3. VM12 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U180,U181, U212-U214	51NW9615F65	I.C. SN74S241N
U184	51NW9615F85	I.C. SN74S38N
U185,U186, U222	51NW9615H01	I.C. AM25LS2521PC
U187,U188	51NW9615J51	I.C. SN74LS684N
U189	(see NOTE)	I.C. Programmed
U210,U211, U224-U227	51NW9615E98	I.C. SN74LS373N
--	(see NOTE)	I.C. Programmed
U221	51NW9615C20	I.C. SN74LS02N
--	03SW993D306	Screw, phillips, M3 x 0.5 x 6
--	07-W4639B01	Plate, stiffener, M68KVM12
U219	09NW9811A04	Socket, IC, DIL, 16-pin
U189	09NW9811A53	Socket, IC, DIL, 20-pin
--	29NW9805B17	Jumper, shorting, insulated, 22 required - (used on the VM12 headers -- refer to Chapter 2 for placement.)
--	55NW9403A18	Extractor/inserter with roll pin
XU22	09NW9811A78	Socket, IC, DIL, 20-pin (used for manufacturing test only)

NOTE: When ordering the programmed I.C.'s, use number labeled on part.

5

5.4 DIAGRAMS

Figure 5-2 is a schematic diagram of the VM12.

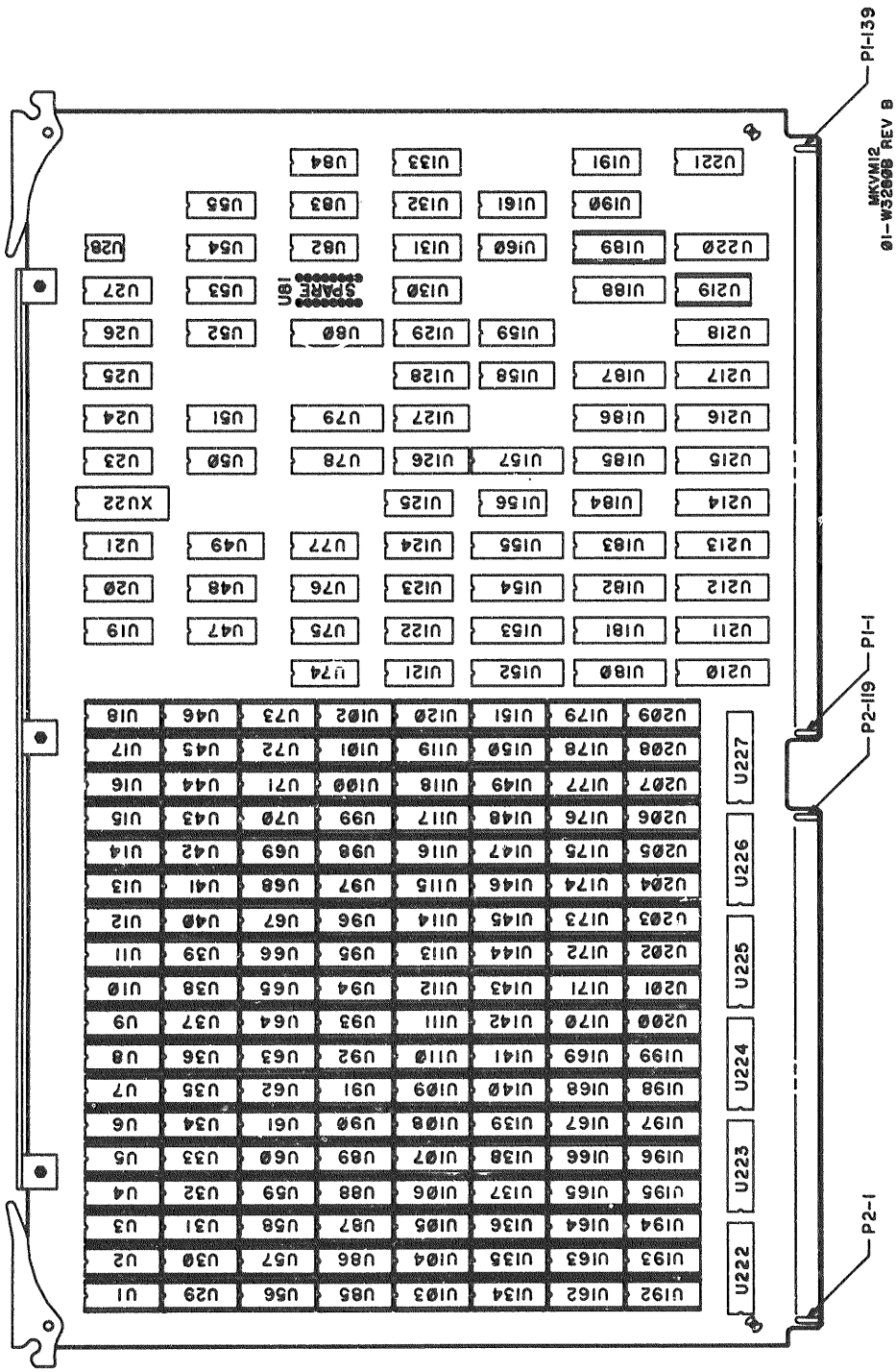


FIGURE 5-1. VM12 Parts Location Diagram (Sheet 1 of 2)

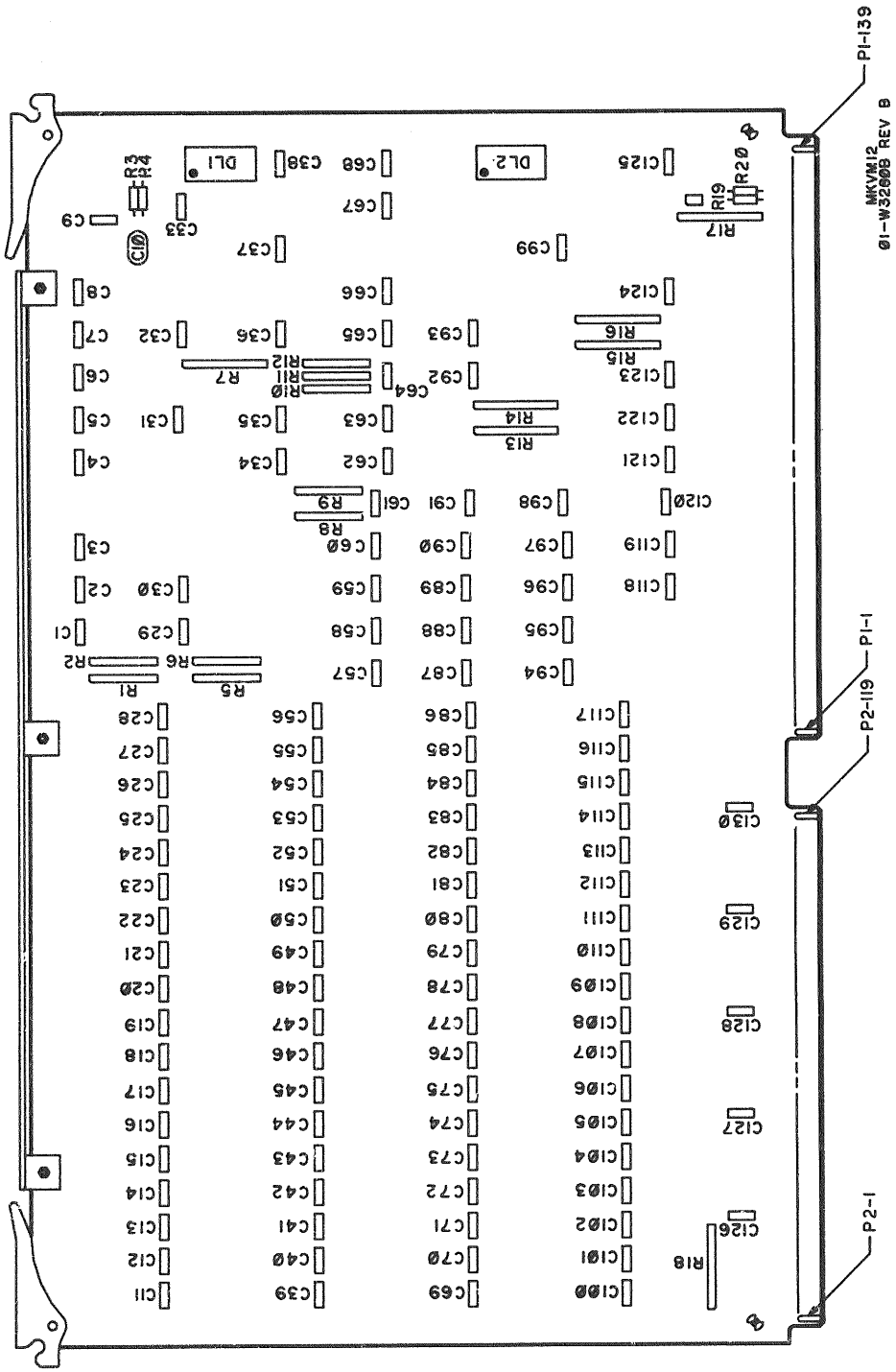


FIGURE 5-1. VM12 Parts Location Diagram (Sheet 2 of 2)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	RELEASE FOR PROTO SG 8-5-83 RTY	9/2/83	AL
	B	RELEASE FOR PILOT SJG 10-11-83 RTY	10/20/83	DB
	C	ECN H3905: SH 1 UPDATED REV. SH 2 DELETED U80G. SH 6 ADDED 10C3 TO SIG [EN IX] SH 10 ADDED U80G. RTY 12-7-83 ACD	10/7/83	DB

NOTES:

1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 81-W3280B01.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ±5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. ⚠ DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   # DENOTES - ACTIVE LOW SIGNAL.
   [] DENOTES - ON BOARD SIGNAL.
   +5VB DENOTES - BATTERY VOLTAGE.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
7. ⚠ PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING. FOR FULL PART TYPE, REFER TO TABLE 1.
8. CODE FOR SHEET TO SHEET REFERENCES IS AS FOLLOWS:
   SHEET — 6 A6 — ZONE

TABLE 1 ⚠

REF DES	TYPE ⚠	GND	+5V	+5VB	SH
DL1	2516MS	7		14	9
DL2	58MS	7		14	8
U1	MCM6256	16		8	13
U2	MCM6256	16		8	13
U3	MCM6256	16		8	13
U4	MCM6256	16		8	13
U5	MCM6256	16		8	13
U6	MCM6256	16		8	13
U7	MCM6456	16		8	13
U8	MCM6256	16		8	13
U9	MCM6256	16		8	14
U10	MCM6256	16		8	14
U11	MCM6256	16		8	14
U12	MCM6256	16		8	14
U13	MCM6256	16		8	14
U14	MCM6256	16		8	14
U15	MCM6256	16		8	14
U16	MCM6256	16		8	14
U17	MCM6256	16		8	21
U18	MCM6256	16		8	21
U19	74S86	7		14	9
U20	74S86	7		14	9
U21	74S86	7		14	9
XU22	TEST SOCKET				7
U23	74S82	7		14	6,9
U24	74S51	7		14	6,8
U25	74S10	7		14	10,12
U26	74S00	7		14	12
U27	74S86	7		14	2,7
U28	MC1455	1		8	8
U29	MCM6256	16		8	13
U30	MCM6256	16		8	13
U31	MCM6256	16		8	13
U32	MCM6256	16		8	13
U33	MCM6256	16		8	13
U34	MCM6256	16		8	13
U35	MCM6256	16		8	13
U36	MCM6256	16		8	13
U37	MCM6256	16		8	14
U38	MCM6256	16		8	14
U39	MCM6256	16		8	14
U40	MCM6256	16		8	14
U41	MCM6256	16		8	14
U42	MCM6256	16		8	14
U43	MCM6256	16		8	14
U44	MCM6256	16		8	14
U45	MCM6256	16		8	21
U46	MCM6256	16		8	21
U47	74S86	7		14	9
U48	74S00	7		14	8
U49	74S138	8		16	2,9
U50	74LS04	7		14	6,8,9,10
U51	74S08	7		14	8
U52	74S74	7		14	6
U53	74LS00	7		14	7,8,10
U54	74S00	7		14	2,8,10,12
U55	74S00	7		14	8,9
U56	MCM6256	16		8	15
U57	MCM6256	16		8	15
U58	MCM6256	16		8	15

TABLE 1 CON'T ⚠

REF DES	TYPE ⚠	GND	+5V	+5VB	SH
U59	MCM6256	16		8	15
U60	MCM6256	16		8	15
U61	MCM6256	16		8	15
U62	MCM6256	16		8	15
U63	MCM6256	16		8	15
U64	MCM6256	16		8	16
U65	MCM6256	16		8	16
U66	MCM6256	16		8	16
U67	MCM6256	16		8	16
U68	MCM6256	16		8	16
U69	MCM6256	16		8	16
U70	MCM6256	16		8	16
U71	MCM6256	16		8	16
U72	MCM6256	16		8	21
U73	MCM6256	16		8	21
U74	74LS288	7	14		11
U75	74LS288	7	14		11
U76	74LS288	7	14		11
U77	74LS288	7	14		11
U78	74S240	10		20	8
U79	74S240	10		20	8
U80	74S240	10		20	2,8,8,9,10
U81	SPARE				2
U82	74S04	7		14	8
U83	74S10	7		14	2,8
U84	74LS04	7		14	2,8,9,12
U85	MCM6256	16		8	15
U86	MCM6256	16		8	15
U87	MCM6256	16		8	15
U88	MCM6256	16		8	15
U89	MCM6256	16		8	15
U90	MCM6256	16		8	15
U91	MCM6256	16		8	15
U92	MCM6256	16		8	15
U93	MCM6256	16		8	16
U94	MCM6256	16		8	16
U95	MCM6256	16		8	16
U96	MCM6256	16		8	16
U97	MCM6256	16		8	16
U98	MCM6256	16		8	16
U99	MCM6256	16		8	16
U100	MCM6256	16		8	16
U101	MCM6256	16		8	21
U102	MCM6256	16		8	21
U103	MCM6256	16		8	17
U104	MCM6256	16		8	17
U105	MCM6256	16		8	17
U106	MCM6256	16		8	17
U107	MCM6256	16		8	17
U108	MCM6256	16		8	17
U109	MCM6256	16		8	17
U110	MCM6256	16		8	17
U111	MCM6256	16		8	18
U112	MCM6256	16		8	18
U113	MCM6256	16		8	18
U114	MCM6256	16		8	18
U115	MCM6256	16		8	18
U116	MCM6256	16		8	18
U117	MCM6256	16		8	18
U118	MCM6256	16		8	18

XU22	XU1-XU21
U227	U22
S2	
R26	
P2	
J8	
DL2	
C136	
HIGHEST NUMBER USED	NOT USED
REFERENCE DESIGNATIONS	

A					
21					
A	A	A	A	A	
16	17	18	19	20	
A	B	A	A	A	
11	12	13	14	15	
C	B	B	B	C	
6	7	8	9	10	

DWG NO. 63DW3280B

REV STATUS OF SHEETS					
C	C	B	A	B	SH 1
1	2	3	4	5	

63DW3280B REV C SH 1 OF 21
S1850-1
07-22-83

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS IN INCHES
METRIC DIMENSIONS IN (MILLIMETERS)
REMOVE ALL BURRS AND SHARP EDGES.
SURFACE TEXTURE IN MICROINCHES
TOLERANCE:
2 PLACE DEC. ±
3 PLACE DEC. ±
HOLES ± ANGLES ±

DRAWN BY	S.GIORLANDO III	DATE 8-8-83
CHECKED BY	R.T.YOUNG	DATE 8-9-83
PROJECT LEADER	R.STANPHILL N.NAUFEL FOR P.S./FAX	DATE 8-12-83
DESIGN MANAGER	N.L.WAGNER	DATE 9/1/83
MFG ENGINEER	D.BOND	DATE 9/12/83
DESIGN ENGINEER	N.NAUFEL. N. NAUFEL / FAX	DATE 8-12-83

DESCRIPTION | PART NO.

MOTOROLA INC.
MOS Integrated Circuits Group
MICROSYSTEMS
2900 South Diablo Way, Tempe, Arizona 85282 U.S.A.

TITLE: SCHEMATIC DIAGRAM - M68KVMI2

D | FSCM NO. | DRAWING NO. 63DW3280B

SCALE: NONE | SHEET 1 OF 21

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 1 of 21)

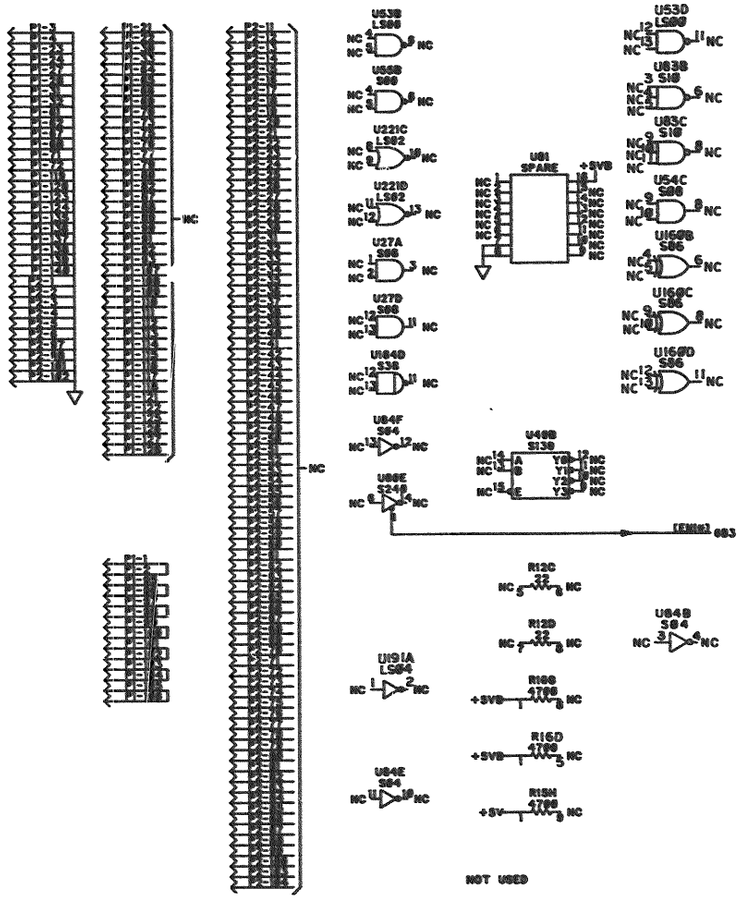
ZONE	REV	REVISIONS DESCRIPTION	DATE	APPROVED
	C	SEE SHEET 1		

TABLE 1 CON'T ⚠

REF DES	TYPE ⚠	GND	+5V	+5VB	SH
U119	MCM6256	16		8	21
U120	MCM6256	16		8	21
U121	74S288	7	14		11
U122	74S288	7	14		11
U123	74S288	7	14		11
U124	74S288	7	14		11
U125	74S84	7	14		11
U126	74S183	8		16	8
U127	74S183	8		16	8
U128	74S183	8		16	8
U129	74S183	8		16	8
U130	74LS383	7		14	8
U131	74S74	7		14	8,16
U132	74S74	7		14	16
U133	74S11	7		14	16
U134	MCM6256	16		8	17
U135	MCM6256	16		8	17
U136	MCM6256	16		8	17
U137	MCM6256	16		8	17
U138	MCM6256	16		8	17
U139	MCM6256	16		8	17
U140	MCM6256	16		8	17
U141	MCM6256	16		8	17
U142	MCM6256	16		8	18
U143	MCM6256	16		8	18
U144	MCM6256	16		8	18
U145	MCM6256	16		8	18
U146	MCM6256	16		8	18
U147	MCM6256	16		8	18
U148	MCM6256	16		8	18
U149	MCM6256	16		8	18
U150	MCM6256	16		8	21
U151	MCM6256	16		8	21
U152	74S373	10	20		12
U153	74S373	10	20		12
U154	74S373	10	20		12
U155	74S373	10	20		12
U156	74S74	7	14		10
U157	25LS2518	10	20		10
U158	74LS283	8	16		7
U159	74LS283	8	16		7
U160	74S86	7	14		2,12
U161	74S288	7		14	7,10
U162	MCM6256	16		8	18
U163	MCM6256	16		8	18
U164	MCM6256	16		8	18
U165	MCM6256	16		8	18
U166	MCM6256	16		8	18
U167	MCM6256	16		8	18
U168	MCM6256	16		8	18
U169	MCM6256	16		8	18
U170	MCM6256	16		8	26
U171	MCM6256	16		8	26
U172	MCM6256	16		8	26
U173	MCM6256	16		8	26
U174	MCM6256	16		8	26
U175	MCM6256	16		8	26
U176	MCM6256	16		8	26
U177	MCM6256	16		8	26
U178	MCM6256	16		8	21

TABLE 1 CON'T ⚠

REF DES	TYPE ⚠	GND	+5V	+5VB	SH
U179	MCM6256	16		8	21
U180	74S241	10	20		12
U181	74S241	10	20		12
U182	74S373	10	20		12
U183	74S373	10	20		12
U184	74S38	7	14		2,10
U185	74LS688	10	20		10
U186	74LS688	10	20		10
U187	74LS682	10	20		7
U188	74LS684	10	20		7
U189	TBP18S22	10		20	12
U190	74LS04	7		14	5,10,12
U191	74LS04	7		14	2,5,8,7,8,12
U192	MCM6256	16		8	19
U193	MCM6256	16		8	19
U194	MCM6256	16		8	19
U195	MCM6256	16		8	19
U196	MCM6256	16		8	19
U197	MCM6256	16		8	19
U198	MCM6256	16		8	19
U199	MCM6256	16		8	19
U200	MCM6256	16		8	28
U201	MCM6256	16		8	28
U202	MCM6256	16		8	28
U203	MCM6256	16		8	28
U204	MCM6256	16		8	28
U205	MCM6256	16		8	28
U206	MCM6256	16		8	28
U207	MCM6256	16		8	28
U208	MCM6256	16		8	21
U209	MCM6256	16		8	21
U210	74LS373	10	20		12
U211	74LS373	10	20		12
U212	74S241	10	20		12
U213	74S241	10	20		12
U214	74S241	10	20		8
U215	74S373	10	20		5
U216	74S373	10	20		5
U217	74S373	10	20		5
U218	74S373	10	20		5
U219	82S129	8	16		5
U220	74S373	10	20		12
U221	74LS62	7		14	2,8
U222	74LS688	10	20		7
U223	74S373	10	20		5
U224	74LS373	10	20		12
U225	74LS373	10	20		12
U226	74LS373	10	20		12
U227	74LS373	10	20		12



63DW3280B REV C SH 2 OF 21

S1050-2
07-22-83

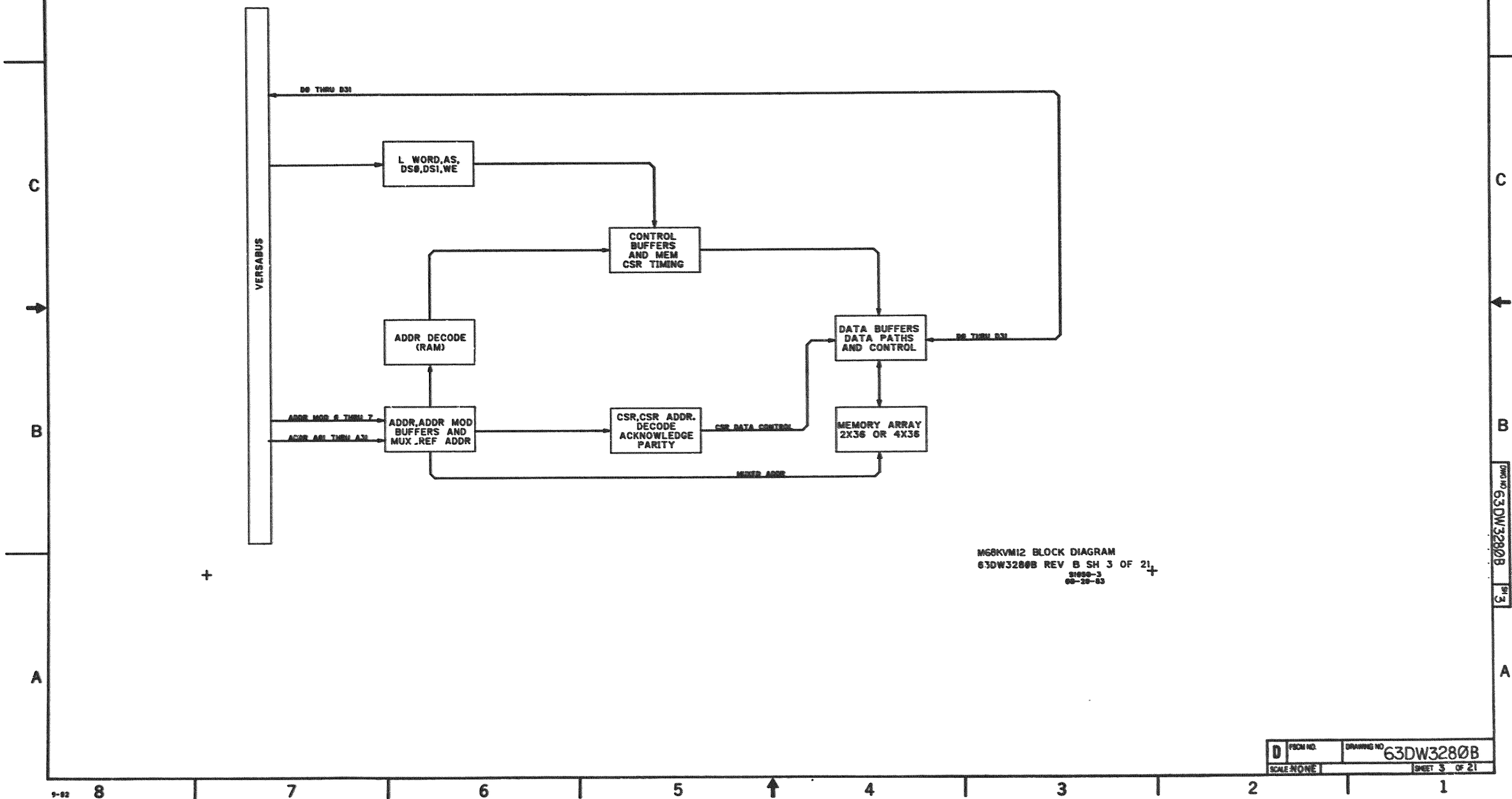
DWG NO 63DW3280B SH 2

D PSCM NO. DRAWING NO 63DW3280B
SCALE: NONE SHEET 2 OF 21

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 2 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	B	SEE SHEET 1.		



M68KVM12 BLOCK DIAGRAM
63DW3280B REV B SH 3 OF 21
S1030-3
08-20-83

DWG NO 63DW3280B SH 3

D	FSCM NO.	DRAWING NO 63DW3280B
SCALE NONE		SHEET 3 OF 21

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 3 of 21)

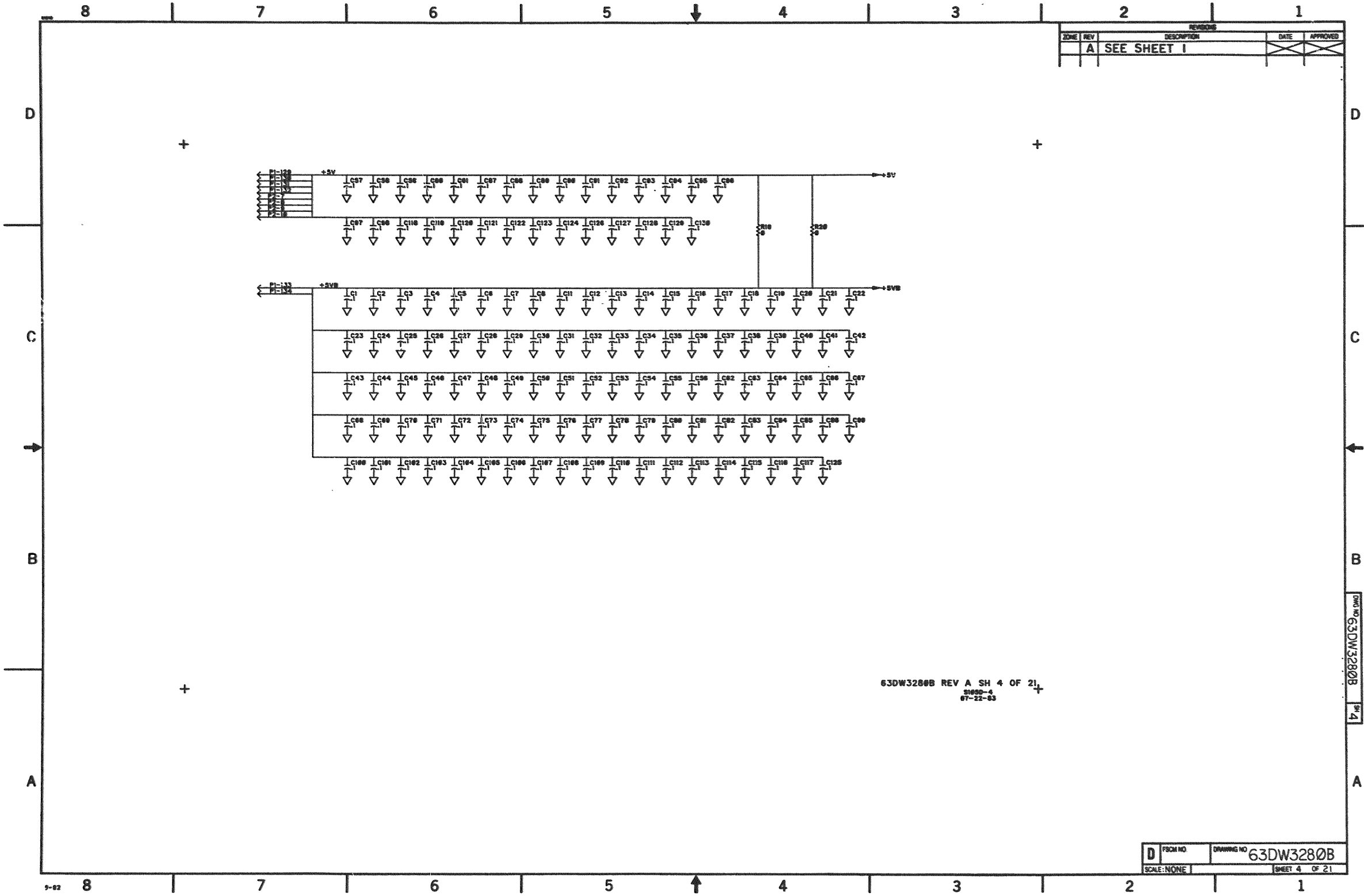


FIGURE 5-2. VM12 Schematic Diagram (Sheet 4 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	B	SEE SHEET 1		

ADDR BUFFERS, MUX

63DW3280B REV B SH 5 OF 21

SIGSD-3
07-22-83

D	FSCM NO.	DRAWING NO 63DW3280B
SCALE NONE		SHEET 5 OF 21

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 5 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	C	SEE SHEET 1		

ADDR BUFFERS, MUX

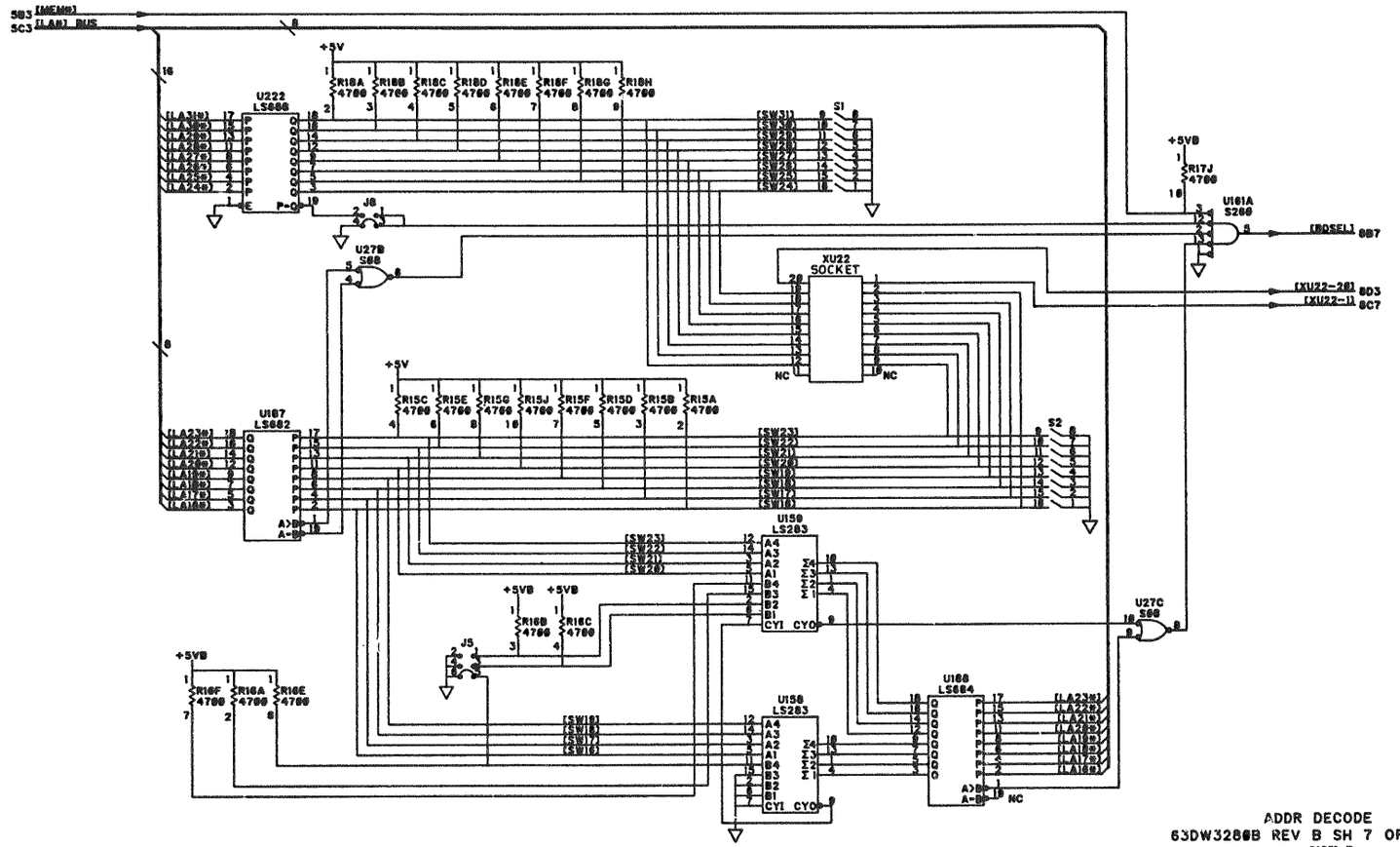
63DW3280B REV C SH 6 OF 21

SI850-6
07-22-83

D	FSCM NO.	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 6 OF 21

FIGURE 5-2. VM12 Schematic Diagram (Sheet 6 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	B	SEE SHEET 1.		



ADDR DECODE
63DW3280B REV B SH 7 OF 21
S1651-7
10-06-83

D	FSCM NO	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 7 OF 21

DWG NO 63DW3280B SH 7

FIGURE 5-2. VM12 Schematic Diagram (Sheet 7 of 21)
5-23/5-24

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	B	SEE SHEET 1		

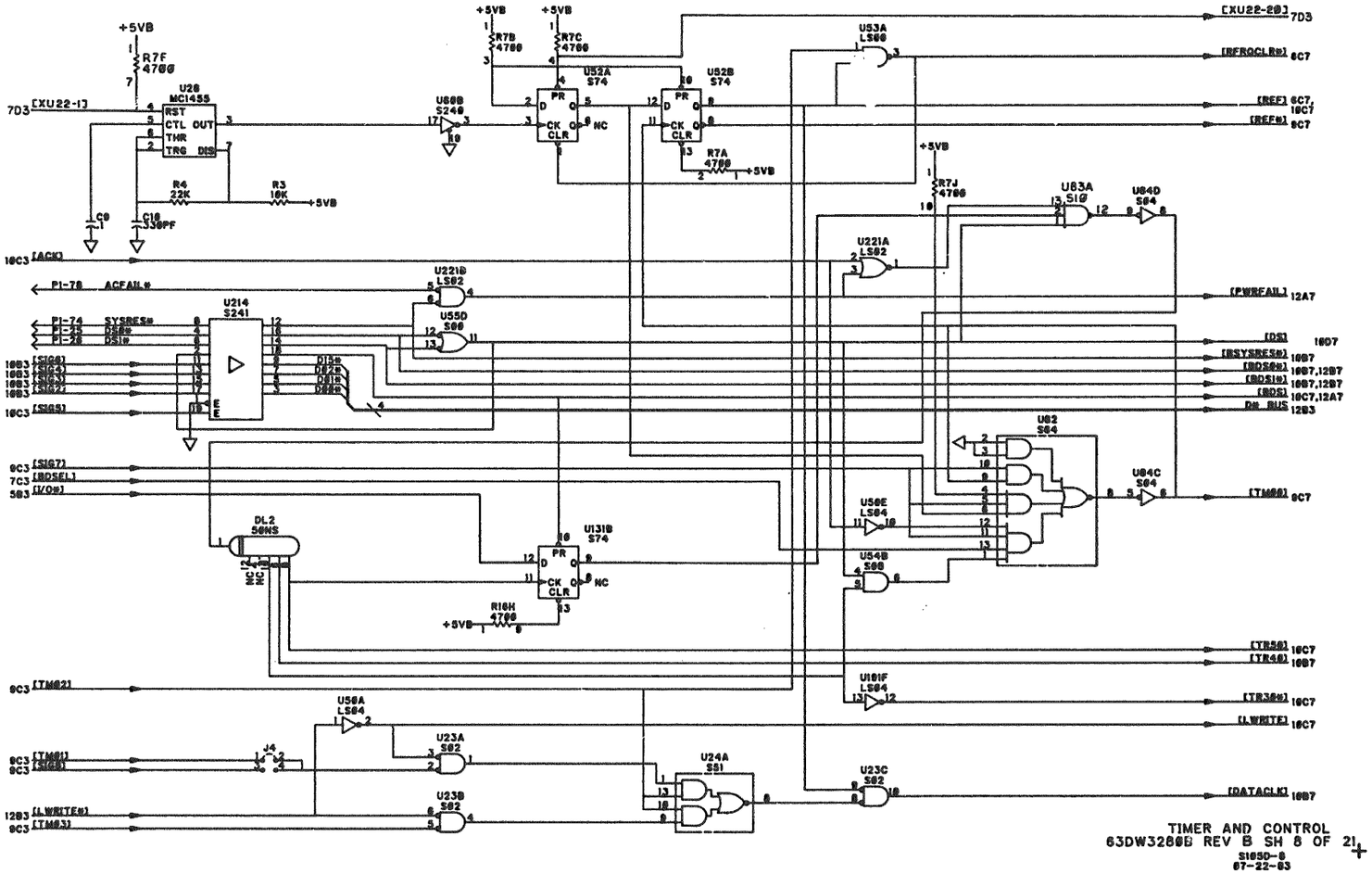
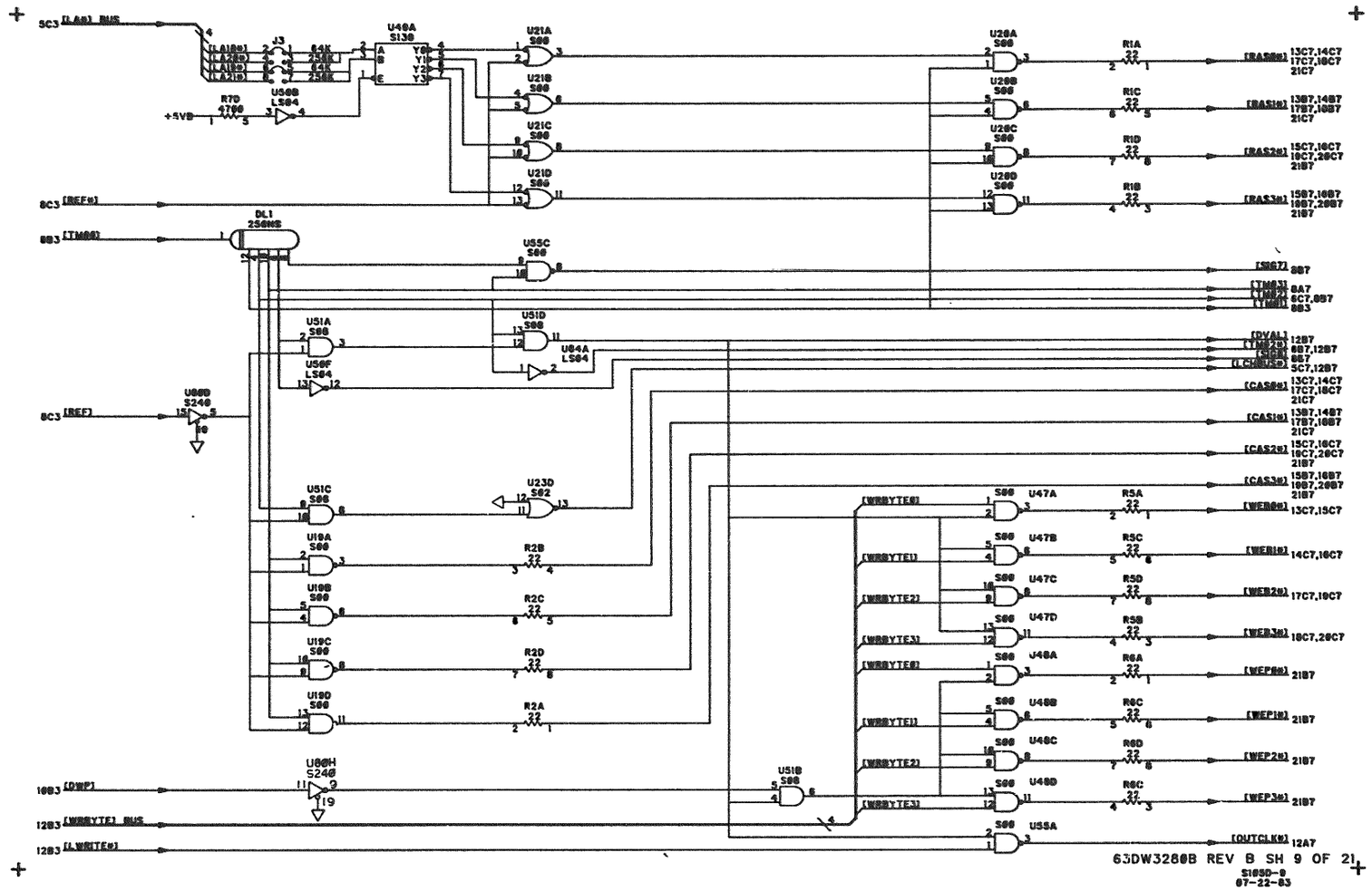


FIGURE 5-2. VM12 Schematic Diagram (Sheet 8 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	B	SEE SHEET 1		



63DW3280B REV B SH 9 OF 21

S105D-9
07-22-83

DWG NO 63DW3280B REV 9

D	FSCM NO	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 9 OF 21

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 9 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	C	SEE SHEET 1		

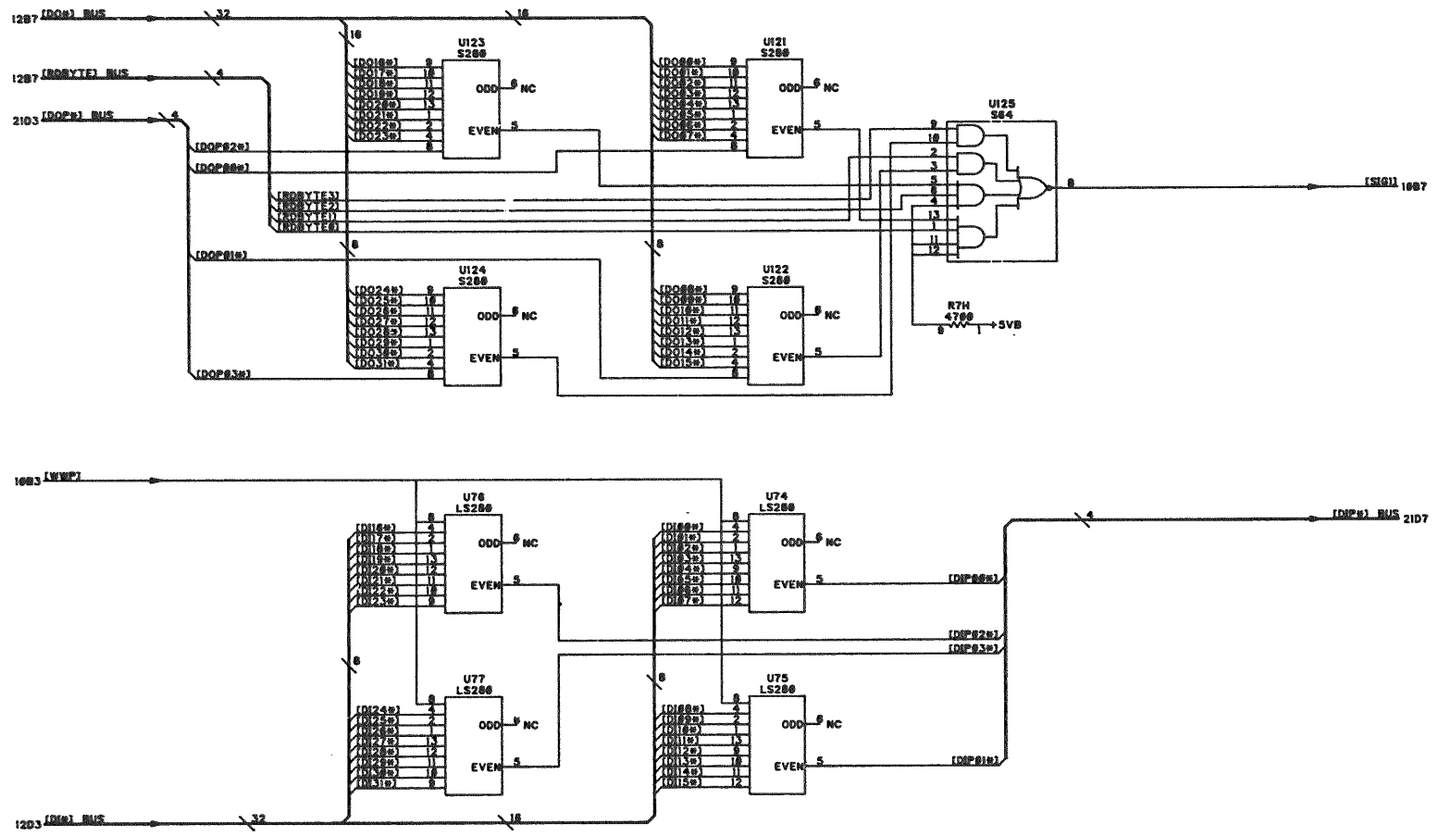
63DW3280B REV C SH 10 OF 21
S1690-10
07-22-83

D	FSCM NO.	DRAWING NO. 63DW3280B
SCALE: NONE		SHEET 10 OF 21

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 10 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	SEE SHEET 1		



PARITY, CSR
63DW3280B REV A SH 11 OF 21
S1050-11
07-27-83

D	FSCM NO.	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 11 OF 21

DWG NO 63DW3280B SH 11

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 11 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	B	SEE SHEET 1		

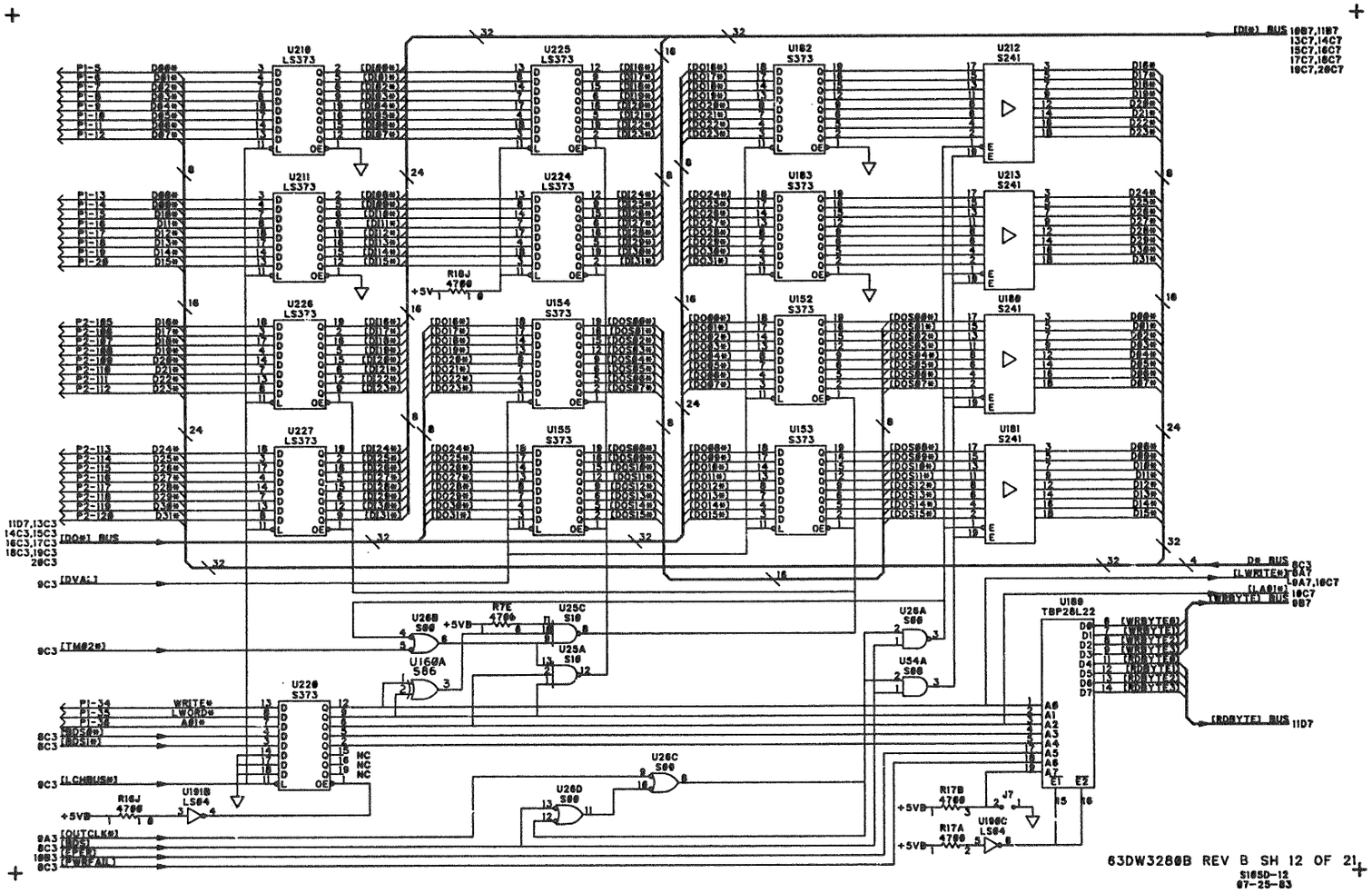
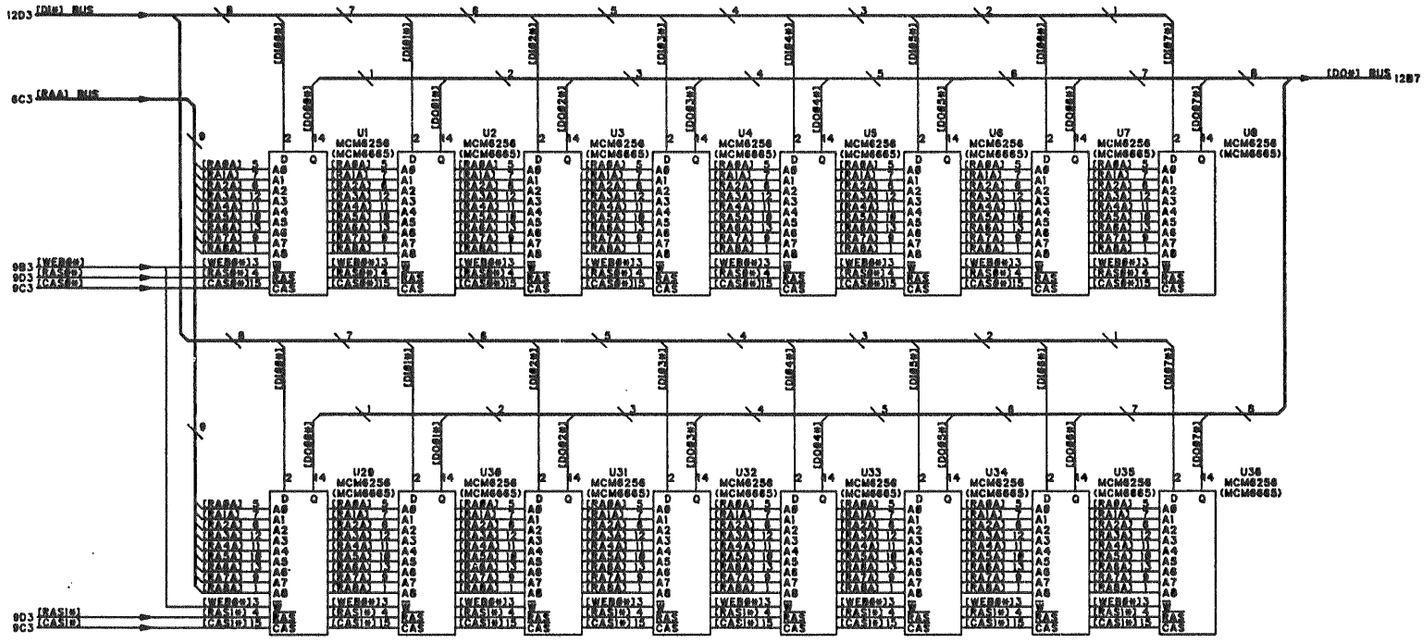


FIGURE 5-2. VM12 Schematic Diagram (Sheet 12 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	SEE SHEET 1		



63DW3280B REV A SH 13 OF 21
S1050-13
07-22-83

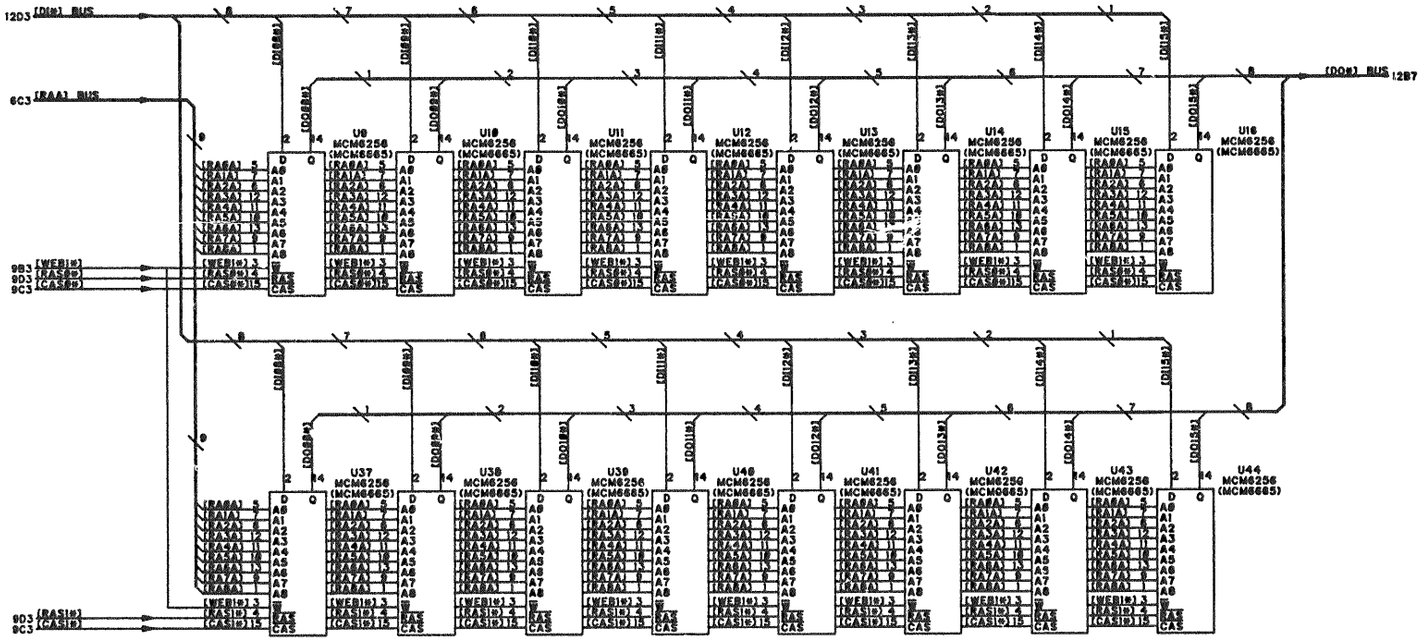
DWG NO 63DW3280B SH 13

D	FSCM NO.	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 13 OF 21

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 13 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	SEE SHEET 1		



63DW3280B REV A SH 14 OF 21
S1650-14
07-22-83

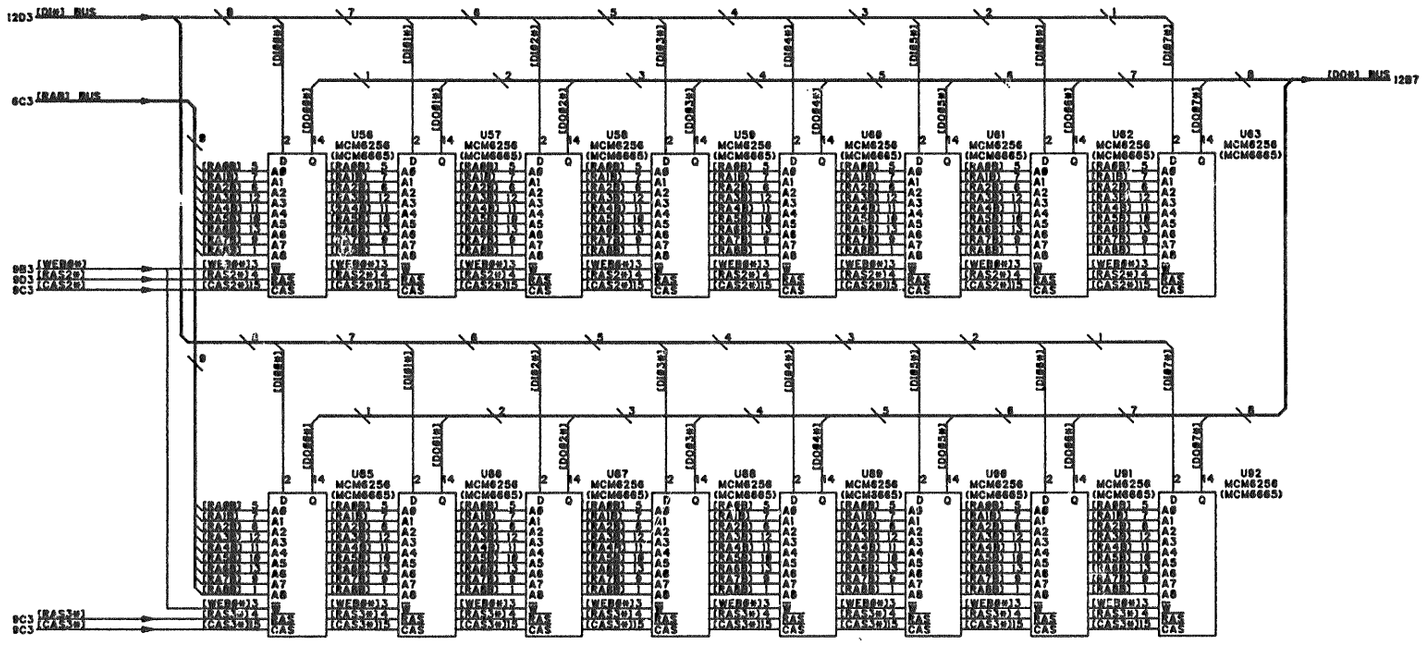
D	FSCM NO.	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 14 OF 21

DWG NO 63DW3280B SH 14

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 14 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	SEE SHEET 1		



63DW3280B REV A SH 15 OF 21
SIGSD-15
07-22-83

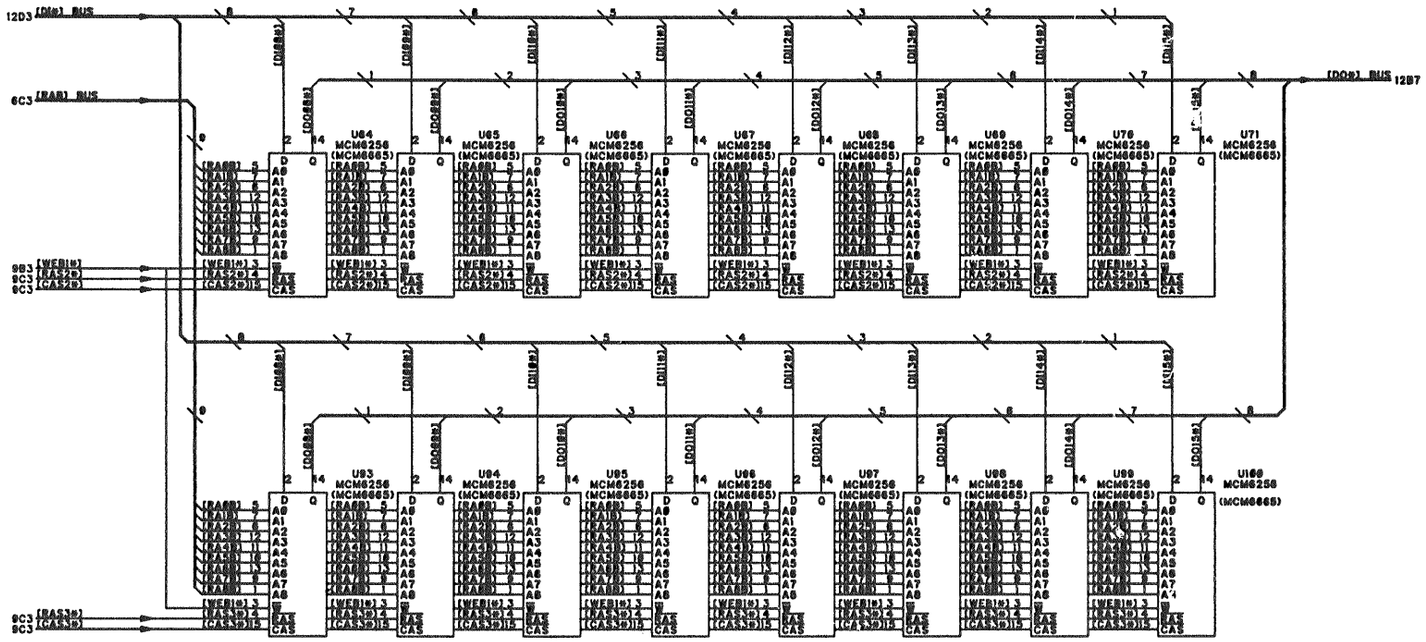
D	FSCM NO	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 15 OF 21

DWG NO 63DW3280B SH 15

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 15 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	SEE SHEET 1		



63DW3280B REV A SH 16 OF 21
S165D-16
07-22-83

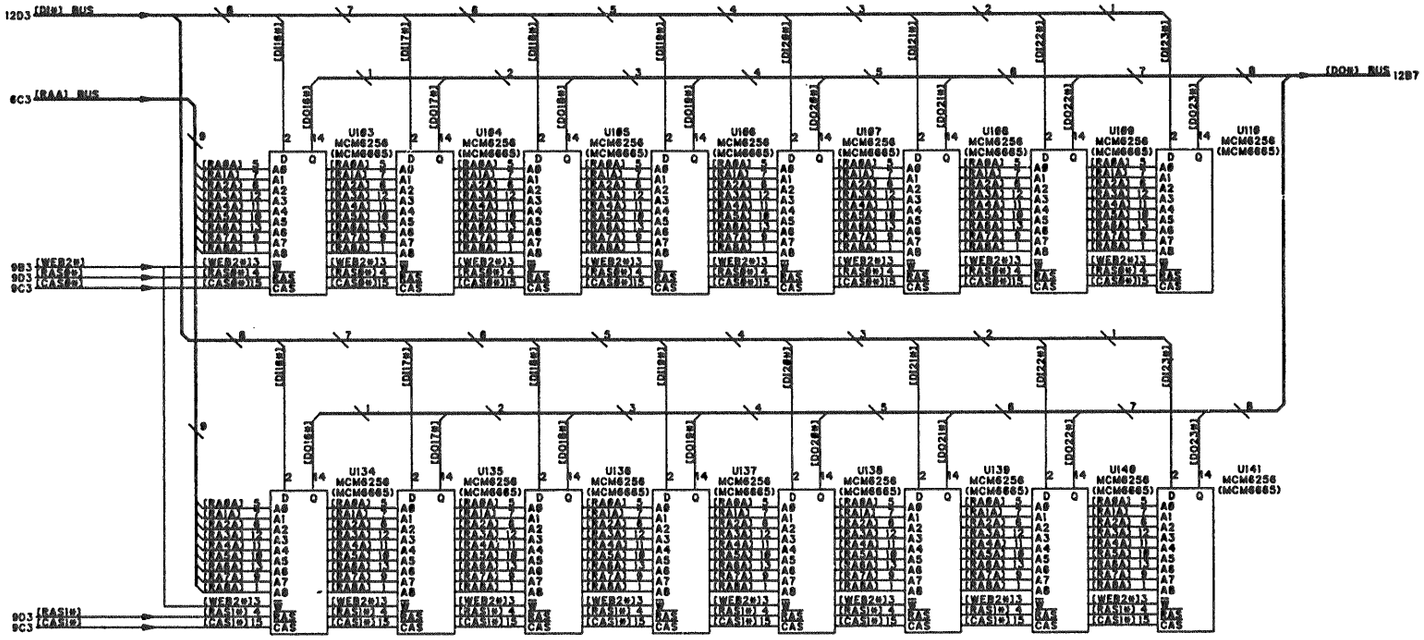
DWG NO 63DW3280B SH 16

D	FSCM NO.	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 16 OF 21

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 16 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	SEE SHEET 1		



63DW3280B REV A SH 17 OF 21
S1050-17
07-22-83

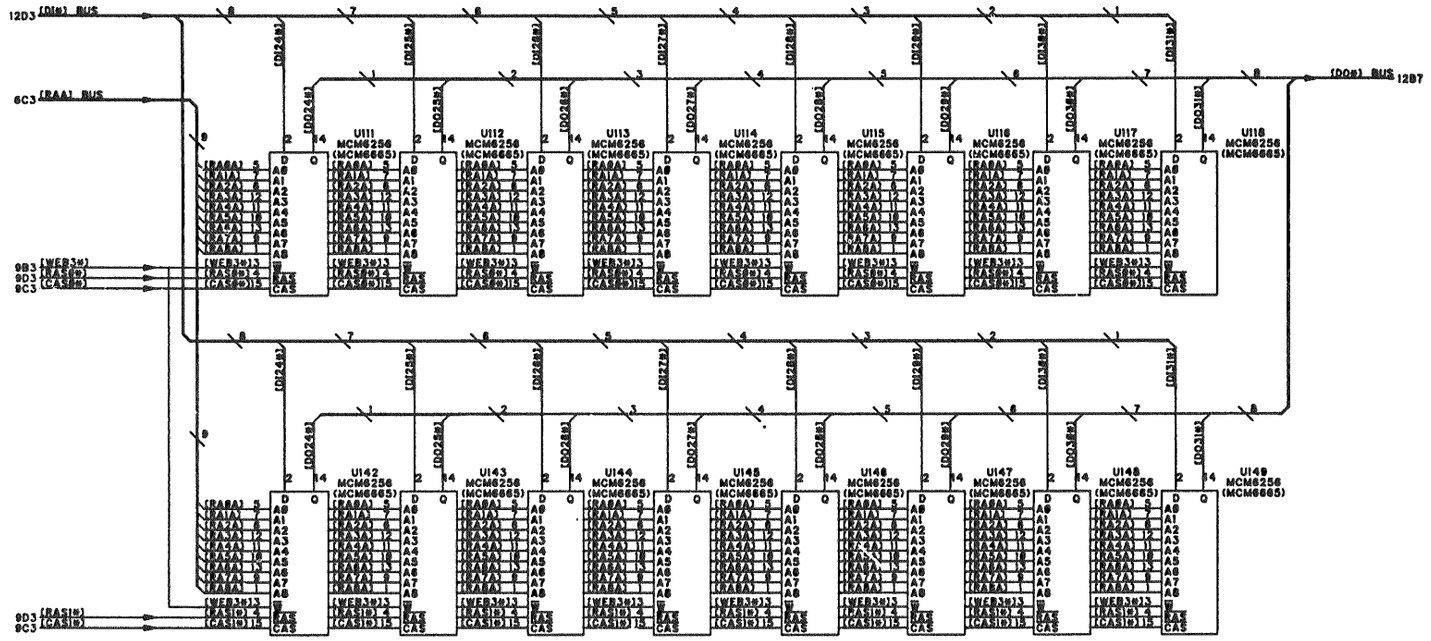
D	FSCM NO.	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 17 OF 21

DWG NO 63DW3280B 1M 17

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 17 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	SEE SHEET 1		



63DW3280B REV A SH 18 OF 21
SI05D-18
07-22-83

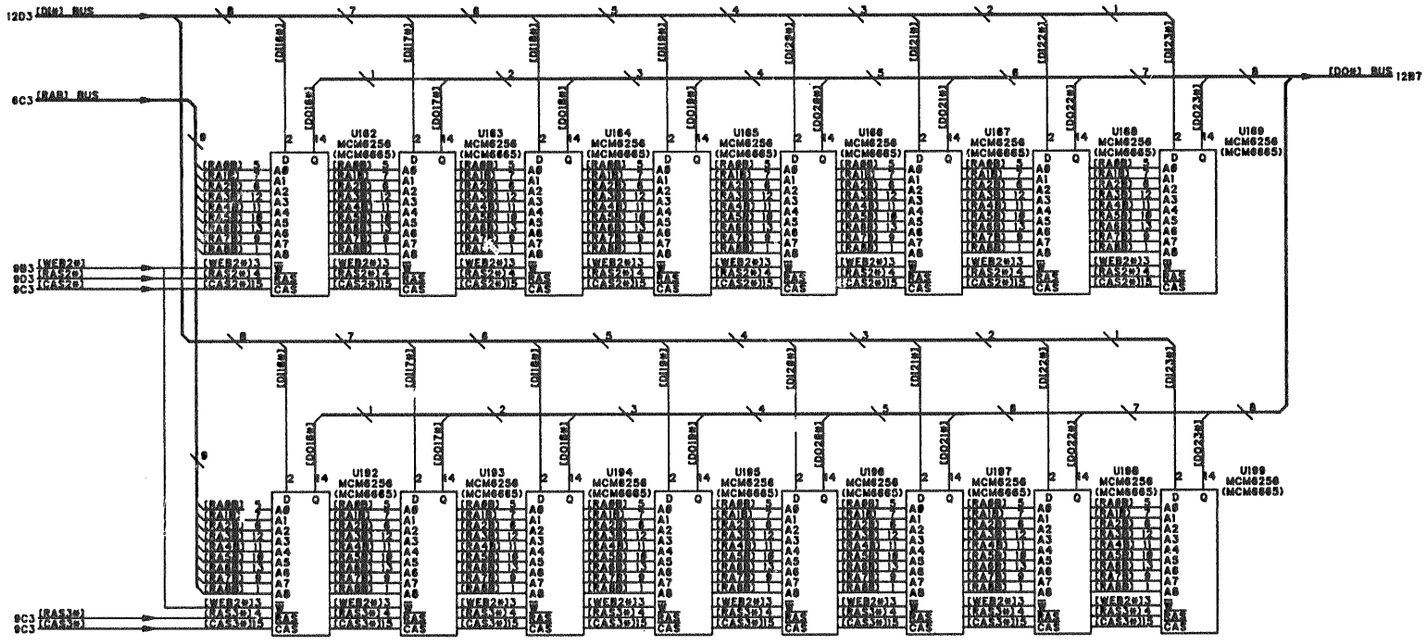
DWG NO 63DW3280B REV 18

D	FSCM NO.	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 18 OF 21

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 18 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	SEE SHEET 1		



63DW3280B REV A SH 19 OF 21
S1650-18
07-22-83

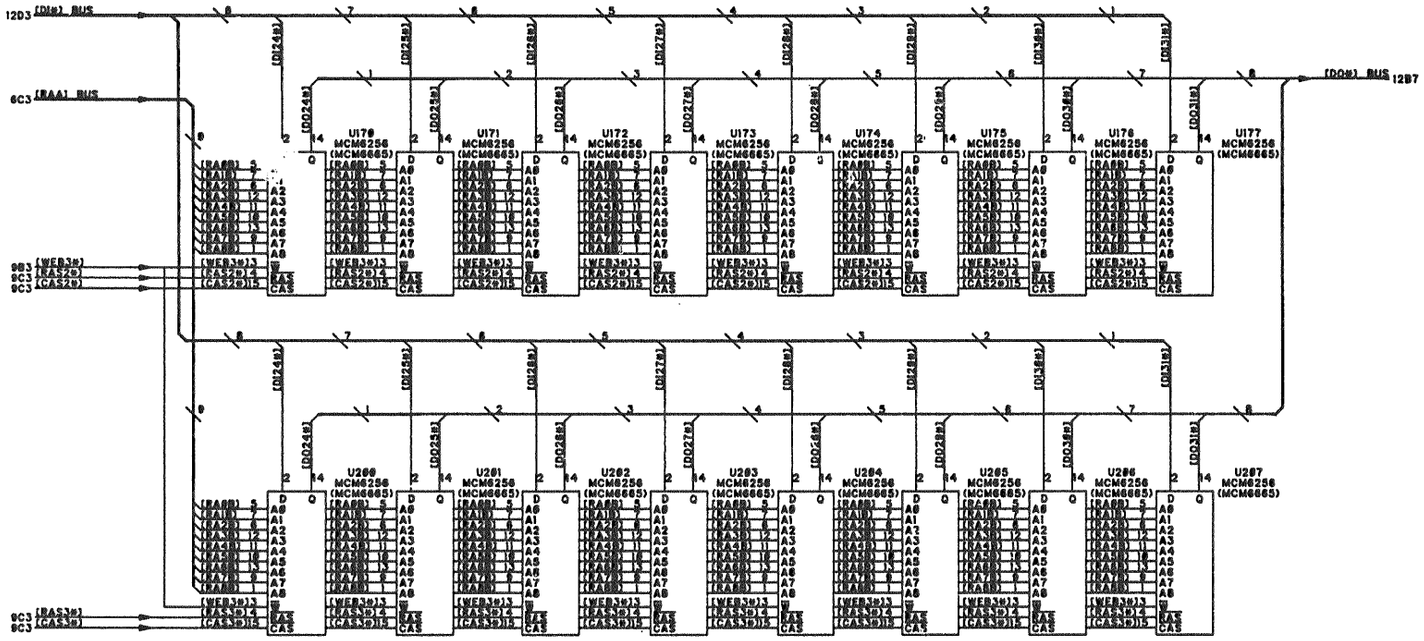
D	FSCM NO	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 19 OF 21

DWG NO 63DW3280B SH 19

9-82

FIGURE 5-2. VM12 Schematic Diagram (Sheet 19 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	SEE SHEET 1		



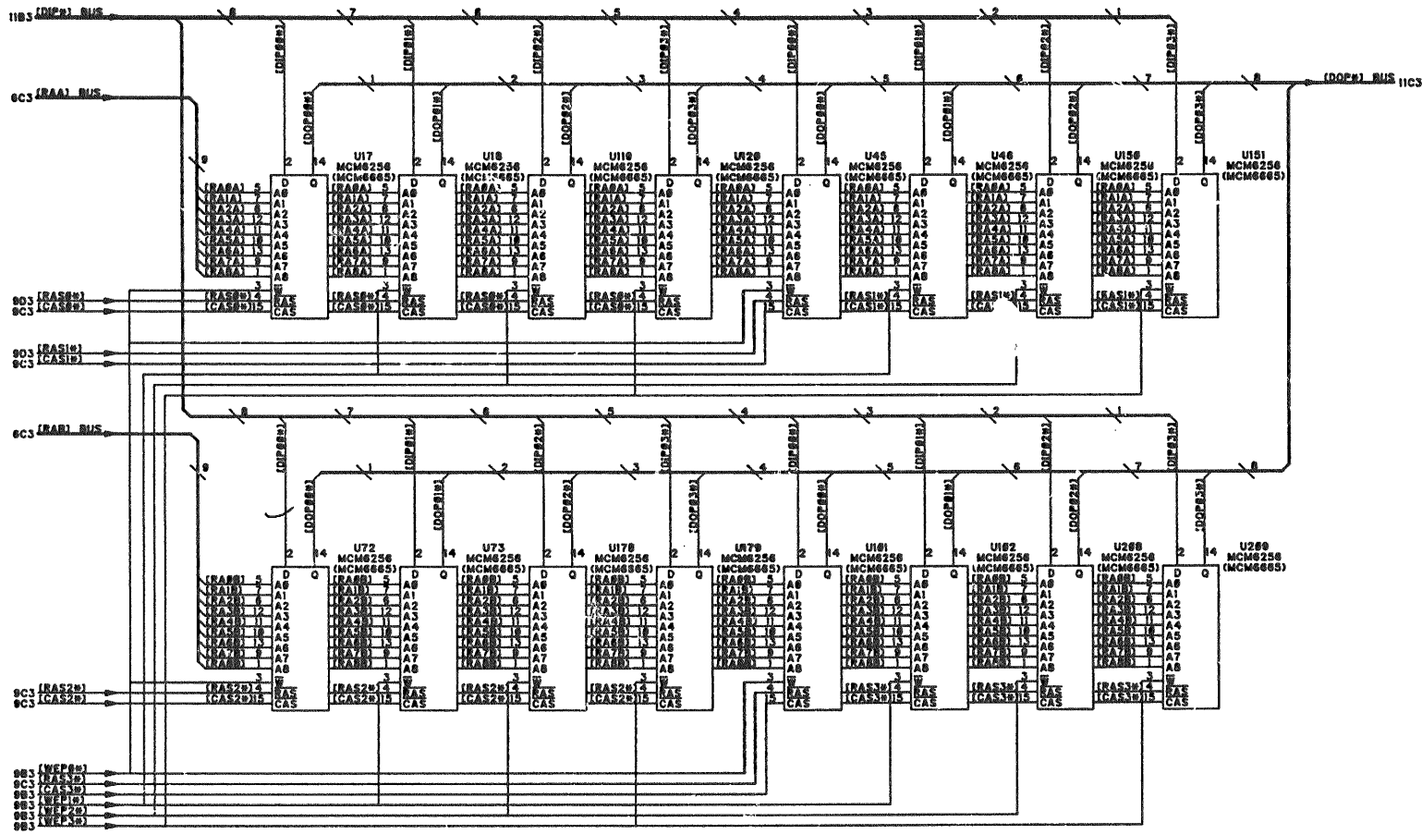
63DW3280B REV A SH 20 OF 21
SI65D-20
07-22-83

D	FSCM NO	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 20 OF 21

DWG NO 63DW3280B SH 20

FIGURE 5-2. VM12 Schematic Diagram (Sheet 20 of 21)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	SEE SHEET 1		



63DW3280B REV A SH 21 OF 21
S165D-21
07-22-83

DWG NO 63DW3280B SH 21

D	FSCM NO.	DRAWING NO 63DW3280B
SCALE: NONE		SHEET 21 OF 21

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FIGURE 5-2. VM12 Schematic Diagram (Sheet 21 of 21)

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