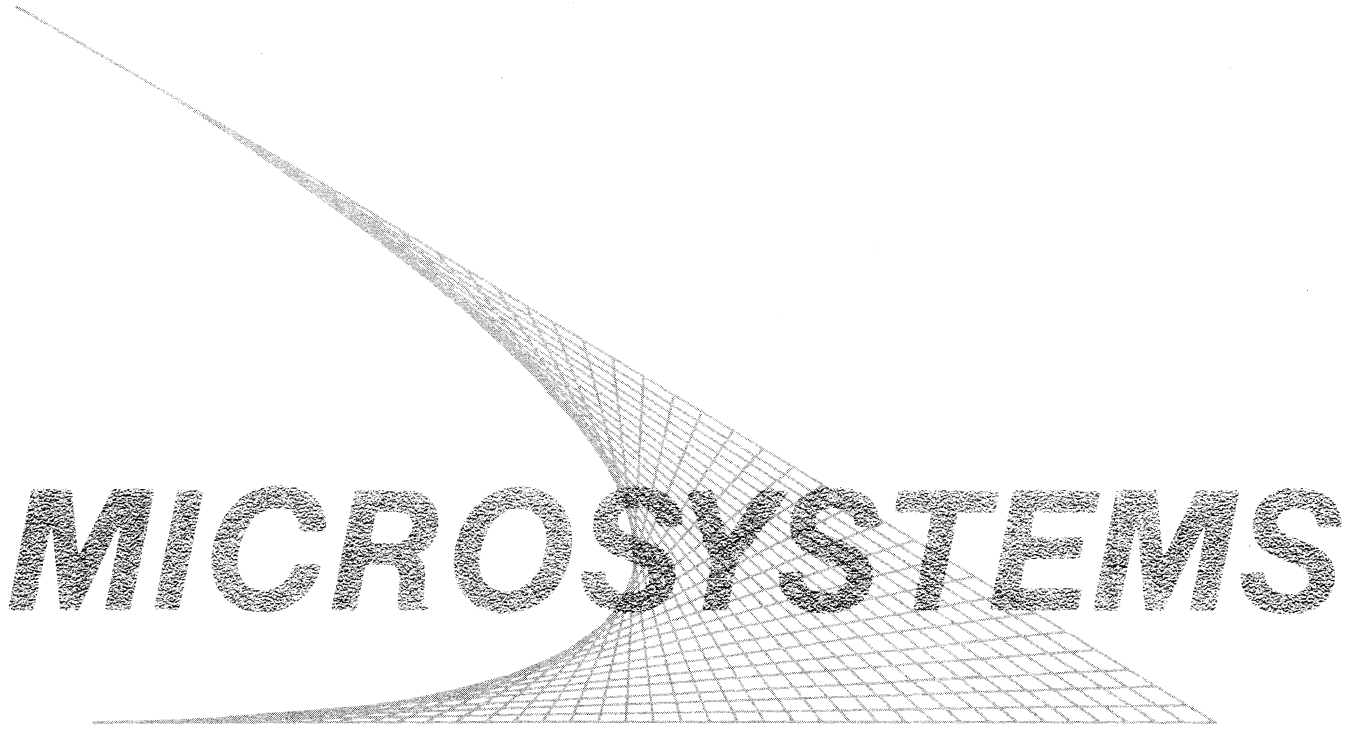
MOTOROLA

MVME400/D2

MVME400
Dual RS-232C
Serial Port Module
User's Manual



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MVME400/D2

AUGUST 1983

MVME400

DUAL RS-232C SERIAL PORT MODULE

USER'S MANUAL

This manual includes previous addendum A1 generated against issue D1.

Second Edition

First Edition October 1982

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Microsystems Warranty and Repair for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

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PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

TABLE OF CONTENTS

TABLE OF CONTENTS (cont'd)

LIST OF ILLUSTRATIONS

LIST OF TABLES

CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, hardware preparation and installation instructions, operating instructions, functional description, and support information for the MVME400 Dual RS-232C Serial Port Module (referred to as DSP throughout this manual). The DSP is shown in Figure 1-1.

1.2 FEATURES

Features of the DSP are listed below.

- Single-wide VME board form factor.
- Motorola I/O Channel interface compatible.
- RS-232C interface compatible.
- Two independent, full duplex RS-232C I/O channels.
- NEC7201 multiprotocol serial controller.
- Asynchronous, bisynchronous, High-level Data Link Control (HDLC), and Synchronous Data Link Control (SDLC) protocol capability.
- Terminal or modem interface jumpers.
- Interrupts jumperable to any of four I/O bus interrupt levels.
- Jumper-selectable base address.
- Eight jumper-selectable baud rates when used with VMEbug; 16 software-programmable baud rates.
- Self-test FAIL LED indicator.

1.3 SPECIFICATIONS

General specifications for the DSP are given in Table 1-1.

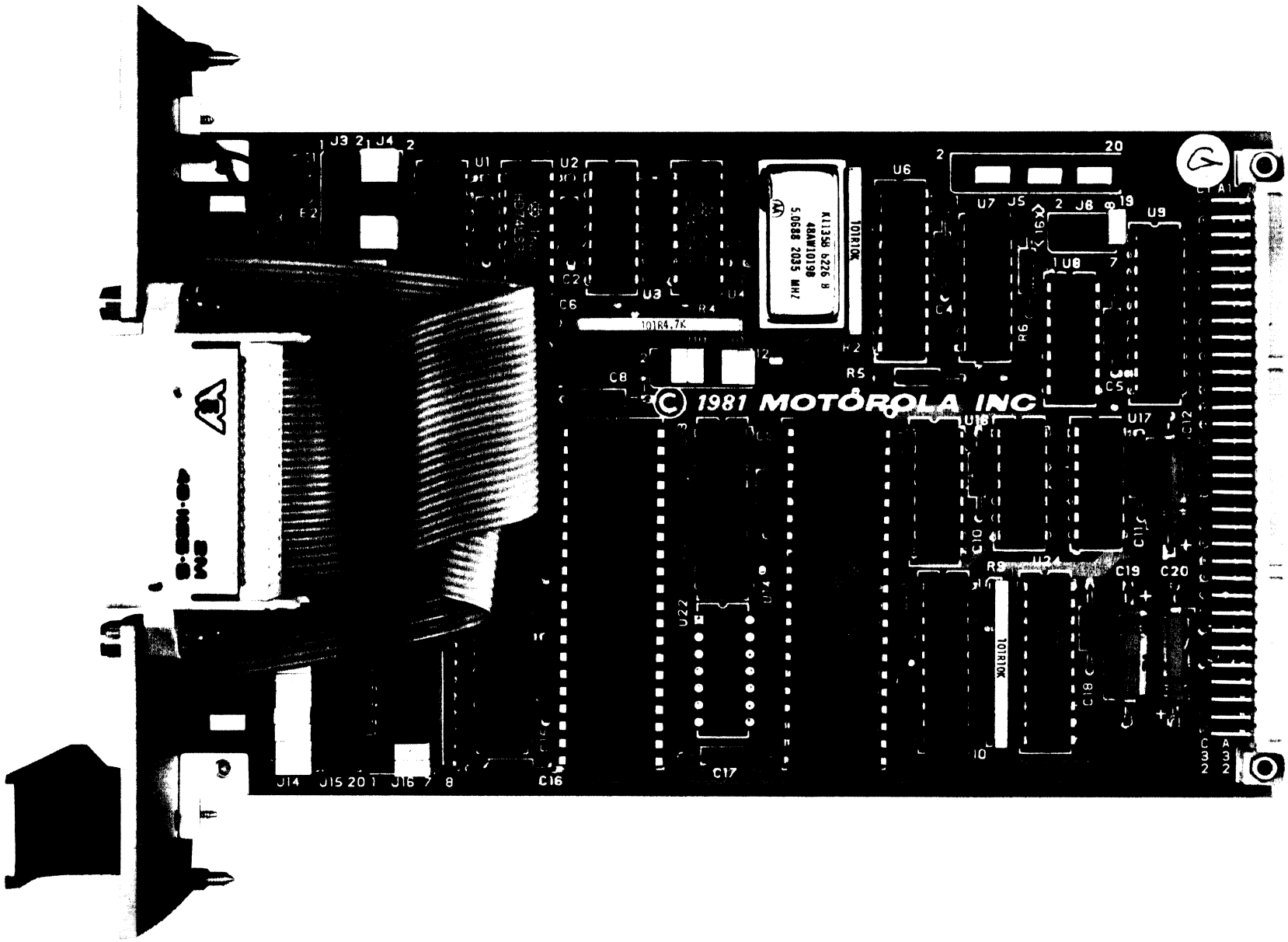


FIGURE 1-1. Dual RS-232C Serial Port Module

TABLE 1-1. Dual RS-232C Serial Port Module Specifications

CHARACTERISTIC	SPECIFICATIONS
Power requirements	+5 Vdc @ 450 mA typical (991 mA maximum)
	+12 Vdc @ 50 mA typical
	-12 Vdc @ 40 mA typical
Temperature	
Operating	0° to 70° C
Storage	-40° to 85° C
Relative humidity	0% to 90% (non-condensing)
Physical characteristics	
PC board only	
Height	6.30 in. (160 mm)
Width	3.94 in. (100 mm)
Thickness	0.59 in. (15 mm)
PC board with connectors and board stiffener	
Height	7.40 in. (188 mm)
Width	5.12 in. (130 mm)
Thickness	1.60 in. (41 mm)

1.4 GENERAL DESCRIPTION

The DSP is an I/O Channel-compatible dual RS-232C serial interface module. This module conforms to the single-wide VME board form factor and interfaces to the I/O Channel with a single 64-pin DIN 41612 standard connector; however, because of the wide front panel, the DSP occupies two module card slots. The DSP is used to expand the resources of an I/O Channel master to include one or two additional RS-232C serial data ports.

An NEC7201 serial controller is used to provide multiprotocol capabilities (asynchronous, bisynchronous, HDLC, and SDLC). Modem output control lines (RTS, CTS, DTR, DCD, DSR, and RI) are provided, in addition to the clock and data lines. A front panel FAIL LED indicator is used to indicate a module malfunction.

The user must provide a connector-compatible I/O Channel backplane or ribbon cable to connect the DSP to the I/O Channel master. Refer to the I/O Channel Specification Manual, Motorola publication number M68RIOCS, for interfacing and backplane information. The user must also provide the RS-232C cables to connect the DSP (via front panel connectors) to the terminal/modem devices.

1.5 RELATED DOCUMENTATION

Related documentation applicable to the DSP are as follows:

- Input/Output Channel Specification Manual, M68RIOCS
- NEC Corp., UPD7201 Technical Manual

CHAPTER 2

HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides unpacking, hardware preparation, and installation instructions for the Dual RS-232C Serial Port Module.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request carrier's agent be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment.

2.3 HARDWARE PREPARATION

This section describes the hardware preparation of the DSP module prior to system installation. The DSP has been factory tested for system operation, and is shipped with factory-installed jumpers. These factory-installed jumper connections should be verified to ensure that the module is properly configured for system operation. The DSP is configurated to interface the I/O Channel master with RS-232C compatible equipment.

There are 15 headers (J2-J16) on the DSP, as shown in Figure 2-1. Table 2-1 lists each header, its function, and the factory-installed jumper configuration.

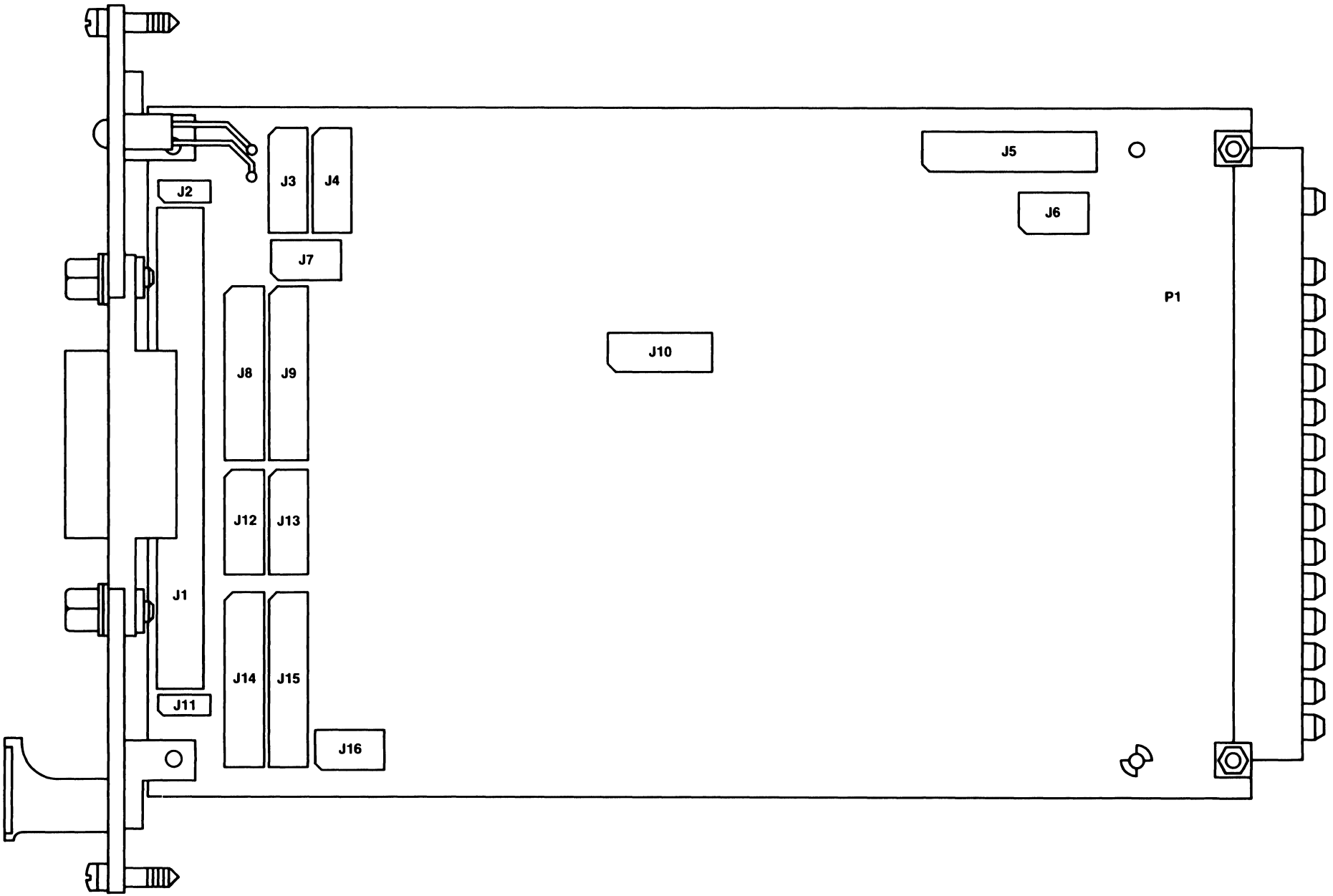


FIGURE 2-1. DSP Module Header Location Diagram

TABLE 2-1. DSP Module Headers

HEADER	FUNCTION	FACTORY CONFIGURATION
J2	Port 2 TxC select	1-2
J3	Port 2 external clock select	No jumpers
J4	Port 2 internal clock select	1-2, 3-4, 9-10, 11-12
J5	Interrupt level select	3-5, 9-11, 15-17
J6	Base address select	7-8
J7	Port 2 CTS flow control	5-7, 6-8
J8	Port 2 to modem select	No jumpers
J9	Port 2 to terminal select	1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, 15-16, 17-18, 19-20
J10	Baud rate port 1 and 2 select	3-4, 5-6,9-10, 11-12
J11	Port 1 TxC select	1-2
J12	Port 1 external clock select	No jumpers
J13	Port 1 internal clock select	1-2, 3-4, 9-10, 11-12
J14	Port 1 to modem select	No jumpers
J15	Port 1 to terminal select	1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, 15-16, 17-18, 19-20
J16	Port 1 CTS flow control	5-7, 6-8

2.3.1 Port 1/2 TxC Select Headers (J2, J11)

Headers J2 (for port 2) and J11 (for port 1) control selection of either a terminal (DTE) or modem (DCE) to receive the TxC signal. Pins 2 and 3 are jumpered to select pin 15 of the subminiature 25-pin D RS-232C connector, or pins 1 and 2 are jumpered to select pin 24 of the connector. Pin 15 is the transmit signal element timing with the DCE as the source. Pin 24 is the transmit signal element timing with the DTE as the source. Figure 2-2 illustrates the factory configuration of these headers.

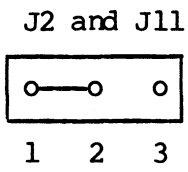


FIGURE 2-2. Port 1/2 TxC Select Headers (J2, J11)

2.3.2 Port 2 Internal/External Clock Headers (J3, J4)

Headers J3/J4 control the internal or external clock signals entering or leaving port 2. The factory header configurations for J3 and J4 are shown in Figure 2-3. Table 2-2 lists the jumper configurations that control the clock signals for port 2. The user must first select one of three operational modes (asynchronous, synchronous, or test). After selecting the desired mode, the user must select the desired clock interconnect (terminal/modem).

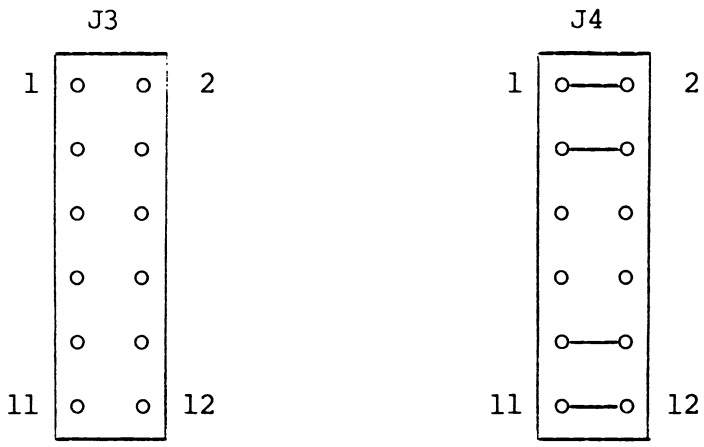


FIGURE 2-3. Port 2 Internal/External Clock Headers (J3, J4)

TABLE 2-2. Headers J3 and J4 Configurations

MODE SELECTION			
MODE	HEADER	PINS CONNECTED	REMARKS
Async. (1)	J3	none	
	J4	1-2*,3-4, 9-10*,11-12	Transmit and receive clocks are internally generated (on board).
Sync. (2,3)	J3	1-2, 3-4, 9-10, 11-12	Transmit and receive clocks are externally generated (off board).
	J4	none	
Test (3,4)	J3	9-10, 11-12	Receive clock is external.
	J4	1-2*, 3-4	Transmit clock is internal.

TERMINAL MODEM SELECTION			
INTER-CONNECT	HEADER	PINS CONNECTED	REMARKS
Modem (3)	J3	5-6, 7-8	Transmit and receive clock lines configured to interface with a modem.
	J4	none	
Terminal (3)	J3	none	
	J4	5-6, 7-8	Transmit and receive clock lines configured to interface with a terminal.

NOTES:

(1) Headers J8/J9 must be configured for the required terminal/modem select.

(2) Headers J2 (TxC select), J3/J4 (internal/external clock), and J8/J9 (terminal/modem select) must be configured to obtain synchronous operation.

(3) Pins 5-6 and 7-8 on header J4 are jumpered to transpose the RxC and TxC lines to interface with a terminal. Pins 5-6 and 7-8 on header J3 are jumpered to route RxC and TxC lines to interface directly with a modem.

(4) This special test configuration could be used to interface port 1 and port 2 (through an external user-provided cable), with one port configured as a terminal and the other as a modem. (See Note 3.)

(5) Asterisk (*) denotes a jumper connection which is unnecessary unless external monitoring of an internally generated clock signal is desired.

2.3.3 Interrupt Level (J5)

Header J5 determines which internal interrupt sources (7201 INT, PIA [IRQA], PIA [IRQB]) are used to drive the selected I/O channel interrupt line (INT1*-INT4*). One, any combination, or all of the internal interrupt sources can be connected to a single I/O channel interrupt line at the same time. However, only one I/O channel interrupt line can be connected to an interrupt source at one time. Figure 2-4 illustrates the factory configuration of header J5. Table 2-3 lists the jumper configurations for header J5.

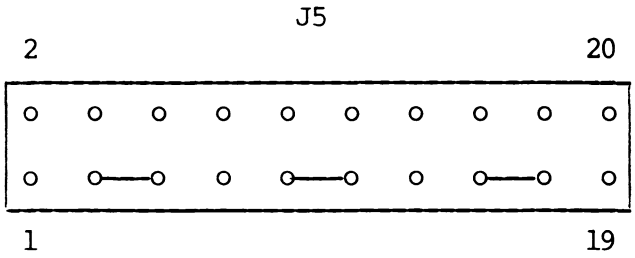


FIGURE 2-4. Interrupt Level (J5)

TABLE 2-3. Header J5 Configurations

PINS CONNECTED	REMARKS
14-16	7201 INT connected to INT1*
13-15	7201 INT connected to INT2*
15-17	7201 INT connected to INT3*
16-18	7201 INT connected to INT4*
2-4	PIA IRQA connected to INT1*
1-3	PIA IRQA connected to INT2*
3-5	PIA IRQA connected to INT3*
4-6	PIA IRQA connected to INT4*
8-10	PIA IRQB connected to INT1*
7-9	PIA IRQB connected to INT2*
9-11	PIA IRQB connected to INT3*
10-12	PIA IRQB connected to INT4*

2.3.4 Base Address Select Header (J6)

Header J6 can be configured to address the DSP to any $10 byte block within the first $100 byte blocks of the I/O Channel memory. Figure 2-5 illustrates the factory configuration of header J6. Table 2-4 lists the jumper configurations for header J6.

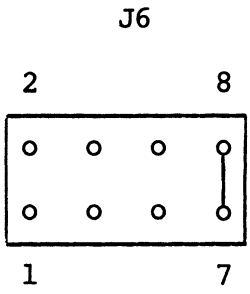


FIGURE 2-5. Base Address Select Header (J6)

TABLE 2-4. Header J6 Configurations

PINS CONNECTED	REMARKS
1-2, 3-4, 5-6, 7-8	Base address is $00
1-2, 3-4, 5-6	Base address is $10
1-2, 3-4, 7-8	Base address is $20
1-2, 3-4	Base address is $30
1-2, 5-6, 7-8	Base address is $40
1-2, 5-6	Base address is $50
1-2, 7-8	Base address is $60
1-2	Base address is $70
3-4, 5-6, 7-8	Base address is $80
3-4, 5-6	Base address is $90
3-4, 7-8	Base address is $A0
3-4	Base address is $B0
5-6, 7-8	Base address is $C0
5-6	Base address is $D0
7-8	Base address is $E0
none	Base address is $F0

2.3.5 CTS Control Headers (J7, J16)

Headers J7 and J16 are used to configure CTS for port 2 and port 1, respectively.

When port 1 is configured to interface with a modem (host), header J16 has no effect. When port 1 is configured to interface with a terminal, header J16 can be configured in two ways. One way is the factory-installed (normal) configuration shown in Figure 2-6, in which header J16 has jumpers installed on pins 5-7 and 6-8. In this configuration, RTS is looped back to CTS at the RS-232C interface and 7201 chip, respectively. The second configuration facilitates direct flow control (inhibition of transmitted data) and is accomplished by jumpering pins 2-4 and 1-3 on header J16. This enables the DTR at the 7201 chip to directly control CTS at the RS-232C interface to inhibit received data. The DTR at the RS-232C interface controls CTS at the 7201 chip and, therefore, can inhibit the DSP from transmitting data.

Port 2 is configured in a similar manner. When configured to interface with a modem, header J7 has no effect. When configured to interface with a terminal, header J7 can be configured in two ways -- the factory installed (normal), as shown in Figure 2-6, or (second configuration) when pins 2-4 and 1-3 are jumpered.

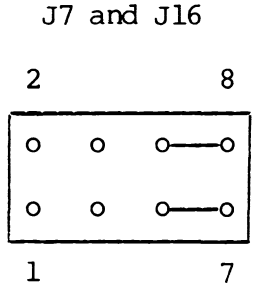


FIGURE 2-6. CTS Control Headers (J7, J16)

2.3.6 Modem/Terminal Select Headers (J8, J9, J14, J15)

Headers J8 and J9 are used to configure port 2 to interface with a modem or a terminal, while headers J14 and J15 perform the same function for port 1.

To interface with a modem, jumpers are installed on pins 1-2, 3-4, ... through 19-20 on header J8 for port 2 (J14 for port 1). Similarly, to interface with a terminal, install jumpers on pins 1-2, 3-4, ... through 19-20 on header J9 for port 2 (J15 for port 1). When header J9 or J15 is configured to interface with a terminal, header J7 or J16 must also be configured for this mode. Modules shipped from the factory are configured to interface with a terminal. Figure 2-7 illustrates the factory configuration of these headers.

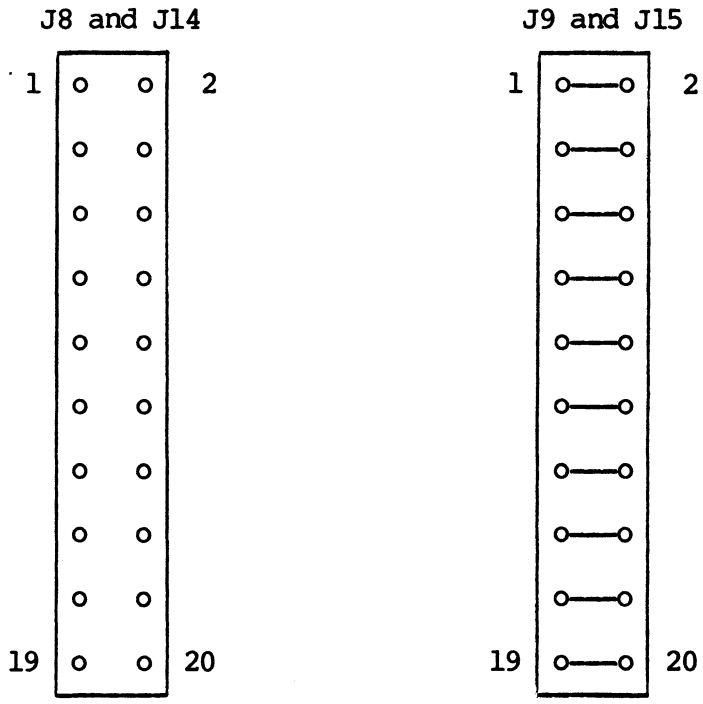


FIGURE 2-7. Modem/Terminal Select Headers (J9 and 15, J8 and J14)

2.3.7 Baud Rate Port 1 and 2 Select Header (J10)

NOTE

Baud rate selection for the DSP is controlled by software. Jumper selection (J10) is interpreted by software in some cases and used to select the baud rate. Before configuring header J10 jumpers, the user should read paragraphs 4.6 and 4.7, which pertain to the baud rate generation and selection capabilities of this module.

Header J10 has 12 pins and is divided into two sections. Pins 1-6 control the baud rate at port 1, while pins 7-12 control the baud rate at port 2. Figure 2-8 illustrates the factory configuration of header J10 for a baud rate of 9600 for both ports, however, the baud rate for each port is independently selectable. Table 2-5 lists jumper-selectable baud rates.

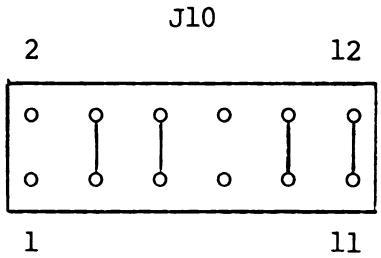


FIGURE 2-8. Baud Rate Port 1 and 2 Select Header (J10)

TABLE 2-5. Header J10 Configurations

PORT 1 PINS CONNECTED	PORT 2 PINS CONNECTED	BAUD RATE
None	None	110
1-2,	7-8	300
3-4,	9-10	1,200
1-2, 3-4,	7-8, 9-10	2,400
5-6,	11-12	4,800
1-2, 5-6,	7-8, 11-12	7,200
3-4, 5-6,	9-10, 11-12	9,600
All	All	19,200

2.3.8 Port 1 Internal/External Clock Headers (J12, J13)

Headers J12, J13 control the internal or external clock signals entering or leaving port 1. The factory header configurations for J12 and J13 are illustrated in Figure 2-9. Table 2-6 lists the jumper configurations that control the clock signals for port 1. The user must first select one of three operational modes (asynchronous, synchronous, or test). After selecting the desired mode, the user must select the desired clock interconnect (terminal/modem).

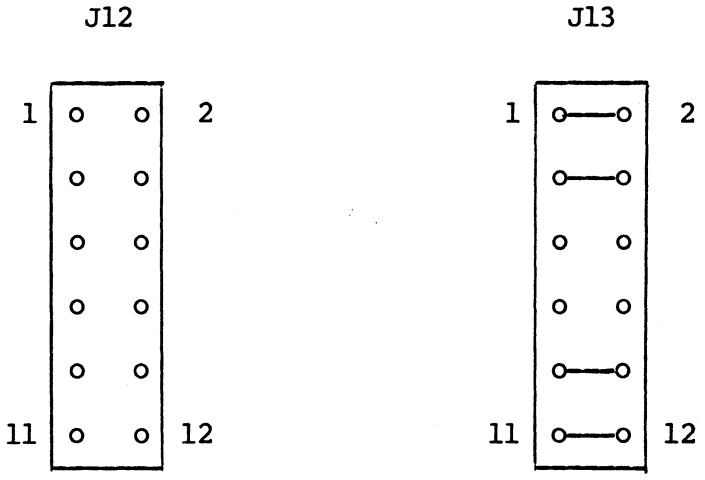


FIGURE 2-9. Port 1 Internal/External Clock Headers (J12, J13)

TABLE 2-6. Headers J12 and J13 Configurations

MODE SELECTION			
MODE	HEADER	PINS CONNECTED	REMARKS
Async. (1)	J12	none	
	J13	1-2*,3-4, 9-10*,11-12	Transmit and receive clocks are internally generated (on board).
Sync. (2,3)	J12	1-2, 3-4, 9-10, 11-12	Transmit and receive clocks are externally generated (off board).
	J13	none	
Test (3,4)	J12	9-10, 11-12	Receive clock is external.
	J13	1-2*, 3-4	Transmit clock is internal.

TERMINAL/MODEM SELECTION			
INTER-CONNECT	HEADER	PINS CONNECTED	REMARKS
Modem (3)	J12	5-6, 7-8	Transmit and receive clock lines configured to interface with a modem.
	J13	none	
Terminal (3)	J12	none	
	J13	5-6, 7-8	Transmit and receive clock lines configured to interface with a terminal.

NOTES:

(1) Headers J14/J15 must be configured for the required terminal/modem select.

(2) Headers J11 (TxC select), J12/J13 (internal/external clock), and J14/J15 (terminal/modem select) must be configured to obtain synchronous operation.

(3) Pins 5-6 and 7-8 on header J13 are jumpered to transpose the RxC and TxC lines to interface with a terminal. Pins 5-6 and 7-8 on header J12 are jumpered to route RxC and TxC lines to interface directly with a modem.

(4) This special test configuration could be used to interface port 1 and port 2 (through an external user-provided cable), with one port configured as a terminal and the other as a modem. (See Note 3.)

(5) Asterisk (*) denotes a jumper connection which is unnecessary unless external monitoring of an internally generated clock signal is desired.

2.4 INSTALLATION INSTRUCTIONS

When the DSP has been configured as desired by the user, it is ready to be installed in a VME chassis or an I/Omodule 5-slot card cage.

2.4.1 Installation in VME Chassis

The DSP is installed in a VME chassis as follows:

a. Turn all equipment power OFF.

CAUTION

CONNECTING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

b. Insert DSP in any single-width card slot.

c. Secure in place with two captive screws.

d. The DSP can be connected to any combination of terminals or modems (up to a total of two) by mating one or two male subminiature D, 25-pin RS-232C connectors to front panel female subminiature D connectors. Flat ribbon cable is not recommended because excessive cross-talk can occur on the clock lines, resulting in errors. Figure 2-10 illustrates a typical interface cabling for the DSP.

e. Equipment power may be turned ON.

2.4.2 Installation in 5-Slot I/Omodule Card Cage

The DSP is installed in a 5-slot I/Omodule card cage as follows:

a. Turn all equipment power OFF.

CAUTION

CONNECTING MODULES WHILE POWER IS APPLIED MAY RESULT IN DAMAGE TO COMPONENTS ON THE MODULE.

b. If card cage in part of VERSAmodule chassis, remove card slot cover plate.

c. Insert DSP in slot and secure with two captive screws.

d. The DSP can be connected to any combination of terminals or modems (up to a total of two) by mating one or two male subminiature D, 25-pin RS-232C connectors to front panel female subminiature D connectors. Flat ribbon cable is not recommended because excessive cross-talk can occur on the clock lines, resulting in errors. Figure 2-10 illustrates a typical interface cabling for the DSP.

e. Equipment power may be turned ON.

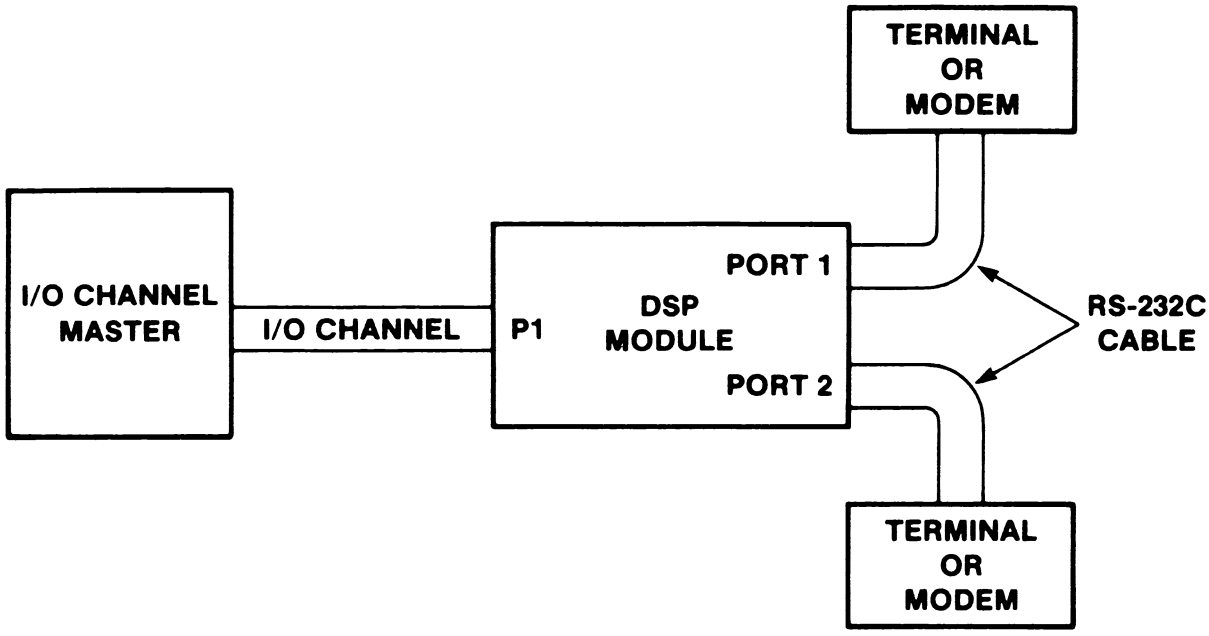


FIGURE 2-10. Typical DSP Interface Cabling Diagram

CHAPTER 3

OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides the necessary information to initialize and operate the Dual RS-232C Serial Port Module in a typical system configuration.

3.2 INDICATOR

The DSP contains one indicator -- a front panel red LED named FAIL. The FAIL LED indicator illuminates when a module failure occurs.

3.3 OPERATING PROCEDURE

The DSP is designed to operate with any RS-232C compatible terminal or modem. Following is a typical procedure showing how to use the DSP to interface with an RS-232C terminal/modem device.

a. Apply power to system equipment.

b. If the I/O Channel master is MVME110, the VMEbug firmware is available for an asynchronous driver for the DSP. (Refer to the VMEbug manual for details.)

c. If the I/O Channel master is VM02, use the downloadable software for an asynchronous driver, or SDLC for the DSP.

d. Figure 3-1 is a typical asynchronous initialization routine for user-generated driver programs. (Refer to the NEC UPD7201 technical manual for further programming information.)

e. Figure 3-2 is the initialization procedure for baud rate selection.

```
                        INITIALIZE THE VERSAmodule-02 SERIAL PORTS

1006 8 0000014A 286A0004          MOVE.L   CCBMEMA(A2),A4      PORT 2 MEMORY MAPPED I/O ADDRESS
1007 8 0000014E 177C00180004      MOVE.B   #$18,CREG(A3)       PORT 1 RESET
1008 8 00000154 197C00180004      MOVE.B   #$18,CREG(A4)       PORT 2 RESET
1009 8 0000015A 177C00020004      MOVE.B   #$02,CREG(A3)       POINT TO CONTROL REGISTER 2-PORT 1
1010 8 00000160 197C00020004      MOVE.B   #$02,CREG(A4)       POINT TO CONTROL REGISTER 2-PORT 2
1011 8 00000166 177C00100004      MOVE.B   #$10,CREG(A3)       BOTH CHANNELS INTERRUPT
1012 8 0000016C 197C00FF0004      MOVE.B   #$FF,CREG(A4)       USE INTERRUPT VECTOR
1013 8 00000172 177C00140004      MOVE.B   #$14,CREG(A3)       POINT TO CONTROL REGISTER 4 PORT 1 & RESET
1014 8 00000178 197C00140004      MOVE.B   #$14,CREG(A4)       POINT TO CONTROL REGISTER 4 PORT 2 & RESET
1015 8 0000017E 177C00440004      MOVE.B   #$44,CREG(A3)       NO PARITY,1 STOP BIT,16X CLOCK RATE-PORT 1
1016 8 00000184 197C00440004      MOVE.B   #$44,CREG(A4)       NO PARITY,1 STOP BIT,16X CLOCK RATE-PORT 2
1017 8 0000018A 177C00030004      MOVE.B   #$03,CREG(A3)       POINT TO CONTROL REGISTER 3 PORT 1
1018 8 00000190 197C00030004      MOVE.B   #$03,CREG(A4)       POINT TO CONTROL REGISTER 3 PORT 2
1019 8 00000196 177C00E00004      MOVE.B   #$E0,CREG(A3)       8 BITS,AUTO-ENABLE,RECEIVER DISABLED-PORT 1
1020 8 0000019C 197C00E00004      MOVE.B   #$E0,CREG(A4)       8 BITS,AUTO-ENABLE,RECEIVER DISABLED-PORT 2
1021 8 000001A2 177C00050004      MOVE.B   #$05,CREG(A3)       POINT TO CONTROL REGISTER 5 PORT 1
1022 8 000001A8 197C00050004      MOVE.B   #$05,CREG(A4)       POINT TO CONTROL REGISTER 5 PORT 2
1023 8 000001AE 177C00E20004      MOVE.B   #$E2,CREG(A3)       8 BITS,TRANSMITTER DISABLED,PORT 1
1024 8 000001B4 197C00E20004      MOVE.B   #$E2,CREG(A4)       8 BITS,TRANSMITTER DISABLED,PORT 2
1025 8 000001BA 177C00110004      MOVE.B   #$11,CREG(A3)       POINT TO CONTROL REGISTER 1 PORT 1
1026 8 000001C0 197C00110004      MOVE.B   #$11,CREG(A4)       POINT TO CONTROL REGISTER 1 PORT 2
1027 8 000001C6 177C001C0004      MOVE.B   #$1C,CREG(A3)       EXT. INTERRUPT & Tx DISABLED,PORT 1
1028 8 000001CC 197C001C0004      MOVE.B   #$1C,CREG(A4)       EXT. INTERRUPT & Tx DISABLED,PORT 2
```

NOTES:

1. A3 = Port 1 Base Address
2. A4 = Port 2 Base Address
3. CREG=4= offset to 7201 control register

FIGURE 3-1. Typical Asynchronous Interrupt 7201 Initialization Procedure

```
 1                00000048      SERFLG   EQU      $48
 2
 3                               ********************************************************************************
 4
 5  0 00000000 4A780048                   TST.W    SERFLG                 IS THE SERIAL I/O CARD IN THE I/O BUS?
 6  0 00000004 673E                       BEQ.S    SKIPO                  IF NOT THEN SKIP INITIALIZATION
 7                               *
 8  0 00000006 207C00FE61C1               MOVE.L   #SERPADDR,A0           POINT TO THE CONTROL PIA OF SERIAL I/O BOARD
 9  0 0000000C 08A800020002               BCLR.B   #2,2(A0)               SETUP TO TALK TO PIA DDRA
10  0 00000012 10BC0018                   MOVE.B   #$18,(A0)              SET 2 OUTPUT BITS (LED AND A/B TOGGLE)
11  0 00000016 117C00040002               MOVE.B   #4,2(A0)               CHANGE TO DATA REGISTER
12  0 0000001C 612C                       BSR.S    SELBAUD                GO FIND BAUD RATE
13  0 0000001E 1200                       MOVE.B   D0,D1                  SAVE B SIDE BAUD RATE
14  0 00000020 08900003                   BCLR.B   #3,(A0)                TOGGLE TO A SIDE BAUD RATE JUMPER
15  0 00000024 6124                       BSR.S    SELBAUD                GO FIND BAUD RATE
16  0 00000026 E908                       LSL.B    #4,D0                  SHIFT TO UPPER PART OF BYTE
17  0 00000028 8200                       OR.B     D0,D1                  PUT A AND B BAUD RATES TOGETHER
18  0 0000002A 08A800020006               BCLR.B   #2,6(A0)               SETUP TO TALK TO PIA DDRB
19  0 00000030 117C00FF0004               MOVE.B   #$FF,4(A0)             SET PIA B TO ALL OUTPUTS
20  0 00000036 117C00040006               MOVE.B   #4,6(A0)               SWITCH TO DATA REGISTER B
21  0 0000003C 11410004                   MOVE.B   D1,4(A0)               LOAD CALCULATED BAUD RATES
22  0 00000040 08900004                   BCLR.B   #4,(A0)                SWITCH OFF THE SERIAL BOARD FAIL LED
23  0 00000044 610000E0      SKIPO        BSR      INITSER                INITIALIZE THE SERIAL PORTS
24  0 00000048 6014                       BRA.S    INITIO
25                               *
26  0 0000004A 1010          SELBAUD      MOVE.B   (A0),D0                GET A SIDE BAUD RATE
27  0 0000004C 02400007                   ANDI.W   #$7,D0                 DROP MS BITS
28  0 00000050 103B0004                   MOVE.B   BAUDTAB(PC,D0.W),D0    SAVE SELECTED BAUD RATE
29  0 00000054 4E75                       RTS
30                               *
31  0 00000056 0F0E0D0C      BAUDTAB      DC.L     $0F0E0D0C
32  0 0000005A 0A070502                   DC.L     $0A070502
33
34                               ********************************************************************************
35
36  0             0000005E     INITIO   EQU      *
37  0             00000126     INITSER  EQU      *+200
38                 00FE61C1     SERPADDR EQU      $FE61C1
39
40                                      END
```

FIGURE 3-2. Baud Rate Selection Initialization Procedure

CHAPTER 4

FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter describes the overall block diagram level descriptions for the Dual RS-232C Serial Port Module. A general description provides an overview of the module, followed by a detailed description of each section of the DSP.

4.2 GENERAL DESCRIPTION

The DSP processes address, data, interrupt, and control signals to expand the resources of an I/O Channel to include two RS-232C serial ports.

The DSP provides two general-purpose, RS-232C serial ports. Figure 4-1 is a block diagram of the DSP. As shown in this figure, the DSP has a common I/O Channel interface section and two serial port sections. Each of the serial port sections consists of a 7201 multiprotocol serial controller and RS-232C drivers and receivers. One PIA to control baud rate and modem control lines DSR and RI is provided.

4.3 I/O CHANNEL INTERFACE

The I/O Channel interface brings the I/O Channel address, data, interrupt, and control signals onto the DSP module. Of the 12 input address lines, A4-A7 are routed to a comparator that compares these four address bits to the I/O Channel base address selected by jumpers on header J6. A8-A11 also are routed to the comparator, and are hardwired to be a logic level zero for an address match. This address match produces a select signal that is synchronized with a free-running, 2-MHz clock which, along with strobe (STB*), produces a chip select signal to the PIA and 7201. A0 and A1 are used as address inputs to the PIA and 7201. A2 is used to select either the PIA or the 7201 (a high logic level selects the 7201). A3 is not used by the DSP. A transmit acknowledge (XACK) signal is generated 625 nsec after the chip select to allow time for the devices to complete the cycle. Read data, write (WT*), A0, A1, and chip select signals are latched for the PIA. Data is not latched during a write cycle. The control lines used are clock (CLK), I/O reset (IORES*), STB*, and WT*. One interrupt signal from the 7201 and two from the PIA may be jumpered at header J5 to any of the four P1 interrupt output pins for transfer to a bus master. Refer to the Input/Output Channel Specification Manual, M68RIOCS, for additional I/O Channel information, including signal timing diagrams. Figure 4-2 shows possible address locations for the DSP in the I/O Channel memory map.

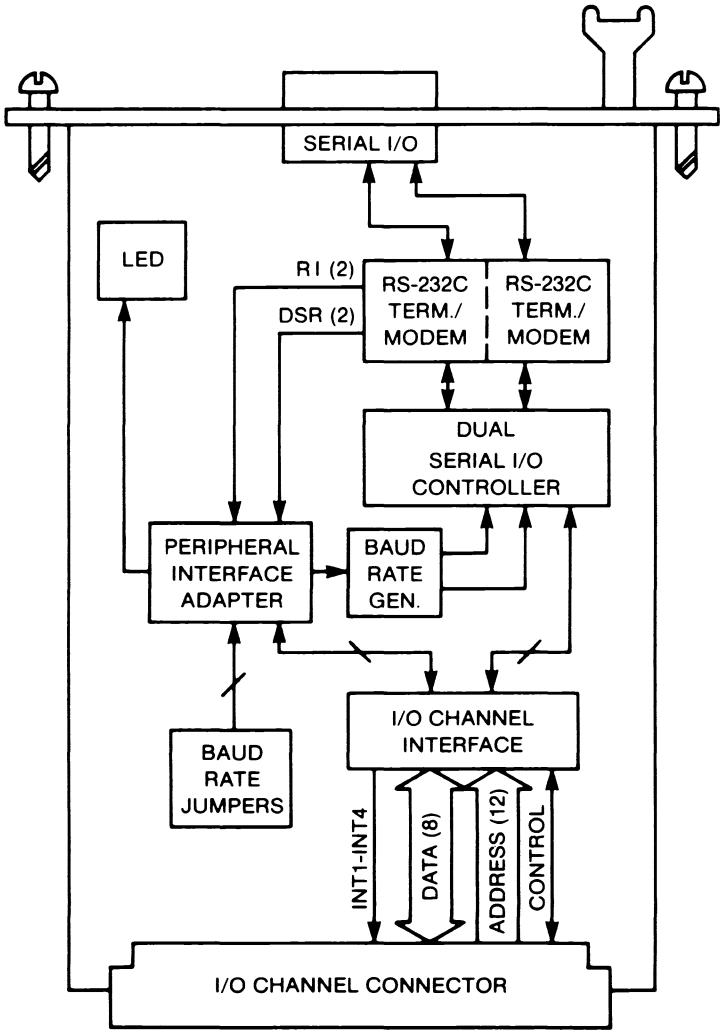


FIGURE 4-1. DSP Block Diagram

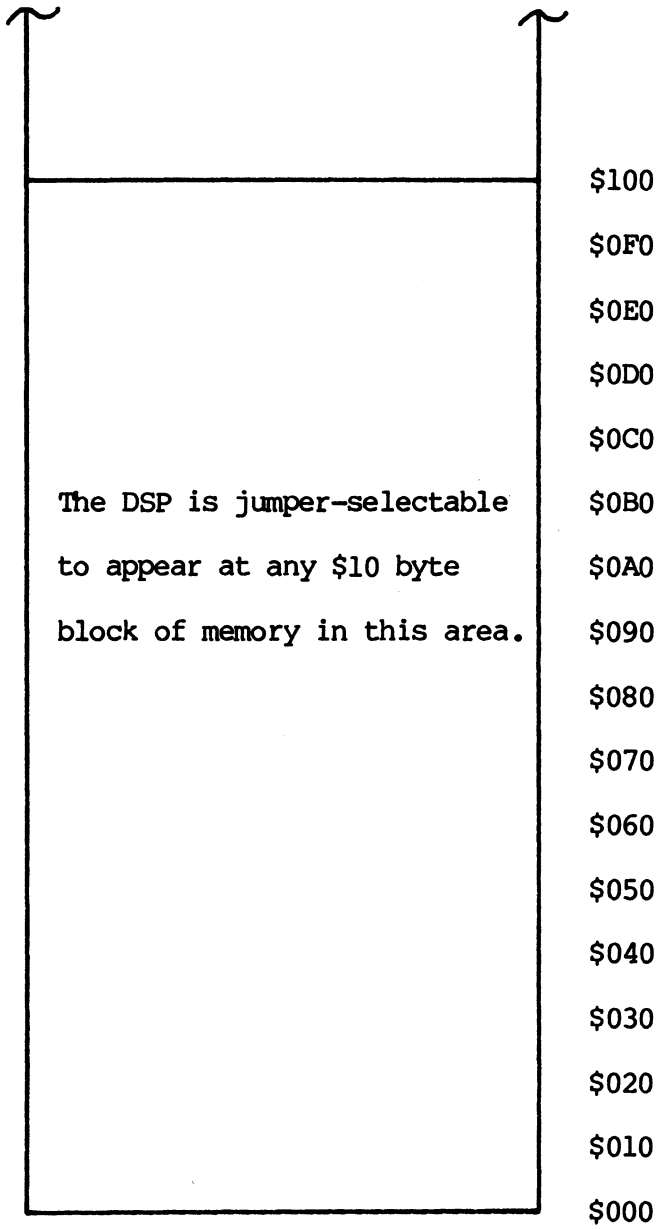


FIGURE 4-2. I/O Channel Memory Map

The DSP uses 16 I/O Channel addresses (lines A4-A7), half of which are redundant. The I/O Channel address functions are listed in Table 4-1, where "X" represents a jumper-selectable base address at header J6.

TABLE 4-1. I/O Channel Address Functions

I/O CHANNEL ADDRESS	REGISTER
0X0	PIA Peripheral A/DDRA
0X1	PIA Control A
0X2	PIA Peripheral B/DDRB
0X3	PIA Control B
0X4	7201 Data A
0X5	7201 Data B
0X6	7201 Control A
0X7	7201 Control B
0X8	PIA Peripheral A/DDRA
0X9	PIA Control A
0XA	PIA Peripheral B/DDRB
0XB	PIA Control B
0XC	7201 Data A
0XD	7201 Data B
0XE	7201 Control A
0XF	7201 Control B

The address that the bus master processor (i.e., VM02 MC68000) senses at the I/O Channel can be determined by multiplying the I/O Channel address (Table 4-1) by 2, and adding it to the I/O Channel memory mapped address. For example, the I/O Channel memory mapped address for the VM02 is F80001. The PIA control register A on the DSP has an I/O Channel address of 0X1. Let "X", the base address, be 0. Thus, the VM02 sees the PIA control register A at F80001 + 2 x (001) = F80003.

4.4 7201 DUAL SERIAL I/O CONTROLLER

The 7201 is a full duplex parallel-to-serial, serial-to-parallel converter/ controller. The unit features multiprotocol control, including asynchronous, bisynchronous, SDLC, and HDLC. Modem control signals include RTS, CTS, DCD, and DTR. Refer to the UPD 7201 technical manual for additional information.

4.5 PERIPHERAL INTERFACE ADAPTER

The PIA supports the modem control lines Data Set Ready (DSR) and Ring Indicator (RI) that are provided on both RS-232C channels and go to CA1, CA2, CB1, and CB2 inputs of the PIA. Complete PIA pin functions are listed in Table 4-2 and are presented as programming aids. Transitions on CA1, CA2, CB1, and CB2 cause interrupts that indicate a change of state of DSR and RI of either channel. In addition, both DSR's are connected to readable bits on the PIA. Another function of the PIA is to provide software baud rate control.

TABLE 4-2. PIA Input/Output Functions

PIA PIN	INPUT/OUTPUT	FUNCTION
CA1	Input	DSR port 1
CA2	Input	RI port 1
PA0-PA2	Input	Baud rate jumpers J10
PA3	Output	Select for port 1 or 2 baud rate jumpers 0 = port 1 1 = port 2
PA4	Output	Control of FAIL LED 1 = LED on 0 = LED off
PA5	Input	FAIL LED status 1 = LED on 0 = LED off
PA6	Input	DSR port 1
PA7	Input	DSR port 2
PB0-3	Output	Baud rate control - port 2 (1)
PB4-7	Output	Baud rate control - port 1 (1)
CB1	Input	DSR port 2
CB2	Input	RI port 2

NOTES:

(1) See Table 4-3.

2. Ports 1 and 2 refer to RS-232C connectors.

4.6 BAUD RATE GENERATION

Baud rate generator U5 (K1135B) contains two sections, each of which is capable of being programmed to generate any of 16 different baud rates. One of the two outputs is connected to J3 and J4, which are the internal/external clock headers for port 2. The other output is connected to J12 and J13 port 1 internal/external clock headers. Both of these headers provide a variety of optional baud rate configurations. With the jumpers installed for the factory configuration, each section of the baud rate generator provides both Tx and Rx internal clocking for the applicable port.

Outputs from the PIA control the baud rate generator to select one of eight jumper-selectable (with proper software in operation) or 16 software-selectable baud rates. When using VMEbug or custom software, during the reset operation inputs to the PIA from the baud rate jumpers are read, and then the appropriate baud rate control is activated. Software, however, has priority over the hardware jumpers and, at the user's discretion, a different code can be initiated to the baud rate generator. Thus, both hardware and software control of baud rates is allowed. The eight hardware and 16 software baud rates are listed in Table 4-3. The user may also supply an external transmit/receive clock signal. In this case, the baud rate is determined by the user.

TABLE 4-3. Baud Rate Control Code

PIA OUTPUTS					ASYNCHRONOUS BAUD RATES	SYNCHRONOUS BAUD RATES
PB3 (PB7)	PB2 (PB6)	PB1 (PB5)	PB0 (PB4)	Port 2 Port 1		
0	0	0	0		50	800
0	0	0	1		75	1200
0	0	1	0		110 (1)	1760 (1)
0	0	1	1		134.5	2152
0	1	0	0		150	2400
0	1	0	1		300 (1)	4800 (1)
0	1	1	0		600	9600
0	1	1	1		1200 (1)	19200 (1)
1	0	0	0		1800	28800
1	0	0	1		2000	32000
1	0	1	0		2400 (1)	38400 (1)
1	0	1	1		3600	57600
1	1	0	0		4800 (1)	76800 (1)
1	1	0	1		7200 (1)	115200 (1)
1	1	1	0		9600 (1)	153600 (1)
1	1	1	1		19200 (1)	307200 (1)

NOTE: (1) Jumper-selectable baud rates.

4.7 BAUD RATE SELECTION

The baud rates for the two ports can be independently controlled by the Peripheral Interface Adapter (PIA) U14 (MC68B21) and its associated software. The PIA contains two sections. Section B is connected to the programmable baud rate generator U5 (K1135B). Table 4-3 lists the baud rates selected vs the PIA control codes. Section A of the PIA is connected to J10, the baud rate select header, through the port select buffer U13. Table 2-5 lists the eight jumper-selectable baud rates.

If the DSP module is used in a VME system with VMEbug, the baud rate selection routine is provided by VMEbug as shown in Figure 3-2, and the installed jumpers will select the baud rates. This routine sequentially reads the J10 jumper configurations for port 2 and then port 1, as controlled by PIA output bit PA3 and buffer U13. These bit patterns are used to access a baud rate lookup table. This baud rate table data is then output as an 8-bit control code to the baud rate generator U5.

If the DSP module is used in a VMC system, the software driver is provided in the VERSAdos operating system program to program U12 (UPD7201) serial controller and set the baud rate. Normally the baud rate is sysgened for 9600 baud but can be changed via display console using the technique as described in the VERSAdos Data Management Services and Program Loader, User's Manual-VMC, Motorola publication number RMS68KIO. Refer to the CONFIGURATION PARAMETERS (Terminal-Configuration Parameter Block - baud rate code) portion of text.

4.8 MALFUNCTION DETECTION

The FAIL LED illuminates when a malfunction is detected in the DSP. After verifying proper operation of the 7201 and the PIA, the I/O Channel master processor turns the FAIL LED off by a write instruction to the PIA.

4.9 RS-232C TERMINAL/MODEM

The RS-232C interface consists of MC1488 drivers and MC1489 receivers that are configured for either "to terminal" or "to modem" operation with jumpers provided. Units are shipped from the factory in the " to terminal" configuration --i.e., with jumpers installed on headers J9 and J15 (see Figure 2-7). The terminal/modem sends and receives serial data and control signals to and from peripheral equipment as directed by the dual serial I/O controller.

4.10 MODULE I/O TIMING

Table 4-4 and Figure 4-3 show the performance characteristics of the DSP from the I/O Channel side. All data transfers on the I/O Channel are between the master and a slave (such as the DSP), and are initiated by the master. All data transfers are asynchronous and rely on two interlocked signal lines -- STB* and XACK*. STB* is generated by the master and initiates a data transfer. XACK* is generated by the addressed slave to indicate that the data transfer has been accomplished.

TABLE 4-4. I/O Channel Timing Signal Characteristics

TIMING PARAMETER		VALUE IN NANOSECONDS	
NUMBER	DESCRIPTION	TYPICAL	MAX
1	STB* low to XACK* low	990	1300
2	STB* high to XACK* low	122	184

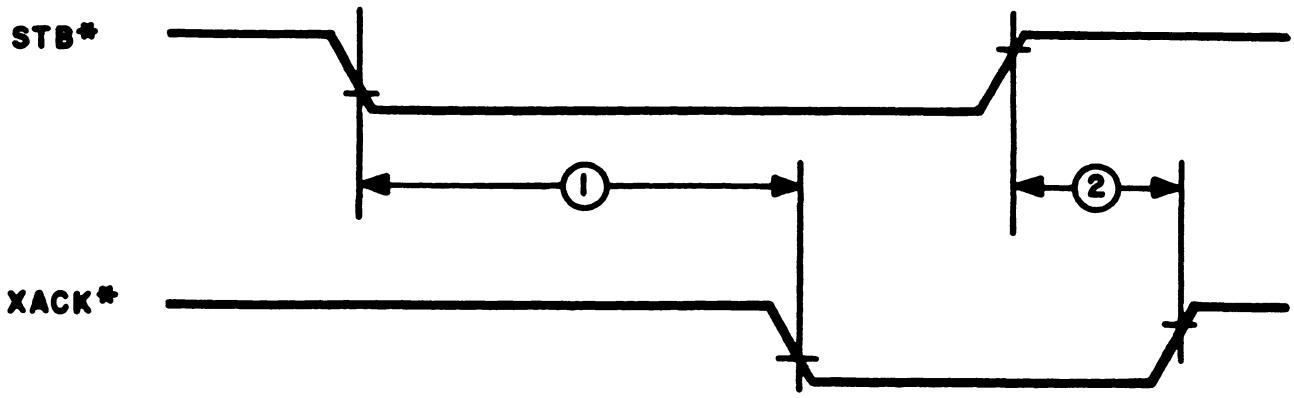


FIGURE 4-3. I/O Channel Timing Signal Diagram

CHAPTER 5

SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the connector signal descriptions, parts list and associated parts location diagram, and a schematic diagram for the Dual RS-232C Serial Port Module.

5.2 CONNECTOR SIGNAL DESCRIPTIONS

The DSP has three interface connectors -- one to connect it to the I/O Channel and two to connect it to terminals or modems.

5.2.1 I/O Channel Connector

I/O Channel connector P1 on the DSP is a standard DIN 41612 triple-row, 64-pin male connector. The back panel ribbon cable uses the female connector. Table 5-1 lists the P1 pin assignments. Additional information can be found in the I/O Channel Specification.

5.2.2 Peripheral Connectors

Front panel peripheral connectors (ports 1 and 2) are female subminiature D 25-pin connectors. Both front panel connectors are connected to module connector J1 via flat ribbon cables. Table 5-2 lists the RS-232C front panel connector pin assignments and the module J1 connector pin assignments by signal mnemonic and signal name and description.

5.3 PARTS LIST

Table 5-3 lists the components of the DSP. A parts location diagram is provided in Figure 5-1. This list reflects the latest issue of DSP hardware.

5.4 DIAGRAMS

Figure 5-2 is the schematic diagram of the DSP.

TABLE 5-1. I/O Connector P1 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A10, A17-A19, A24,A25, A31,A32, C11,C20, C25,C31, C32	GND	GROUND
A11	A11	ADDRESS bus (bit 11) - One of 11 input signals used to selectively access the DSP.
A12	A10	ADDRESS bus (bit 10) - Same as bit A11 on pin A11.
A13	A8	ADDRESS bus (bit 8) - Same as bit A11 on pin A11.
A14	A6	ADDRESS bus (bit 6) - Same as bit A11 on pin A11.
A15	A4	ADDRESS bus (bit 4) - Same as bit A11 on pin A11.
A16	A2	ADDRESS bus (bit 2) - Same as bit A11 on pin A11.
A20	D7	DATA bus (bit 7) - Bidirectional signal used to transmit data between the I/O Channel master and the DSP.
A21	D6	DATA bus (bit 6) - Same as bit D7 on pin A20.
A22	D4	DATA bus (bit 4) - Same as bit D7 on pin A20.
A23	D2	DATA bus (bit 2) - Same as bit D7 on pin A20.
A26,C26	-12V	-12 Vdc Power - Used by the module logic circuits.
A27, C8-C10, C27	(Reserved)	N/A
A28,C28	+12V	+12 Vdc Power - Used by the module logic circuits.
A29,A30, C29,C30	+5V	+5 Vdc Power - Used by the module logic circuits.
C1	INT4*	INTERRUPT REQUEST 4 - One of four active low output signal lines used by the DSP to interrupt the I/O Channel master.
C2	INT3*	INTERRUPT REQUEST 3 - Same as signal INT4* on pin C1.
C3	INT2*	INTERRUPT REQUEST 2 - Same as signal INT4* on pin C1.
C4	INT1*	INTERRUPT REQUEST 1 - Same as signal INT4* on pin C1.

TABLE 5-1. I/O Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C5	IORES*	INPUT/OUTPUT RESET - Active low input signal used to reset the DSP.
C6	XACK*	TRANSMIT ACKNOWLEDGE - Active low output signal used to advise the I/O Channel master that write data is latched and read data is available.
C7	CLK	CLOCK - Free-running input signal used by the DSP for internal synchronization and timing.
C12	A9	ADDRESS bus (bit 9) - Same as bit A11 on pin A11.
C13	A7	ADDRESS bus (bit 7) - Same as bit A11 on pin A11.
C14	A5	ADDRESS bus (bit 5) - Same as bit A11 on pin A11.
C15	A3	ADDRESS bus (bit 3) - Not used.
C16	A1	ADDRESS bus (bit 1) - Same as bit A11 on pin A11.
C17	A0	ADDRESS bus (bit 0) - Same as bit A11 on pin A11.
C18	STB*	STROBE - An input signal. A high to low transition starts the I/O Channel cycle. A low to high transition ends the cycle.
C19	WT*	WRITE - An input signal that is low when the I/O Channel is in the write cycle, and high when the I/O Channel is in the read cycle.
C21	D5	DATA bus (bit 5) - Same as bit D7 on pin A20.
C22	D3	DATA bus (bit 3) - Same as bit D7 on pin A20.
C23	D1	DATA bus (bit 1) - Same as bit D7 on pin A20.
C24	D0	DATA bus (bit 0) - Same as bit D7 on pin A20.

NOTE: When a 50-pin ribbon cable is used, the 14 power lines (A27-A32 and C27-C32) are not connected by the cable. Power to the device interfacing with the I/O Channel must be supplied by alternate means.

TABLE 5-2. DSP RS-232C Connector Pin Assignments

FRONT PANEL PORTS 1 & 2 PIN NUMBER	MODULE J1 PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
2	3,28	TxD	TRANSMITTED DATA - Serial binary data output.
3	5,30	RxD	RECEIVED DATA - Serial binary data input.
4	7,32	RTS	REQUEST TO SEND - A signal denoting terminal has data to send.
5	9,34	CTS	CLEAR TO SEND - A signal that indicates the terminal can transmit data.
6	11,36	DSR	DATA SET READY - A signal denoting the modem is ready (off the hook).
7	13,38	SIG GND	SIGNAL GROUND
8	15,40	DCD	DATA CARRIER DETECT - A signal that indicates to the terminal that a carrier is present.
15	4,29	TxC	TRANSMITTER CLOCK - (DCE Source) A signal that provides timing information for transmitted data.
17	8,33	RxC	RECEIVER CLOCK - A signal that provides timing information for received data.
20	14,39	DTR	DATA TERMINAL READY - A signal that denotes the terminal is ready to transmit or receive data.
22	18,43	RI	RING INDICATOR - A signal to DTE that denotes the modem is receiving a ringing signal.
24	22,47	TxC	TRANSMITTER CLOCK - (DTE Source) A signal that provides timing information for transmitted data.

TABLE 5-3. DSP Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8123B01	Printed wiring board
C1-C11,C12-C18	21SW992C025	Capacitor, ceramic, .1 uF @ 50 Vdc
C19, C20	23NW9618A33	Capacitor, electrolytic, 22 uF @ 25 Vdc
J1	28NW9802D97	Connector, right angle, 50-pin
J2, J11	28NW9802D04	Header, single-row post, 3-pin
J3,J4,J10, J12, J13	28NW9802C63	Header, double-row post, 12-pin
J5,J8,J9, J14,J15	28NW9802B62	Header, double-row post, 20-pin
J6,J7,J16	28NW9802C43	Header, double-row post, 8-pin
P1	28NW9802E05	Connector, 64-pin
R1	06SW-124A28	Resistor, fixed, film, 130 ohm, 5%, 1/4 W
R2,R9,R10	51NW9626A37	Resistor network, 9/10k ohm
R3,R7	51NW9626A95	Resistor network, 7/47k ohm
R4	51NW9626A41	Resistor network, 9/4.7k ohm
R5,R6,R8	06SW-124A65	Resistor, fixed, film, 4.7k ohm, 5%, 1/4 W
U1,U10,U18,U20	51NW9615B30	I.C. MC1489AL
U2,U4	51NW9615C24	I.C. SN74LS32N
U3	51NW9615G38	I.C. SN74LS38N
U5	48AW1019B01	K1135 dual baud rate generator
U6	51NW9615H93	I.C. SN74LS641N
U7	51NW9615H92	I.C. N74LS112N
U8	51NW9615F41	I.C. DM74LS164N
U9	51NW9615H41	I.C. SN74LS682N
U11,U19,U21	51NW9615B29	I.C. MC1488L
U12	51NW9615H44	I.C. UPD7201C

TABLE 5-3. DSP Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U13	51NW9615F46	I.C. 74LS241N
U14	51NW9615D85	I.C. MC68B21P
U15	51NW9615G12	I.C. SN74LS375N
U16	51NW9615C56	I.C. SN74S08N
U17	51NW9615E93	I.C. SN74LS14N
U23	51NW9615E98	I.C. SN74LS373N
U24	51NW9615F02	I.C. 74LS244N
	09NW9811A09	Socket, I.C. DIL, 18-pin (use at U5)
	09NW9811A22	Socket, I.C. DIL, 40-pin (use at U12, U14)
	28NW9802E76	Connector, flat cable, 25-pin
	29NW9805B17	Jumper, shorting insulated (use at J2, J4-J7, J9-J11, J13, J15, J16)
	47NW9405A27	Jackpost assembly, D-subminiature
	48NW9612A34	Indicator light, red, 5 Vdc (use at E1, E2)

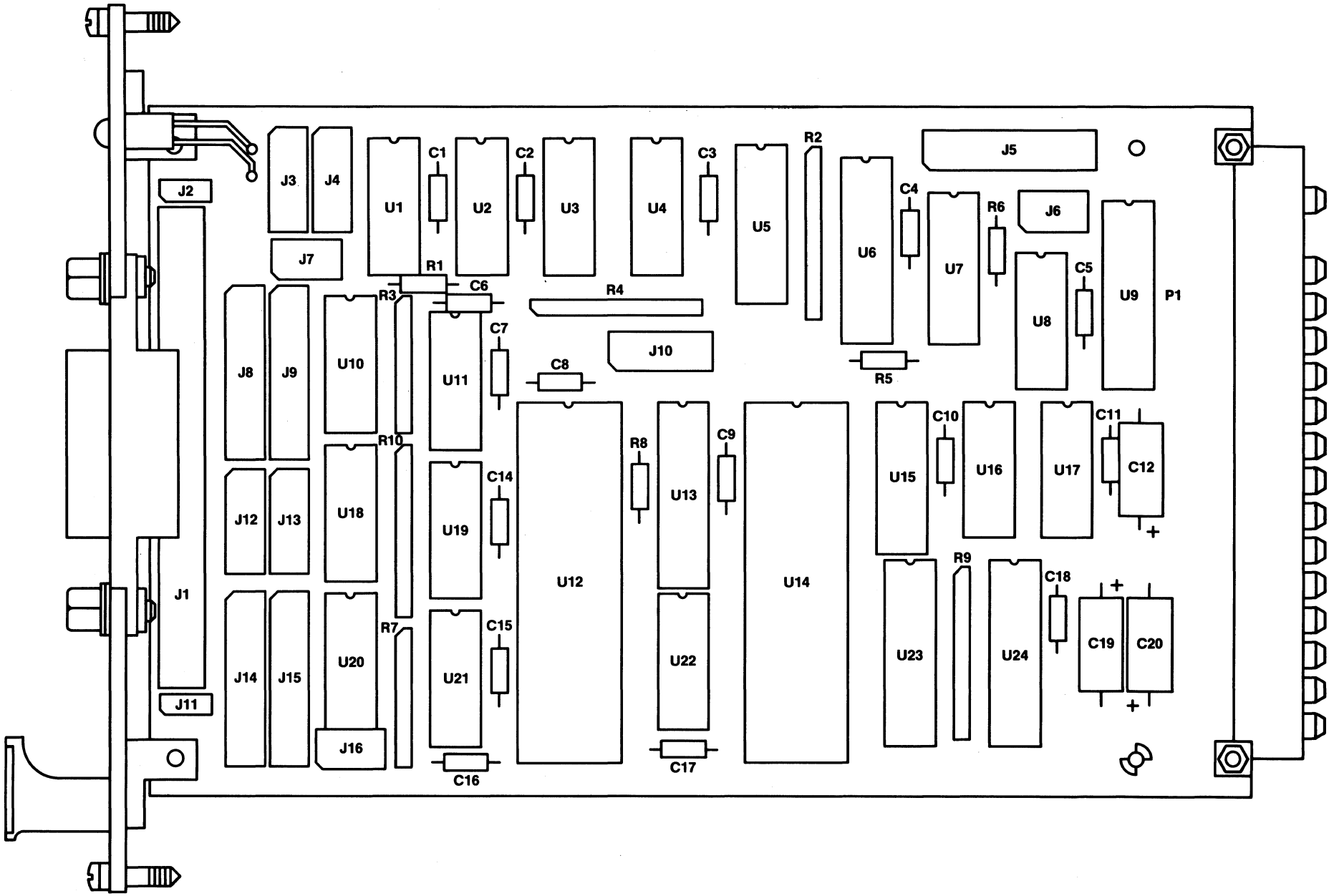


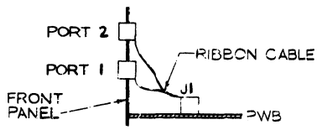
FIGURE 5-1. DSP Module Parts Location Diagram

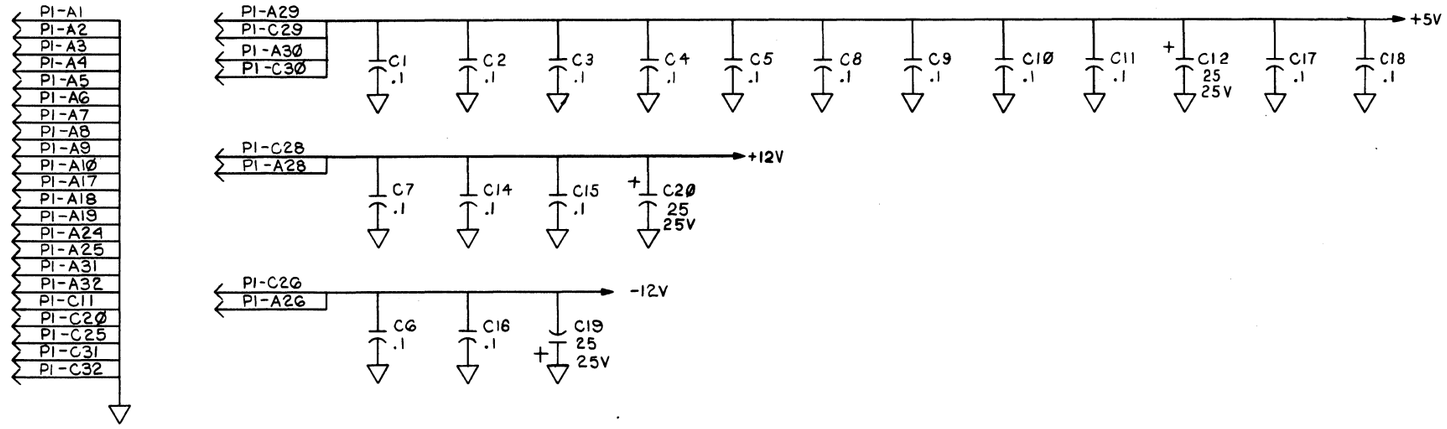
NOTES:

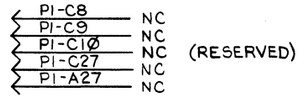
1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3123B01.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ± 5PCT 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES - ACTIVE LOW SIGNAL.
   [ ] DENOTES - ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
7. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING. FOR FULL PART TYPE, REFER TO TABLE I.

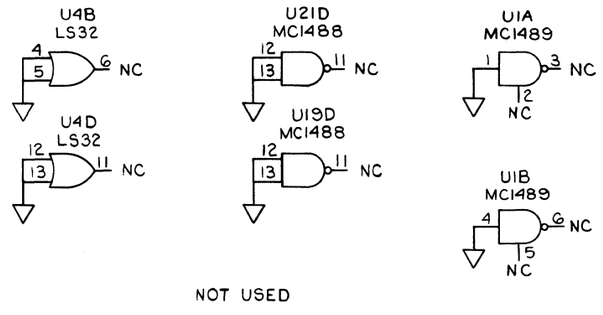
(2) DENOTES PWB HEADER CONNECTOR.

(3) DENOTES FRONT PANEL CONNECTOR.









7 TABLE I

REF DES	TYPE (4)	GND	+5V	-12V	+12V
U1	MC1489	7	14		
U2	74LS32	7	14		
U3	74LS38	7	14		
U4	74LS32	7	14		
U5	K1135B	11	2		
U6	74LSG41	10	20		
U7	74LS112	8	16		
U8	74LS1G4	7	14		
U9	74LSG82	10	20		
U10	MC1489	7	14		
U11	MC1488	7		1	14
U12	UPD72001	20	40		
U13	74LS241	10	20		
U14	MCG8B21	1	20		
U15	74LS375	8	16		
U16	74S08	7	14		
U17	74LS14	7	14		
U18	MC1489	7	14		
U19	MC1488	7		1	14
U20	MC1489	7	14		
U21	MC1488	7		1	14
U22	SPARE	7	14		
U23	74LS373	10	20		
U24	74LS244	10	20		

U24	U22
R10	
DS1	
C22	
HIGHEST NUMBER USED	NOT USED
REFERENCE DESIGNATIONS	

63EW3123B REV E SH 1 OF 3

FIGURE 5-2. DSP Module Schematic Diagram (Sheet 1 of 3)

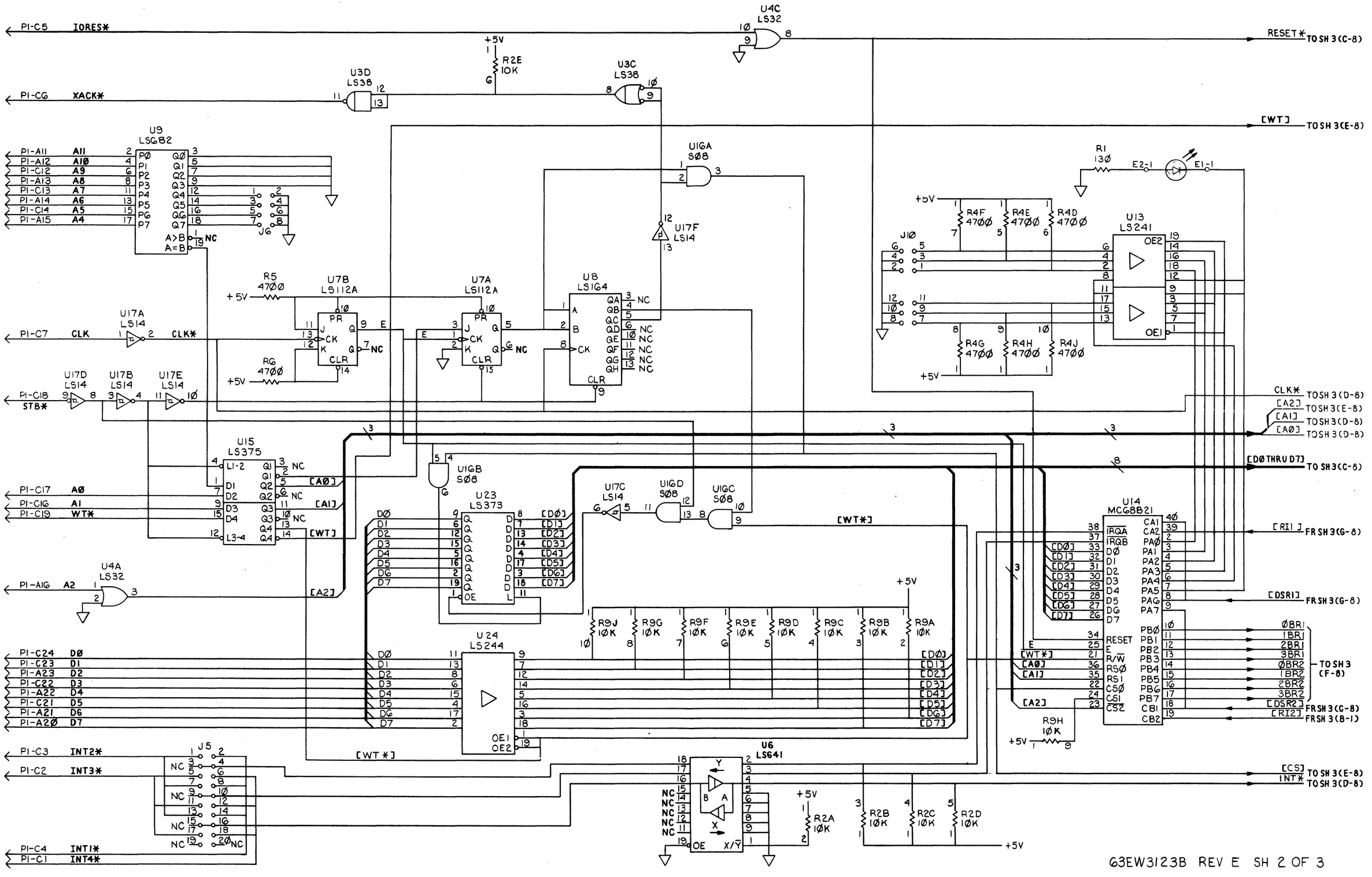


FIGURE 5-2. DSP Module Schematic Diagram (Sheet 2 of 3)

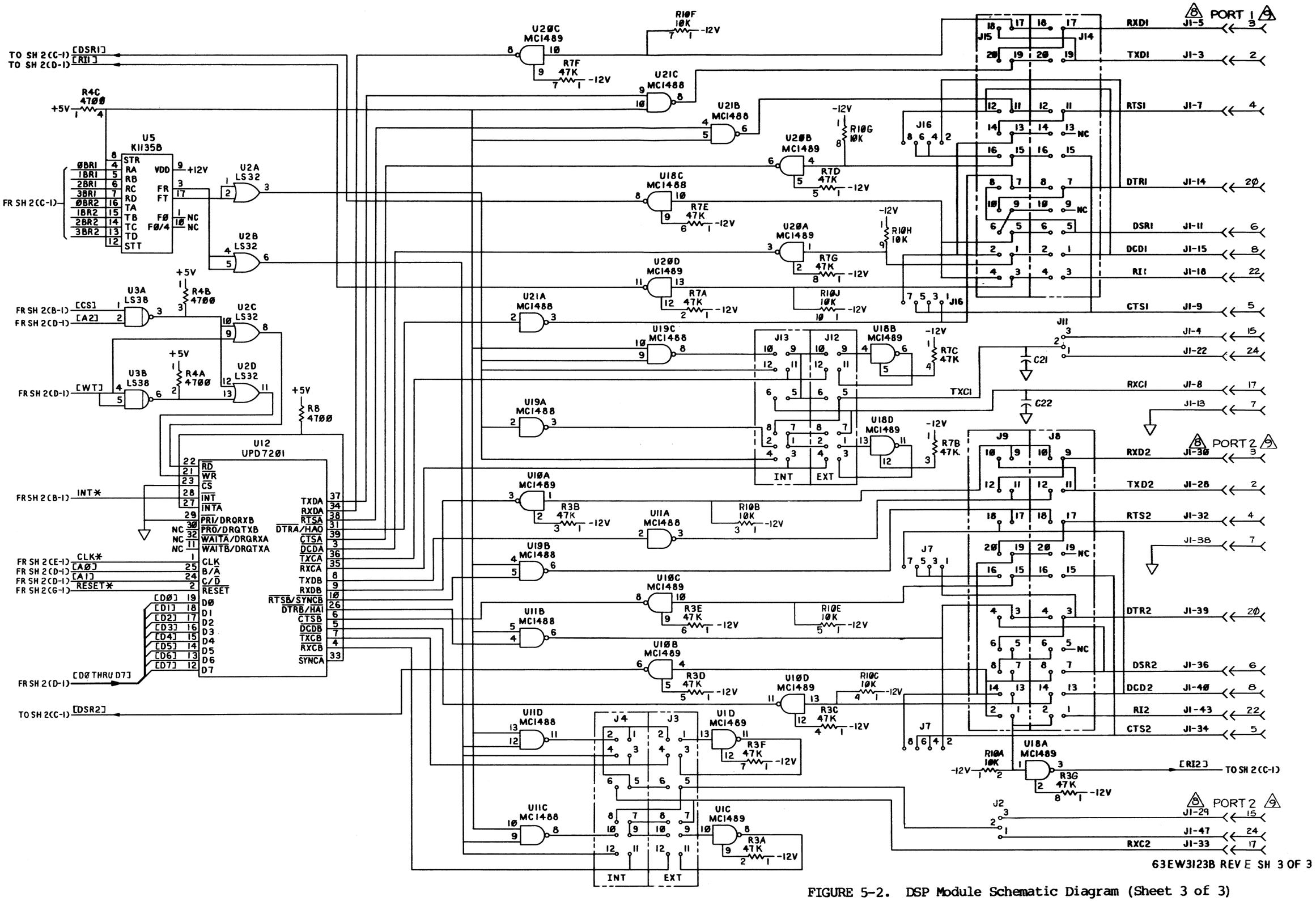


FIGURE 5-2. DSP Module Schematic Diagram (Sheet 3 of 3)

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