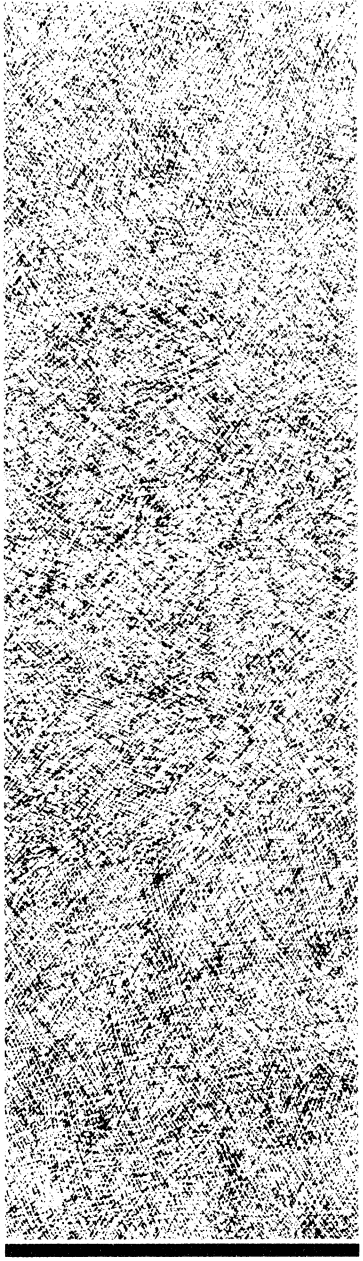
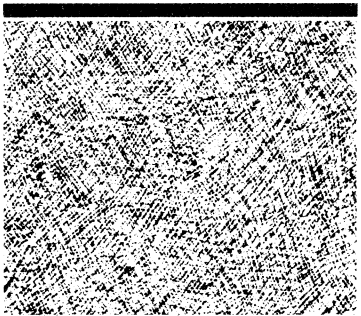


MOTOROLA



MVME236/D2

MVME236
DRAM Memory Modules
User's Manual

MVME236
DRAM Memory Modules
User's Manual
(MVME236/D2)

NOTICE

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Motorola, Inc.
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Tempe, Arizona 85282

PREFACE

This manual provides general information, hardware preparation, installation instructions, and functional description for the MVME236-1, MVME236-2, and MVME236-3 DRAM Memory Modules.

This manual is intended for anyone who wants to design OEM systems, supply additional capability to an existing compatible system, or in a lab environment for experimental purposes.

A basic knowledge of computers, and digital logic is assumed.

To use this manual, you should be familiar with the publications listed in the *Related Documentation* paragraph in Chapter 1 of this manual.

June 1991

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment.
Use extreme caution when handling, testing, and adjusting.

(3/91)

CONTENTS

FIGURES

TABLES

CHAPTER 1
GENERAL INFORMATION

Introduction

This manual provides general information, preparation for use and installation instructions, and functional description for the MVME236 series of VMEbus memory modules (referred to as the MVME236 throughout this manual).

Model Designations

The MVME236 is available in three configurations which are summarized in the following table. The main difference between the versions is memory size.

MVME236 Model Designations

Model Number	Memory Size
MVME236-1	4Mb
MVME236-2	8Mb
MVME236-3	16Mb

Features

The features of the MVME236 include:

- Memory capacity consists of 4Mb, 8Mb or 16Mb using 1-megabit DRAM ZIP packages.
- Standard VMEbus interface with 16-/24-/32-bit address selection and 16-/32-bit data.
- Longword (32-bit), word (16-bit), and byte (8-bit) data transfers.
- Memory base address is switch-selectable on any 1Mb boundary throughout the VMEbus address space.
- Error protection: parity is provided on a byte basis.
- Control and status register: control over parity and error status reporting.

- Fast write: provides early DTACK on a write access.

Specifications

Specifications for the MVME236 are shown in Table 1-1.

Table 1-1. MVME236 Specifications

Characteristics	Specifications
Data transfer size	8-, 16-, and 32-bit
Error detection	Odd byte parity
Data input/output	16-/32-bit VMEbus
Input address	16-/24-/32-bit VMEbus
Power requirements	+4.75 to 5.25 Vdc at 5 A maximum (3.9 A typical)
Relative humidity	5% to 95% (non-condensing)
Operating Temperature	0° C to 50° C inlet air temperature with forced air cooling.
Storage Temperature	-40° C to 85° C
Physical characteristics	(excluding front panel)
Height	9.187 inches (233.35 mm)
Depth	6.299 inches (160.00 mm)
Thickness	0.063 inches (1.6 mm)

General Description

The MVME236 module is a high performance dynamic memory module. The module is available in three memory sizes: the MVME236-1 with a 4Mb memory array (36 ZIP packages), MVME236-2 with an 8Mb memory array (72 ZIP packages), and the MVME236-3 with a 16Mb memory array (144 ZIP packages). The MVME236 receives 16-, 24-, or 32-bit addresses and 16- or 32-bit data through its VMEbus interface. The module supports longword (32-bit), word (16-bit), and byte (8-bit) data transfers. The memory base address can be mapped to start on any 1Mb boundary throughout the VMEbus address space. The MVME236 uses an advanced arbitration method which hides the arbitration time for the next cycle in the current cycle and thus increases throughput.

FCC Compliance

This VMEmodule (MVME236) was tested in an FCC-compliant chassis, and meets the requirements for Class A equipment. FCC compliance was achieved under the following conditions:

1. Shielded cables on all external I/O ports.
2. Cable shields connected to earth ground via metal shell connectors bonded to a conductive module front panel.
3. Conductive chassis rails connected to earth ground. This provides the path for connecting shields to earth ground.
4. Front panel screws properly tightened.

For minimum RF emissions, it is essential that the conditions above be implemented; failure to do so could compromise the FCC compliance of the equipment containing the module.

Related Documentation

The following publications are applicable to the MVME236 and may provide additional helpful information. If not shipped with this product, they may be purchased from the Motorola Literature Distribution Center, 616 West 24th Street, Tempe, AZ 85282; telephone (602) 994-6561. Non-Motorola documents may be obtained from the sources listed.

Document Title	Motorola Publication Number
MVME236 DRAM Memory Modules Support Information(Refer to the *Support Information* section in this chapter)	SIMVME236

NOTE: Although not shown in the above list, each Motorola Computer Group manual publication number is suffixed with characters which represent the revision level of the document, such as /D2 (the second revision of a manual); each supplement bears the same number as the manual but has a suffix such as /A1 (the first supplement to the manual).

The following publications are available from the sources indicated.

ANSI/IEEE Std 1014-1987 Versatile Backplane Bus: The Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, NY 10017, USA. (VMEbus specification)

Support Information

The SIMVME236 manual contains the connector interconnect signal information, parts list, and the schematics for the module.

This manual may be obtained free of charge from Motorola Literature Distribution Center, 616 W. 24th Street, Tempe, AZ 85282; telephone (602) 994-6561.

Manual Terminology

Throughout this manual, a convention has been maintained whereby data and address parameters are preceded by a character which specifies the numeric format as follows:

$	dollar	specifies a hexadecimal number
%	percent	specifies a binary number
&	ampersand	specifies a decimal number

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on high to low transition.

In this manual, assertion and negation are used to specify forcing a signal to a particular state. In particular, assertion and assert refer to a signal that is active or true; negation and negate indicate a signal that is inactive or false. These terms are used independently of the voltage level (high or low) that they represent.

CHAPTER 2
HARDWARE PREPARATION AND INSTALLATION

Introduction

This chapter provides unpacking instructions, hardware preparation, and installation instructions for the MVME236.

Unpacking Instructions

NOTE

If the carton is damaged upon receipt, request carrier's agent be present during unpacking/ inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing and reshipping of equipment.

Hardware Preparation

To select the desired configuration and ensure proper operation of the MVME236, certain modifications may be made before installation. These changes are made through jumper arrangements on the headers. The location of the headers, switches, LEDs, and connectors on the MVME236 is illustrated in Figure 2-1. The module has been factory tested and is shipped with factory-installed jumper configurations that are described in the following sections with each header description. The module is operational with factory-installed jumper configurations. The module is configured to provide the system functions required for a VMEbus system.

Four DIP-type switches (S1, S2, S3, and S4) are located on the MVME236 module. Switches S1/S2 and S3/S4 are used to select the VMEbus address map and the CSR address map, respectively.

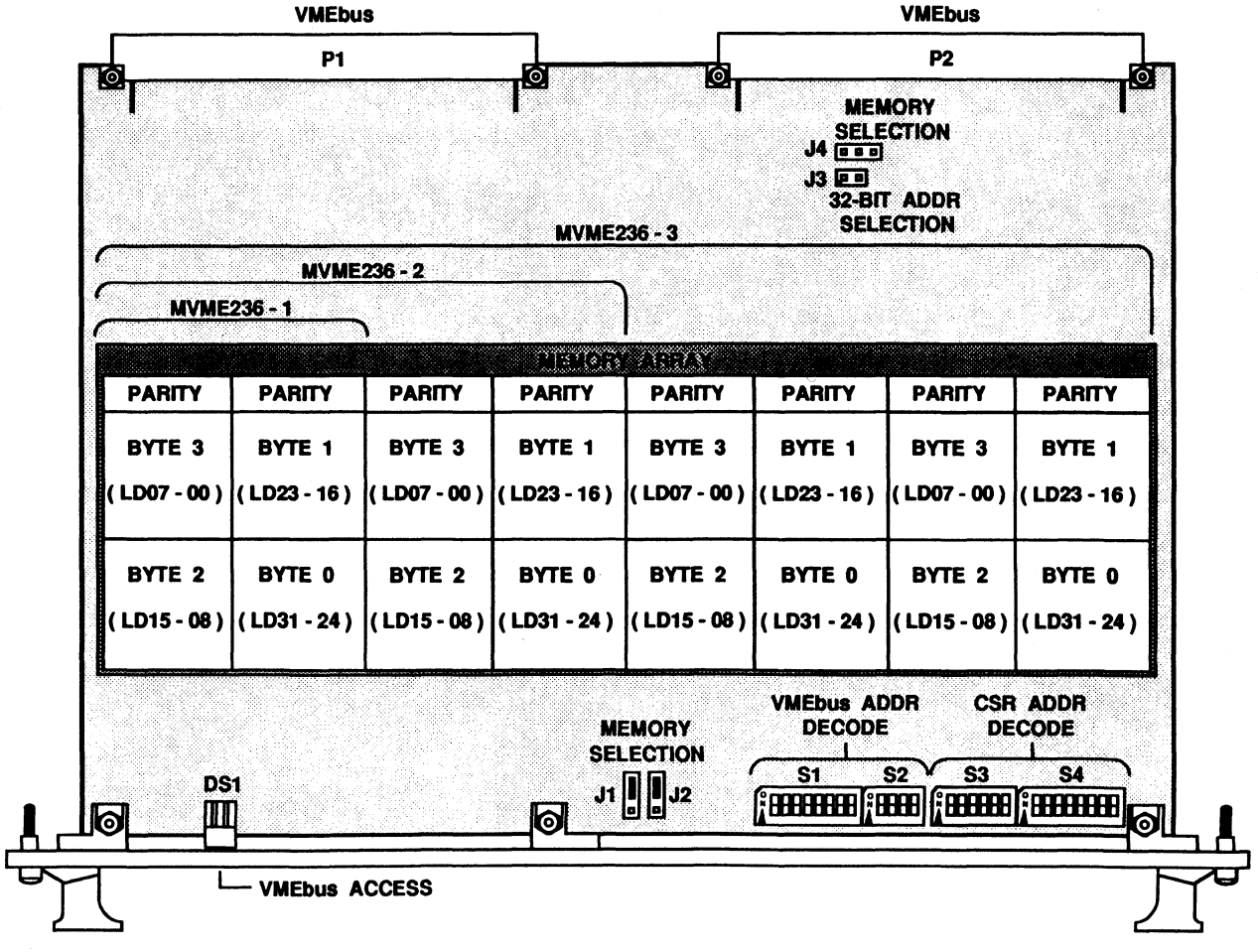
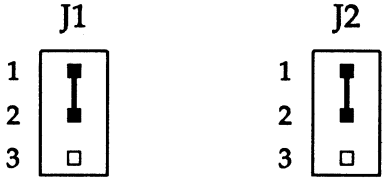


Figure 2-1. MVME236 Header Locations

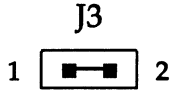
Factory Use Only Headers (J1, J2)

Headers J1 and J2 are for factory use only. A shorting staple is soldered between pins 1 and 2 on all versions of the MVME236.

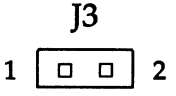


Address Bit Selection (J3)

Header J3 determines the address bit selection. With no jumper installed, 24- or 32-bit addressing is allowed. With a jumper installed between pins 1-2, 24-bit address modifiers are not decoded and the module does not respond to 24-bit addresses.



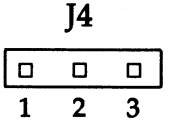
No 24-bit addressing
(Factory Setting)



24- or 32-bit addressing

Factory Use Only Header (J4)

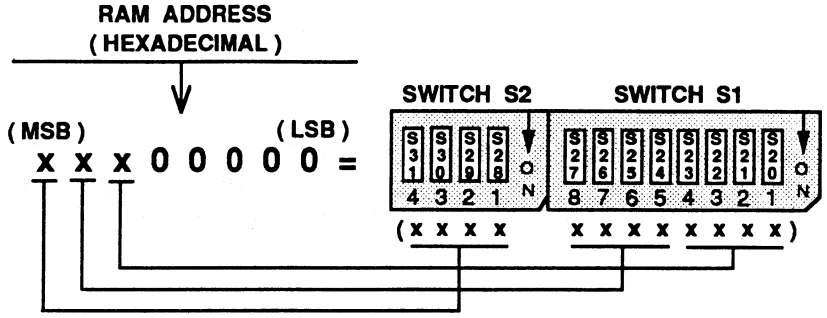
Header J4 is for factory use only. No jumpers are installed on the as-shipped factory configuration for all versions of the module.



2

VMEbus Address Decode Switches (S1, S2)

DIP switches S1 and S2 are used in selecting the starting address for the VMEbus. Addressing is selectable on 1Mb boundaries. Figure 2-2 illustrates how switches S1 and S2 can be set for any required address. Table 2-1 provides the VMEbus address mapping (note switch settings: 0 = ON or closed; 1 = OFF or open).



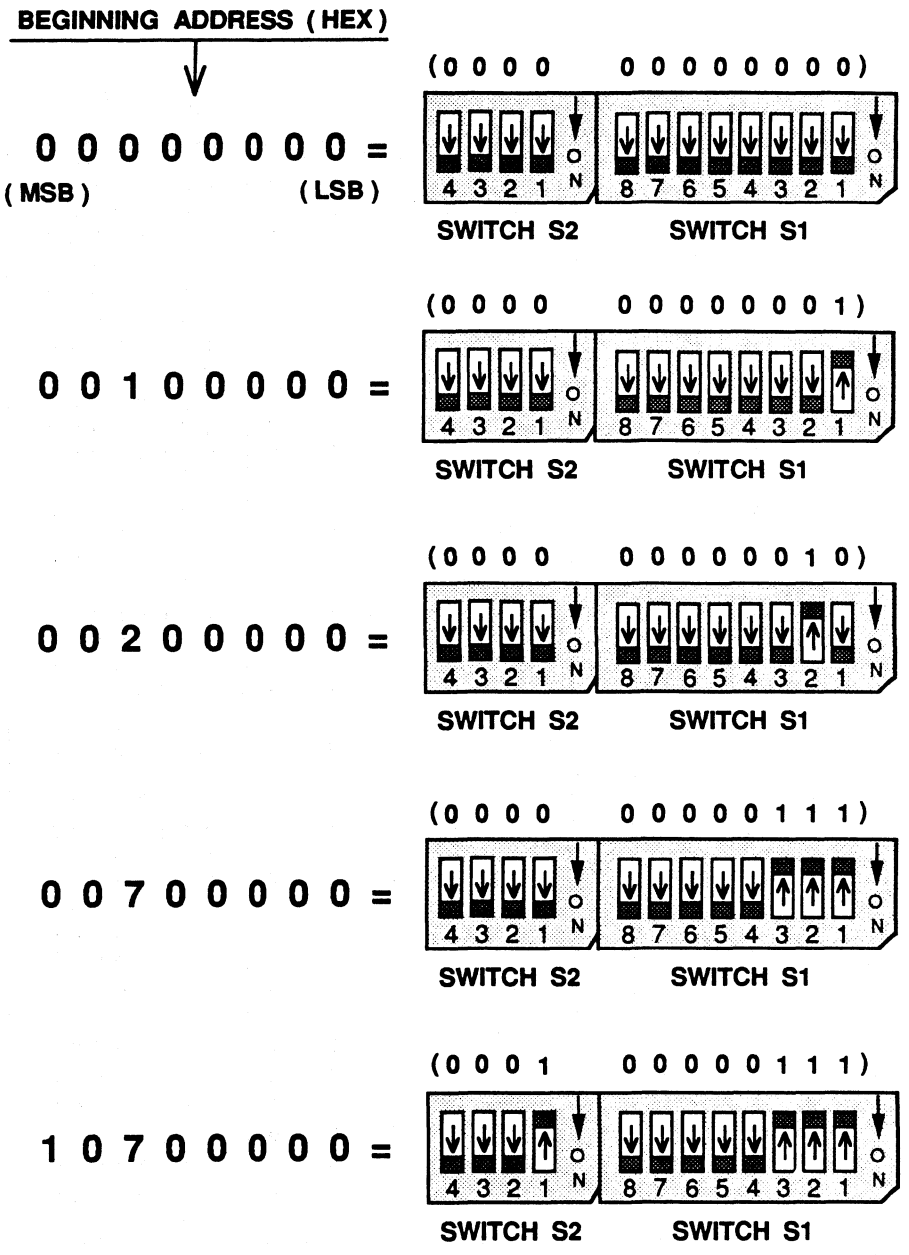


Figure 2-2. VMEbus Address Mapping Examples

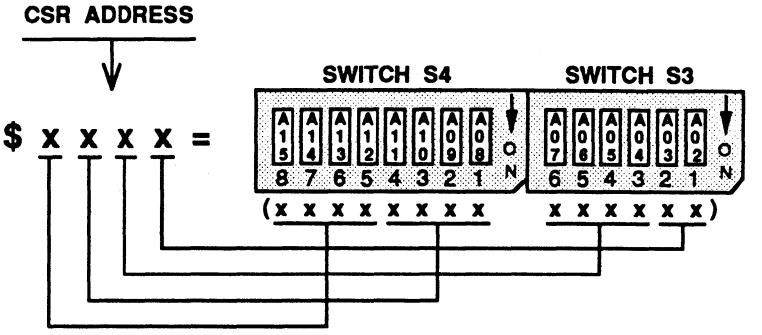
Table 2-1. VMEbus Address Mapping

VME ADDRESS MAPPING SWITCHES												RAM ADDRESS
S2-4	S2-3	S2-2	S2-1	S1-8	S1-7	S1-6	S1-5	S1-4	S1-3	S1-2	S1-1	(HEXADECIMAL)
0	0	0	0	0	0	0	0	0	0	0	0	00000000
0	0	0	0	0	0	0	0	0	0	0	1	00100000
0	0	0	0	0	0	0	0	0	0	1	0	00200000
0	0	0	0	0	0	0	0	0	0	1	1	00300000
0	0	0	0	0	0	0	0	0	1	0	0	00400000
0	0	0	0	0	0	0	0	0	1	0	1	00500000
0	0	0	0	0	0	0	0	0	1	1	0	00600000
0	0	0	0	0	0	0	0	0	1	1	1	00700000
0	0	0	0	0	0	0	0	1	0	0	0	00800000
0	0	0	0	0	0	0	0	1	0	0	0	00900000
0	0	0	0	0	0	0	0	1	0	0	0	00A00000
0	0	0	0	0	0	0	0	1	0	0	0	00B00000
0	0	0	0	0	0	0	0	1	0	0	0	00C00000
0	0	0	0	0	0	0	0	1	0	0	0	00D00000
0	0	0	0	0	0	0	0	1	0	0	0	00E00000
0	0	0	0	0	0	0	0	1	0	0	0	00F00000
0	0	0	0	0	0	0	1	0	0	0	0	01000000
0	0	0	0	0	0	0	1	0	0	0	1	01100000
0	0	0	0	0	0	0	1	0	0	1	0	01200000
0	0	0	0	0	0	0	1	0	0	1	1	01300000
0	0	0	0	0	0	0	1	0	1	0	0	01400000
0	0	0	0	0	0	0	1	0	1	0	1	01500000
0	0	0	0	0	0	0	1	0	1	1	0	01600000
0	0	0	0	0	0	0	1	0	1	1	1	01700000
0	0	0	0	0	0	0	1	1	0	0	0	01800000
0	0	0	0	0	0	0	1	1	0	0	1	01900000
0	0	0	0	0	0	0	1	1	0	1	0	01A00000
0	0	0	0	0	0	0	1	1	0	1	1	01B00000
0	0	0	0	0	0	0	1	1	1	0	0	01C00000
0	0	0	0	0	0	0	1	1	1	0	1	01D00000
0	0	0	0	0	0	0	1	1	1	1	0	01E00000
0	0	0	0	0	0	0	1	1	1	1	1	01F00000
0	0	0	0	0	0	1	0	0	0	0	0	02000000
0	0	0	0	0	1	0	0	0	0	0	0	04000000
0	0	0	0	1	0	0	0	0	0	0	0	08000000
0	0	0	1	0	0	0	0	0	0	0	0	10000000
0	0	1	0	0	0	0	0	0	0	0	0	20000000
0	1	0	0	0	0	0	0	0	0	0	0	40000000
1	0	0	0	0	0	0	0	0	0	0	0	80000000

SWITCH SETTINGS: 0 = CLOSED (ON); 1 = OPEN (OFF).

CSR Address Decode Switches (S3, S4)

DIP switches S3 and S4 are used in selecting the address for the Control/Status Register (CSR) in the short I/O address space. The CSR is independently mappable to byte 1 of any longword in the short I/O address range. Figure 2-3 illustrates how switches S3 and S4 can be set. Table 2-2 provides the switch setting for the CSR address mapping.



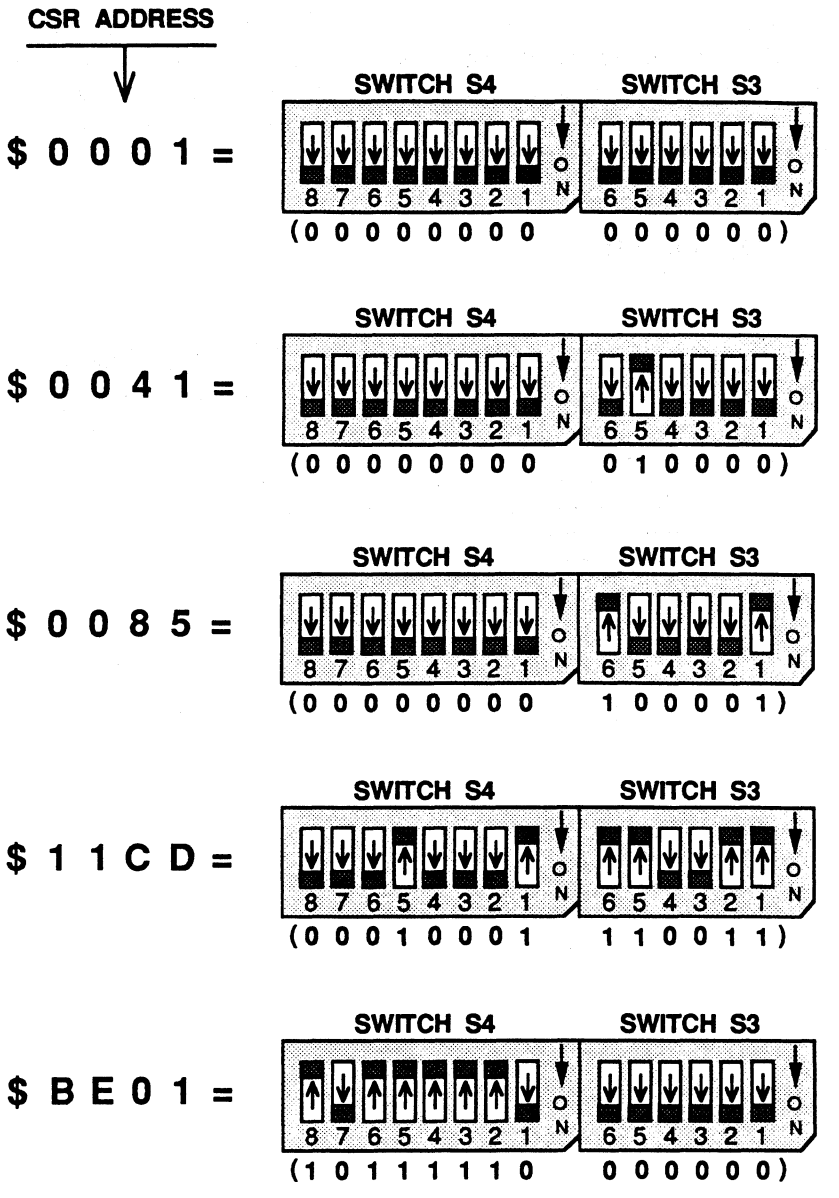


Figure 2-3. CSR Address Mapping Examples

Table 2-2. CSR Address Mapping

CSR ADDRESS MAPPING SWITCHES														CSR
S4-8	S4-7	S4-6	S4-5	S4-4	S4-3	S4-2	S4-1	S3-6	S3-5	S3-4	S3-3	S3-2	S3-1	ADDRESS
0	0	0	0	0	0	0	0	0	0	0	0	0	0	$0001
0	0	0	0	0	0	0	0	0	0	0	0	0	1	$0005
0	0	0	0	0	0	0	0	0	0	0	0	1	0	$0009
0	0	0	0	0	0	0	0	0	0	0	0	1	1	$000D
0	0	0	0	0	0	0	0	0	0	0	1	0	0	$0011
0	0	0	0	0	0	0	0	0	0	0	1	0	1	$0015
0	0	0	0	0	0	0	0	0	0	0	1	1	0	$0019
0	0	0	0	0	0	0	0	0	0	0	1	1	1	$001D
0	0	0	0	0	0	0	0	0	0	1	0	0	0	$0021
0	0	0	0	0	0	0	0	0	0	1	0	0	1	$0025
0	0	0	0	0	0	0	0	0	0	1	0	1	0	$0029
0	0	0	0	0	0	0	0	0	0	1	0	1	1	$002D
0	0	0	0	0	0	0	0	0	0	1	1	0	0	$0031
0	0	0	0	0	0	0	0	0	0	1	1	0	1	$0035
0	0	0	0	0	0	0	0	0	0	1	1	1	0	$0039
0	0	0	0	0	0	0	0	0	0	1	1	1	1	$003D
0	0	0	0	0	0	0	0	0	1	0	0	0	0	$0041
0	0	0	0	0	0	0	0	1	0	0	0	0	0	$0081
0	0	0	0	0	0	0	1	1	0	0	0	0	0	$0181
0	0	0	0	0	0	1	0	0	0	0	0	0	0	$0201
0	0	0	0	0	0	1	1	0	0	0	0	0	0	$0301
0	0	0	0	0	1	0	0	0	0	0	0	0	0	$0401
0	0	0	0	1	0	0	0	0	0	0	0	0	0	$0801
0	0	0	1	0	0	0	0	0	0	0	0	0	0	$1001
0	0	1	0	0	0	0	0	0	0	0	0	0	0	$2001
0	1	0	0	0	0	0	0	0	0	0	0	0	0	$4001
1	0	0	0	0	0	0	0	0	0	0	0	0	0	$8001

SWITCH SETTINGS: 0 = CLOSED (ON); 1 = OPEN (OFF).
CSR ADDRESSES ARE IN SHORT I/O ADDRESS SPACE.

2

Installation Instructions

When the MVME236 has been configured as desired, it can be installed in the system as follows:

1. Turn all equipment power OFF and disconnect power cable from ac power source.

> **CAUTION**
>
> **Connecting Modules While Power is Applied May Result in Damage to Components on the Module.**

> **WARNING**
>
> **DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS EQUIPMENT. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.**

2. Remove chassis cover as instructed in the equipment user's manual.
3. Remove the filler panel from the appropriate card slot at the front of the chassis.
4. Insert the MVME236 into the selected card slot (any card slot except slot 1). Be sure module is seated properly into the connectors on the backplane. Fasten the module in the chassis with the screws provided.
5. The IACK and BG daisy chain jumpers may be removed or installed at chassis backplane for card slot the MVME236 is installed in. The MVME236 does not use these signals but connects the input to the output.
6. Replace cover and turn equipment power ON.

CHAPTER 3
FUNCTIONAL DESCRIPTION

Introduction

This chapter provides an overall block diagram view of the memory module. The discussion includes sections with detailed descriptions of the 4Mb, 8Mb, and 16Mb DRAM array, the DRAM timing and control circuitry, refresh arbitration, the VMEbus interface and address decode, parity generation and checking, and the Control/Status Register (CSR). For the purpose of the following description, the MVME236 is regarded as consisting of the functional blocks as illustrated in Figure 3-3. For further details, refer to the schematic diagram in the *SIMVME236 of Memory Modules Support Information.*

DRAM Array

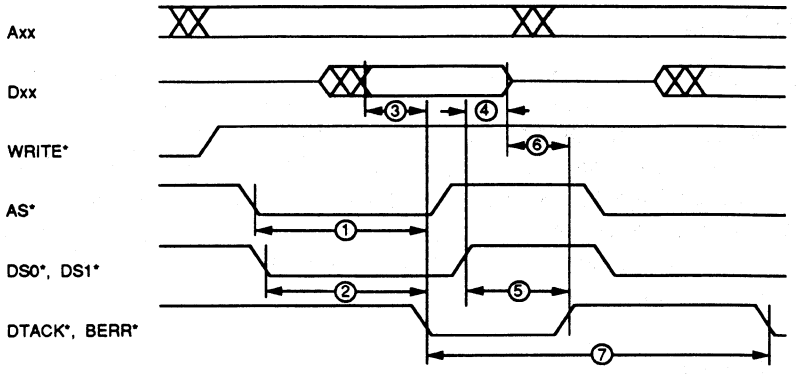
The MVME236-1 (4Mb version) provides a DRAM array of 36 1-megabit DRAMs. The MVME236-2 (8Mb version) provides a DRAM array of 72 1-megabit DRAMs. The MVME236-3 (16Mb version) provides a DRAM array of 144 1-megabit DRAMs. The DRAM array is arranged in 4 bytes with 1 parity bit per byte on the 4Mb version, 8 bytes with 1 parity bit per byte on the 8Mb version, or 16 bytes with 1 parity bit per byte on the 16Mb version.

CAS before RAS refresh is utilized, using the address counter internal to the DRAMs therefore, no refresh addresses must be supplied.

DRAM Timing, Control, and Arbitration

DRAM timing, arbitration of the internal bus between VMEbus, and refresh arbitration are all accomplished from two timing chains. The T0* timing handles arbitration and the RAST0* timing handles RAM signals. One of the two potential users of the arbitration scheme (VMEbus and refresh) has control at any time. When a request for a cycle is generated from the address decode circuit or the refresh circuit, the T0* timing chain is started. This timing chain causes arbitration to take place. If the user that generated the request is the same as the one which has the internal control, then the RAST0* timing is also started. This causes a memory cycle, or CSR cycle to take place. The third possibility is that a cycle can be started on the T0* timing chain by refresh causing an arbitration cycle to start. If within 50 nanoseconds, a cycle is decoded from VME, the RAST0* timing chain starts, causing what started as an arbitration only cycle to become

also a valid memory cycle for VME. Arbitration to refresh also happens during this cycle and it is followed by the refresh cycle. During every refresh cycle, arbitration is returned to VME. The result of this arbitration method is greater performance. The read cycle timing diagram is illustrated in Figure 3-1. The write cycle timing diagram is illustrated in Figure 3-2.



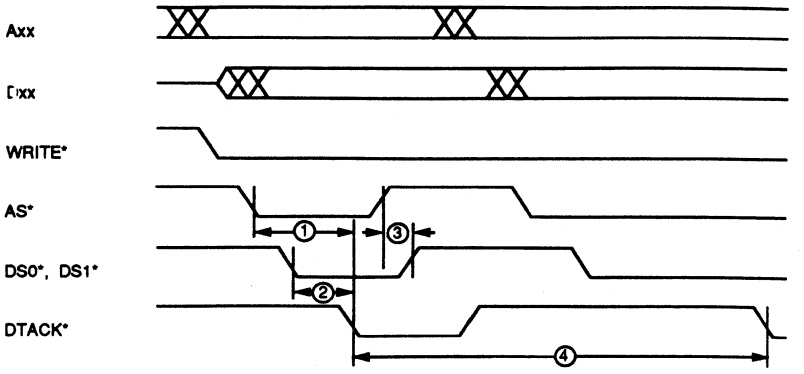
No.	Parameter	Min	Typ	Max	Unit	Notes
1	AS* low to DTACK*/BERR* low	160	170	485	ns	1,3
2	DS0*/DS1* low to DTACK*/BERR* low	160	170	485	ns	3
3	Data valid to DTACK* low	0	-	30	ns	-
4	DS0*/DS1* high to data invalid	10	-	40	ns	-
5	DS0*/DS1* high to DTACK*/BERR* high	15	20	30	ns	-
6	Data high imp. to DTACK*/BERR* high	0	-	35	ns	-
7	DTACK* low to DTACK* low	230	245	485	ns	2,3

NOTES: 1. Provided that the VMEbus master drives AS* and DS0*/DS1* low at the same time.

2. Provided that the VMEbus master drives DS0*/DS1* low less than 40 ns after receiving DTACK* low.

3. The maximum time can result if a refresh cycle has just started when the board is selected.

Figure 3-1. VMEbus Read Cycle Timing



No.	Parameter	Min	Typ	Max	Unit	Notes
1	AS* low to DTACK* low	55	65	355	ns	1,3
2	DS0*/DS1* low to DTACK* low	55	65	355	ns	3
3	DS0*/DS1* high to data high	15	20	30	ns	-
4	DTACK* low to DTACK* low	195	200	435	ns	2,3

NOTES: 1. Provided that the VMEbus master drives AS* and DS0*/DS1* low at the same time.

2. Provided that the VMEbus master drives DS0*/DS1* low less than 40 ns after receiving DTACK* low.

3. The maximum time can result if a refresh cycle has just started when the board is selected.

Figure 3-2. VMEbus Write Cycle Timing

VMEbus Interface

The VMEbus interface is the port to the MVME236 DRAM array. The VMEbus interface receives address, data, and control from the VMEbus and provides access to the DRAM array and the Control and Status Register (CSR).

It supports byte, word, and longword transfer and unaligned transfers. It responds to 24- or 32-bit addresses with the proper address modifier codes supplied. When responding to 24-bit address codes, the upper eight address lines are not considered. However, the upper eight address mapping switches (S1, 5-8 and S2, 1-4) must be mapped to a 0 (closed). Therefore, with 24-bit addressing, the module cannot be decoded higher than 00FFFFFF. It supports 8-, 16- or 32-bit data transfers.

The address modifier codes are decoded in PAL U148, which can be changed to support unique requirements. It may be mapped to be decoded on any 1Mb boundary in the addressing range. It does not support block transfer on the VMEbus. Table 3-1 provides the address modifier codes and functions.

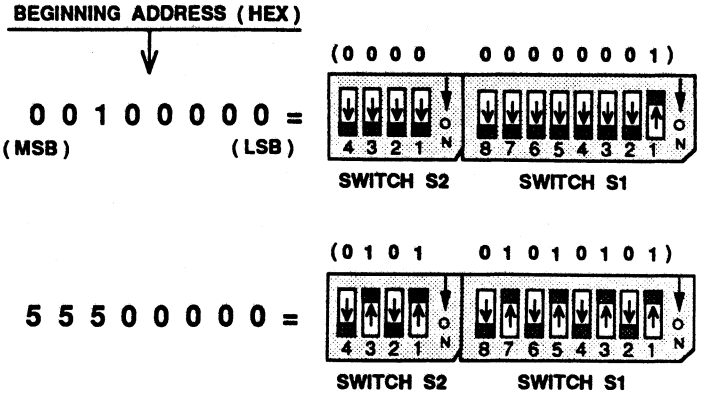
Table 3-1. Address Modifier Decode

AM Code	Function
$3F	Reserved
$3E	Standard Supervisory Program Access
$3D	Standard Supervisory Data Access
$3B-$3C	Reserved
$3A	Standard Non-Privileged Program Access
$39	Standard Non-Privileged Data Access
$2E-$38	Reserved
$2D	Short Supervisory Access (CSR Access)
$2A-$2C	Reserved
$29	Short Non-Privileged Access (CSR Access)
$20-$28	Reserved
$10-$1F	User-Defined Access (does not access MVME236)
$0F	Reserved
$0E	Extended Supervisory Program Access
$0D	Extended Supervisory Data Access
$0B-$0C	Reserved
$0A	Extended Non-Privileged Program Access
$09	Extended Non-Privileged Data Access
$00-$08	Reserved

Address Decoding

The MVME236 can be set to any starting address on 1Mb boundaries through binary encoding of the 12 switch positions located on DIP switches S1 and S2.

To set the starting address:



The switches should be ON for 0 and OFF for 1. Thus, a starting address of 00100000 would have the following switch positions: S1-2 through S1-8 ON; S2-1 through S2-4 ON; and S1-1 OFF. A starting address of 55500000 would have switch positions S1-1, S1-3, S1-5, S1-7, S2-1, and S2-3 OFF, and the rest ON.

Refer to Figure 2-2 and Table 2-2 for the VMEbus address mapping.

Parity

Parity is generated and checked on a byte wide basis. Parity is odd and is checked on each read and reported according to the state of the CSR parity enabled bit (bit 0) in the form of BERR* (VMEbus).

Control and Status Register

The control/status register provides a VMEbus accessible register for MVME236 status and control. This 8-bit register is writable and readable from the VMEbus. The control/status register bits are defined in the following text. Refer to Figure 2-3 and Table 2-3 for the CSR address mapping.

LD07	LD06	LD05	LD04	LD03	LD02	LD01	LD00
PES	N/U	R/W	R/W	R/W	R/W	WWP	EPD

EPD <Enable Parity Detection>

This bit, when set to a 1, allows parity error detection. It is used to enable or disable parity error detection. It is cleared (parity error detection disabled) on power up or reset. It is changed to a 1 when a 1 is written to this bit and cleared to a 0 when a 0 is written to this bit. When this bit is a 0, parity is still written according to the status of the WWP bit.

WWP <Write Wrong Parity>

This bit, when set to a 0, causes parity to be written in the normal (odd) state. When set to a 1, it causes parity to be written to the wrong (even) state. It is used for diagnostics. It is cleared to a 0 (write correct parity) on power up or reset. It is changed to a 1 when a 1 is written to this bit and changed to a 0 when a 0 is written to this bit.

R/W <Read/Write Bits LD02-LD05>

Bits LD02 through LD05 are read/writable bits in the CSR. They provide no control functions, but may be used as flags as needed. They are cleared to a 0 on power up or reset.

N/U <Not Used Bit LD06>

This bit is always driven to a 1. It is never cleared and is not used.

PES <Parity Error Status>

This bit, when set to a 1, indicates that a parity error has occurred on this module on the VMEbus. It does not indicate that the last read was a parity error, but that a parity error has occurred since it was last cleared. It is cleared to a 0 on power up or reset or when any write occurs to the control/status register and changed to a 1 when a parity error is detected, only if the enable parity detection bit is a 1.

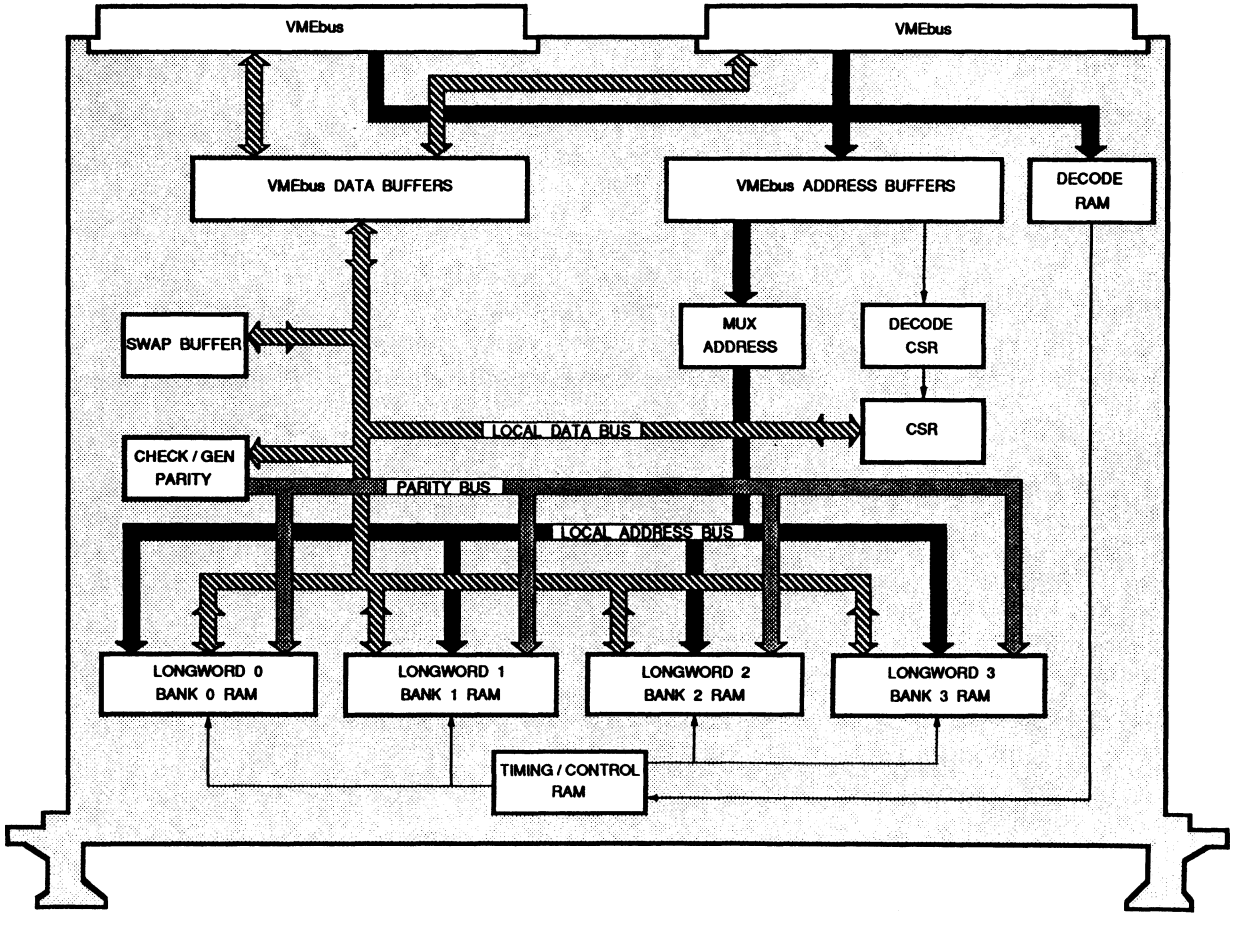


Figure 3-3. MVME236 Block Diagram

Notes

Notes

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