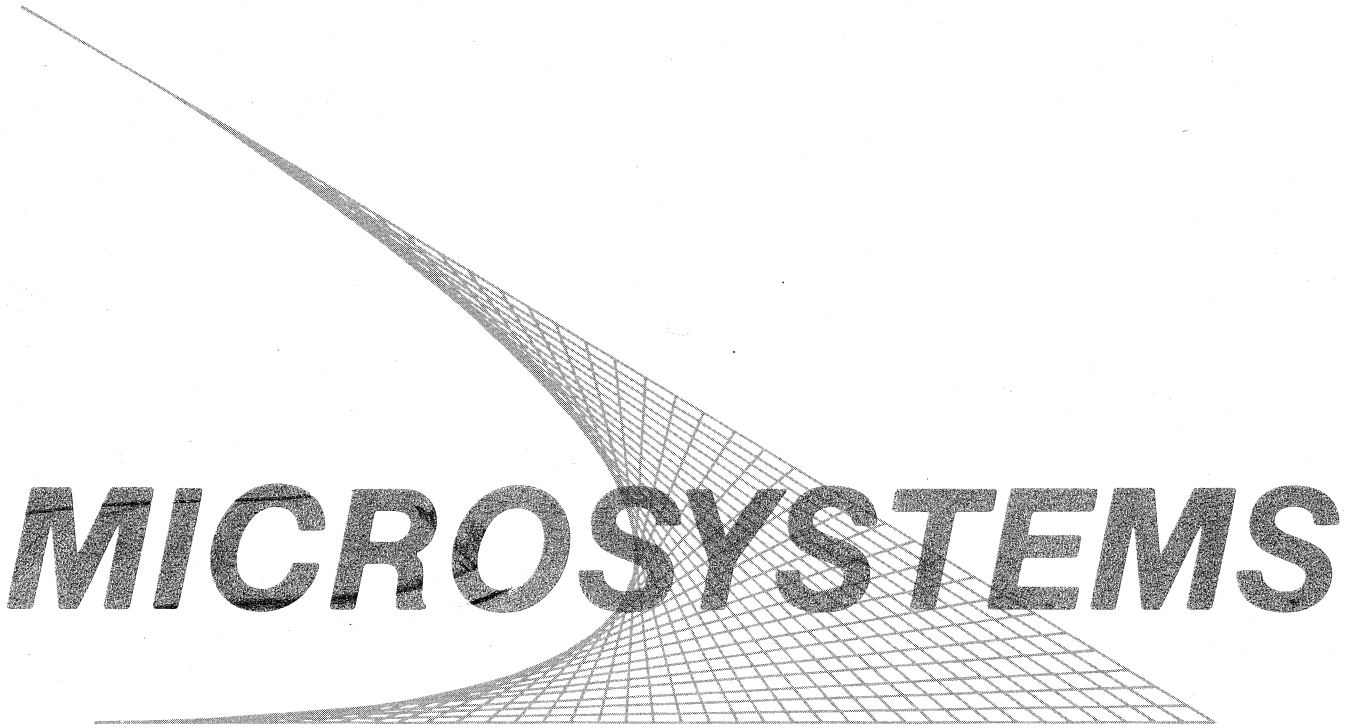
MOTOROLA

MVME110/D2

MVME110
VMEmodule
Monoboard Microcomputer
User's Manual



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MVME110/D2

MARCH 1983

MVME110-1

VMEmodule MONOBOARD MICROCOMPUTER

USER'S MANUAL

WARNING

THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTALLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE INTERFERENCE TO RADIO COMMUNICATIONS. AS TEMPORARILY PERMITTED BY REGULATION, IT HAS NOT BEEN TESTED FOR COMPLIANCE WITH THE LIMITS FOR CLASS A COMPUTING DEVICES PURSUANT TO SUBPART J OF PART 15 OF FCC RULES, WHICH ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINST SUCH INTERFERENCE. OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE INTERFERENCE, IN WHICH CASE THE USER, AT HIS OWN EXPENSE, WILL BE REQUIRED TO TAKE WHATEVER MEASURES MAY BE REQUIRED TO CORRECT THE INTERFERENCE.

Second Edition

First Edition July 1982

SAFETY SUMMARY
SAFETY DEPENDS ON YOU

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola Inc. assumes no liability for the customer's failure to comply with these requirements. The safety precautions listed below represent warnings of certain dangers of which we are aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

GROUND THE INSTRUMENT.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter, with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove equipment covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY EQUIPMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact Motorola Microsystems Warranty and Repair for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

14260 PRINTED IN USA (6/81) MPS 300

PREFACE

Unless otherwise specified, all address references are in hexadecimal throughout this manual.

An asterisk (*) following the signal name for signals which are level significant denotes that the signal is true or valid when the signal is low.

An asterisk (*) following the signal name for signals which are edge significant denotes that the actions initiated by that signal occur on a high to low transition.

Unless otherwise specified, all timing references are in nanoseconds.

TABLE OF CONTENTS

TABLE OF CONTENTS (cont'd)

TABLE OF CONTENTS (cont'd)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (cont'd)

LIST OF TABLES

LIST OF TABLES (cont'd)

CHAPTER 1

GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, hardware preparation and installation instructions, operation, functional description, and support information for the MVME110-1 VMEmodule Monoboard Microcomputer (referred to as the VME110 throughout this manual). The VME110 is shown in Figure 1-1.

1.2 FEATURES

Features of the VME110 are listed below.

- MC68000 8 MHz, 16-bit MPU (upgradable to 10 MHz when module not operating as system controller).
- VME system bus compatibility.
- VME system controller functions (jumper selectable).
  - VME single level bus arbiter
  - VMEbus timeout
  - System reset
  - System clock
- VMEbus requester - MPU may run on local bus without affecting concurrent operation on the VMEbus.
- Four programmable criteria for releasing VMEbus mastership.
- I/O Channel interface allows local bus to be extended.
- 8-bit asynchronous I/O Channel supports 4K-byte memory mapped I/O and four interrupt levels.
- MC6850 serial debug port with RS-232C compatible signal levels and front panel 25-pin connector. The port is configured as Data Communications Equipment (DCE) and may be connected to Data Terminal Equipment (DTE) without modification. The baud rate is jumper-selectable from 50 to 19,200 baud.
- 16-megabyte direct addressing range allowing access to VMEbus global memory, local (on-board) memory, and local I/O.
- Eight 28-pin sockets organized in four socket pairs for user-provided MOS static RAM and MOS ROM/PROM/EPROM devices. Each socket pair is individually configurable and each socket may accommodate a memory device size of up to 32K x 8 bits.
- Zero wait state operation with 150 ns or faster static RAM's at 8 MHz.
- Protect mode allows user to write-protect local RAM on 2K segment boundaries.

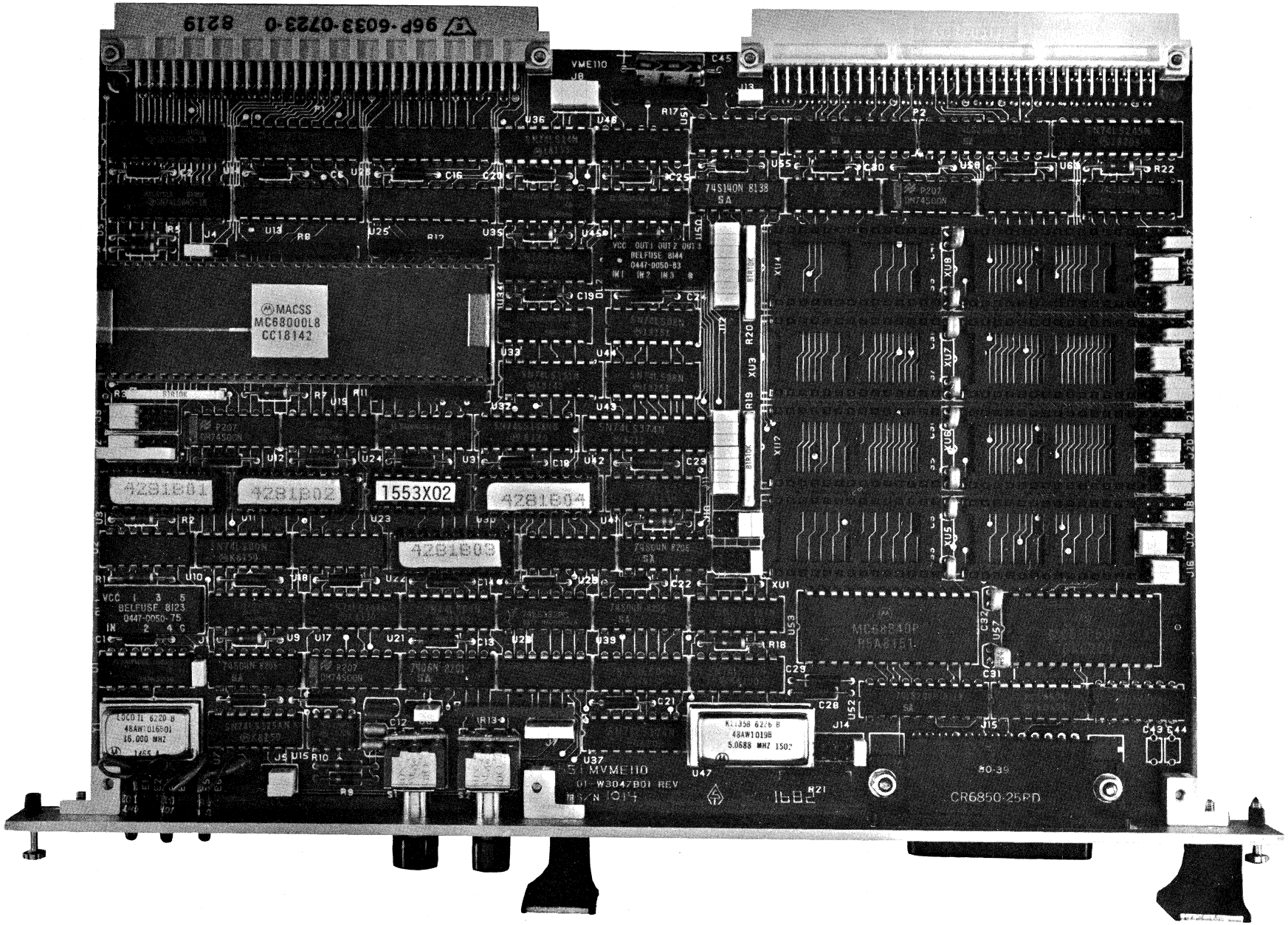

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FIGURE 1-1. MVME110-1 VMEmodule Monoboard Micromputer

- A local-memory-decode PROM allows for contiguous addressing between local memory and global VMEbus memory.

- Two user-configurable jumpers which may be read by the software.

- Module status and control registers.

- An MC6840 programmable timer module provides three independent 16-bit counters/timers. Timer outputs may be cascaded for 32- or 48-bit operation.

  - Watchdog timer - uses two MC6840 timers and allows user to generate NMI and RESET if processor fails to periodically restart the counter.

- Local bus timeout.

- Interrupt handler for up to seven VME interrupt levels plus up to seven local interrupt levels. The interrupt levels of the seven local interrupt sources are user-selectable. The ABORT pushbutton switch and VME ACFAIL* line are connected to non-maskable interrupt level seven.

- The RESET and ABORT pushbutton switches may be enabled or disabled by on-board jumpers.

- Board status indicators.

  - Red FAIL LED indicates module failure.

  - Red HALT LED indicates MPU is halted.

  - Green RUN LED indicates MPU is running.

1.3 SPECIFICATIONS

General specifications for the VME110 are listed in Table 1-1.

TABLE 1-1. VME110 Specifications

CHARACTERISTIC	SPECIFICATIONS
Power requirements (with all eight sockets unpopulated)	+5 Vdc (± 5%), 2.1 A (typical), 2.4 A (max.) +12 Vdc (± 5%), 25 mA (typical), 50 mA (max.) -12 Vdc (± 5%), 25 mA (typical), 50 mA (max.) (see NOTE)
Power requirements (with all eight sockets populated)	+5 Vdc (± 5%), 2.6 A (typical), 3.0 A (max.) +12 Vdc (± 5%), 25 mA (typical), 50 mA (max.) -12 Vdc (± 5%), 25 mA (typical), 50 mA (max.) (see NOTE)
Temperature	
Operating	0° to 70° C
Storage	-55° to +85° C
Relative humidity	0% to 90% (non-condensing)
Physical characteristics	Double-high VME board
Height	9.2 in. (234 mm)
Depth	6.3 in. (160 mm)
Thickness	.662 in. (16.77 mm)

NOTE: The currents at +12 Vdc and -12 Vdc are specified for the MVME110 module with the serial port connectors open. The actual required values depend on the load of the RS-232C ports. All serial port outputs are current-limited to sink or source 12 mA (max) each.

1.4 GENERAL DESCRIPTION

The VME110 is a high performance processing module, designed to function as either a stand-alone microcomputer, as a single CPU/system controller in a VMEbus system, or as one of several CPU elements in a multiprocessor VMEbus configuration. This module features the MC68000 16-bit microprocessor with a total address range of 16 megabytes. Sockets are provided to accommodate up to 256K bytes of user-supplied memory. Full support is provided for the I/O Channel which provides access to a large variety of peripheral and industrial I/O functions. An on-board serial communications port is also included.

The VME110 contains the following functional circuits:

- Local memory
- Serial I/O
- Programmable timer/counter
- Status monitoring and control
- VMEbus interface
- System interrupts
- I/O Channel

1.4.1 Local Memory

The capability for both ROM and RAM are provided by means of eight 28-pin sockets. Operation from on-board RAM is possible with no wait states generated. The on-board RAM memory area can be write protected by the user in 2K-segments, to protect critical program and data areas.

1.4.2 Serial I/O

An RS-232C serial terminal port is provided to allow use of a terminal or a downloading port to this module. Additional serial ports and parallel (Centronics) ports may be added by means of the I/O Channel. (Refer to paragraph 1.4.7).

1.4.3 Programmable Timer/Counter

Three independent 16-bit timer/counters are available to implement various forms of interrupts and watchdog timers, which allows the software and hardware to recover from various fault conditions. This feature is especially useful in industrial control systems.

1.4.4 Status Monitoring and Control

Pushbutton switches are provided for the functions of reset and abort. These switches may be disabled by the user, because some users may not want them to affect the operation of their control system. LED status lights are provided to indicate RUN, HALT, and FAIL status of the board. The FAIL LED is illuminated when power is initially applied and whenever the VME110 is reset. The user software may turn off this indicator to show that a self-test has been completed successfully.

1.4.5 VMEbus Interface

The VME110 provides full support for the VMEbus addressing and control logic. It also provides single-level bus arbitration and the 16-MHz system clock (8 MHz version of VME110 only). This allows systems to be configured without the use of an additional system controller board. The VME110 can access on-board memory while the VMEbus is occupied by either a DMA transfer to high-speed I/O, or by another CPU module. The private bus interconnecting the on-board memory, the processor, and the I/O functions is connected to the VMEbus only when accessing off-board resources.

1.4.6 System Interrupts

The VME110 can respond to seven priority levels of incoming interrupts from the VMEbus. In addition to these seven, four interrupt levels are assigned to the I/O Channel and three are assigned to on-board resources.

1.4.7 I/O Channel

The I/O Channel supports a large variety of mass storage and peripheral controllers (RS-232C, Centronics, SASI, etc.) and a range of industrial I/O control modules.

The I/O Channel is specifically designed to provide a modular low-cost interface for the addition of peripheral and I/O controller modules. It provides a 12-bit address bus and an 8-bit bidirectional data bus, and supports asynchronous operation at up to a 2-megabyte/second data rate. For those modules requiring time-critical operations, four prioritized interrupt lines are provided. The I/O Channel is designed to operate over either a backplane or a ribbon cable.

1.5 RELATED DOCUMENTATION

The following documentation is applicable to the VME110:

- MC68000UM MC68000 16-Bit Microprocessor User's Manual
- MC6840UM MC6840 Programmable Timer Fundamentals and Applications
- MVMEBUG VMEbug Debugging Packages User's Manual
- MVMEBS VMEbus Specification Manual
- M68RIOCS Input/Output Channel Specification Manual

CHAPTER 2

HARDWARE PREPARATION AND INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides unpacking, hardware preparation, and installation instructions for the VME110.

2.2 UNPACKING INSTRUCTIONS

NOTE

If shipping carton is damaged upon receipt, request carrier agent be present during unpacking and inspection of equipment.

Unpack equipment from shipping carton. Refer to packing list and verify that all items are present. Save packing material for storing or reshipping the equipment.

CAUTION

AVOID TOUCHING AREAS OF MOS CIRCUITRY; STATIC DISCHARGE CAN DAMAGE INTEGRATED CIRCUITS

2.3 HARDWARE PREPARATION

This section describes the hardware preparation of VME110 components prior to system installation. The completion of the actions described in this section will ensure that the components are properly configured for system operation.

The VME110 has been factory tested for system operation, and is shipped with factory-installed header jumper connections. There are 26 headers which are used to select the various functions and options of the module. Figure 2-1 illustrates the physical location of each jumper header. Table 2-1 lists each header designation, the function of each header, and the factory-installed configuration. A more detailed description of each header is provided in paragraphs 2.3.1 through 2.3.14.

The user must also program the map decoder PROM as described in paragraph 2.3.15.

Before the installation of the module, the user should verify the jumper configuration of each header and alter the configuration, if necessary, to suit particular system requirements.

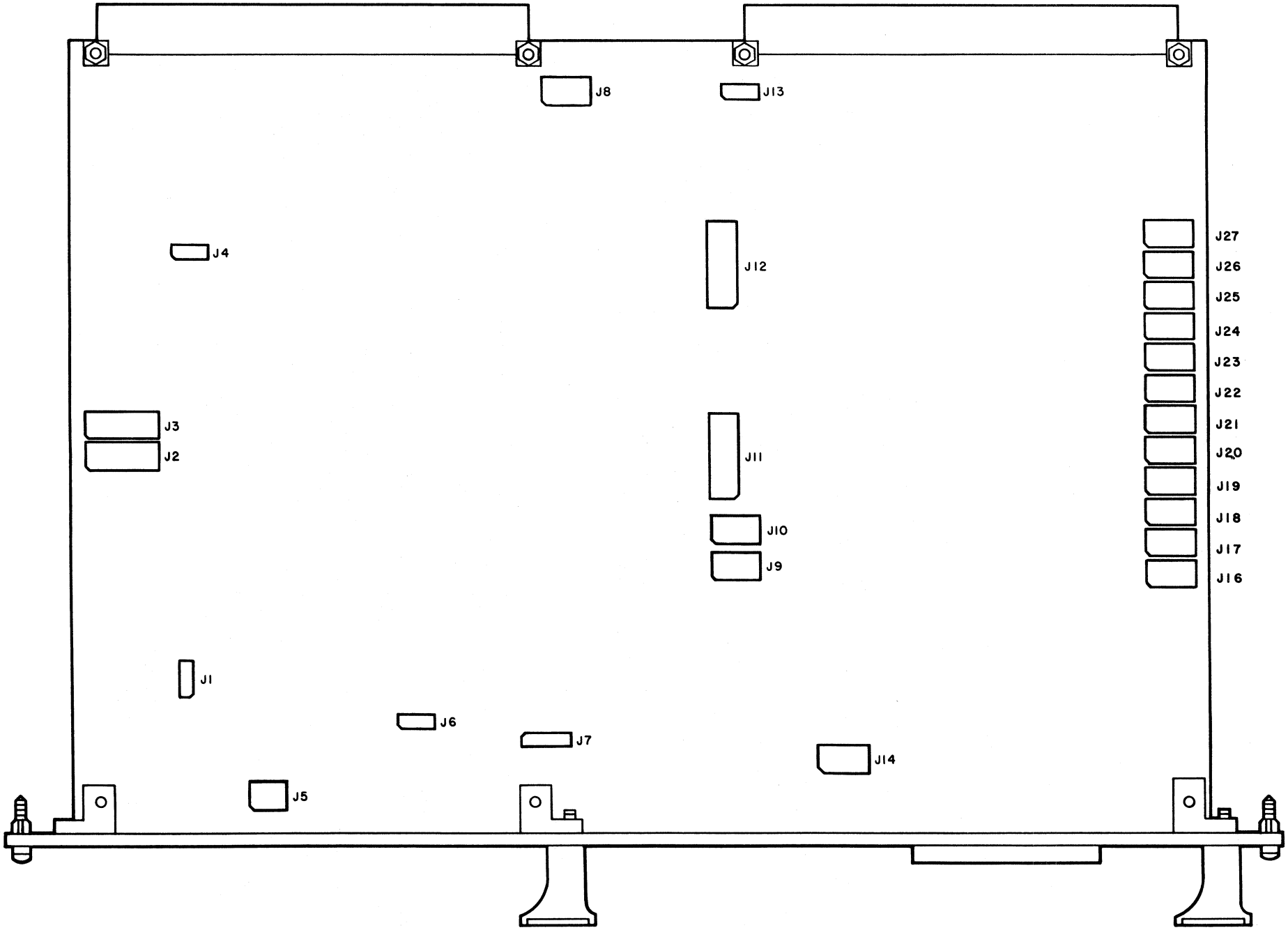


FIGURE 2-1. VME110 Jumper Header Locations

TABLE 2-1. VME110 Headers

HEADER NUMBER	FUNCTION	FACTORY-INSTALLED CONFIGURATION
J1	MPU clock select	1-2
J2	Bus arbitration request level select	1-3, 5-7, 4-6, 9-11
J3	Bus arbitration request level select	4-6, 3-5
J4	Address modifier 3 (AM3) select	1-2
J5	Software status bits (user-configurable)	4-6, 3-5
J6	Local bus timeout	2-3
J7	RESET, ABORT pushbutton switch enables	1-2, 3-4
J8	System controller functions	1-2, 3-4, 5-6, 7-8
J9	ROM access time select	7-8
J10	RAM access time select	5-6, 7-8
J11	Group 1 local interrupt level enables	1-2, 3-4, 5-6, 7-8, 9-10 11-12, 13-14
J12	Group 0 VMEbus interrupt level enables	1-2, 3-4, 5-6, 7-8, 9-10 11-12, 13-14
J13	I/O Channel buffer option	2-3
J14	Baud rate select	7-8
J15	RS-232C connector	
J16	Socket pair 1 local memory configuration headers	3-5, 4-6
J17	Socket pair 1 local memory configuration headers	1-2, 3-4
J18	Socket pair 1 local memory configuration headers	5-7
J19	Socket pair 2 local memory configuration headers	5-7, 6-8
J20	Socket pair 2 local memory configuration headers	3-5, 4-6
J21	Socket pair 2 local memory configuration headers	5-7
J22	Socket pair 3 local memory configuration headers	5-7, 6-8
J23	Socket pair 3 local memory configuration headers	3-5, 4-6
J24	Socket pair 3 local memory configuration headers	5-7
J25	Socket pair 4 local memory configuration headers	5-7, 6-8
J26	Socket pair 4 local memory configuration headers	3-5, 4-6
J27	Socket pair 4 local memory configuration headers	5-7

2.3.1 MPU Clock Speed Header (J1)

Figure 2-2 illustrates the factory configuration of header J1. The standard MPU supplied on the VME110 is an 8-MHz, MC68000 processor. However, the VME110 can also be configured to accept a 10-MHz MPU, as listed in Table 2-2. Refer also to paragraph 2.4 for the additional reconfiguration requirements.

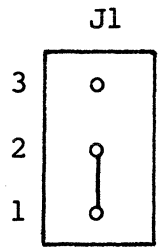


FIGURE 2-2. MPU Clock Speed Header (J1)

TABLE 2-2. Header J1 Configurations

PINS CONNECTED	REMARKS
1-2	8 MHz
2-3	10 Mhz

2.3.2 Bus Arbitration Request Level Select Headers (J2, J3)

Headers J2 and J3 are used to determine the level in which the MPU will request bus mastership. When the VME110 is configured to be the system controller, it monitors only one level of bus request. In this case, the request level must be configured for level three. When the VME110 is used with a system controller board which supports all four bus request levels, any one of the levels may be selected, with level three having the highest priority. This header must also jumper the unused bus-grant-in lines to their respective bus-grant-out lines.

Figure 2-3 illustrates the factory configuration of headers J2 and J3. Table 2-3 lists the jumper configurations that determine which request level is selected.

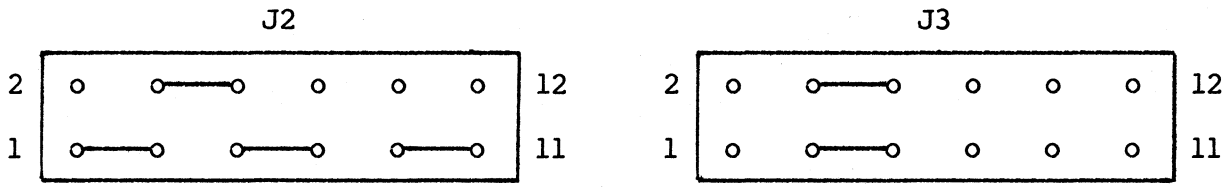


FIGURE 2-3. Bus Arbitration Request Level Select Headers (J2, J3)

TABLE 2-3. Header J2, J3 Configurations

HEADER	PINS CONNECTED	REMARKS
J2	3-5, 4-6	Request level 0
J3	2-4, 3-5, 6-8, 10-12	
J2	3-5, 4-6	Request level 1
J3	1-3, 4-6, 5-7, 9-11	
J2	2-4, 3-5, 6-8, 10-12	Request level 2
J3	3-5, 4-6	
J2	1-3, 4-6 5-7, 9-11	Request level 3 (used whenever a VME110 is configured as the system controller)
J3	3-5, 4-6	

2.3.3 Address Modifier 3 (AM3) Select Header (J4)

Header J4 is used to select the state of the AM3 line during VME data transfers. The standard configuration causes a logic "1". The alternate configuration drives AM3 to a logic '0' when in the protect mode (refer to paragraph 4.3.9.1 and Table 4-7). Figure 2-4 illustrates the factory configuration of header J4. Table 2-4 lists the possible configurations of the header.

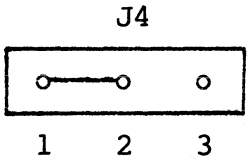


FIGURE 2-4. Address Modifier Select Header (J4)

TABLE 2-4. Header J4 Configurations

PINS CONNECTED	REMARKS
1-2	AM3 always a logic "1"
2-3	Protect mode bit from Module Control Register (MCR) connected to AM3

2.3.4 Software Status Bits Header (J5)

Header J5 is used to determine the logic level that the user software reads as SSB0 and SSB1 from the Module Status Register (MSR). These bits may be used to allow the user software to enter one of four modes, depending on the jumper settings. Figure 2-5 illustrates the factory configuration of this header. Table 2-5 lists the various configurations of the header.

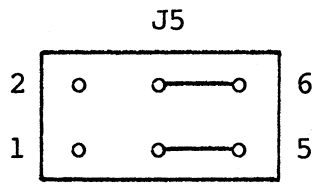


FIGURE 2-5. Software Status Bit Header (J5)

TABLE 2-5. Header J5 Configurations

PINS CONNECTED	REMARKS
4-6	SSB0 logic "0"
2-4	SSB0 logic "1"
3-5	SSB1 logic "0"
1-3	SSB1 logic "1"

2.3.5 Local Bus Timeout Header (J6)

Header J6 is used to enable/disable the local bus timeout counter. The Bus Error (BERR*) signal is generated on any cycle that is not completed within 200 microseconds. BERR* to the processor causes a bus error exception sequence.

Figure 2-6 illustrates the factory configuration of header J6. Table 2-6 lists the possible configurations of this header.

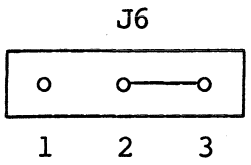


FIGURE 2-6. Local Bus Timeout Header (J6)

TABLE 2-6. Header J6 Configurations

PINS CONNECTED	REMARKS
1-2	Disabled
2-3	Enabled

2.3.6 RESET, ABORT Pushbutton Enable Header (J7)

Header J7 is used to enable or disable the front panel RESET and ABORT pushbuttons. Figure 2-7 illustrates the factory configuration of header J7 (both pushbuttons enabled). If a pushbutton is to be disabled, the corresponding jumper is removed. Table 2-7 lists the pins to be connected to enable each of the functions.

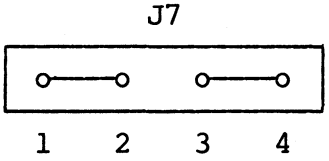


FIGURE 2-7. RESET, ABORT Pushbutton Enable Header (J7)

TABLE 2-7. Header J7 Configurations

PINS CONNECTED	REMARKS
1-2	RESET pushbutton enabled
3-4	ABORT pushbutton enabled

2.3.7 System Controller Functions Header (J8)

Header J8 is used to enable or disable the VME110 as the system controller. When enabled as the system controller, the VME110 must be installed in slot A01 of the VME backplane and provides the system reset, system arbiter, system clock, and system bus timeout functions. Only one board in the system may be designated as the system controller. If any VME110 boards are to be installed with a board already designated as the system controller, this header should be disabled by removing all of the jumpers. Figure 2-8 illustrates the factory configuration of header J8. Table 2-8 lists the pins to be connected to enable the various functions.

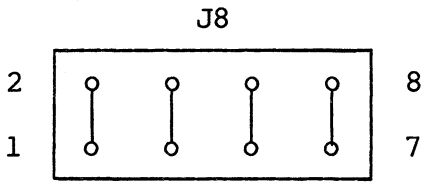


FIGURE 2-8. System-Controller-Functions Header (J8)

TABLE 2-8. Header J8 Configurations

PINS CONNECTED	REMARKS
1-2	System reset enable
3-4	Arbiter enable
5-6	System clock enable
7-8	VMEbus timeout enable

2.3.8 ROM Access-Time-Select Header (J9)

Header J9 is used to select an appropriate delay to compensate for the access times of the ROM memory devices that are installed in local memory. Many types of ROM devices may be used in local memory. The installation of the jumpers on the memory configuration headers varies according to the access times of the ROM devices which are used. Several standard and optional configurations of the memory configuration headers are provided in paragraph 2.3.14. Some of these configurations can be done by using the plastic jumper blocks provided on the VME110. Other configurations require the user to wire-wrap jumper wires between the pins of the configuration blocks. A standard configuration is defined as one which does not require that any jumpers be wire-wrapped. For each of these configurations, the user should compare the access times of the installed ROM devices with the times listed in Table 2-9, and install the appropriate jumper in header J9 to select the maximum delay required.

Certain ROM circuits have both an enable input ($\overline{E}$ or $\overline{CE}$) and an output-enable input ($\overline{OE}$). The access time of these devices can be decreased by jumpering the OE* signal of the VME110 to the enable input of the ROM, and by jumpering the socket pair select (SPn*) to the output-enable input of the ROM. This is because in the VME110, OE* is produced before the SPn* signal. To configure the memory devices to take advantage of this feature requires that certain pins of the memory configuration headers be wire-wrapped. Any configuration of the memory configuration headers which requires a wire-wrapped jumper is defined as an optional configuration. For any optional configuration, the user should compare the access times of the ROM devices being used, with the times listed in Table 2-9, which are preceded by an asterisk, and install the appropriate jumper in header J9 to select the maximum delay required.

Figure 2-9 illustrates the factory configuration of header J9.

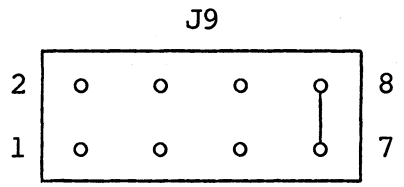


FIGURE 2-9. ROM-Access-Time-Select Header (J9)

TABLE 2-9. Header J9 Configurations

PINS CONNECTED	REMARKS 8 MHz MPU	REMARKS 10 MHz MPU	WAIT CYCLES
1-2	0-165 ns	0-100 ns	0
	* 0-220 ns	* 0-165 ns	
3-4	165-290 ns	100-200 ns	1
	* 220-345 ns	* 165-265 ns	
5-6	290-415 ns	200-300 ns	2
	* 345-470 ns	* 265-365 ns	
7-8	415-550 ns	300-400 ns	3
	* 470-595 ns	* 365-465 ns	

NOTE: Times preceded by asterisks should be used for ROM circuits which require an optional memory configuration (wire-wrapped jumpers in memory configuration headers. Refer to paragraph 2.3.14).

2.3.9 RAM Access-Time-Select Header (J10)

Header J10 is used to select the appropriate delay to compensate for the access times of the RAM memory devices that are installed in local memory. The user should compare the access times of the RAM devices installed with the access times listed in Table 2-10, and install the jumpers in header J10 which correspond to the delay required by the RAM memory devices.

Figure 2-10 illustrates the factory configuration of header J10.

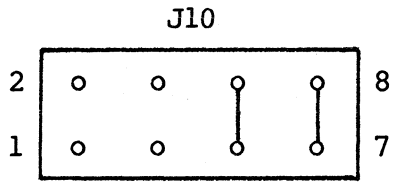


FIGURE 2-10. RAM Access-Time-Select Header (J10)

TABLE 2-10. Header J10 Configurations

PINS CONNECTED	REMARKS		
	8 MHz MPU	10 MHz MPU	WAIT CYCLES
1-2, 3-4	0-165 ns	0-100 ns	0
5-6, 7-8	165-290 ns	100-200 ns	1

2.3.10 Local Interrupt Enable Header (J11)

Header J11 is used to assign seven of the local group 1 interrupts to the desired MPU interrupt level. Any of the seven interrupts may be jumpered to any of the seven MPU interrupt levels. Interrupt conditions may be wired-ORed so that more than one of the interrupt conditions cause a common level of interrupt. It should be noted that if more than one interrupt is connected to a common level within an interrupt group, it may be difficult or impossible for software to determine which event caused the interrupt.

Figure 2-11 illustrates the factory configuration of header J11. Table 2-11 lists the pins to be connected or disconnected to enable or disable the respective interrupt level.

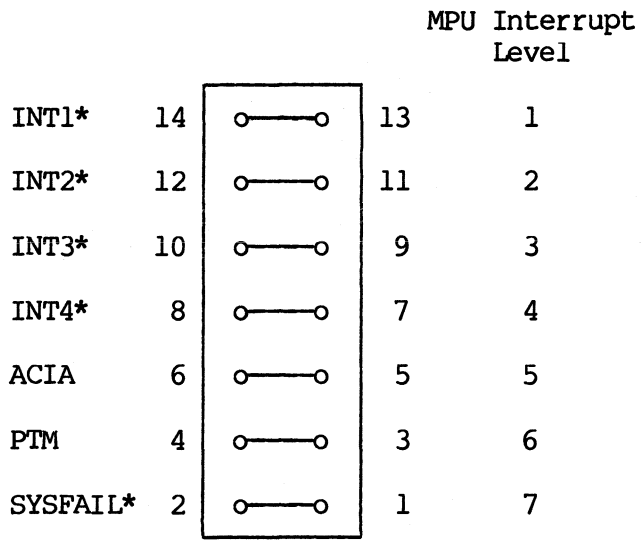


FIGURE 2-11. Local Interrupt Enable Header (J11)

TABLE 2-11. Header J11 Configurations

PINS CONNECTED	REMARKS
1-2	System fail to interrupt level 7
3-4	Programmable timer to interrupt level 6
5-6	ACIA to interrupt level 5
7-8	I/O interrupt 4 to interrupt level 4
9-10	I/O interrupt 3 to interrupt level 3
11-12	I/O interrupt 2 to interrupt level 2
13-14	I/O interrupt 1 to interrupt level 1

2.3.11 VMEbus Interrupt Enable Header (J12)

Header J12 is used to selectively enable or disable any of the VMEbus interrupts from interrupting the MPU. Interrupts from the VMEbus are group 0 interrupts. Figure 2-12 indicates the configuration of the jumpers as shipped from the factory. This configuration allows the on-board MPU to be interrupted by all VMEbus interrupts. If any other MPU's are present on the VMEbus, certain interrupt level jumpers must be removed so that not more than one MPU responds to a given VMEbus interrupt. There can be no duplication of interrupt levels enabled between MPU's. If a given interrupt level is not to be serviced, remove the corresponding interrupt jumper. Table 2-12 lists each of the interrupt levels and the pins to be connected on header J12 to enable the corresponding interrupt.

Group 0 interrupts always expect a vector number from the VMEbus. Never wire-wrap group 0 interrupts to or from group 1 interrupts.

VMEbus interrupts cannot be wired to a different interrupt level. Install the jumpers straight across the pins on the header or omit the appropriate jumpers.

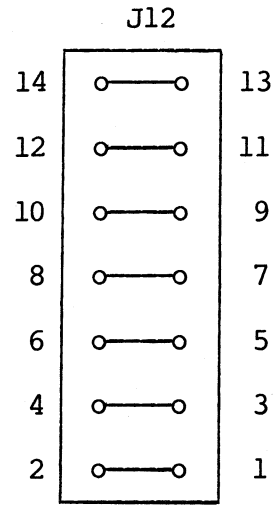


FIGURE 2-12. VMEbus Interrupt Enable Header (J12)

TABLE 2-12. Header J12 Configurations

PINS CONNECTED	REMARKS
13-14	Interrupt level 1
11-12	Interrupt level 2
9-10	Interrupt level 3
7-8	Interrupt level 4
5-6	Interrupt level 5
3-4	Interrupt level 6
1-2	Interrupt level 7

2.3.12 I/O Channel Buffer Option Header (J13)

Header J13 is used to select a factory assembly option. The standard VME110 is shipped with type 74LS244 integrated circuits installed in U55 and U59 and with a jumper connected as shown in Figure 2-13. Table 2-13 lists the possible configurations of header J13.

NOTE

This is intended as a factory option only, and is not to be changed by the user.

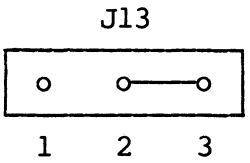


FIGURE 2-13. I/O Channel Buffer Option Header (J13)

TABLE 2-13. Header J13 Configurations

PINS CONNECTED	REMARKS
1-2	74S241
2-3	74LS244

2.3.13 Baud Rate Select Header (J14)

Header J14 is used to select the baud rate of the serial port. Table 2-14 lists the usable jumper configurations. Figure 2-14 illustrates the jumper configuration when shipped from the factory (9600 baud).

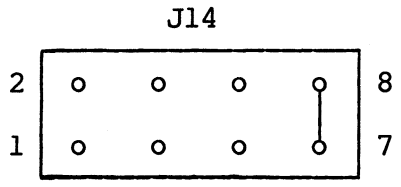


FIGURE 2-14. Baud Rate Select Header (J14)

TABLE 2-14. Header J14 Configurations

PINS CONNECTED	REMARKS
1-2, 3-4, 5-6, 7-8	Baud rate 50
1-2, 3-4, 5-6	Baud rate 75
1-2, 3-4, 7-8	Baud rate 110
1-2, 3-4	Baud rate 134.5
1-2, 5-6, 7-8	Baud rate 150
1-2, 5-6	Baud rate 300
1-2, 7-8	Baud rate 600
1-2	Baud rate 1200
3-4, 5-6, 7-8	Baud rate 1800
3-4, 5-6	Baud rate 2000
3-4, 7-8	Baud rate 2400
3-4	Baud rate 3600
5-6, 7-8	Baud rate 4800
5-6	Baud rate 7200
7-8	Baud rate 9600
No connections	Baud rate 19200

2.3.14 Local Memory Configuration Headers (J16-J27)

Headers J16-J27 are used to configure the various types of memory which may be installed in the local memory socket pairs. The local (on-board) memory of the VME110 is organized into four socket pairs as illustrated in Figure 2-15.

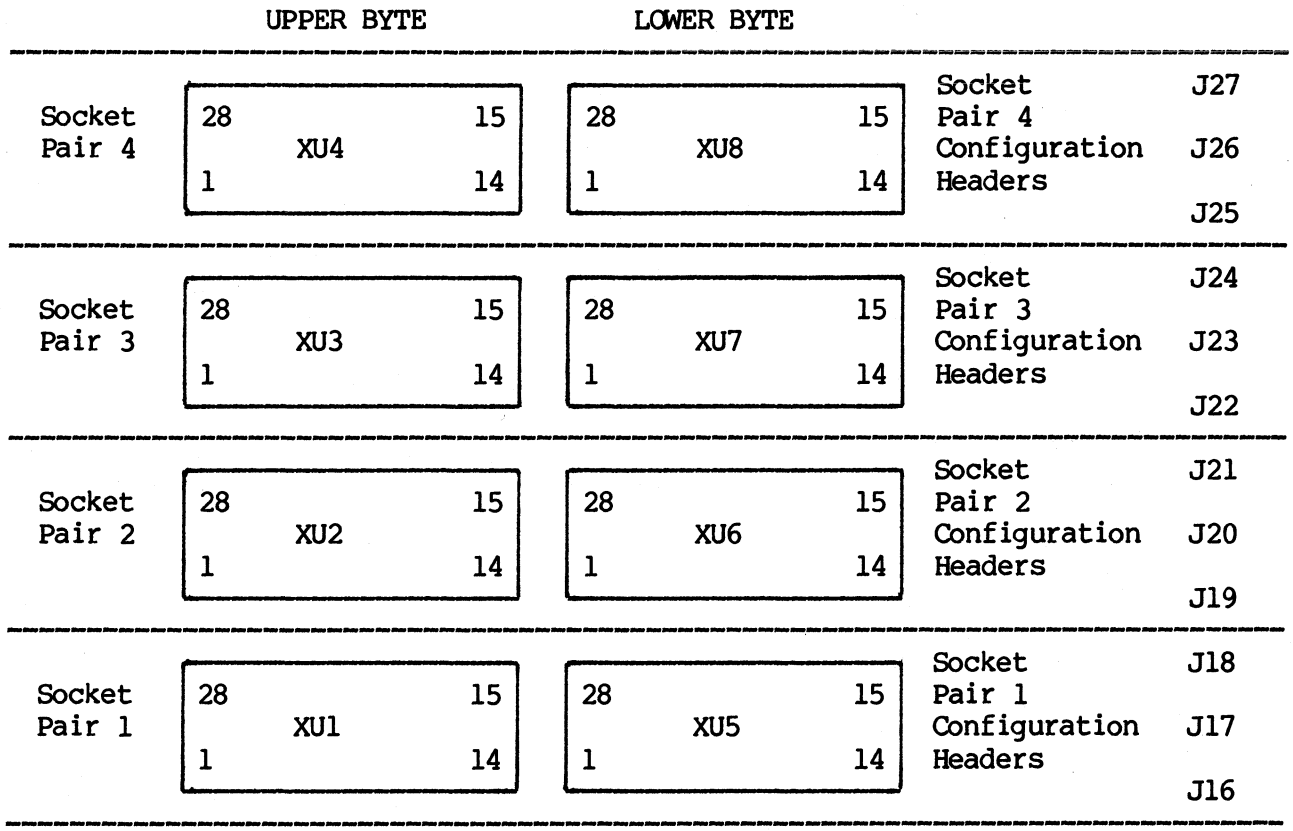


FIGURE 2-15. Local Memory Organization

Each socket pair may be individually configured to accept a wide range of industry standard 24-pin and 28-pin MOS static RAM/s and MOS ROM/PROM/EPROM devices. The user must provide and install the appropriate memory devices to suit the specific application of the VME110. 28-pin devices are inserted with pins 1 through 28 of the device matching pins 1 through 28 of the socket. 24-pin devices are inserted with pins 1 through 24 of the device matching pins 3 through 26 of the socket, as illustrated in Figure 2-16.

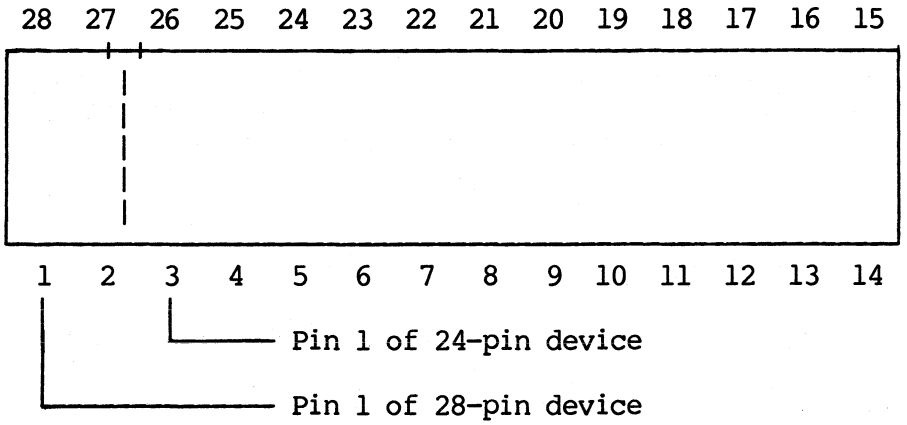


FIGURE 2-16. Placement of Memory Devices in Sockets

The following restrictions apply to the installation of memory devices.

a. The two devices that are installed in a socket pair must be of the same pinout, memory size, and access time.

b. All devices must have an MOS high impedance input characteristic. (Not bipolar)

c. ROM/PROM/EPROM type devices must be installed in socket pair 1 for fetching the initial SSP and PC.

d. 2K x 8, 4K x 8, 8K x 8, 16K x 8, or 32K x 8 devices may be installed.

e. Refer to Memory Access Time selection (paragraphs 2.3.8 and 2.3.9) for information regarding the recommended device access times.

Associated with each socket pair are three local memory configuration headers. All three headers must be configured for each socket pair that contains memory devices. Figure 2-17 shows how the memory configuration headers are configured when the board is shipped from the factory. The factory configuration is socket pair 1, 8K x 8 ROM's; socket pairs 2, 3, and 4, each 2K x 8 RAM's.

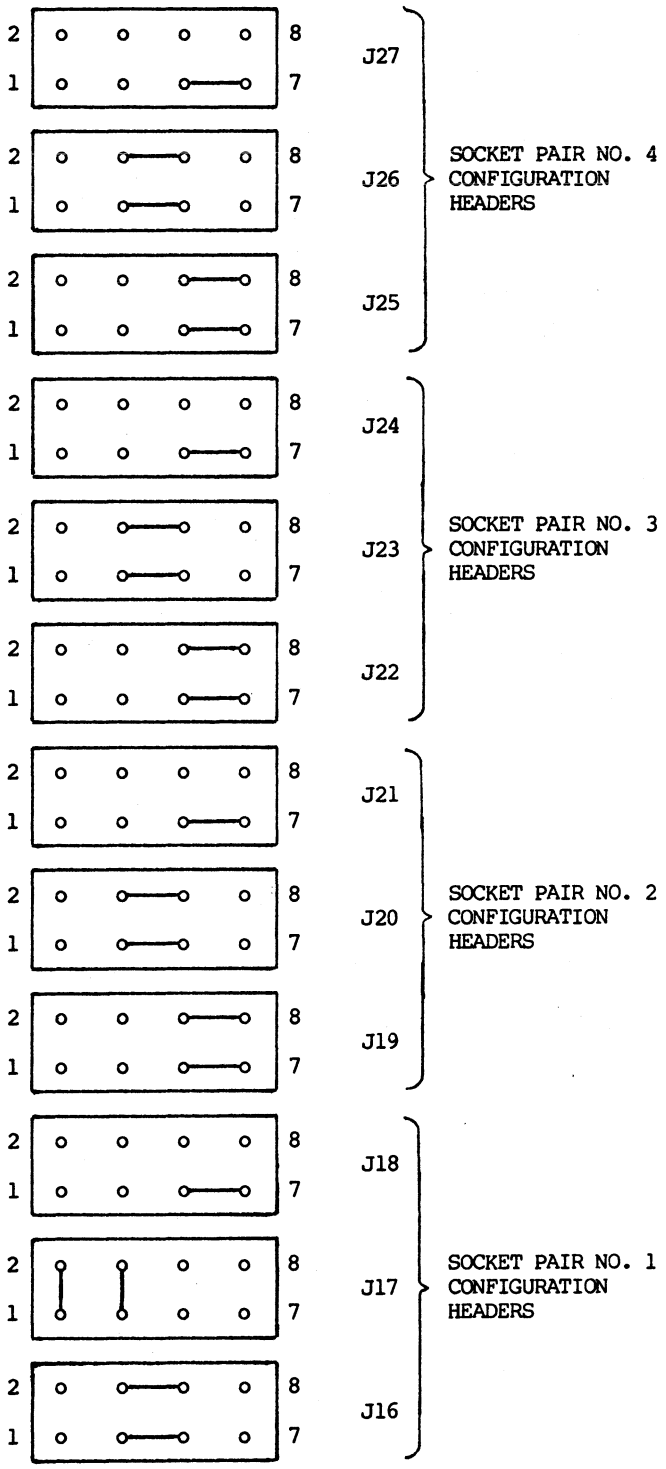


FIGURE 2-17. Local Memory Configuration Headers (J16-J27)

Table 2-15 lists several ROM/PROM/EPROM and RAM devices which may be installed in the socket pairs of local memory. If any of these device types, or device types having similar pinouts are selected for use, the table number and the figure number listed in the HEADER CONFIGURATION column can be used to determine the placement of the header configuration jumpers. The jumpering of pins for some of the header configurations can be performed using the jumpers provided. These configurations are identified by the word (standard).

The configurations identified as (optional) require that some of the header pins be connected by wire-wrap. In some cases, it is necessary to jumper between pins on different headers as illustrated in Figure 2-18.

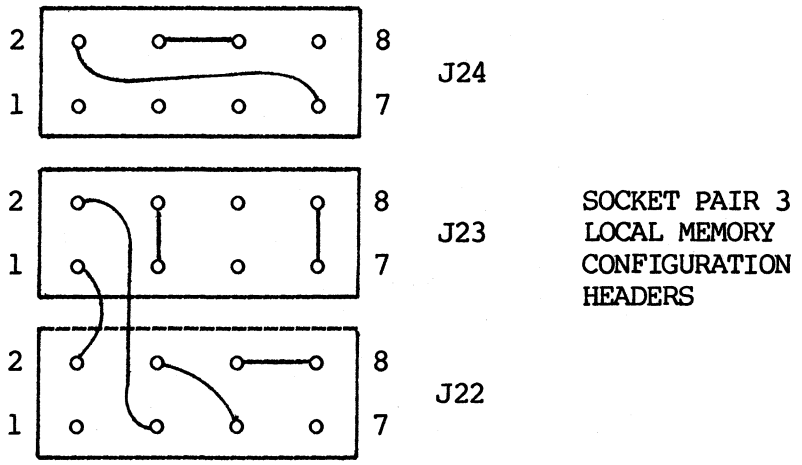


FIGURE 2-18. Wire-Wrapped Jumpers for Configuration Headers Example

The header numbers listed in Tables 2-16 through 2-26 are those which are associated with socket pair 1. The chart below may be used to determine the corresponding header numbers for the other socket pairs.

SOCKET PAIR	HEADERS
1	J16, J17, J18
2	J19, J20, J21
3	J22, J23, J24
4	J25, J26, J27

TABLE 2-15. Allowable ROM/PROM/EPROM and RAM Memory Devices

PART NUMBER	MANUFACTURER	DEVICE TYPE	SIZE	PINS	HEADER CONFIGURATION
MCM2716	Motorola	EPROM	2K x 8	24	Table 2-16 Figure 2-19 (STANDARD)
MCM68316E	Motorola	ROM			
AM2716	Advanced Micro Devices	EPROM			or
EA2716	Electronic Arrays	EPROM			Table 2-17 Figure 2-20 (OPTIONAL)
HM6716	Harris	EPROM			
HN462716	Hitachi	EPROM			
I2316E	Intel	ROM			
I2716	Intel	EPROM			
MBM2716	Fijitsu	EPROM			
MK2716	Mostek	EPROM			
MK34000	Mostek	ROM			
MM52116	National Semiconductor	ROM			
MN2716	Panasonic	EPROM			
MSM2716	OKI Electric Industry	EPROM			
NS2716	National Semiconductor	EPROM			
S4716	American Microsystems Inc.	EPROM			
SM2716	Siemens	EPROM			
SY2716	Synertek	EPROM			
TMS2516	Texas Instruments	EPROM			
UPD2716	Nippon Electric Company	EPROM	2K x 8	24	
MCM2532	Motorola	EPROM	4K x 8	24	Table 2-18 Figure 2-21 (STANDARD)
MCM68332	Motorola	ROM			
MCM68732	Motorola	ROM			
HN462532	Hitachi	EPROM			
MM52132	National Semiconductor	ROM			
NS2532	National Semiconductor	EPROM			
TMS2532	Texas Instruments	EPROM			
TMS4732	Texas Instruments	ROM	4K x 8	24	

TABLE 2-15. Allowable ROM/PROM/EPROM and RAM Memory Devices (cont'd)

PART NUMBER	MANUFACTURER	DEVICE TYPE	SIZE	PINS	HEADER CONFIGURATION
AM2732	Advanced Micro Devices	EPROM	4K x 8	24	Table 2-19 Figure 2-22 (OPTIONAL)
I2332	Intel	ROM			
I2732	Intel	EPROM			
HN462732	Hitachi	EPROM			
MBM2732	Fujitsu	EPROM			
NS2732	National Semiconductor	EPROM			
TMM2732	Texas Instruments	EPROM			
UPD2332	Nippon Electric Company	ROM			
UPD2732	Nippon Electric Company	EPROM	4K x 8	24	
MCM68364	Motorola	ROM	8K x 8	24	Table 2-20 Figure 2-23 (STANDARD)
MCM68365	Motorola	ROM			
MCM68366	Motorola	ROM			
MCM68764	Motorola	EPROM			
MCM68766	Motorola	EPROM			
TMS4764	Texas Instruments	ROM	8K x 8	24	
I2764	Intel	EPROM	8K x 8	28	Table 2-21 Figure 2-24 (OPTIONAL)
HN482764	Hitachi	EPROM			
MBM2764	Fujitsu	EPROM			
MSM2764	OKI Electric Ind.	EPROM			
UPD2364	Nippon Electric Company	ROM			
UPD2764	Nippon Electric Company	EPROM	8K x 8	28	
TMS2564	Texas Instruments	EPROM	8K x 8	28	Table 2-22 Figure 2-25 (OPTIONAL)
I27128	Intel	EPROM	16K x 8	28	Table 2-23 Figure 2-26 (OPTIONAL)

TABLE 2-15. Allowable ROM/PROM/EPROM and RAM Memory Devices (cont'd)

PART NUMBER	MANUFACTURER	DEVICE TYPE	SIZE	PINS	HEADER CONFIGURATION
TMM23256	Toshiba	EPROM	32K x 8	28	Table 2-24 Figure 2-27 (OPTIONAL)
MCM4016	Motorola	RAM	2K x 8	24	Table 2-25 Figure 2-28 (STANDARD)
6116	Integrated Device Technology	RAM			
M58725	Mitsubishi	RAM			
MB2128	Fujitsu	RAM			
MSM2128	OKI Electric Industry	RAM			
TMM2016	Toshiba	RAM			
TMS4016	Texas Instruments	RAM	2K x 8	24	
HM6264	Hitachi	RAM	8K x 8	28	Table 2-26 Figure 2-29 (OPTIONAL)

TABLE 2-16. 2K x 8 ROM Devices Standard Configuration, Headers J16-J27

HEADER NO. - PIN NO.	REMARKS
J16-5 to J16-7	Socket pair select (SPn*) to P20 ($\overline{E}$)
J16-6 to J16-8	Output enable (OE*) to P22 ($\overline{OE}$)
J17-3 to J17-4	P23U to P23L (VPP)
J18-5 to J18-7	+5V to P26 (VCC)
J18-6 to J18-8	+5V to P23U (VPP)

NOTE

The memory configuration headers for 2K x 8 ROM standard devices may optionally be configured as shown in Table 2-17 to decrease the access time. Refer to paragraph 2.3.8.

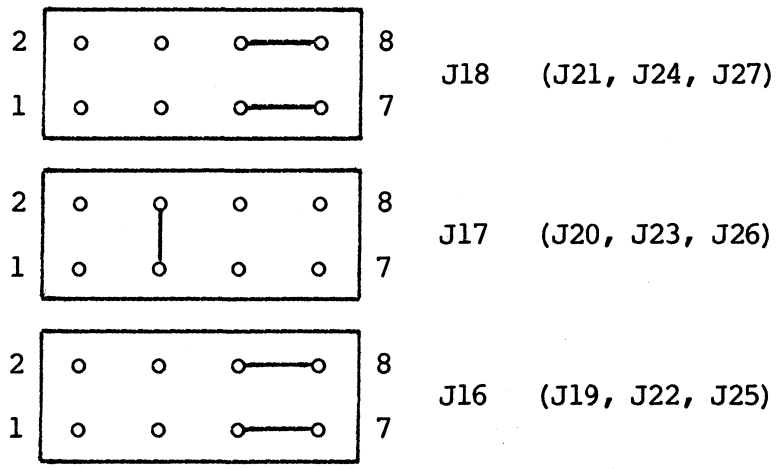


FIGURE 2-19. 2K x 8 ROM Standard Header Configurations

TABLE 2-17. 2K x 8 ROM Devices Optional Configuration, Headers J16-J27

HEADER NO. - PIN NO.	REMARKS
J16-5 to J16-8	Output enable (OE*) to P20 ($\overline{E}$)
J16-4 to J16-6	Socket pair select (SPn*) to P22 ($\overline{OE}$)
J17-3 to J17-4	P23U to P23L (VPP)
J18-5 to J18-7	+5V to P26 (VCC)
J18-6 to J18-8	+5V to P23U (VPP)

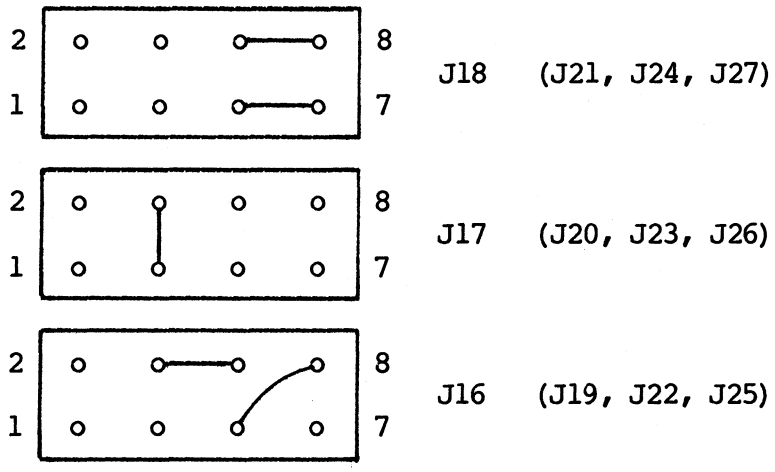


FIGURE 2-20. 2K x 8 ROM Optional Header Configurations

TABLE 2-18. 4K x 8 ROM Devices Standard Configuration, Headers J16-J27

HEADER NO. - PIN NO.	REMARKS
J16-3 to J16-5	Address line 12 (A12) to P20 (A11)
J16-4 to J16-6	Socket pair select (SPn*) to P22 ($\overline{E}$)
J17-3 to J17-4	P23U to P23L (VPP)
J18-5 to J18-7	+5V to P26 (VCC)
J18-6 to J18-8	+5V to P23U (VPP)

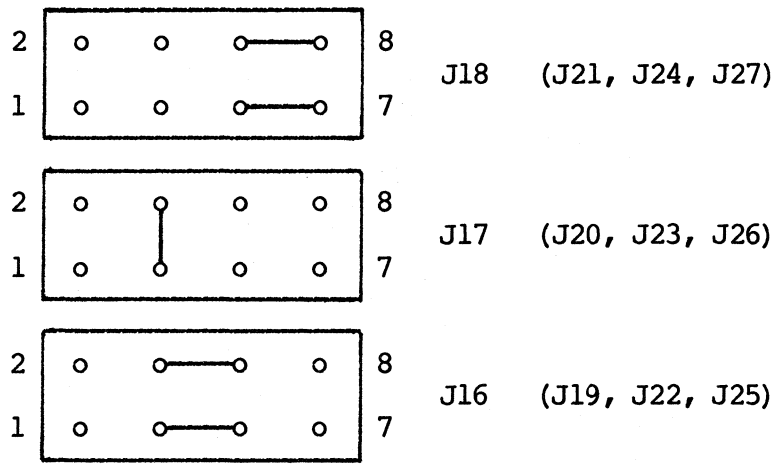


FIGURE 2-21. 4K x 8 ROM Standard Header Configurations

TABLE 2-19. 4K x 8 ROM Devices Optional Configuration, Headers J16-J27

HEADER NO. - PIN NO.	REMARKS
J16-3 to J17-2	Address line 12 (A12) to P23U (A11)
J16-4 to J16-6	Socket pair select (SPn*) to P22 ($\overline{OE}$)
J16-5 to J16-8	Output enable (OE*) to P20 ($\overline{CE}$)
J17-3 to J17-4	P23L to P23U (A11)
J18-5 to J18-7	+5V to P26 (VCC)

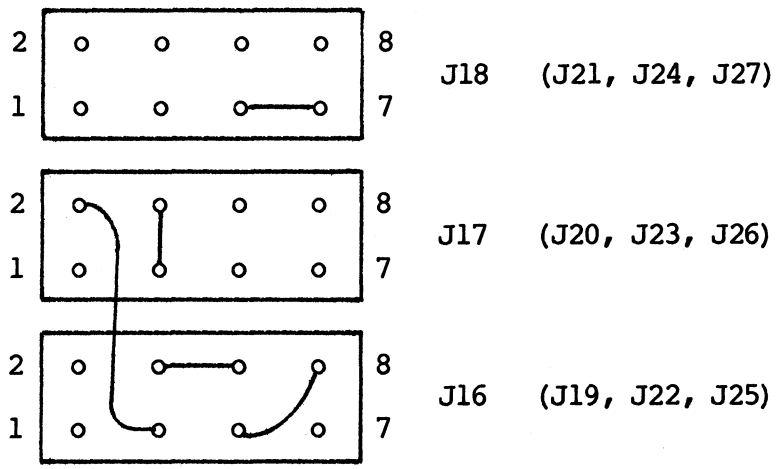


FIGURE 2-22. 4K x 8 ROM Optional Header Configurations

TABLE 2-20. 8K x 8 ROM Devices Standard Configuration, Headers J16-J27

HEADER NO. - PIN NO.	REMARKS
J16-3 to J16-5	Address line 12 (A12) to P20 (A11)
J16-4 to J16-6	Socket pair select (SPn*) to P22 ($\overline{E}$)
J17-1 to J17-2	Address line 13 (A13) to P23U (A12)
J17-3 to J17-4	P23U to P23L (A12)
J18-5 to J18-7	+5V to P26 (VCC)

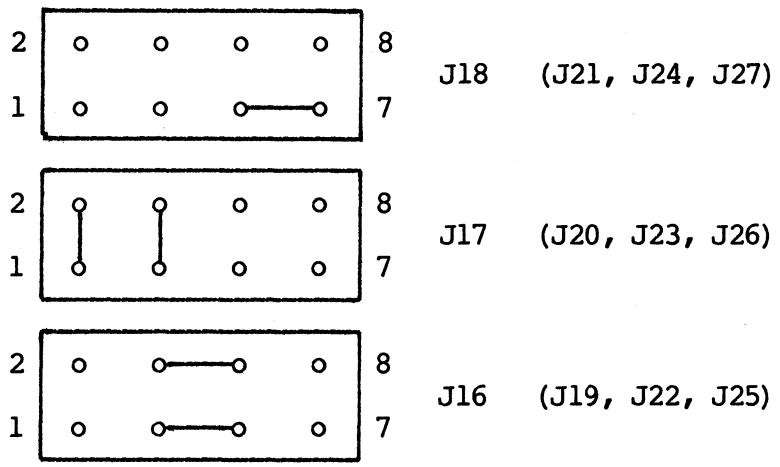


FIGURE 2-23. 8K x 8 ROM Standard Header Configurations

TABLE 2-21. 8K x 8 ROM Devices Optional Configuration, Headers J16-J27

HEADER NO. - PIN NO.	REMARKS
J16-2 to J17-1	Address line 13 (A13) to P2 (A12)
J16-3 to J17-2	Address line 12 (A12) to P23U (A11)
J16-4 to J16-6	Socket pair select (SPn*) to P22 ($\overline{OE}$)
J16-5 to J16-8	Output enable (OE*) to P20 ($\overline{CE}$)
J17-3 to J17-4	P23L (A11) to P23U (A11)
J17-7 to J17-8	P27L ($\overline{PGM}$) to P27U ($\overline{PGM}$)
J18-2 to J18-7	+5V to P27U ($\overline{PGM}$)
J18-4 to J18-6	+5V to P1 (VPP)

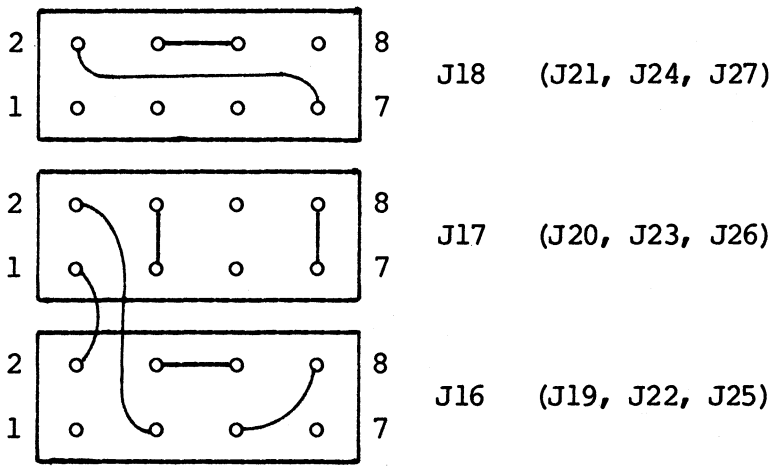


FIGURE 2-24. 8K x 8 ROM Optional Header Configurations

TABLE 2-22. 8K x 8 ROM Devices Optional Configuration, Headers J16-J27

HEADER NO. - PIN NO.	REMARKS
J16-2 to J16-4	Socket pair select (SPn*) to P2 ($\overline{CS}$)
J16-3 to J16-5	Address line 12 (A12) to P20 (A11)
J16-6 to J16-8	Output enable (OE*) to P22 ($\overline{CE}$)
J16-7 to J18-2	Socket pair select (SPn*) to P27U ($\overline{CS}$)
J17-1 to J17-2	Address line 13 (A13) to P23U (A12)
J17-3 to J17-4	P23L to P23U (A12)
J17-7 to J17-8	P27L to P27U ($\overline{CS}$)
J18-4 to J18-6	+5V to P1 (VPP)

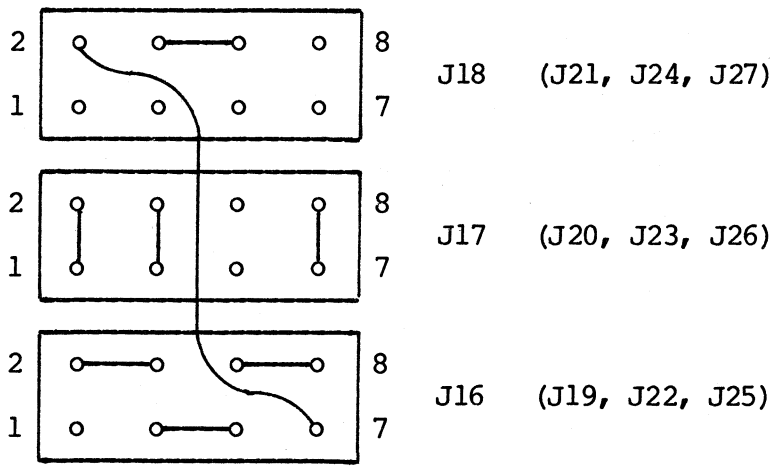


FIGURE 2-25. 8K x 8 ROM Optional Header Configurations

TABLE 2-23. 16K x 8 ROM Devices Optional Configuration, Headers J16-J27

HEADER NO. - PIN NO.	REMARKS
J16-2 to J17-1	Address line 13 (A13) to P2 (A12)
J16-3 to J17-2	Address line 12 (A12) to P23U (A11)
J16-4 to J16-6	Socket pair select (SPn*) to P22 ($\overline{OE}$)
J16-5 to J16-8	Output enable (OE*) to P20 ($\overline{CE}$)
J17-3 to J17-4	P23L (A11) to P23U (A11)
J17-7 to J17-8	P27L to P27U ($\overline{PGM}$)
J18-2 to J18-7	+5V to P27U ($\overline{PGM}$)
J18-3 to J18-5	Address line 14 (A14) to P26 (A13)
J18-4 to J18-6	+5V to P1 (VPP)

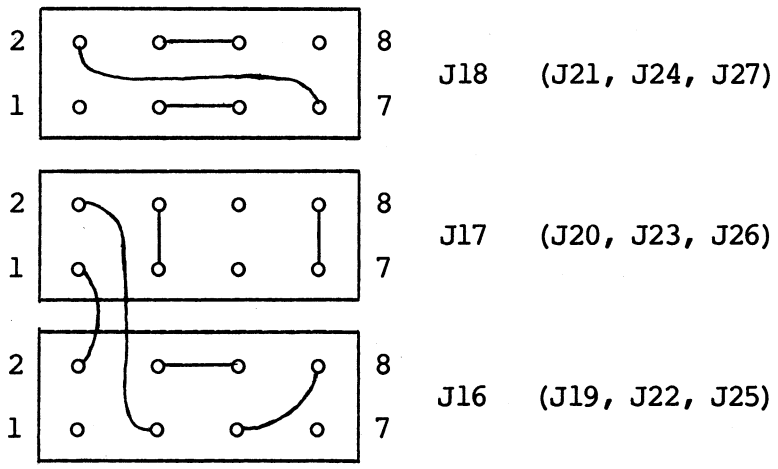


FIGURE 2-26. 16K x 8 ROM Optional Header Configurations

TABLE 2-24. 32K x 8 ROM Devices Optional Configuration, Headers J16-J27

HEADER NO. - PIN NO.	REMARKS
J16-2 to J17-1	Address line 13 (A13) to P2 (A12)
J16-3 to J17-2	Address line 12 (A12) to P23U (A11)
J16-4 to J16-6	Socket pair select (SPn*) to P22 ($\overline{OE}$)
J16-5 to J16-8	Output enable (OE*) to P20 ($\overline{CE}$)
J17-3 to J17-4	P23L to P23U (A11)
J17-7 to J17-8	P27L to P27U (A14)
J18-1 to J18-2	Address line 15 (A15) to P27U (A14)
J18-3 to J18-5	Address line 14 (A14) to P26 (A13)

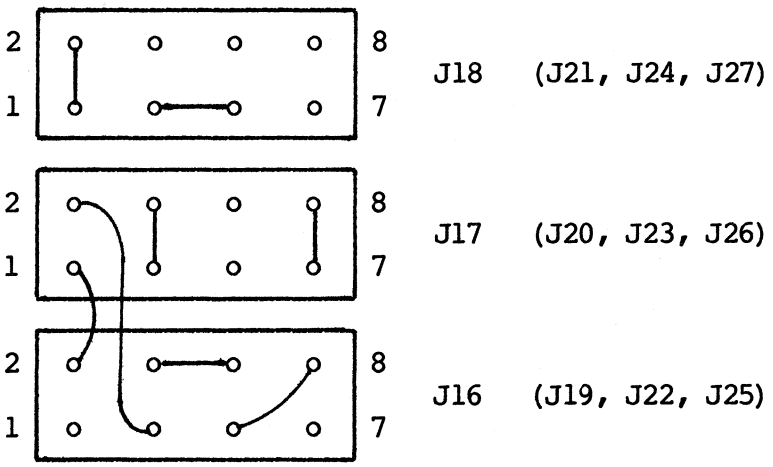


FIGURE 2-27. 32K x 8 ROM Optional Header Configurations

TABLE 2-25. 2K x 8 RAM Devices Standard Configuration, Headers J16-J27

HEADER NO. - PIN NO.	REMARKS
J16-5 to J16-7	Socket pair select (SPn*) to P20 ($\overline{CS}$)
J16-6 to J16-8	Output enable (OE*) to P22 ($\overline{OE}$)
J17-3 to J17-5	Write enable lower (WEL*) to P23L ($\overline{WE}$)
J17-4 to J17-6	Write enable upper (WEU*) to P23U ($\overline{WE}$)
J18-5 to J18-7	+5V to P26 (VCC)

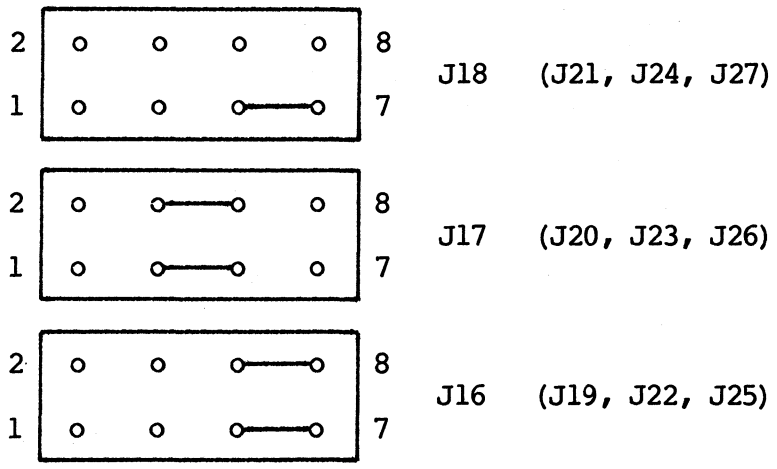


FIGURE 2-28. 2K x 8 RAM Standard Header Configurations

TABLE 2-26. 8K x 8 RAM Devices Optional Configuration, Headers J16-J27

HEADER NO. - PIN NO.	REMARKS
J16-2 to J17-1	Address line 13 (A13) to P2 (A12)
J16-3 to J17-2	Address line 12 (A12) to P23U (A11)
J16-5 to J16-7	Socket pair select (SPn*) to P20 ($\overline{CS1}$)
J16-6 to J16-8	Output enable (OE*) to P22 ($\overline{CE}$)
J17-3 to J17-4	P23L to P23U (A11)
J17-5 to J17-7	Write enable lower (WEL*) to P27L ($\overline{WE}$)
J17-6 to J17-8	Write enable upper (WEU*) to P27U ($\overline{WE}$)
J18-5 to J18-7	+5V to P26 (CS2)

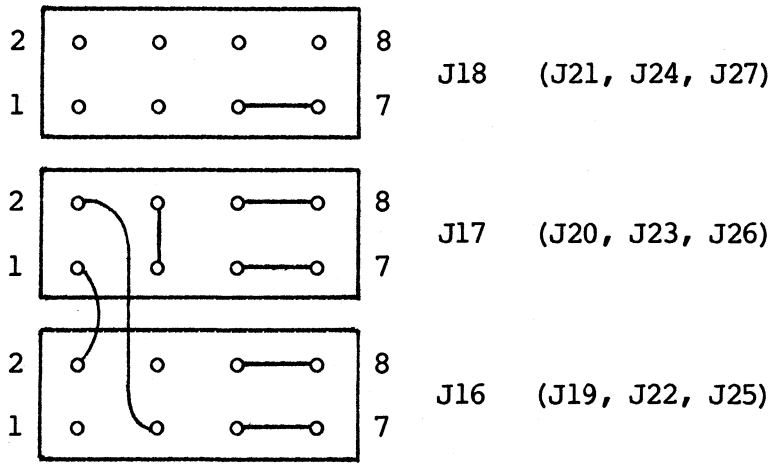


FIGURE 2-29. 8K x 8 RAM Optional Header Configurations

If a device type is to be used which is not listed in Table 2-15, the user must determine the jumpers to be installed. This can be done by mating the appropriate VME110 signal levels to the desired pins of the socket pair. Use Figure 2-30, the schematic diagrams in Figure 5-2, the memory device data sheet, and the local memory timing specifications (paragraphs 4.3.5.1 and 4.3.5.2) to aid in the determination of jumpers to be installed.

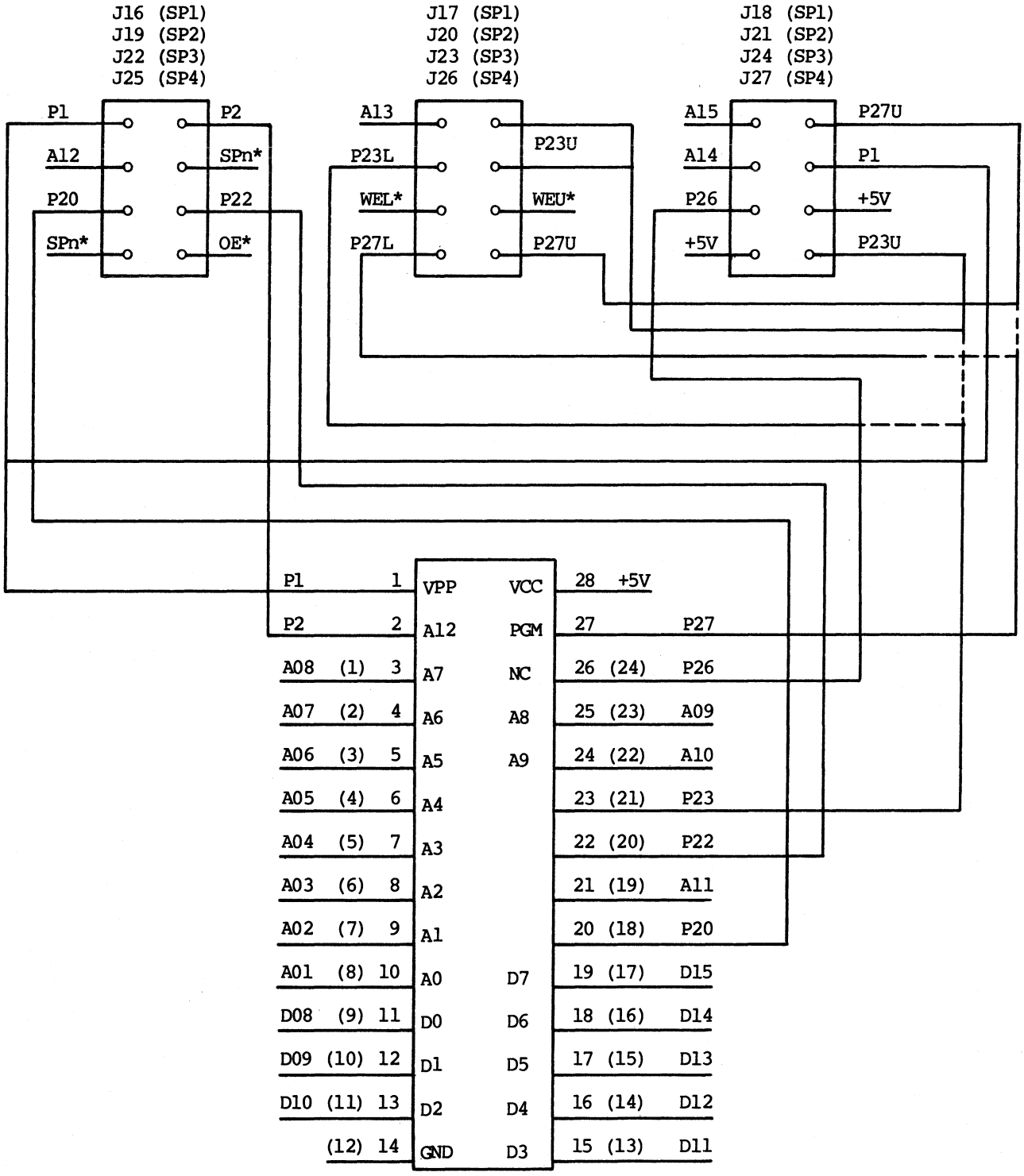


FIGURE 2-30. Memory Configuration Header Signals to Socket Pin Wiring

2.3.15 Programming the Map Decoder PROM (U23)

The Map Decoder PROM is a 512 x 4 bit memory device which is used to provide information regarding address locations which may be used for local memory. Because many different sizes and types of memory devices may be installed on the VME110, a flexible memory map decoding scheme is required.

Within the 16-megabyte memory map of the VME110, two blocks of addresses are allocated for possible use for local on-board memory devices. These blocks are designated as the LO BLOCK which encompasses addresses 000000 through 03FFFF and the HI BLOCK which includes address locations F00000 through F3FFFF. Addresses which are outside the LO BLOCK and HI BLOCK ranges may not be used to address local memory devices; however, if some of the LO BLOCK and HI BLOCK memory addresses are not needed for local memory devices, they may be used for off-board global (VMEbus) memory. The map decoder PROM provides information regarding each of the address locations which are within the LO BLOCK and HI BLOCK ranges. This information includes: whether the memory for a given address is contained in local or global memory, whether a local memory address is ROM or RAM, the socket pair which contains the local memory devices for local addresses, and whether a local memory RAM location is write-protectable by software. Each time a LO BLOCK or HI BLOCK memory address is generated, one of the 4-bit locations is read from the map decoder PROM. The 256K memory addresses in the LO BLOCK and the HI BLOCK are grouped into 2K segments. Each 2K segment is associated with two 4-bit map decoder PROM locations (even and odd). Figure 2-31 demonstrates the relationship between the map decoder even/odd pairs and the 2K segments of the LO BLOCK and HI BLOCK memory addresses. Each location of the map decoder PROM must be programmed by the user to provide the necessary information regarding the 2K segment which it represents. Each map decoder PROM location contains a hex code that specifies which socket pair contains that 2K segment.

The odd location is used to select the memory during supervisory mode. When a zero is written into bit 7 of the module control register, the even PROM locations are used to select the 2K segments. This is called the WRITE PROTECT mode. When in this mode, certain 2K segments (determined by the even locations of the map) cannot be written unless the processor is in the supervisor state.

Figure 2-32 illustrates how the memory devices in the 28-pin sockets appear in the VME110 memory map. The double column at the left shows the pairs (even and odd) of decoder PROM locations which correspond to each 2K segment of memory.

When 2K x 8 memory chips are installed in the 28-pin sockets, they appear as shown in the column labeled "2K". Each box represents one socket pair and occupies 4K of the memory map (2K x 2 chips = 4K). Note that each box begins on a 4K boundary. Any of the four socket pairs may be placed in any of the 4K boxes by programming the appropriate hex codes into the decoder PROM locations in the left-most column (see Table 2-27).

When the 4K memory chips are installed in the sockets, they may be placed in any of the boxes in the third column. In a similar manner, 8K, 16K, and 32K chips can be accommodated.

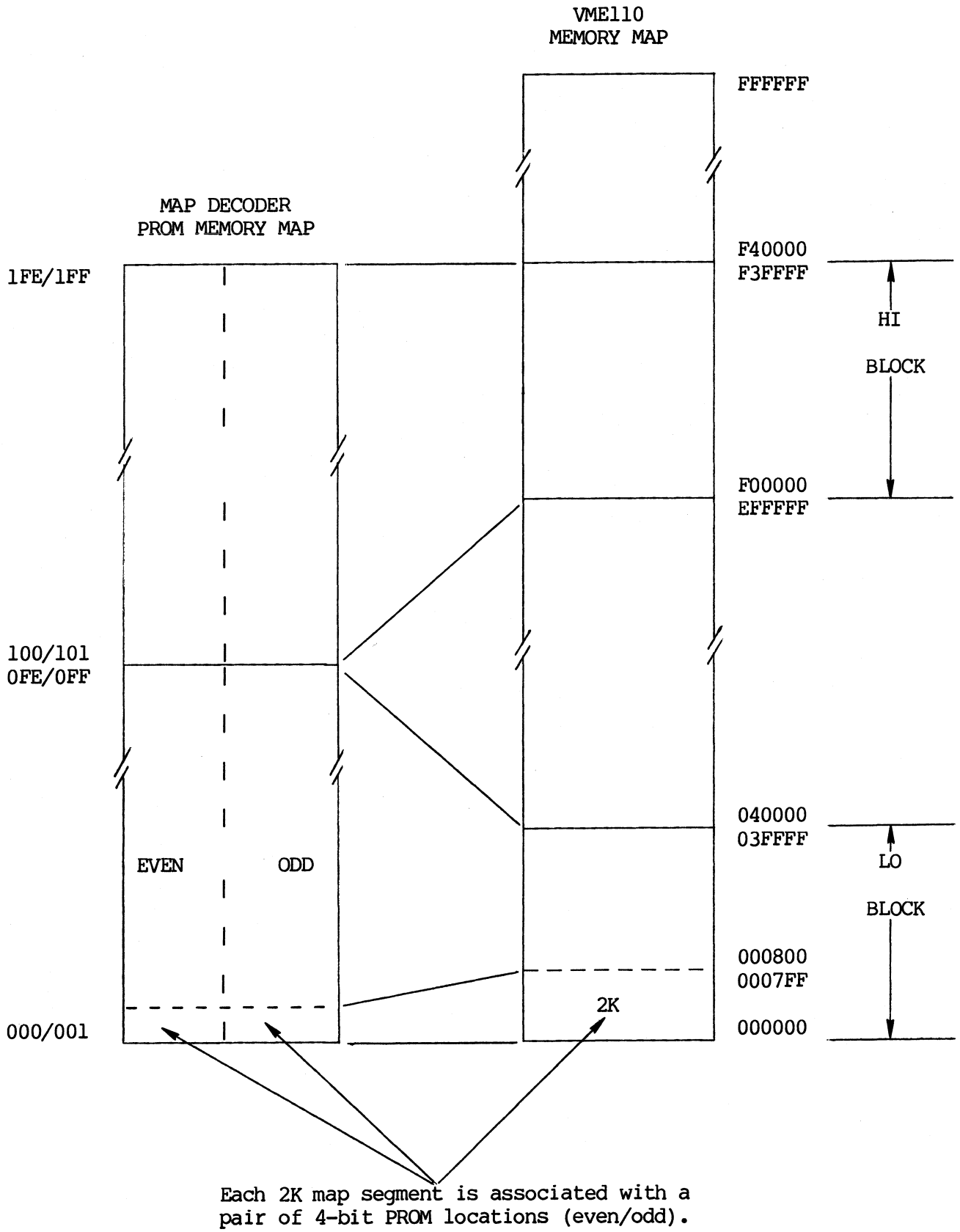


FIGURE 2-31. Relationship of Map Decoder PROM Addresses to VME110 Memory Map

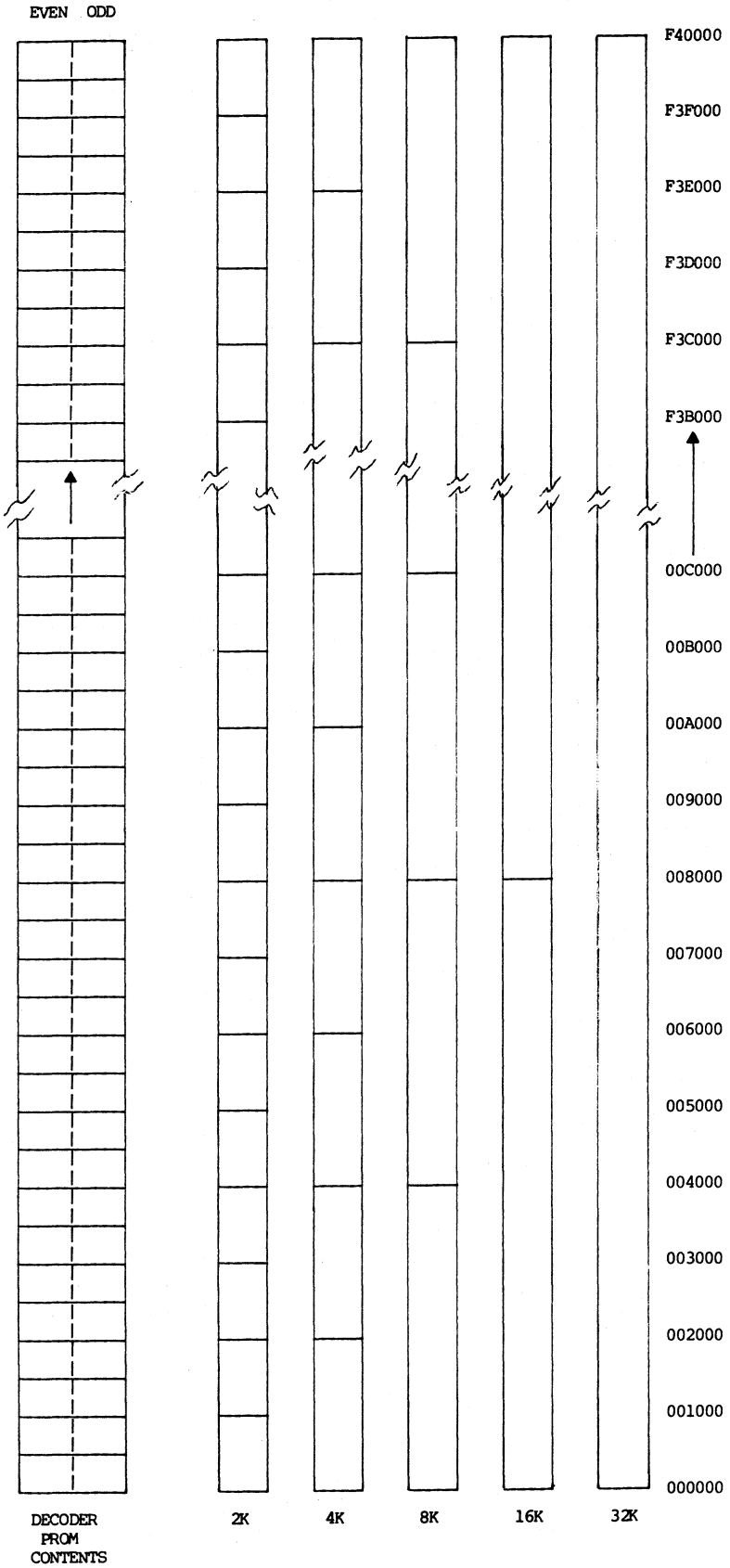


FIGURE 2-32. VME110 Memory Map Address Assignments

TABLE 2-27. Map Decoder PROM Hex Codes

HEX CODE	SELECTED DEVICE
0	Illegal
1	RAM in socket pair 2
2	RAM in socket pair 3
3	RAM in socket pair 4
4	Illegal
5	WRITE PROTECTED RAM in socket pair 2
6	WRITE PROTECTED RAM in socket pair 3
7	WRITE PROTECTED RAM in socket pair 4
8	PROM in socket pair 1
9	PROM in socket pair 2
A	PROM in socket pair 3
B	PROM in socket pair 4
C	VMEbus
D	VMEbus
E	VMEbus
F	VMEbus

NOTE: Codes 0 and 4 are illegal because RAM may not be installed in socket pair 1. (The processor reads the power-on vector from the PROM's in these sockets.)

Memory chips of different sizes may be used as long as each socket pair contains a matching set. Illustrated in Figure 2-33 is an example configuration which has 8K ROM chips installed in socket pair 1, 4K ROM chips in socket pair 3, and 2K RAM chips in socket pairs 2 and 4. In this case, the memory chips have been arranged so that they form a contiguous 32K block of memory. The two 8K ROM chips in socket pair 1 are placed at the lowest address by programming a hexadecimal "8" into the corresponding decoder PROM locations. The 4K PROM's are placed with hexadecimal "9". The 2K RAM's in socket pair 2 correspond to a hexadecimal 1, and the write protected 2K RAM's in socket pair 4 correspond to the hex codes of "7" and "3".

Because the rest of the local memory block is not needed, the decoder PROM locations are programmed with a hex "F". This causes the board to access the VMEbus whenever that area of the map is addressed. If there is a memory board on the VMEbus which contains that address, it will be contiguous with the local memory.

It should be noted that the socket pairs do not necessarily appear in the map in order (socket pairs 1, 3, 2, 4). The placement of the chips into the 28-pin socket pairs does not govern their placement in the memory map. There are some restrictions, however. In the example just described, if the user wanted to rearrange the chips in the order 1, 2, 3, 4, he would run into difficulty. This is because the 8K of memory in socket pair 3 has to be placed on a 4K boundary. Therefore, it could not be contiguous with the 4K of memory in socket pair 2 below it in the memory map.

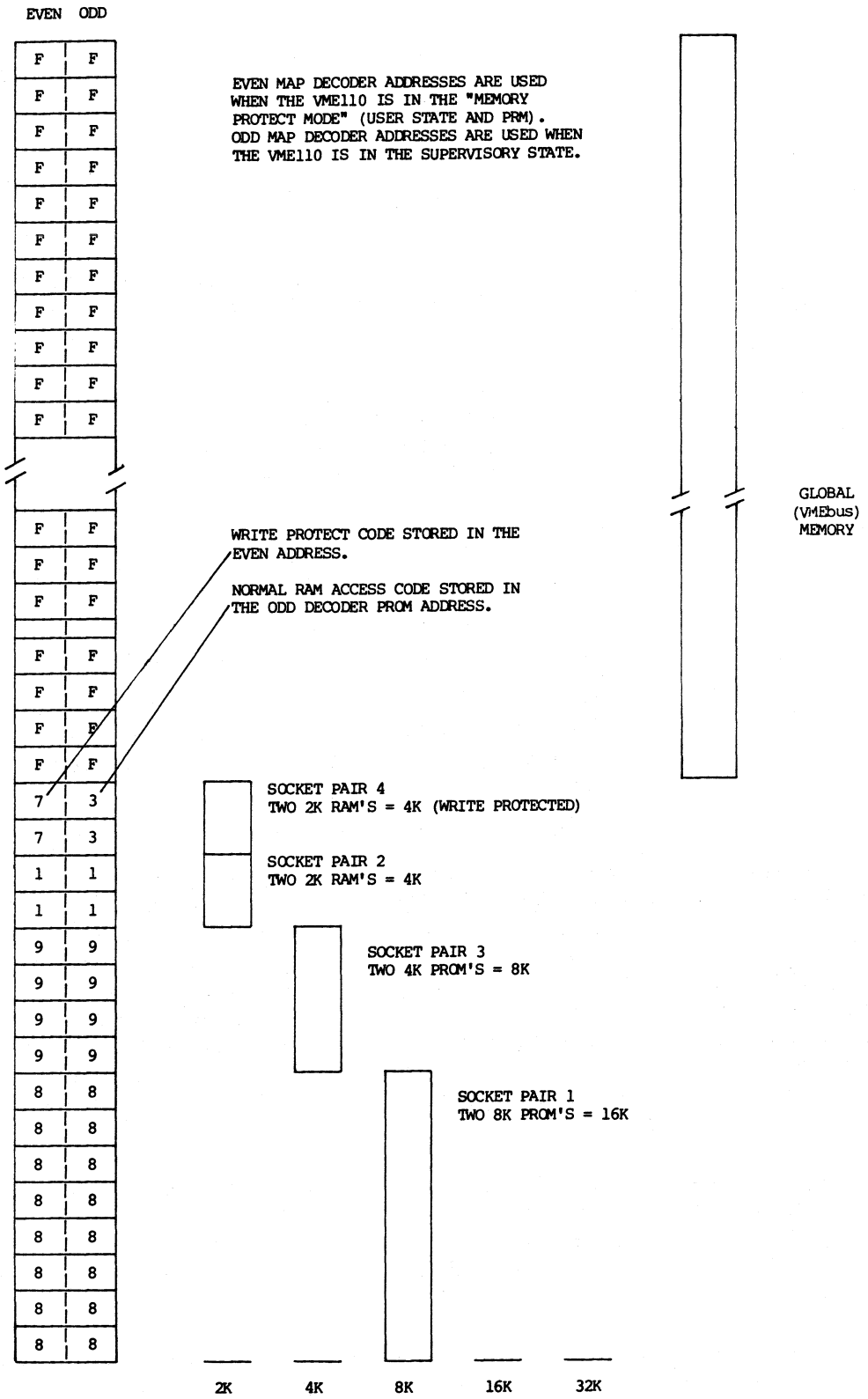
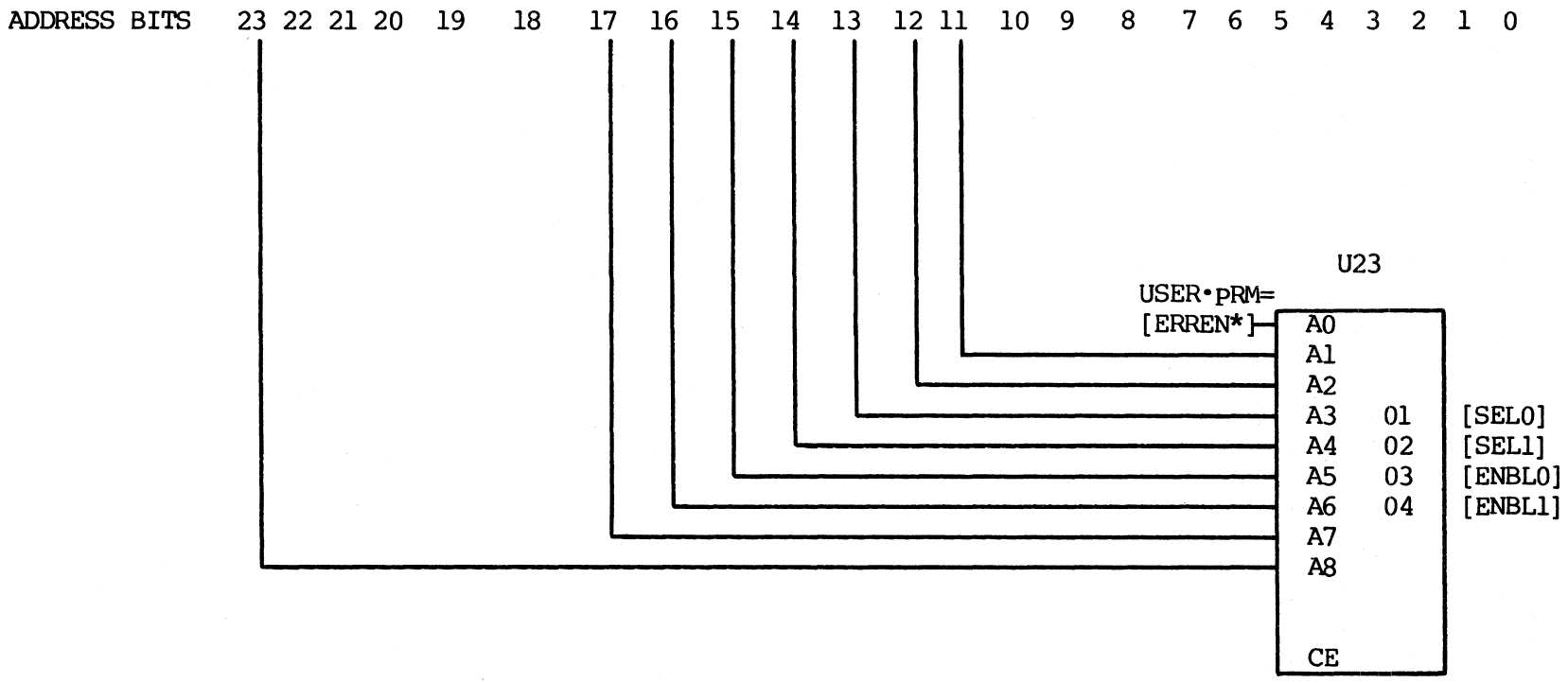


FIGURE 2-33. Map Decoder PROM Example

Another restriction is that RAM may never be placed in socket pair 1. This is because the processor reads the restart vector from socket pair 1, regardless of where it appears in the memory map.

In some cases, the user may want a socket pair to appear two or more places in the map. This can be done by simply programming the decoder PROM with the same hex code in all the appropriate places.

Figure 2-34 illustrates the addressing of the map decoder PROM and the meanings of its outputs. Address line A23 is used to distinguish between the LO BLOCK and HI BLOCK. Address lines A11-A17 select one of the 128 2K segments within each block. The USER•PRM input to A0 of the PROM causes it to output the contents of the even address whenever the memory protect bit (bit 7 of the MCR) is set to zero and the processor is in the user state.



[ENBL1]	[ENBL0]		[SEL1]	[SEL0]	
0	0	LOCAL RAM	0	0	SOCKET PAIR 1 (SP1)
0	1	LOCAL WP RAM	0	1	SOCKET PAIR 2 (SP2)
1	0	LOCAL ROM	1	0	SOCKET PAIR 3 (SP3)
1	1	VME MEMORY	1	1	SOCKET PAIR 4 (SP4)

FIGURE 2-34. Map Decoder PROM Addressing and Meanings of Outputs

EXAMPLE

1. Determine local RAM and ROM memory requirements.

   8K RAM, 24K ROM

2. Select appropriate memory devices and specify the socket pairs into which they will be installed.

   Two 8K x 8 ROM's in socket pair 1
   Two 4K x 8 ROM's in socket pair 2
   Two 2K x 8 RAM's in socket pair 3
   Two 2K x 8 RAM's in socket pair 4

3. Specify the base addresses and address range for each socket pair. Devices should be placed on boundaries equal to their size --i.e., 8K devices on 16K address boundaries, etc.

   Socket pair 1 address $F00000-$F03FFF
   Socket pair 2 address $F04000-$F05FFF
   Socket pair 3 address $000000-$000FFF
   Socket pair 4 address $001000-$001FFF

4. If RAM is to be write-protectable, specify the address range to be write-protected. Write protection must be on 2K segment boundaries.

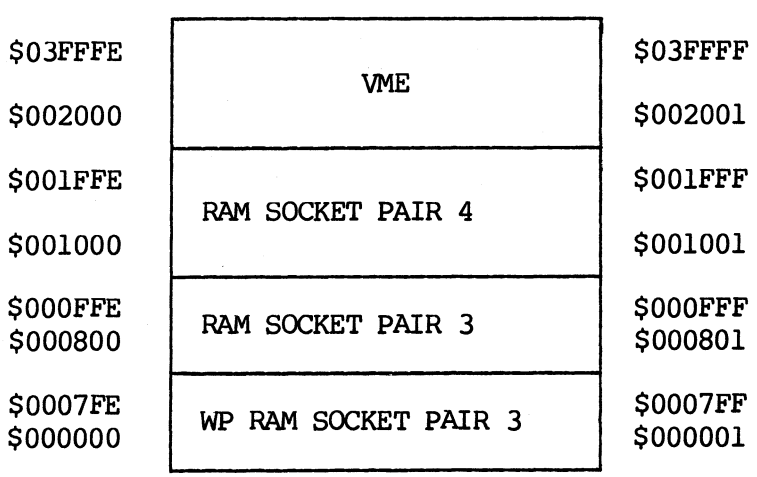
   2K of RAM is to be write-protectable; address range $000000-$0007FF

5. Specify all remaining unused addresses within the LO and HI blocks.

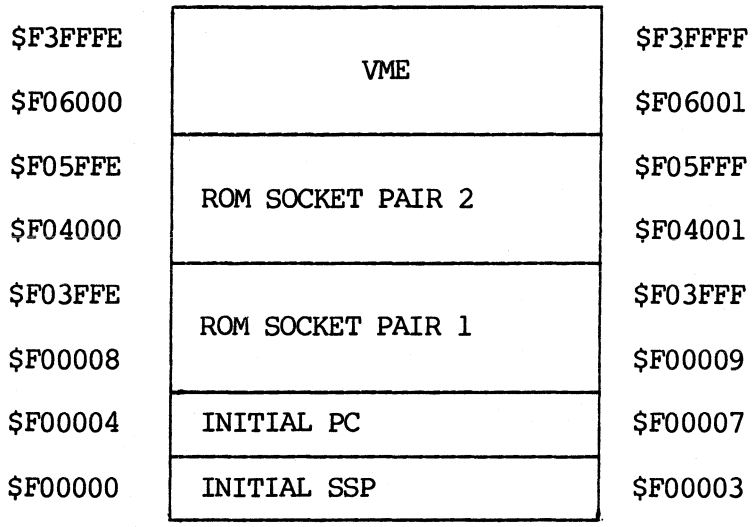
   Unused LO BLOCK addresses from $002000-$03FFFF assigned as VME addresses.
   Unused HI BLOCK addresses from $F06000-$F3FFFF assigned as VME addresses.

6. Make a memory map of the LO and HI blocks showing socket pair locations, RAM write-protectable locations, and VME locations.

7. Determine the map decoder PROM addresses which correspond to each 2K segment of the memory map.



HI BLOCK



7. Referring to the memory maps above, insert the appropriate PROM output codes for the LO and HI blocks in the programming sheet, as illustrated in Figure 2-35.

8. Program the blank 82S131 PROM supplied with the VME110 according to the programming sheets and install at location U23 of the VME110.

In the above example, the MPU will fetch the initial SSP and PC from addresses F00000-F00007 because the RESET vector is always fetched from the ROM in socket pair 1. After this initial fetching, RAM will always appear at address 0-7. Addresses 0-7FF may be protected from any write attempts in the user state by setting the protect mode in the MCR. This will protect the MPU exception vector table and can be used to protect the Supervisor stack area, as well as operating system program and data. When the MPU addresses a device in the LO block above 1FFF or in the HI block above F05FFF, the cycle will be directed to the VMEbus. If a VME memory card is installed at one of these addresses, it will be contiguous with local memory.

LO 256K BLOCK

2K SEGMENT	BEGINNING ADDRESS / ENDING ADDRESS	0 7FF	800 FFF	1000 17FF	1800 1FFF	2000 27FF	2800 2FFF	3000 37FF	3800 3FFF	
MPU ADDRESS	PROM ADDRESS	WP 0 1	WP 2 3	WP 4 5	WP 6 7	WP 8 9	WP A B	WP C D	WP E F	
0-3FFF	0	6 | 2	2 | 2	3 | 3	3 | 3	F | F	F | F	F | F	F | F	0-16K
4000-7FFF	10	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	16K-32K
8000-BFFF	20	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	32K-48K
C000-FFFF	30	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	48K-64K
10000-13FFF	40	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	64K-80K
14000-17FFF	50	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	80K-96K
18000-1BFFF	60	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	96K-112K
1C000-1FFFF	70	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	112K-128K
20000-23FFF	80	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	128K-144K
24000-27FFF	90	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	144K-160K
28000-2BFFF	A0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	160K-176K
2C000-2FFFF	B0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	176K-192K
30000-33FFF	C0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	192K-208K
34000-37FFF	D0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	208K-224K
38000-3BFFF	E0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	224K-240K
3C000-3FFFF	F0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	240K-256K

FIGURE 2-35. Map Decoder PROM Programming Sheet Example (Sheet 1 of 2)

HI 256K BLOCK

2K SEGMENT	BEGINNING ADDRESS / ENDING ADDRESS	0 7FF	800 FFF	1000 17FF	1800 1FFF	2000 27FF	2800 2FFF	3000 37FF	3800 3FFF	
MPU ADDRESS	PROM ADDRESS	WP 0 1	WP 2 3	WP 4 5	WP 6 7	WP 8 9	WP A B	WP C D	WP E F	15M +
F00000-F03FFF	100	8 | 8	8 | 8	8 | 8	8 | 8	8 | 8	8 | 8	8 | 8	8 | 8	0-16K
F04000-F07FFF	110	9 | 9	9 | 9	9 | 9	9 | 9	F | F	F | F	F | F	F | F	16K-32K
F08000-F0BFFF	120	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	32K-48K
F0C000-F0FFFF	130	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	48K-64K
F10000-F13FFF	140	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	64K-80K
F14000-F17FFF	150	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	80K-96K
F18000-F1BFFF	160	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	96K-112K
F1C000-F1FFFF	170	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	112K-128K
F20000-F23FFF	180	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	128K-144K
F24000-F27FFF	190	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	144K-160K
F28000-F2BFFF	1A0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	160K-176K
F2C000-F2FFFF	1B0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	176K-192K
F30000-F33FFF	1C0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	192K-208K
F34000-F37FFF	1D0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	208K-224K
F38000-F3BFFF	1E0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	224K-240K
F3C000-F3FFFF	1F0	F | F	F | F	F | F	F | F	F | F	F | F	F | F	F | F	240K-256K

FIGURE 2-35. Map Decoder PROM Programming Sheet Example (Sheet 2 of 2)

2.4 UPGRADING THE VME110 FROM 8 MHz TO 10 MHz

The standard 8 MHz VME110 may be modified to operate with a 10 MHz MPU. This section contains a step-by-step procedure to accomplish the modification.

2.4.1 Materials Required

- MC68000L10 - Motorola 68000 16-bit microprocessing unit
- K1116A - 20 MHz Crystal Oscillator (frequency tolerance must be within 1%)

2.4.2 Procedure

a. Remove the MC68000L8 MPU from location U4 of the VME110 (see Figure 5-1).

b. Remove the 48AW1016B01, 16 MHz crystal oscillator from location Y1 of the VME110 (see Figure 5-1).

c. Install MC68000L10 MPU in location U4 of the VME110 (see Figure 5-1).

d. Install K1116A, 20 MHz crystal oscillator in location Y1 of the VME110 (see Figure 5-1).

e. Reconfigure MPU clock speed header J1 (refer to paragraph 2.3.1).

f. If this module was previously the system controller, reconfigure header J8 (refer to paragraph 2.3.7).

NOTE

A 10-MHz VME110 may not be used as the system controller because it cannot supply the 16-MHz system clock to the VMEbus.

The 16 MHz system clock signal SYSCLK must be supplied to the VMEbus by another VME110 which is operating at 8 MHz and is configured as the system controller, or by a similar VMEmodule connected to the VMEbus.

g. Reconfigure the ROM access time select header J9 (refer to paragraph 2.3.8).

h. Reconfigure the RAM access time select header J10 (refer to paragraph 2.3.9).

i. Proceed to paragraph 2.5.

2.5 MODULE INSTALLATION

This section describes how to install the VME110 for system operation. Before making any connections to the VME110, ensure all system devices have power off.

CAUTION

INSERTING/REMOVING MODULES WHILE POWER IS APPLIED COULD RESULT IN DAMAGE TO MODULE COMPONENTS.

AVOID TOUCHING AREAS OF MOS CIRCUITRY; STATIC DISCHARGE CAN DAMAGE INTEGRATED CIRCUITS.

Ensure that local memory ROM and RAM is installed and configured, the map decoder PROM is programmed, and all the remaining VME110 headers are configured (refer to paragraph 2.3).

One or more VME110's may be installed in a VMEmodule chassis.

2.5.1 Installation Procedure

If only one VME110 is to be used, configure it as the system controller (refer to paragraph 2.3.7) and install it in slot A01 of the VMEmodule chassis card rack. If a second VME110 is to be used, install it in any other available VMEbus slot in the same chassis. The second VME110 must not be configured as the system controller (refer to paragraph 2.3.7). The VME110 in slot A01 should be configured as the system controller.

2.5.2 VMEmodule Chassis Backplane Daisy-Chain Jumpers

Whenever there are any empty slots between boards in the VMEmodule chassis, jumpers must be installed on the VMEmodule backplane at the empty slot locations to jumper the bus arbitration signals and acknowledge signals across the empty slot(s). Refer to Table 2-28 for a list of the backplane pins to be daisy-chained across the empty slot(s).

TABLE 2-28. VMEmodule Backplane Empty Slot Daisy-Chained Jumpers

BACKPLANE PIN NO.			REMARKS		
A21	to	A22	IACKIN*	to	IACKOUT*
B4	to	B5	BG0IN*	to	BG0OUT*
B6	to	B7	BG1IN*	to	BG1OUT*
B8	to	B9	BG2IN*	to	BG2OUT*
B10	to	B11	BG3IN*	to	BG3OUT*

2.5.3 VMEbus Connection

Connection to the VMEbus is made when the VME110 is installed, by the mating of the DIN 41612 triple-row, 96-pin, P1 connector to the VMEmodule chassis backplane (refer to paragraph 5.2.1).

2.5.4 I/O Channel Connection

Connection to the I/O Channel is made when the VME110 is installed, by the mating of the DIN 41612 double-row, 64-pin, P2 connector to an I/O Channel backplane or ribbon cable (refer to I/O Channel specifications manual, Motorola publication number M68RIOCS).

2.5.5 Terminal Connection

Terminal connection is accomplished by mating a 25-pin, RS-232C cable to plug J15 on the VME110 and connecting the other end of the cable to an RS-232C compatible terminal or host configured as a data terminal (DTE).

CHAPTER 3

OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides the necessary information to initialize and use the VMEmodule Monoboard Microcomputer (VME110) in a system configuration.

3.2 OPERATING CONTROLS AND INDICATORS

The VME110 contains two pushbutton switches (RESET and ABORT) and three LED indicators (RUN, HALT, and FAIL).

3.2.1 RESET Pushbutton

The RESET pushbutton is enabled by a jumper between pins 1 and 2 of header J7. When enabled, depression of the RESET pushbutton causes the timing and control circuits of the VME110 to be reset to the initialized state by a board-level reset.

The I/O channel reset signal IORES* is generated to the I/O channel interface. If the VME110 is the system controller, pins 1 and 2 of header J8 should be connected by a jumper. This enables the board-level reset signal [RSTOUT] to generate the system reset signal SYSRESET* which is sent via the VMEbus to the other modules in the system (see Figure 4-2).

3.2.2 ABORT Pushbutton

The ABORT pushbutton is enabled by a jumper between pins 3 and 4 of header J7. When enabled, depression of the ABORT pushbutton causes a level 7 non-maskable interrupt to the MC68000 Microprocessor Unit (MPU). The user-provided software may then be used to perform appropriate actions to restore the system to a known state.

3.2.3 RUN Indicator

The RUN indicator is illuminated whenever the VME110 is not in the halt state.

3.2.4 HALT Indicator

The HALT indicator is illuminated whenever the VME110 is in the halt state. The halt state is entered temporarily by a board-level reset from the RESET push-button, by the system reset SYSRESET*, or by a reset initiated by the watchdog timer, and will leave the halt state after the reset signal is terminated. If a double-bus fault occurs, the processor will enter the halt state and remain there until the reset is activated and then released.

3.2.5 FAIL Indicator

The FAIL indicator is controlled by bit 4 in the Module Control Register (MCR). It is illuminiated when the software sets bit 4 in the MCR to a logic "1", or by a reset of the VME110. The FAIL indicator can be extinguished only when software resets bit 4 of the MCR.

3.3 OPERATING PROCEDURE

The following is a typical procedure which explains how to use the VME110 in a system environment.

a. Apply power to the VME110. The power-up reset will cause the HALT and FAIL indicators to illuminate. After the reset, the VME110 enters the run mode. The HALT indicator is extinguished and the RUN indicator illuminated. The System Stack Pointer (SSP) and initial Program Counter (PC) values are fetched from the first eight byte locations of the ROM contained in socket pair 1. The MPU begins processing at the address specified by the PC. The FAIL indicator remains illuminated until the user-supplied software resets bit 4 in the MCR.

b. If a terminal is connected to the serial I/O port J15, apply power to the terminal.

c. If the VME110 contains VMEbug and a terminal is connected to the serial I/O port, the terminal can be used to communicate with the VME110. Refer to the VMEbug Debugging Packages User's Manual (Motorola publication number MVMEBUG).

d. The ABORT pushbutton may be depressed on the VME110 to recover from system hang-ups, abnormal program loops, etc. to return the system to an orderly state. The ABORT pushbutton causes a level 7 non-maskable interrupt to the MPU. The user-supplied interrupt routine should safe-store the MPU working registers and any other pertinent data for future diagnosis.

e. Remove power from the VME110 after operations have been completed.

f. Remove power from the terminal if one was in use.

CHAPTER 4

FUNCTIONAL DESCRIPTION

4.1 INTRODUCTION

This chapter describes the VME110 in general, as well as functional descriptions of each section and various modes of operation.

4.2 GENERAL DESCRIPTION

The VME110 is a complete microcomputer module which contains memory and input/output, as well as control functions. The simplified block diagram for the VME110 is shown in Figure 4-1.

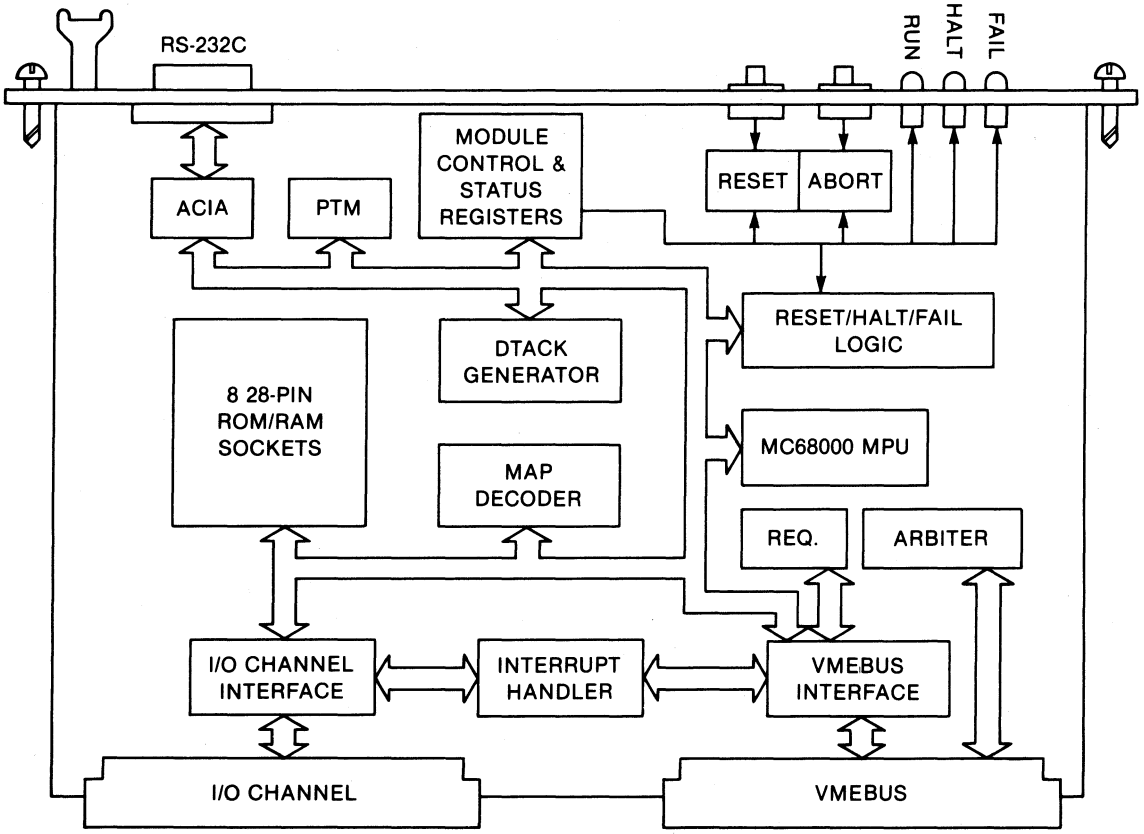


FIGURE 4-1. VME110 Simplified Block Diagram

4.2.1 Local Memory

The 28-pin ROM/PROM/EPROM and RAM sockets, with proper jumper selection, permit the use of 24-pin 2K, 4K and 8K compatible devices as well as 28-pin 8K, 16K, and 32K-byte devices. Asynchronous Data Transfer Acknowledge (DTACK) response time jumper selection is provided to permit the use of a full range of memory device speeds. The local on-board RAM is write-protectable from user state programs on 2K segment boundaries. Local RAM is not accessable from the VMEbus. When 2K segments of RAM are configured as programmable write protect RAM, the on-board MPU may write protect any of these segments, when in the user state, under software control via bit 7 of the Module Control Register (MCR).

4.2.2 Local Bus

The VME110 employs the Motorola MC68000 16-bit microprocessor operating at 8 MHz or 10 MHz. The local bus provides the interconnection of the MPU with ROM, RAM, the serial I/O port, the I/O Channel, the Programmable Timer Module (PTM), and the status and control registers. The local bus allows the VME110 processing to continue at full speed, while another VMEbus master operates simultaneously.

4.2.3 VMEbus Interface

The VMEbus interface is incorporated in the VME110 to allow its use in a high-performance system which requires off-board resources such as other microcomputer modules, external RAM, and intelligent I/O controllers. VMEbus is characterized by asynchronous, bidirectional operation and multiprocessor system operation. The VMEbus interface supports the full 16-megabyte address range of the MPU. The MPU gains access to the VMEbus upon becoming bus master via Bus Request lines (BR0*-BR3*). The priority level of the bus request is jumper selectable to one of four levels. After bus mastership has been granted, the manner in which it is released is determined by the bus release control bits in the MCR.

The VME110 monitors the VMEbus ACFAIL line. This allows user-provided power-up and power-down firmware routines to perform system-wide activities, such as storing critical data in non-volatile RAM in the event of a power-down condition.

4.2.4 System Controller

The VME110 may be configured as the system controller to provide the following system management and control functions.

- Single-level VMEbus artibration - When configured as the system controller, VME110 accepts bus requests on level 3 and issues a bus grant on the BG3IN*/BG3OUT* daisy-chain.
- System clock - When configured for 8 MHz processor clock speed, a 16 MHz clock signal is provided to other VMEbus modules.
- Reset - Upon reset, VME110 drives the SYSRESET* line on the VMEbus if the VME110 is acting as the system controller.
- Bus time-out - Generates a Bus Error (BERR*) when a non-existent or non-responding device is addressed on the VMEbus. Time-out is selectable for 200 microseconds or OFF.

System controller functions are normally provided by one VME110 plugged into the VMEbus backplane. If more than one VME110 is used in a multiprocessor system, only one may be configured as the system controller.

4.2.5 I/O Channel

The I/O Channel allows the user to connect multiple I/O extension boards. The I/O Channel interface lines are available on connector P2.

4.2.6 Serial I/O Port

The RS-232C serial I/O port allows the user to connect a terminal for display and operator dialog with the VME110. Data and control lines for the serial I/O port interface are available on connector J15. The Asynchronous Communication Interface Adapter (ACIA) provides the interface and control between the MPU and the serial I/O port.

4.3 DETAILED DESCRIPTIONS

4.3.1 Processor

The processor section of the VME110 consists of the MC68000 MPU, clock oscillator, reset logic, and front panel pushbutton and indicator logic. The clock oscillator provides the MPU clock and may also be jumpered to provide the VMEbus system clock. The reset logic controls the various types of resets associated with the board. Figure 4-2 illustrates the VME110 reset structure. The front panel LED indicators indicate the following conditions when they are illuminated.

FAIL - FAIL bit in MCR is a logic "1".

HALT - MPU is halted as a result of a reset or double bus fault.

RUN - MPU is running.

4.3.2 Local Memory

Eight 28-pin sockets are provided for user-installed ROM/PROM/EPROM and RAM memory devices. The devices are installed in pairs and configured by headers J16 through J27 (refer to paragraph 2.3.14). Socket pair 1 must contain ROM devices.

For the first four MPU cycles after power is applied, or a system/board reset, data is fetched from the first eight byte locations of the ROM contained in socket pair 1 regardless of the addresses assigned. Therefore, the first eight bytes of ROM in socket pair 1 should contain the initial stack pointer value which is loaded into the Supervisor Stack Pointer (SSP) register and the starting address of the target program, which is loaded into the Program Counter (PC).

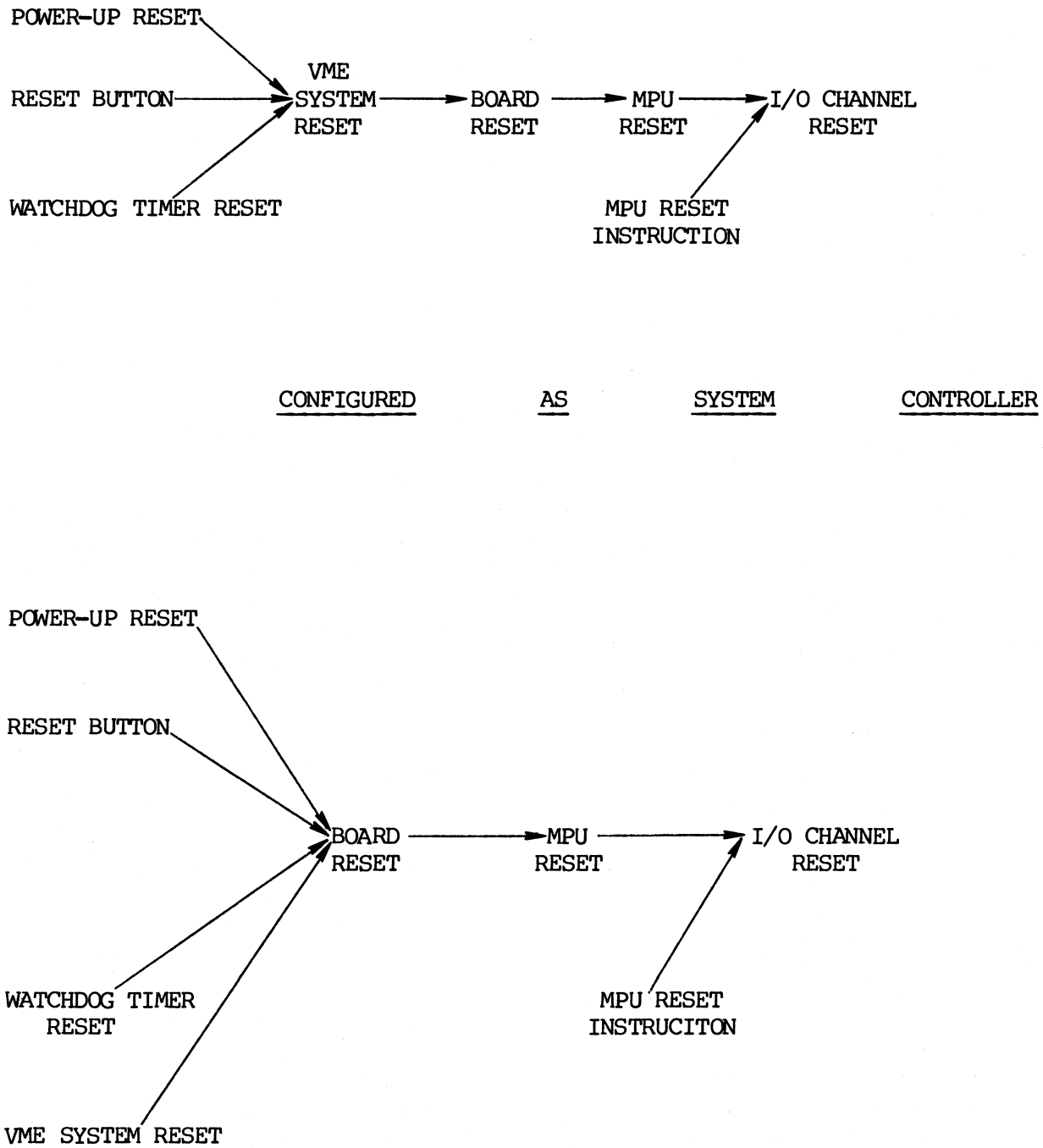


FIGURE 4-2. VME110 Reset Structure

4.3.3 Memory Map Decode

The memory map decode logic is responsible for selecting and controlling the various devices on the VME110. At the start of each MPU cycle, the map decoder first determines the cycle to be either reset, interrupt acknowledge, or normal.

- Reset - for the first four cycles after reset, the ROM devices installed in socket pair 1 are selected.

- Interrupt Acknowledge - the interrupt handler circuitry is selected to determine the interrupt group to be acknowledged.

- Normal - the normal cycles are further decoded into the following: (refer to memory map Figure 4-3)

    a. Local Memory - the local memory map decode PROM U23 determines certain actions to be taken as programmed by the user. (Refer to paragraph 2.3.15)

    b. VME - for addresses specified as VME, the requester is signaled by the map decoder to obtain VMEbus mastership. After bus mastership has been granted, the VME interface circuitry is selected. (refer to paragraph 4.3.9)

    c. LOCAL I/O - a synchronous cycle is initiated and one of the following devices is selected; ACIA, PTM, MCR, or MSR.

    d. I/O Channel - the I/O Channel interface circuitry is selected.

4.3.4 Local I/O

Outlined in Table 4-1 are the memory map addresses which are associated with the PTM and the ACIA. These memory map addresses are reserved for addressing the corresponding on-board hardware.

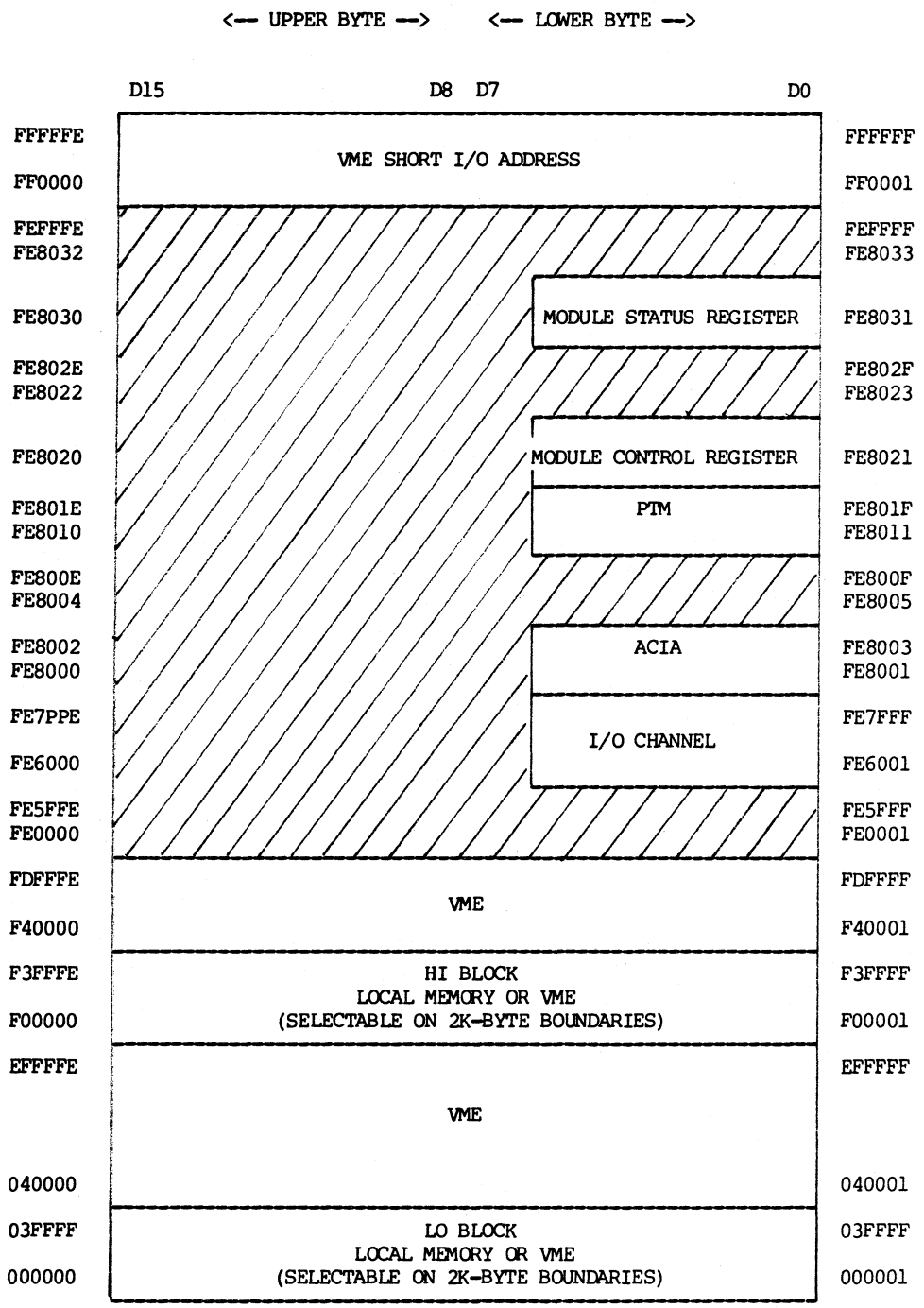


FIGURE 4-3. VME110 Memory Map

NOTES: The initial addresses for the SSP and the PC are obtained from the first four word locations of the ROM installed in socket pair 1.

The shaded portions of the memory map indicate redundant I/O addresses and should not be accessed.

TABLE 4-1. PTM and ACIA Map Definitions

ADDRESS RANGE	MODE	COMMENTS	
FE801F	READ	READ LSB BUFFER REGISTER	
	WRITE	WRITE TIMER #3 LATCHES	
FE801D	READ	READ TIMER #3 COUNTER	
	WRITE	WRITE MSB BUFFER REGISTER	
FE801B	READ	READ LSB BUFFER REGISTER	
	WRITE	WRITE TIMER #2 LATCHES	PTM
FE8019	READ	READ TIMER #2 COUNTER	
	WRITE	WRITE MSB BUFFER REGISTER	
FE8017	READ	READ LSB BUFFER REGISTER	
	WRITE	WRITE TIMER #1 LATCHES	
FE8015	READ	READ TIMER #1 COUNTER	
	WRITE	WRITE MSB BUFFER REGISTER	
FE8013	READ	READ STATUS REGISTER	
	WRITE	WRITE CONTROL REGISTER #2	
FE8011	READ	NO OPERATION	
	WRITE	(CR20 -1) WRITE CONTROL REG #1 (CR20 =0) WRITE CONTROL REG #3	
FE8003	READ	READ RECEIVE DATA REGISTER	
	WRITE	WRITE TRANSMIT DATA REGISTER	ACIA
FE8001	READ	READ STATUS REGISTER	
	WRITE	WRITE CONTROL REGISTER	

NOTE: Refer to the PTM and ACIA data sheets for detailed register descriptions.

4.3.4.1 MC6840 Programmable Timer Module. The MC6840 PTM contains three 16-bit counters. The counters are externally connected for cascading. The output of timer 3 is connected to the input of timer 2 and the output of timer 2 is connected to the input of timer 1. The timer 1 output is not connected. The timer 3 clock input may be the MPU E clock or the baud rate clock from the serial debug port. The PTM gate inputs for the three timers are permanently tied low (enabled). A simplified diagram of the timers is shown in Figure 4-4.

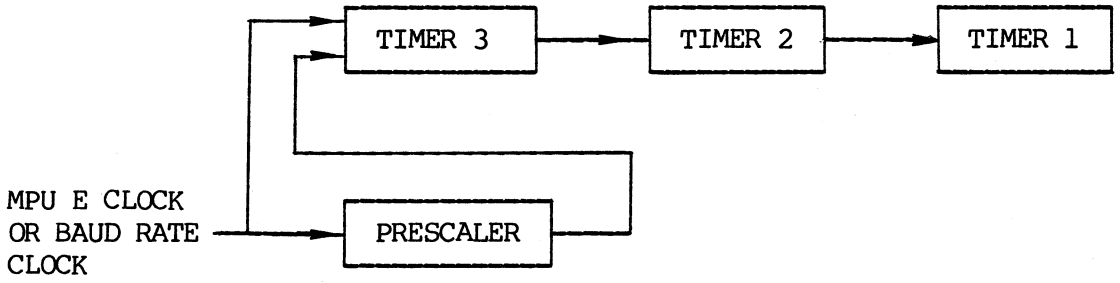


FIGURE 4-4. PTM Interval Timers

The timers may be used as general purpose interval timers for periodically interrupting the MPU for switching between tasks in a multi-tasking application. In systems with two or more VME110's, a task could be created to periodically monitor a section of global memory for communication between the boards. The user should refer to the MC6840 PTM data sheet for detailed register descriptions.

The watchdog timer may be used to initiate a reset to the VME110 and/or to the system if the MPU fails to reset a counter in a specified amount of time. The failure may be due to software bugs or to a hardware malfunction. After the reset, the FAIL indicator is illuminated and the System Failure signal (SYSFAIL*) is generated. This signal could be used to interrupt another VME110 board for backup operation.

The watchdog timer is implemented by using the PTM timers 3 and 2. First, the user must configure the PTM so the output of timer 3 is enabled. This cascades the two timers. The timer 2 output is also enabled. The operating mode for both timers should be configured for the continuous operating mode (CR3,CR4, and CR5 =0).

Timer 3 is loaded for the desired interrupt interval and its corresponding interrupt enable bit is set. Timer 2 is loaded with the maximum number of timer 3 interrupts that are allowed to accumulate before being serviced under normal operating conditions. Each time the timer 3 count reaches zero, an interrupt is sent to the MPU and the timer 2 count is decremented. Each time the timer 3 interrupt is processed, both timers are reloaded with their initial values. If the timer 2 counter ever decrements to zero and the watchdog timer is enabled, the board is reset. If the system reset jumper is installed, the system is also reset. Figure 4-5 shows the PTM timer configuration for the watchdog timer.

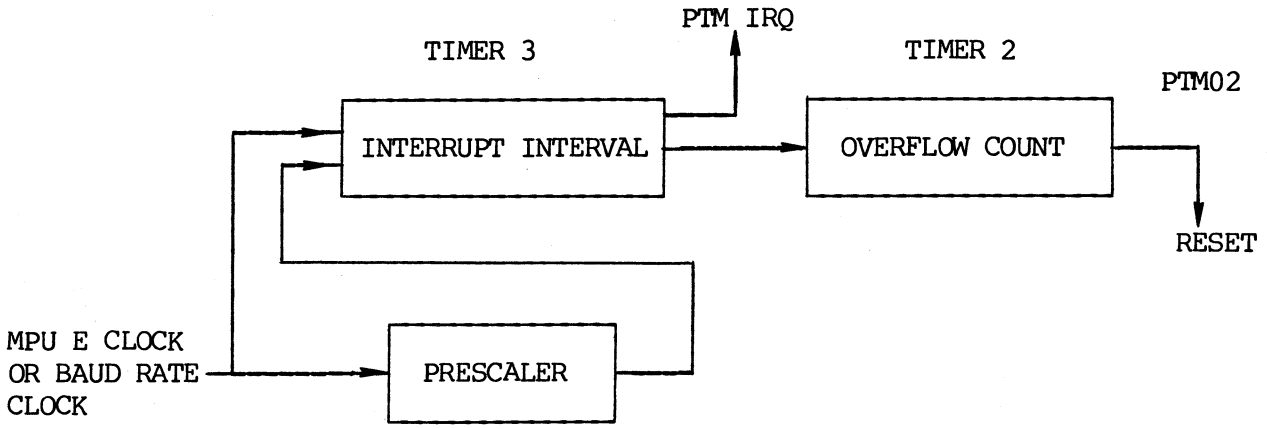


FIGURE 4-5. PTM Watchdog Timer Configuration

4.3.4.2 Asynchronous Communication Interface Adapter (ACIA). The Serial Port consists of an MC6850 ACIA, RS-232C connector and interface, and baud rate select circuitry. The port is configured as Data Communication Equipment (DCE) to be connected to Data Terminal Equipment (DTE). Table 5-3 lists the serial port connector signals. The user should refer to the ACIA data sheet for detailed register descriptions.

The following paragraph covers any special initialization procedures or considerations.

The user should perform a master reset to the ACIA after each MPU reset to ensure proper ACIA initialization. The count divide select should be selected for divide by sixteen. The ACIA Request To Send ($\overline{RTS}$) signal controls the serial port Clear To Send signal (CTS). Normally, the $\overline{RTS}$ signal should be low to allow the terminal to transmit data. If the user wishes to implement flow control, the $\overline{RTS}$ signal may be set high. This causes the CTS signal to the terminal to indicate an off condition and inhibit data transmission. The ACIA Data Carrier Detect ($\overline{DCD}$) input is permanently set low. The ACIA $\overline{CTS}$ signal is low whenever the terminal indicates it is ready.

Two optional capacitors may be installed at C43 and C44 for controlling the slew rate of the Transmit Data (TXD) and Data Terminal Ready (DTR) signals. In noisy environments, the addition of the capacitor allows the rejection of high frequency noise. Refer to the MC1489 data sheet for additional information.

4.3.4.3 Module Control Register (MCR). Memory map address FE8021 is reserved for addressing the MCR (U37).

The MCR contains six bits for controlling various board functions as described below. The MCR may only be written while in the supervisor state. A bus error will be issued if a write attempt is made while in the user state.

Upon initialization, the MCR is reset to $10, which illuminates the FAIL indicator.

7	6	5	4	3	2	1	0
PRM	WDE	SFIE	FAIL	0	0	BRC1	BRC0

PRM - PROTECT MODE
0 Protect Mode disabled.
1 Protect Mode enabled.

WDE - WATCHDOG ENABLE
0 Watchdog Timer disabled.
1 Watchdog Timer enabled.

SFIE - SYSTEM FAIL INTERRUPT ENABLE
0 interrupt disabled.
1 interrupt enabled.

FAIL - 0 No Failure. The FAIL indicator is extinguished and the VMEbus SYSFAIL* signal is deactivated.

1 Failure. The FAIL indicator is illuminated and the VMEbus SYSFAIL* signal is activated.

BRC1, BRC0 - BUS RELEASE CONTROL BITS

BRC1	BRC0	MODE SELECTED
0	0	ROR - Release on request
0	1	RBC - Release on bus clear
1	0	RWD - Release when done
1	1	RNE - Release never

4.3.4.4 Module Status Register (MSR). The MSR (U52) is addressed using address FE8031 of the memory map.

The MSR allows the user to read the current level of ACFAIL*, SYSFAIL*, and the user configurable jumpers. The MSR is a read-only register. Any write attempt to this register results in a bus error.

7	6	5	4	0-3
ACF	SF	SSB1	SSB0	UNDEFINED

ACF - AC FAILURE
0 VMEbus ACFAIL* false.
1 VMEbus ACFAIL* true.

SF - SYSTEM FAILURE
0 VMEbus SYSFAIL* false.
1 VMEbus SYSFAIL* true.

SSB1 - SOFTWARE STATUS BIT 1
0 Header J5 pins 3 and 5 connected.
1 Header J5 pins 1 and 3 connected.

SSB0 - SOFTWARE STATUS BIT 0
0 Header J5 pins 4 and 6 connected.
1 Header J5 pins 2 and 4 connected.

The logic levels of SSB0 and SSB1 are defined by the user. Their logic levels are determined by two jumpers on jumper header J5 (refer to paragraph 2.3.4). The use of these bits is at the discretion of the user. They could be used to provide part of a network address for the serial port, or some other user-defined function.

4.3.5 Data Transfer Operation

The data transfer between the MPU and local memory is performed in an asynchronous manner. The address and data are placed on the address and data buses, and the address and data strobes are generated. The MPU waits until the Data Transfer Acknowledge signal (MPUDTACK*) is driven low before continuing with the current instruction cycle. (Refer to the Motorola MC68000 User's Manual for detailed information.)

4.3.5.1 Read Operation. Figure 4-6 contains a timing diagram which shows the relationships between the various signals. The actual times in nanoseconds are dependent upon the access speeds of the devices being addressed and whether the speed of the MPU is 8 MHz or 10 MHz. The five encircled numbers on the timing diagram can be used as entries into Table 4-2 to determine the actual timing relationships. For example, the time from a socket pair select signal [SP1*-SP4*] to the time when memory data is valid on the data bus [D00-D15] is indicated by the encircled number 2. This number can be used to enter the Local Memory Read Cycle Timing Specification Table 4-2, entry 2.

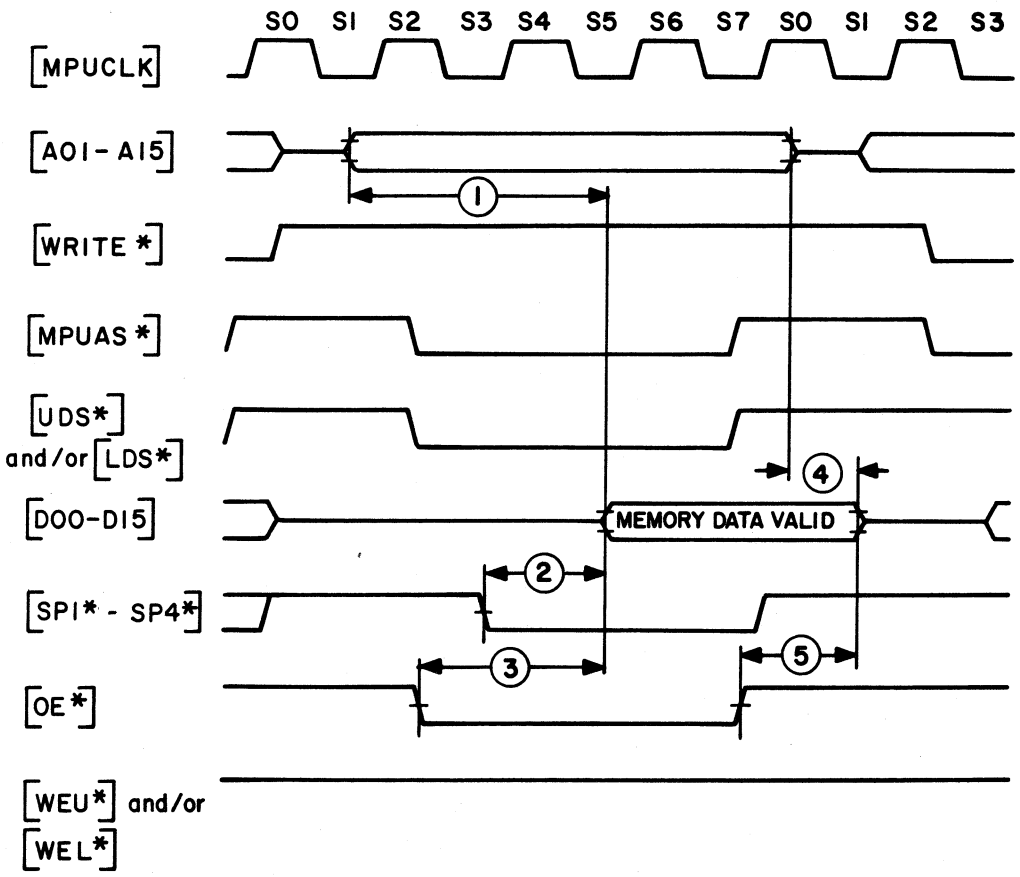
4.3.5.2 Write Operation. Figure 4-7 contains a timing diagram which shows the relationships between the various signals during a write operation. The actual times in nanoseconds are dependent upon the access speeds of the devices being addressed and the speed of the MPU. The encircled numbers on the timing diagram can be used as entries into the Local Memory Write Cycle Timing Specification Table 4-3 to determine the actual timing relationships.

4.3.6 Data Transfer Acknowledge Generation

The following description refers to the schematic diagram sheet 7 of Figure 5-2.

The data transfer acknowledge signal to the MPU [MPUDTACK*] for the on-board memory is generated by a delay of the data strobe signals, Lower Data Strobe (LDS*) or Upper Data Strobe (UDS*) via the shift register U49. The outputs of this shift register provide a set of four signals which are delayed from the clock input. The actual time delay between LDS* or UDS* and MPUDTACK* is chosen separately for the ROM and RAM sections of the on-board memory by wiring one of the shift register output signals through headers J9 and J10 to be gated with [ROMSEL] or [RAMSEL] respectively, according to the access times of the employed devices. (Refer to paragraphs 2.3.8 and 2.3.9.)

Table 4-4 lists the time delays for the wait cycles versus the MPU cycle time from data strobe to data transfer acknowledge.



SIGNAL DESCRIPTIONS

[OE*] - Output Enable - This signal is activated during a read cycle when one or both of the MPU data strobes is activated.

[SP1*-SP4*] Socket Pair Select (1-4) - These signals provide a unique select to the appropriate socket pair. The address range in which these signals are activated is determined by the user PROM.

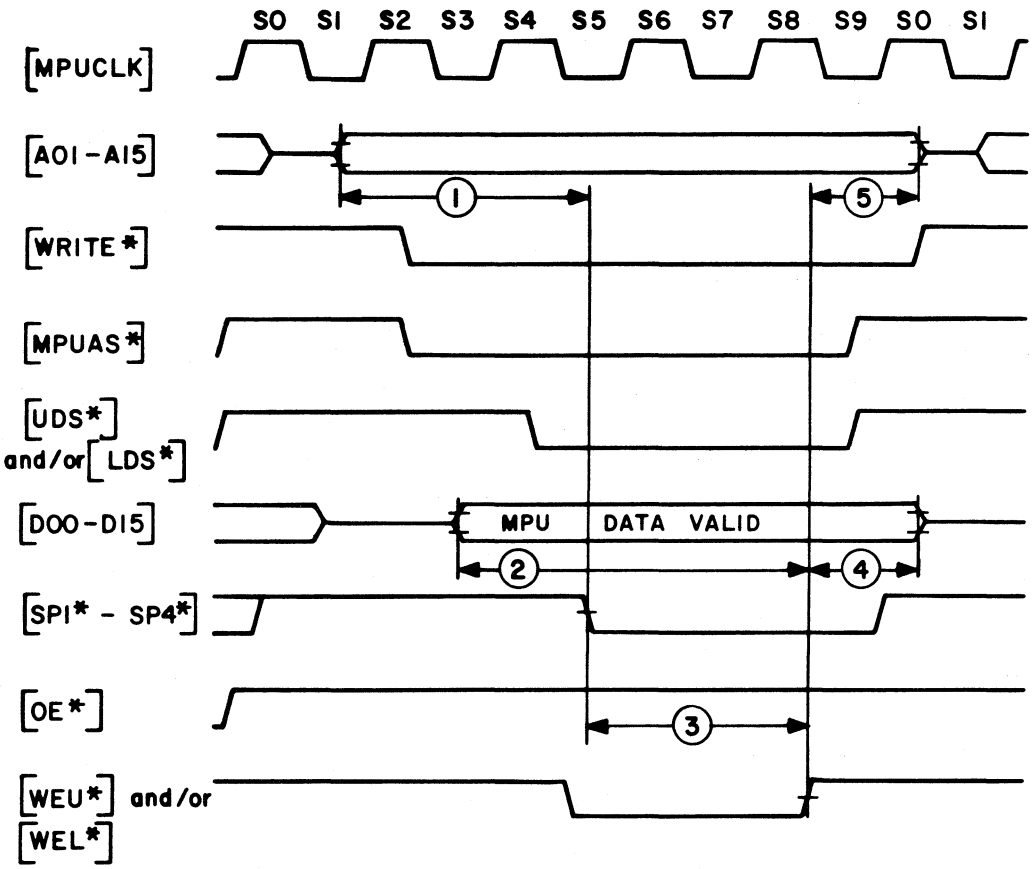
[WEL*] - Write Enable Lower - This signal is activated during a write cycle when the MPU LDS* signal is activated.

[WEU*] - Write Enable Upper - This signal is activated during a write cycle when the MPU UDS* signal is activated.

FIGURE 4-6. Local Memory Read Cycle Timing Diagram

TABLE 4-2. Local Memory Read Cycle Timing Specifications (RAM or ROM)

NO.	CHARACTERISTIC	WAIT CYCLES	8 MHz MIN	8 MHz MAX	10 MHz MIN	10 MHz MAX
1	Address valid to data valid	0		285		225
		1		410		325
		2		535		425
		3		660		525
2	[SP1*],[SP2*],[SP3*], or [SP4*] low to data valid	0		165		100
		1		290		200
		2		415		300
		3		540		400
3	[OE*] low to data valid	0		220		165
		1		345		265
		2		470		365
		3		595		465
4	Address invalid to data invalid	0-3	0		0	
5	[SP1*],[SP2*],[SP3*],[SP4*] or [OE*] high to data high impedance	0-3		100		100



[OE*] - Output Enable - This signal is activated during a read cycle when one or both of the MPU data strobes is activated.

[SP1*-SP4*] Socket Pair Select (1-4) - These signals provide a unique select to the appropriate socket pair. The address range in which these signals are activated is determined by the user PROM.

[WEL*] - Write Enable Lower - This signal is activated during a write cycle when the MPU LDS* signal is activated.

[WEU*] - Write Enable Upper - This signal is activated during a write cycle when the MPU UDS* signal is activated.

FIGURE 4-7. Local Memory Write Cycle Timing Diagram

TABLE 4-3. Local Memory Write Cycle Timing Specifications (RAM)

NO.	CHARACTERISTIC	WAIT CYCLES	8 MHz MIN	8 MHz MAX	10 MHz MIN	10 MHz MAX
1	Address valid to [WEL*] and/or [WEU*] and [SP1*], [SP2*],[SP3*], or [SP4*] low	0 or 1	125		105	
2	Data valid to [WEL*] and [WEU*] high	0	250		205	
		1	375		305	
3	[SP1*],[SP2*],[SP3*], or [SP4*] low and [WEL*] and/or [WEU*] low pulse width	0	155		110	
		1	280		210	
4	[WEL*] and [WEU*] high to address invalid	0 or 1	75		50	
5	[WEL*] and [WEU*] high to data invalid	0 or 1	75		50	

TABLE 4-4. Data Transfer Acknowledge Generation

WAIT CYCLES SELECTED	READ CYCLE 8 MHz MPU TYP	READ CYCLE 8 MHz MPU MAX	WRITE CYCLE 8 MHz MPU TYP	WRITE CYCLE 8 MHz MPU MAX	READ CYCLE 10 MHz MPU TYP	READ CYCLE 10 MHz MPU MAX	WRITE CYCLE 10 MHz MPU TYP	WRITE CYCLE 10 MHz MPU MAX
0	500	500	625	625	400	500	500	600
1	625	625	750	750	500	600	600	700
2	750	750	-	-	600	700	-	-
3	875	875	-	-	700	800	-	-

4.3.7 Local Bus Timeout

The local bus timeout is used to ensure that the MPU does not "hang up" waiting for an acknowledge signal. When an MPU data strobe has been generated and 200 microseconds has elapsed without the receipt of the data acknowledge, a timeout occurs and a bus error is issued to the MPU. The local bus timeout is enabled or disabled, for every MPU cycle, by jumper header J6 (refer to paragraph 2.3.5).

4.3.8 Protect Mode and User/Supervisor State

The protect mode allows the user to write-protect local RAM memory on 2K segment boundaries. The user specifies which segments are to be write-protectable by selecting a special code in the map decoder PROM. When the protect mode is disabled, all local RAM can be read or written (refer to paragraph 2.3.15) in either the supervisor or user state. When the protect mode is enabled, the segments that are designated as write-protectable cannot be written while in the user state. If attempted, the hardware generates a bus error and aborts the write cycle.

If the protect mode is enabled and the watchdog timer is also enabled, the MPU cannot read or write the PTM while in the user state. If attempted, the hardware generates a bus error and the PTM is not selected.

4.3.9 VMEbus Arbitration

Bus arbitration is a technique used by master-type modules to request, be granted, and acknowledge bus mastership. Each VME110 module contains bus arbitration logic, however, only the one configured as the system controller performs the bus arbitration functions.

The arbiter arbitrates use of the bus for all VMEbus masters. When a request is received and the bus is not busy, the arbiter activates a bus grant in and waits for the granted requester to activate bus busy. The arbiter then deactivates bus grant in and the arbitration cycle is complete. The arbiter on the VME110 is an option one single level bus arbiter which arbitrates bus requests on level three only. Figure 4-8 shows the arbiter timing. Table 4-5 lists the arbiter timing relationships in nanoseconds.

When the arbiter is enabled by the system controller header, the VME110 must be located in slot 1 of the VMEbus backplane to ensure it is the first physical device in the arbitration daisy-chain. In this configuration, the VME110 bus requester is the first requester in the daisy-chain and therefore has the highest priority.

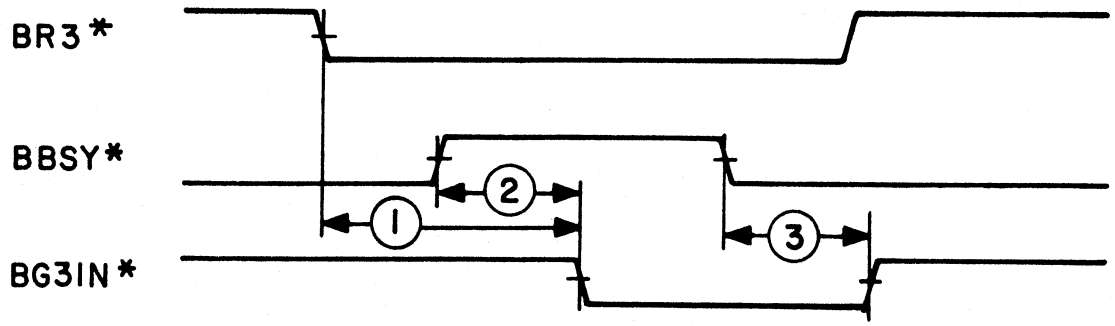


FIGURE 4-8. Arbiter Timing Diagram

TABLE 4-5. Arbiter Timing

NO.	CHARACTERISTIC	TYP	MAX
1	BR3* low to BG3IN* low	25	40
2	BBSY* high to BG3IN* low	25	40
3	BBSY* low to BG3IN* high	50	80

4.3.9.1 VMEbus Requester and VMEbus Interface. The VMEbus requester circuitry obtains bus mastership for all VMEbus cycles and releases bus mastership as selected by the bus release control bits. Once bus mastership has been obtained, the VMEbus interface circuitry is enabled.

When bus mastership is initially required, the requester performs an arbitration cycle at the jumpered request level as shown in Figure 4-9. Table 4-6 lists the typical and maximum times for the timing relationships indicated by the encircled numbers in Figure 4-9. If the bus is currently busy, the MPU will wait indefinitely if the local bus timeout is disabled, or 200 us if it is enabled. After the arbitration cycle is completed and bus mastership has been granted, the VMEbus interface circuitry is enabled. For a typical cycle, the interface presents a 23-bit address on the bus and an address modifier code (Table 4-7). The direction of data transfer is indicated by the write signal. The address strobe and one or both data strobes are produced. The interface then waits for a data transfer acknowledge or bus error signal from the slave to complete the cycle. Table 4-8 shows the number of MPU wait cycles inserted for various VME device slave access times.

When the requester receives bus grant at the jumpered level, and does not presently require use of the bus, the corresponding bus-grant-out signal is produced. The respective bus-grant-in lines and bus-grant-out lines which are not at the jumpered level are connected directly together.

On subsequent VMEbus cycles, if bus mastership has been released, an arbitration cycle is again required to use the bus. However, if bus mastership has not been released, an arbitration cycle is not required and the bus may be used immediately. In systems in which this module is the primary user of the bus, the saving of arbitration time on subsequent bus accesses will increase performance. Conversely, in systems in which there is heavy bus usage between two or more masters, optimum system performance is obtained by having the present bus master release bus mastership as soon as possible.

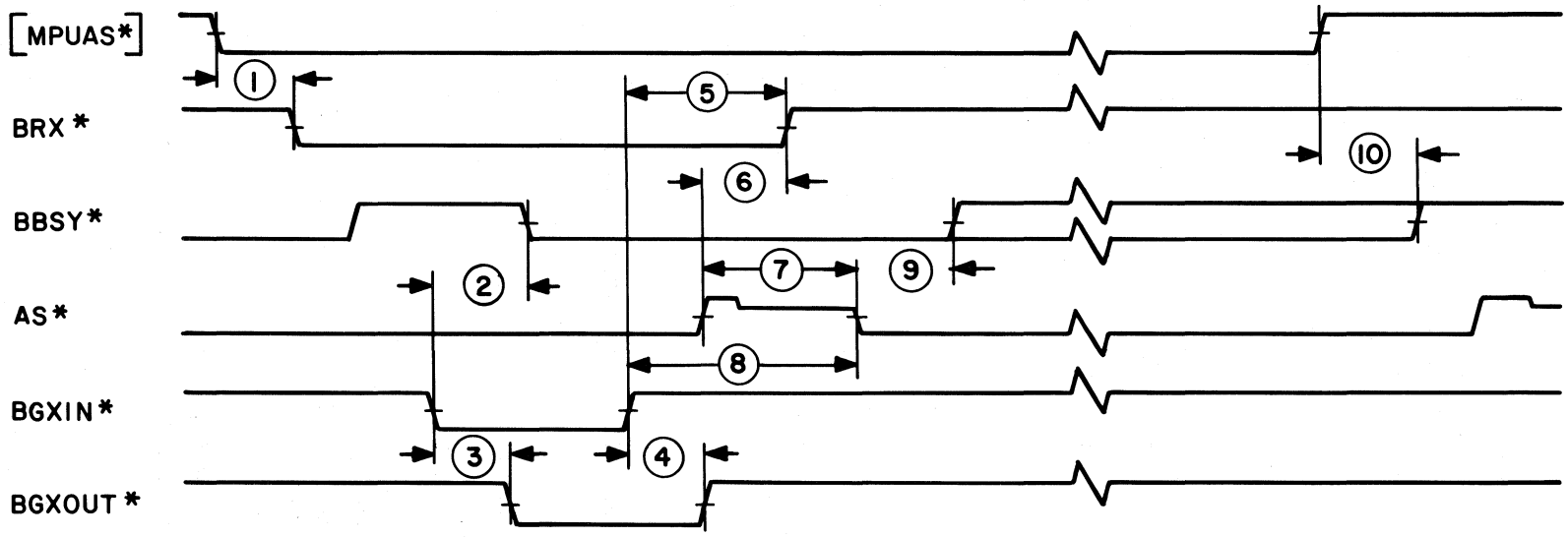
4.3.9.2 VMEbus Release. The manner in which bus mastership is released by the VME110 is determined by the bus release control bits in the MCR (refer to paragraph 4.3.4.3). The four modes provided are described below.

RNE - Release Never. Once bus mastership has been granted, it is never released until the processor changes the bus release control bits to another mode. This mode is intended to guarantee VMEbus availability in time-critical applications. This mode should be used with caution since all potential VMEbus masters will be denied access to the bus until this mode is switched.

RBC - Release on Bus Clear. Once bus mastership has been granted, it is released only by the VMEbus Bus Clear (BCLR*) signal. In systems equipped with a multi-level arbiter, this mode selectively denies or yields access to a requesting bus master based on its bus request priority level. Potential bus masters that are requesting the bus at a priority level less than or equal to the level of this module are denied access to the bus until this mode is switched.

NOTE

Single-level arbiters like the one on the VME110 do not drive the BCLR* line. Therefore, use of this mode has the same effect as the RNE mode.



NOTE: IN THE SIGNAL NAMES ABOVE, X IS THE ARBITRATION REQUEST LEVEL SELECTED ON HEADERS J2 AND J3.

FIGURE 4-9. VMEbus Requester Timing Diagram

ROR - Release on Request. Once bus mastership has been granted, it is released when any potential bus master requests use of the bus. This mode is selected at reset and is intended for systems in which the VME110 is the primary user of the bus.

RWD - Release when Done. Once bus mastership has been granted, it is immediately released shortly after the beginning of the cycle. Arbitration of the next bus cycle may occur concurrently with the completion of the present bus cycle. Arbitration will be required on each VME110 bus cycle. This mode is useful to guarantee quick bus availability to other bus masters in the system.

The chart below demonstrates how MPU performance and VMEbus performance are affected by the various release modes.

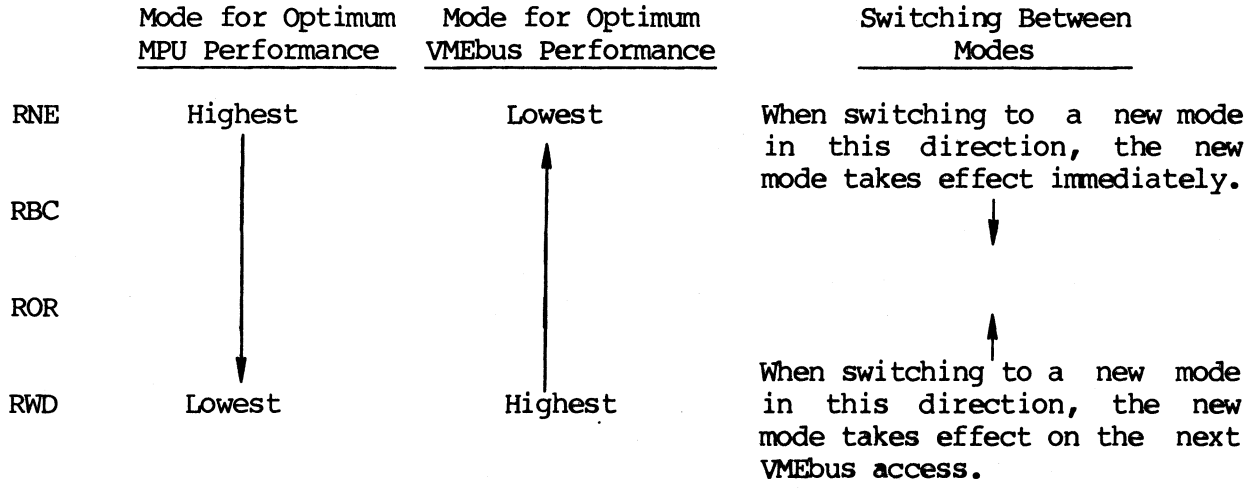


TABLE 4-6. Requester Timing

NO.	CHARACTERISTIC	TYP	MAX
1	[MPUAS*] low to BRX* low	60	70
2	BGXIN* low to BBSY* low	65	100
3	BGXIN* low to BGXOUT* low	35	50
4	BGXIN* high to BGXOUT* high	20	30
5	BGXIN* high to BRX* released	95	120
6	AS* high to BRX* released	60	95
7	AS* high pulse width	115	150
8	BGXIN* high to AS* low	130	175
9	AS* low to BBSY* high (RWD Mode)	45	65
10	[MPUAS*] high to BBSY* high (ROR and RBC Modes) (See Note)	35	50

NOTE: In the ROR and RBC modes, if the release condition is present, the bus will be released within time #10 after the completion of the current MPU cycle. The bus will also be released within time #10 after an MPU halt condition.

TABLE 4-7. Address Modifier Codes Presented By VME110

HEADER J4 PINS 1 & 2 CONNECTED (AM3 ALWAYS TRUE)

HEX CODE	ADDRESS MODIFIER AM5	AM4	AM3	AM2	AM1	AM0	VME110 CONDITIONS
3E	H	H	H	H	H	L	Standard Supervisory Program Access
3D	H	H	H	H	L	H	Standard Supervisory Data Access
3A	H	H	H	L	H	L	Standard Non-Privileged Program Access
39	H	H	H	L	L	H	Standard Non-Privileged Data Access
2D	H	L	H	H	L	H	Short Supervisory I/O Access (1)
29	H	L	H	L	L	H	Short Non-Privileged I/O Access (1)

HEADER J4 PINS 2 & 3 CONNECTED (AM3 DRIVEN BY BIT 7 OF THE MCR). (REFER TO PARAGRAPH 2.3.3)

HEX CODE	ADDRESS MODIFIER AM5	AM4	AM3	AM2	AM1	AM0	VME110 CONDITIONS	MCR BIT 7
3E	H	H	H	H	H	L	Standard Supervisory Program Access	0
3D	H	H	H	H	L	H	Standard Supervisory Data Access	0
3A	H	H	H	L	H	L	Standard Non-Privileged Program Access	0
39	H	H	H	L	L	H	Standard Non-Privileged Data Access	0
36	H	H	L	H	H	L	Undefined	1
35	H	H	L	H	L	H	Undefined	1
32	H	H	L	L	H	L	Undefined	1
31	H	H	L	L	L	H	Undefined	1
2D	H	L	H	H	L	H	Short Supervisory I/O Access (1)	0
29	H	L	H	L	L	H	Short Non-Privileged I/O Access (1)	0
25	H	L	L	H	L	H	Undefined	1
21	H	L	L	L	L	H	Undefined	1

NOTES:

(1) When the processor accesses any location between FF0000 and FFFFFF, one of the short I/O address modifier codes is placed on the VMEbus. (See Figure 4-3.)

2. Bit 7 of the MCR controls the memory protect status of the local VME110 RAM if the user has programmed the map decoder PROM to indicate that the 2K segment which contains the current address to be write-protectable.

3. The AM5 line is not driven by the VME110. It is always high because of the termination on the VMEbus backplane.

TABLE 4-8. MPU Wait Cycles vs. VME Slave Board Access Times

WAIT CYCLES (TYPICAL)	8 MHz		10 MHz	
	READ	WRITE	READ	WRITE
0	0 - 25	0 - 50	-	-
1	25 - 150	50 - 175	0 - 80	0 - 90
2	150 - 275	175 - 300	80 - 180	90 - 190
3	275 - 400	300 - 425	180 - 280	190 - 290
4	400 - 525	425 - 550	280 - 380	290 - 390
5	525 - 650	550 - 675	380 - 480	390 - 490
6	650 - 775	675 - 800	480 - 580	490 - 590
7	775 - 900	800 - 925	580 - 680	590 - 690

NOTES:

1. Slave board access time is referenced at the connector for that particular board. Access time is the time from a data strobe (DS0* or DS1*) low to DTACK* low.

2. Wait cycle calculations assume that no VMEbus arbitration is required. If arbitration is required, wait cycles depend upon how long the processor has to wait to gain control of the VMEbus. Refer to paragraph 4.3.9.2 for the bus release control modes.

3. VMEbus propagation delay is assumed to be 10 ns.

4. The VME110 will provide the following delays from AS* low to DS0* or DS1* low.

   Read Cycle 10 ns min to 35 ns max.
   Write Cycle 100 ns min to 130 ns max.

4.3.10 Bus Error

The bus error signal [MPUBERR*] to the MPU causes the MPU to enter an exception processing sequence. A bus error can result from any one of three major conditions: local error, timeout, or VMEbus error.

4.3.10.1 Local Error. A local error occurs for any one of the five conditions listed below:

- Write attempt to local ROM
- Write attempt to the MSR
- Write attempt to the MCR while in the user state.
- Read or write attempt to the PTM while in the user state with the Protect Mode bit (PRM) and the Watchdog Enable bit (WDE) set in the MCR.
- Write attempt to write-protectable RAM while in the user state with PRM enabled in the MCR.

4.3.10.2 Timeout. A local bus timeout occurs for either of the conditions below:

- The addressed I/O Channel device did not respond.
- Failure to complete a VMEbus cycle within the Timeout (BTO) limit. (This could result from failure to receive bus mastership in time to finish a cycle.)

4.3.10.3 VMEbus Error (BERR*). BERR* on the VMEbus interface occurs for either of the conditions below:

- The accessed device on the VMEbus detected an error condition.
- Neither DTACK* nor BERR* was received within the VMEbus Timeout (BTO) limit.

4.3.11 I/O Channel Interface

The I/O Channel interface provides an 8-bit asynchronous data communications path between the MPU and up to 16 I/O Channel boards. The I/O Channel interface signals are located on connector P2. The user can connect a 50-pin cable from P2 to these I/O boards to provide a private I/O for the VME110. Note that power for the I/O Channel boards is not supplied by the VME110 board.

Twelve address lines provide 4K bytes of memory-mapped I/O for address placement on the I/O Channel. A 4-MHz free-running clock provides a time base for general use. Four open-collector interrupt lines allow modules to interrupt the MPU. As shown in Figure 4-2, execution of the reset instruction will reset the I/O Channel. Table 4-9 shows the number of wait clock cycles inserted for various slave board access times. Refer to the I/O Channel Specification Manual, M68RIOCS, for further I/O Channel information.

The following equation may be used to determine the VME110 address of an I/O Channel device.

VME110 Address = FE6001 + 2X(I/O Channel Address)

TABLE 4-9. MPU Wait Cycles vs. I/O Channel Slave Board Access Times

WAIT CYCLES (TYPICAL)	8 MHz		10 MHz	
	READ	WRITE	READ	WRITE
2	0 - 75	0 - 100	-	0 - 25
3	75 - 200	100 - 225	0 - 75	25 - 125
4	200 - 325	225 - 350	75 - 175	125 - 225
5	325 - 450	350 - 475	175 - 275	225 - 325
6	450 - 575	475 - 600	275 - 375	325 - 425
7	575 - 700	600 - 725	375 - 475	425 - 525
8	700 - 825	725 - 850	475 - 575	525 - 625
9	825 - 950	850 - 975	575 - 675	625 - 725

NOTES:

1. Slave board access time is referenced at the connector of the slave board. Access time is the time from a STB* low to XACK* low.

2. I/O Channel bus propagation delay is assumed to be 10 ns.

4.3.12 Interrupt Handler

Interrupts are categorized into two groups called group 1 and group 0. The group 1 interrupts are local interrupts and use the MPU's auto-vector feature for vector assignment. The factory shipped level and vector assignments for this group are shown below. Note that in this configuration, the ACFAIL, SYSFAIL, and ABORT signals each cause a non-maskable level 7 interrupt request. The user may read the status of the ACFAIL* and SYSFAIL* signals in the MSR for determining the appropriate service routine.

The group 0 interrupts are caused by the VMEbus signals IRQ1* through IRQ7*. The vectors for these interrupts are read over the VMEbus during an interrupt acknowledge cycle. In a VME interrupt acknowledge cycle, the VME110 obtains VMEbus mastership, places the interrupt level to be acknowledged on the lower three address lines and activates Interrupt Acknowledge (IACK*) and the appropriate strobe signals. The interrupting device then places an interrupt vector on the lower data byte lines and generates data transfer acknowledge. The vector is then used as a pointer to the MPU exception vector table.

In the event a group 1 and group 0 interrupt are pending at the same level at the start of an interrupt acknowledge cycle, the group 1 interrupt will be serviced first.

Spurious Interrupt - The spurious interrupt vector is taken when there is a bus error during an interrupt acknowledge cycle. Refer to paragraph 4.3.10 for possible error conditions.

GROUP 1 INTERRUPTS	GROUP 1 EXCEPTION VECTOR ADDRESS (HEX)	MPU INTERRUPT LEVEL	GROUP 0 INTERRUPTS
ACFAIL + SYSFAIL + ABORT	7C	LEVEL 7	IRQ7*
PTM	78	LEVEL 6	IRQ6*
ACIA	74	LEVEL 5	IRQ5*
I/O CHANNEL INT4	70	LEVEL 4	IRQ4*
I/O CHANNEL INT3	6C	LEVEL 3	IRQ3*
I/O CHANNEL INT2	68	LEVEL 2	IRQ2*
I/O CHANNEL INT1	64	LEVEL 1	IRQ1*

CHAPTER 5

SUPPORT INFORMATION

5.1 INTRODUCTION

This chapter provides the interconnect signals, parts list and associated parts location diagram, and a schematic diagram for the VMEmodule Monoboard Microcomputer (VME110).

5.2 CONNECTOR SIGNAL DESCRIPTIONS

The VME110 has three interface connectors -- one which connects it to the VMEbus, one which connects it to the I/O channel, and one which connects it to the RS-232C serial I/O port.

5.2.1 VMEbus Connector

The VMEbus connector P1 on the VME110 is a standard DIN 41612 triple-row, 96-pin, male connector. The VMEmodule chassis backplane uses the female connector. Table 5-1 lists the connector pin numbers, signal mnemonics, signal names, and signal descriptions. Additional information concerning this connector can be found in the VMEbus Specification Manual (Motorola publication number MVMEBS).

5.2.2 I/O Channel Connector

The I/O Channel connector P2 on the VME110 is a standard DIN double-row, 64-pin, male connector. The VMEmodule chassis backplane uses the female connector. Table 5-2 lists the connector pin numbers, signal mnemonics, signal names, and signal descriptions. Additional information concerning this connector can be found in the I/O Channel Specification Manual (Motorola publication number M68RIOCS.

5.2.3 RS-232C Serial I/O Port

The RS-232C serial I/O port connector J15 is a standard 25-pin, subminiature D, female connector. The cable for connecting J15 to an RS-232C compatible terminal must be supplied by the user. Table 5-3 lists the connector pin numbers, signal mnemonics, signal names, and signal descriptions.

TABLE 5-1. VMEbus Connector P1 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-A8	D00-D07	DATA BUS (bits 0-7) - Eight of 16 three-state bidirectional data lines which provide the data path between VMEbus master and slave.
A9,A11,A15, A17,A19 B20,B23, C9	GND	GROUND
A10	SYSCLK	SYSTEM CLOCK - 16-MHz signal used as timing reference. When system controller, this signal is provided by the VME110 to the VMEbus.
A12	DS1*	DATA STROBE 1 - Bidirectional signal that indicates a data transfer on data bus lines D08-D15. When system controller, this signal enables the bus timeout counter.
A13	DS0*	DATA STROBE 0 - Bidirectional signal that indicates a data transfer on data bus lines D00-D07. When system controller, this signal enables the bus timeout counter.
A14	WRITE*	WRITE - Output signal that indicates the direction of data transfers.
A16	DTACK*	DATA TRANSFER ACKNOWLEDGE - Input signal indicates that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle.
A18	AS*	ADDRESS STROBE - The falling edge of this bidirectional signal indicates a valid address is present on the address lines. During bus arbitration, a high level indicates that the previous master has released its signal lines.
A20	IACK*	INTERRUPT ACKNOWLEDGE - Output signal indicates a VME interrupt acknowledge cycle.
A21	IACKIN*	INTERRUPT ACKNOWLEDGE IN - IACKIN* and IACKOUT* form a daisy-chained acknowledge. IACKIN* input signal is connected directly to IACKOUT*.
A22	IACKOUT*	INTERRUPT ACKNOWLEDGE OUT - IACKIN* and IACKOUT* form a daisy-chained acknowledge. IACKOUT* output signal is connected directly to IACKIN*.
A23	AM4	ADDRESS MODIFIER (bit 4) - One of five three-state output lines used to provide additional information about the address bus. Refer to paragraph 4.3.9.1.

TABLE 5-1. VMEbus Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A24	A07	ADDRESS bus (bit 7) - One of 23 three-state driven output lines which specify an address in the memory map (see Figure 4-3).
A25	A06	ADDRESS bus (bit 6) - Similar to pin A24.
A26	A05	ADDRESS bus (bit 5) - Similar to pin A24.
A27	A04	ADDRESS bus (bit 4) - Similar to pin A24.
A28	A03	ADDRESS bus (bit 3) - One of 23 three-state driven output lines which specify a memory address. During an interrupt acknowledge cycle, address bus lines 1-3 are used to indicate the interrupt level which is being acknowledged.
A29	A02	ADDRESS bus (bit 2) - Similar to pin A28.
A30	A01	ADDRESS bus (bit 1) - Similar to pin A28.
A31	-12V	-12 Vdc power - used by logic circuits.
A32 B32 C32	+5V	+5 Vdc power - used by logic circuits.
B1	BBSY*	BUS BUSY - This bidirectional signal is driven low when the VME110 is the VMEbus master. Also an input to the arbiter to indicate that the bus may be arbitrated.
B2	BCLR*	BUS CLEAR - Input signal that causes the release of bus mastership in the RBC mode.
B3	ACFAIL*	AC FAILURE - Input signal that indicates a power failure has occurred and generates a level seven interrupt request.
B4,B6, B8,B10	BG0IN*- BG3IN*	BUS GRANT (0-3) IN - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. A grant received at the jumpered level indicates the VME110 may become the bus master. The remaining three bus-grant-in lines are connected directly to their respective bus-grant-out lines.
B5,B7, B9,B11	BG0OUT*- BG3OUT*	BUS GRANT (0-3) OUT - Bus-grant-in and bus-grant-out form a daisy-chained bus grant. When a bus-grant-in is received at the jumpered level and the MPU is not awaiting bus mastership, the bus-grant-out signal is true on the respective level.

TABLE 5-1. VMEbus Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
B12-15	BR0*-BR3*	BUS REQUEST (0-3) - The bidirectional bus request of the jumpered level is true when the MPU requires bus mastership. When one or more of the bus request lines is true in the ROR mode, bus mastership is released. When the VME110 is the system controller, bus request level three is monitored by the arbiter.
B16-19	AM0-AM3	ADDRESS MODIFIER (bits 0-3) - Similar to pin A23.
B21	SERCLK	Not used.
B22	SERDAT	Not used.
B24-30	IRQ7*-IRQ1*	INTERRUPT REQUEST (7-1) - Seven prioritized interrupt request inputs. Jumper enabled, level seven is the highest priority.
B31	+5V STDBY	Not used.
C1-8	D08-D15	DATA BUS (bits 8-15) - Eight of 16 three-state bidirectional data lines which provide the data path between VMEbus master and slave. Similar to pins A1-8.
C10	SYSFAIL*	SYSTEM FAIL - Reflects state of FAIL bit in MCR and FAIL indicator. When enabled in MCR, this bidirectional signal generates an interrupt request.
C11	BERR*	BUS ERROR - Indicates an error has occurred during data transfer cycle. The cycle is terminated and the MPU starts exception processing. When the VME110 is the system controller, this bidirectional signal is generated when a data transfer cycle did not complete within 200 us.
C12	SYSRESET*	SYSTEM RESET - Causes a board level reset when received from the VMEbus. When system controller, a board level reset causes this bidirectional signal to be generated to the VMEbus (see Figure 4-2).
C13	LWORD*	LONGWORD - Not driven. This terminated signal remains at a high level when the VME110 is bus master.
C14	AM5	ADDRESS MODIFIER (bit 5) - This output line is not driven by the VME110. AM5 always appears as a high (true) level on the VMEbus because of the backplane termination.
C15	A23	ADDRESS bus (bit 23) - One of 23 three-state driven output lines which specifies an address in the memory map (see Figure 4-3). Similar to pin A24.

TABLE 5-1. VMEbus Connector P1 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C16	A22	ADDRESS bus (bit 22) - Similar to pin A24.
C17	A21	ADDRESS bus (bit 21) - Similar to pin A24.
C18	A20	ADDRESS bus (bit 20) - Similar to pin A24.
C19	A19	ADDRESS bus (bit 19) - Similar to pin A24.
C20	A18	ADDRESS bus (bit 18) - Similar to pin A24.
C21	A17	ADDRESS bus (bit 17) - Similar to pin A24.
C22	A16	ADDRESS bus (bit 16) - Similar to pin A24.
C23	A15	ADDRESS bus (bit 15) - Similar to pin A24.
C24	A14	ADDRESS bus (bit 14) - Similar to pin A24.
C25	A13	ADDRESS bus (bit 13) - Similar to pin A24.
C26	A12	ADDRESS bus (bit 12) - Similar to pin A24.
C27	A11	ADDRESS bus (bit 11) - Similar to pin A24.
C28	A10	ADDRESS bus (bit 10) - Similar to pin A24.
C29	A09	ADDRESS bus (bit 9) - Similar to pin A24.
C30	A08	ADDRESS bus (bit 8) - Similar to pin A24.
C31	+12V	+12 Vdc power - used by logic circuits.

TABLE 5-2. I/O Channel Connector P2 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
A1-10, A17-19, A24,A25, A31,A32, C11,C20, C25,C31, C32	GND	GROUND
A11	A11	ADDRESS Channel (bit 11) - One of 12 address output lines used to address I/Omodules.
A12	A10	ADDRESS Channel (bit 10) - Similar to pin A11.
A13	A8	ADDRESS Channel (bit 8) - Similar to pin A11.
A14	A6	ADDRESS Channel (bit 6) - Similar to pin A11.
A15	A4	ADDRESS Channel (bit 4) - Similar to pin A11.
A16	A2	ADDRESS Channel (bit 2) - Similar to pin A11.
A20	D7	DATA Channel (bit 7) - One of eight bidirectional data lines which comprise the byte-wide data bus.
A21	D6	DATA Channel (bit 6) - Similar to pin A20.
A22	D4	DATA Channel (bit 4) - Similar to pin A20.
A23	D2	DATA Channel (bit 2) - Similar to pin A20.
A26 C26	-12Vdc	-12 Vdc power - Not used.
A27 C8,C9, C10,C27	(Reserved)	Not used.
A28 C28	+12Vdc	+12 Vdc power - Not used.
A29,A30 C29,C30	+5Vdc	+5 Vdc power - Not used.
C1-4	INT4*-INT1*	INTERRUPT REQUEST (4-1) - Four prioritized interrupt request input lines. INT4* is the highest priority interrupt.
C5	IORES*	I/O RESET - Reset output signal to external devices produced by a board level reset or by the MPU reset instruction.

TABLE 5-2. I/O Channel Connector P2 Pin Assignments (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
C6	XACK*	TRANSFER ACKNOWLEDGE - Input signal that indicates that valid data is available on the data channel during a read cycle, or that data has been accepted from the data channel during a write cycle.
C7	CLK	CLOCK - 4 MHz clock output signal.
C12	A9	ADDRESS Channel (bit 9) - Similar to pin A11.
C13	A7	ADDRESS Channel (bit 7) - Similar to pin A11.
C14	A5	ADDRESS Channel (bit 5) - Similar to pin A11.
C15	A3	ADDRESS Channel (bit 3) - Similar to pin A11.
C16	A1	ADDRESS Channel (bit 1) - Similar to pin A11.
C17	A0	ADDRESS Channel (bit 0) - Similar to pin A11.
C18	STB*	STROBE - The falling edge of this output signal indicates a valid address is present on the address channel.
C19	WT*	WRITE - This output signal indicates the direction of data transfers.
C21	D5	DATA Channel (bit 5) - Similar to pin A20.
C22	D3	DATA Channel (bit 3) - Similar to pin A20.
C23	D1	DATA Channel (bit 1) - Similar to pin A20.
C24	D0	DATA Channel (bit 0) - Similar to pin A20.

TABLE 5-3. RS-232C Serial Port Connector J15 Pin Assignments

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1,4,9-19, 21-25	(Reserved)	Not connected.
2	TXD	TRANSMIT DATA - Transmit data from terminal. This signal is connected to the ACIA receive data input.
3	RXD	RECEIVE DATA - Receive data to terminal. This signal is connected to the ACIA transmit data output.
5	CTS	CLEAR TO SEND - Indicates terminal may send data. This signal is controlled by the ACIA $\overline{RTS}$ output.
6	DSR	DATA SET READY - Indicates to terminal that port is ready. When power is applied, this signal is true.
7	GND	SIGNAL GROUND
8	DCD	DATA CARRIER DETECT - Indicates to terminal that data carrier is present. When power is applied, this signal is true.
20	DTR	DATA TERMINAL READY - Indicates to port that terminal is ready. This signal is connected to the ACIA $\overline{CTS}$ input and must be true for the ACIA to transmit data.

5.3 PARTS LIST

A parts location diagram for the VME110 is provided in Figure 5-1. The reference designation, Motorola part number, and description for each part are listed in Table 5-4. This parts list reflects the latest issue of the VME110 hardware at the time of the printing of this manual.

TABLE 5-4. VME110 Parts List

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	84-W8047B01	PWB assembly, VME110
C1-9,C13-30, C41,C42	21SW992C025	Capacitor, ceramic, .100 uF @ 50 Vdc
C10,C11, C31-40	21NW9702A09	Capacitor, ceramic, .1 uF @ 50 Vdc
C12	21NW9604A11	Capacitor, ceramic, .47 uF @ 50 Vdc, ± 20%
C43,C44	(see NOTE 1)	
C45	23NW9618A33	Capacitor, 22 uF @ 25 Vdc
DL1	01NW9804B83	Delay, 50 nsec
DL2	01NW9804C09	Delay line, triple, 50 nsec
DS1,DS2	48NW9612A34	Indicator light, red, 5 Vdc
DS3	48NW9612A38	LED, green
J1,J4,J6,J13	28NW9802D04	Header, single-row post, 3-position
J2,3	28NW9802C63	Header, double-row post, 12-pin
J5	28NW9802B21	Header, double-row post, 6-pin
J7	28NW9802E30	Header, single-row post, 4-position
J8,J9,J10, J14,J16-27	28NW9802C43	Header, double-row post, 8-pin
J11,J12	28NW9802C36	Header, double-row post, 14-pin
J15	28NW9802D88	Connector, RS-232C
P1	28NW9802E51	Connector, 96-pin plug
P2	28NW9802E05	Connector, 64-pin plug
R1,R2,R4,R6, R7,R14,R16, R18,R22	06SW-124A65	Resistor, film, 4.7k ohm, 5%, 1/4 W
R3,R19,R20	51NW9626A49	Resistor network, seven 10k ohm
R5,R15	06SW-124A37	Resistor, film, 330 ohm, 5%, 1/4 W
R8,R11,R12	51NW9626A37	Resistor network, nine 10k ohm
R9,10	06SW-124B22	Resistor, film, 1M ohm, 5%, 1/4 W

TABLE 5-4. VME110 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
R13	51NW9626A41	Resistor network, nine 4.7k ohm
R17	51NW9626A76	Resistor network, six 330/470 ohm
R21	51NW9626A46	Resistor network, five 4.7k ohm
S1,S2	40NW9801A54	Switch, SPDT
U1,U35	51NW9615F38	I.C. SN74LS393N
U2	51NW9615C95	I.C. SN74S74N
U3	(See NOTE 2)	I.C. Programmed PROM
U4	51NW9615G97	I.C. MC68000G8
U5,U6	51NW9615H89	I.C. SN74LS645-1N
U7	51NW9615F10	I.C. SN74LS125AN
U8,U39,U40	51NW9615C96	I.C. SN74S04N
U9,U54	51NW9615D32	I.C. SN74S02N
U10,U48	51NW9615E91	I.C. SN74LS00N
U11	(See NOTE 2)	I.C. Programmed PROM
U12,U16,U58	51NW9615C94	I.C. SN74S00N
U13,U14, U25,U26	51NW9615F65	I.C. SN74S241N
U15	51NW9615B65	I.C. MC1455P1
U17,U49	51NW9615F41	I.C. DM74LS164N
U18,U61	51NW9615E27	I.C. 74S10PC
U19	51NW9615D26	I.C. 74S113N
U20	51NW9615A36	I.C. MC7406P
U21,U34,U38	51NW9615C21	I.C. SN74LS04N
U22	(See NOTE 2)	I.C. Programmed PROM
U23	51NW9615D31	I.C. 82S131F Programmable PROM (see NOTE 3)
U24,U33,U45	51NW9615F85	I.C. SN74S38N
U27	51NW9615G38	I.C. SN74LS38N

TABLE 5-4. VME110 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
U28	51NW9615G81	I.C. SN74LS132N
U29	51NW9615E33	I.C. 74S03A
U30	(See NOTE 2)	I.C. Programmed PROM
U31	51NW9615G10	I.C. SN74LS148N
U32	51NW9615E86	I.C. SN74LS151N
U36	51NW9615E93	I.C. SN74LS14N
U37	51NW9615C29	I.C. SN74LS174N
U41	51NW9615E77	I.C. SN74LS27N
U42	51NW9615E99	I.C. SN74LS374N
U43,U44	51NW9615C22	I.C. SN74LS08N
U46	51NW9615D27	I.C. SN74S32N
U47	48AW1019B01	K1135 Dual baud rate generator
U50	51NW9615J11	I.C. SN74S140N
U51	51NW9615H53	I.C. SN74LS09N
U52,U55,U59	51NW9615F02	I.C. 74LS244N
U53	51NW9615F59	I.C. MC68B40P
U56	51NW9615B29	I.C. MC1488L
U57	51NW9615D86	I.C. MC68B50P
U60	51NW9615B30	I.C. MC1489AL
U62	51NW9615H57	I.C. SN74LS194AN
U63	51NW9615E96	I.C. SN74LS245
Y1	48AW1016B01	Crystal oscillator, 16.0 MHz $\pm$ 0.05%
	02SW990D001	Nut, hex M 2.5 x .45 x 2 (2 req'd)
	02SW990D007	Nut, hex M 2 x .4 x 1.6 (4 req'd)
	03SW993D110	Screw, phillips, M 2 x .4 x 10 (4 req'd)

TABLE 5-4. VME110 Parts List (cont'd)

REFERENCE DESIGNATION	MOTOROLA PART NUMBER	DESCRIPTION
	03SW993D206	Screw, phillips, M 2.5 x .45 x 6 (3 req'd)
	03SW993D208	Screw, phillips, M 2.5 x .45 x 8 (2 req'd)
	04SW997D003	Washer, M 2.5 x .6 (2 req'd)
	04SW999D005	Washer, flat, M 2.7 x .5 (2 req'd)
	07-W4252B01	Bracket, card mounting (3 req'd)
	09NW9811A04	Socket, I.C., DIL, 16-pin, low profile (Use at U23)
	09NW9811A09	Socket, I.C., DIL, 18-pin, low profile (Use at U47)
XU1-XU8	09NW9811A21	Socket, I.C., DIL, 28-pin, low profile
	09NW9811A27	Socket, I.C., DIL, 20-pin, low profile (Use at U3, U11, U22, U30)
	09NW9811A30	Socket, I.C., DIL, 64-pin, low profile (Use at U4)
	09NW9811A46	Socket, 4-lead crystal oscillator (Use at Y1)
	29NW9805B17	Jumper, shorting insulated (Use at J1-J14, J16-J27)
	38NW9404B97	Cap, large snap-on, black
	38NW9404C04	Cap, snap-on, red
	64-W4301B01	Front panel, VME110
	33-W4365B02	Label, I.D., module

NOTES: (1) C43 and C44 are optional capacitors which are not installed but may be, at the discretion of the user. Refer to paragraph 4.3.4.2.

(2) When ordering, use number labeled on part. For programming details, see Appendix A.

(3) Must be programmed by user. Refer to paragraph 2.3.15.

5.4 SCHEMATIC DIAGRAMS

Figure 5-2 (14 sheets) contains detailed schematic diagrams of the various internal modules comprising the VME110. These schematic diagrams represent the latest design. Occasionally, minor component changes are made at the factory. Therefore, when replacing a component, always use the same value as the defective component even though the schematic diagram may indicate a different value or type.

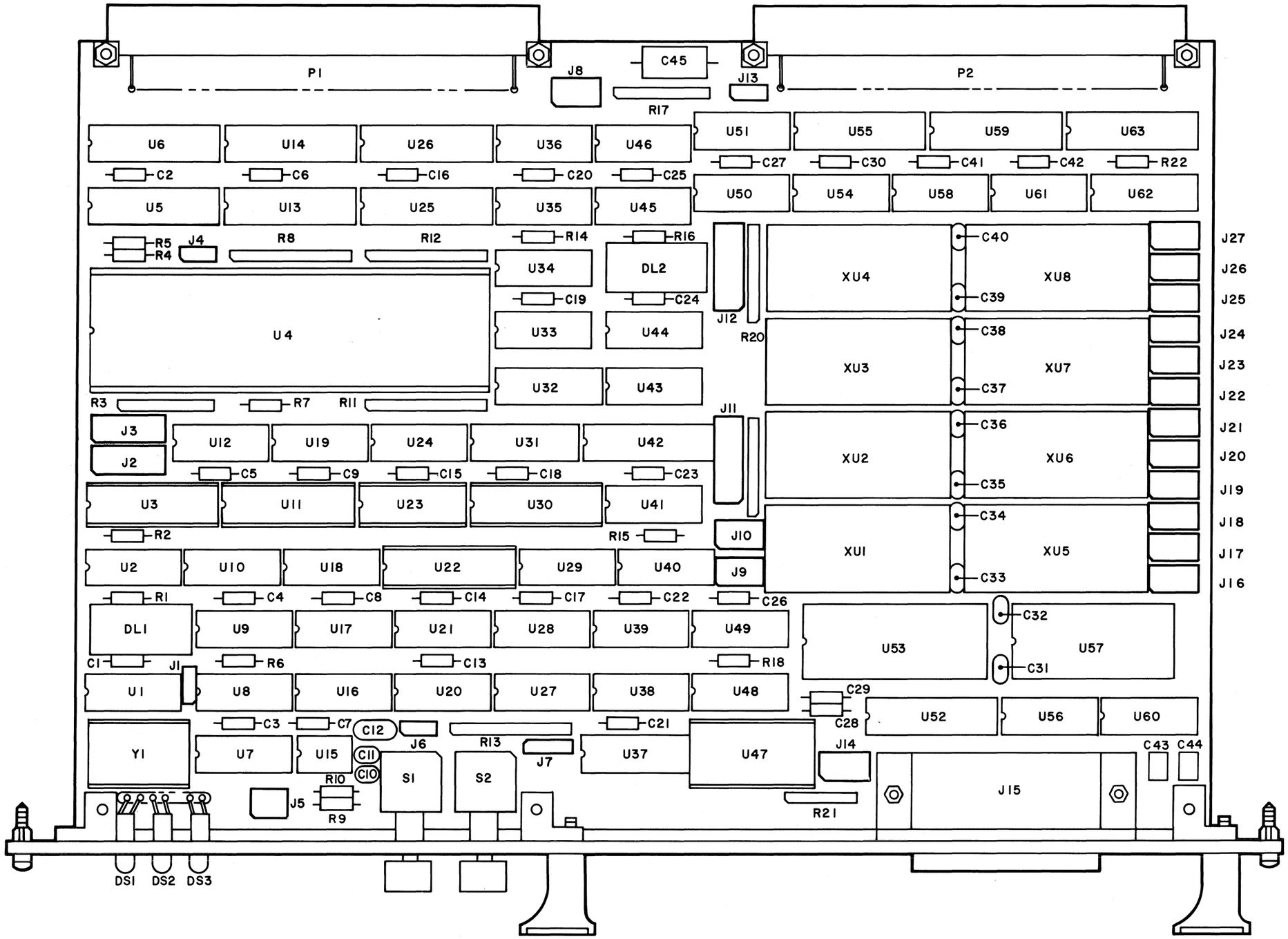


FIGURE 5-1. VME110 Module Parts Location Diagram

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	RELEASED FOR PILOT.	5-19-82	JMB GRA
	B	ECN H2925: SH13; CHANGED U58C PINS 9 AND 10. REF 9-9-82 GRO	9/16/82	
	C	ECN H3077: REVISED SH 7, ADDED SH TO SH REF AT [PROECT], SH 8, REVISED SH TO SH REF AT [RAMSEL]. SDL 11-18-82 DcT	11-22-82	

NOTES:
1. FOR REFERENCE DRAWINGS REFER TO BILL(S) OF MATERIAL 01-W3047B01.
2. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTORS ARE IN OHMS, ± 5PCT, 1/4 WATT.
   ALL CAPACITORS ARE IN UF.
   ALL VOLTAGES ARE DC.
3. INTERRUPTED LINES CODED WITH THE SAME LETTER OR LETTER COMBINATIONS ARE ELECTRICALLY CONNECTED.
4. DEVICE TYPE NUMBER IS FOR REFERENCE ONLY. THE NUMBER VARIES WITH THE MANUFACTURER.
5. SPECIAL SYMBOL USAGE:
   * DENOTES – ACTIVE LOW SIGNAL.
   [] DENOTES – ON BOARD SIGNAL.
6. INTERPRET DIAGRAM IN ACCORDANCE WITH AMERICAN NATIONAL STANDARDS INSTITUTE SPECIFICATIONS, CURRENT REVISION.
7. PART TYPES ARE ABBREVIATED IN THE FIELD OF THE DRAWING, FOR FULL PART TYPE, REFER TO TABLE 1.
8. NOT INSTALLED,USERS OPTION.
9. NUMBERS IN PARENTHESES ARE FOR 24 PIN DEVICES. REFER TO MANUFACTURER'S CATALOGUE FOR MNEMONICS.

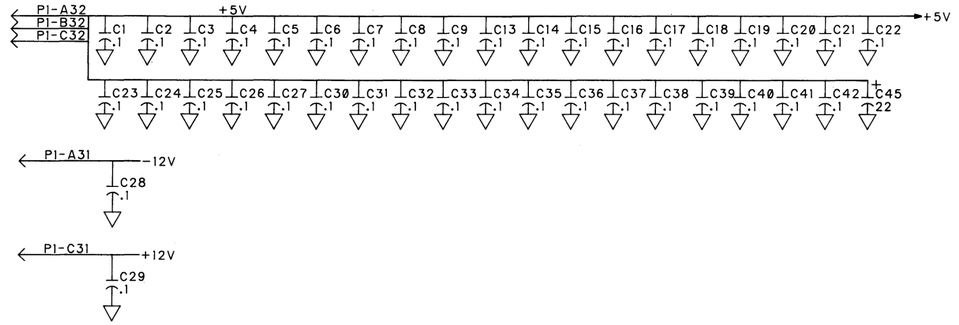


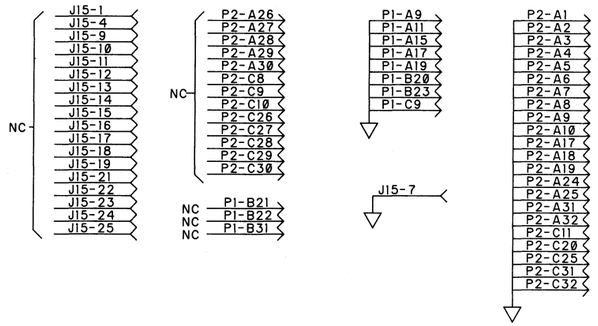
TABLE 1 (7)

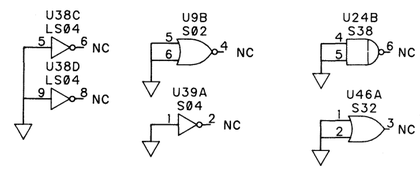
REF DES	TYPE (4)	GND	+5V	+12V	-12V
U1	74LS393	7	14		
U2	74S74	7	14		
U3	PAL16L8	10	20		
U4	MC68000L	53,16	49,14		
U5	74LS645-1	10	20		
U6	74LS645-1	10	20		
U7	74LS125	7	14		
U8	74S04	7	14		
U9	74S02	7	14		
U10	74LS00	7	14		
U11	PAL16L8	10	20		
U12	74S00	7	14		
U13	74S241	10	20		
U14	74S241	10	20		
U15	MC1455	1	8		
U16	74S00	7	14		
U17	74LS164	7	14		
U18	74S10	7	14		
U19	74S113	7	14		
U20	7406	7	14		
U21	74LS04	7	14		
U22	PAL16L8	10	20		
U23	82S131	8	16		
U24	74S38	7	14		
U25	74S241	10	20		
U26	74S241	10	20		
U27	74LS38	7	14		
U28	74LS132	7	14		
U29	74S03	7	14		
U30	PAL16L8	10	20		
U31	74LS148	8	16		
U32	74LS151	8	16		
U33	74S38	7	14		
U34	74LS04	7	14		
U35	74LS393	7	14		
U36	74LS14	7	14		
U37	74LS174	8	16		
U38	74LS04	7	14		

TABLE 1 (7)

REF DES	TYPE (4)	GND	+5V	+12V	-12V
U39	74S04	7	14		
U40	74S04	7	14		
U41	74LS27	7	14		
U42	74LS374	10	20		
U43	74LS08	7	14		
U44	74LS08	7	14		
U45	74S38	7	14		
U46	74S32	7	14		
U47	K1135B	11	2	9	
U48	74LS00	7	14		
U49	74LS164	7	14		
U50	74S140	7	14		
U51	74LS09	7	14		
U52	74LS244	10	20		
U53	MC68B40	1	14		
U54	74S02	7	14		
U55	74LS244	10	20		
U56	MC1488	7		14	1
U57	MS68B50	1	12		
U58	74S00	7	14		
U59	74LS244	10	20		
U60	MC1489	7	14		
U61	74S10	7	14		
U62	74LS194	8	16		
U63	74LS245	10	20		
DL1	50NS (DL)	7	14		
DL2	50NS (DL)	7	14		
Y1	K1148A	7	14		
XU1	SOCKET	14	28		
XU2	SOCKET	14	28		
XU3	SOCKET	14	28		
XU4	SOCKET	14	28		
XU5	SOCKET	14	28		
XU6	SOCKET	14	28		
XU7	SOCKET	14	28		
XU8	SOCKET	14	28		

Y1	
XU8	
U63	
S2	
R22	
P2	
J27	
DS3	
DL2	
C45	
HIGHEST NUMBER USED	NOT USED
REFERENCE DESIGNATIONS	





63EW3047B REV C SH 1 OF 14

	A	A	B	A								
	11	12	13	14								
	A	C	C	A	A							
	6	7	8	9	10							
REV STATUS OF SHEETS	REV	C	A	A	A	A						
	SH	1	2	3	4	5						

DWG NO 63EW3047B SH 1

UNLESS OTHERWISE SPECIFIED: DIMENSIONS IN INCHES; METRIC DIMENSIONS IN MILLIMETERS; REMOVE ALL BURRS AND SHARP EDGES; SURFACE TEXTURE IN MICRONCHES; TOLERANCE: 2 PLACE DEC ±, 3 PLACE DEC ±, ANGLES ±

DRAWN BY	A. DEFOREST	DATE 5-17-82
CHECKED BY	M. MC KINNEY	DATE 5-17-82
PROJECT LEADER	J. BURGER	DATE 5-17-82
DESIGN MANAGER	N.L. WAGNER	DATE 5-17-82
MFG ENGINEER	J. SCHWAB	DATE 5-17-82
DESIGN ENGINEER	J. BURGER	DATE 5-17-82

DESCRIPTION | PART NO

MOTOROLA INC.
MOS Integrated Circuits Division
MICROSYSTEMS
3102 North 56th Street, Phoenix, Arizona 85018 U.S.A.

TITLE: SCHEMATIC DIAGRAM - VME110

E | FSCM NO | DRAWING NO 63EW3047B | SCALE: NONE | SHEET 1 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 1 of 14) 5-15/5-16

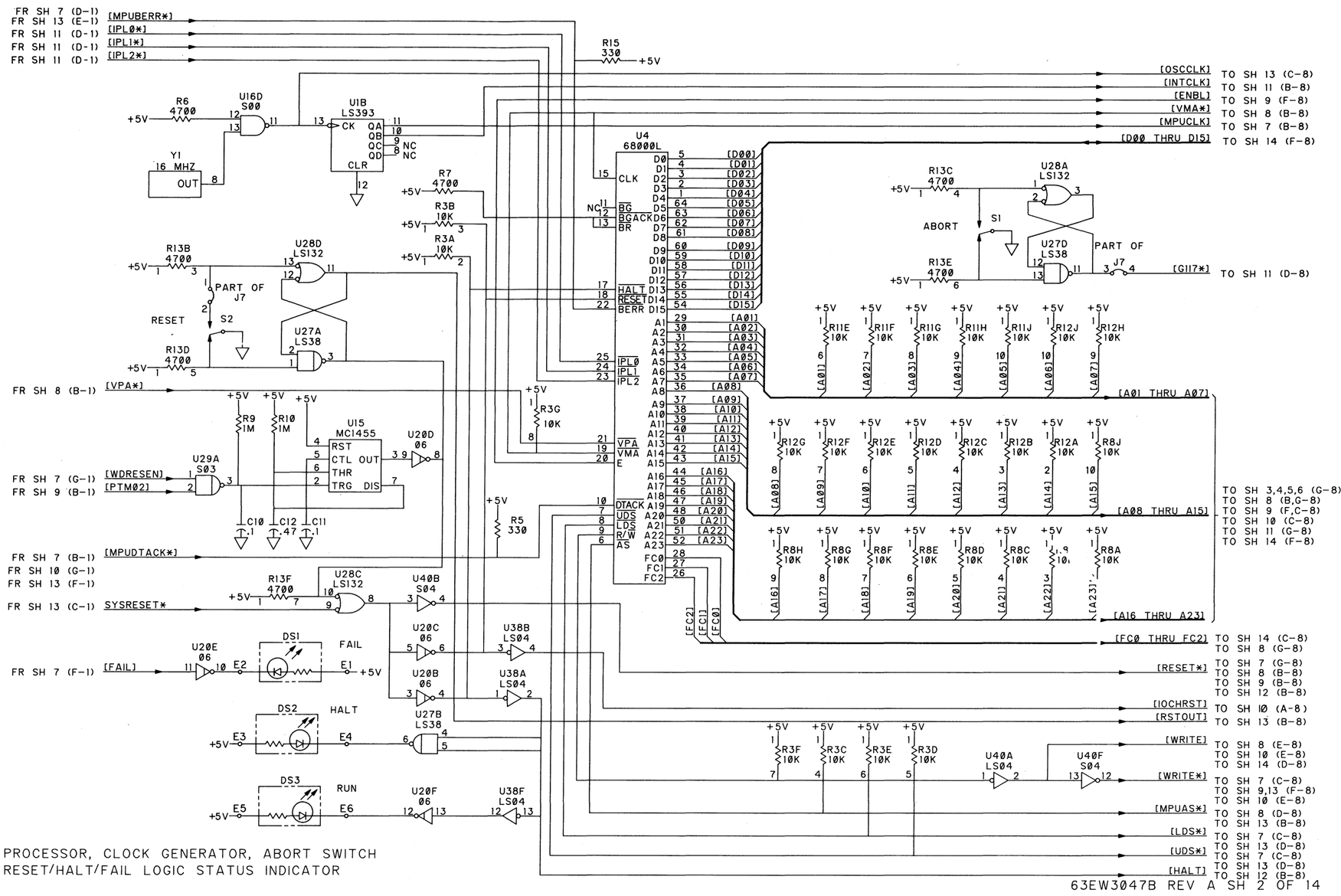


FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 2 of 14) 5-17/5-18

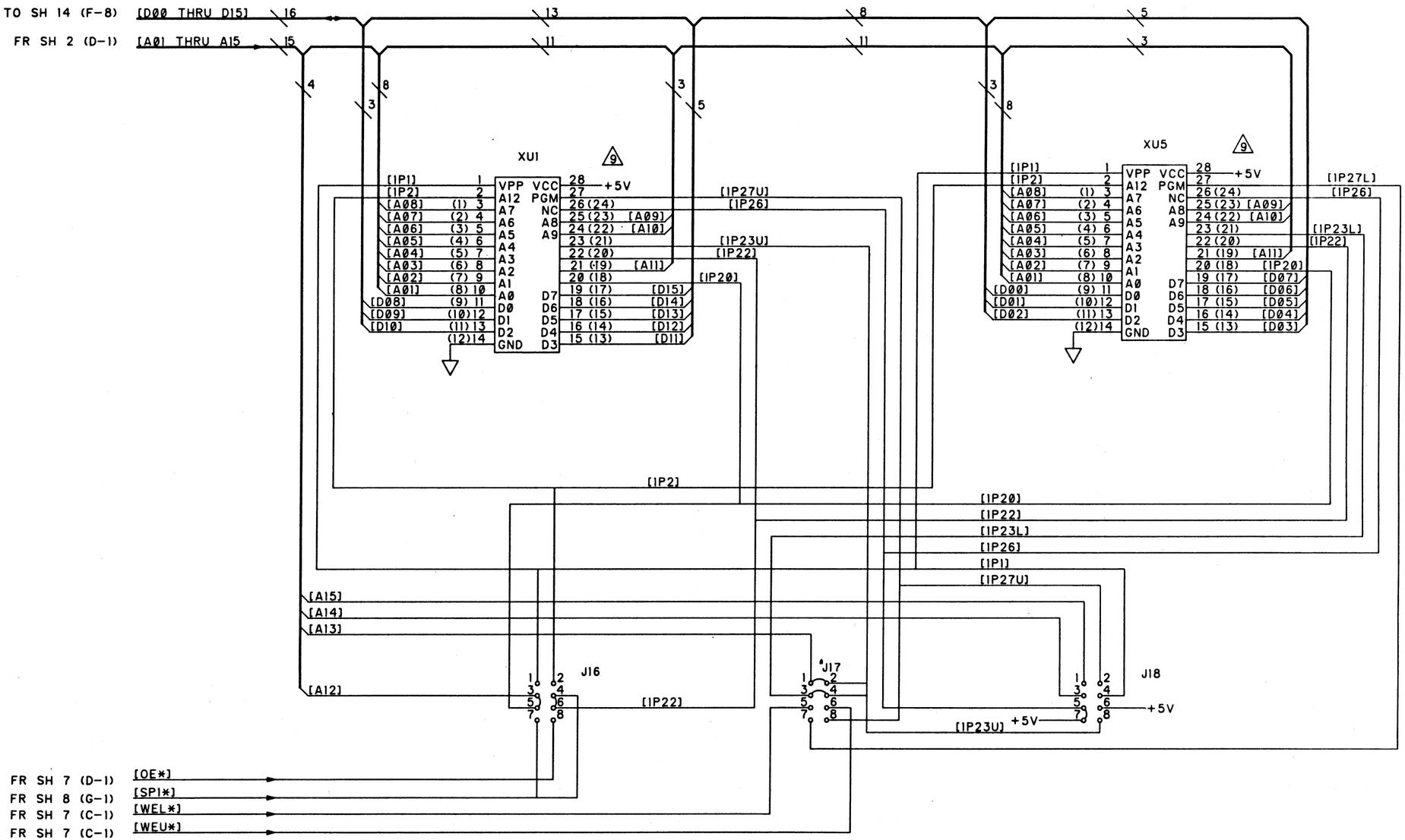
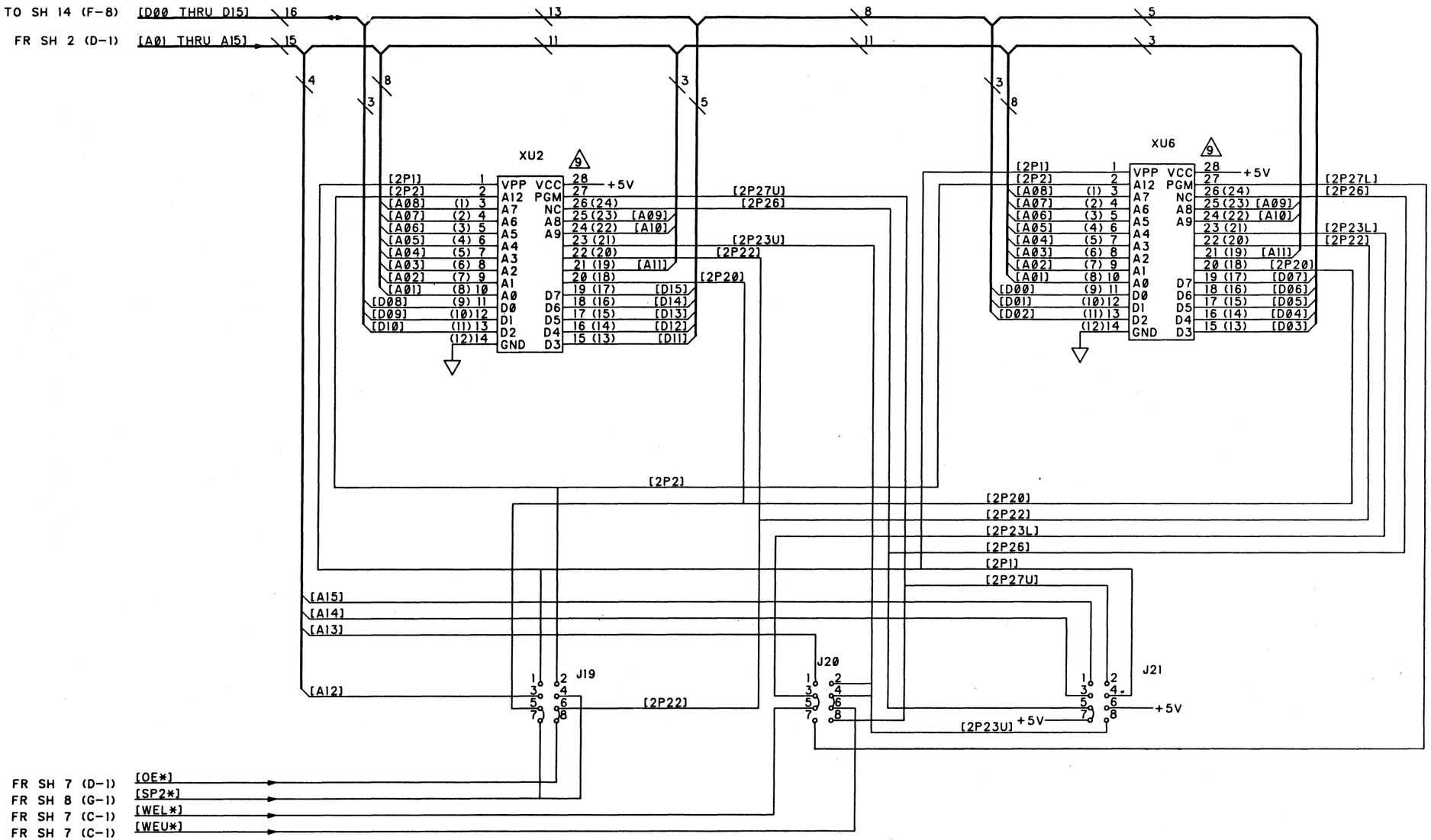
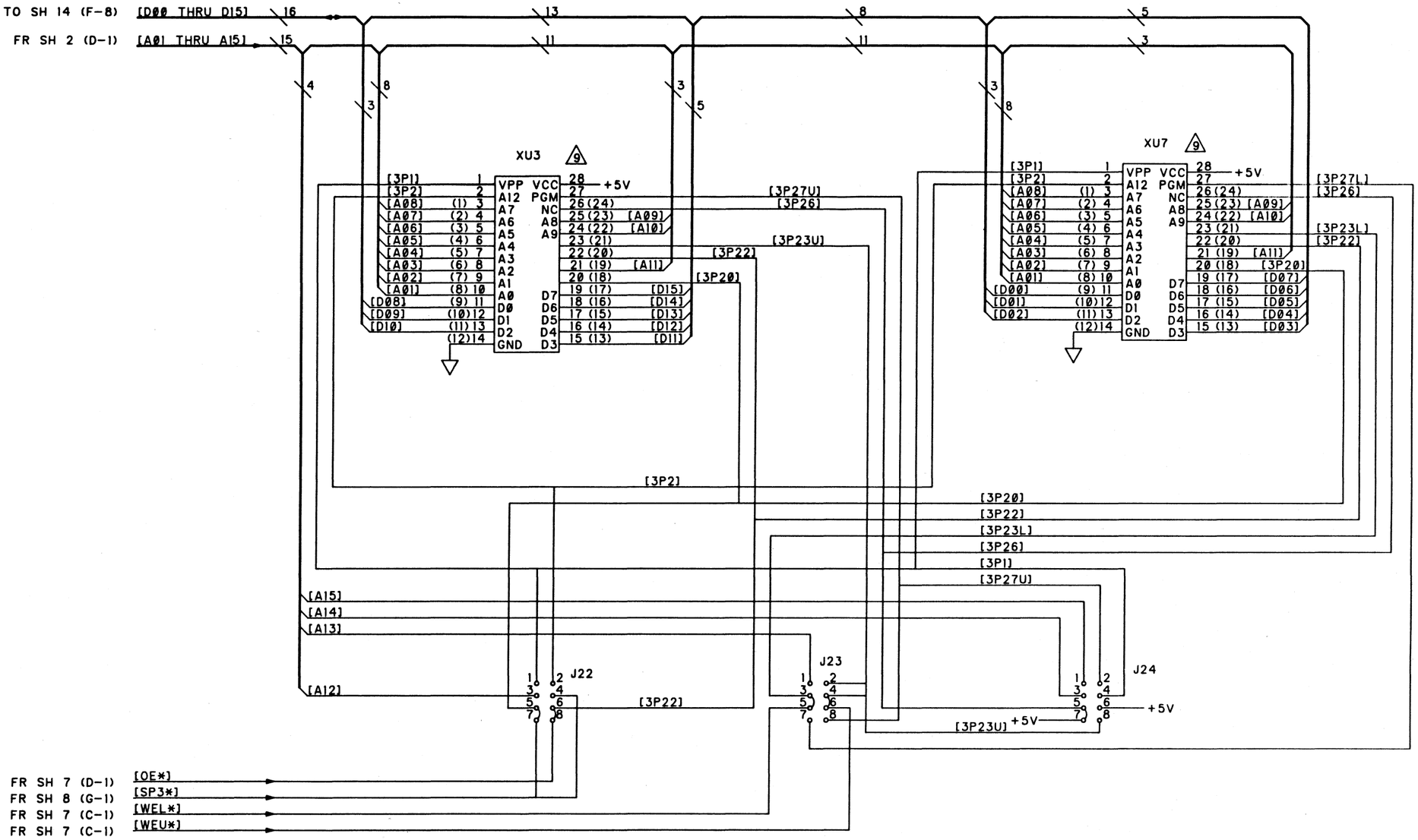


FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 3 of 14) 5-19/5-20



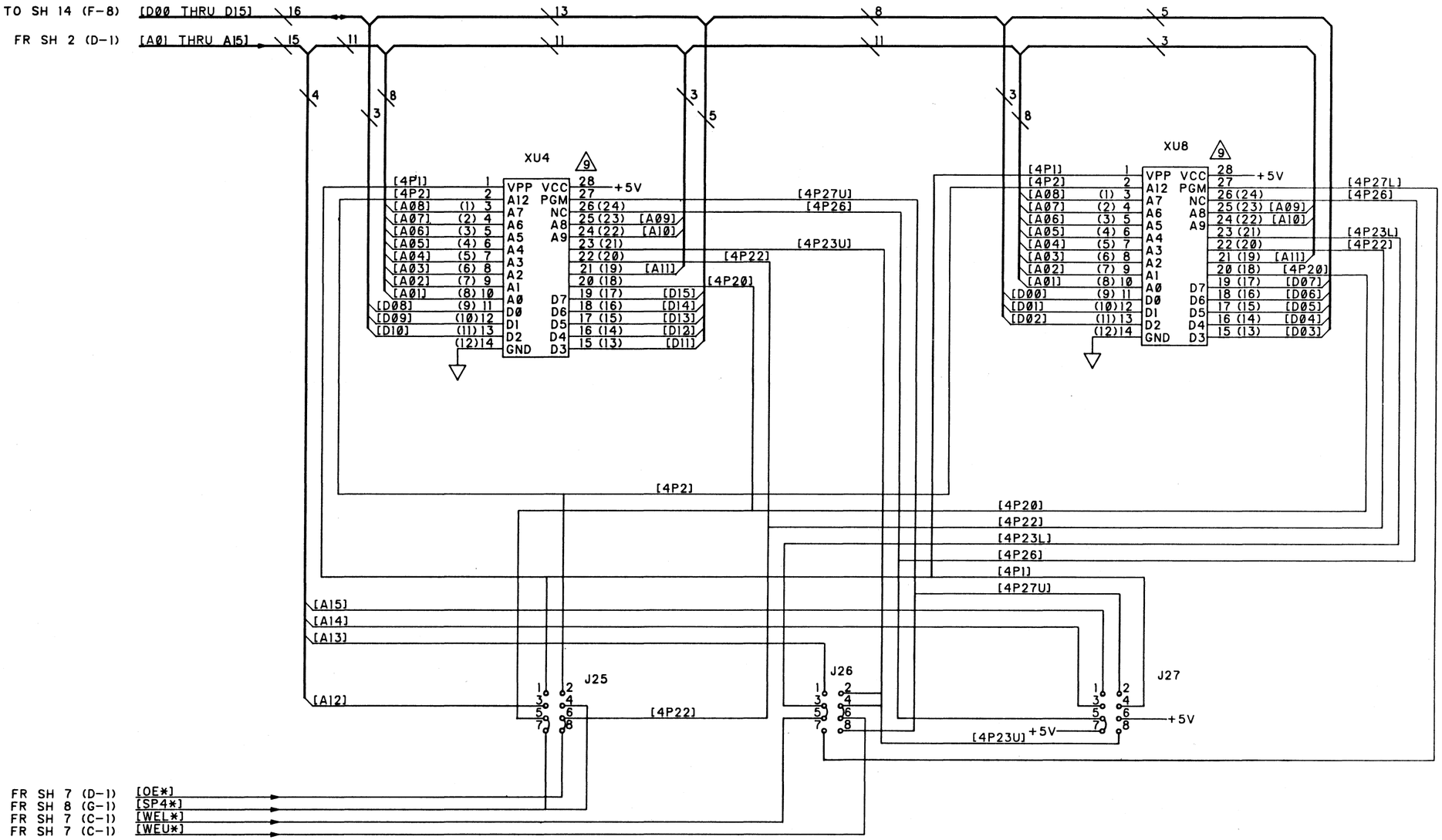
RAM/ROM
63EW3047B REV A SH 4 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 4 of 14) 5-21/5-22



RAM/ROM
63EW3047B REV A SH 5 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 5 of 14) 5-23/5-24



RAM/ROM
63EW3047B REV A SH 6 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 6 of 14) 5-25/5-26

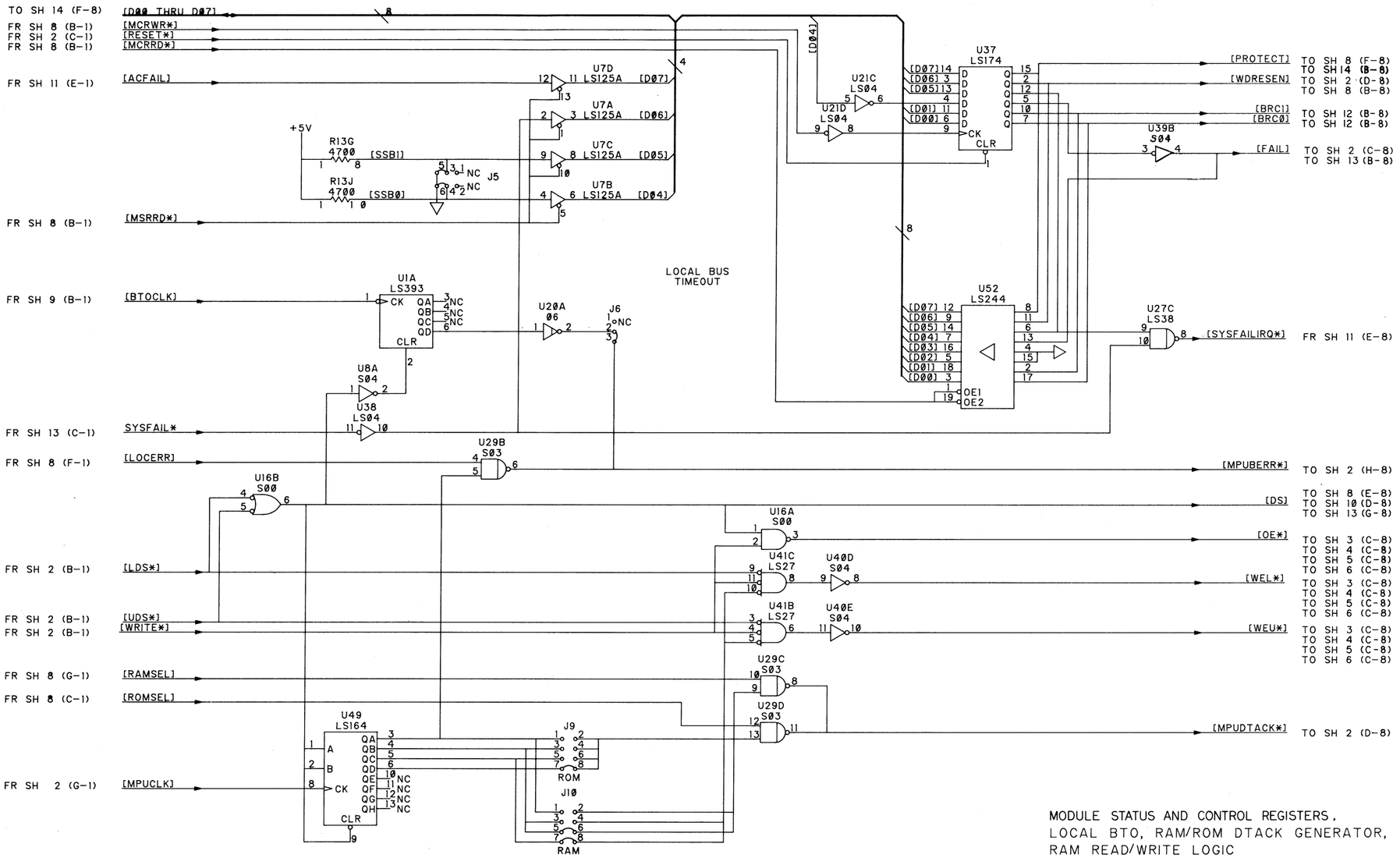


FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 7 of 14) 5-27/5-28

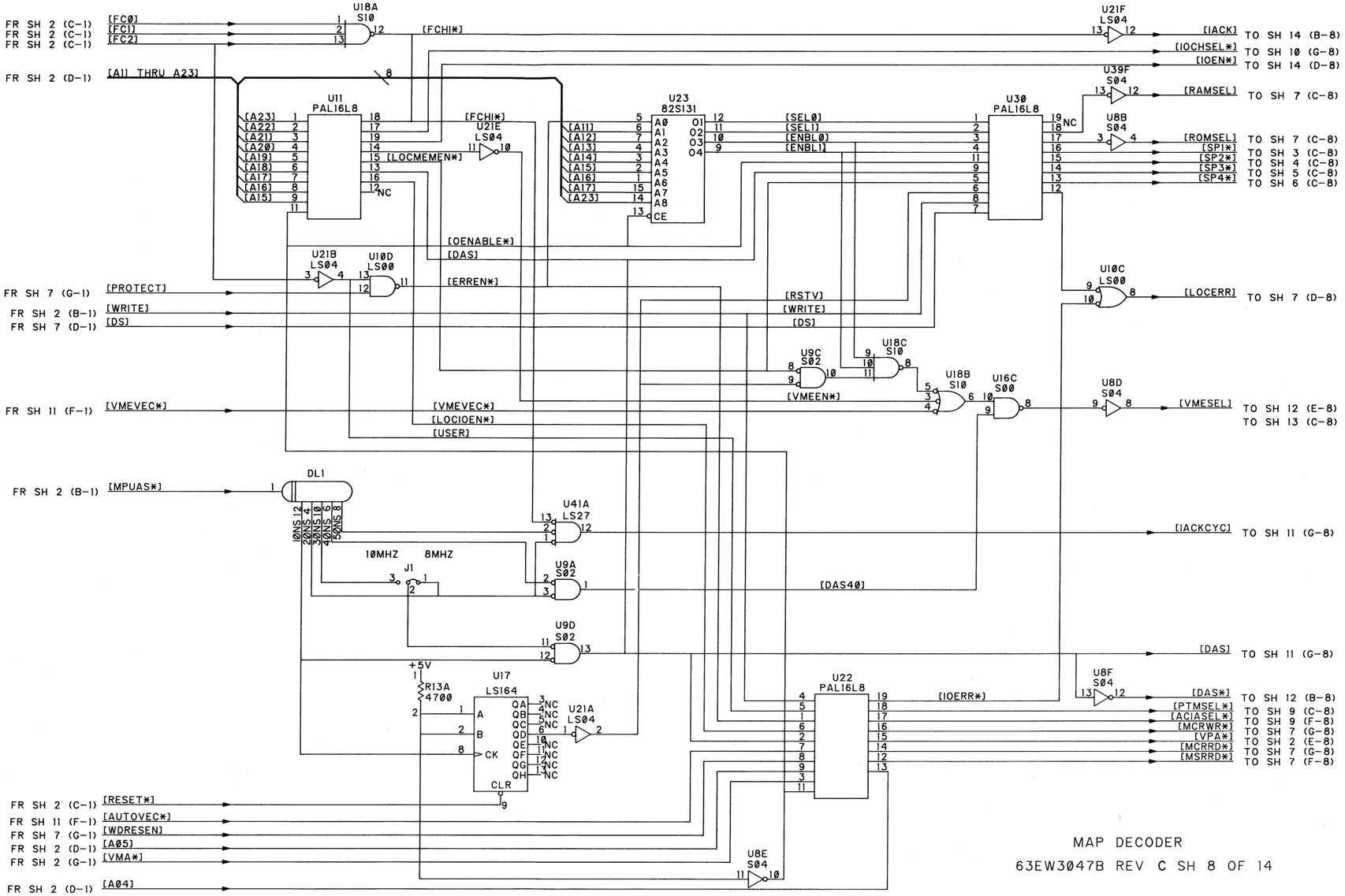
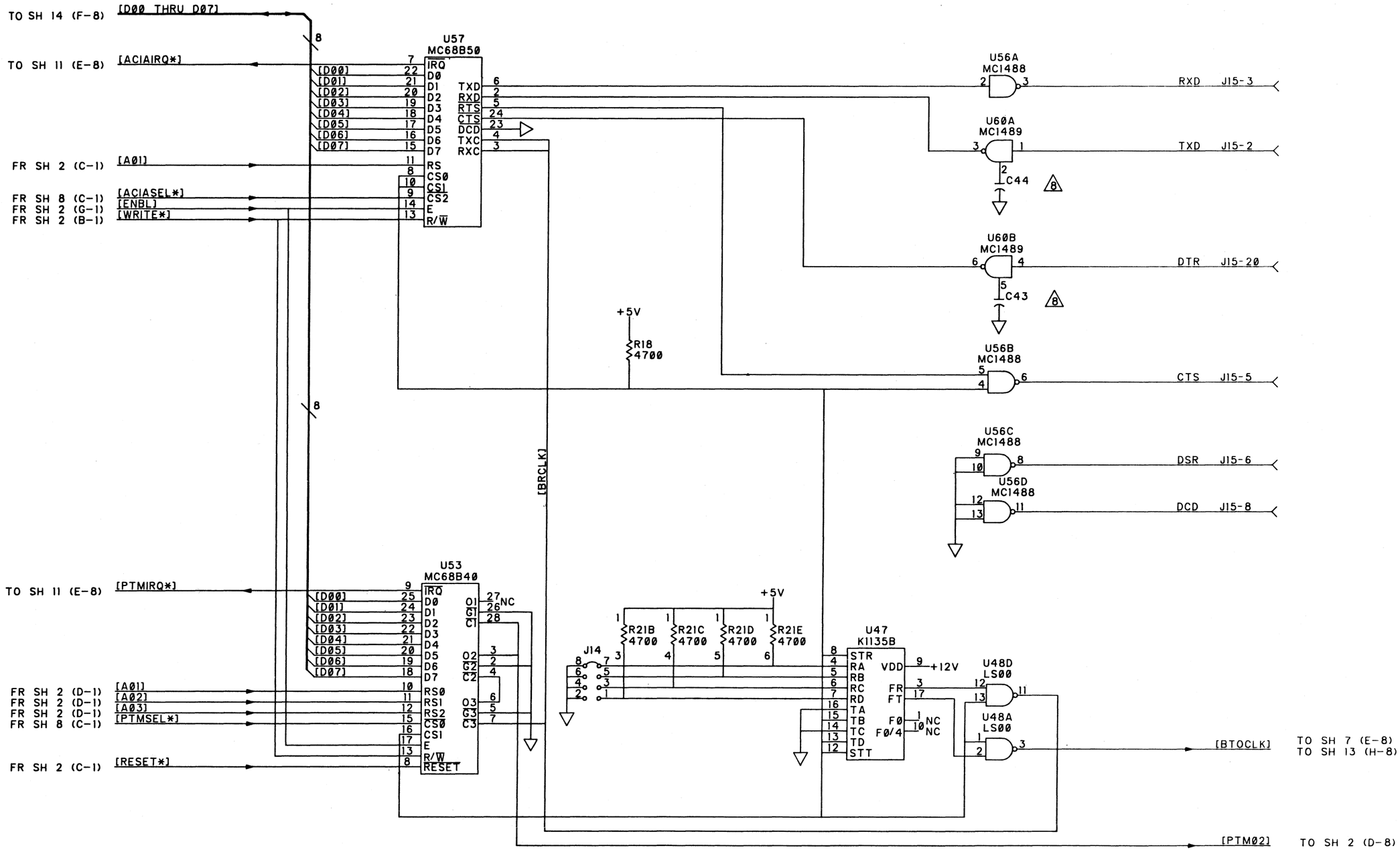


FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 8 of 14) 5-29/5-30



SERIAL PORT, TIMER
BTO CLOCK GENERATOR
63EW3047B REV A SH 9 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 9 of 14) 5-31/5-32

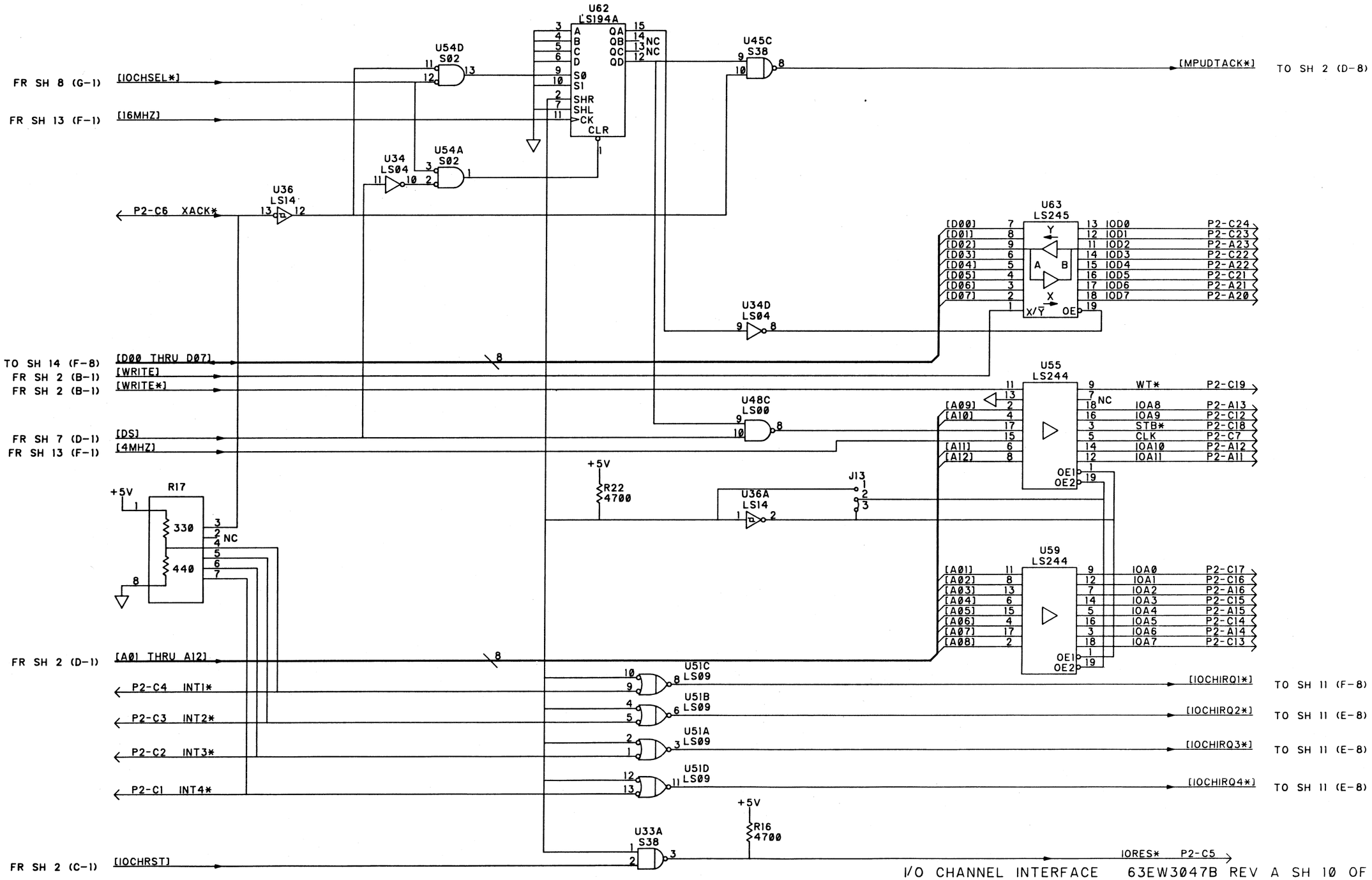
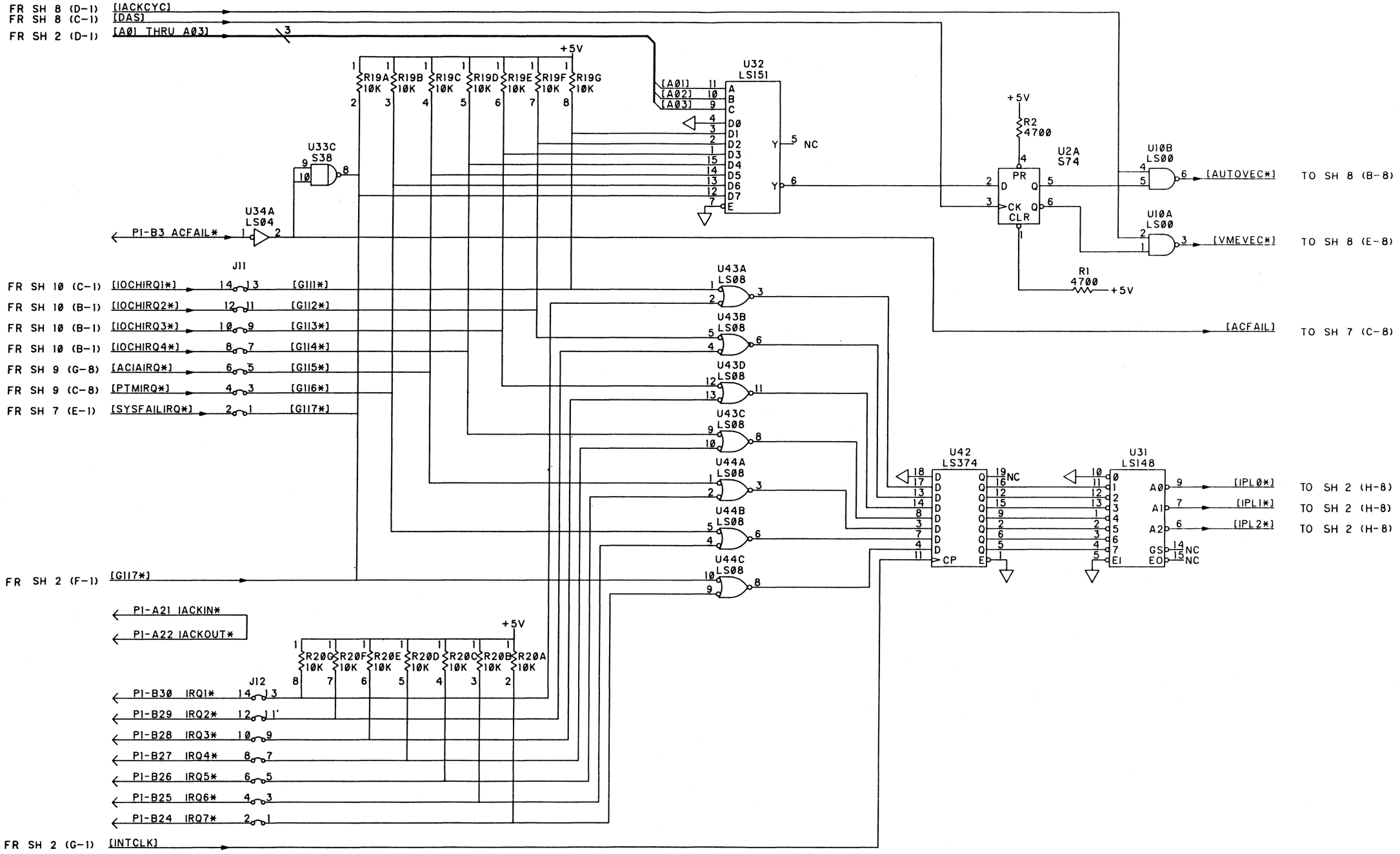


FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 10 of 14) 5-33/5-34



INTERRUPT HANDLER
63EW3047B REV A SH 11 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 11 of 14) 5-35/5-36

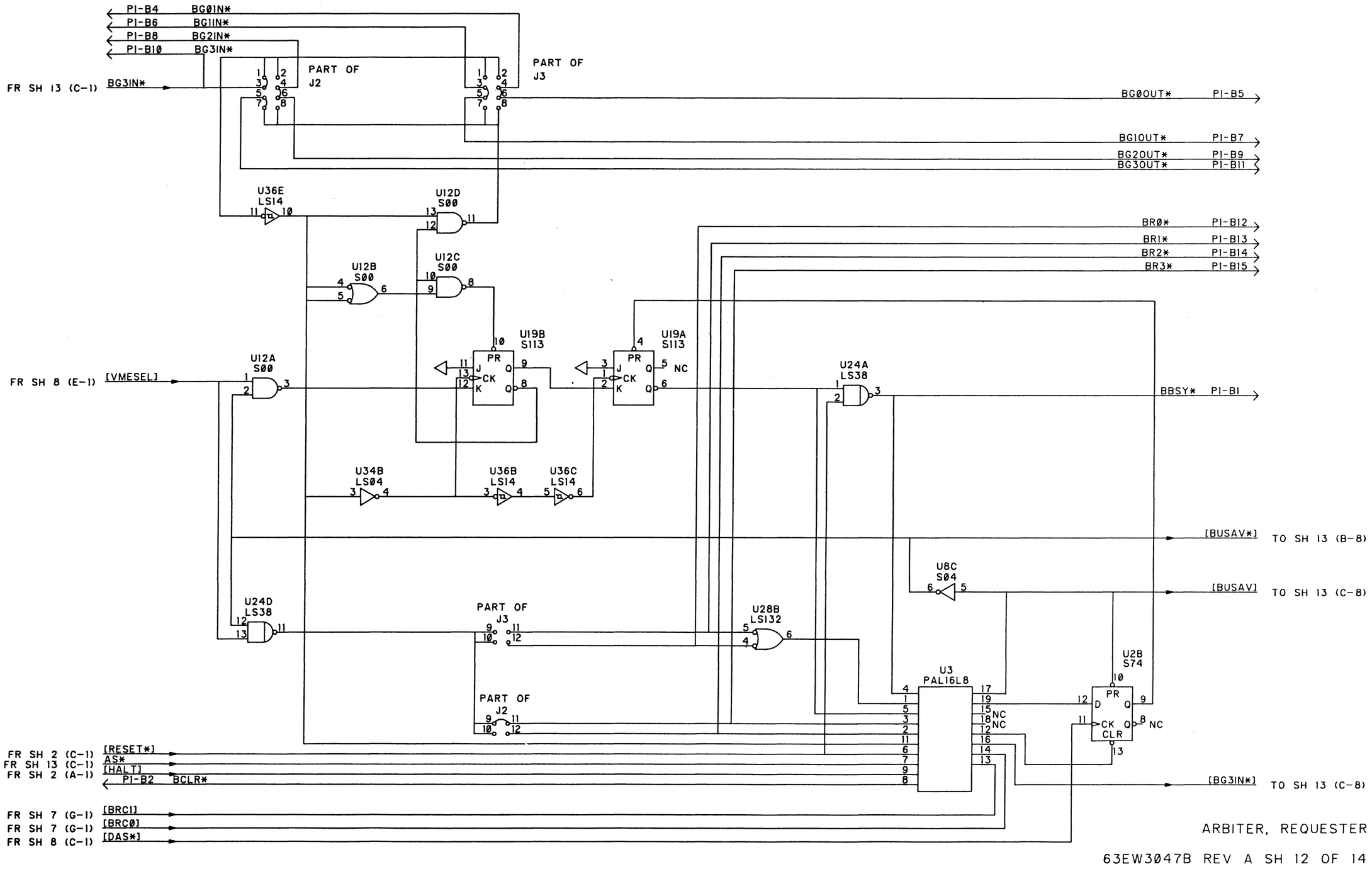
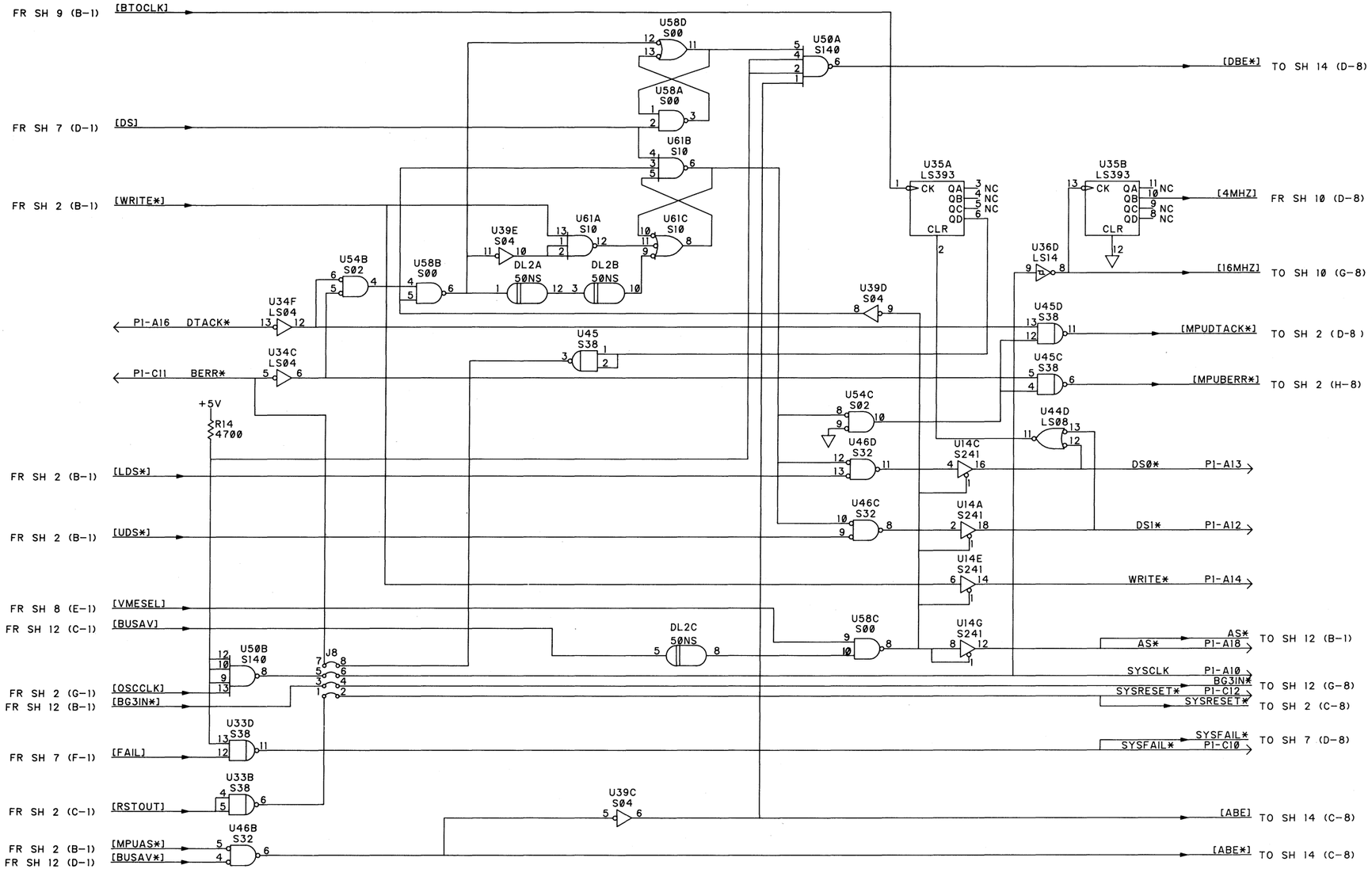
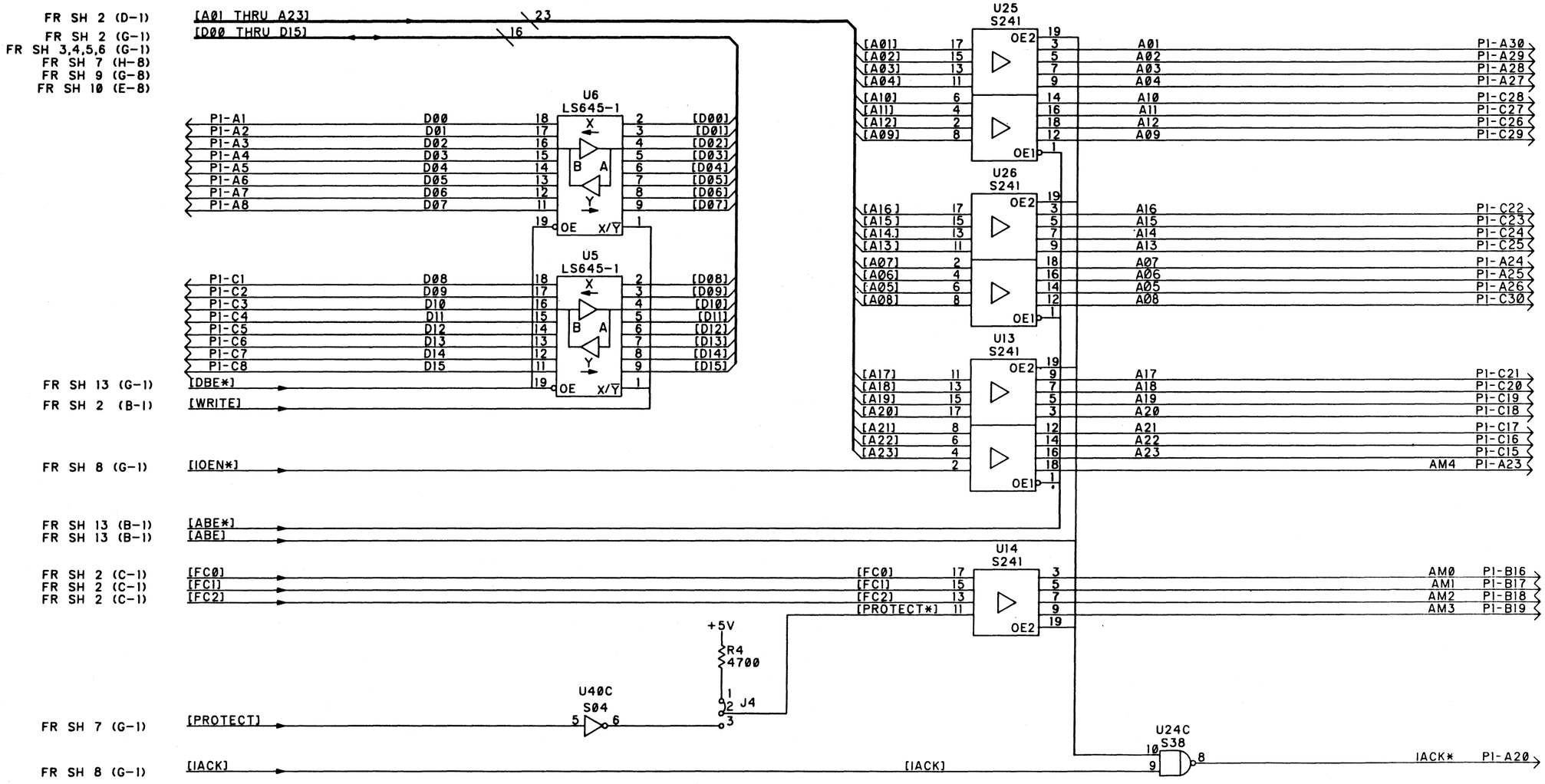


FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 12 of 14) 5-37/5-38



VME INTERFACE
63EW3047B REV B SH 13 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 13 of 14) 5-39/5-40



VME INTERFACE
63EW3047B REV A SH 14 OF 14

FIGURE 5-2. VME110 Module Schematic Diagram (Sheet 14 of 14) 5-41/5-42

APPENDIX A

PROGRAMMABLE ARRAY LOGIC PROGRAM DETAILS

INTRODUCTION

The four type 16L8 Programmable Array Logic (PAL) chips in VME110 are 20-pin I.C.'s designated U3, U11, U22, and U30. This appendix lists the pinouts and output logic equations for each.

U3 PAL

The pinout for U3 is:

PIN NUMBER	SIGNAL MNEMONIC	PIN NUMBER	SIGNAL MNEMONIC
1	BRLO	11	BG
2	BR2	12	BREL
3	BR3	13	BRC1
4	BBSY	14	BRC0
5	LBSY	15	BG3H
6	RESET	16	BG3L
7	AS	17	BAVH
8	BCLR	18	BAVL
9	HALT	19	BREN
10	GND	20	VCC

Outputs for U3 all depend on VCC being high. The output equations are:

$$\overline{BREL} = LBSY \cdot \overline{AS} \cdot BRC1 \cdot \overline{BRC0} \cdot \overline{BAVL} + HALT \cdot \overline{BAVL}$$

$$\overline{BREN} = BRLO \cdot \overline{BRC1} \cdot \overline{BRC0} \cdot \overline{BAVL} + \overline{BR2} \cdot \overline{BRC1} \cdot \overline{BRC0} \cdot \overline{BAVL} + \overline{BR3} \cdot \overline{BRC1} \cdot \overline{BRC0} \cdot \overline{BAVL} + \overline{BCLR} \cdot \overline{BRC1} \cdot BRC0 \cdot \overline{BAVL}$$

$$\overline{BAVL} = RESET \cdot LBSY \cdot AS \cdot \overline{BG} + \overline{RESET} \cdot LBSY + BAVH$$

$$\overline{BAVH} = \overline{RESET} \cdot \overline{LBSY} + \overline{LBSY} \cdot AS + BAVL$$

$$\overline{BG3L} = RESET \cdot \overline{BR3} \cdot BBSY + BG3H$$

$\overline{BG3H}$ = $\overline{RESET}$

+ $\overline{BBSY}$

+ BG3L

U11 PAL

The pinout for U11 is:

PIN NUMBER	SIGNAL MNEMONIC	PIN NUMBER	SIGNAL MNEMONIC
1	A23	11	OE
2	A22	12	NC
3	A21	13	DAS
4	A20	14	VME
5	A19	15	LOCM
6	A18	16	LOCIO
7	A17	17	IOCH
8	A16	18	FCHI
9	A15	19	IOEN
10	GND	20	VCC

Outputs for U11 all depend on OE being low ($\overline{OE}$). The output equations are:

$\overline{IOEN}$ = A23•A22•A21•A20•A19•A18•A17•A16•FCHI

$\overline{IOCH}$ = A23•A22•A21•A20•A19•A18•A17•$\overline{A16}$•$\overline{A15}$•FCHI•DAS

$\overline{LOCIO}$ = A23•A22•A21•A20•A19•A18•A17•$\overline{A16}$•A15•FCHI

$\overline{LOCM}$ = A23•A22•A21•A20•$\overline{A19}$•$\overline{A18}$•FCHI

+ $\overline{A23}$•$\overline{A22}$•$\overline{A21}$•$\overline{A20}$•$\overline{A19}$•$\overline{A18}$•FCHI

$\overline{VME}$ = A23•A22•A21•A20•A19•A18•A17•$\overline{A16}$•FCHI

+ A23•A22•A21•A20•$\overline{A19}$•$\overline{A18}$•FCHI

+ $\overline{A23}$•$\overline{A22}$•$\overline{A21}$•$\overline{A20}$•$\overline{A19}$•$\overline{A18}$•FCHI

+ $\overline{FCHI}$

$\overline{NC}$ = OE

U22 PAL

The pinout for U22 is:

PIN NUMBER	SIGNAL MNEMONIC	PIN NUMBER	SIGNAL MNEMONIC
1	EREN	11	OE
2	DAS	12	MSRRD
3	VMA	13	A4
4	WR	14	MCRRD
5	USER	15	VPA
6	LOCIO	16	MCRWR
7	AVEC	17	ACIA
8	WDRE	18	PTM
9	A5	19	IOERR
10	GND	20	VCC

Outputs for U22 all depend on OE being low ($\overline{OE}$). The output equations are:

$$\overline{VPA} = \overline{LOCIO} \cdot DAS + \overline{AVEC} \cdot DAS$$

$$\overline{IOERR} = \overline{A5} \cdot A4 \cdot \overline{VMA} \cdot \overline{LOCIO} \cdot \overline{EREN} \cdot WDRE + A5 \cdot \overline{A4} \cdot \overline{VMA} \cdot \overline{LOCIO} \cdot WR \cdot USER + A5 \cdot A4 \cdot \overline{VMA} \cdot \overline{LOCIO} \cdot WR$$

$$\overline{ACIA} = \overline{A5} \cdot \overline{A4} \cdot \overline{VMA} \cdot \overline{LOCIO}$$

$$\overline{PTM} = \overline{A5} \cdot A4 \cdot \overline{VMA} \cdot \overline{LOCIO} \cdot \overline{WDRE} + \overline{A5} \cdot A4 \cdot \overline{VMA} \cdot \overline{LOCIO} \cdot EREN$$

$$\overline{MCRWR} = A5 \cdot \overline{A4} \cdot \overline{VMA} \cdot \overline{LOCIO} \cdot WR \cdot \overline{USER}$$

$$\overline{MCRRD} = A5 \cdot \overline{A4} \cdot \overline{VMA} \cdot \overline{LOCIO} \cdot \overline{WR}$$

$$\overline{MSRRD} = A5 \cdot A4 \cdot \overline{VMA} \cdot \overline{LOCIO} \cdot \overline{WR}$$

U30 PAL

The pinout for U30 is:

PIN NUMBER	SIGNAL MNEMONIC	PIN NUMBER	SIGNAL MNEMONIC
1	SEL0	11	OE
2	SEL1	12	ERR
3	ENBL0	13	SP4
4	ENBL1	14	SP3
5	LOCM	15	SP2
6	RSTV	16	SP1
7	DS	17	ROM
8	WR	18	RAM
9	DAS	19	NC
10	GND	20	VCC

Outputs of U30 all depend on OE being low ($\overline{OE}$). The output equations are:

$$\overline{RAM} = \overline{ENBL1}\cdot\overline{ENBL0}\cdot RSTV\cdot\overline{LOCM}\cdot DS\cdot DAS$$
$$+\ \overline{ENBL1}\cdot ENBL0\cdot\overline{WR}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$

$$\overline{ROM} = ENBL1\cdot\overline{ENBL0}\cdot\overline{WR}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$
$$+\ RSTV\cdot DS\cdot DAS$$

$$\overline{ERR} = \overline{ENBL1}\cdot ENBL0\cdot WR\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$
$$+\ ENBL1\cdot\overline{ENBL0}\cdot WR\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$

$$\overline{SP1} = RSTV\cdot DS\cdot DAS$$
$$+\ \overline{ENBL1}\cdot\overline{ENBL0}\cdot\overline{SEL1}\cdot\overline{SEL0}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$
$$+\ \overline{ENBL1}\cdot ENBL0\cdot\overline{SEL1}\cdot\overline{SEL0}\cdot\overline{WR}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$
$$+\ ENBL1\cdot\overline{ENBL0}\cdot\overline{SEL1}\cdot\overline{SEL0}\cdot\overline{WR}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$

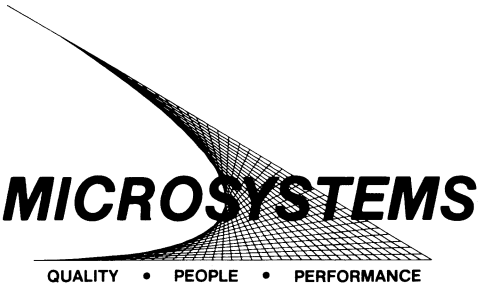
$$\overline{SP2} = \overline{ENBL1}\cdot\overline{ENBL0}\cdot\overline{SEL1}\cdot SEL0\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$
$$+\ \overline{ENBL1}\cdot ENBL0\cdot\overline{SEL1}\cdot SEL0\cdot\overline{WR}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$
$$+\ ENBL1\cdot\overline{ENBL0}\cdot\overline{SEL1}\cdot SEL0\cdot\overline{WR}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$

$$\overline{SP3} = \overline{ENBL1}\cdot\overline{ENBL0}\cdot SEL1\cdot\overline{SEL0}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$
$$+\ \overline{ENBL1}\cdot ENBL0\cdot SEL1\cdot\overline{SEL0}\cdot\overline{WR}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$
$$+\ ENBL1\cdot\overline{ENBL0}\cdot SEL1\cdot\overline{SEL0}\cdot\overline{WR}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$

$$\overline{SP4} = \overline{ENBL1}\cdot\overline{ENBL0}\cdot SEL1\cdot SEL0\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$
$$+\ \overline{ENBL1}\cdot ENBL0\cdot SEL1\cdot SEL0\cdot\overline{WR}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$
$$+\ ENBL1\cdot\overline{ENBL0}\cdot SEL1\cdot SEL0\cdot\overline{WR}\cdot\overline{RSTV}\cdot\overline{LOCM}\cdot DS\cdot DAS$$

$$\overline{NC} = OE$$

SUGGESTION/PROBLEM REPORT



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