MM65K Memory Board

User's Manual

MORROW DESIGNS

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1. INTRODUCTION

Bank select, PHANTOM, extended addressing, fast access time, low power consumption, and IEEE compatible are some of the words that are used to describe Memory products. We at Morrow Designs have made these words a reality with the introduction of the Morrow Designs MM65K16S Memory Board.

The Morrow Designs MM65K16S Static RAM is, without a doubt the most versatile memory board on the market today. With so many features at a price that is affordable, the MM65K16S is an unsurpassed value.

Bank select or extended addressing; you have a choice. The bank select feature is switch setable to any one of 256 available I/O addresses and will respond to any one or combination of the eight data bits that are desired. Extended addressing allows the MM65K16S to reside anywhere in the memory map with no imposed limitations by the addressing range of the microcomputer system.

The MM65K16S draws an average of 5ØØ milliamps (Ma) of current with code executing in RAM and some boards have measured considerably less under the same circumstances. With such a low current drain, it is obvious that only 1 regulator is needed, but for those planning to use a programmed 2716 EPROM or equivalent PROM, extra current demands can easily be met by the three on board regulators. For those dedicated applications where both RAM and ROM are needed, the MM65K16S RAM Board really fits the bill.

The Morrow Designs MM65K16S is guaranteed to run with any 8Ø8Ø, Z8Ø, or 8Ø85 processor on the market today. This includes some of the new 6 MHZ processors that are beginning to surface. In fact, the MM65K16S is guaranteed to run reliably with processors that have clock speeds up to 6 MHZ.

2. OVERVIEW

Before installing the memory board, please read the instructions in this manual. The Morrow Designs MM65K16S is a very sophisticated RAM board and has many options that must be set correctly for proper operation of the system.

Chapter 4 - INSTALLATION PROCEDURES - is an introduction to the Morrow Designs MM65K16S Static RAM board. It deals with the configuration, features, and use of the board. This section provides elaborate coverage of all the most used features and provides a great number of examples to help simplify the set up and testing of the board.

Chapter 5 - SPECIAL APPLICATION NOTES - deals with what the Morrow Designs call "the nice little things to know". This section deals with the special application notes that are necessary for only a few users, but can save time and money in the long run when the system in use has a need for one of these particular features.

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|-------------------------------------------------------------|
|WARNING....NEVER INSERT OR REMOVE THE MORROW DESIGNS  OR ANY  |
|OTHER BOARD WITH POWER ON.  ALWAYS REMOVE POWER FROM THE BUS  |
|AS SERIOUS ELECTRICAL DAMAGE COULD OCCUR TO THE SYSTEM AND    |
|THE BOARD OR BOARDS THAT WERE REMOVED OR INSTALLED.           |
|-------------------------------------------------------------|
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3. SPECIFICATIONS

SPECIFICATIONS FOR THE MORROW DESIGNS MM65K16S

POWER REQUIREMENTS:

8V @ 550-625 MAX 350 MA TYPICAL
+/- 16V NOT USED

RAM CHIPS:

M58725P OR EQUIV
2K X 8 ORGANIZATION
5 MA DESELECTED 40 MA SELECTED
150 NS ACCESS TIME OR BETTER

SPECIAL COMPONENTS:

82S100	FPLA	CUSTOM PROGRAMMED PART
16L2	PAL	CUSTOM PROGRAMMED PART
14L4	PAL	CUSTOM PROGRAMMED PART

FEATURES:

** OPERATION GUARANTEED AT 6 MHZ

** IEEE 696 (S-100) COMPATIBLE

** LOW POWER CONSUMPTION

** EXTENDED ADDRESSING

** BANK SELECT

** TWO INDEPENDENT 32K BANKS OF MEMORY

** 2K SEGMENT DISABLE

** PHANTOM

** MULTIPLE BANK CONTROL FEATURE

** PROM SUBSTITUTION FOR SPECIAL APPLICATIONS

** ENABLE/DISABLE AT POWER ON OR RESET

4. INSTALLATION PROCEDURES

4.1. ENABLES AND PHANTOM

4.1.1. ENABLE/DISABLE AT POWER ON CLEAR OR RESET

The MM65K16S memory board can be divided into two "banks" of memory that can be enabled or disabled when POWER ON CLEAR or RESET are in an active state. In order for all 64K of memory to be active on the bus both "Banks" of memory must be configured to enable in response to either POWER ON CLEAR or RESET.

An 8-pin header is located under IC 15D (74LS74) and is used to set the board so that either one or both of the banks of memory will be enabled or disabled whenever RESET or POWER ON CLEAR are active on the bus. This header is labeled **J6 7 5 4** and is configured by shunts that are placed across the row of pins.

The diagram below shows the jumper indications and the bank of memory that each jumper controls.

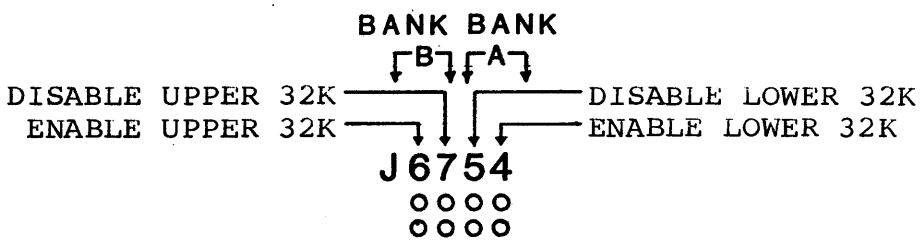
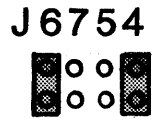


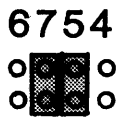
Figure 4-1: RESET AND POJ CONFIGURATION HEADER

The following examples indicate the four possible settings for the enable/disable feature.

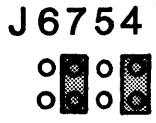
BOTH 32K BANKS ENABLED



BOTH 32K BANKS DISABLED



UPPER 32K DISABLED
LOWER 32K ENABLED



UPPER 32K ENABLED
LOWER 32K DISABLED

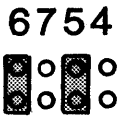


Figure 4-2: POJ AND RESET CONFIGURATIONS

CAUTION: DO NOT INSTALL SHUNT JUMPERS ACROSS (J4 AND J5) OR (J6 AND J7) AT THE SAME TIME, AS UNPREDICTABLE RESULTS COULD OCCUR.

4.1.2. PHANTOM

The PHANTOM option is used to remove a section or sections memory from the bus during specific operations. Some of these operations might include the enabling of a bootstrap loader, ROM monitor, or a POWER ON JUMP function.

Because there are two 32K banks of memory, it is necessary to configure the MM65K15S for proper operation with PHANTOM. Because both the upper and lower 32K banks of RAM individually respond to PHANTOM, it is mandatory that the MM65K16S be properly configured to recognize or ignore the PHANTOM signal.

The headers labeled **J1** and **J2** control PHANTOM. The J1 header is located directly below the DIP switch at 5D and controls PHANTOM for the upper 32K of memory. J2 is located directly below the IC in location 6D and controls the PHANTOM for the lower 32K of memory. As in the enable/disable circuitry, the mode is set by the use of shunts.

The following table shows the PHANTOM configuration header and the proper bank each jumper represents.

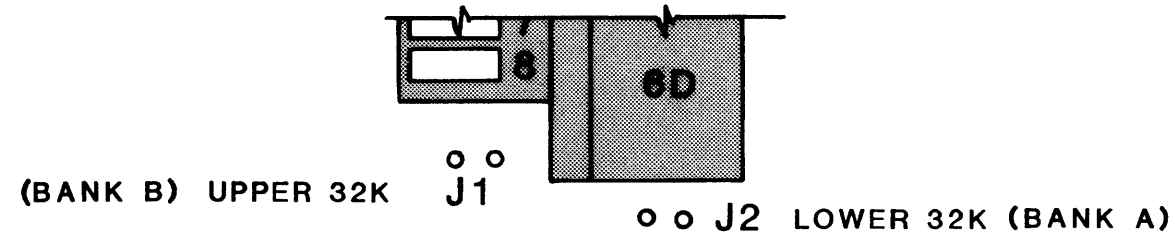


Figure 4-3: PHANTOM CONFIGURATION HEADERS

The following examples indicate the four possible ways that PHANTOM can be set for response.

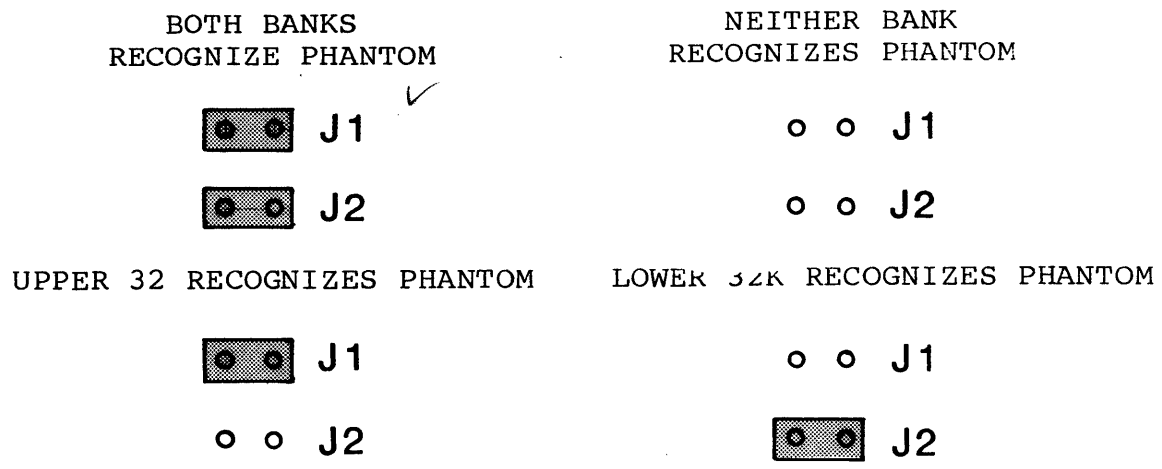


Figure 4-4: PHANTOM CONFIGURATIONS

4.2. MEMORY CONFIGURATION
4.2.1. MEMORY ADDRESSING

The Morrow Designs MM65K16S memory board is configured as four individual 16K blocks of memory. Each of these four blocks can be located on any 16K boundary. Thus, blocks of memory can be assigned at address 0000H, 4000H, 8000H, or C000H.

The DIP switch array located at 5D determines the addressing of the memory board. The DIP switch uses a binary counting system to determine which one of the four blocks will reside on a specific boundary in the memory map.

The table below shows memory addressing:

A15	A14	BLOCK #	ADDRESS FROM - TO	BANK
ON	ON	0	0000H - 3FFFH	A
ON	OFF	1	4000H - 7FFFH	
OFF	ON	2	8000H - BFFFH	B
OFF	OFF	3	C000H - FFFFH	

Table 4-1: MEMORY ADDRESSING TABLE

The table below shows the relationship between the switch settings on the DIP switch at location 5D and the assignment of the individual 16K blocks of memory.

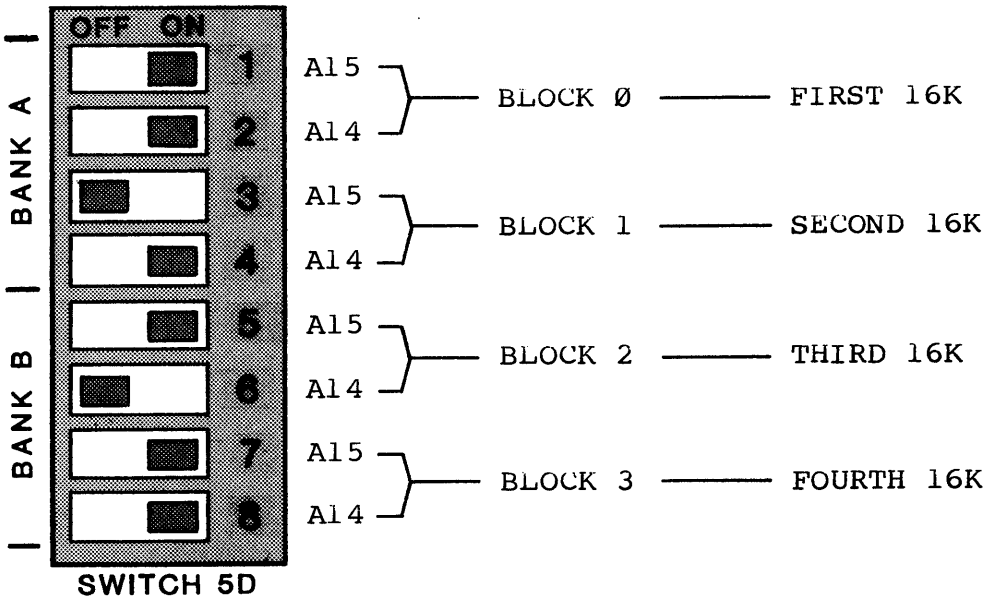


Figure 4-5: ASSIGNMENT OF INDIVIDUAL 16K BLOCKS OF MEMORY

The following examples will show the proper configuration for the memory board so that it will occupy a full 64K compliment.

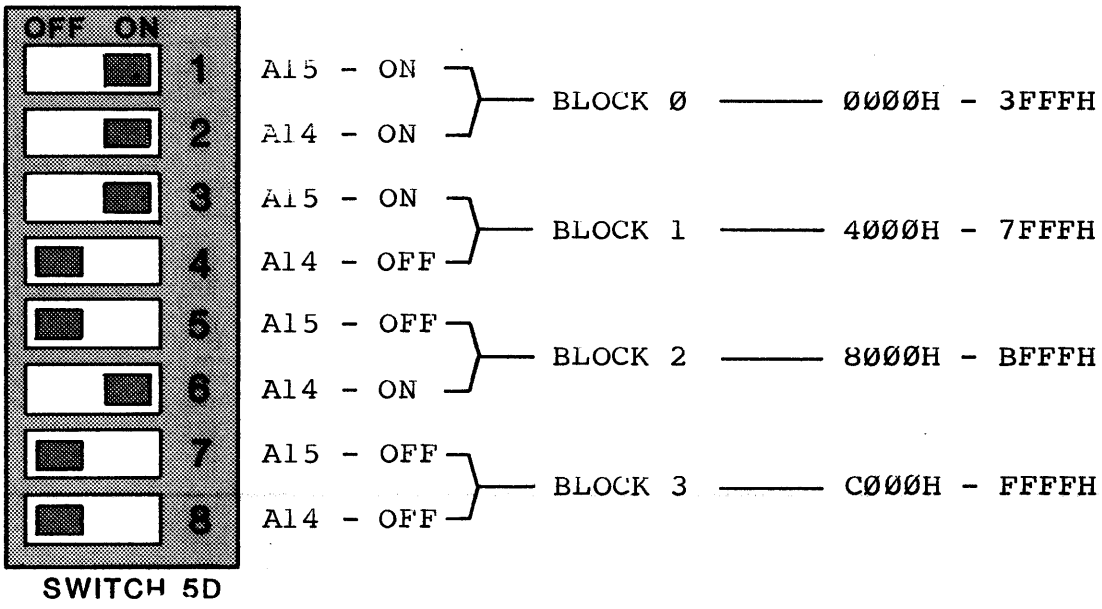


Figure 4-6: EXAMPLE OF STANDARD 64K CONFIGURATION

4.2.2. 2K SEGMENT DISABLE

The MM65K16S RAM board is capable of disabling a 2K segment of memory anywhere in the memory map. This feature is necessary in systems that might include a memory mapped disk controller or memory mapped video display interface.

The 2K disable feature is assigned to BLOCK Ø (paddle 1 and 2 on switch located at 5D. Because each 16K block can be addressed anywhere within the memory map, if a 2K hole is needed in the memory map were BLOCK 3 is normally addressed, simply reverse the addressing switches and locate BLOCK 3 where BLOCK Ø was addressed and re-address BLOCK Ø to reside where BLOCK 3 was addressed.

A 16-pin header (dual 8) is located between IC 2D and IC 3D and is used to select the 2K segment that is to be removed from the memory map. This header is labeled **PAGE Ø** at the top of the header and labeled **PAGE 7** at the bottom of the header. The PAGE number corresponds to the PAGE in memory that is to be disabled by the placement of a shunt across the header.

The table below shows all possible 2K segment disables:

PAGE	1C	BLOCK Ø	BLOCK 1	BLOCK 2	BLOCK 3
		ØØØØ-3FFF	4ØØØ-7FFF	8ØØØ-BFFF	CØØØ-FFFF
Ø	3A	ØØØØ-Ø7FF	4ØØØ-47FF	8ØØØ-87FF	CØØØ-C7FF
1	4A	Ø8ØØ-ØFFF	48ØØ-4FFF	88ØØ-8FFF	C8ØØ-CFFF
2	2B	1ØØØ-17FF	5ØØØ-F7FF	9ØØØ-97FF	DØØØ-D7FF
3	2C	18ØØ-1FFF	58ØØ-5FFF	98ØØ-9FFF	D8ØØ-DFFF
4	2A	2ØØØ-27FF	6ØØØ-67FF	AØØØ-A7FF	EØØØ-E7FF
5	1C	28ØØ-2FFF	68ØØ-6FFF	A8ØØ-AFFF	E8ØØ-EFFF
6	1B	3ØØØ-37FF	7ØØØ-77FF	BØØØ-B7FF	FØØØ-F7FF
7	1A	38ØØ-3FFF	78ØØ-7FFF	B8ØØ-BFFF	F8ØØ-FFFF

Table 4-2: 2K SEGMENT DISABLE TABLE

The table above is designed to provide a quick and accurate method of determining the proper location of a 2K segment. For example, if the shunt is placed across PAGE 5 and BLOCK Ø is addressed as BLOCK Ø, then memory disabled would be in the address range of 28ØØ to 2FFF. In the same manner if the shunt was placed across PAGE 7 and BLOCK Ø is addressed as BLOCK 3, then the 2K segment would be disabled from F8ØØ to FFFF.

The following example shows a 2K segment removed at F8ØØ to provide a hole for a memory mapped controller.

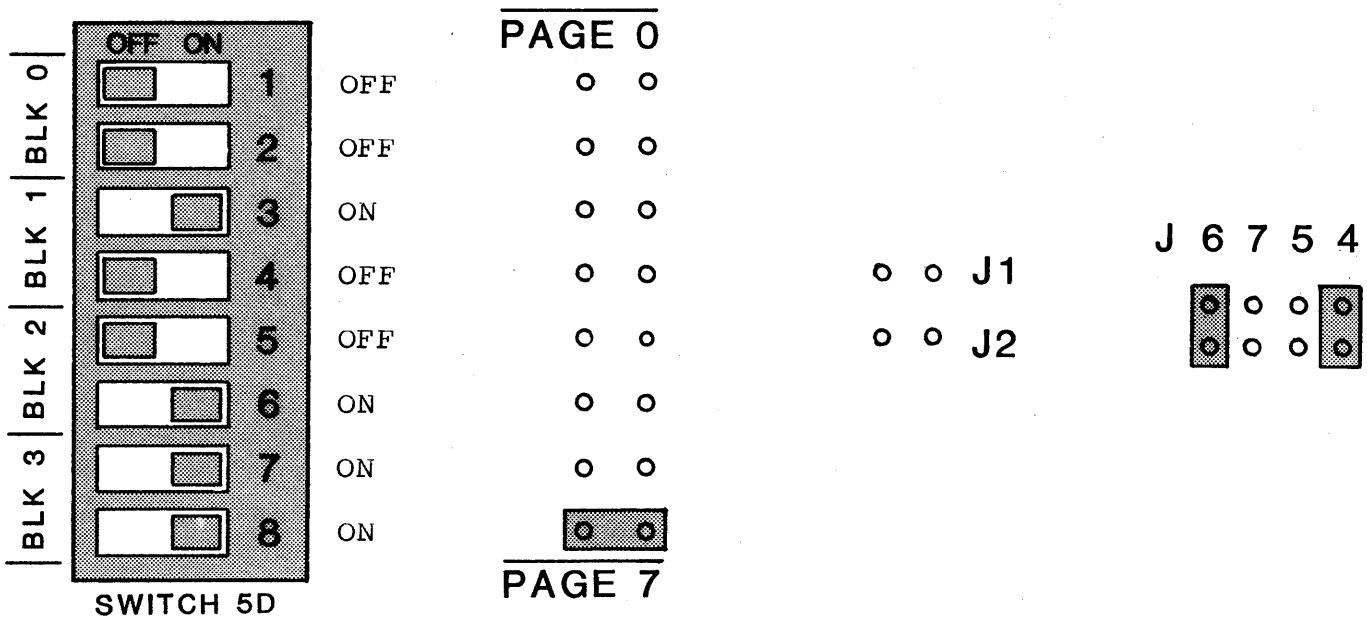


Figure 4-7: EXAMPLE OF 64K CONFIGURATION W/2K REMOVED AT F8ØØ

4.2.3. EXTENDED ADDRESSING

The Morrow Designs MM65K16S conforms to the latest IEEE S-100 standard, and can therefore recognize all 24 address lines that are available on the S-100 bus. Use of extended addressing does away with the 64K limitation imposed by most microcomputer systems.

In order for extended addressing to be enabled, location 1D must have a 25LS2521 IC installed. This IC, if not already in location 1D, will probably be found in location 2D (bank select) and should be removed from 2D and reinstalled in location 1D.

Adjacent to the DIP switch 1C is a header labeled **J3**. This header should NOT have a shunt placed across it unless the board is to be set up for bank select. If there is a shunt placed across J3, it should be removed for proper operation of extended addressing.

Once the 25LS2521 is installed at location 1D and the shunt has been removed from the header at location J3, extended addressing is now activated and bank select has been disabled.

The DIP switch that is located at 1C is used to set the extended addressing for the memory board. By setting the paddles to the OFF position the associated address line is then recognized when it is in its active state.

Extended addressing allows the MM65K16S RAM board to be addressed in 64K increments starting at address 000000H, 010000H, 020000H, up to FF0000H. The DIP switch that is located at 5D then addresses the 64K banks of memory within the extended addressing range. The example below shows the DIP switch at location 1C and its relationship with the incoming address lines.

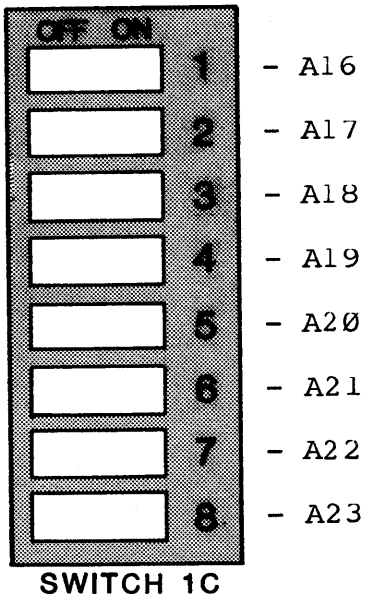


Figure 4-8: DIP SWITCH 1C USED WITH EXTENDED ADDRESSING

The following example indicates the proper switch settings for extended addressing. The board will be set for address Ø30000H.

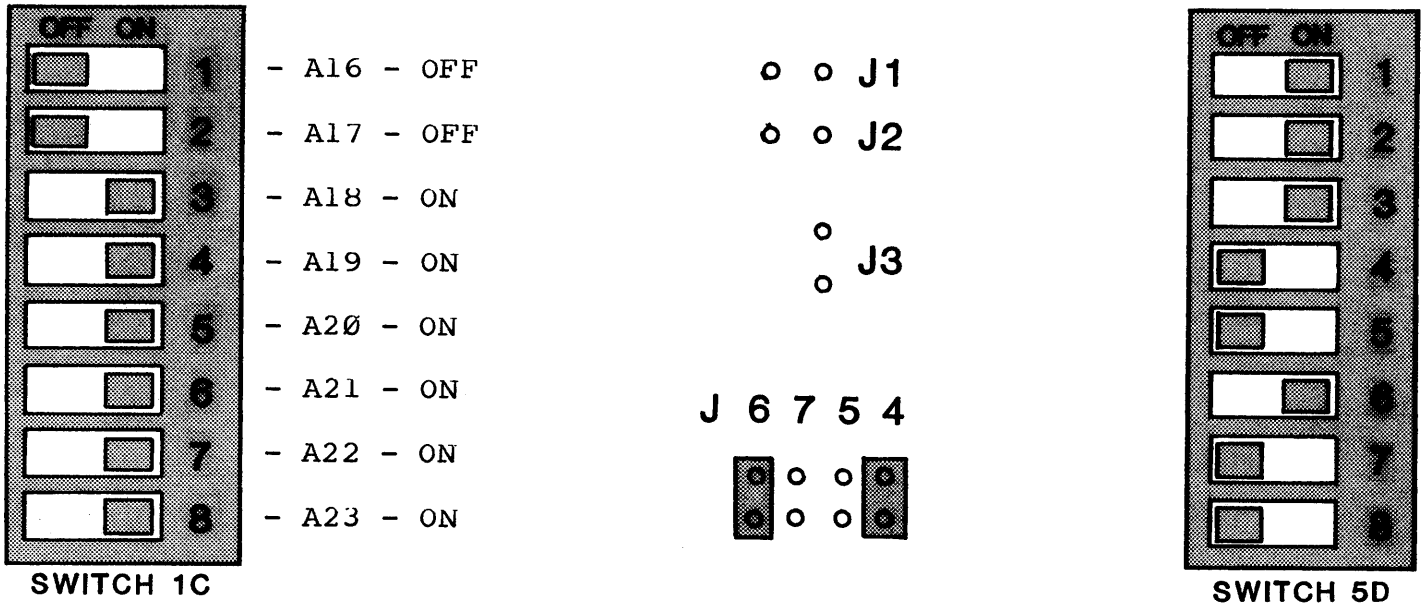


Figure 4-9: EXAMPLE OF EXTENDED ADDRESSING @ Ø30000H - Ø3FFFFH

4.2.4. BANK SELECT

For many existing systems designed before the implementation of the IEEE S-100 standard, the use of bank select was mandatory in order to expand memory beyond the 64K limitations. Using a DIP switch and shunt jumpers the MM65K16S RAM board is capable of being configured as any one of 256 I/O ports available, and can enable or disable itself using any one or a combination of the eight data bits available.

In order for bank select to function properly, there must be a 25LS2521 installed in location 2D. If the 25LS2521 is not installed in location 2D, then it will probably be found in location 1D (extended addressing). In any case, it must be installed in location 2D for bank select to function properly.

The next jumper to check is located adjacent to the DIP switch at location 1C on the board. This jumper is labeled **J3** and should have a shunt jumper across it. If there is no jumper across J3, one should be installed, otherwise bank select will not function properly.

The third and final check, is the setting of the data bit or bits that will enable or disable the individual banks of memory. There are two headers necessary for configuration. These two headers are located on the lower right hand corner of the board adjacent to IC 16D and are labeled **A Ø** and **Ø B** at the top of the header blocks and **A 7** and **7 B** at the bottom of the headers. Bits AØ through A7 control the lower 32K bank of memory and bits ØB through 7B control the upper 32K bank of memory.

It is important to remember that all switch settings in the bank select configuration are set to the software that is being used. If the operating system does bank select at port 40H, then the MM65K16S RAM board must be configured to run at port 40H also. The following diagram shows the address lines in relation to the DIP switch at location IC.

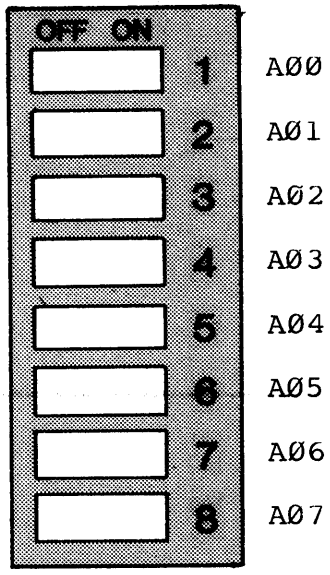


Figure 4-10: DIP SWITCH 1C USED WITH BANK SELECT

In the following diagram the memory board will be configured for port 40H in the bank select mode and data bit-0 will be used to enable both banks of memory.

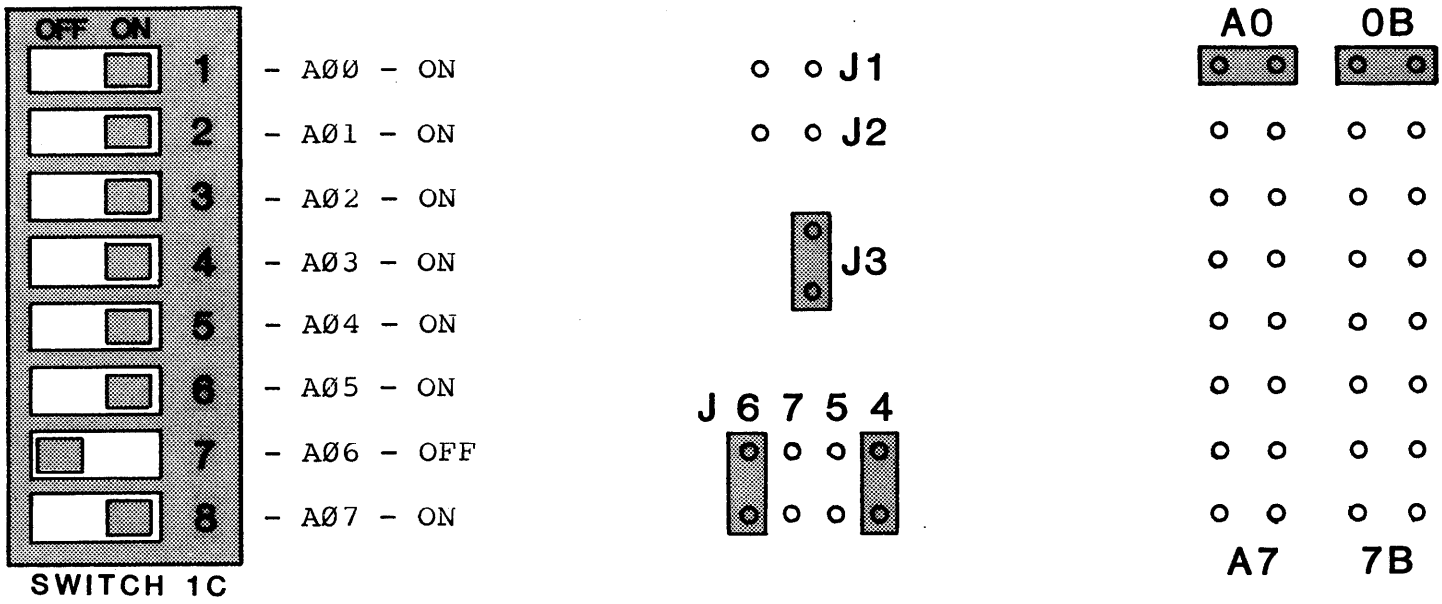


Figure 4-11: EXAMPLE OF BOARD SETUP FOR BANK SELECT

5. SPECIAL APPLICATION NOTES

The purpose of this section is to describe some of the problems that could arise when using the board for applications where special types of configurations are necessary. This section will also describe some of the unique features of the MM65K16S memory board.

5.1. USING PROMS

When using a programmed 2716 EPROM or equivalent PROM, it is necessary to remember that the MM65K16S memory board **DOES NOT** generate any type of wait states for the processor. Therefore, it is mandatory that the PROMS being used are fast enough. If a 4 Mhz processor is being used, then the PROM must have an access time for 300 ns or faster. Using a slower PROM is almost a certain guarantee of problems.

5.2. DISABLING BLOCKS OF MEMORY

The Morrow Designs MM65K16S disables in 32K banks. Therefore, if it is necessary to disable smaller portions of memory, the board can not be used except by depopulation of the board. If the board is to be depopulated for any reason, that bank of RAM must have the PHANTOM enabled. Failure to activate PHANTOM will cause problems because, even though the memory chips were removed from their sockets, they are still active on the bus.

5.3. 32K/48K MAPPING

When the memory is purchased as a 32K board, it is set up as one 32K bank that utilizes BLOCK Ø and BLOCK 1 of the memory board. If the board is purchased as a 48K board, then BLOCKS Ø,1, and 2 will be stuffed and BLOCK 3 will be left unstuffed. If the user decides that two 16K blocks of memory are necessary the tables below will indicate which RAM chip is to be installed into what location on the board for any specific block of memory.

BLOCK Ø

1A, 1B, 1C, 2A, 2B, 2C, 3A, 4A

BLOCK 1

3B, 3C, 4B, 4C, 5A, 5B, 5C, 6A

BLOCK 2

6B, 7A, 7B, 7C, 8A, 8B, 8C, 9A

BLOCK 3

9B, 9C, 10A,10B, 10C, 11A, 11B, 11C

Table 5-1: 32/48K MAPPING TABLE

5.4. MULTIPLE BANK CONTROL FEATURE

One of the more interesting features of the MM65K16S is the manner in which the bank select feature operates. The MM65K16S allows for a total of eight independent users, but by using multiple data bits, one bank of memory can be "forced" to follow other banks of memory, or one board could control multiple banks of memory.

The example below is an example of how the multiple bank feature functions. The data bits for AØ to A7 are set up to represent a data pattern of 83H. Data bits ØB to B7 are set up to represent a data pattern of Ø3H.

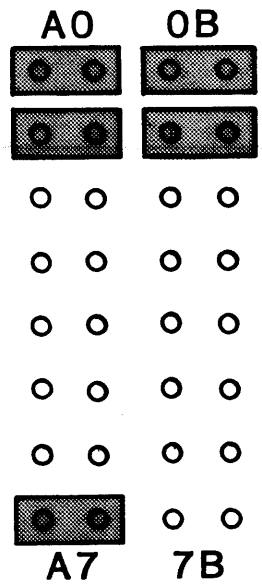


Figure 5-1: EXAMPLE OF MULTIPLE BANK CONTROL

In the above example, data bits Ø and 1 were enabled on both the upper and lower banks of memory. The lower bank of memory had data bit-7 set also, and this should be noted.

Whenever the system software issues a bank select command and the data that is sent to the board is equal to the strapping of the data bits, the board will then enable or disable.

The upper bank of memory will respond to data that is equal to Ø3H (bits Ø and 1), but it will also respond to **ANY** data pattern that has data bits Ø and 1 set. In other words, this Bank will respond to data patterns of Ø3H, Ø7H, 83H, 13H, 4BH, 6FH etc. With this in mind, it is possible for the system software to issue one bank select command and control multiple banks of memory.

The lower bank of memory, (remember data bit-Ø7 was set) is set to recognize a data pattern of 83H, but will respond to any data

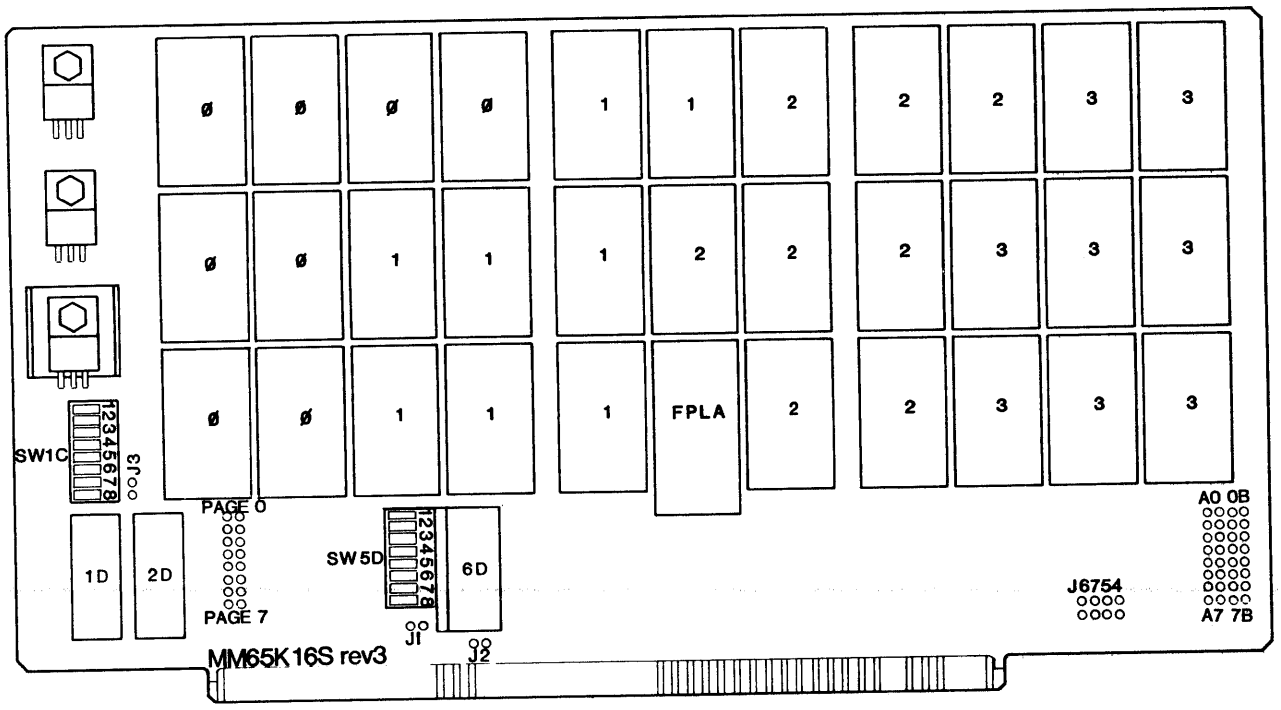
that has bits Ø,1, and 7 set. So, the lower bank of memory could be set to enable or disable when the system software issues a bank select command and the data patterns are 93H, A3H, F3H, or B7H. Therefore, this bank responds to the system commands in the same fashion as the upper bank responded.

5.5. INTERFACING WITH NON IEEE STANDARD SYSTEMS

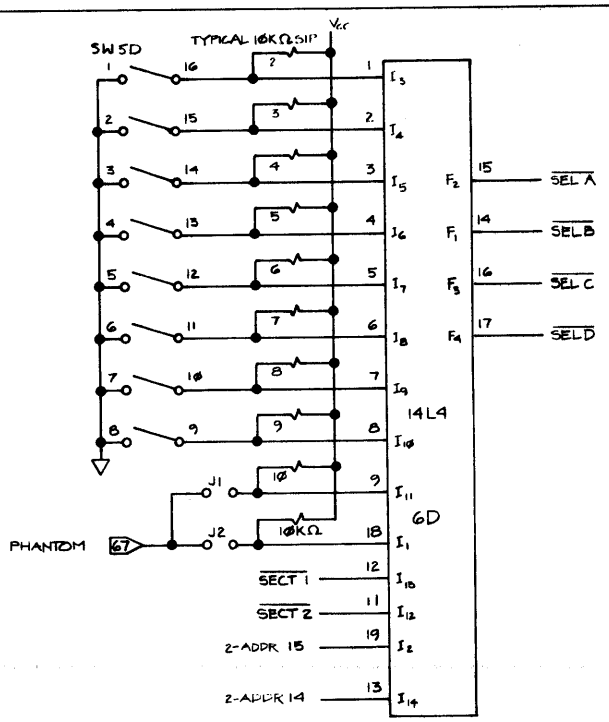
The Morrow Designs MM65K16S is an IEEE standard board, therefore all control lines must be present on the bus in order for the RAM to function correctly. Some manufacturers do not use the signal SWO (pin-97) which the MM65K16S requires to operate correctly. In the event of any difficulty, contact the factory immediately.

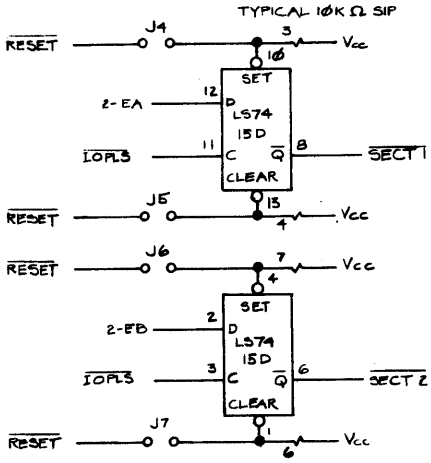
6. SUBJECT INDEX

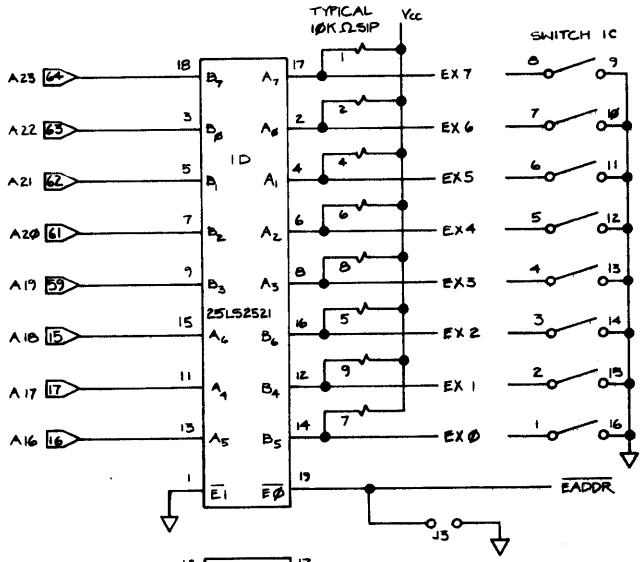
COMPONENT LAYOUT/SCHEMATIC

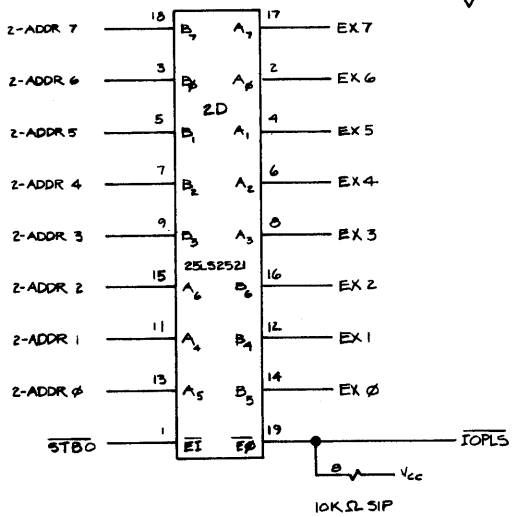


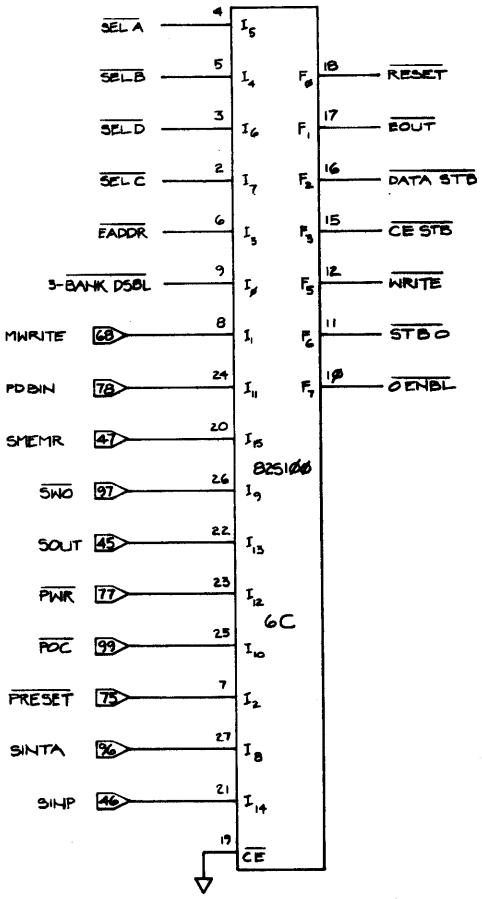
MM65K Memory Board Component Layout











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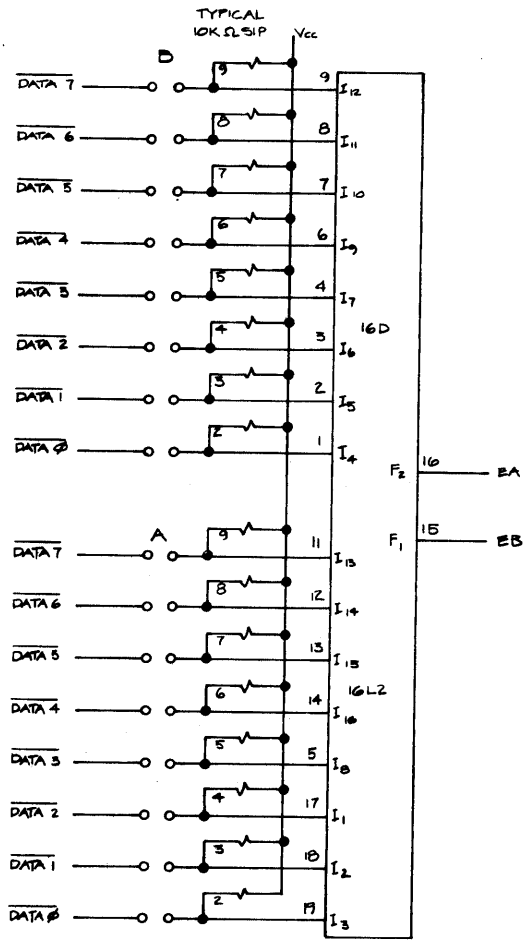
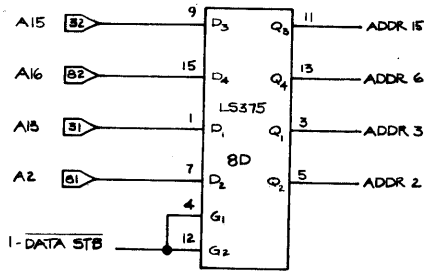
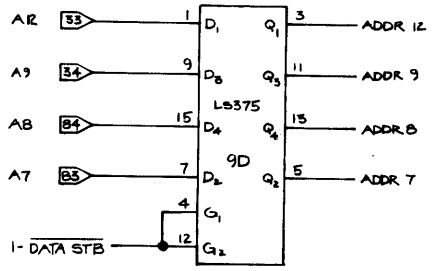
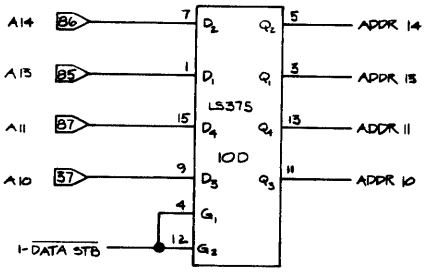
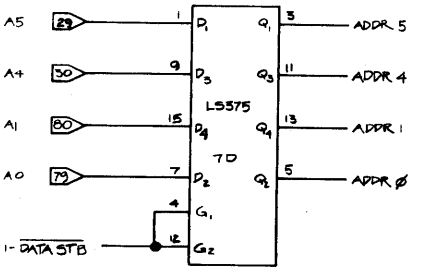
BOARD SELECT LOGIC

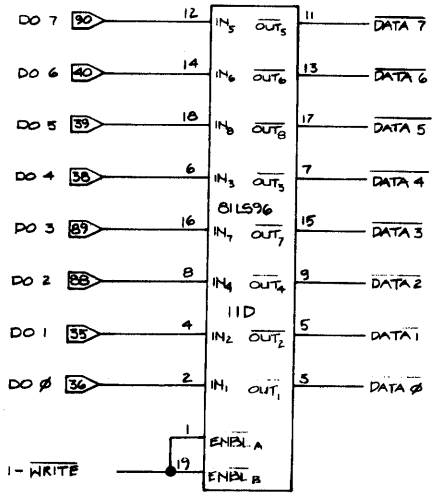


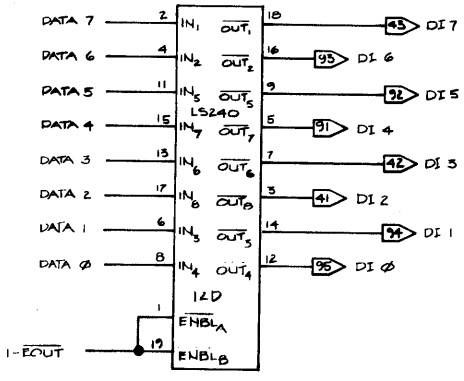












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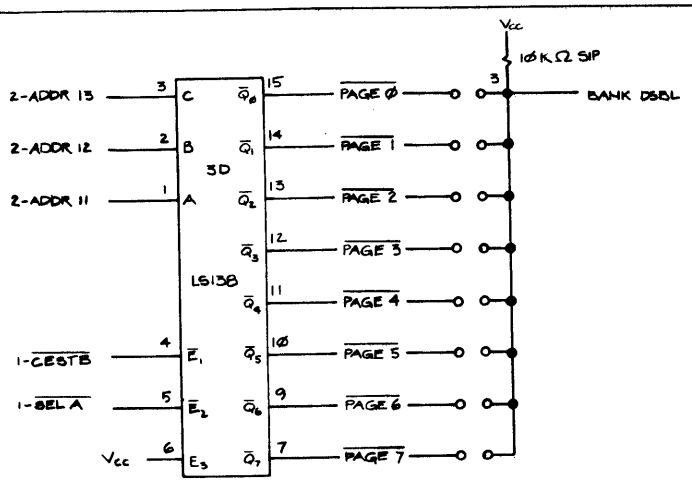
DATA AND ADDRESS BUFFERS



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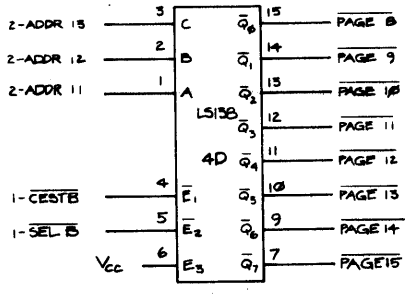
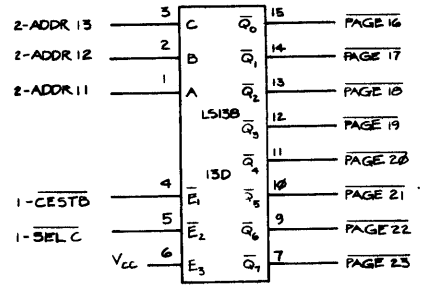
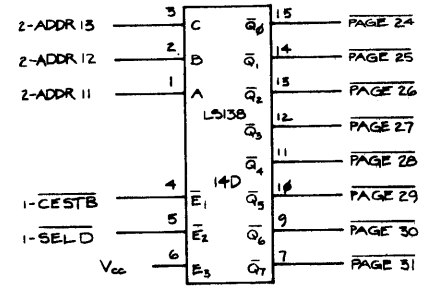
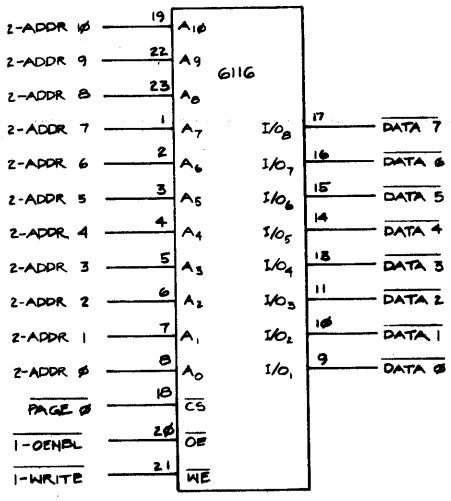
PAGE 1 - 4A
PAGE 2 - 2B
PAGE 3 - 2C
PAGE 4 - 2A
PAGE 5 - 1C
PAGE 6 - 1B
PAGE 7 - 1A
PAGE 8 - 4B
PAGE 9 - 5B
PAGE 10 - 4C
PAGE 11 - 5C
PAGE 12 - 3C
PAGE 13 - 6A
PAGE 14 - 3B
PAGE 15 - 5A
PAGE 16 - 7A
PAGE 17 - 8A
PAGE 18 - 9A
PAGE 19 - 6B
PAGE 20 - 8B
PAGE 21 - 7B
PAGE 22 - 7C
PAGE 23 - 8C
PAGE 24 - 11A
PAGE 25 - 11B
PAGE 26 - 11C
PAGE 27 - 10C
PAGE 28 - 10B
PAGE 29 - 10A
PAGE 30 - 9C
PAGE 31 - 9B

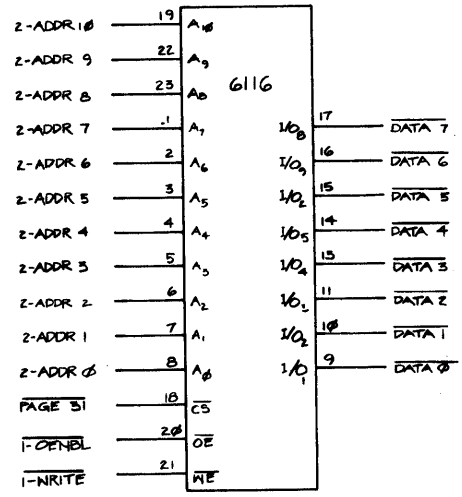
PHYSICAL LAYOUT OF LOGICAL MEMORY PAGES











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DEVICE SELECT LOGIC & MEMORY ARRAY