# A Computer-Integrated Rapid-Access Magnetic Tape System with Fixed Address

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THIS paper describes the internal tape library system planned for the *TX-2* computer at Lincoln Laboratory, Massachusetts Institute of Technology (MIT). One hundred magnetic tape transports will be under the control of a central electronic system; the system will have a storage capacity of $10^{10}$ bits and an access time of about 30 seconds. It is particularly well suited for use with a computer of large random-access storage capacity such as *TX-2*, which has a core memory of $2^1/_2$ million bits. A simple tape transport having a high-speed search mode with redundant information transfer will make the ultimate library system for a computer, reliable and relatively inexpensive.

The tape transports are controlled by electronic circuits closely integrated with the computer. A permanent, constant-density timing track on the tape provides the speed reference for the control circuits and makes possible fixed position address-

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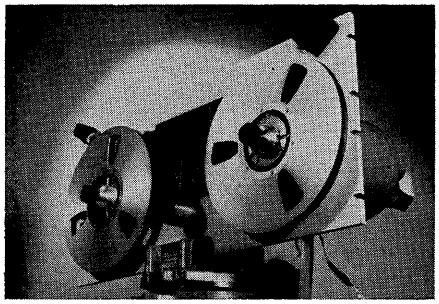

**Fig. 1. Tape transport mechanism**

ing and a variable rate of information transfer. The transport does not employ a constant speed capstan: two conventional 3-phase motors pull the tape in either direction. The control system varies the speed by modifying the torque on the driving motors after comparing the timing track bit rate with the desired bit rate. By this means the computer can select an appropriate speed for recording data in real time over prolonged periods. A separate channel of block marks enables the computer to locate information blocks at any speed, including high-speed search at 920 inches per second (ips). Read and write speeds are 30 to 100 ips and acceleration time to these speeds is 1/2 to $1^1/_2$ seconds.

High reliability in the transfer of information to and from the tape is gained by making five channels out of ten redundantly paired tracks. Thus in the ten-track head assembly there are three information channels, one timing channel, and one block mark channel. Appropriate head shielding reduces crosstalk and permits reading of the timing channel when other channels are being used for writing. Since the amplitude of the signal from the tape varies greatly with speed, a system of recording is used that allows the polarity of the flux change, rather than its amplitude, to be sensed in reading. High-gain amplifiers may then be used in which the output stages are normally saturated and the gain need not be closely controlled.

## Computer/Tape Library Relationship

The primary objective, a large library of quickly accessible information, is provided by a large number of tape transport mechanisms controlled by a small number of circuits which are closely integrated with the computer. One feature of *TX-2*[1,2] is its multiple sequence control; that is, it can share its attention between equipments which are operating simultaneously in real time. The computer commands the selected tape drive to attain some mode of operation, then turns its attention elsewhere until the tape control tells the computer that the desired mode has been attained. Multiple sequence control also enables the computer to vary the speed of the tape during information transfer: this feature would be used, for example, if the computation itself depended upon external, real-time events and the information transfer had to be synchronized with the results of the computation.

Another feature of *TX-2* is its large, random-access core memory[3] which can store large blocks of information at one time and which can be used as a buffer while the tape is accelerating. The control element for the tape library accepts the computer's commands rapidly but does not require instant response by the computer to events in the tape system. Generally the control takes care of the simple local problems and leaves the complex problems of operation to the computer, and therefore the programmer.

The tape mechanism, which has a wide variety of speeds, can search through a reel of tape much faster than the computer can accept information. For this reason, blocks of information on the tape are tagged with block marks that can be read at speeds up to the maximum, 920 ips. The read and write instructions command only a single 9-bit transfer between memory and tape. A series of such instructions is necessary to transfer large blocks of information; the instructions must occur at an average rate determined by the tape's speed.

## Transport Design and Motion Control

### Mechanical Design

The tape transports used in this system were made as simple and fool-proof as possible: they consist of a read-write head assembly, two reels, two drive motors, and a tape guide. The drive mechanism has no capstan. Thus a good deal of mechanical complexity is eliminated and a wide range of tape speeds is made possible. Fast starts and stops are precluded, however: 1/2 second and $7^1/_2$ inches of tape are required to reach 30 ips.

Figs. 1 and 2 show the transport mechanism. The motors are flange mounted, 1,800 rpm, 3-phase induction motors of the conventional type which have roughly constant torque characteristics when operating well below synchronous speed. The horsepower (hp) rating, and therefore the torque, is as high as possible, limited by the tensile strength of the tape. One-eighth-hp motors, each driven by a magnetic amplifier, provide the proper torque to operate 10-inch reels mounted directly on the motor shaft and loaded with polyester tape, 0.001-inch thick and 1/2-inch wide. Maximum tape speed is about 920 ips when the driving reel is full.

The head assembly and guide are shown in the insert, Fig. 2. The relatively large, constant radius of the guide reduces the pressure between tape and guide: At speeds above 20 ips the tape floats on an air cushion and is thus easy to edge guide. Skew, caused by nonuniform tape tension across the width of the tape and by variations in tape width

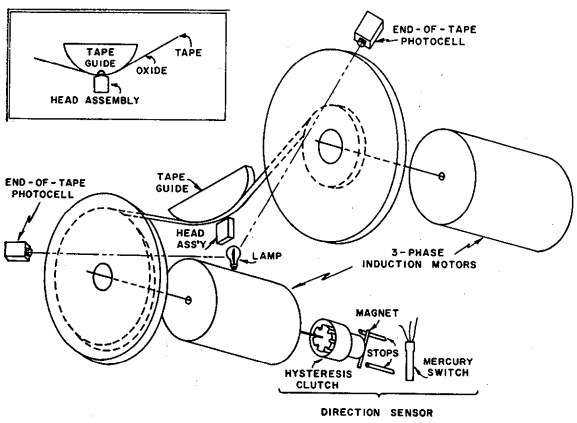


**Fig. 2 (left). Tape transport mechanism**

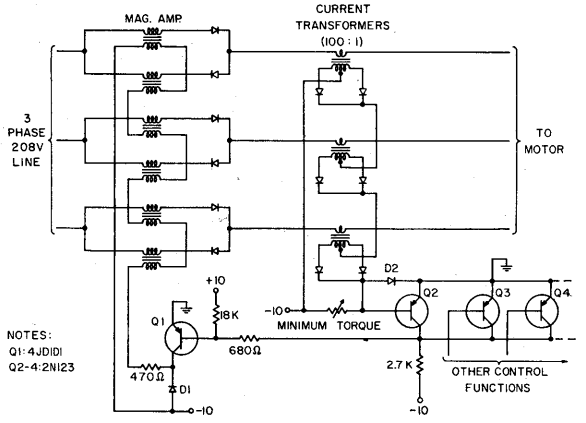


**Fig. 3 (right). Motor control**

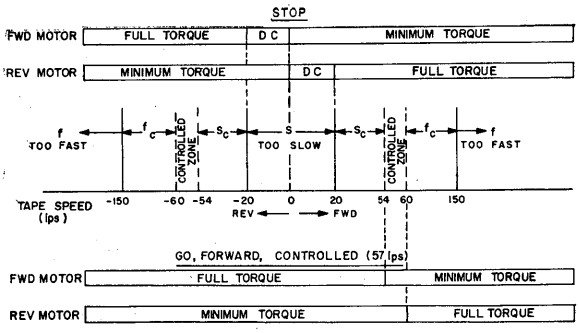


**Fig. 4 (left). Motor torque versus tape speed for several command states**

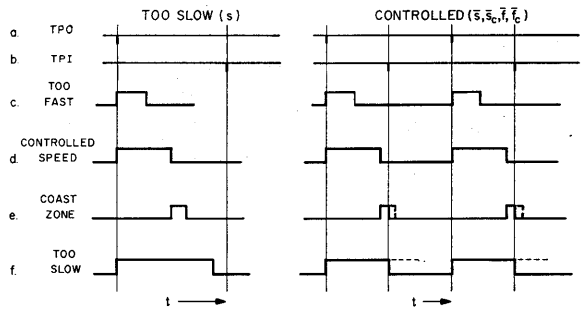


**Fig. 6 (right). Speed - sensing waveforms**

is minimized. There is no wrap around the head. Variations in tape tension, which are large in this transport, do not, therefore, cause excessive pressures on the head and wear is reduced. Because only short wave lengths (0.0025 and 0.005 inch) are used in the system, the area of tape-head contact need not be large.

The direction in which the transport is moving is determined by a sensing device mounted on the rear shaft extension of one motor. The sensor consists of an iron cup dragged against one of a pair of stops by hysteresis from a star-shaped permanent magnet on the motor shaft. The cup operates a mercury switch by rotating an attached magnet. This scheme gives positive direction information even at the slowest tape speed. A mercury wetted contact switch provides computer-level signals to the control without contact bounce and with good reliability.

## Motion Control

Each motor can generate torque in only one direction to pull the tape from one reel to the other. The control of the motors is therefore simpler than if torque had to be reversed. Since tension is limited by tape strength, acceleration is relatively slow. A sudden change of torque, which might allow a loop to form, is prevented by a long time constant in the control windings of the motor magnetic amplifier.

To stop the tape, full torque is first applied by the trailing motor until the tape speed falls below 20 ips: at that point d-c is applied to the trailing motor to bring the tape to a smooth stop. The direction sensor indicates which motor is trailing. With d-c in the motor field winding the rotor will resist applied torque even at zero velocity due to the hysteresis in the rotor. Voltage is never completely removed from either motor in order that some tape tension always be maintained. The end of the tape is sensed by a photoelectric cell which receives light through transparent leaders at each end of the tape. The timing track is continued on the edges of the 100-foot transparent strips so that the control element will know when the tape has fallen below 20 ips as previously described.

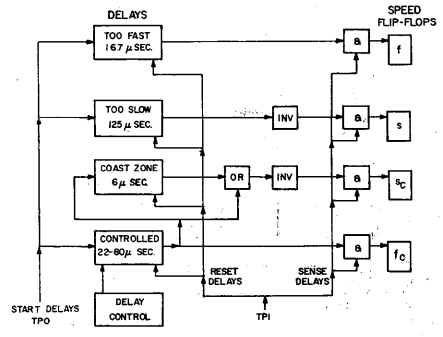


**Fig. 5. Speed-sensing logic**

The control circuit for one of the motors is shown in Fig. 3. The transistor, $Q$-1, regulates the current through the control windings of the 3-phase magnetic amplifier, and it switches between saturation and cutoff at various duty cycles. When $Q$-1 is cut off, $D$-1 conducts, so that the control winding-time constant is determined solely by its own inductance and the 470-ohm resistor. This time constant is made long enough to prevent abrupt torque changes and to average the control current.

Feedback was included to provide close control of minimum torque. Too much minimum torque will either allow the tape to creep or require excessive d-c holding currents in the trailing motor. Too little torque will fail to overcome static friction, and allow a loop of tape to form. The feedback prevents large variations in the output current of the magnetic amplifier which would be caused by unbalanced line voltage or small variations in reactor control current, especially when the amplifiers are nearly cut off. The feedback signal is derived from the sum of currents in all three motor leads. The diode $D$-2 limits the sum output voltage of the current transformers to 10 volts and thus keeps the voltage drop across their primaries negligible under high current conditions. To generate full torque, one of the other transistors such as $Q$-3 is saturated, cutting off the magnetic amplifier control current independent of the feedback and allowing full current to flow to the motor.

The direct current which is applied to the trailing motor when the transport is slowing to a stop is switched to one lead of the motor by a relay contact (not shown on Fig. 3). The d-c flows into that motor lead and out the other two, back through the magnetic amplifiers. Although the magnetic amplifiers are biased into a low torque condition they will pass the d-c (approximately 1 ampere) since the average voltage across any one reactor must be zero.

## Digital Speed Control

To determine which motor should receive full torque, minimum torque, or d-c, the desired condition of the transport is compared with the existing one. As shown in Fig. 4, the motion control is based on a group of speed domains: too fast ($f$), faster than controlled ($f_c$), slower than controlled ($s_c$), and too slow ($s$). Various torque commands are shown as a function of speed and direction for several desired conditions.

The speed sensing logic is diagrammed in Fig. 5. The speed is detected by comparing the interval between timing pulses from the tape with the delays of delay units, as shown in Fig. 6. Two pulses are generated from a tape timing channel as it travels over the head, Fig. 6(A) and (B). The first is used to fire three delay units, two of which, Fig. 6(C) and (F), establish the boundaries between the area of usable speeds and too fast or too slow. The third delay unit, Fig. 6(D), can be set by the computer to any one of several delay times representing speeds in the useful range and provides close speed control at preset and selectable tape speeds. It in turn drives a fourth delay unit, Fig. 6(E), to provide a controlled zone. In this condition the transport coasts. The second timing pulse occurs at a time determined by the speed of the tape. It is used to sense the condition of

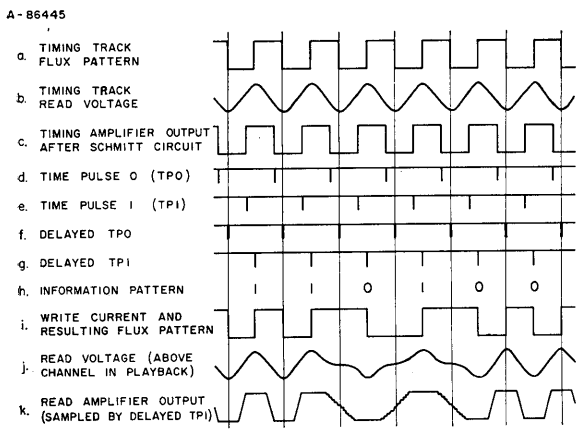


**Fig. 7 (left). Phase-modulated nonreturn-to-zero waveforms**

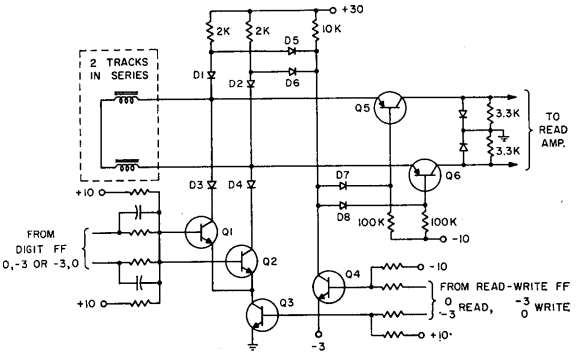


**Fig. 8. Read-write switch and write circuit**

the delay units and to set flip-flops to define the speed domain. It is also used to reset the units so they have time to recover before the next "set" pulse. The dotted waveforms in Fig. 6(E) and (F) indicate this resetting when the tape is in the controlled-speed zone. The delay units must be resettable, and the delay time of one must be capable of electronic variation.

## Head Assembly and Read-Write Method

### Head Assembly Design

The 10-track head assembly contains five channels: three information, one timing, and one block mark. Each channel consists of two redundantly paired tracks; the tracks in each pair are nonadjacent to minimize the effect of a speck of dirt lifting a portion of the tape. The timing channel occupies the two outside tracks which are heavily shielded from the interior ones in order that the timing channel may be read while the others are being written.

The timing channel controls tape speed, information density, and the fixed address feature. It assures constant information density regardless of tape speed and makes possible the changing of a single word in a message. Its density must therefore be known and constant. It is permanently recorded, either with a constant-speed capstan temporarily attached or on a separate constant-speed machine.

### Read and Write Principles

Since the amplitude of the signal from the tape varies greatly with speed, a system of recording is used that allows the polarity of the flux change to be significant rather than its amplitude. High-gain amplifiers may then be used in which the gain need not be constant. Fig. 7 shows the flux pattern and other waveforms. The idealized timing-track flux pattern consists of 200 complete cycles of flux per inch, or 400-flux reversals per inch, see Fig. 7(A). The timing track read voltage, Fig. 7(B), is the expected derivative waveform from a 0.0005-inch gap looking at a signal of this density. The signal is amplified and squared in a Schmitt circuit, Fig. 7(C); the finite hysteresis of the Schmitt circuit delays the signal slightly as shown. Time pulses are generated from the transitions of the Schmitt circuit; time pulse 0 (TP0) from the negative transitions and time pulse 1 (TP1) from the positive transitions, 7(D) and 7(E). The time pulses must then be slightly delayed, 7(F) and 7(G), so that the information flux pattern may be written in phase with the timing flux pattern. The delay is a function of tape speed and is varied by an analog voltage fed to the delay circuit. The analog voltage is in turn derived from a circuit whose output is a predetermined function of the average frequency of the time pulses fed to it. The flux is laid on the tape in phase with the timing flux so that information may be read or written while the tape is moving in either direction.

The delayed time pulses control the transfer of information to the writing flip-flops. Delayed TP0 transfers the bit to be written to the flip-flop which is controlling write current; delayed TP1 complements the flip-flop. Thus a flux change is written in the center of each line corresponding to the bit to be written; there may or may not be flux changes between the lines. A typical information pattern and resulting ideal flux pattern are shown in Fig. 7(H) and 7(I). The voltage which would be read from this channel during read time is shown in Fig. 7(J). Notice that there is a saturation signal at the center of each line, whereas, in between lines there is sometimes a signal and sometimes not. The signal is then amplified more than necessary, Fig. 7(K). The amplifier has enough gain so that one of the redundant tracks may be completely separated from the head by a speck of dirt while a half-amplitude signal is being received from the other track; a saturation signal will still be delivered by the amplifier at the center of the line. The amplifier is strobed by delayed TP1, so that the logic doesn't know what the amplifier output looks like at any other time. The saturation output received at the center of each line with phase-modulated nonreturn-to-zero recording also allows the tape to be read correctly with plenty of amplifier gain margin over a wide range of tape speeds.

### Read and Write Circuits

The read-write switch and write circuit for one digit are shown in Fig. 8. During "write," $Q4$ is cut off and $Q3$ is saturated. With $Q4$ cut off, its $10K$ collector resistor lifts the bases of $Q5$ and $Q6$ towards $+30$, leaving them cut off and the read amplifier disconnected. The silicon diodes at the amplifier input prevent any large voltage excursions from reaching the amplifier. With $Q3$ saturated, the digit flip-flop will cause either $Q1$ or $Q2$ to also be saturated. With the circuit values shown, 15 milliamperes (ma) will flow through the two series-connected tracks and 30 ma through the saturated transistor ($Q1$ or $Q2$). The direction of current flow through the tracks is determined by the flip-flop state; i.e., whether $Q1$ or $Q2$ is saturated.

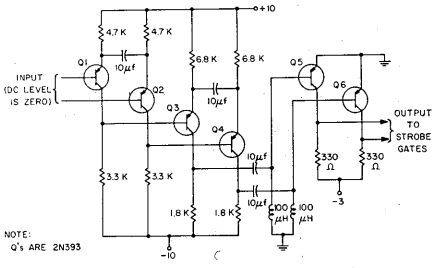


**Fig. 9. Read amplifier**

During "read," $Q3$ is cut off and $Q4$ is saturated. $Q4$ takes the full write current through diodes $D5$ and $D6$, back biasing diodes $D1$ through $D4$. With $Q4$ saturated diodes $D7$ and $D8$ are back biased, allowing $Q5$ and $Q6$ to be saturated, thus connecting the two series-connected tracks to the read amplifier at a d-c level of approximately zero.

### Read Amplifier

The read amplifier, Fig. 9, has two difference-amplifier stages and one output stage with more than enough gain to give a saturation output signal at a tape speed of 20 ips. In the first two stages, the common mode gain per stage is less than unity while the difference signal gain is approximately beta. The low common mode gain insures that power supply noise will not be amplified. Each transistor ($Q1$-$Q4$) is biased to a constant d-c operating point of approximately 3.8-smitter-collector volts and 1.9-ma collector current. The capacitors shown must only be large enough to have negligible signal attenuation at 20 ips, the lowest tape speed of interest. The lowest frequency signal will be at 20 ips and 100 cycles per inch [alternate ones and zeros; see Fig. 7(J)] for a frequency of 2 kc. The highest frequency will be at 920 ips and 200 cycles per inch (all ones or all zeros) for a frequency of 184 kc. The micro-alloy *2N393* transistors have more than enough bandwidth for this application. The signal amplitude at the input to $Q5$ and $Q6$ is large enough so that, most of the time, one of these transistors is saturated. The output signals are of a computer-type amplitude (0 or $-3$) and are sampled by TP1 using conventional *TX-2* logical circuits.[4]

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