LINEAR TECHNOLOGY

1995 Linear Databook Volume IV

Data Conversion
References
Amplifiers
Power Products
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Interface

LINEAR TECHNOLOGY

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QUICK REFERENCE INDEX

Note: All products in **BOLD** are in this Databook, others appear in LTC's 1990, 1992 and 1994 Databooks ('90DB = LTC's 1990 Databook, '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook). Quick Reference Index continued on inside back pages.

"FROM YOUR MIND TO YOUR MARKET... AND EVERYTHING IN BETWEEN"

This is Volume IV of LTC's four volume series of databooks. This issue contains device data sheets and applications circuits for the products introduced since Volume III was printed in June of 1994.

Extraordinary growth in the high performance linear market has continued to drive the design efforts for these products. The result is increased complexity, higher efficiency, lower power and more cost-effective solutions. Included within the four book set are high performance products targeted to suit diverse applications within the Industrial, Test and Measurement, Telecom, Computer, Automotive and Military market segments.

In this edition, you will find a significant number of new products such as; A-to-D and D-to-A Converters, Multiplexers, High Performance Voltage References, High Speed Amplifiers, Ultralow Power Comparators, Low Power Advanced Interface Circuits for RS232 through V.35 protocols, Infrared Receivers, High Frequency Switching Regulators, Fast Response Linear Regulators, PCMCIA devices and other advanced Power Control products.

For a complete set of information consult Volume I (1990), Volume II (1992), Volume III (1994) and this issue, Volume IV.

The Table of Contents and alphanumeric index in this volume provide guides to locate each LTC product within the four volume set. Use this guide to find the correct page in the appropriate volume.

LTC offers the latest in high performance wafer processing including bipolar, LTCMOS, micropower, high speed, complementary bipolar and BiCMOS technologies. These processes are used in two wafer fabrication facilities located in Milpitas, California with a third facility under construction in Camas, Washington at the time this data book went to print. A new assembly plant is located in Penang, Malaysia and our new Far East Headquarters is located in Singapore. The wafer fabrication and test facilities are certified to ISO 9001 by TÜV Rheinland and certified by DESC for JAN B and JAN S level microcircuits. These certifications are part of LTC's Quality and Reliability program in support of military/aerospace and radiation hardened requirements.

LTC appreciates your continued support and remains dedicated to providing the highest quality products, applications assistance and manufacturing knowledge to service your high performance analog requirements.

Linear Technology Corporation

1995 Linear Databook Volume IV

Note: *The 1995 Linear Databook is the fourth volume in our series of databooks to date totaling approximately 5800 pages of product and applications information for approximately 3000 individual products, presented in a four volume set of databooks. The 1990 Linear Databook is Volume I; the 1992 Linear Databook Supplement when reprinted will become Volume II. The 1994 Linear Databook Volume III Table of Contents references device types included in Volumes 1-3. Volume 4 Table of Contents references data in Volumes 1-4.*

LIFE SUPPORT POLICY

LINEAR'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF LINEAR TECHNOLOGY CORPORATION. As used herein:

a. *Life support devices or systems are devices or systems which (1) are intended for surgical implant into the body, or (2) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user.*

b. *A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.*

Information furnished herein by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits, as described herein, will not infringe on existing patent rights.

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1995 Linear Databook Volume IV

SECTION 1—GENERAL INFORMATION

SECTION 2—AMPLIFIERS

Note: All products in **BOLD** are in this Databook, others appear in LTC's 1990, 1992 and 1994 Databooks ('90DB = LTC's 1990 Databook, '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook).

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SECTION 1—GENERAL INFORMATION

SECTION 1—GENERAL INFORMATION

I. ORDER ENTRY

Orders for products contained herein should be directed to: LINEAR TECHNOLOGY CORPORATION, 1630 McCarthy Boulevard, Milpitas, California 95035. Phone: 408-432-1900.

II. ORDERING INFORMATION

Minimum order value is $2000.00 per order; minimum value per line item is $1000.00.

Each item must be ordered using the complete part number exactly as listed on the data sheet.

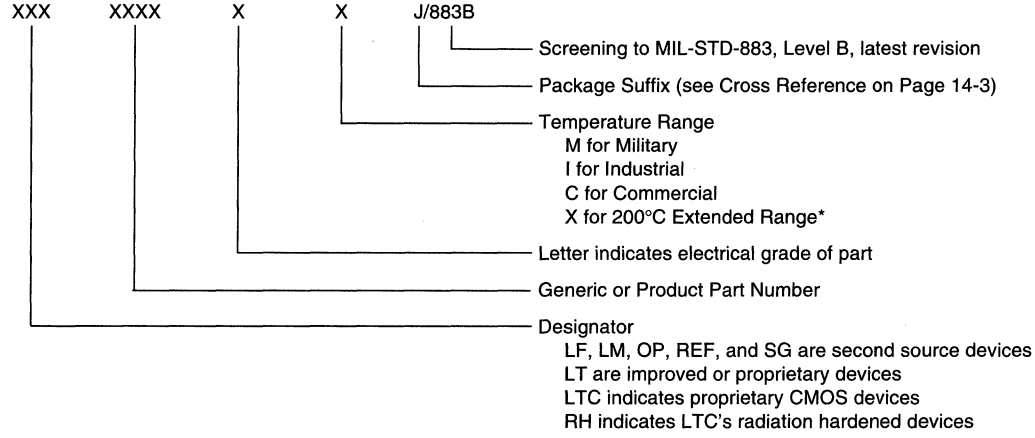
F.O.B.: Milpitas, California.

III. RELIABILITY PROGRAMS

Linear Technology Corporation currently offers the following Reliability Programs:

A. JAN QPL devices.
B. DESC drawings.
C. MIL-STD-883, Level B, latest revision for all military temperature range devices.
D. "R-Flow" Burn-In Program for commercial temperature range devices. Consult Factory regarding burn-in program.
E. Radiation Hardened (RH) products.

IV. PART NUMBER EXPLANATION



V. PACKAGE SUFFIX EXPLANATION

SUFFIX DESIGNATOR	GENERIC PACKAGE	PACKAGE DESCRIPTION
D8	SIDE BRAZED	8-Lead Side Brazed Package (Hermetic)
D	SIDE BRAZED	14-, 16-, 18- and 20-Lead Side Brazed Package (Hermetic)
F	TSSOP	20-Lead TSSOP, Thin Shrink Small Outline Plastic Package (0.173) *Notes 6, 7, 8*
G	SSOP	16-, 20-, 24- and 28-Lead SSOP, Shrink Small Outline Plastic Package (0.209) *Notes 5, 6, 7, 8*
GN	SSOP	16-, 20- and 24-Lead SSOP, Narrow Body, Shrink Small Outline Plastic Package (0.150) *Notes 5, 6, 7, 8*
GW	SSOP	36- and 44-Lead SSOP, Wide Body, Shrink Small Outline Plastic Package (0.300) *Notes 5, 6, 7, 8*
H	"H" is used for Multiple Styles of Metal Cans, as follows:	
	METAL CAN	8- or 10-Lead TO-5 Metal Can Package
	METAL CAN	3- or 4-Lead TO-39 Metal Can Package
	METAL CAN	2-, 3- or 4-Lead TO-46 Metal Can Standard Package or in Thermal Caps
	METAL CAN	3-Lead TO-52 Metal Can Package

GENERAL ORDERING INFORMATION

SUFFIX DESIGNATOR	GENERIC PACKAGE	PACKAGE DESCRIPTION
J8	CERDIP	8-Lead CERDIP, Narrow Body, Dual-In-Line Ceramic Package (0.150 Hermetic)
J	CERDIP	14-, 16-, 18-, 20- and 24-Lead CERDIP, Narrow Body, Dual-In-Line Ceramic Package (0.300 Hermetic)
JW	CERDIP	28-Lead CERDIP, Wide Body, Dual-In-Line Ceramic Package (0.600 Hermetic)
K	TO-3	3-Lead TO-3, Transistor Outline Metal Can Package
L	LCC	20-Pin LCC, Rectangular Shaped, Leadless Chip Carrier Package (Hermetic)
LS	LCC	20-Pin LCC, Square Shaped, Leadless Chip Carrier Package (Hermetic)
M	DD Pak	3-Lead DD Pak, Plastic Package *Notes 6, 7, 8*
N8	PDIP	8-Lead PDIP, Narrow Body, Dual-In-Line Plastic Package (0.300) *Notes 6, 7, 8*
N	PDIP	14-, 16-, 18-, 20- and 24-Lead PDIP, Narrow Body, Dual-In-Line Plastic Package (0.300) *Notes 6, 7, 8*
NW	PDIP	28-Lead PDIP, Wide Body, Dual-In-Line Plastic Package (0.600) *Notes 6, 7, 8*
P	TO-3P	3-Lead TO-3P, Transistor Outline Plastic Package (Similar to a TO-247) *Notes 6, 7, 8*
Q	DD Pak	5-Lead DD Pak, Plastic Package *Notes 6, 7, 8*
R	DD Pak	7-Lead DD Pak, Plastic Package *Notes 6, 7, 8*
S8	SO	8-Lead SO, Narrow Body, Small Outline Plastic Package (0.150) *Notes 3, 6, 7, 8*
S	SO	14- and 16-Lead SO, Narrow Body, Small Outline Plastic Package (0.150) *Notes 1, 2, 6, 7, 8*
SW	SO	16-, 18-, 20-, 24-, and 28-Lead SO, Wide Body, Small Outline Plastic Package (0.300) *Notes 1, 2, 6, 7, 8*
ST	SOT-223	3-Lead SOT-223, Small Outline Transistor Plastic Package *Notes 6, 7, 8*
T	TO-220	3- or 5-Lead TO-220, Transistor Outline Plastic Package *Notes 4, 6, 7, 8*
T7	TO-220	7-Lead TO-220, Transistor Outline Plastic Package (Formerly "Y" Pkg.) *Notes 4, 6, 7, 8*
W	FLATPAK	10-Lead FLATPAK, Glass Sealed Package (Hermetic)
WB	FLATPAK	10- or 14-Lead FLATPAK, Metal Sealed, Bottom Brazed Package (Hermetic)
Z	TO-92	3-Lead TO-92, Transistor Outline Plastic Package *Notes 6, 7, 8*

(All Dimensions Shown in Inches)

Note 1: 16-Lead SO (Small Outline) package is delivered in either narrow (0.150) or wide body (0.300) package styles depending on the device die size. See specific data sheet for pin counts and package dimensions.

Note 2: 18-, 20-, 24- and 28-Lead SO (Small Outline) packages are wide body styles (0.300).

Note 3: Pinout and electrical specifications on S8 (8-Lead Small Outline) package may differ from a standard commercial grade N8 package. See SO (Small Outline) data sheets for specific information.

Note 4: SPECIAL FLOW Lead Form Configurations (trimmed and/or formed) are available for TO-220 packages. See "TO-220 Lead Bend Options" in the back of Section 14 or consult Factory for details.

Note 5: SSOP Shrink Small Outline Packages vary in lead pitch. G = 0.0256, GN = 0.0250, GW = 0.03150.

Note 6: **FLAMMABILITY RATING**: All plastic packages supplied by LTC have obtained Underwriters Laboratories' Flame Retardancy Certification Rating of UL94V-0.

Note 7: **TOXIC MATERIALS**: Molding compounds used by our assembly subcontractors do not contain toxic materials known as; Polybrominated Biphenyls (PBB), Polybrominated Biphenyl Ether (PBBE) or Polybrominated Biphenyl Oxide (PBBO).

Note 8: **OXYGEN INDEX:** All plastic packages supplied by LTC have an oxygen index of 28% minimum.

P/N	LTC DIRECT REPL
AD101A	LM101A
AD232	LT1081*
AD235	LT1130A**
AD237	LT1138A**
AD238	LT1139A**
AD239	LT1137A**
AD241	LT1137A**
AD381	LT1022**
AD510	LT1001*
AD517	LT1001**
AD518	LM118**
	LT118A**
AD524	LT1101**
AD536	LT1088**
AD580	LT580
AD581	LT581
	LT1031**
AD586	LT1027*
AD589	LT1034**
AD636	LT1088**
AD637	LT1088**
AD642	LT1057**
AD647	LT1057**
AD704	LT1114*
AD705	LT1097
AD706	LT1112*
AD707	LT1097
AD711	LT1056**
AD712	LT1057**
AD713	LT1058**
AD736	LT1088**
AD737	LT1088**
AD743	LT1113*
AD744	LT1122
AD790	LT1016**
AD810	LT1252**
AD811	LT1252**
AD813	LT1260**
AD817	LT1360*
AD818	LT1363
AD821	LT1006**
AD822	LT1169*
AD824	LT1014**
AD826	LT1361*
AD827	LT1229**
AD828	LT1364*
AD840	LT1222**
AD841	LT1220**
AD842	LT1221**
AD844	LT1223**
AD845	LT1122
AD846	LT1223**
AD847	LT1360
AD848	LT1192**
AD849	LT1226
	LT1192
AD1671	LTC1410**
AD7306	LT1318**
AD7541	LTC7541A*
AD7541A	LTC7541A*
AD7543	LTC7543*
AD7572	LTC1272**
AD7579	LTC1091**
AD7580	LTC1092**
AD7820	LTC1099*
AD7821	LTC1096/
	LTC1098**
AD7870	LTC1275**
AD7875	LTC1273**
AD7876	LTC1276**
AD7883	LTC1282**
AD7890	LTC1290**
AD7892-1,2	LTC1278-5**

P/N	LTC DIRECT REPL
AD7892-3	LTC1279**
AD8300	LTC1453**
AD9617	LT1223
AD9618	LT1223
AD9686	LT1016**
ADC0820	LTC1099*
ADC0832	LTC1098*
ADC08061	LTC1198**
ADC08231	LTC1196
ADC1031	LTC1091**
ADC1034	LTC1093**
ADC1038	LTC1094**
ADC12062	LTC1410**
ADG201A	LTC201A
ADG202	LTC202
ADG221	LTC221
ADG222	LTC222
ADS7800	LTC1276**
ADS7803	LTC1293**
ADS7804	LTC1272-8**
ADS7810	LTC1410**
ADS7819	LTC1410**
BT8920	LTC1279**
CLC406	LT1227**
CLC414	LT1252
CLC415	LT1230
CLC430	LT1227**
CLC520	LT1228**
CLC532	LT1203**
CMP01	LT1011**
CMP02	LT1011**
DAC8043	LTC8043*
DAC8143	LTC8143*
DAC8512	LTC1451**
DG201A	LTC201
DG202	LTC202
DG508-X	LTC1390**
DS1232	LTC1232
DS14C335	LT1331**
DS3695	LTC485*
EL1224	LT1229*
EL2020	LT1223*
EL2028	LT1220
EL2029	LT1221
EL2030	LT1223
EL2038	LT1222
EL2039	LT1222
EL2040	LT1222
EL2041	LT1220
EL2044	LT1252**
EL2045	LT1363*
EL2082	LT1228**
EL2090	LT1228**
EL2099	LT1206**
EL2120	LT1191**
	LT1223**
	LT1227**
EL2130	LT1227**
EL2210	LT1361*
EL2211	LT1364*
EL2224	LT1229**
	LT1208**
EL2232	LT1229**
EL2242	LT1229**
	LT1358*
EL2244	LT1361*
EL2245	LT1364*
EL2260	LT1229
EL2410	LT1362*
EL2411	LT1365*
EL2444	LT1362
EL2445	LT1254**
EL2460	LT1230
EL4089	LT1228**

P/N	LTC DIRECT REPL
EL4393	LT1260**
EL4441	LT1204**
EL4094/5	LT1256**
GT4123	LT1256**
GY4102	LT1203**
GX4314	LT1205**
HA2500	LT1220
HA2502	LT1220
HA2505	LT1220
HA2510	LT118A**
	LM118**
HA2512	LT118A**
	LM118A**
HA2515	LT318A**
	LM318**
HA2520	LT1220
HA2541	LT1220
HA2544	LT1224
HA5004	LT1223
HA5130-2	OP07A
	LT1001AM*
HA5130-5	OP07E
	LT1001C*
HA5135-2	OP07
	LT1001M*
HA5135-5	OP07C
	LT1001C*
HAOP07	OP07
	LT1001M*
HAOP07A	OP07A
	LT1001AM*
HAOP07C	OP07C
	LT1001C*
HAOP07E	OP07E
	LT1001C*
HI508-X	LTC1390**
HI5810	LTC1272-8
ICL232	LT1081
ICL7650	LTC1050*
	LTC1052**
ICL7652	LTC7652
	LTC1052*
ICL7660	LTC1044*
	LTC1054**
ICL7662	LTC1144*
ICL8069C	LM385-1.2
	LT1004C-1.2*
ICL8069M	LM185-1.2
	LT1004M-1.2*
ISO150	LTC1145**
LF400	LT1122DC
	LT1122CC
LF400A	LT1122BC
	LT1122AC
LH0002	LT1010M**
LH0044	LT1001M*
LH0070	LH0070
	LT1031M*
LH2108	LH2108
LH2108A	LH2108A
LM10	LM10
LM10B	LM10B
LM10C	LM10C
LM399	LM399
LM399A	LM399A
LM399A-20	LM399A-20
LM399A-50	LM399A-50
LM2574	LT1176
LM2575	LT1076**
LM2575N	LT1176
LM2576	LT1074**
LM2577	LT1071**
LM2587	LT1170
LM2935	LT1005**

P/N	LTC DIRECT REPL
LM2940	LT1086**
LM6181	LT1227**
LM6218	LT1203**
LM6361	LT1195**
LP2950-5	LT1117-5**
LP2951	LT1121**
µA96172	LTC486
µA96174	LTC487
µA96176	LTC485
MAX120	LT1278-5**
MAX122	LTC1276**
MAX153	LTC1198**
MAX162	LTC1273*
MAX163	LTC1273*
MAX164	LTC1275*
MAX165	LTC1198**
MAX167	LTC1275**
MAX172	LTC1272*
MAX202	LT1381*
MAX207	LT1138A**
MAX211	LTC1337**
MAX212	LTC1348**
MAX213	LTC1349**
MAX220	LT1281A**
MAX222	LT1280A*
MAX223	LT1237
MAX232A	LT1281A*
MAX235A	LT1130A**
MAX237A	LT1138A**
MAX238A	LT1139A**
MAX239A	LT1137A**
MAX241A	LT1136A**
	LT1137A**
MAX242	LTC1384*
MAX280	LTC1062
MAX281	LTC1065**
MAX400	LT1001
MAX420	LTC1150*
MAX422	LTC1150**
MAX430	LTC1150
MAX432	LTC1150**
MAX441	LT1204**
MAX442	LT1205**
MAX454	LT1204**
MAX467	LT1260**
MAX478	LT1178
MAX479	LT1179
MAX480	LT1077*
MAX481	LTC1481
MAX485	LTC485
MAX487	LTC1487*
MAX492	LT1366**
MAX538	LTC1452
MAX539	LTC1452
MAX543	LTC8043*
MAX560	LT1331**
MAX561	LTC1327**
MAX563	LTC1386*
MAX603	LT1129-5**
MAX604	LT1129-3.3**
MAX613	LT1313**
	LT1315**
MAX614	LT1312**
	LT1314**
MAX630	LT1173**
MAX631	LT1173-5**
MAX632	LT1173-12**
MAX633	LT1173**
MAX634	LT1173**
MAX635	LT1173-5**
MAX636	LT1173-12**
MAX637	LT1173**
MAX638	LT1173-5**
MAX639	LTC1174*

*__LTC Improved Replacement:__ 100% Pin-for-pin compatible with better electrical specifications.
**__Similar Device:__ Please consult the data sheet to determine the suitability of the replacement for specific applications.

P/N	LTC DIRECT REPL
MAX640	LTC1174-3.3
MAX641	LT1173-5**
MAX642	LT1173-12**
MAX643	LTC1147
MAX649	LTC1147-5**
MAX651	LTC1147-3.3**
MAX652	LTC1147**
MAX654	LT1073-5
MAX655	LT1173-5**
MAX656	LT1073-5**
MAX657	LT1073**
MAX658	LT1108-5**
MAX659	LT1108-5**
MAX660	LTC660
MAX662	LTC1262*
MAX667	LT1129**
MAX680	LT1026
MAX690	LTC690
MAX691	LTC691
MAX692	LTC692*
MAX693	LTC693*
MAX694	LTC694
MAX695	LTC695
MAX699	LTC699
MAX724	LT1074
MAX726	LT1076
MAX741D	LTC1147**
MAX741U	LTC1266**
MAX756	LT1304**
MAX757	LT1304**
MAX761	LT1309**
MAX786	LTC1267**
MAX850	LTC1550**
MAX851	LTC1551**
MAX852	LTC1550/51**
MAX853	LTC1550**
MAX856	LT1303**
MAX873	LT1019-2.5
MAX875	LT1019-5
	LT1021-5
	LT1027
MAX876	LT1019-10
	LT1021-10
MAX882	LT1521-3.3**
MAX883	LT1521-5**
MAX884	LT1521-3.3**
MAX1044	LTC1044A
MAX1232	LTC1232
MAX1649	LTC1147-5**
MAX1651	LTC1147-3.3**
MAX1771	LT1170/71**
MAX9686	LT1016
MC78T05	LM323T
	LT323AT*
MC1400AU2	LT1019CN8-2.5**
MC1400AU5	LT1019CN8-5**
MC1400AU10	LT1019CN8-10**
MC1400U2	LT1019CN8-2.5*
MC1400U5	LT1019CN8-5*
MC1400U10	LT1019CN8-10*
MC1558	LT1013M*
MC3486	LTC488*
MC3487	LTC487*
MC145406	LT1039-16*
MC34166	LT1074
MF5	LTC1059*
MF10	LTC1060
	LTC1060*
MIC2557	LT1312**
MIC2558	LT1313**
MIC2560	LTC1472**
ML4861	LT1073**
	LT1110**
ML4864	LT1182**
	LT1183**
ML4876	LT1182**
	LT1183**
MX7541	LTC7541A*
MX7541A	LTC7541A*
MX7572	LTC1272*
MX7820	LTC1099*
OPA177	LT1001A
	LT1097
OPA404	LT1216**
OPA603	LT1252
OPA620	LT1227**
OPA1013	LT1013
	LT1211
OPA2107	LT1169**
OPA2111	LT1169**
OPA2604	LT1124**
OP42	LT1122*
OP77	LT1001
	LT1097*
OP97	LT1012
	LT1097*
OP177	LT1001
OP207	LT1002
OP215	OP215
	LT1057
OP220	LT1078*
OP221	LT1013*
OP227	OP227
OP270	OP270
	LT1124*
OP290	LT1078**
OP291	LT1366**
OP297	LT1112*
OP400	LT1014*
	LT1114*
OP420	LT1079*
OP421	LT1014*
OP467	LT1359*
OP470	OP470
	LT1125*
OP490	LT1079**
OP497	LT1114*
PM1008	LT1008
PM1012	LT1012
PM1558	LT1013M*
PM2108	LH2108
PM2108A	LH2108A
REF01	REF01
	LT1019-10*
	LT1021-10**
REF02	REF02
	LT1019-5*
	LT1021-5**
REF03	LT1019-2.5*
REF43	LT1019A-2.5*
REF101	LT1019-10
	LT1021-10
REF102	LT1019-10
	LT1021-10
REF192	LT1019-2.5**
REF195	LT1236**
REG1117	LT1117-2.85
SG1524	SG1524
	LT1524*
SG1525A	SG1525A
	LT1525A*
SG1527A	SG1527A
	LT1527A*
Si9706	LTC1470**
Si9707	LTC1471**
Si9710	LT1313**
	LTC1315**
	LTC1472**
Si9711	LTC1314**
	LTC1315**
	LTC1472**
SI9712	LTC1472**
SN75172	LTC486*
SN75173	LTC488**
SN75174	LTC487*
SN57175	LTC489**
SN75176	LTC485*
SN75179B	LTC490*
SN75ALS/80	LTC491*
SN75186	LT1134**
SP301	LTC1321*
SP302	LTC1322*
TL431A	LT1431*
LT1431A	LT1431
TLC2543	LTC1296
TPS2010	LTC1477**
TPS2011	LTC1477**
TPS2012	LTC1477**
TPS2013	LTC1477**
TSC04	LT1004-1.2
TSC05	LT1004-2.5
TSC170	LT3846**
TSC171	LT3847**
TSC232	LT1080**
	LT1081**
TSC911	LTC1050*
TSC913	LT1078**
	LTC1051*
TSC914	LT1079**
	LTC1053*
TSC918	LTC7652**
TSC962	LTC1046**
TSC7650	LTC1050*
TSC7652	LTC7652
	LTC1052
TSC7660	LTC1044*
TSC9491	LT1004-1.2
TSC9495	REF02
	LT1019M-5
	LT1021-5**
TSC9496	REF01
	LT1021-10**
UC117	LM117
	LT117A*
UC137	LM137
	LT137A*
	LT1033M**
UC150	LM150
	LT150A*
UC317	LM317
	LT317A*
UC337	LM337
	LT337A*
	LT1033C**
UC350	LM350
	LT350A*
UC1524	SG1524
	LT1524*
UC1525A	SG1525A
	LT1525A*
UC1527A	SG1527A
	LT1527A*
UC1846	LT1846
UC1847	LT1847
XRT3588/89	LTC1345**

***LTC Improved Replacement:** 100% Pin-for-pin compatible with better electrical specifications.
****Similar Device:** Please consult the data sheet to determine the suitability of the replacement for specific applications.

SECTION 2—AMPLIFIERS

SECTION 2—AMPLIFIERS

OP AMPS

Precision

Dual Supply

Low V_{OS}

Zero Drift

LTC1047 (D, 10µV)
LTC1049 (S, 10µV)
LTC1050 (S, 5µV)
LTC1051 (D, 5µV)
LTC1052 (S, 5µV)
LTC1053 (Q, 5µV)
LTC1150 (S, 5µV)
LTC1151 (D, 5µV)
LTC1152 (S, 10µV)
LTC1250 (S, 10µV)

Bipolar

LT1001 (S, 25µV)
LT1002 (D, 60µV)
LT1006 (S, 50µV)
LT1007 (S, 25µV)
LT1008 (S, 120µV)
LT1012 (S, 25µV)
LT1024 (D, 50µV)
LT1028 (S, 40µV)
LT1077 (S, 40µV)
LT1078 (S, 40µV)
LT1079 (Q, 70µV)
LT1097 (S, 50µV)
LT1112 (D, 60µV)
LT1114 (Q, 60µV)
LT1124 (D, 70µV)
LT1125 (Q, 100µV)
LT1413 (D, 60µV)

Low I_B

Zero Drift

LTC1047 (D, 50pA)
LTC1049 (S, 50pA)
LTC1050 (S, 30pA)
LTC1051 (D, 50pA)
LTC1052 (S, 30pA)
LTC1053 (Q, 50pA)
LTC1150 (S, 100pA)
LTC1151 (D, 100pA)
LTC1152 (S, 100pA)

Bipolar

LT1008 (S, 100pA)
LT1012 (S, 100pA)
LT1022 (S, 50pA)
LT1024 (D, 120pA)
LT1055 (S, 50pA)
LT1056 (S, 50pA)
LT1057 (D, 50pA)
LT1058 (Q, 50pA)
LT1097 (S, 250pA)
LT1112 (D, 180pA)
LT1113 (D, 320pA)
LT1114 (Q, 180pA)
LT1122 (S, 75pA)
LT1169 (S, 20pA)
LT1457 (D, 75pA)

Low Noise

LT1007 (S, 3.8nV/√Hz)
LT1028 (S, 1.1nV/√Hz)
LT1037 (S, 3.8nV/√Hz)
LT1113 (D, 6nV/√Hz)
LT1115 (S, 1.1nV/√Hz)
LT1124 (D, 4.2nV/√Hz)
LT1125 (Q, 4.2nV/√Hz)
LT1126 (D, 4.2nV/√Hz)
LT1127 (Q, 4.2nV/√Hz)
LT1128 (S, 1.1nV/√Hz)

Large A_{VOL}

LT1006 (S, 1M)
LT1007 (S, 7M)
LT1012 (S, 300k)
LT1013 (D, 1.5M)
LT1014 (Q, 1.5M)
LT1028 (S, 7M)
LT1037 (S, 7M)
LT1049 (S, 3M)
LT1050 (S, 3M)
LT1051 (D, 1M)
LT1052 (S, 3M)
LT1053 (Q, 1M)
LT1077 (S, 1M)
LT1078 (D, 1M)
LT1079 (Q, 1M)
LT1097 (S, 700k)
LT1112 (D, 5M)
LT1113 (D, 1.2M)
LT1114 (Q, 5M)
LT1115 (S, 7M)
LT1124 (D, 5M)
LT1125 (Q, 5M)
LT1126 (D, 5M)
LT1127 (D, 5M)
LT1128 (S, 7M)
LTC1152 (S, 3M)
LT1169 (D, 1.2M)
LT1413 (D, 1.5M)

Single Supply

Low Power

Single or Dual Supplies

LT1006 (S, 520µA)
LT1013 (D, 1mA)
LT1014 (Q, 2mA)
LTC1047 (S, 55µA)
LTC1049 (S, 300µA)
LT1077 (S, 60µA)
LT1078 (D, 100µA)
LT1079 (Q, 200µA)
LT1178 (D, 36µA)
LT1179 (Q, 72µA)
LT1413 (D, 330µA)

Low V_{OS} Low Power

LT1006 (S, 50µV, 520µA)
LT1013 (D, 150µV,1mA)
LT1014 (Q, 180µV, 2mA)
LTC1049 (S, 10µV, 300µA)
LT1112 (D, 60µV, 800µA)
LT1114 (Q, 60µV, 1.6mA)
LTC1152 (S, 10µV, 2.2mA)
LT1413 (D, 280µV, 0.9µA)

Low V_{OS} Micropower

LTC1047 (D, 10µV, 55µA)
LT1077 (S, 40µV,60µA)
LT1078 (D, 70µV, 100µA)
LT1079 (Q, 100µV, 200µA)
LT1178 (D, 70µV, 36µA)
LT1179 (Q, 100µV, 72µA)

Low V_{OS} High Speed

LT1211 (D, 150µV, 14MHz)
LT1212 (Q, 275µV, 14MHz)
LT1213 (D, 150µV, 28MHz)
LT1214 (Q, 275µV, 28MHz)
LT1215 (D, 300µV, 23MHz)
LT1216 (Q, 450µV, 23MHz)

Rail-to-Rail In/Out, Precision

LTC1152
LT1366/7
LT1368/9

Low Power

Wide Bandwidth

Fast Slew Rate Fast Settling

LT1122 (S, 80V/µs)
LT1187 (S, 165V/µs)
LT1189 (S, 165V/µs)
LT1190 (S, 450V/µs)
LT1191 (S, 450V/µs)
LT1192 (S, 450V/µs)
LT1193 (S, 500V/µs)
LT1194 (S, 500V/µs)
LT1195 (S, 165V/µs)
LT1200 (S, 50V/µs)
LT1201 (D, 50V/µs)
LT1202 (Q, 50V/µs)
LT1204 (S, 1000V/µs)*
LT1206 (S, 900V/µs)*
LT1208 (D, 400V/µs)
LT1209 (Q, 400V/µs)
LT1215 (D, 50V/µs)
LT1216 (Q, 50V/µs)
LT1217 (S, 500V/µs)*
LT1220 (S, 250V/µs)
LT1221 (S, 250V/µs)
LT1222 (S, 200V/µs)
LT1223 (S, 1000V/µs)*
LT1224 (S, 400V/µs)
LT1225 (S, 400V/µs)
LT1226 (S, 400V/µs)
LT1227 (S, 1100V/µs)*
LT1229 (D, 1000V/µs)*
LT1230 (Q, 1000V/µs)*
LT1252 (S, 250V/µs)*
LT1253 (D, 250V/µs)*
LT1254 (Q, 250V/µs)*
LT1259 (D,1600V/µs)*
LT1260 (T, 1600V/µs)*
LT1354 (S, 400V/µs)
LT1355 (D, 400V/µs)
LT1356 (Q, 400V/µs)
LT1357 (S, 600V/µs)
LT1358 (D, 600V/µs)
LT1359 (Q, 600V/µs)
LT1360 (S, 800V/µs)
LT1361 (D, 800V/µs)
LT1362 (Q, 800V/µs)
LT1363 (S, 1000V/µs)
LT1364 (D, 1000V/µs)
LT1365 (Q, 1000V/µs)

Video

LT1187 (S, 50MHz)
LT1189 (S, 35MHz)
LT1190 (S, 50MHz)
LT1191 (S, 90MHz)
LT1192 (S, 40MHz)
LT1193 (S, 70MHz)
LT1194 (S, 40MHz)
LT1195 (S, 50MHz)
LT1204 (S, 70MHz)*
LT1206 (S, 60MHz)*
LT1223 (S, 100MHz)*
LT1227 (S, 140MHz)*
LT1229 (D, 100MHz)*
LT1230 (Q, 100MHz)*
LT1252 (S, 100MHz)*
LT1253 (D, 90MHz)*
LT1254 (Q, 90MHz)*
LT1259 (D, 130MHz)*
LT1260 (T, 130MHz)*
LT1360 (S, 50MHz)
LT1361 (D, 50MHz)
LT1362 (Q, 50MHz)
LT1363 (S, 70MHz)
LT1364 (D, 70MHz)
LT1365 (Q, 70MHz)

Non-Video

LT1220 (S, 45MHz)
LT1221 (S, 37MHz)
LT1222 (S, 50MHz)
LT1224 (S, 45MHz)
LT1225 (S, 30MHz)
LT1226 (S, 40MHz)
LT1208 (D, 45MHz)
LT1209 (Q, 45MHz)
LT1358 (D, 25MHz)
LT1359 (Q, 25MHz)

Low Power

LT1200 (S, 1mA, 10MHz)
LT1201 (D, 1mA, 11MHz)
LT1202 (Q, 1mA, 11MHz)
LT1217 (S, 1mA, 10MHz)*
LT1354 (S, 1mA, 12MHz)
LT1355 (D, 1mA, 12MHz)
LT1356 (Q, 1mA, 12MHz)

*Current feedback amplifier

Instrumentation

Micropower

LT1101

Zero Drift

LTC1100

High Speed

LT1102

2

HIGH SPEED

Instrumentation and Data Acquisition

- Fast DAC Amplifiers
- Signal Processing
- RF Amplification
- RADAR
- Fiber-Optic Systems
- Copiers/Laser Printers

Color, B/W Video and Multimedia

- Frame Grabbers
- Video Cable Drivers
- Video MUXs
- Cable Tappers
- Video Gain Blocks
- Building Security
- Image Recognition
- Video Keyer/Fader

Lowest Offsets, Lowest Bias Current

Fastest Slew Rate, Fastest Settling

Dual Supplies, Largest Bandwidth

±5V, or Single 5V Supplies, Lowest Cost

Single Supply, DC Precision

- Low V_{OS} with High Bandwidth/Slew Rate (150µV Max, A-Grades)
- Single Supply 3.3V, 5V or Dual ±15V Operation
- Low Power (1.3mA/Amp): LT1211/12
- Fast Settling to 0.01%, 250ns, 2V Step: LT1215/16
- SO-8 (Duals) and 0.150" SO-16 (Quads)

	GBW (Typ) MHz	SR (Typ) V/µs	V_{OS} (Max) µV
LT1211 (D)	14	7	150/275
LT1212 (Q)	14	7	275
LT1213 (D)	28	12	150/275
LT1214 (Q)	28	12	275
LT1215 (D)	23	50	300/450
LT1216 (Q)	23	50	450

Voltage Feedback Op Amps

- 12-Bit Accurate: LT1220/21/22
- 10-Bit Accurate: LT1224/25/26
- C-Load: Drives Unlimited Capacitive Loads

	A_V (Min) V/V	GBW (Typ) MHz	0.1% Settling Time ns	SR (Typ) V/µs	V_{OS} (Max) mV
LT1220	1	45	75	250	1.0
LT1221	4	150	65	250	0.6
LT1222	10	500	75	200	0.3
LT1224	1	45	90	400	2.0
LT1225	5	150	90	400	1.0
LT1226	25	1000	100	400	1.0

NEW AMPLIFIER ARCHITECTURE!

Voltage Feedback Op Amps with Current Feedback Speed

- Low Supply Current/Amplifier (1mA): LT1355/6
- Very High Slew Rate (1000V/µs): LT1363
- Low V_{OS} (0.6mV Maximum): LT1358/9
- Low Power (6mA/Amplifier for 1000V/µs Slew Rate)
- Fast Settling (80ns to 0.01%, 50ns to 0.1%, 10V Step)
- C-Load™: Drives Unlimited Capacitive Loads

Single	Dual	Quad	GBW MHz	SR V/µs	I_S/Amp (mA)
LT1354	LT1355	LT1356	12	400	1
LT1357	LT1358	LT1359	25	600	2
LT1360	LT1361	LT1362	50	800	4
LT1363	LT1364	LT1365	70	1000	6

Current Feedback Amps

- Bandwidth Independent of Gain
- "Shutdown" Feature: LT1217, LT1223, LT1227.
- Single Supply Operation/Best for Video: LT1227, LT1229, LT1230.
- 12-Bit Accurate: LT1223
- Low Power (I_S = 1mA): LT1217
- Lowest Cost: LT1252/3/4
- Operates on ±2V to ±15V Supplies*

* LT1223 & LT1217 Min Supply Voltage = ±5V

	BW (Typ) MHz	SR (Typ) V/µs	V_{OS} (Max) mV
LT1227	140	1100	10
LT1223	100	1300	3
LT1229 (D)	100	1000	10
LT1230 (Q)	100	1000	10
LT1217	10	500	3
LT1252	100	250	15
LT1253 (D)	90	250	15
LT1254 (Q)	90	250	15

Low Cost Video Op Amps

- Specified Operation with ±5V and Single 5V Supplies
- Color Video Performance
- "Shutdown" Feature: LT1190/1/2
- Directly Drives Cables: 50mA I_{OUT}
- 450V/µs Slew Rate
- Low Power: LT1195

	GBW (Typ) MHz	SR (Typ) V/µs	A_V (Min) V/V
LT1190	50	450	1
LT1191	90	450	1
LT1192	350	450	5
LT1195	50	165	1

(D) = Dual, (Q) = Quad

C-Load is a trademark of Linear Technology Corporation

Video Products

In addition to high speed amplifiers, LTC offers the following products tailored to video, multimedia and computer graphics applications.

Low Cost Dual/Triple 130MHz CFAs with Shutdown

- LT1260: Triple CFA for RGB Video
- LT1259: Dual CFA with Shutdown
- 90MHz Bandwidth on ±5V
- 0.1dB Gain Flatness, 30MHz: Good for HDTV
- 1600V/µs Slew Rate
- ±2V to ±15V Supply Range
- 100ns/40ns Turn On/Off Times
- Makes 2 or 3 Input MUX Amp
- Low Supply Current (5mA/Amp)
- Narrow SO Packages

±5V Video Difference Amps

- 50dB CMRR @ 10MHz
- Input Voltage Range: (–2.5V to 3.5V)
- ±4V Output Voltage Swing
- Color Video Performance
- "Shutdown" Feature
- Can Directly Drive Cables
- 500V/µs Slew Rate: LT1193/LT1194
- Low Power: LT1187/LT1189

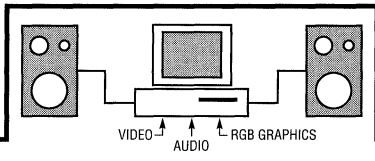
	Gain	A_V (Min) V/V	BW (Typ) MHz
LT1187	Adj.	2	50
LT1189	Adj.	10	35
LT1193	Adj.	2	70
LT1194	Fixed	10	350

Video Distribution Amplifier

- LT1206: 250mA Minimum Output Current
- 60MHz, 900V/µs Current Feedback Amplifier
- Drives Ten 150Ω Video Cables
- Drives Low Impedances and High Capacitances
- Color Video Performance
- Low Current "Shutdown" Mode Available

2:1 and 4:1 Video Multiplexers Very Fast for Pixel Switching

- LT1203 (2:1), LT1205 (2 × 2:1 or 4:1)
- 150MHz, –3dB Bandwidth
- 90dB Channel Separation
- 30MHz, 0.1dB Gain Flatness (HDTV)
- 25ns Channel Switching Time
- 50mV Switching Transient
- 10MΩ Disabled Output Impedance
- Expandable
- 8- and 16-Pin Narrow SO Packages



4:1 Video Multiplexer with 75MHz Current Feedback Amplifier

- LT1204: 4:1 MUX w/ Current Feedback Amp
- 0.1dB Gain Flatness to >30MHz: for HDTV
- 1000V/µs Slew Rate
- 75MHz, –3dB Bandwidth (A_V = 2)
- 90dB Channel Separation
- Expandable
- 16-Pin PDIP and SW Packages

Current Feedback Amp with DC Gain Control

- LT1228: 75MHz Transconductance Amp with 100MHz Current Feedback Amplifier
- Color Video Performance
- Differential Input
- Operates on ±2V to ±15V Supplies
- For Auto-Gain, Tunable Filters, and Specialized Video Circuits.

Video Fader/Gain-Controlled Amplifier

- LT1251: 40MHz Video Fader
- LT1256: 40MHz Gain-Controlled Amplifier
- Accurate 1% Linear Gain Control
- Low Differential Gain/Phase, 0.1%/0.1°
- 14-Pin PDIP and SO Packages

Multimedia

Multimedia systems combine **audio, composite video** (broadcast quality TV) and **high resolution computer graphics.**
Typical requirements are:

Video: NTSC or **PAL** need minimum 50MHz, –3dB bandwidth
HDTV needs 0.1dB flatness to 30MHz

Suggested Products (Refer to above and reverse side):

General Purpose Gain Blocks/Video A/D Buffers	LT1360/61/62/63/64/65: Single/Dual/Quad Voltage Feedback Op Amps with Current Feedback Speed LT1227/29/30: Single/Dual/Quad Current Feedback Amplifiers LT1252/3/4: Low Cost Current Feedback Amplifiers
Multiplexer	LT1204: 4:1 Video MUX with CFA
Video Distribution	LT1206: 250mA Output Current CFA
DC Restoration	LT1228: CFA with Gain Control
Gain Control	LT1228: CFA with Gain Control, LT1256: 40MHz Amplifier with DC Gain Control
COAX Loopthrough/ Twisted-Pair Receiver	LT1187/89/93/94: Video Difference Amplifiers

Graphics: VGA needs >50MHz, **19" monitors** need >100MHz

RGB, YUV, YC, Amps	LT1259/60: Dual/Triple, 130MHz, 1800V/µs Current Feedback Amplifiers with Shutdown
Pixel Switching	LT1203/05: 2:1 and 4:1 Video Multiplexers

Audio: For 8× Oversampling, 200kHz Bandwidth is Required

Gain Blocks	LT1115: Low Noise Preamplifier LT1124/26: Dual Low Noise Preamplifier LT1211/12: High Slew Rate, Single Supply Dual/Quad Op Amps LT1122: Ultra-Low Distortion Op Amp with Symmetric Slew Rates. LT1354/55/56: Ultra-High Slew Rate, Low Supply Current Op Amps

CD-ROM LT1311: Quad Precision I-to-V Converter for Optical Drivers

Commercial Precision Op Amps

PART NUMBER	ELECTRICAL CHARACTERISTICS								IMPORTANT FEATURES
	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (nA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	MIL/ IND TEMP	
SINGLE									
LT1001AC	25	0.6	2.0	450	0.15	18	H, J8, N8	M	Extremely Low Offset Voltage, Low Noise, Low Drift
LT1001C	60	1.0	3.8	400	0.15	18	H, J8, N8, S8	M	
LT1006AC	50	1.3	15	1000	0.25	24†	H, J8	M	Single Supply Operation, Fully Specified for 5V Supply
LT1006C	80	1.8	25	700	0.25	24†	H, J8, N8	M	
LT1006S8	400	3.5	25	700	0.25	25	S8		
LT1007AC	25	0.6	35	7000	1.7	4.5	H, J8, N8	M	Extremely Low Noise, Low Drift
LT1007C	60	1.0	55	5000	1.7	4.5	H, J8, N8, S8	M,I	
LT1008C	120	1.5	0.1	200	0.1	30	H, N8	M, I	Low Bias Current, Low Power
LT1012C	25	0.6	0.1	300	0.1	30	H, N8	M, I	Low V_{OS}, Low Power, C-Load™ Stable
LT1012AC	50	1.5	0.15	200	0.1	30	H, N8	M	
LT1012D	60	1.7	0.15	200	0.1	30	H, N8		
LT1012S8	120	1.8	0.28	200	0.1	30	S8		
LT1022AC	250	5.0	0.05	150	23	50	H	M	Very High Speed JFET Input Op Amp with Very Good DC Specs
LT1022C	600	9.0	0.05	120	18	60	H	M	
LT1022CN8	1000	15.0	0.05	100	18	60	N8		
LT1028AC	40	0.8	90	7000	11	1.7	H, J8, N8	M	Lowest Noise, High Speed, Low Drift
LT1028C	80	1.0	180	5000	11	1.9	H, J8, N8, S8	M	
LT1037AC	25	0.6	35	7000	11	4.5	H, J8, N8	M	Extremely Low Noise, High Speed
LT1037C	60	1.0	55	5000	11	4.5	H, J8, N8, S8	M, I	
LT1055AC	150	4	0.05	150	10	50	H	M	Lowest Offset, JFET Input Op Amp Combines High Speed and Precision
LT1055C	400	8	0.05	120	7.5	60	H	M	
LT1055CN8	700	12	0.05	120	7.5	60	N8		
LT1055S8	1500	15	0.1	120	7.5	70	S8		
LT1056AC	180	4	0.05	150	12	50	H	M	
LT1056C	450	8	0.05	120	9	60	H	M	
LT1056CN8	800	12	0.05	120	9	60	N8		
LT1056S8	1500	15	0.1	120	9.0	70	S8		
LT1077AC	40	0.4	9	250	0.12	40	H, J8, N8	M, I	Micropower, Single Supply, Precision, Low Noise
LT1077C	60	0.4	11	200	0.12	29†	H, J8, N8	M, I	
LT1077S8	150	3.0	11	240	0.05	28†	S8		
LT1097C	50	1.0	0.25	700	0.1	16†	N8	I	Low Cost, Low Power Precision, C-Load Op Amp
LT1097S8	60	1.4	0.35	700	0.1	16†	S8	I	
LT1115C	280	0.5 (Typ)	380	2000	10	1.8	N8, S		Lowest Noise, Ultra Low Distortion Audio Optimized Op Amp
LT1128AC	40	1.0	90	7000	5.0	1.7	J8, N8, S8	M, I	Lowest Noise, High Speed, Precision
LT1128C	80	1.0	180	5000	4.5	1.9	J8, N8, S8	M, I	
LTC1049C	10	0.1	0.050	3162	0.8†	1.0μV_{P-P}**	J8, N8	M, I	Auto Zeroed Precision Op Amp, No External Capacitors Required
LTC1050AC	5	0.05	0.035	3162	4†	0.6μV_{P-P}**	H, J8, N8, S8	M, I	
LTC1050C	5	0.05	0.050	1000	4†	0.6μV_{P-P}**	H, J8, N8, S8	M, I	
LTC1052C	5	0.05	0.03	1000	3†	0.5μV_{P-P}**	H, N8, N	M, I	Low Noise, Auto Zeroed Precision Op Amp
LTC7652C	5	0.05	0.03	1000	3†	0.5μV_{P-P}**	H, N8	M, I	
LTC1150C	5	0.05	0.03	10000	3†	0.6μV_{P-P}**	H, J8, N8, S8	M, I	Auto Zeroed Precision Op Amp That Operates on Standard ±15V Supplies. No External Capacitors Required
LTC1152C	10	0.1	0.1	316	1†	0.5μV_{P-P}	N8, S8		Rail-to-Rail Input and Output, Auto Zeroed Precision Op Amp. C-Load Stable.
LTC1250C	10	0.05	0.02	10000	10†	0.3mV_{P-P}**	J8, N8, S8	M	Low Noise, Auto Zeroed Precision Op Amp

† Typical spec * 100Hz noise ** DC to 1Hz noise C-Load is a trademark of Linear Technology Corporation

NOTE: See page 4-3 for DESC cross reference numbers. Check data sheet for specifications on industrial and military temperature produced and surface mount.

Commercial Precision Op Amps

PART NUMBER	ELECTRICAL CHARACTERISTICS								IMPORTANT FEATURES
	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (nA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	MIL/ IND TEMP	
SINGLE									
LF355A	2000	5	0.05	75	5	25†*	H, N8		JFET Inputs, Low I_B, No Phase Reversal
LF356A	2000	5	0.05	75	10	15†*	H, N8		
LM10B	2000	2†	20	120	—	50†	H, J8	M	On-Chip Reference Operates with +1.2V Single Battery
LM10BL	2000	2†	20	60	—	50†	H, J8		
LM10C	4000	5†	30	80	—	50†	H, J8, N8		
LM10CL	4000	5†	30	80	—	50†	H, J8, N8		
LM308A	500	5	7	60	0.1	30†	H, N8	M	Low Bias, Supply Current
LT318A	1000		250	200	50	42†	H, J8, N8	M	High Speed, 15MHz
LM318	10000		500	25	50	42†	H, J8, N8, S8	M	High Speed, 15MHz
OP-05C	1300	4.5	7	120	0.1	20	H, J8, N8	M	Low Noise, Low Offset Drift with Time
OP-05E	500	2.0	4	200	0.1	18	H, J8, N8	M	
OP-07C	150	1.8	7	120	0.1	20	H, J8, N8, S8	M	Low Initial Offset, Low Noise, Low Drift
OP-07E	75	1.3	4	200	0.1	18	H, J8, N8	M	
OP-15E	500	5	0.05	100	10	20†*	H, N8	M	Precision JFET Input, Low Bias Current, No Phase Reversal
OP-15F	1000	10	0.1	75	7.5	20†*	H, N8	M	
OP-15G	3000	15	0.2	50	5	20†*	H, N8	M	
OP-16E	500	5	0.05	100	18	20†*	H, N8	M	Precision JFET Input, High Speed, No Phase Reversal
OP-16F	1000	10	0.1	75	12	20†*	H, N8	M	
OP-16G	3000	15	0.2	50	9	20†*	H, N8	M	
OP-27E	25	0.6	40	1000	1.7	5.5	H, J8, N8	I	Very Low Noise, Unity Gain Stable
OP-27G	100	1.8	80	700	1.7	8.0	H, N8	I	
OP-37E	25	0.6	40	1000	11	5.5	H, J8, N8	I	Very Low Noise, Stable for Gains ≥ 5
OP-37G	100	1.8	80	700	11	8.0	H, N8	I	
OP-97E	25	0.6	±0.1	300	0.1	30	H, N8	M	Low Power, Low I_B, Precision
DUAL									
LT1002AC	60	0.9	3.0	400	0.15	20	J, N	M	Dual, Matched LT1001 High CMRR, PSRR Matching
LT1002C	100	1.3	4.5	350	0.15	20	J, N	M	
LT1013AC	150	2.0	20	1500	0.2	24†	H, J8	M	Precision Dual Op Amp in 8-Pin Package
LT1013C	300	2.5	30	1200	0.2	24†	H, J8, N8	M, I	
LT1013D	800	5.0	30	1200	0.2	24†	N8, S8		
LT1024AC	50	1.5	0.12	250	0.1	33	N	M	Low V_{OS}, Low Power, Matching Specs
LT1024C	100	2.0	0.20	180	0.1	33	N	M	
LTC1047C	10	0.01	0.02	1000	0.2†	0.8mVp-p**	N8, S		No External Capacitors Required
LTC1051C	5	0.05	0.05	1000	4†	0.4μVp-p**	J8, N8, S	M, I	Dual, Precision Auto Zeroed Op Amp
LT1057AC	450	7	0.05	150	10	26†	H, J8	M	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1057ACN8	450	10	0.05	150	10	26†	N8		
LT1057C	800	12	0.075	100	8	26†	H, J8	M, I	
LT1057CN8	800	16	0.075	100	8	26†	N8, S8	I	
LT1078AC	70	2.0	8	250	0.07†	40	H, J8, N8	M	Micropower, Precision, Single Supply, Low Noise Dual
LT1078C	120	2.5	10	200	0.07†	29†	H, J8, N8, S8	M, I	
LT1112A	60	0.50	0.25	1000	0.16	15†	J8, N8, S8	M, I	Low Power, Precision, Matching Specs, C-Load Op Amp
LT1112C	75	0.75	0.28	800	0.16	15†	J8, N8, S8	M, I	
LT1113AC	1500	15	0.45	1200	2.5	17†	N8, J8, S8	M, I	Dual Low Noise, Precision JFET Input
LT1113C	1800	20	0.48	1000	2.5	17†	N8, J8, S8	M, I	
LT1124AC	70	1	55	2000	3	5.5	N	M, I	Dual Precision Op Amp, Low Noise, High Speed
LT1124C	100	1.5	70	1500	2.7	5.5	J, N, S	M, I	

† Typical spec * 100Hz noise ** DC to 1Hz noise **NOTE:** See page 4-3 for DESC cross reference numbers

Commercial Precision Op Amps

PART NUMBER	ELECTRICAL CHARACTERISTICS								IMPORTANT FEATURES
	V_{OS} MAX (μV)	TC V_{OS} (μV/°C)	I_B MAX (nA)	A_{VOL} MIN (V/mV)	SLEW RATE MIN (V/μs)	NOISE MAX 10Hz (nV/√Hz)	PACKAGES AVAILABLE	MIL/ IND TEMP	
DUAL									
LT1126AC	70	1.0	20	2000	8	5.5	N8	M, I	Dual Precision Op Amp, Low Noise, High Speed
LT1126C	100	1.5	30	1500	8	5.5	J8, N8, S8	M, I	
LT1169A	1500	15	0.003	1200	2.4	17†	J8, N8, S8		Dual Low Noise, Picoampere Bias Current JFET Input Op Amp
LT1169C	1800	20	0.005	1000	2.4	17†	J8, N8, S8		
LT1178AC	70	2.2	5	140	0.013	75	H, J8, N8		17μA Max, Single Supply, Precision Dual
LT1178C	120	3.0	6	110	0.013	50†	H, J8, N8	I	
LT1211C	275	0.6	125	250	4	12.5	J8, N8, S8	M, I	Fast, Precise, Single Supply Op Amps. Industrial Temperature (–40°C to 85°C) Specs Included with Commercial Temperature Devices
LT1211AC	150	0.5	100	250	4	12.5	J8, N8, S8	M, I	
LT1213C	275	0.6	200	250	8.5	10	J8, N8, S8	M, I	
LT1213AC	150	0.5	160	250	8.5	10	J8, N8, S8	M, I	
LT1215C	450	1.0	600	150	30	15	J8, N8, S8	M, I	
LT1215AC	300	0.8	500	150	30	15	J8, N8, S8	M, I	
LT1366C	475	6	35	500	0.12†	29†***	N8, S8	I	Rail-to-Rail Input and Output, Precision
LT1368C	475	6	35	500	—	29†***	N8, S8	I	Rail-to-Rail Input and Output, Precision
LT1413AC	150	2	15	400	0.2	24†	N8	I	Dual Single Supply Precision Op Amp Optimized for 5V and GND
LT1413C	280	2.5	18	350	0.2	24†	N8, S8	I	
LT1413S8	380	2.5	18	350	0.2	24†	S8	I	
LT1457AC	450	10	0.05	150	2	26†	N8	I	Dual Precision JFET Input Op Amp. C-Load Stable
LT1457C	800	16	0.075	100	2	28†	N8, S8	I	
LF412AC	1000	10	0.1	100	10	20†*	H, J8, N8	M	High Performance Dual JFET Input Op Amp
OP-215E	1000	10	0.1	150	10	20†*	H, J8, N8	M	
OP-215G	3000	20	0.2	50	8	20†*	H, J8, N8	M	
OP-227E	80	1.0	40	3000	1.7	6	J, N	M	Dual Matched OP-27
OP-227G	180	1.8	80	2000	1.7	9	J, N	M	
OP-237E	80	1.0	40	3000	10	6	J, N	M	Dual Matched OP-37
OP-237G	180	1.8	80	2000	10	9	J, N	M	
OP-270A	75	1	20	750	1.7	6.5	J	M	Dual Op Amp, Low Noise
OP-270C	250	3	60	350	1.7	3.6†	N, S	M	
QUAD									
LT1014AC	180	2.0	20	1500	0.2	24†	J	M	Precision Quad Op Amp in 14-Pin Package
LT1014C	300	2.5	30	1200	0.2	24†	J, N	M, I	
LT1014D	800	5.0	30	1200	0.2	24†	N, S		
LT1058AC	600	10	0.05	150	10	26†	J	M	Low Offset JFET Input Multiple Op Amps Combine High Speed and Excellent DC Specs
LT1058C	1000	15	0.075	100	8	26†	J, N, S	M, I	
LT1079AC	120	2.0	8	250	0.07†	40	J, N	M	Micropower, Precision, Single Supply, Low Noise Quad
LT1079C	150	2.5	10	200	0.07†	29†	J, N, S	M, I	
LT1114AC	60	0.50	0.25	1000	0.16	15†	J8, N8, S8	M, I	Low Power, Precision, Matching Specs
LT1114C	75	0.75	0.28	800	0.16	15†	J8, N8, S8	M, I	
LT1125AC	90	1	20	2000	3	5.5	N	M	Precision Quad Op Amp, Low Noise, High Speed
LT1125C	140	1.5	30	1500	2.7	5.5	J, N, S	M, I	
LT1127AC	90	1.0	20	2000	8	5.5	N	M	
LT1127C	140	1.5	30	1500	8	5.5	N, J, S	M, I	
LT1179AC	100	2.2	5	140	0.013	75	J, N		17μA Max, Single Supply, Precision Quad
LT1179C	150	3.0	6	110	0.013	50†	J, N	I	
LT1212C	275	6	125	250	4	12.5†	N, S	I	Fast, Precise, Single Supply Op Amps. Industrial Temperature (–40°C to 85°C) Specs Included with Commercial Temperature Devices
LT1214C	275	6	200	250	8.5	10†	N, S	I	
LT1216C	450	10	600	150	30	15†	N, S	I	
LT1367C	800	6	35	500	0.12†	29†***	N8, S8	I	Rail-to-Rail Input and Output, Precision Can Handle 0.1μF C-Load
LT1369C	800	6	35	500	—	29†***	N, S	I	Rail-to-Rail Input and Output, Precision Can Handle 0.1μF C-Load
LTC1053C	5	0.05	0.05	1000	4†	0.4μVp-p**	N, S	I	Quad, Precision Auto Zeroed Op Amp. No External Capacitors Required
OP-470A	400	2	25	500	1.4	6.5	J	M	Quad Op Amp, Low Noise
OP-470C	1000	2†	60	400	1.4	6.5	N, S		

† Typical spec * 100Hz noise ** DC to 1Hz noise *** 1kHz noise

NOTE: See page 4-3 for DESC cross reference numbers

High Speed Op Amps

PART NUMBER	ELECTRICAL CHARACTERISTICS								IMPORTANT FEATURES
	MIN SLEW RATE (V/µs)	TYP SETTLING TIME TO 0.1 % (ns)	TYPICAL GAIN BANDWIDTH PRODUCT (MHz)	MIN A_{VOL} (V/mV)	MAX V_{OS} (mV)	I_B MAX (µA)	PACKAGES AVAILABLE	MIL/ IND TEMP	
SINGLE									
LM118	50		15	50	4	0.25	H, J8	M	Industry Standard
LT118A	50		15	100	1	0.25	H, J8	M	Improvement Over LM118
LT318A	50		15	100	1	0.25	H, J8, N8		Commercial Temp Version of LT118A
LT1028AC	11		75	7000	0.04	0.09	H, J8, N8	M	Ultra-Low Noise, Precision, Low Drift
LT1028C	11		75	5000	0.08	0.18	H, J8, N8, S8	M	Ultra-Low Noise, Precision, Low Drift
LT1037AC	11		60	7000	0.025	0.035	H, J8, N8	M	A_V = 5, Low Noise, Precision
LT1037C	11		60	5000	0.06	0.055	H, J8, N8, S8	M	A_V = 5, Low Noise, Precision
LT1115C	10		70	2000	0.2	0.38	N8, SW16		Ultra-Low Noise, Low Distortion, Audio
LT1122AC	60	340* 540**	14	180	0.6	75pA	J8, N8	M	JFET Input. Faster and Better DC Specs Than OP-42. A and C Have Grades 100% Tested Settling Time
LT1122BC	60	350*	14	180	0.6	75pA	J8, N8	M	
LT1122CC	50	350* 590**	13	150	0.9	100pA	J8, N8, S8	M	
LT1122DC	50	360*	13	150	0.9	100pA	J8, N8, S8	M	
LT1128AC	5		20	7000	0.04	0.09	N8		Ultra-Low Noise, Precision, Unity-Gain Stable
LT1128C	4.5		20	5000	0.08	0.18	N8, S8		Ultra-Low Noise, Precision, Unity-Gain Stable
LT1187C	130	100***	50 (A_V = 2)		10	2	N8, S8		Low Power Video Difference Amplifier
LT1189C	175	1000***	35 (A_V = 10)		3	2	N8, S8		
LT1190C	450†	100	50	3.5	10	2.5	J8, N8, S8	M	±5V Supply Color Video Op Amps
LT1191C	450†	100	90	6	5	2.5	J8, N8, S8	M	
LT1192C	450†	100	400 ($A_V \geq 5$)	16	2.5	2.5	J8, N8, S8	M	
LT1193C	450†	100	70		12	3.5	J8, N8, S8	M	Color Video Differential Amplifier
LT1194C	450†	100	40		6	3.5	J8, N8, S8	M	
LT1195C	140	220***	50	0.5	8	2	J8, N8, S8	M	Low Power, High Speed
LT1200C	30	430	11.0	4	1	1	N8, S8		Low Supply Current Op Amp
LT1206C	600		50	0.6	15	5	N8, R, Y, S8		250mA Current Feedback Amplifier
LT1217C	100	280	10.0	3.2	3	0.5	N8, S8		Low Power Current Feedback Amplifier
LT1220C	200	75	45	20	1	0.3	H, J8, N8, S8		Ultra High Speed, Good DC Specs, C-Load Driving
LT1221C	200	65	150 ($A_V \geq 4$)	50	0.6	0.3	H, J8, N8, S8		
LT1222C	200	75	500 ($A_V \geq 10$)	100	0.3	0.3	H, J8, N8, S8	M	
LT1223C	800	75	100	3.2	3	3	J8, N8, S8	M	Current Feedback Amplifier with Good DC Specs
LT1224C	250	90	45	3.3	2	8	J8, N8, S8	M	High Speed, DC Precision, Stable While Driving Unlimited Capacitive Load (C-Load)
LT1225C	250	70	150 ($A_V \geq 5$)	12.5	1	8	J8, N8, S8	M	
LT1226C	250	75	1000 ($A_V \geq 25$)	50	1	8	J8, N8, S8	M	
LT1227C	500	50	140.0	0.6	10	3	J8, N8, S8	M	Current Feedback Amplifier
LT1228C	300	45	100	0.6	10	3	J8, N8, S8	M	Electronic DC Gain Control
LT1252C	250		100	0.56	15	15	N8, S8		Low Cost Video Amplifier
LT1354C	200	230	12	12	0.8	0.3	N8, S8		1mA, 12MHz, 400V/µs C-Load
LT1357C	300	115	25	20	0.6	0.5	N8, S8		2mA, 25MHz, 600V/µs C-Load
LT1360C	600	60	50	4.5	1	1	N8, S8		4mA, 50MHz, 800V/µs C-Load
LT1363C	750	50	70	4.5	1.5	2	N8, S8		6mA, 70MHz, 1000V/µs C-Load
DUAL									
LT1124AC	3		12.5	5000	0.07	0.025	J8, N8	M	Dual, Low Noise, Precision
LT1124C	2.7		12.5	3000	0.1	0.03	J8, N8, S8	M	Dual, Low Noise, Precision
LT1126AC	8		45	5000	0.07	0.02	J8, N8	M	A_V = 10, Dual, Low Noise, Precision
LT1126C	8		45	3000	0.1	0.03	J8, N8, S8	M	A_V = 10, Dual, Low Noise, Precision
LT1201C	30	330	12	4	2	1	N8, S8		1mA, 12MHz, 50V/µs Dual C-Load
LT1208C	250	90	45	3.3	3	8	N8, S8		45MHz, 450V/µs Dual C-Load

†Typical value *10V step, to 1mV at sum node. **Maximum value, 10V step, to 1mV at sum node. ***3V Step

NOTE: See page 4-3 for DESC cross reference numbers

High Speed Op Amps

PART NUMBER	ELECTRICAL CHARACTERISTICS								IMPORTANT FEATURES
	MIN SLEW RATE (V/μs)	TYP SETTLING TIME TO 0.1 % (ns)	TYPICAL GAIN BANDWIDTH PRODUCT (MHz)	MIN A_{VOL} (V/mV)	MAX V_{OS} (μV)	MAX I_B (μA)	PACKAGES AVAILABLE	MIL/ IND TEMP	
DUAL									
LT1211C	5	2200	14	1200	0.55	0.12	J8, N8, S8	M	14MHz, 7V/μs Single Supply Precision
LT1211AC	5	2200	14	1200	0.4	0.095	J8, N8, S8	M	
LT1213C	10	1100	28	1200	0.55	0.19	J8, N8, S8	M	28MHz, 12V/μs, Single Supply Precision
LT1213AC	10	1100	28	1200	0.4	0.15	J8, N8, S8	M	
LT1215C	40	480	23	1000	0.65	0.55	J8, N8, S8	M	23MHz, 50V/μs, Single Supply Precision
LT1215 AC	40	480	23	1000	0.5	0.5	J8, N8, S8	M	
LT1229C	300	45	100	0.6	10	3	J8, N8, S8	M	Fast Slew Rate, Current Feedback Architecture
LT1253C	250		90	0.560	15	15	N8, S8		Low Cost Video Amplifier
LT1259C	900	75	130	0.71	10	3	N14, S14		Low Cost 130MHz Dual CFAs with Individual Shutdowns
LT1355C	200	230	12	12	0.8	0.3	N8, S8		1mA, 12MHz, 400V/μs Dual C-Load
LT1358C	300	115	25	20	0.6	0.5	N8, S8		2mA, 25MHz, 600V/μs Dual C-Load
LT1361C	600	60	50	4.5	1	1	N8, S8		4mA, 50MHz, 800V/μs Dual C-Load
LT1364C	750	50	70	4.5	1.5	2	N8, S8		6mA, 70MHz, 1000V/μs Dual C-Load
TRIPLE									
LT1260C	900	75	130	0.71	10	3	N16, S16		Low Cost Triple 130MHz CFAs with Individual Shutdowns
QUAD									
LT1125AC	3		12.5	5000	0.09	0.02	J14, N14	M	Quad, Low Noise, Precision
LT1125	2.7		12.5	3000	0.14	0.03	J14, N14, S16	M	Quad, Low Noise, Precision
LT1127AC	8		45	5000	0.09	0.02	J14, N14	M	A_V = 10, Quad, Low Noise, Precision
LT1127C	8		45	3000	0.14	0.03	J14, N14, S16	M	A_V = 10, Quad, Low Noise, Precision
LT1202C	30	330	12	4	2	1	N14, S16		1mA, 12MHz, 50V/μs Quad C-Load
LT1209C	250	90	45	3.3	3	8	N14, S16		45MHz, 450V/μs Quad C-Load
LT1212C	5	2200	14	1200	0.55	0.12	N14, S16		14MHz, 7V/μs Single Supply Precision
LT1214C	10	1100	28	1200	0.55	0.19	N14, S16		28MHz, 12V/μs, Single Supply Precision
LT1216C	40	480	23	1000	0.65	0.55	N14, S16		23MHz, 50V/μs, Single Supply Precision
LT1230C	300	45	100	0.6	10	3	J14, N14, S14	M	Fast Slew Rate, Current Feedback Architecture
LT1254C	250		90	0.560	15	15	N14, S14		Low Cost Video Amplifier
LT1356C	200	230	12	12	0.8	0.3	N14, S16		1mA, 12MHz, 400V/μs Quad C-Load
LT1359C	300	115	25	20	0.6	0.5	N14, S16		2mA, 25MHz, 600V/μs Quad C-Load
LT1362C	600	60	50	4.5	1	1	N14, S16		4mA, 50MHz, 800V/μs Quad C-Load
LT1365C	750	50	70	4.5	1.5	2	N14, S16		6mA, 70MHz, 1000V/μs Quad C-Load

†Typical value *10V step, to 1mV at sum node. **Maximum value, 10V step, to 1mV at sum node. ***3V Step

NOTE: See page 4-3 for DESC cross reference numbers

C-Load™ Stable Op Amps C-Load Operational Amplifiers Are Stable with Any Capacitve Load.

PART NUMBER	# OF AMPS	MIN A_V	MAX V_{OS}	MAX I_B	MIN I_{OUT}	BANDWIDTH	SLEW RATE	I_S/AMP
LT1097	Single	1	60μV	350pA	5.7mA	700kHz	0.2V/μs	380μA
LT1012	Single	1	50μV	150pA	5.7mA	700kHz	0.2V/μs	380μA
LT1112	Dual	1	75μV	230pA	5.7mA	750kHz	0.3V/μs	350μA
LT1114	Quad	1	75μV	230pA	5.7mA	750kHz	0.3V/μs	350μA
LTC1152	Single	1	10μV	100pA	4mA	1MHz	1V/μs	500μA
LT1200	Single	1	1mV	1μA	6mA	11MHz	50V/μs	1mA
LT1201	Dual	1	2mV	1μA	6mA	12MHz	50V/μs	1mA
LT1202	Quad	1	2mV	1μA	6mA	12MHz	50V/μs	1mA
LT1206	Single	1	10mV	5μA	250mA	60MHz	900V/μs	5mA to 22mA
LT1208	Dual	1	3mV	8μA	24mA	45MHz	400V/μs	7mA
LT1209	Quad	1	3mV	8μA	24mA	45MHz	400V/μs	7mA
LT1220	Single	1	1mV	300nA	24mA	45MHz	250V/μs	8mA
LT1221	Single	4	0.6mV	300nA	24mA	150MHz	250V/μs	8mA
LT1222	Single	10	0.3mV	300nA	24mA	500MHz	200V/μs	8mA
LT1224	Single	1	2mV	8μA	20mA	45MHz	400V/μs	7mA
LT1225	Single	5	1mV	8μA	20mA	150MHz	400V/μs	7mA
LT1226	Single	25	1mV	8μA	20mA	1GHz	400V/μs	7mA
LT1354	Single	1	800μV	300nA	30mA	12MHz	400V/μs	1mA
LT1355	Dual	1	800μV	300nA	30mA	12MHz	400V/μs	1mA
LT1356	Quad	1	800μV	300nA	30mA	12MHz	400V/μs	1mA
LT1357	Single	1	600μV	500nA	30mA	25MHz	600V/μs	2mA
LT1358	Dual	1	600μV	500nA	30mA	25MHz	600V/μs	2mA
LT1359	Quad	1	600μV	500nA	30mA	25MHz	600V/μs	2mA
LT1360	Single	1	1mV	1μA	40mA	50MHz	800V/μs	4mA
LT1361	Dual	1	1mV	1μA	40mA	50MHz	800V/μs	4mA
LT1362	Quad	1	1mV	1μA	40mA	50MHz	800V/μs	4mA
LT1363	Single	1	1.5mV	2μA	70mA	70MHz	1000V/μs	6mA
LT1364	Dual	1	1.5mV	2μA	70mA	70MHz	1000V/μs	6mA
LT1365	Quad	1	1.5mV	2μA	70mA	70MHz	1000V/μs	6mA
LT1368	Dual	1	450μV	35nA	30mA	450kHz	0.15V/μs	375μA
LT1369	Quad	1	450μV	35nA	30mA	450kHz	0.15V/μs	375μA
LT1457	Dual	1	800μV	75pA	10mA	1.7MHz	4V/μs	1.8mA

C-Load is a trademark of Linear Technology Corporation

SECTION 2—AMPLIFIERS

PRECISION OPERATIONAL AMPLIFIERS

Dual and Quad Precision Rail-to-Rail Input and Output Op Amps

FEATURES

- **Input Common-Mode Range Includes Both Rails**
- **Output Swings Rail-to-Rail**
- **Low Input Offset Voltage: 150μV**
- High Common-Mode Rejection Ratio: 90dB
- High A_{VOL}: 1V/μV Minimum Driving 2kΩ Load
- Low Input Bias Current: 10nA
- Wide Supply Range: 1.8V to ±15V
- Low Supply Current: 375μA per Amplifier
- High Output Drive: 30mA
- 400kHz Gain-Bandwidth Product
- Slew Rate: 0.13V/μs
- Stable for Capacitive Loads up to 1000pF

APPLICATIONS

- Rail-to-Rail Buffer Amplifiers
- Low Voltage Signal Processing
- Supply Current Sensing at Either Rail
- Driving A/D Converters

DESCRIPTION

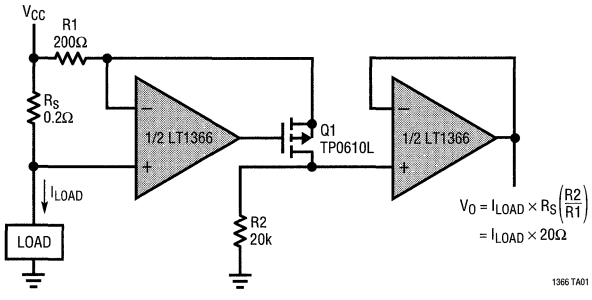
The LT®1366/LT1367/LT1368/LT1369 are dual and quad bipolar op amps which combine rail-to-rail input and output operation with precision specifications. These op amps maintain their characteristics over a supply range of 1.8V to 36V. Operation is specified for 3V, 5V and ±15V supplies. Input offset voltage is typically 150μV, with a minimum open-loop gain A_{VOL} of 1 million while driving a 2k load. Common-mode rejection is typically 90dB over the full rail-to-rail input range, and supply rejection is 110dB.

The LT1366/LT1367 have conventional compensation which assures stability for capacitive loads of 1000pF or less. The LT1368/LT1369 have compensation that requires a 0.1μF output capacitor, which improves the amplifier's supply rejection and reduces output impedance at high frequencies. The output capacitor's filtering action reduces high frequency noise, which is beneficial when driving A/D converters.

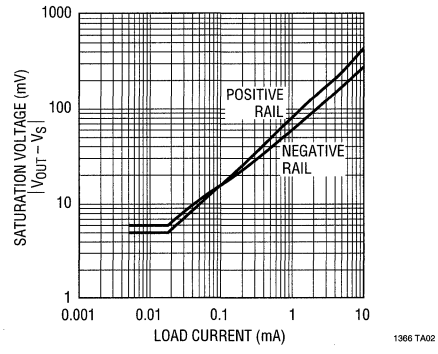
The LT1366/LT1368 are available in plastic 8-pin PDIP and 8-lead SO packages with the standard dual op amp pinout. The LT1367/LT1369 feature the standard quad pinout, which is available in a plastic 16-lead SO package. These devices can be used as plug-in replacements for many standard op amps to improve input/output range and precision.

TYPICAL APPLICATION

Positive Supply Rail Current Sense



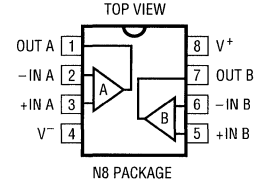
Output Saturation Voltage vs Load Current



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Input Current ..... ±15mA
Output Short-Circuit Duration (Note 1) ..... Continuous
Operating Temperature Range ..... –40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

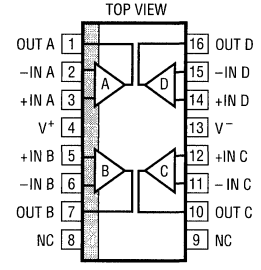


N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 190°C/W (S8)

ORDER PART NUMBER
LT1366CN8 LT1366CS8 LT1368CN8 LT1368CS8
S8 PART MARKING
1366 1368



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1367CS LT1369CS

Consult factory for Industrial and Military parts.

Available Options

PRODUCT NUMBER	NUMBER OF OP AMPS	LOAD CAPACITANCE	MAX V_{OS} (25°C) AT V_S = 5V, 0V	ORDER PART NUMBER	
				PLASTIC (N)	SURFACE MOUNT(S)
LT1366	2	0pF < C_L < 1000pF	475µV	LT1366CN8	LT1366CS8
LT1367	4	0pF < C_L < 1000pF	800µV		LT1367CS
LT1368	2	C_L = 0.1µF	475µV	LT1368CN8	LT1368CS8
LT1369	4	C_L = 0.1µF	800µV		LT1369CS

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V, V_{CM} = 2.5V, V_O = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	V_{CM} = V_{CC} V_{CM} = V_{EE}			150 150	475 475	µV µV
	Input Offset Voltage (LT1367/LT1369)	V_{CM} = V_{CC} V_{CM} = V_{EE}			150 150	800 700	µV µV
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368) Input Offset Voltage Match (Channel to Channel)	V_{CM} = V_{EE} to V_{CC} V_{CM} = V_{EE}, V_{CC} (Notes 4, 5)			150 250	400 700	µV µV
	Input Offset Voltage Shift (LT1367/LT1369) Input Offset Voltage Match (Channel to Channel)	V_{CM} = V_{EE} to V_{CC} V_{CM} = V_{EE}, V_{CC} (Notes 4, 5)			150 250	650 1600	µV µV
I_B	Input Bias Current	V_{CM} = V_{CC} V_{CM} = V_{EE}		0 –35	10 –10	35 0	nA nA
ΔI_B	Input Bias Current Shift	V_{CM} = V_{EE} to V_{CC}			20	70	nA

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = 5V, 0V, V_{CM} = 2.5V, V_O = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OS}	Input Offset Current	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$			1 0.3	6 6	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V_{EE}$ to V_{CC}			1	6	nA
	Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{CC}$ (Note 4) $V_{CM} = V_{EE}$ (Note 4)		0 0	1 1	12 12	nA nA
e_n	Input Noise Voltage Density	f = 1kHz			29		nV/√Hz
i_n	Input Noise Current Density	f = 1kHz			0.07		pA/√Hz
C_{IN}	Input Capacitance				12		pF
A_{VOL}	Large-Signal Voltage Gain	V_O = 50mV to 4.8V, R_L = 10k		500	2000		V/mV
CMRR	Common-Mode Rejection Ratio (LT1366/LT1368) CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} $V_{CM} = V_{EE}$ to V_{CC} (Note 4)		81 75	90 90		dB dB
	Common-Mode Rejection Ratio (LT1367/LT1369) CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} $V_{CM} = V_{EE}$ to V_{CC} (Note 4)		77 71	90 90		dB dB
PSRR	Power Supply Rejection Ratio PSRR Match (Channel to Channel) (Note 4)	V_S = 2.0V to 12V, $V_{CM} = V_O$ = 0.5V V_S = 2.0V to 12V, $V_{CM} = V_O$ = 0.5V		90 84	105 100		dB dB
V_{OL}	Output Voltage Swing LOW	No Load I_{SINK} = 0.5mA I_{SINK} = 2.5mA			6 40 110	12 70 200	mV mV mV
V_{OH}	Output Voltage Swing HIGH	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 2.5mA		V_{CC} – 0.008 V_{CC} – 0.100 V_{CC} – 0.250	V_{CC} – 0.004 V_{CC} – 0.050 V_{CC} – 0.150		V V V
I_{SC}	Short-Circuit Current	(Note 1)		±15	±30		mA
I_S	Supply Current per Amplifier				375	520	µA
GBW	Gain-Bandwidth Product (LT1366/LT1367) Gain-Bandwidth Product (LT1368/LT1369)	A_V = 1000 A_V = 1000			0.4 0.16		MHz MHz
t_S	Settling Time (LT1366/LT1367)	A_V = 1, V_{STEP} = 4V to 0.1%			30		µs

0°C < T_A < 70°C, V_S = 5V, 0V, V_{CM} = 2.5V, V_O = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$	● ●		200 200	575 575	µV µV
	Input Offset Voltage (LT1367/LT1369)	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$	● ●		200 200	950 900	µV µV
V_{OS} TC	Input Offset Voltage Drift	(Note 2)	●		2	6	µV/°C
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368) Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} $V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)	● ●		200 250	425 900	µV µV
	Input Offset Voltage Shift (LT1367/LT1369) Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} $V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)	● ●		200 250	675 1900	µV µV
I_B	Input Bias Current	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$	● ●	0 –45	15 –10	45 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●		25	90	nA
I_{OS}	Input Offset Current	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$	● ●		2 1	15 15	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●		2	15	nA
	Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{CC}$ (Note 4) $V_{CM} = V_{EE}$ (Note 4)	● ●	0 0	2 1	15 15	nA nA

ELECTRICAL CHARACTERISTICS

0°C < T_A < 70°C, V_S = 5V, 0V, V_{CM} = 2.5V, V_O = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	V_O = 50mV to 4.8V, R_L = 10k	●	500	2000		V/mV
CMRR	Common-Mode Rejection Ratio (LT1366/LT1368)	V_{CM} = V_{EE} to V_{CC}	●	80	87		dB
	CMRR Match (Channel to Channel)	V_{CM} = V_{EE} to V_{CC} (Note 4)	●	74	87		dB
	Common-Mode Rejection Ratio (LT1367/LT1369)	V_{CM} = V_{EE} to V_{CC}	●	77	87		dB
	CMRR Match (Channel to Channel)	V_{CM} = V_{EE} to V_{CC} (Note 4)	●	71	87		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.3V to 12V, V_{CM} = V_O = 0.5V	●	88	105		dB
	PSRR Match (Channel to Channel) (Note 4)	V_S = 2.3V to 12V, V_{CM} = V_O = 0.5V	●	82	100		dB
V_{OL}	Output Voltage Swing LOW	No Load	●		9	14	mV
		I_{SINK} = 0.5mA	●		45	80	mV
		I_{SINK} = 2.5mA	●		120	230	mV
V_{OH}	Output Voltage Swing HIGH	No Load	●	V_{CC} – 0.010	V_{CC} – 0.005		V
		I_{SOURCE} = 0.5mA	●	V_{CC} – 0.110	V_{CC} – 0.055		V
		I_{SOURCE} = 2.5mA	●	V_{CC} – 0.300	V_{CC} – 0.180		V
I_{SC}	Short-Circuit Current	(Note 1)	●	±15			mA
I_S	Supply Current per Amplifier		●		360	540	µA

–40°C < T_A < 85°C (Note 3), V_S = 5V, 0V, V_{CM} = 2.5V, V_O = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	V_{CM} = V_{CC}	●		250	900	µV
		V_{CM} = V_{EE}	●		200	750	µV
	Input Offset Voltage (LT1367/LT1369)	V_{CM} = V_{CC}	●		250	1150	µV
		V_{CM} = V_{EE}	●		200	1000	µV
V_{OS} TC	Input Offset Voltage Drift	(Note 2)	●		2	6	µV/°C
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368)	V_{CM} = V_{EE} to V_{CC}	●		200	650	µV
	Input Offset Voltage Match (Channel to Channel)	V_{CM} = V_{EE}, V_{CC} (Notes 4, 5)	●		250	1800	µV
	Input Offset Voltage Shift (LT1367/LT1369)	V_{CM} = V_{EE} to V_{CC}	●		200	725	µV
	Input Offset Voltage Match (Channel to Channel)	V_{CM} = V_{EE}, V_{CC} (Notes 4, 5)	●		250	2300	µV
I_B	Input Bias Current	V_{CM} = V_{CC}	●	0	45	80	nA
		V_{CM} = V_{EE}	●	–45	–10	0	nA
ΔI_B	Input Bias Current Shift	V_{CM} = V_{EE} to V_{CC}	●		55	125	nA
I_{OS}	Input Offset Current	V_{CM} = V_{CC}	●		4	30	nA
		V_{CM} = V_{EE}	●		1	20	nA
ΔI_{OS}	Input Offset Current Shift	V_{CM} = V_{EE} to V_{CC}	●		4	30	nA
	Input Bias Current Match (Channel to Channel)	V_{CM} = V_{CC} (Note 4)	●	0	4	30	nA
		V_{CM} = V_{EE} (Note 4)	●	0	1	20	nA
A_{VOL}	Large Signal Voltage Gain	V_O = 50mV to 4.8V, R_L = 10k	●	400	2000		V/mV
CMRR	Common-Mode Rejection Ratio (LT1366/LT1368)	V_{CM} = V_{EE} to V_{CC}	●	77	87		dB
	CMRR Match (Channel to Channel)	V_{CM} = V_{EE} to V_{CC} (Note 4)	●	71	87		dB
	Common-Mode Rejection Ratio (LT1367/LT1369)	V_{CM} = V_{EE} to V_{CC}	●	76	87		dB
	CMRR Match (Channel to Channel)	V_{CM} = V_{EE} to V_{CC} (Note 4)	●	70	87		dB
PSRR	Power Supply Rejection Ratio	V_S = 2.3V to 12V, V_{CM} = V_O = 0.5V	●	88	105		dB
	PSRR Match (Channel to Channel) (Note 4)	V_S = 2.3V to 12V, V_{CM} = V_O = 0.5V	●	82	100		dB
V_{OL}	Output Voltage Swing LOW	No Load	●		9	20	mV
		I_{SINK} = 0.5mA	●		45	80	mV
		I_{SINK} = 2.5mA	●		130	230	mV

ELECTRICAL CHARACTERISTICS

$-40°C < T_A < 85°C$ (Note 3), $V_S = 5V, 0V$, $V_{CM} = 2.5V$, $V_O = 2.5V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	Output Voltage Swing HIGH	No Load	●	$V_{CC} - 0.015$	$V_{CC} - 0.006$		V
		$I_{SOURCE} = 0.5mA$	●	$V_{CC} - 0.110$	$V_{CC} - 0.055$		V
		$I_{SOURCE} = 2.5mA$	●	$V_{CC} - 0.300$	$V_{CC} - 0.190$		V
I_{SC}	Short-Circuit Current	(Note 1)	●	±12			mA
I_S	Supply Current per Amplifier		●		375	575	µA

$T_A = 25°C$, $V_S = 3V, 0V$, $V_{CM} = 1.5V$, $V_O = 1.5V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	$V_{CM} = V_{CC}$			150	475	µV
		$V_{CM} = V_{EE}$			150	475	µV
	Input Offset Voltage (LT1367/LT1369)	$V_{CM} = V_{CC}$			150	850	µV
		$V_{CM} = V_{EE}$			150	750	µV
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}			150	400	µV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)			250	700	µV
	Input Offset Voltage Shift (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}			150	650	µV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)			250	1700	µV
I_B	Input Bias Current	$V_{CM} = V_{CC}$		0	10	35	nA
		$V_{CM} = V_{EE}$		−35	−10	0	nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V_{EE}$ to V_{CC}			20	70	nA
I_{OS}	Input Offset Current	$V_{CM} = V_{CC}$			1.0	6	nA
		$V_{CM} = V_{EE}$			0.3	6	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V_{EE}$ to V_{CC}			1	6	nA
	Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{CC}$ (Note 4)		0	1	12	nA
		$V_{CM} = V_{EE}$ (Note 4)		0	1	12	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = 50mV$ to $2.8V$, $R_L = 10k$		500	1500		V/mV
CMRR	Common-Mode Rejection Ratio (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}		77	86		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 4)		71	86		dB
	Common-Mode Rejection Ratio (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}		73	86		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 4)		67	86		dB
V_{OL}	Output Voltage Swing LOW	No Load			6	12	mV
		$I_{SINK} = 0.5mA$			40	70	mV
		$I_{SINK} = 2.5mA$			110	200	mV
V_{OH}	Output Voltage Swing HIGH	No Load		$V_{CC} - 0.008$	$V_{CC} - 0.004$		V
		$I_{SOURCE} = 0.5mA$		$V_{CC} - 0.100$	$V_{CC} - 0.050$		V
		$I_{SOURCE} = 2.5mA$		$V_{CC} - 0.250$	$V_{CC} - 0.150$		V
I_{SC}	Short-Circuit Current	(Note 1)		±10	±20		mA
I_S	Supply Current per Amplifier				350	500	µA

$0°C < T_A < 70°C$, $V_S = 3V, 0V$, $V_{CM} = 1.5V$, $V_O = 1.5V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	$V_{CM} = V_{CC}$	●		200	575	µV
		$V_{CM} = V_{EE}$	●		200	575	µV
	Input Offset Voltage (LT1367/LT1369)	$V_{CM} = V_{CC}$	●		200	950	µV
		$V_{CM} = V_{EE}$	●		200	900	µV

ELECTRICAL CHARACTERISTICS

0°C < T_A < 70°C, V_S = 3V, 0V, V_{CM} = 1.5V, V_O = 1.5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}	●		200	425	µV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)	●		250	900	µV
	Input Offset Voltage Shift (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}	●		200	675	µV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)	●		250	1900	µV
V_{OS} TC	Input Offset Voltage Drift	(Note 2)	●		2	6	µV/°C
I_B	Input Bias Current	$V_{CM} = V_{CC}$	●	0	15	45	nA
		$V_{CM} = V_{EE}$	●	–45	–10	0	nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●		25	90	nA
I_{OS}	Input Offset Current	$V_{CM} = V_{CC}$	●		2	15	nA
		$V_{CM} = V_{EE}$	●		1	15	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●		2	15	nA
	Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{CC}$ (Note 4)	●	0	2	15	nA
		$V_{CM} = V_{EE}$ (Note 4)	●	0	1	15	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = 50mV to 2.8V, R_L = 10k	●	300	1500		V/mV
CMRR	Common-Mode Rejection Ratio (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}	●	76	83		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 4)	●	70	83		dB
	Common-Mode Rejection Ratio (LT1367 /LT1369)	$V_{CM} = V_{EE}$ to V_{CC}	●	72	83		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 4)	●	66	83		dB
V_{OL}	Output Voltage Swing LOW	No Load	●		9	14	mV
		I_{SINK} = 0.5mA	●		45	80	mV
		I_{SINK} = 2.5mA	●		120	230	mV
V_{OH}	Output Voltage Swing HIGH	No Load	●	V_{CC} – 0.010	V_{CC} – 0.005		V
		I_{SOURCE} = 0.5mA	●	V_{CC} – 0.110	V_{CC} – 0.055		V
		I_{SOURCE} = 2.5mA	●	V_{CC} – 0.300	V_{CC} – 0.180		V
I_{SC}	Short-Circuit Current	(Note 1)	●	±10			mA
I_S	Supply Current per Amplifier		●		350	520	µA

–40°C < T_A < 85°C (Note 3), V_S = 3V, 0V, V_{CM} = 1.5V, V_O = 1.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	$V_{CM} = V_{CC}$	●		250	900	µV
		$V_{CM} = V_{EE}$	●		200	750	µV
	Input Offset Voltage (LT1367/LT1369)	$V_{CM} = V_{CC}$	●		250	1200	µV
		$V_{CM} = V_{EE}$	●		200	1000	µV
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}	●		200	650	µV
	Input Offset Voltage Match (Channel to Channel)	$Vx_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)	●		250	1800	µV
	Input Offset Voltage Shift (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}	●		200	775	µV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)	●		250	2400	µV
V_{OS} TC	Input Offset Voltage Drift	(Note 2)	●		2	6	µV/°C
B	Input Bias Current	$V_{CM} = V_{CC}$	●	0	45	80	nA
		$V_{CM} = V_{EE}$	●	–45	–10	0	nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●		55	125	nA
OS	Input Offset Current	$V_{CM} = V_{CC}$	●		4	30	nA
		$V_{CM} = V_{EE}$	●		1	20	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●		4	30	nA
	Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{CC}$ (Note 4)	●	0	4	30	nA
		$V_{CM} = V_{EE}$ (Note 4)	●	0	1	20	nA

ELECTRICAL CHARACTERISTICS

$-40°C < T_A < 85°C$ (Note 3), $V_S = 3V, 0V$, $V_{CM} = 1.5V$, $V_O = 1.5V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
A_{VOL}	Large-Signal Voltage Gain	V_O = 50mV to 2.8V, R_L = 10k	●	250	1000		V/mV
CMRR	Common-Mode Rejection Ratio (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}	●	73	83		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 4)	●	67	83		dB
	Common-Mode Rejection Ratio (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}	●	71	83		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 4)	●	65	83		dB
V_{OL}	Output Voltage Swing LOW	No Load	●		9	20	mV
		I_{SINK} = 0.5mA	●		45	80	mV
		I_{SINK} = 2.5mA	●		130	230	mV
V_{OH}	Output Voltage Swing HIGH	No Load	●	V_{CC} – 0.015	V_{CC} – 0.006		V
		I_{SOURCE} = 0.5mA	●	V_{CC} – 0.110	V_{CC} – 0.055		V
		I_{SOURCE} = 2.5mA	●	V_{CC} – 0.300	V_{CC} – 0.190		V
I_{SC}	Short-Circuit Current	(Note 1)	●	±10			mA
I_S	Supply Current per Amplifier		●		350	550	µA

$T_A = 25°C$, $V_S = \pm 15V$, $V_{CM} = 0V$, $V_O = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	$V_{CM} = V_{CC}$			200	700	µV
		$V_{CM} = V_{EE}$			200	700	µV
	Input Offset Voltage (LT1367/LT1369)	$V_{CM} = V_{CC}$			200	1000	µV
		$V_{CM} = V_{EE}$			200	900	µV
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}			150	500	µV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)			300	1300	µV
	Input Offset Voltage Shift (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}			150	650	µV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)			300	2000	µV
I_B	Input Bias Current	$V_{CM} = V_{CC}$		0	10	35	nA
		$V_{CM} = V_{EE}$		–35	–10	0	nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V_{EE}$ to V_{CC}			20	70	nA
I_{OS}	Input Offset Current	$V_{CM} = V_{CC}$			1.0	6	nA
		$V_{CM} = V_{EE}$			0.3	6	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V_{EE}$ to V_{CC}			1	6	nA
	Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{CC}$ (Note 4)		0	1	12	nA
		$V_{CM} = V_{EE}$ (Note 4)		0	1	12	nA
C_{IN}	Input Capacitance				7.1		pF
A_{VOL}	Large-Signal Voltage Gain	V_O = –14.7V to 14.7V, R_L = 10k		2000	10000		V/mV
		V_O = –10V to 10V, R_L = 2k		1000	10000		V/mV
	Channel Separation	V_O = –10V to 10V, R_L = 2k		120	135		dB
SR	Slew Rate (LT1366/LT1367)	A_V = –1, R_L = Open, V_O = ±10V, Measured at V_O = ±5V			0.13		V/µs
	Slew Rate (LT1368/LT1369)	A_V = –1, R_L = Open, V_O = ±10V, Measured at V_O = ±5V			0.065		V/µs
CMRR	Common-Mode Rejection Ratio (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}		95	106		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 4)		89	106		dB
	Common-Mode Rejection Ratio (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}		93	106		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 4)		87	106		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V		90	110		dB
	PSRR Match (Channel to Channel)	V_S = ±5V to ±15V (Note 4)		84	105		dB

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_S = ±15V, V_{CM} = 0V, V_O = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Output Voltage Swing LOW	No Load I_{SINK} = 0.5mA I_{SINK} = 10mA			V_{EE} + 0.006 V_{EE} + 0.040 V_{EE} + 0.240	V_{EE} + 0.012 V_{EE} + 0.070 V_{EE} + 0.500	V V V
V_{OH}	Output Voltage Swing HIGH	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 10mA		V_{CC} – 0.008 V_{CC} – 0.100 V_{CC} – 0.800	V_{CC} – 0.004 V_{CC} – 0.050 V_{CC} – 0.400		V V V
I_{SC}	Short-Circuit Current	(Note 1)		±30	±75		mA
I_S	Supply Current per Amplifier				385	550	µA

0°C < T_A < 70°C, V_S = ±15V, V_{CM} = 0V, V_O = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$	● ●		250 250	850 850	µV µV
	Input Offset Voltage (LT1367/LT1369)	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$	● ●		250 250	1150 1000	µV µV
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368) Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} $V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)	● ●		200 300	525 1500	µV µV
	Input Offset Voltage Shift (LT1367/LT1369) Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} $V_{CM} = V_{EE}$, V_{CC} (Note 4, 5)	● ●		200 300	750 2300	µV µV
V_{OS} TC	Input Offset Voltage Drift	(Note 2)	●		2	8	µV/°C
I_B	Input Bias Current	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$	● ●	0 –45	15 –10	45 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●		25	90	nA
I_{OS}	Input Offset Current	$V_{CM} = V_{CC}$ $V_{CM} = V_{EE}$	● ●		2 1	15 15	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●		2	15	nA
	Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{CC}$ (Note 4) $V_{CM} = V_{EE}$ (Note 4)	● ●	0 0	2 1	15 15	nA nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –14.7V to 14.7V, R_L = 10k V_O = –10V to 10V, R_L = 2k	● ●	1500 1000	6000 6000		V/mV V/mV
	Channel Separation	V_O = –10V to 10V, R_L = 2k	●	110	135		dB
CMRR	Common-Mode Rejection Ratio (LT1366/LT1368) CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} $V_{CM} = V_{EE}$ to V_{CC} (Note 4)	● ●	95 89	103 103		dB dB
	Common-Mode Rejection Ratio (LT1367/LT1369) CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} $V_{CM} = V_{EE}$ to V_{CC} (Note 4)	● ●	92 86	103 103		dB dB
PSRR	Power Supply Rejection Ratio PSRR Match (Channel to Channel)	V_S = ±5V to ±15V V_S = ±5V to ±15V (Note 4)	● ●	80 75	105 100		dB dB
V_{OL}	Output Voltage Swing LOW	No Load I_{SINK} = 0.5mA I_{SINK} = 10mA	● ● ●		V_{EE} + 0.009 V_{EE} + 0.045 V_{EE} + 0.300	V_{EE} + 0.014 V_{EE} + 0.080 V_{EE} + 0.600	V V V
V_{OH}	Output Voltage Swing HIGH	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 10mA	● ● ●	V_{CC} – 0.01 V_{CC} – 0.11 V_{CC} – 0.95	V_{CC} – 0.005 V_{CC} – 0.055 V_{CC} – 0.500		V V V
I_{SC}	Short-Circuit Current	(Note 1)		±30			mA
I_S	Supply Current per Amplifier				360	575	µA

ELECTRICAL CHARACTERISTICS

$-40°C < T_A < 85°C$ (Note 3), $V_S = \pm 15V$, $V_{CM} = 0V$, $V_O = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage (LT1366/LT1368)	$V_{CM} = V_{CC}$	●		250	1000	µV
		$V_{CM} = V_{EE}$	●		250	1000	µV
	Input Offset Voltage (LT1367/LT1369)	$V_{CM} = V_{CC}$	●		250	1350	µV
		$V_{CM} = V_{EE}$	●		250	1200	µV
ΔV_{OS}	Input Offset Voltage Shift (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}	●		200	700	µV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)	●		300	2000	µV
	Input Offset Voltage Shift (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}	●		200	800	µV
	Input Offset Voltage Match (Channel to Channel)	$V_{CM} = V_{EE}$, V_{CC} (Notes 4, 5)	●		300	2700	µV
V_{OS} TC	Input Offset Voltage Drift	(Note 2)	●		2	8	µV/°C
I_B	Input Bias Current	$V_{CM} = V_{CC}$	●	0	45	80	nA
		$V_{CM} = V_{EE}$	●	–45	–10	0	nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●		55	125	nA
I_{OS}	Input Offset Current	$V_{CM} = V_{CC}$	●		4	30	nA
		$V_{CM} = V_{EE}$	●		1	20	nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V_{EE}$ to V_{CC}	●		4	30	nA
	Input Bias Current Match (Channel to Channel)	$V_{CM} = V_{CC}$ (Note 4)	●	0	4	30	nA
		$V_{CM} = V_{EE}$ (Note 4)	●	0	1	20	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = -14.7V$ to $14.7V$, $R_L = 10k$	●	1000	6000		V/mV
		$V_O = -10V$ to $10V$, $R_L = 2k$	●	800	6000		V/mV
	Channel Separation	$V_O = -10V$ to $10V$, $R_L = 2k$	●	110	130		dB
CMRR	Common-Mode Rejection Ratio (LT1366/LT1368)	$V_{CM} = V_{EE}$ to V_{CC}	●	92	103		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 4)	●	86	103		dB
	Common-Mode Rejection Ratio (LT1367/LT1369)	$V_{CM} = V_{EE}$ to V_{CC}	●	91	103		dB
	CMRR Match (Channel to Channel)	$V_{CM} = V_{EE}$ to V_{CC} (Note 4)	●	85	103		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 5V$ to $\pm 15V$	●	80	105		dB
	PSRR Match (Channel to Channel)	$V_S = \pm 5V$ to $\pm 15V$ (Note 4)	●	75	100		dB
V_{OL}	Output Voltage Swing LOW	No Load	●		$V_{EE} + 0.009$	$V_{EE} + 0.020$	V
		$I_{SINK} = 0.5mA$	●		$V_{EE} + 0.045$	$V_{EE} + 0.080$	V
		$I_{SINK} = 10mA$	●		$V_{EE} + 0.300$	$V_{EE} + 0.600$	V
V_{OH}	Output Voltage Swing HIGH	No Load	●	$V_{CC} - 0.015$	$V_{CC} - 0.006$		V
		$I_{SOURCE} = 0.5mA$	●	$V_{CC} - 0.110$	$V_{CC} - 0.055$		V
		$I_{SOURCE} = 10mA$	●	$V_{CC} - 1.100$	$V_{CC} - 0.550$		V
I_{SC}	Short-Circuit Current	(Note 1)		±30			mA
I_S	Supply Current per Amplifier				385	600	µA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: Applies to short circuits to ground for all split supplies and for single supplies less than 20V. Short circuits to either supply for supplies greater than 20V total may permanently damage the part. A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 2: This parameter is not 100% tested.

Note 3: At –40°C and 85°C, the LT1366, LT1367, LT1368, and LT1369 are neither tested nor quality assurance sampled. The specifications indicated are guaranteed by design; correlated, and/or inferred from the 0°C, 25°C, and 70°C tests.

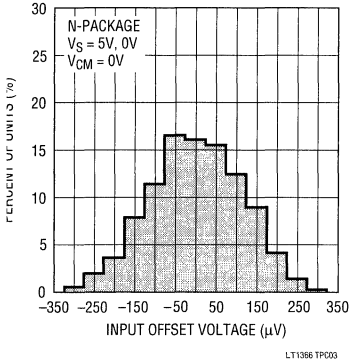
Note 4: Matching parameters are the difference between amplifiers A and D and between B and C on the LT1367/LT1369; between the two amplifiers on the LT1366/LT1368.

Note 5: Input offset voltage match is the difference in offset voltage between amplifiers measured at both $V_{CM} = V_{EE}$ and $V_{CM} = V_{CC}$.

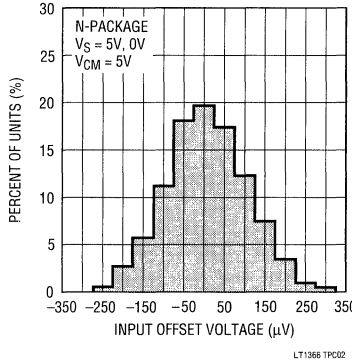
TYPICAL PERFORMANCE CHARACTERISTICS

The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)

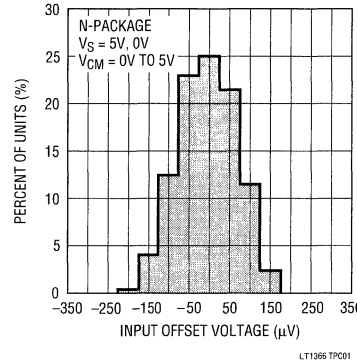
PNP Stage V_{OS} Distribution (LT1366/LT1368)



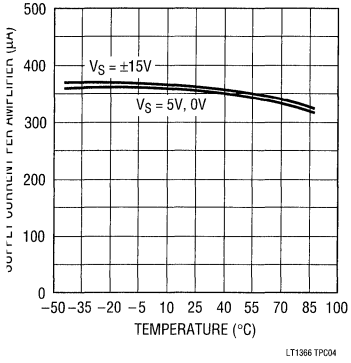
NPN Stage V_{OS} Distribution (LT1366/LT1368)



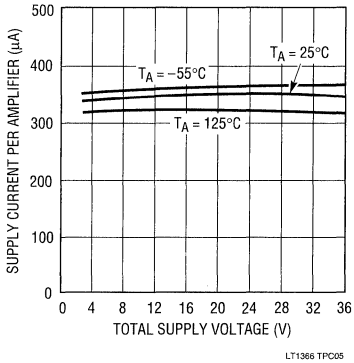
ΔV_{OS}-Shift Between PNP and NPN Stages (LT1366/LT1368)



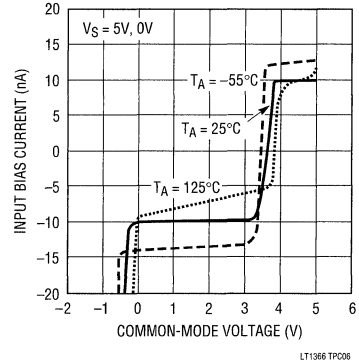
Supply Current vs Temperature



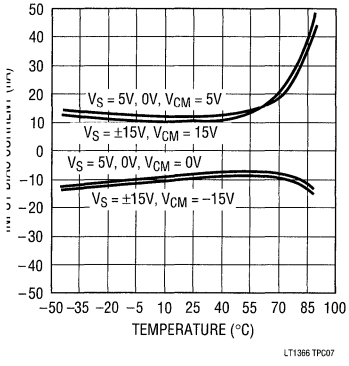
Supply Current vs Supply Voltage



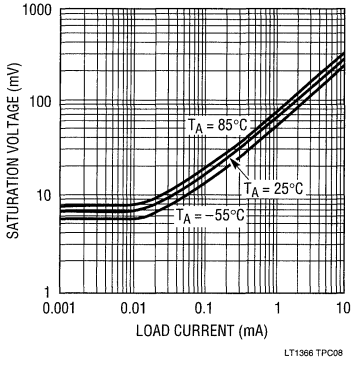
Input Bias Current vs Common-Mode Voltage



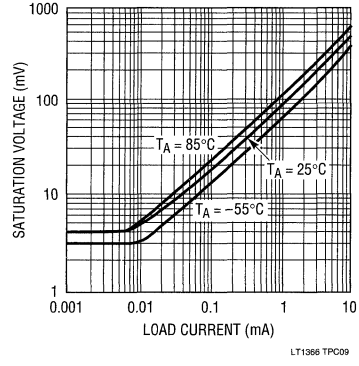
Input Bias Current vs Temperature



Output Saturation Voltage vs Load Current (Output HIGH)



Output Saturation Voltage vs Load Current (Output LOW)

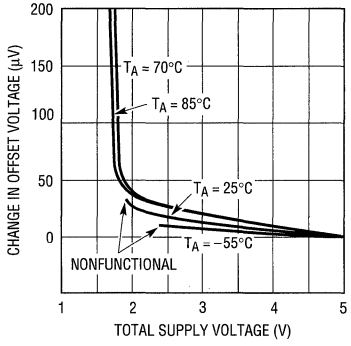


2

TYPICAL PERFORMANCE CHARACTERISTICS

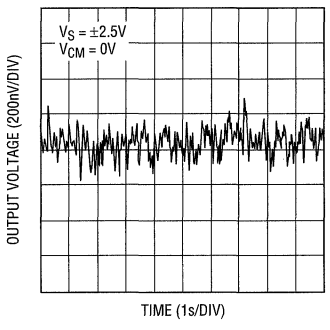
(The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)

Minimum Supply Voltage



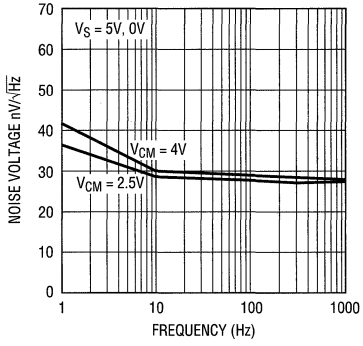
LT1366 TPC10

0.1Hz to 10Hz Output Voltage Noise



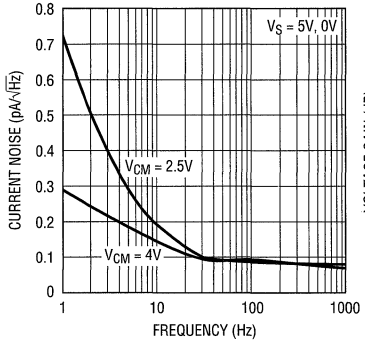
LT1366 TPC11

Noise Voltage Spectrum



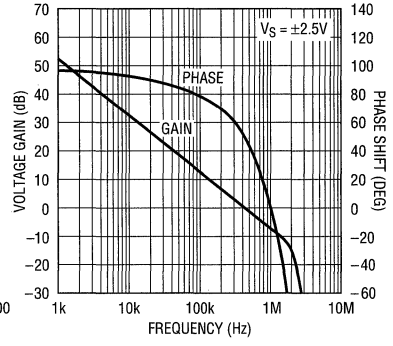
LT1366 TPC12

Noise Current Spectrum



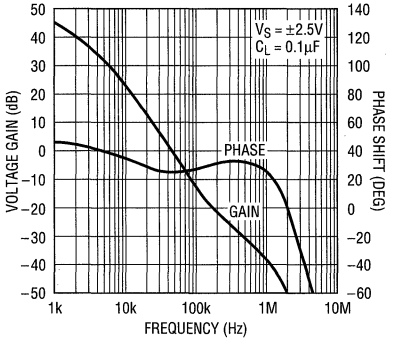
LT1366 TPC13

Gain and Phase Shift vs Frequency (LT1366/LT1367)



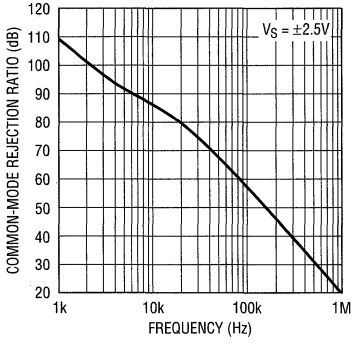
LT1366 TPC14

Gain and Phase Shift vs Frequency (LT1368/LT1369)



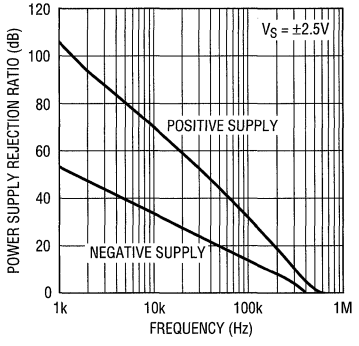
LT1366 TPC15

CMRR vs Frequency (LT1366 and LT1367)



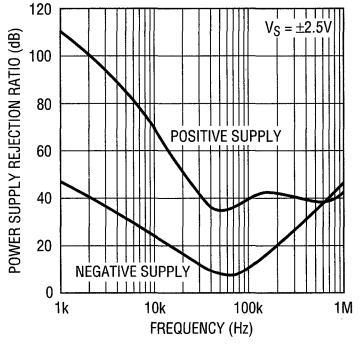
LT1366 TPC16

PSRR vs Frequency (LT1366/LT1367)



LT1366 TPC17

PSRR vs Frequency (LT1368/LT1369)

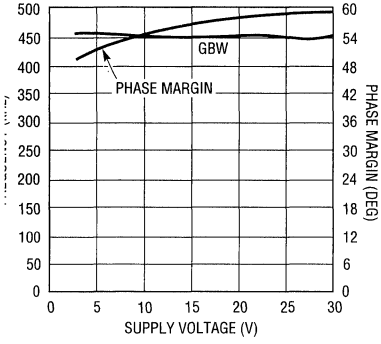


LT1366 TPC18

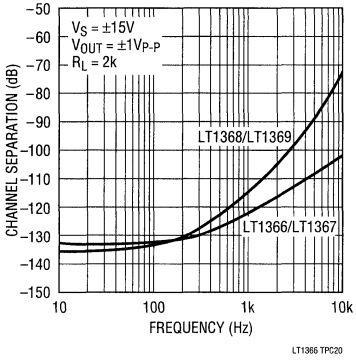
TYPICAL PERFORMANCE CHARACTERISTICS

The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)

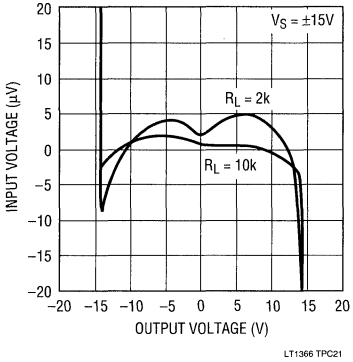
Gain-Bandwidth and Phase Margin vs Supply Voltage (LT1366/LT1367)



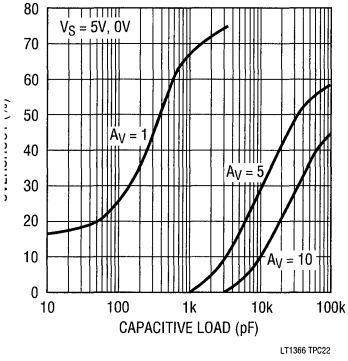
Channel Separation vs Frequency



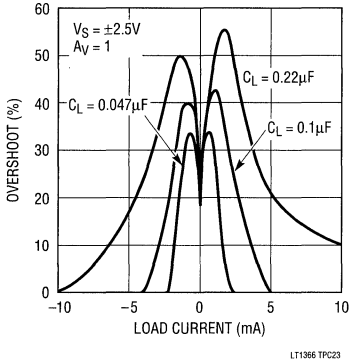
Open-Loop Gain



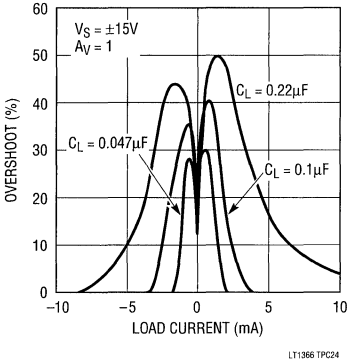
Capacitive Load Handling (LT1366/LT1367)



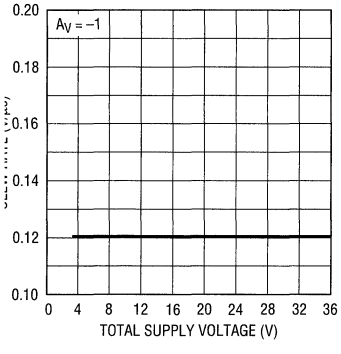
Overshoot vs Load Current (LT1368/LT1369)



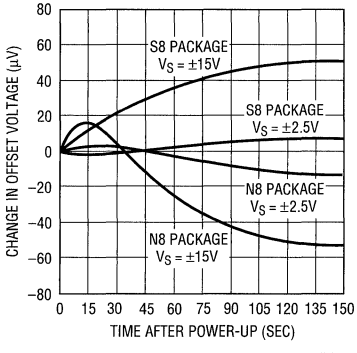
Overshoot vs Load Current (LT1368/LT1369)



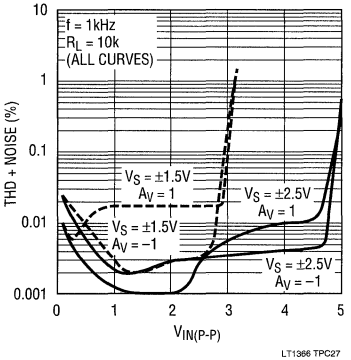
Slew Rate vs Supply Voltage



Warm-Up Drift vs Time



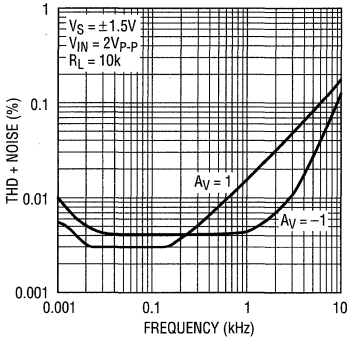
THD + Noise vs Peak-to-Peak Voltage



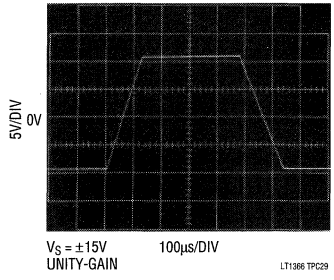
TYPICAL PERFORMANCE CHARACTERISTICS

(The data presented here applies to the LT1366/LT1367/LT1368/LT1369 unless otherwise noted.)

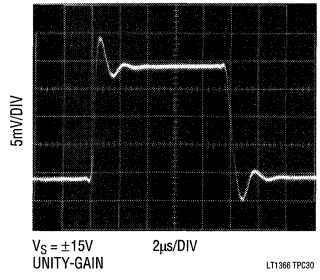
THD + Noise vs Frequency



Large-Signal Response (LT1366/LT1367)



Small-Signal Response (LT1366/LT1367)



APPLICATIONS INFORMATION

Rail-to-Rail Operation

The LT1366 family differs from conventional op amps in the design of both the input and output stages. Figure 1 shows a simplified schematic of the amplifier. The input stage consists of two differential amplifiers, a PNP stage Q1/Q2 and an NPN stage Q3/Q4, which are active over different portions of the input common-mode range. Lateral devices are used in both input stages, eliminating the need for clamps across the input pins. Each input stage is trimmed for offset voltage. A complementary output configuration (Q23 through Q26) is employed to create an output stage with rail-to-rail swing. The amplifier is fabri-

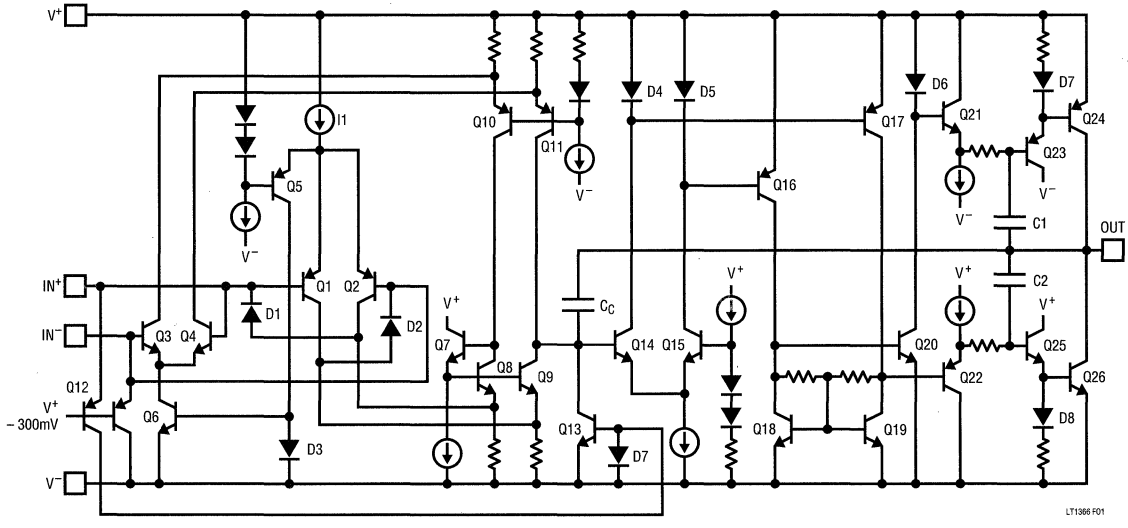


Figure 1. LT1366 Simplified Schematic Diagram

IPPLICATIONS INFORMATION

ated on Linear Technology's proprietary complementary ipolar process, which ensures very similar DC and AC haracteristics for the output devices Q24 and Q26.

simple comparator Q5 steers current from current ource I1 between the two input stages. When the input ommon-mode voltage V_{CM} is near the negative supply, 5 is reverse biased, and I1 becomes the tail current for ie PNP differential pair Q1/Q2. At the other extreme, hen V_{CM} is within about 1.3V from the positive supply, 5 diverts I1 to the current mirror D3/Q6, which furnishes ie tail current for the NPN differential pair Q3/Q4.

he collector currents of the two input pairs are combined the second stage, consisting of Q7 through Q11. Most f the voltage gain in the amplifier is contained in this age. Differential amplifier Q14/Q15 buffers the output of ie second stage, converting the output voltage to differ- ntial currents. The differential currents pass through urrent mirrors D4/Q17 and D5/Q16, and are converted to fferential voltages by Q18 and Q19. These voltages are so buffered and applied to the output Darlington pairs 23/Q24 and Q25/Q26. Capacitors C1 and C2 form local edback loops around the output devices, lowering the utput impedance at high frequencies.

put Offset Voltage

ince the amplifier has two input stages, the input offset oltage changes depending upon which stage is active. ie input offsets are random, but bounded voltages. hen the amplifier switches between stages, offset volt- ges may go up, down, or remain flat; but will not exceed e guaranteed limits. This behavior is illustrated in three stribution plots of input offset voltage in the Typical erformance Characteristics section.

verdrive Protection

wo circuits prevent the output from reversing polarity hen the input voltage exceeds the common-mode range. hen the noninverting input exceeds the positive supply approximately 300mV, the clamp transistor Q12 (Fig- e 1) turns on, pulling the output of the second stage low, hich forces the output high. For inputs below the nega- ve supply, diodes D1 and D2 turn on, overcoming the turation of the input pair Q1/Q2.

When overdriven, the amplifier draws input current that exceeds the normal input bias current. Figures 2 and 3 show some typical overdrive currents as a function of input voltage. The input current must be less than 1mA of positive overdrive or less than 7mA of negative overdrive, for the phase reversal protection to work properly. When the amplifier is severely overdriven, an external resistor should be used to limit the overdrive current. In addition to overdrive protection, the amplifier is protected against ESD strokes up to 4kV on all pins.

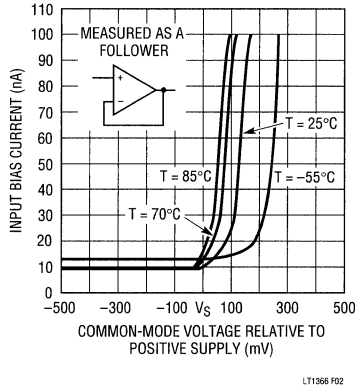


Figure 2. Input Bias Current vs Common-Mode Voltage

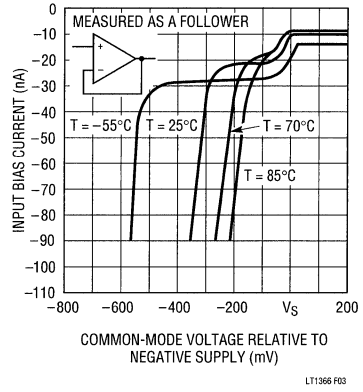


Figure 3. Input Bias Current vs Common-Mode Voltage

APPLICATIONS INFORMATION

Improved Supply Rejection in the LT1368/LT1369

The LT1368/LT1369 are variations of the LT1366/LT1367 offering greater supply rejection and lower high frequency output impedance. The LT1368/LT1369 require a 0.1µF load capacitance for compensation. The output capacitance forms a filter, which reduces pickup from the supply and lowers the output impedance. This additional filtering is helpful in mixed analog/digital systems with common supplies, or systems employing switching supplies. Filtering also reduces high frequency noise, which may be beneficial when driving A/D converters.

Figure 4 shows the outputs of the LT1366/LT1368 perturbed by a 200mV$_{P-P}$ 50kHz square wave added to the positive supply. The LT1368's power supply rejection is about ten times greater than that of the LT1366 at 50kHz. Note the 5-to-1 scale change in the output voltage traces.

The tolerance of the external compensation capacitor is not critical. The plots of Overshoot vs Load Current in the Typical Performance Characteristics section illustrate the effect of a capacitive load.

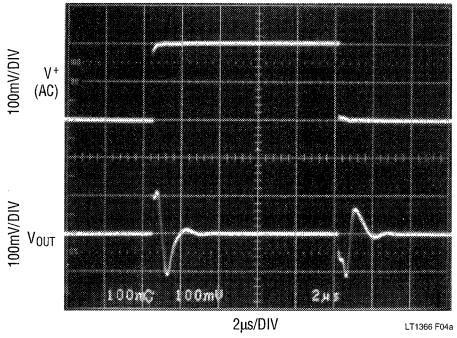


Figure 4a. LT1366 Power Supply Rejection Test

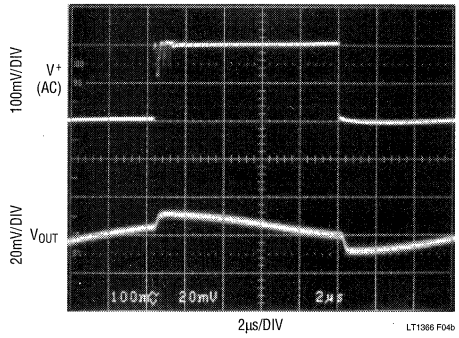


Figure 4b. LT1368 Power Supply Rejection Test

TYPICAL APPLICATIONS

Buffering A/D Converters

Figure 5 shows the LT1368 driving an LTC®1288 two-channel micropower A/D Converter (ADC). The LTC1288 can accommodate voltage references and input signals equal to the supply rails. The sampling nature of this ADC eliminates the need for an external sample-and-hold, but may call for a drive amplifier because of the ADC's 12µs settling requirement. The LT1368's rail-to-rail operation and low input offset voltage make it well-suited for low power, low frequency A/D applications. Either the LT1366 or LT1368 could be used for this application. However, for low frequencies (f < 1kHz) the LT1368 provides better supply rejection.

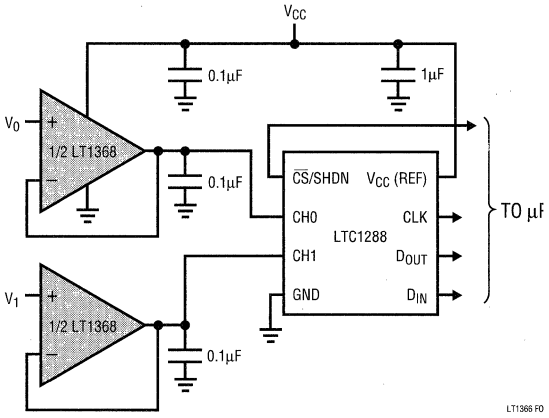


Figure 5. Two-Channel Low Power A/D Converter

YPICAL APPLICATIONS

ecision Low Dropout Regulator

croprocessors and complex digital circuits frequently ecify tight control of power supply characteristics. The cuit shown in Figure 6 provides a precise 3.6V, 1A tput from a minimum 3.8V input voltage. The circuit's minal operating voltage is 4.75V ±5%. The voltage erence and resistor ratios determine output voltage curacy, while the LT1366's high gain enforces 0.2% line d load regulation. Quiescent current is about 1mA and es not change appreciably with supply or load. All mponents are available in surface mount packages.

e regulator's main loop consists of A1 and a logic level T, Q1. The output is fed back to the op amp's positive ıut because of the phase inversion through Q1. The ıulator's frequency response is limited by Q1's roll-off d the phase lead introduced by the output capacitor's ective series resistance (ESR). Two pole-zero networks mpensate for these effects. The pole formed with R5 d C2 rolls off the gain set with the feedback network, ile the pole formed with R7 and C3 rolls off A1's gain ectly, which is the dominant influence on settling time. e zeros formed with R6 and C2, and R8 and C3 provide ase boost near the unity-gain crossover, which increases the regulator's phase margin. Although not directly part of the compensation, R9 decouples the op amp's output from Q1's large gate capacitance.

A second loop provides a foldback current limit. A2 compares the sense voltage across R1 with 50mV referenced to the positive rail. When the sense voltage exceeds the reference, A2's output drives Q1's gate positive via A1. In current limit, the output voltage collapses and the current limit LED (D1) turns on causing about 30mV to drop across R3. A2 regulates Q1's drain current so that the deficit between the 50mV reference and the voltage across R3 is made up across the sense resistor. The reduced sense voltage is 20mV, which sets the current limit to about 400mA. As the supply voltage increases, the voltage across R3 increases, and the current limit folds back to a lower level. The current limit loop deactivates when the load current drops below the regulated output current. When the supply turns on rapidly, C1 bypasses the fold back circuit allowing the regulator to start-up into a heavy load.

Q1 does not require a heat sink. When mounted on a type FR4 PC board, Q1 has a thermal resistance of 50°C/W. At 1.4W worst case dissipation, Q1 can operate up to 80°C.

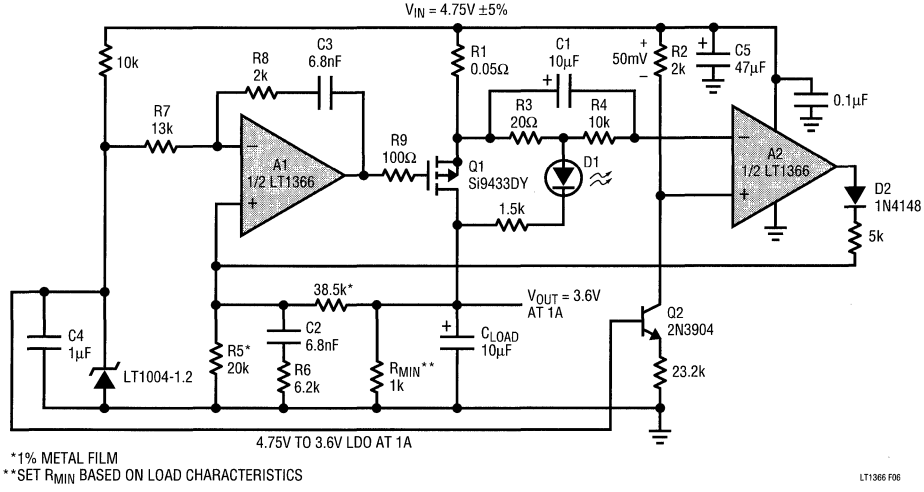


Figure 6. Precision 3.6V, 1A Low Dropout Regulator

TYPICAL APPLICATIONS

High-Side Current Source

The wide-compliance current source shown in Figure 7 takes advantage of the LT1366's ability to measure small signals near the positive supply rail. The LT1366 adjusts Q1's gate voltage to force the voltage across the sense resistor (R_{SENSE}) to equal the voltage from the supply to the potentiometer's wiper. A rail-to-rail op amp is needed because the voltage across the sense resistor must drop to zero when the divided reference voltage is set to zero. Q2 acts as a constant current sink to minimize error in the reference voltage when the supply voltage varies.

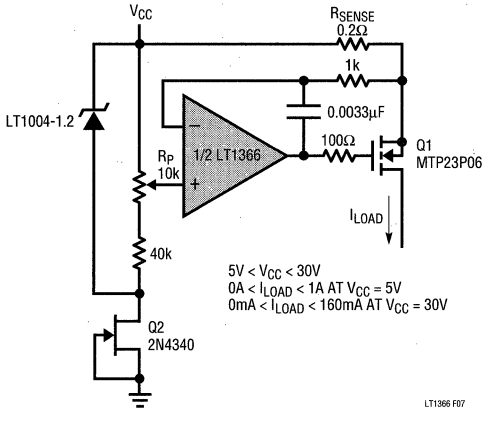


Figure 7. High-Side Current Source

The circuit can operate over a wide supply range (5V < V_{CC} < 30V). At low input voltage, circuit operation is limited by the MOSFET's gate drive requirements. At high input voltage, circuit operation is limited by the LT1366's absc lute maximum ratings and the output power require ments.

The circuit delivers 1A at 200mV of sense voltage. With 5V input supply, the power dissipation is 5W. For opera tion at 70°C ambient temperature, the MOSFET's heat sin must have a thermal resistance of:

$$\theta_{HS} = \theta_{JA\ SYSTEM} - \theta_{JC\ FET}$$
$$= (125°C - 70°C)/5W - 1.25°C/W$$
$$= 11°C/W - 1.25°C/W$$
$$= 9.75°C/W$$

which is easily achievable with a small heat sink. Inpu voltages greater than 5V require the use of a larger hea sink or a reduction of the output current.

The circuit's supply regulation is about 0.03%/V. Th output impedance is equal to the MOSFET's output imped ance multiplied by the op amp's open-loop gain. Degrada tions in current-source compliance occur when the volt age across the MOSFET's on-resistance and the sens resistor drops below the voltage required to maintain th desired output current. This condition occurs when [V_C – V_{OUT}] < [I_{LOAD} × (R_{SENSE} + R_{ON})].

Single Supply, 1kHz, 4th Order Butterworth Filter

An LT1367 is used in Figure 8 to form a 4th orde Butterworth filter. The filter is a simplified state variabl architecture consisting of two cascaded 2nd order sec tions. Each section uses the 360 degree phase shift aroun

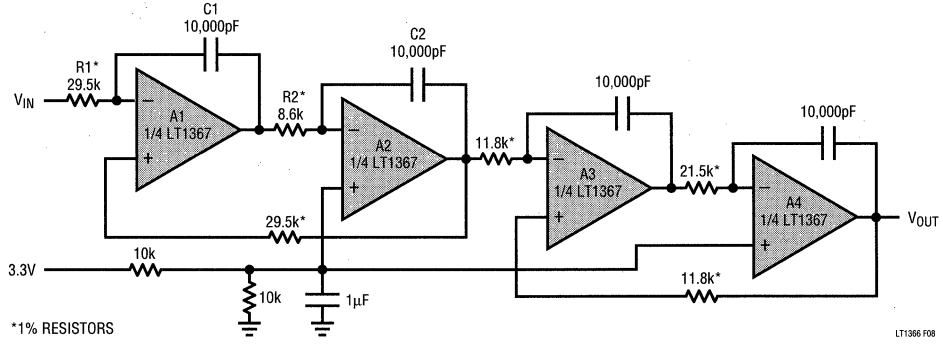


Figure 8. Four-Pole 1kHz, 3.3V Single Supply, State Variable Filter Using the LT1367

TYPICAL APPLICATIONS

:he 2 op amp loop to create a negative summing junction
it A1's positive input[1]. The circuit has low sensitivities for
:enter frequency and Q, which are set with the following
:quations:

$$\omega_0^2 = 1/(R1 \times C1 \times R2 \times C2)$$

Where,

$$R1 = 1/(\omega_0 \times Q \times C1) \text{ and } R2 = Q/(\omega_0 \times C2).$$

The DC bias applied to A2 and A4, half supply, is not
needed when split supplies are available. The circuit
swings rail-to-rail in the passband making it an excellent
anti-aliasing filter for ADCs. The amplitude response is flat
to 1kHz then rolls off at 80dB/decade.

James Hahn, "State Variable Filter Trims Predecessor's Component Count," *Electronics*, April
1, 1982.

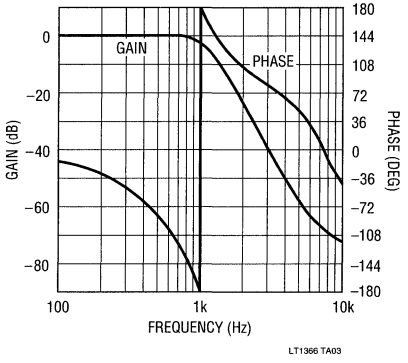


Figure 9. Frequency Response of 4th Order Butterworth Filter

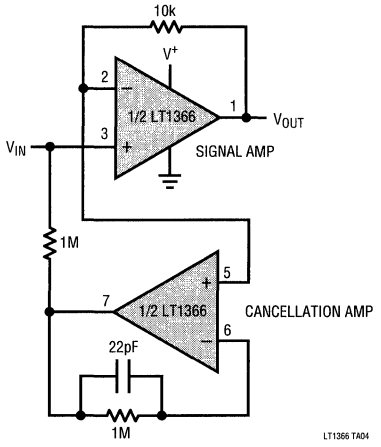


Figure 10. Input Bias Current Cancellation

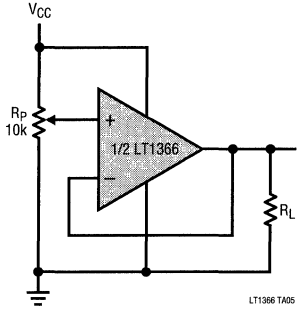


Figure 11. Rail-to-Rail Potentiometer Buffer

RELATED PARTS

PART	DESCRIPTION	COMMENTS
LT1078/LT1079	Dual/Quad 55μA Max, Single Supply, Precision Op Amps	Input/Output Common-Mode Includes Ground, 70μV $V_{OS(MAX)}$ and 2.5μV/C Drift (Max), 200kHz GBW, 0.07V/μs Slew Rate
LTC1152	Rail-to-Rail Input, Rail-to-Rail Output, Zero-Drift Amplifier	High DC Accuracy, 10μV $V_{OS(MAX)}$, 100nV/C Drift, 1MHz GBW, 1V/μs Slew Rate, Supply Current 2.2mA (Max), Single Supply, Can Be Configured for C-Load™ Operation
LT1178/LT1179	Dual/Quad 17μA Max, Single Supply, Precision Op Amps	Input/Output Common-Mode Includes Ground, 70μV $V_{OS(MAX)}$ and 4μV/C Drift (Max), 85kHz GBW, 0.04V/μs Slew Rate
LT1211/LT1212	Dual/Quad 14MHz, 7V/μs, Single Supply, Precision Op Amps	Input Common-Mode Includes Ground, 275μV $V_{OS(MAX)}$ and 6μV/C Drift (Max), Supply Current 1.8mA per Op Amp (Max)

C-Load is a trademark of Linear Technology Corporation

SECTION 2—AMPLIFIERS

HIGH SPEED OPERATIONAL AMPLIFIERS

Quad 12MHz, 145ns Settling Precision Current-to-Voltage Converter for Optical Disk Drives

FEATURES

- **Four Complete Current-to-Voltage Converters**
- **14-Lead Small Outline Package**
- **Accurate Gain: 20mV/μA, ±4%**
- Low Offset Error: 250nA Max
- Low Offset Drift: 2.5nA/°C Max
- Fast Settling: 145ns to 0.1% for a 2V Step
- Wide Bandwidth: 12MHz
- Low Noise: 5pA/$\sqrt{Hz}$
- Low Quiescent Current: 11mA Max
- Wide Supply Range: ±2V to ±18V or 4V to 36V

APPLICATIONS

- Optical Disk Drive
  - Photo Diode Amplifiers
  - Focus and Tracking Summing Amplifiers
- Color Scanners
  - RGB Amplifiers
  - Selectable Gain Amplifiers
- Matched Inverting Amplifiers

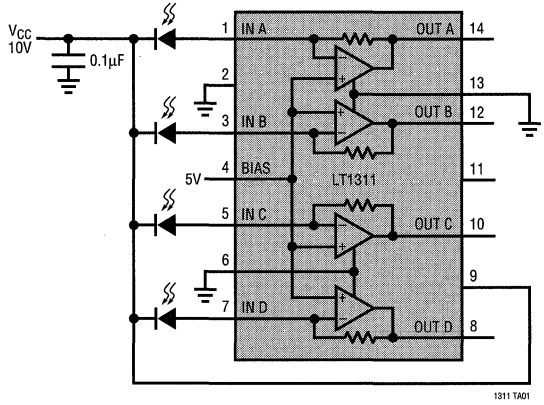
DESCRIPTION

The LT®1311 is a quad current-to-voltage converter designed for the demanding requirements of photo diode amplification. A new approach to current-to-voltage conversion provides excellent DC and AC performance without external DC trims or AC frequency compensation. The LT1311 is ideal for converting multiple photo diode currents to voltages and for general purpose matched inverting amplifier applications.

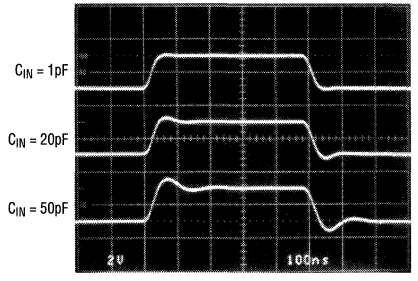
The LT1311 contains four current feedback amplifiers, each with an internal 20k feedback resistor. A supply bypass capacitor is the only external component required to convert four signal currents to voltages. Unlike voltage feedback-based current-to-voltage converters that operate with only a specified value of input capacitance, the current feedback LT1311 settles cleanly with any input capacitance up to 50pF. Only in the most demanding applications will the LT1311 need to be mounted close to the photo diodes.

TYPICAL APPLICATION

Photo Diode Current-to-Voltage Converter



Transient Response



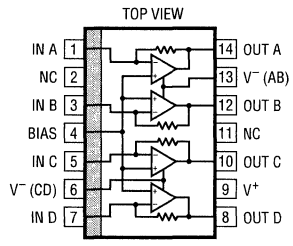
INPUT = 100μA STEP
V_S = ±5V

1311 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
Input Current ..... ±15mA
Output Short-Circuit Duration (Note 1)..... Continuous
Operating Temperature Range ..... −40°C to 85°C
Specified Temperature Range ..... 0°C to 70°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 160°C/W

ORDER PART NUMBER
LT1311CS

Consult factory for Industrial and Military grade parts.

2

ELECTRICAL CHARACTERISTICS

V_S = 10V, V_{BIAS} = 5V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Current to Voltage Gain	V_{OUT} = 2V to 8V, R_L = 2k to 5V	●	19.2	20	20.8	mV/µA
	Current to Voltage Gain Drift		●		−70		ppm/°C
	Current to Voltage Gain Mismatch	Between Amplifiers (ΔG/20k) × 100%	●		0.1	1.0	%
V_{OS}	Input Offset Voltage	With Respect to V_{BIAS}	●		±150	±500	µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift				±1		µV/°C
	Output Offset Voltage	With Respect to V_{BIAS}	●		±1.5	±5	mV
		V_S = ±15V, V_{BIAS} = 0V	●		±3	±10	mV
	Output Offset Voltage Drift		●		±10	±50	µV/°C
		(A + B) − (C + D)	●			±80	µV/°C
	Output Offset Voltage Mismatch	Between Amplifiers	●		±2	±4	mV
	Bias Input Current	Pin 4	●		±5	±20	µA
	Output Noise Voltage Density	f = 1kHz			100		nV/√Hz
i_n	Input Noise Current Density	f = 1kHz			5		pA/√Hz
e_n	Input Noise Voltage Density	f = 1kHz, A_V = 40dB			4.5		nV/√Hz
	Input Impedance	$\Delta V_{OS}/\Delta I_{IN}$, DC, ΔV_{OUT} = 2V to 8V (I_{IN} = ±150µA)	●		0.2	2	Ω
		$\Delta V_{OS}/\Delta I_{IN}$, f = 10MHz			400		Ω
	Bias Voltage Range		●	V^- + 2V		V^+ − 2V	V
	Bias Rejection Ratio	$\Delta V_{OUT}/\Delta V_{BIAS}$, V_{BIAS} = 2V to 8V	●	55	64		dB
	Bias Input Resistance	V_{BIAS} = 2V to 8V	●	250	500		kΩ
	Bias Input Capacitance	f = 100kHz			18		pF
PSRR	Power Supply Rejection Ratio	V_S = ±2V to ±15V, V_{BIAS} = 0V	●	90	103		dB
	Minimum Supply Voltage	V_{BIAS} = 2V	●	4			V
	Voltage Gain	$\Delta V_{OUT}/\Delta V_{OS}$, V_{OUT} = 2V to 8V, R_L = 2k to 5V	●	10	100		V/mV
V_{OUT}	Maximum Output Voltage Swing	Output High, No Load, I_{IN} = −250µA	●	8.8	9.0		V
		Output High, I_{SOURCE} = 10mA, I_{IN} = −250µA	●	8.5	8.8		V
		Output Low, No Load, I_{IN} = 250µA	●		1.0	1.2	V
		Output Low, I_{SINK} = 10mA, I_{IN} = 250µA	●		1.2	1.5	V
	Output Impedance	I_{OUT} = 0mA, f = 10MHz			60		Ω
I_{OUT}	Maximum Output Current	I_{IN} = ±200µA, V_{OUT} = 5V	●	±30	±55		mA
I_S	Supply Current	I_{IN} = 0	●		7	11	mA
SR	Slew Rate	I_{IN} = ±150µA, V_{OUT} at 3V, 7V			80		V/µs

ELECTRICAL CHARACTERISTICS

V_S = 10V, V_{BIAS} = 5V, T_A = 25°C, unless otherwise noted.

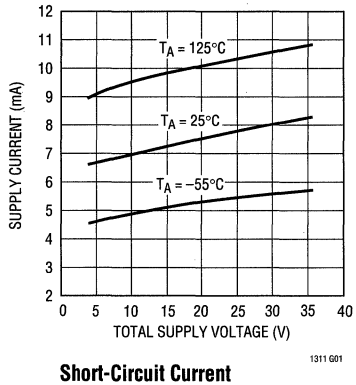
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BW	Small-Signal Bandwidth				12		MHz
	Full Power Bandwidth	V_{OUT} = 2.5V_{P-P}, R_{IN} = 20k			10		MHz
t_r, t_f	Rise Time, Fall Time	10% to 90%, V_{OUT} = 6V_{P-P}, R_{IN} = 20k 10% to 90%, V_{OUT} = 100mV_{P-P}, R_{IN} = 20k			65 35		ns ns
OS	Overshoot	V_{OUT} = 100mV_{P-P}, R_{IN} = 20k			0		%
t_S	Settling Time	ΔV_{OUT} = 2V, 0.1%, R_{IN} = 20k V_S = ±15V, ΔV_{OUT} = 10V, 0.1%, R_{IN} = 20k			145 210		ns ns
THD	Total Harmonic Distortion	V_{OUT} = 2V_{RMS}, 20Hz to 20kHz, R_{IN} = 20k			0.004		%
	Crosstalk	V_{OUT} = 3V to 7V, R_L = 2k to 5V, f = 100Hz, 3 Channels Driven			110		dB

The ● denotes specifications which apply over the full specified temperature range of 0°C to 70°C.

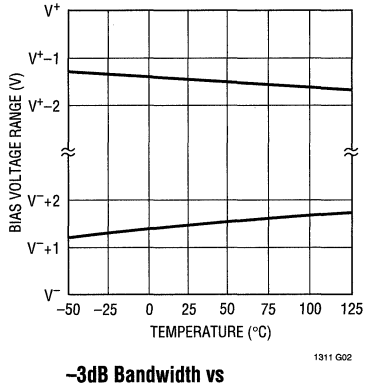
Note 1: A heat sink may be required depending on the power supply voltage and the number of amplifiers that are shorted.

TYPICAL PERFORMANCE CHARACTERISTICS

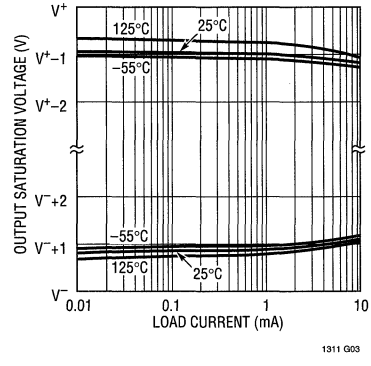
Supply Current vs Supply Voltage



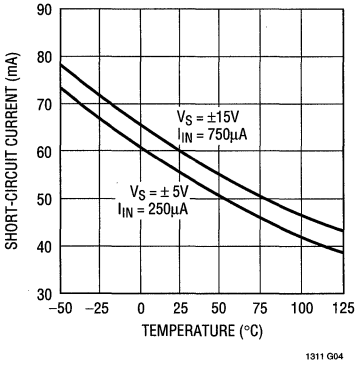
Bias Voltage Range vs Temperature



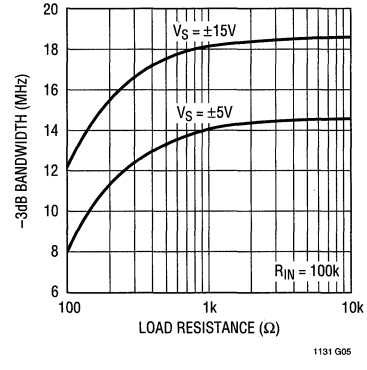
Output Saturation Voltage vs Load Current



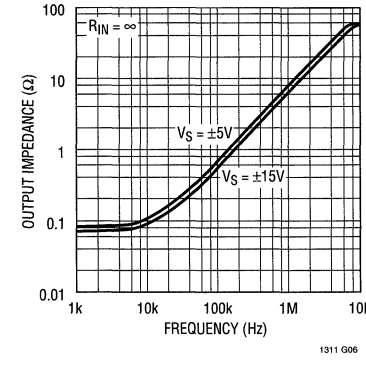
Short-Circuit Current vs Temperature



–3dB Bandwidth vs Load Resistance

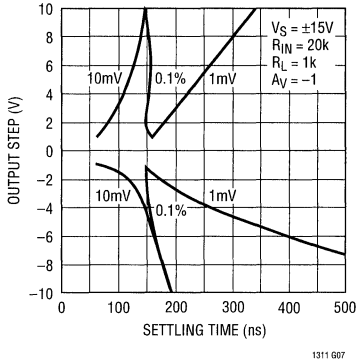


Output Impedance vs Frequency

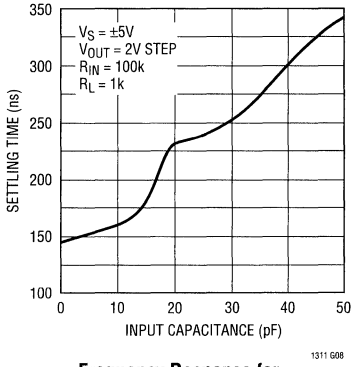


TYPICAL PERFORMANCE CHARACTERISTICS

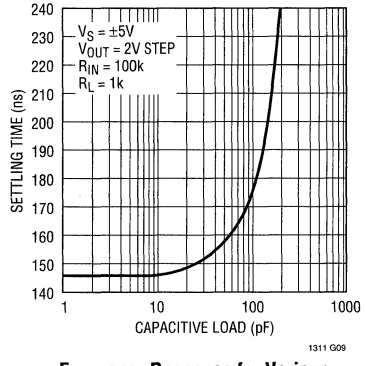
Settling Time to 0.1%, 1mV,10mV vs Output Step



0.1% Settling Time vs Input Capacitance

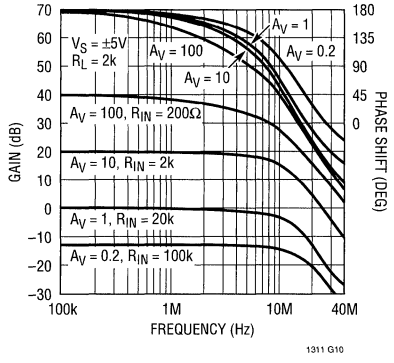


0.1% Settling Time vs Capacitive Load

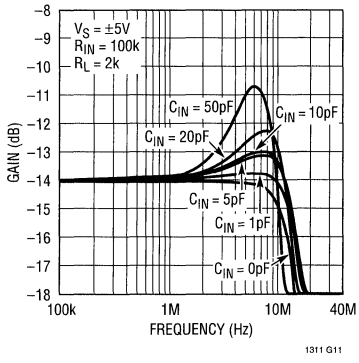


2

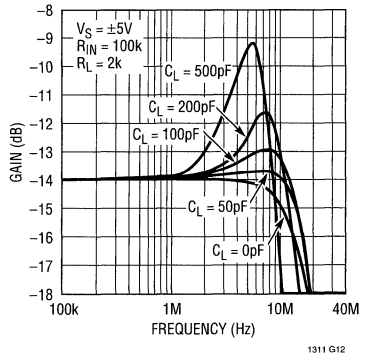
Gain and Phase vs Frequency



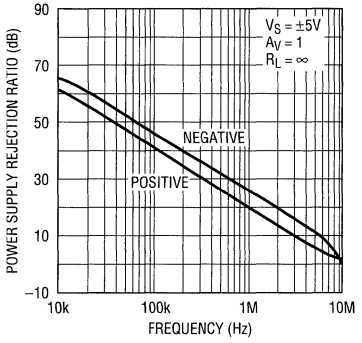
Frequency Response for Various Input Capacitance



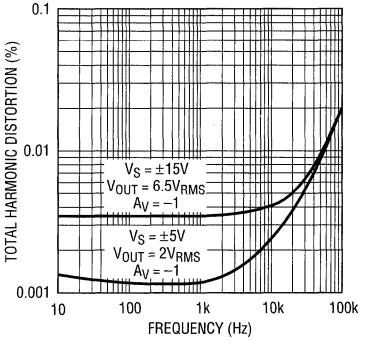
Frequency Response for Various Capacitive Loads



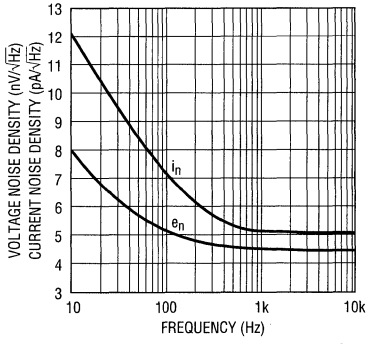
Power Supply Rejection Ratio vs Frequency



Total Harmonic Distortion vs Frequency

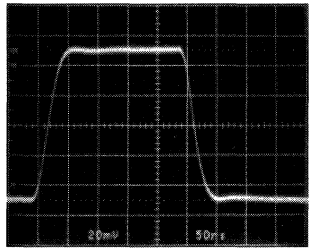


Noise Spectrum



TYPICAL PERFORMANCE CHARACTERISTICS

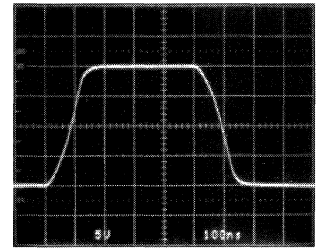
Small-Signal Response



$V_S = \pm 5V$
$A_V = -1$
$R_L = 2k$

1311 G16

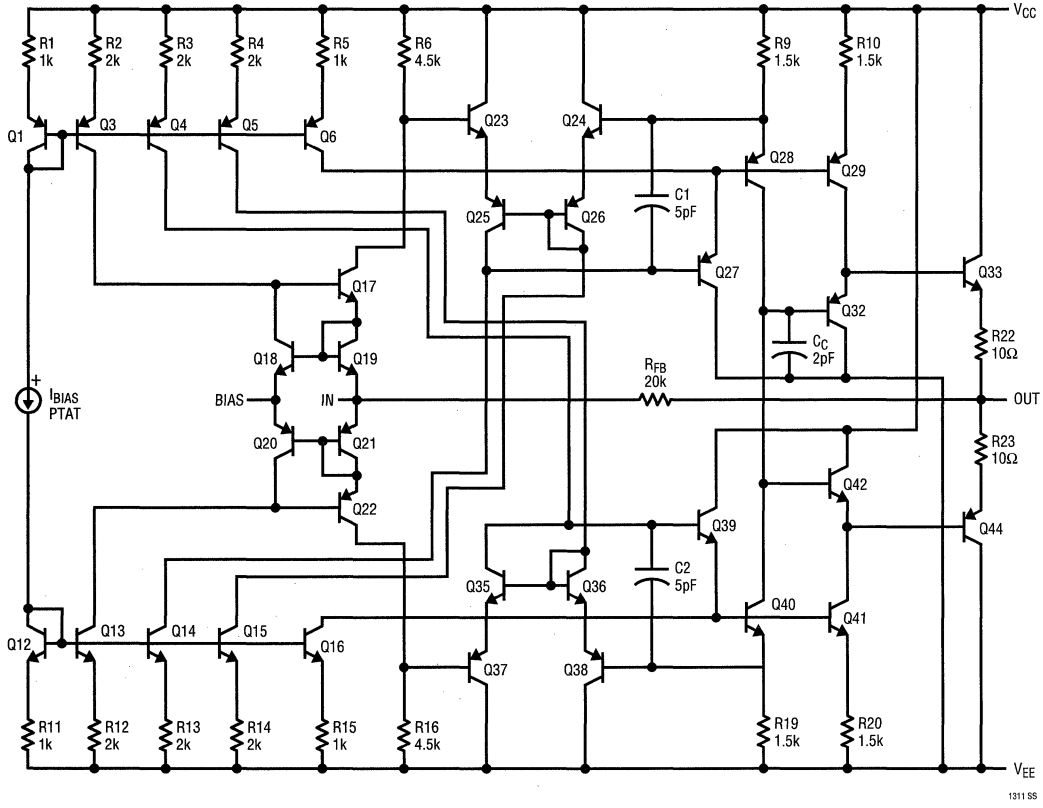
Large-Signal Response



$V_S = \pm 15V$
$A_V = -1$
$R_L = 2k$

1311 G17

SIMPLIFIED SCHEMATIC



1311 SS

APPLICATIONS INFORMATION

Description

The LT1311 contains four identical current feedback amplifiers with their noninverting inputs tied together at pin 4. An external bias voltage is applied to this pin to set the quiescent output voltage of each amplifier. Each amplifier has an internal 20k feedback resistor between the output and the inverting input. The amplifiers are packaged in a 14-pin SO (small outline) package with all four inverting inputs on one side and the outputs on the other. None of the inputs (or the outputs) are on adjacent pins for excellent channel separation.

The feedback resistors in the LT1311 are laser-trimmed at wafer sort to set the current-to-voltage gain. The gain is set to 20mV/μA; the change with temperature is typically –70ppm/°C. The gain matching of the four amplifiers is ten times better. The input offset voltage and bias current are trimmed as well. The trimming also minimizes the resulting output offset drift. For more detailed circuit information, please see the May 1995 (Volume 5, Number 2) issue of *Linear Technology* magazine.

Supply Voltages

The LT1311 can be operated on single or split supplies. The total supply voltage must be greater than 4V and less than 36V. The bias voltage applied to pin 4 can be any value from 2V above the negative supply to 2V below the positive supply. The outputs can swing to within 1V of either supply.

The LT1311 is trimmed while operating on a single 10V supply with a bias voltage of 5V; this is the equivalent of ±5V supplies with the bias at ground. Operation on a single 5V supply with a bias voltage of 2.5V results in very similar performance. Operation on ±15V supplies results in slightly more bandwidth and offset (see the electrical tables and the characteristic curves).

Bypassing the supplies and bias voltage pins requires no special care. For accurate settling, a 0.1μF capacitor within an inch or two of the package works well.

Input Characteristics

The inputs of the LT1311 are low impedance summing nodes. The current feedback amplifiers in the LT1311 have an open-loop input impedance of only a few hundred ohms and therefore the closed-loop response is fairly independent of stray capacitance on the inputs. This is a significant advantage over voltage feedback amplifiers that have to be set up for a particular input capacitance. The LT1311 settles cleanly with any input capacitance from zero to 50pF as shown in the characteristic curves. When the LT1311 is used to convert photo diode currents to signal voltages, the LT1311 does not have to be located close to the diodes.

Output Characteristics

The outputs of the LT1311 are complementary emitter followers. The outputs will swing to within 1V of the supplies with no load, 1.2V delivering 10mA. The outputs are short-circuit protected with a 55mA current limit.

Voltage Gain Applications

When the LT1311 is used with external input resistors to make an inverting voltage gain amplifier, the bandwidth remains fairly constant for gains of 10 or less. At high gains the bandwidth is limited by a gain bandwidth product of about 250MHz. See the characteristic curves for details.

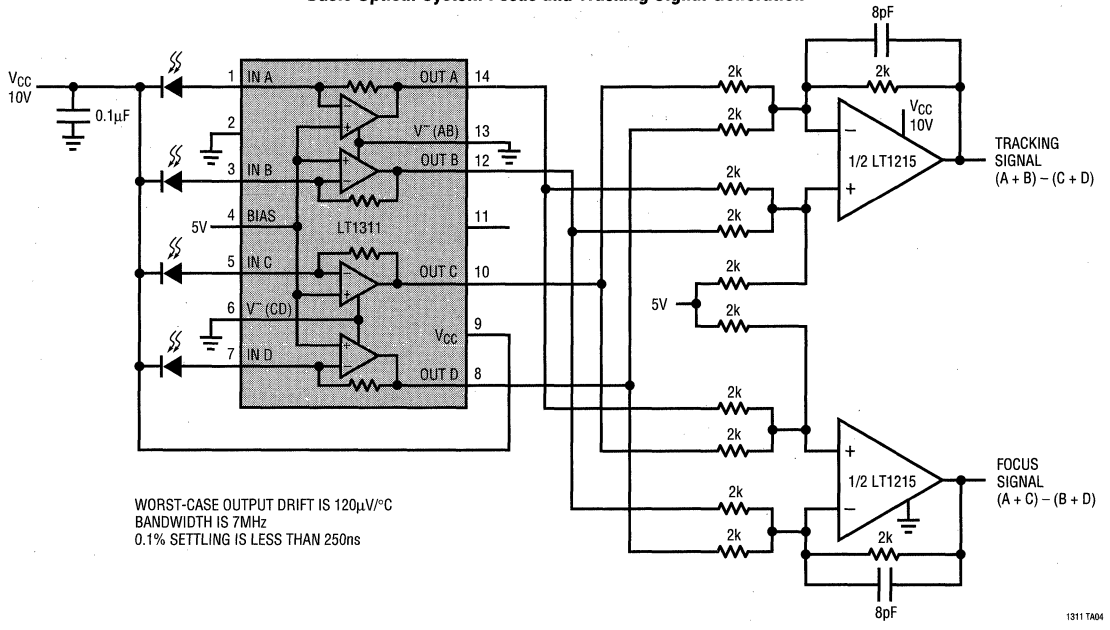
The bandwidth is also influenced by any stray capacitance in parallel with the input resistor. The parallel stray capacitance results in a zero that pushes out the bandwidth. This is particularly noticeable with large input resistors that give gains less than one. For example, a single 100k input resistor results in a bandwidth of 14MHz but two 50k resistors in series result in only 10MHz bandwidth.

Overload Recovery

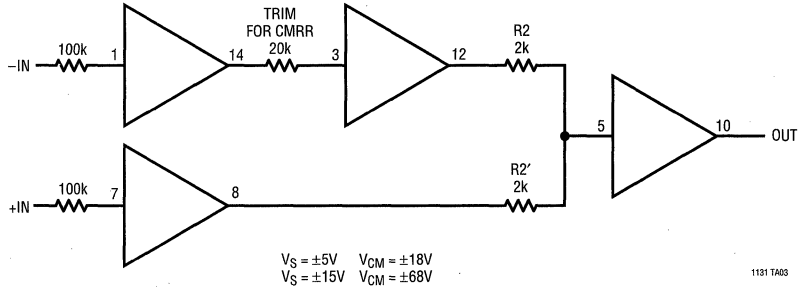
When one or more of the outputs is driven into the rail it will not affect the other amplifiers. However, the output that hit the rail will generate a glitch and take one to two microseconds to recover. Supply current will increase 2mA to 3mA for each amplifier while it is driven into the rail.

TYPICAL APPLICATIONS

Basic Optical System Focus and Tracking Signal Generation



Wide Common-Mode Range Instrumentation Amplifier



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1113	Dual Low Noise, Precision, JFET Input Op Amp	Lowest Voltage Noise FET Op Amp
LT1169	Dual Low Noise, Picoampere Bias Current, JFET Input Op Amp	5pA Input Bias Current
LT1213/LT1214	28MHz, 12V/µs, Single Supply, Dual and Quad Precision Op Amps	Highest Bandwidth, Precision Single Supply Op Amps
LT1215/LT1216	23MHz, 50V/µs Single Supply, Dual and Quad Precision Op Amps	Fastest Settling, Precision Single Supply Op Amps
LT1222	Low Noise, Very High Speed Op Amp	External Compensation and Output Clamping

SECTION 2—AMPLIFIERS

ZERO-DRIFT OPERATIONAL AMPLIFIERS

Rail-to-Rail Input Rail-to-Rail Output Zero-Drift Op Amp

FEATURES

- **Input Common-Mode Range Includes Both Rails**
- **Output Swings Rail to Rail**
- **Output Will Drive 1kΩ Load**
- No External Components Required
- Input Offset Voltage: 10μV Max
- Input Offset Drift: 100nV/°C Max
- Minimum CMRR: 115dB
- Supply Current: 3.0mA Max
- Shutdown Pin Drops Supply Current to 5μA Max
- Output Configurable to Drive Any Capacitive Load
- Operates from 2.7V to 14V Total Supply Voltage

APPLICATIONS

- Rail-to-Rail Amplifiers and Buffers
- High Resolution Data Acquisition Systems
- Supply Current Sensing in Either Rail
- Low Supply Voltage Transducer Amplifiers
- High Accuracy Instrumentation
- Single Negative Supply Operation

DESCRIPTION

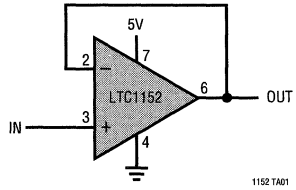
The LTC®1152 is a high performance, low power zero-drift op amp featuring an input stage that common modes to both power supply rails and an output stage that provides rail-to-rail swing, even into heavy loads. The wide input common-mode range is achieved with a high frequency on-board charge pump. This technique eliminates the crossover distortion and limited CMRR imposed by competing technologies. The LTC1152 is a C-Load™ of amp, enabling it to drive any capacitive load.

The LTC1152 shares the excellent DC performance specs of LTC's other zero-drift amplifiers. Typical offset voltage is 1μV and typical offset drift is 10nV/°C. CMRR and PSRR are 130dB and 120dB and open-loop gain is 130dB. Input noise voltage is $2\mu V_{P-P}$ from 0.1Hz to 10Hz. Gain-bandwidth product is 0.7MHz and slew rate is 0.5V/μs, all with supply current of 3.0mA max over temperature. The LTC1152 also includes a shutdown feature which drops supply current to 1μA and puts the output stage in a high impedance state.

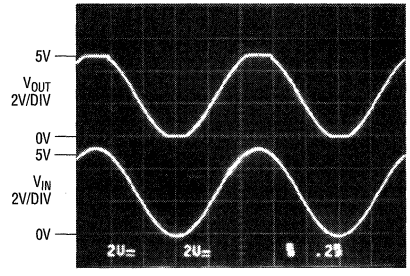
The LTC1152 is available in 8-pin PDIP and 8-pin SO packages and uses the standard op amp pinout, allowing it to be a plug-in replacement for many standard op amps.

TYPICAL APPLICATION

Rail-to-Rail Buffer



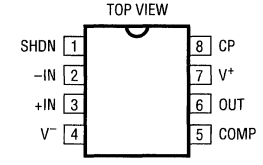
Input and Output Waveforms



ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 14V
Input Voltage ..... $V^+ + 0.3V$ to $V^- - 0.3V$
Output Short-Circuit Duration (Pin 6) ..... Indefinite
Operating Temperature Range
LTC1152C..... 0°C to 70°C
LTC1152I..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP
S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 110°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 110°C, θ_{JA} = 200°C/W (S8)

ORDER PART NUMBER
LTC1152CN8 LTC1152CS8 LTC1152IN8 LTC1152IS8
S8 PART MARKING
1152 1152I

Consult factory for Military grade parts.

2

ELECTRICAL CHARACTERISTICS

V_S = 5V, T_A = operating temperature range, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C (Note 1)			±1	±10	µV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●		±10	±100	nV/°C
	Long-Term Offset Drift				±50		nV/√Mo
I_B	Input Bias Current	T_A = 25°C (Note 2)	 ●		±10	±100 ±1000	pA pA
I_{OS}	Input Offset Current	T_A = 25°C (Note 2)	 ●		±20	±200 ±500	pA pA
e_n	Input Noise Voltage (Note 3)	R_S = 100Ω, 0.1Hz to 10Hz R_S = 100Ω, 0.1Hz to 1Hz			2 0.5	3 1	μV_{P-P} μV_{P-P}
i_n	Input Noise Current	f = 10Hz			0.6		fA/√Hz
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 5V	●	115	130		dB
PSRR	Power Supply Rejection Ratio	V_S = 3V to 12V	 ●	110 105	120		dB dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k, V_{OUT} = 0.5V to 4.5V	●	110	130		dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	R_L = 1k, V_S = Single 5V R_L = 1k, V_S = ±2.5V R_L = 100k, V_S = ±2.5V	● ●	4.0 ±2.0	4.4 2.2 ±2.49		V V V
SR	Slew Rate	R_L = 10k, C_L = 50pF, V_S = ±2.5V			0.5		V/µs
GBW	Gain-Bandwidth Product	R_L = 10k, C_L = 50pF, V_S = ±2.5V			0.7		MHz
I_S	Supply Current	No Load Shutdown = 0V	● ●		2.2 1	3.0 5	mA µA
I_{OSD}	Output Leakage Current	Shutdown = 0V	●		±10	±100	nA
V_{CP}	Charge Pump Output Voltage	I_{CP} = 0			7.3		V
V_{IL}	Shutdown Pin Input Low Voltage				2.5		V
V_{IH}	Shutdown Pin Input High Voltage				4		V
I_{IN}	Shutdown Pin Input Current	V_{SHDN} = 0V	●		–1	–5	µA
f_{CP}	Internal Charge Pump Frequency	T_A = 25°C			4.7		MHz
f_{SMPL}	Internal Sampling Frequency	T_A = 25°C			2.3		kHz

ELECTRICAL CHARACTERISTICS

V_S = 3V, T_A = operating temperature range, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	T_A = 25°C (Note 1)			±1	±10	µV
ΔV_{OS}	Average Input Offset Drift	(Note 1)	●		±10	±100	nV/°C
I_B	Input Bias Current	T_A = 25°C (Note 2) 	 ●		±5	±100 ±1000	pA pA
I_{OS}	Input Offset Current	T_A = 25°C (Note 2) 	 ●		±10	±200 ±500	pA pA
e_n	Input Noise Voltage (Note 3)	R_S = 100Ω, 0.1Hz to 10Hz R_S = 100Ω, 0.1Hz to 1Hz			2 0.75		μV_{P-P} μV_{P-P}
i_n	Input Noise Current	f = 10Hz			0.6		fA/√Hz
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0V to 3V	●		130		dB
A_{VOL}	Large-Signal Voltage Gain	R_L = 10k, V_{OUT} = 0.5V to 2.5V	●	106	130		dB
V_{OUT}	Maximum Output Voltage Swing (Note 4)	R_L = 1k, V_S = Single 3V R_L = 100k, V_S = ±1.5V	●	2.0	2.5 ±1.48		V V
SR	Slew Rate	R_L = 10k, C_L = 50pF, V_S = ±1.5V			0.4		V/µs
GBW	Gain-Bandwidth Product	R_L = 10k, C_L = 50pF, V_S = ±1.5V			0.5		MHz
I_S	Supply Current	No Load Shutdown = 0V	● ●		1.8 1	2.5 5	mA µA
I_{OSD}	Output Leakage Current	Shutdown = 0V	●		±10		nA
V_{CP}	Charge Pump Output Voltage	I_{CP} = 0			4.5		V
V_{IL}	Shutdown Pin Input Low Voltage				1.2		V
V_{IH}	Shutdown Pin Input High Voltage				2.3		V
I_{IN}	Shutdown Pin Input Current	V_{SHDN} = 0V			–1		µA
f_{CP}	Internal Charge Pump Frequency	T_A = 25°C			4.2		MHz
f_{SMPL}	Internal Sampling Frequency	T_A = 25°C			2.1		kHz

The ● denotes specifications which apply over the full operating temperature range.

Note 1: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels during automated testing.

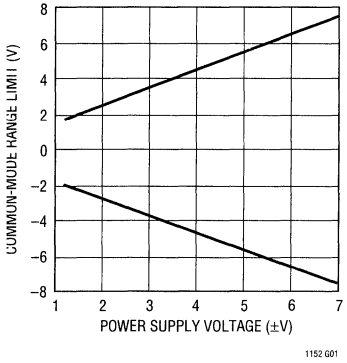
Note 2: At T ≤ 0°C these parameters are guaranteed by design and not tested.

Note 3: 0.1Hz to 10Hz noise is specified DC coupled in a 10-sec window; 0.1Hz to 1Hz noise is specified in a 100-sec window with an RC highpass filter at 0.1Hz. Contact LTC factory for sample tested or 100% tested noise parts.

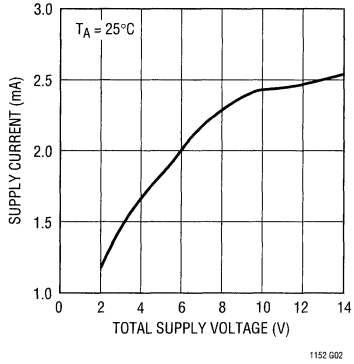
Note 4: All output swing measurements are taken with the load resistor connected from output to ground. For single supply tests, only the positive swing is specified (negative swing will be 0V due to the pull-down effect of the load resistor). For dual supply operation, both positive and negative swing are specified.

TYPICAL PERFORMANCE CHARACTERISTICS

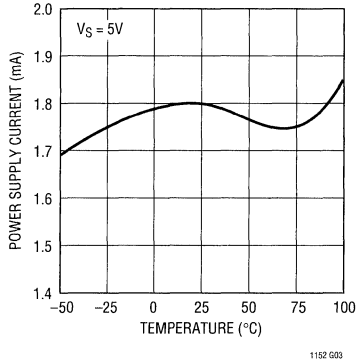
Common-Mode Range vs Supply Voltage



Supply Current vs Supply Voltage

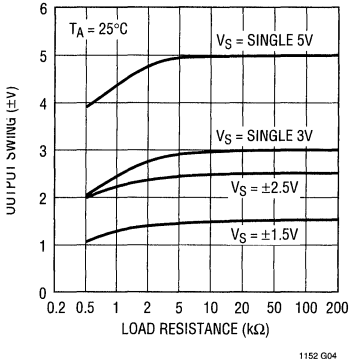


Supply Current vs Temperature

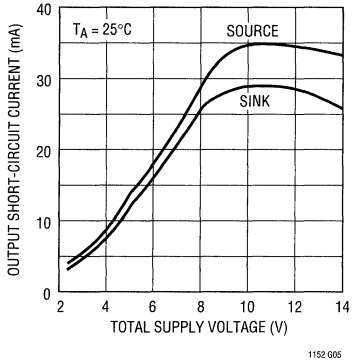


2

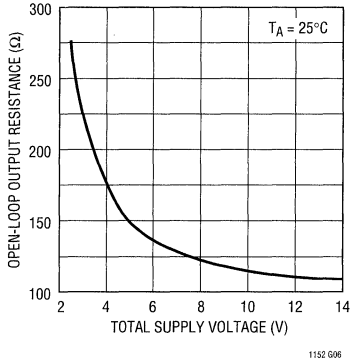
Output Swing vs Load Resistance



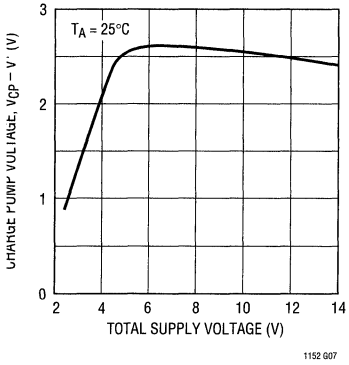
Output Short-Circuit Current vs Supply Voltage



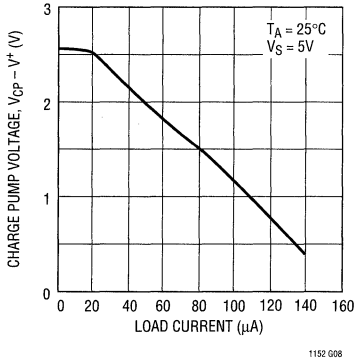
Open-Loop Output Resistance vs Supply Voltage



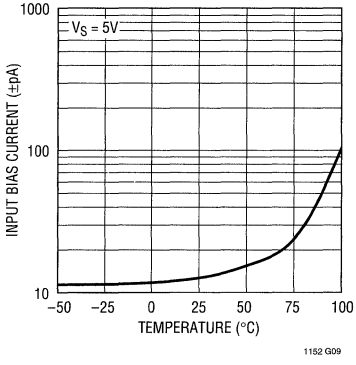
Charge Pump Voltage vs Supply Voltage



Charge Pump Voltage vs Load Current

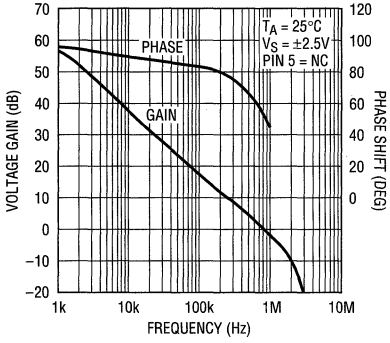


Input Bias Current vs Temperature



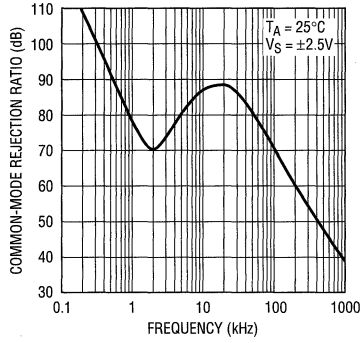
TYPICAL PERFORMANCE CHARACTERISTICS

Gain and Phase Shift vs Frequency



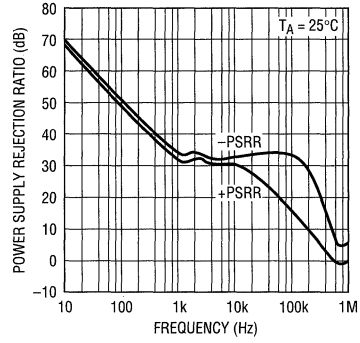
1152 G10

Common-Mode Rejection Ratio vs Frequency



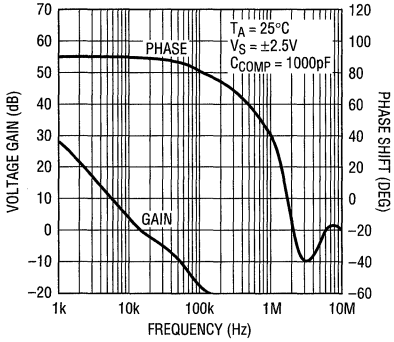
1152 G13

Power Supply Rejection Ratio vs Frequency



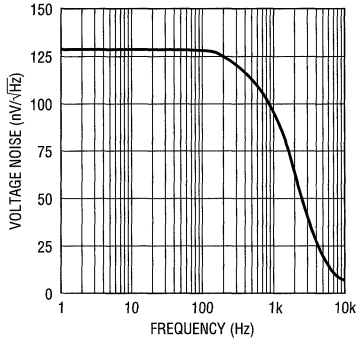
1152 G14

Gain and Phase Shift vs Frequency



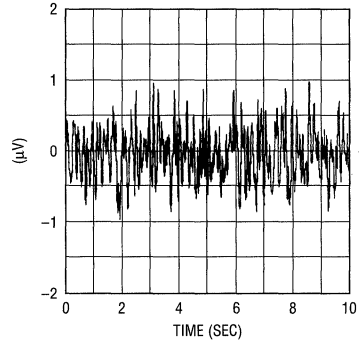
1152 G11

Voltage Noise vs Frequency



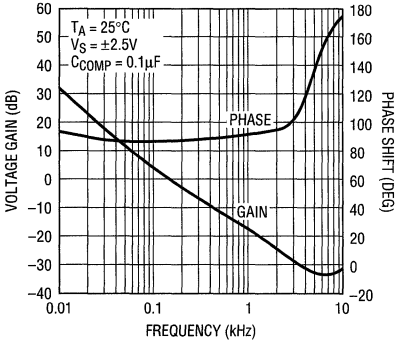
1152 G15

0.1Hz to 10Hz Input Noise



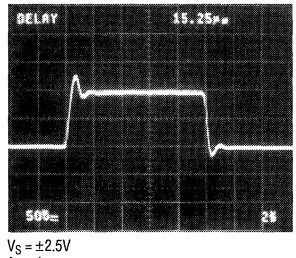
1152 G18

Gain and Phase Shift vs Frequency



1152 G12

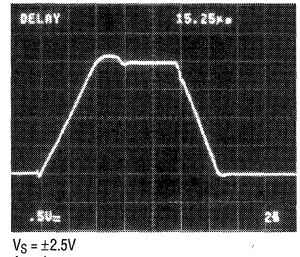
Small-Signal Transient Response



V_S = ±2.5V
A_V = 1

1152 G16

Large-Signal Transient Response



V_S = ±2.5V
A_V = 1

1152 G17

APPLICATIONS INFORMATION

Rail-to-Rail Operation

The LTC1152 is a rail-to-rail input common-mode range, rail-to-rail output swing op amp. Most CMOS op amps, including the entire LTC zero-drift amplifier line, and even a few bipolar op amps, can and do, claim rail-to-rail output swing. One obvious use for such a device is to provide a unity-gain buffer for 0V to 5V signals running from a single 5V power supply. This is not possible with the vast majority of so-called "rail-to-rail" op amps; although the output can swing to both rails, the negative input (which is connected to the output) will exceed the common-mode input range of the device at some point (generally about 1.5V below the positive supply), opening the feedback loop and causing unpredictable and sometimes bizarre behavior.

The LTC1152 is an exception to this rule. It features both rail-to-rail output swing and rail-to-rail input common-mode range (CMR); the input CMR actually extends beyond either rail by about 0.3V. This allows unity-gain buffer circuits to operate with any input signal within the power supply rails; input signal swing is limited only by the output stage swing into the load. Additionally, signals occurring at either rail (power supply current sensing, for example) can be amplified without any special circuitry.

Internal Charge Pump

The LTC1152 achieves its rail-to-rail input CMR by using a charge pump to generate an internal voltage approximately 2V higher than V^+. The input stages of the op amp are run from this higher voltage, making signals at V^+ appear to be 2V below the front end's power supply (Figure 1). The charge pump is contained entirely within the LTC1152; no external components are required.

About $100\mu V_{P-P}$ of residual charge pump switching noise will be present on the output of the LTC1152. This feedthrough is at 4.7MHz, higher than the gain-bandwidth of the LTC1152, and will generally not cause any problems. Very sensitive applications can reduce this feedthrough by connecting a capacitor from the CP pin (pin 8) to V^+(pin 7); a 0.1µF capacitor will reduce charge pump feedthrough to negligible levels. The LTC1152 includes an internal diode from pin 8 to pin 7 to prevent external parasitic capacitance from lengthening start-up

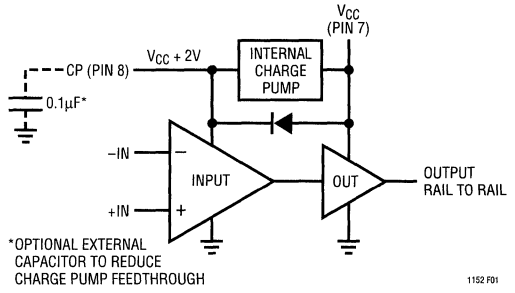


Figure 1. LTC1152 Internal Block Diagram

time. This diode can stand short-term peak currents of about 50mA, allowing it to quickly charge external capacitance to ground or V^-. Large capacitors (>1µF) should not be connected between pin 8 and ground or V^- to prevent excessive diode current from flowing at start-up. The LTC1152 can withstand continuous short circuits between pin 8 and V^+; however, short circuiting pin 8 to ground or V^- will cause large amounts of current to flow through the diode, destroying the LTC1152. Don't do it.

Output Drive

The LTC1152 features an enhanced output stage that can sink and source 10mA with a single 5V supply while maintaining rail-to-rail output swing under most loading conditions. The output stage can be modeled as a perfect rail-to-rail voltage source with a resistor in series with it; this open-loop output resistance limits the output swing by creating a resistor divider with the output load.

The output resistance drops as total power supply voltage increases, as shown in the typical performance curves. It is typically 140Ω with a single 5V supply, allowing a 4.4V output swing into a 1k resistor with a single 5V supply.

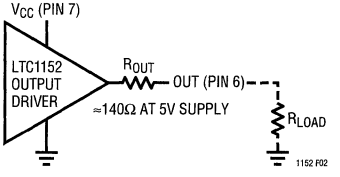


Figure 2. LTC1152 Output Resistance Model

APPLICATIONS INFORMATION

Compensation/Bandwidth Limiting

The LTC1152 is unity-gain stable with capacitive loads up to 1000pF. Larger capacitive loads can be driven by externally compensating the LTC1152. Adding 1000pF between COMP (pin 5) and OUT (pin 6) allows capacitive loading of up to 1μF; 0.1μF between pins 5 and 6 allows the LTC1152 to drive infinite capacitive load (Figure 3).

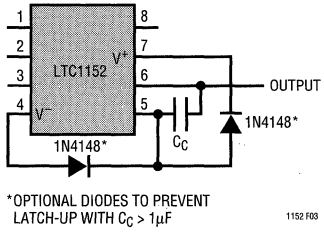


Figure 3. Output Compensation Connection

Large compensation capacitors can also be used to limit the bandwidth of the LTC1152. With 0.1μF from pin 5 to pin 6, the LTC1152's gain-bandwidth product is reduced from 700kHz to around 200Hz. Note that compensation capacitors greater than 1μF can cause latch-up under severe output fault conditions; this can be prevented by clamping pin 5 to each supply with standard signal diodes, as shown in Figure 3.

Shutdown

The LTC1152 includes a shutdown pin (pin 1). When this pin is at V^+, the LTC1152 operates normally. An internal 1μA pull-up keeps the pin high if it is left floating. When pin 1 is pulled low, the part enters shutdown mode; supply current drops to 1μA, all internal clocking stops and the output enters a high impedance state. During shutdown the voltage at the CP pin (pin 8) will drop to 0.5V below V^+. When pin 1 is brought high again, about 10μs will elapse before the charge pump regains full voltage. During this time the LTC1152 will operate normally, but the input CMR may not include V^+. Pin 1 is compatible with CMOS logic running from the same supply as the LTC1152. Additionally, the input trip levels allow ground referenced CMOS logic signals to interface directly to pin 1 when the LTC1152 is running from ±5V or ±3V supplies. The internal 1μA pull-up also allows pin 1 to interface with open-collector/open-drain devices or discrete transistors.

The high impedance output in shutdown allows several LTC1152s to be connected together as a MUX, with their outputs tied in parallel and the active channel selected by using the shutdown pins. Deselected (shutdown) channels will go to high impedance at the outputs, preventing them from fighting with the active channel. This works best when the individual LTC1152s are connected in noninverting feedback configurations to prevent the feedback resistors from passing signals through deselected channels. See the Typical Applications section for a circuit example.

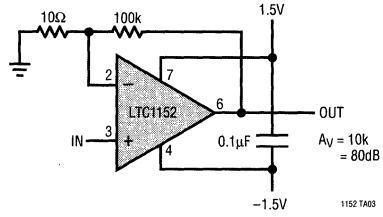
Zero-Drift Operation

The LTC1152 is a zero-drift op amp. Like other LTC zero-drift op amps, it features virtually error-free DC performance, very little drift over time and temperature, and very low noise at low frequencies. The internal nulling clock runs at about 2.3kHz (the charge pump frequency of 4.7MHz divided by 2048) and is synchronized to the internal charge pump to prevent beat frequencies from appearing at the output. The self-nulling circuit constantly corrects the input offset voltage, keeping it typically below ±1μV over the entire input common-mode range. This has the added benefit of providing exceptional CMRR and PSRR at low frequencies—far better than competing rail-to-rail op amps.

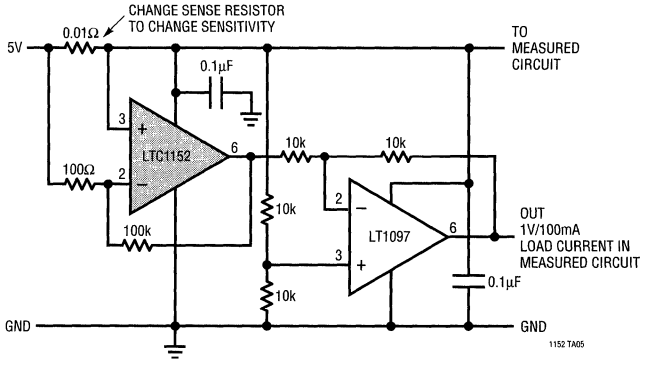
Because it uses a sampling front end, the LTC1152 will exhibit aliasing behavior and clock noise at frequencies near the internal 2.3kHz sampling frequency. The LTC1152 includes an internal anti-aliasing circuit to keep these error terms to a minimum. As a rule, alias frequencies will be down by (80dB – A_{CLG}) in most standard amplifier configurations, where A_{CLG} is the closed-loop gain of the LTC1152 circuit. Clock noise is also dependent on closed-loop gain; it will generally consist of spikes of about 100μV in amplitude, input referred. In general, these error terms are too small to affect most applications. For a more detailed explanation of zero-drift amplifier behavior, see the LTC1051/LTC1053 data sheet.

APPLICATIONS INFORMATION

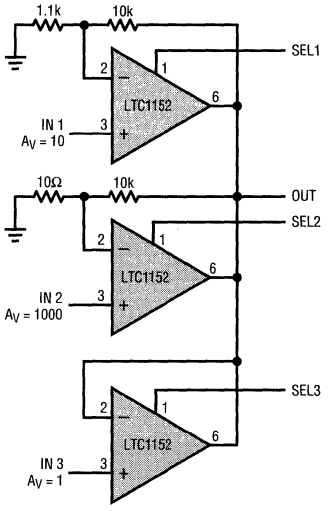
High Gain Amplifier with ±1.5V Supplies



High Side Power Supply Current Sensing



High Precision Three-Input MUX



SELECT INPUTS ARE CMOS LOGIC COMPATIBLE.
SELECT ONLY ONE CHANNEL AT ONCE! 1152 TA04

2

SECTION 3—INSTRUMENTATION AMPLIFIERS

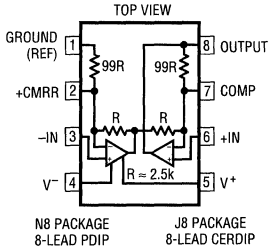
SECTION 3—INSTRUMENTATION AMPLIFIERS

Complete Instrumentation Amplifiers in 8-Pin Packages

- LTC1100: Zero Offset, Drift; Gain of 100
- LT1101: Micropower, Single Supply; Gain of 10 or 100
- LT1102: High Speed JFET Input; Gain of 10 or 100

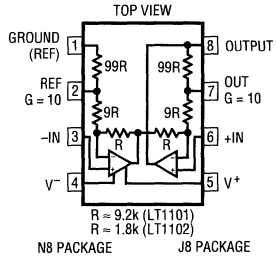
PARAMETER	LTC1100A $V_S = \pm5V$	LT1101A $V_S = 5V$	LT1102A $V_S = \pm15V$
Offset (Max)	10µV	160µV	600µV
Offset Drift (Max)	100nV/°C	2µV/°C	8µV/°C
Bias Current (Max)	50pA	8nA	40pA
Noise (0.1Hz to 10Hz)	$1.9\mu V_{P-P}$ Typ	$0.9\mu V_{P-P}$ Typ	$2.8\mu V_{P-P}$ Typ
Gain	100/10 (SOL PKG)	10/100	10/100
Gain Error (Max)	0.05%	0.05%	0.05%
Gain Drift	4ppm/°C Typ	4ppm/°C Max	18ppm/°C Max
Gain Nonlinearity (Max)	8ppm	8ppm	14ppm
CMRR (G = 100)(Min)	104dB	95dB	84dB
Power Supply (Max)	Single, Dual, 16V	Single, Dual, 44V	Dual, 44V
Supply Current (Max)	2.8mA	130µA	5mA
Slew Rate	1.5V/µs Typ	0.06V/µs Min	21V/µs Min (6:10)
Bandwidth (G = 10)	18kHz Typ	22kHz Min	2MHz Min

LTC1100



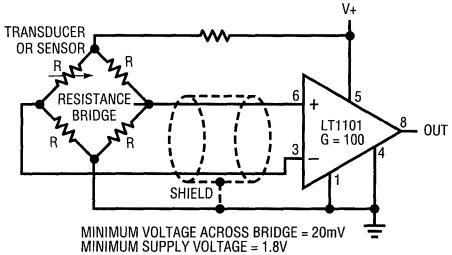
N8 PACKAGE 8-LEAD PDIP J8 PACKAGE 8-LEAD CERDIP

LT1101/LT1102



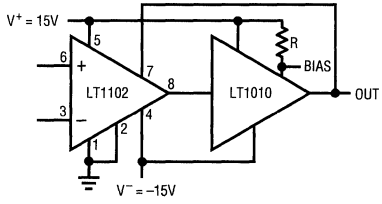
N8 PACKAGE 8-LEAD PDIP J8 PACKAGE 8-LEAD CERDIP

Differential Voltage Amplification from a Resistance Bridge (Single 5V Powered)



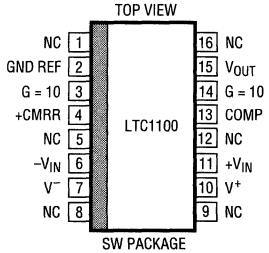
MINIMUM VOLTAGE ACROSS BRIDGE = 20mV
MINIMUM SUPPLY VOLTAGE = 1.8V

Wideband Instrumentation Amplifier with ±150mA Output Current



OUTPUT = ±10V INTO 75Ω TO 330kHz (R = 50Ω)
±10V INTO 200Ω TO 330kHz (R = 200Ω)
DRIVES 2.2nF CAP LOAD
GAIN = 10, DEGRADED 0.01% DUE TO LT1010

LTC1100CS



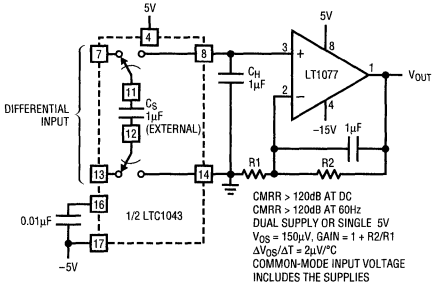
SW PACKAGE
16-LEAD PLASTIC SO WIDE

Dual Precision Instrumentation Switched Capacitor Building Block: LTC1043

- Up to 120dB CMRR
- Adjustable Gain-Set by Output Op Amp
- Offset and Offset Drift as Low as Output Amp Specs
- Precise, Charge-Balanced Switching
- Up to 5MHz Clock Rate
- Internal or External Clock

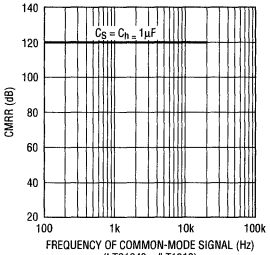
PARAMETER	LTC1043 (USING LTC1050 AMPLIFIER)
Offset	0.5µV
Offset Drift	50nV/°C
Bias Current	10pA
Noise (0.1Hzk to 10Hz)	1.6µV
Gain	Resistor Programmable
Gain Error	Resistor Limited 0.001% Possible
Gain Drift	Resistor Limited <1ppm/°C Possible
Gain Nonlinearity	Resistor Limited 1ppm Possible
CMRR	120dB
Power Supply	Single, Dual (18V, ±9V Max)
Supply Current	2mA
Slew Rate	1mV/ms
Bandwidth	10Hz

Instrumentation Amplifier



CMRR > 120dB AT DC
CMRR > 120dB AT 60Hz
DUAL SUPPLY OR SINGLE 5V
V_{OS} = 150µV, GAIN = 1 + R2/R1
$\Delta V_{OS}/\Delta T$ = 2µV/°C
COMMON-MODE INPUT VOLTAGE INCLUDES THE SUPPLIES

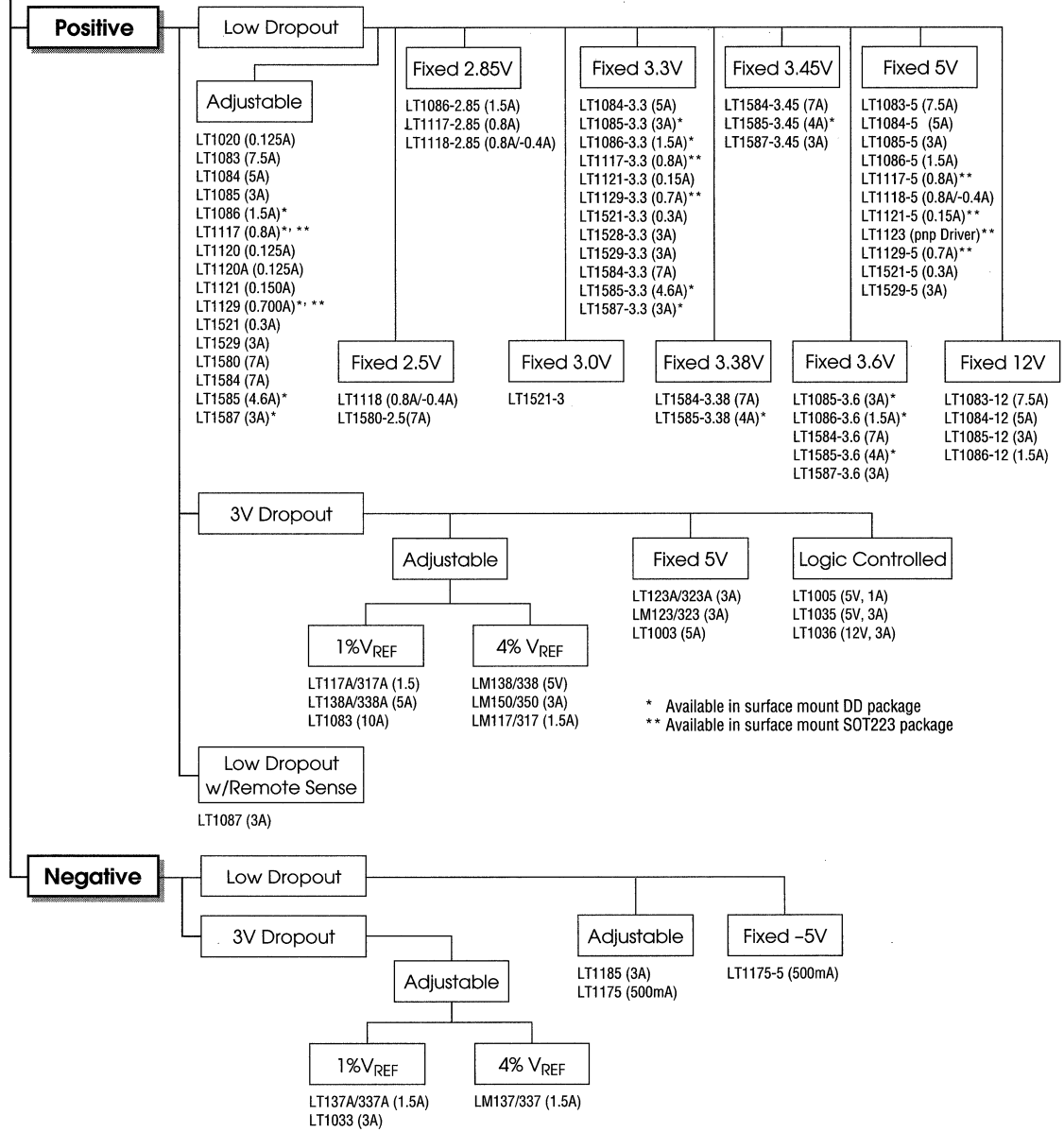
CMRR vs Frequency



SECTION 4—POWER PRODUCTS

SECTION 4—POWER PRODUCTS

LINEAR REGULATORS



Positive Regulators

I_{OUT}	PART NUMBER	DROPOUT VOLTAGE	MICRO-POWER	ADJUST-ABLE	FIXED OUTPUT VOLTAGES AVAILABLE	REMOTE SENSE	SHUTDOWN	DUAL OUTPUT	HIGH VOLTAGE	LOW BATT DETECTOR	SURFACE MOUNT PACKAGE
125mA	LT1020	0.4V	✓	✓		✓	✓			✓	SW
	LT1120	0.4V	✓	✓		✓	✓			✓	S8
	LT1120A	0.4V	✓	✓		✓	✓			✓	S8
150mA	LT1121	0.42V	✓	✓			✓				S8, SOT223
300mA	LT1521	0.5V	✓	✓	3, 3.3, 5		✓				S8, SOT223
500mA	LT317AH	3V		✓					(LT317AHVH)		
	LT1086	0.95V		✓							
800mA	LT1129	0.4V	✓	✓		✓	✓				S8, DD, SOT223
	LT1117	1.1V		✓							SOT223, DD
1A	LT1005	2V			5		✓	✓			
1.5A	LT317A	3V		✓					(LT317AHVK)		
	LT1086	1.3V		✓	2.85, 3.3, 3.6, 5, 12						DD
3A	LT323A	2.5V			5						
	LT350A	3V		✓							
	LT1035	2.2V			5V/3A, 5V/75mA		✓	✓			
	LT1036	2.4V			5V/75mA, 12V/3A		✓	✓			
	LT1085	1.3V		✓							DD (-3.3, -3.6 Only)
	LT1528	0.6V	✓	✓			✓				DD
	LT1529	0.5V	✓	✓	3.3, 5		✓				DD
	LT1587	1.1V		✓	3.3, 3.45, 3.6						DD
4A/4.6A	LT1585	1.1V		✓	3.3, 3.38*, 3.45*, 3.6*						DD (Also 3.38, 3.45V)
5A	LT338A	3V		✓							
	LT1003	2.5V			5						
	LT1084	1.3V		✓	3.3, 5, 12						
	LT1087	1.3V		✓		✓					
7A	LT1580	0.5V		✓	2.5	✓					
	LT1584	1.1V		✓	3.3, 3.38, 3.45, 3.6						
7.5A	LT1083	1.3V		✓	5, 12						
10A	LT1038	3V		✓							
-400/800	LT1118	1V		✓	2.5, 2.85, 5		✓ (S8)				S8, SOT-223

Negative Regulators

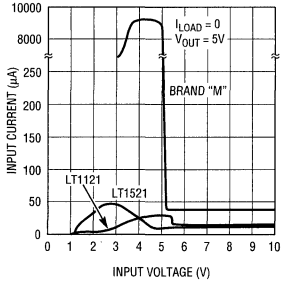
500mA	LT337A	3V		✓					(LT337AHVH)		
	LT1175	0.5V	✓	✓	-5	✓	✓				S8, DD
1.5A	LT337A	3V		✓					(LT337AHVK)		
3A	LT1033	3V		✓							
	LT1185	0.8V		✓		✓	✓				

Discrete PNP Pass Element Driver and Regulators

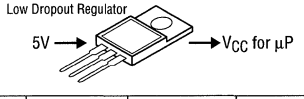
	LT1123	0.45V				✓					SOT223

Not all output voltage variations are available in the indicated surface mount packages. Please consult factory for availability.
*The adjustable and fixed output 3.3V versions of the LT1585 are 4.6A rated, the rest are 4.0A.

LT1120A/LT1521: Lowest Quiescent Current, Best Efficiency



Easy 5V to V_{CC} for New Microprocessors



I_{OUT}	2.5V	3.3V	3.38V	3.45V	3.6V
1.5A	—	LT1086-3.3	—	LT1086	LT1086-3.6
3A	—	LT1587-3.3	—	LT1587-3.45	LT1587-3.6
4A/4.6A	—	LT1585-3.3	LT1585-3.38	LT1585-3.45	LT1585-3.6
7A	LT1580-2.5	LT1584-3.3	LT1584-3.38	LT1584-3.45	LT1584-3.6
7.5A	—	LT1083	—	LT1083	LT1083
10A	—	2×LT1087	—	2×LT1087	2×LT1087

- Perfect for Pentium® Processors
- SMT Packages up to 4.6A
- Three Terminal Regulators; No Design Required
- LT1580 Recommended For Up to 7A Applications; 540mV Dropout

SWITCHING REGULATOR SELECTION GUIDE

		OPTIMIZED FOR STEP-UP OR FLYBACK CONFIGURATIONS							OPTIMIZED FOR STEP-DOWN OR INVERTING APPLICATIONS		OFF-LINE AND/OR PWM CONTROLLERS		
		OSCILLATOR FREQUENCY											
		40kHz	60kHz	100kHz	150kHz	250kHz	500kHz	1MHz	100kHz	500kHz	200kHz	500kHz	1MHz
SWITCH CURRENT	10A		LT1270A										
	8A		LT1270										
	7.5A				LT1268								
	5A	LT1070		LT1170					LT1074				
	4A		LT1271	LT1269									
	3A						LT1371						
	2.5A	LT1071		LT1171									
	2A								LT1076*		LT1103		
	1.5A					LT1373	LT1372	LT1377					
	1.25A	LT1072		LT1172*					LT1176*	LT1375/6			
	1A		LT1082										
	External										LT1105	LT124x	LT1246/47

*LT1572 has built-in Schottky diode.

	INPUT VOLTAGE (V) MIN	MAX	MAXIMUM SWITCH VOLTAGE (V)	MAX RATED SWITCH CURRENT (A)	PACKAGES AVAILABLE
LT1070	3	40	65	5	K, T
LT1070HV	3	60	75	5	K, T
LT1071	3	40	65	2.5	K, T
LT1071HV	3	60	75	2.5	K, T
LT1072	3	40	65	1.25	K, T, N8, S8, SW16
LT1072HV	3	60	75	1.25	K, T
LT1074	8	40	65	5	K, Q, T
LT1074HV	8	60	75	5	K, T
LT1076*	8	40	65	2	K, R, T, Y
LT1076HV	8	60	75	2	K, R, T, Y
LT1082	3	75	100	1	J8, N8, Q, T
LT1170	3	40	65	5	K, T
LT1170HV	3	60	75	5	K, T
LT1171	3	40	65	2.5	K, Q, T
LT1171HV	3	60	75	2.5	K, T
LT1172	3	40	65	1.25	K, T, N8, S8, SW16, Q
LT1172HV	3	60	75	1.25	K, T
LT1176*	8	38	38	1.25	N, SW
LT1268	3	30	60	7.5	T, Q
LT1269	3	30	60	4	SW, T
LT1270A	3	30	60	10	T
LT1270	3	30	60	8	T
LT1271	3	30	60	4	T, Q
LT1371	2.7	30	35	3	R, SW
LT1372	2.7	30	35	1.5	N8, S8
LT1373	2.7	30	35	1.5	N8, S8
LT1375	4.7	25	25	2	N8, S8
LT1376	4.7	25	25	2	N8, S8
LT1377	2.7	30	35	1.5	S8

*Fixed 5V output version available

Commercial Temperature

CURRENT (AMPS)	POS OR NEG OUTPUT	PART NUMBER	PACKAGE TYPE	V_{IN}/V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT (V)	MIL/ IND TEMP	FEATURE/COMMENTS
10.0	Pos Adj	LT1038CK	Steel TO-3	35	1.2 to 33	M	2% V_{OUT} Tol, Plug In Compatible with 317, 350, 338 Types
	Switching	LT1270ACT	TO-220	30	Adjustable		Self-Contained 60kHz PWM and 10 Amp Switch in a 5-Pin Package
8.0	Switching	LT1270CT	TO-220	30	Adjustable		Self-Contained 60kHz PWM and 8 Amp Switch in a 5-Pin Package
7.5	Pos Fixed	LT1083CK-5 LT1083CP-5 LT1083CK-12 LT1083CP-12	Steel TO-3 Plastic TO-3P Steel TO-3 Plastic TO-3P	30 30 30 30	5 5 12 12	M M 	Low Dropout (1.2V), 1% V_{OUT} Tol
	Pos Adj	LT1083CK LT1083CP	Steel TO-3 Plastic TO-3P	30 30	1.2 to 29 1.2 to 29	M, I	Low Dropout (1.2V), Pin Compatible with 317, 350, 338 Types
	Switching	LT1268CQ LT1268CT	Plastic DD TO-220	30 30	Adjustable Adjustable		Self-Contained 150kHz PWM and 7.5A Switch in 5-Pin Package
7.0	Pos Fixed	LT1584CT-3.3 LT1584CT-3.38 LT1584CT-3.45 LT1584CT-3.6	Plastic TO-220 Plastic TO-220 Plastic TO-220 Plastic TO-220	7 7 7 7	3.3 3.38 3.45 3.3		Low Dropout, Fast Transient Response for Microprocessor Applications
	Pos Adj	LT1584CT	Plastic TO-220	7	Adjustable		
5.0	Pos Fixed	LT1003CK LT1003CP	Steel TO-3 Plastic TO-3P	20 20	5 5	M 	2% V_{OUT} Tol
		LT1084CT-3.3 LT1084CK-5 LT1084CP-5 LT1084CT-5 LT1084CK-12 LT1084CP-12 LT1084CT-12	TO-220 Steel TO-3 Plastic TO-3P TO-220 Steel TO-3 Plastic TO-3P TO-220	30 30 30 30 30 30 30	3.3 5 5 5 12 12 12	 M M 	Low Dropout (1.2V), 1% V_{OUT} Tol
	Pos Adj	LT338AK LM338K LT338AP LM338P	Steel TO-3 Plastic TO-3P	35 35	1.2 to 32 1.2 to 32	M 	LT338A Has 1% V_{REF} Tol
		LT1084CK LT1084CP LT1084CT	Steel TO-3 Plastic TO-3P TO-220	30 30 30	1.2 to 29 1.2 to 29 Adjustable	M, I	Low Dropout (1.2V), Pin Compatible with 317, 350, 338 Types
		LT1087CT	TO-220	30	1.2 to 29		Low Dropout (1.2V) with Kelvin Sense
	Switching	LT1070CK LT1070CT LT1070HVCK LT1070HVCT	Steel TO-3 TO-220 Steel TO-3 TO-220	40 40 60 60	Adjustable Adjustable Adjustable Adjustable	M, I I M I	Self-Contained 40kHz PWM and 5A Switch in a 5-Pin Package
		LT1074CK LT1074CT	Steel TO-3 TO-220	45 45	Adjustable Adjustable	M I	Self-Contained 100kHz PWM and 5A Switch in a 5-Pin Package, Step-Down
		LT1074CY	7-Lead TO-220	45	Adjustable		Self-Contained 100kHz PWM and 5A Switch in a 7-Pin Package, Step-Down
		LT1074HVCK LT1074HVCT	Steel TO-3 TO-220	64 64	Adjustable Adjustable	 I	Self-Contained 100kHz PWM and 5A Switch in a 5-Pin Package, Step-Down
		LT1074HVCY	7-Lead TO-220	64	Adjustable		Self-Contained 100kHz PWM and 5A Switch in a 7-Pin Package, Step-Down
		LT1170CK LT1170CQ LT1170CT LT1170HVCT	Steel TO-3 Plastic DD TO-220 TO-220	40 30 40 60	Adjustable Adjustable Adjustable Adjustable	M I 	Self-Contained 100kHz PWM and 5A Switch in a 5-Pin Package, Step-Up/Flyback
4.6	Pos Fixed	LT1585CM-3.3 LT1585CT-3.3	Plastic DD Plastic TO-220	7 7	3.3 3.3		Low Dropout, Fast Transient Response for Microprocessor Applications
	Pos Adj	LT1585CM LT1585CT	Plastic DD Plastic TO-220	7 7	Adjustable Adjustable		
4.0	Pos Fixed	LT1585CM-3.38 LT1585CT-3.38 LT1585CM-3.45 LT1585CT-3.45 LT1585CM-3.6 LT1585CT-3.6	Plastic DD Plastic TO-220 Plastic DD Plastic TO-220 Plastic DD Plastic TO-220	7 7 7 7 7 7	3.38 3.38 3.45 3.45 3.6 3.6		Low Dropout, Fast Transient Response for Microprocessor Applications
	Switching	LT1269CQ LT1269CT	Plastic DD TO-220	30 30	Adjustable Adjustable		Self-Contained 100kHz PWM and 4A Switch in 5-Pin Package
		LT1269CS	20-Lead SO	30	Adjustable		Self-Contained 100kHz PWM and 4A Switch in 20-Lead SO Pkg
		LT1271CQ LT1271CT	Plastic DD TO-220	30 30	Adjustable Adjustable		Self-Contained 60kHz PWM and 4A Switch in 5-Pin Package
3.0	Pos Fixed	LT1587CM-3.3 LT1587CT-3.3 LT1587CM-3.45 LT1587CT-3.45 LT1587CM-3.6 LT1587CT-3.6	Plastic DD Plastic TO-220 Plastic DD Plastic TO-220 Plastic DD TO-220	7 7 7 7 7 7	3.3 3.3 3.45 3.45 3.3 3.3		Low Dropout, Fast Transient Response for Microprocessor Applications
		LT1528CT LT1528CQ	5-Lead TO-220 5-Lead DD	15	Adjustable Adjustable		Low Dropout (0.6V at 3A), Fast Transient Response for Microprocessor Applications
		LT1529CT LT1529-3.3 LT1529-5 LT1529CQ LT1529-3.3 LT1529-5	5-Lead TO-220 5-Lead TO-220 5-Lead TO-220 5-Lead DD 5-Lead DD 5-Lead DD	15 15 	Adjustable 3.3V 5V Adjustable 3.3V 5V		Micropower (50µA Quiescent Current) Ultra Low Dropout (0.5V at 3A)
		LT323AK LM323K LT323AT	Steel TO-3 TO-220	20 20	5 5	M 	LT323A Has 1% V_{OUT} Tol LT323A Has 1% V_{OUT} Tol
		LT1085CT-3.3	TO-220	30	3.3		Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1085CM-3.3 LT1085CM-3.6	Plastic DD Plastic DD	30 30	3.3 3.6		Low Dropout (1.2V), 1% V_{OUT} Tol 3-Pin Surface Mount Package
		LT1085CT-3.6 LT1085CK-5	TO-220 Steel TO-3	30 30	3.6 5	 M, I	Low Dropout (1.2V), 1% V_{OUT} Tol

Commercial Temperature

CURRENT (AMPS)	POS OR NEG OUTPUT	PART NUMBER	PACKAGE TYPE	V_{IN}/V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT (V)	MIL/ IND TEMP	FEATURE/COMMENTS
3.0	Pos Fixed	LT1085CT-5 LT1085CK-12 LT1085CT-12	TO-220 Steel TO-3 TO-220	30 30 30	5 12 12	I M, I I	Low Dropout (1.2V), 1% V_{OUT} Tolerance
	Pos Adj	LT1587CM LT1587CT	Plastic DD TO-220	7 7	Adjustable Adjustable		Low Dropout, Fast Transient Response for Microprocessor Applications
		LT350AK LM350K LT350AT LM350T LT350AP LM350P	Steel TO-3 TO-220 Plastic TO-3P	35 35 35	1.2 to 33 1.2 to 33 1.2 to 33	M	LT350A Has 1% V_{REF} Tol
		LT1085CK LT1085CT	Steel TO-3 TO-220	30 30	1.2 to 29 1.2 to 29	M, I I	Low Dropout (1.2V), Pin Compatible with 317, 350 Types
	Neg Adj	LT1033CK LT1033CP LT1033CT	Steel TO-3 Plastic TO-3P TO-220	35 35 35	–1.2 to –32 –1.2 to –32 –1.2 to –32	M	2% V_{REF} Tol
		LT1185CT	TO-220	35	–2.5 to –25	M, I	Low Dropout (0.75V) with Prog Current Limit and Shutdown
	Dual Pos Fixed	LT1035CK LT1035CT	Steel TO-3 TO-220	20 20	Two 5V Outputs Two 5V Outputs	M	Logic Controlled Main Output Voltage, 75mA Auxiliary Output
	Positive	LT1036CK LT1036CT	Steel TO-3 TO-220	30 30	12, 5 12, 5	M	Logic Controlled 12V, 3A Output, 5V, 75mA Auxiliary Output
	Switching	LT1371CR LT1371CS	7-Lead DD 20-Lead SW	40 40	Adjustable Adjustable		Self-Contained 500kHz PWM and 3A Switch
2.5	Switching	LT1071CK LT1071CT LT1071HVCK LT1071HVCT	Steel TO-3 TO-220 Steel TO-3 TO-220	40 40 60 60	Adjustable Adjustable Adjustable Adjustable	M I M I	Self-Contained 40kHz PWM and 2.5A Switch in a 5-Pin Package
		LT1171CK LT1171CT LT1171HVCT	Steel TO-3 TO-220 TO-220	40 40 60	Adjustable Adjustable Adjustable	M I	Self-Contained 100kHz PWM and 2.5A Switch in a 5-Pin Package
		LT1171CQ	Plastic DD	40	Adjustable		Self-Contained 100kHz PWM and 2.5A Switch in a 5-Pin Sur Mt Pack
2.0	Switching	LT1076CK	Steel TO-3	45	Adjustable	M	Self-Contained 100kHz PWM and 2A Switch
		LT1076CR	Plastic DD	45	Adjustable		Self-Contained 100kHz PWM and 2A Switch in a 7-Pin Sur Mt Pack
		LT1076CT LT1076HVCK	TO-220 Steel TO-3	45 64	Adjustable Adjustable	I	Self-Contained 100kHz PWM and 2A Switch
		LT1076HVCT	TO-220	64	Adjustable	I	Self-Contained 100kHz PWM and 2A Switch in a 5-Pin Package
		LT1076CY-5 LT1076HVCY-5	7-Lead TO-220 7-Lead TO-220	45 64	5 5		100kHz PWM and 2A Switch in 7-Pin Package with Shutdown and Fixed 5V Output
		LT1076CR-5	Plastic DD	45	5		Self-Contained 100kHz PWM and 2A Switch in a 7-Pin Sur Mt Pack
		LT1076CY LT1076HVCY	7-Lead TO-220 7-Lead TO-220	45 64	Adjustable Adjustable		Self-Contained 100kHz PWM and 2A Switch in a 7-Pin Package
		LT1103CY	7-Lead TO-220	30	Adjustable	I	Designed for AC Line Powered Applications, Minimum External Components Required for 75W Isolated Power Supply
		LT1302CN8 LT1302CS8	8-Pin PDIP 8-Pin Plastic SO	10 10	Adjustable Adjustable		Micropower Switching Regulator Works Down to 2V Input and Produces 5V at 600mA
		LT1302CN8-5 LT1302CS8-5	8-Pin PDIP 8-Pin Plastic SO	5 5	5 5		Micropower Switching Regulator Works Down to 2V Input and Produces 5V at 600mA
1.5	Pos Fixed	LT1086CT-2.85	TO-220	30	2.85		Intended for SCSI-2 Active Termination
	Switching	LT1372CN8 LT1372CS8	8-Pin PDIP 8-Pin Plastic SO	30 30	Adjustable Adjustable		Self-Contained 500kHz PWM and 1.5A Switch in a 8-Pin Package
		LT1372CN8-12 LT1372CS8-12	8-Pin PDIP 8-Pin Plastic SO	30 30	12 12		Self-Contained 500kHz PWM and 1.5A Switch in a 8-Pin Package
0.5 to 1.5	Pos Fixed	LT1086CT-3.3 LT1086CM-3.3	TO-220 Plastic DD	30 30	3.3 3.3		Low Dropout (1.2V), 1% V_{OUT} Tol
		LT1086CT-3.6 LT1086CM-3.6	TO-220 Plastic DD	30 30	3.6 3.6		Low Dropout (1.2V) 1% V_{OUT} Tol
		LT1086CK-5 LT1086CT-5 LT1086CK-12 LT1086CT-12	Steel TO-3 TO-220 Steel TO-3 TO-220	30 30 30 30	5 5 12 12	M,I I M, I I	Low Dropout (1.2V), 1% V_{OUT} Tol
	Pos Adj	LT317AK LM317K LT317AH LM317H LT317AT LM317T	Steel TO-3 TO-39 TO-220	40 40 40	1.2 to 37 1.2 to 37 1.2 to 37	M M	LT317A Has 1% V_{REF} Tol
		LT1086CK LT1086CT LT1086CH LT1086CM	Steel TO-3 TO-220 TO-39 Plastic DD	30 30 30 30	1.2 to 29 1.2 to 29 1.2 to 29 1.2 to 29	M, I I M	Low Dropout (1.2V),1% V_{REF} Tol Pin-Compatible with 317 Types Low Dropout (1.2V), 1% V_{REF} Tol 3-Pin Surface Mount Package
	Neg Adj	LT337AK LM337K LT337AH LM337H LT337AT LM337H	Steel TO-3 TO-39 TO-220	40 40 40	–1.2 to –37 –1.2 to –37 –1.2 to –37	M M	LT337A Has 1% V_{REF} Tol
	Pos Adj High Voltage	LT317AHVK LM317HVK LT317AHVH LM317HVH	Steel TO-3 TO-39	60 60	1.2 to 57 1.2 to 57	M M	LT317AHV Has 1% V_{REF} Tol
	Neg Adj High Voltage	LT337AHVK LM337HVK LT337AHVH LM337HVH	Steel TO-3 TO-39	50 50	–1.2 to –47 –1.2 to –47	M M	LT337AHV Has 1% V_{REF} Tol
1.25	Switching	LT1072CK LT1072CT LT1072HVCK LT1072HVCT	Steel TO-3 TO-220 Steel TO-3 TO-220	40 40 60 60	Adjustable Adjustable Adjustable Adjustable	M, I I M, I I	Self-Contained 40kHz PWM and 1.25A Switch in a 5-Pin Package
		LT1072CJ8 LT1072CN8 LT1072CS8	8-Pin CERDIP 8-Pin PDIP 8-Pin Plastic SO	40 40 40	Adjustable Adjustable Adjustable	M I	Self-Contained 40kHz PWM and 1.25A Switch
		LT1172CK LT1172CT LT1172HVCT	Steel TO-3 TO-220 TO-220	40 40 60	Adjustable Adjustable Adjustable	M	Self-Contained 100kHz PWM and 1.25A Switch

Commercial Temperature

CURRENT (AMPS)	POS OR NEG OUTPUT	PART NUMBER	PACKAGE TYPE	V_{IN}/V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT (V)	MIL/ IND TEMP	FEATURE/COMMENTS
1.25	Switching	LT1172CJ8 LT1172CN8 LT1172CQ LT1172CS8	8-Pin CERDIP 8-Pin PDIP Plastic DD 8-Pin Plastic SO	40 40 40 40	Adjustable Adjustable Adjustable Adjustable	M I I	Self-Contained 100kHz PWM and 1.25A Switch
		LT1176CN8 LT1176CN8-5	8-Pin PDIP 8-Pin PDIP	38 38	Adjustable 5		Self-Contained 100kHz PWM and 1.2A Switch in 8-Pin DIP Package
		LT1176CS LT1176CS-5	20-Lead SO 20-Lead SO	38 38	Adjustable 5		Self-Contained 100kHz PWM and 1.2A Switch in 20-Lead SO
		LTC1265CN LTC1265CS LTC1265CN-3.3 LTC1265CS-3.3 LTC1265CN-5 LTC1265CS-5	14-Pin PDIP 14-Pin PDIP 14-Pin PDIP 14-Pin PDIP 14-Pin PDIP 14-Pin PDIP	13 13 13 13 13 13	Adjustable Adjustable 3.3 3.3 5 5		Micropower 1A Step-Down Switching Regulator Achieves 90% Efficiency
		LT1572CS	16-Pin SO	40	Adjustable		Built-In 1A Schottky Diode, otherwise similar to LT1172
1.0	Dual Pos Fixed	LT1005CK LT1005CT	Steel TO-3 TO-220	20 20	Two 5V Outputs Two 5V Outputs	M	Logic Controlled Main Output Voltage
	Switching	LT1073CN8 LT1073CS8 LT1073CN8-5 LT1073CS8-5 LT1073CN8-12 LT1073CS8-12	8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO	15 15 15 15 15 15	Adjustable Adjustable 5 5 12 12		Micropower Switching Regulator Works Down to 1V Input. Requires Only 3 External Components (-5, -12 Versions)
		LT1082CN8 LT1082CT	8-Pin PDIP TO-220	75 75	Adjustable *	I I	60kHz PWM and 1A, 100V Switch 60kHz PWM and 1A, 100V Switch
		LT1107CN8 LT1107CS8 LT1107CN8-5 LT1107CS8-5 LT1107CN8-12 LT1107CS8-12	8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO	36 36 36 36 36 36	Adjustable Adjustable 5 5 12 12	M M M 	Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (–5, –12 Versions). Optimized for $V_{IN} \geq 2V$, Allows Use of Surface Mount Inductors.
		LT1108CN8 LT1108CS8 LT1108CN8-5 LT1108CS8-5 LT1108CN8-12 LT1108CS8-12	8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO	36 36 36 36 36 36	Adjustable Adjustable 5 5 12 12		Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (-5, -12 Versions) Optimized for $V_{IN} \geq 2V$
		LT1109CZ-5 LT1109CZ-12 LT1109CN8-5 LT1109CS8-12 LT1109CN8-5 LT1109CS8-12	3-Pin TO-92 3-Pin TO-92 8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO	36 36 36 36 36 36	5 12 5 5 12 12		Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (–5, –12 Versions). Optimized for $V_{IN} \geq 2V$. Available in 3-Pin TO-92 Package. N8/S8 Versions Also Offer Shutdown Feature. 12V Version Ideal for Flash Memory Vpp Pulse Generation from 5V or 3V
		LT1109ACN8 LT1109ACS8 LT1109ACN8-5 LT1109ACS8-5 LT1109ACN8-12 LT1109ACS8-12	8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO	36 36 36 36 36 36	Adjustable Adjustable 5 5 12 12		Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (–5, –12 Versions). Optimized for $V_{IN} \geq 2V$. 12V Version Ideal for Flash Memory Vpp Pulse Generation from 5V or 2V. Includes Shutdown Feature.
		LT1110CN8 LT1110CS8 LT1110CN8-5 LT1110CS8-5 LT1110CN8-12 LT1110CS8-12	8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO	15 15 15 15 15 15	Adjustable Adjustable 5 5 12 12		Micropower Switching Regulator Works Down to 1V Input. Requires Only 3 External Components (-5, -12 Versions). 60kHz Oscillator Allows Use of Surface Mount Inductors
		LT1111CN8 LT1111CS8 LT1111CN8-5 LT1111CS8-5 LT1111CN8-12 LT1111CS8-12	8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO	36 36 36 36 36 36	Adjustable Adjustable 5 5 12 12	M I M M 	Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (-5, -12 Versions). Optimized for $V_{IN} \geq 2V$. 70kHz Oscillator Allows Use of Surface Mount Inductors
		LT1173CN8 LT1173CS8 LT1173CN8-5 LT1173CS8-5 LT1173CN8-12 LT1173CS8-12	8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO	36 36 36 36 36 36	Adjustable Adjustable 5 5 12 12		Micropower Switching Regulator Works Down to 2V Input. Requires Only 3 External Components (-5, -12 Versions). Optimized for $V_{IN} \geq 2V$
		LT1303CN8-5 LT1303CS8-5	8-Pin PDIP 8-Pin Plastic SO	7 7	5V 5V		Micropower Switching Regulator Works Down to 1.8V Input. Includes Low-Battery Detector
		LT1304CN8-5 LT1304CS8-5 LT1304CN8 LT1304CS8 LT1304CN8-3.3 LT1304CS8-3.3	8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO	7 7 7 7 7 7	5V 5V Adjustable Adjustable 12V 12V		Micropower Switching Regulator Works Down to 1.8V Input. Includes Low-Battery Detector
	Switching (Positive Boost)	LT1300CN8 LT1300CS8	8-Pin PDIP 8-Pin Plastic SO	7 7	3.3/5 3.3/5		Micropower Switching Regulator Works Down to 1.8V Input. Includes Selectable 3.3V or 5V Output and Shutdown
		LT1301CN8 LT1301CS8	8-Pin PDIP 8-Pin Plastic SO	10 10	5/12 5/12	I I	Micropower Switching Regulator Works Down to 1.8V Input. Optimized for Flash Memory VPP Generation from 5V or 2V
	Switching	LT1303CN8 LT1303CS8	8-Pin PDIP 8-Pin Plastic SO	7 7	Adjustable Adjustable		Micropower Switching Regulator Works Down ot 1.8V Input. Includes Low-Battery Detector
800mA	Pos Fixed	LT1117CST LT1117CST-2.85 LT1117CST-3.3 LT1117CST-5	3-Pin SOT-223 3-Pin SOT-223 3-Pin SOT-223 3-Pin SOT-223	15 12 10 10	Adjustable 2.85 3.3 5		Adjustable Low Dropout Regulator, SOT-223 Package Active SCSI-2 Terminator, SOT-223 Package 3.3 Low Dropout Regulator, SOT-223 Package 5V Low Dropout Regulator, SOT-223 Package
700mA	Pos	LT1129CS8 LT1129CS8-3.3 LT1129CS8-5	8-Pin SO 8-Pin SO 8-Pin SO	30 30 30	Adjustable 3.3 5	 I I	Micropower Regulator With Shutdown, Dropout Voltage = 0.4V, Reverse Battery Protection in Low Thermal Resistance SO-8 Package

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Commercial Temperature

CURRENT (AMPS)	POS OR NEG OUTPUT	PART NUMBER	PACKAGE TYPE	V_{IN}/V_{DIFF} MAX (V)	V_O NOMINAL REGULATED OUTPUT (V)	MIL/ IND TEMP	FEATURE/COMMENTS
700mA	Pos	LT1129CT LT1129CQ LT1129CT-3.3 LT1129CST-3.3 LT1129CQ-3.3 LT1129CT-5 LT1129CST-5 LT1129CQ-5	5-Pin TO-220 Plastic DD 5-Pin TO-220 3-Pin SOT-223 5-Pin DD 5-Pin TO-220 3-Pin SOT-223 5-Pin DD	30 30 30 30 30 30 30 30	Adjustable Adjustable 3.3 3.3 3.3 5 5 5	I I I I I I I I	Micropower Regulator With Shutdown, Dropout Voltage = 0.4V, Reverse Battery Protection
500mA	Negative	LT1175CS8 LT1175CN8 LT1175CQ LT1175CT	8-Pin Plastic SO 8-Pin PDIP 5-Pin DD 5-Pin TO-220	–25 –25 –25 –25	Adjustable Adjustable Adjustable Adjustable		Negative Low Dropout has Low Quiescent Current, Adjustable Current Limit
		LT1175CS8-5 LT1175CN8-5 LT1175CQ-5 LT1175CT-5	8-Pin Plastic SO 8-Pin PDIP 5-Pin DD 5-Pin TO-220	–25 –25 –25 –25	–5 –5 –5 –5		Negative Low Dropout has Low Quiescent Current, Adjustable Current Limit
	Switching (Positive Boost)	LT1106CF	20-Pin TSSOP	7	12V or 5V		Thin Package and 500kHz Operation Allows use in Type I PCMCIA Cards
	Switching (Positive Boost)	LT1309CS8	8-Pin Plastic SO	7	12V		500kHz Operation Allows Use of Smallest Inductors/ Capacitors
400mA	Switching (Positive Step-Down)	LTC1174CN8 LTC1174CN8-3.3 LTC1174CN8-5 LTC1174CS8 LTC1174CS8-3.3 LTC1174CS8-5	8-Pin DIP 8-Pin DIP 8-Pin DIP 8-Pin SO 8-Pin SO 8-Pin SO	13.5 13.5 13.5 13.5 13.5 13.5	Adjustable 3.3 5 Adjustable 3.3 5	I I 	Micropower Step-Down Switching Regulator With 90% Efficiency. Selectable 200mA or 400mA Current Limit. Intended for 6V-9V Battery Applications
		LTC1174HVCN8 LTC1174HVCN8 LTC1174HVCN8-3.3 LTC1174HVCS8-3.3 LTC1174HVCN8-5 LTC1174HVCS8-5	8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO	18.5 18.5 18.5 18.5 18.5 18.5	Adjustable Adjustable 3.3 3.3 5 5		Micropower Step-Down Switching Regulator with 90% Efficiency and High Input Voltage Capability
		LTC1574CS LTC1574CS-3.3 LTC1574CS-5	16-Pin Plastic SO 16-Pin Plastic SO 16-Pin Plastic SO	18.5 18.5 18.5	Adjustable 3.3 5		Micropower Step-Down Switching Regulator with On-Chip Schottky Diode and 90% Efficiency
300mA	Pos	LTC1521CS8 LTC1521CS8-3 LTC1521CS8-3.3 LTC1521CS8-5 LTC1521CST-3 LTC1521CST-3.3 LTC1521CST-5	8-Pin Plastic SO 8-Pin Plastic SO 8-Pin Plastic SO 8-Pin Plastic SO 3-Lead SOT-223 3-Lead SOT-223 3-Lead SOT-223	20 20 20 20 20 20 20	Adjustable 3 3.3 5 3 3.3 5		Micropower Regulator With SHutdown: Ultra-Low Dropout (0.5V) and Quiescent Current (12µA). 3-Pin Versions Have Shutdown
150mA	Pos	LT1121ACS8 LT1121ACS8-3.3 LT1121ACS8-5	8-Lead SO 8-Lead SO 8-Lead SO	30 30 30	Adjustable 3.3 5	I I I	Micropower Regulator With Shutdown, Dropout Voltage = 0.4V, Reverse Battery Protection in Low Thermal Resistance SO-8 Package
		LT1121CN8 LT1121CS8 LT1121CN8-3.3 LT1121CS8-3.3 LT1121CST-3.3 LT1121CN8-5 LT1121CS8-5 LT1121CST-5	8-Pin PDIP 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO 3-Pin SOT-223 8-Pin PDIP 8-Pin Plastic SO 3-Pin SOT-223	30 30 30 30 30 30 30 30	Adjustable Adjustable 3.3 3.3 3.3 5 5 5	I I I I I I I I	Micropower Regulator With Shutdown, Dropout Voltage = 0.4V, Reverse Battery Protection
125mA	Pos Adj	LT1020CJ LT1020CN LT1020CS	14-Pin CERDIP 14-Pin PDIP 16-Pin Plastic SW	36 36 36	4 to 30 4 to 30 4 to 30	M, I I I	Dropout Voltage = 0.4V, 40µA I_Q, Reference and Comparator
		LT1120CJ8 LT1120CN8 LT1120CH	8-Pin CERDIP 8-Pin PDIP 8-Pin TO-5	36 36 36	4 to 30 4 to 30 4 to 30	M I	Dropout Voltage = 0.4V, 40µA I_Q, Reference, Comparator, Shutdown, 8-Pin Package
		LT1120ACN8 LT1120ACS8	8-Pin PDIP 8-Pin PDIP	36 36	4 to 30 4 to 30		Dropout Voltage = 0.4V, 20µA I_Q, Reference, Comparator, Shutdown, 8-Pin Package
100mA	Pos Adj	LT1431CJ8 LT1431CN8 LT1431CS8 LT1431CZ	8-Pin CERDIP 8-Pin PDIP 8-Pin Plastic SO TO-92	36 36 36 36	2.5 to 36 2.5 to 36 2.5 to 36 2.5 to 36	M I I I	0.4% Initial Tolerance, 1% Over Temperature
20mA to 100mA	Switched Capacitor	LT1026CJ8 LT1026CN8 LT1026CH LT1026CS8	8-Pin CERDIP 8-Pin PDIP 8-Pin TO-5 Can 8-Pin SO	10 10 10 10	* * * *	M M 	Dual Voltage Converter, 10mA Output, $5V_{IN}$, $\pm 10V_{OUT}$
		LTC1044CJ8 LTC1044CN8 LTC1044CH LTC1044CS8 LTC1044ACN8 LTC1044ACS8	8-Pin CERDIP 8-Pin PDIP 8-Pin TO-5 Can 8-Pin Plastic SO 8-Pin PDIP 8-Pin Plastic SO	9.5 9.5 9.5 9.5 13 13	* * * * * *	M M I I	Voltage Converter, 20mA Output
		LTC1046CN8 LTC1046CS8	8-Pin PDIP 8-Pin Plastic SO	6 6	* *	I I	50mA Output Current, 165µA Supply Current, 35Ω Max Output Impedance
		LT1054CJ8 LT1054CN8 LT1054CH LT1054CS8	8-Pin CERDIP 8-Pin PDIP 8-Pin TO-5 Can 8-Pin Plastic SO	16 16 16 16	† † † †	M I M 	Voltage Converter and Regulator, 100mA Output, 25kHz Switching Rate
		LTC1144CN8 LTC1144CS8	8-Pin PDIP 8-Pin Plastic SO	20 20	* *	I I	Voltage Converter, 20mA Output, Up to 18V Operation

* These devices are nonregulating converters.
† The available output voltage range is dependent upon the mode of operation selected.

Battery Management and Charging

PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LTC1325	µProcessor Controlled Battery Management System	N18, SW18	Fast Charge NiCd, NiMH, Li-Ion, or Pb-Acid Batteries Under µP Control. Also Provides Full Charge/Discharge Management
LT1510	Constant-Voltage, Constant-Current Battery Charger	S8, N16, S16	Charges NiCd, NiMH and Li-Ion Batteries, 1 Resistor Required to Program Charge Current. Step-Down Topology, 200kHz Switching
LT1512	SEPIC Constant Current/Voltage Battery Charger	N8, S8	SEPIC Topology Means Charger V_{IN} can be Higher or Lower than Battery Voltage

Power Factor Correction Controllers

PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LT1248	Average Current-Mode Power Factor Corrector	N16, S16	Low Line Current Distortion, >0.99 Power Factor, Synchronization, Overvoltage Protection
LT1249	Average Current-Mode Power Factor Corrector	N8, S8	Low Parts Count, Full Feature Power Factor Correction

Regulating Pulse-Width Modulators

PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LT1105	Off-Line Regulating Pulse Width Modulator	N8, N14	Designed for AC Line Powered Applications
LT1241 Series	500kHz Regulating Pulse Width Modulators	J8, N8, S8	Improved Replacements for UC1842, 1843, 1844, 1845
LT1246/LT1247	1MHz Regulating Pulse Width Modulators	N8, S8	1MHz Current Mode PWM, 1.5% V_{REF}, 30ns Current Sense
LT1524/LT3524	Regulating Pulse Width Modulator	J, N, S	Improved SG1524, 2% V_{REF}, Guaranteed Oscillator Accuracy
LT1525A/LT3525A LT1527A/LT3527A	Regulating Pulse Width Modulator	J, N	Improved SG1525A/1527A Switching Regulator with Undervoltage Lockout, Guaranteed Long Term Stability
SG1524/SG3524	Regulating Pulse Width Modulator	J, N	Industry Standard Switching Power Supply Control Circuit
SG1525A/SG3525A	Regulating Pulse Width Modulator	J, N	More Features Than 1524 Series, 100mA Source/Sink Outputs
SG1527A/SG3527A	Regulating Pulse Width Modulator	J, N	Same as SG1525A with Inverted Output Logic
LT1846/3846 LT1847/3847	Current Mode Regulating Pulse Width Modulator	J, N	Current Mode PWM with UV Lockout, Soft Start, 1% V_{REF}, 500kHz Operation, 200mA Totem Pole Outputs

Ultra-High Efficiency Switching Regulator Controllers

PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LTC1142	Dual Step-Down Switching Regulator Controller	SSOP	Dual Synchronous Switching Regulator Controllers with both 3.3V and 5V Outputs
LTC1142HV	Dual Step-Down Switching Regulator Controller	SSOP	20V Max Input Voltage Dual 3.3V/5V or Adjustable Output Synchronous Switching Regulator
LTC1143	Dual Step-Down Switching Regulator Controller	SW16	Dual Switching Regulator Controller with Low Parts Count and both 3.3V and 5V Outputs
LTC1147, LTC1147L	Step-Down Switching Regulator Controller	N8, S8	Low Parts Count, 90% Efficiency Using a Single External P-Channel MOSFET
LTC1148, LTC1148L	Step-Down Switching Regulator Controller	N, S	Synchronized Switching Regulator Controller Using Two External MOSFETs for 95% Efficiency. Up to 16V Inputs
LTC1148HV	Step-Down Switching Regulator Controller	N,S	Synchronized Switching Regulator Controller Using Two External MOSFETs for 95% Efficiency. Up to 20V Inputs
LTC1149	Step-Down Switching Regulator Controller	N, S	Synchronized Switching Regulator Controller Using Two External MOSFETs for 95% Efficiency. Up to 48V Inputs
LTC1159	Step-Down Switching Regulator Controller	G, N, S	Synchronized Switching Regulator Controller Using Two External MOSFETs for 95% Efficiency. Operation to 5V Min, 40V Max Inputs
LTC1266	Step-Down Switching Regulator Controller	S	Synchronized Switching Regulator Using Two External N-Channel MOSFETs for 95% Efficiency. Ideal for 5V to 3.3V Applications
LTC1267	Dual Step-Down Switching Regulator Controller	SSOP	40V Max Input Voltage Dual 3.3V, 5V or Adjustable Output Synchronous Switching Regulator Controller
LTC1430	Step-Down Switching Regulator Controller for PCs	S8, S16	High Current Synchronous Switching Regulator for High Current, 5V to 3.XX or 2.XX Supplies

4

CCFL Backlight Inverters and LCD Contrast Switching Regulator

Part Number	Package	CCFL Supply? Floating Bulb	CCFL Supply? Grounded Bulb	Brightness Control
LT1182	SO16	Y	Y	I, V, PWM
LT1183	SO16	Y	Y	I, V, PWM
LT1184F	SO16	Y	Y	I, V, PWM
LT1184	SO16	N	Y	I, V, PWM
LT1186	SO16	Y	Y	Digital

Regulator Drivers

BASE DRIVE CURRENT	PART NUMBER	PACKAGE TYPE	V_{IN} MAX (V)	V_O NOMINAL REGULATED OUTPUT VOLTAGE	FEATURES/ COMMENTS
150mA	LT1123CZ	TO-92	30	5.0	Requires External PNP, 1% Output Tolerance, 600µA Quiescent Current

LT1103/1105 Off-Line Switching Regulators

APPLICATION	LT1105	LT1103 (Internal Sense Resistor)
Universal Off-Line	10W to Over 100W	10W to 50W
Battery Charger, Isolated Off-Line	OK	OK
Telecom, –48V Input Isolated	OK	OK
Low Voltage Isolated DC/DC (≤24V)	Requires External MOSFET	Needs No MOSFET
High Voltage Isolated DC/DC	OK	OK

Inductor and Capacitor Part Numbers/Manufacturers

INDUCTOR VALUE (µH)	COILTRONICS†	COILCRAFT†	SUMIDA†
15	–	DT3316-153	CD54-150LC
18	CTX20-1	–	CD54-180LC
20	CTX20-1	–	–
22	CTX20-1	DT3316-223	CD54-220LC
27	–	–	CD54-270LC
33	–	DT3316-473	CD54-330LC
47	CTX50-1	DT3316-683	CD74-470LC
68	–	DT3316-104	CD74-680LC
82	CTX82-1	DT3316-154	CD74-820LC
100	CTX100-1	–	CD105-101MC
120	CTX100-1	–	CD105-121MC
180	CTX250-4	–	CDR125-181MC
220	CTX250-4	–	CDR125-221MC
470	–	–	CDR125-471MC

†Surface mount inductors

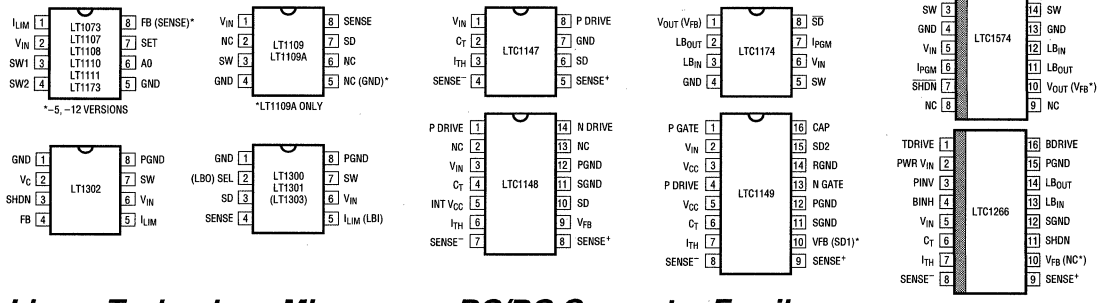
Inductor Manufacturers

Gowanda Elect.	Gowanda, NY, USA	716-532-2234	FAX: 716-532-2702
Coiltronics Intl.	Boca Raton, FL, USA	407-241-7876	FAX: 407-241-9335
Sumida	Arlington Heights, IL, USA	708-956-0666	FAX: 708-956-0702
Coilcraft	Cary, IL, USA	800-322-2645	FAX: 708-639-1469

Capacitor Manufacturers

Best:	TPS Series	AVX	Myrtle Beach, SC,USA	803-946-0690
Better:	OS-CON Series	Sanyo Video	San Diego, CA, USA	619-661-6322
Good:	PL Series	Nichicon America	Schaumberg, IL, USA	708-843-7500

Device Pinouts (DIP and SO Packages)



Linear Technology Micropower DC/DC Converter Family

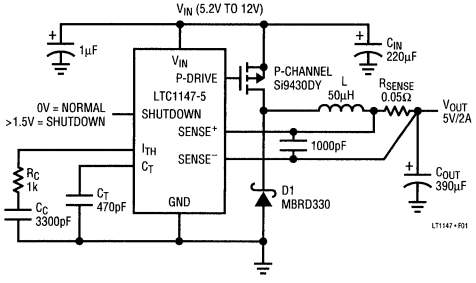
DEVICE	V_{IN} (MIN)	V_{IN} (MAX)	I_{SW} (A) (MAX)	STEP-UP	STEP-DOWN	I_Q (µA)	S/D	LOW BATT DETECT	DROPOUT VOLTAGE (V)	3.3V OUT	5V OUT	12V OUT	ADJ	# OF PINS	SO PACK	APPLICATION EXAMPLE
LT1073	1	15	1	X	X	95		X			X	X	X	8	X	1 Cell to 5V, 40mA
LT1107	2	30	1	X	X	300		X			X	X	X	8	X	2 Cells to 5V, 150mA
LT1108	2	30	1	X	X	110		X			X	X	X	8	X	2 Cells to 5V, 150mA
LT1109	2	30	0.5	X		320					X	X	X	3, 8	X	5V to 12V VPP, 60mA (Flash Memory)
LT1109A	2	20	1	X		320					X	X	X	8	X	5V to 12V VPP, 120mA (Flash Memory)
LT1110	1	15	1	X	X	350		X			X	X	X	8	X	1 Cell to 5V, 40mA
LT1111	2	30	1	X	X	300		X			X	X	X	8	X	2 Cells to 5V, 90mA
LTC1142	6	16	Ext.		X	320	X		0	X	X			16	X	6-8 Cells to both 5V and 3.3V
LTC1142HV	6	20	Ext.		X	320	X		0	X	X			28	X	8-10 Cells NiCad to 5V and 3.3V or ADJ
LTC1143	6	16	Ext.		X	320	X		0	X	X			28	X	6-8 Cells to both 5V and 3.3V
LTC1147	6	16	Ext.		X	160	X		0	X	X			8	X	6-8 Cells NiCd to 5V or 3.3V or ADJ at 1A+
LTC1148	6	16	Ext.		X	160	X		0	X	X		X	14	X	6-8 Cells NiCd to 5V or 3.3V at 2A
LTC1148HV	6	20	Ext.		X	160	X		0	X	X		X	14	X	8-10 Cells NiCd to 5V or 3.3V at 2A
LTC1149	7	48	Ext.		X	600	X		2	X	X		X	16	X	≥8 Cells NiCd to 5V or 3.3V at 2A
LTC1159	5	40	Ext.		X	300	X		0	X	X	X	X	16	X	≥6 Cells NiCd to 5V or 3.3V at 2A
LT1173	2	30	1	X	X	110		X			X	X	X	8	X	2 Cells to 5V, 90mA
LTC1174	3.5	13.5	0.6		X	450	X	X	0.5	X	X		X	8	X	9V to 5V at up to 400mA5
LTC1265	3.5	13.5	1		X	160	X	X	0.5	X	X		X	14	X	9V to 5V at 800mA
LTC1266	3.5	20	Ext.		X	170	X	X	0	X	X		X	16	X	5V to 3.3V at 10A
LTC1267	4	40	Ext.		X	300	X		0	X	X		X	28	X	>8 Cells NiCad to 5V and 3.3V or ADJ
LT1300	2	6	1	X		120	X			X	X			8	X	2 Cells to 3.3V or 5V at 250mA
LT1301	2	6	1	X		120	X				X	X		8	X	2 Cells to 5V or 12V at 220mA or 50mA
LT1302	2	10	2	X		200	X						X	8	X	2 Cells to 5V at 600mA
LT1303	2	6	1	X		120	X	X			X		X	8	X	2 Cells to 5V at 220mA
LT1304	2	6	1	X		120	X	X		X	X		X	8	X	2 Cells to 5V at 220mA, LBD Active in Shutdown
LT1305	2	6	2	X		120	X	X					X	8	X	Ideal for EL panel supply
LT1309	3.3	5	0.5	X		500	X					X		8	X	3.3V or 5V to 12V VPP (PCMCIA)
LTC1574	4	16	0.6		X	450	X	X	X	X	X		X	16	X	9V to 5V at up to 400mA. No External Schottky Diode Needed.

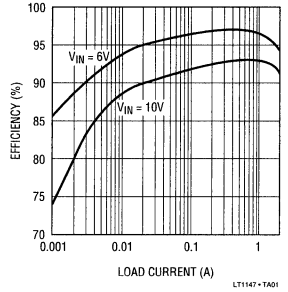
ULTRA-HIGH EFFICIENCY REGULATORS WITH Burst Mode™ OPERATION

- Very High Efficiency: Over 95% Possible
- Current-Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over 3 Decades of Output Current
- Short-Circuit Protection
- Very Low Dropout Operation (100% Duty Cycle)
- Dual 3.3V and 5V Outputs (LTC1142 and LTC1143)

Burst Mode is a trademark of Linear Technology Corporation.

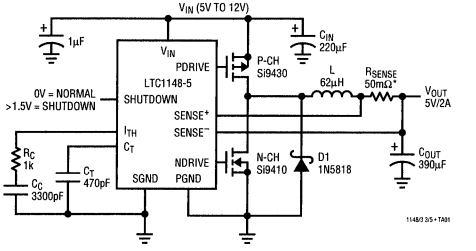
LTC1147: Up to 95% Efficient Step-Down Regulator in 8-Pin SO
LTC1143: Dual Output (3.3V/5V), Up to 95% Efficiency Step-Down Regulator in 16-Pin SO

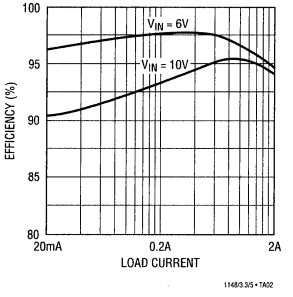




- Low 160µA Standby Current at Light Loads
- Logic Controlled Micropower Shutdown (I_Q < 20µA)
- Wide V_{IN} Range: 4V to 16V
- Low Number of External Parts
- Output Can Be Externally Held High in Shutdown
- LTC1147 Available in 8-Pin Narrow SO Package
- LTC1147L for Low Dropout 3.3V Applications
- LTC1265 for 1.25A Internal PFET

LTC1148: 95% Efficient 3.3V or 5V Battery-Powered Regulator (Synchronous Rectifier)
LTC1142: Dual Output (3.3V/5V), 95% Efficient Regulator in SSOP Package

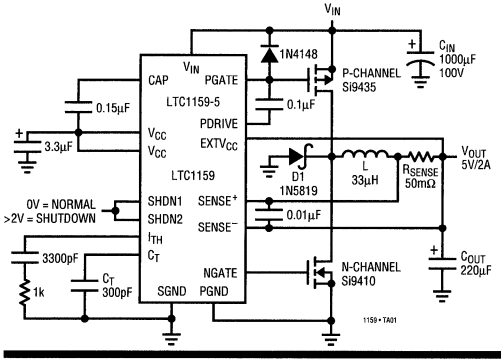


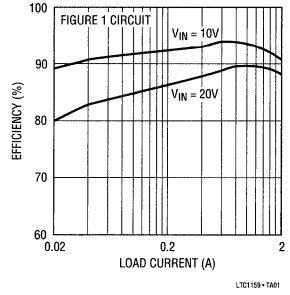


- 160µA Standby Current at Light Loads
- Micropower Shutdown: I_Q < 20µA
- Wide V_{IN} Range: 4V to 18V
- Short-Circuit Protection
- Very Low Dropout Operation
- Adaptive Non-Overlap Gate Drives
- Output Can be Externally Held High in Shutdown
- LTC1148 Available in 14-Pin Narrow SO Package
- LTC1148L for Low Dropout 3.3V Applications

For High Current 5V to 3.3V, See LTC1266 All N-Channel Solution

LTC1159: Highest Efficiency for V_{IN} Up to 40V, 3.3V or 5V Output (Synchronous Rectifier)
LTC1267: Dual Output (3.3V/5V or Adjustable) in SSOP Package





- Wide V_{IN} Range: 4V to 40V
- Logic-Controlled Micropower Shutdown
- Adaptive Non-Overlap Gate Drives
- Available in 16-Lead Narrow SO Package
- 250µA Operating Current
- 20µA Shutdown Current

The following tables form a shortform component selection guide for a collection of commonly used battery-powered DC/DC conversion applications. No design is required since inductor, capacitor and resistor values are completely specified. Choose the appropriate LTC DC/DC converter for your application from the following tables.

The LT1073, LT1107, LT1108, LT1110, LT1111, LT1173, LTC1174, LT1303, and LT1304 all have low-battery detection capability.

Step-Up From One Cell (1V)

V_{OUT} (V)	I_{OUT} (mA)	DEVICE	I_Q (µA)	L (µH)	C (µF)	R (Ω)	FIG	COMMENTS
5	40	LT1073-5	95	82	100	0	1	Lowest I_Q
	40	LT1110-5	350	27	33	0	1	Best For Surface Mount
12	15	LT1073-12	95	82	100	0	1	Lowest I_Q
	15	LT1110-12	350	27	33	0	1	Best For Surface Mount

Adjustable versions also available for V_{OUT} up to 50V

Step-Up From Two Cells (2V)

V_{OUT} (V)	I_{OUT} (mA)	DEVICE	I_Q (µA)	L (µH)	C (µF)	R (Ω)	FIG	COMMENTS
3.3	400	LT1300**	120	10	100	–	2	Selectable 3.3V/5V Out
5	90	LT1173-5	110	47	100	47	1	Lowest I_Q
		LT1111-5	300	18	33	47	1	Surface Mount
	150	LT1107-5	300	33	33	47	1	Surface Mount
		LT1108-5	110	100	100	47	1	Lowest I_Q
	220	LT1300**	120	10	100	–	2	Selectable 3.3V/5V Out
		LT1301**	120	10	100	–	2	Selectable 5V/12V Out
	600	LT1302	200	10	100	–	*	Highest Power Output
12	20	LT1173-12	110	47	47	47	1	Lowest I_Q
		LT1111-12	300	18	22	47	1	Surface Mount
	40	LT1107-12	300	27	33	47	1	Surface Mount
		LT1108-12	110	82	100	47	1	Lowest I_Q
	50	LT1301**	120	10	100	–	2	Selectable 5V/12V Out
	120	LT1302	200	3.3	66	–	*	Highest Power Output
		LT1305	120	10	100	–	2	High Power Output

*See LT1302 data sheet **For low-battery detection use LT1303 or LT1304

Step-Up From 5V To 12V

V_{OUT} (V)	I_{OUT} (mA)	DEVICE	I_Q (µA)	L (µH)	C (µF)	R (Ω)	FIG	COMMENTS
12	90	LT1173-12	110	120	100	0	1	Lowest I_Q
		LT1111-12	300	47	33	0	1	Surface Mount
	175	LT1107-12	300	60	32	0	1	Surface Mount
		LT1108-12	110	180	100	0	1	Lowest I_Q
	200	LT1301**	120	33	47	–	2	True Shutdown
	250	LT1373	1000	22	47	–	***	Fixed Frequency

For low-battery detection use LT1303 or LT1304 * See data sheet

Flash Memory VPP (12V) Generation

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)	DEVICE	I_Q (µA)	L (µH)	C (µF)	FIG	COMMENTS
5	12	60	LT1109-12	320	33	22	3	Small, SMT
		120	LT1109A-12	320	27	47	3	Small, SMT
		200	LT1301**	120	27	47	2	True Shutdown
2 Cells	12	60	LT1109A-12	320	10	22	1	All Surface Mount
		80	LT1301**	120	10	47	2	True Shutdown

**For low-battery detection use LT1303 or LT1304

Basic Step-Up Converters

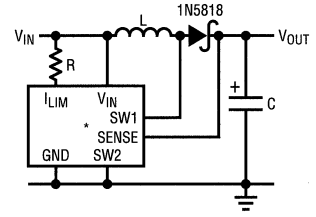
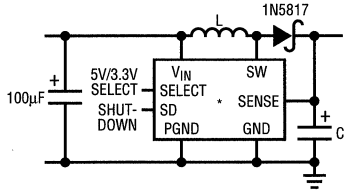


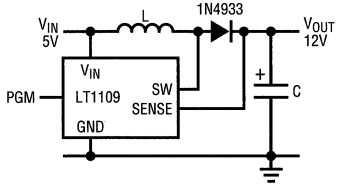
Figure 1



*SEE TABLES FOR RECOMMENDED PART, INDUCTOR, CAPACITOR, AND RESISTOR VALUES

Figure 2

Flash Memory VPP Generator



*SEE TABLE FOR RECOMMENDED INDUCTOR AND CAPACITOR VALUES

Figure 3

Step-Down Conversion to 3.3V

V_{IN} (V)	I_{OUT} (mA)	DEVICE	I_Q (μA)	L (μH)	C (μF)	I_{PGM}	Fig	COMMENTS
4.5 to 12.5	200 425	LTC1174-3.3	450 450	50 50	2 × 33 2 × 33	To GND To V_{IN}	5 5	Low Dropout, Surface Mount
4.5 to 12.5	200 425	LTC1574-3.3	450 450	50 50	2 × 33 2 × 33	To GND To V_{IN}	5 5	Low Dropout, SMT No External Diode
5 to 16	2A	LTC1148-3.3	160	–	–	–	–	See Ultra-High Efficiency Regs – Pg 4
12 to 60	2A	LTC1149-3.3	600	–	–	–	–	See Ultra-High Efficiency Regs – Pg 4

Step-Down Conversion to 5V

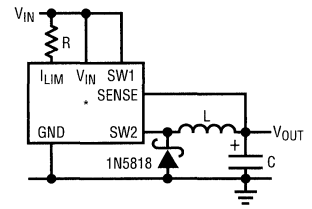
V_{IN} (Max)	I_{OUT} (mA)	DEVICE	I_Q (μA)	L (μH)	C (μF)	R/ I_{PGM}	Fig	COMMENTS
5.5 to 12	200 400	LTC1174-5	450 450	100 100	2 × 33 2 × 33	To GND To V_{IN}	5 5	Low Dropout, Surface Mount
5.5 to 16	200 400	LTC1574-5	450 450	100 100	2 × 33 2 × 33	To GND To V_{IN}	5 5	Low Dropout, SMT No External Diode
12 to 20	300 300	LT1107-5 LT1108-5	300 110	60 180	100 330	100 100	4 4	Surface Mount Lowest I_Q
20 to 30	300 300	LT1173-5 LT1111-5	110 300	470 180	470 220	100 100	4 4	Lowest I_Q Surface Mount
6 to 16	2A+	LTC1147/8-5	160	–	–	–	–	See Ultra-High Efficiency Regs – Pg 4
12 to 60	2A+	LTC1149-5	600	–	–	–	–	See Ultra-High Efficiency Regs – Pg 4

Adjustable output voltages up to 6.2V can be obtained with the adjustable versions of LT1173, LT1111, LT1107, LT1108, or LT1110.

Positive-to-Negative Voltage Conversion

V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)	DEVICE	I_Q (μA)	L (μH)	C (μF)	R (Ω)	Fig	COMMENTS
5	–5	75	LT1108-5 LT1107-5	110 300	100 33	100 33	100 100	6 6	Lowest I_Q Surface Mount
		150	LTC1174-5	450	50	2 × 33	–	7	Surface Mount
12	–5	250 250	LT1173-5 LT1111-5	110 300	470 180	220 82	100 100	6 6	Lowest I_Q Surface Mount
4 8 12.5	–5	110 170 235	LTC1574-5	450	50	100	–	7	SMT, No Ext. Schottky Diode Required

Step-Down Converters



*SEE TABLES FOR RECOMMENDED PART, INDUCTOR, CAPACITOR, AND RESISTOR VALUES

Figure 4

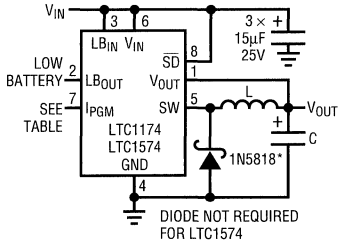
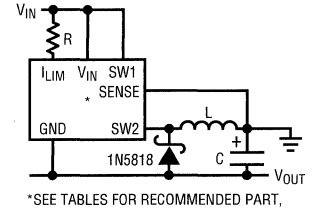


Figure 5

Positive-to-Negative Converters



*SEE TABLES FOR RECOMMENDED PART, INDUCTOR, CAPACITOR, AND RESISTOR VALUES

Figure 6

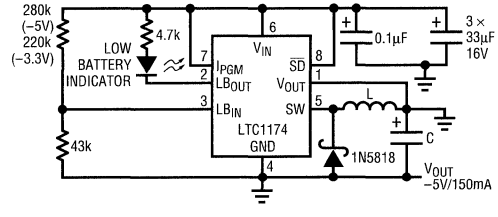


Figure 7

PCMCIA, POWER AND MOTOR CONTROL CIRCUITS

High Side Switch Drivers

LTC1153 – Electronic Circuit Breaker w/ Programmable Trip, Reset, Current Level
LTC1154 – Single N-Ch FET Switch Driver w/ Short-Circuit Protection
LTC1155 – Dual N-Ch FET Switch Drivers w/ Short-Circuit Protection
LTC1156 – Quad N-Ch FET Switch Drivers w/ Short-Circuit Protection
LTC1157 – Dual N-Ch FET Switch Drivers for 3.3V Operation (Also for Low Cost 5V Applications)
LT1161 – Quad High Voltage N-Channel FET Switch Drivers with Reset and Short-Circuit Portection
LTC1163 – Triple N-Ch FET Switch Drivers for 1.8V Operation (and up to 5V Applications)
LTC1165 – Triple N-Ch FET Switch Drivers for 1.8V Operation (and up to 5V Applications)
LTC1177 – UL Recognized Isolated MOSFET Driver
LTC1255 – Dual N-Ch FET Switch Drivers w/ Short Circuit Protection, 24V Operation

Integrated High Side Switches

LT1188 – 1.5A HSS, Output Protected Against Inductive Kickback Controlled Slew Rate/Low RF Noise STATUS Line for Diagnostics Protected Against Overtemp, Load Faults
LT1089 – 7.5A HSS Low Loss, Only 1.5V at 7.5A Protected Against Overtemp, Overcurrent Low Quiescent Current
LTC1477/78 – Single/Dual Protected 1.5A HSS. Low 0.07Ω ON Resistance, Operates From 2.7V to 5.5V, No Parasitic Body Diode

Half-/Full-Bridge N-Ch MOSFET Drivers

LT1158 – 5V to 30V Operation, Drives DC Motors and Switching Power Supply N-Ch MOSFET Switch Gates, On-Chip Charge Pump, Adaptive Anti-Shoot-Through, Fully Protected, 150ns Transition Times Driving 3000pF
LT1160 – 10V to 60V Operation, Drives DC Motors and Switching Power Supply N-CH MOSFET Switch Gates, Adaptive Anti-Shoot Through, 180ns Transition Times Driving 10,000pF
LT1162 – Full-Bridge Version of LT1160

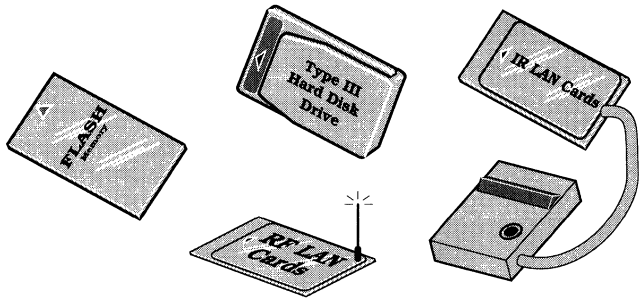
PRODUCT	PACKAGES	FUNCTION	MIN V_{SUPPLY}	MAX V_{IN}	COMMENTS
LT1089	TO-220, TO-3	7.5A High-Side Switch	4V	20V	Low loss, Low I_Q
LT1106	20-Pin TSSOP	VPP Flash Memory Supply	5V	7V	500kHz Operation, 1.1mm Component Height
LTC1153	8-Pin DIP, SO	Electronic Circuit Breaker	4.5V	22V	Has Adjustable Reset Time
LTC1154	8-Pin DIP, SO	Single High Side Driver	4.5V	22V	Single Version of LTC1155
LTC1155	8-Pin DIP, SO	Dual High Side Driver	4.5V	22V	Good for Power Management
LTC1156	16-Pin DIP, SO	Quad High Side Driver	4.5V	22V	Good for Multiple Supply Switching
LTC1157	8-Pin DIP, SO	Dual 3.3V High Side Driver	2.7V	7V	Good for 3.3V Power Management
LT1158	16-Pin DIP, SO	Half-Bridge Driver	4.5V	36V	Synchronous Switching Regulators Too
LT1160	14-Pin DIP, SO	Half-Bridge Driver	10V	60V	Dual N-Channel MOSFET Driver
LT1161	20-Pin DIP, SO	Quad High Side Driver	8V	60V	Good for Industrial (24V) Applications
LT1162	24-Pin DIP, SO	Full-Bridge Driver	10V	60V	Dual Version of LT1160
LTC1163	8-Pin DIP, SO	Triple High Side Driver	1.8V	6V	Good for 2-Cell Power Management
LTC1165	8-Pin DIP, SO	Triple High Side Driver	1.8V	6V	Inverted Logic Version of LTC1163
LTC1177	18-Pin SO Wide	Isolated MOSFET Driver	5/12	—	No Secondary Power Required. UL Recognized
LT1188	TO-220, TO-3	1.5A High Side Switch	5V	30V	Good for Automotive
LTC1255	8-Pin DIP, SO	Dual High Side Driver	9V	30V	Good for Industrial (24V) Applications
LT1312	8-Pin SO	Single VPP Regulator	13V	20V	SafeSlot™ Protection, Low I_Q
LT1313	16-Pin SO	Dual VPP Regulator	13V	20V	SafeSlot Protection, Low I_Q
LTC1314	14-Pin SO	Single VPP Switch/V_{CC} Driver	5V	13.2V	Drives Low Cost N-Channels, Low 0.1μA I_Q
LTC1315	24-Pin SSOP	Dual VPP Switch/V_{CC} Driver	5V	13.2V	Drives Low Cost N-Channels, Low 0.1μA I_Q
LTC1470	8-Pin SO	Protected V_{CC} 5V/3V Switch	5V	—	Internal 1A MOSFET Switches
LTC1471	16-Pin SO	Dual Protected V_{CC} Switch	5V	—	Internal 1A MOSFET Switches
LTC1472	16-Pin SO	Single VPP/V_{CC} Switch	5V	—	Internal VPP and V_{CC} MOSFET Switches

SafeSlot is a trademark of Linear Technology Corporation

Host

PCMCIA Power Switching Solutions
V_{CC}: 3.3V or 5V
VPP: 0V, V_{CC}, 12V, High-Z

Cards



On-Card DC/DC Conversion Solutions
(See pages 3-23 to 3-26)

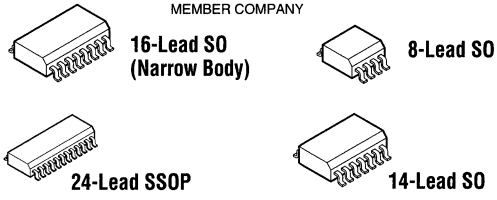
PC Card Host Power Interface

Linear Technology PCMCIA Product Family

DEVICE	DESCRIPTION	PACKAGE
LT1312	Single PCMCIA VPP Driver/Regulator	8-Pin SO
LT1313	Dual PCMCIA VPP Driver/Regulator	16-Pin SO*
LTC1314	Single PCMCIA Switch Matrix	14-Pin SO
LTC1315	Dual PCMCIA Switch Matrix	24-Pin SSOP
LTC1470	Protected V_{CC} 5V/3.3V Switch Matrix	8-Pin SO
LTC1471	Dual Protected V_{CC} 5V/3.3V Switch Matrix	16-Pin SO*
LTC1472	Protected V_{CC} and VPP Switch Matrix	16-Pin SO*

Narrow Body

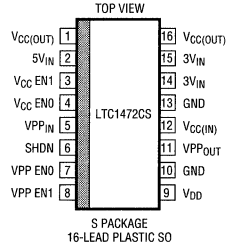
PCMCIA
PC Card
MEMBER COMPANY

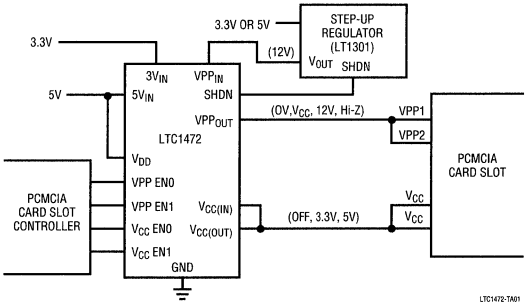


(Packages Enlarged for Clarity)

LTC1472 Protected PCMCIA V_{CC} and VPP Switching Matrix

- Both V_{CC} and VPP Switching in a Single Package
- Built-In SafeSlot™ Current Limit and Thermal Shutdown
- 16-Pin (Narrow) SO Package
- Inrush Current Limited (Drives 150µF Loads)
- Continuous 12V Power Not Required
- Extremely Low $R_{DS(ON)}$ NMOS Switches
- Guaranteed 1A V_{CC} Current and 120mA VPP Current
- 1µA Quiescent Current in Standby
- No External Components Required
- Compatible with Industry Standard Controllers
- Break-Before-Make Switching
- Controlled Rise and Fall Times
- Compatible with Cirrus Logic CL-PD6720, Intel 365-type and Other PCMCIA Host Adaptor Chips





V_{CC} Switch Truth Table

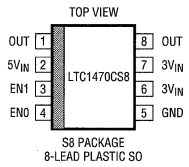
V_{CC} ENO	V_{CC} EN1	$V_{CC(OUT)}$
0	0	Off
1	0	5V
0	1	3.3V
1	1	Off

VPP Switch Truth Table

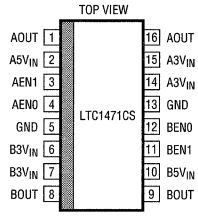
VPP ENO	VPP EN1	VPP_{OUT}
0	0	0V
0	1	$V_{CC(IN)}$
1	0	VPP_{IN}
1	1	Hi-Z

LTC1470/LTC1471 Single/Dual PCMCIA Protected 5V/3.3V V_{CC} Switch

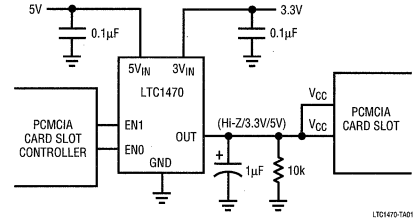
- 3.3V/5V Switching in 8-Pin SO Package
- Built-In SafeSlot Current Limit and Thermal Shutdown
- Extremely Low $R_{DS(ON)}$ MOSFET Switches
- 1A Output Current Capability
- 1μA Quiescent Current in Standby
- Built-In Charge Pump (No 12V Required)
- Compatible with Industry Standard Controllers
- Break-Before-Make Switching
- Controlled Rise and Fall Times
- Logic Compatible with Standard PCMCIA Controllers
- LTC1470 (Single) and LTC1471 (Dual)



S8 PACKAGE
8-LEAD PLASTIC SO

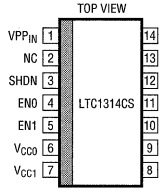


S PACKAGE
16-LEAD NARROW PLASTIC SO

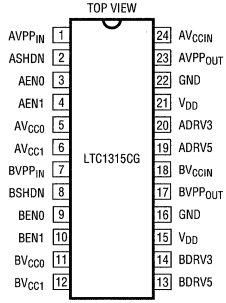


LTC1314/LTC1315 Single/Dual PCMCIA Switching Matrix with Built-In N-Channel MOSFET V_{CC} Switch Drivers

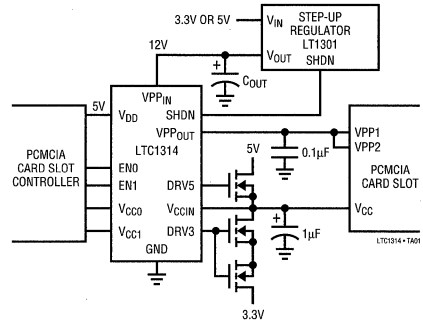
- Output Current Capability: 120mA
- 12V Regulator Can Be Shut Down
- Built-In N-Channel V_{CC} Switch Drivers
- Digital Selection of 0V, $V_{CC(IN)}$, VPP_{IN} or Hi-Z
- 3.3V or 5V V_{CC} Supply
- Break-Before-Make Switching
- 0.1μA Quiescent Current in Hi-Z or 0V Mode
- No VPP_{OUT} Overshoot
- Logic Compatible with Standard PCMCIA Controllers
- LTC1314 (Single) and LTC1315 (Dual)



S PACKAGE
14-LEAD PLASTIC SO

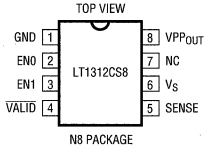


G PACKAGE
24-LEAD PLASTIC SSOP

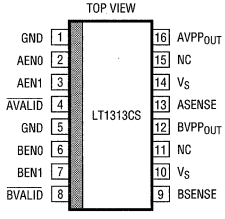


LT1312/LT1313 Single/Dual PCMCIA V_{CC} Driver/Regulator

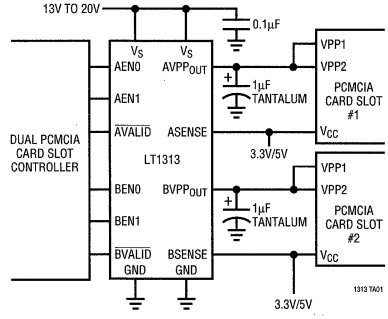
- Digital Selection of 0V, V_{CC}, 12V or Hi-Z
- Output Current Capability: 120mA
- Internal Current Limiting and Thermal Shutdown
- Automatic Switching from 3.3V to 5V
- Powered from Unregulated 13V to 20V Supply
- Logic Compatible with Standard PCMCIA Controllers
- Output Capacitors: 1μF
- Quiescent Current in Hi-Z or 0V Mode: 60μA
- Independent VPP Valid Status Feedback Signals
- No VPP Overshoot



N8 PACKAGE
8-LEAD PDIP
S8 PACKAGE
8-LEAD PLASTIC SO



S PACKAGE
16-LEAD NARROW PLASTIC SO



LINEAR TECHNOLOGY

SECTION 4—POWER PRODUCTS

Switched Capacitor Regulated Voltage Inverter

FEATURES

- **Regulated Negative Voltage from a Single Positive Supply**
- **Can Provide Regulated –5V from a 3V Supply**
- **REG Pin Indicates Output is in Regulation**
- Low Output Ripple: 5mV Typ
- Supply Current: 600µA Typ
- Shutdown Mode Drops Supply Current to 5µA
- Up to 15mA Output Current
- Adjustable or Fixed Output Voltages
- Requires Only Three or Four External Capacitors
- Available in SO-8 Packages

APPLICATIONS

- GaAs FET Bias Generators
- Negative Supply Generators
- Battery-Powered Systems
- Single Supply Applications

DESCRIPTION

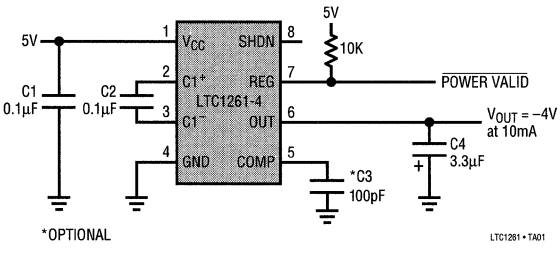
The LTC®1261 is a switched-capacitor voltage inverter designed to provide a regulated negative voltage from a single positive supply. The LTC1261CS operates from a single 3V to 8V supply and provides an adjustable output voltage from –1.25V to –8V. An on-chip resistor string allows the LTC1261CS to be configured for output voltages of –3.5V, –4V, –4.5V or –5V with no external components. The LTC1261CS8 is optimized for applications which use a 5V or higher supply or which require low output voltages. It requires a single external 0.1µF capacitor and provides adjustable and fixed output voltage options in 8-pin SO packages. The LTC1261CS requires one or two external 0.1µF capacitors, depending on input voltage. Both versions require additional external input and output bypass capacitors. An optional compensation capacitor at ADJ/COMP can be used to reduce the output voltage ripple.

Each version of the LTC1261 will supply up to 15mA output current with guaranteed output regulation of 5%. The LTC1261 includes an open-drain REG output which pulls low when the output is within 5% of the set value. Output ripple is typically as low as 5mV. Quiescent current is typically 600µA when operating and 5µA in shutdown.

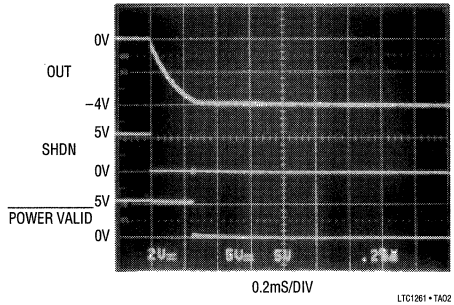
The LTC1261 is available in a 14-pin narrow body SO package and an 8-pin SO package.

TYPICAL APPLICATION

–4V Generator with $\overline{\text{Power Valid}}$



Waveforms for –4V Generator with $\overline{\text{Power Valid}}$

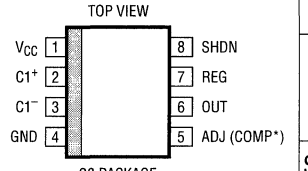


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Note 2) 9V
Output Voltage (Note 5) ..... 0.3V to –9V
Total Voltage, V_{CC} to V_{OUT} (Note 2) 12V
Input Voltage
SHDN Pin ..... –0.3V to V_{CC} + 0.3V
REG Pin ..... –0.3V to 12V
ADJ, R_O, R1, R_{ADJ} ..... V_{OUT} – 0.3V to V_{CC} + 0.3V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

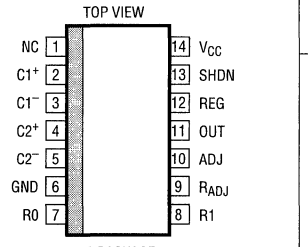
PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO
*FOR FIXED VERSIONS

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1261CS8 LTC1261CS8-4 LTC1261CS8-4.5
S8 PART MARKING
1261 12614 126145



S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1261CS

Consult factory for Industrial or Military grade parts.

4

ELECTRICAL CHARACTERISTICS

V_{CC} = 3V to 6.5V, T_A = 25°C unless otherwise specified.

				0°C ≤ T_A ≤ 70°C			–40°C ≤ T_A ≤ 85°C (Note 7)			
SYMBOL	**PARAMETER**	**CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
VREF	Reference Voltage		●	1.20	1.24	1.28	1.20	1.24	1.28	V
	Supply Current	No Load, SHDN Floating	●		600	1000		600	1500	µA
		No Load, V_{SHDN} = V_{CC}	●		5	20		5	20	µA
fSC	Internal Oscillator Frequency				550			550		kHz
EFF	Power Efficiency				65			65		%
VOL	REG Output Low Voltage	I_{REG} = 1mA	●		0.1	0.8		0.1	0.8	V
IREG	REG Sink Current	V_{REG} = 0.8V, V_{CC} = 3.3V	●	5	8		5	8		mA
		V_{REG} = 0.8V, V_{CC} = 5.0V	●	8	15		8	15		mA
IADJ	Adjust Pin Current	V_{ADJ} = 1.24V	●		0.01	1		0.01	1	µA
VIH	SHDN Input High Voltage		●	2			2			V
VIL	SHDN Input Low Voltage		●			0.8			0.8	V
IIN	SHDN Input Current	V_{SHDN} = V_{CC}	●		5	20		5	25	µA
tON	Turn-On Time	I_{OUT} = 15mA			500			500		µs

ELECTRICAL CHARACTERISTICS

Doubler Mode. V_{CC} = 5V ±10%, C1 = 0.1µF, C2 = 0 (Note 4), C_{OUT} = 3.3µF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		0°C ≤ T_A ≤ 70°C MIN	TYP	MAX	–40°C ≤ T_A ≤ 85°C (Note 7) MIN	TYP	MAX	UNITS
ΔV_{OUT}	Output Regulation	–1.24V ≥ V_{OUT} ≥ –4V, 0 ≤ I_{OUT} ≤ 10mA	●		1	5				%
		–4V ≥ V_{OUT} ≥ –5V, 0 ≤ I_{OUT} ≤ 10mA (Note 6)			2					%
		–1.24V ≥ V_{OUT} ≥ –4V, 0 ≤ I_{OUT} ≤ 8mA	●					1	5	%
		–4V ≥ V_{OUT} ≥ –5V, 0 ≤ I_{OUT} ≤ 8mA (Note 6)						2		%
V_{OUT}	Output Voltage (Note 6)	V_{OUT} Set to –3.5V, 0 ≤ I_{OUT} ≤ 15mA	●	–3.33	–3.5	–3.68	–3.33	–3.5	–3.68	V
		V_{OUT} Set to –4V, 0 ≤ I_{OUT} ≤ 10mA	●	–3.80	–4.0	–4.20				V
		V_{OUT} Set to –4.5V, 0 ≤ I_{OUT} ≤ 10mA	●	–3.80	–4.5	–4.73				V
		V_{OUT} Set to –5V, 0 ≤ I_{OUT} ≤ 10mA		–3.80	–5.0	–5.25				V
		V_{OUT} Set to –4V, 0 ≤ I_{OUT} ≤ 8mA	●				–3.80	–4.0	–4.20	V
		V_{OUT} Set to –4.5V, 0 ≤ I_{OUT} ≤ 8mA	●				–3.80	–4.5	–4.73	V
		V_{OUT} Set to –5V, 0 ≤ I_{OUT} ≤ 8mA					–3.80	–5.0	–5.25	V
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V	●		60	125		60	125	mA
V_{RIP}	Output Ripple Voltage	I_{OUT} = 5mA, V_{OUT} = –4V			10			10		mV

LTC1261CS Only. Tripler Mode. V_{CC} = 2.7V, C1 = C2 = 0.1µF (Note 4), C_{OUT} = 3.3µF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		0°C ≤ T_A ≤ 70°C MIN	TYP	MAX	–40°C ≤ T_A ≤ 85°C (Note 7) MIN	TYP	MAX	UNITS
ΔV_{OUT}	Output Regulation	–1.24V ≥ V_{OUT} ≥ –4V, 0 ≤ I_{OUT} ≤ 5mA	●		1	5		1	5	%
V_{OUT}	Output Voltage	V_{OUT} Set to –3.5V, 0 ≤ I_{OUT} ≤ 6mA	●	–3.33	–3.5	–3.68	–3.33	–3.5	–3.68	V
		V_{OUT} Set to –4V, 0 ≤ I_{OUT} ≤ 5mA	●	–3.80	–4.0	–4.20	–3.80	–4.0	–4.20	V
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V	●		25	75		25	75	mA
V_{RIP}	Output Ripple Voltage	I_{OUT} = 5mA, V_{OUT} = –4V			5			5		mV

LTC1261CS Only. Tripler Mode. V_{CC} = 3.3V ±10%, C1 = C2 = 0.1µF (Note 4), C_{OUT} = 3.3µF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		0°C ≤ T_A ≤ 70°C MIN	TYP	MAX	–40°C ≤ T_A ≤ 85°C (Note 7) MIN	TYP	MAX	UNITS
ΔV_{OUT}	Output Regulation	–1.24V ≥ V_{OUT} ≥ –4V, 0 ≤ I_{OUT} ≤ 12mA	●		1	5		1	5	%
		–4V ≥ V_{OUT} ≥ –5V, 0 ≤ I_{OUT} ≤ 8mA	●		2	5		2		%
V_{OUT}	Output Voltage	V_{OUT} Set to –3.5V, 0 ≤ I_{OUT} ≤ 15mA	●	–3.33	–3.5	–3.68	–3.33	–3.5	–3.68	V
		V_{OUT} Set to –4V, 0 ≤ I_{OUT} ≤ 12mA	●	–3.80	–4.0	–4.20	–3.80	–4.0	–4.20	V
		V_{OUT} Set to –4.5V, 0 ≤ I_{OUT} ≤ 10mA	●	–4.28	–4.5	–4.73	–4.28	–4.5	–4.73	V
		V_{OUT} Set to –5V, 0 ≤ I_{OUT} ≤ 8mA	●	–4.75	–5.0	–5.25				V
		V_{OUT} Set to –5V, 0 ≤ I_{OUT} ≤ 6mA	●				–4.75	–5.0	–5.25	V
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V	●		35	75		35	75	mA
V_{RIP}	Output Ripple Voltage	I_{OUT} = 5mA, V_{OUT} = –4V			5			5		mV

LTC1261CS Only. Tripler Mode. V_{CC} = 5V ±10%, C1 = C2 = 0.1µF (Note 4), C_{OUT} = 3.3µF unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS (Note 2)		0°C ≤ T_A ≤ 70°C MIN	TYP	MAX	–40°C ≤ T_A ≤ 85°C (Note 7) MIN	TYP	MAX	UNITS
ΔV_{OUT}	Output Regulation	–1.24V ≥ V_{OUT} ≥ –4V, 0 ≤ I_{OUT} ≤ 12mA	●		1	5		1	5	%
		–4V ≥ V_{OUT} ≥ –5V, 0 ≤ I_{OUT} ≤ 10mA	●		2	5		2	5	%
V_{OUT}	Output Voltage	V_{OUT} Set to –3.5V, 0 ≤ I_{OUT} ≤ 15mA	●	–3.33	–3.5	–3.68	–3.33	–3.5	–3.68	V
		V_{OUT} Set to –4V, 0 ≤ I_{OUT} ≤ 12mA	●	–3.80	–4.0	–4.20	–3.80	–4.0	–4.20	V
		V_{OUT} Set to –4.5V, 0 ≤ I_{OUT} ≤ 10mA	●	–4.28	–4.5	–4.73	–4.28	–4.5	–4.73	V
		V_{OUT} Set to –5V, 0 ≤ I_{OUT} ≤ 10mA	●	–4.75	–5.0	–5.25	–4.75	–5.0	–5.25	V
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V	●		70	125		70	125	mA
V_{RIP}	Output Ripple Voltage	I_{OUT} = 5mA, V_{OUT} = –4V			7			7		mV

LECTRICAL CHARACTERISTICS

ɜ ● denotes specifications which apply over the full operating ıperature range.

te 1: The absolute maximum ratings are those values beyond which the of a device may be impaired.

te 2: All currents into device pins are positive; all currents out of device s are negative. All voltages are referenced to ground unless otherwise ɔcified.

te 3: All typicals are given at T_A = 25°C.

te 4: C1 = C2 = 0.1µF means the specifications apply to tripler mode ere $V_{CC} - V_{OUT} = 3V_{CC}$ (LTC1261CS only; the LTC1261CS8 cannot be ınected in tripler mode) with C1 connected between $C1^+$ and $C1^-$ and connected between $C2^+$ and $C2^-$. C2 = 0 implies doubler mode where $V_{CC} - V_{OUT} = 2V_{CC}$; for the LTC1261CS this means C1 connects from $C1^+$ to $C2^-$ with $C1^-$ and $C2^+$ floating. For the LTC1261CS8 in doubler mode, C1 connects from $C1^+$ to $C1^-$; there are no C2 pins.

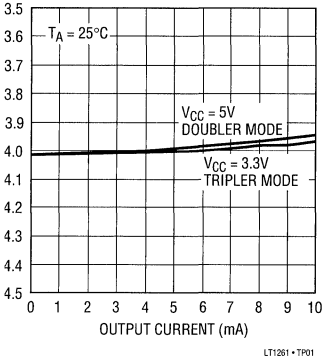
Note 5: Setting output to <–7V will exceed the absolute voltage maximum rating with a 5V supply. With supplies higher than 5V, the output should never be set to exceed V_{CC} – 12V.

Note 6: For output voltages below –4.5V the LTC1261 may reach 50% duty cycle and fall out of regulation with heavy load or low input voltages. Beyond this point, the output will follow the input with no regulation.

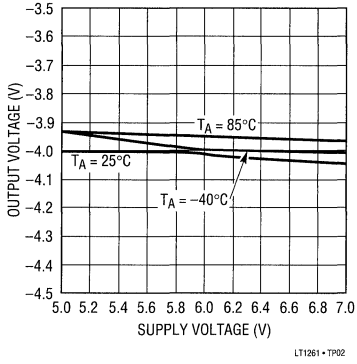
Note 7: This data is guaranteed by correlation and not tested over the –45°C to +85°C temperature range.

YPICAL PERFORMANCE CHARACTERISTICS (See Test Circuits)

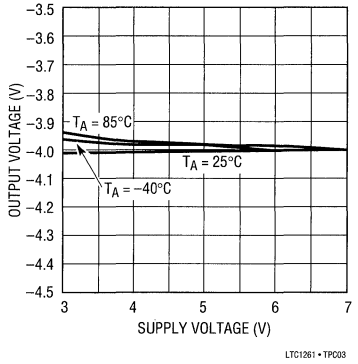
Output Voltage vs Output Current



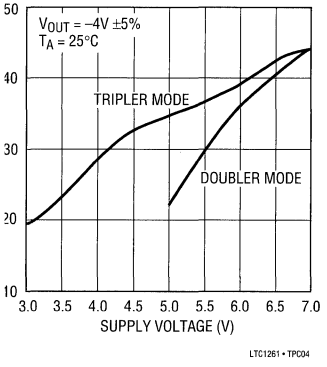
Output Voltage (Doubler Mode) vs Supply Voltage



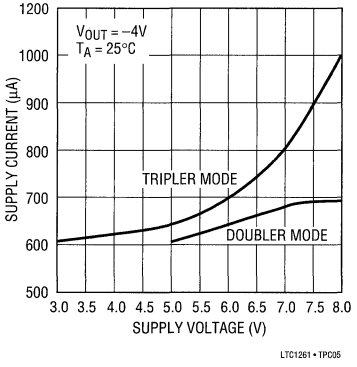
Output Voltage (Tripler Mode) vs Supply Voltage



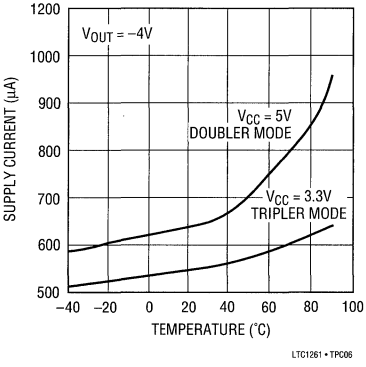
Maximum Output Current vs Supply Voltage



Supply Current vs Supply Voltage

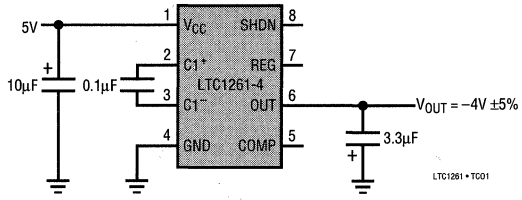


Supply Current vs Temperature

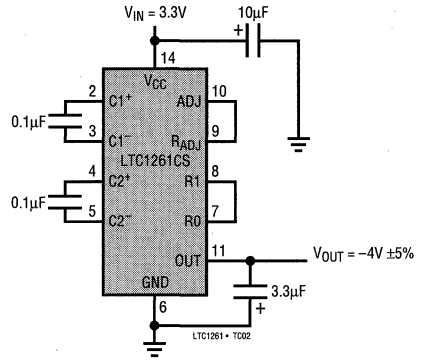


TEST CIRCUITS

Doubler Mode



Tripler Mode



PIN FUNCTIONS

Pin numbers are shown as (LTC1261CS/LTC1261CS8).

NC (Pin 1/NA): No Internal Connection.

C1+ (Pin 2/Pin 2): C1 Positive Input. Connect a 0.1µF capacitor between C1+ and C1–. With the LTC1261CS in doubler mode, connect a 0.1µF capacitor from C1+ to C2–.

C1– (Pin 3/Pin 3): C1 Negative Input. Connect a 0.1µF capacitor from C1+ to C1–. With the LTC1261CS in doubler mode only, C1– should float.

C2+ (Pin 4/NA): C2 Positive Input. In tripler mode connect a 0.1µF capacitor from C2+ to C2–. This pin is used with the LTC1261CS in tripler mode only; in doubler mode this pin should float.

C2– (Pin 5/NA): C2 Negative Input. In tripler mode connect a 0.1µF capacitor from C2+ to C2–. In doubler mode connect a 0.1µF capacitor from C1+ to C2–.

GND (Pin 6/Pin 4): Ground. Connect to a low impedance ground. A ground plane will help to minimize regulation errors.

R0 (Pin 7/NA): Internal Resistor String, 1st Tap. See Table 2 in the Applications Information section for information on internal resistor string pin connections vs output voltage.

R1 (Pin 8/NA): Internal Resistor String, 2nd Tap.

R_{ADJ} (Pin 9/NA): Internal Resistor String Output. Connect this pin to ADJ to use the internal resistor divider. See Table 2 in the Applications Information section fo information on internal resistor string pin connections v output voltage.

ADJ (COMP for fixed versions) (Pin 10/Pin 5): Outpu Adjust/Compensation Pin. For adjustable parts this pin i used to set the output voltage. The output voltage shoul be divided down with a resistor divider and fed back t this pin to set the regulated output voltage. The resisto divider can be external or the internal divider string ca be used if it can provide the required output voltage Typically the resistor string should draw ≥10µA from th output to minimize errors due to the bias current at th adjust pin. Fixed output parts have the internal resisto string connected to this pin inside the package. The pi can be used to trim the output voltage if desired. It ca also be used as an optional feedback compensation pi to reduce output ripple on both adjustable and fixe output voltage parts. See Applications Information sec tion for more information on compensation and outpu ripple.

OUT (Pin 11/Pin 6): Negative Voltage Output. This pi must be bypassed to ground with a 1µF or larger capaci tor; it must be at least 3.3µF to provide specified outpu ripple. The size of the output capacitor has a strong effec on output ripple. See the Applications Information sec tion for more details.

REG (Pin 12/Pin 7): This is an open drain output that pull low when the output voltage is within 5% of the set value

IN FUNCTIONS

will sink 8mA to ground with a 5V supply. The external rcuitry must provide a pull-up or REG will not swing gh. The voltage at REG may exceed V_{CC} and can be ılled up to 12V above ground without damage.

ŀDN (Pin 13/Pin 8): Shutdown. When this pin is at ound the LTC1261 operates normally. An internal 5µA ıll-down keeps SHDN low if it is left floating. When ŀDN is pulled high, the LTC1261 enters shutdown ode. In shutdown the charge pump stops, the output collapses to 0V and the quiescent current drops to 5µA typically.

V_{CC} (Pin 14/Pin 1): Power Supply. This requires an input voltage between 3V and 6.5V. Certain combinations of output voltage and operating mode may place additional restrictions on the input voltage. V_{CC} must be bypassed to ground with at least a 0.1µF capacitor placed in close proximity to the chip. See the Applications Information section for details.

ıPPLICATIONS INFORMATION

ODES OF OPERATION

ıe LTC1261 uses a charge pump to generate a negative ıtput voltage that can be regulated to a value either gher or lower than the original input voltage. It has two odes of operation: a "doubler" inverting mode, which ın provide a negative output equal to or less than the ısitive power supply and a "tripler" inverting mode, ıich can provide negative output voltages either larger or naller in magnitude than the original positive supply. The pler offers greater versatility and wider input range but quires four external capacitors and a 14-pin package. ıe doubler offers the SO-8 package and requires only ree external capacitors.

ıubler Mode

ıubler mode allows the LTC1261 to generate negative ıtput voltage magnitudes up to that of the supply voltage, ɜating a voltage between V_{CC} and OUT of up to two times ;. In doubler mode the LT1261 uses a single flying pacitor to invert the input supply voltage, and the output ltage is stored on the output bypass capacitor between /itch cycles. The LTC1261CS8 is always configured in ıubler mode and has only one pair of flying capacitor ıs (Figure 1a). The LTC1261CS can be configured in ıubler mode by connecting a single flying capacitor tween the $C1^+$ and $C2^-$ pins. $C1^-$ and $C2^+$ should be left ating (Figure 1b).

ipler Mode

e LTC1261CS can be used in a tripler mode which can nerate negative output voltages up to twice the supply voltage. The total voltage between the V_{CC} and OUT pins can be up to three times V_S. For example, tripler mode can be used to generate –5V from a single positive 3.3V supply. Tripler mode requires two external flying capacitors. The first connects between $C1^+$ and $C1^-$ and the second between $C2^+$ and $C2^-$ (Figure 1c). Because of the relatively high voltages that can be generated in this mode, care must be taken to ensure that the total input-to-output voltage never exceeds 12V or the LTC1261 may be damaged. In most applications the output voltage will be kept in check by the regulation loop. Damage is possible however, with supply voltages above 4V in tripler mode and above 6V in doubler mode. As the input supply voltage rises the allowable output voltage drops, finally reaching –4V with an 8.5V supply. To avoid this problem use doubler mode whenever possible with high input supply voltages.

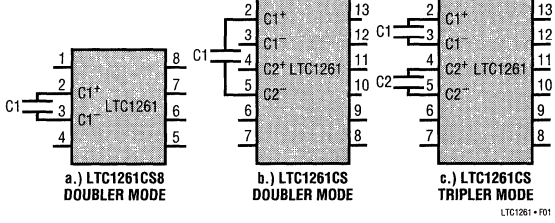


Figure 1. Flying Capacitor Connections

THEORY OF OPERATION

A block diagram of the LTC1261 is shown in Figure 2. The heart of the LTC1261 is the charge pump core shown in the dashed box. It generates a negative output voltage by first

4

APPLICATIONS INFORMATION

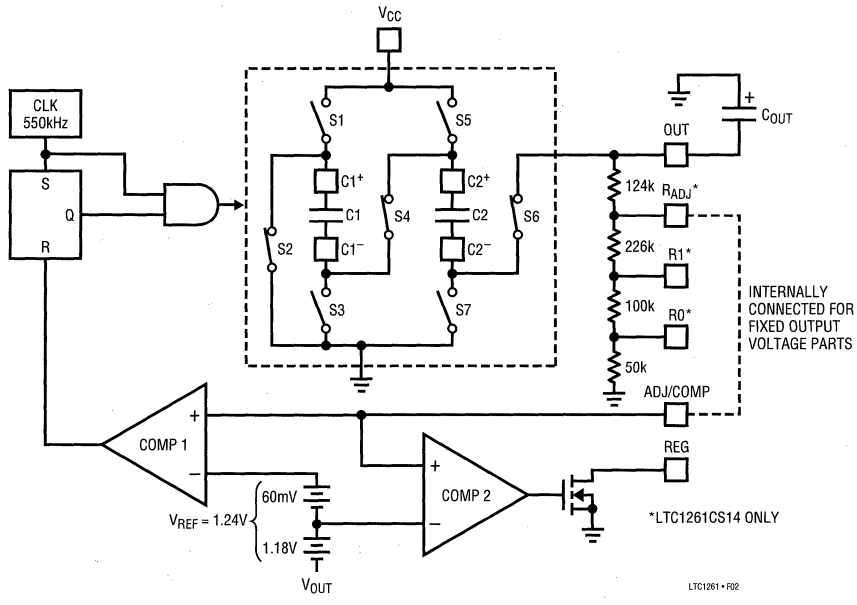


Figure 2. Block Diagram

charging the flying capacitors between V_{CC} and ground. It then stacks the flying capacitors on top of each other and connects the top of the stack to ground forcing the bottom of the stack to a negative voltage. The charge on the flying capacitors is transferred to the output bypass capacitor, leaving it charged to the negative output voltage. This process is driven by the internal clock.

Figure 2 shows the charge pump configured in tripler mode. With the clock low, C1 and C2 are charged to V_{CC} by S1, S3, S5 and S7. At the next rising clock edge, S1, S3, S5 and S7 open and S2, S4 and S6 close, stacking C1 and C2 on top of each other. S2 connects $C1^+$ to ground, S4 connects $C1^-$ to $C2^+$ and $C2^-$ is connected to the output by S6. The charge in C1 and C2 is transferred to C_{OUT}, setting it to a negative voltage. Doubler mode works the same way except that the single flying capacitor (C1) is connected between $C1^+$ and $C2^-$. S3, S4 and S5 don't do anything useful in doubler mode. C1 is charged initially by S1 and S7 and connected to the output by S2 and S6.

The output voltage is monitored by COMP1 which compares a divided replica of the output at ADJ (COMP for fixed output parts) to the internal reference. At the beginning of a cycle the clock is low, forcing the output of the AND gate low and charging the flying capacitors. The next rising clock edge sets the RS latch, setting the charge pump to transfer charge from the flying capacitors to the output capacitor. As long as the output is below the set point, COMP1 stays low, the latch stays set and the charge pump runs at the full 50% duty cycle of the clock gated through the AND gate. As the output approaches the set voltage, COMP1 will trip whenever the divided signal exceeds the internal 1.24V reference relative to OUT. This resets the RS latch and truncates the clock pulses, reducing the amount of charge transferred to the output capacitor and regulating the output voltage. If the output exceeds the set point, COMP1 stays high, inhibiting the RS latch and disabling the charge pump.

COMP2 also monitors the divided signal at ADJ but it is connected to a 1.18V reference, 5% below the main reference voltage. When the divided output exceeds this lower reference voltage indicating that the output is within 5% of the set value, COMP2 goes high turning on the REG output transistor. This is an open drain N-channel device

APPLICATIONS INFORMATION

capable of sinking 5mA with a 3.3V V_{CC} and 8mA with a 5V V_{CC}. When in the "off" state (divided output more than 5% below V_{REF}) the drain can be pulled above V_{CC} without damage up to a maximum of 12V above ground. Note that the REG output only indicates if the magnitude of the output is *below* the magnitude of the set point by 5% (i.e., $V_{OUT} > -4.75V$ for a $-5V$ set point). If the magnitude of the output is forced *higher* than the magnitude of the set point (i.e., to $-6V$ when the output is set for $-5V$) the REG output will stay low.

OUTPUT RIPPLE

Output ripple in the LTC1261 comes from two sources; voltage droop at the output capacitor between clocks and frequency response of the regulation loop. Voltage droop is easy to calculate. With a typical clock frequency of 550kHz, the charge on the output capacitor is refreshed once every 1.8µs. With a 15mA load and a 3.3µF output capacitor, the output will droop by:

$$I_{LOAD} \times \left(\frac{\Delta t}{C_{OUT}}\right) = 15mA \times \left(\frac{1.8\mu s}{3.3\mu F}\right) = 8.2mV$$

This can be a significant ripple component when the output is heavily loaded, especially if the output capacitor is small. If absolute minimum output ripple is required, a 10µF or greater output capacitor should be used.

Regulation loop frequency response is the other major contributor to output ripple. The LTC1261 regulates the output voltage by limiting the amount of charge transferred to the output capacitor on a cycle-by-cycle basis. The output voltage is sensed at the ADJ pin (COMP for fixed output versions) through an internal or external resistor divider from the OUT pin to ground. As the flying capacitors are first connected to the output, the output voltage begins to change quite rapidly. As soon as it exceeds the set point COMP1 trips, switching the state of the charge pump and stopping the charge transfer. Because the RC time constant of the capacitors and the switches is quite short, the ADJ pin must have a wide AC bandwidth to be able to respond to the output in time. External parasitic capacitance at the ADJ pin can reduce the bandwidth to the point where the comparator cannot respond by the time the clock pulse finishes. When this happens the comparator will allow a few complete pulses through, then overcorrect and disable the charge pump until the output drops below the set point. Under these conditions the output will remain in regulation but the output ripple will increase as the comparator "hunts" for the correct value.

To prevent this from happening, an external capacitor can be connected from ADJ (or COMP for fixed output parts) to ground to compensate for external parasitics and increase the regulation loop bandwidth (Figure 3). This sounds counterintuitive until we remember that the internal reference is generated with respect to OUT, not ground.

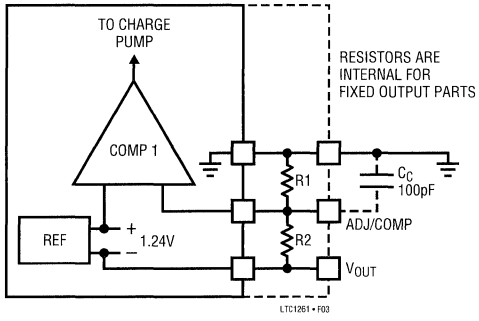


Figure 3. Regulator Loop Compensation

The feedback loop actually sees ground as its "output," thus the compensation capacitor should be connected across the "top" of the resistor divider, from ADJ (or COMP) to ground. By the same token, avoid adding capacitance between ADJ (or COMP) and V_{OUT}. This will slow down the feedback loop and increase output ripple. A 100pF capacitor from ADJ or COMP to ground will compensate the loop properly under most conditions.

OUTPUT FILTERING

If extremely low output ripple (<5mV) is required, additional output filtering is required. Because the LTC1261 uses a high 550kHz switching frequency, fairly low value RC or LC networks can be used at the output to effectively filter the output ripple. A 10Ω series output resistor and a 3.3µF capacitor will cut output ripple to below 3mV (Figure 4). Further reductions can be obtained with larger filter capacitors or by using an LC output filter.

APPLICATIONS INFORMATION

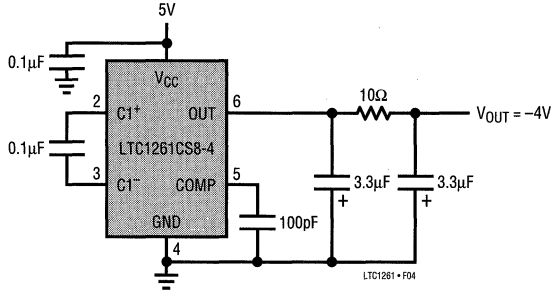


Figure 4. Output Filter Cuts Ripple Below 3mV

CAPACITOR SELECTION

Capacitor Sizing

The performance of the LTC1261 can be affected by the capacitors it is connected to. The LTC1261 requires bypass capacitors to ground for both the V_{CC} and OUT pins. The input capacitor provides most of LTC1261's supply current while it is charging the flying capacitors. This capacitor should be mounted as close to the package as possible and its value should be equal to or larger than the flying capacitor in doubling mode and at least twice the value of the flying capacitors in tripling mode. Ceramic capacitors generally provide adequate performance but avoid using a tantalum capacitor as the input bypass unless there is at least a 0.1µF ceramic capacitor in parallel with it. The charge pump capacitors are somewhat less critical since their peak currents are limited by the switches inside the LTC1261. Most applications should use 0.1µF as the flying capacitor value. Conveniently, ceramic capacitors are the most common type of 0.1µF capacitor and they work well here. Usually the easiest solution is to use the same capacitor type for both the input bypass and the flying capacitors.

In applications where the maximum load current is well-defined and output ripple is critical or input peak currents need to be minimized, the flying capacitor values can be tailored to the application. Reducing the value of the flying capacitors reduces the amount of charge transferred with each clock cycle. This limits maximum output current, but also cuts the size of the voltage step at the output with each clock cycle. The smaller capacitors draw smaller pulses of current out of V_{CC} as well, limiting peak currents and reducing the demands on the input supply. Table 1 shows recommended values of flying capacitor vs maximum load capacity.

Table 1. Typical Max Load (mA) vs Flying Capacitor Value at $T_A = 25°C$, $V_{OUT} = -4V$

FLYING CAPACITOR VALUE (µF)	MAX LOAD (mA) V_{CC} = 5V DOUBLER MODE	MAX LOAD (mA) V_{CC} = 3.3V TRIPLER MODE
0.1	22	20
0.047	16	15
0.033	8	11
0.022	4	5
0.01	1	3

The output capacitor performs two functions: it provides output current to the load during half of the charge pump cycle and its value helps to set the output ripple voltage. For applications that are insensitive to output ripple, the output bypass capacitor can be as small as 1µF. To achieve specified output ripple with 0.1µF flying capacitors, the output capacitor should be at least 3.3µF. Larger output capacitors will reduce output ripple further at the expense of turn-on time.

Capacitor ESR

Output capacitor Equivalent Series Resistance (ESR) is another factor to consider. Excessive ESR in the output capacitor can fool the regulation loop into keeping the output artificially low by prematurely terminating the charging cycle. As the charge pump switches to recharge the output a brief surge of current flows from the flying capacitors to the output capacitor. This current surge can be as high as 100mA under full load conditions. A typical 3.3µF tantalum capacitor has 1Ω or 2Ω of ESR; 100mA × 2Ω = 200mV. If the output is within 200mV of the set point this additional 200mV surge will trip the feedback comparator and terminate the charging cycle. The pulse dissipates quickly and the comparator returns to the correct state, but the RS latch will not allow the charge pump to respond until the next clock edge. This prevents the charge pump from going into very high frequency oscillation under such conditions but it also creates an output error as the feedback loop regulates based on the top of the spike, not the average value of the output (Figure 5). The resulting output voltage behaves as if a resistor of value $C_{ESR} \times (I_{PK}/I_{AVE})\Omega$ was placed in series with the output. To

APPLICATIONS INFORMATION

Avoid this nasty sequence of events connect a 0.1µF ceramic capacitor in parallel with the larger output capacitor. The ceramic capacitor will "eat" the high frequency spike, preventing it from fooling the feedback loop, while the larger but slower tantalum or aluminum output capacitor supplies output current to the load between charge cycles.

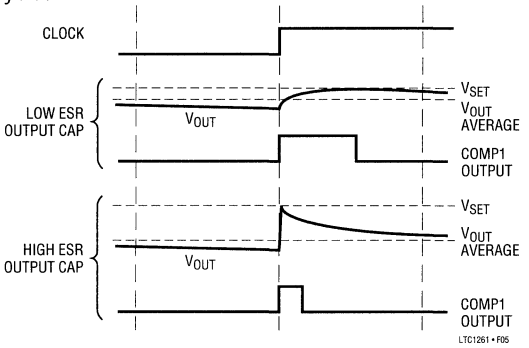


Figure 5. Output Ripple with Low and High ESR Capacitors

Note that ESR in the flying capacitors will not cause the same condition; in fact, it may actually improve the situation by cutting the peak current and lowering the amplitude of the spike. However, more flying capacitor ESR is not necessarily better. As soon as the RC time constant approaches half of a clock period (the time the capacitors have to share charge at full duty cycle) the output current capability of the LTC1261 will begin to diminish. For 0.1µF flying capacitors, this gives a maximum total series resistance of:

$$\frac{1}{2}\left(\frac{t_{CLK}}{C_{FLY}}\right) = \frac{1}{2}\left(\frac{1}{550kHz}\right) / 0.1\mu F = 9.1\Omega$$

Most of this resistance is already provided by the internal switches in the LTC1261 (especially in tripler mode). More than 1Ω or 2Ω of ESR on the flying capacitors will start to affect the regulation at maximum load.

RESISTOR SELECTION

Resistor selection is easy with the fixed output versions of the LTC1261—no resistors are needed! Selecting the right resistors for the adjustable parts is only a little more difficult. A resistor divider should be used to divide the signal at the output to give 1.24V at the ADJ pin *with respect to* V_{OUT} (Figure 6). The LTC1261 uses a positive reference with respect to V_{OUT}, not a negative reference with respect to ground (Figure 2 shows the reference connection). Be sure to keep this in mind when connecting the resistors! If the initial output is not what you expected, try swapping the two resistors.

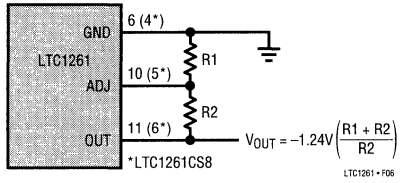


Figure 6. External Resistor Connections

The 14-pin adjustable parts include a built-in resistor string which can provide an assortment of output voltages by using different pin-strapping options at the R0, R1, and R_{ADJ} pins (Table 2). The internal resistors are roughly 124k, 226k, 100k, and 50k (see Figure 2) giving output options of –3.5V, –4V, –4.5V, and –5V. The resistors are carefully matched to provide accurate divider ratios, but the absolute values can vary substantially from part to part. It is not a good idea to create a divider using an external resistor and one of the internal resistors unless the output voltage accuracy is not critical.

Table 2. Output Voltages Using the Internal Resistor Divider

PIN CONNECTIONS	OUTPUT VOLTAGE
ADJ to R_{ADJ}	–5V
ADJ to R_{ADJ}, R0 to GND	–4.5V
ADJ to R_{ADJ}, R1 to R0	–4V
ADJ to R_{ADJ}, R1 to GND	–3.5V
ADJ to R1	–1.77V
ADJ to R0	–1.38V
ADJ to GND	–1.24V

There are some oddball output voltages available by connecting ADJ to R0 or R1 and shorting out some of the internal resistors. If one of these combinations gives you the output voltage you want, by all means use it!

The internal resistor values are the same for the fixed output versions of the LTC1261 as they are for the adjust-

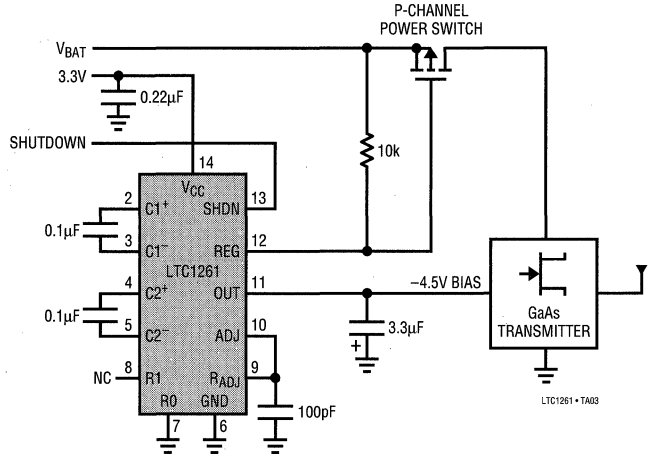
APPLICATIONS INFORMATION

able. The output voltage can be trimmed, if desired, by connecting external resistance from the COMP pin to OUT or ground to alter the divider ratio. As in the adjustable parts, the absolute value of the internal resistors may vary significantly from unit to unit. As a result, the further the trim shifts the output voltage the less accurate the output voltage will be. If a precise output voltage other than one of the available fixed voltages is required, it is better to use an adjustable LTC1261 and use precision external resistors. The internal reference is trimmed at the factory to within 3.5% of 1.24V; with 1% external resistors the output will be within 5.5% of the nominal value, even under worst case conditions.

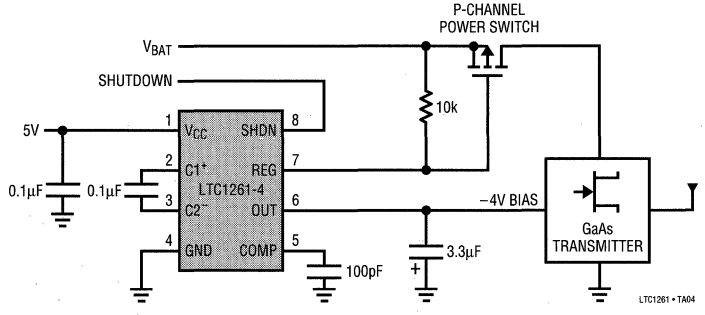
The LTC1261 can be internally configured with nonstandard fixed output voltages. Contact the Linear Technology Marketing Department for details.

TYPICAL APPLICATIONS

3.3V Input, –4.5V Output GaAs FET Bias Generator

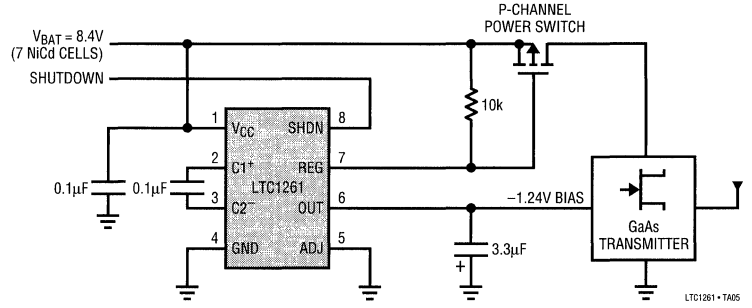


5V Input, –4V Output GaAs FET Bias Generator

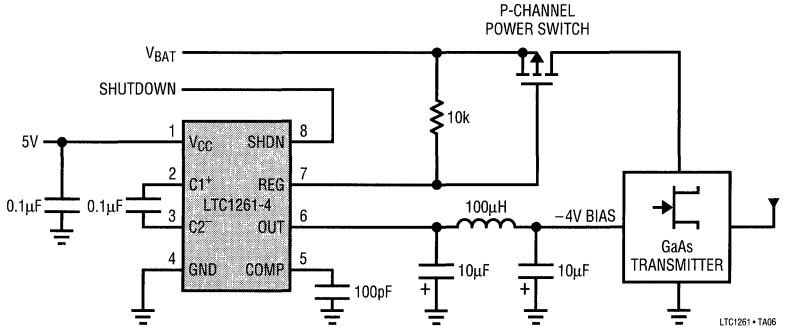


TYPICAL APPLICATIONS

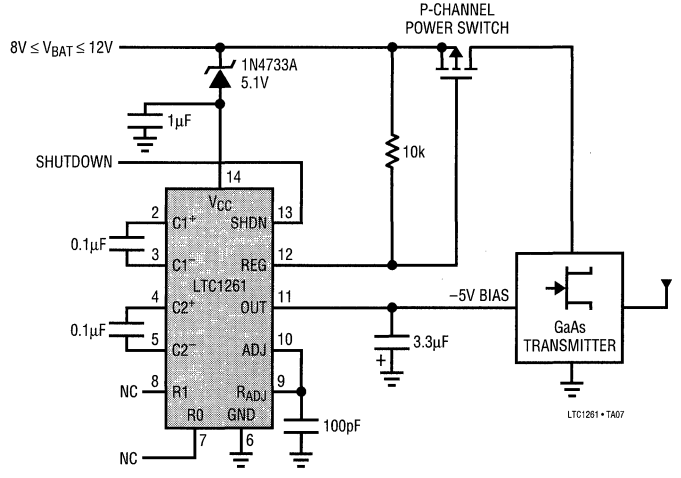
7 Cells to –1.24V Output GaAs FET Bias Generator



1mV Ripple, 5V Input, –4V Output GaAs FET Bias Generator

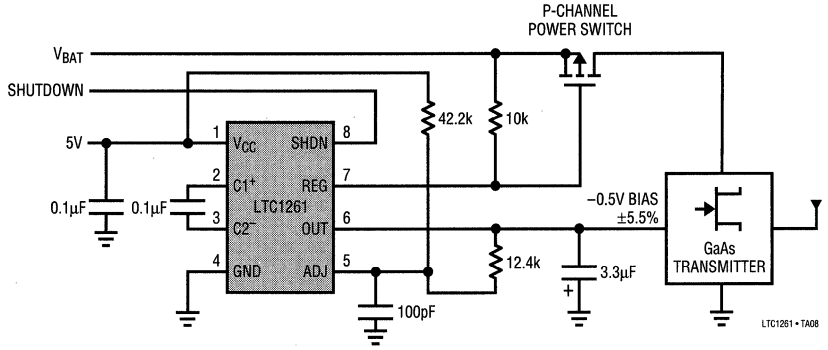


High Supply Voltage, –5V Output GaAs FET Bias Generator

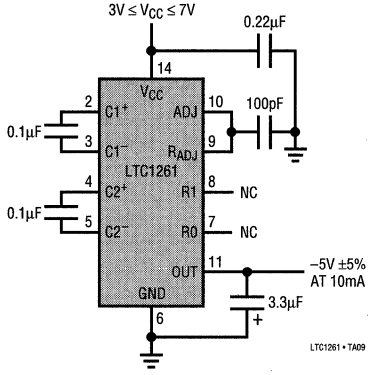


TYPICAL APPLICATIONS

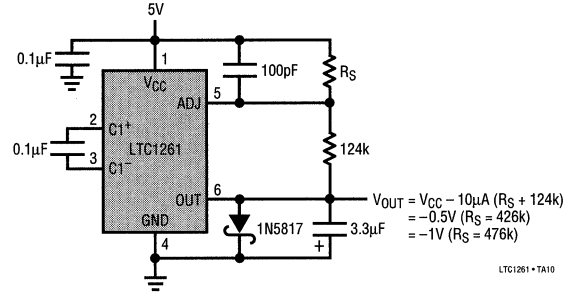
5V Input, –0.5V Output GaAs FET Bias Generator



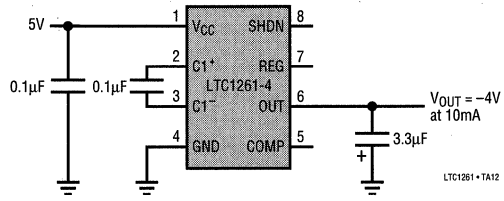
–5V Supply Generator



Low Output Voltage Generator



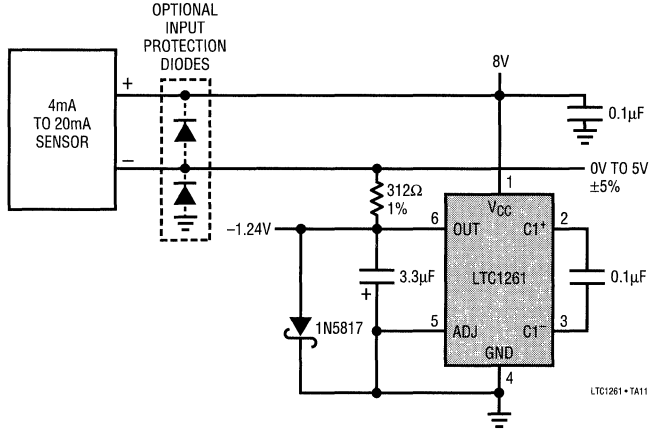
Minimum Parts Count –4V Generator



TYPICAL APPLICATIONS

This circuit uses the LTC1261CS8 to generate a –1.24V output at 20mA. Attached to this output is a 312Ω resistor to make the current/voltage conversion. 4mA through 312Ω generates 1.24V, giving a net 0V output. 20mA through 312Ω gives 6.24V across the resistor, giving a net 5V output. If the 4mA to 20mA source requires an operating voltage greater than 8V, it should be powered from a separate supply; the LTC1261 can then be powered from any convenient supply, $3V \leq V_S \leq 8V$. The Schottky diode prevents the external voltage from damaging the LTC1261 in shutdown or under fault conditions. The LTC1261's reference is trimmed to 3.5% and the resistor adds 1% uncertainty, giving 4.5% total output error.

–1.24V Generator for 4mA-20mA to 0V-5V Conversion



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1550/LTC1551	Low Noise Switched Capacitor Regulated Voltage Inverter	GaAs FET Bias with Linear Regulator 1mV Ripple
LTC1429	Clock Synchronized Switched Capacitor Regulated Voltage Inverter	GaAs FET Bias
LT1121	Micropower Low Dropout Regulators with Shutdown	0.4V Dropout Voltage at 150mA, Low Noise, Switched Capacitor Regulated Voltage Inverter

12V, 30mA Flash Memory Programming Supply

FEATURES

- Regulated 12V ±5% Output Voltage
- **No Inductors**
- Supply Voltage Range: 4.75V to 5.5V
- **Guaranteed 30mA Output**
- **Low Power: I_{CC} = 500µA**
- I_{CC} in Shutdown: 0.5µA
- 8-Pin PDIP or SO-8 Package

APPLICATIONS

- 12V Flash Memory Programming Supplies
- Compact 12V Op Amp Supplies
- Battery-Powered Systems

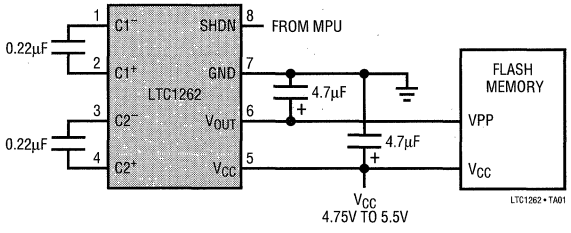
DESCRIPTION

The LTC®1262 is a regulated 12V, 30mA output DC/DC converter. It is designed to provide the 12V ±5% output necessary to program byte-wide flash memories. The output will provide up to 30mA from input voltages as low as 4.75V without using any inductors. Only four external capacitors are required to complete an extremely small surface mountable circuit.

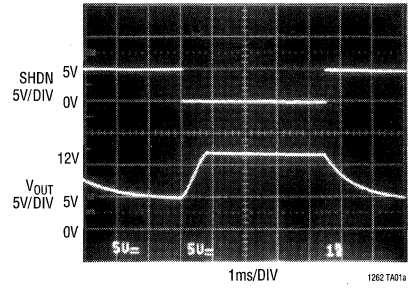
The TTL compatible shutdown pin can be directly connected to a microprocessor and reduces the supply current to less than 0.5µA. The LTC1262 offers improved shutdown current performance and requires fewer external components than competing solutions.

The LTC1262 is available in an 8-pin PDIP or SO-8 package.

TYPICAL APPLICATION



In/Out of Shutdown

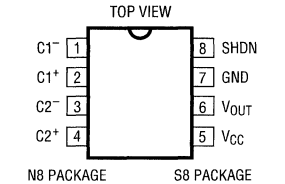


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6V
Input Voltage (SHDN) ..... −0.3V to V_{CC} + 0.3V
Output Current (I_{OUT}) 50mA
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LTC1262CN8 LTC1262CS8
S8 PART MARKING
1262

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.75V to 5.5V, T_A = 0°C to 70°C, (Notes 2, 3), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage	0mA ≤ I_{OUT} ≤ 30mA, V_{SHDN} = 0V	●	11.4		12.6	V
I_{CC}	Supply Current	No Load, V_{SHDN} = 0V	●		0.5	1	mA
I_{SHDN}	Shutdown Supply Current	No Load, V_{SHDN} = V_{CC}	●		0.5	10	µA
f_{OSC}	Oscillator Frequency	V_{CC} = 5V, I_{OUT} = 30mA			300		kHz
	Power Efficiency	V_{CC} = 5V, I_{OUT} = 30mA			74		%
R_{SW}	V_{CC} to V_{OUT} Switch Impedance	V_{CC} = V_{SHDN} = 5V, I_{OUT} = 0mA	●		0.18	2	kΩ
V_{IH}	SHDN Input High Voltage		●	2.4			V
V_{IL}	SHDN Input Low Voltage		●			0.8	V
	SHDN Input Current	V_{CC} = 5V, V_{SHDN} = 0V V_{CC} = 5V, V_{SHDN} = 5V	● ●	−20	−10 0.06	−5 10	µA µA
t_{ON}	Turn-On Time	C1 = C2 = 0.22µF, C_{IN} = C_{OUT} = 4.7µF, (Figures 1, 2)			500		µs
t_{OFF}	Turn-Off Time	C1 = C2 = 0.22µF, C_{IN} = C_{OUT} = 4.7µF, (Figures 1, 2)			3.3		ms

The ● denotes specifications which apply over the full operating temperature range.

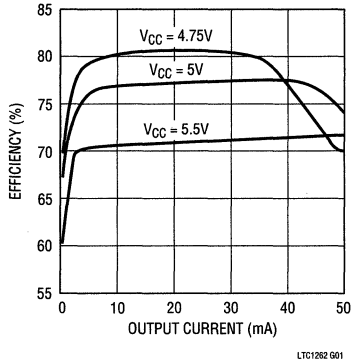
Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

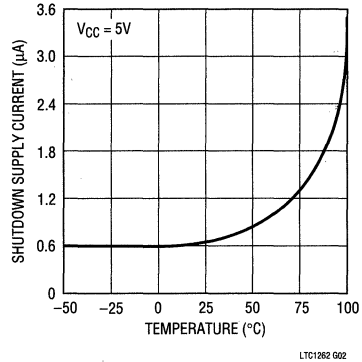
Note 3: All typicals are given at V_{CC} = 5V, T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

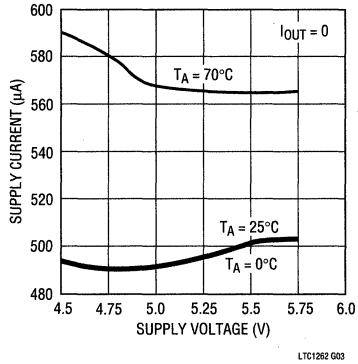
Efficiency vs Output Current



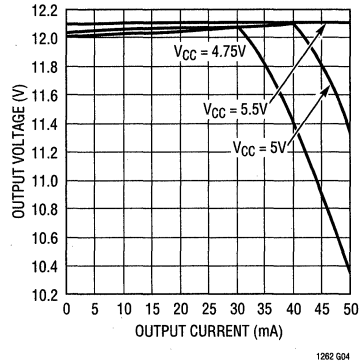
Shutdown Supply Current vs Temperature



Supply Current vs Supply Voltage



Output Voltage vs Output Current



PIN FUNCTIONS

$C1^-$ (Pin 1): C1 Negative Input. Connect a 0.22µF capacitor C1 between $C1^+$ and $C1^-$.

$C1^+$ (Pin 2): C1 Positive Input. Connect a 0.22µF capacitor C1 between $C1^+$ and $C1^-$.

$C2^-$ (Pin 3): C2 Negative Input. Connect a 0.22µF capacitor C2 between $C2^+$ and $C2^-$.

$C2^+$ (Pin 4): C2 Positive Input. Connect a 0.22µF capacitor C2 between $C2^+$ and $C2^-$.

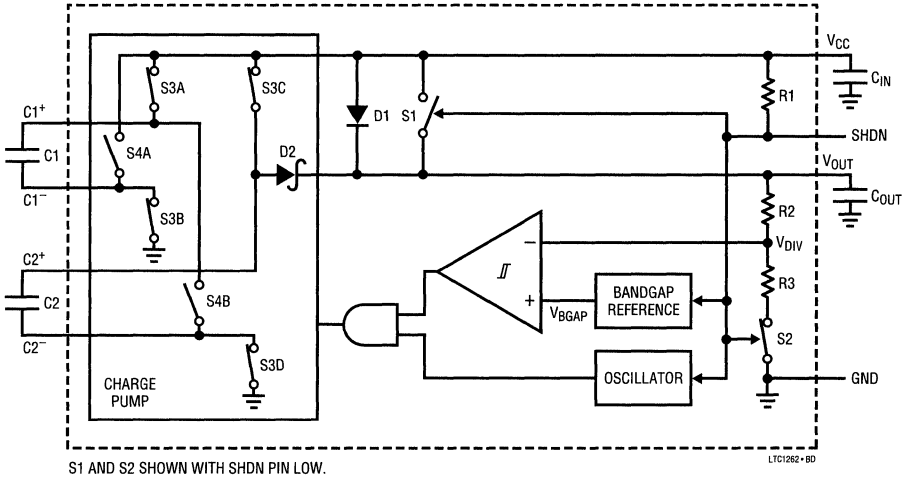
V_{CC} (Pin 5): Positive Supply Input Where $4.75V \leq V_{CC} \leq 5.5V$. Connect a 4.7µF bypass capacitor C_{IN} to ground.

V_{OUT} (Pin 6): 12V Output. Connect a 4.7µF bypass capacitor C_{OUT} to ground. When in the shutdown mode $V_{OUT} = V_{CC}$.

GND (Pin 7): Ground.

SHDN (Pin 8): Logic Level Shutdown Pin. Application of a logic low at SHDN pin will place the regulator in normal operation. With no external connection, or with SHDN tied to V_{CC}, the device will be put into shutdown mode. Connect to GND for normal operation. In shutdown mode the charge pump is turned off and $V_{OUT} = V_{CC}$.

BLOCK DIAGRAM



S1 AND S2 SHOWN WITH SHDN PIN LOW.
S3A, S3B, S3C, S3D, S4A AND S4B SHOWN WITH OSCILLATOR OUTPUT LOW AND $V_{DIV} < V_{BGAP} - V_{HYST}$.
COMPARATOR HYSTERISIS IS $\pm V_{HYST}$.

4

TIMING DIAGRAMS

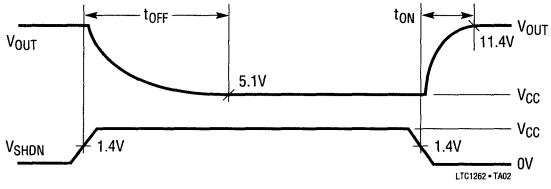


Figure 1. LTC1262 Timing Diagram

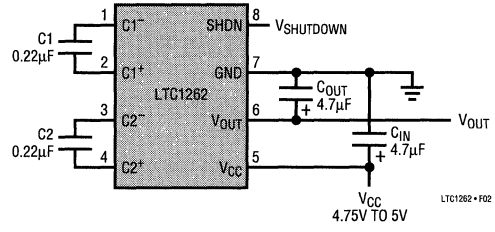


Figure 2. LTC1262 Timing Circuit

APPLICATIONS INFORMATION

Operation

The LTC1262 uses a charge pump tripler to generate 12V from a V_{CC} of 5V. The charge pump operates when clocked by a 300kHz oscillator. When the oscillator output is low, C1 and C2 are connected between V_{CC} and GND, charging them to V_{CC}. When the oscillator output goes high, C1 and C2 are stacked in series with the bottom plate of C1 pulled to V_{CC}. The top plate of C2 is switched to charge C_{OUT} and V_{OUT} rises. V_{OUT} is regulated to within 5% of 12V by an oscillator pulse gating scheme. A resistor divider senses V_{OUT}. When the output of the divider (V_{DIV}) is less than the output of a bandgap (V_{BGAP}) by the hysteresis voltage (V_{HYST}) of the comparator, oscillator pulses are applied to the charge pump to raise V_{OUT}. When V_{DIV} is above V_{BGAP} by V_{HYST}, the oscillator pulses are prevented from clocking the charge pump. V_{OUT} drops until V_{DIV} is below V_{BGAP} by V_{HYST} again. The gates of all internal switches are driven between V_{OUT} and GND. An internal diode ensures that the LTC1262 will start up under load by charging C_{OUT} to one diode drop below V_{CC}.

To reduce supply current the LTC1262 may be put into shutdown mode by floating the SHDN pin or taking it to V_{CC}. In this mode the bandgap, comparator, oscillator and resistor divider are switched off to reduce supply current to typically 0.5µA. At the same time an internal switch shorts V_{OUT} to V_{CC}; V_{OUT} takes 3.3ms to reach 5.1V (see t_{OFF} in Figure 1). When the SHDN pin is low, the LTC1262 exits shutdown and the charge pump operates to raise V_{OUT} to 12V. V_{OUT} takes 500µs to reach the lower regulation limit of 11.4V (see t_{ON} in Figure 1).

Choice of Capacitors

The LTC1262 is tested with the capacitors shown in Figure 2. C1 and C2 are 0.22µF ceramic capacitors and C_{IN} and C_{OUT} are 4.7µF tantalum capacitors. Refer to Table 1 if other choices are desired.

Table 1. Recommended Capacitor Types and Values

CAPACITOR	CERAMIC	TANTALUM	ALUMINUM
C1, C2	0.22µF to 1µF	Not Recommended	Not Recommended
C_{OUT}	2µF (Min)	4.7µF (Min)	10µF (Min)
C_{IN}	1µF (Min)	4.7µF (Min)	10µF (Min)

C1 and C2 should be ceramic capacitors with values in the range of 0.22µF to 1µF. Higher values provide better load regulation. Tantalum capacitors are not recommended as the higher ESR of these capacitors degrades performance when the load current is above 25mA with V_{CC} = 4.75V.

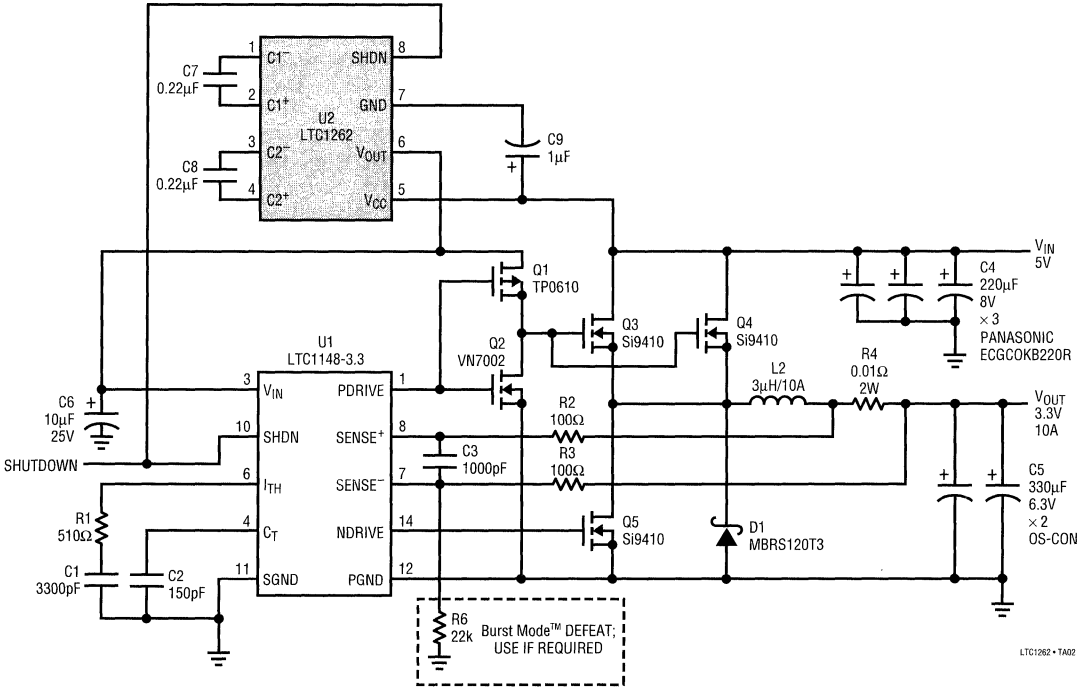
C_{IN} and C_{OUT} can be ceramic, tantalum or electrolytic capacitors. The ESR of C_{OUT} introduces steps in the V_{OUT} waveform whenever the charge pump charges C_{OUT}. This tends to increase V_{OUT} ripple. Ceramic or tantalum capacitors are recommended for C_{OUT} if minimum ripple is desired. The LTC1262 does not require a 0.1µF capacitor between V_{CC} and V_{OUT} for stability.

Maximum Load Current

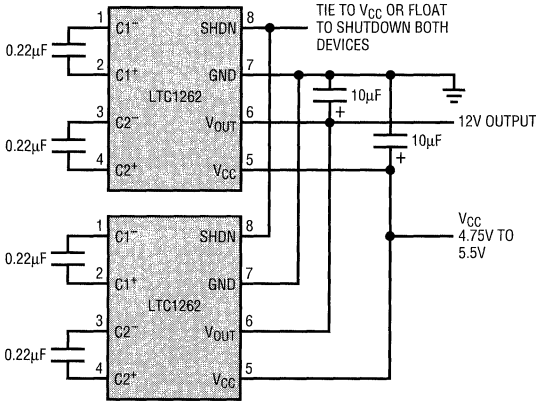
The LTC1262 will source up to 50mA continuously without any damage to itself. **Do not short the V_{OUT} pin to ground.** If the V_{OUT} pin is shorted to ground, irreversible damage to the device will result.

TYPICAL APPLICATIONS

5V to 3.3V/10A Converter



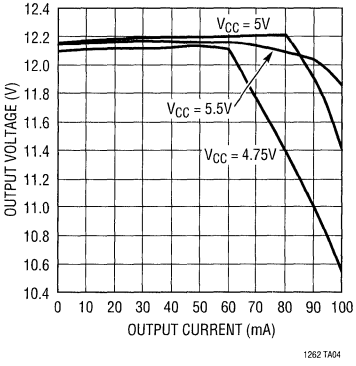
Paralleling Devices



NOTE: KEEP DEVICES CLOSE TOGETHER OR USE SEPARATE 4.7µF TANTALUM CAPACITORS IF THIS IS NOT POSSBILE.

LTC1262 • TA03

Output Voltage vs Output Current for Two Paralleled Devices



SEE FIGURE AT LEFT.

Burst Mode is a trademark of Linear Technology Corporation.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1106*	Micropower Step-Up DC/DC Converter for PCMCIA Card Flash Memory	PCMCIA Card Power Control, 9μA I_{SHDN}, Small SMT Components, Requires External Inductor
LT1109-12	Micropower Low Cost DC/DC Converter Adjustable and Fixed 12V	Three-Lead Z Package, Requires External Inductor
LT1109A-12	Micropower DC/DC Converter Flash Memory VPP Generator Adjustable and Fixed 12V	Requires External Inductor
LT1301	Micropower High Efficiency 5V/12V Step-Up DC/DC Converter for Flash Memory	7μA I_{SHDN}, SMT Inductor and Capacitors
LT1309	500kHz Micropower DC/DC Converter for Flash Memory	Small SMT Inductor and Capacitors, 6μA I_{SHDN}

* See also LT1312/LT1313 PCMCIA VPP drivers/regulators, LT1314/LT1315 PCMCIA switch matrix and the LTC1470/LTC1471/LTC1472 Protected V_{CC} and VPP switching matrices

Clock-Synchronized Switched Capacitor Regulated Voltage Inverter

FEATURES

- **Regulated Negative Voltage from a Single Positive Supply**
- **External Clock for Synchronization in Noise Sensitive Systems**
- **REG Output Indicates Output is in Regulation**
- **Low Output Ripple: 5mV Typ**
- Can Provide Regulated –5V from a 3V Supply
- Supply Current: 600µA Typ
- Shutdown Mode Drops Supply Current to 0.2µA
- Up to 12mA Output Current
- Adjustable or Fixed Output Voltages
- Requires Only Three or Four External Caps
- Output Regulation: 5%
- Available in SO-8 Packages

APPLICATIONS

- GaAs FET Bias Generators
- Negative Supply Generators
- Battery Powered Systems
- Single Supply Applications

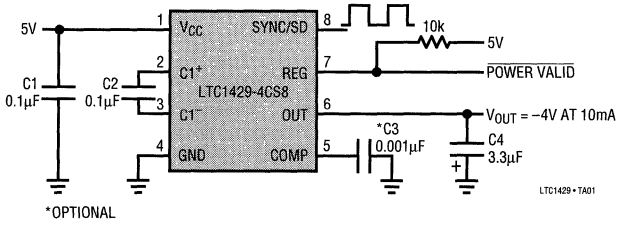
DESCRIPTION

The LTC®1429 is a switched-capacitor voltage inverter designed to provide a regulated negative voltage from a single positive supply and permits clock synchronization in noise sensitive systems. The LTC1429CS operates from a single 3V to 8V supply and provides an adjustable output voltage from –1.25V to –8V. An on-chip resistor string allows the LTC1429CS to be configured for output voltages of –3.5V, –4V, –4.5V or –5V. The LTC1429CS8 is optimized for applications which require a fixed –4V output from a 5V supply and requires only a single external 0.1µF flying capacitor. The LTC1429CS requires one or two external 0.1µF capacitors, depending on input voltage. Both versions require additional external input and output bypass capacitors. An optional compensation capacitor at ADJ/COMP can be used to reduce the output voltage ripple.

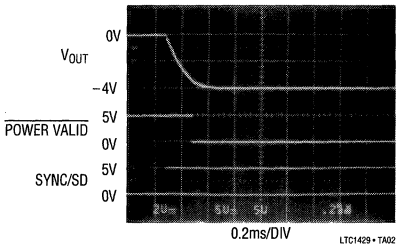
Each version of the LTC1429 guarantees output regulation of 5%. The LTC1429 includes an open-drain REG output which pulls low when the output is within 5% of the set value. Output ripple is typically as low as 5mV. The LTC1429 requires an external clock applied to the SYNC/SD for normal operation and consumes a typical quiescent current of 600µA. Holding the SYNC/SD either high or low brings the device into shutdown and the supply current drops to 0.2µA. For applications which don't have a clock signal available, the LTC1261 provides the same functionality with an internal oscillator. For applications which require output ripple below 1mV, see the LTC1550/LTC1551. The LTC1429CS is available in a 14-pin SO package and the LTC1429CS8 is available in an 8-pin SO package.

TYPICAL APPLICATION

–4V Generator with $\overline{\text{Power Valid}}$



Waveforms for –4V Generator with $\overline{\text{Power Valid}}$

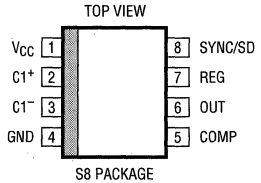


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (Note 2) 9V
Output Voltage ..... 0.3V to –9V
Total Voltage, V_{CC} to V_{OUT} (Note 2) 12V
Input Voltage (SYNC/SD Pin) ..... –0.3V to (V_{CC} + 0.3V)
Input Voltage (REG Pin) ..... –0.3V to 12V
Input Voltage (ADJ, RO-1, R_{ADJ}) ..... (V_{OUT} – 0.3V) to (V_{CC} + 0.3V)
Output Short Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

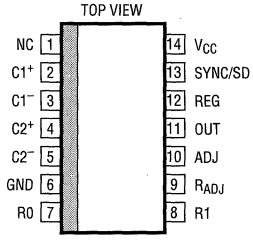
PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1429CS8-4*
S8 PART MARKING
14294



S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1429CS

Consult factory for Industrial and Military grade parts. *Contact factory for other output voltages or 8-pin adjustable parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 3V to 6.5V. C1 = C2 = 0.1µF (Note 4), C_{OUT} = 3.3µF, F_{SYNC} = 700kHz with 50% duty cycle square wave, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1429CS8/LTC1429CS MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage		●	1.20	1.24	1.28	V
I_S	Supply Current	V_{CC} = 3.3V	●		600	1500	µA
		V_{CC} = 5V	●		600	1500	µA
		$V_{SYNC/SD}$ = V_{CC} or GND	●		0.2	5	µA
F_{SYNC}	Synchronous Clock Frequency (Note 8)	V_{CC} ≤ 5V		60	700	2000	kHz
		V_{CC} = 6.5V		100	700	2000	kHz
P_{EFF}	Power Efficiency				65		%
V_{OL}	REG Output Low Voltage	I_{REG} = 1mA	●		0.1	0.8	V
I_{REG}	REG Sink Current	V_{REG} = 0.8V, V_{CC} = 3.3V	●	5	8		mA
		V_{REG} = 0.8V, V_{CC} = 5V	●	8	15		mA
I_{ADJ}	Adjust Pin Current	V_{ADJ} = 1.24V (Note 5)	●		0.01	1	µA
V_{IH}	SYNC/SD Input High Voltage	V_{CC} = 5V	●	2.0			V
V_{IL}	SYNC/SD Input Low Voltage	V_{CC} = 5V	●			0.8	V
I_{IN}	SYNC/SD Input Current	$V_{SYNC/SD}$ = V_{CC} or GND	●			±1	µA
T_{ON}	Turn On Time	I_{OUT} = 10mA			200		µs

ELECTRICAL CHARACTERISTICS

Tripler Mode, V_{CC} = 3.3V, C1 = C2 = 0.1µF (Note 4), C_{OUT} = 3.3µF, F_{SYNC} = 700kHz with 50% duty cycle square wave, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1429CS MIN	LTC1429CS TYP	LTC1429CS MAX	UNITS
ΔV_{OUT}	Output Regulation	$-1.24V \geq V_{OUT} \geq -4V$, $0 \leq I_{OUT} \leq 12mA$	●		1	5	%
		$-4V \geq V_{OUT} \geq -5V$, $0 \leq I_{OUT} \leq 8mA$	●		2	5	%
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V	●		35	75	mA
V_{RIP}	Output Ripple Voltage	I_{OUT} = 5mA, V_{OUT} = −4V			5		mV

Doubler Mode, V_{CC} = 5V, C1 = 0.1µF, C2 = 0 (Note 4), C_{OUT} = 3.3µF, F_{SYNC} =700kHz with 50% duty cycle, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1429CS8/LTC1429CS MIN	LTC1429CS8/LTC1429CS TYP	LTC1429CS8/LTC1429CS MAX	UNITS
ΔV_{OUT}	Output Regulation	$-1.24V \geq V_{OUT} \geq -4V$, $0 \leq I_{OUT} \leq 10mA$	●		1	5	%
		$-4V \geq V_{OUT} \geq -4.5V$, $0 \leq I_{OUT} \leq 10mA$ (Note 6)	●		2	5	%
V_{OUT}	Output Voltage	V_{OUT} Set to −4V, $0 \leq I_{OUT} \leq 10mA$	●	−3.80	−4.00	−4.20	V
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V	●		80	125	mA
V_{RIP}	Output Ripple Voltage	I_{OUT} = 5mA, V_{OUT} = −4V			10		mV

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Setting output to < −7V will exceed the total voltage maximum rating with a 5V supply. With supplies higher than 4V the output should never be set to exceed (V_{CC} − 12V).

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground, unless otherwise specified. All typicals are given at T_A = 25°C.

Note 4: C1 = C2 = 0.1µF means the specifications apply to tripler mode where $V_{CC} - V_{OUT} = 3.3V_{CC}$ (LTC1429CS only; the LTC1429CS8 cannot be connected in tripler mode), with C1 connected between $C1^+$ and $C1^-$ and C2 connected between $C2^+$ and $C2^-$. C2 = 0 implies doubler mode where $V_{CC} - V_{OUT} = 2V_{CC}$; for the LTC1429CS, this means C1 connects from $C1^+$ to $C2^-$ with $C1^-$ and $C2^+$ floating. For the LTC1429CS8 in doubler mode, C1 connects from $C1^+$ to $C1^-$; there are no C2 pins.

Note 5: Adjustable output parts only; does not apply to fixed output parts.

Note 6: For output voltages below −4.5V, the LTC1429 may reach 50% duty cycle and fall out of regulation with heavy load or low input voltages. Beyond this point, the output will follow the input with no regulation.

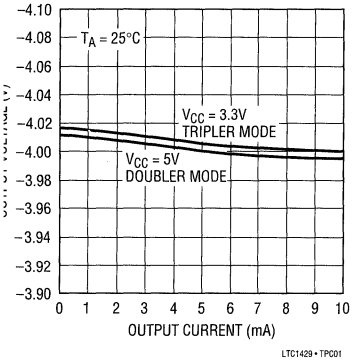
Note 7: LTC1429 will operate with square wave of 40% to 60% duty cycle. For best performance, use a square wave with 50% duty cycle.

Note 8: Maximum frequency is not tested. Typical part can be used beyond 2MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

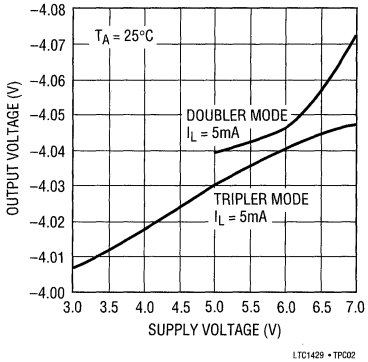
(See Test Circuits; Figure 1 for Doubler Mode, Figure 2 for Tripler Mode)

Output Voltage vs Output Current



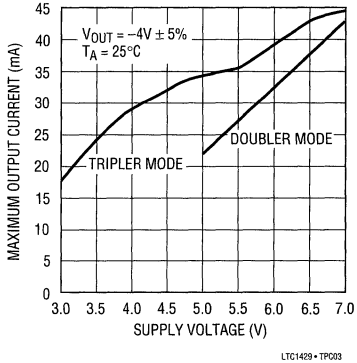
LTC1429 • TPC01

Output Voltage vs Supply Voltage



LTC1429 • TPC02

Maximum Output Current vs Supply Voltage

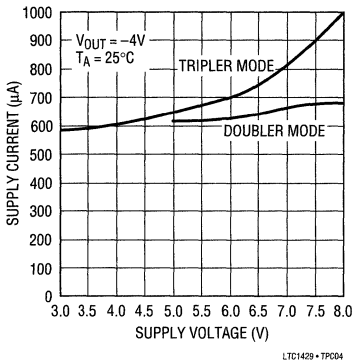


LTC1429 • TPC03

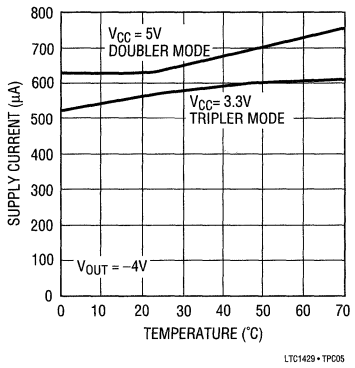
TYPICAL PERFORMANCE CHARACTERISTICS

(See Test Circuits: Figure 1 for Doubler Mode, Figure 2 for Tripler Mode)

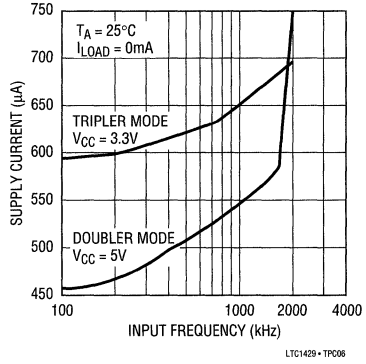
Supply Current vs Supply Voltage



Supply Current vs Temperature



Supply Current vs Input Frequency



PIN FUNCTIONS

Pin numbers are shown as (LTC1429CS/LTC1429CS8).

NC (Pin 1/NA): No Internal Connection.

C1⁺ (Pin 2/Pin 2): C1 Positive Input. Connect an 0.1µF capacitor between C1⁺ and C1⁻. With the LTC1429CS in doubler mode, connect a 0.1µF capacitor from C1⁺ to C2⁻.

C1⁻ (Pin 3/Pin 3): C1 Negative Input. Connect a 0.1µF capacitor from C1⁺ to C1⁻. With the LTC1429CS in doubler mode only, C1⁻ should float.

C2⁺ (Pin 4/NA): C2 Positive Input. In tripler mode, connect a 0.1µF capacitor from C2⁺ to C2⁻. This pin is used with the LTC1429CS in tripler mode only; in doubler mode, this pin should float.

C2⁻ (Pin 5/NA): C2 Negative Input. In tripler mode, connect a 0.1µF capacitor from C2⁺ to C2⁻. In doubler mode, connect a 0.1µF capacitor from C1⁺ to C2⁻.

GND (Pin 6/Pin 4): Ground. Connect to a low-impedance ground. A ground plane will help to minimize regulation errors.

R0 (Pin 7/NA): Internal Resistor String-1st Tap. See Table 3 in the Applications Information section for information on internal resistor string pin connections vs output voltage.

R1 (Pin 8/NA): Internal Resistor String-2nd Tap.

R_{ADJ} (Pin 9/NA): Internal Resistor String Output. Connect this pin to ADJ to use the internal resistor divider. See Table 3 in the Applications Information section for information on internal resistor string pin connections vs output voltage.

ADJ (COMP for fixed output versions) (Pin 10/Pin 5): Output Adjust/Compensation. For adjustable parts, this pin is used to set the output voltage. The output voltage should be divided down with a resistor divider and fed back to this pin to set the regulated output voltage. The resistor divider can be external or the internal divider string can be used if it can provide the required output voltage. Typically the resistor string should draw ≥ 10µA from the output to minimize errors due to the bias current at the adjust pin. Fixed output parts have the internal resistor string connected to this pin inside the package; the pin can be used to trim the output voltage if desired. It can also be used as an optional feedback compensation pin to reduce output ripple on both adjustable and fixed output voltage parts. See the Applications Information section for more on compensation and output ripple.

OUT (Pin 11/Pin 6): Negative Voltage Output. This pin must be bypassed to ground with a 1.0µF or larger capacitor; it must be at least 3.3µF to provide specified output ripple. The size of the output capacitor has a strong

PIN FUNCTIONS

effect on output ripple; see the Applications Information section for more details.

REG (Pin 12/Pin 7): This is an open drain output that pulls low when the output voltage is within 5% of the set value. It will sink 10mA to ground with a 5V supply. The external circuitry must provide a pull-up or REG will not swing high. The voltage at REG may exceed V_{CC}; it can be pulled up to 12V above ground without damage.

SYNC/SD (Pin 13/Pin 8): Synchronous Clock Input. A minimum input clock frequency (60kHz with $V_{CC} \leq 5V$ and 100kHz with V_{CC} = 6.5V) must be applied to this input to keep the LTC1429 operating normally. An input clock below the minimum frequency may cause the charge pump to operate erratically or the device to shut down. A logic high or low at the SYNC/SD pin will put the device into SHUTDOWN and drop the supply current to 0.2µA. The LTC1429 will operate with input square wave of 40% to 60% duty cycle. For best performance, use a square wave of 50% duty cycle.

V_{CC} (Pin 14/Pin 1): Power Supply. This requires an input voltage between 3V and 6.5V. Certain combinations of output voltage and operating mode may place additional restrictions on the input voltage; see the Applications Information section for details. V_{CC} must be bypassed to ground with at least a 0.1µF capacitor, placed in close proximity to the chip; again, see the Applications Information section.

TEST CIRCUITS

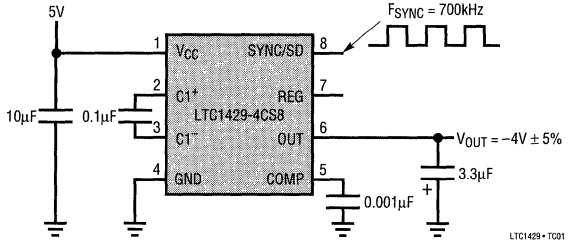


Figure 1. Doubler Mode

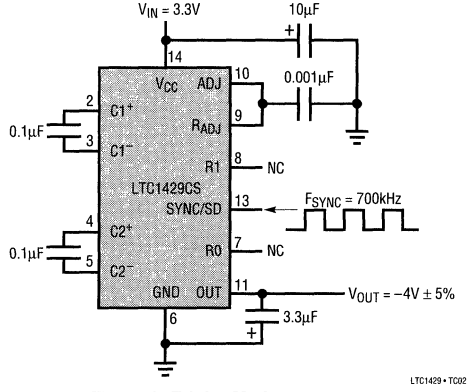


Figure 2. Tripler Mode

APPLICATIONS INFORMATION

MODES OF OPERATION

The LTC1429 uses a charge pump to generate a negative output voltage that can be regulated to a value either higher or lower than the original input voltage. It has two modes of operation: a doubler inverting mode, which can provide a negative output equal to or less than the positive power supply, and a tripler inverting mode, which can provide negative output voltages either larger or smaller in magnitude than the original positive supply. The tripler offers greater versatility and wider input range but requires four external capacitors and a 14-pin package; the doubler offers the SO-8 package and requires only three external capacitors. The optional compensation capacitor at ADJ/COMP is used to reduce the ripple output voltage.

Doubler Mode

This mode allows the LTC1429 to generate negative output voltage magnitudes up to that of the supply voltage,

APPLICATIONS INFORMATION

creating a voltage between V_{CC} and OUT of up to $2 \times V_{CC}$. In doubler mode, the LTC1429 uses a single flying capacitor to invert the input supply voltage and the output voltage is stored on the output bypass capacitor between switch cycles. The LTC1429CS8 is always configured in doubler mode and has only one pair of flying capacitor pins (Figure 3a). The LTC1429CS can be configured in doubler mode by connecting a single flying capacitor between the $C1^+$ and $C2^-$ pins; $C1^-$ and $C2^+$ should be left floating (Figure 3b).

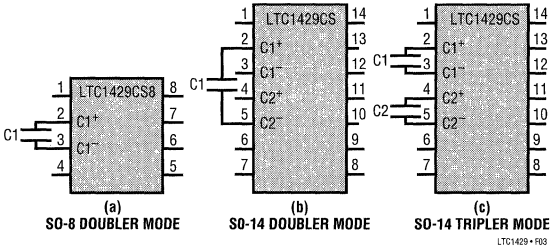


Figure 3. Flying Capacitor Connections

Tripler Mode

The LTC1429CS can be used in a tripler mode which can generate negative output voltages up to twice the supply voltage; the total voltage between the V_{CC} and OUT pins is $3 \times V_{CC}$. Tripler mode can be used to generate –5V from a single positive 3.3V supply, for example. Tripler mode requires two external flying capacitors. The first connects between $C1^+$ and $C1^-$ and the second between $C2^+$ and $C2^-$ (Figure 3c). Because of the relatively high voltages that can be generated in this mode, care must be taken to ensure that the total input-to-output voltage never exceeds 12V, or the LTC1429 may be damaged. This is possible with supply voltages above 4V in tripler mode and above 6V in doubler mode, although in most applications the output voltage will be kept in check by the regulation loop. As the input supply voltage rises, the allowable output voltage drops, finally reaching –4V with a 8.5V supply. To avoid this problem, use doubler mode whenever possible with high input supply voltages.

THEORY OF OPERATION

A block diagram of the LTC1429 is shown in Figure 4. The heart of the LTC1429 is the charge pump core, shown in the dashed line. It generates a negative output voltage by first charging the flying caps between V_{CC} and ground. It then

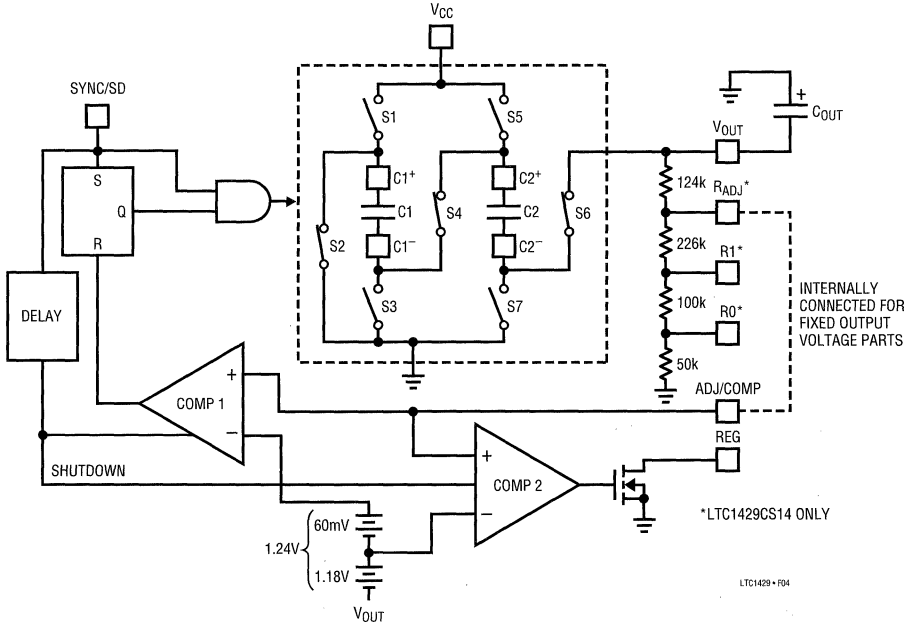


Figure 4. Block Diagram

APPLICATIONS INFORMATION

stacks the flying caps on top of each other and connects the top of the stack to ground; this forces the bottom of the stack to a negative voltage. The charge on the flying capacitors is transferred to the output bypass cap, leaving it charged to the negative output voltage. This process is driven by the external 700kHz clock via the SYNC/SD pin.

Figure 4 shows the charge pump configured in tripler mode. With the external input clock low, C1 and C2 are charged to V_{CC} by S1, S3, S5 and S7. At the next rising clock edge, S1, S3, S5 and S7 open and S2, S4 and S6 close, stacking C1 and C2 on top of each other. S2 connects $C1^+$ to ground, S4 connects $C1^-$ to $C2^+$ and $C2^-$ is connected to the output by S6. The charge in C1 and C2 is transferred to C_{OUT}, setting it to a negative voltage. Doubler mode works the same way except that the single flying capacitor (C1) is connected between $C1^+$ and $C2^-$. S3, S4 and S5 don't do anything useful in doubler mode. C1 is charged initially by S1 and S7, and connected to the output by S2 and S6.

The output voltage is monitored by COMP1, which compares a divided replica of the output at ADJ (COMP for fixed output parts) to the internal reference. At the beginning of a cycle, the clock is low, forcing the output of the AND gate low and charging the flying caps. The next rising clock edge sets the RS latch, setting the charge pump to transfer charge from the flying caps to the output capacitor. As long as the output is below the set point, COMP1 stays low, the latch stays set and the charge pump runs at the duty cycle of the input clock signal, gated through the AND gate. As the output approaches the set voltage, COMP1 will trip whenever the divided signal exceeds the internal 1.24V reference, relative to OUT. This resets the RS latch and truncates the clock pulses, internally reducing the amount of charge transferred to the output capacitor and regulating the output voltage. If the output exceeds the set point, COMP1 stays high, inhibiting the RS latch and disabling the charge pump.

COMP2 also monitors the divided signal at ADJ, but it is connected to a 1.18V reference, 5% below the main reference voltage. When the divided output exceeds this lower reference voltage, indicating that the output is within 5% of the set value, COMP2 goes high, turning on the REG output transistor. This is an open drain N-channel device capable of sinking 8mA with a 3.3V V_{CC} and 15mA with a 5V V_{CC}. When in "off" state (divided output more than 5% below V_{REF}) the drain can be pulled above V_{CC} without damage, up to a maximum of 12V above ground. Note that the REG output only indicates if the magnitude of the output is *below* the magnitude of the set point by 5% (i.e., $V_{OUT} > -4.75V$ for a $-5V$ set point). If the magnitude of the output is forced *higher* than the magnitude of the set point (i.e., to $-6V$ when the output is set for $-5V$) the REG output will stay low.

OUTPUT RIPPLE

Output ripple in the LTC1429 comes from two sources: voltage droop at the output capacitor between clocks and frequency response of the regulation loop. Voltage droop is easy to calculate. With a typical external input clock frequency of 700kHz, the charge on the output capacitor is refreshed once every 1.43µs. With a 15mA load and a 3.3µF output capacitor, the output will droop by:

$$I_{LOAD} \times \left(\frac{\Delta t}{C_{OUT}}\right) = 15mA \times \left(\frac{1.43\mu s}{3.3\mu F}\right) = 6.5mV$$

There can be a significant ripple component when the output is heavily loaded, especially if the output capacitor is small or the external input clock frequency is low. If absolute minimum output ripple is required, a 10µF or greater output capacitor, high input clock rate (F_{SYNC}) and lower value (<0.1µF) of flying capacitor should be used.

Regulation loop frequency response is the other major contributor to output ripple. The LTC1429 regulates the output voltage by limiting the amount of charge transferred to the output capacitor on a cycle-by-cycle basis. The output voltage is sensed at the ADJ pin (COMP for fixed output versions) through an internal or external resistor divider from the OUT pin to ground. As the flying caps are first connected to the output, the output voltage begins to change quite rapidly. As soon as it exceeds the set point, COMP1 trips, switching the state of the charge pump and stopping the charge transfer. Because the RC time constant of the capacitors and the switches is quite short, the ADJ pin must have a wide AC bandwidth to be able to respond to the output in time. External parasitic capacitance at the ADJ pin can reduce the bandwidth to the point where the comparator cannot respond by the time

APPLICATIONS INFORMATION

the clock pulse finishes. When this happens, the comparator will allow a few complete pulses through, then overcorrect and disable the charge pump until the output drops below the set point. Under these conditions, the output will remain in regulation, but the output ripple will increase as the comparator "hunts" for the correct value.

To help prevent this from happening, an external capacitor can be connected from ADJ (or COMP for fixed output parts) to ground to compensate for external parasitics and increase the regulation loop bandwidth (Figure 5). This sounds counter-intuitive until we remember that the internal reference is generated with respect to OUT, not ground. The feedback loop actually sees ground as its "output"; thus the compensation capacitor should be connected across the "top" of the resistor divider from ADJ (or COMP) to ground. By the same token, avoid adding capacitance between ADJ (or COMP) and V_{OUT}; this will slow down the feedback loop and increase output ripple. A 1000pF capacitor from ADJ or COMP to ground will compensate the loop properly under most conditions.

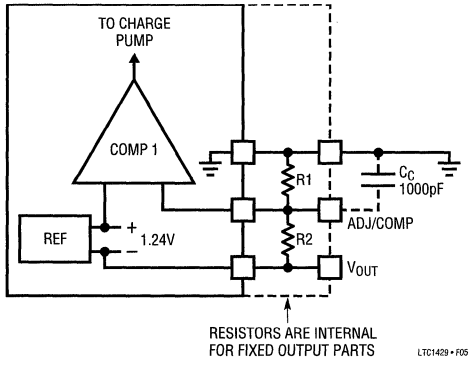


Figure 5. Regulator Loop Compensation

EXTERNAL CLOCK

The LTC1429 requires an external clock to operate. This clock signal should be TTL or CMOS compatible and should be applied to the SYNC/SD pin. The external clock allows the user to control the frequency at which the LTC1429 operates, preventing it from interfering with other frequency-sensitive circuitry. The LTC1429 can be synchronized to any frequency between 60kHz (100kHz for $V_{CC} > 5$) and 2MHz. Higher clock frequencies can help reduce output ripple at the cost of additional quiescent current. The clock signal should have a duty cycle between 40% and 60% for proper regulation loop performance.

The LTC 1429 can be shut down by stopping the clock. An internal circuit monitors the time between clock edges at the SYNC/SD pin. If a 10μs period elapses without a rising or falling edge, LTC1429 assumes the clock has stopped and goes into shutdown mode and the quiescent current drops to below 1μA. The next clock edge at the SYNC/SD pin will reawaken the LTC1429. At clock frequencies below 50kHz (50% duty cycle) the LTC1429 may enter shutdown mode briefly during each clock cycle causing erratic operation. Minimum operating frequency should be kept above 60kHz (above 100kHz with $V_{CC} > 5$) to prevent this from happening.

Radiation from the clock signal at the SYNC/SD pin can interfere with the feedback node at the ADJ/COMP pin causing errors in the output voltage. The clock line should be routed away from the circuitry at the ADJ/COMP pin and should be shielded with a ground plane or with coaxial cable. A compensation capacitor from the ADJ/COMP pin to ground can also help to reduce this effect: 0.001μF is adequate for most applications.

OUTPUT FILTERING

If extremely low output ripple (< 10mV) is required, additional output filtering is required. Because the LTC1429 uses a high, external control switching frequency, fairly low value RC or LC networks can be used at the output to effectively filter the output ripple. With F_{SYNC} = 700kHz, a 10Ω series output resistor and a 3.3μF capacitor will cut output ripple to below 3mV (see Figure 6). Further reduc-

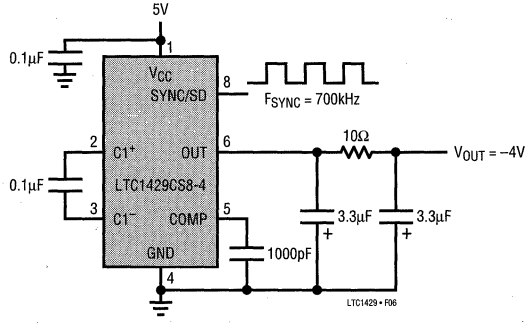


Figure 6. Output Filter Cuts Ripple Below 3mV

APPLICATIONS INFORMATION

tions can be obtained with larger filter capacitors or by using an LC output filter or higher F_{SYNC} clock rate with a lower value (<0.1µF) of flying capacitor. Also see the section on Output Capacitor ESR. For applications requiring ripple below 1mV, see the LTC1550/LTC1551 data sheet.

CAPACITOR SELECTION

Capacitor Sizing

The performance is dependent on the type of capacitors used. The LTC1429 requires bypass caps to ground for both the V_{CC} and OUT pins. The input cap provides most of the LTC1429's supply current while it is charging the flying caps. It should be mounted as close to the package as possible, its value should be equal to or larger than the flying cap in doubling mode and at least twice the value of the flying caps in tripling mode. Ceramic capacitors generally provide adequate performance; avoid using a tantalum capacitor as the input bypass unless there is at least a 0.1µF ceramic cap in parallel with it. The charge pump caps are somewhat less critical, since their peak currents are limited by the switches inside the LTC1429. Most applications should use 0.1µF as the flying cap value; conveniently, ceramic caps are the most common type of 0.1µF cap and they work well here. Usually the easiest solution is to use the same type of capacitor for both the input bypass and flying caps.

The output cap performs two functions; it provides output current to the load during half of the charge pump cycle and its value helps to set the output ripple voltage. For applications that are insensitive to output ripple, the output bypass cap can be as small as 1µF. To achieve specified low output ripple, a 3.3µF or greater output capacitor, high input clock rate (F_{SYNC}) and lower value (<0.1µF) of flying capacitor should be used. Larger output caps will reduce output ripple further, at the expense of turn on time.

In an application where the maximum load current is well-defined and output ripple is critical or input peak currents need to be minimized, the flying capacitor values can be tailored to the application. Reducing the value of the flying capacitors reduces the amount of charge transferred with each clock cycle. The smaller capacitors draw smaller pulses of current out of V_{CC} as well, limiting peak currents and reducing the demands on the input supply. Tables 1 and 2 show recommended values of flying capacitors vs maximum load capacity at F_{SYNC} = 400kHz and 700kHz respectively.

Table 1. Typical Max Load (mA) vs Flying Capacitor Value at T_A = 25°C, V_{OUT} = –4V, F_{SYNC} = 400kHz

FLYING CAPACITOR VALUE (µF)	MAX LOAD (mA) V_{CC} = 5V DOUBLER MODE	MAX LOAD (mA) V_{CC} = 3.3V TRIPLER MODE
0.1	22	20
0.047	16	15
0.033	8	11
0.022	4	5
0.01	1	3

Table 2. Typical Max Load (mA) vs Flying Capacitor Value at T_A = 25°C, V_{OUT} = –4V, F_{SYNC} = 700kHz

FLYING CAPACITOR VALUE (µF)	MAX LOAD (mA) V_{CC} = 5V DOUBLER MODE	MAX LOAD (mA) V_{CC} = 3.3V TRIPLER MODE
0.1	18	25
0.047	17	22
0.033	14	20
0.022	12	17
0.01	3	9

Output Capacitor ESR

Output capacitor the Equivalent Series Resistance (ESR) is another factor to consider. Excessive ESR in the output capacitor can fool the regulation loop into keeping the output artificially low by prematurely terminating the charging cycle. As the charge pump switches to recharge the output, a brief surge of current flows from the flying caps to the output cap. This current surge can be as high as 100mA under full load conditions. A typical 3.3µF tantalum capacitor has 1Ω or 2Ω of ESR; 100mA × 2Ω = 200mV. If the output is within 200mV of the set point, this additional 200mV surge will trip the feedback comparator and terminate the charging cycle. The pulse dissipates quickly and the comparator returns to the correct state, but the RS latch will not allow the charge pump to respond until the next clock edge. This prevents the charge pump from

APPLICATIONS INFORMATION

going into very high frequency oscillation under such conditions. It also creates an output error as the feedback loop regulates based on the top of the spike, not the average value of the output (Figure 7). The resulting output voltage behaves as if a resistor of value $C_{ESR} \times (I_{PK}/I_{AVE})\Omega$ was placed in series with the output. To minimize this effect, output capacitor ESR should be as low as possible or smaller value high frequency bypass (typically a 0.1µF ceramic) should be added in parallel with the output capacitor.

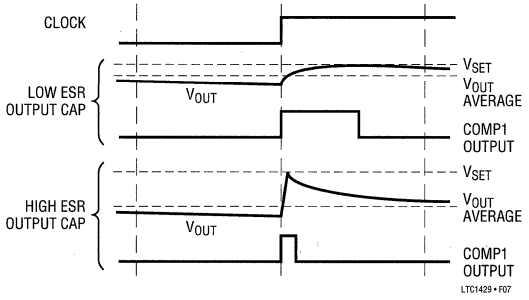


Figure 7. Output Ripple with Low and High ESR Caps

Note that ESR in the flying caps will not cause the same condition; in fact, it may actually improve the situation by cutting the peak currents and lowering the amplitude of the spike. More flying cap ESR is not necessarily better, however; as soon as the RC time constant approaches half of a clock period (the time the capacitors have to share charge at full duty cycle) the output current capability of the LTC1429 will begin to diminish. For 0.1µF flying capacitors and typical 700kHz external clock, this gives a maximum total series resistance of:

$$\frac{1}{2}\left(\frac{t_{CLK}}{C_{FLY}}\right) = \frac{1}{2}\left(\frac{1}{700kHz}\right) / 0.1\mu F = 7.14\Omega$$

Most of this resistance is already provided by the internal switches in the LTC1429 (especially in tripler mode). More than 1Ω or 2Ω of ESR on the flying caps will start to affect the regulation at maximum load.

RESISTOR SELECTION

Resistor selection is easy with the fixed output versions of the LTC1429; no resistors are needed! Selecting the right resistors for the adjustable parts is only a little more difficult. A resistor divider should be used to divide the signal at the output to give 1.24V at the ADJ pin *with respect to* V_{OUT} (Figure 8). The LTC1429 uses a positive reference with respect to V_{OUT}, not a negative reference with respect to ground (Figure 4 shows reference connection). Be sure to keep this in mind when connecting the resistors! If the initial output is not what you expected, try swapping the two resistors.

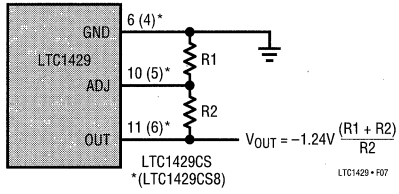


Figure 8. External Resistor Connections

The 14-pin adjustable parts include a built-in resistor string which can provide an assortment of output voltages by using different pin-strapping options at the RO, R1 and R_{ADJ} pins (Table 3). The internal resistors are roughly 124k, 226k, 100k and 50k (see Figure 4) giving output options of –3.5V, –4V, –4.5V and –5V. The resistors are carefully matched to provide accurate divider ratios, but the absolute values can vary substantially from part to part. It's not a good idea to create a divider using an external resistor and one of the internal resistors unless the output voltage accuracy is not critical.

Table 3. Output Voltages Using the Internal Resistor Divider

PIN CONNECTIONS	OUTPUT VOLTAGE
ADJ - R_{ADJ}	–5.0V
ADJ - R_{ADJ}, RO - GND	–4.5V
ADJ - R_{ADJ}, R1 - RO	–4.0V
ADJ - R_{ADJ}, R1-GND	–3.5V
ADJ - R1	–1.77V
ADJ - RO	–1.38V
ADJ - GND	–1.24V

There are some oddball output voltages available as well. They are obtained by connecting ADJ to RO or R1 and shorting out some of the internal resistors. If one of them gives you the output voltage you want, by all means use it!

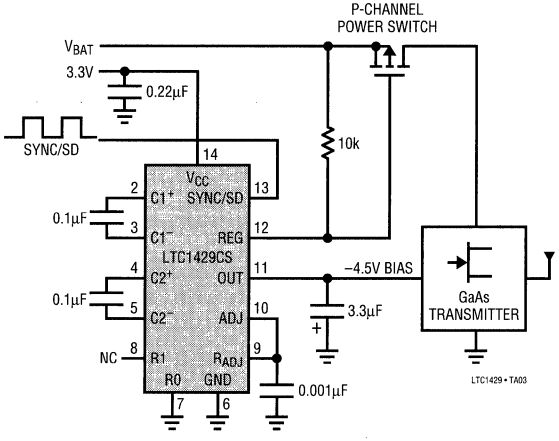
APPLICATIONS INFORMATION

The internal resistor values are the same for the fixed output versions of the LTC1429 as they are for the adjustable parts. The output voltage can be trimmed, if desired, by connecting external resistance from the COMP pin to OUT or ground to alter the divider ratio. As in the adjustable parts, the absolute value of the internal resistors may vary significantly from unit to unit. As a result, the further the trim shifts the output voltage, the less accurate the output voltage will be. If a precise output voltage other than one of the available fixed voltages is required, it's better to use an adjustable LTC1429 and use precision external resistors. The internal reference is trimmed at the factory to within 3.5% of 1.24V. With 1% external resistors, the output will be within 5.5% of the nominal value, even under worst case conditions.

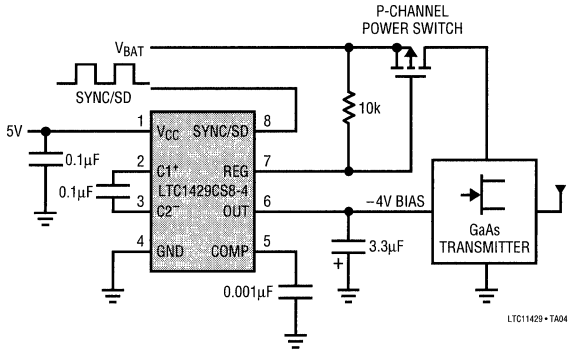
The LTC1429 can be internally configured with nonstandard fixed output voltages. For details, contact the Linear Technology Marketing Department.

TYPICAL APPLICATIONS

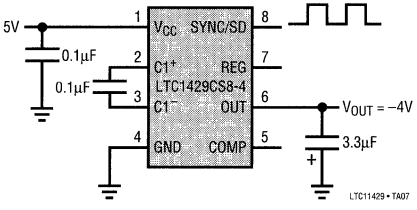
3.3V In, –4.5V Out GaAs FET Bias Generator



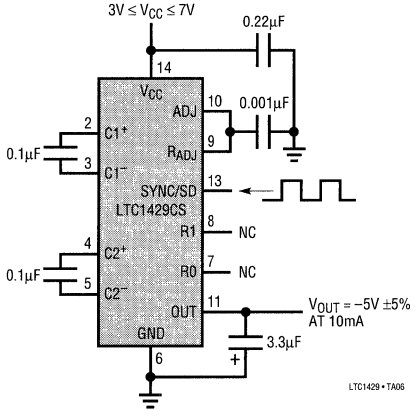
5V In, –4V Out GaAs FET Bias Generator



Minimum Parts Count –4V Generator

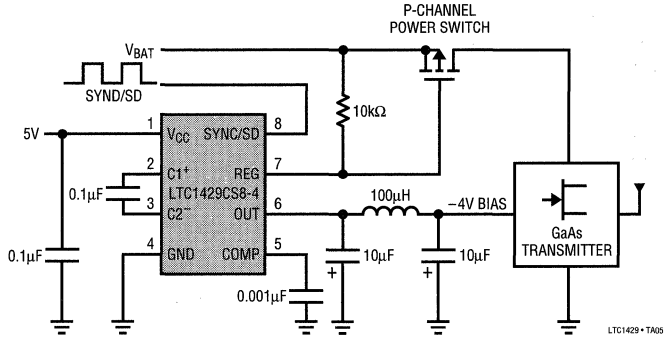


–5V Supply Generator



TYPICAL APPLICATIONS

1mV Ripple, 5V In, –4V Out GaAs FET Bias Generator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1121	Micropower Low Dropout Regulators with Shutdown	0.4V Dropout Voltage at 150mA, Low Noise, Switched Capacitor Regulated Voltage Inverter
LTC1261	Switched Capacitor Regulated Voltage Inverter	Selectable Fixed Output Voltage
LTC1550/LTC1551	Low Noise Switched Capacitor Regulated Voltage Inverter	GaAs FET Bias with Linear Regulator 1mV Ripple

100mA CMOS Voltage Converter

FEATURES

- **Simple Conversion of 5V to –5V Supply**
- **Output Drive: 100mA**
- **R_{OUT}: 6.5Ω (0.65V Loss at 100mA)**
- Boost Pin (Pin 1) for Higher Switching Frequency
- Inverting and Doubling Modes
- Minimum Open Circuit Voltage Conversion Efficiency: 99%
- Typical Power Conversion Efficiency with a 100mA Load: 88%
- Easy to Use

APPLICATIONS

- Conversion of 5V to ±5V Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems
- High Current Upgrade to LTC1044 or 7660

DESCRIPTION

The LTC®660 is a monolithic CMOS switched-capacitor voltage converter. It performs supply voltage conversion from positive to negative from an input range of 1.5V to 5.5V, resulting in complementary output voltages of –1.5V to –5.5V. It also performs a doubling at an input voltage range of 2.5V to 5.5V, resulting in a doubled output voltage of 5V to 11V. Only two external capacitors are needed for the charge pump and charge reservoir functions.

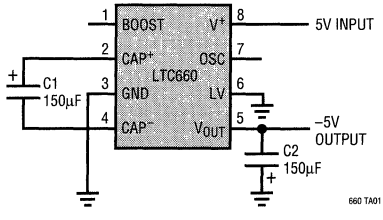
The converter has an internal oscillator that can be overdriven by an external clock or slowed down when connected to a capacitor. The oscillator runs at a 10kHz frequency when unloaded. A higher frequency outside the audio band can also be obtained if the Boost pin is tied to V^+.

The LTC660 contains an internal oscillator, divide-by-two, voltage level shifter and four power MOSFETs.

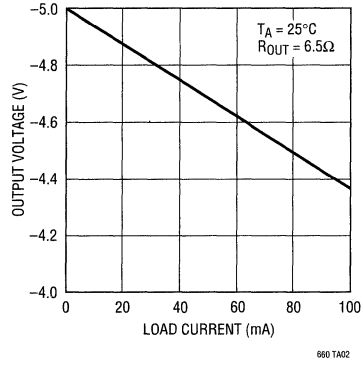
4

TYPICAL APPLICATION

Generating –5V from 5V



Output Voltage vs Load Current for V^+ = 5V

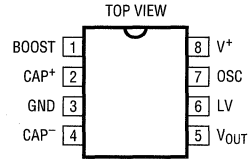


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+) 6V
Input Voltage on Pins 1, 6, 7
(Note 2) ..... $-0.3V < V_{IN} < (V^+ + 0.3V)$
Output Short-Circuit Duration to GND
(Note 5) ..... 1 sec
Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 100°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LTC660CN8 LTC660CS8
S8 PART MARKING
660

Consult Factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V^+ = 5V, C1 and C2 = 150µF, Boost = Open, C_{OSC} = 0pF, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
	Supply Voltage	R_L = 1k	Inverter, LV = Open	●	3		5.5	V
			Inverter, LV = GND	●	1.5		5.5	V
			Doubler, LV = V_{OUT}	●	2.5		5.5	V
I_S	Supply Current	No Load	Boost = Open	●		0.08	0.5	mA
			Boost = V^+	●		0.23	3	mA
I_{OUT}	Output Current	V_{OUT} More Negative Than −4V		●	100			mA
R_{OUT}	Output Resistance	I_L = 100mA (Note 3)		●		6.5	10	Ω
f_{OSC}	Oscillator Frequency	Boost = Open				10		kHz
		Boost = V^+ (Note 4)				45		kHz
	Power Efficiency	R_L = 1k Connected Between V^+ and V_{OUT}		●	96	98		%
		R_L = 500Ω Connected Between V_{OUT} and GND		●	92	96		%
		I_L = 100mA to GND				88		%
	Voltage Conversion Efficiency	No Load			99	99.96		%
	Oscillator Sink or Source Current	Boost = Open				±1.1		µA
		Boost = V^+				±5.0		µA

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals are at T_A = 25°C.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: Connecting any input terminal to voltages greater than V^+ or less than ground may cause destructive latch-up. It is recommended that no inputs from source operating from external supplies be applied prior to power-up of the LTC660.

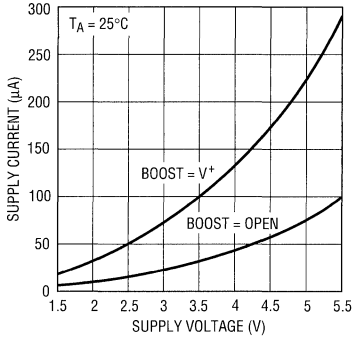
Note 3: The output resistance is a combination of internal switch resistance and external capacitor ESR. To maximize output voltage and efficiency, keep external capacitor ESR < 0.2Ω.

Note 4: f_{OSC} is tested with C_{OSC} = 100pF to minimize the effects of test fixture capacitance loading. The 0pF frequency is correlated to this 100pF test point, and is intended to simulate the capacitance at pin 7 when the device is plugged into a test socket and no external capacitor is used.

Note 5: OUT may be shorted to GND for 1 sec without damage, but shorting OUT to V^+ may damage the device and should be avoided. Also, for temperatures above 85°C, OUT must not be shorted to GND or V^+, even instantaneously, or device damage may result.

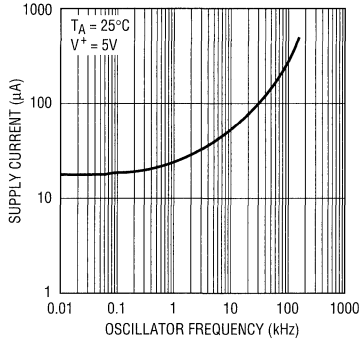
TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit in Figure 1)

Supply Current vs Supply Voltage



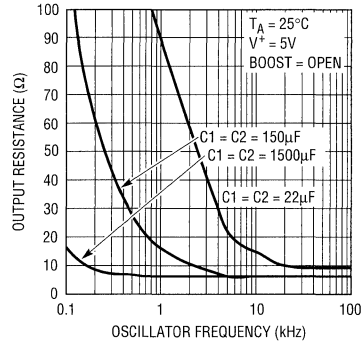
LTC660 • G01

Supply Current vs Oscillator Frequency



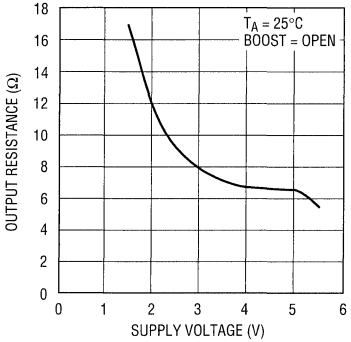
LTC660 • G02

Output Resistance vs Oscillator Frequency



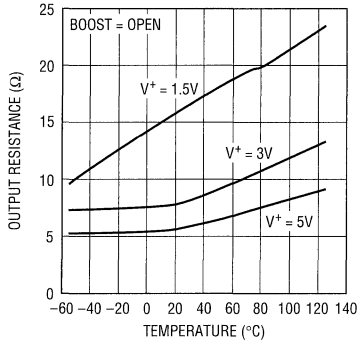
LTC660 • TPC03

Output Resistance vs Supply Voltage



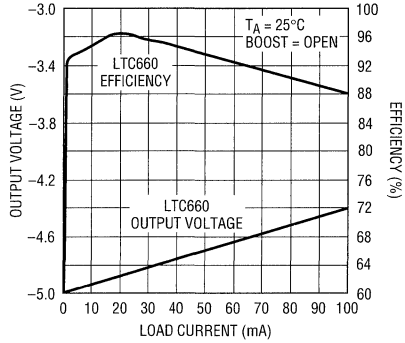
LTC690 • TPC04

Output Resistance vs Temperature



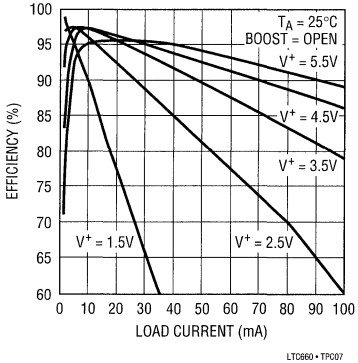
LTC660 • TPC05

Output Voltage and Efficiency vs Load Current, V^+ = 5V



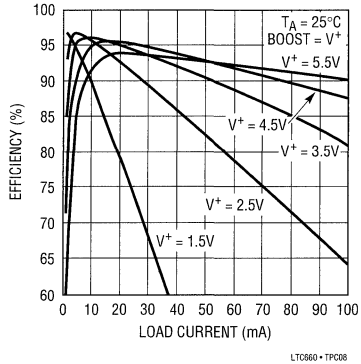
LTC660 • TPC06

Efficiency vs Load Current



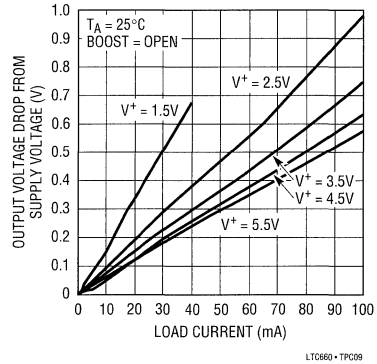
LTC660 • TPC07

Efficiency vs Load Current



LTC660 • TPC08

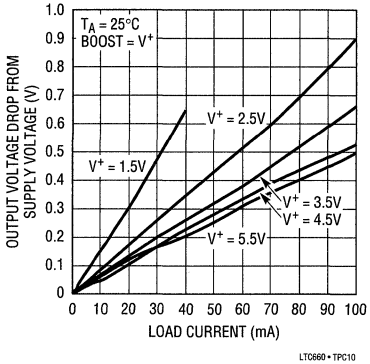
Output Voltage Drop vs Load Current



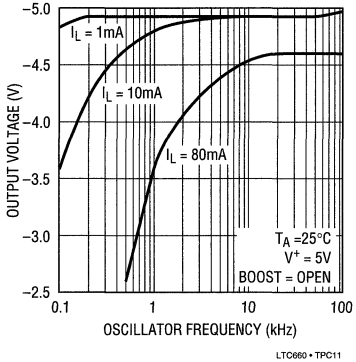
LTC660 • TPC09

TYPICAL PERFORMANCE CHARACTERISTICS (Using Test Circuit in Figure 1)

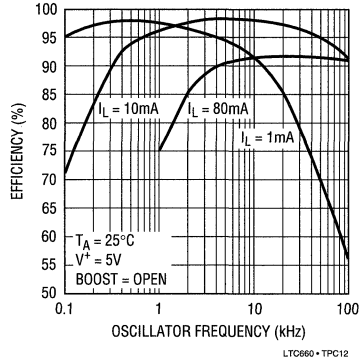
Output Voltage Drop vs Load Current



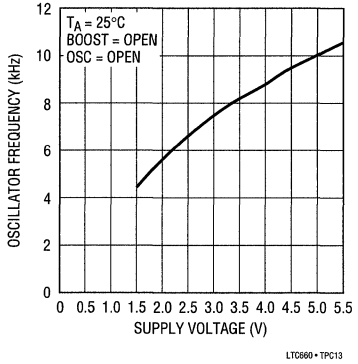
Output Voltage vs Oscillator Frequency



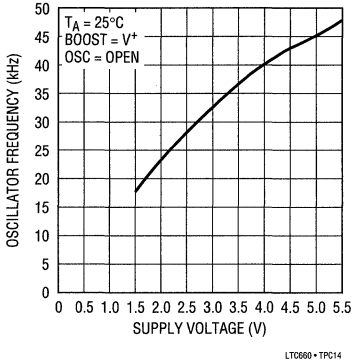
Efficiency vs Oscillator Frequency



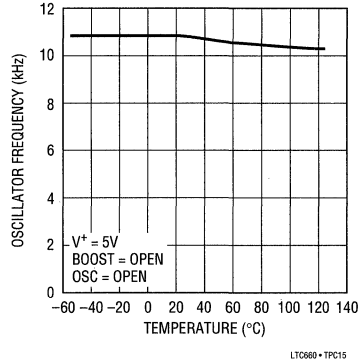
Oscillator Frequency vs Supply Voltage



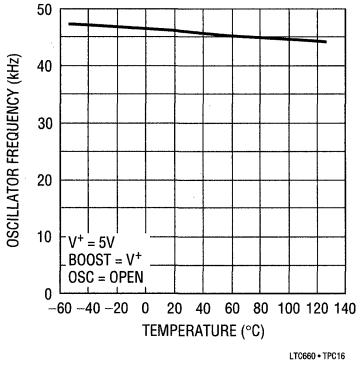
Oscillator Frequency vs Supply Voltage



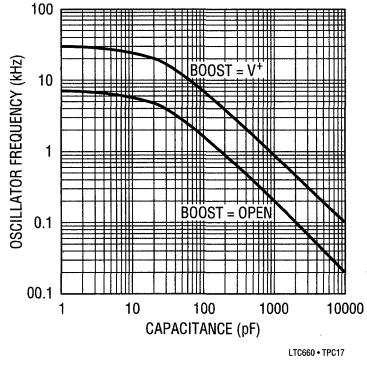
Oscillator Frequency vs Temperature



Oscillator Frequency vs Temperature



Oscillator Frequency vs External Capacitance



PIN FUNCTIONS

PIN	NAME	INVERTER	DOUBLER
1	BOOST	Internal Oscillator Frequency Control Pin. Boost = Open, f_{OSC} = 10kHz typ; Boost = V^+, f_{OSC} = 45kHz typ; when OSC is driven externally Boost has no effect.	Same
2	CAP^+	Positive Terminal for Charge Pump Capacitor	Same
3	GND	Power Supply Ground Input	Positive Voltage Input
4	CAP^-	Negative Terminal for Charge Pump Capacitor	Same
5	V_{OUT}	Negative Voltage Output	Power Supply Ground Input
6	LV	Tie LV to GND when the input voltage is less than 3V. LV may be connected to GND or left open for input voltages above 3V. Connect LV to GND when overdriving OSC.	LV must be tied to V_{OUT} for all input voltages.
7	OSC	An external capacitor can be connected to this pin to slow the oscillator frequency. Keep stray capacitance to a minimum. An external oscillator can be applied to this pin to overdrive the internal oscillator.	Same except standard logic levels will not be able to overdrive OSC pin.
8	V^+	Positive Voltage Input	Positive Voltage Output

4

TEST CIRCUIT

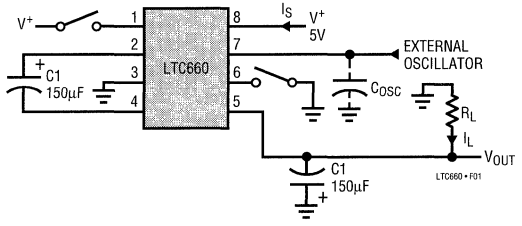


Figure 1. Test Circuit

APPLICATIONS INFORMATION

Theory of Operation

To understand the theory of operation for the LTC660, a review of a basic switched-capacitor building block is helpful. In Figure 2, when the switch is in the left position, capacitor C1 will charge to voltage V1. The total charge on C1 will be q1 = C1V1. The switch then moves to the right, discharging C1 to voltage V2. After this discharging time, the charge on C1 is q2 = C1V2. Note that charge has been transferred from the source V1 to the output V2. The amount of charge transferred is:

$$\Delta q = q1 - q2 = C1\ (V1 - V2)$$

If the switch is cycled "f" times per second, the charge transfer per unit time (i.e., current) is:

$$I = f \times \Delta q = f \times C1\ (V1 - V2)$$

Rewriting in terms of voltage and impedance equivalence,

$$I = \frac{V1 - V2}{1/fC1} = \frac{V1 - V2}{R_{EQUIV}}$$

A new variable R_{EQUIV} has been defined such that $R_{EQUIV} = 1/fC1$. Thus, the equivalent circuit for the switched-capacitor network is as shown in Figure 3.

Figure 4 shows that the LTC660 has the same switching action as the basic switched-capacitor building block.

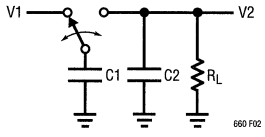


Figure 2. Switched-Capacitor Building Block

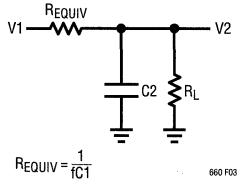


Figure 3. Switched-Capacitor Equivalent Circuit

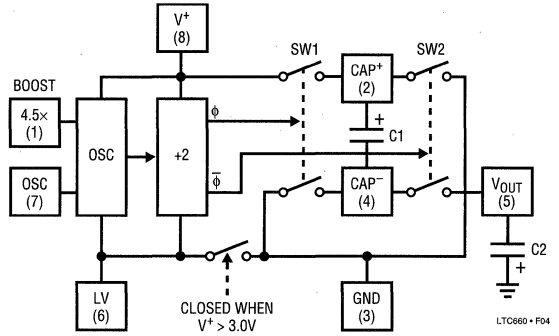


Figure 4. LTC660 Switched-Capacitor Voltage Converter Block Diagram

This simplified circuit does not include finite on-resistance of the switches and output voltage ripple, however, it does give an intuitive feel for how the device works. For example, if you examine power conversion efficiency as a function of frequency this simple theory will explain how the LTC660 behaves. The loss and hence the efficiency is set by the output impedance. As frequency is decreased, the output impedance will eventually be dominated by the 1/fC1 term and voltage losses will rise decreasing the efficiency. As the frequency increases the quiescent current increases. At high frequency this current loss becomes significant and the power efficiency starts to decrease.

The LTC660 oscillator frequency is designed to run where the voltage loss is a minimum. With the external 150µF capacitors the effective output impedance is determined by the internal switch resistances and the capacitor ESRs.

LV (Pin 6)

The internal logic of the LTC660 runs between V^+ and LV (pin 6). For $V^+ \geq 3V$, an internal switch shorts LV to ground (pin 3). For $V^+ < 3V$, the LV pin should be tied to ground. For $V^+ \geq 3V$, the LV pin can be tied to ground or left floating.

OSC (Pin 7) and Boost (Pin 1)

The switching frequency can be raised, lowered or driven from an external source. Figure 5 shows a functional diagram of the oscillator circuit.

APPLICATIONS INFORMATION

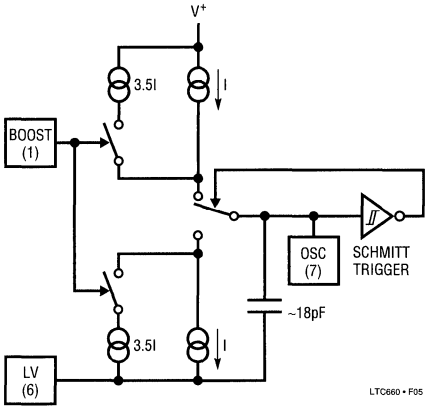


Figure 5. Oscillator

By connecting the Boost pin (pin 1) to V^+, the charge and discharge current is increased and, hence, the frequency is increased by approximately four and a half times. Increasing the frequency will decrease output impedance and ripple for high load currents.

Loading pin 7 with more capacitance will lower the frequency. Using the Boost (pin 1) in conjunction with external capacitance on pin 7 allows user selection of the frequency over a wide range.

Driving the LTC660 from an external frequency source can be easily achieved by driving pin 7 and leaving the Boost pin open, as shown in Figure 6. The output current from pin 7 is small, typically 1.1μA to 5μA, so a logic gate is capable of driving this current. (A CMOS logic gate can be used to drive the OSC pin.) For 5V applications, a TTL logic gate can be used by simply adding an external pull-up resistor (see Figure 6).

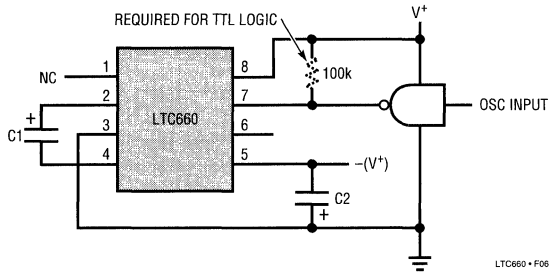


Figure 6. External Clocking

Capacitor Selection

While the exact values of C1 and C2 are noncritical, good quality, low ESR capacitors are necessary to minimize voltage losses at high currents. For C1 the effect of the ESR of the capacitor will be multiplied by four, due to the fact the switch currents are approximately two times higher than the output current and losses will occur on both the charge and discharge cycle. This means using a capacitor with 1Ω of ESR for C1 will have the same effect as increasing the output impedance of the LTC660 by 4Ω. This represents a significant increase in the voltage losses. For C2 the effect of ESR is less dramatic. A C2 with 1Ω of ESR will increase the output impedance by 1Ω. The size of C2 and the load current will determine the output voltage ripple. It is alternately charged and discharged at a current approximately equal to the output current. This will cause a step function to occur in the output voltage at the switch transitions. For example, for a switching frequency of 5kHz (one-half the nominal 10kHz oscillator frequency) and C2 = 150μF with an ESR of 0.2Ω, ripple is approximately 90mV with a 100mA load current.

TYPICAL APPLICATIONS

Negative Voltage Converter

Figure 7 shows a typical connection which will provide a negative supply from an available positive supply. This circuit operates over full temperature and power supply ranges without the need of any external diodes. The LV pin (pin 6) is shown grounded, but for $V^+ \geq 3V$, it may be floated, since LV is internally switched to ground (pin 3) for $V^+ \geq 3V$.

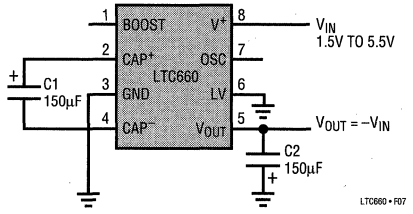


Figure 7. Voltage Inverter

The output voltage (pin 5) characteristics of the circuit are those of a nearly ideal voltage source in series with a 6.5Ω resistor. The 6.5Ω output impedance is composed of two terms: 1) the equivalent switched-capacitor resistance (see Theory of Operation), and 2) a term related to the on-resistance of the MOS switches.

At an oscillator frequency of 10kHz and C1 = 150µF, the first term is:

$$R_{EQUIV} = \frac{1}{(f_{OSC}/2) \times C1} =$$

$$\frac{1}{5 \times 10^3 \times 150 \times 10^{-6}} = 1.3\Omega.$$

Notice that the equation for R_{EQUIV} is not a capacitive reactance equation ($X_C = 1/\omega C$) and does not contain a 2π term.

The exact expression for output impedance is complex, but the dominant effect of the capacitor is clearly shown on the typical curves of output impedance and power efficiency versus frequency. For C1 = C2 = 150µF, the output impedance goes from 6.5Ω at f_{OSC} = 10kHz to 110Ω at f_{OSC} = 100Hz. As the 1/fC term becomes large compared to the switch on-resistance term, the output resistance is determined by 1/fC only.

Voltage Doubling

Figure 8 shows the LTC660 operating in the voltage doubling mode. The external Schottky (1N5817) diode is for start-up only. The output voltage is $2 \times V_{IN}$ without a load. The diode has no effect on the output voltage.

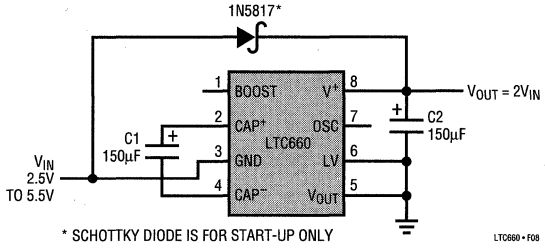


Figure 8. Voltage Doubler

Ultra-Precision Voltage Divider

An ultra-precision voltage divider is shown in Figure 9. To achieve the 0.002% accuracy indicated, the load current should be kept below 100nA. However, with a slight loss in accuracy, the load current can be increased.

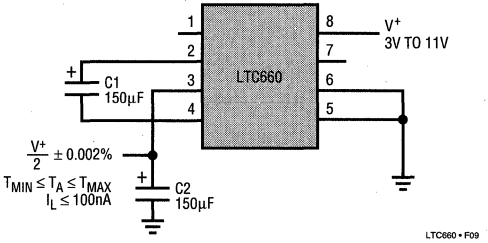


Figure 9. Ultra-Precision Voltage Divider

Battery Splitter

A common need in many systems is to obtain positive and negative supplies from a single battery or single power supply system. Where current requirements are small, the circuit shown in Figure 10 is a simple solution. It provides symmetrical positive or negative output voltages, both equal to one-half the input voltage. The output voltages are both referenced to pin 3 (Output Common).

TYPICAL APPLICATIONS

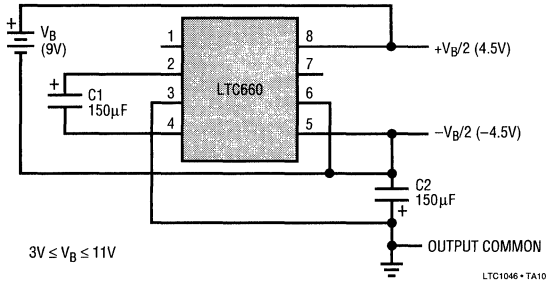


Figure 10. Battery Splitter

Paralleling for Lower Output Resistance

Additional flexibility of the LTC660 is shown in Figures 11 and 12. Figure 11 shows two LTC660s connected in parallel to provide a lower effective output resistance. If, however, the output resistance is dominated by 1/fC1, increasing the capacitor size (C1) or increasing the frequency will be of more benefit than the paralleling circuit shown.

Stacking for Higher Voltage

Figure 12 makes use of "stacking" two LTC660s to provide even higher voltages. In Figure 12, a negative voltage doubler or tripler can be achieved depending upon how pin 8 of the second LTC660 is connected, as shown schematically by the switch.

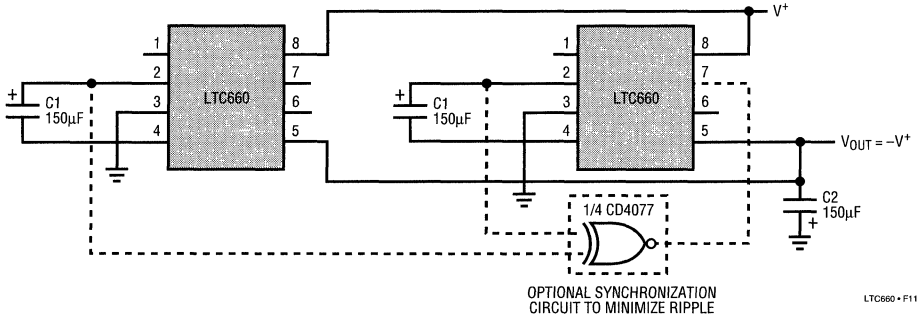


Figure 11. Paralleling for 200mA Load Current

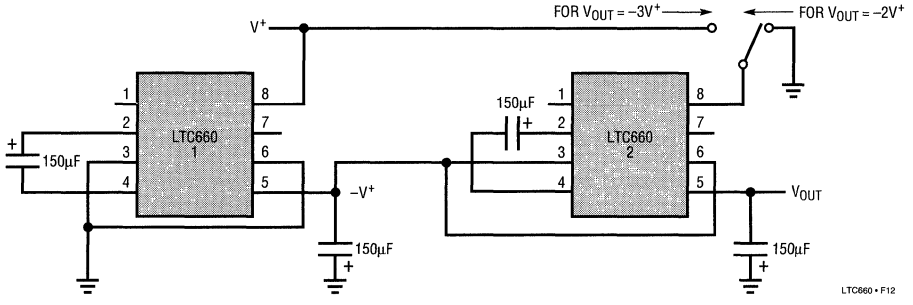


Figure 12. Stacking for High Voltage

RELATED PARTS

PART NUMBER	OUTPUT CURRENT	MAXIMUM V_{IN}	COMMENTS
Unregulated Output Voltage			
LTC660	100mA	6V	Highest Current
LTC1046	50mA	6V	
LTC1044	20mA	9.5V	Lowest Cost
LTC1044A	20mA	13V	
LTC1144	20mA	20V	Highest Voltage
Regulated Output Voltage			
LT1054	100mA	16V	Adjustable Output
LTC1262	30mA	6V	12V Fixed Output
LTC1261	10mA	9V	–4V, –4.5V and Adjustable Outputs

All devices are available in plastic 8-lead SO and PDIP packages

SECTION 4—POWER PRODUCTS

Low I_Q, Low Dropout, 800mA Source and Sink Regulators Fixed 2.5V, 2.85V, 5V Output

FEATURES

- **Regulates While Sourcing or Sinking Current**
- Provides Termination for up to 27 SCSI Lines
- **600µA Quiescent Current**
- Ultra-Low Power Shutdown Mode
- Current Limit and Thermal Shutdown Protection
- Stable for Any $C_{LOAD} \geq 0.22\mu F$
- Fast Settling Time
- 1V Dropout Voltage

APPLICATIONS

- Active Negation SCSI Terminations
- Computers
- Disk Drives
- CD-ROM
- Supply Splitter

DESCRIPTION

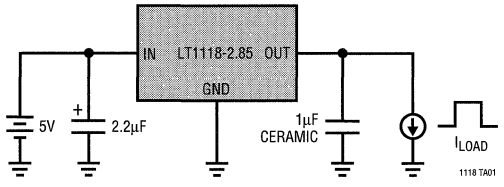
The LT®1118 family of low dropout regulators has the unique capability of maintaining output regulation while sourcing or sinking load current. The 2.85V output voltage regulator is ideal for use as a Boulay termination of up to 27 SCSI data lines. The regulator maintains regulation while both sourcing and sinking current, enabling the use of active negation drivers for improved noise immunity on the data lines. Regulation of output voltage is maintained for TERMPWR voltages as low as 4.0V. When unloaded, quiescent supply current is a low 600µA, allowing continuous connection to the TERMPWR lines. An ultra-low power shutdown mode is also available on the SO-8 version. In Shutdown the output is high impedance and supply current drops to less than 10µA.

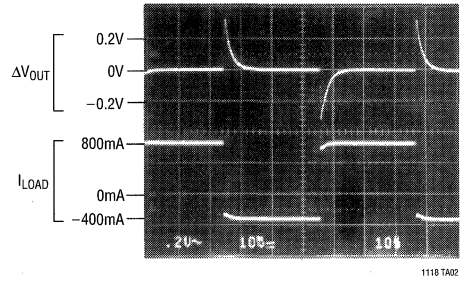
Current limits in both sourcing and sinking modes, plus on-chip thermal shutdown make the circuit tolerant of output fault conditions.

The LT1118 is available in 3-lead SOT-223 and 8-lead SO packages.

TYPICAL APPLICATION

Load Transient Response





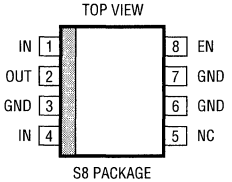
ABSOLUTE MAXIMUM RATINGS

Note 1)

Supply Voltage (V_{CC}) 15V
nput Voltage (Enable) ..... −0.2V to 7V
Output Voltage ..... −0.2V to V_{CC} + 0.5V

Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

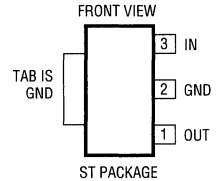
PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JC} = 15°C/W

ORDER PART NUMBER
LT1118CS8-2.5 LT1118CS8-2.85 LT1118CS8-5
S8 PART MARKING
111825 111828 11185



ST PACKAGE
3-LEAD PLASTIC SOT-223

T_{JMAX} = 125°C, θ_{JC} = 15°C/W

ORDER PART NUMBER
LT1118CST-2.5 LT1118CST-2.85 LT1118CST-5

Consult factory for Industrial and Military grade parts.

4

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Current (V_{IN})		V_{EN} = 5V	●		0.6	1	mA
Quiescent Current in Shutdown (V_{IN})		V_{EN} = 0V	●		1	10	µA
Enable Input Thresholds		Input Low Level Input High Level	● ●	0.8	1.4 1.4	 2.0	V V
Enable Input Current		0V ≤ V_{EN} ≤ 5V	●	−1		25	µA
Output Voltage	LT1118-2.5	No Load (25°C) All Operating Conditions (Note 3)	 ●	2.47 2.45	2.5 2.5	2.53 2.55	V V
	LT1118-2.85	No Load (25°C) All Operating Conditions (Note 3)	 ●	2.82 2.79	2.85 2.85	2.88 2.91	V V
	LT1118-5	No Load (25°C) All Operating Conditions (Note 3)	 ●	4.95 4.90	5.0 5.0	5.05 5.10	V V
Line Regulation (Note 4)	LT1118-2.5 LT1118-2.85 LT1118-5	I_L = 0mA, 4.2V ≤ V_{IN} ≤ 15V I_L = 0mA, 4.75V ≤ V_{IN} ≤ 15V I_L = 0mA, 6.5V ≤ V_{IN} ≤ 15V	● ● ●			6 6 10	mV mV mV
Load Regulation (Note 4)	LT1118-2.5	0mA ≤ I_L ≤ 800mA −400mA ≤ I_L ≤ 0mA	● ●			10 10	mV mV
	LT1118-2.85	0mA ≤ I_L ≤ 800mA −400mA ≤ I_L ≤ 0mA	● ●			10 10	mV mV
	LT1118-5	0mA ≤ I_L ≤ 800mA −400mA ≤ I_L ≤ 0mA	● ●			20 20	mV mV
Dropout Voltage (Note 5)		I_L = 100mA I_L = 800mA			0.85 1.0	1.1 1.3	V V
Ripple Rejection		f_{RIPPLE} = 120Hz, V_{IN} − V_{OUT} = 2V V_{RIPPLE} = 0.5V_{P-P}		60	80		dB

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Load Transient Settling Time, ΔV = 1%	0mA ≤ I_L ≤ 800mA, C_{LOAD} = 1μF −400mA ≤ I_L ≤ 0mA, C_{LOAD} = 1μF			5 5		μs μs
Output Short-Circuit Current, I_{SC}^+ I_{SC}^-	V_{OUT} = 0V V_{OUT} = V_{IN}		800	1200 −700	 −400	mA mA
Thermal Shutdown Junction Temperature	No Load			170		°C
Enable Turn-On Delay	No Load			50		μs

The ● denotes specifications which apply over the operating temperature range (0°C ≤ T_A ≤ 70°C for commercial grade).

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Unless otherwide specified, testing done at V_{CC} = 5V (LT1118-2.5, LT1118-2.85) or V_{CC} = 7V (LT1118-5). V_{EN} = V_{CC}. Output C_{LOAD} = 1μF, I_{LOAD} = 0.

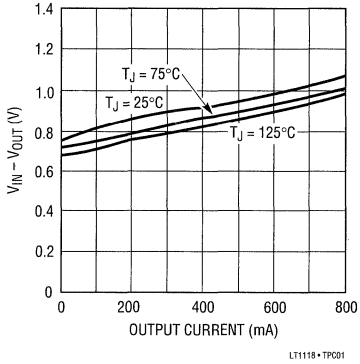
Note 3: All operating conditions include the combined effects of load current, input voltage, and temperature over each parameter's full range.

Note 4: Load and line regulation are tested at a constant junction temperature by low duty cycle pulse testing.

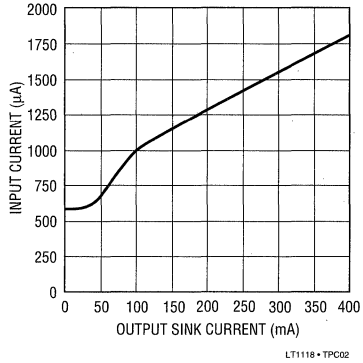
Note 5: Dropout voltage is defined as the minimum input to output voltage measured while sourcing the specified current.

TYPICAL PERFORMANCE CHARACTERISTICS

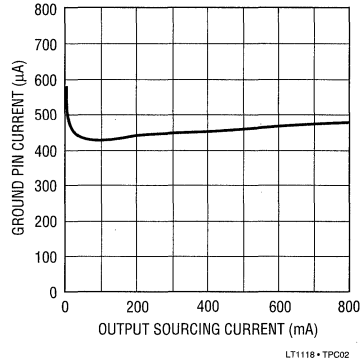
Dropout Voltage vs Output Current



Input Current vs Output Sink Current



Ground Pin Current vs Output Source Current



PIN FUNCTIONS

IN: Input Supply Pin. This pin should be decoupled with a 1μF or larger low ESR capacitor. The two IN pins on the SO-8 package must be directly connected on the printed circuit board to prevent voltage drops between the two inputs. When used as a SCSI active termination, IN connects to term power. When used as a supply splitter, IN is also the positive supply output.

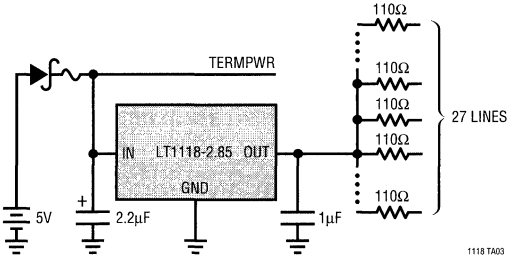
GND: Ground Pin. The three GND pins on the SO-8 package are internally connected, but lowest load regulation errors will result if these pins are tightly connected on the printed circuit board. This will also aid heat dissipation at high power levels.

EN: TTL/CMOS Logic Input. A high level allows normal operation. A low level reduces supply current to zero. This pin is internally connected to V_{IN} on 3-lead ST packaged devices.

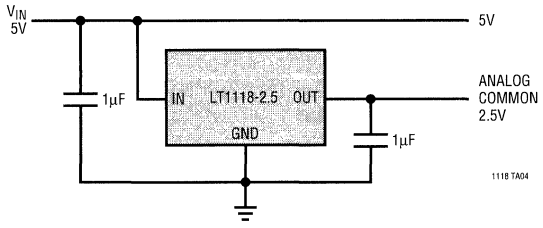
OUT: Regulated Output Voltage. Output can source or sink current. Current limit for sourcing and sinking current is provided to protect the device from fault conditons. The output must have a low ESR output filter capacitor. C_{OUT} ≥ 0.22μF to guarantee stability. A 0.1μF ceramic capacitor may be needed if the ESR of the main C_{OUT} ≥ 0.22μF is too high.

TYPICAL APPLICATIONS

SCSI Active Terminator



Power Supply Splitter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1005	Logic Controlled Regulator	5V, 1A Main Output Plus 35mA Auxilliary Output
LT1117	800mA Low Dropout Regulator	Fixed 2.85V, 3.3V, 5V or Adjustable Outputs
LT1120A	Micropower Regulator with Comparator and Shutdown	20µA Supply Current, 2.5V Reference Output
LT1121	Micropower Low Dropout Regulator with Shutdown	Reverse Voltage and Reverse Current Protection

4

500mA Negative Low Dropout Micropower Regulator

FEATURES

- Stable with Wide Range of Output Capacitors
- **Operating Current: 45µA**
- Shutdown Current: 10µA
- **Adjustable Current Limit**
- Positive or Negative Shutdown Logic
- **Low Voltage Linear Dropout Characteristics**
- Fixed 5V and Adjustable Versions
- Tolerates Reverse Output Voltage

APPLICATIONS

- Analog Systems
- Modems
- Instrumentation
- A/D and D/A Converters
- Interface Drivers
- Battery-Powered Systems

DESCRIPTION

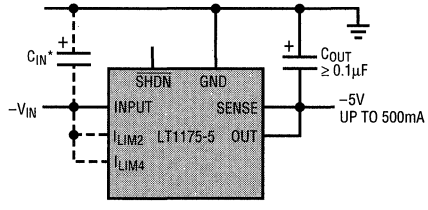
The LT®1175 is a negative micropower low dropout regulator. It features 45µA quiescent current, dropping to 10µA in shutdown. A new reference amplifier topology gives precision DC characteristics along with the ability to maintain good loop stability with an extremely wide range of output capacitors. Very low dropout voltage and high efficiency are obtained with a unique power transistor anti-saturation design. Adjustable and fixed 5V versions are available.

Several new features make the LT1175 very user-friendly. The shutdown pin can interface directly to either positive or negative logic levels. Current limit is user-selectable at 200mA, 400mA, 600mA and 800mA. The output can be forced to reverse voltage without damage or latch-up. Unlike some earlier designs, the increase in quiescent current during a dropout condition is actively limited.

The LT1175 has complete blowout protection with current limiting, power limiting, and thermal shutdown. Special attention was given to the problem of high temperature operation with micropower operating currents, preventing output voltage rise under no-load conditions. The LT1175 is available in 8-pin CERDIP, plastic DIP and SO packages, as well as 5-pin surface mount DD and through-hole TO-220 packages. The 8-pin SO package is specially constructed for low thermal resistance.

TYPICAL APPLICATION

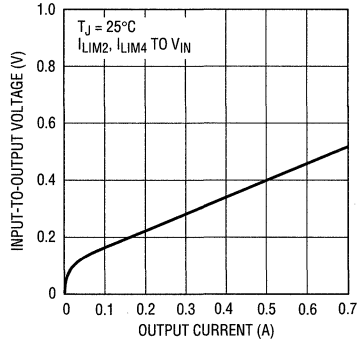
Typical LT1175 Connection



*C_{IN} IS NEEDED ONLY IF REGULATOR IS MORE THAN 6" FROM INPUT SUPPLY CAPACITOR. SEE APPLICATIONS INFORMATION SECTION FOR DETAILS

1175 TA01

Minimum Input-to-Output Voltage

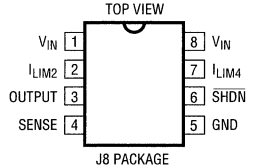


1175 TA02

ıBSOLUTE MAXIMUM RATINGS

ıput Voltage (Transient 1 sec, Note 10) 25V
ıput Voltage (Continuous) 20V
ıput-to-Output Differential Voltage 20V
V Sense Pin (with Respect to GND Pin) ..... 2V, –10V
DJ Sense Pin
(with Respect to Output Pin) ..... 20V, –0.5V
V Sense Pin
(with Respect to Output Pin) ..... 20V, – 7V
utput Reverse Voltage 2V
HDN Pin to GND Pin Voltage ..... 15V, –20V
$\overline{SHDN}$ Pin to V_{IN} Pin Voltage ..... 30V, –5V
Operating Junction Temperature Range
LT1175C ..... 0°C to 125°C
LT1175M ..... –55°C to 150°C
Ambient Operating Temperature Range
LT1175C ..... 0°C to 70°C
LT1175M ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

'ACKAGE/ORDER INFORMATION

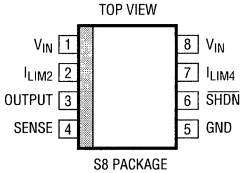


J8 PACKAGE
8-LEAD CERDIP
N8 PACKAGE
8-LEAD PDIP

θ_{JA} = 90°C/ W TO 120°C/W (J8)
θ_{JA} = 80°C/ W TO 120°C/W DEPENDING ON PC BOARD LAYOUT (N8)

ORDER PART NUMBER

LT1175CN8
LT1175CN8-5
LT1175MJ8



S8 PACKAGE
8-LEAD PLASTIC SO

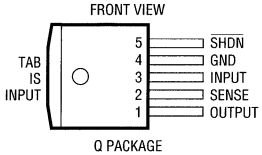
θ_{JA} = 120°C/W TO 170°C/W DEPENDING ON PC BOARD LAYOUT.
PINS 1, 8 ARE INTERNALLY CONNECTED TO DIE ATTACH PADDLE FOR HEAT SINKING. ELECTRICAL CONTACT CAN BE MADE TO EITHER PIN. FOR BEST THERMAL RESISTANCE, PINS 1, 8 SHOULD BE CONNECTED TO AN EXPANDED LAND THAT IS OVER AN INTERNAL OR BACKSIDE PLANE. SEE APPLICATIONS INFORMATION

ORDER PART NUMBER

LT1175CS8
LT1175CS8-5

S8 PART MARKING

1175
11755

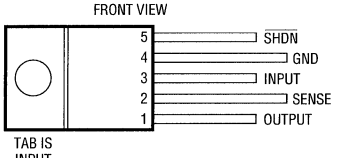


Q PACKAGE
5-LEAD PLASTIC DD

θ_{JA} = 27°C/ W TO 60°C/W DEPENDING ON PC MOUNTING. SEE APPLICATIONS INFORMATION FOR DETAILS

ORDER PART NUMBER

LT1175CQ
LT1175CQ-5



T PACKAGE
5-LEAD PLASTIC TO-220

θ_{JA} = 50°C/ W, θ_{JC} = 5°C/ W

ORDER PART NUMBER

LT1175CT
LT1175CT-5

ınsult factory for Industrial grade parts.

LECTRICAL CHARACTERISTICS

ıUT = 5V; V_{IN} = 7V, I_{OUT} = 0, V_{SHDN} = 3V, I_{LIM2} and I_{LIM4} tied to V_{IN}, T_J = 25°C, unless otherwise noted. To avoid confusion with nin" and "max" as applied to negative voltages, all voltages are shown as absolute values except where polarity is not obvious.

ıRAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
edback Sense Voltage	Adjustable Part		3.743	3.8	3.857	V
	Fixed 5V Part		4.93	5.0	5.075	V
ıtput Voltage Initial Accuracy	Adjustable, Measured at 3.8V Sense			0.5	1.5	%
	Fixed 5V			0.5	1.5	%
ıtput Voltage Accuracy (All Conditions)	$V_{IN} – V_{OUT}$ = 1V to V_{IN} = 25V, I_{OUT} = 0A to 500mA	●		1.5	2.5	%
	P = 0 to P_{MAX}, $T_J = T_{MIN}$ to T_{MAX} (Note 2)					

ELECTRICAL CHARACTERISTICS

V_{OUT} = 5V; V_{IN} = 7V, I_{OUT} = 0, V_{SHDN} = 3V, I_{LIM2} and I_{LIM4} tied to V_{IN}, T_J = 25°C, unless otherwise noted. To avoid confusion with "min" and "max" as applied to negative voltages, all voltages are shown as absolute values except where polarity is not obvious.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Quiescent Input Supply Current	$V_{IN} - V_{OUT}$ Up to 12V			45	65	µA
		●			80	µA
GND Pin Current Increase with Load (Note 3)		●		10	20	µA/mA
Input Supply Current in Shutdown	V_{SHDN} = 0V			10	20	µA
		●			25	µA
Shutdown Thresholds (Note 8)	Either Polarity on $\overline{\text{Shutdown}}$ Pin	●	0.8		2.5	V
$\overline{\text{Shutdown}}$ Pin Current (Note 1)	V_{SHDN} = 0V to 10V (Flows Into Pin)	●		4	8	µA
	V_{SHDN} = –15V to 0V (Flows Into Pin)			1	4	µA
Output Bleed Current in Shutdown (Note 5)	V_{OUT} = 0V, V_{IN} = 15V			0.1	1	µA
		●		1	5	µA
Sense Pin Input Current	(Adjustable Part Only, Current Flows Out of Pin)	●		75	150	nA
	(Fixed Voltage Only, Current Flows Out of Pin)	●		12	20	µA
Dropout Voltage (Note 6)	I_{OUT} = 25mA	●		0.1	0.2	V
	I_{OUT} = 100mA	●		0.18	0.26	V
	I_{OUT} = 500mA	●		0.5	0.7	V
	I_{LIM2} Open, I_{OUT} = 300mA	●		0.33	0.5	V
	I_{LIM4} Open, I_{OUT} = 200mA	●		0.3	0.45	V
	I_{LIM2}, I_{LIM4} Open, I_{OUT} = 100mA	●		0.26	0.4	V
Current Limit (Note 10)	$V_{IN} - V_{OUT}$ = 1V to 12V	●	520	800		mA
	I_{LIM2} Open	●	390	600		mA
	I_{LIM4} Open	●	260	400		mA
	I_{LIM2}, I_{LIM4} Open	●	130	200		mA
Line Regulation (Note 9)	$V_{IN} - V_{OUT}$ = 1V to V_{IN} = 25V	●		0.003	0.015	%/V
Load Regulation (Note 4, 9)	I_{OUT} = 0 to 500mA	●		0.1	0.25	%
Thermal Regulation	P = 0 to P_{MAX} (Notes 2, 7) 5-Pin Packages			0.04	0.1	%/W
	8-Pin Packages			0.1	0.2	%/W
Output Voltage Temperature Drift	T_J = 25°C to T_{JMIN}, or 25°C to T_{JMAX}			0.25	1.25	%

The ● denotes specifications which apply over the operating temperature range.

Note 1: $\overline{\text{Shutdown}}$ pin maximum positive voltage is 30V with respect to $-V_{IN}$ and 15V with respect to GND. Maximum negative voltage is –20V with respect to ground and –5V with respect to $-V_{IN}$.

Note 2: P_{MAX} = 1.5W for 8-pin packages, and 6W for 5-pin packages. This power level holds only for input-to-output voltages up to 12V, beyond which internal power limiting may reduce power. See Guaranteed Current Limit curve in Typical Performance Characteristics section. Note that all conditions must be met.

Note 3: Ground pin current increases because of power transistor base drive. At low input-to-output voltages (< 1V) where the power transistor is in saturation, Ground pin current will be slightly higher. See Typical Performance Characteristics.

Note 4: With I_{LOAD} = 0, at T_J > 125°C, power transistor leakage could increase higher than the 10µA to 25µA drawn by the output divider or fixed voltage Sense pin, causing the output to rise above the regulated value. To prevent this condition, an internal active pull-up will automatically turn on, but supply current will increase.

Note 5: This is the current required to pull the output voltage to within 1V of ground during shutdown.

Note 6: Dropout voltage is measured by setting the input voltage equal to the normal regulated output voltage and measuring the difference between V_{IN} and V_{OUT}. For currents between 100mA and 500mA, with both I_{LIM} pins tied to V_{IN}, maximum dropout can be calculated from $V_{DO} = 0.15 + 1.1\Omega\ (I_{OUT})$.

Note 7: Thermal regulation is a change in the output voltage caused by die temperature gradients, so it is proportional to chip power dissipation. Temperature gradients reach final value in less than 100ms. Output voltage changes after 100ms are due to absolute die temperature changes and reference voltage temperature coefficient.

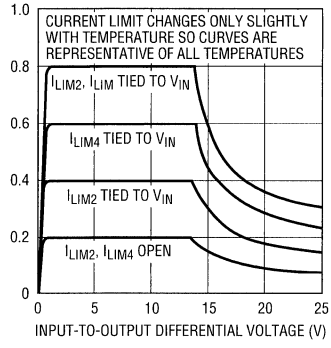
Note 8: The lower limit of 0.8V is guaranteed to keep the regulator in shutdown. The upper limit of 2.5V is guaranteed to keep the regulator active. Either polarity may be used, referenced to Ground pin.

Note 9: Load and line regulation are measured on a pulse basis with pulse width of 20ms or less to keep chip temperature constant. DC regulation will be affected by thermal regulation (Note 7) and chip temperature changes. Load regulation specification also holds for currents up to the specified current limit when I_{LIM2} or I_{LIM4} are left open.

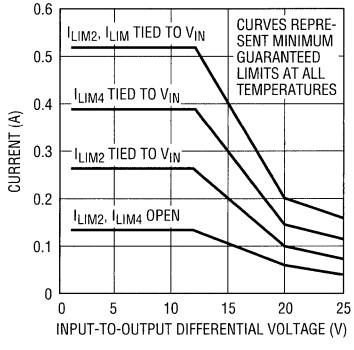
Note 10: Current limit is reduced for input-to-output voltage above 12V. See the graph in Typical Performance Characteristics for guaranteed limits above 12V.

TYPICAL PERFORMANCE CHARACTERISTICS

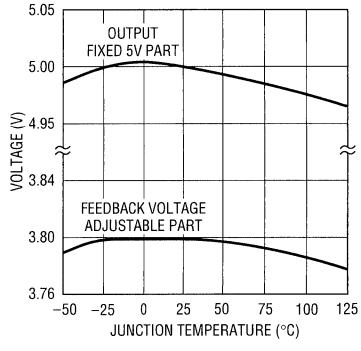
Typical Current Limit Characteristics



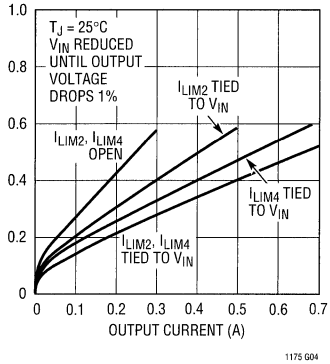
Guaranteed Current Limit



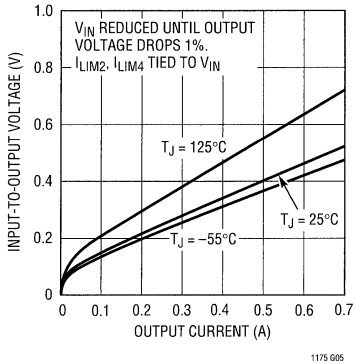
Output Voltage Temperature Drift



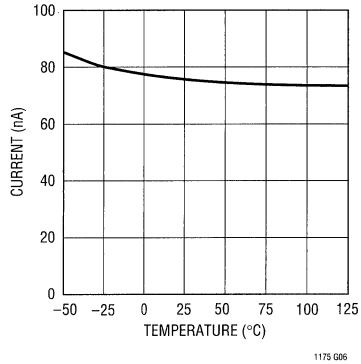
Minimum Input-to-Output Voltage



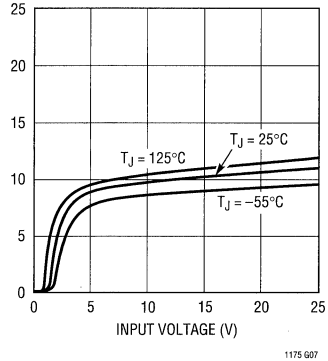
Minimum Input-to-Output Voltage



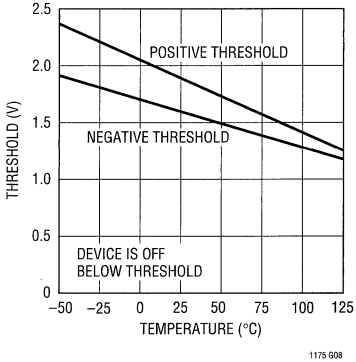
Sense Bias Current (Adjustable Part)



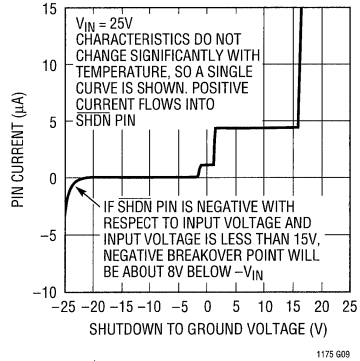
Shutdown Input Current



Shutdown Thresholds



$\overline{\text{Shutdown}}$ Pin Characteristics



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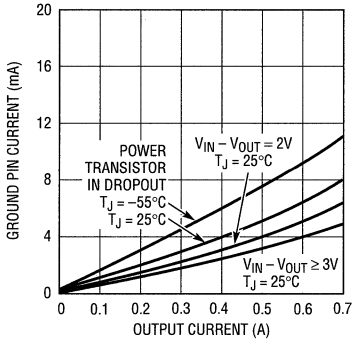
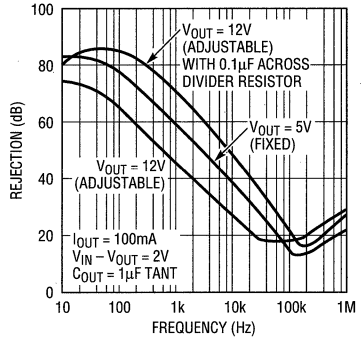
TYPICAL PERFORMANCE CHARACTERISTICS

Ground Pin Current



Ripple Rejection



RIPPLE REJECTION IS RELATIVELY INDEPENDENT OF INPUT VOLTAGE AND LOAD FOR CURRENTS BETWEEN 25mA AND 500mA. LARGER OUTPUT CAPACITORS DO NOT IMPROVE REJECTION FOR FREQUENCIES BELOW 50kHz. AT VERY LIGHT LOADS, REJECTION WILL IMPROVE WITH LARGER OUTPUT CAPACITORS 1175 G11

PIN FUNCTIONS

SENSE Pin: The Sense pin is used in the adjustable version to allow custom selection of output voltage, with an external divider set to generate 3.8V at the Sense pin. Input bias current is typically 75nA flowing out of the pin. Maximum forced voltage on the Sense pin is 2V and –10V with respect to Ground pin.

The fixed 5V version utilizes the Sense pin to give true Kelvin connections to the load or to drive an external pass transistor for higher output currents. Bias current out of the 5V Sense pin is approximately 12µA. Separating the Sense and Output pins also allows for a new loop compensation technique described in the Applications Information section.

$\overline{\text{SHDN}}$ Pin: The $\overline{\text{Shutdown}}$ pin is specially configured to allow it to be driven from either positive voltage logic or with negative only logic. Forcing the $\overline{\text{Shutdown}}$ pin 2V either above or below the Ground pin will turn the regulator on. This makes it simple to connect directly to positive logic signals for active low $\overline{\text{shutdown}}$. If no positive voltages are available, the $\overline{\text{Shutdown}}$ pin can be driven below the Ground pin to turn the regulator on. *When left open, the $\overline{\text{Shutdown}}$ pin will default low to a regulator "on" condition.* For all voltages below absolute maximum ratings, the $\overline{\text{Shutdown}}$ pin draws only a few microamperes of current (see Typical Performance Characteristics). Maximum voltage on the $\overline{\text{Shutdown}}$ pin is 15V, –20V with respect to the Ground pin and 35V, –5V with respect to the negative Input pin.

I_{LIM} Pins: The two Current Limit pins are emitter sections of the power transistor. When left open, they float several hundred millivolts above the negative input voltage. When shorted to the input voltage, they increase current limit by a minimum of 200mA for I_{LIM2} and 400mA for I_{LIM4}. These pins must be connected only to the input voltage, either directly or through a resistor.

OUTPUT Pin: The Output pin is the collector of the NPN power transistor. It can be forced to the input voltage, to ground or up to 2V positive with respect to ground without damage or latch-up (see Output Voltage Reversal in Applications Information section). The LT1175 has foldback current limit, so maximum current at the Output pin is a function of input-to-output voltage. See Typical Performance Characteristics.

GND Pin: The Ground pin has a quiescent current of 45µA at zero load current, increasing by approximately 10µA per mA of output current. At 500mA output current, Ground pin current is about 5mA. Current flows into the Ground pin.

PPLICATIONS INFORMATION

lote to Reader: To avoid confusion when working with egative voltages (is –6V more or less than –5V?), I have ecided to treat the LT1175 as if it were a positive egulator and express all voltages as positive values, both ı text and in formulas. If you do the same and simply add negative sign to the eventual answer, confusion should e avoided. Please don't give me a hard time about preciseness" or "correctness." I have to field phone calls om around the world and this is my way of dealing with multitude of conventions. Thanks for your patience.

tting Output Voltage

ıe LT1175 adjustable version has a feedback sense ltage of 3.8V with a bias current of approximately 75nA wing out of the Sense pin. To avoid output voltage rors caused by this current, the output divider string ee Figure 1) should draw about 25µA. Table 1 shows ggested resistor values for a range of output voltages. ıe second part of the table shows resistor values which aw only 10µA of current. Output voltage error caused by as current with the lower valued resistors is about 0.4% aximum and with the higher values, about 1% maxi- um. A formula is also shown for calculating the resistors r any output voltage.

ble 1.

UTPUT OLTAGE	R1 I_{DIV} = 25µA	R2 NEAREST 1%	R1 I_{DIV} = 10µA	R2 NEAREST 1%
5V	150k	47.5k	383k	121k
6V	150k	86.6k	383k	221k
8V	150k	165k	383k	422k
10V	150k	243k	383k	619k
12V	150k	324k	383k	825k
15V	150k	442k	383k	1.13M

$$R1 = \frac{3.8V}{I_{DIV}}$$

$$R2 = \frac{R1(V_{OUT} - 3.8V)}{3.8V} \quad \text{(Simple formula)}$$

$$R2 = \frac{R1(V_{OUT} - 3.8V)}{3.8V + R1(I_{FB})} \quad \left(\begin{array}{l}\text{Taking Sense pin bias}\\ \text{current into account}\end{array}\right)$$

I_{DIV} = Desired divider current

The LT1175-5 is a fixed 5V design with the Sense pin acting as a Kelvin connection to the output. Normally the Sense pin and the Output pin are connected directly together, either close to the regulator or at the remote load point.

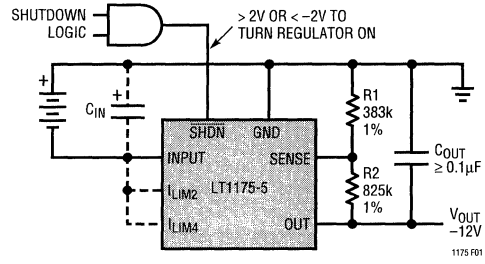


Figure 1. Typical LT1175 Adjustable Connection

Setting Current Limit

The LT1175 uses two I_{LIM} pins to set current limit (typical) at 200mA, 400mA, 600mA or 800mA. The corresponding minimum guaranteed currents are 130mA, 260mA, 390mA and 520mA. This allows the user to select a current limit tailored to his specific application and prevents the situation where short-circuit current is many times higher than full-load current. Problems with input supply overload or excessive power dissipation in a faulted load are prevented. Power limiting in the form of foldback current limit is built-in and reduces current limit as a function of input-to-output voltage differential for differentials exceeding 14V. See the graph in Typical Performance Characteristics. The LT1175 is guaranteed to be blowout-proof regardless of current limit setting. The power limiting combined with thermal shutdown protects the device from destructive junction temperatures under all load conditions.

Shutdown

In shutdown, the LT1175 draws only about 10µA. Special circuitry is used to minimize increases in shutdown current at high temperatures, but a slight increase is seen above 125°C. One option *not taken* was to actively pull down on the output during shutdown. This means that the output will fall slowly after shutdown is initiated, at a rate determined by load current plus the 12µA internal load, and the size of the output capacitor. Active pull-down is

APPLICATIONS INFORMATION

normally a good thing when the regulator is used by itself, but it prevents the user from shutting down the regulator when a second power source is connected to the LT1175 output. If active output pull-down is needed in shutdown, it can be added externally with a depletion mode PFET as shown in Figure 2. Note that the maximum pinch-off voltage of the PFET must be less than the positive logic high level to ensure that the device is completely off when the regulator is active. The Motorola J177 device has 300Ω on resistance for zero gate source voltage.

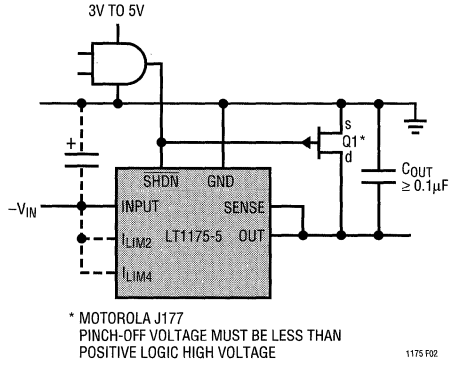


Figure 2. Active Output Pull-Down During Shutdown

Minimum Dropout Voltage

Dropout voltage is the minimum voltage required between input and output to maintain proper output regulation. For older three-terminal regulator designs, dropout voltage was typically 1.5V to 3V. The LT1175 uses a saturating power transistor design which gives much lower dropout voltage, typically 100mV at light loads and 450mV at full load. Special precautions were taken to ensure that this technique does not cause quiescent supply current to be high under light load conditions. When the regulator input voltage is too low to maintain a regulated output, the pass transistor is driven hard by the error amplifier as it tries to maintain regulation. The current drawn by the driver transistor could be tens of milliamperes even with little or no load on the output. This indeed was the case for older IC designs that did not actively limit driver current when the power transistor saturated. The LT1175 uses a new anti-saturation technique that prevents high driver current, yet allows the power transistor to approach its theoretical saturation limit.

Output Capacitor

Several new regulator design techniques are used to make the LT1175 extremely tolerant of output capacitor selection. Like most low dropout designs which use a collector or drain of the power transistor to drive the output node the LT1175 uses the output capacitor as part of the overall loop compensation. Older regulators generally require the output capacitor to have a minimum value of 1μF to 100μF, a *maximum* ESR (Effective Series Resistance) of 0.1Ω to 1Ω and a *minimum* ESR in the range of 0.03Ω to 0.3Ω. These restrictions usually could be met only with good quality solid tantalum capacitors. Aluminum capacitors have problems with high ESR unless much higher values of capacitance are used (physically large). The ESR of ceramic or film capacitors was too *low*, which made the capacitance/ESR zero frequency too high to maintain phase margin in the regulator. Even with optimum capacitors, loop phase margin was very low in previous designs when output current was low. These problems led to a new design technique for the LT1175 error amplifier and internal frequency compensation as shown in Figure 3.

A conventional regulator loop consists of error amplifier A1, driver transistor Q2 and power transistor Q1. Added to this basic loop are secondary loops generated by Q3 and C_F. A DC negative feedback current fed into the error amplifier through Q3 and R_N causes overall loop current gain to be very low at light load currents. This is not a problem because very little gain is needed at light loads. In addition to low gain, the parasitic pole frequency at Q2 base is extended by the DC feedback. The combination of these two effects dramatically improves loop phase margin at light loads and makes the loop tolerant of large ESR in the output capacitor. With heavy loads, loop phase and gain are not nearly as troublesome and large negative feedback could degrade regulation. The logarithmic behavior of the base emitter voltage of Q1 reduces Q3 negative feedback at heavy loads to prevent poor regulation.

In a conventional design, even with the nonlinear feedback, poor loop phase margin would occur at medium to heavy loads if the ESR of the output capacitor fell below

APPLICATIONS INFORMATION

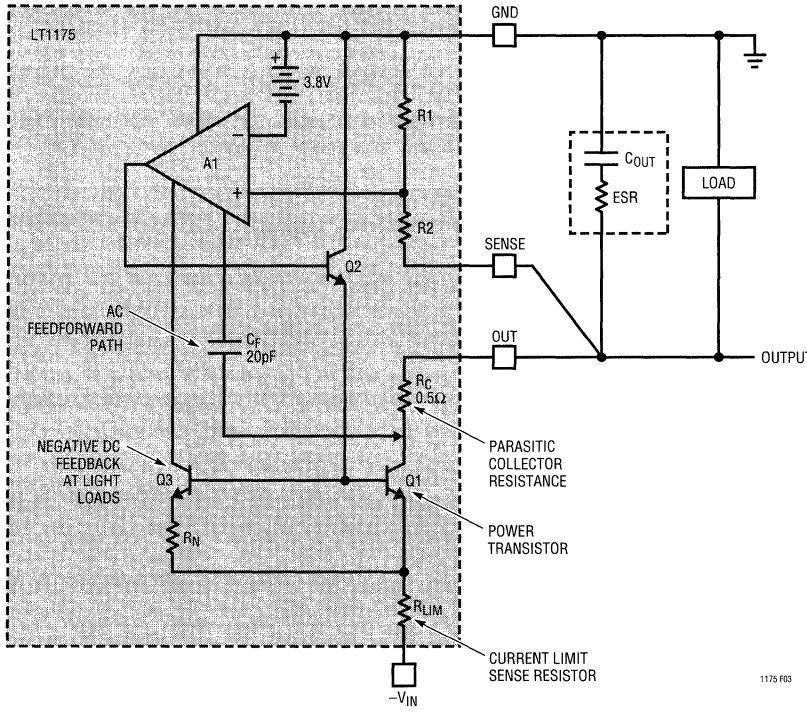


Figure 3.

0.3Ω. This condition can occur with ceramic or film capacitors which often have an ESR under 0.1Ω. With previous designs, the user was forced to add a real resistor in series with the capacitor to guarantee loop stability. The LT1175 uses a unique AC feedforward technique to eliminate this problem. C_F is a conventional feedforward capacitor often used in regulators to cancel the pole formed by the output capacitor. It would normally be connected from the regulated output node to the feedback node at the R1/R2 junction or to an internal node on the amplifier as shown. In this case, however, the capacitor is connected to the internal structure of the power transistor. R_C is the unavoidable parasitic collector resistance of the power transistor. Access to the node at the bottom of R_C is available only in monolithic structures where Kelvin connections can be made to the NPN buried collector layer. The loop now responds as if R_C were in series with the output capacitor and good loop stability is achieved even with extremely low ESR in the output capacitor.

The end result of all this attention to loop stability is that the output capacitor used with the LT1175 can range in value from 0.1μF to hundreds of microfarads, with an ESR from 0Ω to 10Ω. This range allows the use of ceramic, solid tantalum, aluminum and film capacitors over a wide range of values.

The optimum output capacitor type for the LT1175 is still solid tantalum, but there is considerable leeway in selecting the exact unit. If large load current transients are expected, larger capacitors with lower ESR may be needed to control worst case output variation during transients. If transients are not an issue, the capacitor can be chosen for small physical size, low price, etc. Concerns about surge currents in tantalum capacitors are not an issue for the

APPLICATIONS INFORMATION

output capacitor because the LT1175 limits inrush current to well below the level which can cause capacitor damage. Surges caused by shorting the regulator output are also not a problem because tantalum capacitors do not fail during a "shorting out" surge, only during a "charge up" surge.

The output capacitor should be located within several inches of the regulator. If remote sensing is used, the output capacitor can be located at the remote sense node, but the ground pin of the regulator should also be connected to the remote site. The basic rule is to keep Sense and Ground pins close to the output capacitor, regardless of where it is.

Input Capacitor

The LT1175 requires a separate input bypass capacitor only if the regulator is located more than six inches from the raw supply output capacitor. A 1μF or larger tantalum capacitor is suggested for all applications, but if low ESR capacitors such as ceramic or film are used for the output *and* input capacitors, the input capacitor should be at least three times the value of the output capacitor. If a solid tantalum or aluminum electrolytic output capacitor is used, the input capacitor is very noncritical.

High Temperature Operation

The LT1175 is a micropower design with only 45μA quiescent current. This could make it perform poorly at high temperatures (>125°C), where power transistor leakage might exceed the output node loading current (5μA to 15μA). To avoid a condition where the output voltage drifts uncontrolled high during a high temperature no-load condition, the LT1175 has an active load which turns on when the output is pulled above the nominal regulated voltage. This load absorbs power transistor leakage and maintains good regulation. There is one downside to this feature, however. If the output is pulled high deliberately, as it might be when the LT1175 is used as a backup to a slightly higher output from a primary regulator, the LT1175 will act as an unwanted load on the primary regulator. Because of this, the active pull-down is deliberately "weak." It can be modeled as a 2k resistor in series with an internal clamp voltage when the regulator output is being pulled high. If a 4.8V output is pulled to 5V, for instance, the load on the primary regulator would be (5V – 4.8V)/2kΩ = 100μA. This also means that if the internal pass transistor leaks 50μA, the output voltage will be (50μA)(2kΩ) = 100mV high. This condition will not occur under normal operating conditions, but could occur immediately after an output short circuit had overheated the chip.

Thermal Considerations

The LT1175 is available in a special 8-pin surface mount package which has pins 1 and 8 connected to the die attach paddle. This reduces thermal resistance when pins 1 and 8 are connected to expanded copper lands on the PC board. Table 2 shows thermal resistance for various combinations of copper lands and backside or internal planes. Table 2 also shows thermal resistance for the 5-pin DD surface mount package and the 8-pin DIP and CERDIP packages.

Table 2. Package Thermal Resistance (°C/W)

LAND AREA	DIP	CERDIP	SO	Q
Minimum	140	120	170	60
Minimum with Backplane	110	100	150	50
1cm^2 Top Plane with Backplane	100	90	135	35
10cm^2 Top Plane with Backplane	80	90	120	27

To calculate die temperature, maximum power dissipation or maximum input voltage, use the following formulas with correct thermal resistance numbers from Table 2. For through-hole TO-220 applications use θ_{JA} = 50°C/W without a heat sink and θ_{JA} = 5°C/W + heat sink thermal resistance when using a heat sink.

$$\text{Die Temp} = T_A + \theta_{JA}\left(V_{IN} - V_{OUT}\right)\left(I_{LOAD}\right)$$

$$\text{Maximum Power Dissipation} = \frac{T_{MAX} - T_A}{\theta_{JA}}$$

$$\text{Maximum Input Voltage for Thermal Considerations} = \frac{T_{MAX} - T_A}{\theta_{JA}\left(I_{LOAD}\right)} + V_{OUT}$$

APPLICATIONS INFORMATION

T_A = Maximum ambient temperature

T_{MAX} = Maximum LT1175 die temperature (125°C for commercial and industrial, 150°C for military)

θ_{JA} = LT1175 thermal resistance, junction to ambient

V_{IN} = Maximum continuous input voltage at maximum load current

I_{LOAD} = Maximum load current

Example: LT1175S8 with I_{LOAD} = 200mA, V_{OUT} = 5V, V_{IN} = 7V, T_A = 60°C. Maximum die temperature for the LT1175S8 is 125°C. Thermal resistance from Table 2 is found to be 80°C/W.

Die Temperature = 60 + 80 (0.2A)(8 – 5) = 108°C

$$\text{Maximum Power Dissipation} = \frac{125-60}{80} = 0.81W$$

$$\text{Maximum Continuous Input Voltage (for Thermal Considerations)} = \frac{125-60}{80(0.2)} + 5 = 9V$$

Output Voltage Reversal

The LT1175 is designed to tolerate an output voltage reversal of up to 2V. Reversal might occur, for instance, if the output was shorted to a positive 5V supply. This would almost surely destroy IC devices connected to the negative output. Reversal could also occur during start-up if the positive supply came up first and loads were connected between the positive and negative supplies. *For these reasons, it is always good design practice to add a reverse biased diode from each regulator output to ground to limit output voltage reversal.* The diode should be rated to handle full negative load current for start-up situations, or the short-circuit current of the positive supply if supply-to-supply shorts must be tolerated.

Input Voltage Lower Than Output

Linear Technology's positive low dropout regulators LT1121 and LT1129, will not draw large currents if the input voltage is less than the output. These devices use a lateral PNP power transistor structure that has 40V emitter base breakdown voltage. *The LT1175, however, uses an NPN power transistor structure that has a parasitic diode between the input and output of the regulator.* Reverse voltages between input and output above 1V will damage the regulator if large currents are allowed to flow. Simply disconnecting the input source with the output held up will not cause damage even though the input-to-output voltage will become slightly reversed.

High Frequency Ripple Rejection

The LT1175 will sometimes be powered from switching regulators that generate the unregulated or quasi-regulated input voltage. This voltage will contain high frequency ripple that must be rejected by the linear regulator. Special care was taken with the LT1175 to maximize high frequency ripple rejection, but as with any micropower design, rejection is strongly affected by ripple frequency. The graph in the Typical Performance Characteristics section shows 60dB rejection at 1kHz, but only 15dB rejection at 100kHz for the 5V part. Photographs in Figures 4a and 4b show actual output ripple waveforms with square wave and tri-wave input ripple.

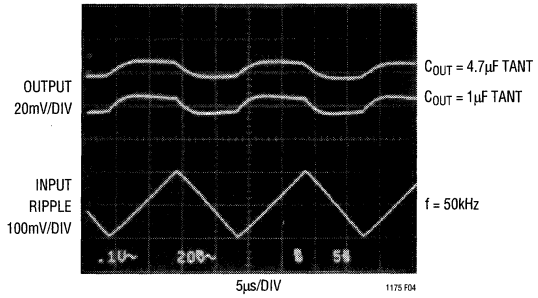


Figure 4a.

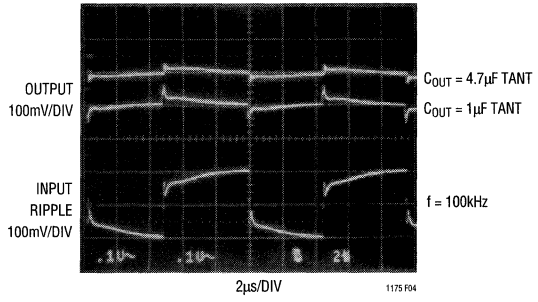


Figure 4b.

APPLICATIONS INFORMATION

To estimate regulator output ripple under different conditions, the following general comments should be helpful:

1. Output ripple at high frequency is only weakly affected by load current or output capacitor size for medium to heavy loads. At very light loads (<10mA), higher frequency ripple may be reduced by using larger output capacitors.
2. A feedforward capacitor across the resistor divider used with the adjustable part is effective in reducing ripple only for output voltages greater than 5V and only for frequencies less than 100kHz.
3. Input-to-output voltage differential has little effect on ripple rejection until the regulator actually enters a dropout condition of 0.2V to 0.6V.

If ripple rejection needs to be improved, an input filter can be added. This filter can be a simple RC filter using a 1Ω to 10Ω resistor. A 3.3Ω resistor for instance, combined with a 0.3Ω ESR solid tantalum capacitor, will give an additional 20dB ripple rejection. The size of the resistor will be dictated by maximum load current. If the maximum voltage drop allowable across the resistor is "V_R," and maximum load current is I_{LOAD}, $R = V_R/I_{LOAD}$. At light loads, larger resistors and smaller capacitors can be used to save space. At heavier loads an inductor may have to be used in place of the resistor. The value of the inductor can be calculated from:

$$L_{FIL} = \frac{ESR}{2\pi(f)\left(10^{rr/20}\right)}$$

ESR = Effective series resistance of filter capacitor. This assumes that the capacitive reactance is small compared to ESR, a reasonable assumption for solid tantalum capacitors above 2.2μF and 50kHz.

f = Ripple frequency

rr = Ripple rejection ratio of filter in dB

Example: ESR = 1.2Ω, f = 100kHz, rr = –25dB.

$$L_{FIL} = \frac{1.2}{6.3\left(10^{5}\right)\left(10^{-25/20}\right)} = 34\mu H$$

Solid tantalum capacitors are suggested for the filter to keep filter Q fairly low. This prevents unwanted ringing at the resonant frequency of the filter and oscillation problems with the filter/regulator combination.

RELATED PARTS

LT1121	150mA Positive Micropower Low Dropout Regulator with Shutdown
LT1129	700mA Positive Micropower Low Dropout Regulator with Shutdown
LT1185	3A Negative Low Dropout Regulator
LT1521	300mA Positive Micropower Low Dropout Regulator with Shutdown
LT1529	3A Positive Micropower Low Dropout Regulator with Shutdown

300mA Low Dropout Regulators with Micropower Quiescent Current and Shutdown

FEATURES

- **Dropout Voltage: 0.5V**
- **Output Current: 300mA**
- **Quiescent Current: 12μA**
- **No Protection Diodes Needed**
- Adjustable Output from 3.8V to 20V
- Fixed Output Voltages: 3V, 3.3V, 5V
- Controlled Quiescent Current in Dropout
- Shutdown I_Q = 6μA
- 5μA Quiescent Current in Shutdown
- Reverse Battery Protection
- No Reverse Current
- Thermal Limiting

APPLICATIONS

- Low Current Regulator
- Regulator for Battery-Powered Systems
- Post Regulator for Switching Supplies

DESCRIPTION

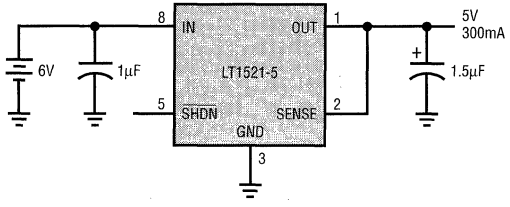
The LT®1521/LT1521-3/LT1521-3.3/LT1521-5 are low dropout regulators with micropower quiescent current and shutdown. These devices are capable of supplying 300mA of output current with a dropout voltage of 0.5V. Designed for use in battery-powered systems, the low quiescent current, 12μA operating and 6μA in shutdown, makes them an ideal choice. The quiescent current is well controlled; it does not rise in dropout as it does with many other low dropout PNP regulators.

Other features of the LT1521/LT1521-3/LT1521-3.3/LT1521-5 include the ability to operate with very small output capacitors. They are stable with only 1.5μF on the output while most older devices require between 10μF and 100μF for stability. Small ceramic capacitors can be used, enhancing manufacturability. Also, the input may be connected to voltages lower than the output voltage, including negative voltages, without reverse current flow from output to input. This makes the LT1521 series ideal for backup power situations where the output is held high and the input is low or reversed. Under these conditions only 5μA will flow from the output pin to ground.

4

TYPICAL APPLICATION

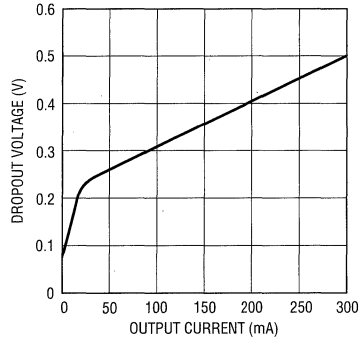
5V Battery-Powered Supply with Shutdown



V_{SHDN} (PIN 5)	OUTPUT
<0.25	OFF
>2.80	ON
NC	ON

LT1521 • TA01

Dropout Voltage



LT1521 • TA02

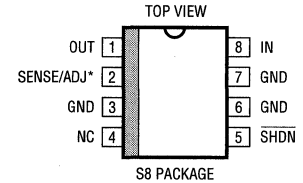
ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... ±20V*
Output Pin Reverse Current 10mA
Adjust Pin Current 10mA
Shutdown Pin Input Voltage (Note 1) ..... 6.5V, –0.6V
Shutdown Pin Input Current (Note 1) 5mA
Output Short-Circuit Duration ..... Indefinite

Storage Temperature Range ..... –65°C to 150°C
Operating Junction Temperature Range (Note 2)
Commercial ..... 0°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

*For applications requiring input voltage ratings greater than 20V, contact the factory.

PACKAGE/ORDER INFORMATION

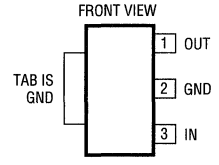


S8 PACKAGE
8-LEAD PLASTIC SO

*PIN 2 = SENSE FOR LT1521-3/LT1521-3.3/LT1521-5
= ADJ FOR LT1521

T_{JMAX} = 125°C, θ_{JA} = 70°C/W
SEE THE APPLICATIONS INFORMATION SECTION

ORDER PART NUMBER
LT1521CS8 LT1521CS8-3 LT1521CS8-3.3 LT1521CS8-5
S8 PART MARKING
1521 15213 152133 15215



ST PACKAGE
3-LEAD PLASTIC SOT-223

T_{JMAX} = 125°C, θ_{JA} = 50°C/W
SEE THE APPLICATIONS INFORMATION SECTION

ORDER PART NUMBER
LT1521CST-3 LT1521CST-3.3 LT1521CST-5
ST PART MARKING
15213 152133 15215

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Regulated Output Voltage (Note 3)	LT1521-3	V_{IN} = 3.5V, I_{OUT} = 1mA, T_J = 25°C		2.950	3.000	3.050	V
		4V < V_{IN} < 20V, 1mA < I_{OUT} < 300mA	●	2.900	3.000	3.100	V
	LT1521-3.3	V_{IN} = 3.8V, I_{OUT} = 1mA, T_J = 25°C		3.250	3.300	3.350	V
		4.3V < V_{IN} < 20V, 1mA < I_{OUT} < 300mA	●	3.200	3.300	3.400	V
	LT1521-5	V_{IN} = 5.5V, I_{OUT} = 1mA, T_J = 25°C		4.925	5.000	5.075	V
		6V < V_{IN} < 20V, 1mA < I_{OUT} < 300mA	●	4.850	5.000	5.150	V
	LT1521 (Note 4)	V_{IN} = 4.3V, I_{OUT} = 1mA, T_J = 25°C		3.695	3.750	3.805	V
		4.8V < V_{IN} < 20V, 1mA < I_{OUT} < 300mA	●	3.640	3.750	3.860	V
Line Regulation	LT1521-3	ΔV_{IN} = 4.5 to 20V, I_{OUT} = 1mA	●		1.5	20	mV
	LT1521-3.3	ΔV_{IN} = 4.8 to 20V, I_{OUT} = 1mA	●		1.5	20	mV
	LT1521-5	ΔV_{IN} = 5.5 to 20V, I_{OUT} = 1mA	●		1.5	20	mV
	LT1521 (Note 4)	ΔV_{IN} = 4.3 to 20V, I_{OUT} = 1mA	●		1.5	20	mV
Load Regulation	LT1521-3	ΔI_{LOAD} = 1mA to 300mA	●		–20	–45	mV
	LT1521-3.3	ΔI_{LOAD} = 1mA to 300mA	●		–20	–45	mV
	LT1521-5	ΔI_{LOAD} = 1mA to 300mA	●		–25	–50	mV
	LT1521 (Note 4)	ΔI_{LOAD} = 1mA to 300mA	●		–20	–45	mV

ELECTRICAL CHARACTERISTICS

ARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ropout Voltage (Note 5)	I_{LOAD} = 1mA, T_J = 25°C			130	170	mV
	I_{LOAD} = 1mA	●			250	mV
	I_{LOAD} = 50mA, T_J = 25°C			290	350	mV
	I_{LOAD} = 50mA	●			450	mV
	I_{LOAD} = 100mA, T_J = 25°C			350	420	mV
	I_{LOAD} = 100mA	●			550	mV
	I_{LOAD} = 150mA, T_J = 25°C			400	470	mV
	I_{LOAD} = 150mA	●			600	mV
	I_{LOAD} = 300mA, T_J = 25°C			500	600	mV
	I_{LOAD} = 300mA	●			750	mV
round Pin Current (Note 6)	I_{LOAD} = 0mA	●		12	20	µA
	I_{LOAD} = 1mA	●		65	100	µA
	I_{LOAD} = 10mA	●		300	450	µA
	I_{LOAD} = 50mA	●		0.8	1.5	mA
	I_{LOAD} = 100mA	●		1.4	2.5	mA
	I_{LOAD} = 150mA	●		2.2	4.0	mA
	I_{LOAD} = 300mA	●		6.5	12.0	mA
djust Pin Bias Current (Notes 4, 7)	T_J = 25°C			50	100	nA
hutdown Threshold	V_{OUT} = Off to On	●		1.20	2.80	V
	V_{OUT} = On to Off	●	0.25	0.75		V
hutdown Pin Current (Note 8)	$V_{\overline{SHDN}}$ = 0V	●		2.0	5.0	µA
uiescent Current in Shutdown (Note 9)	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V	●		6	12	µA
ipple Rejection	$V_{IN} - V_{OUT}$ = 1V(Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 150mA		50	58		dB
urrent Limit	$V_{IN} - V_{OUT}$ = 7V, T_J = 25°C			400	800	mA
	$V_{IN} = V_{OUT}$ (NOMINAL) + 1.5V, ΔV_{OUT} = −0.1V	●	320	400		mA
put Reverse Leakage Current	V_{IN} = −20V, V_{OUT} = 0V	●			1.0	mA
everse Output Current (Note 10)	LT1521-3 V_{OUT} = 3V, V_{IN} < 3V, T_J = 25°C			5	10	µA
	LT1521-3.3 V_{OUT} = 3.3V, V_{IN} < 3.3V, T_J = 25°C			5	10	µA
	LT1521-5 V_{OUT} = 5V, V_{IN} < 5V, T_J = 25°C			5	10	µA
	LT1521 (Note 4) V_{OUT} = 3.8V, V_{IN} < 3.75V, T_J = 25°C			5	10	µA

4

ıe ● denotes specifications which apply over the full operating mperature range.

ote 1: The shutdown pin input voltage rating is required for a low ıpedance source. Internal protection devices connected to the shutdown n will turn on and clamp the pin to approximately 7V or −0.6V. This nge allows the use of 5V logic devices to drive the pin directly. For high ıpedance sources or logic running on supply voltages greater than 5.5V, e maximum current driven into the shutdown pin must be limited to less an 5mA.

ote 2: For junction temperatures greater than 110°C, a minimum load of nA is recommended. For T_J > 110°C and I_{OUT} < 1mA, output voltage ay increase by 1%.

ote 3: Operating conditions are limited by maximum junction mperature. The regulated output voltage specification will not apply for possible combinations of input voltage and output current. When ıerating at maximum input voltage, the output current range must be nited. When operating at maximum output current, the input voltage nge must be limited.

Note 4: The LT1521 (adjustable version) is tested and specified with the adjust pin connected to the output pin.

Note 5: Dropout voltage is the minimum input/output voltage required to maintain regulation at the specified output current. In dropout the output voltage will be equal to: ($V_{IN} - V_{DROPOUT}$)

Note 6: Ground pin current is tested with $V_{IN} = V_{OUT}$ (nominal) and a current source load. This means the device is tested while operating in its dropout region. This is the worst-case ground pin current. The ground pin current will decrease slightly at higher input voltages.

Note 7: Adjust pin bias current flows into the adjust pin.

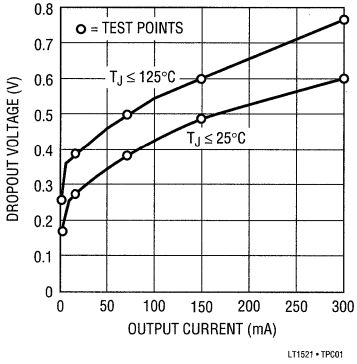
Note 8: Shutdown pin current at $V_{\overline{SHDN}}$ = 0V flows out of the shutdown pin.

Note 9: Quiescent current in shutdown is equal to the total sum of the shutdown pin current (2µA) and the ground pin current (4µA).

Note 10: Reverse output current is tested with the input pin grounded and the output pin forced to the rated output voltage. This current flows into the output pin and out of the ground pin.

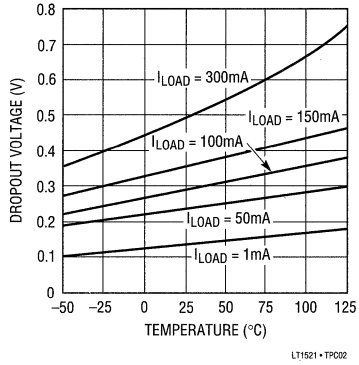
TYPICAL PERFORMANCE CHARACTERISTICS

Guaranteed Dropout Voltage



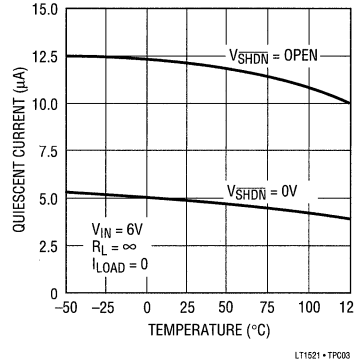
LT1521 • TPC01

Dropout Voltage



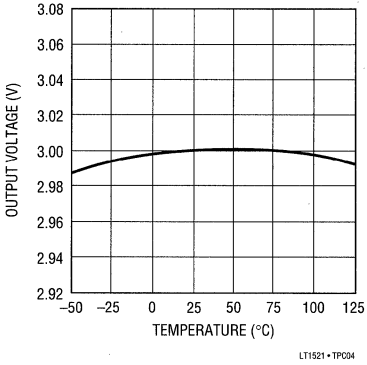
LT1521 • TPC02

Quiescent Current



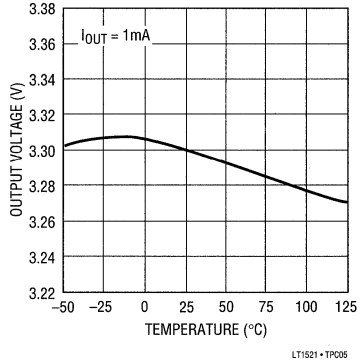
LT1521 • TPC03

LT1521-3
Output Voltage



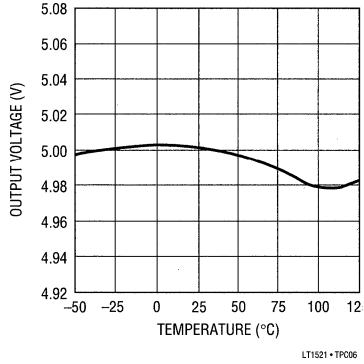
LT1521 • TPC04

LT1521-3.3
Output Voltage



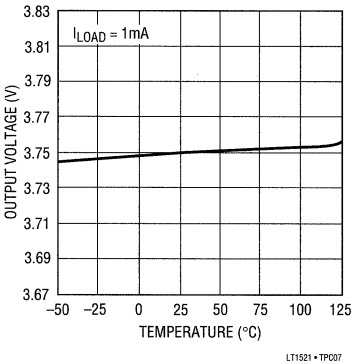
LT1521 • TPC05

LT1521-5
Output Voltage



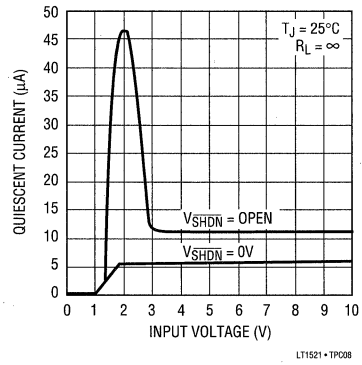
LT1521 • TPC06

LT1521
Adjust Pin Voltage



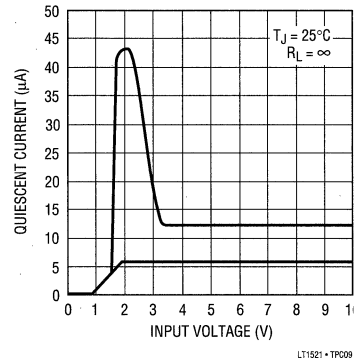
LT1521 • TPC07

LT1521-3
Quiescent Current



LT1521 • TPC08

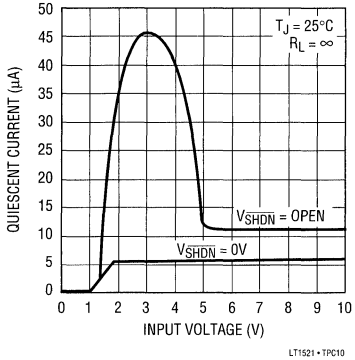
LT1521-3.3
Quiescent Current



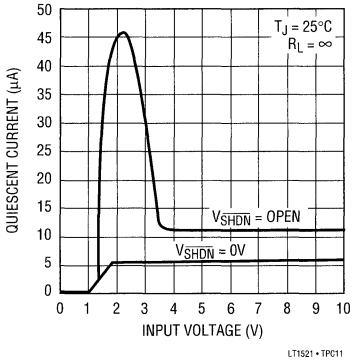
LT1521 • TPC09

TYPICAL PERFORMANCE CHARACTERISTICS

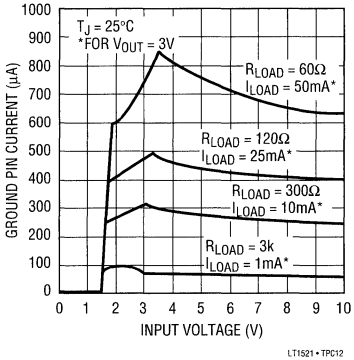
LT1521-5
Quiescent Current



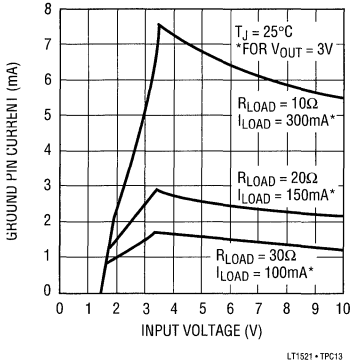
LT1521
Quiescent Current



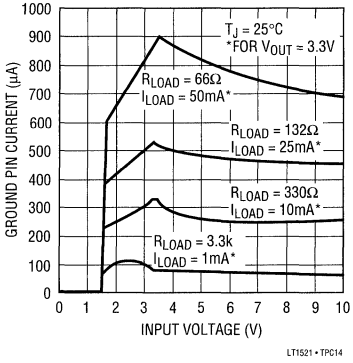
LT1521-3
Ground Pin Current



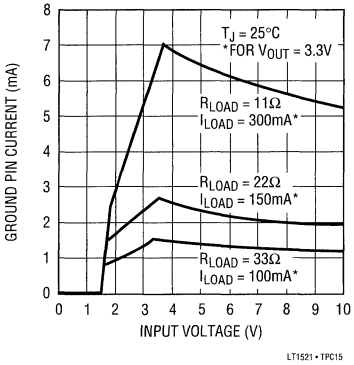
LT1521-3
Ground Pin Current



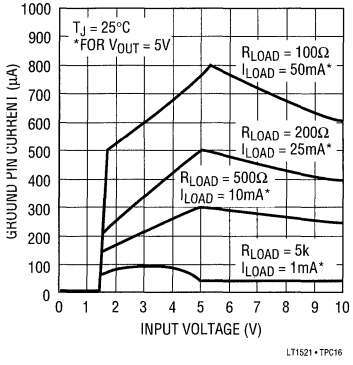
LT1521-3.3
Ground Pin Current



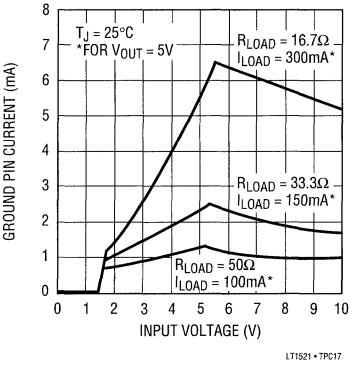
LT1521-3.3
Ground Pin Current



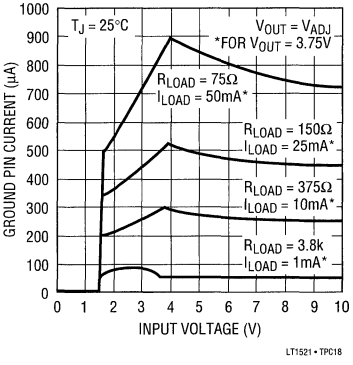
LT1521-5
Ground Pin Current



LT1521-5
Ground Pin Voltage



LT1521
Ground Pin Current



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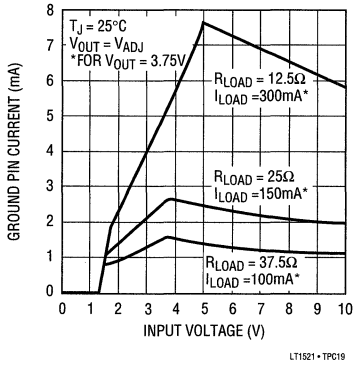
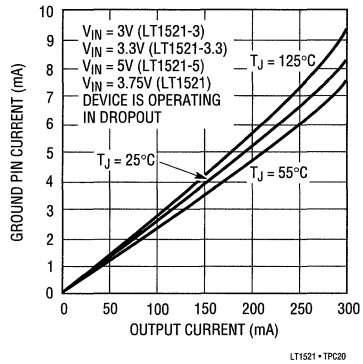
TYPICAL PERFORMANCE CHARACTERISTICS

LT1521
Ground Pin Current



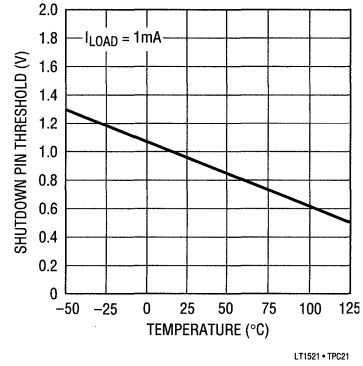
LT1521 • TPC19

Ground Pin Current



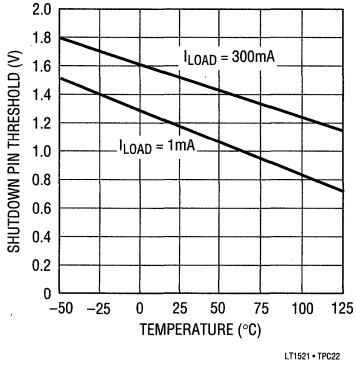
LT1521 • TPC20

Shutdown Pin Threshold (On-to-Off)



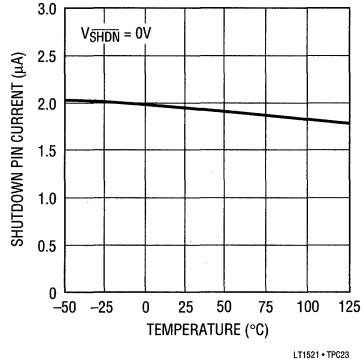
LT1521 • TPC21

Shutdown Pin Threshold (Off-to-On)



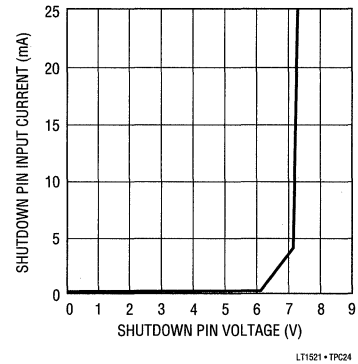
LT1521 • TPC22

Shutdown Pin Current



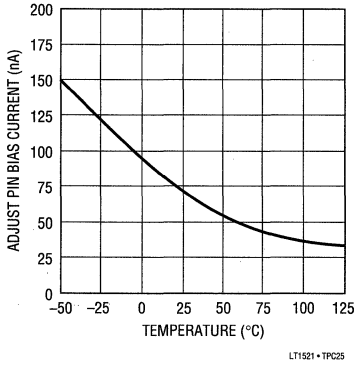
LT1521 • TPC23

Shutdown Pin Input Current



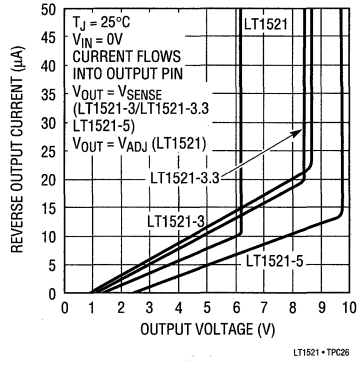
LT1521 • TPC24

Adjust Pin Bias Current



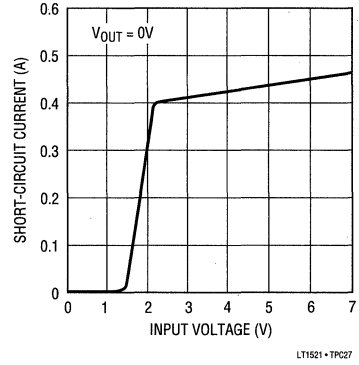
LT1521 • TPC25

Reverse Output Voltage



LT1521 • TPC26

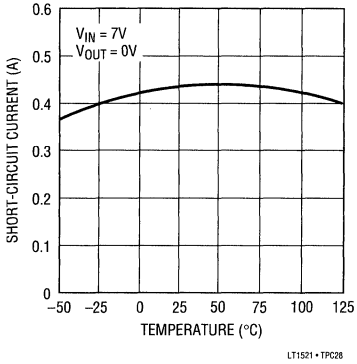
Current Limit



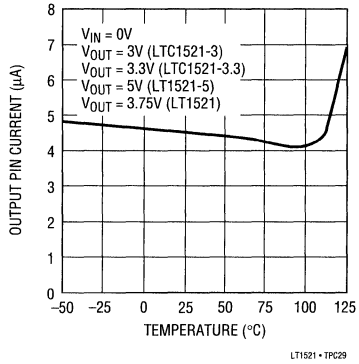
LT1521 • TPC27

TYPICAL PERFORMANCE CHARACTERISTICS

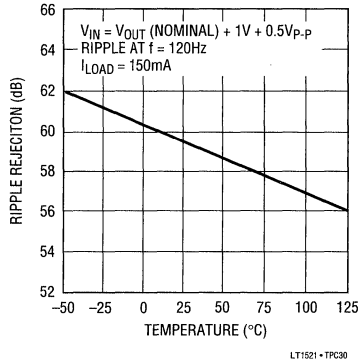
Current Limit



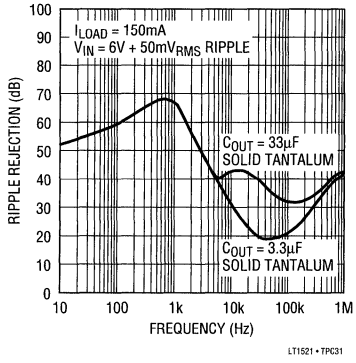
Reverse Output Current



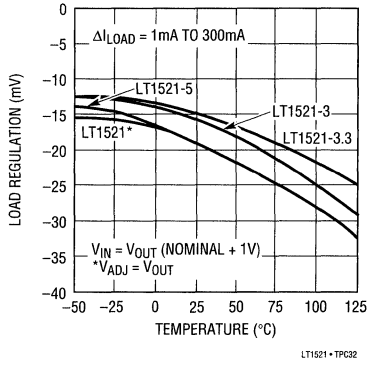
Ripple Rejection



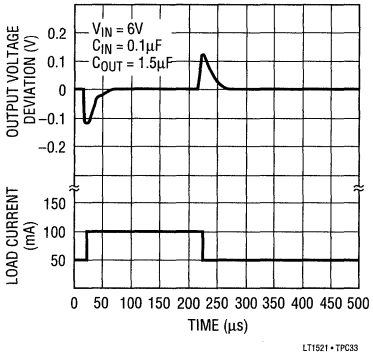
Ripple Rejection



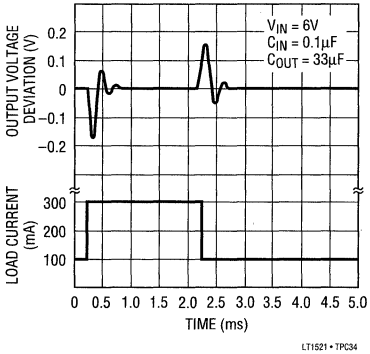
Load Regulation



LT1521-5
Transient Response



LT1521-5
Transient Response



4

PIN FUNCTIONS

OUT (Pin 1): The output pin supplies power to the load. A minimum output capacitor of 1.5µF is required to prevent oscillations, but larger values of output capacitor will be necessary to deal with larger load transients. See the Applications Information section for more on output capacitance and reverse output characteristics.

SENSE (Pin 2): For fixed voltage versions of the LT1521 (LT1521-3, LT1521-3.3, LT1521-5), the sense pin is the input to the error amplifier. Optimum regulation will be obtained at the point where the sense pin is connected to the output pin of the regulator. In critical applications small voltage drops caused by the resistance (R_P) of PC traces between the regulator and the load, which would normally degrade regulation, may be eliminated by connecting the sense pin to the output at the load as shown in Figure 1 (Kelvin Sense Connection). Note that the voltage drop across the external PC traces will add to the dropout voltage of the regulator. The sense pin bias current is 5µA at the nominal regulated output voltage. This pin is internally clamped to –0.6V (one V_{BE}).

ADJ (Pin 2): For adjustable LT1521, the adjust pin is the input to the error amplifier. This pin is internally clamped to 6V and –0.6V (one V_{BE}). It has a bias current of 50nA which flows into the pin. See Adjust Pin Bias Current vs Temperature in the Typical Performance Characteristics section. The adjust pin reference voltage is 3.75V referenced to ground. The output voltage range that can be produced by this device is 3.75V to 20V.

$\overline{\text{SHDN}}$ (Pin 5): The shutdown pin is used to put the device into shutdown. In shutdown the output of the device is turned off. This pin is active low. The device will be shut down if the shutdown pin is pulled low. The shutdown pin current with the pin pulled to ground will be 1.7µA. The shutdown pin is internally clamped to 7V and –0.6V (one V_{BE}). This allows the shutdown pin to be driven directly by 5V logic or by open collector logic with a pull-up resistor. The pull-up resistor is only required to supply the leakage current of the open collector gate, normally several microamperes. Pull-up current must be limited to a maximum of 5mA. A curve of the shutdown pin input current as a function of voltage appears in the Typical Performance Characteristics. If the shutdown pin is not used it can be left open circuit. The device will be active (output on) if the shutdown pin is not connected.

IN (Pin 8): Power is supplied to the device through the input pin. The input pin should be bypassed to ground if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF is sufficient. The LT1521 is designed to withstand reverse voltages on the input pin with respect to ground and the output pin. In the case of reversed input, which can happen if a battery is plugged in backwards, the LT1521 will act as if there is a diode in series with its input. There will be no reverse current flow into the LT1521 and no reverse voltage will appear at the load. The device will protect both itself and the load.

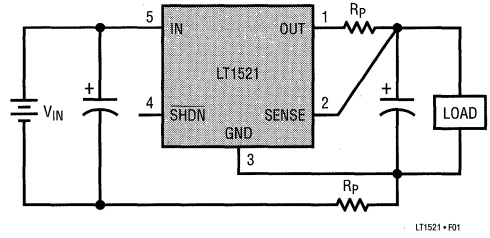


Figure 1. Kelvin Sense Connection

APPLICATIONS INFORMATION

The LT1521 is a 300mA low dropout regulator with micropower quiescent current and shutdown. The device is capable of supplying 300mA at a dropout of 0.5V and operates with very low quiescent current (12µA). In shutdown, the quiescent current drops to only 6µA. In addition to the low quiescent current, the LT1521 incorporates several protection features which make it ideal for use in battery-powered systems. The device is protected against both reverse input voltages and reverse output voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to

APPLICATIONS INFORMATION

ground, the LT1521 acts like it has a diode in series with its output and prevents reverse current flow.

Adjustable Operation

The adjustable version of the LT1521 has an output voltage range of 3.75V to 20V. The output voltage is set by the ratio of two external resistors as shown in Figure 2. The device servos the output voltage to maintain the voltage at the adjust pin at 3.75V. The current in R1 is then equal to 3.75V/R1. The current in R2 is equal to the sum of the current in R1 and the adjust pin bias current. The adjust pin bias current, 50nA at 25°C, flows through R2 into the adjust pin. The output voltage can be calculated using the formula in Figure 2. The value of R1 should be less than 100k to minimize errors in the output voltage caused by the adjust pin bias current. Note that in shutdown the output is turned off and the divider current will be zero. Curves of Adjust Pin Voltage vs Temperature and Adjust Pin Bias Current vs Temperature appear in the Typical Performance Characteristics. The reference voltage at the adjust pin has a positive temperature coefficient of approximately 15ppm/°C. The adjust pin bias current has a negative temperature coefficient. These effects will tend to cancel each other.

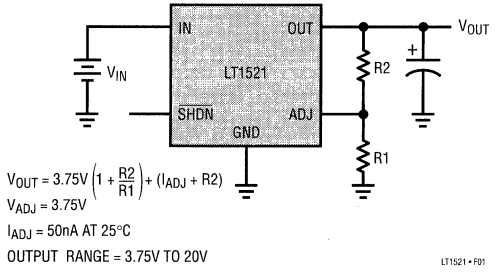


Figure 2. Adjustable Operation

The adjustable device is specified with the adjust pin tied to the output pin. This sets the output voltage to 3.75V. Specifications for output voltages greater than 3.75V will be proportional to the ratio of the desired output voltage to 3.75V; (V_{OUT}/3.75V). For example: load regulation for an output current change of 1mA to 300mA is –20mV typical at V_{OUT} = 3.75V. At V_{OUT} = 12V, load regulation would be:

(12V/3.75V) × (–20mV) = –64mV

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C). The power dissipated by the device will be made up of two components:

1. Output current multiplied by the input/output voltage differential: $I_{OUT} \times (V_{IN} - V_{OUT})$, and
2. Ground pin current multiplied by the input voltage: $I_{GND} \times V_{IN}$

The ground pin current can be found by examining the Ground Pin Current curves in the Typical Performance Characteristics. Power dissipation will be equal to the sum of the two components listed above.

The LT1521 series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal load conditions the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

The following tables list thermal resistance for each package. Measured values of thermal resistance for several different board sizes and copper areas are listed for each package. All measurements were taken in still air on 3/32" FR-4 board with one ounce copper. All NC leads were connected to the ground plane.

Table 1. S8 Package*

COPPER AREA			THERMAL RESISTANCE
TOPSIDE**	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	2500 sq mm	60°C/W
1000 sq mm	2500 sq mm	2500 sq mm	60°C/W
225 sq mm	2500 sq mm	2500 sq mm	68°C/W
100 sq mm	2500 sq mm	2500 sq mm	74°C/W

* Pins 3, 6, 7 are ground. ** Device is mounted on topside.

APPLICATIONS INFORMATION

Table 2. SOT-223 Package (Thermal Resistance Junction-to-Tab 20°C/W)

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	2500 sq mm	50°C/W
1000 sq mm	2500 sq mm	2500 sq mm	50°C/W
225 sq mm	2500 sq mm	2500 sq mm	58°C/W
100 sq mm	2500 sq mm	2500 sq mm	64°C/W
1000 sq mm	1000 sq mm	1000 sq mm	57°C/W
1000 sq mm	0	1000 sq mm	60°C/W

* Tab of device attached to topside copper.

Calculating Junction Temperature

Example: Given an output voltage of 3.3V, an input voltage range of 4.5V to 7V, an output current range of 0mA to 150mA and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be equal to:

$$I_{OUT(MAX)} \times (V_{IN(MAX)} - V_{OUT}) + (I_{GND} \times V_{IN(MAX)})$$

Where,

$I_{OUT(MAX)} = 150mA$

$V_{IN(MAX)} = 7V$

I_{GND} at ($I_{OUT} = 150mA$, $V_{IN} = 7V$) = 2.1mA

So,

$$P = 150mA \times (7V - 3.3V) + (2.1mA \times 7V) = 0.57W$$

If we use a SOT-223 package, then the thermal resistance will be in the range of 50°C/W to 65°C/W depending on the copper area. So the junction temperature rise above ambient will be approximately equal to:

$$0.57W \times 60°C/W = 34.2°C$$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_{JMAX} = 50°C + 34.2°C = 84.2°C$$

Output Capacitance and Transient Performance

The LT1521 is designed to be stable with a wide range of output capacitors. A minimum output capacitor of 1.5µF is required to prevent oscillations. The LT1521 is a micropower device and output transient response will be a function of output capacitance. See the Transient Response curves in the Typical Performance Characteristics. Larger values of output capacitance will decrease the peak deviations and provide improved output transient response for larger load current deltas. Bypass capacitors, used to decouple individual components powered by the LT1521, will increase the effective value of the output capacitor.

Protection Features

The LT1521 incorporates several protection features which make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse input voltages, reverse output voltages and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperatures should not exceed 125°C.

The input of the device will withstand reverse voltages of 20V. Current flow into the device will be limited to less than 1mA (typically less than 100µA) and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries that can be plugged in backward.

For fixed voltage versions of the device, the output can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20V. The output will act like an open circuit, no current will flow out of the pin. If the input is powered by voltage source, the output will source the short-circuit current of the device and will protect itself by thermal limiting. For the adjustable version of the device, the output pin is internally clamped at one diode drop below ground. Reverse current for the adjustable device must be limited to 5mA.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open circuit. Current flow back into the output will vary depending on the conditions. Many battery-powered circuits

APPLICATIONS INFORMATION

ncorporate some form of power management. The following information will help optimize battery life. Table 3 summarizes the following information.

The reverse output current will follow the curve in Figure 3 when the input is pulled to ground. This current flows through the output pin to ground. The state of the shutdown pin will have no effect on output current when the nput pin is pulled to ground.

n some applications it may be necessary to leave the input on the LT1521 unconnected when the output is held high. This can happen when the LT1521 is powered from a ectified AC source. If the AC source is removed, then the nput of the LT1521 is effectively left floating. The reverse output current also follows the curve in Figure 3 if the input pin is left open. The state of the shutdown pin will have no effect on the reverse output current when the input pin is floating.

When the input of the LT1521 is forced to a voltage below its nominal output voltage and its output is held high, the output current will follow the curve shown in Figure 3. This can happen if the input of the LT1521 is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or by second regulator circuit. When the input pin is forced below the output pin or the output pin is pulled above the input pin, the input current will typically drop to less than 2µA (see Figure 4). The state of the shutdown pin will have no effect on the reverse output current when the output is pulled above the input.

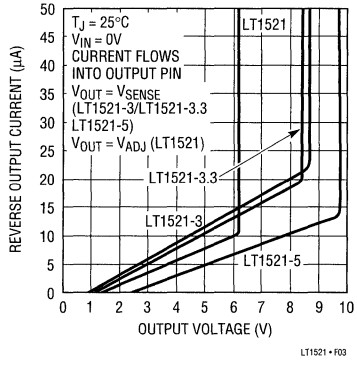


Figure 3. Reverse Output Current

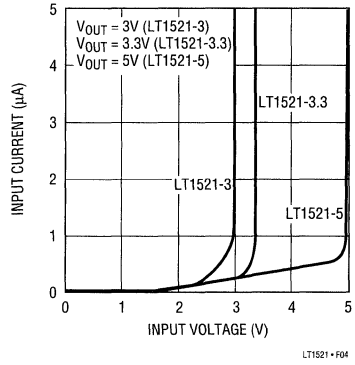


Figure 4. Input Current

Table 3. Fault Conditions

INPUT PIN	$\overline{SHDN}$ PIN	OUTPUT/SENSE PINS	RESULTING CONDITIONS
< V_{OUT} (Nominal)	Open (High)	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 5µA (See Figure 3) Input Current ≈ 1µA (See Figure 4)
< V_{OUT} (Nominal)	Grounded	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 5µA (See Figure 3) Input Current ≈ 1µA (See Figure 4)
Open	Open (High)	> 1V	Reverse Output Current ≈ 5µA (See Figure 3)
Open	Grounded	> 1V	Reverse Output Current ≈ 5µA (See Figure 3)
≤ 0.8V	Open (High)	≤ 0V	Output Current = 0
≤ 0.8V	Grounded	≤ 0V	Output Current = 0
> 1.5V	Open (High)	≤ 0V	Output Current = Short-Circuit Current
−20V < V_{IN} < 20V	Grounded	≤ 0V	Output Current = 0

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1174	425mA High Efficiency Step-Down Switching Regulator	>90% Efficiency, SO-8 Package
LT1175	500mA Micropower Low Dropout Negative Linear Regulator	Selectable Current Limit
LT1120A	125mA Micropower Low Dropout Linear Regulator	20μA Quiescent Current, Includes Comparator
LT1304	Micropower Step-Up DC/DC Converter	15μA Quiescent Current, 1.5 Minimum Input
LT1529	3A Micropower Low Dropout Regulator	50μA Quiescent Current

3A Low Dropout Regulator for Microprocessor Applications

FEATURES

- **Dropout Voltage: 0.6V at I_{OUT} = 3A**
- **Fast Transient Response**
- **Output Current: 3A**
- Quiescent Current: 400μA
- No Protection Diodes Needed
- Fixed Output Voltage: 3.3V
- Controlled Quiescent Current in Dropout
- Shutdown I_Q = 125μA
- Stable with 3.3μF Output Capacitor
- Reverse Battery Protection
- No Reverse Output Current
- Thermal Limiting

APPLICATIONS

- Microprocessor Applications
- Post Regulator for Switching Supplies
- 5V to 3.3V Logic Regulator

DESCRIPTION

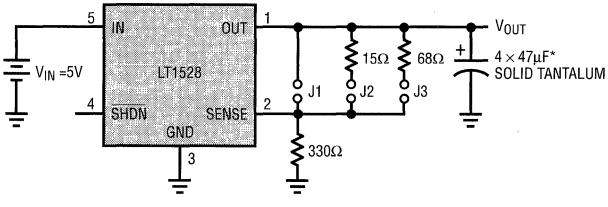
The LT®1528 is a 3A low dropout regulator optimized to handle the large load current transients associated with the current generation of microprocessors. This device has the fastest transient response of currently available PNP regulators and is very tolerant of variations in capacitor ESR. Dropout voltage is 75mV at 10mA, rising to 300mV at 1A and 600mV at 3A. The device has a quiescent current of 400μA. Quiescent current is well controlled; it does not increase significantly as the device enters dropout. The regulator can operate with output capacitors as small as 3.3μF, although larger capacitors will be needed to achieve the performance required in most microprocessor applications. The LT1528 is available with a fixed output voltage of 3.3V. An external Sense pin allows adjustment to output voltages greater than 3.3V, using a simple resistive divider. This allows the device to be adjusted over a wide range of output voltages, including the 3.3V to 4.2V range required by a variety of processors from Intel, IBM, AMD, and Cyrix.

The LT1528 has both reverse input and reverse output protection and includes a shutdown feature. Quiescent current drops to 125μA in shutdown. The LT1528 is available in 5-lead TO-220 and 5-lead DD packages.

4

TYPICAL APPLICATION

Microprocessor Supply with Shutdown



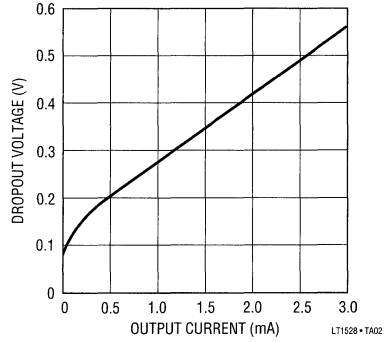
V_{SHDN} (PIN 4)	OUTPUT
<0.25	OFF
>2.80	ON
NC	ON

SHORTING	V_{OUT}
J1	3.30
J2	3.45
J3	4.00

*CHOOSE CAPACITORS TO MEET PROCESSOR REQUIREMENTS

LT1528 • TA01

Dropout Voltage



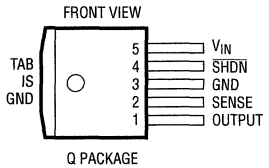
LT1528 • TA02

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... ±15V*
Output Pin Reverse Current 10mA
Sense Pin Current 10mA
Shutdown Pin Input Voltage (Note 1) ..... 6.5V, –0.6V
Shutdown Pin Input Current (Note 1) 5mA
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to 150°C
Operating Junction Temperature Range
LT1528C ..... 0°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

*For applications requiring input voltage ratings greater than 15V, contact the factory.

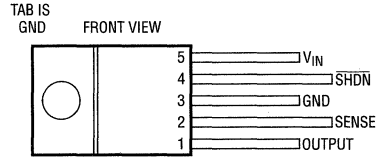
PACKAGE/ORDER INFORMATION



Q PACKAGE
5-LEAD PLASTIC DD PAK

T_{JMAX} = 125°C, θ_{JA} = 30°C/W

ORDER PART NUMBER
LT1528CQ



T PACKAGE
5-LEAD PLASTIC TO-220

T_{JMAX} = 125°C, θ_{JA} = 50°C/W

ORDER PART NUMBER
LT1528CT

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Regulated Output Voltages (Notes 2, 3)	V_{IN} = 3.8V, I_{OUT} = 1mA, T_J = 25°C		3.250	3.300	3.350	V
	4.3V < V_{IN} < 15V, 1mA < I_{OUT} < 3A	●	3.200	3.300	3.400	V
Line Regulation (Note 3)	ΔV_{IN} = 3.8V to 15V, I_{OUT} = 1mA	●		1.5	10	mV
Load Regulation (Note 3)	ΔI_{LOAD} = 1mA to 3A, V_{IN} = 4.3V, T_J = 25°C			12	20	mV
	ΔI_{LOAD} = 1mA to 3A, V_{IN} = 4.3V	●		15	30	mV
Dropout Voltage (Note 4)	I_{LOAD} = 10mA, T_J = 25°C			70	110	mV
	I_{LOAD} = 10mA	●			150	mV
	I_{LOAD} = 100mA, T_J = 25°C			150	200	mV
	I_{LOAD} = 100mA	●			250	mV
	I_{LOAD} = 700mA, T_J = 25°C			280	320	mV
	I_{LOAD} = 700mA	●			420	mV
	I_{LOAD} = 1.5A, T_J = 25°C			390	450	mV
	I_{LOAD} = 1.5A	●			600	mV
	I_{LOAD} = 3A, T_J = 25°C			570	670	mV
	I_{LOAD} = 3A	●			850	mV

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Ground Pin Current (Note 5)	I_{LOAD} = 0mA, T_J = 25°C			450	750	µA
	I_{LOAD} = 0mA, T_J = 125°C (Note 6)			1.9		mA
	I_{LOAD} = 100mA, T_J = 25°C			1.2	2.5	mA
	I_{LOAD} = 100mA, T_J = 125°C (Note 6)			2.7		mA
	I_{LOAD} = 300mA, T_J = 25°C			2.6	4.0	mA
	I_{LOAD} = 300mA, T_J = 125°C (Note 6)			4.1		mA
	I_{LOAD} = 700mA, T_J = 25°C			7.3	12.0	mA
	I_{LOAD} = 700mA, T_J = 125°C (Note 6)			8.8		mA
	I_{LOAD} = 1.5A	●		22	40	mA
	I_{LOAD} = 3A	●		85	140	mA
Sense Pin Current (Notes 3, 7)	T_J = 25°C		90	130	250	µA
Shutdown Threshold	V_{OUT} = Off-to-On	●		1.20	2.80	V
	V_{OUT} = On-to-Off	●	0.25	0.75		V
Shutdown Pin Current (Note 8)	$V_{\overline{SHDN}}$ = 0V	●		37	100	µA
Quiescent Current in Shutdown (Note 9)	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V	●		110	220	µA
Ripple Rejection	$V_{IN} - V_{OUT}$ = 1V(Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 1.5A		50	67		dB
Current Limit	$V_{IN} - V_{OUT}$ = 7V, T_J = 25°C			4.5		A
	V_{IN} = 4.3V, ΔV_{OUT} = –0.1V	●	3.2	4.0		A
Input Reverse Leakage Current	V_{IN} = –15V, V_{OUT} = 0V	●			1.0	mA
Reverse Output Current (Note 10)	V_{OUT} = 3.3V, V_{IN} = 0V			120	250	µA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The Shutdown pin input voltage rating is required for a low impedance source. Internal protection devices connected to the Shutdown pin will turn on and clamp the pin to approximately 7V or –0.6V. This range allows the use of 5V logic devices to drive the pin directly. For high impedance sources or logic running on supply voltages greater than 5.5V, the maximum current driven into the Shutdown pin must be less than 5mA.

Note 2: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current must be limited. When operating at maximum output current, the input voltage range must be limited.

Note 3: The LT1528 is tested and specified with the Sense pin connected to the Output pin.

Note 4: Dropout voltage is the minimum input/output voltage required to maintain regulation at the specified output current. In dropout the output voltage will be equal to: ($V_{IN} - V_{DROPOUT}$).

Note 5: Ground pin current is tested with $V_{IN} = V_{OUT}$ (nominal) and a current source load. This means that the device is tested while operating in its dropout region. This is the worst-case Ground pin current. The Ground pin current will decrease slightly at higher input voltages.

Note 6: Ground pin current will rise at $T_J > 75°C$. This is due to internal circuitry designed to compensate for leakage currents in the output transistor at high temperatures. This allows quiescent current to be minimized at lower temperatures, yet maintain output regulation at high temperatures with light loads. See quiescent current curve in typical performance characteristics section.

Note 7: Sense pin current flows into the Sense pin.

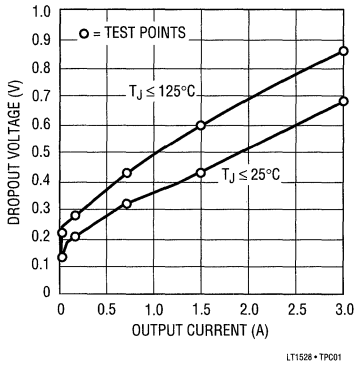
Note 8: Shutdown pin current at $V_{\overline{SHDN}}$ = 0V flows out of the Shutdown pin.

Note 9: Quiescent current in shutdown is equal to the total sum of the Shutdown pin current (40µA) and the Ground pin current (70µA).

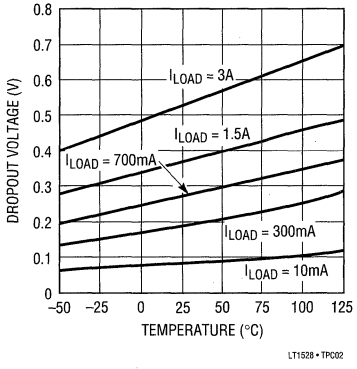
Note 10: Reverse output current is tested with the input pin grounded and the Output pin forced to the rated output voltage. This current flows into the Output pin and out of the Ground pin.

TYPICAL PERFORMANCE CHARACTERISTICS

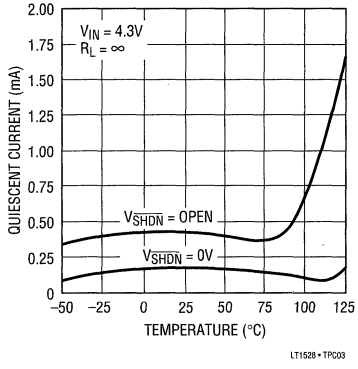
Guaranteed Dropout Voltage



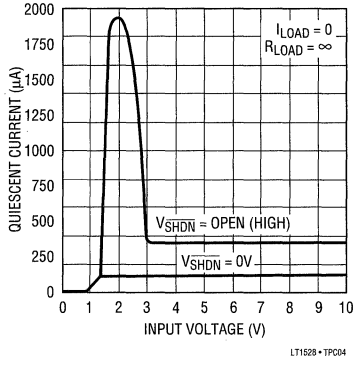
Dropout Voltage



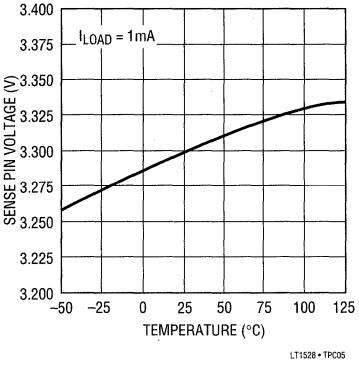
Quiescent Current



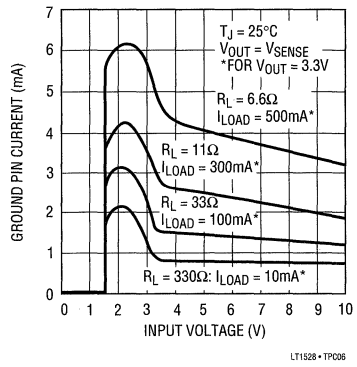
Quiescent Current



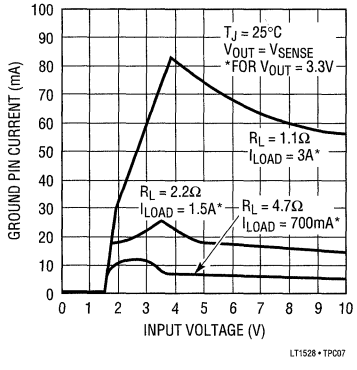
Sense Pin Voltage



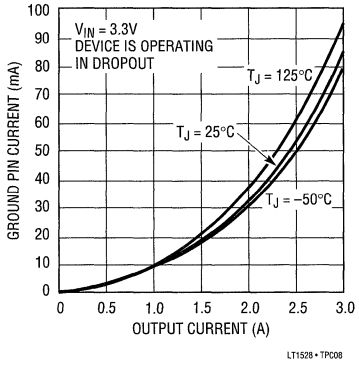
Ground Pin Current



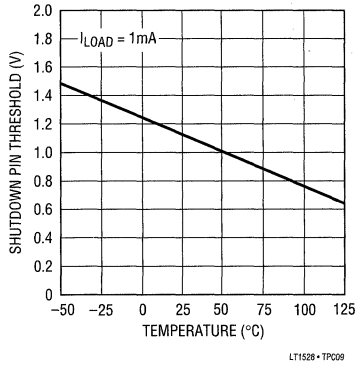
Ground Pin Current



Ground Pin Current

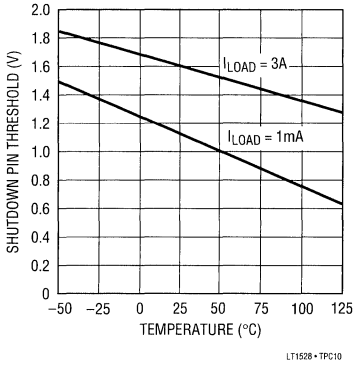


Shutdown Pin Threshold (On-to-Off)



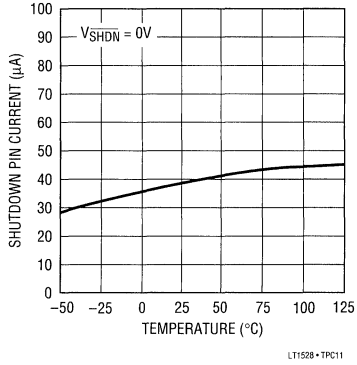
TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown Pin Threshold (Off-to-On)



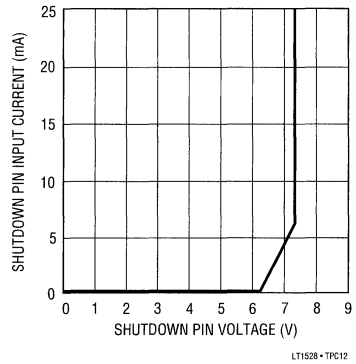
LT1528 • TPC10

Shutdown Pin Current



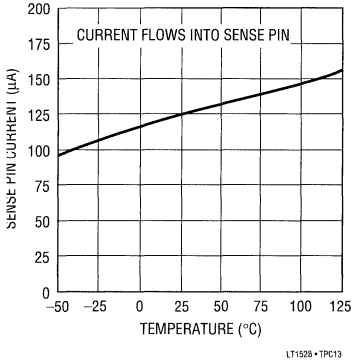
LT1528 • TPC11

Shutdown Pin Input Current



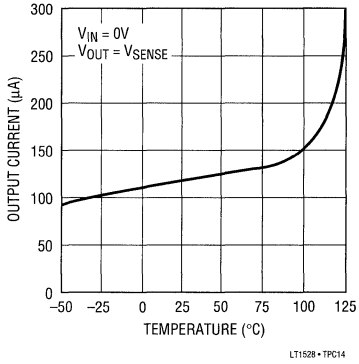
LT1528 • TPC12

Sense Pin Current



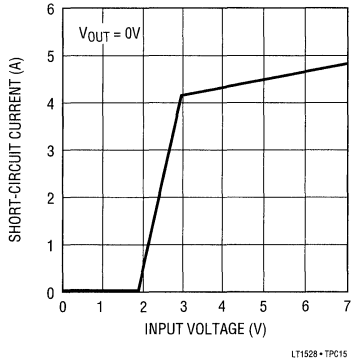
LT1528 • TPC13

Reverse Output Current



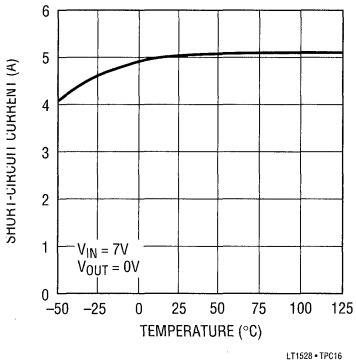
LT1528 • TPC14

Current Limit



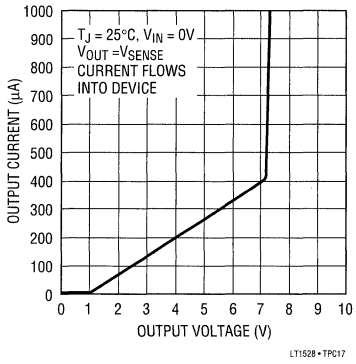
LT1528 • TPC15

Current Limit



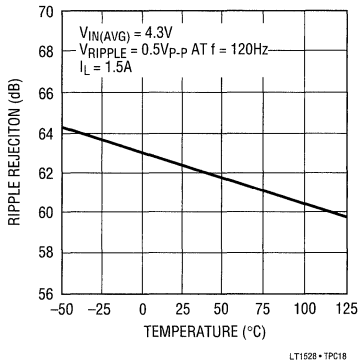
LT1528 • TPC16

Reverse Output Current



LT1528 • TPC17

Ripple Rejection

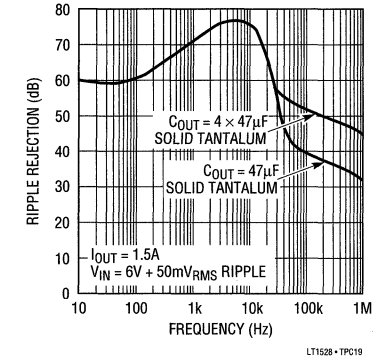


LT1528 • TPC18

4

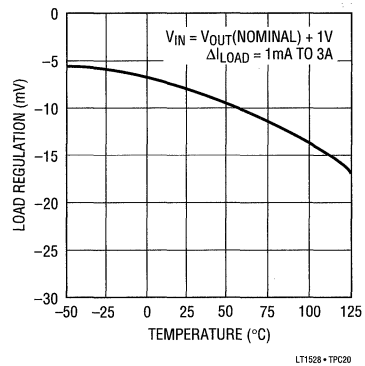
TYPICAL PERFORMANCE CHARACTERISTICS

Ripple Rejection



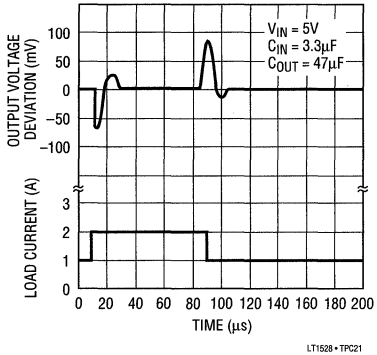
LT1528 • TPC19

Load Regulation



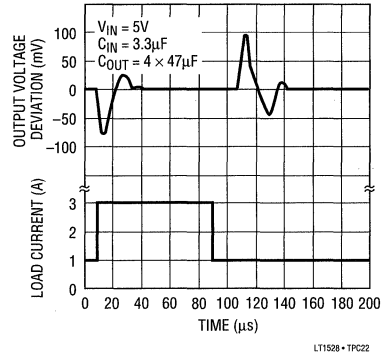
LT1528 • TPC20

Transient Response



LT1528 • TPC21

Transient Response



LT1528 • TPC22

PIN FUNCTIONS

OUTPUT (Pin 1): The Output pin supplies power to the load. A minimum output capacitor of 3.3µF is required to prevent oscillations. Larger values will be needed to achieve the transient performance required by high speed microprocessors. See the Applications Information section for more on output capacitance and reverse output characteristics.

SENSE (Pin 2): The Sense pin is the input to the error amplifier. Optimum regulation will be obtained at the point where the Sense pin is connected to the Output pin. For most applications the Sense pin is connected directly to the Output pin at the regulator. In critical applications small voltage drops caused by the resistance (R_P) of PC traces between the regulator and the load, which would normally degrade regulation, may be eliminated by connecting the Sense pin to the Output pin at the load as shown in Figure 1 (Kelvin Sense Connection). Note that the voltage drop across the external PC traces will add to the dropout voltage of the regulator. The Sense pin bias current is 150µA at the nominal regulated output voltage. See Sense Pin Current vs Temperature in the Typical Performance Characteristics section. This pin is internally clamped to –0.6V (one V_{BE}).

The Sense pin can also be used with a resistor divider to achieve output voltages above 3.3V. See the Applications Information section for information on adjustable operation.

PIN FUNCTIONS

$\overline{SHDN}$ (Pin 4): This pin is used to put the device into shutdown. In shutdown the output of the device is turned off. This pin is active low. The device will be shut down if the Shutdown pin is actively pulled low. The Shutdown pin current with the pin pulled to ground will be 60µA. The Shutdown pin is internally clamped to 7V and –0.6V (one V_{BE}). This allows the Shutdown pin to be driven directly by 5V logic or by open collector logic with a pull-up resistor. The pull-up resistor is only required to supply the leakage current of the open collector gate, normally several microamperes. Pull-up current must be limited to a maximum of 5mA. A curve of Shutdown pin input current as a function of voltage appears in the Typical Performance Characteristics section. If the Shutdown pin is not used it can be left open circuit. The device will be active output on if the Shutdown pin is not connected.

V_{IN} (Pin 5): Power is supplied to the device through the input pin. The input pin should be bypassed to ground if the device is more than six inches away from the main input filter capacitor. The LT1528 is designed to withstand reverse voltages on the input pin with respect to ground and the Output pin. In the case of reversed input, the LT1528 will act as if there is a diode in series with its input. There will be no reverse current flow into the LT1528 and no reverse voltage will appear at the load. The device will protect both itself and the load.

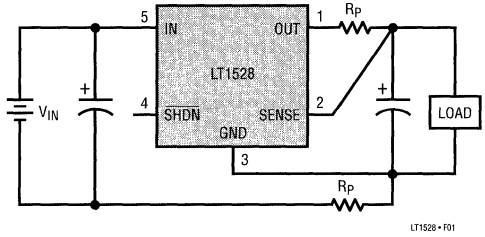


Figure 1. Kelvin Sense Connection

APPLICATIONS INFORMATION

The LT1528 is a 3A low dropout regulator optimized for microprocessor applications. Dropout voltage is only 0.6V at 3A output current. With the Sense pin shorted to the Output pin, the output voltage is set to 3.3V. The device operates with a quiescent current of 400µA. In shutdown, the quiescent current drops to only 125µA. The LT1528 incorporates several protection features, including protection against reverse input voltages. If the output is held at the rated output voltage when the input is pulled to ground, the LT1528 acts like it has a diode in series with its output and prevents reverse current flow.

Adjustable Operation

The LT1528 can be used as an adjustable regulator with an output voltage range of 3.3V to 14V. The output voltage is set by the ratio of two external resistors as shown in Figure 2. The device servos the output voltage to maintain the voltage at the Sense pin at 3.3V. The current in R1 is then equal to 3.3V/R1. The current in R2 is equal to the sum of the current in R1 and the Sense pin current. The Sense pin current, 130µA at 25°C, flows through R2 into the Sense pin. The output voltage can be calculated using the formula in Figure 2. The value of R1 should be less than 330Ω to minimize errors in the output voltage caused by the Sense pin current. Note that in shutdown the output is turned off and the divider current will be zero. Curves of Sense Pin Voltage vs Temperature and Sense Pin Current vs Temperature appear in the Typical Performance Characteristics section.

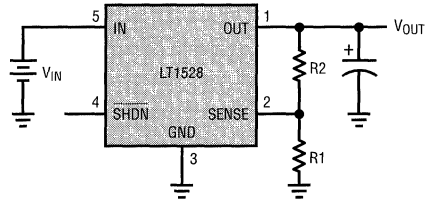


Figure 2. Adjustable Operation

APPLICATIONS INFORMATION

The LT1528 is specified with the Sense pin tied to the Output pin. This sets the output voltage to 3.3V. Specifications for output voltage greater than 3.3V will be proportional to the ratio of the desired output voltage to 3.3V (V_{OUT}/3.3V). For example, load regulation for an output current change of 1mA to 1.5A is –5mV (typical) at V_{OUT} = 3.3V. At V_{OUT} = 12V, load regulation would be:

$(12V/3.3V) \times (-5mV) = (-18mV)$

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C). The power dissipated by the device will be made up of two components:

1. Output current multiplied by the input/output voltage differential, $I_{OUT} \times (V_{IN} - V_{OUT})$, and
2. Ground pin current multiplied by the input voltage, $I_{GND} \times V_{IN}$.

The Ground pin current can be found by examining the Ground Pin Current curves in the Typical Performance Characteristics. Power dissipation will be equal to the sum of the two components listed above.

The LT1528 has internal thermal limiting designed to protect the device during overload conditions. For continuous normal load conditions the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction-to-ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Experiments have shown that the heat spreading copper layer does not have to be electrically connected to the tab of the device. The PC material can be very effective at transmitting heat between the pad area, attached to the tab of the device, and a ground or power plane either inside or on the opposite side of the board. Although the actual thermal resistance of the PC material is high, the length/area ratio of the thermal resistor between layers is small. Copper board stiffeners and plated through holes can also be used to spread the heat generated by power devices.

Table 1a lists thermal resistance for the DD package. For the TO-220 package (Table 1b) thermal resistance is given for junction-to-case only since this package is usually mounted to a heat sink. Measured values of thermal resistance for several different copper areas are listed for the DD package. All measurements were taken in still air on 3/32" FR-4 board with one ounce copper. This data can be used as a rough guideline in estimating thermal resistance. The thermal resistance for each application will be affected by thermal interactions with other components as well as board size and shape. Some experimentation will be necessary to determine the actual value.

Table 1a. Q-Package, 5-Lead DD

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	2500 sq mm	23°C/W
1000 sq mm	2500 sq mm	2500 sq mm	25°C/W
125 sq mm	2500 sq mm	2500 sq mm	33°C/W

*Device is mounted on topside.

Table 1b. T Package, 5-Lead TO-220

Thermal Resistance (Junction-to-Case)	2.5°C/W

Calculating Junction Temperature

Example: Given an output voltage of 3.3V, an input voltage range of 4.5V to 5.5V, an output current range of 0mA to 500mA and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be equal to:

$I_{OUT(MAX)} \times (V_{IN(MAX)} - V_{OUT}) + [I_{GND} \times V_{IN(MAX)}]$

where,

$I_{OUT(MAX)}$ = 500mA
$V_{IN(MAX)}$ = 5.5V
I_{GND} at (I_{OUT} = 500mA, V_{IN} = 5.5V) = 4mA

so,

$P = 500mA \times (5.5V - 3.3V) + (4mA \times 5.5V) = 1.12W$

If we use a DD package, the thermal resistance will be in the range of 23°C/W to 33°C/W depending on the copper area. So the junction temperature rise above ambient will be approximately equal to:

$1.12W \times 28°C/W = 31.4°C$

APPLICATIONS INFORMATION

The maximum junction temperature will be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$T_{JMAX} = 50°C + 31.4°C = 81.4°C$

Output Capacitance and Transient Performance

The LT1528 is designed to be stable with a wide range of output capacitors. The minimum recommended value is 3.3µF with an ESR of 2Ω or less. The LT1528 output transient response will be a function of output capacitance. See the Transient Response curves in the Typical Performance Characteristics. Larger values of output capacitance will decrease the peak deviations and provide improved output transient response for larger load transients. Bypass capacitors, used to decouple individual components powered by the LT1528, will increase the effective value of the output capacitor.

Microprocessor Applications

The LT1528 has been optimized for microprocessor applications, with the fastest transient response of current PNP low dropout regulators. In order to deal with the large load transients associated with current generation microprocessors, output capacitance must be increased. To meet worst-case voltage specifications for many popular processors, four 47µF solid tantalum surface mount capacitors are recommended for decoupling at the microprocessor. These capacitors should have an ESR of approximately 0.1Ω to 0.2Ω to minimize transient response under worst-case load deltas. The Typical Application shows connections needed to supply power for several different processors. This application allows the output voltage to be jumper selectable.

Protection Features

The LT1528 incorporates several protection features, such as current limiting and thermal limiting, in addition to the normal protection features associated with monolithic regulators. The device is protected against reverse input voltages and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against overload conditions. For normal operation the junction temperatures should not exceed 125°C.

The input of the device will withstand reverse voltages of 15V. Current flow into the device will be limited to less than 1mA (typically less than 100µA) and no negative voltage will appear at the output. The device will protect both itself and the load.

The Sense pin is internally clamped to one diode drop below ground. If the Sense pin is pulled below ground, with the input open or grounded, current must be limited to less than 5mA.

Several different input/output conditions can occur in regulator circuits. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open circuit. Current flow back into the output will vary depending on the conditions. Many circuits incorporate some form of power management. The following information summarized in Table 2 will help optimize power usage.

Table 2. Fault Conditions

INPUT PIN	$\overline{SHDN}$ PIN	OUTPUT/SENSE PINS	RESULTING CONDITIONS
< V_{OUT} (Nominal)	Open (High)	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 150µA (See Figure 3) Input Current ≈ 1µA (See Figure 4)
< V_{OUT} (Nominal)	Grounded	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 150µA (See Figure 3) Input Current ≈ 1µA (See Figure 4)
Open	Open (High)	> 1V	Reverse Output Current ≈ 150µA (See Figure 3)
Open	Grounded	> 1V	Reverse Output Current ≈ 150µA (See Figure 3)
≤ 0.8V	Open (High)	≤ 0V	Output Current = 0
≤ 0.8V	Grounded	≤ 0V	Output Current = 0
> 1.5V	Open (High)	≤ 0V	Output Current = Short-Circuit Current
−15V < V_{IN} < 15V	Grounded	≤ 0V	Output Current = 0

APPLICATIONS INFORMATION

The reverse output current will follow the curve in Figure 3 when the input is pulled to ground. This current flows through the Output pin to ground. The state of the Shutdown pin will have no effect on output current when the input pin is pulled to ground.

In some applications it may be necessary to leave the input on the LT1528 unconnected when the output is held high. This can happen when the LT1528 is powered from a rectified AC source. If the AC source is removed, then the input of the LT1528 is effectively left floating. The reverse output current also follows the curve in Figure 3 if the input pin is left open. The state of the Shutdown pin will have no effect on the reverse output current when the input pin is floating.

When the input of the LT1528 is forced to a voltage below its nominal output voltage and its output is held high, the output current will follow the curve shown in Figure 3. This can happen if the input of the LT1528 is connected to a low voltage and the output is held up by a second regulator circuit. When the input pin is forced below the Output pin or the Output pin is pulled above the input pin, the input current will typically drop to less than 2μA (see Figure 4). The state of the Shutdown pin will have no effect on the reverse output current when the output is pulled above the input.

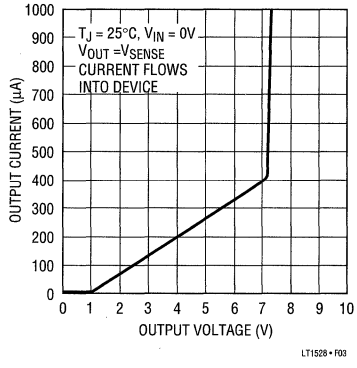


Figure 3. Reverse Output Current

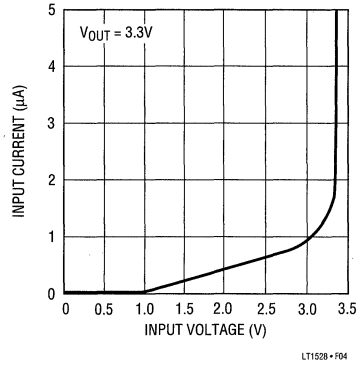


Figure 4. Input Current

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1265	High Efficiency Step-Down Switching Regulator	>90% Efficient 1A, 5V to 3.3V Conversion
LTC1266	Synchronous Switching Controller	>90% Efficient High Current Microprocessor Supply
LT1521	300mA Micropower Low Dropout Regulator	15μA Quiescent Current
LT1584	7A Low Dropout Fast Transient Response Regulator	For High Performance Microprocessors
LT1585	4.6A Low Dropout Fast Transient Response Regulator	For High Performance Microprocessors

3A Low Dropout Regulators with Micropower Quiescent Current and Shutdown

FEATURES

- **Dropout Voltage: 0.6V at I_{OUT} = 3A**
- **Output Current: 3A**
- **Quiescent Current: 50μA**
- **No Protection Diodes Needed**
- Adjustable Output from 3.8V to 14V
- 3.3V and 5V Fixed Output Voltages
- Controlled Quiescent Current in Dropout
- Shutdown I_Q = 16μA
- Stable with 3.3μF Output Capacitor
- Reverse Battery Protection
- No Reverse Current
- Thermal Limiting

APPLICATIONS

- High Efficiency Regulator
- Regulator for Battery-Powered Systems
- Post Regulator for Switching Supplies
- 5V to 3.3V Logic Regulator

DESCRIPTION

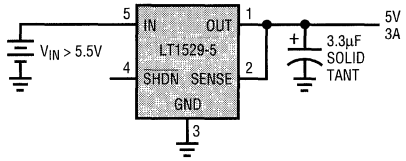
The LT®1529/LT1529-3.3/LT1529-5 are 3A low dropout regulators with micropower quiescent current and shutdown. The devices are capable of supplying 3A of output current with a dropout voltage of 0.6V. Designed for use in battery-powered systems, the low quiescent current, 50μA operating and 16μA in shutdown, make them an ideal choice. The quiescent current is well controlled; it does not rise in dropout as it does with many other low dropout PNP regulators.

Other features of the LT1529 /LT1529-3.3/LT1529-5 include the ability to operate with small output capacitors. They are stable with only 3.3μF on the output while most older devices require between 10μF and 100μF for stability. Small ceramic capacitors can be used, enhancing manufacturabiltiy. Also the input may be connected to voltages lower than the output voltage, including negative voltages, without reverse current flow from output to input. This makes the LT1529/LT1529-3.3/LT1529-5 ideal for backup power situations where the output is held high and the input is at ground or reversed. Under these conditions, only 16μA will flow from the output pin to ground. The devices are available in 5-lead TO-220 and 5-lead DD packages.

4

TYPICAL APPLICATION

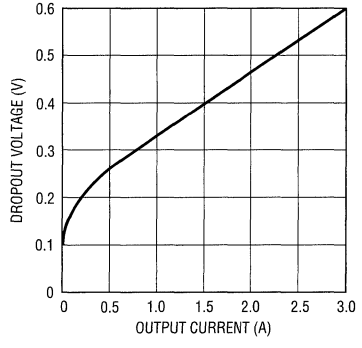
5V Supply with Shutdown



$V_{\overline{SHDN}}$ (PIN 4)	OUTPUT
<0.25	OFF
>2.8	ON
NC	ON

LT1529 • TA01

Dropout Voltage



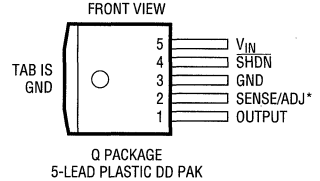
LT1529 • TA02

ABSOLUTE MAXIMUM RATINGS

Input Voltage ..... ±15V*
Output Pin Reverse Current 10mA
Sense Pin Current 10mA
Adjust Pin Current 10mA
Shutdown Pin Input Voltage (Note 1) ..... 6.5V, –0.6V
Shutdown Pin Input Current (Note 1) 5mA
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range ..... –65°C to 150°C
Operating Junction Temperature Range ... 0°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

* For applications requiring input voltage ratings greater than 15V, contact the factory.

PACKAGE/ORDER INFORMATION

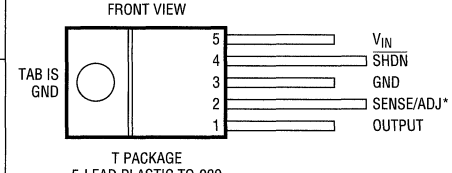


Q PACKAGE
5-LEAD PLASTIC DD PAK

*PIN 2 = SENSE FOR LT1529-3.3/LT1529-5
= ADJ FOR LT1529

$\theta_{JA} \approx 30°C/W$

ORDER PART NUMBER
LT1529CQ
LT1529CQ-3.3
LT1529CQ-5



T PACKAGE
5-LEAD PLASTIC TO-220

*PIN 2 = SENSE FOR LT1529-3.3/LT1529-5
= ADJ FOR LT1529

$\theta_{JA} \approx 50°C/W$

ORDER PART NUMBER
LT1529CT
LT1529CT-3.3
LT1529CT-5

Consult factory for Industrial or Military grade parts.

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Regulated Output Voltage (Note 2)	LT1529-3.3	V_{IN} = 3.8V, I_{OUT} = 1mA, T_J = 25°C		3.250	3.300	3.350	V
		4.3V < V_{IN} < 15V, 1mA < I_{OUT} < 3A	●	3.200	3.300	3.400	V
	LT1529-5	V_{IN} = 5.5V, I_{OUT} = 1mA, T_J = 25°C		4.925	5.000	5.075	V
		6V < V_{IN} < 15V, 1mA < I_{OUT} < 3A	●	4.850	5.000	5.150	V
	LT1529 (Note 3)	V_{IN} = 4.3V, I_{OUT} = 1mA, T_J = 25°C		3.695	3.750	3.805	V
		4.8V < V_{IN} < 15V, 1mA < I_{OUT} < 3A	●	3.640	3.750	3.860	V
Line Regulation	LT1529-3.3	ΔV_{IN} = 3.8V to 15V, I_{OUT} = 1mA	●		1.5	10	mV
	LT1529-5	ΔV_{IN} = 5.5V to 15V, I_{OUT} = 1mA	●		1.5	10	mV
	LT1529 (Note 3)	ΔV_{IN} = 4.3V to 15V, I_{OUT} = 1mA	●		1.5	10	mV
Load Regulation	LT1529-3.3	ΔI_{LOAD} = 1mA to 3A, V_{IN} = 4.3V, T_J = 25°C			5	20	mV
		ΔI_{LOAD} = 1mA to 3A, V_{IN} = 4.3V	●		12	30	mV
	LT1529-5	ΔI_{LOAD} = 1mA to 3A, V_{IN} = 6V, T_J = 25°C			5	20	mV
		ΔI_{LOAD} = 1mA to 3A, V_{IN} = 6V	●		12	30	mV
	LT1529 (Note 3)	ΔI_{LOAD} = 1mA to 3A, V_{IN} = 4.8V, T_J = 25°C			5	20	mV
		ΔI_{LOAD} = 1mA to 3A, V_{IN} = 4.8V	●		12	30	mV
Dropout Voltage (Note 4)	I_{LOAD} = 10mA, T_J = 25°C				110	180	mV
	I_{LOAD} = 10mA		●			250	mV
	I_{LOAD} = 100mA, T_J = 25°C				200	300	mV
	I_{LOAD} = 100mA		●			400	mV

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Dropout Voltage (Note 4)	I_{LOAD} = 700mA, T_J = 25°C			320	430	mV
	I_{LOAD} = 700mA	●			550	mV
	I_{LOAD} = 1.5A, T_J = 25°C			430	550	mV
	I_{LOAD} = 1.5A	●			700	mV
	I_{LOAD} = 3A, T_J = 25°C			600	750	mV
	I_{LOAD} = 3A	●			950	mV
Ground Pin Current (Note 5)	I_{LOAD} = 0mA, T_J = 25°C			50	100	µA
	I_{LOAD} = 0mA, T_J = 125°C (Note 6)			400		µA
	I_{LOAD} = 100mA, T_J = 25°C			0.6	1.0	mA
	I_{LOAD} = 100mA, T_J = 125°C (Note 6)			1.0		mA
	I_{LOAD} = 700mA	●		5.5	12	mA
	I_{LOAD} = 1.5A	●		20	40	mA
	I_{LOAD} = 3A	●		80	160	mA
Adjust Pin Bias Current (Notes 3, 7)	T_J = 25°C			150	300	nA
Shutdown Threshold	V_{OUT} = Off to On	●		1.20	2.8	V
	V_{OUT} = On to Off	●	0.25	0.75		V
Shutdown Pin Current (Note 8)	$V_{\overline{SHDN}}$ = 0V	●		4.5	10	µA
Quiescent Current in Shutdown (Note 9)	V_{IN} = 6V, $V_{\overline{SHDN}}$ = 0V	●		15	30	µA
Ripple Rejection	$V_{IN} - V_{OUT}$ = 1V (Avg), V_{RIPPLE} = 0.5V_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 1.5A		50	62		dB
Current Limit	$V_{IN} - V_{OUT}$ = 7V, T_J = 25°C			5		A
	V_{IN} = V_{OUT} (Nominal) + 1.5V, ΔV_{OUT} = −0.1V	●	3.2	4.7		A
Input Reverse Leakage Current	V_{IN} = −15V, V_{OUT} = 0V	●			1.0	mA
Reverse Output Current (Note 10)	LT1529-3.3 V_{OUT} = 3.3V, V_{IN} = 0V			16		µA
	LT1529-5 V_{OUT} = 5V, V_{IN} = 0V			16		µA
	LT1529 (Note 4) V_{OUT} = 3.8V, V_{IN} = 0V			16		µA

The ● denotes specifications which apply over the operating temperature range.

Note 1: The shutdown pin input voltage rating is required for a low impedance source. Internal protection devices connected to the shutdown pin will turn on and clamp the pin to approximately 7V or −0.6V. This range allows the use of 5V logic devices to drive the pin directly. For high impedance sources or logic running on supply voltages greater than 5.5V, the maximum current driven into the shutdown pin must be limited to less than 5mA.

Note 2: Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current the input voltage range must be limited.

Note 3: The LT1529 is tested and specified with the adjust pin connected to the output pin.

Note 4: Dropout voltage is the minimum input/output voltage required to maintain regulation at the specified output current. In dropout the output voltage will be equal to ($V_{IN} - V_{DROPOUT}$).

Note 5: Ground pin current is tested with V_{IN} = V_{OUT} (nominal) and a current source load. This means that the device is tested while operating in its dropout region. This is the worst-case ground pin current. The ground pin current will decrease slightly at higher input voltages.

Note 6: Ground pin current will rise at T_J > 75°C. This is due to internal circuitry designed to compensate for leakage currents in the output transistor at high temperatures. This allows quiescent current to be minimized at lower temperatures, yet maintain output regulation at high temperatures with light loads. See quiescent current curve in typical performance characteristics.

Note 7: Adjust pin bias current flows into the adjust pin.

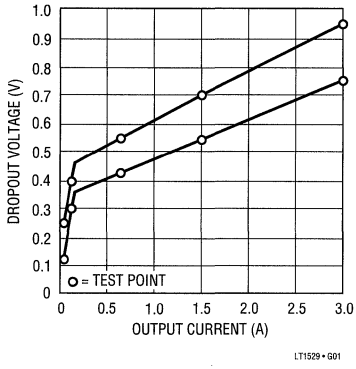
Note 8: Shutdown pin current at V_{SHDN} = 0V flows out of the shutdown pin.

Note 9: Quiescent current in shutdown is equal to the sum total of the shutdown pin current (5µA) and the ground pin current (10µA).

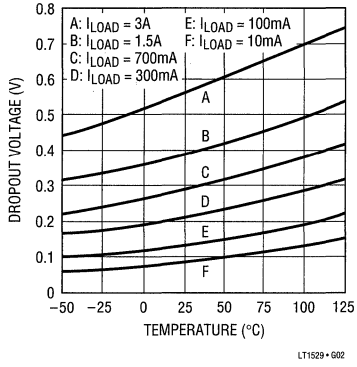
Note 10: Reverse output current is tested with the input pin grounded and the output pin forced to the rated output voltage. This current flows into the output pin and out of the ground pin.

TYPICAL PERFORMANCE CHARACTERISTICS

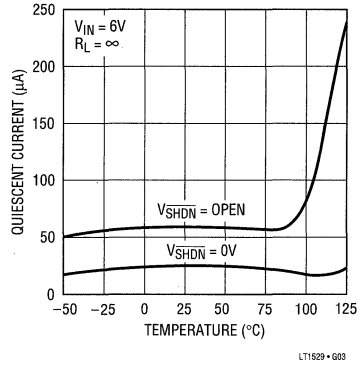
Guaranteed Dropout Voltage



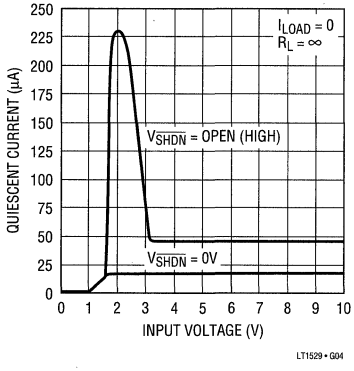
Dropout Voltage



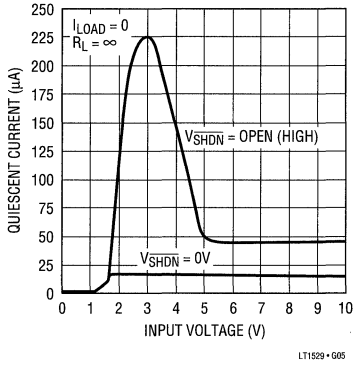
Quiescent Current



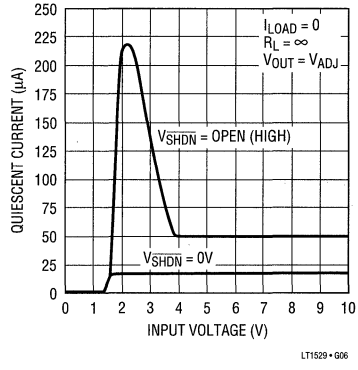
LT1529-3.3 Quiescent Current



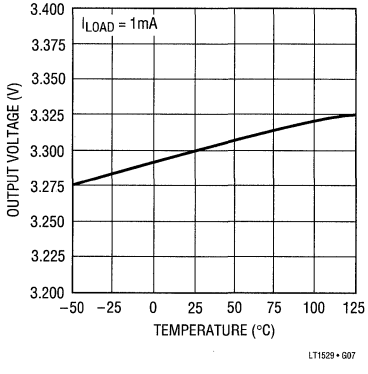
LT1529-5 Quiescent Current



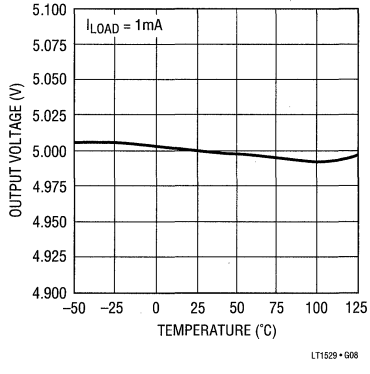
LT1529 Quiescent Current



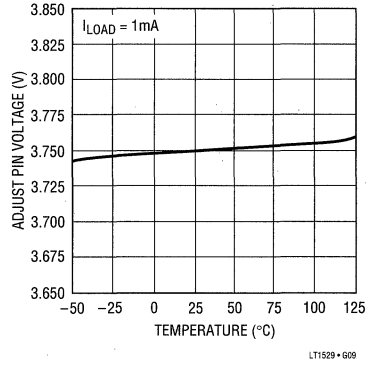
LT1529-3.3 Output Voltage



LT1529-5 Output Voltage

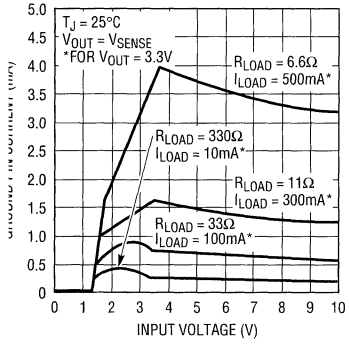


LT1529 Adjust Pin Voltage

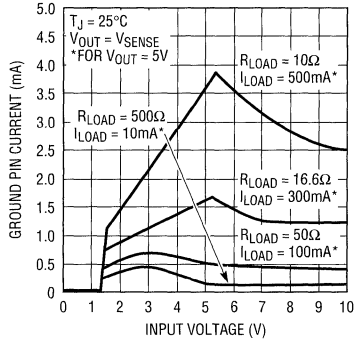


TYPICAL PERFORMANCE CHARACTERISTICS

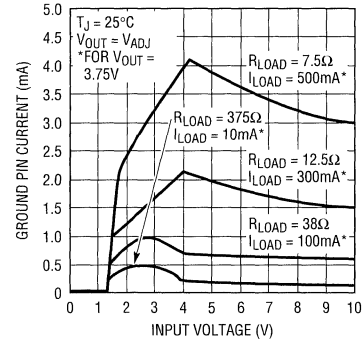
LT1529-3.3
Ground Pin Current



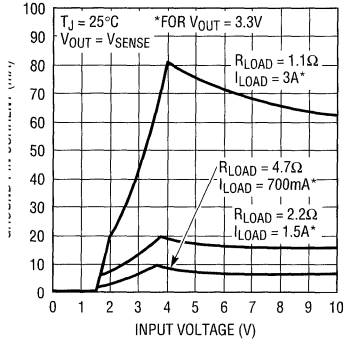
LT1529-5
Ground Pin Current



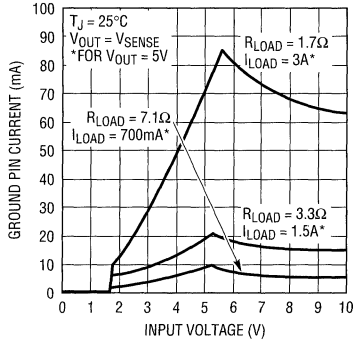
LT1529
Ground Pin Current



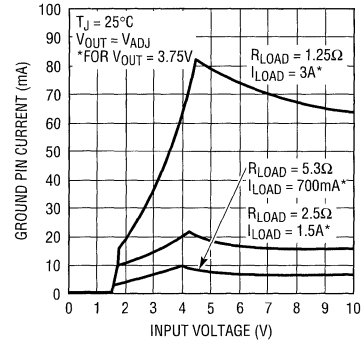
LT1529-3.3
Ground Pin Current



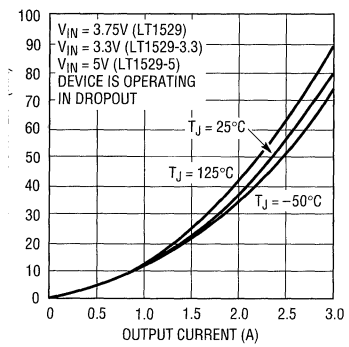
LT1529-5
Ground Pin Current



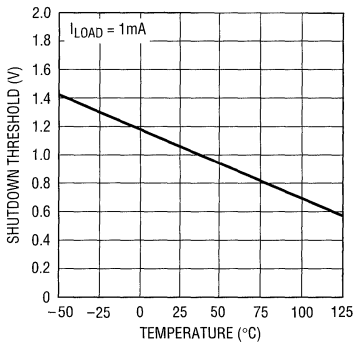
LT1529
Ground Pin Current



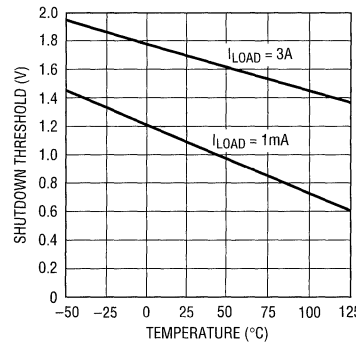
Ground Pin Current



Shutdown Pin Threshold
(On-to-Off)

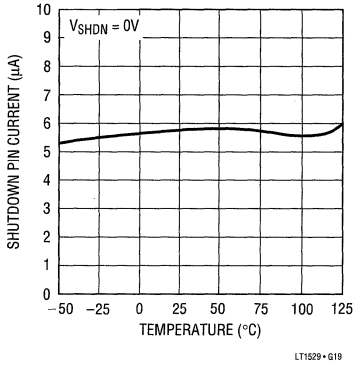


Shutdown Pin Threshold
(Off-to-On)

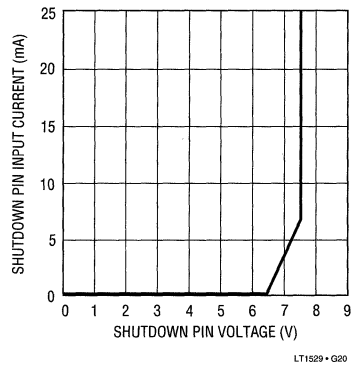


TYPICAL PERFORMANCE CHARACTERISTICS

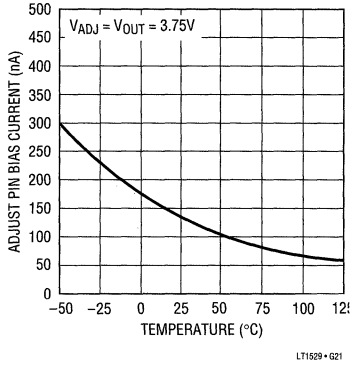
Shutdown Pin Current



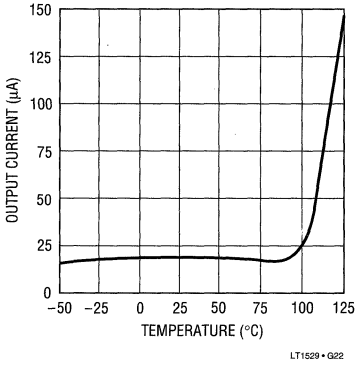
Shutdown Pin Input Current



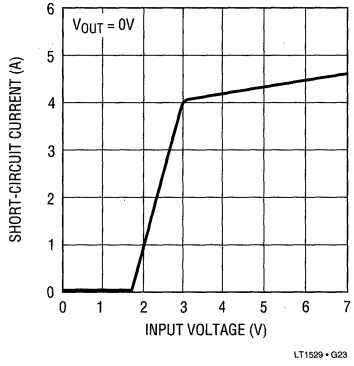
Adjust Pin Bias Current



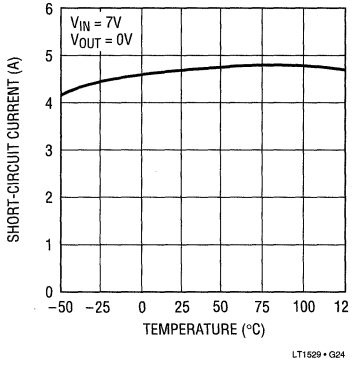
Reverse Output Current



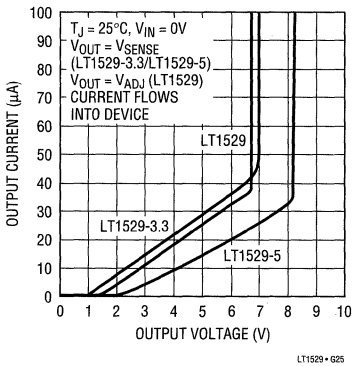
Current Limit



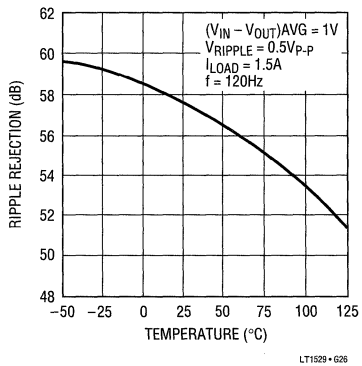
Current Limit



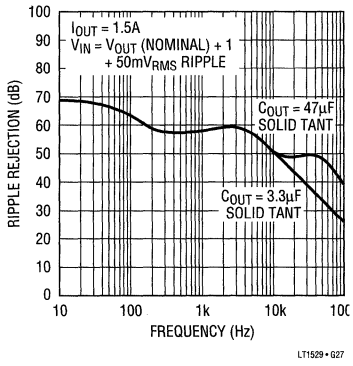
Reverse Output Current



Ripple Rejection

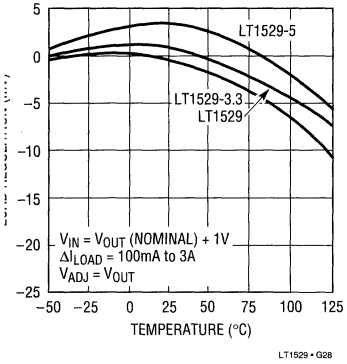


Ripple Rejection

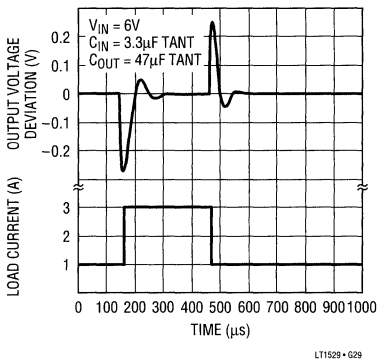


TYPICAL PERFORMANCE CHARACTERISTICS

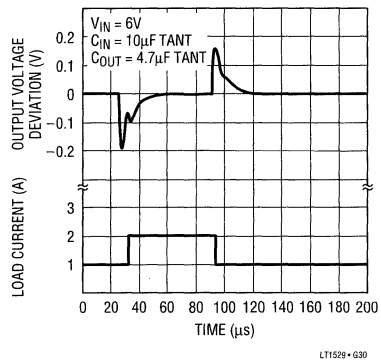
Load Regulation



LT1529-5 Transient Response



LT1529-5 Transient Response



PIN FUNCTIONS

VOUT (Pin 1): Output Pin. The output pin supplies power to the load. A minimum output capacitor of 3.3µF is required to prevent oscillations. Larger values will be required to optimize transient response for large load current deltas. See the Applications Information section for further information on output capacitance and reverse output characteristics.

SENSE (Pin 2): Sense Pin. For fixed voltage versions of the LT1529 (LT1529-3.3, LT1529-5) the sense pin is the input to the error amplifier. Optimum regulation will be obtained at the point where the sense pin is connected to the output pin. For most applications the sense pin is connected directly to the output pin at the regulator. In critical applications small voltage drops caused by the resistance (R_P) of PC traces between the regulator and the load, which would normally degrade regulation, may be eliminated by connecting the sense pin to the output pin at the load as shown in Figure 1 (Kelvin Sense Connection). Note that the voltage drop across the external PC traces will add to the dropout voltage of the regulator. The sense pin bias current is 15µA at the nominal regulated output voltage. This pin is internally clamped to –0.6V (one V_{BE}).

ADJ (Pin 2): Adjust Pin. For the LT1529 (adjustable version) the adjust pin is the input to the error amplifier. This pin is internally clamped to 6V and –0.6V (one V_{BE}).

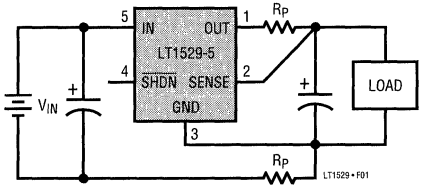


Figure 1. Kelvin Sense Connection

This pin has a bias current of 150nA which flows into the pin. See Bias Current curve in the Typical Performance Characteristics. The adjust pin reference voltage is equal to 3.75V referenced to ground.

SHDN (Pin 4): Shutdown Pin. This pin is used to put the device into shutdown. In shutdown the output of the device is turned off. This pin is active low. The device will be shut down if the shutdown pin is actively pulled low. The shutdown pin current with the pin pulled to ground will be 6µA. The shutdown pin is internally clamped to 7V and –0.6V (one V_{BE}). This allows the shutdown pin to be driven directly by 5V logic or by open-collector logic with a pull-up resistor. The pull-up resistor is only required to supply the leakage current of the open-collector gate, normally several microamperes. Pull-up current must be limited to a maximum of 5mA. A curve of shutdown pin input current as a function of voltage appears in the Typical Perfor-

PIN FUNCTIONS

mance Characteristics. If the shutdown pin is not used it can be left open circuit. The device will be active, output on, if the shutdown pin is not connected.

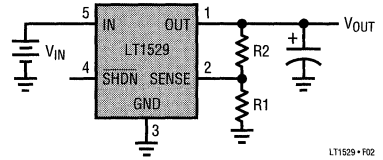
V_{IN} (Pin 5): Input Pin. Power is supplied to the device through the input pin. The input pin should be bypassed to ground if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor in the range of 1µF to 10µF is sufficient The LT1529 is designed to withstand reverse voltages or the input pin with respect to ground and output pin. In the case of a reversed input, which can happen if a battery is plugged in backwards, the LT1529 will act as if there is a diode in series with its input. There will be no reverse current flow into the LT1529 and no reverse voltage will appear at the load. The device will protect both itself and the load.

APPLICATIONS INFORMATION

The LT1529 is a 3A low dropout regulator with micropower quiescent current and shutdown capable of supplying 3A of output current at a dropout voltage of 0.6V. The device operates with very low quiescent current (50µA). In shutdown the quiescent current drops to only 16µA. In addition to the low quiescent current the LT1529 incorporates several protection features which make it ideal for use in battery-powered systems. The device is protected against reverse input voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground, the LT1529 acts like it has a diode in series with its output and prevents reverse current flow.

Adjustable Operation

The adjustable version of the LT1529 has an output voltage range of 3.75V to 14V. The output voltage is set by the ratio of two external resistors as shown in Figure 2. The device servos the output voltage to maintain the voltage at the adjust pin at 3.75V. The current in R1 is then equal to 3.75V/R1. The current in R2 is equal to the sum of the current in R1 and the adjust pin bias current. The adjust pin bias current, 150nA at 25°C, flows through R2 into the adjust pin. The output voltage can be calculated according to the formula in Figure 2. The value of R1 should be less than 400k to minimize errors in the output voltage caused by the adjust pin bias current. Note that in shutdown the output is turned off and the divider current will be zero. Curves of Adjust Pin Voltage vs Temperature and Adjust



$$V_{OUT} = 3.75V\left(1 + \frac{R2}{R1}\right) + (I_{ADJ} \times R2)$$

$V_{ADJ} = 3.75V$
$I_{ADJ} = 150nA$ AT 25°C
OUTPUT RANGE = 3.3V TO 14V

Figure 2. Adjustable Operation

Pin Bias Current vs Temperature appear in the Typical Performance Characteristics. The reference voltage at the adjust pin has a positive temperature coefficient of approximately 15ppm/°C. The adjust pin bias current has a negative temperature coefficient. These effects will tend to cancel each other.

The adjustable device is specified with the adjust pin tied to the output pin. This sets the output voltage to 3.75V. Specifications for output voltage greater than 3.75V will be proportional to the ratio of the desired output voltage to 3.75V (V_{OUT}/3.75V). For example: load regulation for an output current change of 1mA to 3A is –0.5mV typical at V_{OUT} = 3.75V. At V_{OUT} = 12V, load regulation would be:

$$\left(\frac{12V}{3.75V}\right) \times (-0.5mV) = (-1.6mV)$$

APPLICATIONS INFORMATION

Thermal Considerations

The power handling capability of the device will be limited by the maximum rated junction temperature (125°C). The power dissipated by the device will be made up of two components:

1. Output current multiplied by the input/output voltage differential: $I_{OUT} \times (V_{IN} - V_{OUT})$, and
2. Ground pin current multiplied by the input voltage: $I_{GND} \times V_{IN}$.

The ground pin current can be found by examining the Ground Pin Current curves in the Typical Performance Characteristics. Power dissipation will be equal to the sum of the two components listed above.

The LT1529 series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal load conditions the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Experiments have shown that the heat spreading copper layer does not need to be electrically connected to the tab of the device. The PC material can be very effective at transmitting heat between the pad area, attached to the tab of the device, and a ground or power plane layer either inside or on the opposite side of the board. Although the actual thermal resistance of the PC material is high, the length/area ratio of the thermal resistor between layers is small. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

The following tables list thermal resistances for each package. For the TO-220 package, thermal resistance is given for junction-to-case only since this package is usually mounted to a heat sink. Measured values of thermal resistance for several different copper areas are listed for the DD package. All measurements were taken in still air on 3/32" FR-4 board with 1-oz copper. This data can be used as a rough guideline in estimating thermal resistance. The thermal resistance for each application will be affected by thermal interactions with other components as well as board size and shape. Some experimentation will be necessary to determine the actual value.

Table 1. Q Package, 5-Lead DD

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq. mm	2500 sq. mm	2500 sq. mm	23°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	25°C/W
125 sq. mm	2500 sq. mm	2500 sq. mm	33°C/W

* Device is mounted on topside.

T Package, 5-Lead TO-220
Thermal Resistance (Junction-to-Case) = 2.5°C/W

Calculating Junction Temperature

Example: Given an output voltage of 3.3V, an input voltage range of 4.5V to 5.5V, an output current range of 0mA to 500mA, and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

The power dissipated by the device will be equal to:

$$I_{OUT(MAX)} \times (V_{IN(MAX)} - V_{OUT}) + (I_{GND} \times V_{IN(MAX)})$$

where, $I_{OUT(MAX)} = 500mA$
$V_{IN(MAX)} = 5.5V$
I_{GND} at ($I_{OUT} = 500mA$, $V_{IN} = 5.5V$) = 3.6mA

so, $P = 500mA \times (5.5V - 3.3V) + (3.6mA \times 5.5V)$
$= 1.12W$

If we use a DD package, then the thermal resistance will be in the range of 23°C/W to 33°C/W depending on copper area. So the junction temperature rise above ambient will be approximately equal to:

$$1.12W \times 28°C/W = 31.4°C$$

The maximum junction temperature will then be equal to the maximum junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_{JMAX} = 50°C + 31.4°C = 81.4°C$$

Output Capacitance and Transient Performance

The LT1529 is designed to be stable with a wide range of output capacitors. The minimum recommended value is 3.3µF with an ESR of 2Ω or less. The LT1529 is a

APPLICATIONS INFORMATION

micropower device and output transient response will be a function of output capacitance. See the Transient Response curves in the Typical Performance Characteristics. Larger values of output capacitance will decrease the peak deviations and provide improved output transient response for larter load current deltas. Bypass capacitors, used to decouple individual components powered by the LT1529, will increase the effective value of the output capacitor.

Protection Features

The LT1529 incorporates several protection features which make it ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse input voltages, and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device will withstand reverse voltages of 15V. Current flow into the device will be limited to less than 1mA (typically less than 100µA) and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries that can be plugged in backwards.

For fixed voltage versions of the device, the sense pin is internally clamped to one diode drop below ground. For the adjustable version of the device, the output pin is internally clamped at one diode drop below ground. If the output pin of an adjustable device, or the sense pin of a fixed voltage device, is pulled below ground, with the input open or grounded, current must be limited to less than 5mA.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit. Current flow back into the output will vary depending on the conditions. Many battery-powered circuits incorporate some form of power management. The following information will help optimize battery life. Table 2 summarizes the following information.

The reverse output current will follow the curve in Figure 3 when the input is pulled to ground. This current flows through the device to ground. The state of the shutdown pin will have no effect on output current when the input pin is pulled to ground.

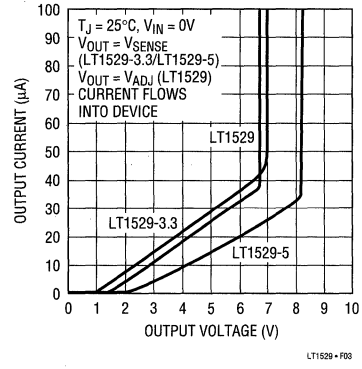


Figure 3. Reverse Output Current

Table 2. Fault Conditions

INPUT PIN	$\overline{SHDN}$ PIN	OUTPUT/SENSE PINS	
$<V_{OUT}$ (Nominal)	Open (High)	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 15µA (See Figure 3), Input Current ≈ 1µA (See Figure 4)
$<V_{OUT}$ (Nominal)	Grounded	Forced to V_{OUT} (Nominal)	Reverse Output Current ≈ 15µA (See Figure 3), Input Current ≈ 1µA (See Figure 4)
Open	Open (High)	> 1V	Reverse Output Current ≈ 15µA Peak (See Figure 3)
Open	Grounded	> 1V	Reverse Output Current ≈ 15µA (See Figure 3)
≤0.8V	Open (High)	≤0V	Output Current = 0
≤0.8V	Grounded	≤0V	Output Current = 0
>1.5V	Open (High)	≤0V	Output Current = Short-Circuit Current
$-15V < V_{IN} < 15V$	Grounded	≤0V	Output Current = 0

IPPLICATIONS INFORMATION

ı some applications it may be necessary to leave the input ı the LT1529 unconnected when the output is held high. ıis can happen when the LT1529 is powered from a ːctified AC source. If the AC source is removed, then the put of the LT1529 is effectively left floating. The reverse ɹtput current also follows the curve in Figure 3 if the input n is left open. The state of the shutdown pin will have no ffect on the reverse output current when the input pin is ɔating.

/hen the input of the LT1529 is forced to a voltage below ɜ nominal output voltage and its output is held high, the ɹtput current will follow the curve shown in Figure 3. This ɪn happen if the input of the LT1529 is connected to a scharged (low voltage) battery and the output is held up / either a backup battery or by a second regulator circuit. /hen the input pin is forced below the output pin or the ɹtput pin is pulled above the input pin, the input current will typically drop to less than 2µA (see Figure 4). The state of the shutdown pin will have no effect on the reverse output current when the output is pulled above the input.

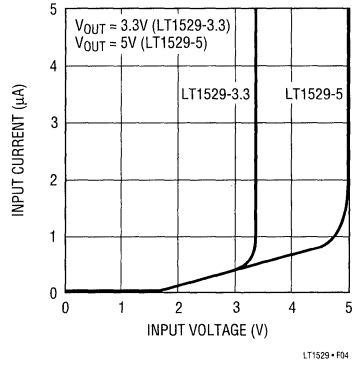


Figure 4. Input Current

4

ELATED PARTS

ART NUMBER	DESCRIPTION	COMMENTS
1120A	125mA Low Dropout Regulator with 20µA I_Q	Includes 2.5V Reference and Comparator
C®1174	High Efficiency 425mA Step-Down DC/DC Converter	Over 90% Efficiency, Includes Comparator
1303	Micropower Step-Up DC/DC Converter	Includes Comparator, Good for EL Displays
1376	500kHz 1.25A Step-Down DC/DC Converter	Uses Extremely Small External Components
1521	300µA Low Dropout Regulator with 15µA I_Q	Lowest I_Q Low Dropout Regulator

7A, 4.6A, 3A Low Dropout Fast Response Positive Regulators Adjustable and Fixed

FEATURES

- **Fast Transient Response**
- **Guaranteed Dropout Voltage at Multiple Currents**
- Load Regulation: 0.05% Typ
- Trimmed Current Limit
- On-Chip Thermal Limiting
- Standard 3-Pin Power Package

APPLICATIONS

- Pentium™ Processor Supplies
- PowerPC™ Supplies
- Other 2.5V to 3.6V Microprocessor Supplies
- Low Voltage Logic Supplies
- Battery-Powered Circuitry
- Post Regulator for Switching Supply

LT1585/7CM, LT1584/5/7CT	Adjustable
LT1585/7CM-3.3, LT1584/5/7CT-3.3	3.3V Fixed
LT1585CM-3.38, LT1584/5CT-3.38	3.38V Fixed
LT1585/7CM-3.45, LT1584/5/7CT-3.45	3.45V Fixed
LT1585/7CM-3.6, LT1584/5/7CT-3.6	3.6V Fixed

DESCRIPTION

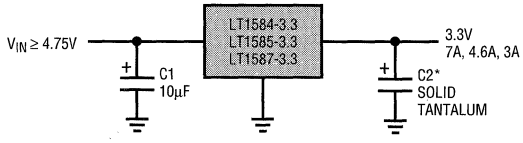
The LT®1584/LT1585/LT1587 are low dropout three terminal regulators with 7A, 4.6A and 3A output curren capability, respectively. Design has been optimized for lov voltage applications where transient response and mini mum input voltage are critical. Similar to the LT1083/4/5 family, it has lower dropout voltage and faster transien response. These improvements make it ideal for low volt age microprocessor applications requiring a regulatec 2.5V to 3.6V output with an input supply below 7V.

Current limit is trimmed to ensure specified output curren and controlled short-circuit current. On-chip thermal lim iting provides protection against any combination of over load that would create excessive junction temperatures.

The LT1585/LT1587 are available in both the through-hol and surface mount versions of the industry standard 3-pi TO-220 power package. The LT1584 is available in th through-hole 3-pin TO-220 power package.

TYPICAL APPLICATION

3.3V, 7A, 4.6A, 3A Regulator

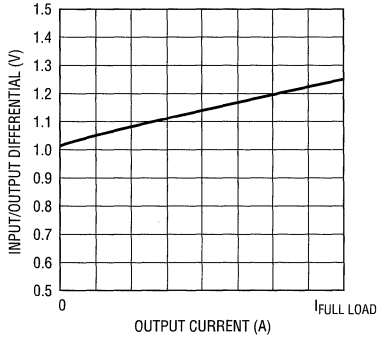


* REQUIRED FOR STABILITY
LT1584: C2 = 22µF,
LT1585/LT1587: C2 = 10µF

1585 TA01

NOTE: MICROPROCESSOR APPLICATIONS WITH LOAD TRANSIENTS OF 3.8A REQUIRE OUTPUT DECOUPLING CAPACITANCE > 1300µF ON FIXED VOLTAGE PARTS TO ACHIEVE < 50mV OF DEVIATION FROM NOMINAL OUTPUT. CONSULT FACTORY FOR DETAILS

Dropout Voltage vs Output Current



1585 TA02

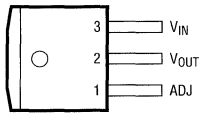
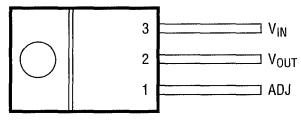
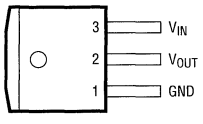
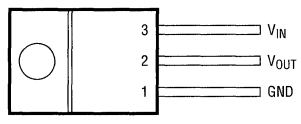
BSOLUTE MAXIMUM RATINGS

N 7V
)erating Junction Temperature Range
Control Section ..... 0°C to 125°C
Power Transistor ..... 0°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PRECONDITIONING

100% Thermal Limit Functional Test

ACKAGE/ORDER INFORMATION

FRONT VIEW  M PACKAGE 3-LEAD PLASTIC DD PAK θ_{JA} = 30°C/W*	ORDER PART NUMBER LT1585CM LT1587CM	FRONT VIEW  T PACKAGE 3-LEAD PLASTIC TO-220 θ_{JA} = 50°C/W	ORDER PART NUMBER LT1584CT LT1585CT LT1587CT
FRONT VIEW  M PACKAGE 3-LEAD PLASTIC DD PAK θ_{JA} = 30°C/W*	LT1585CM-3.3 LT1585CM-3.38 LT1585CM-3.45 LT1585CM-3.6 LT1587CM-3.3 LT1587CM-3.45 LT1587CM-3.6	FRONT VIEW  T PACKAGE 3-LEAD PLASTIC TO-220 θ_{JA} = 50°C/W	LT1584CT-3.3 LT1584CT-3.45 LT1585CT-3.3 LT1585CT-3.45 LT1587CT-3.3 LT1587CT-3.45 LT1584CT-3.38 LT1584CT-3.6 LT1585CT-3.38 LT1585CT-3.6 LT1587CT-3.6

/ith package soldered to 0.5 square inch copper area over backside
round plane or internal power plane. θ_{JA} can vary from 20°C/W to 40°C/W with other mounting techniques.

Consult factory for Industrial and Military grade parts.

LECTRICAL CHARACTERISTICS

RAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
erence Voltage	LT1584 LT1585 LT1587	1.5V ≤ (V_{IN} – V_{OUT}) ≤ 3V, 10mA ≤ I_{OUT} ≤ 7A 1.5V ≤ (V_{IN} – V_{OUT}) ≤ 5.75V, 10mA ≤ I_{OUT} ≤ 4.6A, T_J ≥ 25°C 1.5V ≤ (V_{IN} – V_{OUT}) ≤ 5.75V, 10mA ≤ I_{OUT} ≤ 4A, T_J < 25°C 1.5V ≤ (V_{IN} – V_{OUT}) ≤ 5.75V, 10mA ≤ I_{OUT} ≤ 3A	●	1.225 (– 2%)	1.250	1.275 (+2%)	V
:put Voltage	LT1584-3.3 LT1585-3.3 LT1587-3.3	4.75V ≤ V_{IN} ≤ 6.3V, 0mA ≤ I_{OUT} ≤ 7A 4.75V ≤ V_{IN} ≤ 7V, 0mA ≤ I_{OUT} ≤ 4.6A, T_J ≥ 25°C 4.75V ≤ V_{IN} ≤ 7V, 0mA ≤ I_{OUT} ≤ 4A, T_J < 25°C 4.75V ≤ V_{IN} ≤ 7V, 0mA ≤ I_{OUT} ≤ 3A	●	3.235 (– 2%)	3.300	3.365 (+2%)	V
	LT1584-3.38 LT1585-3.38	4.75V ≤ V_{IN} ≤ 6.38V, 0mA ≤ I_{OUT} ≤ 7A 4.75V ≤ V_{IN} ≤ 7V, 0mA ≤ I_{OUT} ≤ 4A	●	3.313 (– 2%)	3.380	3.465 (+2.5%)	V
	LT1584-3.45 LT1585-3.45 LT1587-3.45	4.75V ≤ V_{IN} ≤ 6.45V, 0mA ≤ I_{OUT} ≤ 7A 4.75V ≤ V_{IN} ≤ 7V, 0mA ≤ I_{OUT} ≤ 4A 4.75V ≤ V_{IN} ≤ 7V, 0mA ≤ I_{OUT} ≤ 3A	●	3.381 (– 2%)	3.450	3.519 (+2%)	V
	LT1584-3.6 LT1584-3.6 LT1584-3.6 LT1584-3.6	4.75V ≤ V_{IN} ≤ 7V, 0mA ≤ I_{OUT} ≤ 6A 4.80V ≤ V_{IN} ≤ 7V, 0mA ≤ I_{OUT} ≤ 6A 4.80V ≤ V_{IN} ≤ 6.6V, 0mA ≤ I_{OUT} ≤ 7A 4.85V ≤ V_{IN} ≤ 6.6V, 0mA ≤ I_{OUT} ≤ 7A	● ● ● ●	3.400 (– 5.5%) 3.450 (– 4%) 3.431 (– 4.7%) 3.481 (– 3.3%)	3.600 3.600 3.600 3.600	3.672 (+2%) 3.672 (+2%) 3.672 (+2%) 3.672 (+2%)	V V V V

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
Output Voltage	LT1585/7-3.6	$4.75V \le V_{IN} \le 7V$, $0mA \le I_{OUT} \le 3A$	●	3.474 (–3.5%)	3.600	3.672 (+2%)	
	LT1585/7-3.6	$4.80V \le V_{IN} \le 7V$, $0mA \le I_{OUT} \le 3A$	●	3.528 (–2%)	3.600	3.672 (+2%)	
	LT1585-3.6	$4.80V \le V_{IN} \le 7V$, $0mA \le I_{OUT} \le 4A$	●	3.450 (–4%)	3.600	3.672 (+2%)	
	LT1585-3.6	$4.85V \le V_{IN} \le 7V$, $0mA \le I_{OUT} \le 4A$	●	3.492 (–3%)	3.600	3.672 (+2%)	
Line Regulation (Notes 1, 2)	LT1584/5/7	$2.75V \le V_{IN} \le 7V$, $I_{OUT} = 10mA$					
	LT1584/5/7-3.3	$4.75V \le V_{IN} \le 7V$, $I_{OUT} = 0mA$					
	LT1584/5-3.38	$4.75V \le V_{IN} \le 7V$, $I_{OUT} = 0mA$					
	LT1584/5/7-3.45	$4.75V \le V_{IN} \le 7V$, $I_{OUT} = 0mA$					
	LT1584/5/7-3.6	$4.75V \le V_{IN} \le 7V$, $I_{OUT} = 0mA$	●		0.005	0.2	%
Load Regulation (Notes 1, 2, 3)	LT1584/5/7	$(V_{IN} - V_{OUT}) = 3V$, $T_J = 25°C$, $10mA \le I_{OUT} \le I_{FULL\ LOAD}$					
	LT1584/5/7-3.3	$V_{IN} = 5V$, $T_J = 25°C$, $0mA \le I_{OUT} \le I_{FULL\ LOAD}$					
	LT1584/5-3.38	$V_{IN} = 5V$, $T_J = 25°C$, $0mA \le I_{OUT} \le I_{FULL\ LOAD}$					
	LT1584/5/7-3.45	$V_{IN} = 5V$, $T_J = 25°C$, $0mA \le I_{OUT} \le I_{FULL\ LOAD}$					
	LT1584/5/7-3.6	$V_{IN} = 5.25V$, $T_J = 25°C$, $0mA \le I_{OUT} \le I_{FULL\ LOAD}$			0.05	0.3	%
			●		0.05	0.5	%
Dropout Voltage	LT1585/7	$\Delta V_{REF} = 1\%$, $I_{OUT} = 3A$					
	LT1585/7-3.3	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 3A$					
	LT1585-3.38	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 3A$					
	LT1585/7-3.45	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 3A$					
	LT1585/7-3.6	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 3A$	●		1.150	1.300	
	LT1585	$\Delta V_{REF} = 1\%$, $I_{OUT} = 4.6A$, $T_J \ge 25°C$					
		$\Delta V_{REF} = 1\%$, $I_{OUT} = 4A$, $T_J < 25°C$					
	LT1585-3.3	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 4.6A$, $T_J \ge 25°C$					
		$\Delta V_{OUT} = 1\%$, $I_{OUT} = 4A$, $T_J < 25°C$					
	LT1585-3.38	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 4A$					
	LT1585-3.45	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 4A$					
	LT1585-3.6	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 4A$	●		1.200	1.400	
	LT1584	$\Delta V_{REF} = 1\%$, $I_{OUT} = 6A$					
	LT1584-3.3	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 6A$					
	LT1584-3.38	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 6A$					
	LT1584-3.45	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 6A$					
	LT1584-3.6	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 6A$					
		$T_J \ge 25°C$	●		1.200	1.300	
		$T_J < 25°C$	●		1.200	1.350	
	LT1584	$\Delta V_{REF} = 1\%$, $I_{OUT} = 7A$					
	LT1584-3.3	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 7A$					
	LT1584-3.38	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 7A$					
	LT1584-3.45	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 7A$					
	LT1584-3.6	$\Delta V_{OUT} = 1\%$, $I_{OUT} = 7A$	●		1.250	1.400	
Current Limit (Note 3)	LT1584	$(V_{IN} - V_{OUT}) = 3V$					
	LT1584-3.3	$(V_{IN} - V_{OUT}) = 3V$					
	LT1584-3.38	$(V_{IN} - V_{OUT}) = 3V$					
	LT1584-3.45	$(V_{IN} - V_{OUT}) = 3V$					
	LT1584-3.6	$(V_{IN} - V_{OUT}) = 3V$	●	7.100	8.250		
	LT1585	$(V_{IN} - V_{OUT}) = 5.5V$					
	LT1585-3.3	$(V_{IN} - V_{OUT}) = 5.5V$					
		$T_J \ge 25°C$	●	4.600	5.25		
		$T_J < 25°C$	●	4.100	5.25		
	LT1585-3.38	$(V_{IN} - V_{OUT}) = 5.5V$					
	LT1585-3.45	$(V_{IN} - V_{OUT}) = 5.5V$					
	LT1585-3.6	$(V_{IN} - V_{OUT}) = 5.5V$	●	4.100	4.750		
	LT1587	$(V_{IN} - V_{OUT}) = 5.5V$					
	LT1587-3.3	$(V_{IN} - V_{OUT}) = 5.5V$					
	LT1587-3.45	$(V_{IN} - V_{OUT}) = 5.5V$					
	LT1587-3.6	$(V_{IN} - V_{OUT}) = 5.5V$	●	3.100	3.750		

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Adjust Pin Current	LT1584/5/7		●		55	120	µA
Adjust Pin Current Change (Note 3)	LT1584 LT1585/7	$1.5V \le (V_{IN} - V_{OUT}) \le 3V$, $10mA \le I_{OUT} \le I_{FULL\ LOAD}$ $1.5V \le (V_{IN} - V_{OUT}) \le 5.75V$, $10mA \le I_{OUT} \le I_{FULL\ LOAD}$	 ●		 0.2	 5	 µA
Minimum Load Current	LT1584/5/7	$1.5V \le (V_{IN} - V_{OUT}) \le 5.75V$	●		2	10	mA
Quiescent Current	LT1584/5/7-3.3 LT1584/5-3.38 LT1584/5/7-3.45 LT1584/5/7-3.6	$V_{IN} = 5V$ $V_{IN} = 5V$ $V_{IN} = 5V$ $V_{IN} = 5V$	 ●		 8	 13	 mA
Ripple Rejection	LT1584 LT1584-3.3 LT1584-3.38 LT1584-3.45 LT1584-3.6 LT1585 LT1585-3.3 LT1585-3.38 LT1585-3.45 LT1585-3.6 LT1587 LT1587-3.3 LT1587-3.45 LT1587-3.6	f = 120Hz, C_{OUT} = 25µF Tant., $(V_{IN} - V_{OUT})$ = 2.5V, I_{OUT} = 7A f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 5.8V, I_{OUT} = 7A f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 5.88V, I_{OUT} = 7A f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 5.95V, I_{OUT} = 7A f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 6.1V, I_{OUT} = 7A f = 120Hz, C_{OUT} = 25µF Tant., $(V_{IN} - V_{OUT})$ = 3V, I_{OUT} = 4.6A, $T_J \ge 25°C$ f = 120Hz, C_{OUT} = 25µF Tant., $(V_{IN} - V_{OUT})$ = 3V, I_{OUT} = 4A, $T_J < 25°C$ f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 6.3V, I_{OUT} = 4.6A, $T_J \ge 25°C$ f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 6.3V, I_{OUT} = 4A, $T_J < 25°C$ f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 6.38V, I_{OUT} = 4A f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 6.45V, I_{OUT} = 4A f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 6.6V, I_{OUT} = 4A f = 120Hz, C_{OUT} = 25µF Tant., $(V_{IN} - V_{OUT})$ = 3V, I_{OUT} = 3A f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 6.3V, I_{OUT} = 3A f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 6.45V, I_{OUT} = 3A f = 120Hz, C_{OUT} = 25µF Tant., V_{IN} = 6.6V, I_{OUT} = 3A	 ●	 60	 72	 	 dB
Thermal Regulation	LT1584/5/7 LT1584/5/7-3.3 LT1584/5-3.38 LT1584/5/7-3.45 LT1584/5/7-3.6	T_A = 25°C, 30ms pulse T_A = 25°C, 30ms pulse T_A = 25°C, 30ms pulse T_A = 25°C, 30ms pulse T_A = 25°C, 30ms pulse	 	 	 0.004	 0.02	 %/W
Temperature Stability			●		0.5		%
Long-Term Stability		T_A = 125°C, 1000 Hrs.			0.03	1.0	%
RMS Output Noise (% of V_{OUT})		T_A = 25°C, 10Hz ≤ f ≤ 10kHz			0.003		%
Thermal Resistance Junction to Case	LT1584 LT1585 LT1585 LT1587 LT1587	T Package: Control Circuitry/Power Transistor T Package: Control Circuitry/Power Transistor M Package: Control Circuitry/Power Transistor T Package: Control Circuitry/Power Transistor M Package: Control Circuitry/Power Transistor	 	 	 	0.65/2.7 0.7/3.0 0.7/3.0 0.7/3.0 0.7/3.0	°C/W °C/W °C/W °C/W °C/W

The ● denotes specifications which apply over the specified operating temperature range.

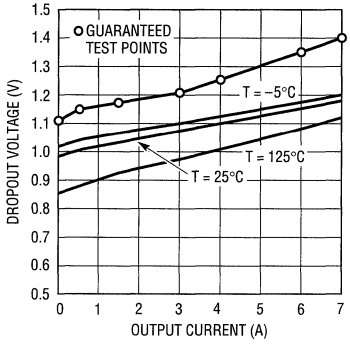
Note 1: See thermal regulation specifications for changes in output voltage due to heating effects. Load and line regulation are measured at a constant junction temperature by low duty cycle pulse testing.

Note 2: Line and load regulation are guaranteed up to the maximum power dissipation (25W for the LT1584 in T package, 26.5W for the LT1585 in T package, 18W for the LT1587 in T package). Power dissipation is determined by input/output differential and the output current. Guaranteed maximum output power will not be available over the full input/output voltage range.

Note 3: $I_{FULL\ LOAD}$ is defined as the maximum value of output load current as a function of input-to-output voltage. $I_{FULL\ LOAD}$ is equal to 7A for the LT1584, 4.6A at $T_J \ge 25°C$ and 4A at $T_J < 25°C$ for the LT1585/LT1585-3.3 and 3A for the LT1587. The remaining LT1585 fixed voltage versions are 4A. The LT1585 and LT1587 have constant current limit with changes in input-to-output voltage. The LT1584 has variable current limit which decreases about 4A as input-to-output voltage increases from 3V to 7V.

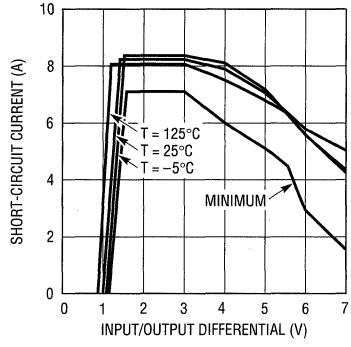
TYPICAL PERFORMANCE CHARACTERISTICS

LT1584 Dropout Voltage vs Output Current



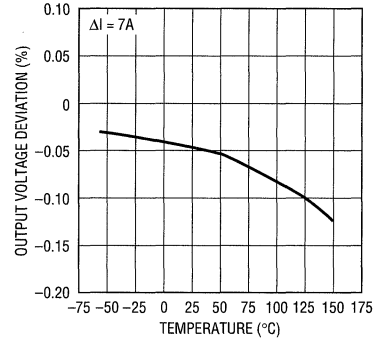
LTC1584 • TPC01

LT1584 Short-Circuit Current vs Input/Output Differential



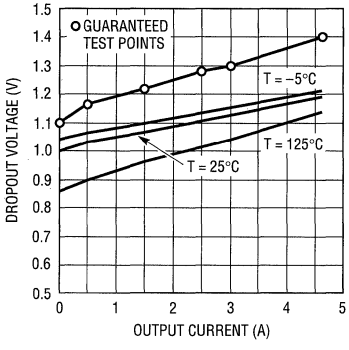
LT1584 • TPC02

LT1584 Load Regulation vs Temperature



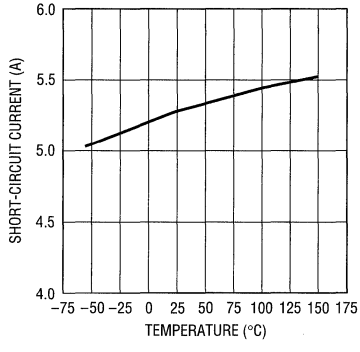
LT1584 • TPC03

LT1585 Dropout Voltage vs Output Current



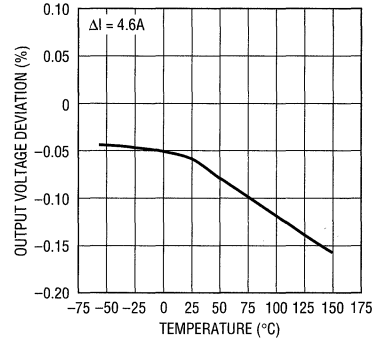
LT1585 • TPC04

LT1585 Short-Circuit Current vs Temperature



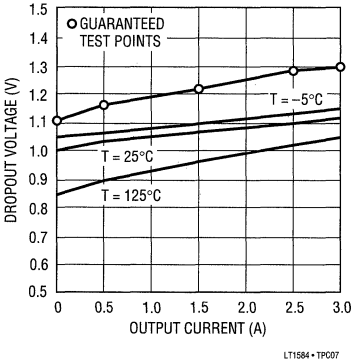
LT1584 • TPC05

LT1585 Load Regulation vs Temperature



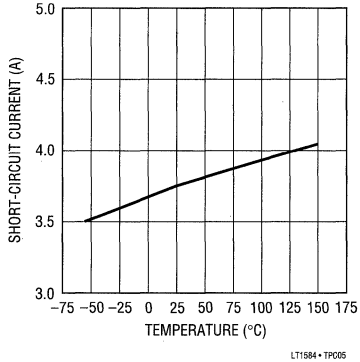
LT1584 • TPC03

LT1587 Dropout Voltage vs Output Current



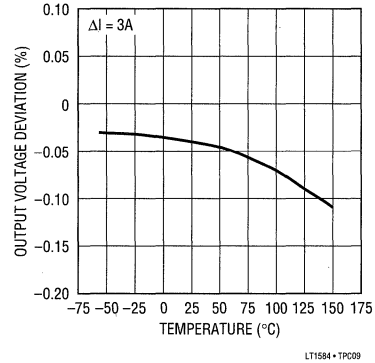
LT1584 • TPC07

LT1587 Short-Circuit Current vs Temperature



LT1584 • TPC05

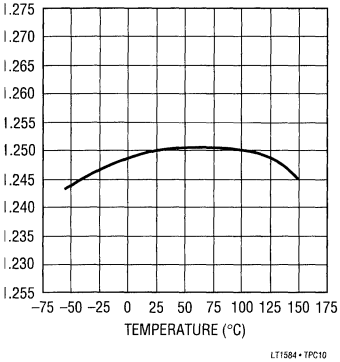
LT1587 Load Regulation vs Temperature



LT1584 • TPC09

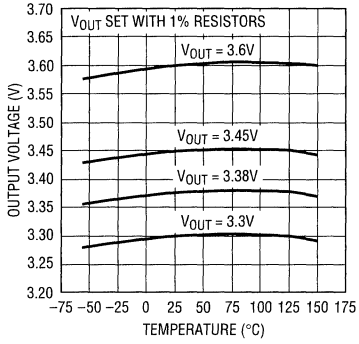
TYPICAL PERFORMANCE CHARACTERISTICS

LT1584/5/7 Reference Voltage vs Temperature



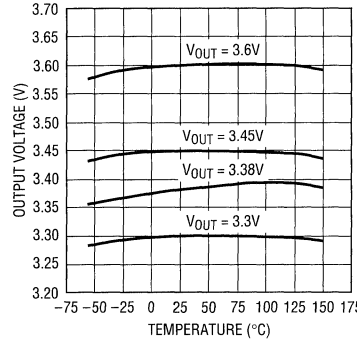
LT1584 • TPC10

Output Voltage vs Temperature Using Adjustable LT1584/5/7



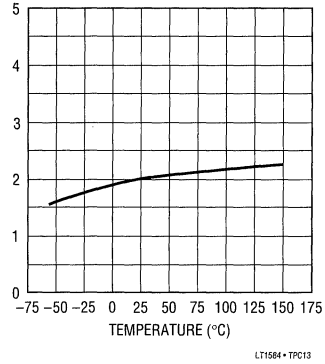
LT1584 • TPC11

LT1584/5/7-3.XX Output Voltage vs Temperature



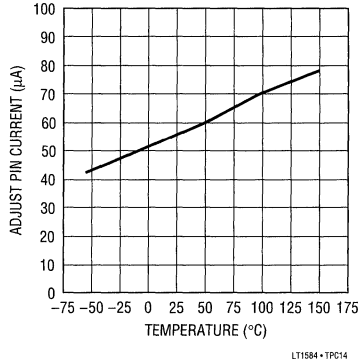
LT1584 • TPC12

LT1584/5/7 Minimum Load Current vs Temperature



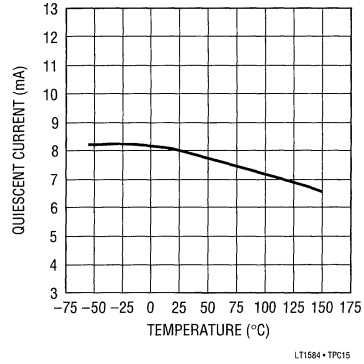
LT1584 • TPC13

LT1584/5/7 Adjust Pin Current vs Temperature



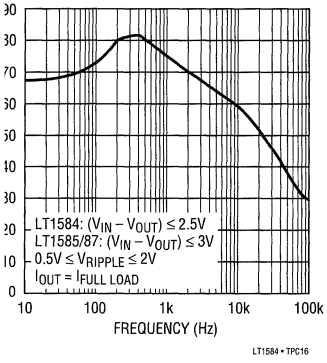
LT1584 • TPC14

LT1584/5/7-3.XX Quiescent Current vs Temperature



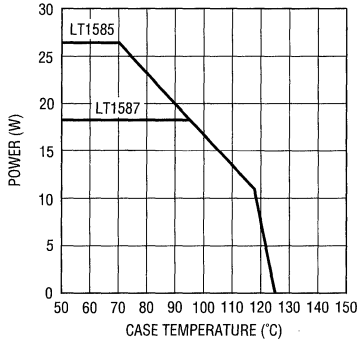
LT1584 • TPC15

LT1584/5/7 Ripple Rejection vs Frequency



LT1584 • TPC16

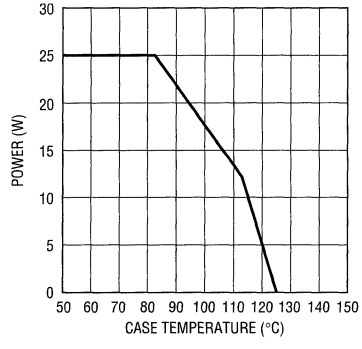
LT1585/7 Maximum Power Dissipation*



LT1584 • TPC17

*AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

LT1584 Maximum Power Dissipation*

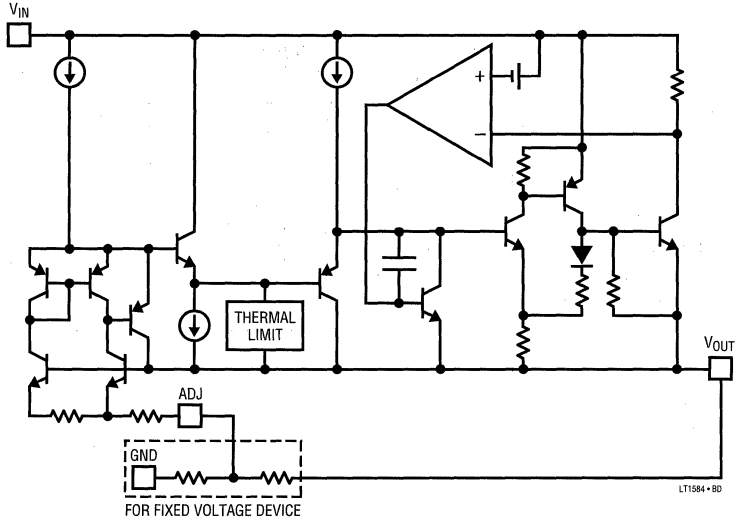


LT1584 • TPC18

*AS LIMITED BY MAXIMUM JUNCTION TEMPERATURE

4

SIMPLIFIED SCHEMATIC



APPLICATIONS INFORMATION

General

The LT1584/LT1585/LT1587 family of three-terminal regulators is easy to use and has all the protection features expected in high performance linear regulators. The devices are short-circuit protected, safe-area protected, and provide thermal shutdown to turn off the regulators should the junction temperature exceed about 150°C. The LT1584/LT1585/LT1587 family includes adjustable and fixed voltage versions.

These ICs are pin compatible with the LT1083/LT1084/LT1085 family of linear regulators but offer lower dropout voltage and faster transient response. The trade-off for this improved performance is a 7V maximum supply voltage. Similar to the LT1083/LT1084/LT1085 family, the LT1584/LT1585/LT1587 regulators require an output capacitor for stability. However, the improved frequency compensation permits the use of capacitors with much lower ESR while still maintaining stability. This is critical in addressing the needs of modern, low voltage, high speed microprocessors.

Current generation microprocessors cycle load current from almost zero to amps in tens of nanoseconds. Output voltage tolerances are tighter and include transient response as part of the specification. The LT1584/LT1585/LT1587 family is specifically designed to meet the fa current load-step requirements of these microprocesso and saves total cost by needing less output capacitance order to maintain regulation.

Stability

The circuit design in the LT1584/LT1585/LT1587 fami requires the use of an output capacitor as part of th frequency compensation. For all operating conditions, th addition of a 22µF solid tantalum or a 100µF aluminu electrolytic on the output ensures stability. Normally, th LT1584/LT1585/LT1587 can use smaller value capacitor Many different types of capacitors are available and ha widely varying characteristics. These capacitors differ capacitor tolerance (sometimes ranging up to ±100% equivalent series resistance, equivalent series inductanc and capacitance temperature coefficient. The LT158 LT1585/LT1587 frequency compensation optimizes fr quency response with low ESR capacitors. In general, us capacitors with an ESR of less than 1Ω.

On the adjustable LT1584/LT1585/LT1587, bypassing th adjust terminal improves ripple rejection and transie response. Bypassing the adjust pin increases the require output capacitor value. The value of 22µF tantalum

PPLICATIONS INFORMATION

0µF aluminum covers all cases of bypassing the adjust minal. With no adjust pin bypassing, smaller values of pacitors provide equally good results.

rmally, capacitor values on the order of several hundred crofarads are used on the output of the regulators to sure good transient response with heavy load current anges. Output capacitance can increase without limit d larger values of output capacitance further improve the bility and transient response of the LT1584/LT1585/ 1587 family.

rge load current changes are exactly the situation pre- nted by modern microprocessors. The load current step ntains higher order frequency components that the tput decoupling network must handle until the regulator ottles to the load current level. Capacitors are not ideal ments and contain parasitic resistance and inductance. ese parasitic elements dominate the change in output tage at the beginning of a transient load step change. e ESR of the output capacitors produces an instanta- ous step in output voltage ($\Delta V = \Delta I \times ESR$). The ESL of output capacitors produces a droop proportional to the e of change of output current ($V = L \times \Delta I/\Delta t$). The output pacitance produces a change in output voltage propor- nal to the time until the regulator can respond ($\Delta V = \Delta t$ $\Delta I/C$). These transient effects are illustrated in Figure 1.

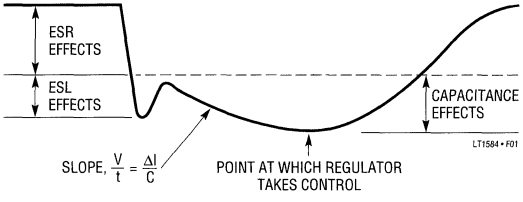


Figure 1

e use of capacitors with low ESR, low ESL, and good high quency characteristics is critical in meeting the output tage tolerances of these high speed microprocessors. ese requirements dictate a combination of high quality, face mount tantalum capacitors and ceramic capaci- s. The location of the decoupling network is critical to nsient response performance. Place the decoupling work as close as possible to the processor pins because ce runs from the decoupling capacitors to the processor s are inductive. The ideal location for the decoupling network is actually inside the microprocessor socket cavity. In addition, use large power and ground plane areas to minimize distribution drops.

A possible stability problem that occurs in monolithic linear regulators is current limit oscillations. The LT1585/LT1587 essentially have a flat current limit over the range of input supply voltage. The lower current limit rating and 7V maximum supply voltage rating for these devices permit this characteristic. Current limit oscillations are typically nonexistent, unless the input and output decoupling capacitors for the regulators are mounted several inches from the terminals. The LT1584 differs from the LT1585/ LT1587 and provides current limit foldback as input-to-output differential voltage increases. This safe-area characteristic exhibits a negative impedance because increasing voltage causes output current to decrease. Negative resistance during current limit is not unique to the LT1584 devices and is present on many power IC regulators. The value of the negative resistance is a function of how fast the current limit is folded back as input-to-output voltage increases. This negative resistance can react with capacitors and inductors on the input and output to cause oscillation during current limit. Depending on the values of series resistances, the overall system may end up unstable. However, the oscillation causes no problem and the IC remains protected. In general, if this problem occurs and is unacceptable, increasing the amount of output capacitance helps dampen the system.

Protection Diodes

In normal operation, the LT1584/LT1585/LT1587 family does not require any protection diodes. Older three-terminal regulators require protection diodes between the output pin and the input pin or between the adjust pin and the output pin to prevent die overstress.

On the adjustable LT1584/LT1585/LT1587, internal resistors limit internal current paths on the adjust pin. Therefore, even with bypass capacitors on the adjust pin, no protection diode is needed to ensure device safety under short-circuit conditions.

A protection diode between the input and output pins is usually not needed. An internal diode between the input and output pins on the LT1584/LT1585/LT1587 family can

APPLICATIONS INFORMATION

handle microsecond surge currents of 50A to 100A. Even with large value output capacitors it is difficult to obtain those values of surge currents in normal operation. Only with large values of output capacitance, such as 1000µF to 5000µF, and with the input pin instantaneously shorted to ground can damage occur. A crowbar circuit at the input of the LT1584/LT1585/LT1587 can generate those levels of current, and a diode from output to input is then recommended. This is shown in Figure 2. Usually, normal power supply cycling or system "hot plugging and unplugging" will not generate current large enough to do any damage.

The adjust pin can be driven on a transient basis ±7V with respect to the output, without any device degradation. As with any IC regulator, exceeding the maximum input-to-output voltage differential causes the internal transistors to break down and none of the protection circuitry is then functional.

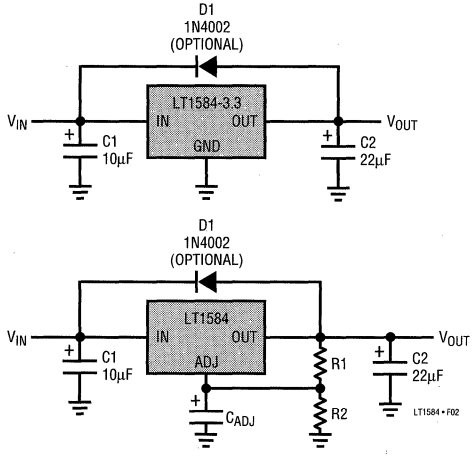


Figure 2

Overload Recovery

The LT1584 devices have safe-area protection similar to the LT1083/LT1084/LT1085. The safe-area protection decreases current limit as input-to-output voltage increases. This behavior keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The LT1584 protection circuitry provides some output current at all values of input-to-output voltage up to the 7V maximum supply voltage. When power is first applied, th input voltage rises and the output voltage follows the inpu The input-to-output voltage remains small and the regula tor can supply large output currents. This action permit the regulator to start-up into very heavy loads.

With higher input voltages, a problem can occur where th removal of an output short does not permit the outpu voltage to recover. This problem is not unique to th LT1584 devices and is present on the LT1083/LT1084 LT1085 family and older generation linear regulators. Th problem occurs with a heavy output load, a high inpu voltage, and a low output voltage. An example is immed ately after the removal of a short circuit. The load line c such a load may intersect the output current curve at tw points. If this happens, two stable output operating point exist for the regulator. With this double intersection, th power supply may require cycling down to zero and bac up again to make the output recover. This situation doe not occur with the LT1585/LT1587 because no foldbac circuitry is required to provide safe-area protection.

Ripple Rejection

The typical curve for ripple rejection reflects values for th LT1584/LT1585/LT1587 fixed output voltage parts be tween 3.3V and 3.6V. In applications that require improve ripple rejection, use the adjustable devices. A bypas capacitor from the adjust pin to ground reduces the outpu ripple by the ratio of V_{OUT}/1.25V. The impedance of th adjust pin capacitor at the ripple frequency should be les than the value of R1 (typically in the range of 100Ω t 120Ω) in the feedback divider network in Figure 2. There fore, the value of the required adjust pin capacitor is function of the input ripple frequency. For example, if R equals 100Ω and the ripple frequency equals 120Hz, th adjust pin capacitor should be 22µF. At 10kHz, only 0.22µ is needed.

Output Voltage

The LT1584/LT1585/LT1587 adjustable regulators develo a 1.25V reference voltage between the output pin and th adjust pin (see Figure 3). Placing a resistor R1 betwee these two terminals causes a constant current to flo through R1 and down through R2 to set the overall outpu voltage. Normally, this current is the specified minimur

PPLICATIONS INFORMATION

ıd current of 10mA. The current out of the adjust pin adds the current from R1 and is typically 55µA. Its output ltage contribution is small and only needs consideration ıen very precise output voltage setting is required.

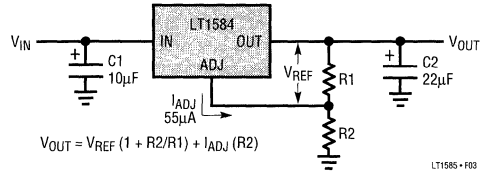


Figure 3. Basic Adjustable Regulator

ıad Regulation

is not possible to provide true remote load sensing cause the LT1584/LT1585/LT1587 are three-terminal vices. Load regulation is limited by the resistance of the re connecting the regulators to the load. Load regulation r the data sheet specification is measured at the bottom the package.

r fixed voltage devices, negative side sensing is a true lvin connection with the ground pin of the device re- ned to the negative side of the load. This is illustrated in jure 4.

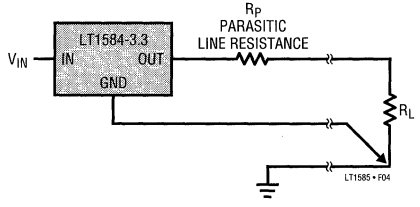


Figure 4. Connection for Best Load Regulation

r adjustable voltage devices, negative side sensing is a e Kelvin connection with the bottom of the output divider urned to the negative side of the load. The best load julation is obtained when the top of resistor divider R1 nnects directly to the regulator output and not to the ıd. Figure 5 illustrates this point. If R1 connects to the ıd, the effective resistance between the regulator and the ıd is:

× (1 + R2/R1), R_P = Parasitic Line Resistance

The connection shown in Figure 5 does not multiply R_P by the divider ratio. As an example, R_P is about four milliohms per foot with 16-gauge wire. This translates to 4mV per foot at 1A load current. At higher load currents, this drop represents a significant percentage of the overall regulation. It is important to keep the positive lead between the regulator and the load as short as possible and to use large wire or PC board traces.

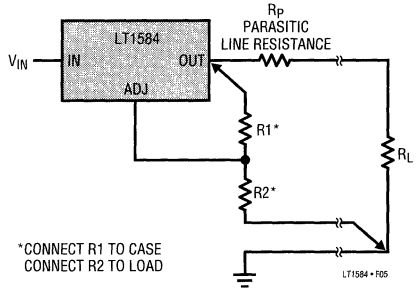


Figure 5. Connection for Best Load Regulation

Thermal Considerations

The LT1584/LT1585/LT1587 family protects the device under overload conditions with internal power and thermal limiting circuitry. However, for normal continuous load conditions, do not exceed maximum junction temperature ratings. It is important to consider all sources of thermal resistance from junction-to-ambient. These sources include the junction-to-case resistance, the case-to-heat sink interface resistance, and the heat sink resistance. Thermal resistance specifications have been developed to more accurately reflect device temperature and ensure safe operating temperatures. The electrical characteristics section provides a separate thermal resistance and maximum junction temperature for both the control circuitry and the power transistor. Older regulators, with a single junction-to-case thermal resistance specification, use an average of the two values provided here and allow excessive junction temperatures under certain conditions of ambient temperature and heat sink resistance. Calculate the maximum junction temperature for both sections to ensure that both thermal limits are met.

Junction-to-case thermal resistance is specified from the IC junction to the bottom of the case directly below the die.

4

APPLICATIONS INFORMATION

This is the lowest resistance path for heat flow. Proper mounting ensures the best thermal flow from this area of the package to the heat sink. Linear Technology strongly recommends thermal compound at the case-to-heat sink interface. Use a thermally conductive spacer if the case of the device must be electrically isolated and include its contribution to the total thermal resistance. Please consult "Mounting Considerations for Power Semiconductors" *1990 Linear Applications Handbook, Volume I*, Pages RR3-1 to RR3-20. The output connects to the case of all devices in the LT1584/LT1585/LT1587 series.

For example, using an LT1585CT-3.3 (TO-220, commercial) and assuming:

V_{IN}(Max Continuous) = 5.25V (5V + 5%), V_{OUT} = 3.3V, I_{OUT} = 4.6A

T_A = 70°C, $\theta_{HEAT\ SINK}$ = 4°C/W

$\theta_{CASE\text{-}TO\text{-}HEAT\ SINK}$ = 1°C/W (with Thermal Compound)

Power dissipation under these conditions is equal to:

$P_D = (V_{IN} - V_{OUT})(I_{OUT}) = (5.25 - 3.3)(4.6) = 9W$

Junction temperature will be equal to:

$T_J = T_A + P_D(\theta_{HEAT\ SINK} + \theta_{CASE\text{-}TO\text{-}HEAT\ SINK} + \theta_{JC})$

For the Control Section:

T_J = 70°C + 9W (4°C/W + 1°C/W + 0.7°C/W) = 121.3°C
121.3°C < 125°C = T_{JMAX} (Control Section Commercial range)

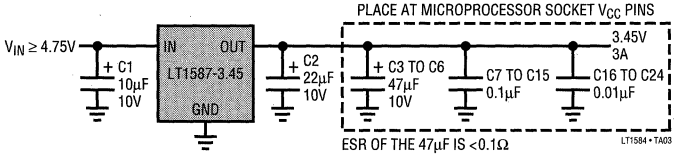
For the Power Transistor:

T_J = 70°C + 9W (4°C/W + 1°C/W + 3°C/W) = 142°C
142°C < 150°C = T_{JMAX} (Power Transistor Commercial Range)

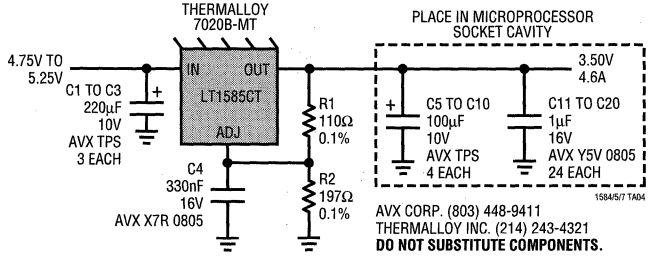
In both cases the junction temperature is below the maximum rating for the respective sections, ensuring reliable operation.

TYPICAL APPLICATIONS

Recommended LT1587-3.45 Circuit for the Intel 486™ DX4™ Overdrive Microprocessor

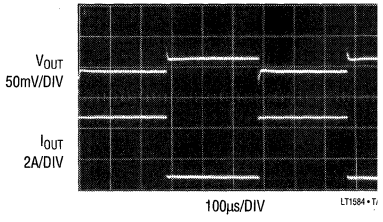


Minimum Parts Count LT1585 Adjustable Circuit for the Intel Pentium VRE Processor



AVX CORP. (803) 448-9411
THERMALLOY INC. (214) 243-4321
DO NOT SUBSTITUTE COMPONENTS.

LT1585 Transient Response for 3.8A Load Current Step*



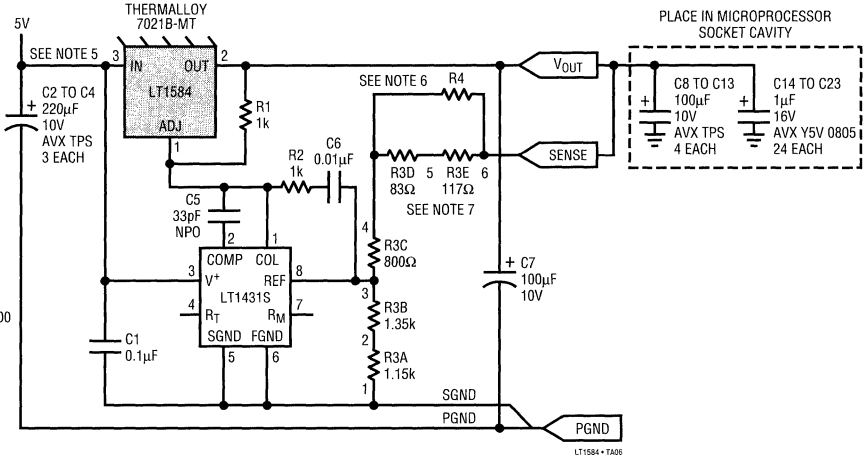
*TRANSIENT RESPONSE MEASURED WITH AN INTEL POWER VALIDATOR. V_{OUT} IS MEASURED AT THE POWER VALIDATOR

486 and DX4 are trademarks of Intel Corporation.

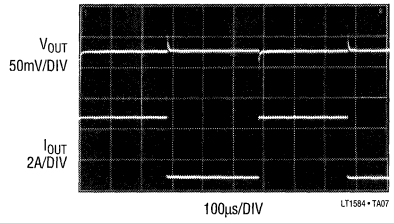
YPICAL APPLICATIONS

Guaranteed LT1584/LT1431 Circuit for the Intel 90MHz and 100MHz Pentium Processors (Meets Intel Specifications with Worst-Case Tolerances)

TES: UNLESS OTHERWISE SPECIFIED
ALL RESISTOR VALUES ARE OHMS, 1/8W, 5%
ALL CAPACITORS ARE 50V, 20%
ALL POLARIZED CAPACITORS ARE AVX TYPE TPS OR EQUIVALENT
NPUT CAPACITANCE MAY BE REDUCED F THE 5V SUPPLY IS WELL BYPASSED
OR 100MHz PENTIUM PROCESSOR, NPUT VOLTAGE MUST BE AT LEAST 4.85V AT THE REGULATOR INPUT
OR PENTIUM VRE PROCESSOR, 34 NOT INSTALLED
- FOR 3.3V OUTPUT, INSTALL 0Ω JUMPER RESISTOR R4
R3A TO R3E ARE B.I. TECHNOLOGY 627V100



LT1584/LT1431 Transient Response for 3.8A Load Current Step*



*TRANSIENT RESPONSE MEASURED WITH AN INTEL POWER VALIDATOR. V_{OUT} IS MEASURED AT THE POWER VALIDATOR

4

ELATED PARTS

RT NUMBER	DESCRIPTION	COMMENTS
083/84/85	7.5A, 5A, 3A Low Dropout Linear Regulators	Fixed Output at 3.3V, 3.6V, 5V and 12V, V_{IN} to 25V
083/84/85	7.5A, 5A, 3A Low Dropout Linear Regulators	Adjustable Output with up to 30V ($V_{IN} - V_{OUT}$) Differential
086	1.5A Low Dropout Linear Regulator	Both Fixed and Adjustable Versions, ($V_{IN} - V_{OUT}$) to 30V
521	300mA Low Dropout Linear Regulator with 12µA Quiescent Current and Shutdown	Both Fixed and Adjustable Versions, Surface Mount Package Available
529	3A Low Dropout Linear Regulator with 50µA Quiescent Current and Shutdown	Both Fixed and Adjustable Versions, Surface Mount Package Available
580	7A Very Low Dropout Linear Regulator	540mV Dropout at 7A, Remote Sensing

ECTION 4—POWER PRODUCTS

1MHz Off-Line Current Mode PWM and DC/DC Converter

FEATURES

- **Current Mode Operation to 1MHz**
- **30ns Current Sense Delay**
- < 250μA Low Start-Up Current
- **Current Sense Leading Edge Blanking**
- Pin Compatible with UC1842
- Undervoltage Lockout with Hysteresis
- No Cross-Conduction Current
- Trimmed Bandgap Reference
- 1A Totem Pole Output
- Trimmed Oscillator Frequency and Sink Current
- Active Pull-Down on Reference and Output During Undervoltage Lockout
- 18V High Level Output Clamp

APPLICATIONS

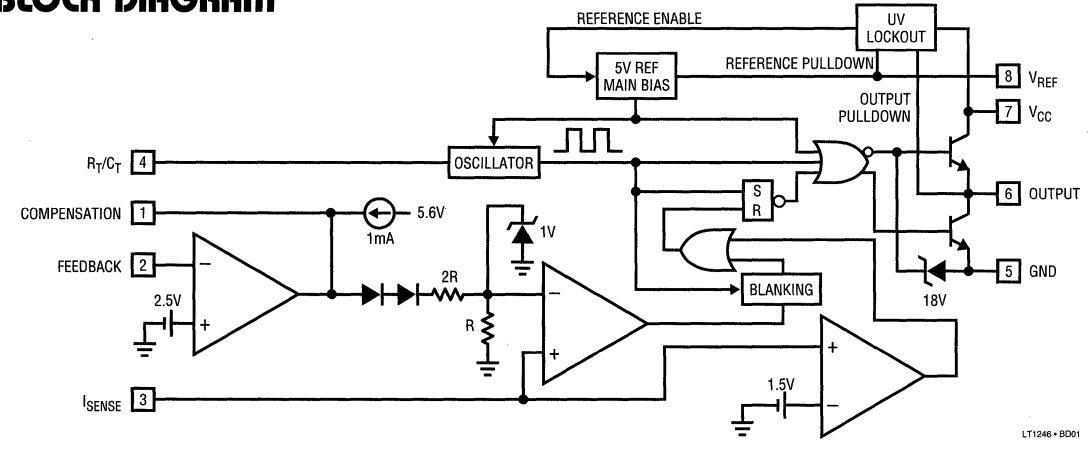
- Off-Line Converters
- DC/DC Converters

Device	Start-Up Threshold	Minimum Operating Voltage	Maximum Duty Cycle	Replaces
LT1246	16V	10V	100%	UC1842
LT1247	8.4V	7.6V	100%	UC1843

DESCRIPTION

The LT®1246/LT1247 are 8-pin, fixed frequency, current mode, pulse width modulators. These devices are designed to be improved plug compatible versions of the industry standard UC1842 PWM circuit. The LT1246/LT1247 are optimized for off-line and DC/DC converter applications. They contain a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output stage ideally suited to driving power MOSFETs. Start-up current has been reduced to less than 250μA. Cross-conduction current spikes in the totem pole output stage have been eliminated, making 1MHz operation practical. Several new features have been incorporated. Leading edge blanking has been added to the current sense comparator. This minimizes or eliminates the filter that is normally required. Eliminating this filter allows the current sense loop to operate with minimum delays. Trims have been added to the oscillator circuit for both frequency and sink current and both of these parameters are tightly specified. The output stage is clamped to a maximum V_{OUT} of 18V in the on state. The output and the reference output are actively pulled low during under-voltage lockout.

BLOCK DIAGRAM

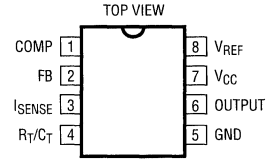


ABSOLUTE MAXIMUM RATINGS

Supply Voltage 25V
Output Current ..... ±1A*
Output Energy (Capacitive Load per Cycle) 5µJ
Analog Inputs (Pins 2, 3) ..... –0.3 to 6V
Error Amplifier Output Sink Current 10mA
Power Dissipation at $T_A \leq 25°C$ 1W
Operating Junction Temperature Range
LT1246C/LT1247C ..... 0°C to 100°C
Storage Temperature Range ..... – 65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

*The 1A rating for output current is based on transient switching requirements.

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 100°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LT1246CN8 LT1246CS8 LT1247CN8 LT1247CS8
S8 PART MARKING
1246 1247

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS (Notes 1, 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Section						
Output Voltage	I_O = 1mA, T_J = 25°C		4.925	5.000	5.075	V
Line Regulation	12V < V_{CC} < 25V	●		3	20	mV
Load Regulation	1mA < I_{REF} < 20mA	●		–6	–25	mV
Temperature Stability				0.1		mV/°C
Total Output Variation	Line, Load, Temperature	●	4.87		5.13	V
Output Noise Voltage	10Hz < F < 10kHz, T_J = 25°C			50		µV
Long-Term Stability	T_A = 125°C, 1000 Hrs.			5	25	mV
Output Short-Circuit Current		●	–30	–90	–180	mA
Oscillator Section						
Initial Accuracy	R_T = 10k, C_T = 3.3nF, T_J = 25°C R_T = 6.2k, C_T = 500pF, T_J = 25°C		47.5 465	50 500	52.5 535	kHz kHz
Voltage Stability	12V < V_{CC} < 25V, T_J = 25°C				1	%
Temperature Stability	T_{MIN} < T_J < T_{MAX}			–0.05		%/°C
Amplitude	Pin 4			1.7		V
Clock Ramp Reset Current	V_{OSC} (Pin 4) = 2V, T_J = 25°C		7.9	8.2	8.5	mA
Error Amplifier Section						
Feedback Pin Input Voltage	$V_{PIN\ 1}$ = 2.5V	●	2.42	2.50	2.58	V
Input Bias Current	V_{FB} = 2.5V	●			–2	µA
Open-Loop Voltage Gain	2 < V_O < 4V	●	65	90		dB
Unity-Gain Bandwidth	T_J = 25°C		1	2		MHz
Power Supply Rejection Ratio	12V < V_{CC} < 25V	●	60			dB
Output Sink Current	$V_{PIN\ 2}$ = 2.7V, $V_{PIN\ 1}$ = 1.1V	●	2	6		mA
Output Source Current	$V_{PIN\ 2}$ = 2.3V, $V_{PIN\ 1}$ = 5V	●	–0.5	–0.75		mA

ELECTRICAL CHARACTERISTICS (Notes 1, 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier Section						
Output Voltage High Level	$V_{PIN\ 2}$ = 2.3V, R_L = 15k to GND	●	5	5.6		V
Output Voltage Low Level	$V_{PIN\ 2}$ = 2.7V, R_L = 15k to Pin 8	●		0.2	1.1	V
Current Sense Section						
Gain		●	2.85	3.00	3.15	V/V
Maximum Current Sense Input Threshold	$V_{PIN\ 3}$ < 1.1V	●	0.90	1.00	1.10	V
Power Supply Rejection Ratio				70		dB
Input Bias Current		●		–1	–10	µA
Delay to Output				30		ns
Blanking Time				60		ns
Blanking Override Voltage				1.5		V
Output Section						
Output Low Level	I_{OUT} = 20mA I_{OUT} = 200mA	● ●		0.25 0.75	0.4 2.2	V V
Output High Level	I_{OUT} = 20mA I_{OUT} = 200mA	● ●	12.0 11.75			V V
Rise Time	C_L = 1nF, T_J = 25°C			30	70	ns
Fall Time	C_L = 1nF, T_J = 25°C			20	60	ns
Output Clamp Voltage	I_O = 1mA	●		18	19	V
Undervoltage Lockout						
Start-Up Threshold	LT1246 LT1247	● ●	15 7.8	16 8.4	17 9.0	V V
Minimum Operating Voltage	LT1246 LT1247	● ●	9.0 7.0	10 7.6	11 8.2	V V
Hysteresis	LT1246 LT1247	● ●	5.5 0.4	6.0 0.8		V V
PWM						
Maximum Duty Cycle	T_J = 25°C		94		100	%
Minimum Duty Cycle	T_J = 25°C			0		%
Total Device						
Start-Up Current		●		170	250	µA
Operating Current		●		13	20	mA

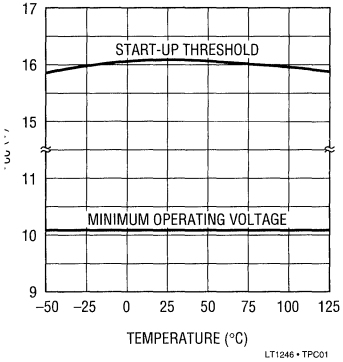
The ● denotes those specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified, V_{CC} = 15V, R_T = 10k, C_T = 3.3nF.

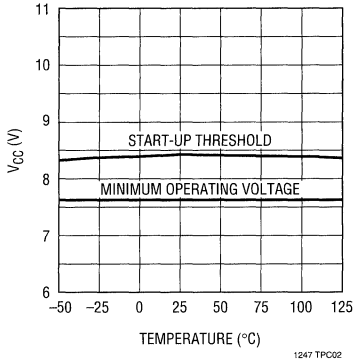
Note 2: Low duty cycle pulse techniques are used during test to maintain junction temperature close to ambient.

TYPICAL PERFORMANCE CHARACTERISTICS

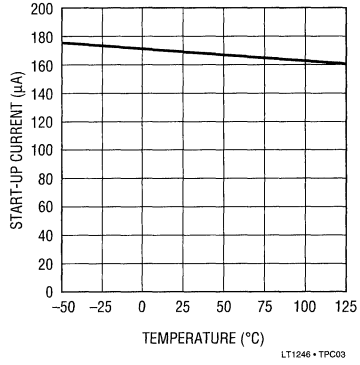
LT1246 Undervoltage Lockout



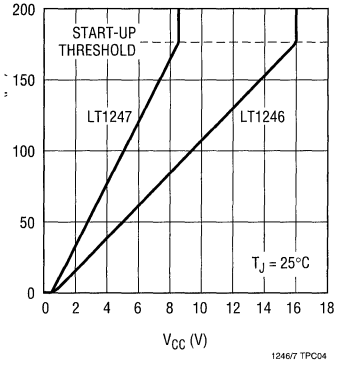
LT1247 Undervoltage Lockout



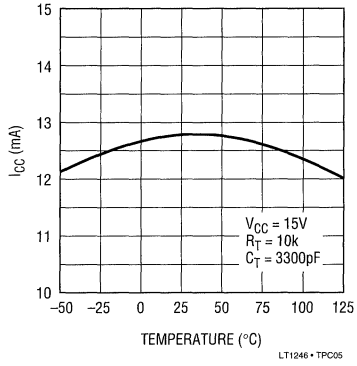
Start-Up Current



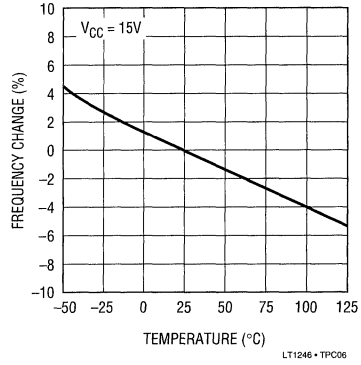
Start-Up Current



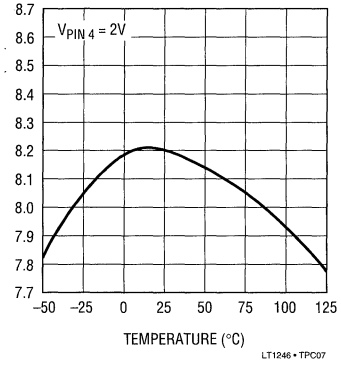
Supply Current



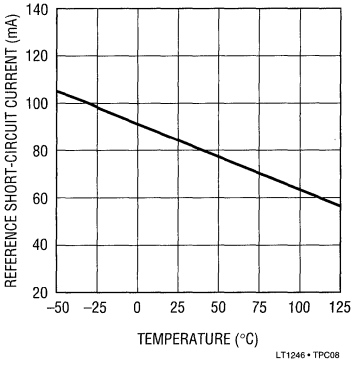
Oscillator Frequency



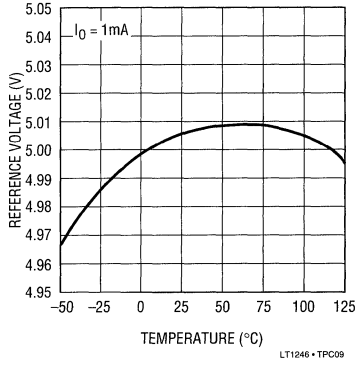
Oscillator Sink Current



Reference Short-Circuit Current



Reference Voltage



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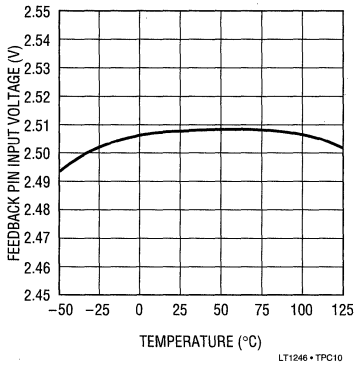
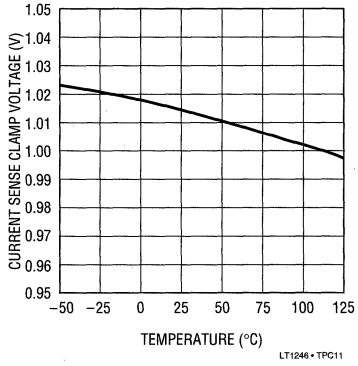
TYPICAL PERFORMANCE CHARACTERISTICS

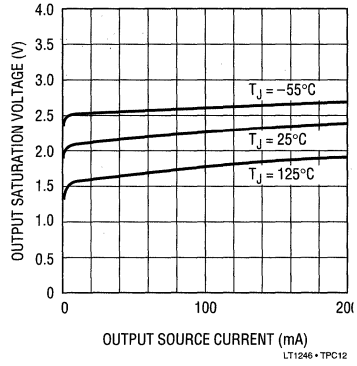
Feedback Pin Input Voltage



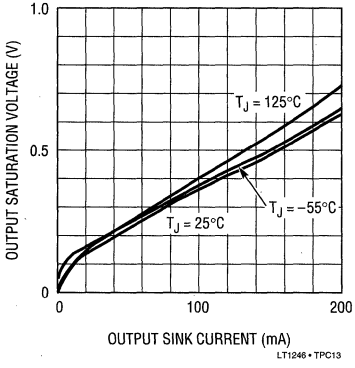
Current Sense Clamp Voltage



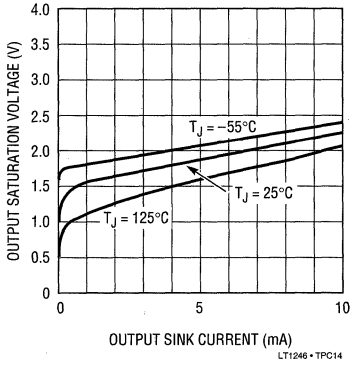
High Level Output Saturation Voltage



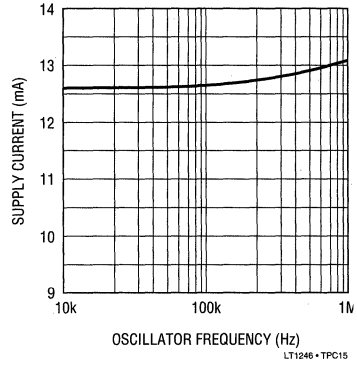
Low Level Output Saturation Voltage



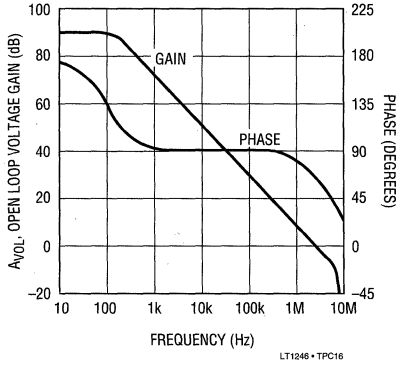
Low Level Output Saturation Voltage During Undervoltage Lockout



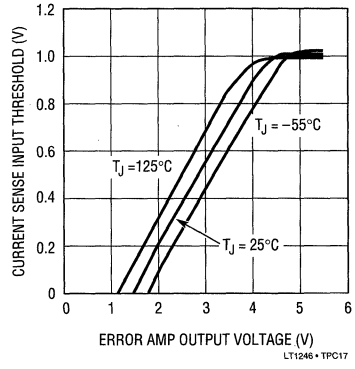
Supply Current vs Oscillator Frequency



Error Amplifier Open-Loop Gain and Phase

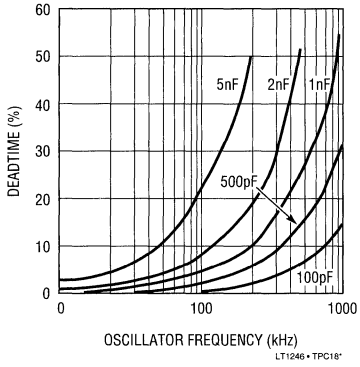


Current Sense Input Threshold

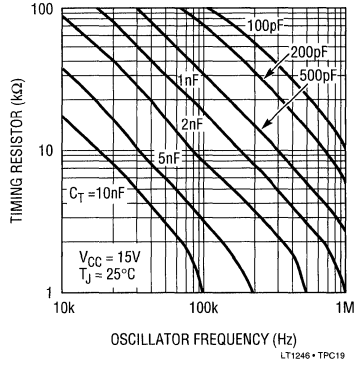


TYPICAL PERFORMANCE CHARACTERISTICS

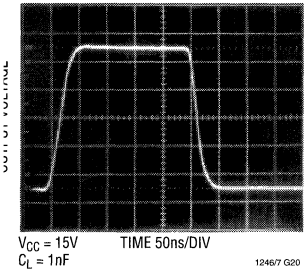
Output Deadtime vs Oscillator Frequency



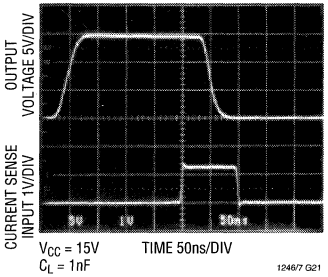
Timing Resistor vs Oscillator Frequency



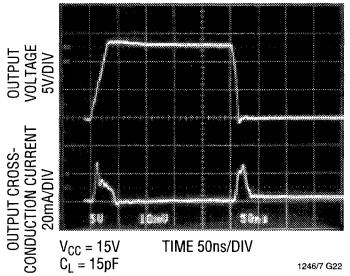
Output Rise and Fall Time



Current Sense Delay



Output Cross-Conduction



4

PIN FUNCTIONS

COMP (Pin 1): Compensation Pin. This pin is the output of the Error Amplifier and is made available for loop compensation. It can also be used to adjust the maximum value of the current sense clamp voltage to less than 1V. This pin can source a minimum of 0.5mA (0.8mA typ.) and sink a minimum of 2mA (4mA typ.)

FB (Pin 2): Voltage Feedback. This pin is the inverting input of the Error Amplifier. The output voltage is normally fed back to this pin through a resistive divider. The noninverting input of the Error Amplifier is internally committed to a 2.5V reference point.

I_{SENSE} (Pin 3): Current Sense. This is the input to the current sense comparator. The trip point of the comparator is set by, and is proportional to, the output voltage of the Error Amplifier.

R_T/C_T (Pin 4) : The oscillator frequency and the deadtime are set by connecting a resistor (R_T) from V_{REF} to R_T/C_T and a capacitor (C_T) from R_T/C_T to GND.

The rise time of the oscillator waveform is set by the RC time constant of R_T and C_T. The fall time, which is equal to the output deadtime, is set by a combination of the RC time constant and the oscillator sink current (8.2mA typ.).

PIN FUNCTIONS

GND (Pin 5): Ground.

OUTPUT (Pin 6): Current Output. This pin is the output of a high current totem pole output stage. It is capable of driving up to ±1A of current into a capacitive load such as the gate of a MOSFET.

V_{CC} (Pin 7): Supply Voltage. This pin is the positive supply of the control IC.

V_{REF} (Pin 8): Reference. This is the reference output of the IC. The reference output is used to supply charging current to the external timing resistor R_T. The reference provides biasing to a large portion of the internal circuitry, and is used to generate several internal reference levels including the V_{FB} level and the current sense clamp voltage.

APPLICATIONS INFORMATION

Device	Start-Up Threshold	Minimum Operating Voltage	Maximum Duty Cycle	Replaces
LT1246	16V	10V	100%	UC1842
LT1247	8.4V	7.6V	100%	UC1843

Oscillator

The LT1246/LT1247 are fixed frequency current mode pulse width modulators. The oscillator frequency and the oscillator discharge current are both trimmed and tightly specified to minimize the variations in frequency and deadtime. The oscillator frequency is set by choosing a resistor and capacitor combination, R_T and C_T. This RC combination will determine both the frequency and the maximum duty cycle. The resistor R_T is connected from V_{REF} (pin 8) to the R_T/C_T pin (pin 4). The capacitor C_T is connected from the R_T/C_T pin to ground. The charging current for C_T is determined by the value of R_T. The discharge current for C_T is set by the difference between the current supplied by R_T and the discharge current of the LT1246/LT1247. The discharge current of the device is trimmed to 8.2mA. For large values of R_T discharge time will be determined by the discharge current of the device and the value of C_T. As the value of R_T is reduced it will have more effect on the discharge time of C_T. During an oscillator cycle capacitor C_T is charged to approximately 2.8V and discharged to approximately 1.1V. The output is enabled during the charge time of C_T and disabled, in an off state, during the discharge time of C_T. The deadtime of the circuit is equal to the discharge time of C_T. The maximum duty cycle is limited by controlling the deadtime of the oscillator. There are many combinations of R_T and C_T that will yield a given oscillator frequency, however there is only one combination that will yield a specific deadtime at that frequency. Curves of oscillator frequency and deadtime for various values of R_T and C_T appear in the Typical Performance Characteristics section. Frequency and deadtime can also be calculated using the following formulas:

Oscillator Rise Time: $t_r = 0.583 \bullet RC$

Oscillator Discharge Time: $t_d = \dfrac{3.46 \bullet RC}{0.0164R - 11.73}$

Oscillator Period: $t_{OSC} = t_r + t_d$

Oscillator Frequency: $f_{OSC} = \dfrac{1}{t_{OSC}}$

Maximum Duty Cycle: $D_{MAX} = \dfrac{t_r}{t_{OSC}} = \dfrac{t_{OSC} - t_d}{t_{OSC}}$

The above formulas will give values that will be accurate to approximately ±5%, at the oscillator, over the full operating frequency range. This is due to the fact that the oscillator trip levels are constant versus frequency and the discharge current and initial oscillator frequency are trimmed. Some fine adjustment may be required to achieve more accurate results. Once the final R_T/C_T combination is selected, the oscillator characteristics will be repeatable from device to device. Note that there will be some slight differences between maximum duty cycle at the oscillator and maximum duty cycle at the output due to the finite rise and fall times of the output.

Error Amplifier

The LT1246/LT1247 contain a fully compensated error amplifier with a DC gain of 90dB and a unity-gain frequency of 2MHz. Phase margin at unity-gain is 80°. The noninverting input is internally committed to a 2.5V reference point derived from the 5V reference of pin 8. The

APPLICATIONS INFORMATION

nverting input (pin 2) and the output (pin 1) are made ıvailable to the user. The output voltage in a regulator :ircuit is normally fed back to the inverting input of the :rror amplifier through a resistive divider. The output of he error amplifier is made available for external loop :ompensation. The output current of the error amplifier is imited to approximately 0.8mA sourcing and approxi-nately 6mA sinking.

n a current mode PWM the peak switch current is a unction of the output voltage of the error amplifier. In the .T1246/LT1247 the output of the error amplifier is offset)y two diodes (1.4V at 25°C), divided by a factor of three, ınd fed to the inverting input of the current sense com-)arator. For output voltages less than 1.4V the duty cycle)f the output stage will be zero. The maximum offset that :an appear at the current sense input is limited by a 1V :lamp. This occurs when the error amplifier output reaches).4V at 25°C. The output of the error amplifier can be :lamped below 4.4V in order to reduce the maximum 'oltage allowed across the current sensing resistor to less han 1V. The supply current will increase by the value of he output source current when the output voltage of the :rror amplifier is clamped.

:urrent Sense Comparator and PWM Latch

.T1246/LT1247 are current mode controllers. Under nor-nal operating conditions the output (pin 6) is turned on at he start of every oscillator cycle, coincident with the rising dge of the oscillator waveform. The output is then turned)ff when the switch current reaches a threshold level)roportional to the error voltage at the output of the error mplifier. Once the output is turned off it is latched off until he start of the next cycle. The peak switch current is thus)roportional to the error voltage and is controlled on a ycle by cycle basis. The peak switch current is normally ensed by placing a sense resistor in the source lead of the utput MOSFET. This resistor converts the switch current) a voltage that can be fed into the current sense input. For ormal operating conditions the peak inductor current, /hich is equal to the peak switch current, will be equal to:

$$I_{PK} = \frac{\left(V_{PIN1} - 1.4V\right)}{\left(3R_S\right)}$$

During fault conditions the maximum threshold voltage at the input of the current sense comparator is limited by the internal 1V clamp at the inverting input. The peak switch current will be equal to:

$$I_{PK(MAX)} = \frac{1.0V}{R_S}$$

In certain applications such as high power regulators it may be desirable to limit the maximum threshold voltage to less than 1V in order to limit the power dissipated in the sense resistor or to limit the short-circuit current of the regulator circuit. This can be accomplished by clamping the output of the error amplifier. A voltage level of approximately 1.4V at the error amplifier output will give a threshold voltage of 0V. A voltage level of approximately 4.4V at the output of the error amplifier will give a threshold level of 1V. Between 1.4V and 4.4V the threshold voltage will change by a factor of one third of the change in the error amplifier output voltage. The threshold voltage will be 0.333V for an error amplifier voltage of 2.4V. To reduce the maximum current sense threshold to less than 1V the error amplifier output should be clamped to less than 4.4V.

4

Blanking

A unique feature of the LT1246/LT1247 is the built-in blanking circuit at the output of the current sense comparator. A common problem with current mode PWM circuits is erratic operation due to noise at the current sense input. The primary cause of noise problems is the leading edge current spike due to transformer interwinding capacitance and diode reverse recovery time. This current spike can prematurely trip the current sense comparator causing an instability in the regulator circuit. A filter at the current sense input is normally required to eliminate this instability. This filter will in turn slow down the current sense loop. A slow current sense loop wil increase the minimum pulse width which will increase the short-circuit current in an overload condition. The LT1246/LT1247 blank (lock out) the signal at the output of the current sense comparator for a fixed amount of time after the switch is turned on. This prevents the PWM latch from tripping due to the leading edge current spike. The blanking time will be a function of the voltage at the feedback pin (pin 2). The blanking time will be 60ns for normal operat-

APPLICATIONS INFORMATION

ing conditions (V_{FB} = 2.5V). The blanking time goes to zero as the feedback pin is pulled to 0V. This means that the blanking time will be minimized during start-up and also during an output short-circuit fault. This blanking circuit eliminates the need for an input filter at the current sense input except in extreme cases. Eliminating the filter allows the current sense loop to operate with minimum delays, reducing peak currents during fault conditions.

Undervoltage Lockout

The LT1246/LT1247 incorporate an undervoltage lockout comparator which prevents the internal reference circuitry and the output from starting up until the supply voltage reaches the start-up threshold voltage. The quiescent current, below the start-up threshold, has been reduced to less than 250μA (170μA typ.). This minimizes the power loss due to the start-up resistor used in off-line converters. In undervoltage lockout both V_{REF} (pin 8) and the Output (pin 6) are actively pulled low by Darlington connected PNP transistors. They are designed to sink a few milliamps of current and will pull down to about 1V. The pull-down transistor at the reference pin can be used to reset the external soft start capacitor. The pull-down transistor at the output eliminates the external pull-down resistor required, with earlier devices, to hold the external MOSFET gate low during undervoltage lockout.

Output

The LT1246/LT1247 incorporate a single high current totem pole output stage. This output stage is capable of driving up to ±1A of output current. Cross-conduction current spikes in the output totem pole have been eliminated. These devices are primarily intended for driving MOSFET switches. Rise time is typically 30ns and fall time is typically 20ns when driving a 1.0nF load. A clamp is built into the device to prevent the output from rising above 18V in order to protect the gate of the MOSFET switch. The output is actively pulled low during undervoltage lockout by a Darlington PNP. This PNP is designed to sink several milliamps and will pull the output down to approximately 1V. This active pull-down eliminates the need for the external resistor which was required in older designs.

The output pin of the device connects directly to the emitter of the upper NPN drive transistor and the collector of the lower NPN drive transistor in the totem pole. The collector of the lower transistor, which is n-type silicon, forms a p-n junction with the substrate of the device. The substate of the device is tied to ground. This junction is reverse biased during normal operation. In some applications the parasitic LC of the external MOSFET gate can ring and pull the output pin below ground. If the output pin is pulled negative by more than a diode drop, the parasitic diode formed by the collector of the output NPN and the substrate will turn on. This can cause erratic operation of the device. In these cases a Schottky clamp diode is recommended from output to ground.

Reference

The internal reference of the LT1246/LT1247 is a 5V Bandgap reference, trimmed to within ±1% initial tolerance. The reference is used to power the majority of the internal logic and the oscillator circuitry. The oscillator charging current is supplied from the reference. The feedback pin voltage and the clamp level for the current sense comparator are derived from the reference voltage. The reference can supply up to 20mA of current to power external circuitry. Note that using the reference in this manner, as a voltage regulator, will significantly increase the power dissipation in the device, which will reduce the operating ambient temperature range.

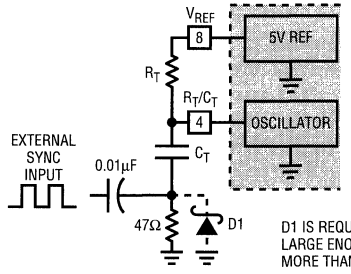
Design/Layout Considerations

LT1246/LT1247 are high speed circuits capable of generating pulsed output drive currents of up to 1A peak. The rise and fall time for the output drive current is in the range of 10ns to 20ns. High Speed circuit layout techniques must be used to insure proper operation of the devices. **Do not attempt to use Proto-boards or wire-wrap techniques to breadboard high speed switching regulator circuits. They will not work properly.**

Printed circuit layouts should include separate ground paths for the voltage feedback network, oscillator capacitor, and switch drive current. These ground paths should be connected together directly at the ground pin (pin 5) of the LT1246/LT1247. This will minimize noise problems due to pulsed ground pin currents. V_{CC} should be bypassed, with a minimum of 0.1μF, as close to the device as possible. High current paths should be kept short and they should be separated from the feedback voltage network with shield traces if possible.

TYPICAL APPLICATIONS

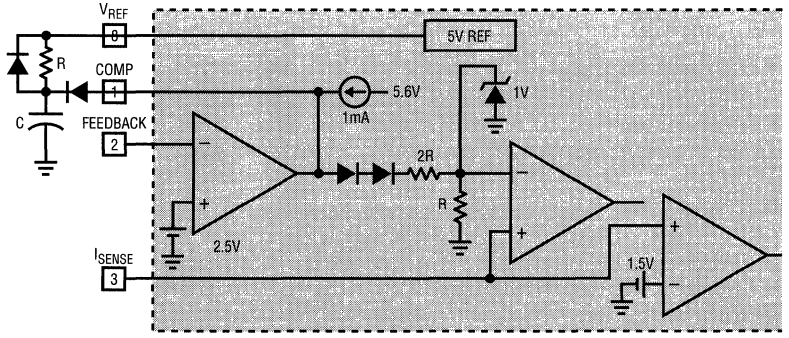
External Clock Synchronization



D1 IS REQUIRED IF THE SYNC AMPLITUDE IS LARGE ENOUGH TO PULL THE BOTTOM OF C_T MORE THAN 300mV BELOW GROUND.

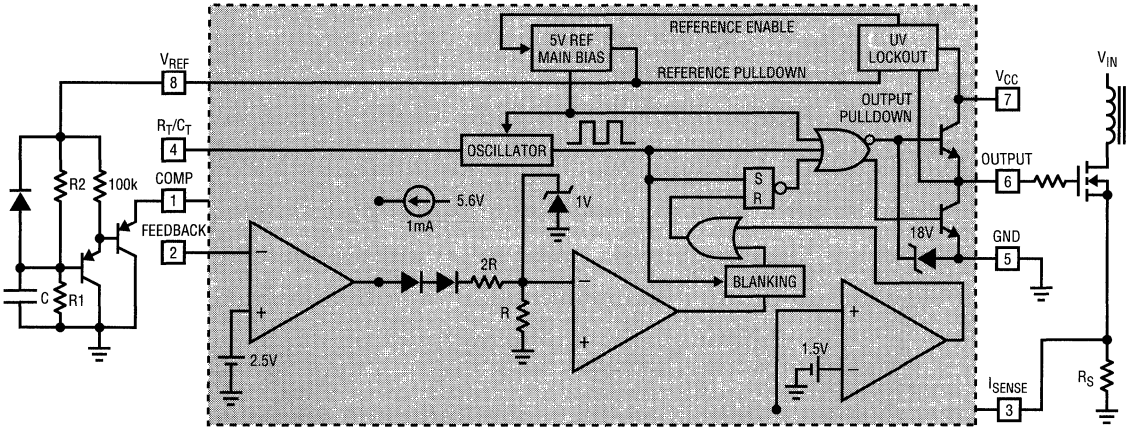
LT1246 • TA05

Soft Start



LT1246 • TA06

Adjustable Clamp Level with Soft Start

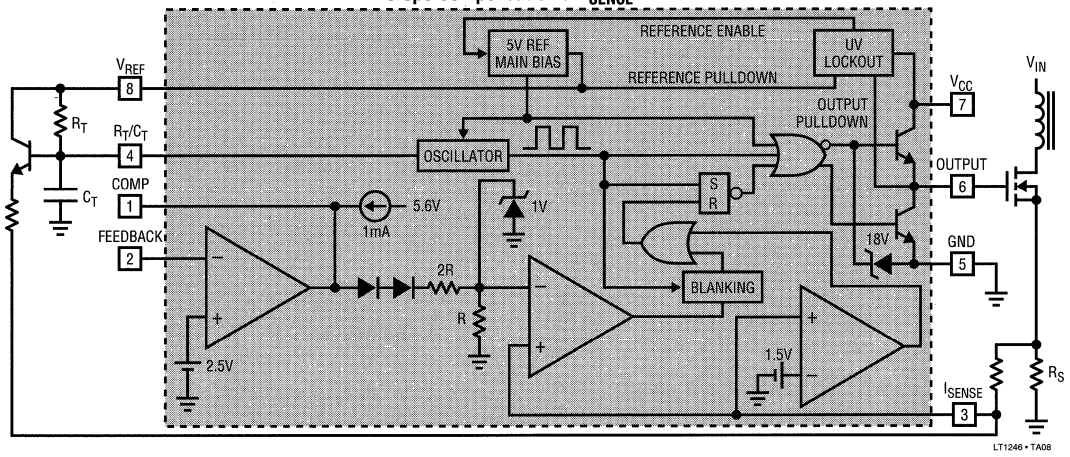


$$V_{CLAMP} \approx \frac{1.67}{\left(\frac{R2}{R1} + 1\right)} \qquad I_{PK\,(MAX)} \approx \frac{V_{CLAMP}}{R_S} \qquad \text{WHERE: } 0 \le V_{CLAMP} \le 1.0V \qquad t_{SOFT\,START} = -\ln\left[1 - \frac{V_C}{3 \bullet V_{CLAMP}}\right] C \frac{R1\,R2}{R1 + R2}$$

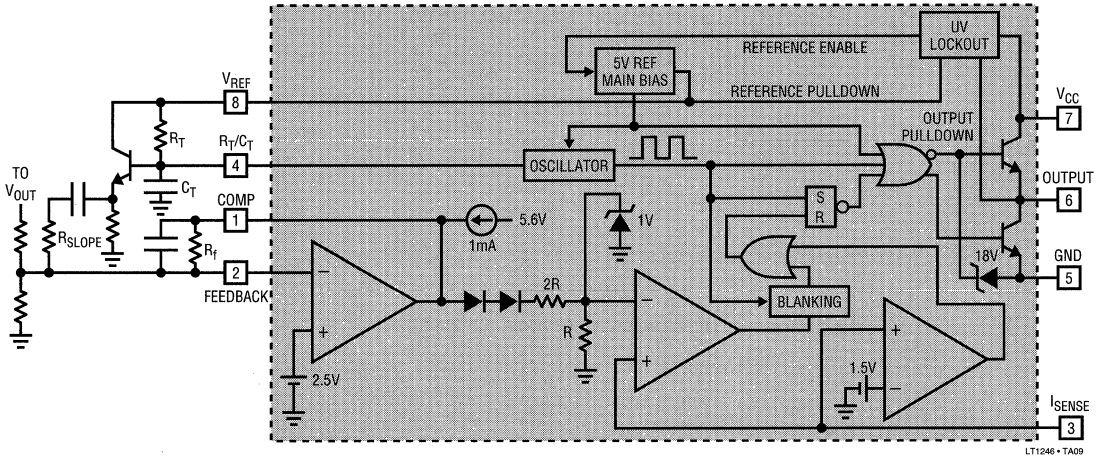
LT1246 • TA07

TYPICAL APPLICATIONS

Slope Compensation at I_{SENSE} Pin



Slope Compensation at Error Amp



RELATED PARTS

PART NUMBER	DESCRIPTION
LT1105	Off-Line Switching Regulator Controller
LT1170/LT1171/LT1172	High Efficiency 100kHz Switching Regulators
LT1241-5	500kHz Low Power Current Mode Pulse Width Modulator
LT1248/LT1249	Power Factor Controllers
LT1372	High Efficiency 500kHz Boost Switching Regulator
LT1376	1.5A, 500kHz Step-Down Switching Regulator
LT1377	1MHz High Efficiency Boost Switching Regulator
LT1431	Programmable Reference

3.3V High Efficiency Step-Down Switching Regulator Controller

FEATURES

- Accurate Preset 3.3V Output
- Up to 87% Efficiency
- Optional Burst Mode™ Operation for Light Loads
- Can Be Used with Many LTC Switching ICs
- **Accurate Ultra-Low-Loss Current Limit**
- **Operates with Inputs from 4.5V to 30V**
- **Shutdown Mode Draws Only 15µA**
- Uses Small 30µH Inductor

APPLICATIONS

- Laptop and Palmtop Computers
- Portable Data-Gathering Instruments

DESCRIPTION

The LT®1432-3.3 is a control chip designed to operate with the LT1171/LT1271 family of switching regulators to make a very high efficiency 3.3V step-down (buck) switching regulator. A minimum of external components is needed.

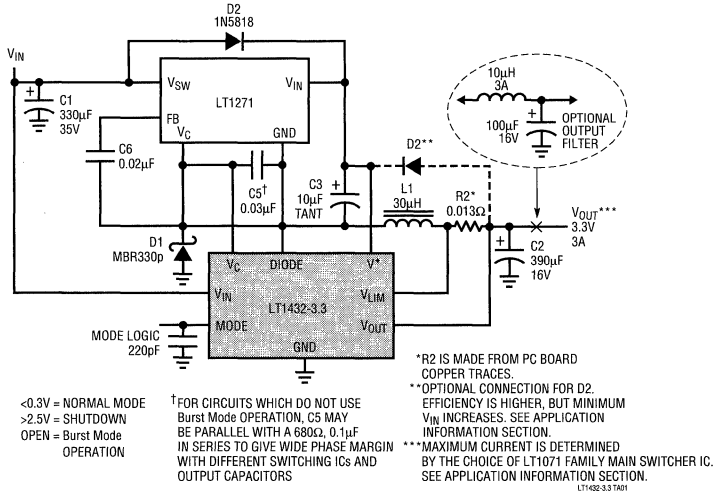
Included is an accurate current limit which uses only 60mV sense voltage and uses "free" PC board trace material for the sense resistor. Logic controlled electronic shutdown mode draws only 15µA battery current. The switching regulator operates down to 4.5V input.

The LT1432-3.3 has a logic controlled Burst Mode operation to achieve high efficiency at very light load currents (0mA to 100mA) such as memory keep-alive. In normal switching mode, the standby power loss is about 30mW, limiting efficiency at light loads. In Burst Mode operation, standby loss is reduced to approximately 11mW. Output current in this mode is typically in the 5mA to 100mA range.

The LT1432-3.3 is available in 8-pin SO and PDIP packages. The LT1171/LT1271 is also available in surface mount DD packages.

4

TYPICAL APPLICATION



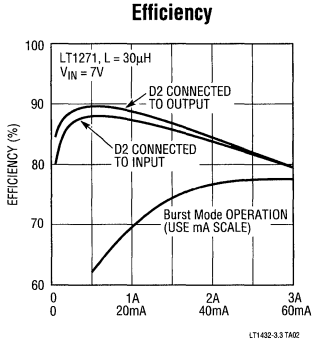
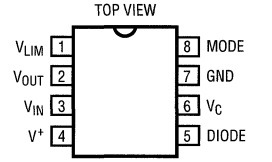


Figure 1. High Efficiency 5V Buck Converter

ABSOLUTE MAXIMUM RATINGS

V_{IN} Pin 30V
V^+ Pin 40V
V_C 35V
V_{LIM} and V_{OUT} Pins 7V
Diode Pin Voltage 30V
Mode Pin Current (Note 2) 1mA
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1432CN8-3.3 LT1432CS8-3.3

Consult factory for Military and Industrial grade parts.

ELECTRICAL CHARACTERISTICS

V_C = 4V, V_{IN} = 4V, V^+ = 8V, V_{DIODE} = Open, V_{LIM} = V_{OUT}, V_{MODE} = 0V, T_J = 25°C
Device is in standard test loop unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Regulated Output Voltage	V_C Current = 220µA	●	3.24	3.30	3.36	V
Output Voltage Line Regulation	V_{IN} = 4V to 30V	●		5	20	mV
Input Supply Current (Note 1)	V_{IN} = 4V to 30V, $V^+ = V_{IN}$ + 5V, $V_C = V_{IN}$ + 1V	●		0.3	0.5	mA
Quiescent Output Load Current				0.9	1.2	mA
Mode Pin Current	V_{MODE} = 0V (Current Is Out of Pin) V_{MODE} = 3.3V (Shutdown)	● ●		30 15	50 30	µA µA
Mode Pin Threshold Voltage (Normal to Burst)	I_{MODE} = 10µA (Out of Pin)	●	0.6	0.9	1.5	V
V_C Pin Saturation Voltage	V_{OUT} = 3.6V (Forced)	●		0.25	0.45	V
V_C Pin Maximum Sink Current	V_{OUT} = 3.6V (Forced)	●	0.45	0.8	1.5	mA
V_C Pin Source Current	V_{OUT} = 3.0V (Forced)	●	35	60	100	µA
Current Limit Sense Voltage (Note 3)	Device in Current Limit Loop		56	60	64	mV
V_{LIM} Pin Current	Device in Current Limit Loop (Current Is Out of Pin)	●	30	45	70	µA
Supply Current in Shutdown	$V_{MODE} > 3V$, $V_{IN} < 30V$, V_C and V^+ = 0V			15	60	µA
Burst Mode Operation Output Ripple	Device in Burst Test Circuit			100		mV_{p-p}
Burst Mode Operation Average Output Voltage	Device in Burst Test Circuit	●	3.15	3.30	3.45	V
Clamp Diode Forward Voltage	I_F = 1mA, All Other Pins Open	●		0.5	0.65	V
Start-up Drive Current	V_{OUT} = 1.5V (Forced), V_{IN} = 4V to 26V, $V^+ = V_{IN} - 1V$, $V_C = V_{IN} - 1.5V$	●	30	45		mA
Restart Time Delay	(Note 4)		0.7	1.2	10	ms
Transconductance, Output to V_C Pin	I_C = 150µA to 250µA	●	2700	3600	5000	µmho

ELECTRICAL CHARACTERISTICS

Operating parameters in standard circuit configuration.
V_{IN} = 7V, I_{OUT} = 0, unless otherwise noted. These parameters guaranteed where indicated, but not tested.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Burst Mode Operation Quiescent Input Supply Current				1.6	2.2	mA
Burst Mode Operation Output Ripple Voltage	I_{OUT} = 0 I_{OUT} = 50mA			80 120		mV_{p-p} mV_{p-p}
Normal Mode Equivalent Input Supply Current	Extrapolated from I_{OUT} = 20mA			3.0		mA
Normal Mode Minimum Operating Input Voltage	100mA < I_{OUT} < 1.5A			4.5		V
Burst Mode Operation Minimum Operating Input Voltage	5mA < I_{OUT} < 50mA		4.1		V	
Efficiency	Normal Mode I_{OUT} = 0.5A Burst Mode Operation I_{OUT} = 25mA			86 70		% %
Load Regulation	Normal Mode 50mA < I_{OUT} < 2A Burst Mode Operation 0 < I_{OUT} < 50mA			5 30	15	mV mV

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Does not include current drawn by the power IC. See operating parameters in standard circuit.

Note 2: Breakdown voltage on the Mode pin is 7V. External current must be limited to value shown.

Note 3: Current limit sense voltage temperature coefficient is +0.33%/°C to match TC of copper trace material.

Note 4: V_{OUT} pin switched from 3.6V to 3.0V.

4

EQUIVALENT SCHEMATIC

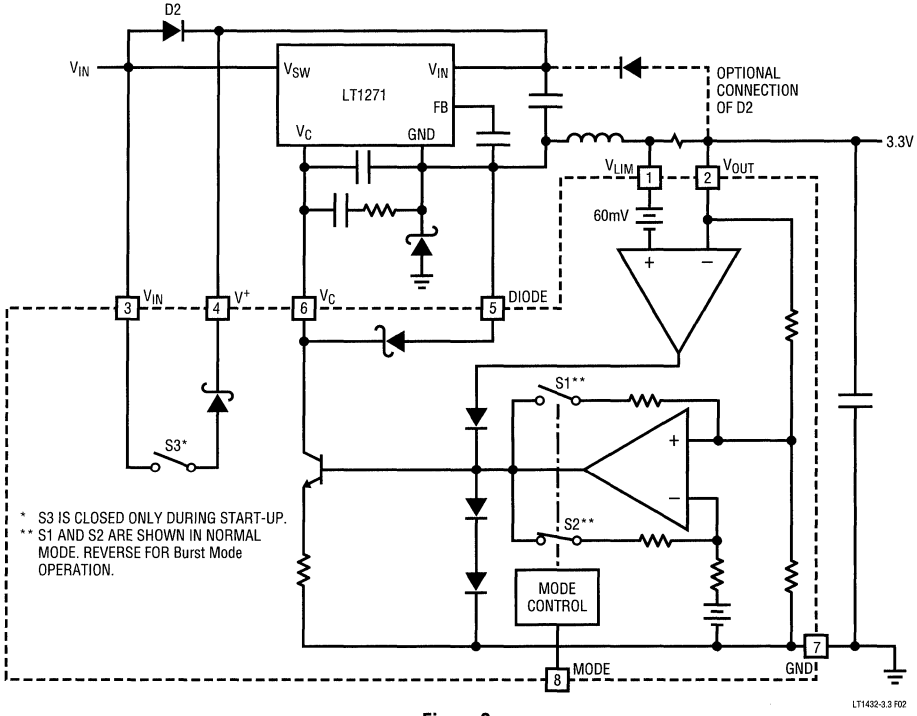
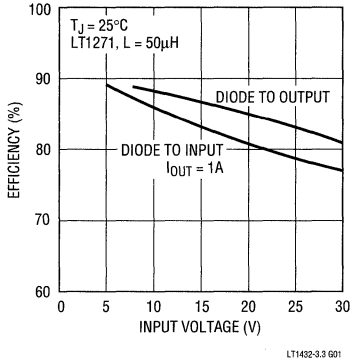


Figure 2

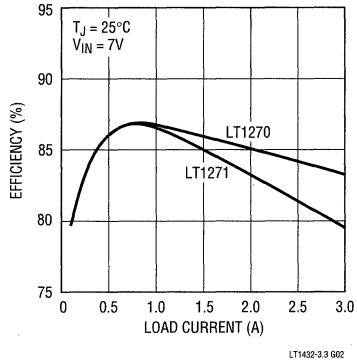
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Input Voltage



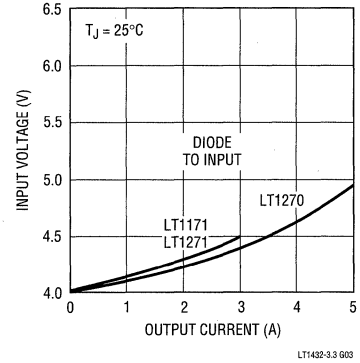
LT1432-3.3 G01

Efficiency vs Load Current



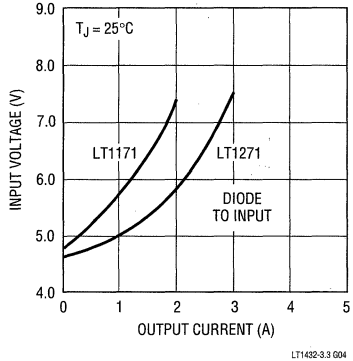
LT1432-3.3 G02

Minimum Input Voltage to Start – Normal Mode (Diode to Input)



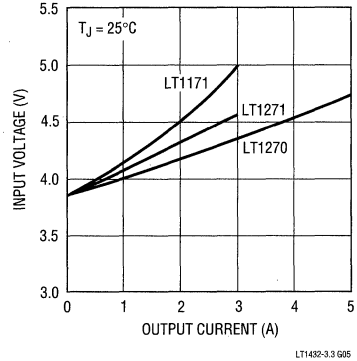
LT1432-3.3 G03

Minimum Input Voltage – Normal Mode (Diode to Output)



LT1432-3.3 G04

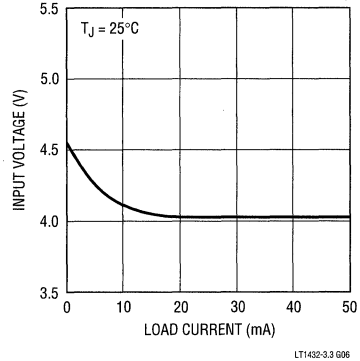
Minimum Running Voltage – Normal Mode*



LT1432-3.3 G05

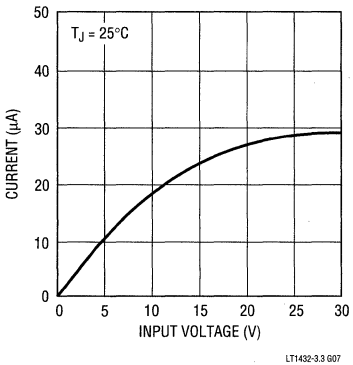
*SEE MINIMUM INPUT VOLTAGE TO START

Burst Mode Operation Minimum Input Voltage



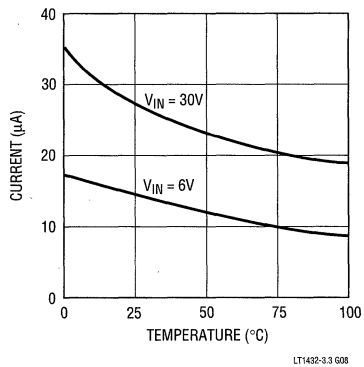
LT1432-3.3 G06

Shutdown Current vs Input Voltage



LT1432-3.3 G07

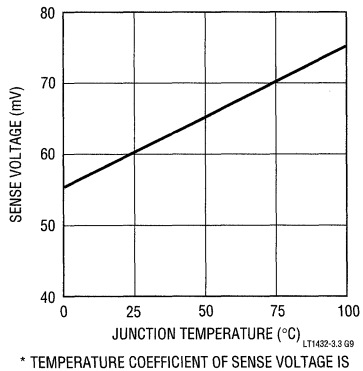
Battery Current in Shutdown*



LT1432-3.3 G08

*DOES NOT INCLUDE LT1271 SWITCH LEAKAGE.

Current Limit Sense Voltage*

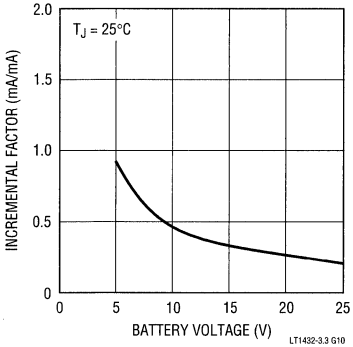


LT1432-3.3 G09

* TEMPERATURE COEFFICIENT OF SENSE VOLTAGE IS DESIGNED TO TRACK COPPER RESISTANCE.

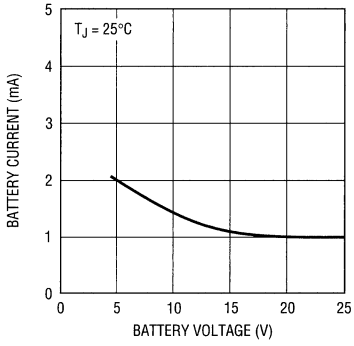
TYPICAL PERFORMANCE CHARACTERISTICS

Incremental Battery Current * in Burst Mode Operation

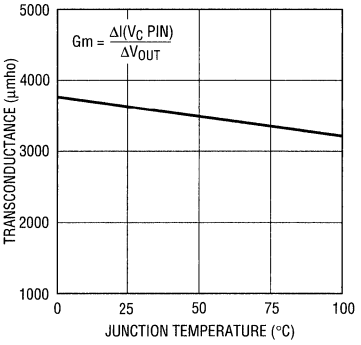


* TO CALCULATE TOTAL BATTERY CURRENT IN Burst Mode OPERATION, MULTIPLY LOAD CURRENT BY INCREMENTAL FACTOR AND ADD NO-LOAD CURRENT.

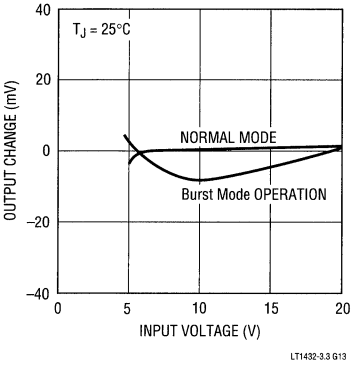
No Load Battery Current in Burst Mode Operation



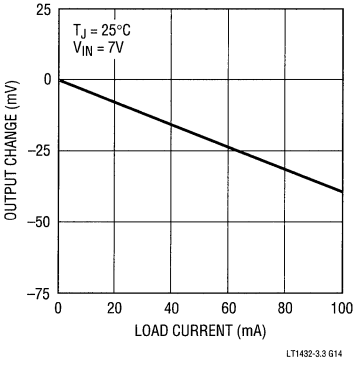
Transconductance – V_{OUT} to V_C Current



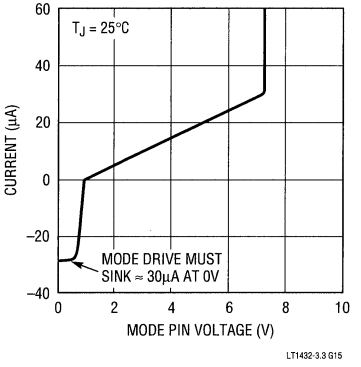
Line Regulation



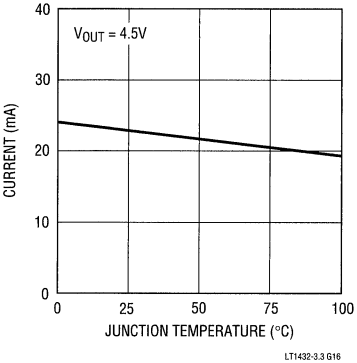
Burst Mode Operation Load Regulation



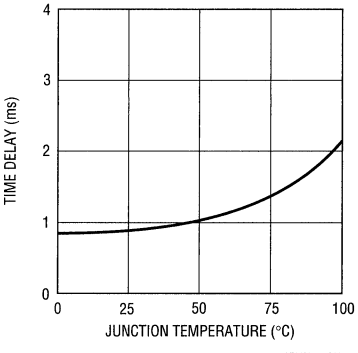
Mode Pin Current



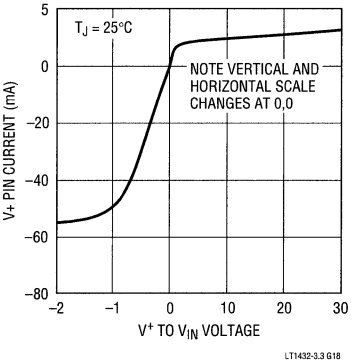
Restart Load Current



Restart Time Delay



Start-up Switch Characteristics



APPLICATIONS INFORMATION

More applications information on the LT1432-3.3 is available in the LT1432 data sheet.

Basic Circuit Description

The LT1432-3.3 is a dedicated 3.3V buck converter driver chip intended to be used with an IC switcher from the LT1171/ LT1271 family. This family of current mode switchers includes current ratings from 1.25A to 10A, and switching frequencies from 40kHz to 100kHz as shown in the table below.

DEVICE	SWITCH CURRENT	FREQUENCY	OUTPUT CURRENT IN BUCK CONVERTER
LT1270A	10A	60kHz	7.5A
LT1270	8A	60kHz	6A
LT1170	5A	100kHz	3.75A
LT1070	5A	40kHz	3.75A
LT1269	4A	100kHz	3A
LT1271	4A	60kHz	3A
LT1171	2.5A	100kHz	1.8A
LT1071	2.5A	40kHz	1.8A
LT1172	1.25A	100kHz	0.9A
LT1072	1.25A	40kHz	0.9A

The maximum load current which can be delivered by these chips in a buck converter is approximately 75% of their switch current rating. This is partly due to the fact that buck converters must operate at very high duty cycles when input voltage is low. The current mode nature of the LT1271 family requires an internal reduction of peak current limit at high duty cycles, so these devices are rated at only 80% of their full current rating when duty cycle is 80%. A second factor is inductor ripple current, half of which subtracts from maximum available load current. The LT1271 family was originally intended for topologies which have the negative side of the switch grounded, such as boost converters. It has an extremely efficient quasi-saturating NPN switch which mimics the linear resistive nature of a MOSFET but consumes much less die area. Driver losses are kept to a minimum with a patented adaptive antisat drive that maintains a forced beta of 40 over a wide range of switch currents. This family is attractive for high efficiency buck converters because of the low switch loss, but to operate as a positive buck converter, the GND pin of the IC must be floated to act as the switch output node. This requires a floating power supply for the chip and some means for level shifting the feedback signal. The LT1432-3.3 performs these functions as well as adding current limiting, micropower shutdown, and dual mode operation for high conversion efficiency with both heavy and very light loads.

The circuit in Figure 1 is a basic 3.3V positive buck converter which can operate with input voltage from 4.5V to 30V. The power switch is located between the V_{SW} pin and GND pin on the LT1271. Its current and duty cycle are controlled by the voltage on the V_C pin with respect to the GND pin. This voltage ranges from 1V to 2V as switch current increases from zero to full-scale. Correct output voltage is maintained by the LT1432-3.3 which has an internal reference and error amplifier (see Equivalent Schematic in Figure 2). The amplifier output is level shifted with an internal open collector NPN to drive the V_C pin of the switcher. The normal resistor divider feedback to the switcher feedback pin cannot be used because the feedback pin is referenced to the GND pin, which is switching up and down. The Feedback pin (FB) is simply bypassed with a capacitor. This forces the switcher V_C pin to swing high with about 200μA sourcing capability. The LT1432-3.3 V_C pin then sinks this current to control the loop. Transconductance from the regulator output to the V_C pin current is controlled to approximately 3600μmhos by local feedback around the LT1432-3.3 error amplifier (S2 closed in Figure 2). This is done to simplify frequency compensation of the overall loop. **A word of caution about the FB pin bypass capacitor (C6): this capacitor value is very non-critical, but the capacitor must be connected directly to the GND pin or tab of the switcher to avoid differential spikes created by fast switch currents flowing in the external PCB traces. This is also true for the frequency compensation capacitor C5. C5 forms the dominant loop pole.**

A floating power supply for the switcher is generated by D2 and C3 which peak detect the input voltage during switch off time. This is different than the 5V version of the LT1432 which connects the anode of the diode to the output rather than the input. The output connection is more efficient because the floating voltage is a constant 5V (or 3.3V), independent of input voltage, but in the case of the 3.3V circuit, minimum required input voltage for starting is several volts higher (see the Typical Performance Characteristics curves). When the diode is connected to the input, the suggested type is a

APPLICATIONS INFORMATION

Schottky 1N5818. Diode type is more critical for the output connection because the high capacitance of Schottky diodes creates narrow output spikes. These spikes will be eliminated if a secondary output filter is used or if there is sufficient lead length between the regulator output and the load bypass capacitors. Low capacitance diodes like the 1N4148 do not create large spikes, but their high forward resistance requires even higher input voltage to start.

D1, L1 and C2 act as the conventional catch diode and output filter of the buck converter. These components should be selected carefully to maintain high efficiency and acceptable output ripple. See the original LT1432 (5V) data sheet for detailed discussions of these parts.

Current limiting is performed by R2. Sense voltage is only 60mV to maintain high efficiency. This also reduces the value of the sense resistor enough to utilize a printed circuit board trace as the sense resistor. The sense voltage has a positive temperature coefficient of 0.33%/°C to match the temperature coefficient of copper.

The basic regulator has three different operating modes, defined by the Mode pin drive. Normal operation occurs when the Mode pin is grounded. A low quiescent current Burst Mode operation can be initiated by floating the Mode pin. Input supply current is typically 1.3mA in this mode, and output ripple voltage is $100mV_{p-p}$. Pulling the Mode pin above 2.5V forces the entire regulator into micropower shutdown where it typically draws less than 20μA.

Burst Mode Operation

Burst Mode operation is initiated by allowing the Mode pin to float, where it will assume a DC voltage of approximately 1V. If AC pickup from surrounding logic lines is likely, the Mode pin should be bypassed with a 200pF capacitor. Burst Mode operation is used to reduce quiescent operating current when the regulator output current is very low, as in sleep mode in a lap-top computer. In this mode, hysteresis is added to the error amplifier to make it switch on and off, rather than maintain a constant amplifier output. This forces the switching IC to either provide a rapidly increasing current or to go into full micropower shutdown. Current is delivered to the output capacitor in pulses of higher amplitude and low duty cycle rather than a continuous stream of low amplitude pulses. This maximizes efficiency at light load by eliminating quiescent current in the switching IC during the period between bursts.

The result of pulsating currents into the output capacitor is that output ripple amplitude increases and ripple frequency becomes a function of load current. The typical output ripple in Burst Mode operation is 100mVp-p, and ripple frequency can vary from 50Hz to 2kHz. This is not normally a problem for the logic circuits which are kept alive during sleep mode.

Some thought must be given to proper sequencing between normal mode and Burst Mode operation. A heavy (>100mA) load in Burst Mode operation can cause excessive output ripple, and an abnormally light load (10mA to 30mA, see Figure 3) in *normal* mode can cause the regulator to revert to a quasi-Burst Mode operation that also has higher output ripple. The worst condition is a sudden, large increase in load current (>100mA) during this quasi-Burst Mode operation or just after a switch from Burst Mode operation to normal mode. This can cause the output to sag badly while the regulator is establishing normal mode operation (≈100μs). To avoid problems, it is suggested that the power-down sequence consist of reducing load current to below 100mA, but greater than the minimum for normal mode, then switching to Burst Mode operation, followed by a reduction of load current to the final sleep value. Power-up would consist of increasing the load current to the minimum for

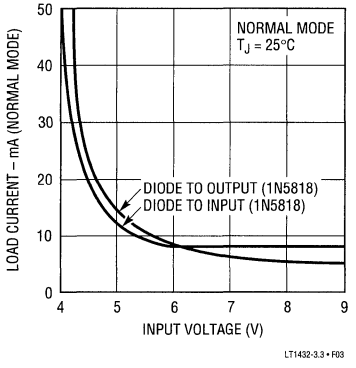


Figure 3. Minimum Normal Mode Load Current

APPLICATIONS INFORMATION

normal mode, then switching to normal mode, pausing for 1ms, followed by return to full load.

If this sequence is not possible, an alternative is to increase the output capacitor to > 680µF. This modification will often allow the power-down sequence to consist of simultaneous turn-off of load current and switch to Burst Mode operation. Power-up is accomplished by switching to normal mode and simultaneously increasing load current to the lowest possible value (30mA to 500mA), followed by a short pause and return to full load current.

Full Shutdown

When the Mode pin is driven high, full shutdown of the regulator occurs. Regulator input current will then consist of the LT1432 shutdown current (≈15µA) plus the switch leakage of the switching IC (≈1µA to 25µA). Mode input current (≈15µA at 5V) must also be considered. Start-up from shutdown can be in either normal or Burst Mode operation, but one should always check start-up overshoot, especially if the output capacitor or frequency compensation components have been changed.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1148	High Efficiency Step-Down Switching Regulator Controller	5V Regulated Output Voltage
LT1432	High Efficiency Synchronous Step-Down Switching Regulator	Adjustable and Fixed 5V or 3.3V Outputs
LT1507	1.5A, 500kHz Step-Down Switching Regulator	Fixed Frequency PWM for Low Input Voltages from 4.5V to 12V

SECTION 4—POWER PRODUCTS

Micropower Step-Up DC/DC Converter for PCMCIA Card Flash Memory

FEATURES

- **60mA Output Current at 12V from 3V Supply**
- **Shutdown to 10μA**
- Programmable 12V or 5V Output
- Up to 85% Efficiency
- Quiescent Current: 750μA
- Low V_{CESAT} Switch: 300mV at 0.5A Typical
- Uses Low Value, Thin, Surface Mount Inductors
- **Ultra-Thin 20-Lead TSSOP Package**

APPLICATIONS

- PCMCIA Card Flash Memory VPP Generator
- Portable Computers
- Portable Instruments
- DC/DC Converter Module Replacements

DESCRIPTION

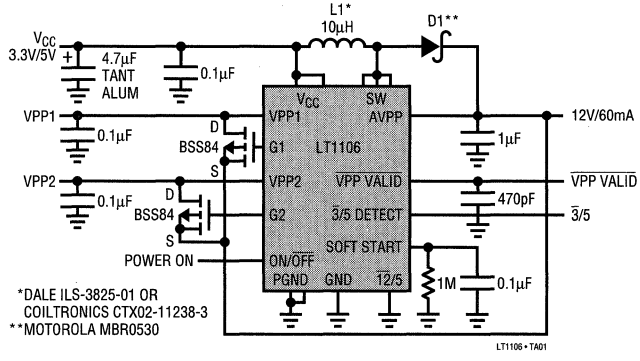
The LT®1106 is the industry's first DC/DC converter designed for use on Type I and Type II PCMCIA cards. The device senses the VPP1 and VPP2 lines at the PCMCIA socket and generates a regulated 12V, 60mA programming supply if the socket does not provide it. Internal logic simplifies the interface to PCMCIA card microcontrollers. One input selects a 12V or 5V regulated output, while another input controls micropower shutdown. Two logic outputs indicate when the selected programming voltage is valid and whether the input supply is 3.3V or 5V.

The regulator features Burst Mode™ operation with a 0.5A, 300mV switch for efficiency up to 85%. High frequency 500kHz switching permits the use of small value, flat inductors that fit neatly on PCMCIA cards. The device requires just 1μF of output capacitance.

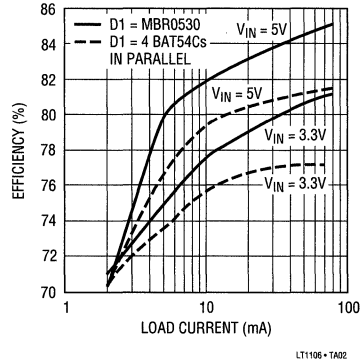
Quiescent current is 750μA which drops to 350μA when the card runs off the socket supply. The shutdown pin reduces supply current to only 10μA. The device includes a soft start feature which limits supply current transients when the card is inserted into a hot socket.

TYPICAL APPLICATION

12V, 60mA Flash Memory Programming Supply



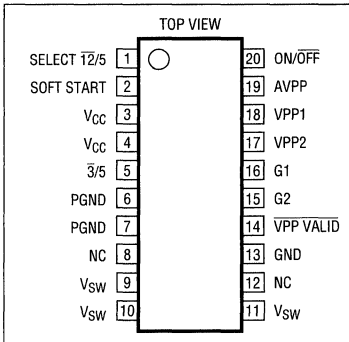
12V Output Efficiency



ABSOLUTE MAXIMUM RATINGS

V_{CC} Voltage 7V
V_{SW} Voltage 20V
AVPP Voltage 20V
VPP1, VPP2 Voltage 20V
G1, G2 Voltage 20V
$V_{ON/\overline{OFF}}$ Voltage 7V
V_{SEL} Voltage 7V
I_{LIM} Voltage 7V
Maximum Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



F PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 100°C, θ_{JA} = 90°C/W

ORDER PART NUMBER
LT1106CF

Consult factory for Industrial and Military grade parts

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5V, $V_{ON/\overline{OFF}}$ = 3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	V_{SEL} = 0.2V, AVPP = 12V			750	900	µA
	Quiescent Current, Shutdown	$V_{ON/\overline{OFF}}$ = 0.2V			9	15	µA
	"Doze" Mode Current	V_{SEL} = 0.2V, VPP1 or VPP2 = 12V			320		µA
	Input Voltage Range			2		6	V
	Output Sense Voltage	V_{SEL} = 3V, VPP1 and VPP2 Floating V_{SEL} = 0.2V, VPP1 and VPP2 Floating	● ●	4.75 11.50	5 12	5.25 12.60	V V
	Output Referred Comparator Hysteresis	V_{SEL} = 3V V_{SEL} = 0.2V			15 35		mV mV
f_{OSC}	Oscillator Frequency	Current Limit Not Asserted		400	500	700	kHz
DC	Maximum Duty Cycle		●	80	85	92	%
t_{ON}	Switch On-Time				1.7		µs
	Reference Line Regulation	2V < V_{IN} < 6V			0.06	0.15	%/V
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 0.5A			230	350	mV
	Switch Leakage Current	V_{SW} = 12V, Switch Off			0.1	10	µA
	Switch Current Limit	V_{IN} = 5V, Soft Start Floating V_{IN} = 3V, Soft Start Floating		450 500	600 650	900 950	mA mA
	Soft Start Pin Current	Soft Start Grounded			80	120	µA
	Select Input Voltage Low					0.8	V
	Select Input Voltage High			1.6			V
	ON/$\overline{OFF}$ Input Voltage Low					0.8	V
	ON/$\overline{OFF}$ Input Voltage High			1.6			V
	ON/$\overline{OFF}$ Bias Current	$V_{ON/\overline{OFF}}$ = 5V $V_{ON/\overline{OFF}}$ = 3V $V_{ON/\overline{OFF}}$ = 0V			16.0 8.0 0.1	24.0 14.0 1.1	µA µA µA

4

ELECTRICAL CHARACTERISTICS

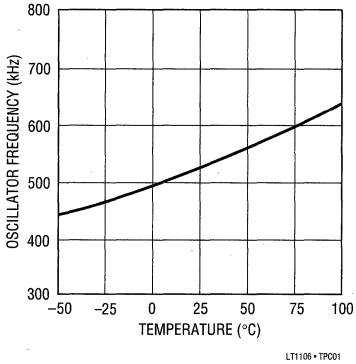
T_A = 25°C, V_{CC} = 5V, $V_{ON/\overline{OFF}}$ = 3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Select Pin Bias Current	0V < V_{SEL} < 5V			0.1	1	µA
	VPP1/VPP2 Input Sense Threshold			11.0	11.5	11.9	V
	AVPP Pin Input Current				50	90	µA
		$V_{ON/\overline{OFF}}$ = 0.2V			0.1	1	µA
	VPP1/VPP2 Pin Input Current				50	90	µA
		$V_{ON/\overline{OFF}}$ = 0.2V			0.1	1	µA
	$\overline{\text{VPP VALID}}$ Threshold	AVPP Rising (High to Low Transition)	●	11.4		12	V
	$\overline{\text{VPP VALID}}$ Output Voltage Low	I_{SINK} = 100µA			0.13	0.3	V
	$\overline{\text{VPP VALID}}$ Output Voltage High	I_{SOURCE} = 2.5µA		4	4.5		V
	$\overline{3}$/5 Comparator Threshold		●	3.6	3.75	4.2	V
	$\overline{3}$/5 Comparator Output High	I_{LOAD} = 50µA		3.65	3.8		V
	$\overline{3}$/5 Comparator Output Low	I_{LOAD} = 50µA			0.75	0.9	V
	Off State Current at G1/G2	VPP1 = 10V, VG1 = 12V or VPP2 = 10V, VG2 = 12V or $V_{ON/\overline{OFF}}$ = 0V			0.1	1	µA

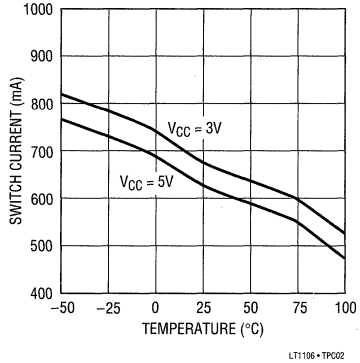
The ● denotes specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

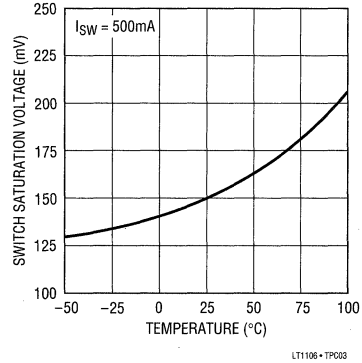
Oscillator Frequency



Switch Current Limit

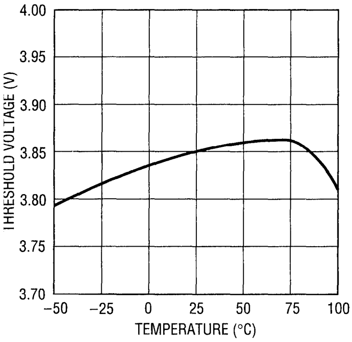


Switch Saturation Voltage



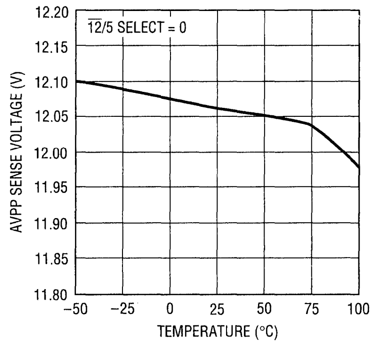
TYPICAL PERFORMANCE CHARACTERISTICS

3̄/5 Comparator Threshold



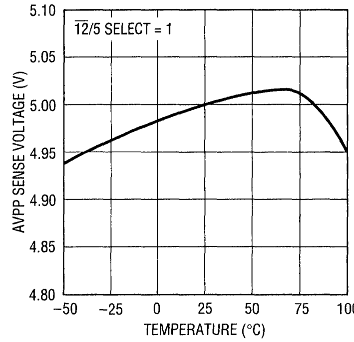
LT1106 • TPC04

AVPP Sense Voltage



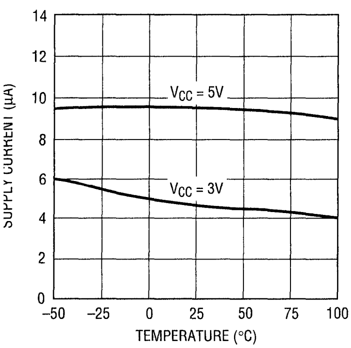
LT1106 • TPC05

AVPP Sense Voltage



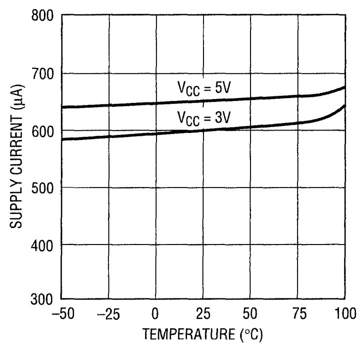
LT1106 • TPC06

Supply Current in Shutdown



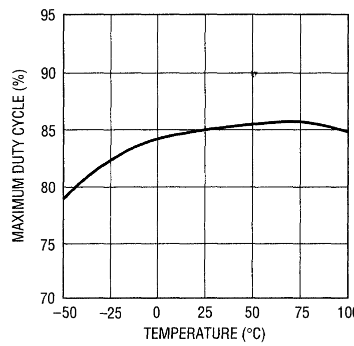
LT1106 • TPC07

Supply Current



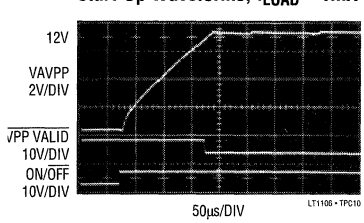
LT1106 • TPC08

Maximum Duty Cycle



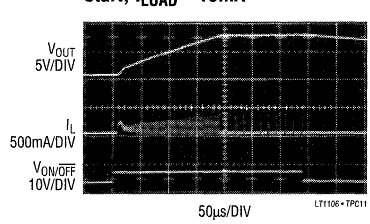
LT1106 • TPC09

Start-Up Waveforms, I_{LOAD} = 1mA



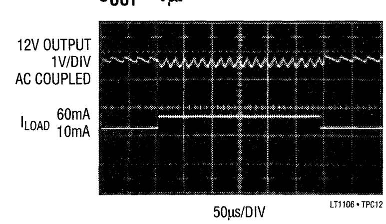
LT1106 • TPC10

Start-Up Waveforms with Soft Start, I_{LOAD} = 10mA



LT1106 • TPC11

Load Transient Response, C_{OUT} = 1μF



LT1106 • TPC12

4

PIN FUNCTIONS

SELECT $\overline{12}$/5 (Pin 1): Tie to V_{IN} or logic 1 for 5V output; tie to GND or logic 0 for 12V output.

SOFT START (Pin 2): A 0.1µF/1MΩ parallel RC from this pin to GND provides a Soft Start function upon device turn-on. Initially about 80µA will flow from the pin into the capacitor. When the voltage at the pin reaches approximately 0.4V, current ceases flowing out of the pin. See Applications Information section.

V_{CC} (Pins 3, 4): Input Supply. Both pins should be tied together. At least 1µF input bypass capacitance is required. More capacitance reduces ringing on the supply line.

$\overline{3}$/5 (Pin 5): Supply Comparator Output. This pin provides logic output indicating the value of the input supply. High when V_{CC} = 5V; low when V_{CC} = 3.3V.

PGND (Pins 6, 7): Power Ground. Connect to ground plane.

V_{SW} (Pins 9, 10, 11): Collector of Power Switch. High dV/dt present on this pin. To minimize radiated noise keep layout short and direct.

GND (Pin 13): Signal Ground. Connect of ground plane.

$\overline{\text{VPP VALID}}$ (Pin 14): This pin provides a logic signal indicating that ouput voltage is greater than 11.4V. Active low with internal 200k pull-up resistor.

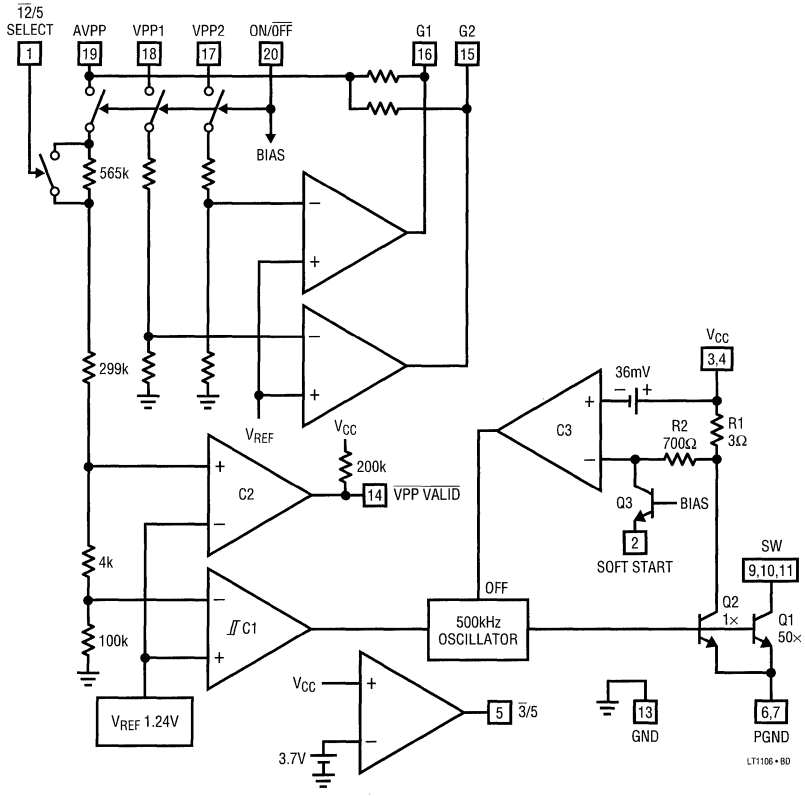
G1, G2 (Pins 16, 15): External MOSFET Gate Drives. When VPP1 or VPP2 is greater than 11.7V, G1 or G2 is driven to about 0.8V. When VPP1 or VPP2 is less than 11.7V, the drives assume a high impedance state pulled up to the AVPP pin through an internal 100k resistor.

VPP1, VPP2 (Pins 18, 17): Programming Power Inputs. The LT1106 senses both VPP1 and VPP2 supplies at the PCMCIA card socket. If VPP1 or VPP2 is greater than 11V, the LT1106 operates in "Doze" Mode—the switching regulator turns off and the drive to external P-channel MOSFETs turns on. Supply current in Doze Mode is about 350µA. Input current into VPP1 and VPP2 is about 1µA when the device is shut down.

AVPP (Pin 19): Output Sense Pin. This pin connects to a 1MΩ resistive divider that sets the output voltage. In shutdown, the resistor string is disconnected and current into this pin is reduced to <1µA.

ON/$\overline{\text{OFF}}$ (Pin 20): Shutdown Control. When pulled below 1.5V, this pin disables the LT1106 and reduces supply current to 10µA. All circuitry except the $\overline{3}$/5 comparator is disabled in shutdown. The part is enabled when ON/$\overline{\text{OFF}}$ is greater than 1.5V.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Functional Description

The LT1106 is a micropower, step-up DC/DC converter specifically configured for PCMCIA flash memory card VPP generation. The device generates a 5V or 12V output selectable via the 12/5 Select pin. If 12V is present on either the VPP1 or VPP2 pins, gate drive outputs G1 and G2 are driven low, turning on external PMOS devices. The switching regulator inside the LT1106 is idled when 12V is present on VPP1 or VPP2.

The VPP VALID output goes low when the voltage at AVPP exceeds 11.4V This signal can be used to indicate presence of a valid programming voltage. The 3/5 comparator indicates whether the input voltage is 3.3V or 5V.

The Soft Start pin can be used to limit inrush current upon start-up. A 0.1µF capacitor in parallel with a 1M resistor is connected between this pin and ground to limit peak inductor current at start-up.

Switching Regulator Operation

When 12V is not present on the VPP1 or VPP2 pins and the device is enabled (ON/OFF = 1), the LT1106 generates a regulated voltage at the AVPP pin. This voltage is programmable between 5V or 12V depending on the state of the 12/5 Select pin. Referring to the block diagram, hysteretic comparator C1 monitors AVPP via the resistor divider. When the negative input of C2 falls below 1.24V, C1's

APPLICATIONS INFORMATION

output goes high, enabling the oscillator. Switch Q1 alternately turns on causing current build-up in the inductor; then turns off allowing the built-up current to flow into the output capacitor via the catch diode. As the output voltage increases, so does the voltage at C1's negative input. When it exceeds the reference voltage plus C1's hysteresis, C1 turns the oscillator off.

Switch current is limited to approximately 600mA by Q2, R1 and C3. Two percent of Q1's collector current flows in Q2; this current flows through R1 causing a voltage drop in R1 proportional to Q1's collector current. When R1's drop equals 36mV, comparator C3 forces the oscillator off. This action results in varying on-time, fixed off-time operation that keeps peak switch current controlled. By connecting a 0.1μF capacitor from the Soft Start pin to ground, a current will flow in Q3 upon start-up. The current flows through 700Ω resistor R2, reducing the amount of current needed from Q2 to force the oscillator off. As current flows into the 0.1μF capacitor, the voltage at pin 2 increases and eventually current ceases to flow in Q3.

Inductor Selection

All components for use in PCMCIA Type I cards must be less than 1.1mm high. This somewhat limits the selection of appropriate inductors. Dale Electronics (605-665-9301) manufactures the ILS-3825-01, a monolithic ferrite inductor that meets Type I height requirements. Generally, inductors used with the LT1106 must fulfill several requirements. It must be able to carry 0.95A (the maximum switch current) without saturation. DCR should be kept low to maintain efficiency. The switching frequency of the LT1106 is quite high, over 500kHz so magnetic material is important. Ferrite core material works well in this frequency range. Avoid low cost iron powder cores which have substantial AC loss at the LT1106's switching frequency. Inductance value need not be over 10μH.

Capacitor Selection

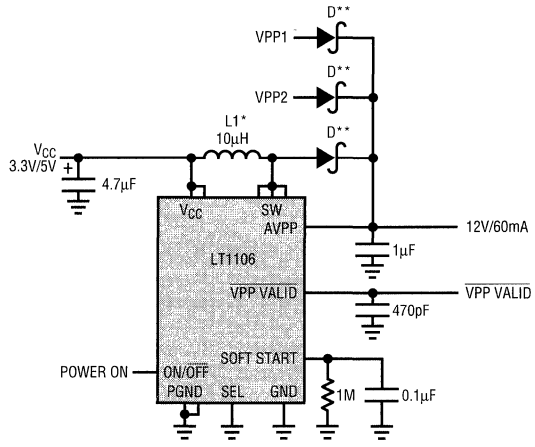
The LT1106 will operate with 1μF of output capacitance. Output ripple voltage is approximately 400mV with this value and can be reduced significantly by increasing output capacitance. The ripple voltage, although on the high side, poses no problems for programming flash memory. If operating the device in 5V ouput mode the capacitance should be increased. Ceramic capacitors are suitable for the output. Distributed capacitance, i.e., 0.1μF or 0.2μF units next to individual flash memory chips, is acceptable. The input capacitor should have at least some tantalum capacitance (low Q) to minimize resonance on the input. Flash memory cards are typically several inches away from a solid low impedance supply due to sockets, connectors, etc. If just ceramic capacitors are used at the supply pin of the LT1106, switching currents will resonate the supply line causing ringing that can exceed $500mV_{P-P}$. The high Q, low ESR nature of ceramic capacitors causes this. A few microfarad's worth of tantalum capacitors with moderate ESR and low Q characteristics will reduce or eliminate the problem.

Diode Selection

As with inductors, most good power Schottky diodes are in packages that exceed the 1.1mm height limit of the Type I PCMCIA card. Motorola manufactures the MBR0530 Schottky diode, ideal for use with the LT1106. This diode's maximum height however, is 1.35mm, making it difficult to use in Type 1 cards. Philips Components manufactures the BAT54C. Four units in parallel make an adequate diode.

TYPICAL APPLICATION

Alternative Scheme Allows 12V from VPP1/VPP2 to Provide Power When LT1106 is in Shutdown



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RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1109	5V to 12V/60mA VPP Generator	300µA I_Q, 120kHz Oscillator
LT1109A	5V to 12V/120mA VPP Generator	300µA I_Q, 120kHz Oscillator
LT1301	5V to 12V/200mA VPP Generator	120µA I_Q, 155kHz Oscillator
LT1309	5V to 12V/60mA VPP Generator	650µA I_Q, 650kHz Oscillator

High Efficiency Synchronous Step-Down Switching Regulators

FEATURES

- **Operation from 4V to 40V Input Voltage**
- **Ultra-High Efficiency: Up to 95%**
- **20μA Supply Current in Shutdown**
- High Efficiency Maintained Over Wide Current Range
- Current Mode Operation for Excellent Line and Load Transient Response
- Very Low Dropout Operation: 100% Duty Cycle
- Short-Circuit Protection
- Synchronous FET Switching for High Efficiency
- Adaptive Non-Overlap Gate Drives
- Available in SSOP and SO Packages

APPLICATIONS

- Step-Down and Inverting Regulators
- Notebook and Palmtop Computers
- Portable Instruments
- Battery-Operated Digital Devices
- Industrial Power Distribution
- Avionics Systems
- Telecom Power Supplies

DESCRIPTION

The LTC®1159 series is a family of synchronous step-down switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. These devices drive external complementary power MOSFETs at switching frequencies up to 250kHz using a constant off-time current-mode architecture.

A separate pin and on-board switch allow the MOSFET driver power to be derived from the regulated output voltage providing significant efficiency improvement when operating at high input voltages. The constant off-time current-mode architecture maintains constant ripple current in the inductor and provides excellent line and load transient response. The output current level is user programmable via an external current sense resistor.

The LTC1159 automatically switches to power saving Burst Mode operation when load current drops below approximately 15% of maximum current. Standby current is only 300μA while still regulating the output and shutdown current is a low 20μA.

TYPICAL APPLICATION

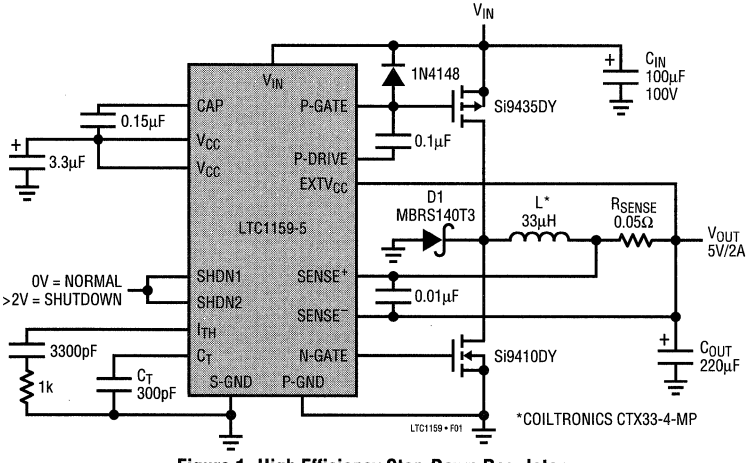
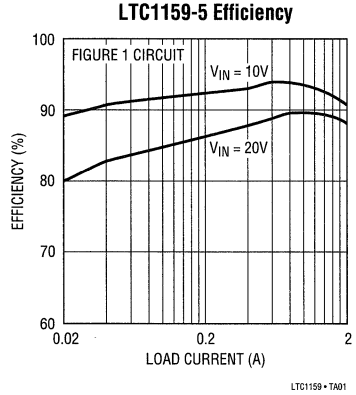


Figure 1. High Efficiency Step-Down Regulator

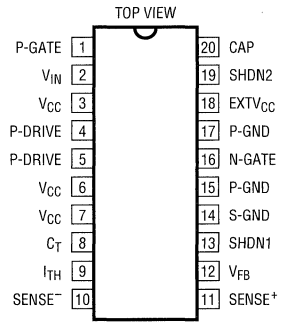


ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 2) ..... –15V to 60V
I_{CC} Output Current (Pin 3) 50mA
Continuous Pin Currents (Any Pin) 50mA
Sense Voltages ..... –0.3V to 13V
Shutdown Voltages 7V
$EXTV_{CC}$ Input Voltage 15V

Operating Temperature Range ..... 0°C to 70°C
Extended Commercial
Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

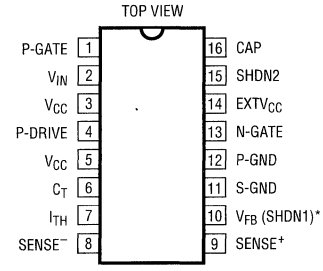


G PACKAGE
20-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 135°C/W

ORDER PART NUMBER

LTC1159CG
LTC1159CG-3.3
LTC1159CG-5



N PACKAGE
16-LEAD PDIP

S PACKAGE
16-LEAD PLASTIC SO

*FIXED OUTPUT VERSIONS

T_{JMAX} = 125°C, θ_{JA} = 80°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER

LTC1159CN
LTC1159CN-3.3
LTC1159CN-5
LTC1159CS
LTC1159CS-3.3
LTC1159CS-5

4

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{SHDN1} = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{FB}	Feedback Voltage (LTC1159 Only)		●	1.21	1.25	1.29	V
I_{FB}	Feedback Current (LTC1159 Only)		●		0.2		µA
V_{OUT}	Regulated Output Voltage LTC1159-3.3 LTC1159-5	V_{IN} = 9V I_{LOAD} = 700mA I_{LOAD} = 700mA	 ● ●	 3.23 4.90	 3.33 5.05	 3.43 5.20	 V V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 9V to 40V		–40	0	40	mV
	Output Voltage Load Regulation LTC1159-3.3 LTC1159-5	 5mA < I_{LOAD} < 2A 5mA < I_{LOAD} < 2A	 ● ●	 	 40 60	 65 100	 mV mV
	Burst Mode Output Ripple	I_{LOAD} = 0A			50		mV_{P-P}
I_N	V_{IN} Pin Current (Note 3) Normal Mode Shutdown	 V_{IN} = 12V, $EXTV_{CC}$ = 5V V_{IN} = 40V, $EXTV_{CC}$ = 5V V_{IN} = 12V, V_{SHDN2} = 2V V_{IN} = 40V, V_{SHDN2} = 2V	 	 	 200 300 15 25	 	 µA µA µA µA
I_{EXTVCC}	$EXTV_{CC}$ Pin Current (Note 3)	$EXTV_{CC}$ = 5V, Sleep Mode			250		µA
V_{CC}	Internal Regulator Voltage	V_{IN} = 12V to 40V, $EXTV_{CC}$ = 0V, I_{CC} = 10mA	●	4.25	4.5	4.75	V
$V_{IN} – V_{CC}$	V_{CC} Dropout Voltage	V_{IN} = 4V, $EXTV_{CC}$ = Open, I_{CC} = 10mA			300	400	mV

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{SHDN1} = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{EXT} - V_{CC}$	$EXTV_{CC}$ Switch Drop	V_{IN} = 12V, $EXTV_{CC}$ = 5V, I_{SWITCH} = 10mA			250	350	mV
$V_{P-GATE} - V_{IN}$	P-Gate to Source Voltage (Off)	V_{IN} = 12V V_{IN} = 40V		−0.2 −0.2	0 0		V V
$V_{SENSE^+} - V_{SENSE^-}$	Current Sense Threshold Voltage LTC1159	 V_{SENSE^-} = 5V, V_{FB} = 1.32V (Forced) V_{SENSE^-} = 5V, V_{FB} = 1.15V (Forced)	 ●	 130	 25 150	 170	 mV mV
	LTC1159-3.3	V_{SENSE^-} = 3.4V (Forced) V_{SENSE^-} = 3.1V (Forced)	 ●	 130	25 150	 170	mV mV
	LTC1159-5	V_{SENSE^-} = 5.2V (Forced) V_{SENSE^-} = 4.7V (Forced)	 ●	 130	25 150	 170	mV mV
V_{SNDN1}	SHDN1 Threshold LTC1159CG, LTC1159-3.3, LTC1159-5			0.6	0.8	2	V
V_{SHDN2}	SHDN2 Threshold			0.8	1.4	2	V
I_{SHDN2}	Shutdown 2 Input Current	V_{SHDN2} = 5V			12	20	µA
I_{CT}	C_T Pin Discharge Current	V_{OUT} in Regulation V_{OUT} = 0V		50	70 2	90 10	µA µA
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V		4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins P-Drive and N-Gate), V_{IN} = 6V			100	200	ns

−40°C ≤ T_A ≤ 85°C (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{FB}	Feedback Voltage (LTC1159 Only)		1.2	1.25	1.3	V
V_{OUT}	Regulated Output Voltage LTC1159-3.3 LTC1159-5	V_{IN} = 9V I_{LOAD} = 700mA I_{LOAD} = 700mA	 3.17 4.85	 3.30 5.05	 3.43 5.25	 V V
I_{IN}	V_{IN} Pin Current (Note 3) Normal	 V_{IN} = 12V, $EXTV_{CC}$ = 5V V_{IN} = 40V, $EXTV_{CC}$ = 5V		 200 300		 µA µA
	Shutdown	V_{IN} = 12V, V_{SHDN2} = 2V V_{IN} = 40V, V_{SHDN2} = 2V		15 25		µA µA
I_{EXTVCC}	$EXTV_{CC}$ Pin Current (Note 3)	$EXTV_{CC}$ = 5V, Sleep Mode		250		µA
V_{CC}	Internal Regulator Voltage	V_{IN} = 12V to 40V, $EXTV_{CC}$ = 0V, I_{CC} = 10mA		4.5		V
$V_{SENSE^+} - V_{SENSE^-}$	Current Sense Threshold Voltage	Low Threshold (Forced) High Threshold (Forced)	 125	25 150	 175	mV mV
V_{SHDN2}	SHDN2 Threshold		0.8	1.4	2	V
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V	3.5	5	6.5	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
LTC1159CG, LTC1159CG-3.3, LTC1159CG-5: $T_J = T_A + (P_D \times 135°C/W)$
LTC1159CN, LTC1159CN-3.3, LTC1159CN-5: $T_J = T_A + (P_D \times 80°C/W)$
LTC1159CS, LTC1159CS-3.3, LTC1159CS-5: $T_J = T_A + (P_D \times 110°C/W)$

Note 2: On LTC1159 versions which have a SHDN1 pin, it must be at ground potential for testing.

Note 3: The LTC1159 V_{IN} and $EXTV_{CC}$ current measurements exclude MOSFET driver currents. When V_{CC} power is derived from the output via $EXTV_{CC}$, the input current increases by ($I_{GATECHG}$ × Duty Cycle)/(Efficiency). See Typical Performance Characteristics and Applications Information.

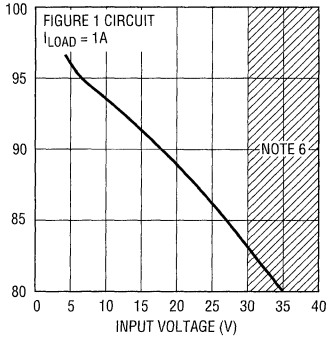
Note 4: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

Note 5: The LTC1159, LTC1159-3.3, and LTC1159-5 are not tested and not quality assurance sampled at −40°C and 85°C. These specifications are guaranteed by design and/or correlation.

Note 6: The logic-level power MOSFETs shown in Figure 1 are rated for $V_{DS(MAX)}$ = 30V. For operation at V_{IN} > 30V, use standard threshold MOSFETs with $EXTV_{CC}$ powered from a 12V supply. See Applications Information.

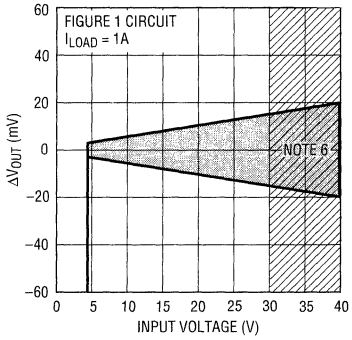
YPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Input Voltage



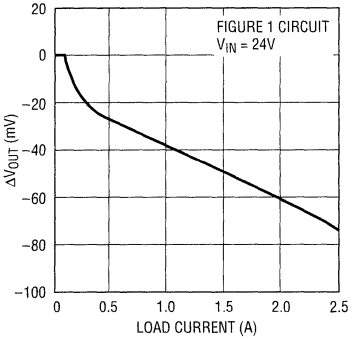
LTC1159 • TPC01

Line Regulation



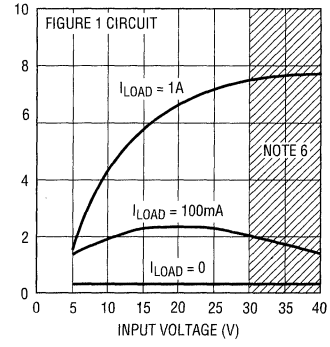
LT1159 • TPC02

Load Regulation



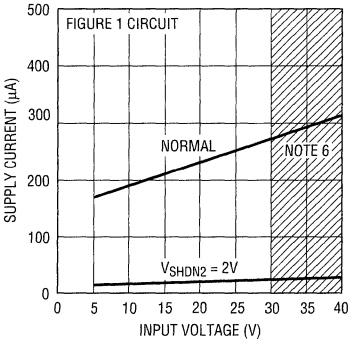
LTC1159 • TPC03

$EXTV_{CC}$ Pin Current



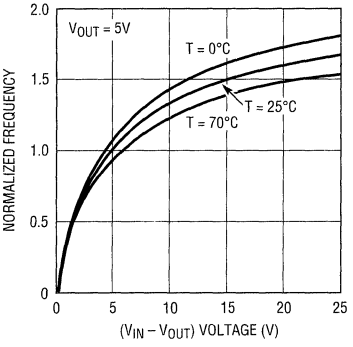
LTC1159 • TPC04

V_{IN} Pin Current



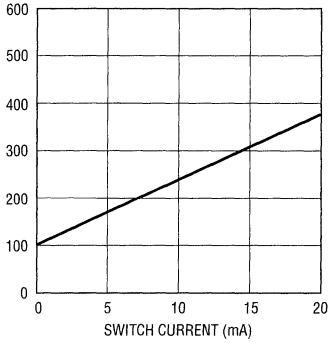
LTC1159 • TPC05

Operating Frequency vs (V_{IN} – V_{OUT})



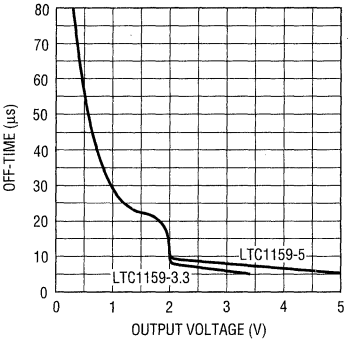
LTC1159 • TPC06

$EXTV_{CC}$ Switch Drop



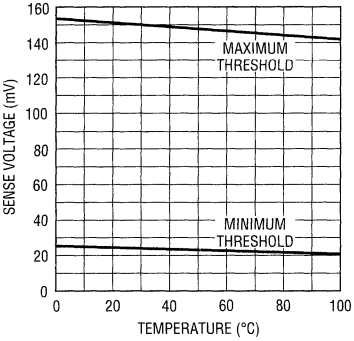
LTC1159 • TPC07

Off-Time vs V_{OUT}



LTC1159 • TPC08

Current Sense Threshold Voltage



LTC1159 • TPC09

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PIN FUNCTIONS

V_{IN}: Main Supply Input Pin.

S-GND: Small Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

P-GND: Driver Power Grounds. Connect to source of N-channel MOSFET and the (–) terminal of C_{IN}.

V_{CC}: Outputs of internal 4.5V linear regulator, $EXTV_{CC}$ switch, and supply inputs for driver and control circuits. The driver and control circuits are powered from the higher of the 4.5V regulator or $EXTV_{CC}$ voltage. Must be closely decoupled to power ground.

C_T: External capacitor C_T from this pin to ground sets the operating frequency. (The frequency is also dependent on the ratio V_{OUT}/V_{IN}.)

I_{TH}: Gain Amplifier Decoupling Point. The current comparator threshold increases with the I_{TH} pin voltage.

V_{FB}: For the LTC1159 adjustable version, the V_{FB} pin receives the feedback voltage from an external resistive divider used to set the output voltage.

Sense⁻: Connects to internal resistive divider which sets the output voltage in fixed output versions. The Sense⁻ pin is also the (–) input of the current comparator.

Sense⁺: The (+) Input for the Current Comparator. A built-in offset between the Sense⁺ and Sense⁻ pins, in conjunction with R_{SENSE}, sets the current trip threshold.

N-Gate: High Current Drive for the Bottom N-Channel MOSFET. The N-Gate pin swings from ground to V_{CC}.

P-Gate: Level-Shifted Gate Drive Signal for the Top P-Channel MOSFET. The voltage swing at the P-gate pin is from V_{IN} to $V_{IN} - V_{CC}$.

P-Drive: High Current Gate Drive for the Top P-Channel MOSFET. The P-drive pin(s) swing(s) from V_{CC} to ground.

CAP: Charge Compensation Pin. A capacitor to V_{CC} provides charge required by the P-gate level-shift capacitor during supply transitions. *The charge compensation capacitor must be larger than the gate drive capacitor.*

SHDN1: This pin shuts down the control circuitry only (V_{CC} is not affected). Taking SHDN1 pin high turns off the control circuitry and holds both MOSFETs off. This pin must be at ground potential for normal operation.

SHDN2: Master Shutdown Pin. Taking SHDN2 high shuts down V_{CC} and all control circuitry.

OPERATION (Refer to Functional Diagram)

The LTC1159 uses a current mode, constant off-time architecture to synchronously switch an external pair of complementary power MOSFETs. Operating frequency is set by an external capacitor at the C_T pin.

The output voltage is sensed either by an internal voltage divider connected to the Sense⁻ pin (LTC1159-3.3 and LTC1159-5) or an external divider returned to the V_{FB} pin (LTC1159). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1159 automatically switches between two modes of operation, burst and continuous.

A low dropout 4.5V regulator provides the operating voltage V_{CC} for the MOSFET drivers and control circuitry during start-up. During normal operation, the LTC1159 family powers the drivers and control from the output via the $EXTV_{CC}$ pin to improve efficiency. The N-gate pin is referenced to ground and drives the N-channel MOSFET gate directly. The P-channel gate drive must be referenced to the main supply input V_{IN}, which is accomplished by level-shifting the P-drive signal via an internal 550k resistor and external capacitor.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between the Sense⁺ and Sense⁻ pins connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the P-gate output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor C_T is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage to model the inductor current, which decays at a rate which is also proportional to the output voltage. While the timing capacitor is discharging, the N-gate output is high, turning on the N-channel MOSFET.

OPERATION (Refer to Functional Diagram)

When the voltage on C_T has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the N-gate output to go low (turning off the N-channel MOSFET) and the P-gate output to also go low (turning the P-channel MOSFET back on). The cycle then repeats. As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage to increase the current comparator threshold, thus tracking the load current.

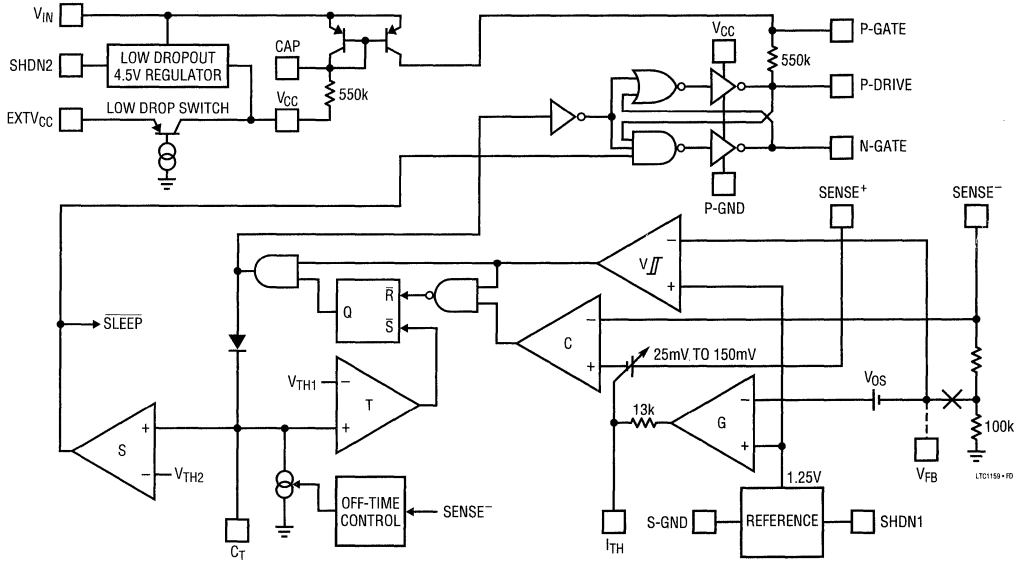
The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{SLEEP}$ line to go low and the P-channel MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode, much of the circuitry is turned off, dropping the supply current from several milliamps (with the MOSFETs switching) to 300μA. When the output capacitor has discharged by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats. To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset is incorporated in the gain stage.

To prevent both the external MOSFETs from being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the N-gate output can go high, the P-drive output must also be high. Likewise, the P-drive output is prevented from going low when the N-gate output is high.

4

FUNCTIONAL DIAGRAM Internal divider broken at V_{FB} for adjustable versions.



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The LTC1159 Compared to the LTC1148/LTC1149 Families

The LTC1159 family is closest in operation to the LTC1149 and shares much of the applications information. In addition to reduced quiescent and shutdown currents, the LTC1159 adds an internal switch which allows the driver and control sections to be powered from an external source for higher efficiency. This change affects Power MOSFET Selection, $EXTV_{CC}$ Pin Connection, Important Information About LTC1159 Adjustable Applications, and Efficiency Considerations found in this section.

The basic LTC1159 application circuit shown in Figure 1 is limited to a maximum input voltage of 30V due to MOSFET breakdown. If the application does not require greater than 18V operation, then the LTC1148 or LTC1148HV should be used. For higher input voltages where quiescent and shutdown current are not critical, the LTC1149 may be a better choice since it is set up to drive standard threshold MOSFETs.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1159 current comparator has a threshold range which extends from a minimum of $0.025V/R_{SENSE}$ to a maximum of $0.15V/R_{SENSE}$. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)} = 0.025V/R_{SENSE}$ (see C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1159 and external component values yields:

$$R_{SENSE} = \frac{100}{I_{MAX}}\ m\Omega$$

A graph for selecting R_{SENSE} versus maximum output current is given in Figure 2. The LTC1159 series works well with values of R_{SENSE} from 0.02Ω to 0.2Ω.

The load current below which Burst Mode operation commences, I_{BURST}, and the peak short-circuit current, $I_{SC(PK)}$, both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following equations:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

The LTC1159 automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

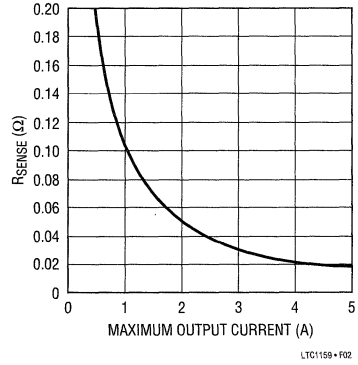

Figure 2. R_{SENSE} vs Maximum Output Current

L and C_T Selection for Operating Frequency

The LTC1159 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. The value of C_T is calculated from the desired continuous mode operating frequency, f:

$$C_T = \frac{7.8 \times 10^{-5}}{f}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A graph for selecting C_T versus frequency including the effects of input voltage is given in Figure 3.

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency is given by:

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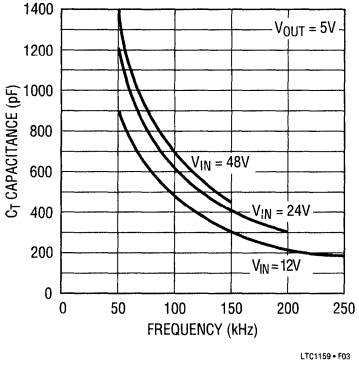

Figure 3. Timing Capacitor Selection

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where $t_{OFF} = 1.3 \times 10^4 \times C_T$

ınce the frequency has been set by C_T, the inductor L ıust be chosen to provide no more than $0.025V/R_{SENSE}$ f peak-to-peak inductor ripple current. This results in a ıinimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

s the inductor value is increased from the minimum value, ıe ESR requirements for the output capacitor are eased at ıe expense of efficiency. If too small an inductor is used, ıe LTC1159 may not enter Burst Mode operation and ffficiency will be severely degraded at low currents.

ıductor Core Selection

nce the minimum value for L is known, the type of ıductor must be selected. High efficiency converters ənerally cannot afford the core loss found in low cost ɔwdered iron cores, forcing the use of more expensive ırrite, molypermalloy, or Kool Mμ® cores. Actual core loss independent of core size for a fixed inductor value, but it very dependent on the inductance selected. As induc-ınce increases, core losses go down but copper (I^2R) ısses will increase.

ərrite designs have very low core loss, so design goals can ɔncentrate on copper loss and preventing saturation. ərrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered in the LTC1159. Do not allow the core to saturate!

Molypermalloy (from Magnetics, Inc.) is a low loss core material for toroids, but it is more expensive than ferrite. A reasonable compromise from the same manufacturer is Kool Mμ. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new surface mount designs available from Coiltronics do not increase the height significantly.

Power MOSFET Selection

Two external power MOSFETs must be selected for use with the LTC1159: a P-channel MOSFET for the main switch and an N-channel MOSFET for the synchronous switch.

The peak-to-peak drive levels are set by the V_{CC} voltage on the LTC1159. This voltage is typically 4.5V during start-up and 5V to 7V during normal operation (see $EXTV_{CC}$ Pin Connection). Consequently, *logic-level threshold MOSFETs must be used in most LTC1159 family applications.* The only exception is applications in which $EXTV_{CC}$ is powered from an external supply greater than 8V, in which standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage, and maximum output current. When the LTC1159 is operating in continuous mode, the duty cycle for the P-channel MOSFET is given by:

$$\text{P-Ch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{N-Ch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET dissipations at maximum output current are given by:

ol Mμ is a registered trademark of Magnetics, Inc.

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$$\text{P-Ch } P_D = \frac{V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_P) R_{DS(ON)} + k(V_{IN})^2 (I_{MAX}) (C_{RSS}) (f)$$

$$\text{N-Ch } P_D = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \partial_N) R_{DS(ON)}$$

where ∂ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current.

Both MOSFETs have I^2R losses while the P-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. The N-channel MOSFET losses are the greatest at high input voltage or during a short circuit when the N-channel duty cycle is nearly 100%.

The term $(1 + \partial)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\partial = 0.007/°C$ can be used as an approximation for low voltage MOSFETs. C_{RSS} is usually specified in the MOSFET electrical characteristics. The constant k = 5 can be used for the LTC1159 to estimate the relative contributions of the two terms in the P-channel dissipation equation.

The Schottky diode D1 shown in Figure 1 only conducts during the dead time between the conduction of the two power MOSFETs. D1 prevents the body diode of the N-channel MOSFET from turning on and storing charge during the dead time, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 is omitted). Therefore, D1 should be selected for a forward voltage of less than 0.6V when conducting I_{MAX}.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the P-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX} [V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{MAX}/2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. An additional 0.1µF ceramic capacitor may also be required on V_{IN} for high frequency decoupling.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1159:

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. Manufacturers such as Nichicon, Chemicon, and Sprague should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. For example, if 200µF/10V is called for in an application requiring 3mm height, two AVX 100µF/10V (P/N TPSD107K010) could be used. Consult the manufacturer for other specific recommendations.

At low supply voltages, a minimum value of C_{OUT} is suggested to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes the Burst Mode operation to be activated when the LTC1159 would normally be in continuous operation. The effect is most

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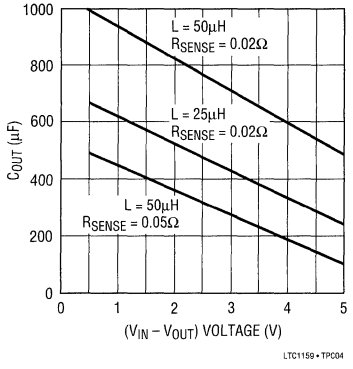

Figure 4. Minimum Suggested C_{OUT}

'onounced with low values of R_{SENSE} and can be ıproved by operating at higher frequencies with lower ılues of L. The output remains in regulation at all times.

ıad Transient Response

witching regulators take several cycles to respond to a ep in DC (resistive) load current. When a load step :curs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \times ESR$, here ESR is the effective series resistance of C_{OUT}. I_{LOAD} also begins to charge or discharge C_{OUT} until the gulator loop adapts to the current change and returns ɔUT to its steady state value. During this recovery time ɔUT can be monitored for overshoot or ringing which ould indicate a stability problem. The I_{TH} external ɔmponents shown in the Figure 1 circuit will provide lequate compensation for most applications.

second, more severe transient is caused by switching in ads with large (>1µF) supply bypass capacitors. The scharged bypass capacitors are effectively put in parallel ith C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can :liver enough current to prevent this problem if the load vitch resistance is low and it is driven quickly. The only ılution is to limit the rise time of the switch drive so that e load rise time is limited to approximately $25 \times C_{LOAD}$. ıus a 10µF capacitor would require a 250µs rise time, niting the charging current to about 200mA.

Line Transient Response

The LTC1159 has better than 60dB line rejection and is generally impervious to large positive or negative line voltage transients. However, one rarely occurring condition can cause the output voltage to overshoot if the proper precautions are not observed. This condition is a negative V_{IN} transition of several volts followed within 100µs by a positive transition of greater than 0.5V/µs slew rate.

The reason this condition rarely occurs is because it takes tens of amps to slew the regulator input capacitor at this rate! The solution is to add a diode between the cap and V_{IN} pins of the LTC1159 as shown in several of the typical application circuits. If you think your system could have this problem, add the diode. Note that in surface mount applications it can be combined with the P-gate diode by using a low cost common cathode dual diode.

$EXTV_{CC}$ Pin Connection

The LTC1159 contains an internal PNP switch connected between the $EXTV_{CC}$ and V_{CC} pins. The switch closes and supplies the V_{CC} power whenever the $EXTV_{CC}$ pin is higher in voltage than the 4.5V internal regulator. This allows the MOSFET driver and control power to be derived from the output during normal operation and from the internal regulator when the output is out of regulation (start-up, short circuit).

Significant efficiency gains can be realized by powering V_{CC} from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Efficiency). For 5V regulators this simply means connecting the $EXTV_{CC}$ pin directly to V_{OUT}. However, for 3.3V and other low voltage regulators, additional circuitry is required to derive V_{CC} power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ Left Open. This will cause V_{CC} to be powered only from the internal 4.5V regulator resulting in reduced MOSFET gate drive levels and an efficiency penalty of up to 10% at high input voltages.

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2. EXTV$_{CC}$ Connected Directly to V$_{OUT}$. This is the normal connection for a 5V regulator and provides the highest efficiency.
3. EXTV$_{CC}$ Connected to an Output-Derived Boost Network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting EXTV$_{CC}$ to an output-derived voltage which has been boosted to greater than 4.5V. This can be done either with the inductive boost winding shown in Figure 5a or the capacitive charge pump shown in Figure 5b. The charge pump has the advantage of simple magnetics and generally provides the highest efficiency at the expense of a slightly higher parts count.
4. EXTV$_{CC}$ Connected to an External Supply. If an external supply is available in the 5V to 12V range, it may be used to power EXTV$_{CC}$ providing it is compatible with the MOSFET gate drive requirements. There are no restrictions on the EXTV$_{CC}$ voltage relative to V$_{IN}$. EXTV$_{CC}$ may be higher than V$_{IN}$ providing EXTV$_{CC}$ does not exceed the 15V absolute maximum rating.

When driving standard threshold MOSFETs, the external supply must always be present during operation to prevent MOSFET failure due to insufficient gate drive. The LTC1149 family should also be considered for applications which require the use of standard threshold MOSFETs.

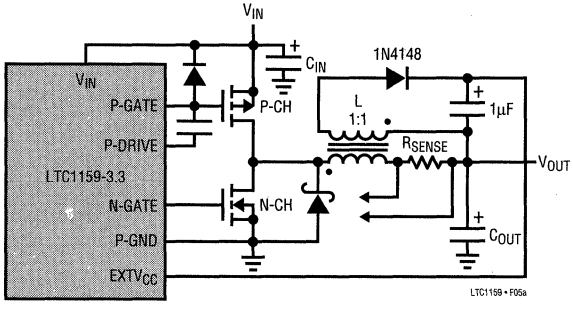

Figure 5a. Inductive Boost Circuit for EXTV$_{CC}$

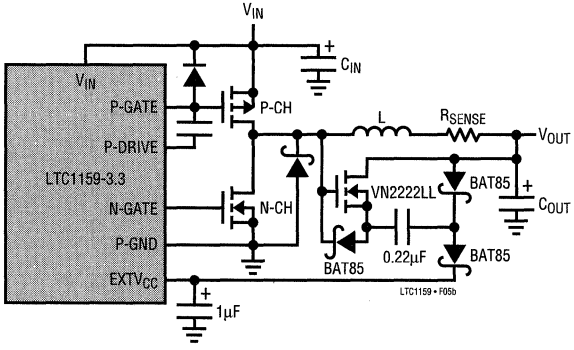

Figure 5b. Capacitive Charge Pump for EXTV$_{CC}$

Important Information About LTC1159 Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1159 adjustable version is used with an external resistive divider from V$_{OUT}$ to the V$_{FB}$ pin (Figure 6). The regulated voltage is determined by:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) 1.25V$$

The V$_{FB}$ pin is extremely sensitive to pickup from the inductor switching node. Care should be taken to isolate the feedback network from the inductor, and the 100pF capacitor should be connected between the V$_{FB}$ and S-GND pins next to the package.

In LTC1159N and LTC1159S applications with V$_{OUT}$ > 5.5V, the V$_{CC}$ pin may self-power through the Sense pins when SHDN2 is taken high, preventing shutdown. In these applications, a pull-down must be added to the Sense$^-$ pin as shown in Figure 6. This pull-down effectively takes the place of the SHDN1 pin, ensuring complete shutdown. Note: For versions in which both the SHDN1 and SHDN2 pins are available (LTC1159G and all fixed output versions), the two pins are simply connected to each other and driven together to guarantee complete shutdown.

The Figure 6 circuit cannot be used to regulate a V$_{OUT}$ which is greater than the maximum voltage allowed on the LTC1159 Sense pins (13V). In applications with V$_{OUT}$ > 13V, R$_{SENSE}$ must be moved to the ground side of the output capacitor and load. This operates the current sense

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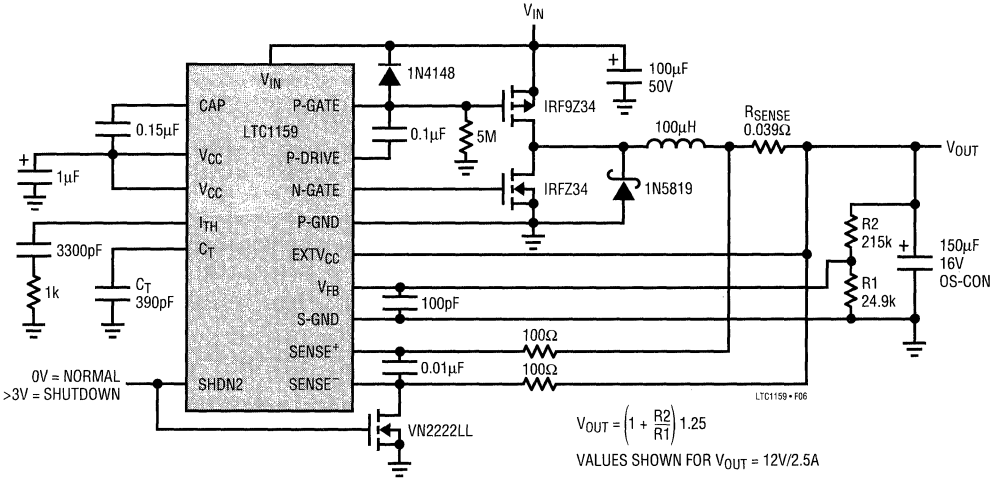

Figure 6. High Efficiency Adjustable Regulator with 5.5V < V_{OUT} < 13V

mparator at 0V common mode, increasing the off-time proximately 40% and requiring the use of a smaller ıing capacitor C_T.

ıerting Regular Applications

e LTC1159 can also be used to obtain negative output ltages from positive inputs. In these inverting applica-ns, the current sense resistor connects to ground while ; LTC1159 and N-channel MOSFET connections, which ıuld normally go to ground, instead ride on the negative tput. This allows the negative output voltage to be set by ; same process as in conventional applications, using ıer the internal divider (LTC1159-3.3, LTC1159-5) or an :ernal divider with the adjustable version.

ure 15 in the Typical Applications shows a synchronous V to –12V converter which can supply up to 1A with :ter than 85% efficiency. By grounding the $EXTV_{CC}$ pin in Figure 15 circuit, the entire 12V output voltage is placed oss the driver and control circuits since the LTC1159 ound pins are at –12V. During start-up or short-circuit ıditions, operating power is supplied by the internal V regulator. The shutdown signal is level-shifted to the gative output rail by Q3, and Q4 ensures that Q1 and Q2 nain off during the entire shutdown sequence.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100 - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1159 circuits: 1) LTC1159 V_{IN} current, 2) LTC1159 V_{CC} current, 3) I^2R losses, and 4) P-channel transition losses.

1. LTC1159 V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<1%) loss which increases with V_{IN}.
2. LTC1159 V_{CC} current is the sum of the MOSFET driver and control circuit currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from

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low to high to low again, a packet of charge dQ moves from V_{CC} to ground. The resulting dQ/dt is a current out of V_{CC} which is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} \approx f (Q_P + Q_N)$, where Q_P and Q_N are the gate charges of the two MOSFETs.

By powering EXTV_{CC} from an output-derived source, the additional V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Efficiency). For example in a 20V to 5V application, 10mA of V_{CC} current results in approximately 3mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode all of the output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 0.1Ω, R_L = 0.15Ω, and R_{SENSE} = 0.05Ω, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll-off at high output currents.
4. Transition losses apply only to the P-channel MOSFET, and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

   Transition Loss $\approx 5(V_{IN})^2(I_{MAX})(C_{RSS})(f)$

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead time, and inductor core losses, generally account for less than 2% total additional loss.

Auxiliary Windings – Suppressing Burst Mode Operation

The LTC1159 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary ou puts may be loaded without regard to the primary outpı load, providing that the loop remains in continuoı mode operation.

Burst Mode operation can be suppressed at low outpı currents with a simple external network which cancels tl 0.025V minimum current comparator threshold. This tecl nique is also useful for eliminating audible noise froı certain types of inductors in high current (I_{OUT} > 5A applications when they are lightly loaded.

An external offset is put in series with the Sense⁻ pin t subtract from the built-in 0.025V offset. An example of th technique is shown in Figure 7. Two 100Ω resistors aı inserted in series with the leads from the sense resisto With the addition of R3, a current is generated through R causing an offset of:

$$V_{OFFSET} = V_{OUT}\left(\frac{R1}{R1 + R3}\right)$$

If V_{OFFSET} > 0.025V, the minimum threshold will b cancelled and Burst Mode operation is prevented froı occurring. Since V_{OFFSET} is constant, the maximum loa current is also decreased by the same offset. Thus, to gı back to the same I_{MAX}, the value of the sense resistor mu: be reduced:

$$R_{SENSE} \approx \frac{75}{I_{MAX}}\ m\Omega$$

To prevent noise spikes from erroneously tripping tl current comparator, a 1000pF capacitor is needed acros the Sense⁻ and Sense⁺ pins.

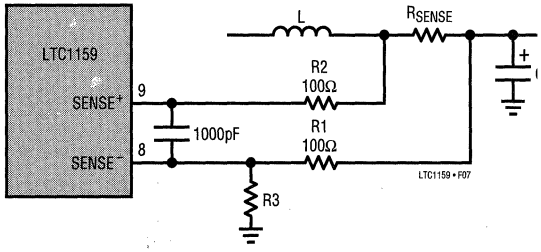

Figure 7. Suppressing Burst Mode Operation

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ard Layout Checklist

ıen laying out the printed circuit board, the following ecklist should be used to ensure proper operation of the C1159. These items are also illustrated graphically in ; layout diagram of Figure 8. Check the following in your 'out:

Are the signal and power grounds segregated? The LTC1159 signal ground must connect separately to the (–) plate of C_{OUT}. The other ground pin(s) should return to the source of the N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.

Does the LTC1159 Sense$^-$ pin connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground.

Are the Sense$^-$ and Sense$^+$ leads routed together with minimum PC trace spacing? The differential decoupling capacitor between the two Sense pins should be as close as possible to the LTC1159. Up to 100Ω may be placed in series with each sense lead to help decouple the Sense pins. However, when these resistors are used, the capacitor should be no larger than 1000pF.

4) Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? An additional 0.1µF ceramic capacitor between V_{IN} and power ground may be required in some applications.

5) Is the V_{CC} decoupling capacitor connected closely between the V_{CC} pins of the LTC1159 and power ground? This capacitor carries the MOSFET driver peak currents.

6) In adjustable versions, the feedback pin is very sensitive to pickup from the switch node. Care must be taken to isolate V_{FB} from possible capacitive coupling of the inductor switch signal.

7) Is the SHDN1 pin actively pulled to ground during normal operation? SHDN1 is a high impedance pin and must not be allowed to float.

4

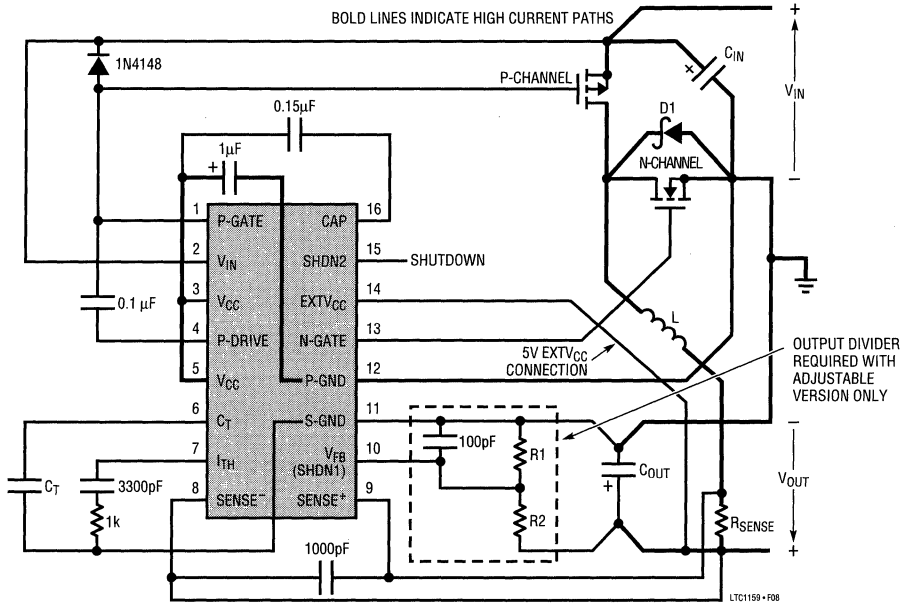


Figure 8. LTC1159 Layout Diagram (N and S Packages)

APPLICATIONS INFORMATION

Troubleshooting Hints

Since efficiency is critical to LTC1159 applications it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the C_T pin .

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a. When the load current is low ($I_{LOAD} < I_{BURST}$), Burst Mode operation should occur with the C_T waveform periodically falling to ground as shown in Figure 9b.

If the C_T pin is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

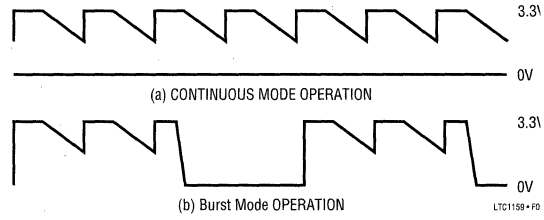
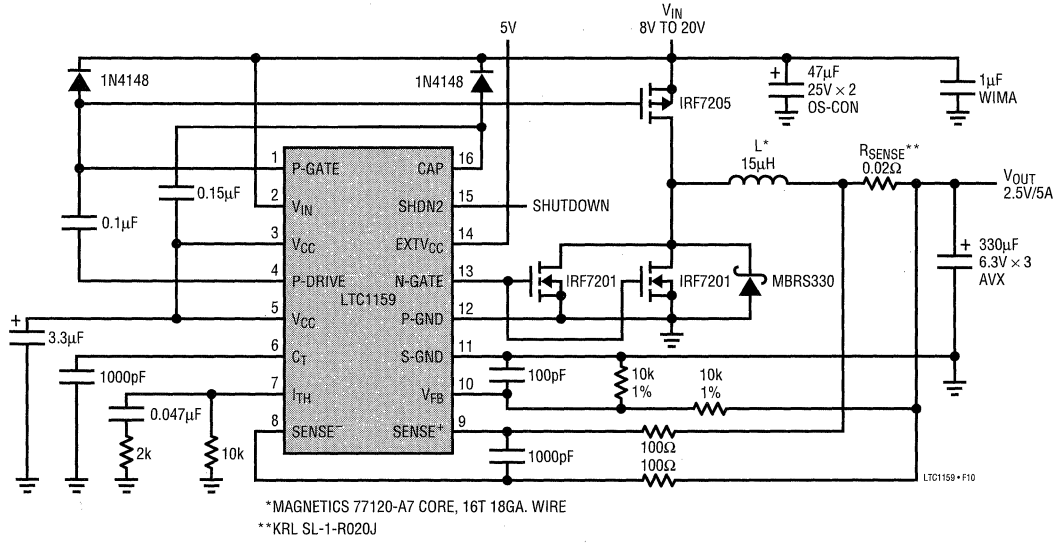


Figure 9. C_T Pin 6 Waveforms

TYPICAL APPLICATIONS



*MAGNETICS 77120-A7 CORE, 16T 18GA. WIRE
**KRL SL-1-R020J

Figure 10. High Efficiency 8V to 20V Input 2.5/5A Output Regulator

YPICAL APPLICATIONS

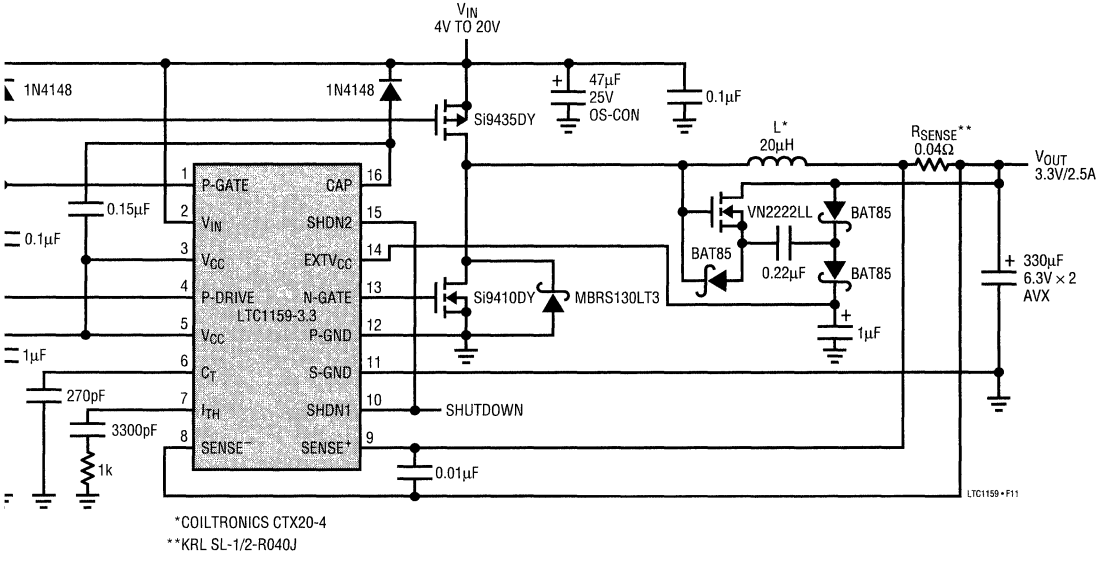


Figure 11. 5:1 Input Range (4V to 20V) High Efficiency 3.3V/2.5A Regulator

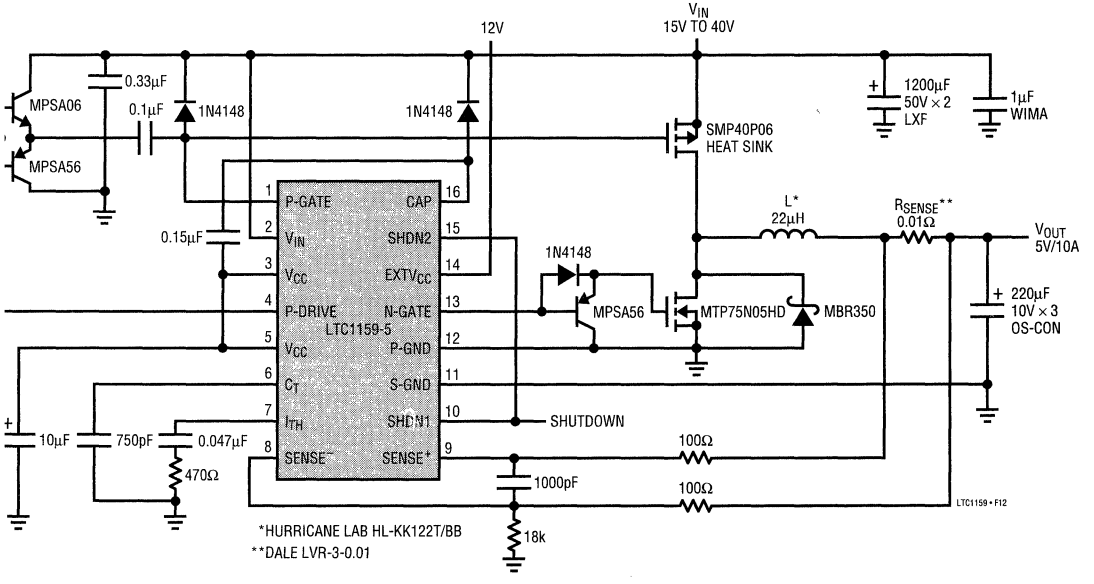


Figure 12. High Current, High Efficiency 15V to 40V Input 5V/10A Output Regulator

TYPICAL APPLICATIONS

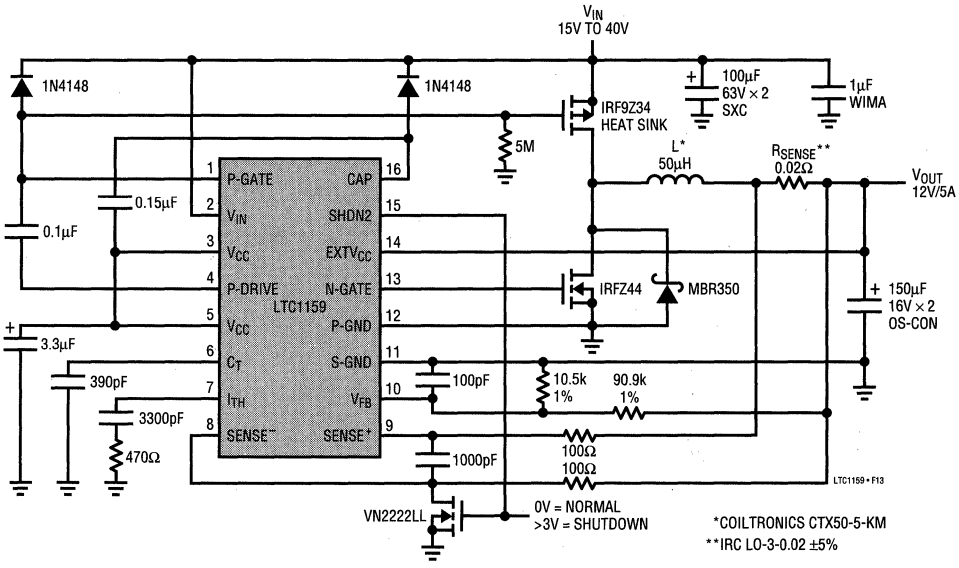


Figure 13. High Efficiency 15V to 40V Input 12V/5A Output Regulator

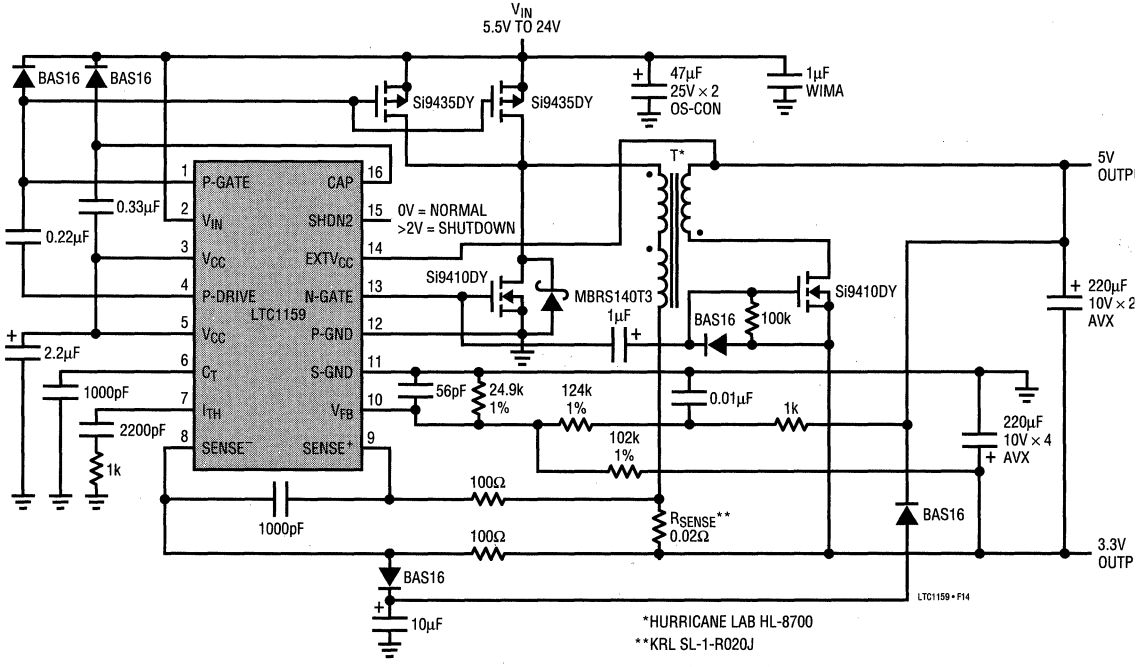


Figure 14. 17W Dual Output High Efficiency 5V and 3.3V Regulator

TYPICAL APPLICATIONS

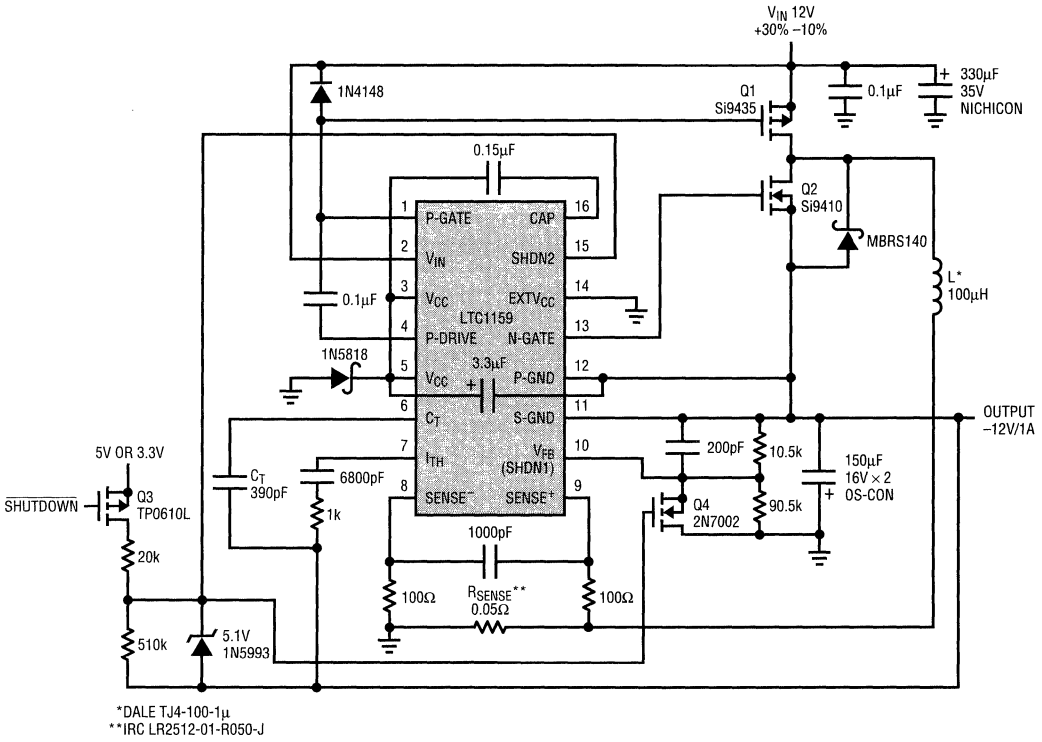


Figure 15. High Efficiency 12V to –12V 1A Converter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142	Dual High Efficiency Synchronous Step-Down Switching Regulator	Dual Version of LTC1148
LTC1143	Dual High Efficiency Step-Down Switching Regulator Controller	Dual Version of LTC1147
LTC1147	High Efficiency Step-Down Switching Regulator Controller	Nonsynchronous, 8-Lead, $V_{IN} \leq 16V$
LTC1148	High Efficiency Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 20V$
LTC1149	High Efficiency Step-Down Switching Regulator	Synchronous, $V_{IN} \leq 48V$, for Standard Threshold FETs
LTC1174	High Efficiency Step-Down and Inverting DC/DC Converter	0.5A Switch, $V_{IN} \leq 18.5V$, Comparator
LTC1265	High Efficiency Step-Down DC/DC Converter	1.2A Switch, $V_{IN} \leq 13V$, Comparator
LTC1267	Dual High Efficiency Synchronous Step-Down Switching Regulators	Dual Version of LTC1159

CCFL/LCD Contrast Switching Regulators

FEATURES

- **Wide Input Voltage Range: 3V to 30V**
- Low Quiescent Current
- High Switching Frequency: 200kHz
- CCFL Switch: 1.25A, LCD Switch: 625mA
- **Grounded or Floating Lamp Configurations**
- **Open-Lamp Protection**
- Positive or Negative Contrast Capability

APPLICATIONS

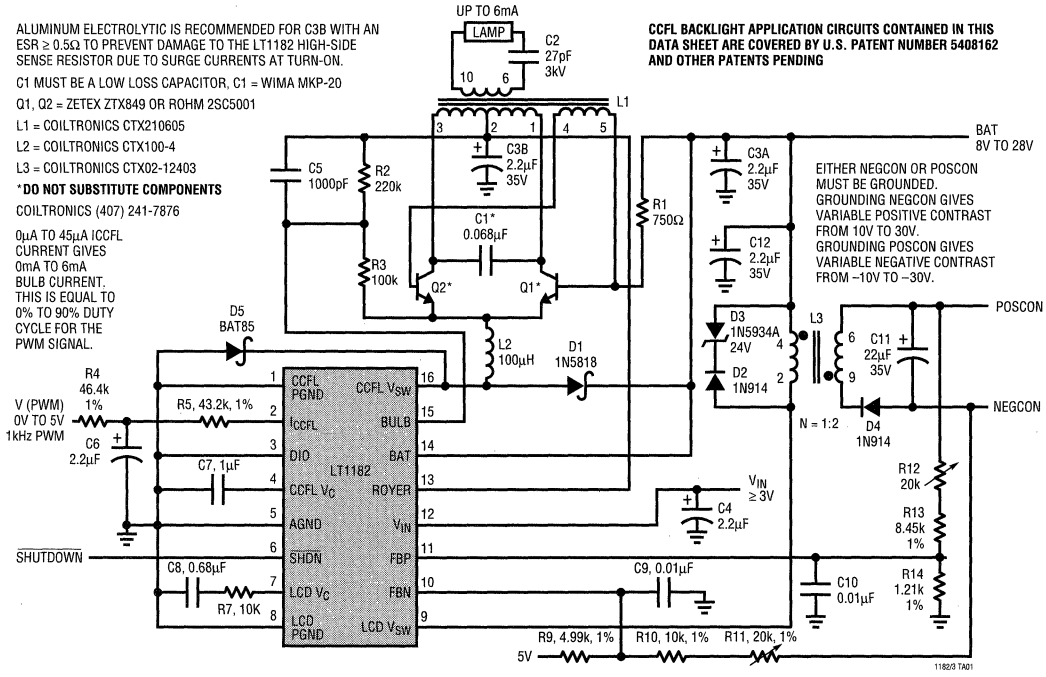
- Notebook and Palmtop Computers
- Portable Instruments
- Automotive Displays
- Retail Terminals

DESCRIPTION

The LT®1182/LT1183 are dual current mode switching regulators that provide the control function for Cold Cathode Fluorescent Lighting (CCFL) and Liquid Crystal Display (LCD) Contrast. The LT1184/LT1184F provide only the CCFL function. The ICs include high current, high efficiency switches, an oscillator, a reference, output drive logic, control blocks and protection circuitry. The LT1182 permits positive or negative voltage LCD contrast operation. The LT1183 permits unipolar contrast operation and pins out an internal reference. The LT1182/LT1183 support grounded and floating lamp configurations. The LT1184F supports grounded and floating lamp configurations. The LT1184 supports only grounded lamp configurations. The

TYPICAL APPLICATION

90% Efficient Floating CCFL Configuration with Dual Polarity LCD Contrast



DESCRIPTION

.T1184/LT1184F pin out the reference for simplified programming of lamp current.

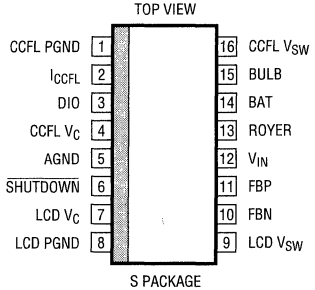
The LT1182/LT1183/LT1184/LT1184F operate with input supply voltages from 3V to 30V. The ICs also have a battery supply voltage pin that operates from 4.5V to 30V. The LT1182/LT1183 draw 9mA typical quiescent current while the LT1184/LT1184F draw 6mA typical quiescent current. An active low shutdown pin typically reduces total supply current to 35µA for standby operation. A 200kHz switching frequency minimizes the size of required magnetic components. The use of current mode switching techniques with cycle-by-cycle limiting gives high reliability and simple loop frequency compensation. The LT1182/LT1183/LT1184/LT1184F are all available in 16-pin narrow SO packages.

ABSOLUTE MAXIMUM RATINGS

V_{IN}, BAT, Royer, Bulb 30V
CCFL V_{SW}, LCD V_{SW} 60V
Shutdown 6V
I_{CCFL} Input Current 10mA
DIO Input Current (Peak, < 100ms) 100mA
LT1182: FBP, FBN, LT1183: FB Pin Current ..... ±2mA
LT1183/LT1184/1184F: REF Pin Source Current 1mA
Junction Temperature (Note 1) ..... 100°C
Operating Ambient Temperature Range ..... 0°C to 100°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

4

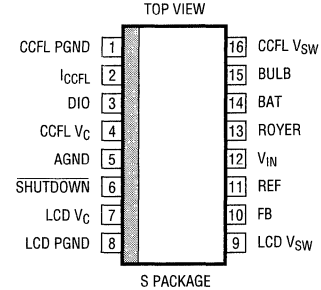
PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

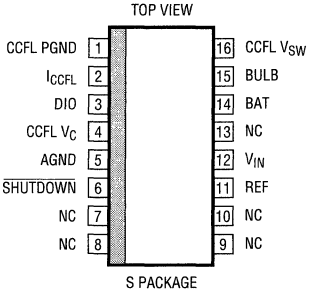
LT1182CS



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

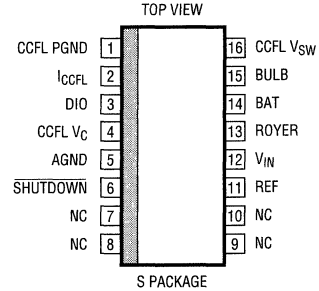
LT1183CS



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1184CS



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LT1184FCS

Consult factory for Industrial and Military grade parts

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 5V, BAT = Royer = Bulb = 12V, I_{CCFL} = $\overline{SHUTDOWN}$ = CCFL V_{SW} = Open, DIO = GND, CCFL V_C = 0.5V, (LT1182/LT1183) LCD V_C = 0.5V, LCD V_{SW} = Open, (LT1182) FBN = FBP = GND, (LT1183) FB = GND, (LT1183/LT1184/LT1184F) REF = Open, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	LT1182/LT1183: 3V ≤ V_{IN} ≤ 30V	●		9	14	mA
		LT1184/LT1184F: 3V ≤ V_{IN} ≤ 30V	●		6	9.5	mA
$I_{\overline{SHDN}}$	$\overline{SHUTDOWN}$ Supply Current	$\overline{SHUTDOWN}$ = 0V, CCFL V_C = LCD V_C = Open (Note 2)			35	70	µA
	$\overline{SHUTDOWN}$ Input Bias Current	$\overline{SHUTDOWN}$ = 0V, CCFL V_C = LCD V_C = Open			3	6	µA
	$\overline{SHUTDOWN}$ Threshold Voltage		●	0.6	0.85	1.2	V
f	Switching Frequency	Measured at CCFL V_{SW} and LCD V_{SW}, I_{SW} = 50mA, I_{CCFL} = 100µA, CCFL V_C = Open, (LT1182) FBN = FBP = 1V, (LT1183) FB = 1V, (LT1182/LT1183) LCD V_C = Open		175	200	225	kHz
			●	160	200	240	kHz
DC(MAX)	Maximum Switch Duty Cycle	Measured at CCFL V_{SW} and LCD V_{SW}		80	85		%
			●	75	85		%
BV	Switch Breakdown Voltage	Measured at CCFL V_{SW} and LCD V_{SW}		60	70		V
	Switch Leakage Current	V_{SW} = 12V, Measured at CCFL V_{SW} and LCD V_{SW}				20	µA
		V_{SW} = 30V, Measured at CCFL V_{SW} and LCD V_{SW}				40	µA
	I_{CCFL} Summing Voltage	3V ≤ V_{IN} ≤ 30V, Measured on LT1182/LT1183		0.41	0.45	0.49	V
			●	0.37	0.45	0.54	V
		3V ≤ V_{IN} ≤ 30V, Measured on LT1184/LT1184F		0.425	0.465	0.505	V
			●	0.385	0.465	0.555	V
	ΔI_{CCFL} Summing Voltage for ΔInput Programming Current	I_{CCFL} = 0µA to 100µA			5	15	mV
	CCFL V_C Offset Sink Current	CCFL V_C = 1.5V, Positive Current Measured into Pin		–5	5	15	µA
	ΔCCFL V_C Source Current for ΔI_{CCFL} Programming Current	I_{CCFL} = 25µA, 50µA, 75µA, 100µA, CCFL V_C = 1.5V	●	4.70	4.95	5.20	µA/µA
	CCFL V_C to DIO Current Servo Ratio	DIO = 5mA out of Pin, Measure I_{VC} at CCFL V_C = 1.5V	●	94	99	104	µA/mA
	CCFL V_C Low Clamp Voltage	V_{BAT} – V_{BULB} = Bulb Protect Servo Voltage	●		0.1	0.3	V
	CCFL V_C High Clamp Voltage	I_{CCFL} = 100µA	●	1.7	2.1	2.4	V
	CCFL V_C Switching Threshold	CCFL V_{SW} DC = 0%	●	0.6	0.95	1.3	V
	CCFL High-Side Sense Servo Current	I_{CCFL} = 100µA, I_{VC} = 0µA at CCFL V_C = 1.5V	●	0.93	1.00	1.07	A
	CCFL High-Side Sense Servo Current Line Regulation	BAT = 5V to 30V, I_{CCFL} = 100µA, I_{VC} = 0µA at CCFL V_C = 1.5V			0.1	0.16	%/V
	CCFL High-Side Sense Supply Current	Current Measured into BAT and Royer Pins	●	50	100	150	µA
	Bulb Protect Servo Voltage	I_{CCFL} = 100µA, I_{VC} = 0µA at CCFL V_C = 1.5V, Servo Voltage Measured Between BAT and Bulb Pins	●	6.5	7.0	7.5	V
	Bulb Input Bias Current	I_{CCFL} = 100µA, I_{VC} = 0µA at CCFL V_C = 1.5V			5	9	µA
I_{LIM1}	CCFL Switch Current Limit	Duty Cycle = 50%	●	1.25	1.9	3.0	A
		Duty Cycle = 75% (Note 3)	●	0.9	1.6	2.6	A
V_{SAT1}	CCFL Switch On-Resistance	CCFL I_{SW} = 1A	●		0.6	1.0	Ω
$\frac{\Delta I_Q}{\Delta I_{SW1}}$	Supply Current Increase During CCFL Switch On-Time	CCFL I_{SW} = 1A			20	30	mA/A
V_{REF}	Reference Voltage	Measured at REF (Pin 11) on LT1183/LT1184/LT1184F		1.224	1.244	1.264	V
			●	1.214	1.244	1.274	V
	Reference Output Impedance	Measured at REF (Pin 11) on LT1183	●	20	45	70	Ω
		Measured at REF (Pin 11) on LT1184/LT1184F	●	5	15	30	Ω

ELECTRICAL CHARACTERISTICS

$_A$ = 25°C, V_{IN} = 5V, BAT = Royer = Bulb = 12V, I_{CCFL} = $\overline{SHUTDOWN}$ = CCFL V_{SW} = Open, DIO = GND, CCFL V_C = 0.5V, .T1182/LT1183) LCD V_C = 0.5V, LCD V_{SW} = Open, (LT1182) FBN = FBP = GND, (LT1183) FB = GND, .T1183/LT1184/LT1184F) REF = Open, unless otherwise specified.

YMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	$V_{REF} - I_{CCFL}$ Summing Voltage	Measured on LT1183		0.760	0.795	0.830	V
			●	0.725	0.795	0.865	V
	$V_{REF} - I_{CCFL}$ Summing Voltage	Measured on LT1184/LT1184F		0.740	0.775	0.810	V
			●	0.705	0.775	0.845	V
EF1	LCD FBP/FB Reference Voltage	LT1182: Measured at FBP Pin, FBN = 1V, LCD V_C = 0.8V		1.224	1.244	1.264	V
		LT1183: Measured at FB Pin, LCD V_C = 0.8V	●	1.214	1.244	1.274	V
	REF1 Voltage Line Regulation	$3V \le V_{IN} \le 30V$, LCD V_C = 0.8V	●		0.01	0.03	%/V
	FBP/FB Input Bias Current	LT1182: FBP = REF1, FBN = 1V, LCD V_C = 0.8V					
		LT1183: FB = REF1, LCD V_C = 0.8V	●		0.35	1.0	µA
	LCD FBN/FB Offset Voltage	LT1182: Measured at FBN Pin, FBP = 0V, LCD V_C = 0.8V		−20	−12	−4	mV
		LT1183: Measured at FB Pin, LCD V_C = 0.8V	●	−27	−12	−1	mV
	Offset Voltage Line Regulation	$3V \le V_{IN} \le 30V$, LCD V_C = 0.8V	●		0.01	0.2	%/V
	FBN/FB Input Bias Current	LT1182: FBN = Offset Voltage, FBP = 0V, LCD V_C = 0.8V					
		LT1183: FB = Offset Voltage, LCD V_C = 0.8V	●	−3.0	−1.0		µA
η	FBP/FB to LCD V_C Transconductance	LT1182: ΔI_{VC} = ±25µA, FBN = 1V		650	900	1150	µmhos
		LT1183: ΔI_{VC} = ±25µA	●	500	900	1300	µmhos
	FBN/FB to LCD V_C Transconductance	LT1182: ΔI_{VC} = ±25µA, FBP = GND		550	800	1050	µmhos
		LT1183: ΔI_{VC} = ±25µA	●	400	800	1200	µmhos
	LCD Error Amplifier Source Current	LT1182: FBP = FBN = 1V or 0.25V,	●	50	100	175	µA
		LT1183: FB = 1V or 0.25V					
	LCD Error Amplifier Sink Current	LT1182: FBP = FBN = 1.5V or −0.25V,	●	35	100	175	µA
		LT1183: FB = 1.5V or −0.25V					
	LCD V_C Low Clamp Voltage	LT1182: FBP = FBN = 1.5V, LT1183: FB = 1.5V			0.01	0.3	V
	LCD V_C High Clamp Voltage	LT1182: FBP = FBN = 1V, LT1183: FB = 1V		1.7	2.0	2.4	V
	LCD V_C Switching Threshold	LT1182: FBP = FBN = 1V, LT1183: FB = 1V, V_{SW} DC = 0%		0.6	0.95	1.3	V
IM2	LCD Switch Current Limit	Duty Cycle = 50%	●	0.625	1.00	1.5	A
		Duty Cycle = 75% (Note 3)	●	0.400	0.85	1.3	A
SAT2	LCD Switch On-Resistance	LCD I_{SW} = 0.5A	●		1.0	1.65	Ω
ΔI_Q / I_{SW2}	Supply Current Increase During LCD Switch On-Time	LCD I_{SW} = 0.5A			20	30	mA/A
	Switch Minimum On-Time	Measured at CCFL V_{SW} and LCD V_{SW}			0.45		µs

ıe ● denotes specifications which apply over the specified operating mperature range.

ote 1: T_J is calculated from the ambient temperature T_A and power ssipation P_D according to the following formula:

T1182CS/LT1183CS/LT1184CS/LT1184FCS: $T_J = T_A + (P_D \times 100°C/W)$

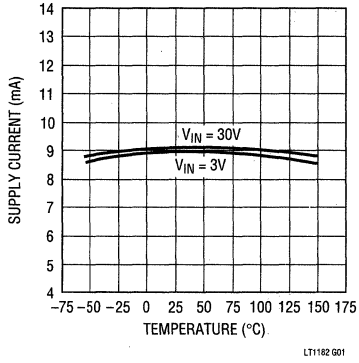
Note 2: Does not include switch leakage.

Note 3: For duty cycles (DC) between 50% and 75%, minimum guaranteed switch current is given by $I_{LIM} = 1.4(1.393 - DC)$ for the CCFL regulator and $I_{LIM} = 0.7(1.393 - DC)$ for the LCD contrast regulator due to internal slope compensation circuitry.

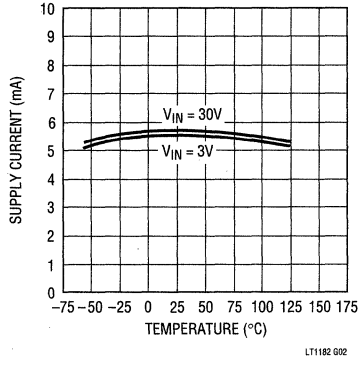
4

TYPICAL PERFORMANCE CHARACTERISTICS

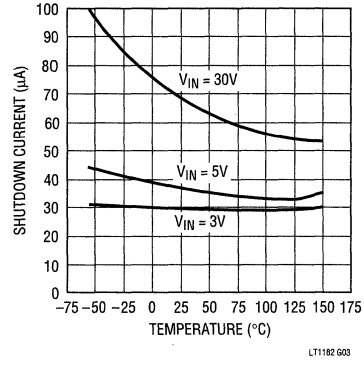
LT1182/LT1183 Supply Current vs Temperature



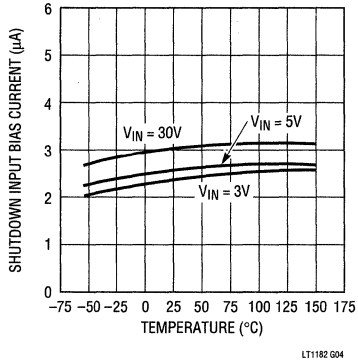
LT1184/LT1184F Supply Current vs Temperature



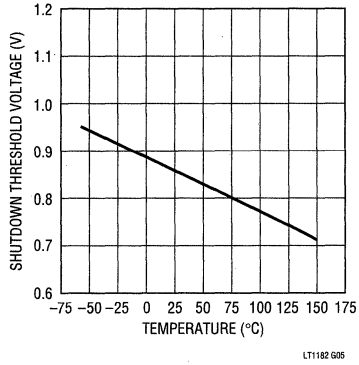
Shutdown Current vs Temperature



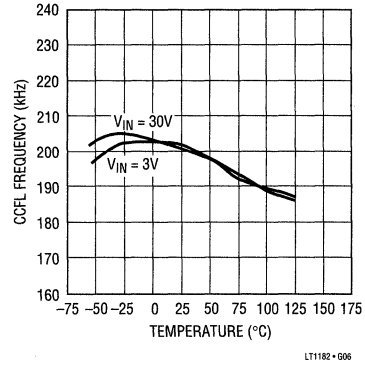
Shutdown Input Bias Current vs Temperature



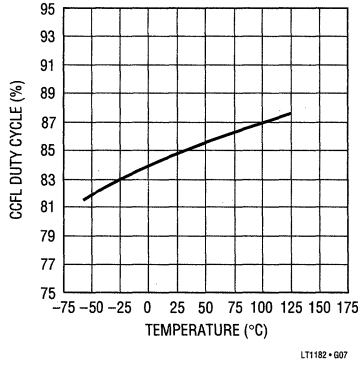
Shutdown Threshold Voltage vs Temperature



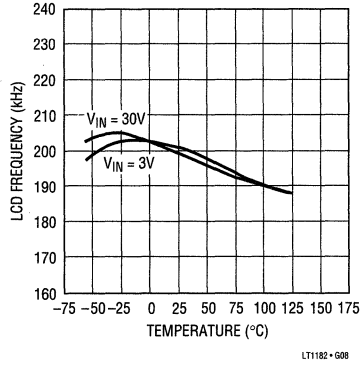
CCFL Frequency vs Temperature



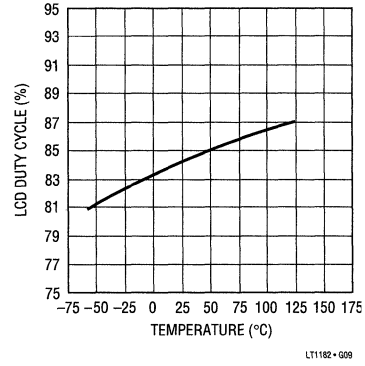
CCFL Duty Cycle vs Temperature



LCD Frequency vs Temperature

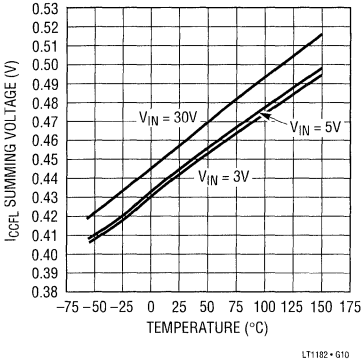


LCD Duty Cycle vs Temperature

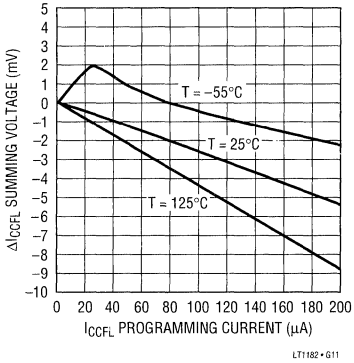


TYPICAL PERFORMANCE CHARACTERISTICS

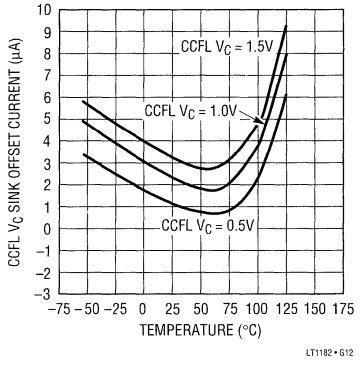
I_{CCFL} Summing Voltage vs Temperature



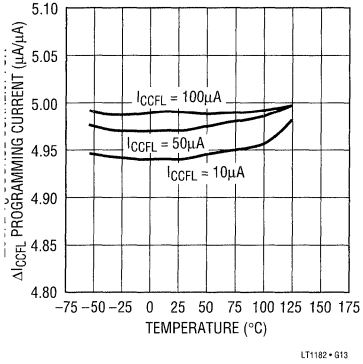
I_{CCFL} Summing Voltage Load Regulation



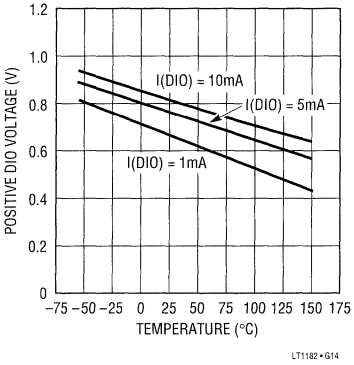
CCFL V_C Offset Sink Current vs Temperature



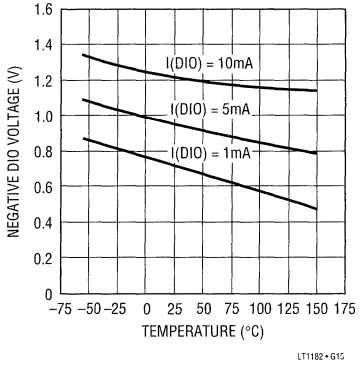
ΔCCFL V_C Source Current for ΔI_{CCFL} Programming Current vs Temperature



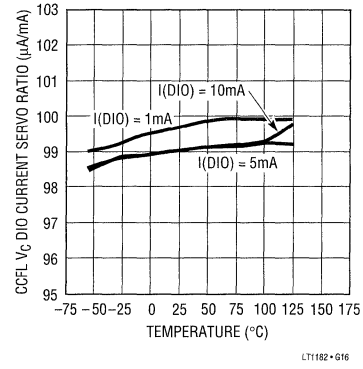
Positive DIO Voltage vs Temperature



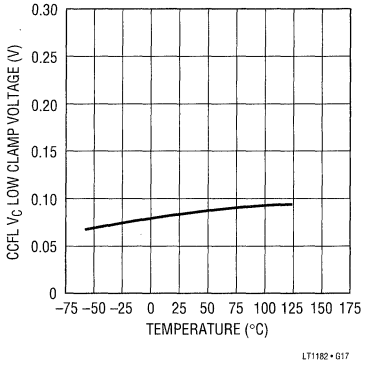
Negative DIO Voltage vs Temperature



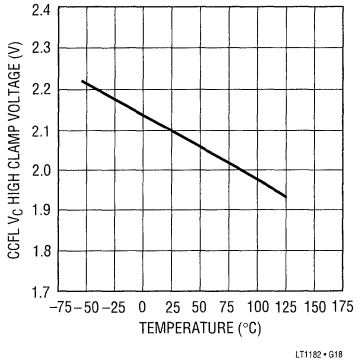
CCFL V_C to DIO Current Servo Ratio vs Temperature



CCFL V_C Low Clamp Voltage vs Temperature

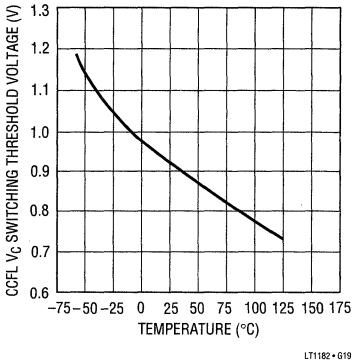


CCFL V_C High Clamp Voltage vs Temperature



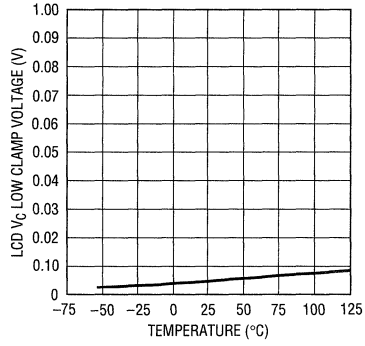
TYPICAL PERFORMANCE CHARACTERISTICS

CCFL V_C Switching Threshold Voltage vs Temperature



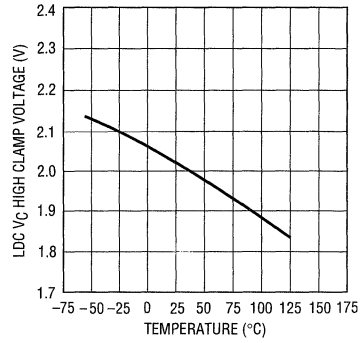
LT1182 • G19

LCD V_C Low Clamp Voltage vs Temperature



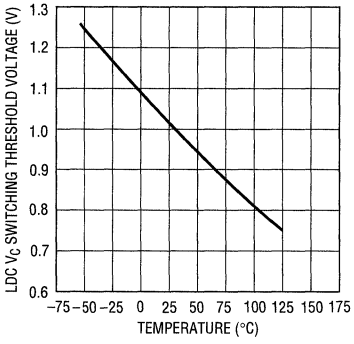
LT1182 • G20

LCD V_C High Clamp Voltage vs Temperature



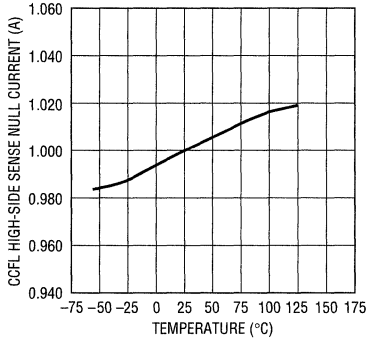
LT1182 • G21

LCD V_C Switching Threshold Voltage vs Temperature



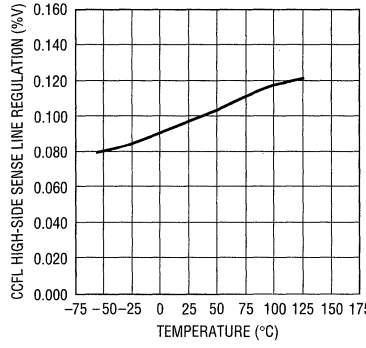
LT1182 • G22

CCFL High-Side Sense Null Current vs Temperature



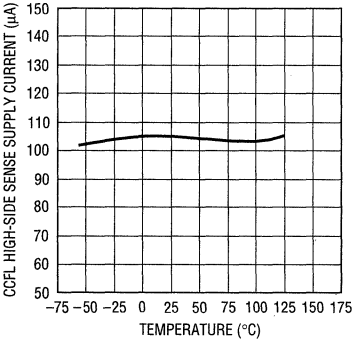
LT1182 • G23

CCFL High-Side Sense Null Current Line Regulation vs Temperature



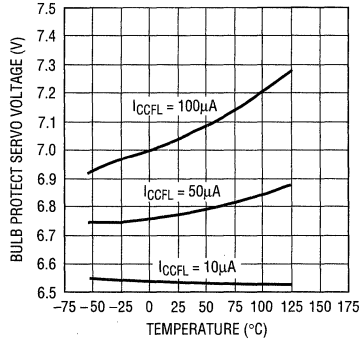
LT1182 • G24

CCFL High-Side Sense Supply Current vs Temperature



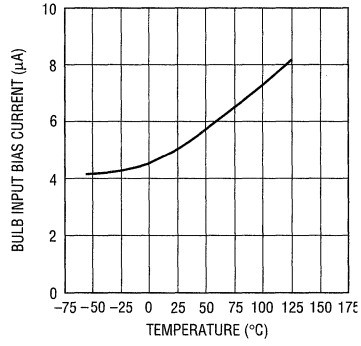
LT1182 • G25

Bulb Protect Servo Voltage vs Temperature



LT1182 • G26

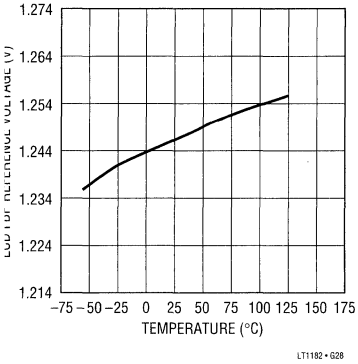
Bulb Input Bias Current vs Temperature



LT1182 • G27

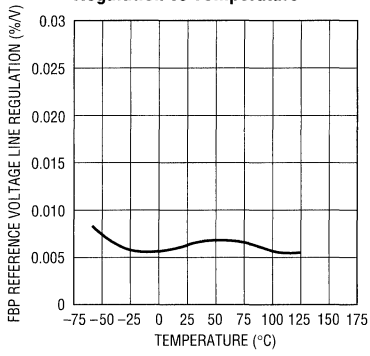
TYPICAL PERFORMANCE CHARACTERISTICS

LCD FBP Reference vs Temperature



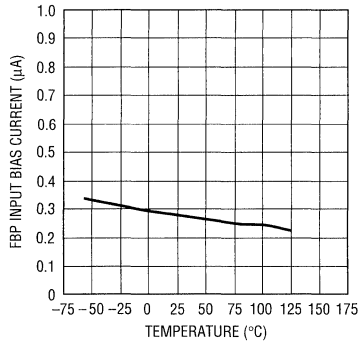
LT1182 • G28

FBP Reference Voltage Line Regulation vs Temperature



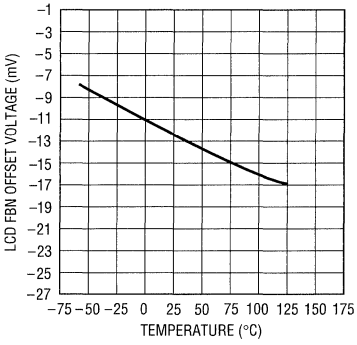
LT1182 • G29

FBP Input Bias Current vs Temperature

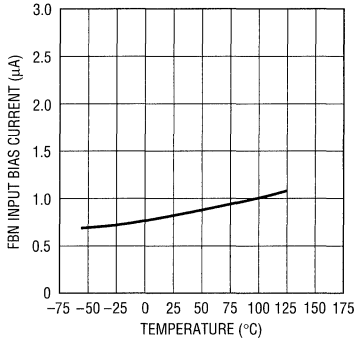


LT1182 • G30

LCD FBN Offset Voltage vs Temperature

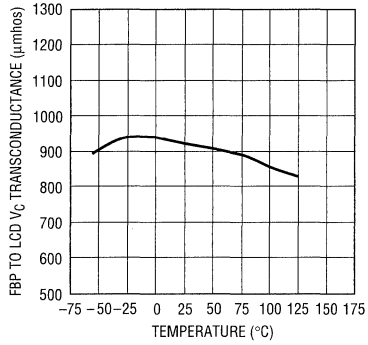


FBN Input Bias Current vs Temperature



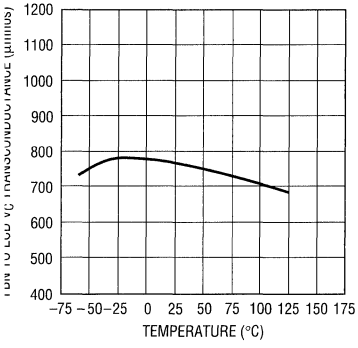
LT1182 • G32

FBP to LCD V_C Transconductance vs Temperature



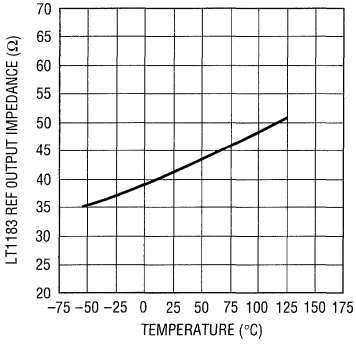
LT1182 • G33

FBN to LCD V_C Transconductance vs Temperature



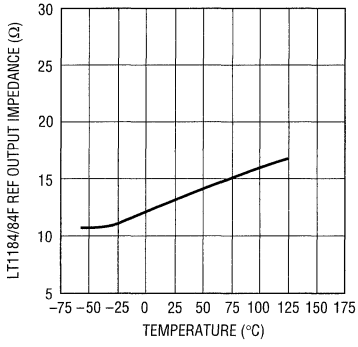
LT1182 • G34

LT1183 REF Output Impedance vs Temperature



LT1182 • G35

LT1184/84F REF Output Impedance vs Temperature

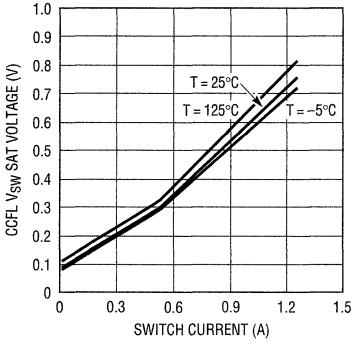


LT1182 • G36

4

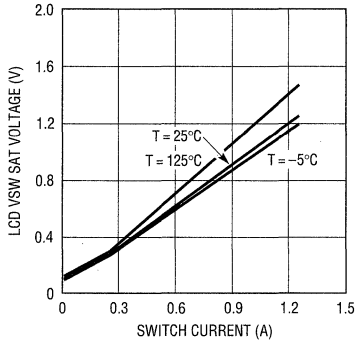
TYPICAL PERFORMANCE CHARACTERISTICS

CCFL V_{SW} Sat Voltage vs Switch Current



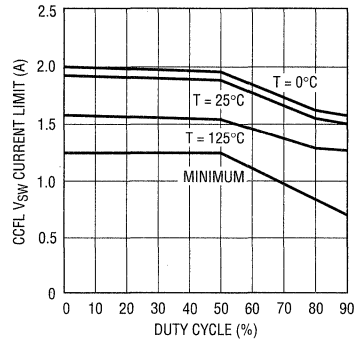
LT1182 • G37

LCD V_{SW} Sat Voltage vs Switch Current



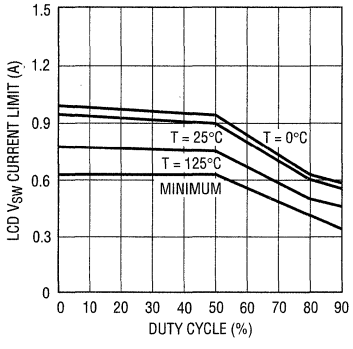
LT1182 • G38

CCFL V_{SW} Current Limit vs Duty Cycle



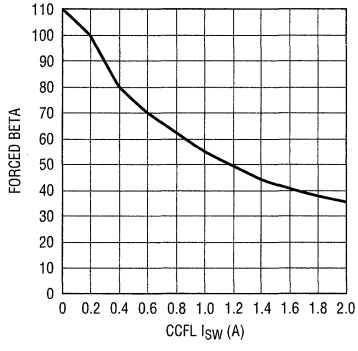
LT1182 • G39

LCD V_{SW} Current Limit vs Duty Cycle



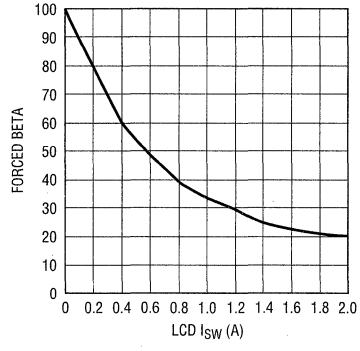
LT1182 • G40

Forced Beta vs I_{SW} on CCFL V_{SW}



LT1182 • G41

Forced Beta vs I_{SW} on LCD V_{SW}



LT1182 • G42

PIN FUNCTIONS

LT1182/LT1183/LT1184/LT1184F

CCFL PGND (Pin 1): This pin is the emitter of an internal NPN power switch. CCFL switch current flows through this pin and permits internal, switch-current sensing. The regulators provide a separate analog ground and power ground(s) to isolate high current ground paths from low current signal paths. Linear Technology recommends the use of star-ground layout techniques.

I_{CCFL} (Pin 2): This pin is the input to the CCFL lamp current programming circuit. This pin internally regulates to 450mV (LT1182/LT1183) or 465mV (LT1184/LT1184F). The pin accepts a DC input current signal of 0μA to 100μA full scale. This input signal is converted to a 0μA to 500μA source current at the CCFL V_C pin. By shunt regulating the I_{CCFL} pin, the input programming current can be set with DAC, PWM or potentiometer control. As input programming current increases, the regulated lamp current increases. For a typical 6mA lamp, the range of input programming current is about 0μA to 50μA.

DIO (Pin 3): This pin is the common connection between the cathode and anode of two internal diodes. The remaining terminals of the two diodes connect to ground. In a grounded lamp configuration, DIO connects to the low voltage side of the lamp. Bidirectional lamp current flows in the DIO pin and thus the diodes conduct alternately on half cycles. Lamp current is controlled by monitoring one-half of the average lamp current. The diode conducting on negative half cycles has one-tenth of its current diverted to the CCFL V_C pin. This current nulls against the source current provided by the lamp-current programmer circuit. A single capacitor on the CCFL V_C pin provides both stable loop compensation and an averaging function to the half-wave-rectified sinusoidal lamp current. Therefore, input programming current relates to one-half of average lamp current. This scheme reduces the number of loop compensation components and permits faster loop transient response in comparison to previously published circuits. If a floating-lamp configuration is used, ground the DIO pin.

CCFL V_C (Pin 4): This pin is the output of the lamp current programmer circuit and the input of the current comparator for the CCFL regulator. Its uses include frequency compensation, lamp-current averaging for grounded lamp circuits, and current limiting. The voltage on the CCFL V_C pin determines the current trip level for switch turnoff. During normal operation this pin sits at a voltage between 0.95V (zero switch current) and 2.0V (maximum switch current) with respect to analog ground (AGND). This pin has a high impedance output and permits external voltage clamping to adjust current limit. A single capacitor to ground provides stable loop compensation. This simplified loop compensation method permits the CCFL regulator to exhibit single-pole transient response behavior and virtually eliminates transformer output overshoot.

AGND (Pin 5): This pin is the low current analog ground. It is the negative sense terminal for the internal 1.24V reference and the I_{CCFL} summing voltage in the LT1182/LT1183/LT1184/LT1184F. It is also a sense terminal for the LCD dual input error amplifier in the LT1182/LT1183. Connect external feedback divider networks that terminate to ground and frequency compensation components that terminate to ground directly to this pin for best regulation and performance.

$\overline{\text{SHUTDOWN}}$ (Pin 6): Pulling this pin low causes complete regulator shutdown with quiescent current typically reduced to 35μA. The nominal threshold voltage for this pin is 0.85V. If the pin is not used, it can float high or be pulled to a logic high level (maximum of 6V). Carefully evaluate active operation when allowing the pin to float high. Capacitive coupling into the pin from switching transients could cause erratic operation.

CCFL V_{SW} (Pin 16): This pin is the collector of the internal NPN power switch for the CCFL regulator. The power switch provides a minimum of 1.25A. Maximum switch current is a function of duty cycle as internal slope compensation ensures stability with duty cycles greater than 50%. Using a driver loop to automatically adapt base drive current to the minimum required to keep the switch in a quasi-saturation state yields fast switching times and high efficiency operation. The ratio of switch current to driver current is about 50:1.

PIN FUNCTIONS

Bulb (Pin 15): This pin connects to the low side of a 7V threshold comparator between the BAT and Bulb pins. This circuit sets the maximum voltage level across the primary side of the Royer converter under all operating conditions and limits the maximum secondary output under start-up conditions or open lamp conditions. This eases transformer voltage rating requirements. Set the voltage limit to insure lamp start-up with worst-case, lamp start voltages and cold-temperature system operating conditions. The Bulb pin connects to the junction of an external divider network. The divider network connects from the center tap of the Royer transformer or the actual battery supply voltage to the top side of the current source "tail inductor". A capacitor across the top of the divider network filters switching ripple and sets a time constant that determines how quickly the clamp activates. When the comparator activates, sink current is generated to pull the CCFL V_C pin down. This action transfers the entire regulator loop from current mode operation into voltage mode operation.

BAT (Pin 14): This pin connects to the battery or battery charger voltage from which the CCFL Royer converter and LCD contrast converter operate. This voltage is typically higher than the V_{IN} supply voltage but can be equal or less than V_{IN}. However, the BAT voltage must be at least 2.1V greater than the internal 2.4V regulator or 4.5V minimum up to 30V maximum. This pin provides biasing for the lamp current programming block, is used with the Royer pin for floating lamp configurations, and connects to one input for the open lamp protection circuitry. For floating lamp configurations, this pin is the noninverting terminal of a high-side current sense amplifier. The typical quiescent current is 50µA into the pin. The BAT and Royer pins monitor the primary side Royer converter current through an internal 0.1Ω top side current sense resistor. A 0A to 1A primary side, center tap converter current is translated to an input signal range of 0mV to 100mV for the current sense amplifier. This input range translates to a 0µA to 500µA sink current at the CCFL V_C pin that nulls against the source current provided by the programmer circuit. The BAT pin also connects to the top side of an internal clamp between the BAT and Bulb pins.

Royer (Pin 13): This pin connects to the center-tapped primary of the Royer converter and is used with the BAT pin in a floating lamp configuration where lamp current is controlled by sensing Royer primary side converter current. This pin is the inverting terminal of a high-side current sense amplifier. The typical quiescent current is 50µA into the pin. If the CCFL regulator is not used in a floating lamp configuration, tie the Royer and BAT pins together. This pin is only available on the LT1182/LT1183/LT1184F.

V_{IN} (Pin 12): This pin is the supply pin for the LT1182/LT1183/LT1184/LT1184F. The ICs accept an input voltage range of 3V minimum to 30V maximum with little change in quiescent current (zero switch current). An internal, low dropout regulator provides a 2.4V supply for most of the internal circuitry. Supply current increases as switch current increases at a rate approximately 1/50 of switch current. This corresponds to a forced Beta of 50 for each switch. The ICs incorporate undervoltage lockout by sensing regulator dropout and lockout switching for input voltages below 2.5V. Hysteresis is not used to maximize the useful range of input voltage. The typical input voltage is a 3.3V or 5V logic supply.

LT1182/LT1183

LCD V_C (Pin 7): This pin is the output of the LCD contrast error amplifier and the input of the current comparator for the LCD contrast regulator. Its uses include frequency compensation and current limiting. The voltage on the LCD V_C pin determines the current trip level for switch turnoff. During normal operation, this pin sits at a voltage between 0.95V (zero switch current) and 2.0V (maximum switch current). The LCD V_C pin has a high impedance output and permits external voltage clamping to adjust current limit. A series R/C network to ground provides stable loop compensation.

LCD PGND (Pin 8): This pin is the emitter of an internal NPN power switch. LCD contrast switch current flows through this pin and permits internal, switch-current sensing. The regulators provide a separate analog ground and power ground(s) to isolate high current ground paths from low current signal paths. Linear Technology recommends star-ground layout techniques.

PIN FUNCTIONS

LCD V_{SW} (Pin 9): This pin is the collector of the internal NPN power switch for the LCD contrast regulator. The power switch provides a minimum of 625mA. Maximum switch current is a function of duty cycle as internal slope compensation ensures stability with duty cycles greater than 50%. Using a driver loop to automatically adapt base drive current to the minimum required to keep the switch in a quasi-saturation state yields fast switching times and high efficiency operation. The ratio of switch current to driver current is about 50:1.

LT1182

FBN (Pin 10): This pin is the noninverting terminal for the negative contrast control error amplifier. The inverting terminal is offset from ground by –12mV and defines the error amplifier output state under start-up conditions. The FBN pin acts as a summing junction for a resistor divider network. Input bias current for this pin is typically 1μA flowing out of the pin. If this pin is not used, force FBN to greater than 0.5V to deactivate the negative contrast control input stage. The proximity of FBN to the LCD V_{SW} pin makes it sensitive to ringing on the switch pin. A small capacitor (0.01μF) from FBN to ground filters switching ripple.

FBP (Pin 11): This pin is the inverting terminal for the positive contrast control error amplifier. The noninverting terminal is tied to an internal 1.244V reference. Input bias current for this pin is typically 0.5μA flowing into the pin. If this pin is not used, ground FBP to deactivate the positive contrast control input stage. The proximity of FBP to the LCD V_{SW} pin makes it sensitive to ringing on the switch pin. A small capacitor (0.01μF) from FBP to ground filters switching ripple.

LT1183

FB (Pin 10): This pin is the common connection between the noninverting terminal for the negative contrast error amplifier and the inverting terminal for the positive-contrast error amplifier. In comparison to the LT1182, the FBN and the FBP pins tie together and come out as one pin. This scheme permits one polarity of contrast to be regulated. The proximity of FB to the LCD V_{SW} pin makes it sensitive to ringing on the switch pin. A small capacitor (0.01μF) from FB to ground filters switching ripple.

The FB pin requires attention to start-up conditions when generating negative contrast voltages. The pin has two stable operating points; regulating to 1.244V for positive contrast voltages or regulating to –12mV for negative contrast voltages. Under start-up conditions, the FB pin heads to a positive voltage. If negative contrast voltages are generated, tie a diode from the FB pin to ground. This ensures that the FB pin will clamp before reaching the positive reference voltage. Switching action then pulls the FB pin back to its normal servo voltage.

LT1183/LT1184/LT1184F

REF (Pin 11): This pin brings out the 1.244V reference. Its functions include the programming of negative contrast voltages with an external resistor divider network (LT1183 only) and the programming of lamp current for the I_{CCFL} pin. LTC does not recommend using the REF pin for both functions at once. The REF pin has a typical output impedance of 45Ω on the LT1183 and a typical output impedance of 15Ω on the LT1184/LT1184F. Reference load current should be limited to a few hundred microamperes, otherwise reference regulation will be degraded. REF is used to generate the maximum programming current for the I_{CCFL} pin by placing a resistor between the pins. PWM or DAC control subtracts from the maximum programming current. A small decoupling capacitor (0.1uF) is recommended to filter switching transients.

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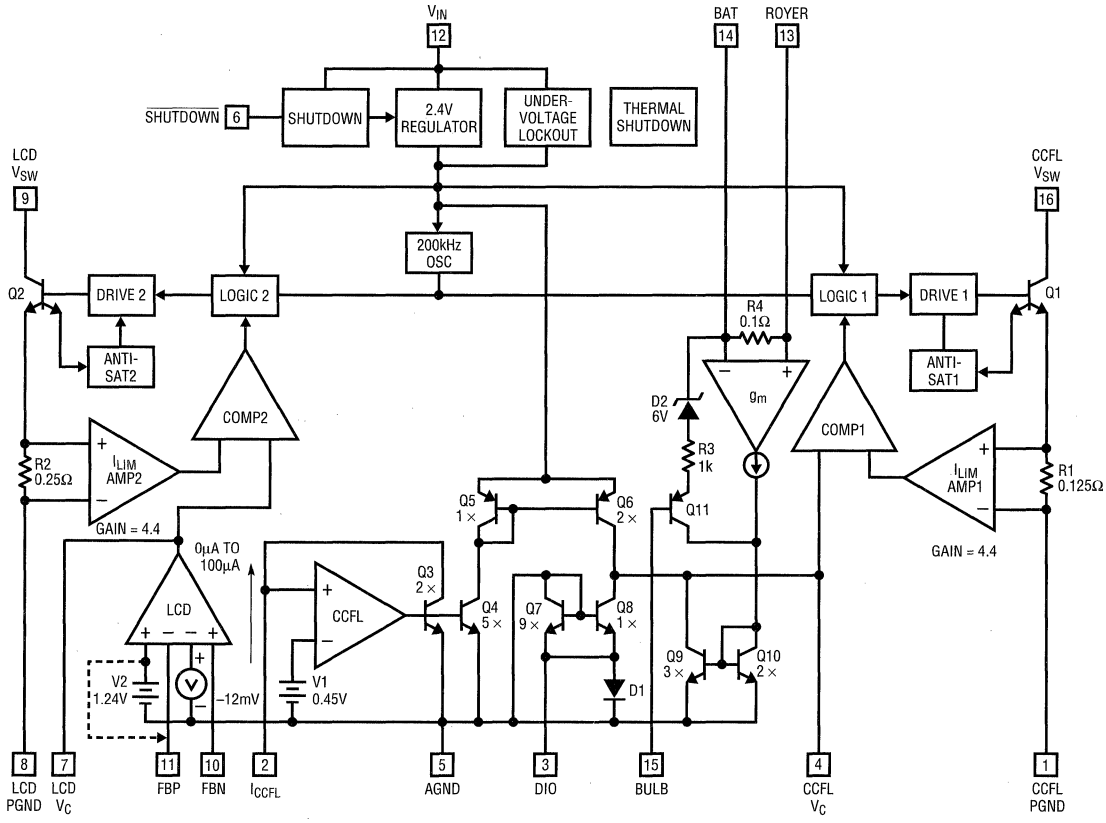
BLOCK DIAGRAM

LT1182/LT1183 CCFL/LCD Contrast Regulator Top Level Block Diagram

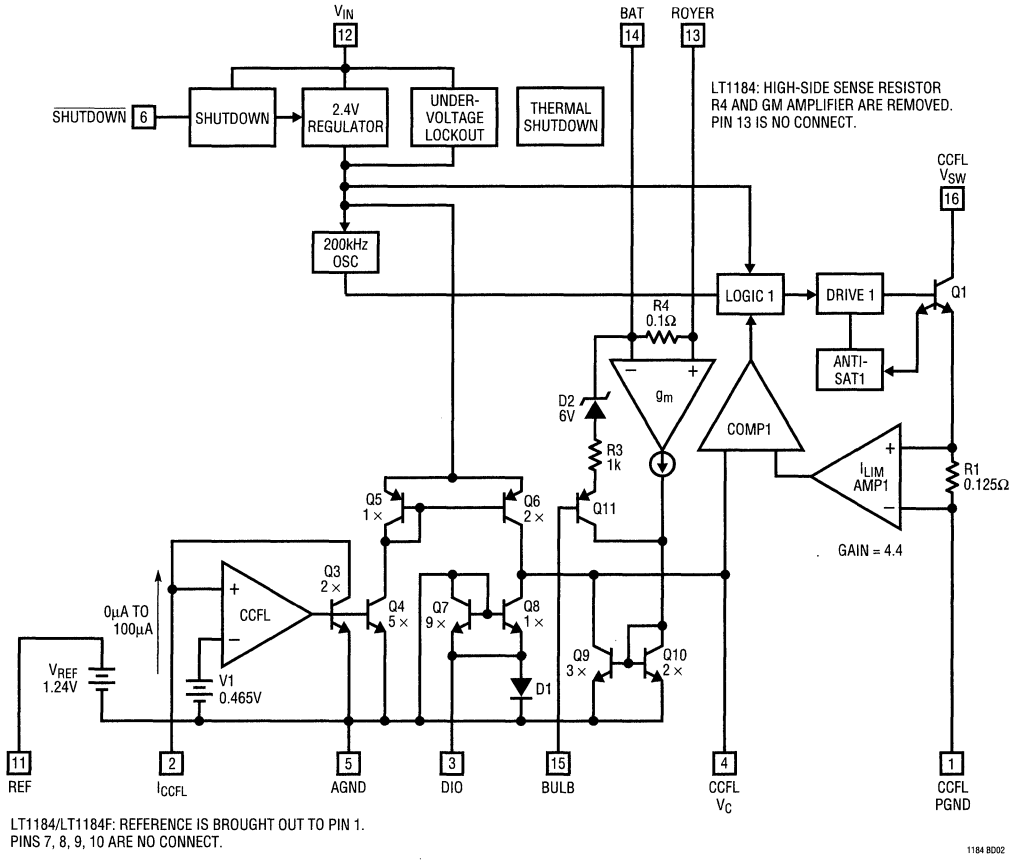


LT1183: FBP AND FBN ARE TIED TOGETHER TO CREATE FB AT PIN 10. THE REFERENCE IS BROUGHT OUT TO PIN 11.

1182 BD01

BLOCK DIAGRAM

LT1184/LT1184F CCFL Regulator Top Level Block Diagram



LT1184/LT1184F: REFERENCE IS BROUGHT OUT TO PIN 1.
PINS 7, 8, 9, 10 ARE NO CONNECT.

1184 BD02

APPLICATIONS INFORMATION

Introduction

Current generation portable computers and instruments use backlit Liquid Crystal Displays (LCDs). These displays also appear in applications extending to medical equipment, automobiles, gas pumps, and retail terminals. Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency in backlighting the display. Providing the most light out for the least amount of input power is the most important goal. These lamps require high voltage AC to operate, mandating an efficient high voltage DC/AC converter. The lamps operate from DC, but migration effects damage the lamp and shorten its lifetime. Lamp drive should contain zero DC component. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This minimizes EMI and RF emissions. Such emissions can interfere with other devices and can also degrade overall operating efficiency. Sinusoidal CCFL drive maximizes current-to-light conversion in the lamp. The circuit should also permit lamp intensity control from zero to full brightness with no hysteresis or "pop-on".

APPLICATIONS INFORMATION

Manufacturers offer a wide array of monochrome and color displays. LCD display types include passive matrix and active matrix. These displays differ in operating voltage polarity (positive and negative contrast voltage displays), operating voltage range, contrast adjust range, and power consumption. LCD contrast supplies must regulate, provide output adjustment over a significant range, operate over a wide input voltage range, and provide load currents from milliamps to tens of milliamps.

The small size and battery-powered operation associated with LCD equipped apparatus dictate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture and long battery life is a priority. Laptop and handheld portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50% of the battery drain. Displays found in newer color machines can have a contrast power supply battery drain as high as 20%.

Additionally, all components including PC board and hardware, usually must fit within the LCD enclosure with a height restriction of 5mm to 10mm.

The CCFL switching regulator in the LT1182/LT1183/LT1184/LT1184F typically drives an inductor that acts as a switched mode current source for a current driven Royer class converter with efficiencies as high as 90%. The control loop forces the regulator to pulse-width modulate the inductor's average current to maintain constant current in the lamp. The constant current's value, and thus lamp intensity is programmable. This drive technique provides a wide range of intensity control. A unique lamp current programming block permits either grounded-lamp or floating-lamp configurations. Grounded-lamp circuits directly control one-half of actual lamp current. Floating-lamp circuits directly control the Royer's primary side converter current. Floating-lamp circuits provide differential drive to the lamp and reduce the loss from stray lamp-to-frame capacitance, extending illumination range.

The LCD contrast switching regulator in the LT1182/LT1183 is typically configured as a flyback converter and generates a bias supply for contrast control. Other topology choices for generating the bias supply include a boost converter or a boost/charge pump converter. The supply's variable output permits adjustment of contrast for the majority of available displays. Some newer types of displays require a fairly constant supply voltage and provide contrast adjustment through a digital control pin. A unique, dual polarity, error amplifier and the selection of a flyback converter topology allow either positive or negative LCD contrast voltages to be generated with minor circuit changes. The difference between the LT1182 and LT1183 is found in the pinout for the inputs of the LCD contrast error amplifier. The LT1182 brings out the error amplifier inputs individually for setting up positive and negative polarity contrast capability. This feature allows an output connector to determine the choice of contrast operating polarity by a ground connection. The LT1183 ties the error amplifier inputs together and brings out an internal reference. The reference may be used in generating negative contrast voltages or in programming lamp current.

Block Diagram Operation

The LT1182/LT1183/LT1184/LT1184F are fixed frequency, current mode switching regulators. Fixed frequency, current mode switchers control switch duty cycle directly by switch current rather than by output voltage. Referring to the block diagram for the LT1182/LT1183, the switch for each regulator turns ON at the start of each oscillator cycle. The switches turn OFF when switch current reaches a predetermined level. The operation of the CCFL regulator in the LT1184/LT1184F is identical to that in the LT1182/LT1183. The control of output lamp current is obtained by using the output of a unique programming block to set current trip level. The contrast voltage is controlled by the output of a dual-input-stage error amplifier, which sets current trip level. The current mode switching technique has several advantages. First, it provides excellent rejection of input voltage variations. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short-circuit conditions.

The LT1182/LT1183/LT1184/LT1184F incorporate a low dropout internal regulator that provides a 2.4V supply for most of the internal circuitry. This low dropout design allows input voltage to vary from 3V to 30V with little

APPLICATIONS INFORMATION

change in quiescent current. An active low shutdown pin typically reduces total supply current to 35μA by shutting off the 2.4V regulator and locking out switching action for standby operation. The ICs incorporate undervoltage lockout by sensing regulator dropout and locking out switching below about 2.5V. The regulators also provide thermal shutdown protection that locks out switching in the presence of excessive junction temperatures.

A 200kHz oscillator is the basic clock for all internal timing. The oscillator turns on an output via its own logic and driver circuitry. Adaptive anti-sat circuitry detects the onset of saturation in a power switch and adjusts base drive current instantaneously to limit switch saturation. This minimizes driver dissipation and provides rapid turn-off of the switch. The CCFL power switch is guaranteed to provide a minimum of 1.25A in the LT1182/LT1183/LT1184/LT1184F and the LCD power switch is guaranteed to provide a minimum of 0.625A in the LT1182/LT1183. The anti-sat circuitry provides a ratio of switch current to driver current of about 50:1.

Simplified Lamp Current Programming

A programming block in the LT1182/LT1183/LT1184/LT1184F controls lamp current, permitting either grounded-lamp or floating-lamp configurations. Grounded configurations control lamp current by directly controlling one-half of actual lamp current and converting it to a feedback signal to close a control loop. Floating configurations control lamp current by directly controlling the Royer's primary side converter current and generating a feedback signal to close a control loop.

Previous backlighting solutions have used a traditional error amplifier in the control loop to regulate lamp current. This approach converted an RMS current into a DC voltage for the input of the error amplifier. This approach used several time constants in order to provide stable loop frequency compensation. This compensation scheme meant that the loop had to be fairly slow and that output overshoot with startup or overload conditions had to be carefully evaluated in terms of transformer stress and breakdown voltage requirements.

The LT1182/LT1183/LT1184/LT1184F eliminate the error amplifier concept entirely and replace it with a lamp current programming block. This block provides an easy-to-use interface to program lamp current. The programmer circuit also reduces the number of time constants in the control loop by combining the error signal conversion scheme and frequency compensation into a single capacitor. The control loop thus exhibits the response of a single pole system, allows for faster loop transient response and virtually eliminates overshoot under startup or overload conditions.

Lamp current is programmed at the input of the programmer block, the I_{CCFL} pin. This pin is the input of a shunt regulator and accepts a DC input current signal of 0μA to 100μA. This input signal is converted to a 0μA to 500uA source current at the CCFL V_C pin. The programmer circuit is simply a current-to-current converter with a gain of five. By regulating the I_{CCFL} pin, the input programming current can be set with DAC, PWM or potentiometer control. The typical input current programming range for 0mA to 6mA lamp current is 0μA to 50μA.

The I_{CCFL} pin is sensitive to capacitive loading and will oscillate with capacitance greater than 10pF. For example, loading the I_{CCFL} pin with a 1× or 10× scope probe causes oscillation and erratic CCFL regulator operation because of the probe's respective input capacitance. A current meter in series with the I_{CCFL} pin will also produce oscillation due to its shunt capacitance. Use a decoupling resistor of several kilo-ohms between the I_{CCFL} pin and the control circuitry if excessive stray capacitance exists. This is basically free with potentiometer or PWM control as these control schemes use resistors. A current output DAC should use an isolating resistor as the DAC can have significant output capacitance that changes as a function of input code.

Grounded-Lamp Configuration

In a grounded-lamp configuration, the low voltage side of the lamp connects directly to the LT1182/LT1183/LT1184/LT1184F DIO pin. This pin is the common connection between the cathode and anode of two internal diodes. In previous grounded-lamp solutions, these diodes were discrete units and are now integrated onto the IC, saving cost and board space. Bi-directional lamp current flows in the DIO pin and thus, the diodes conduct alternately on half

APPLICATIONS INFORMATION

cycles. Lamp current is controlled by monitoring one-half of the average lamp current. The diode conducting on negative half cycles has one-tenth of its current diverted to the CCFL pin and nulls against the source current provided by the lamp current programmer circuit. The compensation capacitor on the CCFL V_C pin provides stable loop compensation and an averaging function to the rectified sinusoidal lamp current. Therefore, input programming current relates to one-half of average lamp current.

The transfer function between lamp current and input programming current must be empirically determined and is dependent on the particular lamp/display housing combination used. The lamp and display housing are a distributed loss structure due to parasitic lamp-to-frame capacitance. This means that the current flowing at the high voltage side of the lamp is higher than what is flowing at the DIO pin side of the lamp. The input programming current is set to control lamp current at the high voltage side of the lamp, even though the feedback signal is the lamp current at the bottom of the lamp. This insures that the lamp is not overdriven which can degrade the lamp's operating lifetime.

Floating-Lamp Configuration

In a floating-lamp configuration, the lamp is fully floating with no galvanic connection to ground. This allows the transformer to provide symmetric, differential drive to the lamp. Balanced drive eliminates the field imbalance associated with parasitic lamp-to-frame capacitance and reduces "thermometering" (uneven lamp intensity along the lamp length) at low lamp currents.

Carefully evaluate display designs in relation to the physical layout of the lamp, it leads and the construction of the display housing. Parasitic capacitance from any high voltage point to DC or AC ground creates paths for unwanted current flow. This parasitic current flow degrades electrical efficiency and losses up to 25% have been observed in practice. As an example, at a Royer operating frequency of 60kHz, 1pF of stray capacitance represents an impedance of 2.65MΩ. With an operating lamp voltage of 400V and an operating lamp current of 6mA, the parasitic current is 150μA. The efficiency loss is 2.5%. Layout techniques that increase parasitic capacitance include long high voltage lamp leads, reflective metal foil around the lamp, and displays supplied in metal enclosures. Losses for a good display are under 5% whereas losses for a bad display range from 5% to 25%. Lossy displays are the primary reason to use a floating-lamp configuration. Providing symmetric, differential drive to the lamp reduces the total parasitic loss by one-half.

Maintaining closed-loop control of lamp current in a floating lamp configuration now necessitates deriving a feedback signal from the primary side of the Royer transformer. Previous solutions have used an external precision shunt and high side sense amplifier configuration. This approach has been integrated onto the LT1182/LT1183/LT1184F for simplicity of design and ease of use. An internal 0.1W resistor monitors the Royer converter current and connects between the input terminals of a high-side sense amplifier. A 0A to 1A Royer primary side, center tap current is translated to a 0μA to 500uA sink current at the CCFL V_C pin to null against the source current provided by the lamp current programmer circuit. The compensation capacitor on the CCFL V_C pin provides stable loop compensation and an averaging function to the error sink current. Therefore, input programming current is related to average Royer converter current. Floating-lamp circuits operate similarly to grounded-lamp circuits, except for the derivation of the feedback signal.

The transfer function between primary side converter current and input programming current must be empirically determined and is dependent upon a myriad of factors including lamp characteristics, display construction, transformer turns ratio, and the tuning of the Royer oscillator. Once again, lamp current will be slightly higher at one end of the lamp and input programming current should be set for this higher level to insure that the lamp is not overdriven.

The internal 0.1Ω high-side sense resistor on the LT1182/LT1183/LT1184F is rated for a maximum DC current of 1A. However, this resistor can be damaged by extremely high surge currents at start-up. The Royer converter typically uses a few microfarads of bypass capacitance at the center tap of the transformer. This capacitor charges up when the system is first powered by the battery pack or an AC wall adapter. The amount of current delivered at start-up can be

APPLICATIONS INFORMATION

very large if the total impedance in this path is small and the voltage source has high current capability. Linear Technology recommends the use of an aluminum electrolytic for the transformer center tap bypass capacitor with an ESR greater than or equal to 0.5Ω. This lowers the peak surge currents to an acceptable level. In general, the wire and trace inductance in this path also help reduce the di/dt of the surge current. This issue only exists with floating lamp circuits as grounded-lamp circuits do not make use of the high-side sense resistor.

Optimizing Optical Efficiency vs Electrical Efficiency

Evaluating the performance of an LCD backlight requires the measurement of both electrical and photometric efficiencies. The best optical efficiency operating point does not necessarily correspond to the best electrical efficiency. However, these two operating points are generally close. The desired goal is to maximize the amount of light out for the least amount of input power. It is possible to construct backlight circuits that operate with over 90% electrical efficiency, but produce significantly less light output than circuits that operate at 80% electrical efficiency.

The best electrical efficiency typically occur's just as the CCFL's transformer drive waveforms begin to exhibit artifacts of higher order harmonics reflected back from the Royer transformer secondary. Maximizing electrical efficiency equates to smaller values for the Royer primary side, resonating capacitor and larger values for the Royer secondary side ballast capacitor. The best optical efficiency occurs with nearly ideal sinusoidal drive to the lamp. Maximizing optical efficiency equates to larger values for the Royer primary side resonating capacitor and smaller values for the Royer secondary side ballast capacitor. The preferred operating point for the CCFL converter is somewhere in between the best electrical efficiency and the best optical efficiency. This operating point maximizes photometric output per watt of input power.

Making accurate and repeatable measurements of electrical and optical efficiency is difficult under the best circumstances. Requirements include high voltage measurements and equipment specified for this operation, specialized calibrated voltage and current probes, wideband RMS voltmeters, a photometer, and a calorimeter (for the backlight enthusiast). Linear Technology's Application Note 55 and Design Note 101 contain detailed information regarding equipment needs.

Input Supply Voltage Operating Range

The backlight/LCD contrast control circuits must operate over a wide range of input supply voltage and provide excellent line regulation for the lamp current and the contrast output voltage. This range includes the normal range of the battery pack itself as well as the AC wall adapter voltage, which is normally much higher than the maximum battery voltage. A typical input supply is 7V to 28V; a 4 to 1 supply range.

Operation of the CCFL control circuitry from the AC wall adapter generates the worst-case stress for the CCFL transformer. Evaluations of loop compensation for overshoot on startup transients and overload conditions are essential to avoid destructive arcing, overheating, and transformer failure. Open-lamp conditions force the Royer converter to operate open-loop. Component stress is again worst-case with maximum input voltage conditions. The LT1182/LT1183/LT1184/LT1184F open-lamp protection clamps the maximum transformer secondary voltage to safe levels and transfers the regulator loop from current mode operation into voltage mode operation. Other fault conditions include board shorts and component failures. These fault conditions can increase primary side currents to very high levels, especially at maximum input voltage conditions. Solutions to these fault conditions include electrical and thermal fuses in the supply voltage trace.

Improvements in battery technology are increasing battery lifetimes and decreasing battery voltages required by the portable systems. However, operation at reduced battery voltages requires higher, turns-ratio transformers for the CCFL to generate equivalent output drive capability. The penalty incurred with high ratio transformers is higher, circulating currents acting on the same primary side components. Loss terms increase and electrical efficiency often decreases.

APPLICATIONS INFORMATION

Size Constraints

Tighter length, width, and height constraints for CCFL and LCD contrast control circuitry are the result of LCD display enclosure sizes remaining fairly constant while display screen sizes have increased. Space requirements for connector hardware include the input power supply and control signal connector, the lamp connector, and the contrast output voltage connector.

Even though size requirements are shrinking, the high voltage AC required to drive the lamp has not decreased. In some cases, the use of longer bulbs for color, portable equipment has increased the high voltage requirement. Accommodating the high voltage on the circuit board dictates certain layout spacings and routings, involves providing creepages and clearances in the transformer design, and most importantly, involves routing a hole underneath the CCFL transformer. Routing this hole minimizes high voltage leakage paths and prevents moisture buildup that can result in destructive arcing. In addition to high voltage layout techniques, use appropriate layout techniques for isolating high current paths from low-current signal paths.

This leaves the remaining space for control circuitry at a premium. Minimum component count is required and minimum size for the components used is required. This squeeze on component size is often in direct conflict with the goals of maximizing battery life and efficiency. Compromise is often the only remaining choice.

LCD Contrast Circuits

The LCD contrast switching regulator on the LT1182/LT1183 operates in many standard switching configurations and is used as a classic DC/DC converter. The dual-input-stage error amplifier easily regulates either positive or negative contrast voltages. Topology choices for the converter include single inductor and transformer-based solutions. The switching regulator operates equally well either in continuous mode or discontinuous mode. Efficiencies for LCD contrast circuits range from 75% to 85% and depend on the total power drain of the particular display. Adjustment control of the LCD contrast voltage is provided by either potentiometer, PWM, or DAC control.

Applications Support

Linear Technology invests an enormous amount of time, resources, and technical expertise in understanding, designing and evaluating backlight/LCD contrast solutions for system designers. The design of an efficient and compact LCD backlight system is a study of compromise in a transduced electronic system. Every aspect of the design is interrelated and any design change requires complete re-evaluation for all other critical design parameters. Linear Technology has engineered one of the most complete test and evaluation setups for backlight designs and understands the issues and tradeoffs in achieving a compact, effficient and economical customer solution. Linear Technology welcomes the opportunity to discuss, design, evaluate, and optimize any backlight/LCD contrast system with a customer. For further information on backlight/LCD contrast designs, consult the references listed below.

References

1. Williams, Jim. August 1992. *Illumination Circuitry for Liquid Crystal Displays*. Linear Technology Corporation, Application Note 49.

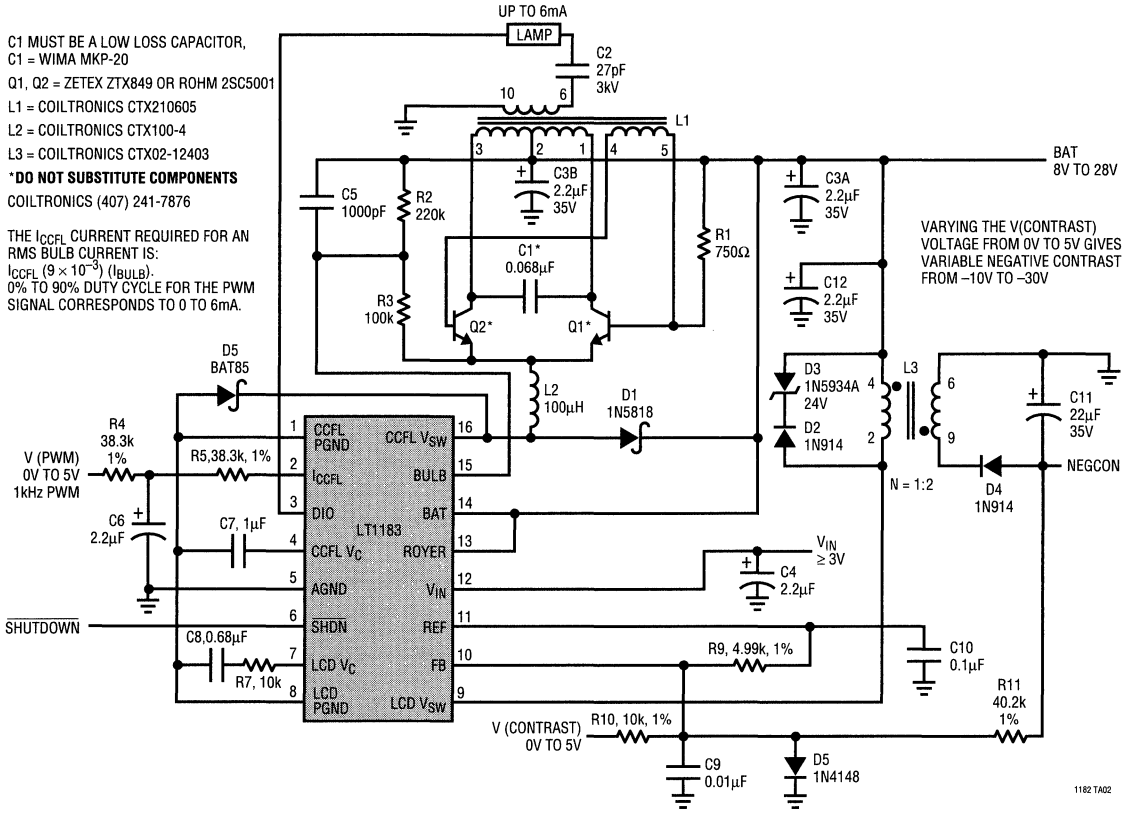
2. Williams, Jim. August 1993. *Techniques for 92% Efficient LCD Illumination*. Linear Technology Corporation, Application Note 55.

3. Bonte, Anthony. March 1995. *LT1182 Floating CCFL with Dual Polarity Contrast*. Linear Technology Corporation, Design Note 99.

4. Williams, Jim. April 1995. *A Precision Wideband Current Probe for LCD Backlight Meaasurement*. Linear Technology Corporation, Design Note 101.

TYPICAL APPLICATIONS

90% Efficient Grounded CCFL Configuration with Negative Polarity LCD Contrast



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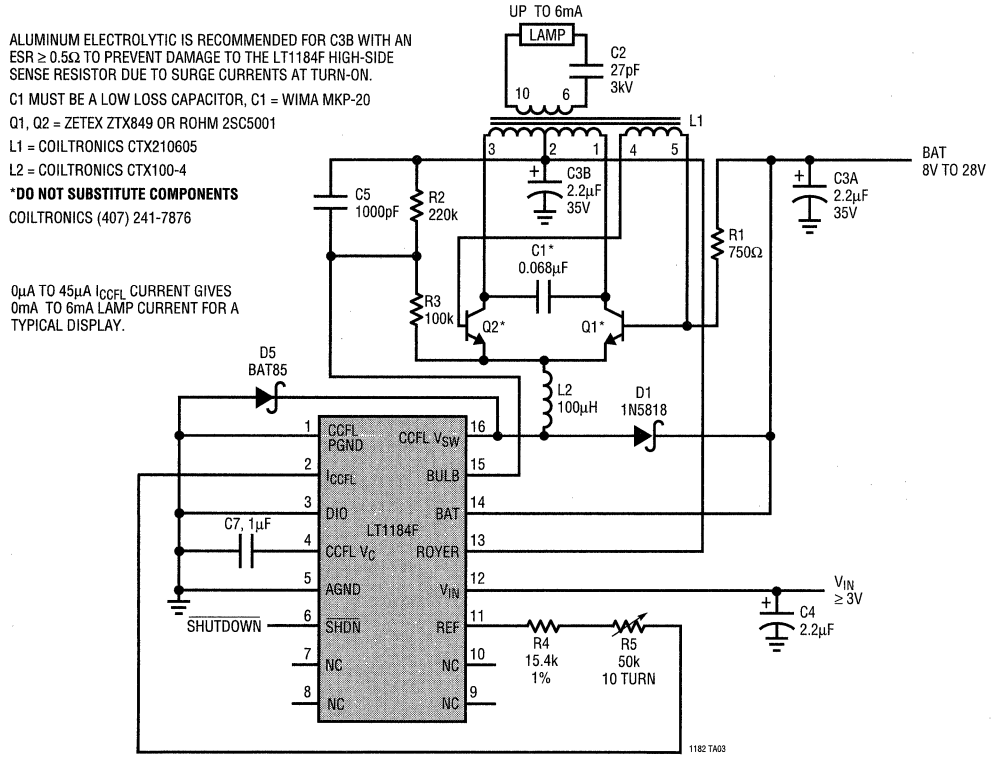
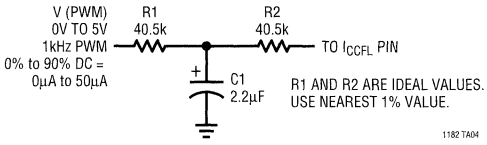
TYPICAL APPLICATIONS

LT1184F Floating CCFL with Potentiometer Control of Lamp Current

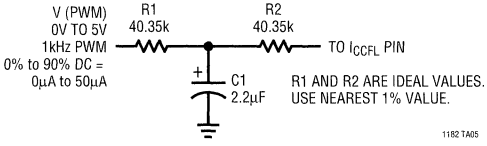


TYPICAL APPLICATIONS

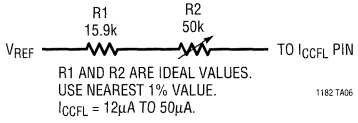
LT1182/LT1183 I_{CCFL} PWM Programming



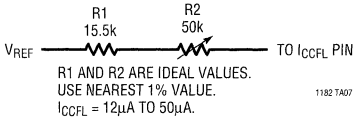
LT1184/LT1184F I_{CCFL} PWM Programming



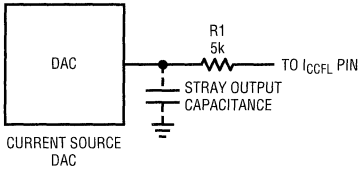
LT1183 I_{CCFL} Programming with Potentiometer Control



LT1184/LT1184F I_{CCFL} Programming with Potentiometer Control



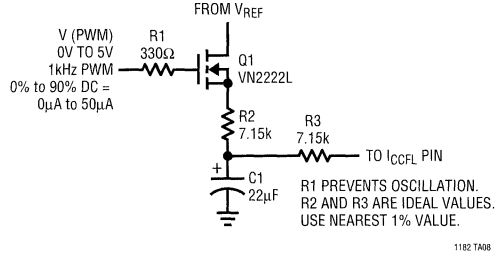
LT1182/LT1183/LT1184/LT1184F I_{CCFL} Programming with DAC Control



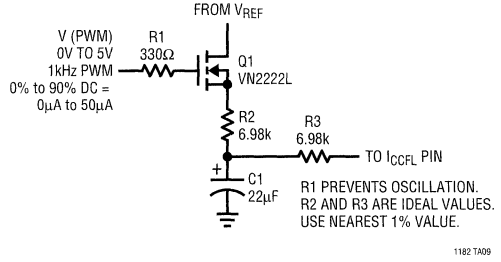
R1 DECOUPLES THE DAC OUTPUT CAPACITANCE FROM THE I_{CCFL} PIN.

1182 TA12

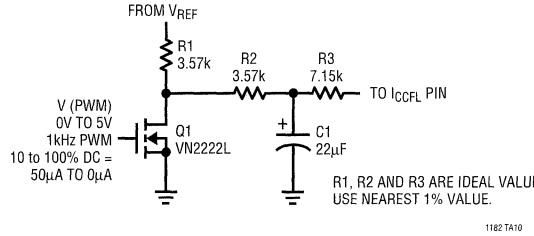
LT1183 I_{CCFL} PWM Programming with V_{REF}



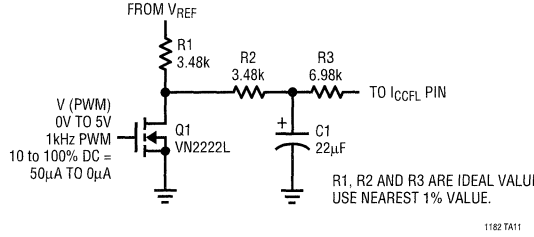
LT1184/LT1184F I_{CCFL} PWM Programming with V_{REF}



LT1183 I_{CCFL} PWM Programming with V_{REF}



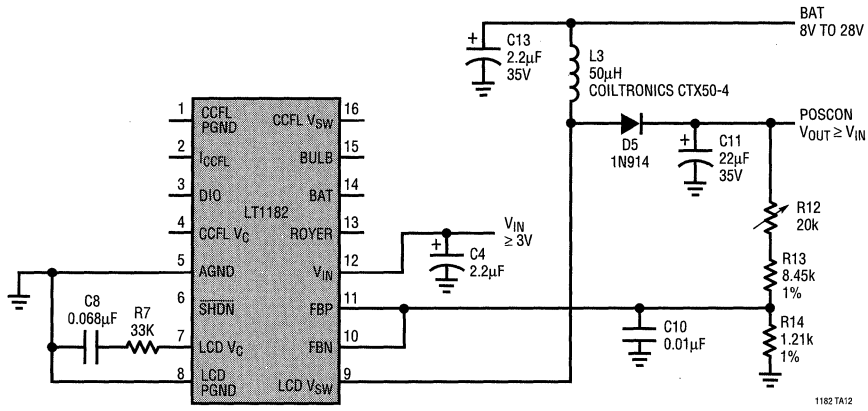
LT1184/LT1184F I_{CCFL} PWM Programming with V_{REF}



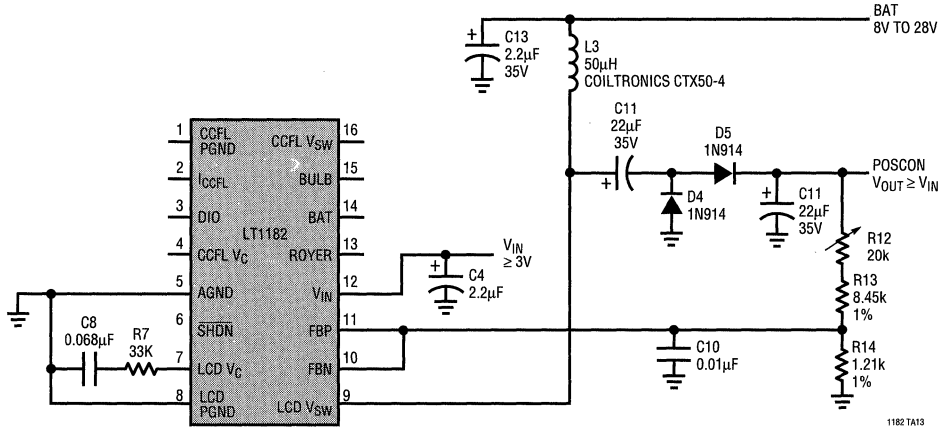
4

TYPICAL APPLICATIONS

LT1182 LCD Contrast Positive Boost Converter

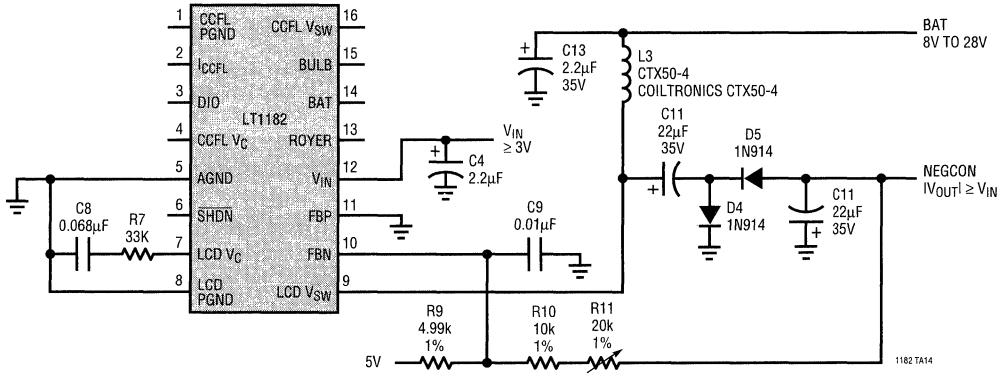


LT1182 LCD Contrast Positive Boost/Charge Pump Converter



TYPICAL APPLICATIONS

LT1182 LCD Contrast Positive to Negative/Charge Pump Converter



RELATED PARTS

PART NUMBER	FREQUENCY	SWITCH CURRENT	DESCRIPTION
LT1107	63kHz Hysteretic	1A	Micropower DC/DC Converter for LCD Contrast Control
LT1172	100kHz	1.25A	Current Mode Switching Regulator for CCFL or LCD Contrast Control
LT1173	24kHZ Hysteretic	1A	Micropower DC/DC Converter for LCD Contrast Control
LT1186	200kHz	1.25A	CCFL Switching Regulator with DAC for "Bits to Brightness Control"
LT1372	500kHz	1.5A	Current Mode Switching Regulator for CCFL or LCD Contrast Control

DAC Programmable CCFL Switching Regulator (Bits-to-Nits™)

FEATURES

- Wide Battery Input Range: 4.5V to 30V
- **Grounded Lamp or Floating Lamp Configurations**
- Open Lamp Protection
- **Precision 50µA Full-Scale DAC Programming Current**
- Standard SPI Mode or Pulse Mode
- **DAC Setting Is Retained in Shutdown**

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Retail Terminals

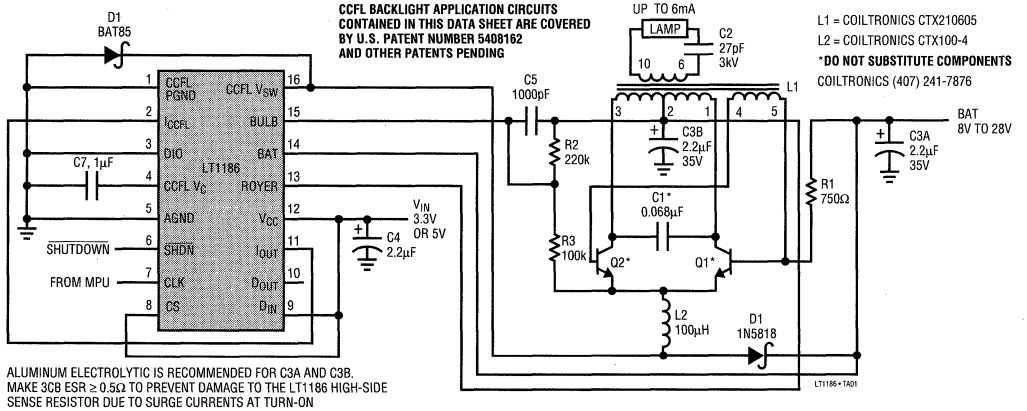
DESCRIPTION

The LT®1186 is a fixed frequency, current mode, switching regulator that provides the control function for Cold Cathode Fluorescent Lighting (CCFL). The IC includes an efficient high current switch, an oscillator, output drive logic, control circuitry and a micropower 8-bit 50µA full-scale current output DAC. The DAC provides simple "bits-to-lamp current control" and communicates in two interface modes including standard SPI mode and pulse mode. On power-up, the DAC counter resets to half-scale and the DAC configures to SPI or pulse mode depending on the $\overline{CS}$ signal level. In SPI mode, the system microprocessor serially transfers the present 8-bit data and reads back the previous 8-bit data. In pulse mode, the upper six bits of the DAC configure as increment-only (single-wire interface) or increment/decrement (two-wire interface) operation depending on the D_{IN} signal level.

The LT1186 control circuitry operates from a logic supply voltage of 3.3V or 5V. The IC also has a battery supply voltage pin that operates from 4.5V to 30V. The LT1186 draws 6mA typical quiescent current. An active low shutdown pin reduces total supply current to 35µA for standby operation and the DAC retains its last setting. A 200kHz switching frequency minimizes magnetic component size. Current mode switching techniques with cycle-by-cycle limiting gives high reliability and simple loop frequency compensation. The LT1186 is available in a 16-pin narrow SO package.

TYPICAL APPLICATION

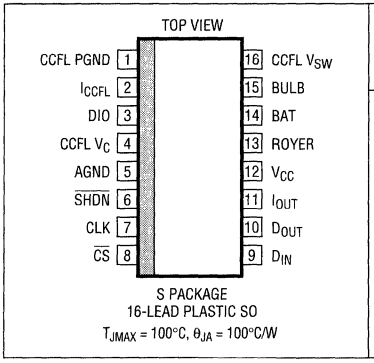
90% Efficient Floating CCFL with Single-Wire (Increment Only) Pulse Mode Control of Lamp Current



ABSOLUTE MAXIMUM RATINGS

V_{CC} 7V
BAT, Royer, Bulb 30V
CCFL V_{SW} 60V
Shutdown 6V
I_{CCFL} Input Current 10mA
DIO Input Current (Peak, <100ms) 100mA
Digital Inputs ..... −0.3V to V_{CC} + 0.3V
Digital Outputs ..... −0.3V to V_{CC} + 0.3V
DAC Output Voltage ..... −20V to V_{CC} + 0.3V
Junction Temperature (Note 1) ..... 100°C
Operating Ambient Temperature Range ... 0°C to 100°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT1186CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = $\overline{SHUTDOWN}$ = D_{IN} = $\overline{CS}$ = 3.3V, BAT = Royer = Bulb = 12V, I_{CCFL} = CCFL V_{SW} = Open, D_{OUT} = Three-State, DIO = I_{OUT} = CLK = GND, CCFL V_C = 0.5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Supply Current	3V ≤ V_{CC} ≤ 6.5V, 1/2 Full-Scale DAC Output Current	●		6	9.5	mA
$I_{\overline{SHDN}}$	$\overline{SHUTDOWN}$ Supply Current	$\overline{SHUTDOWN}$ = 0V, CCFL V_C Open (Note 2)			35	70	µA
	$\overline{SHUTDOWN}$ Input Bias Current	$\overline{SHUTDOWN}$ = 0V, CCFL V_C = Open			5	10	µA
	$\overline{SHUTDOWN}$ Threshold Voltage		●	0.45	0.85	1.2	V
f	Switching Frequency	Measured at CCFL V_{SW}, I_{SW} = 50mA, I_{CCFL} = 100µA, CCFL V_C = Open	 ●	175 160	200 200	225 240	kHz kHz
DC(MAX)	Maximum Switch Duty Cycle	Measured at CCFL V_{SW}	 ●	80 75	85 85		% %
BV	Switch Breakdown Voltage	Measured at CCFL V_{SW}		60	70		V
	Switch Leakage Current	V_{SW} = 12V, Measured at CCFL V_{SW} V_{SW} = 30V, Measured at CCFL V_{SW}				20 40	µA µA
	I_{CCFL} Summing Voltage	3V ≤ V_{CC} ≤ 6.5V	 ●	0.425 0.385	0.465 0.465	0.505 0.555	V V
	ΔI_{CCFL} Summing Voltage for ΔInput Programming Current	I_{CCFL} = 0µA to 100µA			5	15	mV
	CCFL V_C Offset Sink Current	CCFL V_C = 1.5V, Positive Current Measured into Pin		−5	5	15	µA
	ΔCCFL V_C Source Current for ΔI_{CCFL} Programming Current	I_{CCFL} = 25µA, 50µA, 75µA, 100µA, CCFL V_C = 1.5V	●	4.70	4.95	5.20	µA/µA
	CCFL V_C to DIO Current Servo Ratio	DIO = 5mA out of Pin, Measure I(V_C) at CCFL V_C = 1.5V	●	94	99	104	µA/mA
	CCFL V_C Low Clamp Voltage	V_{BAT} − V_{Bulb} = Bulb Protect Servo Voltage	●		0.1	0.3	V
	CCFL V_C High Clamp Voltage	I_{CCFL} = 100µA	●	1.7	2.1	2.4	V
	CCFL V_C Switching Threshold	CCFL V_{SW} DC = 0%	●	0.6	0.95	1.3	V
	CCFL High-Side Sense Servo Current	I_{CCFL} = 100µA, I(V_C) = 0µA at CCFL V_C = 1.5V	●	0.93	1.00	1.07	A
	CCFL High-Side Sense Servo Current Line Regulation	BAT = 5V to 30V, I_{CCFL} = 100µA, I(V_C) = 0µA at CCFL V_C = 1.5V			0.1	0.16	%/V

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = $\overline{SHUTDOWN}$ = D_{IN} = $\overline{CS}$ = 3.3V, BAT = Royer = Bulb = 12V, I_{CCFL} = CCFL V_{SW} = Open, D_{OUT} = Three-State, DIO = I_{OUT} = CLK = GND, CCFL V_C = 0.5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
	CCFL High-Side Sense Supply Current	Current Measured into BAT and Royer Pins	●	50	100	150	µA
	Bulb Protect Servo Voltage	I_{CCFL} = 100µA, I(V_C) = 0µA at CCFL V_C = 1.5V, Servo Voltage Measured between BAT and Bulb Pins	●	6.5	7.0	7.5	V
	Bulb Input Bias Current	I_{CCFL} = 100µA, I(V_C) = 0µA at CCFL V_C = 1.5V			5	9	µA
I_{LIM}	CCFL Switch Current Limit	Duty Cycle = 50% Duty Cycle = 75% (Note 3)	● ●	1.25 0.9	1.9 1.6	3.0 2.6	A A
V_{SAT}	CCFL Switch On Resistance	CCFL I_{SW} = 1A	●		0.6	1.0	Ω
$\frac{\Delta I_Q}{\Delta I_{SW}}$	Supply Current Increase During CCFL Switch On Time	CCFL I_{SW} = 1A			20	30	mA/A
	DAC Resolution				8		Bits
	DAC Full-Scale Current	V(I_{OUT}) = 0.465V, Measured in SPI Mode	 ●	48.75 47.50	50 50	51.25 52.50	µA µA
	DAC Zero Scale Current	V(I_{OUT}) = 0.465V, Measured in SPI Mode				200	nA
	DAC Differential Nonlinearity		●			±2.0	LSB
	DAC Supply Voltage Rejection	3V ≤ V_{CC} ≤ 6.5V, I_{OUT} = Full Scale, V(I_{OUT}) = 0.465V	●		2	4	LSB
	Logic Input Current	0 ≤ V_{IN} ≤ V_{CC}	●			±1	µA
V_{IH}	High Level Input Voltage	V_{CC} = 3.3V V_{CC} = 5V	● ●	1.9 2			V V
V_{IL}	Low Level Input Voltage	V_{CC} = 3.3V V_{CC} = 5V	● ●			0.45 0.80	V V
V_{OH}	High Level Output Voltage	V_{CC} = 3.3V, I_O = 400µA V_{CC} = 5V, I_O = 400µA	● ●	2.1 2.4			V V
V_{OL}	Low Level Output Voltage	V_{CC} = 3.3V, I_O = 1mA V_{CC} = 5V, I_O = 2mA	● ●			0.4 0.4	V V
I_{OZ}	Three-State Output Leakage	$V_{\overline{CS}}$ = V_{CC}	●			±5	µA
SERIAL INTERFACE (Notes 4, 5)							
f_{CLK}	Clock Frequency		●			2	MHz
t_{CKS}	Setup Time, CLK↓ Before $\overline{CS}$↓		●	150			ns
t_{CSS}	Setup Time, $\overline{CS}$↓ Before CLK↑		●	400			ns
t_{DV}	$\overline{CS}$↓ to D_{OUT} Valid	See Test Circuits	●	150			ns
t_{DS}	Data in Setup Time Before CLK↑		●	150			ns
t_{DH}	Data in Hold Time After CLK↑		●	150			ns
t_{DO}	CLK↓ to D_{OUT} Valid	See Test Circuits	●	150			ns
t_{CKHI}	CLK High Time		●	200			ns
t_{CKLO}	CLK Low Time		●	250			ns
t_{CSH}	CLK↓ Before $\overline{CS}$↑		●	150			ns
t_{DZ}	$\overline{CS}$↑ to D_{OUT} In Hi-Z	See Test Circuits	●			400	ns
t_{CKH}	$\overline{CS}$↑ Before CLK↑		●			400	ns
t_{CSLO}	$\overline{CS}$ Low Time	f_{CLK} = 2MHz	●	4550			ns
t_{CSHI}	$\overline{CS}$ High Time		●	400			ns

ELECTRICAL CHARACTERISTICS

ıe ● denotes specifications which apply over the specified operating mperature range.

ote 1: T_J is calculated from the ambient temperature T_A and power ssipation P_D according to the following formula:

LT1186CS: $T_J = T_A + (P_D \times 100°C/W)$

ote 2: Does not include switch leakage.

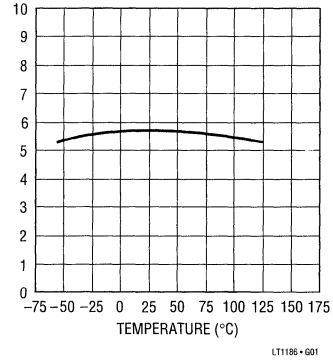
Note 3: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by $I_{LIM} = 1.4(1.393 - DC)$ for the LT1186 due to internal slope compensation circuitry.

Note 4: Timings for all input signals are measured at 0.8V for a High-to-Low transition and 2.0V for a Low-to-High transition.

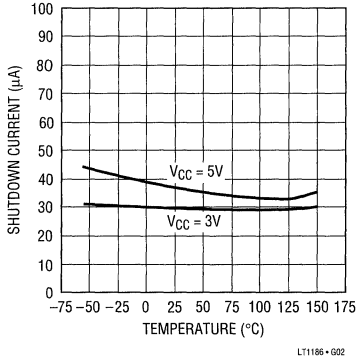
Note 5: Timings are guaranteed but not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

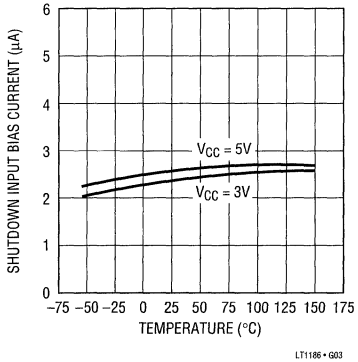
Supply Current vs Temperature



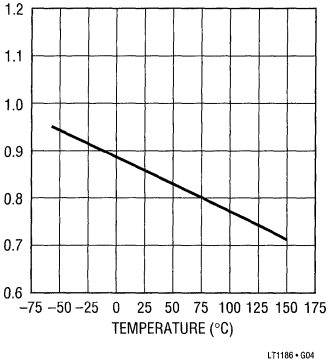
Shutdown Current vs Temperature



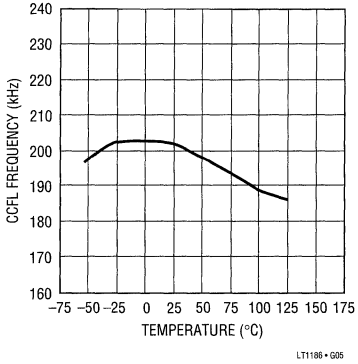
Shutdown Input Bias Current vs Temperature



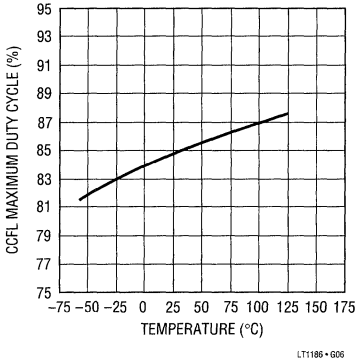
Shutdown Threshold Voltage vs Temperature



Frequency vs Temperature



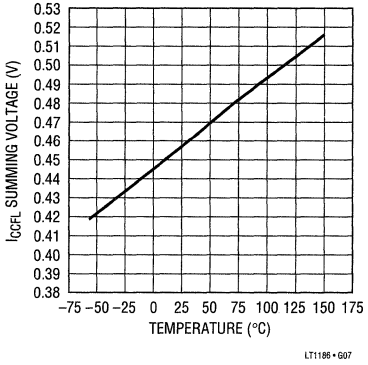
Maximum Duty Cycle vs Temperature



4

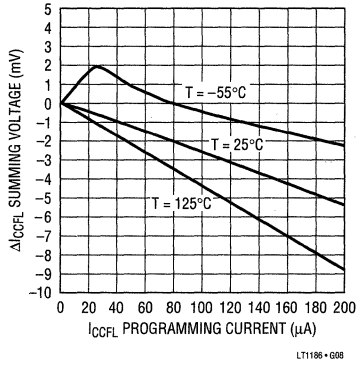
TYPICAL PERFORMANCE CHARACTERISTICS

I_{CCFL} Summing Voltage vs Temperature



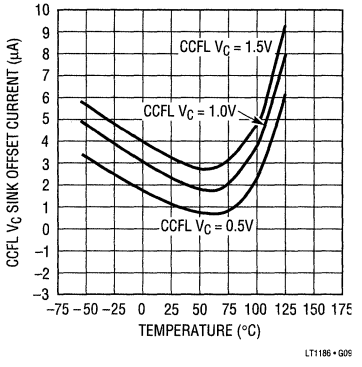
LT1186 • G07

I_{CCFL} Summing Voltage Load Regulation



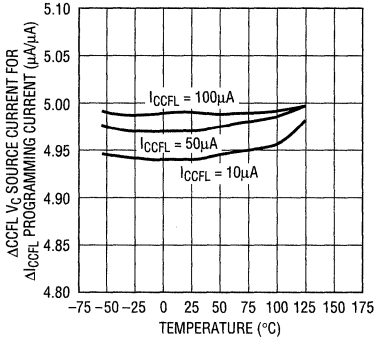
LT1186 • G08

V_C Sink Offset Current vs Temperature



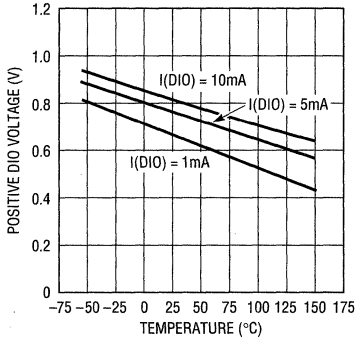
LT1186 • G09

ΔCCFL V_C Source Current for ΔI_{CCFL} Programming Current vs Temperature



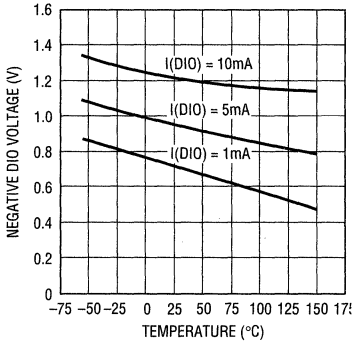
LT1186 • G10

Positive DIO Voltage vs Temperature



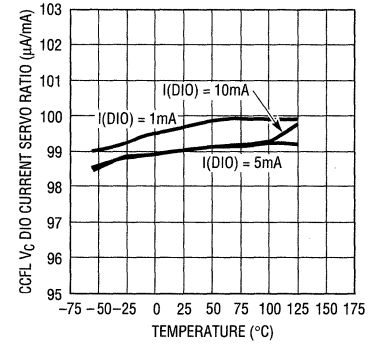
LT1186 • G11

Negative DIO Voltage vs Temperature



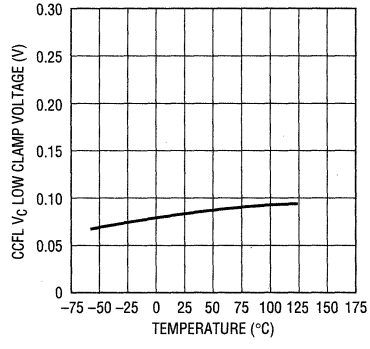
LT1186 • G12

V_C to DIO Current Servo Ratio vs Temperature



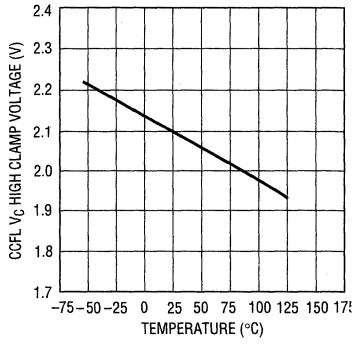
LT1186 • G13

V_C Low Clamp Voltage vs Temperature



LT1186 • G14

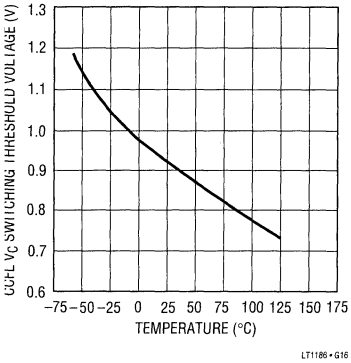
V_C High Clamp Voltage vs Temperature



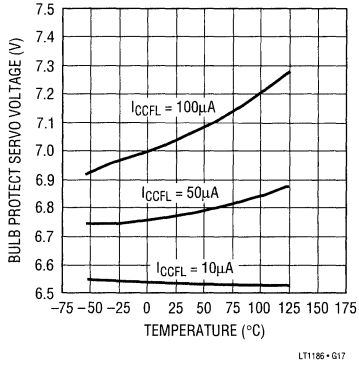
LT1186 • G15

TYPICAL PERFORMANCE CHARACTERISTICS

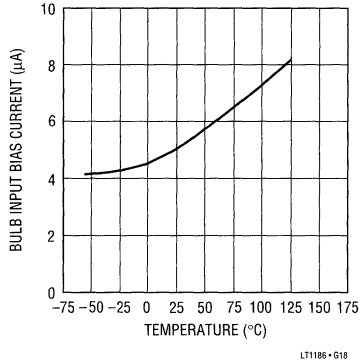
V_C Switching Threshold vs Temperature



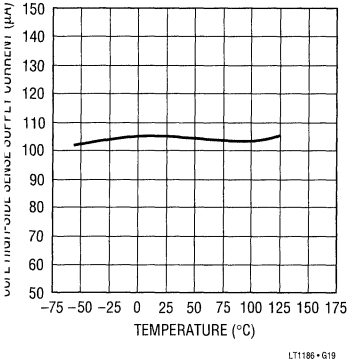
Bulb Protect Servo Voltage vs Temperature



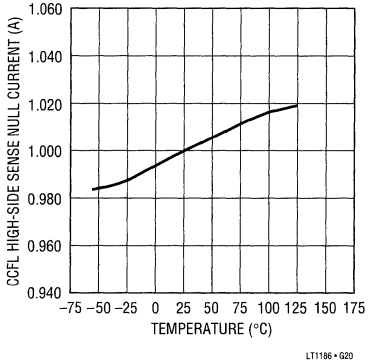
Bulb Input Bias Current vs Temperature



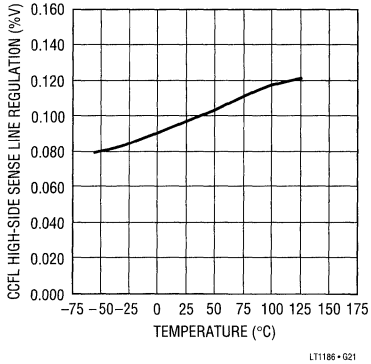
High-Side Sense Supply Current vs Temperature



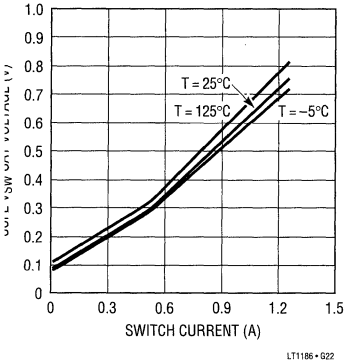
High-Side Sense Null Current vs Temperature



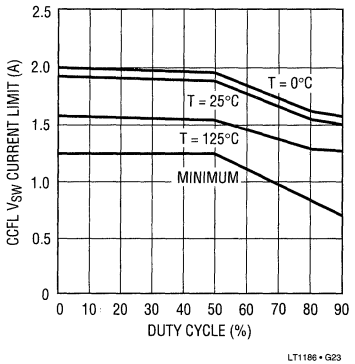
High-Side Sense Null Current Line Regulation vs Temperature



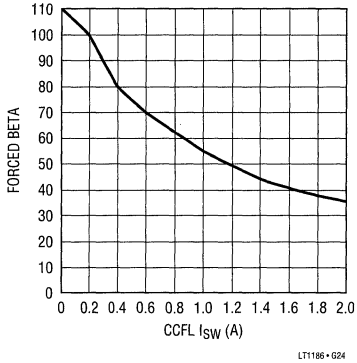
V_{SW} Sat Voltage vs Switch Current



V_{SW} Current Limit vs Duty Cycle



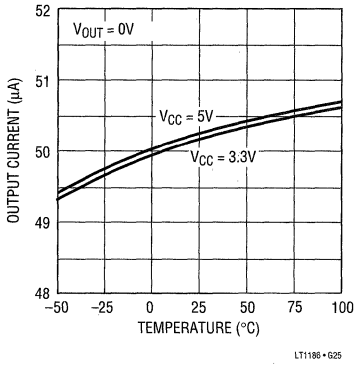
Forced Beta vs I_{SW} on V_{SW}



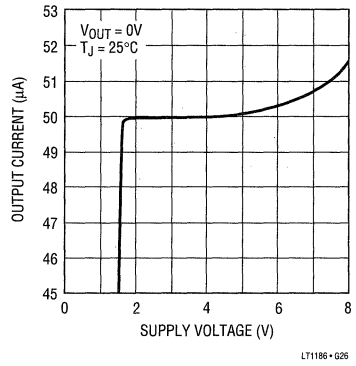
4

TYPICAL PERFORMANCE CHARACTERISTICS

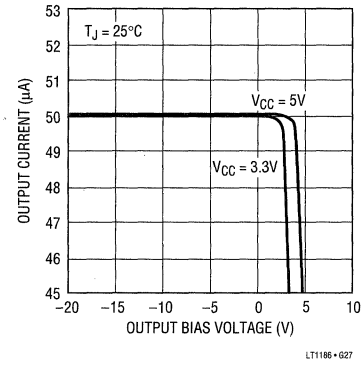
DAC I_{OUT} vs Temperature



DAC I_{OUT} vs Supply Voltage



DAC I_{OUT} vs I_{OUT} Bias Voltage



PIN FUNCTIONS

CCFL PGND (Pin 1): This pin is the emitter of an internal NPN power switch. CCFL switch current flows through this pin and permits internal, switch-current sensing. The regulator provides a separate analog ground and power ground to isolate high current ground paths from low current signal paths. Linear Technology recommends the use of star-ground layout techniques.

I_{CCFL} (Pin 2): This pin is the input to the CCFL lamp current programming circuit. This pin internally regulates to 465mV. The pin accepts a DC input current signal of 0µA to 50µA full scale from the DAC. This input signal is converted to a 0µA to 250µA source current at the CCFL V_C pin. As input programming current increases, the regulated lamp current increases. For a typical 6mA lamp, the range of input programming current is about 0µA to 50µA.

DIO (Pin 3): This pin is the common connection between the cathode and anode of two internal diodes. The remaining terminals of the two diodes connect to ground. In a grounded-lamp configuration, DIO connects to the low voltage side of the lamp. Bidirectional lamp current flows in the DIO pin and thus the diodes conduct alternately on half cycles. Lamp current is controlled by monitoring one-half of the average lamp current. The diode conducting on negative half cycles has one-tenth of its current diverted to the CCFL V_C pin. This current nulls against the source current provided by the lamp-current programmer circuit. A single capacitor on the CCFL V_C pin provides both stable loop compensation and an averaging function to the half-wave-rectified sinusoidal lamp current. Therefore, input programming current relates to one-half of average lamp current. This scheme reduces the number of loop compensation components and permits faster loop transient response in comparison to previously published circuits. If a floating lamp configuration is used, ground the DIO pin.

CCFL V_C (Pin 4): This pin is the output of the lamp current programmer circuit and the input of the current comparator for the CCFL regulator. Its uses include frequency compensation, lamp-current averaging for grounded-lamp circuits and current limiting. The voltage on the CCFL V_C pin determines the current trip level for switch turn-off. During normal operation this pin sits at a voltage between 0.95V (zero switch current) and 2.0V (maximum switch current) with respect to analog ground (AGND). This pin has a high impedance output and permits external voltage clamping to adjust current limit. A single capacitor to ground provides stable loop compensation. This simplified loop compensation method permits the CCFL regulator to exhibit single-pole transient response behavior and virtually eliminates transformer output overshoot.

PIN FUNCTIONS

AGND (Pin 5): This is the low current analog ground. It is the negative sense terminal for the internal 1.24V reference and the I_{CCFL} summing voltage in the LT1186. Connect low current signal paths that terminate to ground and frequency compensation components that terminate to ground directly to this pin for best regulation and performance.

$\overline{SHDN}$ (Pin 6): Pulling this pin low causes complete regulator shutdown with quiescent current typically reduced to 35µA. If the pin is not used, use a pull-up resistor to force a logic high level (maximum of 6V) or tie directly to V_{CC}. In a shutdown condition, the DAC retains its last output current setting and returns to this level when the logic-low signal at the shutdown pin is removed.

CLK (Pin 7): This pin is the shift clock for the DAC. This clock synchronizes the serial data and is a Schmitt trigger input. In standard SPI mode, the clock shifts data into D_{IN} and out of D_{OUT} on the rising and falling edges of the clock respectively. In pulse mode, the rising edge of the clock either increments or decrements the counter. This action depends on the choice of a single-wire interface (increment only) or a two-wire interface (increment/decrement).

$\overline{CS}$ (Pin 8): This pin is the chip select input for the DAC. In SPI mode, a logic low on the $\overline{CS}$ pin enables the DAC to receive and transfer 8-bit serial data. After the serial input data is shifted in, a rising edge of $\overline{CS}$ transfers the data into the counter, the DAC assumes the new I_{OUT} value and the D_{OUT} pin returns to the high impedance state. On power up, a logic high places the DAC into pulse mode. Pulling $\overline{CS}$ low after this places the DAC into SPI mode until V_{CC} resets.

D_{IN} or UP/$\overline{DN}$ (Pin 9): This pin is the digital input for the DAC. In SPI mode, the 8-bit serial data is shifted into the D_{IN} input on each rising edge of the clock signal. In pulse mode, on power up, a logic high at D_{IN} transfers the pin function from D_{IN} to UP/$\overline{DN}$, puts the counter into increment-only mode and the pin function shifts to up or down increment control of DAC output current. If UP/$\overline{DN}$ receives a logic-low signal, the counter configures to increment/decrement mode until V_{CC} resets.

D_{OUT} (Pin 10): This pin is the digital output for the DAC. In SPI mode, D_{OUT} is in three-state until $\overline{CS}$ falls low. The D_{OUT} pin then serially transfers the previous 8-bit data on every falling edge of the clock. When $\overline{CS}$ rises high again, D_{OUT} returns to a three-state condition. In pulse mode, D_{OUT} is always three-stated.

I_{OUT} (Pin 11): This pin is the analog current output for the DAC and provides an output current of 50 ±2.5µA over temperature. This pin can be biased from –20V to 2V for a 3.3V V_{CC} supply voltage or from –20V to 2.5V for a 5V V_{CC} supply voltage. However, this pin is tied to the I_{CCFL} pin and provides the programming current which sets operating lamp current. The I_{OUT} pin has very little bias voltage change when it is tied to the I_{CCFL} pin as I_{CCFL} is regulated. The programming current is sourced from the I_{OUT} pin and sunk by the I_{CCFL} pin.

V_{CC} (Pin 12): This is the supply pin for the LT1186. The IC accepts an input voltage range of 3V minimum to 6.5V maximum with little change in quiescent current (zero switch current). An internal, low-dropout regulator provides a 2.4V supply for most of the internal circuitry. Supply current increases as switch current increases at a rate approximately 1/50 of switch current. This corresponds to a forced Beta of 50 for the power switch. The IC incorporates undervoltage lockout by sensing regulator dropout and locking out switching for input voltages below 2.5V. Hysteresis is not used to maximize the useful range of input voltage. The typical input voltage is a 3.3V or 5V logic supply.

ROYER (Pin 13): This pin connects to the center-tapped primary of the Royer converter and is used with the BAT pin in a floating-lamp configuration where lamp current is controlled by sensing Royer primary-side converter current. This pin is the inverting terminal of a high-side current sense amplifier. The typical quiescent current is 50µA into the pin. If the CCFL regulator is not used in a floating-lamp configuration, tie the Royer and BAT pins together.

PIN FUNCTIONS

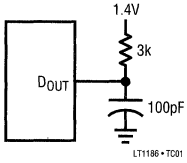
BAT (Pin 14): This pin connects to the battery or AC wall adapter voltage from which the CCFL Royer converter operates. This voltage is typically higher than the V_{CC} supply voltage but can equal V_{CC} if V_{CC} is a 5V logic supply. The BAT voltage must be at least 2.1V greater than the internal 2.4V regulator or 4.5V. This pin provides biasing for the lamp-current programming block, is used with the Royer pin for floating-lamp configurations and connects to one input for the open-lamp protection circuitry. For floating-lamp configurations, this pin is the noninverting terminal of a high-side current sense amplifier. The typical quiescent current is 50μA into the pin. The BAT and Royer pins monitor the primary-side Royer converter current through an internal 0.1Ω topside current sense resistor. A 0A to1A primary-side, center tap converter current is translated to an input signal range of 0mV to 100mV for the current sense amplifier. This input range translates to a 0μA to 500μA sink current at the CCFL V_C pin that nulls against the source current provided by the programmer circuit. The BAT pin also connects to the top side of the internal clamp between the BAT and Bulb pins that is used for open-lamp protection.

BULB (Pin 15): This pin connects to the low side of a 7V threshold comparator between the BAT and Bulb pins. This circuit sets the maximum voltage level across the primary side of the Royer converter under all operating conditions and limits the maximum secondary output under start-up conditions or open-lamp conditions. This eases transformer voltage rating requirements. Set the voltage limit to ensure lamp start-up with worst-case, lamp start voltages and cold temperature, system operating conditions. The Bulb pin connects to the junction of an external divider network. The divider network connects from the center tap of the Royer transformer or the actual battery supply voltage to the top side of the current source "tail inductor." A capacitor across the top of the divider network filters switching ripple and sets a time constant that determines how quickly the clamp activates. When the comparator activates, sink current is generated to pull the CCFL V_C pin down. This action transfers the entire regulator loop from current mode operation into voltage mode operation.

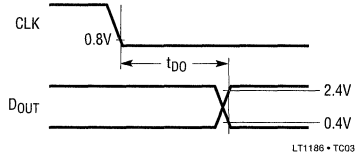
CCFL V_{SW} (Pin 16): This pin is the collector of the internal NPN power switch for the CCFL regulator. The power switch provides a minimum of 1.25A. Maximum switch current is a function of duty cycle as internal slope compensation ensures stability with duty cycles greater than 50%. Using a driver loop to automatically adapt base drive current to the minimum required to keep the switch in a quasi-saturation state yields fast switching times and high efficiency operation. The ratio of switch current to driver current is about 50:1.

TEST CIRCUITS

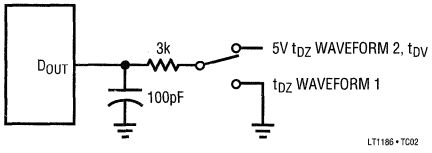
Load Circuit for t_{DO}



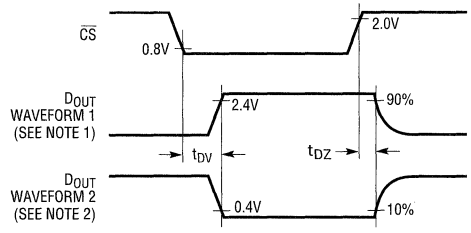
Voltage Waveforms for t_{DO}



Load Circuit for t_{DZ}, t_{DV}



Voltage Waveforms for t_{DZ}, t_{DV}



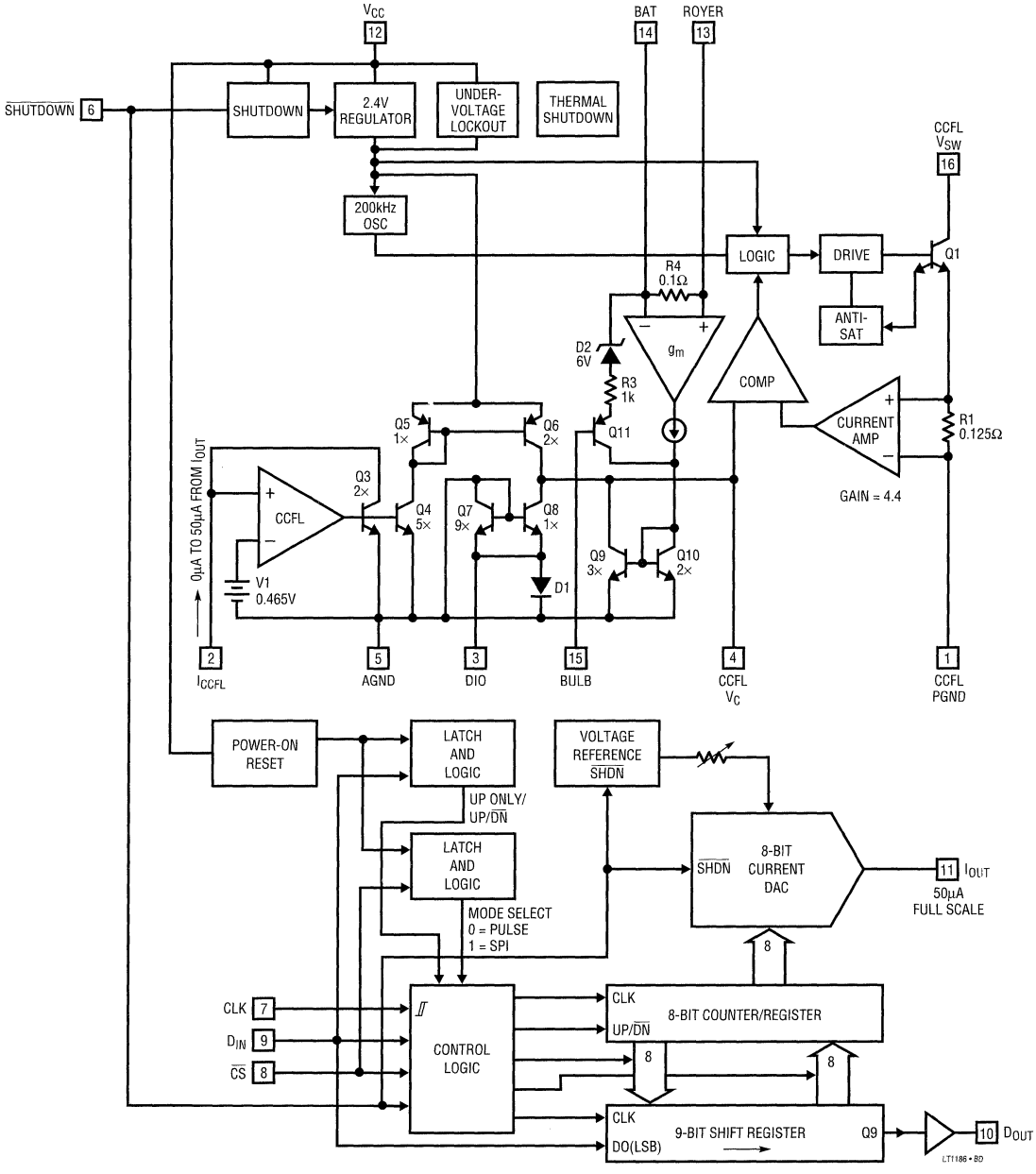
NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY $\overline{CS}$

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY $\overline{CS}$

LT1186 • TC04

BLOCK DIAGRAM

LT1186 DAC Programmable CCFL Switching Regulator



APPLICATIONS INFORMATION

Introduction

Current generation portable computers and instruments use backlit Liquid Crystal Displays (LCDs). Cold Cathode Fluorescent Lamps (CCFLs) provide the highest available efficiency in back lighting the display. Providing the most light out for the least amount of input power is the most important goal. These lamps require high voltage AC to operate, mandating an efficient high voltage DC/AC converter. The lamps operate from DC, but migration effects damage the lamp and shorten its lifetime. Lamp drive should contain zero DC component. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This minimizes EMI and RF emissions. Such emissions can interfere with other devices and can also degrade overall operating efficiency. Sinusoidal CCFL drive maximizes current-to-light conversion in the lamp. The circuit should also permit lamp intensity control from zero to full brightness with no hysteresis or "pop-on."

The small size and battery-powered operation associated with LCD equipped apparatus dictate low component count and high efficiency for these circuits. Size constraints place severe limitations on circuit architecture and long battery life is a priority. Laptop and handheld portable computers offer an excellent example. The CCFL and its power supply are responsible for almost 50% of the battery drain. Additionally, all components, including PC board and hardware, usually must fit within the LCD enclosure with a height restriction of 5mm to 10mm.

The CCFL regulator drives an inductor that acts as a switched-mode current source for a current-driven Royer-class converter with efficiencies as high as 90%. The control loop forces the CCFL PWM to modulate the average inductor current to maintain constant current in the lamp. The constant current value, and thus lamp intensity, is programmable. This drive technique provides a wide range of intensity control. A unique lamp-current programming block permits either grounded lamp or floating lamp configurations. Grounded lamp circuits directly sense one-half of average lamp current. Floating lamp circuits directly sense the Royer's primary-side converter current. Floating-lamp circuits provide symmetric differential drive to the lamp and reduce the parasitic loss from stray lamp-to-frame capacitance, extending illumination range.

Block Diagram Operation

The LT1186 is a fixed frequency, current mode switching regulator. A fixed frequency, current mode switcher controls switch duty cycle directly by switch current rather than by output voltage. Referring to the block diagram for the LT1186, the switch turns ON at the start of each oscillator cycle. The switch turns OFF when switch current reaches a predetermined level. The control of output lamp current is obtained by using the output of a unique programming block to set current trip level. The current mode switching technique has several advantages. First, it provides excellent rejection of input voltage variations. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short-circuit conditions.

The LT1186 incorporates a low dropout internal regulator that provides a 2.4V supply for most of the internal circuitry. This low dropout design allows input voltage to vary from 3V to 6.5V with little change in quiescent current. An active low shutdown pin typically reduces total supply current to 35μA by shutting off the 2.4V regulator and locks out switching action for standby operation. The IC incorporates undervoltage lockout by sensing regulator dropout and locking out switching below about 2.5V. The regulator also provides thermal shutdown protection that locks out switching in the presence of excessive junction temperatures.

A 200kHz oscillator is the basic clock for all internal timing. The oscillator turns on the output switch via its own logic and driver circuitry. Adaptive anti-sat circuitry detects the onset of saturation in the power switch and adjusts base drive current instantaneously to limit switch saturation. This minimizes driver dissipation and provides rapid turn-off of the switch. The CCFL power switch is guaranteed to provide a minimum of 1.25A in the LT1186. The anti-sat

IPPLICATIONS INFORMATION

rcuitry provides a ratio of switch current to driver current f about 50:1.

-Bit Current Output DAC

he 8-bit current output DAC is guaranteed monotonic and digitally adjustable by the 8-bit counter in 256 equal eps. On power up, the counter resets to 80H and the DAC ssumes its mid-range value. The current output I_{OUT} rives the I_{CCFL} pin and sets control current for the lamp urrent programming block. The DAC has its own 1.24V andgap reference and a voltage to current converter that trimmed at wafer sort to provide the precision full-scale urrent reference. Over temperature, the current output of ie DAC is 50µA ±5%.

igital Interface

n power-up, a logic high at $\overline{CS}$ configures the DAC into ulse mode. If $\overline{CS}$ is ever pulled low, the chip configures to SPI mode until V_{CC} resets. On power-up in pulse ode, a logic high at D_{IN} puts the counter into increment-nly mode. If UP/$\overline{DN}$ (D_{IN}) is ever pulled low, the counter onfigures into increment/decrement mode until V_{CC} re-ts. These modes are illustrated in Figure 1.

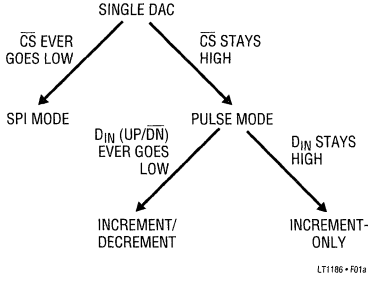


Figure 1a. Tree Diagram (LT1186 DAC Operating Modes)

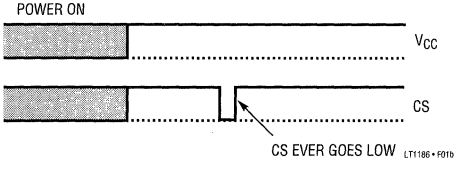


Figure 1b. SPI Mode Setup

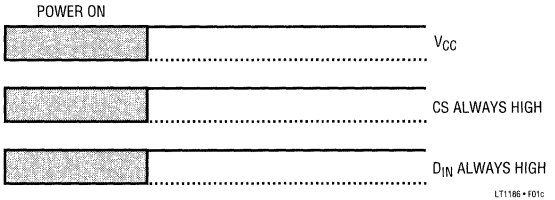


Figure 1c. Pulse Mode Setup (Increment Only)

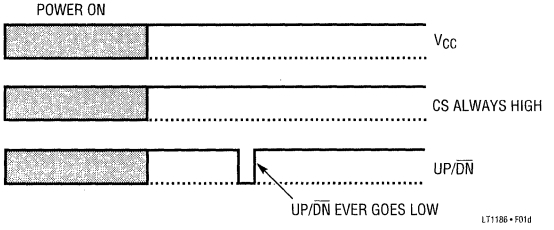


Figure 1d. Pulse Mode Setup (Increment/Decrement)

Standard SPI Mode

Refer to the serial interface operating sequence in Figure 2. A falling edge at $\overline{CS}$ initiates the data transfer. After the falling $\overline{CS}$ is recognized, D_{OUT} comes out of three-state. The clock (CLK) synchronizes the data transfer. Each input bit shifts into D_{IN} beginning with the MSB on the rising CLK edge and each previous data bit shifts out of D_{OUT} beginning with the MSB on the falling CLK edge. After the 8-bit serial input data is shifted in, a rising edge at $\overline{CS}$ transfers the data into the counter, the DAC assumes the new value I_{OUT} = (8-bit serial input data) × 50µA/255 and the D_{OUT} pin returns to a high impedance state.

Single-Wire Interface (Pulse Mode)

In increment-only pulse mode, each rising edge of CLK increments the upper six bits of the counter by one count. When incremented beyond 11111100B, the counter rolls over and sets the DAC to the minimum value 00000000B. Therefore, a single pulse applied to CLK increases the upper 6-bit counter by one-step, and 63 pulse applied to CLK decreases the counter by one-step. The last two LSBs are always zero in this mode. $I_{OUT} = (B_7B_6B_5B_4B_3B_2B_1B_0) \times 50\mu A/255$. The upper 6-bit counter = $B_7B_6B_5B_4B_3B_2$ and $B_1 = B_0 = 0$. To configure the LT1186 into increment-only mode, tie $\overline{CS}$ and D_{IN} to V_{CC}.

4

APPLICATIONS INFORMATION

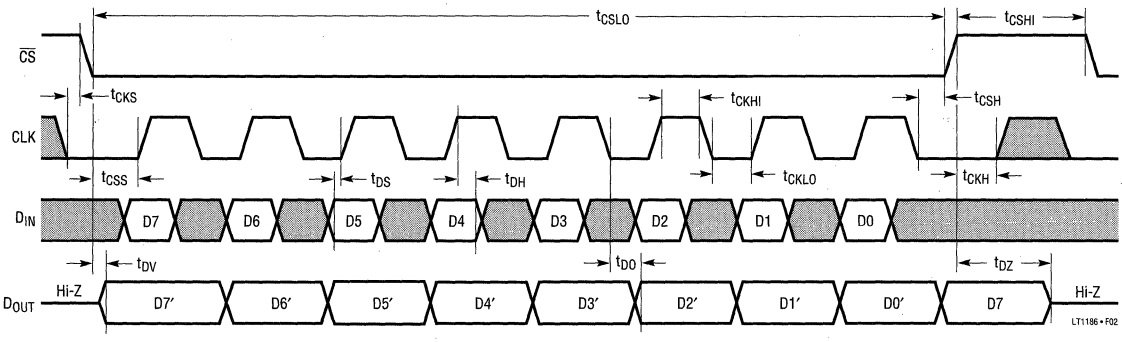


Figure 2. SPI Interface Timing Specification

Two-Wire Interface (Pulse Mode)

In increment/decrement pulse mode, a logic high at UP/$\overline{DN}$ programs the counter into increment mode and each rising edge of CLK increments the upper six bits of the counter by one. The counter stops incrementing at 11111100B. A logic low at UP/$\overline{DN}$ programs the counter into decrement mode and each rising edge of CLK decrements the upper six bits of the counter by one. The counter stops decrementing at 00000000B. The last two LSBs are always zero in this mode. $I_{OUT} = (B_7B_6B_5B_4B_3B_2B_1B_0) \times 50\mu A/255$. The upper 6-bit counter = $B_7B_6B_5B_4B_3B_2$ and $B_1 = B_0 = 0$. To configure the LT1186 into increment/decrement mode, tie $\overline{CS}$ to V_{CC} and pulse the UP/$\overline{DN}$ pin once on power-up.

Simplified Lamp Current Programming

A programming block in the LT1186 controls lamp current, permitting either grounded lamp or floating lamp configurations. Grounded configurations control lamp current by directly controlling one-half of actual lamp current and converting it to a feedback signal to close a control loop. Floating configurations control lamp current by directly controlling the Royer's primary-side converter current and generating a feedback signal to close a control loop.

Previous backlighting solutions have used a traditional error amplifier in the control loop to regulate lamp current. This approach converted an RMS current into a DC voltage for the input of the error amplifier. This approach used several time constants in order to provide stable loop frequency compensation. This compensation scheme meant that the loop had to be fairly slow and that output overshoot with start-up or overload conditions had to be carefully evaluated in terms of transformer stress and breakdown voltage requirements.

The LT1186 eliminates the error amplifier concept entirely and replaces it with a lamp current programming block. This block provides an easy-to-use interface to program lamp current. The programmer circuit also reduces the number of time constants in the control loop by combining the error signal conversion scheme and frequency compensation into a single capacitor. The control loop thus exhibits the response of a single pole system, allows for faster loop transient response and virtually eliminates overshoot under start-up or overload conditions.

Lamp current is programmed at the input of the programmer block, the I_{CCFL} pin. This pin is the input of a shunt regulator and accepts a DC input current signal of 0μA to 50μA from the DAC. This input signal is converted to a 0μA to 250μA source current at the CCFL V_C pin. The programmer circuit is simply a current-to-current converter with a gain of five. The typical input current programming range for 0mA to 6mA lamp current is 0μA to 50μA.

The I_{CCFL} pin is sensitive to capacitive loading and will oscillate with capacitance greater than 10pF. For example, loading the I_{CCFL} pin with a 1× or 10× scope probe causes oscillation and erratic CCFL regulator operation because of the probe's respective input capacitance. A current meter in series with the I_{CCFL} pin will also produce oscillation due to its shunt capacitance. Use a decoupling

PPLICATIONS INFORMATION

sistor of several kilohms between the I_{CCFL} pin and the JT pin if excessive trace stray capacitance exists. Nor-ılly, this resistor is not required.

some applications, the maximum programming current quired at the I_{CCFL} pin for a maximum lamp current will less than the full-scale output current of the DAC, which 50µA. The system designer can either limit the maxi-ım programming current through software built into the stem, or use a current splitter which shunts a percent-e of the full-scale current from the I_{CCFL} pin. A splitter cuit is illustrated in Figure 3. A divider string is used m a reference voltage to set up a voltage level equal to I_{CCFL} summing voltage, or 465mV. The main current wing in the divider string should be chosen to swamp t the effects of the shunted current into the divider ing.

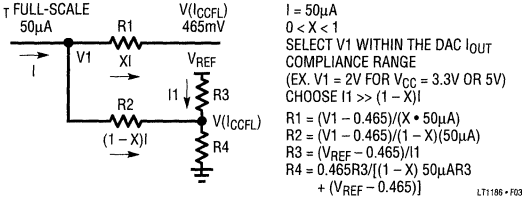


Figure 3

ounded Lamp Configuration

a grounded lamp configuration, the low voltage side of lamp connects directly to the LT1186 DIO pin. This pin the common connection between the cathode and ode of two internal diodes. In previous grounded lamp utions, these diodes were discrete units and are now egrated onto the IC, saving cost and board space. lirectional lamp current flows in the DIO pin and thus, diodes conduct alternately on half cycles. Lamp cur-ıt is controlled by monitoring one-half of the average ıp current. The diode conducting on negative half cles has one-tenth of its current diverted to the CCFL pin l nulls against the source current provided by the lamp rent programmer circuit. The compensation capacitor the CCFL V_C pin provides stable loop compensation and averaging function to the rectified sinusoidal lamp rent. Therefore, input programming current relates to e-half of average lamp current.

The transfer function between lamp current and input programming current must be empirically determined and is dependent on the particular lamp/display housing combination used. The lamp and display housing are a distributed loss structure due to parasitic lamp-to-frame capacitance. This means that the current flowing at the high-voltage side of the lamp is higher than what is flowing at the DIO pin side of the lamp. The input programming current is set to control lamp current at the high-voltage side of the lamp, even though the feedback signal is the lamp current at the bottom of the lamp. This ensures that the lamp is not overdriven which can degrade the lamp's operating lifetime. Therefore, the full scale current of the DAC does not necessarily correspond to the current required to set maximum lamp current.

Floating Lamp Configuration

In a floating lamp configuration, the lamp is fully floating with no galvanic connection to ground. This allows the transformer to provide symmetric differential drive to the lamp. Balanced drive eliminates the field imbalance associated with parasitic lamp-to-frame capacitance and reduces "thermometering" (uneven lamp intensity along the lamp length) at low lamp currents.

Carefully evaluate display designs in relation to the physical layout of the lamp, its leads and the construction of the display housing. Parasitic capacitance from any high voltage point to DC or AC ground creates paths for unwanted current flow. This parasitic current flow degrades electrical efficiency and losses up to 25% have been observed in practice. As an example, at a Royer operating frequency of 60kHz, 1pF of stray capacitance represents an impedance of 2.65MΩ. With an operating lamp voltage of 400V and an operating lamp current of 6mA, the parasitic current is 150µA. This additional current must be supplied by the transformer secondary. Layout techniques that increase parasitic capacitance include long high voltage lamp leads, reflective metal foil around the lamp and displays supplied in metal enclosures. Losses for a good display are under 5%, whereas, losses for a bad display range from 5% to 25%. Lossy displays are the primary reason to use a floating lamp configuration. Providing symmetric, differential drive to the lamp reduces the total parasitic loss by one-half.

APPLICATIONS INFORMATION

Maintaining closed-loop control of lamp current in a floating lamp configuration necessitates deriving a feedback signal from the primary side of the Royer transformer. Previous solutions have used an external precision shunt and high-side sense amplifier configuration. This approach has been integrated onto the LT1186 for simplicity of design and ease of use. An internal 0.1Ω resistor monitors the Royer converter current and connects between the input terminals of a high-side sense amplifier. A 0 – 1 Amp Royer primary-side, center-tap current is translated to a 0μA to 500μA sink current at the CCFL V_C pin to null against the source current provided by the lamp current programmer circuit. The compensation capacitor on the CCFL V_C pin provides stable loop compensation and an averaging function to the error sink current. Therefore, input programming current is related to average Royer converter current. Floating lamp circuits operate similarly to grounded lamp circuits except for the derivation of the feedback signal.

The transfer function between lamp current and input programming current must be empirically determined and is dependent upon a myriad of factors including lamp characteristics, display construction, transformer turns ratio and the tuning of the Royer oscillator. Once again, lamp current will be slightly higher at one end of the lamp and input programming current should be set for this higher level to ensure that the lamp is not overdriven.

The internal 0.1Ω high-side sense resistor on the LT1186 is rated for a maximum DC current of 1A. This resistor can be damaged by extremely high surge currents at start-up. The Royer converter typically uses a few microfarads of bypass capacitance at the center tap of the transformer. This capacitor charges up when the system is first powered by the battery pack or an AC wall adapter. The amount of current delivered at start-up can be very large if the total impedance in this path is small and the voltage source has high current capability. Linear Technology recommends the use of an aluminum electrolytic for the transformer center-tap bypass capacitor with an ESR greater than or equal to 0.5Ω. This lowers the peak surge currents to an acceptable level. In general, the wire and trace inductance in this path also help reduce the di/dt of the surge current. This issue only exists with floating lamp circuits as grounded lamp circuits do not make use of the high-sid sense resistor.

Input Capacitor Type

Caution must be used in selecting the input capacitor typ for switching regulators. Aluminum electrolytics are elec trically rugged and the lowest cost, but are physically larg to meet required ripple current ratings, and size cor straints (especially height) may preclude their use. Ce ramic capacitors are now available in larger values an their high ripple current and voltage rating make ther ideal for input bypassing. Cost is fairly high and footprir can be large.

Solid tantalum capacitors would be a good choice excep for a history of occasional failure when subjected to larg current surges during start-up. The input bypass capac tor of regulators can see these high surges when a batter or high capacitance source is connected. Some manufac turers have developed tantalum capacitor lines speciall tested for surge capability (AVX TPS series for instance but even these units may fail if the input voltage surg approaches the capacitor's maximum voltage rating. AV recommends derating the capacitor voltage by 2:1 for hig surge applications.

Applications Support

Linear Technology invests an enormous amount of time resources and technical expertise in understanding, de signing and evaluating backlight/LCD contrast solution for system designers. The design of an efficient an compact LCD backlight system is a study of compromis in a transduced electronic system. Every aspect of th design is interrelated and any design change require complete re-evaluation for all other critical design paran eters. Linear Technology has engineered one of the mos complete test and evaluation setups for backlight design and understands the issues and tradeoffs in achieving compact, efficient and economical customer solution Linear Technology welcomes the opportunity to discus design, evaluate and optimize any backlight/LCD contra system with a customer. For further information on back light/LCD contrast designs, consult the References.

APPLICATIONS INFORMATION

References

1. Williams, Jim. August 1992. *Illumination Circuitry for Liquid Crystal Displays.* Linear Technology Corporation, Application Note 49.

2. Williams, Jim. August 1993. *Techniques for 92% Efficient LCD Illumination.* Linear Technology Corporation, Application Note 55.

3. Bonte, Anthony. March 1995. *LT1182 Floating CCFL with Dual Polarity Contrast.* Linear Technology Corporation, Design Note 99.

4. Williams, Jim. April 1995. *A Precision Wideband Current Probe for LCD Backlight Measurement.* Linear Technology Corporation, Design Note 101.

5. LT1182/LT1183/LT1184/LT1184F Data Sheet. *CCFL/LCD Contrast Switching Regulators.* April 1995. Linear Technology Corporation.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1107	Micropower DC/DC Converter for LCD Contrast Control	1A, 63kHz, Hysteretic
LT1172	Current Mode Switching Regulator for CCFL or LCD Contrast Control	1.25A, 100kHz
LT1173	Micropower DC/DC Converter for LCD Contrast Control	1A, 24kHz, Hysteretic
LT1182	Dual Current Mode Switching Regulator for CCFL and LCD Contrast Control	1.25A, 0.625A, 200kHz
LT1183	Dual Current Mode Switching Regulator for CCFL and LCD Contrast Control	1.25A, 0.625A, 200kHz
LT1184	Current Mode Switching Regulator for CCFL Control	1.25A, 200kHz
LT1184F	Current Mode Switching Regulator for CCFL Control	1.25A, 200kHz
LT1372	Current Mode Switching Regulator for CCFL or LCD Contrast Contol	1.5A, 500kHz

1.2A, High Efficiency Step-Down DC/DC Converter

FEATURES

- **High Efficiency: Up to 95%**
- Current Mode Operation for Excellent Line and Load Transient Response
- **Internal 0.3Ω Power Switch (V_{IN} = 10V)**
- Short-Circuit Protection
- Low Dropout Operation: 100% Duty Cycle
- Low-Battery Detector
- Low 160μA Standby Current at Light Loads
- Active-High Micropower Shutdown: I_Q < 15μA
- Peak Inductor Current Independent of Inductor Value
- Available in 14-pin SO Package

APPLICATIONS

- 5V to 3.3V Conversion
- Distributed Power Systems
- Step-Down Converters
- Inverting Converters
- Memory Backup Supply
- Portable Instruments
- Battery-Powered Equipment
- Cellular Telephones

DESCRIPTION

The LTC®1265 is a monolithic step-down current mode DC/DC converter featuring Burst Mode™ operation at low output current. The LTC1265 incorporates a 0.3Ω switch (V_{IN} =10V) allowing up to 1.2A of output current.

Under no load condition, the converter draws only 160μA. In shutdown it typically draws a mere 5μA making this converter ideal for current sensitive applications. In dropout the internal P-channel MOSFET switch is turned on continuously maximizing the life of the battery source. The LTC1265 incorporates automatic power saving Burst Mode operation to reduce gate charge losses when the load currents drop below the level required for continuous operation.

The inductor current is user-programmable via an external current sense resistor. Operation up to 700kHz permits the use of small surface mount inductors and capacitors.

For applications requiring higher output currents, see the LTC1148 data sheet. For applications requiring less than 450mA, see the LTC1174 data sheet.

TYPICAL APPLICATION

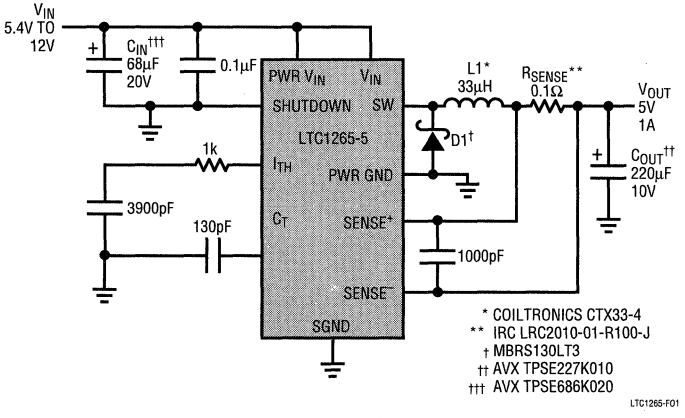
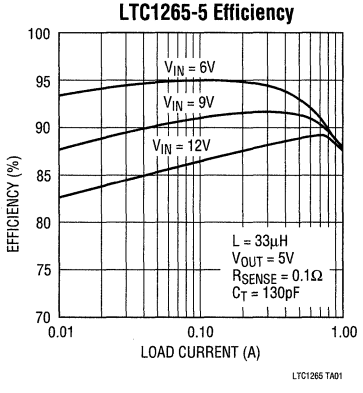


Figure 1. High Efficiency Step-Down Converter

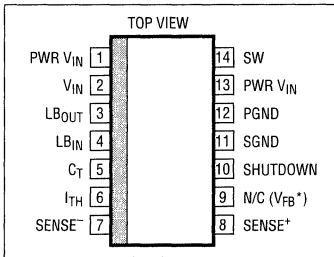


IBSOLUTE MAXIMUM RATINGS

oltages Refer to GND Pin)

put Supply Voltage (Pins 1, 2, 13) ..... –0.3V to 13V
C Switch Current (Pin 14) 1.2A
eak Switch Current (Pin 14) 1.6A
witch Voltage (Pin 14) ..... V_{IN} – 13.0
perating Temperature Range ..... 0° to 70°C
nction Temperature (Note 1) ..... 125°C
orage Temperature Range ..... –65° to 150°C
ad Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
14-LEAD PLASTIC SO

*ADJUSTABLE OUTPUT VERSION

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1265CS
LTC1265CS-5
LTC1265CS-3.3

Consult factory for Industrial and Military grade parts.

LECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, $V_{SHUTDOWN}$ = 0V, unless otherwise specified.

MBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Feedback Current into Pin 9	LTC1265			0.2	1	µA
	Feedback Voltage	LTC1265	●	1.22	1.25	1.28	V
JT	Regulator Output Voltage	LTC1265-3.3: I_{LOAD} = 800mA	●	3.22	3.3	3.40	V
		LTC1265-5: I_{LOAD} = 800mA	●	4.9	5	5.2	V
OUT	Output Voltage Line Regulation	V_{IN} = 6.5V to 10V, I_{LOAD} = 800mA		–40	0	40	mV
	Output Voltage Load Regulation	LTC1265-3.3: 10mA < I_{LOAD} < 800mA			40	65	mV
		LTC1265-5: 10mA < I_{LOAD} < 800mA			60	100	mV
	Burst Mode Output Ripple	I_{LOAD} = 0mA			50		mV_{P-P}
	Input DC Supply Current (Note 2)	Active Mode: 3.5V < V_{IN} < 10V			1.8	2.4	mA
		Sleep Mode: 3.5V < V_{IN} < 10V			160	230	µA
		Sleep Mode: 5V < V_{IN} < 10V (LTC1265-5)			160	230	µA
		Shutdown: $V_{SHUTDOWN}$ = V_{IN}, 3.5V < V_{IN} < 10V			5	15	µA
TRIP	Low-Battery Trip Point			1.15	1.25	1.35	V
N	Current into Pin 4					0.5	µA
UT	Current Sunk by Pin 3	V_{LBOUT} = 0.4V, V_{LBIN} = 0V		0.5	1.0	1.5	mA
		V_{LBOUT} = 5V, V_{LBIN} = 10V				1.0	µA
– V_7	Current Sense Threshold Voltage	LTC1265: V_{SENSE^-} = 5V, V_9 = V_{OUT}/4 + 25mV (Forced)			25		mV
		V_{SENSE^-} = 5V, V_9 = V_{OUT}/4 – 25mV (Forced)	●	135	150	180	mV
		LTC1265-3.3: V_{SENSE^-} = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE^-} = V_{OUT} – 100mV (Forced)	●	135	150	180	mV
		LTC1265-5: V_{SENSE^-} = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE^-} = V_{OUT} – 100mV (Forced)	●	135	150	180	mV
N	ON Resistance of Switch		●		0.3	0.60	Ω
	C_T Pin Discharge Current	V_{OUT} in Regulation, V_{SENSE^-} = V_{OUT}		50	70	90	µA
		V_{OUT} = 0V			2	10	µA
:	Switch Off-Time (Note 3)	C_T = 390pF, I_{LOAD} = 800mA	●	4	5	6	µs
	Shutdown Pin High	Min Voltage at Pin 10 for Device to be in Shutdown		1.2			V
	Shutdown Pin Low	Max Voltage at Pin 10 for Device to be Active				0.6	V
	Shutdown Pin Input Current	$V_{SHUTDOWN}$ = 8V				0.5	µA

4

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range.

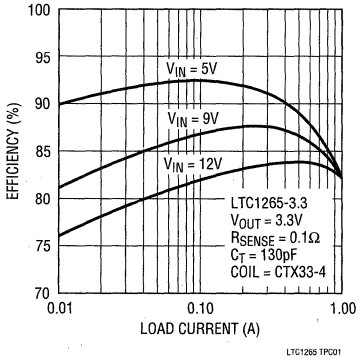
Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:
LTC1265CS, LTC1265CS-3.3, LTC1265CS-5:
$T_J = T_A + (P_D \times 110°C/W)$

Note 2: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

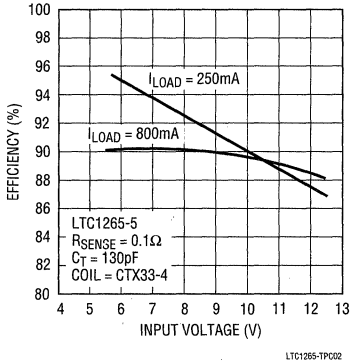
Note 3: In applications where R_{SENSE} is placed at ground potential, the off-time increases by approximately 40%.

TYPICAL PERFORMANCE CHARACTERISTICS

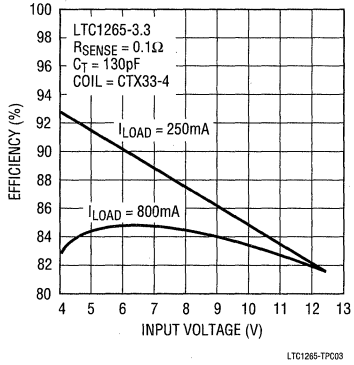
Efficiency vs Load Current



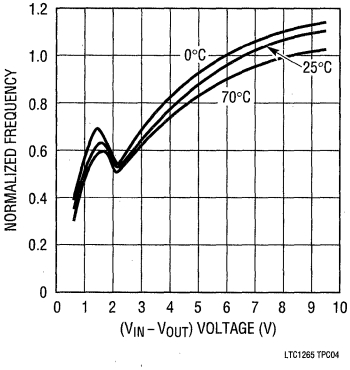
Efficiency vs Input Voltage (V_{OUT} = 5V)



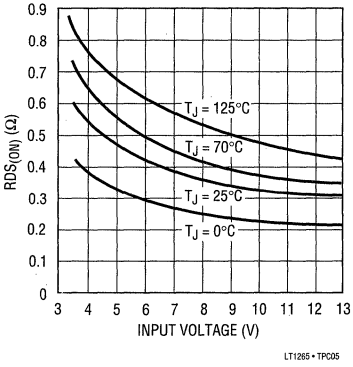
Efficiency vs Input Voltage (V_{OUT} = 3.3V)



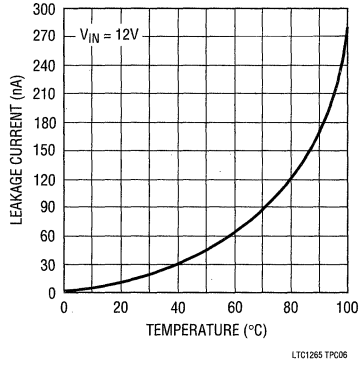
Operating Frequency vs (V_{IN} – V_{OUT})



Switch Resistance

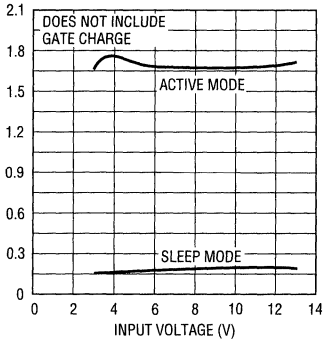


Switch Leakage Current

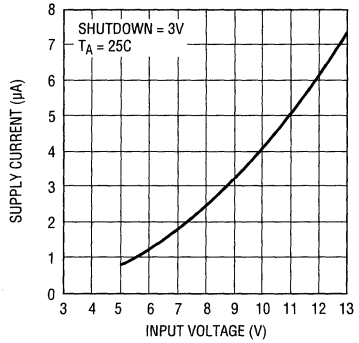


YPICAL PERFORMANCE CHARACTERISTICS

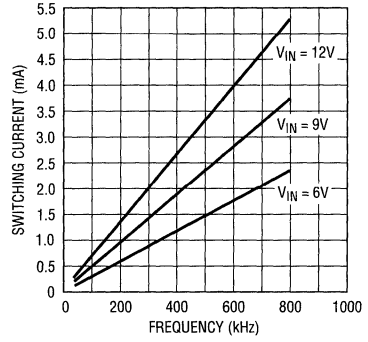
DC Supply Current



Supply Current in Shutdown



Gate Charge Losses



IN FUNCTIONS

VR V_{IN} (Pins 1, 13): Supply for the Power MOSFET and Driver. Must decouple this pin properly to ground. Must vays tie pins 1 and 13 together.

I (Pin 2): Main Supply for all the control circuitry in the C1265.

OUT (Pin 3): Open Drain Output of the Low-Battery mparator. This pin will sink current when pin 4 (LB_{IN}) es below 1.25V. During shutdown, this pin is high pedance.

IN (Pin 4): The (–) Input of the Low-Battery Comparator. e (+) Input is connected to a reference voltage of 1.25V.

(Pin 5): External capacitor C_T from pin 5 to ground sets switch off-time. The operating frequency is dependent the input voltage and C_T.

(Pin 6): Feedback Amplifier Decoupling Point. The rent comparator threshold is proportional to pin 6 tage.

NSE⁻ (Pin 7): Connect to the (–) Input of the current mparator. For LTC1265-3.3 and LTC1265-5, it also nects to an internal resistive divider which sets the tput voltage.

SENSE⁺ (Pin 8): The (+) Pin to the Current Comparator. A built-in offset between pins 7 and 8 in conjunction with R_{SENSE} sets the current trip threshold.

N/C, V_{FB} (Pin 9): For the LTC1265 adjustable version, this pin serves as the feedback pin from an external resistive divider used to set the output voltage. On the LTC1265-3.3 and LTC1265-5 versions, this pin is not used.

Shutdown (Pin 10): Pulling this pin HIGH keeps the internal switch off and puts the LTC1265 in micropower shutdown. Do not float this pin.

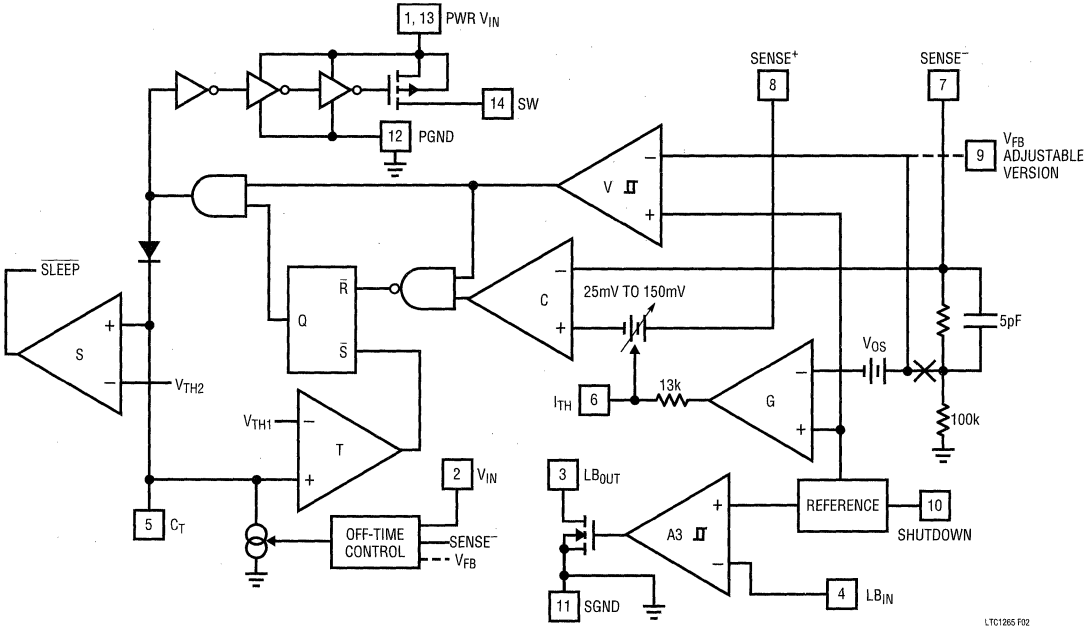
SGND (Pin 11): Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

PGND (Pin 12): Switch Driver Ground. Connects to the (–) terminal of C_{IN}. Anode of the Schottky diode must be connected close to this pin.

SW (Pin 14): Drain of the P-Channel MOSFET Switch. Cathode of the Schottky diode must be connected close to this pin.

4

FUNCTIONAL DIAGRAM (Pin 9 connection shown for LTC1265-3.3 and LTC1265-5; change create LTC1265)



OPERATION (Refer to Functional Diagram)

The LTC1265 uses a constant off-time architecture to switch its internal P-channel power MOSFET. The off-time is set by an external timing capacitor at C_T (pin 5). The operating frequency is then determined by the off-time and the difference between V_{IN} and V_{OUT}.

The output voltage is set by an internal resistive divider (LTC1265-3.3 and LTC1265-5) connected to Sense$^-$ (pin 7) or an external divider returned to V_{FB} (pin 9 for LTC1265). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V.

To optimize efficiency, the LTC1265 automatically switches between continuous and Burst Mode operation. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

When the load is heavy, the LTC1265 is in continuous operation. During the switch ON time, current comparator C monitors the voltage between pins 7 and 8 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches the comparator's threshold value, its output signal will change state, settin the flip flop and turning the internal P-channel MOSFET of The timing capacitor connected to pin 5 is now allowed t discharge at a rate determined by the off-time controller

When the voltage on the timing capacitor has discharge past V_{TH1}, comparator T trips, sets the flip flop and cause the switch to turn on. Also, the timing capacitor is re charged. The inductor current will again ramp up until th current comparator C trips. The cycle then repeats.

When the load current increases, the output voltage de creases slightly. This causes the output of the gain stag (pin 6) to increase the current comparator threshold, thu tracking the load current.

When the load is relatively light, the LTC1265 automati cally goes into Burst Mode operation. The current loop i interrupted when the output voltage exceeds the desire regulated value. The hysteretic voltage comparator V trip when V_{OUT} is above the desired output voltage, shuttin off the switch and causing the capacitor to discharge. Thi capacitor discharges past V_{TH1} until its voltage drop

›PERATION (Refer to Functional Diagram)

:low V_{TH2}. Comparator S then trips and a sleep signal is :nerated. The circuit now enters into sleep mode with the)wer MOSFET turned off. In sleep mode, the LTC1265 is standby and the load current is supplied by the output pacitor. All unused circuitry is shut off, reducing quies- nt current from 2mA to 160µA. When the output capaci- r discharges by the amount of the hysteresis of the mparator V, the P-channel switch turns on again and the ocess repeats itself. During Burst Mode operation the ak inductor current is set at $25mV/R_{SENSE}$.

avoid the operation of the current loop interfering with ırst Mode operation, a built-in offset V_{OS} is incorporated in the gain stage. This prevents the current from increasing until the output voltage has dropped below a minimum threshold.

Using constant off-time architecture, the operating frequency is a function of the voltage. To minimize the frequency variation as dropout is approached, the off-time controller increases the discharge current as V_{IN} drops below V_{OUT} + 2V. In dropout the P-channel MOSFET is turned on continuously (100% duty cycle) providing low dropout operation with $V_{OUT} \cong V_{IN}$.

PPLICATIONS INFORMATION

e basic LTC1265 application circuit is shown in Figure External component selection is driven by the load ıuirement, and begins with the selection of R_{SENSE}. ce R_{SENSE} is known, C_T and L can be chosen. Next, the hottky diode D1 is selected followed by C_{IN} and C_{OUT}.

ENSE Selection for Output Current

ENSE is chosen based on the required output current. th the current comparator monitoring the voltage devel- ed across R_{SENSE}, the threshold of the comparator termines the peak inductor current. Depending on the d current condition, the threshold of the comparator s between $25mV/R_{SENSE}$ and $150mV/R_{SENSE}$. The maxi- ım output current of the LTC1265 is:

$$I_{OUT(MAX)} = \frac{150mV}{R_{SENSE}} - \frac{I_{RIPPLE}}{2} \text{ (A)}$$

ere I_{RIPPLE} is the peak-to-peak inductor ripple current.

a relatively light load, the LTC1265 is in Burst Mode eration. In this mode the peak inductor current is set at mV/R_{SENSE}. To fully benefit from Burst Mode operation, inductor current should be continuous during burst iods. Hence, the peak-to-peak inductor ripple current ıst not exceed $25mV/R_{SENSE}$.

account for light and heavy load conditions, the $I_{OUT(MAX)}$ hen given by:

$$I_{OUT(MAX)} = \frac{150mV}{R_{SENSE}} - \frac{25mV}{2 \times R_{SENSE}} \text{ (A)}$$

$$= \frac{137.5mV}{R_{SENSE}} \text{ (A)}$$

Solving for R_{SENSE} and allowing a margin of variations in the LTC1265 and extended component values yields:

$$R_{SENSE} = \frac{100mV}{I_{OUT(MAX)}} (\Omega) \quad (1)$$

The LTC1265 is rated with a capability to supply a maximum of 1.2A of output current. *Therefore, the minimum value of R_{SENSE} that can be used is 0.083Ω.* A graph for selecting R_{SENSE} versus maximum output is given in Figure 2.

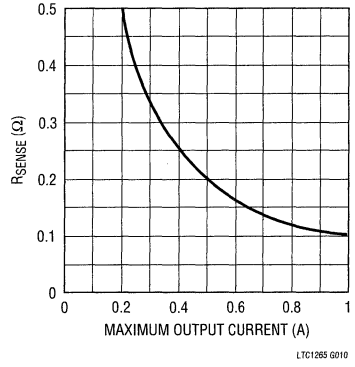


Figure 2. Selecting R_{SENSE}

4

APPLICATIONS INFORMATION

Under short-circuit condition, the peak inductor current is determined by:

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}} \text{ (A)}$$

In this condition, the LTC1265 automatically extends the off-time of the P-channel MOSFET to allow the inductor current to decay far enough to prevent any current build-up. The resulting ripple current causes the average short-circuit current to be approximately $I_{OUT(MAX)}$.

C_T and L Selection for Operating Frequency

The LTC1265 uses a constant off-time architecture with t_{OFF} determined by an external capacitor C_T. Each time the P-channel MOSFET turns on, the voltage on C_T is reset to approximately 3.3V. During the off-time , C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise, decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency:

$$C_T = \frac{1}{1.3 \times 10^4 \times f}\left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right)(F) \quad (2)$$

where V_D is the drop across the Schottky diode.

As the operating frequency is increased the gate charge losses will reduce efficiency. The complete expression for operating frequency is given by:

$$f \approx \frac{1}{t_{OFF}}\left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right)(Hz)$$

where:

$$t_{OFF} = 1.3 \times 10^4 \times C_T \times \left(\frac{V_{REG}}{V_{OUT}}\right)(sec)$$

V_{REG} is the desired output voltage (i.e. 5V, 3.3V). V_{OUT} is the measured output voltage. Thus V_{REG}/V_{OUT} = 1 in regulation.

Note that as V_{IN} decreases, the frequency decreases. When the input-to-output voltage differential drops below 2V, the LTC1265 reduces t_{OFF} by increasing the discharg current in C_T. This prevents audible operation prior t dropout. (See shelving effect shown in the Operatin Frequency curve under Typical Performance Characteris tics.)

To maintain continuous inductor current at light load, th inductor must be chosen to provide no more than 25mV R_{SENSE} of peak-to-peak ripple current. This results in th following expression for L:

$$L \geq 5.2 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG} \quad (3)$$

Using an inductance smaller than the above value wil result in the inductor current being discontinuous. A consequence of this is that the LTC1265 will delay enterin Burst Mode operation and efficiency will be degraded a low currents.

Inductor Core Selection

With the value of L selected, the type of inductor must b chosen. Basically, there are two kinds of losses in a inductor; core and copper losses.

Core losses are dependent on the peak-to-peak ripp current and core material. However it is independent of th physical size of the core. By increasing the inductance, th peak-to-peak inductor ripple current will decrease, there fore reducing core loss. Utilizing low core loss material such as molypermalloy or Kool Mμ® will allow user t concentrate on reducing copper loss and preventing satu ration.

Although higher inductance reduces core loss, it increase copper loss as it requires more windings. When space i not at a premium, larger wire can be used to reduce th wire resistance. This also prevents excessive heat dissipa tion.

CATCH DIODE SELECTION

Losses in the catch diode depend on forward drop an switching times. Therefore Schottky diodes are a goo choice for low drop and fast switching times.

The catch diode carries load current during the off-time The average diode current is therefore dependent on th

Kool Mμ is a registered trademark of Magnetics, Inc.

IPPLICATIONS INFORMATION

-channel switch duty cycle. At high input voltages, the iode conducts most of the time. As V_{IN} approaches V_{OUT}, ıe diode conducts only a small fraction of the time. The ıost stressful condition for the diode is when the output short circuited. Under this condition, the diode must ıfely handle $I_{SC(PK)}$ at close to 100% duty cycle. Most TC1265 circuits will be well served by either a 1N5818 or MBRS130LT3 Schottky diode. An MBRS0520 is a good ıoice for $I_{OUT(MAX)} \leq 500mA$.

IN

ı continuous mode, the input current of the converter is square wave of duty cycle V_{OUT}/V_{IN}. To prevent large ɔltage transients, a low ESR input capacitor must be ɜed. In addition, the capacitor must handle a high RMS ırrent. The C_{IN} RMS current is given by:

$$IRMS \approx \frac{I_{OUT}[V_{OUT}(V_{IN}-V_{OUT})]^{1/2}}{V_{IN}} \quad (ARMS) \quad (4)$$

ıis formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case is commonly used for ɜsign because even significant deviations do not offer ıuch relief. Note that capacitor manufacturer's ripple ırrent ratings are often based on only 2000 hours life-ne. This makes it advisable to further derate the capaci-r, or to choose a capacitor rated at a higher temperature an required. **Do not underspecify this component**. An ıdditional 0.1µF ceramic capacitor is also required on /R V_{IN} for high frequency decoupling.

ɔUT

ıe selection of C_{OUT} is based upon the effective series sistance (ESR) for proper operation of the LTC1265. ıe required ESR of C_{OUT} is:

$$ESR_{COUT} < 50mV/I_{RIPPLE}$$

here I_{RIPPLE} is the ripple current of the inductor. For the ıse where the I_{RIPPLE} is $25mV/R_{SENSE}$, the required ESR C_{OUT} is:

$$ESR_{COUT} < 2R_{SENSE} \quad (5)$$

ɔ avoid overheating, the output capacitor must be sized handle the ripple current generated by the inductor. The worst case RMS ripple current in the output capacitor is given by:

$$IRMS \approx \frac{150mV}{2 \times R_{SENSE}} \quad (ARMS)$$

Generally, once the ESR requirement for C_{OUT} has been met, the RMS current rating far exceeds the $I_{RIPPLE(P-P)}$ requirement.

ESR is a direct function of the volume of the capacitor. Manufacturers such as Nichicon, AVX and Sprague should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR for its size at a somewhat higher price.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolyte and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are both available in surface mount configuration and are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, available in case heights ranging from 2mm to 4mm. Consult the manufacturer for other specific recommendations.

When the capacitance of C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1265 would normally be in continuous operation. The effect will be most pronounced with low value of R_{SENSE} and can be improved at higher frequencies with lower values of L.

Low-Battery Detection

The low-battery comparator senses the input voltage through an external resistive divider. This divided voltage connects to the (–) input of a voltage comparator (pin 4) which is compared with a 1.25V reference voltage. Neglecting pin 4 bias current, the following expression is used for setting the trip limit:

$$V_{LB\_TRIP} = 1.25\left(1 + \frac{R4}{R3}\right)$$

APPLICATIONS INFORMATION

The output, pin 3, is an N-channel open drain which goes low when the battery voltage is below the threshold set by R3 and R4. In shutdown, the comparator is disabled and pin 3 is in a high impedance state.

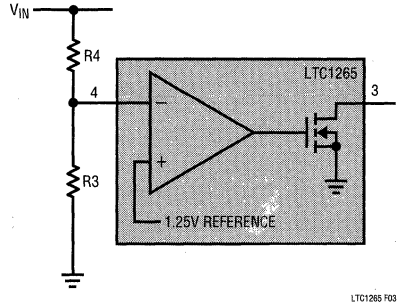


Figure 3. Low-Battery Comparator

LTC1265 ADJUSTABLE APPLICATIONS

The LTC1265 develops a 1.25V reference voltage between the feedback (pin 9) terminal and signal ground (see Figure 4). By selecting resistor R1, a constant current is caused to flow through R1 and R2 to set overall output voltage. The regulated output voltage is determined by:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

For most applications a 30k resistor is suggested for R1. To prevent stray pickup, a 100pF capacitor is suggested across R1 located close to the LTC1265.

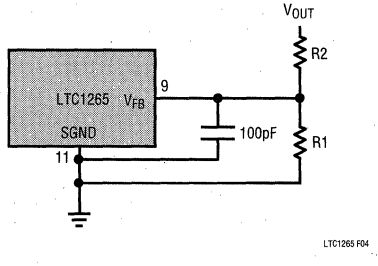


Figure 4. LTC1265 Adjustable Configuration

THERMAL CONSIDERATIONS

In a majority of applications, the LTC1265 does not dissipate much heat due to its high efficiency. However, in applications where the switching regulator is running at high duty cycles or the part is in dropout with the switch turned on continuously (DC), the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated by the regulator exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = P \times \theta_{JA}$$

where P is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature is simply given by:

$$T_J = T_R + T_A$$

As an example, consider the LTC1265 is in dropout at an input voltage of 4V with a load current of 0.5A. From the Typical Performance Characteristics graph of Switch Resistance, the ON resistance of the P-channel is 0.55Ω. Therefore power dissipated by the part is:

$$P = I^2 \times R_{DSON} = 0.1375W$$

For the SO package, the θ_{JA} is 110°C/W.

Therefore the junction temperature of the regulator when it is operating in ambient temperature of 25°C is:

$$T_J = 0.1375 \times 110 + 25 = 40.1°C$$

Remembering that the above junction temperature is obtained from a R_{DSON} at 25°C, we need to recalculate the junction temperature based on a higher R_{DSON} since it increases with temperature. However, we can safely assume that the actual junction temperature will not exceed the absolute maximum junction temperature of 125°C.

Now consider the case of a 1A regulator with V_{IN} = 4V and T_A = 65°C. Starting with the same 0.55Ω assumption for R_{DSON}, the T_J calculation will yield 125°C. But from the graph, this will increase the R_{DSON} to 0.76Ω, which when used in the above calculation yields an actual T_J > 148°C. Therefore the LTC1265 would be unsuitable for a 4V input, 1A output regulator operating at T_A = 65°C.

PPLICATIONS INFORMATION

ıard Layout Checklist

hen laying out the printed circuit board, the following ecklist should be used to ensure proper operation of the C1265. These items are also illustrated graphically in ɜ layout diagram of Figure 5. Check the following in your ʻout:

Are the signal and power grounds segregated? The LTC1265 signal ground (pin 11) must return to the (–) plate of C_{OUT}. The power ground (pin 12) returns to the anode of the Schottky diode, and the (–) plate of C_{IN}, whose leads should be as short as possible.

Does the (+) plate of the C_{IN} connect to the power V_{IN} (pins 1,13) as close as possible? This capacitor provides the AC current to the internal P-channel MOSFET and its driver.

Is the input decoupling capacitor (0.1µF) connected closely between power V_{IN} (pins 1,13) and power ground (pin 12)? This capacitor carries the high frequency peak currents.

4. Is the Schottky diode closely connected between the power ground (pin 12) and switch (pin 14)?
5. Does the LTC1265 Sense⁻ (pin 7) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and signal ground.
6. Are the Sense⁻ and Sense⁺ leads routed together with minimum PC trace spacing? The 1000pF capacitor between pins 7 and 8 should be as close as possible to the LTC1265.
7. Is Shutdown (pin 10) actively pulled to ground during normal operation? The Shutdown pin is high impedance and must not be allowed to float.

4

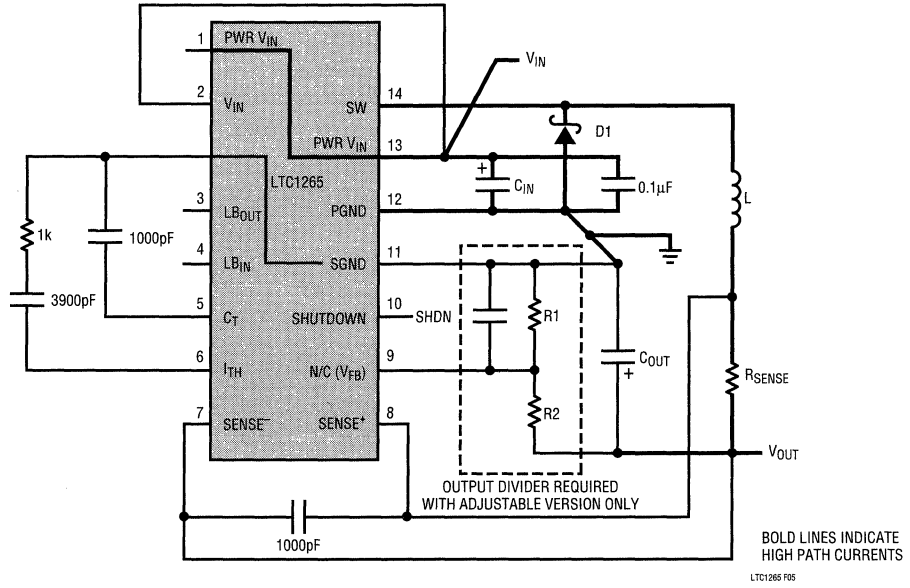


Figure 5. LTC1265 Layout Diagram (See Board Layout Checklist)

APPLICATIONS INFORMATION

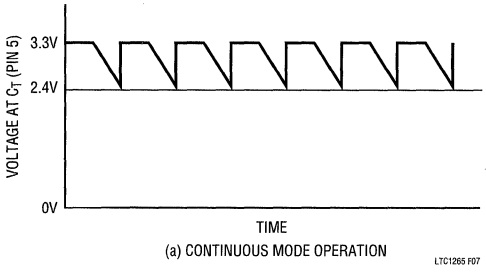
Troubleshooting Hints

Since efficiency is critical to LTC1265 applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. As the LTC1265 is highly tolerant of poor layout, the output voltage will still be regulated. Therefore, monitoring the output voltage will not tell you whether you have a good or bad layout. The waveform to monitor is the voltage on the timing capacitor pin 5.

In continuous mode the voltage on the C_T pin is a sawtooth with approximately $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 6a.

When the load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation occurs. The voltage on C_T pin now falls to ground for periods of time as shown in Figure 6b. During this time the LTC1265 is in sleep mode with quiescent current reduced to 160μA.

The inductor current should also be monitored. If the circuit is poorly decoupled, the peak inductor current will be haphazard as in Figure 7a. A well decoupled LTC1265 has a clean inductor current as in Figure 7b.



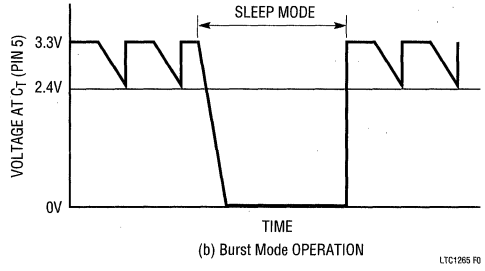
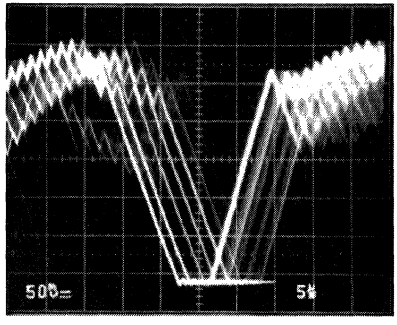
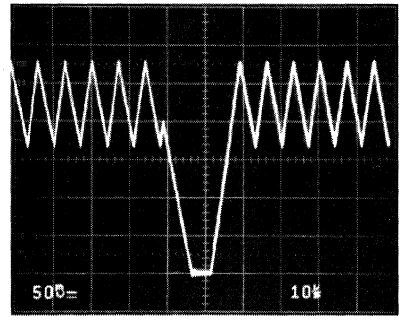


Figure 6. C_T Waveforms



(a) POORLY DECOUPLED LTC1265



(b) WELL DECOUPLED LTC1265

Figure 7. Inductor Waveforms

APPLICATIONS INFORMATION

Design Example

As a design example, assume V_{IN} = 5V, V_{OUT} = 3.3V, I_{MAX} = 0.8A and f = 250kHz. With this information we can easily calculate all the important components.

From (1),

$$R_{SENSE} = 100mV/0.8 = 0.125\Omega$$

From (2) and assuming V_D = 0.4V,

$$C_T \cong 100pF$$

Using (3), the value of the inductor is:

$$L \geq 5.2 \times 10^5 \times 0.125 \times 100pF \times 3.3V = 22\mu H$$

For the catch diode, a MBRS130LT3 or 1N5818 will be sufficient in this application.

C_{IN} will require an RMS current rating of at least 0.4A at temperature, and C_{OUT} will require an ESR of (from 5):

$$ESR_{COUT} < 0.25\Omega$$

The inductor ripple current is given by:

$$I_{RIPPLE} = \left(\frac{V_{OUT} + V_D}{L}\right) t_{OFF} = 0.22A$$

At light loads the peak inductor current is at:

$$I_{PEAK} = 25mV/0.125 = 0.2A$$

Therefore, at load current less than 0.1A the LTC1265 will be in Burst Mode operation. Figure 8 shows the complete circuit and Figure 9 shows the efficiency curve with the above calculated component values.

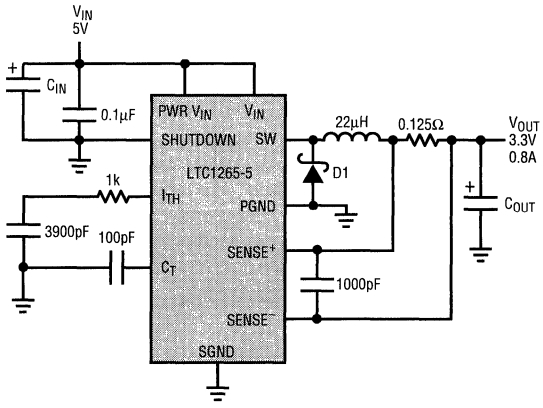


Figure 8. Design Example Circuit

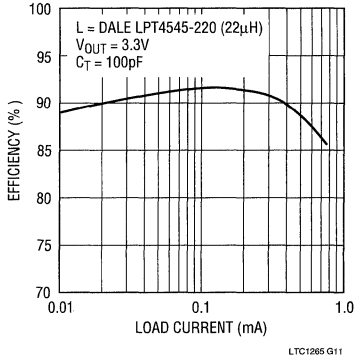
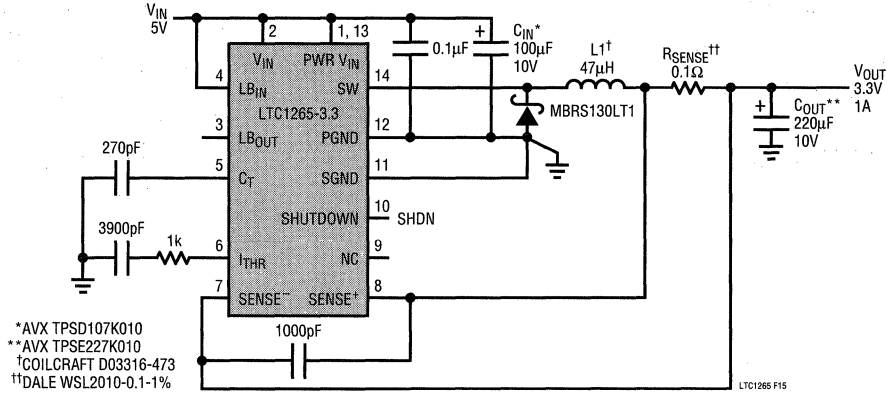


Figure 9. Design Example Efficiency Curve

TYPICAL APPLICATIONS

High Efficiency 5V to 3.3V Converter



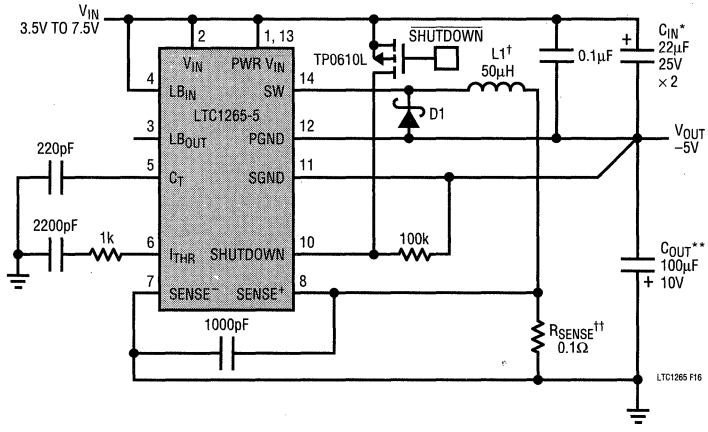
Positive-to-Negative (–5V) Converter

*AVX TPSD226K025
**AVX TPSD107K010
†L1 SELECTION

MANUFACTURER	PART NO.
COILCRAFT	DO3316-473
COILTRONICS	CTX50-4
DALE	LPT4545-500LA
SUMIDA	CD74-470

††IRC LRC2010-01-R100-J
D1= MBRS130LT3

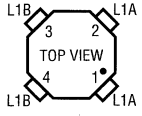
V_{IN} (V)	$I_{OUT(MAX)}$ (mA)
3.5	360
4.0	430
5.0	540
6.0	630
7.0	720
7.5	740



TYPICAL APPLICATIONS

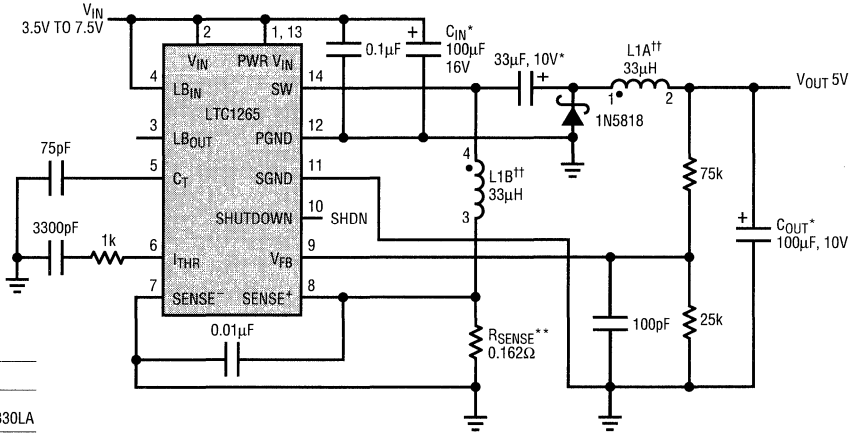
5V Buck-Boost Converter

V_{IN} (V)	$I_{OUT(MAX)}$ (mA)
3.5	240
4.0	275
5.0	365
6.0	490
7.0	610
7.5	665



*SANYO OS-CON CAPACITOR
**IRC LRC2010-01-R162-J
†L1A, L2A SELECTION

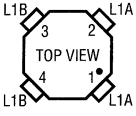
MANUFACTURER	PART NO.
COILTRONICS	CTX33-4
DALE	LPT4545-330LA



LTC1265 F09

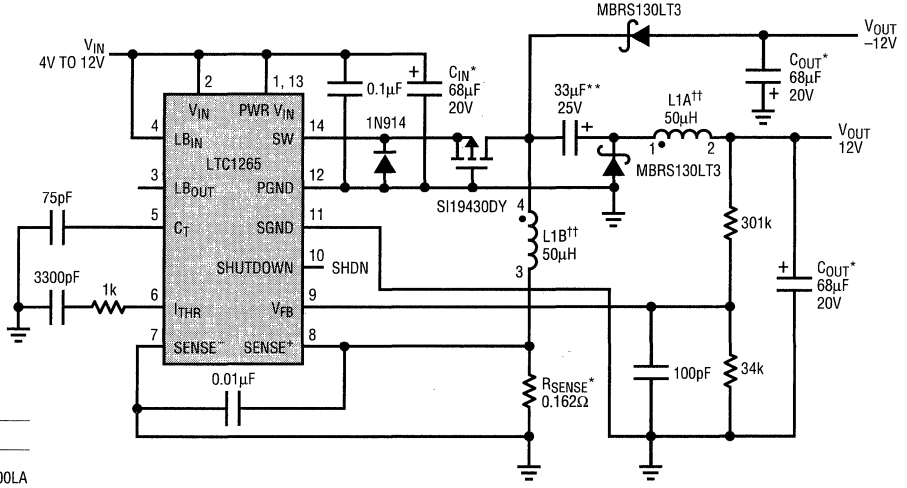
9V to 12V and – 12V Outputs

V_{IN} (V)	$I_{OUT(MAX)}$ (mA)
1.0	40
3.0	60
5.0	80
7.0	100
9.0	115
11.0	130
10.0	150
11.0	165
12.0	180



*AVX TPSE686K020
*AVX TPSE336K025
†IRC LRC2010-01-R162-J
†L1A,L2A SELECTION

MANUFACTURER	PART NO.
COILTRONICS	CTX50-4
DALE	LPT4545-500LA

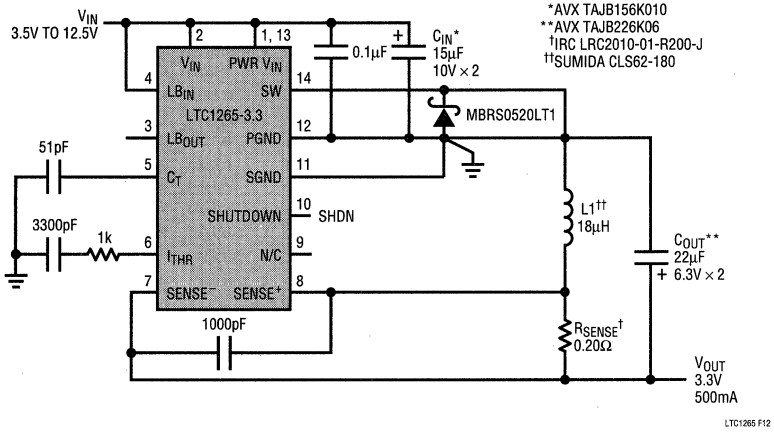


LTC1265 F10

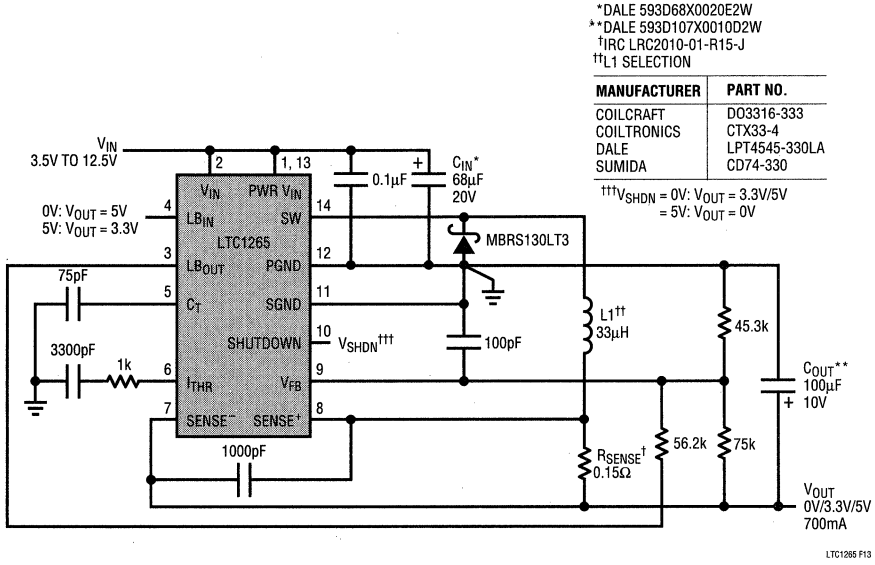
4

TYPICAL APPLICATIONS

2.5mm Max Height 5V-to-3.3V (500mA)

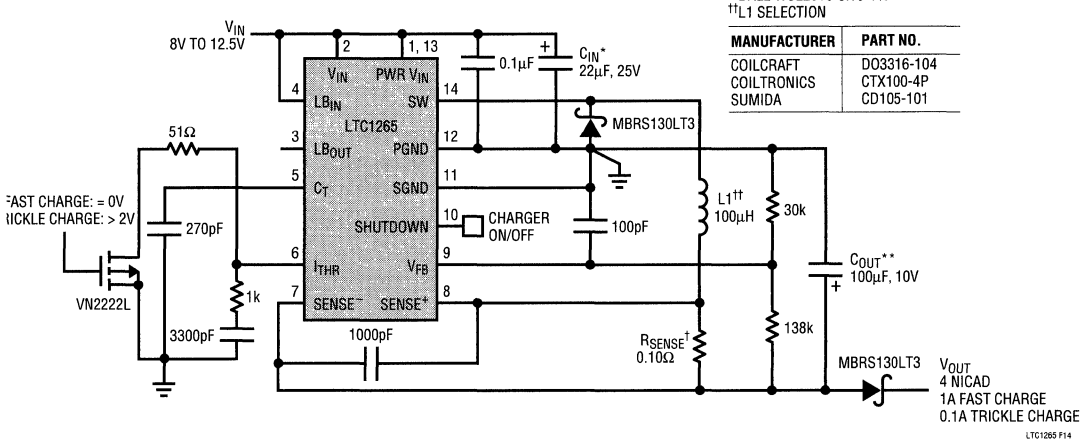


Logic Selectable 0V/3.3V/5V 700mA Regulator



YPICAL APPLICATIONS

4-NiCad Battery Charger



*DALE 593D226X0025D2W
**DALE 593D107X0016E2W
†DALE WSL2010-0.10-1%
††L1 SELECTION

MANUFACTURER	PART NO.
COILCRAFT	DO3316-104
COILTRONICS	CTX100-4P
SUMIDA	CD105-101

ELATED PARTS

ART NUMBER	DESCRIPTION	COMMENTS
C1142	Dual Step-Down Switching Regulator Controller	Dual Version of LTC1148
C1143	Dual Step-Down Switching Regulator Controller	Dual Version of LTC1147
C1147	Step-Down Switching Regulator Controller	Nonsynchronous, 8-Pin, $V_{IN} \leq 16V$
C1148	Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 20V$
C1149	Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 48V$, for Standard Threshold FETs
C1159	Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 40V$, for Logic Level FETs
C1174	Step-Down Switching Regulator with Internal 0.5A Switch	$V_{IN} \leq 18.5V$, Comparator/Low Battery Detector
C1266	Step-Up/Down Switching Regulator Controller	Synchronous N- or P-Channel FETs, Comparator/Low Battery Detector
C1574	Step-Down Switching Regulator with Internal 0.5A Switch and Schottky Diode	$V_{IN} \leq 18.5V$, Comparator

Synchronous Regulator Controller for N- or P-Channel MOSFETs

FEATURES

- **Ultra-High Efficiency: Over 95% Possible**
- **Drives N-Channel MOSFET for High Current or P-Channel MOSFET for Low Dropout**
- Pin Selectable Burst Mode Operation
- 1% Output Accuracy (LTC1266A)
- Pin Selectable Phase of Topside Driver for Boost or Step-Down Operation
- Wide V_{IN} Range: 3.5V to 20V
- On-Chip Low-Battery Detector
- High Efficiency Maintained over Large Current Range
- Low 170μA Standby Current at Light Loads
- Current Mode Operation for Excellent Line and Load Transient Response
- Logic Controlled Micropower Shutdown: I_Q < 40μA
- Short Circuit Protection
- Synchronous Switching with Nonoverlaping Gate Drives
- Available in 16-Pin Narrow SO Package

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Cellular Telephones
- DC Power Distribution Systems
- GPS Systems

DESCRIPTION

The LTC®1266 series is a family of synchronous switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. These devices drive external power MOSFETs at switching frequencies up to 400kHz using a constant off-time current mode architecture providing constant ripple current in the inductor. They can drive either an N-channel or a P-channel topside MOSFET.

The operating current level is user-programmable via an external current sense resistor. Wide input supply range allows operation from 3.5V to 18V (20V maximum). Constant off-time architecture provides low dropout regulation limited only by the $R_{DS(ON)}$ of the topside MOSFET (when using the P-channel) and the resistance of the inductor and current sense resistor.

The LTC1266 series combines synchronous switching for maximum efficiency at high currents with an automatic low current operating mode, called Burst Mode operation, which reduces switching losses. Standby power is reduced to only 1mW at V_{IN} = 5V (at I_{OUT} = 0). Load currents in Burst Mode operation are typically 0mA to 500mA.

TYPICAL APPLICATION

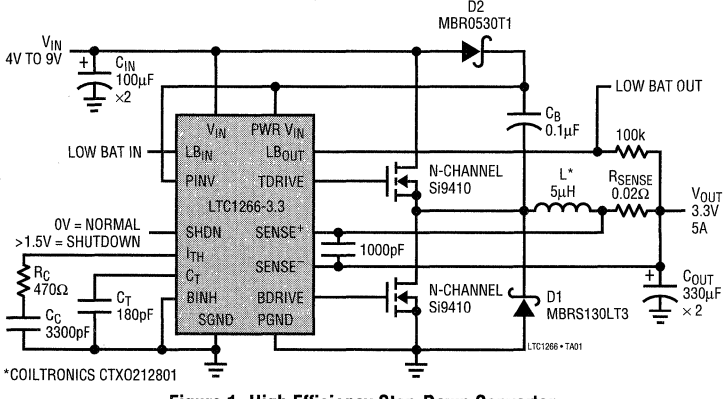
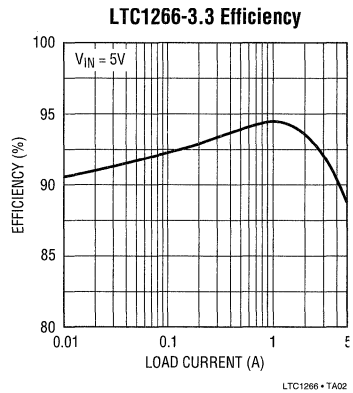


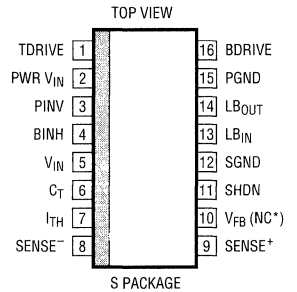
Figure 1. High Efficiency Step-Down Converter



ıBSOLUTE MAXIMUM RATINGS

ıput Supply Voltage (Pins 2, 5) ..... 20V to –0.3V
ontinuous Output Current (Pins 1, 16) 50mA
ense Voltages (Pins 8, 9) ..... 13V to –0.3V
INV, BINH, SHDN, LB_{IN}
(Pins 3, 4, 11, 13) ..... 20V to –0.3V
B_{OUT} Output Current 12mA
perating Ambient Temperature Range ..... 0°C to 70°C
xtended Commercial
Temperature Range ..... –40°C to 85°C
unction Temperature (Note 1) ..... 125°C
torage Temperature Range ..... –65°C to 150°C
ead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

*FIXED OUTPUT VERSIONS

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1266CS
LTC1266CS-3.3
LTC1266CS-5
LTC1266ACS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, V_{SHDN} = V_{BINH} = 0V unless otherwise noted.

YMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FB	Feedback Voltage	V_{IN} = 9V, I_{LOAD} = 700mA, V_{PINV} = V_{PWR},					
	LTC1266ACS	Topside Switch = N-Ch	●		1.275		V
	LTC1266CS		●	1.210	1.25	1.290	V
B	Feedback Current (LTC1266 Only)		●		0.2	1	µA
OUT	Regulated Output Voltage	V_{IN} = 9V, I_{LOAD} = 700mA, V_{PINV} = V_{PWR},					
	LTC1266CS-3.3	Topside Switch = N-Ch, V_{PWR} = 14V	●	3.23	3.33	3.43	V
	LTC1266CS-5		●	4.90	5.05	5.20	V
	Output Ripple (Burst Mode Operation)	I_{LOAD} = 150mA			50		mV_{P-P}
ΔV_{OUT}	Output Voltage Line Regulation	I_{LOAD} = 50mA					
		V_{PINV} = 0V, Topside Switch = P-Ch, V_{IN} = 7V to 12V		–40	0	40	mV
		V_{PINV} = V_{PWR}, Topside Switch = N-Ch, V_{IN} = 7V to 12V		–40	0	40	mV
	Output Voltage Load Regulation	5mA < I_{LOAD} < 2A, R_{SENSE} = 0.05Ω					
	LTC1266-3.3	Burst Mode Operation Enabled, V_{BINH} = 0V	●		40	65	mV
	LTC1266-3.3	Burst Mode Operation Inhibited, V_{BINH} = 2V	●		15	25	mV
	LTC1266-5	Burst Mode Operation Enabled, V_{BINH} = 0V	●		60	100	mV
	LTC1266-5	Burst Mode Operation Inhibited, V_{BINH} = 2V	●		25	40	mV
1	V_{IN} Pin DC Supply Current (Note 2)						
	Normal Mode	3.5V < V_{IN} < 18V			2.1	3.0	mA
	Sleep Mode	3.5V < V_{IN} < 18V			170	250	µA
	Shutdown	V_{SHDN} = 2.1V, 3.5V < V_{IN} < 18V			25	50	µA
2	PWR V_{IN} DC Supply Current (Note 2)						
	Normal Mode	3.5V < PWR V_{IN} < 18V			20	40	µA
	Sleep Mode	3.5V < PWR V_{IN} < 18V			1	5	µA
	Shutdown	V_{SHDN} = 2.1V, 3.5V < PWR V_{IN} < 18V			1	5	µA
SENSE 1	Current Sense Threshold	V_{BINH} = 0V					
	(Burst Mode Operation Enabled)						
	LTC1266	V_{SENSE^-} = 3.3V, V_{FB} = V_{OUT}/2.64 + 25mV (Forced)			25		mV
		V_{SENSE^-} = 3.3V, V_{FB} = V_{OUT}/2.64 – 25mV (Forced)	●	135	155	175	mV
	LTC1266-3.3	V_{SENSE^-} = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE^-} = V_{OUT} – 100mV (Forced)	●	135	155	175	mV
	LTC1266-5	V_{SENSE^-} = V_{OUT} + 100mV (Forced)			25		mV
		V_{SENSE^-} = V_{OUT} – 100mV (Forced)	●	135	155	175	mV

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, V_{SHDN} = V_{BINH} = 0V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
$V_{SENSE\,2}$	Current Sense Threshold (Burst Mode Operation Disabled)	V_{BINH} = 2.1V					
	LTC1266	V_{SENSE^-} = 3.3V, V_{FB} = V_{OUT}/2.64 + 25mV (Forced)			–20		m
		V_{SENSE^-} = 3.3V, V_{FB} = V_{OUT}/2.64 – 25mV (Forced)	●	135	155	175	m
	LTC1266-3.3	V_{SENSE^-} = V_{OUT} + 100mV (Forced)			–20		m
		V_{SENSE^-} = V_{OUT} – 100mV (Forced)	●	135	155	175	m
	LTC1266-5	V_{SENSE^-} = V_{OUT} + 100mV (Forced)			–20		m
		V_{SENSE^-} = V_{OUT} – 100mV (Forced)	●	135	155	175	m
V_{SHDN}	Shutdown Pin Threshold			0.6	0.8	2	
I_{SHDN}	Shutdown Pin Input Current	0V < V_{SHDN} < 8V, V_{IN} = 16V			1.2	5	µ
I_{PINV}	Phase Invert Pin Input Current	0V < V_{PINV} < 18V, V_{IN} = 18V			0.2	1	µ
V_{BINH}	Burst Mode Operation Inhibit Pin Threshold			0.8	1.2	2	
I_{BINH}	Burst Mode Operation Inhibit Pin Input Current	0V < V_{BINH} < 18V, V_{IN} = 18V			0.2	1	µ
I_{CT}	C_T Pin Discharge Current	V_{SENSE^+} = V_{OUT} – 100mV, V_{SENSE^-} = V_{OUT} – 300mV		50	70	90	µ
		V_{OUT} = 0V			2	10	µ
t_{OFF}	Off-Time (Note 3)	C_T = 390pF, I_{LOAD} = 700mA		4	5	6	µ
t_{MAX}	Max On-Time	V_{OUT} = 0V, V_{IN} = 18V			60		µ
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (Pins 1, 16), V_{IN} = 6V			100	200	n
V_{CLAMP}	Output Voltage Clamp in Burst Mode Operation Inhibit	V_{BINH} = 2.1V					
	LTC1266	Measured at V_{FB}			1.30		
	LTC1266-3.3	Measured at V_{SENSE^-}			3.43		
	LTC1266-5	Measured at V_{SENSE^-}			5.20		
V_{LBTRIP}	Low-Battery Trip Point	V_{IN} = 5V		1.14	1.25	1.35	
		V_{IN} = 12V		1.17	1.30	1.42	
I_{LBLEAK}	Max Leakage Current into Pin 14	V_{LBOUT} = 18V, V_{LBIN} = 2V			25	200	n
I_{LBSINK}	Max Sink Current into Pin 14	V_{LBOUT} = 1V, V_{LBIN} = 0V, 2.5V < V_{IN} < 18V		1	8		m
I_{LBIN}	Max Leakage Current into Pin 13	V_{LBIN} = 18V			0.2	1	µ

–40°C < T_A < 85°C (Note 4), V_{IN} = 10V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{FB}	Feedback Voltage (LTC1266 only)	V_{IN} = 9V, I_{LOAD} = 700mA		1.21	1.25	1.29	
V_{OUT}	Regulated Output Voltage	V_{IN} = 9V, I_{LOAD} = 700mA					
	LTC1266-3.3			3.23	3.33	3.43	
	LTC1266-5			4.90	5.05	5.20	
I_{Q1}	V_{IN} Pin DC Supply Current (Note 2)						
	Normal Mode	3.5V < V_{IN} < 18V			2.1	3.3	m
	Sleep Mode	3.5V < V_{IN} < 18V			170	260	µ
	Shutdown	$V_{SHUTDOWN}$ = 2.1V, 3.5V < V_{IN} < 18V			25	60	µ
I_{Q2}	PWR V_{IN} DC Supply Current (Note 2)						
	Normal Mode	3.5V < PWR V_{IN} < 18V			20	50	µ
	Sleep Mode	3.5V < PWR V_{IN} < 18V			1	7	µ
	Shutdown	$V_{SHUTDOWN}$ = 2.1V, 3.5V < PWR V_{IN} < 18V			1	7	µ

ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{SENSE1}	Current Sense Threshold (Burst Mode Operation Enabled)	V_{BINH} = 0V				
	LTC1266	V_{SENSE}^- = 3.3V, $V_{FB} = V_{OUT}/2.64 + 25mV$ (Forced)		25		mV
		V_{SENSE}^- = 3.3V, $V_{FB} = V_{OUT}/2.64 - 25mV$ (Forced)	135	155	180	mV
	LTC1266-3.3, LTC1266-5	V_{SENSE}^- = V_{OUT} + 100mV (Forced)		25		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	135	155	180	mV
Sense 2	Current Sense Threshold (Burst Mode Operation Disabled)	V_{BINH} = 2.1V				
	LTC1266	V_{SENSE}^- 3.3V, $V_{FB} = V_{OUT}/2.64 + 25mV$ (Forced)		–20		mV
		V_{SENSE}^- 3.3V, $V_{FB} = V_{OUT}/2.64 - 25mV$ (Forced)	130	155	185	mV
	LTC1266-3.3, LTC1266-5	V_{SENSE}^- = V_{OUT} + 100mV (Forced)		–20		mV
		V_{SENSE}^- = V_{OUT} – 100mV (Forced)	130	155	185	mV
V_{SHDN}	Shutdown Pin Threshold		0.55	0.8	2	V
OFF	Off-Time (Note 3)	C_T = 390pF, I_{LOAD} = 700mA	3.8	5	6.5	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \times 110°C/W)$

Note 2: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 3: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

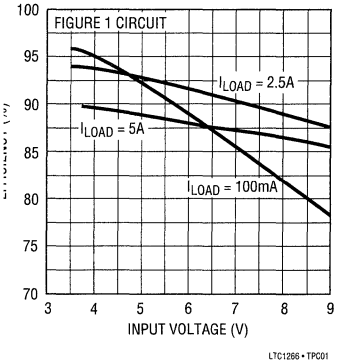
Note 4: The LTC1266, LTC1266-3.3, and LTC1266-5 are not tested and not quality assurance sampled at –40°C and 85°C. These specifications are guaranteed by design and/or correlation.

Note 5: Unless otherwise noted the specifications for the LTC1266A are the same as those for the LTC1266.

4

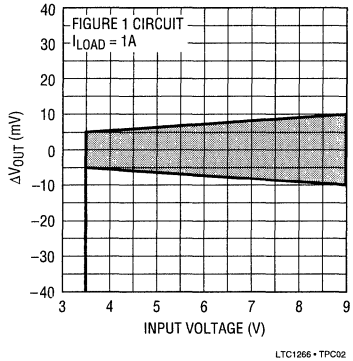
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Input Voltage



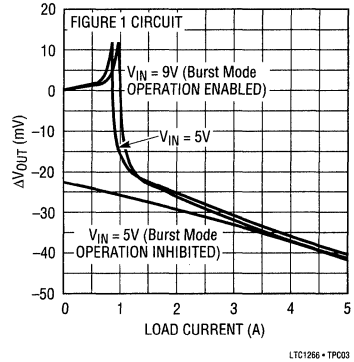
LTC1266 • TPC01

Line Regulation



LTC1266 • TPC02

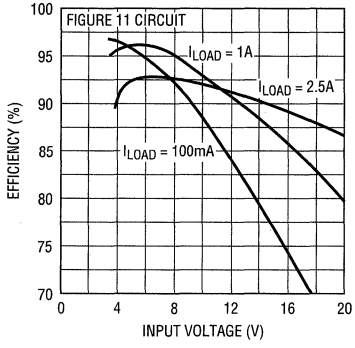
Load Regulation



LTC1266 • TPC03

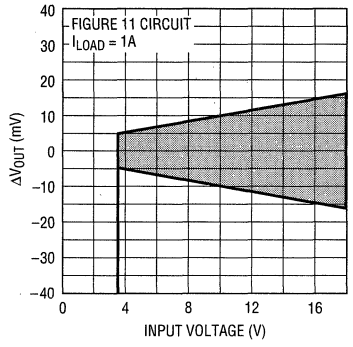
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Input Voltage



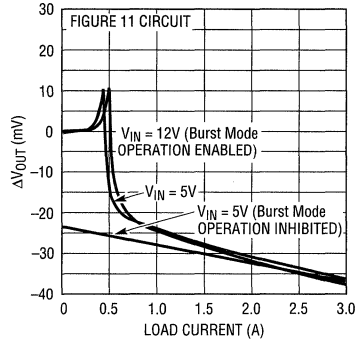
LTC1266 • TPC04

Line Regulation



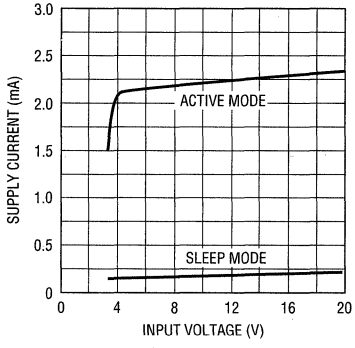
LTC1266 • TPC05

Load Regulation



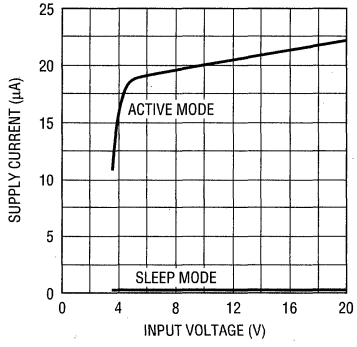
LTC1266 • TPC06

V_{IN} DC Supply Current



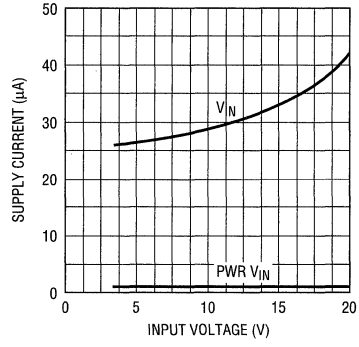
LTC1266 • TPC07

Power V_{IN} DC Supply Current



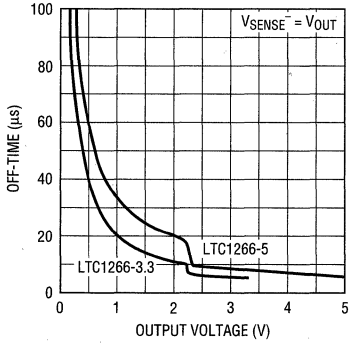
LTC1266 • TPC08

Supply Current in Shutdown



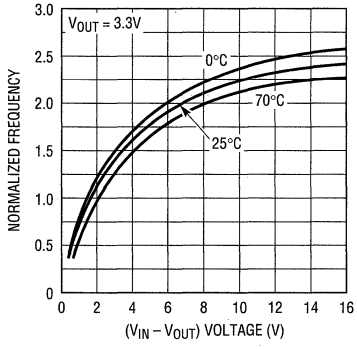
LTC1266 • TPC09

Off-Time vs Output Voltage



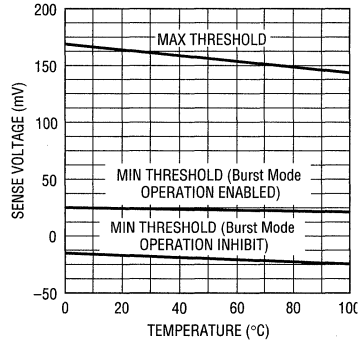
LTC1266 • TPC10

Operating Frequency vs (V_{IN} – V_{OUT}) Voltage



LTC1266 • TPC11

Current Sense Threshold Voltage



LTC1266 • TPC12

PIN FUNCTIONS

TDrive (Pin 1): High Current Drive for Topside MOSFET. This MOSFET can be either P-channel or N-channel, user selectable by Pin 3. Voltage swing at this pin is from PWR V_{IN} to ground.

PWR V_{IN} (Pin 2): Power Suppy for Drive Signals. Must be closely decoupled to power ground (Pin 15).

PINV (Pin 3): Phase Invert. Sets the phase of the topside driver to drive either a P-channel or an N-channel MOSFET as follows:

P-channel: Pin 3 = 0V
N-channel: Pin 3 = PWR V_{IN}

BINH (Pin 4): Burst Mode Operation Inhibit. A CMOS logic high on this pin will disable the Burst Mode operation feature forcing continuous operation down to zero load.

V_{IN} (Pin 5): Main Supply Pin.

C_T (Pin 6): External Capacitor. C_T from Pin 4 to ground sets the operating frequency. The actual frequency is also dependent on the input voltage.

I_{TH} (Pin 7): Gain Amplifier Decoupling Point. The current comparator threshold increases with the Pin 7 voltage.

Sense$^-$ (Pin 8): Connects to internal resistive divider which sets the output voltage in LTC1266-3.3 and LTC1266-5 versions. Pin 8 is also the (–) input for the current comparator.

Sense$^+$ (Pin 9): The (+) Input to the Current Comparator. A built-in offset between Pins 8 and 9 in conjunction with R_{SENSE} sets the current trip threshold.

V_{FB} (Pin 10): For the LTC1266 adjustable version, Pin 10 serves as the feedback pin from an external resistive divider used to set the output voltage. On LTC1266-3.3 and LTC1266-5 versions this pin is not used.

SHDN (Pin 11): When grounded, the LTC1266 series operates normally. Pulling Pin 11 high holds both MOSFETs off and puts the LTC1266 in micropower shutdown mode. Requires CMOS logic signal with t_r, $t_f < 1\mu s$. Should not be left floating.

SGND (Pin 12): Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

LB_{IN} (Pin 13): Input to the Low-Battery Comparator. This input is compared to an internal 1.25V reference.

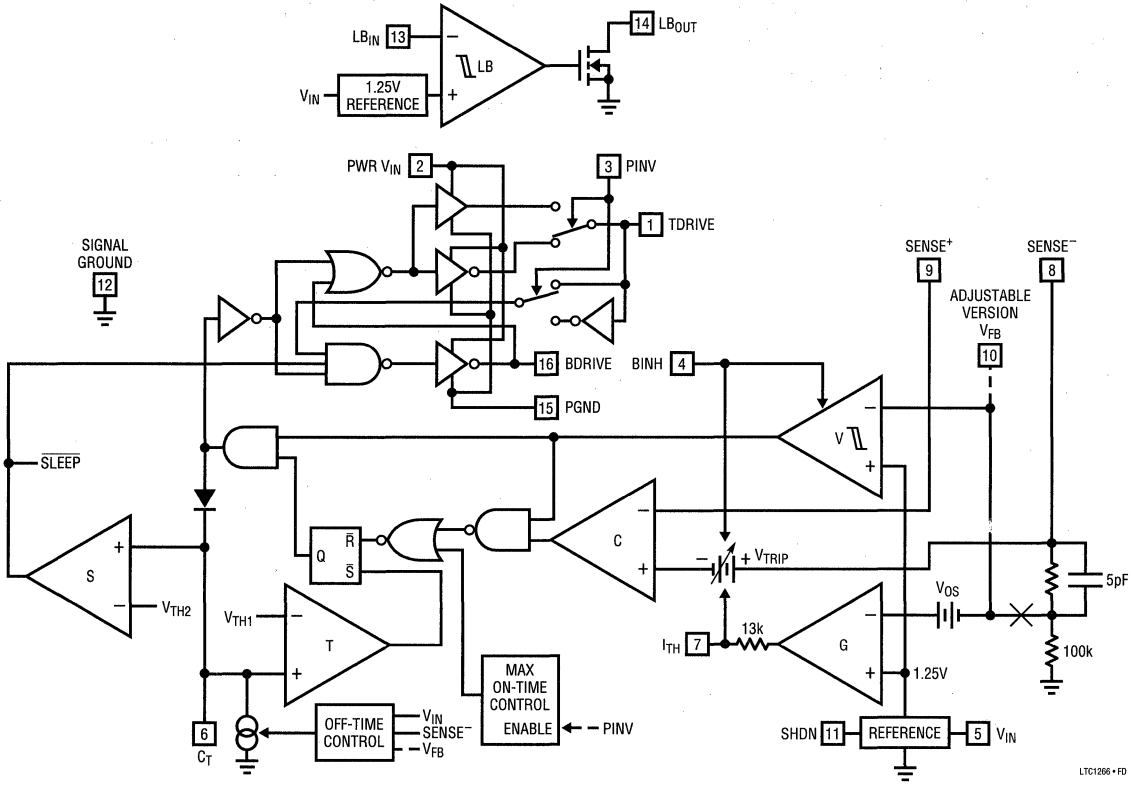
LB_{OUT} (Pin 14): Open Drain Output of the Low-Battery Comparator. This pin will sink current when Pin 13 is below 1.25V.

PGND (Pin 15): Driver Power Ground. Connects to source of N-channel MOSFET and the (–) terminal of C_{IN}.

BDrive (Pin 16): High Current Drive for Bottom N-Channel MOSFET. Voltage swing at Pin 16 is from ground to PWR V_{IN}.

FUNCTIONAL DIAGRAM

Pin 10 Connection Shown for LTC1266-3.3 and LTC1266-5; Changes Create LTC1266



OPERATION

The LTC1266 series uses a current mode, constant off-time architecture to synchronously switch an external pair of power MOSFETs. Operating frequency is set by an external capacitor at the timing capacitor Pin 6.

The output voltage is sensed by an internal voltage divider connected to Sense$^-$, Pin 8, (LTC1266-3.3 and LTC1266-5) or external divider returned to V_{FB}, Pin 10, (LTC1266). A voltage comparator V, and a gain block G, compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1266 automatically switches between two modes of operation, burst and continuous. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

During the switch ON cycle in continuous mode, current comparator C monitors the voltage between Pins 8 and 9 connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the topside driver output is switched to turn off the topside MOFSET (Power V_{IN} for P-channel or ground for N-channel). The timing capacitor connected to Pin 6 is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage (measured by Pin 8) to model the inductor current, which decays at a rate which is also proportional to the output voltage. While the timing capacitor is discharging, the bottom-side drive output is switched to power V_{IN} to turn on the bottom-side N-channel MOSFET.

OPERATION

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the bottom-side output to switch off and the topside output to switch on (ground for P-channel and Power V_{IN} for N-channel). The cycle then repeats.

As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage (Pin 7) to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the topside MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal sleep line to go low and the bottom-side MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode, a majority of the circuitry is turned off, dropping the quiescent current from 2.1mA to 170μA. The load current is now being supplied from the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the topside MOSFET is again turned on and this process repeats.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset V_{OS} is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

To prevent both the external MOSFETs from ever being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the bottom-side drive output can turn on, the topside output must be off. Likewise, the topside output is prevented from turning on while the bottom-side drive output is still on.

The LTC1266 has two select pins which provide the user with choice of topside switch and with the option of inhibiting Burst Mode operation. The phase select pin allows the user to choose whether the topside MOSFET is a P-channel or an N-channel. The phase select pin does two things: sets the proper phase of the drive signal (ON = Power V_{IN} for N-channel and ON = 0V for P-channel) and also sets an upper limit for the on-time (60μs) when set to the N-channel. The on-time limit ensures proper start-up when used in a single supply bootstrap circuit configuration (see Applications Information). In P-channel mode there is no on-time limit and thus, in dropout, the P-channel MOSFET is turned on continuously (100% duty cycle).

The Burst Mode operation inhibit (BINH, Pin 4) allows the Burst Mode operation to be disabled by applying a CMOS logic high to this pin. With Burst Mode operation disabled, the LTC1266 will remain in continuous mode down to zero load. Burst Mode operation is disabled by allowing the lower current threshold limit to go below zero so that the voltage comparator will never trip. The voltage comparator trip point is also raised up so that it will not be tripped by transients. It is still active to provide a voltage clamp to prevent the output from overshooting.

APPLICATIONS INFORMATION

One of the three basic LTC1266 application circuits is shown in Figure 1. This circuit uses an N-channel topside driver and a single supply. The other two circuit configurations (see Typical Applications) use an N-channel topside driver and dual supply, and a P-channel topside driver. Selections of other external components are driven by the load requirement and are the same for all three circuit configurations. The first step is the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. Using an N-channel topside switch, input voltages are limited to a maximum of about 15V. With a P-channel, the input voltage may be as high as 20V.

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R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1266 series current comparator has a threshold range which extends from a minimum of 25mV/R_{SENSE} (when Burst Mode operation is enabled) to a maximum of 155mV/R_{SENSE}. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)}$ = 25mV/R_{SENSE} (see C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1266 series and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

A graph for selecting R_{SENSE} vs maximum output current is given in Figure 2.

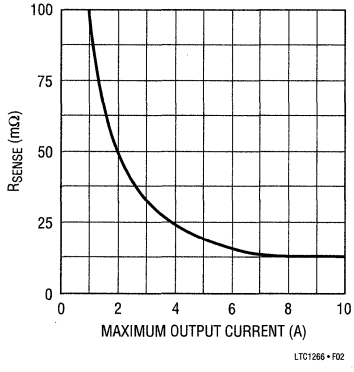

Figure 2. Selecting R_{SENSE}

The load current, below which Burst Mode operation commences, (I_{BURST}), and the peak short circuit current, ($I_{SC(PK)}$), both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{155mV}{R_{SENSE}}$$

The LTC1266 series automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

L and C_T Selection for Operating Frequency

The LTC1266 series uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. Each time the topside MOSFET switch turns on, the voltage on C_T is reset to approximately 3.3V. During the off-time, C_T is discharged by a current which is proportional to V_{OUT}. The voltage on C_T is analogous to the current in inductor L, which likewise decays at a rate proportional to V_{OUT}. Thus the inductor value must track the timing capacitor value.

The value of C_T is calculated from the desired continuous mode operating frequency, f:

$$C_T = \frac{1}{2.6 \times 10^4 \times f}$$

assumes $V_{IN} = 2V_{OUT}$, (Figure 1 circuit).

A graph for selecting C_T vs frequency including the effects of input voltage is given in Figure 3.

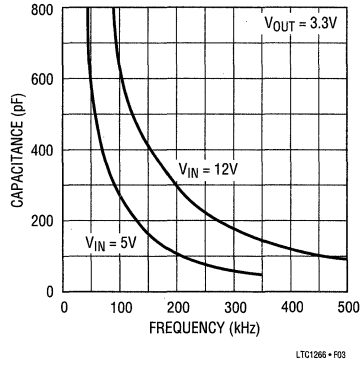

Figure 3. Timing Capacitor Value

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As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency of the circuit in Figure 1 is given by:

$$f = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3 \times 10^4 \times C_T \times \left(\frac{V_{REG}}{V_{OUT}}\right)$$

V_{REG} is the desired output voltage (i.e., 5V, 3.3V). V_{OUT} is the measured output voltage. Thus $V_{REG}/V_{OUT} = 1$ in regulation.

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than $25mV/R_{SENSE}$ of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{REG}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the inductor current will decrease past zero and change polarity. A consequence of this is that the LTC1266 series may not enter Burst Mode operation and efficiency will be slightly degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. The highest efficiency will be obtained using ferrite, Kool Mμ® on molypermalloy (MPP) cores. Lower cost powdered iron cores provide suitable performance but cut efficiency by 3% to 7%. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses increase.

Ferrite designs have very low core loss, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple which can cause Burst Mode operation to be falsely triggered. Do not allow the core to saturate!

Kool Mμ is a very good, low loss core material for toroids, with a "soft" saturation characteristic. Molypermalloy is slightly more efficient at high (>200kHz) switching frequency. Toroids are very space efficient, especially when you can use several layers of wire. Because they generally lack a bobbin, mounting is more difficult. However, new designs for surface mount are available from Coiltronics and Beckman Industrial Corp. which do not increase the height significantly.

Power MOSFET and D1 Selection

Two external power MOSFETs must be selected for use with the LTC1266 series: either a P-channel MOSFET or an N-channel MOSFET for the main switch and an N-channel MOSFET for the synchronous switch. The main selection criteria for the power MOSFETs are the type of MOSFET, threshold voltage $V_{GS(TH)}$ and on-resistance $R_{DS(ON)}$.

The cost and maximum output current determine the type of MOSFET for the topside switch. N-channel MOSFETs have the advantage of lower cost and lower $R_{DS(ON)}$ at the expense of slightly increased circuit complexity. For lower current applications where the losses due to $R_{DS(ON)}$ are small, a P-channel MOSFET is recommended due to the lower circuit complexity. However, at load currents in excess of 3A where the $R_{DS(ON)}$ becomes a significant portion of the total power loss, an N-channel is strongly recommended to maximize efficiency.

The maximum output current I_{MAX} determines the $R_{DS(ON)}$ requirement for the two MOSFETs. When the LTC1266 series is operating in continuous mode, the simplifying assumption can be made that one of the two MOSFETs is always conducting the average load current. The duty cycles for the two MOSFETs are given by:

$$\text{TopSide Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Bottom-Side Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

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From the duty cycles, the required $R_{DS(ON)}$ for each MOSFET can be derived:

$$\text{TS } R_{DS(ON)} = \frac{V_{IN} \times P_T}{V_{OUT} \times I_{MAX}^2 \times (1 + \delta_T)}$$

$$\text{BS } R_{DS(ON)} = \frac{V_{IN} \times P_B}{(V_{IN} - V_{OUT}) \times I_{MAX}^2 \times (1 + \delta_B)}$$

where P_T and P_B are the allowable power dissipations and δ_T and δ_B are the temperature dependencies of $R_{DS(ON)}$. P_T and P_B will be determined by efficiency and/or thermal requirements (see Efficiency Considerations). For a MOSFET, $(1 + \delta)$ is generally given in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta_{PCH} = 0.007/°C$ and $\delta_{NCH} = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

The minimum input voltage determines whether standard threshold or logic-level threshold MOSFETs must be used. For $V_{IN} > 8V$, standard threshold MOSFETs ($V_{GS(TH)} < 4V$) may be used. If V_{IN} is expected to drop below 8V, logic-level threshold MOSFETs ($V_{GS(TH)} < 2.5V$) are strongly recommended. The LTC1266 series Power V_{IN} must always be less than the absolute maximum V_{GS} ratings for the MOSFETs.

The Schottky diode D1 shown in Figure 1 only conducts during the deadtime between the conduction of the two power MOSFETs. D1's sole purpose in life is to prevent the body diode of the bottom-side MOSFET from turning on and storing charge during the deadtime, which could cost as much as 1% in efficiency (although there are no other harmful effects if D1 is omitted). Therefore, D1 should be selected for a forward voltage of less than 0.7V when conducting I_{MAX}.

C_{IN} and C_{OUT} Selection

In continuous mode, the current through the topside MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR (Effective Series Resistance) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question. An additional 0.1µF to 1µF ceramic capacitor is also required on Power V_{IN} (Pin 2) for high frequency decoupling.

The selection of C_{OUT} is driven by the required ESR. *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1266 series:*

$$C_{OUT} \text{ Required ESR} < 2R_{SENSE}$$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent. If Burst Mode operation is disabled, the ESR requirement can be relaxed and is limited only by the allowable output voltage ripple.

Manufacturers such as Nichicon and United Chemicon should be considered for high performance capacitors. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR/size ratio of any aluminum electrolytic at a somewhat higher price. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement.

In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirements of the application. An excellent choice is the AVX TPS series of surface mount tantalums.

At low supply voltages, a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip the voltage comparator. This causes Burst Mode operation to be activated when the LTC1266

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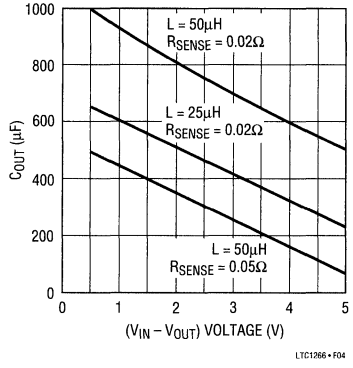

Figure 4. Minimum Value of C_{OUT}

series would normally be in continuous operation. The output remains in regulation at all times. This minimum capacitance requirement may be relaxed if Burst Mode operation is disabled.

N-Channel vs P-Channel MOSFETs

The LTC1266 has the capability to drive either an N-channel or a P-channel topside switch to give the user more flexibility. N-channel MOSFETs are superior in performance to P-channel due to their lower $R_{DS(ON)}$ and lower gate capacitance and are typically less expensive; however, they do have a slightly more complicated gate drive requirement and a more limited input voltage range (see following sections).

Driving P-Channel Topside MOSFETs

The P-channel topside switch circuit configuration is the most straightforward due to the requirement of only one supply voltage level. This is due to the negative gate threshold of the P-channel MOSFET which allows the MOSFET to be switched on and off by swinging the gate between V_{IN} and ground. The phase invert (Pin 3) is tied to ground to choose this operating mode. Normally, the converter input (V_{IN}) is connected to the LTC1266 supply Pins 2 and 5 and can go as high as 20V. Pin 2 supplies the high frequency current pulses to switch the MOSFETs and should be decoupled with a 0.1µF to 1µF ceramic capacitor. Pin 5 supplies most of the quiescent power to the rest of the chip.

Driving N-Channel Topside MOSFETs

Driving an N-channel topside MOSFET (PINV, Pin 3, tied to PWR V_{IN}) is a little trickier than driving a P-channel since the gate voltage must be positive with respect to the source to turn it on, which means that the gate voltage must be higher than V_{IN}. This requires either a second supply at least $V_{GS(ON)}$ above V_{IN} or a bootstrapping circuit to boost the V_{IN} to the proper level. The easiest method is using a higher supply (see Figure 14) but if one is not available, the bootstrap method can be used at the expense of an additional diode (see Figure 1). The bootstrap works by charging the bootstrap capacitor to V_{IN} during the off-time. During the on-time, the bottom plate of the capacitor is pulled up to V_{IN} so that the voltage at Pin 2 is now twice V_{IN} (plus any ringing on the switch node).

Since the maximum allowable voltage at Pin 2 is 20V, the Figure 1 bootstrap circuit limits V_{IN} to less than 10V. A higher V_{IN} can be achieved if the bootstrap capacitor is charged to a voltage less than V_{IN}, in which case $V_{IN(MAX)} = 20 - V_{CAP}$.

N-channel mode, internal circuitry limits the maximum on-time to 60µs to guarantee start-up of the bootstrap circuit. This maximum on-time reduces the maximum duty cycle to:

$$\text{Max Duty Cycle} = \frac{60\mu s}{60\mu s + t_{OFF}}$$

which slightly increases the minimum input voltage at which dropout occurs. However, because of the superior on-conductance of the N-channel, the dropout performance of an all N-channel regulator is still better (see Figure 5) even with the duty cycle limitation, except at light loads.

Low-Battery Comparator

The LTC1266 has an on-chip low-battery comparator which can be used to sense a low-battery condition when implemented as shown in Figure 6. The resistor divider R1, R2 sets the comparator trip point as follows:

$$V_{TRIP} = 1.25\left(1 + \frac{R2}{R1}\right)$$

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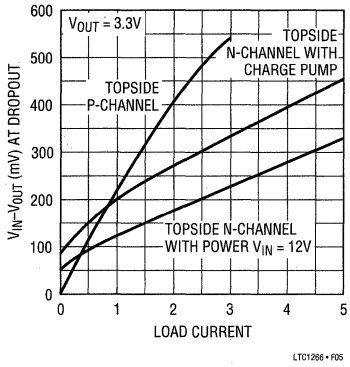

Figure 5. Comparison of Dropout Performance

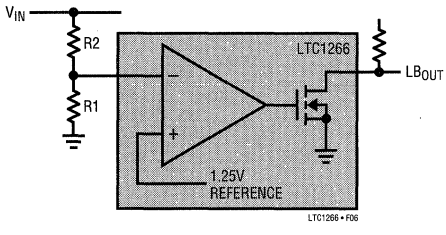

Figure 6. Low-Battery Comparator

The divided down voltage at the "–" input to the comparator is compared to an internal 1.25V reference. This reference is separate from the 1.25V reference used by the voltage comparator and current comparator for regulation and is not disabled by the shutdown pin, therefore the low-battery detection is operational even when the rest of the chip is shut down. The comparator is functional down to an input voltage of 2.5V. Thus, the output will provide a valid state even when the rest of the chip does not have sufficient voltage to operate. For best performance, the value of the pull-up resistor should be high enough that the output is pulled down to ground when sinking 200µA or less.

Suppressing Burst Mode Operation

Normally, enabling Burst Mode operation is desired due to its superior efficiency at low load currents (see Figure 7).

However, in certain applications it may be desirable to inhibit this feature. Some reasons for doing so are:

1. To eliminate audible noise from certain types of inductors at light loads.

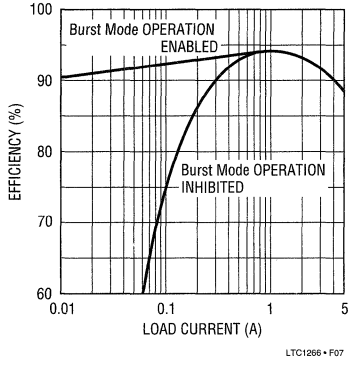

Figure 7. Effect of Disabling Burst Mode Operation on Efficiency

2. If the load is never expected to drop low enough to benefit from the efficiency advantages of Burst Mode operation, the output capacitor ESR and minimum capacitance requirements (which may falsely trigger Burst Mode operation if not met) can be relaxed if Burst Mode operation is disabled.
3. If an auxiliary winding is used. Disabling Burst Mode operation guarantees switching independent of the load on the primary. This allows power to be taken from the auxiliary winding independently.
4. Tighter load regulation (< 1%).

Burst Mode operation is disabled by applying a CMOS logic high voltage (>2.1V) to Pin 4. When it is disabled, the voltage comparator limit is raised high enough so that it no longer is involved in regulation; however it is still active and is useful as a voltage clamp to keep the output from overshooting.

Note that since the inductor current must reverse to regulate the output at zero load when Burst Mode operation is disabled, the minimum inductance (L_{MIN}) specified during Inductor Core Selection is no longer applicable.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or

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discharge C_{OUT} until the regulator loop adapts to the current change and returns V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing which would indicate a stability problem. The Pin 7 external components shown in the Figure 1 circuit will prove adequate compensation for most applications.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits, only small errors are incurred by expressing losses as a percentage of output power).

Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC1266 series circuits: 1) LTC1266 DC bias current, 2) MOSFET gate charge current and 3) I^2R losses.

1. The DC supply current is the current which flows into V_{IN} (Pin 2). For V_{IN} = 10V the LTC1266 DC supply current is 170μA for no load, and increases proportionally with load up to a constant 2.1mA after the LTC1266 series has entered continuous mode. Because the DC bias current is drawn from V_{IN}, the resulting loss increases with input voltage. For V_{IN} = 5V the DC bias losses are generally less than 1% for load currents over 30mA. However, at very low load currents the DC bias current accounts for nearly all of the loss.

2. MOSFET gate charge current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from Power V_{IN} to ground. The resulting dQ/dt is a current flowing into Power V_{IN} (Pin 5) which is typically much larger than the DC supply current. In continuous mode, $I_{GATECHG} = f(Q_N + Q_P)$. The typical gate charge for a 0.05Ω N-channel power MOSFET is 15nC. This results in $I_{GATECHG}$ = 6mA in 200kHz continuous operation for a 2% to 3% typical mid-current loss with V_{IN} = 5V.

   Note that the gate charge loss increases directly with both input voltage and operating frequency. This is the principal reason why the highest efficiency circuits operate at moderate frequencies. Furthermore, it argues against using larger MOSFETs than necessary to control I^2R losses, since overkill can cost efficiency as well as money!

3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor and current shunt. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside and bottom-side MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 0.05Ω, R_L = 0.05Ω and R_{SENSE} = 0.02Ω, then the total resistance is 0.12Ω. This results in losses ranging from 3.5% to 15% as the output current increases from 1A to 5A. I^2R losses cause the efficiency to roll off at high output currents.

Figure 8 shows how the efficiency losses in a typical LTC1266 series regulator end up being apportioned. The gate charge loss is responsible for the majority of the efficiency lost in the mid-current region. If Burst Mode operation was not employed at low currents, the gate charge loss alone would cause efficiency to drop to

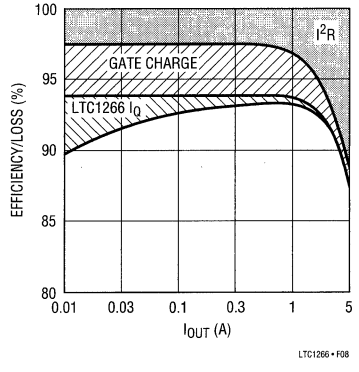

Figure 8. Efficiency Loss

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unacceptable levels (see Figure 7). With Burst Mode operation, the DC supply current represents the lone (and unavoidable) loss component which continues to become a higher percentage as output current is reduced. As expected the I^2R losses dominate at high load currents.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, MOSFET switching losses, Schottky conduction losses during deadtime and inductor core losses, generally account for less than 2% total additional loss.

Design Example

As a design example, assume V_{IN} = 5V (nominal), V_{OUT} = 3.3V, I_{MAX} = 5A and f = 200kHz; R_{SENSE}, C_T and L can immediately be calculated:

$R_{SENSE} = 100mV/5 = 0.02\Omega$

$t_{OFF} = (1/200kHz) \times [1 - (3.3/5)] = 1.7\mu s$

$C_T = 1.7\mu s/(1.3 \times 10^4) = 130pF$

$L_{MIN} = 5.1 \times 10^5 \times 0.02\Omega \times 130pF \times 3.3V = 5\mu H$

Assume that the MOSFET dissipations are to be limited to $P_T = P_B = 2W$.

If T_A = 40°C and the thermal resistance of each MOSFET is 50°C/W, then the junction temperatures will be 140°C and $\delta_T = \delta_B = 0.60$. The required $R_{DS(ON)}$ for each MOSFET can now be calculated:

$$TS\ R_{DS(ON)} = \frac{5(2)}{3.3(5)^2\ (1.60)} = 0.076\Omega$$

$$BS\ R_{DS(ON)} = \frac{5(2)}{1.7(5)^2\ (1.60)} = 0.147\Omega$$

The topside FET requirement can be met by an N-channel Si9410DY which has an $R_{DS(ON)}$ of about 0.04Ω at V_{GS} = 5V. The bottom-side FET requirement is exceeded by an Si9410DY. Note that the most stringent requirement for the bottom-side MOSFET is with V_{OUT} = 0 (i.e., short circuit). During a continuous short circuit, the worst-case dissipation rises to:

$$P_B = I_{SC(AVG)}{}^2 \times R_{DS(ON)} \times (1 + \delta_B)$$

With the 0.02Ω sense resistor, $I_{SC(AVG)} \approx 6A$ will result, increasing the 0.04Ω bottom-side FET dissipation to 2.3W. C_{IN} will require an RMS current rating of at least 2.5A at temperature and C_{OUT} will require an ESR of 0.02Ω for optimum efficiency.

Now allow V_{IN} to drop to its minimum value. The minimum V_{IN} can be calculated from the maximum duty cycle and voltage drop across the topside FET,

$$V_{MIN} = \frac{V_{OUT} + I_{LOAD} \times (R_{DS(ON)} + R_L + R_{SENSE})}{D_{MAX}} = 4.0V$$

At this lower input voltage, the operating frequency decreases and the topside FET will be conducting most of the time, causing the power dissipation to increase. At dropout,

$$f_{MIN} = \frac{1}{t_{ON\ (MAX)} + t_{OFF}} = 16kHz$$

$$P_T = I^2_{LOAD} \times R_{DS(ON)} \times (1 + \delta_T) \times D_{MAX}$$

This last step is necessary to assure that the power dissipation and junction temperature of the topside FET are not exceeded.

These last calculations assume that Power V_{IN} is high enough to keep the topside FET fully turned on at dropout, as would be the case with the Figure 11circuit. If this isn't true (as with the Figure 1 circuit) the $R_{DS(ON)}$ will increase which in turn increases V_{MIN} and P_T.

Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1266 adjustable version is used with an external resistive divider from V_{OUT} to V_{FB}, Pin 10. The regulated voltage is determined by:

$$V_{OUT} = 1.25\left(1 + \frac{R2}{R1}\right)$$

To prevent stray pickup a 100pF capacitor is suggested across R1 located close to the LTC1266.

For Figure 1 applications with V_{OUT} below 2V, or when R_{SENSE} is moved to ground, the current sense comparator inputs operate near ground. When the current comparator is operated at less than 2V common mode, the off-time increases approximately 40%, requiring the use of a smaller timing capacitor C_T.

APPLICATIONS INFORMATION

Troubleshooting Hints

Since efficiency is critical to LTC1266 series applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the timing capacitor, Pin 6.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation should occur with the C_T pin waveform periodically falling to ground for periods of time as shown in Figure 9b.

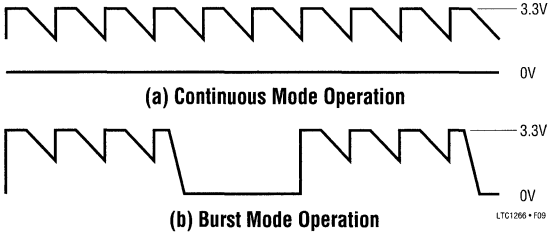


Figure 9. C_T Waveforms

If Pin 6 is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1266 series. These items are also illustrated graphically in the layout diagram of Figure 10. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1266 signal ground (Pin 12) must return to the (–) plate of C_{OUT}. The power ground returns to the source of the bottom-side MOSFET, anode of the Schottky diode and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2. Does the LTC1266 Sense$^-$ (Pin 8) connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications, the resistive divider R1 and R2 must be connected between the (+) plate of C_{OUT} and signal ground.

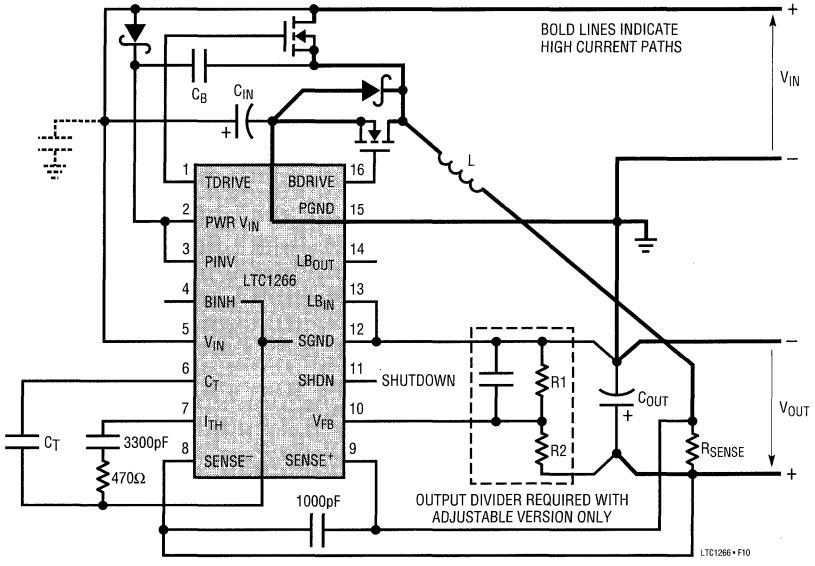


Figure 10. LTC1266 Layout Diagram (See Layout Checklist)

APPLICATIONS INFORMATION

3. Are the Sense$^-$ and Sense$^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between Pins 8 and 9 should be as close as possible to the LTC1266.
4. Does the (+) plate of C_{IN} connect to the source of the topside MOSFET as closely as possible? This capacitor provides the AC current to the topside MOSFET.
5. A 0.1µF to 1µF decoupling capacitor connected between V_{IN} (Pin 5) and ground is optional, but is sometimes helpful in eliminating instabilities at high input voltage and high output loads.
6. Is the Shutdown (Pin 11) actively pulled to ground during normal operation? The Shutdown pin is high impedance and must not be allowed to float. The Select (Pins 3 and 4) are also high impedance and must be tied high or low depending on the application.

TYPICAL APPLICATIONS (Layout Assist Schematics)

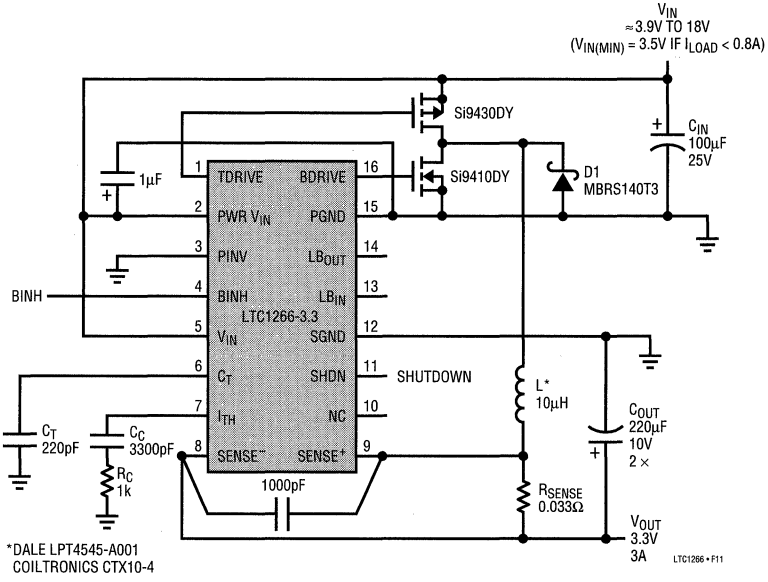


Figure 11. Low Dropout, 3.3V/3A High Efficiency Regulator

TYPICAL APPLICATIONS (Layout Assist Schematics)

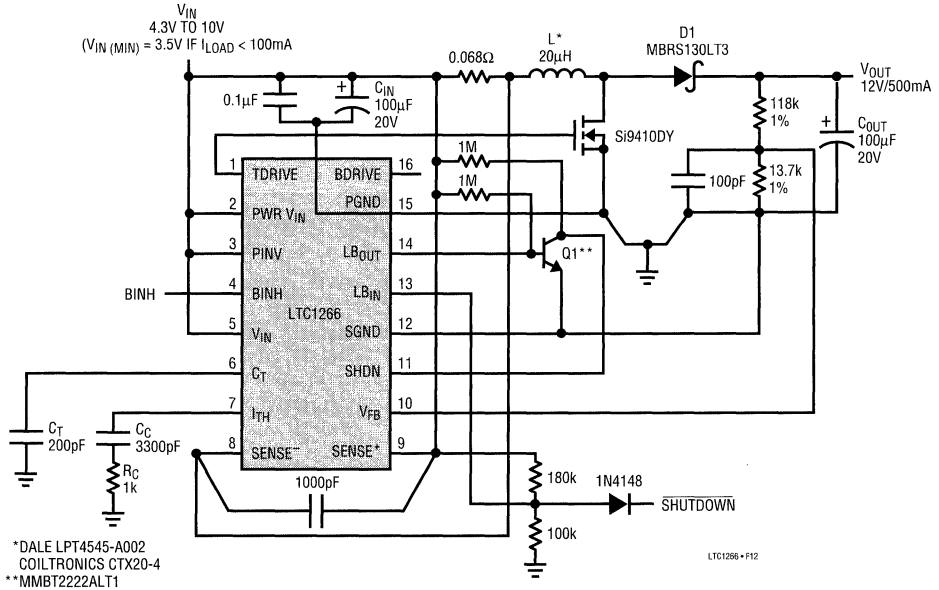


Figure 12. 5V to 12V/500mA High Efficiency Boost Regulator

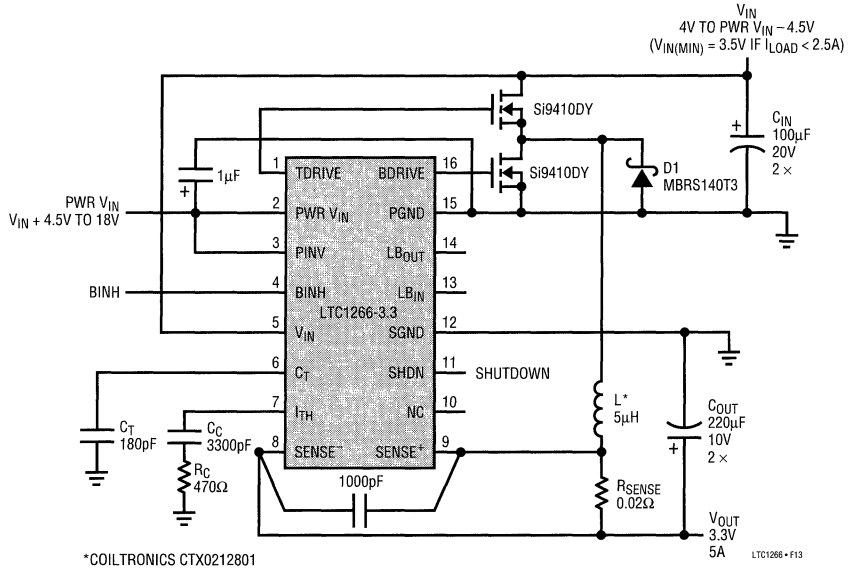


Figure 13. All N-Channel 5V to 3.3V/5A Converter with Drivers Powered from External PWR V_{IN} Supply

TYPICAL APPLICATIONS (Layout Assist Schematics)

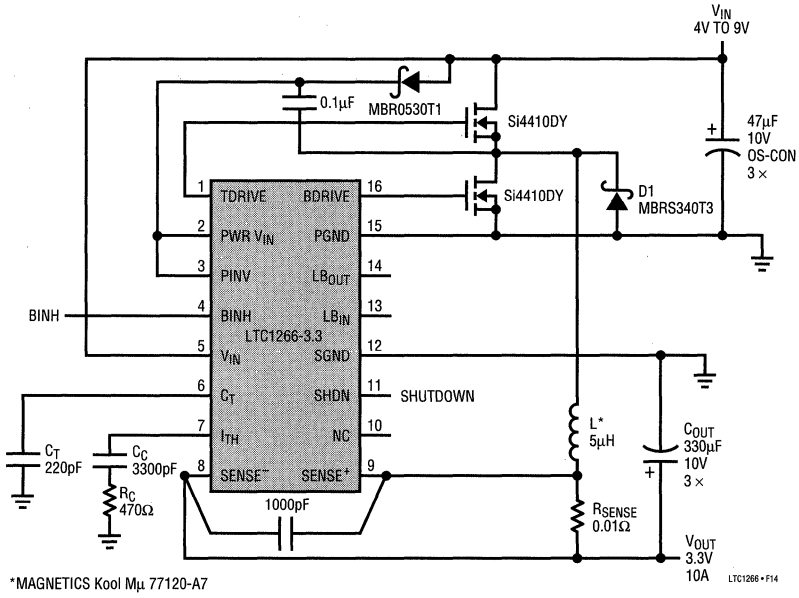


Figure 14. All N-Channel 5V to 3.3V/10A High Efficiency Regulator

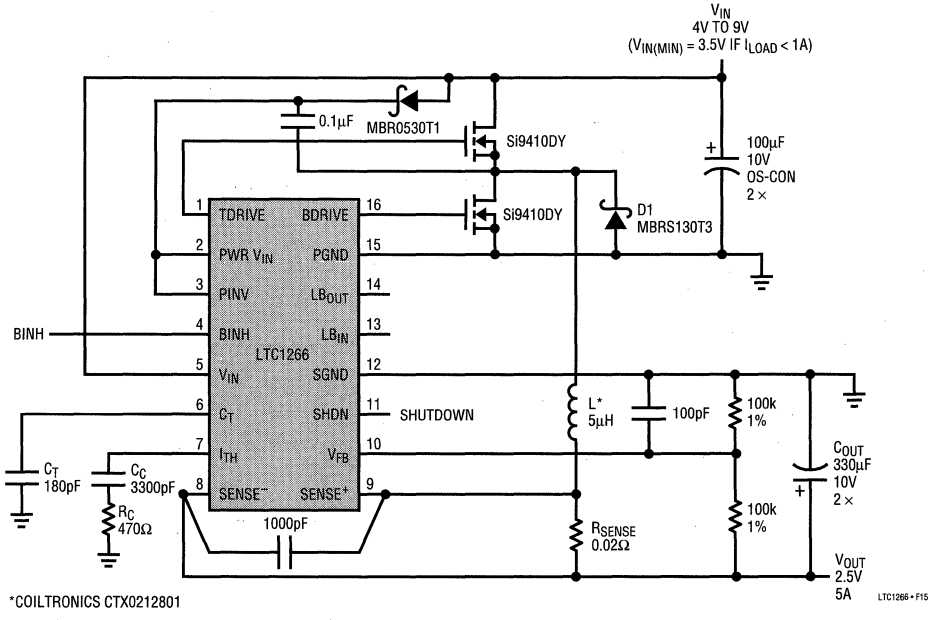


Figure 15. All N-Channel 5V to 2.5V/5A High Efficiency Regulator

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142	Dual High Efficiency Synchronous Step-Down Switching Regulator	Dual Version of LTC1148
LTC1143	Dual High Efficiency Step-Down Switching Regulator Controller	Dual Version of LTC1147
LTC1147	High Efficiency Step-Down Switching Regulator Controller	Nonsynchronous, 8-Lead, $V_{IN} \leq 16V$
LTC1148	High Efficiency Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 20V$
LTC1149	High Efficiency Step-Down Switching Regulator	Synchronous, $V_{IN} \leq 48V$, for Standard Threshold FETs
LTC1159	High Efficiency Synchronous Step-Down Switching Regulator	$V_{IN} \leq 40V$, for Logic Level FETs
LTC1174	High Efficiency Step-Down and Inverting DC/DC Converter	0.5A Switch, $V_{IN} \leq 18.5V$, Comparator
LTC1265	High Efficiency Step-Down DC/DC Converter	1.2A Switch, $V_{IN} \leq 13V$, Comparator
LTC1267	Dual High Efficiency Synchronous Step-Down Switching Regulators	Dual Version of LTC1159

Dual High Efficiency Synchronous Step-Down Switching Regulators

FEATURES

- **Dual Outputs: 3.3V and 5V, Two Adjustables or Adjustable and 5V**
- **Wide V_{IN} Range: 4V to 40V**
- **Ultra-High Efficiency: Up to 95%**
- **Low Supply Current in Shutdown: 20μA**
- Current Mode Operation for Excellent Line and Load Transient Response
- High Efficiency Maintained Over a Wide Output Current Range
- Independent Micropower Shutdown
- Very Low Dropout Operation: 100% Duty Cycle
- Synchronous FET Switching for High Efficiency
- Available in Standard 28-Pin SSOP

APPLICATIONS

- Notebook and Palmtop Computers
- Battery-Operated Digital Devices
- Portable Instruments
- DC Power Distribution Systems

DESCRIPTION

The LTC®1267 series are dual synchronous step-down switching regulator controllers featuring automatic Burst Mode™ operation to maintain high efficiencies at low output currents. The LTC1267 is composed of two separate regulator blocks, each driving a pair of external complementary power MOSFETs at switching frequencies up to 400kHz. The LTC1267 uses a constant off-time current-mode architecture to provide constant ripple current in the inductor and provide excellent line and load transient response.

A separate pin and on-board switch allow the MOSFET driver power to be derived from the regulated output voltage, providing significant efficiency improvement when operating at high input voltage. The output current level is user-programmable via an external current sense resistor.

The LTC1267 series is ideal for applications requiring dual output voltages with high conversion efficiencies over a wide load current range in a small amount of board space.

TYPICAL APPLICATION

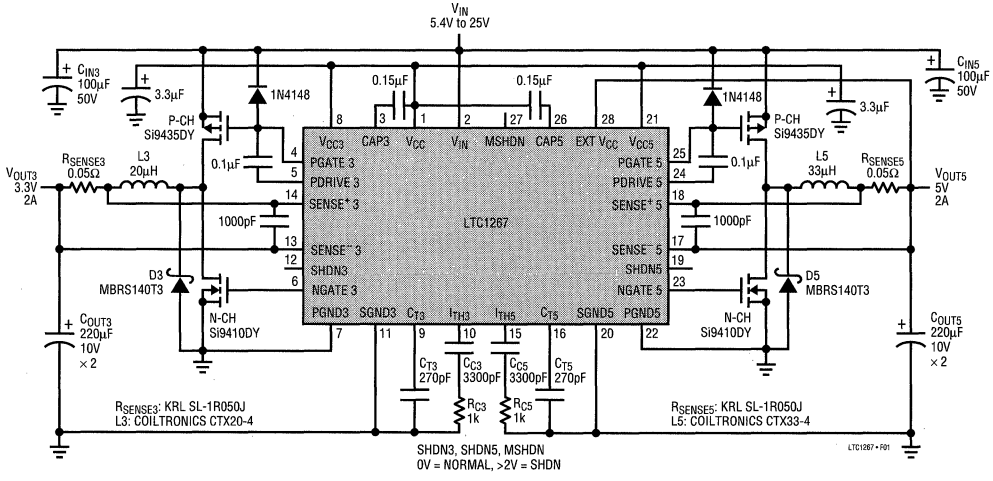
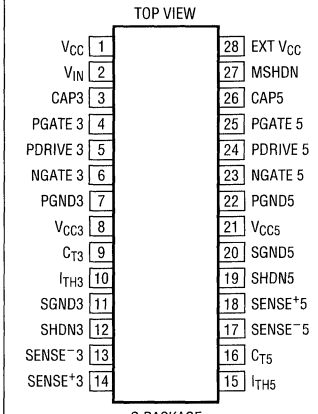


Figure 1. High Efficiency Dual 3.3V, 5V

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage (Pin 2) ..... –0.3V to 40V
V_{CC} Output Current (Pin 1) 50mA
EXT V_{CC} Input Voltage (Pin 28) 10V
Continuous Output Current (Pins 5, 6, 23, 24) 50mA
Sense Voltages
  LTC1267 (Pins 13, 14, 17, 18) ..... V_{CC} to –0.3V
  LTC1267-ADJ (Pins 12, 13, 17, 18) ..... V_{CC} to –0.3V
  LTC1267-ADJ5 (Pins 12, 13, 17, 18) ... V_{CC} to –0.3V
Shutdown Voltages
  LTC1267 (Pins 12, 19, 27) 7V
  LTC1267-ADJ (Pins 11, 27) 7V
  LTC1267-ADJ5 (Pins 11, 19, 27) 7V
Operating Ambient Temperature Range ..... 0°C to 70°C
Extended Commercial
  Temperature Range ..... –40°C to 85°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

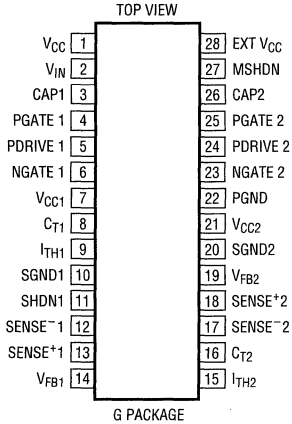
PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

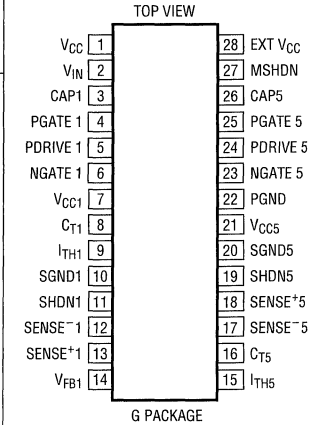
ORDER PART NUMBER
LTC1267CG



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC1267CG-ADJ



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC1267CG-ADJ5

Consult factory for Industrial and Military grade parts.
The LTC1267 demo circuit board is now available. Consult factory.

4

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 12V, V_{MSHDN}, $V_{SHDN1,3,5}$ = 0V (Note 2), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{FB1,2}$	Feedback Voltage	LTC1267-ADJ, LTC1267-ADJ5: V_{IN} = 9V	●	1.21	1.25	1.29	V
$I_{FB1,2}$	Feedback Current	LTC1267-ADJ, LTC1267-ADJ5	●		0.2	1	µA
V_{OUT}	Regulated Output Voltage						
	3.3V Output	LTC1267: V_{IN} = 9V, I_{LOAD} = 700mA	●	3.23	3.33	3.43	V
	5V Output	LTC1267, LTC1267-ADJ5: V_{IN} = 9V, I_{LOAD} = 700mA	●	4.90	5.05	5.20	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 9V to 40V		–40	0	40	mV
	Output Voltage Load Regulation	Figure 1 Circuit					
	3.3V Output	5mA < I_{LOAD} < 2.0A	●		40	65	mV
	5V Output	5mA < I_{LOAD} < 2.0A	●		60	100	mV
	Burst Mode Output Ripple	I_{LOAD} = 0A			50		mV_{P-P}
V_{CC}	Internal Regulator Voltage	V_{IN} = 12V to 40V, EXT V_{CC} = 0V, I_{CC} = 10mA	●	4.25	4.5	4.75	V
$V_{IN} - V_{CC}$	V_{CC} Dropout Voltage	V_{IN} = 4V, EXT V_{CC} = Open, I_{CC} = 10mA			200	300	mV
I_{EXTVCC}	EXT V_{CC} Pin Current (Note 3)	EXT V_{CC} = 5V, Sleep Mode			360		µA
I_{IN}	V_{IN} Pin Current (Note 3)						
	Normal	V_{IN} = 12V, EXT V_{CC} = 5V			320		µA
		V_{IN} = 40V, EXT V_{CC} = 5V			550		µA
	Shutdown	V_{IN} = 12V, V_{MSHDN} = 2V			15		µA
		V_{IN} = 40V, V_{MSHDN} = 2V			25		µA
$V_{EXTVCC} - V_{CC}$	EXT V_{CC} Switch Drop	V_{IN} = 12V, EXT V_{CC} = 5V, I_{SWITCH} = 10mA			200	300	mV
$V_{PGATE} - V_{IN}$	PGate to Source Voltage (Off)	V_{IN} = 12V		–0.2	0		V
		V_{IN} = 40V		–0.2	0		V
$V_{SENSE^+1,2} - V_{SENSE^-1,2}$	Current Sense Threshold Voltage	LTC1267-ADJ, LTC1267-ADJ5					
		$V_{SENSE^-1,2}$ = 5.1V, $V_{FB1,2} = V_{OUT}/4$ + 25mV (Forced)			25		mV
		$V_{SENSE^-1,2}$ = 4.9V, $V_{FB1,2} = V_{OUT}/4$ – 25mV (Forced)	●	135	160	180	mV
$V_{SENSE^+3,5} - V_{SENSE^-3,5}$	Current Sense Threshold Voltage	LTC1267					
		$V_{SENSE^-3,5} = V_{OUT}$ + 100mV (Forced)			25		mV
		$V_{SENSE^-3,5} = V_{OUT}$ – 100mV (Forced)	●	135	160	180	mV
V_{SHDN}	Shutdown Threshold						
	MSHDN			0.8	1.4	2.0	V
	SHDN1, 3, 5			0.6	0.8	2.0	V
I_{MSHDN}	MSHDN Input Current	V_{MSHDN} = 5V			12	20	µA
I_{CT}	C_T Pin Discharge Current	V_{OUT} in Regulation		50	70	90	µA
		V_{OUT} = 0V			2	10	µA
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V		4	5	6	µs
t_r, t_f	Driver Output Transition Times	C_L = 3000pF (PDrive and NGate Pins), V_{IN} = 6V			100	200	ns

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, V_{IN} = 12V, V_{MSHDN}, $V_{SHDN1,3,5}$ = 0V (Notes 2, 5), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{FB1,2}$	Feedback Voltage	LTC1267-ADJ, LTC1267-ADJ5: V_{IN} = 9V		1.2	1.25	1.3	V
V_{OUT}	Regulated Output Voltage	V_{IN} = 9V					
	3.3V Output	I_{LOAD} = 700mA		3.17	3.30	3.48	V
	5V Output	I_{LOAD} = 700mA		4.85	5.05	5.25	V
I_{IN}	V_{IN} Pin Current (Note 3)						
	Normal	V_{IN} = 12V, EXT V_{CC} = 5V			320		µA
		V_{IN} = 40V, EXT V_{CC} = 5V			550		µA
	Shutdown	V_{IN} = 12V, V_{MSHDN} = 2V			15		µA
		V_{IN} = 40V, V_{MSHDN} = 2V			25		µA
I_{EXTVCC}	EXT V_{CC} Pin Current (Note 3)	EXT V_{CC} = 5V, Sleep Mode			360		µA
V_{CC}	Internal Regulator Voltage	V_{IN} = 12V to 40V, EXT V_{CC} = 0V, I_{CC} = 20mA			4.5		V
$V_{SENSE}^+ - V_{SENSE}^-$	Current Sense Threshold Voltage	Low Threshold (Forced)			25		mV
		High Threshold (Forced)		130	160	185	mV
V_{MSHDN}	Shutdown Threshold MSHDN			0.8	1.4	2.0	V
t_{OFF}	Off-Time (Note 4)	C_T = 390pF, I_{LOAD} = 700mA, V_{IN} = 10V		3	5	7	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC1267/LTC1267-ADJ/LTC1267ADJ5: $T_J = T_A + (P_D \times 95°C/W)$

Note 2: On LTC1267 versions which have MSHDN and SHDN1, 3, 5 pins, they must be at ground potential for testing.

Note 3: The LTC1267 V_{IN} and EXT V_{CC} current measurements exclude MOSFET driver currents. When V_{CC} power is derived from the output via EXT V_{CC}, the input current increases by ($I_{GATECHG}$ × Duty Cycle)/Efficiency. See Typical Performance Characteristics and Applications Information.

Note 4: In applications where R_{SENSE} is placed at ground potential, the off-time increases approximately 40%.

Note 5: The LTC1267/LTC1267-ADJ/LTC1267-ADJ5 are not tested and quality-assurance sampled at –40°C to 85°C. These specifications are guaranteed by design and/or correlation.

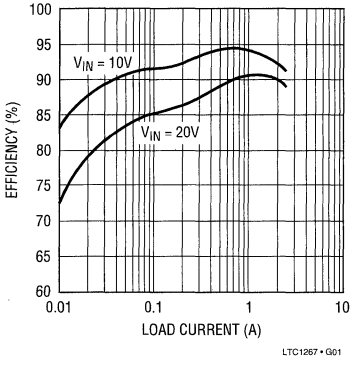
Note 6: The logic level power MOSFETs shown in Figure 1 are rated for $V_{DS(MAX)}$ = 30V. For operation at V_{IN} > 30V, use standard threshold MOSFETs with EXT V_{CC} powered from a 9V supply. See applications information.

Note 7: LTC1267-ADJ and LTC1267-ADJ5 are tested at an output of 3.3V

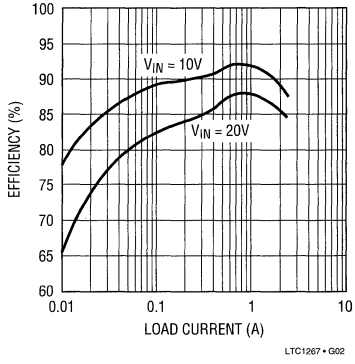
4

TYPICAL PERFORMANCE CHARACTERISTICS

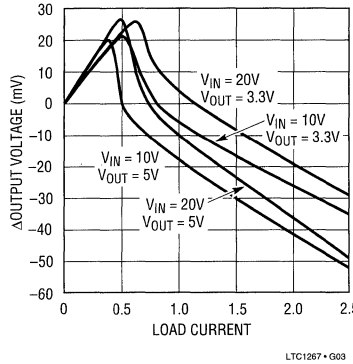
5V Output Efficiency vs Load Current



3.3V Output Efficiency vs Load Current

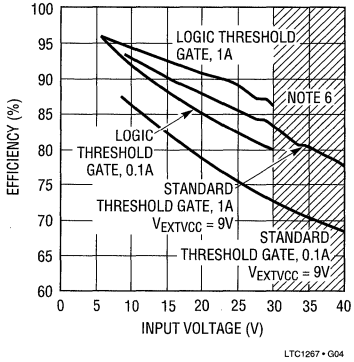


Load Regulation

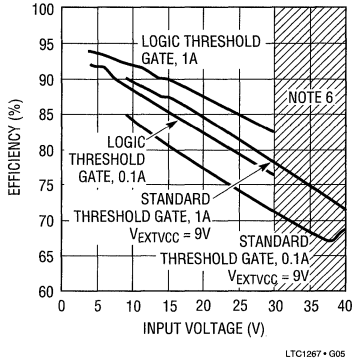


TYPICAL PERFORMANCE CHARACTERISTICS

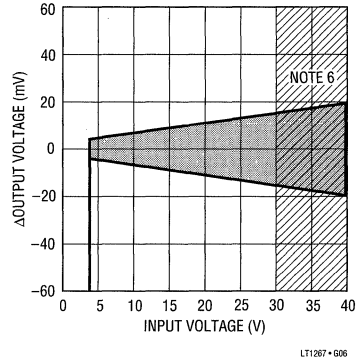
5V Output Efficiency vs Line Voltage



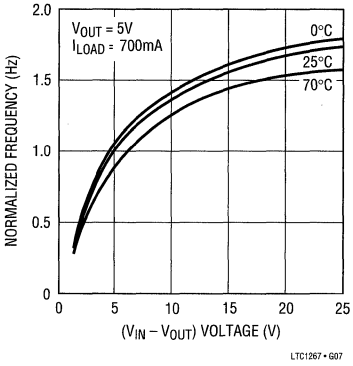
3.3V Output Efficiency vs Line Voltage



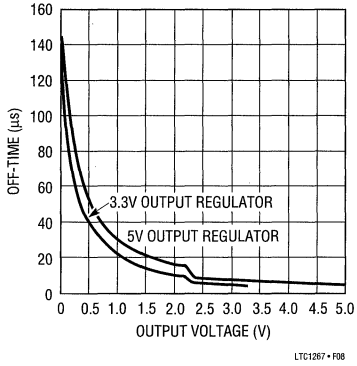
Line Regulation



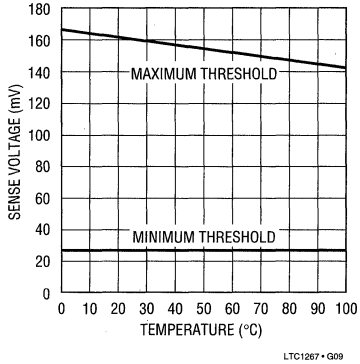
Operating Frequency vs (V_{IN} – V_{OUT})



Off-Time vs Output Voltage



Current Sense Threshold Voltage



PIN FUNCTIONS (Applies to both regulator sections)

V_{IN}: Main Supply Input Pin.

EXT V_{CC}: External V_{CC} Supply for the Regulators. See EXT V_{CC} Pin Connection.

V_{CC}: Output of the Internal 4.5V Linear Regulator, EXT V_{CC} Switch, and Supply Inputs for Driver and Control Circuits. The driver and control circuits are powered from the higher of the 4.5V regulator or EXT V_{CC} voltage. Must be closely decoupled to the power ground.

PGND: Power Ground. Connect to the source of N-channel MOSFET and the (–) terminal of C_{IN}.

SGND: Small-Signal Ground. Must be routed separately from other grounds to the (–) terminal of C_{OUT}.

PGATE: Level Shifted Gate Drive for the Top P-channel MOSFET. The voltage swing at the PGate pin is from V_{IN} to (V_{IN} – V_{CC}).

PDRIVE: High Current Gate Drive for the Top P-channel MOSFET. The PDrive pin swings from V_{CC} to GND.

NGATE: High Current Drive for the Bottom N-channel MOSFET. The NGate pin swings from GND to V_{CC}.

PIN FUNCTIONS

CAP: Charge Compensation Pin. A capacitor to V_{CC} provides charge required by the PGate level shift capacitor during supply transitions. The charge compensation capacitor must be larger than the gate drive capacitor.

C_T: External Capacitor. From this pin to ground sets the operating frequency. (The frequency is also dependent upon the ratio V_{OUT}/V_{IN}).

I_{TH}: Gain Amplifier Decoupling Point. The regulator current comparator threshold increases with the I_{TH} pin voltage.

SENSE⁻: Connects to internal resistive divider which sets the output voltage. The Sense⁻ pin is also the (–) input of the current comparator.

SENSE⁺: The (+) Input for the Current Comparator. A built-in offset between the Sense⁺ and Sense⁻ pins, in conjunction with R_{SENSE}, sets the current trip threshold.

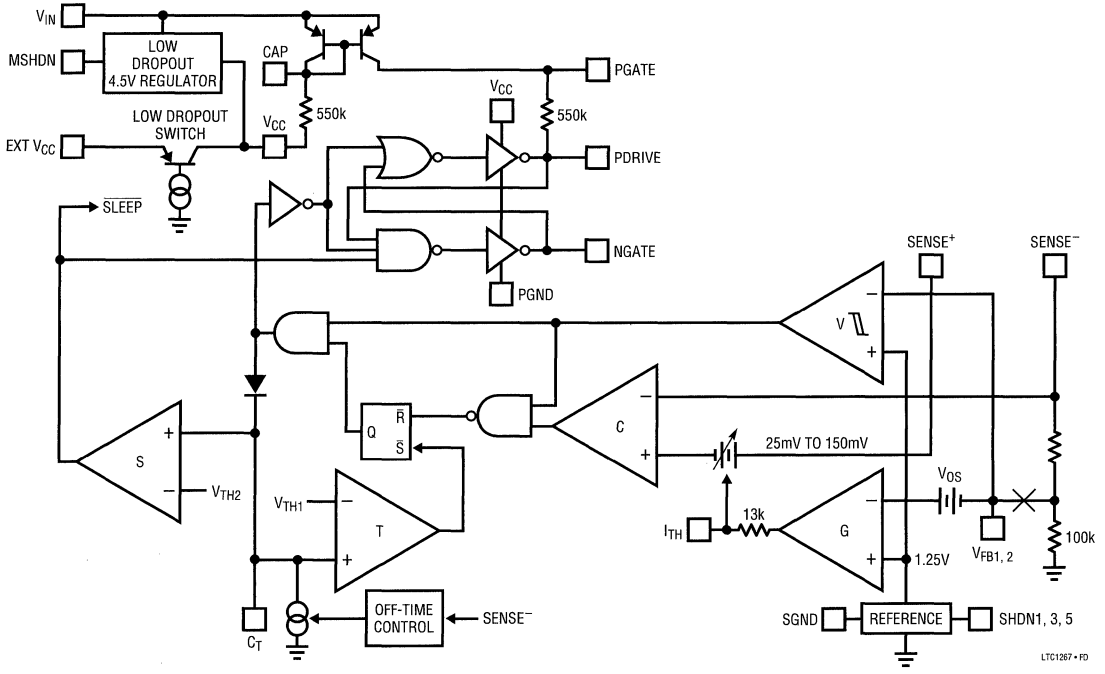
$V_{FB1, 2}$: These pins receive the feedback voltage from an external resistive divider used to set the output voltage of the adjustable section.

MSHDN: Master Shutdown Pin. Taking MSHDN high shuts down V_{CC} and all control circuitry.

SHDN1, 3, 5: These pins shut down the individual regulator control circuitry (V_{CC} is not affected). Taking SHDN1, 3, 5 pins high turns off the control circuitry of adjustable 1, 3.3V, 5V sections and holds both MOSFETs off. Must be at ground potential for normal operation.

FUNCTIONAL DIAGRAM

Internal divider broken at $V_{FB1,2}$ for adjustable versions. Only one regulator block shown.)



OPERATION (Refer to Functional Diagram)

The LTC1267 series consists of two individual regulator blocks, each using current mode, constant off-time architectures to synchronously switch an external pair of complementary power MOSFETs. The two regulators are internally set to provide output voltages of 3.3V and 5V for the LTC1267. The LTC1267-ADJ is configured to provide two adjustable output voltages, each set by their individual external resistor dividers. The LTC1267-ADJ5 has adjustable and 5V output voltages. Operating frequency is individually set on each section by the external capacitors attached to the C_T pin.

The output voltage is sensed by an internal voltage divider connected to the Sense$^-$ pin or external divider returned to the V_{FB} pin (LTC1267-ADJ, LTC1267-ADJ5). A voltage comparator V and a gain block G compare the divided output voltage with a reference voltage of 1.25V. To optimize efficiency, the LTC1267 series automatically switches between two modes of operation, Burst Mode and continuous mode. The voltage comparator is the primary control element when the device is in Burst Mode operation, while the gain block controls the output voltage in continuous mode.

A low dropout 4.5V regulator provides the operating voltage V_{CC} for the MOSFET drivers and control circuitry during start-up. During normal operation, the LTC1267 family powers the drivers and control from the output via the EXT V_{CC} pin to improve efficency. The NGate pin is referenced to ground and drives the N-channel MOSFET gate directly. The P-channel gate drive must be referenced to the main supply input V_{IN}, which is accomplished by level-shifting the PDrive signal via an internal 550k resistor and an external capacitor.

During the switch "ON" cycle in continuous mode, current comparator C monitors the voltage between Sense$^+$ and Sense$^-$ pins connected across an external shunt in series with the inductor. When the voltage across the shunt reaches its threshold value, the PGate output is switched to V_{IN}, turning off the P-channel MOSFET. The timing capacitor C_T is now allowed to discharge at a rate determined by the off-time controller. The discharge current is made proportional to the output voltage to model the inductor current, which decays at a rate that is also proportional to the output voltage. While the timing capacitor is discharging, the NGate output is high, turning on the N-channel MOSFET.

When the voltage on the timing capacitor has discharged past V_{TH1}, comparator T trips, setting the flip-flop. This causes the NGate output to go low (turning off the N-channel MOSFET) and the PGate output to also go low (turning the P-channel MOSFET back on). The cycle then repeats. As the load current increases, the output voltage decreases slightly. This causes the output of the gain stage to increase the current comparator threshold, thus tracking the load current.

The sequence of events for Burst Mode operation is very similar to continuous operation with the cycle interrupted by the voltage comparator. When the output voltage is at or above the desired regulated value, the P-channel MOSFET is held off by comparator V and the timing capacitor continues to discharge below V_{TH1}. When the timing capacitor discharges past V_{TH2}, voltage comparator S trips, causing the internal $\overline{SLEEP}$ line to go low and the N-channel MOSFET to turn off.

The circuit now enters sleep mode with both power MOSFETs turned off. In sleep mode a majority of the circuitry is turned off, dropping the quiescent current from several mA (with the MOSFETs switching) to 360μA. The load current is now being supplied by the output capacitor. When the output voltage has dropped by the amount of hysteresis in comparator V, the P-channel MOSFET is again turned on and this process repeats.

To avoid the operation of the current loop interfering with Burst Mode operation, a built-in offset V_{OS} is incorporated in the gain stage. This prevents the current comparator threshold from increasing until the output voltage has dropped below a minimum threshold.

To prevent both the external MOSFETs from ever being turned on at the same time, feedback is incorporated to sense the state of the driver output pins. Before the NGate output can go high, the PDrive output must also be high. Likewise, the PDrive output is prevented from going low while the NGate output is high.

APPLICATIONS INFORMATION

The LTC1267 Compared to the LTC1159, LTC1149 and LTC1142 Family

The LTC1267 family is a dual LTC1159. Identical to the LTC1159, the LTC1267 can reduce the quiescent and shutdown currents by making use of an internal switch which allows the driver and control sections to be powered from an external source to improve efficiency.

The basic LTC1267 application circuit shown in Figure 1 is limited to a maximum input voltage of 30V due to external MOSFET breakdown. If the application does not require greater than 18V operation the LTC1142HV should be used.

Component Selection

The basic LTC1267 application circuit is shown in Figure 1. External component selection is driven by the load requirement and begins with the selection of R_{SENSE}. Once R_{SENSE} is known, C_T and L can be chosen. Next, the power MOSFETs and diode are selected. Finally, C_{IN} and C_{OUT} are selected and the loop is compensated. Since the adjustable, 3.3V and 5V sections in the LTC1267 are identical, the process of component selection is the same for both sections.

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The LTC1267 current comparators have a threshold range which extends from a minimum of $25mV/R_{SENSE}$ to a maximum of $150mV/R_{SENSE}$. The current comparator threshold sets the peak of the inductor ripple current, yielding a maximum output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current. *For proper Burst Mode operation, $I_{RIPPLE(P-P)}$ must be less than or equal to the minimum current comparator threshold.*

Since efficiency generally increases with ripple current, the maximum allowable ripple current is assumed, i.e., $I_{RIPPLE(P-P)} = 25mV/R_{SENSE}$ (see C_T and L Selection for Operating Frequency). Solving for R_{SENSE} and allowing a margin for variations in the LTC1267 and external component values yields:

$$R_{SENSE} = \frac{100mV}{I_{MAX}}$$

The LTC1267 works well with values of R_{SENSE} from 0.02Ω to 0.2Ω. Figure 2 shows the selection of R_{SENSE} vs maximum output current.

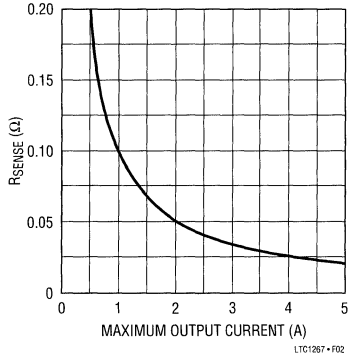


Figure 2. Selecting R_{SENSE}

The load current below which Burst Mode operation commences, I_{BURST} and the peak short-circuit current $I_{SC(PK)}$ both track I_{MAX}. Once R_{SENSE} has been chosen, I_{BURST} and $I_{SC(PK)}$ can be predicted from the following:

$$I_{BURST} \approx \frac{15mV}{R_{SENSE}}$$

$$I_{SC(PK)} = \frac{150mV}{R_{SENSE}}$$

The LTC1267 automatically extends t_{OFF} during a short circuit to allow sufficient time for the inductor current to decay between switch cycles. The resulting ripple current causes the average short-circuit current $I_{SC(AVG)}$ to be reduced to approximately I_{MAX}.

C_T and L Selection for Operating Frequency

Each regulator section of the LTC1267 uses a constant off-time architecture with t_{OFF} determined by an external timing capacitor C_T. The value of C_T is calculated from the desired continuous mode operating frequency (f_O):

$$C_T = \frac{7.8 \times 10^{-5}}{f_O}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

A graph for selecting C_T vs frequency including the effects of input voltage is given in Figure 3.

APPLICATIONS INFORMATION

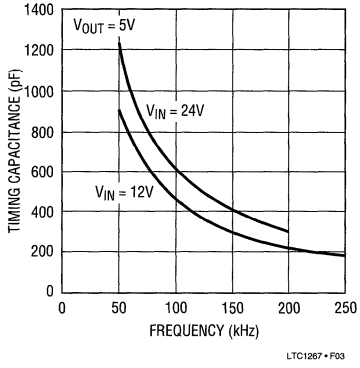


Figure 3. Timing Capacitor Value

As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The complete expression for operating frequency is given by:

$$f_O = \frac{1}{t_{OFF}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where:

$$t_{OFF} = 1.3 \times 10^4 \times C_T$$

Once the frequency has been set by C_T, the inductor L must be chosen to provide no more than $0.025V/R_{SENSE}$ of peak-to-peak inductor ripple current. This results in a minimum required inductor value of:

$$L_{MIN} = 5.1 \times 10^5 \times R_{SENSE} \times C_T \times V_{OUT}$$

As the inductor value is increased from the minimum value, the ESR requirements for the output capacitor are eased at the expense of efficiency. If too small an inductor is used, the LTC1267 may not enter Burst Mode operation and efficiency will be severely degraded at low currents.

Inductor Core Selection

Once the minimum value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite, molypermalloy (MPP), or Kool Mμ® cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down but copper I^2R losses increase. For additional information regarding inductor selection, please refer to the LTC1159 data sheet.

Power MOSFET and Diode Selection

Two external power MOSFETs must be selected for use with each section of the LTC1267: a P-channel MOSFET for the main switch, and an N-channel MOSFET for the synchronous switch.

The peak-to-peak gate drive levels are set by the V_{CC} voltage on the LTC1267. This voltage is typically 4.5V during start-up and 5V to 7V during normal operation (see EXT V_{CC} Pin Connection). Consequently, *logic-level threshold MOSFETs must be used in most LTC1267 family applications.* The only exceptions are applications in which EXT V_{CC} is powered from an external supply greater than 8V, in which standard threshold MOSFETs ($V_{GS(TH)}$ > 4V) may be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, input voltage, and maximum output current. When the LTC1267 is operating in continuous mode, the duty cycles for the two MOSFETs are given by:

$$\text{Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{N-Channel Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET dissipations at maximum output current are given by:

$$\text{P-Ch } P_D = \frac{V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \delta_P) R_{DS(ON)} + k (V_{IN})^2 (I_{MAX}) (C_{RSS}) f_O$$

$$\text{N-Ch } P_D = \frac{V_{IN} - V_{OUT}}{V_{IN}} (I_{MAX})^2 (1 + \delta_N) R_{DS(ON)}$$

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Vhere δ is the temperature dependency of $R_{DS(ON)}$ and k s a constant inversely related to the gate drive current.

oth MOSFETs have I^2R losses, while the P-channel quation includes an additional term for transition losses, vhich are highest at high input voltages. For $V_{IN} < 20V$, the igh current efficiency generally improves with larger IOSFETs, while for $V_{IN} > 20V$, the transition losses rapidly ncrease to the point that the use of a higher $R_{DS(ON)}$ device vith lower C_{RSS} actually provides higher efficiency. The l-channel MOSFET losses are the greatest at high input oltage or during a short circuit when the N-channel duty ycle is nearly 100%.

he term (1 + δ) is generally given for a MOSFET in the orm of a normalized $R_{DS(ON)}$ vs temperature curve, but δ 0.007/°C can be used as an approximation for low oltage MOSFETs. C_{RSS} is usually specified in the MOSFET lectrical characteristics. The constant k = 5 can be used or the LTC1267 to estimate the relative contributions of ne two terms in the P-channel dissipation equation.

he Schottky diodes D3 and D5 shown in Figure 1 only onduct during the dead-time between the conduction of ne respective power MOSFETs. The sole purpose of D3 nd D5 is to prevent the body diode of the N-channel IOSFET from turning on and storing charge during the ead-time, which could cost as much as 1% in efficiency lthough there are no other harmful effects if D3 and D5 re omitted). Therefore, D3 and D5 should be selected for forward voltage of less than 0.6V when conducting I_{MAX}.

$_{IN}$ and C_{OUT} Selection

n continuous mode, the source current of the P-channel IOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To revent large voltage transients, a low ESR input capaci- or sized for the maximum RMS current must be used. The aximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx I_{MAX} \frac{[V_{OUT}(V_{IN} - V_{OUT})]^{1/2}}{V_{IN}}$$

his formula has a maximum at $V_{IN} = 2V_{OUT}$ where $I_{RMS} = {}_{OUT}/2$. This simple worst-case condition is commonly sed for design because even significant deviations do not ffer much relief. Note that capacitor manufacturer's pple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question. An additional 0.1µF ceramic capacitor is also required on V_{IN} for high frequency decoupling.

The selection of C_{OUT} is driven by the required Effective Series Resistance (ESR). *The ESR of C_{OUT} must be less than twice the value of R_{SENSE} for proper operation of the LTC1267:*

C_{OUT} Required ESR < $2R_{SENSE}$

Optimum efficiency is obtained by making the ESR equal to R_{SENSE}. As the ESR is increased up to $2R_{SENSE}$, the efficiency degrades by less than 1%. If the ESR is greater than $2R_{SENSE}$, the voltage ripple on the output capacitor will prematurely trigger Burst Mode operation, resulting in disruption of continuous mode and an efficiency hit which can be several percent.

Manufacturers such as Nichicon, United Chemicon, and Sprague should be considered for high performance capacitors. In surface mount applications multiple capacitors may have to be paralleled to meet the capacitance, ESR, or RMS current handling requirements of the application. For additional information regarding capacitor selection, please refer to the LTC1159 data sheet.

At low supply voltages, a minimum capacitance at C_{OUT} is needed to prevent an abnormal low frequency operating mode (see Figure 4). When C_{OUT} is made too small, the output ripple at low frequencies will be large enough to trip

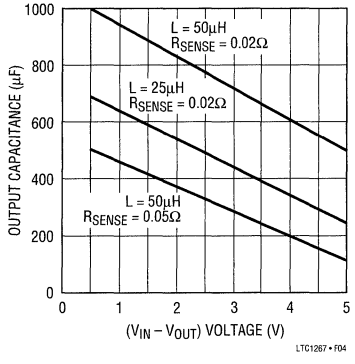

Figure 4. Minimum Suggested C_{OUT}

APPLICATIONS INFORMATION

the voltage comparator. This causes Burst Mode operation to be activated when the LTC1267 would normally be in continuous operation. The effect is most pronounced with low values of R_{SENSE} and can be improved by operating at higher frequencies with lower values of L. The output remains in regulation at all times.

EXT V_{CC} Pin Connection

The LTC1267 contains an internal PNP switch connected between the EXT V_{CC} and V_{CC} pins. The switch closes and supplies the V_{CC} power whenever the EXT V_{CC} pin is higher in voltage than the 4.5V internal regulator. This allows the MOSFET driver and control power to be derived from the output during normal operation and from the internal regulator when the output is out of regulation (start-up, short circuit).

Significant efficiency gain can be realized by powering V_{CC} from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For LTC1267, LTC1267-ADJ or LTC1267-ADJ5 this simply means connecting the EXT V_{CC} pin directly to V_{OUT} of the 5V regulator.

The following list summarizes the four possible connections for EXT V_{CC}:

1. EXT V_{CC} left open. This will cause V_{CC} to be powered only from the internal 4.5V regulator, resulting in reduced MOSFET gate drive levels and an efficiency penalty of up to 10% at high input voltages.
2. EXT V_{CC} connected directly to highest V_{OUT} of the two regulators. This is the normal connection for LTC1267/LTC1267-ADJ/LTC1267-ADJ5 and provides the highest efficiency.
3. EXT V_{CC} connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting EXT V_{CC} to an output-derived voltage which has been boosted to greater than 4.5V. This can be done either with the inductive boost winding shown in Figure 5a or the capacitive charge pump shown in Figure 5b. The charge pump has the advantage of simple magnetics and generally provides the highest efficiency at the expense of a slightly higher parts count.

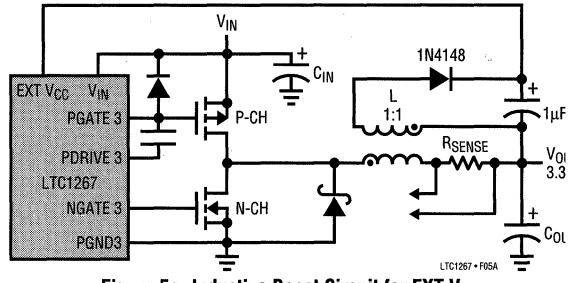

Figure 5a. Inductive Boost Circuit for EXT V_{CC}

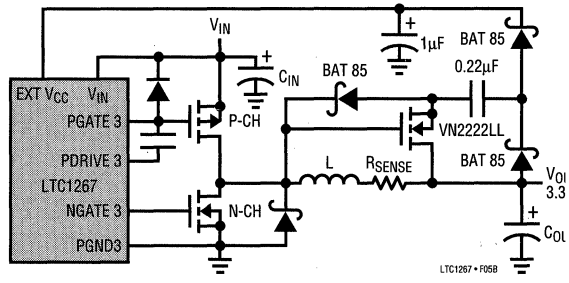

Figure 5b. Capacitive Charge Pump for EXT V_{CC}

4. EXT V_{CC} connected to an external supply. If an external supply is available in the 5V to 10V range it may be used to power EXT V_{CC} providing it is compatible with the MOSFET gate drive requirements. When driving standard threshold MOSFETs, the external supply must always be present during operation to prevent MOSFET failure due to insufficient gate drive.

   Under the condition that EXT V_{CC} is connected to V_{OUT1} which is greater than 5.5V, to power down the whole regulator, both the pins MSHDN and SHDN1 have to be pulled high. If SHDN1 is left floating or grounded the EXT V_{CC} may self-power from V_{OUT1}, preventing complete shutdown.

LTC1267 Adjustable Applications

When an output voltage other than 3.3V or 5V is required, the LTC1267-ADJ and LTC1267-ADJ5 adjustable versions are used with an external resistive divider from V_{OUT} to the $V_{FB1,2}$ pins. This is shown in Figure 6. The regulated voltage is determined by:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) 1.25V$$

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The $V_{FB1, 2}$ pin is extremely sensitive to pickup from the inductor switching node. Care should be taken to isolate the feedback network from the inductor and a 100pF capacitor should be connected between the $V_{FB1, 2}$ and SGND pins next to the package.

The circuit in Figure 6 cannot be used to regulate a V_{OUT} which is greater than the maximum voltage allowed on the LTC1267 EXT V_{CC} pin (10V). In applications with $V_{OUT} > 10V$, R_{SENSE} must be moved to the ground side of the output capacitor and load. This operates the current sense comparator at 0V common mode, increasing the off-time approximately 40% and requiring the use of a smaller timing capacitor C_T.

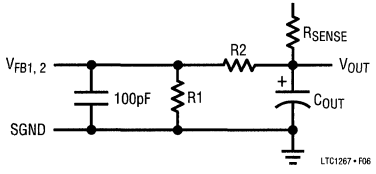

Figure 6. LTC1267-ADJ/LTC1267-ADJ5 External Feedback Network

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc., are the individual losses as a percentage of input power. (For high efficiency circuits, only small errors are incurred by expressing losses as a percentage of output power.)

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC1267 circuits:

1. LTC1267 V_{IN} current
2. LTC1267 V_{CC} current
3. I^2R losses
4. P-channel transition losses

1. LTC1267 V_{IN} current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. V_{IN} currents results in a small (<1%) loss which increases with V_{IN}.

2. LTC1267 V_{CC} current is the sum of the MOSFET driver and control circuits currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{CC} to ground. The resulting dQ/dt is a current out of V_{CC} which is typically much larger than the control circuit current. In continuous mode $I_{GATECHG} \approx f_O(Q_P + Q_N)$, where Q_P and Q_N are the gate charges of the two MOSFETs.

   By powering EXT V_{CC} from an output-derived source, the additional V_{IN} current resulting from the driver and control currents will be scaled by a factor of Duty Cycle/Efficiency. For example, in a 20V to 5V application, 10mA of V_{CC} current results in approximately 3mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are easily predicted from the DC resistances of the MOSFET, inductor, and current shunt. In continuous mode all the output current flows through L and R_{SENSE}, but is "chopped" between the P-channel and N-channel MOSFETs. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 0.1\Omega$, $R_L = 0.15\Omega$, and $R_{SENSE} = 0.05\Omega$, then the total resistance is 0.3Ω. This results in losses ranging from 3% to 12% as the output current increases from 0.5A to 2A. I^2R losses cause the efficiency to roll off at high output currents.

4. Transition losses apply only to the P-channel MOSFET and only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} \approx 5 \times V_{IN}^2 \times I_{MAX} \times C_{RSS} \times f_O$$

   Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead-time,

4

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and inductor core losses, generally account for less than 2% total additional loss.

Auxiliary Windings—Suppressing Burst Mode Operation

The LTC1267 synchronous switch removes the normal limitation that power must be drawn from the inductor primary winding in order to extract power from auxiliary windings. With synchronous switching, auxiliary outputs may be loaded without regard to the primary output load, providing that the loop remains in continuous mode operation.

Burst Mode operation can be suppressed at low output currents with a simple external network which cancels the 25mV minimum current comparator threshold. This technique is also useful for eliminating audible noise from certain types of inductors in high current (I_{OUT} > 5A) applications when they are lightly loaded.

An external offset is put in series with the Sense$^-$ pin to subtract from the built-in 25mV offset. An example of this technique is shown in Figure 7. Two 100Ω resistors are inserted in series with the sense leads from the sense resistor.

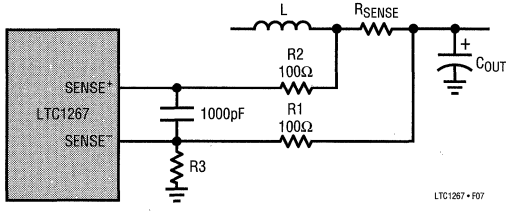


Figure 7. Suppressing Burst Mode Operation

With the addition of R3 a current is generated through R1 causing an offset of:

$$V_{OFFSET} = V_{OUT}\left(\frac{R1}{R1 + R3}\right)$$

If V_{OFFSET} > 25mV, the built-in offset will be cancelled and Burst Mode operation is prevented from occurring. Since V_{OFFSET} is constant, the maximum load current is also decreased by the same offset. Thus, to get back to the same I_{MAX}, the value of the sense resistor must be reduced:

$$R_{SENSE} \approx \frac{75}{I_{MAX}}\ m\Omega$$

To prevent noise spikes from erroneously tripping the current comparator, a 1000pF capacitor is needed across Sense$^+$ and Sense$^-$ pins.

Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC1267. These items are also illustrated graphically in the layout diagram of Figure 8. In general each block should be self-contained with little cross coupling for best performance. Check the following in your layout:

1. Are the signal and power grounds segregated? The LTC1267 signal ground must return to the (–) plate of C_{OUT}. The power ground returns to the source of the N-channel MOSFET, anode of the Schottky diode, and (–) plate of C_{IN}, which should have as short lead lengths as possible.
2. Does the LTC1267 Sense$^-$ pin connect to a point close to R_{SENSE} and the (+) plate of C_{OUT}? In adjustable applications the resistive divider R1 and R2 must be connected between the (+) plate of C_{OUT} and signal ground.
3. Are the Sense$^-$ and Sense$^+$ leads routed together with minimum PC trace spacing? The 1000pF capacitor between the two Sense pins should be as close as possible to the LTC1267. Up to 100Ω may be placed in series with each Sense lead to help decouple the Sense pins. However, when these resistors are used the capacitor should be no larger than 1000pF.
4. Does the (+) plate of C_{IN} connect to the source of the P-channel MOSFET as closely as possible? An additional 0.1µF ceramic capacitor between V_{IN} and power ground may be required in some applications.
5. Is the V_{CC} decoupling capacitor connected closely between the V_{CC} pins of the LTC1267 and power ground? This capacitor carries the MOSFET driver peak currents.

APPLICATIONS INFORMATION

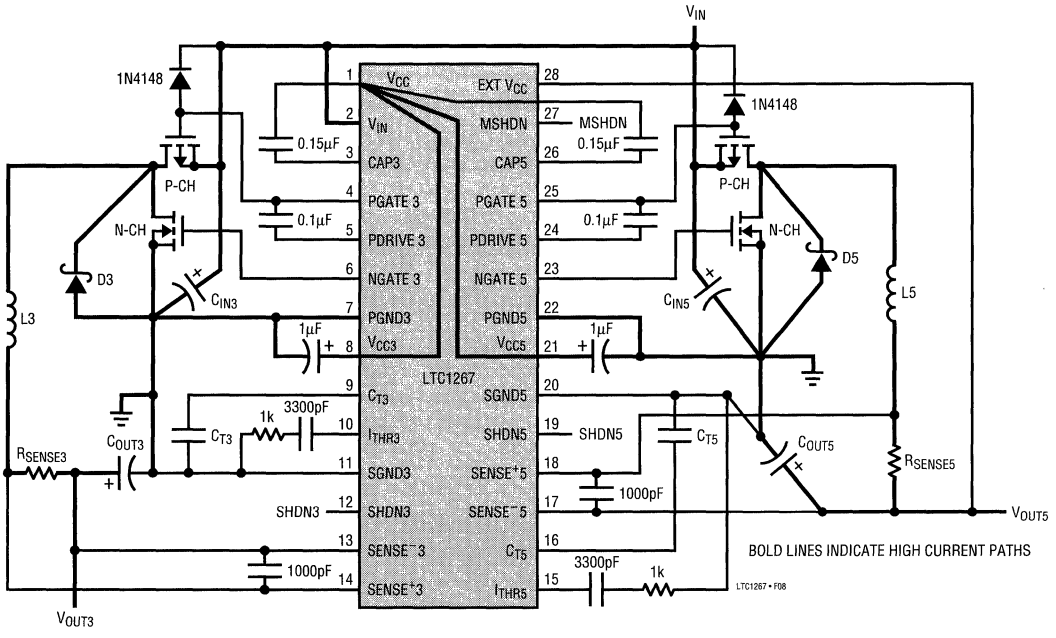


Figure 8. LTC1267 Layout Diagram

6. In adjustable versions, the feedback pin is very sensitive to pickup from the switch node. Care must be taken to isolate $V_{FB1, 2}$ from possible capacitive coupling of the inductor switch signal.
7. Are MSHDN and SHDN1, 3, 5 actively pulled to ground during normal operation? These shutdown pins are high impedance and must not be allowed to float.

Troubleshooting Hints

Since efficiency is critical to LTC1267 applications, it is very important to verify that the circuit is functioning correctly in both continuous and Burst Mode operation. The waveform to monitor is the voltage on the C_T pin.

In continuous mode ($I_{LOAD} > I_{BURST}$) the voltage on the C_T pin should be a sawtooth with a $0.9V_{P-P}$ swing. This voltage should never dip below 2V as shown in Figure 9a.

When load currents are low ($I_{LOAD} < I_{BURST}$) Burst Mode operation occurs. The voltage on the C_T pin now falls to ground for periods of time as shown in Figure 9b.

If the C_T is observed falling to ground at high output currents, it indicates poor decoupling or improper grounding. Refer to the Board Layout Checklist.

Inductor current should also be monitored. Look to verify that the peak-to-peak ripple current in continuous mode operation is approximately the same as in Burst Mode operation.

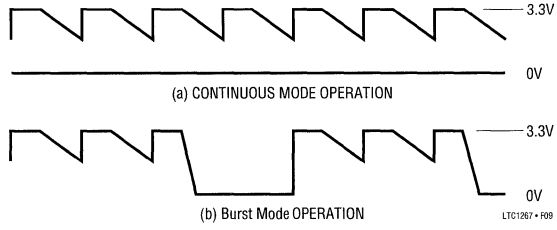
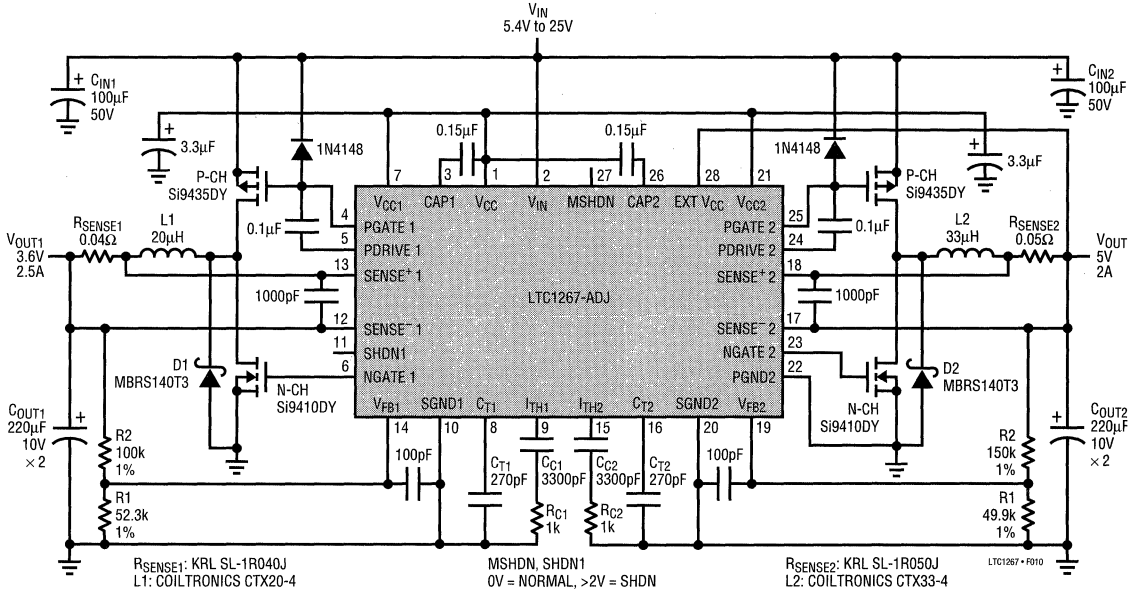


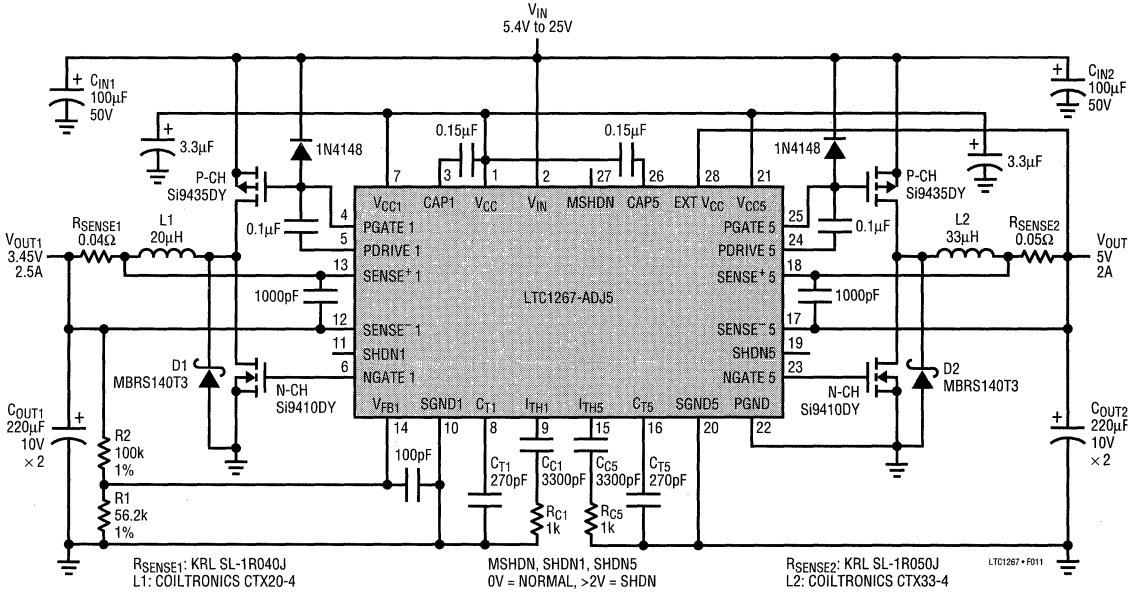
Figure 9. C_T Waveforms

TYPICAL APPLICATIONS

LTC1267-ADJ Dual Regulator with 3.6V/2.5A and 5V/2A Outputs



LTC1267-ADJ5 Dual Regulator with 3.45V/2.5A and 5V/2A Outputs



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142	Dual Step-Down Switching Regulator Controller	Dual Version of LTC1148
LTC1143	Dual Step-Down Switching Regulator Controller	Dual Version of LTC1147
LTC1147	Step-Down Switching Regulator Controller	Nonsynchronous, 8-Pin, $V_{IN} \leq 16V$
LTC1148	Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 20V$
LTC1149	Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 48V$, for Standard Threshold FETs
LTC1159	Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 40V$, for Logic Level FETs
LTC1174	Step-Down Switching Regulator with Internal 0.5A Switch	$V_{IN} \leq 18.5V$, Comparator/Low Battery Detector
LTC1265	Step-Down Switching Regulator with Internal 1A Switch	$V_{IN} \leq 13V$, Comparator/Low Battery Detector
LTC1266	Step-Up/Down Switching Regulator Controller	Synchronous N- or P-Channel FETs, Comparator/Low Battery Detector
LTC1574	Step-Down Switching Regulator with Internal 0.5A Switch and Schottky Diode	$V_{IN} \leq 18.5V$, Comparator

Micropower High Output Current Step-Up Adjustable and Fixed 5V DC/DC Converters

FEATURES

- **5V at 600mA or 12V at 120mA from 2-Cell Supply**
- **200μA Quiescent Current**
- Logic Controlled Shutdown to 15μA
- Low V_{CESAT} Switch: 310mV at 2A Typical
- Burst Mode™ Operation at Light Load
- Current Mode Operation for Excellent Line and Load Transient Response
- Available in 8-Lead SO or PDIP
- **Operates with Supply Voltage as Low as 2V**

APPLICATIONS

- Notebook and Palmtop Computers
- Portable Instruments
- Personal Digital Assistants
- Cellular Telephones
- Flash Memory

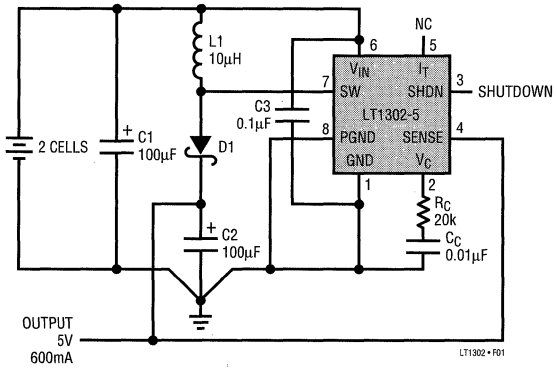
DESCRIPTION

The LT®1302/LT1302-5 are micropower step-up DC/DC converters that maintain high efficiency over a wide range of output current. They operate from a supply voltage as low as 2V and feature automatic shifting between Burst Mode operation at light load, and current mode operation at heavy load.

The internal low loss NPN power switch can handle current in excess of 2A and switch at frequencies up to 400kHz. Quiescent current is just 200μA and can be further reduced to 15μA in shutdown.

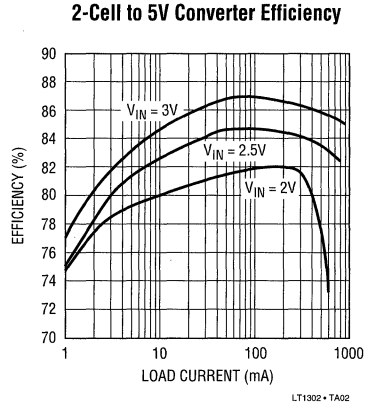
Available in 8-pin PDIP or 8-pin SO packaging, the LT1302/LT1302-5 have the highest switch current rating of any similarly packaged switching regulators presently on the market.

TYPICAL APPLICATION



C1 = C2 = SANYO OS-CON
L1 = COILTRONICS CTX10-3
COILCRAFT DO3316-103
D1 = MOTOROLA MBRS130LT3

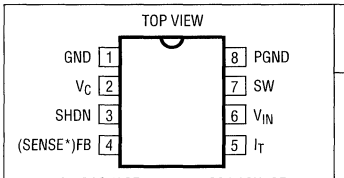
Figure 1. 2-Cell to 5V/600mA DC/DC Converter



ıBSOLUTE MAXIMUM RATINGS

IN Voltage 10V
W Voltage 25V
3 Voltage 10V
HDN Voltage 10V
C Voltage 4V
Voltage 4V
laximum Power Dissipation 700mW
perating Temperature Range ..... 0°C to 70°C
torage Temperature Range ..... –65°C to 150°C
ead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

*FIXED VERSION

PINS 1 AND 8 ARE INTERNALLY CONNECTED IN SOIC PACKAGE

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 80°C/W (S8)

ORDER PART NUMBER
LT1302CN8 LT1302CS8 LT1302CN8-5 LT1302CS8-5
S8 PART MARKING
1302 13025

Consult factory for Industrial and Military grade parts.

ıC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 2.5V, unless otherwise noted.

'MBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Quiescent Current	V_{SHDN} = 0.5V, V_{FB} = 1.3V	●		200	300	µA
		V_{SHDN} = 1.8V	●		15	25	µA
V	Input Voltage Range			2.0			V
			●	2.2		8	V
B	Feedback Voltage (LT1302)	V_C = 0.4V	●	1.22	1.24	1.26	V
	Feedback Pin Bias Current (LT1302)	V_{FB} = 1V			100		nA
	Output Sense Voltage (LT1302-5)	V_C = 0.4V	●	4.85	5.05	5.25	V
	Output Ripple Voltage (LT1302-5)	V_C = 0.4V			50		mV
	Sense Pin Resistance to Ground (LT1302-5)				420		kΩ
S	Offset Voltage	See Block Diagram			15		mV
	Comparator Hysteresis	(Note 1)			5		mV
	Oscillator Frequency	Current Limit Not Asserted (Note 2)		175	220	265	kHz
			●	160		310	kHZ
	Maximum Duty Cycle			75	86	95	%
N	Switch On Time	Current Limit Not Asserted			3.9		µs
F	Switch Off Time				0.7		µs
	Output Line Regulation	2 < V_{IN} < 8V	●		0.06	0.15	%/V
ESAT	Switch Saturation Voltage	I_{SW} = 2A			310	400	mV
			●			475	mV
	Switch Leakage Current	V_{SW} = 5V, Switch Off	●		0.1	10	µA
	Switch Current Limit	V_C = 0.4V (Burst Mode Operation)			1		A
		V_C = 1.25V (Full Power) (Note 3)	●	2.0	2.8	3.9	A
	Error Amplifier Voltage Gain	0.9V ≤ V_C ≤ 1.2V, $\Delta V_C/\Delta V_{FB}$		50	75		V/V
HDNH	Shutdown Pin High		●	1.8			V
HDNL	Shutdown Pin Low		●			0.5	V
IDN	Shutdown Pin Bias Current	V_{SHDN} = 5V	●		8	20	µA
		V_{SHDN} = 2V			3		µA
		V_{SHDN} = 0V	●		0.1	1	µA
	I_T Pin Resistance to Ground				3.9		kΩ

e ● denotes specifications which apply over the 0°C to 70°C
nperature range.

te 1: Hysteresis is specified at DC. Output ripple depends on capacitor
e and ESR.

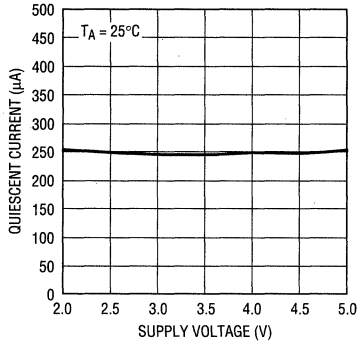
Note 2: The LT1302 operates in a variable frequency mode. Switching frequency depends on load inductance and operating conditions and may be above specified limits.

Note 3: Minimum switch current 100% tested. Maximum switch current guaranteed by design.

4

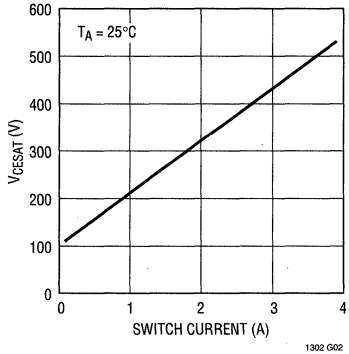
TYPICAL PERFORMANCE CHARACTERISTICS

No-Load Quiescent Current
Circuit of Figure 1



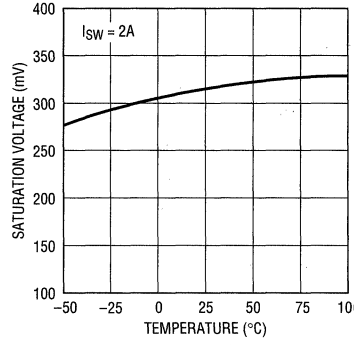
1302 G01

Switch Saturation Voltage



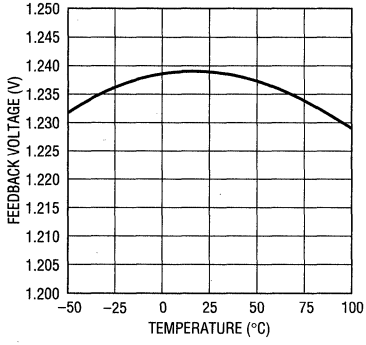
1302 G02

Switch Saturation Voltage



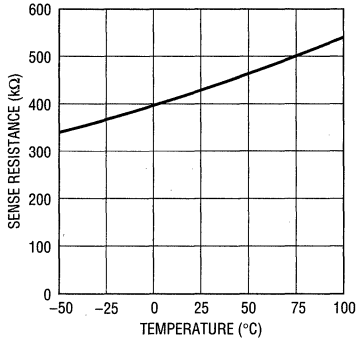
1302 G03

LT1302 Feedback Voltage



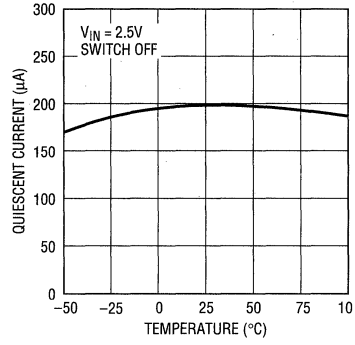
1302 G04

LT1302-5 Sense Pin Resistance



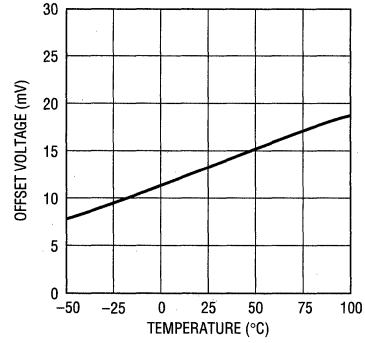
1302 G05

Quiescent Current



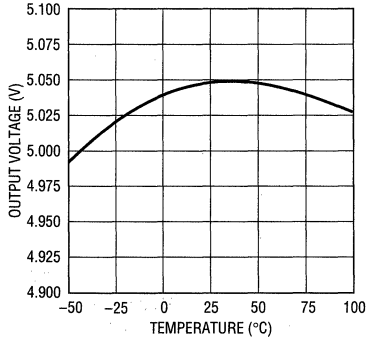
1302 G06

Error Amplifier Offset Voltage



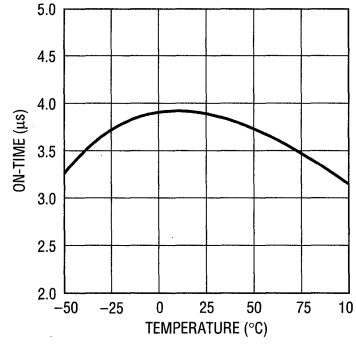
1302 G07

LT1302-5 Output Voltage



1302 G08

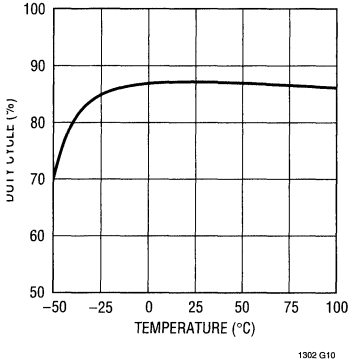
Maximum On-Time



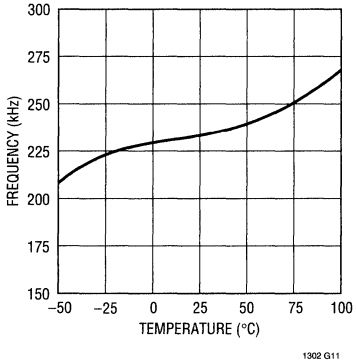
1302 G09

TYPICAL PERFORMANCE CHARACTERISTICS

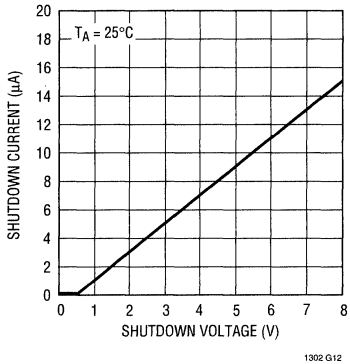
Maximum Duty Cycle



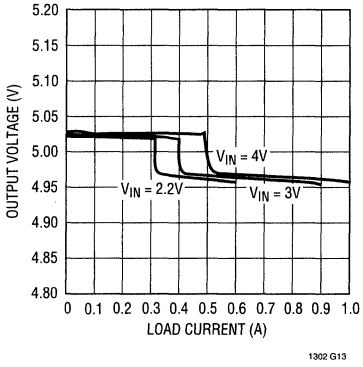
Oscillator Frequency



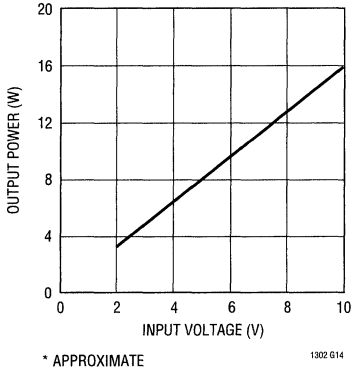
Shutdown Pin Bias Current



LT1302-5 Output Voltage vs Load Current



Maximum Output Power* Boost Mode



4

PIN FUNCTIONS

GND (Pin 1): Signal Ground. Feedback resistor and 0.1µF ceramic bypass capacitor from V_{IN} should be connected directly to this pin.

I_C (Pin 2): Frequency Compensation Pin. Connect series RC to GND. Keep trace short.

SHDN (Pin 3): Shutdown. Pull high to effect shutdown; tie to ground for normal operation.

FB/Sense (Pin 4): Feedback/Sense. On the LT1302 this pin connects to CMP1 input. On the LT1302-5 this pin connects to the output resistor string.

I_T (Pin 5): Normally left floating. Addition of a 3.3k resistor to GND forces the LT1302 into current mode at light loads. Efficiency drops at light load but increases at medium loads. See Applications Information section.

V_{IN} (Pin 6): Supply Pin. Must be bypassed with: (1) a 0.1µF ceramic to GND, and (2) a large value electrolytic to PGND. When V_{IN} is greater than 5V, a low value resistor (2Ω to 10Ω) is recommended to isolate the V_{IN} pin from input supply noise.

PIN FUNCTIONS

SW (Pin 7): Switch Pin. Connect inductor and diode here. Keep layout short and direct.

PGND (Pin 8): Power Ground. Pins 8 and 1 should be connected under the package. In the SO package, pins 1 and 8 are thermally connected to the die. One square inch of PCB copper provides an adequate heat sink for the device.

BLOCK DIAGRAMS

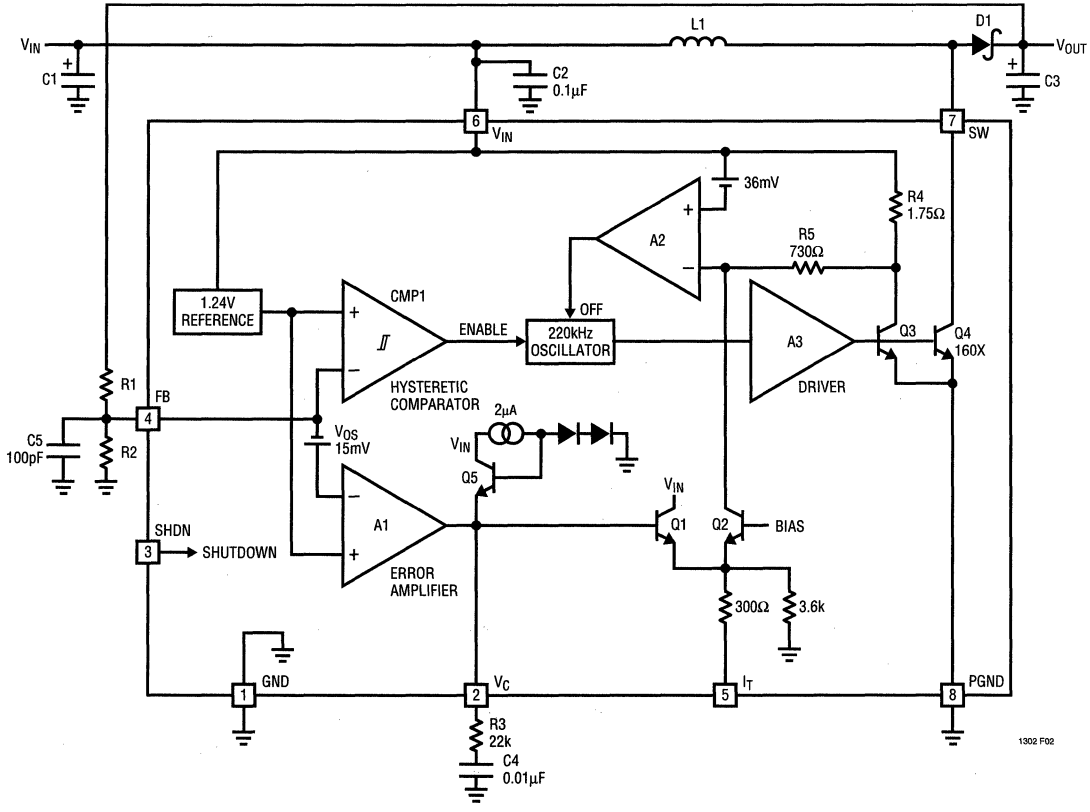


Figure 2. LT1302 Block Diagram

BLOCK DIAGRAMS

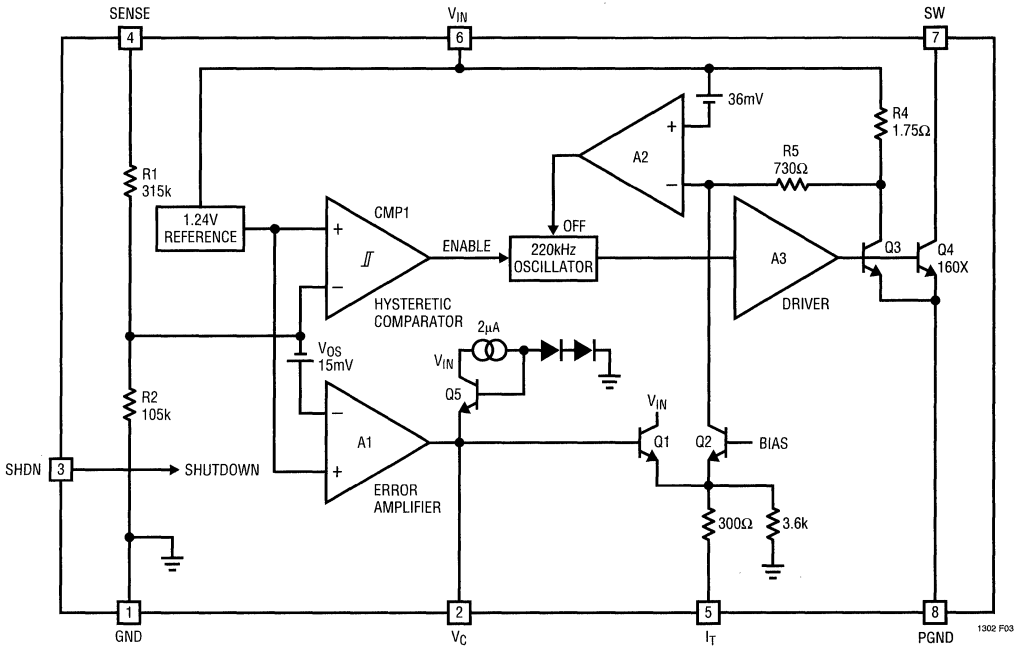


Figure 3. LT1302-5 Block Diagram

OPERATION

The LT1302's operation can best be understood by examining the block diagram in Figure 2. The LT1302 operates in one of two modes, depending on load. With light loads, comparator CMP1 controls the output; with heavy loads, control is passed to error amplifier A1. Burst Mode operation consists of monitoring the FB pin voltage with hysteretic comparator CMP1. When the FB voltage, related to the output voltage by external attenuator R1 and R2, falls below the 1.24V reference voltage, the oscillator is enabled. Switch Q4 alternately turns on, causing current buildup in inductor L1, then turns off, allowing the built-up current to flow into output capacitor C3 via D1. As the output voltage increases, so does the FB voltage; when it exceeds the reference plus CMP1's hysteresis (about 5mV) CMP1 turns the oscillator off. In this mode, peak switch current is limited to approximately 1A by A2, Q2, and Q3. Q2's current, set at 34μA, flows through R5, causing A2's negative input to be 25mV lower than V_{IN}. This node must fall more than 36mV below V_{IN} for A2 to trip and turn off the oscillator. The remaining 11mV is generated by Q3's current flowing through R4. Emitter-area scaling sets Q3's collector current to 0.625% of switch Q4's current. When Q4's current is 1A, Q3's current is 6.25mA, creating an 11mV drop across R4 which, added to R5's 25mV drop, is enough to trip A2.

When the output load is increased to the point where the 1A peak current cannot support the output voltage,

OPERATION

CMP1 stays on and the peak switch current is regulated by the voltage on the V_C pin (A1's output). V_C drives the base of Q1. As the V_C voltage rises, Q2 conducts less current, resulting in less drop across R5. Q4's peak current must then increase in order for A2 to trip. This current mode control results in good stability and immunity to input voltage variations. Because this is a linear, closed-loop system, frequency compensation is required. A series RC from V_C to ground provides the necessary pole-zero combination.

The LT1302-5 incorporates feedback resistors R1 and R2 into the device. Output voltage is set at 5.05V in Burst Mode, dropping to 4.97V in current mode.

APPLICATIONS INFORMATION

Inductor Selection

Inductors used with the LT1302 must fulfill two requirements. First, the inductor must be able to handle current of 2.5A to 3A without runaway saturation. Rod or drum core units usually saturate gradually and it is acceptable to exceed manufacturers' published saturation currents by 20% or so. Second, it should have low DCR, under 0.05Ω so that copper loss is kept low. Inductance value is not critical. Generally, for low voltage inputs down to 2V, a 10µH inductor is recommended (such as Coilcraft DO3316-103). For inputs above 4V to 5V use a 22µH unit (such as Coilcraft DO3316-223). Switching frequency can reach up to 400kHz so the core material should be able to handle high frequency without loss. Ferrite or molypermalloy cores are a better choice than powdered iron. If EMI is a concern a toroidal inductor is suggested, such as Coiltronics CTX20-4.

For a boost converter, duty cycle can be calculated by the following formula:

$$DC = 1 - \left(\frac{V_{IN}}{V_{OUT}}\right)$$

A special situation exists where the V_{OUT}/V_{IN} differential is high, such as a 2V-to-12V converter. The required duty cycle is higher than the LT1302 can provide, so the converter must be designed for *discontinuous* operation. This means that inductor current goes to zero during the switch off-time. In the 2V-to-12V case, inductance must be low enough so that current in the inductor can reach 2A in a single cycle. Inductor value can be defined by:

$$L \leq \frac{(V_{IN} - V_{SW}) \times t_{ON}}{2A}$$

With the 2V input a value of 3.3µH is acceptable. Since the inductance is so low, usually a smaller core size can be used. Efficiency will not be as high as for the continuous case since peak currents will necessarily be higher.

Table 1 lists inductor suppliers along with appropriate part numbers.

Table 1. Recommended Inductors

VENDOR	PART NO.	VALUE(µH)	PHONE NO.
Coilcraft	DO3316-103 DO3316-153 DO3316-223	10 15 22	(708) 639-6400
Coiltronics	CTX10-2 CTX20-4	10 20	(407) 241-7876
Dale	LPT4545-100LA LPT4545-200LA	10 20	(605) 665-9301
Sumida	CD105-100 CD105-150 CDR125-220	10 15 22	(708) 956-0666

Capacitor Selection

The output capacitor should have low ESR for proper performance. A high ESR capacitor can result in "mode-hopping" between current mode and Burst Mode at high load currents because the output voltage will increase by $I_{SW} \times$ ESR when the inductor current is flowing into the diode. Figure 4 shows output voltage of an LT1302-5 boost converter with two 220µF AVX TPS capacitors at the output. Ripple voltage at a 510mA load is about $30mV_{P-P}$

APPLICATIONS INFORMATION

and there is no low frequency component. The total ESR is under 0.03Ω. If a single 100µF aluminum electrolytic capacitor is used instead, the converter mode-hops between current mode and Burst Mode due to high ESR, causing the voltage comparator to trip as shown in Figure 5. The ripple voltage is now over 500mV$_{P-P}$ and contains a low frequency component. Maximum allowable output capacitor ESR can be calculated by the following formula:

$$ESR_{MAX} = \frac{V_{OS} \times V_{OUT}}{V_{REF} \times 1A}$$

where,

V_{OS} = 15mV

V_{REF} = 1.24V

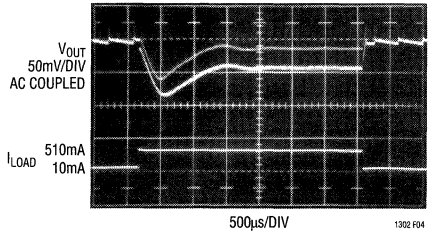


Figure 4. Low ESR Output Capacitor Results in Stable Operation. Ripple Voltage is Under 30mV$_{P-P}$

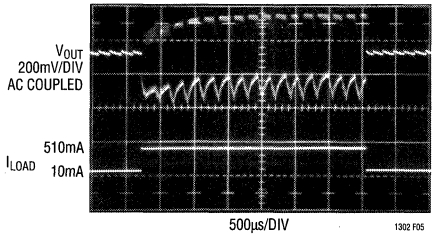


Figure 5. Inexpensive Electrolytic Capacitor Has High ESR, Resulting in Mode-Hop, Ripple Voltage Amplitude Is Over 500mV$_{P-P}$ and Includes Low Frequency Component

Input Capacitor

The input supply should be decoupled with a good quality electrolytic capacitor close to the LT1302 to provide a stable input supply. Long leads or traces from power source to the switcher can have considerable impedance at the LT1302's switching frequency. The input capacitor provides a low impedance at high frequency. A 0.1µF ceramic capacitor is required right at the V_{IN} pin. When the input voltage can be above 5V, a 10Ω/1µF decoupling network for V_{IN} is recommended as detailed in Figure 6. This network is also recommended when driving a transformer.

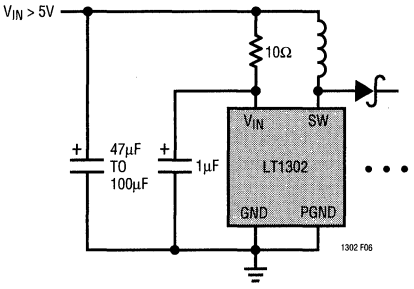


Figure 6. A 10Ω/1µF Decoupling Network at V_{IN} Is Recommended When Input Voltage Is Above 5V

Table 2 lists capacitor vendors along with device types.

Table 2. Recommended Capacitors

VENDOR	SERIES	TYPE	PHONE NO.
AVX	TPS	Surface Mount	(803) 448-9411
Sanyo	OS-CON	Through Hole	(619) 661-6835
Sprague	595D	Surface Mount	(603) 224-1961

Diode Selection

A 2A Schottky diode such as Motorola MBRS130LT3 has been found to be the best available. Other choices include 1N5821 or MBRS130T3. Do not use "general purpose" diodes such as 1N4001. They are much too slow for use in switching regulator applications.

APPLICATIONS INFORMATION

Frequency Compensation

Obtaining proper RC values for the frequency compensation network is largely an empirical procedure, since variations in input and output voltage, topology, capacitor ESR and inductance make a simple formula elusive. As an example, consider the case of a 2.5V to 5V boost converter supplying 500mA. To determine optimum compensation, the circuit is built and a transient load is applied to the circuit. Figure 7 shows the setup.

In Figure 7a, the V_C pin is simply left floating. Although output voltage is maintained and transient response is good, switch current rises instantaneously to the internal current limit upon application of load. This is an undesirable situation as it places maximum stress on the switch and the other power components. Additionally, efficiency is well down from its optimal value. Next, a 0.1µF capacitor is connected with no resistor. Figure 7b details response. Although the circuit eventually stabilizes, the loop is quite underdamped. Initial output "sag" exceeds 5%. Aberrant behavior in the 4th graticule is the result of the LT1302's Burst Mode comparator turning off all switching as output voltage rises above its threshold.

In Figure 7c, the 0.1µF capacitor has been replaced by a 0.01µF unit. Undershoot is less but the response is still underdamped. Figure 7d shows the results of the 0.1µF capacitor and a 10k resistor in series. Now some amount of damping is observed, and behavior is more controlled. Figure 7e details response with a 0.01µF/10k series network. Undershoot is down to around 100mV, or 2%. A slight underdamping is still noticeable.

Finally, a 0.01µF/24k series network results in the response shown in Figure 7f. This has optimal damping, undershoot less than 100mV and settles in less than 1ms.

The V_C pin is sensitive to high frequency noise. Some layouts may inject enough noise to modulate peak switch current at 1/2 the switching frequency. A small capacitor connected from V_C to ground will eliminate this. Do not exceed 1/10 of the compensation capacitor value.

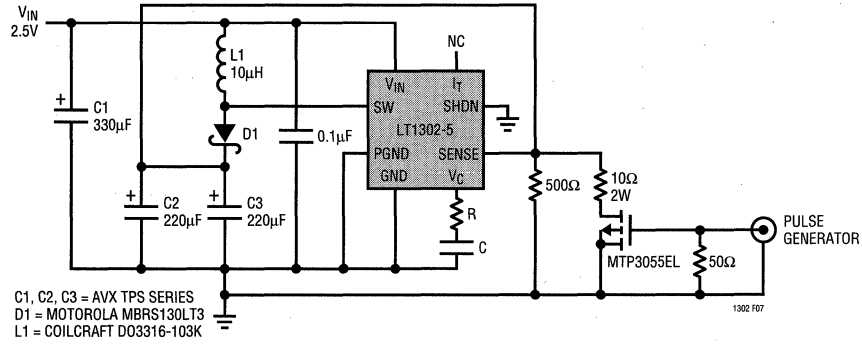


Figure 7. Boost Converter with Simulated Load

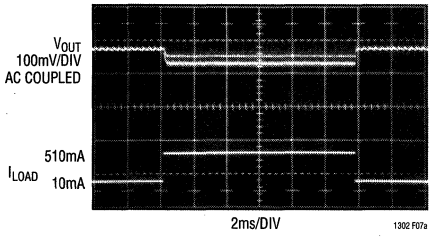


Figure 7a. V_C Pin Left Unconnected. Output Shows Low Frequency Components Under Load

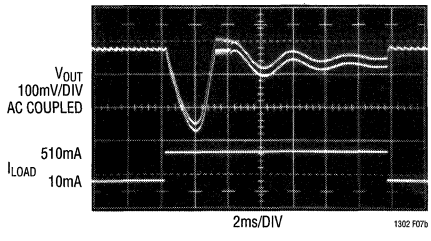


Figure 7b. 0.1µF from V_C to Ground. Better, but More Improvement Needed

APPLICATIONS INFORMATION

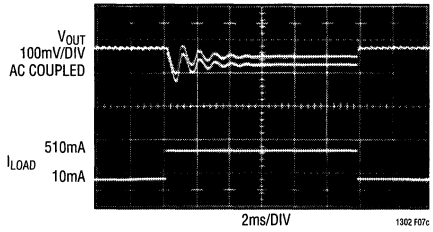


Figure 7c. 0.01μF from V_C to Ground. Underdamped Response Requires Series R

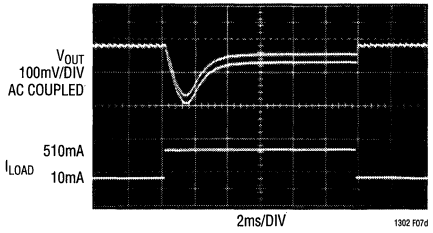


Figure 7d. 0.1μF with 10k Series RC. Classic Overdamped Response

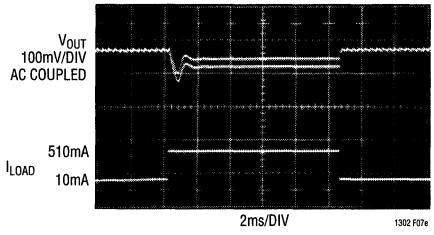


Figure 7e. 0.01μF, 10k Series RC Shows Good Transient Response. Slight Underdamping Still Noticeable

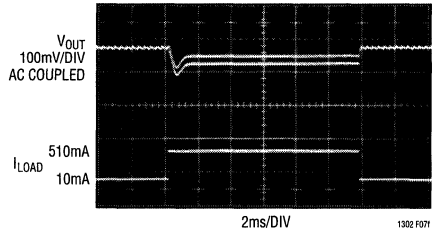


Figure 7f. 0.01μF, 24k Series RC Results in Optimum Response

I_T Pin

The I_T pin is used to disable Burst Mode, forcing the LT1302 to operate in current mode even at light load. To disable Burst Mode, 3.3k resistor R1 is connected from I_T to gound. More conservative frequency compensation must be used when in this mode. A 0.1μF capacitor and 4.7k resistor from V_C to ground has been found to be adequate. Low frequency Burst Mode ripple can be reduced or eliminated using this technique in many applications.

To illustrate, the transient load response of Figure 8's circuit is pictured without and with R1. Figure 8a shows output voltage and inductor current without the resistor. Note the 6kHz burst rate when the converter is delivering 25mA. By adding the 3.3k resistor, the low frequency bursting is eliminated, as shown in Figure 8b. This feature is useful in systems that contain audio circuitry. At very light or zero load, switching frequency drops and eventu-

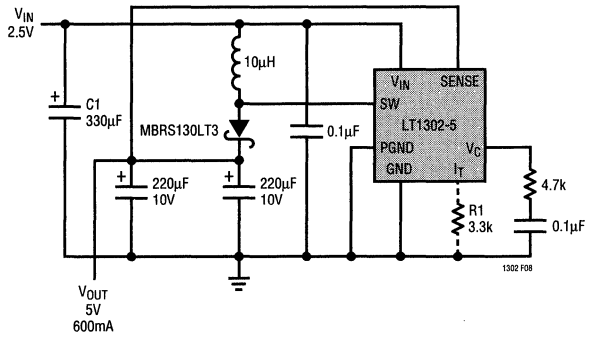


Figure 8. Addition of R1 Eliminates Low Frequency Output Ripple in This 2.5V to 5V Boost Converter

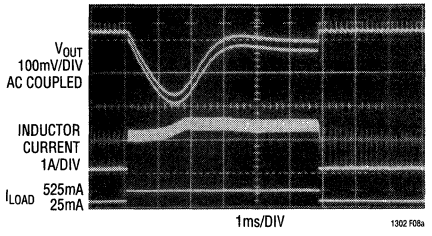


Figure 8a. I_T Pin Floating. Note 6kHz Burst Rate at I_{LOAD} = 25mA. 0.1μF/4.7k Compensation Network Causes 220mV Undershoot

APPLICATIONS INFORMATION

ally reaches audio frequencies, but at a much lighter load than without the I_T feature. At some input voltage/load current combinations, some residual bursting may occur at frequencies out of the audio band.

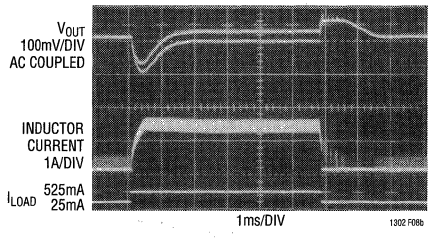


Figure 8b. 3.3k Resistor from I_T Pin to Ground Forces LT1302 into Current Mode Regardless of Load. Audio Frequency Component Eliminated

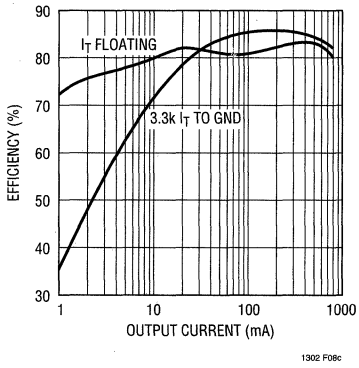


Figure 8c. 3.3k Resistor for I_T to Ground Increases Efficiency at Moderate Load, Decreases at Light Load

The I_T pin cannot be used as a soft-start. Large capacitors connected to the pin will cause erratic operation. If operating the device in Burst Mode, let the pin float. Keep high dV/dt signals away from the pin.

Figure 8c details efficiency with and without the addition of R1. Burst Mode operation keeps efficiency high at light load with I_T floating. Efficiency falls off at light load with R1 added because the LT1302 cannot transition into Burst Mode.

Layout

The high speed, high current switching associated with the LT1302 mandates careful attention to layout. Follow the suggested component placement in Figure 9 for proper operation. High current functions are separated by the package from sensitive control functions. Feedback resistors R1 and R2 should be close to the feedback pin (pin4). Noise can easily be coupled into this pin if care is not taken. A small capacitor (100pF to 200pF) from FB to ground provides a high frequency bypass. If the LT1302 is operated off a three-cell or higher input, R3 (2Ω to 10Ω) in series with V_{IN} is recommended. This isolates the device from noise spikes on the input supply. Do not put in R3 if the device must operate from a 2V input, as input current will cause the voltage at the LT1302's V_{IN} pin to go below 2V. The 0.1µF ceramic bypass capacitor C3 (use X7R, not Z5U) should be mounted as close as possible to the package. When R3 is used, C3 should be a 1µF tantalum unit. Grounding should be segregated as illustrated. C3's ground trace should not carry switch current. Run a

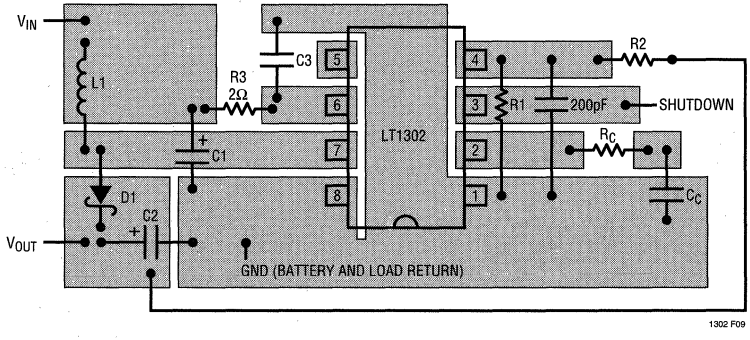


Figure 9. Suggested Component Placement for LT1302

APPLICATIONS INFORMATION

separate ground trace up under the package as shown. The battery and load return should go to the power side of the ground copper.

Thermal Considerations

The LT1302 contains a thermal shutdown feature which protects against excessive internal (junction) temperature. If the junction temperature of the device exceeds the protection threshold, the device will begin cycling between normal operation and an off state. The cycling is not harmful to the part. The thermal cycling occurs at a slow rate, typically 10ms to several seconds, which depends on the power dissipation and the thermal time constants of the package and heat sinking. Raising the ambient temperature until the device begins thermal shutdown gives a good indication of how much margin there is in the thermal design.

For surface mount devices heat sinking is accomplished by using the heat spreading capabilities of the PC board and its copper traces. Experiments have shown that the heat spreading copper layer does not need to be electrically connected to the tab of the device. The PCB material can be very effective at transmitting heat between the pad area attached to pins 1 and 8 of the device, and a ground or power plane layer either inside or on the opposite side of the board. Although the actual thermal resistance of the PCB material is high, the length/area ratio of the thermal resistance between the layer is small. Copper board stiffeners and plated through holes can also be used to spread the heat generated by the device.

Table 3 lists thermal resistance for the SO package. Measured values of thermal resistance for several different board sizes and copper areas are listed for each surface mount package. All measurements were taken in still air on 3/32" FR-4 board with 1oz copper. This data can be used as a rough guideline in estimating thermal resistance. The thermal resistance for each application will be affected by thermal interactions with other components as well as board size and shape.

Table 3. S8 Package, 8-Lead Plastic SO

COPPER AREA			THERMAL RESISTANCE
TOPSIDE*	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
2500 sq. mm	2500 sq. mm	2500 sq. mm	60°C/W
1000 sq. mm	2500 sq. mm	2500 sq. mm	62°C/W
225 sq. mm	2500 sq. mm	2500 sq. mm	65°C/W
100 sq. mm	2500 sq. mm	2500 sq. mm	69°C/W
100 sq. mm	1000 sq. mm	2500 sq. mm	73°C/W
100 sq. mm	225 sq. mm	2500 sq. mm	80°C/W
100 sq. mm	100 sq. mm	2500 sq. mm	83°C/W

* Pins 1 and 8 attached to topside copper
N8 Package, 8-Lead DIP:
Thermal Resistance (Junction-to-Ambient) = 100°C/W

Calculating Temperature Rise

Power dissipation internal to the LT1302 in a boost regulator configuration is approximately equal to:

$$P_D = I_{OUT}^2 R \left[\left(\frac{V_{OUT} + V_D}{V_{IN} - \frac{I_{OUT} V_{OUT} R}{V_{IN}}} \right)^2 - \left(\frac{V_{OUT} + V_D}{V_{IN} - \frac{I_{OUT} V_{OUT} R}{V_{IN}}} \right) \right] + \frac{I_{OUT}\left(V_{OUT} + V_D - V_{IN}\right)}{27}$$

The first term in this equation is due to switch "on-resistance." The second term is from the switch driver. R is switch resistance, typically 0.15Ω. V_D is the diode forward drop.

The temperature rise can be calculated from:

$$\Delta T = P_D \times \theta_{JA}$$

where:

ΔT = Temperature Rise
P_D = Device Power Dissipation
θ_{JA} = Thermal Resistance (Junction-to-Ambient)

APPLICATIONS INFORMATION

As an example, consider a boost converter with the following specifications:

V_{IN} = 3V

V_{OUT} = 6V

I_{OUT} = 700mA

Total power loss in the LT1302, assuming R = 0.15Ω and V_D = 0.45V, is:

$$P_D = (700mA)^2(0.15\Omega)\left[\left(\frac{6+0.45}{3-\frac{0.7\times 6\times 0.15}{3}}\right)^2 - \left(\frac{6+0.45}{3-\frac{0.7\times 6\times 0.15}{3}}\right)\right] + \frac{(0.7)(6+0.45-3)}{27}$$

$$= 223mW + 89mW = 312mW$$

Using the CS8 package with 100 sq. mm topside and backside heat sinking:

ΔT = (312mW)(84°C/W) = 25.9°C rise

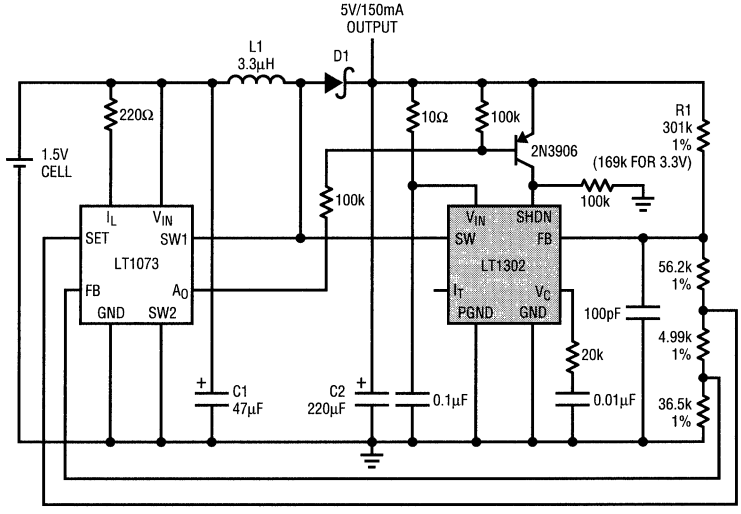
With the N8 package:

ΔT = 31.2°C

At a 70°C ambient, die temperature would be 101.2°C.

TYPICAL APPLICATIONS

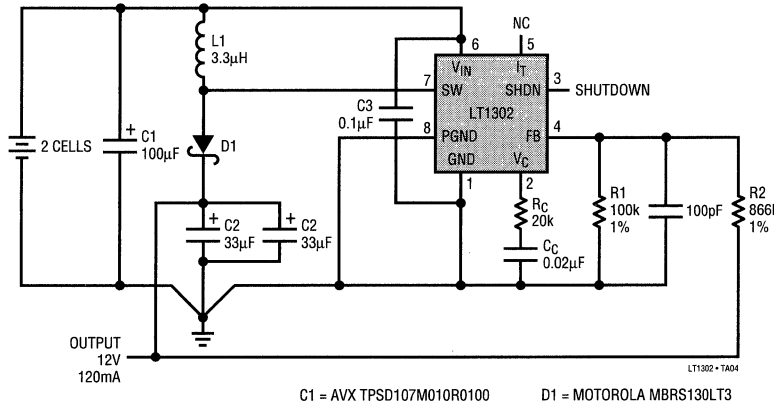
Single Cell to 5V/150mA Converter



L1 = COILCRAFT DO3316-332
D1 = MOTOROLA MBRS130LT3
C1 = AVX TPSD476M016R0150
C2 = AVX TPSE227M010R0100
COILCRAFT (708) 639-2361

1302 TA03

2V to 12V/120mA Converter

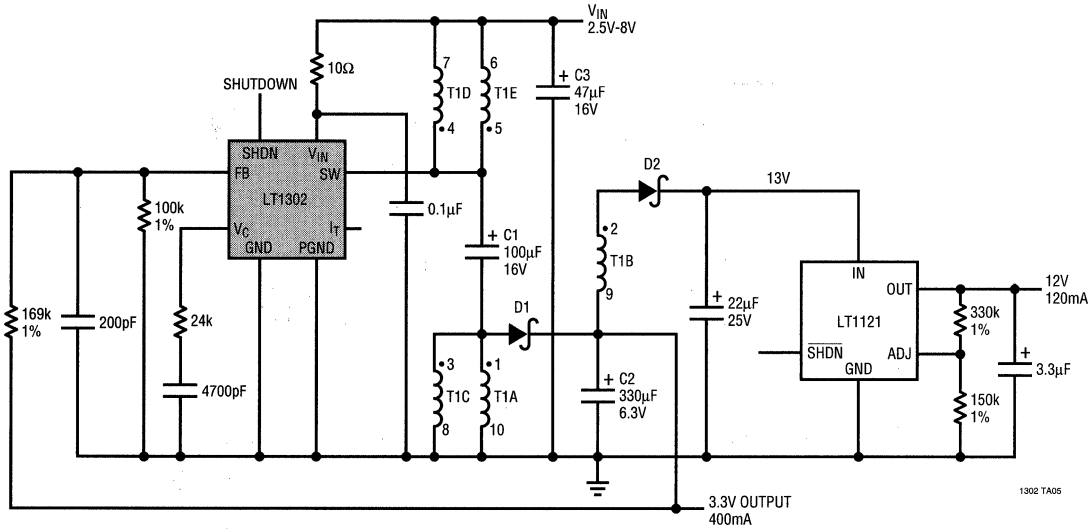


LT1302 • TA04

C1 = AVX TPSD107M010R0100
C2 = AVX TPSD336M025R0200
D1 = MOTOROLA MBRS130LT3
L1 = COILCRAFT DO3316-332

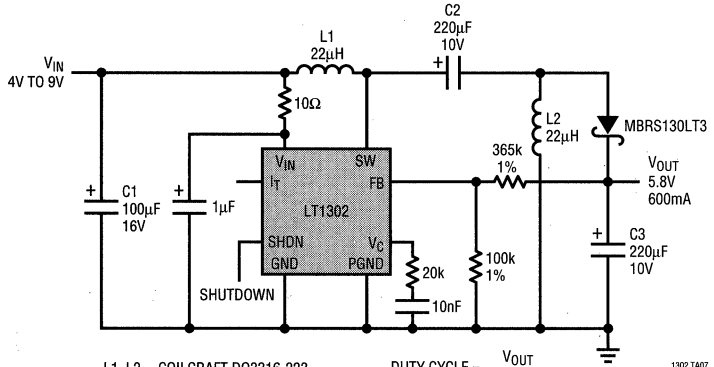
TYPICAL APPLICATIONS

3 Cell to 3.3V Buck-Boost Converter with Auxiliary 12V Regulated Output



T1 = DALE LPE-6562-A069, 1:3:1:1:1 TURNS RATIO, 10µH PRIMARY. DALE (605) 665-9301
D1, D2 = MOTOROLA MBRS130LT3
C1 = AVX TPSE107016R0100
C2 = AVX TPSE337006R0100
C3 = AVX TPSD476016R0150

2 Li-Ion Cell to 5.8V/600mA DC/DC Converter



L1, L2 = COILCRAFT DO3316-223
C1 = AVX TPSE107016R0100
C2, C3 = AVX TPSE227010R0100

DUTY CYCLE = $\frac{V_{OUT}}{V_{IN} + V_{OUT}}$

PEAK SWITCH VOLTAGE = $V_{IN} + V_{OUT}$

Micropower High Efficiency DC/DC Converters with Low-Battery Detector Adjustable and Fixed 5V

FEATURES

- **5V at 200mA from a 2V Input**
- Supply Voltage As Low As 1.8V
- Up to 88% Efficiency
- **120μA Quiescent Current**
- **Low-Battery Detector**
- Low V_{CESAT} Switch: 170mV at 1A Typ
- Uses Inexpensive Surface Mount Inductors
- 8-Lead PDIP or SO Package

APPLICATIONS

- EL Panel Drivers
- 2-Cell and 3-Cell to 5V Conversion
- Palmtop Computers
- Portable Instruments
- Bar-Code Scanners
- PDAs
- Wireless Systems

DESCRIPTION

The LT®1303/LT1303-5 are micropower step-up high efficiency DC/DC converters using Burst Mode™ operation. They are ideal for use in small, low-voltage battery-operated systems. The LT1303-5 accepts an input voltage between 1.8V and 5V and converts it to a regulated 5V. The LT1303 is an adjustable version that can supply an output voltage up to 25V. Quiescent current is only 120μA from the battery and the shutdown pin further reduces current to 10μA. The low-battery detector provides an open-collector output that goes low when the input voltage drops below a preset level. The on-chip NPN power switch has a low 170mV saturation voltage at a switch current of 1A. The LT1303/LT1303-5 are available in 8-lead PDIP or SO packages, easing board space requirements.

For higher output current, please see the LT1305 or LT1302.

LT, LTC and LT are registered trademarks of Linear Technology Corporation.
Burst Mode is a trademark of Linear Technology Corporation.

4

TYPICAL APPLICATION

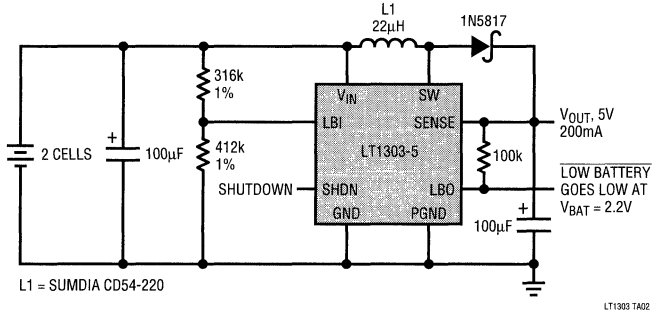
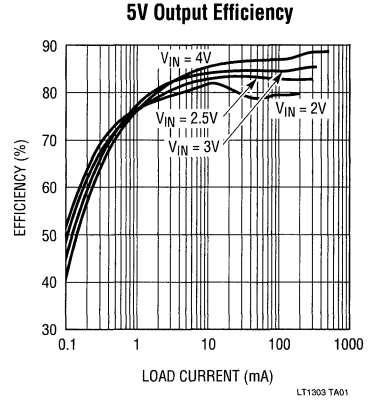


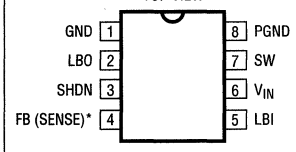
Figure 1. 2-Cell to 5V DC/DC Converter with Low-Battery Detect



ABSOLUTE MAXIMUM RATINGS

V_{IN} Voltage 10V
SW1 Voltage 25V
Sense Voltage (LT1303-5) 20V
FB Voltage (LT1303) 10V
Shutdown Voltage 10V
LBO Voltage 10V
LBI Voltage 10V
Maximum Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

*FIXED VERSION

T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 100°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LT1303CN8 LT1303CS8 LT1303CN8-5 LT1303CS8-5
S8 PART MARKING
1303 13035

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 2.0V, unless otherwise noted.

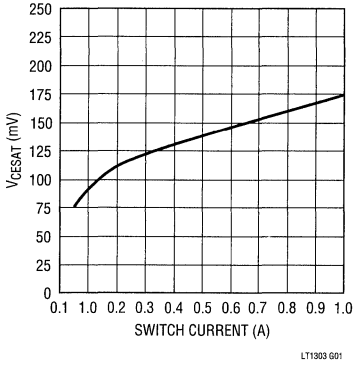
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	V_{SHDN} = 0.5V, V_{SEL} = 5V, V_{SENSE} = 5.5V	●		120	200	µA
		V_{SHDN} = 1.8V	●		7	15	µA
V_{IN}	Input Voltage Range			1.8	1.55		V
			●	2.0			V
	Feedback Voltage	LT1303	●	1.22	1.24	1.26	V
	Output Sense Voltage	LT1303-5	●	4.8	5.0	5.2	V
	Comparator Hysteresis	LT1303 (Note 1)	●		6	12.5	mV
	Output Hysteresis	LT1303-5 (Note 1)	●		22	50	mV
	Feedback Pin Bias Current	LT1303, V_{FB} = 1V	●		7	20	nA
	Oscillator Frequency	Current Limit Not Asserted		120	155	185	kHz
	Oscillator TC				0.2		%/°C
DC	Maximum Duty Cycle		●	75	86	95	%
t_{ON}	Switch On Time	Current Limit Not Asserted			5.6		µs
	Output Line Regulation	1.8V < V_{IN} < 6V	●		0.06	0.15	%/V
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 700mA	●		130	200	mV
	Switch Leakage Current	V_{SW} = 5V, Switch Off	●		0.1	10	µA
	Peak Switch Current	V_{IN} = 2V	●	0.75	1.0	1.25	A
		V_{IN} = 5V		0.65	0.9	1.15	A
	LBI Trip Voltage		●	1.21	1.24	1.27	V
	LBI Input Bias Current	V_{LBI} = 1V	●		7	20	nA
	LBO Output Low	I_{LOAD} = 100µA	●		0.11	0.4	V
	LBO Leakage Current	V_{LBI} = 1.3V, V_{LBO} = 5V	●		0.1	5	µA
V_{SHDNH}	Shutdown Pin High		●	1.8			V
V_{SHDNL}	Shutdown Pin Low					0.5	V
I_{SHDN}	Shutdown Pin Bias Current	V_{SHDN} = 5V	●		8.0	20	µA
		V_{SHDN} = 2V	●		3.0		µA
		V_{SHDN} = 0V	●		0.1	1	µA

The ● denotes specifications which apply over the 0°C to 70°C operating temperature range.

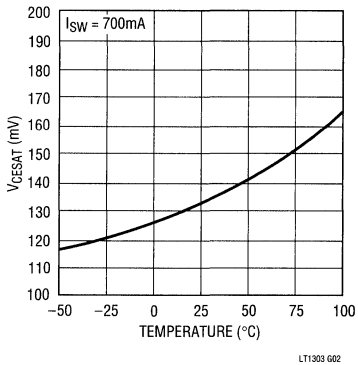
Note 1: Hysteresis specified is DC. Output ripple may be higher if output capacitance is insufficient or capacitor ESR is excessive.

TYPICAL PERFORMANCE CHARACTERISTICS

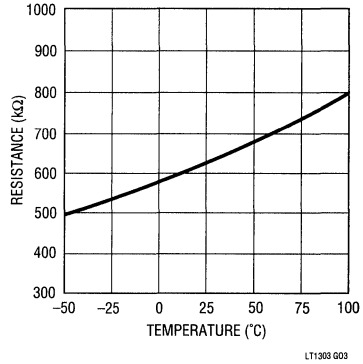
V_{CESAT} vs Switch Current



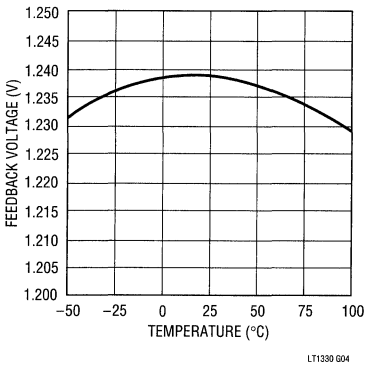
V_{CESAT} vs Temperature



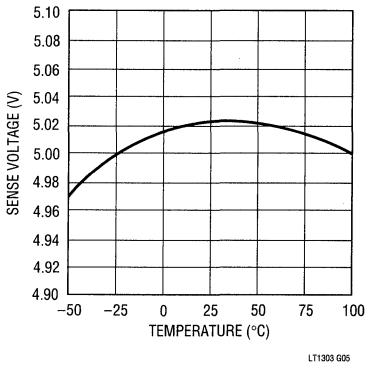
LT1303-5 Sense Pin Resistance to Ground



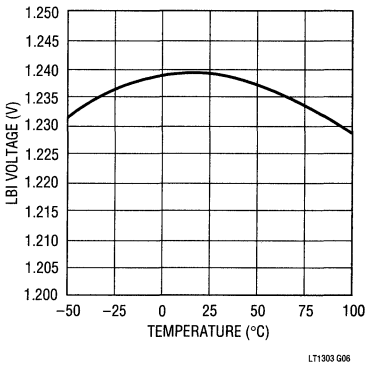
LT1303 FB Voltage



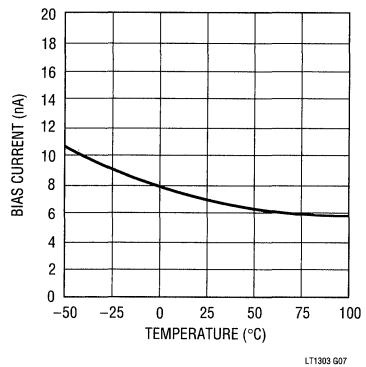
LT1303-5 Sense Voltage



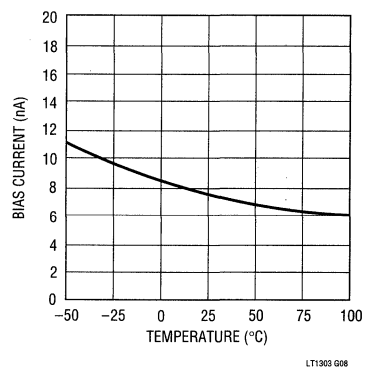
Low Battery Detect Trip Point



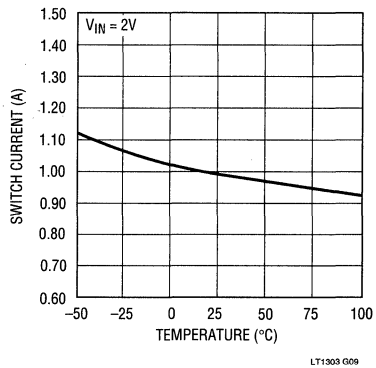
LBI Pin Bias Current



FB Pin Bias Current



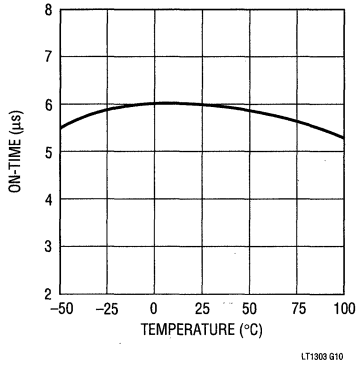
Switch Current Limit



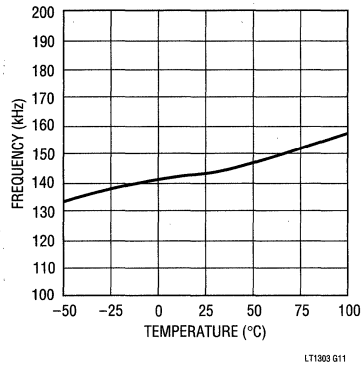
4

TYPICAL PERFORMANCE CHARACTERISTICS

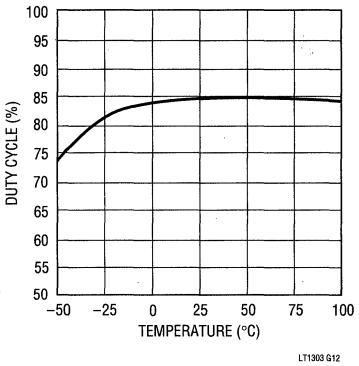
Switch On-Time



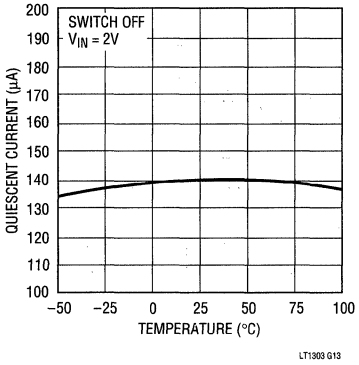
Oscillator Frequency



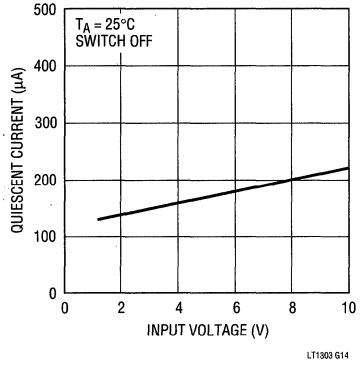
Maximum Duty Cycle



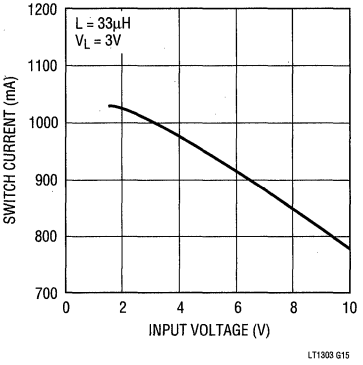
Quiescent Current



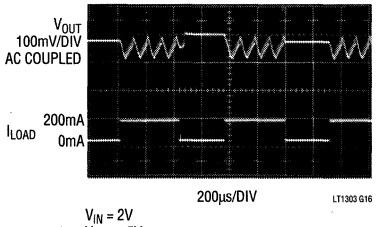
Quiescent Current



Switch Current Limit

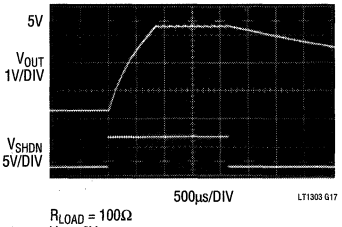


Transient Response
Figure 1 Circuit



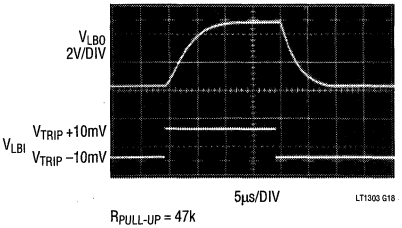
VIN = 2V
VOUT = 5V

Shutdown Pin Response



RLOAD = 100Ω
VIN = 2V
VOUT = 5V
COUT = 100µF

Low Battery Detector Transient Response



RPULL-UP = 47k

PIN FUNCTIONS

GND (Pin 1): Signal Ground. Tie to PGND under the package.

LBO (Pin 2): Open-Collector Output of Low-Battery Comparator. Can sink 100µA. Disabled when device is in shutdown.

SHDN (Pin 3): Shutdown. Pull high to shut down the device. Ground for normal operation.

FB/Sense (Pin 4): On 1303 (adjustable) this pin connects to the main comparator C1 input. On LT1303-5 this pin connects to the resistor string that sets output voltage at 5V.

LBI (Pin 5): Low-Battery Comparator Input. When voltage on this pin below 1.24V, LBO is low.

V_{IN} (Pin 6): Supply Pin. Must be bypassed with a large value electrolytic to ground. Keep bypass within 0.2" of the device.

SW (Pin 7): Switch Pin. Connect inductor and diode here. Keep layout short and direct to minimize radio frequency interference.

PGND (Pin 8): Power ground. Tie to signal ground (pin1) under the package. Bypass capacitor from V_{IN} should be tied directly to PGND within 0.2" of the device.

BLOCK DIAGRAMS

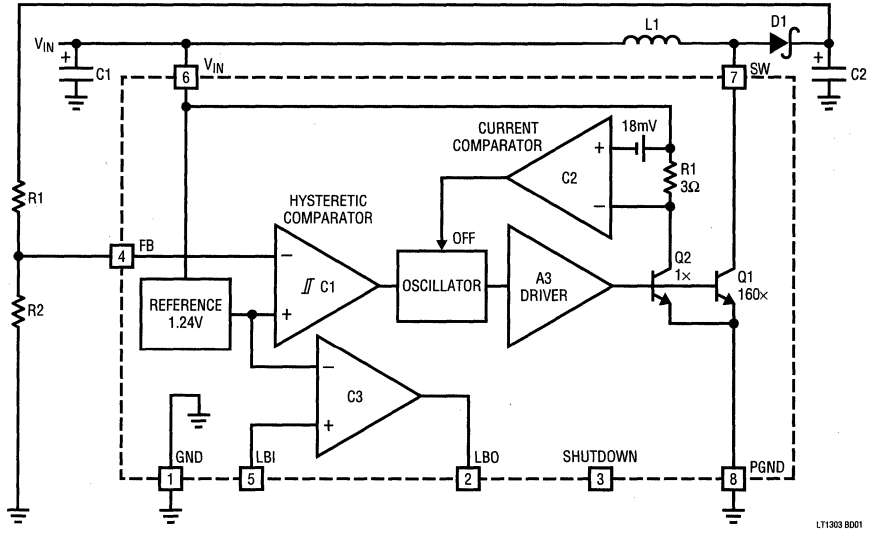


Figure 2. LT1303 Block Digram

BLOCK DIAGRAMS

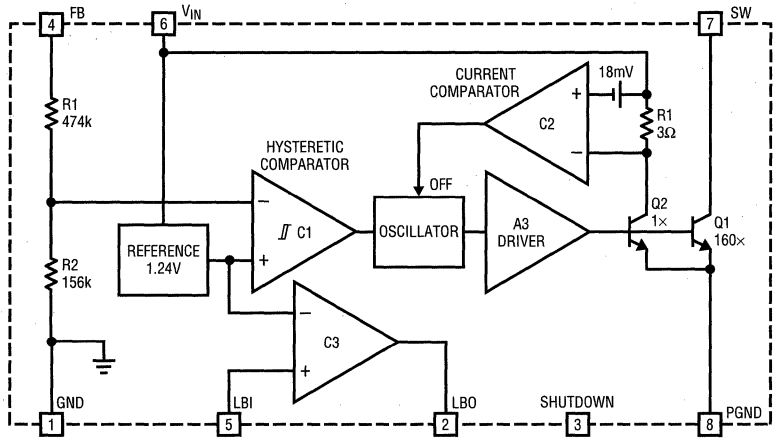


Figure 3. LT1303-5 Block Diagram

OPERATION

Operation of the LT1303 is best understood by referring to the Block Diagram in Figure 2. When C1's negative input, related to the output voltage by the appropriate resistor-divider ratio, is higher than the 1.24V reference voltage, C1's output is low. C2, A3 and the oscillator are turned off, drawing no current. Only the reference and C1 consume current, typically 140μA. When C1's negative input drops below 1.24V and overcomes C1's 6mV hysteresis, C1's output goes high, enabling the oscillator, current comparator C2 and driver A3. Quiescent current increases to 2mA as the device goes into active switching mode. Q1 then turns on in controlled saturation for nominally 6μs or until current comparator C2 trips, whichever comes first. The switch then turns off for approximately 1.5μs, then turns on again. The LT1303's switching causes current to alternately build up in L1 and dump into output capacitor C4 via D1, increasing the output voltage. When the output is high enough to cause C1's output to go high, switching action ceases. Capacitor C4 is left to supply current to the load until V_{OUT} decreases enough to force C1's output high, and the entire cycle repeats. Figure 4 details relevant waveforms. C1's cycling causes low-to-mid-frequency ripple voltage on the output. Ripple can be reduced by making the output capacitor large. The 100μF unit specified results in ripple of 50mV to 100mV on the 5V output. A 220μF capacitor will decrease ripple by approximately 50%.

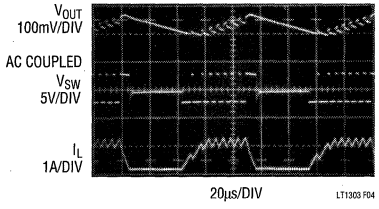


Figure 4. Burst Mode Operation in Action

If switch current reaches 1A, causing C2 to trip, switch on-time is reduced and off-time increases slightly. This allows continuous operation during bursts. C2 monitors the voltage across 3Ω resistor R1 which is directly related to the switch current. Q2's collector current is set by the emitter-area ratio to 0.6% of Q1's collector current. When R1's voltage drop exceeds 18mV, corresponding to 1A switch current, C2's output goes high, truncating the on-time portion of the oscillator cycle and increasing off-time

OPERATION

to about 2µs. Response time of C2, which determines minimum on-time, is approximately 300ns.

Low Battery Detector

The low battery detector is enabled when SHDN is low and disabled when SHDN is high. The comparator has no hysteresis built in, but hysteresis can be added by connecting a high-value resistor from LBI to LBO as shown in Figure 5. The internal reference can be accessed via the comparator as shown in Figure 6.

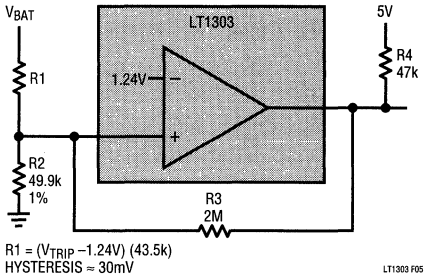


Figure 5. R3 Adds Hysteresis to Low-Battery Detector

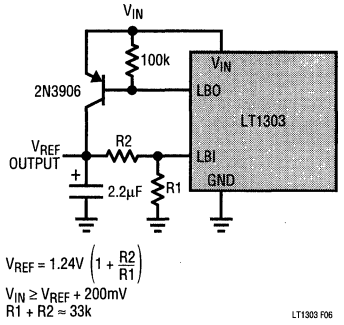


Figure 6. Accessing Internal Reference

4

APPLICATIONS INFORMATION

Inductor Section

Inductors suitable for use with the LT1303 usually fall in the 5µH to 50µH range. The inductor must: (1) handle current of 1.25A without saturating, (2) have enough inductance to provide a di/dt lower than 400mA/µs, and (3) have low enough DC resistance to avoid excessive heating or efficiency losses. Higher value inductors will deliver more power but tend to be physically larger. Most ferrite core drum or rod inductors such as those specified in Table 1 are suitable for use. It is acceptable to bias open-flux inductors (e.g. Sumida CD54) into saturation by 10 to 20% without adverse effects.

Table 1. Recommended Inductors

VENDOR	SERIES	APPROPRIATE VALUES	PHONE NUMBERS
Coilcraft	D03316 D01608	10µH to 47µH 10µH	(708) 639-6400
Coiltronics	OCTAPAK CTX20-1 CTX20-2 CTX33-4	 20µH 20µH 33µH	(407) 241-7876
Sumida	CD54	10µH to 33µH	(708) 956-0666
Gowanda	GA10	10µH to 33µH	(716) 532-2234

Figure 7 shows inductor current of a suitable inductor, di/dt is controlled at all times. The rapid rise in current shown in Figure 8 results from this inductor saturating at approximately 1A. Saturation occurs when the inductor cannot hold any more magnetic energy in the core. Current then increases rapidly, limited only by the resistance of the winding. Figure 9's inductor has high DC resistance which results in the exponential time constant shape of the inductor current.

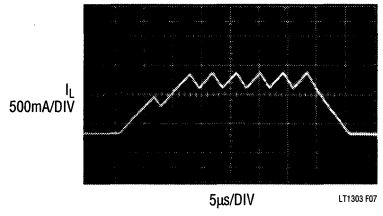


Figure 7. Properly Chosen Inductor Does Not Saturate

APPLICATIONS INFORMATION

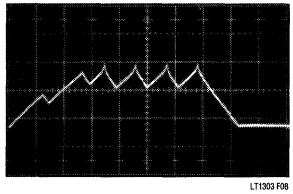


Figure 8. This Inductor Saturates at $I_L \approx 1A$. A Poor Choice

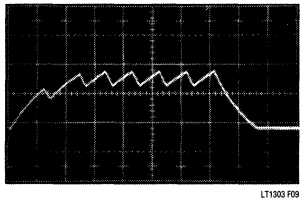


Figure 9. Slight Exponential Shape to Inductor Current Waveform Indicates Excessive DC Resistance

Diode Selection

The LT1303's high switching speed demands a high speed rectifier. Schottky diodes are preferred for their low forward drop and fast recovery. Suitable choices include the 1N5817, MBRS120LT3, and MBR0520LT1. Do not use signal diodes such as 1N4148. They cannot carry 1A current. Also avoid "general-purpose" diodes such as 1N4001. These are far too slow and are unsuitable for any switching regulator application. For high temperature applications a silicon diode such as the MUR105 will have less leakage.

Capacitor Selection

Input and output capacitors should have low ESR for best efficiency. Recommended capacitors include AVX TPS series, Sprague 595D series, and Sanyo OS-CON. The output capacitor's ESR determines the high frequency ripple amplitude. A 100µF capacitor is the minimum recommended for a 5V output. Higher output voltages can use lower capacitance values. For example, a 12V output can use a 33µF or 47µF capacitor. The V_{IN} pin of the LT1303 should be decoupled with a 47µF or 100µF capacitor at the pin. When driving a transformer, an additional decoupling network of 10Ω and 0.1µF ceramic is recommended as shown in Figure 10.

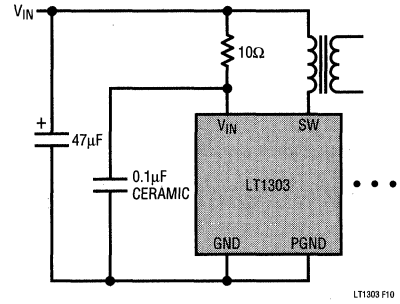


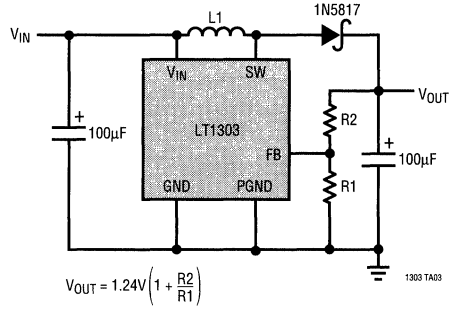
Figure 10. 10Ω-1µF Network to LT1303 V_{IN} Pin Provides Additional Decoupling. Recommended When Driving Transformers.

Table 2. Recommended Capacitors

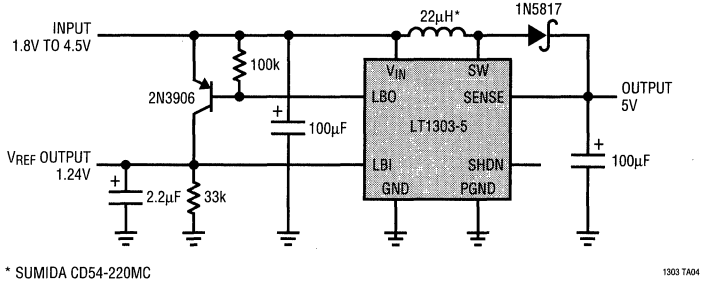
VENDOR	SERIES	TYPE	PHONE NUMBERS
AVX	TPS	Surface Mount	(803) 448-9411
Sanyo	OS-CON	Through-Hole	(619) 661-6835
Panasonic	HFQ	Through-Hole	(201) 348-5200
Sprague	595D	Surface Mount	(603) 224-1961

TYPICAL APPLICATIONS

Setting Output Voltage on LT1303

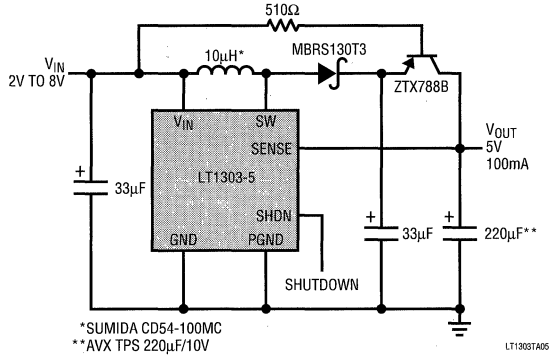


5V Step-Up Converter with Reference Output

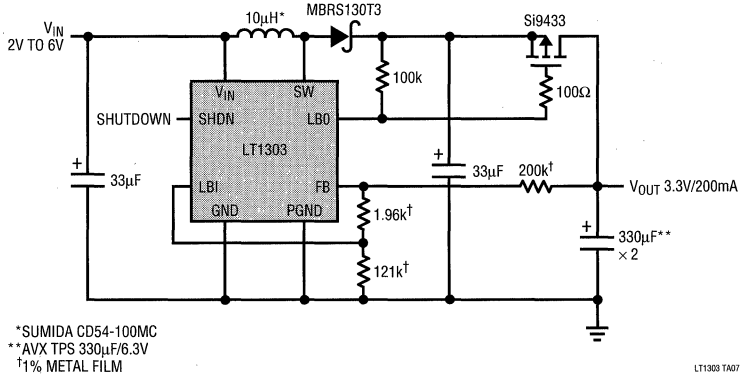


TYPICAL APPLICATIONS

4-, 5-Cell to 5V Converter with Output Disconnect

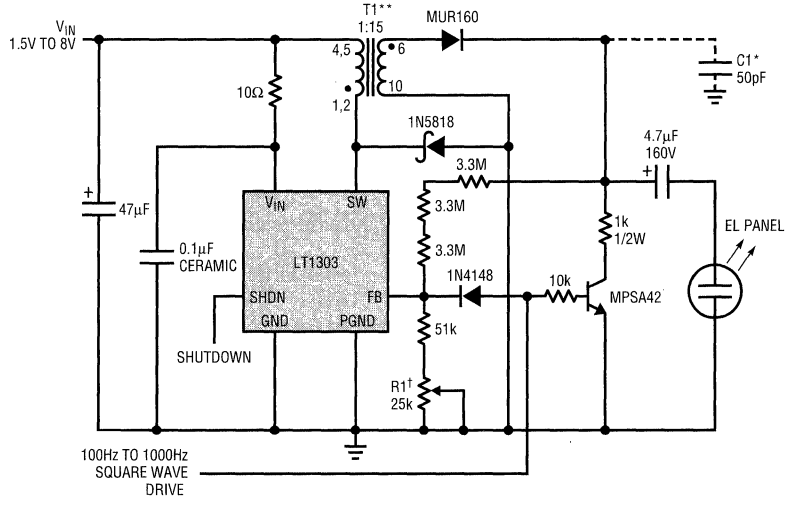


3-Cell to 3.3V Boost/Linear Converter with Output Disconnect



TYPICAL APPLICATIONS

EL Panel Driver



*ADD C1 FOR OPEN-PANEL PROTECTION
**DALE LPE5047-A132 1:15 TURNS RATIO (605) 666-9301
†R1 ADJUSTS V_{OUT} $83V_{RMS}$ TO $115V_{RMS}$

LT1303 TA06

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1129	Micropower Low Dropout Regulator	700mA Output Current in SO-8 Package
LT1182/83/84	LCD and CCFL Backlight Controller	High Efficiency and Excellent Backlight Control Range
LT1301	5V to 12V/200mA Step-Up DC/DC Converter	120µA Quiescent Current
LT1302	2-Cell to 5V/600mA Step-Up DC/DC Converter	200µA Quiescent Current
LT1305	Micropower 2A Switch DC/DC Converter with Low-Battery Detect	2V to 5V at 400mA
LT1372	500kHz Step-Up PWM, 1.5A Switch	Low Noise, Fixed Frequency Operation
LTC®1472	PCMCIA Host Switch with Protection	Includes Current Limit and Thermal Shutdown

Micropower High Power DC/DC Converter with Low-Battery Detector

FEATURES

- **5V at 400mA from 2V Input**
- Supply Voltage As Low As 1.8V
- 120μA Quiescent Current
- **Low-Battery Detector**
- **Low V_{CESAT} Switch: 310mV at 2A Typ**
- Uses Inexpensive Surface Mount Inductors
- 8-Lead SO Package

APPLICATIONS

- 2-Cell and 3-Cell to 5V Conversion
- EL Panel Drivers
- Portable Instruments

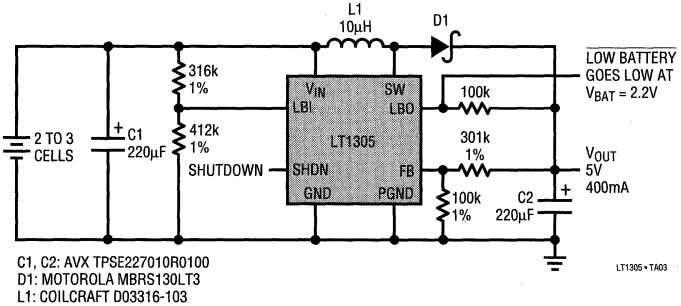
DESCRIPTION

The LT®1305 is a micropower step-up DC/DC converter that uses Burst Mode™ operation. Similar to the LT1303, the LT1305 features a 2A internal low-loss switch and can deliver up to four times the output power of the LT1303.

Quiescent current is only 120μA and the Shutdown pin further reduces current to 10μA. A low-battery detector provides an open-collector output that goes low when the input voltage drops below a preset level. The LT1305 is available in an 8-pin SO, easing board space requirements.

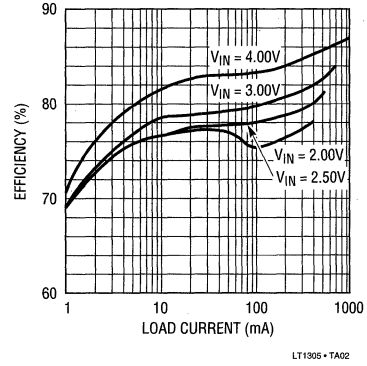
TYPICAL APPLICATION

2-Cell and 3-Cell to 5V/400mA DC/DC Converter with Low-Battery Detect



C1, C2: AVX TPSE227010R0100
D1: MOTOROLA MBRS130LT3
L1: COILCRAFT D03316-103

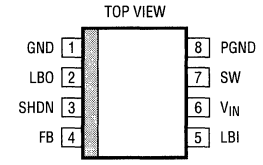
Efficiency



ABSOLUTE MAXIMUM RATINGS

V_{IN} Voltage 10V
SW1 Voltage 25V
FB Voltage 10V
Shutdown Voltage 10V
LBO Voltage 10V
LBI Voltage 10V
Maximum Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 80°C/W

ORDER PART NUMBER
LT1305CS8
S8 PART MARKING
1305

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 2.0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	V_{SHDN} = 0.5V, V_{FB} = 2V	●		120	200	µA
		V_{SHDN} = 1.8V	●		7	15	µA
V_{IN}	Input Voltage Range			1.8	1.55		V
			●	2.0			V
	Feedback Voltage		●	1.22	1.24	1.26	V
	Comparator Hysteresis		●		6	12.5	mV
	Feedback Pin Bias Current	V_{FB} = 1V	●		7	20	nA
	Oscillator Frequency	Current Limit Not Asserted		120	155	185	kHz
	Oscillator TC				0.2		%/°C
DC	Maximum Duty Cycle		●	75	86	95	%
t_{ON}	Switch On Time	Current Limit Not Asserted			5.6		µs
	Output Line Regulation	1.8V < V_{IN} < 6V	●		0.06	0.15	%/V
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 1A	●		140	280	mV
	Switch Leakage Current	V_{SW} = 5V, Switch Off	●		0.1	10	µA
	Peak Switch Current	V_{IN} = 2V		1.35	2	2.35	A
			●	1.20		2.50	A
		V_{IN} = 5V		1.15		2.15	A
	LBI Trip Voltage	(Note 2)	●	1.21	1.24	1.27	V
	LBI Input Bias Current	V_{LBI} = 1V	●		7	20	nA
	LBO Output Low	I_{LOAD} = 100µA	●		0.11	0.4	V
	LBO Leakage Current	V_{LBI} = 1.3V, V_{LBO} = 5V	●		0.1	5	µA
V_{SHDNH}	Shutdown Pin High		●	1.8			V
V_{SHDNL}	Shutdown Pin Low					0.5	V
I_{SHDN}	Shutdown Pin Bias Current	V_{SHDN} = 5V	●		8.0	20	µA
		V_{SHDN} = 2V	●		3.0		µA
		V_{SHDN} = 0V	●		0.1	1	µA

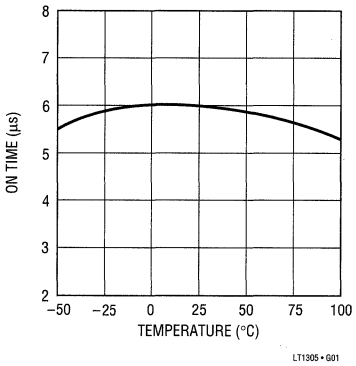
The ● denotes specifications which apply over the 0°C to 70°C operating temperature range.

Note 1: Hysteresis specified is DC. Output ripple may be higher if output capacitance is insufficient or capacitor ESR is excessive.

Note 2: Low-battery detector comparator is inoperative when device is in shutdown.

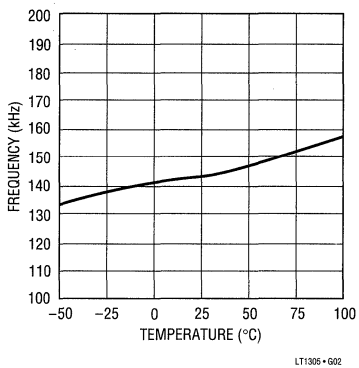
TYPICAL PERFORMANCE CHARACTERISTICS

Switch On Time



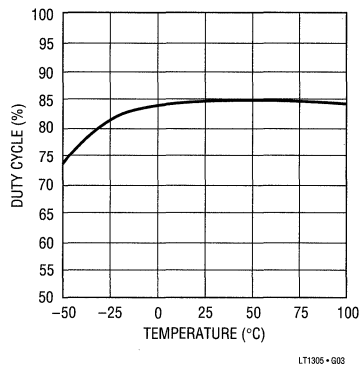
LT1305 • G01

Oscillator Frequency



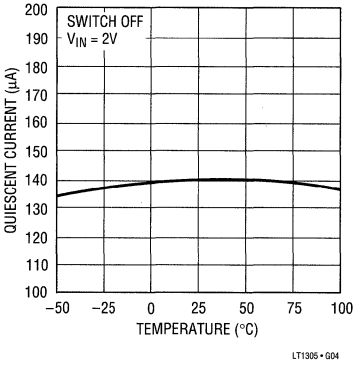
LT1305 • G02

Maximum Duty Cycle



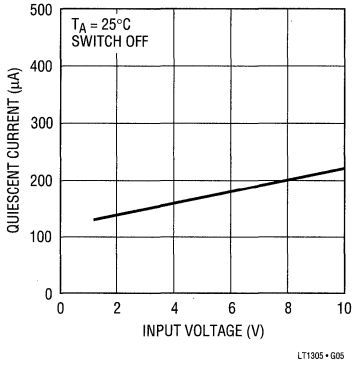
LT1305 • G03

Quiescent Current



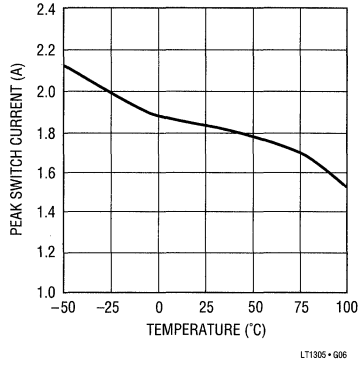
LT1305 • G04

Quiescent Current



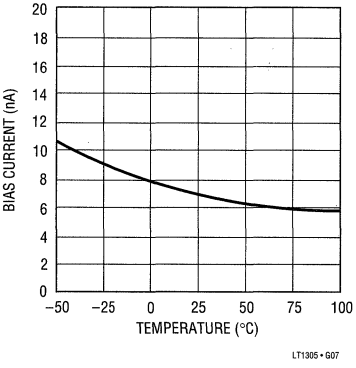
LT1305 • G05

Current Limit



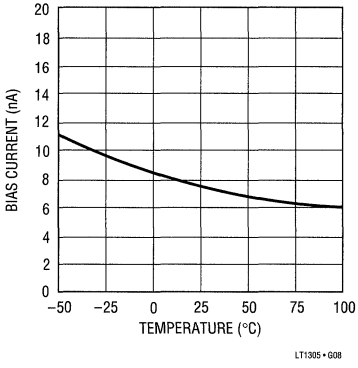
LT1305 • G06

LBI Pin Bias Current



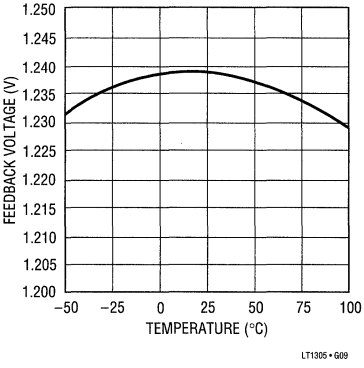
LT1305 • G07

FB Pin Bias Current



LT1305 • G08

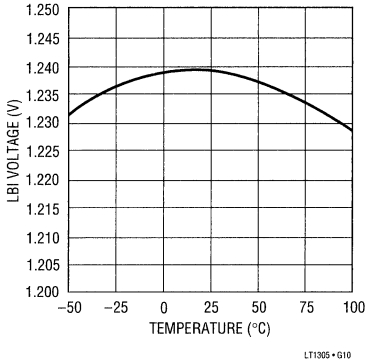
FB Voltage



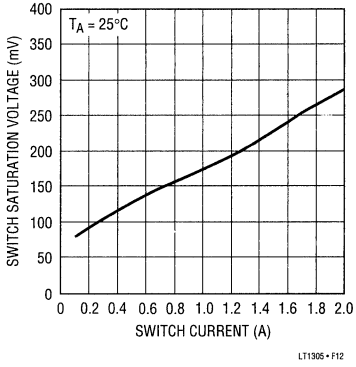
LT1305 • G09

TYPICAL PERFORMANCE CHARACTERISTICS

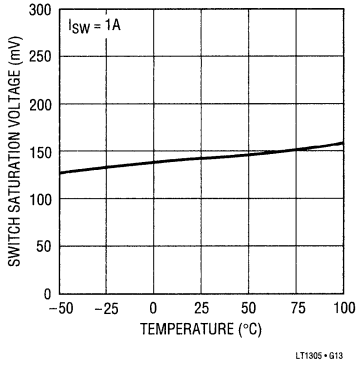
Low-Battery Detect Trip Point



Switch Saturation Voltage



Switch Saturation Voltage



PIN FUNCTIONS

GND (Pin 1): Signal Ground. Tie to PGND under the package.

LBO (Pin 2): Open-Collector Output of Comparator C3. Can sink 100µA. High impedance when device is in shutdown.

SHDN (Pin 3): Shutdown. Pull high to shut down the LT1305. Ground for normal operation.

FB (Pin 4): Feedback Input. Connects to main comparator C1 input.

LBI (Pin 5): Low-Battery Comparator Input. When voltage on this pin is below 1.24V, LBO is low.

V_{IN} (Pin 6): Supply Pin. Must be bypassed with a large value capacitor to gound. Keep bypass within 0.2" of the device.

SW (Pin 7): Switch Pin. Connect inductor and diode here. Keep layout short and direct to minimize radio frequency interference.

PGND (Pin 8): Power Ground. Tie to signal ground (pin 1) under the package. Bypass capacitor from V_{IN} should be tied directly to PGND within 0.2" of the device.

BLOCK DIAGRAM

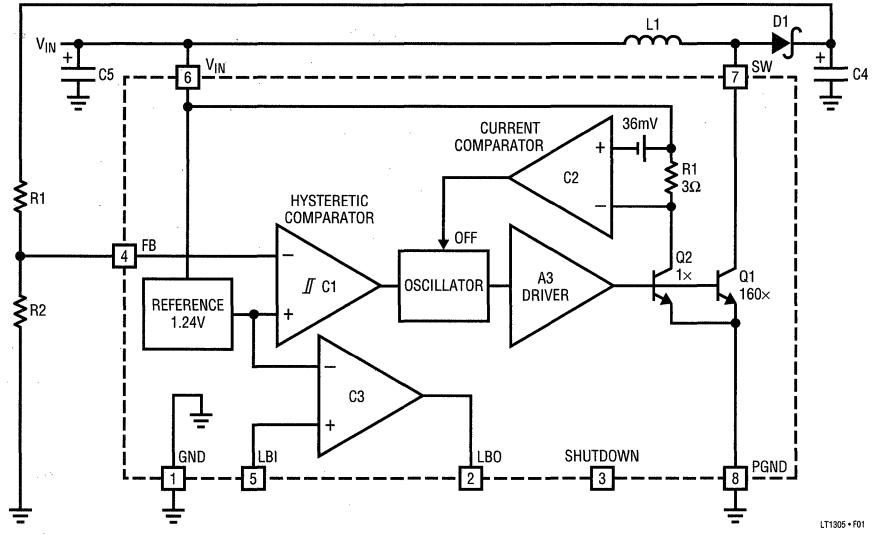


Figure 1. LT1305 Block Diagram

OPERATION

Operation of the LT1305 is best understood by referring to the Block Diagram in Figure 1. When C1's negative input, related to the output voltage by the appropriate resistor-divider ratio, is higher than the 1.24V reference voltage, C1's output is low. C2, A3 and the oscillator are turned off, drawing no current. Only the reference and C1 consume current, typically 120μA. When C1's negative input drops below 1.24V and overcomes C1's 6mV hysteresis, C1's output goes high, enabling the oscillator, current comparator C2 and driver A3. Quiescent current increases to 2mA as the device goes into active switching mode. Q1 then turns on in controlled saturation for nominally 6μs or until current comparator C2 trips, whichever comes first. The switch then turns off for approximately 1.5μs, then turns on again. The LT1305's switching causes current to alternately build up in L1 and dump into output capacitor C4 via D1, increasing the output voltage. When the output is high enough to cause C1's output to go high, switching action ceases. Capacitor C4 is left to supply current to the load until V_{OUT} decreases enough to force C1's output high, and the entire cycle repeats. Figure 2 details relevant waveforms. C1's cycling causes low-to-mid-frequency ripple voltage on the output. Ripple can be reduced by making the output capacitor large. The 220μF unit specified results in ripple of 50mV to 100mV on the 5V output. Paralleling two capacitors will decrease ripple by approximately 50%.

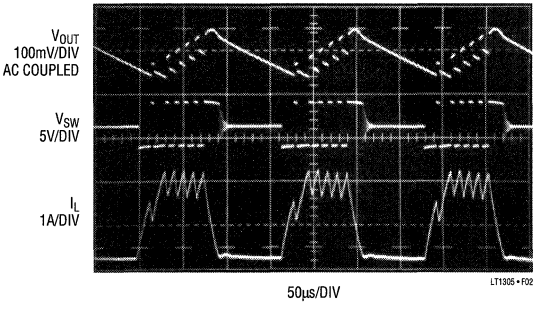


Figure 2. Burst Mode Operation

OPERATION

If switch current reaches 2A, causing C2 to trip, switch on time is reduced and off time increases slightly. This allows continuous operation during bursts. C2 monitors the voltage across 3Ω resistor R1 which is directly related to the switch current. Q2's collector current is set by the emitter-area ratio to 0.6% of Q1's collector current. When R1's voltage drop exceeds 36mV, corresponding to 2A switch current, C2's output goes high, truncating the on time portion of the oscillator cycle and increasing off time to about 2μs. Response time of C2, which determines minimum on time, is approximately 300ns.

Low-Battery Detector

The low-battery detector is enabled when SHDN is low and disabled when SHDN is high. The comparator has no hysteresis built in, but hysteresis can be added by connecting a high-value resistor from LBI to LBO as shown in Figure 3. The internal reference can be accessed via the comparator as shown in Figure 4.

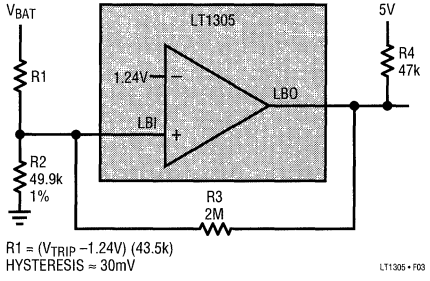


Figure 3. R3 Adds Hysteresis to Low-Battery Detector

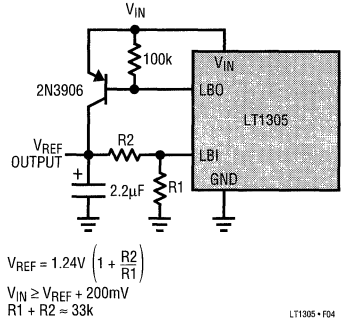


Figure 4. Accessing Internal Reference

Inductor Selection

Inductors used with the LT1305 must fulfill two requirements. First, the inductor must be able to handle current of 2A to 2.5A without runaway saturation. Rod or drum core units usually saturate gradually and it is acceptable to exceed manufacturer's published saturation current by 20% or so. Second, the unit must have low DCR, under 0.05Ω so that copper loss is kept low and excess heating is avoided. Inductance value is not critical. Generally, for low voltage inputs below 3V a 10μH inductor is recommended (such as Coilcraft DO3316-103). For inputs above 4V to 5V use a 22μH unit (such as Coilcraft DO3316-223). Switching frequency can reach up to 300kHz so the core material should be able to operate at high frequency without excessive core loss. Ferrite or molypermalloy cores are a better choice than powdered iron. If EMI is a concern, a toroidal inductor is suggested, such as Coiltronics CTX20-4.

Capacitor Selection

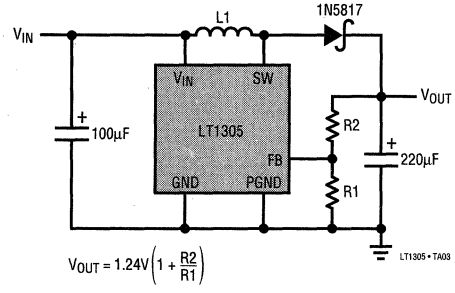
Output and input capacitors should have low ESR for best performance. Inexpensive aluminum electrolytics sometimes have ESR above 1Ω, even for relatively large values such as 100μF, 16V units. Since the LT1305 has a 2A current limit, 2V of ripple voltage would result with such a capacitor at the output. Keep ESR below 0.05Ω to 0.1Ω for reasonable ripple voltage. Tantalum capacitors such as AVX TPS series or Sprague 593D have low ESR and are surface mount components. For lowest ESR, use Sanyo OS-CON units (OS-CON is also available from Vishay). These capacitors have superior ESR, small size and perform well at cold temperatures.

Diode Selection

A 2A Schottky diode such as Motorola MBRS130LT3 is a good choice for the rectifier diode. A 1N5821 or MBRS130T3 are suitable as well. Do not use "general purpose" diodes such as 1N4001. They are much too slow for use in switching regulator applications.

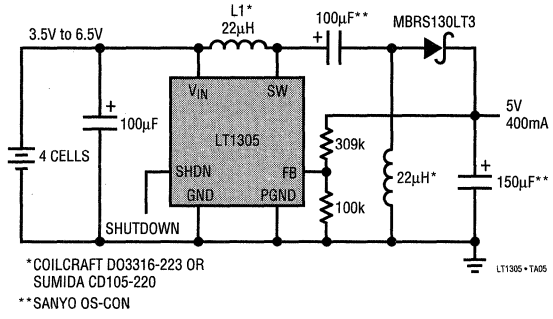
TYPICAL APPLICATIONS

Setting Output Voltage



$$V_{OUT} = 1.24V\left(1 + \frac{R2}{R1}\right)$$

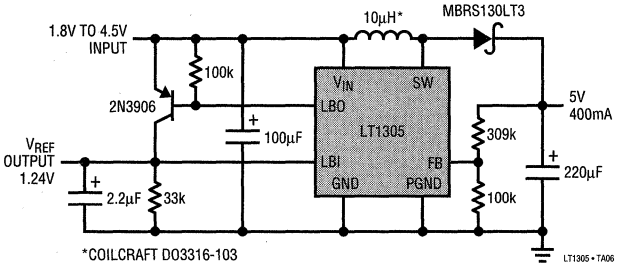
4-Cell-to-5V Converter



*COILCRAFT DO3316-223 OR
SUMIDA CD105-220

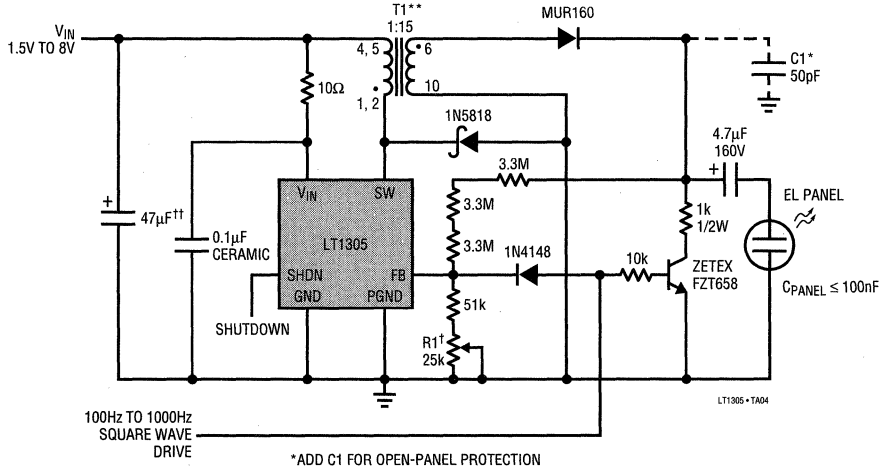
**SANYO OS-CON

5V Step-Up Converter with Reference Output



*COILCRAFT DO3316-103

EL Panel Driver



*ADD C1 FOR OPEN-PANEL PROTECTION

**DALE LPE5047-A132 1:15 TURNS RATIO
10µH PRIMARY INDUCTANCE (605) 666-9301

†R1 ADJUSTS V_{OUT} 83V_{RMS} TO 115V_{RMS}

††AVX TPS OR SANYO OS-CON MUST HAVE ESR ≤0.15Ω

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1129	Micropower Low Dropout Regulator	700mA Output Current in SO-8 Package
LT1182/83/84	LCD and CCFL Backlight Controller	High Efficiency and Excellent Backlight Control Range
LT1301	5V to 12V/200mA Step-Up DC/DC Converter	120μA Quiescent Current
LT1302	2-Cell to 5V/600mA Step-Up DC/DC Converter	200μA Quiescent Current
LT1303	Micropower DC/DC Converter with Low-Battery Detect	2V to 5V at 200mA
LT1372	500kHz Step-Up PWM, 1.5A Switch	Low Noise, Fixed Frequency Operation
LTC®1472	PCMCIA Host Switch with Protection	Includes Current Limit and Thermal Shutdown

500kHz High Efficiency 3A Switching Regulator

FEATURES

- **Faster Switching with Increased Efficiency**
- **Uses Small Inductors: 4.7μH**
- All Surface Mount Components
- Low Minimum Supply Voltage: 2.7V
- Quiescent Current: 4mA Typ
- Current Limited Power Switch: 3A
- Regulates Positive or Negative Outputs
- Shutdown Supply Current: 12μA Typ
- Easy External Synchronization

APPLICATIONS

- Boost Regulators
- Laptop Computer Supplies
- Multiple Output Flyback Supplies
- Inverting Supplies

DESCRIPTION

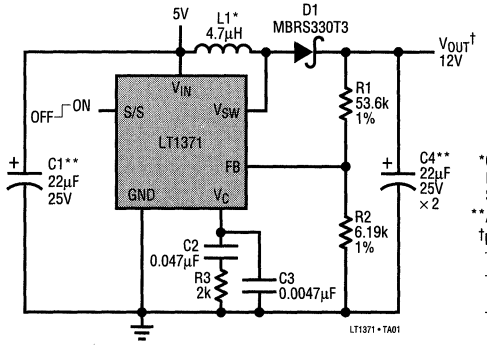
The LT®1371 is a monolithic high frequency current mode switching regulator. It can be operated in all standard switching configurations including boost, buck, flyback, forward, inverting and "Cuk." A 3A high efficiency switch is included on the die, along with all oscillator, control and protection circuitry.

The LT1371 typically consumes only 4mA quiescent current and has higher efficiency than previous parts. High frequency switching allows for very small inductors to be used.

New design techniques increase flexibility and maintain ease of use. Switching is easily synchronized to an external logic level source. A logic low on the Shutdown pin reduces supply current to 12μA. Unique error amplifier circuitry can regulate positive or negative output voltage while maintaining simple frequency compensation techniques. Nonlinear error amplifier transconductance reduces output overshoot on start-up or overload recovery. Oscillator frequency shifting protects external components during overload conditions.

TYPICAL APPLICATION

5V-to-12V Boost Converter



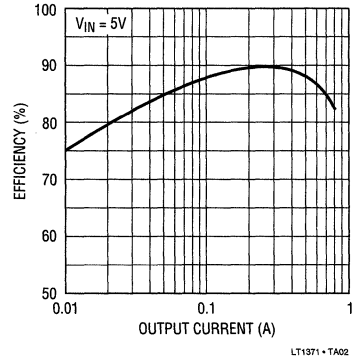
*COILCRAFT DO3316P-472 (4.7μH), DO3316P-103 (10μH) OR SUMIDA CD104-100MC (10μH)

**AVX TPSD226M025R0200

†MAX I_{OUT}

L1	I_{OUT}
4.7μH	0.7A
10μH	0.8A

12V Output Efficiency

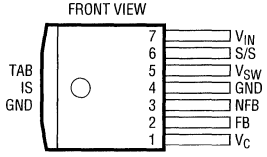


ABSOLUTE MAXIMUM RATINGS

Supply Voltage 30V
Switch Voltage 35V
S/S, $\overline{SHDN}$, SYNC Pin Voltage 30V
Feedback Pin Voltage (Transient, 10ms) ..... ±10V
Feedback Pin Current 10mA
Negative Feedback Pin Voltage
(Transient, 10ms) ..... ±10V

Operating Junction Temperature Range
Operating ..... 0°C to 125°C
Short Circuit ..... 0°C to 150°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



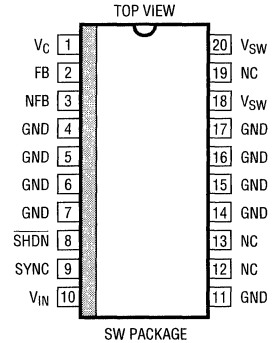
R PACKAGE
7-LEAD PLASTIC DD

T_{JMAX} = 125°C, θ_{JA} = 30°C/W

WITH PACKAGE SOLDERED TO 0.5 INCH² COPPER AREA OVER BACKSIDE GROUND PLANE OR INTERNAL POWER PLANE. θ_{JA} CAN VARY FROM 20°C/W TO >40°C/W DEPENDING ON MOUNTING TECHNIQUE

ORDER PART NUMBER
LT1371CR

For 7-lead TO-220 package availability contact LTC Marketing.



SW PACKAGE
20-LEAD PLASTIC SO WIDE

T_{JMAX} = 125°C, θ_{JA} = 50°C/W

θ_{JA} WILL VARY FROM APPROXIMATELY 40°C/W WITH 0.75 INCH² OF 1 OZ COPPER TO 50°C/W WITH 0.33 INCH² OF 1 OZ COPPER ON A DOUBLE-SIDED BOARD

ORDER PART NUMBER
LT1371CSW

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, V_{SW}, S/S, $\overline{SHDN}$, SYNC and NFB pins open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin		1.230	1.245	1.260	V
		V_C = 0.8V	●	1.225	1.245	1.265	V
I_{FB}	Feedback Input Current	V_{FB} = V_{REF}			250	550	nA
			●			900	nA
	Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.03	%/V
V_{NFR}	Negative Feedback Reference Voltage	Measured at Negative Feedback Pin		−2.535	−2.490	−2.445	V
		Feedback Pin Open, V_C = 0.8V	●	−2.570	−2.490	−2.410	V
I_{NFB}	Negative Feedback Input Current	V_{NFB} = V_{NFR}	●	−45	−30	−15	µA
	Negative Feedback Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.05	%/V
g_m	Error Amplifier Transconductance	ΔI_C = ±25µA		1100	1500	1900	µmho
			●	700		2300	µmho

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, V_{SW}, S/S, $\overline{SHDN}$, SYNC and NFB pins open, unless otherwise noted.

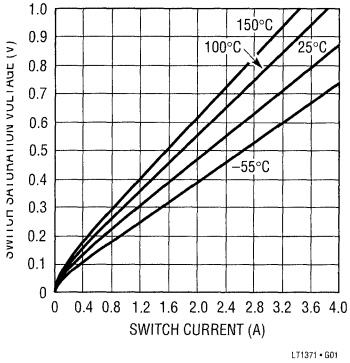
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Error Amplifier Source Current	$V_{FB} = V_{REF} - 150mV$, V_C = 1.5V	●	120	200	350	µA
	Error Amplifier Sink Current	$V_{FB} = V_{REF} + 150mV$, V_C = 1.5V	●		1400	2400	µA
	Error Amplifier Clamp Voltage	High Clamp, V_{FB} = 1V Low Clamp, V_{FB} = 1.5V		1.70 0.25	1.95 0.40	2.30 0.52	V V
A_V	Error Amplifier Voltage Gain				500		V/V
	V_C Pin Threshold	Duty Cycle = 0%		0.8	1	1.25	V
f	Switching Frequency	2.7V ≤ V_{IN} ≤ 25V	 ●	460 440	500 500	540 560	kHz kHz
	Maximum Switch Duty Cycle		●	85	95		%
	Switch Current Limit Blanking Time				130	260	ns
BV	Output Switch Breakdown Voltage	2.7V ≤ V_{IN} ≤ 25V	●	35	47		V
V_{SAT}	Output Switch ON Resistance	I_{SW} = 2A	●		0.25	0.45	Ω
I_{LIM}	Switch Current Limit	Duty Cycle = 50% Duty Cycle = 80% (Note 1)	● ●	3.0 2.6	3.8 3.4	4.8 4.4	A A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch ON Time				15	25	mA/A
	Control Voltage to Switch Current Transconductance				4		A/V
	Minimum Input Voltage		●		2.4	2.7	V
I_Q	Supply Current	2.7V ≤ V_{IN} ≤ 25V	●		4	5.5	mA
	Shutdown Supply Current	2.7V ≤ V_{IN} ≤ 25V, $V_{S/S}$ ≤ 0.6V	●		12	30	µA
	Shutdown Threshold	2.7V ≤ V_{IN} ≤ 25V	●	0.6	1.3	2	V
	Shutdown Delay		●	5	12	25	µs
	S/S or $\overline{SHDN}$ Pin Input Current	0V ≤ $V_{S/S}$ or $V_{\overline{SHDN}}$ ≤ 5V	●	–10		12	µA
	Synchronization Frequency Range		●	600		800	kHz

The ● denotes specifications which apply over the full operating temperature range.

Note 1: For duty cycles (DC) between 50% and 85%, minimum guaranteed switch current is given by I_{LIM} = 1.33 (2.75 – DC).

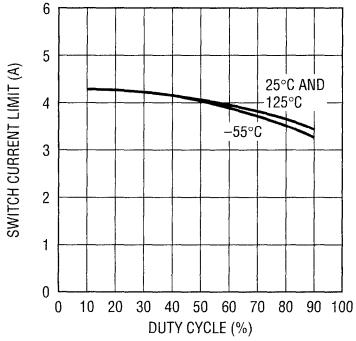
TYPICAL PERFORMANCE CHARACTERISTICS

Switch Saturation Voltage vs Switch Current



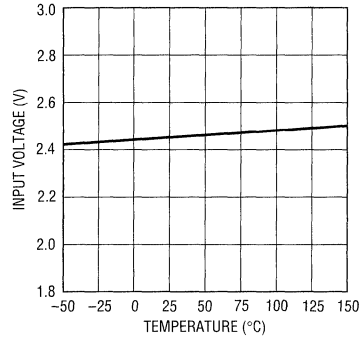
LT1371 • G01

Switch Current Limit vs Duty Cycle



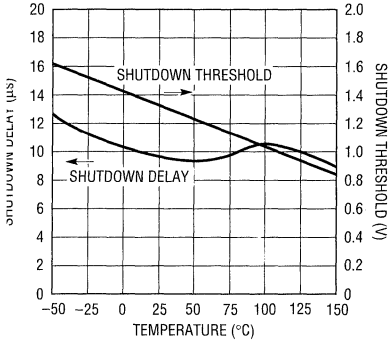
LT1371 • G02

Minimum Input Voltage vs Temperature



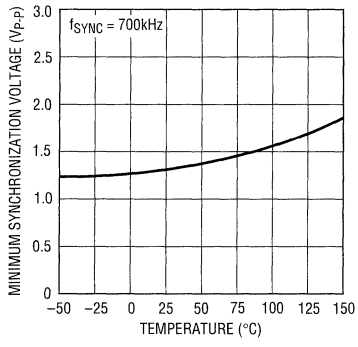
LT1371 • G03

Shutdown Delay and Threshold vs Temperature



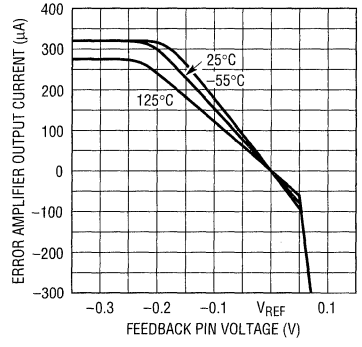
LT1371 • G04

Minimum Synchronization Voltage vs Temperature



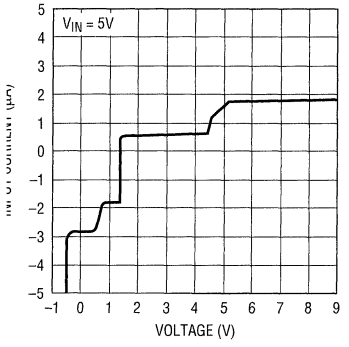
LT1371 • G05

Error Amplifier Output Current vs Feedback Pin Voltage



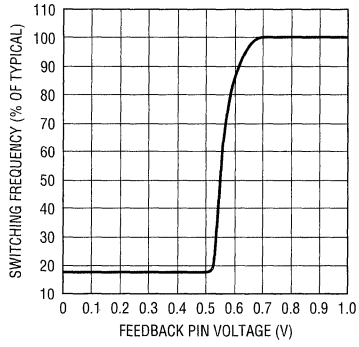
LT1371 • G06

S/S or $\overline{SHDN}$ Pin Input Current vs Voltage



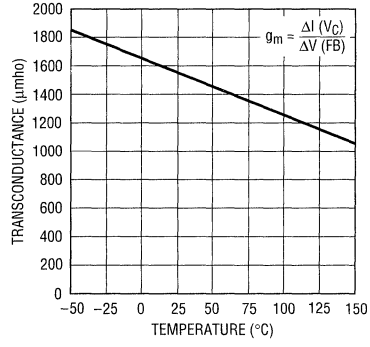
LT1371 • G07

Switching Frequency vs Feedback Pin Voltage



LT1371 • G08

Error Amplifier Transconductance vs Temperature

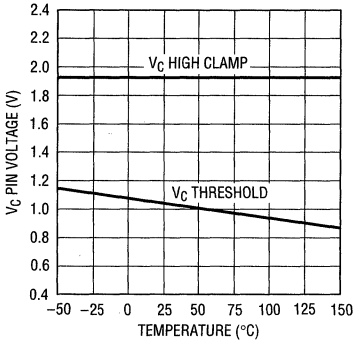


LT1371 • G09

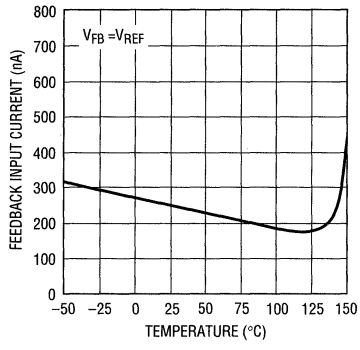
4

TYPICAL PERFORMANCE CHARACTERISTICS

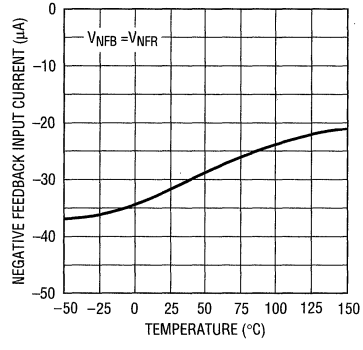
V_C Pin Threshold and High Clamp Voltage vs Temperature



Feedback Input Current vs Temperature



Negative Feedback Input Current vs Temperature



PIN FUNCTIONS

V_C: The compensation pin is used for frequency compensation, current limiting and soft start. It is the output of the error amplifier and the input of the current comparator. Loop frequency compensation can be performed with an RC network connected from the V_C pin to ground.

FB: The feedback pin is used for positive output voltage sensing and oscillator frequency shifting. It is the inverting input to the error amplifier. The noninverting input of this amplifier is internally tied to a 1.245V reference.

NFB: The negative feedback pin is used for negative output voltage sensing. It is connected to the inverting input of the negative feedback amplifier through a 100k source resistor.

S/S (R Package Only): Shutdown and Synchronization Pin. The S/S pin is logic level compatible. Shutdown is active low and the shutdown threshold is typically 1.3V. For normal operation, pull the S/S pin high, tie it to V_{IN} or leave it floating. To synchronize switching, drive the S/S pin between 600kHz and 800kHz.

$\overline{SHDN}$: (SW Package Only): The Shutdown pin is active low and the shutdown threshold is typically 1.3V. For normal operation, pull the $\overline{SHDN}$ pin high, tie it to V_{IN} or leave it floating.

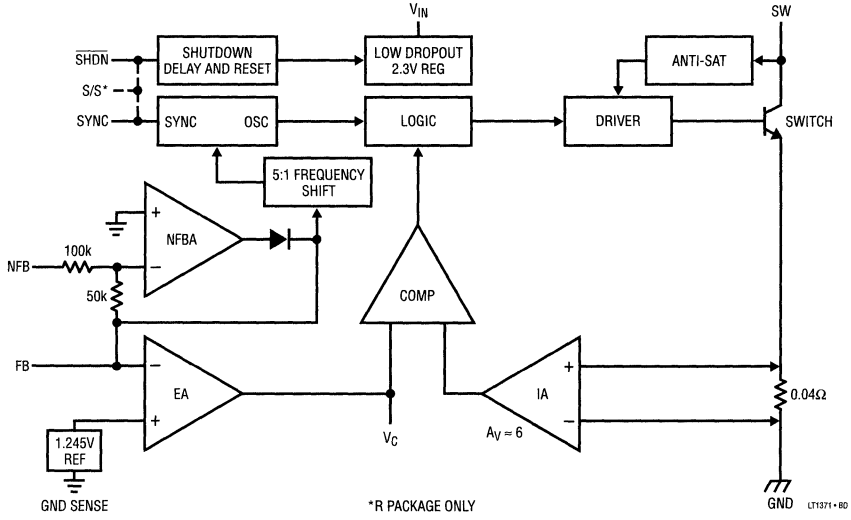
SYNC (SW Package Only): To synchronize switching, drive the SYNC pin between 600kHz and 800kHz. If not used, the SYNC pin can be tied high, low or left floating.

V_{IN}: Bypass input supply pin with a low ESR capacitor, 10µF or more. The regulator goes into undervoltage lockout when V_{IN} drops below 2.5V. Undervoltage lockout stops switching and pulls the V_C pin low.

V_{SW}: The switch pin is the collector of the power switch and has large currents flowing through it. Keep the traces to the switching components as short as possible to minimize radiation and voltage spikes.

GND: Tie all ground pins to a good quality ground plane.

BLOCK DIAGRAM



OPERATION

The LT1371 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned ON at the start of each oscillator cycle. It is turned OFF when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike voltage mode switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry. This low dropout design allows input voltage to vary from 2.7V to 45V with virtually no change in device performance. A 200kHz oscillator is the basic clock for all internal timing. It turns ON the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.245V bandgap reference biases the positive input of the error amplifier. The negative input of the amplifier is brought out for positive output voltage sensing. The error amplifier has nonlinear transconductance to reduce output overshoot on start-up or overload recovery. When the feedback voltage exceeds the reference by 40mV, error amplifier transconductance increases 10 times, which reduces output overshoot. The feedback input also invokes oscillator frequency shifting, which helps protect components during overload conditions. When the feedback voltage drops below 0.6V, the oscillator frequency is reduced 5:1. Lower switching frequency allows full control of switch current limit by reducing minimum switch duty cycle.

Unique error amplifier circuitry allows the LT1371 to directly regulate negative output voltages. The negative feedback amplifier's 100k source resistor is brought out for negative output voltage sensing. The NFB pin regulates at –2.49V while the amplifier output internally drives the FB pin to 1.245V. This architecture, which uses the same main error amplifier, prevents duplicating functions and

APPLICATIONS INFORMATION

maintains ease of use. Consult LTC, Marketing for units that can regulate down to –1.25V.

The error signal developed at the amplifier output is brought out externally. This pin (V_C) has three different functions. It is used for frequency compensation, current limit adjustment and soft starting. During normal regulator operation this pin sits at a voltage between 1V (low output current) and 1.9V (high output current). The error amplifier is a current output (g_m) type, so this voltage can be externally clamped for lowering current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled below the control pin threshold, placing the LT1371 in an idle mode.

APPLICATIONS INFORMATION

Positive Output Voltage Setting

The LT1371 develops a 1.245V reference (V_{REF}) from the FB pin to ground. Output voltage is set by connecting the FB pin to an output resistor divider (Figure 1). The FB pin bias current represents a small error and can usually be ignored for values of R2 up to 7k. The suggested value for R2 is 6.19k. The NFB pin is normally left open for positive output applications. Positive fixed voltage versions are available (consult LTC, Marketing).

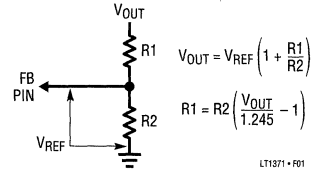


Figure 1. Positive Output Resistor Divider

Negative Output Voltage Setting

The LT1371 develops a –2.49V reference (V_{NFR}) from the NFB pin to ground. Output voltage is set by connecting the NFB pin to an output resistor divider (Figure 2). The –30µA NFB pin bias current (I_{NFB}) can cause output voltage errors and should not be ignored. This has been accounted for in the formula in Figure 2. The suggested value for R2 is 2.49k. The FB pin is normally left open for negative output applications.

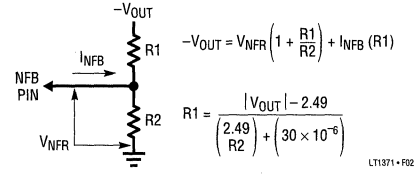


Figure 2. Negative Output Resistor Divider

Dual Polarity Output Voltage Sensing

Certain applications benefit from sensing both positive and negative output voltages. One example is the "Dual Output Flyback Converter with Overvoltage Protection" circuit shown in the Typical Applications section. Each output voltage resistor divider is individually set as described above. When both the FB and NFB pins are used, the LT1371 acts to prevent either output from going beyond its set output voltage. For example, in this application if the positive output were more heavily loaded than the negative, the negative output would be greater and would regulate at the desired set-point voltage. The positive output would sag slightly below its set-point voltage. This technique prevents either output from going unregulated high at no load.

Shutdown and Synchronization

The 7-pin R package device has a dual function S/S pin which is used for both shutdown and synchronization. The SW package device has both a Shutdown ($\overline{SHDN}$) pin and a Synchronization (SYNC) pin which can be used separately or tied together. These pins are logic level compatible and can be pulled high, tied to V_{IN} or left floating for normal operation. A logic low on the S/S pin or $\overline{SHDN}$ pin activates shutdown, reducing the part's supply current to 12µA. Typical synchronization range is from 1.05 to 1.8 times the part's natural switching frequency, but is only guaranteed between 600kHz and 800kHz. A 12µs resetable shutdown delay network guarantees the part will not go into shutdown while receiving a synchronization signal when the functions are combined.

IPPLICATIONS INFORMATION

aution should be used when synchronizing above 700kHz ecause at higher sync frequencies the amplitude of the ıternal slope compensation used to prevent subharmonic witching is reduced. This type of subharmonic switching nly occurs when the duty cycle of the switch is above 50%. igher inductor values will tend to eliminate problems.

hermal Considerations

are should be taken to ensure that the worst-case input oltage and load current conditions do not cause excesive die temperatures. Typical thermal resistance is 0°C/W for the R package and 50°C/W for the SW package ut these numbers will vary depending on the mounting chniques (copper area, air flow, etc.). Heat is transferred om the R package via the tab and from the SW package ia pins 4 to 7 and 14 to 17.

verage supply current (including driver current) is:

$I_{IN} = 4mA + DC\ [I_{SW}/60 + I_{SW}\ (0.004)]$

I_{SW} = switch current

DC = switch duty cycle

witch power dissipation is given by:

$P_{SW} = (I_{SW})^2\ (R_{SW})(DC)$

R_{SW} = output switch ON resistance

otal power dissipation of the die is the sum of supply ırrent times supply voltage, plus switch power:

$P_{D(TOTAL)} = (I_{IN})(V_{IN}) + P_{SW}$

urface mount heat sinks are also becoming available hich can lower package thermal resistance by 2 or 3 mes. One manufacturer is Wakefield Engineering who ffers surface mount heat sinks for both the R package)D) and SW package (SW20) and can be reached at (617) 45-5900.

hoosing the Inductor

or most applications the inductor will fall in the range of 2µH to 22µH. Lower values are chosen to reduce physiıl size of the inductor. Higher values allow more output ırrent because they reduce peak current seen by the ower switch, which has a 3A limit. Higher values also duce input ripple voltage and reduce core loss.

When choosing an inductor you might have to consider maximum load current, core and copper losses, allowable component height, output voltage ripple, EMI, fault current in the inductor, saturation and, of course, cost. The following procedure is suggested as a way of handling these somewhat complicated and conflicting requirements.

1. Assume that the average inductor current for a boost converter is equal to load current times V_{OUT}/V_{IN} and decide whether or not the inductor must withstand continuous overload conditions. If average inductor current at maximum load current is 1A, for instance, a 1A inductor may not survive a continuous 3A overload condition. Also be aware that boost converters are not short circuit protected and that, under output short conditions, inductor current is limited only by the available current of the input supply.

2. Calculate peak inductor current at full load current to ensure that the inductor will not saturate. Peak current can be significantly higher than output current, especially with smaller inductors and lighter loads, so don't omit this step. Powdered iron cores are forgiving because they saturate softly, whereas ferrite cores saturate abruptly and other core materials fall in between. The following formula assumes continuous mode operation but it errs only slightly on the high side for discontinuous mode, so it can be used for all conditions.

$$I_{PEAK} = (I_{OUT})\left(\frac{V_{OUT}}{V_{IN}}\right) + \frac{V_{IN}(V_{OUT} - V_{IN})}{2(f)(L)(V_{OUT})}$$

V_{IN} = Minimum Input Voltage
f = 500kHz Switching Frequency

3. Decide if the design can tolerate an "open" core geometry, like a rod or barrel, which has high magnetic field radiation, or whether it needs a closed core, like a toroid, to prevent EMI problems. One would not want an open core next to a magnetic storage media, for instance! This is a tough decision because the rods or barrels are temptingly cheap and small and there are no helpful guidelines to calculate when the magnetic field radiation will be a problem.

APPLICATIONS INFORMATION

4. Start shopping for an inductor which meets the requirements of core shape, peak current (to avoid saturation), average current (to limit heating) and fault current. If the inductor gets too hot, wire insulation will melt and cause turn-to-turn shorts. Keep in mind that all good things like high efficiency, low profile and high temperature operation will increase cost, sometimes dramatically.
5. After making an initial choice, consider the secondary things like output voltage ripple, second sourcing, etc. Use the experts in the LTC, Applications Department if you feel uncertain about the final choice. They have experience with a wide range of inductor types and can tell you about the latest developments in low profile, surface mounting, etc.

Output Capacitor

The output capacitor is normally chosen by its effective series resistance (ESR), because this is what determines output ripple voltage. At 500kHz any polarized capacitor is essentially resistive. To get low ESR takes *volume*, so physically smaller capacitors have high ESR. The ESR range needed for typical LT1371 applications is 0.025Ω to 0.2Ω. A typical output capacitor is an AVX type TPS, 22µF at 25V (2 each), with a guaranteed ESR less than 0.2Ω. This is a "D" size surface mount solid tantalum capacitor. TPS capacitors are specially constructed and tested for low ESR, so they give the lowest ESR for a given volume. To further reduce ESR, multiple output capacitors can be used in parallel. The value in microfarads is not particularly critical, and values from 22µF to greater than 500µF work well, but you cannot cheat mother nature on ESR. If you find a tiny 22µF solid tantalum capacitor, it will have high ESR and output ripple voltage will be terrible. Table 1 shows some typical solid tantalum surface mount capacitors.

Table 1. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

E CASE SIZE	ESR (MAX Ω)	RIPPLE CURRENT (A)
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.7 to 0.9	0.4
D CASE SIZE		
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.9 to 2.0	0.36 to 0.24
C CASE SIZE		
AVX TPS	0.2 (Typ)	0.5 (Typ)
AVX TAJ	1.8 to 3.0	0.22 to 0.17
B CASE SIZE		
AVX TAJ	2.5 to 10	0.16 to 0.08

Many engineers have heard that solid tantalum capacitors are prone to failure if they undergo high surge currents This is historically true and AVX type TPS capacitors are specially tested for surge capability, but surge ruggedness is not a critical issue with the *output* capacitor. Solic tantalum capacitors fail during very high *turn-on* surges which do not occur at the output of regulators. High *discharge* surges, such as when the regulator output is dead-shorted, do not harm the capacitors.

Single inductor boost regulators have large RMS ripple current in the output capacitor, which must be rated to handle the current. The formula to calculate this is:

Output Capacitor Ripple Current (RMS)

$$I_{RIPPLE}\ (RMS) = I_{OUT}\sqrt{\frac{DC}{1-DC}}$$

$$= I_{OUT}\sqrt{\frac{V_{OUT}-V_{IN}}{V_{IN}}}$$

DC = Switch Duty Cycle

Input Capacitors

The input capacitor of a boost converter is less critical due to the fact that the input current waveform is triangular and does not contain large squarewave currents as is found in the output capacitor. Capacitors in the range of 10µF to 100µF, with an ESR of 0.2Ω or less, work well up to full 3A switch current. Higher ESR capacitors may be acceptable at low switch currents. Input capacitor ripple current for a boost converter is :

$$I_{RIPPLE} = \frac{0.3(V_{IN})(V_{OUT}-V_{IN})}{(f)(L)(V_{OUT})}$$

f = 500kHz Switching Frequency

The input capacitor can see a very high surge current when a battery or high capacitance source is connected "live" and solid tantalum capacitors can fail under this condition

APPLICATIONS INFORMATION

Several manufacturers have developed tantalum capacitors specially tested for surge capability (AVX TPS series, for instance) but even these units may fail if the input voltage approaches the maximum voltage rating of the capacitor during a high surge. AVX recommends derating capacitor voltage by 2:1 for high surge applications. Ceramic, OS-CON and aluminum electrolytic capacitors may also be used and have a high tolerance to turn-on surges.

Ceramic Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. These are tempting for switching regulator use because of their very low ESR. Unfortunately, the ESR is so low that it can cause loop stability problems. Solid tantalum capacitor ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before ESR becomes effective. They are appropriate for input bypassing because of their high ripple current ratings and tolerance of turn-on surges.

Output Diode

The suggested output diode (D1) is a 1N5821 Schottky or its Motorola equivalent MBR330. It is rated at 3A average forward current and 30V reverse voltage. Typical forward voltage is 0.6V at 3A. The diode conducts current only during switch OFF time. Peak reverse voltage for boost converters is equal to regulator output voltage. Average forward current in normal operation is equal to output current.

Frequency Compensation

Loop frequency compensation is performed on the output of the error amplifier (V_C pin) with a series RC network. The main pole is formed by the series capacitor and the output impedance (≈500kΩ) of the error amplifier. The pole falls in the range of 2Hz to 20Hz. The series resistor creates a "zero" at 1kHz to 5kHz, which improves loop stability and transient response. A second capacitor, typically one-tenth the size of the main compensation capacitor, is sometimes used to reduce the switching frequency ripple on the V_C pin. V_C pin ripple is caused by output voltage ripple attenuated by the output divider and multiplied by the error amplifier. Without the second capacitor, V_C pin ripple is:

$$V_C \text{ Pin Ripple} = \frac{1.245(V_{RIPPLE})(g_m)(R_C)}{(V_{OUT})}$$

V_{RIPPLE} = Output ripple (V_{P-P})
g_m = Error amplifier transconductance (≈1500μmho)
R_C = Series resistor on V_C pin
V_{OUT} = DC output voltage

To prevent irregular switching, V_C pin ripple should be kept below 50mV_{P-P}. Worst-case V_C pin ripple occurs at maximum output load current and will also be increased if poor quality (high ESR) output capacitors are used. The addition of a 0.0047μF capacitor on the V_C pin reduces switching frequency ripple to only a few millivolts. A low value for R_C will also reduce V_C pin ripple, but loop phase margin may be inadequate.

Switch Node Considerations

For maximum efficiency, LT1371 switch rise and fall times are made as short as possible. To prevent radiation and high frequency resonance problems, proper layout of the components connected to the switch node is essential. B field (magnetic) radiation is minimized by keeping output diode, Switch pin and output bypass capacitor leads as short as possible. Figures 3 and 4 show recommended

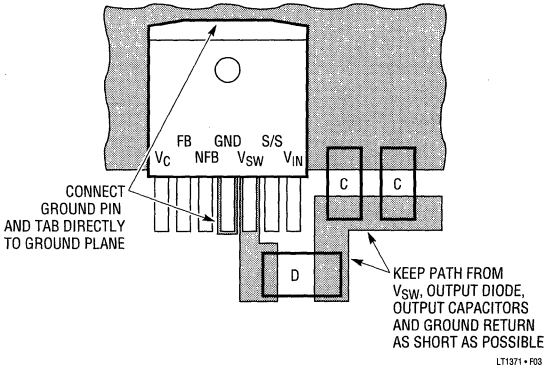


Figure 3. Layout Considerations—R Package

APPLICATIONS INFORMATION

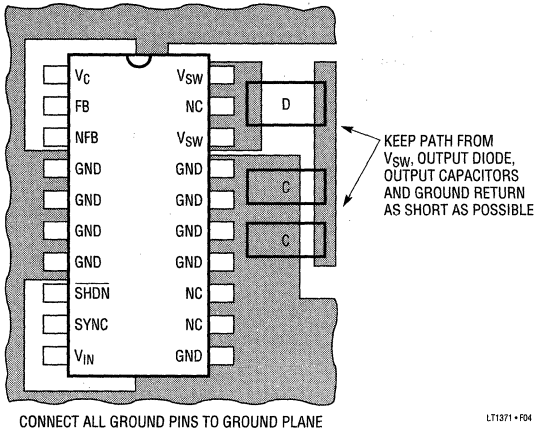


Figure 4. Layout Considerations—SW Package

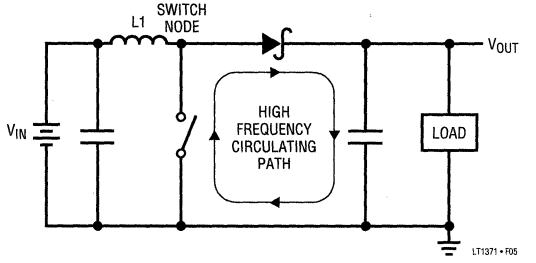


Figure 5

positions for these components. E field radiation is kep low by minimizing the length and area of all traces con nected to the Switch pin. A ground plane should always be used under the switcher circuitry to prevent interplane coupling.

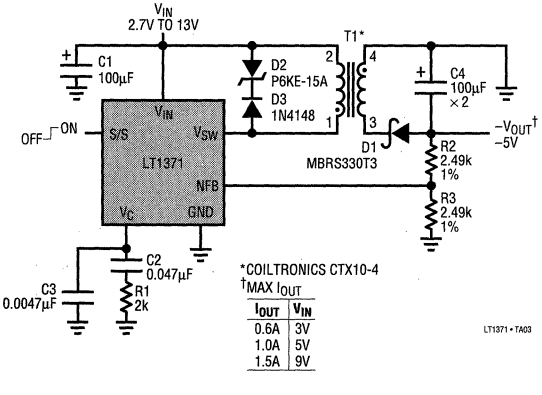
The high speed switching current path is shown schemati cally in Figure 5. Minimum lead length in this path is essential to ensure clean switching and low EMI. The path including the switch, output diode and output capacitor is the only one containing nanosecond rise and fall times Keep this path as short as possible.

More Help

For more detailed information on switching regulato circuits, please see Application Note 19. Linear Technol ogy also offers a computer software program SwitcherCAD, to assist in designing switching converters In addition, our Applications Department is always ready to lend a helping hand.

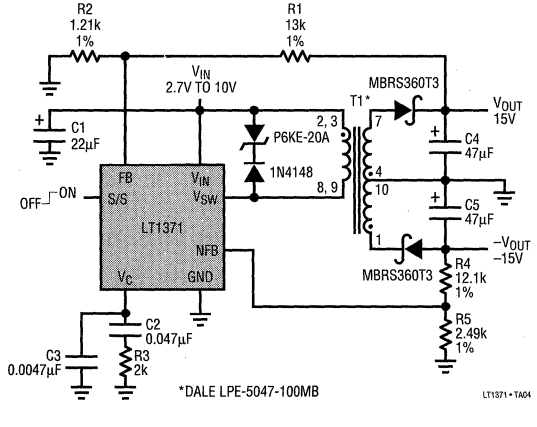
TYPICAL APPLICATIONS

Positive-to-Negative Converter with Direct Feedback



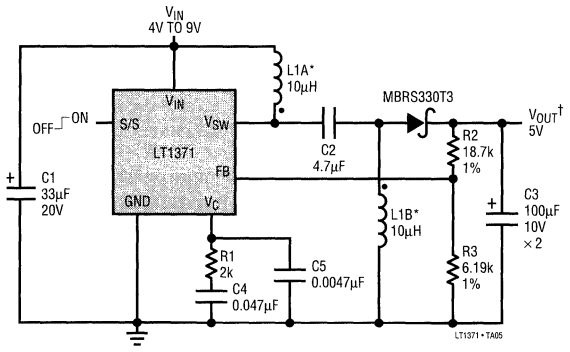
IOUT	VIN
0.6A	3V
1.0A	5V
1.5A	9V

Dual Output Flyback Converter with Overvoltage Protection



TYPICAL APPLICATIONS

2 Li-Ion Cells to 5V SEPIC Converter**

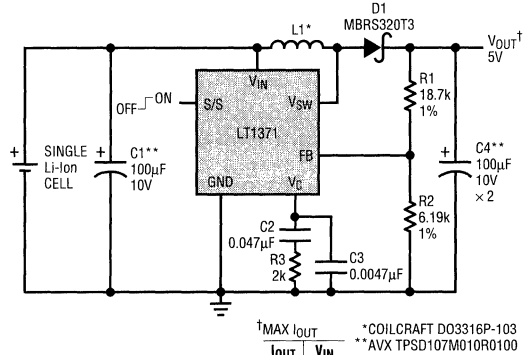


C1 = AVX TPSD 336M020R0200
C2 = TOKIN 1E475ZY5U-C304
C3 = AVX TPSD107M010R0100
* SINGLE INDUCTOR WITH TWO WINDINGS COILTRONICS CTX10-4
** INPUT VOLTAGE MAY BE GREATER OR LESS THAN OUTPUT VOLTAGE

†MAX I_{OUT}

I_{OUT}	V_{IN}
0.85A	4V
1A	5V
1.3A	7V
1.5A	9V

Single Li-Ion Cell to 5V



*COILCRAFT DO3316P-103
**AVX TPSD107M010R0100

†MAX I_{OUT}

I_{OUT}	V_{IN}
1.2A	2.7V
1.6A	3.3V
1.8A	3.6V

4

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
T1171	100kHz 2.5A Boost Switching Regulator	Good for Up to V_{IN} = 40V
TC®1265	12V 1.2A Monolithic Buck Converter	Converts 5V to 3.3V at 1A with 90% Efficiency
T1302	Micropower 2A Boost Converter	Converts 2V to 5V at 600mA in SO-8 Packages
T1372	500kHz 1.5A Boost Switching Regulator	Also Regulates Negative Flyback Outputs
T1373	Low Supply Current 250kHz 1.5A Boost Switching Regulator	90% Efficient Boost Converter with Constant Frequency
T1376	500kHz 1.5A Buck Switching Regulator	Steps Down from Up to 25V Using 4.7µH Inductors
T1512	500kHz 1.5A SEPIC Battery Charger	Input Voltage May Be Greater or Less Than Battery Voltage
T1513	500kHz 3A SEPIC Battery Charger	Input Voltage May Be Greater or Less Than Battery Voltage

500kHz and 1MHz High Efficiency 1.5A Switching Regulators

FEATURES

- **Faster Switching with Increased Efficiency**
- **Uses Small Inductors: 4.7μH**
- All Surface Mount Components
- Only 0.5 Square Inch of Board Space
- Low Minimum Supply Voltage: 2.7V
- Quiescent Current: 4mA Typ
- Current Limited Power Switch: 1.5A
- Regulates Positive or Negative Outputs
- Shutdown Supply Current: 12μA Typ
- Easy External Synchronization
- 8-Pin SO or PDIP Packages

APPLICATIONS

- Boost Regulators
- CCFL Backlight Driver
- Laptop Computer Supplies
- Multiple Output Flyback Supplies
- Inverting Supplies

DESCRIPTION

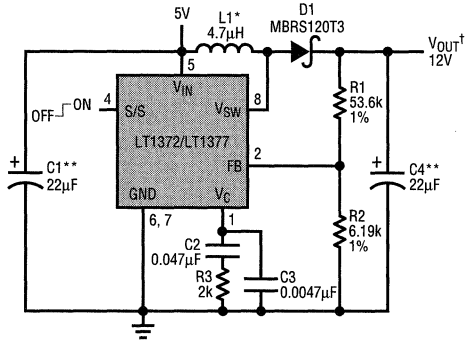
The LT®1372/LT1377 are monolithic high frequency switching regulators. They can be operated in all standard switching configurations including boost, buck, flyback, forward, inverting and "Cuk." A 1.5A high efficiency switch is included on the die, along with all oscillator, control and protection circuitry. All functions of the LT1372/LT1377 are integrated into 8-pin SO/PDIP packages.

The LT1372/LT1377 typically consumes only 4mA quiescent current and has higher efficiency than previous parts. High frequency switching allows for very small inductors to be used. All surface mount components consume less than 0.5 square inch of board space.

New design techniques increase flexibility and maintain ease of use. Switching is easily synchronized to an external logic level source. A logic low on the shutdown pin reduces supply current to 12μA. Unique error amplifier circuitry can regulate positive or negative output voltage while maintaining simple frequency compensation techniques. Nonlinear error amplifier transconductance reduces output overshoot on start-up or overload recovery. Oscillator frequency shifting protects external components during overload conditions.

TYPICAL APPLICATION

5V-to-12V Boost Converter



*COILCRAFT DO1608-472 (4.7μH) OR
COILCRAFT DT3316-103 (10μH) OR
SUMIDA CD43-4R7 (4.7μH) OR
SUMIDA CD73-100KC (10μH) OR

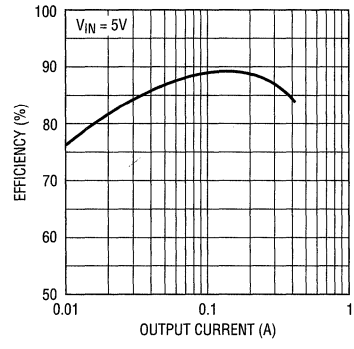
**AVX TPSD226M025R0200

†MAX I_{OUT}

L1	I_{OUT}
4.7μH	0.25A
10μH	0.35A

LT1372 • TA01

12V Output Efficiency



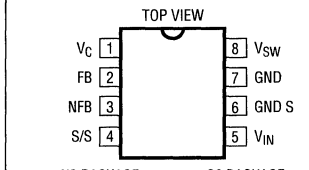
LT1372 • TA02

ABSOLUTE MAXIMUM RATINGS

upply Voltage 30V
witch Voltage 35V
/S Pin Voltage 30V
eedback Pin Voltage (Transient, 10ms) ..... ±10V
eedback Pin Current 10mA
legative Feedback Pin Voltage
(Transient, 10ms) ..... ±10V
Operating Junction Temperature Range
Operating ..... 0°C to 125°C*
Short Circuit ..... 0°C to 150°C
torage Temperature Range ..... –65°C to 150°C
ead Temperature (Soldering, 10 sec) ..... 300°C

Units shipped prior to Date Code 9552 are rated at 100°C maximum operating temperature.

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 120°C/W (S8)

ORDER PART NUMBER
LT1372CN8 LT1372CS8 LT1377CS8
S8 PART MARKING
1372 1377

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

IN = 5V, V_C = 0.6V, V_{FB} = V_{REF}, V_{SW}, S/S and NFB pins open, unless otherwise noted.

YMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
REF	Reference Voltage	Measured at Feedback Pin V_C = 0.8V	 ●	1.230 1.225	1.245 1.245	1.260 1.265	V V
B	Feedback Input Current	V_{FB} = V_{REF}	 ●		250	550 900	nA nA
	Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.03	%/V
NFR	Negative Feedback Reference Voltage	Measured at Negative Feedback Pin Feedback Pin Open, V_C = 0.8V	 ●	–2.535 –2.570	–2.490 –2.490	–2.445 –2.410	V V
FB	Negative Feedback Input Current	V_{NFB} = V_{NFR}	●	–45	–30	–15	µA
	Negative Feedback Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.05	%/V
m	Error Amplifier Transconductance	ΔI_C = ±25µA	 ●	1100 700	1500	1900 2300	µmho µmho
	Error Amplifier Source Current	V_{FB} = V_{REF} – 150mV, V_C = 1.5V	●	120	200	350	µA
	Error Amplifier Sink Current	V_{FB} = V_{REF} + 150mV, V_C = 1.5V	●		1400	2400	µA
	Error Amplifier Clamp Voltage	High Clamp, V_{FB} = 1V Low Clamp, V_{FB} = 1.5V		1.70 0.25	1.95 0.40	2.30 0.52	V V
/	Error Amplifier Voltage Gain				500		V/V
	V_C Pin Threshold	Duty Cycle = 0%		0.8	1	1.25	V
	Switching Frequency	2.7V ≤ V_{IN} ≤ 25V LT1372 LT1377	 ● ●	 460 440 0.92 0.88	 500 500 1 1	 540 560 1.08 1.12	 kHz kHz MHz MHz
	Maximum Switch Duty Cycle		●	90	95		%
	Switch Current Limit Blanking Time				130	260	ns
/	Output Switch Breakdown Voltage	2.7V ≤ V_{IN} ≤ 25V	●	35	47		V
SAT	Output Switch "On" Resistance	I_{SW} = 1A	●		0.5	0.8	Ω

4

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, V_{SW}, S/S and NFB pins open, unless otherwise noted.

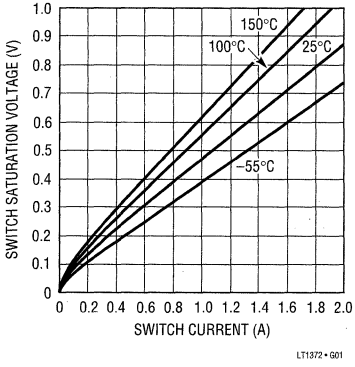
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{LIM}	Switch Current Limit	Duty Cycle = 50% Duty Cycle = 80% (Note 1)	● ●	1.5 1.3	1.9 1.7	2.4 2.2	A A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time				15	25	mA/A
	Control Voltage to Switch Current Transconductance				2		A/V
	Minimum Input Voltage		●		2.4	2.7	V
I_Q	Supply Current	2.7V ≤ V_{IN} ≤ 25V	●		4	5.5	mA
	Shutdown Supply Current	2.7V ≤ V_{IN} ≤ 25V, $V_{S/S}$ ≤ 0.6V	●		12	30	µA
	Shutdown Threshold	2.7V ≤ V_{IN} ≤ 25V	●	0.6	1.3	2	V
	Shutdown Delay		●	5	12	25	µs
	S/S Pin Input Current	0V ≤ $V_{S/S}$ ≤ 5V	●	–10		12	µA
	Synchronization Frequency Range	LT1372 LT1377	● ●	600 1.2		800 1.6	kHz MHz

The ● denotes specifications which apply over the full operating temperature range.

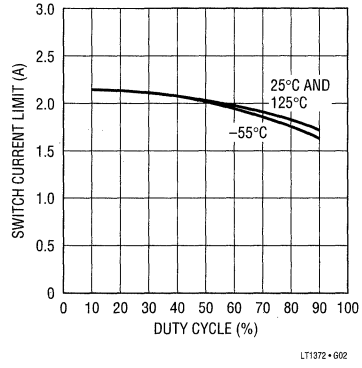
Note 1: For duty cycles (DC) between 50% and 90%, minimum guaranteed switch current is given by I_{LIM} = 0.667 (2.75 – DC).

TYPICAL PERFORMANCE CHARACTERISTICS

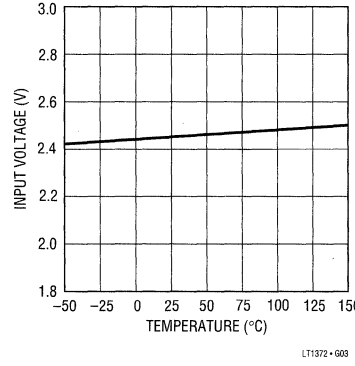
Switch Saturation Voltage vs Switch Current



Switch Current Limit vs Duty Cycle

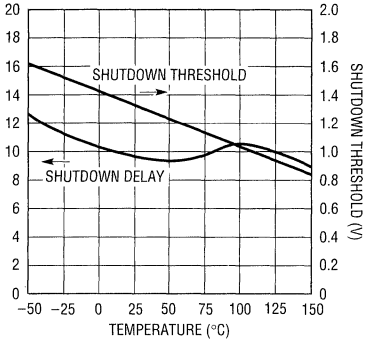


Minimum Input Voltage vs Temperature



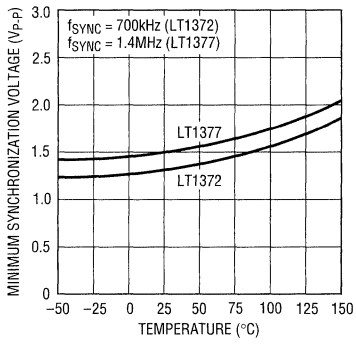
TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown Delay and Threshold vs Temperature



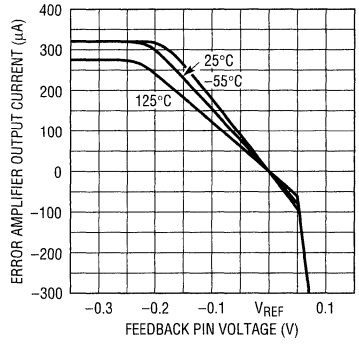
LT1372 • G04

Minimum Synchronization Voltage vs Temperature



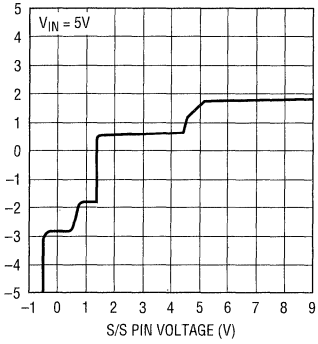
LT1372 • G05

Error Amplifier Output Current vs Feedback Pin Voltage



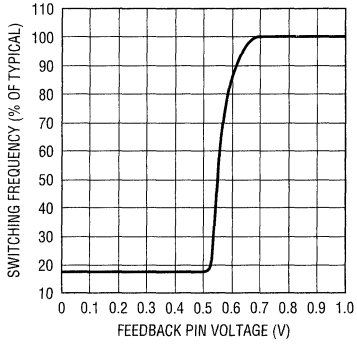
LT1372 • G06

S/S Pin Input Current vs Voltage



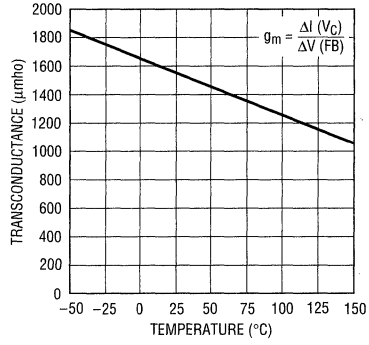
LT1372 • G07

Switching Frequency vs Feedback Pin Voltage



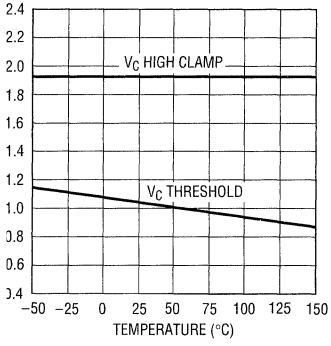
LT1372 • G08

Error Amplifier Transconductance vs Temperature



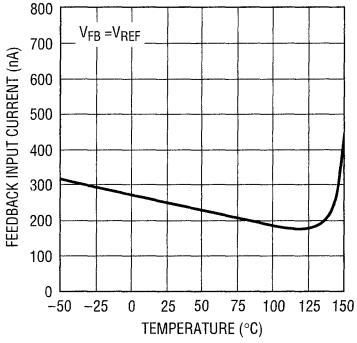
LT1372 • G09

V_C Pin Threshold and High Clamp Voltage vs Temperature



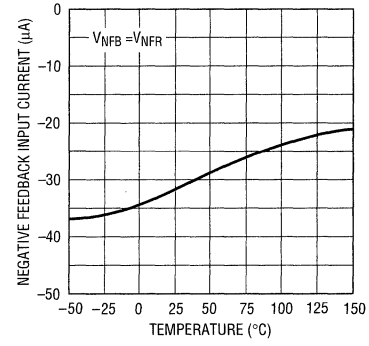
LT1372 • G10

Feedback Input Current vs Temperature



LT1372 • G11

Negative Feedback Input Current vs Temperature



LT1372 • G12

PIN FUNCTIONS

V_C (Pin 1): The compensation pin is used for frequency compensation, current limiting and soft start. It is the output of the error amplifier and the input of the current comparator. Loop frequency compensation can be performed with an RC network connected from the V_C pin to ground.

FB (Pin 2): The feedback pin is used for positive output voltage sensing and oscillator frequency shifting. It is the inverting input to the error amplifier. The noninverting input of this amplifier is internally tied to a 1.245V reference.

NFB (Pin 3): The negative feedback pin is used for negative output voltage sensing. It is connected to the inverting input of the negative feedback amplifier through a 100k source resistor.

S/S (Pin 4): Shutdown and Synchronization Pin. The S/S pin is logic level compatible. Shutdown is active low and the shutdown threshold is typically 1.3V. For normal operation, pull the S/S pin high, tie it to V_{IN} or leave it floating. To synchronize switching, drive the S/S pin between 600kHz and 800kHz (LT1372) or 1.2MHz to 1.6MHz (LT1377).

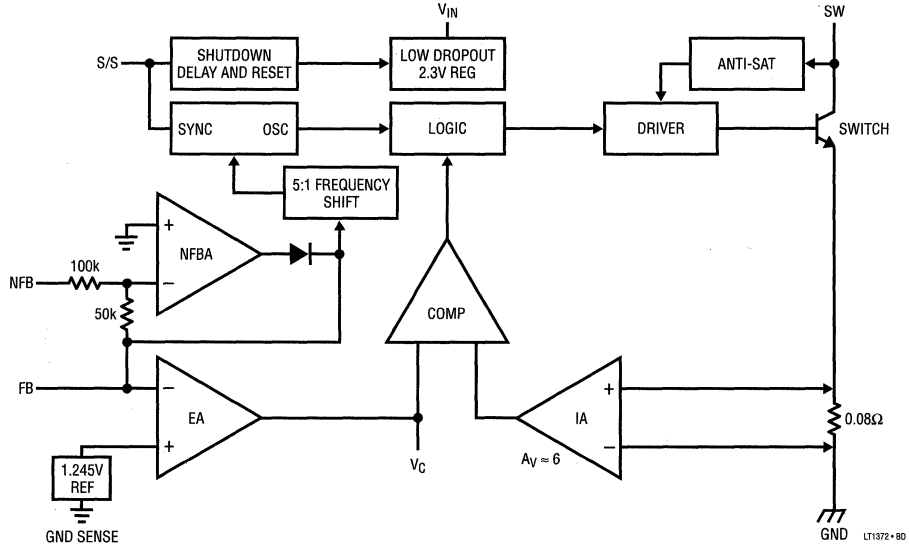
V_{IN} (Pin 5): Bypass input supply pin with 10µF or more. Th part goes into undervoltage lockout when V_{IN} drops belo 2.5V. Undervoltage lockout stops switching and pulls th V_C pin low.

GND S (Pin 6): The ground sense pin is a "clean" groun The internal reference, error amplifier and negative feed back amplifier are referred to the ground sense pin. Cor nect it to ground. Keep the ground path connection to th output resistor divider and the V_C compensation netwo free of large ground currents.

GND (Pin 7): The ground pin is the emitter connection the power switch and has large currents flowing through i It should be connected directly to a good quality groun plane.

V_{SW} (Pin 8): The switch pin is the collector of the pow switch and has large currents flowing through it. Keep th traces to the switching components as short as possible t minimize radiation and voltage spikes.

BLOCK DIAGRAM



OPERATION

he LT1372/LT1377 are current mode switchers. This ieans that switch duty cycle is directly controlled by witch current rather than by output voltage. Referring to ie block diagram, the switch is turned "On" at the start of ach oscillator cycle. It is turned "Off" when switch current eaches a predetermined level. Control of output voltage is btained by using the output of a voltage sensing error mplifier to set current trip level. This technique has everal advantages. First, it has immediate response to iput voltage variations, unlike voltage mode switchers /hich have notoriously poor line transient response. econd, it reduces the 90° phase shift at mid-frequencies i the energy storage inductor. This greatly simplifies losed-loop frequency compensation under widely vary- ig input voltage or output load conditions. Finally, it llows simple pulse-by-pulse current limiting to provide iaximum switch protection under output overload or hort conditions. A low dropout internal regulator pro- ides a 2.3V supply for all internal circuitry. This low ropout design allows input voltage to vary from 2.7V to 5V with virtually no change in device performance. A 00kHz (LT1372) or 1MHz (LT1377) oscillator is the basic lock for all internal timing. It turns "On" the output switch ia the logic and driver circuitry. Special adaptive anti-sat ircuitry detects onset of saturation in the power switch nd adjusts driver current instantaneously to limit switch aturation. This minimizes driver dissipation and provides ery rapid turn-off of the switch.

1.245V bandgap reference biases the positive input of ie error amplifier. The negative input of the amplifier is rought out for positive output voltage sensing. The error mplifier has nonlinear transconductance to reduce output overshoot on start-up or overload recovery. When the feedback voltage exceeds the reference by 40mV, error amplifier transconductance increases ten times, which reduces output overshoot. The feedback input also invokes oscillator frequency shifting, which helps protect components during overload conditions. When the feedback voltage drops below 0.6V, the oscillator frequency is reduced 5:1. Lower switching frequency allows full control of switch current limit by reducing minimum switch duty cycle.

Unique error amplifier circuitry allows the LT1372/LT1377 to directly regulate negative output voltages. The negative feedback amplifier's 100k source resistor is brought out for negative output voltage sensing. The NFB pin regulates at –2.49V while the amplifier output internally drives the FB pin to 1.245V. This architecture, which uses the same main error amplifier, prevents duplicating functions and maintains ease of use. Consult Linear Technology marketing for units that can regulate down to –1.25V.

The error signal developed at the amplifier output is brought out externally. This pin (V_C) has three different functions. It is used for frequency compensation, current limit adjustment and soft starting. During normal regulator operation this pin sits at a voltage between 1V (low output current) and 1.9V (high output current). The error amplifier is a current output (g_m) type, so this voltage can be externally clamped for lowering current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled below the control pin threshold, placing the LT1372/LT1377 in an idle mode.

APPLICATIONS INFORMATION

ositive Output Voltage Setting

he LT1372/LT1377 develops a 1.245V reference (V_{REF}) om the FB pin to ground. Output voltage is set by onnecting the FB pin to an output resistor divider igure 1). The FB pin bias current represents a small ror and can usually be ignored for values of R2 up to 7k. he suggested value for R2 is 6.19k. The NFB pin is ormally left open for positive output applications.

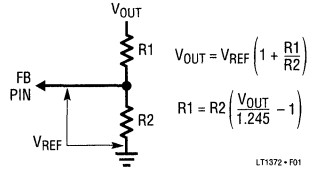


Figure 1. Positive Output Resistor Divider

APPLICATIONS INFORMATION

Positive fixed voltage versions are available (consult Linear Technology marketing).

Negative Output Voltage Setting

The LT1372/LT1377 develops a –2.49V reference (V_{NFR}) from the NFB pin to ground. Output voltage is set by connecting the NFB pin to an output resistor divider (Figure 2). The –30µA NFB pin bias current (I_{NFB}) can cause output voltage errors and should not be ignored. This has been accounted for in the formula in Figure 2. The suggested value for R2 is 2.49k. The FB pin is normally left open for negative output application.

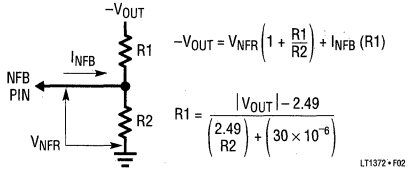


Figure 2. Negative Output Resistor Divider

Dual Polarity Output Voltage Sensing

Certain applications benefit from sensing both positive and negative output voltages. One example is the "Dual Output Flyback Converter with Overvoltage Protection" circuit shown in the Typical Applications section. Each output voltage resistor divider is individually set as described above. When both the FB and NFB pins are used, the LT1372/LT1377 acts to prevent either output from going beyond its set output voltage. For example in this application, if the positive output were more heavily loaded than the negative, the negative output would be greater and would regulate at the desired set-point voltage. The positive output would sag slightly below its set-point voltage. This technique prevents either output from going unregulated high at no load.

Shutdown and Synchronization

The dual function S/S pin provides easy shutdown and synchronization. It is logic level compatible and can be pulled high, tied to V_{IN} or left floating for normal operation. A logic low on the S/S pin activates shutdown, reducing the part's supply current to 12µA. Typical synchronization range is from 1.05 to 1.8 times the part's natural switchin frequency, but is only guaranteed between 600kHz an 800kHz (LT1372) or 1.2MHz and 1.6MHz (LT1377). A 12µs resetable shutdown delay network guarantees th part will not go into shutdown while receiving a synchro nization signal.

Caution should be used when synchronizing above 700kH (LT1372) or 1.4MHz (LT1377) because at higher syn frequencies the amplitude of the internal slope compensa tion used to prevent subharmonic switching is reduced This type of subharmonic switching only occurs when th duty cycle of the switch is above 50%. Higher inducto values will tend to eliminate problems.

Thermal Considerations

Care should be taken to ensure that the worst-case inpu voltage and load current conditions do not cause exces sive die temperatures. The packages are rated at 120°C/W for SO (S8) and 130°C/W for PDIP (N8).

Average supply current (including driver current) is:

$I_{IN} = 4mA + DC\ (I_{SW}/60 + I_{SW} \times 0.004)$

I_{SW} = switch current

DC = switch duty cycle

Switch power dissipation is given by:

$P_{SW} = (I_{SW})^2 \times R_{SW} \times DC$

R_{SW} = output switch "On" resistance

Total power dissipation of the die is the sum of supply current times supply voltage plus switch power:

$P_{D(TOTAL)} = (I_{IN} \times V_{IN}) + P_{SW}$

Choosing the Inductor

For most applications the inductor will fall in the range o 2.2µH to 22µH. Lower values are chosen to reduce physi cal size of the inductor. Higher values allow more outpu current because they reduce peak current seen by th power switch, which has a 1.5A limit. Higher values als reduce input ripple voltage and reduce core loss.

When choosing an inductor you might have to conside maximum load current, core and copper losses, allowabl component height, output voltage ripple, EMI, faul

PPLICATIONS INFORMATION

ırrent in the inductor, saturation, and of course, cost. ıe following procedure is suggested as a way of handling ese somewhat complicated and conflicting requirements.

Assume that the average inductor current for a boost converter is equal to load current times V_{OUT}/V_{IN} and decide whether or not the inductor must withstand continuous overload conditions. If average inductor current at maximum load current is 0.5A, for instance, a 0.5A inductor may not survive a continuous 1.5A overload condition. Also be aware that boost converters are not short circuit protected, and that under output short conditions, inductor current is limited only by the available current of the input supply.

Calculate peak inductor current at full load current to ensure that the inductor will not saturate. Peak current can be significantly higher than output current, especially with smaller inductors and lighter loads, so don't omit this step. Powdered iron cores are forgiving because they saturate softly, whereas ferrite cores saturate abruptly. Other core materials fall in between somewhere. The following formula assumes continuous mode operation but it errors only slightly on the high side for discontinuous mode, so it can be used for all conditions.

$$I_{PEAK} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2(f)(L)(V_{OUT})}$$

V_{IN} = Minimum Input Voltage
f = 500kHz Switching Frequency (LT1372) or
1MHz Switching Frequency (LT1377)

Decide if the design can tolerate an "open" core geometry like a rod or barrel, which have high magnetic field radiation, or whether it needs a closed core like a toroid to prevent EMI problems. One would not want an open core next to a magnetic storage media for instance! This is a tough decision because the rods or barrels are temptingly cheap and small, and there are no helpful guidelines to calculate when the magnetic field radiation will be a problem.

4. Start shopping for an inductor which meets the requirements of core shape, peak current (to avoid saturation), average current (to limit heating) and fault current. If the inductor gets too hot, wire insulation will melt and cause turn-to-turn shorts. Keep in mind that all good things like high efficiency, low profile and high temperature operation will increase cost, sometimes dramatically.
5. After making an initial choice, consider the secondary things like output voltage ripple, second sourcing, etc. Use the experts in the Linear Technology application department if you feel uncertain about the final choice. They have experience with a wide range of inductor types and can tell you about the latest developments in low profile, surface mounting, etc.

Output Capacitor

The output capacitor is normally chosen by its effective series resistance, (ESR), because this is what determines output ripple voltage. At 500kHz, any polarized capacitor is essentially resistive. To get low ESR takes *volume*, so physically smaller capacitors have high ESR. The ESR range for typical LT1372 and LT1377 applications is 0.05Ω to 0.5Ω. A typical output capacitor is an AVX type TPS, 22µF at 25V, with a guaranteed ESR less than 0.2Ω. This is a "D" size surface mount solid tantalum capacitor. TPS capacitors are specially constructed and tested for low ESR, so they give the lowest ESR for a given volume. To further reduce ESR, multiple output capacitors can be used in parallel. The value in microfarads is not particularly critical, and values from 22µF to greater than 500µF work well, but you cannot cheat mother nature on ESR. If you find a tiny 22µF solid tantalum capacitor, it will have high ESR, and output ripple voltage will be terrible. Table 1 shows some typical solid tantalum surface mount capacitors.

APPLICATIONS INFORMATION

Table 1. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

E CASE SIZE	ESR (MAX Ω)	RIPPLE CURRENT (A)
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.7 to 0.9	0.4
D CASE SIZE		
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.9 to 2.0	0.36 to 0.24
C CASE SIZE		
AVX TPS	0.2 (Typ)	0.5 (Typ)
AVX TAJ	1.8 to 3.0	0.22 to 0.17
B CASE SIZE		
AVX TAJ	2.5 to 10	0.16 to 0.08

Many engineers have heard that solid tantalum capacitors are prone to failure if they undergo high surge currents. This is historically true and type TPS capacitors are specially tested for surge capability, but surge ruggedness is not a critical issue with the *output* capacitor. Solid tantalum capacitors fail during very high *turn-on* surges, which do not occur at the output of regulators. High *discharge* surges, such as when the regulator output is dead shorted, do not harm the capacitors.

Single inductor boost regulators have large RMS ripple current in the output capacitor, which must be rated to handle the current. The formula to calculate this is:

Output Capacitor Ripple Current (RMS)

$$I_{RIPPLE}\ (RMS) = I_{OUT}\sqrt{\frac{DC}{1-DC}}$$

$$= I_{OUT}\sqrt{\frac{V_{OUT}-V_{IN}}{V_{IN}}}$$

Input Capacitors

The input capacitor of a boost converter is less critical due to the fact that the input current waveform is triangular and does not contain large squarewave currents as is found in the output capacitor. Capacitors in the range of 10µF to 100µF with an ESR of 0.3Ω or less work well up to full 1.5A switch current. Higher ESR capacitors may be acceptable at low switch currents. Input capacitor ripple current for boost converter is :

$$I_{RIPPLE} = \frac{0.3(V_{IN})(V_{OUT}-V_{IN})}{(f)(L)(V_{OUT})}$$

f = 500kHz Switching frequency (LT1372) or,
1MHz Switching frequency (LT1377)

The input capacitor can see a very high surge current whe a battery or high capacitance source is connected "live and solid tantalum capacitors can fail under this conditior Several manufacturers have developed a line of soli tantalum capacitors specially tested for surge capabilit (AVX TPS series, for instance), but even these units ma fail if the input voltage approaches the maximum voltag rating of the capacitor. AVX recommends derating capac tor voltage by 2:1 for high surge applications. Ceramic an aluminum electrolytic capacitors may also be used an have a high tolerance to turn-on surges.

Ceramic Capacitors

Higher value, lower cost ceramic capacitors are no\ becoming available in smaller case sizes. These are temp ing for switching regulator use because of their very lo\ ESR. Unfortunately, the ESR is so low that it can caus loop stability problems. Solid tantalum capacitor ES generates a loop "zero" at 5kHz to 50kHz that is instrumer tal in giving acceptable loop phase margin. Ceramic ca pacitors remain capacitive to beyond 300kHz and usuall resonate with their ESL before ESR becomes effectiv\ They are appropriate for input bypassing because of the high ripple current ratings and tolerance of turn-on surge\ Linear Technology plans to issue a Design Note on the us of ceramic capacitors in the near future.

Output Diode

The suggested output diode (D1) is a 1N5818 Schottky c its Motorola equivalent, MBR130. It is rated at 1A averag forward current and 30V reverse voltage. Typical forwar voltage is 0.42V at 1A. The diode conducts current onl during switch off time. Peak reverse voltage for boo\ converters is equal to regulator output voltage. Averag forward current in normal operation is equal to outpu current.

APPLICATIONS INFORMATION

Frequency Compensation

Loop frequency compensation is performed on the output of the error amplifier (V_C pin) with a series RC network. The main pole is formed by the series capacitor and the output impedance (≈500kΩ) of the error amplifier. The pole falls in the range of 2Hz to 20Hz. The series resistor creates a "zero" at 1kHz to 5kHz, which improves loop stability and transient response. A second capacitor, typically one-tenth the size of the main compensation capacitor, is sometimes used to reduce the switching frequency ripple on the V_C pin. V_C pin ripple is caused by output voltage ripple attenuated by the output divider and multiplied by the error amplifier. Without the second capacitor, V_C pin ripple is:

$$V_C \text{ Pin Ripple} = \frac{1.245(V_{RIPPLE})(g_m)(R_C)}{(V_{OUT})}$$

V_{RIPPLE} = Output ripple (V_{P-P})
g_m = Error amplifier transconductance (≈1500μmho)
R_C = Series resistor on V_C pin
V_{OUT} = DC output voltage

To prevent irregular switching, V_C pin ripple should be kept below 50mV_{P-P}. Worst-case V_C pin ripple occurs at maximum output load current and will also be increased if poor quality (high ESR) output capacitors are used. The addition of a 0.0047μF capacitor on the V_C pin reduces switching frequency ripple to only a few millivolts. A low value for R_C will also reduce V_C pin ripple, but loop phase margin may be inadequate.

Switch Node Considerations

For maximum efficiency, switch rise and fall time are made as short as possible. To prevent radiation and high frequency resonance problems, proper layout of the components connected to the switch node is essential. B field (magnetic) radiation is minimized by keeping output diode, switch pin, and output bypass capacitor leads as short as possible. E field radiation is kept low by minimizing the length and area of all traces connected to the switch pin. A ground plane should always be used under the switcher circuitry to prevent interplane coupling.

The high speed switching current path is shown schematically in Figure 3. Minimum lead length in this path is essential to ensure clean switching and low EMI. The path including the switch, output diode, and output capacitor is the only one containing nanosecond rise and fall times. Keep this path as short as possible.

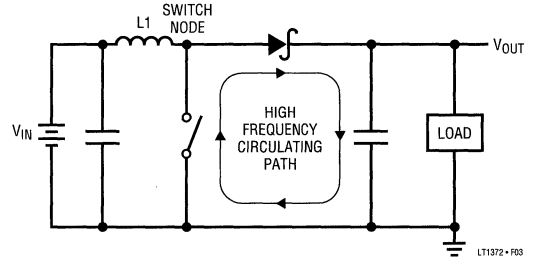


Figure 3

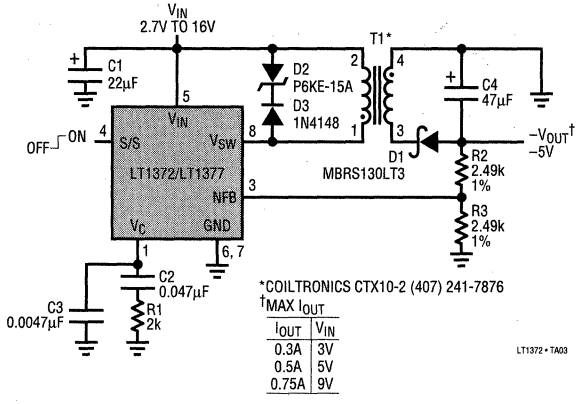
More Help

For more detailed information on switching regulator circuits, please see Application Note 19. Linear Technology also offers a computer software program, SwitcherCAD, to assist in designing switching converters. SwitcherCAD will be updated in late 1995 for the LT1372 and LT1377. In addition, our applications department is always ready to lend a helping hand.

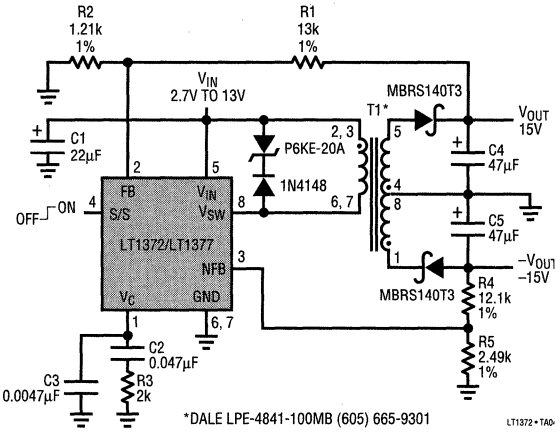
4

TYPICAL APPLICATIONS

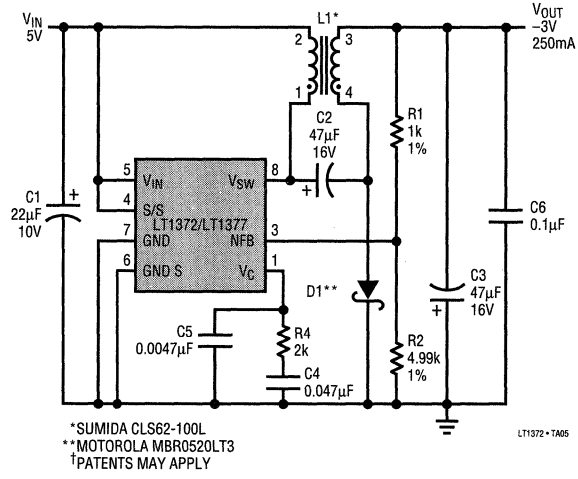
Positive-to-Negative Converter with Direct Feedback



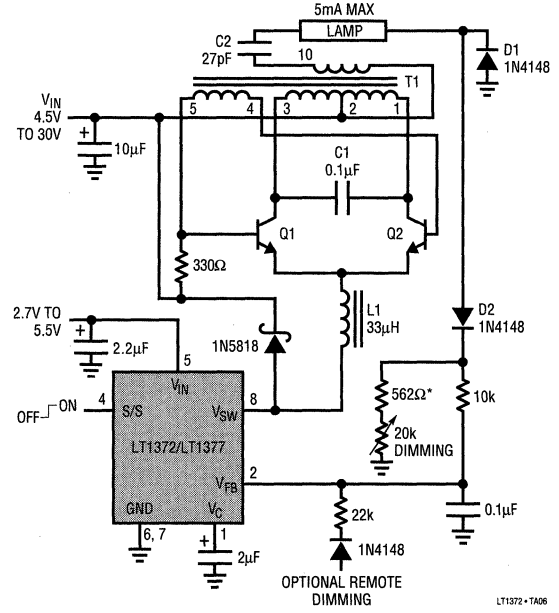
Dual Output Flyback Converter with Overvoltage Protection



Low Ripple 5V to –3V "Cuk"† Converter



90% Efficient CCFL Supply



C1 = WIMA MKP-20
L1 = COILCRAFT DT3316-333
Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
T1 = COILTRONICS CTX 110609
* = 1% FILM RESISTOR

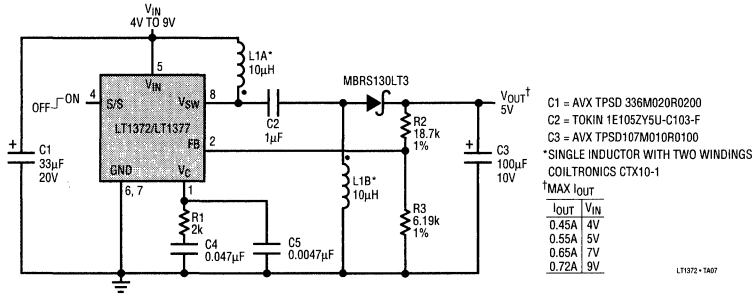
DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (407) 241-7876
COILCRAFT (708) 639-6400

CCFL BACKLIGHT APPLICATION CIRCUITS CONTAINED IN THIS DATA SHEET ARE COVERED BY U.S. PATENT NUMBER 5408162 AND OTHER PATENTS PENDING

TYPICAL APPLICATIONS

2 Li-Ion Cell to 5V SEPIC Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1172	100kHz 1.25A Boost Switching Regulator	Good for Up to V_{IN} = 40V
LTC®1265	12V 1.2A Monolithic Buck Converter	Converts 5V to 3.3V at 1A with 90% Efficiency
LT1302	Micropower 2A Boost Converter	Converts 2V to 5V at 600mA in SO8 Packages
LT1376	500kHz 1.5A Buck Switching Regulator	Steps Down from Up to 25V Using 4.7µH Inductors
LT1373	Low Supply Current 250kHz 1.5A Boost Switching Regulator	90% Efficient Boost Converter with Constant Frequency

4

250kHz Low Supply Current High Efficiency 1.5A Switching Regulator

FEATURES

- **1mA I_Q at 250kHz**
- **Uses Small Inductors: 15µH**
- All Surface Mount Components
- Only 0.6 Square Inch of Board Space
- Low Minimum Supply Voltage: 2.7V
- Constant Frequency Current Mode
- Current Limited Power Switch: 1.5A
- Regulates Positive or Negative Outputs
- Shutdown Supply Current: 12µA Typ
- Easy External Synchronization
- 8-Pin SO or PDIP Packages

APPLICATIONS

- Boost Regulators
- CCFL Backlight Driver
- Laptop Computer Supplies
- Multiple Output Flyback Supplies
- Inverting Supplies

DESCRIPTION

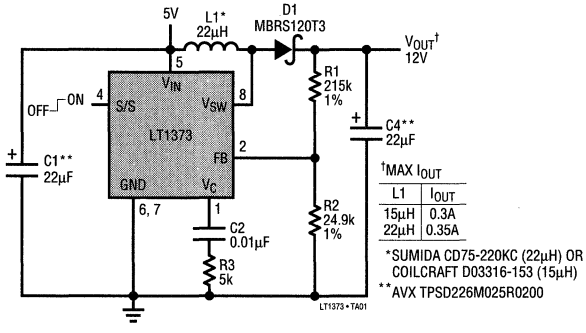
The LT®1373 is a low supply current high frequency current mode switching regulator. It can be operated in all standard switching configurations including boost, buck, flyback, forward, inverting and "Cuk." A 1.5A high efficiency switch is included on the die, along with all oscillator, control, and protection circuitry. All functions of the LT1373 are integrated into 8-pin SO/PDIP packages.

Compared to the 500kHz LT1372, which draws 4mA of quiescent current, the LT1373 switches at 250kHz, typically consumes only 1mA and has higher efficiency. High frequency switching allows for small inductors to be used. All surface mount components consume less than 0.6 square inch of board space.

New design techniques increase flexibility and maintain ease of use. Switching is easily synchronized to an external logic level source. A logic low on the shutdown pin reduces supply current to 12µA. Unique error amplifier circuitry can regulate positive or negative output voltage while maintaining simple frequency compensation techniques. Nonlinear error amplifier transconductance reduces output overshoot on start-up or overload recovery. Oscillator frequency shifting protects external components during overload conditions.

TYPICAL APPLICATION

5V-to-12V Boost Converter



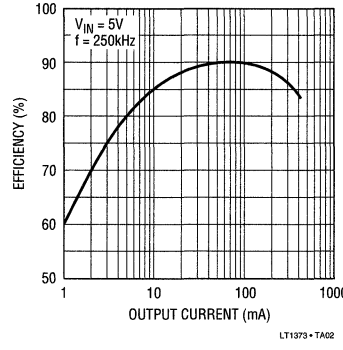
†MAX I_{OUT}

L1	I_{OUT}
15µH	0.3A
22µH	0.35A

*SUMIDA CD75-220KC (22µH) OR COILCRAFT D03316-153 (15µH)

**AVX TPSD226M025R0200

12V Output Efficiency

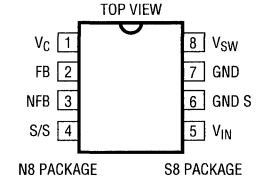


ABSOLUTE MAXIMUM RATINGS

Supply Voltage 30V
Switch Voltage 35V
S/S Pin Voltage 30V
Feedback Pin Voltage (Transient, 10ms) ..... ±10V
Feedback Pin Current 10mA
Negative Feedback Pin Voltage
(Transient, 10ms) ..... ±10V
Operating Junction Temperature Range
Operating ..... 0°C to 125°C*
Short Circuit ..... 0°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

*Units shipped prior to Date Code 9552 are rated at 100°C maximum operating temperature.

PACKAGE/ORDER INFORMATION



T_{JMAX} = 125°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 120°C/W (S8)

ORDER PART NUMBER
LT1373CN8 LT1373CS8
S8 PART MARKING
1373

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, V_{SW}, S/S and NFB pins open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin V_C = 0.8V	 ●	1.230 1.225	1.245 1.245	1.260 1.265	V V
I_{FB}	Feedback Input Current	V_{FB} = V_{REF}	 ●		50	150 275	nA nA
	Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.03	%/V
V_{NFR}	Negative Feedback Reference Voltage	Measured at Negative Feedback Pin Feedback Pin Open, V_C = 0.8V	 ●		–2.490 –2.490		V V
I_{NFB}	Negative Feedback Input Current	V_{NFB} = V_{NFR}	●	–12	–7	–2	µA
	Negative Feedback Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.05	%/V
g_m	Error Amplifier Transconductance	ΔI_C = ±5µA	 ●	250 150	375	500 600	µmho µmho
	Error Amplifier Source Current	V_{FB} = V_{REF} – 150mV, V_C = 1.5V	●	25	50	90	µA
	Error Amplifier Sink Current	V_{FB} = V_{REF} + 150mV, V_C = 1.5V	●		850	1500	µA
	Error Amplifier Clamp Voltage	High Clamp, V_{FB} = 1V Low Clamp, V_{FB} = 1.5V		1.70 0.25	1.95 0.40	2.30 0.52	V V
A_V	Error Amplifier Voltage Gain				250		V/V
	V_C Pin Threshold	Duty Cycle = 0%		0.8	1	1.25	V
f	Switching Frequency	2.7V ≤ V_{IN} ≤ 25V	 ●	225 210	250 250	275 290	kHz kHz
	Maximum Switch Duty Cycle		●	90	95		%
	Switch Current Limit Blanking Time				340	500	ns
BV	Output Switch Breakdown Voltage	2.7V ≤ V_{IN} ≤ 25V	●	35	47		V
V_{SAT}	Output Switch "On" Resistance	I_{SW} = 1A	●		0.5	0.85	Ω

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, V_{SW}, S/S and NFB pins open, unless otherwise noted.

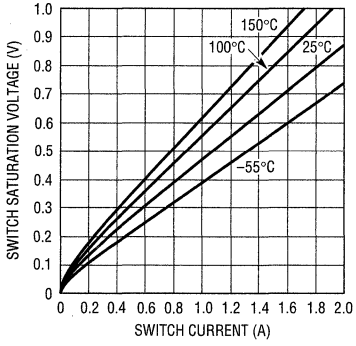
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{LIM}	Switch Current Limit	Duty Cycle = 50% Duty Cycle = 80% (Note 1)	● ●	1.5 1.3	1.9 1.7	2.4 2.2	A A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time				10	20	mA/A
	Control Voltage to Switch Current Transconductance				2		A/V
	Minimum Input Voltage		●		2.4	2.7	V
I_Q	Supply Current	2.7V ≤ V_{IN} ≤ 25V	●		1	1.5	mA
	Shutdown Supply Current	2.7V ≤ V_{IN} ≤ 25V, $V_{S/S}$ ≤ 0.6V	●		12	30	µA
	Shutdown Threshold	2.7V ≤ V_{IN} ≤ 25V	●	0.6	1.3	2	V
	Shutdown Delay		●	5	12	100	µs
	S/S Pin Input Current	0V ≤ $V_{S/S}$ ≤ 5V	●	–10		12	µA
	Synchronization Frequency Range		●	300		360	kHz

The ● denotes specifications which apply over the full operating temperature range.

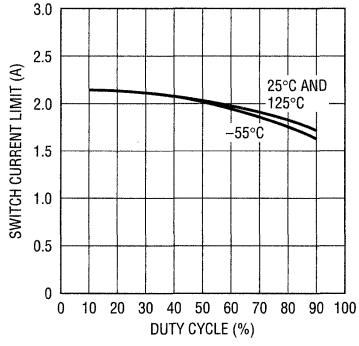
Note 1: For duty cycles (DC) between 50% and 90%, minimum guaranteed switch current is given by I_{LIM} = 0.667 (2.75 – DC).

TYPICAL PERFORMANCE CHARACTERISTICS

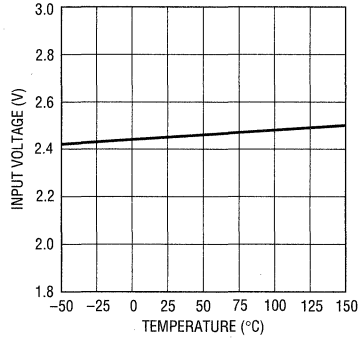
Switch Saturation Voltage vs Switch Current



Switch Current Limit vs Duty Cycle

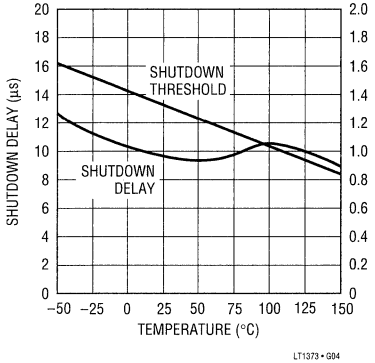


Minimum Input Voltage vs Temperature

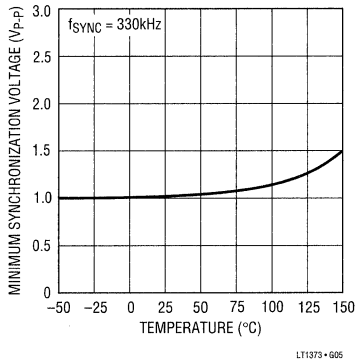


TYPICAL PERFORMANCE CHARACTERISTICS

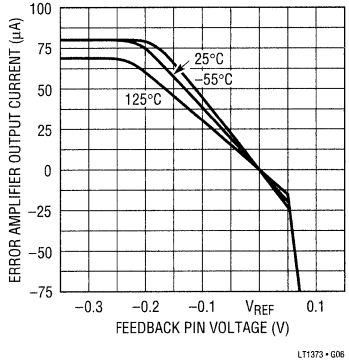
Shutdown Delay and Threshold vs Temperature



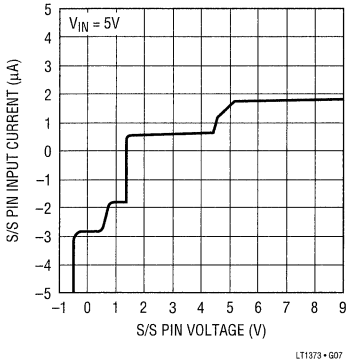
Minimum Synchronization Voltage vs Temperature



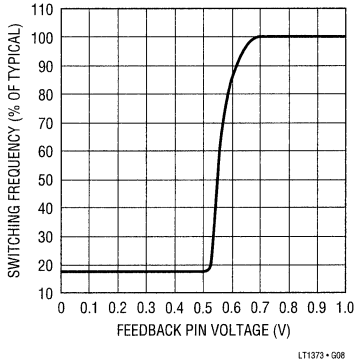
Error Amplifier Output Current vs Feedback Pin Voltage



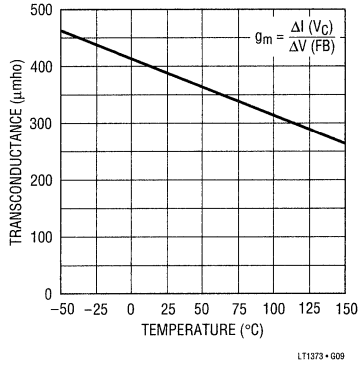
S/S Pin Input Current vs Voltage



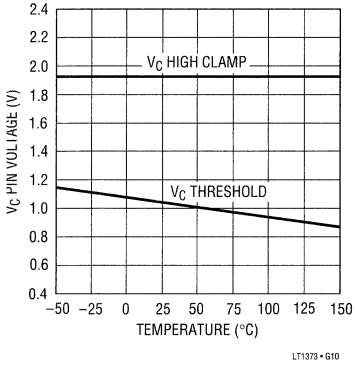
Switching Frequency vs Feedback Pin Voltage



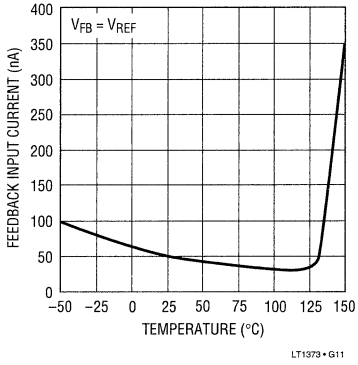
Error Amplifier Transconductance vs Temperature



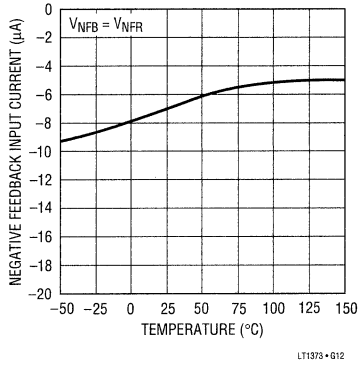
V_C Pin Threshold and High Clamp Voltage vs Temperature



Feedback Input Current vs Temperature



Negative Feedback Input Current vs Temperature



PIN FUNCTIONS

V_C (Pin 1): Compensation Pin. The V_C pin is used for frequency compensation, current limiting and soft start. It is the output of the error amplifier and the input of the current comparator. Loop frequency compensation can be performed with an RC network connected from the V_C pin to ground.

FB (Pin 2): The feedback pin is used for positive output voltage sensing and oscillator frequency shifting. It is the inverting input to the error amplifier. The noninverting input of this amplifier is internally tied to a 1.245V reference.

NFB (Pin 3): The negative feedback pin is used for negative output voltage sensing. It is connected to the inverting input of the negative feedback amplifier through a 400k source resistor.

S/S (Pin 4): Shutdown and Synchronization Pin. The S/S pin is logic level compatible. Shutdown is active low and the shutdown threshold is typically 1.3V. For normal operation, pull the S/S pin high, tie it to V_{IN} or leave it floating. To synchronize switching, drive the S/S pin between 300kHz and 360kHz.

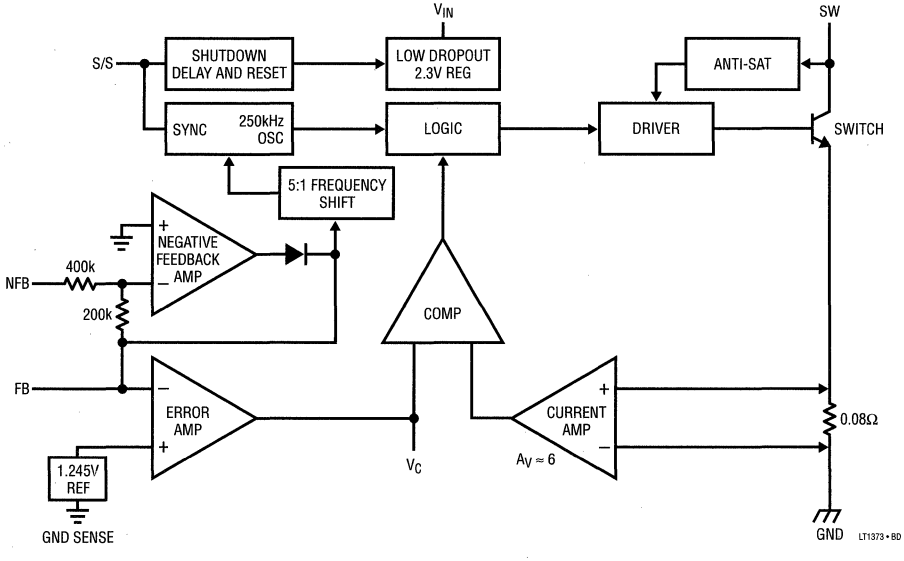
V_{IN} (Pin 5): Input Supply Pin. Bypass V_{IN} with 10µF or more. The part goes into undervoltage lockout when V_{IN} drops below 2.5V. Undervoltage lockout stops switching and pulls the V_C pin low.

GND S (Pin 6): The ground sense pin is a "clean" ground. The internal reference, error amplifier and negative feedback amplifier are referred to the ground sense pin. Connect it to ground. Keep the ground path connection to the output resistor divider and the V_C compensation network free of large ground currents.

GND (Pin 7): The ground pin is the emitter connection of the power switch and has large currents flowing through it. It should be connected directly to a good quality ground plane.

V_{SW} (Pin 8): The switch pin is the collector of the power switch and has large currents flowing through it. Keep the traces to the switching components as short as possible to minimize radiation and voltage spikes.

BLOCK DIAGRAM



OPERATION

The LT1373 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "On" at the start of each oscillator cycle. It is turned "Off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike voltage mode switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry. This low dropout design allows input voltage to vary from 2.7V to 25V with virtually no change in device performance. A 250kHz oscillator is the basic clock for all internal timing. It turns "On" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.245V bandgap reference biases the positive input of the error amplifier. The negative input of the amplifier is brought out for positive output voltage sensing. The error amplifier has nonlinear transconductance to reduce output overshoot on start-up or overload recovery. When the feedback voltage exceeds the reference by 40mV, error amplifier transconductance increases ten times, which reduces output overshoot. The feedback input also invokes oscillator frequency shifting, which helps protect components during overload conditions. When the feedback voltage drops below 0.6V, the oscillator frequency is reduced 5:1. Lower switching frequency allows full control of switch current limit by reducing minimum switch duty cycle.

Unique error amplifier circuitry allows the LT1373 to directly regulate negative output voltages. The negative feedback amplifier's 400k source resistor is brought out for negative output voltage sensing. The NFB pin regulates at –2.49V while the amplifier output internally drives the FB pin to 1.245V. This architecture, which uses the same main error amplifier, prevents duplicating functions and maintains ease of use. (Consult Linear Technology Marketing for units that can regulate down to –1.25V.)

The error signal developed at the amplifier output is brought out externally. This pin (V_C) has three different functions. It is used for frequency compensation, current limit adjustment and soft starting. During normal regulator operation this pin sits at a voltage between 1V (low output current) and 1.9V (high output current). The error amplifier is a current output (g_m) type, so this voltage can be externally clamped for lowering current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled below the control pin threshold, placing the LT1373 in an idle mode.

APPLICATIONS INFORMATION

Positive Output Voltage Setting

The LT1373 develops a 1.245V reference (V_{REF}) from the FB pin to ground. Output voltage is set by connecting the FB pin to an output resistor divider (Figure 1). The FB pin bias current represents a small error and can usually be ignored for values of R2 up to 25k. The suggested value for R2 is 24.9k. The NFB pin is normally left open for positive output applications. Positive fixed voltage versions are available. (Consult Linear Technology Marketing.)

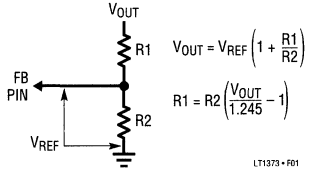


Figure 1. Positive Output Resistor Divider

APPLICATIONS INFORMATION

Negative Output Voltage Setting

The LT1373 develops a –2.49V reference (V_{NFR}) from the NFB pin to ground. Output voltage is set by connecting the NFB pin to an output resistor divider (Figure 2). The –7µA NFB pin bias current (I_{NFB}) can cause output voltage errors and should not be ignored. This has been accounted for in the formula in Figure 2. The suggested value for R2 is 2.49k. The FB pin is normally left open for negative output applications.

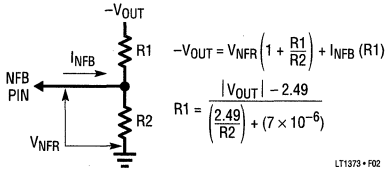


Figure 2. Negative Output Resistor Divider

Dual Polarity Output Voltage Sensing

Certain applications benefit from sensing both positive and negative output voltages. One example is the Dual Output Flyback Converter with Overvoltage Protection circuit shown in the Typical Applications section. Each output voltage resistor divider is individually set as described above. When both the FB and NFB pins are used, the LT1373 acts to prevent either output from going beyond its set output voltage. For example in this application, if the positive output were more heavily loaded than the negative, the negative output would be greater and would regulate at the desired set-point voltage. The positive output would sag slightly below its set-point voltage. This technique prevents either output from going unregulated high at no load.

Shutdown and Synchronization

The dual function S/S pin provides easy shutdown and synchronization. It is logic level compatible and can be pulled high, tied to V_{IN} or left floating for normal operation. A logic low on the S/S pin activates shutdown, reducing the part's supply current to 12µA. Typical synchronization range is from 1.05 and 1.8 times the part's natural switching frequency, but is only guaranteed between 300kHz and 360kHz. A 12µs resetable shutdown delay network guarantees the part will not go into shutdown while receiving a synchronization signal.

Caution should be used when synchronizing above 330kHz because at higher sync frequencies the amplitude of the internal slope compensation used to prevent subharmonic switching is reduced. This type of subharmonic switching only occurs when the duty cycle of the switch is above 50%. Higher inductor values will tend to eliminate problems.

Thermal Considerations

Care should be taken to ensure that the worst-case input voltage and load current conditions do not cause excessive die temperatures. The packages are rated at 120°C/W for SO (S8) and 130°C/W for PDIP (N8).

Average supply current (including driver current) is:

$I_{IN} = 1mA + DC (I_{SW}/60 + I_{SW} \times 0.004)$

I_{SW} = switch current

DC = switch duty cycle

Switch power dissipation is given by:

$P_{SW} = (I_{SW})^2 \times R_{SW} \times DC$

R_{SW} = output switch "On" resistance

Total power dissipation of the die is the sum of supply current times supply voltage plus switch power:

$P_{D(TOTAL)} = (I_{IN} \times V_{IN}) + P_{SW}$

Choosing the Inductor

For most applications the inductor will fall in the range of 10µH to 50µH. Lower values are chosen to reduce physical size of the inductor. Higher values allow more output current because they reduce peak current seen by the power switch which has a 1.5A limit. Higher values also reduce input ripple voltage, and reduce core loss.

When choosing an inductor you might have to consider maximum load current, core and copper losses, allowable component height, output voltage ripple, EMI, fault current in the inductor, saturation, and of course, cost. The following procedure is suggested as a way of handling these somewhat complicated and conflicting requirements.

APPLICATIONS INFORMATION

1. Assume that the average inductor current (for a boost converter) is equal to load current times V_{OUT}/V_{IN} and decide whether or not the inductor must withstand continuous overload conditions. If average inductor current at maximum load current is 0.5A, for instance, a 0.5A inductor may not survive a continuous 1.5A overload condition. Also, be aware that boost converters are not short-circuit protected, and that under output short conditions, inductor current is limited only by the available current of the input supply.

2. Calculate peak inductor current at full load current to ensure that the inductor will not saturate. Peak current can be significantly higher than output current, especially with smaller inductors and lighter loads, so don't omit this step. Powered iron cores are forgiving because they saturate softly, whereas ferrite cores saturate abruptly. Other core materials fall in between somewhere. The following formula assumes continuous mode operation, but it errors only slightly on the high side for discontinuous mode, so it can be used for all conditions.

$$I_{PEAK} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2(f)(L)(V_{OUT})}$$

V_{IN} = minimum input voltage
f = 250kHz switching frequency

3. Decide if the design can tolerate an "open" core geometry like a rod or barrel, which have high magnetic field radiation, or whether it needs a closed core like a toroid to prevent EMI problems. One would not want an open core next to a magnetic storage media for instance! This is a tough decision because the rods or barrels are temptingly cheap and small, and there are no helpful guidelines to calculate when the magnetic field radiation will be a problem.

4. Start shopping for an inductor which meets the requirements of core shape, peak current (to avoid saturation), average current (to limit heating), and fault current, (if the inductor gets too hot, wire insulation will melt and cause turn-to-turn shorts). Keep in mind that all good things like high efficiency, low profile and high temperature operation will increase cost, sometimes dramatically.

5. After making an initial choice, consider the secondary things like output voltage ripple, second sourcing, etc. Use the experts in the Linear Technology application department if you feel uncertain about the final choice. They have experience with a wide range of inductor types and can tell you about the latest developments in low profile, surface mounting, etc.

Output Capacitor

The output capacitor is normally chosen by its effective series resistance (ESR), because this is what determines output ripple voltage. At 500kHz, any polarized capacitor is essentially resistive. To get low ESR takes *volume*, so physically smaller capacitors have high ESR. The ESR range for typical LT1373 applications is 0.05Ω to 0.5Ω. A typical output capacitor is an AVX type TPS, 22µF at 25V, with a guaranteed ESR less than 0.2Ω. This is a "D" size surface mount solid tantalum capacitor. TPS capacitors are specially constructed and tested for low ESR, so they give the lowest ESR for a given volume. To further reduce ESR, multiple output capacitors can be used in parallel. The value in microfarads is not particularly critical and values from 22µF to greater than 500µF work well, but you cannot cheat mother nature on ESR. If you find a tiny 22µF solid tantalum capacitor, it will have high ESR and output ripple voltage will be terrible. Table 1 shows some typical solid tantalum surface mount capacitors.

Table 1. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

E CASE SIZE	ESR (MAX Ω)	RIPPLE CURRENT (A)
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.7 to 0.9	0.4
D CASE SIZE		
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.9 to 2.0	0.36 to 0.24
C CASE SIZE		
AVX TPS	0.2 (Typ)	0.5 (Typ)
AVX TAJ	1.8 to 3.0	0.22 to 0.17
B CASE SIZE		
AVX TAJ	2.5 to 10	0.16 to 0.08

Many engineers have heard that solid tantalum capacitors are prone to failure if they undergo high surge currents. This is historically true and type TPS capacitors are

APPLICATIONS INFORMATION

specially tested for surge capability, but surge ruggedness is not a critical issue with the *output* capacitor. Solid tantalum capacitors fail during very high *turn-on* surges, which do not occur at the output of regulators. High *discharge* surges, such as when the regulator output is dead shorted, do not harm the capacitors.

Single inductor boost regulators have large RMS ripple current in the output capacitor, which must be rated to handle the current. The formula to calculate this is:

Output Capacitor Ripple Current (RMS)

$$I_{RIPPLE}\ (RMS) = I_{OUT}\sqrt{\frac{DC}{1-DC}}$$

$$= I_{OUT}\sqrt{\frac{V_{OUT}-V_{IN}}{V_{IN}}}$$

Input Capacitors

The input capacitor of a boost converter is less critical due to the fact that the input current waveform is triangular, and does not contain large squarewave currents as is found in the output capacitor. Capacitors in the range of 10µF to 100µF with an ESR (effective series resistance) of 0.3Ω or less work well up to a full 1.5A switch current. Higher ESR capacitors may be acceptable at low switch currents. Input capacitor ripple current for boost converter is:

$$I_{RIPPLE} = \frac{0.3(V_{IN})(V_{OUT}-V_{IN})}{(f)(L)(V_{OUT})}$$

f = 250kHz switching frequency

The input capacitor can see a very high surge current when a battery or high capacitance source is connected "live", and solid tantalum capacitors can fail under this condition. Several manufacturers have developed a line of solid tantalum capacitors specially tested for surge capability (AVX TPS series, for instance), but even these units may fail if the input voltage approaches the maximum voltage rating of the capacitor. AVX recommends derating capacitor voltage by 2:1 for high surge applications. Ceramic and aluminum electrolytic capacitors may also be used and have a high tolerance to turn-on surges.

Ceramic Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. These are tempting for switching regulator use because of their very low ESR. Unfortunately, the ESR is so low that it can cause loop stability problems. Solid tantalum capacitor ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before ESR becomes effective. They are appropriate for input bypassing because of their high ripple current ratings and tolerance of turn-on surges. Linear Technology plans to issue a Design Note on the use of ceramic capacitors in the near future.

Output Diode

The suggested output diode (D1) is a 1N5818 Schottky or its Motorola equivalent, MBR130. It is rated at 1A average forward current and 30V reverse voltage. Typical forward voltage is 0.42V at 1A. The diode conducts current only during switch-off time. Peak reverse voltage for boost converters is equal to regulator output voltage. Average forward current in normal operation is equal to output current.

Frequency Compensation

Loop frequency compensation is performed on the output of the error amplifier (V_C pin) with a series R_C network. The main pole is formed by the series capacitor and the output impedance (≈1MΩ) of the error amplifier. The pole falls in the range of 5Hz to 30Hz. The series resistor creates a "zero" at 2kHz to 10kHz, which improves loop stability and transient response. A second capacitor, typically one tenth the size of the main compensation capacitor, is sometimes used to reduce the switching frequency ripple on the V_C pin. V_C pin ripple is caused by output voltage ripple attenuated by the output divider and multiplied by the error amplifier. Without the second capacitor, V_C pin ripple is:

$$V_C\ \text{Pin Ripple} = \frac{1.245(V_{RIPPLE})(g_m)(R_C)}{V_{OUT}}$$

APPLICATIONS INFORMATION

V_{RIPPLE} = output ripple (V_{P-P})
g_m = error amplifier transconductance (≈375μmho)
R_C = series resistor on V_C pin
V_{OUT} = DC output voltage

To prevent irregular switching, V_C pin ripple should be kept below $50mV_{P-P}$. Worst-case V_C pin ripple occurs at maximum output load current and will also be increased if poor quality (high ESR) output capacitors are used. The addition of a 0.001μF capacitor on the V_C pin reduces switching frequency ripple to only a few millivolts. A low value for R_C will also reduce V_C pin ripple, but loop phase margin may be inadequate.

Switch Node Considerations

For maximum efficiency, switch rise and fall time are made as short as possible. To prevent radiation and high frequency resonance problems, proper layout of the components connected to the switch node is essential. B field (magnetic) radiation is minimized by keeping output diode, switch pin and output bypass capacitor leads as short as possible. E field radiation is kept low by minimizing the length and area of all traces connected to the switch pin. A ground plane should always be used under the switcher circuitry to prevent interplane coupling.

The high speed switching current path is shown schematically in Figure 3. Minimum lead length in this path is essential to ensure clean switching and low EMI. The path including the switch, output diode and output capacitor is the only one containing nanosecond rise and fall times. Keep this path as short as possible.

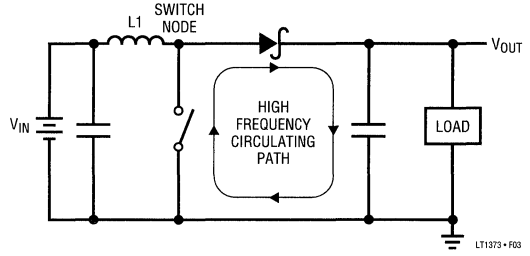


Figure 3

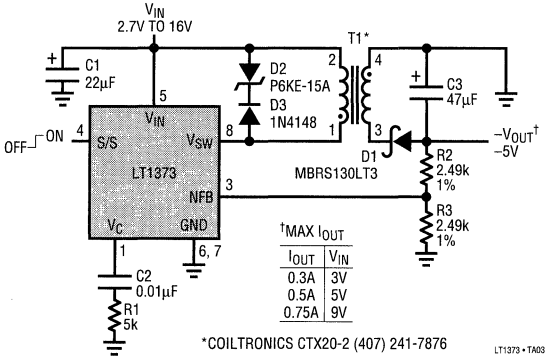
More Help

For more detailed information on switching regulator circuits, please see AN19. Linear Technology also offers a computer software program, SwitcherCAD, to assist in designing switching converters. SwitcherCAD will be updated in late 1995 for the LT1373. In addition, our applications department is always ready to lend a helping hand.

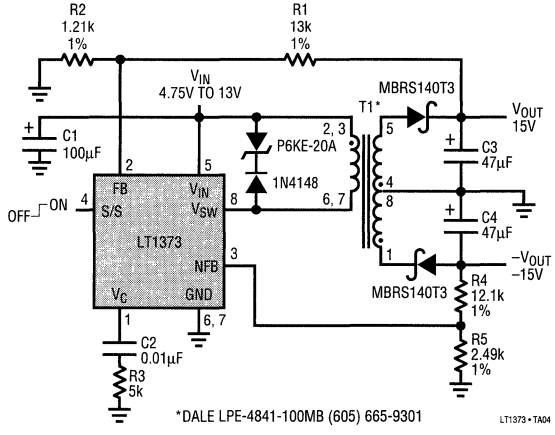
4

TYPICAL APPLICATIONS

Positive-to-Negative Converter with Direct Feedback

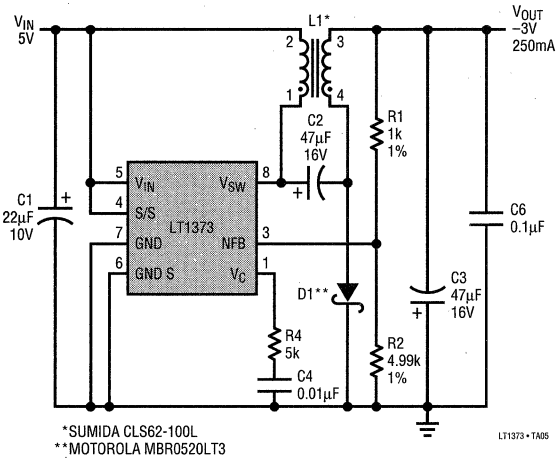


Dual Output Flyback Converter with Overvoltage Protection



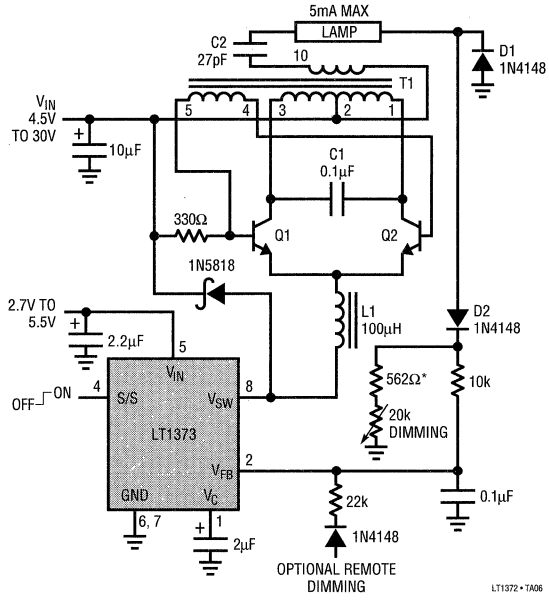
TYPICAL APPLICATIONS

Low Ripple 5V to –3V "Cuk"† Converter



*SUMIDA CLS62-100L
**MOTOROLA MBR0520LT3
†PATENTS MAY APPLY

90% Efficient CCFL Supply



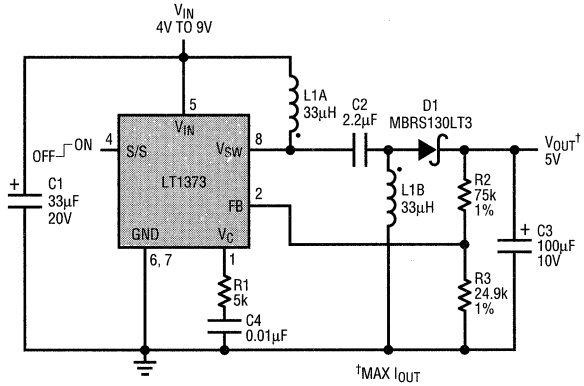
C1 = WIMA MKP-20
L1 = COILCRAFT D03316-104
Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
T1 = COILTRONICS CTX 110609
* = 1% FILM RESISTOR

DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (407) 241-7876
COILCRAFT (708) 639-6400

CCFL BACKLIGHT APPLICATION CIRCUITS CONTAINED IN THIS DATA SHEET ARE COVERED BY U.S. PATENT NUMBER 5408162 AND OTHER PATENTS PENDING

Two Li-Ion Cells to 5V SEPIC Conveter



C1 = AVX TPSD 336M020R0200
C2 = TOKIN 1E225ZY5U-C203-F
C3 = AVX TPSD 107M010R0100
L1 = COILTRONICS CTX33-2, SINGLE INDUCTOR WITH TWO WINDINGS

†MAX I_{OUT}

I_{OUT}	V_{IN}
0.45A	4V
0.55A	5V
0.65A	7V
0.72A	9V

LT1373 • TA07

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1172	100kHz 1.25A Boost Switching Regulator	Also for Flyback, Buck and Inverting Configurations
LTC®1265	13V 1.2A Monolithic Buck Converter	Includes PMOS Switch On-Chip
LT1302	Micropower 2A Boost Converter	Converts 2V to 5V at 600mA
LT1372	500kHz 1.5A Boost Switching Regulator	Also Regulates Negative Flyback Outputs
LT1376	500kHz 1.5A Buck Switching Regulator	Handles Up to 25V Inputs
LT1377	1MHz 1.5A Boost Switching Regulator	Only 1MHz Integrated Switching Regulator Available

1.5A, 500kHz Step-Down Switching Regulators

FEATURES

- **Constant 500kHz Switching Frequency**
- Easily Synchronizable
- **Uses All Surface Mount Components**
- **Inductor Size Reduced to 5μH**
- Saturating Switch Design: 0.4Ω
- Effective Supply Current: 2.5mA
- Shutdown Current: 20μA
- Cycle-by-Cycle Current Limiting

APPLICATIONS

- Portable Computers
- Battery-Powered Systems
- Battery Charger
- Distributed Power

DESCRIPTION

The LT®1375/LT1376 are 500kHz monolithic buck mode switching regulators. A 1.5A switch is included on the die along with all the necessary oscillator, control, and logic circuitry. High switching frequency allows a considerable reduction in the size of external components. The topology is current mode for fast transient response and good loop stability. Both fixed output voltage and adjustable parts are available.

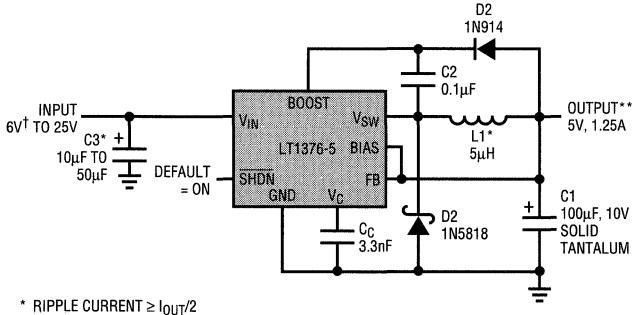
A special high speed bipolar process and new design techniques achieve high efficiency at high switching frequency. Efficiency is maintained over a wide output current range by using the output to bias the circuitry and by utilizing a supply boost capacitor to saturate the power switch. A shutdown signal will reduce supply current to 20μA on both parts. The LT1375 can be externally synchronized from 550kHz to 1MHz with logic level inputs.

The LT1375/LT1376 fit into standard 8-pin PDIP and SO packages. Full cycle-by-cycle short-circuit protection and thermal shutdown are provided. Standard surface mount external parts are used, including the inductor and capacitors.

For low input voltage applications with 3.3V output, see LT1507. This is a functionally identical part that can operate with input voltages between 4.5V and 12V.

TYPICAL APPLICATION

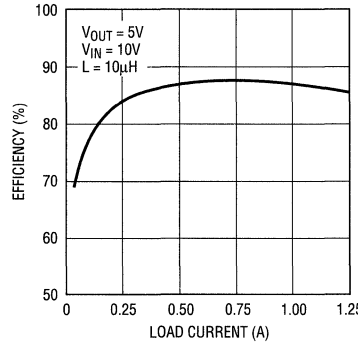
5V Buck Converter



* RIPPLE CURRENT ≥ $I_{OUT}/2$
** INCREASE L1 TO 10μH FOR LOAD CURRENTS ABOVE 0.6A AND TO 20μH ABOVE 1A
† FOR INPUT VOLTAGE BELOW 7.5V, SOME RESTRICTIONS MAY APPLY. SEE APPLICATIONS INFORMATION.

1375/76 TA01

Efficiency vs Load Current



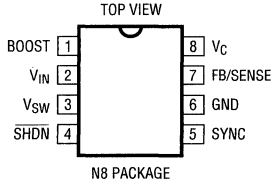
1375/76 TA02

ABSOLUTE MAXIMUM RATINGS

nput Voltage 25V
3oost Pin Voltage 35V
SHDN Pin Voltage 7V
3ias Pin Voltage 7V
FB Pin Voltage (Adjustable Part) 3.5V
FB Pin Current (Adjustable Part) 1mA
Sense Voltage (Fixed 5V Part) 7V
Sync Pin Voltage 7V

Operating Ambient Temperature Range
LT1375C/LT1376C ..... 0°C to 70°C
LT1375I/LT1376I ..... –40°C to 85°C
Operating Junction Temperature Range
LT1375C/LT1376C ..... 0°C to 125° C
LT1375I/LT1376I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

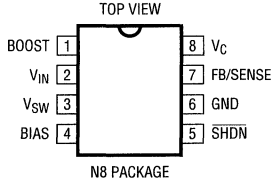


N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

θ_{JA} = 100°C/W (N8)
θ_{JA} = 120°C/W TO 150°C/W DEPENDING ON PC BOARD LAYOUT (S8)

ORDER PART NUMBER
LT1375CN8
LT1375CN8-5
LT1375CS8
LT1375CS8-5
LT1375IN8
LT1375IN8-5
LT1375IS8
LT1375IS8-5
S8 PART MARKING
1375
13755
1375I
1375I5



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

θ_{JA} = 100°C/W (N8)
θ_{JA} = 120°C/W TO 150°C/W DEPENDING ON PC BOARD LAYOUT (S8)

ORDER PART NUMBER
LT1376CN8
LT1376CN8-5
LT1376CS8
LT1376CS8-5
LT1376IN8
LT1376IN8-5
LT1376IS8
LT1376IS8-5
S8 PART MARKING
1376
13765
1376I
1376I5

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

T_J = 25°C, V_{IN} = 15V, V_C = 1.5V, boost open, switch open, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Voltage (Adjustable)			2.39	2.42	2.45	V
	All Conditions	●	2.36		2.48	V
Sense Voltage (Fixed 5V)			4.94	5.0	5.06	V
	All Conditions	●	4.90		5.10	V
Sense Pin Resistance			7	10	14	kΩ
Reference Voltage Line Regulation	5V ≤ V_{IN} ≤ 25V			0.01	0.03	%/V
Feedback Input Bias Current		●		0.5	1.5	µA
Error Amplifier Voltage Gain	$V_{\overline{SHDN}}$ = 1V (Notes 1, 7)		200	400		
Error Amplifier Transconductance	$V_{\overline{SHDN}}$ = 1V, ΔI (V_C) = ±10µA (Note 7)		1500	2000	2700	µMho
		●	1100		3000	µMho

ELECTRICAL CHARACTERISTICS

T_J = 25°C, V_{IN} = 15V, V_C = 1.5V, boost open, switch open, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_C Pin to Switch Current Transconductance				2		A/V
Error Amplifier Source Current	$V_{\overline{SHDN}}$ = 1V, V_{FB} = 2.7V or V_{SENSE} = 4.4V	●	150	225	280	µA
Error Amplifier Sink Current	$V_{\overline{SHDN}}$ = 1V, V_{FB} = 2.7V or V_{SENSE} = 5.6V			2		mA
V_C Pin Switching Threshold	Duty Cycle = 0			0.9		V
V_C Pin High Clamp	$V_{\overline{SHDN}}$ = 1V			2.1		V
Switch Current Limit	V_C Open, V_{FB} = 2.1V or V_{SENSE} = 4.4V, V_{BOOST} = V_{IN} + 5V DC ≤ 50%	●	1.50	2	3	A
	DC = 80%	●	1.35		3	A
Switch On Resistance (Note 6)	I_{SW} = 1.5A, V_{BOOST} = V_{IN} + 5V			0.3	0.4	Ω
		●			0.5	Ω
Maximum Switch Duty Cycle	V_{FB} = 2.1V or V_{SENSE} = 4.4V		90	93		%
	−55°C ≤ T_J ≤ 125°C		86	93		%
	T_J = 150°C		85	93		%
Switch Frequency	V_C Set to Give 50% Duty Cycle		460	500	540	kHz
	−25°C ≤ T_J ≤ 150°C		440		560	kHz
	T_J ≤ −25°C		440		570	kHz
Switch Frequency Line Regulation	5V ≤ V_{IN} ≤ 25V	●		0.05	0.15	%/V
Frequency Shifting Threshold on FB Pin	Δf = 10kHz	●	0.8	1.0	1.3	V
Minimum Input Voltage (Note 2)		●		5.0	5.5	V
Minimum Boost Voltage (Note 3)	I_{SW} ≤ 1.5A	●		3	3.5	V
Boost Current (Note 4)	V_{BOOST} = V_{IN} + 5V I_{SW} = 500mA	●		12	22	mA
	I_{SW} = 1.5A	●		25	35	mA
Input Supply Current (Note 5)	V_{BIAS} = 5V	●		0.9	1.4	mA
Output Supply Current (Note 5)	V_{BIAS} = 5V	●		3.2	4.0	mA
Shutdown Supply Current	$V_{\overline{SHDN}}$ = 0V, V_{IN} ≤ 25V, V_{SW} = 0V, V_C Open			15	50	µA
		●			75	µA
Lockout Threshold	V_C Open	●	2.3	2.38	2.46	V
Shutdown Thresholds	V_C Open Device Shutting Down	●	0.15	0.37	0.60	V
	Device Starting Up	●	0.25	0.45	0.60	V
Minimum Synchronizing Amplitude (LT1375 Only)	V_{IN} = 5V	●		1.5	2.2	V
Synchronizing Range (LT1375 Only)			580		900	kHz
Sync Pin Input Resistance				40		kΩ

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Gain is measured with a V_C swing equal to 200mV above the low clamp level to 200mV below the upper clamp level.

Note 2: Minimum input voltage is not measured directly, but is guaranteed by other tests. It is defined as the voltage where internal bias lines are still regulated so that the reference voltage and oscillator frequency remain constant. Actual minimum input voltage to maintain a regulated output will depend on output voltage and load current. See Applications Information.

Note 3: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

Note 4: Boost current is the current flowing into the boost pin with the pin held 5V above input voltage. It flows only during switch-on time.

Note 5: Input supply current is the bias current drawn by the input pin when the bias pin is held at 5V with switching disabled. Output supply current is the current drawn by the bias pin when the bias pin is held at 5V. Total input referred supply current is calculated by summing input supply current (I_{SI}) with a fraction of output supply current (I_{SO}):

$$I_{TOT} = I_{SI} + (I_{SO})(V_{OUT}/V_{IN})(1.15)$$

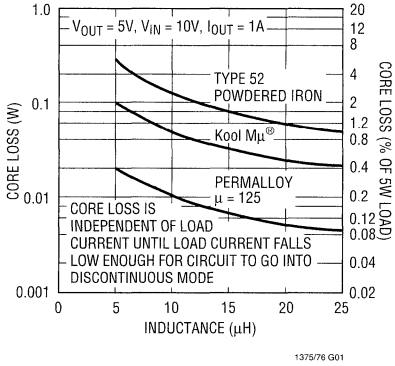
With V_{IN} = 15V, V_{OUT} = 5V, I_{SI} = 0.9mA, I_{SO} = 3.6mA, I_{TOT} = 2.28mA.

Note 6: Switch-on resistance is calculated by dividing V_{IN} to V_{SW} voltage by the forced current (1.5A). See Typical Performance Characteristics for the graph of switch voltage at other currents.

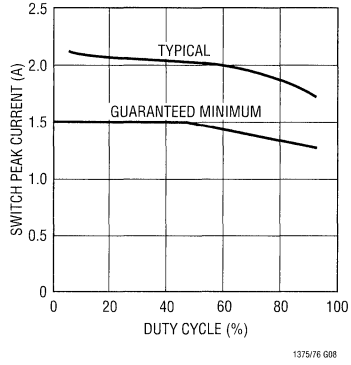
Note 7: Transconductance and voltage gain refer to the internal amplifier exclusive of the voltage divider. To calculate gain and transconductance refer to sense pin on fixed voltage parts. Divide values shown by the ratio V_{OUT}/2.42.

TYPICAL PERFORMANCE CHARACTERISTICS

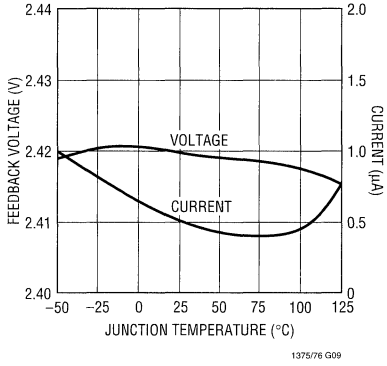
Inductor Core Loss



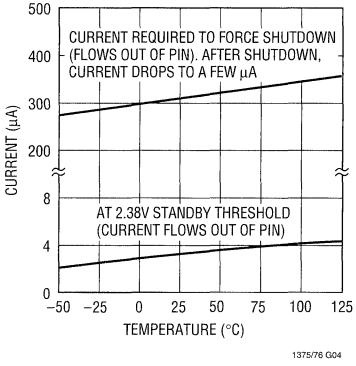
Switch Peak Current Limit



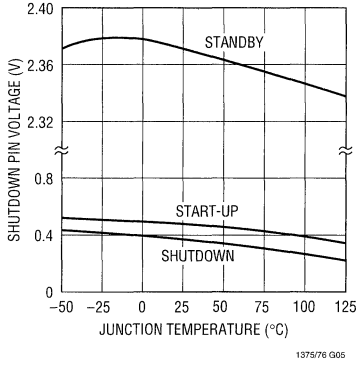
Feedback Pin Voltage and Current



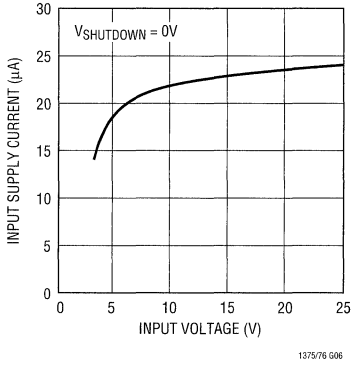
Shutdown Pin Bias Current



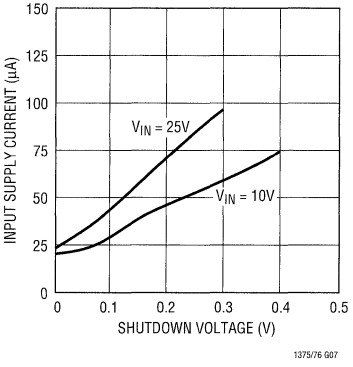
Standby and Shutdown Thresholds



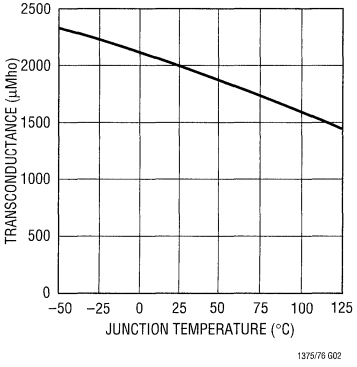
Shutdown Supply Current



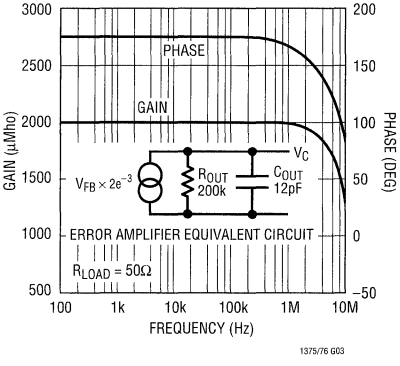
Shutdown Supply Current



Error Amplifier Transconductance



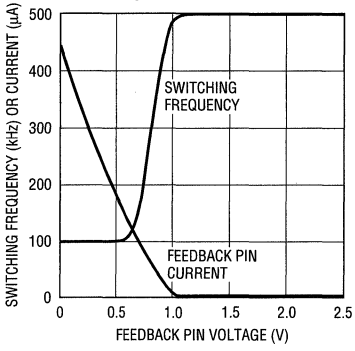
Error Amplifier Transconductance



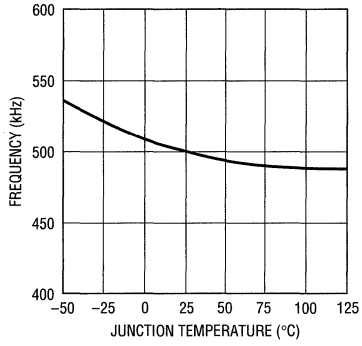
Kool Mμ is a registered trademark of Magnetics, Inc.

TYPICAL PERFORMANCE CHARACTERISTICS

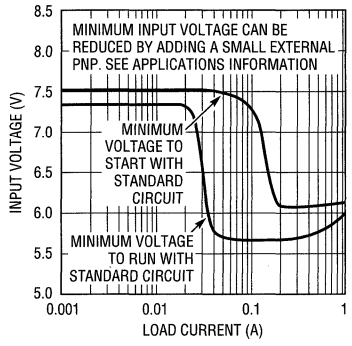
Frequency Foldback



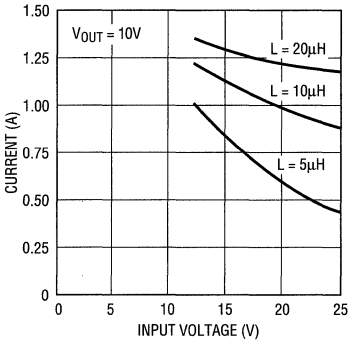
Switching Frequency



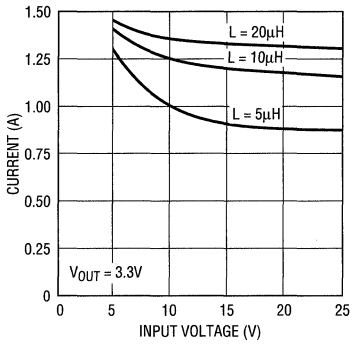
LT1376 Minimum Input Voltage with 5V Output



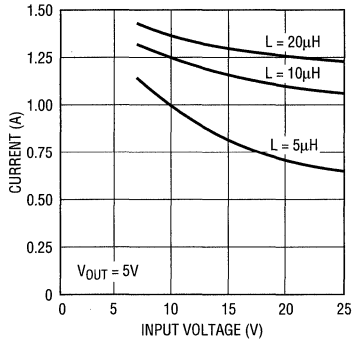
Maximum Load Current at V_{OUT} = 10V



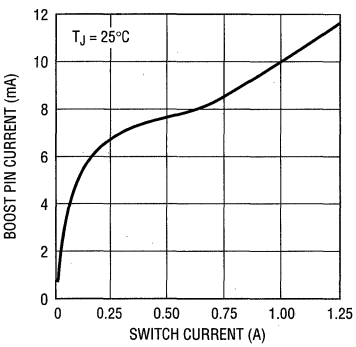
Maximum Load Current at V_{OUT} = 3.3V



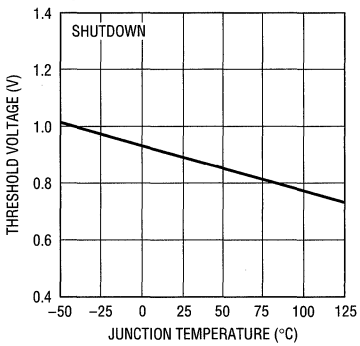
Maximum Load Current at V_{OUT} = 5V



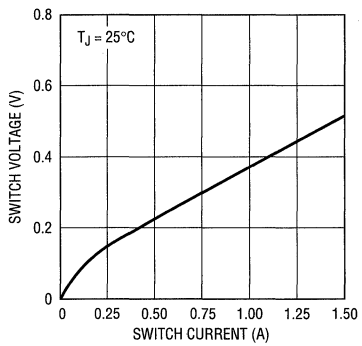
Boost Pin Current



V_C Pin Shutdown Threshold



Switch Voltage Drop



PIN FUNCTIONS

BOOST (Pin 1): The boost pin is used to provide a drive voltage, higher than the input voltage, to the internal bipolar NPN power switch. Without this added voltage, the typical switch voltage loss would be about 1.5V. The additional boost voltage allows the switch to saturate and voltage loss approximates that of a 0.3Ω FET structure, but with much smaller die area. Efficiency improves from 75% for conventional bipolar designs to > 87% for these new parts.

V_{SW} (Pin 3): The switch pin is the emitter of the on-chip power NPN switch. It is driven up to the input pin voltage during switch on time. Inductor current drives the switch pin negative during switch off time. Negative voltage is clamped with the external catch diode. Maximum negative switch voltage allowed is –0.8V.

$\overline{SHDN}$ (Pin 4 for LT1375, Pin 5 for LT1376): The shutdown pin is used to turn off the regulator and to reduce input drain current to a few microamperes. Actually, this pin has two separate thresholds, one at 2.38V to disable switching, and a second at 0.4V to force complete micropower shutdown. The 2.38V threshold functions as an accurate undervoltage lockout (UVLO). This is sometimes used to prevent the regulator from operating until the input voltage has reached a predetermined level.

BIAS (Pin 4, LT1376 Only): The bias pin is used to improve efficiency when operating at higher input voltages and light load current. Connecting this pin to the regulated output voltage forces most of the internal circuitry to draw its operating current from the output voltage rather than the input supply. This is a much more efficient way of doing business if the input voltage is much higher than the output. *Minimum output voltage setting for this mode of operation is 3.3V.* Efficiency improvement at V_{IN} = 20V, V_{OUT} = 5V, and I_{OUT} = 25mA is over 10%.

SYNC (Pin 5, LT1375 Only): The sync pin is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 10% and 90% duty cycle. The synchronizing range is equal to *initial* operating frequency, up to 900kHz. See Synchronizing section in Applications Information for details.

FB/SENSE (Pin 7): The feedback pin is used to set output voltage, using an external voltage divider that generates 2.42V at the pin with the desired output voltage. The fixed voltage (-5) parts have the divider included on the chip, and the FB pin is used as a sense pin, connected directly to the 5V output. Two additional functions are performed by the FB pin. When the pin voltage drops below 1.7V, switch current limit is reduced. Below 1V, switching frequency is also reduced. See Feedback Pin Function section in Applications Information for details.

V_C (Pin 8): The V_C pin is the output of the error amplifier and the input of the peak switch current comparator. It is normally used for frequency compensation, but can do double duty as a current clamp or control loop override. This pin sits at about 1V for very light loads and 2V at maximum load. It can be driven to ground to shut off the regulator, but if driven high, current must be limited to 4mA.

BLOCK DIAGRAM

The LT1376 is a constant frequency, current mode buck converter. This means that there is an internal clock and two feedback loops that control the duty cycle of the power switch. In addition to the normal error amplifier, there is a current sense amplifier that monitors switch current on a cycle-by-cycle basis. A switch cycle starts with an oscillator pulse which sets the RS flip-flop to turn the switch on. When switch current reaches a level set by the inverting input of the comparator, the flip-flop is reset and the switch turns off. Output voltage control is obtained by using the output of the error amplifier to set the switch current trip point. This technique means that the error amplifier commands current to be delivered to the output rather than voltage. A voltage fed system will have low phase shift up to the resonant frequency of the inductor and output capacitor, then an abrupt 180° shift will occur. The current fed system will have 90° phase shift at a much lower frequency, but will not have the additional 90° shift

BLOCK DIAGRAM

until well beyond the LC resonant frequency. This makes it much easier to frequency compensate the feedback loop and also gives much quicker transient response.

Most of the circuitry of the LT1376 operates from an internal 2.9V bias line. The bias regulator normally draws power from the regulator input pin, but if the BIAS pin is connected to an external voltage higher than 3V, bias power will be drawn from the external source (typically the regulated output voltage). This will improve efficiency if the bias pin voltage is lower than regulator input voltage.

High switch efficiency is attained by using the boost pin to provide a voltage to the switch driver which is higher than the input voltage, allowing switch to be saturated. This boosted voltage is generated with an external capacitor and diode. Two comparators are connected to the shutdown pin. One has a 2.38V threshold for undervoltage lockout and the second has a 0.4V threshold for complete shutdown.

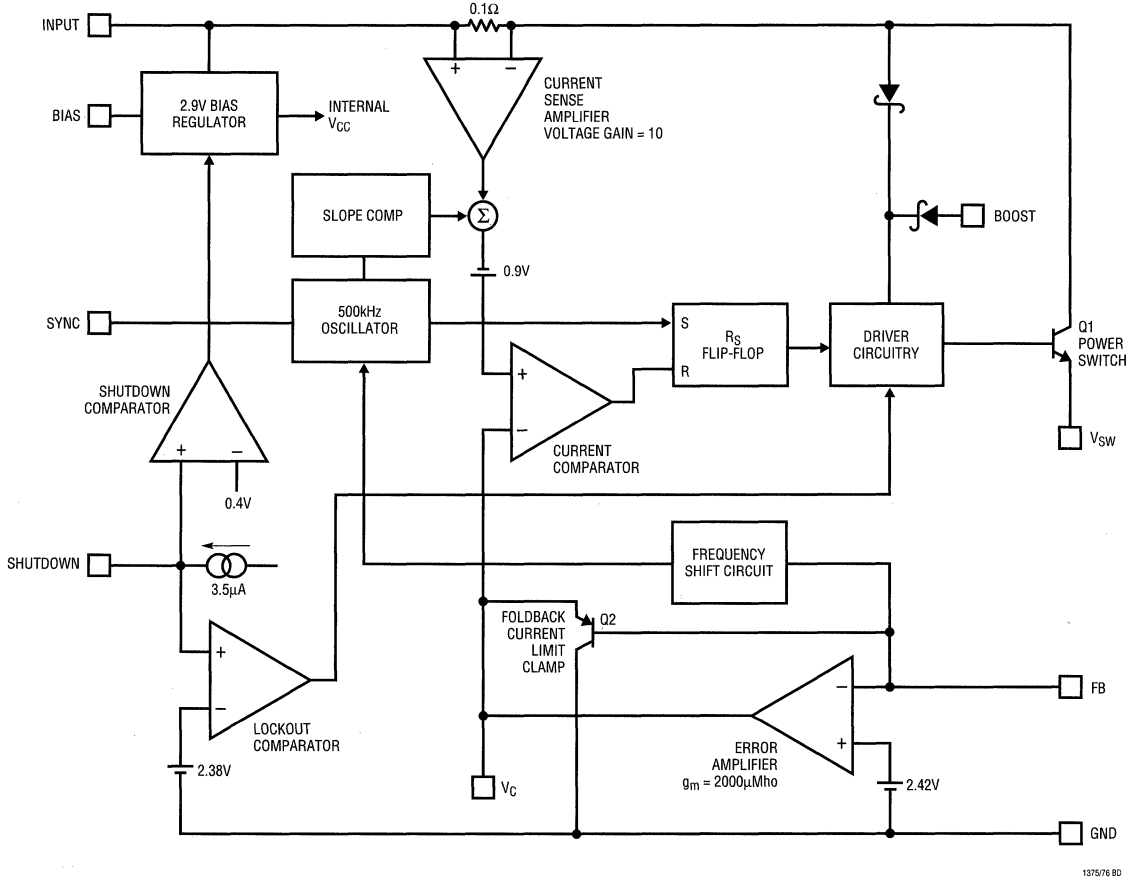


Figure 1. Block Diagram

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FEEDBACK PIN FUNCTIONS

The feedback (FB) pin on the LT1376 is used to set output voltage and also to provide several overload protection features. The first part of this section deals with selecting resistors to set output voltage and the remaining part talks about foldback frequency and current limiting created by the FB pin. Please read both parts before committing to a final design. The fixed 5V LT1376-5 has internal divider resistors and the FB pin is renamed SENSE, connected directly to the output.

The suggested value for the output divider resistor (see Figure 2) from FB to ground (R2) is 5k or less, and a formula for R1 is shown below. The output voltage error caused by ignoring the input bias current on the FB pin is less than 0.25% with R2 = 5k. A table of standard 1% values is shown in Table 1 for common output voltages. Please read the following if divider resistors are increased above the suggested values.

$$R1 = \frac{R2\left(V_{OUT} - 2.42\right)}{2.42}$$

Table 1.

OUTPUT VOLTAGE (V)	R2 (kΩ)	R1 (NEAREST 1%) (kΩ)	% ERROR AT OUTPUT DUE TO DISCREET 1% RESISTOR STEPS
3	4.99	1.21	+0.23
3.3	4.99	1.82	+0.08
5	4.99	5.36	+0.39
6	4.99	7.32	−0.5
8	4.99	11.5	−0.04
10	4.99	15.8	+0.83
12	4.99	19.6	−0.62
15	4.99	26.1	+0.52

More Than Just Voltage Feedback

The feedback pin is used for more than just output voltage sensing. It also reduces switching frequency and current limit when output voltage is very low (see the Frequency Foldback graph in Typical Performance Characteristics). This is done to control power dissipation in both the IC and in the external diode and inductor during short-circuit conditions. A shorted output requires the switching regulator to operate at very low duty cycles, and the average current through the diode and inductor is equal to the short-circuit current limit of the switch (typically 2A for the

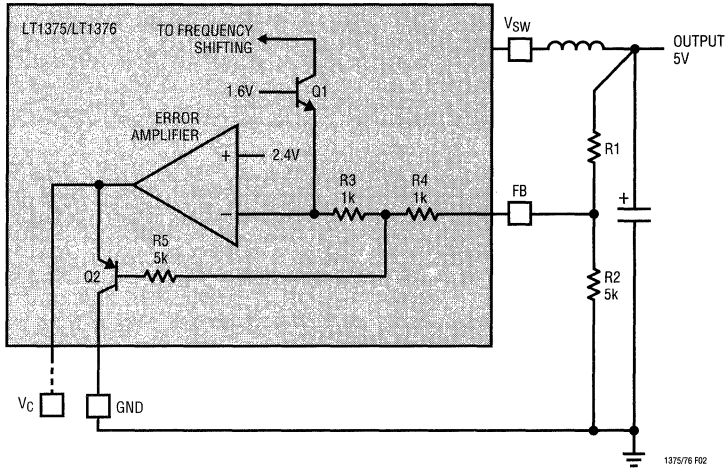

Figure 2. Frequency and Current Limit Foldback

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LT1376, folding back to less than 1A). Minimum switch on time limitations would prevent the switcher from attaining a sufficiently low duty cycle if switching frequency were maintained at 500kHz, so frequency is reduced by about 5:1 when the feedback pin voltage drops below 1V (see Frequency Foldback graph). This does not affect operation with normal load conditions; one simply sees a gear shift in switching frequency during start-up as the output voltage rises.

In addition to lower switching frequency, the LT1376 also operates at lower switch current limit when the feedback pin voltage drops below 1.7V. Q2 in Figure 2 performs this function by clamping the V_C pin to a voltage less than its normal 2.3V upper clamp level. This *foldback current limit* greatly reduces power dissipation in the IC, diode and inductor during short-circuit conditions. Again, it is nearly transparent to the user under normal load conditions. The only loads which may be affected are current source loads which maintain full load current with output voltage less than 50% of final value. In these rare situations the feedback pin can be clamped above 1.5V with an external diode to defeat foldback current limit. *Caution:* clamping the feedback pin means that frequency shifting will also be defeated, so a combination of high input voltage and dead shorted output may cause the LT1376 to lose control of current limit.

The internal circuitry which forces reduced switching frequency also causes current to flow out of the feedback pin when output voltage is low. The equivalent circuitry is shown in Figure 2. Q1 is completely off during normal operation. If the FB pin falls below 1V, Q1 begins to conduct current and reduces frequency at the rate of approximately 5kHz/μA. To ensure adequate frequency foldback (under worst-case short-circuit conditions), the external divider Thevinin resistance must be low enough to pull 150μA out of the FB pin with 0.6V on the pin ($R_{DIV} \leq 4k$). *The net result is that reductions in frequency and current limit are affected by output voltage divider impedance. Although divider impedance is not critical, caution should be used if resistors are increased beyond the suggested values and short-circuit conditions will occur with high input voltage.* High frequency pickup will increase and the protection accorded by frequency and current foldback will decrease.

MAXIMUM OUTPUT LOAD CURRENT

Maximum load current for a buck converter is limited by the maximum switch current rating (I_P) of the LT1376. This current rating is 1.5A up to 50% duty cycle (DC), decreasing to 1.35A at 80% duty cycle. This is shown graphically in Typical Performance Characteristics and as shown in the formula below:

$I_P = 1.5A$ for $DC \leq 50\%$

$I_P = 1.65A - 0.15\,(DC) - 0.26\,(DC)^2$ for $50\% < DC < 90\%$

DC = Duty cycle = V_{OUT}/V_{IN}

Example: with $V_{OUT} = 5V$, $V_{IN} = 8V$; DC = 5/8 = 0.625, and;

$$I_{SW(MAX)} = 1.64 - 0.15\,(0.625) - 0.26\,(0.625)^2 = 1.44A$$

Current rating decreases with duty cycle because the LT 1376 has internal slope compensation to prevent current mode subharmonic switching. For more details, read Application Note 19. The LT1376 is a little unusual in this regard because it has nonlinear slope compensation which gives better compensation with less reduction in current limit.

Maximum load current would be equal to maximum switch current *for an infinitely large inductor*, but with finite inductor size, maximum load current is reduced by one-half peak-to-peak inductor current. The following formula assumes continuous mode operation, implying that the term on the right is less than one-half of I_P.

$$I_{OUT(MAX)} = \text{Continuous Mode} \qquad I_P - \frac{(V_{OUT})(V_{IN} - V_{OUT})}{2(L)(f)(V_{IN})}$$

For the conditions above;

$$I_{OUT(MAX)} = 1.44 - \frac{(5)(8-5)}{2\left(10e^{-6}\right)\left(500e^{3}\right)(8)}$$

$$= 1.44 - 0.19 = 1.25A$$

At $V_{IN} = 15V$, duty cycle is 33%, so I_P is just equal to a fixed 1.5A, and $I_{OUT(MAX)}$ is equal to:

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$$1.5-\frac{(5)(15-5)}{2(10e^{-6})(500e^{3})(15)}=1.5-0.33=1.17A$$

Note that there is less load current available at the higher input voltage because inductor ripple current increases. This is not always the case. Certain combinations of inductor value and input voltage range may yield lower available load current at the lowest input voltage due to reduced peak switch current at high duty cycles. If load current is close to the maximum available, please check maximum available current at both input voltage extremes. To calculate actual peak switch current with a given set of conditions, use:

$$I_{SW(PEAK)}=I_{OUT}+\frac{V_{OUT}(V_{IN}-V_{OUT})}{2(L)(f)(V_{IN})}$$

For lighter loads where discontinuous operation can be used, maximum load current is equal to:

$$I_{OUT(MAX)}\ \text{Discontinuous mode}=\frac{(I_P)^2(f)(L)(V_{OUT})}{2(V_{OUT})(V_{IN}-V_{OUT})}$$

Example: with L = 2μH, VOUT = 5V, and VIN(MAX) = 15V,

$$I_{OUT(MAX)}=\frac{(1.5)^2(500e^{3})(2e^{-6})(15)}{2(5)(15-5)}=338mA$$

The main reason for using such a tiny inductor is that it is physically very small, but keep in mind that peak-to-peak inductor current will be very high. This will increase output ripple voltage. If the output capacitor has to be made larger to reduce ripple voltage, the overall circuit could actually wind up larger.

CHOOSING THE INDUCTOR AND OUTPUT CAPACITOR

For most applications the output inductor will fall in the range of 3μH to 20μH. Lower values are chosen to reduce physical size of the inductor. Higher values allow more output current because they reduce peak current seen by the LT1376 switch, which has a 1.5A limit. Higher values also reduce output ripple voltage, and reduce core loss. Graphs in the Typical Performance Characteristics section show maximum output load current versus inductor size and input voltage. A second graph shows core loss versus inductor size for various core materials.

When choosing an inductor you might have to consider maximum load current, core and copper losses, allowable component height, output voltage ripple, EMI, fault current in the inductor, saturation, and of course, cost. The following procedure is suggested as a way of handling these somewhat complicated and conflicting requirements.

1. Choose a value in microhenries from the graphs of maximum load current and core loss. Choosing a small inductor with lighter loads may result in discontinuous mode of operation, but the LT1376 is designed to work well in either mode. Keep in mind that lower core loss means higher cost, at least for closed core geometries like toroids. The core loss graphs show both absolute loss and percent loss for a 5W output, so actual percent losses must be calculated for each situation.

   Assume that the average inductor current is equal to load current and decide whether or not the inductor must withstand continuous fault conditions. If maximum load current is 0.5A, for instance, a 0.5A inductor may not survive a continuous 1.5A overload condition. Dead shorts will actually be more gentle on the inductor because the LT1376 has foldback current limiting.

2. Calculate peak inductor current at full load current to ensure that the inductor will not saturate. Peak current can be significantly higher than output current, especially with smaller inductors and lighter loads, so don't omit this step. Powdered iron cores are forgiving because they saturate softly, whereas ferrite cores saturate abruptly. Other core materials fall in between somewhere. The following formula assumes continu-

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ous mode of operation, but it errs only slightly on the high side for discontinuous mode, so it can be used for all conditions.

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT}(V_{IN} - V_{OUT})}{2(f)(L)(V_{IN})}$$

V_{IN} = Maximum input voltage
f = Switching frequency, 500kHz

3. Decide if the design can tolerate an "open" core geometry like a rod or barrel, which have high magnetic field radiation, or whether it needs a closed core like a toroid to prevent EMI problems. One would not want an open core next to a magnetic storage media, for instance! This is a tough decision because the rods or barrels are temptingly cheap and small and there are no helpful guidelines to calculate when the magnetic field radiation will be a problem.
4. Start shopping for an inductor (see representative surface mount units in Table 2) which meets the requirements of core shape, peak current (to avoid saturation), average current (to limit heating), and fault current (if the inductor gets too hot, wire insulation will melt and cause turn-to-turn shorts). Keep in mind that all good things like high efficiency, low profile, and high temperature operation will increase cost, sometimes dramatically. Get a quote on the cheapest unit first to calibrate yourself on price, then ask for what you really want.
5. After making an initial choice, consider the secondary things like output voltage ripple, second sourcing, etc. Use the experts in the Linear Technology's applications department if you feel uncertain about the final choice. They have experience with a wide range of inductor types and can tell you about the latest developments in low profile, surface mounting, etc.

Table 2.

VENDOR/ PART NO.	VALUE (μH)	DC (Amps)	CORE TYPE	SERIES RESISTANCE(Ω)	CORE MATERIAL	HEIGHT (mm)
Coiltronics						
CTX5-1	5	2.3	Tor	0.027	KMμ	4.2
CTX10-1	10	1.9	Tor	0.039	KMμ	4.2
CTX20-1	20	1.0	Tor	0.137	KMμ	4.2
CTX15-2	15	1.8	Tor	0.058	KMμ	6.0
CTX20-3	20	1.5	Tor	0.093	KMμ	4.7
CTX20-4	20	2.2	Tor	0.059	KMμ	6.4
CTX5-1P	5	1.8	Tor	0.021	52	4.2
CTX10-1P	10	1.6	Tor	0.030	52	4.2
CTX15-1P	15	1.2	Tor	0.046	52	4.2
CTX20-1P	20	1.0	Tor	0.081	52	4.2
CTX20-2P	20	1.3	Tor	0.052	52	6.0
CTX20-4P	20	1.8	Tor	0.039	52	6.35
Sumida						
CDRH64	10	1.7	SC	0.084	Fer	4.5
CDRH74	22	1.2	SC	0.077	Fer	4.5
CDRH73	10	1.7	SC	0.055	Fer	3.4
CDRH73	22	1.1	SC	0.15	Fer	3.4
CD73	10	1.4	Open	0.062	Fer	3.5
CD73	18	1.1	Open	0.085	Fer	3.5
CD104	10	2.4	Open	0.041	Fer	4.0
CD104	18	1.7	Open	0.062	Fer	4.0
Gowanda						
SM20-102K	10	1.3	Open	0.038	Fer	7.0
SM20-152K	15	1.3	Open	0.049	Fer	7.0
SM20-222K	22	1.3	Open	0.059	Fer	7.0
Dale						
IHSM-4825	10	3.1	Open	0.071	Fer	5.6
IHSM-4825	22	1.7	Open	0.152	Fer	5.6
IHSM-5832	10	4.3	Open	0.053	Fer	7.1
IHSM-5832	22	2.8	Open	0.12	Fer	7.1
IHSM-7832	22	3.8	Open	0.054	Fer	7.1

Tor = Toroid
SC = Semi-closed geometry
Fer = Ferrite core material
52 = Type 52 powdered iron core material
KMμ = Kool Mμ

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Output Capacitor

The output capacitor is normally chosen by its Effective Series Resistance (ESR), because this is what determines output ripple voltage. At 500kHz, any polarized capacitor is essentially resistive. To get low ESR takes *volume*, so physically smaller capacitors have high ESR. The ESR range for typical LT1376 applications is 0.05Ω to 0.5Ω. A typical output capacitor is an AVX type TPS, 100µF at 10V, with a guaranteed ESR less than 0.1Ω. This is a "D" size surface mount solid tantalum capacitor. TPS capacitors are specially constructed and tested for low ESR, so they give the lowest ESR for a given volume. The value in microfarads is not particularly critical, and values from 22µF to greater than 500µF work well, but you cannot cheat mother nature on ESR. If you find a tiny 22µF solid tantalum capacitor, it will have high ESR, and output ripple voltage will be terrible. Table 3 shows some typical solid tantalum surface mount capacitors.

Table 3. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

Case Size	ESR (Max., Ω)	Ripple Current (A)
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.7 to 0.9	0.4
Case Size		
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.9 to 2.0	0.36 to 0.24
Case Size		
AVX TPS	0.2 (typ)	0.5 (typ)
AVX TAJ	1.8 to 3.0	0.22 to 0.17
Case Size		
AVX TAJ	2.5 to 10	0.16 to 0.08

Many engineers have heard that solid tantalum capacitors are prone to failure if they undergo high surge currents. This is historically true, and type TPS capacitors are specially tested for surge capability, but surge ruggedness is not a critical issue with the *output* capacitor. Solid tantalum capacitors fail during very high *turn-on* surges, which do not occur at the output of regulators. High *discharge* surges, such as when the regulator output is lead shorted, do not harm the capacitors.

Unlike the input capacitor, RMS ripple current in the output capacitor is normally low enough that ripple current rating is not an issue. The current waveform is triangular with a typical value of $200mA_{RMS}$. The formula to calculate this is:

Output Capacitor Ripple Current (RMS):

$$I_{RIPPLE(RMS)} = \frac{0.29(V_{OUT})(V_{IN} - V_{OUT})}{(L)(f)(V_{IN})}$$

Ceramic Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. These are tempting for switching regulator use because of their very low ESR. Unfortunately, the ESR is so low that it can cause loop stability problems. Solid tantalum capacitor's ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before ESR becomes effective. They are appropriate for input bypassing because of their high ripple current ratings and tolerance of turn-on surges. Linear Technology plans to issue a design note on the use of ceramic capacitors in the near future.

OUTPUT RIPPLE VOLTAGE

Figure 3 shows a typical output ripple voltage waveform for the LT1376. Ripple voltage is determined by the high frequency impedance of the output capacitor, and ripple current through the inductor. Peak-to-peak ripple current through the inductor into the output capacitor is:

$$I_{P-P} = \frac{(V_{OUT})(V_{IN} - V_{OUT})}{(V_{IN})(L)(f)}$$

For high frequency switchers, the sum of ripple current slew rates may also be relevant and can be calculated from:

$$\Sigma \frac{dI}{dt} = \frac{V_{IN}}{L}$$

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Peak-to-peak output ripple voltage is the sum of a *triwave* created by peak-to-peak ripple current times ESR, and a *square* wave created by parasitic inductance (ESL) and ripple current slew rate. Capacitive reactance is assumed to be small compared to ESR or ESL.

$$V_{RIPPLE} = (I_{P-P})(ESR) + (ESL)\Sigma\frac{dI}{dt}$$

Example: with V_{IN} = 10V, V_{OUT} = 5V, L = 10µH, ESR = 0.1Ω, ESL = 10nH:

$$I_{P-P} = \frac{(5)(10-5)}{(10)(10e^{-6})(500e^{3})} = 0.5A$$

$$\Sigma\frac{dI}{dt} = \frac{10}{10e^{-6}} = 1e^{6}$$

$$V_{RIPPLE} = (0.5A)(0.1) + (10e^{-9})(1e^{6})$$

$$= 0.05 + 0.01 = 60mV_{P-P}$$

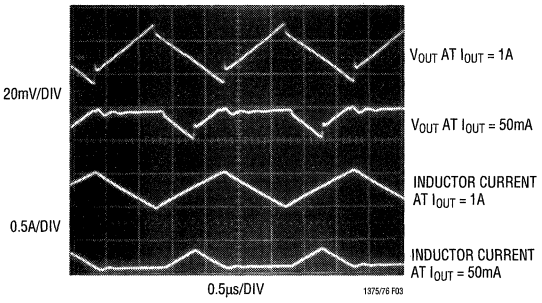

Figure 3. LT1376 Ripple Voltage Waveform

CATCH DIODE

The suggested catch diode (D1) is a 1N5818 Schottky, or its Motorola equivalent, MBR130. It is rated at 1A average forward current and 30V reverse voltage. Typical forward voltage is 0.42V at 1A. The diode conducts current only during switch off time. Peak reverse voltage is equal to regulator input voltage. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = \frac{I_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}$$

This formula will not yield values higher than 1A with maximum load current of 1.25A unless the ratio of input to output voltage exceeds 5:1. The only reason to consider a larger diode is the worst-case condition of a high input voltage and *overloaded* (not shorted) output. Under short-circuit conditions, foldback current limit will reduce diode current to less than 1A, but if the output is overloaded and does not fall to less than 1/3 of nominal output voltage, foldback will not take effect. With the overloaded condition, output current will increase to a typical value of 1.8A, determined by peak switch current limit of 2A. With V_{IN} = 15V, V_{OUT} = 4V (5V overloaded) and I_{OUT} = 1.8A:

$$I_{D(AVG)} = \frac{1.8(15-4)}{15} = 1.32A$$

This is safe for short periods of time, but it would be prudent to check with the diode manufacturer if continuous operation under these conditions must be tolerated.

BOOST PIN CONSIDERATIONS

For most applications, the boost components are a 0.1µF capacitor and a 1N914 or 1N4148 diode. The anode is connected to the regulated output voltage and this generates a voltage across the boost capacitor nearly identical to the regulated output. In certain applications, the anode may instead be connected to the unregulated input voltage. This could be necessary if the regulated output voltage is very low (< 3V) or if the input voltage is less than 6V. Efficiency is not affected by the capacitor value, but the capacitor should have an ESR of less than 2Ω to ensure that it can be recharged fully under the worst-case condition of minimum input voltage. Almost any type of film or ceramic capacitor will work fine.

WARNING! Peak voltage on the boost pin is the sum of unregulated input voltage plus the voltage across the boost capacitor. This normally means that peak boost pin voltage is equal to input voltage plus output voltage, but *when the boost diode is connected to the regulator input, peak boost pin voltage is equal to twice the input voltage.*

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Be sure that boost pin voltage does not exceed its maximum rating.

For nearly all applications, a 0.1uF boost capacitor works just fine, but for the curious, more details are provided here. The size of the boost capacitor is determined by switch drive current requirements. During switch on time, drain current on the capacitor is approximately 10mA + I_{OUT}/75. At peak load current of 1.25A, this gives a total drain of 27mA. Capacitor ripple voltage is equal to the product of on time and drain current divided by capacitor value; $\Delta V = t_{ON} \times 27mA/C$. To keep capacitor ripple voltage to less than 0.5V (a slightly arbitrary number) at the worst-case condition of t_{ON} = 1.8µs, the capacitor needs to be 0.1µF. Boost capacitor ripple voltage is not a critical parameter, but if the minimum voltage across the capacitor drops to less than 3V, the power switch may not saturate fully and efficiency will drop. An *approximate* formula for absolute minimum capacitor value is:

$$C_{MIN} = \frac{(10mA + I_{OUT}/75)(V_{OUT}/V_{IN})}{(f)(V_{OUT} - 3V)}$$

f = Switching frequency
V_{OUT} = Regulated output voltage
V_{IN} = Minimum input voltage

This formula can yield capacitor values substantially less than 0.1µF, but it should be used with caution since it does not take into account secondary factors such as capacitor series resistance, capacitance shift with temperature and output overload.

SHUTDOWN FUNCTION AND UNDERVOLTAGE LOCKOUT

Figure 4 shows how to add undervoltage lockout (UVLO) to the LT1376. Typically, UVLO is used in situations where the input supply is *current limited*, or has a relatively high source resistance. A switching regulator draws constant power from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. UVLO prevents the regulator from operating at source voltages where these problems might occur.

Threshold voltage for lockout is about 2.38V, slightly less than the internal 2.42V reference voltage. A 3.5µA bias current flows *out* of the pin at threshold. This internally generated current is used to force a default high state on the shutdown pin if the pin is left open. When low shutdown current is not an issue, the error due to this current can be minimized by making R_{LO} 10k or less. If shutdown current is an issue, R_{LO} can be raised to 100k, but the error due to initial bias current and changes with temperature should be considered.

$$R_{LO} = 10k \text{ to } 100k \ (25k \text{ suggested})$$

$$R_{HI} = \frac{R_{LO}(V_{IN} - 2.38V)}{2.38V - R_{LO}(3.5\mu A)}$$

V_{IN} = Minimum input voltage

Keep the connections from the resistors to the shutdown pin short and make sure that interplane or surface capacitance to the switching nodes are minimized. If high resistor values are used, the shutdown pin should be bypassed with a 1000pF capacitor to prevent coupling problems from the switch node. If hysteresis is desired in the undervoltage lockout point, a resistor R_{FB} can be added to the output node. Resistor values can be calculated from:

$$R_{HI} = \frac{R_{LO}\left[V_{IN} - 2.38\left(\Delta V/V_{OUT} + 1\right) + \Delta V\right]}{2.38 - R2(3.5\mu A)}$$

$$R_{FB} = (R_{HI})(V_{OUT}/\Delta V)$$

25k suggested for R_{LO}
V_{IN} = Input voltage at which switching stops as input voltage descends to trip level
ΔV = Hysteresis in input voltage level

Example: output voltage is 5V, switching is to stop if input voltage drops below 12V and should not restart unless input rises back to 13.5V. ΔV is therefore 1.5V and V_{IN} = 12V. Let R_{LO} = 25k.

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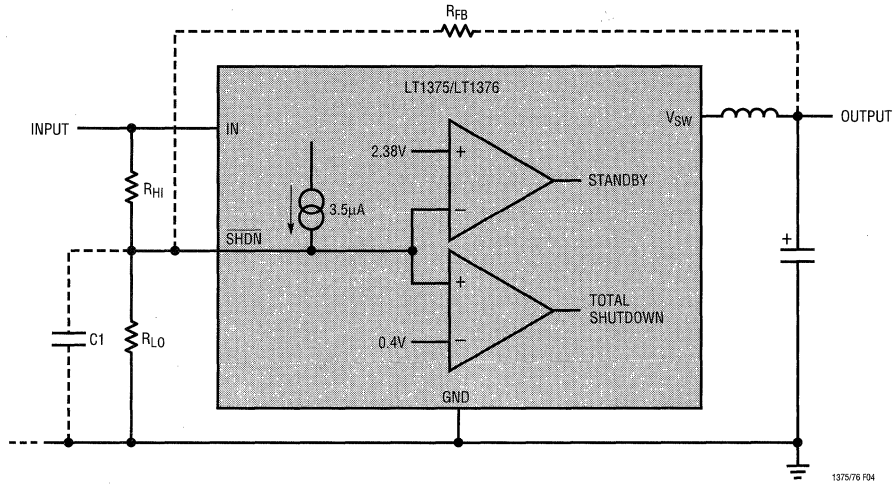

Figure 4. Undervoltage Lockout

$$R_{HI} = \frac{25k\left[12 - 2.38\left(1.5/5 + 1\right) + 1.5\right]}{2.38 - 25k\left(3.5\mu A\right)}$$

$$= \frac{25k\left(10.41\right)}{2.29} = 114k$$

$$R_{FB} = 114k\left(5/1.5\right) = 380k$$

SWITCH NODE CONSIDERATIONS

For maximum efficiency, switch rise and fall times are made as short as possible. To prevent radiation and high frequency resonance problems, proper layout of the components connected to the switch node is essential. B field (magnetic) radiation is minimized by keeping catch diode, switch pin, and input bypass capacitor leads as short as possible. E field radiation is kept low by minimizing the length and area of all traces connected to the switch pin and boost pin. A ground plane should always be used under the switcher circuitry to prevent interplane coupling. A suggested layout for the critical components is shown in Figure 5. Note that the feedback resistors and compensation components are kept as far as possible from the switch node. Also note that the high current ground path of the catch diode and input capacitor are kept very short and separate from the analog ground line.

The high speed switching current path is shown schematically in Figure 6. Minimum lead length in this path is essential to ensure clean switching and low EMI. The path including the switch, catch diode, and input capacitor is the only one containing nanosecond rise and fall times. If you follow this path on the PC layout, you will see that it is irreducibly short. If you move the diode or input capacitor away from the LT1376, get your resumé in order. The other paths contain only some combination of DC and 500kHz triwave, so are much less critical.

PARASITIC RESONANCE

Resonance or "ringing" may sometimes be seen on the switch node (see Figure 7). Very high frequency ringing following switch rise time is caused by switch/diode/input capacitor lead inductance and diode capacitance. Schottky diodes have very high "Q" junction capacitance that can ring for many cycles when excited at high frequency. If total lead length for the input capacitor, diode and switch path is 1 inch, the inductance will be approximately 25nH. Schottky diode capacitance of 100pF will create a resonance at 100MHz. This ringing is not harmful to the LT1376 and can normally be ignored.

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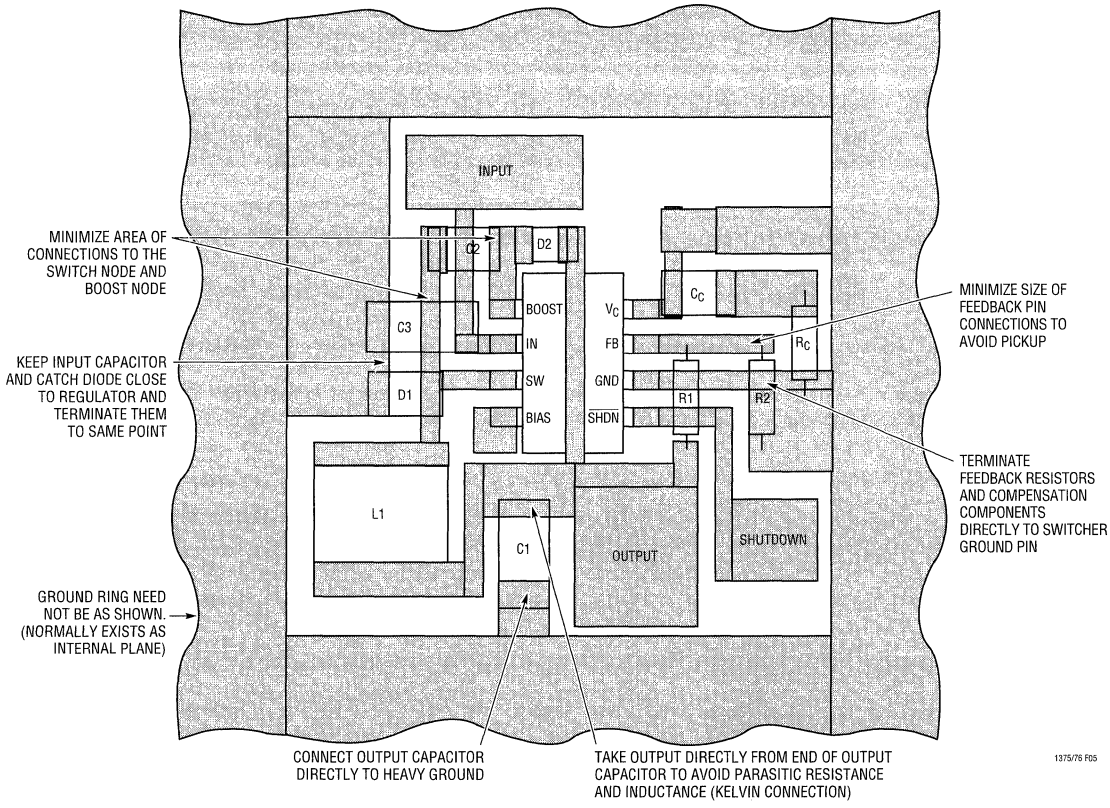

Figure 5. Suggested Layout

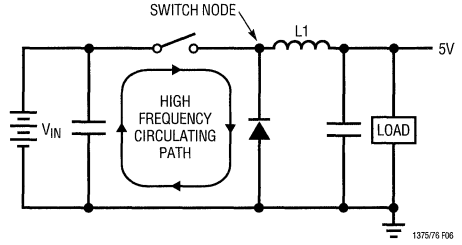

Figure 6. High Speed Switching Path

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Overshoot or ringing following switch fall time is created by switch capacitance rather than diode capacitance. This ringing per se is not harmful, but the overshoot can cause problems if the amplitude becomes too high. The negative voltage can forward bias parasitic junctions on the IC chip and cause erratic switching. The LT1376 has special circuitry inside which mitigates this problem, but negative voltages over 1V lasting longer than 10ns should be avoided. Note that 100MHz oscilloscopes are barely fast enough to see the details of the falling edge overshoot in Figure 7.

A second, much lower frequency ringing is seen during switch off time if load current is low enough to allow the inductor current to fall to zero during part of the switch off time (see Figure 8). Switch and diode capacitance resonate with the inductor to form damped ringing at 1MHz to 10 MHz. Again, this ringing is not harmful to the regulator and it has not been shown to contribute significantly to EMI. Any attempt to damp it with a resistive snubber will degrade efficiency.

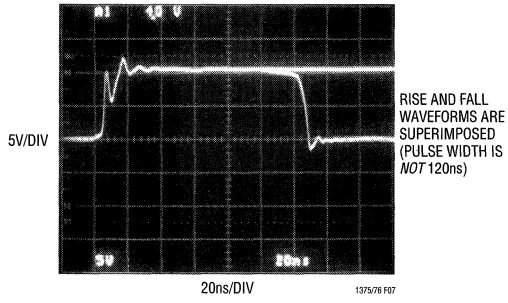

Figure 7. Switch Node Resonance

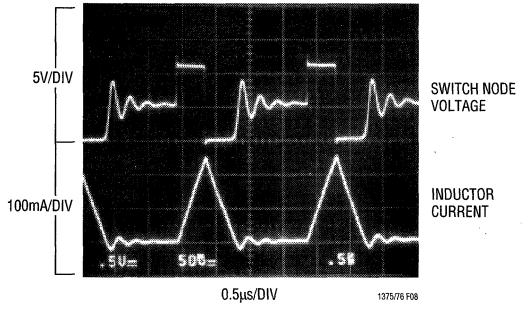

Figure 8. Discontinuous Mode Ringing

INPUT BYPASSING AND VOLTAGE RANGE

Input Bypass Capacitor

Step-down converters draw current from the input supply in pulses. The average height of these pulses is equal to load current, and the duty cycle is equal to V_{OUT}/V_{IN}. Rise and fall time of the current is very fast. A local bypass capacitor across the input supply is necessary to ensure proper operation of the regulator and minimize the ripple current fed back into the input supply. *The capacitor also forces switching current to flow in a tight local loop, minimizing EMI.*

Do not cheat on the ripple current rating of the Input bypass capacitor, but also don't get hung up on the value in microfarads. The input capacitor is intended to absorb all the switching current ripple, which can have an RMS value as high as one half of load current. Ripple current ratings on the capacitor must be observed to ensure reliable operation. The actual value of the capacitor in microfarads is not particularly important because at 500kHz, any value above 5µF is essentially resistive. RMS ripple current rating is the critical parameter. Actual RMS current can be calculated from:

$$I_{RIPPLE(RMS)} = I_{OUT}\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)/V_{IN}^{2}}$$

The term inside the radical has a maximum value of 0.5 when input voltage is twice output, and stays near 0.5 for a relatively wide range of input voltages. It is common practice therefore to simply use the worst-case value and assume that RMS ripple current is one half of load current. At maximum output current of 1.5A for the LT1376, the input bypass capacitor should be rated at 0.75A ripple current. Note however, that there are many secondary considerations in choosing the final ripple current rating. These include ambient temperature, average versus peak load current, equipment operating schedule, and required product lifetime. For more details, see Application Notes 19 and 46, and Design Note 95.

Input Capacitor Type

Some caution must be used when selecting the type of capacitor used at the input to regulators. Aluminum

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lectrolytics are lowest cost, but are physically large to chieve adequate ripple current rating, and size contraints (especially height), may preclude their use. Ceamic capacitors are now available in larger values, and neir high ripple current and voltage rating make them deal for input bypassing. Cost is fairly high and footprint nay also be somewhat large. Solid tantalum capacitors would be a good choice, except that they have a history of ccasional spectacular failures when they are subjected to irge current surges during power-up. The capacitors can hort and then burn with a brilliant white light and lots of asty smoke. This phenomenon occurs in only a small ercentage of units, but it has led some OEM companies o forbid their use in high surge applications. The input ypass capacitor of regulators can see these high surges hen a battery or high capacitance source is connected. everal manufacturers have developed a line of solid ntalum capacitors specially tested for surge capability AVX TPS series for instance, see Table 3), but even these nits may fail if the input voltage surge approaches the aximum voltage rating of the capacitor. AVX recomends derating capacitor voltage by 2:1 for high surge pplications. The highest voltage rating is 50V, so 25V nay be a practical upper limit when using solid tantalum apacitors for input bypassing.

arger capacitors may be necessary when the input voltge is very close to the minimum specified on the data heet. Small voltage dips during switch on time are not ormally a problem, but at very low input voltage they may ause erratic operation because the input voltage drops elow the minimum specification. Problems can also ccur if the input-to-output voltage differential is near inimum. The amplitude of these dips is normally a nction of capacitor ESR and ESL because the capacitive eactance is small compared to these terms. ESR tends to e the dominate term and is inversely related to physical apacitor size within a given capacitor type.

inimum Input Voltage (After Start-Up)

linimum input voltage to make the LT1376 "run" corctly is typically 5V, but to regulate the output, a buck onverter input voltage must always be higher than the utput voltage. To calculate minimum operating input voltage, switch voltage loss and maximum duty cycle must be taken into account. With the LT1376, there is the additional consideration of proper operation of the boost circuit. The boost circuit allows the power switch to saturate for high efficiency, but it also sometimes results in a start-up or operating voltage that is several volts higher than the standard running voltage, especially at light loads. An approximate formula to calculate minimum *running* voltage at load currents above 100mA is:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT})(0.4\Omega)}{0.88}$$

Minimum Start-Up Voltage and Operation at Light Loads

The boost capacitor supplies current to the Boost pin during switch on time. This capacitor is recharged only during switch off time. Under certain conditions of light load and low input voltage, the capacitor may not be recharged fully during the relatively short off time. This causes the boost voltage to collapse and minimum input voltage is increased. Start-up voltage at light loads is higher than normal running voltage for the same reasons. The graph in Figure 9 shows minimum input voltage for a 5V output, both for start-up and for normal operation.

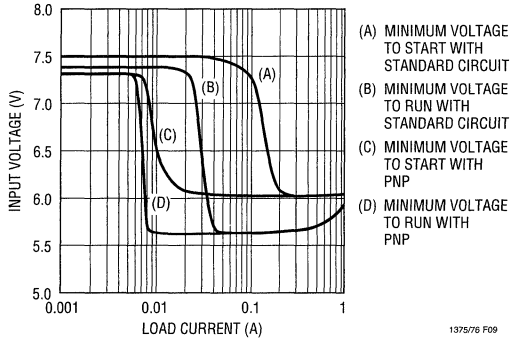

Figure 9. Minimum Input Voltage

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The circuit in Figure 10 will allow operation at light load with low input voltages. It uses a small PNP to charge the boost capacitor C2, and an extra diode D3 to complete the power path from V_{SW} to the boost capacitor.

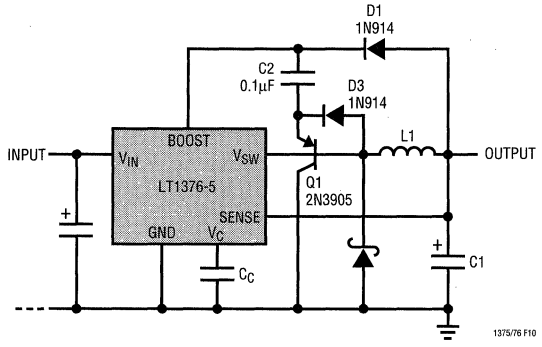

Figure 10. Reducing Minimum Input Voltage

SYNCHRONIZING (Available on LT1375 Only)

The LT1375 has the bias pin replaced with a sync pin, which is used to synchronize the internal oscillator to an external signal. It is directly logic compatible and can be driven with any signal between 10% and 90% duty cycle. The synchronizing range is equal to *initial* operating frequency up to 900kHz. This means that *minimum* practical sync frequency is equal to the worst-case *high* self-oscillating frequency (560kHz), not the typical operating frequency of 500kHz. Caution should be used when synchronizing above 700kHz because at higher sync frequencies the amplitude of the internal slope compensation used to prevent subharmonic switching is reduced. This type of subharmonic switching only occurs at input voltages less than twice output voltage. Higher inductor values will tend to eliminate problems. See Frequency Compensation section for a discussion of an entirely different cause of subharmonic switching before assuming that the cause is insufficient slope compensation. Application Note 19 has more details on the theory of slope compensation.

FREQUENCY COMPENSATION

Loop frequency compensation of switching regulators can be a rather complicated problem because the reactive components used to achieve high efficiency also introduce multiple poles into the feedback loop. The inductor and output capacitor on a conventional step-down converter actually form a resonant tank circuit that can exhibit peaking and a rapid 180° phase shift at the resonant frequency. By contrast, the LT1376 uses a "current mode" architecture to help alleviate phase shift created by the inductor. The basic connections are shown in Figure 11. Figure 12 shows a Bode plot of the phase and gain of the

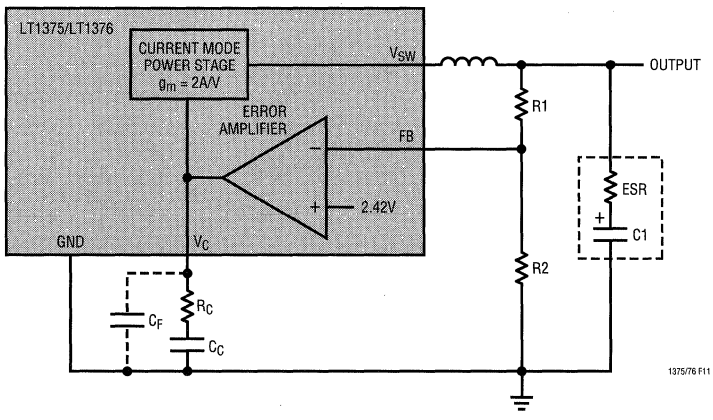

Figure 11. Model for Loop Response

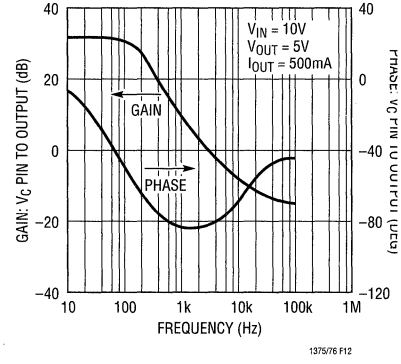

Figure 12. Response from V_C Pin to Output

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ower section of the LT1376, measured from the V_C pin to ıe output. Gain is set by the 2A/V transconductance of the T1376 power section and the effective complex impednce from output to ground. Gain rolls off smoothly above ıe 100Hz pole frequency set by the 100µF output capaci-ɔr. Phase drop is limited to about 85°. Phase recovers and ain levels off at the zero frequency (≈16kHz) set by apacitor ESR (0.1Ω).

rror amplifier transconductance phase and gain are shown ı Figure 13. The error amplifier can be modeled as a ansconductance of 2000µMho, with an output impednce of 200kΩ in parallel with 12pF. In all practical pplications, the compensation network from V_C pin to round has a much lower impedance than the output npedance of the amplifier at frequencies above 500Hz. his means that the error amplifier characteristics themelves do not contribute excess phase shift to the loop, and ıe phase/gain characteristics of the error amplifier secon are completely controlled by the external compensaon network.

ı Figure 14, full loop phase/gain characteristics are hown with a compensation capacitor of 0.0033µF, giving ıe error amplifier a pole at 240Hz, with phase rolling off ɔ 90° and staying there. The overall loop has a gain of 7dB at low frequency, rolling off to unity-gain at 20kHz. hase shows a two-pole characteristic until the ESR of the utput capacitor brings it back above 10kHz. Phase marin is about 60° at unity-gain.

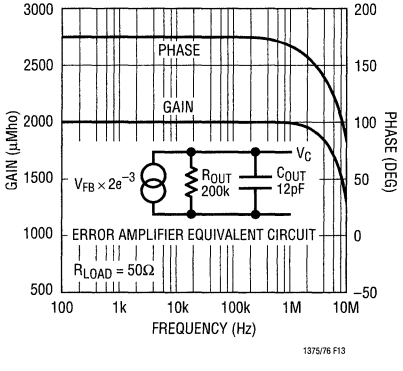

Figure 13. Error Amplifier Gain and Phase

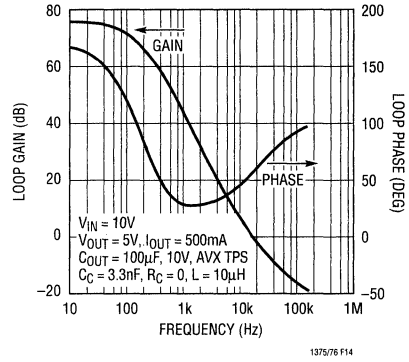

Figure 14. Overall Loop Characteristics

Analog experts will note that around 1kHz, phase dips very close to the zero phase margin line. This is typical of switching regulators, especially those that operate over a wide range of loads. This region of low phase is not a problem as long as it does not occur near unity-gain. In practice, the variability of output capacitor ESR tends to dominate all other effects with respect to loop response. Variations in ESR *will* cause unity-gain to move around, but at the same time phase moves with it so that adequate phase margin is maintained over a very wide range of ESR (≥ ±3:1).

What About a Resistor in the Compensation Network?

It is common practice in switching regulator design to add a "zero" to the error amplifier compensation to increase loop phase margin. This zero is created in the external network in the form of a resistor (R_C) in series with the compensation capacitor. Increasing the size of this resistor generally creates better and better loop stability, but there are two limitations on its value. First, the combination of output capacitor ESR and a large value for R_C may cause loop gain to stop rolling off altogether, creating a gain margin problem. An approximate formula for R_C where gain margin falls to zero is:

$$R_C(\text{Loop Gain} = 1) = \frac{V_{OUT}}{(G_{MP})(G_{MA})(ESR)(2.42)}$$

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G_{MP} = Transconductance of power stage = 2A/V
G_{MA} = Error amplifier transconductance = $2e^{-3}$
ESR = Output capacitor ESR
2.42 = Reference voltage

With V_{OUT} = 5V and ESR = 0.1Ω, a value of 5.17k for R_C would yield zero gain margin, so this represents an upper limit. There is a second limitation however which has nothing to do with theoretical small signal dynamics. This resistor sets high frequency gain of the error amplifier, including the gain at the switching frequency. If switching frequency gain is high enough, output ripple voltage will appear at the V_C pin with enough amplitude to muck up proper operation of the regulator. In the marginal case, *subharmonic* switching occurs, as evidenced by alternating pulse widths seen at the switch node. In more severe cases, the regulator squeals or hisses audibly even though the output voltage is still roughly correct. None of this will show on a theoretical Bode plot because Bode is an amplitude insensitive analysis. *Tests have shown that if ripple voltage on the V_C is held to less than 100mV_{P-P}, the LT1376 will be well behaved.* The formula below will give an estimate of V_C ripple voltage when R_C is added to the loop, assuming that R_C is large compared to the reactance of C_C at 500kHz.

$$V_{C(RIPPLE)} = \frac{(R_C)(G_{MA})(V_{IN} - V_{OUT})(ESR)(2.4)}{(V_{IN})(L)(f)}$$

G_{MA} = Error amplifier transconductance (2000μMho)

If a computer simulation of the LT1376 showed that a series compensation resistor of 3k gave best overall loop response, with adequate gain margin, the resulting V_C pin ripple voltage with V_{IN} = 10V, V_{OUT} = 5V, ESR = 0.1Ω, L = 10μH, would be:

$$V_{C(RIPPLE)} = \frac{(3k)(2e^{-3})(10-5)(0.1)(2.4)}{(10)(10e^{-6})(500e^{3})} = 0.144V$$

This ripple voltage is high enough to possibly create subharmonic switching. In most situations a compromise value (<2k in this case) for the resistor gives acceptable phase margin and no subharmonic problems. In other cases, the resistor may have to be larger to get acceptable phase response, and some means must be used to control ripple voltage at the V_C pin. The suggested way to do this is to add a capacitor (C_F) in parallel with the R_C/C_C network on the V_C pin. Pole frequency for this capacitor is typically set at one-fifth of switching frequency so that it provides significant attenuation of switching ripple, but does not add unacceptable phase shift at loop unity-gain frequency. With R_C = 3k,

$$C_F = \frac{5}{(2\pi)(f)(R_C)} = \frac{5}{2\pi(500e^{3})(3k)} = 531pF$$

How Do I Test Loop Stability?

The "standard" compensation for LT1376 is a 3.3nF capacitor for C_C, with R_C = 0. While this compensation will work for most applications, the "optimum" value for loop compensation components depends, to various extent, on parameters which are not well controlled. These include *inductor value* (±30% due to production tolerance, load current and ripple current variations), *output capacitance* (±20% to ±50% due to production tolerance, temperature, aging and changes at the load), *output capacitor ESR* (±200% due to production tolerance, temperature and aging), and finally, *DC input voltage and output load current*. This makes it important for the designer to check out the final design to ensure that it is "robust" and tolerant of all these variations.

I check switching regulator loop stability by pulse loading the regulator output while observing transient response at the output, using the circuit shown in Figure 15. The regulator loop is "hit" with a small transient AC load current at a relatively low frequency, 50Hz to 1kHz. This causes the output to jump a few millivolts, then settle back to the original value, as shown in Figure 16. A well behaved loop will settle back cleanly, whereas a loop with poor phase or gain margin will "ring" as it settles. The *number* of rings indicates the degree of stability, and the *frequency* of the ringing shows the approximate unity-gain frequency of the loop. *Amplitude* of the signal is not particularly important, as long as the amplitude is not so high that the loop behaves nonlinearly.

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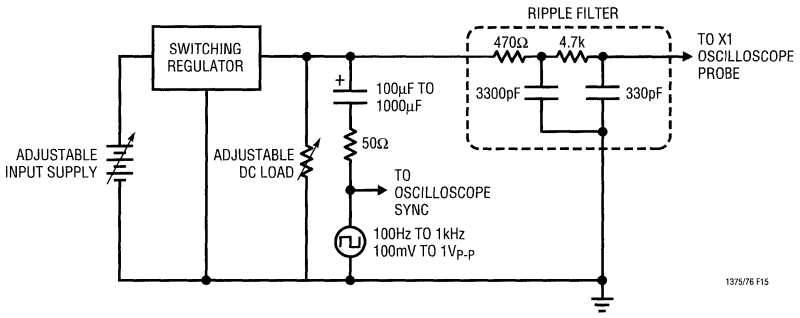

Figure 15. Loop Stability Test Circuit

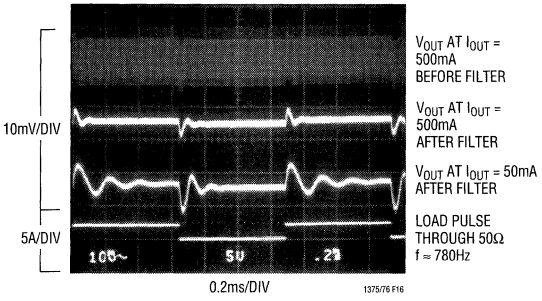

Figure 16. Loop Stability Check

he output of the regulator contains both the desired low equency transient information and a reasonable amount f high frequency (500kHz) ripple. The ripple makes it ifficult to observe the small transient, so a two-pole, 00kHz filter has been added. This filter is not particularly ritical; even if it attenuated the transient signal slightly, his wouldn't matter because amplitude is not critical.

fter verifying that the setup is working correctly, I start arying load current and input voltage to see if I can find ny combination that makes the transient response look uspiciously "ringy." This procedure may lead to an ad- ıstment for best loop stability or faster loop transient esponse. Nearly always you will find that loop response oks better if you add in several kΩ for R_C. Do this only necessary, because as explained before, R_C above 1k ay require the addition of C_F to control V_C pin ripple. If verything looks OK, I use a heat gun and cold spray on the ircuit (especially the output capacitor) to bring out any emperature-dependent characteristics.

Keep in mind that this procedure does not take initial component tolerance into account. You should see fairly clean response under all load and line conditions to ensure that component variations will not cause problems. One note here: according to Murphy, the component most likely to be changed in production is the output capacitor, because that is the component most likely to have manufacturer variations (in ESR) large enough to cause problems. It would be a wise move to lock down the sources of the output capacitor in production.

A possible exception to the "clean response" rule is at very light loads, as evidenced in Figure 16 with I_{LOAD} = 50mA. Switching regulators tend to have dramatic shifts in loop response at very light loads, mostly because the inductor current becomes discontinuous. One common result is very slow but stable characteristics. A second possibility is low phase margin, as evidenced by ringing at the output with transients. The good news is that the low phase margin at light loads is not particularly sensitive to component variation, so if it looks reasonable under a transient test, it will probably not be a problem in production. Note that *frequency* of the light load ringing may vary with component tolerance but phase margin generally hangs in there.

THERMAL CALCULATIONS

Power dissipation in the LT1376 chip comes from four sources: switch DC loss, switch AC loss, boost circuit current, and input quiescent current. The following formulas show how to calculate each of these losses. These

4

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formulas assume continuous mode operation, so they should not be used for calculating efficiency at light load currents.

Switch loss:

$$P_{SW} = \frac{R_{SW}(I_{OUT})^2(V_{OUT})}{V_{IN}} + 16ns(I_{OUT})(V_{IN})(f)$$

Boost current loss:

$$P_{BOOST} = \frac{V_{OUT}^2(0.008 + I_{OUT}/75)}{V_{IN}}$$

Quiescent current loss:

$$P_Q = V_{IN}(0.001) + V_{OUT}(0.005) + \frac{(V_{OUT}^2)(0.002)}{V_{IN}}$$

R_{SW} = Switch resistance ($\approx$0.4)
16ns = Equivalent switch current/voltage overlap time
f = Switch frequency

Example: with V_{IN} = 10V, V_{OUT} = 5V and I_{OUT} = 1A:

$$P_{SW} = \frac{(0.4)(1)^2(5)}{10} + (16e^{-9})(1)(10)(500e^3)$$
$$= 0.2 + 0.08 = 0.28W$$

$$P_{BOOST} = \frac{(5)^2(0.008 + 1/75)}{10} = 0.053W$$

$$P_Q = 10(0.001) + 5(0.005) + \frac{(5)^2(0.002)}{10} = 0.04W$$

Total power dissipation is 0.28 + 0.053 + 0.04 = 0.37W.

Thermal resistance for LT1376 package is influenced by the presence of internal or backside planes. With a full plane under the SO package, thermal resistance will be about 120°C/W. No plane will increase resistance to about 160°C/W. To calculate die temperature, use the proper thermal resistance number for the desired package and add in worst-case ambient temperature:

$$T_J = T_A + \theta_{JA}(P_{TOT})$$

With the SO-8 package (θ_{JA} = 120°C/W), at an ambient temperature of 70°C,

$$T_J = 70 + 120\ (0.37) = 114.4°C$$

Die temperature is highest at low input voltage, so use lowest continuous input operating voltage for thermal calculations.

POSITIVE-TO-NEGATIVE CONVERTER

The circuit in Figure 17 is a classic positive-to-negative topology using a grounded inductor. It differs from the standard approach in the way the IC chip derives its feedback signal, however. Because the LT1376 accepts only positive feedback signals, the ground pin must be tied to the regulated negative output. A resistor divider to ground or, in this case, the sense pin, then provides the proper feedback voltage for the chip.

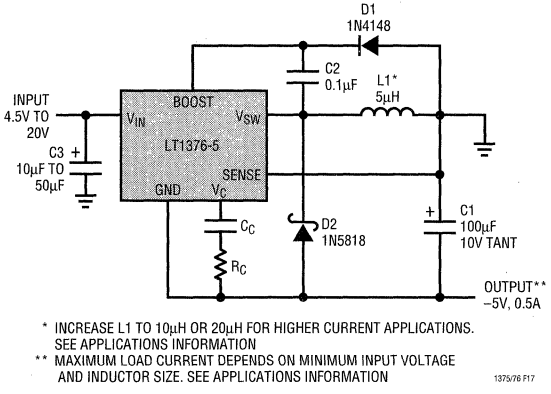

Figure 17. Positive-to-Negative Converter

Inverting regulators differ from buck regulators in the basic switching network. Current is delivered to the output as *square waves with a peak-to-peak amplitude much greater than load current.* This means that *maximum load current will be significantly less than the LT1376's 1.5A maximum switch current, even with large inductor values.* The buck converter in comparison, delivers current to the output as a triangular wave superimposed on a DC level equal to load current, and load current can approach 1.5A

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with large inductors. Output ripple voltage for the positive-to-negative converter will be much higher than a buck converter. Ripple current in the output capacitor will also be much higher. The following equations can be used to calculate operating conditions for the positive-to-negative converter.

Maximum load current:

$$I_{MAX} = \frac{\left[I_P - \frac{(V_{IN})(V_{OUT})}{2(V_{OUT}+V_{IN})(f)(L)}\right](V_{OUT})(V_{IN}-0.5)}{(V_{OUT}+V_{IN}-0.5)(V_{OUT}+V_F)}$$

I_P = Maximum rated switch current
V_{IN} = Minimum input voltage
V_{OUT} = Output voltage
V_F = Catch diode forward voltage
0.5 = Switch voltage drop at 1.5A

Example: with $V_{IN(MIN)}$ = 4.7V, V_{OUT} = 5V, L = 10µH, V_F = 0.5V, I_P = 1.5A: I_{MAX} = 0.52A. Note that this equation does not take into account that maximum rated switch current (I_P) on the LT1376 is reduced slightly for duty cycles above 50%. If duty cycle is expected to exceed 50% (input voltage less than output voltage), use the actual I_P value from the Electrical Characteristics table.

Operating duty cycle:

$$DC = \frac{V_{OUT}+V_F}{V_{IN}-0.3+V_{OUT}+V_F}$$

(This formula uses an average value for switch loss, so it may be several percent in error.)

With the conditions above:

$$DC = \frac{5+0.5}{4.7-0.3+5+0.5} = 56\%$$

This duty cycle is close enough to 50% that I_P can be assumed to be 1.5A.

OUTPUT DIVIDER

If the adjustable part is used, the resistor connected to V_{OUT} (R2) should be set to approximately 5k. R1 is calculated from:

$$R1 = \frac{R2(V_{OUT}-2.42)}{2.42}$$

INDUCTOR VALUE

Unlike buck convertors, positive-to-negative converters cannot use large inductor values to reduce output ripple voltage. At 500kHz, values larger than 25µH make almost no change in output ripple. The graph in Figure 18 shows peak-to-peak output ripple voltage for a 5V to –5V converter versus inductor value. The criteria for choosing the inductor is therefore typically based on ensuring that peak switch current rating is not exceeded. This gives the lowest value of inductance that can be used, but in some cases (lower output load currents) it may give a value that creates unnecessarily high output ripple voltage. A compromise value is often chosen that reduces output ripple. As you can see from the graph, *large* inductors will not give arbitrarily low ripple, but *small* inductors can give high ripple.

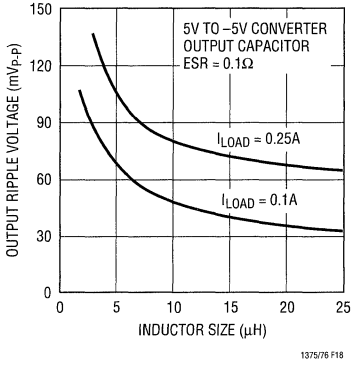


Figure 18. Ripple Voltage on Positive-to-Negative Converter

APPLICATIONS INFORMATION

The difficulty in calculating the minimum inductor size needed is that you must first know whether the switcher will be in continuous or discontinuous mode at the critical point where switch current is 1.5A. The first step is to use the following formula to calculate the load current where the switcher must use continuous mode. If your load current is less than this, use the discontinuous mode formula to calculate minimum inductor needed. f load current is higher, use the continuous mode formula.

Output current where continuous mode is needed:

$$I_{CONT} = \sqrt{\frac{(V_{IN})^2(I_P)^2}{4(V_{IN}+V_{OUT})(V_{IN}+V_{OUT}+V_F)}}$$

Minimum inductor discontinuous mode:

$$L_{MIN} = \frac{2(V_{OUT})(I_{OUT})}{(f)(I_P)^2}$$

Minimum inductor continuous mode:

$$L_{MIN} = \frac{(V_{IN})(V_{OUT})}{2(f)(V_{IN}+V_{OUT})\left[I_P - I_{OUT}\left(1+\frac{(V_{OUT}+V_F)}{V_{IN}}\right)\right]}$$

For the example above, with maximum load current of 0.25A:

$$I_{CONT} = \sqrt{\frac{(5)^2(1.5)^2}{4(5+5)(5+5+0.5)}} = 0.37A$$

This says that discontinuous mode can be used and the minimum inductor needed is found from:

$$L_{MIN} = \frac{2(5)(0.25)}{(500e^3)(1.5)^2} = 2.2\mu H$$

In practice, the inductor should be increased by about 30% over the calculated minimum to handle losses and variations in value. This suggests a minimum inductor of 3µH for this application, but looking at the ripple voltage chart shows that output ripple voltage could be reduced by a factor of two by using a 15µH inductor. There is no rule of thumb here to make a final decision. If modest ripple is needed and the larger inductor does the trick, go for it. If ripple is noncritical use the smaller inductor. If ripple is extremely critical, a second tilter may have to be added in any case, and the lower value of inductance can be used. Keep in mind that the output capacitor is the other critical factor in determining output ripple voltage. Ripple shown on the graph (Figure 18) is with a capacitor ESR of 0.1Ω. This is reasonable for an AVX type TPS "D" or "E" size surface mount solid tantalum capacitor, but the final capacitor chosen must be looked at carefully for ESR characteristics.

Ripple Current in the Input and Output Capacitors

Positive-to-negative converters have high ripple current in both the input and output capacitors. For long capacitor lifetime, the RMS value of this current must be less than the high frequency ripple current rating of the capacitor. The following formula will give an *approximate* value for RMS ripple current. *This formula assumes continuous mode and large inductor value.* Small inductors will give somewhat higher ripple current, especially in discontinuous mode. The exact formulas are very complex and appear in Application Note 44, pages 30 and 31. For our purposes here I have simply added a fudge factor (ff). The value for ff is about 1.2 for higher load currents and L ≥10µH. It increases to about 2.0 for smaller inductors at lower load currents.

$$\text{Capacitor } I_{RMS} = (ff)(I_{OUT})\sqrt{\frac{V_{OUT}}{V_{IN}}}$$

ff = Fudge factor[1] (1.2 to 2.0)

Diode Current

Average diode current is equal to load current. *Peak* diode current will be considerably higher.

[1]Normally, Jamoca Almond

IPPLICATIONS INFORMATION

eak diode current:

$$\text{Continuous Mode} = I_{OUT}\frac{(V_{IN}+V_{OUT})}{V_{IN}}+\frac{(V_{IN})(V_{OUT})}{2(L)(f)(V_{IN}+V_{OUT})}$$

$$\text{Discontinuous Mode} = \sqrt{\frac{2(I_{OUT})(V_{OUT})}{(L)(f)}}$$

eep in mind that during start-up and output overloads, verage diode current may be much higher than with ormal loads. Care should be used if diodes rated less than A are used, especially if continuous overload conditions ust be tolerated.

Dual Output SEPIC Converter

The circuit in Figure 19 generates both positive and negative 5V outputs with a single piece of magnetics. The two inductors shown are actually just two windings on a standard Coiltronics inductor. The topology for the 5V output is a standard buck converter. The –5V topology would be a simple flyback winding coupled to the buck converter if C4 were not present. C4 creates the SEPIC (Single-Ended Primary Inductance Converter) topology which improves regulation and reduces ripple current in L1. For details on this circuit see Design Note 100.

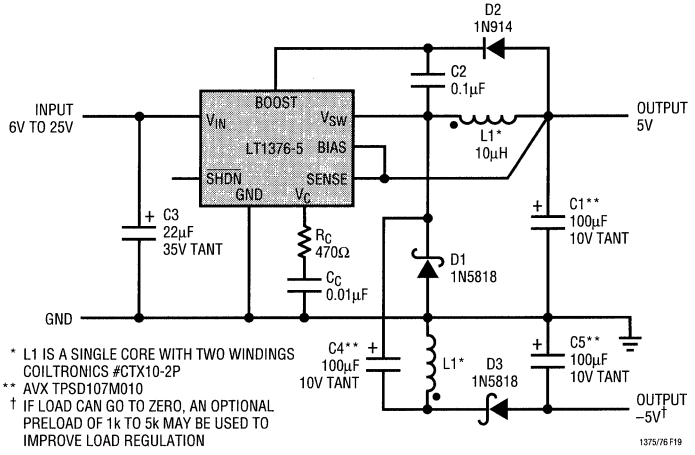


Figure 19. Dual Output SEPIC Converter

ELATED PARTS

RT NUMBER	DESCRIPTION	COMMENTS
1074/LT1076	Step-Down Switching Regulator	40V Input, 100kHz, 5A and 2A
C1148	High Efficiency Synchronous Step-Down Switching Regulator	External FET Switches
C1149	High Efficiency Synchronous Step-Down Switching Regulator	External FET Switches
C1174	High Efficiency Step-Down and Inverting DC/DC Converter	0.5A, 150kHz Burst Mode™ Operation
1176	Step-Down Switching Regulator	PDIP LT1076
1372/LT1377	500kHz and 1MHz High Efficiency 1.5A Switching Regulators	Boost Topology

st Mode is a trademark of Linear Technology Corporation.

High Power Step-Down Switching Regulator Controller

FEATURES

- **High Power 5V to 3.xV Switching Controller: Can Exceed 10A Output**
- **All N-Channel External MOSFETs**
- Constant Frequency Operation—Small L
- **Excellent Output Regulation: ±1% Over Line, Load and Temperature Variations**
- High Efficiency: Over 95% Possible
- Fixed Frequency Operation
- No Low Value Sense Resistor Needed
- Outputs Can Drive External FETs with Up to 10,000pF Gate Capacitance
- Quiescent Current: 350μA Typ, 1μA in Shutdown
- Fast Transient Response
- Adjustable or Fixed 3.3V Output
- Available in 8- and 16-Lead PDIP and SO Packages

APPLICATIONS

- Power Supply for P6™ and Pentium® Microprocessors
- High Power 5V to 3.xV Regulators
- Local Regulation for Dual Voltage Logic Boards
- Low Voltage, High Current Battery Regulation

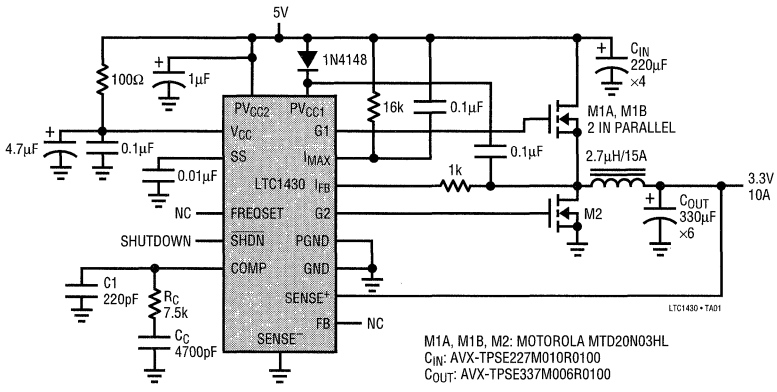
DESCRIPTION

The LTC®1430 is a high power, high efficiency switching regulator controller optimized for 5V to 3.xV applications. It includes a precision internal reference and an internal feedback system that can provide output regulation of ±1% over temperature, load current and line voltage shifts. The LTC1430 uses a synchronous switching architecture with two N-channel output devices, eliminating the need for a high power, high cost P-channel device. Additionally, it senses output current across the drain source resistance of the upper N-channel FET, providing an adjustable current limit without an external low value sense resistor.

The LTC1430 includes a fixed frequency PWM oscillator for low output ripple under virtually all operating conditions. The 200kHz free-running clock frequency can be externally adjusted from 100kHz to above 500kHz. The LTC1430 features low 350μA quiescent current, allowing greater than 90% efficiency operation in converter designs from 1A to greater than 50A output current. Shutdown mode drops the LTC1430 supply current to 1μA.

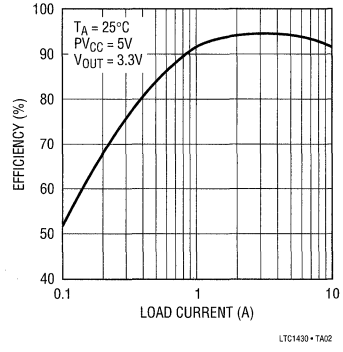
TYPICAL APPLICATION

Typical 5V to 3.3V, 10A Application



M1A, M1B, M2: MOTOROLA MTD20N03HL
C_{IN}: AVX-TPSE227M010R0100
C_{OUT}: AVX-TPSE337M006R0100

Efficiency



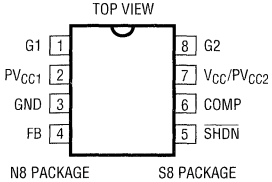
BSOLUTE MAXIMUM RATINGS

ote 1)

ıpply Voltage
V_{CC} 9V
$PV_{CC1, 2}$ 13V
ɒut Voltage
I_{FB} ..... −0.3V to 18V
All Other Inputs ..... −0.3V to V_{CC} + 0.3V

Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

ACKAGE/ORDER INFORMATION



N8 PACKAGE 8-LEAD PDIP
S8 PACKAGE 8-LEAD PLASTIC SO

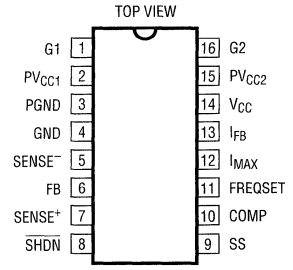
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER

LTC1430CN8
LTC1430CS8

S8 PART MARKING

1430



N PACKAGE 16-LEAD PDIP
S PACKAGE 16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER

LTC1430CN
LTC1430CS

ısult factory for Industrial and Military grade parts.

LECTRICAL CHARACTERISTICS

(Note 2) V_{CC} = 5V, T_A = 25°C unless otherwise noted.

MBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
;	Supply Voltage		●	4		8	V
CC	PV_{CC1}, PV_{CC2}		●			13	V
JT	Output Voltage	Figure 1	●		3.30		V
	Feedback Voltage	Figure 1, $SENSE^+$ and $SENSE^-$ Floating	●	1.25	1.265	1.28	V
OUT	Output Load Regulation Output Line Regulation	Figure 1, I_{OUT} = 0A to 10A (Note 3) Figure 1, V_{CC} = 4.75V to 5.25V (Note 3)	● ●		5 1	20 5	mV mV
C	Supply Current (V_{CC} Only)	Figure 2, $V_{\overline{SHDN}}$ = V_{CC} $V_{\overline{SHDN}}$ = 0V	●		350 1	700 10	µA µA
CC	Supply Current (PV_{CC})	Figure 2, PV_{CC} = 5V, $V_{\overline{SHDN}}$ = V_{CC} (Note 4) $V_{\overline{SHDN}}$ = 0V			1.5 0.1		mA µA
C	Internal Oscillator Frequency	FREQSET Floating	●	140	200	260	kHz
	$\overline{SHDN}$ Input High Voltage		●	2.4			V
	$\overline{SHDN}$ Input Low Voltage		●			0.8	V
	$\overline{SHDN}$ Input Current		●		±0.1	±1	µA
V	Error Amplifier Transconductance				650		µMho
I	I_{LIM} Amplifier Transconductance	(Note 5)			1300		µMho

ELECTRICAL CHARACTERISTICS

(Note 2) V_{CC} = 5V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
I_{MAX}	I_{MAX} Sink Current	$V_{I(MAX)} = V_{CC}$	●	8	12	16	µ
I_{SS}	Soft Start Source Current	$V_{SS} = 0$	●	−8	−12	−16	µ
t_r, t_s	Driver Rise/Fall Time	Figure 3, $PV_{CC1} = PV_{CC2} = 5V$			80	250	n
t_{NOV}	Driver Non-Overlap Time	Figure 3, $PV_{CC1} = PV_{CC2} = 5V$		25	130	250	n
DC_{MAX}	Maximum Duty Cycle	$V_{COMP} = V_{CC}$	●		90	96	

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: This parameter is guaranteed by correlation and is not tested directly.

Note 4: Supply current in normal operation is dominated by the current needed to charge and discharge the external FET gates. This will vary with the LTC1430 operating frequency, operating voltage and the external FETs used.

Note 5: The I_{LIM} amplifier can sink but cannot source current. Under normal (not current limited) operation, the I_{LIM} output current will be zero

PIN FUNCTIONS

(16-Lead Package/8-Lead Package)

G1 (Pin 1/Pin 1): Driver Output 1. Connect this pin to the gate of the upper N-channel MOSFET, M1. This output will swing from PV_{CC1} to PGND. It will always be low when G2 is high.

PV_{CC1} (Pin 2/Pin 2): Power V_{CC} for Driver 1. This is the power supply input for G1. G1 will swing from PGND to PV_{CC1}. PV_{CC1} must be connected to a potential of at least $PV_{CC} + V_{GS(ON)}$(M1). This potential can be generated using an external supply or a simple charge pump connected to the switching node between the upper MOSFET and the lower MOSFET; see Applications Information for details.

PGND (Pin 3/Pin 3): Power Ground. Both drivers return to this pin. It should be connected to a low impedance ground in close proximity to the source of M2. 8-lead parts have PGND and GND tied together at pin 3.

GND (Pin 4/Pin 3): Signal Ground. All low power internal circuitry returns to this pin. To minimize regulation errors due to ground currents, GND should be connected to PGND right at the LTC1430. 8-lead parts have PGND and GND tied together internally at pin 3.

SENSE⁻, FB, SENSE⁺ (Pins 5, 6, 7/Pin 4): These three pins connect to the internal resistor divider and to the internal feedback node. To use the internal divider to set the output voltage to 3.3V, connect SENSE⁺ to the positive terminal of the output capacitor and SENSE⁻ to the negative terminal. FB should be left floating in applications that use the internal divider. To use an external resistor divider to set the output voltage, float SENSE⁺ and SENSE⁻ and connect the external resistor divider to FB.

$\overline{SHDN}$ (Pin 8/Pin 5): Shutdown. A TTL compatible low level at $\overline{SHDN}$ for longer than 50µs puts the LTC1430 into shutdown mode. In shutdown, G1 and G2 go low, all internal circuits are disabled and the quiescent current drops to 10µA max. A TTL compatible high level at $\overline{SHDN}$ allows the part to operate normally.

SS (Pin 9/NA): Soft Start. The SS pin allows an external capacitor to be connected to implement a soft start function. An external capacitor from SS to ground controls the start-up time and also compensates the current limit loop allowing the LTC1430 to enter and exit current limit cleanly. See Applications Information for more details.

COMP (Pin 10/Pin 6): External Compensation. The COMP pin is connected directly to the output of the error amplifier and the input of the PWM. An RC network is used at this node to compensate the feedback loop to provide optimum transient response. See Applications Information for compensation details.

FREQSET (Pin 11/NA): Frequency Set. This pin is used to set the free running frequency of the internal oscillator. With the pin floating, the oscillator runs at about 200kHz. A resistor from FREQSET to ground will speed up the

'IN FUNCTIONS (16-Lead Package/8-Lead Package)

scillator; a resistor to V_{CC} will slow it down. See Applica-ons Information for resistor selection details.

ıAX (Pin 12/NA): Current Limit Set. I_{MAX} sets the thresh-ld for the internal current limit comparator. If I_{FB} drops elow I_{MAX} with G1 on, the LTC1430 will go into current ıit. I_{MAX} has a 12µA pull-down to GND. It can be adjusted ·ith an external resistor to PV_{CC} or an external voltage ɔurce.

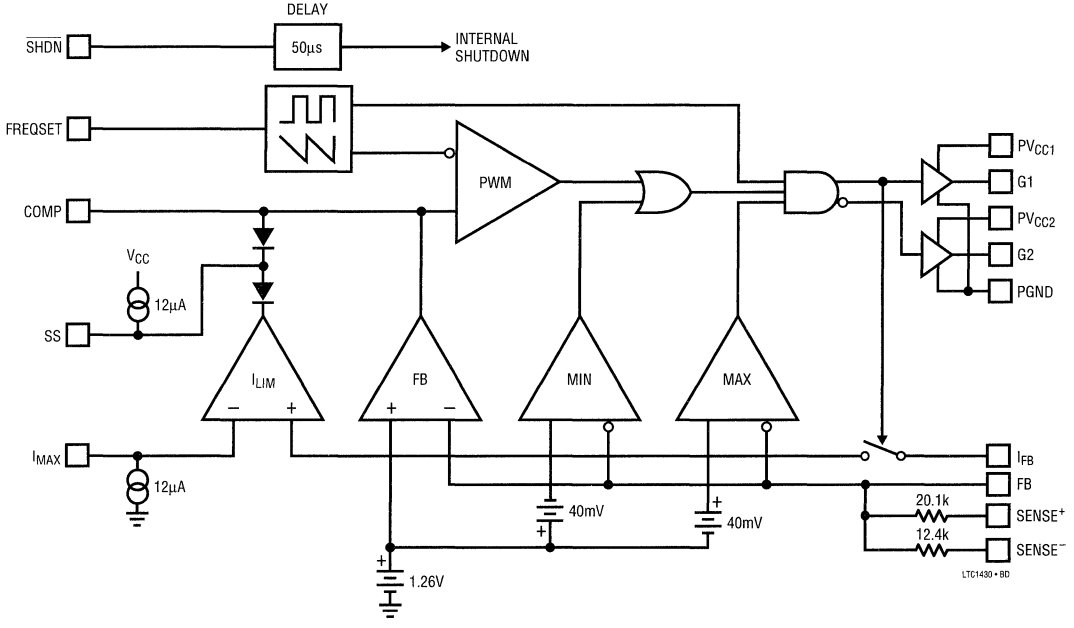
'B (Pin 13/NA): Current Limit Sense. Connect to the ıvitched node at the source of M1 and the drain of M2 ırough a 1k resistor. The 1k resistor is required to prevent ɔltage transients from damaging I_{FB}. This pin can be ıken up to 18V above GND without damage.

V_{CC} (Pin 14/Pin 7): Power Supply. All low power internal circuits draw their supply from this pin. Connect to a clean power supply, separate from the main PV_{CC} supply at the drain of M1. This pin requires a 4.7µF bypass capacitor. 8-lead parts have V_{CC} and PV_{CC2} tied together at pin 7 and require a 10µF bypass to GND.

PV_{CC2} (Pin 15/Pin 7): Power V_{CC} for Driver 2. This is the power supply input for G2. G2 will swing from GND to PV_{CC2}. PV_{CC2} is usually connected to the main high power supply. The 8-lead parts have V_{CC} and PV_{CC2} tied together at pin 7 and require a 10µF bypass to GND.

G2 (Pin 16/Pin 8): Driver Output 2. Connect this pin to the gate of the lower N-channel MOSFET, M2. This output will swing from PV_{CC2} to PGND. It will always be low when G1 is high.

ıLOCK DIAGRAM



TEST CIRCUITS

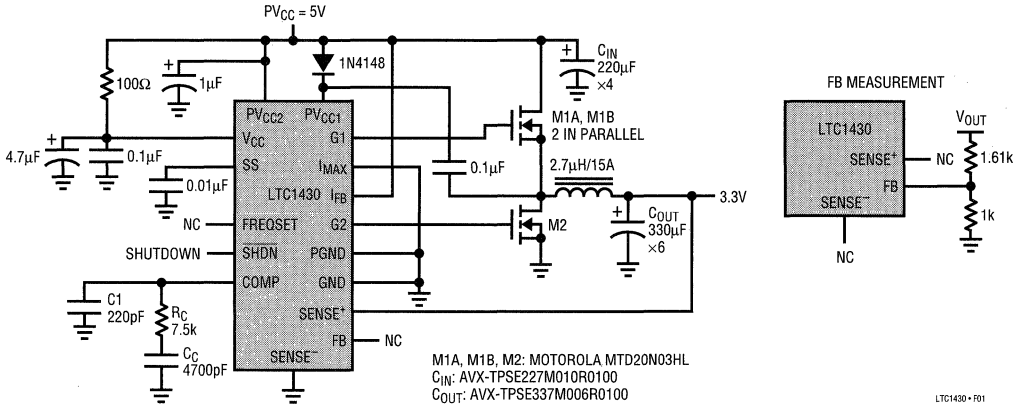


Figure 1

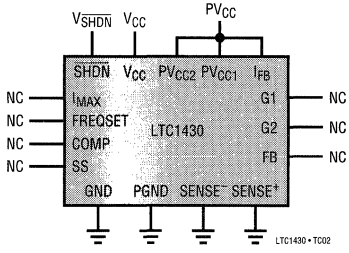


Figure 2

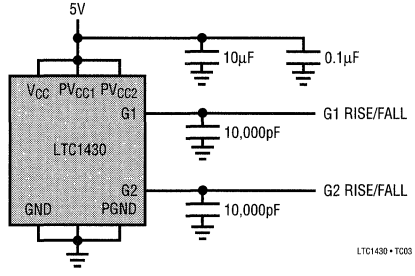


Figure 3

APPLICATIONS INFORMATION

OVERVIEW

The LTC1430 is a voltage feedback PWM switching regulator controller (see Block Diagram) designed for use in high power, low voltage step-down (buck) converters. It includes an onboard PWM generator, a precision reference trimmed to ±0.5%, two high power MOSFET gate drivers and all necessary feedback and control circuitry to form a complete switching regulator circuit. The PWM loop nominally runs at 200kHz.

The 16-lead versions of the LTC1430 include a current limit sensing circuit that uses the upper external power MOSFET as a current sensing element, eliminating the need for an external sense resistor.

Also included in the 16-lead version is an internal soft start feature that requires only a single external capacitor to operate. In addition, 16-lead parts feature an adjustable oscillator which can run at frequencies from 50kHz to beyond 500kHz, allowing added flexibility in external component selection. The 8-lead versions do not include current limit, internal soft start or frequency adjustability

APPLICATIONS INFORMATION

THEORY OF OPERATION

Primary Feedback Loop

The LTC1430 senses the output voltage of the circuit at the output capacitor with the SENSE$^+$ and SENSE$^-$ pins and feeds this voltage back to the internal transconductance amplifier FB. FB compares the resistor-divided output voltage to the internal 1.26V reference and outputs an error signal to the PWM comparator. This is then compared to a fixed frequency sawtooth waveform generated by the internal oscillator to generate a pulse width modulated signal. This PWM signal is fed back to the external MOSFETs through G1 and G2, closing the loop. Loop compensation is achieved with an external compensation network at COMP, the output node of the FB transconductance amplifier.

MIN, MAX Feedback Loops

Two additional comparators in the feedback loop provide high speed fault correction in situations where the FB amplifier may not respond quickly enough. MIN compares the feedback signal to a voltage 40mV (3%) below the internal reference. At this point, the MIN comparator overrides the FB amplifier and forces the loop to full duty cycle, set by the internal oscillator at about 90%. Similarly, the MAX comparator monitors the output voltage at 3% above the internal reference and forces the output to 0% duty cycle when tripped. These two comparators prevent extreme output perturbations with fast output transients, while allowing the main feedback loop to be optimally compensated for stability.

Current Limit Loop

The 16-lead LTC1430 devices include yet another feedback loop to control operation in current limit. The current limit loop is disabled in 8-lead devices. The I_{LIM} amplifier monitors the voltage drop across external MOSFET M1 with the I_{FB} pin during the portion of the cycle when G1 is high. It compares this voltage to the voltage at the I_{MAX} pin. As the peak current rises, the drop across M1 due to its $R_{DS(ON)}$ increases. When I_{FB} drops below I_{MAX}, indicating that M1's drain current has exceeded the maximum level, I_{LIM} starts to pull current out of the external soft start capacitor, cutting the duty cycle and controlling the output current level. At the same time, the I_{LIM} comparator generates a signal to disable the MIN comparator to prevent it from conflicting with the current limit circuit. If the internal feedback node drops below about 0.8V, indicating a severe output overload, the circuitry will force the internal oscillator to slow down by a factor of as much as 100. If desired, the turn on time of the current limit loop can be controlled by adjusting the size of the soft start capacitor, allowing the LTC1430 to withstand short overcurrent conditions without limiting.

By using the $R_{DS(ON)}$ of M1 to measure the output current, the current limit circuit eliminates the sense resistor that would otherwise be required and minimizes the number of components in the external high current path. Because power MOSFET $R_{DS(ON)}$ is not tightly controlled and varies with temperature, the LTC1430 current limit is not designed to be accurate; it is meant to prevent damage to the power supply circuitry during fault conditions. The actual current level where the limiting circuit begins to take effect may vary from unit to unit, depending on the power MOSFETs used. See Soft Start and Current Limit for more details on current limit operation.

MOSFET Gate Drive

Gate drive for the top N-channel MOSFET M1 is supplied from PV_{CC1}. This supply must be above PV_{CC} (the main power supply input) by at least one power MOSFET $V_{GS(ON)}$ for efficient operation. An internal level shifter allows PV_{CC1} to operate at voltages above V_{CC} and PV_{CC}, up to 13V maximum. This higher voltage can be supplied with a separate supply, or it can be generated using a simple charge pump as shown in Figure 4. When using a separate PV_{CC1} supply, the PV_{CC} input may exhibit a large inrush current if PV_{CC1} is present during power up. The 90% maximum duty cycle ensures that the charge pump will always provide sufficient gate drive to M1. Gate drive for the bottom MOSFET M2 is provided through PV_{CC2} for 16-lead devices or V_{CC}/PV_{CC2} for 8-lead devices. PV_{CC2} can usually be driven directly from PV_{CC} with 16-lead parts, although it can also be charge pumped or connected to an alternate supply if desired. The 8-lead parts require an RC filter from PV_{CC} to ensure proper operation; see Input Supply Considerations.

APPLICATIONS INFORMATION

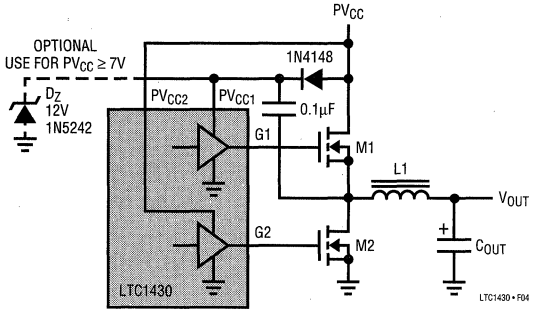


Figure 4. Doubling Charge Pump

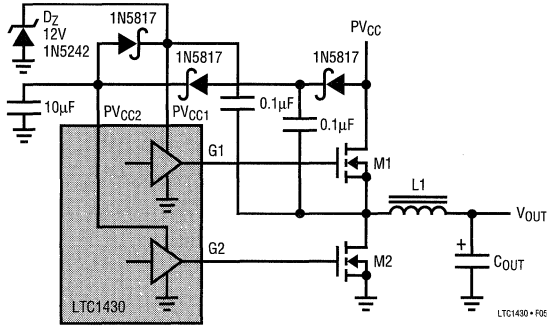


Figure 5. Tripling Charge Pump

EXTERNAL COMPONENT SELECTION

Power MOSFETs

Two N-channel power MOSFETs are required for most LTC1430 circuits. These should be selected based primarily on threshold and on-resistance considerations; thermal dissipation is often a secondary concern in high efficiency designs. Required MOSFET threshold should be determined based on the available power supply voltages and/or the complexity of the gate drive charge pump scheme. In 5V input designs where an auxiliary 12V supply is available to power PV_{CC1} and PV_{CC2}, standard MOSFETs with $R_{DS(ON)}$ specified at V_{GS} = 5V or 6V can be used with good results. The current drawn from this supply varies with the MOSFETs used and the LTC1430's operating frequency, but is generally less than 50mA.

LTC1430 designs that use a doubler charge pump to generate gate drive for M1 and run from PV_{CC} voltages below 7V cannot provide enough gate drive voltage to fully enhance standard power MOSFETs. When run from 5V, a doubler circuit may work with standard MOSFETs, but the MOSFET R_{ON} may be quite high, raising the dissipation in the FETs and costing efficiency. Logic level FETs are a better choice for 5V PV_{CC} systems; they can be fully enhanced with a doubler charge pump and will operate at maximum efficiency. Doubler designs running from PV_{CC} voltages near 4V will begin to run into efficiency problems even with logic level FETs; such designs should be built with tripler charge pumps (see Figure 5) or with newer, super low threshold MOSFETs. Note that doubler charge pump designs running from more than 7V and all tripler charge pump designs should include a zener clamp diode D_Z at PV_{CC1} to prevent transients from exceeding the absolute maximum rating at that pin.

Once the threshold voltage has been selected, R_{ON} should be chosen based on input and output voltage, allowable power dissipation and maximum required output current. In a typical LTC1430 buck converter circuit operating in continuous mode, the average inductor current is equal to the output load current. This current is always flowing through either M1 or M2 with the power dissipation split up according to the duty cycle:

$$DC\ (M1) = \frac{V_{OUT}}{V_{IN}}$$

$$DC\ (M2) = 1 - \frac{V_{OUT}}{V_{IN}} = \frac{(V_{IN} - V_{OUT})}{V_{IN}}$$

The R_{ON} required for a given conduction loss can now be calculated by rearranging the relation $P = I^2R$:

$$R_{ON}\ (M1) = \frac{P_{MAX}\ (M1)}{DC\ (M1) \times I_{MAX}^2} = \frac{V_{IN} \times P_{MAX}\ (M1)}{V_{OUT} \times I_{MAX}^2}$$

APPLICATIONS INFORMATION

$$R_{ON}(M2) = \frac{P_{MAX}(M2)}{DC(M2) \times I_{MAX}^2}$$

$$= \frac{V_{IN} \times P_{MAX}(M2)}{(V_{IN} - V_{OUT}) \times I_{MAX}^2}$$

P_{MAX} should be calculated based primarily on required efficiency. A typical high efficiency circuit designed for 5V in, 3.3V at 10A out might require no more than 3% efficiency loss at full load for each MOSFET. Assuming roughly 90% efficiency at this current level, this gives a P_{MAX} value of $(3.3V \times 10A/0.9) \times 0.03 = 1.1W$ per FET and a required R_{ON} of:

$$R_{ON}(M1) = \frac{5V \times 1.1W}{3.3V \times 10A^2} = 0.017\Omega$$

$$R_{ON}(M2) = \frac{5V \times 1.1W}{(5V - 3.3V) \times 10A^2} = 0.032\Omega$$

Note that the required R_{ON} for M2 is roughly twice that of M1 in this example. This application might specify a single 0.03Ω device for M2 and parallel two more of the same devices to form M1. Note also that while the required R_{ON} values suggest large MOSFETs, the dissipation numbers are only 1.1W per device or less — large TO-220 packages and heat sinks are not necessarily required in high efficiency applications. Siliconix Si4410DY (in SO-8) and Motorola MTD20N03HL (in DPAK) are two small, surface mount devices with R_{ON} values of 0.03Ω or below with 5V of gate drive; both work well in LTC1430 circuits with up to 10A output current. A higher P_{MAX} value will generally decrease MOSFET cost and circuit efficiency and increase MOSFET heat sink requirements.

Inductor

The inductor is often the largest component in an LTC1430 design and should be chosen carefully. Inductor value and type should be chosen based on output slew rate requirements and expected peak current. Inductor value is primarily controlled by the required current slew rate. The maximum rate of rise of the current in the inductor is set by its value, the input-to-output voltage differential and the maximum duty cycle of the LTC1430. In a typical 5V to 3.3V application, the maximum rise time will be:

$$90\% \times \frac{(V_{IN} - V_{OUT})}{L} \frac{AMPS}{SECOND} = \frac{1.53A}{\mu s} \frac{I}{L}$$

where L is the inductor value in µH. A 2µH inductor would have a 0.76A/µs rise time in this application, resulting in a 6.5µs delay in responding to a 5A load current step. During this 6.5µs, the difference between the inductor current and the output current must be made up by the output capacitor, causing a temporary droop at the output. To minimize this effect, the inductor value should usually be in the 1µH to 5µH range for most typical 5V to 3.xV LTC1430 circuits. Different combinations of input and output voltages and expected loads may require different values.

Once the required value is known, the inductor core type can be chosen based on peak current and efficiency requirements. Peak current in the inductor will be equal to the maximum output load current added to half the peak-to-peak inductor ripple current. Ripple current is set by the inductor value, the input and output voltage and the operating frequency. If the efficiency is high and can be approximately equal to 1, the ripple current is approximately equal to:

$$\Delta I = \frac{(V_{IN} - V_{OUT})}{f_{OSC} \times L} \times DC$$

$$DC = \frac{V_{OUT}}{V_{IN}}$$

f_{OSC} = LTC1430 oscillator frequency
L = inductor value

Solving this equation with our typical 5V to 3.3V application, we get:

$$\frac{1.7 \times 0.66}{200kHz \times 2\mu H} = 2.8A_{P-P}$$

Peak inductor current at 10A load:

$$10A + \frac{2.8A}{2} = 11.4A$$

The inductor core must be adequate to withstand this peak current without saturating, and the copper resistance in the winding should be kept as low as possible to minimize resistive power loss. Note that the current may rise above

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this maximum level in circuits under current limit or under fault conditions in unlimited circuits; the inductor should be sized to withstand this additional current.

Input and Output Capacitors

A typical LTC1430 design puts significant demands on both the input and output capacitors. Under normal steady load operation, a buck converter like the LTC1430 draws square waves of current from the input supply at the switching frequency, with the peak value equal to the output current and the minimum value near zero. Most of this current must come from the input bypass capacitor, since few raw supplies can provide the current slew rate to feed such a load directly. The resulting RMS current flow in the input capacitor will heat it up, causing premature capacitor failure in extreme cases. Maximum RMS current occurs with 50% PWM duty cycle, giving an RMS current value equal to $I_{OUT}/2$. A low ESR input capacitor with an adequate ripple current rating must be used to ensure reliable operation. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours (3 months) lifetime; further derating of the input capacitor ripple current beyond the manufacturer's specification is recommended to extend the useful life of the circuit.

The output capacitor in a buck converter sees much less ripple current under steady-state conditions than the input capacitor. Peak-to-peak current is equal to that in the inductor, usually a fraction of the total load current. Output capacitor duty places a premium not on power dissipation but on ESR. During an output load transient, the output capacitor must supply all of the additional load current demanded by the load until the LTC1430 can adjust the inductor current to the new value. ESR in the output capacitor results in a step in the output voltage equal to the ESR value multiplied by the change in load current. A 5A load step with a 0.05Ω ESR output capacitor will result in a 250mV output voltage shift; this is a 7.6% output voltage shift for a 3.3V supply! Because of the strong relationship between output capacitor ESR and output load transient response, the output capacitor is usually chosen for ESR, not for capacitance value; a capacitor with suitable ESR will usually have a larger capacitance value than is needed to control steady-state output ripple.

Electrolytic capacitors rated for use in switching power supplies with specified ripple current ratings and ESR can be used effectively in LTC1430 applications. OS-CON electrolytic capacitors from Sanyo give excellent performance and have a very high performance/size ratio for an electrolytic capacitor. Surface mount applications can use either electrolytic or dry tantalum capacitors. Tantalum capacitors must be surge tested and specified for use in switching power supplies; low cost, generic tantalums are known to have very short lives followed by explosive deaths in switching power supply applications. AVX TPS series surface mount devices are popular tantalum capacitors that work well in LTC1430 applications. A common way to lower ESR and raise ripple current capability is to parallel several capacitors. A typical LTC1430 application might require an input capacitor with a 5A ripple current capacity and 2% output shift with a 10A output load step, which requires a 0.007Ω output capacitor ESR. Sanyo OS-CON part number 10SA220M (220µF/10V) capacitors feature 2.3A allowable ripple current at 85°C and 0.035Ω ESR; three in parallel at the input and six at the output will meet the above requirements.

Input Supply Considerations/Charge Pump

The 16-lead LTC1430 requires four supply voltages to operate: PV_{CC} for the main power input, PV_{CC1} and PV_{CC2} for MOSFET gate drive and a clean, low ripple V_{CC} for the LTC1430 internal circuitry (Figure 6). In many applications, PV_{CC} and PV_{CC2} can be tied together and fed from a common high power supply, provided that the supply voltage is high enough to fully enhance the gate of external MOSFET M2. This can be the 5V system supply if a logic level MOSFET is used for M2. V_{CC} can usually be filtered

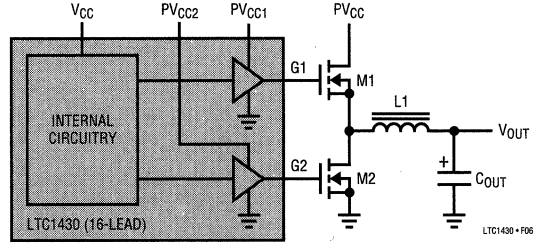

Figure 6. 16-Lead Power Supplies

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with an RC from this same high power supply; the low quiescent current (typically 350μA) allows the use of relatively large filter resistors and correspondingly small filter capacitors. 100Ω and 4.7μF usually provide adequate filtering for V_{CC}.

The 8-lead versions of the LTC1430 have the PV_{CC2} and V_{CC} pins tied together inside the package (Figure 7). This pin, brought out as V_{CC}/PV_{CC2}, has the same low ripple requirements as the 16-lead part, but must also be able to supply the gate drive current to M2. This can be obtained by using a larger RC filter from the PV_{CC} pin; 22Ω and 10μF work well here. The 10μF capacitor must be VERY close to the part (preferably right underneath the unit) or output regulation may suffer.

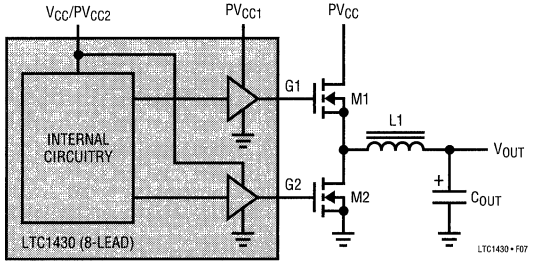

Figure 7. 8-Lead Power Supplies

For both versions of the LTC1430, PV_{CC1} must be higher than PV_{CC} by at least one external MOSFET $V_{GS(ON)}$ to fully enhance the gate of M1. This higher voltage can be provided with a separate supply (typically 12V) which should power up after PV_{CC}, or it can be generated with a simple charge pump (Figure 4). The charge pump consists of a 1N4148 diode from PV_{CC} to PV_{CC1} and a 0.1μF capacitor from PV_{CC1} to the switching node at the drain of M2. This circuit provides $2PV_{CC} - V_F$ to PV_{CC1} while M1 is ON and $PV_{CC} - V_F$ while M1 is OFF where V_F is the ON voltage of the 1N4148 diode. Ringing at the drain of M2 can cause transients above $2PV_{CC}$ at PV_{CC1}; if PV_{CC} is higher than 7V, a 12V zener diode should be included from PV_{CC1} to PGND to prevent transients from damaging the circuitry at PV_{CC2} or the gate of M1.

More complex charge pumps can be constructed with the 16-lead versions of the LTC1430 to provide additional voltages for use with standard threshold MOSFETs or very low PV_{CC} voltages. A tripling charge pump (Figure 5) can provide $2PV_{CC}$ and $3PV_{CC}$ voltages. These can be connected to PV_{CC2} and PV_{CC1} respectively, allowing standard threshold MOSFETs to be used with 5V at PV_{CC} or 5V logic level threshold MOSFETs to be used with 3.3V at PV_{CC}. V_{CC} can be driven from the same potential as PV_{CC2}, allowing the entire system to run from a single 3.3V supply. Tripling charge pumps require the use of Schottky diodes to minimize forward drop across the diodes at start-up. The tripling charge pump circuit will tend to rectify any ringing at the drain of M2 and can provide well more than $3PV_{CC}$ at PV_{CC1}; all tripling (or higher multiplying factor) circuits should include a 12V zener clamp diode D_Z to prevent overvoltage at PV_{CC1}.

Compensation and Transient Response

The LTC1430 voltage feedback loop is compensated at the COMP pin; this is the output node of the internal g_m error amplifier. The loop can generally be compensated properly with an RC network from COMP to GND and an additional small C from COMP to GND (Figure 8). Loop stability is affected by inductor and output capacitor values and by other factors. Optimum loop response can be obtained by using a network analyzer to find the loop poles and zeros; nearly as effective and a lot easier is to empirically tweak the R_C values until the transient recovery looks right with an output load step. Table 1 shows recommended compensation components for 5V to 3.3V applications based on the inductor and output capacitor values. The values were calculated using multiple paralleled 330μF AVX TPS series surface mount tantalum capacitors as the output capacitor.

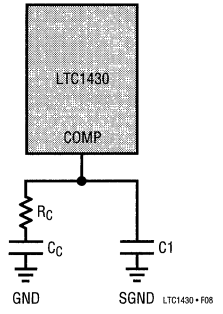

Figure 8. Compensation Pin Hook-Up

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Table 1. Recommended Compensation Network for 5V to 3.3V Application Using Multiple 330µF AVX Output Capacitors

L1 (µH)	C_{OUT} (µF)	R_C (kΩ)	C_C (µF)	C1 (pF)
1	990	1.8	0.022	820
1	1980	3.6	0.01	470
1	4950	9.1	0.0047	150
1	9900	18	0.0022	82
2.7	990	3.6	0.01	470
2.7	1980	7.5	0.0047	220
2.7	4950	18	0.0022	82
2.7	9900	39	0.001	39
5.6	990	9.1	0.0047	150
5.6	1980	18	0.0022	82
5.6	4950	47	820pF	33
5.6	9900	91	470pF	15
10	990	18	0.0022	82
10	1980	39	0.001	39
10	4950	91	470pF	15
10	9900	180	220pF	10

Output transient response is set by three major factors: the time constant of the inductor and the output capacitor, the ESR of the output capacitor, and the loop compensation components. The first two factors usually have much more impact on overall transient recovery time than the third; unless the loop compensation is way off, more improvement can be had by optimizing the inductor and the output capacitor than by fiddling with the loop compensation components. In general, a smaller value inductor will improve transient response at the expense of ripple and inductor core saturation rating. Minimizing output capacitor ESR will also help optimize output transient response. See Input and Output Capacitors for more information.

Soft Start and Current Limit

The 16-lead versions of the LTC1430 include a soft start circuit at the SS pin; this circuit is used both for initial start-up and during current limit operation. The soft start and current limit circuitry is disabled in 8-lead versions. SS requires an external capacitor to GND with the value determined by the required soft start time. An internal 12µA current source is included to charge the external capacitor. Soft start functions by clamping the maximum voltage that the COMP pin can swing to, thereby controlling the duty cycle (Figure 9). The LTC1430 will begin to operate at low duty cycle as the SS pin rises to about 2V below V_{CC}. As SS continues to rise, the duty cycle will increase until the error amplifier takes over and begins to regulate the output. When SS reaches 1V below V_{CC} the LTC1430 will be in full operation. An internal switch shorts the SS pin to GND during shutdown.

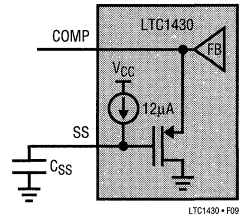

Figure 9. Soft Start Clamps COMP Pin

The LTC1430 detects the output current by watching the voltage at I_{FB} while M1 is ON. The I_{LIM} amplifier compares this voltage to the voltage at I_{MAX} (Figure 10). In the ON state, M1 has a known resistance; by calculating backwards, the voltage generated at I_{FB} by the maximum output current in M1 can be determined. As I_{FB} falls below I_{MAX}, I_{LIM} will begin to sink current from the soft start pin, causing the voltage at SS to fall. As SS falls, it will limit the output duty cycle, limiting the current at the output. Eventually the system will reach equilibrium, where the pull-up current at the SS pin matches the pull-down current in the I_{LIM} amplifier; the LTC1430 will stay in this state until the overcurrent condition disappears. At this time I_{FB} will rise, I_{LIM} will stop sinking current and the internal pull-up will recharge the soft start capacitor, restoring normal operation. Note that the I_{FB} pin requires an external 1k series resistor to prevent voltage transients at the drain of M2 from damaging internal structures.

The I_{LIM} amplifier pulls current out of SS in proportion to the difference between I_{FB} and I_{MAX}. Under mild overload conditions, the SS pin will fall gradually, creating a time delay before current limit takes effect. Very short, mild overloads may not trip the current limit circuit at all. Longer overload conditions will allow the SS pin to reach

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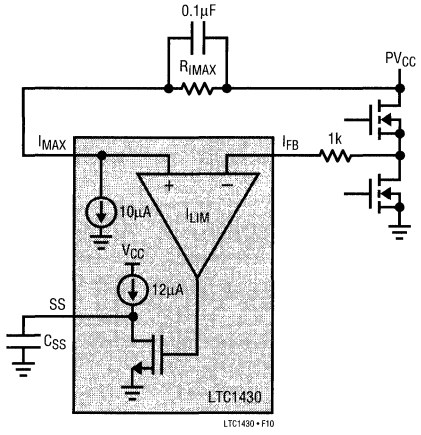

Figure 10. Current Limit Operation

a steady level, and the output will remain at a reduced voltage until the overload is removed. Serious overloads will generate a larger overdrive at I_{LIM}, allowing it to pull SS down more quickly and preventing damage to the output components.

The I_{LIM} amplifier output is disabled when M1 is OFF to prevent the low I_{FB} voltage in this condition from activating the current limit. It is re-enabled a fixed 170ns after M1 turns on; this allows for the I_{FB} node to slew back high and the I_{LIM} amplifier to settle to the correct value. As the LTC1430 goes deeper into current limit, it will reach a point where the M1 on-time needs to be cut to below 170ns to control the output current. This conflicts with the minimum settling time needed for proper operation of the I_{LIM} amplifier. At this point, a secondary current limit circuit begins to reduce the internal oscillator frequency, lengthening the off-time of M1 while the on-time remains constant at 170ns. This further reduces the duty cycle, allowing the LTC1430 to maintain control over the output current.

Under extreme output overloads or short circuits, the I_{LIM} amplifier will pull the SS pin more than 2V below V_{CC} in a single switching cycle, cutting the duty cycle to zero. At this point all switching stops, the output current decays through M2 and the LTC1430 runs a partial soft start cycle and restarts. If the short is still present the cycle will repeat. Peak currents can be quite high in this condition, but the average current is controlled and a properly designed circuit can withstand short circuits indefinitely with only moderate heat rise in the output FETs. In addition, the soft start cycle repeat frequency can drop into the low kHz range, causing vibrations in the inductor which provide an audible alarm that something is wrong.

Oscillator Frequency

The LTC1430 includes an onboard current controlled oscillator which will typically free-run at 200kHz. An internal 20µA current is summed with any current in or out of the FREQSET pin (pin 11), setting the oscillator frequency to approximately 10kHz/µA. FREQSET is internally servoed to the LTC1430 reference voltage (1.26V). With FREQSET floating, the oscillator is biased from the internal 20µA source and runs at 200kHz. Connecting a 50k resistor from FREQSET to ground will sink an additional 25µA from FREQSET, causing the internal oscillator to run at approximately 450kHz. Sourcing an external 10µA current into FREQSET will cut the internal frequency to 100kHz. An internal clamp prevents the oscillator from running slower than about 50kHz. Tying FREQSET to V_{CC} will cause it to run at this minimum speed.

Shutdown

The LTC1430 includes a low power shutdown mode, controlled by the logic at the $\overline{SHDN}$ pin. A high at $\overline{SHDN}$ allows the part to operate normally. A low level at $\overline{SHDN}$ stops all internal switching, pulls COMP and SS to ground internally and turns M1 and M2 off. In shutdown, the LTC1430 itself will drop below 1µA quiescent current typically, although off-state leakage in the external MOSFETs may cause the total PV_{CC} current to be somewhat higher, especially at elevated temperatures. When $\overline{SHDN}$ rises again, the LTC1430 will rerun a soft start cycle and resume normal operation. Holding the LTC1430 in shutdown during PV_{CC} power up removes any PV_{CC1} sequencing constraints.

LAYOUT CONSIDERATIONS

Grounding

Proper grounding is critical for the LTC1430 to obtain specified output regulation. Extremely high peak currents

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(as high as several amps) can flow between the bypass capacitors and the PV_{CC1}, PV_{CC2} and PGND pins. These currents can generate significant voltage differences between two points that are nominally both "ground." As a general rule, GND and PGND should be totally separated on the layout, and should be brought together at only one point, right at the LTC1430 GND and PGND pins. This helps minimize internal ground disturbances in the LTC1430 by keeping PGND and GND at the same potential, while preventing excessive current flow from disrupting the operation of the circuits connected to GND. The PGND node should be as compact and low impedance as possible, with the negative terminals of the input and output capacitors, the source of M2, the LTC1430 PGND node, the output return and the input supply return all clustered at one point. Figure 11 is a modified schematic showing the common connections in a proper layout. Note that at 10A current levels or above, current density in the PC board itself can become a concern; traces carrying high currents should be as wide as possible.

Output Voltage Sensing

The LTC1430 provides three pins for sensing the output voltage: $SENSE^+$, $SENSE^-$ and FB. $SENSE^+$ and $SENSE^-$ connect to an internal resistor divider which is connected to FB. To set the output of the LTC1430 to 3.3V, connect $SENSE^+$ to the output as near to the load as practical and connect $SENSE^-$ to the common GND/PGND point. Note that $SENSE^-$ is not a true differential input sense input; it is just the bottom of the internal divider string. Connecting $SENSE^-$ to the ground near the load will not improve load regulation. For any other output voltage, the $SENSE^+$ and $SENSE^-$ pins should be floated and an external resistor string should be connected to FB (Figure 12). As before, connect the top resistor (R1) to the output as close to the load as practical and connect the bottom resistor (R2) to the common GND/PGND point. In both cases, connecting the top of the resistor divider (either $SENSE^+$ or R1) close to the load can significantly improve load regulation by compensating for any drops in PC traces or hookup wires between the LTC1430 and the load.

Power Component Hook-Up/Heat Sinking

As current levels rise much above 1A, the power components supporting the LTC1430 start to become physically large (relative to the LTC1430, at least) and can require special mounting considerations. Input and output capacitors need to carry high peak currents and must have

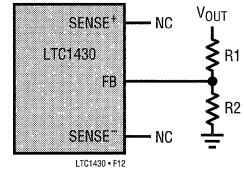

Figure 12. Using External Resistors to Set Output Voltages

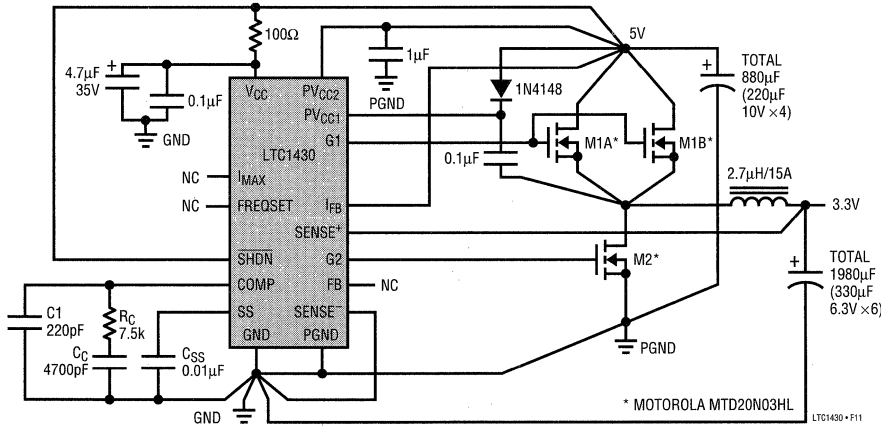

Figure 11. Typical Schematic Showing Layout Considerations

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ow ESR; this mandates that the leads be clipped as short as possible and PC traces be kept wide and short. The power inductor will generally be the most massive single component on the board; it can require a mechanical hold-down in addition to the solder on its leads, especially if it s a surface mount type.

The power MOSFETs used require some care to ensure proper operation and reliability. Depending on the current evels and required efficiency, the MOSFETs chosen may be as large as TO-220s or as small as SO-8s. High efficiency circuits may be able to avoid heat sinking the power devices, especially with TO-220 type MOSFETs. As an example, a 90% efficient converter working at a steady 3.3V/10A output will dissipate only (33W/90%) × 10% = 3.7W. The power MOSFETs generally account for the majority of the power lost in the converter; even assuming that they consume 100% of the power used by the converter, that's only 3.7W spread over two or three devices. A typical SO-8 MOSFET with a R_{ON} suitable to provide 90% efficiency in this design can commonly dissipate 2W when soldered to an appropriately sized piece of copper trace on a PC board. Slightly less efficient or higher output current designs can often get by with standing a TO-220 MOSFET straight up in an area with some airflow; such an arrangement can dissipate as much as 3W without a heat sink. Designs which must work in high ambient temperatures or which will be routinely overloaded will generally fare best with a heat sink.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1142	Current Mode Dual Step-Down Switching Regulator Controller	Dual Version of LTC1148
LTC1148	Current Mode Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 20V$
LTC1149	Current Mode Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 48V$, For Standard Threshold FETs
LTC1159	Current Mode Step-Down Switching Regulator Controller	Synchronous, $V_{IN} \leq 40V$, For Logic Threshold FETs
LTC1266	Current Mode Step-Up/Down Switching Regulator Controller	Synchronous N- or P-Channel FETs, Comparator/ Low-Battery Detector
LTC1267	Current Mode Dual Step-Down Switching Regulator Controller	Dual Version of LTC1159

100kHz, 1.25A Switching Regulator with Catch Diode

FEATURES

- **Catch Diode Included in Package**
- Wide Input Voltage Range: 3V to 30V
- Low Quiescent Current: 6mA
- **Internal 1.25A Switch**
- Very Few External Parts Required
- Self-Protected Against Overloads
- **Operates in Nearly All Switching Topologies**
- Shutdown Mode Draws Only 50µA Typical Current
- Can Be Externally Synchronized

APPLICATIONS

- 3.3V-to-5V and 5V-to-12V Boost Converters
- Negative-to-Positive Converter
- SEPIC Converter (Input Can Be Greater or Less Than Output)
- Battery Charger

DESCRIPTION

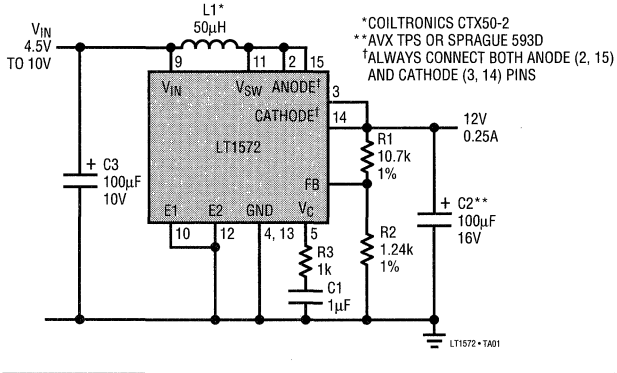
The LT®1572 is a 1.25A 100kHz monolithic switching regulator with on-board switch and catch diode included in one package. It combines an LT1172 with a 1A Schottky catch diode. The LT1572 can be operated in all standard switching configurations, including boost, buck, SEPIC, flyback, forward, inverting and "Cuk". All necessary control, oscillator and protection circuitry is included on the die with the high efficiency switch. This makes the part extremely easy to use and provides "bustproof" operation similar to that obtained with 3-pin linear regulators.

The LT1572 operates with supply voltages from 3V to 30V and draws only 6mA quiescent current. It can deliver load power up to 15W with no external power devices. By utilizing a current mode switching technique, the LT1572 achieves excellent response to load and line transients.

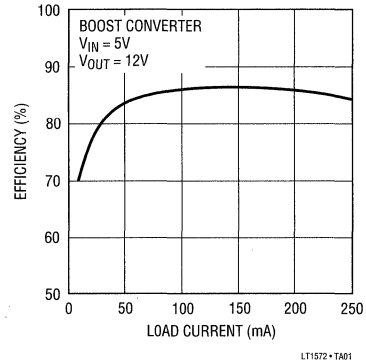
The LT1572 has many unique features not found on the more difficult to use control chips presently available. It uses adaptive anti-sat switch drive to allow very wide ranging load currents with no loss in efficiency. An externally activated shutdown mode reduces total supply current to 50µA typical for standby operation. External synchronizing of switching frequency is possible, with a range of 120kHz to 160kHz.

TYPICAL APPLICATION

5V-to-12V Boost Converter



Boost Converter Efficiency



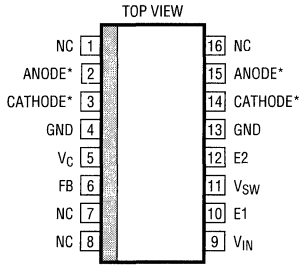
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 4) 40V
Switch Output Voltage (Note 4) 60V
Feedback Pin Voltage (Transient, 1ms) ..... ±15V
Operating Junction Temperature Range
  Operating ..... 0°C to 100°C
  Short Circuit ..... 0°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

DIODE

Average Forward Current 1A
Peak Repetitive Forward Current 2A
Peak Non-Repetitive Forward Current 3A
Peak Repetitive Reverse Voltage 20V
Continuous (Average) Reverse Voltage 15V
Operating Junction Temperature ..... 125°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

*ALWAYS CONNECT BOTH ANODE AND BOTH CATHODE PINS

T_{JMAX} (REGULATOR) = 100°C
T_{JMAX} (DIODE) = 125°C
SEE THERMAL MANAGEMENT SECTION FOR θ_{JA}

ORDER PART NUMBER
LT1572CS

Consult factory for Industrial and Military grade parts.

Note 1: Minimum effective switch "on" time for the LT1572 (in current limit only) is ≈ 0.6µs. This limits the maximum safe input voltage during an output shorted condition. Buck mode and inverting mode input voltage during an output shorted condition is limited to:

V_{IN} (max, output shorted) = 15V + $\frac{R \times I_L + V_f}{t \times f}$
buck and inverting mode

R = Inductor DC resistance

I_L = 2.5A

V_f = Output catch diode forward voltage at I_L

t = 0.6µs, f = 100kHz switching frequency

Maximum input voltage can be increased by increasing R or V_f.

External current limiting such as that shown in AN19, Figure 39, will provide protection up to the full supply voltage rating. C1 in Figure 39 should be reduced to 200pF.

Transformer designs will tolerate much higher input voltages because leakage inductance limits rate of rise of current in the switch. These designs must be evaluated individually to assure that current limit is well controlled up to maximum input voltage.

Boost mode designs are never protected against output shorts because the external catch diode and inductor connect input to output.

4

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin		1.224	1.244	1.264	V
		V_C = 0.8V	●	1.214	1.244	1.274	V
I_B	Feedback Input Current	V_{FB} = V_{REF}			350	750	nA
			●			1100	nA
g_m	Error Amplifier Transconductance	ΔI_C = ±25µA		3000	4400	6000	µmho
			●	2400		7000	µmho
	Error Amplifier Source or Sink Current	V_C = 1.5V		150	200	350	µA
			●	120		400	µA
	Error Amplifier Clamp Voltage	Hi Clamp, V_{FB} = 1V		1.80		2.30	V
		Lo Clamp, V_{FB} = 1.5V		0.25	0.38	0.52	V
	Reference Voltage Line Regulation	3V ≤ V_{IN} ≤ 40V, V_C = 0.8V	●			0.03	%/V
A_V	Error Amplifier Voltage Gain	0.9V ≤ V_C ≤ 1.4V		500	800		V/V
	Minimum Input Voltage (Note 3)		●		2.6	3.0	V
I_Q	Supply Current	3V ≤ V_{IN} ≤ 40V, V_C = 0.6V			6	9	mA

ELECTRICAL CHARACTERISTICS

V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Control Pin Threshold	Duty Cycle = 0		0.8	0.9	1.08	V
			●	0.6		1.25	V
	Normal/Flyback Threshold on Feedback Pin			0.4	0.45	0.54	V
V_{FB}	Flyback Reference Voltage (Note 3)	I_{FB} = 50µA		15.0	16.3	17.6	V
			●	14.0		18.0	V
	Change in Flyback Reference Voltage	0.05 ≤ I_{FB} ≤ 1mA		4.5	6.8	9	V
	Flyback Reference Voltage Line Regulation (Note 3)	I_{FB} = 50µA 7V ≤ V_{IN} ≤ V_{MAX}			0.01	0.03	%/V
	Flyback Amplifier Transconductance (g_m)	ΔI_C = ±10µA		150	300	500	µmho
	Flyback Amplifier Source and Sink Current	V_C = 0.6V, Source	●	15	32	70	µA
		I_{FB} = 50µA, Sink	●	25	40	70	µA
BV	Output Switch Breakdown Voltage (Note 4)	3V ≤ V_{IN} ≤ 40V, I_{SW} = 1.5mA	●	60	80		V
V_{SAT}	Output Switch "On" Resistance (Note 1)		●		0.60	1.00	Ω
	Control Voltage to Switch Current Transconductance				2		A/V
I_{LIM}	Switch Current Limit	Duty Cycle = 50%, T_J ≥ 25°C	●	1.25		3.0	A
		Duty Cycle = 50%, T_J < 25°C	●	1.25		3.5	A
		Duty Cycle = 80% (Note 2)	●	1.00		2.5	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time				25	35	mA/A
f	Switching Frequency			88	100	112	kHz
			●	85		115	kHz
DC_{MAX}	Maximum Switch Duty Cycle		●	80	90	95	%
	Shutdown Mode Supply Current	3V ≤ V_{IN} ≤ 40V V_C = 0.05V			100	250	µA
	Shutdown Mode Threshold Voltage	3V ≤ V_{IN} ≤ 40V		100	150	250	mV
			●	50		300	mV
	Flyback Sense Delay Time (Note 3)				1.5		µs

DIODE

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Forward Voltage (Note 5)	I_f = 200mA	●		0.45	0.57	V
	I_f = 500mA	●		0.52	0.65	V
	I_f = 1A	●		0.55	0.70	V
Reverse Leakage (Note 5)	V_R = 5V, T_J = 25°C			1	5	µA
	V_R = 5V, T_J = 75°C			25	100	µA
	V_R = 20V, T_J = 25°C			3	15	µA
	V_R = 20V, T_J = 75°C			70	300	µA
Diode Thermal Resistance	(Note 6)			90		°C/W

ELECTRICAL CHARACTERISTICS V_{IN} = 15V, V_C = 0.5V, V_{FB} = V_{REF}, output pin open, unless otherwise noted.

The ● denotes the specifications which apply over the full operating temperature range, 0°C to 100°C for the regulator chip and 0°C to 125°C for the diode.

Note 1: Measured with V_C in hi clamp, V_{FB} = 0.8V. I_{SW} = 1A.

Note 2: For duty cycles (DC) between 50% and 80%, minimum guaranteed switch current is given by I_{LIM} = 0.833 (2 – DC).

Note 3: Minimum input voltage for isolated flyback mode is 7V.

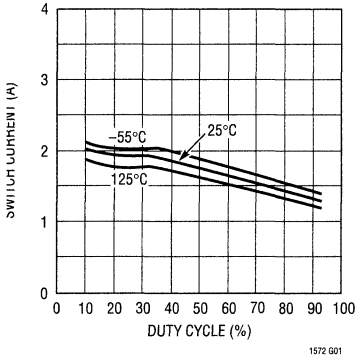
Note 4: Because the catch diode has a peak repetitive reverse voltage of 20V, diode breakdown may be the limiting factor on input voltage or switch voltage in many applications.

Note 5: See graphs for guaranteed forward voltage and reverse leakage current over temperature. Parameters are 100% tested at 25°C and guaranteed at other temperatures by design and QA sampling.

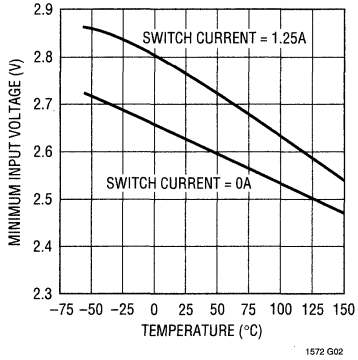
Note 6: Package soldered to FR4 board with ≥1oz copper and an internal or backside plane underneath the package to aid thermal transfer. Diode is partly thermally coupled to regulator section. See Application Information section for details on thermal calculations.

TYPICAL PERFORMANCE CHARACTERISTICS

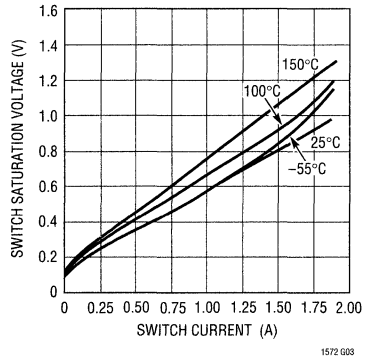
Switch Current Limit vs Duty Cycle



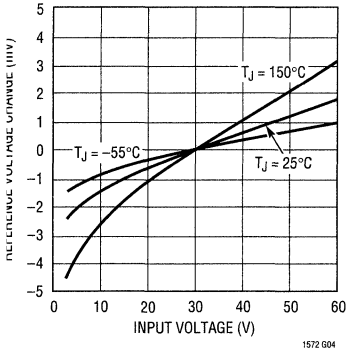
Minimum Input Voltage



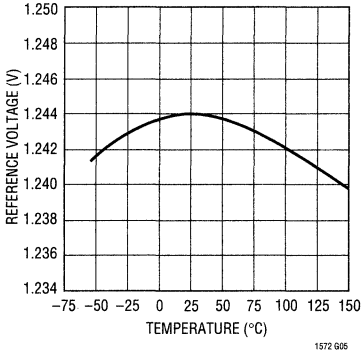
Switch Saturation Voltage



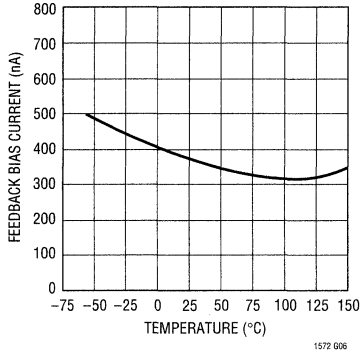
Line Regulation



Reference Voltage vs Temperature



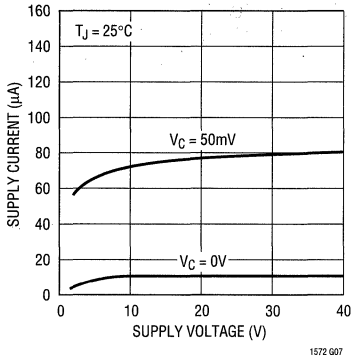
Feedback Bias Current vs Temperature



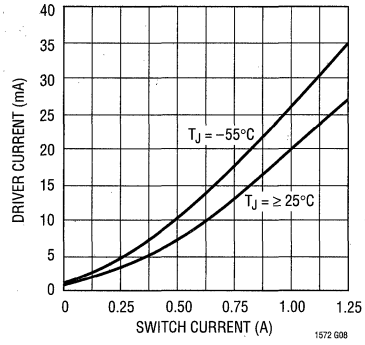
4

TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage (Shutdown Mode)

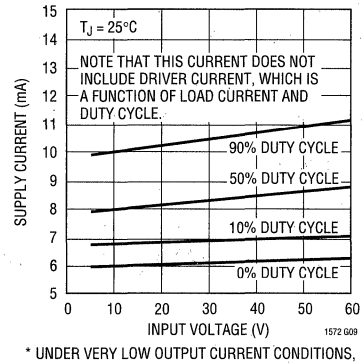


Driver Current* vs Switch Current



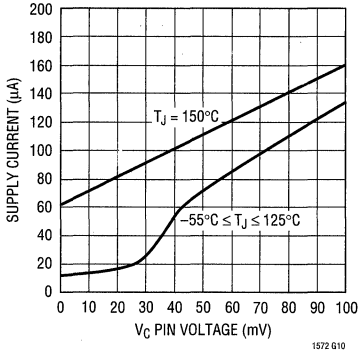
* AVERAGE POWER SUPPLY CURRENT IS FOUND BY MULTIPLYING DRIVER CURRENT BY DUTY CYCLE, THEN ADDING QUIESCENT CURRENT.

Supply Current vs Input Voltage*

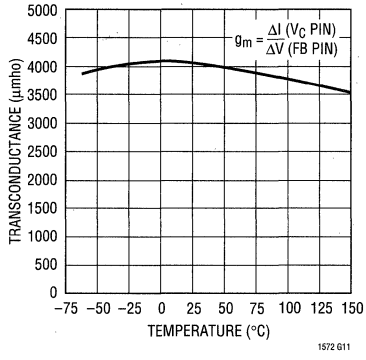


* UNDER VERY LOW OUTPUT CURRENT CONDITIONS, DUTY CYCLE FOR MOST CIRCUITS WILL APPROACH 10% OR LESS.

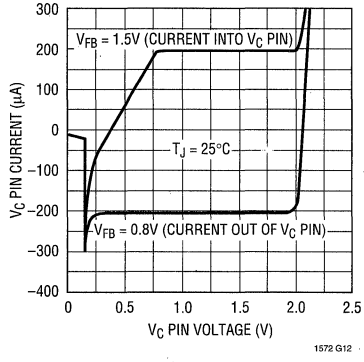
Shutdown Mode Supply Current



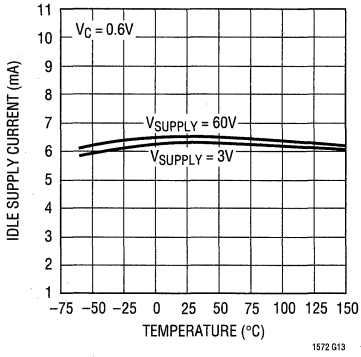
Error Amplifier Transconductance



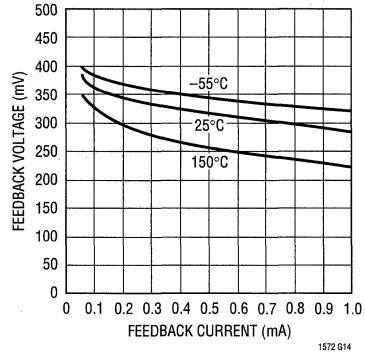
V_C Pin Characteristics



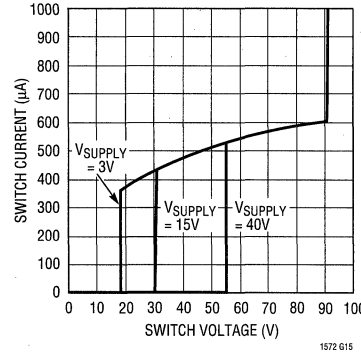
Idle Supply Current vs Temperature



Feedback Pin Clamp Voltage

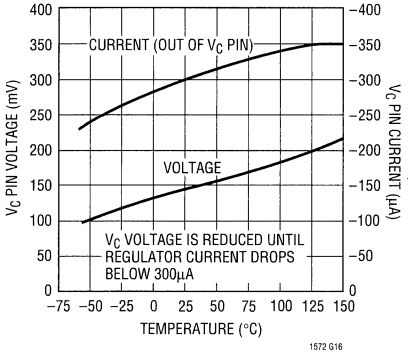


Switch "Off" Characteristics

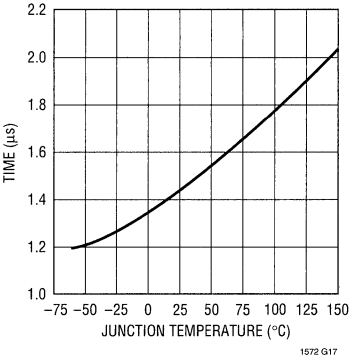


TYPICAL PERFORMANCE CHARACTERISTICS

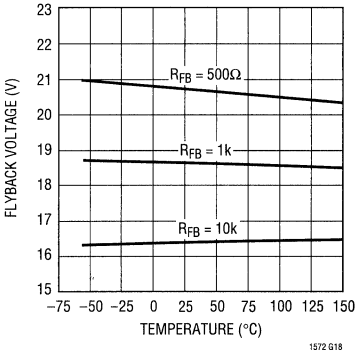
Shutdown Thresholds



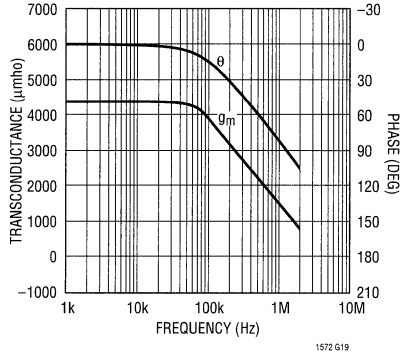
Flyback Blanking Time



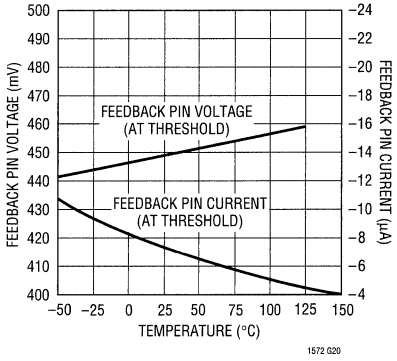
Isolated Mode Flyback Reference Voltage



Transconductance of Error Amplifier

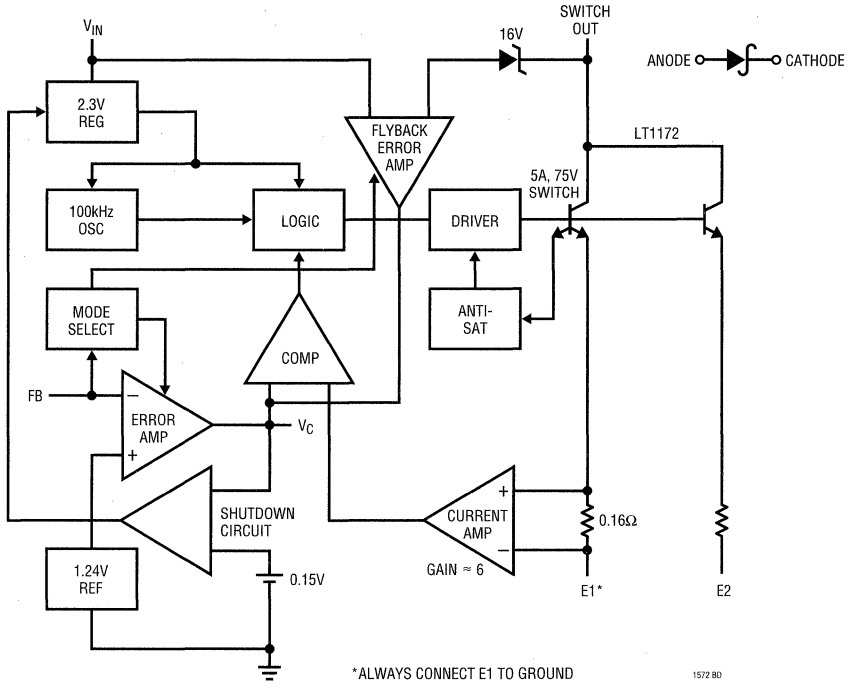


Normal/Flyback Mode Threshold on Feedback Pin



4

BLOCK DIAGRAM



OPERATION

The LT1572 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike ordinary switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions.

A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1572. This low dropout design allows input voltage to vary from 3V to 40V with virtually no change in device performance. A 100kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.2V bandgap reference biases the positive input of the error amplifier. The negative input is brought out for output voltage sensing. This feedback pin has a second function; when pulled low with an external resistor, it programs the LT1572 to disconnect the main error amplifier output and connects the output of the flyback amplifier

OPERATION

to the comparator input. The LT1572 will then regulate the value of the flyback pulse with respect to the supply voltage.[1] This flyback pulse is directly proportional to output voltage in the traditional transformer coupled flyback topology regulator. By regulating the amplitude of the flyback pulse, the output voltage can be regulated with no direct connection between input and output. The output is fully floating up to the breakdown voltage of the transformer windings. Multiple floating outputs are easily obtained with additional windings. A special delay network inside the LT1572 ignores the leakage inductance spike at the leading edge of the flyback pulse to improve output regulation.

The error signal developed at the comparator input is brought out externally. This pin (V_C) has four different functions. It is used for frequency compensation, current limit adjustment, soft starting, and total regulator shutdown. During normal regulator operation this pin sits at a voltage between 0.9V (low output current) and 2.0V (high output current). The error amplifiers are current output (g_m) types, so this voltage can be externally clamped for adjusting current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled to ground through a diode, placing the LT1572 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown, with only 50µA supply current for shutdown circuitry biasing. See AN19 for full application details.

E1 and E2 Pins

The LT1572 has the emitters of the power transistor brought out separately from the ground pin. This eliminates errors due to ground pin voltage drops and allows the user to reduce switch current limit 2:1 by leaving the second emitter (E2) disconnected. The first emitter (E1) should always be connected to the ground pin. Note that switch "on" resistance doubles when E2 is left open, so efficiency will suffer somewhat when switch currents exceed 300mA. Also, note that chip dissipation will actually *increase* with E2 open during normal load operation, even though dissipation in current limit mode will *decrease*.

[1]See note under block diagram.

Other Application Help

More circuits and application help for the LT1572 can be found in the LT1172 data sheet, both in loose form and in the *1994 Linear Databook Volume III*. Extensive additional help is contained in Application Note 19. All application circuits using the LT1172 can also use the LT1572 as long as the 20V maximum reverse voltage of the diode is not exceeded. A CAD program called SwitcherCAD is also available. This program can be used with the LT1572 by simply treating the LT1572 as an LT1172 and ignoring the predicted die temperature results obtained from SwitcherCAD itself.

Thermal Management

Thermal management is particularly important with the LT1572 because both switch and diode power dissipation increase rapidly at low input voltage when using the popular boost topology. Regulator and diode die temperature must be calculated *separately* because they are not connected to an isothermal plane inside the package. Diode *plus* regulator thermal resistance is approximately 70°C/W when the LT1572 is soldered to 1oz copper traces over an internal or backside copper plane using FR4 board material. However, individual calculation of die temperature must take thermal coupling into account. To accomplish this, thermal resistance is broken into two sections, a common (coupled) section and a second uncoupled section. Die temperatures are calculated from:

$$T_{REG} = T_A + P_{REG}\,(90°C/W) + P_{DIODE}\,(45°C/W)$$

$$T_{DIODE} = T_A + P_{DIODE}\,(90°C/W) + P_{REG}\,(45°C/W)$$

T_A = ambient temperature
T_{REG} = regulator die temperature
T_{DIODE} = diode die temperature
P_{REG} = total regulator power dissipation
P_{DIODE} = diode power dissipation

The following formulas can be used as a rough guide to calculate LT1572 power dissipation. For more details, the reader is referred to Application Note 19 (AN19), "Efficiency Calculations" section.

OPERATION

Average supply current (including driver current) is:

$I_{IN} \approx 6mA + I_{SW}(0.004 + DC/40)$

I_{SW} = switch current
DC = switch duty cycle

Switch power dissipation is given by:

$P_{SW} = (I_{SW})^2 \times R_{SW} \times DC$

R_{SW} = LT1572 switch "on" resistance (1Ω maximum)

Total power dissipation is the sum of supply current times input voltage plus switch power:

$P_{REG} = I_{IN} \times V_{IN} + P_{SW}$

In a typical example, using a boost converter to generate 12V at 0.12A from a 5V input, duty cycle is approximately 60%, and switch current is about 0.65A, yielding:

$I_{IN} = 6mA + 0.65(0.004 + DC/40) = 18mA$

$P_{SW} = (0.65)^2 \times 1\Omega \times 0.6 = 0.25W$

$P_{REG} = 5V \times 0.018A + 0.25 = 0.34W$

Approximate diode power dissipation for boost and buck converters is shown below. For other topologies or more accurate results, see Application Note 19 or use SwitcherCAD.

Boost: $P_{DIODE} = I_{OUT} \times V_f$

Buck: $P_{DIODE} = I_{OUT} \times V_f \times (V_{IN} - V_{OUT})/V_{IN}$

V_f = diode forward voltage at a current equal to I_{OUT} for a buck converter and $I_{OUT} \times V_{OUT}/V_{IN}$ for a boost converter.

In most applications, full load current is used to calculate die temperature. However, if overload conditions must also be accounted for, three approaches are possible. First, if loss of regulated output is acceptable under overload conditions, the internal *thermal limit* of the LT1572 will protect the die in most applications by shutting off switch current. *Thermal limit is not a tested parameter*, however, and should be considered only for noncritical applications with temporary overloads.

The second approach for lower current applications is to leave the second switch emitter (E2) open. This increases switch "on" resistance by 2:1, but reduces switch current limit by 2:1 also, resulting in a net 2:1 reduction in I^2R switch dissipation under current limit conditions.

The third approach is to clamp the V_C pin to a voltage less than its internal clamp level of 2V. The LT1172 switch current limit is zero at approximately 1V on the V_C pin and 2A at 2V on the V_C pin. Peak switch current can be externally clamped between these two levels with a diode. See AN19 for details.

Diode Characteristics

The catch diode used in the LT1572 is a power Schottky diode with a very low storage time and low forward voltage. This gives good efficiency in switching regulator applications, but some thought must be given to maximum operating voltage and high temperature reverse leakage. *Peak repetitive reverse voltage rating on the diode is 20V.* In a boost converter, maximum diode reverse voltage is equal to regulated output voltage, so this limits maximum output voltage to 20V. In a negative-to-positive converter, maximum diode voltage will be equal to the sum of output voltage *plus* input voltage. Use the equations in Application Note 19 or SwitcherCAD or calculate maximum diode voltage for other topologies.

Diode reverse leakage increases rapidly with temperature. This leakage is not high enough to significantly impact efficiency or diode power dissipation, but it can be of concern in shutdown mode if the diode is connected in such a way that the leakage adds to regulator shutdown current. Use the graphs of diode leakage versus voltage and temperature to ensure proper high temperature system performance.

The LT1572 diode is internally bonded to more than two package pins to reduce internal bond wire currents. *All pins must be used to prevent excessive current in the individual internal bond wires.* This is important in low load current applications because the LT1572 will draw high surge currents during start-up (to charge the output capacitor) even with no output load current.

OPERATION

Synchronizing

The LT1572 can be externally synchronized in the frequency range of 120kHz to 160kHz. This is accomplished as shown in the accompanying figures. Synchronizing occurs when the V_C pin is pulled to ground with an external transistor. To avoid disturbing the DC characteristics of the internal error amplifier, the width of the synchronizing pulse should be under 0.3µs. C2 sets the pulse width at ≅ 0.2µs. The effect of a synchronizing pulse on the LT1572 amplifier offset can be calculated from:

$$\Delta V_{OS} = \frac{\left(\frac{KT}{q}\right)(t_S)(f_S)\left(I_C + \frac{V_C}{R3}\right)}{I_C}$$

$\frac{KT}{q}$ = 26mV at 25°C

t_S = pulse width

f_S = pulse frequency

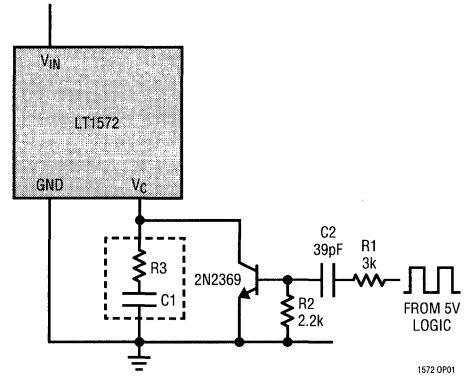
I_C = V_C source current (≈200µA)

V_C = operating V_C voltage (1V to 2V)

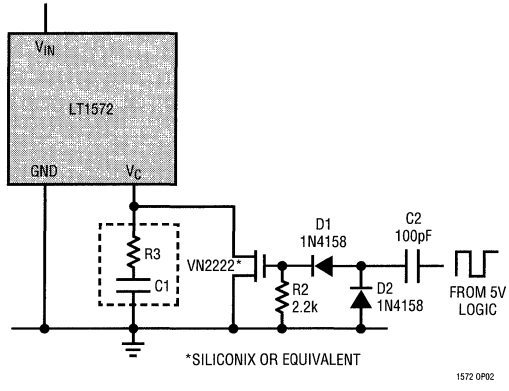
R3 = resistor used to set mid-frequency "zero" in frequency compensation network.

With t_S = 0.2µs, f_S = 150kHz, V_C = 1.5V, and R3 = 2k, offset voltage shift is ≈3.8mV. This is not particularly bothersome, but note that high offsets could result if R3 were reduced to a much lower value. Also, the synchronizing transistor must sink higher currents with low values of R3, so larger drives may have to be used. The transistor must be capable of pulling the V_C pin to within 200mV of ground to ensure synchronizing.

Synchronizing with Bipolar Transistor



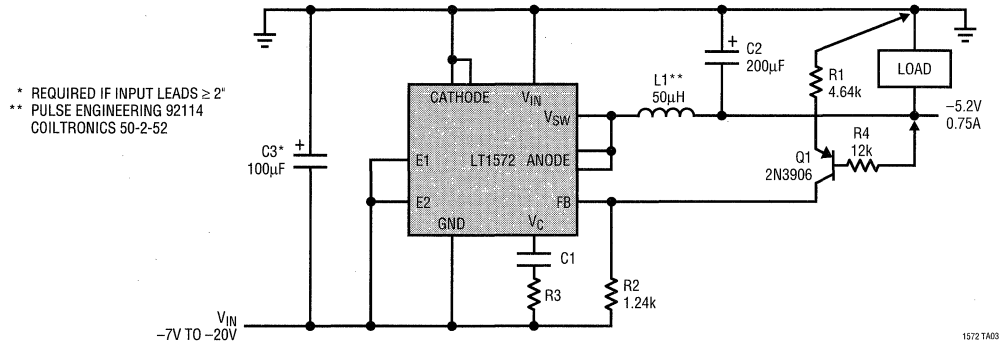
Synchronizing with MOS Transistor



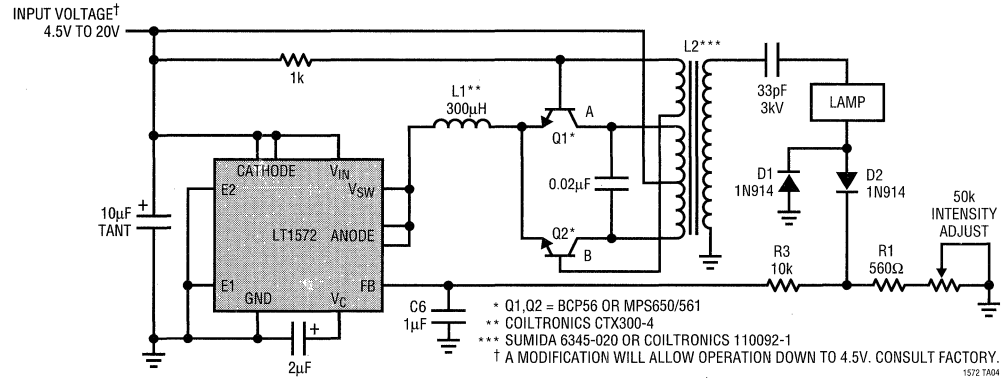
4

TYPICAL APPLICATIONS

Negative Buck Converter



Backlight CCFL Supply (see AN55 for details)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1172	100kHz, 1.25A High Efficiency Switching Regulator	LT1572 Without Diode
LT1173	Micropower DC/DC Converter Adjustable and Fixed 5V, 12V	Operates Down to 2V Input
LT1372	500kHz High Efficiency 1.5A Step-Up Switching Regulator	Latest Technology, Uses Tiny Inductors
LTC1574	High Efficiency Step-Down DC/DC Converter with Internal Schottky Diode	LTC1174 with Diode

High Efficiency Step-Down DC/DC Converters with Internal Schottky Diode

FEATURES

- **High Efficiency: Up to 94%**
- Usable in Noise-Sensitive Products
- Peak Inductor Current Independent of Inductor Value
- Short-Circuit Protection
- **Internal Low Forward Drop Schottky Diode**
- **Only Three External Components Required**
- Wide V_{IN} Range: 4V to 18.5V (Absolute Maximum)
- Low Dropout Operation
- Low-Battery Detector
- Pin Selectable Current Limit
- Internal 0.9Ω Power Switch: V_{IN} = 12V
- Standby Current: 130µA
- Active Low Micropower Shutdown

APPLICATIONS

- Inverting Converters
- Step-Down Converters
- Memory Backup Supply
- Portable Instruments
- Battery-Powered Equipment
- Distributed Power Systems

DESCRIPTION

The LTC®1574 is a family of easy-to-use current mode DC/DC converters ideally suited for 9V to 5V, 5V to 3.3V and inverting operation. With an internal 0.9Ω switch (at a supply voltage of 12V) and a low forward drop Schottky diode (0.450V typ at 200mA, T_A = 25°C), the LTC1574 requires only three external components to construct a complete high efficiency DC/DC converter.

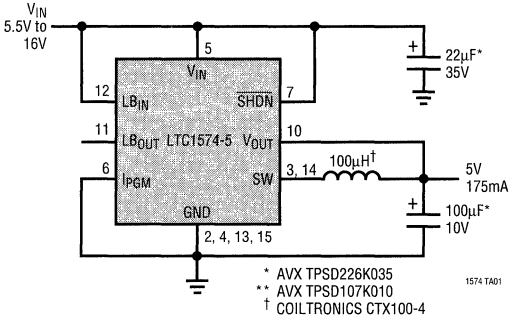
Under no load condition, the LTC1574 draws only 130µA. In shutdown, it draws a mere 2µA making this converter ideal for battery-powered applications. In dropout, the internal P-channel MOSFET switch is turned on continuously allowing the user to maximize the life of the battery source.

The maximum inductor current of the LTC1574 family is pin selectable to either 340mA or 600mA, optimizing efficiency for a wide range of applications. Operation up to 200kHz permits the use of small surface mount inductors and capacitors.

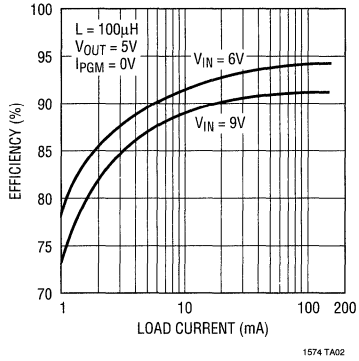
For applications requiring higher output current or ultra-high efficiency, see the LTC1148 and LTC1265 data sheets. For detailed applications information, see the LTC1174 data sheet.

TYPICAL APPLICATION

High Efficiency Step-Down Converter



LTC1574-5 Efficiency

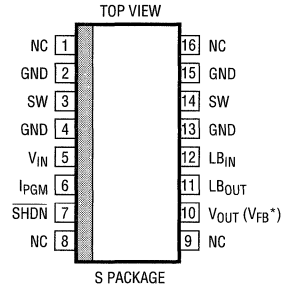


ABSOLUTE MAXIMUM RATINGS

(Voltage Referred to GND Pin)

Input Supply Voltage (Pin 5) ..... –0.3V to 18.5V
Switch Current (Pin 3, 14) 1A
Switch Voltage (Pin 3, 14) ..... V_{IN} – 18.5V
Operating Temperature Range ..... 0°C to 70°C
Junction Temperature (Note 1) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

*ADJUSTABLE OUTPUT VERSION

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER
LTC1574CS
LTC1574CS-3.3
LTC1574CS-5

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 9V, $V_{\overline{SHUTDOWN}}$ = V_{IN}, I_{PGM} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
I_{FB}	Feedback Current into Pin 10	LTC1574					1	µA
V_{FB}	Feedback Voltage	LTC1574		●	1.20	1.25	1.30	V
V_{OUT}	Regulated Output Voltage	LTC1574-3.3		●	3.14	3.30	3.46	V
		LTC1574-5		●	4.75	5.00	5.25	V
ΔV_{OUT}	Output Voltage Line Regulation	V_{IN} = 6V to 12V, I_{LOAD} = 100mA, I_{PGM} = V_{IN} (Note 2)				10	70	mV
	Output Voltage Load Regulation	LTC1574-3.3 (Note 2)	20mA < I_{LOAD} < 175mA, I_{PGM} = 0V			–5	–70	mV
			20mA < I_{LOAD} < 400mA, I_{PGM} = V_{IN}			–45	–70	mV
		LTC1574-5 (Note 2)	20mA < I_{LOAD} < 175mA, I_{PGM} = 0V			–5	–70	mV
			20mA < I_{LOAD} < 400mA, I_{PGM} = V_{IN}			–50	–70	mV
I_Q	Input DC Supply Current (Note 3)							
	Active Mode	4V < V_{IN} < 16V, I_{PGM} = 0V				450	600	µA
	Sleep Mode	4V < V_{IN} < 16V				130	180	µA
	$\overline{\text{Shutdown}}$ (Note 4)	$V_{\overline{SHUTDOWN}}$ = 0V, 4V < V_{IN} < 16V				2	25	µA
V_{LBTRIP}	Low-Battery Trip Point					1.25	1.4	V
I_{LBIN}	Current into Pin 12						0.5	µA
I_{LBOUT}	Current Sunk by Pin 11	V_{LBOUT} = 0.4V, V_{LBIN} = 0V			0.5	1.0	1.5	mA
		V_{LBOUT} = 5V, V_{LBIN} = 10V					1.0	µA
V_{HYST}	Comparator Hysteresis				7.5	15	30	mV
I_{PEAK}	Current Limit	I_{PGM} = V_{IN}, V_{OUT} = 0V		●	0.54	0.60	0.78	A
		I_{PGM} = 0V, V_{OUT} = 0V		●	0.27	0.34	0.50	A
R_{ON}	ON Resistance of Switch			●		0.9	1.55	Ω
t_{OFF}	Switch Off Time	V_{OUT} at Regulated Value			3	4	5	µs
V_{IH}	$\overline{\text{Shutdown}}$ Pin High	Minimum Voltage at Pin 7 for Device to Be Active			1.2			V
V_{IL}	$\overline{\text{Shutdown}}$ Pin Low	Maximum Voltage at Pin 7 for Device to Be in Shutdown					0.75	V
I_{IH}	$\overline{\text{Shutdown}}$ Pin Input Current	$V_{\overline{SHUTDOWN}}$ = 16V					2	µA

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 9V, $V_{\overline{SHUTDOWN}}$ = V_{IN}, I_{PGM} = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	$\overline{\text{Shutdown}}$ Pin Input Current	$0 \le V_{\overline{SHUTDOWN}} \le 0.8V$				0.5	µA
V_F	Schottky Diode Forward Voltage	Forward Current = 200mA			0.450	0.570	V
I_R	Schottky Reverse Current	Reverse Voltage = 5V Reverse Voltage = 18.5V			10 100	25 250	µA µA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

$T_J = T_A + (P_D \times 110°C/W)$

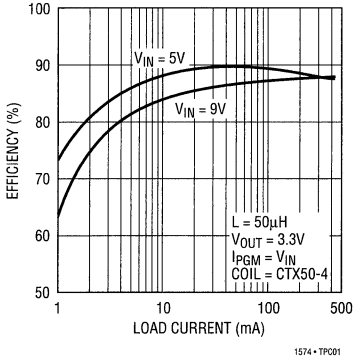
Note 2: Guaranteed by Design.

Note 3: Does not include Schottky reverse current. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

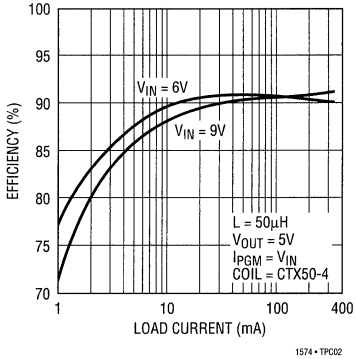
Note 4: Current into Pin 5 only, measured without electrolytic input capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

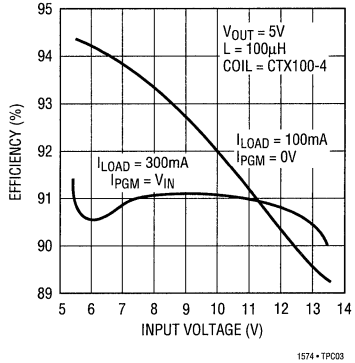
Efficiency vs Load Current



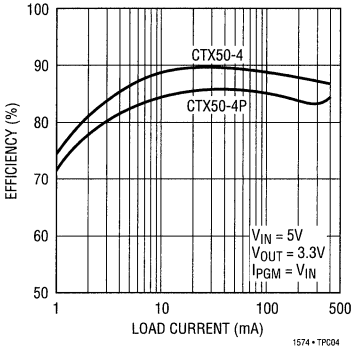
Efficiency vs Load Current



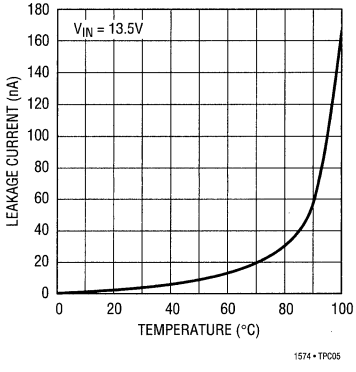
Efficiency vs Input Voltage



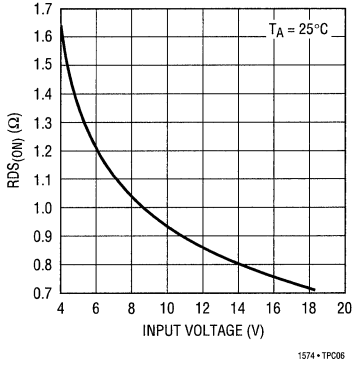
Efficiency Using Different Types of Inductor Core Material



Switch Leakage Current vs Temperature



Switch Resistance vs Input Voltage



PIN FUNCTIONS

NC (Pins 1, 8, 9, 16): No Connection.

GND (Pins 2, 4, 13, 15): Ground.

SW (Pins 3, 14): Drain of P-Channel MOSFET Switch and Cathode of Schottky Diode.

V_{IN} (Pin 5): Input Supply Voltage. It must be decoupled close to ground (Pin 4).

I_{PGM} (Pin 6): This pin selects the current limit of the P-channel switch. With $I_{PGM} = V_{IN}$, the current trip point is 600mA and with I_{PGM} = 0V, the current trip point is reduced to 340mA.

$\overline{SHDN}$ (Pin 7): Pulling this pin to ground keeps the internal switch off and puts the LTC1574 in micropower shutdown.

V_{OUT} or V_{FB} (Pin 10): For the LTC1574, this pin connects to the main voltage comparator input. On the LTC1574-5 and LTC1574-3.3, this pin goes to an internal resistive divider which sets the output voltage.

LB_{OUT} (Pin 11): Open drain of an N-Channel Pull-Down. This pin will sink current when (Pin 12) LB_{IN} goes below 1.25V.

LB_{IN} (Pin 12): The (–) Input of the Low-Battery Voltage Comparator. The (+) input is connected to a reference voltage of 1.25V.

APPLICATIONS INFORMATION

Operating Frequency and Inductor

Since the LTC1574 utilizes a constant off-time architecture, its operating frequency is dependent on the value of V_{IN}. The frequency of operation can be expressed as:

$$f = \frac{1}{t_{OFF}}\left(\frac{V_{IN} - V_{OUT}}{V_{IN} + V_D}\right) \quad (Hz)$$

where t_{OFF} = 4µs and V_D is the voltage drop across the internal Schottky diode. Note that the operating frequency is a function of the input and output voltage.

Although the size of the inductor does not affect the frequency or inductor peak current, it does affect the ripple current. The peak-to-peak ripple current is given by:

$$I_{RIPPLE} = 4 \times 10^{-6}\left(\frac{V_{OUT} + V_D}{L}\right) \quad (A_{P-P})$$

By choosing a smaller inductor, a low ESR (Effective Series Resistance) output filter capacitor has to be used. Core loss will increase due to higher ripple current.

Short-Circuit Protection

The LTC1574 is protected from output short circuits by its internal current limit. Depending on the condition of the I_{PGM} pin, the limit is either set to 340mA or 600mA. In addition, the off-time of the switch is increased to allow the inductor current to decay far enough to prevent any current build-up (see Figure 1).

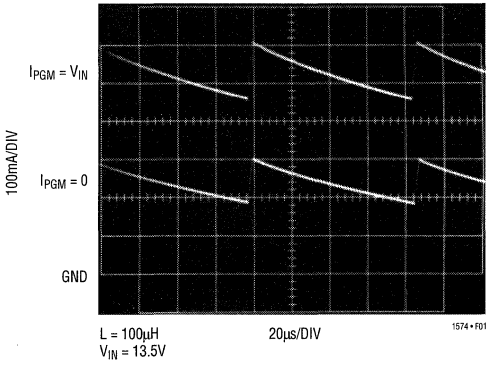


Figure 1. Inductor Current with Output Shorted

Low-Battery Detector

The low-battery indicator senses the input voltage through an external resistive divider. This divided voltage connects to the "–" input of a voltage comparator (Pin 12) which is compared with a 1.25V reference voltage. With the current

APPLICATIONS INFORMATION

going into Pin 12 being negligible, the following expression is used for setting the trip limit:

$$V_{LBTRIP} = 1.25\left(1+\frac{R4}{R3}\right)$$

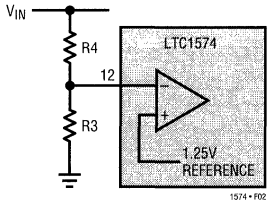


Figure 2. Low-Battery Comparator

LTC1574 Adjustable Applications

The LTC1574 develops a 1.25V reference voltage between the feedback terminal (Pin 10) and ground (see Figure 3). By selecting resistor R1, a constant current is caused to flow through R1 and R2 to set the overall output voltage. The regulated output voltage is determined by:

$$V_{OUT} = 1.25\left(1+\frac{R2}{R1}\right)$$

For most applications, a 30k resistor is suggested for R1. To prevent stray pickup, a 100pF capacitor is suggested across R1 located close to the LTC1574.

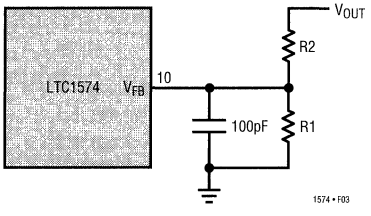


Figure 3. LTC1574 Adjustable Configuration

Inverting Applications

The LTC1574 can easily be set up for a negative output voltage. If –5V is desired, the LTC1574-5 is ideal for this application as it requires the least components. Figure 4 shows the schematic for this application. Note that the output voltage is now taken off the GND pins. Therefore, the maximum input voltage is now determined by the difference between the absolute maximum voltage rating and the output voltage. A maximum of 12V is specified in Figure 4, giving the circuit 1.5V of headroom for V_{IN}. Note that the circuit can operate from a minimum of 4V, making it ideal for a four NiCd cell application. For a higher output current circuit, please refer to the Typical Applications section.

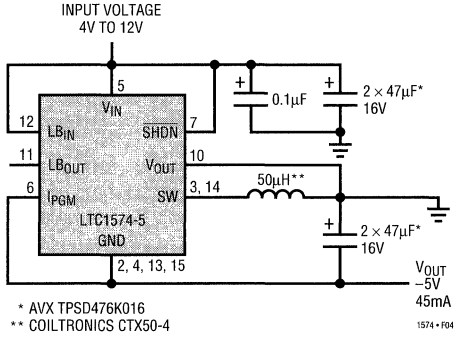


Figure 4. Positive-to-Negative 5V Converter

Low Noise Regulators

In some applications it is important not to introduce any switching noise within the audio frequency range. Due to the nature of the LTC1574 during Burst Mode™ operation, there is a possibility that the regulator will introduce audio noise at some load currents. To circumvent this problem, a feed-forward capacitor can be used to shift the noise spectrum up and out of the audio band. Figure 5 shows the low noise connection with C2 being the feed-forward capacitor. The peak-to-peak output ripple is reduced to 30mV over the entire load range. A toroidal surface mount

Burst Mode is a trademark of Linear Technology Corporation

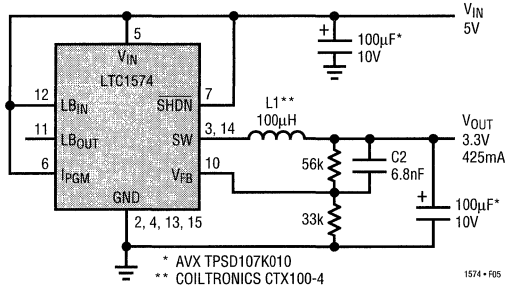


Figure 5. Low Noise 5V to 3.3V Regulator

APPLICATIONS INFORMATION

inductor L1 is chosen for its excellent self-shielding properties. Open magnetic structures such as drum and rod cores are to be avoided since they inject high flux levels into their surroundings. This can become a major source of noise in any converter circuit.

Design Example

As a design example, assume V_{IN} = 9V (nominal), V_{OUT} = 5V and I_{OUT} = 350mA maximum. The LTC1574-5 is used for this application with I_{PGM} (Pin 6) connected to V_{IN}. The minimum value of L is determined by assuming the LTC1574-5 is operating in continuous mode.

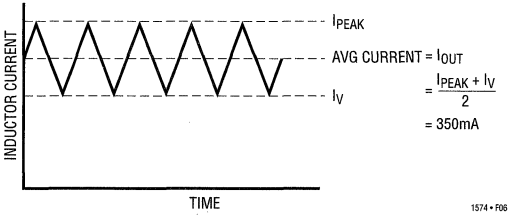


Figure 6. Continuous Inductor Current

With I_{OUT} = 350mA and I_{PEAK} = 0.6A (I_{PGM} = V_{IN}), I_V = 0.1A. The peak-to-peak ripple inductor current, I_{RIPPLE}, is 0.5A and is also equal to:

$$I_{RIPPLE} = 4 \times 10^{-6}\left(\frac{V_{OUT} + V_D}{L}\right) \quad (A_{P\text{-}P})$$

Solving for L in the above equation and with V_D = 0.5V, L = 44µH. The next higher standard value of L is 50µH (example: Coiltronics CTX50-4). The operating frequency, ignoring voltage across diode V_D is:

$$f \approx 2.5 \times 10^5\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$= 111kHz$$

With the value of L determined, the requirements for C_{IN} and C_{OUT} are calculated. For C_{IN}, its RMS current rating should be at least:

$$I_{RMS} = \frac{I_{OUT}\left[V_{OUT}\left(V_{IN} - V_{OUT}\right)\right]^{1/2}}{V_{IN}} \quad (A_{RMS})$$

$$= 174mA$$

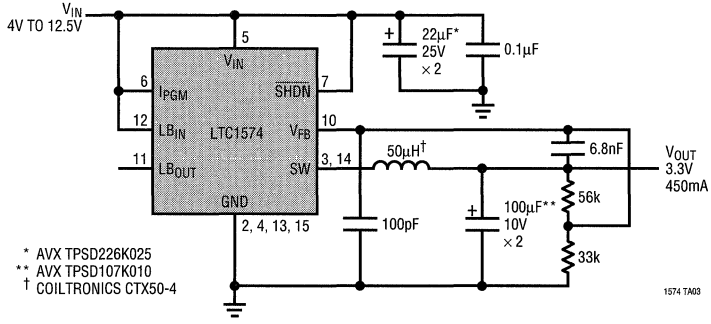
For C_{OUT}, the RMS current rating should be at least:

$$I_{RMS} \approx \frac{I_{PEAK}}{2} \quad (A_{RMS})$$

$$= 300mA$$

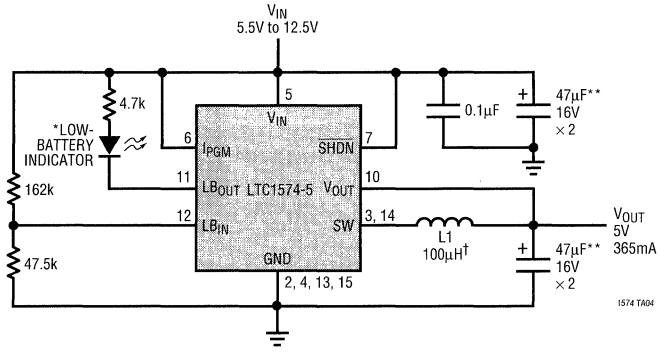
TYPICAL APPLICATIONS

Low Noise, High Efficiency 3.3V Regulator



TYPICAL APPLICATIONS

Low Dropout 5V Step-Down Regulator with Low-Battery Detection

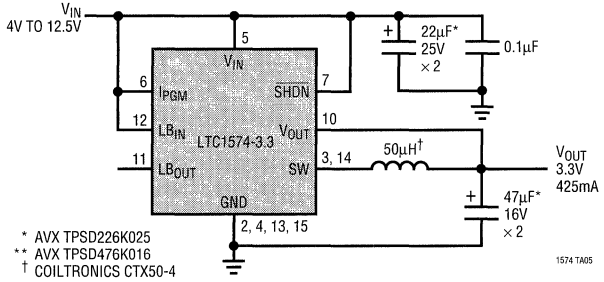


* LOW-BATTERY INDICATOR IS SET UP TO TRIP AT V_{IN} = 5.5V
** AVX TPSD476K016

† SELECTION

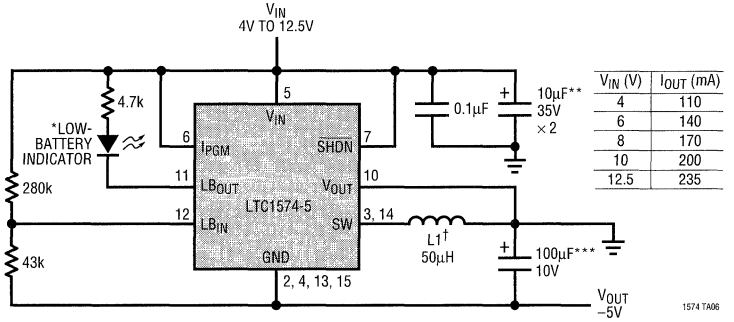
MANUFACTURER	PART NO.	TYPE
COILTRONICS	CTX100-4	SURFACE MOUNT
SUMIDA	CD75-101	SURFACE MOUNT
GOWANDA	GA10-103K	THROUGH HOLE

High Efficiency 3.3V Regulator



* AVX TPSD226K025
** AVX TPSD476K016
† COILTRONICS CTX50-4

Positive to –5V Converter



V_{IN} (V)	I_{OUT} (mA)
4	110
6	140
8	170
10	200
12.5	235

* LOW-BATTERY INDICATOR IS SET TO TRIP AT V_{IN} = 4.4V
** AVX TPSD106K035
*** AVX TPSD107K010

† SELECTION

MANUFACTURER	PART NO.	TYPE
COILTRONICS	CTX50-3	SURFACE MOUNT
COILCRAFT	DT3316-473	SURFACE MOUNT
SUMIDA	CD54-470	SURFACE MOUNT
GOWANDA	GA10-472K	THROUGH HOLE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1076	Step-Down Switching Regulator	2A Monolithic Bipolar Switcher for V_{IN} to 60V
LTC1174	High Efficiency Step-Down/Inverting DC/DC Converter	Same as LTC1574 Without Schottky Diode in SO-8 Package
LTC1265	1.2A, High Efficiency Step-Down DC/DC Converter	Current Mode with 0.3Ω Switch for Higher Current
LT1375/LT1376	1.5A, 500kHz Step-Down Switching Regulator	High Frequency, Synchronizable in SO-8 Package

SECTION 4—POWER PRODUCTS

Single PCMCIA VPP Driver/Regulator

FEATURES

- **Digital Selection of 0V, V_{CC}, 12V or Hi-Z**
- **120mA Output Current Capability**
- **Internal Current Limiting and Thermal Shutdown**
- Automatic Switching from 3.3V to 5V
- Powered from Unregulated 13V to 20V Supply
- Logic Compatible with Standard PCMCIA Controllers
- 1µF Output Capacitor
- 30µA Quiescent Current in Hi-Z or 0V Mode
- VPP Valid Status Feedback Signal
- No VPP Overshoot
- 8-Pin SO Packaging

APPLICATIONS

- Notebook Computers
- Palmtop Computers
- Pen-Based Computers
- Handi-Terminals
- Bar-Code Readers
- Flash Memory Programming

DESCRIPTION

The LT®1312 is a member of Linear Technology Corporation's family of PCMCIA drivers/regulators. The LT1312 provides 0V, 3.3V, 5V, 12V and Hi-Z regulated power to the VPP pin of a PCMCIA card slot from a single unregulated 13V to 20V supply. When used in conjunction with a PC card interface controller, the LT1312 forms a complete minimum component-count interface for palmtop, pen-based and notebook computers. The VPP output voltage is selected by two logic compatible digital inputs which interface directly with industry standard PC card interface controllers.

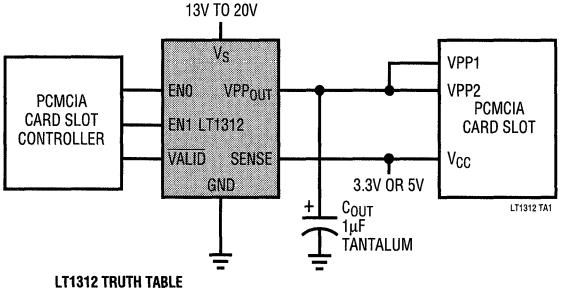
Automatic 3.3V to 5V switching is provided by an internal comparator which continuously monitors the PC card V_{CC} supply and automatically adjusts the regulated VPP output to match V_{CC} when the VPP = V_{CC} mode is selected.

An open-collector VPP $\overline{\text{VALID}}$ output is driven low when VPP is in regulation at 12V.

The LT1312 is available in an 8-pin SO package.

TYPICAL APPLICATION

Typical PCMCIA Single Slot VPP Driver



LT1312 TRUTH TABLE

EN0	EN1	SENSE	VPP_{OUT}	$\overline{\text{VALID}}$
0	0	X	0V	1
1	0	X	12V	0
0	1	3.0V TO 3.6V	3.3V	1
0	1	4.5V TO 5.5V	5V	1
1	1	X	Hi-Z	1

X = DON'T CARE

Linear Technology PCMCIA Product Family

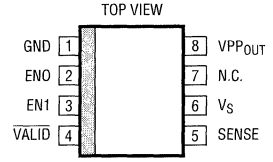
DEVICE	DESCRIPTION	PACKAGE
LT1312	SINGLE PCMCIA VPP DRIVER/REGULATOR	8-PIN SO
LT1313	DUAL PCMCIA VPP DRIVER/REGULATOR	16-PIN SO*
LTC®1314	SINGLE PCMCIA SWITCH MATRIX	14-PIN SO
LTC1315	DUAL PCMCIA SWITCH MATRIX	24-PIN SSOP
LTC1470	PROTECTED V_{CC} 5V/3.3V SWITCH MATRIX	8-PIN SO
LTC1472	PROTECTED V_{CC} AND VPP SWITCH MATRIX	16-PIN SO*

*NARROW BODY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 22V
Digital Input Voltage ..... 7V to (GND – 0.3V)
Sense Input Voltage ..... 7V to (GND – 0.3V)
Valid Output Voltage ..... 15V to (GND – 0.3V)
Output Short-Circuit Duration ..... Indefinite
Operating Temperature ..... 0°C to 70°C
Junction Temperature ..... 0°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1312CS8
S8 PART MARKING
1312

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = 13V to 20V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{PPOUT}	Output Voltage	Program to 12V, $I_{OUT} \leq 120mA$ (Note 1)	●	11.52	12.00	12.48	V
		Program to 5V, $I_{OUT} \leq 30mA$ (Note 1)	●	4.75	5.00	5.25	V
		Program to 3.3V, $I_{OUT} \leq 30mA$ (Note 1)	●	3.135	3.30	3.465	V
		Program to 0V, $I_{OUT} = -300\mu A$			0.42	0.60	V
I_{LKG}	Output Leakage	Program to Hi-Z, $0V \leq V_{PPOUT} \leq 12V$	●	–10		10	µA
I_S	Supply Current	Program to 0V	●		30	50	µA
		Program to Hi-Z	●		30	50	µA
		Program to 12V, No Load	●		230	360	µA
		Program to 5V, No Load	●		75	120	µA
		Program to 3.3V, No Load	●		55	90	µA
		Program to 12V, I_{OUT} = 120mA	●		126	132	mA
		Program to 5V, I_{OUT} = 30mA	●		31	33	mA
		Program to 3.3V, I_{OUT} = 30mA	●		31	33	mA
I_{LIM}	Current Limit	Program to 3.3V, 5V or 12V			330	500	mA
V_{ENH}	Enable Input High Voltage		●	2.4			V
V_{ENL}	Enable Input Low Voltage		●			0.4	V
I_{ENH}	Enable Input High Current	$2.4V \leq V_{IN} \leq 5.5V$			20	50	µA
I_{ENL}	Enable Input Low Current	$0V \leq V_{IN} \leq 0.4V$			0.01	1	µA
V_{SEN5}	V_{CC} Sense Threshold	V_{PPOUT} = 3.3V to 5V	●	3.60	4.05	4.50	V
V_{SEN3}	V_{CC} Sense Threshold	V_{PPOUT} = 5V to 3.3V	●	3.60	4.00	4.50	V
I_{SEN}	V_{CC} Sense Input Current	V_{SENSE} = 5V			38	60	µA
		V_{SENSE} = 3.3V			18	30	µA
$V_{VALID\ TH}$	V_{PP} $\overline{VALID}$ Threshold Voltage	Program to 12V	●	10.5	11	11.5	V
$V_{\overline{VALID}}$	V_{PP} $\overline{VALID}$ Output Drive Current	Program to 12V, $V_{\overline{VALID}}$ = 0.4V		1	3.3		mA
	V_{PP} $\overline{VALID}$ Output Leakage Current	Program to 0V, $V_{\overline{VALID}}$ = 12V			0.1	10	µA

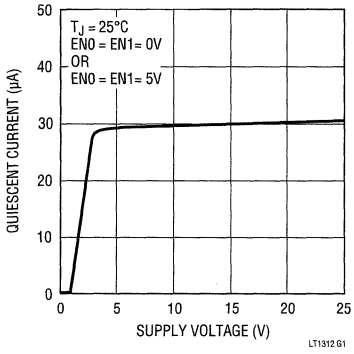
The ● denotes the specifications which apply over the full operating temperature range.

Note 1: For junction temperatures greater than 110°C, a minimum load of 1mA is recommended.

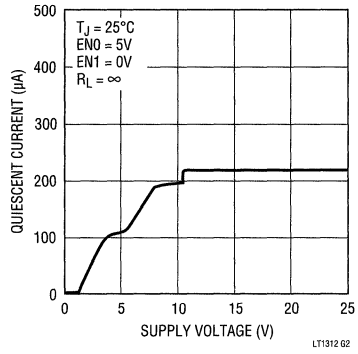
4

TYPICAL PERFORMANCE CHARACTERISTICS

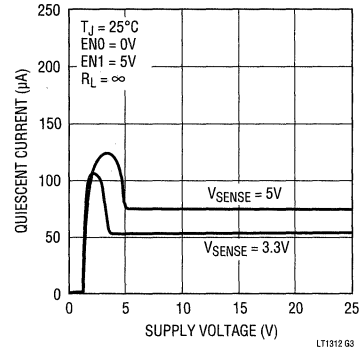
Quiescent Current (0V or Hi-Z Mode)



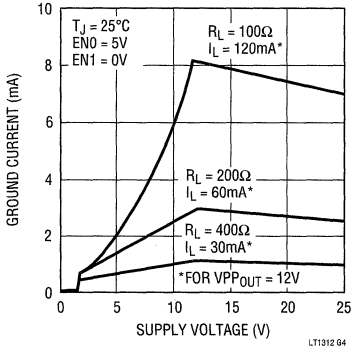
Quiescent Current (12V Mode)



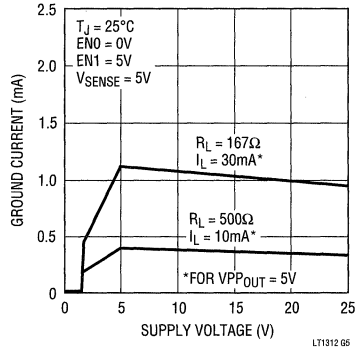
Quiescent Current (3.3V/5V Mode)



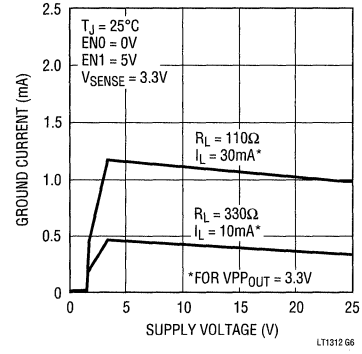
Ground Pin Current (12V Mode)



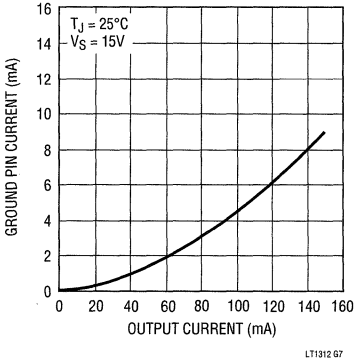
Ground Pin Current (5V Mode)



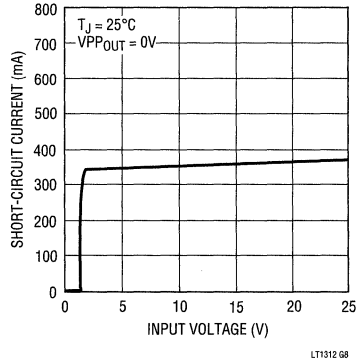
Ground Pin Current (3.3V Mode)



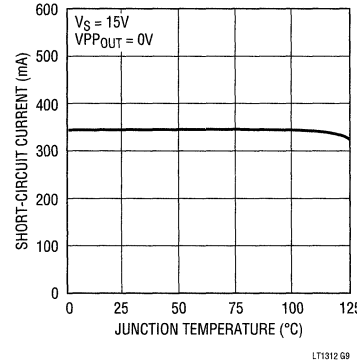
Ground Pin Current



Current Limit

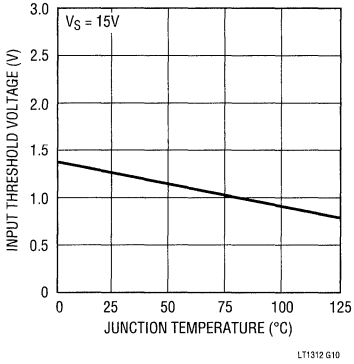


Current Limit

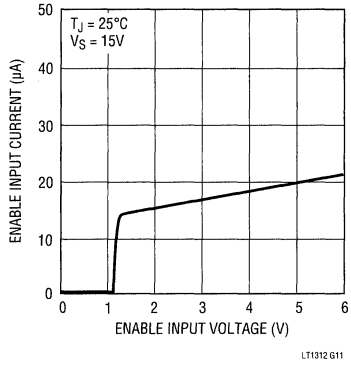


TYPICAL PERFORMANCE CHARACTERISTICS

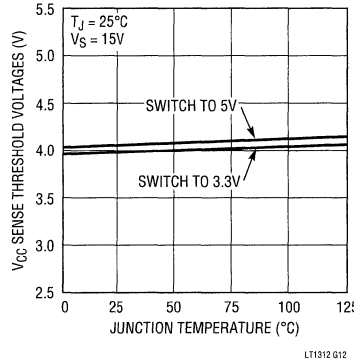
Enable Input Threshold Voltage



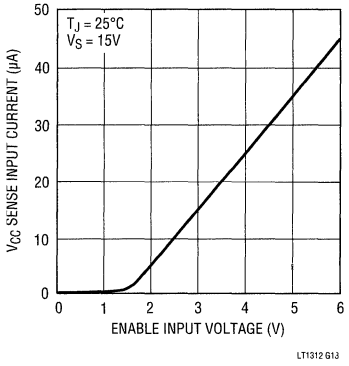
Enable Input Current



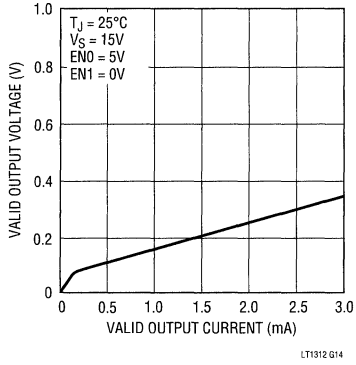
V_{CC} Sense Threshold Voltage



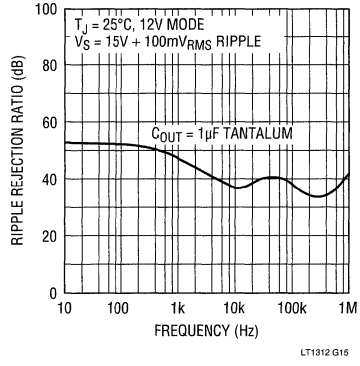
V_{CC} Sense Input Current



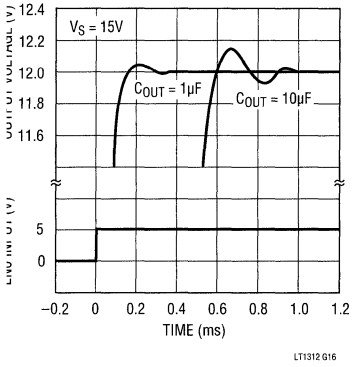
$\overline{VALID}$ Output Voltage



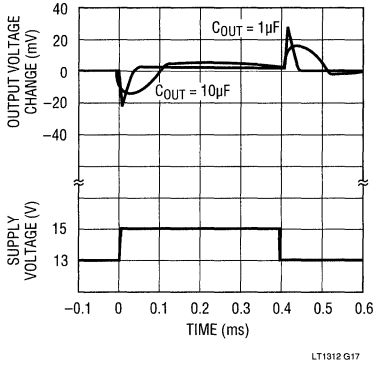
Ripple Rejection (12V)



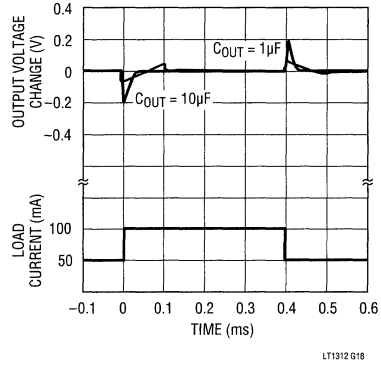
12V Turn-On Waveform



Line Transient Response (12V)



Load Transient Response (12V)



PIN FUNCTIONS

Supply Pin: Power is supplied to the device through the supply pin. The supply pin should be bypassed to ground if the device is more than 6 inches away from the main supply capacitor. A bypass capacitor in the range of 0.1µF to 1µF is sufficient. The supply voltage to the LT1312 can be loosely regulated between 13V and 20V. See Applications Information section for more detail.

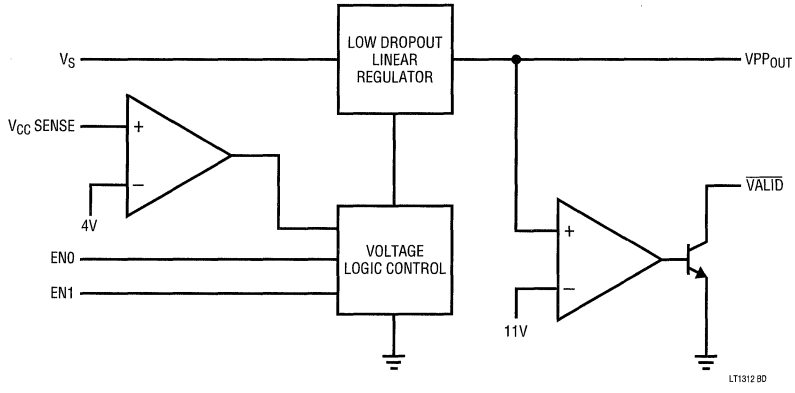
VPP_{OUT} Pin: This regulated output supplies power to the PCMCIA card VPP pins which are typically tied together at the card socket. The VPP_{OUT} output is current limited to approximately 330mA. Thermal shutdown provides a second level of protection. A 1µF to 10µF tantalum output capacitor is recommended. See Applications Information section for more detail on output capacitor considerations.

Input Enable Pins: The two digital input pins are high impedance inputs with approximately 20µA input current at 2.4V. The input thresholds are compatible with CMOS controllers and can be driven from either 5V or 3.3V CMOS logic. ESD protection diodes limit input excursions to 0.6V below ground.

$\overline{VALID}$ Output Pin: This pin is an open-collector NPN output which is driven low when the VPP_{OUT} pin is in regulation, i.e., when it is above 11V. An external 51k pull-up resistor is connected between this output and the same 5V or 3.3V logic supply powering the PCMCIA compatible control logic.

V_{CC} Sense Pin: A built-in comparator and 4V reference automatically switches the VPP_{OUT} from 5V to 3.3V depending upon the voltage sensed at the PCMCIA card socket V_{CC} pin. The input current for this pin is approximately 30µA. For 5V only operation, connect the Sense pin directly to ground. An ESD protection diode limits the input voltage to 0.6V below ground.

BLOCK DIAGRAM



OPERATION

The LT1312 is a programmable output voltage, low-dropout linear regulator designed specifically for PCMCIA VPP drive applications. Input power is typically obtained from a loosely regulated input supply between 13V and 20V (see Applications Information section for more detail on the input power supply). The LT1312 consists of the following blocks:

Low Dropout Voltage Linear Regulator: The heart of the LT1312 is a PNP-based low-dropout voltage regulator which drops the unregulated supply voltage from 13V to 20V down to 12V, 5V, 3.3V, 0V or Hi-Z depending upon the state of the two Enable inputs and the V_{CC} Sense input. The regulator has built-in current limiting and thermal shutdown to protect the device, the load, and the socket against inadvertent short circuiting to ground.

Voltage Control Logic: The LT1312 has five possible output modes: 0V, 3.3V, 5V, 12V and Hi-Z. These five modes are selected by the two Enable inputs and the V_{CC} Sense input as described by the Truth Table.

V_{CC} Sense Comparator: When the V_{CC} mode is selected, the LT1312 automatically adjusts the regulated VPP output voltage to 3.3V or 5V depending upon the voltage present at the PC card V_{CC} supply pin. The threshold voltage for the comparator is set at 4V and there is approximately 50mV of hysteresis provided to ensure clean switching between 3.3V and 5V.

VPP $\overline{\text{VALID}}$ Comparator: A voltage comparator monitors the output voltage when the 12V mode is selected and is driven low when the output is in regulation above 11V.

APPLICATIONS INFORMATION

The LT1312 is a voltage programmable linear regulator designed specifically for PCMCIA VPP driver applications. The device operates with very low quiescent current (30µA) in the 0V and Hi-Z modes of operation. In the Hi-Z mode, the output leakage current falls to 1µA. Unloaded quiescent current rises to only 55µA and 75µA when programmed to 3.3V and 5V respectively. In addition to the low quiescent currents, the LT1312 incorporates several protection features which make it ideal for PCMCIA applications. The LT1312 has built-in current limiting (330mA) and thermal shutdown to protect the device and the socket VPP pins against inadvertent short-circuit conditions.

AUXILIARY WINDING POWER SUPPLIES

Because the LT1312 provides excellent output regulation, the input power supply may be loosely regulated. One convenient (and economic) source of power is an auxiliary winding on the main 5V switching regulator inductor in the main system power supply.

LTC®1142HV Auxiliary Winding Power Supply

Figure 1 is a schematic diagram which describes how a loosely regulated 14V power supply is created by adding an auxiliary winding to the 5V inductor in a split 3.3V/5V LTC1142HV power supply system. A turns ratio of 1:1.8 is used for transformer T1 to ensure that the input voltage to the LT1312 falls between 13V and 20V under all load conditions. The 9V output from this additional winding is rectified by diode D2, added to the main 5V output and applied to the input of the LT1312. (Note that the auxiliary winding must be phased properly as shown in Figure 1.)

The auxiliary winding is referenced to the 5V output which provides DC current feedback from the auxiliary supply to the main 5V section. The AC transient response is improved by returning the negative lead of C5 to the 5V output as shown.

When the 12V output is activated by a TTL high on the Enable line, the 5V section of the LTC1142HV is forced into continuous mode operation. A resistor divider composed of R2, R3 and switch Q3 forces an offset which is subtracted from the internal offset at the Sense⁻ input (pin 14) of the LTC1142HV. When this external offset cancels the built-in 25mV offset, Burst Mode™ operation is inhibited and the LTC1142HV is forced into continuous mode operation. (See the LTC1142HV data sheet for further detail). In this mode, the 14V auxiliary supply can be

Burst Mode is a trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

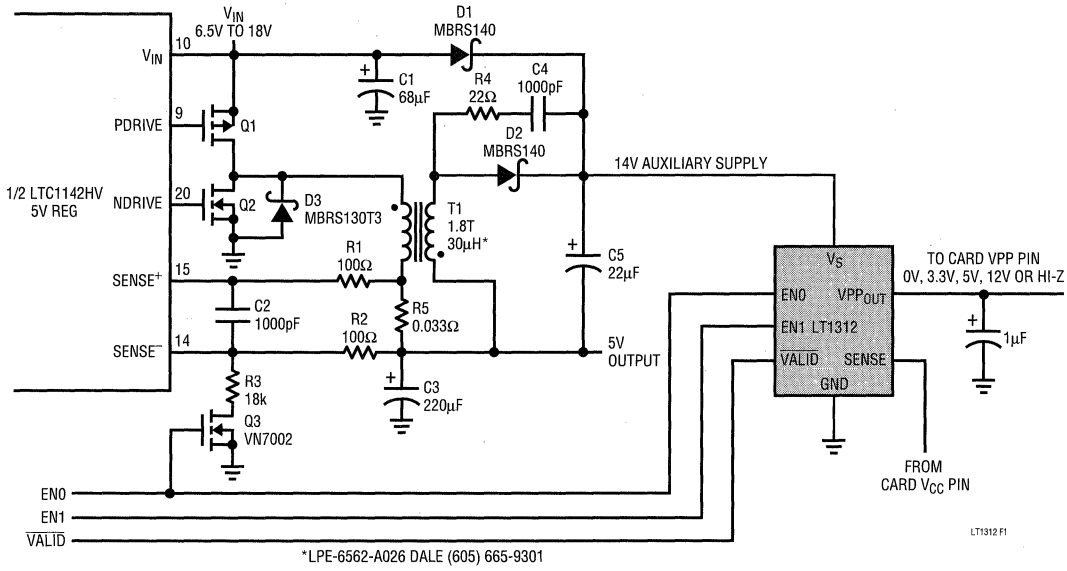


Figure 1. Deriving 14V Power from an Auxiliary Winding on the LTC1142HV 5V Regulator

loaded without regard to the loading on the 5V output of the LTC1142HV.

Continuous mode operation is only invoked when the LT1312 is programmed to 12V. If the LT1312 is programmed to 0V, 3.3V or 5V, power is obtained directly from the main power source (battery pack) through diode D1. Again, the LT1312 output can be loaded without regard to the loading of the main 5V output.

R4 and C4 absorb transient voltage spikes associated with the leakage inductance inherent in T1's secondary winding and ensure that the auxiliary supply does not exceed 20V.

Figure 2 is a graph of output voltage versus output current for the auxiliary 14V supply shown in Figure 1. Note that the auxiliary supply voltage is slightly higher when the 5V output is heavily loaded. This is due to the increased energy flowing through the main 5V inductor.

LTC1142 Auxiliary Power from the 3.3V Output

The circuit of Figure 1 can be modified for operation with low-battery count applications (6 cell). As the input voltage falls, the 5V duty cycle increases to the point where there is simply not enough time to transfer energy from the 5V primary to the auxiliary winding. For applications where heavy 12V load currents exist in conjunction with low input voltages (<6.5V), the auxiliary winding can be derived from the 3.3V section instead of the 5V section of the LTC1142. In this case, a transformer with a turns ratio of 1:3.4 to 1:3.6 should be used in place of the 3.3V section

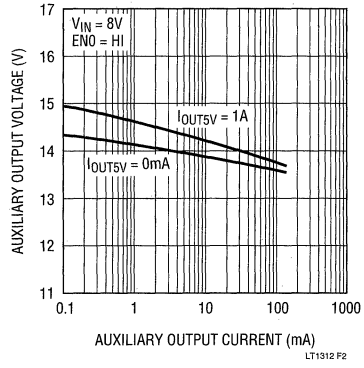


Figure 2. LTC1142 Auxiliary Supply Voltage

ıPPLICATIONS INFORMATION

ıductor as shown in Figure 3. MOSFET Q4 and diode D4 ave been added and diode D1 is no longer used. In the revious circuit, power is drawn directly from the batteries ırough D1, when the LTC1142 is in Burst Mode operation nd the VPP pin requires 3.3V or 5V. For these lower input oltages this technique is no longer valid as the input will ıll below the LT1312 regulator's dropout voltage. To orrect for this situation, the additional switch Q4 forces ıe switching regulator into continuous mode operation /henever 3.3V, 5V or 12V is selected.

INE POWERED SUPPLIES

ı line operated products such as: desktop computers, edicated PC card readers/writers, medical equipment, ɜst and measurement equipment, etc., it is possible to erive power from a relatively "raw" source such as a 5V r 12V power supply. The 12V supply line in a desktop omputer however, is usually too "dirty" to apply directly ɔ the VPP pins of a PCMCIA card socket. Power supply witching and load transients may create voltage spikes on this line that may damage sensitive PCMCIA flash memory cards if applied directly to the VPP pins.

Flash Memory Card VPP Power Considerations

PCMCIA compatible flash memory cards require tight regulation of the 12V VPP programming supply to ensure that the internal flash memory circuits are never subjected to damaging conditions. Flash memory circuits are typically rated with an absolute maximum of 13.5V and VPP must be maintained at 12V ±5% under all possible load conditions during erase and program cycles. Undervoltage can decrease specified flash memory reliability and overvoltage can damage the device[1].

Generating 14V from 5V or 12V

It is important that the 12V VPP supply for the two VPP lines to the card be free of voltage spikes. There should be little or no overshoot during transitions to and from the 12V level.

[1]See Application Note AP-357, "Power Supply Solutions for Flash Memory," Intel Corporation, 1992.

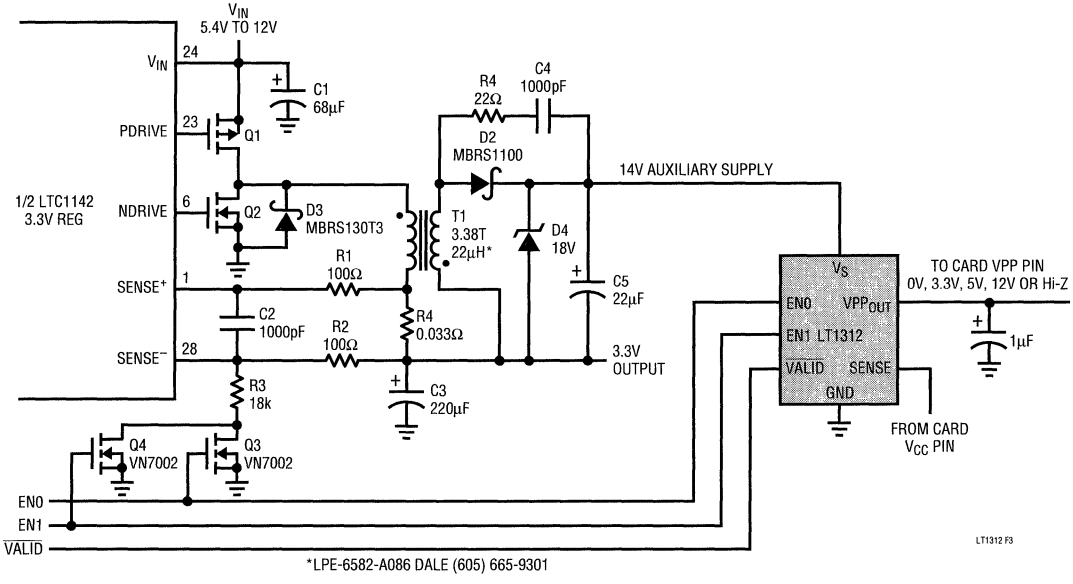


Figure 3. Deriving Auxiliary 14V Power from an LTC1142 3.3V Regulator

APPLICATIONS INFORMATION

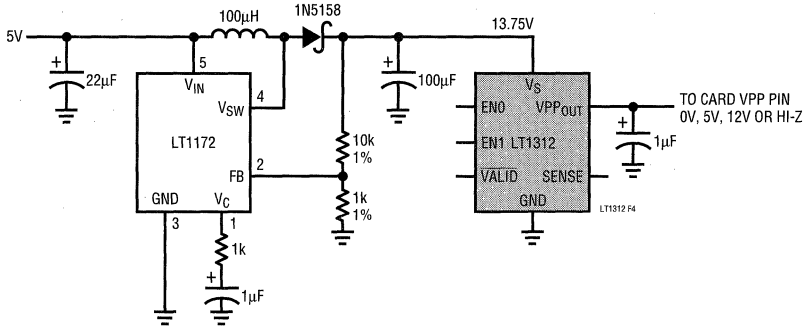


Figure 4. Local 5V to 15V Boost Regulator for Line Operated Applications

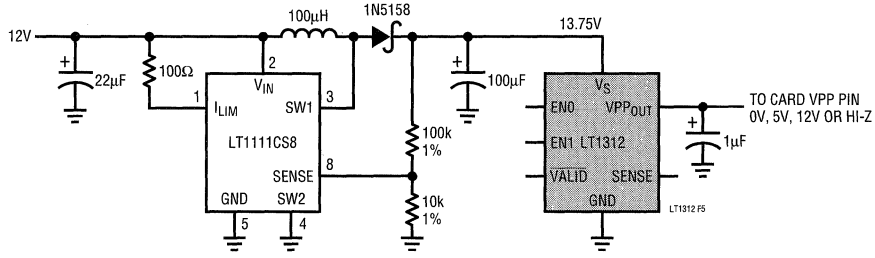


Figure 5. Local 12V to 15V Boost Regulator for Line Operated Applications

This is easily accomplished by generating a local 14V supply from a relatively "dirty" 5V or 12V supply as shown in Figures 4 and 5. Precise voltage control (and further filtering) is provided by the LT1312 driver/regulator. A further advantage to this scheme is that it adds current limit in series with the VPP pins to eliminate possible damage to the card socket, the PC card, or the switching power supply in the event of an accidental short circuit.

Output Capacitance

The LT1312 is designed to be stable with a wide range of output capacitors. The minimum recommended value is a 1µF with an ESR of 3Ω or less. The capacitor is connected directly between the output pin and ground as shown in Figure 6.

For applications where space is very limited, capacitors as low as 0.33µF can be used. Extremely low ESR ceramic capacitors with values less than 1µF must have a 2Ω resistor added in series with the output capacitor as shown in shown in Figure 7.

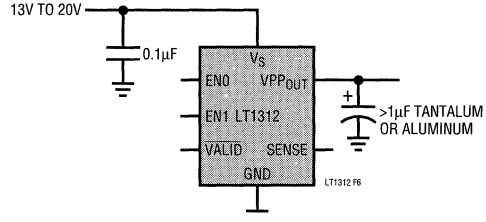


Figure 6. Recommended >1µF Tantalum Output Capacitor

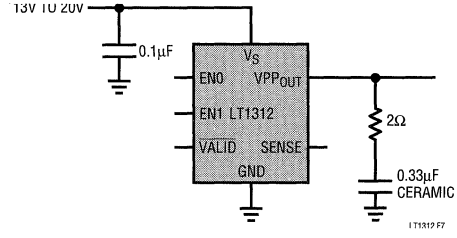


Figure 7. Using a 0.33µF to 1µF Output Capacitor

APPLICATIONS INFORMATION

Transient and Switching Performance

The LT1312 is designed to produce minimal overshoot with capacitors in the range of 1µF to 10µF. Larger capacitor values can be used with a slowing of rise and fall times.

The positive output slew rate is determined by the 330mA current limit and the output capacitor. The rise time for a 0V to 12V transition is approximately 40µs, the rise time for a 10µF capacitor is roughly 400µs (see the Transient Response curves in the Typical Performance Characteristics section).

The fall time from 12V to 0V is set by the output capacitor and an internal pull-down current source which sinks about 30mA. This source will fully discharge a 1µF capacitor in less than 1ms.

Thermal Considerations

Power dissipated by the device is the sum of two components: output current multiplied by the input-output differential voltage $I_{OUT} \times (V_{IN} - V_{OUT})$, and ground pin current multiplied by supply voltage $I_{GND} \times V_{IN}$.

The ground pin current can be found by examining the Ground Pin Current curves in the Typical Performance Characteristics section.

Heat sinking, for surface mounted devices, is accomplished by using the heat spreading capabilities of the PC board and its copper traces.

The junction temperature of the LT1312 must be limited to 25°C to ensure proper operation. Use Table 1 in conjunction with the typical performance graphs, to calculate the power dissipation and die temperature for a particular application and ensure that the die temperature does not exceed 125°C under any operating conditions.

Table 1. S8 Package*

COPPER AREA TOPSIDE	COPPER AREA BACKSIDE	BOARD AREA	THERMAL RESISTANCE (JUNCTION-TO-AMBIENT)
2500 sq mm	2500 sq mm	2500 sq mm	120°C/W
1000 sq mm	2500 sq mm	2500 sq mm	120°C/W
225 sq mm	2500 sq mm	2500 sq mm	125°C/W
1000 sq mm	1000 sq mm	1000 sq mm	131°C/W

*Device is mounted topside.

Calculating Junction Temperature

Example: given an output voltage of 12V, an input supply voltage of 14V, an output current of 100mA, and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

Power dissipated by the device will be equal to:

$$I_{OUT} \times (V_S - VPP_{OUT}) + (I_{GND} \times V_{IN})$$

where:

I_{OUT} = 100mA

V_{IN} = 14V

I_{GND} at (I_{OUT} = 100mA, V_{IN} = 14V) = 5mA

so,

$$P_D = 100mA \times (14V - 12V) + (5mA \times 15V) = 0.275W$$

Using Table 1, the thermal resistance will be in the range of 120°C/W to 131°C/W depending upon the copper area. So the junction temperature rise above ambient will be less than or equal to:

$$0.275W \times 131°C/W = 36°C$$

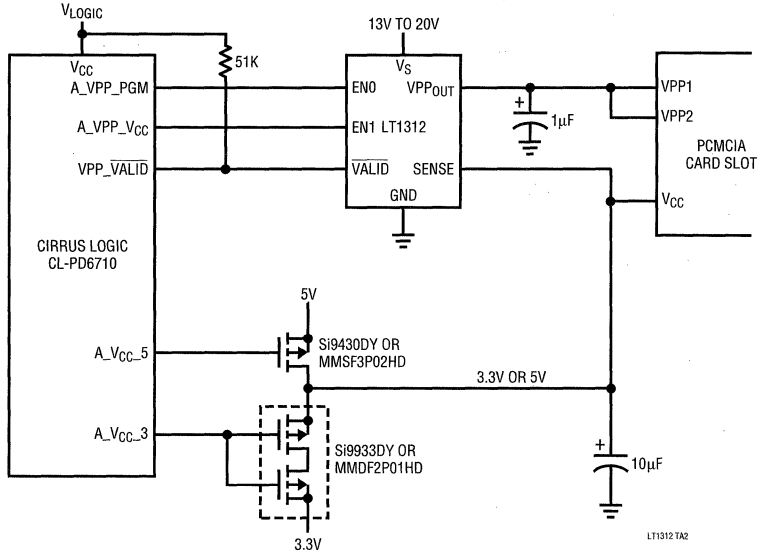
The maximum junction temperature will then be equal to the junction temperature rise above ambient plus the maximum ambient temperature or:

$$T_{JMAX} = 50°C + 36°C = 86°C.$$

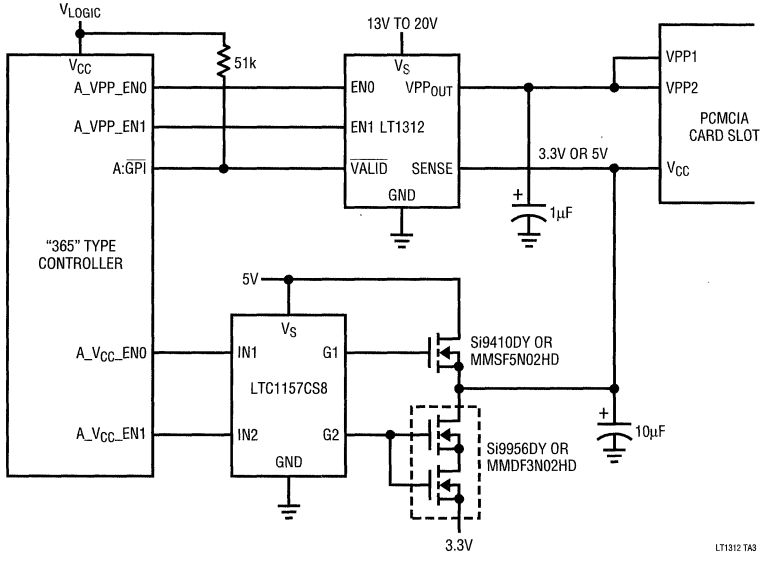
4

TYPICAL APPLICATIONS

Single Slot Interface to CL-PD6710



Single Slot Interface to "365" Type Controller



RELATED PARTS

See PCMCIA Product Family table on the first page of this data sheet.

Dual PCMCIA VPP Driver/Regulator

FEATURES

- **Digital Selection of 0V, V_{CC}, 12V or Hi-Z**
- **Output Current Capability: 120mA**
- **Internal Current Limiting and Thermal Shutdown**
- Automatic Switching from 3.3V to 5V
- Powered from Unregulated 13V to 20V Supply
- Logic Compatible with Standard PCMCIA Controllers
- Output Capacitors: 1µF
- Quiescent Current in Hi-Z or 0V Mode: 60µA
- Independent VPP Valid Status Feedback Signals
- No VPP Overshoot

APPLICATIONS

- Notebook Computers
- Palmtop Computers
- Pen-Based Computers
- Handi-Terminals
- Bar-Code Readers
- Flash Memory Programming

DESCRIPTION

The LT®1313 is a member of Linear Technology Corporation's PCMCIA driver/regulator family. It provides 0V, 3.3V, 5V, 12V and Hi-Z regulated power to the VPP pins of two PCMCIA card slots from a single unregulated 13V to 20V supply. When used in conjunction with a PC Card Interface Controller, the LT1313 forms a complete minimum component-count interface for palmtop, pen-based and notebook computers. The two VPP output voltages are independently selected by four logic compatible digital inputs which interface directly with industry standard PC Card Interface Controllers.

Automatic 3.3V to 5V switching is provided by two independent comparators which continuously monitor each PC card V_{CC} supply voltage and automatically adjust the VPP output to match the associated V_{CC} pin voltage when the VPP = V_{CC} mode is selected.

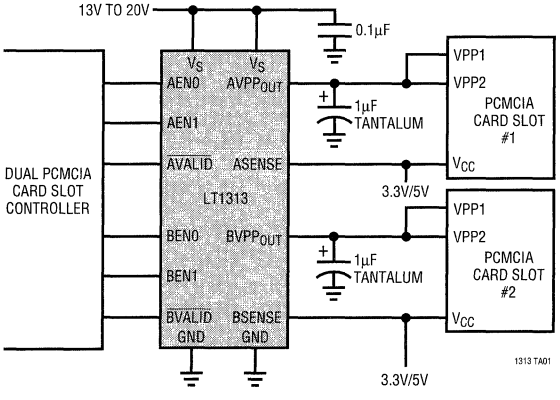
Two open-collector VPP $\overline{\text{VALID}}$ outputs are provided to indicate when the VPP outputs are in regulation at 12V.

The LT1313 is available in 16-pin SO packaging.

4

TYPICAL APPLICATION

Typical PCMCIA Dual Slot VPP Driver



Linear Technology PCMCIA Product Family

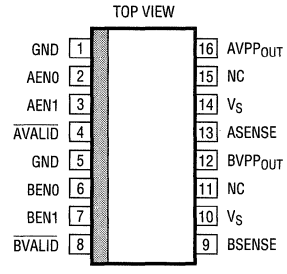
DEVICE	DESCRIPTION	PACKAGE
LT1312	SINGLE PCMCIA VPP DRIVER/REGULATOR	8-PIN SO
LT1313	DUAL PCMCIA VPP DRIVER/REGULATOR	16-PIN SO*
LTC®1314	SINGLE PCMCIA SWITCH MATRIX	14-PIN SO
LTC1315	DUAL PCMCIA SWITCH MATRIX	24-PIN SSOP
LTC1470	PROTECTED V_{CC} 5V/3.3V SWITCH MATRIX	8-PIN SO
LTC1472	PROTECTED V_{CC} AND VPP SWITCH MATRIX	16-PIN SO*

*NARROW BODY

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 22V
Digital Input Voltage ..... 7V to (GND – 0.3V)
Sense Input Voltage ..... 7V to (GND – 0.3V)
$\overline{\text{VALID}}$ Output Voltage ..... 15V to (GND – 0.3V)
Output Short-Circuit Duration ..... Indefinite
Operating Temperature ..... 0°C to 70°C
Junction Temperature ..... 0°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO
T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1313CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_S = 13V to 20V, T_A = 25°C (Note 1), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VPP_{OUT}	Output Voltage	Program to 12V, $I_{OUT} \le 120mA$ (Note 2)	●	11.52	12.00	12.48	V
		Program to 5V, $I_{OUT} \le 30mA$ (Note 2)	●	4.75	5.00	5.25	V
		Program to 3.3V, $I_{OUT} \le 30mA$ (Note 2)	●	3.135	3.30	3.465	V
		Program to 0V, $I_{OUT} = -300\mu A$			0.42	0.60	V
I_{LKG}	Output Leakage	Program to Hi-Z, $0V \le VPP_{OUT} \le 12V$	●	–10		10	µA
I_S	Supply Current	Both Channels Programmed to 0V	●		60	100	µA
		Both Channels Programmed to Hi-Z	●		60	100	µA
		One Channel Programmed to 12V, No Load (Note 3)	●		260	400	µA
		One Channel Programmed to 5V, No Load (Note 3)	●		105	150	µA
		One Channel Programmed to 3.3V, No Load (Note 3)	●		85	120	µA
		One Channel Programmed to 12V, I_{OUT} = 120mA (Note 3)	●		126	132	mA
		One Channel Programmed to 5V, I_{OUT} = 30mA (Note 3)	●		31	33	mA
		One Channel Programmed to 3.3V, I_{OUT} = 30mA (Note 3)	●		31	33	mA
I_{LIM}	Current Limit	Program to 3.3V, 5V or 12V (Note 3)			330	500	mA
V_{ENH}	Enable Input High Voltage		●	2.4			V
V_{ENL}	Enable Input Low Voltage		●			0.4	V
I_{ENH}	Enable Input High Current	$2.4V \le V_{IN} \le 5.5V$			20	50	µA
I_{ENL}	Enable Input Low Current	$0V \le V_{IN} \le 0.4V$			0.01	1	µA
V_{SEN5}	V_{CC} Sense Threshold	VPP_{OUT} = 3.3V to 5V (Note 4)	●	3.60	4.05	4.50	V
V_{SEN3}	V_{CC} Sense Threshold	VPP_{OUT} = 5V to 3.3V (Note 4)	●	3.60	4.00	4.50	V
I_{SEN}	V_{CC} Sense Input Current	V_{SENSE} = 5V			38	60	µA
		V_{SENSE} = 3.3V			18	30	µA
$V_{VALID\ TH}$	VPP_{VALID} Threshold Voltage	Program to 12V, (Note 5)	●	10.5	11	11.5	V
$I_{\overline{VALID}}$	VPP_{VALID} Output Drive Current	Program to 12V, V_{VALID} = 0.4V, (Note 5)		1	3.3		mA
	VPP_{VALID} Output Leakage Current	Program to 0V, V_{VALID} = 12V, (Note 5)			0.1	10	µA

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: Both V_S pins (10, 14) must be connected together, and both ground pins (1, 5) must be connected together.

Note 2: For junction temperatures greater than 110°C, a minimum load of 1mA is recommended.

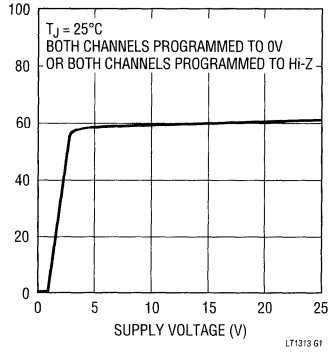
Note 3: The other channel is programmed to the 0V mode (XEN0 = XEN1 = 0V) during this test.

Note 4: The V_{CC} sense threshold voltage tests are performed independently.

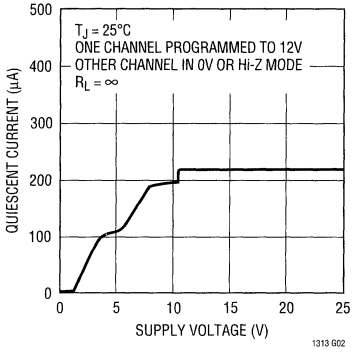
Note 5: The VPP_{VALID} tests are performed independently.

TYPICAL PERFORMANCE CHARACTERISTICS

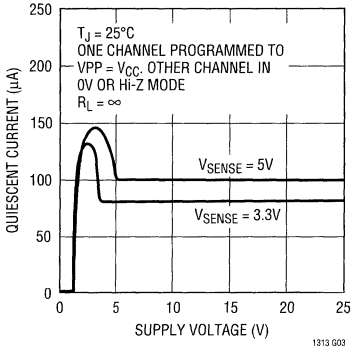
Quiescent Current (0V or Hi-Z Mode)



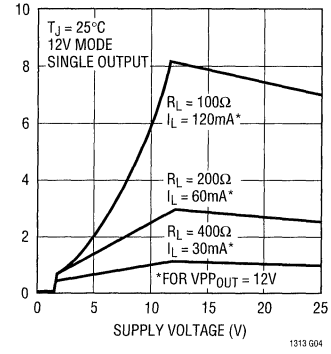
Quiescent Current (12V Mode)



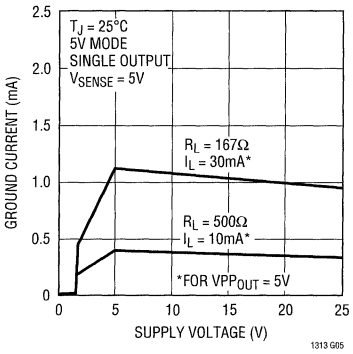
Quiescent Current (3.3V/5V Mode)



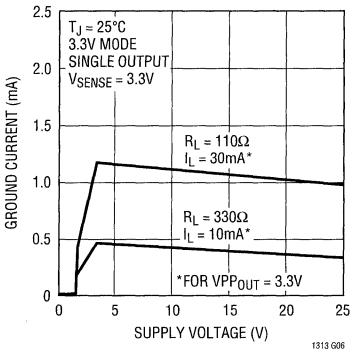
Ground Pin Current (12V Mode)



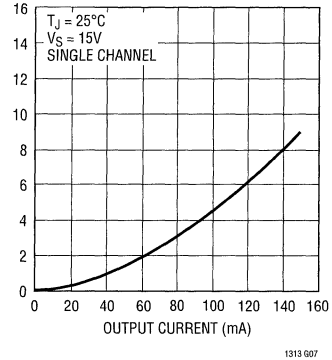
Ground Pin Current (5V Mode)



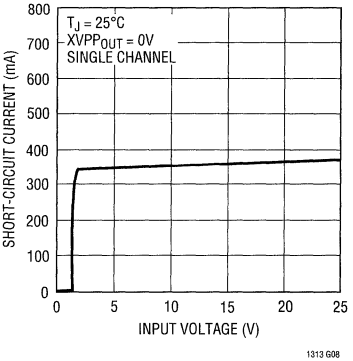
Ground Pin Current (3.3V Mode)



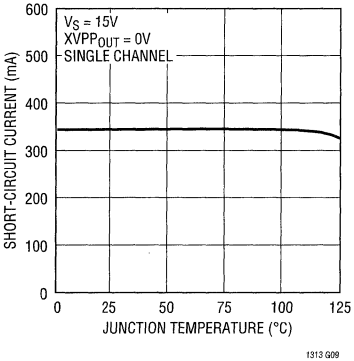
Ground Pin Current



Current Limit



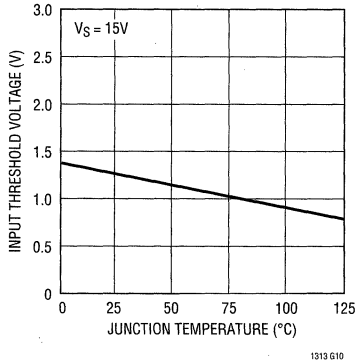
Current Limit



4

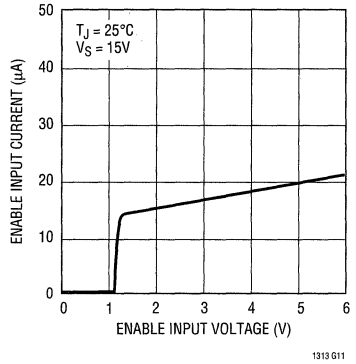
TYPICAL PERFORMANCE CHARACTERISTICS

Enable Input Threshold Voltage



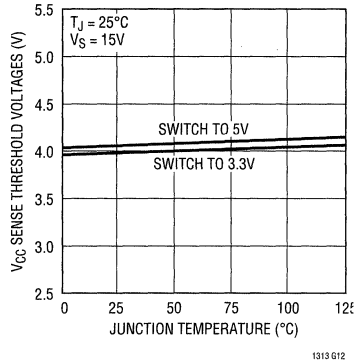
1313 G10

Enable Input Current



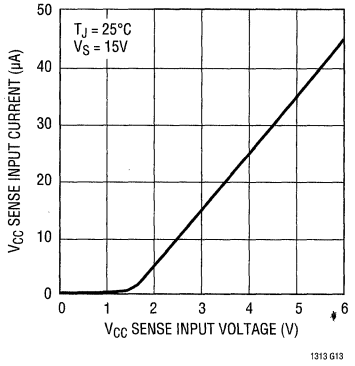
1313 G11

V_{CC} Sense Threshold Voltage



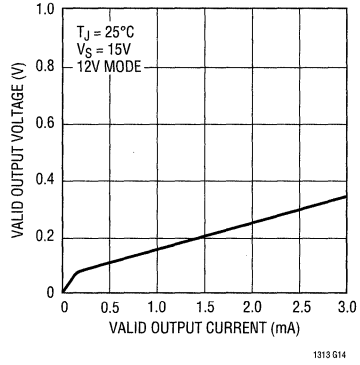
1313 G12

V_{CC} Sense Input Current



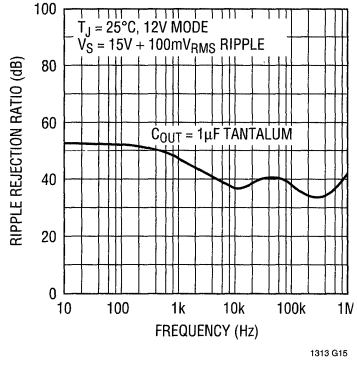
1313 G13

$\overline{\text{VALID}}$ Output Voltage



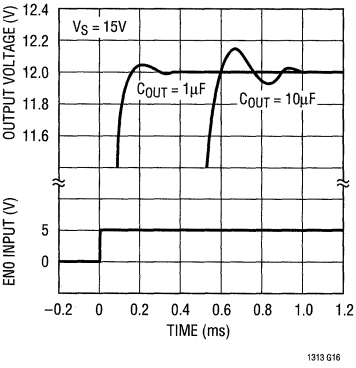
1313 G14

Ripple Rejection (12V)



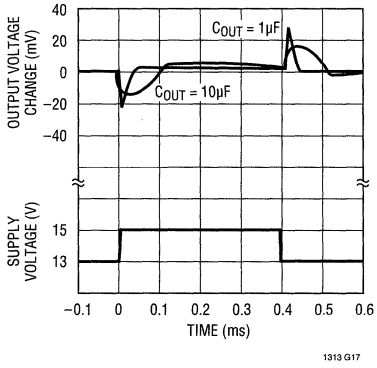
1313 G15

12V Turn-On Waveform



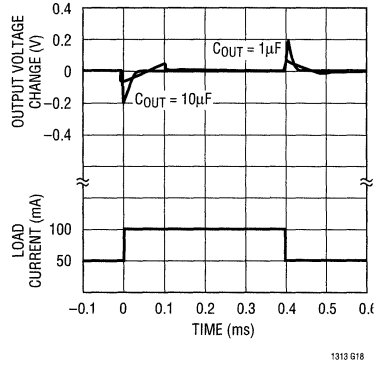
1313 G16

Line Transient Response (12V)



1313 G17

Load Transient Response (12V)



1313 G18

IN FUNCTIONS

ıpply Pins: Power is supplied to the device through the 'o supply pins *which must be connected together at all nes* . The supply pins should be bypassed to ground if e device is more than six inches away from the main ıpply capacitor. A bypass capacitor in the range of 0.1µF 1µF is sufficient. The supply voltage to the LT1313 can loosely regulated between 13V and 20V.

P_{OUT} Pins: Each regulated output supplies power to the 'o PCMCIA card VPP pins which are typically tied to- ther at the socket. Each VPP_{OUT} output is current limited approximately 330mA. Thermal shutdown provides a cond level of protection. A 1µF to 10µF tantalum output pacitor is recommended.

put Enable Pins: The four digital input pins are high ıpedance inputs with approximately 20µA input current 2.4V. The input thresholds are compatible with CMOS ıntrollers and can be driven from either 5V or 3.3V CMOS gic. ESD protection diodes limit input excursions to 0.6V low ground.

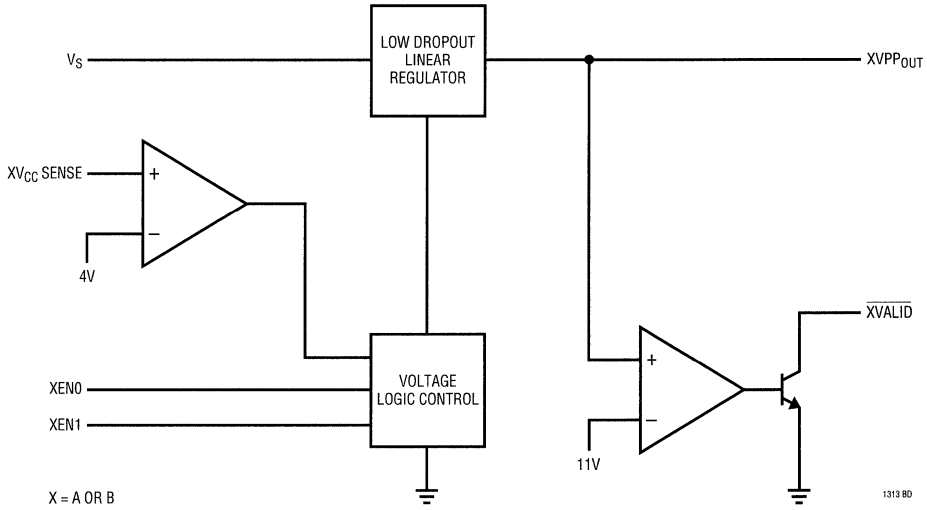
$\overline{VALID}$ Output Pins: These pins are open-collector NPN outputs which are driven low when the corresponding VPP_{OUT} pin is in regulation, i.e., when it is above 11V. Two external 51k pull-up resistors are connected between these outputs and the same 5V or 3.3V logic supply powering the PCMCIA compatible control logic.

V_{CC} Sense Pins: Two independent comparators and 4V references automatically switch the VPP_{OUT} outputs from 5V to 3.3V depending upon the voltage sensed at the corresponding PCMCIA card socket V_{CC} pin. The input current for these pins is approximately 30µA. For 5V only operation, connect the Sense pins directly to ground. An ESD protection diode limits the input voltage to 0.6V below ground.

Ground Pins: *The two ground pins must be connected together at all times.*

4

LOCK DIAGRAM (One Channel)



OPERATION

The LT1313 is two programmable output voltage, low-dropout linear regulators designed specifically for PCMCIA VPP drive applications. Input power is typically obtained from a loosely regulated input supply between 13V and 20V. The LT1313 consists of the following blocks:

Two Low Dropout Voltage Linear Regulators: The heart of the LT1313 is two PNP-based low-dropout voltage regulators which drop the unregulated supply voltage from 13V to 20V down to 12V, 5V, 3.3V, 0V or Hi-Z depending upon the state of the four Enable inputs and the two V_{CC} Sense inputs. The regulators have built-in current limiting and thermal shutdown to protect the device, the loads, and the sockets against inadvertent short circuiting to ground.

Voltage Control Logic: The two VPP_{OUT} outputs have five possible output modes: 0V, 3.3V, 5V, 12V and Hi-Z. These five modes are selected by the four Enable inputs and the two V_{CC} Sense inputs as described by the Truth Table.

V_{CC} Sense Comparators: When the V_{CC} mode is selected, the LT1313 automatically adjusts each regulated VPP output voltage to 3.3V or 5V depending upon the voltage present at the corresponding PC card V_{CC} supply pin. The thresh old voltage for these comparators is set at 4V and there i approximately 50mV of hysteresis provided to ensur clean switching between 3.3V and 5V.

VPP $\overline{\text{VALID}}$ Comparator: Two voltage comparators moni tor each output voltage when the 12V mode is selected an are driven low when the output is in regulation above 11V These two outputs function separately.

LT1313 Truth Table

AEN0	AEN1	ASENSE	$AVPP_{OUT}$	$\overline{\text{AVALID}}$
0	0	X	0V	1
1	0	X	12V	0
0	1	3.0V to 3.6V	3.3V	1
0	1	4.5V to 5.5V	5V	1
1	1	X	Hi-Z	1

X = Don't Care

BEN0	BEN1	BSENSE	$BVPP_{OUT}$	$\overline{\text{BVALID}}$
0	0	X	0V	1
1	0	X	12V	0
0	1	3.0V to 3.6V	3.3V	1
0	1	4.5V to 5.5V	5V	1
1	1	X	Hi-Z	1

Note: Each channel is independently controlled.

APPLICATIONS INFORMATION

The LT1313 is two voltage programmable linear regulators designed specifically for PCMCIA VPP driver applications. The device operates with very low quiescent current (60µA) in the 0V and Hi-Z modes of operation. In the Hi-Z mode, the output leakage current falls to 1µA. In addition to the low quiescent currents, the LT1313 incorporates several protection features which make it ideal for PCMCIA applications. The LT1313 has built-in current limiting (330mA) and thermal shutdown to protect the device and the socket VPP pins against inadvertent short-circuit conditions.

Output Capacitance

The LT1313 is designed to be stable with a wide range of output capacitors. The minimum recommended value is a 1µF with an ESR of 3Ω or less. The capacitor is connected directly between the output pin and ground. For applications where space is very limited, capacitors as low as 0.33µF can be used. Extremely low ESR ceramic capacitors with value less than 1µF must have a 2Ω resistor added in series wit the output capacitor.

Transient and Switching Performance

The LT1313 is designed to produce minimal overshoo with capacitors in the range of 1µF to 10µF. Large capacitor values can be used with a slowing of rise an fall times.

The positive output slew rate is determined by the 330m current limit and the output capacitor. The rise time for a 0V to 12V transition is approximately 40µs and the ris time for a 10µF capacitor is roughly 400µs (see th Transient Response curves in the Typical Performanc Characteristics section).

ıPPLICATIONS INFORMATION

he fall time from 12V to 0V is set by the output capacitor nd an internal pull-down current source which sinks bout 30mA. This source will fully discharge a 1µF capaci- ɔr in less than 1ms.

hermal Considerations

'ower dissipated by the device is the sum of two compo- ents: output current multiplied by the input-output differ- ntial voltage: $I_{OUT} \times (V_{IN} - V_{OUT})$, and ground pin current ıultiplied by supply voltage: $(I_{GND} \times V_{IN})$.

he ground pin current can be found by examining the ıround Pin Current curves in the Typical Performance haracteristics section.

leat sinking, for surface mounted devices, is accom- lished by using the heat spreading capabilities of the PC oard and its copper traces.

he junction temperature of the LT1313 must be limited to 25°C to ensure proper operation. Use Table 1, in con- ınction with the typical performance graphs, to calculate ıe power dissipation and die temperature for a particular pplication and ensure that the die temperature does not xceed 125°C under any operating conditions.

able 1. 16-Pin SO Package*

COPPER AREA			THERMAL RESISTANCE
)PSIDE	BACKSIDE	BOARD AREA	(JUNCTION-TO-AMBIENT)
500 sq mm	2500 sq mm	2500 sq mm	120°C/W
000 sq mm	2500 sq mm	2500 sq mm	120°C/W
25 sq mm	2500 sq mm	2500 sq mm	125°C/W
000 sq mm	1000 sq mm	1000 sq mm	131°C/W

Device is mounted on topside.

Calculating Junction Temperature

Example: given an output voltage of 12V, an input supply voltage of 14V, and an output current of 100mA (one VPP output), and a maximum ambient temperature of 50°C, what will the maximum junction temperature be?

Power dissipated by the device will be equal to:

$$I_{OUT} \times (V_S - VPP_{OUT}) + (I_{GND} \times V_{IN})$$

where,

I_{OUT} = 100mA
V_{IN} = 14V
I_{GND} at (I_{OUT} = 100mA, V_{IN} = 14V) = 5mA

so,

$$P_D = 100mA \times (14V - 12V) + (5mA \times 15V) = 0.275W$$

Using Table 1, the thermal resistance will be in the range of 120°C/W to 131°C/W depending upon the copper area. So the junction temperature rise above ambient will be less than or equal to:

$$0.275W \times 131°C/W = 36°C$$

The maximum junction temperature will then be equal to the junction temperature rise above ambient plus the maximum ambient temperature or:

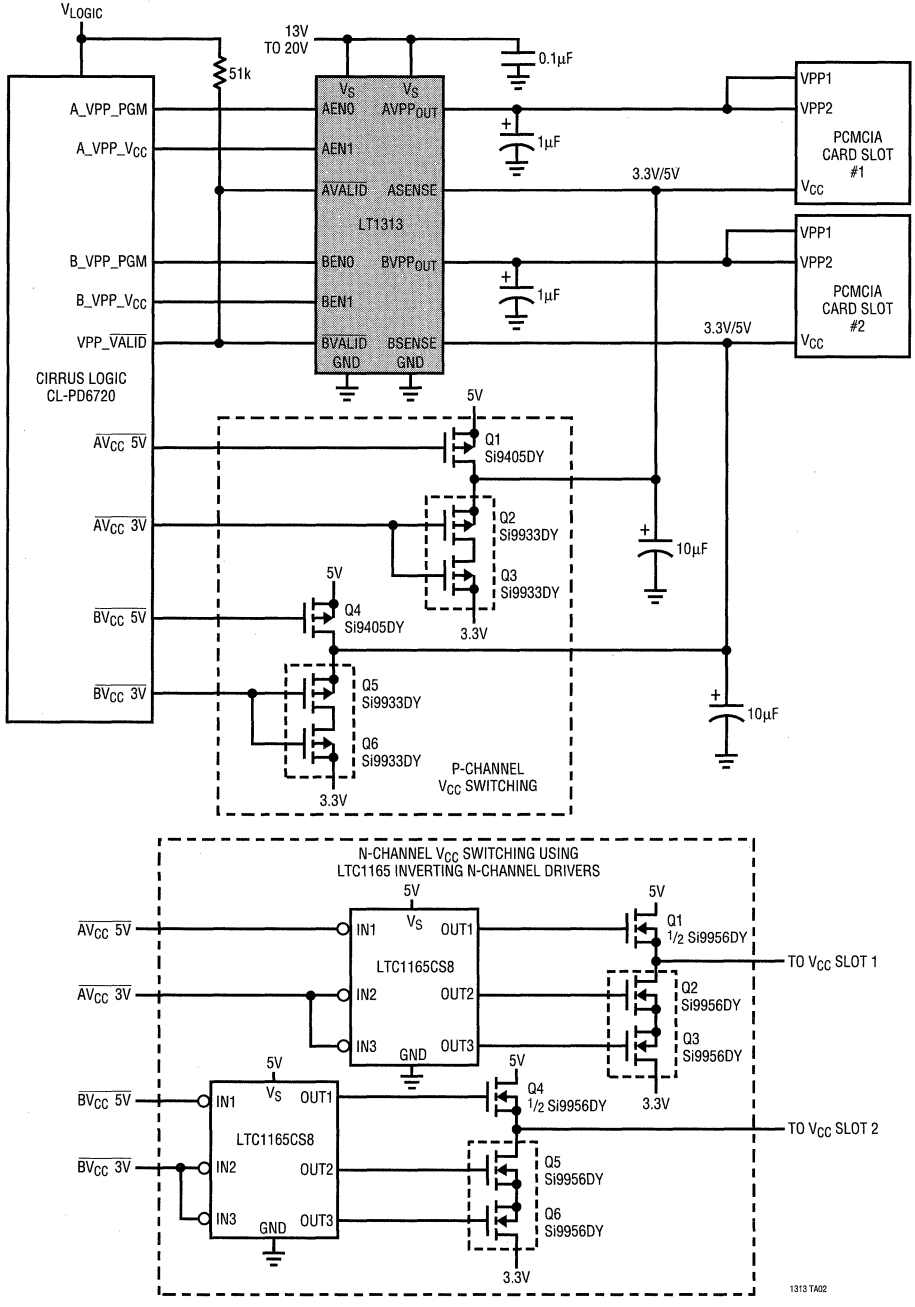
$$T_{JMAX} = 50°C + 36°C = 86°C$$

For more detailed applications information, see the LT1312 Single PCMCIA VPP Driver/Regulator data sheet.

4

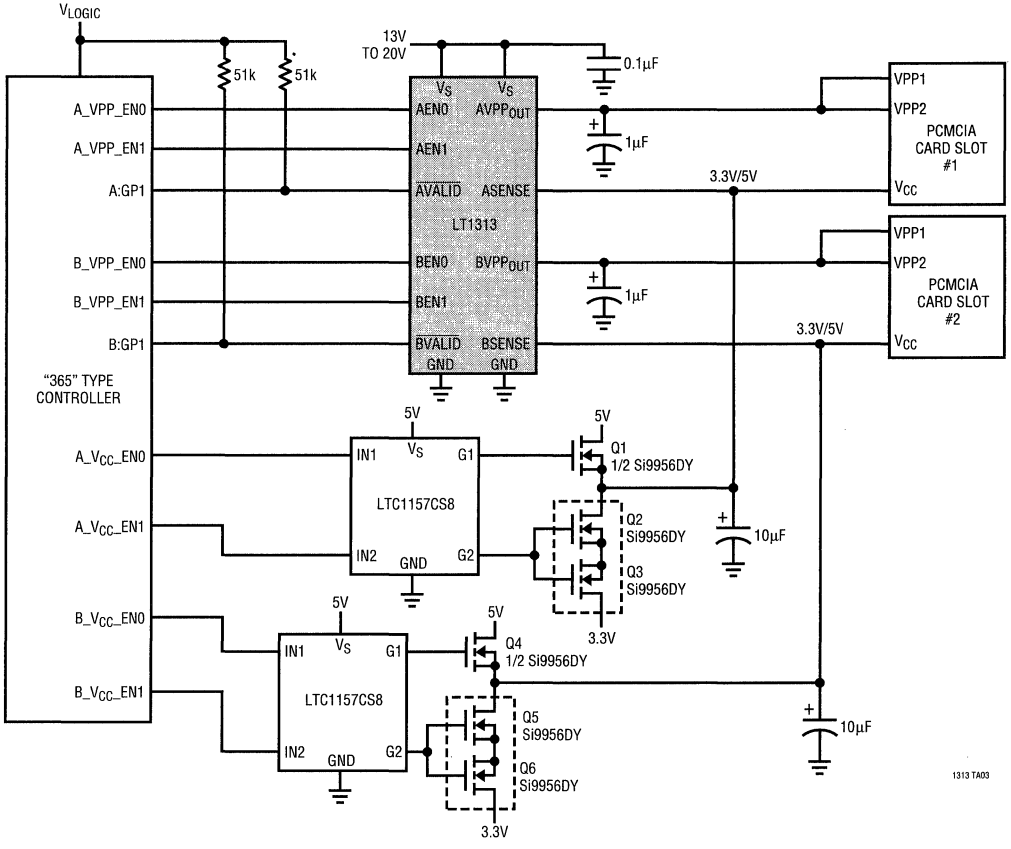
TYPICAL APPLICATIONS

Dual Slot PCMCIA Interface to CL-PD6720



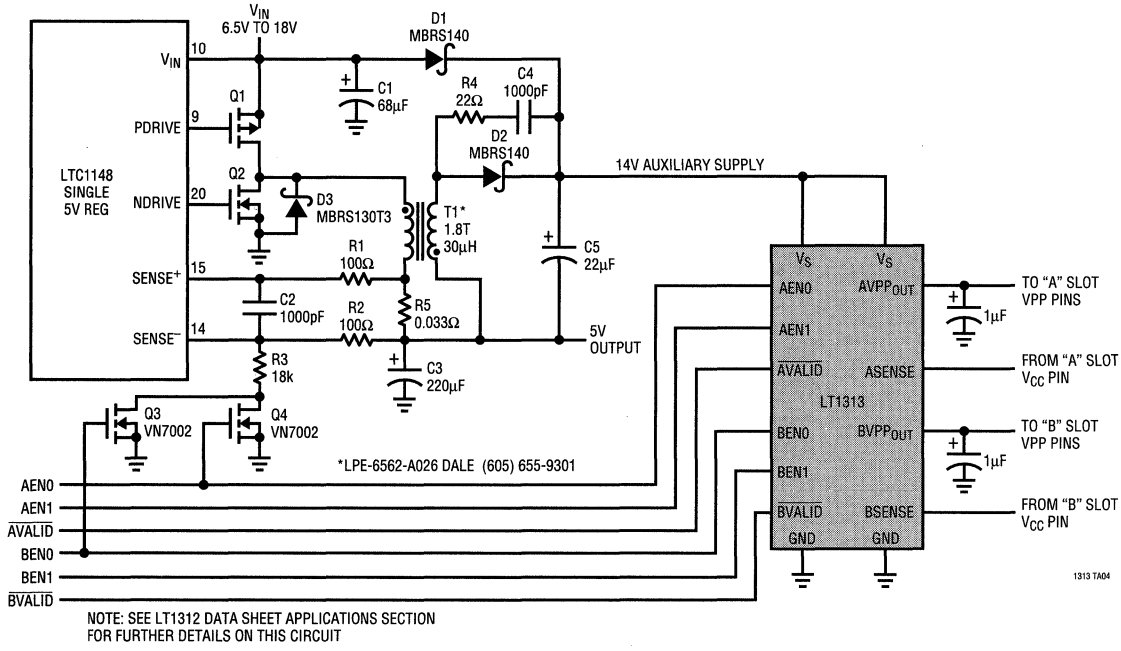
TYPICAL APPLICATIONS

Dual Slot PCMCIA Interface to "365" Type Controller



TYPICAL APPLICATIONS

Dual Slot PCMCIA Driver/Regulator Powered from Auxiliary Winding on 5V Inductor of LTC1142HV Dual 5V/3.3V Switching Regulator



NOTE: SEE LT1312 DATA SHEET APPLICATIONS SECTION FOR FURTHER DETAILS ON THIS CIRCUIT

RELATED PARTS

See PCMCIA Product Family table on the first page of this data sheet.

PCMCIA Switching Matrix with Built-In N-Channel V_{CC} Switch Drivers

FEATURES

- **Output Current Capability: 120mA**
- **External 12V Regulator Can Be Shut Down**
- **Built-In N-Channel V_{CC} Switch Drivers**
- Digital Selection of 0V, V_{CCIN}, VPP_{IN} or Hi-Z
- 3.3V or 5V V_{CC} Supply
- Break-Before-Make Switching
- 0.1μA Quiescent Current in Hi-Z or 0V Mode
- No VPP_{OUT} Overshoot
- Logic Compatible with Standard PCMCIA Controllers

APPLICATIONS

- Notebook Computers
- Palmtop Computers
- Pen-Based Computers
- Handi-Terminals
- Bar-Code Readers

DESCRIPTION

The LTC®1314/LTC1315 provide the power switching necessary to control Personal Computer Memory Card International Association (PCMCIA) Release 2.0 card slots. When used in conjunction with a PC card interface controller, these devices form a complete minimum component count interface for palmtop, pen-based and notebook computers.

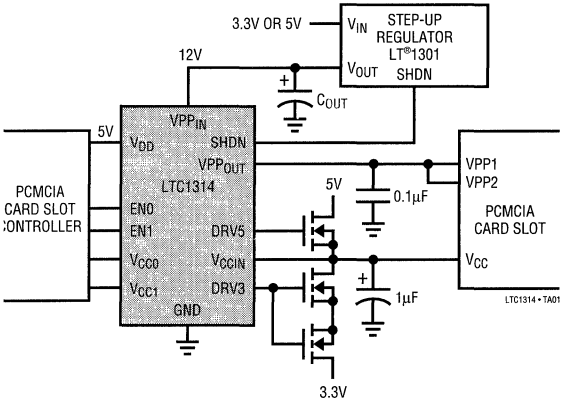
The LTC1314/LTC1315 provide 0V, 3.3V, 5V, 12V and Hi-Z power output for flash VPP programming. A built-in charge pump produces 12V of gate drive for inexpensive N-channel 3.3V/5V V_{CC} switching. The 12V regulator can be shut down when 12V is not required at VPP_{OUT}. All digital inputs are TTL compatible and interface directly with industry standard PC card interface controllers.

The LTC1314 is available in 14-pin SO and the LTC1315 in 24-pin SSOP.

4

TYPICAL APPLICATION

Typical PCMCIA Single Slot Driver



Linear Technology PCMCIA Product Family

DEVICE	DESCRIPTION	PACKAGE
LT1312	SINGLE PCMCIA VPP DRIVER/REGULATOR	8-PIN SO
LT1313	DUAL PCMCIA VPP DRIVER/REGULATOR	16-PIN SO*
LTC®1314	SINGLE PCMCIA SWITCH MATRIX	14-PIN SO
LTC1315	DUAL PCMCIA SWITCH MATRIX	24-PIN SSOP
LTC1470	PROTECTED V_{CC} 5V/3.3V SWITCH MATRIX	8-PIN SO
LTC1472	PROTECTED V_{CC} AND VPP SWITCH MATRIX	16-PIN SO*

*NARROW BODY

LTC1314 Truth Table

EN0	EN1	V_{CC0}	V_{CC1}	VPP_{OUT}	DRV3	DRV5
0	0	X	X	GND	X	X
0	1	X	X	V_{CCIN}	X	X
1	0	X	X	VPP_{IN}	X	X
1	1	X	X	Hi-Z	X	X
X	X	1	0	X	1	0
X	X	0	1	X	0	1
X	X	0	0	X	0	0
X	X	1	1	X	0	0

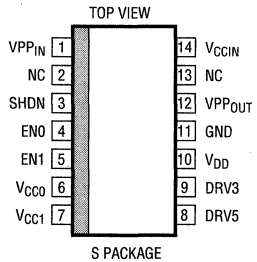
X = DON'T CARE

ABSOLUTE MAXIMUM RATINGS

VPP_{IN} to GND ..... 13.2V to –0.3V
V_{DD} to GND ..... 7V to –0.3V
V_{CCIN} to GND ..... 7V to –0.3V
VPP_{OUT} to GND ..... 13.2V to –0.3V

Digital Input Voltage ..... 7V to –0.3V
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

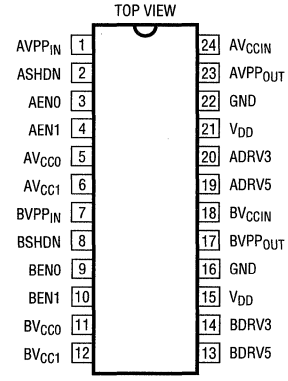


S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC1314CS



G PACKAGE
24-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC1315CG

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{CCIN} = 5V, VPP_{IN} = 12V, T_A = 25°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1314/LTC1315 MIN	TYP	MAX	UNITS
V_{CCIN}	Input Voltage Range		●	3		5.5	V
VPP_{IN}	Input Voltage Range		●	0		12.6	V
V_{DD}	Supply Voltage Range		●	4.5		5.5	V
I_{CC}	V_{CCIN} Supply Current, No Load	VPP_{OUT} = VPP_{IN}, V_{CCIN}, 0V or Hi-Z	●		0.1	1	µA
I_{PP}	VPP_{IN} Supply Current, No Load	VPP_{OUT} = VPP_{IN}, V_{CCIN} VPP_{OUT} = 0V, Hi-Z	● ●		15 0.1	40 1	µA µA
I_{DD}	V_{DD} Supply Current, No Load	VPP_{OUT} = VPP_{IN} or V_{CCIN} VPP_{OUT} = 0V or Hi-Z VPP_{OUT} = 0V or Hi-Z, DRV3 or DRV5 On	● ● ●		60 0.1 85	120 10 200	µA µA µA
I_{IN}	Input Current: EN0, EN1, V_{CC0} or V_{CC1}	0V < V_{IN} < V_{DD}	●			±1	µA
I_{OUT}	High Impedance Output Leakage Current	EN0 = EN1 = 5V, 0V < VPP_{OUT} < 12V	●		0.1	10	µA
R_{ON}	On Resistance, VPP_{OUT} = VPP_{IN} On Resistance, VPP_{OUT} = V_{CCIN} On Resistance, VPP_{OUT} = GND	VPP_{IN} = 12V, I_{LOAD} = 120mA V_{CCIN} = 5V, I_{LOAD} = 5mA V_{DD} = 5V, I_{SINK} = 1mA	● ● ●		0.55 2 100	1.2 5 250	Ω Ω Ω
V_{INH}	Input High Voltage, Digital Inputs		●	2			V
V_{INL}	Input Low Voltage, Digital Inputs		●			0.8	V

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{CCIN} = 5V, VPP_{IN} = 12V, T_A = 25°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC1314/LTC1315 MIN	TYP	MAX	UNITS
V_{OH}	SHDN Output High Voltage	VPP_{OUT} = V_{CCIN}, 0V or Hi-Z, I_{LOAD} = 400µA	●	3.5			V
V_{OL}	SHDN Output Low Voltage	VPP_{OUT} = VPP_{IN}, I_{SINK} = 400µA	●			0.4	V
V_G-V_{DD}	Gate Voltage Above Supply	V_{DRV3} or V_{DRV5}	●	6	7	13	V
t_{ON}	Turn-On Time, DRV3 and DRV5	C_{GATE} = 1000pF, Time for V_{GATE} > V_{DD} + 1V		50	150	500	µs
t_{OFF}	Turn-Off Time, DRV3 and DRV5	C_{GATE} = 1000pF, Time for V_{GATE} < 0.5V		3	10	30	µs
t_1	Delay + Rise Time	VPP_{OUT} = GND to V_{CCIN}, VPP_{IN} = 0V, Note 1		5	15	50	µs
t_2	Delay + Rise Time	VPP_{OUT} = GND to VPP_{IN} (Note 1)		5	15	50	µs
t_3	Delay + Rise Time	VPP_{OUT} = V_{CCIN} to VPP_{IN} (Note 1)		5	15	50	µs
t_4	Delay + Fall Time	VPP_{OUT} = VPP_{IN} to V_{CCIN} (Note 3)		2	6	20	µs
t_5	Delay + Fall Time	VPP_{OUT} = VPP_{IN} to GND (Note 2)		15	50	150	µs
t_6	Delay + Fall Time	VPP_{OUT} = V_{CCIN} to GND, VPP_{IN} = 0V (Note 2)		10	25	100	µs
t_7	Output Turn-On Delay	VPP_{OUT} = Hi-Z to VPP_{IN} or V_{CCIN} (Notes 1, 6)		5	15	50	µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: To 90% of the final value, C_{OUT} = 0.1µF, R_{OUT} = 2.9k.

Note 2: To 10% of the final value, C_{OUT} = 0.1µF, R_{OUT} = 2.9k.

Note 3: To 50% of the initial value, C_{OUT} = 0.1µF, R_{OUT} = 2.9k.

Note 4: Measured current data is per channel.

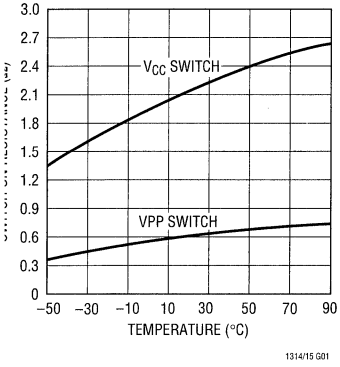
Note 5: Input logic low equal to 0V, high equal to 5V.

Note 6: VPP_{IN} = 0V when switching from Hi-Z to V_{CCIN}.

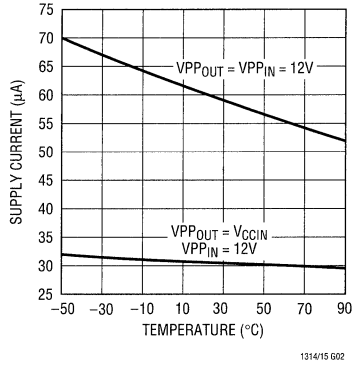
4

TYPICAL PERFORMANCE CHARACTERISTICS

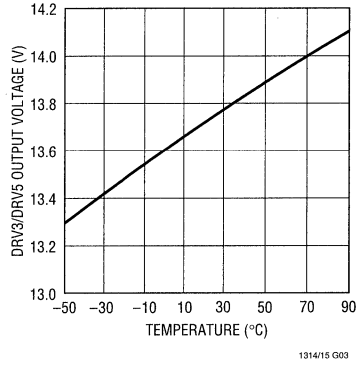
Switch On Resistance vs Temperature



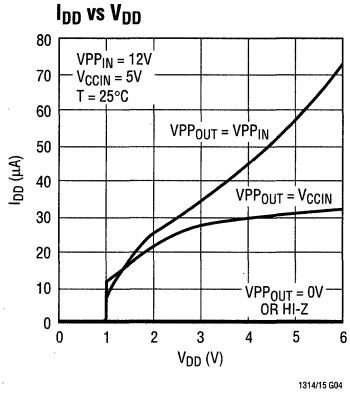
Supply Current vs Temperature

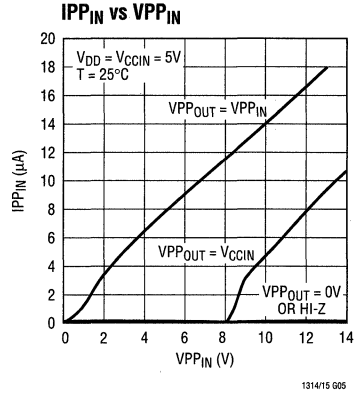


DRV3/DRV5 Output Voltage vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS





PIN FUNCTIONS

LTC1314

VPP_{IN} (Pin 1): 12V Power Input.

NC (Pin 2): Not Connected.

SHDN (Pin 3): Shutdown Output. When the output is high, the external 12V regulator can be shut down to conserve power consumption.

EN0, EN1 (Pins 4, 5): Logic inputs that control the voltage output on VPP_{OUT}. The input thresholds are compatible with TTL/CMOS levels. Refer to Truth Table.

V_{CC0} (Pin 6): Logic input that controls the state of the MOSFET gate driver DRV3. ESD protection device limits input excursions to 0.6V below ground.

V_{CC1} (Pin 7): Logic input that controls the state of the MOSFET gate driver DRV5. ESD protection device limits input excursions to 0.6V below ground.

DRV5, DRV3 (Pins 8, 9): Gate driver outputs that control the external MOSFETs that switch the V_{CC} pin of card slot to Hi-Z, 3.3V, or 5V.

V_{DD} (Pin 10): Positive Supply, $4.5V \leq V_{DD} \leq 5.5V$. This pin supplies the power to the control logic and the charge pumps and must be continuously powered.

GND (Pin 11): Ground Connection.

VPP_{OUT} (Pin 12): Switched output that provides 0V, 3.3V, 5V, 12V, or Hi-Z to the VPP pin of the card slot. Refer to Truth Table.

NC (Pin 13): Not Connected.

V_{CCIN} (Pin 14): 5V or 3.3V Power Input.

PIN FUNCTIONS

LTC1315

VPP$_{IN}$ (Pins 1, 7): 12V Power Inputs.

SHDN (Pins 2, 8): Shutdown Outputs. When the output is high, the external 12V regulator can be shut down to conserve power consumption.

EN0, EN1 (Pins 3, 4, 9, 10): Logic inputs that control the voltage output on VPP$_{OUT}$. The input thresholds are compatible with TTL/CMOS levels. Refer to the Truth Table.

V$_{CC0}$ (Pins 5, 11): Logic inputs that control the state of the MOSFET gate driver DRV3. ESD protection device limits input excursions to 0.6V below ground.

V$_{CC1}$ (Pins 6, 12): Logic inputs that control the state of the MOSFET gate driver DRV5. ESD protection device limits input excursions to 0.6V below ground.

DRV5, DRV3 (Pins 13, 14, 19, 20): Gate driver outputs that control the external MOSFETs that switch the V$_{CC}$ pin of card slot to Hi-Z, 3.3V, or 5V.

V$_{DD}$ (Pins 15, 21): Positive Supplies, 4.5V ≤ V$_{DD}$ ≤ 5.5V. These pins supply the power to the control logic and the charge pumps and must be continuously powered.

GND (Pins 16, 22): Ground Connections.

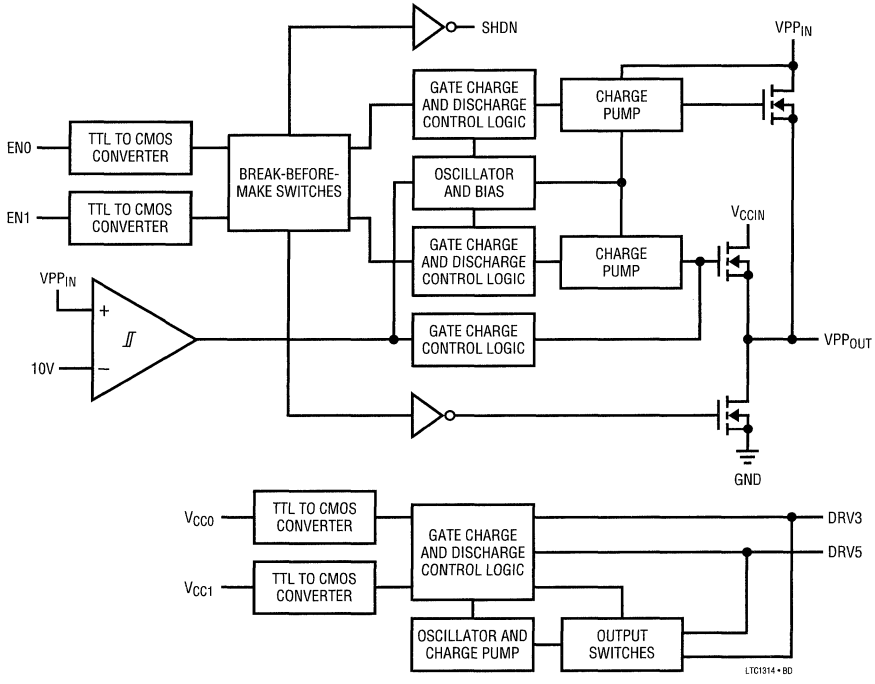
VPP$_{OUT}$ (Pins 17, 23): Switched outputs that provide 0V, 3.3V, 5V, 12V, or Hi-Z to the VPP pin of the card slot. Refer to the Truth Table.

V$_{CCIN}$ (Pins 18, 24): 5V or 3.3V Power Inputs.

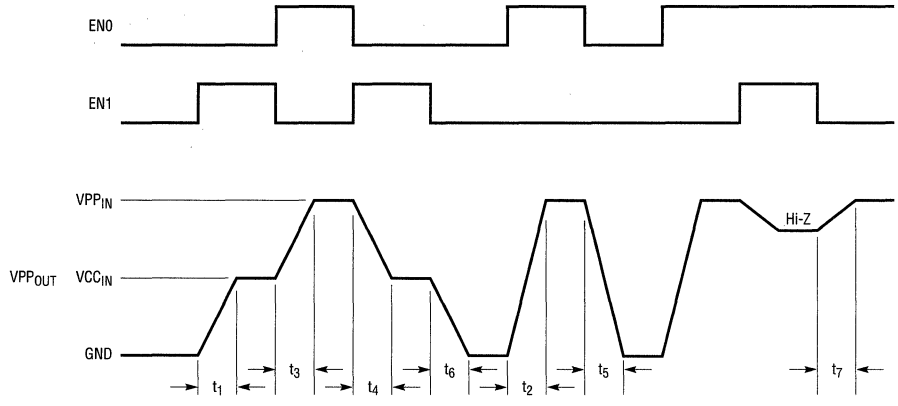
4

BLOCK DIAGRAM

LTC1314 or 1/2 LTC1315



SWITCHING TIME WAVEFORMS



NOTE: 1µF CAPACITOR CONNECTED ON BOTH VPP$_{IN}$ AND V$_{CCIN}$ PINS AT TIMING TEST

LTC1314•SW

APPLICATIONS INFORMATION

PCMCIA VPP control is easily accomplished using the LTC1314 or LTC1315 switching matrix. Two control bits (LTC1314) or four control bits (LTC1315) determine the output voltage and standby/operate mode conditions. Output voltages of 0V, V$_{CCIN}$ (3.3V or 5V), VPP$_{IN}$, or a high impedance state are available. When either the high impedance or low voltage (0V) conditions are selected, the device switches into "sleep" mode and draws 0.1µA of current from the V$_{DD}$ supply.

The LTC1314/LTC1315 are low resistance power MOSFET switching matrices that operate from the computer system main power supply. Device power is obtained from V$_{DD}$, which is 5V ±0.5V. The gate drives for the NFETs (both internal and external) are derived from internal charge pumps, therefore VPP$_{IN}$ is only required when it's switched to VPP$_{OUT}$. Internal break-before-make switches determine the output voltage and device mode.

Flash Memory Card VPP Power Considerations

PCMCIA compatible flash memory cards require tight regulation of the 12V VPP programming supply to ensure that the internal flash memory circuits are never subjected to damaging conditions. Flash memory circuits are typically rated with an absolute maximum of 13.5V and VPP must be maintained at 12V ±5% under all possible load conditions during erase and program cycles. Undervoltage can decrease specified flash memory reliability and overvoltage can damage the device.

V$_{CC}$ Switch Driver and VPP Switch Matrix

Figures 1 and 2 show the approach that is very space and power efficient. The LTC1314/LTC1315 used in conjunction with the LT1301 DC/DC converter, provide complete power management for a PCMCIA card slot. The LTC1314/LTC1315 and LT1301 combination provides a highly efficient, minimal parts count solution. These circuits are especially good for applications that are adding a PCMCIA socket to existing systems that currently have only 5V or 3.3V available.

The LTC1314 drives three N-channel (LTC1315 six N-channel) MOSFETs that provide V$_{CC}$ pin power switching. On-chip charge pumps provide the necessary voltage to fully enhance the switches. With the charge pumps on-chip, the MOSFET drive is available without the need for a 12V supply. The LTC1314/LTC1315 provide a natural break-before-make action and smooth transitions due to

APPLICATIONS INFORMATION

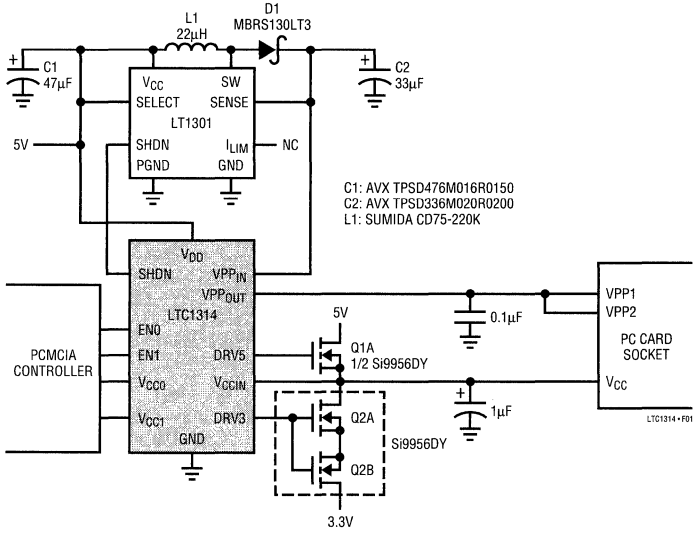


Figure 1. LTC1314 Switch Matrix with the LT1301 Boost Regulator

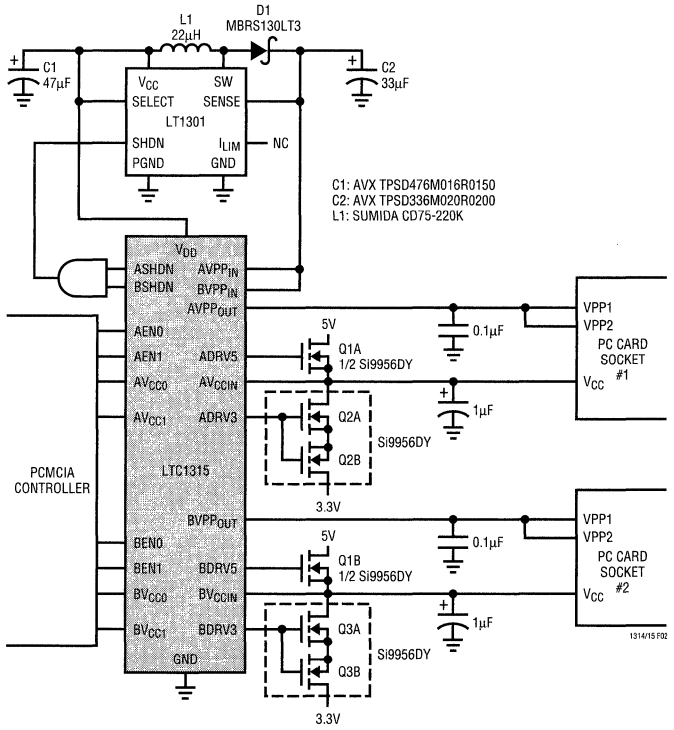


Figure 2. Typical Two-Socket Application Using the LTC1315 and the LT1301

APPLICATIONS INFORMATION

the asymmetrical turn-on and turn-off of the MOSFETs. The LT1301 switching regulator is in shutdown mode and consumes only 10μA until the VPP pins require 12V.

The VPP switching is accomplished by a combination of the LTC1314/LTC1315 and LT1301. The LT1301 is in shutdown mode to conserve power until the VPP pins require 12V. When the VPP pins require 12V, the LT1301 is activated and the LTC1314/LTC1315's internal switches route the VPP_{IN} pin to the VPP_{OUT} pin. The LT1301 is capable of delivering 12V at 120mA maintaining high efficiency. The LTC1314/LTC1315's break-before-make and slope-controlled switching will ensure that the output voltage transition will be smooth, of moderate slope, and without overshoot. This is critical for flash memory products to prevent damaging parts from overshoot and ringing exceeding the 13.5V device limit.

With Higher Voltage Supplies Available

Often systems have an available supply voltage greater than 12V. The LTC1314/LTC1315 can be used in conjunction with an LT1121 linear regulator to supply the PC card socket with all necessary voltages. Figures 3 and 4 show these circuits. The LTC1314/LTC1315 enable the LT1121 linear regulator only when 12V is required at the VPP pins. In all other modes the LT1121 is in shutdown mode and consumes only 16μA. The LT1121 also provides thermal shutdown and current limiting features to protect the socket, the card and the system regulator.

Supply Bypassing

For best results, bypass V_{CCIN} and VPP_{IN} at their inputs with 1μF capacitors. VPP_{OUT} should have a 0.01μF to 0.1μF capacitor for noise reduction and electrostatic discharge (ESD) damage prevention. Larger values of output capacitor will create large current spikes during transitions, requiring larger bypass capacitors on the V_{CCIN} and VPP_{IN} pins.

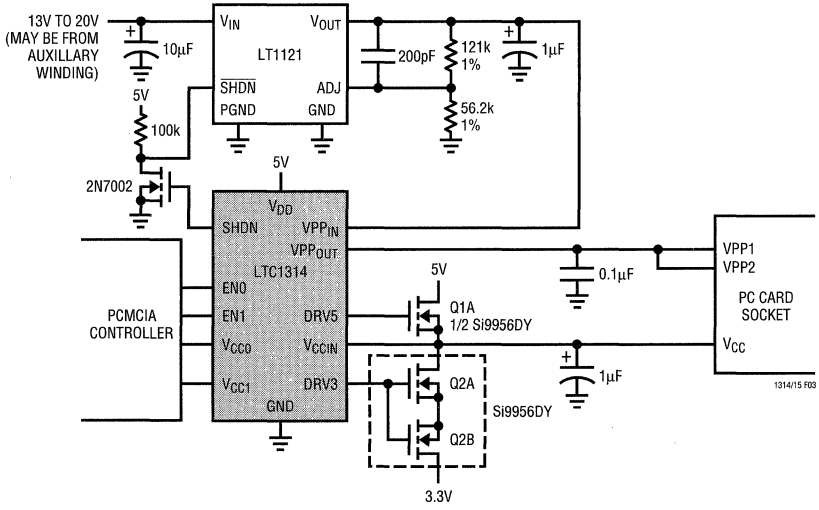


Figure 3. LTC1314 with the LT1121 Linear Regulator

APPLICATIONS INFORMATION

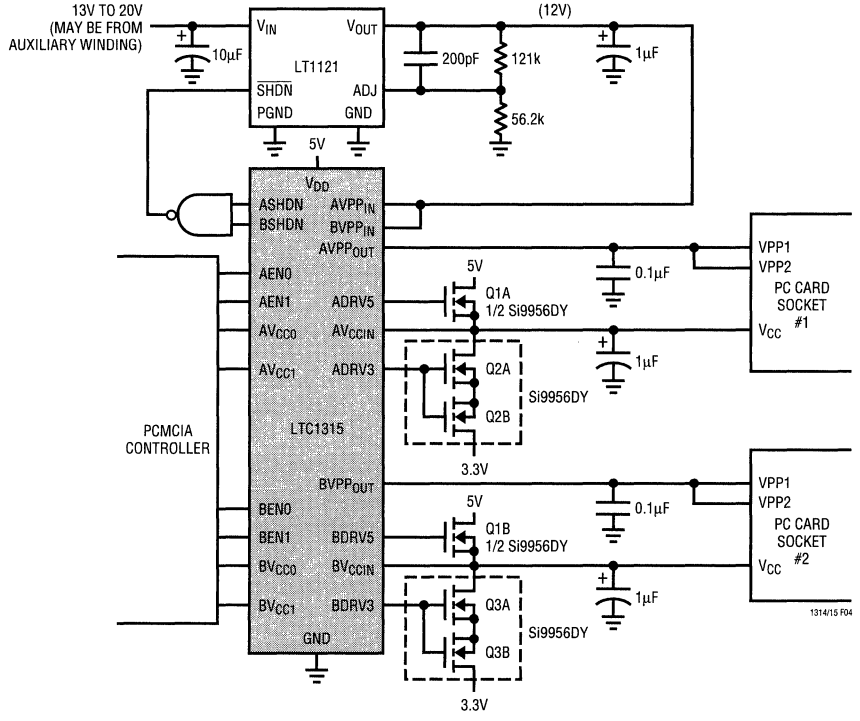
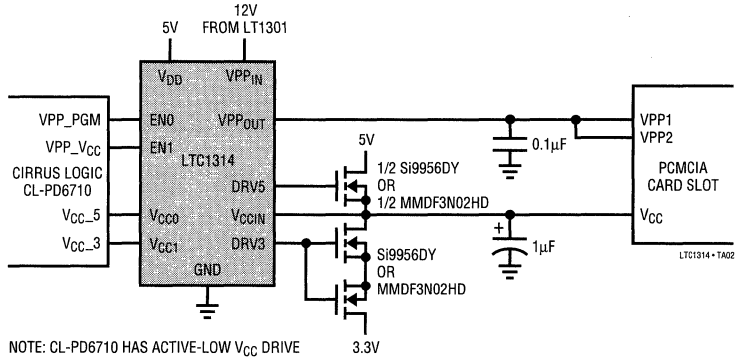


Figure 4. Typical Two-Socket Application Using the LTC1315 and the LT1121

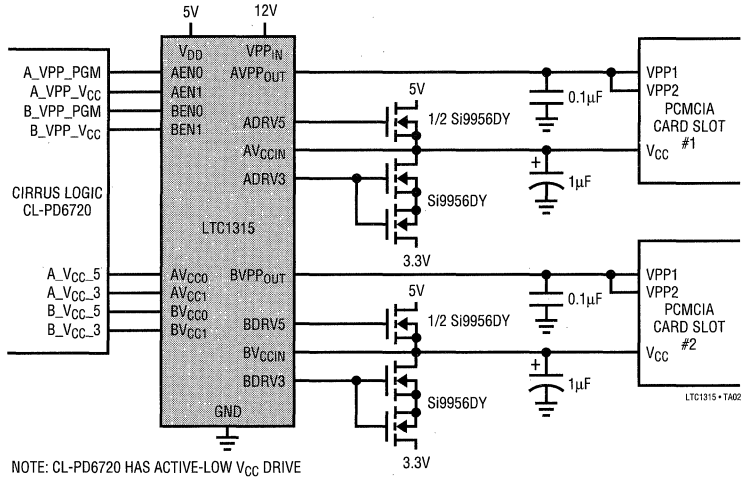
TYPICAL APPLICATIONS

Single Slot Interface to CL-PD6710



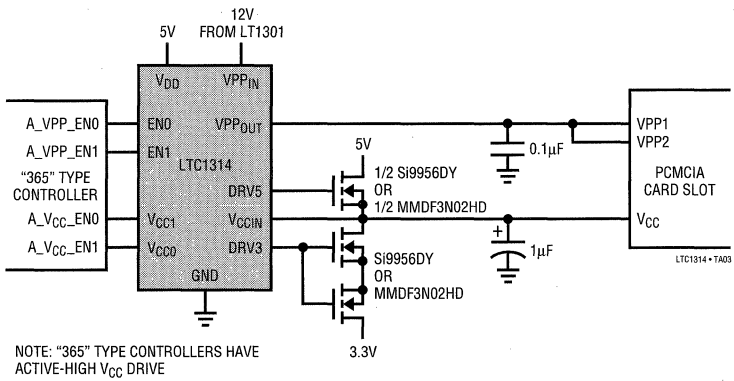
TYPICAL APPLICATIONS

Dual Slot Interface to CL-PD6720



NOTE: CL-PD6720 HAS ACTIVE-LOW V_{CC} DRIVE

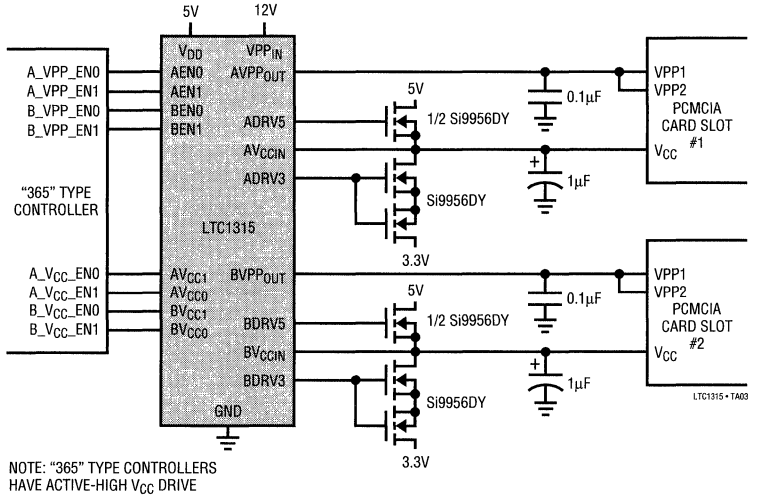
Single Slot Interface to "365" Type Controller



NOTE: "365" TYPE CONTROLLERS HAVE
ACTIVE-HIGH V_{CC} DRIVE

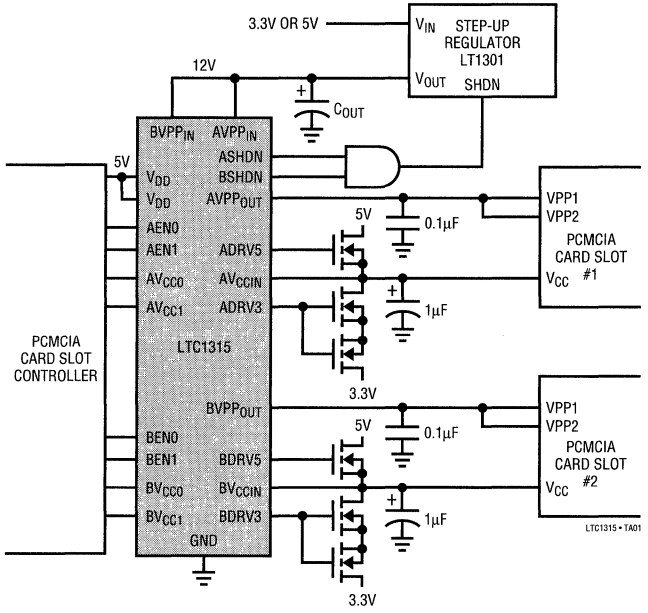
TYPICAL APPLICATIONS

Dual Slot Interfae to "365" Type Controller



NOTE: "365" TYPE CONTROLLERS HAVE ACTIVE-HIGH V_{CC} DRIVE

Typical PCMCIA Dual Slot Driver



LTC1315 Truth Table

EN0	EN1	V_{CC0}	V_{CC1}	VPP_{OUT}	DRV3	DRV5
0	0	X	X	GND	X	X
0	1	X	X	V_{CCIN}	X	X
1	0	X	X	VPP_{IN}	X	X
1	1	X	X	Hi-Z	X	X
X	X	1	0	X	1	0
X	X	0	1	X	0	1
X	X	0	0	X	0	0
X	X	1	1	X	0	0

X = DON'T CARE

RELATED PARTS

See PCMCIA Product Family table on the first page of this data sheet.

Single and Dual PCMCIA Protected 3.3V/5V V_{CC} Switches

FEATURES

- **Single 3.3V/5V Switch in 8-Pin SO Package**
- **Dual 3.3V/5V Switch in 16-Pin SO Package**
- **Built-In Current Limit and Thermal Shutdown**
- Built-In Charge Pumps (No 12V Required)
- Extremely Low $R_{DS(ON)}$ MOSFET Switches
- Output Current Capability: 1A
- Inrush Current Limited (Drives 150µF Loads)
- Quiescent Current in Standby: 1µA
- No Parasitic Body Diodes
- Built-In XOR Function Eliminates "Glue" Logic
- Break-Before-Make Switching
- Controlled Rise and Fall Times

APPLICATIONS

- Notebook Computers
- Palmtop Computers
- Pen-Based Computers
- Handi-Terminals
- PC Card Reader/Writers
- 3.3V/5V Power Supply Switch

DESCRIPTION

The LTC®1470 switches the V_{CC} pins of a Personal Computer Memory Card International Association (PCMCIA) card slot between three operating states: OFF, 3.3V and 5V. Two low $R_{DS(ON)}$ N-channel power MOSFETs are driven by a built-in charge pump which generates a voltage higher than the supply voltage to fully enhance each switch when selected by the input control logic.

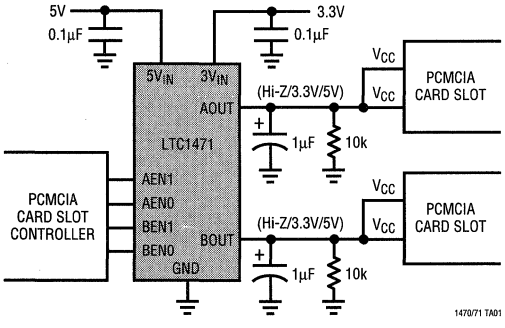
The LTC1470 inputs are compatible with industry standard PCMCIA controllers. A built-in XOR ensures that both switches are never on at the same time. This function also makes the LTC1470 compatible with both active-low and active-high controllers (see Applications Information section). The switch rise times are controlled to eliminate power supply glitching.

The LTC1470 features built-in SafeSlot™ current limit and thermal shutdown. The output is limited to 1A during short circuit to ground but 2A of peak operating current is allowed.

The LTC1471 is a dual version of the LTC1470 and is available in a 16-pin SO package.

TYPICAL APPLICATION

Dual Slot PCMCIA 3.3V/5V V_{CC} Switch



Linear Technology PCMCIA Product Family

DEVICE	DESCRIPTION	PACKAGE
LT®1312	Single PCMCIA VPP Driver/Regulator	8-Pin SO
LT1313	Dual PCMCIA VPP Driver/Regulator	16-Pin SO*
LTC1314	Single PCMCIA Switch Matrix	14-Pin SO
LTC1315	Dual PCMCIA Switch Matrix	24-Pin SSOP
LTC1470	Single Protected V_{CC} 3.3V/5V Switch Matrix	8-Pin SO
LTC1471	Dual Protected V_{CC} 3.3V/5V Switch Matrix	16-Pin SO*
LTC1472	Protected V_{CC} and VPP Switch Matrix	16-Pin SO*

*Narrow Body

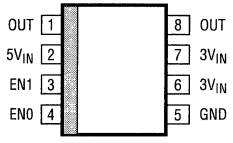
ABSOLUTE MAXIMUM RATINGS

3.3V Supply Voltage (Note 1) 7V
5V Supply Voltage (Note1) 7V
Enable Input Voltage ..... 7V to (GND – 0.3V)
Output Voltage (OFF) (Note 1) ..... 7V to (GND – 0.3V)
Output Short-Circuit Duration ..... Indefinite

Operating Temperature ..... 0°C to 70°C
Junction Temperature ..... 100°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

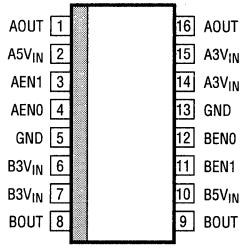


S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1470CS8
S8 PART MARKING
1470

TOP VIEW



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC1471CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

$3V_{IN}$ = 3.3V, $5V_{IN}$ = 5V (Note 2), T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$3V_{IN}$	3.3V Supply Voltage Range			2.70		3.60	V
$5V_{IN}$	5V Supply Voltage Range			4.75		5.25	V
I_{3VIN}	3.3V Supply Current	Program to Hi-Z (Note 3)	●		0.01	10	µA
		Program to 3.3V, No Load (Note 3)	●		40	80	µA
		Program to 5V, No Load (Note 3)	●		0.01	10	µA
I_{5VIN}	5V Supply Current	Program to Hi-Z (Note 3)	●		0.01	10	µA
		Program to 3.3V (Note 3)	●		100	160	µA
		Program to 5V (Note 3)	●		140	200	µA
R_{ON}	3.3V Switch ON Resistance	Program to 3.3V, I_{OUT} = 500mA			0.12	0.16	Ω
	5V Switch ON Resistance	Program to 5V, I_{OUT} = 500mA			0.14	0.18	Ω
I_{LKG}	Output Leakage Current OFF	Program to Hi-Z, 0V ≤ V_{OUT} ≤ 5V (Note 3)	●			±10	µA
I_{LIM3V}	3.3V Current Limit	Program to 3.3V, V_{OUT} = 0V (Note 4)			1		A
I_{LIM5V}	5V Current Limit	Program to 5V, V_{OUT} = 0V (Note 4)			1		A
V_{ENH}	Enable Input High Voltage		●	2.0			V
V_{ENL}	Enable Input Low Voltage		●			0.8	V
I_{EN}	Enable Input Current	0V ≤ V_{EN} ≤ 5V	●			±1	µA

ELECTRICAL CHARACTERISTICS

$3V_{IN}$ = 3.3V, $5V_{IN}$ = 5V (Note 2), T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_0 to t_3	Delay and Rise Time (Note 5)	Transition from 0V to 3.3V, R_{OUT} = 100Ω, C_{OUT} = 1µF	0.2	0.32	1.0	ms
t_3 to t_5	Delay and Rise Time (Note 5)	Transition from 3.3V to 5V, R_{OUT} = 100Ω, C_{OUT} = 1µF	0.2	0.52	1.0	ms
t_0 to t_5	Delay and Rise Time (Note 5)	Transition from 0V to 5V, R_{OUT} = 100Ω, C_{OUT} = 1µF	0.2	0.38	1.0	ms

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: For the LTC1470, the two output pins (1, 8) must be connected together and the two 3.3V supply input pins (6 , 7) must be connected together. For the LTC1471, the two AOUT pins (1, 16) must be connected together, the two BOUT pins (8, 9) must be connected together, the two $A3V_{IN}$ supply input pins (14, 15) must be connected together, the two $B3V_{IN}$ supply pins (6, 7) must be connected together and the two GND pins (5, 13) must be connected together.

Note 2: Power for the input logic and charge pump circuitry is derived from the $5V_{IN}$ supply pin(s) which must be continuously powered.

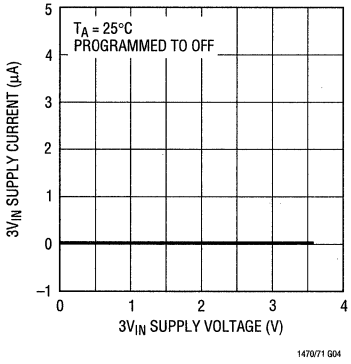
Note 3: Measured current is per channel with the other channel programmed off for the LTC1471.

Note 4: The output is protected with foldback current limit which reduces the short-circuit (0V) currents below peak permissible current levels at higher output voltages.

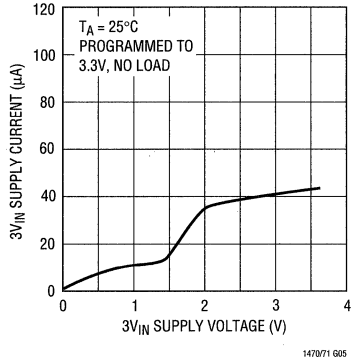
Note 5: To 90% of final value.

TYPICAL PERFORMANCE CHARACTERISTICS (LTC1470 or 1/2 LTC1471)

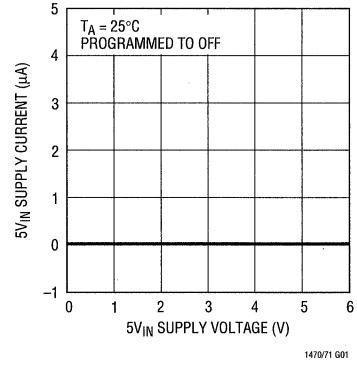
$3V_{IN}$ Supply Current (OFF)



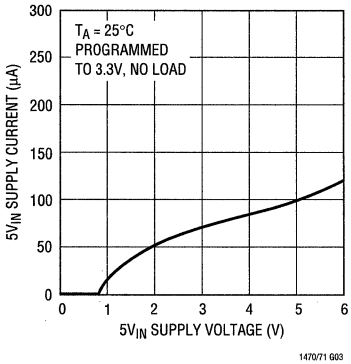
$3V_{IN}$ Supply Current (3.3V ON)



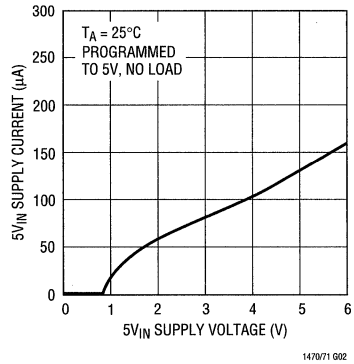
$5V_{IN}$ Supply Current (OFF)



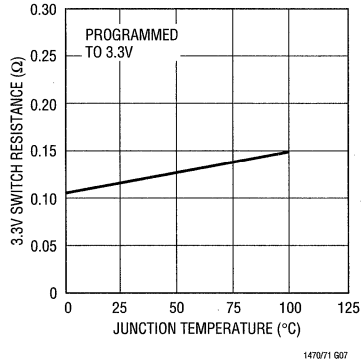
$5V_{IN}$ Supply Current (3.3V ON)



$5V_{IN}$ Supply Current (5V ON)

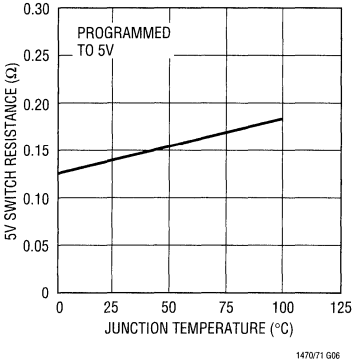


3.3V Switch Resistance

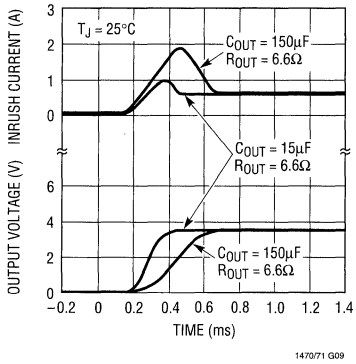


TYPICAL PERFORMANCE CHARACTERISTICS (LTC1470 or 1/2 LTC1471)

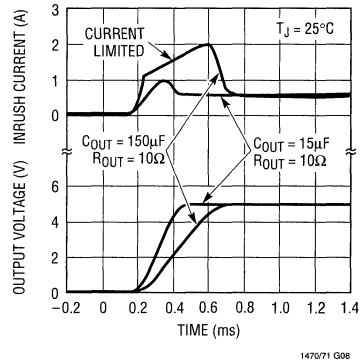
5V Switch Resistance



Inrush Current (3.3V Switch)



Inrush Current (5V Switch)



PIN FUNCTIONS

4

LTC1470

OUT (Pins 1, 8): Output Pins. The outputs of the LTC1470 are switched between three operating states: OFF, 3.3V and 5V. These pins are protected against accidental short circuits to ground by SafeSlot current limit circuitry which protects the socket, the card, and the system power supplies against damage. A second level of protection is provided by thermal shutdown circuitry which protects both switches against over-temperature conditions.

$5V_{IN}$ (Pin 2): 5V Input Supply Pin. The $5V_{IN}$ supply pin serves two purposes. The first purpose is as the power supply input for the 5V NMOS switch. The second purpose is to provide power for the input, gate drive, and protection circuitry for both the 3.3V and 5V V_{CC} switches. This pin must therefore be continuously powered.

EN1, EN0 (Pins 3, 4): Enable Inputs. The two V_{CC} Enable inputs are designed to interface directly with industry standard PCMCIA controllers and are high impedance CMOS gates with ESD protection diodes to ground, and should not be forced below ground. Both inputs have about 100mV of built-in hysteresis to ensure clean switching between operating modes. The LTC1470 is designed to operate *without* 12V power. The gates of the V_{CC} NMOS switches are powered by charge pumps from the $5V_{IN}$ supply pins (see Applications Information section for more detail). The Enable inputs should be turned off (both asserted high or both asserted low) at least 100µs before the $5V_{IN}$ power is removed to ensure that both V_{CC} NMOS switch gates are fully discharged and both switches are in the high impedance mode.

GND (Pin 5): Ground Connection.

$3V_{IN}$ (Pins 6, 7): 3V Input Supply Pins. The $3V_{IN}$ supply pins serve as the power supply input for the 3.3V switches. These pins do not provide any power to the internal control circuitry and therefore do not consume any power when unloaded or turned off.

PIN FUNCTIONS

LTC1471

AOUT, BOUT(Pins 1, 16, 8, 9): Output Pins. The outputs of the LTC1471 are switched between three operating states: OFF, 3.3V and 5V. These pins are protected against accidental short circuits to ground by SafeSlot current limit circuitry which protects the socket, the card, and the system power supplies against damage. A second level of protection is provided by thermal shutdown circuitry.

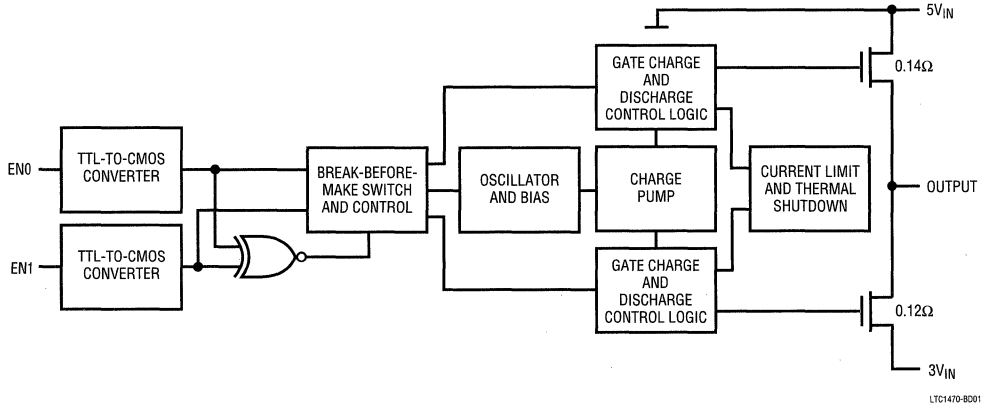
$5V_{IN}$ (Pins 2, 10): 5V Input Supply Pins. The $5V_{IN}$ supply pins serve two purposes. The first purpose is as the power supply input for the 5V NMOS switches. The second purpose is to provide power for the input, gate drive, and protection circuitry. These pins must therefore be continuously powered.

EN1, EN0 (Pins 3, 4, 11, 12): Enable Inputs. The enable inputs are designed to interface directly with industry standard PCMCIA controllers and are high impedance CMOS gates with ESD protection diodes to ground, and should not be forced below ground. All four inputs have about 100mV of built-in hysteresis to ensure clean switching between operating modes. The LTC1471 is designed to operate *without* 12V power. The gates of the V_{CC} NMOS switches are powered by charge pumps from the $5V_{IN}$ supply pins (see Applications Information section for more detail). The enable inputs should be turned off at least 100µs before the $5V_{IN}$ power is removed to ensure that all NMOS switch gates are fully discharged and are in the high impedance mode.

GND (Pins 5, 13): Ground Connections.

$3V_{IN}$ (Pins 6, 7, 14, 15):3V Input Supply Pins. The $3V_{IN}$ supply pins serve as the power supply input for the 3.3V switches. These pins do not not provide any power to the internal control circuitry, and therefore, do not consume any power when unloaded or turned off.

BLOCK DIAGRAM (LTC1470 or 1/2 LTC1471)



OPERATION

The LTC1470 (or 1/2 of the LTC1471) consists of the following functional blocks:

Input TTL/CMOS Converters

The enable inputs are designed to accommodate a wide range of 3V and 5V logic families. The input threshold voltage is approximately 1.4V with approximately 100mV of hysteresis. The inputs enable the bias generator, the gate charge pumps and the protection circuitry which are powered from the 5V supply. Therefore, when the inputs are turned off, the entire circuit is powered down and the 5V supply current drops below 1µA.

XOR Input Circuitry

By employing an XOR function, which locks out the 3.3V switch when the 5V switch is turned on and locks out the 5V switch when the 3.3V switch is turned on, there is no danger of both switches being on at the same time. This XOR function also makes it possible to work with either active-low or active-high PCMCIA V_{CC} switch control logic (see Applications Information section for further details).

Break-Before-Make Switch Control

Built-in delays are provided to ensure that the 3.3V and 5V switches are non-overlapping. Further, the gate charge pump includes circuitry which ramps the NMOS switches on slowly (400µs typical rise time) but turns them off much more quickly (typically 10µs).

Bias, Oscillator and Gate Charge Pump

When either the 3.3V or 5V switch is enabled, a bias current generator and high frequency oscillator are turned on. The on-chip capacitive charge pump generates approximately 12V of gate drive for the internal low $R_{DS(ON)}$ NMOS V_{CC} switches from the $5V_{IN}$ power supply. Therefore, an external 12V supply is not required to switch the V_{CC} output. The $5V_{IN}$ supply current drops below 1µA when both switches are turned off.

Gate Charge and Discharge Control

All switches are designed to ramp on slowly (400µs typical rise time). Turn-off time is much quicker (typically 10µs). To ensure that both V_{CC} NMOS switch gates are fully discharged, program the switch to the high impedance mode at least 100µs before turning off the 5V power supply.

Switch Protection

Both switches are protected against accidental short circuits with SafeSlot foldback current limit circuits which limit the output current to typically 1A when the output is shorted to ground. Both switches also have thermal shutdown which limits the power dissipation to safe levels.

APPLICATIONS INFORMATION

The LTC1470/LTC1471 are designed to interface directly with industry standard PCMCIA card controllers.

Interfacing with the CL-PD6710

Figure 1 is a schematic diagram showing the LTC1470 interfaced with a standard PCMCIA slot controller. The LTC1470 accepts logic control directly from the CL-PD6710.

The XOR input function allows the LTC1470 to interface directly to the active-low V_{CC} control outputs of the CL-PD6710 for 3.3V/5V voltage selection (see the following Switch Truth Table). Therefore, no "glue" logic is required to interface to this PCMCIA compatible card controller.

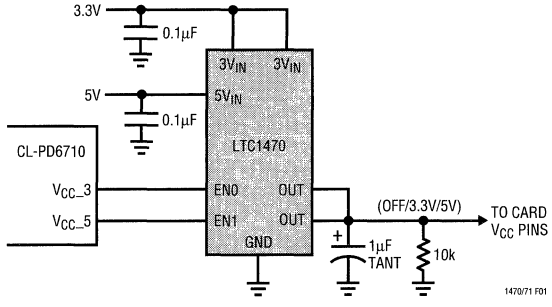


Figure 1. Direct Interface to CL-PD6710 PCMCIA Controller

APPLICATIONS INFORMATION

Truth Table for CL-PD6710 Controller

A_V_{CC}_3	A_V_{CC}_5	
EN0	EN1	OUT
0	0	Hi-Z
0	1	3.3V
1	0	5V
1	1	Hi-Z

Interfacing with "365" Type Controllers

The LTC1470 also interfaces directly with "365" type controllers as shown in Figure 2. Note that the V_{CC} Enable inputs are connected differently than to the CL-PD6710 controller because the "365" type controllers use active-high logic control of the V_{CC} switches (see the following Switch Truth Table). No "glue" logic is required to interface to this type of PCMCIA compatible controller.

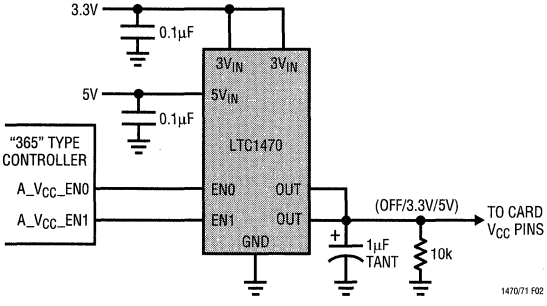


Figure 2. Direct Interface with "365" Type PCMCIA Controller

Truth Table for "365" Type Controller

A_V_{CC}_EN0	A_V_{CC}_EN1	
EN0	EN1	OUT
0	0	Hi-Z
0	1	3.3V
1	0	5V
1	1	Hi-Z

Supply Bypassing

For best results bypass the supply input pins with 1µF capacitors as close as possible to the LTC1470. Sometimes much larger capacitors are already available at the outputs of the 3.3V and 5V power supply. In this case it is still good practice to use 0.1µF capacitors as close as possible to the device, especially if the power supply output capacitors are more than 2" away on the printed circuit board.

Output Capacitors and Pull-Down Resistor

The output pin is designed to ramp on slowly, typically 400µs rise time. Therefore, capacitors as large as 150µF can be driven without producing voltage spikes on the $3V_{IN}$ or $5V_{IN}$ supply pins (see graphs in Typical Performance Characteristics section). The output pin should have a 0.1µF to 1µF capacitor for noise reduction and smoothing.

A 10k pull-down resistor is recommended at the output to ensure that the output capacitor is fully discharged when the output is switched OFF. This resistor also ensures that the output is discharged between the 3.3V and 5V transition.

Supply Sequencing

Because the 5V supply is the source of power for both of the switch control circuits, it is best to sequence the power supplies such that the 5V supply is powered before, or simultaneous to, the application of 3.3V.

It is interesting to note, however, that the switches are NMOS transistors which require charge pumps to generate gate voltages higher than the supply rails for full enhancement. Because the gate voltages start at 0V when the supplies are first activated, the switches always start in the off state and do not produce glitches at the outputs when powered.

If the 5V supply must be turned off, it is important to program all switches to the Hi-Z or 0V state at least 100µs before the 5V power is removed to ensure that the NMOS switch gates are fully discharged to 0V. Whenever possible, however, it is best to leave the $5V_{IN}$ pin(s) continuously powered. The LTC1470/LTC1471 quiescent current drops to <1µA with all the switches turned off and therefore no 5V power is consumed in the standby mode.

APPLICATIONS INFORMATION

TOTAL SYSTEM COST CONSIDERATIONS

The cost of an additional step-up switching regulator, inductor, rectifier and capacitors to produce 12V for VPP can be eliminated by using an auxiliary winding on either the 3.3V or 5V output of the system switching regulator to produce an auxiliary 15V supply for VPP power.

And, because the LTC1470/LTC1471 do not require 12V power to operate (only 5V), the 12V VPP regulation and switching may be operated separately from the 3.3V/5V V_{CC} switching. This increases system configuration flexibility and *reduces total system cost* by eliminating the need for a third regulator for 12V power.

LTC1142HV Auxiliary Winding Power Supply

Figure 3 is a schematic diagram which describes how a loosely regulated 15V power supply is created by adding an auxiliary winding to the 5V inductor in a split 3.3V/5V LTC1142HV power supply system. An LT1313, dual VPP regulator/driver with SafeSlot protection, produces "clean" 3.3V, 5V and 12V power from this loosely regulated 15V output for the PC card slot VPP pins. (See LT1312 and LT1313 data sheets for further detail.)

A turns ratio of 1:1.8 is used for transformer T1 to ensure that the input voltage to the LT1313 falls between 13V and 20V under all load conditions. The 9V output from this additional

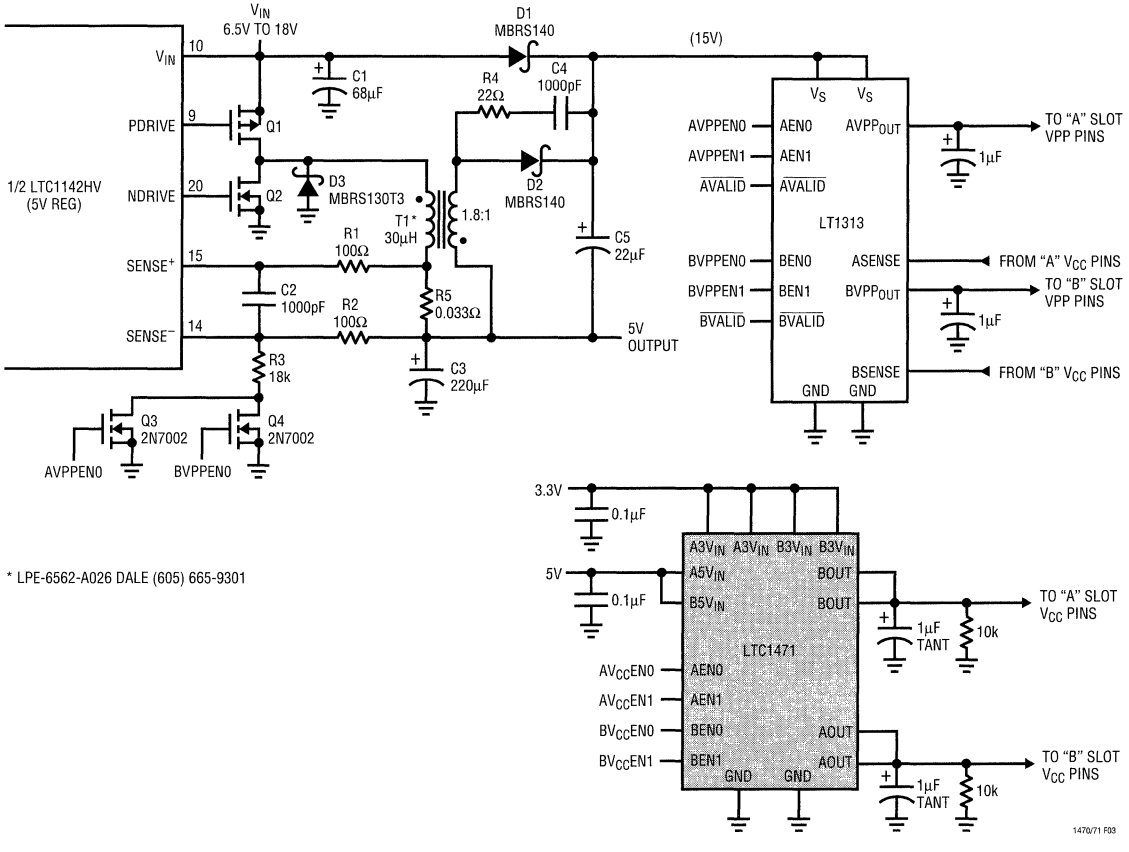


Figure 3. Cost Effective Complete SafeSlot Dual PCMCIA Power Management System (with 15V Auxiliary Supply from LTC1142HV 5V Regulator Inductor)

APPLICATIONS INFORMATION

winding is rectified by diode D2, added to the main 5V output and applied to the input of the LT1313. (Note that the auxiliary winding must be phased properly as shown in Figure 3.)

When the 12V output is activated by a TTL high on either VPP enable lines, the 5V section of the LTC1142HV is forced into continuous mode operation. A resistor divider composed of R2, R3 and switch Q3 forces an offset which is subtracted from the internal offset at the Sense⁻ input (pin 14) of the LTC1142HV. When this external offset cancels the built-in 25mV offset, Burst Mode™ operation is inhibited and the LTC1142HV is forced into continuous mode operation. (See LTC1142HV data sheet for further detail.) In this mode, the 15V auxiliary supply can be loaded without regard to the loading on the 5V output of the LTC1142HV.

Continuous mode operation is only invoked when the LT1313 is programmed to 12V. If the LT1313 is programmed to 0V, 3.3V or 5V, power is obtained directly from the main power source (battery pack) through diode D1. Again, the LT1313 output can be loaded without regard to the loading of the main 5V output.

R4 and C4 absorb transient voltage spikes associated with the leakage inductance inherent in T1's secondary winding and ensure that the auxiliary supply does not exceed 20V.

Auxiliary Power from the LTC1142 3.3V Output

For low-battery count applications (<6.5V) it is necessary to modify the circuit of Figure 3. As the input voltage falls, the 5V duty cycle increases to the point where there is simply not enough time to transfer energy from the 5V primary winding to the auxiliary winding. For applications where 12V load currents exist in conjunction with these low input voltages, use the circuit shown in Figure 4. In this circuit, the auxiliary 15V supply is generated from an overwinding on the 3.3V inductor of the LTC1142 regulator output.

In Figure 3, power is drawn directly from the batteries through D1 when the regulator is in Burst Mode operation and the VPP pins require 3.3V or 5V. In this circuit, however, Q3 and Q4 force the LTC1142 3.3V regulator into continuous mode operation whenever 3.3V, 5V or 12V is programmed at the VPP_{OUT} pins of the LT1313. (See the LT1312 and LT1313 data sheets for further detail.)

Burst Mode is a trademark of Linear Technology Corporation.

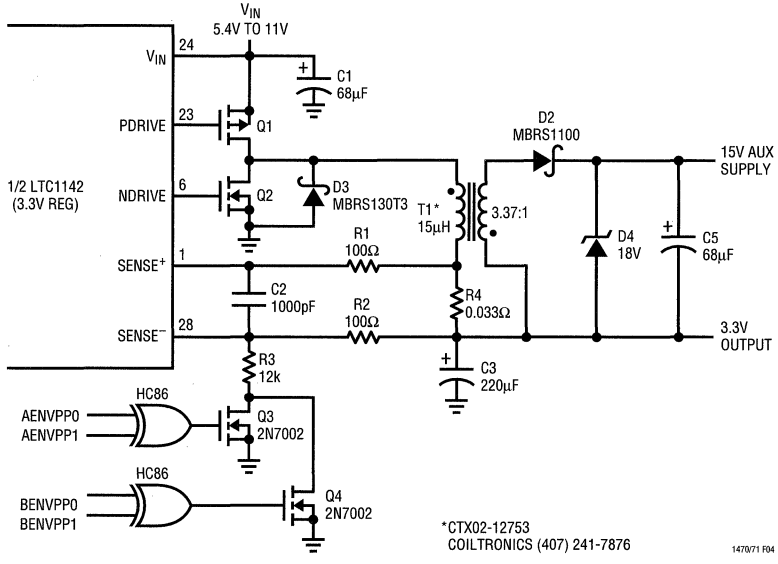
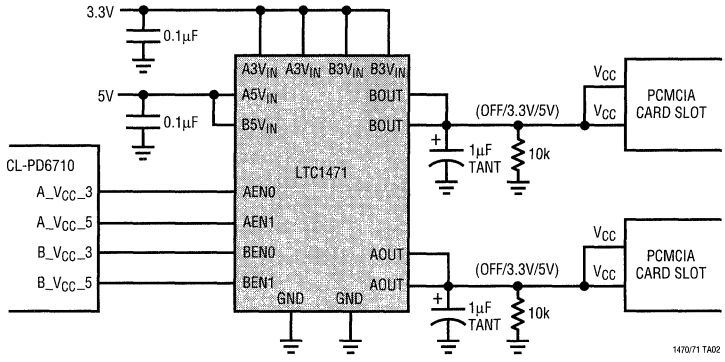


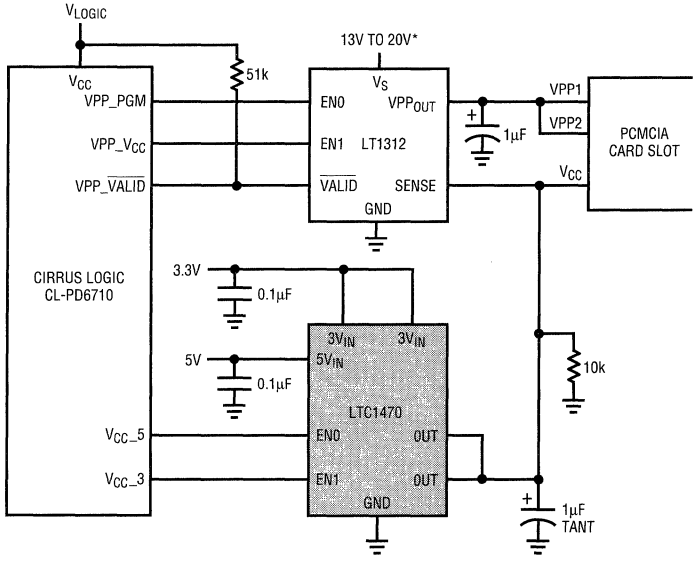
Figure 4. Deriving 15V from the 3.3V Output of the LTC1142 for VPP Power

TYPICAL APPLICATIONS

Dual Slot 3.3V/5V PCMCIA Controller with SafeSlot Current Limit (Systems with No 12V Power Requirements)



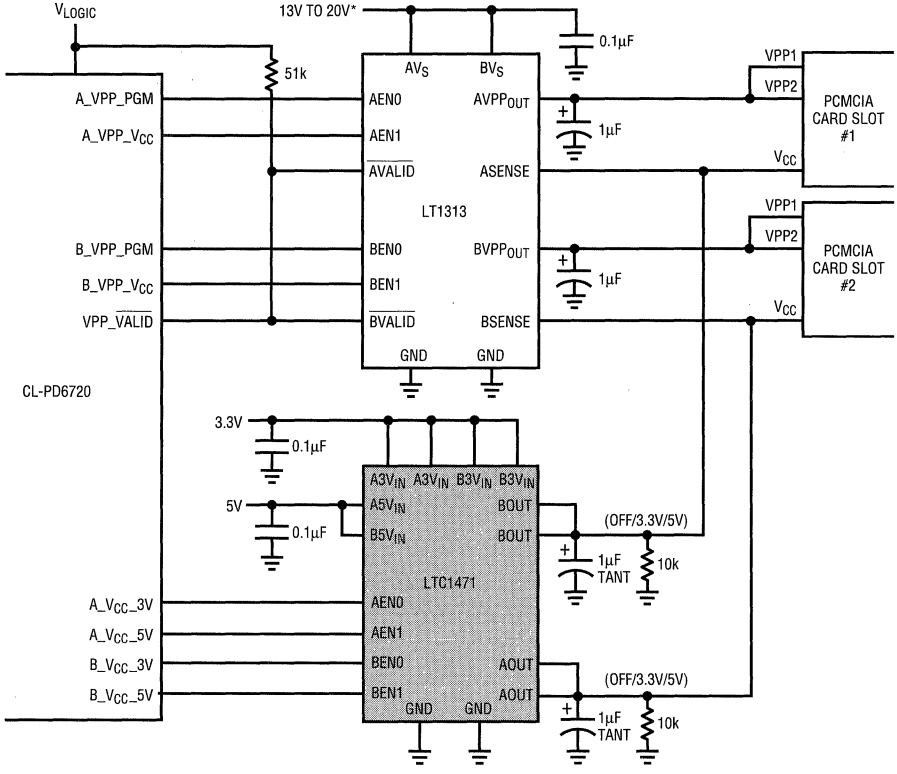
Single Slot PCMCIA Controller with SafeSlot Current Limit Protection Using LT1312 Single VPP Regulator/Driver



* FROM OVERWINDING ON 3.3V OR 5V INDUCTOR IN SYSTEM POWER SUPPLY. SEE FIGURES 3, 4 FOR FURTHER DETAIL

TYPICAL APPLICATIONS

Dual Slot PCMCIA Controller with SafeSlot Current Limit Protection Using LT1313 Dual VPP Regulator/Driver



* FROM OVERWINDING ON 3.3V OR 5V INDUCTOR IN SYSTEM POWER SUPPLY. SEE FIGURES 3, 4 FOR FURTHER DETAILS

1470/71 TA04

RELATED PARTS

See PCMCIA Product Family table on the first page of this data sheet.

Protected PCMCIA V_{CC} and VPP Switching Matrix

FEATURES

- **Both V_{CC} and VPP Switching in a Single Package**
- **Built-In Current Limit and Thermal Shutdown**
- **16-Pin (Narrow) SOIC Package**
- Inrush Current Limited (Drives 150µF Loads)
- Continuous 12V Power Not Required
- Extremely Low $R_{DS(ON)}$ NMOS Switches
- Guaranteed 1A V_{CC} Current and 120mA VPP Current
- 1µA Quiescent Current in Standby
- No External Components Required
- Compatible with Industry Standard Controllers
- Break-Before-Make Switching
- Controlled Rise and Fall Times

APPLICATIONS

- Notebook Computers
- Palmtop Computers
- Pen-Based Computers
- Handi-Terminals
- Bar-Code Readers

DESCRIPTION

The LTC®1472 switching matrix routes power to both the V_{CC} and VPP power supply pins of the PCMCIA compatible card socket. The V_{CC} output of the LTC1472 is switched between three operating states: OFF, 3.3V, and 5V. The VPP output is switched between four operating states: 0V, V_{CC}, 12V, and Hi-Z. The output voltages are selected by two sets of digital inputs which are compatible with industry standard PC Card controllers (see Truth Tables).

The V_{CC} output of the LTC1472 can supply up to 1A of current and the VPP output up to 120mA. Both switches have built-in SafeSlot™ current limiting and thermal shutdown to protect the card, socket and power supply against accidental short-circuit conditions.

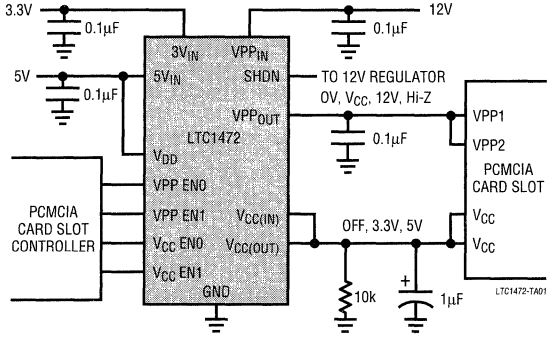
The LTC1472 is designed to conserve power by automatically dropping to 1µA standby current when the two outputs are switched OFF. A shutdown pin is provided which holds the external 12V regulator in standby mode except when required for VPP power.

The LTC1472 is available in 16-pin SO.

4

TYPICAL APPLICATION

Protected PCMCIA V_{CC} and VPP Card Driver



Linear Technology PCMCIA Product Family

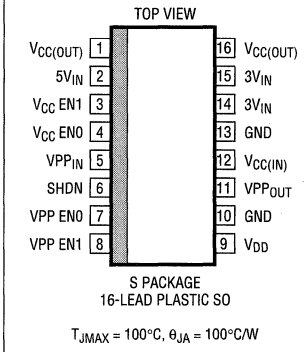
DEVICE	DESCRIPTION	PACKAGE
LT®1312	Single PCMCIA VPP Driver/Regulator	8-Pin SO
LT1313	Dual PCMCIA VPP Driver/Regulator	16-Pin SO*
LTC1314	Single PCMCIA Switch Matrix	14-Pin SO
LTC1315	Dual PCMCIA Switch Matrix	24-Pin SSOP
LTC1470	Protected V_{CC} 5V/3.3V Switch Matrix	8-Pin SO
LTC1471	Dual Protected V_{CC} 5V/3.3V Switch Matrix	16-Pin SO*
LTC1472	Protected V_{CC} and VPP Switch Matrix	16-Pin SO*

*Narrow Body

ABSOLUTE MAXIMUM RATINGS

$5V_{IN}$ Supply Voltage ..... −0.3V to 7V
$3V_{IN}$ Supply Voltage ..... −0.3V to 7V
VPP_{IN} Supply Voltage ..... −0.3V to 13.2V
$V_{CC(IN)}$ Supply Voltage ..... −0.3 to 7V
$V_{DD(IN)}$ Supply Voltage ..... −0.3V to 7V
VPP_{OUT} (OFF) ..... −0.3V to 13.2V
$V_{CC(OUT)}$ (OFF) ..... −0.3V to 7V
Enable Inputs ..... −0.3V to 7V
VPP_{OUT} Short-Circuit Duration ..... Indefinite
$V_{CC(OUT)}$ Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Junction Temperature ..... 100°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC1472CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS (V_{CC} Switch Section)

$5V_{IN}$ = 5V, $3V_{IN}$ = 3.3V, VPP EN0 = VPP EN1 = 0V, T_A = 25°C, (Note 1) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$5V_{IN}$	$5V_{IN}$ Supply Voltage Range	(Note 2)		4.75		5.25	V
$3V_{IN}$	$3V_{IN}$ Supply Voltage Range	(Note 3)		0		3.60	V
I_{5VIN}	$5V_{IN}$ Supply Current	Program to Hi-Z	●		0.01	10	µA
		Program to 5V, No Load	●		140	200	µA
		Program to 3.3V, No Load	●		100	160	µA
I_{3VIN}	$3V_{IN}$ Supply Current	Program to Hi-Z.	●		0.01	10	µA
		Program to 5V, No Load	●		0.01	10	µA
		Program to 3.3V, No Load	●		40	80	µA
R_{ON}	5V Switch On Resistance	Program to 5V, I_{OUT} = 500mA			0.14	0.18	Ω
	3.3V Switch On Resistance	Program to 3.3V, I_{OUT} = 500mA			0.12	0.16	Ω
I_{LKG}	Output Leakage Current OFF	V_{CC} EN0 = V_{CC} EN1 = 0V or 5V, 0V ≤ $V_{CC(OUT)}$ ≤ 5V	●			±10	µA
I_{LIM5V}	$V_{CC(OUT)}$ 5V Current Limit	Program to 5V, $V_{CC(OUT)}$ = 0V (Note 4)			1		A
I_{LIM3V}	$V_{CC(OUT)}$ 3.3V Current Limit	Program to 3.3V, $V_{CC(OUT)}$ = 0V (Note 4)			1		A
V_{CCENH}	V_{CC} Enable Input High Voltage		●	2			V
V_{CCENL}	V_{CC} Enable Input Low Voltage		●			0.8	V
I_{VCCEN}	V_{CC} Enable Input Current	0V ≤ V_{CCEN} ≤ 5V	●			±1	µA
t_{VCC1}	Delay + Rise Time	From 0V to 3.3V, R_{LOAD} = 100Ω, C_{LOAD} = 1µF (Note 5)		0.2	0.32	1	ms
t_{VCC2}	Delay + Rise Time	From 3.3V to 5V, R_{LOAD} = 100Ω, C_{LOAD} = 1µF (Note 5)		0.2	0.52	1	ms
t_{VCC3}	Delay + Rise Time	From 0V to 5V, R_{LOAD} = 100Ω, C_{LOAD} = 1µF (Note 5)		0.2	0.38	1	ms

ELECTRICAL CHARACTERISTICS (VPP Switch Section)

V_{DD} = 5V, $V_{CC(IN)}$ = 5V, VPP_{IN} = 12V, V_{CCEN0} = V_{CCEN1} = 0V, T_A= 25°C, (Note 1), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CC(IN)}$	V_{CC} Input Voltage Range		●	3		5.5	V
VPP_{IN}	VPP Input Voltage Range	(Note 6)	●	0		12.6	V
V_{DD}	Logic Supply Voltage Range	(Note 7)	●	4.5		5.5	V
I_{CCIN}	$V_{CC(IN)}$ Supply Current, No Load	Program to VPP_{IN} or $V_{CC(IN)}$ VPP_{IN} = 12V Program to 0V or Hi-Z	● ●		35 0.01	60 10	µA µA
I_{PPIN}	VPP_{IN} Supply Current, No Load	Program to VPP_{IN} or $V_{CC(IN)}$ Program to 0V or Hi-Z	● ●		40 0.01	80 10	µA µA
I_{DD}	V_{DD} Supply Current, No Load	Program to VPP_{IN} Program to $V_{CC(IN)}$, VPP_{IN} = 0V Program to $V_{CC(IN)}$, VPP_{IN} = 12V Program to 0V or Hi-Z	● ● ● ●		70 85 40 0.01	120 150 80 10	µA µA µA µA
I_{VPPOUT}	Hi-Z Output Leakage Current	Program to Hi-Z, 0V < VPP_{OUT} < 12V	●		0.01	10	µA
R_{ON}	On Resistance VPP_{OUT} to VPP_{IN} On Resistance VPP_{OUT} to $V_{CC(IN)}$ On Resistance VPP_{OUT} to GND	VPP_{IN} = 12V, I_{LOAD} = 120mA $V_{CC(IN)}$ = 5V, I_{LOAD} = 5mA V_{DD} = 5V, I_{SINK} = 1mA			0.50 1.70 100	1 5 250	Ω Ω Ω
VPP_{ENH}	VPP Enable Input High Voltage	V_{DD} = 5V	●	2			V
VPP_{ENL}	VPP Enable Input Low Voltage	V_{DD} = 5V	●			0.8	V
I_{VPPEN}	VPP Enable Input Current	0V < VPP EN < VDD	●			±1	µA
V_{SDH}	SHDN Output High Voltage	Program to 0V, $V_{CC(IN)}$ or Hi-Z, I_{LOAD} = 400µA	●	3.5			V
V_{SDL}	SHDN Output Low Voltage	Program to VPP_{IN}, I_{SINK} = 400µA	●			0.4	V
I_{LIMVCC}	VPP_{OUT} Current Limit, $V_{CC(IN)}$	Program to $V_{CC(IN)}$, VPP_{OUT} = 0V (Note 4)			60		mA
I_{LIMVPP}	VPP_{OUT} Current Limit, VPP_{IN}	Program to VPP_{IN}, VPP_{OUT} = 0V (Note 4)			100		mA
t_{VPP1}	Delay and Rise Time	From 0V to $V_{CC(IN)}$, VPP_{IN} = 0V (Note 8)		5	15	50	µs
t_{VPP2}	Delay and Rise Time	From 0V to VPP_{IN} (Note 8)		25	85	250	µs
t_{VPP3}	Delay and Rise Time	From $V_{CC(IN)}$ to VPP_{IN} (Note 8)		30	100	300	µs
t_{VPP4}	Delay and Fall Time	From VPP_{IN} to $V_{CC(IN)}$ (Note 9)		5	15	50	µs
t_{VPP5}	Delay and Fall Time	From VPP_{IN} to 0V (Note 10)		10	35	100	µs
t_{VPP6}	Delay and Fall Time	From $V_{CC(IN)}$ to 0V, VPP_{IN} = 0V (Note 10)		10	30	100	µs
t_{VPP7}	Output Turn-On Delay	From Hi-Z to $V_{CC(IN)}$ (Note 8)		5	15	50	µs
t_{VPP8}	Output Turn-On Delay	From Hi-Z to VPP_{IN} (Note 8)		25	85	250	µs

The ● denotes the specifications which apply over the full operating temperature range.

Note 1: V_{ENH} = 5V, V_{ENL} = 0V. See V_{CC} and VPP Switch Truth Tables for programming enable inputs for desired output states.

Note 2: Power for the V_{CC} input logic and charge pump circuitry is derived from the $5V_{IN}$ power supply which must be continuously powered. 12V and 3.3V power is not required to control the NMOS V_{CC} switches. (See Applications Information.)

Note 3: The two $3V_{IN}$ supply input pins (14 and 15) must be connected together and the two $V_{CC(OUT)}$ output pins (1 and 16) must be connected together. The $3V_{IN}$ supply pins do not need to be continuously powered and may drop to 0V when not required.

Note 4: The V_{CC} and VPP output are protected with foldback current limit which reduces the short-circuit (0V) currents below peak permissible current levels at higher output voltages.

Note 5: To 90% of final value.

Note 6: 12V power is only required when VPP_{OUT} is programmed to 12V. The external 12V regulator can be shutdown at all other times. Built-in charge pumps power the internal NMOS switches from the 5V V_{DD} supply when 12V is not present.

Note 7: Power for the VPP input logic and charge pump circuitry is derived from the V_{DD} power supply which must be continuously powered.

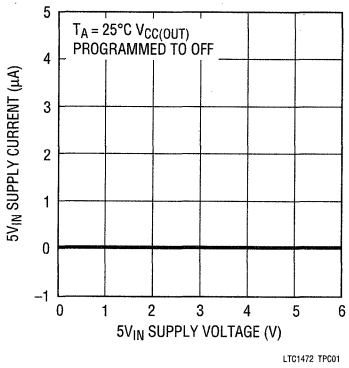
Note 8: To 90% of the final value, C_{OUT} = 0.1µF, R_{OUT} = 2.9k.

Note 9: To 10% of the final value, C_{OUT} = 0.1µF, R_{OUT} = 2.9k.

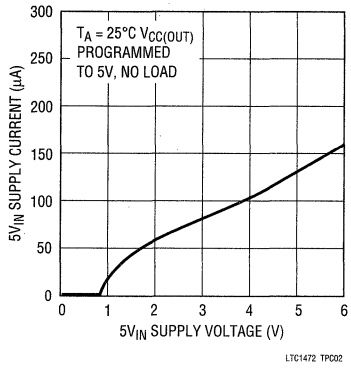
Note 10: To 50% of the initial value, C_{OUT} = 0.1µF, R_{OUT} = 2.9k.

TYPICAL PERFORMANCE CHARACTERISTICS (V_{CC} Section) VPP EN0 = VPP EN1 = 0V

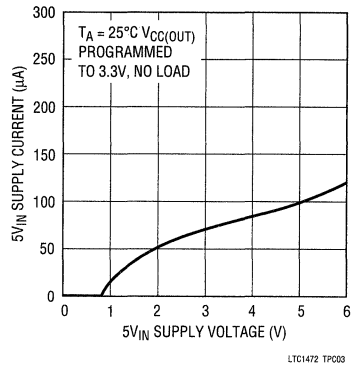
$5V_{IN}$ Supply Current (OFF)



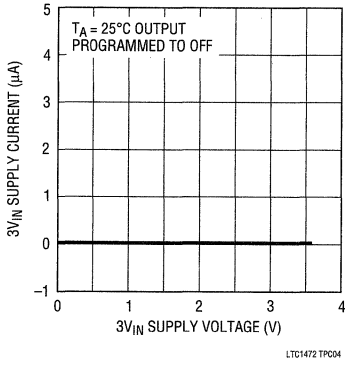
$5V_{IN}$ Supply Current (5V ON)



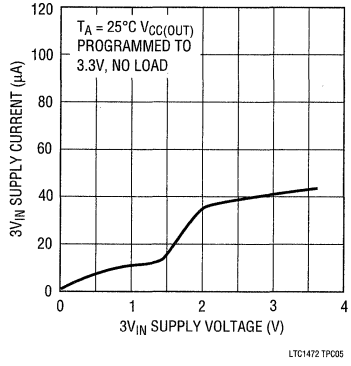
$5V_{IN}$ Supply Current (3.3V ON)



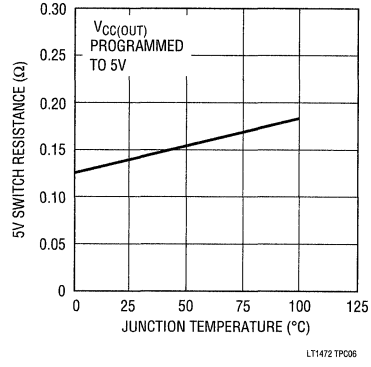
$3V_{IN}$ Supply Current (OFF)



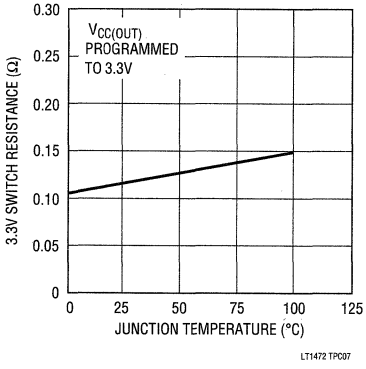
$3V_{IN}$ Supply Current (3.3V ON)



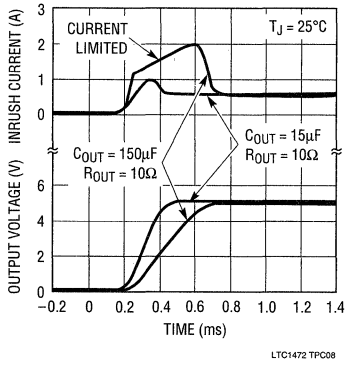
5V Switch Resistance



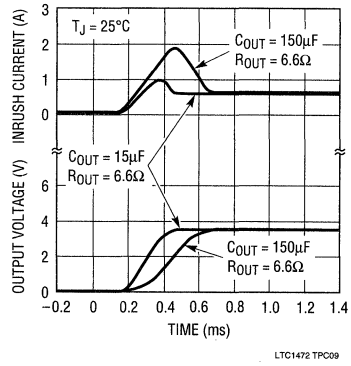
3.3V Switch Resistance



Inrush Current (5V Switch)

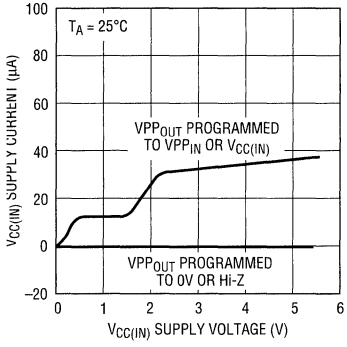


Inrush Current (3.3V Switch)



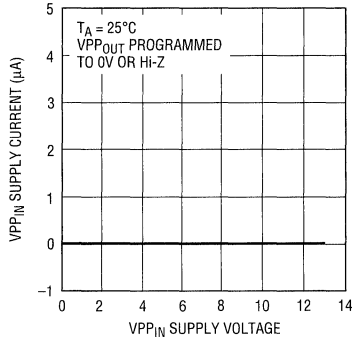
TYPICAL PERFORMANCE CHARACTERISTICS (VPP Section) V_{CC} EN0 = V_{CC} EN1 = 0V

$V_{CC(IN)}$ Supply Current (No Load)



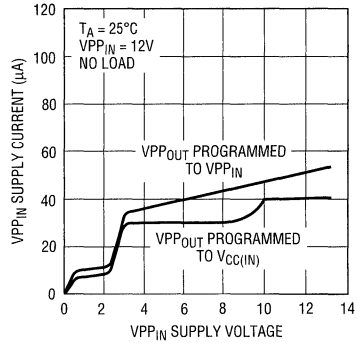
LTC1472 TPC10

VPP_{IN} Supply Current (OFF)



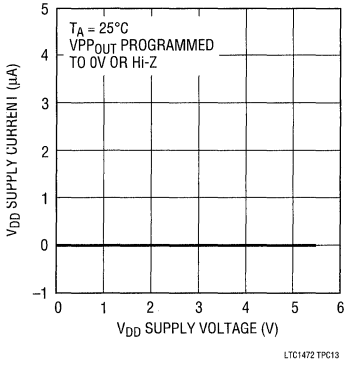
LTC1472 TPC11

VPP_{IN} Supply Current (No Load)



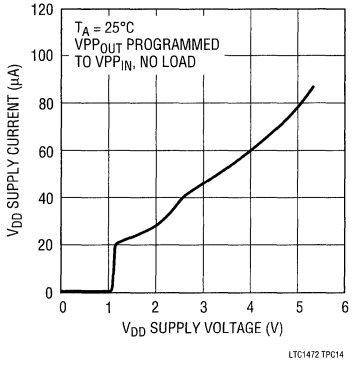
LTC1472 TPC12

V_{DD} Supply Current (OFF)



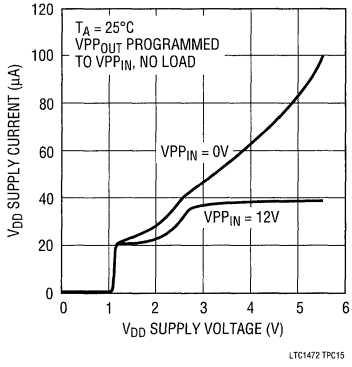
LTC1472 TPC13

V_{DD} Supply Current (No Load)



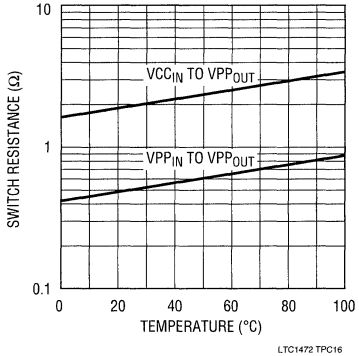
LTC1472 TPC14

V_{DD} Supply Current (ON)



LTC1472 TPC15

Switch Resistances



LTC1472 TPC16

4

PIN FUNCTIONS

Enable Input (Pins 3,4,7,8)

The two V_{CC} and two VPP Enable inputs are designed to interface directly with industry standard PCMCIA controllers. They are high impedance CMOS gates with ESD protection diodes to ground, and should not be forced below ground. Both sets of inputs have about 100mV of built-in hysteresis to ensure clean switching between operating modes.

Shutdown Output (Pin 6)

The LTC1472 is designed to operate *without* continuous 12V power. The gates of the V_{CC} NMOS switches are powered by charge pumps from the $5V_{IN}$ supply, and the gates of the VPP NMOS switches are powered by charge pumps powered from the V_{DD} supply when 12V is not present at the VPP_{IN} pin (see Application Information for more details). Therefore, the external 12V regulator can be shut down most of the time, and only turned on when programming the socket VPP pin to 12V.

The shutdown output is active high; i.e. the system 12V regulator is shut down when this output is held high and turned on when this output is held low.

VPP_{IN} Supply (Pin 5)

The VPP_{IN} supply pin serves two purposes. The first purpose is to provide power and gate drive for the VPP_{IN}-VPP_{OUT} switch. The second purpose is to provide optional 12V gate drive for the $V_{CC(IN)}$-VPP_{OUT} switch. If, however, this 12V power is not available, gate drive is obtained automatically from the 5V V_{DD} supply by an internal 5V to 12V charge pump converter.

V_{DD} Supply (Pin 9)

The V_{DD} pin provides power for the input, charge pump and control circuitry for the VPP section of the LTC1472 and therefore must be continuously powered. The standby quiescent current is typically 0.1µA when the VPP_{OUT} pin is programmed to 0V or Hi-Z and only rises to micropower levels when the VPP switches are active.

$V_{CC(IN)}$ Supply (Pin 12)

The $V_{CC(IN)}$ supply pin is typically connected directly to the $V_{CC(OUT)}$ pin from the V_{CC} switch section of the LTC1472. It can also be connected directly to a 3.3V or 5V power supply if desired. This supply pin does not provide any power to the internal control circuitry and is simply the input to the $V_{CC(IN)}$-VPP_{OUT} switch and therefore does not consume any power when unloaded or turned off.

$5V_{IN}$ Supply (Pin 2)

The $5V_{IN}$ supply pin serves two purposes. The first purpose is as the power supply input for the 5V NMOS switch. The second purpose is to provide power for the input, gate drive and protection circuitry for both the 3.3V and 5V V_{CC} switches, *this pin must be continuously powered.*

The enable inputs should be turned off (both asserted high or both asserted low) at least 100µs before the $5V_{IN}$ power is removed to ensure that both V_{CC} NMOS switch gates are fully discharged and both switches are in the high impedance mode.

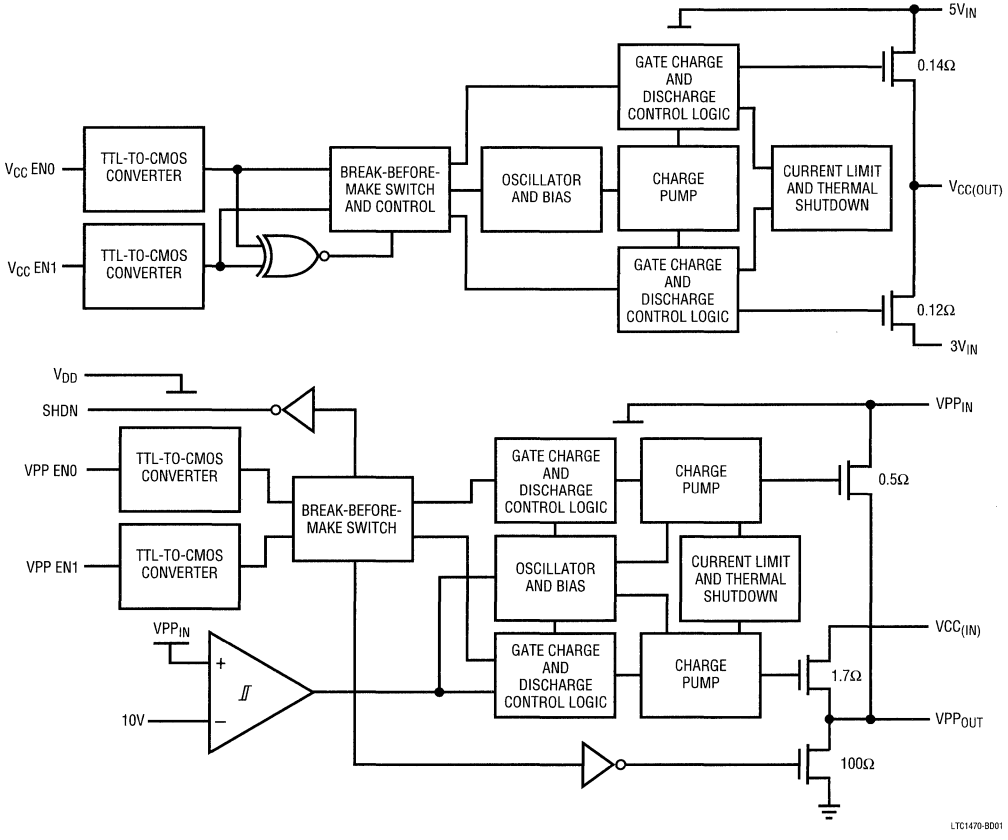
$3V_{IN}$ Supply (Pins 14,15)

The $3V_{IN}$ supply pin serves as the power supply input for the 3.3V switch. This pin does not provide any power to the internal control circuitry and therefore does not consume any power when unloaded or turned off.

$V_{CC(OUT)}$ and VPP_{OUT} Output (Pins 1,11,16)

The V_{CC} output of the LTC1472 is switched between the three operating states: OFF, 3.3V, and 5V. The VPP output is switched between four operating states: 0, V_{CC}, 12V and Hi-Z. Both pins are protected against accidental short-circuit conditions to ground by independent SafeSlot foldback current-limit circuitry which protects the socket, card and the system power supplies against damage. A second level of protection is provided by independent thermal shut down circuitry which protects each switch against overtemperature conditions.

BLOCK DIAGRAM



OPERATION

The LTC1472 protected switch matrix is designed to be a complete single slot solution for V_{CC} and VPP switching in a PCMCIA compatible card system. The LTC1472 consists of two independent functional sections: the V_{CC} switching section, and the VPP switching section.

THE V_{CC} SWITCHING SECTION

The V_{CC} switching section of the LTC1472 consist of the following functional blocks:

V_{CC} Switch Input TTL-CMOS Converters

The LTC1472 V_{CC} inputs are designed to accommodate a wide range of 3V and 5V logic families. The input threshold voltage is approximately 1.4V with approximately 100mV of hysteresis. The inputs enable the bias generator, the gate charge pumps and the protection circuity which are powered from the $5V_{IN}$ supply. Therefore, when the inputs are turned off, the entire circuit is powered down and the $5V_{IN}$ supply current drops below 1μA.

OPERATION

V_{CC} XOR Input Circuitry

The LTC1472 ensures that the 3.3V and 5V switches are never turned on at the same time by employing an XOR function which locks out the 3.3V switch when the 5V switch is turned on, and locks out the 5V switch when the 3.3V switch is turned on. This XOR function also makes it possible for the LTC1472 to work with either active-low or active-high PCMCIA V_{CC} switch control logic (see Applications Information for further details).

V_{CC} Break-Before-Make Switch Control

The LTC1472 has built-in delays to ensure that the 3.3V and 5V switch are non-overlapping. Further, the gate charge pumps include circuity which ramps the NMOS switches on slowly (400µs typical rise time) but turn off much more quickly (typically 10µs).

V_{CC} Bias, Oscillator and Gate Charge Pump

When either the 3.3V or 5V switch is enabled, a bias current generator and high frequency oscillator are turned on. An on-chip capacitive charge pump generates approximately 12V of gate drive for the internal low $R_{DS(ON)}$ NMOS V_{CC} switches from the $5V_{IN}$ power supply. Therefore, an external 12V supply is not required to switch the V_{CC} output. The $5V_{IN}$ supply current drops below 1µA when both switches are turned off.

V_{CC} Gate Charge and Discharge Control

Both V_{CC} switches are designed to ramp on slowly (400µs typical rise time). Turn off time is much quicker (typically 10µs).

To ensure that both V_{CC} NMOS switch gates are fully discharged, program the switch to the high impedance mode at least 100µs before turning off the $5V_{IN}$ power supply.

V_{CC} Switch Protection

Two levels of protection are designed into each of the power switches in the LTC1472. Both V_{CC} switches are protected against accidental short circuits with SafeSlot fold-back current limit circuits which limit the output current to typically 1A when the $V_{CC(OUT)}$ output is shorted to ground. Both switches also have independent thermal shutdown which limits the power dissipation to safe levels.

V_{CC} Switch Truth Table

V_{CC} EN0	V_{CC} EN1	$V_{CC(OUT)}$
0	0	OFF
1	0	5V
0	1	3.3V
1	1	OFF

THE VPP SWITCHING SECTION

The VPP switching section of the LTC1472 consists of the following functional blocks:

VPP Switch Input TTL-CMOS Converters

The VPP inputs are designed to accommodate a wide range of 3V and 5V logic families. The input threshold voltage is 1.4V with ≈ 100mV of hysteresis. The inputs enable the bias generator, the gate charge pumps and the protection circuitry. When the inputs are turned off, the entire circuit is powered down and the V_{DD} and VPP_{IN} supply currents drop below 1µA.

VPP Break-Before-Make Switch Control

The VPP input section has built-in delays to ensure that the VPP switchs are non-overlapping. Further, the gate charge pumps include circuitry which ramps the NMOS switches on slowly but turns them off quickly.

VPP Bias, Oscillator and Gate Charge Pump

When either the VPP_{IN}-VPP_{OUT} or $V_{CC(IN)}$-VPP_{OUT} switch is enabled, a bias current generator and high frequency oscillator are turned on. An on-chip capacitive charge pump generates approximately 23V of gate drive for the internal low $R_{DS(ON)}$ NMOS VPP_{IN}-VPP_{OUT} switch from the VPP_{IN} power supply. The gate of the $V_{CC(IN)}$-VPP_{OUT} NMOS switch is either powered by the external 12V regulator (if left on) or automatically from a built-in charge pump powered from the V_{DD} supply when the external 12V supply drops below 10V. The V_{DD} supply current drops below 1µA when switched to either the 0V or Hi-Z mode.

OPERATION

VPP Gate Charge and Discharge Control

The VPP switches are designed to ramp slowly (typically tens of µs) between output modes to reduce supply glitching when powering large capacitive loads.

VPP Switch Protection

Both VPP power switches are protected against accidental short circuits with SafeSlot fold-back current limit circuits which limit the short-circuit (0V) output current to typically 100mA when protecting the 12V VPP_{IN} supply and 60mA when protecting the $V_{CC(IN)}$ supply. (Higher operating currents are allowed at higher output voltages). Both switches also have thermal shutdown.

VPP Switch Truth Table

VPP EN0	VPP EN1	VPP_{OUT}
0	0	0V
0	1	$V_{CC(IN)}$
1	0	VPP_{IN}
1	1	Hi-Z

APPLICATIONS INFORMATION

The LTC1472 is a complete single slot V_{CC} and VPP power supply switch matrix with SafeSlot current limit protection on both outputs. It is designed to interface directly with industry standard PCMCIA card controllers and to industry standard 12V regulators.

Interfacing to the CL-PD6710 and the LT®1301

Figure 1 shows the LTC1472 interfaced to a standard PCMCIA slot controller and an LT1301 step-up switching regulator. The LTC1472 accepts logic control directly from the CL-PD6710 and in turn, controls the LT1301 to provide clean 12V VPP programming power when required. The LT1301 is then shutdown (10µA standby current) at all other times to conserve power.

The XOR V_{CC} input function allows the LTC1472 to interface directly to the active-low V_{CC} control outputs of the CL-PD6710 for 3.3V/5V voltage selection (see the V_{CC} Switch Truth Table). Therefore, no "glue" logic is required to interface to this PCMCIA compatible controller.

The LTC1472 provides SafeSlot current-limit protection for the LT1301 step-up regulator, the system 3.3V and 5V regulators, the socket and the card. Further, depending upon the system regulator's own current limits, it may allow the system power supplies to continue operation during a card/slot short circuit without losing data, etc.

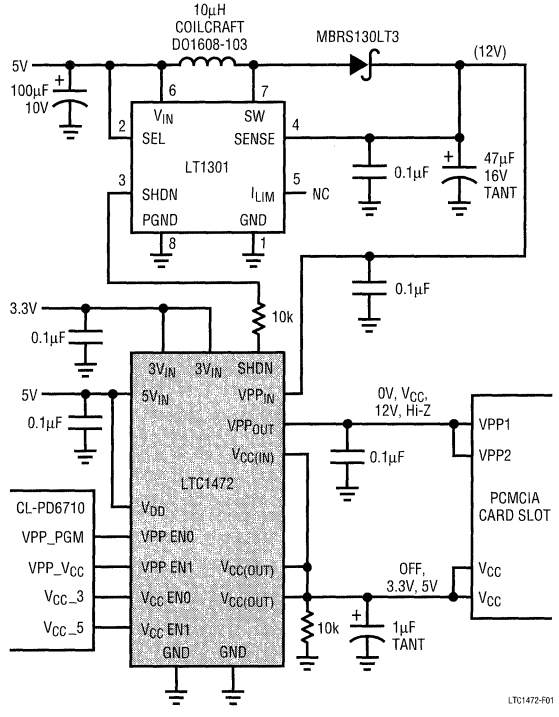


Figure 1. Direct Interface to Industry Standard PCMCIA Controller and LT1301 Step-Up Switching Regulator

APPLICATIONS INFORMATION

Interfacing to "365" Type Controllers

The LTC1472 also interfaces directly with "365" type controllers as shown in Figure 2. The V_{CC} Enable inputs are connected differently than to the CL-PD6710 controller because the "365" type controllers use active-high logic control of the V_{CC} switches (see the V_{CC} Switch Truth Table). No "glue logic" is required to interface to this type of PCMCIA compatible controller.

12V Power Requirements

Note that in Figure 2, a "local" 5V to 12V converter is not used. The LTC1472 works equally well with or without continuous 12V power. If the main power supply system has 12V continuously available, simply connect it to the VPP_{IN} pin. Internal circuitry automatically senses its presence and uses it to switch the internal VPP switches.

The 12V shutdown output can be used to shut down the system 12V power supply (if not required for any purpose other than VPP programming).

5V Power Requirements

The LTC1472 has been designed to operate without continuous 12V power, but continuous 5V power is required at the V_{DD} and $5V_{IN}$ supply pins for proper operation and should always be present when a card is powered (whether it is a 5V or 3.3V only card).

If the 5V power must be turned off, for example, to enter a 3.3V only full system "sleep" mode, the 5V supply must be turned off at least 100µs after the V_{CC} and VPP switches have been programmed to the Hi-Z or 0V states. This ensures that the gates of the NMOS switches are completely discharged.

Also, the V_{CC} switches cannot be operated properly without 5V power. They must be programmed to the off state at least 100µs prior to turning the 5V supply off, or they may be left in an indeterminate state.

Supply Bypassing

For best results, bypass the supply input pins with 1µF capacitors as close as possible to the LTC1472. Sometimes, much larger capacitors are already available at the outputs of the 3.3V, 5V and 12V power supply. In this case, it is still good practice to use 0.1µF capacitors as close as possible to the LTC1472, especially if the power supply output capacitors are more than 2" away on the printed circuit board.

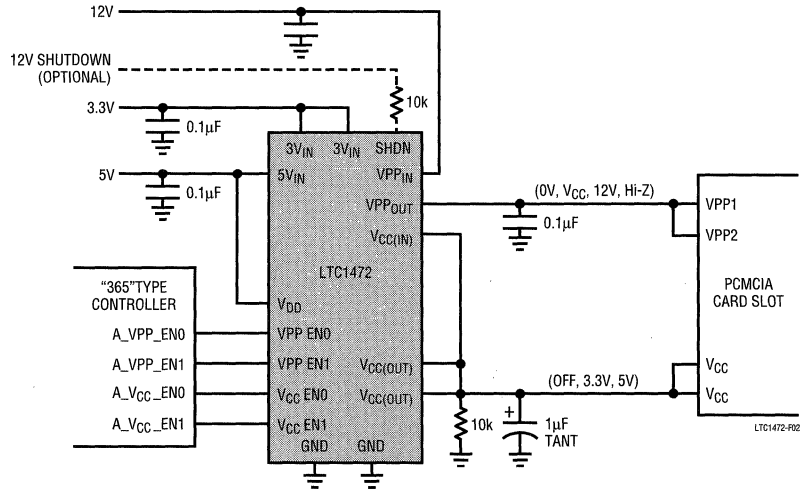


Figure 2. Direct Interface to Industry Standard PCMCIA Controller and LT1301 Step-Up Switching Regulator

APPLICATIONS INFORMATION

Output Capacitors

The $V_{CC(OUT)}$ pin is designed to ramp on slowly, typically 100µs rise time. Therefore, capacitors as large as 150µF can be driven without producing voltage spikes on the $5V_{IN}$ or $3V_{IN}$ supply pins (see graphs in Typical Performance Characteristics). The $V_{CC(OUT)}$ pin should have a 0.1µF to 1µF capacitor for noise reduction and smoothing.

The VPP_{OUT} pin should have a 0.01µF to 0.1µF capacitor for noise reduction. The VPP_{IN} capacitors should be at least equal to the VPP_{OUT} capacitors to ensure smooth transitions between output voltages without creating spikes on the system power supply lines.

Supply Sequencing

Because the 5V supply is the source of power for both the V_{CC} and VPP switch control logic, it is best to sequence the power supplies such that the 5V supply is powered before or simultaneous to the application of 3.3V or 12V power.

It is interesting to note however, that all of the switches in the LTC1472 are NMOS transistors which require charge pumps to generate gate voltages higher than the supply rails for full enhancement. Because the gate voltages start a 0V when the supplies are first activated, the switches always start in the off state and do not produce glitches at the output when powered.

Some PCMCIA switch matrix products employ PMOS switches for 12V VPP control and great care must be taken to ensure that the 5V control logic is powered before the 12V supply is turned on. If this sequence is not followed, the PMOS VPP switch gate may start at ground potential and the VPP output may be inadvertently forced to 12V.

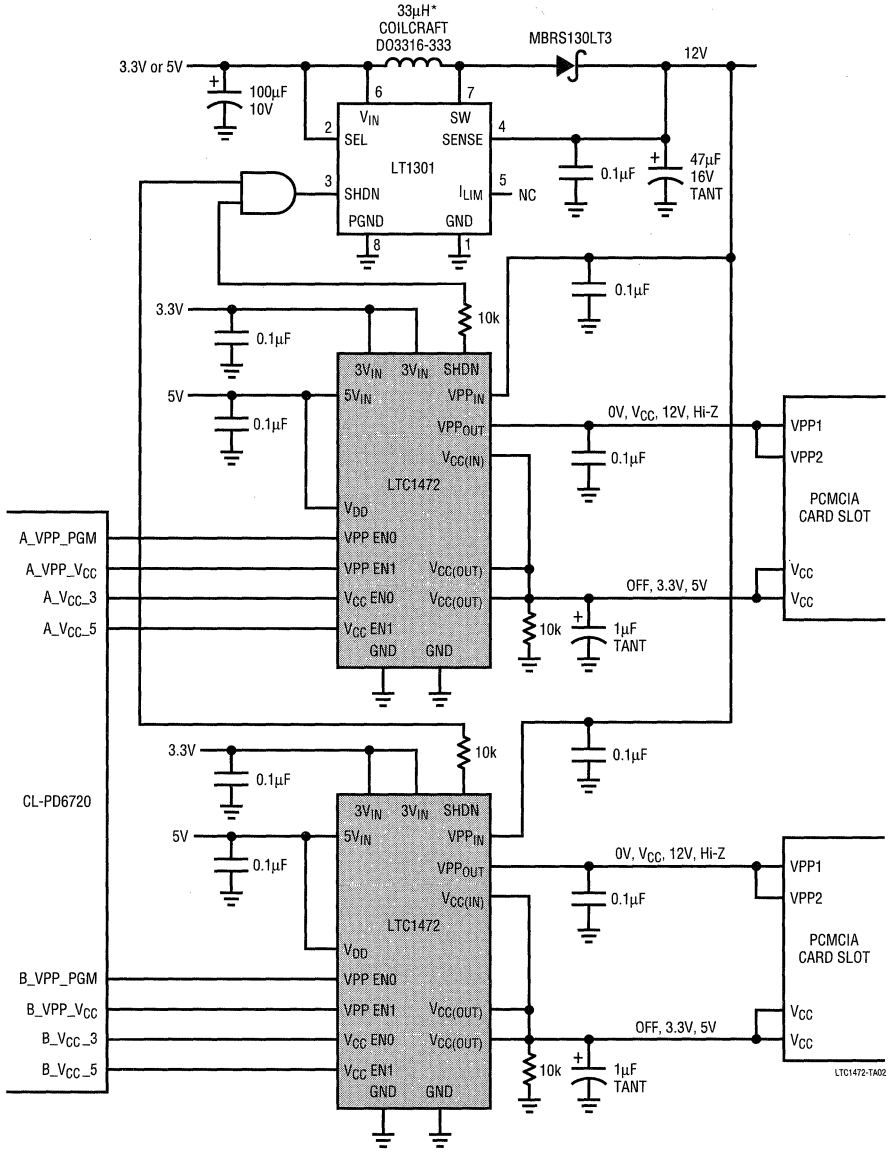
Although, not advisable, it is possible to power the 12V VPP_{IN} supply pin of the LTC1472 prior to application of 5V power. Only about 50µA flows to the VPP_{OUT} pin under these conditions.

If the 5V supply must be turned off, it is important to program all switches to the Hi-Z or 0V state at least 100µs before the 5V power is removed to ensure that all NMOS switch gates are fully discharged to 0V.

Whenever possible however, it is best to leave the $5V_{IN}$ and V_{DD} pins continuously powered. The LTC1472 quiescent current drops to < 1µA with all the switches turned off and therefore no 5V power is consumed in the standby mode.

TYPICAL APPLICATIONS

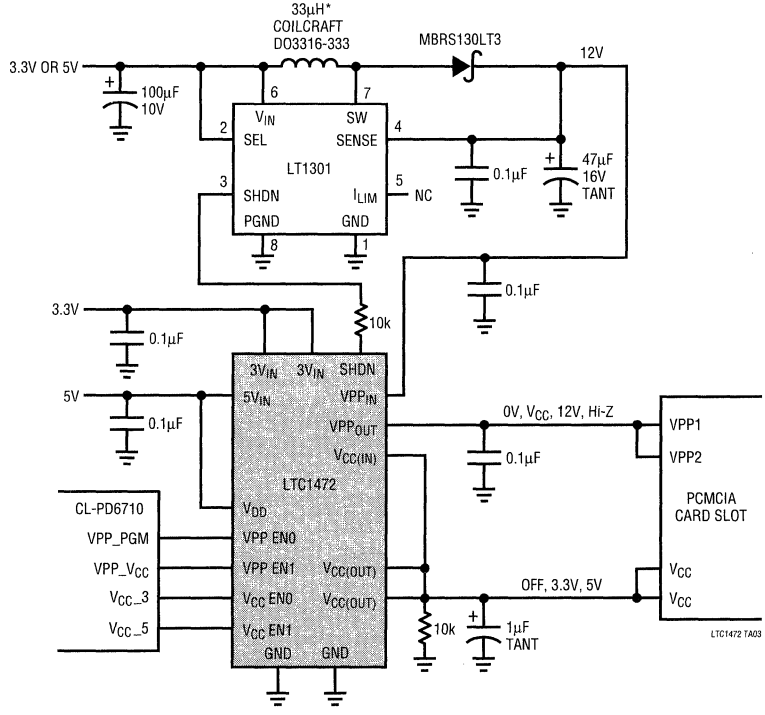
Dual Protected PCMCIA Power Management System



*FOR 5V TO 12V CONVERSION USE 10µH, COILCRAFT DO1608-103. SEE LT1301 DATA SHEET FOR MORE DETAILED INFORMATION ON INDUCTOR AND CAPACITOR SELECTION.

TYPICAL APPLICATIONS

Single Protected PCMCIA Power Management System Using the LT1301 Powered from 3.3V or 5V



*FOR 5V TO 12V CONVERSION USE 10µH, COILCRAFT D01608-103. SEE LT1301 DATA SHEET FOR MORE DETAILED INFORMATION ON INDUCTION AND CAPACITOR SELECTION.

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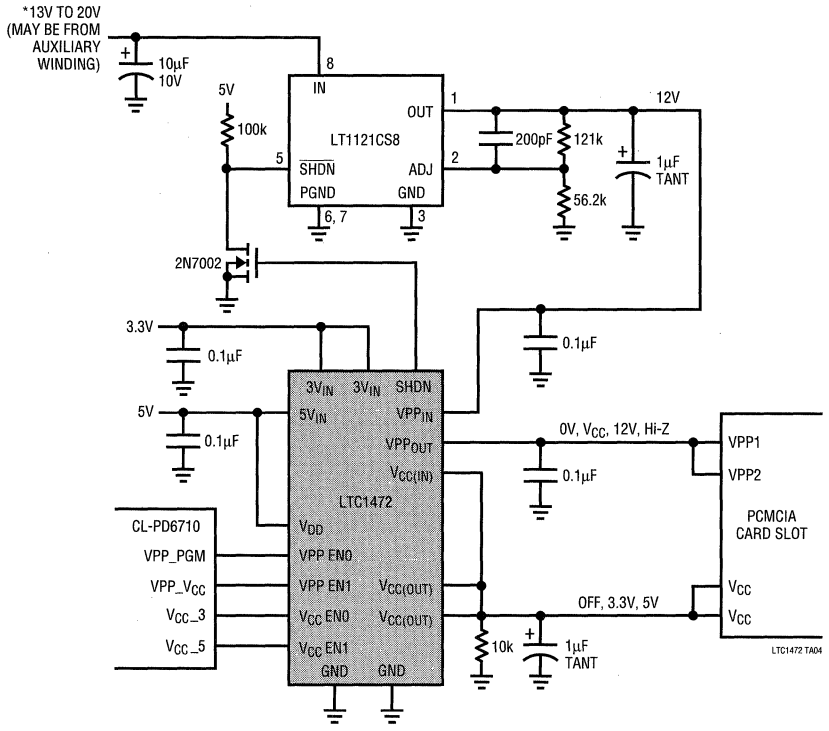
TYPICAL APPLICATIONS

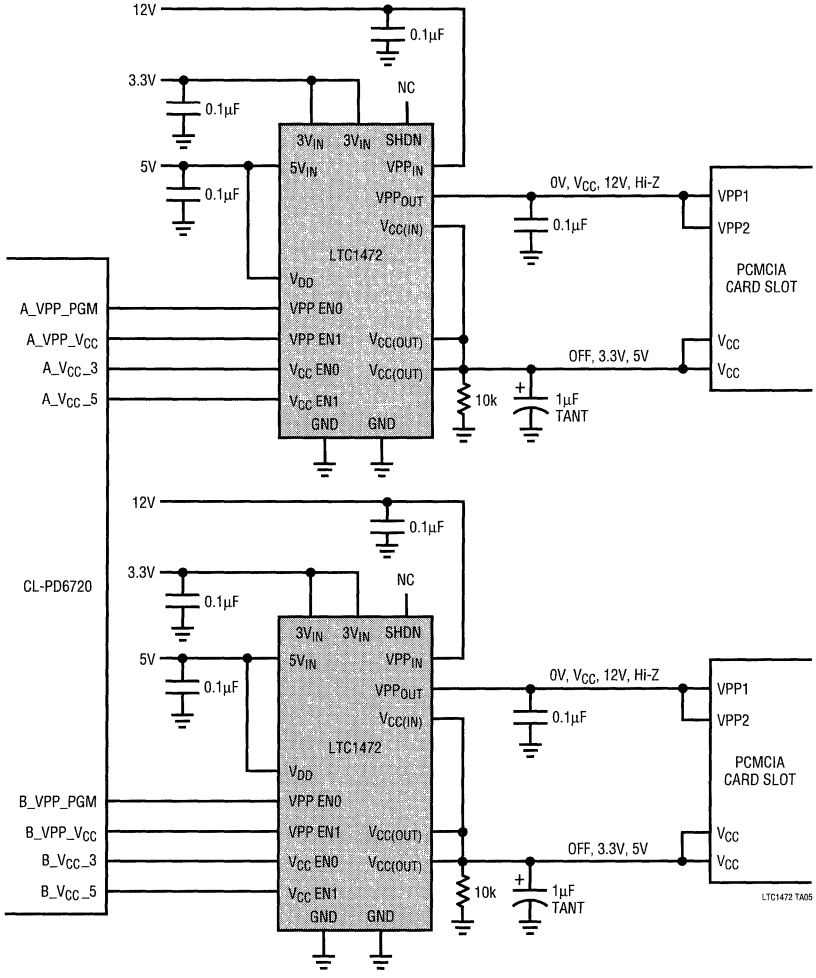
Single Protected PCMCIA Power Management System
Using the LT1121 Powered from an Auxiliary Winding for 12V VPP Power



*SEE THE LTC1142 DATA SHEET FOR AN EXAMPLE OF A 3.3V/5V DUAL REGULATOR WITH AUXILIARY WINDING 15V OUTPUT

TYPICAL APPLICATIONS

Dual Protected PCMCIA Power Management System
Powered by System 12V Supply



RELATED PARTS

See PCMCIA Product Family table on the first page of this data sheet.

SECTION 4—POWER PRODUCTS

Backup Battery Management Circuit

FEATURES

- **Micropower Operation (I_Q = 20μA)**
- **Adjustable Regulator for Battery Charging**
- **4.85V Regulator for Battery Regulation**
- Cell Voltage Equalization in 2-Cell Systems
- Low-Battery Detector Protects Lithium Cells
- Comparator for Automatic Power Switching
- Shutdown
- Output Current Sensing
- Current and Thermal Limiting
- Reverse Output Protection
- 16-Pin SO Package
- Operates on 7V to 30V Input

APPLICATIONS

- Backup Battery Management Systems for Portable Computers
- Lithium-Ion Backup Systems
- NiCd Backup Systems

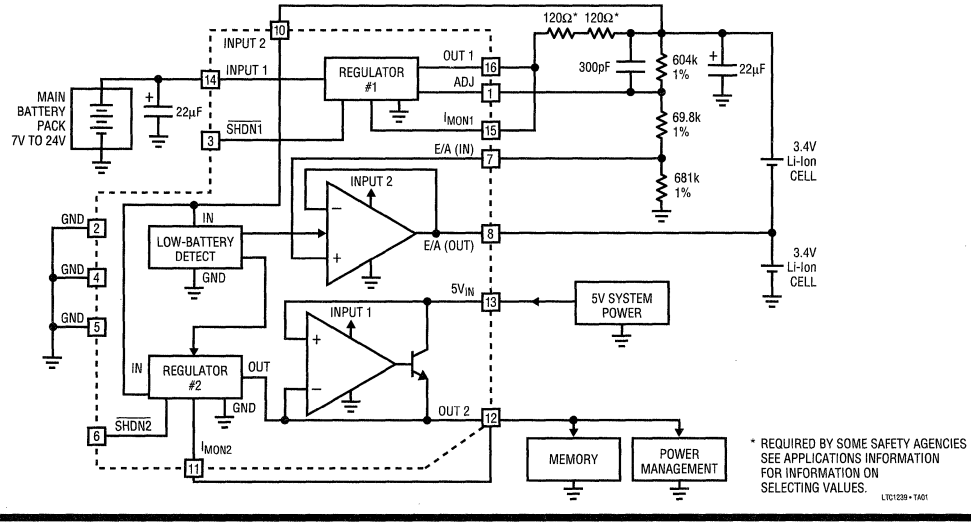
DESCRIPTION

The LT®1239 is a micropower backup battery management system for portable computers and instrumentation. It contains two regulators for regulating the battery voltage and memory voltage and a comparator for switching between main power and backup power. The first regulator provides a constant voltage charge for the backup batteries and is adjustable from 3.75V up to 20V. An equalization amplifier combined with the first regulator provides precision charge equalization for a 2-cell lithium-ion system. A second regulator with 4.85V output provides a regulated backup battery voltage to the memory when main power is lost. The second regulator also isolates the backup battery from the main 5V supply during normal operation when the memory is being powered by the 5V supply.

A comparator is included which provides automatic switchover from main 5V power to backup power ensuring uninterrupted power for memory and power monitor-

TYPICAL APPLICATION

Lithium-Ion Backup System



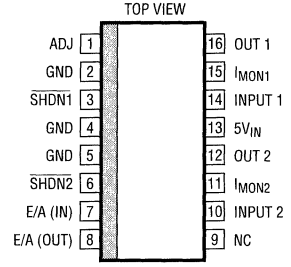
ESCRIPTION

g circuitry. A low-battery detector with a 5V threshold wers down the second regulator and the error amplifier limit the discharge voltage of the backup cells. This prevents deep discharge damage to the lithium cells. Both regulators have independent shutdown and current monitor functions.

BSOLUTE MAXIMUM RATINGS

ote 1)
put 1 Voltage ..... ±30V
put 2 Voltage ..... 30V, –0.6V
itput 1 Voltage ..... 30V, –0.6V
itput 2 Voltage ..... 6V, –0.6V
ljust Pin Current 10mA
HDN1, $\overline{SHDN2}$ (Note 2)
Input Voltage ..... 6V, –0.6V
Input Current 5mA
ON1 Voltage
(Note 3) ..... $(V_{IN1} - 30V) < I_{MON1} < V_{IN1}$
ON2 Voltage
(Note 4) ..... $(V_{IN2} - 30V) < I_{MON2} < V_{IN2}$
A Output Voltage (Note 5) .... $-0.6V < V_{E/A(OUT)} < V_{IN2}$
A Input Voltage (Note 5) ..... $-0.6V < V_{E/A(IN)} < V_{IN2}$
' Input Voltage ..... 6V, –0.6V
erating Temperature Range ..... 0 to 70°C
nction Temperature Range ..... (Note 6)
orage Temperature Range ..... –65°C to 150°C
ad Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 100°C, θ_{JA} = 120°C/W

ORDER PART NUMBER
LT1239CS

Consult factory for Industrial and Military grade parts.

4

LECTRICAL CHARACTERISTICS

RAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
gulator 1 (Notes 7, 8)						
gulated Output Voltage ($V_{ADJ} = V_{OUT1}$)	V_{IN1} = 4.3V, I_{OUT} = 1mA, T_J = 25°C		3.700	3.750	3.800	V
	V_{IN1} = 4.8V to 24V, I_{OUT} = 1mA to 30mA	●	3.650	3.750	3.825	V
e Regulation	I_{LOAD} = 1mA, V_{IN1} = 4.3V to 30V	●		2	10	mV
ad Regulation	V_{IN1} = 5V, I_{LOAD} = 1mA to 30mA, T_J = 25°C			–12	–25	mV
	V_{IN1} = 5V, I_{LOAD} = 1mA to 30mA	●		–20	–50	mV
	V_{IN1} = 5V, I_{LOAD} = 1mA to 50mA, T_J = 25°C			–20		mV
	V_{IN1} = 5V, I_{LOAD} = 1mA to 50mA			–30		mV
pout Voltage (Note 9)	I_{LOAD} = 1mA, T_J = 25°C			0.15	0.20	V
	I_{LOAD} = 30mA, T_J = 25°C			0.25	0.40	V
	I_{LOAD} = 50mA, T_J = 25°C			0.30		V
ound Pin Current (Notes 10, 11)	I_{LOAD} = 0mA, V_{IN1} = 3.75V	●		20	30	µA
	I_{LOAD} = 30mA, V_{IN1} = 3.75V	●		0.80	1.2	mA
	I_{LOAD} = 50mA, V_{IN1} = 3.75V			1.35		mA
ust Pin Bias Current (Note 12)	T_J = 25°C			40	120	nA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Regulator 1 (Notes 7, 8)						
Shutdown Threshold	V_{OUT1} = Off to On	●		1.20	2.8	V
	V_{OUT1} = On to Off	●	0.25	0.75		V
Shutdown Pin Current (Note 13)	$V_{\overline{SHDN1}}$ = 0V	●		2	4	µA
Quiescent Current in Shutdown (Note 10)	V_{IN1} = 24V, $V_{\overline{SHDN1}}$ = 0V	●		10	16	µA
Ripple Rejection	V_{IN1} = 5V (Avg), V_{RIPPLE} = 0.5V_{P-P} f_{RIPPLE} = 120Hz, I_{LOAD} = 20mA, T_J = 25°C		50	59		dB
Current Limit	V_{IN1} = 7V, V_{OUT1} = 0V, T_J = 25°C V_{OUT1} = $V_{OUT1(NOM)}$ – 100mV, T_J = 25°C		30 40	50 70		mA mA
Reverse Output Current	V_{OUT1} = 3.75V, V_{IN1} < 3.75V V_{OUT1} = 3.75V, V_{IN1} = Open Circuit	● ●		6 6	12 12	µA µA
Current Monitor Pin Output Current	V_{OUT1} = 3.75V, V_{IMON1} = 0V, I_{OUT1} = 1mA V_{OUT1} = 3.75V, V_{IMON1} = 0V, I_{OUT1} = 10mA V_{OUT1} = 3.75V, V_{IMON1} = 0V, I_{OUT1} = 50mA	 ● 	 38 	4.6 44 215	 50 	µA µA µA
Comparator						
Output Saturation Voltage (V_{5VIN} – V_{OUT2})	V_{IN1} = 7V, V_{IN2} = 0V, V_{5VIN} = 5V, I_{OUT2} = 1mA V_{IN1} = 7V, V_{IN2} = 0V, V_{5VIN} = 5V, I_{OUT2} = 30mA V_{IN1} = 7V, V_{IN2} = 0V, V_{5VIN} = 5V, I_{OUT2} = 50mA	● ● ●		12 110 135	40 150 220	mV mV mV
Low-Battery Detector						
Turn-Off Threshold	T_J = 25°C		4.85	5.00	5.15	V
Turn-On Threshold	T_J = 25°C			5.3		V
Hysteresis	T_J = 25°C		0.2	0.3		V
Regulator 2						
Regulated Output Voltage	V_{IN2} = 6.8V, I_{OUT} = 1mA, T_J = 25°C		4.775	4.850	4.925	V
Output Voltage Temperature Coefficient				–0.5		mV/°C
Line Regulation	I_{OUT2} = 1mA, V_{IN2} = 5.4V to 10V	●		2	5	mV
Load Regulation	V_{IN2} = 6.8V, I_{LOAD} = 1mA to 30mA, T_J = 25°C V_{IN2} = 6.8V, I_{LOAD} = 1mA to 30mA V_{IN2} = 6.8V, I_{LOAD} = 1mA to 50mA, T_J = 25°C V_{IN2} = 6.8V, I_{LOAD} = 1mA to 50mA	 ● 	 	–12 –20 –20 –30	–25 –50 	mV mV mV mV
Ground Pin Current	I_{LOAD} = 0mA, V_{IN2} = 5.4V I_{LOAD} = 30mA, V_{IN2} = 5.4V I_{LOAD} = 50mA, V_{IN2} = 5.4V	● ● ●		16 0.80 1.35	25 1.2 	µA mA mA
Shutdown Threshold	V_{OUT2} = Off to On V_{OUT2} = On to Off	● ●	 0.25	1.20 0.75	2.8 	V V
Shutdown Pin Current	$V_{\overline{SHDN2}}$ = 0V	●		1.7	4	µA
Ripple Rejection	V_{IN2} = 6.4V (Avg), V_{RIPPLE} = 0.5V_{P-P} f_{RIPPLE} = 120Hz, I_{LOAD} = 20mA, T_J = 25°C		50	58		dB
Current Limit	V_{IN2} = 6.8V, V_{OUT2} = 0V, T_J 25°C V_{OUT2} = $V_{OUT2(NOM)}$ – 100mV, T_J = 25°C		30 40	50 70		mA mA
Reverse Output Current	V_{OUT2} = 4.85V, V_{IN2} < 4.85V V_{OUT2} = 4.85V, V_{IN2} = Open Circuit	● ●		6 6	12 12	µA µA
Current Monitor Pin Output Current	V_{OUT2} = 6.8V, V_{IMON2} = 0V, I_{OUT2} = 1mA V_{OUT2} = 6.8V, V_{IMON2} = 0V, I_{OUT2} = 10mA V_{OUT2} = 6.8V, V_{IMON2} = 0V, I_{OUT2} = 50mA	 ● 	 35 	4.7 41 210	 47 	µA µA µA
Error Amplifier						
Bias Current	$V_{E/A(IN)}$ = 3.4V, V_{IN2} = 6.8V	●		3	20	nA

LECTRICAL CHARACTERISTICS

AMETER	CONDITIONS		MIN	TYP	MAX	UNITS
set Voltage		●		0	15	mV
put Current Sourcing Sinking	V_{IN2} = 6.8V, $V_{E/A(IN)}$ = 3.4V, T_J = 25°C V_{IN2} = 6.8V, $V_{E/A(IN)}$ = 3.4V, T_J = 25°C		3 3	5 5		mA mA
ulator 2, Low Battery Detector and Error Amplifier						
escent Current	V_{IN2} = 6.8V, $5V_{IN}$ = 0V, $V_{E/A(IN)}$ = 3.4V V_{IN2} = 6.8V, $5V_{IN}$ = 0V, $V_{E/A(IN)}$ = 3.4V, V_{PIN6} = 0V V_{IN2} = 4.8V, $5V_{IN}$ = 0V, $V_{E/A(IN)}$ = 2.4V	● ● ●		20 8 3	30 12 6	µA µA µA

● denotes specifications which apply over the full operating perature range.

e 1: All voltages are with respect to the ground pins of the device is 2, 4, 5) unless otherwise specified.

e 2: The shutdown pin input voltage rating is required for a low edance source. Internal protection devices connected to the shutdown will turn on and clamp the pin to approximately 7V or –0.6V. This ge allows the use of 5V logic devices to drive the pin directly. For high edance sources or logic running on supply voltages greater than 5.5V, maximum current driven into the shutdown pin must be limited to A.

e 3: The current monitor pin for regulator 1 (pin 15) can be pulled 30V ow the input pin (pin 14). The current monitor pin must not be pulled ve the input pin.

e 4: The current monitor pin for regulator 2 (pin 11) can be pulled 30V ow the input pin (pin 10). The current monitor pin must not be pulled ve the input pin.

e 5: E/A (OUT) pin should not be pulled below ground or above voltage at Input 2.

e 6: The device is specified to an operating temperature range of 0°C to C. The device is guaranteed to be functional up to the thermal tdown temperature. The thermal shutdown temperature for this device pproximately 100°C.

Note 7: Operating conditions are limited by maximum junction temperature. The regulated output specification will not apply for all possible combinations of input voltage and output current. When operating at maximum output current, the input voltage range must be limited. When operating at maximum input voltage, the output current range must be limited.

Note 8: Regulator 1 of the LT1239 is tested and specified with the adjust pin (pin 1) tied to the output pin (pin 16). See Applications Information.

Note 9: Dropout voltage is the minimum input/output voltage required to maintain regulation at the specified output current. In dropout, the output voltage measured at the package pins will be equal to (V_{IN} – $V_{DROPOUT}$).

Note 10: The quiescent current of the comparator is included in the ground pin current and quiescent current specifications for regulator 1. The comparator output is turned off (pin 13 = 0V, pin 12 = 5V) during these tests.

Note 11: Ground pin current for regulator 1 is tested with V_{IN} = V_{OUT} (nominal) and a current source load. This means that the device is tested in it's dropout region. Ground pin current will decrease slightly at higher input voltages.

Note 12: Adjust pin current flows into the adjust pin.

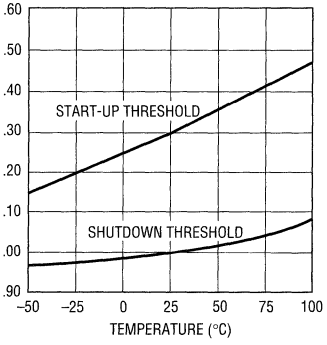
Note 13: Shutdown pin current at $V_{\overline{SHDN}}$ = 0V flows out of the shutdown pin.

Note 14: 6.8V is the nominal voltage of two lithium-ion cells.

4

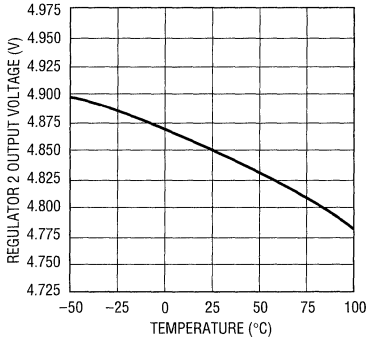
PICAL PERFORMANCE CHARACTERISTICS

Low-Battery Detector Thresholds vs Temperature



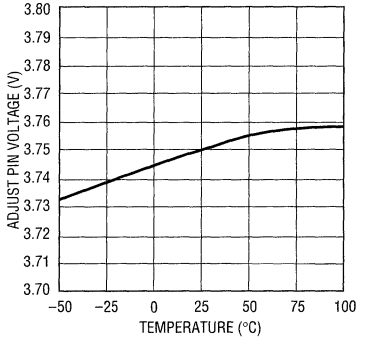
LT1239 • TPC01

Regulator 2 Output Voltage vs Temperature



LT1239 • TPC02

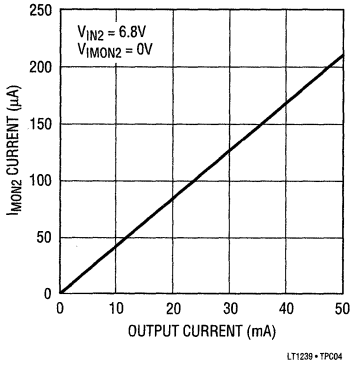
Regulator 1 Adjust Pin Voltage vs Temperature



LT1239 • TPC03

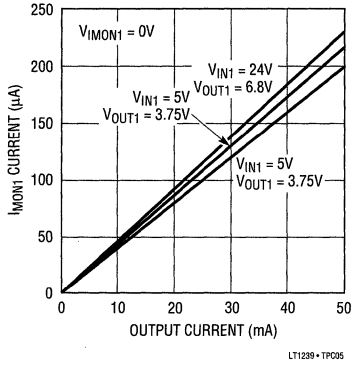
TYPICAL PERFORMANCE CHARACTERISTICS

Regulator 2 I_{MON2} Current vs Output Current



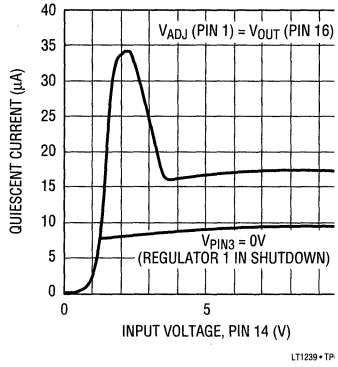
LT1239 • TPC04

Regulator 1 I_{MON} Current vs Output Current



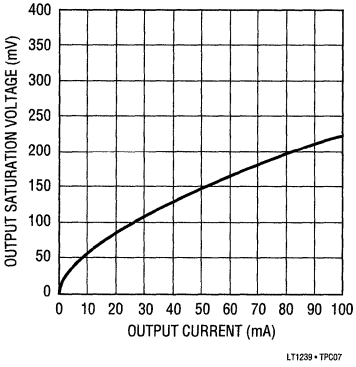
LT1239 • TPC05

Regulator 1, Comparator Quiescei Current vs Input Voltage, Pin 14



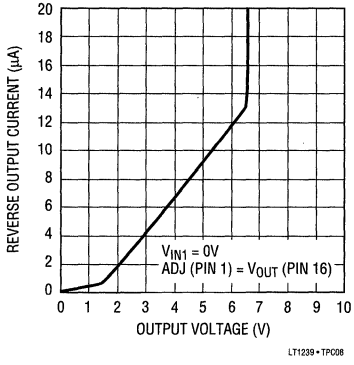
LT1239 • TP

Comparator Output Saturation Voltage vs Output Current



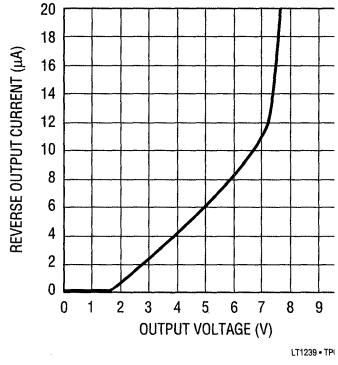
LT1239 • TPC07

Regulator 1 Reverse Output Current vs Output Voltage



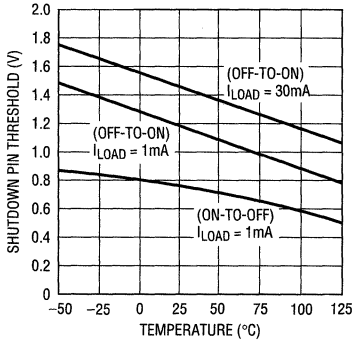
LT1239 • TPC08

Regulator 2 Reverse Output Current vs Output Voltage



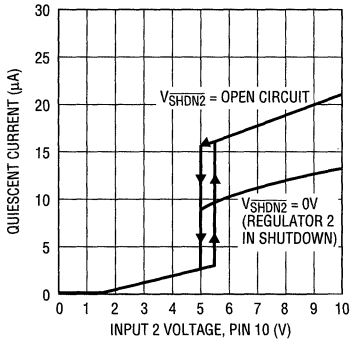
LT1239 • TP

Shutdown Pin Threshold



LT1239 • TPC10

Regulator 2, Error Amp, Low-Battery Detector Quiescent Current



LT1239 • TPC11

PIN FUNCTIONS

ADJ (Pin 1): Adjust Pin of Regulator 1. The regulator will servo the adjust pin to 3.75V referred to ground. Bias current will be approximately 50nA and will flow into the adjust pin.

GND (Pin 2): Ground Pin for Regulator 1. Note that the three ground pins (pins 2, 4, 5) are connected together internally and should all be grounded externally.

SHDN1 (Pin 3): Shutdown Pin for Regulator 1. Regulator output will be on if the shutdown pin is either: 1) Left floating (open circuit) or 2) pulled up to the 5V rail. If the shutdown function is not used, the shutdown pin is normally left open circuit. Regulator 1 output will be off if the shutdown pin is pulled to ground. The shutdown pin current with the pin pulled to ground will be in the range of 1µA flowing out of the pin. The shutdown pin current with the pin pulled up to 5V will be zero.

GND (Pin 4): Ground. This ground pin is tied to the substrate of the die, between regulator 1 and the rest of the circuit. It is used as an isolation barrier between regulator and the rest of the circuitry.

GND (Pin 5): Ground Pin for Regulator 2.

SHDN2 (Pin 6): Shutdown Pin for Regulator 2. Regulator output will be on if the shutdown pin is either: 1) Left floating (open circuit) or 2) pulled up to the 5V rail. If the shutdown function is not used, the shutdown pin is normally left open circuit. Regulator 2 output will be off if the shutdown pin is pulled to ground. The shutdown pin current with the pin pulled to ground will be in the range of 1µA flowing out of the pin. The shutdown pin current with the pin pulled up to 5V will be zero.

E/A (IN) (Pin 7): Noninverting Input of the Error Amplifier. This pin should be tied to the center tap point in the output divider for regulator 1. The bias current for this pin will be in the range of 3nA and it will flow out of the pin.

E/A (OUT) (Pin 8): Output of the Error Amplifier. This is normally connected to the center tap of the backup cells.

NC (Pin 9): Not Connected.

INPUT 2 (Pin 10): Input Pin (V_{CC}) for Regulator 2, the Error Amplifier, and the Low-Battery Detection Circuit.

I_{MON} 2 (Pin 11): Current Monitor Pin for Regulator 2. If the current monitor function is not used, this pin should be tied to the output pin of regulator 2.

OUT 2 (Pin 12): Output of Regulator 2. It is also the inverting input and output of the comparator. If the main 5V system supply is up and running then the comparator output will pull the output of regulator 2 up to 5V.

$5V_{IN}$ (Pin 13): Noninverting Input of the comparator and the collector of the output driver. The collector of the output driver is normally connected to the main 5V system supply.

INPUT 1 (Pin 14): Input Pin (V_{CC}) of Regulator 1.

I_{MON} 1 (Pin 15): Current Monitor Pin for Regulator 1. The current flowing out of this pin will be approximately 1/200 of the output current of regulator 1. If the current monitor function is not used, this pin should be tied to the output pin of regulator 1.

OUT 1 (Pin 16): Output of Regulator 1.

FUNCTIONAL DESCRIPTION

Regulator 1: Regulator 1 is used to supply the charging current to the backup batteries. It converts the voltage on the main battery to a fixed output voltage to charge the backup cells. The output voltage is set with a voltage divider connected between the output and ground with a tap point of the divider connected to the adjust pin. The regulator servos its output in order to maintain the adjust pin at 3.75V referred to ground. The resistor divider should be chosen such that the divider current is approximately 5µA. This means the impedance from the adjust pin to ground should be approximately 750kΩ. For safety requirements a resistor can be placed between the output pin and the top of the divider that sets the regulated output voltage. The regulator will regulate the voltage at the top of the divider. Quiescent current will be 10µA to 15µA. Output short-circuit current will be approximately 70mA.

FUNCTIONAL DESCRIPTION

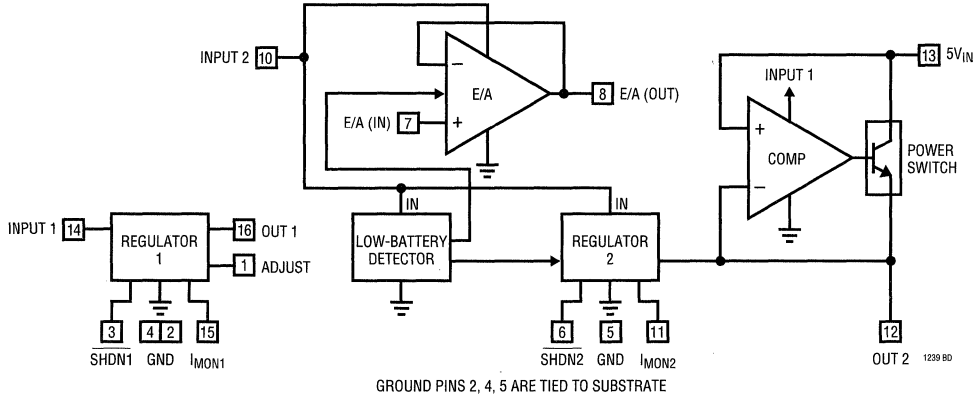
Comparator: The output of the comparator is connected to the output of regulator 2. This point provides power to memory and power management circuitry. The comparator looks at the main 5V power line and the output voltage of regulator 2. If the main 5V line is up and regulating the comparator output will pull up to 5V and supply power to the memory from the main 5V regulator. If the main 5V power line drops below 4.85V the comparator switches off and regulator 2 will supply power to the memory from the backup batteries. The comparator is powered from the raw battery voltage at the input of regulator 1.

Error Amplifier: The Error Amplifier is used to equalize the cell voltages of two lithium-ion cells connected in series. The error amplifier is designed to source or sink 5mA.

Low-Battery Detector: The low-battery detector circuit acts as an undervoltage lockout. This circuit turns regulator 2 and the error amplifier off if the backup battery voltage drops below 5V. The low-battery detector circuit will turn regulator 2 and the error amplifier back on when the backup battery voltage rises above 5.3V. This circuit has a quiescent current of approximately 3μA in the undervoltage condition.

Regulator 2: Regulator 2 is used to regulate the voltage of the backup batteries and isolate the backup batteries from the main 5V line. This regulator will prevent reverse current flow from the main 5V supply back into the backup cells.

BLOCK DIAGRAM



GROUND PINS 2, 4, 5 ARE TIED TO SUBSTRATE

APPLICATIONS INFORMATION

Device Overview

The LT1239 provides several functions needed for backup battery management. It provides:

1. Battery Charging: The LT1239 can be set up to charge lithium-ion or nickel cadmium batteries in either constant voltage or constant current mode.
2. Memory Power Control: The LT1239 provides power for the memory and includes automatic switchover between the backup battery and the main 5V system power. When the 5V system supply is up and running it is used to power the memory, the regulator prevents reverse current flow back into the backup battery. Automatic switchover occurs when the 5V system supply drops below 4.85V and the regulator then provides power to the memory from the backup cells. Memory power is uniterruptable.

IPPLICATIONS INFORMATION

Protection: Regulator 1 allows the use of current limiting resistors to prevent overcharging lithium-ion cells. A low-battery detector shuts down regulator 2 and the error amplifier to prevent over discharging the lithium cells. An error amplifier is included to provide voltage equalization for two series connected lithium-ion cells.

ljusting Output Voltage

ɜgulator 1 is an adjustable regulator. This allows the ıtput voltage to be set for various battery types and ıltages. The output voltage is adjustable from 3.75V up 20V. The regulator will servo its output voltage in order maintain the adjust pin at 3.75V with respect to ground. ıe output voltage is set with a resistor divider from output ground as shown in Figure 1. The resistor values should chosen so that the current in the divider is approxiately 5µA. This means that the impedance from the just pin to ground should be approximately 750kΩ. The as current at the adjust pin is 50nA (typical) and will flow to the adjust pin. The error in the output voltage, due to e adjust pin bias current will be equal to the bias current ultiplied by the value of R2 ($I_{ADJ} \times R2$). This error is small d is compensated for in the formulas shown in Figure 1.

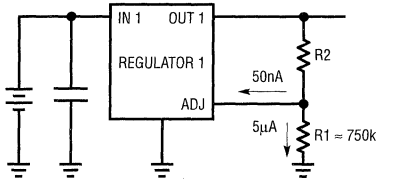


Figure 1. Adjusting Output Voltage

ample: To set the output voltage to 6.8V for a 2-cell ıium-ion system, use R1 = 750k and I_{ADJ} = 50nA.

en:

$$R2 = \frac{6.8V - 3.75V}{(3.75V/750k) + 50nA} = 604k$$

Equalizing Lithium-Ion Cells

The error amplifier on the LT1239 is used to equalize the cell voltages in a 2-cell lithium-ion backup system. The error amplifier is internally connected as a unity-gain follower and is designed to sink or source about 3mA. The bias current for the error amplifier will be approximately 3nA and will flow out of the pin. The output voltage of the error amplifier can be set by connecting the input to a tap point on the resistor divider used to set the output voltage for regulator 1 as shown in Figure 2. The error amplifier will then equalize the cell voltages by charging the cell with the lowest output voltage. The output voltage of regulator 1 controls the total cell voltage and the error amplifier forces the cell voltages to be equal. The error amplifier output current will go to zero when the cell voltages are equal and the total cell voltage is equal to the output voltage of regulator 1.

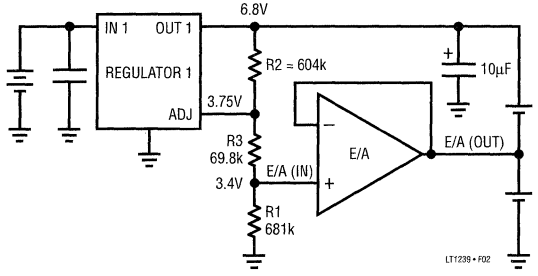


Figure 2. Equalizing Lithium-Ion Cells

For battery voltages greater than the low-battery detection threshold the error amplifier is active. For battery voltages lower than the low-battery detection threshold the output of the error amplifier is inactive. When the error amplifier is active it can source or sink approximately 3mA. When the error amplifier is inactive its output is a high impedance, as long as it is not forced above V_{IN2} or below ground.

The error amplifier is powered from the same supply pin as regulator 2. In most applications the backup batteries and the output of regulator 1 will provide power to this point. This means that the protection resistors (R4 in Figure 5) in series with the output of regulator 2 will limit the output current capability of the error amplifier in a fault condition.

APPLICATIONS INFORMATION

Using the Current Monitor Function

The current monitor pin outputs a current proportional to the output current of the regulator. Both regulator 1 and regulator 2 have independent current monitor pins. The current monitor function can be used to monitor charge in the backup cells, to set up a constant current output or to adjust the current limit of the regulator. The current monitor pin should be tied to the output pin if the current monitor function is not used. This will minimize quiescent current.

The current output of the current monitor pin can be converted to a voltage by feeding the current monitor pin output current through a resistor. The voltage across the resistor will be proportional to output current. This signal can be used to monitor the output current for either regulator. Regulator 1 output current is equal to the charge current for the backup batteries plus the load current of regulator 2. If regulator 1 output current is greater than regulator 2 output current, the difference between the currents is the charge current for the backup cells. If regulator 2 output current is greater than regulator 1 output current, the difference between the currents is the discharge current for the backup cells. By integrating the difference between regulator 1 output current and regulator 2 output current the total charge in the backup cells can be determined.

Constant Current Charging

NiCd backup batteries are normally charged with a constant current trickle charge. This can be accomplished using regulator 1 and the circuit shown in Figure 3 In this circuit the voltage at the adjust pin is proportiona to the output current. Regulator 1 will servo its output tc force 3.75V at the adjust pin. The output current will be scaled from the current monitor pin current by a ratio o 220:1. Output current is equal to 220 × current monitor pir current. The output current is set by choosing resistor R1 in the formula shown in Figure 3. Regulator 1 will source a constant current as long as the voltage at its input is greater than the battery voltage plus the dropout voltage o regulator 1. External power monitoring circuitry can be used to shutdown regulator 1 to terminate charge when a low current sleep mode is desired.

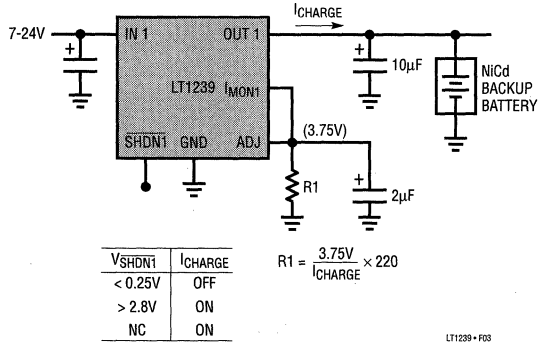


Figure 3. Constant Current Charging

Setting Current Limit Using the Current Monitor Pin

With the addition of some simple external circuitry the current monitor pin can be used to control the outpu short-circuit current of the regulator. As shown in Figure 4, the current monitor pin can be tied to ground through a resistor to generate a voltage proportional to outpu current. When the voltage across R3 is equal to approximately 0.6V (one V_{BE}) Q1 will turn on and pull down on the shutdown pin of the regulator. Q1 effectively steals drive current from the regulator to limit the output current. C1 is needed to roll off the gain of Q1. Current limit can be se using the formula shown in Figure 4. This circuit can be used with either regulator. The shutdown function car also be used. An open-collector gate connected in paralle with Q1 can shut down the regulator.

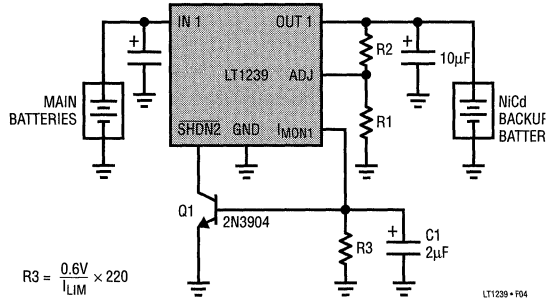


Figure 4. Reducing Current Limit

Using the Comparator

The comparator in the LT1239 is intended to be used as ar automatic switchover circuit between the main 5\

APPLICATIONS INFORMATION

system power and the backup batteries. The comparator output will be driven high if the output of the 5V system supply is greater than the 4.85V output of regulator 2. Regulator 2 will act as a diode to prevent current flow from the 5V system supply back into the backup battery. Current flow into the output of regulator 2, with the output pulled up to 5V, will be limited to approximately 6μA and will flow to ground. If the main 5V system supply drops below the 4.85V output of regulator 2 the comparator will switch off and regulator 2 will provide power to the memory. The comparator combined with regulator 2 and the batteries provide an uninterruptable power source to the memory and power monitoring circuitry.

Choosing Current Limiting Resistors

Due to UL safety considerations, circuits used to charge lithium-ion batteries must have external resistors (passive components) to limit the available charge current in the event of a failure in the charging circuit. The LT1239 allows these resistors to be placed in series with the output transistor of the regulator 1 as shown in Figure 5. The current limiting resistor (R4) will be in series with the main charge current path but will be inside the feedback loop of regulator 1. Because the resistors are inside the feedback loop they will not affect output voltage regulation in normal operating conditions. The resistors should be selected so that they limit the charge current below the maximum level specified by the battery manufacturer. For a typical 3.4V, 50mA rechargeable backup cell (Panasonic VL2330) the maximum charge current is specified at 300mA. Most users will choose to limit the current well below the maximum charge current. It is important to note that these resistors can also limit the charge current during normal operation. Since the charge current for a typical lithium-ion button cell is normally less than 20mA, limited by the internal impedance of the cells during a constant voltage charge, the current limiting resistors do not significantly affect the charge times for the backup cells. The worst case would occur if the regulator failed as a short and the main battery is at its maximum charge voltage. The current limiting resistor (R4) must be chosen to limit the current to less than the manufacturers maximum charging current with the difference between the main battery voltage and the backup battery voltage dropped across it.

For example with a main battery voltage of 24V max, a backup battery voltage of 6.8V and a maximum charge current of 300mA, R4 must be greater than (24V – 6.8V)/300mA, R4 > 57Ω.

R4 can also be used to limit the power dissipated by regulator 1 as shown in the following section. C1 is needed for stability in circuits with protection resistors (R4).

The power dissipation in R4 during fault conditons can be significant. it will be equal to:

$$\frac{(V_{INL} - V_{BATTERY})^2}{R4}$$

Power resistors with ratings greater than 0.25W or fusable resistors may be required.

Thermal Considerations

The power dissipation of this device is made up of several components.They are the power dissipation of each regulator, the comparator and the error amplifier. The largest component will be due to the power in regulator 1, when the charge current for the batteries is the highest and the input voltage to regulator 1 is at the maximum. In most systems this condition only occurs for a short period after the backup battery has been completely discharged. Both regulators have thermal limiting circuitry which limits the power in the regulator when the junction temperature reaches about 100°C. The thermal limit temperature is set low because the device is designed to work with batteries specified to run at ambient temperatures below 60°C. The power in regulator 1 can be limited with external resistors placed in the feedback loop as shown in Figure 5. In lithium-ion systems these resistors are required for safety reasons.

The power in regulator 1 will be equal to:

$$[(V_{MAINBATTERY} - V_{BACKUPBATTERY}) \times I_{CHG}] - (I_{CHG} \times R4)$$

Note that for circuits with a current limiting resistor (R4) the worst-case power point occurs when I_{CHG} is equal to the maximum charging current/2.

Example: $[(24V - 6.8V) \times (71mA/2)] - [(71mA/2) \times 240]$
$= 300mW$

This is the only significant component of power dissipation in the device and this condition will only occur when the

APPLICATIONS INFORMATION

backup batteries have been completely discharged. Once the backup batteries are charged the power in regulator 1 drops significantly. The power in regulator 2 when regulator 2 is providing power to the memory will be equal to:

$(V_{BACKUPBATTERY} - 4.85V) \times I_{OUT}$

I_{OUT} is the current needed to power the memory and power monitoring circuitry.

Example: $(6.8V - 4.85V) \times 30mA = 58.5mW$

The power in the comparator when the comparator is providing power to the memory will be equal to:

$(V_{SAT} \times I_{OUT})$

I_{OUT} is the current needed to power the memory and power monitoring circuitry. Comparator Output Saturation Voltage vs Output Current can be found in the Typical Performance Characteristics.

Example: $(V_{SAT} \times I_{LOAD}) = (0.15V \times 30mA) = 4.5mW$

Note that power for memory will be supplied by either regulator 2 or the comparator. The power in the error amplifier when the cells are unequalized will be equal to:

$(V_{BACKUPBATTERY}/2) \times 3mA$

Example: $(6.8V/2) \times 3mA = 10.2mW$

This component goes to zero when the cell voltages are equalized.

The thermal resistance of the LT1239 is 120°C/W when the device is mounted to a PC board with at least one ground or power plane. The junction temperature rise will be equal to the total power in the device multiplied by 120°C/W or ($P_{TOTAL} \times 120°C/W$). For 300mW dissipation the junction temperature rise will be ($300mW \times 120°C/W$) = 36°C. Given that the thermal limit temperature is approximately 100°C, this allows for a maximum ambient temperature of roughly 60°C before the device thermal limits. This temperature is near the maximum ambient allowed for most battery types.

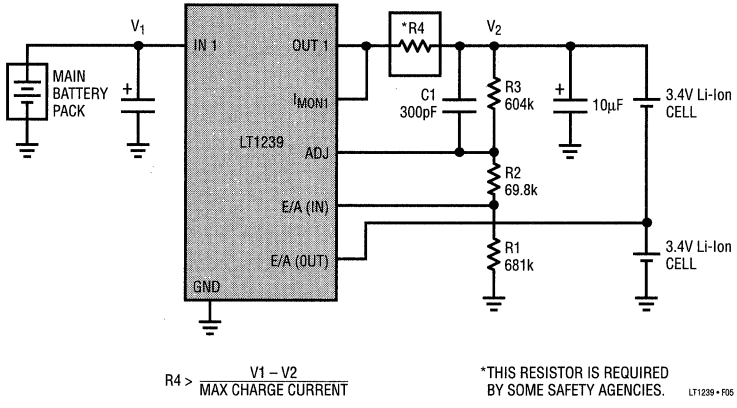
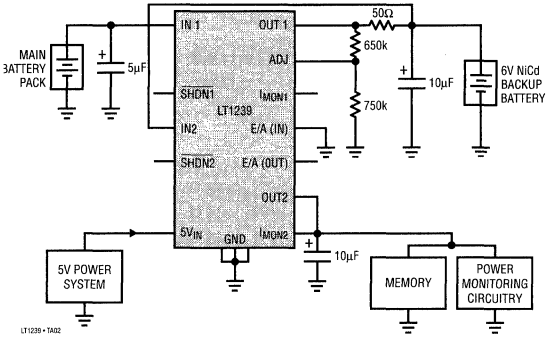


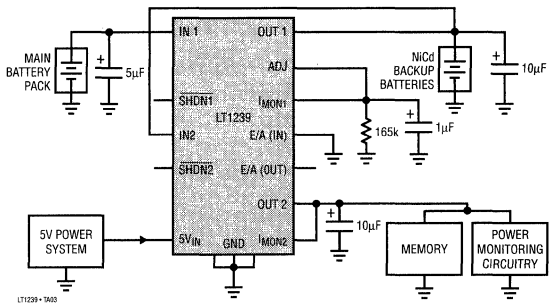
Figure 5. Adding a Protection Resistor for Lithium-Ion Charger

TYPICAL APPLICATIONS

NiCd Backup System with 20mA Charge Current



NiCd Backup System with 5mA Trickle Charge



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1111	Micropower DC/DC Converter with Adjustable or Fixed 5V or 12V Output	Low-Battery Detector
LT1120A	Micropower Regulator and Comparator with Shutdown	20µA Supply Current
LT1121	Micropower Regulator with Shutdown	0.4V Dropout Voltage at 150mA
LTC®1232	Microprocessor Supervisory Circuit	Minimum External Components
LTC1325	Microprocessor-Controlled Battery Management System	Charges Battery and Provides Gas Gauge
LTC1443/LTC1444/LTC1445	Quad Micropower Comparators with Reference	6µA Quiescent Current
LT1510	Programmable PWM Battery Charger with 2A Peak Current Capability	Charges NiCd, NiMH

4

Microprocessor-Controlled Battery Management System

FEATURES

- **Fast Charge Nickel-Cadmium, Nickel-Metal-Hydride, Lithium Ion or Lead-Acid Batteries under µP Control**
- **Flexible Current Regulation:**
  - Programmable 111kHz PWM Current Regulator with Built-In PFET Driver
  - PFET Current Gating for Use with External Current Regulator or Current Limited Transformer
- Discharge Mode
- Measures Battery Voltage, Battery Temperature and Ambient Temperature with Internal 10-Bit ADC
- **Battery Voltage, Temperature and Charge Time Fault Protection**
- Built-In Voltage Regulator and Programmable Battery Attenuator
- **Easy-to-Use 3- or 4-Wire Serial µP Interface**
- **Accurate Gas Gauge Function**
- Wide Supply Range: V_{DD} = 4.5V to 16V
- Can Charge Batteries with Voltages Greater Than V_{DD}
- Can Charge Batteries from Charging Supplies Greater Than V_{DD}
- Digital Input Pins Are High Impedance in Shutdown Mode

APPLICATIONS

- System Integrated Battery Charger

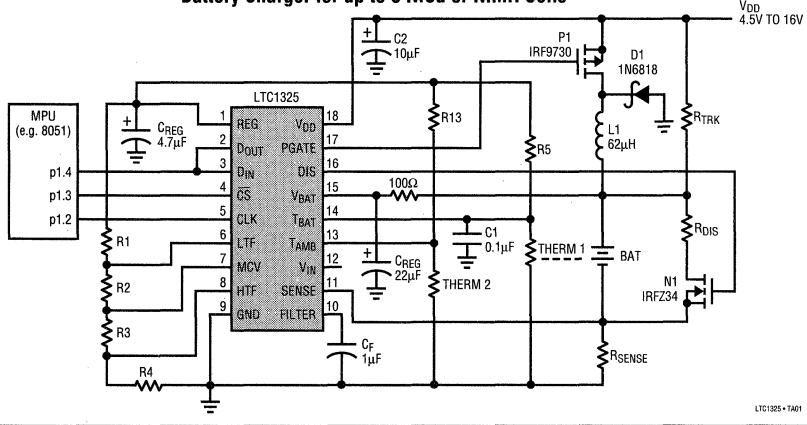
DESCRIPTION

The LTC®1325 provides the core of a flexible, cost-effective solution for an integrated battery management system. The monolithic CMOS chip controls the fast charging of nickel-cadmium, nickel-metal-hydride, lead-acid or lithium batteries under microprocessor control. The device features a programmable 111kHz PWM constant current source controller with built-in FET driver, 10-bit ADC, internal voltage regulator, discharge-before-charge controller, programmable battery voltage attenuator and an easy-to-use serial interface.

The chip may operate in one of five modes: power shutdown, idle, discharge, charge or gas gauge. In power shutdown the supply current drops to 30µA and in the idle mode, an ADC reading may be made without any switching noise affecting the accuracy of the measurement. In the discharge mode, the battery is discharged by an external transistor while the battery is being monitored by the LTC1325 for fault conditions. The charge mode is terminated by the µP while monitoring any combination of battery voltage and temperature, ambient temperature and charge time. The LTC1325 also monitors the battery for fault conditions before and during charging. In the gas gauge mode the LTC1325 allows the total charge leaving the battery to be calculated.

TYPICAL APPLICATION

Battery Charger for up to 8 NiCd or NiMH Cells

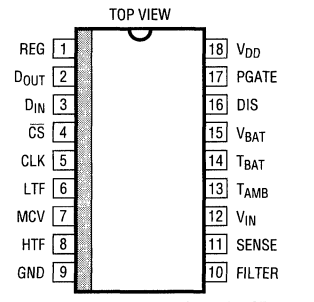


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{DD} to GND 17V
All Other Pins ..... −0.3V to V_{DD} + 0.3V
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
18-LEAD PDIP

SW PACKAGE
18-LEAD PLASTIC SO WIDE

T_{JMAX} = 125°C, θ_{JA} = 75°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 100°C/W (SW)

ORDER PART NUMBER
LTC1325CN LTC1325CSW

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V ±5%, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	V_{DD} Supply Voltage		●	4.5		16	V
I_{DD}	V_{DD} Supply Current	All TTL Inputs = 0V or 5V, No Load on REG	●		1200	2000	µA
I_{PD}	V_{DD} Supply Current	Power-Down Mode, All TTL Inputs = 0V or 5V	●		30	50	µA
V_{REG}	Regulator Output Voltage	No Load	●	3.047	3.072	3.097	V
ΔV_{DREG}	Regulator Load Regulation	Sourcing Only, I_{REG} = 0mA to 2mA			−1	−5	mV/mA
ΔV_{IREG}	Regulator Line Regulation	No Load, V_{DD} = 4.5V to 16V			−60	−100	µV/V
TC_{REG}	Regulator Output Tempco	No Load, 0°C < T_A < 70°C			50		ppm/°C
V_{DAC}	DAC Output Voltage	VR1 = 1, VR0 = 1, 100% Duty Ratio, I_{CHRG} = I (Note 7) VR1 = 1, VR0 = 0, 100% Duty Ratio, I_{CHRG} = I/3 VR1 = 0, VR0 = 1, 100% Duty Ratio, I_{CHRG} = I/5 VR1 = 0, VR0 = 0, 100% Duty Ratio, I_{CHRG} = I/10		140 48 30 16	160 55 34 18	180 62 38 21	mV mV mV mV
V_{HYST}	Fault Comparator Hysteresis	V_{HTF} = 1V, V_{EDV} = 0.9V, V_{BATR} = 100mV V_{MCV} = V_{LTF} = 2V			±20 ±10		mV mV
V_{OS}	Fault Comparator Offset	V_{HTF} = 1V, V_{EDV} = 0.9V, V_{BATR} = 100mV V_{MCV} = V_{LTF} = 2V			±50		mV
V_{BATR}	V_{BAT} for BATR = 1				100		mV
V_{BATP}	V_{BAT} for BATP = 1		●	V_{DD} − 1.8			V
V_{EDV}	Internal EDV Voltage		●	860	900	945	mV
V_{LTF}, V_{MCV}	LTF, MCV Voltage Range			1.6		2.8	V
V_{HTF}	HTF Voltage Range			0.5		1.3	V
A_{GG}	Gas Gauge Gain	−0.4V < V_{SENSE} < 0V			−4		
$V_{OS(GG)}$	Gas Gauge Offset	−0.4V < V_{SENSE} < 0V (Note 6)			±1		LSB
R_F	Internal Filter Resistor				1000		Ω
TOL_{BATD}	Battery Divider Tolerance	All Division Ratios	●	−2		2	%
V_{IL}	Input Low Voltage	CLK, $\overline{CS}$, D_{IN}	●	0.8	1.3		V
V_{IH}	Input High Level	CLK, $\overline{CS}$, D_{IN}	●		1.7	2.4	V
I_{IL}	Low Level Input Current	V_{CLK}, $V_{\overline{CS}}$ or V_{DIN} = 0V	●	−2.5		2.5	µA
I_{IH}	High Level Input Current	V_{CLK}, $V_{\overline{CS}}$ or V_{DIN} = 5V	●	−2.5		2.5	µA

4

ELECTRICAL CHARACTERISTICS

V_{DD} = 12V ±5%, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Output Low Voltage	D_{OUT}, I_{OUT} = 1.6mA	●			0.4	V
V_{OH}	Output High Voltage	D_{OUT}, I_{OUT} = –1.6mA	●	2.4			V
I_{OZ}	Hi-Z Output Leakage	$V_{\overline{CS}}$ = 5V	●			±10	µA
V_{OHFET}	DIS or PGATE Output High	V_{DD} = 4.5V to 16V	●	V_{DD} – 0.05			V
V_{OLFET}	DIS or PGATE Output Low	V_{DD} = 4.5V to 16V	●			0.05	V
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Valid	See Test Circuits	●			650	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●			510	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●			400	ns
t_{hDO}	Time D_{OUT} Remains Valid After CLK↓	See Test Circuits	●		30		ns
t_{rDOUT}	D_{OUT} Rise Time	See Test Circuits	●			250	ns
t_{fDOUT}	D_{OUT} Fall Time	See Test Circuits	●			100	ns
f_{CLK}	Serial I/O Clock Frequency	CLK Pin	●	25		500	kHz
t_{rPGATE}	PGATE Rise Time	C_{LOAD} = 1500pF	●			150	ns
t_{fPGATE}	PGATE Fall Time	C_{LOAD} = 1500pF	●			150	ns
f_{OSC}	Internal Oscillator Frequency	Charge Mode, Fail-Safes Disabled		90	111	130	kHz
A/D Converter							
	Offset Error	V_{IN} Channel (Note 3)	●			±2	LSB
	Linearity Error	V_{IN} Channel (Notes 3, 4)	●			±0.5	LSB
	Full-Scale Error	V_{IN} Channel (Note 3)	●			±1	LSB
	On-Channel Leakage	V_{IN} Channel ON Only (Notes 3, 5)	●			±10	µA
	Off-Channel Leakage	V_{IN} Channel OFF (Notes 3, 5)	●			±10	µA

RECOMMENDED CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{hDI}	Hold Time, D_{IN} After CLK↑		150			ns
$t_{dsu\overline{CS}}$	Setup Time, $\overline{CS}$ Before First CLK↑		1			µs
t_{dsuDI}	Setup Time, D_{IN} Stable Before First CLK↑		400			ns
t_{WHCLK}	CLK High Time		0.8			µs
t_{WLCLK}	CLK Low Time		1			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfers		1			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	MSBF = 1 MSBF = 0	43 52			CLK Cycles CLK Cycles

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to the GND pin.

Note 3: V_{REG} within specified min and max limits, CLK (Pin 5) = 500kHz, unless otherwise stated. ADC clock is the serial CLK.

Note 4: Linearity error is specified between the actual end points of the A/D transfer curve.

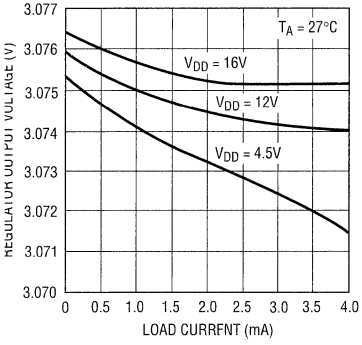
Note 5: Channel leakage is measured after channel selection.

Note 6: Gas gauge offset excludes A/D offset error.

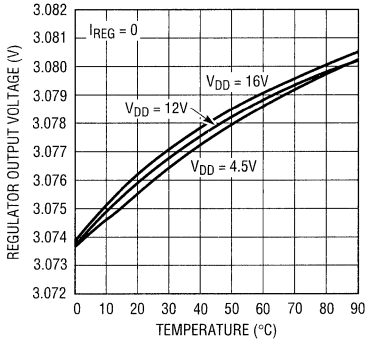
Note 7: $I = V_{DAC}(\text{Duty Ratio})/R_{SENSE}$, where V_{DAC} is the DAC output voltage with control bits VR1 = VR0 = 1, duty ratio = 1 and R_{SENSE} is determined by the user.

TYPICAL PERFORMANCE CHARACTERISTICS

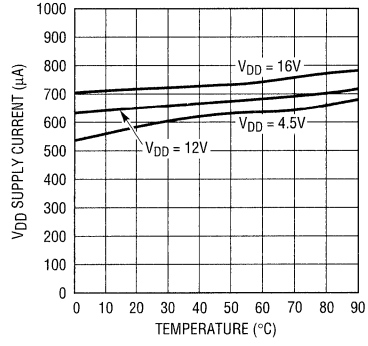
Regulator Output Voltage vs Load Current



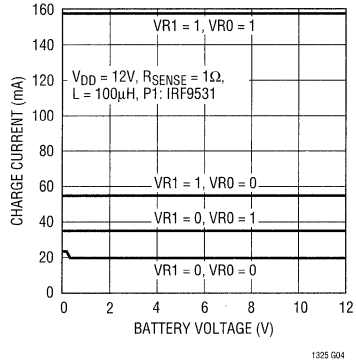
Regulator Output Voltage vs Temperature



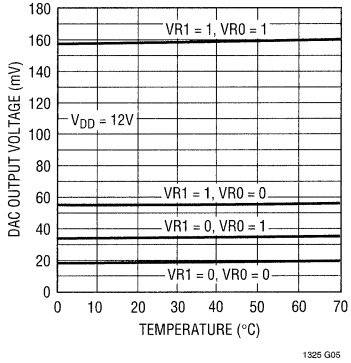
V_{DD} Supply Current vs Temperature



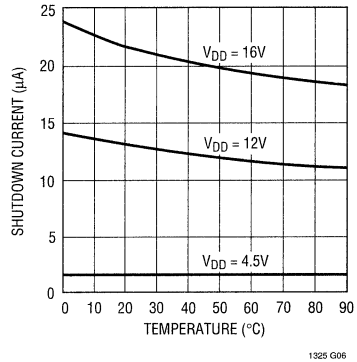
Charge Current vs Battery Voltage



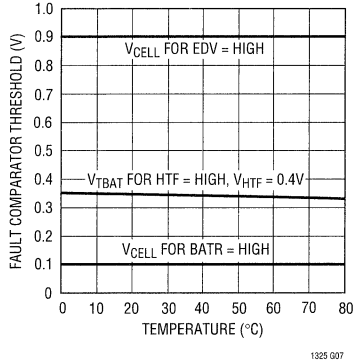
DAC Output Voltage vs Temperature



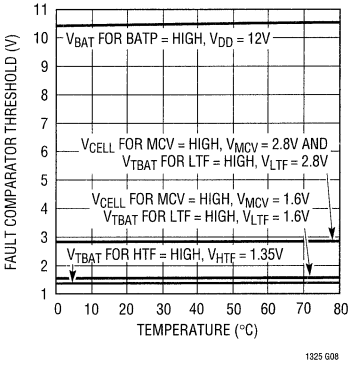
Shutdown Current vs Temperature



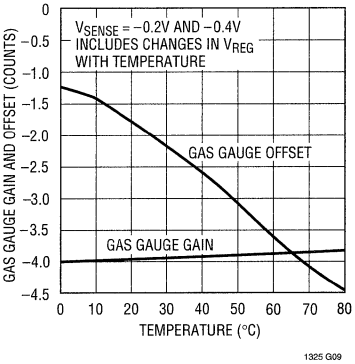
Fault Comparator Threshold vs Temperature



Fault Comparator Threshold vs Temperature

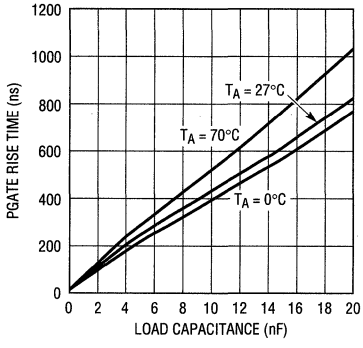


Gas Gauge Gain and Offset vs Temperature

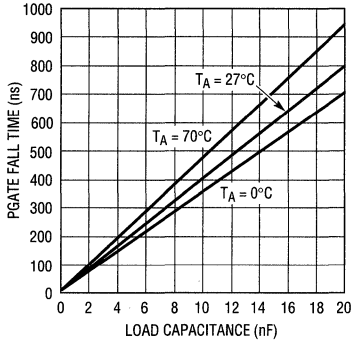


TYPICAL PERFORMANCE CHARACTERISTICS

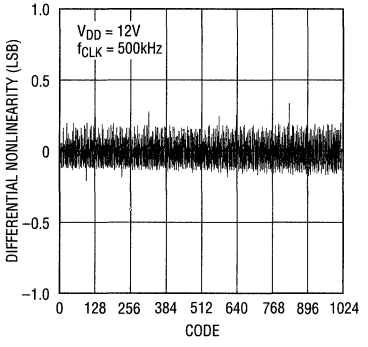
PGATE Rise Time vs Load Capacitance



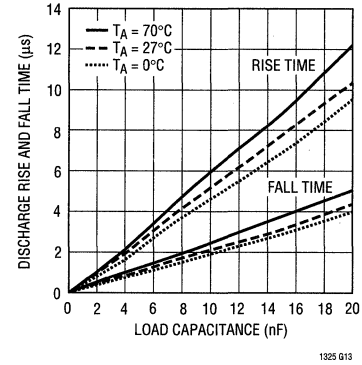
PGATE Fall Time vs Load Capacitance



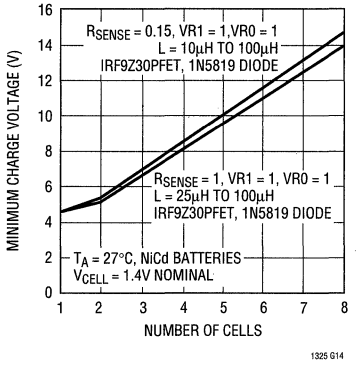
Differential Nonlinearity



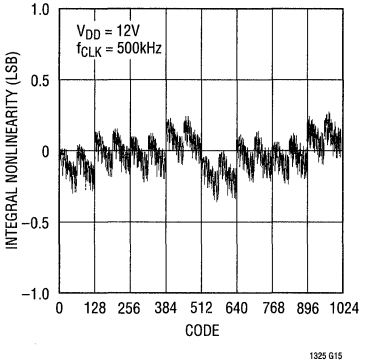
Discharge Rise and Fall Time vs Load Capacitance



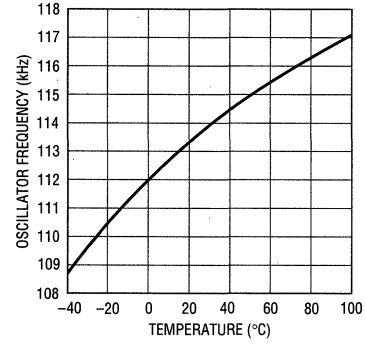
Minimum Charging Supply vs Number of Cells



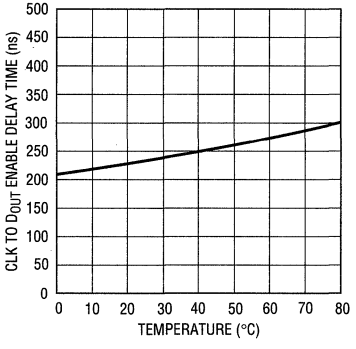
Integral Nonlinearity



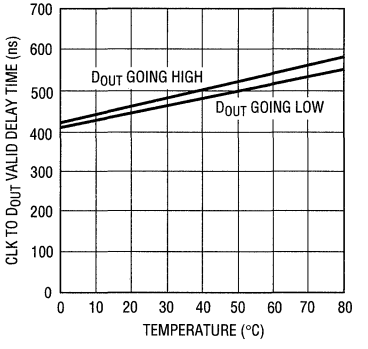
Oscillator Frequency vs Temperature



CLK to D_{OUT} Enable Delay Time vs Temperature



CLK to D_{OUT} Valid Delay Time vs Temperature



PIN FUNCTIONS

REG (Pin 1): Internal Regulator Output. The regulator provides a steady 3.072V to the internal analog circuitry and provides a temperature stable reference voltage for generating MCV, HTF, LTF and thermistor bias voltages with external resistors. Requires a 4.7µF or greater bypass capacitor to ground.

D_{OUT} (Pin 2): TTL Data Output Signal for the Serial Interface. D_{OUT} and D_{IN} may be tied together to form a 3-wire interface, or remain separated to form a 4-wire interface. Data is transmitted on the falling edge of CLK (Pin 5).

D_{IN} (Pin 3): TTL Data Input Signal for the Serial Interface. The data is latched into the chip on the rising edge of the CLK (Pin 5).

$\overline{CS}$ (Pin 4): TTL Chip Select Signal for the Serial Interface.

CLK (Pin 5): TTL Clock for the Serial Interface.

LTF (Pin 6): Minimum Allowable Battery Temperature Analog Input. LTF may be generated by a resistive divider between REG (Pin 1) and ground.

MCV (Pin 7): Maximum Allowable Cell Voltage Analog Input. MCV may be generated by a resistive divider between REG (Pin 1) and ground.

HTF (Pin 8): Maximum Allowable Battery Temperature Analog Input. HTF may be generated by a resistive divider between REG (Pin 1) and ground.

GND (Pin 9): Ground.

FILTER (Pin 10): The external filter capacitor C_F is connected to this pin. The filter capacitor is connected to the output of the internal resistive divider across the battery to reduce the switching noise while charging. In the gas gauge mode, C_F along with an internal R_F = 1k form a lowpass filter to average the voltage across the sense resistor.

SENSE (Pin 11): The Sense pin controls the switching of the 111kHz PWM constant current source in the charging mode. The Sense pin is connected to an external sense resistor R_{SENSE} and the negative side of the battery. The charging loop forces the average voltage at the Sense pin to equal a programmable internal reference voltage V_{DAC}. The battery charging current is equal to V_{DAC}/R_{SENSE}.

In the gas gauge mode the voltage across the Sense pin is filtered by an RC network (R_F and C_F), amplified by an inverting gain of four, then multiplexed to the ADC so the average discharge current through the battery may be measured and the total charge leaving the battery calculated.

V_{IN} (Pin 12): General Purpose ADC Input.

T_{AMB} (Pin 13): Ambient Temperature Input. Connect to an external thermistor network. Tie to REG if not used. May be used as another general purpose ADC input.

T_{BAT} (Pin 14): Battery Temperature Input. Connect to an external NTC thermistor network. Tie to REG if not used.

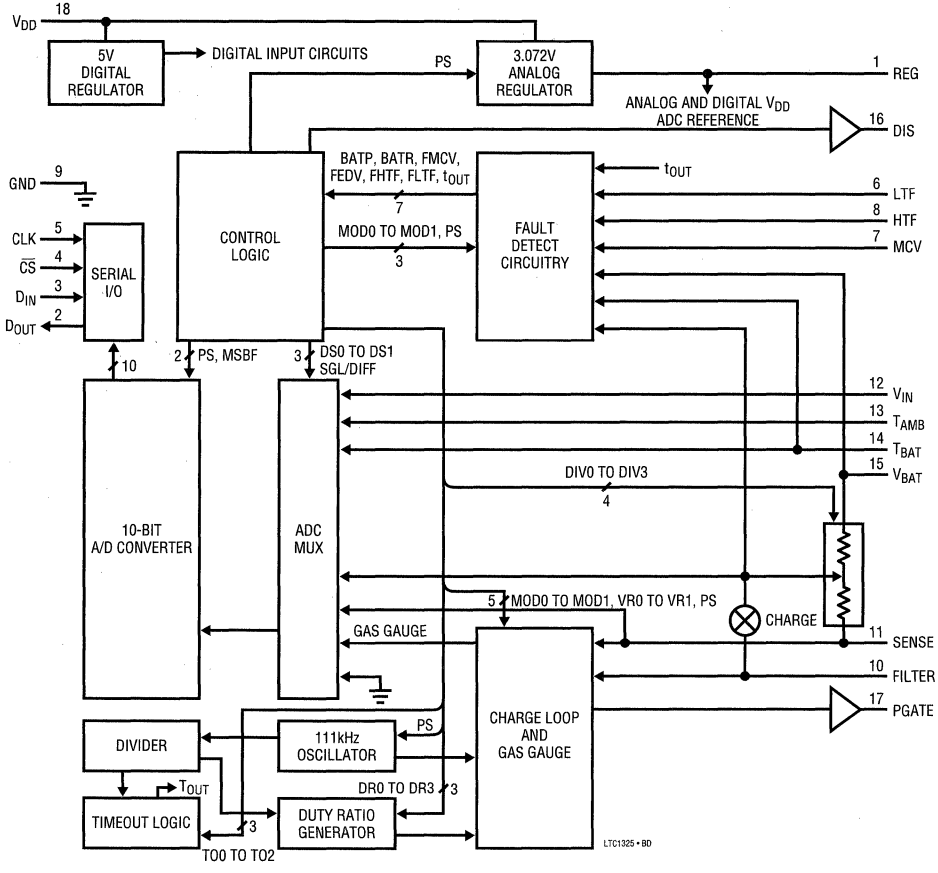
V_{BAT} (Pin 15): Battery Input. An internal voltage divider is connected between the V_{BAT} and Sense pins to normalize all battery measurements to one cell voltage. The divider is programmable to the following ratios: 1/1, 1/2, 1/3 . . . 1/15, 1/16. In shutdown and gas gauge modes the divider is disconnected.

DIS (Pin 16): Active High Discharge Control Pin. Used to turn on an external transistor which discharges the battery.

PGATE (Pin 17): FET Driver Output. Swings from GND to V_{DD}.

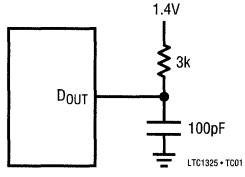
V_{DD} (Pin 18): Positive Supply Voltage. 4.5V < V_{DD} < 16V.

BLOCK DIAGRAM

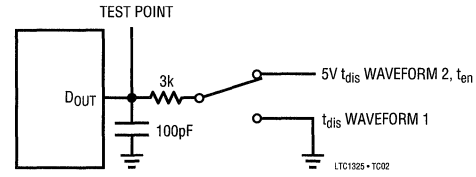


TEST CIRCUITS

Load Circuit for t_{dDO}, t_r and t_f

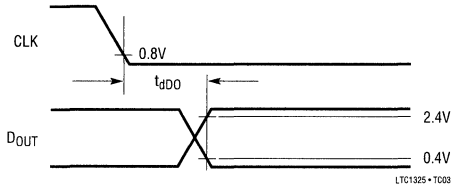


Load Circuit for t_{dis} and t_{en}

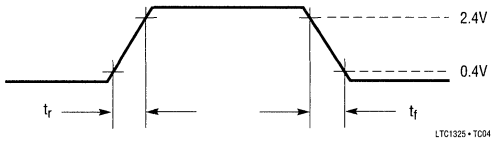


TEST CIRCUITS

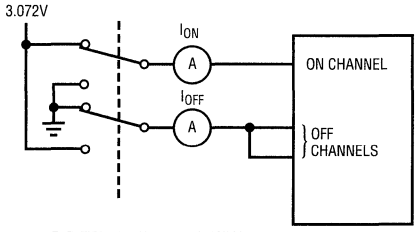
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



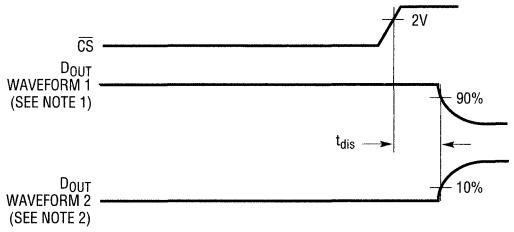
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



On and Off Channel Leakage



Voltage Waveforms for t_{dis}

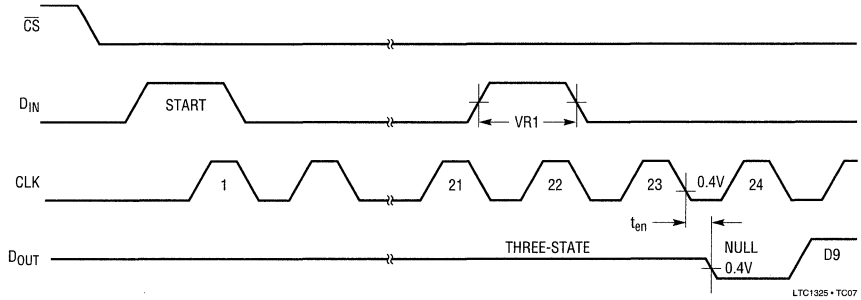


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY $\overline{CS}$.

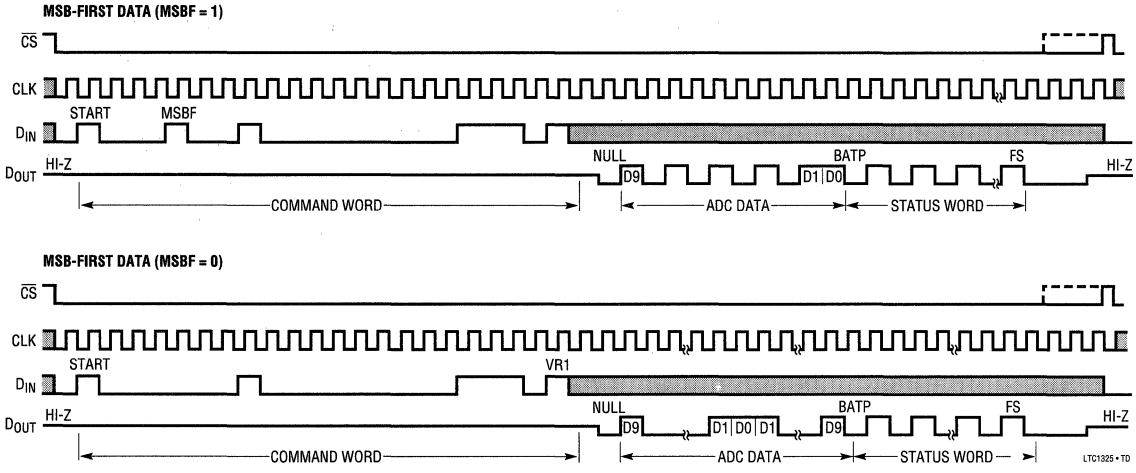
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY $\overline{CS}$.

LTC1325 • TC06

Voltage Waveforms for t_{en}



TIMING DIAGRAM



NOTE: THE TIMING DIAGRAM SHOWS TWO POSSIBLE COMMAND WORDS. REFER TO FUNCTIONAL DESCRIPTION FOR INFORMATION ON HOW TO CONSTRUCT THE COMMAND WORD

FUNCTIONAL DESCRIPTION

GENERAL DESCRIPTION

During normal operation, a command word is shifted into the chip via the serial interface, then an ADC measurement is made and the 10-bit reading and chip status word are shifted out. The command word configures the LTC1325 and forces it into one of five modes: power shutdown, idle, discharge, charge or gas gauge mode.

In the power shutdown mode, the analog section is turned off and the supply current drops to 30μA. The voltage regulator, which provides power to the internal analog circuitry and external bias networks, is shut down. The voltage divider across the battery is disconnected and only the voltage regulator for the serial interface logic is left on.

During the idle mode, the chip is fully powered but the discharge, charge, and gas gauge circuits are off. The chip may be placed in the idle mode momentarily while charging the battery, allowing an ADC measurement to be made without any switching noise from the PWM current source affecting the accuracy of the reading. The mode command bits are picked off as they appear at D_{IN}, allowing the charging loop to turn off and settle while the remainder of the command word is being shifted in.

During the discharge mode, the battery is discharged by an external transistor and series resistor. The battery is monitored for fault conditions.

In the charge mode, the μP monitors the battery's voltage, temperature and ambient temperature via the 10-bit ADC. Termination methods such as $-\Delta V_{BAT}$, $\Delta V_{BAT}/\Delta Time$, ΔT_{BAT}, $\Delta T_{BAT}/\Delta Time$, $\Delta(T_{BAT} - T_A)$, maximum temperature, maximum voltage and maximum charge time may be accurately implemented in software. The LTC1325 also monitors the battery for fault conditions.

In the gas gauge mode, the average voltage across the sense resistor can be measured to determine the average battery load current. The sense voltage is filtered by an RC circuit, multiplied by an inverting gain of four, then converted by the ADC. The μP can then accumulate the ADC measurements and do a time average to determine the total charge leaving the battery. The RC circuit consists of an internal 1k resistor R_F and an external capacitor C_F connected to the Filter pin.

FUNCTIONAL DESCRIPTION

COMMAND WORD

The command word is 22 bits long and contains all the information needed to configure and control the chip. On power-up all bits are cleared to logical "0."

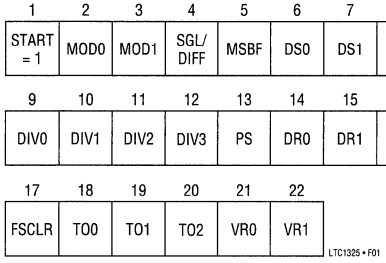


Figure 1. Command Word

Bit 1: Start Bit (Start)

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer and all leading zeros which precede this logical one will be ignored. After the start bit is received, the remaining bits of the command word will be clocked in.

Bits 2 and 3: Mode Select (MOD0 and MOD1)

The two mode bits determine which of four modes the chip will be in: idle, discharge, charge or gas gauge.

MOD1	MOD0	DESCRIPTION
0	0	Idle
0	1	Discharge
1	0	Charge
1	1	Gas Gauge

Bit 4: Single-Ended Differential Conversion (SGL/DIFF)

SGL/DIFF determines whether the ADC makes a single-ended measurement with respect to ground or a differential measurement with respect to the Sense pin.

SGL/DIFF	DESCRIPTION
0	Single-Ended ADC Conversion
1	Differential ADC Conversion (with respect to Sense)

Bit 5: MSB-First/LSB-First (MSBF)

The ADC data is programmed for MSB-first or LSB-first sequence using the MSBF bit. See Serial I/O description for details.

MSBF	DESCRIPTION
0	LSB-First Data Follows MSB-First Data
1	MSB-First Data Only

Bits 6 to 8: ADC Data Input Select (DS0 to DS2)

DS2, DS1 and DS0 select which circuit is connected to the ADC input. Do not use unlisted combinations.

DS2	DS1	DS0	DESCRIPTION
0	0	0	Gas Gauge Output
0	0	1	Battery Temperature Pin, T_{BAT}
0	1	0	Ambient Temperature Pin, T_{AMB}
0	1	1	Battery Divider Output Voltage, V_{CELL}
1	0	0	V_{IN} Pin

Bits 9 to 12: Battery Divider Ratio Select (DIV0 to DIV3)

DIV3, DIV2, DIV1 and DIV0 select the division ratio for the voltage divider across the battery.

DIV3	DIV2	DIV1	DIV0	DESCRIPTION
0	0	0	0	$(V_{BAT} - V_{SENSE})/1$
0	0	0	1	$(V_{BAT} - V_{SENSE})/2$
0	0	1	0	$(V_{BAT} - V_{SENSE})/3$
0	0	1	1	$(V_{BAT} - V_{SENSE})/4$
0	1	0	0	$(V_{BAT} - V_{SENSE})/5$
0	1	0	1	$(V_{BAT} - V_{SENSE})/6$
0	1	1	0	$(V_{BAT} - V_{SENSE})/7$
0	1	1	1	$(V_{BAT} - V_{SENSE})/8$
1	0	0	0	$(V_{BAT} - V_{SENSE})/9$
1	0	0	1	$(V_{BAT} - V_{SENSE})/10$
1	0	1	0	$(V_{BAT} - V_{SENSE})/11$
1	0	1	1	$(V_{BAT} - V_{SENSE})/12$
1	1	0	0	$(V_{BAT} - V_{SENSE})/13$
1	1	0	1	$(V_{BAT} - V_{SENSE})/14$
1	1	1	0	$(V_{BAT} - V_{SENSE})/15$
1	1	1	1	$(V_{BAT} - V_{SENSE})/16$

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FUNCTIONAL DESCRIPTION

Bit 13: Power Shutdown (PS)

PS selects between the normal operating mode, or the shutdown mode.

PS	DESCRIPTION
0	Normal Operation
1	Shutdown All Circuits Except Digital Inputs

Bits 14 to 16: Duty Ratio Select (DR0 to DR2)

DR2, DR1 and DR0 select the duty cycle of the charging loop operation (not 111kHz PWM duty cycle). The last three selections place the chip into a test mode and should not be used.

DR2	DR1	DR0	DESCRIPTION
0	0	0	1/16
0	0	1	1/8
0	1	0	1/4
0	1	1	1/2
1	0	0	1
1	0	1	Test Mode 1
1	1	0	Test Mode 2
1	1	1	Test Mode 3

Bit 17: Fail-Safe Latch Clear (FSCLR)

When FSCLR bit is set to one, the internal fail-safe timer is reset to 0, and the fail-safe latches are reset. FSCLR is automatically reset to 0 when $\overline{CS}$ goes high.

FSCLR	DESCRIPTION
0	No Action
1	Reset Fail-Safe Timer and Latches

Bits 18 to 20: Timeout Period Select (TO0 to TO2)

TO2, TO1 and TO0 select the desired fail-safe timeout period, t_{OUT}. On power-up, the default timeout is 5 minutes.

TO2	TO1	TO0	TIMEOUT (MINUTES)
0	0	0	5
0	0	1	10
0	1	0	20
0	1	1	40
1	0	0	80
1	0	1	160
1	1	0	320
1	1	1	Indefinite (No Timeout)

Bits 21 and 22: Charging Loop Reference Voltage Select (VR0 and VR1)

VR1 and VR0 select the desired reference voltage V_{CHRG} for the charging loop. The charging loop will force the average voltage at the Sense pin to be equal to V_{DAC}. The average charging current is V_{DAC}/R_{SENSE} (see Figure 4).

VR1	VR0	V_{DAC} (mV)
0	0	18
0	1	34
1	0	55
1	1	160

STATUS WORD

The status word is 8 bits long and contains the status of the internal fail-safe circuits.

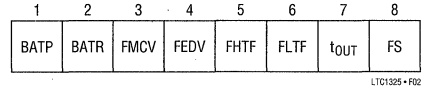

Figure 2. Status Word

Bit 1: Battery Present (BATP)

The BATP bit = 1 indicates the presence of the battery. The bit is set to 1 when the voltage at the V_{BAT} pin falls below (V_{DD} – 1.8V). BATP = 0 when the battery is removed and V_{BAT} is pulled high by R_{TRK} (see Figure 3).

BATP	CONDITIONS
0	$(V_{DD} - 1.8) < V_{BAT} < V_{DD}$
1	$V_{BAT} < (V_{DD} - 1.8)$

Bit 2: Battery Reversed (BATR) or Shorted

The BATR bit indicates when the battery is connected backwards or shorted. The bit is set when the battery cell voltage at the output of the battery divider V_{CELL} is below 100mV.

BATR	CONDITIONS
0	$V_{CELL} > 100mV$
1	$V_{CELL} < 100mV$

FUNCTIONAL DESCRIPTION

Bit 3: Maximum Cell Voltage (FMCV)

The MCV bit indicates when the battery cell voltage has exceeded the preset limit. The bit is set when V_{CELL} is greater than the voltage at the MCV pin.

FMCV	CONDITIONS
0	$V_{CELL} < V_{MCV}$
1	$V_{CELL} > V_{MCV}$

Bit 4: End Discharge Voltage (FEDV)

The EDV bit indicates when the battery cell voltage has dropped below an internally preset limit. The bit is set when the battery cell voltage at the output of the voltage divider V_{CELL} is less than 900mV.

FEDV	CONDITIONS
0	$V_{CELL} > 900mV$
1	$V_{CELL} < 900mV$

Bit 5: High Temperature Fault (FHTF)

The HTF bit indicates when the battery temperature is too high. Using a negative TC thermistor, the bit is set when the voltage at the T_{BAT} pin is less than the voltage at the HTF pin.

FHTF	CONDITIONS
0	$T_{BAT} > V_{HTF}$
1	$T_{BAT} < V_{HTF}$

Bit 6: Low Temperature Fault (FLTF)

The LTF bit indicates when the battery temperature is too low. Using a negative TC thermistor, the bit is set when the voltage at the T_{BAT} pin is greater than the voltage at the LTF pin.

FLTF	CONDITIONS
0	$T_{BAT} < V_{LTF}$
1	$T_{BAT} > V_{LTF}$

Bit 7: Timeout (t_{OUT})

The t_{OUT} bit indicates that the battery charging time has exceeded the preset limit. The bit is set when the internal timer exceeds the limit set by the command bits TO0, TO1 and TO2.

T_{OUT}	CONDITIONS
0	No Timeout Has Occurred
1	Timeout Has Occurred

Bit 8: Fail-Safe Occurred (FS)

The FS bit indicates that one of the fault detection circuits halted the discharging or charging cycle. The bit is set when an EDV, LTF, HTF, or t_{OUT} fault occurs during discharge. During charging, the bit is set when a MCV, LTF, HTF, or t_{OUT} fault occurs. The bit is reset by the command word bit FSCLR.

FS	CONDITIONS
0	No Fail-Safe Has Occurred
1	Fail-Safe Has Occurred

DETAILED DESCRIPTION

Fault Conditions

The LTC1325 monitors the battery for fault conditions before and during discharge and charge (see Figure 3). They include: battery removed/present (BATP), battery reversed/shorted (BATR), maximum cell voltage exceeded

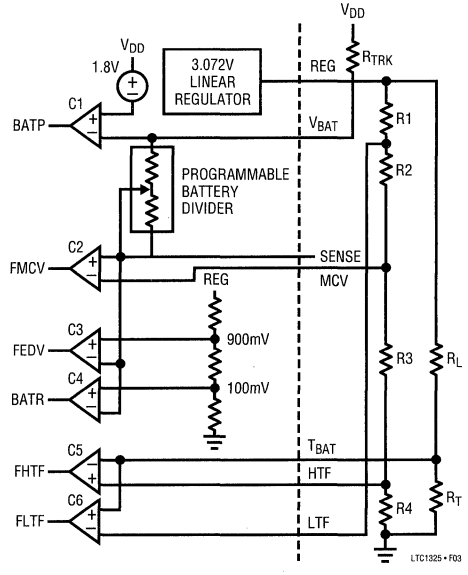

Figure 3. Fail-Safe or Fault Detection Circuitry

FUNCTIONAL DESCRIPTION

(MCV), minimum cell voltage exceeded (EDV), high temperature limit exceeded (HTF), low temperature limit exceeded (LTF) and time limit exceeded (t_{OUT}). When a fault condition occurs, the discharge and charge loops are disabled or prevented from turning on and the fail-safe bit (FS) is set. The chip is reset by shifting in a new command word with the fail-safe clear FSCLR bit set. The 8-bit status word contains the state of each fault condition.

Power Shutdown Mode

Command: MOD1 = X, MOD0 = X, PS = 1

Status: BATP = X, BATR = X, FMCV = X, FEDV = X, FHTF = X, FLTF = X, t_{OUT} = X

In the power shutdown mode, the analog section is turned off and the supply current drops to 30µA. The voltage regulator, which provides power to the internal analog circuitry and external bias networks, is shut down. The voltage divider across the battery is disconnected and the only circuit left on is the voltage regulator for the serial interface logic.

Idle Mode

Command: MOD1 = 0, MOD0 = 0, PS = 0

Status: BATP = X, BATR = X, FMCV = X, FEDV = X, FHTF = X, FLTF = X, t_{OUT} = X

The chip enters the idle mode when the proper mode command bits are set and the power shutdown command bit is cleared. During the idle mode, the chip is fully powered, but the discharge, charge and gas gauge circuits are off. The chip may be placed in the idle mode momentarily while charging the battery, allowing an ADC measurement to be made without any switching noise from the PWM current source affecting the accuracy of the reading. The mode command bits are picked off as they appear at D_{IN}, so that while the rest of the command word is being shifted in, the charging loop has time to settle before an ADC measurement is made.

Discharge Mode

Command: MOD1 = 0, MOD0 = 1, PS = 0

Status: BATP = 1, BATR = 0, FMCV = X, FEDV = 0, FHTF = 0, FLTF = 0, t_{OUT} = 0

The chip enters the discharge mode when the proper mode command bits are set and the power shutdown command bit is clear. If a fault condition does not exist, then the DIS pin is pulled up to V_{DD} by the internal driver. The DIS voltage is used to turn on an external transistor which discharges the battery through an external series resistor R_{DIS}.

Discharging will continue until a new command word is input to change the mode or a fault condition occurs.

Charge Mode

Command: MOD1 = 1, MOD0 = 0, PS = 0

Status: BATP = 1, BATR = 0, FMCV = 0, FEDV = X, FHTF = 0, FLTF = 0, t_{OUT} = 0

The chip enters the charge mode when the proper mode command bits are set and the power shutdown command bit is clear. If a fault condition does not exist then charging can begin. Charging will continue until a new command word is input to change the mode or a fault condition occurs.

The charge current may be regulated by a programmable 111kHz PWM buck current regulator, or by using the PFET to gate an external current regulator or current limited transformer.

111kHz PWM Controller

The block diagram of the charging loop connected as a PWM buck current regulator is shown in Figure 4. The PWM may operate in either continuous or discontinuous mode. The loop forces the average voltage across the sense resistor to be equal to the voltage at the output of the DAC, so that the charging current becomes V_{DAC}/R_{SENSE}.

With switch S2 on and the others off, amplifier A1 along with C1, R1 and R2 are configured as an integrator with 16kHz bandwidth. The output of the integrator is the average difference between the voltage across the sense resistor and the DAC output voltage.

The rising edge of the oscillator waveform triggers the one shot which sets the flip-flop output high. This turns on the external PFET P1 by pulling its gate low via the FET driver. With P1 on, the current through the inductor L1 starts to

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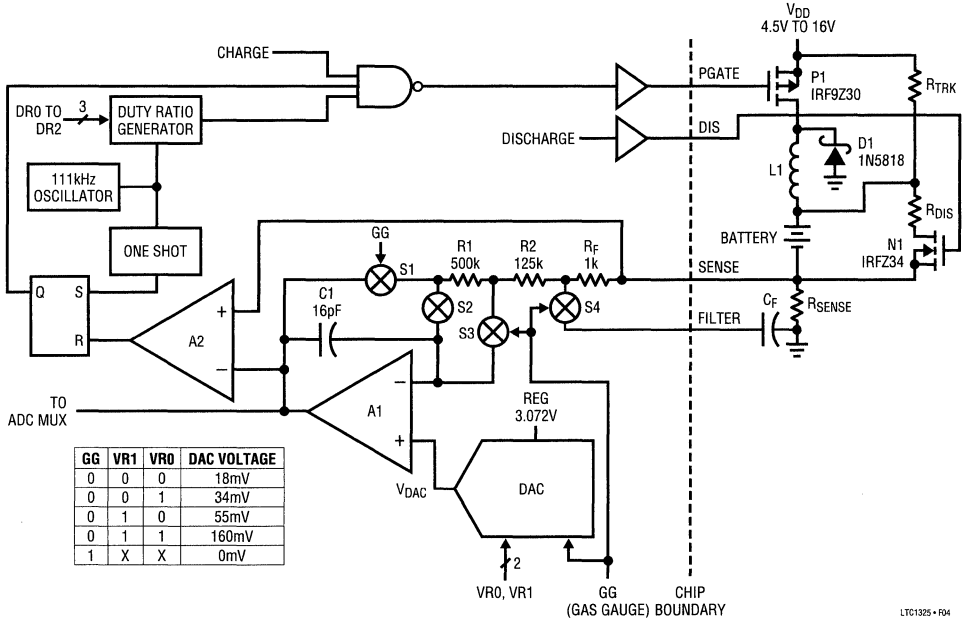

GG	VR1	VR0	DAC VOLTAGE
0	0	0	18mV
0	0	1	34mV
0	1	0	55mV
0	1	1	160mV
1	X	X	0mV

Figure 4. Charging Loop Block Diagram

ise as does the voltage across the sense resistor. When he voltage across the sense resistor is greater than the ıutput of the integrator, comparator A2 changes state. 'his resets the flip-flop and P1 is turned off. Catch diode)1 clamps the drain of P1 one diode drop below ground vhen the inductor flies back and the current through the ıductor starts to drop. The voltage across the sense esistor also drops and may reach zero and stay there until he next clock cycle begins.

'he average charging current is set by the output of the)AC (V_{DAC}) and the duty ratio generator. V_{DAC} can be ırogrammed to one of four values with the following atios: 1, 1/3, 1/5 or 1/10. The duty ratio can be set to /16, 1/8, 1/4, 1/2 or 1. When the duty ratio is 1, the duty atio generator output is always low and the charge loop ıperates continuously (see Figure 4). At other duty ratio ettings, the duty generator output is a square wave with period of 42 seconds. The time for which the generator utput is low varies with the duty ratio setting. For example, if a duty ratio of 1/2 is programmed, the generator output is low only for 42/2 = 21 seconds. Since the loop operates for only 21 out of every 42 seconds, the average charging current is halved. In general, the average charging current is:

$$I_{CHRG} = V_{DAC}(\text{Duty Ratio})/R_{SENSE}$$

Gated PFET Controller

When using an external current regulator or current limited wall pack, simply remove the inductor L1 and catch diode D1. Set the DAC control bits VR1 = 1 and VR0 = 1, and select the desired duty ratio. By insuring that the voltage at the Sense pin is never greater than 140mV, the output of the integrator A1 will saturate high and the comparator A2 will never trip and turn the loop off. This can be achieved by removing the sense resistor and grounding the Sense pin or if the gas gauge is to be used, selecting R_{SENSE} so that $R_{SENSE}/I_{CHRG} < 140mV$.

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Gas Gauge Mode

Command: MOD1 = 1, MOD0 = 1, PS = 0

Status: BATP = X, BATR = X, FMCV = X, FEDV = X, FHTF = X, FLTF = X, t_{OUT} = X

In the gas gauge mode, the average voltage across the sense resistor can be measured to determine the average battery load current. The output of the DAC is set to ground and switches S1, S3 and S4 are closed. A1 is configured as an inverting amplifier with R1 and R2 setting the gain to –4. The voltage across the sense resistor is filtered by an RC circuit (R_F, C_F) amplified by A1, then converted by the ADC.

The microprocessor can then accumulate the ADC measurements and do a time average to determine the total charge leaving the battery. The Sense pin voltage should not be more negative than –450mV to ensure linearity.

The R_FC_F circuit consists of an internal 1k resistor and an external capacitor connected to the Filter pin. R_FC_F should be longer than the measurement interval. With the serial clock running at 100kHz, it take 380µs to shift in the command word and shift out the ADC measurement and status word.

Trickle Resistor

An external trickle resistor has several functions. First, it provides a continuous trickle charge current for topping off the battery and countering the effects of self-discharge. Second, it can be used to condition a deeply discharged battery for charging. The LTC1325 will not charge a battery unless its cell voltage is above 100mV (BATR). Finally, the resistor is required by the battery detect circuit to pull the V_{BAT} pin high when the battery is removed.

SERIAL INTERFACE

The LTC1325 communicates with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface. The clock CLK synchronizes the data transfer with each bit being transmitted on the falling edge and captured on the rising CLK edge in both transmitting and receiving systems. The LTC1325 first receives input data and then transmits back the A/D conversion result and status word (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just three wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select $\overline{CS}$ signal. After $\overline{CS}$ falls, the LTC1325 looks for a start bit on D_{IN}. The start bit is the first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low. The LTC1325 will ignore all leading zeros which precede this logical one. After the start bit is received, the 21 other control bits are shifted into the D_{IN} pin to configure the LTC1325 and start a conversion. After the last command bit, the D_{OUT} pin remains in three-state for one clock period before it is taken low for one null bit. Following the null bit, the conversion results and the 8 status bits are shifted out on the D_{OUT} pin. At the end of the data exchange, $\overline{CS}$ should be brought high.

MSB-First/LSB-First (MSBF Control Bit)

The output data of the LTC1325 is programmed for MSB-first or LSB-first sequence using the MSFB control bit. When MSBF = 1, data will appear on D_{OUT} in MSB-first format. This is followed by the 8 status bits. Logical zeros will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When MSBF = 0, LSB-first data will follow the MSB-first data. Regardless of the state of MSBF, the status bits are always shifted out in the same order (see Figure 2).

Accommodating Microprocessors with Different Word Lengths

The LTC1325 will fill zeros indefinitely after the transmitted data until $\overline{CS}$ is brought high. At that time D_{OUT} is disabled (three-stated). This makes for easy interfacing to MPU serial ports with different transfer increments including 4 bits (e.g., COP400) and 8 bits (e.g., SPI and MICROWIRE/PLUS™). Any word length can be accommodated by the correct positioning of the start bit in the input word.

Operation with D_{IN} and D_{OUT} Tied Together

The LTC1325 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to

MICROWIRE/PLUS is a trademark of National Semiconductor Corp.

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communicate with the microprocessor. Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1325 will take control of the data line and drive it low after the 23rd falling CLK edge after the start bit is received. Therefore the processor port must be switched to an input before this happens to avoid a conflict.

Power-Up After Shutdown

When a control word with the PS bit set to one is written to the LTC1325, it enters shutdown mode in which the V_{DD} supply current is reduced to 30µA. In this mode the on-chip 3V regulator and all circuits powered off it are shut down. The only circuits that remain alive are D_{IN}, $\overline{CS}$ and CLK input buffers. To take the LTC1325 out from shutdown mode, a high to low edge must be applied to the $\overline{CS}$ pin. Either D_{IN} or CLK must be low when $\overline{CS}$ is low to prevent a false control word from being transmitted to the LTC1325. The 3V output decays with a time constant of 300ms with C_{REG} = 4.7µF. The microprocessor should wait three seconds before applying a wake-up edge to the $\overline{CS}$ pin to ensure proper power-up.

TEMPERATURE SENSING

NTC (Negative Temperature Coefficient) Thermistors

The simplest method to sense temperature (battery or ambient) with an NTC thermistor is to use a voltage divider powered by the REG pin. This divider consists of a load resistor R_L in series with a thermistor R_T as shown in Figure 3. For a given thermistor, there is a value of R_L which makes V_{DIV} (T) linear over a narrow but adequate temperature range. The easiest method (Inflection Point Method) to calculate R_L is to set the second temperature derivative of the divider output to 0. The equations relevant to this method are:

$$\frac{V_{DIV}(T)}{V_{REG}} = \frac{1}{\left(\frac{1+R_L}{R_T}\right)} = f(T) \quad (1)$$

$$\frac{R_T}{R_{TO}} = \exp\left[\beta\left(\frac{1}{T}-\frac{1}{T_O}\right)\right] \quad (2)$$

$$R_L = R_{TO}\left(\frac{\beta-2T_O}{\beta+2T_O}\right) \quad (3)$$

$$\beta = \left[T\left(\frac{T_O}{T_O-T}\right)\right]\ln\left(\frac{R_T}{R_{TO}}\right) \quad (4)$$

$$\alpha = \frac{1}{R_T}\left(\frac{dR_T}{dT}\right) \quad (5)$$

$$\alpha = \frac{-\beta}{T^2} \quad (6)$$

$$\frac{dV_{DIV}}{dT} = V_{DIV}(T_O)\left(-\frac{-\beta}{2T_O{}^2}+\frac{1}{T_O}\right) \quad (7)$$

where,

V_{DIV} (T) is the output of the divider,

V_{REG} is the voltage at the REG pin (3.072V nominal),

R_T is the thermistor resistance at some temperature T,

R_{TO} is the thermistor resistance at some reference temperature T_O,

β is a constant dependent on thermistor material,

α is the temperature coefficient (in %/°C) of R_T at T_O, and

all temperatures are in °K (i.e., T°C + 273)

There are two assumptions in the derivation of the above equations. β is assumed to be constant and the temperature coefficient of R_L is small compared to that of the thermistor.

Most thermistor data sheets specify R_{TO}, β, R_T/R_{TO} ratios for two temperatures, α, and tolerances for β and R_{TO}. Given β, and R_{TO}, it is easy to calculate R_L from equation

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(3). Alternatively, β may be calculated from the R_T/R_{TO} ratio using equation (4) or from α, using equation (6).

As a numerical example, consider the Panasonic ERT-D2FHL103S thermistor which has the following characteristics:

1. R_T (25°C) = R_{TO} = 10k
2. α = −4.6%/°C at T_O = 25°C
3. Ratio R_{25}/R_{50} = 2.9

Using equation (4) and R_{25}/R_{50} = 2.9, β = (323 × 298)ln (2.9)/(298 − 323) = 4099k. Alternatively, using equation (6) and α = −4.6%/°C, β = −(−0.046)$(298)^2$ = 4085k.

Both values of β are close to each other. Substituting β = 4085k into equation (3) gives R_L = 10k [4085 − (2 × 298)]/[4085 + (2 × 298)] = 7.45k. The nearest 1% resistor value is 7.5k. Figure 5 shows a plot of $V_{DIV}(T)$ measured at various temperatures for this thermistor with a 7.5k R_L.

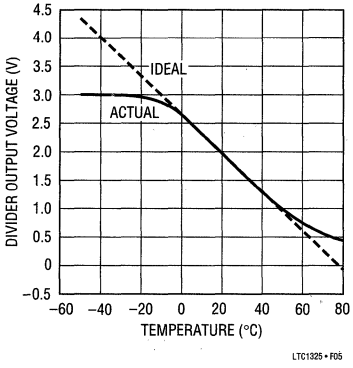

Figure 5. ERT-D2FHL103S Divider

There are two methods of calculating battery or ambient temperature from ADC readings of the T_{BAT} or T_{AMB} channels. The first method is to store the $V_{DIV}(T)$ vs T curve as a lookup table. The second method is to use a straight line approximation. The equation of this line may be calculated from the slope dV_{DIV}/dT at T_O [see equation (7)] and assuming that the line passes through the point $[T_O, V_{DIV}(T_O)]$ on the curve. For the ERT-D2FHL103S, the slope is minus 34mV/°C and the equation of the line is T = [2.605 − $V_{DIV}(T)$]/0.034. The straight line approximation is accurate to within 2°C over a temperature range of 5°C to 45°C, assuming 3% β and 10% R_{TO} tolerances.

PTC (Positive Temperature Coefficient) Thermistors

Positive Temperature Coefficient (PTC) thermistors may be used in battery chargers that do not require accurate temperature measurements. The resistance vs temperature characteristics of PTC exhibits a sharp increase at a selectable switch temperature T_S. This sharp change is exploited in chargers which use TCO (Temperature Cutoff) or ΔTCO (Difference between battery and ambient temperature). With TCO termination, a voltage divider consisting of a PTC and a low temperature coefficient load resistor is connected between REG and GND with the top end of the PTC at REG. The PTC is mounted on the battery to sense its temperature. The divider output is tied to T_{BAT}. When the switch temperature is reached, the PTC resistance increases sharply causing T_{BAT} to fall below HTF. This causes an HTF fault and charging is terminated. To implement ΔTCO termination, the load resistor can, in principle, be replaced by a matching PTC and the divider now responds to differences between battery and ambient temperature. With both TCO and ΔTCO terminations, the position of the battery temperature PTC can be swapped with the load resistor or ambient temperature PTC. In both cases, an LTF fault terminates charge when the trip point is reached. Note that in practice, matched PTCs are not readily available and for ΔTCO termination, NTC thermistors are recommended.

HARDWARE DESIGN PROCEDURE

This section discusses the considerations in selecting each component of a simple battery charger (see Figures 3 and 4). Further applications assistance is provided in Application Note 64, using the LTC1325 Battery Management IC.

1. R_{SENSE}: There are three factors in selecting R_{SENSE}:
   a. LTC1325 V_{REF} and Duty Ratio Settings
   b. Sense Resistor Dissipation
   c. $I_{LOAD}(R_{SENSE})$ < −450mV for Gas Gauge Linearity

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The LTC1325 has five duty ratio and four V_{DAC} settings giving 20 possible charge rates (for a given value of R_{SENSE}) as shown in the following table. For any combination of V_{DAC} and duty ratio, the average charging current is given by:

$$AVG\ I_{CHRG} = V_{DAC}(Duty\ Ratio)/R_{SENSE}$$

NORMALIZED V_{DAC}	DUTY RATIO				
	1	1/2	1/4	1/8	1/16
1(VR1 = 1, VR0 = 1)	1	1/2	1/4	1/8	1/16
1/3(VR1 = 1, VR0 = 0)	1/3	1/6	1/12	1/24	1/48
1/5(VR1 = 0, VR0 = 1)	1/5	1/10	l/20	1/40	1/80
1/10(VR1 = 0, VR0 = 0)	1/10	1/20	1/40	1/80	1/160

Note that the table entries give relative charge rates assuming that the VR1 = 1, VR0 = 1, duty ratio = 1 entry is equivalent to a 1C charge rate. Therefore, the charge rate (in C-units) for other VR1, VR0, and duty ratio settings may be read directly from the table. In general, the VR1 = 1, VR0 = 1, duty ratio = 1 entry can be equivalent to any charge rate, say k times 1C. Then all entries in the table should be multiplied by k. In general, V_{DAC} and duty ratio settings are changed by the microprocessor to charge batteries of different capacities or to alter charge rates when charging the same battery in several stages. For best accuracy, VR1 and VR0 should be set to 1 where possible.

The power dissipation of the sense resistor varies between charge, discharge and gas gauge modes and should be calculated for all three modes. Typically, dissipation is higher in discharge and gas gauge modes since batteries can deliver higher currents than they can be charged with.

In gas gauge mode, the load current supplied by the battery should not exceed $450mV/R_{SENSE}$ for the gas gauge to remain linear in response. R_{SENSE} should be low enough to ensure that $I_{LOAD}(R_{SENSE})$ does not fall below ground by more than 1 diode drop.

2. V_{DD} Supply: V_{DD} should be at least 1.8V above the maximum battery voltage to prevent a BATP = 0 error when the LTC1325 is in charge or discharge mode. If this requirement cannot be met in a specific application, an external battery divider should be connected between the V_{BAT} and Sense pins and the internal divider should be set to divide-by-1.

   The minimum V_{DD} supply must be greater than the end-of-charge voltage V_{EC} times the number of cells (n) in the battery plus drops across the on-resistance of the PFET, inductor (V_L), battery internal resistance R_{INT} and sense resistor R_{SENSE}.

   Minimum V_{DD} should be the greater voltage of the results from these two equations:

   $$Min\ V_{DD} = I_{CHRG}[R_{DS(ON)}(P1) + R_{SENSE} + n(R_{INT})] + n(V_{EC}) + V_L$$

   or,

   $$Min\ V_{DD} = n(V_{EC}) + 1.8V$$

   Assuming V_{EC} = 1.6V, the LTC1325 will charge up to 8 cells with a 16V supply. For a higher number of cells, an external level shifter and regulator are needed.

   In some applications, there are other circuits attached to the charging supply. When the charging supply (V_{DC}) is powered down or removed, the battery may supply current to these circuits through the PFET body diode. To prevent this, a blocking diode can be added in series with V_{DC} as shown in the circuit in the Typical Application section.

3. Inductor L: To minimize losses, the inductor should have low winding resistance. It should be able to handle expected peak charging currents without saturation. If the inductor saturates, the charging current is limited only by the total PFET $R_{DS(ON)}$, inductor winding resistance, R_{SENSE} and V_{DD} source resistance. This fault current may be high enough to damage the battery or cause the maximum power ratings of the PFET, inductor or R_{SENSE} to be exceeded.

4. Catch Diode D1: The catch diode should have a low forward drop and fast reverse recovery time to minimize power dissipation. Total power loss is given by:

   $$P_{dD1} = V_F(I_F) + (V_R)(f)(t_{RR})(I_F')$$

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where,

I_F = forward diode current,

I_F' = forward diode current just prior to turn off,

V_F = forward drop,

V_R = reverse diode voltage (approximately equal to V_{DD}),

f = PWM frequency (111kHz), and

t_{RR} = reverse recovery time

The power and maximum reverse voltage ratings of the diode should be greater than P_{dD1} and V_{DD} respectively. The catch diode should also have fast turn-on times to reduce the voltage glitch at its cathode when turning on.

Schottky diodes have fast switching times and low forward drops and are recommended for D1.

5. Trickle Resistor R_{TRK}: R_{TRK} sets the desired trickle current in the battery to compensate for self-discharge which is in the order 1% and 2% of capacity per day for NiCd and NiMH batteries respectively. Trickle charge rates are typically in the C/30 to C/50 range, where C is battery capacity.

   $I_{TRK} = (V_{DD} - V_{BAT})/R_{TRK}$

   where V_{BAT} is the voltage of a full charged battery. Note that I_{TRK} varies as the battery is being charged.

6. Thermistor R_T and Load R_L: The total resistance of the thermistor network should be greater than 30k at the high temperature extreme to minimize effects of load regulation (see REG pin loading).

7. Fault Setting Resistors R1, R2, R3 and R4: The voltage levels at the LTF, HTF and MCV pins are tapped from a resistor divider powered by the REG pin. The voltage levels are selected taking into account:

   a. Manufacturer Recommended Temperature and Voltage limits,

   b. Loading on the REG Pin (< 2mA)

   c. Input Voltage Ranges of the LTF, HTF and MCV Comparators:

   $1.6V < V_{LTF}, V_{MCV} < 2.8V$ and $0.5V < V_{HTF} < 1.3V$

d. Thermistor Divider Temperature Curve

Typical temperature limits for both NiCd and NiMH batteries are shown below.

BATTERY TYPE	DISCHARGE TEMP RANGE (°C)		CHARGE TEMP RANGE (°C)	
	MIN	MAX	MIN	MAX
Standard	–20	45 to 50	0	45 to 50
Quick	–20	45 to 50	10	45 to 50
Fast or Rapid	–20	45 to 50	15	45 to 50
Trickle	–20	45 to 50	0	45 to 50

Note that the discharge limits are wider than the charge limits. To prolong battery life, manufacturers generally recommend discharge temperatures that are similar to the charge limits. For this reason, the LTC1325 recognizes the same LTF and HTF limits in both charge and discharge modes. MCV should be set just above the charging voltage per cell given in battery specifications. The voltage at the LTF and HTF pins should be set to correspond to narrowest temperature range. These are typically 15°C and 45°C. The corresponding voltages may be read from the thermistor divider temperature curve such as that shown in Figure 5. For this thermistor, it works out to be about for 2.12V for LTF and for 1.13V for HTF. The MCV may be conveniently tied to LTF since MCV is typically 2V. If desired, external analog switches under microprocessor control may be used to vary the LTF, HTF and MCV voltages between modes or for different charge rates. The values of R1, R2, R3 and R4 in Figure 3 can be calculated from the following equations:

$R4 = V_{HTF}(RE/V_{REG})$

$R3 = V_{MCV}(RE - R4)$

$R2 = V_{LTF}(RE) - (R3 + R4)$

$R1 = RE - (R2 + R3 + R4)$

where RE = R1 + R2 + R3 + R4 is chosen to minimize loading on the REG pin. A minimum value of 30k is recommended. Note that V_{LTF} is assumed to be greater than V_{MCV}. If this is not the case, V_{LTF} and V_{MCV} in the above equations should be swapped. If the MCV and LTF pins are shorted to the same point, R2 should be set to 0.

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8. REG Pin Loading: The 3.072V regulator has a load regulation specification of –5mV/mA. Since the ADC uses the same regulator as reference, it is desirable to reduce loading effects on the REG pin especially over temperature. Thermistors with R_{TO} values of at least 10k at 25°C are recommended. At 50°C, the thermistor resistance could drop by a factor of 3 from its value at 25°C. R_L is chosen as explained in the section on Temperature Sensing. The temperature coefficient of R_L is not critical since the thermistor tempco dominates the sensing circuit.

9. R_{DIS}: R_{DIS} is selected to limit the discharge current to a value within the battery discharge specifications and must have a power rating above $I_{DIS}^2(R_{DIS})$ where:

   $I_{DIS} = V_{BAT}/[R_{DIS} + R_{DS(ON)}(N1)]$

10. PFET(P1) and NFET(N1): For operation of the charge and discharge loops, $|V_{GS}| < V_{DD}$ since the PGATE and DIS pins swing between 0 and V_{DD}. $|V_{GS}| \ll V_{DD}$ to minimize power dissipation. The power ratings of P1 and N1 should be above $I_{CHRG}^2[R_{DS(ON)}(P1)]$ and $I_{DIS}^2[R_{DS(ON)}(N1)]$ respectively. $V_{DS(MAX)}$ should be above V_{DD}.

Charging from Supplies Above 16V

In many applications, the charging supply is greater than the 16V maximum V_{DD} rating of the LTC1325. The LTC1325 can easily be adapted to charge the batteries from a charging supply V_{DC} that is above 16V by adding three external sub-circuits:

1. A regulator to drop V_{DC} down to within the supply range of the LTC1325.
2. A level shifter between the PGATE and the gate of the PFET, P1, to ensure that P1 can be completely turned off when PGATE rises to V_{DD}.
3. A voltage clamp on the V_{BAT} pin to prevent R_{TRK} from pulling V_{BAT} above V_{DD}.

The Wide Voltage Battery Charger circuit in the Typical Application section shows low cost implementations of all three sub-circuits. C1, R11 and D4 generate a 15V V_{DD} for the LTC1325. D3, R12 and C2 form a level shifter. The zener D3 is chosen to clamp the source gate voltage of the PFET to within the maximum gate source voltage rating of the latter. Finally, D2 clamps V_{BAT} to 15V.

Charging Batteries with Voltages Above 16V

To charge a battery with a maximum (fully charged) voltage of above 16V, the charging supply V_{DC} must be above 16V. Thus the charger will need the regulator, level shifter and clamp mentioned in the previous section. In addition, an external battery divider must be added to limit the voltage at the V_{BAT} pin to less than V_{DD}. This is shown in the typical application circuit, Wide Voltage Battery Charger. The resistors R9 and R10 are selected to divide the battery voltage by the number of cells in the battery and the battery divider internal to the LTC1325 is set to divide-by-1. The external divider prevents V_{BAT} from ever rising to V_{DD} and this causes the BATP (Battery Present Flag) to be high regardless of whether the battery is physically present or not. This does not affect the other operations of the LTC1325.

4

SOFTWARE DESIGN

A general charging algorithm consists of the following stages:

Discharge Before Charge

Fast Charge

Top Off Charge

Trickle Charge

Under some operating and storage conditions, NiCd and NiMH batteries may not provide full capacity. In particular, repeated shallow charge and discharge cycles cause the "memory effect" in NiCd batteries. In order to restore full capacity (battery conditioning), these batteries have to be subjected to several deep discharge/charge cycles which will be provided by repetitions of the above algorithm.

Figure 6 shows a simplified flowchart of a charging algorithm. In practice, this flowchart has to be augmented to take into account the occurrence of fail-safes at any point in the algorithm. For example, the battery temperature could rise above HTF during discharging or charging. General programming notes are as follows:

1. The start bit is always high.
2. The SGL/DIFF bit is generally set to low so that the ADC makes conversions with respect to ground.

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3. The MSBF bit is set depending on whether the microprocessor clocks in serial data with MSB- or LSB-first.
4. The DS0 to DS2 bits can be anything except when entering idle mode or when requesting for ADC readings. In these cases, DS0 to DS2 are set to select the desired reading: T_{BAT}, V_{CELL} or T_{AMB}.
5. The PS bit should always be 0 so that the LTC1325 does not go into shutdown mode.
6. The DR0 to DR2 should not select any of the test modes. It may assume different settings between Fast charge and Top Off charge in order to alter the charging current.
7. The FSCLR bit should be set to 1 to clear any faults and reset the timer when starting Discharge, Fast charge or Top Off. The status bits that the LTC1325 returns during the same I/O operation (that FSCLR is set to 1) should be checked to determine if faults were indeed cleared, i.e., discharging or charging has begun. This is not shown in the simplified flowchart of Figure 6. For commands other than the START commands, FSCLR should be set to 0 so as not to reset the timer.
8. The TO0 to TO2 bits should all be set to 1 in discharge mode to ensure discharge does not end prematurely due to a timeout fault. During Fast charge or Top Off charge, these bits are set to a value suitable for the charge rate used. For example, if the charge rate is 1C, the timeout period should be set to 80 minutes.
9. In charge mode, the C_F capacitor filters the V_{CELL} node and sees a small ripple due to ripple at the Sense pin. Prior to taking an ADC reading, the LTC1325 is put in

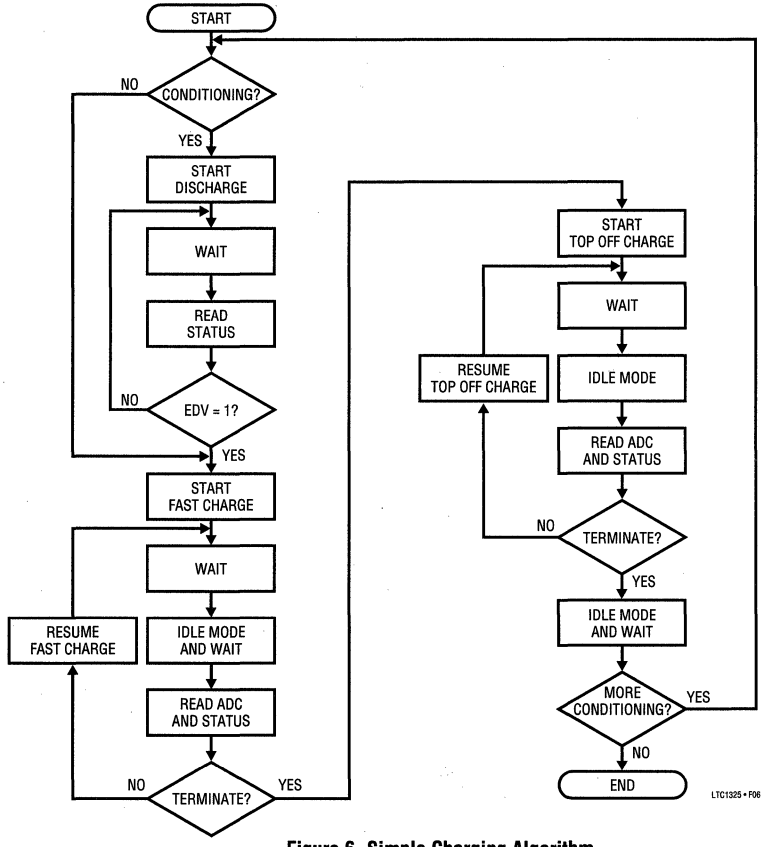


Figure 6. Simple Charging Algorithm

APPLICATIONS INFORMATION

idle mode to minimize noise. The microprocessor should either disregard readings or wait for a second or so before taking a reading. This is to allow V_{CELL} to decay to the correct cell voltage. The worst case time constant is 150kΩ(C_F).

10. Prior to the first START command, the battery divider setting may be incorrect so that C_F may charge to a voltage that causes EDV, BATR or MCV faults. The worst case time constant is as in (9). The microprocessor should check faults during the transmission of a START command and resend the START command again when C_F has been given enough time to charge up to the correct value.

MICROPROCESSOR INTERFACES

The LTC1325 can interface directly to either synchronous, serial or parallel I/O ports of most popular microprocessors. With a parallel port, 3 or 4 I/O lines can be programmed to form a serial link to the LTC1325.

Motorola SPI (68HC11)

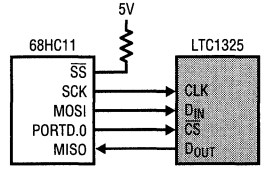
The 68HC11 has a dedicated synchronous serial interface called the Serial Peripheral Interface (SPI) which transfers data with MSB-first and in 8-bit increments. To communicate with this microprocessor, the LTC1325 MSBF control bit should be set to 1. The SPI has four lines: Master In Slave Out (MISO), Master Out Slave In (MOSI), Serial Clock (SCK) and Slave Select ($\overline{SS}$). The 68HC11 is configured as a Master by tying the $\overline{SS}$ line high. A control byte is written to the Serial Peripheral Control Register (SPCR) to select master mode, set baud rate and clock timing relationship. Another byte is written to the Port D Direction Register (DDRD) to set MOSI, SCK and bit 0 ($\overline{CS}$ of LTC1325) as outputs. The 68HC11 clocks in data from the LTC1325 simultaneously under the control of SCK. The microprocessor transmits the LTC1325 command word in 4 bytes. This is followed by 2 more dummy bytes (with all bits set low) in order to clock in the remaining LTC1325 ADC and status bits.

This software example allows you to verify communications with the LTC1325. The command word configures the LTC1325 to perform an A/D conversion on the general purpose V_{IN} input. V_{IN} can be tied to GND or REG or to a wiper on a potentiometer between these two. Table 1 illustrates a complete 6-byte exchange. Note that the first byte is padded with zeroes to align the A/D data and status with byte boundaries.

SPCR = (SPIE = 0, SPE = 1, DWOM = 0, MSTR = 1, CPOL = 0, CPHA = 0, SPR1 = 0, SPR0 = 1)

DDRD = (BIT7 = 0, BIT6 = 0, DDR5 = 1, DDR4 = 1, DDR3 = 1, DDR2 = 0, DDR1 = 0, DDR0 = 1)

Table 1. 6-Byte Exchange SPI Communication with LTC1325



0	0	0	0	0	0	START	MOD0	BYTE #1 TX
X	X	X	X	X	X	X	X	BYTE #1 RX
MOD1	SGL/ DIFF	MSBF	DS0	DS1	DS2	DIV0	DIV1	BYTE #2 TX
X	X	X	X	X	X	X	X	BYTE #2 RX
DIV2	DIV3	PS	DR0	DR1	DR2	FSCLR	TO0	BYTE #3 TX
X	X	X	X	X	X	X	X	BYTE #3 RX
TO1	TO2	VR0	VR1	0	0	0	0	BYTE #4 TX
X	X	X	X	X	0	D9	D8	BYTE #4 RX
X	X	X	X	X	X	X	X	BYTE #5 TX
D7	D6	D5	D4	D3	D2	D1	D0	BYTE #5 RX
X	X	X	X	X	X	X	X	BYTE #6 TX
BATP	BATR	FMCV	FEVD	FHTF	FLTF	t_{OUT}	FS	BYTE #6 RX

X = DON'T CARE

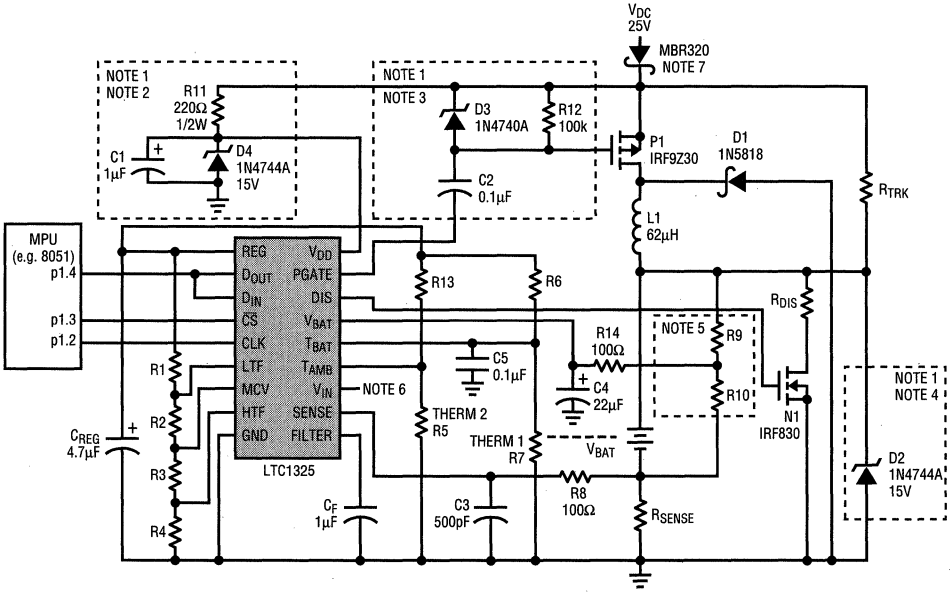
LTC1325 • AI01

APPLICATIONS INFORMATION

LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$51	Write control byte to the SPCR	LOOP4	TST	$1029	Check for SPI transfer
	STAA	$1028			BPL	LOOP4	complete bit
	LDAA	#$39	Setup Port D DDRD		LDAA	$102A	Get A/D high byte
	STAA	$1009	Port D Bit 0 is $\overline{CS}$		ANDA	#$03	Mask off unwanted bits
	LDX	#$1000	Load port base ADDR		STAA	HIDATA	Store in user memory
CSLOW	BCLR	$08,X,#$01	Take $\overline{CS}$ low		LDAA	#$00	Send dummy Byte #1
	LDAA	#$02	Send Byte #1 (MSB) with		STAA	$102A	
	STAA	$102A	START bit	LOOP5	TST	$1029	Check for SPI transfer
LOOP1	TST	$1029	Check for SPI transfer		BPL	LOOP5	complete bit
	BPL	LOOP1	complete bit		LDAA	$102A	Get A/D low byte
	LDAA	#$24	Send Byte 2		STAA	LODATA	Store in user memory
	STAA	$102A			LDAA	#$00	Send dummy Byte #2
LOOP2	TST	$1029	Check for SPI transfer		STAA	$102A	
	BPL	LOOP2	complete bit	LOOP6	TST	$1029	Check for SPI transfer
	LDAA	#$03	Send Byte 3		BPL	LOOP6	complete bit
	STAA	$102A			LDAA	$102A	Get STATUS byte
LOOP3	TST	$1029	Check for SPI transfer		STAA	STATUS	Store in user memory
	BPL	LOOP3	complete bit		BSET	$08,X,#$01	Raise $\overline{CS}$ high
	LDAA	#$C0	Send Byte 4		BRA	CSLOW	Loop for continuous readings
	STAA	$102A					

TYPICAL APPLICATION

Wide Voltage Battery Charger



NOTE 1: NEEDED WHEN V_{DC} > 16V OR MAXIMUM BATTERY VOLTAGE, V_{BAT} > 16V.

NOTE 2: REGULATOR. OMIT THIS BLOCK AND SHORT VDD TO V_{DC} WHEN V_{DC} < 16V.

NOTE 3: LEVEL SHIFTER. OMIT THIS BLOCK AND SHORT PGATE TO P1 GATE WHEN V_{DC} < 16V.

NOTE 4: ZENER TO CLAMP V_{BAT} TO BELOW V_{DD}. OMIT WHEN V_{DC} < 16V.

NOTE 5: EXTERNAL BATTERY DIVIDER. NEEDED WHEN MAXIMUM BATTERY VOLTAGE, V_{BAT} > 16V.

NOTE 6: V_{IN} IS AN UNCOMMITTED A/D CHANNEL.

NOTE 7: OPTIONAL DIODE TO PREVENT BATTERY DRAIN WHEN THE CHARGING SUPPLY IS POWERED DOWN (SEE SECTION 2, HARDWARE DESIGN PROCEDURE).

1325 TA02

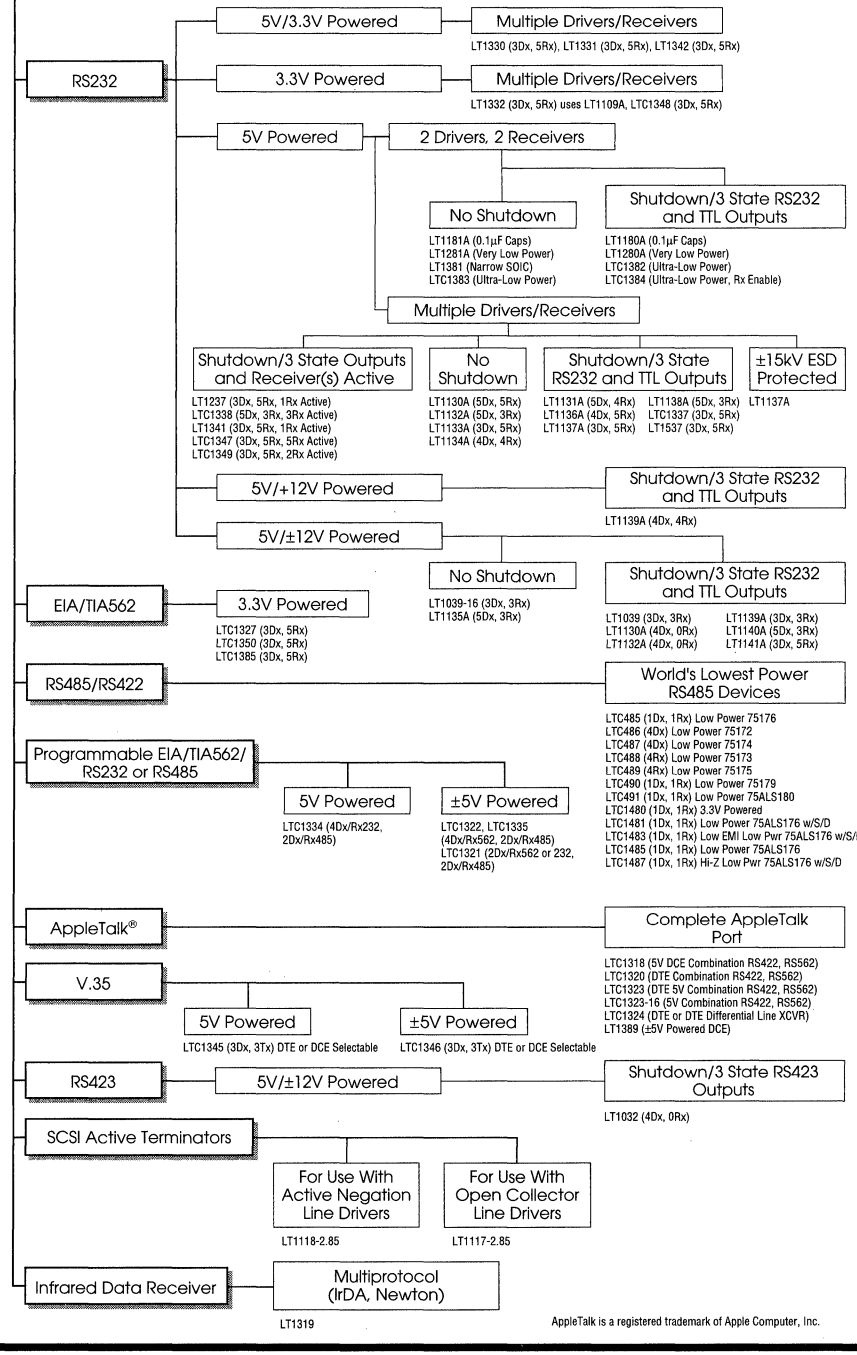
RELATED PARTS

ART NUMBER	DESCRIPTION	COMMENTS
T®1510	Constant Voltage/Constant Current Battery Charger	1.3A, Li-Ion, NiCd, NiMH, Pb-Acid Charger
T1512	SEPIC Constant Current/Constant Voltage Battery Charger	0.75A, V_{IN} Greater or Less Than V_{BAT}

SECTION 5—INTERFACE

SECTION 5—INTERFACE

INTERFACE



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5

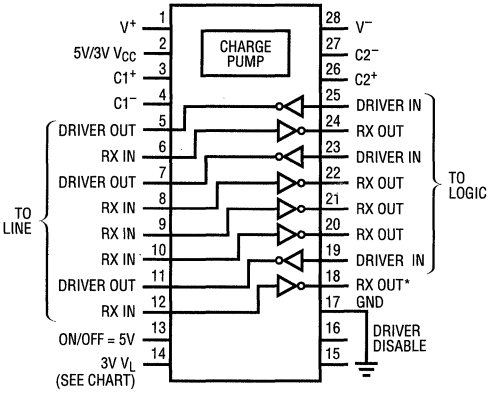
Complete RS232 PC Serial Ports: 3 Drivers, 5 Receivers

- ±15kV ESD Protection (LT1137A)
- ±10kV ESD Protection (All Others)
- 3V Logic Compatible
- Receiver Keep-Alive in Shutdown
- SO, SSOP Packages
- Ultra-Low Power (LTC1337: 1.5mW)
- Flowthrough Architecture
- 0.1µF Capacitors
- Low Power Shutdown
- 120kBaud Operation
- Capable of Mouse Driving
- 3.3V or 5V Powered

SUPPLY VOLTAGE	3V OR 5V LOGIC	TYP POWER DISS(mW)	Rx ACTIVE IN SHDN	I_Q IN SHDN (µA)	DRIVER DISABLE	10kV ESD	0.1µF CAPS	DEVICE TYPE
5	5	60	0	1	X	X†	X	LT1137A
5	5	30	1	60	X	X	X*	LT1237
3	3	1.5	0	1	—	X	X	LTC1327
5 & 3	3	30	1	60	X	X	X*	LT1330
3	3	42	1	60	X	X	X	LT1331
5 & 3	3	34	1	60	X	X	X*	LT1331
3	3	1.5	1	70	—	X	X	LT1332**
5	5	1.5	0	1	—	X	X	LTC1337
5	5	60	1	60	X	X	X	LT1341
5 & 3	3	60	0	1	X	X	X	LT1342
5	5	1.5	5	80	—	X	X	LTC1347
3	3	1.5	0 or 5	0.2 or 10	—	X	X	LTC1348
5	5	1.5	2	35	—	X	X	LTC1349
3	3	1.5	2	35	—	X	X	LTC1350
5	5	40	0	1	X	X	X	LT1537

*Requires one 1µF capacitor
** Works with switching power supply to generate full RS232 output levels from 3V supplies
† 15kV ESD protection

Typical Pin Configuration†



* REMAINS ALIVE IN SHUTDOWN DEPENDING ON PART TYPE
† EXCEPT LT1332 AND LTC1348

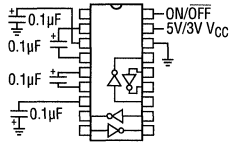
IC11

5V Powered RS232 2 Driver/2 Receiver Circuits

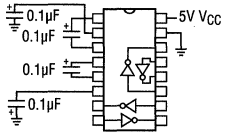
- Rugged Bipolar Construction
- ±10kV ESD Protection
- 0.1µF Charge Pump Capacitors
- Immune to Latch-Up
- Low Power Shutdown
- Three-State Outputs When Shut Down

SHUTDOWN/ RS232 AND TTL THREE-STATE OUTPUTS	FAULT TOLERANT TO ±25V	COMMENTS	PART NUMBER
Yes	Yes	Ideal for Surface Mount, 10kV ESD	LT1180A
No	Yes	Replaces MAX202, 232A, 10kV ESD	LT1181A
Yes	Yes	Low Power LT1080	LT1280A
No	Yes	Low Power LT1081	LT1281A
No	±15V	Replaces MAX202	LT1381*
Yes	Yes	Ultra-Low Power LT1180A	LTC1382
No	Yes	Ultra-Low Power LT1181A, MAX232A Replacement	LTC1383*
Yes	Yes	Ultra-Low Power LT1180A w/ 2Rx Alive in SHDN	LTC1384
Yes	Yes	Ultra-Low Power 3V LT1180A	LTC1385
No	Yes	Ultra-Low Power 3V LT1181A	LTC1386*

*Narrow 16-lead SO package



LT1180A, LT1280A, LTC1382/4/5
2 Dx, 2 Rx



LT1181A, LT1281A, LT1381, LTC1383
2 Dx, 2 RX

Other RS232 Driver/Receiver Combinations

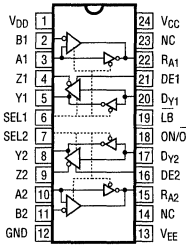
DRIVERS	RECEIVERS	SUPPLIES REQUIRED	SHUTDOWN/ RS232 and TTL THREE-STATE OUTPUTS	FAULT TOLERANT to ±25V	REQ'D CHARGE PUMP CAP SIZE	COMMENTS	PART NUMBER
4	0	±12V	Yes	Yes	N/A	Low Power 1488 Upgrade	LT1030
4	0	±12V	Yes	Yes	N/A	Low Power 1488 Upgrade Also Supports RS423	LT1032
3	3	5V, ±12V	Yes	Yes	N/A	One Receiver Active in Shutdown	LT1039
3	3	5V, ±12V	No	Yes	N/A	Rugged MC145406 Replacement	LT1039-16
5	5	5V	No	Yes	0.1µF	Synchronous Communications, ±10kV ESD	LT1130A
5	4	5V	Yes	Yes	0.1µF	Synchronous Modem/DCE Interface, ±10kV ESD	LT1131A
5	3	5V	No	Yes	0.1µF	Modem/DCE Interface, ±10kV ESD	LT1132A
3	5	5V	No	Yes	0.1µF	PC/DTE Interface, ±10kV ESD	LT1133A
4	4	5V	No	Yes	0.1µF	5V Only 1488/1489 Replacement, ±10kV ESD	LT1134A
5	3	5V, ±12V	No	Yes	N/A	Modem/DCE Interface, ±10kV ESD	LT1135A
4	5	5V	Yes	Yes	0.1µF	Synchronous PC/DTE Interface, ±10kV ESD	LT1136A
5	3	5V	Yes	Yes	0.1µF	Modem/DCE Interface, ±10kV ESD	LT1138A
4	4	5V, 12V	Yes	Yes	0.1µF	1488/1489 Replacement, ±10kV ESD	LT1139A
5	3	5V, ±12V	Yes	Yes	N/A	Modem/DCE Interface, ±10kV ESD	LT1140A
3	5	5V, ±12V	Yes	Yes	N/A	PC/DTE Interface, ±10kV ESD	LT1141A
5	3	5V	Yes	Yes	0.1µF	Ultra-Low Power, 1 Receiver Keep-Alive in SHDN, ±10kV ESD	LTC1338

Programmable EIA/TIA562/RS232 and RS485 I/O Ports

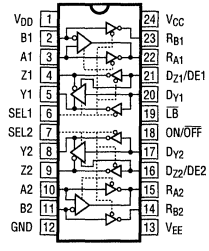
Low Supply Current: **1mA Typical**
15µA Supply Current in Shutdown
5V Powered (LTC1334)
120kBaud in EIA/TIA562 or RS232
10MBaud in RS485/RS422
Self-Testing Capability in Loopback Mode
LTC1321/LTC1322 Have the Same Pinout as SP301/SP302

- LTC1335 Features Receiver Three-State Outputs
- Power-Up/Down Glitch-Free Outputs
- Driver Maintains High Impedance in Three-State, Shutdown, or With Power Off
- Thermal Shutdown Protection
- Protection: I/O Lines Can Withstand ±25V
- Withstands Repeated ±10kV ESD Pulses
- SO Wide or Dual-In-Line Packages

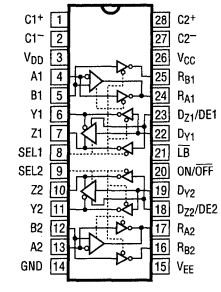
RS232 OR EIA/TIA562 TRANSCEIVERS	RS485 TRANSCEIVERS	OUTPUT LEVELS	DRIVER ENABLE	SELF TEST LOOPBACK	PART NUMBER
2	2	232/562	—	Yes	LTC1321
4	2	232/562	—	Yes	LTC1322
4	2	232	Yes	Yes	LTC1334
4	2	562	Yes	Yes	LTC1335



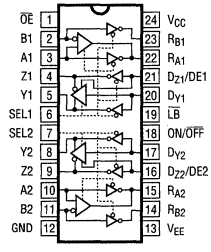
LTC1321
2 RS485 DRIVERS/RECEIVERS
EIA/TIA562 DRIVERS/RECEIVERS



LTC1322
2 RS485 DRIVERS/RECEIVERS
4 EIA/TIA562 DRIVERS/RECEIVERS



LTC1334
2 RS485 DRIVERS/RECEIVERS
4 RS232 DRIVERS/RECEIVERS
5V POWERED

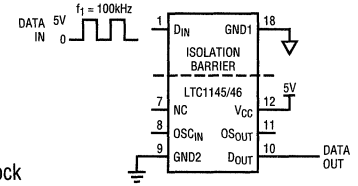


LTC1335
2 RS485 DRIVERS/RECEIVERS
4 EIA/TIA562 DRIVERS/RECEIVERS

Low Power Digital Isolators

- UL Recognized (LTC1145A,LTC1146A) File E151738 to UL1577
- Low Input Current
  LTC1145: 700µA, LTC1146: 70µA
- Maximum Input Frequency
  LTC1145: 200kHz, LTC1146: 20kHz
- TTL Level Output
- Noise Filter Prevents Glitches at the Output
- Output Can Be Synchronized to and External Clock

Digital Isolation Interface
Data Rate Up to 200kHz



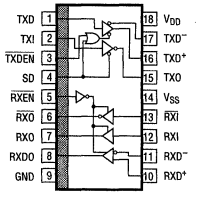
- Low Power Opto-Isolator Replacemen
- Isolated Serial Data Interfaces
- Isolated Power MOSFET Drivers

ISOLATION VOLTAGE	INPUT CURRENT	MAX INPUT FREQUENCY	GLITCH-FREE OUTPUT FILTER	EXT CLOCK SYNCH	UL RECOGNIZED	PART NUMBER
2500	700µA	200kHz	Yes	Yes	✓	LTC1145A
2500	70µA	20kHz	Yes	Yes	✓	LTC1146A
500	700µA	200kHz	Yes	Yes		LTC1145
500	70µA	20kHz	Yes	Yes		LTC1146

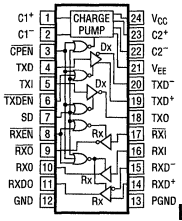
Complete AppleTalk/LocalTalk® Transceivers

- Single Chip Complete AppleTalk DCE/DTE Solutions
- Low Power
- Micropower Shutdown (LTC1320/LTC1323/LTC1323-16)
- Micropower Receiver Keep Alive (LTC1323)
- 5V Powered (LTC1323/LTC1323-16/LTC1318)
- Surface Mount Packages
- Thermal/Short Circuit Protection
- Small Charge Pump Capacitors
- Drivers High Impedance in Shutdown/Power Off States

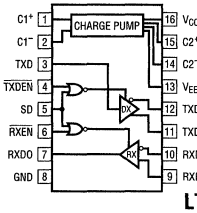
DCE/DTE	REQUIRED SUPPLIES	SUPPLY CURRENT	SHUTDOWN FUNCTION	1 RECEIVER KEEP ALIVE	SUPPLY IN SHUTDOWN	PART NUMBER
DTE	±5V	1.2mA	Yes	—	30µA	LTC1320
DTE	5V	2.4mA	Yes	Yes	65µA	LTC1323
DTE	5V	2.4mA	Yes	—	65µA	LTC1323-16
DCE	5V	18mA	No	—	—	LTC1318
DTE/DCE	5V	1mA	Yes	—	1µA	LTC1324
DCE	5V	8mA/–3mA	Yes	—	10µA	LT1389



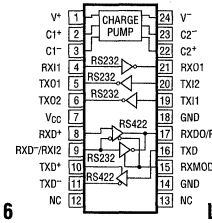
DTE LTC1320



DTE LTC1323



DTE LTC1323-16



DCE LTC1318

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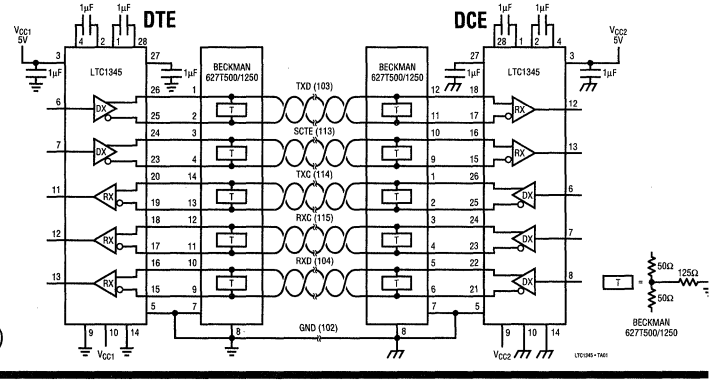
V.35 Interface

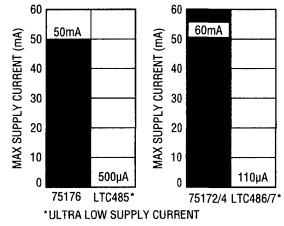
- Single Chip Provides All V.35 Differential Clock and Data Signals
- Operates From Single 5V Supply (LTC1345)
- Shutdown Mode Reduces I_{CC} to 1µA Typ
- Software Selectable DTE or DCE Configuration
- ±10kV ESD Protection
- 10MBaud Transmission Rate
- Transmitter Maintains High Impedance When Disabled, Shut Down or with Power Off
- Meets CCITT V.35 Specification
- Transmitters are Short-Circuit Protected
- Available in Surface Mount SW Packages
- 5V Powered (LTC1345) ±5V Powered (LTC1346)



RS485 Family Features

- Ultra-Low Power
- CMOS Schottky Process
- Designed for RS485 and RS422 Applications
- Three-State RS485 Outputs When Shut Down
- Power-Up/Down Glitch Free Outputs
- Power-Saving Shutdown Mode (LTC1481, LTC1483, LTC1487)
- Low EMI (LTC1483, LTC1487)
- 10MB Operation (LTC486-489, LTC1485)
- Industry Standard Pinouts
- SO Available

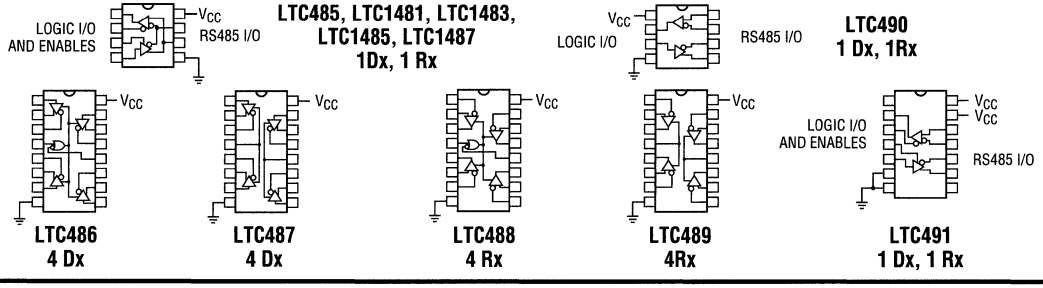
The LTC RS485 Advantage: Low Power



*ULTRA LOW SUPPLY CURRENT

RS485/RS422 Interface

DRIVERS	RECEIVERS	SUPPLIES REQUIRED	MAX DATA RATE	MAX SUPPLY CURRENT	SHUTDOWN SUPPLY CURRENT	DRIVERS DISABLE SUPPLY CURENT	INDUSTRY STANDARD PINOUT	COMMENTS	PART NUMBER
1	1	5V	2.5MB	500µA			75176	Half Duplex 2-Wire RS485	LTC485
4	0	5V	10MB	150µA			75172	Good For RS449, RS530, V.35 Interface	LTC486
4	0	5V	10MB	150µA			75174	Good For RS449, RS530, V.35 Interface	LTC487
0	4	5V	10MB	10mA			75173	Good For RS449, RS530, V.35 Interface	LTC488
0	4	5V	10MB	10mA			75175	Good For RS449, RS530, V.35 Interface	LTC489
1	1	5V	2.5MB	500µA			75179	Full Duplex 4-Wire RS485	LTC490
1	1	5V	2.5MB	500µA			75ALS180	Full Duplex 4-Wire RS485	LTC491
1	1	5V	2.5MB	500µA	10µA	120µA	75176	Ultra-Low Power Half Duplex 2-Wire RS485 w/SD	LTC1481
1	1	5V	150kB	500µA	10µA	120µA	75176	Low EMI Ultra-Low Power 2-Wire RS485 w/SD	LTC1483
1	1	5V	10MB	3.5mA			75ALS176B	High Speed/Half Duplex	LTC1485
1	1	5V	250kB	200µA	10µA	120µA	75176	High Input Impedance, Ultra-Low Power, Low EMI 2-Wire RS485 w/Shutdown	LTC1487



Interface Standards

SPECIFICATION		RS232	RS423	RS422	RS485	RS562
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential	Single-Ended
Number of Drivers and Receivers Allowed on One Line		1 Driver, 1 Receiver	1 Driver, 10 Receivers	1 Driver, 10 Receivers	32 Drivers, 32 Receivers	1 Driver, 1 Receiver
Maximum Cable Length		50 feet*	4000 feet	4000 feet	4000 feet	50 feet*
Maximum Data Rate		20kb/s	100kb/s	10Mb/s	10Mb/s	64kb/s
Maximum Voltage Applied to Driver Output		±25V	±6V	−0.25V to 6V	−7V to 12V	±25V
Driver Output Signal	Loaded	±5V	±3.6V	±2V	±1.5V	±3.7V
	Unloaded	±15V	±6V	±5V	±5V	±13.2V
Driver Load		3kΩ to 7kΩ	450Ω (Min)	100Ω	54Ω	3kΩ to 7kΩ
Maximum Driver Output Current (High-Impedance State)	Power ON	—	—	—	—	60mA
	Power OFF	V_{MAX}/300Ω	±100µA	±100µA	±100µA	V_{MAX}/300Ω
Output Slew Rate		30V/µs (Max)	Controls Provided	—	—	30V/µs (Max)
Receiver Input Voltage Range		±15V	±12V	±7V	−7V to 12V	±25V
Receiver Input Sensitivity		±3V	±200mV	±200mV	±200mV	±3V
Receiver Input Resistance		3kΩ to 7kΩ	4kΩ (Min)	4kΩ (Min)	12kΩ (Min)	3kΩ to 7kΩ

*or 2500pF cable capacitance, as per EIA 232E

SECTION 5—INTERFACE

5

3.3V/5.0V Low Power RS232 3-Driver/5-Receiver Transceiver

FEATURES

- **Low Supply Current: 500μA**
- **Supply Current in Shutdown: 0.2μA**
- **Supply Current in Receiver Alive Mode: 15μA**
- **ESD Protection over ±10kV**
- **Operates from a Single 3.3V or 5V Supply**
- Operates to 120kBaud with 0.1μF Flying Capacitors
- Three-State Outputs Are High Impedance When Off
- Output Overvoltage Does Not Force Current Back into Supplies
- RS232 I/O Lines Can Be Forced to ±25V Without Damage
- Flowthrough Architecture

APPLICATIONS

- Notebook Computers
- Palmtop Computers
- Printers
- Portable Instruments

DESCRIPTION

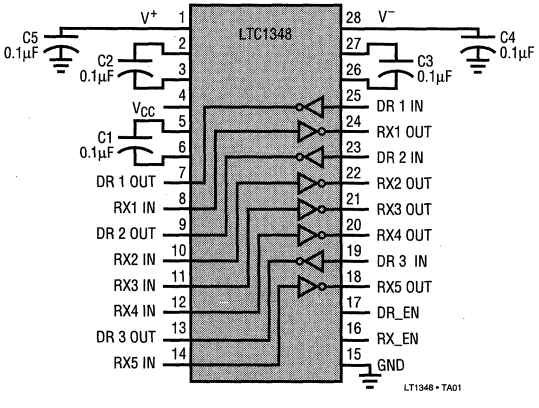
The LTC®1348 is a 3-driver/5-receiver RS232 transceiver with very low supply current. The charge pump only requires five 0.1μF capacitors. The LTC1348 provides full RS232 output levels when operated over a wide supply range of 3.0V to 5.5V

The transceiver operates in one of four modes: Normal, Receiver Disable, Receiver Alive and Shutdown. In Normal or Receiver Disable mode, I_{CC} is only 500μA in the no load condition. In Shutdown mode, the supply current is further reduced to 0.2μA. In Receiver Alive mode, all five receivers are kept alive and the supply current is 15μA. All RS232 outputs assume a high impedance state in Shutdown or Receiver Alive mode or with the power off. The receiver outputs assume a high impedance state in Receiver Disable or with the power off.

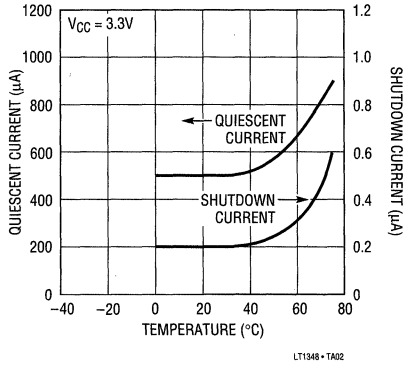
The LTC1348 is fully compliant with all data rate and overvoltage RS232 specifications. The transceiver operates up to 120kbaud with all drivers loaded with 1000pF, 3kΩ. Both driver outputs and receiver inputs can be forced to ±25V without damage and can survive multiple ±10kV ESD strikes.

TYPICAL APPLICATION

3-Drivers/5-Receivers with Shutdown



Supply Current

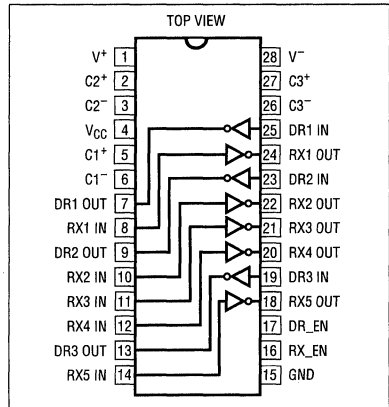


ABSOLUTE MAXIMUM RATINGS

Note 1)

Supply Voltage (V_{CC}) 6V
Input Voltage
  Driver ..... $-0.3V$ to $V_{CC} + 0.3V$
  Receiver ..... $-25V$ to $25V$
  Driver/Receiver Enable Pin ..... $-0.3V$ to $V_{CC} + 0.3V$
Output Voltage
  Driver ..... $-25V$ to $25V$
  Receiver ..... $-0.3V$ to $V_{CC} + 0.3V$
Short-Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1348CG
LTC1348CSW

Consult factory for Industrial and Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = C5 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Any Driver							
Output Voltage Swing	3k to GND	Positive	●	5.0	6.7		V
		Negative	●	−5.0	−6.5		V
Logic Input Voltage Level	Input Low Level (V_{OUT} = High)		●		1.4	0.8	V
	Input High Level (V_{OUT} = Low)		●	2.0	1.4		V
Logic Input Current	$V_{IN} = V_{CC}$		●			5	µA
	V_{IN} = 0V		●		−5	−20	µA
Output Short-Circuit Current	V_{OUT} = 0V				±12		mA
Output Leakage Current	Shutdown (Note 3) or Receiver Alive (Note 4), $V_{OUT} = \pm 20V$		●		±10	±500	µA
Any Receiver							
Input Voltage Thresholds	Input Threshold (Receiver Alive Mode)		●	0.8	1.5	2.4	V
	Input Low Threshold (Normal Mode)		●	0.8	1.3		V
	Input High Threshold (Normal Mode)		●		1.7	2.4	V
Hysteresis	Normal Mode		●	0.1	0.4	1	V
Input Resistance	$V_{IN} = \pm 10V$			3	5	7	kΩ
Output Voltage	Output Low, $I_{OUT} = -1.6mA$ (V_{CC} = 3.3V)		●		0.2	0.4	V
	Output High, $I_{OUT} = 160\mu A$ (V_{CC} = 3.3V)		●	3.0	3.2		V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$			−3	−20		mA
Output Leakage Current	Shutdown (Note 3), $0V \le V_{OUT} \le V_{CC}$		●		1	10	µA

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V, C1 = C2 = C3 = C4 = C5 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output Voltage	I_{OUT} = 0mA			8.0		V
	I_{OUT} = 8mA			7.5		V
V^- Output Voltage	I_{OUT} = 0mA			–8.0		V
	I_{OUT} = –8mA			–7.0		V
Supply Rise Time	Shutdown to Turn-On			0.2		ms
Power Supply						
V_{CC} Supply Current	No Load (Note 2) V_{CC} = 3.3V or 5V	●		0.5	1.5	mA
	Receiver Alive Mode (Note 4) V_{CC} = 3.3V or 5V	●		15.0	30.0	µA
Supply Leakage Current (V_{CC})	Shutdown (Note 3)	●		0.2	10	µA
Driver/Receiver Enable Threshold Low	V_{CC} = 3.3V	●		1.4	0.8	V
Driver/Receiver Enable Threshold High	V_{CC} = 3.3V	●	2.0	1.4		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V or 5V, C1 = C2 = C3 = C4 = C5 = 0.1µF, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Data Rate	R_L = 3k, C_L = 1000pF, One Driver Switching	●	120	250		kbps
Slew Rate	R_L = 3k, C_L = 51pF			8	30	V/µs
	R_L = 3k, C_L = 2500pF			4		V/µs
Driver Propagation Delay (TTL to RS232)	t_{HLD} (Figure 1)	●		2	3.5	µs
	t_{LHD} (Figure 1)	●		2	3.5	µs
Receiver Propagation Delay (RS232 to TTL)	t_{HLR} (Figure 2) (Normal Mode)	●		0.3	0.8	µs
	t_{LHR} (Figure 2) (Normal Mode)	●		0.2	0.8	µs
	t_{HLR} (Figure 2) (Receiver Alive Mode)	●		1.0	2.0	µs
	t_{LHR} (Figure 2) (Receiver Alive Mode)	●		0.3	2.0	µs

The ● denotes specifications which apply over the operating temperature range of 0°C ≤ T_A ≤ 70°C.

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

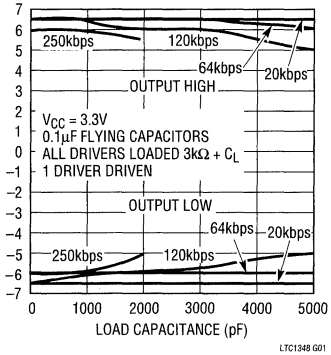
Note 2: Supply current is measured with driver and receiver outputs unloaded. The V_{DR_EN} and V_{RX_EN} = V_{CC}.

Note 3: Supply current measurement in Shutdown is performed with V_{DR_EN} and V_{RX_EN} = 0V.

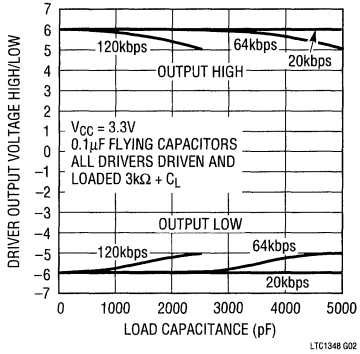
Note 4: Supply current measurement in Receiver Alive mode is performed with V_{DR_EN} = 0V and V_{RX_EN} = V_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

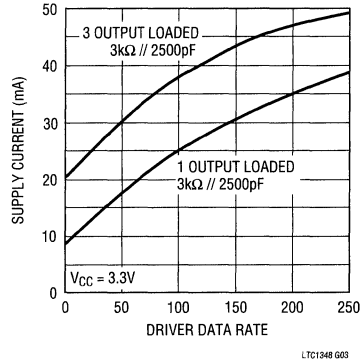
Driver Output Voltage High/Low vs. Load Capacitance (C_L)



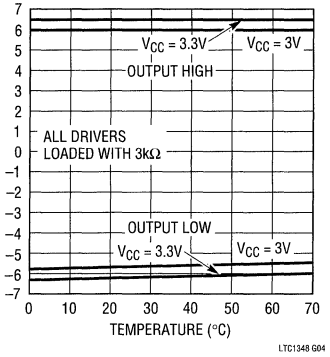
Driver Output Voltage High/Low vs. Load Capacitance (C_L)



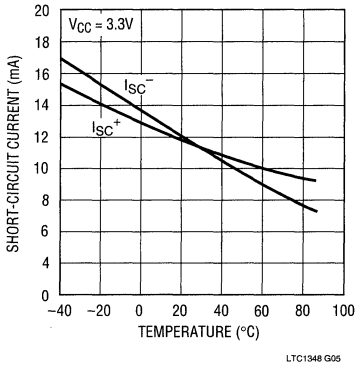
Supply Current vs. Driver Data Rate



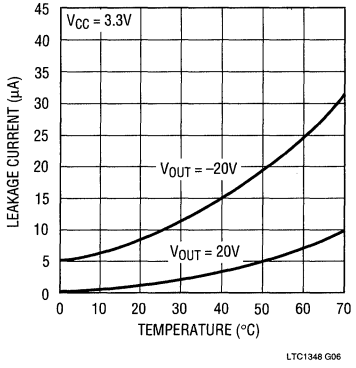
Driver Output Voltage High/Low vs. Temperature (°C)



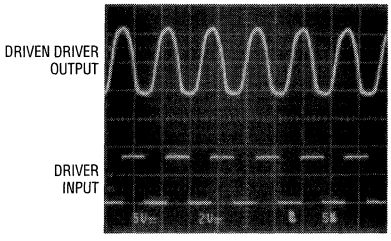
Driver Short-Curcuit Current vs. Temperature (°C)



Driver Leakage in SHUTDOWN vs. Temperature (°C)



With V_{CC} = 3.3V All Driver Outputs Loaded with 3kΩ, 1000pF. 1 Driven at 250kbps



5

PIN FUNCTIONS

V_{CC}: 3.3V or 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor.

GND: Ground Pin.

RX_EN: TTL/CMOS Compatible Enable Pin. Refer to Table 1 for its functional description.

DR_EN: TTL/CMOS Compatible Enable Pin. Refer to Table 1 for its functional description.

V^+: Positive Supply Output (RS232 Drivers). This pin requires an external capacitor C = 0.1µF for charge storage. The capacitor may be tied to ground or V_{CC}. With multiple devices, the V^+ and V^- pins may be paralleled into common capacitors. For large numbers of devices, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (RS232 Drivers). This pin requires an external capacitor C = 0.1µF for charge storage.

$C1^+$, $C1^-$, $C2^+$, $C2^-$, $C3^+$, $C3^-$: Commutating Capacitor Inputs. These pins require three external capacitors C = 0.1µF: one from $C1^+$ to $C1^-$, another from $C2^+$ to $C2^-$ and another from $C3^+$ to $C3^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 1Ω. Ceramic capacitors are recommended.

DR IN: RS232 Driver Input Pins. Inputs are TTL/CMOS compatible. The inputs of unused drivers can be left unconnected since 300k input pull-up resistors to V_{CC} are included on chip. To minimize power consumption, the internal driver pull-up resistors are disconnected from V_{CC} in the Shutdown or Receiver Alive mode.

DR OUT: Driver Outputs at RS232 Voltage Levels. Outputs are in a high impedance state when in the Shutdown Receiver Alive mode or V_{CC} = 0V. The driver outputs are protected against ESD to ±10kV for human body model discharges.

RX IN: Receiver Inputs. These pins can be forced to ±25V without damage. The receiver inputs are protected against ESD to ±10kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. In Receiver Alive mode all receivers have no hysteresis.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in the Shutdown or Receiver Disable mode to allow data line sharing.

Table 1. Functional Description

MODE	RX ENABLE	DR ENABLE	DRIVERS	RECEIVERS	I_{CC} TYP
Shutdown	0	0	All Drivers Shutdown. All Driver Outputs Assume High Impedance. All Driver Pull-Up Resistors Disconnect From V_{CC}.	All Receivers Shutdown. All Receiver Outputs Assume High Impedance.	0.2µA
Receiver Disable	0	1	All Drivers Alive.	All Receiver Outputs in Three-State.	500µA
Receiver Alive	1	0	All Drivers Shutdown. All Driver Outputs in Three-State. All Driver Pull-Up Resistors Disconnect From V_{CC}.	All Receivers Alive.	15µA
Normal	1	1	All Drivers Alive.	All Receivers Alive.	500µA

SWITCHING TIME WAVEFORMS

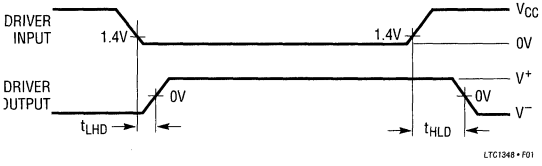


Figure 1. Driver Propagation Delay Timing

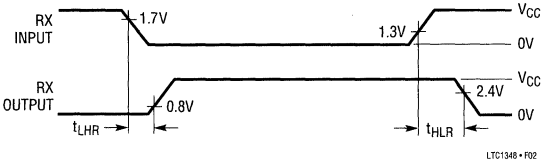


Figure 2. Receiver Propagation Delay Timing

TEST CIRCUITS

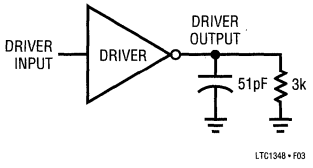


Figure 3. Driver Timing Test Load

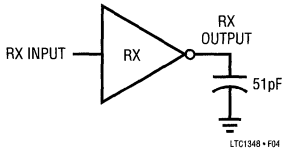
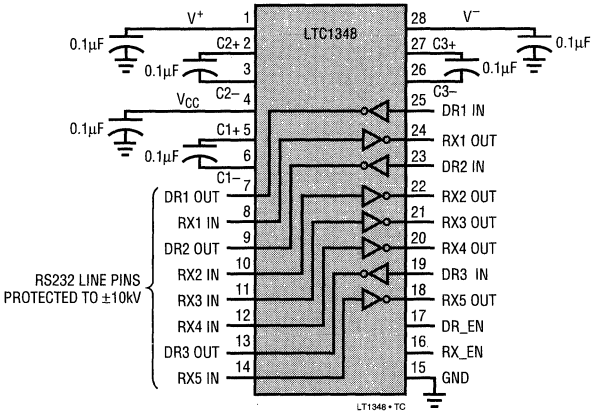


Figure 4. Receiver Timing Test Load

ESD Test Circuit



APPLICATIONS INFORMATION

Power Supply

The LTC1348 includes an on-board voltage-tripling charge pump capable of generating ±8V from a single 3.3V supply. This allows the LTC1348 drivers to provide guaranteed ±5V RS232-compliant voltage levels with a 3.3V supply. With all outputs loaded with 3kΩ, the LTC1348 can typically swing ±5V with voltages as low as 2.85V. It will meet the ±3.7V EIA562 levels with supply voltages as low as 2.2V. The charge pump requires three external flying capacitors to operate; 0.1µF ceramic capacitors are adequate for most applications. For applications requiring extremely high data rates or abnormally heavy output loads, 0.33µF flying capacitors are recommended. Bypass and output capacitor values should match those of the flying capacitors and all capacitors should be mounted as close to the package as possible.

APPLICATIONS INFORMATION

High Data Rates

The LTC1348 maintains true RS232 ±5V minimum driver output even at high data rates. Figure 5 shows a test circuit with 2m wires connecting the two test chips. Both chips are run from 3.3V supplies. Figure 6 shows the typical line waveforms with all three drivers, loaded with 1000pF and 3kΩ, toggling simultaneously at 120kbaud. Figure 7 shows the same circuit with a single 1000pF/3kΩ loaded driver driven at 250kbaud, and the other two drivers loaded but not toggling. This closely approximates the actual behavior of an RS232 serial port, with only one driver (TX) driven at high speed and the other two drivers (RTS and DTR) driven at a relatively low data rate or at DC. Under the same conditions, the LTC1348 can go as fast as 350kbaud and still meet EIA562 (±3.7V) minimum driver output levels.

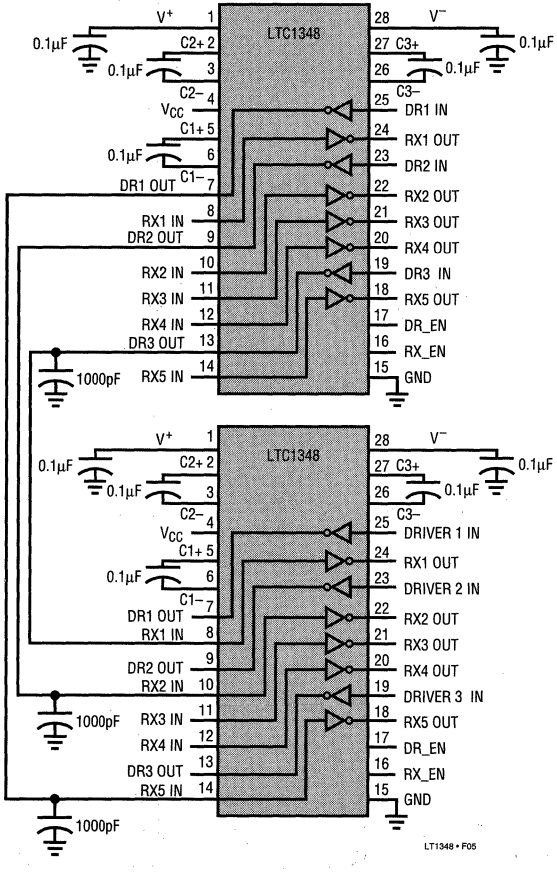


Figure 5. Data Rate Evaluation Circuit

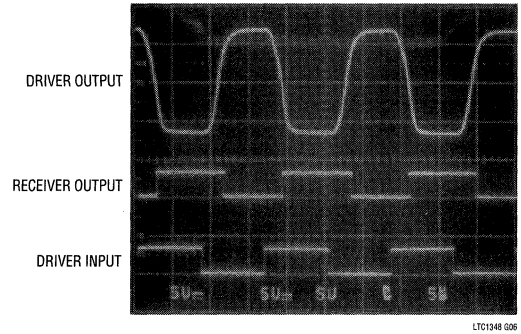


Figure 6. Driver Test Result at 120kbps

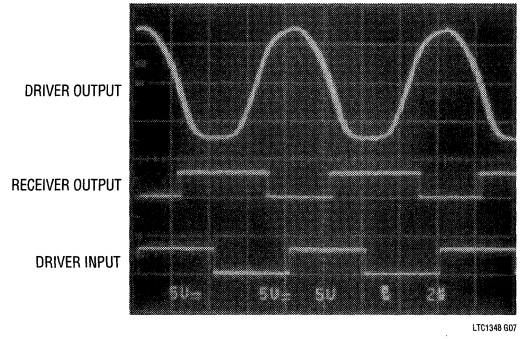


Figure 7. Driver Test Results at 250kbps

ELATED PARTS

RT NUMBER	DESCRIPTION	COMMENTS
1137A	3-DR/5-RX RS232 Transceiver	±15kV IEC-801-2 ESD Protection
C1327	3-DR/5-RX RS562 Transceiver	3.3V Operation
1330	3-DR/5-RX RS232	3V Logic Interface
1331	3-DR/5-RX RS232/RS562 Transceiver	5V RS232 or 3V RS562 Operation
C1347	3-DR/5-RX Micropower RS232 Transceiver	5 Receivers Active in Shutdown

LINEAR TECHNOLOGY

LT1537

Advanced Low Power 5V RS232 Transceiver with Small Capacitors

FEATURES

- **Low Cost**
- Uses Small Capacitors: 0.1µF, 0.2µF
- **1µA Supply Current in Shutdown**
- 120kBaud Operation for R_L = 3k, C_L = 2500pF
- **250kBaud Operation for R_L = 3k, C_L = 1000pF**
- CMOS Comparable Low Power: 40mW
- Operates from a Single 5V Supply
- Easy PC Layout: Flow-through Architecture
- Rugged Bipolar Design
- Outputs Assume a High Impedance State When Off or Powered Down
- Improved Protection: RS232 I/O Lines Can Be Forced to ±25V Without Damage
- Output Overvoltage Does Not Force Current Back into Supplies
- Absolutely No Latch-Up
- Available in SO Package

APPLICATIONS

- Notebook Computers
- Palmtop Computers

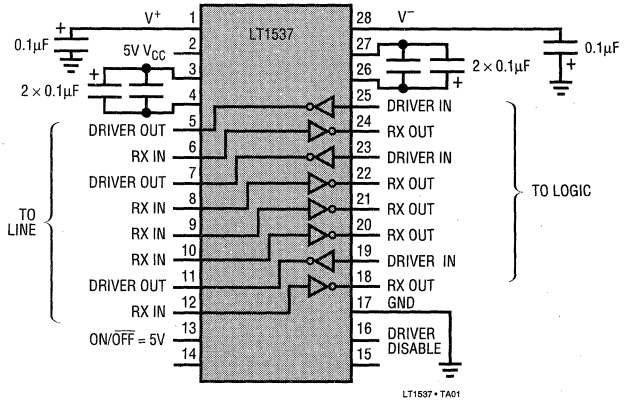
DESCRIPTION

The LT®1537 is a three-driver, five-receiver RS232 transceiver, pin compatible with the LT1137A, offering performance improvements and two shutdown modes. The LT1537's charge pump is designed for extended compliance and can deliver over 35mA of load current. Supply current is typically 8mA, competitive with similar CMOS devices. An advanced driver output stage operates up to 250kbaud while driving heavy capacitive loads.

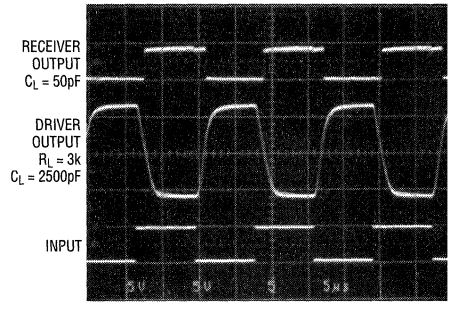
The LT1537 is fully compliant with all RS232 specifications. Special bipolar construction techniques protect the drivers and receivers beyond the fault conditions stipulated for RS232. Driver outputs and receiver inputs can be shorted to ±25V without damaging the device or the power supply generator. In addition, the RS232 I/O pins are resilient to multiple ±5kV ESD strikes.

The transceiver has two shutdown modes. One mode disables the drivers and the charge pump, the other shuts down all circuitry. While shut down, the drivers and receivers assume high impedance output states.

TYPICAL APPLICATION



Output Waveforms



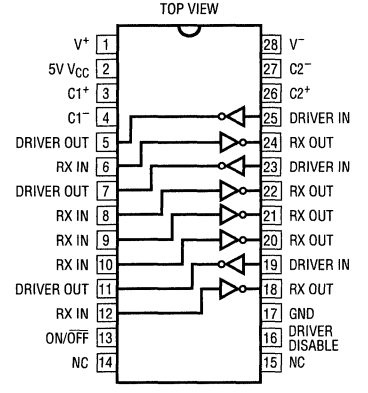
LINEAR TECHNOLOGY

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 5.5V
V^+ 13.2V
V^- (Note 7) ..... −6.5V
Input Voltage
  Driver ..... V^- to V^+
  Receiver ..... −25V to 25V
Output Voltage
  Driver ..... V^+ − 25V to V^- + 25V
  Receiver ..... −0.3V to V_{CC} + 0.3V
Short Circuit Duration
  V^+ ..... 30 sec
  V^- ..... 30 sec
  Driver Output ..... Indefinite
  Receiver Output ..... Indefinite
Operating Temperature Range
  LT1537C ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
28-LEAD PLASTIC SSOP

SW PACKAGE
28-LEAD PLASTIC SO WIDE

T_{JMAX} = 150°C, θ_{JA} = 96°C/W (G)
T_{JMAX} = 150°C, θ_{JA} = 85°C/W (SW)

ORDER PART NUMBER
LT1537CG
LT1537CSW

Consult factory for Industrial and Military grade parts.

5

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Generator						
V^+ Output				8.6		V
V^- Output				−7.0		V
Supply Current (V_{CC})	(Note 3)	●		8	17	mA
Supply Current When OFF (V_{CC})	Shutdown (Note 4) DRIVER DISABLE	● 		1.0 1.5	10 	µA mA
Shutdown to Turn-On	C^+, C^- = 0.1µF, C1, C2 = 0.2µF			0.2		ms
ON/$\overline{OFF}$ Pin Thresholds	Input LOW Level (Device Shutdown) Input HIGH Level (Device Enabled)	● ●	 2.4	1.4 1.4	0.8 	V V
ON/$\overline{OFF}$ Pin Current	0V ≤ $V_{ON/OFF}$ ≤ 5V	●	−15		80	µA
Driver Disable Pin Thresholds	Input LOW Level (Drivers Enabled) Input HIGH Level (Drivers Disabled)	● ●	 2.4	1.4 1.4	0.8 	V V
Driver Disable Pin Current	0V ≤ $V_{DRIVER\ DISABLE}$ ≤ 5V	●	−10		500	µA
Oscillator Frequency				130		kHz
Any Driver						
Output Voltage Swing	Load = 3k to GND Positive Negative	● ●	5.0 	7.5 −6.3	 −5.0	V V
Logic Input Voltage Level	Input LOW Level (V_{OUT} = HIGH) Input HIGH Level (V_{OUT} = LOW)	● ●	 2	1.4 1.4	0.8 	V
Logic Input Current	0.8V ≤ V_{IN} ≤ 2V	●		5	20	µA
Output Short-Circuit Current	V_{OUT} = 0V			±17		mA

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Any Driver						
Output Leakage Current	Shutdown V_{OUT} = ±15V (Note 4)	●		10	100	µA
Data Rate	R_L = 3k, C_L = 2500pF R_L = 3k, C_L = 1000pF		120 250			kBaud kBaud
Slew Rate	R_L = 3k, C_L = 51pF R_L = 3k, C_L = 2500pF		 4	15 15	30	V/µs V/µs
Propagation Delay	Output Transition t_{HL} HIGH to LOW (Note 5) Output Transition t_{LH} LOW to HIGH			0.6 0.5	1.3 1.3	µs µs
Any Receiver						
Input Voltage Thresholds	Input LOW Threshold (V_{OUT} = HIGH) Input HIGH Threshold (V_{OUT} = LOW)	● ●	0.8	1.3 1.7	 2.4	V V
Hysteresis		●	0.1	0.4	1.0	V
Input Resistance	V_{IN} = ±10V		3	5	7	kΩ
Output Voltage	Output LOW, I_{OUT} = −1.6mA Output HIGH, I_{OUT} = 160µA (V_{CC} = 5V)	● ●	 3.5	0.2 4.2	0.4	V V
Output Leakage Current	Shutdown (Note 4) 0 ≤ V_{OUT} ≤ V_{CC}	●		1	10	µA
Output Short-Circuit Current	Sinking Current, V_{OUT} = V_{CC} Sourcing Current, V_{OUT} = 0V		 10	−20 20	−10	mA mA
Propagation Delay	Output Transition t_{HL} HIGH to LOW (Note 6) Output Transition t_{LH} LOW to HIGH			250 350	600 600	ns ns

The ● denotes specifications which apply over the operating temperature range (0°C ≤ T_A ≤ 70°C for commercial grade and −40°C ≤ T_A ≤ 85°C for industrial grade).

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: Testing done at V_{CC} = 5V and $V_{ON/\overline{OFF}}$ = 3V. C1 = C2 = 0.2µF, $C^+ = C^-$ = 0.1µF.

Note 3: Supply current is measured with driver and receiver outputs unloaded and the driver inputs tied high.

Note 4: Supply current and leakage current measurements in shutdown are performed with $V_{ON/\overline{OFF}}$ = 0.1V. Supply current measurements using DRIVER DISABLE are performed with $V_{DRIVER\ DISABLE}$ = 3V.

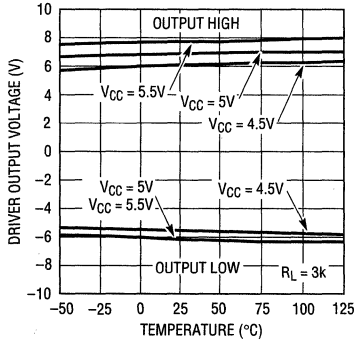
Note 5: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing (t_{HL} = 1.4V to 0V and t_{LH} = 1.4V to 0V).

Note 6: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V).

Note 7: Absolute maximum externally applied voltage. Internal charge pump may force a larger value on this pin.

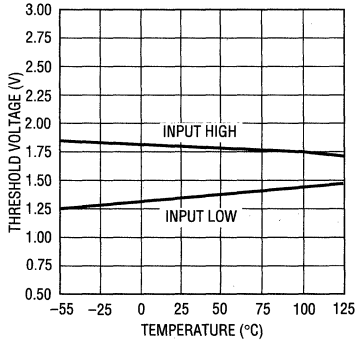
TYPICAL PERFORMANCE CHARACTERISTICS

Driver Output Voltage



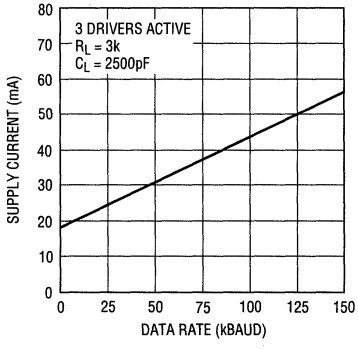
LT1537 • TPC01

Receiver Input Thresholds



ILT1537 • TPC02

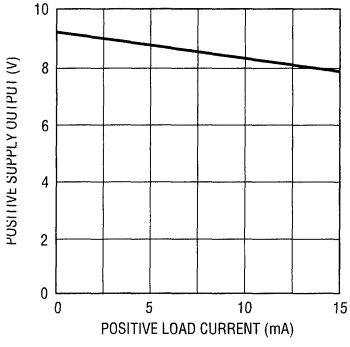
Supply Current vs Data Rate



LTX1537 • TPC03

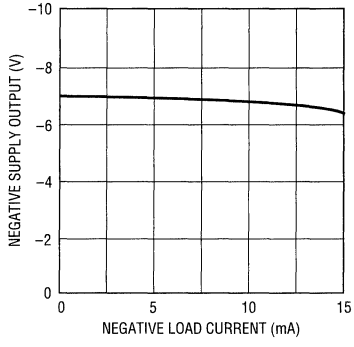
TYPICAL PERFORMANCE CHARACTERISTICS

Positive Supply Output Compliance Curve



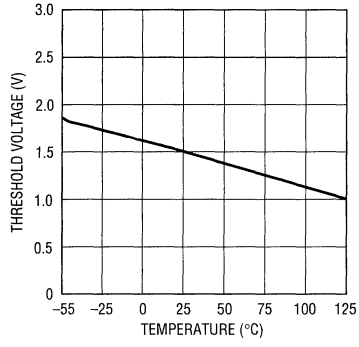
LT1537 • TPC04

Negative Supply Output Compliance Curve



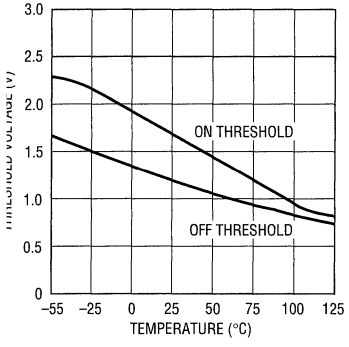
LT1537 • TPC05

Driver Disable Threshold



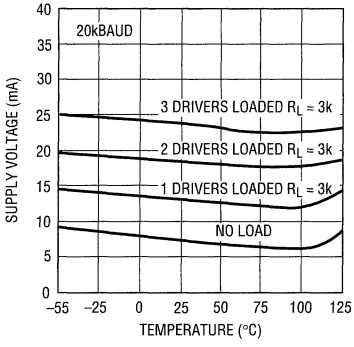
LT1537 • TPC06

On/Off Thresholds



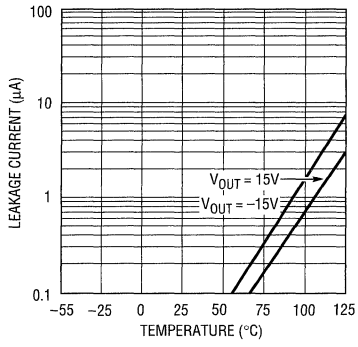
LT1537 • TPC07

Supply Current



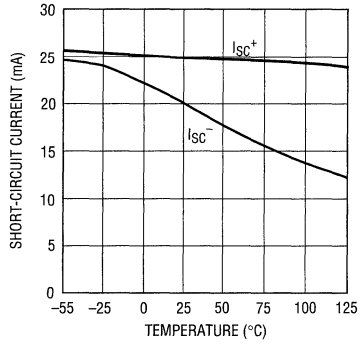
LT1537 • TPC08

Driver Leakage in Shutdown



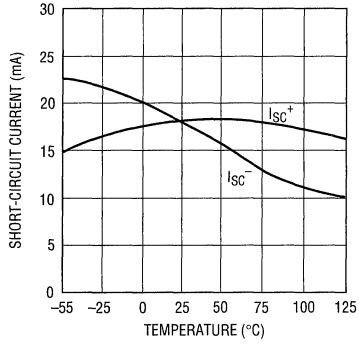
LT1537 • TPC09

Driver Output Short-Circuit Current



LT1537 • TPC10

Receiver Short-Circuit Current

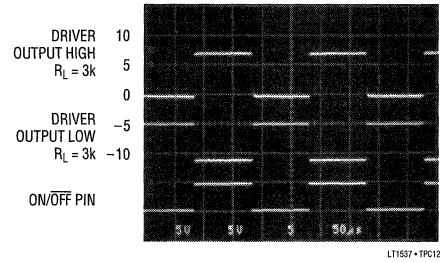


LT1537 • TPC11

5

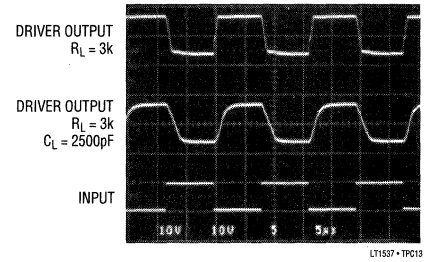
TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown to Driver Output



LT1537 • TPC12

Driver Output Waveforms



LT1537 • TPC13

PIN FUNCTIONS

V_{CC}: 5V Input Supply Pin. Supply current drops to zero in the shutdown mode. This pin should be decoupled with a 0.1µF ceramic capacitor close to the package pin. Insufficient supply bypassing can result in low output drive levels and erratic charge pump operation.

GND: Ground Pin.

ON/$\overline{OFF}$: TTL/CMOS Compatible Operating Mode Control. A logic LOW puts the device in the shutdown mode which reduces input supply current to zero and places all of the drivers and receivers in high impedance state. A logic HIGH fully enables the transceiver.

DRIVER DISABLE: This pin provides an alternate control for the charge pump and RS232 drivers. A logic HIGH on this pin shuts down the charge pump and places all drivers in a high impedance state. Receivers remain active under these conditions. Floating the driver disable pin or driving it to a logic LOW level fully enables the transceiver. A logic LOW on the On/$\overline{Off}$ pin supersedes the state of the Driver Disable pin. Supply current drops to 1.5mA when in DRIVER DISABLE mode.

V^+: Positive Supply Output (RS232 Drivers). $V^+ \approx 2V_{CC} - 1.5V$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$, tied to ground or V_{CC}. Larger value capacitors may be used to reduce supply ripple. With multiple transceivers, the V^+ and V^- pins may be paralleled into common capacitors. For large numbers of transceivers, increasing the size of the shared common storage capacitors is recommended to reduce ripple.

V^-: Negative Supply Output (RS232 Drivers). $V^- \approx -(2V_{CC} - 2.5V)$. This pin requires an external charge storage capacitor $C \geq 0.1\mu F$. V^- is short-circuit proof for 30 seconds.

$C1^+$, $C1^-$, $C2^+$, $C2^-$: Commutating Capacitor Inputs. These pins require two external capacitors $C \geq 0.2\mu F$: one from $C1^+$ to $C1^-$ and another from $C2^+$ to $C2^-$. To maintain charge pump efficiency, the capacitor's effective series resistance should be less than 2Ω. Low ESR ceramic capacitors work well in this application.

DRIVER IN: RS232 Driver Input Pins. These inputs are TTL/CMOS compatible. Inputs should not be allowed to float. Tie unused inputs to V_{CC}.

DRIVER OUT: Driver Outputs at RS232 Voltage Levels. Driver output swing meets RS232 levels for loads up to 3k. Slew rates are controlled for lightly loaded lines. Output current capability is sufficient for load conditions up to 2500pF. Outputs are in a high impedance state when in shutdown mode, V_{CC} = 0V or when the driver disable pin is active. Outputs are fully short-circuit protected from V^- + 25V to V^+ – 25V. Applying higher voltages will not damage the device if the overdrive is moderately current limited. Short circuits on one output can load the power supply generator and may disrupt the signal levels of the other outputs. The driver outputs are protected against ESD to ±5kV for human body model discharges.

PIN FUNCTIONS

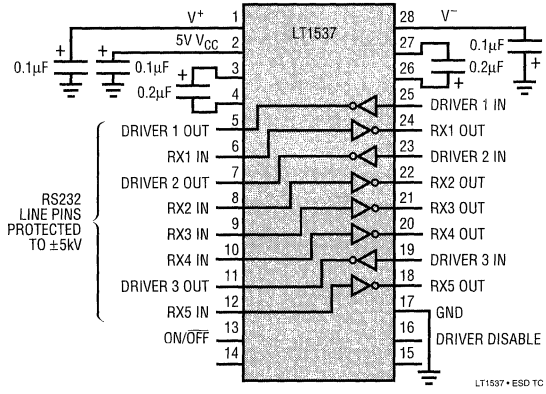
RX IN: Receiver Inputs. These pins accept RS232 level signals (±25V) into a protected 5k terminating resistor. The receiver inputs are protected against ESD to ±5kV for human body model discharges. Each receiver provides 0.4V of hysteresis for noise immunity. Open receiver inputs assume a logic low state.

RX OUT: Receiver Outputs with TTL/CMOS Voltage Levels. Outputs are in a high impedance state when in shutdown mode to allow data line sharing. Outputs are fully short-circuit protected to ground or V_{CC} with the power on, off, or in shutdown mode.

ESD PROTECTION

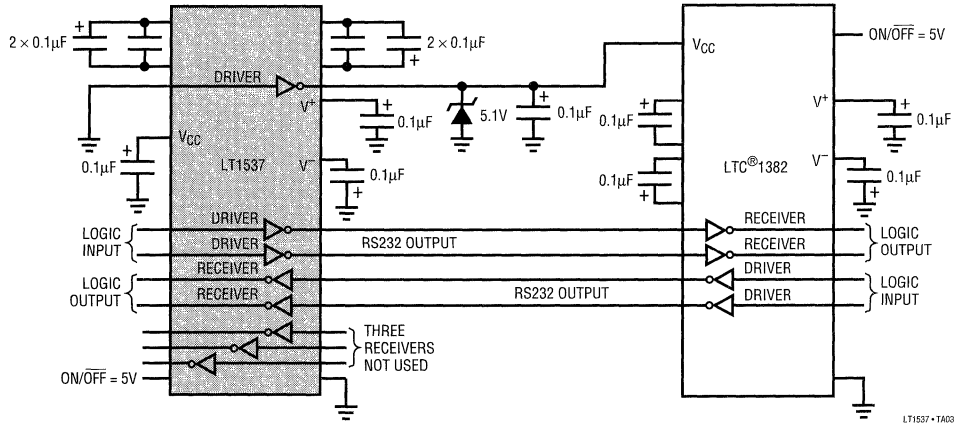
The RS232 line inputs of the LT1537 have on-chip protection from ESD transients up to ±5kV during shutdown or power ON state. The protection structures act to divert the static discharge safely to system ground. In order for the ESD protection to function effectively, the power supply and ground pins of the LT1537 must be connected to ground through low impedances. The power supply decoupling capacitors and charge pump storage capacitors provide this low impedance in normal application of the circuit. The only constraint is that low ESR capacitors must be used for bypassing and charge storage. ESD testing must be done with pins V_{CC}, V^+, V^- and GND shorted to ground or connected with low ESR capacitors.

ESD Test Circuit



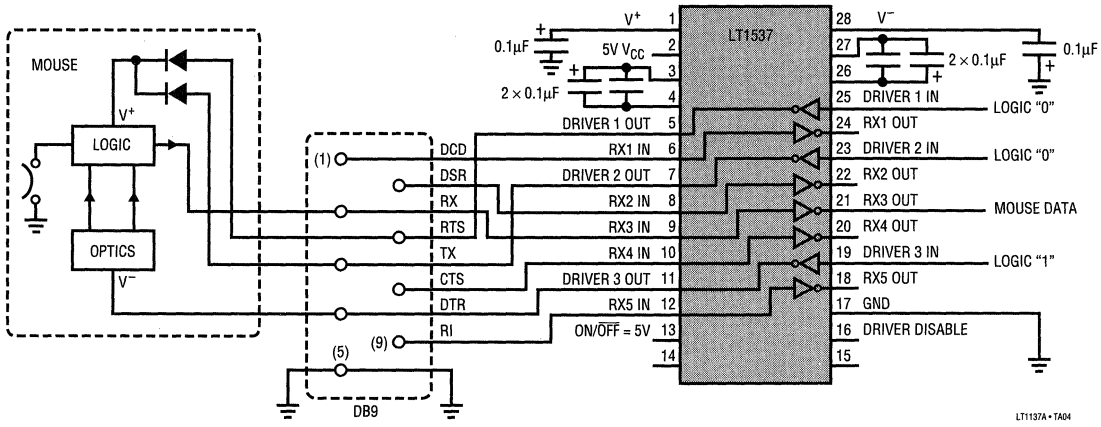
TYPICAL APPLICATIONS

LT1537 Driving Remote Powered LTC1382



TYPICAL APPLICATIONS

Typical Mouse Driving Application



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1137A	5V 3-Driver/5-Receiver RS232 Transceiver with Shutdown	Premium Performance Upgrade to LT1537
LT1138A	5V 5-Driver/3-Receiver RS232 Transceiver	Premium Performance DCE, Compliment to LT1537
LT1237	5V 3-Driver/5-Receiver RS232 Transceiver with One Receiver Active in Shutdown	Lower Power, Premium Performance Upgrade to LT1537
LT1330	5V 3-Driver/5-Receiver RS232 Transceiver with 3V Logic Interface and Shutdown	Premium Performance Device for 5V Systems with 3V Logic Supplies
LT1331	5V 3-Driver/5-Receiver RS232 Transceiver with 3V Logic Interface and Receiver Active in Shutdown	LT1330 with Low Power Receiver That Stays Active During Shutdown
LTC1337	Ultra-Low Power 5V 3-Driver/5-Receiver RS232 Transceiver with Shutdown	Ultra-Low Power, Premium Performance Upgrade to LT1537
LTC1338	5V 5-Driver/3-Receiver RS232 Transceiver with Shutdown	Ultra-Low Power, Peripheral-Side Compliment to LT1537

SECTION 5—INTERFACE

RS485

5

3.3V Ultra-Low Power RS485 Transceiver

FEATURES

- **True RS485 from a Single 3.3V Supply**
- **Low Power: I_{CC} = 500μA Max with Driver Disabled**
- **I_{CC} = 600μA Max with Driver Enabled, No Load**
- **1μA Quiescent in Shutdown Mode**
- **ESD Protection to ±10kV on Receiver Inputs and Driver Outputs**
- –7V to 12V Common-Mode Range Permits ±7V Ground Difference Between Devices on the Data Line
- Thermal Shutdown Protection
- Power Up/Down Glitch-Free Driver Outputs Permit Live Insertion or Removal of Transceiver
- Driver Maintains High Impedance in Three-State or with the Power Off
- Up to 32 Transceivers on the Bus
- 50ns Typical Driver Propagation Delays with 10ns Skew
- Pin Compatible with the LTC485

APPLICATIONS

- Battery-Powered RS485/RS422 Applications
- Low Power RS485/RS422 Transceiver
- Level Translator

DESCRIPTION

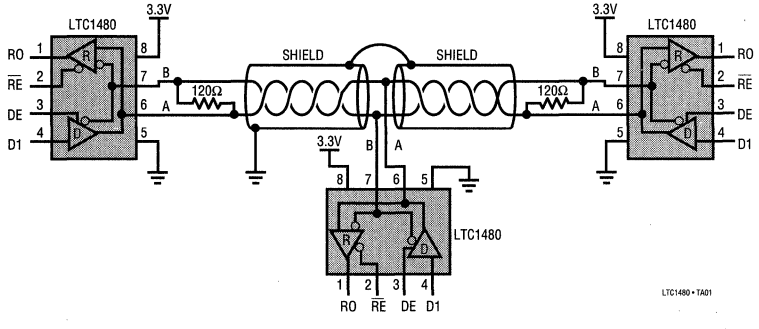
The LTC®1480 is an ultra-low power differential line transceiver which provides full RS485 compatibility while operating from a single 3.3V supply. It is designed for data transmission standard RS485 applications with extended common-mode range (12V to –7V). It also meets the requirements of RS422 and features high speed operation up to 2.5Mb/s. The CMOS design offers significant power savings without sacrificing ruggedness against overload or ESD damage. Typical quiescent current is only 300μA while operating and 1μA in shutdown.

The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common-mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state. The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open. I/O pins are protected against multiple ESD strikes of up to ±10kV.

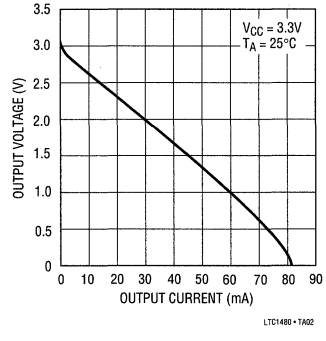
The LTC1480 is fully specified over the commercial and extended industrial temperature range. The LTC1480 is available in 8-pin SO and DIP packages.

TYPICAL APPLICATION

3.3V RS485 Network



Driver Differential Output Voltage vs Output Current

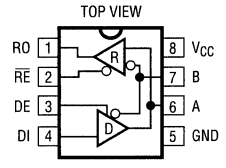


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 7V
Control Input Voltage ..... $-0.3V$ to $V_{CC} + 0.3V$
Driver Input Voltage ..... $-0.3V$ to $V_{CC} + 0.3V$
Driver Output Voltage ..... $\pm 14V$
Receiver Input Voltage ..... $\pm 14V$
Receiver Output Voltage ..... $-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range
LTC1480C ..... $0°C \le T_A \le 70°C$
LTC1480I ..... $-40°C \le T_A \le 85°C$
Storage Temperature Range ..... $-65°C$ to $150°C$
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX} = 125°C$, $\theta_{JA} = 130°C/W$ (N8)
$T_{JMAX} = 125°C$, $\theta_{JA} = 150°C/W$ (S8)

ORDER PART NUMBER
LTC1480CN8 LTC1480IN8 LTC1480CS8 LTC1480IS8
S8 PART MARKING
1480 1480I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3V$ (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0V$	●			3.3	V
V_{OD2}	Differential Driver Output Voltage (with Load)	R = 27Ω (RS485), Figure 1 R = 50Ω (RS422)	● ●	1.5 2.0		3.3	V V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{OC}	Driver Common-Mode Output Voltage	R = 27Ω or R = 50Ω, Figure 1	●			2	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{IH}	Input HIGH Voltage	DE, DI, $\overline{RE}$	●	2			V
V_{IL}	Input LOW Voltage	DE, DI, $\overline{RE}$	●			0.8	V
I_{IN1}	Input Current	DE, DI, $\overline{RE}$	●			±2	µA
I_{IN2}	Input Current (A, B)	DE = 0, V_{CC} = 0V or 3.6V, V_{IN} = 12V DE = 0, V_{CC} = 0V or 3.6V, V_{IN} = −7V	● ●			1.0 −0.8	mA mA
V_{TH}	Differential Input Threshold Voltage for Receiver	$-7V \le V_{CM} \le 12V$	●	−0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	$V_{CM} = 0V$			70		mV
V_{OH}	Receiver Output HIGH Voltage	$I_O = -4mA$, $V_{ID} = 200mV$	●	2			V
V_{OL}	Receiver Output LOW Voltage	$I_O = 4mA$, $V_{ID} = -200mV$	●			0.4	V
I_{OZR}	Three-State (High Impedance) Output Current at Receiver	V_{CC} = Max, $0.4V \le V_O \le 2.4V$	●			±1	µA
R_{IN}	Receiver Input Resistance	$-7V \le V_{CM} \le 12V$	●	12			kΩ
I_{CC}	Supply Current	No Load, Output Enabled No Load, Output Disabled	● ●		400 300	600 500	µA µA
I_{SHDN}	Supply Current in Shutdown Mode	DE = 0, $\overline{RE} = V_{CC}$			1	10	µA
I_{OSD1}	Driver Short-Circuit Current, V_{OUT} = HIGH	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSD2}	Driver Short-Circuit Current, V_{OUT} = LOW	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSR}	Receiver Short-Circuit Current	$0V \le V_O \le V_{CC}$	●	7		85	mA

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SWITCHING CHARACTERISTICS V_{CC} = 3.3V (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3 and 5)	●	25	50	80	ns
t_{PHL}	Driver Input to Output		●	25	50	80	
t_{SKEW}	Driver Output to Output		●		10	20	
t_R, t_F	Driver Rise or Fall Time		●	5	15	40	
t_{ZH}	Driver Enable to Output HIGH	C_L = 100pF (Figures 4, 6), S2 Closed	●		70	120	ns
t_{ZL}	Driver Enable to Output LOW	C_L = 100pF (Figures 4, 6), S1 Closed	●		70	120	ns
t_{LZ}	Driver Disable Time from LOW	C_L = 15pF (Figures 4, 6), S1 Closed	●		70	120	ns
t_{HZ}	Driver Disable Time from HIGH	C_L = 15pF (Figures 4, 6), S2 Closed	●		70	120	ns
t_{PLH}	Receiver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figure 3, 7)	●	30	140	200	ns
t_{PHL}	Receiver Input to Output		●	30	140	200	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew				13		ns
t_{ZL}	Receiver Enable to Output LOW	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		50	80	ns
t_{ZH}	Receiver Enable to Output HIGH	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		50	80	ns
t_{LZ}	Receiver Disable from LOW	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		50	80	ns
t_{HZ}	Receiver Disable from HIGH	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		50	80	ns
f_{MAX}	Maximum Data Rate		●	2.5			Mbits/s
t_{SHDN}	Time to Shutdown	DE = 0, $\overline{RE}$ = ⊓	●	50	200	600	ns
$t_{ZH(SHDN)}$	Driver Enable from Shutdown to Output HIGH	C_L = 100pF (Figures 4, 6), S2 Closed	●		70	120	ns
$t_{ZL(SHDN)}$	Driver Enable from Shutdown to Output LOW	C_L = 100pF (Figures 4, 6), S1 Closed	●		70	120	ns
$t_{ZH(SHDN)}$	Receiver Enable from Shutdown to Output HIGH	C_L = 15pF (Figures 2, 8), S2 Closed	●			4500	ns
$t_{ZL(SHDN)}$	Receiver Enable from Shutdown to Output LOW	C_L = 15pF (Figures 2, 8), S1 Closed	●			4500	ns

The ● denotes specifications which apply over the full operating temperature range.

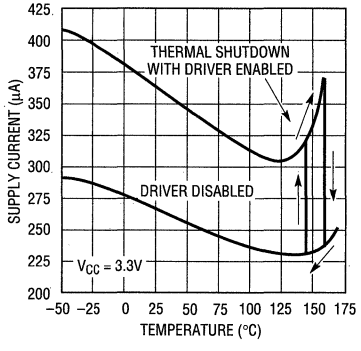
Note 1: Absolute maximum ratings are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out ot device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 3.3V and T_A = 25°C.

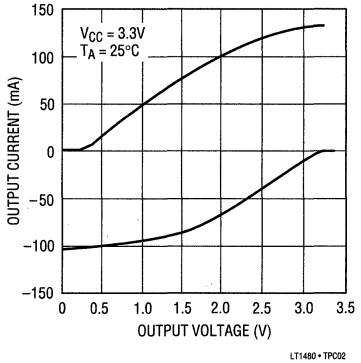
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature



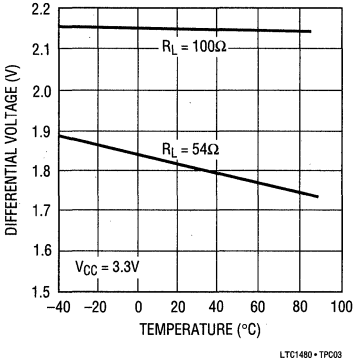
LT1480 • TPC01

Driver Output Low/High Voltage vs Output Current



LT1480 • TPC02

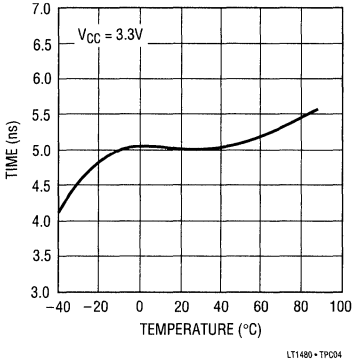
Driver Differential Output Voltage vs Temperature



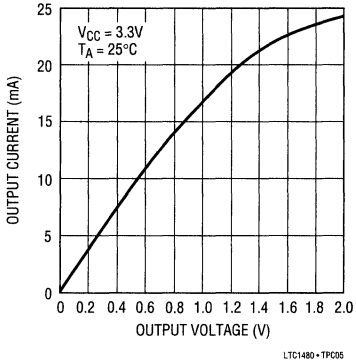
LTC1480 • TPC03

TYPICAL PERFORMANCE CHARACTERISTICS

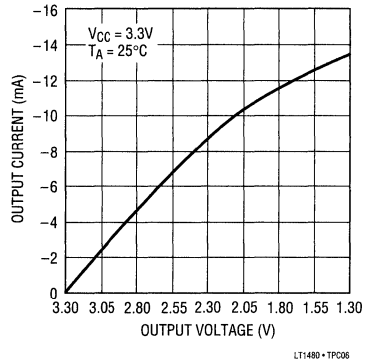
Driver Skew vs Temperature



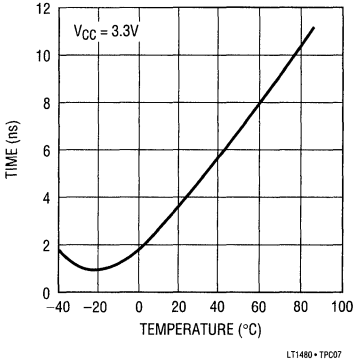
Receiver Output Low Voltage vs Output Current



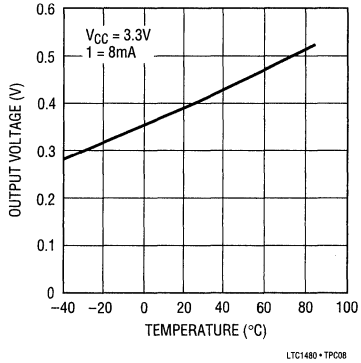
Receiver Output High Voltage vs Output Current



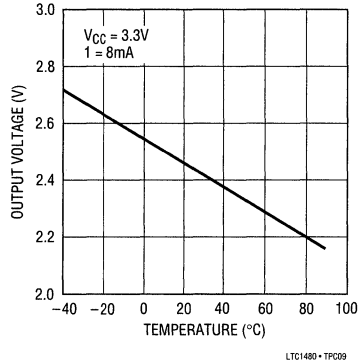
Receiver $|t_{PLH} - t_{PHL}|$ vs Temperature



Receiver Output Low Voltage vs Temperature



Receiver Output High Voltage vs Temperature



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PIN FUNCTIONS

RO (Pin 1): Receiver Output. If the receiver output is enabled ($\overline{RE}$ LOW) and A > B by 200mV, then RO will be HIGH. If A < B by 200mV, then RO will be LOW.

$\overline{RE}$ (Pin 2): Receiver Output Enable. A LOW enables the receiver output, RO. A HIGH input forces the receiver output into a high impedance state.

DE (Pin 3): Driver Outputs Enable. A HIGH on DE enables the driver output. A, B and the chip will function as a line driver. A low input will force the driver outputs into a high impedance state and the chip will function as a line receiver. If $\overline{RE}$ is high and DE is LOW, the part will enter a low power (1µA) shutdown state. If $\overline{RE}$ is low and DE is high, the driver outputs will be fed back to the receiver and the receive output will correspond to the driver input.

DI (Pin 4): Driver Input. If the driver outputs are enabled (DE HIGH) then a low on DI forces the outputs A LOW and B HIGH. A HIGH on DI with the driver outputs enabled will force A HIGH and B LOW.

GND (Pin 5): Ground.

A (Pin 6): Driver Output/Receiver Input.

B (Pin 7): Driver Output/Receiver Input.

V_{CC} (Pin 8): Positive Supply. 3.0V < V_{CC} < 3.6V.

FUNCTION TABLES

LTC1480 Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Z	Z
1	0	X	Z*	Z*

*Shutdown mode

LTC1480 Receiving

INPUTS			OUTPUTS
$\overline{RE}$	DE	A – B	RO
0	0	≥0.2V	1
0	0	≤–0.2V	0
0	0	Inputs Open	1
1	0	X	Z*

*Shutdown mode

TEST CIRCUITS

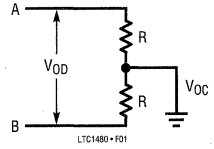

Figure 1. Driver DC Test Load

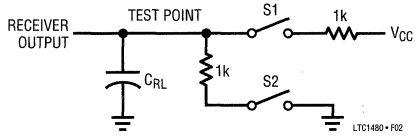

Figure 2. Receiver Timing Test Load

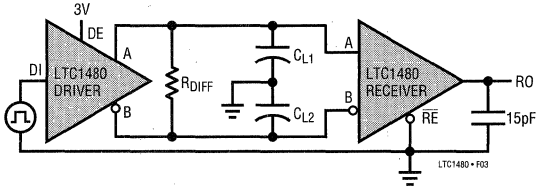

Figure 3. Driver/Receiver Timing Test Circuit

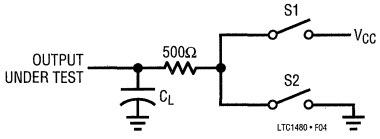

Figure 4. Driver Timing Test Load

SWITCHING TIME WAVEFORMS

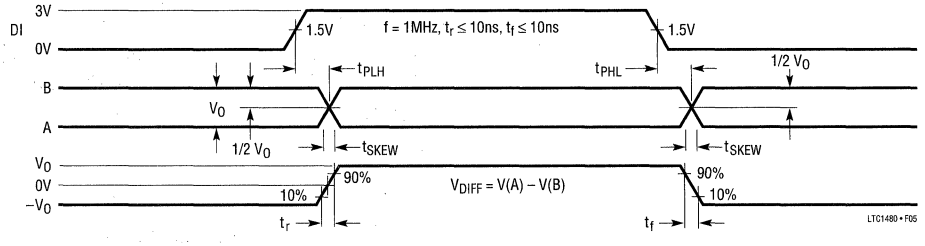

Figure 5. Driver Propagation Delays

SWITCHING TIME WAVEFORMS

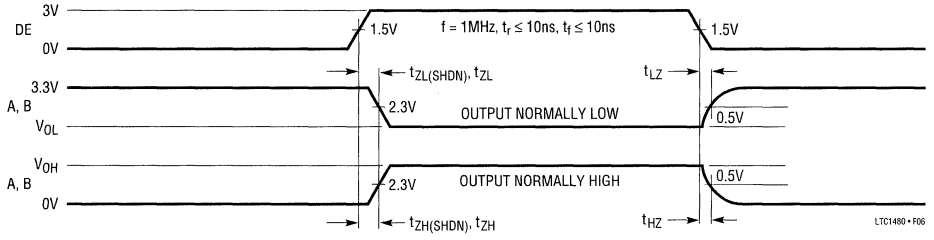

Figure 6. Driver Enable and Disable Times

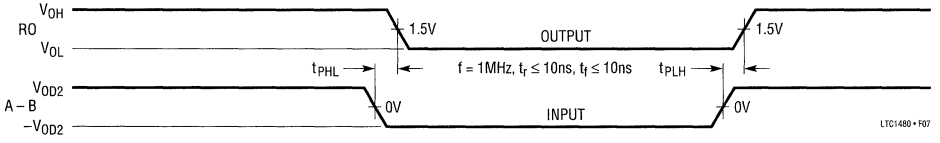

Figure 7. Receiver Propagation Delays

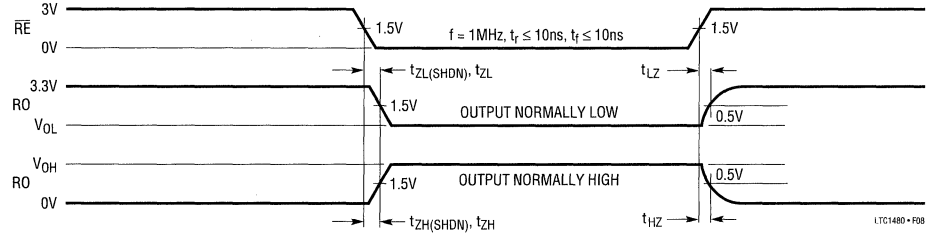

Figure 8. Receiver Enable and Disable Times

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APPLICATIONS INFORMATION

CMOS Output Driver

The LTC1480 transceiver provides full RS485 compatibility while operating from a single 3.3V supply. The RS485 specification requires that a transceiver withstand common-mode voltages of up to 12V or –7V at the RS485 line connections. Additionally, the transceiver must be immune to both ESD and latch-up, This rules out traditional CMOS drivers, which include parasitic diodes from their driver outputs to each supply rail (Figure 9). The LTC1480 uses a proprietary process enhancement which adds a pair of Schottky diodes to the output stage (Figure 10), preventing current from flowing when the common-mode

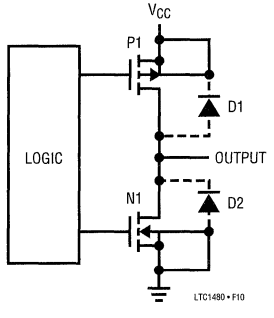


Figure 9. Conventional CMOS Output Stage

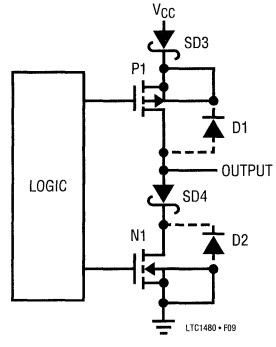


Figure 10. LTC1480 Output Stage

APPLICATIONS INFORMATION

voltage exceeds the supply rails. Latch-up at the output drivers is virtually eliminated and the driver is prevented from loading the line under RS485 specified fault conditions. A proprietary output protection structure protects the transceiver line terminals against ESD strikes of up to ±10kV.

When two or more drivers are connected to the same transmission line, a potential condition exists whereby more than two drivers are simultaneously active. If one or more drivers is sourcing current while another driver is sinking current, excessive power dissipation may occur within either the sourcing or sinking element. This condition is defined as driver contention, since multiple drivers are competing for one transmission line. The LTC1480 provides a current limiting scheme to prevent driver contention failure. When driver contention occurs, the current drawn is limited to about 70mA preventing excessive power dissipation within the drivers.

The LTC1480 has a thermal shutdown feature which protects the part from excessive power dissipation. Under extreme fault conditions, up to 250mA can flow through the part causing rapid internal temperature rise. The thermal shutdown circuit will disable the driver outputs when the internal temperature reaches 150°C and turns them back on when the temperature cools to 130°C. This cycle will repeat as necessary until the fault condition is removed.

Receiver Inputs

The LTC1480 features an input common-mode range covering the entire RS485 specified range of –7V to 12V. Differential signals of greater than ±200mV within the specified input common-mode range will be converted to a TTL compatible signal at the receiver output. A small amount of input hysteresis is included to minimize the effects of noise on the line signals. If the receiver inputs are floating (unterminated) an internal pull-up of 10µA at the A input will force the receiver output to a known high state.

Low Power Operation

The LTC1480 draws very little supply current whenever the driver outputs are disabled. In shutdown mode the quiescent current is typically less than 1µA. With the receiver active and the driver outputs disabled, the LTC1480 will typically draw 300µA quiescent current. With the driver outputs enabled but unterminated, quiescent current will rise as one of the two outputs sources current into the internal receiver input resistance. With the minimum receiver input resistance of 12k and the maximum output swing of 3.3V, the quiescent current will rise by a maximum of 275µA. Typical quiescent current rise with the driver enabled is about 100µA.

The quiescent current rises significantly if the driver is enabled when it is externally terminated. With 1/2 termination load (120Ω between the driver outputs) the quiescent current will jump to at least 13mA as the drivers force a minimum of 1.5V across the termination resistance. With a fully terminated 60Ω line attached, the current will rise to greater than 25mA with the driver enabled, completely overshadowing the extra 100µA drawn by internal receiver inputs.

Shutdown Mode

Both the receiver output ($\overline{RO}$) and the driver outputs (A, B) can be placed in three-state mode by bringing $\overline{RE}$ HIGH and DE LOW respectively. In addition, the LTC1480 will enter shutdown mode when $\overline{RE}$ is HIGH and DE is LOW.

In shutdown the LTC1480 typically draws only 1µA of supply current. In order to guarantee that the part goes into shutdown, $\overline{RE}$ must be high and DE must be LOW for at least 600ns simultaneously. If this time duration is less than 50ns the part will not enter shutdown mode.

Propagation Delay

Many digital encoding schemes are dependent upon the difference in the propagation delay times of the driver and receiver. Figure 11 shows the test circuit for the LTC1480 propagation delay.

The receiver delay times are:

$|t_{PLH} - t_{PHL}|$ = 13ns Typ, V_{CC} = 3.3V

The driver's skew times are:

t_{SKEW} = 10ns Typ, V_{CC} = 3.3V

20ns Max, V_{CC} = 3.3V, T_A = –40°C to 85°C

APPLICATIONS INFORMATION

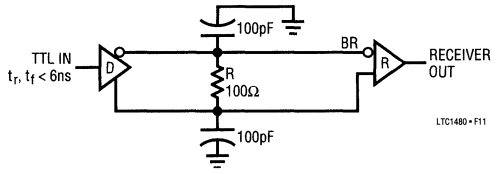


Figure 11. Receiver Propagation Delay Test Circuit

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC485	5V Low Power RS485 Interface Transceiver	Low power
LTC1481	5V Ultra-Low Power RS485 Transceiver with Shutdown	Lowest power
LTC1483	5V Ultra-Low Power RS485 Low EMI Transceiver with Shutdown	Low EMI/lowest power
LTC1485	5V Differential Bus Transceiver	Highest speed
LTC1487	5V Ultra-Low Power RS485 with Low EMI Shutdown and High Input Impendance	High input impendance/low EMI/lowest power

5

Ultra-Low Power RS485 Transceiver with Shutdown

FEATURES

- **Low Power: I_{CC} = 120μA Max with Driver Disabled**
- I_{CC} = 500μA Max with Driver Enabled, No Load
- **Drivers/Receivers Have ±10kV ESD Protection**
- **1μA Quiescent Current in Shutdown Mode**
- **High Speed: Up to 2.5Mbits/s Data Rate**
- Single 5V Supply
- –7V to 12V Common-Mode Range Permits ±7V Ground Difference Between Devices on the Data Line
- Thermal Shutdown Protection
- Power Up/Down Glitch-Free Driver Outputs Permit Live Insertion or Removal of Transceiver
- Driver Maintains High Impedance in Three-State or with the Power Off
- Up to 32 Transceivers on the Bus
- 30ns Typical Driver Propagation Delays with 5ns Skew
- Pin Compatible with the LTC485

APPLICATIONS

- Battery-Powered RS485/RS422 Applications
- Low Power RS485/RS422 Transceiver
- Level Translator

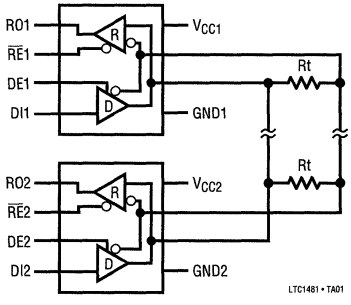
DESCRIPTION

The LTC®1481 is an ultra-low power differential line transceiver designed for data transmission standard RS485 applications. It will also meet the requirements of RS422. The CMOS design offers significant power savings over its bipolar counterparts without sacrificing ruggedness against overload or ESD damage. Typical quiescent current is only 80μA while operating and less than 1μA in shutdown.

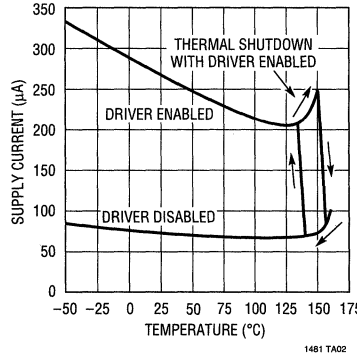
The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common-mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state. The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open.

The LTC1481 is fully specified over the commercial and extended industrial temperature range and is available in 8-pin DIP and SO packages.

TYPICAL APPLICATION



Supply Current vs Temperature

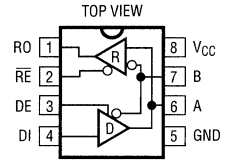


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 12V
Control Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Output Voltage ..... $\pm 14V$
Receiver Input Voltage ..... $\pm 14V$
Receiver Output Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Operating Temperature Range
LTC1481C ..... $0°C \le T_A \le 70°C$
LTC1481I ..... $-40°C \le T_A \le 85°C$
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX} = 125°C$, $\theta_{JA} = 130°C/W$ (N8)
$T_{JMAX} = 125°C$, $\theta_{JA} = 150°C/W$ (S8)

ORDER PART NUMBER
LTC1481CN8 LTC1481IN8 LTC1481CS8 LTC1481IS8
S8 PART MARKING
1481 1481I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$	●			5	V
V_{OD2}	Differential Driver Output Voltage (with Load)	R = 50Ω (RS422) R = 27Ω (RS485), Figure 1	● ●	2.0 1.5		 5	V V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{OC}	Driver Common-Mode Output Voltage	R = 27Ω or R = 50Ω, Figure 1	●			3	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{IH}	Input High Voltage	DE, DI, $\overline{RE}$	●	2			V
V_{IL}	Input Low Voltage	DE, DI, $\overline{RE}$	●			0.8	V
I_{IN1}	Input Current	DE, DI, $\overline{RE}$	●			±2	µA
I_{IN2}	Input Current (A, B)	DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = 12V DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = −7V	● ●			1.0 −0.8	mA mA
V_{TH}	Differential Input Threshold Voltage for Receiver	$-7V \le V_{CM} \le 12V$	●	−0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V	●		45		mV
V_{OH}	Receiver Output High Voltage	$I_O = -4mA$, $V_{ID} = 200mV$	●	3.5			V
V_{OL}	Receiver Output Low Voltage	$I_O = 4mA$, $V_{ID} = -200mV$	●			0.4	V
I_{OZR}	Three-State (High Impedance) Output Current at Receiver	V_{CC} = Max, $0.4V \le V_O \le 2.4V$	●			±1	µA
R_{IN}	Receiver Input Resistance	$-7V \le V_{CM} \le 12V$	●	12			kΩ
I_{CC}	Supply Current	No Load, Output Enabled No Load, Output Disabled	● ●		300 80	500 120	µA µA
I_{SHDN}	Supply Current in Shutdown Mode	DE = 0, $\overline{RE} = V_{CC}$			1	10	µA
I_{OSD1}	Driver Short-Circuit Current, V_{OUT} = HIGH	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSD2}	Driver Short-Circuit Current, V_{OUT} = LOW	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSR}	Receiver Short-Circuit Current	$0V \le V_O \le V_{CC}$	●	7		85	mA

5

SWITCHING CHARACTERISTICS

V_{CC} = 5V (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3, 5)	●	10	30	60	ns
t_{PHL}	Driver Input to Output		●	10	30	60	ns
t_{SKEW}	Driver Output to Output		●		5	10	ns
t_r, t_f	Driver Rise or Fall Time		●	3	15	40	ns
t_{ZH}	Driver Enable to Output High	C_L = 100pF (Figures 4, 6), S2 Closed	●		40	70	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100pF (Figures 4, 6), S1 Closed	●		40	70	ns
t_{LZ}	Driver Disable Time from Low	C_L = 15pF (Figures 4, 6), S1 Closed	●		40	70	ns
t_{HZ}	Driver Disable Time from High	C_L = 15pF (Figures 4, 6), S2 Closed	●		40	70	ns
t_{PLH}	Receiver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3, 7)	●	30	140	200	ns
t_{PHL}	Receiver Input to Output		●	30	140	200	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew		●		13		ns
t_{ZL}	Receiver Enable to Output Low	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t_{ZH}	Receiver Enable to Output High	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
t_{LZ}	Receiver Disable from Low	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t_{HZ}	Receiver Disable from High	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
f_{MAX}	Maximum Data Rate		●	2.5			Mbits/s
t_{SHDN}	Time to Shutdown	DE = 0, $\overline{RE}$ = ⅃	●	50	200	600	ns
$t_{ZH(SHDN)}$	Driver Enable from Shutdown to Output High	C_L = 100pF (Figures 4, 6), S2 Closed	●		40	100	ns
$t_{ZL(SHDN)}$	Driver Enable from Shutdown to Output Low	C_L = 100pF (Figures 4, 6), S1 Closed	●		40	100	ns
$t_{ZH(SHDN)}$	Receiver Enable from Shutdown to Output High	C_L = 15pF (Figures 2, 8), S2 Closed	●			3500	ns
$t_{ZL(SHDN)}$	Receiver Enable from Shutdown to Output Low	C_L = 15pF (Figures 2, 8), S1 Closed	●			3500	ns

The ● denotes specifications which apply over the full operating temperature range.

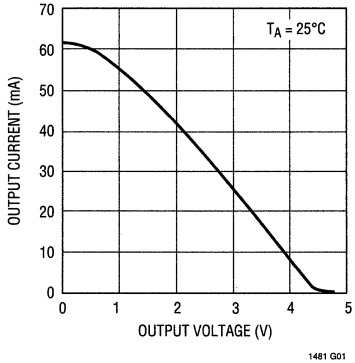
Note 1: Absolute maximum ratings are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out ot device pins are negative. All voltages are referenced to device ground unless otherwise specified.

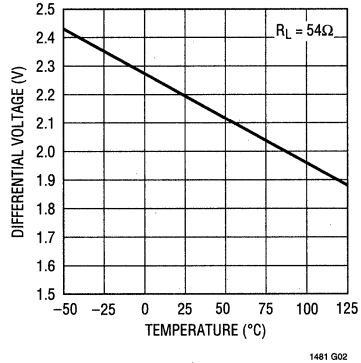
Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

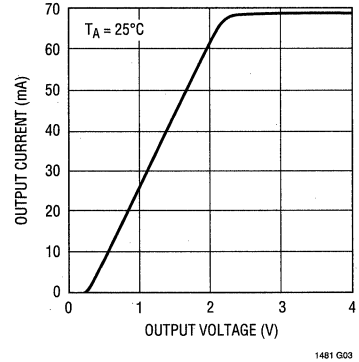
Driver Differential Output Voltage vs Output Current



Driver Differential Output Voltage vs Temperature

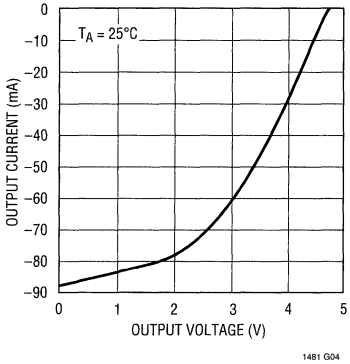


Driver Output Low Voltage vs Output Current

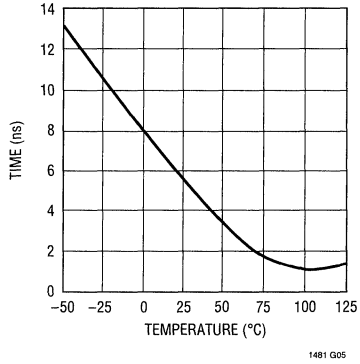


TYPICAL PERFORMANCE CHARACTERISTICS

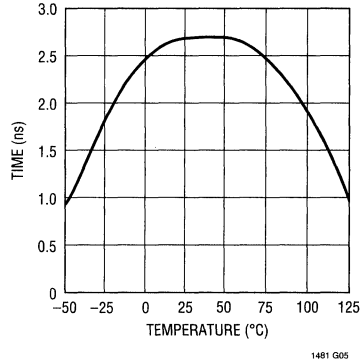
Driver Output High Voltage vs Output Current



Receiver $|t_{PLH} - t_{PHL}|$ vs Temperature



Driver Skew vs Temperature



PIN FUNCTIONS

RO (Pin 1): Receiver Output. If the receiver output is enabled ($\overline{RE}$ low), then if A > B by 200mV, RO will be high. If A < B by 200mV, then RO will be low.

$\overline{RE}$ (Pin 2): Receiver Output Enable. A low enables the receiver output, RO. A high input forces the receiver output into a high impedance state.

DE (Pin 3): Driver Outputs Enable. A high on DE enables the driver output. A, B and the chip will function as a line driver. A low input will force the driver outputs into a high impedance state and the chip will function as a line receiver. If $\overline{RE}$ is high and DE is low, the part will enter a low power (1μA) shutdown state.

DI (Pin 4): Driver Input. If the driver outputs are enabled (DE high) then a low on DI forces the outputs A low and B high. A high on DI with the driver outputs enabled will force A high and B low.

GND (Pin 5): Ground.

A (Pin 6): Driver Output/Receiver Input.

B (Pin 7): Driver Output/Receiver Input.

V_{CC} (Pin 8): Positive Supply. 4.75V < V_{CC} < 5.25V.

5

FUNCTION TABLES

LTC1481 Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Z	Z
1	0	X	Z*	Z*

*Shutdown mode for LTC1481

LTC1481 Receiving

INPUTS			OUTPUTS
$\overline{RE}$	DE	A – B	RO
0	0	≥0.2V	1
0	0	≤–0.2V	0
0	0	Inputs Open	1
1	0	X	Z*

*Shutdown mode for LTC1481

TEST CIRCUITS

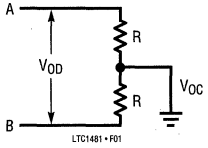


Figure 1. Driver DC Test Load

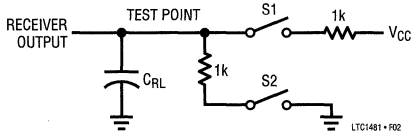


Figure 2. Receiver Timing Test Load

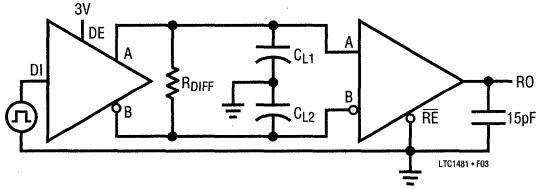


Figure 3. Driver/Receiver Timing Test Circuit

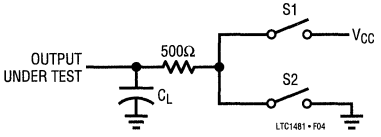


Figure 4. Driver Timing Test Load

SWITCHING TIME WAVEFORMS

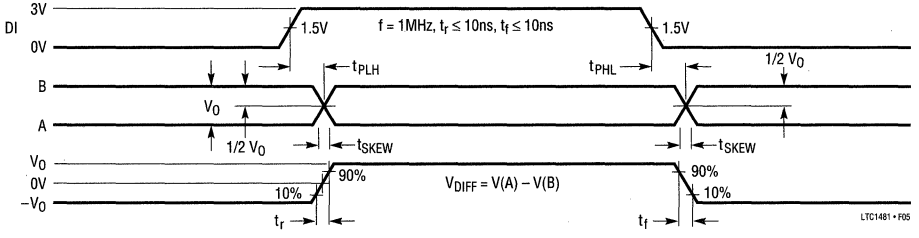


Figure 5. Driver Propagation Delays

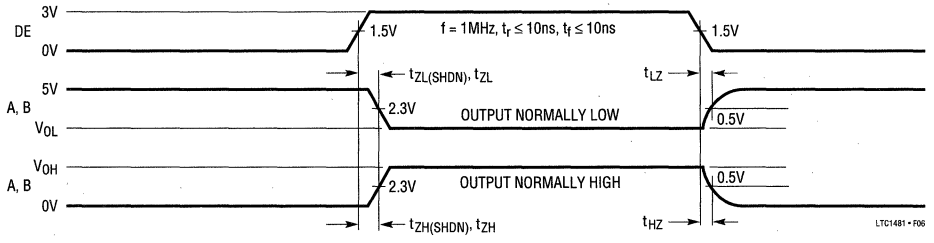


Figure 6. Driver Enable and Disable Times

SWITCHING TIME WAVEFORMS

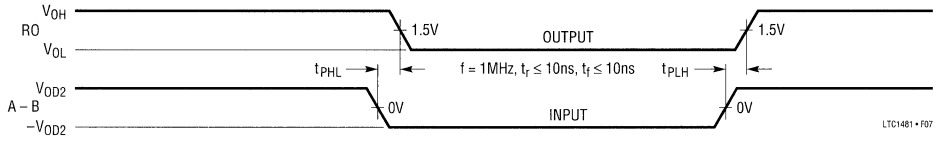


Figure 7. Receiver Propagation Delays

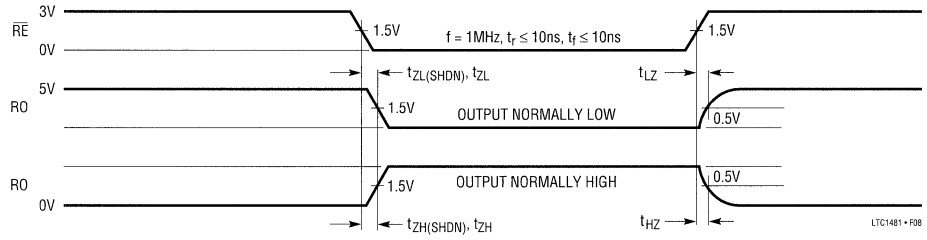


Figure 8. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

5

Basic Theory of Operation

Traditionally, RS485 transceivers have been designed using bipolar technology because the common-mode range of the device must extend beyond the supplies and the device must be immune to ESD damage and latch-up. Unfortunately, most bipolar devices draw a large amount of supply current, which is unacceptable for the numerous applications that require low power consumption. The LTC1481 is a CMOS RS485/RS422 transceiver which features ultra-low power consumption without sacrificing ESD and latch-up immunity.

The LTC1481 uses a proprietary driver output stage, which allows a common-mode range that extends beyond the power supplies while virtually eliminating latch-up and providing excellent ESD protection. Figure 9 shows the LTC1481 output stage while Figure 10 shows a conventional CMOS output stage.

When the conventional CMOS output stage of Figure 10 enters a high impedance state, both the P-channel (P1) and the N-channel (N1) are turned off. If the output is then driven above V_{CC} or below ground, the P+/N-well diode (D1) or the N+/P-substrate diode (D2) respectively will turn on and clamp the output to the supply. Thus, the output stage is no longer in a high impedance state and is not able to meet the RS485 common-mode range requirement. In addition, the large amount of current flowing through either diode will induce the well-known CMOS latch-up condition, which could destroy the device.

The LTC1481 output stage of Figure 9 eliminates these problems by adding two Schottky diodes, SD3 and SD4. The Schottky diodes are fabricated by a proprietary modification to the standard N-well CMOS process. When the output stage is operating normally, the Schottky diodes are forward biased and have a small voltage drop across them. When the output is in the high impedance state and is driven above V_{CC} or below ground, the parasitic diode D1 or D2 still turns on, but SD3 or SD4 will reverse bias and prevent current from flowing into the N-well or the substrate. Thus the high impedance state is maintained even with the output voltage beyond the supplies. With no minority carrier current flowing into the N-well or substrate, latch-up is virtually eliminated under power-up or power-down conditions.

APPLICATIONS INFORMATION

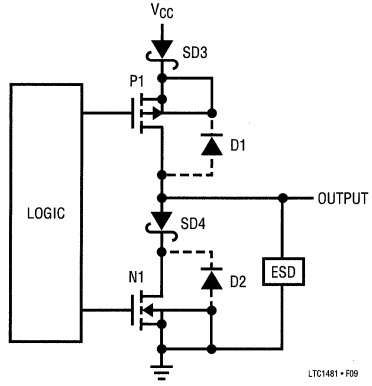


Figure 9. LTC1481 Output Stage

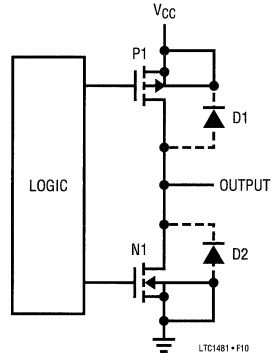


Figure 10. Conventional CMOS Output Stage

The LTC1481 output stage will maintain a high impedance state until the breakdown of the N-channel or P-channel is reached when going positive or negative respectively. The output will be clamped to either V_{CC} or ground by a Zener voltage plus a Schottky diode drop, but this voltage is well beyond the RS485 operating range. Because the ESD injected current in the N-well or substrate consists of majority carriers, latch-up is prevented by careful layout techniques. An ESD cell protects output against multiple 10kV human body model ESD strikes.

Low Power Operation

The LTC1481 is designed to operate with a quiescent current of 120µA max. With the driver in three-state, I_{CC} will drop to this 120µA level. With the driver enabled there will be additional current drawn by the internal 12k resistor. Under normal operating conditions this additional current is overshadowed by the current drawn by the external bus impedance.

Shutdown Mode

Both the receiver output (RO) and the driver outputs (A, B) can be placed in three-state mode by bringing $\overline{RE}$ high and DE low respectively. In addition, the LTC1481 will enter shutdown mode when $\overline{RE}$ is high and DE is low.

In shutdown the LTC1481 typically draws only 1µA of supply current. In order to guarantee that the part goes into shutdown, DE must be low and $\overline{RE}$ must be high for at least 600ns simultaneously. If this time duration is less than 50ns the part will not enter shutdown mode. Toggling either $\overline{RE}$ or DE will wake the LTC1481 back up within 3.5µs.

Propagation Delay

Many digital encoding schemes are dependent upon the difference in the propagation delay times of the driver and receiver. Figure 11 shows the test circuit for the LTC1481 propagation delay.

The receiver delay times are:

$|t_{PLH} - t_{PHL}|$ = 13ns Typ, V_{CC} = 5V

The drivers skew times are:

Skew = 5ns Typ, V_{CC} = 5V

10ns Max, V_{CC} = 5V, T_A = –40°C to 85°C

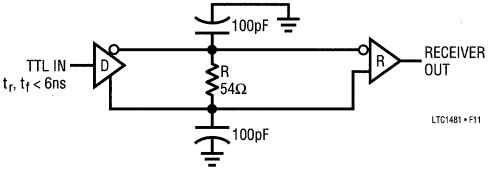


Figure 11. Receiver Propagation Delay Test Circuit

Ultra-Low Power RS485 Low EMI Transceiver with Shutdown

FEATURES

- **Low Power: I_{CC} = 120μA Max with Driver Disabled**
- I_{CC} = 500μA Max with Driver Enabled, No Load
- **1μA Quiescent Current in Shutdown Mode**
- Controlled Slew Rate Driver for Reduced EMI
- Single 5V Supply
- **Drivers/Receivers Have ±10kV ESD Protection**
- –7V to 12V Common-Mode Range Permits ±7V Ground Difference Between Devices on the Data Line
- Thermal Shutdown Protection
- Power Up/Down Glitch-Free Driver Outputs Permit Live Insertion or Removal of Transceiver
- Driver Maintains High Impedance in Three-State or with the Power Off
- Up to 32 Transceivers on the Bus
- Pin Compatible with the LTC485

APPLICATIONS

- Battery-Powered RS485/RS422 Applications
- Low Power RS485/RS422 Transceiver
- Level Translator

DESCRIPTION

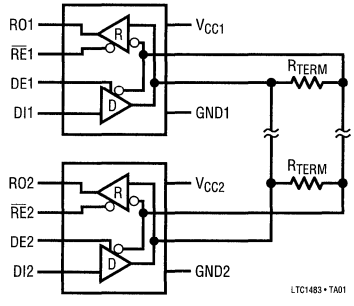
The LTC®1483 is an ultra-low power differential line transceiver designed for data transmission standard RS485 applications with extended common-mode range (–7V to 12V). It will also meet the requirements of RS422. The LTC1483 features output drivers with controlled slew rate, decreasing the EMI radiated from the RS485 lines, and improving signal fidelity with misterminated lines. The CMOS design offers significant power savings over its bipolar counterparts without sacrificing ruggedness against overload or ESD damage. Typical quiescent current is only 80μA while operating and less than 1μA in shutdown.

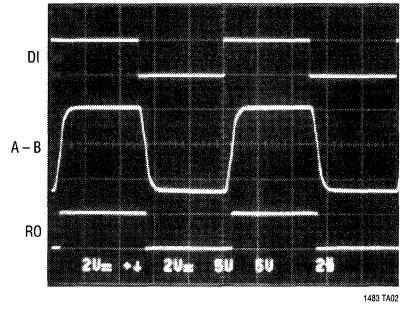
The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common-mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state. The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open. I/O pins are protected against multiple ESD strikes of over ±10kV.

The LTC1483 is fully specified over the commercial and extended industrial temperature range and is available in 8-pin DIP and SO packages.

5

TYPICAL APPLICATION



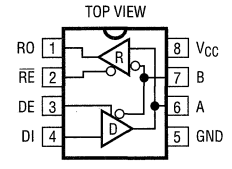


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 12V
Control Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Output Voltage ..... $\pm 14V$
Receiver Input Voltage ..... $\pm 14V$
Receiver Output Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Operating Temperature Range
LTC1483C ..... $0°C \le T_A \le 70°C$
LTC1483I ..... $-40°C \le T_A \le 85°C$
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX} = 125°C$, $\theta_{JA} = 130°C/W$ (N8)
$T_{JMAX} = 125°C$, $\theta_{JA} = 150°C/W$ (S8)

ORDER PART NUMBER
LTC1483CN8 LTC1483IN8 LTC1483CS8 LTC1483IS8
S8 PART MARKING
1483 1483I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$	●			5	V
V_{OD2}	Differential Driver Output Voltage (with Load)	R = 50Ω (RS422) R = 27Ω (RS485), Figure 1	● ●	2 1.5		 5	V V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{OC}	Driver Common-Mode Output Voltage	R = 27Ω or R = 50Ω, Figure 1	●			3	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{IH}	Input High Voltage	DE, DI, $\overline{RE}$	●	2			V
V_{IL}	Input Low Voltage	DE, DI, $\overline{RE}$	●			0.8	V
I_{IN1}	Input Current	DE, DI, $\overline{RE}$	●			±2	µA
I_{IN2}	Input Current (A, B)	DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = 12V DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = −7V	● ●			1.0 −0.8	mA mA
V_{TH}	Differential Input Threshold Voltage for Receiver	$-7V \le V_{CM} \le 12V$	●	−0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V	●		45		mV
V_{OH}	Receiver Output High Voltage	$I_O = -4mA$, $V_{ID} = 200mV$	●	3.5			V
V_{OL}	Receiver Output Low Voltage	$I_O = 4mA$, $V_{ID} = -200mV$	●			0.4	V
I_{OZR}	Three-State (High Impedance) Output Current at Receiver	V_{CC} = Max, $0.4V \le V_O \le 2.4V$	●			±1	µA
R_{IN}	Receiver Input Resistance	$-7V \le V_{CM} \le 12V$	●	12	25		kΩ
I_{CC}	Supply Current	No Load, Output Enabled No Load, Output Disabled	● ●		300 80	500 120	µA µA
I_{SHDN}	Supply Current in Shutdown Mode	DE = 0, $\overline{RE} = V_{CC}$			1	10	µA
I_{OSD1}	Driver Short-Circuit Current, V_{OUT} = HIGH	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSD2}	Driver Short-Circuit Current, V_{OUT} = LOW	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSR}	Receiver Short-Circuit Current	$0V \le V_O \le V_{CC}$	●	7		85	mA

SWITCHING CHARACTERISTICS

V_{CC} = 5V, (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1483 MIN	LTC1483 TYP	LTC1483 MAX	UNITS
t_{PLH}	Driver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3, 5)	●	150		1200	ns
t_{PHL}	Driver Input to Output		●	150		1200	ns
t_{SKEW}	Driver Output to Output		●		100	600	ns
t_r, t_f	Driver Rise or Fall Time		●	150		1200	ns
t_{ZH}	Driver Enable to Output High	C_L = 100pF (Figures 4, 6), S2 Closed	●	100		1500	ns
t_{ZL}	Driver Enable to Output Low	C_L = 100pF (Figures 4, 6), S1 Closed	●	100		1500	ns
t_{LZ}	Driver Disable Time from Low	C_L = 15pF (Figures 4, 6), S1 Closed	●	150		1500	ns
t_{HZ}	Driver Disable Time from High	C_L = 15pF (Figures 4, 6), S2 Closed	●	150		1500	ns
t_{PLH}	Receiver Input to Output	R_{DIFF} = 54Ω, C_{L1} = C_{L2} = 100pF, (Figures 3, 7)	●	30	140	200	ns
t_{PHL}	Receiver Input to Output		●	30	140	200	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew		●		13		ns
t_{ZL}	Receiver Enable to Output Low	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t_{ZH}	Receiver Enable to Output High	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
t_{LZ}	Receiver Disable from Low	C_{RL} = 15pF (Figures 2, 8), S1 Closed	●		20	50	ns
t_{HZ}	Receiver Disable from High	C_{RL} = 15pF (Figures 2, 8), S2 Closed	●		20	50	ns
f_{MAX}	Maximum Data Rate		●	250			kbits/s
t_{SHDN}	Time to Shutdown	DE = 0, $\overline{RE}$ = ⤓	●	50	200	600	ns
$t_{ZH(SHDN)}$	Driver Enable from Shutdown to Output High	C_L = 100pF (Figures 4, 6), S2 Closed	●			2000	ns
$t_{ZL(SHDN)}$	Driver Enable from Shutdown to Output Low	C_L = 100pF (Figures 4, 6), S1 Closed	●			2000	ns
$t_{ZH(SHDN)}$	Receiver Enable from Shutdown to Output High	C_L = 15pF (Figures 2, 8), S2 Closed	●			3500	ns
$t_{ZL(SHDN)}$	Receiver Enable from Shutdown to Output Low	C_L = 15pF (Figures 2, 8), S1 Closed	●			3500	ns

The ● denotes specifications which apply over the full operating temperature range.

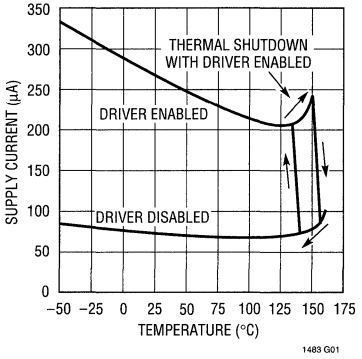
Note 1: Absolute maximum ratings are those beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out ot device pins are negative. All voltages are referenced to device ground unless otherwise specified.

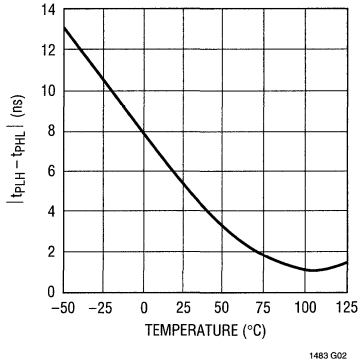
Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

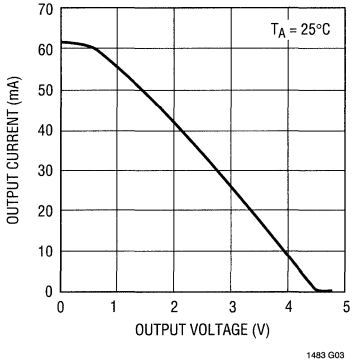
Supply Current vs Temperature



Receiver $\lvert t_{PLH} - t_{PHL} \rvert$ vs Temperature

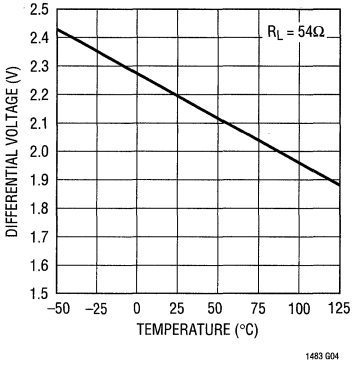


Driver Differential Output Voltage vs Output Current

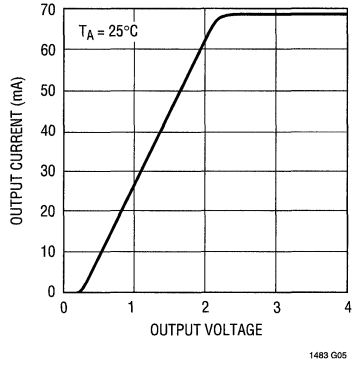


TYPICAL PERFORMANCE CHARACTERISTICS

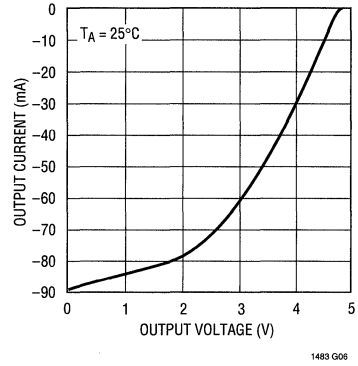
Driver Differential Output Voltage vs Temperature



Driver Output Low Voltage vs Output Current



Driver Output High Voltage vs Output Current



PIN FUNCTIONS

RO (Pin 1): Receiver Output. If the receiver output is enabled ($\overline{RE}$ low), then if A > B by 200mV, RO will be high. If A < B by 200mV, then RO will be low.

$\overline{RE}$ (Pin 2): Receiver Output Enable. A low enables the receiver output, RO. A high input forces the receiver output into a high impedance state.

DE (Pin 3): Driver Outputs Enable. A high on DE enables the driver output. A, B and the chip will function as a line driver. A low input will force the driver outputs into a high impedance state and the chip will function as a line receiver. If $\overline{RE}$ is high and DE is low, the part will enter a low power (1μA) shutdown state.

DI (Pin 4): Driver Input. If the driver outputs are enabled (DE high) then a low on DI forces the outputs A low and B high. A high on DI with the driver outputs enabled will force A high and B low.

GND (Pin 5): Ground.

A (Pin 6): Driver Output/Receiver Input.

B (Pin 7): Driver Output/Receiver Input.

V_{CC} (Pin 8): Positive Supply. 4.75V < V_{CC} < 5.25V.

FUNCTION TABLES

LTC1483 Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Z	Z
1	0	X	Z*	Z*

*Shutdown mode for LTC1483

LTC1483 Receiving

INPUTS			OUTPUTS
$\overline{RE}$	DE	A – B	RO
0	0	≥0.2V	1
0	0	≤–0.2V	0
0	0	Inputs Open	1
1	0	X	Z*

*Shutdown mode for LTC1483

TEST CIRCUITS

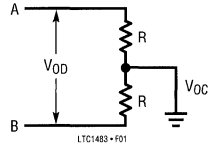


Figure 1. Driver DC Test Load

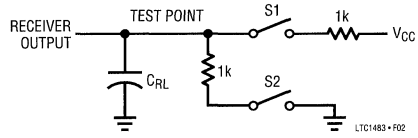


Figure 2. Receiver Timing Test Load

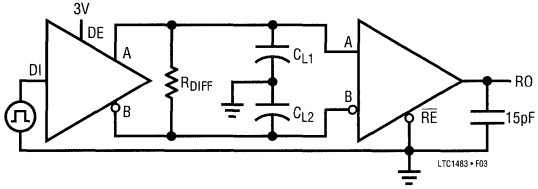


Figure 3. Driver/Receiver Timing Test Circuit

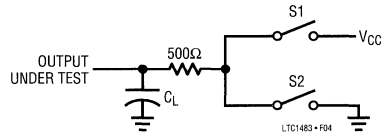


Figure 4. Driver Timing Test Load

SWITCHING TIME WAVEFORMS

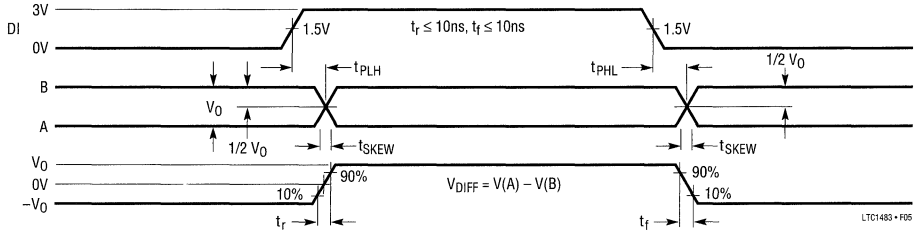


Figure 5. Driver Propagation Delays

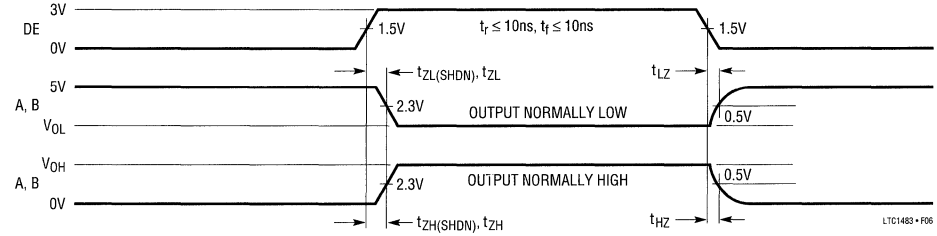


Figure 6. Driver Enable and Disable Times

SWITCHING TIME WAVEFORMS

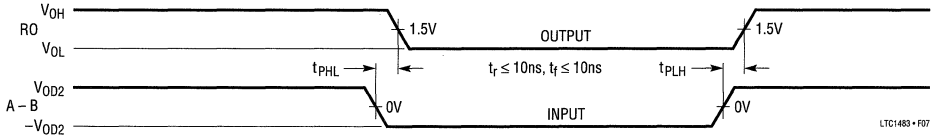


Figure 7. Receiver Propagation Delays

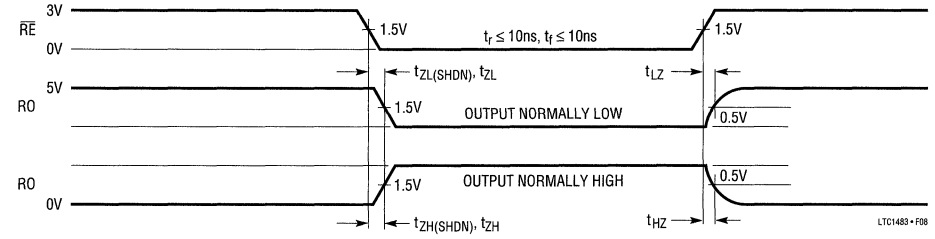


Figure 8. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

Basic Theory of Operation

Traditionally RS485 transceivers have been designed using bipolar technology because the common-mode range of the device must extend beyond the supplies and the device must be immune to ESD damage and latch-up. Unfortunately, most bipolar devices draw a large amount of supply current, which is unacceptable for the numerous applications that require low power consumption. The LTC1483 is a CMOS RS485/RS422 transceiver which features ultra-low power consumption without sacrificing ESD and latch-up immunity.

The LTC1483 uses a proprietary driver output stage, which allows a common-mode range that extends beyond the power supplies while virtually eliminating latch-up and providing excellent ESD protection. Figure 9 shows the LTC1483 output stage while Figure 10 shows a conventional CMOS output stage.

When the conventional CMOS output stage of Figure 10 enters a high impedance state, both the P-channel (P1) and the N-channel (N1) are turned off. If the output is then driven above V_{CC} or below ground, the P+/N-well diode (D1) or the N+/P-substrate diode (D2) respectively will turn on and clamp the output to the supply. Thus, the output stage is no longer in a high impedance state and is not able to meet the RS485 common-mode range requirement. In addition, the large amount of current flowing through either diode will induce the well-known CMOS latch-up condition, which could destroy the device.

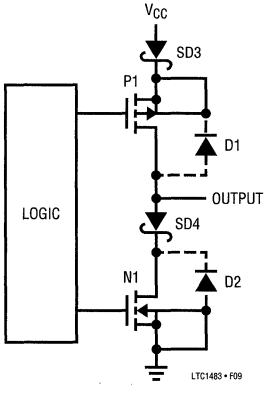


Figure 9. LTC1483 Output Stage

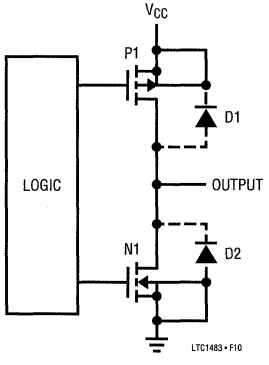


Figure 10. Conventional CMOS Output Stage

APPLICATIONS INFORMATION

The LTC1483 output stage of Figure 9 eliminates these problems by adding two Schottky diodes, SD3 and SD4. The Schottky diodes are fabricated by a proprietary modification to the standard N-well CMOS process. When the output stage is operating normally, the Schottky diodes are forward biased and have a small voltage drop across them. When the output is in the high impedance state and is driven above V_{CC} or below ground, the parasitic diode D1 or D2 still turns on, but SD3 or SD4 will reverse bias and prevent current from flowing into the N-well or the substrate. Thus the high impedance state is maintained even with the output voltage beyond the supplies. With no minority carrier current flowing into the N-well or substrate, latch-up is virtually eliminated under power-up or power-down conditions.

The LTC1483 output stage will maintain a high impedance state until the breakdown of the N-channel or P-channel is reached when going positive or negative respectively. The output will be clamped to either V_{CC} or ground by a Zener voltage plus a Schottky diode drop, but this voltage is well beyond the RS485 operating range. An ESD cell protects output against multiple ±10kV human body model ESD strikes. Because the ESD injected current in the N-well or substrate consists of majority carriers, latch-up is prevented by careful layout techniques.

Slew Rate

The LTC1483 is designed for systems that are sensitive to electromagnetic radiation. The part features a slew rate limited driver that reduces high frequency electromagnetic emissions, while improving signal fidelity by reducing reflections due to misterminated cables. Figures 11 and 12 show the spectrum of the signal at the driver output for a standard slew rate RS485 driver and the slew rate limited LTC1483. The LTC1483 shows significant reduction of the high frequency harmonics. Because the driver is slew rate limited, the maximum operating frequency is limited to 250kbits/s.

Low Power Operation

The LTC1483 is designed to operate with a quiescent current of 120µA max. With the driver in three-state I_{CC} will drop to this 120µA level. With the driver enabled there will be additional current drawn by the internal 12k resistor. Under normal operating conditions this additional current is overshadowed by the current drawn by the external bus impedance.

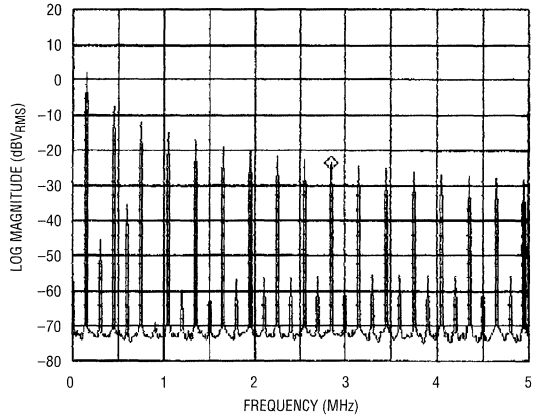


Figure 11. Typical RS485 Driver Output Spectrum Transmitting at 150kHz

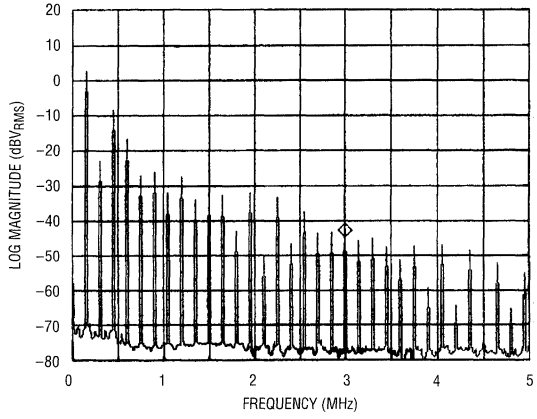


Figure 12. Slew Rate Limited LTC1483 Driver Output Spectrum Transmitting at 150kHz

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APPLICATIONS INFORMATION

Shutdown Mode

Both the receiver output (RO) and the driver outputs (A, B) can be placed in three-state mode by bringing $\overline{RE}$ high and DE low respectively. In addition, the LTC1483 will enter shutdown mode when $\overline{RE}$ is high and DE is low.

In shutdown the LTC1483 typically draws only 1μA of supply current. In order to guarantee that the part goes into shutdown, $\overline{RE}$ must be high and DE must be low for at least 600ns simultaneously. If this time duration is less than 50ns the part will not enter shutdown mode. Toggling either $\overline{RE}$ or DE will wake the LTC1483 back up within 3.5μs.

If the slow slew rate driver was active immediately prior to shutdown, the supply current will not drop to 1μA until the driver outputs have reached a steady state; this can take as long as 2.6μs under worst case conditions. If the driver was disabled prior to shutdown the supply current will drop to 1μA immediately.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC485	5V Low Power RS485 Interface Transceiver	Low Power
LTC1480	3.3V Ultra-Low Power RS485 Transceiver	World's First 3V Powered 485 Transceiver with Low Power Consumption
LTC1481	5V Ultra-Low Power RS485 Transceiver with Shutdown	Lowest Power
LTC1485	5V Differential Bus Transceiver	Highest Speed
LTC1487	5V Ultra-Low Power RS485 with Low EMI Shutdown and High Input Impendance	High Input Impendance/Low EMI/Lowest Power

Ultra-Low Power RS485 with Low EMI, Shutdown and High Input Impedance

FEATURES

- **High Input Impedance: Up to 256 Transceivers on the Bus**
- **Low Power: I_{CC} = 120μA Max with Driver Disabled**
- I_{CC} = 200μA Max with Driver Enabled, No Load
- **1μA Quiescent Current in Shutdown Mode**
- Controlled Slew Rate Driver for Reduced EMI
- Single 5V Supply
- ESD Protection to ±10kV On Receiver Inputs and Driver outputs
- –7V to 12V Common-Mode Range Permits ±7V Ground Difference Between Devices on the Data Line
- Thermal Shutdown Protection
- Power Up/Down Glitch-Free Driver Outputs Permit Live Insertion or Removal of Transceiver
- Driver Maintains High Impedance in Three-State or with the Power Off
- Pin Compatible with the LTC485

APPLICATIONS

- Battery-Powered RS485/RS422 Applications
- Low Power RS485/RS422 Transceiver
- Level Translator

DESCRIPTION

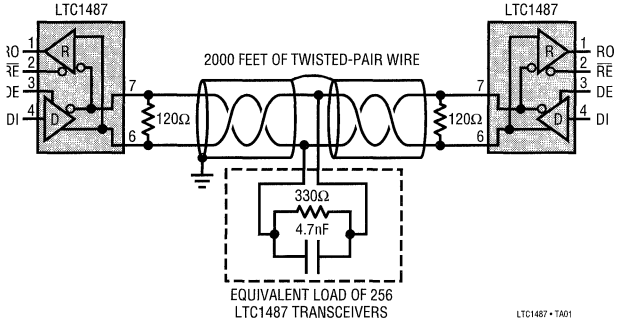
The LTC®1487 is an ultra-low power differential line transceiver designed with high impedance inputs allowing up to 256 transceivers to share a single bus. It meets the requirements of RS485 and RS422. The LTC1487 features output drivers with controlled slew rate, decreasing the EMI radiated from the RS485 lines, and improving signal fidelity with misterminated lines. The CMOS design offers significant power savings without sacrificing ruggedness against overload or ESD damage. Typical quiescent current is only 80μA while operating and 1μA in shutdown.

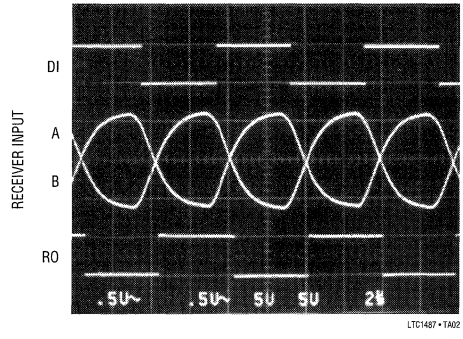
The driver and receiver feature three-state outputs, with the driver outputs maintaining high impedance over the entire common-mode range. Excessive power dissipation caused by bus contention or faults is prevented by a thermal shutdown circuit which forces the driver outputs into a high impedance state. The receiver has a fail-safe feature which guarantees a high output state when the inputs are left open. I/O pins are protected against multiple ESD strikes of over ±10kV using the Human Body Model.

The LTC1487 is fully specified over the commercial temperature range and is available in 8-pin DIP and SO packages.

5

TYPICAL APPLICATION



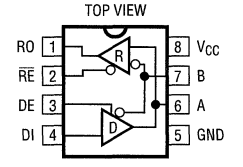


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 12V
Control Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Input Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Driver Output Voltage ..... $\pm 14V$
Receiver Input Voltage ..... $\pm 14V$
Receiver Output Voltage ..... $-0.5V$ to $V_{CC} + 0.5V$
Operating Temperature Range ..... $0°C \le T_A \le 70°C$
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX} = 125°C$, $\theta_{JA} = 130°C/W$ (N8)
$T_{JMAX} = 125°C$, $\theta_{JA} = 150°C/W$ (S8)

ORDER PART NUMBER
LTC1487CN8 LTC1487CS8 LTC1487IN8 LTC1487IS8
S8 PART MARKING
1487 1487I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_{CC} = 5V$ (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$	●			5	V
V_{OD2}	Differential Driver Output Voltage (with Load)	R = 50Ω (RS422) R = 27Ω (RS485), Figure 1	● ●	2.0 1.5		 5	V V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{OC}	Driver Common-Mode Output Voltage	R = 27Ω or R = 50Ω, Figure 1	●			3	V
$\Delta \lvert V_{OC} \rvert$	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	R = 27Ω or R = 50Ω, Figure 1	●			0.2	V
V_{IH}	Input High Voltage	DE, DI, $\overline{RE}$	●	2			V
V_{IL}	Input Low Voltage	DE, DI, $\overline{RE}$	●			0.8	V
I_{IN1}	Input Current	DE, DI, $\overline{RE}$	●			±2	µA
I_{IN2}	Input Current (A, B)	DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = 12V DE = 0, V_{CC} = 0V or 5.25V, V_{IN} = −7V	● ●			0.30 −0.15	mA mA
V_{TH}	Differential Input Threshold Voltage for Receiver	$-7V \le V_{CM} \le 12V$	●	−0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	V_{CM} = 0V	●		45		mV
V_{OH}	Receiver Output High Voltage	$I_O = -4mA$, $V_{ID} = 200mV$	●	3.5			V
V_{OL}	Receiver Output Low Voltage	$I_O = 4mA$, $V_{ID} = -200mV$	●			0.4	V
I_{OZR}	Three-State (High Impedance) Output Current at Receiver	V_{CC} = Max, $0.4V \le V_O \le 2.4V$	●			±1	µA
R_{IN}	Receiver Input Resistance	$-7V \le V_{CM} \le 12V$	●	70	96		kΩ
I_{CC}	Supply Current	No Load, Output Enabled No Load, Output Disabled	● ●		120 80	200 120	µA µA
I_{SHDN}	Supply Current in Shutdown Mode	DE = 0V, $\overline{RE} = V_{CC}$			1	10	µA
I_{OSD1}	Driver Short-Circuit Current, V_{OUT} = HIGH	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSD2}	Driver Short-Circuit Current, V_{OUT} = LOW	$-7V \le V_O \le 12V$	●	35		250	mA
I_{OSR}	Receiver Short-Circuit Current	$0V \le V_O \le V_{CC}$	●	7		85	mA

ELECTRICAL CHARACTERISTICS

$-40°C \le T_A \le 85°C$, $V_{CC} = 5V$ (Note 4) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD1}	Differential Driver Output Voltage (Unloaded)	$I_O = 0$	●			5	V
V_{OD2}	Differential Driver Output Voltage (with Load)	R = 50Ω (RS422) R = 27Ω (RS485), Figure 1	● ●	2.0 1.5		 5	V V
V_{OC}	Driver Common-Mode Output Voltage	R = 27Ω or R = 50Ω, Figure 1	●			3	V
V_{TH}	Differential Input Threshold Voltage for Receiver	$-7V \le V_{CM} \le 12V$	●	−0.2		0.2	V
ΔV_{TH}	Receiver Input Hysteresis	$V_{CM} = 0V$	●		45		mV
I_{CC}	Supply Current	No Load, Output Enabled No Load, Output Disabled	● ●		120 80	200 120	µA µA
I_{SHDN}	Supply Current in Shutdown Mode	DE = 0V, $\overline{RE} = V_{CC}$			1	10	µA
t_{PLH}	Driver Input to Output	$R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$, (Figures 3, 5)	●	150		1200	ns
t_{PHL}	Driver Input to Output		●	150		1200	ns
t_{SKEW}	Driver Output to Output		●		100	600	ns
t_r, t_f	Driver Rise or Fall Time		●	150		2000	ns
t_{PLH}	Receiver Input to Output	$R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$, (Figures 3, 7)	●	30	140	250	ns
t_{PHL}	Receiver Input to Output		●	30	140	250	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew		●		13		ns
f_{MAX}	Maximum Data Rate		●	250			kbps

SWITCHING CHARACTERISTICS

$0°C \le T_A \le 70°C$, $V_{CC} = 5V$ (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Driver Input to Output	$R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$, (Figures 3, 5)	●	150		1200	ns
t_{PHL}	Driver Input to Output		●	150		1200	ns
t_{SKEW}	Driver Output to Output		●		250	600	ns
t_r, t_f	Driver Rise or Fall Time		●	150		1200	ns
t_{ZH}	Driver Enable to Output High	$C_L = 100pF$ (Figures 4, 6), S2 Closed	●	100		1500	ns
t_{ZL}	Driver Enable to Output Low	$C_L = 100pF$ (Figures 4, 6), S1 Closed	●	100		1500	ns
t_{LZ}	Driver Disable Time from Low	$C_L = 15pF$ (Figures 4, 6), S1 Closed	●	150		1500	ns
t_{HZ}	Driver Disable Time from High	$C_L = 15pF$ (Figures 4, 6), S2 Closed	●	150		1500	ns
t_{PLH}	Receiver Input to Output	$R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$, (Figures 3, 7)	●	30	140	250	ns
t_{PHL}	Receiver Input to Output		●	30	140	250	ns
t_{SKD}	$\lvert t_{PLH} - t_{PHL} \rvert$ Differential Receiver Skew		●		13		ns
t_{ZL}	Receiver Enable to Output Low	$C_{RL} = 15pF$ (Figures 2, 8), S1 Closed	●		20	50	ns
t_{ZH}	Receiver Enable to Output High	$C_{RL} = 15pF$ (Figures 2, 8), S2 Closed	●		20	50	ns
t_{LZ}	Receiver Disable from Low	$C_{RL} = 15pF$ (Figures 2, 8), S1 Closed	●		20	50	ns
t_{HZ}	Receiver Disable from High	$C_{RL} = 15pF$ (Figures 2, 8), S2 Closed	●		20	50	ns
f_{MAX}	Maximum Data Rate		●	250			kbps
t_{SHDN}	Time to Shutdown	DE = 0, $\overline{RE}$ =	●	50	200	600	ns

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SWITCHING CHARACTERISTICS

$0°C \le TA \le 70°C$, $V_{CC} = 5V$ (Notes 2, 3) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{ZH(SHDN)}$	Driver Enable from Shutdown to Output High	C_L = 100pF (Figures 4, 6), S2 Closed	●			2000	ns
$t_{ZL(SHDN)}$	Driver Enable from Shutdown to Output Low	C_L = 100pF (Figures 4, 6), S1 Closed	●			2000	ns
$t_{ZH(SHDN)}$	Receiver Enable from Shutdown to Output High	C_L = 15pF (Figures 2, 8), S2 Closed	●			2000	ns
$t_{ZL(SHDN)}$	Receiver Enable from Shutdown to Output Low	C_L = 15pF (Figures 2, 8), S1 Closed	●			2000	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those beyond which the safety of the device cannot be guaranteed.

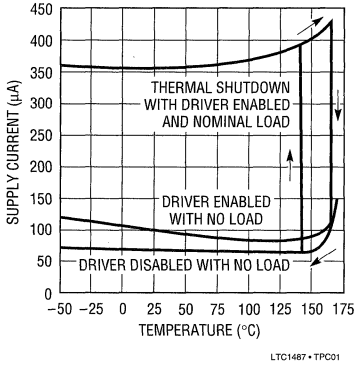
Note 2: All currents into device pins are positive; all currents out ot device pins are negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V and T_A = 25°C.

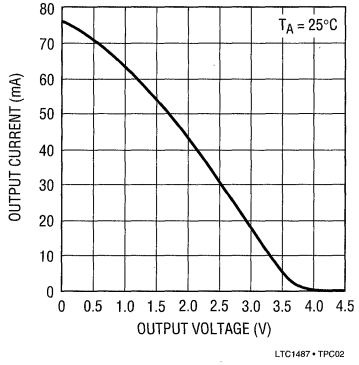
Note 4: The LTC1487 is not tested and is not quality-assurance sampled at –40°C and at 85°C. These specifications are guaranteed by design, correlation, and/or inference from 0°C, 25°C and/or 70°C tests.

TYPICAL PERFORMANCE CHARACTERISTICS

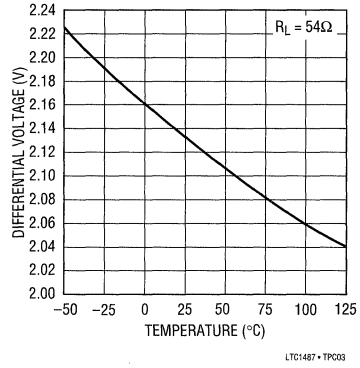
Supply Current vs Temperature



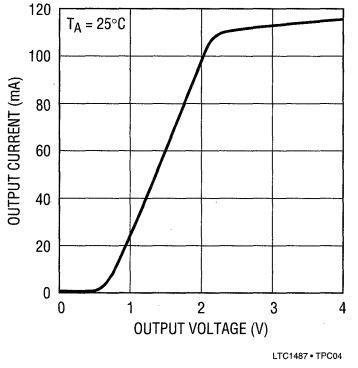
Driver Differential Output Voltage vs Output Current



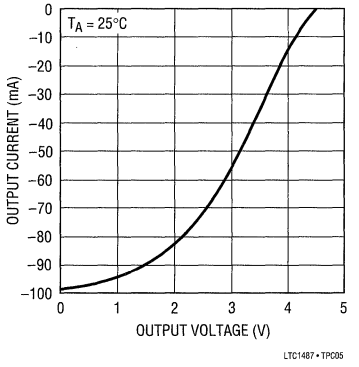
Driver Differential Output Voltage vs Temperature



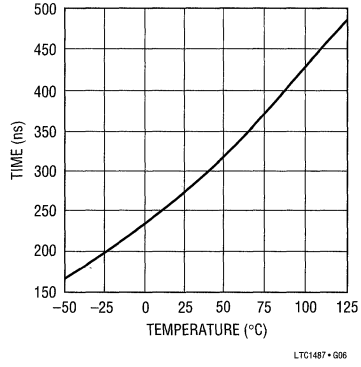
Driver Output Low Voltage vs Output Current



Driver Output High Voltage vs Output Current



Driver Skew vs Temperature



PIN FUNCTIONS

RO (Pin 1): Receiver Output. If the receiver output is enabled ($\overline{RE}$ LOW), and A > B by 200mV, RO will be HIGH. If A < B by 200mV, then RO will be LOW.

$\overline{RE}$ (Pin 2): Receiver Output Enable. A LOW enables the receiver output, RO. A HIGH input forces the receiver output into a high impedance state.

DE (Pin 3): Driver Outputs Enable. A HIGH on DE enables the driver output. A and B and the chip will function as a line driver. A LOW input will force the driver outputs into a high impedance state and the chip will function as a line receiver. If $\overline{RE}$ is HIGH and DE is LOW, the part will enter a low power (1µA) shutdown state.

DI (Pin 4): Driver Input. If the driver outputs are enabled (DE HIGH) then a LOW on DI forces the outputs A LOW and B HIGH. A HIGH on DI with the driver outputs enabled will force A HIGH and B LOW.

GND (Pin 5): Ground.

A (Pin 6): Driver Output/Receiver Input.

B (Pin 7): Driver Output/Receiver Input.

V_{CC} (Pin 8): Positive Supply. 4.75V < V_{CC} < 5.25V.

FUNCTION TABLES

LTC1487 Transmitting

INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	Z	Z
1	0	X	Z*	Z*

*Shutdown mode

LTC1487 Receiving

INPUTS			OUTPUTS
$\overline{RE}$	DE	A – B	RO
0	0	≥0.2V	1
0	0	≤–0.2V	0
0	0	Inputs Open	1
1	0	X	Z*

*Shutdown mode

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TEST CIRCUITS

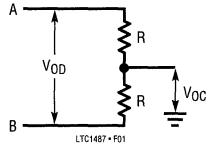

Figure 1. Driver DC Test Load

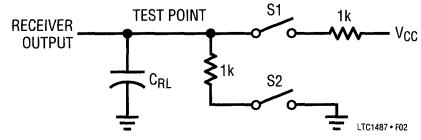

Figure 2. Receiver Timing Test Load

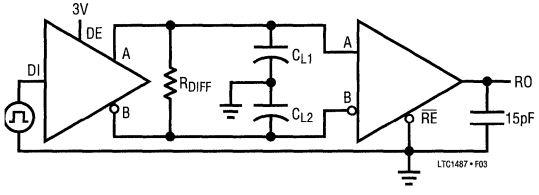

Figure 3. Driver/Receiver Timing Test Circuit

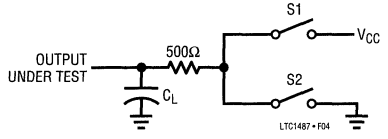

Figure 4. Driver Timing Test Load

SWITCHING TIME WAVEFORMS

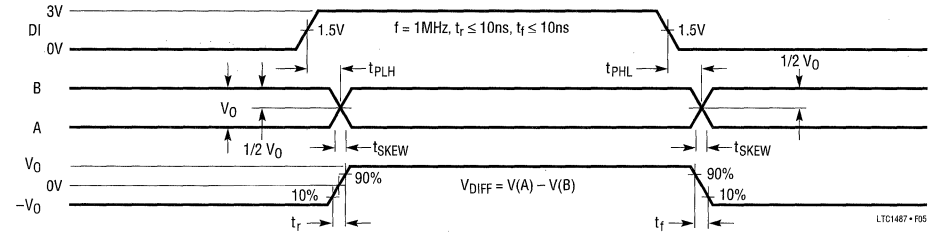

Figure 5. Driver Propagation Delays

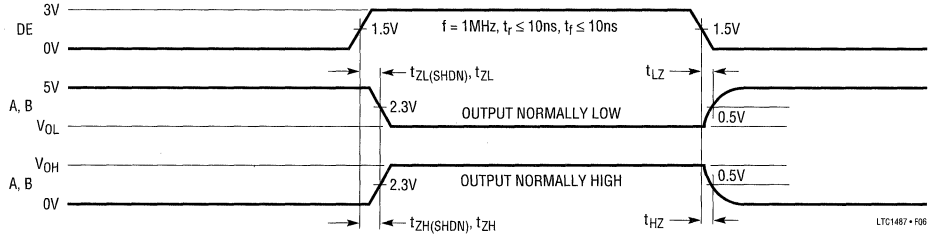

Figure 6. Driver Enable and Disable Times

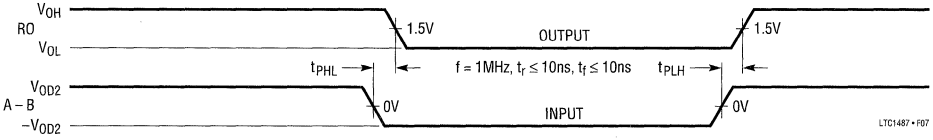

Figure 7. Receiver Propagation Delays

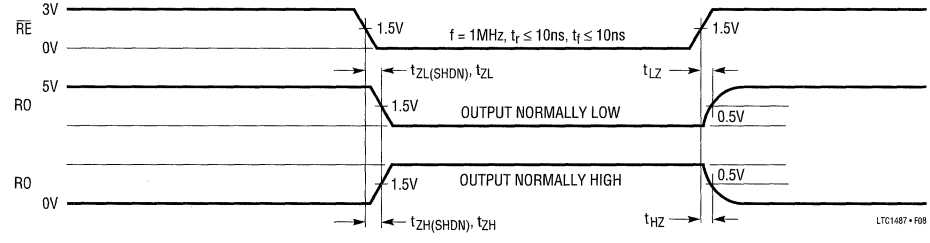

Figure 8. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

High Input Impedance

The LTC1487 is designed with a 96kΩ (typ) input impedance to allow up to 256 transceivers to share a single RS485 differential data bus. The RS485 specification requires that a transceiver be able to drive as many as 32 "unit loads." One unit load (UL) is defined as an impedance that draws a maximum of 1mA with up to 12V across it. Typical RS485 transceivers present between 0.5 and 1 unit load at their inputs. The 96kΩ input impedance of the LTC1487 will draw only 125µA under the same 12V condition, presenting only 0.125UL to the bus. As a result, 256 LTC1487 transceivers (32UL/0.125UL = 256) can be connected to a single RS485 data bus without exceeding the RS485 driver load specification. The LTC1487 meets all other RS485 specifications, allowing it to operate equally well with standard RS485 transceiver devices or high impedance transceivers.

CMOS Output Driver

The RS485 specification requires that a transceiver withstand common-mode voltages of up to 12V or –7V at the RS485 line connections. Additionally, the transceiver must be immune to both ESD and latch-up. This rules out traditional CMOS drivers, which include parasitic diodes from their driver outputs to each supply rail (Figure 9). The LTC1487 uses a proprietary process enhancement which adds a pair of Schottky diodes to the output stage (Figure 10), preventing current from flowing when the common-mode voltage exceeds the supply rails. Latch-up at the output drivers is virtually eliminated and the driver is prevented from loading the line under RS485 specified fault conditions. A proprietary output protection structure protects the transceiver line terminals against ESD strikes (Human Body Model) of up to ±10kV.

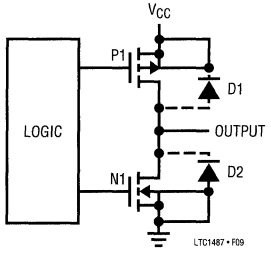

Figure 9. Conventional CMOS Output Stage

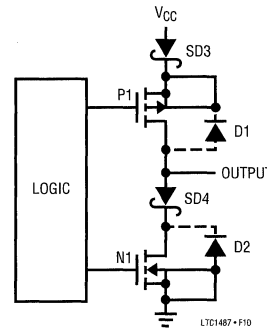

Figure 10. LTC1487 Output Stage

When two or more drivers are connected to the same transmission line, a potential condition exists whereby more than two drivers are simultaneously active. If one or more drivers is sourcing current while another driver is sinking current, excessive power dissipation may occur within either the sourcing or sinking element. This condition is defined as driver contention, since multiple drivers are competing for one transmission line. The LTC1487 provides a current limiting scheme to prevent driver contention failure. When driver contention occurs, the current drawn is limited to about 70mA, preventing excessive power dissipation within the drivers.

The LTC1487 has a thermal shutdown feature which protects the part from excessive power dissipation. Under extreme fault conditions, up to 250mA can flow through the part, causing rapid internal temperature rise. The thermal shutdown circuit will disable the driver outputs when the internal temperature reaches 150°C and turns them back on when the temperature cools to 130°C. This cycle will repeat as necessary until the fault condition is removed.

Receiver Inputs

The LTC1487 receiver features an input common-mode range covering the entire RS485 specified range of –7V to 12V. Internal 96k input resistors from each line terminal to ground provide the 0.125UL load to the RS485 bus. Differential signals of greater than ±200mV within the specified input common-mode range will be converted to a TTL-compatible signal at the receiver output. A small amount of input hysteresis is included to minimize the

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APPLICATIONS INFORMATION

effects of noise on the line signals. If the line is terminated or the receiver inputs are shorted together, the receiver output will retain the last valid line signal due to the 45mV of hysteresis incorporated in the receiver circuit. If the LTC1487 transceiver inputs are left floating (unterminated), an internal pull-up of 10μA at the A input will force the receiver output to a known high state.

Low Power Operation

The LTC1487 draws very little supply current whenever the driver outputs are disabled. In shutdown mode, the quiescent current is typically less than 1μA. With the receiver active and the driver outputs disabled, the LTC1487 will typically draw 80μA quiescent current. With the driver outputs enabled but unterminated, quiescent current will rise slightly as one of the two outputs sources current into the internal receiver input resistance. With the minimum receiver input resistance of 70k and the maximum output swing of 5V, the quiescent current will rise by a maximum of 72μA. Typical quiescent current rise with the driver enabled is about 40μA.

The quiescent current rises significantly if the driver is enabled when it is externally terminated. With 1/2 termination load (120Ω between the driver outputs), the quiescent current will jump to at least 13mA as the drivers force a minimum of 1.5V across the termination resistance. With a fully terminated 60Ω line attached, the current will rise to greater than 25mA with the driver enabled, completely overshadowing the extra 40μA drawn by the internal receiver inputs.

Shutdown Mode

Both the receiver output (RO) and the driver outputs (A, B) can be placed in three-state mode by bringing $\overline{RE}$ HIGH and DE LOW respectively. In addition, the LTC1487 will enter shutdown mode when $\overline{RE}$ is HIGH and DE is LOW.

In shutdown the LTC1487 typically draws only 1μA of supply current. In order to guarantee that the part goes into shutdown, $\overline{RE}$ must be HIGH and DE must be LOW for at least 600ns simultaneously. If this time duration is less than 50ns the part will not enter shutdown mode. Toggling either $\overline{RE}$ or DE will wake the LTC1487 back up within 3.5μs.

If the driver is active immediately prior to shutdown, the supply current will not drop to 1μA until the driver outputs have reached a steady state; this can take as long as 2.6μs under worst case conditions. If the driver is disabled prior to shutdown the supply current will drop to 1μA immediately.

Slew Rate and Propagation Delay

Many digital encoding schemes are dependent upon the difference in the propagation delay times of the driver and receiver. Figure 11 shows the test circuit for the LTC1487 propagation delay.

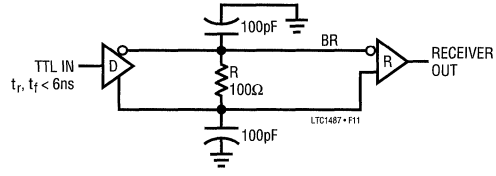


Figure 11. Receiver Propagation Delay Test Circuit

The receiver delay times are:

$|t_{PLH} - t_{PHL}|$ = 13ns Typ, V_{CC} = 5V

The LTC1487 drivers feature controlled slew rate to reduce system EMI and improve signal fidelity by reducing reflections due to misterminated cables.

The driver's skew times are:

Skew = 250ns Typ, V_{CC} = 5V

600ns Max, V_{CC} = 5V, T_A = –40°C to 85°C

SECTION 5—INTERFACE

V.35

Single Supply V.35 Transceiver

FEATURES

- **Single Chip Provides All V.35 Differential Clock and Data Signals**
- **Operates From Single 5V Supply**
- Shutdown Mode Reduces I_{CC} to 1μA Typ
- **Software Selectable DTE or DCE Configuration**
- **Transmitters and Receivers Will Withstand Repeated ±10kV ESD Pulses**
- 10MBaud Transmission Rate
- Transmitter Maintains High Impedance When Disabled, Shut Down, or with Power Off
- Meets CCITT V.35 Specification
- Transmitters are Short-Circuit Protected

APPLICATIONS

- Modems
- Telecommunications
- Data Routers

DESCRIPTION

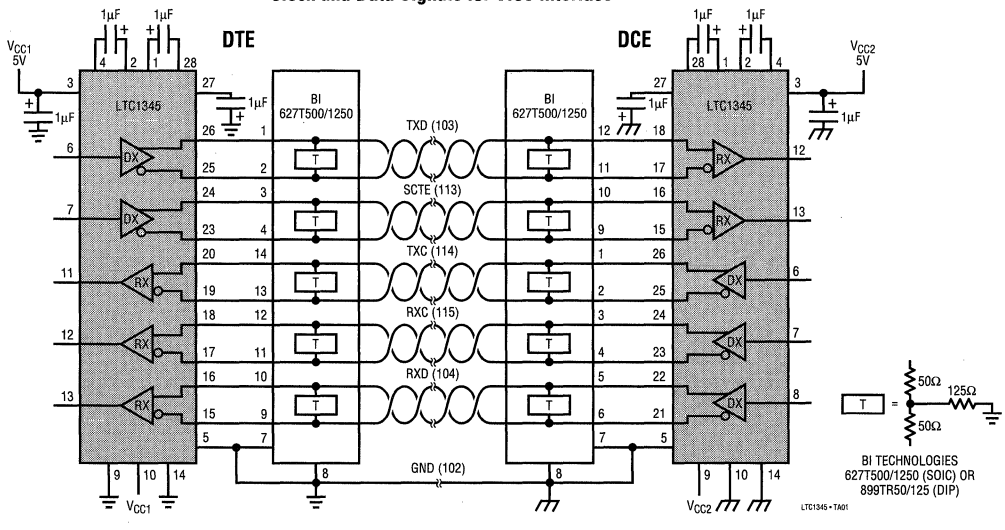
The LTC®1345 is a single chip transceiver that provides the differential clock and data signals for a V.35 interface from a single 5V supply. Combined with an external resistor termination network and an LT®1134A RS232 transceiver for the control signals, the LTC1345 forms a complete low power DTE or DCE V.35 interface port operating from a single 5V supply.

The LTC1345 features three current output differential transmitters, three differential receivers, and a charge pump. The transceiver can be configured for DTE or DCE operation or shut down using two Select pins. In the Shutdown mode, the supply current is reduced to 1μA.

The transceiver operates up to 10Mbaud. All transmitters feature short-circuit protection and a Receiver Output Enable pin allows the receiver outputs to be forced into a high impedance state. Both transmitter outputs and receiver inputs feature ±10kV ESD protection. The charge pump features a regulated V_{EE} output using three external 1μF capacitors.

TYPICAL APPLICATION

Clock and Data Signals for V.35 Interface

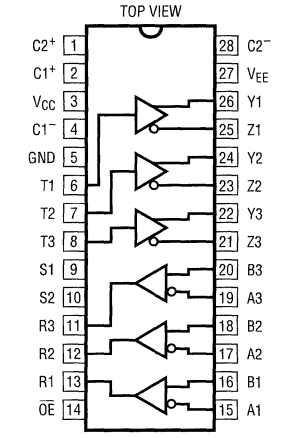


ıBSOLUTE MAXIMUM RATINGS

ıote 1)

ıpply Voltage, V_{CC} 6V
put Voltage
Transmitters ..... −0.3V to (V_{CC} + 0.3V)
Receivers ..... −18V to 18V
S1, S2, $\overline{OE}$ ..... −0.3V to (V_{CC} + 0.3V)
ıtput Voltage
Transmitters ..... −18V to 18V
Receivers ..... −0.3V to (V_{CC} + 0.3V)
V_{EE} ..... −10V to 0.3V
ıort-Circuit Duration
Transmitter Output ..... Indefinite
Receiver Output ..... Indefinite
V_{EE} ..... 30 sec
ɔerating Temperature Range
Commercial ..... 0°C to 70°C
Industrial ..... −40°C to 85°C
:orage Temperature Range ..... −65°C to 150°C
ːad Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



NW PACKAGE
28-LEAD PDIP WIDE

SW PACKAGE
28-LEAD PLASTIC SO WIDE

THREE V.35 TRANSMITTERS AND THREE RECEIVERS

T_{JMAX} = 125°C, θ_{JA} = 56°C/W (NW)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (SW)

ORDER PART NUMBER
LTC1345CNW
LTC1345CSW
LTC1345INW
LTC1345ISW

Consult factory for Military grade parts.

5

ɔC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5% (Notes 2, 3), unless otherwise specified.

MBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
D	Transmitter Differential Output Voltage	Figure 1, −4V ≤ V_{OS} ≤ 4V	●	0.44	0.55	0.66	V
C	Transmitter Common-Mode Output Voltage	Figure 1, V_{OS} = 0V	●	−0.6	0	0.6	V
I	Transmitter Output High Current	$V_{Y, Z}$ = 0V	●	−12.6	−11	−9.4	mA
	Transmitter Output Low Current	$V_{Y, Z}$ = 0V	●	9.4	11	12.6	mA
	Transmitter Output Leakage Current	S1 = S2 = 0V, −5V ≤ $V_{Y, Z}$ ≤ 5V	●		±1	±100	µA
	Transmitter Output Impedance	−2V ≤ $V_{Y, Z}$ ≤ 2V			100		kΩ
H	Differential Receiver Input Threshold Voltage	−7V ≤ (V_A + V_B)/2 ≤ 7V	●		25	200	mV
TH	Receiver Input Hysterisis	−7V ≤ (V_A + V_B)/2 ≤ 7V			50		mV
	Receiver Input Current (A, B)	−7V ≤ $V_{A, B}$ ≤ 7V	●			0.4	mA
I	Receiver Input Impedance	−7V ≤ $V_{A, B}$ ≤ 7V	●	17.5	30		kΩ
H	Receiver Output High Voltage	I_O = 4mA, $V_{B, A}$ = 0.2V	●	3	4.5		V
L	Receiver Output Low Voltage	I_O = 4mA, $V_{B, A}$ = −0.2V	●		0.2	0.4	V
R	Receiver Output Short-Circuit Current	0V ≤ V_O ≤ V_{CC}	●	7		85	mA
R	Receiver Three-State Output Current	S1 = S2 = 0V, 0V ≤ V_O ≤ V_{CC}	●			±10	µA
I	Logic Input High Voltage	T, S1, S2, $\overline{OE}$	●	2			V
	Logic Input Low Voltage	T, S1, S2, $\overline{OE}$	●			0.8	V
	Logic Input Current	T, S1, S2, $\overline{OE}$	●			±10	µA
	V_{CC} Supply Current	Figure 1, V_{OS} = 0, S1 = S2 = HIGH No Load, S1 = S2 = HIGH Shutdown, S1 = S2 = 0V	● ● ●		118 19 1	170 30 100	mA mA µA
:	V_{EE} Voltage	No Load, S1 = S2 = HIGH			−5.5		V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5% (Notes 2, 3), unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
t_R, t_F	Transmitter Rise or Fall Time	Figures 1 and 3, V_{OS} = 0V	●		7	40	n
t_{PLH}	Transmitter Input to Output ↗	Figures 1 and 3, V_{OS} = 0V	●		25	70	n
t_{PHL}	Transmitter Input to Output ↘	Figures 1 and 3, V_{OS} = 0V	●		25	70	n
t_{SKEW}	Transmitter Output to Output	Figures 1 and 3, V_{OS} = 0V			0		n
t_{PLH}	Receiver Input to Output ↗	Figures 1 and 4, V_{OS} = 0V	●		49	100	n
t_{PHL}	Receiver Input to Output ↘	Figures 1 and 4, V_{OS} = 0V	●		52	100	n
t_{SKEW}	Differential Receiver Skew, $t_{PLH} - t_{PHL}$	Figures 1 and 4, V_{OS} = 0V			3		n
t_{ZL}	Receiver Enable to Output LOW	Figures 2 and 5, C_L = 15pF, S1 Closed	●		40	70	n
t_{ZH}	Receiver Enable to Output HIGH	Figures 2 and 5, C_L = 15pF, S2 Closed	●		35	70	n
t_{LZ}	Receiver Disable From LOW	Figures 2 and 5, C_L = 15pF, S1 Closed	●		30	70	n
t_{HZ}	Receiver Disable From HIGH	Figures 2 and 5, C_L = 15pF, S2 Closed	●		35	70	n
f_{OSC}	Charge Pump Oscillator Frequency				200		kH
BR_{MAX}	Maximum Data Rate (Note 4)		●	10	15		Mbau

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

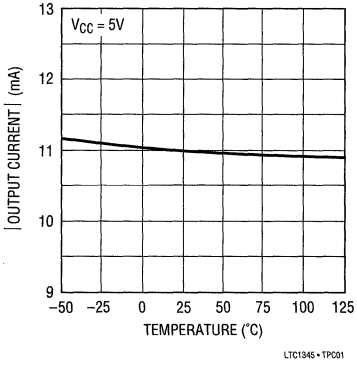
Note 2: All currents into device pins are termed positive; all currents out of device pins are termed negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: All typicals are given for V_{CC} = 5V, C1 = C2 = C3 = 1µF ceramic capacitors and T_A = 25°C.

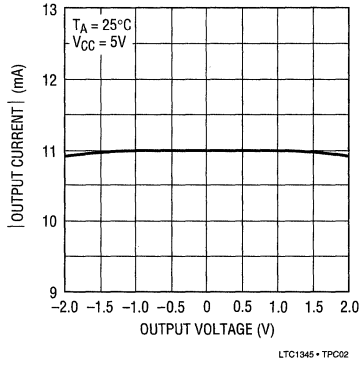
Note 4: Maximum data rate is specified for NRZ data encoding scheme. The maximum data rate may be different for other data encoding schemes Data rate is guaranteed by correlation and is not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

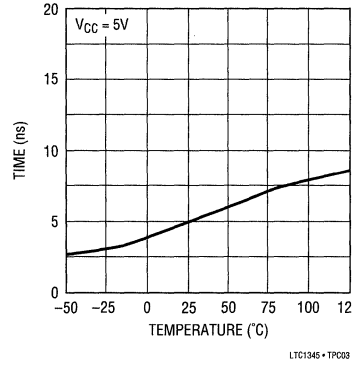
Transmitter Output Current vs Temperature



Transmitter Output Current vs Output Voltage

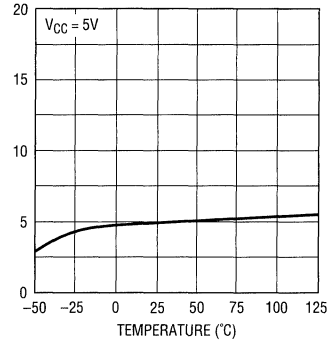


Transmitter Output Skew vs Temperature



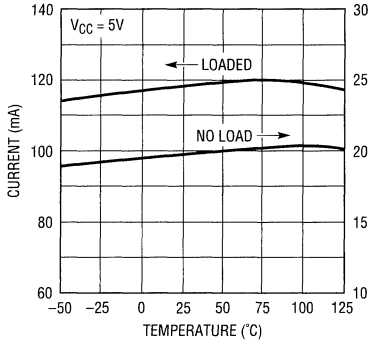
TYPICAL PERFORMANCE CHARACTERISTICS

Receiver $|t_{PLH} - t_{PHL}|$ vs Temperature



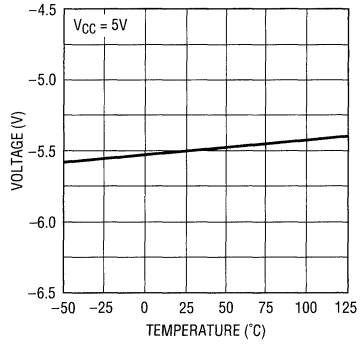
LTC1345 • TPC04

Supply Current vs Temperature



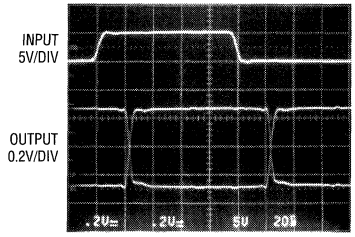
LTC1345 • TPC05

V_{EE} Voltage vs Temperature



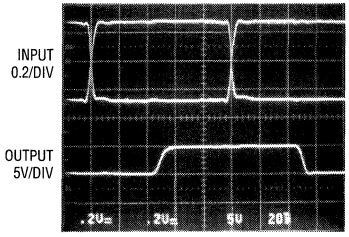
LTC1345 • TPC06

Transmitter Output Waveforms



LTC1345 • TPC07

Receiver Output Waveforms



LTC1345 • TPC08

5

PIN FUNCTIONS

$C2^+$ (Pin 1): Capacitor C2 Positive Terminal.

$C1^+$ (Pin 2): Capacitor C1 Positive Terminal.

V_{CC} (Pin 3): Positive Supply, $4.75 \leq V_{CC} \leq 5.25V$.

$C1^-$ (Pin 4): Capacitor C1 Negative Terminal.

GND (Pin 5): Ground. The positive terminal of C3 is connected to ground.

T1 (Pin 6): Transmitter 1 Input.

T2 (Pin 7): Transmitter 2 Input.

T3 (Pin 8): Transmitter 3 Input.

S1 (Pin 9): Select Input 1.

S2 (Pin 10): Select Input 2.

R3 (Pin 11): Receiver 3 Output.

R2 (Pin 12): Receiver 2 Output.

R1 (Pin 13): Receiver 1 Output.

$\overline{OE}$ (Pin 14): Receiver Output Enable.

A1 (Pin 15): Receiver 1 Inverting Input.

B1 (Pin 16): Receiver 1 Noninverting Input.

A2 (Pin 17): Receiver 2 Inverting Input.

B2 (Pin 18): Receiver 2 Noninverting Input.

A3 (Pin 19): Receiver 3 Inverting Input.

B3 (Pin 20): Receiver 3 Noninverting Input.

Z3 (Pin 21): Transmitter 3 Inverting Output.

PIN FUNCTIONS

Y3 (Pin 22): Transmitter 3 Noninverting Output.

Z2 (Pin 23): Transmitter 2 Inverting Output.

Y2 (Pin 24): Transmitter 2 Noninverting Output

Z1 (Pin 25): Transmitter 1 Inverting Output.

Y1 (Pin 26): Transmitter 1 Noninverting Output.

V_{EE} (Pin 27): Charge Pump Output. Connected to negative terminal of capacitor C3.

$C2^-$ (Pin 28): Capacitor C2 Negative Terminal.

FUNCTION TABLES

Transmitter and Receiver Configuration

S1	S2	TX#	RX#	REMARKS
0	0	—	—	Shutdown
1	0	1, 2, 3	1, 2	DCE Mode, RX3 Shut Down
0	1	1, 2	1, 2, 3	DTE Mode, TX3 Shut Down
1	1	1, 2, 3	1, 2, 3	All Active

Transmitter

	INPUTS			OUTPUTS			
CONFIGURATION	S1	S2	T	Y1 AND Y2	Z1 AND Z2	Y3	Z3
DTE	0	1	0	0	1	Z	Z
DTE	0	1	1	1	0	Z	Z
DCE or All ON	1	X	0	0	1	0	1
DCE or All ON	1	X	1	1	0	1	0
Shutdown	0	0	X	Z	Z	Z	Z

Receiver

	INPUTS				OUTPUTS	
CONFIGURATION	S1	S2	$\overline{OE}$	B – A	R1 AND R2	R3
DTE or All ON	X	1	0	≥0.2V	1	1
DTE or All ON	X	1	0	≤–0.2V	0	0
DCE	1	0	0	≥0.2V	1	Z
DCE	1	0	0	≤–0.2V	0	Z
Disabled	X	X	1	X	Z	Z
Shutdown	0	0	X	X	Z	Z

TEST CIRCUITS

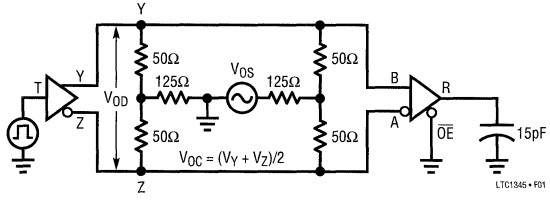


Figure 1. V.35 Transmitter/Receiver Test Circuit

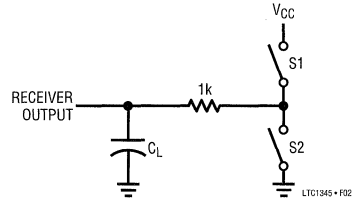


Figure 2. Receiver Output Enable/Disable Timing Test Load

WITCHING TIME WAVEFORMS

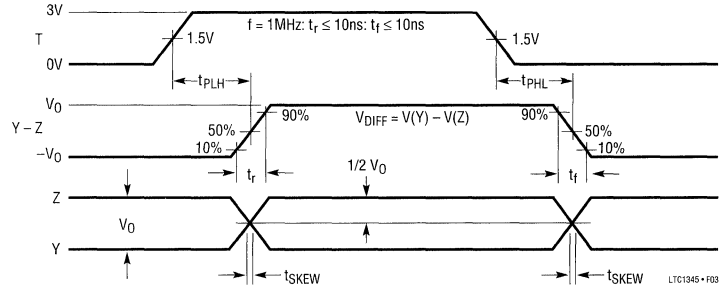


Figure 3. V.35 Transmitter Propagation Delays

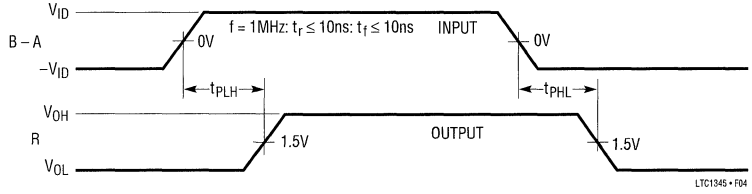


Figure 4. V.35 Receiver Propagation Delays

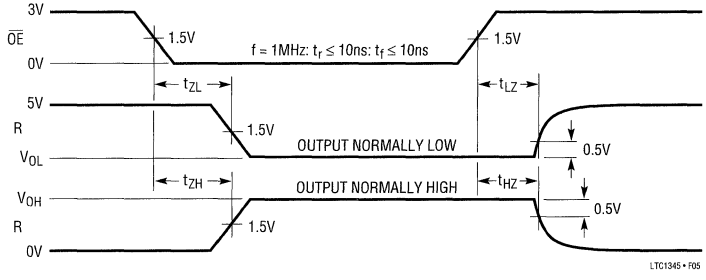


Figure 5. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

Review of CCITT Recommendation V.35 Electrical Specifications

V.35 is a CCITT recommendation for synchronous data transmission via modems. Appendix 2 of the recommendation describes the electrical specifications which are summarized below:

1. The interface cable is balanced twisted-pair with 80Ω to 120Ω impedance.

2. The transmitter's source impedance is between 50Ω and 150Ω.

3. The transmitter's resistance between shorted terminals and ground is 150Ω ±15Ω.

4. When terminated by a 100Ω resistive load, the terminal-to-terminal voltage should be 0.55V ±20%.

5. The transmitter's rise time should be less than 1% of the signal pulse or 40ns, whichever is greater.

6. The common-mode voltage at the transmitter output should not exceed 0.6V.

7. The receiver impedance is 100Ω ±10Ω.

8. The receiver impedance to ground is 150Ω ±15Ω.

9. The transmitter or receiver should not be damaged by connection to earth ground, short-circuiting, or cross connection to other lines.

10. No data errors should occur with ±2V common-mode change at either the transmitter or receiver, or ±4V ground potential difference between transmitter and receiver.

Cable Termination

Each end of the cable connected to an LTC1345 must be terminated by either one of two electrically equivalent external Y or Δ resistor networks for proper operation. The Y-termination has two series connected 50Ω resistors and a 125Ω resistor connected between ground and the center tap of the two 50Ω resistors as shown in Figure 6A.

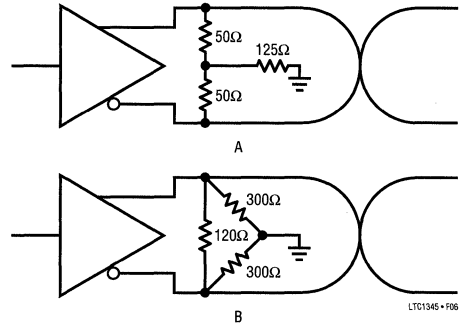


Figure 6. Y and Δ Termination Networks

The alternative Δ-termination has a 120Ω resistor across the twisted wires and two 300Ω resistors between each wire and ground as shown in Figure 6B. Standard 1/8W 5% surface mount resistors can be used for the termination network. To maintain the proper differential output swing the resistor tolerance must be 5% or less. A termination network that combines all the resistors into an SO-14 package is available from:

BI Technologies (Formerly Beckman Industrial)
Resistor Networks
4200 Bonita Place
Fullerton, CA 92635
Phone: (714) 447-2357
FAX: (714) 447-2500
Part #: BI Technologies 627T500/1250 (SOIC)
899TR50/125 (DIP)

APPLICATIONS INFORMATION

Theory of Operation

The transmitter output consists of complementary switched-current sources as shown in Figure 7.

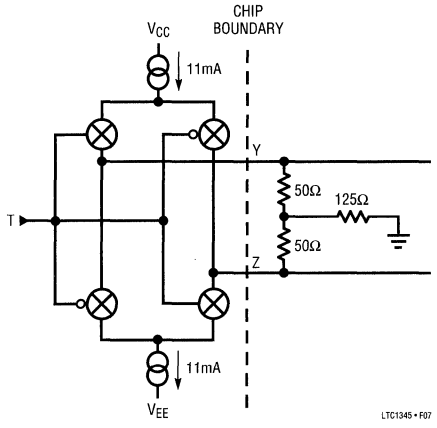


Figure 7. Simplified Transmitter Schematic

With a logic zero at the transmitter input, the inverting output Z sources 11mA and the noninverting output Y sinks 11mA. The differential transmitter output voltage is then set by the termination resistors. With two differential 50Ω resistors at each end of the cable, the voltage is set to (50Ω × 11mA) = 0.55V. With a logic 1 at the transmitter input, output Z sinks 11mA and Y sources 11mA. The common-mode voltage of Y and Z is 0V when both current sources are matched and there is no ground potential difference between the cable terminations. The transmitter current sources have a common-mode range of ±2V, which allows for a ground difference between cable terminations of ±4V.

Each receiver input has a 30k resistance to ground and requires external termination to meet the V.35 input impedance specification. The receivers have an input hysteresis of 50mV to improve noise immunity. The receiver output may be forced into a high impedance state by pulling the output enable ($\overline{OE}$) pin high. For normal operation $\overline{OE}$ should be pulled low.

A charge pump generates the regulated negative supply voltage (V_{EE}) with three 1µF capacitors. Commutating capacitors C1 and C2 form a voltage doubler and inverter while C3 acts as a reservoir capacitor. To insure proper operation, the capacitors must have an ESR less than 1Ω. Monolithic ceramic or solid tantalum capacitors are good choices. Under light loads, regulation at about –5.2V is provided by a pulse-skipping scheme. Under heavy loads the charge pump is on continuously. A small ripple of about 500mV will be present on V_{EE}.

Two Select pins, S1 and S2, configure the chip for DTE, DCE, all transmitters and receivers on, or Shutdown. In Shutdown mode, I_{CC} drops to 1µA. The outputs of the transmitters and receivers are in high impedance states, the charge pump stops and V_{EE} is clamped to ground.

ESD Protection

LTC1345 transmitter outputs and receiver inputs have on-chip protection from multiple ±10kV ESD transients. ESD testing is done using the Human Body ESD Model. ESD testing must be done with an AC ground on the V_{CC} and V_{EE} supply pins. The low ESR supply decoupling and V_{EE} reservoir capacitors provide this AC ground during normal operation.

Complete V.35 Port

Figure 8 shows the schematic of a complete surface mounted, single 5V DTE and DCE V.35 port using only three ICs and eight capacitors per port. The LTC1345 is used to transmit the clock and data signals, and the LT1134A to transmit the control signals. If test signals 140, 141, and 142 are not used, the transmitter inputs should be tied to V_{CC}.

5

APPLICATIONS INFORMATION

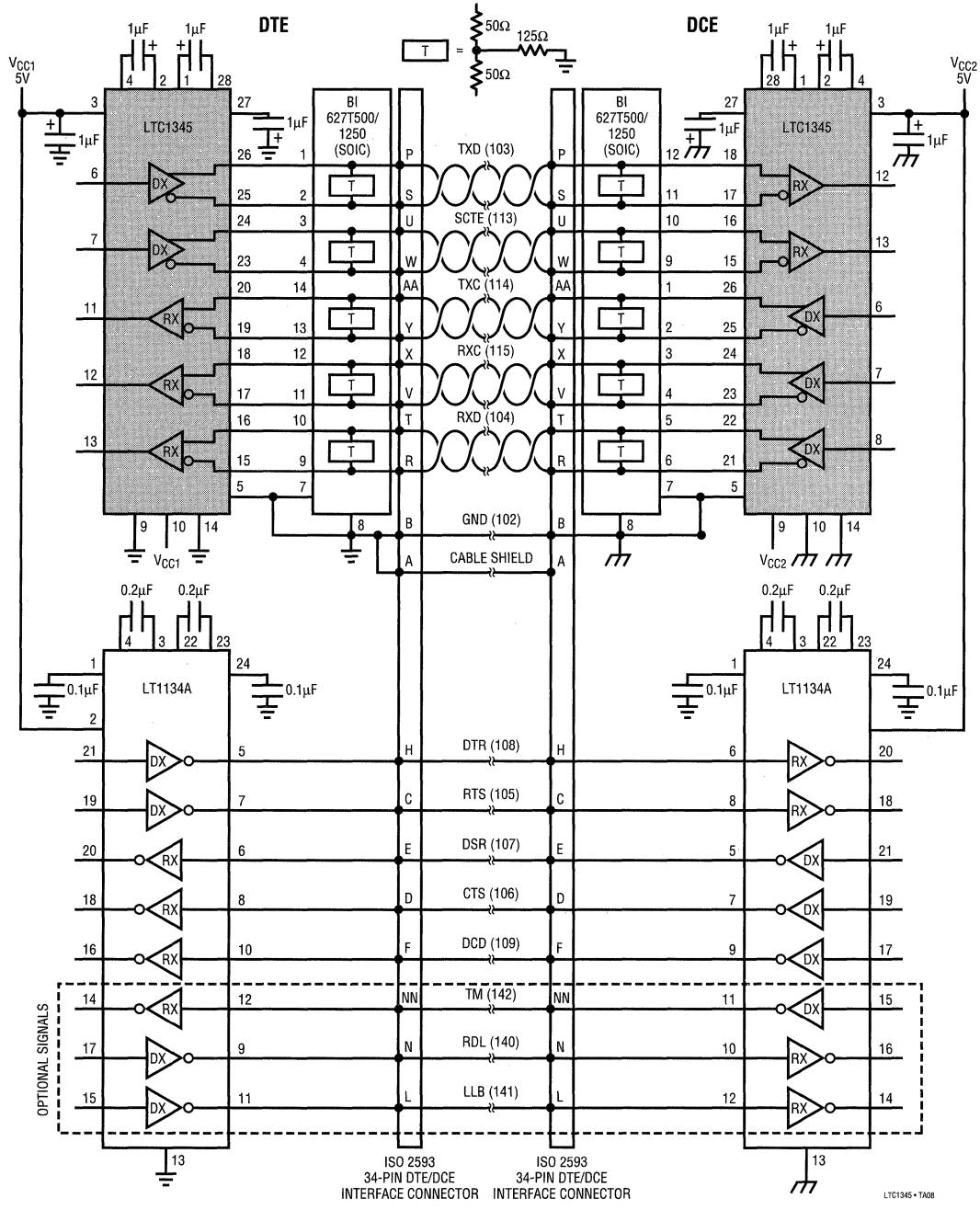


Figure 8. Complete Single 5V V.35 Interface

APPLICATIONS INFORMATION

RS422/RS485 Applications

The receivers on the LTC1345 are ideal for RS422 and RS485 applications. Using the test circuit in Figure 9, the LTC1345 receivers are able to successfully reconstruct the data stream with the common-mode voltage meeting RS422 and RS485 requirements (12V to –7V).

Figures 10 and 11 show that the LTC1345 receivers are very capable of reconstructing data at rates up to 10Mbaud.

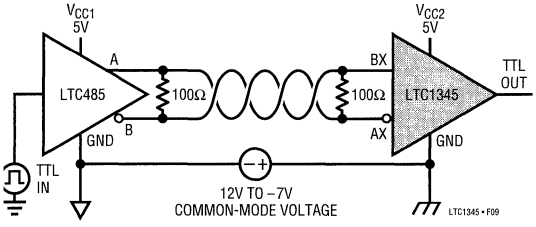


Figure 9 RS422/RS485 Receiver Interface

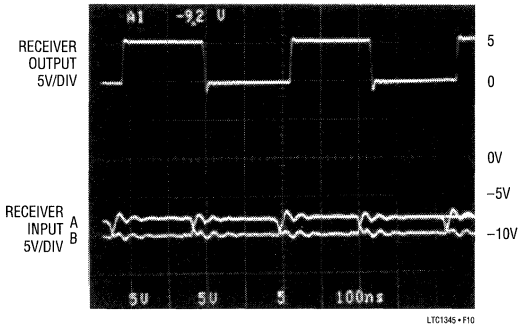


Figure 10. –7V Common Mode

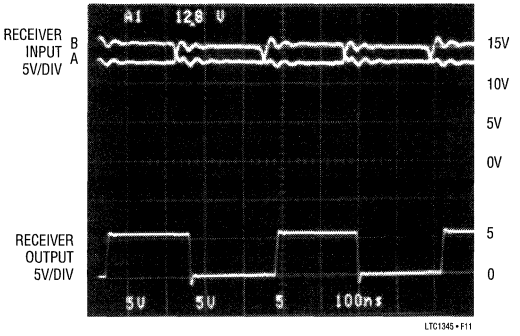


Figure 11. 12V Common Mode

5

SECTION 5—INTERFACE

Single 5V RS232/RS422/AppleTalk® DCE Transceiver

FEATURES

- **Single Chip Provides DCE RS232 or RS422/AppleTalk DCE Port**
- **Operates from a Single 5V Supply**
- Charge Pump Uses 0.1µF Capacitors
- Output Common-Mode Voltage Range Exceeds Power Supply Rails for All Drivers
- Driver Outputs Are High Impedance with Power Off
- Pin Selectable RS232/RS422 Receiver
- Thermal Shutdown Protection
- Drivers Are Short-Circuit Protected

APPLICATIONS

- Dual-Mode RS232/RS422 Peripherals
- AppleTalk Peripherals
- Single 5V Systems

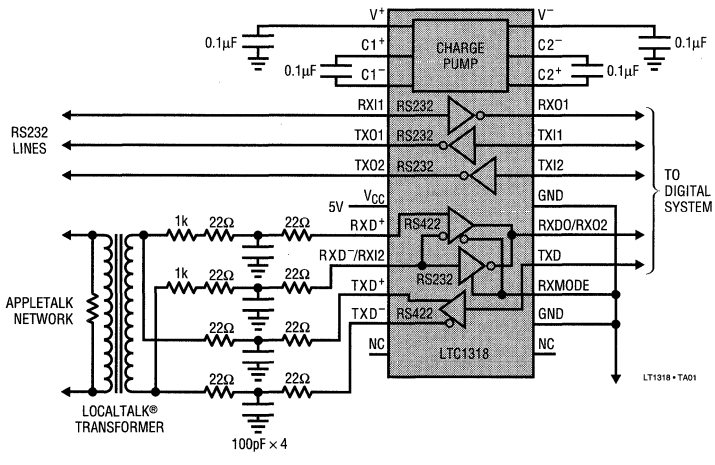
DESCRIPTION

The LTC®1318 is a single 5V, RS232/RS422 transceiver for connection to the DCE, or peripheral side of an interface link. It includes an on-board charge pump to generate a ±8V supply which allows true RS232 output swings. The charge pump requires only four external 0.1µF capacitors. The LTC1318 includes two RS232 drivers, a differential RS422 driver, a dedicated RS232 receiver, and a pin selectable RS232/RS422 receiver which can receive either single-ended or differential signals.

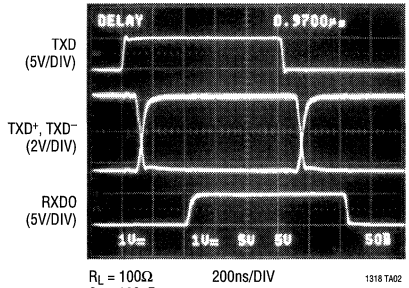
The LTC1318 features driver outputs which can be taken to common-mode voltages outside the power supply rails without damage. Additionally, the driver outputs assume a high impedance state when the power is shut off, preventing externally applied signals from feeding back into the power supplies. The RS232 devices will operate at speeds up to 100kbaud. The RS422 devices will operate up to 2Mbaud.

The LTC1318 is available in a 24-lead SO Wide package.

TYPICAL APPLICATION



Driver Output Waveforms



ABSOLUTE MAXIMUM RATINGS

Note 1)

Supply Voltage:
- V_{CC} 7V
- V^+ 13.2V
- V^- ..... −13.2V

Input Voltage:
- All Drivers ..... −0.3 to (V_{CC} + 0.3V)
- All Receivers ..... −25V to 25V
- RXMODE Pin ..... −0.3V to (V_{CC} + 0.3V)

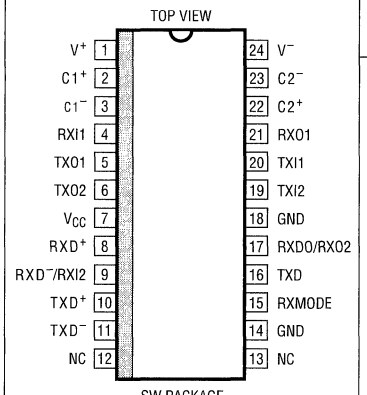
Output Voltage:
- RS232 Drivers ..... (V^+ − 30V) to (V^- + 30V)
- RS422 Drivers ..... ±15V
- All Receivers ..... −0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration:
- V^+ or V^- to GND ..... 30 sec
- Driver or Receiver Outputs ..... Indefinite

Operating Temperature Range ..... 0°C to 70°C

Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC1318CSW

Consult factory for Industrial and Military grade parts

ELECTRICAL CHARACTERISTICS

V_S = 5V ±5%, C1 = C2 = 0.1µF, T_A = 0°C to 70°C, unless otherwise specified. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{CC}	Supply Current	No Load	●		9	30	mA
V^+	Positive Charge Pump Output Voltage	I_{OUT} = 0mA I_{OUT} = 10mA, V_{CC} = 5V	● ●	7.8 6.8	8.8 7.4		V V
V^-	Negative Charge Pump Output Voltage	I_{OUT} = 0mA I_{OUT} = − 5mA, V_{CC} = 5V	● ●	−7.3 −6.3	−8.6 −7.3		V V
Differential Driver							
V_{OD}	Differential Driver Output Voltage	No Load (Figure 1) R_L = 100Ω (Figure 1)	● ●	±4 ±2			V V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	R_L = 100Ω (Figure 1)	●			0.2	V
V_{OC}	Common-Mode Output Voltage	R_L = 100Ω (Figure 1)	●			3	V
I_{OSS}	Short-Circuit Output Current	−1V < V_{CMR} < 7V	●	35		200	mA
V_{IL}	Input Low Voltage		●			0.8	V
V_{IH}	Input High Voltage		●	2.0			V
Single-Ended Driver							
V_O	Output Voltage Swing	R_L = 3k	●	±5	7.3/−6.5		V
I_{OSS}	Short-Circuit Output Current	V_{OUT} = 0V	●	±5	17		mA
V_{IL}	Input Low Voltage		●			0.8	V
V_{IH}	Input High Voltage		●	2			V
SR	Output Slew Rate	R_L = 3k, C_L = 51pF	●	4	20	30	V/µS

ELECTRICAL CHARACTERISTICS

V_S = 5V ±5%, C1 = C2 = 0.1µF, T_A = 0°C to 70°C, unless otherwise specified. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Receiver							
V_{TH}	Differential Receiver Threshold		●	–0.2		0.2	V
CMR	Common-Mode Input Range		●	–7		7	V
	Hysteresis	V_{CM} = OV	●		30		mV
R_{IN}	Input Resistance	TA = 25°C		3	5	7	kΩ
V_{OL}	Output Low Voltage	I_{OUT} = –1.6mA				0.4	V
V_{OH}	Output High Voltage	I_{OUT} = 160µA, V_{CC} = 5V	●	3.5			V
I_{OSS}	Short-Circuit Output Current	V_O = GND or V_{CC}	●	±7		±85	mA
Single-Ended Receiver							
V_L	Input Voltage Low Threshold		●	0.8	1.4		V
V_{IH}	Input Voltage High Threshold		●		1.8	2.4	V
	Hysteresis		●	0.1	0.4	1.0	V
R_{IN}	Input Resistance	TA = 25°C		3	5	7	kΩ
V_{OL}	Output Low Voltage	I_{OUT} = –4mA	●		0.2	0.4	V
V_{OH}	Output High Voltage	I_{OUT} = 4mA, V_{CC} = 5V	●	3.5	4.8		–V
I_{OSS}	Short-Circuit Output Current	V_O = GND or V_{CC}	●	±7		±85	mA
V_{ILRXM}	RXMODE Input Low Voltage		●	0.8	1.6		V
V_{IHRXM}	RXMODE Input High Voltage		●		1.6	2.0	V
I_{INRXM}	RXMODE Input Current	V_{IN} = OV or V_{CC}	●			±2	µA
Switching Characteristics							
$t_{PLH,HL}$	Differential Driver Propagation Delay	R_L = 100Ω, C_L = 100pF (Figures 2,3)	●		35	100	ns
t_{SKEW}	Differential Driver Output to Output	R_L = 100Ω, C_L = 100pF (Figures 2,3)	●		5	35	ns
$t_{R,F}$	Differential Driver Rise, Fall Time	R_L = 100Ω, C_L = 100pF (Figures 2,3)	●		15	50	ns
$t_{PLH,HL}$	Differential Receiver Propagation Delay	C_L = 15pF, (Figures 4)	●		110	200	ns
t_{SEL}	Receiver Mode Switching Time		●		25	100	ns

The ● denotes specifications which apply over the full operating temperature range.

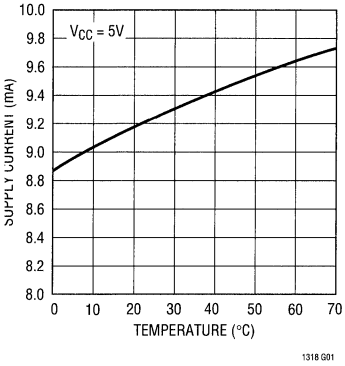
Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All currents into device pins are negative, all currents out of device pins are positive. All voltages are referenced to ground unless otherwise specified.

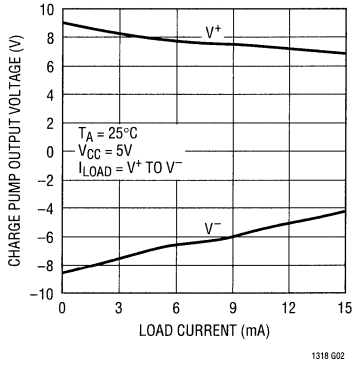
Note 3: All typicals are given at V_{CC} = 5V, T_A = 25°C.

TYPICAL PERFORMANCE CHARACTERISTICS

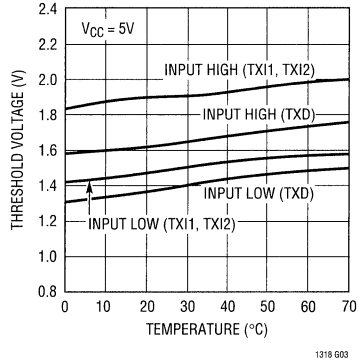
Supply Current vs Temperature



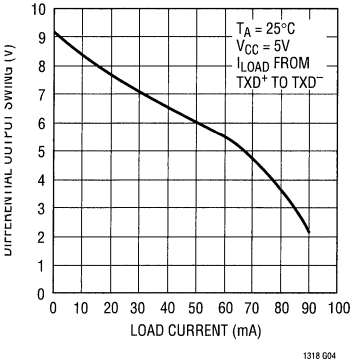
Charge Pump Output Voltage vs Load Current



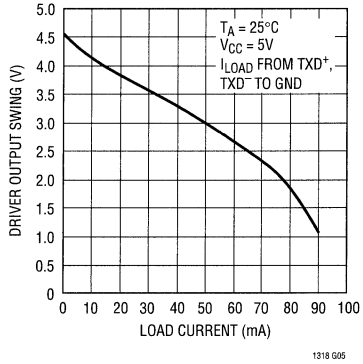
TTL Input Threshold vs Temperature



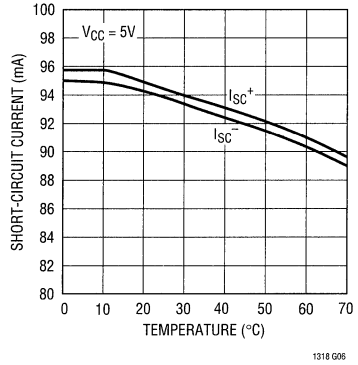
RS422 Driver Differential Output Swing vs Load Current



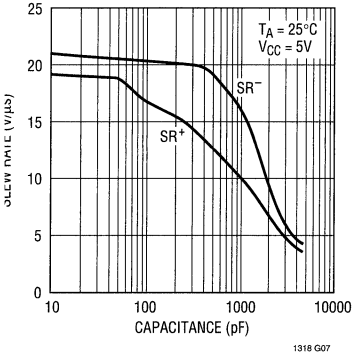
RS422 Driver Single-Ended Output Swing vs Load Current



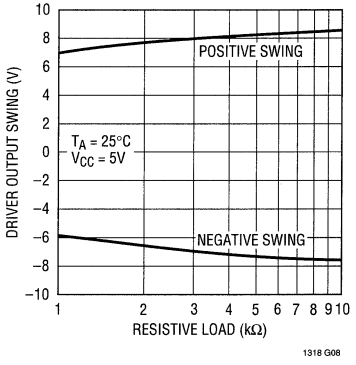
RS422 Driver Short-Circuit Current vs Temperature



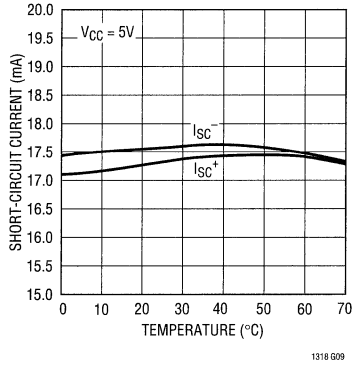
RS232 Driver Slew Rate vs Load Capacitance



RS232 Driver Output Swing vs Resistive Load



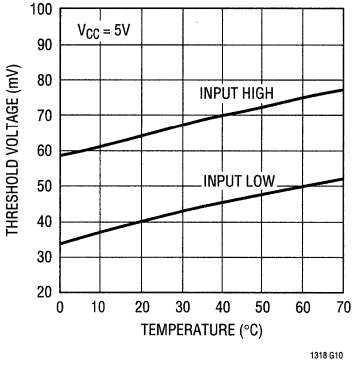
RS232 Driver Short-Circuit Current vs Temperature



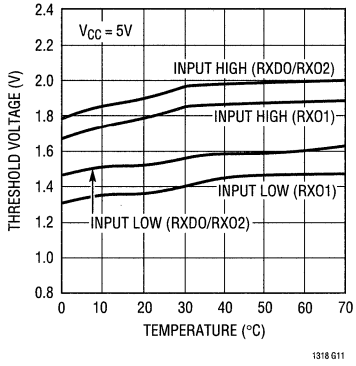
5

TYPICAL PERFORMANCE CHARACTERISTICS

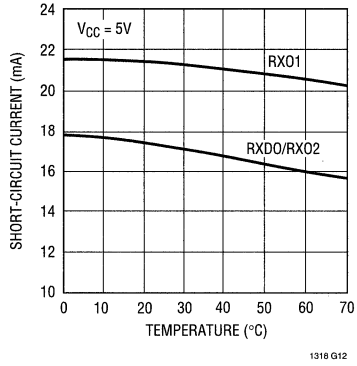
RS422 Receiver Differential Threshold vs Temperature



RS232 Receiver Input Threshold vs Temperature



TTL Output Short-Circuit Current vs Temperature



PIN FUNCTIONS

V^+ (Pin 1): Charge Pump Positive Output. This pin requires a 0.1µF capacitor to ground. Under normal operation this pin maintains a voltage of about 8.8V above ground. An external load can be connected between this pin and ground or V^-.

$C1^+$, $C1^-$ (Pins 2, 3): C1 Inputs. Connect a 0.1µF capacitor between $C1^+$ and $C1^-$.

RXI1 (Pin 4): First RS232 Single-Ended Receiver Input. This is an inverting receiver.

TXO1, TXO2 (Pins 5,6): RS232 Single-Ended Driver Outputs.

V_{CC} (Pin 7): Positive Supply Input. Apply $4.75V \leq V_{CC} \leq 5.25V$ to this pin. A 0.1µF bypass capacitor is required.

RXD^+ (Pin 8): When RXMODE (pin 15) is low, this pin acts as the differential RS422 receiver positive input. When RXMODE is high, this pin is disabled.

RXD^-/RXI2 (Pin 9): When RXMODE (pin 15) is low, this pin acts as the differential RS422 receiver negative input. When RXMODE is high, this pin acts as the second RS232 receiver input. The receiver is inverting in RS232 mode.

TXD^+ (Pin 10): Differential RS422 Driver Noninverting Output.

TXD^- (Pin 11): Differential RS422 Driver Inverting Output.

NC (Pins 12,13): No Internal Connection.

GND (Pins 14, 18): Power Supply Ground. Connect both pins to each other and to the ground.

RXMODE (Pin 15): This pin controls the state of the differential/single-ended receiver. When RXMODE is low, the receiver is in differential mode and will receive RS422 compatible signals at RXD^+ and RXD^-/RXI2 (pins 8 and 9). When RXMODE goes high, the receiver enters single-ended mode and will receive RS232 compatible signals at RXD^-/RXI2. RXD^+ is disabled in single-ended mode. Both modes use the RXDO/RXO2 pin (pin 17) as their output.

TXD (Pin 16): Differential RS422 Driver Input (TTL Compatible).

RXDO/RXO2 (Pin 17): This is the output of the configurable differential/single-ended receiver.

TXI1, TXI2 (Pins 20, 19): RS232 Driver Inputs (TTL Compatible). Both are inverting inputs.

RXO1 (Pin 21): First RS232 Receiver Outputs (TTL compatible).

PIN FUNCTIONS

C2+, C2– (Pins 22, 23): C2 inputs. Connect a 0.1µF capacitor between C2+ and C2–.

V– (Pin 24): Charge Pump Negative Output. This pin requires a 0.1µF capacitor to ground. Under normal operation, this pin maintains a voltage of about 8.6V below ground. An external load can be connected between this pin and ground or V+.

TEST CIRCUITS

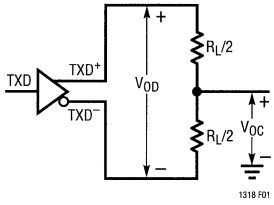


Figure 1.

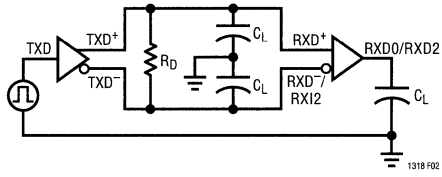


Figure 2.

SWITCHING WAVEFORMS

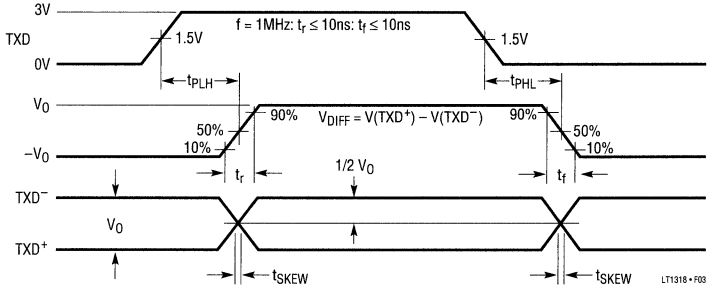


Figure 3. Differential Driver

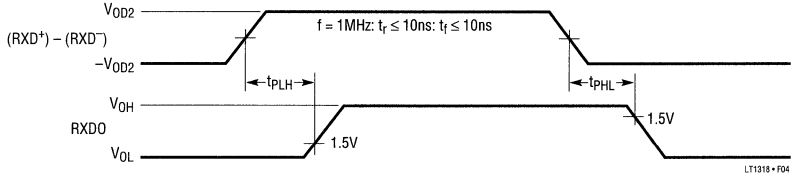


Figure 4. Differential Receiver

APPLICATION INFORMATION

Interface Standards

The LTC1318 provides compatibility with both RS232 and RS422/AppleTalk/LocalTalk standards in a single chip, enabling a system to communicate using either protocol as necessary. The LTC1318 provides two RS232 single-ended drivers, one RS422 differential driver, and two receivers. One of the receivers is a dedicated RS232 single-ended receiver, while the other can be configured for RS232 (single-ended) or RS422 (differential) operation by controlling the logic state of the select pin. All single-ended drivers and receivers meet the RS232C specification for output swing, load driving capacity and input range, and can additionally transmit and receive signals as high as 100kbaud. The differential driver and receiver can interface to both RS422 and AppleTalk networks, and can transmit and receive signals at rates exceeding 2Mbaud.

Fault Protection

The LTC1318 incorporates many protection features to make it as "bustproof" as possible. All driver outputs and receiver inputs are protected against ESD strikes to ±6kV, eliminating the need for external protection devices in most applications. All driver outputs can be taken outside the power supply rails without damage and will not allow current to be forced back into the supplies, preventing the output fault from affecting other logic circuits using the same power supply. Additionally, the driver outputs enter a high impedance state when the power is removed, preventing the system from loading the data lines when it is shut off. All driver and receiver outputs are protected against short circuits to ground or to the supply rails.

Charge Pump Power Supply

The LTC1318 includes an on-board charge pump to generate the voltages necessary for true RS232 compatible output swing. This charge pump requires just four external 0.1µF capacitors to operate; two flying caps connected to the $C1^+/C1^-$ and $C2^+/C2^-$ pins, and two hold caps, one from V^+ to ground and one from V^- to ground. The charge pump has enough extra capacity to drive light external loads and still meet RS232 specifications; it will support a 10mA load from V^+ to ground or a 5mA from V^+ to V^- (Figure 5).

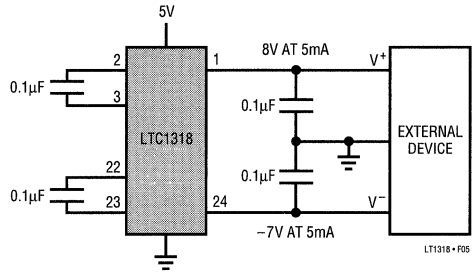


Figure 5.

Configurable RS422/RS232 Receiver

There are two line receivers in the LTC1318. One is a dedicated RS232 receiver; the other can receive both single-ended RS232 signals and differential RS422 signals. This second receiver has two inputs: RXD^+ (pin 8) and RXD^- (pin 9) to accept differential signals. The RXD^+ input is disabled in single-ended mode. The receiver mode is set by the RXMODE (pin 15). A low level on RXMODE configures the receiver in differential mode; it accepts input at RXD^+ and RXD^- and outputs the data at RXDO (pin 17). A high level at RXMODE forces the receiver into single-ended mode; RXD^+ is disabled, pin 9 switches identity from RXD^- to RXI2, and pin 17 switches from RXDO to RXO2, the single-ended data output. In this mode the receiver accepts RS232 signals at RXI2 and outputs the data through RXO2. The receiver becomes inverting in single-ended mode. This receiver can switch between its two modes within 100ns, allowing the system to sense the input signal and configure itself accordingly.

Single 5V AppleTalk® Transceiver

FEATURES

- **Single Chip Provides Complete LocalTalk®/AppleTalk Port**
- **Operates From a Single 5V Supply**
- ESD Protection to ±10kV on Receiver Inputs and Driver Outputs
- **Low Power: I_{CC} = 2.4mA Typ**
- Shutdown Pin Reduces I_{CC} to 0.5µA Typ
- Receiver Keep-Alive Function: I_{CC} = 65µA Typ
- **Differential Driver Drives Either Differential AppleTalk or Single-Ended EIA562 Loads**
- Drivers Maintain High Impedance in Three-State or with Power Off
- Thermal Shutdown Protection
- Drivers are Short-Circuit Protected

APPLICATIONS

- LocalTalk Peripherals
- Notebook/Palmtop Computers
- Battery-Powered Systems

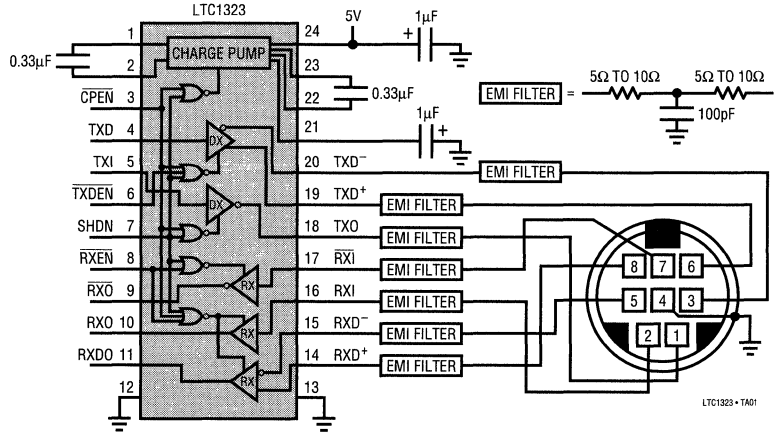
DESCRIPTION

The LTC®1323 is a multi-protocol line transceiver designed to operate on AppleTalk or EIA562-compatible single-ended networks while operating from a single 5V supply. There are two versions of the LTC1323 available: a 16-pin version designed to connect to an AppleTalk network, and a 24-pin version which also includes the additional single-ended drivers and receivers necessary to create an Apple-compatible serial port. An on-board charge pump generates a –5V supply which can be used to power external devices. Additionally, the 24-pin LTC1323 features a micropower keep-alive mode during which one of the single-ended receivers is kept active to monitor external wake-up signals. The LTC1323 draws only 2.4mA quiescent current when active, 65µA in receiver keep-alive mode, and 0.5µA in shutdown, making it ideal for use in battery-powered systems.

The differential driver can drive either differential AppleTalk loads or conventional single-ended loads. The driver outputs three-state when disabled, during shutdown, in receiver keep-alive mode, or when the power is off. The driver outputs will maintain high impedance even with output common-mode voltages beyond the power supply rails. Both the driver outputs and receiver inputs are protected against ESD damage to ±10kV.

5

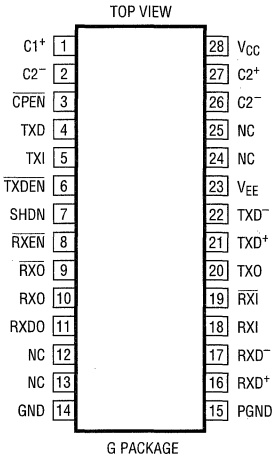
TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) 7V
Input Voltage
  Logic Inputs ..... −0.3V to V_{CC} + 0.3V
  Receiver Inputs ..... ±15V
Driver Output Voltage (Forced) ..... ±15V
Driver Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

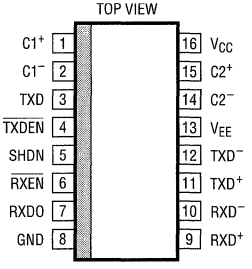


G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 96°C/W

ORDER PART NUMBER

LTC1323CG

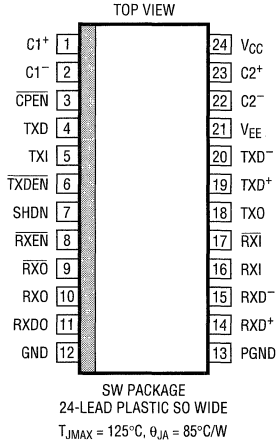


S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1323CS



SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 125°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1323CSW

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±10%, T_A = 0°C to 70°C (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{CC}	Normal Operation Supply Current	No Load, SHDN = 0V, $\overline{CPEN}$ = 0V, $\overline{TXDEN}$ = 0V, $\overline{RXEN}$ = 0V	●		2.4	4	mA
	Receiver Keep-Alive Supply Current	No Load, SHDN = 0V, $\overline{CPEN}$ = V_{CC}, $\overline{TXDEN}$ = 0V, $\overline{RXEN}$ = 0V	●		65	100	µA
	Shutdown Supply Current	No Load, SHDN = V_{CC}, $\overline{CPEN}$ = X, $\overline{TXDEN}$ = X, $\overline{RXEN}$ = 0V	●		0.5	10	µA
V_{EE}	Negative Supply Output Voltage	$I_{LOAD} \leq$ 10mA (Note 4), V_{CC} = 5V, R_L = 100Ω (Figure 1), TXI = V_{CC}, R_{TXO} = 3k (Figure 5)	●	–5.5	–5	–4.5	V
f_{OSC}	Charge Pump Oscillator Frequency				200		kHz
Differential Driver							
V_{OD}	Differential Output Voltage	No Load R_L = 100Ω (Figure 1)	● ●	±8 ±2			V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	R_L = 100Ω (Figure 1)			0.2		V
Differential Driver							
V_{OC}	Differential Common-Mode Output Voltage	R_L = 100Ω			3		V
V_{OS}	Single-Ended Output Voltage	No Load R_L = 3k to GND	● ●	±4.0 ±3.7			V V
V_{CMR}	Common-Mode Range	SHDN = V_{CC} or $\overline{CPEN}$ = V_{CC} or Power Off	●			±10	V
I_{SS}	Short-Circuit Current	$-5V \leq V_O \leq 5V$	●	35	120	500	mA
I_{OZ}	Three-State Output Current	SHDN = V_{CC} or $\overline{CPEN}$ = V_{CC} or Power Off, $-10V \leq V_O \leq 10V$	●		±2	±200	µA
Single-Ended Driver (Note 5)							
V_{OS}	Single-Ended Output Voltage	No Load R_L = 3k to GND	● ●	±4.5 ±3.7			V V
V_{CMR}	Common-Mode Range	SHDN = V_{CC} or $\overline{CPEN}$ = V_{CC} or $\overline{TXDEN}$ = V_{CC} or Power Off	●			±10	V
I_{SS}	Short-Circuit Current	$-5V \leq V_O \leq 5V$	●	35	220	500	mA
I_{OZ}	Three-State Output Current	SHDN = V_{CC} or $\overline{CPEN}$ = V_{CC} or $\overline{TXDEN}$ = V_{CC} or Power Off, $-10V \leq V_O \leq 10V$	●		±2	±200	µA
Receivers							
R_{IN}	Input Resistance	$-7V \leq V_{IN} \leq 7V$	●	12			kΩ
	Differential Receiver Threshold Voltage	$-7V \leq V_{CM} \leq 7V$	●	–200		200	mV
	Differential Receiver Input Hysteresis	$-7V \leq V_{CM} \leq 7V$	●		70		mV
	Single-Ended Input, Low Voltage	(Note 5)	●			0.8	V
	Single-Ended Input, High Voltage	(Note 5)	●	2			V
V_{OH}	Output High Voltage	I_O = –4mA	●	3.5			V
V_{OL}	Output Low Voltage	I_O = 4mA	●			0.4	V
I_{SS}	Output Short-Circuit Current	$-5V \leq V_O \leq 5V$	●	7		85	mA
I_{OZ}	Output Three-State Current	$-5V \leq V_O \leq 5V$, $\overline{RXEN}$ = V_{CC}	●		±2	±100	µA

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ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±10%, T_A = 0°C to 70°C (Notes 2 and 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Logic Inputs							
V_{IH}	Input High Voltage	All Logic Input Pins	●	2.0			V
V_{IL}	Input Low Voltage	All Logic Input Pins	●			0.8	V
I_C	Input Current	All Logic Input Pins	●		±1.0	±20	µA
Switching Characteristics							
t_{PLH}, t_{PHL}	Differential Driver Propagation Delay	R_L = 100Ω, C_L = 100pF (Figures 2, 7)	●		40	120	ns
	Differential Driver Propagation Delay with Single-Ended Load	R_L = 3k, C_L = 100pF (Figures 3, 9)	●		120	180	ns
	Single-Ended Driver Propagation Delay	R_L = 3k, C_L = 100pF, (Figures 5, 10) (Note 5)	●		40	120	ns
	Differential Receiver Propagation Delay	C_L = 15pF (Figures 2, 11)	●		70	160	ns
	Single-Ended Receiver Propagation Delay	C_L = 15pF (Figures 6, 12) (Note 5)	●		70	160	ns
	Inverting Receiver Propagation Delay in Keep-Alive Mode, SHDN = 0V, $\overline{CPEN}$ = V_{CC}	C_L = 15pF (Figures 6, 12) (Note 5)	●		150	600	ns
t_{SKEW}	Differential Driver Output to Output	R_L = 100Ω, C_L = 100pF (Figures 2, 7)	●		10	50	ns
t_r, t_f	Differential Driver Rise/Fall Time	R_L = 100Ω, C_L = 100pF (Figures 2, 7)	●		50	150	ns
	Differential Driver Rise/Fall Time with Single-Ended Load	R_L = 3k, C_L = 100pF (Figures 3, 9)	●		50	150	ns
	Single-Ended Driver Rise/Fall Time	R_L = 3k, C_L = 100pF (Figures 5, 10) (Note 5)	●		15	80	ns
t_{HDIS}, t_{LDIS}	Differential Driver Output Active to Disable	C_L = 15pF (Figures 4, 8)	●		180	250	ns
	Any Receiver Output Active to Disable	C_L = 15pF (Figures 4, 13)	●		30	100	ns
t_{ENH}, t_{ENL}	Differential Driver Enable to Output Active	C_L = 15pF (Figures 4, 8)	●		180	250	ns
	Any Receiver, Enable to Output Active	C_L = 15pF (Figures 4, 13)	●		30	100	ns
V_{EER}	Supply Rise Time from Shutdown or Receiver Keep-Alive	C1 = C2 = 0.33µF, C_{VEE} = 1µF	●		0.2		ms

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

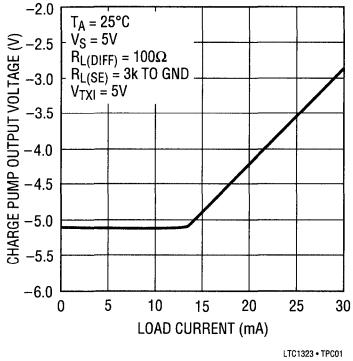
Note 3: All typicals are given at V_{CC} = 5V, T_A = 25°C.

Note 4: I_{LOAD} is an external current being sunk into the V_{EE} pin.

Note 5: These specifications apply to the 24-pin SO Wide package only.

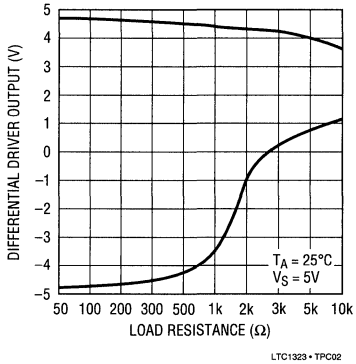
TYPICAL PERFORMANCE CHARACTERISTICS

Charge Pump Output Voltage vs Load Current



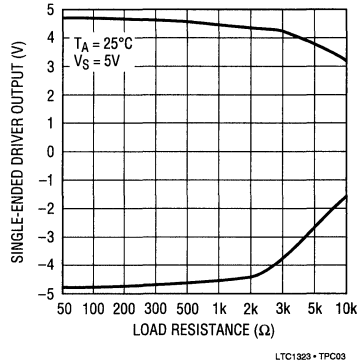
LTC1323 • TPC01

Differential Driver Swing vs Load Resistance



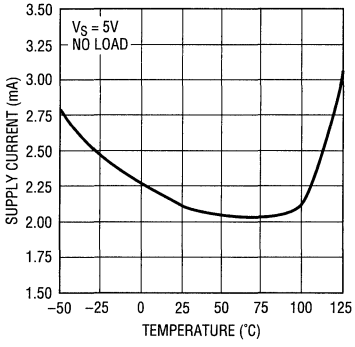
LTC1323 • TPC02

Single-Ended Driver Swing vs Load Resistance



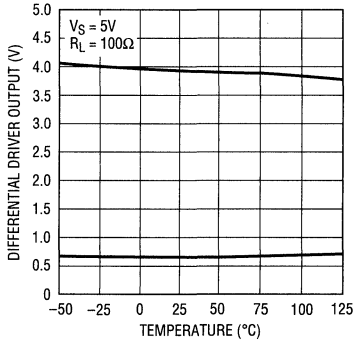
LTC1323 • TPC03

Supply Current vs Temperature



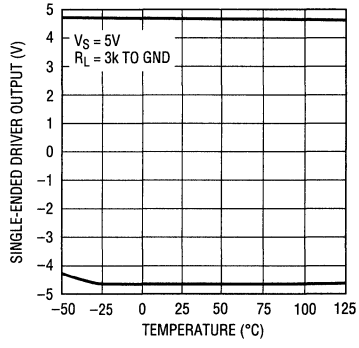
LTC1323 • TPC04

Differential Driver Swing vs Temperature



LTC1323 • TPC05

Single-Ended Driver Swing vs Temperature



LTC1323 • TPC06

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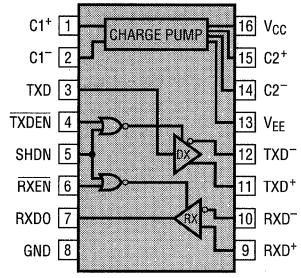
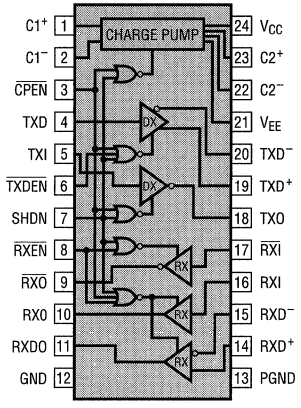
PIN FUNCTIONS

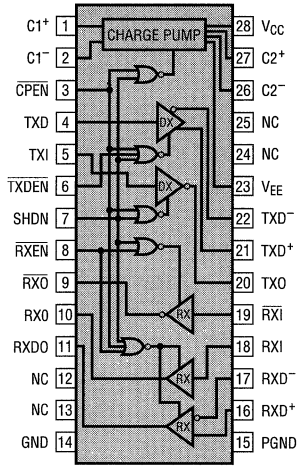
LTC1323CS



LTC1323CSW



LTC1323CG



C1+: C1 Positive Input. Connect a 0.33µF capacitor between C1+ and C1–.

C1–: C1 Negative Input. Connect a 0.33µF capacitor between C1+ and C1–.

$\overline{\text{CPEN}}$: TTL Level Charge Pump Enable Input. With $\overline{\text{CPEN}}$ held low, the charge pump is enabled and the chip operates normally. When $\overline{\text{CPEN}}$ is pulled high, the charge pump is disabled as well as both drivers, the noninverting single-ended receiver, and the differential receiver. The inverting single-ended receiver (RXI) is kept alive to monitor the control line and I_{CC} drops to 65µA. To turn off the receiver and drop I_{CC} to 0.5µA, pull the SHDN pin high.

TXD: Differential Driver Input (TTL compatible).

TXI: Single-Ended Driver Input (TTL compatible).

$\overline{\text{TXDEN}}$: Differential Driver Output Enable (TTL compatible). A high level on this pin forces the differential driver into three-state; a low level enables the driver. This input does not affect the single-ended driver.

SHDN: Shutdown Input (TTL compatible). When this pin is high, the chip is shut down. All driver and receiver outputs are three-state, the charge pump turns off, and the supply current drops to 0.5µA. A low level on this pin allows normal operation.

$\overline{\text{RXEN}}$: Receiver Enable (TTL compatible). A high level on this pin disables the receivers and three-states the logic outputs; a low level allows normal operation.

$\overline{\text{RXO}}$: Inverting Single-Ended Receiver Output. Remains active in the receiver keep-alive mode.

RXO: Noninverting Single-Ended Receiver Output.

RXDO: Differential Receiver Output.

GND: Signal Ground. Connect to PGND with 24-pin package.

PGND: Power ground is connected internally to the charge pump and differential driver. Connect to the GND pin.

RXD+: Differential Receiver Noninverting Input. When this pin is ≥200mV above RXD–, RXDO will be high; when this pin is ≥200mV below RXD–, RXDO will be low.

RXD–: Differential Receiver Inverting Input.

RXI: Noninverting Receiver Input. This input controls the RXO output.

$\overline{\text{RXI}}$: Inverting Receiver Input. This input controls the $\overline{\text{RXO}}$ output. In receiver keep-alive mode ($\overline{\text{CPEN}}$ high, SHDN low), this receiver can be used to monitor a wake-up control signal.

PIN FUNCTIONS

TXO: Single-Ended Driver Output.

TXD⁺: Differential Driver Noninverting Output.

TXD⁻: Differential Driver Inverting Output.

V_{EE}: Negative Supply Charge Pump Output. Requires a 1µF bypass capacitor to ground. If an external load is connected to the V_{EE} pin, the bypass capacitor value should be increased to 4.7µF.

C2⁻: C2 Negative Input. Connect a 0.33µF capacitor between C2⁺ and C2⁻.

C2⁺: C2 Positive Input. Connect a 0.33µF capacitor between C2⁺ and C2⁻.

V_{CC}: Positive Supply Input. $4.5V \le V_{CC} \le 5.5V$. Requires a 1µF bypass capacitor to ground.

TEST CIRCUITS

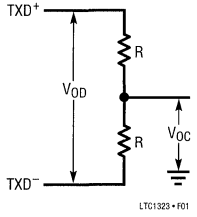


Figure 1

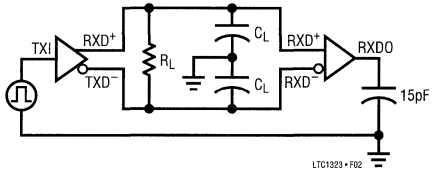


Figure 2

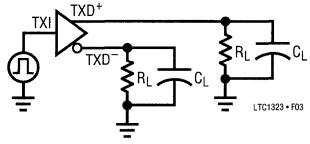


Figure 3

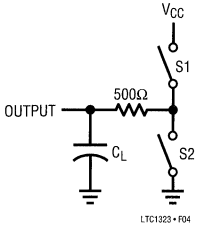


Figure 4

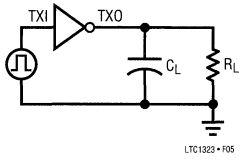


Figure 5

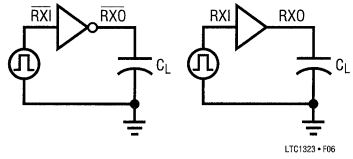


Figure 6

SWITCHING WAVEFORMS

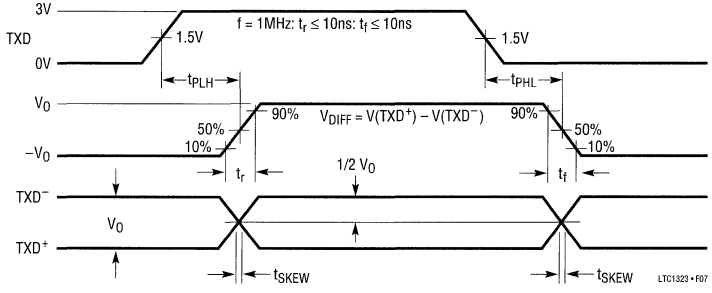


Figure 7. Differential Driver

SWITCHING WAVEFORMS

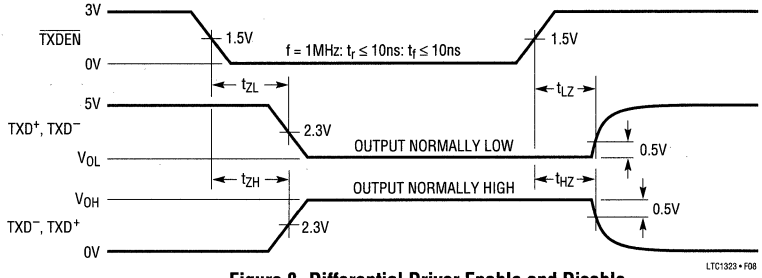


Figure 8. Differential Driver Enable and Disable

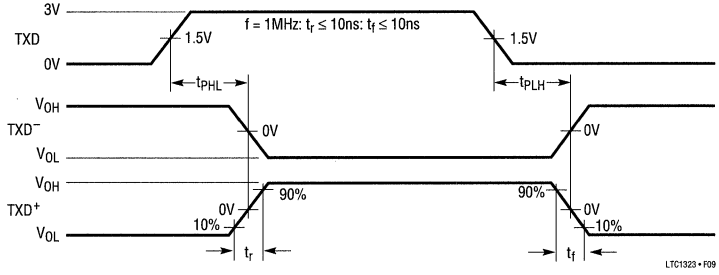


Figure 9. Differential Driver With Single-Ended Load

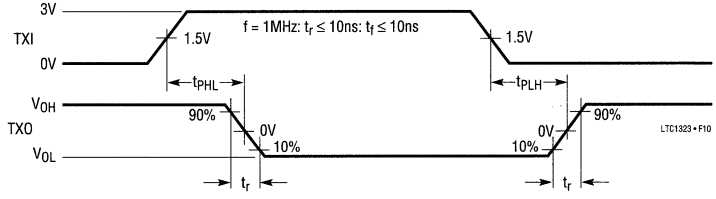


Figure 10. Single-Ended Driver

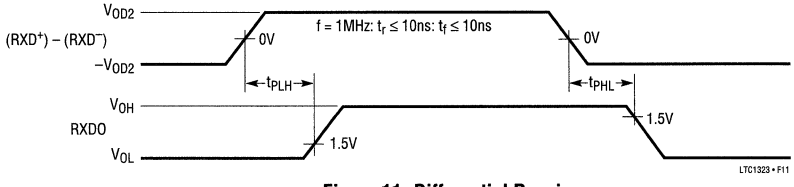


Figure 11. Differential Receiver

SWITCHING WAVEFORMS

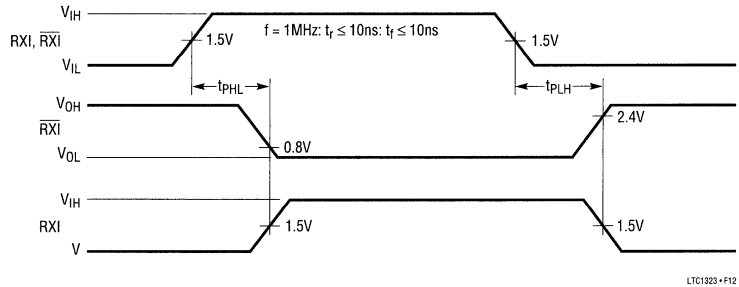


Figure 12. Single-Ended Receiver

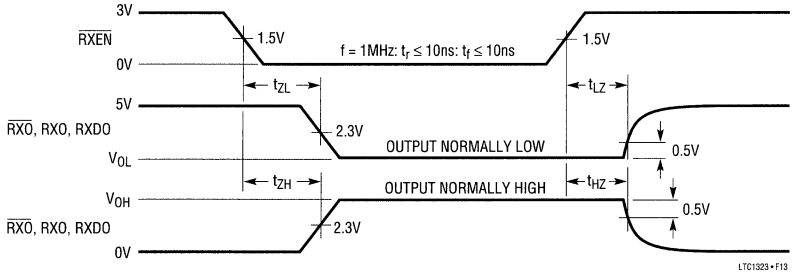


Figure 13. Receiver Enable and Disable

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APPLICATIONS INFORMATION

Functional Description

The "serial port" on the back of an Apple-compatible computer or peripheral is a fairly versatile "multi-protocol" connector. It must be able to connect to a wide bandwidth LAN (an AppleTalk/LocalTalk network), which requires a high speed differential transceiver to meet the AppleTalk specification, and it must also be able to connect directly to a printer or modem through a short RS232 style link. The LTC1323 is designed to provide all the functions necessary to implement such a port on a single chip. Two versions of the LTC1323 are available: a 16-pin SO version which provides the minimum solution for interfacing to an AppleTalk network in a smaller package, and a larger 24-pin SO Wide version which additionally includes all the handshaking lines required to implement a complete AppleTalk/modem/printer serial port. All LTC1323s run from a single 5V power supply while providing true single-ended compatibility, and include a 0.5μA low power shutdown mode to improve lifetime in battery-powered devices. The 24-pin SO Wide version also includes a receiver keep-alive mode for monitoring external signals while drawing 65μA typically.

The LTC1323 includes an RS422-compatible differential driver/receiver pair for data transmission, with the driver specified to drive 2V into the 100Ω primary of a typical LocalTalk interface transformer/RFI interference network. Either output of the differential RS422 driver can also act as an single-ended driver, allowing the LTC1323 to communicate over a standard serial connection. The 24-pin SO Wide LTC1323 also includes an extra single ended only driver and two extra RS232-compatible single-ended receivers for handshaking lines. All versions include an on-board charge pump to provide a regulated –5V supply required for the single-ended drivers. The charge pump can also provide up to 10mA of external load current to power other circuitry.

APPLICATIONS INFORMATION

Driving Differential AppleTalk or Single-Ended Loads

The differential driver is able to drive either an AppleTalk load or a single-ended load such as a printer or modem. With a differential AppleTalk load, TXD^+ and TXD^- will typically swing between 1.2V and 3.5V (Figure 14a). With a single-ended 3k load such as a printer, either TXD^+ or TXD^- will meet the single-ended voltage swing requirement of ±3.7V (Figure 14b). An automatic switching circuit prevents the differential driver from overloading the charge pump if the outputs are shorted to ground while driving single-ended signals. This allows the second single-ended driver to continue to operate normally when the first is shorted, and allows external circuitry attached to the charge pump output to continue to operate even if there are faults at the driver outputs.

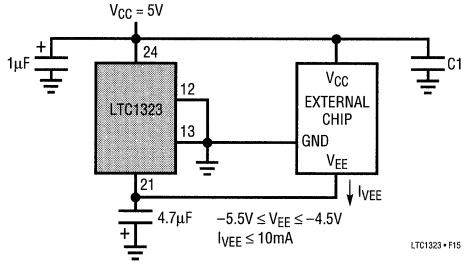


Figure 14

Thermal Shutdown Protection

The LTC1323 includes a thermal shutdown circuit which protects against prolonged shorts at the driver outputs. If a driver output is shorted to another output or to the power supply, the current will be initially limited to a maximum of 500mA. When the die temperature rises above 150°C, the thermal shutdown circuit disables the driver outputs. When the die cools to about 130°C, the outputs are re-enabled. If the short still exists, the part will heat again and the cycle will repeat. This oscillation occurs at about 10Hz and prevents the part from being damaged by excessive power dissipation. When the short is removed, the part will return to normal operation.

Power Shutdown

The power shutdown feature of the LTC1323 is designed for battery-powered systems. When SHDN is forced high the part enters shutdown mode. In shutdown the supply current typically drops from 2.4mA to 0.5µA, the charge pump turns off, and the driver and receiver outputs are three-stated.

Receiver Keep-Alive Mode (24-Pin SO Wide Only)

The 24-pin SO Wide version of the LTC1323 also features a power saving receiver keep-alive mode. When $\overline{CPEN}$ is pulled high the charge pump is turned off and the outputs of both drivers, the noninverting single-ended receiver and the differential receiver are forced into three-state. The inverting single-ended receiver ($\overline{RXI}$) is kept alive with I_{CC} dropping to 65µA and the receiver delay time increasing to a maximum of 400ns. The receiver can then be used to monitor a wake-up control signal.

Charge Pump Capacitors and Supply Bypassing

The LTC1323 requires two external 0.33µF capacitors for the charge pump to operate: one from $C1^+$ to $C1^-$ and one from $C2^+$ to $C2^-$. These capacitors should be low ESR types and should be mounted as close as possible to the LTC1323. Monolithic ceramic capacitors work well in this application. Do not use capacitors greater than 2µF at the charge pump pins or internal peak currents can rise to destructive levels. The LTC1323 also requires that both V_{CC} and V_{EE} be well bypassed to ensure proper charge pump operation and prevent data errors. A 1µF capacitor from V_{CC} to ground is adequate. A 1µF capacitor is required from V_{EE} to ground and should be increased to 4.7µF if an external load is connected to the V_{EE} pin. Ceramic or tantalum capacitors are adequate for power supply bypassing; aluminum electrolytic capacitors should only be used if their ESR is low enough for proper charge pump operation. Inadequate bypass or charge pump capacitors will cause the charge pump output to go out of regulation prematurely, degrading the output swing at the SINGLE-ENDED driver outputs.

APPLICATIONS INFORMATION

Driving an External Load from V_{EE}

An external load may be connected between ground and the V_{EE} pin as shown in Figure 15. The LTC1323 V_{EE} pin will sink up to a maximum of 10mA while maintaining the pin voltage between –4.5V and –5.5V. If an external load is connected, the V_{EE} bypass capacitor should be increased to 4.7µF. Both LTC1323 and the external chip should have separate V_{CC} bypass capacitors but can share the V_{EE} capacitor.

EMI Filter

Most LocalTalk applications use an electromagnetic interference (EMI) filter consisting of a resistor-capacitor T network between each driver and receiver and the connector. Unfortunately, the resistors significantly attenuate the drivers output signals before they reach the cable. Because the LTC1323 uses a single supply differential driver, the resistor values should be reduced to 5Ω to 10Ω to guarantee adequate voltage swing on the cable (Figure 16a). In most applications, removing the resistors completely does not cause an increase in EMI as long as a shielded connector and cable are used (Figure 16b). With the resistors removed the only DC load is the primary resistance of the LocalTalk transformer. This will increase the DC standby current when the driver outputs are active, but does not adversely affect the drivers because they can handle a direct indefinite short circuits without damage. Transformer primary resistance should be above 15Ω to keep the LTC1323 operating normally and prevent it from entering thermal shutdown. For maximum swing and EMI immunity, a ferrite bead and capacitor T network can be used (Figure 16c).

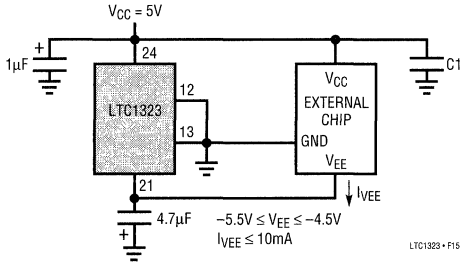


Figure 15

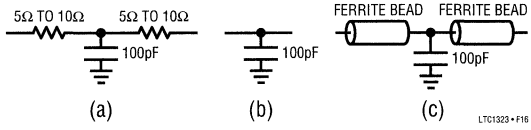
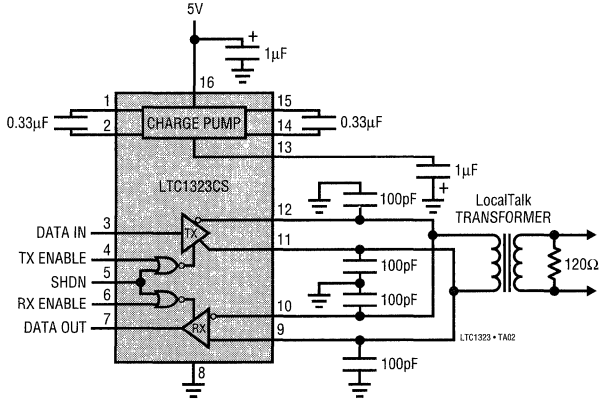


Figure 16. EMI Filters

5

TYPICAL APPLICATION

Typical LocalTalk Connection



SECTION 5—INTERFACE

Multiple Modulation Standard Infrared Receiver

FEATURES

- **Receives Multiple IR Modulation Methods**
- **Low Noise, High Speed Preamp: 2pA/√Hz, 7MHz**
- **Low Frequency Ambient Rejection Loops**
- **Dual Gain Channels: 8MHz, 400V/V**
- 25ns and 60ns Comparators
- 16-Lead SO Package
- 5V Single Supply Operation
- Supply Current: 14mA
- Shutdown Supply Current: 500µA
- External Comparator Threshold Setting

MODULATION STANDARDS

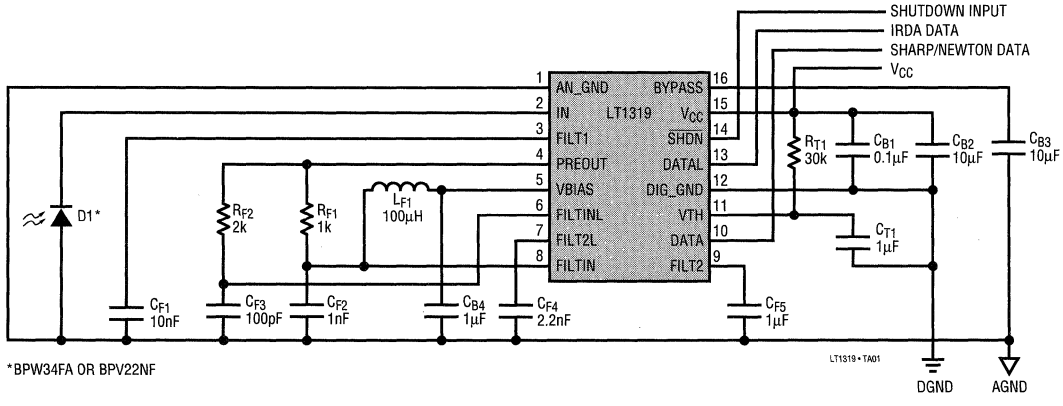
- IRDA: SIR, FIR
- Sharp/Newton
- TV Remote
- High Data Rate Modulation Methods

DESCRIPTION

The LT®1319 is a general purpose building block that contains all the circuitry necessary to transform modulated photodiode signals back to digital signals. The circuit's flexibility permits it to receive multiple modulation methods. A low noise, high frequency preamplifier performs a current-to-voltage conversion while rejecting low frequency ambient interference with an AC coupling loop. Two separate high impedance filter buffer inputs are provided so that off-chip filtering can be tailored for specific modulation schemes. The filter buffers drive separate differential gain stages that end in comparators with internal hysteresis. The comparator thresholds are adjustable externally by the current into pin 11. One channel has a high speed 25ns comparator required for high data rates. The second channel's comparator has a 60ns response time and is well suited to more modest data rates. A power saving shutdown feature is useful in portable applications.

TYPICAL APPLICATION

IRDA and Sharp/Newton Data Receiver

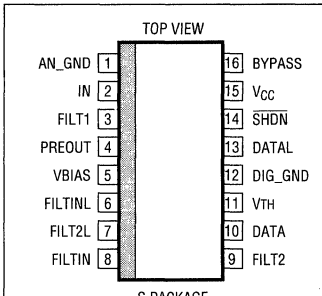


*BPW34FA OR BPV22NF

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_{CC} to GND) 6V
Differential Voltage (Any Two Pins) 6V
Maximum Junction Temperature ..... 150°C
Operating Temperature Range ..... 0°C to 70°C
Specified Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LT1319CS

Consult factory for Industrial or Military grade parts.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{15} = 5V, V_1 = V_{12} = 0V, V_6 = V_8 = V_{14} = 2V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Preamp Input Offset Voltage	V (Pin 2) – V (Pin 5)		4	15	mV
	Preamp Output Offset Voltage	V (Pin 4) – V (Pin 5)		10	25	mV
	Preamp Loop Offset Voltage	V (Pin 3) – V (Pin 5)	50	150	250	mV
	High Gain Loop Offset Voltage	V (Pin 9) – V (Pin 5)	600	800	950	mV
	Low Gain Loop Offset Voltage	V (Pin 7) – V (Pin 5)	600	800	950	mV
A_{VP}	Preamp Transimpedance	±10µA Into Pin 2, Measure ΔV (Pin 4), Fix Pin 3	10	15	17	kΩ
	Preamp Output Swing, Positive	100µA Out of Pin 2, Measure ΔV (Pin 4), Fix Pin 3	0.25	0.4	0.55	V
	Preamp Output Swing, Negative	100µA Into Pin 2, Measure ΔV (Pin 4), Fix Pin 3	−0.55	−0.4	−0.25	V
BW_P	Preamp Bandwidth	C (Pin 3) = 1µF, Measure f_{-3dB}		7		MHz
i_n	Preamp Input Noise Current	C (Pin 3) = 1µF, f = 10kHz		2		pA/√Hz
	Preamp Loop Rejection, Positive	50µA Into Pin 2, Measure ΔV (Pin 4)	−3	−1	3	mV
	Preamp Loop Rejection, Negative	50µA Out of Pin 2, Measure ΔV (Pin 4)	−3	1	3	mV
	Preamp Loop Output Current, Positive	100µA Out of Pin 2, Measure I (Pin 3), (Note 1)	−150	−100	−50	µA
	Preamp Loop Output Current, Negative	100µA Into Pin 2, Measure I (Pin 3), (Note 1)	50	100	150	µA
V_{BIAS}	Bias Voltage	V (Pin 5)	1.7	1.9	2.1	V
V_{BYPASS}	Bypass Voltage	V (Pin 16)	4.75	4.9	4.95	V
I_B	Filter Buffer Input Bias Current	I (Pin 6), I (Pin 8)	0.1	0.5	1.4	µA
R_{IN}	Filter Buffer Input Resistance	ΔV = 0.1V, Measure $ΔI_B$ Pin 6, Pin 8		40		MΩ
	Gain Stage Loop Rejection, Positive	ΔV = 50mV (Pin 6, Pin 8), Measure ΔV (Pin 7, Pin 9)	0.33	0.45	0.57	V
	Gain Stage Loop Rejection, Negative	ΔV = −50mV (Pin 6, Pin 8), Measure ΔV (Pin 7, Pin 9)	−0.57	−0.45	−0.33	V
A_{VG}	Gain Stages Voltage Gain	(Note 2)		400		V/V
BW_G	Gain Stages Bandwidth	C (Pin 7) = C (Pin 9) = 1µF		8		MHz
t_r	Fast Comparator Response Time	10mV Overdrive		25		ns
	Slow Comparator Response Time	10mV Overdrive		60		ns
V_{HYS}	Fast Comparator Hysteresis Voltage	(Note 3)		35		mV
	Slow Comparator Hysteresis Voltage	(Note 3)		40		mV
V_{OH}	Fast Comparator Output High Voltage	ΔV (Pin 9) = −200mV, 1mA Out of Pin 10 (Note 4)	2.4	3.5		V
	Slow Comparator Output High Voltage	ΔV (Pin 7) = −200mV, 0.1mA Out of Pin 13 (Note 4)	2.4	3.9		V
V_{OL}	Fast Comparator Output Low Voltage	ΔV (Pin 9) = 200mV, 800µA Into Pin 10		0.35	0.5	V
	Slow Comparator Output Low Voltage	ΔV (Pin 7) = 200mV, 800µA Into Pin 13		0.39	0.5	V

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ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{15} = 5V, V_1 = V_{12} = 0V, V_6 = V_8 = V_{14} = 2V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Threshold Transimpedance	100µA Into Pin 11 (Note 5)		2		kΩ
V_{TH}	Threshold External Voltage	100µA Into Pin 11, V (Pin 11)	0.8	0.9	1.2	V
V_{IH}	Shutdown Input High Voltage		2			V
V_{IL}	Shutdown Input Low Voltage				0.8	V
I_{IH}	Shutdown Input High Current	V (Pin 14) = 2.4V	–140	–60	–10	µA
I_{IL}	Shutdown Input Low Current	V (Pin 14) = 0.4V	–400	–260	–130	µA
I_S	Supply Current	V (Pin 14) = 2V	10	14	18	mA
I_{SHDN}	Supply Current in Shutdown	V (Pin 14) = 0.8V, V (Pin 6) = V (Pin 8) = 0V	300	500	800	µA

0°C ≤ T_A ≤ 70°C, V_{15} = 5V, V_1 = V_{12} = 0V, V_6 = V_8 = V_{14} = 2V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Preamp Input Offset Voltage	V (Pin 2) – V (Pin 5)		4	17	mV
	Preamp Output Offset Voltage	V (Pin 4) – V (Pin 5)		10	27	mV
	Preamp Loop Offset Voltage	V (Pin 3) – V (Pin 5)	30	150	350	mV
	High Gain Loop Offset Voltage	V (Pin 9) – V (Pin 5)	400	800	1200	mV
	Low Gain Loop Offset Voltage	V (Pin 7) – V (Pin 5)	400	800	1200	mV
A_{VP}	Preamp Transimpedance	±10µA Into Pin 2, Measure ΔV (Pin 4)	8.5	15	18.5	kΩ
	Preamp Output Swing, Positive	100µA Out of Pin 2, Measure ΔV (Pin 4)	0.2	0.4	0.6	V
	Preamp Output Swing, Negative	100µA Into Pin 2, Measure ΔV (Pin 4)	–0.6	–0.4	–0.2	V
	Preamp Loop Rejection, Positive	50µA Into Pin 2, Measure ΔV (Pin 4)	–3.5	–1	3.5	mV
	Preamp Loop Rejection, Negative	50µA Out of Pin 2, Measure ΔV (Pin 4)	–3.5	1	3.5	mV
	Preamp Loop Output Current, Positive	100µA Out of Pin 2, Measure I (Pin 3), (Note 1)	–160	–100	–40	µA
	Preamp Loop Output Current, Negative	100µA Into Pin 2, Measure I (Pin 3), (Note 1)	40	100	160	µA
V_{BIAS}	Bias Voltage	V (Pin 5)	1.5	1.9	2.3	V
V_{BYPASS}	Bypass Voltage	V (Pin 16)	4.7	4.9	4.97	V
I_B	Filter Buffer Input Bias Current	I (Pin 6), I (Pin 8)	0.05	0.5	1.6	µA
	Gain Stage Loop Rejection, Positive	ΔV = 50mV (Pin 6, Pin 8), Measure ΔV (Pin 7, Pin 9)	0.3	0.45	0.6	V
	Gain Stage Loop Rejection, Negative	ΔV = –50mV (Pin 6, Pin 8), Measure ΔV (Pin 7, Pin 9)	–0.6	–0.45	–0.3	V
V_{OH}	Fast Comparator Output High Voltage	ΔV (Pin 9) = –200mV, 1mA Out of Pin 10 (Note 4)	2.4	3.5		V
	Slow Comparator Output High Voltage	ΔV (Pin 7) = –200mV, 0.1mA Out of Pin 13 (Note 4)	2.4	3.9		V
V_{OL}	Fast Comparator Output Low Voltage	ΔV (Pin 9) = 200mV, 800µA Into Pin 10		0.35	0.5	V
	Slow Comparator Output Low Voltage	ΔV (Pin 7) = 200mV, 800µA Into Pin 13		0.39	0.5	V
V_{TH}	Threshold External Voltage	100µA Into Pin 11, V (Pin 11)	0.7	0.9	1.3	V
V_{IH}	Shutdown Input High Voltage		2			V
V_{IL}	Shutdown Input Low Voltage				0.8	V
I_{IH}	Shutdown Input High Current	V (Pin 14) = 2.4V	–160	–60	0	µA
I_{IL}	Shutdown Input Low Current	V (Pin 14) = 0.4V	–450	–260	–80	µA
I_S	Supply Current	V (Pin 14) = 2V	9	14	20	mA
I_{SHDN}	Supply Current in Shutdown	V (Pin 14) = 0.8V, V (Pin 6) = V (Pin 8) = 0V	200	500	900	µA

Note 1: Measure V (Pin 3) without input current for pin 2. Force pin 3 to this measured voltage (which disables the preamp loop). Measure the current into and out of Pin 3 when Pin 2 is driven.

Note 2: The gain is the differential voltage at the comparator inputs divided by the differential voltage between the filter buffer output and VBIAS. This parameter is not tested.

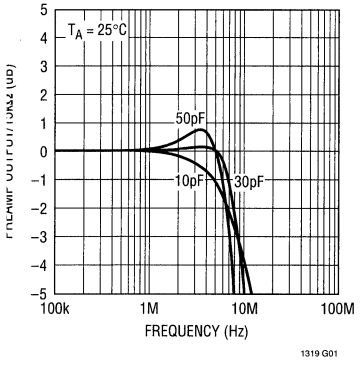
Note 3: Hysteresis is the difference in comparator trip point measured when the output is high and when the output is low. This parameter is not tested.

Note 4: Measure V (Pin 7) and V (Pin 9). Force these voltages to 200mV below their nominal value to switch the comparators high.

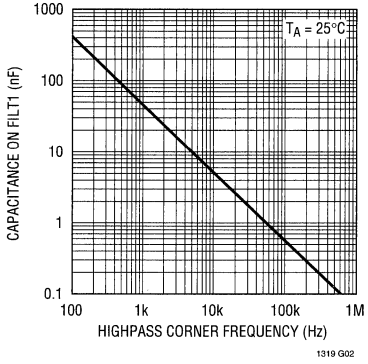
Note 5: The current into Pin 11 is multiplied by 4 and then applied to a 500Ω resistor on the positive comparator inputs. The threshold is I (Pin 11) × 4 × 500Ω.

TYPICAL PERFORMANCE CHARACTERISTICS

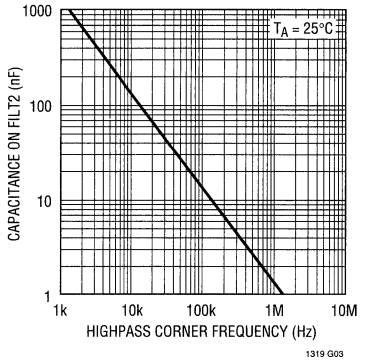
Preamp Frequency Response vs Input Capacitance



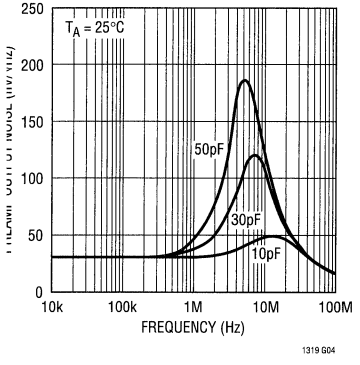
Preamp Highpass vs Capacitance on FILT1



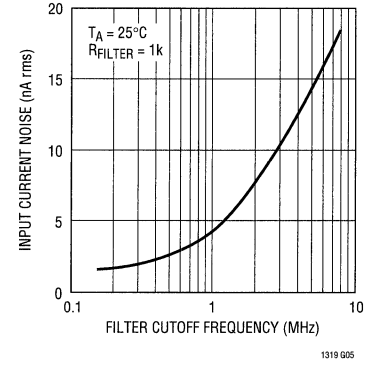
Gain Stage Highpass vs Capacitance on FILT2 or FILT2L



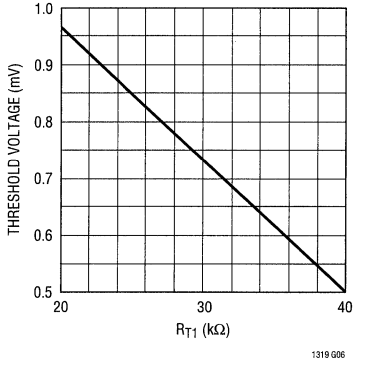
Preamp Output Noise vs Input Capacitance



Input-Referred Noise vs Lowpass Filter on PREOUT



FILTIN- or FILTINL- Referred Threshold Voltage vs R_{T1}

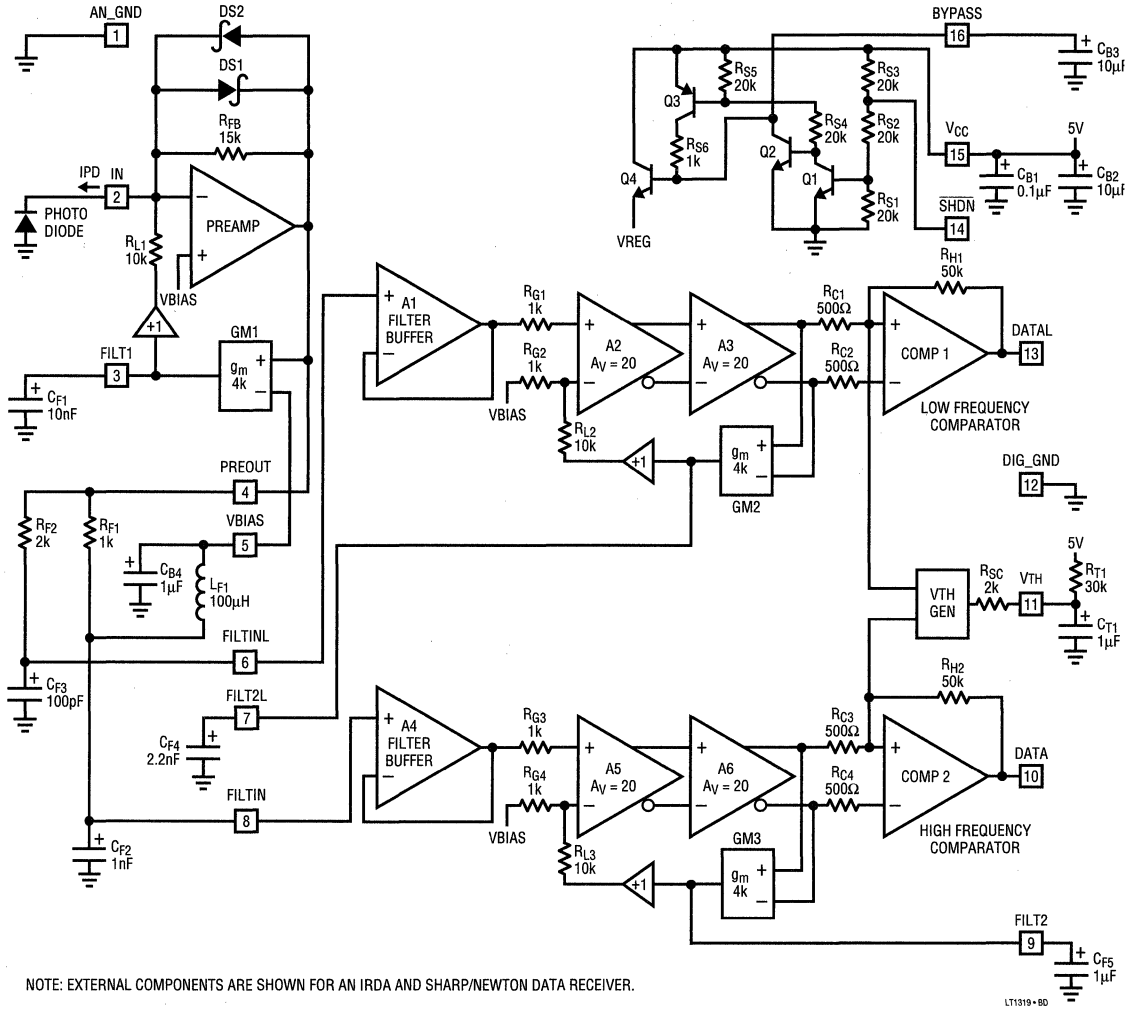


CIRCUIT DESCRIPTION

The LT1319 is a general purpose low noise, high speed, high gain, infrared receiver designed to easily provide IR communications with portable computers, PDAs, desktop computers and peripherals. The receiver takes the photocurrent from an infrared photodiode (Siemens BPW34FA or Temic BPV22NF) and performs a current-to-voltage conversion. After external filtering that is tailored for the desired communication standard, two filter buffers are provided. There are dual gain chains with nominal gain of 100V/V that feed internal comparators with hysteresis. The comparator thresholds are set externally with a current into the VTH pin. The high frequency comparator has a response time of 25ns and is well-suited to high data rates.

The low frequency comparator responds in 60ns and is useful for more modest data rates such as Sharp/Newton and IRDA-SIR. The circuit also contains shutdown circuitry to reduce power consumption. Rejection of ambient interference is accomplished with AC coupling loops around the preamp and the two gain stages. The rejection frequency is set with an internal resistor and an external capacitor to ground. This feature allows changing of the break frequency by simply switching in additional capacitors. To aid in rejection of power supply noise there is internal supply regulation and a fully differential topology after the filter buffers.

BLOCK DIAGRAM



NOTE: EXTERNAL COMPONENTS ARE SHOWN FOR AN IRDA AND SHARP/NEWTON DATA RECEIVER.

APPLICATIONS INFORMATION

Layout and Passive Components

The LT1319 requires careful layout techniques to minimize parasitic signal coupling to the preamp input. A sample board layout for the circuit on the first page is shown in the Typical Application section. The lead lengths on the photodiode must be as short as possible to Pin 2. Shielding is recommended over the entire circuit. A ground plane must be used and connected to Pin 1. The ground plane should extend under the package and surround Pins 1 to 9 and Pin 16. A single point connection should be made to the ground plane at Pin 12 (DIG_GND). The leads on Pins 6 and 8 should be short to prevent pickup into the gain stages. The comparator output leads (Pins 10 and 13) should be as short as possible to minimize coupling back to the input via parasitic capacitance.

Capacitance on Pin 10 should be minimized as the comparator output is pulled up by an internal 5k resistor. The associated digital circuitry should be located on the opposite side of the PC board from the LT1319 or separated as much as possible if on the same side of the board. Filter components should be located on the analog ground side of the package. Bypass capacitors should be used on Pins 5, 11, 15 and 16 for best supply rejection.

Preamp

The LT1319 preamp is a low noise, high speed current-to-voltage converter that has been optimized for an input capacitance of 30pF (which corresponds to the capacitance of the above-mentioned photodiodes with approximately 2V of back bias). A range of 0pF to 50pF is acceptable. The amplifier obtains high bandwidth by providing a low impedance input so that the input current is not filtered by the photodiode capacitance.

The dynamic range of the circuit will be limited at the low end by the input-referred current noise of the preamplifier and the desired signal-to-noise ratio. At the other extreme of the dynamic range for very large input signals, the output of the preamp is clamped by Schottky diodes across the feedback resistor.

The noise bandwidth is shaped by filtering at the output of the preamplifier and by the AC coupling loop. The input capacitance causes noise peaking for high bandwidth applications. Noise peaking can be explained by considering the voltage noise gain. Referring to the Block Diagram, at frequencies beyond the corner frequency of the AC coupling loop, the preamp is in a noise gain of 2.5 due to the ratio of $(R_{FB} + R_{L1})/R_{L1}$. At high frequencies the input capacitance approaches the same impedance as R_{L1} so the noise gain increases. For example, at 500kHz the 30pF input capacitance looks like 10.6kΩ which increases the noise gain to almost 4. The preamp is compensated to provide a flat current-to-voltage frequency response with a –3dB corner at 7MHz. The input current noise peaks up considerably if full bandwidth is used. To obtain best noise performance, the output of the preamp should be filtered to the minimum bandwidth required for the desired modulation scheme. The graph of input-referred noise versus lowpass filtering on the preamp output shows the noise penalty for higher bandwidths.

AC Coupling Loops

There are three AC loops in the circuit that reject low frequency inputs. The first loop is around the preamp and provides rejection of ambient light sources. The operation can be explained by looking at the Block Diagram. For low frequency signals the transconductance amplifier, GM1, compares the preamp output to the VBIAS voltage. This differential voltage is transformed into a current that is fed into the high impedance node at Pin 3 and transformed back to a voltage. There is a voltage gain of approximately 60dB to this point which is then buffered to drive a 10k resistor that is connected back to the input of the preamp. This high gain loop attenuates the effect of low frequency signals by the amount of the loop gain times the ratio of R_{L1} to R_{FB} (i.e., 1000V/V × 10/15 = 667). For higher frequencies the attenuation decreases due to the external capacitor on Pin 3. At frequencies beyond where the loop gain equals 15/10, signals are no longer attenuated. This high frequency cutoff is at:

$$f = (15/10)/(2\pi \times 4k\Omega \times C_{PIN3})$$

where 1/(4kΩ) is the transconductance of the loop amplifier. For example, if C_{PIN3} = 300pF, the highpass frequency is 200kHz which can aid in rejection of a wide range of ambient interference.

The other two loops operate similarly around the gain stages and also provide low frequency rejection. In addi-

APPLICATIONS INFORMATION

tion, the loops around the gain stages provide an accurate DC threshold setting for the comparators. At DC, the loops force the differential voltages at the output of the gain stages to zero. The comparator threshold is set by the currents provided by the V_{TH} generator through the 500Ω resistors R_{C1} and R_{C3}. These currents are equal to 4 times the current into pin 11. For 100μA into pin 11, the comparator thresholds are nominally 200mV.

Power Supply Rejection and Biasing

The LT1319 has very high gain and bandwidth so great care is taken to reduce false output transitions due to power supply noise. As a first step the V_{CC} input is regulated down to approximately 4V to power all the analog sections of the circuit which are also tied to Analog Ground (Pin 1) as is the substrate of the die. Additionally, the internal 4V is bypassed at Pin 16. The digital circuitry (the comparators and shutdown logic) is powered directly off of V_{CC} and is returned to Digital Ground (Pin 12). To provide a clean bias point for the preamp, filter buffers and the gain stages, a 1.9V reference is generated from the 4V rail and is bypassed at Pin 5. The gain stages are pure differential designs which inherently reject supply variations.

Filtering

Filtering is needed for two main reasons: sensitivity and ambient rejection. Lowpass filtering is needed to limit the bandwidth in order to minimize the noise. Low noise permits reliable detection of smaller input signals over a larger distance. Highpass filtering is used to reject interfering ambient signals. Interference includes low frequency sources of infrared light such as sunlight, incandescent lights, and ordinary fluorescent lights, as well as high frequency sources such as TV remote controls (40kHz) and high frequency fluorescent lighting (40kHz to 80kHz).

The circuit topology allows for filtering between the preamplifier and the filter buffers as well as filtering with the three internal highpass loops. With two channels the filtering can be optimized for different modulation schemes. The high speed channel (with a 25ns comparator) is ideal for modulation schemes using frequencies above 1MHz. Carrier-based methods as well as narrow pulse schemes can have superior ambient rejection by adding in a dedicated highpass filter network. The application on the first page of the data sheet is repeated in the Block Diagram and can be used to illustrate the filtering for IRDA-SIR and Sharp/Newton. The preamp highpass zero is set by GM1 and C_{F1}. The break frequency is located at:

$$f = (15k\Omega/10k\Omega)/(2\pi \times 4k\Omega \times 10nF) = 6kHz$$

On the low speed channel there is a lowpass filter at 800kHz set by R_{F2} and C_{F3}. The gain stage has a highpass filter set by GM2 and C_{F4} at approximately 500kHz. The high speed channel has an LC tank circuit at 500kHz with Q = 3 set by R_{F1}. The high speed gain stage has a highpass characteristic set by GM3 and C_{F5} with a break frequency of 1.1kHz. These filters are suitable for the 1.6μs pulses and up to 115kbaud data rates of IRDA-SIR on the slow channel. The fast channel is used for Sharp/Newton ASK Modulation with 500kHz bursts at data rates up to 38.4kbaud.

A second circuit is shown in the Typical Applications section for IRDA SIR/FIR. The first filter is the preamp highpass loop set at 4kHz by C_{F1}. SIR is run on the low speed channel and is next filtered by an 800kHz lowpass formed by R_{F2} and C_{F3} to reduce the noise bandwidth. A final highpass for the lower speed channel is set by C_{F4} at 400kHz. The high speed channel is used by FIR which uses 220ns wide pulses. A lowpass formed by R_{F1} and C_{F2} limit the noise bandwidth. A 480kHz highpass filter is set by C_{F6} and R_{F3}. Note that R_{F3} is also used to bias the filter buffer input to VBIAS (Pin 5). A final highpass at 110kHz is set by C_{F5}. The squelch circuit formed by Q1, Q2 and R_{C1} to R_{C4} extends the short range performance and will be discussed later.

In designing custom filters for different applications, the following guidelines should be used.

1. Limit the noise bandwidth with a lowpass filter that has a rise time equal to half the pulse width. For example, for 1μs pulses a 700kHz lowpass filter has a 10% to 90% rise time of 0.35/700kHz = 500ns.
2. Limit the maximum highpass to 1/(4 × pulse width). For 1μs pulses, 1/4μs = 250kHz.

APPLICATIONS INFORMATION

3. In setting the highpass filters, space the filters apart by a factor of 5 to 10 to reduce overshoot due to filter interaction. Overshoot becomes especially important for high input levels because it can cause false pulses which may not be tolerated in certain modulation schemes. It is also more of a problem in modulation schemes such as IRDA-SIR and FIR where the duty cycle can get very low (i.e., transmitting data with lots of ones which are signaled with the absence of pulses). AC coupled receivers when faced with low duty cycle data set their thresholds close to the baseline DC level of the data stream which converts small overshoots into erroneously received pulses.
4. As a general rule, place the lowest frequency highpass around the preamp and the highest highpass around the gain stage or between the preamp and gain stage. The reason for this is again due to high signal levels where there can be slow photocurrent tails. The tail response can be filtered out by high enough frequency filters.
5. In all cases with custom filtering, or when modifying one of the applications presented in this data sheet, try the system over the full distance range with a full range of duty cycle data streams. Modulation methods with fixed or limited duty cycle are superior because they have little or no data dependent problems.

Dynamic Range

The calculation of dynamic range can only be made in the context of a specific modulation scheme and with the system variations taken into account. The required information includes: minimum signal-to-noise ratio (or BER, Bit Error Rate requirement), photodiode capacitance at 1.9V back bias, preamp noise spectrum, preamp output filtering, AC loop cutoff frequencies, modulation method, demodulation method including allowable pulse widths and the effect of missing or extra pulses, photodiode rise and fall times, and ambient interference. The best solution is to experimentally determine the maximum and minimum distances at which a desired BER is obtained. This measure of dynamic range is more meaningful in terms of the overall system than any analytic solution.

Using the IRDA-SIR modulation scheme as an example, however, we can illustrate how some limits on the required receiver/photodiode combination can be obtained. The minimum light intensity in the angular range is 40mW/sr which translates to a photodiode current as follows (using the BPW34FA data sheet specs):

$$I_{PD(MIN)} = (40mW/sr) \times \left(\frac{7mm^2}{(1000mm)^2}\right) \times (0.65A/W)(0.95)(0.95) = 164nA$$

The $7mm^2$ term is the photodiode area. The 1000mm is the distance from the light source. The 0.65A/W is the spectral sensitivity at 880nm wavelength. The first 0.95 term is the relative sensitivity at 850nm wavelength and the second term is the sensitivity at 15° off axis. Similar calculations are detailed in the Infrared Data Association Serial Infrared (SIR) Physical Layer Link Specification, version 1.0. This minimum photocurrent implies that the input-referred noise current of the receiver be less than 13.7nA rms for a bit error rate of 1E-9. With an 800kHz lowpass filter on the preamp output the LT1319 has approximately 3.6nA rms of input-referred current noise. The maximum photodiode current at 20mm, on-axis with 500mW/sr intensity:

$$I_{PD(MAX)} = (500mW/sr) \times \left(\frac{7mm^2}{(20mm)^2}\right) \times (0.65A/W)(0.95) = 5.4mA$$

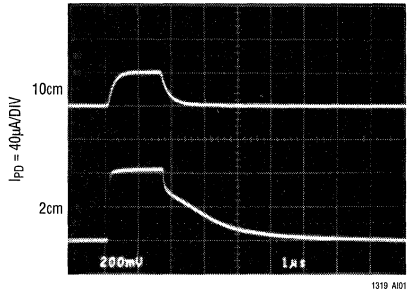
so we see that the dynamic range requirement is 90.4dB. What is not obvious, however, is that the photodiode output current is not simply a pulse of current, there is a significant tail at high current levels that has a time constant of more than 1µs which can cause distortion in the output pulse width of the LT1319. This tail can be shown in the following photograph which shows the voltage across a 5k resistor that is connected between the anode of a photodiode and ground. The cathode of the photodiode is connected to 2V. There is a 2pF Schottky diode across the resistor to clamp the voltage swing to less than 0.5V. With about 30pF photodiode capacitance and 10pF for an oscil-

5

APPLICATIONS INFORMATION

loscope probe, any tail observed with a time constant greater than 210ns is due to decaying photocurrent. The first trace in the photograph shows the current with the photodiode 10cm from a source with 100mW/sr intensity. At 200mV/div, there is about 40µA of peak current and the decay is consistent with the 210ns time constant. The lower trace shows the current with the photodiode 2cm from the LEDs where the photodiode current is theoretically 25 times greater than at 10cm. The voltage is clamped by the photodiode to nearly 0.4V, but what is now noticeable is that there is a tail with a time constant a bit greater than 1µs. If the signal is AC coupled and has a low duty cycle, the waveform will be centered at the very bottom which can result in very wide output pulses. This issue will be discussed later in more detail and a method to circumvent it will be shown.

Photocurrent Waveforms



Threshold Adjustment

The comparator thresholds are set by the current into Pin 11. The simplest method of setting this current is by a resistor, R_{T1} tied between Pin 11 and Pin 15 (V_{CC}). Pin 11 should be bypassed. The current is given by:

$$I_{TH} = \frac{(V_{CC} - 0.9V)}{(R_{T1} + 2k\Omega)}$$

The threshold referred to the input of the filter buffer is:

$$V_{TH} = \frac{I_{TH} \times 4 \times 500\Omega}{400V/V}$$

or nominally 0.68mV for R_{T1} = 30k. The largest practical value of R_{T1} is 39k. The limitation tends to be switching transients at the comparator outputs parasitically coupling to the FILTIN or FILTINL inputs and is layout dependent.

Extending Short Range Performance

The short range performance of the LT1319 is normally limited by the photocurrent tail, but in some instances the peak current level cannot be supported by the output of the preamplifier and the input will sag at Pin 2. Typically the maximum input current is 6mA. To increase this current to 20mA or more, place an NPN transistor with its emitter tied to Pin 2, the base to Pin 4 and collector to the 5V supply. The choice of transistor is dependent on the bandwidth required for the preamp. The base-emitter capacitance of the transistor (C_{JE}), is in parallel with the 15k feedback resistor of the preamplifier and performs a lowpass filtering function. For modest data rates such as IRDA-SIR and Sharp/Newton a 2N3904 limits the bandwidth to 2MHz which is ample. For the highest data rates, a transistor with f_T greater than 1GHz is needed such as MMBR941LT1.

Another issue with large input signals is the photocurrent tail. When this tail is AC coupled and the data has a low duty cycle, the output pulse width can become so wide that it extends into the next bit interval. A highpass filter can reject this tail, but for the case of IRDA-SIR, rejecting the 1µs time constant can cause rejection of the 1.6µs pulse which leads to a loss of sensitivity and reduced maximum link distance. The circuit on the front page of the data sheet uses a 500kHz highpass that trades off some sensitivity for rejection of this tail. Unfortunately both maximum and minimum distance are compromised. An alternative is shown in the IRDA-SIR/FIR application. In this instance the final highpass filter for SIR and FIR is moved into 400kHz, but a clamp/squelch circuit consisting of Q1, Q2, and R_{C1} to R_{C4} is added. Q1 is used as described above to clamp the input, but the input current level at which the clamp engages has been modified by R_{C1} and R_{C2}.

Without the resistors, Q1 would turn on when the voltage across the 15k resistor in the preamp reaches about 0.7V (a current of 0.7V/15kΩ = 47µA). The drop across R_{C1} reduces this voltage by about 480mV. The drop is set by the

APPLICATIONS INFORMATION

current through R_{C2} which is $[V_{CC} - (V_{BIAS} + 0.48V)]/11k\Omega = 238\mu A$ where $V_{BIAS} = 1.9V$. At this new level (0.22V/15kΩ = 14.7μA), Q1 turns on which clamps the preamp output. The collector current of Q1 provides base drive for Q2 which saturates and pulls its collector close to 5V. The FILT2L and FILT2 inputs are now pulled positive by R_{C3} and R_{C4} which forces an offset at the inputs to the gain stages. Referring to the Block Diagram, pulling FILT2L or FILT2 positive a voltage ΔV provides a voltage of ΔV/11 at the inverting input of the first gain stage. This offset effectively cuts off a portion of the tail at high input levels. The magnitude of ΔV is set by the value of R_{C3}, the current sinking capability of the transconductance stages (100μA), the value of C_{F4},C_{F5} and the duty cycle of the data pulses.

LED Drive Circuits

There are several simple circuits for driving LEDs. For low speed modulation methods such as IRDA-SIR and Sharp/Newton with pulses over 1μs, a 2N3904 in a SOT-23 package can be used as a switch with a series resistor in the collector to limit the current drive. This circuit is shown below with a suggested limiting resistor of 16Ω which typically sets the current at 200mA. The supply voltage must be well bypassed at the connection to the LED in order for the supply not to sag when hit with a fast current pulse. A 10μF low ESR capacitor should be used as well as a 0.1μF RF quality capacitor to reduce the high frequency spikes.

The current must be selected to achieve the minimum output light intensity at a given angle and must be lower than the manufacturer's maximum current rating at the maximum duty cycle of the modulation method. The optimum current is a function of the LED output, the LED forward voltage, the drop across the transistor and the minimum supply voltage.

$$I_{LED} = \frac{\left(V_{CC} - V_{LED} - V_{SW}\right)}{R_{SERIES}}$$

The minimum light output then can be obtained from the LED data sheet. For IRDA-SIR the minimum intensity at 15° off axis is 40mW/sr. For IRDA-FIR the spec rises to 100mW/sr. To increase light output and distance of the link, a second LED can be inserted in series with the first to obtain twice the light output without consuming additional supply current. The current variation will now be greater because two LED forward drops must be accounted for and the drop across the series resistor is greatly reduced.

For pulse widths less than 500ns the NPN should be replaced by an N-channel MOSFET with on-resistance of less than 1Ω with 5V on the gate. The FET can turn off much more quickly than the saturated NPN and provides a lower effective on-resistance. A suggested circuit is shown below and includes two devices available in the SOT-23 package.

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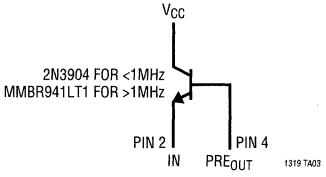
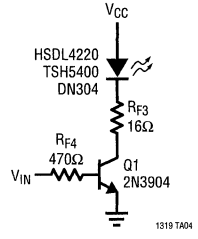
TYPICAL APPLICATIONS

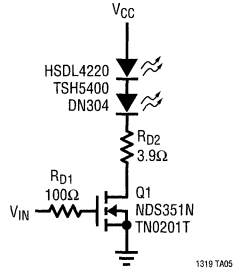
Optional Clamp Circuit



LED Drive Circuit for IRDA-SIR and Sharp/Newton

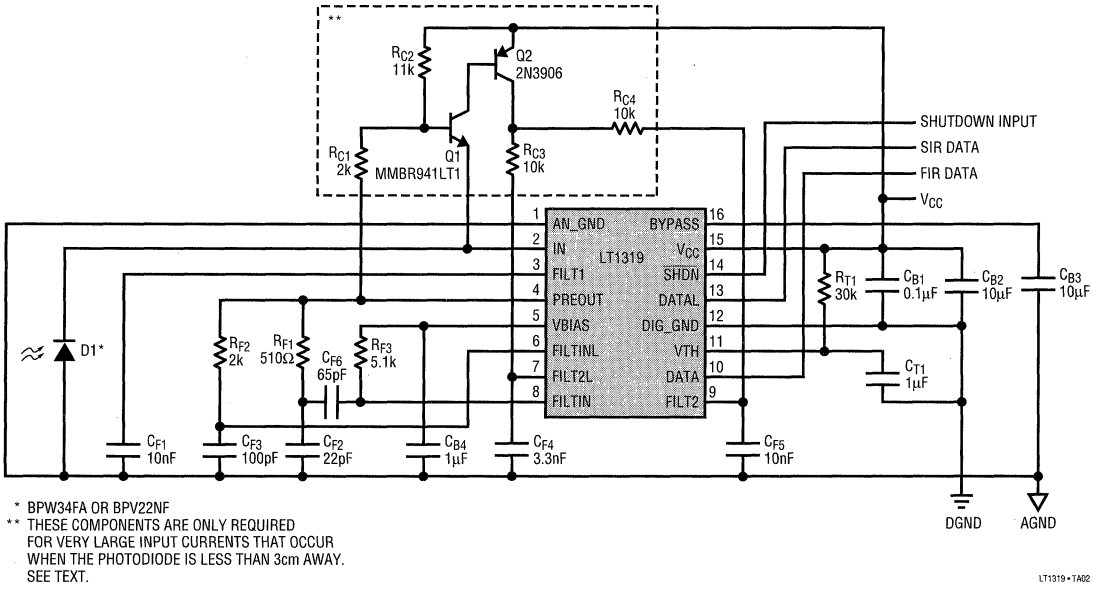


2 LED Drive Circuit for IRDA-FIR



TYPICAL APPLICATIONS

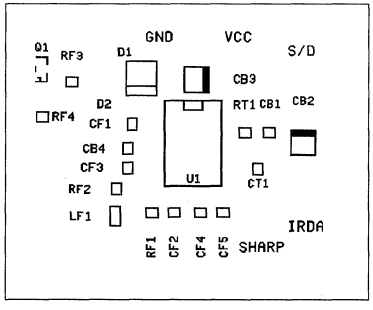
IRDA-SIR/FIR Data Receiver



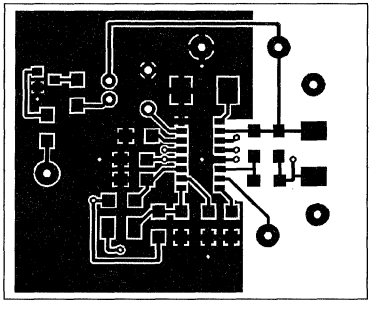
* BPW34FA OR BPV22NF
** THESE COMPONENTS ARE ONLY REQUIRED FOR VERY LARGE INPUT CURRENTS THAT OCCUR WHEN THE PHOTODIODE IS LESS THAN 3cm AWAY. SEE TEXT.

LT1319 • TA02

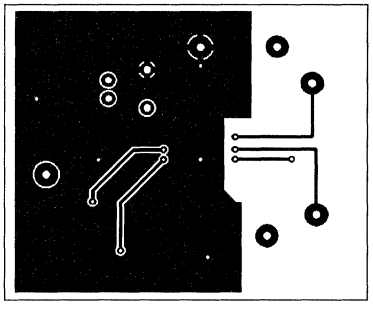
PC Board Layout for IRDA-SIR and Sharp/Newton Data Receiver with LED Drive Circuit



COMPONENT



TOP



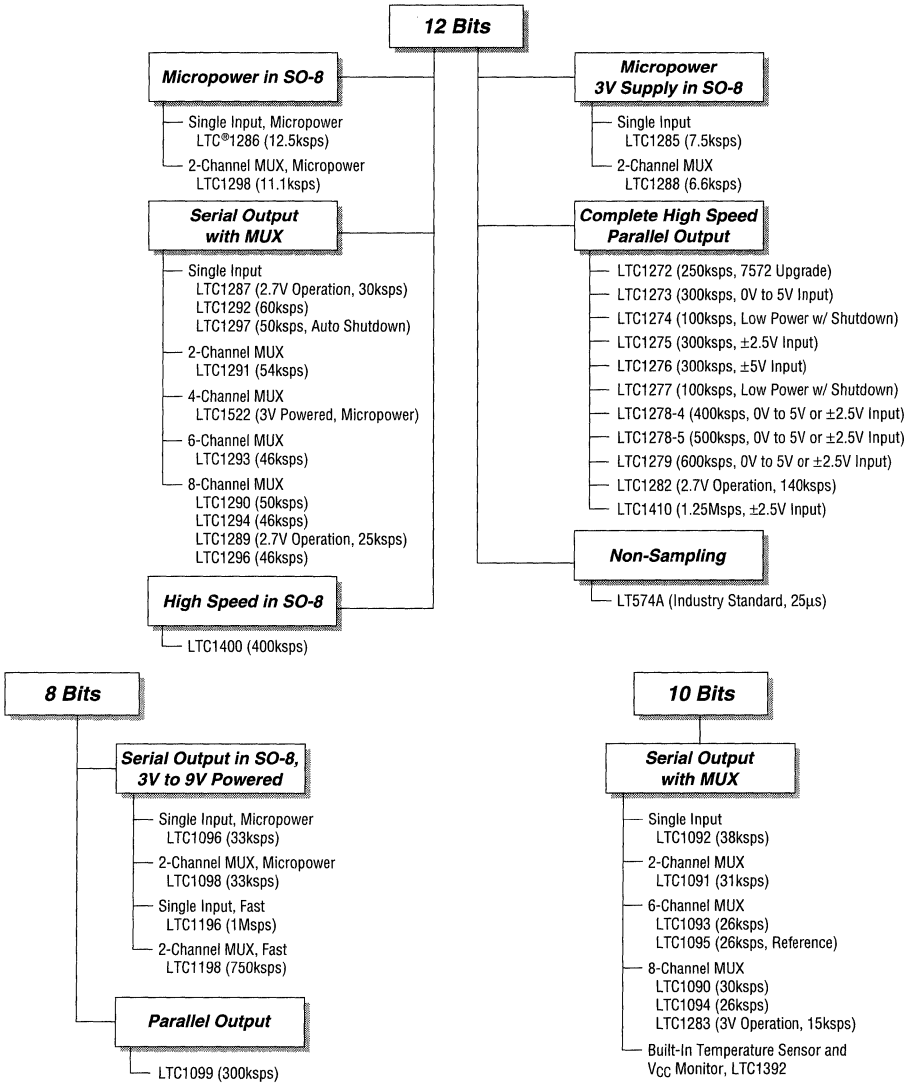
BOTTOM

SECTION 5—INTERFACE

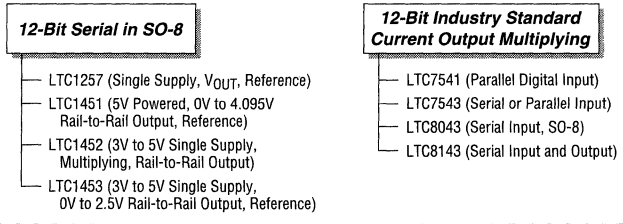
SECTION 6—DATA CONVERSION

SECTION 6—DATA CONVERSION

Analog-to-Digital Converters



Digital-to-Analog Converters

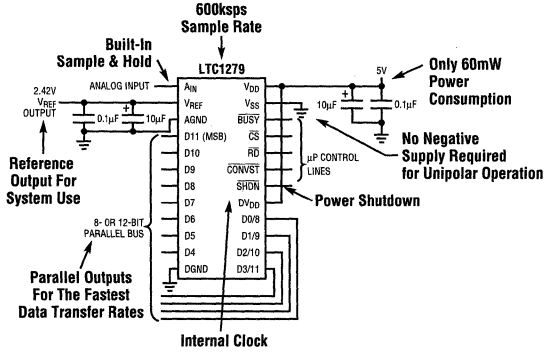


Complete Linear Technology 12-Bit A/D Feature Matrix

	SAMPLE RATE (ksps)	CONVERSION TIME (µs)	SUPPLY CURRENT (mA)	MICROPOWER	3V SINGLE SUPPLY OPERATION	5V SINGLE SUPPLY OPERATION	NUMBER OF INPUT CHANNELS	DIFFERENTIAL INPUT	BIPOLAR INPUT	HALF-DUPLEX SERIAL I/O	FULL-DUPLEX SERIAL I/O	PARALLEL I/O	SOFTWARE CONFIGURE	ONBOARD REFERENCE	MIN SPAN (V)	SHUTDOWN	SYSTEM SHUTDOWN OUTPUT	PACKAGES	NUMBER OF PINS
LTC1272-3	250	3	15			✓					✓		✓	N/A			J, N, SW	24
LTC1272-8	110	8	15			✓					✓		✓	N/A			J, N, SW	24
LTC1273	300	2.7	15			✓					✓		✓	5			J, N, SW	24
LTC1274	100	8	2.0			✓		✓			✓		✓	4	✓		SW	24
LTC1275	300	2.7	15					✓			✓		✓	±2.5			J, N, SW	24
LTC1276	300	2.7	15					✓			✓		✓	±5			J, N, SW	24
LTC1277	100	8	2			✓		✓	✓		✓		✓	4	✓		SW	24
LTC1278-4	400	2	15			✓			✓		✓		✓	5 ±2.5	✓		N, SW	24
LTC1278-5	500	1.6	15			✓			✓		✓		✓	5 ±2.5	✓		N, SW	24
LTC1279	600	1.4	12			✓			✓		✓		✓	5 ±2.5	✓		N, SW	24
LTC1282	140	5	4.0		✓				✓		✓		✓	2.5 ±1.25			J, N, SW	24
LTC1285	7.5	125	0.160*	✓	✓			✓		✓				1	✓		N, SO	8
LTC1286	12.5	80	0.250*	✓		✓		✓		✓				1	✓		N, SO	8
LTC1287	30	24	1.5		✓			✓		✓				1.2			J, N	8
LTC1288	6.6	141	0.210*	✓	✓		2	✓		✓			✓	2.7	✓		N, SO	8
LTC1289	25	26	1.5		✓		8	✓	✓		✓		✓	1.2	✓		J, N, SW	20
LTC1290	50	13	6			✓	8	✓	✓		✓		✓	1.2	✓		J, N, SW	20
LTC1291	54	12	6			✓	2	✓		✓			✓	N/A	✓		J, N	8
LTC1292	60	12	6			✓		✓		✓				1.2			J, N	8
LTC1293	46	12	6			✓	6	✓	✓	✓			✓	1.2	✓		J, N, SW	16
LTC1294	46	12	6			✓	8	✓	✓	✓			✓	1.2	✓		J, N	20
LTC1296	46	12	6			✓	8	✓	✓	✓			✓	1.2	✓	✓	J, N	20
LTC1297	50	12	6			✓		✓		✓				1.2	✓		J, N	8
LTC1298	11.1	90	0.340*	✓		✓	2	✓		✓			✓	2.7	✓		N, SO	8
LTC1400	400	2.1	15			✓			✓	✓			✓	4.1	✓		N8, S8	8
LTC1410	1250	0.75	12 –20					✓	✓		✓		✓	±2.5	✓		N, SO	28
LTC1522	10.5	60	0.16	✓	✓	✓	4			✓		✓		1.5			SO	16
LT574A	–	25	40 –25							✓	✓		✓	10			N	28

*Average supply current drops with sample rate. Supply current listed is at $f_{SAMPLE(MAX)}$

High Speed 12-Bit A/D Converters



- LTC1400: 400ksps in SO-8 Package!!

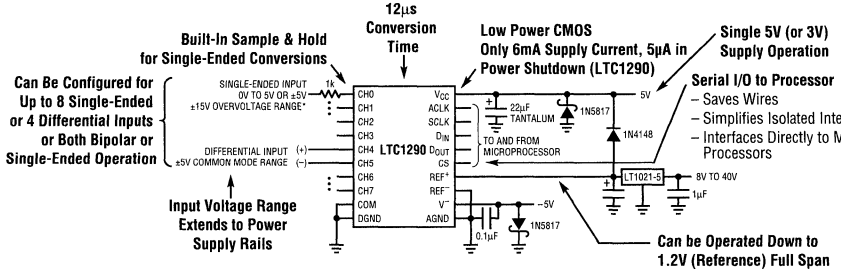
Comparison of Specs and Features

DEVICE TYPE	SAMPLING FREQ	S/(N + D) AT NYQUIST	INPUT RANGE	POWER SUPPLY	POWER DISSIPATION
LTC1272	250ksps	65dB	0V-5V	5V	75mW
LTC1273	300ksps	70dB	0V-5V	5V	75mW
LTC1274	100ksps	73dB	0V-4.096V or ±2.048	5V or ±5V	10mW 5µW (Shutdown)
LTC1275	300ksps	70dB	±2.5V	±5V	75mW
LTC1276	300ksps	70dB	±5V	±5V	75mW
LTC1277	100ksps	73dB	0V-4.096V or ±2.048	5V or ±5V	10mW 0.8mW*
LTC1278-4	400ksps	70dB	0V-5V or ±2.5V	5V or ±5V	75mW 5mW*
LTC1278-5	500ksps	70dB	0V-5V or ±2.5V	5V or ±5V	75mW 5mW*
LTC1279	600ksps	70dB	0V-5V or ±2.5V	5V or ±5V	60mW 7.5mW*
LTC1282	140ksps	68dB	0V-2.5V or ±1.25V	3V or ±3V	12mW
LTC1400	400ksps	70dB	0V-4.096V or ±2.048V	5V or ±5V	75mW
LTC1410	1.25Msps	71dB	±2.5	±5V	160mW

*Low power shutdown with instant wake up

Serial I/O 12-Bit A/D Converters

12-Bit Serial Interface A/D Converter Systems



Comparison of Specs and Features

Device Type	Analog Input Channels	Supply Voltage (V)	Sample Rate (ksps)	Number of Pins	Full/Half Duplex I/O	Auto Shutdown	Shutdown Status Pin
LTC1287	1	3	30	8	Half		
LTC1289	8	3/±3	25	20	Full		
LTC1290	8	5/±5	50	20	Full		
LTC1291	2	5	54	8	Half		
LTC1292	1	5	60	8	Half		
LTC1293	6	5/±5	46	16	Half		
LTC1294	8	5/±5	46	20	Half		
LTC1296	8	5/±5	46	20	Half		X
LTC1297	1	5	50	8	Half	X	
LTC1522	4	3	10.5	16	Half	X	

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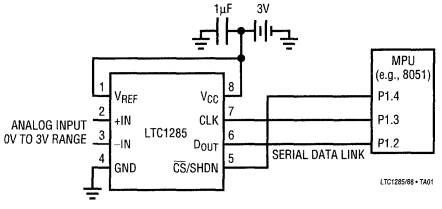
Micropower 12-Bit A/D Converters in SO-8 Packages

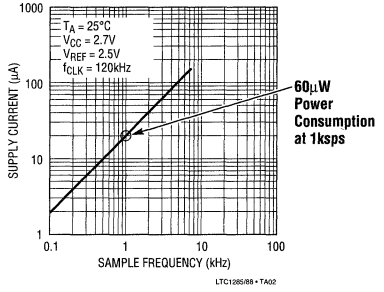
World's Lowest Power 12-Bit ADCs

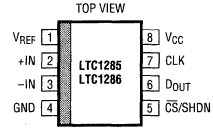
12-Bit Resolution
8-Pin SO Plastic Package
Low Cost
Low Supply Current: 160µA Typ (LTC1285)
Guaranteed ±3/4LSB Max DNL
Auto-Shutdown to 1nA Typ
Single Supply 3V to 6V Operation
(LTC1285/88) or 5V to 9V (LTC1286/98)
On-Chip Sample-and-Hold
100µs Conversion Time
Sampling Rates: 12.5ksps (LTC1286)
11.1ksps (LTC1298)
I/O Compatible with SPI, Microwire, etc.
Differential Inputs (LTC1285, LTC1286)
2-Channel MUX (LTC1288, LTC1298)

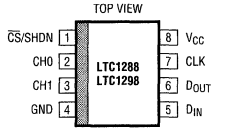
12µW, SO-8 Package, 12-Bit ADC
Samples at 200Hz and Runs Off a 3V Battery



Supply Current vs Sample Rate
(LTC1285)







S8 Package:
8-Lead Plastic SO

8-Bit A/D Converters in 8-Pin SO Packages

Lowest Power: LTC1096/LTC1098

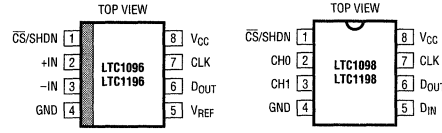
- 80µA Maximum Supply Current
- 1nA Supply Current in Shutdown
- Operate from 2.7V to 9V Single Supply
- 33ksps Sample Rate

Highest Speed: LTC1196/LTC1198

- 8-Bit Resolution
- 1Msps Sample Rate
- 100ns Sample/Hold Acquisition Time
- Single Supply 2.7V to 6V Operation
- Low Power: 10mW at 3V, 50mW at 5V
- Auto-Shutdown to 1nA (LTC1198)

Comparison of Specs and Features

Device Type	Supply Voltage Range (V_{CC})	Max Sampling Rate (ksps)	P_D (mW) @ V_{CC} MSR @ $f_{S(MAX)}$	P_D @ 1ksps (mW)	Input Range
LTC1096	2.7 to 9	33	0.6 @ 5V	0.017	0V to V_{REF}
LTC1098	2.7 to 6	33	0.6 @ 5V	0.017	0V to V_{CC}
LTC1196	2.7 to 6	1000	55 @ 5V	40	0V to V_{REF}
LTC1198	2.7 to 6	750	55 @ 5V	0.05	0V to V_{CC}

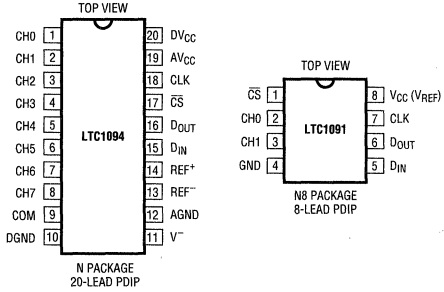


N8 Package: 8-Lead PDIP
S8 Package: 8-Lead Plastic SO

10-Bit A/D Converter "Systems on a Chip"

	Sample Rate (kHz)	Conversion Time (µs)	Supply Current (mA)	3V Single Supply Operation	5V Single Supply Operation	Number of Input Channels	Differential Input	Bipolar Input	Half-Duplex Serial I/O	Full-Duplex Serial I/O	Software Configured	Onboard Reference	Min Span. (V)	Packages	Number of Pins	Price (100+, P DIP)
LTC1090	30	22	1		✓	8	✓	✓		✓	✓		0.2	J, N, SW	20	9.90
LTC1091	31	20	1.5		✓	2	✓		✓		✓		N/A	J, N	8	9.90
LTC1092	38	20	1		✓		✓		✓				0.2	J, N	8	9.90
LTC1093	26	20	1		✓	6	✓	✓	✓		✓		0.2	J, N, SW	16	9.90
LTC1094	26	20	1		✓	8	✓	✓	✓		✓		0.2	J, N	20	9.90
LTC1095	26	20	2.3		✓	6	✓	✓	✓		✓	✓	N/A	J	18	12.00
LTC1283	15	44	0.15	✓		8	✓	✓		✓	✓		0.2	J, N	20	11.40

Representative Pin Configurations

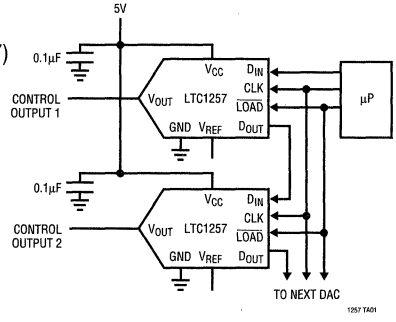


LTC1257/LTC1451/LTC1453: Complete Single Supply 12-Bit Voltage Output DACs in SO-8 Packages

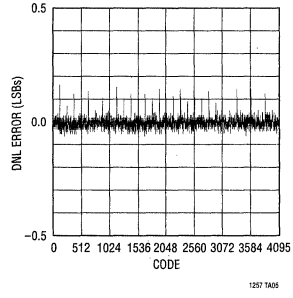
Features

- 8-Pin SO Package
- Buffered Voltage Output
- Built-In Reference (Except LTC1452)
- 500µV/LSB with 2.048V Full Scale (LTC1257)
- 1mV/LSB with 4.095V Full Scale (LTC1451)
- 1/2 LSB Max DNL Error
- Guaranteed 12-Bit Monotonic
- 3-Wire Cascadable Serial Interface
- Wide Single Supply Range: (LTC1257) V_{CC} = 4.75V to 15.75V
- Low Power: I_{CC} Typ = 350µA with 5V Supply
- Power-On Reset: LTC1451/52/53

Typical Application



Differential Nonlinearity vs Input Code



Applications

- Digital Offset/Gain Adjustment
- Industrial Process Control
- Automatic Test Equipment

ECTION 6—DATA CONVERSION

12-Bit, 600ksps Sampling A/D Converter with Shutdown

FEATURES

- **Single Supply 5V or ±5V Operation**
- **Sample Rate: 600ksps**
- **70dB S/(N + D) and 74dB THD at Nyquist**
- **Power Dissipation: 60mW Typ**
- Power Shutdown with Instant Wake-Up
- Internal Reference Can Be Overdriven Externally
- Internal Synchronized Clock; No Clock Required
- High Impedance Analog Input
- Input Range: 0V to 5V or ±2.5V
- New Flexible, Friendly Parallel Interface Eases Connections to DSPs and FIFOs
- 24-Pin SO Wide Package

APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Spectrum Analysis

DESCRIPTION

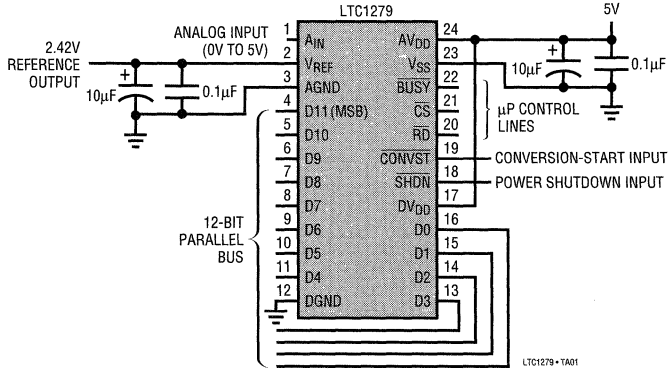
The LTC®1279 is a 1.4µs, 600ksps, sampling 12-bit A/D converter which draws only 60mW from a single 5V or ±5V supplies. This easy-to-use device comes complete with a 160ns sample-and-hold, a precision reference and an internally trimmed clock. Unipolar and bipolar conversion modes add to the flexibility of the ADC. The low power dissipation is reduced even more, drawing only 8.5mW in power shutdown mode. Instant wake-up from power shutdown allows the converter to be powered down even during brief inactive periods.

The LTC1279 converts 0V to 5V unipolar inputs from a single 5V supply and ±2.5V bipolar inputs from ±5V supplies. Maximum DC specs include ±1LSB INL and ±1LSB DNL. Outstanding guaranteed AC performance includes 70dB S/(N+D) and 78dB THD at the input frequency of 100kHz over temperature.

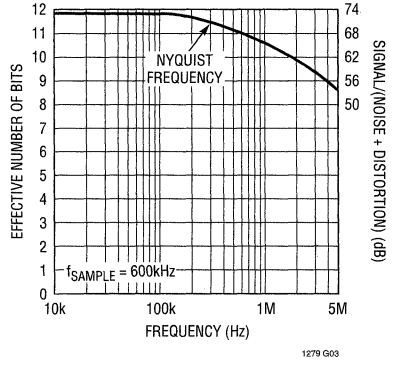
The internal clock is trimmed for 1.4µs conversion time. The clock automatically synchronizes to each sample command, eliminating problems with asynchronous clock noise found in competitive devices. A separate conversion start input and a data-ready signal ($\overline{BUSY}$) ease connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION

Single 5V Supply, 600kHz, 12-Bit Sampling A/D Converter



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

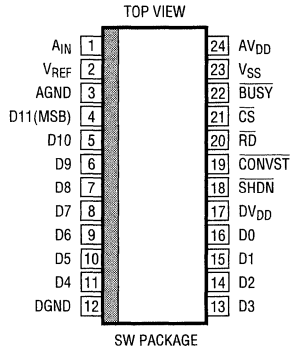


ıBSOLUTE MAXIMUM RATINGS

/DD = DVDD = VDD (Notes 1, 2)

upply Voltage (V_{DD}) 7V
egative Supply Voltage (V_{SS})
Bipolar Operation Only ..... −6V to GND
ɔtal Supply Voltage (V_{DD} to V_{SS})
Bipolar Operation Only 12V
nalog Input Voltage (Note 3)
Unipolar Operation ..... − 0.3V to V_{DD} + 0.3V
Bipolar Operation..... V_{SS} − 0.3V to V_{DD} + 0.3V
igital Input Voltage (Note 4)
Unipolar Operation ..... −0.3V to 12V
Bipolar Operation..... V_{SS} − 0.3V to 12V
igital Output Voltage
Unipolar Operation ..... −0.3V to V_{DD} + 0.3V
Bipolar Operation..... − 0.3V to V_{DD} + 0.3V
ɔwer Dissipation..... 500mW
perating Temperature Range
LTC1279C..... 0°C to 70°C
LTC1279I..... −40°C to 85°C
torage Temperature Range ..... −65°C to 150°C
ɜad Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER*
LTC1279CSW
LTC1279ISW

*Consult factory for plastic DIP package.
Consult factory for Military grade parts.

6

ONVERTER CHARACTERISTICS With Internal Reference (Notes 5, 6)

ıRAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ɜolution (No Missing Codes)		●	12			Bits
ɜgral Linearity Error	(Note 7)	●			±1	LSB
ffferential Linearity Error		●			±1	LSB
ɔolar Offset Error	(Note 8)				±4	LSB
		●			±6	LSB
ıipolar Offset Error					±6	LSB
		●			±8	LSB
ɜin Error					±15	LSB
ɜin Error Tempco	$I_{OUT(REF)}$ = 0	●		±10	±45	ppm/°C

ıNALOG INPUT (Note 5)

′MBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ɣ	Analog Input Range (Note 9)	4.95V ≤ V_{DD} ≤ 5.25V (Unipolar)	●		0 to 5		V
		4.75V ≤ V_{DD} ≤ 5.25V, −5.25V ≤ V_{SS} ≤ −2.45V (Bipolar)	●		±2.5		V
	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
ɣ	Analog Input Capacitance	Between Conversions (Sample Mode)			25		pF
		During Conversions (Hold Mode)			5		pF

DYNAMIC ACCURACY (Notes 5, 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal 300kHz Input Signal	● 	70	72 70		dB dB
THD	Total Harmonic Distortion First 5 Harmonics	100kHz Input Signal 300kHz Input Signal	● 		−82 −74	−78	dB dB
	Peak Harmonic or Spurious Noise	100kHz Input Signal 300kHz Input Signal	● 		−82 −80	−78	dB dB
IMD	Intermodulation Distortion	f_{IN1} = 94.189kHz, f_{IN2} = 97.705kHz 2nd Order Terms 3rd Order Terms			 −81 −78		 dB dB
		f_{IN1} = 299.26kHz, f_{IN2} = 305.12kHz 2nd Order Terms 3rd Order Terms			 −77 −74		 dB dB
	Full Power Bandwidth				5		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 68dB)				500		kHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.400	2.420	2.440	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±10	±45	ppm/°C
V_{REF} Line Regulation	4.95V ≤ V_{DD} ≤ 5.25V −5.25V ≤ V_{SS} ≤ −4.95V			0.01 0.01		LSB/V LSB/V
V_{REF} Load Regulation	−5mA ≤ I_{OUT} ≤ 800µA			2		LSB/mA

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.95V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.95V I_O = −10µA I_O = −200µA	 ●	 4.0	 4.9 	 	 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.95V I_O = 160µA I_O = 1.6mA	 ●	 	 0.05 0.10	 0.4	 V V
I_{OZ}	High-Z Output Leakage D11 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High-Z Output Capacitance D11 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage (Notes 11, 12)	Unipolar		4.95		5.25	V
		Bipolar		4.75		5.25	V
V_{SS}	Negative Supply Voltage (Note 11, 12)	Bipolar Only		–2.45		–5.25	V
I_{DD}	Positive Supply Current	f_{SAMPLE} = 600ksps	●		12	24	mA
		$\overline{SHDN}$ = 0V	●		1.7	3	mA
I_{SS}	Negative Supply Current	f_{SAMPLE} = 600ksps, V_{SS} = –5V	●		0.12	0.30	mA
P_D	Power Dissipation	f_{SAMPLE} = 600ksps	●		60	120	mW
		$\overline{SHDN}$ = 0V	●		8.5	15	mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	600			kHz
$t_{SAMPLE(MIN)}$	Minimum Throughput Time (Acquisition Time Plus Conversion Time)		●			1.66	µs
t_{CONV}	Conversion Time		●		1.4	1.6	µs
t_{ACQ}	Acquisition Time				160		ns
	$\overline{CS}\downarrow$ to $\overline{RD}\downarrow$ Setup Time	(Notes 9, 11)	●	0			ns
	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Notes 9, 11)	●	20			ns
	$\overline{SHDN}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	(Note 11)			350		ns
	$\overline{CONVST}$ Low Time	(Notes 11, 13)	●	40			ns
	$\overline{CONVST}\downarrow$ to $\overline{BUSY}\downarrow$ Delay	C_L = 100pF			50	110	ns
		Commercial	●			130	ns
		Industrial	●			140	ns
	Data Ready Before $\overline{BUSY}\uparrow$	C_L = 20pF	●	20	40		ns
	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$	Mode 2, (See Figure 14) (Note 9)	●	–20			ns
	Data Access Time After $\overline{RD}\downarrow$	C_L = 20pF (Note 9)			35	90	ns
		Commercial	●			110	ns
		Industrial	●			120	ns
		C_L = 100pF			50	125	ns
		Commercial	●			150	ns
		Industrial	●			170	ns
	Bus Relinquish Time	(3k and 10pF Connected as Shown in Test Circuits)		10	30	75	ns
		Commercial	●	10		85	ns
		Industrial	●	10		90	ns
t_{10}	$\overline{RD}$ Low Time	(Note 9)	●	t_8			ns
t_{11}	$\overline{CONVST}$ High Time	(Notes 9, 13)	●	40			ns
t_{12}	Aperture Delay of Sample-and-Hold	Jitter <50ps			12		ns

6

TIMING CHARACTERISTICS (Note 5)

The ● indicates specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When the analog input voltage is taken below V_{SS} (ground for unipolar mode) or above V_{DD}, it will be clamped by internal diodes. This product can handle input currents greater than 80mA below V_{SS} (ground for unipolar mode) or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} (ground for unipolar mode), they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for unipolar mode) without latch-up. These pins are not clamped to V_{DD}.

Note 5: AV_{DD} = DV_{DD} = V_{DD} = 5V, (V_{SS} = –5V for bipolar mode), f_{SAMPLE} = 600kHz, t_r = t_f = 5ns unless otherwise specified.

Note 6: Linearity, offset and full scale specifications apply for unipolar and bipolar modes.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. Th deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –1/2LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

Note 10: The AC test is for bipolar mode. The signal-to-noise plus distortion ratio is about 1dB lower for unipolar mode, so the typical S/(N + D) at 100kHz in unipolar mode is 71dB.

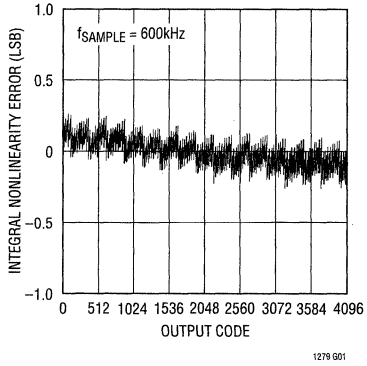
Note 11: Recommended operating conditions.

Note 12: A_{IN} must not exceed V_{DD} or fall below V_{SS} by more than 50mV fo specified accuracy. Therefore the minimum supply voltage for the unipolar mode is 4.95V. The minimum for the bipolar mode is 4.75V, –2.45V.

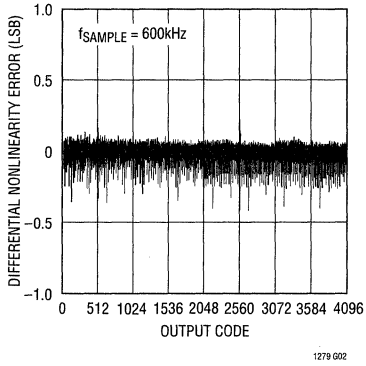
Note 13: The falling $\overline{CONVST}$ edge starts a conversion. If $\overline{CONVST}$ returns high at a bit decision point during the conversion it can create small errors For best performance ensure that $\overline{CONVST}$ returns high either within 120n after conversion start (i.e., before the first bit decision) or after $\overline{BUSY}$ rises (i.e., after the last bit test). See mode 1a and 1b (Figures 12 and 13) timing diagrams.

TYPICAL PERFORMANCE CHARACTERISTICS

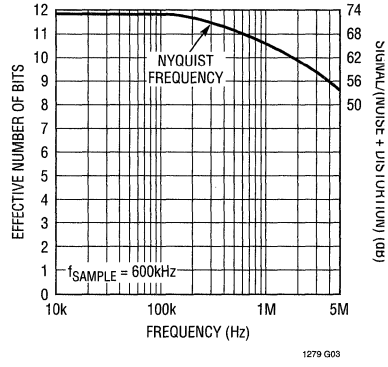
Integral Nonlinearity vs Output Code



Differential Nonlinearity vs Output Code

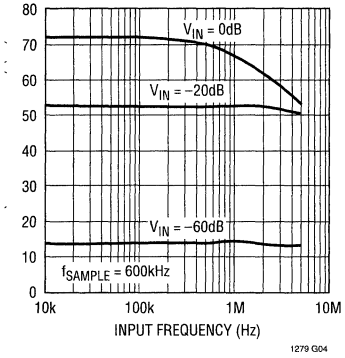


ENOBs and S/(N + D) vs Input Frequency

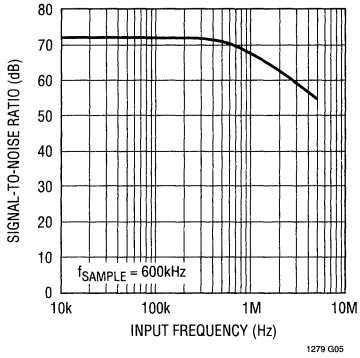


TYPICAL PERFORMANCE CHARACTERISTICS

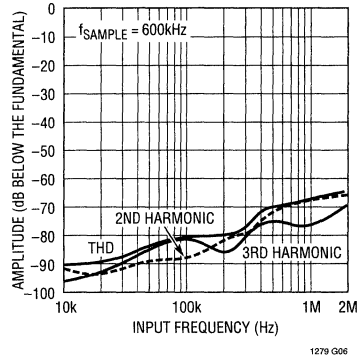
S/(N + D) vs Input Frequency and Amplitude



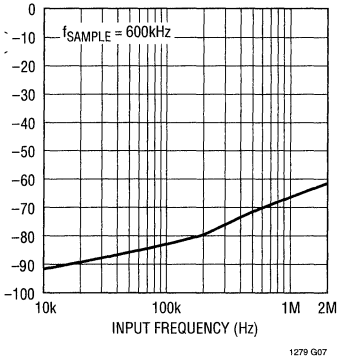
Signal-to-Noise Ratio (Without Harmonics) vs Input Frequency



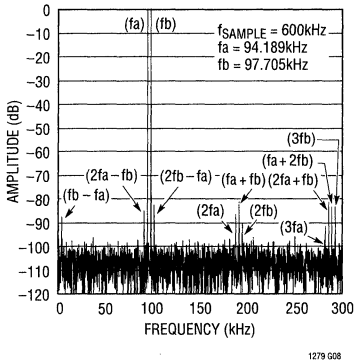
Distortion vs Input Frequency



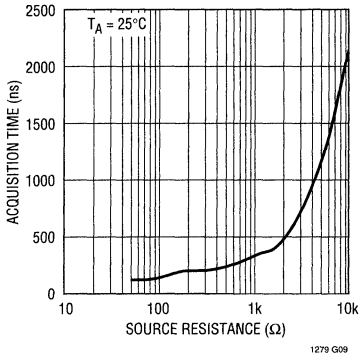
Peak Harmonic or Spurious Noise vs Input Frequency



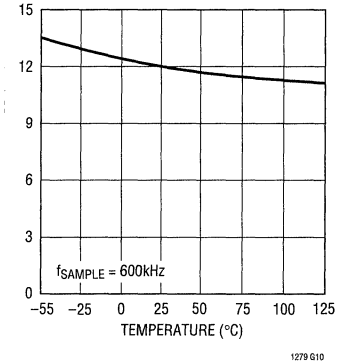
Intermodulation Distortion Plot



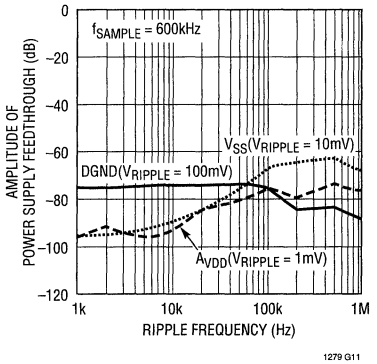
Acquisition Time vs Source Impedance



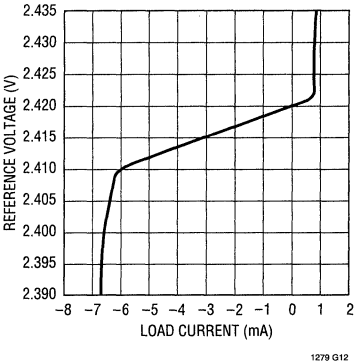
Supply Current vs Temperature



Power Supply Feedthrough vs Ripple Frequency



Reference Voltage vs Load Current



6

PIN FUNCTIONS

A_{IN} (Pin 1): Analog Input. 0V to 5V (Unipolar), ±2.5V (Bipolar).

V_{REF} (Pin 2): 2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

AGND (Pin 3): Analog Ground.

D11 to D4 (Pins 11 to 4): Three-State Data Outputs. D11 is the Most Significant Bit.

DGND (Pin 12): Digital Ground.

D3 to D0 (Pins 13 to 16): Three-State Data Outputs.

DV_{DD} (Pin 17): Digital Power Supply, 5V. Tie to AV_{DD} pin.

$\overline{SHDN}$ (Pin 18): Power Shutdown. The LTC1279 powers down when $\overline{SHDN}$ is low.

$\overline{CONVST}$ (Pin 19): Conversion Start Input. It is active low. The falling edge of the $\overline{CONVST}$ signal initiates a conversion. The LTC1279 responds to $\overline{CONVST}$ signal only if the signal applied to $\overline{CS}$ is a logic low.

$\overline{RD}$ (Pin 20): READ Input. A logic low signal applied to this pin enables the output data drivers when the signal applied to the $\overline{CS}$ pin is a logic low.

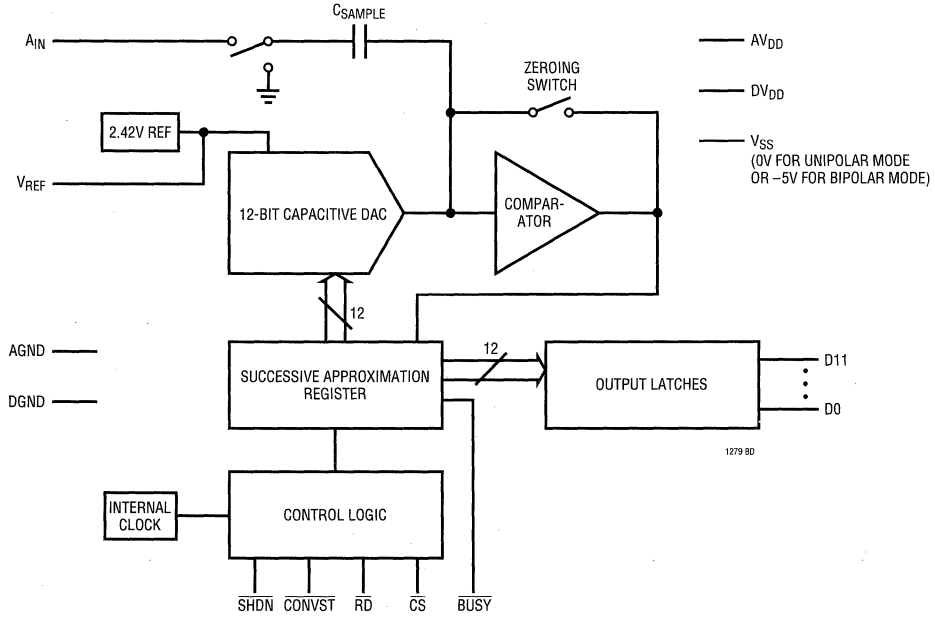
$\overline{CS}$ (Pin 21): The CHIP SELECT input must be a logic low for the ADC to recognize the signals applied to the $\overline{CONVST}$ and $\overline{RD}$ inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ output shows the converter status. It is a logic low during a conversion.

V_{SS} (Pin 23): Negative Supply. –5V will select bipolar operation. Bypass to AGND with 0.1µF ceramic. Tie to analog ground to select unipolar operation.

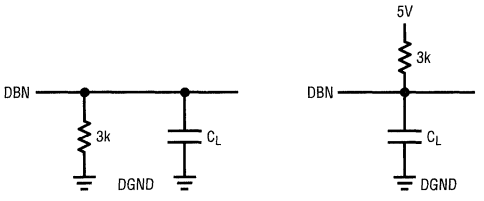
AV_{DD} (Pin 24): Positive Supply, 5V. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

FUNCTIONAL BLOCK DIAGRAM

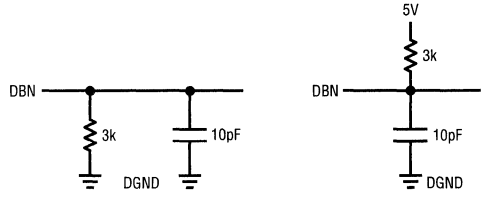


TEST CIRCUITS

Load Circuits for Access Timing

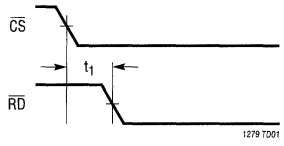


Load Circuits for Output Float Delay

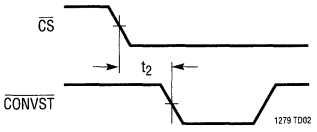


TIMING DIAGRAMS

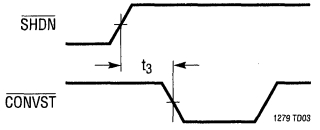
$\overline{CS}$ to $\overline{RD}$ Setup Timing



$\overline{CS}$ to $\overline{CONVST}$ Setup Timing



$\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing



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CONVERSION DETAILS

The LTC1279 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit parallel output. The ADC is complete with a precision reference and an internal clock. The control logic provides easy interface to microprocessors and DSPs. (Please refer to the Digital Interface section for the data format.)

Conversion start is controlled by the $\overline{CS}$ and $\overline{CONVST}$ inputs. At the start of conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor during the acquire phase, and the comparator offset is nulled by the feedback switch. In this acquire phase, a minimum delay of 160ns will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switch switches C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively com-

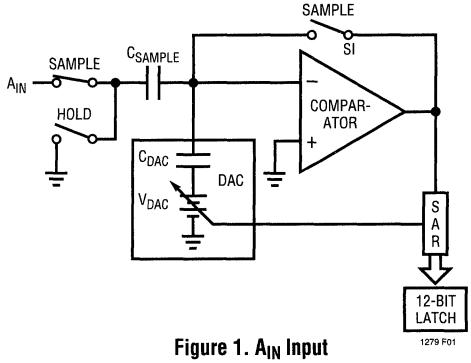

Figure 1. A_{IN} Input

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pared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} input charge. The SAR contents (a 12-bit data word) which represent the A_{IN} are loaded into the 12-bit output latches.

DYNAMIC PERFORMANCE

The LTC1279 has excellent high speed sampling capability. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figures 2a and 2b show typical LTC1279 FFT plots.

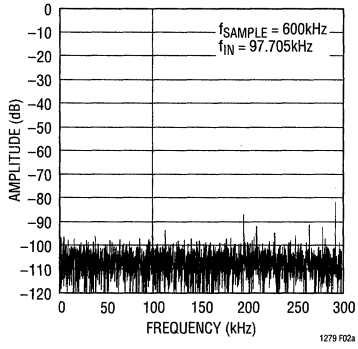

Figure 2a. LTC1279 Nonaveraged, 4096 Point FFT Plot with 100kHz Input Frequency

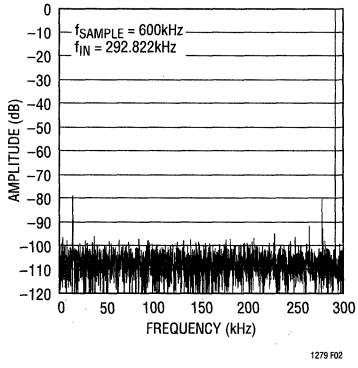

Figure 2b. LTC1279 Nonaveraged, 4096 Point FFT Plot with 300kHz Input Frequency

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. The output is band limited to frequencies above DC and below half the sampling frequency. Figure 2a shows a typical spectral content with a 600kHz sampling rate and a 100kHz input. The dynamic performance is excellent for input frequencies up to the Nyquist limit of 300kHz as shown in Figure 2b.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02$$

where N is the Effective Number of Bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 600kHz the LTC1279 maintains very good ENOBs up to the Nyquist input frequency of 300kHz. Refer to Figure 3.

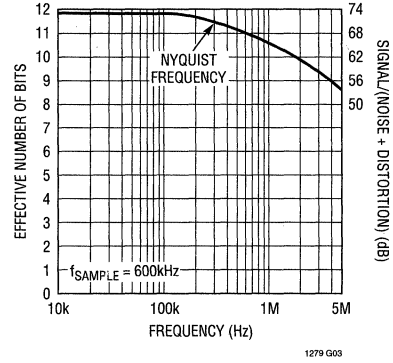

Figure 3. Effective Bits and Signal/(Noise + Distortion) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

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$$THD = 20\log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 \ldots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics. THD versus input frequency is shown in Figure 4. The LTC1279 has good distortion performance up to the Nyquist frequency and beyond.

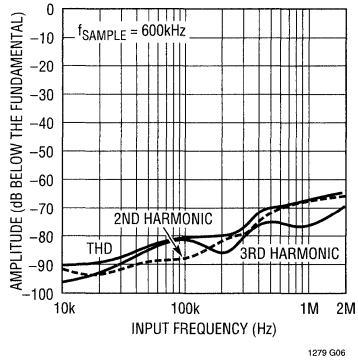

Figure 4. Distortion vs Input Frequency

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include (fa + fb) and (fa – fb) while the 3rd order IMD terms include (2fa + fb), (2fa – fb), (fa + 2fb), and (fa – 2fb). If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\ (fa \pm fb) = 20\log \frac{\text{Amplitude at } (fa \pm fb)}{\text{Amplitude at fa}}$$

Figure 5 shows the IMD performance at a 100kHz input.

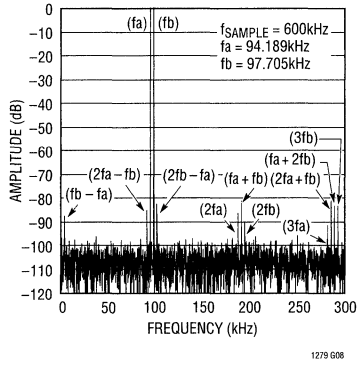

Figure 5. Intermodulation Distortion Plot

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibels relative to the RMS value of a full scale input signal.

Full Power and Full Linear Bandwidth

The full power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full scale input signal.

The full linear bandwidth is the input frequency at which the S/(N + D) has dropped to 68dB (11 effective bits). The LTC1279 has been designed to optimize input bandwidth, allowing ADC to undersample input signals with frequencies above the converter's Nyquist Frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Driving the Analog Input

The LTC1279's analog input is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion the analog input draws no current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 160ns to small current transients will allow maximum speed operation. If slower

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op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's A_{IN} input include the LT®1360, LT1220, LT1223 and LT1224 op amps.

Internal Reference

The LTC1279 has an on-chip, temperature compensated, curvature corrected, bandgap reference that is factory trimmed to 2.42V. It is internally connected to the DAC and is available at pin 2 to provide up to 800µA current to an external load.

For minimum code transition noise, the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic).

The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment in bipolar mode. The V_{REF} pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should be driven to no more than 4.8V to keep the input span within the ±5V supplies.

Figure 6 shows an LT1006 op amp driving the V_{REF} pin. (In the unipolar mode, the input span is already 0V to 5V with the internal reference so driving the reference is not recommended, since the input span will exceed the supply and codes will be lost at the full scale.) Figure 7 shows a typical reference, the LT1019A-2.5 connected to the LTC1279. This will provide an improved drift (equal to the LT1019A-2.5's maximum of 5ppm/°C) and a ±2.582V full scale.

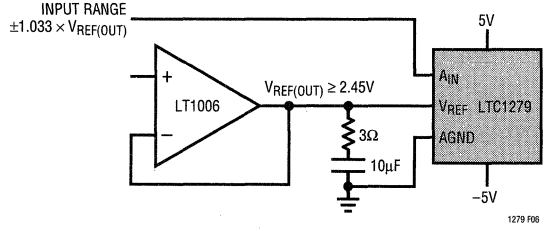

Figure 6. Driving the V_{REF} with the LT1006 Op Amp

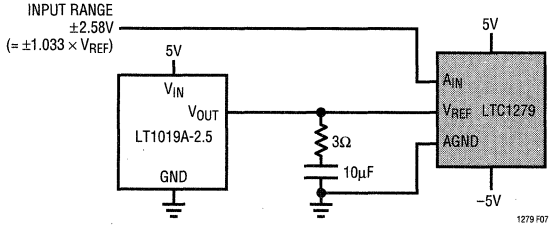

Figure 7. Supplying a 2.5V Reference Voltage to the LTC1279 with the LT1019A-2.5

UNIPOLAR/BIPOLAR OPERATION AND ADJUSTMENT

Figure 8a shows the ideal input/output characteristics for the LTC1279. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, ... FS – 1.5LSB). The output code is naturally binary with 1LSB = FS/4096 = 5V/4096 = 1.22mV. Figure 8b shows the input/output transfer characteristics for the bipolar mode in two's complement format.

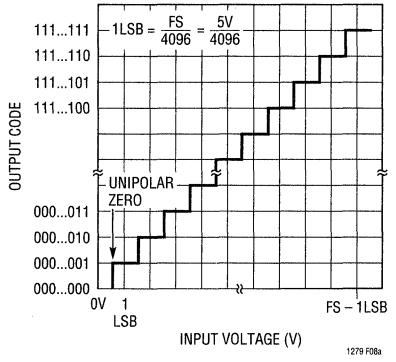

Figure 8a. LTC1279 Unipolar Transfer Characteristics

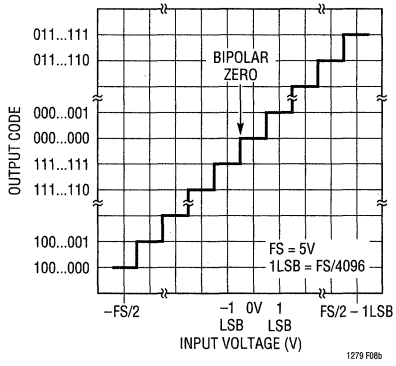

Figure 8b. LTC1279 Bipolar Transfer Characteristics

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Unipolar Offset and Full-Scale Error Adjustments

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 9a shows the extra components required for full-scale error adjustment. If both offset and full-scale adjustments are needed, the circuit in Figure 9b can be used. For zero offset error apply 0.61mV (i.e., 0.5LSB) at the input and adjust the offset trim until the LTC1279 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error apply an analog input of 4.99817V (i.e., FS – 1.5LSB or last code transition) at the input and adjust R5 until the LTC1279 output code flickers between 1111 1111 1110 and 1111 1111 1111.

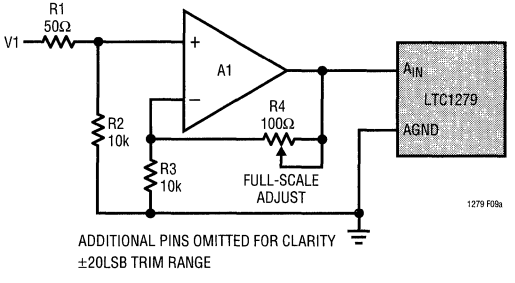

Figure 9a. Full-Scale Adjust Circuit

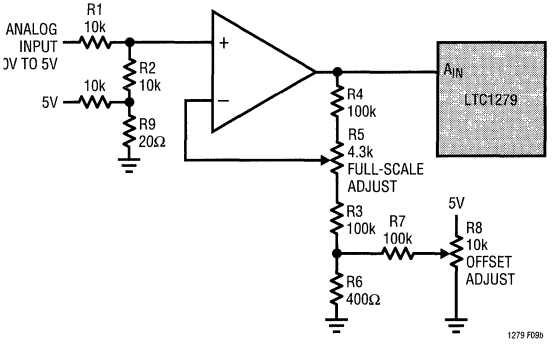

Figure 9b. LTC1279 Unipolar Offset and Full-Scale Adjust Circuit

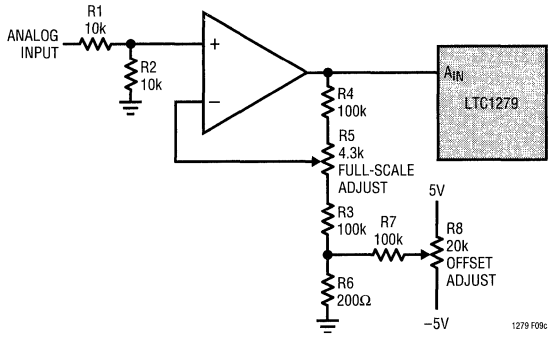

Figure 9c. LTC1279 Bipolar Offset and Full-Scale Adjust Circuit

Bipolar Offset and Full-Scale Error Adjustments

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Again, bipolar offset must be adjusted before full-scale error. Bipolar offset error adjustment is achieved by trimming the offset of the op amp driving the analog input of the LTC1279 while the input voltage is 0.5LSB below ground. This is done by applying an input voltage of –0.61mV (–0.5LSB) to the input in Figure 9c and adjusting the R8 until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full scale adjustment, an input voltage of 2.49817V (FS – 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1279, a printed circuit board is required. The printed circuit board's layout should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital trace alongside an analog signal trace or underneath the ADC. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the AV_{DD} and V_{REF} pins as shown in Figure 10. For the bipolar mode, a 0.1µF ceramic provides

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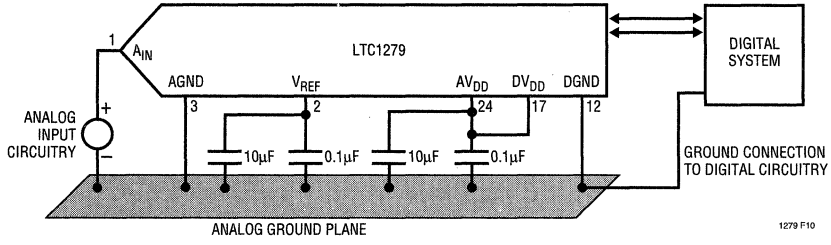

Figure 10. Power Supply Grounding Practice

adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Input signal traces to A_{IN} (pin 1) and signal return traces from AGND (pin 3) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between the signal source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

A single point analog ground, separate from the logic system ground, should be established with an analog ground plane at pin 3 (AGND) or as close as possible to the ADC. Pin 12 (DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion.

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 1.4µs. No external adjustments are required, and with the typical acquisition time of 160ns, throughput performance of 600ksps is assured.

Power Shutdown

The LTC1279 provides a power shutdown feature that saves power when the ADC is in inactive periods. To power down the ADC, pin 18 ($\overline{SHDN}$) needs to be driven low. When in power shutdown mode, the LTC1279 will not start a conversion even though the $\overline{CONVST}$ goes low. All the power is off except the Internal Reference which is still active and provides 2.42V output voltage to the other circuitry. In this mode the ADC draws 8.5mW instead of 60mW (for minimum power, the logic inputs must be within 600mV of the supply rails). The wake-up time from the power shutdown to active state is 350ns.

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Timing and Control

Conversion start and data read operations are controlled by three digital inputs: $\overline{CS}$, $\overline{CONVST}$ and $\overline{RD}$. Figure 11 shows the logic structure associated with these inputs. A logic "0" for $\overline{CONVST}$ will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

Figures 12 through 16 show several different modes of operation. In modes 1a and 1b (Figures 12 and 13) $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

In mode 2 (Figure 14) $\overline{CS}$ is tied low. The falling $\overline{CONVST}$ signal again starts the conversion. Data outputs are in three-state until read by MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared MPU databus.

In Slow memory and ROM modes (Figures 15 and 16) $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts conversion and reads the output with the $\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

In Slow memory mode the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting the conversion. $\overline{BUSY}$ goes low, forcing the processor into a WAIT state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high, releasing the processor; the processor applies a logic high to $\overline{RD}$ (= $\overline{CONVST}$) and reads the new conversion data.

In ROM mode, the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result (which will initiate another conversion).

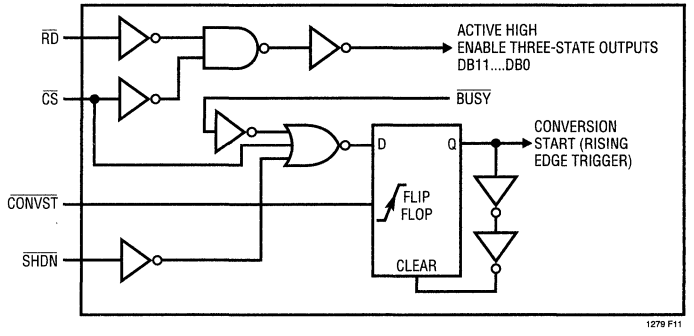

Figure 11. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$, $\overline{CONVST}$ and $\overline{SHDN}$

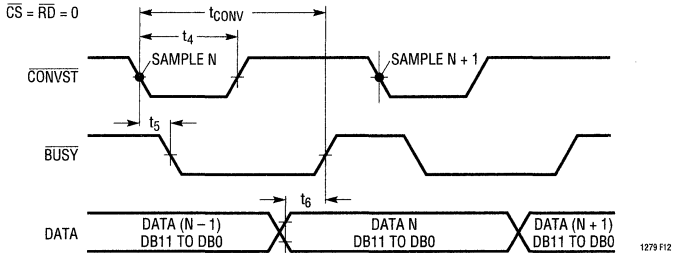

Figure 12. Mode 1a. $\overline{CONVST}$ Starts a Conversion. Data Ouputs Always Enabled. ($\overline{CONVST}$ = ⊓⊔⊓)

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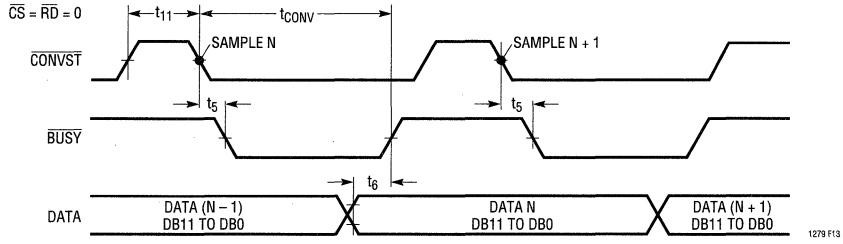


Figure 13. Mode 1b. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled.($\overline{CONVST}$ = ⎍‾⎍)

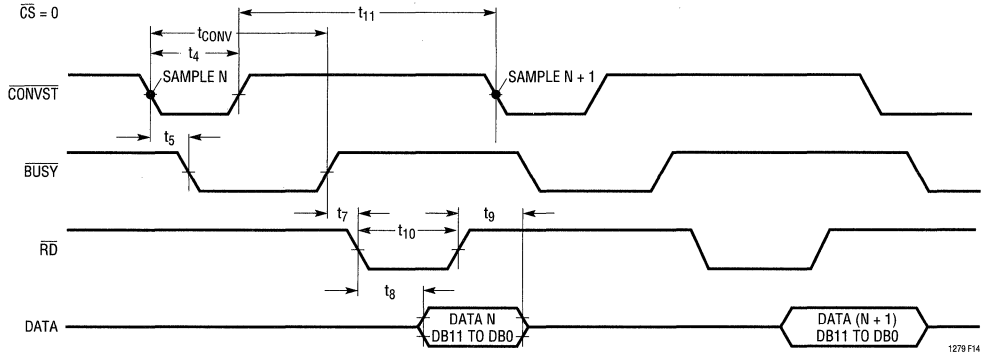


Figure 14. Mode 2. $\overline{CONVST}$ Starts a Conversion. Data is Read by $\overline{RD}$

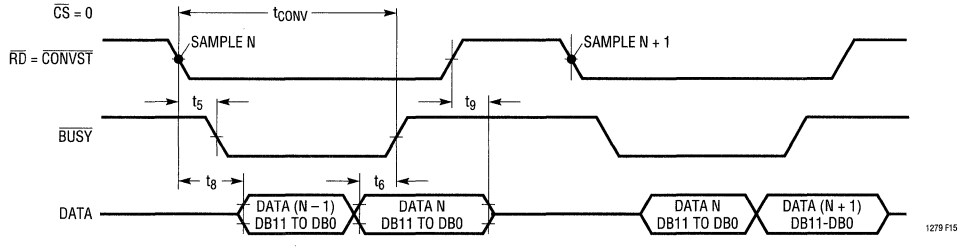


Figure 15. Slow Memory Mode

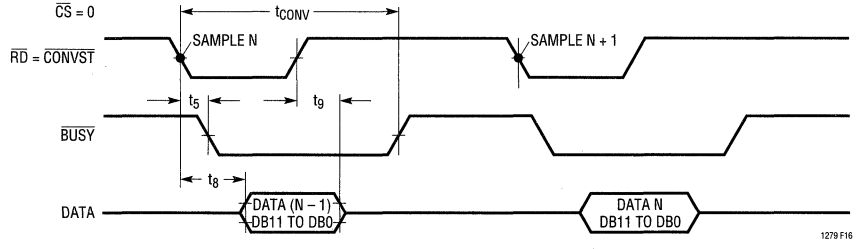


Figure 16. ROM Mode Timing

RELATED PARTS (12 Bit)

PART NUMBER	DESCRIPTION	COMMENTS
LTC1272	12-Bit, 3µs, 250kHz Sampling A/D Converter	Single 5V, Sampling 7572 Upgrade
LTC1273/LTC1275/LTC1276	12-Bit, 300ksps Sampling A/D Converters with Reference	Complete with Clock, Reference
LTC1274/LTC1277	12-Bit, 10mW, 100ksps A/D Converters with 1µA Shutdown	Complete with Clock, Reference
LTC1278	12-Bit, 500ksps Sampling A/D Converter with Shutdown	70dB SINAD at Nyquist, Low Power
LTC1282	3V, 140ksps 12-Bit Sampling A/D Converter with Reference	3V or ±3V ADC with Reference, Clock
LTC1409	12-Bit, 800ksps Sampling A/D Converter with Shutdown	Fast, Complete Low Power ADC
LTC1410	12-Bit, 1.25Msps Sampling A/D Converter with Shutdown	Fast, Complete, Wideband ADC

3V Micropower Sampling 12-Bit A/D Converters in SO-8 Packages

FEATURES

- **12-Bit Resolution**
- **8-Pin SO Plastic Package**
- **Low Cost**
- **Low Supply Current: 160μA Typ**
- Auto Shutdown to 1nA Typ
- Guaranteed ±3/4LSB Max DNL
- Single Supply 3V to 6V Operation
- Differential Inputs (LTC1285)
- 2-Channel MUX (LTC1288)
- On-Chip Sample-and-Hold
- 100μs Conversion Time
- Sampling Rates:
  7.5ksps (LTC1285)
  6.6ksps (LTC1288)
- I/O Compatible with SPI, Microwire, etc.

APPLICATIONS

- Pen Screen Digitizing
- Battery-Operated Systems
- Remote Data Acquisition
- Isolated Data Acquisition
- Battery Monitoring
- Temperature Measurement

DESCRIPTION

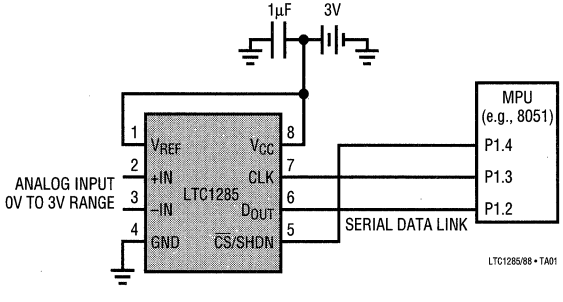
The LTC®1285/LTC1288 are 3V micropower, 12-bit, successive approximation sampling A/D converters. They typically draw only 160μA of supply current when converting and automatically power down to a typical supply current of 1nA whenever they are not performing conversions. They are packaged in 8-pin SO packages and operate on 3V to 6V supplies. These 12-bit, switched-capacitor, successive approximation ADCs include sample-and-holds. The LTC1285 has a single differential analog input. The LTC1288 offers a software selectable 2-channel MUX.

On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over three wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

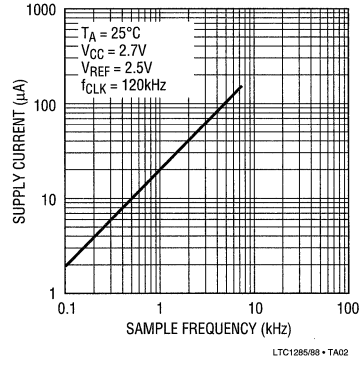
These circuits can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (to 1.5V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

TYPICAL APPLICATIONS

12μW, SO-8 Package, 12-Bit ADC
Samples at 200Hz and Runs Off a 3V Supply



Supply Current vs Sample Rate

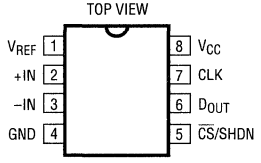


ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V
Voltage
  Analog and Reference ..... −0.3V to V_{CC} + 0.3V
  Digital Inputs ..... −0.3V to 12V
  Digital Output ..... −0.3V to V_{CC} + 0.3V

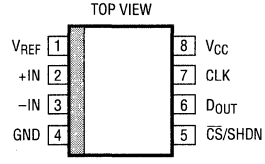
Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



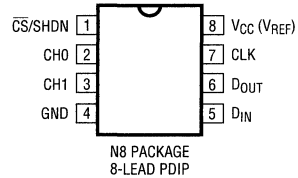
N8 PACKAGE
8-LEAD PDIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1285CN8



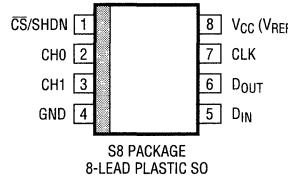
S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER
LTC1285CS8
PART MARKING
1285C



N8 PACKAGE
8-LEAD PDIP
T_{JMAX} = 150°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1288CN8



S8 PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER PART NUMBER
LTC1288CS8
PART MARKING
1288C

Consult factory for Industrial and Military grade parts.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage (Note 3)	LTC1285 LTC1288	2.7 2.7		6 6	V V
f_{CLK}	Clock Frequency	V_{CC} = 2.7V	(Note 4)		120	kHz
t_{CYC}	Total Cycle Time	LTC1285, f_{CLK} = 120kHz LTC1288, f_{CLK} = 120kHz	125.0 141.5			µs µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 2.7V	450			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	LTC1285, V_{CC} = 2.7V LTC1288, V_{CC} = 2.7V	2 2			µs µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 2.7V	600			ns
t_{WHCLK}	CLK High Time	V_{CC} = 2.7V	3.5			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 2.7V	3.5			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 2.7V	2			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	LTC1285, f_{CLK} = 120kHz LTC1288, f_{CLK} = 120kHz	123.0 139.5			µs µs

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		LTC1285 MIN	LTC1285 TYP	LTC1285 MAX	LTC1288 MIN	LTC1288 TYP	LTC1288 MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 6)	●		±3/4	±2		±3/4	±2	LSB
Differential Linearity Error		●		±1/4	±3/4		±1/4	±3/4	LSB
Offset Error		●		±3/4	±3		±3/4	±3	LSB
Gain Error		●		±2	±8		±2	±8	LSB
Analog Input Range	(Note 7 and 8)	●		−0.05V to V_{CC} + 0.05V					V
REF Input Range (LTC1285) (Notes 7, 8, and 9)	2.7 ≤ V_{CC} ≤ 6V			1.5V to V_{CC} + 0.05V					V V
Analog Input Leakage Current (Note 10)		●		±1				±1	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	2			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			−2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA V_{CC} = 2.7V, I_O = 360µA	● ●	2.4 2.1	2.64 2.30		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = High	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			−10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			15		mA
R_{REF}	Reference Input Resistance (LTC1285)	$\overline{CS}$ = V_{IH} $\overline{CS}$ = V_{IL}			2700 54		MΩ kΩ
I_{REF}	Reference Current (LTC1285)	$\overline{CS}$ = V_{CC} t_{CYC} ≥ 640µs, f_{CLK} ≤ 25kHz t_{CYC} = 134µs, f_{CLK} = 120kHz	● ●		0.001 50 50	2.5 70	µA µA µA
I_{CC}	Supply Current	$\overline{CS}$ = V_{CC}	●		0.001	±3.0	µA
		LTC1285, t_{CYC} ≥ 640µs, f_{CLK} ≤ 25kHz LTC1285, t_{CYC} = 134µs, f_{CLK} = 120kHz	 ●		150 160	 320	µA µA
		LTC1288, t_{CYC} ≥ 720µs, f_{CLK} ≤ 25kHz LTC1288, t_{CYC} = 150µs, f_{CLK} = 120kHz	 ●		200 210	 390	µA µA

DYNAMIC ACCURACY f_{SMPL} = 7.5kHz (LTC1285), f_{SMPL} = 6.6kHz (LTC1288) (Note 5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N +D)	Signal-to-Noise Plus Distortion Ratio	1kHz Input Signal		67		dB
THD	Total Harmonic Distortion (Up to 5th Harmonic)	1kHz Input Signal		−80		dB
SFDR	Spurious-Free Dynamic Range	1kHz Input Signal		88		dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal		−88		dB

AC CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			1.5		CLK Cycles
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	LTC1285 LTC1288	● ●	7.5 6.6			kHz kHz
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		600	1500	ns
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		220	660	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enable	See Test Circuits	●		180	500	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			520		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		60	180	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		80	180	ns
C_{IN}	Input Capacitance	Analog Inputs, On Channel Analog Inputs, Off Channel Digital Input			20 5 5		pF pF pF

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: These devices are specified at 3V. For 5V specified devices, see LTC1286 and LTC1298.

Note 4: Increased leakage currents at elevated temperatures cause the sample-and-hold to droop, therefore it is recommended that $f_{CLK} \geq 75kHz$ at 70° and $f_{CLK} \geq 1kHz$ at 25°C.

Note 5: V_{CC} = 2.7V, V_{REF} = 2.5V and CLK = 120kHz unless otherwise specified.

Note 6: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. This spec allows 50mV forward bias of either diode for $2.7V \leq V_{CC} \leq 6V$. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV the output code will be correct. To achieve an absolute 0V to 2.7V input voltage range will therefore require a minimum supply voltage of 2.650V over initial tolerance, temperature variations and loading. For $2.7V < V_{CC} \leq 6V$, reference and analog input range cannot exceed 6.05V. If reference and analog input range are greater than 6.05V, the output code will not be guaranteed to be correct.

Note 8: The supply voltage range for the LTC1285 and the LTC1288 is from 2.7V to 6V.

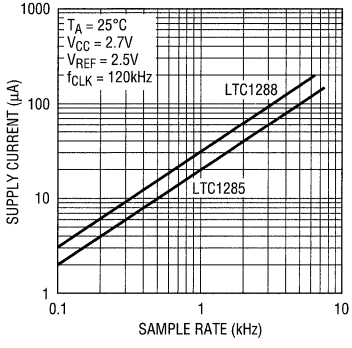
Note 9: Recommended operating conditions

Note 10: Channel leakage current is measured after the channel selection.

6

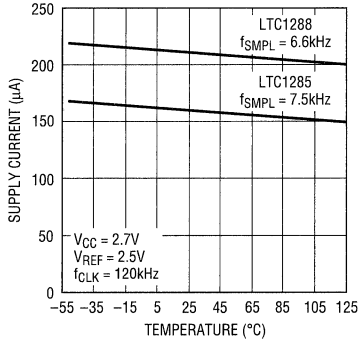
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Sample Rate



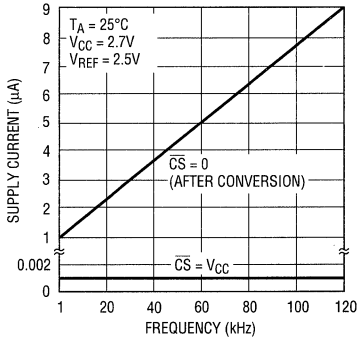
LTC1285/88 • TPC01

Supply Current vs Temperature



LTC1285/88 • TPC02

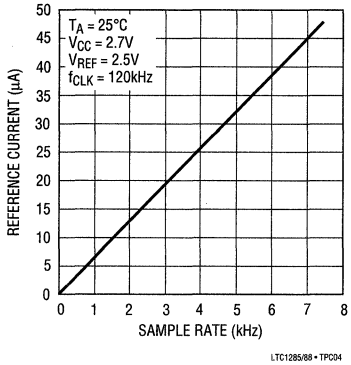
Shutdown Supply Current vs Clock Rate with $\overline{CS}$ High and $\overline{CS}$ Low



LTC1285/88 • TPC03

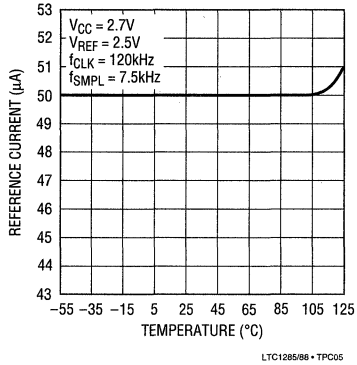
TYPICAL PERFORMANCE CHARACTERISTICS

Reference Current vs Sample Rate (LTC1285)



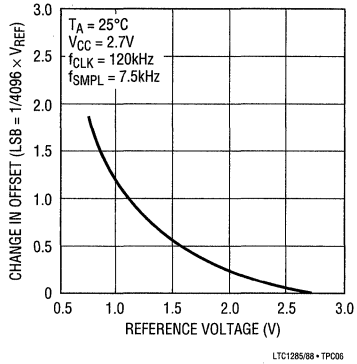
LTC1285/88 • TPC04

Reference Current vs Temperature



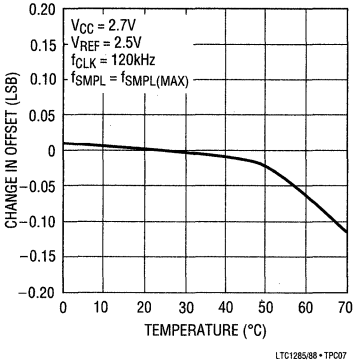
LTC1285/88 • TPC05

Change in Offset vs Reference Voltage



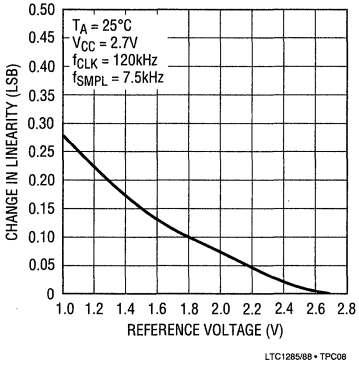
LTC1285/88 • TPC06

Change in Offset vs Temperature



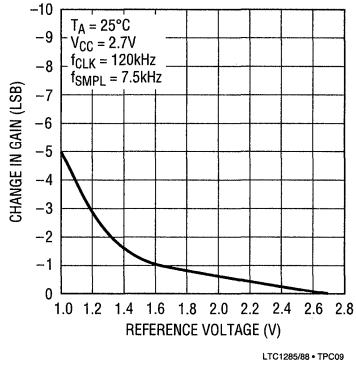
LTC1285/88 • TPC07

Change in Linearity vs Reference Voltage



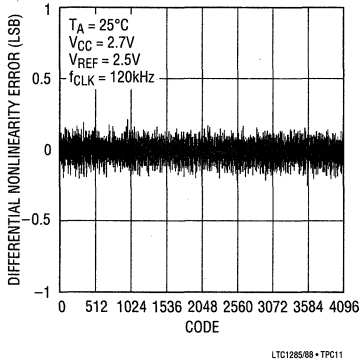
LTC1285/88 • TPC08

Change in Gain vs Reference Voltage



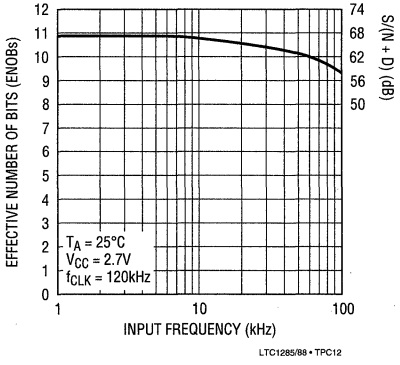
LTC1285/88 • TPC09

Differential Nonlinearity vs Code



LTC1285/88 • TPC11

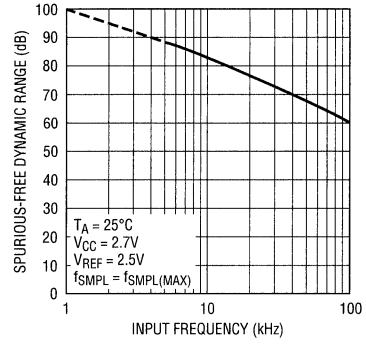
Effective Bits and S/(N + D) vs Input Frequency



LTC1285/88 • TPC12

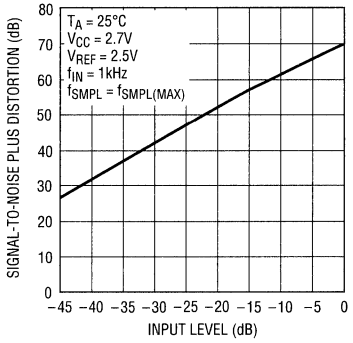
TYPICAL PERFORMANCE CHARACTERISTICS

Spurious-Free Dynamic Range vs Input Frequency



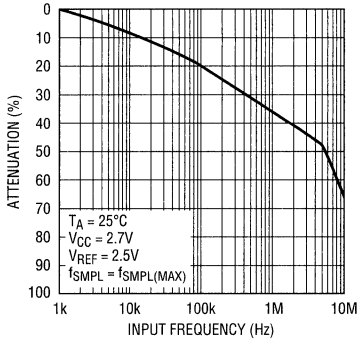
LTC1285/88 • G13

S/(N + D) vs Input Level



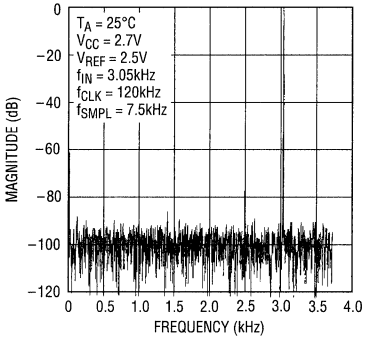
LTC1285/88 • TPC14

Attenuation vs Input Frequency



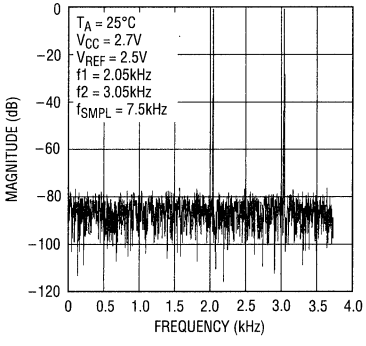
LTC1285/86 • TPC15

4096 Point FFT Plot



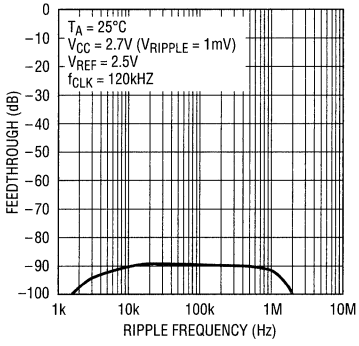
LTC1285/88 • TPC16

Intermodulation Distortion



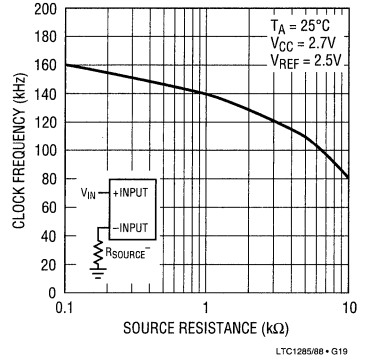
LTC1285/88 • TPC17

Power Supply Feedthrough vs Ripple Frequency



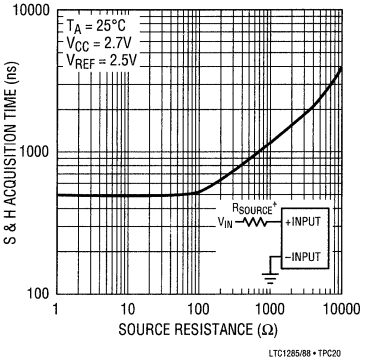
LTC1285/86 • TPC18

Maximum Clock Frequency vs Source Resistance



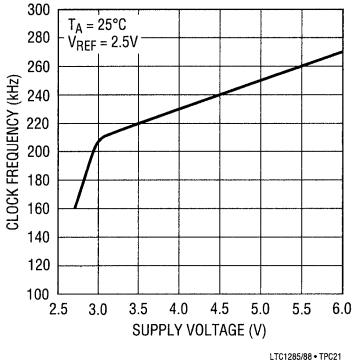
LTC1285/88 • G19

Sample-and-Hold Acquisition Time vs Source Resistance



LTC1285/88 • TPC20

Maximum Clock Frequency vs Supply Voltage

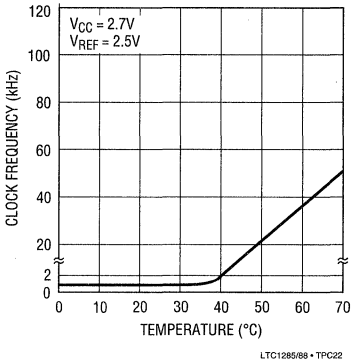


LTC1285/88 • TPC21

6

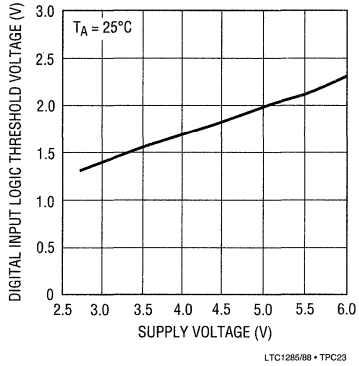
TYPICAL PERFORMANCE CHARACTERISTICS

Minimum Clock Frequency for 0.1 LSB Error vs Temperature



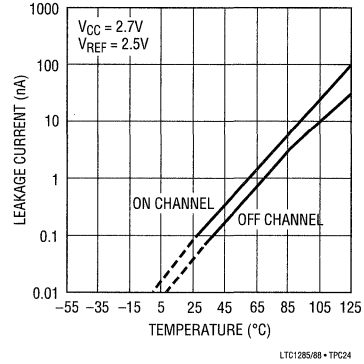
LTC1285/88 • TPC22

Digital Input Logic Threshold vs Supply Voltage



LTC1285/88 • TPC23

Input Channel Leakage Current vs Temperature



LTC1285/88 • TPC24

PIN FUNCTIONS

LTC1285

V_{REF} (Pin 1): Reference Input. The reference input defines the span of the A/D converter.

IN^+ (Pin 2): Positive Analog Input.

IN^- (Pin 3): Negative Analog Input.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

$\overline{CS}$/SHDN (Pin 5): Chip Select Input. A logic low on this input enables the LTC1285. A logic high on this input disables and powers down the LTC1285.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer and determines conversion speed.

V_{CC} (Pin 8): Power Supply Voltage. This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1288

$\overline{CS}$/SHDN (Pin 1): Chip Select Input. A logic low on this input enables the LTC1288. A logic high on this input disables and powers down the LTC1288.

CH0 (Pin 2): Analog Input.

CH1 (Pin 3): Analog Input.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

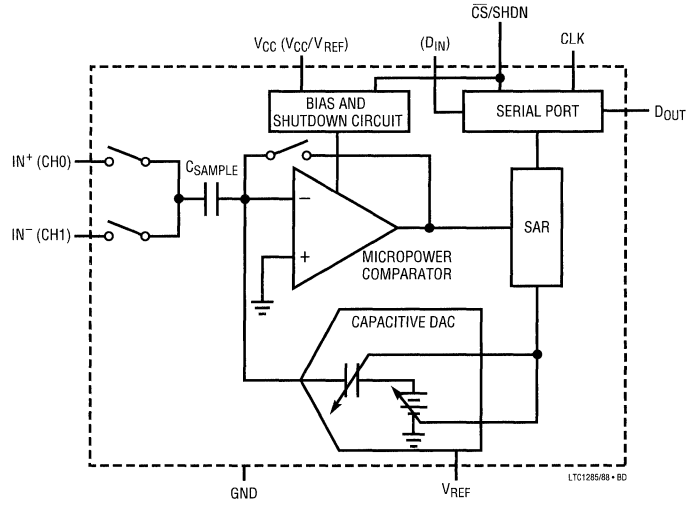
D_{IN} (Pin 5): Digital Data Input. The multiplexer address is shifted into this input.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer and determines conversion speed.

V_{CC}/V_{REF} (Pin 8): Power Supply and Reference Voltage. This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

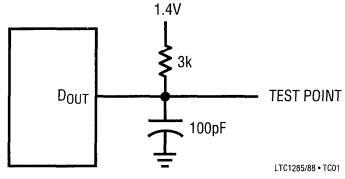


PIN NAMES IN PARENTHESES REFER TO THE LTC1288

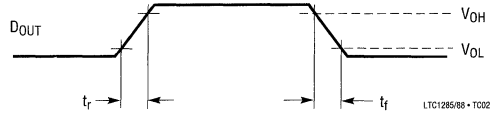
TEST CIRCUITS

6

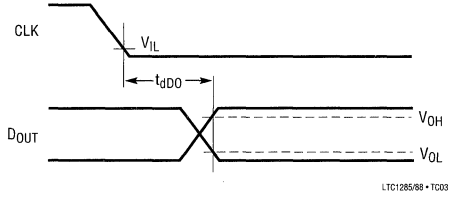
Load Circuit for t_{dDO}, t_r and t_f



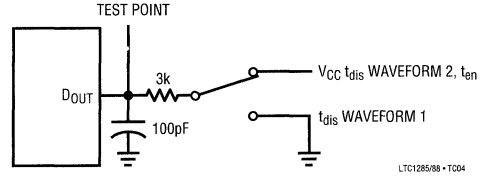
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}

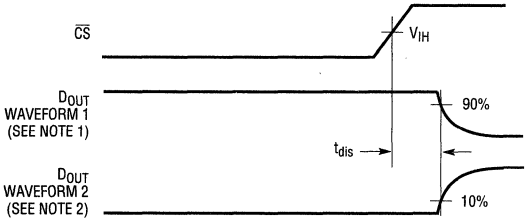


Load Circuit for t_{dis} and t_{en}



TEST CIRCUITS

Voltage Waveforms for t_{dis}

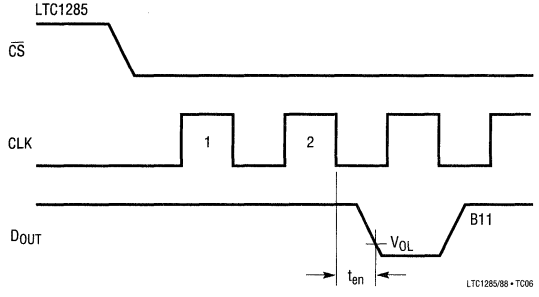


NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

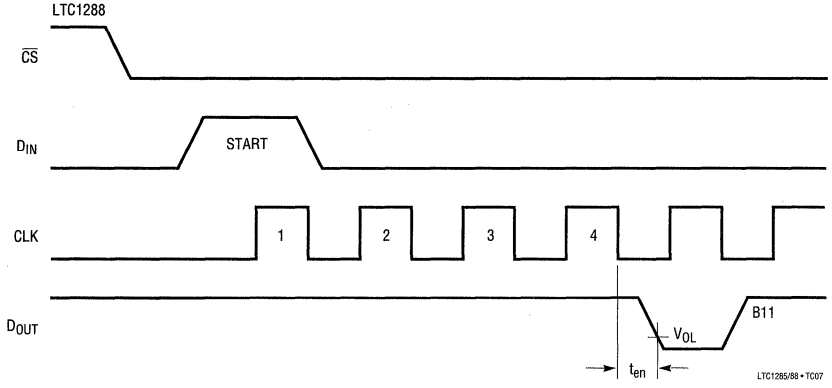
LTC1285/88 • TC05

Voltage Waveforms for t_{en}



LTC1285/88 • TC06

Voltage Waveforms for t_{en}



LTC1285/88 • TC07

APPLICATION INFORMATION

OVERVIEW

The LTC1285 and LTC1288 are 3V micropower, 12-bit, successive approximation sampling A/D converters. The LTC1285 typically draws 160µA of supply current when sampling at 7.5kHz while the LTC1288 nominally consumes 210µA of supply current when sampling at 6.6 kHz. The extra 50µA of supply current on the LTC1288 comes from the reference input which is intentionally tied to the supply. Supply current drops linearly as the sample rate is reduced (see Supply Current vs Sample Rate). The ADCs automatically power down when not performing conversions, drawing only leakage current. They are packaged in 8-pin SO and DIP packages. The LTC1285 and LTC1288 operate on a single supply from 2.7V to 6V.

Both the LTC1285 and the LTC1288 contain a 12-bit, switched-capacitor ADC, a sample-and-hold, and a serial port (see Block Diagram). Although they share the same basic design, the LTC1285 and LTC1288 differ in some respects. The LTC1285 has a differential input and has an external reference input pin. It can measure signals floating on a DC common-mode voltage and can operate with reduced spans to 1.5V. Reducing the spans allows it to achieve 366µV resolution. The LTC1288 has a two-channel input multiplexer and can convert either channel with respect to ground or the difference between the two. The reference input is tied to the supply pin.

SERIAL INTERFACE

The 2-channel LTC1288 communicates with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface. The single channel LTC1285 uses a 3-wire interface (see Operating Sequence in Figures 1 and 2).

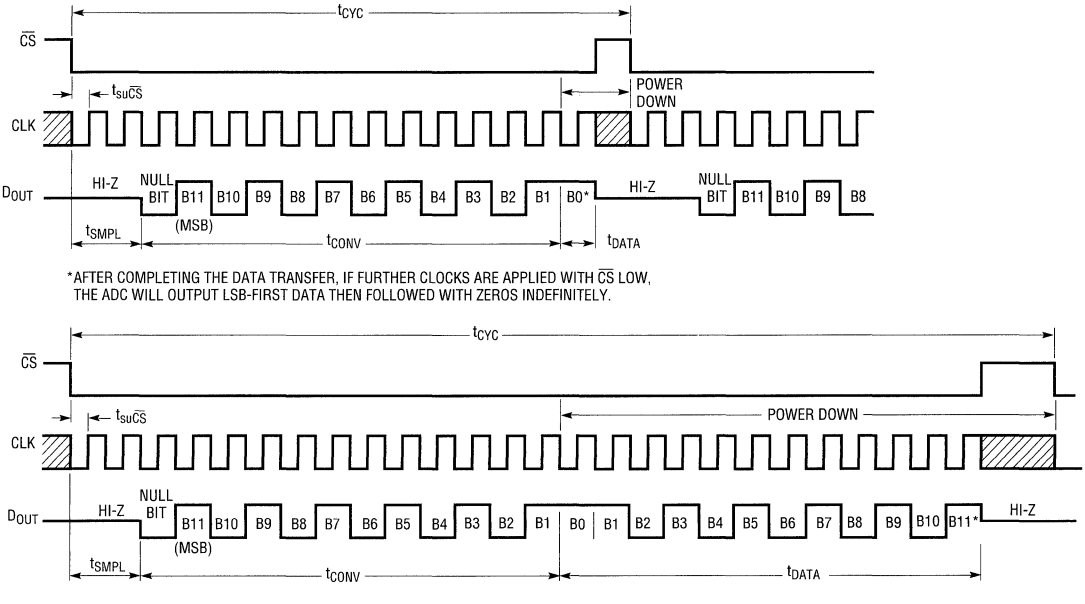
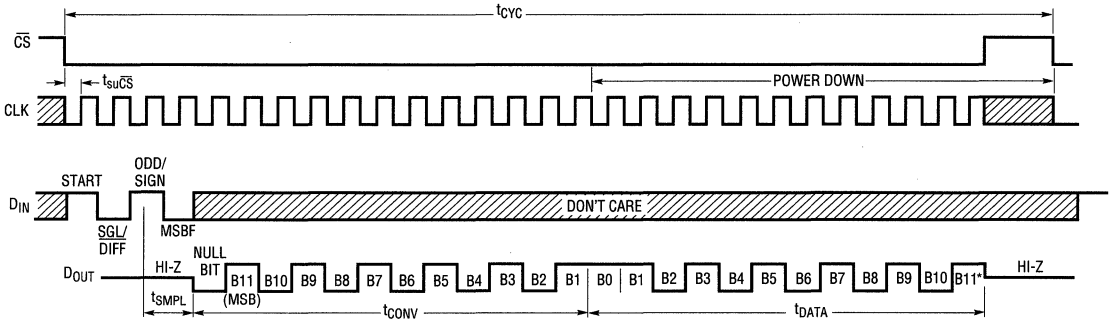


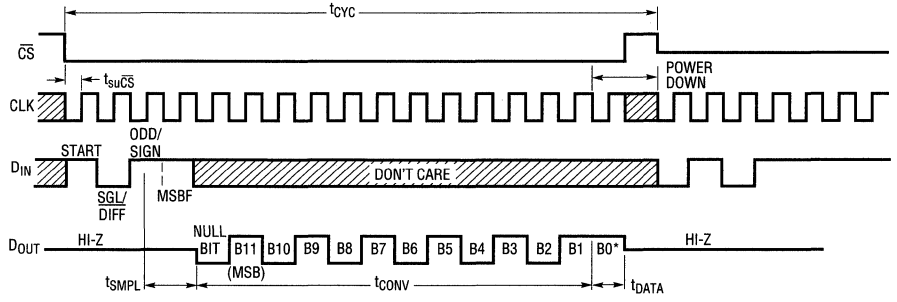
Figure 1. LTC1285 Operating Sequence

APPLICATION INFORMATION

MSB-First Data (MSBF = 0)



MSB-First Data (MSBF = 1)



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY.

t_{DATA}: DURING THIS TIME, THE BIAS CIRCUIT AND THE COMPARATOR POWER DOWN AND THE REFERENCE INPUT BECOMES A HIGH IMPEDANCE NODE, LEAVING THE CLK RUNNING TO CLOCK OUT LSB-FIRST DATA OR ZEROES.

LTC1285/88 • F02

Figure 2. LTC1288 Operating Sequence Example: Differential Inputs (CH^+, CH^-)

APPLICATION INFORMATION

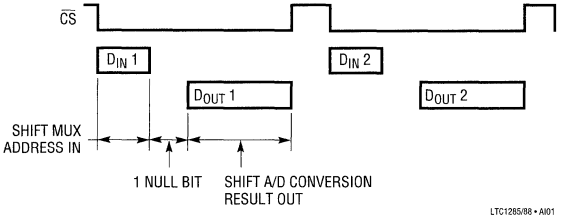
Data Transfer

The CLK synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems.

The LTC1285 does not require a configuration input word and has no D_{IN} pin. A falling $\overline{CS}$ initiates data transfer as shown in the LTC1285 operating sequence. After $\overline{CS}$ falls the second CLK pulse enables D_{OUT}. After one null bit the A/D conversion result is output on the D_{OUT} line. Bringing $\overline{CS}$ high resets the LTC1285 for the next data exchange.

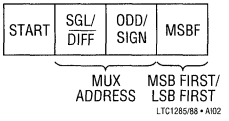
The LTC1288 first receives input data and then transmits back the A/D conversion result (half duplex). Because of the half duplex operation, D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1288 looks for a start bit. After the start bit is received, the 3-bit input word is shifted into the D_{IN} input which configures the LTC1288 and starts the conversion. After one null bit, the result of the conversion is output on the D_{OUT} line. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1288 in preparation for the next data exchange.



Input Data Word

The LTC1285 requires no D_{IN} word. It is permanently configured to have a single differential input. The conversion result appears on the D_{OUT} line. The data format is MSB first followed by the LSB sequence. This provides easy interface to MSB or LSB first serial ports. For MSB first data the $\overline{CS}$ signal can be taken high after B0 (see Figure 1). The LTC1288 clocks data into the D_{IN} input on the rising edge of the clock. The input data words are defined as follows:



Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1288 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following tables. In single-ended mode, all input channels are measured with respect to GND.

LTC1288 Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/DIFF	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

LTC1285/88 • AI03

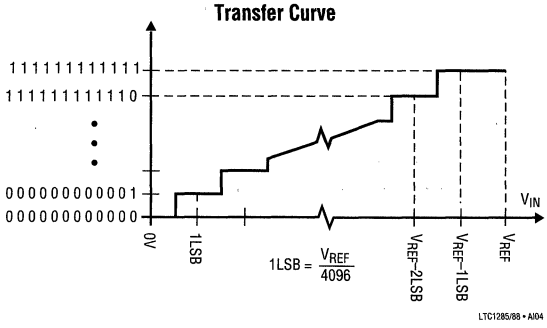
MSB First/LSB First (MSBF)

The output data of the LTC1288 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB first format. Logical zeros will be filled in indefinitely following the last data bit. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the D_{OUT} line (see Operating Sequence).

APPLICATION INFORMATION

Transfer Curve

The LTC1285/LTC1288 are permanently configured for unipolar only. The input span and code assignment for this conversion type are shown in the following figures.



Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5.000V)
111111111111111	V_{REF} – 1LSB	4.99878V
111111111111110	V_{REF} – 2LSB	4.99756V
•	•	•
•	•	•
•	•	•
000000000000001	1LSB	0.00122V
000000000000000	0V	0V

LTC1285/88 • AI05

Operation with D_{IN} and D_{OUT} Tied Together

The LTC1288 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the microprocessor (MPU). Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1288 will take control of the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 3). Therefore the processor port line must be switched to an input before this happens to avoid a conflict.

In the Typical Applications section, there is an example of interfacing the LTC1288 with D_{IN} and D_{OUT} tied together to the Intel 8051 MPU.

ACHIEVING MICROPOWER PERFORMANCE

With typical operating currents of 160µA and automatic shutdown between conversions, the LTC1285/LTC1288 achieves extremely low power consumption over a wide range of sample rates (see Figure 4). The auto-shutdown allows the supply curve to drop with reduced sample rate.

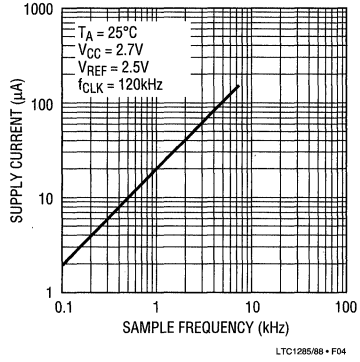


Figure 4. Automatic Power Shutdown Between Conversions Allows Power Consumption to Drop with Sample Rate

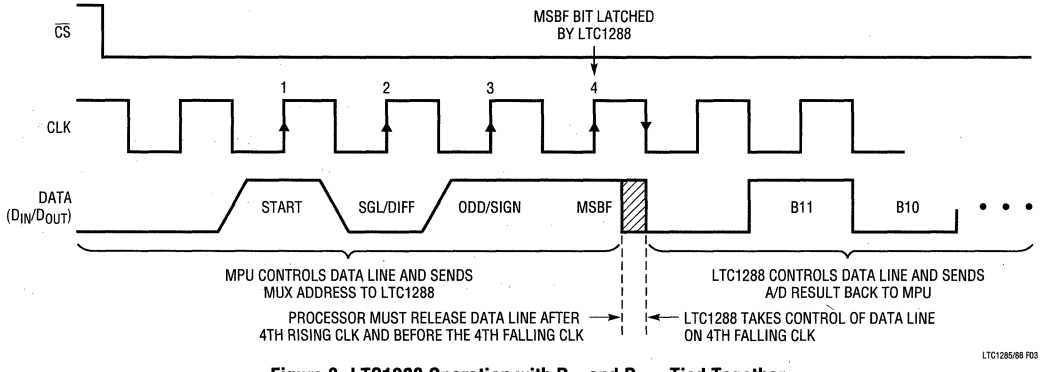


Figure 3. LTC1288 Operation with D_{IN} and D_{OUT} Tied Together

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Several things must be taken into account to achieve such a low power consumption.

Shutdown

The LTC1285/LTC1288 are equipped with automatic shutdown features. They draw power when the $\overline{CS}$ pin is low and shut down completely when that pin is high. The bias circuit and comparator powers down and the reference input becomes high impedance at the end of each conversion leaving the CLK running to clock out the LSB first data or zeroes (see Figures 1 and 2). If the $\overline{CS}$ is not running rail-to-rail, the input logic buffer will draw current. This current may be large compared to the typical supply current. To obtain the lowest supply current, bring the $\overline{CS}$ pin to ground when it is low and to supply voltage when it is high.

When the $\overline{CS}$ pin is high (= supply voltage), the converter is in shutdown mode and draws only leakage current. The status of the D_{IN} and CLK input have no effect on supply current during this time. There is no need to stop D_{IN} and CLK with $\overline{CS}$ = high; they can continue to run without drawing current.

Minimize $\overline{CS}$ Low Time

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{CS}$ low time. Bringing $\overline{CS}$ low, transferring data as quickly as possible, and then bringing it back high will result in the lowest current drain. This minimizes the amount of time the device draws power. After a conversion the ADC automatically shuts down even if $\overline{CS}$ is held low (see Figures 1 and 2). If the clock is left running to clock out LSB-data or zero, the logic will draw a small current. Figure 5 shows that the typical supply current with $\overline{CS}$ = ground varies from 1μA at 1kHz to 9μA at 120kHz. When $\overline{CS}$ = V_{CC}, the logic is gated off and no supply current is drawn regardless of the clock frequency.

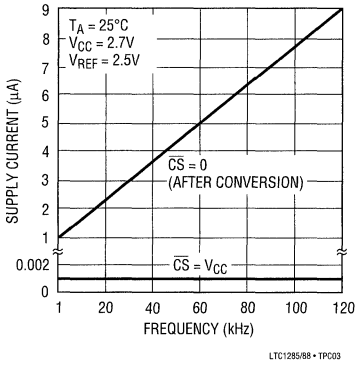


Figure 5. Shutdown Current with $\overline{CS}$ High is 1nA Typically, Regardless of the Clock. Shutdown Current with $\overline{CS}$ = Ground Varies From 1μA at 1kHz to 9μA at 120kHz

D_{OUT} Loading

Capacitive loading on the digital output can increase power consumption. A 100pF capacitor on the D_{OUT} pin can add more than 16.2μA to the supply current at a 120kHz clock frequency. An extra 16.2μA or so of current goes into charging and discharging the load capacitor. The same goes for digital lines driven at a high frequency by any logic. The C × V × f currents must be evaluated and the troublesome ones minimized.

OPERATING ON OTHER THAN 3V SUPPLIES

Both the LTC1285 and the LTC1288 operate from a 2.7V to 6V supply. To operate the LTC1285/LTC1288 on other than 3V supplies a few things must be kept in mind.

Input Logic Levels

The input logic levels of $\overline{CS}$, CLK and D_{IN} are made to meet TTL on a 3V supply. When the supply voltage varies, the input logic levels also change. For the LTC1285/LTC1288 to sample and convert correctly, the digital inputs have to be in the proper logical low and high levels relative to the operating supply voltage (see typical curve of Digital Input Logic Threshold vs Supply Voltage). If achieving micropower consumption is desirable, the digital inputs must go rail-to-rail between supply voltage and ground (see ACHIEVING MICROPOWER PERFORMANCE section).

Clock Frequency

The maximum recommended clock frequency is 120kHz for the LTC1285/LTC1288 running off a 3V supply. With the supply voltage changing, the maximum clock frequency for the devices also changes (see the typical curve

APPLICATION INFORMATION

of Maximum Clock Rate vs Supply Voltage). If the maximum clock frequency is used, care must be taken to ensure that the device converts correctly.

Mixed Supplies

It is possible to have a microprocessor running off a 5V supply and communicate with the LTC1285/LTC1288 operating on a 3V supply. The inputs of $\overline{CS}$, CLK and D_{IN} of the LTC1285/LTC1288 have no problem to take a voltage swing from 0V to 5V. With the LTC1285 operating on a 3V supply, the output of D_{OUT} may only go between 0V and 3V. The 3V output level is higher enough to trip a TTL input of the MPU. Figure 6 shows a 3V powered LTC1285 interfacing a 5V system.

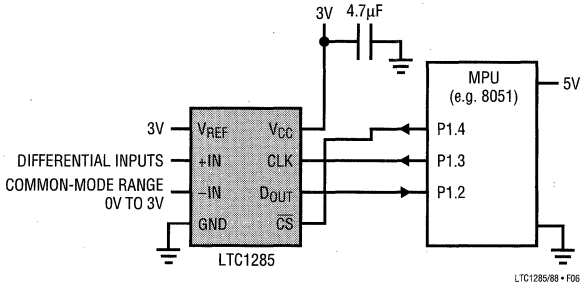


Figure 6. Interfacing a 3V Powered LTC1285 to a 5V System

BOARD LAYOUT CONSIDERATIONS

Grounding and Bypassing

The LTC1285/LTC1288 are easy to use if some care is taken. They should be used with an analog ground plane and single point grounding techniques. The GND pin should be tied directly to the ground plane.

The V_{CC} pin should be bypassed to the ground plane with a 10µF tantalum capacitor with leads as short as possible. If the power supply is clean, the LTC1285/LTC1288 can also operate with smaller 1µF or less surface mount or ceramic bypass capacitors. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

SAMPLE-AND-HOLD

Both the LTC1285 and the LTC1288 provide a built-in sample-and-hold (S&H) function to acquire signals. The S&H of the LTC1285 acquires input signals from "+" input relative to "–" input during the t_{SMPL} time (see Figure 1). However, the S&H of the LTC1288 can sample input signals in the single-ended mode or in the differential inputs during the t_{SMPL} time (see Figure 7).

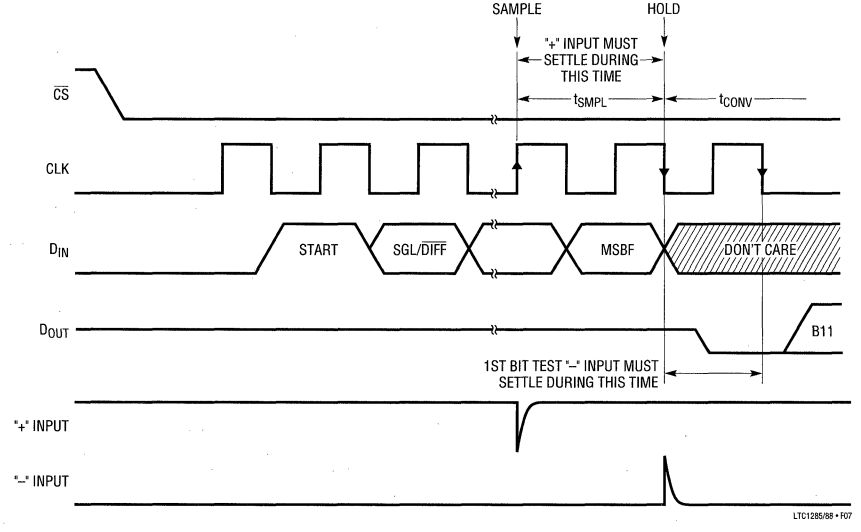


Figure 7. LTC1288 "+" and "–" Input Settling Windows

APPLICATION INFORMATION

Single-Ended Inputs

The sample-and-hold of the LTC1288 allows conversion of rapidly varying signals. The input voltage is sampled during the t_{SMPL} time as shown in Figure 7. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling CLK edge after the MSBF bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

Differential Inputs

With differential inputs, the ADC no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 12 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \times 2 \times \pi \times f(\text{"}-\text{"}) \times 12/f_{CLK}$$

Where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. In most cases V_{ERROR} will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (152μV) with the converter running at CLK = 120kHz, its peak value would have to be 4.03mV.

ANALOG INPUTS

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1285/LTC1288 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

"+" Input Settling

The input capacitor of the LTC1285 is switched onto "+" input during the t_{SMPL} time (see Figure 1) and samples the input signal within that time. However, the input capacitor of the LTC1288 is switched onto "+" input during the sample phase (t_{SMPL}, see Figure 7). The sample phase is 1 1/2 CLK cycles before conversion starts. The voltage on the "+" input must settle completely within t_{SMPLE} for the LTC1285 and the LTC1288 respectively. Minimizing R_{SOURCE}^+ and C1 will improve the input settling time. If a large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency.

"–" Input Settling

At the end of the t_{SMPL}, the input capacitor switches to the "–" input and conversion starts (see Figures 1 and 7). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage settles completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- and C2 will improve settling time. If a large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 7). Again, the"+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps, including the LT1006 and LT1413 single supply op amps, can be made to settle well even with the minimum settling windows of 12.5μs ("+" input) which occur at the maximum clock rate of 120kHz.

Source Resistance

The analog inputs of the LTC1285/LTC1288 look like a 20pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}) as shown in Figure 8. C_{IN} gets switched between the

APPLICATION INFORMATION

selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

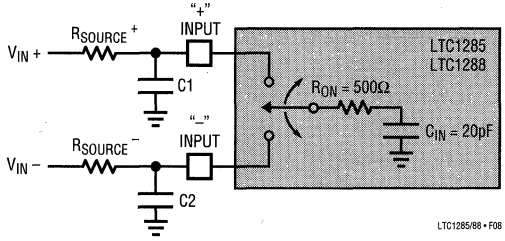


Figure 8. Analog Input Equivalent Circuit

RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 9. For large values of C_F (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 20pF \times V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 133.3µs, the input current equals 0.375µA at V_{IN} = 2.5V. In this case, a filter resistor of 160Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time.

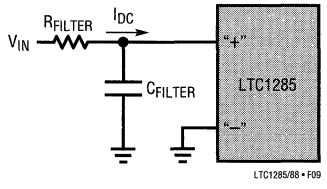


Figure 9. RC Input Filtering

Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 240Ω will cause a voltage drop of 240µV or 0.4LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

REFERENCE INPUTS

The reference input of the LTC1285 is effectively a 50kΩ resistor from the time $\overline{CS}$ goes low to the end of the conversion. The reference input becomes a high impedence node at any other time (see Figure 10). Since the voltage on the reference input defines the voltage span of the A/D converter, the reference input should be driven by a reference with low R_{OUT} (ex. LT1004, LT1019 and LT1021) or a voltage source with low R_{OUT}.

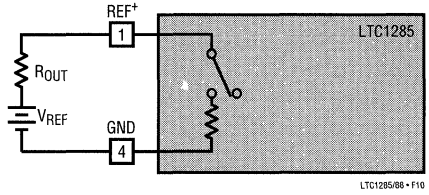


Figure 10. Reference Input Equivalent Circuit

Reduced Reference Operation

The minimum reference voltage of the LTC1288 is limited to 2.7V because the V_{CC} supply and reference are internally tied together. However, the LTC1285 can operate with reference voltages below 1.5V.

The effective resolution of the LTC1285 can be increased by reducing the input span of the converter. The LTC1285 exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Change in Linearity vs Reference Voltage and Change in Gain vs Reference

APPLICATION INFORMATION

Voltage). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values:

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

Offset with Reduced V_{REF}

The offset of the LTC1285 has a larger effect on the output code. When the ADC is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Change in Offset vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 122µV which is 0.2LSB with a 2.5V reference becomes 1LSB with a 1V reference and 5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input of the LTC1285.

Noise with Reduced V_{REF}

The total input referred noise of the LTC1285 can be reduced to approximately 400µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 2.5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 2.5V reference, the 400µV noise is only 0.66LSB peak-to-peak. In this case, the LTC1285 noise will contribute a little bit of uncertainty to the output code. However, for reduced references the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference this same 400µV noise is 1.32LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 1LSB. If the reference is further reduced to 1V, the 400µV noise becomes equal to 3.3LSBs and a stable code may be difficult to achieve. In this case averaging multiple readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage to be used the more critical it becomes to have a clean, noise free setup.

Conversion Speed with Reduced V_{REF}

With reduced reference voltages, the LSB step size is reduced and the LTC1285 internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low values of V_{REF} are used.

DYNAMIC PERFORMANCE

The LTC1285/LTC1288 have exceptional sampling capability. Fast Fourier Transform (FFT) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 11 shows a typical LTC1285 plot.

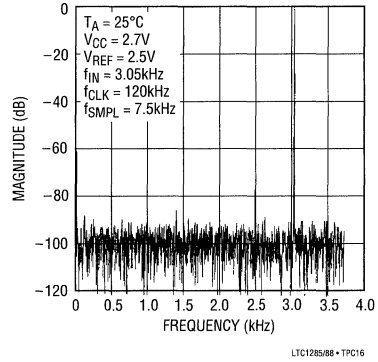


Figure 11. LTC1285 Non-Averaged, 4096 Point FFT Plot

APPLICATION INFORMATION

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio (S/N + D) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the ADC's output. The output is band limited to frequencies above DC and below one half the sampling frequency. Figure 12 shows a typical spectral content with a 7.5kHz sampling rate.

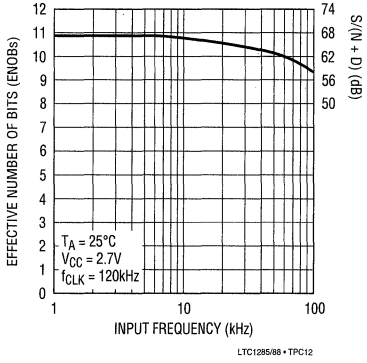


Figure 12. Effective Bits and S/(N + D) vs Input Frequency

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to S/(N+D) by the equation:

$$ENOB = [S/(N + D) - 1.76]/6.02$$

where S/(N + D) is expressed in dB. At the maximum sampling rate of 7.5kHz with a 2.7V supply, the LTC1285 maintains above 10.7 ENOBs at 10kHz input frequency. Above 10kHz the ENOBs gradually decline, as shown in Figure 12, due to increasing second harmonic distortion. The noise floor remains low.

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half of the sampling frequency. THD is defined as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + ... + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through the N^{th} harmonics. The typical THD specification in the Dynamic Accuracy table includes the 2nd through 5th harmonics. With a 1kHz input signal, the LTC1285/LTC1288 have typical THD of 80dB with V_{CC} = 2.7V.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include $(f_a + f_b)$ and $(f_a - f_b)$ while 3rd order IMD terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$. If the two input sine waves are equal in magnitudes, the value (in dB) of the 2nd order IMD products can be expressed by the following formula:

$$IMD(f_a \pm f_b) = 20\log\left[\frac{\text{amplitude}\,(f_a \pm f_b)}{\text{amplitude at } f_a}\right]$$

For input frequencies of 2.05kHz and 3.05kHz, the IMD of the LTC1285/LTC1288 is 72dB with a 2.7V supply.

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in dBs relative to the RMS value of a full-scale input signal.

TYPICAL APPLICATIONS

MICROPROCESSOR INTERFACES

The LTC1285/LTC1288 can interface directly without external hardware to most popular microprocessor (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then 3 or 4 of the MPU's parallel port lines can be programmed to form the serial link to the LTC1285/LTC1288. Included here is one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC11)

The MC68HC11 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB-first and in 8-bit increments. The D_{IN} word sent to the data register starts with the SPI process. With three 8-bit transfers, the A/D result is read into the MPU. The second 8-bit transfer clocks B11 through B8 of the A/D conversion result into the processor. The third 8-bit transfer clocks the remaining bits, B7 through B0, into the MPU. The data is right justified into two memory locations. ANDing the second byte with OF_{HEX} clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

MC68HC11 Code

In this example the D_{IN} word configures the input MUX for a single-ended input to be applied to CH0. The conversion result is output MSB-first.

Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1286/LTC1298

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2,S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD63705	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	CSI/O
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MICROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS†
HPC16000 Family	MICROWIRE/PLUS†
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020	Serial Port
Intel	
8051	Bit Manipulation on Parallel Port

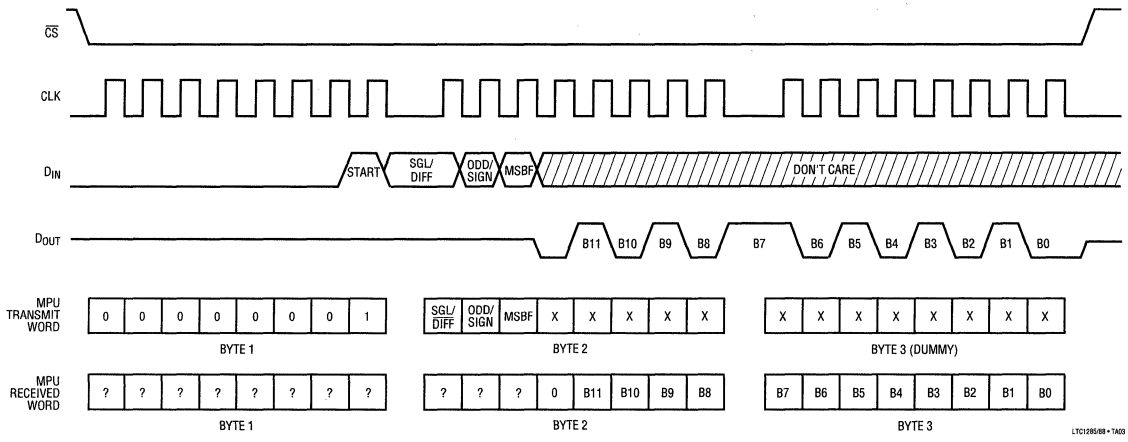
* Requires external hardware

† MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

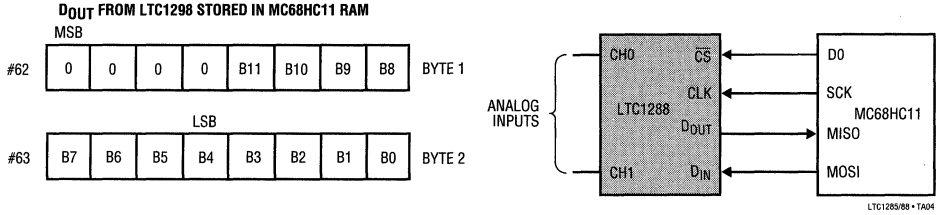
6

TYPICAL APPLICATIONS

Timing Diagram for Interface to the MC68HC11



Hardware and Software Interface to the MC68HC11



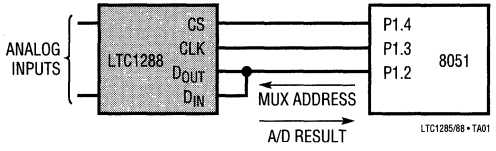
LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR	WAIT1	BPL	WAIT1	CHECK IF TRANSFER IS DONE
	STAA	$1028	LOAD DATA INTO SPCR ($1028)		LDAA	$51	LOAD DIN INTO ACC A FROM $51
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR		STAA	$102A	LOAD DIN INTO SPI, START SCK
	STAA	$1009	LOAD DATA INTO PORT D DDR	WAIT2	LDAA	$1029	CHECK SPI STATUS REG
	LDAA	#$01	LOAD DIN WORD INTO ACC A		BPL	WAIT2	CHECK IF TRANSFER IS DONE
	STAA	$50	LOAD DIN DATA INTO $50		LDAA	$102A	LOAD LTC1288 MSBs INTO ACC A
	LDAA	#$A0	LOAD DIN WORD INTO ACC A		STAA	$62	STORE MSBs IN $62
	STAA	$51	LOAD DIN DATA INTO $51		LDAA	$52	LOAD DUMMY INTO ACC A FROM $52
	LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A		STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
	STAA	$52	LOAD DUMMY DIN DATA INTO $52				
	LDX	#$1000	LOAD INDEX REGISTER X WITH $1000	WAIT3	LDAA	$1029	CHECK SPI STATUS REG
					BPL	WAIT3	CHECK IF TRANSFER IS DONE
LOOP	BCLR	$08,X,#$01	DO GOES LOW (CS GOES LOW)		BSET	$08,X#$01	DO GOES HIGH (CS GOES HIGH)
	LDAA	$50	LOAD DIN INTO ACC A FROM $50		LDAA	$102A	LOAD LTC1288 LSBs IN ACC
	STAA	$102A	LOAD DIN INTO SPI, START SCK		STAA	$63	STORE LSBs IN $63
	LDAA	$1029	CHECK SPI STATUS REG		JMP	LOOP	START NEXT CONVERSION

TYPICAL APPLICATIONS

Interfacing to the Parallel Port of the INTEL 8051 Family

The Intel 8051 has been chosen to demonstrate the interface between the LTC1288 and parallel port microprocessors. Normally the $\overline{CS}$, CLK and D_{IN} signals would be generated on 3 port lines and the D_{OUT} signal read on a 4th port line. This works very well. However, we will demonstrate here an interface with the D_{IN} and D_{OUT} of the LTC1288 tied together as described in the SERIAL INTERFACE section. This saves one wire.

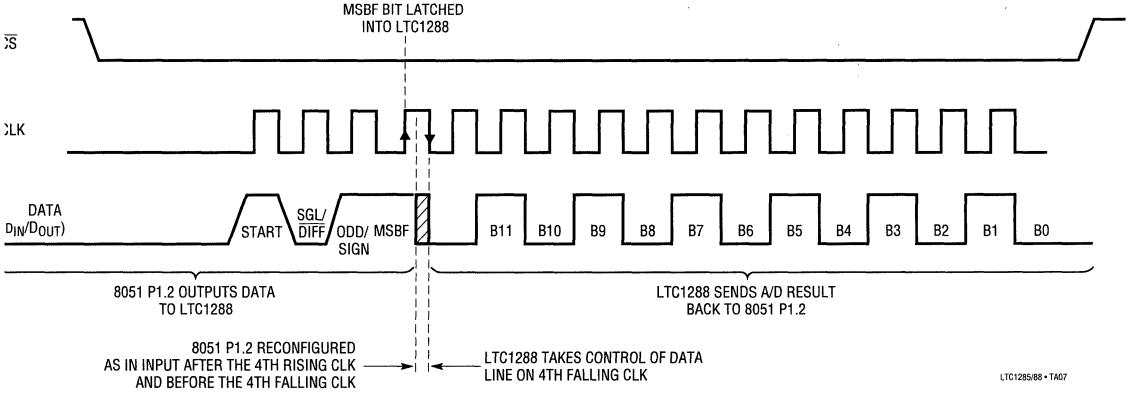
The 8051 first sends the start bit and MUX address to the LTC1288 over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 12-bit A/D result over the same data line.



LABEL	MNEMONIC	OPERAND	COMMENTS
	MOV	A, #FFH	D_{IN} word for LTC1288
	SETB	P1.4	Make sure $\overline{CS}$ is high
	CLR	P1.4	$\overline{CS}$ goes low
	MOV	R4, #04	Load counter
LOOP 1	RLC	A	Rotate D_{IN} bit into Carry
	CLR	P1.3	SCLK goes low
	MOV	P1.2, C	Output D_{IN} bit to LTC1288
	SETB	P1.3	SCLK goes high
	DJNZ	R4, LOOP 1	Next bit
	MOV	P1, #04	Bit 2 becomes an input
	CLR	P1.3	SCLK goes low
	MOV	R4, #09	Load counter
LOOP 2	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	DJNZ	R4, LOOP 2	Next bit
	MOV	R2, A	Store MSBs in R2
	CLR	A	Clear Acc.
	MOV	R4, #04	Load counter
LOOP 3	MOV	C, P1.2	Read data bit into Carry
	RLC	A	Rotate data bit into Acc.
	SETB	P1.3	SCLK goes high
	CLR	P1.3	SCLK goes low
	DJNZ	R4, LOOP 3	Next bit
	MOV	R4, #04	Load counter
LOOP 4	RRC	A	Rotate right into Acc.
	DJNZ	R4, LOOP 4	Next Rotate
	MOV	R3, A	Store LSBs in R3
	SETB	P1.4	$\overline{CS}$ goes high

D_{OUT} FROM 1288 STORED IN 8501 RAM

	MSB							
R2	B11	B10	B9	B8	B7	B6	B5	B4
	LSB							
R3	B3	B2	B1	B0	0	0	0	0



TYPICAL APPLICATIONS

A "Quick Look" Circuit for the LTC1285

Users can get a quick look at the function and timing of the LT1285 by using the following simple circuit (Figure 13). V_{REF} is tied to V_{CC}. V_{IN} is applied to the +IN input and the –IN input is tied to the ground. $\overline{CS}$ is driven at 1/16 the clock rate by the 74C161 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 14). Note the LSB data is partially clocked out before $\overline{CS}$ goes high.

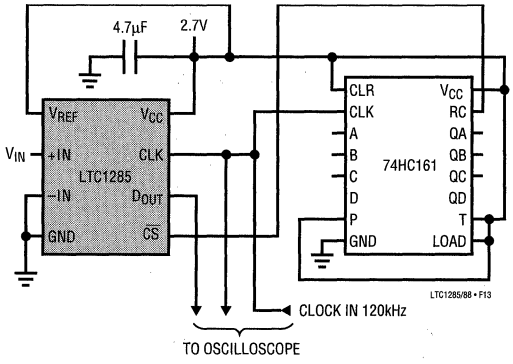


Figure 13. "Quick Look" Circuit for the LTC1285

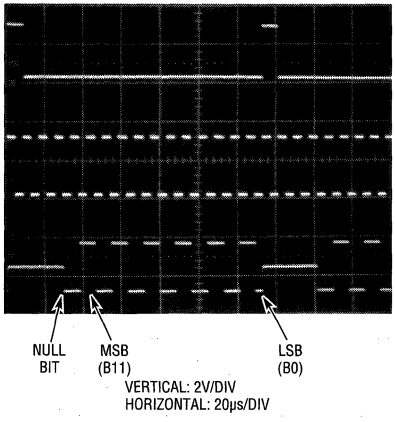


Figure 14. Scope Trace the LTC1285 "Quick Look" Circuit Showing A/D Output 101010101010 (AAA_{HEX})

Micropower Battery Voltage Monitor

A common problem in battery systems is battery voltage monitoring. This circuit monitors the 10 cell stack of NiCad or NiMH batteries found in laptop computers. It draws only 40µA from the 2.7V supply at f_{SMPL} = 0.1kHz and 30µA to 62µA from the battery. The 12-bits of resolution of the LTC1285 are positioned over the desired range of 8V to 16V. This is easily accomplished by using the ADC's differential inputs. Tying the –input to the reference gives an ADC input span of V_{REF} to $2V_{REF}$ (1.2V to 2.4V). The resistor divider then scales the input voltage for 8V to 16V.

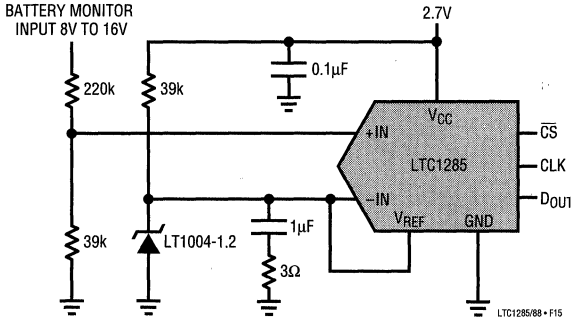


Figure 15. Micropower Battery Voltage Monitor

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
TC1096/LTC1098	8-Pin SOIC, Micropower 8-Bit ADC	Low Power, Small Size, Low Cost
TC1196/LTC1198	8-Pin SOIC, 1Msps 8-bit ADC	Low Power, Small Size, Low Cost
TC1282	3V High Speed Parallel 12-Bit ADC	Complete, V_{REF}, CLK, Sample-and-Hold, 140ksps
TC1289	Multiplexed 3V, 1A 12-Bit ADC	8-Channel, 12-Bit Serial I/O
TC1522	16-Pin SOIC, 3V Micropower 12-Bit ADC	4-Channel, 12-Bit Serial I/O

Complete 12-Bit A/D Converter

FEATURES

- Industry-Standard 574A Compatible
- Complete 12-Bit A/D Converter with Reference and Clock
- Improved Reference Output Current Capability
- 25µs Maximum Conversion Time
- Fast Bus Access Time
- 8- or 16-Bit Microprocessor Interface
- Guaranteed Linearity over Temperature

APPLICATIONS

- Signal Processing
- Data Acquisition
- Process Monitoring and Control

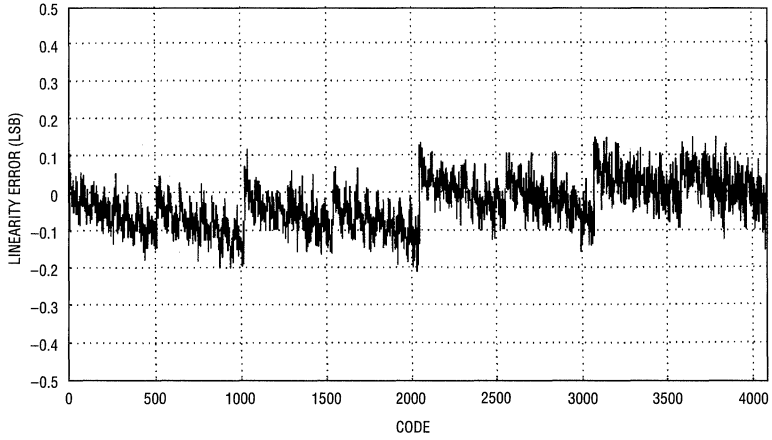
DESCRIPTION

The LT®574A is a complete 12-bit A/D converter in the industry-standard 574A pinout. The three-state output buffers interface directly to an 8- or 16-bit microprocessor bus. A high precision 10V reference and clock are included on-chip, and the device provides full-rated performance without external circuitry or clock signals.

The LT574A provides several advantages over other 574A type devices. External load driving capability of the reference has been improved to up to 8.5mA beyond the ADC current required. Maximum V_{CC} has been increased to 22V and the reference can source full load current at a V_{CC} of 11.4V without requiring an external buffer. The reference is trimmed to 10.00V with 0.2% maximum error and 5ppm/°C typical TC. Bus timing specifications are significantly faster than original 574A specifications, easing microprocessor interface concerns.

TYPICAL PERFORMANCE

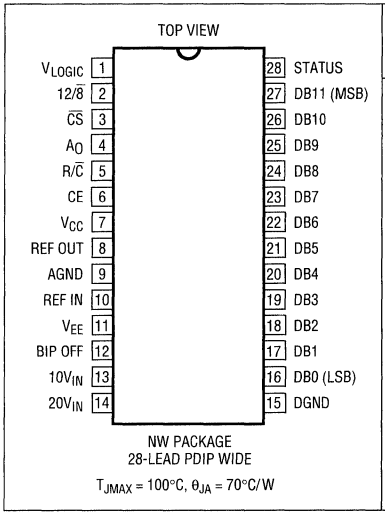
Integral Linearity



ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0V to 22V
V_{EE} to Digital Common ..... 0V to –16.5V
V_{LOGIC} to Digital Common ..... 0V to 7V
Analog Common to Digital Common ..... ±1V
Digital Inputs to
  Digital Common..... $-0.5V$ to $V_{LOGIC} + 0.5V$
Analog Inputs (REF In, BIP Off, $10V_{IN}$)
  to Analog Common..... V_{EE} to 16.5V
$20V_{IN}$ to Analog Common..... V_{EE} to 24V
REF Out ..... Indefinite Short to Analog Common
  Momentary Short to V_{CC}
Power Dissipation..... 1000mW
Junction Temperature..... 165°C
Operating Temperature Range
  J, K, L Grades ..... 0°C to 70°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LT574AJNW
LT574AKNW
LT574ALNW

Consult factory for Industrial and Military grade parts.

CONVERTER ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 12V or 15V, V_{EE} = – 12V, V_{LOGIC} = 5V, unless otherwise specified.

PARAMETER		LT574AJ MIN	LT574AJ TYP	LT574AJ MAX	LT574AK MIN	LT574AK TYP	LT574AK MAX	LT574AL MIN	LT574AL TYP	LT574AL MAX	UNITS
Resolution	●			12			12			12	Bits
Integral Linearity Error	●			±1			±0.5			±0.5	LSB
Differential Linearity Error (Minimum Resolution for Which No Missing Codes are Guaranteed)	●	11			12			12			Bits
Unipolar Offset (Adjustable to Zero)				±2			±1			±1	LSB
Bipolar Offset (Adjustable to Zero)				±4			±4			±2	LSB
Full-Scale Calibration Error (With Fixed 50Ω REF Out to REF In (Adjustable to Zero)				±10			±10			±4	LSB
Temperature Coefficients											
Unipolar Offset	●			±2(10)			±1(5)			±1(5)	LSB(ppm/°C)
Bipolar Offset	●			±2(10)			±1(5)			±1(5)	LSB(ppm/°C)
Full-Scale Calibration	●			±9(50)			±5(27)			±2(10)	LSB(ppm/°C)
Supply Sensitivity (Change in Full Scale Calibration)											
$13.5V \le V_{CC} \le 16.5V$ or $11.4V \le V_{CC} \le 12.6V$	●			±2.0			±1.0			±1.0	LSB
$-16.5V \le V_{EE} \le -13.5V$ or $12.6V \le V_{EE} \le -11.4V$	●			±2.0			±1.0			±1.0	LSB
$4.5V \le V_{LOGIC} \le 5.5V$	●			±0.5			±0.5			±0.5	LSB
Input Ranges											
Unipolar	●	0		10	0		10	0		10	V
	●	0		20	0		20	0		20	V
Bipolar	●	–5		5	–5		5	–5		5	V
	●	–10		10	–10		10	–10		10	V
Input Impedance											
10V Span	●	3	5	7	3	5	7	3	5	7	kΩ
20V Span	●	6	10	14	6	10	14	6	10	14	kΩ

INTERNAL REFERENCE ELECTRICAL CHARACTERISTICS

PARAMETER		LT574AJ MIN	LT574AJ TYP	LT574AJ MAX	LT574AK MIN	LT574AK TYP	LT574AK MAX	LT574AL MIN	LT574AL TYP	LT574AL MAX	UNITS
REF OUT Voltage (No Load)		9.98		10.02	9.98		10.02	9.99		10.01	V
Line Regulation, $11.4 \le V_{IN} \le 22V$			1	5		1	5		1	5	ppm/V
	●			10			10			10	ppm/V
Load Regulation (Sourcing Current), $0 \le I_{OUT} \le 10mA$			12	30		12	30		12	30	ppm/mA
	●			50			50			50	ppm/mA
Reference Temperature Coefficient	●			50			27			10	ppm/°C

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS		LT574A, All Grades MIN	LT574A, All Grades TYP	LT574A, All Grades MAX	UNITS
	V_{LOGIC} Supply Range		●	4.5	5.0	5.5	V
	V_{EE} Supply Range		●	−11.4		−16.5	V
	V_{CC} Supply Range		●	11.4		22.0	V
	V_{LOGIC} Operating Current		●		27	40	mA
	V_{EE} Operating Current		●		−15	−25	mA
	V_{CC} Operating Current		●		1.7	3.5	mA
	Power Dissipation		●		390	700	mW
V_{IH}	Logic High Input Voltage	12/8, CE, A_0, R/C, CE	●	2.0		5.5	V
V_{IL}	Logic Low Input Voltage	12/8, CE, A_0, R/C, CE	●	−0.5		0.8	V
I_{IN}	Logic Input Current		●	−100		100	µA
C_{IN}	Digital Input Pin Capacitance				5		pF
V_{OH}	Logic Output Voltage	$I_{SOURCE} \le 600\mu A$		2.4			V
V_{OL}	Logic Low Output Voltage	$I_{SINK} \le 1.6mA$				0.4	V
	Leakage Current	High-Z State		−20		20	µA
C_{OUT}	Output Capacitance				5		pF

The ● denotes the specifications which apply over the full operating temperature range.

DIGITAL TIMING ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 15V, V_{EE} = −15V, V_{LOGIC} = 5V, unless otherwise specified.

	SYMBOL	PARAMETER	LT574A, All Grades MIN	LT574A, All Grades TYP	LT574A, All Grades MAX	UNITS
Read Timing, Full Control Mode	t_{DD}	Access Time (from CE)		75	150	ns
	t_{HD}	Data Valid After CE Low	25			ns
	t_{HL}	Output Float Delay			150	ns
	t_{SSR}	$\overline{CS}$-to-CE Setup	50			ns
	t_{SRR}	R/$\overline{C}$-to-CE Setup	0			ns
	t_{SAR}	AO-to-CE Setup	50			ns
	t_{HSR}	$\overline{CS}$ Valid After CE Low	50			ns
	t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
	t_{HAR}	A_0 Valid After CE Low	50			ns

DIGITAL TIMING ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 15V, V_{EE} = –15V, V_{LOGIC} = 5V, unless otherwise specified.

	SYMBOL	PARAMETER	LT574A, All Grades MIN	TYP	MAX	UNITS
Convert Start Timing, Full Control Mode	t_{DSC}	STS Delay from CE			200	ns
	t_{HEC}	CE Pulse Width	50			ns
	t_{SSC}	CS-to-CE Setup	50			ns
	t_{HSC}	CS Low During CE High	50			ns
	t_{SRC}	R/C-to-CE Setup	50			ns
	t_{HRC}	R/C Low During CE High	50			ns
	t_{SAC}	AO-to-CE Setup	0			ns
	t_{HAC}	AO Valid During CE High	50			ns
	t_C	Conversion Time				
		8-Bit Cycle	10		17	µs
		12-Bit Cycle	15		25	µs
Stand-Alone Mode Timing	t_{HRL}	Low R/C Pulse Width	50			ns
	t_{DS}	STS Delay From R/C			200	ns
	t_{HDR}	Data Valid After R/C Low	25			ns
	t_{HS}	STS Delay After Data Valid	25		600	ns
	t_{HRH}	High R/C Pulse Width	150			ns
	t_{DDR}	Data Access Time			150	ns

BLOCK DIAGRAM

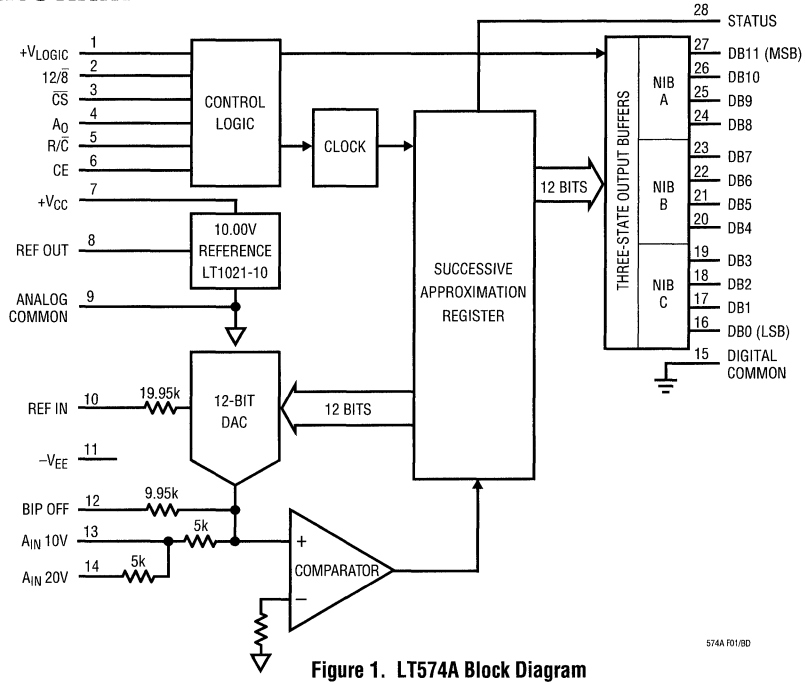


Figure 1. LT574A Block Diagram

DISCUSSION OF SPECIFICATIONS

Integral Linearity Error

Integral linearity (INL) error refers to the deviation of each code from a theoretical line drawn from "full scale." Zero is defined as the input voltage occurring 0.5LSB (1.22mV for 10V full scale) before the first code transition (0 to 1) and "full scale" is defined as the voltage occurring 1.5LSB beyond the last code transition (4094 to 4095).

Differential Linearity Error

A guaranteed "no missing codes" specification requires that every code combination appears in a monotonically increasing sequence. Thus LT574A grades which guarantee no missing codes to 12-bit resolution have a maximum DNL error of ±1LSB; grades which guarantee no missing code to an 11-bit level means that all code combinations of the upper 11 bits are present. In practice very few of the 12-bit codes are missing on the lower grade(s).

Unipolar Offset

Unipolar offset error is defined as the deviation of the first code transition from a level 0.5LSB above analog common. Unipolar offset can be adjusted as shown on the following pages. The unipolar offset temperature coefficient specifies the change of the first transition value versus a change in ambient temperature.

Bipolar Offset

The major carry transition (2047 to 2048) should occur for an analog value 0.5LSB above analog common in the bipolar mode. Bipolar offset error can also be adjusted as shown on the following pages. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error versus temperature.

Quantization Uncertainty

Analog-to-digital converters have inherent quantization uncertainty of ±0.5LSB. This uncertainty is a fundamental property of the conversion process and cannot be reduced for a converter of a given resolution.

Left-Justified Data

The LT574A uses a left-justified data format. The analog input is represented as a fraction of full scale, ranging from 0 to 4095/4096. A binary point to the left of the MSB is implied.

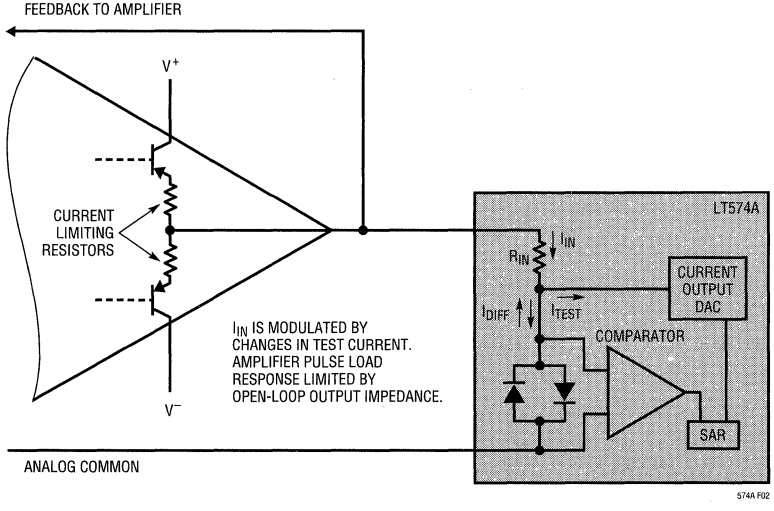


Figure 2. Op Amp/LT574A Interface

DISCUSSION OF SPECIFICATIONS

Full-Scale Calibration Error

The last output code transition (4094 to 4095) should occur for an analog value 1.5LSB below the nominal full scale (9.9963V for 10.000V full scale). The deviation of the actual level at which this transition occurs from the ideal level is the full-scale calibration error. Typically less than 0.1% of full scale, this error can be adjusted to zero as shown in Figures 3 and 4.

Temperature Coefficients

The temperature coefficients for unipolar offset, bipolar offset and full-scale calibration specify the maximum change from the nominal (25°C) value to T_{MIN} or T_{MAX}.

Power Supply Sensitivity

The LT574A is specified using 5V and ±15V or ±12V supplies. The major effect of power supply voltage deviations from the rated values will be a small change in full-scale calibration. This change results in a proportional change in all code values.

Code Width

Code width is defined as the range of analog values for which a given output code will occur. The ideal value of a code width is equivalent to 1LSB (least significant bit) of the full-scale range. In a 10V full-scale range one LSB corresponds to 2.44mV.

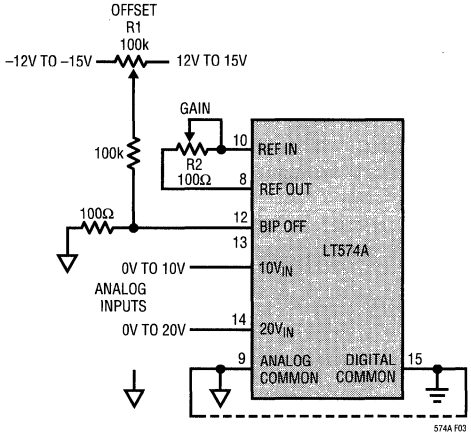


Figure 3. Unipolar Input Connections

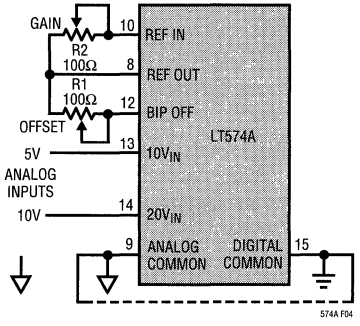


Figure 4. Bipolar Input Connections

6

OPERATION

Circuit Operation

The LT574A provides the complete 12-bit analog-to-digital function with no external components. A block diagram of the LT574A is shown in Figure 1. After a conversion is initiated via the control section (described later) the clock is enabled and the SAR is set to 1000 0000 0000. Once a conversion is started it cannot be stopped or restarted. The output buffers go into the Hi-Z state. The SAR, driven by the internal clock, will sequence through the conversion cycle and return a signal indicating end-of-conversion to the control section. The control section then disables the clock, bring the Status output low, and enables control functions to allow data read functions via external command.

During a conversion, the internal 12-bit current-output DAC is sequenced by the SAR starting with the most significant bit (MSB) and ending with the least significant bit (LSB). At the end of the process the DAC outputs a current which accurately balances the input signal current through the 5k (10k) input resistor. The comparator looks at the summing node at every bit test. If the DAC current sum is greater than the input current, the bit is turned off;

OPERATION

if less, the bit is left on. After all 12 bits have been tested, the SAR contains a 12-bit digital representation of the analog input signal accurate to 12 bits ±0.5LSB. Two 5k input scaling resistors allow either 10V or 20V span operation. The 10k bipolar offset resistor is connected to the 10V reference for bipolar operation, or grounded for unipolar operation.

Internal 10.00V Reference

An LT1021-10 low noise, high stability, buried-zener reference is used inside the LT574A device and guarantees superior stability over time and temperature. This reference provides improved performance over other 574-type references in both voltage range and output current sourcing capability. The reference is trimmed to 10.00V ±2%. It can supply up to 8.5mA to an external load in addition to the current required by the reference input resistor (0.5mA) and the bipolar offset resistor (1mA). This is an additional 7mA over most other 574A-type devices. (The external load should not change during a conversion.) The LT574A also has an improved V_{CC} supply range; the V_{CC} input can range from 11.2V to 22V. If operating from ±12V supplies, improved driving capability eliminates the need for an external buffer to source external loads at room temperature or over the specified temperature range.

Driving the LT574A Analog Inputs

The signal source driving the LT574A input looks into a 5k or 10k impedance. However, the current drawn out of the input pins is abruptly modulated as the ADC steps through the bit tests. Low source impedance at high frequency, necessary to hold the input voltage constant through the conversion cycle, is required for 12-bit accurate conversions. The output impedance of an op amp is equal to its open-loop output impedance divided by the loop gain available at the frequency of interest. Acceptable loop gain at 500kHz is needed for use with the LT574A. An op amp can be checked for suitability by monitoring the LT574A's input with an oscilloscope while a conversion is in progress. Each of the 12 disturbances should settle in 1µs or less. Suitable op amps include the LT1055 or LT1122.

Layout Precautions and Supply Decoupling

It is critically important the LT574A power supplies be well regulated and free of high frequency noise. Noisy supplies will cause unstable output codes. If switching power supplies must be used, considerable care must be used to ensure that switching spikes are eliminated. (For more information on constructing switching power supplies suitable for use with precision analog circuits, please see Linear Technology's Application Note 29). Just a few millivolts of high frequency noise on the power supply will result in several counts of error.

Decoupling capacitors should be used on all power supply pins. V_{LOGIC} decoupling should be connected directly from pin 1 to pin 15 (digital common) and V_{CC} and V_{EE} pins should be decoupled directly to analog common (pin 9). A 4.7µF tantalum unit in parallel with a 0.1µF ceramic type makes a suitable decoupling capacitor.

The LT574A should be located as far as possible from digital circuitry on the board layout. Coupling between analog and digital lines should be minimized. If analog and digital lines must cross, they should do so at right angles. Parallel analog and digital lines should be separated by a pattern connected to common. Wire-wrap construction is not recommended; careful printed circuit layout is preferred instead.

Grounding Considerations

The analog common (pin 9) is the internal reference ground and should be connected directly to the analog reference point of the system. It is the "high quality" ground point. Pin 9 should be connected to digital common (pin 15) at the package to achieve all the high performance accuracy available from the LT574A in noisy digital environments. This single-point grounding is the preferred method for grounding mixed analog/digital systems. Be sure there are no digital ground returns on the analog side of the line; input signal returns should be isolated from digital ground and returned directly to the single-point ground at the LT574A package.

)PERATION

ange Connections

he LT574A has four standard input ranges: 0V to 10V, V to 20V, –5V to 5V, and –10V to 10V. To use the 10V ınge, connect the input signal between pins 13 and 9. To se the 20V range, connect the input signal between pins 4 and 9. In both cases, the other pin of the two is left nconnected. Full-scale and offset adjustments are shown ı Figure 3. If full-scale trim is not needed, connect a 50Ω, % metal film resistor between pins 8 and 10. To extend ıe 10V range to 10.24V (2.5mV/bit) with gain trim otentiometer (R2) should be replaced by a 50Ω resistor ıd a 200Ω potentiometer should be placed in series ith the $10V_{IN}$ pin. To obtain a full-scale range of 20.48V ;mV/bit), a 500Ω potentiometer should be used in ;ries with pin 14. Gain trim is now implemented with ıese potentiometers.

nipolar Calibration

ıe first transition of the LT574A occurs at a value 0.5LSB)ove analog common, so that the exact analog input for given code will be halfway between the code transitions. This 0.5LSB offset is built into the LT574A. The unit will behave in this manner, within specifications, if pin 12 is connected to analog common (pin 9). Referring to Figure 3, R1 performs the offset adjust function. It should be adjusted so that the first transition falls at exactly 0.5LSB above the analog common potential (nominally ground). The circuit, as shown, will give approximately ±15mV of offset trim range. The full-scale trim is calibrated by applying a voltage 1.5LSB below full scale (9.9963V for 10V full scale) and adjusting R2 such that the unit outputs the codes 4096 and 4097 (1111 1111 1110 and 1111 1111 1111).

Bipolar Operation

Bipolar operation connections are shown in Figure 4. The trim potentiometers can be replaced by 50Ω, 1% resistors if offset and gain specifications are sufficient. To calibrate, apply an input signal 0.5LSB above negative full scale (0000 0000 0000 to 0000 0000 0001), then apply a signal 1.5LSB below positive full scale (4.9963V for the ±5V range) and adjust R2 so that the last transition (1111 1111 1110 to 1111 1111 1111) is output.

SECTION 6—DATA CONVERSION

FEATURES

- 12-Bit Resolution
- **Buffered True Rail-to-Rail Voltage Output**
- 3V Operation (LTC1453), I_{CC}: 250µA Typ
- 5V Operation (LTC1451), I_{CC}: 400µA Typ
- 3V to 5V Operation (LTC1452), I_{CC}: 225µA Typ
- Built-In Reference: 2.048V (LTC1451)
  1.220V (LTC1453)
- Multiplying Version (LTC1452)
- Power-On Reset
- **SO-8 Package**
- 3-Wire Cascadable Serial Interface
- **Maximum DNL Error: 0.5LSB**
- Low Cost

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

DESCRIPTION

The LTC®1451/LTC1452/LTC1453 are complete single supply, rail-to-rail voltage output 12-bit digital-to-analog converters (DACs) in an SO-8 package. They include an output buffer amplifier and an easy-to-use 3-wire cascadable serial interface.

The LTC1451 has an onboard reference of 2.048V and a full-scale output of 4.095V. It operates from a single 4.5V to 5.5V supply.

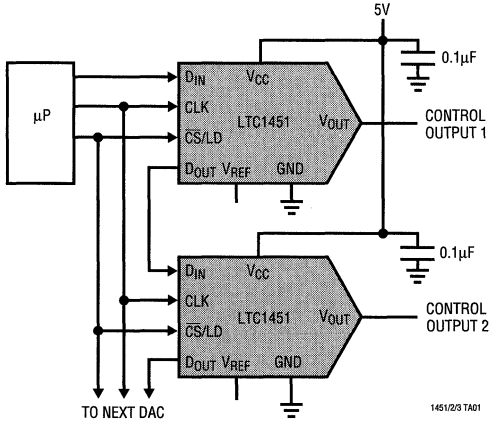
The LTC1452 is a multiplying DAC with a full-scale output of twice the reference input voltage. It operates from a single supply of 2.7V to 5.5V.

The LTC1453 has an onboard 1.22V reference and a full-scale output of 2.5V. It operates from a single supply of 2.7V to 5.5V.

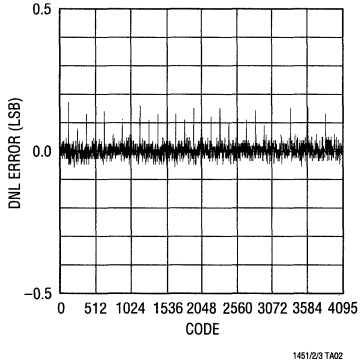
The low power supply current makes the LTC1451 family ideal for battery-powered applications. The space saving 8-pin SO package and operation with no external components provide the smallest 12-bit DAC system available.

TYPICAL APPLICATION

Daisy-Chained Control Outputs



Differential Nonlinearity vs Input Code

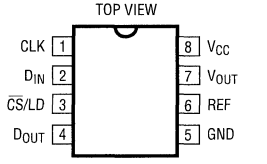


ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... −0.5V to 7.5V
TTL Input Voltage ..... −0.5V to 7.5V
V_{OUT} ..... −0.5V to V_{CC} + 0.5V
REF ..... −0.5V to V_{CC} + 0.5V
Maximum Junction Temperature ..... −65°C to 125°C

Operating Temperature Range
Commercial ..... 0°C to 70°C
Industrial ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER		S8 PART MARKING
LTC1451CN8	LTC1451CS8	1451C
LTC1452CN8	LTC1452CS8	1451I
LTC1453CN8	LTC1453CS8	1452C
LTC1451IN8	LTC1451IS8	1452I
LTC1452IN8	LTC1452IS8	1453C
LTC1453IN8	LTC1453IS8	1453I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1451), 2.7V to 5.5V (LTC1452/LTC1453), internal or external reference ($V_{REF} \leq V_{CC}/2$), V_{OUT} and REF unloaded, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC							
	Resolution		●	12			Bits
NL	Differential Nonlinearity	Guaranteed Monotonic (Note 1)	●			±0.5	LSB
IL	Integral Nonlinearity	T_A = 25°C				±3.5	LSB
		(Note 1)	●			±4	LSB
OS	Offset Error	T_A = 25°C				±12	mV
			●			±18	mV
OSTC	Offset Error Temperature Coefficient				±15		µV/°C
FS	Full-Scale Voltage	When Using Internal Reference, LTC1451, T_A = 25°C		4.065	4.095	4.125	V
		LTC1451	●	4.045	4.095	4.145	V
		External 2.048V Reference, V_{CC} = 5V, LTC1452	●	4.075	4.095	4.115	V
		When Using Internal Reference, LTC1453, T_A = 25°C		2.470	2.500	2.530	V
		LTC1453	●	2.460	2.500	2.540	V
FSTC	Full-Scale Voltage Temperature Coefficient	When Using Internal Reference, LTC1451			±0.10		LSB/°C
		When Using External 2.048V Reference, LTC1452			±0.02		LSB/°C
		When Using Internal Reference, LTC1453			±0.10		LSB/°C

6

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1451), 2.7V to 5.5V (LTC1452/LTC1453), internal or external reference ($V_{REF} \leq V_{CC}/2$), V_{OUT} and REF unloaded, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference (LTC1451/LTC1453)							
	Reference Output Voltage	LTC1451 LTC1453	● ●	2.008 1.195	2.048 1.220	2.088 1.245	V V
	Reference Output Temperature Coefficient				±0.08		LSB/°C
	Reference Line Regulation		●		0.7	±2	LSB/V
	Reference Load Regulation	$0 \leq I_{OUT} \leq 100\mu A$, LTC1451 LTC1453	● ●		0.2 0.6	±1.5 ±3	LSB LSB
	Reference Input Range	$V_{REF} \leq V_{CC} - 1.5V$	●			$V_{CC}/2$	V
	Reference Input Resistance		●	8	14	30	kΩ
	Reference Input Capacitance				15		pF
	Short-Circuit Current	REF Shorted to GND	●			80	mA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance, LTC1451 LTC1452 LTC1453	● ● ●	4.5 2.7 2.7		5.5 5.5 5.5	V V V
I_{CC}	Supply Current	$4.5V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1451 $2.7V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1452 $2.7V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1453	● ● ●	300 120 150	400 225 250	620 350 500	µA µA µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●			100	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●			120	mA
	Output Impedance to GND	Input Code = 0	●		40	120	Ω
AC Performance							
	Voltage Output Slew Rate	(Note 2)	●	0.5	1.0		V/µs
	Voltage Output Settling Time	(Notes 2, 3) to ±0.5LSB			14		µs
	Digital Feedthrough				0.3		nV•s
	AC Feedthrough	REF = 1kHz, $2V_{P-P}$, LTC1452			–95		dB
SINAD	Signal-to-Noise + Distortion	REF = 1kHz, $2V_{P-P}$, (Code: All 1s) LTC1452			85		dB

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V (LTC1451LTC1452), V_{CC} = 3V (LTC1453), $T_A = T_{MIN}$ to T_{MAX}

SYMBOL	PARAMETER	CONDITIONS		LTC1451/LTC1452 MIN	LTC1451/LTC1452 TYP	LTC1451/LTC1452 MAX	LTC1453 MIN	LTC1453 TYP	LTC1453 MAX	UNITS
Digital I/O										
V_{IH}	Digital Input High Voltage		●	2.4			2.0			V
V_{IL}	Digital Input Low Voltage		●			0.8			0.6	V
V_{OH}	Digital Output High Voltage	I_{OUT} = –1mA	●			V_{CC} – 1.0			V_{CC} – 0.7	V
V_{OL}	Digital Output Low Voltage	I_{OUT} = 1mA	●	0.4			0.4			V
I_{LEAK}	Digital Input Leakage	V = GND to V_{CC}	●			±10			±10	µA
C_{IN}	Digital Input Capacitance	Guaranteed by Design Not Subject to Test	●			10			10	pF
Switching										
1	D_{IN} Valid to CLK Setup		●			40			60	ns
2	D_{IN} Valid to CLK Hold		●			0			0	ns
3	CLK High Time		●			40			60	ns
4	CLK Low Time		●			40			60	ns
5	$\overline{CS}$/LD Pulse Width		●			50			80	ns
6	LSB CLK to $\overline{CS}$/LD		●			40			60	ns
7	$\overline{CS}$/LD Low to CLK		●			20			30	ns
8	D_{OUT} Output Delay	C_{LOAD} = 15pF	●			150			220	ns
9	CLK Low to $\overline{CS}$/LD Low		●			20			30	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 4095 (full scale).

Note 2: Load is 5kΩ in parallel with 100pF.

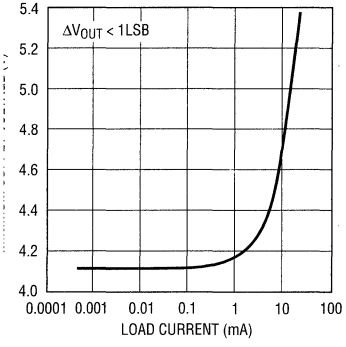
Note 3: DAC switched between all 1s and the code corresponding to V_{OS} for the part, i.e., LTC1451: code 18; LTC1453: code 30.

Note 4: Digital inputs at 0V or V_{CC}.

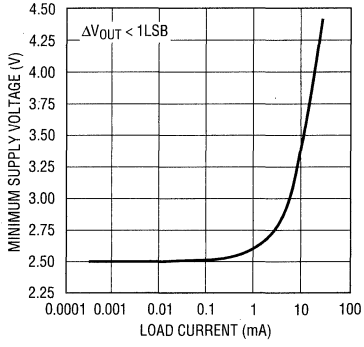
6

TYPICAL PERFORMANCE CHARACTERISTICS

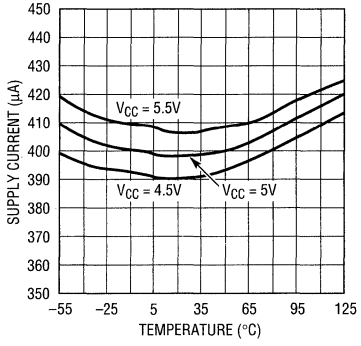
LTC1451 Minimum Supply Voltage vs Load Current



LTC1453 Minimum Supply Voltage vs Load Current

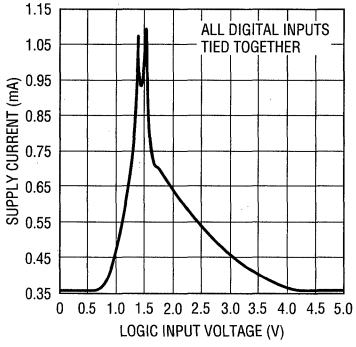


LTC1451 Supply Current vs Temperature

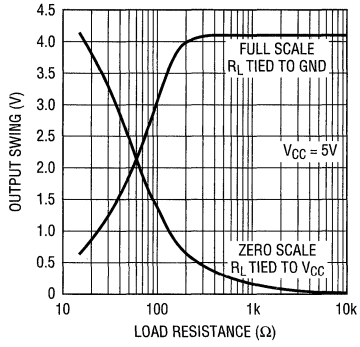


TYPICAL PERFORMANCE CHARACTERISTICS

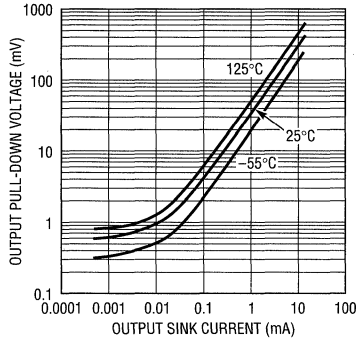
LTC1451
Supply Current vs Logic Input Voltage



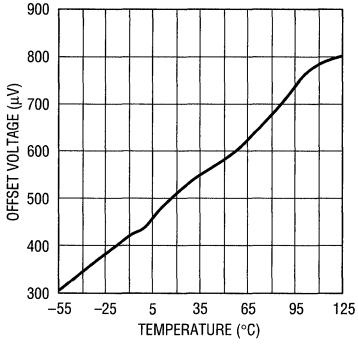
LTC1451
Output Swing vs Load Resistance



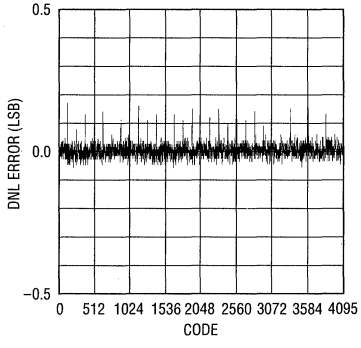
LTC1451
Pull-Down Voltage vs Output Sink Current Capability



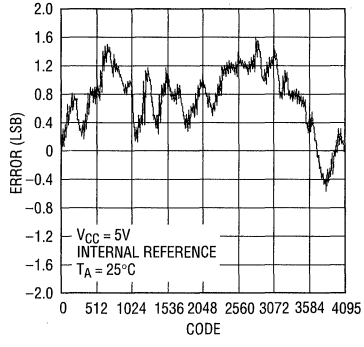
LTC1451
Offset Voltage vs Temperature



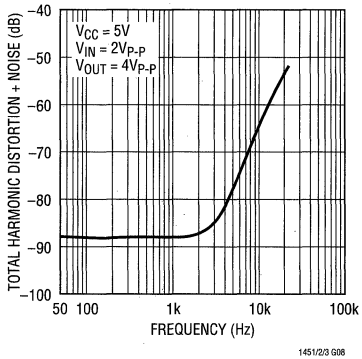
LTC1451
Differential Nonlinearity (DNL)



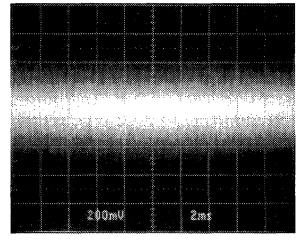
LTC1451
Integral Nonlinearity (INL)



LTC1452
Total Harmonic Distortion + Noise vs Frequency



LTC1451
Broadband Output Noise



PIN FUNCTIONS

CLK: The TTL Level Input for the Serial Interface Clock.

D_{IN}: The TTL Level Input for the Serial Interface Data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock.

$\overline{CS}$/LD: The TTL Level Input for the Serial Interface Enable and Load Control. When $\overline{CS}$/LD is low the CLK signal is enabled, so the data can be clocked in. When $\overline{CS}$/LD is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

D_{OUT}: The Output of the Shift Register which Becomes Valid on the Rising Edge of the Serial Clock.

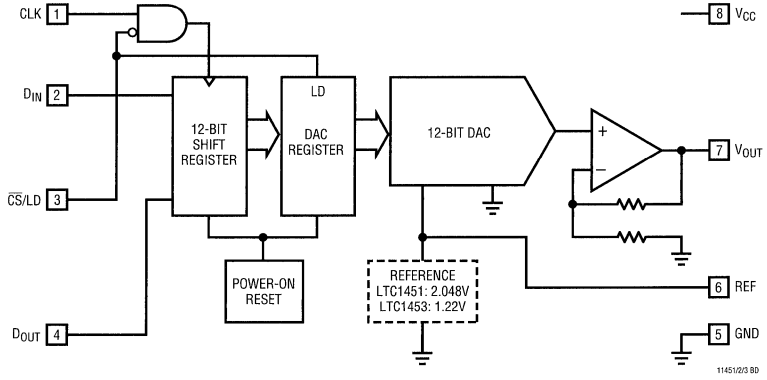
GND: Ground.

REF: The Output of the Internal Reference and the Input to the DAC Resistor Ladder. An external reference with voltage up to $V_{CC}/2$ may be used for the LTC1452.

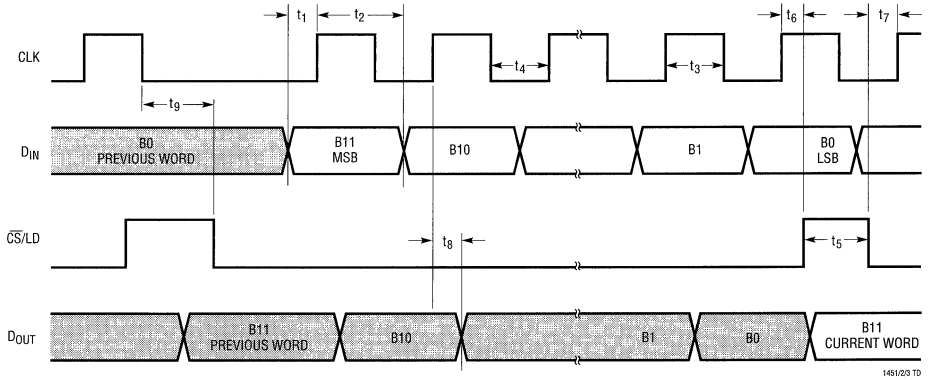
V_{OUT}: The Buffered DAC Output.

V_{CC}: The Positive Supply Input. $4.5V \leq V_{CC} \leq 5.5V$ (LTC1451), $2.7 \leq V_{CC} \leq 5.5V$ (LTC1452/LTC1453). Requires a bypass capacitor to ground.

BLOCK DIAGRAM



TIMING DIAGRAM



DEFINITIONS

Resolution (n): Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states (2^n) that divide the full-scale range. The resolution does not imply linearity.

Full-Scale Voltage (V_{FS}): This is the output of the DAC when all bits are set to 1.

Voltage Offset Error (V_{OS}): The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code \times V_{FS})/(2^n - 1)]$$

Least Significant Bit (LSB): One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/(2^n - 1) = (V_{FS} - V_{OS})/4095$$

Nominal LSBs:

LTC1451 LSB = 4.095V/4095 = 1mV
LTC1452 LSB = V(REF)/4095
LTC1453 LSB = 2.5V/4095 = 0.610mV

Integral Nonlinearity (INL): End-point INL is the maximum deviation from a straight line passing through the end-points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/4095)]/LSB$
V_{OUT} = The output voltage of the DAC measured at the given input code

Differential Nonlinearity (DNL): DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$DNL = (\Delta V_{OUT} - LSB)/LSB$
ΔV_{OUT} = The measured voltage difference between two adjacent codes

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in nV × sec.

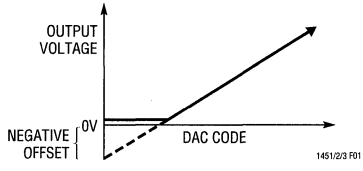


Figure 1. Effect of Negative Offset

OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first. The DAC register loads the data from the shift register when $\overline{CS}$/LD is pulled high. The CLK is disabled internally when $\overline{CS}$/LD is high. Note: CLK must be low before $\overline{CS}$/LD is pulled low to avoid an extra internal clock pulse.

The buffered output of the 12-bit shift register is available on the D_{OUT} pin which swings from GND to V_{CC}.

Multiple LTC1451/LTC1452/LTC1453s may be daisy-chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip, while the CLK and $\overline{CS}$/LD signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the $\overline{CS}$/LD signal is pulled high to update all of them simultaneously.

Reference

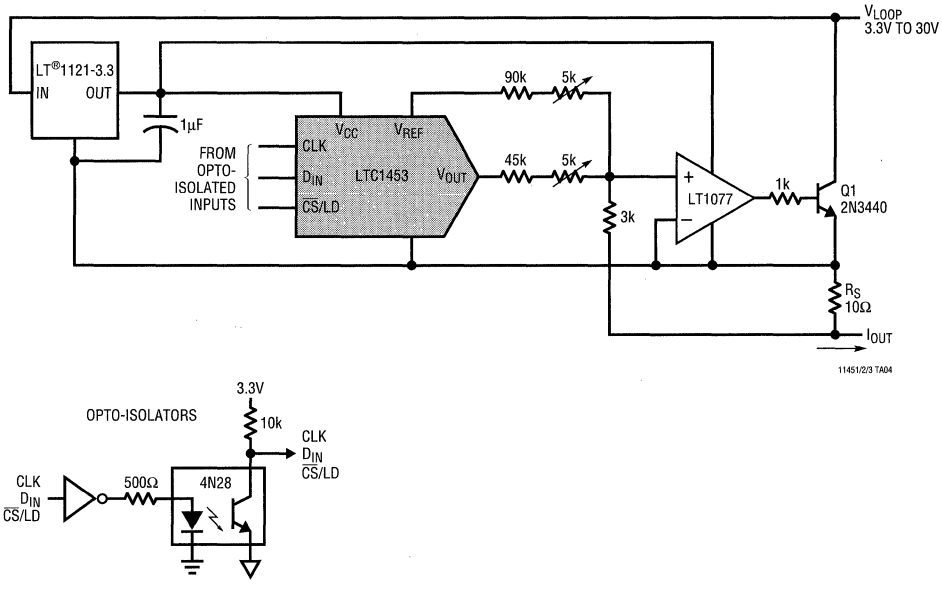
The LTC1451 includes an internal 2.048V reference, making 1LSB equal to 1mV (gain of 2). The LTC1453 has an internal reference of 1.22V with a full scale of 2.5V (gain of 2.05). The internal reference output is turned off when the pin is forced above the reference voltage, allowing an external reference to be connected to the reference pin. The LTC1452 has no internal reference and the REF pin must be driven externally. The buffer gain is 2, so the external reference must be less than $V_{CC}/2$ and be capable of driving the 8k minimum DAC resistor ladder.

Voltage Output

The LTC1451 family's rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails. The output can drive 1000pF without going into oscillation.

TYPICAL APPLICATIONS

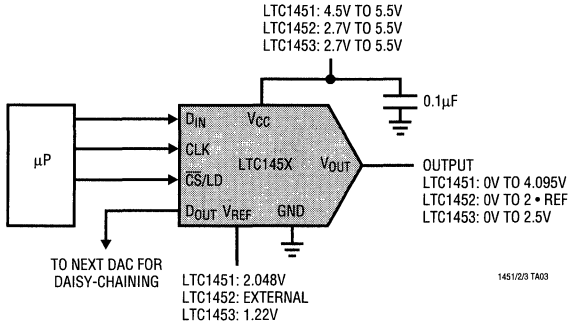
An Isolated 4mA to 20mA Process Controller Has 3.3V Minimum Loop Voltage



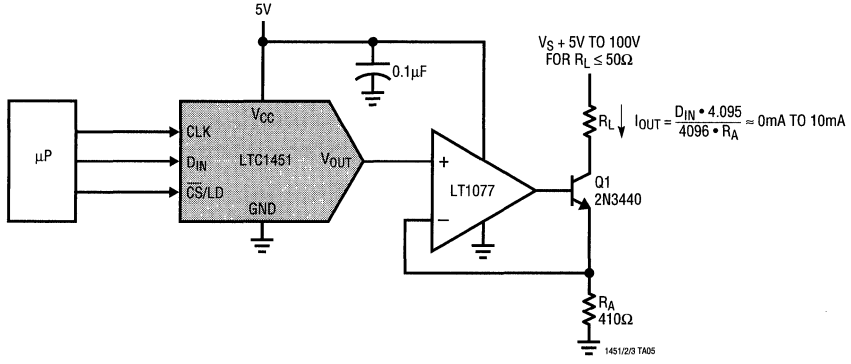
This circuit shows how to use an LTC1453 to make an opto-isolated digitally controlled 4mA to 20mA process controller. The controller circuitry, including the opto-isolation, is powered by the loop voltage that can have a wide range of 3.3V to 30V. The 1.22V reference output of the LTC1453 is used for the 4mA offset current and V_{OUT} is used for the digitally controlled 0mA to 16mA current. R_S is a sense resistor and the op amp modulates the transistor Q1 to provide the 4mA to 20mA current through this resistor. The potentiometers allow for offset and full-scale adjustment. The control circuitry dissipates well under the 4mA budget at zero-scale.

TYPICAL APPLICATIONS

12-Bit 3V to 5V Voltage Output DAC



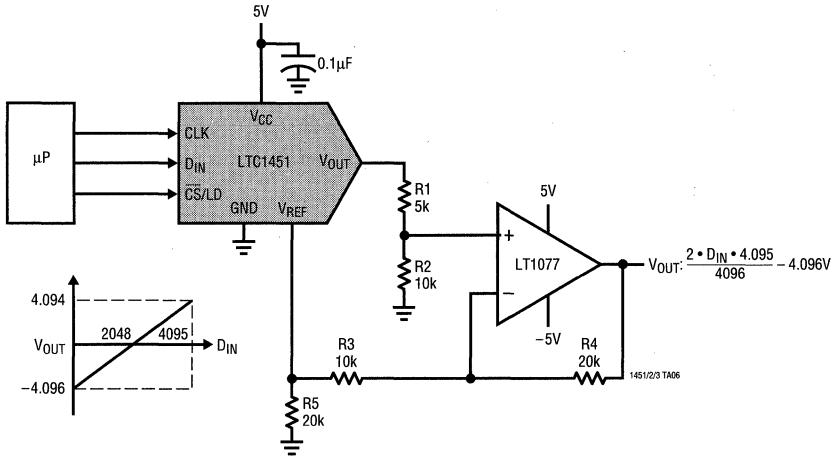
Digitally Programmable Current Source



This circuit shows a digitally programmable current source from an external voltage source using an external op amp, an LT1077 and an NPN transistor (2N3440). Any digital word from 0 to 4095 is loaded into the LTC1451 and its output correspondingly swings from 0V to 4.095V. In the configuration shown, this voltage will be forced across the resistor R_A. If R_A is chosen to be 410Ω the output current will range from 0mA at zero-scale to 10mA at full-scale. The minimum voltage for V_S is determined by the load resistor R_L and Q1's V_{CESAT} voltage. With a load resistor of 50Ω, the voltage source can be as low as 5V.

TYPICAL APPLICATIONS

A Wide Swing, Bipolar Output 12-Bit DAC



This circuit shows how to make a bipolar output 12-bit DAC with a wide output swing using an LTC1451 and an LT®1077. R1 and R2 resistively divide down the LTC1451 output and an offset is summed in using the LTC1451 onboard 2.048V reference and R3 and R4. R5 ensures that the onboard reference is always sourcing current and never has to sink any current even when V_{OUT} is at full-scale. The LT1077 output will have a wide bipolar output swing of –4.096V to 4.094V as shown in the figure above. With this output swing 1LSB = 2mV.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Single 12-Bit V_{OUT} DAC, Full Scale: 2.048V, V_{CC}: 4.75V to 15.75V. Reference Can Be Overdriven Up to 12V, i.e., FS MAX = 12V	5V to 15V Single Supply, Complete V_{OUT} DAC in SO-8 Package
LTC7541	12-Bit Multiplying Parallel I_{OUT} DAC	5V to 16V Supply, 12-Bit Wide Interface
LTC7543/LTC8143	12-Bit Multiplying Serial I_{OUT} DAC	5V Supply, Clear Pin and Serial Data Output (LTC8143)
LTC8043	12-Bit Multiplying Serial I_{OUT} DAC	5V Supply, SO-8 Package

Improved Industry Standard CMOS 12-Bit Multiplying DAC

FEATURES

- Improved Direct Replacement for AD7541A and AD7541
- 4-Quadrant Multiplication
- **12-Bit End-Point Linearity: ±0.5LSB DNL and INL Over Temperature**
- All Grades Guaranteed Monotonic
- **Maximum Gain Error: ±1LSB**
- Single 5V to 15V Supply
- TTL and CMOS Logic Compatible
- Reduced Sensitivity to Op Amp Offset
- Low Power Consumption
- Virtually Latch-Up Proof
- Low Cost

APPLICATIONS

- Motion Control Systems
- Microprocessor-Controlled Calibration
- Automatic Test Equipment
- Programmable Gain Amplifiers
- Digitally Controlled Filters

DESCRIPTION

The LTC®7541A is a 12-bit resolution multiplying digital-to-analog converter (DAC).

Laser-trimmed thin-film resistors provide excellent absolute accuracy. Precision matched resistors and CMOS circuitry result in remarkable stability with temperature and supply variations.

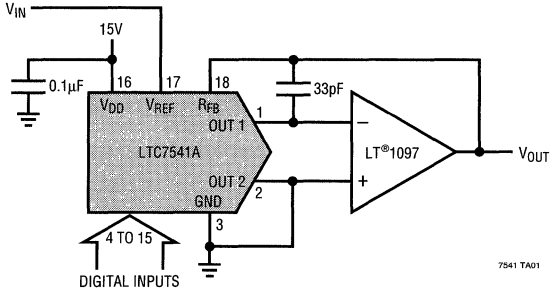
The LTC7541A is a superior pin compatible replacement for the industry standard AD7541A/AD7541. Improvements include better typical accuracy and stability and reduced sensitivity to output amplifier offset. The LTC7541A is also very resistant to latch-up.

In addition to 2-quadrant and 4-quadrant multiplying configurations, the LTC7541A performs well in digitally programmable gain and noninverting voltage output applications. Low cost, improved performance and versatility make the LTC7541A the best choice for many new designs and for upgrading existing systems. Parts are available in 18-pin PDIP and 18-pin SO Wide packages.

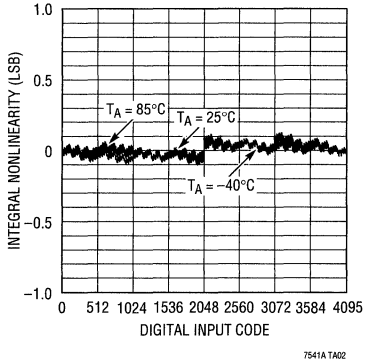
6

TYPICAL APPLICATION

2-Quadrant Multiplying DAC Has Less Than 0.5LSB (Typ) Total Unadjusted Error



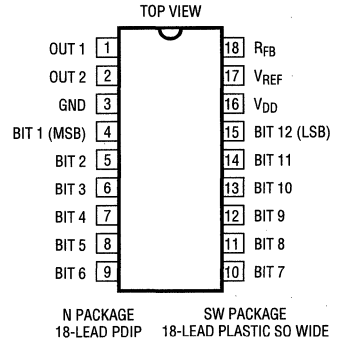
Integral Nonlinearity Over Temperature



ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... −0.5V to 17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Inputs to GND ..... −0.5V to (V_{DD} + 0.5V)
OUT 1, OUT 2 to GND ..... −0.5V to (V_{DD} + 0.5V)
Power Dissipation 450mW
(Derate 6mW/°C Above 75°C)
Maximum Junction Temperature ..... −65°C to 125°C
Operating Temperature Range
Commercial (J, K Versions) ..... 0°C to 70°C
Industrial (B Version) ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER
LTC7541ABN
LTC7541ABSW
LTC7541AJN
LTC7541AKN
LTC7541AJSW
LTC7541AKSW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{DD} = 15V, V_{REF} = 10V, OUT 1 = OUT 2 = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC7541AJ MIN	LTC7541AJ TYP	LTC7541AJ MAX	LTC7541AK/LTC7541AB MIN	LTC7541AK/LTC7541AB TYP	LTC7541AK/LTC7541AB MAX	UNITS
Accuracy										
	Resolution		●	12			12			Bits
INL	Integral Nonlinearity (Relative Accuracy)	(Note 1)	●			±1			±0.5	LSB
DNL	Differential Nonlinearity	Guaranteed Monotonic, T_{MIN} to T_{MAX}	●			±1			±0.5	LSB
GE	Gain Error	(Note 2) T_A = 25°C				±6			±1	LSB
		T_{MIN} to T_{MAX}	●			±8			±2	LSB
	Gain Temperature Coefficient	(Note 3)	●		1	5		1	5	ppm/°C
I_{LKG}	Output Leakage Current	(Note 4) T_A = 25°C				±5			±5	nA
		T_{MIN} to T_{MAX}	●			±10			±10	nA
PSRR	Power Supply Rejection	V_{DD} = 15V ±5%	●			±0.002			±0.002	%/%
Reference Input										
R_{REF}	V_{REF} Input Resistance		●	7	11	15	7	11	15	kΩ
	V_{REF} Input Resistance Temperature Coefficient				−100			−100		ppm/°C

ELECTRICAL CHARACTERISTICS

V_{DD} = 15V, V_{REF} = 10V, OUT 1 = OUT 2 = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		ALL GRADES MIN	TYP	MAX	UNIT
Power Supply							
V_{DD}	Operating Supply Range		●	5	15	16	V
I_{DD}	Suppy Current	Digital Inputs = V_{IH} or V_{IL}	●			2	mA
		Digital Inputs = 0V or V_{DD}	●			100	µA
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current		●		0.001	±1	µA
C_{IN}	Digital Input Capacitance	(Note 3), V_{IN} = 0V	●			8	pF
AC Performance							
	Propagation Delay	(Notes 5, 6)			100		ns
	Digital-to-Analog Glitch Impulse	(Notes 5, 7)			1000		nV-sec
	Multiplying Feedthrough Error	V_{REF} = ±10V, 10kHz Sinewave			1.0		mV_{P-P}
	Output Current Settling Time	(Note 5), To 0.01% for Full-Scale Change			0.6		µs
C_{OUT}	Output Capacitance (Note 3)	Digital Inputs = V_{IH} C_{OUT1}	●			200	pF
		C_{OUT2}	●			70	pF
		Digital Inputs = V_{IL} C_{OUT1}	●			70	pF
		C_{OUT2}	●			200	pF

The ● denotes specifications which apply over the full operating temperature range.

Note 1: ±0.5LSB = ±0.012% of full scale.

Note 2: Using internal feedback resistor.

Note 3: Guaranteed by design, not subject to test.

Note 4: I_{OUT1} with all digital inputs = 0V or I_{OUT2} with all digital inputs = V_{DD}.

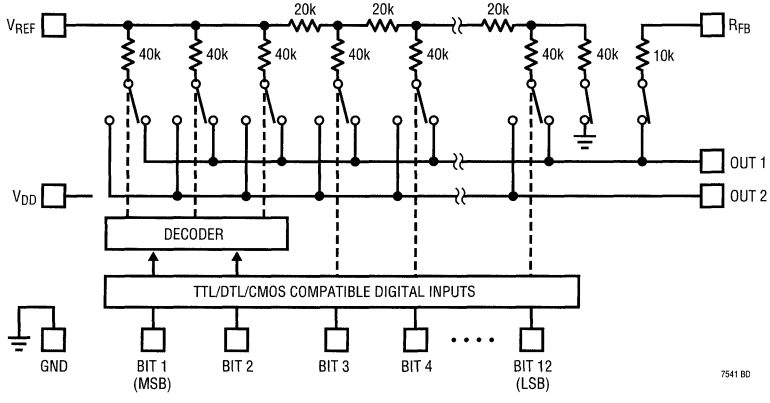
Note 5: OUT 1 load = 100Ω in parallel with 13pF.

Note 6: Measured from digital input change to 90% of final analog value. Digital inputs = 0V to V_{DD} or V_{DD} to 0V.

Note 7: V_{REF} = 0V. All digital inputs 0V to V_{DD} or V_{DD} to 0V. Measured using LT1363 as output amplifier.

6

BLOCK DIAGRAM



TYPICAL APPLICATIONS

Unipolar Operation (2-Quadrant Multiplication)

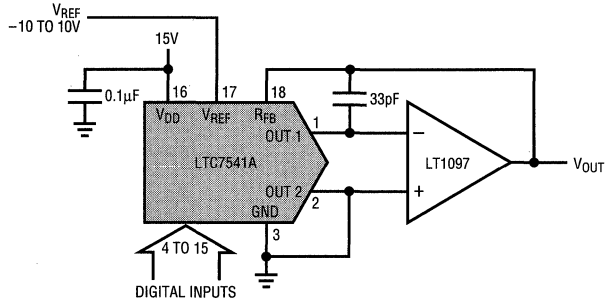


Table 1. Unipolar Binary Code Table

DIGITAL INPUT			ANALOG OUTPUT V_{OUT}
MSB		LSB	
1111	1111	1111	$-V_{REF}$ (4095/4096)
1000	0000	0000	$-V_{REF}$ (2048/4096) = $-V_{REF}/2$
0000	0000	0001	$-V_{REF}$ (1/4096)
0000	0000	0000	0V

7541 TA03

Bipolar Operation (4-Quadrant Multiplication)

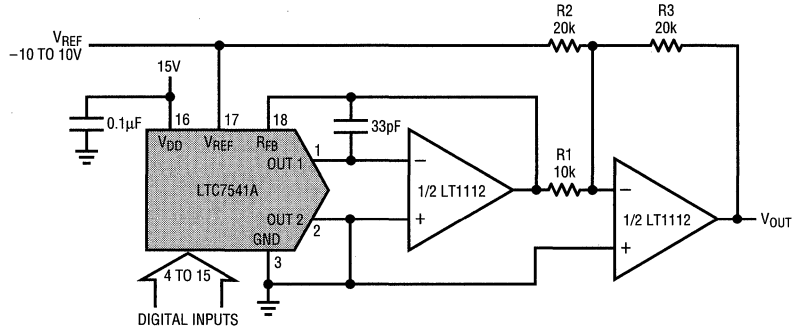


Table 2. Bipolar Offset Binary Code Table

DIGITAL INPUT			ANALOG OUTPUT V_{OUT}
MSB		LSB	
1111	1111	1111	V_{REF} (2047/2048)
1000	0000	0001	V_{REF} (1/2048)
1000	0000	0000	0V
0111	1111	1111	$-V_{REF}$ (1/2048)
0000	0000	0000	$-V_{REF}$

7541 TA04

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Complete Serial I/O V_{OUT} 12-Bit DAC	5V to 15V Single Supply in 8-Pin SO and PDIP
LTC1451/LTC1452/LTC1453	Complete Serial I/O V_{OUT} 12-Bit DACs	3V/5V Single Supply in 8-Pin SO and PDIP
LTC7543/LTC8143	Serial I/O Muliplying 12-Bit DACs	Clear Pin, Serial Data Output (LTC8143)
LTC8043	Serial Mulitplying 12-Bit DAC	8-Pin SO and PDIP

Improved Industry Standard Serial 12-Bit Multiplying DACs

FEATURES

- **Improved Direct Replacement for AD7543 and DAC-8143**
- **Low Cost**
- **DNL and INL Over Temperature: ±0.5LSB**
- Easy, Fast and Flexible Serial Interface
- Daisy-Chain 3-Wire Interface for Multiple DAC Systems (LTC8143)
- 1LSB Maximum Gain Error Over Temperature Eliminates Adjustment
- Asynchronous Clear Input for Initialization
- Four-Quadrant Multiplication
- Low Power Consumption
- 16-Pin PDIP and SO Packages

APPLICATIONS

- Process Control and Industrial Automation
- Remote Microprocessor-Controlled Systems
- Digitally Controlled Filters and Power Supplies
- Programmable Gain Amplifiers
- Automatic Test Equipment

DESCRIPTION

The LTC®7543/LTC8143 are serial-input 12-bit multiplying digital-to-analog converters (DACs). They are superior pin compatible replacements for the AD7543 and DAC-8143. Improvements include better accuracy, better stability over temperature and supply variations, lower sensitivity to output amplifier offset, tighter timing specifications and lower output capacitance.

An easy-to-use serial interface includes an asynchronous CLEAR input for systems requiring initialization to a known state. The LTC8143 has a serial data output to allow daisy-chaining multiple DACs on a 3-wire interface bus.

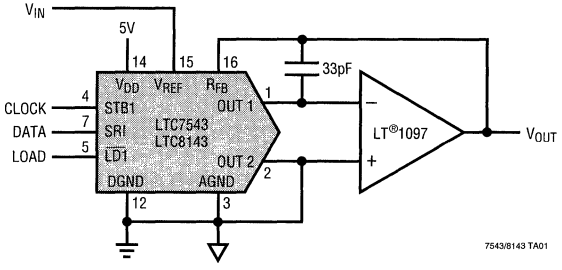
These DACs are extremely versatile. They can be used for 2-quadrant and 4-quadrant multiplying, programmable gain and single supply applications, such as noninverting voltage output and biased or offset ground mode.

Parts are available in 16-pin PDIP and SO packages and are specified over the extended industrial temperature range, –40°C to 85°C.

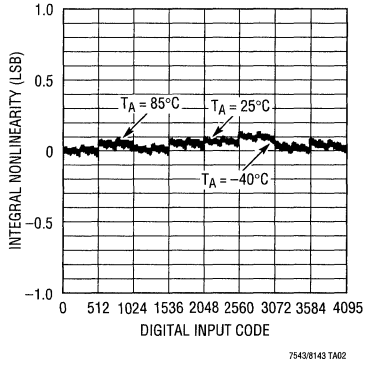
6

TYPICAL APPLICATION

Multiplying DAC Has Easy 3-Wire Serial Interface



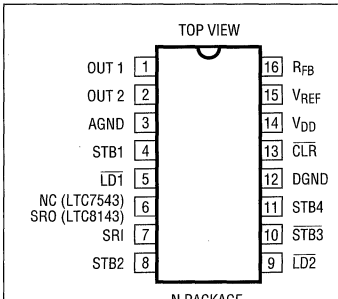
Integral Nonlinearity Over Temperature



ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... −0.5V to 7V
V_{DD} to DGND ..... −0.5V to 7V
AGND to DGND ..... V_{DD} + 0.5V
DGND to AGND ..... V_{DD} + 0.5V
Digital Inputs to DGND ..... −0.5V to (V_{DD} + 0.5V)
V_{OUT1}, V_{OUT2} to AGND ..... −0.5V to (V_{DD} + 0.5V)
V_{REF} to AGND, DGND ..... ±25V
V_{RFB} to AGND, DGND ..... ±25V
Maximum Junction Temperature ..... 150°C
Operating Temperature Range ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PDIP
SW PACKAGE
16-LEAD PLASTIC SO WIDE

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 130°C/W (SW)

ORDER PART NUMBER
LTC7543GKN
LTC7543KN
LTC7543GKSW
LTC7543KSW
LTC8143EN
LTC8143FN
LTC8143ESW
LTC8143FSW

Consult factory for Military grade parts.

ACCURACY CHARACTERISTICS – LTC7543

V_{DD} = 5V, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = DGND =0V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC7543GK MIN	LTC7543GK TYP	LTC7543GK MAX	LTC7543K MIN	LTC7543K TYP	LTC7543K MAX	UNITS
	Resolution		●	12			12			Bits
INL	Integral Nonlinearity (Relative Accuracy)	(Note 1)	●			±0.5			±0.5	LSB
DNL	Differential Nonlinearity	Guaranteed Monotonic, T_{MIN} to T_{MAX}	●			±0.5			±0.5	LSB
GE	Gain Error	(Note 2) T_A = 25°C				±1			±2	LSB
		T_{MIN} to T_{MAX}	●			±1			±2	LSB
	Gain Temperature Coefficient (ΔGain/ΔTemp)	(Note 3)	●		1	5		1	5	ppm/°C
I_{LKG}	Output Leakage Current	(Note 4) T_A = 25°C				±1			±1	nA
		T_{MIN} to T_{MAX}	●			±10			±10	nA
	Zero-Scale Error	T_A = 25°C				±0.006			±0.006	LSB
		T_{MIN} to T_{MAX}	●			±0.06			±0.06	LSB
PSRR	Power Supply Rejection Ratio	V_{DD} = 5V ±5%	●		±0.0001	±0.002		±0.0001	±0.002	%/%

ACCURACY CHARACTERISTICS – LTC8143

V_{DD} = 5V, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC8143E MIN	LTC8143E TYP	LTC8143E MAX	LTC8143F MIN	LTC8143F TYP	LTC8143F MAX	UNITS
	Resolution		●	12			12			Bits
INL	Integral Nonlinearity (Relative Accuracy)	(Note 1)	●			±0.5			±1	LSB
DNL	Differential Nonlinearity	Guaranteed Monotonic, T_{MIN} to T_{MAX}	●			±0.5			±1	LSB
GE	Gain Error	(Note 2) T_A = 25°C				±1			±2	LSB
		T_{MIN} to T_{MAX}	●			±2			±2	LSB
	Gain Temperature Coefficient (ΔGain/ΔTemp)	(Note 3)	●		1	5		1	5	ppm/°C
I_{LKG}	Output Leakage Current	(Note 4) T_A = 25°C				±5			±5	nA
		T_{MIN} to T_{MAX}	●			±25			±25	nA
	Zero-Scale Error	T_A = 25°C				±0.03			±0.03	LSB
		T_{MIN} to T_{MAX}	●			±0.15			±0.15	LSB
PSRR	Power Supply Rejection Ratio	V_{DD} = 5V ±5%	●		±0.0001	±0.002		±0.0001	±0.002	%/%

ELECTRICAL CHARACTERISTICS – LTC7543/LTC8143

V_{DD} = 5V, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS			LTC7543/LTC8143 ALL GRADES MIN	TYP	MAX	UNITS
Reference Input								
R_{REF}	V_{REF} Input Resistance	(Note 5)		●	8	11	15	kΩ
AC Performance (Note 3)								
	Output Current Settling Time	(Notes 6, 7)		●		0.25	1	µs
	Multiplying Feedthrough Error	V_{REF} = ±10V, 10kHz Sinewave		●		0.8	2	mV_{P-P}
	Digital-to-Analog Glitch Energy	(Notes 6, 8)		●		2	20	nV-sec
THD	Total Harmonic Distortion	(Note 9)		●		–108	–92	dB
	Output Noise Voltage Density	(Note 10)		●			13	nV/√Hz
Analog Outputs (Note 3)								
C_{OUT}	Output Capacitance	DAC Register Loaded to All 1s	C_{OUT1}	●		60	90	pF
			C_{OUT2}	●		20	60	pF
		DAC Register Loaded to All 0s	C_{OUT1}	●		30	60	pF
			C_{OUT2}	●		50	90	pF
Digital Inputs								
V_{IH}	Digital Input High Voltage			●	2.4			V
V_{IL}	Digital Input Low Voltage			●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}		●		0.001	±1	µA
C_{IN}	Digital Input Capacitance	(Note 3), V_{IN} = 0V		●			8	pF
Digital Outputs: SRO (LTC8143 Only)								
V_{OH}	Digital Output High	I_{OH} = –200µA		●	4			V
V_{OL}	Digital Output Low	I_{OL} = 1.6mA		●			0.4	V

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ELECTRICAL CHARACTERISTICS – LTC7543/LTC8143

V_{DD} = 5V, V_{REF} = 10V, V_{OUT1} = V_{OUT2} = AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC7543/LTC8143 ALL GRADES MIN	TYP	MAX	UNITS
Timing Characteristics (Note 3)							
t_{DS1}	Serial Input to Strobe Setup Time (t_{STB} = 80ns)	STB1 Used as the Strobe	●	50	5		ns
t_{DS2}		STB2 Used as the Strobe	●	20	–5		ns
t_{DS3}		$\overline{STB3}$ Used as the Strobe	●	0	–30		ns
t_{DS4}		STB4 Used as the Strobe	●	0	–30		ns
t_{DH1}	Serial Input to Strobe Hold Time (t_{STB} = 80ns)	STB1 Used as the Strobe	●	30	10		ns
t_{DH2}		STB2 Used as the Strobe	●	50	25		ns
t_{DH3}		$\overline{STB3}$ Used as the Strobe	●	80	55		ns
t_{DH4}		STB4 Used as the Strobe	●	80	55		ns
t_{SRI}	Serial Input Data Pulse Width		●	80			ns
t_{STB1}, t_{STB2}, t_{STB3}, t_{STB4}	Strobe Pulse Width	(Note 11)	●	80			ns
$t_{\overline{STB1}}$, $t_{\overline{STB2}}$, $t_{\overline{STB3}}$, $t_{\overline{STB4}}$	$\overline{Strobe}$ Pulse Width	(Note 12)	●	80			ns
t_{LD1}, t_{LD2}	Load Pulse Width		●	140			ns
t_{ASB}	LSB Strobed into Input Register to Load DAC Register Time		●	0			ns
t_{CLR}	Clear Pulse Width		●	80			ns
SRO Timing Characteristics (LTC8143 Only)							
t_{PD}	STB2, $\overline{STB3}$, STB4 Strobe to SRO Propagation Delay	C_L = 50pF	●	220	120		ns
t_{PD1}	STB1 to SRO Propagation Delay	C_L = 50pF	●	150	80		ns
Power Supply							
V_{DD}	Supply Voltage		●	4.75	5	5.25	V
I_{DD}	Supply Current	Digital Inputs = 0V or V_{DD}	●			0.1	mA
		Digital Inputs = V_{IH} or V_{IL}	●			2	mA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: ±0.5LSB = ±0.012% of full scale.

Note 2: Using internal feedback resistor.

Note 3: Guaranteed by design, not subject to test.

Note 4: I_{OUT1} with DAC register loaded with all 0s or I_{OUT2} with DAC register loaded with all 1s.

Note 5: Typical temperature coefficient is 100ppm/°C.

Note 6: OUT 1 load = 100Ω in parallel with 13pF.

Note 7: To 0.01% for a full-scale change, measured from falling edge of $\overline{LD1}$ or $\overline{LD2}$.

Note 8: V_{REF} = 0V. DAC register contents changed from all 0s to all 1s or from all 1s to all 0s.

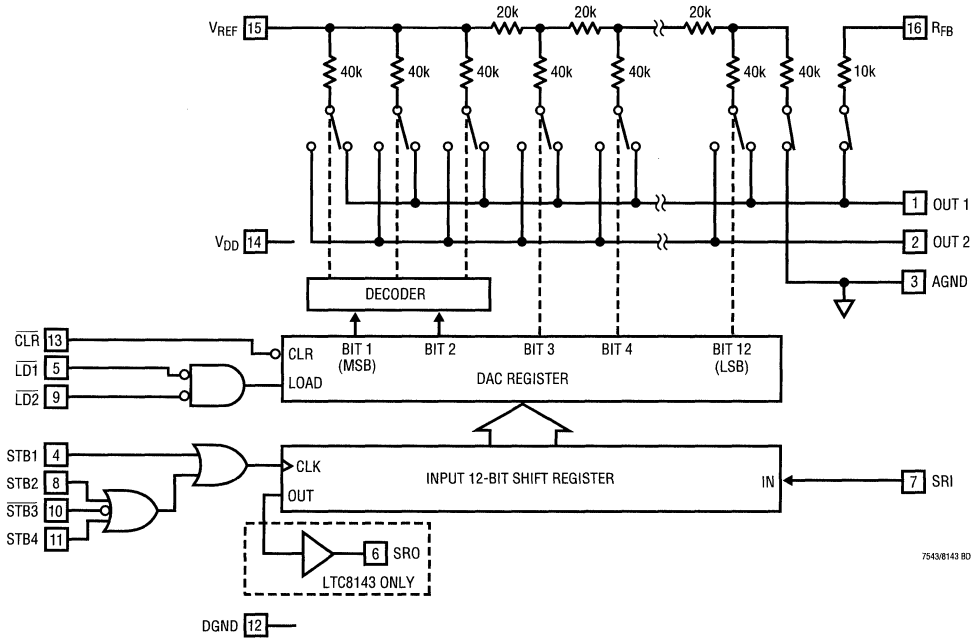
Note 9: V_{REF} = $6V_{RMS}$ at 1kHz. DAC register loaded with all 1s.

Note 10: Calculation from $e_n = \sqrt{4KTRB}$ where: K = Boltzmann constant (J/K°); R = resistance (Ω); T = resistor temperature (°K); B = bandwidth (Hz).

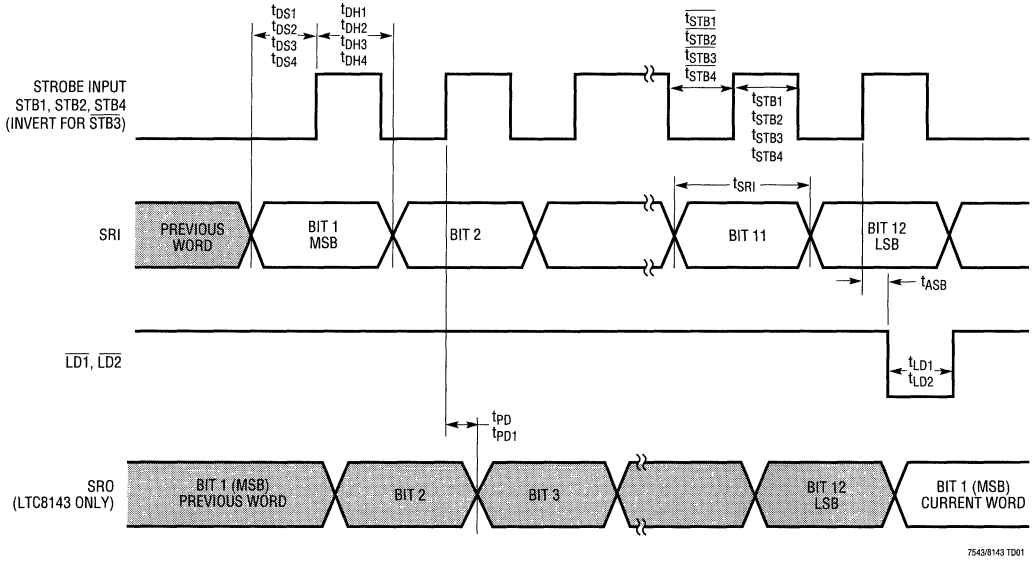
Note 11: Minimum high time for STB1, STB2, STB4. Minimum low time for $\overline{STB3}$.

Note 12. Minimum low time for STB1, STB2, STB4. Minimum high time for $\overline{STB3}$.

BLOCK DIAGRAM



TIMING DIAGRAM



TRUTH TABLES

Table 1. LTC7543/LTC8143 Input Register

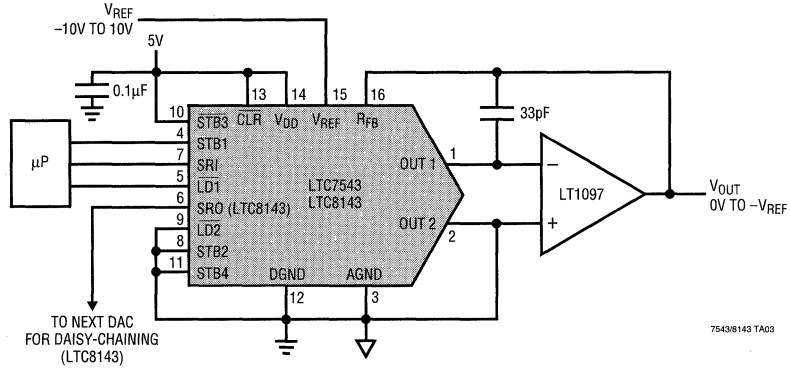
CONTROL INPUTS				Input Register Operation
STB1	STB2	$\overline{STB3}$	STB4	(LTC8143: SRO Operation)
↓	0	1	0	Serial Data Bit on SRI Loaded into Input Register, MSB First (LTC8143: Data Bit or SRI Appears on SRO Pin After 12 Clocked Bits)
0	↓	1	0	
0	0	↓	0	
0	0	1	↓	
1	X	X	X	No Input Register Operation (LTC8143: No SRO Operation)
X	1	X	X	
X	X	0	X	
X	X	X	1	

Table 2. LTC7543/LTC8143 DAC Register

CONTROL INPUTS			
$\overline{CLR}$	$\overline{LD1}$	$\overline{LD2}$	DAC Register Operation
0	X	X	Reset DAC Register to All 0s (Asynchronous Operation; No Effect on Input Register)
1	1	X	No DAC Register Operation
1	X	1	
1	0	0	Load DAC Register with the Contents of Input Register

TYPICAL APPLICATIONS

Unipolar Operation (2-Quadrant Multiplication)

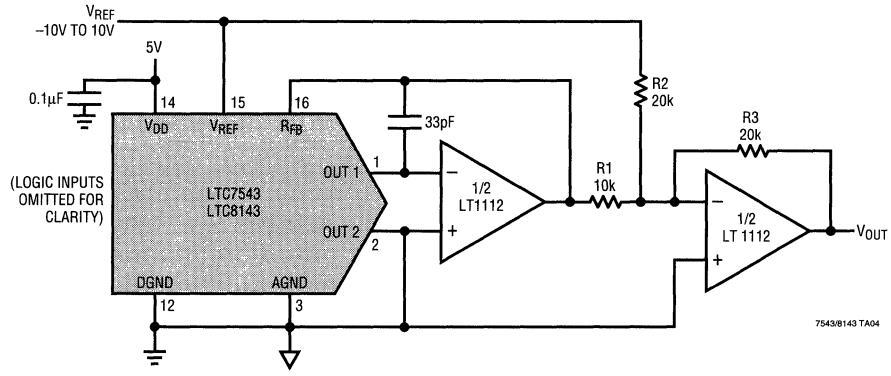


Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT V_{OUT}
MSB		LSB	
1111	1111	1111	$-V_{REF}$ (4095/4096)
1000	0000	0000	$-V_{REF}$ (2048/4096) = $-V_{REF}/2$
0000	0000	0001	$-V_{REF}$ (1/4096)
0000	0000	0000	0V

TYPICAL APPLICATIONS

Bipolar Operation (4-Quadrant Multiplication)



Bipolar Offset Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT V_{OUT}
MSB		LSB	
1111	1111	1111	V_{REF} (2047/2048)
1000	0000	0001	V_{REF} (1/2048)
1000	0000	0000	0V
0111	1111	1111	$-V_{REF}$ (1/2048)
0000	0000	0000	$-V_{REF}$ (2048/2048) = $-V_{REF}$

6

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Complete Serial I/O V_{OUT} 12-Bit DAC	5V to 15V Single Supply in 8-Pin SO and PDIP
LTC1451/LTC1452/LTC1453	Complete Serial I/O V_{OUT} 12-Bit DACs	3V/5V Single Supply in 8-Pin SO and PDIP
LTC7541A	Parallel I/O Mulitplying 12-Bit DAC	12-Bit Wide Input
LTC8043	Serial Mulitplying 12-Bit DAC	8-Pin SO and PDIP

Serial 12-Bit Multiplying DAC in SO-8

FEATURES

- Improved Direct Replacement for DAC-8043 and MAX543
- **SO-8 Package**
- **DNL and INL Over Temperature: ±0.5LSB**
- Easy, Fast and Flexible Serial Interface
- **±1LSB Maximum Gain Error**
- 4-Quadrant Multiplication
- Low Power Consumption
- Low Cost

APPLICATIONS

- Process Control and Industrial Automation
- Remote Microprocessor-Controlled Systems
- Digitally Controlled Filters and Power Supplies
- Programmable Gain Amplifiers
- Automatic Test Equipment

DESCRIPTION

The LTC®8043 is a serial-input 12-bit multiplying digital-to-analog converter (DAC). It is a superior pin compatible replacement for the DAC-8043. Improvements include better accuracy, better stability over temperature and supply variations, lower sensitivity to output amplifier offset, tighter timing specifications and lower output capacitance.

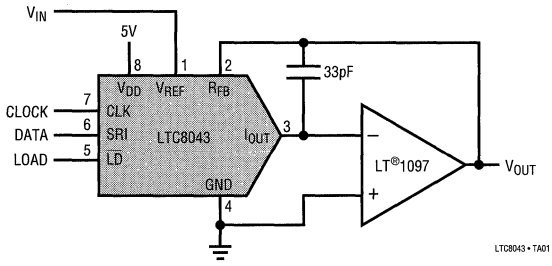
An easy-to-use 3-wire serial interface is well-suited to remote or isolated applications

The LTC8043 is extremely versatile. It can be used for 2-quadrant and 4-quadrant multiplying, programmable gain and single supply applications, such as noninverting voltage output mode.

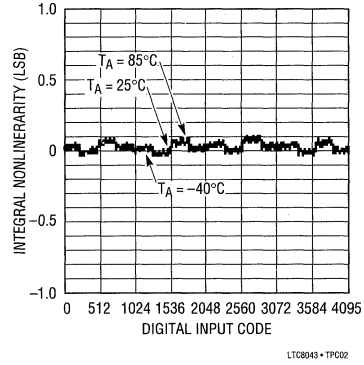
Parts are available in 8-pin SO and PDIP packages and are specified over the extended industrial temperature range, –40°C to 85°C.

TYPICAL APPLICATION

SO-8 Multiplying DAC Has Easy 3-Wire Serial Interface



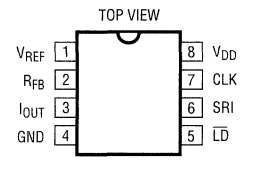
Integral Nonlinearity Over Temperature



ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... −0.5V to 7V
Digital Inputs to GND ..... −0.5V to (V_{DD} + 0.5V)
V_{IOUT} to GND ..... −0.5V to (V_{DD} + 0.5V)
V_{REF} to GND ..... ±25V
V_{RFB} to GND ..... ±25V
Maximum Junction Temperature ..... 150°C
Operating Temperature Range ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/ W (N8)
T_{JMAX} = 150°C, θ_{JA} = 190°C/ W (S8)

ORDER PART NUMBER
LTC8043EN8
LTC8043FN8
LTC8043ES8
LTC8043FS8

Consult factory for Military grade parts.

ACCURACY CHARACTERISTICS

V_{DD} = 5V, V_{REF} = 10V, V_{IOUT} = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		LTC8043E MIN	LTC8043E TYP	LTC8043E MAX	LTC8043F MIN	LTC8043F TYP	LTC8043F MAX	UNITS
	Resolution		●	12			12			Bits
INL	Integral Nonlinearity	(Note 1)	●			±0.5			±1	LSB
DNL	Differential Nonlinearity	Guaranteed Monotonic, T_{MIN} to T_{MAX}	●			±0.5			±1	LSB
GE	Gain Error	(Note 2) T_A = 25°C				±1			±2	LSB
		T_{MIN} to T_{MAX}	●			±2			±2	LSB
	Gain Temperature Coefficient (ΔGain/ΔTemp)	(Note 3)	●		1	5		1	5	ppm/°C
I_{LKG}	Output Leakage Current	(Note 4) T_A = 25°C				±5			±5	nA
		T_{MIN} to T_{MAX}	●			±25			±25	nA
	Zero-Scale Error	T_A = 25°C				±0.03			±0.03	LSB
		T_{MIN} to T_{MAX}	●			±0.15			±0.15	LSB
PSRR	Power Supply Rejection Ratio	V_{DD} = 5V ±5%	●		±0.0001	±0.002		±0.0001	±0.002	%/%

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{REF} = 10V, V_{IOUT} = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		ALL GRADES MIN	ALL GRADES TYP	ALL GRADES MAX	UNITS
Reference Input							
R_{REF}	V_{REF} Input Resistance	(Note 5)	●	7	11	15	kΩ
AC Performance (Note 3)							
	Output Current Settling Time	(Notes 6, 7)	●		0.25	1	µs
	Multiplying Feedthrough Error	V_{REF} = ±10V, 10kHz Sinewave	●		0.7	1	mV_{P-P}
	Digital-to-Analog Glitch Energy	(Notes 6, 8)	●		2	20	nVSEC
THD	Total Harmonic Distortion	(Note 9)	●		−108	−92	dB
	Output Noise Voltage Density	(Note 10)	●			17	nV/√Hz
Analog Outputs (Note 3)							
C_{OUT}	Output Capacitance	DAC Register Loaded to All 1s	●		60	90	pF
		DAC Register Loaded to All 0s	●		30	60	pF

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, V_{REF} = 10V, V_{IOUT} = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		ALL GRADES MIN	TYP	MAX	UNITS
Digital Inputs							
V_{IH}	Digital Input High Voltage		●	2.4			V
V_{IL}	Digital Input Low Voltage		●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●		0.001	±1	µA
C_{IN}	Digital Input Capacitance	V_{IN} = 0V,(Note 3)	●			8	pF
Timing Characteristics (Note 3)							
t_{DS}	Serial Input to Clock Setup Time		●	30	–5		ns
t_{DH}	Serial Input to Clock Hold Time		●	60	25		ns
t_{SRI}	Serial Input Data Pulse Width		●	80			ns
t_{CH}	Clock Pulse Width High		●	80			ns
t_{CL}	Clock Pulse Width Low		●	80			ns
t_{LD}	Load Pulse Width		●	140			ns
t_{ASB}	LSB Clocked into Input Register to Load DAC Register Time		●	0			ns
Power Supply							
V_{DD}	Supply Voltage		●	4.75	5	5.25	V
I_{DD}	Supply Current	Digital Inputs = 0V or V_{DD} Digital Inputs = V_{IH} or V_{IN}	● ●			100 500	µA µA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: ±0.5LSB = ±0.012% of full scale.

Note 2: Using internal feedback resistor.

Note 3: Guaranteed by design, not subject to test.

Note 4: I_{OUT} with DAC register loaded with all 0s.

Note 5: Typical temperature coefficient is 100ppm/°C.

Note 6: I_{OUT} load = 100Ω in parallel with 13pF.

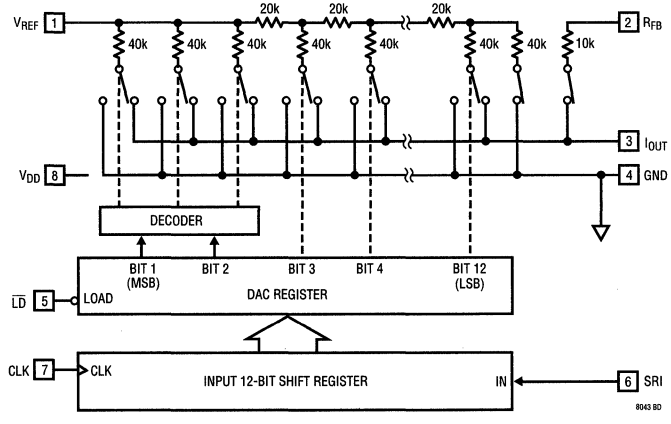
Note 7: To 0.01% for a full-scale change, measured from falling edge of $\overline{LD}$.

Note 8: V_{REF} = 0V. DAC register contents changed from all 0s to all 1s or from all 1s to all 0s.

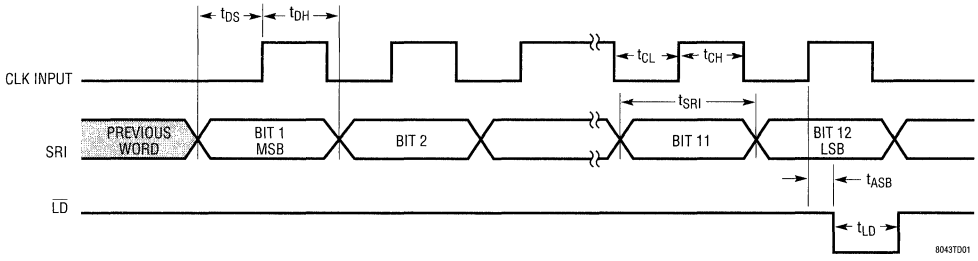
Note 9: V_{REF} = $6V_{RMS}$ at 1kHz. DAC register loaded with all 1s.

Note 10: 10Hz to 100kHz between R_{FB} and I_{OUT}. Calculation from e_n = $\sqrt{4KTRB}$ where: K = Boltzmann constant (J/K°); R = resistance (Ω); T = resistor temperature (°K); B = bandwidth (Hz).

BLOCK DIAGRAM



TIMING DIAGRAM



TYPICAL APPLICATIONS

Unipolar Operation (2-Quadrant Multiplication)

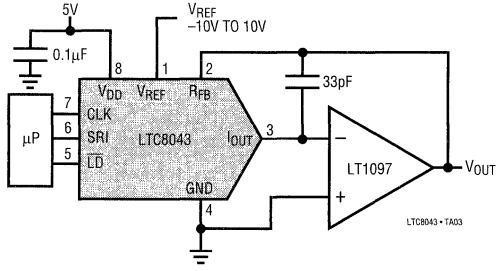


Table 1. Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT V_{OUT}
MSB		LSB	
1111	1111	1111	$-V_{REF}$ (4095/4096)
1000	0000	0000	$-V_{REF}$ (2048/4096) = $-V_{REF}/2$
0000	0000	0001	$-V_{REF}$ (1/4096)
0000	0000	0000	0V

Bipolar Operation (4-Quadrant Multiplication)

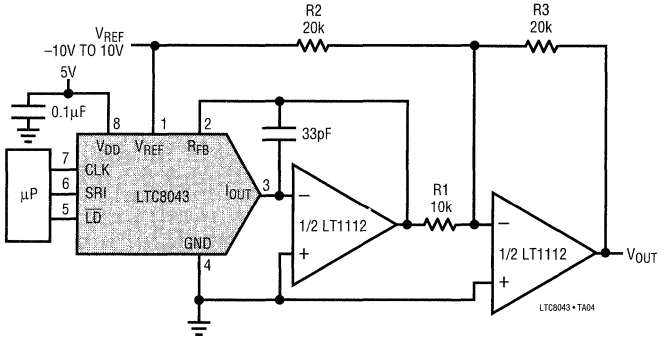


Table 2. Bipolar Offset Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT V_{OUT}
MSB		LSB	
1111	1111	1111	$+V_{REF}$ (2047/2048)
1000	0000	0001	$+V_{REF}$ (1/2048)
1000	0000	0000	0V
0111	1111	1111	$-V_{REF}$ (1/2048)
0000	0000	0000	$-V_{REF}$ (2048/2048) = $-V_{REF}$

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Complete Serial I/O V_{OUT} 12-Bit DAC	5V to 15V Single Supply in 8-Pin SO and PDIP
LTC1451/LTC1452/LTC1453	Complete Serial I/O V_{OUT} 12-Bit DACs	3V/5V Single Supply in 8-Pin SO and PDIP
LTC7541A	Parallel I/O Multiplying 12-Bit DAC	12-Bit Wide Input
LTC7543/LTC8143	Serial I/O Mulitplying 12-Bit DACs	Clear Pin and Serial Data Output (LTC8143)

SECTION 6—DATA CONVERSION

MULTIPLEXERS

8-Channel Analog Multiplexer with Serial Interface

FEATURES

- **3-Wire Serial Digital Interface**
- Data Retransmission Allows Series Connection with Serial A/D Converters
- **Single 3V to ±5V Supply Operation**
- Analog Inputs May Extend to Supply Rails
- **Low Charge Injection**
- Low R_{ON}: 75Ω Max
- Low Leakage: ±5nA Max
- Guaranteed Break-Before-Make
- TTL/CMOS Compatible for All Digital Inputs
- Cascadable to Allow Additional Channels
- Can Be Used as a Demultiplexer

APPLICATIONS

- Data Acquisition Systems
- Communication Systems
- Signal Multiplexing/Demultiplexing

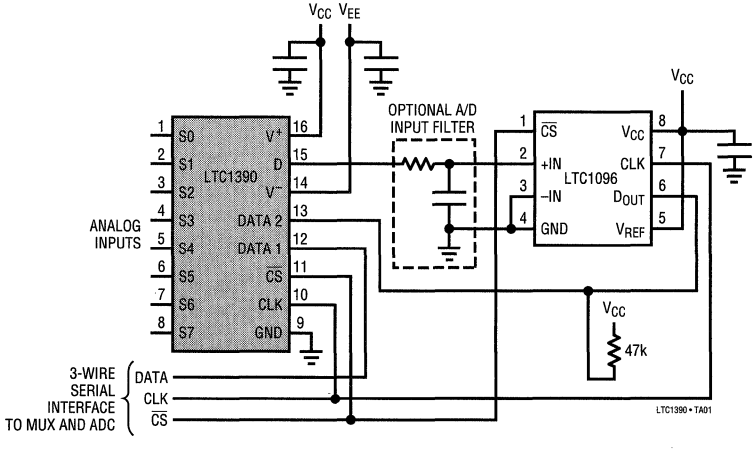
DESCRIPTION

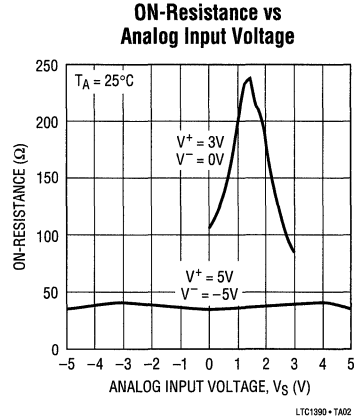
The LTC®1390 is a high performance CMOS 8-to-1 analog multiplexer. It features a 3-wire digital interface with a bidirectional data retransmission feature, allowing it to be wired in series with a serial A/D converter while using only one serial port. The interface also allows several LTC1390s to be wired in series or parallel, increasing the number of MUX channels available using only a single digital port. All the above features are also valid when LTC1390 operates as a demultiplexer such as with a D/A converter.

The LTC1390 features a typical R_{ON} of 45Ω, typical switch leakage of 50pA, and guaranteed break-before-make operation. Charge injection is ±10pC maximum. All digital inputs are TTL and CMOS compatible when operated from single or dual supplies. The inputs can withstand 100mA fault currents.

The LTC1390 is available in 16-pin PDIP and narrow SO packages.

TYPICAL APPLICATION



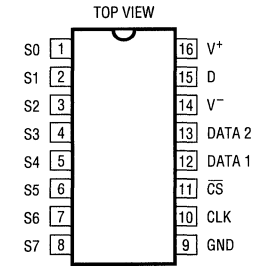


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 15V
Input Voltage
  Analog Inputs ..... V^- – 0.3V to V^+ + 0.3V
  Digital Inputs ..... –0.3V to 15V
  Digital Outputs ..... –0.3V to V^+ + 0.3V
Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PDIP

S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (S)

ORDER PART NUMBER
LTC1390CN
LTC1390CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V^+ = 5V, V^- = –5V, GND = 0V, T_A = operating temperature unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch							
V_{ANALOG}	Analog Signal Range	(Note 2)	●	–5		5	V
R_{ON}	On Resistance	V_S = ±3.5V, I_D = 1mA					
		T_{MIN}				75	Ω
		25°C			45	75	Ω
		T_{MAX}				120	Ω
	ΔR_{ON} vs V_S				20		%
	ΔR_{ON} vs Temperature				0.5		%/°C
$I_{S(OFF)}$	Off Input Leakage	V_S = 4V, V_D = –4V; V_S = –4V, V_D = 4V			0.05	±5	nA
		Channel Off	●			±50	nA
$I_{D(OFF)}$	Off Output Leakage	V_S = 4V, V_D = –4V; V_S = –4V, V_D = 4V			0.05	±5	nA
		Channel Off	●			±50	nA
$I_{D(ON)}$	On Channel Leakage	V_S = V_D = ±4V			0.05	±5	nA
		Channel On	●			±50	nA
Input							
V_{INH}	High Level Input Voltage	V^+ = 5.25V	●	2.4			V
V_{INL}	Low Level Input Voltage	V^+ = 4.75V	●			0.8	V
I_{INL}, I_{INH}	Low or High Level Current	V_{IN} = 5V, V_{IN} = 0V	●			±1	µA
V_{OH}	High Level Output Voltage	V^+ = 4.75V, I_O = 10µA			4.74		V
		V^+ = 4.75V, I_O = 360µA	●	2.4	4.50		V
V_{OL}	Low Level Output Voltage	V^+ = 4.75V, I_O = 0.5mA	●		0.16	0.8	V

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ELECTRICAL CHARACTERISTICS

V^+ = 5V, V^- = −5V, GND = 0V, T_A = operating temperature unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Dynamic							
f_{CLK}	Clock Frequency					5	MHz
t_{ON}	Enable Turn-On Time	V_S = 2.5V, R_L = 1k, C_L = 35pF			260	400	ns
t_{OFF}	Enable Turn-Off Time	V_S = 2.5V, R_L = 1k, C_L = 35pF			100	200	ns
t_{OPEN}	Break-Before-Make Interval			35	155		ns
OIRR	Off Isolation	$V_S = 2V_{P-P}$, R_L = 1k, f = 100kHz			70		dB
O_{INJ}	Charge Injection	R_S = 0, C_L = 1000pF, V_S = 1V (Note 2)			±2	±10	pC
$C_{S(OFF)}$	Source Off Capacitance				5		pF
$C_{D(OFF)}$	Drain Off Capacitance				10		pF
Supply							
I^+	Positive Supply Current	All Logic Inputs Tied Together, V_{IN} = 0V or V_{IN} = 5V	●		15	40	µA
I^-	Negative Supply Current	All Logic Inputs Tied Together, V_{IN} = 0V or V_{IN} = 5V	●		15	40	µA

V^+ = 3V, V^- = GND = 0V, T_A = operating temperature unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch							
V_{ANALOG}	Analog Signal Range	(Note 2)	●	0		3	V
R_{ON}	On Resistance	V_S = 1.2V, I_D = 1mA					
		T_{MIN}				255	Ω
		25°C			200	255	Ω
		T_{MAX}				300	Ω
	ΔR_{ON} vs V_S				20		%
	ΔR_{ON} vs Temperature				0.5		%/°C
$I_{S(OFF)}$	Off Input Leakage	V_S = 2.5V, V_D = 0.5V; V_S = 0.5V, V_D = 2.5V (Note 3)			±0.05	±5	nA
		Channel Off	●			±50	nA
$I_{D(OFF)}$	Off Output Leakage	V_S = 2.5V, V_D = 0.5V; V_S = 0.5V, V_D = 2.5V (Note 3)			±0.05	±5	nA
		Channel Off	●			±50	nA
$I_{D(ON)}$	On Channel Leakage	$V_S = V_D$ = 0.5V, $V_S = V_D$ = 2.5V (Note 3)			±0.05	±5	nA
		Channel On	●			±50	nA
Input							
V_{INH}	High Level Input Voltage	V^+ = 3.3V	●	2.4			V
V_{INL}	Low Level Input Voltage	V^+ = 2.7V	●			0.8	V
I_{INL}, I_{INH}	Low or High Level Current	V_{IN} = 3V, V_{IN} = 0V	●			±1	µA
V_{OH}	High Level Output Voltage	V^+ = 2.7V, I_O = 20µA			2.68		V
		V^+ = 2.7V, I_O = 400µA	●	2	2.27		V
V_{OL}	Low Level Output Voltage	V^+ = 2.7V, I_O = 20µA			0.01		V
		V^+ = 2.7V, I_O = 300µA	●		0.15	0.8	V

ELECTRICAL CHARACTERISTICS

/+ = 3V, V⁻ = GND = 0V, T_A = operating temperature unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
)ynamic							
CLK	Clock Frequency					5	MHz
ON	Enable Turn-On Time	V_S = 1.5V, R_L = 1k, C_L = 35pF (Note 4)			490	700	ns
OFF	Enable Turn-Off Time	V_S = 1.5V, R_L = 1k, C_L = 35pF (Note 4)			190	300	ns
OPEN	Break-Before-Make Interval	(Note 4)		125	290		ns
)IRR	Off Isolation	$V_S = 2V_{P-P}$, R_L = 1k, f = 100kHz			70		dB
$)_{INJ}$	Charge Injection	R_S = 0, C_L = 1000pF, V_S = 1V (Note 2)			±1	±5	pC
$'_{S(OFF)}$	Source Off Capacitance				5		pF
$'_{D(OFF)}$	Drain Off Capacitance				10		pF
;upply							
+	Positive Supply Current	All Logic Inputs Tied Together, V_{IN} = 0V or V_{IN} = 3V	●		0.2	2	µA

'he ● denotes specifications which apply over the full operating emperature range.

lote 1: Absolute maximum ratings are those beyond which the safety of he device may be impaired.

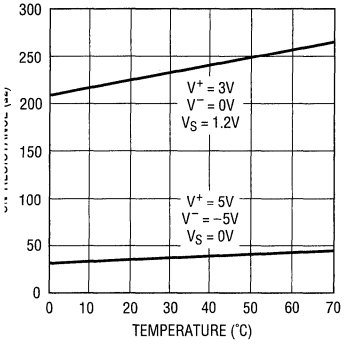
lote 2: Guaranteed by design.

Note 3: Leakage current with a single 3V supply is guaranteed by correlation with the leakage current of the ±5V supply.

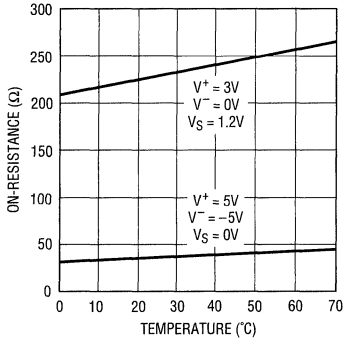
Note 4: Timing specifications with a single 3V supply is guaranteed by correlation with the timing specifications of the ±5V supply.

TYPICAL PERFORMANCE CHARACTERISTICS

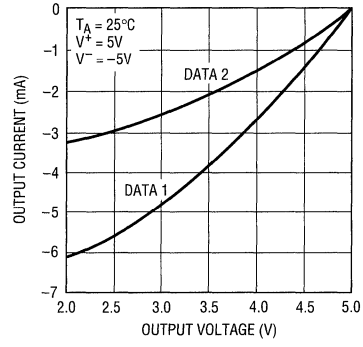
ON-Resistance vs Temperature



Driver Output Low Voltage vs Output Current



Driver Output High Voltage vs Output Current



6

PIN FUNCTIONS

S0 to S7 (Pins 1 to 8): Analog Multiplexer Inputs/Analog Demultiplexer Outputs.

GND (Pin 9): Digital Ground. Connect to system ground.

CLK (Pin 10): System Clock (TTL/CMOS Compatible). The clock synchronizes the channel selection bits and the serial data transfer from Data 1 to Data 2.

$\overline{CS}$ (Pin 11): Chip Select Input (TTL/CMOS Compatible). A logic high on this input enables LTC1390 to read in the channel selection bits and allow data transfer from Data 1 to Data 2. A logic low enables the desired channel for analog signal transmission and allows data transfer from Data 2 to Data 1.

Data 1 (Pin 12): Bidirectional Digital Input/Output (TTL/CMOS Compatible). Input for the channel selection bits.

Data 2 (Pin 13): Bidirectional Digital Input/Output (TTL/CMOS Compatible).

V^- (Pin 14): Negative Supply.

D (Pin 15): Analog Multiplexer Output/Analog Demultiplexer Input.

V^+ (Pin 16): Positive Supply.

APPLICATIONS INFORMATION

Multiplexer Operation

Figure 1 shows the block diagram of the components within the LTC1390 required for MUX operation. The LTC1390 uses Data 1 to select its 8 channels and a chip select input $\overline{CS}$ to switch on the selected channel as shown in Figure 2.

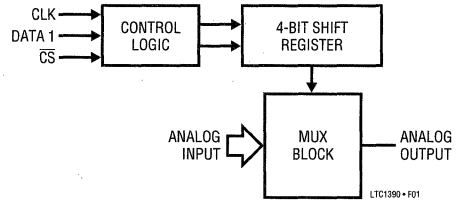


Figure 1: Simplified Block Diagram of the MUX Operation

When $\overline{CS}$ is high, the input data on the Data 1 pin is latched into the 4-bit shift register on each rising clock edge. The input data consists of an "EN" bit and a string of three bits for channel selection. If "EN" bit is logic high as illustrated in the first input data sequence, it enables the selected channel. To ensure correct operation, the $\overline{CS}$ must be pulled low before the next rising clock edge.

Once the $\overline{CS}$ is pulled low, all channels are simultaneously switched off to ensure a break-before-make interval. After a delay of t_{ON}, the selected channel is switched on allowing signal transmission. The selected channel remains on until the next falling edge of $\overline{CS}$, and after a delay of t_{OFF}, it terminates the analog signal transmission and subsequently allows the selection of the next channel. If "EN" bit is logic low, as illustrated in the second data sequence, it disables all channels and there will be no analog signal

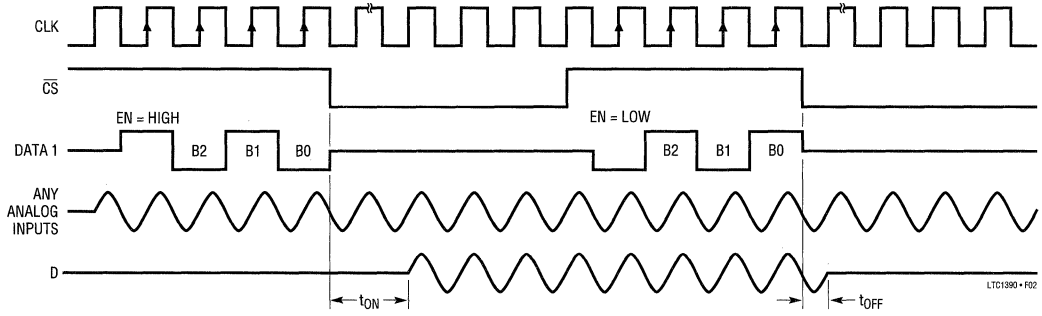


Figure 2: Multiplexer Operation

APPLICATIONS INFORMATION

transmission. Table 1 shows the various bit combinations for channel selection.

Table 1. Logic Table for Channel Selection

CHANNEL STATUS	EN	B2	B1	B0
All Off	0	X	X	X
S0	1	0	0	0
S1	1	0	0	1
S2	1	0	1	0
S3	1	0	1	1
S4	1	1	0	0
S5	1	1	0	1
S6	1	1	1	0
S7	1	1	1	1

Digital Data Transfer Operation

The block diagram of Figure 3 shows the components contained within the LTC1390 required for digital data transfer. Digital data transfer operation can be performed from Data 1 to Data 2 and vice versa as shown in Figure 4. When $\overline{CS}$ is high, Buffer 1 is enabled and Buffer 2 is disabled. The digital input data is fed into the 4-bit shift register and then shifted to the MUX switches for channel selection or to Data 2 via Buffer 1 for data transfer. Data appears at Data 2 after the fourth rising edge of the clock. When $\overline{CS}$ is low, Buffer 2 is enabled and Buffer 1 is disabled, thus digital input data is directly transferred from Data 2 to Data 1 without any clock delay.

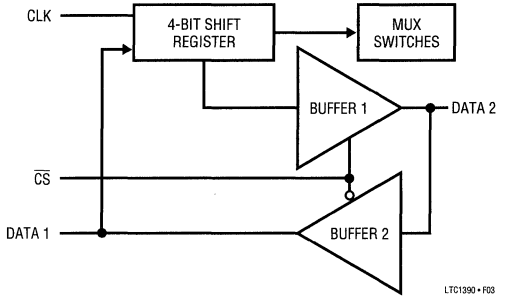


Figure 3. Simplified Block Diagram of the Digital Data Transfer Operation

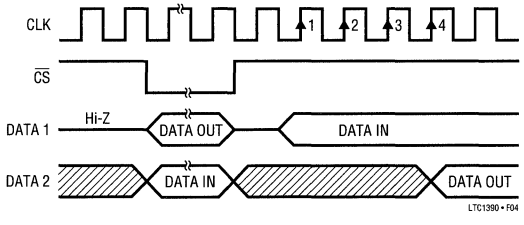


Figure 4. Digital Data Transfer Operation

Multiplexer Expansion

Several LTC1390s can be daisy-chained to expand the number of multiplexer inputs. No additional interface ports are required for the expansion. Figure 5 shows two LTC1390s connected at their analog outputs to form a 16-to-1 multiplexer at the input to an LTC1286 A/D converter.

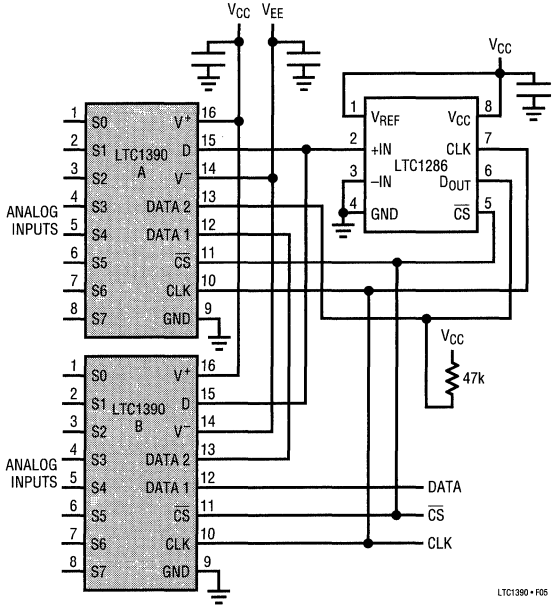


Figure 5. Daisy-Chaining Two LTC1390s for Expansion

To ensure that only one channel is switched on at any one time, two sets of channel selection bits are needed for Data as shown in Figure 6. The first data sequence is used to switch off one MUX and the second data sequence is used to select one channel from the other MUX, or vice versa. In other words, if bit "ENA" is high and bit "ENB" is low, one channel of MUX A is switched on and all channels of MUX B are switched off. If bit "ENA" is low and bit "ENB" is high, all channels of MUX A are switched off and one channel of MUX B is switched on.

APPLICATIONS INFORMATION

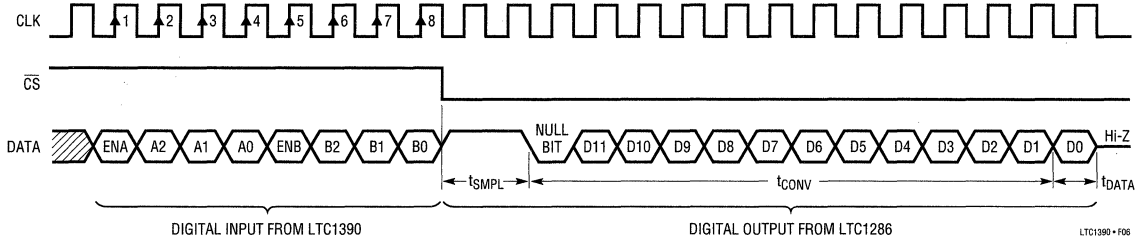
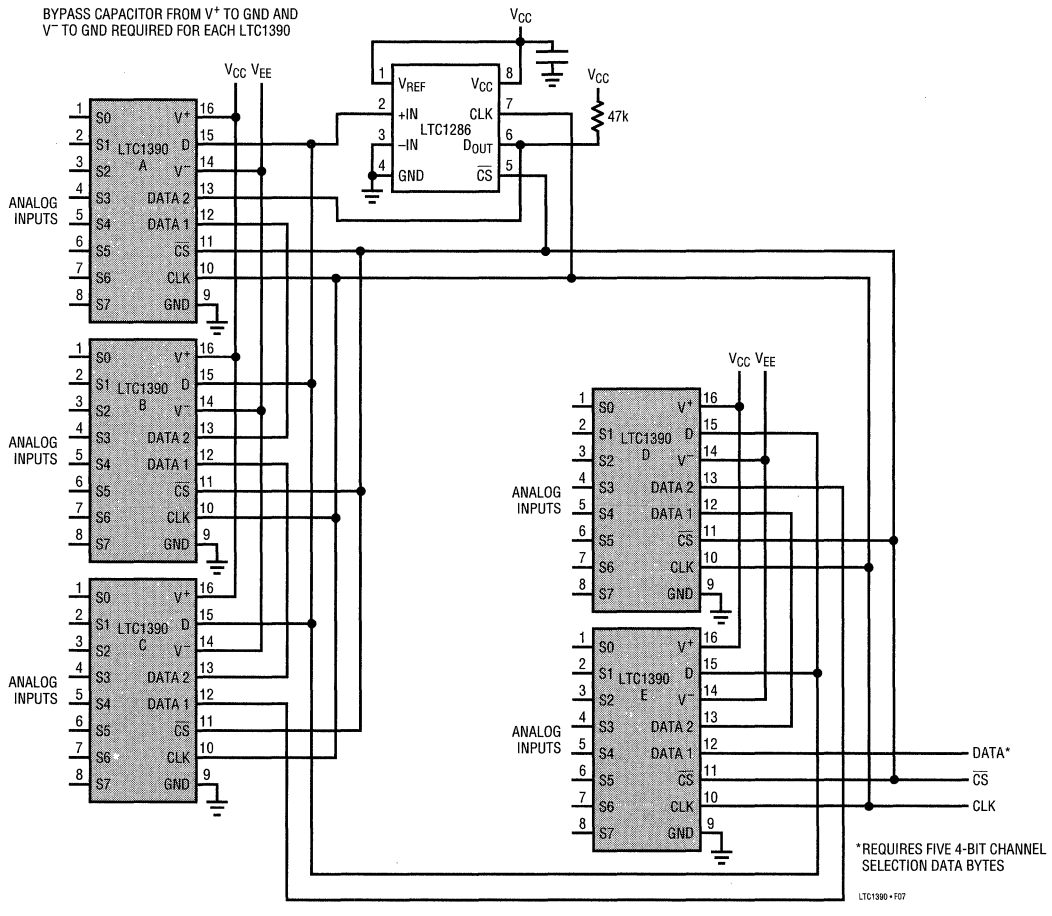


Figure 6. Timing Diagram for Figure 5

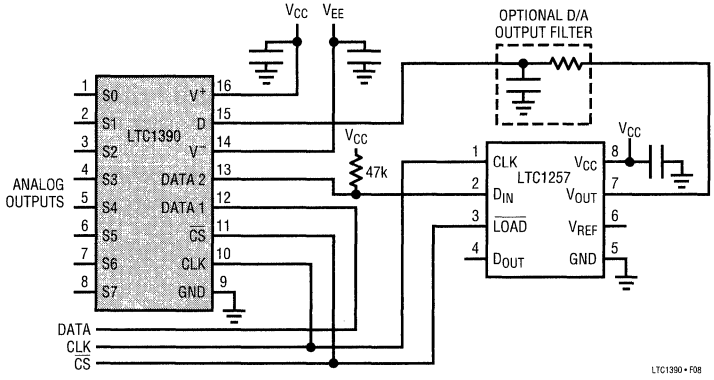
TYPICAL APPLICATIONS

Daisy-Chaining Five LTC1390s



TYPICAL APPLICATIONS

Interfacing LTC1390 with LTC1257 for Demultiplex Operation



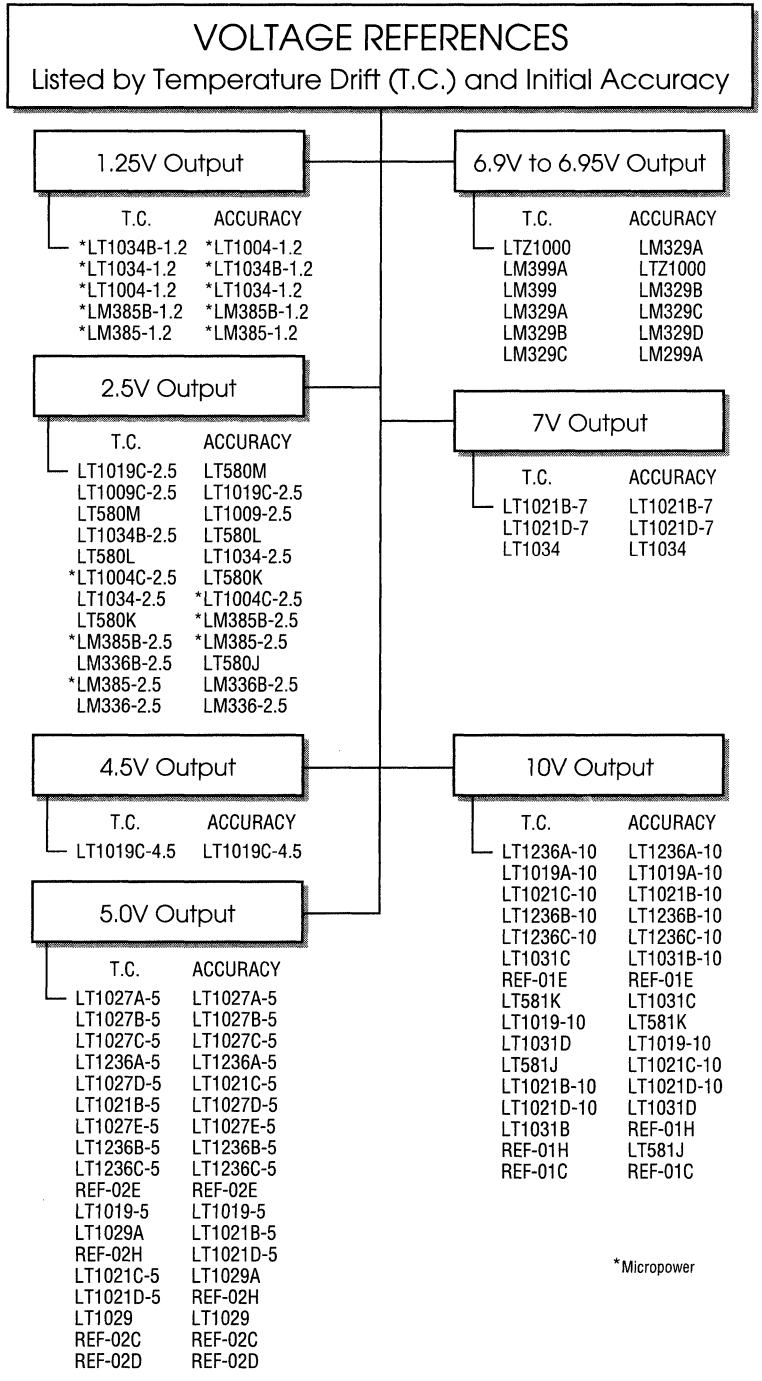
RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC201A/LTC202/LTC203	Micropower, Low Charge Injection, Quad CMOS Analog Switches	Each Channel is Independently Controlled
LTC221/LTC222	Micropower, Low Charge Injection, Quad CMOS Analog Switches with Data Latches	Parallel Controlled with Data Latches
LTC128x/LTC129x	Serial A/Ds with Integral MUXs	

6

SECTION 7—VOLTAGE REFERENCES

SECTION 7—VOLTAGE REFERENCES


VOLTAGE REFERENCES
Listed by Temperature Drift (T.C.) and Initial Accuracy
1.25V Output
T.C.
ACCURACY
*LT1034B-1.2
*LT1034-1.2
*LT1004-1.2
*LM385B-1.2
*LM385-1.2
*LT1004-1.2
*LT1034B-1.2
*LT1034-1.2
*LM385B-1.2
*LM385-1.2
2.5V Output
T.C.
ACCURACY
LT1019C-2.5
LT1009C-2.5
LT580M
LT1034B-2.5
LT580L
*LT1004C-2.5
LT1034-2.5
LT580K
*LM385B-2.5
LM336B-2.5
*LM385-2.5
LM336-2.5
LT580M
LT1019C-2.5
LT1009-2.5
LT580L
LT1034-2.5
LT580K
*LT1004C-2.5
*LM385B-2.5
*LM385-2.5
LT580J
LM336B-2.5
LM336-2.5
4.5V Output
T.C.
ACCURACY
LT1019C-4.5
LT1019C-4.5
5.0V Output
T.C.
ACCURACY
LT1027A-5
LT1027B-5
LT1027C-5
LT1236A-5
LT1027D-5
LT1021B-5
LT1027E-5
LT1236B-5
LT1236C-5
REF-02E
LT1019-5
LT1029A
REF-02H
LT1021C-5
LT1021D-5
LT1029
REF-02C
REF-02D
LT1027A-5
LT1027B-5
LT1027C-5
LT1236A-5
LT1021C-5
LT1027D-5
LT1027E-5
LT1236B-5
LT1236C-5
REF-02E
LT1019-5
LT1021B-5
LT1021D-5
LT1029A
REF-02H
LT1029
REF-02C
REF-02D
6.9V to 6.95V Output
T.C.
ACCURACY
LTZ1000
LM399A
LM399
LM329A
LM329B
LM329C
LM329A
LTZ1000
LM329B
LM329C
LM329D
LM299A
7V Output
T.C.
ACCURACY
LT1021B-7
LT1021D-7
LT1034
LT1021B-7
LT1021D-7
LT1034
10V Output
T.C.
ACCURACY
LT1236A-10
LT1019A-10
LT1021C-10
LT1236B-10
LT1236C-10
LT1031C
REF-01E
LT581K
LT1019-10
LT1031D
LT581J
LT1021B-10
LT1021D-10
LT1031B
REF-01H
REF-01C
LT1236A-10
LT1019A-10
LT1021B-10
LT1236B-10
LT1236C-10
LT1031B-10
REF-01E
LT1031C
LT581K
LT1019-10
LT1021C-10
LT1021D-10
LT1031D
LT581J
REF-01C
*Micropower

Commercial 0°C to 70°C

VOLTAGE V_Z (V)	VOLTAGE TOLERANCE MAXIMUM T_A = 25°C	PART NUMBER	TEMPETATURE DRIFT, ppm/°C OR mV CHANGE	MIL/IND TEMP	OPERATING CURRENT RANGE (OR SUPPLY CURRENT)	PACKAGE TYPE	IMPORTANT FEATURES
1.235	±0.32%	LT1004-1.2	20ppm (typ)	M, I	10µA to 20mA	H, S, Z	Micropower
	±1%	LT1034B-1.2	20ppm (max)	M, I	20µA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±1%	LT1034-1.2	40ppm (max)	M, I	20µA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±2%	LM385-1.2	20ppm (typ)	M, I	15µA to 20mA	H, Z	Micropower
	±1%	LM385B-1.2	20ppm (typ)	M	15µA to 20mA	H, Z	Micropower
2.5	±0.8%	LT1004-2.5	20ppm (typ)	M, I	20µA to 20mA	H, S, Z	Micropower
	±0.2%	LT1009	6mV (max)	M, I	400µA to 10mA	H, Z	Precision
	±0.4%	LT1009S8	25ppm (max)	M, I	400µA to 20mA	S	Precision
	±0.05%	LT1019A-2.5	5ppm (max)	M	1.0mA	H, N	Precision Bandgap
	±0.2%	LT1019-2.5	20ppm (max)	M, I	1.2mA	H, N, S	Precision Bandgap
	±1%	LT1034B-2.5	20ppm (max)	M, I	20µA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±1%	LT1034-2.5	40ppm (max)	M, I	20µA to 20mA	H, S, Z	Low TC Micropower with 7V Aux Reference
	±4%	LM336-2.5	6mV (max)	M	400µA to 10mA	H, Z	General Purpose
	±2%	LM336B-2.5	6mV (max)	M	400µA to 10mA	H, Z	General Purpose
	±3%	LM385-2.5	20ppm (typ)	M, I	20µA to 20mA	H, Z	Micropower
	±1.5%	LM385B-2.5	20ppm (typ)	M	20µA to 20mA	H, Z	Micropower
	±3%	LT580J	85ppm (max)		1.5mA	H	3 Terminal Low Drift
	±1%	LT580K/K	40ppm (max)	M	1.5mA	H	3 Terminal Low Drift
	±0.4%	LT580L/U	25ppm (max)	M	1.5mA	H	3 Terminal Low Drift
	±0.4%	LT580M	10ppm (max)		1.5mA	H	3 Terminal Low Drift
4.5	±0.05%	LT1019A-4.5	5ppm (max)	M	1.2mA	H, N	Precision Bandgap
	±0.2%	LT1019-4.5	20ppm (max)	M, I	1.2mA	H, N, S	Precision Bandgap
5.0	±0.05%	LT1019A-5	5ppm (max)	M	1.2mA	H, N	Precision Bandgap
	±0.2%	LT1019-5	20ppm (max)	M, I	1.2mA	H, N, S	Precision Bandgap
	±1%	LT1021B-5	5ppm (max)	M, I	1.2mA	H, N	Very Low Drift
	±0.05%	LT1021C-5	20ppm (max)	M, I	1.2mA	H, N	Very Tight Initial Tolerance
	±1%	LT1021D-5	20ppm (max)	M, I	1.2mA	H, J, N, S	Low Cost, High Performance
	±0.02%	LT1027A	2ppm (max)		2mA	H	Precision, Enhanced Dynamics
	±0.05%	LT1027B	2ppm (max)		2mA	H, N	Precision, Enhanced Dynamics
	± 0.05%	LT1027C	3ppm (max)		2mA	H, N	Precision, Enhanced Dynamics
	± 0.05%	LT1027D	5ppm (max)		2mA	N, H, S	Precision, Enhanced Dynamics
	± 0.1%	LT1027E	7.5ppm (max)		2mA	N, H, S	Precision, Enhanced Dynamics
	±0.2%	LT1029A	20ppm (max)	M	700µA to 10mA	H, Z	Precision Bandgap
	±1%	LT1029	34ppm (max)	M	700µA to 10mA	H, Z	Precision Bandgap
	±0.05%	LT1236A-5	5ppm (max)	I	1.2mA	N, S	Tight Tolerance and Low TC Together
	±0.1%	LT1236B-5	10ppm (max)	I	1.2mA	N, S	Tight Tolerance and Low TC Together
	±0.1%	LT1236C-5	15ppm (max)	I	1.2mA	N, S	Tight Tolerance and Low TC Together
	±1%	REF02C	65ppm (max)		1.6mA	H, J, N	Precision Bandgap
	±2%	REF02D	250ppm (max)		2.0mA	H, J, N	Bandgap
	±0.3%	REF02E/A	8.5ppm (max)	M	1.4mA	H, J, N	Precision Bandgap
	±0.5%	REF02H	25ppm (max)		1.4mA	H, J, N	Precision Bandgap
6.9	±3%	LM329A	10ppm (max)	M	600µA to 15mA	H, Z	Low Drift
	±5%	LM329B	20ppm (max)	M	600µA to 15mA	H, Z	Low Drift
	±5%	LM329C	50ppm (max)	M	600µA to 15mA	H, Z	General Purpose
	±5%	LM329D	100ppm (max)		600µA to 15mA	H, Z	General Purpose
	±4%	LTZ1000	0.1ppm		4mA	H	Ultra Low Drift, 2ppm Long Term Stability*
6.95	±5%	LM399	2ppm (max)	M	500µA to 10mA	H	Ultra Low Drift
	±5%	LM399A	1ppm (max)	M	500µA to 10mA	H	Ultra Low Drift
7.0	±0.7%	LT1021B-7	5ppm (max)	M	1.0mA	H, N	Low Drift/Noise, Exc Stability
	±0.7%	LT1021D-7	20ppm (max)	M	1.0mA	H, N, S	Low Cost, High Performance
10.0	±0.05%	LT1019A-10	5ppm (max)	M	1.2mA	H, N	Precision Bandgap
	±0.2%	LT1019-10	20ppm (max)	M, I	1.2mA	H, N, S	Precision Bandgap
	±0.5%	LT1021B-10	5ppm (max)	M, I	1.7mA	H, N	Very Low Drift
	±0.05%	LT1021C-10	20ppm (max)	M, I	1.7mA	H, N	Very Tight Initial Tolerance
	±0.5%	LT1021D-10	20ppm (max)	M, I	1.7mA	H, N, S	Low Cost, High Performance
	±0.05%	LT1031B	5ppm (max)	M	1.7mA	H	Very Low Drift
	±0.1%	LT1031C	15ppm (max)	M	1.7mA	H	Very Tight Initial Tolerance
	±0.2%	LT1031D	25ppm (max)	M	1.7mA	H	Low Cost, High Performance
	±0.05%	LT1236A-10	5ppm (max)	I	1.2mA	N, S	Tight Tolerance and Low TC Together
	±0.1%	LT1236B-10	10ppm (max)	I	1.2mA	N, S	Tight Tolerance and Low TC Together
	±0.1%	LT1236C-10	15ppm (max)	I	1.2mA	N, S	Tight Tolerance and Low TC Together
	±0.3%	LT581J/S	30ppm (max)	M	1.0mA	H	3 Terminal Low Drift
	±0.1%	LT581K/T	15ppm (max)	M	1.0mA	H	3 Terminal Low Drift
	±0.05%	LT581L/U	5ppm (max)	M	1.0mA	H	3 Terminal Low Drift
	±1%	REF01C	65ppm (max)	M	1.6mA	H, J, N	Precision Bandgap
	±0.3%	REF01E/A	8.5ppm (max)	M	1.4mA	H, J, N	Precision Bandgap
	±0.5%	REF01H	25ppm (max)		1.4mA	H, J, N	Precision Bandgap

*LTZ1000 requires external control and biasing circuits.

FEATURES

- **Ultra-Low Drift: 5ppm/°C Max**
- **Trimmed to High Accuracy: 0.05% Max**
- **Industrial Temperature Range SO Package**
- Operates in Series or Shunt Mode
- Pin Compatible with AD586, AD587
- Output Sinks and Sources in Series Mode
- Very Low Noise < 1ppm $_{P-P}$ (0.1Hz to 10Hz)
- 100% Noise Tested
- > 100dB Ripple Rejection
- Minimum Input/Output Differential of 1V

APPLICATIONS

- A/D and D/A Converters
- Precision Regulators
- Precision Scales
- Inertial Navigation Systems
- Digital Voltmeters

DESCRIPTION

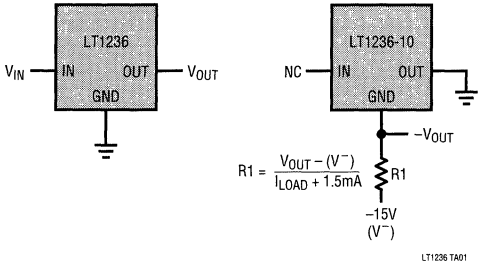
The LT®1236 is a precision reference that combines ultra-low drift and noise with excellent long-term stability and high output accuracy. The reference output will both source and sink up to 10mA and is almost totally immune to input voltage variations. Two voltages are available: 5V and 10V. The 10V version can be used as a shunt regulator (two-terminal zener) with the same precision characteristics as the three-terminal connection. Special care has been taken to minimize thermal regulation effects and temperature induced hysteresis.

The LT1236 combines both superior accuracy and temperature coefficient specifications without the use of high power, on-chip heaters. The LT1236 references are based on a buried zener diode structure which eliminates noise and stability problems with surface breakdown devices. Further, a subsurface zener exhibits better temperature drift and time stability than even the best band-gap references.

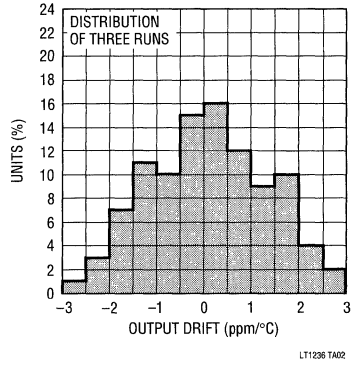
7

TYPICAL APPLICATION

Basic Positive and Negative Connections



Typical Distribution of Temperature Drift

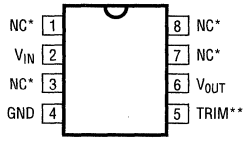


ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Input/Output Voltage Differential 35V
Output-to-Ground Voltage (Shunt Mode Current Limit)
  LT1236-5 ..... 10V
  LT1236-10 ..... 16V
Trim Pin-to-Ground Voltage
  Positive ..... Equal to V_{OUT}
  Negative ..... – 20V
Output Short-Circuit Duration
  V_{IN} = 35V ..... 10 sec
  $V_{IN} \leq$ 20V ..... Indefinite
Operating Temperature Range
  LT1236AC, BC, CC ..... 0°C to 70°C
  LT1236AI, BI, CI ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



N8 PACKAGE
8-LEAD PDIP

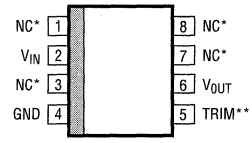
*CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS

**SEE APPLICATIONS INFORMATION SECTION

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LT1236ACN8-5
LT1236BCN8-5
LT1236CCN8-5
LT1236ACN8-10
LT1236BCN8-10
LT1236CCN8-10
LT1236AIN8-5
LT1236BIN8-5
LT1236CIN8-5
LT1236AIN8-10
LT1236BIN8-10
LT1236CIN8-10

TOP VIEW



S8 PACKAGE
8-LEAD PLASTIC SO

*CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS

**SEE APPLICATIONS INFORMATION SECTION

T_{JMAX} = 125°C, θ_{JA} = 190°C/W

ORDER PART NUMBER	
LT1236ACS8-5	LT1236AIS8-5
LT1236BCS8-5	LT1236BIS8-5
LT1236CCS8-5	LT1236CIS8-5
LT1236ACS8-10	LT1236AIS8-10
LT1236BCS8-10	LT1236BIS8-10
LT1236CCS8-10	LT1236CIS8-10

S8 PART MARKING	
236AC5	236AI5
236BC5	236BI5
236CC5	236CI5
236AC1	236AI1
236BC1	236BI1
236CC1	236CI1

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 10V, I_{OUT} = 0, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		LT1236-5 MIN	LT1236-5 TYP	LT1236-5 MAX	UNITS
Output Voltage (Note 1)	LT1236A-5		4.9975	5.000	5.0025	V
	LT1236B-5/LT1236C-5		4.9950	5.000	5.0050	V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \leq T_J \leq T_{MAX}$					
	LT1236A-5			2	5	ppm/°C
	LT1236B-5			5	10	ppm/°C
	LT1236C-5			10	15	ppm/°C
Line Regulation (Note 3)	7.2V ≤ V_{IN} ≤ 10V			4	12	ppm/V
		●			20	ppm/V
	10V ≤ V_{IN} ≤ 40V			2	6	ppm/V
		●			10	ppm/V
Load Regulation (Sourcing Current) (Note 3)	0 ≤ I_{OUT} ≤ 10mA			10	20	ppm/mA
		●			35	ppm/mA

ELECTRICAL CHARACTERISTICS V_{IN} = 10V, I_{OUT} = 0, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		LT1236-5 MIN	LT1236-5 TYP	LT1236-5 MAX	UNITS
Load Regulation (Sinking Current) (Note 3)	$0 \le I_{OUT} \le 10mA$	 ●		60	100 150	ppm/mA ppm/mA
Supply Current		 ●		0.8	1.2 1.5	mA mA
Output Voltage Noise (Note 5)	0.1Hz ≤ f ≤ 10Hz 10Hz ≤ f ≤ 1kHz			3.0 2.2	 3.5	μV_{P-P} μV_{RMS}
Long-Term Stability of Output Voltage (Note 6)	Δt = 1000Hrs Non-Cumulative			20		ppm
Temperature Hysteresis of Output (Note 7)	ΔT = ±25°C			10		ppm

V_{IN} = 15V, I_{OUT} = 0, T_A= 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		LT1236-10 MIN	LT1236-10 TYP	LT1236-10 MAX	UNITS
Output Voltage (Note 1)	LT1236A-10 LT1236B-10/LT1236C-10		9.995 9.990	10.000 10.000	10.005 10.010	V V
Output Voltage Temperature Coefficient (Note 2)	$T_{MIN} \le T_J \le T_{MAX}$ LT1236A-10 LT1236B-10 LT1236C-10			 2 5 10	 5 10 15	 ppm/°C ppm/°C ppm/°C
Line Regulation (Note 3)	$11.5V \le V_{IN} \le 14.5V$ $14.5V \le V_{IN} \le 40V$ 	 ● ●		1.0 0.5 	4 6 2 4	ppm/V ppm/V ppm/V ppm/V
Load Regulation (Sourcing Current) (Note 3)	$0 \le I_{OUT} \le 10mA$	 ●		12	25 40	ppm/mA ppm/mA
Load Regulation (Shunt Mode) (Notes 3, 4)	$1.7mA \le I_{SHUNT} \le 10mA$	 ●		50	100 150	ppm/mA ppm/mA
Series Mode Supply Current		 ●		1.2	1.7 2.0	mA mA
Shunt Mode Minimum Current	V_{IN} is Open	 ●		1.1	1.5 1.7	mA mA
Output Voltage Noise (Note 5)	0.1Hz ≤ f ≤ 10Hz 10Hz ≤ f ≤ 1kHz			6.0 3.5	 6	μV_{P-P} μV_{RMS}
Long-Term Stablility of Output Voltage (Note 6)	Δt = 1000Hrs Non-Cumulative			30		ppm
Temperature Hysteresis of Output (Note 7)	ΔT = ±25°C			5		ppm

The ● denotes specifications which apply over the specified temperature range.

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

Note 2: Temperature coefficient is measured by dividing the change in output voltage over the temperature range by the change in temperature. **Incremental slope is also measured at 25°C.**

Note 3: Line and load regulation are measured on a pulse basis. Output changes due to die temperature change must be taken into account separately.

Note 4: Shunt mode regulation is measured with the input open. With the input connected, shunt mode current can be reduced to 0mA. Load regulation will remain the same.

Note 5: RMS noise is measured with a 2-pole highpass filter at 10Hz and a 2-pole lowpass filter at 1kHz. The resulting output is full-wave rectified and then integrated for a fixed period, making the final reading an average as opposed to RMS. Correction factors are used to convert from average to RMS, and 0.88 is used to correct for the non-ideal bandbass of the filters.

Peak-to-peak noise is measured with a single highpass filter at 0.1Hz and a 2-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. Test time is 10 seconds.

Note 6: Long-term stability typically has a logarithmic characteristic and therefore, changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one third that of the first thousand hours, with a continuing trend toward reduced drift with time. Significant improvement in long-term drift can be

ELECTRICAL CHARACTERISTICS

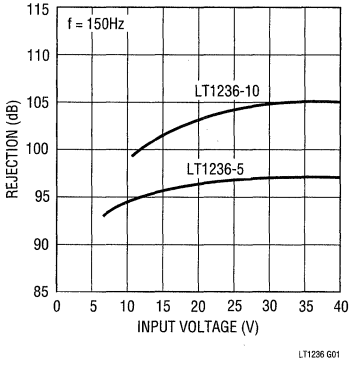
V_{IN} = 15V, I_{OUT} = 0, T_A = 25°C, unless otherwise noted.

realized by preconditioning the IC with a 100-200 hour, 125°C burn in. Long term stability will also be affected by differential stresses between the IC and the board material created during board assembly. Temperature cycling and baking of completed boards is often used to reduce these stresses in critical applications.

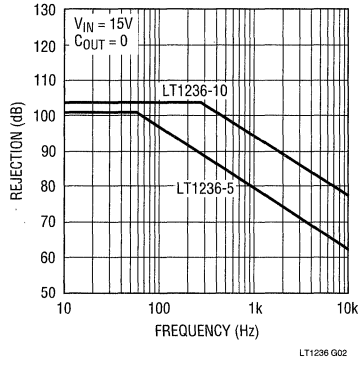
Note 7: Hysteresis in output voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to 50°C or 0°C before successive measurements. Hysteresis is roughly proportional to the square of temperature change. Hysteresis is not normally a problem for operational temperature excursions, but can be significant in critical narrow temperature range applications where the instrument might be stored at high or low temperatures.

TYPICAL PERFORMANCE CHARACTERISTICS

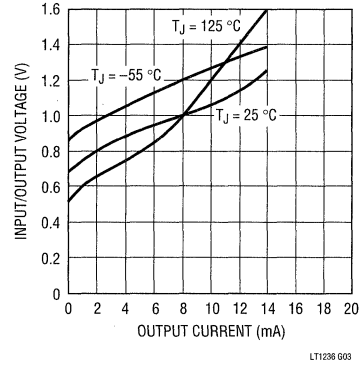
Ripple Rejection



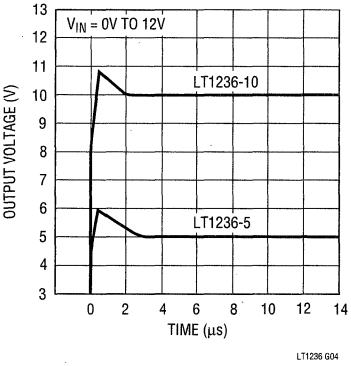
Ripple Rejection



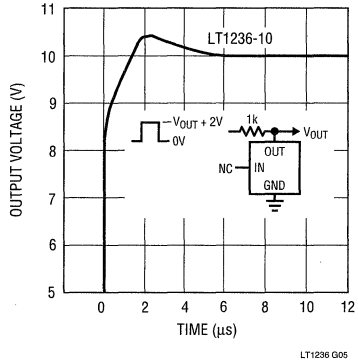
Minimum Input/Output Differential, LT1236-10



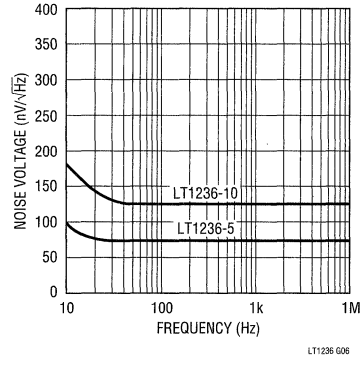
Start-Up (Series Mode)



Start-Up (Shunt Mode), LT1236-10

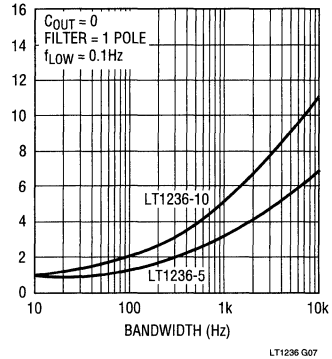


Output Voltage Noise Spectrum

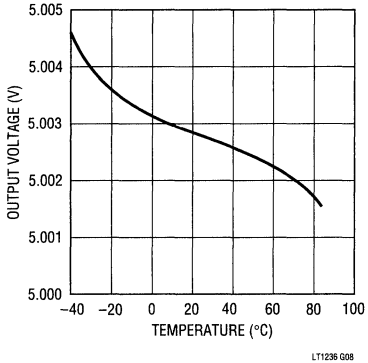


YPICAL PERFORMANCE CHARACTERISTICS

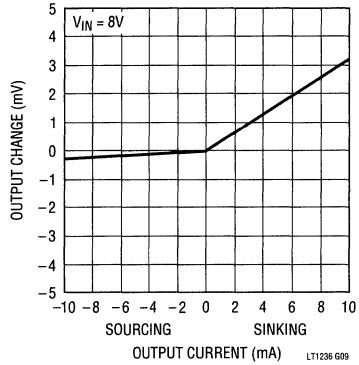
Output Voltage Noise



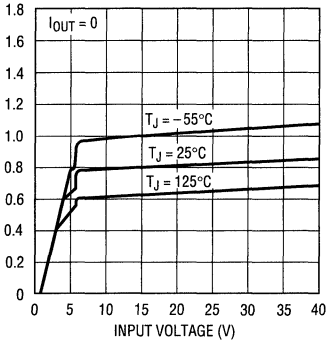
Output Voltage Temperature Drift LT1236-5



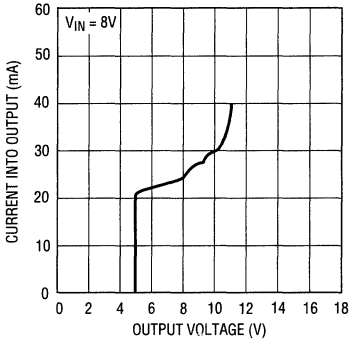
Load Regulation LT1236-5



Quiescent Current, LT1236-5



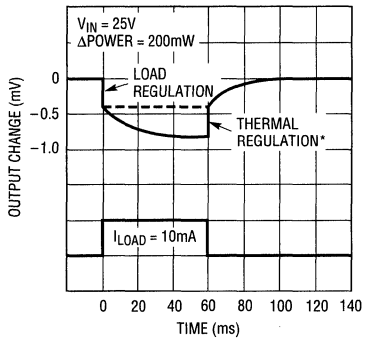
Sink Mode* Current Limit, LT1236-5



*NOTE THAT AN INPUT VOLTAGE IS REQUIRED FOR 5V UNITS.

LT1236 G11

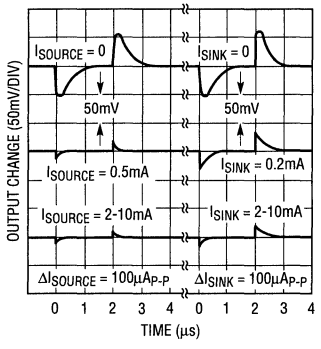
Thermal Regulation, LT1236-5



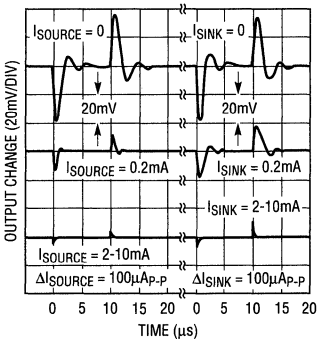
*INDEPENDENT OF TEMPERATURE COEFFICIENT

LT1236 G12

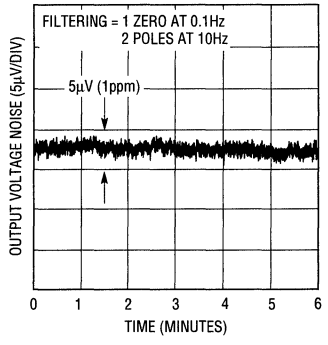
Load Transient Response, LT1236-5, C_{LOAD} = 0



Load Transient Response, LT1236-5, C_{LOAD} = 1000pF



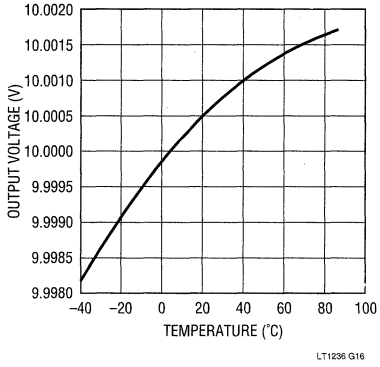
Output Noise 0.1Hz to 10Hz, LT1236-5



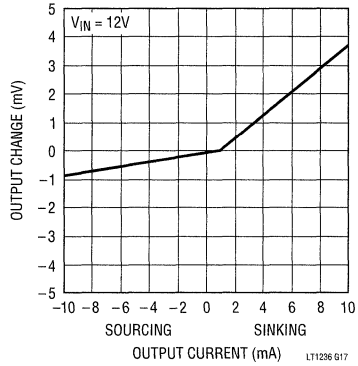
7

TYPICAL PERFORMANCE CHARACTERISTICS

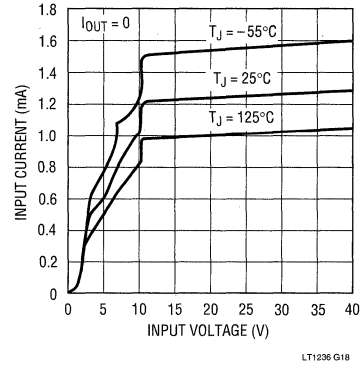
Output Voltage Temperature Drift, LT1236-10



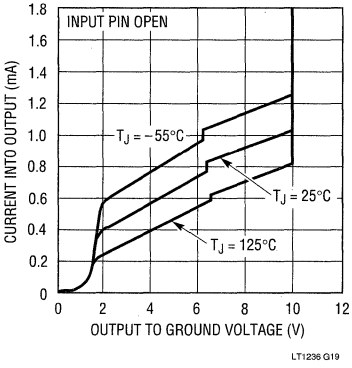
Load Regulation, LT1236-10



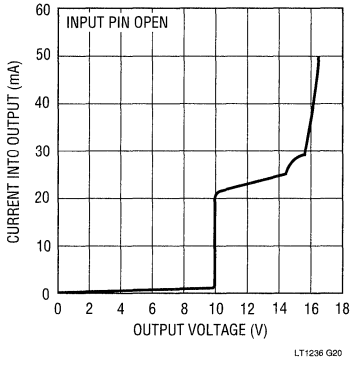
Input Supply Current, LT1236-10



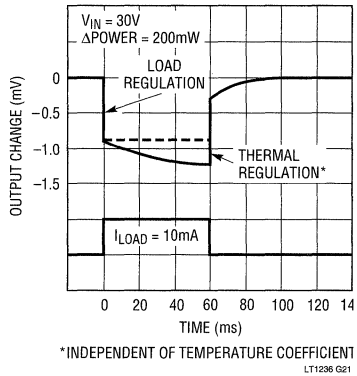
Shunt Characteristics, LT1236-10



Shunt Mode Current Limit, LT1236-10

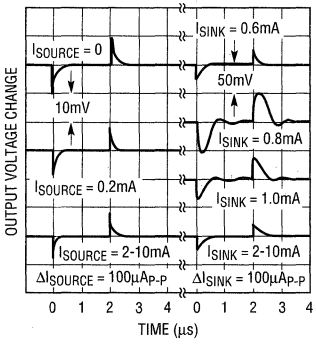


Thermal Regulation, LT1236-10



*INDEPENDENT OF TEMPERATURE COEFFICIENT

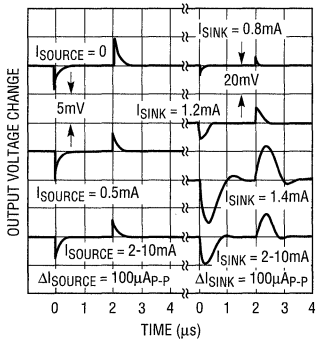
Load Transient Response, LT1236-10, C_{LOAD} = 0



NOTE VERTICAL SCALE CHANGE BETWEEN SOURCING AND SINKING

LT1236 G22

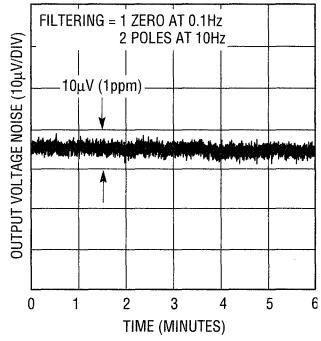
Load Transient Response, LT1236-10, C_{LOAD} = 1000pF



NOTE VERTICAL SCALE CHANGE BETWEEN SOURCING AND SINKING

LT1236 G23

Output Noise 0.1Hz to 10Hz, LT1236-10



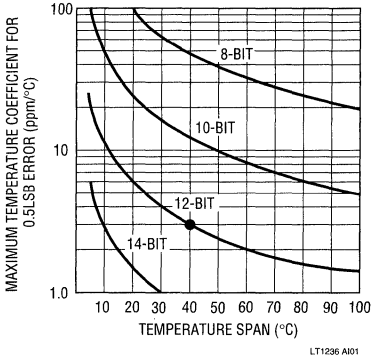
LT1236 G24

IPPLICATIONS INFORMATION

ffect of Reference Drift on System Accuracy

large portion of the temperature drift error budget in any systems is the system reference voltage. This graph dicates the maximum temperature coefficient allowable the reference is to contribute no more than 0.5LSB error the overall system performance. The example shown is 12-bit system designed to operate over a temperature nge from 25°C to 65°C. Assuming the system calibra-n is performed at 25°C, the temperature span is 40°C. can be seen from the graph that the temperature coeffi-ent of the reference must be no worse than 3ppm/°C if is to contribute less than 0.5LBS error. For this reason, e LT1236 family has been optimized for low drift.

Maximum Allowable Reference Drift



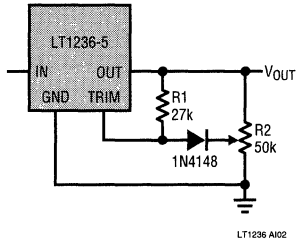
imming Output Voltage

e LT1236-10 has a trim pin for adjusting output voltage. e impedance of the trim pin is about 12kΩ with a minal open circuit voltage of 5V. It is designed to be iven from a source impedance of 3kΩ or less to mini-ize changes in the LT1236 TC with output trimming. tenuation between the trim pin and the output is 70:1. is allows ±70mV trim range when the trim pin is tied to e wiper of a potentiometer connected between the tput and ground. A 10kΩ potentiometer is recom-ended, preferably a 20 turn cermet type with stable aracteristics over time and temperature.

e LT1236-10 "A" version is pre-trimmed to ±5mV and erefore can utilize a restricted trim range. A 75k resistor in series with a 20kΩ potentiometer will give ±10mV trim range. Effect on the output TC will be only 1ppm/°C for the ±5mV trim needed to set the "A" device to 10.000V.

LT1236-5

The LT1236-5 does have an output voltage trim pin, but the TC of the nominal 4V open circuit voltage at pin 5 is about –1.7mV/°C. For the voltage trimming not to affect reference output TC, the external trim voltage must track the voltage on the trim pin. Input impedance of the trim pin is about 100kΩ and attenuation to the output is 13:1. The technique shown below is suggested for trimming the output of the LT1236-5 while maintaining minimum shift in output temperature coefficient. The R1/R2 ratio is chosen to minimize interaction of trimming and TC shifts, so the exact values shown should be used.



Capacitive Loading and Transient Response

The LT1236 is stable with all capacitive loads, but for optimum settling with load transients, output capacitance should be under 1000pF. The output stage of the reference is class AB with a fairly low idling current. This makes transient response worse-case at light load currents. Because of internal current drain on the output, actual worst-case occurs at I_{LOAD} = 0 on LT1236-5 and I_{LOAD} = 1.4mA (sinking) on LT1236-10. Significantly better load transient response is obtained by moving slightly away from these points. See Load Transient Response curves for details. In general, best transient response is obtained when the output is sourcing current. In critical applications, a 10µF solid tantalum capacitor with several ohms in series provides optimum output bypass.

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APPLICATIONS INFORMATION

Kelvin Connections

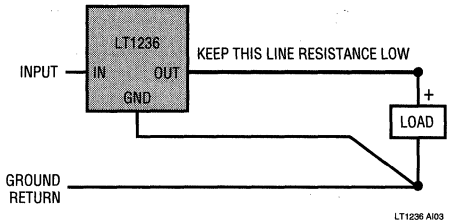
Although the LT1236 does not have true force/sense capability at its outputs, significant improvements in ground loop and line loss problems can be achieved with proper hook-up. In series mode operation, the ground pin of the LT1236 carries only ≈ 1mA and can be used as a sense line, greatly reducing ground loop and loss problems on the low side of the reference. The high side supplies load current so line resistance must be kept low. Twelve feet of #22 gauge hook-up wire or 1 foot of 0.025 inch printed circuit trace will create 2mV loss at 10mA output current. This is equivalent to 1LSB in a 10V, 12-bit system.

The following circuits show proper hook-up to minimize errors due to ground loops and line losses. Losses in the output lead can be greatly reduced by adding a PNP boost transistor if load currents are 5mA or higher. R2 can be added to further reduce current in the output sense lead.

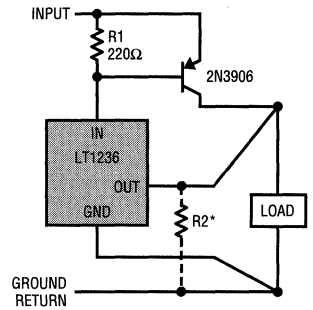
Effects of Air Movement on Low Frequency Noise

The LT1236 has very low noise because of the buried zener used in its design. In the 0.1Hz to 10Hz band, peak-to-peak noise is about 0.5ppm of the DC output. To achieve this low noise, however, care must be taken to shield the reference from ambient air turbulence. Air movement can create noise because of thermoelectric differences between IC package leads and printed circuit board materials and/or sockets. Power dissipation in the reference, even though it rarely exceeds 20mW, is enough to cause small temperature gradients in the package leads. Variations ir thermal resistance, caused by uneven air flow, create differential lead temperatures, thereby causing thermoelectric voltage noise at the output of the reference.

Standard Series Mode



Series Mode with Boost Transistor

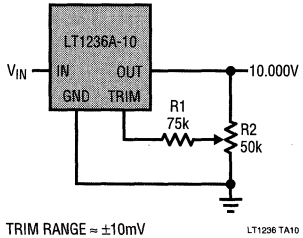


*OPTIONAL—REDUCES CURRENT IN OUTPUT SENSE LEAD: R2 = 2.4k (LT1236-5), 5.6k (LT1236-10)

LT1236 AI04

TYPICAL APPLICATIONS

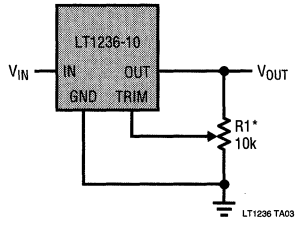
Restricted Trim Range for Improved Resolution, 10V, "A" Version Only



TRIM RANGE ≈ ±10mV

LT1236 TA10

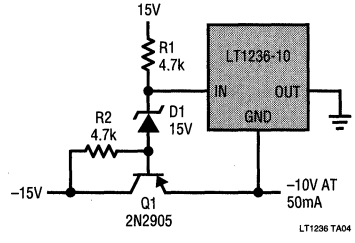
LT1236-10 Full Trim Range (±0.7%)



LT1236 TA03

*CAN BE RAISED TO 20k FOR LESS CRITICAL APPLICATIONS

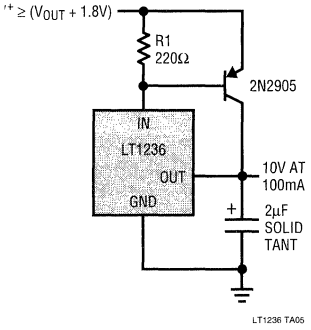
Negative Series Reference



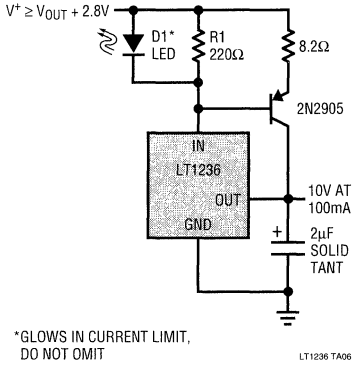
LT1236 TA04

TYPICAL APPLICATIONS

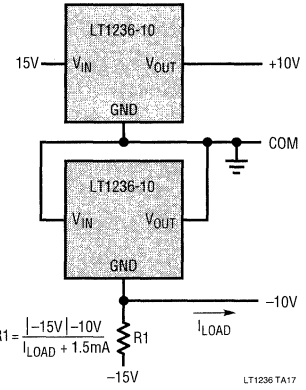
Boosted Output Current with No Current Limit



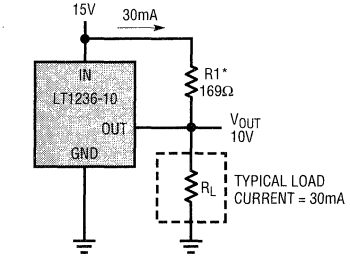
Boosted Output Current with Current Limit



±10V Output Reference



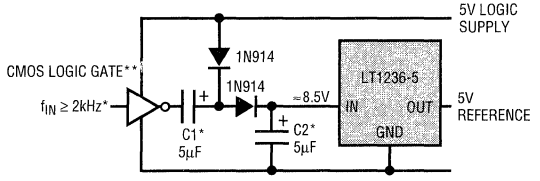
Handling Higher Load Currents



*SELECT R1 TO DELIVER TYPICAL LOAD CURRENT. LT1236 WILL THEN SOURCE OR SINK AS NECESSARY TO MAINTAIN PROPER OUTPUT. DO NOT REMOVE LOAD AS OUTPUT WILL BE DRIVEN UNREGULATED HIGH. LINE REGULATION IS DEGRADED IN THIS APPLICATION

LT1236 TA07

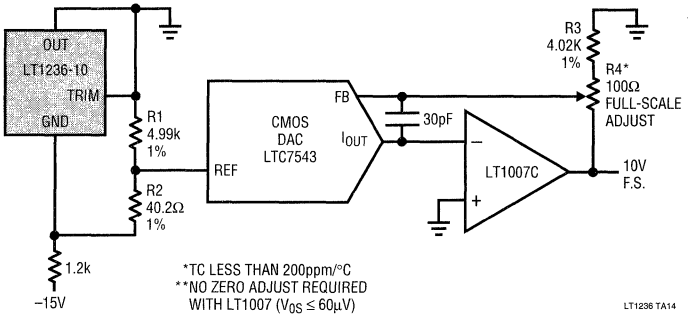
Operating 5V Reference from 5V Supply



*FOR HIGHER FREQUENCIES C1 AND C2 MAY BE DECREASED
**PARALLEL GATES FOR HIGHER REFERENCE CURRENT LOADING

LT1236 TA15

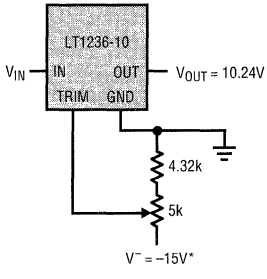
CMOS DAC with Low Drift Full-Scale Trimming**



*TC LESS THAN 200ppm/°C
**NO ZERO ADJUST REQUIRED WITH LT1007 ($V_{OS} \leq 60\mu V$)

LT1236 TA14

Trimming 10V Units to 10.24V



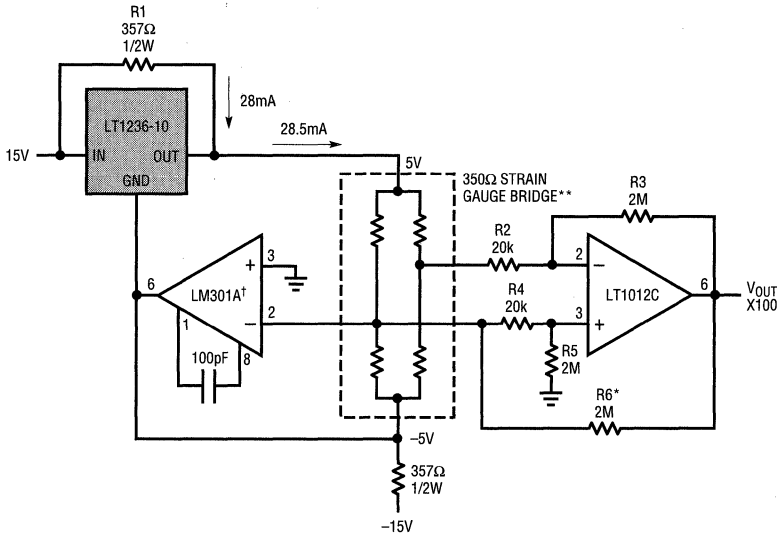
*MUST BE WELL REGULATED

$\frac{dV_{OUT}}{dV^-} = \frac{15mV}{V}$

LT1236 TA11

TYPICAL APPLICATIONS

Strain Gauge Conditioner for 350Ω Bridge



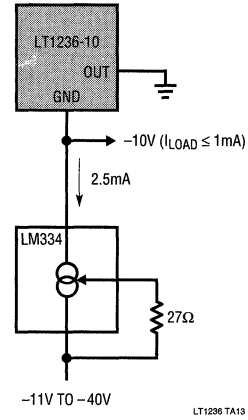
*THIS RESISTOR PROVIDES POSITIVE FEEDBACK TO THE BRIDGE TO ELIMINATE LOADING EFFECT OF THE AMPLIFIER. EFFECTIVE Z_{IN} OF AMPLIFIER STAGE IS ≥ 1MΩ. IF R2 TO R5 ARE CHANGED, SET R6 = R3

**BRIDGE IS ULTRA-LINEAR WHEN ALL LEGS ARE ACTIVE, TWO IN COMPRESSION AND TWO IN TENSION, OR WHEN ONE SIDE IS ACTIVE WITH ONE COMPRESSED AND ONE TENSIONED LEG

†OFFSET AND DRIFT OF LM301A ARE VIRTUALLY ELIMINATED BY DIFFERENTIAL CONNECTION OF LT1012C

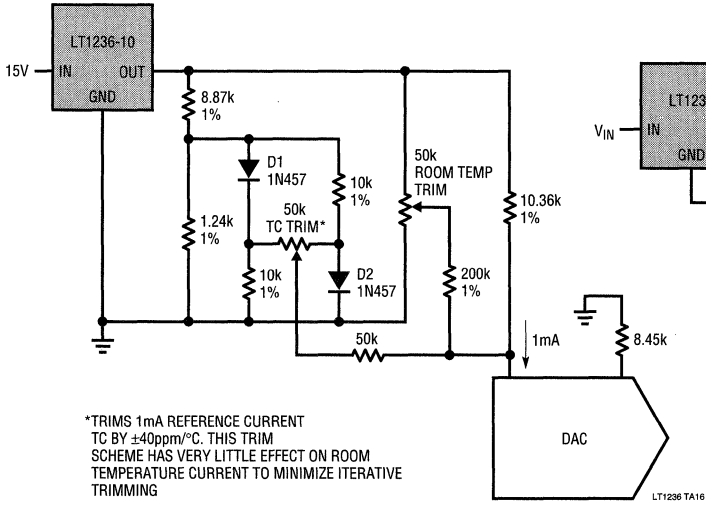
LT1236 TA08

Negative Shunt Reference Driven by Current Source



LT1236 TA13

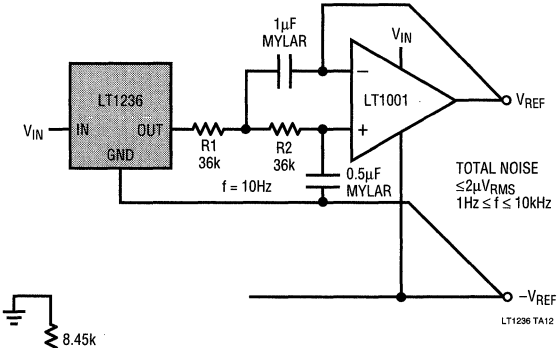
Precision DAC Reference with System TC Trim



*TRIMS 1mA REFERENCE CURRENT TC BY ±40ppm/°C. THIS TRIM SCHEME HAS VERY LITTLE EFFECT ON ROOM TEMPERATURE CURRENT TO MINIMIZE ITERATIVE TRIMMING

LT1236 TA16

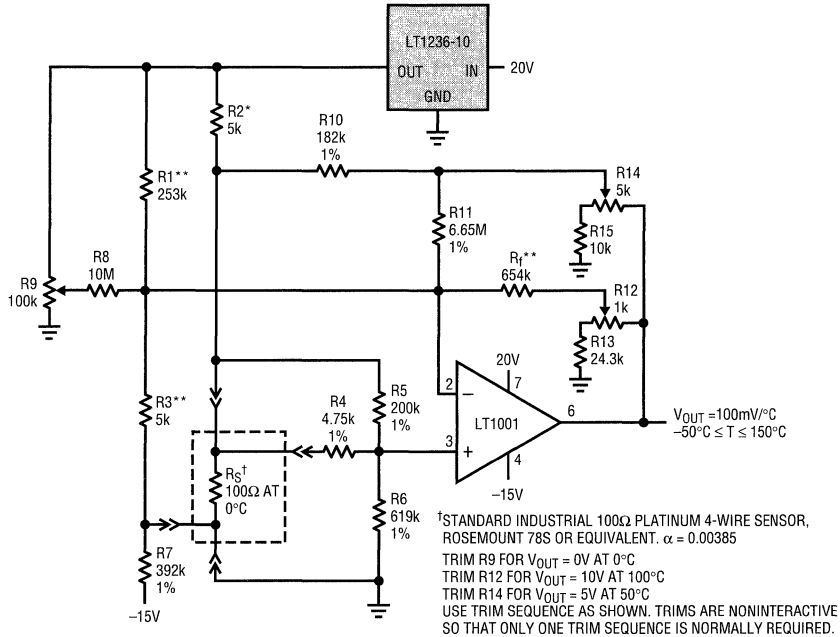
2-Pole Lowpass Filtered Reference



LT1236 TA12

TYPICAL APPLICATIONS

Ultra-Linear Platinum Temperature Sensor*



†STANDARD INDUSTRIAL 100Ω PLATINUM 4-WIRE SENSOR, ROSEMOUNT 78S OR EQUIVALENT. $\alpha = 0.00385$

TRIM R9 FOR V_{OUT} = 0V AT 0°C
TRIM R12 FOR V_{OUT} = 10V AT 100°C
TRIM R14 FOR V_{OUT} = 5V AT 50°C
USE TRIM SEQUENCE AS SHOWN. TRIMS ARE NONINTERACTIVE SO THAT ONLY ONE TRIM SEQUENCE IS NORMALLY REQUIRED.

*FEEDBACK LINEARIZES OUTPUT TO ± 0.005°C FROM –50°C TO 150°C

**WIREWOUND RESISTORS WITH LOW TC

LT1236 TA09

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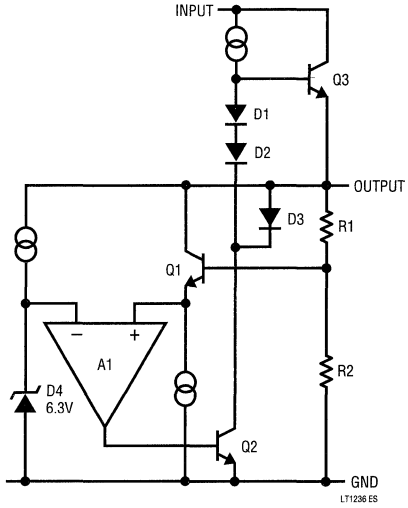
EQUIVALENT SCHEMATIC



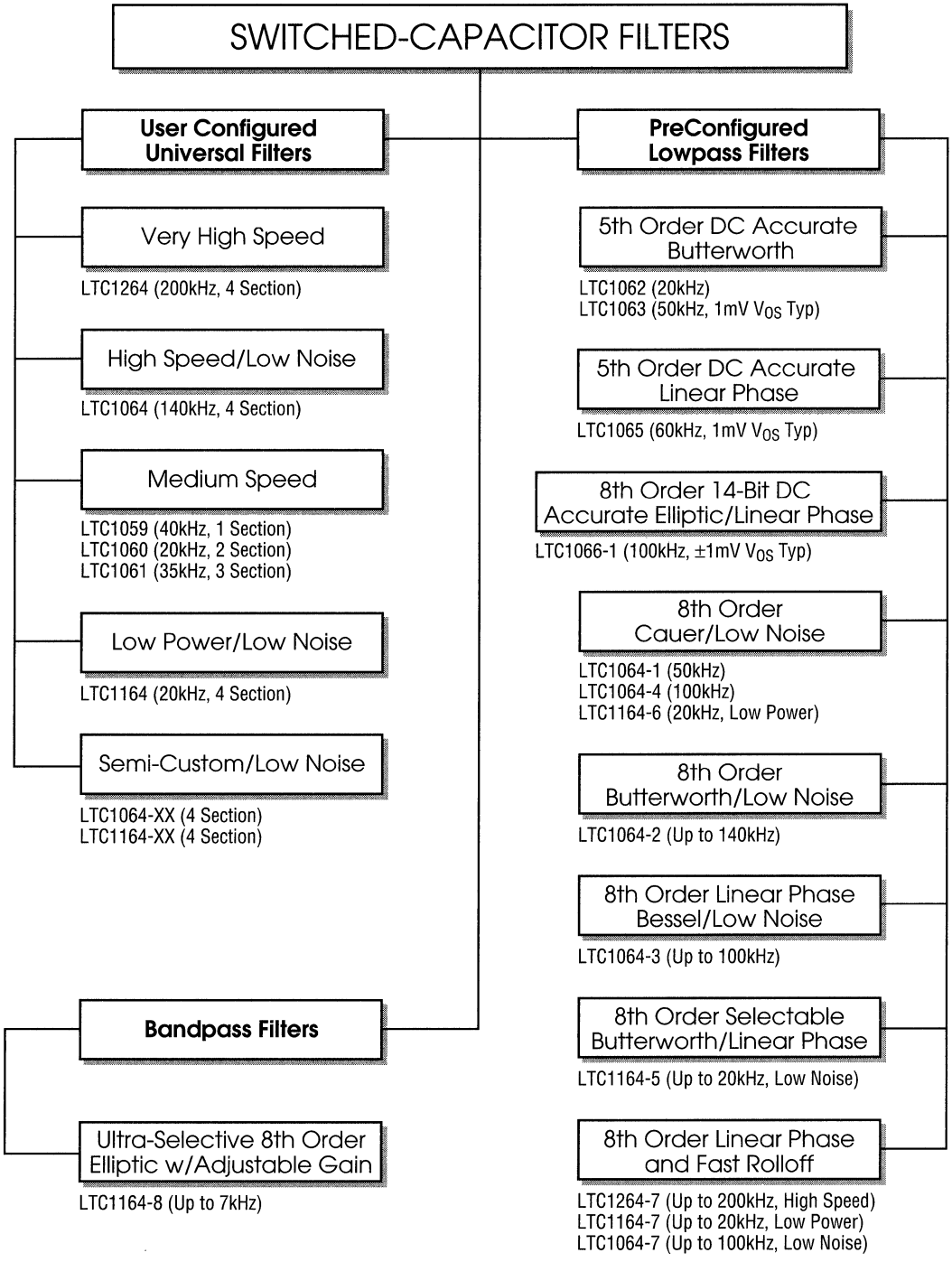
LT1236 ES

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1019	Precision Bandgap Reference	0.05%, 5ppm/°C
LT1027	Precision 5V Reference	0.02%, 2ppm/°C

SECTION 8—MONOLITHIC FILTERS

SECTION 8—MONOLITHIC FILTERS


SWITCHED-CAPACITOR FILTERS
User Configured Universal Filters
Very High Speed
LTC1264 (200kHz, 4 Section)
High Speed/Low Noise
LTC1064 (140kHz, 4 Section)
Medium Speed
LTC1059 (40kHz, 1 Section)
LTC1060 (20kHz, 2 Section)
LTC1061 (35kHz, 3 Section)
Low Power/Low Noise
LTC1164 (20kHz, 4 Section)
Semi-Custom/Low Noise
LTC1064-XX (4 Section)
LTC1164-XX (4 Section)
Bandpass Filters
Ultra-Selective 8th Order Elliptic w/Adjustable Gain
LTC1164-8 (Up to 7kHz)
PreConfigured Lowpass Filters
5th Order DC Accurate Butterworth
LTC1062 (20kHz)
LTC1063 (50kHz, 1mV V_{OS} Typ)
5th Order DC Accurate Linear Phase
LTC1065 (60kHz, 1mV V_{OS} Typ)
8th Order 14-Bit DC Accurate Elliptic/Linear Phase
LTC1066-1 (100kHz, ±1mV V_{OS} Typ)
8th Order Cauer/Low Noise
LTC1064-1 (50kHz)
LTC1064-4 (100kHz)
LTC1164-6 (20kHz, Low Power)
8th Order Butterworth/Low Noise
LTC1064-2 (Up to 140kHz)
8th Order Linear Phase Bessel/Low Noise
LTC1064-3 (Up to 100kHz)
8th Order Selectable Butterworth/Linear Phase
LTC1164-5 (Up to 20kHz, Low Noise)
8th Order Linear Phase and Fast Rolloff
LTC1264-7 (Up to 200kHz, High Speed)
LTC1164-7 (Up to 20kHz, Low Power)
LTC1064-7 (Up to 100kHz, Low Noise)

ANALOG FILTER SELECTION GUIDE

Introduction

The LTC family of switched-capacitor filters offers the system designer cost effective and space saving alternatives to filter designs implemented with op amps. A single IC filter can be used to replace multiple amplifiers and external capacitors.

Since their center frequencies are set by a stable external clock, switched-capacitor filters virtually eliminate the temperature drift problems associated with active RC filter designs. This clock tuning also allows the adjustment of corner frequency over a wide range (greater than 10^6:1 for the LTC1064 family), permitting one filter to do the job of multiple active RC filters.

LTC's filter offerings include single, dual, triple, and quad block products and range in performance from improved replacements for the industry standard MF5 and MF10, to state-of-the-art products such as the LTC1064/1164/1264 families. The LTC1064/1164/1264 "Dash Series" products are one chip solutions requiring no external components. Our semi-custom programs offer an ASIC solution to high performance or higher volume system needs.

Features

- Clock-Tunable Center Frequencies
- Stable, Selectable Clock-to-Center Frequency Ratios
- Center Frequencies to 200kHz
- Noise Performance As Low As 80μV_{RMS}
- Available with Zero DC Offset
- Filter CAD Program Available for Low-Effort Design
- Available as Universal Filter Blocks, Dedicated Filters, or Semi-Custom Fixed Filters
- Improved Replacements for Industry Standard MF5 and MF10
- Available in Surface Mount Packages

Applications

- Anti-Aliasing Filters
- Smoothing Filters
- Telecom Filters
- Spectral Analysis
- Loop Filters
- Audio

PART NUMBER	FILTER ORDER	f_0 MAX	fO/fCLK	TCf_0	SO PKG	MIL TEMP AVAIL	PIN COUNT	FEATURES
LTC1059	2	40kHz	100, 50:1	5ppm/°C	Y	Y	14	Low Noise, Low Crosstalk, Universal Filter Block
LTC1060	4	20kHz	100, 50:1	10ppm/°C	Y	Y	20	Improved MF5 Replacement
LTC1061	6	35kHz	100, 50:1	1ppm/°C	Y	Y	20	Improved MF10 Replacement
LTC1062	5	20kHz	100:1	10ppm/°C	Y	Y	8	Fifth Order Low Pass Filter, No DC Offset
LTC1063	5	50kHz	100:1	1ppm/°C	Y	N	8	Clock-Tunable DC Accurate Butterworth
LTC1064	8	140kHz	100, 50:1	1ppm/°C	Y	Y	24	Universal, Low Noise, Fast Quad Filter
LTC1064-1	8	50kHz	100:1	1ppm/°C	Y	Y	14	Low Noise, Cauer Lowpass Filter
LTC1064-2	8	140kHz	100, 50:1	1ppm/°C	Y	Y	14	Low Noise, High Frequency Butterworth Lowpass FIlter
LTC1064-3	8	100kHz	150, 75:1	1ppm/°C	Y	Y	14	Low Noise, Linear Phase Bessel Lowpass Filter
LTC1064-4	8	100kHz	100, 50:1	1ppm/°C	Y	Y	14	Low Noise, High Speed Cauer Lowpass Filter
LTC1064-7	8	100kHz	100, 50:1	1ppm/°C	Y	Y	14	Constant Group Delay, Lowpass Filter
LTC1064-XX	8	to 140kHz	100, 50:1	1ppm/°C	Y	Y	14	Semi-Custom Low Noise, High Speed Filter
LTC1065	5	60kHz	100:1	1ppm/°C	Y	N	8	Clock-Tunable DC Accurate Bessel
LTC1066-1	8	100kHz	100, 50:1	1ppm/°C	Y	N	18	14-Bit DC Accurate, Pin Selectable Cauer/Bessel
LTC1164	8	20kHz	100, 50:1	1ppm/°C	Y	Y	24	Universal, Low Noise, Low Power, Wide Dynamic Range Filter
LTC1164-5	8	20kHz	100, 50:1	1ppm/°C	Y	Y	14	Low Power, Butterworth/Bessel Lowpass Filter
LTC1164-6	8	20kHz	100, 50:1	1ppm/°C	Y	Y	14	Low Power, Elliptic Lowpass Filter
LTC1164-7	8	20kHz	100, 50:1	1ppm/°C	Y	Y	14	Constant Group Delay, Low Power, Lowpass Filter
LTC1164-8	8	7kHz	100:1	1ppm/°C	Y	N	14	Ultra-Selective Elliptic Bandpass Filter w/Adjustable Gain
LTC1164-XX	8	to 20kHz	100, 50:1	1ppm/°C	Y	Y	14	Semi-Custom Low Noise, Low Power Filter
LTC1264	8	200kHz	20:1	1ppm/°C	Y	Y	24	Very High Speed Universal Quad Filter
LTC1264-7	8	200kHz	50, 25:1	1ppm/°C	Y	Y	14	Constant Group Delay, High Speed, Lowpass Filter
LTC1264-XX	8	to 200kHz	50, 25:1	1ppm/°C	Y	Y	14	Semi-Custom Very High Speed Filter

Ultra-Selective, Low Power 8th Order Elliptic Bandpass Filter with Adjustable Gain

FEATURES

- **Ultra-Selectivity (50dB Attenuation at ±4% of Center Frequency)**
- **Adjustable Passband Gain**
- **Noise Independent of Gain**
- Filter Noise: 270μV_{RMS}, V_S = Single 5V Supply
- Clock-Tunable (Center Frequency = $f_{CLK}/100$)
- Center Frequencies up to 5kHz, V_S = ±5V (Typical I_{SUPPLY} = 3.2mA)
- Center Frequencies up to 4kHz, V_S = Single 5V Supply (Typical I_{SUPPLY} = 2.3mA)

APPLICATIONS

- Asynchronous Narrowband Signal Detectors
- Low Frequency Asynchronous Demodulators
- Handheld Spectrum Analyzers
- In-Band Tone Signaling Detectors

DESCRIPTION

The LTC®1164-8 is a monolithic ultra-selective, 8th order, elliptic bandpass filter. The passband of the LTC1164-8 is tuned with an external clock and the clock-to-center frequency ratio is 100:1. The –3dB pass bandwidth is typically 1% of the filter center frequency. The stopband attenuation of the LTC1164-8 is greater than 50dB. The lower and upper stopband frequencies are less than 0.96 × center frequency and greater than 1.04 × center frequency, respectively.

The LTC1164-8 requires an external op amp and two external resistors (see the circuit below). The filter's gain at center frequency is set by the ratio R_{IN}/R_F. For a gain equal to one and an optimum dynamic range, R_F should be set to 61.9k and R_{IN} should be 340k. For gains other than one, R_{IN} = 340k/Gain. Gains up to 1000 are obtainable. Setting the filter's gain with input resistor R_{IN} does not increase the filter's wideband noise. The 270μV_{RMS} wideband noise of the LTC1164-8 is independent of the filter's center frequency.

The LTC1164-8 is available in a 14-pin PDIP or a 16-pin surface mount SO Wide package.

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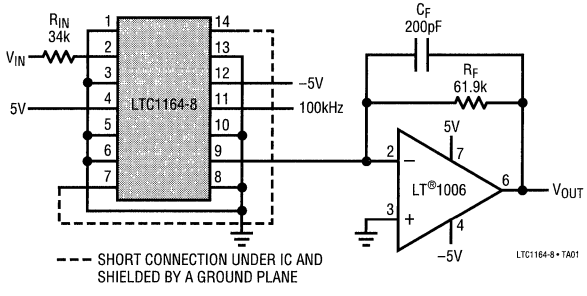
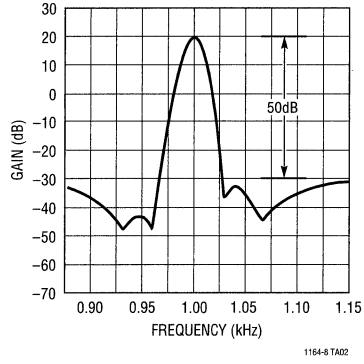
TYPICAL APPLICATION

Ultra-Narrow 1kHz Bandpass Filter with Gain = 10
Gain = 340k/R_{IN}, $1/(2\pi \times R_F \times C_F) \geq 10 \times$ Center Frequency



Frequency Response



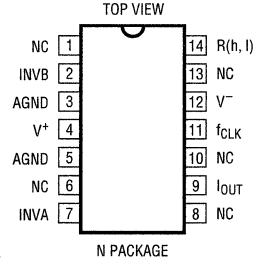
ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 16.5V
Power Dissipation 700mW
Burn-In Voltage 16.5V
Voltage at Any Input .... $(V^- - 0.3V) \leq V_{IN} \leq (V^+ + 0.3V)$
Operating Temperature Range* ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Maximum Clock Frequency
$V_S = \pm 7.5V$ 720kHz
$V_S = \pm 5V$ 540kHz
V_S = Single 5V 430kHz

*For an extended operating temperature range contact LTC Marketing for details.

PACKAGE/ORDER INFORMATION

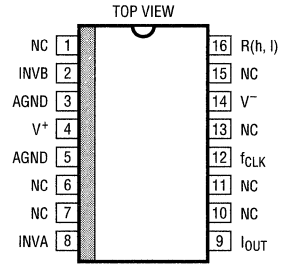


N PACKAGE
14-LEAD PDIP

T_{JMAX} = 110°C, θ_{JA} = 65°C/W

ORDER PART NUMBER

LTC1164-8CN



SW PACKAGE
16-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 85°C/W

ORDER PART NUMBER

LTC1164-8CSW

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS (See Test Circuit)

T_A = 25°C, Center Frequency = $f_{CLK}/100$, f_{CLK} = 100kHz (the clock signal is a TTL or CMOS square wave, clock rise or fall time ≤ 1µs), the AC test signal level is $1V_{RMS}$ for $V_S = \pm 5V$ or $0.5V_{RMS}$ for $V_S = \pm 2.375V$, unless otherwise specified.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Gain at Center Frequency	$V_S = \pm 2.375V$	f_{IN} = 1000Hz		–3	0±1.5	3	dB
			●	–4	0±2.0	4	dB
	$V_S = \pm 5V$	f_{IN} = 1000Hz		–3	0±1.5	3	dB
			●	–4	0±2.0	4	dB
Gain at 0.995 × Center Frequency and 1.005 × Center Frequency (Referenced to Gain at Center Frequency)	$V_S = \pm 2.375V$	f_{IN} = 995Hz		–8	–3±2	–1	dB
			●	–9		0	dB
		f_{IN} = 1005Hz		–8	–3±2	–1	dB
			●	–9		0	dB
	$V_S = \pm 5V$	f_{IN} = 995Hz			–3±2		dB
		f_{IN} = 1005Hz			–3±2		dB
Lower Stopband Attenuation (Referenced to Gain at Center Frequency)	$V_S = \pm 2.375V$	f_{IN} = 960Hz (Note 1)		–48	–52		dB
		f_{IN} = 800Hz		–50	–52	–58	dB
			●	–48		–60	dB
	$V_S = \pm 5V$	f_{IN} = 960Hz (Note 1)		–48	–52		dB
		f_{IN} = 800Hz			–52		dB

ELECTRICAL CHARACTERISTICS (See Test Circuit)

T_A = 25°C, Center Frequency = f_{CLK}/100, f_{CLK} = 100kHz (the clock signal is a TTL or CMOS square wave, clock rise or fall time ≤ 1μs), he AC test signal level is 1V_{RMS} for V_S = ±5V or 0.5V_{RMS} for V_S = ±2.375V, unless otherwise specified.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Upper Stopband Attenuation (Referenced to Gain at Center Frequency)	V_S = ±2.375V	f_{IN} = 1040Hz (Note 1)		−48	−52		dB
		f_{IN} = 1200Hz		−50	−52	−58	dB
			●	−48		−60	dB
	V_S = ±5V	f_{IN} = 1040Hz (Note 1)		−48	−52		dB
		f_{IN} = 1200Hz			−52		dB
Maximum Output for < 0.25% Total Harmonic Distortion	V_S = ±2.5V	f_{IN} = 1000Hz			1.0		V_{RMS}
	V_S = ±5V	f_{IN} = 1000Hz			2.5		V_{RMS}
Output DC Offset	V_S = ±2.5V (At the Output of External Op Amp)				−40±50		mV
	V_S = ±5V				−50±60		mV
Power Supply Current (Note 2)	V_S = ±2.375V				2.3	4.0	mA
			●			4.5	mA
	V_S = ±5V				3.2	7.0	mA
			●			8.0	mA
	V_S = ±7.5V				4.5	11.0	mA
			●			12.5	mA
Power Supply Range				±2.375		±8	V

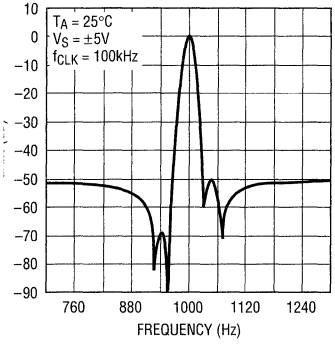
The ● denotes specifications which apply over the full operating temperature range.

Note 1: The minimum stopband attenuation at 960Hz and 1040Hz is guaranteed by design and test correlation.

Note 2: The maximum current over temperature is at 0°C. At 70°C the maximum current is less than its maximum value at 25°C.

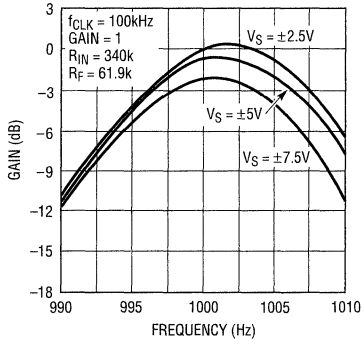
TYPICAL PERFORMANCE CHARACTERISTICS

Gain vs Frequency



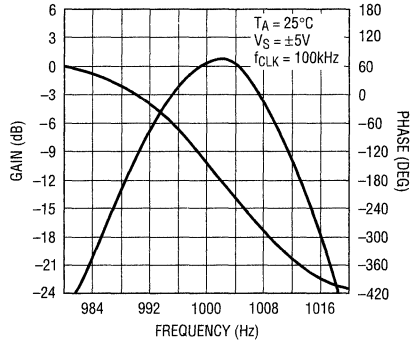
LTC1164-8 • TPC01

Passband Variations vs Power Supply



LTC1164-8 • TPC02

Passband Gain and Phase vs Frequency



LTC1164-8 • TPC03

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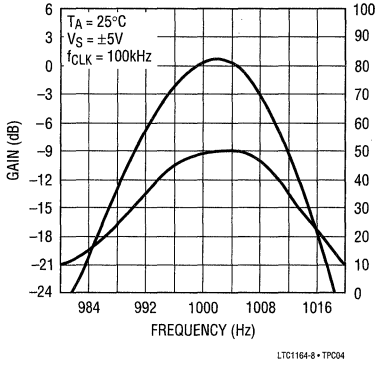
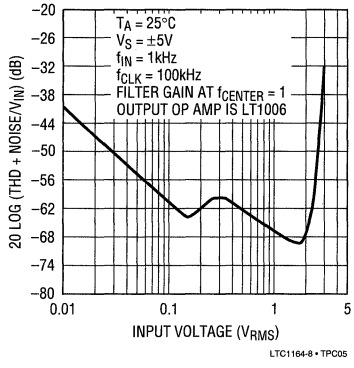
TYPICAL PERFORMANCE CHARACTERISTICS

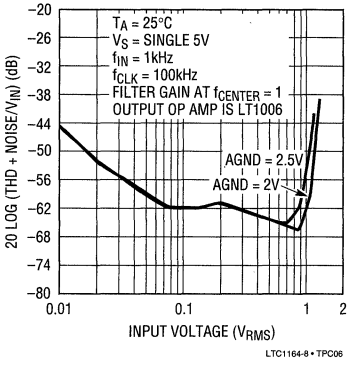
Passband Gain and Delay vs Frequency



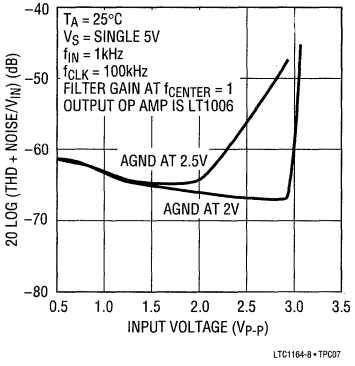
THD + Noise vs Input Voltage



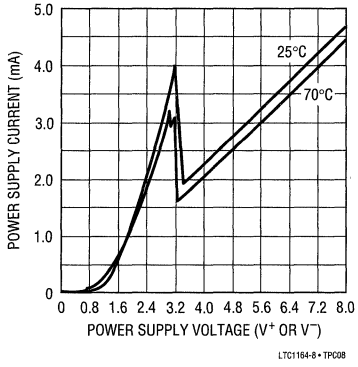
THD + Noise vs Input Voltage



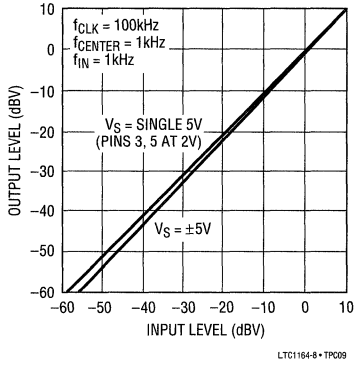
THD + Noise vs Input Voltage



Power Supply Current vs Power Supply Voltage



Output vs Input



PIN FUNCTIONS (14-Lead PDIP)

V^+, V^- (Pins 4, 12): Power Supply Pins. The V^+ (pin 4) and the V^- (pin 12) should be bypassed with a 0.1µF capacitor to a reliable ground plane. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The power supply during power-up should have a slew rate of less than 1V/µs.

For dual supply operation if the V^+ supply is applied before the V^- supply or the V^- supply is applied before the V^+ supply, a signal diode on each supply pin to ground will prevent latch-up. Figures 1 and 2 show typical connections for dual and single supply operation.

f_{CLK} (Pin 11): Clock Input Pin. Any TTL or CMOS clock source with a square wave output and 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to the clock's ground at a single point only. Table 1 shows the clock's low and high level threshold values for dual or single supply operation. A pulse generator can be used as a clock source provided the high level on-time is at least 1µs. Sine waves are not recommended for clock input frequencies less than 100kHz. The clock's rise or fall time should be equal to or less than 1µs.

Table 1. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
Single Supply = 5V	>1.45V	<0.5V
Single Supply = 12V	>7.80V	<6.5V
Dual Supply = ±2.5V	>0.73V	<–2.0V
Dual Supply = ±5V	>1.45V	<0.5V
Dual Supply = ±7.5V	>2.18V	<0.5V

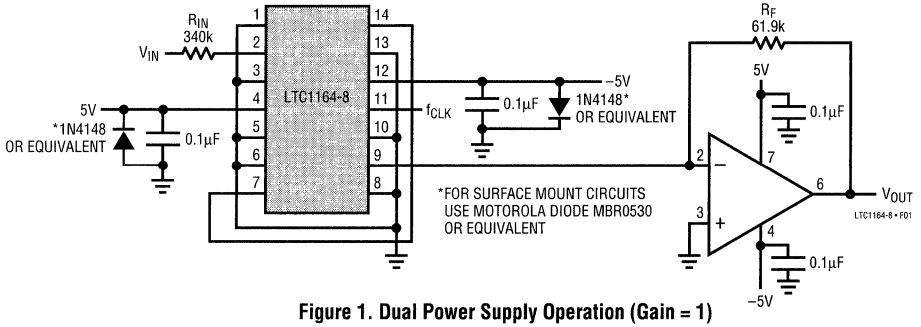


Figure 1. Dual Power Supply Operation (Gain = 1)

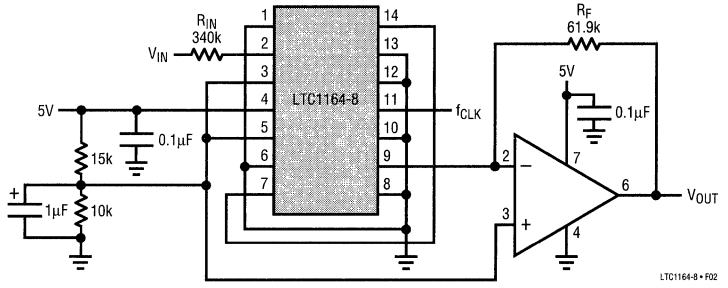


Figure 2. Single Power Supply Operation (Gain = 1)

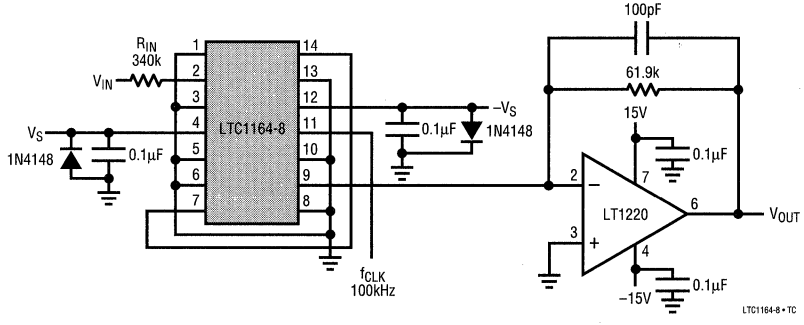
PIN FUNCTIONS

AGND (Pins 3, 5): Analog Ground Pins. For dual supply operation, pins 3 and 5 (AGND) are connected to an analog ground plane. For single supply operation, pins 3 and 5 should be biased at 1/2 of the V^+ supply and be bypassed to the analog ground plane with a 1µF (tantalum or better) capacitor (Figure 2). For optimum gain linearity and single 5V supply operation, the analog ground pins 3 and 5 should be biased at 2V. Under these conditions the typical output AC swing is 0.5V to 3.5V (please refer to the THD + Noise vs Input Voltage graph). The filter performance depends on the quality of the analog ground. For either a dual or a single supply operation, an analog ground plane surrounding the package is necessary. The analog ground plane for the filter should be connected to any digital ground plane at a single point.

INVB, INVA, I_{OUT}, [R (h, l]) (Pins 2, 7, 9, 14): External Connection Pins. Pin 2 (INVB) is the inverting input on an op amp. Pin 9 (I_{OUT}) is the junction of two internal resistors. Pin 7 (INVA) is the inverting input of an op amp, pin 14 [R (h, l)] is the junction of two internal resistors. For normal filter operation an external input resistor (R_{IN}) should be connected to input pin 2 and the output pin 9 should be connected to the inverting input of an external op amp with a feedback resistor (R_F). Also pins 7 and 14 should be connected together (Figures 1 and 2). On a printed circuit board the external connections should be less than one inch and surrounded by a ground plane. The input resistor and output op amp with feedback resistor determine the filter's gain and dynamic range. Please refer to the Applications Information section for more information.

NC (1, 6, 8, 10, 13): NC Pins. Pins 1, 6, 8, 10 and 13 are not connected to any circuit point on the device and should be tied to analog ground for dual or single supply operation.

TEST CIRCUIT



APPLICATIONS INFORMATION

Passband Gain and Dynamic Range

The filter's gain at f_{CENTER} is set with an external op amp and resistors R_{IN} and R_F (Figure 1). The filter's center frequency (f_{CENTER}) is equal to the clock frequency divided by 100. The output dynamic range of LTC1164-8 is optimized for minimum noise and maximum voltage swing when resistor R_F is 61.9k. The value of resistor R_{IN} depends on the filter's gain, and it is calculated by the equation R_{IN} = 340k/Gain. Table 2 lists the values of R_{IN} and R_F for some typical gains. *Increasing the filter's gain with resistor R_{IN} does not increase the noise generated by the filter.* Table 3 shows the noise generated by the filter with its input grounded.

Table 2. Passband Gain at Center Frequency, R_{IN} and R_F

GAIN	R_{IN} (±1%)	R_F (±1%)	GAIN IN dB	R_{IN} (±1%)	R_F (±1%)
1	340k	61.9k	0	340k	61.9k
2	169k	61.9k	10	107k	61.9k
5	68.1k	61.9k	15	60.4k	61.9k
10	34k	61.9k	20	34k	61.9k
20	16.9k	61.9k	25	19.1k	61.9k
50	6.81k	61.9k	30	10.7k	61.9k
100	3.4k	61.9k	35	6.01k	61.9k
200	1.69k	61.9k	40	3.4k	61.9k
500	680Ω	61.9k	45	1.91k	61.9k
1000	340Ω	61.9k	50	1.07k	61.9k

Table 3. LTC1164-8 Noise with Its Input Grounded

POWER SUPPLY	NOISE (μV_{RMS})
±5V	360 ±10%
Single 5V	270 ±10%

The passband of the LTC1164-8 is from 0.995 × f_{CENTER} to 1.005 × f_{CENTER}. At the passband's end points the typical filter gain is −3dB ±2dB relative to the gain at f_{CENTER}. Figure 3 shows typical passband gain variations versus percent of frequency deviation from f_{CENTER}. Outside the filter's passband, signal attenuation increases to −50dB for frequencies less than 0.96 × f_{CENTER} and greater than 1.04 × f_{CENTER}.

In applications where a signal is to be detected in the presence of wideband noise, the ultra-selectivity of the LTC1164-8 can improve the output signal-to-noise ratio. When wideband noise (white noise) appears at the input to the filter, only a small amount of input noise will reach the filter's output. If the output noise of the LTC1164-8 is neglected, the signal-to-noise ratio at the output of the filter divided by the signal-to-noise ratio at the input of the filter equals:

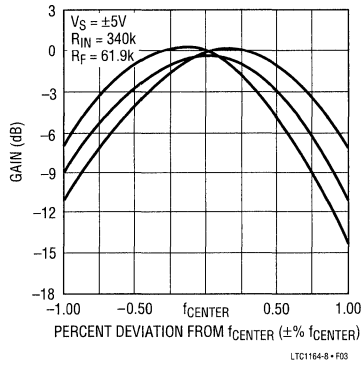


Figure 3. Typical Passband Variations

$$(S/N)_{OUT}/(S/N)_{IN} = 20 \times \text{Log} \sqrt{(BW)_{IN}/(BW)_f}$$

where,

$(BW)_{IN}$ = noise bandwidth at the input of the filter
$(BW)_f = 0.01 \times f_{CENTER}$ = noise equivalent filter bandwidth

Example: A small 1kHz signal is sent through a cable that also conducts random noise. The cable bandwidth is 3.4kHz. An LTC1164-8 is used to detect the 1kHz signal. The signal-to-noise ratio at the output of the filter is 25.3dB larger than the signal-to-noise ratio at the input of the filter ($20 \times \text{Log} \sqrt{(BW)_{IN}/(BW)_f} = 20 \times \text{Log} \sqrt{3.4\text{kHz}/0.01 \times 1\text{kHz}}$ = 25.3dB).

The AC output swing with ±5V supplies is ±4V, with a single 5V supply it is 1V to 4V, when AGND (pins 3, 5) is biased at 2.5V. Table 4 lists op amps that are recommended for use with an LTC1164-8. The LTC1164-8 is designed and specified for a dual ±5V or single 5V supply operation. The filter's passband gain linearity is optimum at single 5V supply and with pins 3, 5 (AGND) biased at 2V. Filter operation at ±7.5V supplies is not tested or specified. At V_S = 7.5V, the filter will operate with center frequencies up to 7kHz. Please refer to the Passband

APPLICATIONS INFORMATION

Variations vs Power Supply graph in the Typical Performance Characteristics.

Table 4. Recommended Op Amps for LTC1164-8

SINGLE	DUAL	QUAD
LT1006	LT1013	LT1014
LT1012	LT1078	LT1079
LT1077	LT1112	LT1114
	LT1413	

Aliasing

At the filter's output, alias signals will appear when signals at the filter's input have substantial energy very near the clock frequency or any of its multiples ($2 \times f_{CLK}$, $3 \times f_{CLK}$, ... etc.). For example, if an LTC1164-8 filter operates with a 100kHz clock and has a 99kHz, 10mV signal at its input, a 1kHz, 10mV alias signal will appear at the filter's output. Table 5 shows details.

Table 5. Aliasing (f_{CLK} = 100kHz)

INPUT FREQUENCY	OUTPUT LEVEL (RELATIVE TO INPUT)	OUTPUT FREQUENCY (ALIAS FREQUENCY)
99.04kHz (or 100.96kHz)	<–50dB	960Hz
99.02kHz (or 100.98kHz)	<–40dB	980Hz
99.01kHz (or 100.99kHz)	<–6dB	990Hz
99.005kHz (or 100.995Hz)	–3dB ±2dB	995Hz
99.00kHz (or 101.00kHz)	0dB ±1dB	1000Hz
98.995kHz (or 101.005kHz)	–3dB ±2dB	1005Hz
98.99kHz (or 101.01kHz)	<–6dB	1010Hz
98.98kHz (or 101.02kHz)	<–40dB	1020Hz
98.96kHz (or 101.04kHz)	<–50dB	1040Hz

Clock Feedthrough

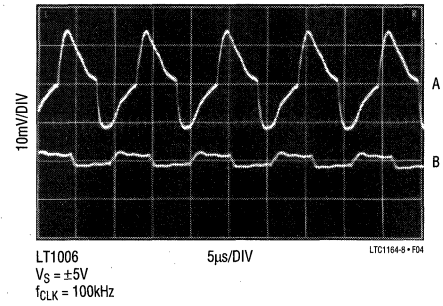


Figure 4. Clock Feedthrough at the Output of External Op Amp
A. With No Capacitor Across Feedback Resistor R_F
B. With Capacitor C_F Across Feedback Resistor R_F
$1/(2\pi \times R_F \times C_F) = 10 \times f_{CENTER}$

Transient Response

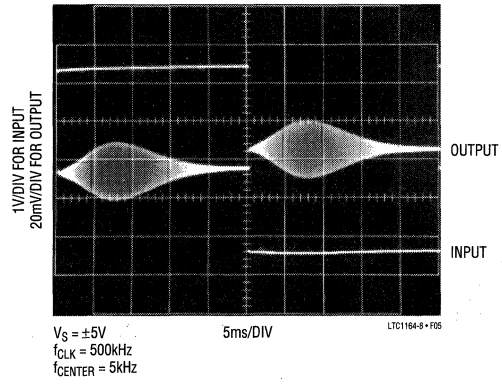


Figure 5. Square Wave Input (±2.5V)

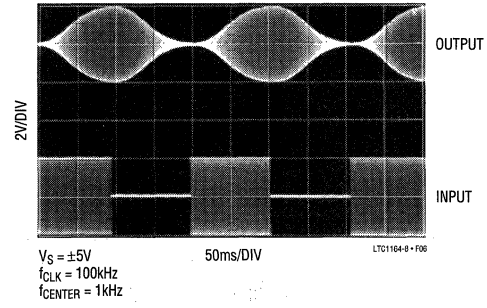


Figure 6. Sine Wave Burst Input

APPLICATIONS INFORMATION

Printed Circuit Layout

For optimum filter performance, an LTC1164-8 should be operating on a printed circuit board that has been laid out for precision analog signal processing circuits. On a printed circuit board, an LTC1164-8 should be surrounded with an adequate analog signal ground plane and its power supply pins bypassed to ground with 0.1µF capacitors. The ground plane of an LTC1164-8 and any digital ground plane should preferably meet at a single point on a system ground (star system ground).

The following external filter connections should be one inch or less:

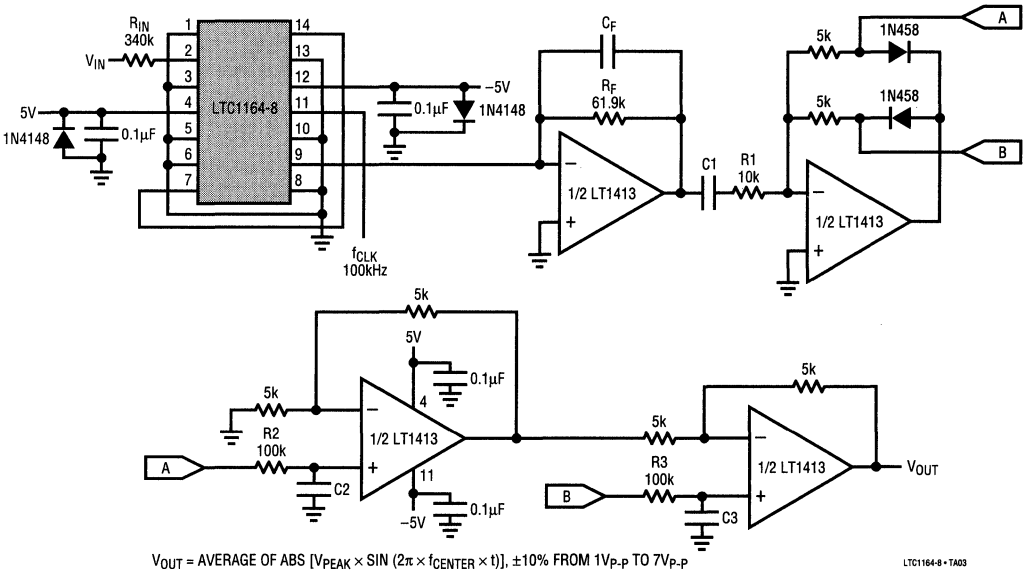
N Package
- Resistor R_{IN} to Pin 2
- Pin 14 to Pin 7
- Pin 9 to the Inverting Node of an External Op Amp
- Ground Pins 1, 3, 5, 6, 8, 10 and 13

SW Package
- Resistor R_{IN} to Pin 2
- Pin 16 to Pin 8
- Pin 9 to the Inverting Node of External Op Amp
- Ground Pins 1, 3, 5, 6, 7, 10, 11, 13 and 15

Any signal or power supply printed circuit traces should be at least 0.2 inches away from the above mentioned connections (this rule applies also to the routing of the printed circuit trace originating from a clock source in a digital circuit and terminating at a clock input pin of an LTC1164-8). **Operating an LTC1164-8 in an IC socket is not recommended.**

TYPICAL APPLICATIONS

Tone Detector and Average Value Circuit



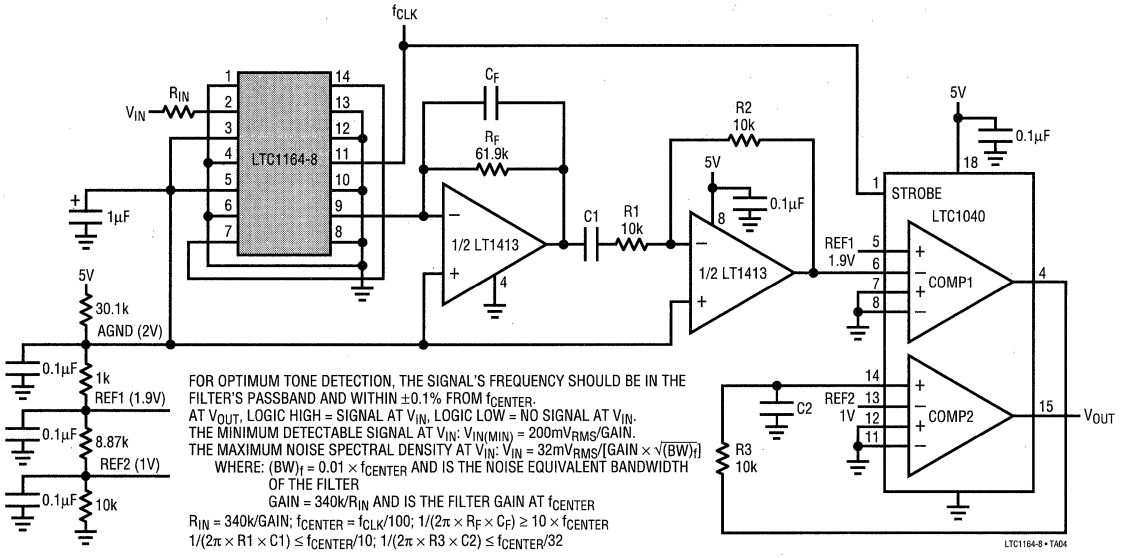
V_{OUT} = AVERAGE OF ABS [$V_{PEAK} \times SIN(2\pi \times f_{CENTER} \times t)$], ±10% FROM 1$V_{P-P}$ TO 7V_{P-P}
R_{IN} = 340k/GAIN; $f_{CENTER} = f_{CLK}/100$; $1/(2\pi \times R_F \times C_F) \geq 10 \times f_{CENTER}$
$1/(2\pi \times R1 \times C1) \leq f_{CENTER}/10$; $1/(2\pi \times R2 \times C2) \leq f_{CENTER}/25$; $R2 \times C2 = R3 \times C3$

LTC1164-8 • TA03

8

TYPICAL APPLICATIONS

Tone Detector—Detecting a Low Level Signal Buried in Wideband Noise



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1064	Universal Filter Building Block	This Part, with External Resistors, Allows Design of Bandpass Filters Similar to LTC1164-8 (Up to 50kHz)
LTC1164	Universal Filter Building Block	This Part, with External Resistors, Allows Design of Bandpass Filters Similar to LTC1164-8 (Low Power Up to 20kHz)
LTC1264	Universal Filter Building Block	This Part, with External Resistors, Allows Design of Bandpass Filters Similar to LTC1164-8 (Up to 100kHz)

See Table 4 for additional information

SECTION 9—MICROPROCESSOR SUPERVISORY CIRCUITS

SECTION 9—MICROPROCESSOR SUPERVISORY CIRCUITS

LTC Family of Supervisory Circuit Products

FUNCTION	1235	690	691	692	693	694/694-3.3	695/695-3.3	699	1232
Pushbutton Reset	X								X
Battery Backup Switching-**UL Recognized**	X	X	X	X	X	X	X		
Conditional Battery Backup	X								
RAM Write Protect	X		X		X		X		
Watchdog Timer	X	X	X	X	X	X	X	X	X
Power Fail Warning	X	X	X	X	X	X	X		
Power Up/Down Reset	X	X	X	X	X	X	X	X	X
Reset Threshold (V)	4.65	4.65	4.65	4.40	4.40	4.65/2.90	4.65/2.90	4.65	4.62[1]
Reset Pulse Width (ms)	200	50	50	200	200	200	200	200	610
Guaranteed V_{CC} Reset Level (V)	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Power Supply Current (μA)	600	600	600	600	600	600	600	600	500
Packages: Plastic	16	8	16	8	16	8	16	8	8
CERDIP		8	16			8	16		
SO	16[2]	8[3]	16[2]	8[3]	16[2]	8[3]	16[2]	8[3]	8[3]
Temperature Ranges	C	C, I	C, I	C, I	C, I	C, I	C, I	C	C

Notes: 1. 4.62V or 4.37V threshold selectable
2. 0.300" SO wide package
3. 0.150" SO narrow package
4. Temperature ranges: C = 0°C to 70°C I = –40°C to 85°C M = –55°C to 125°C

Definitions of Functions

Pushbutton Reset: Provides a manual reset input, usually triggered by a pushbutton switch, which is debounced and will initiate the usual reset sequence.

Battery Backup Switching: When V_{CC} drops below the battery voltage, V_{OUT} is connected to V_{BATT} and the device is placed in standby mode to conserve power. This provides backup power to the CMOS RAM while consuming less than 1μA of supply current. LTC devices are UL recognized for lithium battery backup.

Conditional Battery Backup: Electrically disconnects the battery during shipment and storage to prevent unnecessary discharge. Disconnection is done by detecting the power down sequencing of the supply and battery inputs.

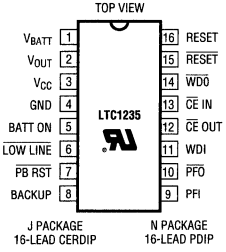
RAM Write Protect: The system RAM enable line is gated by the supervisory circuit. When the supply voltage drops below the reset voltage threshold, the enable line is inhibited, preventing erroneous data from being written into the RAM when V_{CC} is at an invalid level. The maximum enable delay for LTC's supervisors is 45ns.

Watchdog Timer: Monitors the activity of the μP. The processor must toggle this input line before the given timeout period expires, or a reset will be initiated. This function is intended to prevent μP's from becoming accidentally stalled in microcode loops indefinitely.

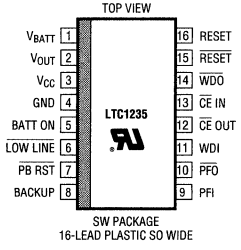
Power Fail Warning: Provides early warning to the μP of an impending power failure by monitoring the unregulated power supply. This gives the processor time to perform shutdown activities before all regulated power is lost.

Power Up/Down Reset: Resets the μP when the power supply line drops below the preset threshold. LTC's supervisors will hold the reset line low down to supply voltages of 1.0V, providing a reliable reset through V_{CC} voltages which may allow the processor to begin operation.

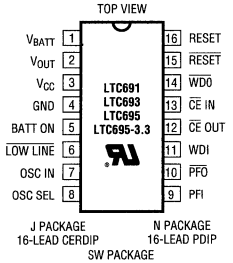
Pin Configurations



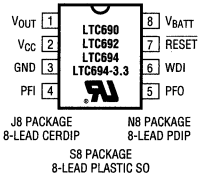
J PACKAGE 16-LEAD CERDIP
N PACKAGE 16-LEAD PDIP



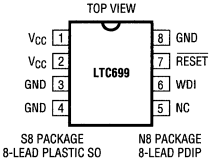
SW PACKAGE 16-LEAD PLASTIC SO WIDE



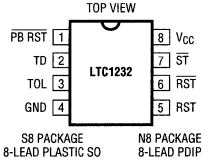
J PACKAGE 16-LEAD CERDIP
N PACKAGE 16-LEAD PDIP
SW PACKAGE 16-LEAD PLASTIC SO WIDE



J8 PACKAGE 8-LEAD CERDIP
N8 PACKAGE 8-LEAD PDIP
S8 PACKAGE 8-LEAD PLASTIC SO



S8 PACKAGE 8-LEAD PLASTIC SO
N8 PACKAGE 8-LEAD PDIP



S8 PACKAGE 8-LEAD PLASTIC SO
N8 PACKAGE 8-LEAD PDIP

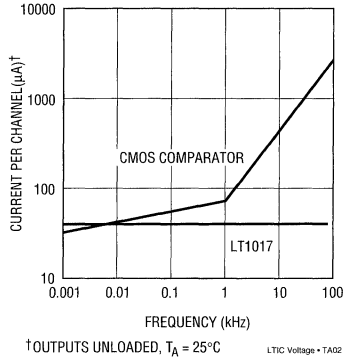
SECTION 10—COMPARATORS

SECTION10—COMPARATORS

Comparators

Response Time	V_{OS} (MAX) 20mV	10mV	3mV	2.5mV	2mV	1.5mV	1mV	0.5mV	TTL OUTPUTS	ECL OUTPUTS	QUAD	DUAL	GROUND SENSE	MICRO-POWER	ADDITIONAL COMMENTS
100µs								LTC1040				LTC1040	LTC1040	LTC1040	Sampling: Consumes 1.5µW at 1 Sample/Sec.
								LTC1041					LTC1041	LTC1041	Bang-Bang Controller: 1.5µW at 1 Sample/Sec.
							LTC1042						LTC1042	LTC1042	Sampling Window Comp.: 1.5µW at 1 Sample/Sec.
15µs							LT1017					LT1017	LT1017	LT1017	60µA Max. I_{CC}/Operates to 1.1V
12µs		LTC1443/4/5									LTC1443/4/5		LTC1443/4/5	LTC1443/4/5	Built-In Reference, 8.5µA Supply Current
4µs							LT1018					LT1018	LT1018	LT1018	250µA Max. I_{CC}/Operates to 1.1V
250ns						LT1011		LT1011A							12-Bit Accurate
14ns	LT1015								LT1015			LT1015			High Speed 2-Channel Line Receiver
			LT1116						LT1116				LT1116		Ground Sense/Single Supply
12ns				LT1016					LT1016						No Min. Input Slew Rate Requirement/Latched Output
6.5ns					LT685					LT685					Latched Outputs

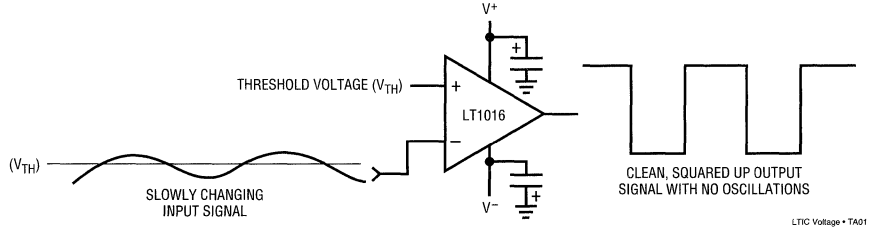
LT1017 Provides Lower Power Operation than CMOS as Input Frequency Increases



†OUTPUTS UNLOADED, T_A = 25°C

LTIC Voltage • TA02

LT1016 Doesn't Oscillate with Slowly Changing Input Signals



LTIC Voltage • TA01

10

SECTION 11—SPECIAL FUNCTION

SECTION 11—SPECIAL FUNCTIONS

Analog Switches

Family Features

- Micropower: 40μA Max Supply Current
- Single 5V or ±15V Operation
- 8pC Charge Injection
- Low ON Resistance
- Low Leakage
- Guaranteed Break Before Make

PART NUMBER	NUMBER OF CHANNELS	LATCHED INPUTS	MAX ON RESISTANCE	MAX INPUT AND OUTPUT OFF LEAKAGE	MAX SUPPLY CURRENT	MAX T_{ON}/T_{OFF}	FEATURES
LTC201A	4		125Ω	5nA	40μA	400ns/300ns	Lower ON Resistance, Charge Injection, Supply Current Than DG201A. Single 5V to ±15V Supply Operation
LTC202	4		125Ω	5nA	40μA	400ns/300ns	Lower ON Resistance, Charge Injection, Supply Current Than DG202. Single 5V to ±15V Supply Operation
LTC203	4		125Ω	5nA	40μA	400ns/300ns	Low ON Resistance, Charge Injection, Supply Current
LTC221	4	X	90Ω	5nA	40μA	400ns/300ns	Lower Charge Injection, Supply Current Than DG221
LTC222	4	X	90Ω	5nA	40μA	400ns/300ns	Lower Charge Injection, Supply Current Than DG222

Other Products

PART NUMBER	DESCRIPTION	PACKAGE OPTIONS	FEATURES
LF198(A)/LF398(A)	Sample-and-Hold Amplifier	H, J8, N8, S	12-Bit Accurate (LF198A), 6μs Acquisition Time, 0.005% Max Gain Error.
LM134/LM334	Adjustable Current Source	H, Z, S8	1μA to 10mA Adjustment Range, Floating Current Source, 0.02%/V Regulation, Can Be Used as Temperature Sensor.
LT1025	Thermocouple Cold Junction Compensator	J8, N8	Provides 0°C Cold Junction Compensation of Types E, J, K, R, S, T Thermocouples. Low Supply Current (80μA) and Operates with Single 4V to 36V DC Supply.
LT1088	RMS to DC Converter	D, N	Thermal RMS to DC Conversion Permits 1% Accuracy to 50MHz, 2% to 100MHz and Handles Crest Factor up to 50:1.
LTC1043	Precision Switched-Capacitor Building Block	D, N, S	120dB CMRR, when Used as Instrumentation Front End, Allows Switched-Capacitor Design Techniques at Board Level.
LTK001	Thermocouple Cold Junction Compensator Matched Amplifier	J, N	LT1025 with Matched Amplifier (LTKA00 or LTKA01) Provides Lower Error Specs than Using Worst Case Errors of LT1025 and Standard Precision Op Amp.

SECTION 12—MILITARY PRODUCTS

SECTION 12—MILITARY PRODUCTS

NOTE

Military product data sheets are available from your local LTC Sales Representative, or by calling LTC Communications at (800) 637-5545.

LINEAR TECHNOLOGY MILITARY PRODUCTS/ PROGRAMS

Linear Technology Corporation (LTC) offers a comprehensive range of high performance analog/linear integrated circuits including; Data Converters, Interface devices, High Speed Amplifiers, Precision Operational Amplifiers, Comparators, Voltage References, DC-DC Converters, Switches, Voltage Regulators, Switching Regulators, PWMs, and other special function products serving the rigorous demands of the military marketplace.

The Company's specification system, quality procedures and policies were set up from the beginning to meet the exacting demands of MIL-Q-9858 (Quality Program Requirements), MIL-I-45208 (Inspection System Requirements), MIL-M-38510 (General Specification for Microcircuits), MIL-STD-976 (Certification Requirements for Microcircuits), MIL-STD-883 (Test Methods and Procedures for Microelectronics) and more recently the ISO 9000 (Internal Standards for Quality Management).

In addition, the Company has introduced a line of radiation tolerant devices which are offered with two different in-house levels of enhanced reliability processing to serve ground, air and/or space applications, including customer generated Source Controlled Drawings (SCDs) for a variety of missions.

LTC's military programs include:

- JAN Class S
- JAN Class B
- Standard Military Drawings (SMDs)
- 883
- Hi-Rel (SCDs)
- LTC "RH", Radiation hardened devices

LTC JAN

At the end of 1969, the Solid State Applications Branch of the Rome Air Development Center (RADC) issued the first copy of MIL-M-38510. This general specification for microcircuits established the procedures that a manufacturer must follow to have products listed on the Qualified Parts List (QPL).

One major problem faced by defense contractors using semiconductor devices was the inability to interchange devices caused by a proliferation of non-standard electrical specifications. The 38510 (JAN) program addressed this problem by publishing detailed electrical specifications (slash sheets) for each component to be listed on the QPL.

JAN devices are completely processed in the United States or its territories and all wafer fabrication, wafer sort, assembly, testing, and conformance testing are performed onshore.

In August 1984, LTC was visited by a team of Defense Electronics Supply Center (DESC) personnel. This team spent almost four days auditing LTC and at the end of the visit they awarded the Company "Class B Line Certification." *This was a first for any company to receive this distinction on their first audit!*

In early 1985, LTC joined the ranks of the eighteen existing QPL suppliers. Of these eighteen, only a handful of suppliers participate in the linear military JAN market. LTC believes its analog design experience and manufacturing strength has and will continue to make significant contributions to this market.

LTC's first QPL listing was achieved in February 1985, one year after the Company made JAN Class B a corporate

goal. Other companies have typically taken 2 to 3 years to achieve this status. The line certification and QPL approvals were awarded to MIL-M-38510 and MIL-STD-883 specifications. Since that time the Company has been reaudited to the latest revisions of these specifications and has maintained an uninterrupted certification record for the manufacture of JAN QPL products.

In November 1987, LTC was audited by a team from DESC, Naval Weapons Support Center and Aerospace Corporation and was awarded "Class S Line Certification."

LTC's policy of providing JAN linear components supports the United States Government's position of standardization to decrease the number of active part types maintained by DESC. This number is currently in excess of 85,000 for all types of components (contrasted to approximately 8,000 industry standard components). Standardization will clearly decrease costs and assist in the maintenance of military weapons systems and equipment now in the field.

LTC maintains its JAN product offerings under the current revision of MIL-I-38535, Appendix A. LTC now offers 45 products listed on the Class B Qualified Parts List (Part 1) and 40 products on the Class S Qualified Parts List (Part 1). To receive an updated copy of LTC's current JAN QPL product offering, contact your local LTC sales office or LTC Military Marketing.

For JAN Flows see Figure 1 and Figure 2.

In June 1994, LTC was granted transitional Qualified Manufacturers List (QML) certification to MIL-I-38535 by DESC, and will be pursuing full QML certification.

LTC Standard Military Drawings

DESC drawings were initiated in 1976 to standardize the electrical requirements for full temperature-tested military components. These DESC drawings (or minispecs) were initially issued for low power Schottky devices (54LS) used by defense subcontractors on the Air Force's F16. The program accomplished standardization of testing, without the delays associated with the qualification process for JAN components.

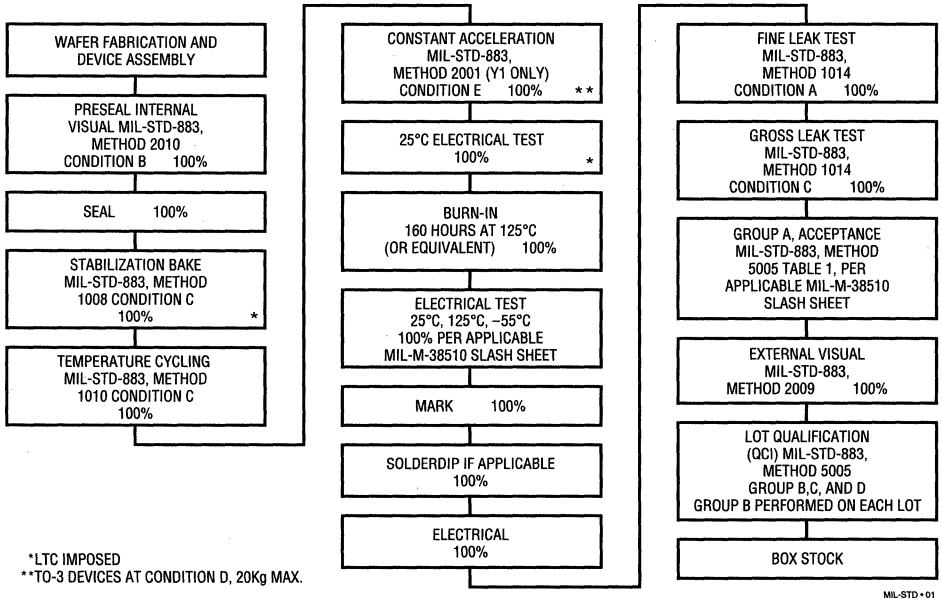
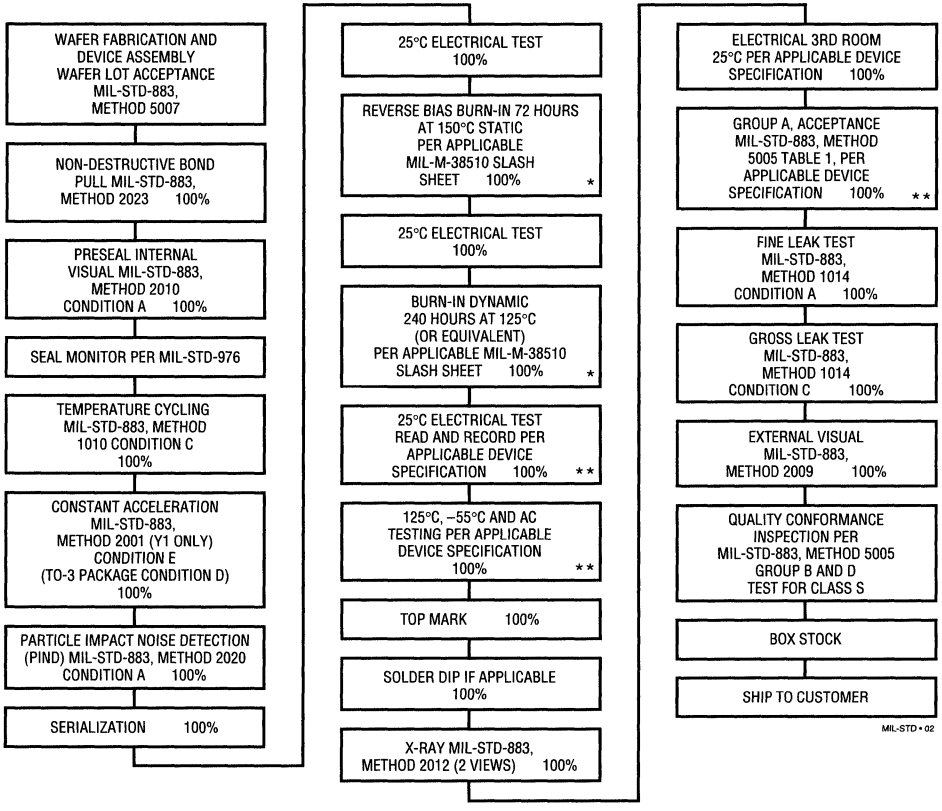


Figure 1. MIL-M-38510 Class B Flow



* IN THE CASE WHERE THERE IS NO APPLICABLE MIL-M38510 SLASH SHEET, THE BURN-IN SCHEMATIC AS WELL AS THE APPLICABILITY OF 100% DYNAMIC BURN-IN SHALL BE NEGOTIATED BETWEEN THE CUSTOMER AND LINEAR TECHNOLOGY CORPORATION.
** APPLICABLE DEVICE SPECIFICATION SHALL BE THE MIL-M38510 DEVICE SPECIFICATION, OR A DEVICE SPECIFICATION AGREED UPON BETWEEN THE CUSTOMER AND LINEAR TECHNOLOGY CORPORATION.
* CUSTOMER SOURCE INSPECTION WILL BE ADDED AS SPECIFIED IN CUSTOMER'S PURCHASE ORDER.

Figure 2. MIL-M-38510 Class S Flow

The DESC drawing was viewed as a preliminary specification prior to JAN approval, and it ranks second in the order of purchasing hierarchy to JAN. This order is defined in Requirement 64 of MIL-STD-454. If a JAN part is available, it is still preferred, however, there are many types of devices where the volume is such that the cost of a full JAN qualification may not be justified, but where a need exists for electrical standardization.

CMOS and analog circuits were added to the DESC Drawing Program in 1977, 1978 and 1979, but widespread acceptance of these parts was not achieved. Today with more emphasis being placed on standardization, the interest level in DESC drawings has accelerated. This category of product can be built offshore with 883-level processing and the electrical parameters are tested specifically to the DESC drawing.

To provide parts to a DESC drawing, a manufacturer has to have at least one part on the 38510 QPL. He must also provide DESC with a certificate of compliance agreeing to the tests and conditions listed on the drawing.

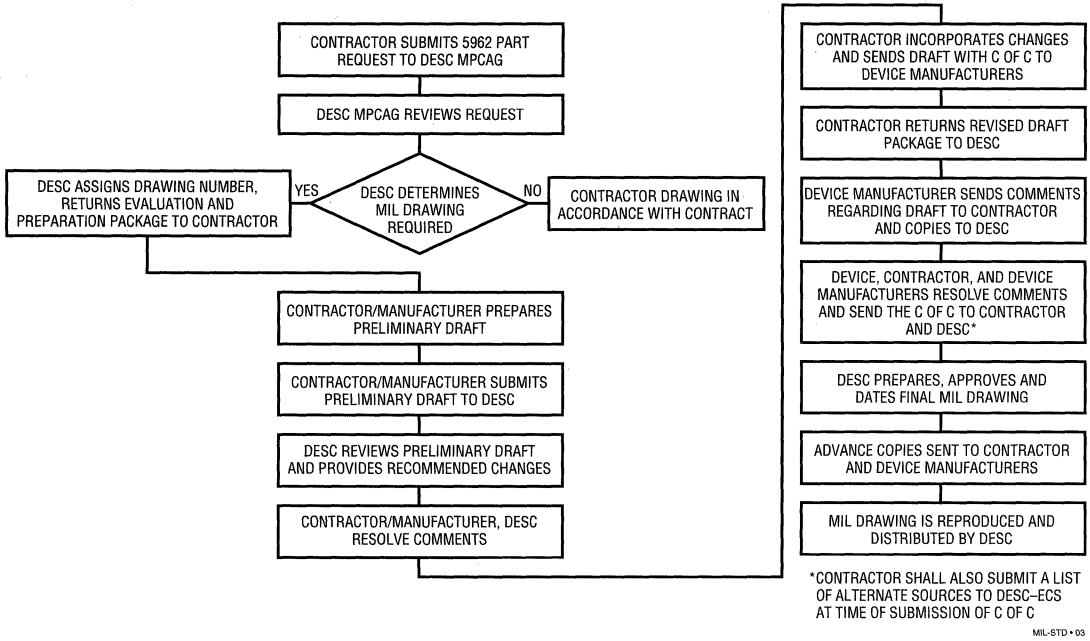


Figure 3. SMD Preparation Flowchart

In 1986 a new program named Standard Military Drawings (SMDs) was launched by DESC. This replaced the previous DESC Drawing Program. This new program is aimed directly at standardizing electrical requirements with the objective to decrease the time required to issue a military drawing. To achieve this, we have set up a computer link-up with the DESC Standardized Mil Drawing Group. LTC is actively supporting this Standard Military Drawing program and we are working closely with DESC and OEMs to participate in this government plan toward a greater level of standardization in military specifications.

LTC has over 134 devices listed on DESC and Mil drawings, and we are actively supporting these standardization programs by having parts available off the shelf from LTC and from distribution outlets.

For SMD Flow see Figure 3.

SMDs Get A New Part Numbering System

A new numbering system has been introduced to standardize the part numbering system for JAN 38510 and SMD (Standard Military Drawing) products.

Under the new system, the SMD number 5962-XXXXXZZ(_)YY will be used, with a minor change for the 38510 qual'd devices. This will make one part have one part number with just the grade identification being different (M = SMD, B = JAN B and S = JAN S). An example of this follows:

Old System

LTC PART NUMBER	"OLD" SMD NO.	JAN PART NUMBER
LT1021CMH-5/883	5962-8876202GA	JM38510/12407BGA

New System

LTC PART NUMBER	"NEW" SMD ONE PART NUMBER SYSTEM
LT1021CMH-5/883	5962-8876202(M, B or S)GA

This was implemented on January 1, 1990, for all SMDs and slash sheets created after this date. Devices listed or approved in the past will retain their respective existing part numbers.

LTC MIL-STD-883 Product

The semiconductor industry 883 designation on military semiconductor components established a defacto standard in response to a significant demand from the military defense contractors. The Government recognized the existence of 883 components in the recent revisions of MIL-STD-883. Requirements for compliant 883 components are now defined very specifically in paragraph 1.2.1 of this document.

MIL-STD-883 is a test procedures and methods document which is revised periodically and defines the conditions for two categories of product, Class B and Class S. Class B is intended for applications where maintenance is difficult or expensive and where reliability is vital. Class S is intended for space and critical applications where replacement is extremely difficult or impossible and where reliability is imperative.

On December 31, 1984, a key clause was added to MIL-STD-883, "paragraph 1.2.1." This states that if a manufacturer advertises, certifies, or marks parts as compliant with MIL-STD-883 those parts must meet all of the provisions of MIL-STD-883, a practice consistent with "Truth in Advertising."

According to the Defense Electronics Supply Center (a branch of the Defense Department's Logistics Agency), the intent of paragraph 1.2.1 was to link MIL-STD-883 with the controls and details contained in MIL-M-38510, and, by extension, MIL-I-38535, Appendix A.

LTC can state that all of its 883 products are in full compliance with the latest revision of MIL-STD-883. We have over 333 versions of our 883 products listed in our current catalog, including operational amplifiers, voltage regulators, voltage references, comparators, and our advanced line of proprietary CMOS circuits.

Table 1. LTC 883 Group A Sampling Plan

		883	
TEST	**CONDITION**	**SAMPLE SIZE**	**ACCEPT**
DC Parametric	$T_A = 25°C$	116	0
DC Parametric	$T_A = -55°C$	116	0
	$+125°C$	116	0
AC Parametric	$T_A = 25°C$	116	0

LTC Hi-Rel (SCDs)

LTC recognizes the need for Source Controlled Drawings (SCDs) and the Company's DESC-certified line is well equipped to handle these requirements for space and hi-rel applications. The Company has a comprehensive specification review procedure and emphasis is placed on compliance to test methods and procedures. Over 8,000 specifications have been reviewed to date with fast feedback to our customers.

LTC has serviced SCD orders including "S" level specifications with an emphasis on compliance with customer purchase order requirements and on-time delivery performance. A dedicated SL traveller is initiated to baseline the manufacturing and test flow requirements to service each order.

LTC's Product Marketing Group can provide you with more details on a case-by-case basis.

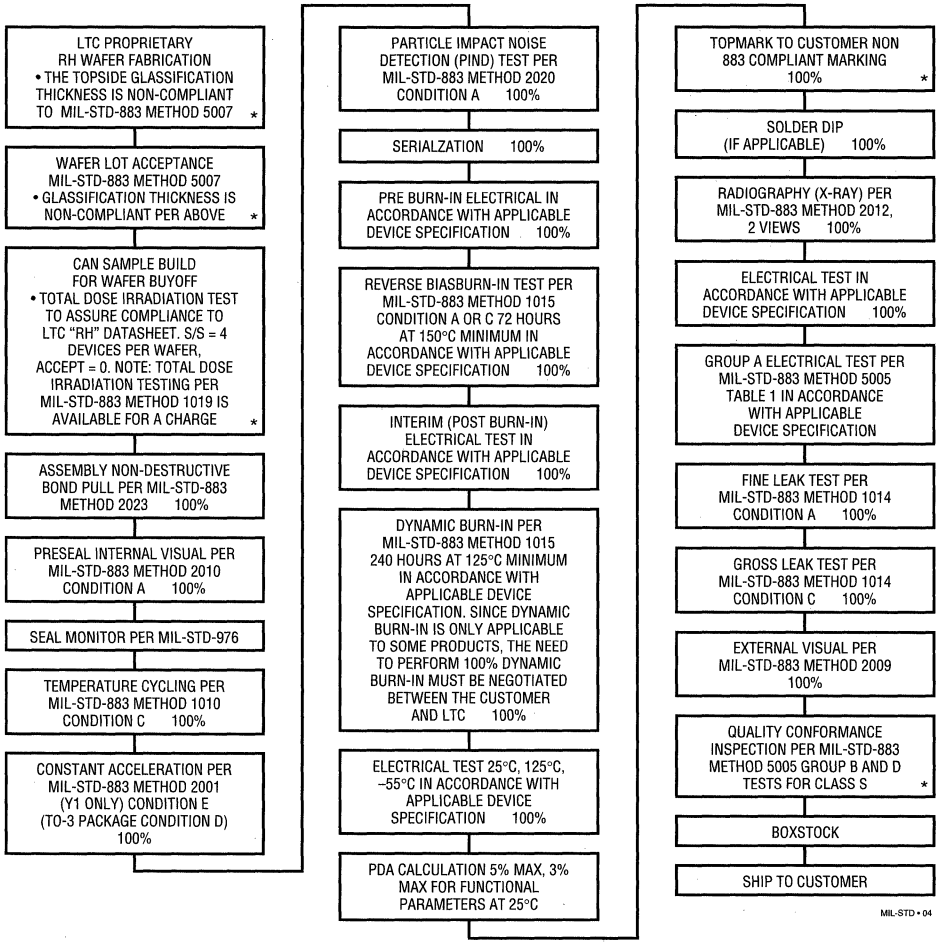
LTC's Radiation Hardness Program

LTC has developed a proprietary design/wafer fabrication process for RAD HARD (RH prefix) products, complemented by a separate set of RH data sheets. Each RH data sheet specifies the end point electrical test requirements for Total Dose irradiation testing performed on a sample basis. We offer in certain cases, the option of using the slash sheet electricals for the pre-radiation test limits instead of the LTC RH data sheet electricals. But in all cases the post-radiation electricals are per LTC's RH data sheets.

Due to the unique wafer processing required to make RH products, the RH products are not totally compliant with all the Class S requirements of MIL-STD-883. Since MIL-STD-883 specifically prohibits the marking of non-compliant products with the 883 compliance (c) indicator, LTC's RH products are marked with the LTC RH prefix part number or with a special mark specified by the customer.

Military Market Commitment

LTC is a focused, dedicated company servicing the needs of the linear military marketplace. We are shipping to the top U.S. defense electronics contractors who have qualified and approved our products. LTC is committed to being the best and most proficient high quality supplier of analog military components.



NOTE: 1. APPLICABLE DEVICE SPECIFICATION SHALL BE THE MIL-M-38510 DEVICE SPECIFICATION, OR A DEVICE SPECIFICATION AGREED UPON BETWEEN THE CUSTOMER AND LTC.
2. CUSTOMER SOURCE INSPECTION WILL BE ADDED AS SPECIFIED ON CUSTOMER'S PURCHASE ORDER.

* DENOTES PROCESS STEPS THAT ARE NON-COMPLIANT TO THE CLASS S REQUIREMENTS OF MIL-STD-883. FOR MORE DETAILS CONSULT THE FACTORY.

Figure 4. LTC Representative "RH" Product Manufacturing Flow

883 CERTIFICATE OF CONFORMANCE — LEVEL B

.TC Part Number _____

.ot Traceability No. _____

'urchase Order No. _____

QUALITY ASSURANCE INSPECTOR	
DATE	SIGNATURE

;ustomer Name _____ P/N _____ Qty _____

)ate Code _____ Shipper # _____ Traveller Lot # _____

;roup A = _____ Group B = _____ Group C = _____ Group D = _____

;roup B/3 Re-Inspection Date, If Applicable _____

.INEAR TECHNOLOGY CORPORATION HEREBY DECLARES THAT THE COMPONENTS SPECIFIED ON THE ABOVE 'URCHASE ORDER COMPLY WITH YOUR SPECIFICATIONS AND REQUIREMENTS OF MIL-STD-883. ALL ;UPPORTING DOCUMENTATION AND RECORDS ARE RETAINED ON FILE BY LTC AND ARE AVAILABLE FOR NSPECTION. THE MAJOR ELEMENTS OF THE 883 PROGRAM ARE SHOWN BELOW.

Operation	Screening Procedure MIL-STD-883, Method 5004	
Internal Visual	Method 2010, Condition B	
Temperature Cycling	Method 1010, Condition C, 10 cycles –65°C to 150°C	
Constant Acceleration	Method 2001, Condition E, 30k g Y1 axis (TO-3 PKG Condition D at 20k g)	
Fine Leak	Method 1014, Condition A	
Gross Leak	Method 1014, Condition C	
Burn-in	Method 1015, 160 hrs at 125°C (or equivalent)	
Final Electrical	+25°C DC (per LTC Data Sheet) PDA = 5%	
	+125°C or 150°C DC	
	–55°C DC	
	+25°C AC	
QA Acceptance	Method 5005	Group A (sample/lot)
Quality Conformance		Group B (sample/lot)
		Group C (sample every 6 months/Circuit Group)
		Group D (sample every 6 months/Package Family)
External Visual	Method 2009	

NOTE: Each operation is performed on a 100% basis unless otherwise stated.

FORM No. 00-03-6072

.INEAR TECHNOLOGY CORPORATION
630 McCarthy Blvd.
Milpitas, CA 95035-7487

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LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP A DATA
Mil-Std-883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

	ACC #	S/S	# FAILED	DATE TESTED	OPER NUMBER
SUBGROUP 1 Static tests at 25°C	0	116			
SUBGROUP 2 Static tests at maximum rated operating temperature	0	116			
SUBGROUP 3 Static tests at minimum rated operating temperature	0	116			
SUBGROUP 4 Dynamic tests at 25°C	0	116			
SUBGROUP 5 Dynamic tests at maximum rated operating temperature	0	116			
SUBGROUP 6 Dynamic tests at minimum rated operating temperature	0	116			
SUBGROUP 7 Functional tests at 25°C	0	116			
SUBGROUP 8 Functional tests at maximum and minimum operating temperature	0	116			
SUBGROUP 9 Switching tests at 25°C	0	116			
SUBGROUP 10 Switching tests at maximum rated operating temperature	0	116			
SUBGROUP 11 Switching tests at minimum rated operating temperature	0	116			

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6037

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP B DATA (Class B)
Mil-Std-883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	SAMPLE SIZE SERIES	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 2 Resistance to Solvents	2015			0	3			
SUBGROUP 3 Solderability	2003	Soldering Temp. of 245°C ± 5°C	10	0				
SUBGROUP 5 Bond Strength	2011	C or D	15	0				

EXAMPLE

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6006

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP C DATA (Class B)
Mil-Std-883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE:
_____ CT. GROUP: _____

TEST	METHOD	CONDITION	SAMPLE SIZE SERIES	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1 Steady State Life Test Electrical Endpoints	1005	T_A = 125°C (1000 Hours or Equiv.) Test #	5	0	45			

EXAMPLE

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6007

12

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Blvd.
Milpitas, CA 95035-7487

GROUP B DATA (Class S)
Mil-Std-883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	SAMPLE SIZE SERIES	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1								
Physical Dimensions	2016							
Internal Water-Vapor Content	1018	5000 ppm Max						
SUBGROUP 2								
Resistance to Solvents	2015			0	3			
Internal Visual and Mechanical	2013, 2014	Design and Construction Requirements		0	2			
Bond Strength	2011	C or D	10	0	22 Wires			
Die Shear Test	2019			0	3			
SUBGROUP 3								
Solderability	2003 or 2022	Soldering Temp. of 245°C ±5°C	10	0	22 Leads			
SUBGROUP 4								
Lead Integrity	2004	B_2 (Lead Fatigue)	5	0	45 Leads			
Seal	1014							
Fine								
Gross								
Lid Torque	2024	Glass Frit Seal Only						
SUBGROUP 5								
Electrical End-Points		Test #	5	0	45			
Steady State Life	1005	C, D, or E						
Electrical End-Points		Test #						
SUBGROUP 6								
Electrical End-Points		Test #	15	0	15			
Temperature Cycling	1010	C 100 Cycles						
Constant Acceleration	2001	E Y_1 Only						
Seal	1014	(TO-3 at Condition D, 20Kg)						
Fine								
Gross								
Electrical End-Points		Test #						
SUBGROUP 7								
ESD Classification	3015	Qual or Re-Design Only	15	N/A	—			

QA APPROVAL: _____ DATE: _____

INEAR TECHNOLOGY CORPORATION
630 McCarthy Blvd.
'ilpitas, CA 95035-7487

GROUP D DATA (Class B or S)
Mil-Std-883, METHOD 5005

LTC P/N: _____ LOT #: _____
GENERIC TYPE: _____ PKG: _____ DATE CODE: _____
ASSEMBLY LOC: _____

TEST	METHOD	CONDITION	SAMPLE SIZE SERIES	ACC #	S/S	# FAILED	DATE TESTED	OPER #
SUBGROUP 1			15	0	15			
Physical Dimensions	2016							
SUBGROUP 2			5	0	45 Leads			
Lead Integrity	2004	B_2 (Lead Fatigue)						
Fine Leak	1014							
Gross Leak	1014							
SUBGROUP 3			15	0	15			
Thermal Shock	1011	B 15 Cycles						
Temperature Cycle	1010	C 100 Cycles						
Moisture Resistance	1004							
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1004/ 1010							
Electrical End-Points		Test #						
SUBGROUP 4			15	0	15			
Mechanical Shock	2002	B						
Vibration, Variable Frequency	2007	A						
Constant Acceleration	2001	E Y1 Only						
Fine Leak	1014							
Gross Leak	1014	(TO-3 at						
Visual Examination	1010/ 1011	Condition D, 20Kg)						
Electrical End-Points		Test #						
SUBGROUP 5				15	0	15		
Salt Atmosphere	1009	A						
Fine Leak	1014							
Gross Leak	1014							
Visual Examination	1009	Visual Criteria						
SUBGROUP 6				0	3			
Internal Water-Vapor	1018	5000 ppm Max						
SUBGROUP 7			15	0	15			
Adhesion of Lead Finish	2025							
SUBGROUP 8				0	5			
Lid Torque	2024	Glass Frit Seal Only						

QA APPROVAL: _____ DATE: _____

FORM No. 00-03-6008

MILITARY PARTS LIST

JAN S QPL

JM38510/10103SGA (LM101AH)
JM38510/10103SHA (LM101AW)
JM38510/10103SPA (LM101AJ8)
JM38510/10104SCA (LM108AJ)
JM38510/10104SGA (LM108AH)
JM38510/10104SHA (LM108AW)
JM38510/10104SPA (LM108AJ8)
JM38510/10107SGA (LM118H)
JM38510/10304SGA (LM111H)
JM38510/10306SCA (LM119J)
JM38510/10306SIA (LM119H)
JM38510/10306SHA (LM119W)
JM38510/10307SCA (LT119AJ)
JM38510/10307SIA (LT119AH)
JM38510/10307SHA (LT119AW)
JM38510/11401SPA (LF155J8)
JM38510/11402SGA (LF156H)
JM38510/11402SPA (LF156J8)
JM38510/11404SGA (LF155AH)
JM38510/11404SPA (LF155AJ8)
JM38510/11405SGA (LF156AH)
JM38510/11405SPA (LF156AJ8)
JM38510/11703SXA (LM117H)
JM38510/11704SYA (LM117K)
JM38510/11803SXA (LM137H)
JM38510/11804SYA (LM137K)
JM38510/12407SGA (LT1021-5H)
JM38510/12408SGA (LT1021-7H)
JM38510/12409SGA (LT1021-10H)
JM38510/12501SGA (LF198H)
JM38510/13501SGA (OP07AH)
JM38510/13501SPA (OP07AJ8)
JM38510/13502SGA (OP07H)
JM38510/13502SPA (OP07J8)
JM38510/13503SGA (OP27AH)
JM38510/13503SPA (OP27AJ8)
JM38510/14802SXA (LT1009H)

JAN B QPL

JM38510/10103BCA (LM101AJ)
JM38510/10103BGA (LM101AH)
JM38510/10103BHA (LM101AW)
JM38510/10103BPA (LM101AJ8)
JM38510/10104BCA (LM108AJ)
JM38510/10104BGA (LM108AH)
JM38510/10104BPA (LM108AJ8)
JM38510/10106BEA (LH2108AD)
JM38510/10107BCA (LM118J)
JM38510/10107BGA (LM118H)
JM38510/10107BHA (LM118W)
JM38510/10107BPA (LM118J8)
JM38510/10304BGA (LM111H)
JM38510/10306BIA (LM119H)
JM38510/10306BCA (LM119J)
JM38510/10306BHA (LM119W)
JM38510/10307BCA (LT119AJ)
JM38510/10307BIA (LT119AH)
JM38510/10307BHA (LT119AW)
JM38510/11401BGA (LF155H)
JM38510/11401BPA (LF155J8)
JM38510/11402BGA (LF156H)
JM38510/11402BHA (LF156W)
JM38510/11402BPA (LF156J8)
JM38510/11404BGA (LF155AH)
JM38510/11404BPA (LF155AJ8)
JM38510/11405BGA (LF156AH)
JM38510/11405BHA (LF156W)
JM38510/11405BPA (LF156AJ8)
JM38510/11703BXA (LM117H)
JM38510/11704BYA (LM117K)
JM38510/11706BYA (LM138K)
JM38510/11803BXA (LM137H)
JM38510/11804BYA (LM137K)
JM38510/12407BGA (LT1021-5H)
JM38510/12408BGA (LT1021-7H)
JM38510/12409BGA (LT1021-10H)
JM38510/12501BGA (LF198H)
JM38510/13501BGA (OP07AH)
JM38510/13501BPA (OP07AJ8)
JM38510/13502BGA (OP07H)
JM38510/13502BPA (OP07J8)
JM38510/13503BGA (OP27AH)
JM38510/13503BPA (OP27AJ8)
JM38510/14802BXA (LT1009H)

DESC Drawings

7703401XA (LM117H)
7703401YA (LM117K)
7703402XA (LM117HVH)
7703402YA (LM117HVK)
7703403XA (LM137H)
7703403YA (LM137K)
7703404XA (LM137HVH)
7703404YA (LM137HVK)
7703405XA (LT117AH)
7703405YA (LT117AK)
7703406XA (LT137AH)
7703406YA (LT137AK)
7703407XA (LT117AHVH)
7703407YA (LT117AHVK)
7703408XA (LT137AHVH)
7703408YA (LT137AHVK)
7802801EA (SG1524J)
8203601GA (OP07AH)
8203601PA (OP07AJ8)
8203602GA (OP07H)
8203602PA (OP07J8)
8418001XA (LM136AH-2.5)
8551401GA (REF02AH)
8551401PA (REF02AJ8)
8600801EA (LT685)
8601401CA (LM119J)
8601401HA (LM119W)
8601401IA (LM119H)
8601402CA (LT119AJ)
8601402HA (LT119AW)
8601402IA (LT119AH)
8687702XA (LT111AH)
8687702PA (LT111AJ8)

Standard Military Drawings (SMD)

5962-3870701MGA (LTC1044MH)
5962-3870702MPA (LTC1044MJ)
5962-8680601EA (LT1846J)
5962-8680602EA (LT1847J)
5962-8684501IA (LT1016MH)
5962-8684501PA (LT1016MJ8)
5962-8686101XA (LT580SH)
5962-8686102XA (LT580TH)
5962-8686103XA (LT580UH)
5962-8687701GA (LT111AH)
5962-8687701PA (LT111AJ8)
5962-8688201XA (LH0070-0H)
5962-8688202XA (LH0070-1H)
5962-8688203XA (LH0070-2H)
5962-8688701CA (OP227AJ)
5962-8757801GA (LT1007AMH)
5962-8757801PA (LT1007AMJ8)
5962-8759401XA (LM185H-1.2)
5962-8759402XA (LM185H-2.5)
5962-8760401GA (LM10H)
5962-8760401PA (LM10J8)
5962-8766601VA (LT1080MJ)
5962-8766602EA (LT1081MJ)
5962-8767501XA (LM150K)
5962-8767502XA (LT150AK)
5962-8771501CA (LT1002AMJ)
5962-8773801GA (LT1001MH)
5962-8773801PA (LT1001MJ8)
5962-87738036A (LT1001AMH)
5962-87738036PA (LT1001AMJ)
5962-8774101XA (LT1033MK)
5962-8777501YA (LM123K)
5962-8777502YA (LM123AK)
5962-8853701GA (OP37AH)
5962-8853701PA (OP37AJ8)
5962-8853702GA (OP37BH)
5962-8853702PA (OP37BJ8)
5962-8853703GA (OP37CH)
5962-8853703PA (OP37CJ8)
5962-8856101XA (LM199AH)
5962-8856102XA (LM199H)
5962-8856201XA (LT1010MH)
5962-8856201YA (LT1010MK)
5962-8856701GA (LT1037AMH)
5962-8856701PA (LT1037AMJ8)
5962-8859701XA (LT1004MH-1.2)
5962-8859702XA (LT1004MH-2.5)
5962-8860001GA (LT1021BMH-10)
5962-8860002GA (LT1021CMH-10)
5962-8860003GA (LT1021DMH-10)
5962-8862201GA (LT1028MH)
5962-8862201PA (LT1028MJ8)
5962-8862202GA (LT1028AMH)
5962-8862202PA (LT1028AMJ8)
5962-8864101RA (LTC1060AMJ)
5962-8864102RA (LTC1060MJ)
5962-8864601XA (LT1085MK)
5962-8864701GA (LT1021BMH-7)
5962-8864702GA (LT1021DMH-7)
5962-8875101VA (LT1039MJ)
5962-8875102EA (LT1039MJ16)
5962-8876001GA (LT1013AMH)
5962-8876001PA (LT1013AMJ8)
5962-8876002GA (LT1013MH)
5962-8876002PA (LT1013MJ8)
5962-8876201GA (LT1021BMH-5)
5962-8876202GA (LT1021CMH-5)
5962-8876203GA (LT1021DMH-5)
5962-8944001CA (LT1032MJ)
5962-8948301LA (LTC1064MJ)
5962-8950401GA (LT1017MH)
5962-8950401PA (LT1017MJ8)
5962-8950402GA (LT1018MH)
5962-8950402PA (LT1018MJ8)
5962-8951101EA (LT1525AJ)
5962-8951102EA (LT1527AJ)
5962-8952101XA (LT1084MK)
5962-8956201GA (LT1054MH)
5962-8956201PA (LT1054MJ8)
5962-8958101GA (REF01AH)
5962-8958101PA (REF01AJ8)
5962-8961001XA (LT1009MH)
5962-8962201GA (LT1022AMH)
5962-8962202GA (LT1022MH)
5962-8967701CA (LT1014AMJ)
5962-8967702CA (LT1014MJ)
5962-8978201CA (LTC1052MJ)
5962-8978201GA (LTC1052MH)
5962-8978201PA (LTC1052MJ8)
5962-8980201XA (LT1031BMH)
5962-8980202XA (LT1031CMH)
5962-8980203XA (LT1031DMH)
5962-8983002RA (LTC1290BMJ)
5962-8983003RA (LTC1290CMJ)
5962-8983004RA (LTC1290DMJ)
5962-8987301YA (LT1003MK)
5962-8989701CA (LT1058AMJ)
5962-8989701XA (LT1058AML)
5962-8989702CA (LT1058MJ)
5962-8992101XA (LM129AH)
5962-8992102XA (LM129BH)
5962-8992103XA (LM129CH)
5962-8997601GA (LT1055AMH)
5962-8997602GA (LT1056AMH)
5962-8997603GA (LT1055MH)
5962-8997604GA (LT1056MH)
5962-8998101XA (LT1086MK)
5962-8998101YA (LT1086MH)
5962-9050701XA (LM134H-3)
5962-9050702XA (LM134H-6)
5962-9050703XA (LM134H)
5962-9051901XA (LT1029AMH)
5962-9051902XA (LT1029MH)
5962-9054501RA (LTC1045MJ)
5962-9056801CA (OP237AJ)
5962-9056802CA (OP237CJ)
5962-9059501GA (LT1019AMH-10)
5962-9059502GA (LT1019AMH-5)
5962-9059503GA (LT1019AMH-4.5)
5962-9059504GA (LT1019AMH-2.5)
5962-9059505GA (LT1019MH-10)
5962-9059506GA (LT1019MH-5)
5962-9059507GA (LT1019MH-4.5)
5962-9059508GA (LT1019MH-2.5)
5962-9062701GA (LT1011AMH)
5962-9062701PA (LT1011AMJ8)
5962-9062702GA (LT1011MH)
5962-9062702PA (LT1011MJ8)
5962-9064901CA (LTC1064-4MJ)
5962-9064901XA (LTC1064-4ML)
5962-9069301MCA (LTC1064-1MJ/883)
5962-9069302MCA (LTC1064-1AMJ/883)
5962-9073902MXA (LT1084-5MK)
5962-9073903MXA (LT1085-5MK)
5962-9073904MXA (LT1086-5MK)
5962-9081701MGA (LT1057AMH)
5962-9081701MPA (LT1057AMJ8)
5962-9081702MGA (LT1057MH)
5962-9081702MPA (LT1057MJ8)
5962-9082501MYA (LT1070MK)
5962-9082502MYA (LT1071MK)
5962-9082503MYA (LT1072MK)
5962-9082503MPA (LT1072MJ8)
5962-9082504MYA (LT1070HVMK)
5962-9082505MYA (LT1071HVMK)
5962-9082506MYA (LT1072HVMK)
5962-9084101MCA (LT1020MJ)
5962-9084201MGA (LT1012MH)
5962-9084201MPA (LT1012MJ8)
5962-9084202MGA (LT1012AMH)
5962-9084202MPA (LT1012AMJ8)
5962-9159501MPA (LTC1062MJ8)
5962-9161901MPA (LTC1042MK)
5962-9163201MCA (LT1079MJ)
5962-9163202MCA (LT1079AMJ)
5962-9163203MCA (LT1078MJ)
5962-9163204MCA (LT1078AMJ)
5962-9163204MGA (LT1078AMH)
5962-9163204MPA (LT1078AMJ8)
5962-9172901MVA (LT1180MJ)
5962-9172902MEA (LT1181MJ)
5962-9172903MVA (LT1280MJ)
5962-9172904MEA (LT1281MJ)
5962-9207901MPA (LT1172MJ8)
5962-9207901MPA (LT1172MJ8)
5962-9208001MPA (LTC485MJ8)
5962-9305701MPA (LTC1291CMJ)
5962-9305702MPA (LTC1292CMJ)
5962-9305703MEA (LTC1293CMJ)
5962-9305704MRA (LTC1294CMJ)
5962-9311901MYA (LT1076MK)
5962-9311902MYA (LT1076HVMK)
5962-9318401MPA (LT1229MJ8)
5962-9318402MCA (LT12320MJ)
5962-9319001MPA (LT1241MJ8)
5962-9319002MPA (LT1242MJ8)
5962-9319003MPA (LT1243MJ8)
5962-9319004MPA (LT1244MJ8)
5962-9319005MPA (LT1245MJ8)
5962-9321201MPA (LT1111MJ8)
5962-9322401MPA (LT1120MJ8)
5962-9323801MCA (LT1125MJ)
5962-9323802MPA (LT1124MJ)
5962-9323803MCA (LT1125AMJ)
5962-9323804MPA (LT1124AMJ)
5962-9451601MPA (LT118AJ8)

Radiation Hardened

RH07
RH27C
RH37C
RH101A
RH108A
RH111
RH117
RH118
RH119
RH129
RH137
RH1009
RH1011
RH1013
RH1014
RH1021-5
RH1021-7
RH1021-10
RH1056
RH1078

MILITARY PARTS LIST

883 Operational Amplifiers

LF155AH/883	LM101AJ8/883	LT1007AMH/883	LT1078AMH/883	LTC1050AMJ/883	OP-07AJ8/883	OP-37AJ8/883
LF155H/883	LM107H/883	LT1007AMJ8/883	LT1078AMJ8/883	LTC1050MH/883	OP-07H/883	OP-37BJ8/883
LF156AH/883	LM107J8/883	LT1007MH/883	LT1078MH/883	LTC1050MJ8/883	OP-07J8/883	OP-37CH/883
LF156H/883	LM108AH/883	LT1007MJ8/883	LT1078MJ8/883	LTC1050MJ/883	OP-15AH/883	OP-37CJ8/883
LF156J8/883	LM108H/883	LT1008MH/883	LT1079AMJ/883	LTC1051AMH/883	OP-15BH/883	OP-227AJ/883
LF156W/883	LM108AJ8/883	LT1012AMH/883	LT1079MJ/883	LTC1051AMJ8/883	OP-15CH/883	OP-227CJ/883
LF412AMH/883	LT118AH/883	LT1012MD/883	LT1124AMJ8\883	LTC1051MJ8/883	OP-15CJ8/883	OP-237AJ/883
LF412MH/883	LT118AJ8/883	LT1012MH/883	LT1124MJ8/883	LTC1052MH/883	OP-16AH/883	OP-237CJ/883
LF412AMJ8/883	LT1001AMH/883	LT1013AMH/883	LT1125AMJ8/883	LTC1052MJ/883	OP-16BH/883	
LF412MJ8/883	LT1001AMJ8/883	LT1013AMJ8/883	LT1125MJ8/883	LTC1052MJ8/883	OP-16CH/883	
LH0070-0H/883	LT1001MH/883	LT1013MH/883	LT1126AMJ8/883	LTC1150MJ8/883	OP-16CJ8/883	
LH0070-1H/883	LT1001MJ8/883	LT1013MJ8/883	LT1126MJ8/883	OP-05AH/883	OP-27AH/883	
LH0070-2H/883	LT1002AMJ/883	LT1014AMJ/883	LT1127AMJ8/883	OP-05AJ8/883	OP-27AJ8/883	
LH2108AD/883	LT1002MJ/883	LT1014MJ/883	LT1127MJ/883	OP-05H/883	OP-27BJ8/883	
LH2108D/883	LT1006AMH/883	LT1024AMD/883	LT1172MJ8/883	OP-05J8/883	OP-27BH/883	
LM10H/883	LT1006AMJ8/883	LT1024MD/883	LT1228MJ8/883	OP-05AW/883	OP-27CH/883	
LM10J8/883	LT1006MH/883	LT1055AMH/883	LTC1050AMH/883	OP-05W/883	OP-27CJ8/883	
LM101AH/883	LT1006MJ8/883	LT1055MH/883	LTC1050AMJ8/883	OP-07AH/883	OP-37AH/883	

883 High Speed Op Amps

LM118H/883	LT1028AMH/883	LT1037AMJ8/883	LT1057AMH/883	LT1058AML/883	LT1191MJ8/833	LT1223MJ8/883
LM118J8/883	LT1028AMJ8/883	LT1037MH/883	LT1057AMJ8/883	LT1058MJ/883	LT1192MJ8/883	LT1229MJ8/883
LM118W/883	LT1028MH/883	LT1037MJ8/883	LT1057MH/883	LT1187MJ8/883	LT1193MJ8/883	LT1230MJ/883
LT1022AMH/883	LT1028MJ8/883	LT1056AMH/883	LT1057MJ8/883	LT1189MJ8/883	LT1194MJ8/883	
LT1022MH/883	LT1037AMH/883	LT1056MH/883	LT1058AMJ/883	LT1190MJ8/883	LT1195MJ8/883	

883 Regulators

LM117H/883	LM137HVK/883	LT117AK/883	LT150AK/883	LT1035MK/883	LT1076HVMK/883	LT1086MH/883
LM117HVH/883	LM137K/883	LT123AK/883	LT1003MK/883	LT1036MK/883	LT1083MK-5/883	LT1086MK/883
LM117HVK/883	LM138K/883	LT137AH/883	LT1005MK/883	LT1054MJ8/883	LT1083MK-12/883	LT1086MK-5/883
LM117K/883	LM150K/883	LT137AHVH/883	LT1020MJ/883	LT1054MH/883	LT1084MK/883	LT1086MK-12/883
LM123K/883	LT117AH/883	LT137AHVK/883	LT1026MJ8/883	LT1074MK/883	LT1084MK-5/883	LT1120MJ8/883
LM137H/883	LT117AHVH/883	LT137AK/883	LT1026MH8/883	LT1074HVMK/883	LT1084MK-12/883	
LM137HVH/883	LT117AHVK/883	LT138AK/883	LT1033MK/883	LT1076MK/883	LT1085MK/883	

883 References

LM129AH/883	LM199AH/883	LT1004MH-2.5/883	LT1021BMH-5/883	LT1031BMH/883	REF-01J8/883
LM129BH/883	LM199AH-20/883	LT1009MH/883	LT1021CMH-5/883	LT1031CMH/883	REF-02AH/883
LM129CH/883	LM199H/883	LT1019AMH-2.5/883	LT1021DMH-5/883	LT1031DMH/883	REF-02AJ8/883
LM134H/883	LT580SH/883	LT1019AMH-4.5/883	LT1021BMH-7/883	LT1034BMH-1.2/883	REF-02H/883
LM134H-3/883	LT580TH/883	LT1019AMH-5/883	LT1021DMH-7/883	LT1034BMH-2.5/883	REF-02J8/883
LM134H-6/883	LT580UH/883	LT1019AMH-10/883	LT1021BMH-10/883	LT1034MH-1.2/883	
LM136AH-2.5/883	LT581SH/883	LT1019MH-2.5/883	LT1021CMH-10/883	LT1034MH-2.5/883	
LM136H-2.5/883	LT581TH/883	LT1019MH-4.5/883	LT1021DMH-10/883	REF-01AH/883	
LM185H-1.2/883	LT581UH/883	LT1019MH-5/883	LT1029AMH/883	REF-01AJ8/883	
LM185H-2.5/883	LT1004MH-1.2/883	LT1019MH-10/883	LT1029MH/883	REF-01H/883	

883 Comparators

LM111H/883	LM119W/883	LT119AJ/883	LT1011AMJ8/883	LT1016MJ/883	LT1017MJ8/883
LM111J8/883	LT111AH/883	LT685MH/883	LT1011MH/883	LT1016MJ8/883	LT1018MH/883
LM119H/883	LT111AJ8/883	LT685MJ/883	LT1011MJ8/883	LT1016ML/883	LT1018MJ8/883
LM119J/883	LT119AH/883	LT1011AMH/883	LT1016MH/883	LT1017MH/883	LTC1042MJ8/883

883 Switched-Mode Control Circuits

LT1070MK/883	LT1072MK/883	LT1242MJ8/883	LT1524J/883	LT1847J/883
LT1070HVMK/883	LT1072HVMK/883	LT1243MJ8/883	LT1525AJ/883	SG1524J/883
LT1071MK/883	LT1072MJ8/883	LT1244MJ8/883	LT1527AJ/883	SG1525AJ/883
LT1071HVMK/883	LT1241MJ8/883	LT1245MJ8/883	LT1846J/883	SG1527AJ/883

883 Interface

LT1032MJ/883	LT1080MJ/883	LT1180AMJ/883	LT1280MJ/883	LTC1045MJ/883
LT1039MJ/883	LT1081MJ/883	LT1181AMJ/883	LT1281MJ/883	
LT1039MJ16/883	LT1180MJ/883	LT1181MJ/883	LTC485MJ8/883	

883 Filters

LTC1059AMJ/883	LTC1061AMJ/883	LTC1064MJ/883	LTC1064-2ML/883	LTC1164AMJ/883	
LTC1059MJ/883	LTC1061MJ/883	LTC1064-1AMJ/883	LTC1064-4MJ/883	LTC1164-5MJ/883	
LTC1060AMJ/883	LTC1062MJ8/883	LTC1064-1MJ/883	LTC1064-4ML/883	LTC1164-7MJ/883	
LTC1060MJ/883	LTC1063MJ8/883	LTC1064-2MJ/883	LTC1164MJ/883		

883 Data Converters

LTC1094MJ/883	LTC1290DMJ/883	LTC1293DMJ/883	LTC1294DMJ/883
LTC1290BMJ/883	LTC1293BMJ/883	LTC1294BMJ/883	
LTC1290CMJ/883	LTC1293CMJ/883	LTC1294CMJ/883	

Other 883

LF198AH/883	LT1010MK/883	LTC1043MD/883
LF198H/883	LTC201AMJ/883	LTC1044MH/883
LT1010MH/883	LTC1041MJ8/883	LTC1044MJ8/883

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SECTION 13—NEW PRODUCTS

SECTION 13—NEW PRODUCTS

Half-/Full-Bridge N-Channel Power MOSFET Drivers

July 1995

FEATURES

- **Floating Top Driver Switches Up to 60V**
- Drives Gate of Top N-Channel MOSFET above Load HV Supply
- **180ns Transition Times Driving 10,000pF**
- **Adaptive Nonoverlapping Gate Drives Prevent Shoot-Through**
- Top Drive Protection at High Duty Cycles
- TTL/CMOS Input Levels
- Undervoltage Lockout with Hysteresis
- Operates at Supply Voltages from 10V to 15V
- Separate Top and Bottom Drive Pins

APPLICATIONS

- PWM of High Current Inductive Loads
- Half-Bridge and Full-Bridge Motor Control
- Synchronous Step-Down Switching Regulators
- 3-Phase Brushless Motor Drive
- High Current Transducer Drivers
- Class D Power Amplifiers

DESCRIPTION

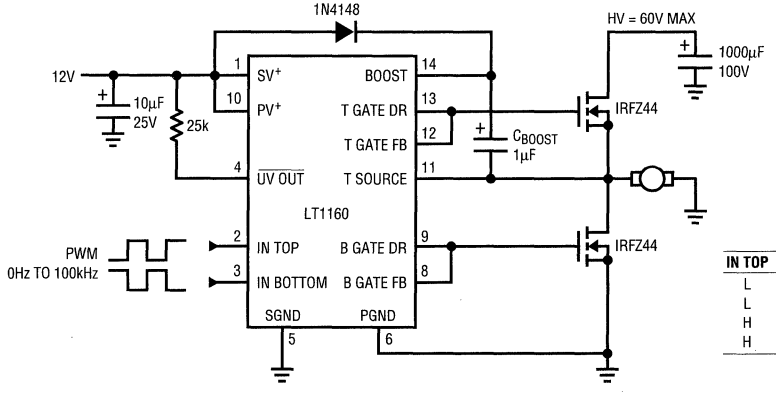
The LT®1160/LT1162 are cost effective half-/full-bridge N-channel power MOSFET drivers. The floating driver can drive the top side N-channel power MOSFETs operating off a high voltage (HV) rail of up to 60V (absolute maximum).

The internal logic prevents the inputs from turning the power MOSFETs in a half-bridge on at the same time. Its unique adaptive protection against shoot-through currents eliminates all matching requirements for the two MOSFETs. This greatly eases the design of high efficiency motor control and switching regulator systems.

During low supply or start-up conditions, the undervoltage lockout actively pulls the driver outputs low to prevent the power MOSFETs from being partially turned on. The 0.5V hysteresis allows reliable operation even with slowly varying supplies.

The LT1162 is a dual version of the LT1160 and is available in a 24-pin PDIP or in a 24-pin SO Wide package.

TYPICAL APPLICATION



IN TOP	IN BOTTOM	T GATE DR	B GATE DR
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

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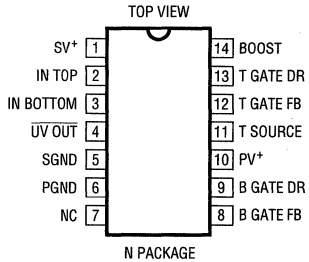
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1) 20V
Boost Voltage 75V
Peak Output Currents (< 10μs) 1.5A
Input Pin Voltages ..... −0.3V to V+ + 0.3V
Top Source Voltage ..... −5V to 60V
Boost to Source Voltage ..... −0.3V to 20V

Operating Temperature Range
Commercial ..... 0°C to 70°C
Industrial ..... −40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



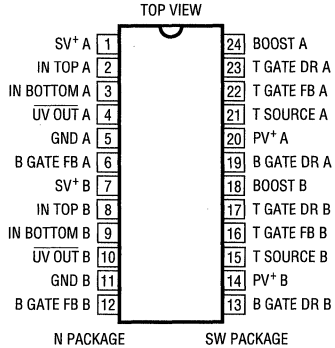
N PACKAGE
14-LEAD PDIP

S PACKAGE
14-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 110°C/W (S)

ORDER PART NUMBER

LT1160CN
LT1160CS
LT1160IN
LT1160IS



N PACKAGE
24-LEAD PDIP

SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 125°C, θ_{JA} = 58°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 80°C/W (SW)

ORDER PART NUMBER

LT1162CN
LT1162CSW
LT1162IN
LT1162ISW

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

Test Circuit, T_A = 25°C, $V^+ = V_{BOOST}$ = 12V, $V_{TSOURCE}$ = 0V, C_{GATE} = 3000pF. Gate Feedback pins connected to Gate Drive pins, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	DC Supply Current (Note 3)	V^+ = 15V, V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 2V V^+ = 15V, V_{INTOP} = 2V, $V_{INBOTTOM}$ = 0.8V V^+ = 15V, V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 0.8V		7 7 7	11 10 11	15 15 15	mA mA mA
I_{BOOST}	Boost Current (Note 3)	V^+ = 15V, $V_{TSOURCE}$ = 60V, V_{BOOST} = 75V, V_{INTOP} = $V_{INBOTTOM}$ = 0.8V		3	4.5	6	mA
V_{IL}	Input Logic Low		●		1.4	0.8	V
V_{IH}	Input Logic High		●	2	1.7		V
I_{IN}	Input Current	V_{INTOP} = $V_{INBOTTOM}$ = 4V	●		7	25	μA
V^+_{UVH}	V^+ Undervoltage Start-Up Threshold			8.3	8.8	9.3	V
V^+_{UVL}	V^+ Undervoltage Shutdown Threshold			7.8	8.3	8.8	V
V_{BUVH}	V_{BOOST} Undervoltage Start-Up Threshold	$V_{TSOURCE}$ = 60V (V_{BOOST} − $V_{TSOURCE}$)		8.8	9.3	9.8	V
V_{BUVL}	V_{BOOST} Undervoltage Shutdown Threshold	$V_{TSOURCE}$ = 60V (V_{BOOST} − $V_{TSOURCE}$)		8.2	8.7	9.2	V

LECTRICAL CHARACTERISTICS

Test Circuit, T_A = 25°C, $V^+ = V_{BOOST}$ = 12V, $V_{TSOURCE}$ = 0V, C_{GATE} = 3000pF. te Feedback pins connected to Gate Drive pins, unless otherwise specified.

MBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AK	Undervoltage Output Leakage	V^+ = 15V	●		0.1	5	µA
AT	Undervoltage Output Saturation	V^+ = 7.5V, I_4 = 2.5mA	●		0.2	0.4	V
H	Top Gate ON Voltage	V_{INTOP} = 2V, $V_{INBOTTOM}$ = 0.8V	●	11	11.3	12	V
	Bottom Gate ON Voltage	V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 2V	●	11	11.3	12	V
-	Top Gate OFF Voltage	V_{INTOP} = 0.8V, $V_{INBOTTOM}$ = 2V	●		0.4	0.7	V
	Bottom Gate OFF Voltage	V_{INTOP} = 2V, $V_{INBOTTOM}$ = 0.8V	●		0.4	0.7	V
	Top Gate Rise Time	V_{INTOP} (+) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR}$ (Note 4)	●		130	200	ns
	Bottom Gate Rise Time	$V_{INBOTTOM}$ (+) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 4)	●		90	200	ns
	Top Gate Fall Time	V_{INTOP} (–) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR}$ (Note 4)	●		60	140	ns
	Bottom Gate Fall Time	$V_{INBOTTOM}$ (–) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 4)	●		60	140	ns
	Top Gate Turn On Delay	V_{INTOP} (+) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR}$ (Note 4)	●		250	500	ns
	Bottom Gate Turn On Delay	$V_{INBOTTOM}$ (+) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 4)	●		200	400	ns
	Top Gate Turn Off Delay	V_{INTOP} (–) Transition, $V_{INBOTTOM}$ = 0.8V, Measured at $V_{TGATE\ DR}$ (Note 4)	●		300	600	ns
	Bottom Gate Turn Off Delay	$V_{INBOTTOM}$ (–) Transition, V_{INTOP} = 0.8V, Measured at $V_{BGATE\ DR}$ (Note 4)	●		200	400	ns
	Top Gate Lockout Delay	$V_{INBOTTOM}$ (+) Transition, V_{INTOP} = 2V, Measured at $V_{TGATE\ DR}$ (Note 4)	●		300	600	ns
	Bottom Gate Lockout Delay	V_{INTOP} (+) Transition, $V_{INBOTTOM}$ = 2V, Measured at $V_{BGATE\ DR}$ (Note 4)	●		250	500	ns
	Top Gate Release Delay	$V_{INBOTTOM}$ (–) Transition, V_{INTOP} = 2V, Measured at $V_{TGATE\ DR}$ (Note 4)	●		250	500	ns
	Bottom Gate Release Delay	V_{INTOP} (–) Transition, $V_{INBOTTOM}$ = 2V, Measured at $V_{BGATE\ DR}$ (Note 4)	●		200	400	ns

● denotes specifications which apply over the full operating
perature range.

e 1: For the LT1160, Pins 1, 10 should be connected together. For the
162, Pins 1, 7, 14, 20 should be connected together.

e 2: T_J is calculated from the ambient temperature T_A and power
sipation P_D according to the following formulas:

LT1160CN/LT1160IN: $T_J = T_A + (P_D \times 70°C/W)$
LT1160CS/LT1160IS: $T_J = T_A + (P_D \times 110°C/W)$
LT1162CN/LT1162IN: $T_J = T_A + (P_D \times 58°C/W)$
LT1162CS/LT1162IS: $T_J = T_A + (P_D \times 80°C/W)$

Note 3: I_S is the sum of currents through SV^+, PV^+ and Boost pins. I_{BOOST} is the current through the Boost pin. Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Typical Performance Characteristics and Applications Information sections. The LT1160 = 1/2 LT1162.

Note 4: Gate rise times are measured from 2V to 10V and fall times are measured from 10V to 2V. Delay times are measured from the input transition to when the gate voltage has risen to 2V or decreased to 10V.

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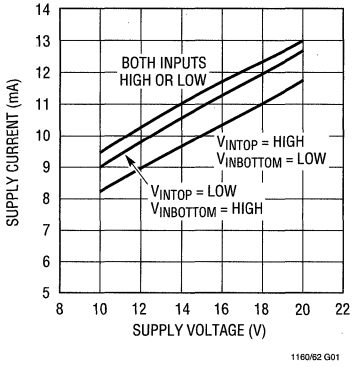
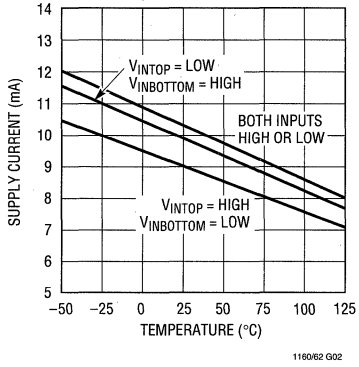
TYPICAL PERFORMANCE CHARACTERISTICS (LT1160 or 1/2 LT1162)

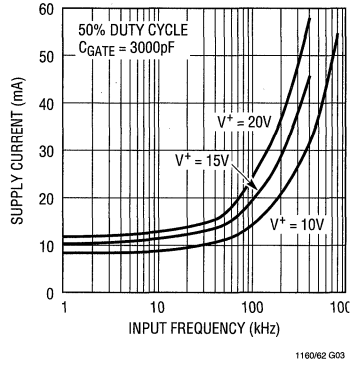
DC Supply Current vs Supply Voltage



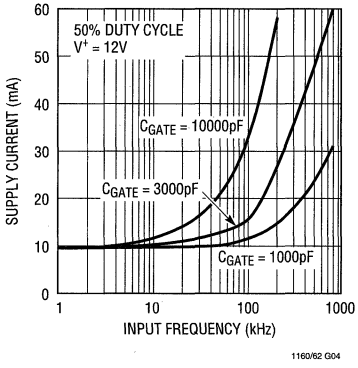
DC Supply Current vs Temperature



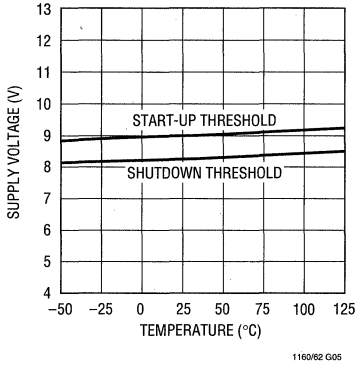
DC + Dynamic Supply Current vs Input Frequency



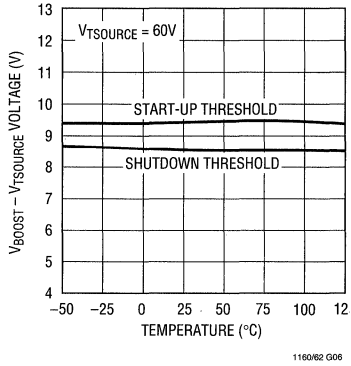
DC + Dynamic Supply Current vs Input Frequency



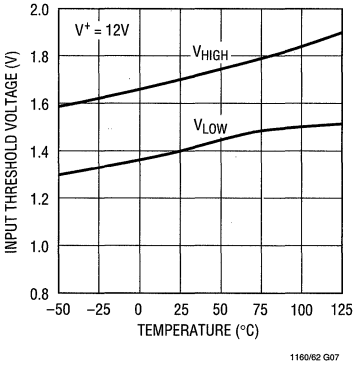
Undervoltage Lockout (V+)



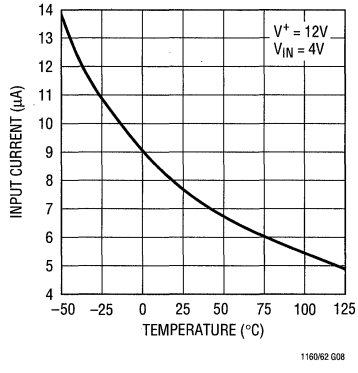
Undervoltage Lockout (V_{BOOST})



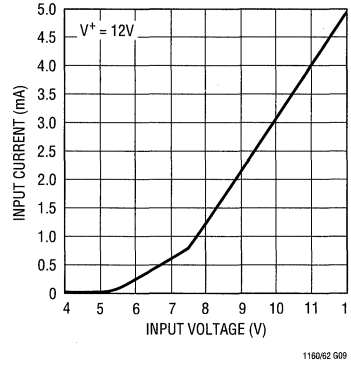
Input Threshold Voltage vs Temperature



Top or Bottom Input Pin Current vs Temperature

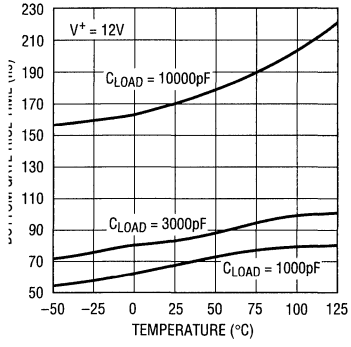


Top or Bottom Input Pin Current vs Input Voltage

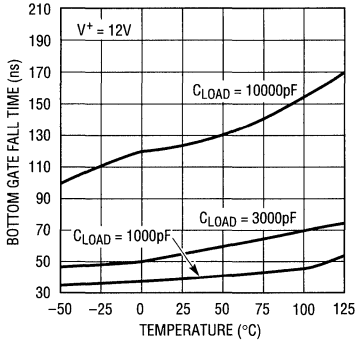


TYPICAL PERFORMANCE CHARACTERISTICS (LT1160 or 1/2 LT1162)

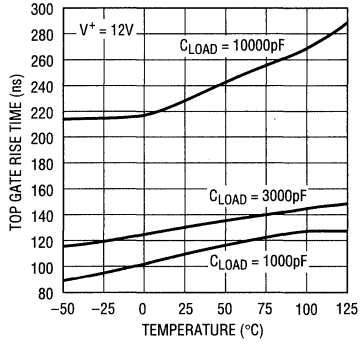
Bottom Gate Rise Time vs Temperature



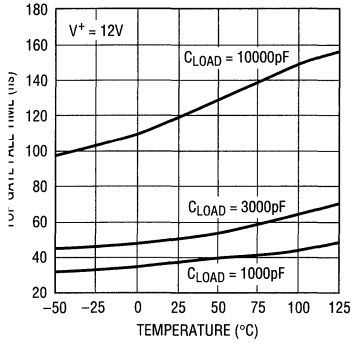
Bottom Gate Fall Time vs Temperature



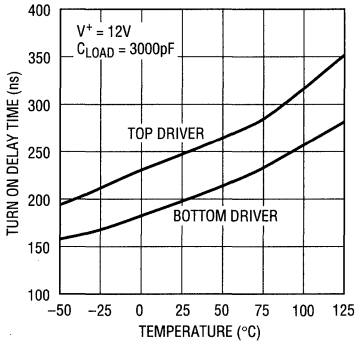
Top Gate Rise Time vs Temperature



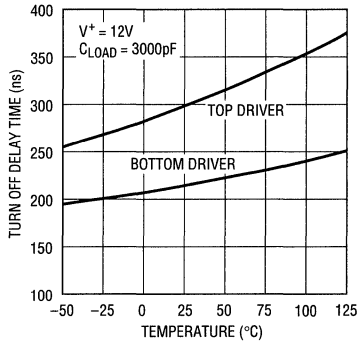
Top Gate Fall Time vs Temperature



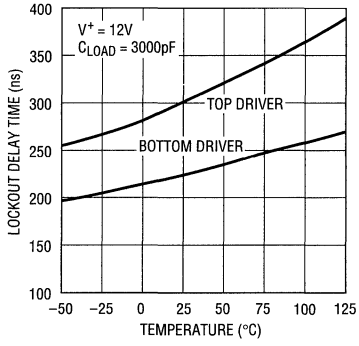
Turn On Delay Time vs Temperature



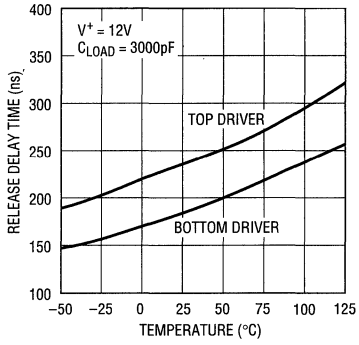
Turn Off Delay Time vs Temperature



Lockout Delay Time vs Temperature



Release Delay Time vs Temperature



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PIN FUNCTIONS

LT1160

SV+ (Pin 1): Main Signal Supply. Must be closely decoupled to the signal ground Pin 5.

IN TOP (Pin 2): Top Driver Input. Pin 2 is disabled when Pin 3 is high. A 3k input resistor followed by a 5V internal clamp prevents saturation of the input transistors.

IN BOTTOM (Pin 3): Bottom Driver Input. Pin 3 is disabled when Pin 2 is high. A 3k input resistor followed by a 5V internal clamp prevents saturation of the input transistors.

$\overline{\text{UV OUT}}$ (Pin 4): Undervoltage Output. Open collector NPN output which turns on when V^+ drops below the undervoltage threshold.

SGND (Pin 5): Small Signal Ground. Must be routed separately from other grounds to the system ground.

PGND (Pin 6): Bottom Driver Power Ground. Connects to source of bottom N-channel MOSFET.

B GATE FB (Pin 8): Bottom Gate Feedback. Must connect directly to the bottom power MOSFET gate. The top MOSFET turn-on is inhibited until Pin 8 has discharged to below 2.5V.

B GATE DR (Pin 9): Bottom Gate Drive. The high current drive point for the bottom MOSFET. When a gate resistor is used it is inserted between Pin 9 and the gate of the MOSFET.

PV+ (Pin 10): Bottom Driver Supply. Must be connected to the same supply as Pin 1.

T SOURCE (Pin 11): Top Driver Return. Connects to the top MOSFET source and the low side of the bootstrap capacitor.

T GATE FB (Pin 12): Top Gate Feedback. Must connect directly to the top power MOSFET gate. The bottom MOSFET turn-on is inhibited until $V_{12}-V_{11}$ has discharged to below 2.9V.

T GATE DR (Pin 13): Top Gate Drive. The high current drive point for the top MOSFET. When a gate resistor is used it is inserted between Pin 13 and the gate of the MOSFET.

BOOST (Pin 14): Top Driver Supply. Connects to the high side of the bootstrap capacitor.

LT1162

SV+ (Pins 1, 7): Main Signal Supply. Must be closely decoupled to ground Pins 5 and 11.

IN TOP (Pins 2, 8): Top Driver Input. The Input Top is disabled when the Input Bottom is high. A 3k input resistor followed by a 5V internal clamp prevents saturation of the input transistors.

IN BOTTOM (Pins 3, 9): Bottom Driver Input. The Input Bottom is disabled when the Input Top is high. A 3k input resistor followed by a 5V internal clamp prevents saturation of the input transistors.

$\overline{\text{UV OUT}}$ (Pins 4, 10): Undervoltage Output. Open collector NPN output which turns on when V^+ drops below the undervoltage threshold.

GND (Pins 5, 11): Ground Connection.

B GATE FB (Pins 6, 12): Bottom Gate Feedback. Must connect directly to the bottom power MOSFET gate. The top MOSFET turn-on is inhibited until Bottom Gate Feedback pins have discharged to below 2.5V.

B GATE DR (Pins 13, 19): Bottom Gate Drive. The high current drive point for the bottom MOSFET. When a gate resistor is used it is inserted between Bottom Gate Drive pin and the gate of the MOSFET.

PV+ (Pins 14, 20): Bottom Driver Supply. Must be connected to the same supply as Pins 1 and 7.

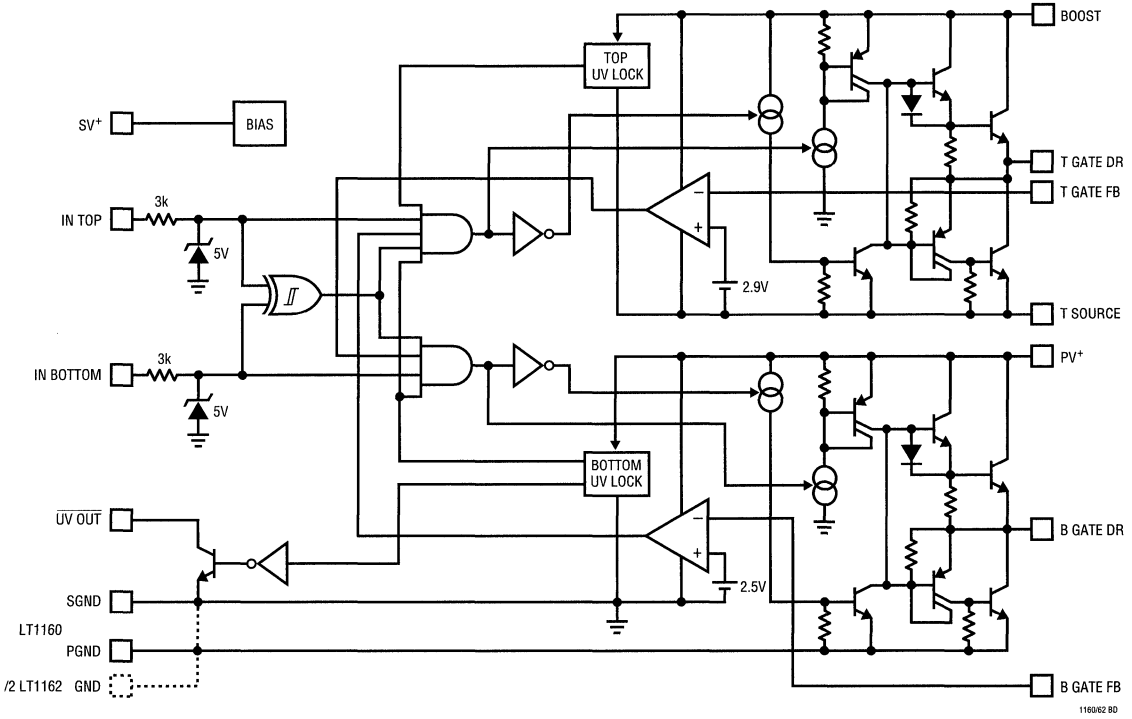
T SOURCE (Pins 15, 21): Top Driver Return. Connects to the top MOSFET source and the low side of the bootstrap capacitor.

T GATE FB (Pins 16, 22): Top Gate Feedback. Must connect directly to the top power MOSFET gate. The bottom MOSFET turn-on is inhibited until $V_{TGF}-V_{TSOURCE}$ has discharged to below 2.9V.

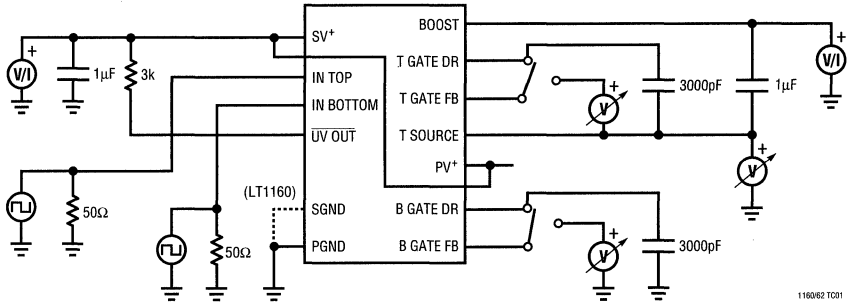
T GATE DR (Pins 17, 23): Top Gate Drive. The high current drive point for the top MOSFET. When a gate resistor is used it is inserted between the Top Gate Drive pin and the gate of the MOSFET.

BOOST (Pins 18, 24): Top Driver Supply. Connects to the high side of the bootstrap capacitor.

FUNCTIONAL DIAGRAM (LT1160 or 1/2 LT1162)



TEST CIRCUIT (LT1160 or 1/2 LT1162)



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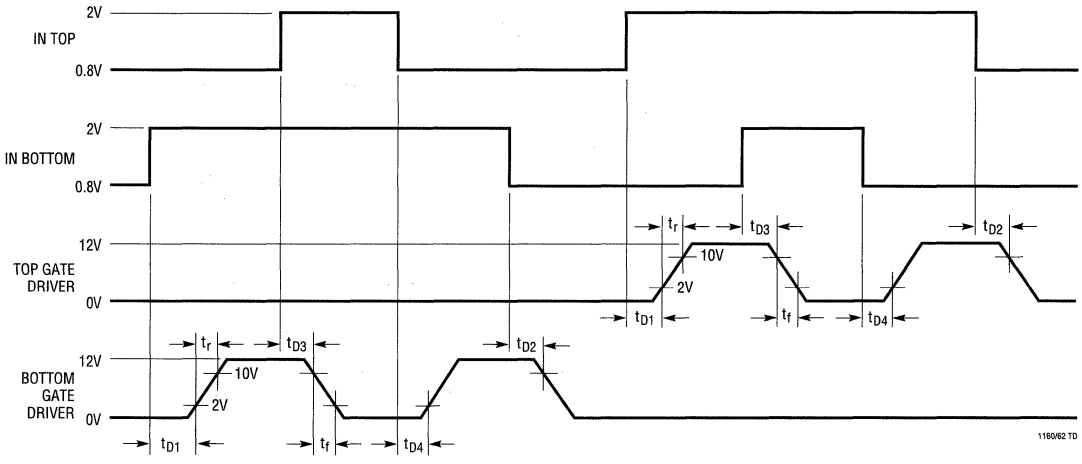
TIMING DIAGRAM



OPERATION (Refer to Functional Diagram)

The LT1160 (or 1/2 LT1162) incorporates two independent driver channels with separate inputs and outputs. The inputs are TTL/CMOS compatible; they can withstand input voltages as high as V^+. The 1.4V input threshold is regulated and has 300mV of hysteresis. Both channels are noninverting drivers. The internal logic prevents both outputs from simultaneously turning on under any input conditions. When both inputs are high both outputs are actively held low.

The floating supply for the top driver is provided by a bootstrap capacitor between the Boost pin and the Top Source pin. This capacitor is recharged each time the negative plate goes low in PWM operation.

The undervoltage detection circuit disables both channels when V^+ is below the undervoltage trip point. A separate UV detect block disables the high side channel when $V_{BOOST} - V_{TSOURCE}$ is below its own undervoltage trip point.

The top and bottom gate drivers in the LT1160 each utilize two gate connections: 1) a gate drive pin, which provides the turn on and turn off currents through an optional series gate resistor, and 2) a gate feedback pin which connects directly to the gate to monitor the gate-to-source voltage.

Whenever there is an input transition to command the outputs to change states, the LT1160 follows a logical sequence to turn off one MOSFET and turn on the other. First, turn off is initiated, then V_{GS} is monitored until it has decreased below the turn off threshold, and finally the other gate is turned on.

IPPLICATIONS INFORMATION

ɔwer MOSFET Selection

nce the LT1160 (or 1/2 LT1162) inherently protects the p and bottom MOSFETs from simultaneous conduction, ere are no size or matching constraints. Therefore selec-ɔn can be made based on the operating voltage and ɔS(ON) requirements. The MOSFET BV_{DSS} should be eater than the HV and should be increased to 2 × HV in ırsh environments with frequent fault conditions. For the ⁻1160 maximum operating HV supply of 60V, the MOSFET /DSS should be from 60V to 120V.

ıe MOSFET $R_{DS(ON)}$ is specified at T_J = 25°C and is ɜnerally chosen based on the operating efficiency re-ıired as long as the maximum MOSFET junction tem-ɜrature is not exceeded. The dissipation while each OSFET is on is given by:

$$P = D(I_{DS})^2(1+\partial)R_{DS(ON)}$$

here D is the duty cycle and ∂ is the increase in $R_{DS(ON)}$ the anticipated MOSFET junction temperature. From this ıuation the required $R_{DS(ON)}$ can be derived:

$$R_{DS(ON)} = \frac{P}{D(I_{DS})^2(1+\partial)}$$

ɪr example, if the MOSFET loss is to be limited to 2W ıen operating at 5A and a 90% duty cycle, the required ɔS(ON) would be 0.089Ω/(1 + ∂). (1 + ∂) is given for each OSFET in the form of a normalized $R_{DS(ON)}$ vs tempera-re curve, but ∂ = 0.007/°C can be used as an approxima-ɪn for low voltage MOSFETs. Thus, if T_A = 85°C and the ailable heat sinking has a thermal resistance of 20°C/W, ɜ MOSFET junction temperature will be 125°C and = 0.007(125 – 25) = 0.7. This means that the required ɔS(ON) of the MOSFET will be 0.089Ω/1.7 = 0.0523Ω, ıich can be satisfied by an International Rectifier IRFZ34.

ansition losses result from the power dissipated in each ɔSFET during the time it is transitioning from off to on, from on to off. These losses are proportional to f × $(HV)^2$ d vary from insignificant to being a limiting factor on erating frequency in some high voltage applications.

Paralleling MOSFETs

When the above calculations result in a lower $R_{DS(ON)}$ than is economically feasible with a single MOSFET, two or more MOSFETs can be paralleled. The MOSFETs will inherently share the currents according to their $R_{DS(ON)}$ ratio as long as they are thermally connected (e.g., on a common heat sink). The LT1160 top and bottom drivers can each drive five power MOSFETs in parallel with only a small loss in switching speeds (see Typical Performance Characteristics). A low value resistor (10Ω to 47Ω) in series with each individual MOSFET gate may be required to "decouple" each MOSFET from its neighbors to prevent high frequency oscillations (consult manufacturer's recommendations). If gate decoupling resistors are used the corresponding gate feedback pin can be connected to any one of the gates as shown in Figure 1.

Driving multiple MOSFETs in parallel may restrict the operating frequency to prevent overdissipation in the LT1160 (see the following Gate Charge and Driver Dissipation).

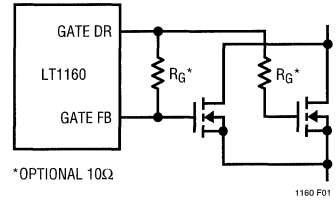


Figure 1. Paralleling MOSFETs

Gate Charge and Driver Dissipation

A useful indicator of the load presented to the driver by a power MOSFET is the total gate charge Q_G, which includes the additional charge required by the gate-to-drain swing. Q_G is usually specified for V_{GS} = 10V and $V_{DS} = 0.8V_{DS(MAX)}$. When the supply current is measured in a switching application, it will be larger than given by the DC electrical characteristics because of the additional supply current associated with sourcing the MOSFET gate charge:

$$I_{SUPPLY} = I_{DC} + \left(\frac{dQ_G}{dt}\right)_{TOP} + \left(\frac{dQ_G}{dt}\right)_{BOTTOM}$$

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APPLICATIONS INFORMATION

The actual increase in supply current is slightly higher due to LT1160 switching losses and the fact that the gates are being charged to more than 10V. Supply Current vs Input Frequency is given in the Typical Performance Characteristics.

The LT1160 junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LT1160IS is limited to less than 31mA from a 12V supply:

$T_J = 85°C + (31mA \times 12V \times 110°C/W)$

$= 126°C$ exceeds absolute maximum

In order to prevent the maximum junction temperature from being exceeded, the LT1160 supply current must be verified while driving the full complement of the chosen MOSFET type at the maximum switching frequency.

Ugly Transient Issues

In PWM applications the drain current of the top MOSFET is a square wave at the input frequency and duty cycle. To prevent large voltage transients at the top drain, a low ESR electrolytic capacitor must be used and returned to the power ground. The capacitor is generally in the range of 25µF to 5000µF and must be physically sized for the RMS current flowing in the drain to prevent heating and premature failure. In addition, the LT1160 requires a separate 10µF capacitor connected closely between Pins 1 and 5 (the LT1162 requires two 10µF capacitors connected between Pins 1 and 5, and Pins 7 and 11).

The LT1160 top source is internally protected against transients below ground and above supply. However, the gate drive pins cannot be forced below ground. In most applications, negative transients coupled from the source to the gate of the top MOSFET do not cause any problems.

Switching Regulator Applications

The LT1160 (or 1/2 LT1162) is ideal as a synchronous switch driver to improve the efficiency of step-down (buck) switching regulators. Most step-down regulators use a high current Schottky diode to conduct the inductor current when the switch is off. The fractions of the oscillator period that the switch is on (switch conducting) an off (diode conducting) are given by:

$$\text{Switch ON} = \left(\frac{V_{OUT}}{HV}\right) \times \text{Total Period}$$

$$\text{Switch OFF} = \left(\frac{HV - V_{OUT}}{HV}\right) \times \text{Total Period}$$

Note that for $HV > 2V_{OUT}$ the switch is off longer than it i on, making the diode losses more significant than th switch. The worst case for the diode is during a sho circuit, when V_{OUT} approaches zero and the diode con ducts the short-circuit current almost continuously.

Figure 2 shows the LT1160 used to synchronously drive pair of power MOSFETs in a step-down regulator applica tion, where the top MOSFET is the switch and the botto MOSFET replaces the Schottky diode. Since both conduc tion paths have low losses, this approach can result in ver high efficiency (90% to 95%) in most applications. Fo regulators under 10A, using low $R_{DS(ON)}$ N-channe MOSFETs eliminates the need for heat sinks. R_{GS} holds th top MOSFET off when HV is applied before the 12V supply

One fundamental difference in the operation of a step down regulator with synchronous switching is that it neve becomes discontinuous at light loads. The inductor cur rent doesn't stop ramping down when it reaches zero bu actually reverses polarity resulting in a constant rippl current independent of load. This does not cause a signifi cant efficiency loss (as might be expected) since th negative inductor current is returned to HV when th switch turns back on. However, I^2R losses will occu under these conditions due to the recirculating currents

The LT1160 performs the synchronous MOSFET drive in step-down switching regulator. A reference and PWM ar required to complete the regulator. Any voltage mode o current mode PWM controller may be used but the LT352 is particularly well-suited to high power, high efficienc applications such as the 10A circuit shown in Figure 4. I higher current regulators a small Schottky diode across th bottom MOSFET helps to reduce reverse-recovery switchin losses.

APPLICATIONS INFORMATION

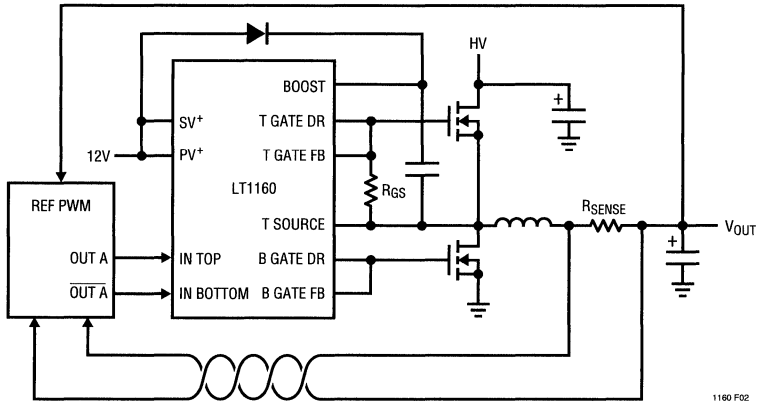


Figure 2. Adding Synchronous Switching to a Step-Down Switching Regulator

Motor Drive Applications

In applications where rotation is always in the same direction, a single LT1160 controlling a half-bridge can be used to drive a DC motor. One end of the motor may be connected either to supply or to ground as seen on Figure 3. A motor in this configuration is controlled by its inputs which give three alternatives: run, free running stop (coasting) and fast stop ("plugging" braking, with the motor shorted by one of the MOSFETs).

To drive a DC motor in both directions the LT1162 can be used to drive an H-bridge output stage. In this configuration the motor can be made to run clockwise, counterclockwise, stop rapidly ("plugging" braking) or free run (coast) to a stop. A very rapid stop may be achieved by reversing the current, though this requires more careful design to stop the motor dead. In practice a closed-loop control system with tachometric feedback is usually necessary.

The motor speed in these examples can be controlled by switching the drivers with pulse width modulated square waves. This approach is particularly suitable for microcomputers/DSP control loops.

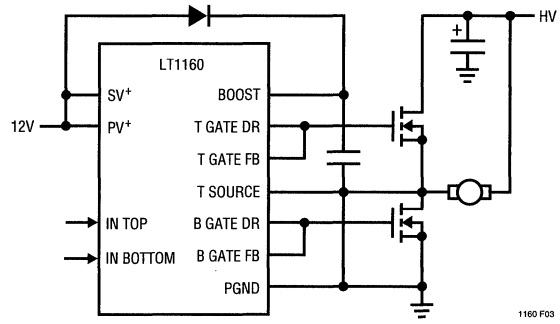


Figure 3. Driving a Supply Referenced Motor

13

TYPICAL APPLICATIONS

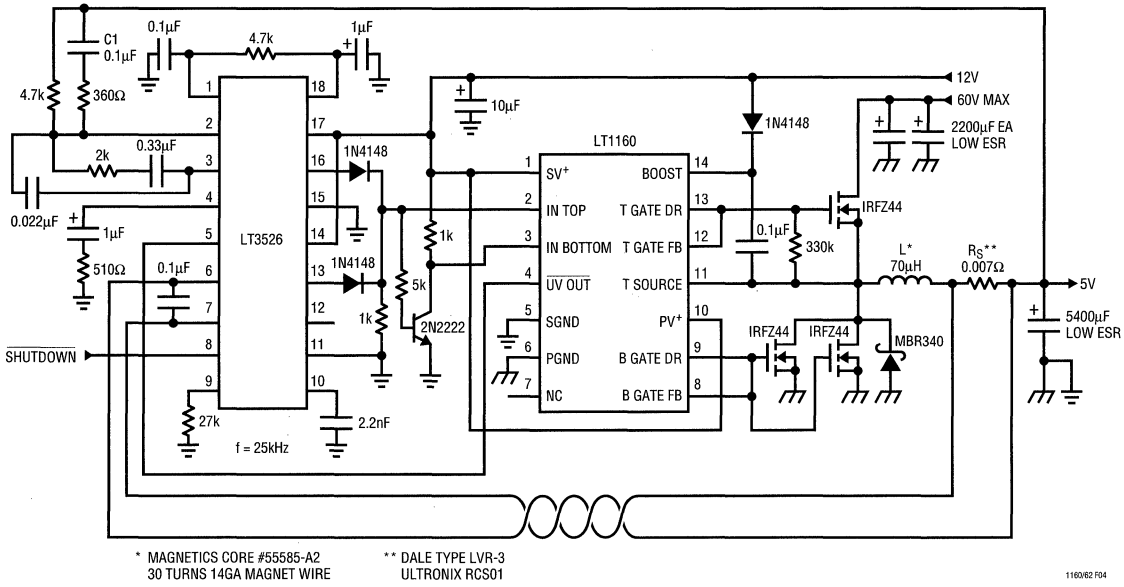


Figure 4. 90% Efficiency, 40V to 5V 10A Low Dropout Voltage Mode Switching Regulator

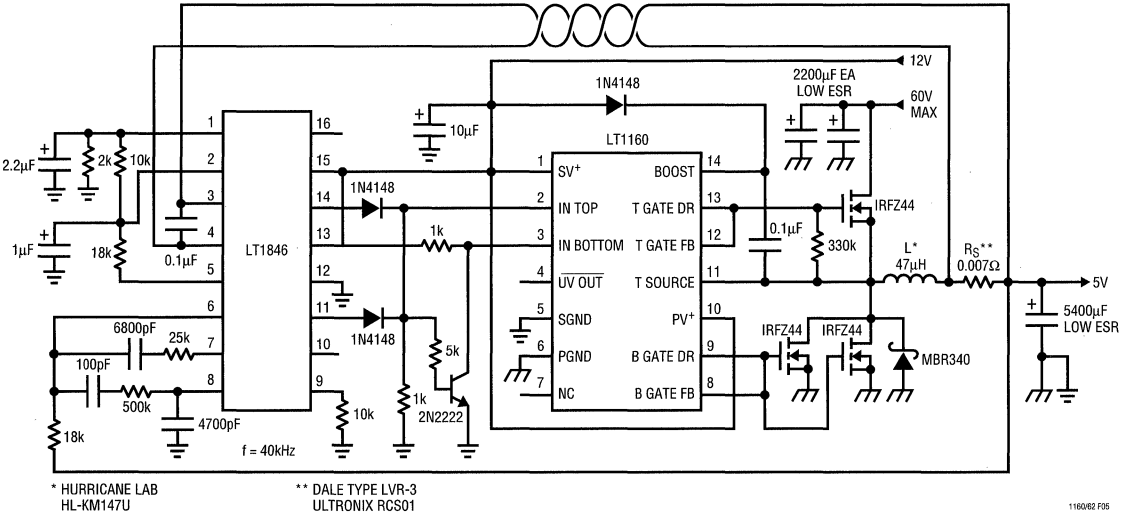


Figure 5. 90% Efficiency, 40V to 5V 10A Low Dropout Current Mode Switching Regulator

TYPICAL APPLICATIONS

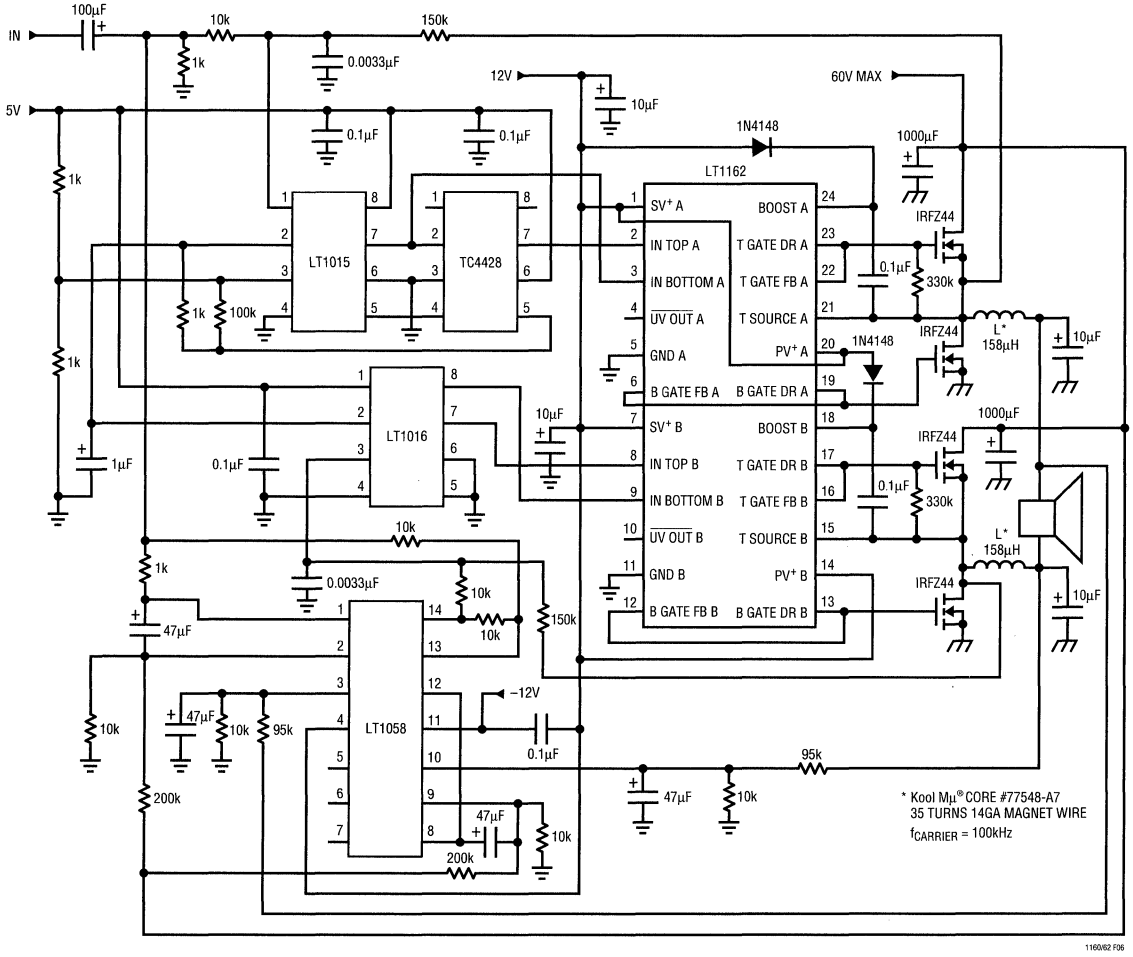


Figure 6. 200W Class D, 10Hz to 1kHz Amplifier

Kool Mµ is a registered trademark of Magnetics, Inc.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1158	Half-Bridge N-Channel Power MOSFET Driver	Single Input, Continuous Current Protection and Internal Charge Pump for DC Operation

LTC1177-5/LTC1177-12

Isolated MOSFET Drivers

May 1995

FEATURES

- **UL Recognized ® File E151738 to UL1577**
- **No Secondary Power Supply**
- **Drives Any Logic Level FET**
- Low Input Current: 1mA Typ (LTC1177-5), 2.5mA Typ (LTC1177-12)
- Turns On in 1ms Typ and Turns Off in 1ms Typ
- $2500V_{RMS}$ of Isolation Voltage
- Isolates Input from High Voltage Transients at Load
- Clean, Bounce-Free Switching
- Current Limit
- Small Outline Package

APPLICATIONS

- Solid State Relay
- Isolated Solenoid Driver
- Isolated Motor Driver
- Isolated Lamp Driver

DESCRIPTION

The LTC®1177-5/LTC1177-12 are isolated high-side MOSFET drivers. When used with an external N-channel MOSFET, the LTC1177-5/LTC1177-12 form an isolated solid state switch for reliable bounce-free switching operation. The output does not require an auxiliary power supply to maintain an on-state condition.

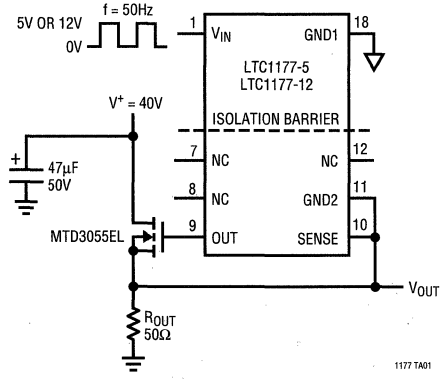
Two lead frame capacitors are used to transfer energy from the input to drive the gate of the MOSFET and provide the necessary isolation. Unlike opto-isolated FET drivers, the input current for the LTC1177-5 is only 1mA and 2.5mA for LTC1177-12. It also does not have the aging problems endemic to opto-couplers.

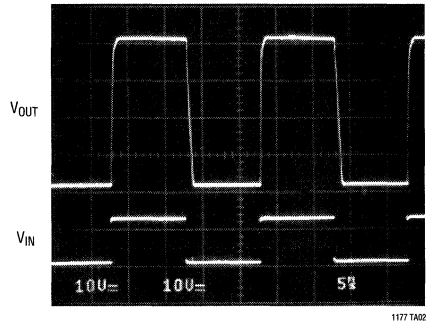
Both devices provide $2500V_{RMS}$ (1 minute) or $3000V_{RMS}$ (1 second) of output-to-input isolation.

The LTC1177-5/LTC1177-12 are available in the 18-pin PDIP or 28-pin SO Wide package.

TYPICAL APPLICATION

Isolated High-Side Switch





ABSOLUTE MAXIMUM RATINGS

Input Voltages
- V_{IN} (LTC1177-5) ..... 6V to (GND1 – 0.3V)
- V_{IN} (LTC1177-12) ..... 13.2V to (GND1 – 0.3V)
- Sense (LTC1177-5) ..... 6V to (GND2 – 0.3V)
- Sense (LTC1177-12) ..... 12V to (GND2 – 0.3V)

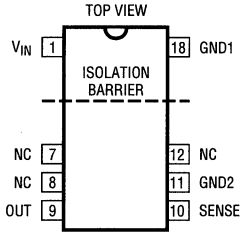
Output Voltages ..... 12V to (GND2 – 0.3V)

Operating Temperature Range
- Commercial ..... 0°C to 70°C
- Industrial ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

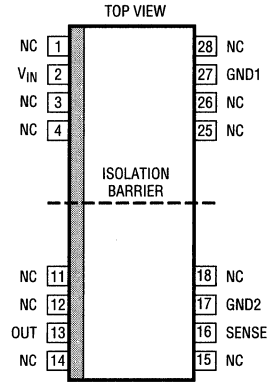


N PACKAGE
18-LEAD PDIP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC1177CN-5
LTC1177CN-12
LTC1177IN-5
LTC1177IN-12



SW PACKAGE
28-LEAD PLASTIC SO WIDE

T_{JMAX} = 125°C, θ_{JA} = 125°C/W

ORDER PART NUMBER

LTC1177CSW-5
LTC1177CSW-12
LTC1177ISW-5
LTC1177ISW-12

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1177-5 MIN	LTC1177-5 TYP	LTC1177-5 MAX	UNITS
V_{OUT}	Output Voltage (Refer to GND2)	C_{OUT} = 1000pF, No Load (N Pkg)	●	6.5	7.5	10	V
		C_{OUT} = 1000pF, No Load, V_{IN} = 4.75V (N Pkg)	●	5.5	6.5	10	V
		C_{OUT} = 1000pF, No Load (SW Pkg)	●	7.0	8.0	10	V
		C_{OUT} = 1000pF, No Load, V_{IN} = 4.75V (SW Pkg)	●	6.0	7.0	10	V
I_{IN}	Input Current	C_{IN} = 1000pF	●		1.0	1.5	mA
I_{LIM}	Current Limit	R_{SENSE} = 1Ω (LTC1177C-5)	●	400	620	800	mA
		R_{SENSE} = 1Ω (LTC1177I-5)	●	350	620	900	mA
t_{ON}	Turn On Time	C_{OUT} = 1000pF, No Load (LTC1177C-5)	●		1.0	4.0	ms
		C_{OUT} = 1000pF, No Load (LTC1177I-5)	●		1.0	4.5	ms
t_{OFF}	Turn Off Time	C_{OUT} = 1000pF, No Load	●		1.0	1.8	ms
V_{ISO}	Isolation Voltage	1 Minute (Note 1)		2500			V_{RMS}
		1 Second		3000			V_{RMS}
CM	Common-Mode Slew Rate	V_{OUT} < 1.5, C_{OUT}= 1000pF				1000	V/µs

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C unless otherwise noted.

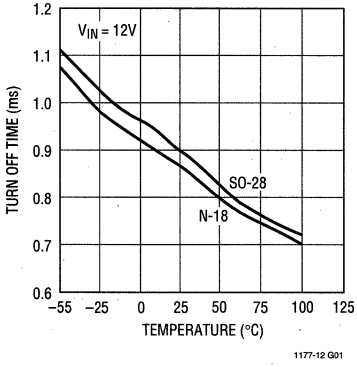
SYMBOL	PARAMETER	CONDITIONS		LTC1177-12 MIN	LTC1177-12 TYP	LTC1177-12 MAX	UNITS
V_{OUT}	Output Voltage (Refer to GND2)	C_{OUT} = 1000pF, No Load (LTC1177C-12, N Pkg)	●	4.65	5.2	8	V
		C_{OUT} = 1000pF, No Load (LTC1177C-12, SW Pkg)	●	5.00	5.7	8	V
		C_{OUT} = 1000pF, V_{IN} = 11.4V (LTC1177C-12, N Pkg)	●	4.40	4.9	7	V
		C_{OUT} = 1000pF, V_{IN} = 11.4V (LTC1177C-12, SW Pkg)	●	4.60	5.3	7	V
		C_{OUT} = 1000pF, No Load (LTC1177I-12, N Pkg)	●	4.50	5.2	8	V
		C_{OUT} = 1000pF, No Load (LTC1177I-12, SW Pkg)	●	4.75	5.7	8	V
		C_{OUT} = 1000pF, V_{IN} = 11.4V (LTC1177I-12, SW Pkg)	●	4.50	5.3	7	V
I_{IN}	Input Current	C_{IN} = 1000pF (LTC1177C-12)	●		2.5	3.0	mA
		C_{IN} = 1000pF (LTC1177I-12)	●		2.5	3.4	mA
I_{LIM}	Current Limit	R_{SENSE} = 1Ω (LTC1177C-12)	●	400	620	800	mA
		R_{SENSE} = 1Ω (LTC1177I-12)	●	350	620	900	mA
t_{ON}	Turn On Time	C_{OUT} = 1000pF, No Load (LTC1177C-12)	●		1.0	2.5	ms
		C_{OUT} = 1000pF, No Load (LTC1177I-12, N Pkg)			1.0		ms
		C_{OUT} = 1000pF, No Load (LTC1177I-12, SW Pkg)	●		1.0	2.5	ms
t_{OFF}	Turn Off Time	C_{OUT} = 1000pF, No Load (LTC1177C-12)	●		1.0	1.2	ms
		C_{OUT} = 1000pF, No Load (LTC1177I-12, N Pkg)			1.0		ms
		C_{OUT} = 1000pF, No Load (LTC1177I-12, SW Pkg)	●		1.0	1.5	ms
V_{ISO}	Isolation Voltage	1 Minute (Note 1)		2500			V_{RMS}
		1 Second		3000			V_{RMS}
TCM	Common-Mode Slew Rate	V_{OUT} < 1.5V, C_{OUT}= 1000pF				1000	V/µs

The ● denotes specifications which apply over the full operating temperature range.

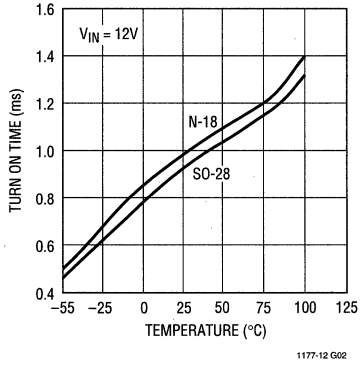
Note 1: Value derived from 1 second test.

TYPICAL PERFORMANCE CHARACTERISTICS

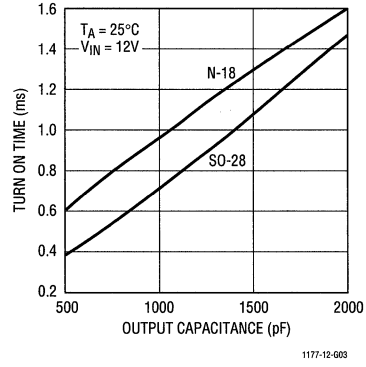
LTC1177-12
Turn Off Time vs Temperature



LTC1177-12
Turn On Time vs Temperature

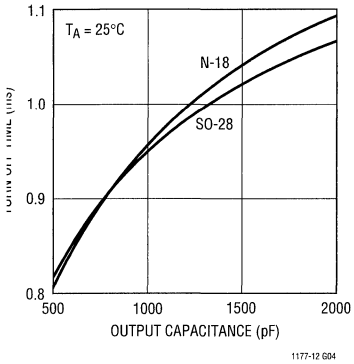


LTC1177-12
Turn On Time to V_{OUT} = 4.5V vs Output Capacitance

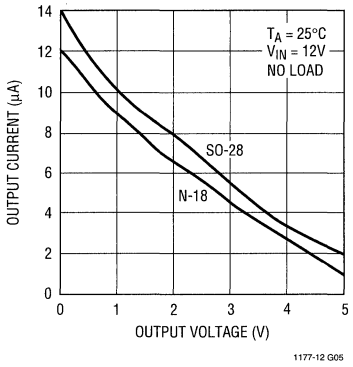


TYPICAL PERFORMANCE CHARACTERISTICS

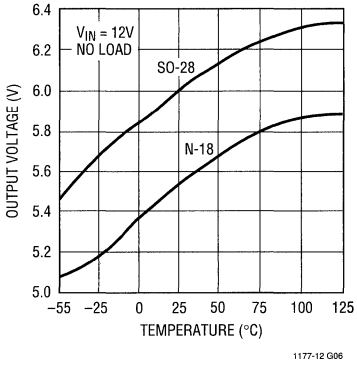
LTC1177-12
Turn-Off Time to V_{OUT} = 1V vs Output Capacitance



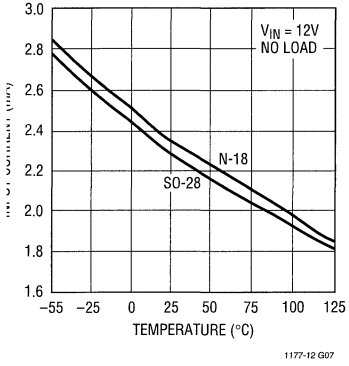
LTC1177-12
Output Current vs Output Voltage



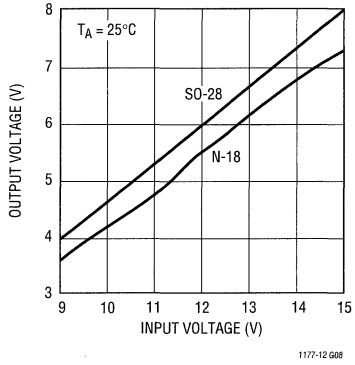
LTC1177-12
Output Voltage vs Temperature



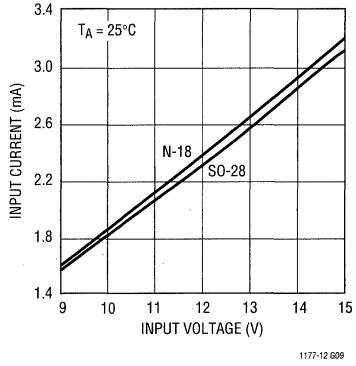
LTC1177-12
Input Current vs Temperature



LTC1177-12
Output Voltage vs Input Voltage



LTC1177-12
Input Current vs Input Voltage



PIN FUNCTIONS

V_{IN}: Voltage Input, 5.25V ≥ V_{IN} ≥ 4.75V (LTC1177-5) and 2.6V ≥ V_{IN} ≥ 11.4V (LTC1177-12). Connect a 0.01µF capacitor between V_{IN} and GND1 when the source impedance is high or the V_{IN} connection is long.

OUT: Output Voltage. The output voltage level is 8V (typ) for SW package and 7.5V (typ) for N package (LTC1177-5) with 5V at V_{IN} pin; 5.7V (typ) for SW package and 5.2V (typ) for N package (LTC1177-12) with 12V at V_{IN} pin. This pin is to drive the gate of the external N-channel MOSFET.

SENSE: Current Limit Sense Input. Connecting a 1Ω resistor from the Sense pin to GND2 would limit the current through the power MOSFET at around 620mA (typ). I_{LIM} = 620mV/R_{SENSE}.

GND2: Floating Ground Connects to the source of the external N-channel MOSFET.

GND1: Input Ground. The ground connection of the input control signal.

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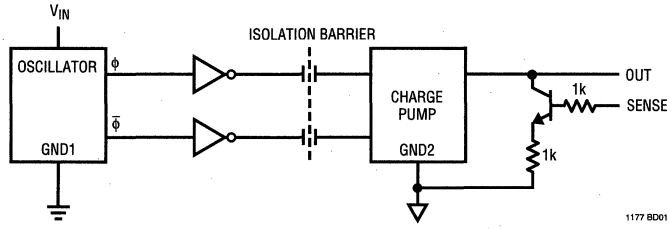
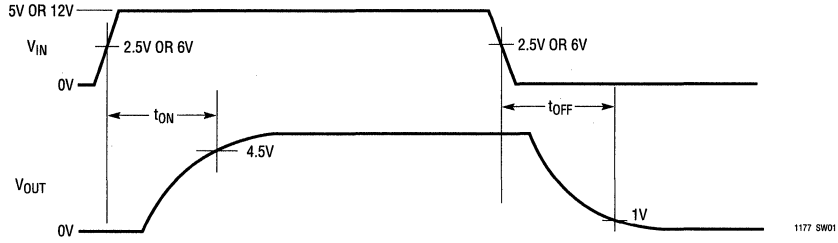
BLOCK DIAGRAM

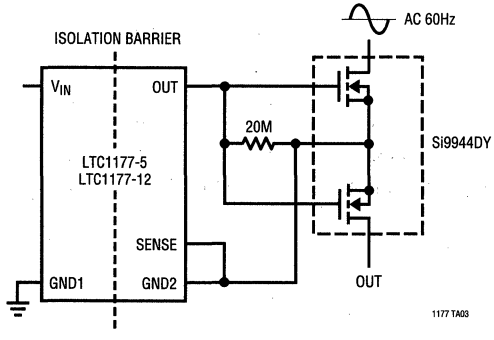


SWITCHING WAVEFORMS

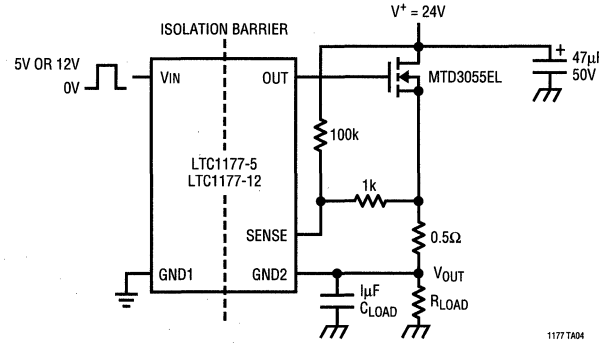


TYPICAL APPLICATIONS

Solid State Relay

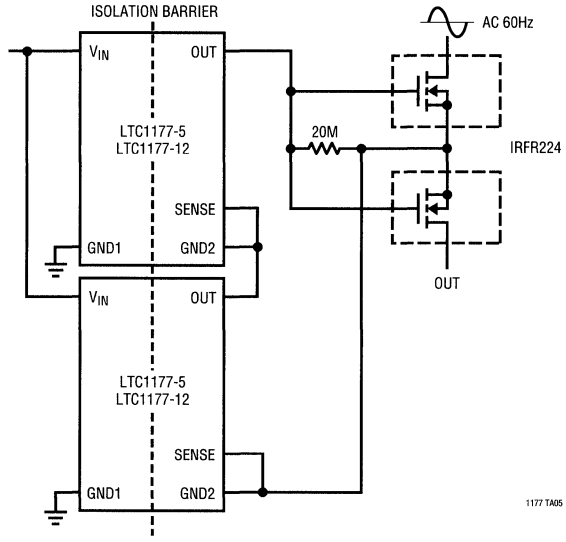


Isolated High-Side Switch with Fold-Back Current Limit

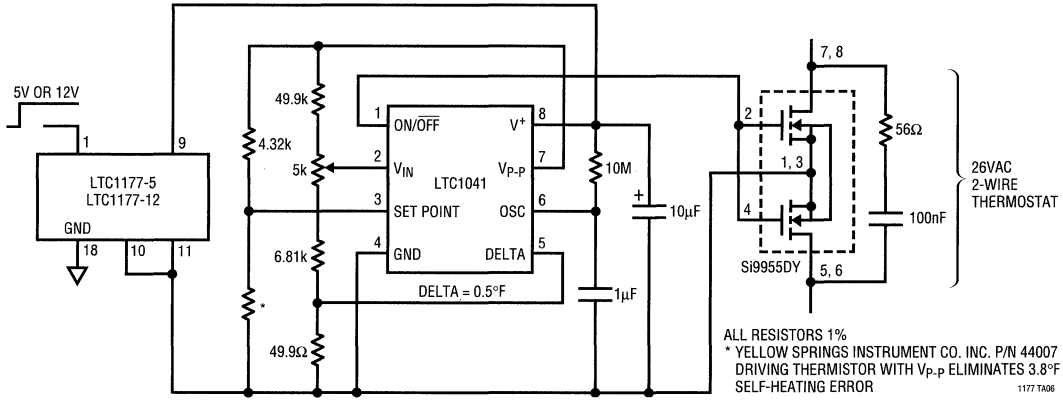


TYPICAL APPLICATIONS

Solid State Relay



Fully Floating 50°F to 100°F Thermostat



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1145/LTC1146	Low Power Digital Isolator	Can Pass Digital Information Across Isolation Barrier
LT1158	Half-Bridge N-Channel Power MOSFET Driver	Can Be Used for Motor Speed Control
LTC1255	Dual 24V High-Side MOSFET Driver	User Set Current Limiting

12-Bit, 10mW, 100ksps ADCs with 1µA Shutdown

June 1995

FEATURES

- **Low Power Dissipation: 10mW Typical**
- **Sample Rate: 100ksps**
- Samples Inputs Well Beyond Nyquist, 71dB S/(N + D) and 77dB THD Minimum at f_{IN} = 100kHz
- Single Supply 5V or ±5V Operation
- ±0.5LSB Maximum INL and ±0.75LSB Maximum DNL (A Grade)
- **Power Shutdown to 1µA in Sleep Mode**
- 160µA Nap Mode (LTC1277) with Instant Wake-Up
- 30ppm/°C (Max) Internal Reference (A Grade) Can Be Overdriven
- Internal Synchronized Clock
- 0V to 4.096V or ±2.048V Input Ranges (1mV/LSB)
- 24-Lead SO Wide Package

APPLICATIONS

- Battery-Powered Portable Systems
- High Speed Data Acquisition for PCs
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Spectrum Analysis

DESCRIPTION

The LTC®1274/LTC1277 are 8µs sampling 12-bit A/D converters which draw only 2mA (typ) from a single 5V or ±5V supplies. These easy-to-use devices come complete with a 2µs sample-and-hold, a precision reference and an internally trimmed clock. Unipolar and bipolar conversion modes add to the flexibility of the ADCs.

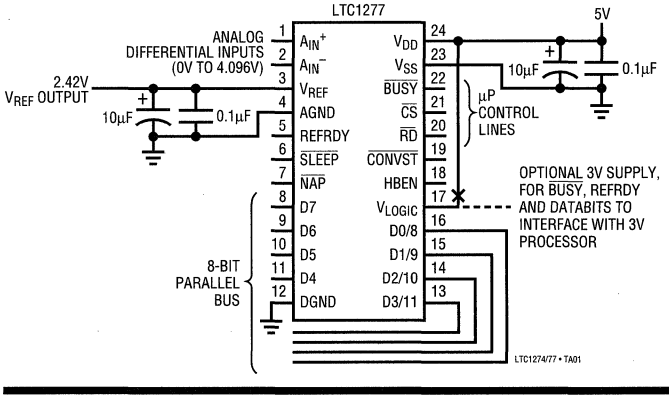
Two power-down modes are available in the LTC1277. In Nap mode, the LTC1277 draws only 160µA and the instant wake-up from Nap mode allows the LTC1277 to be powered down even during brief inactive periods. In Sleep mode only 1µA will be drawn. A REFRDY signal is used to show the ADC is ready to sample after waking up from Sleep mode. The LTC1274 also provides the Sleep mode and REFRDY signal.

The A/D converters convert 0V to 4.096V unipolar inputs from a single 5V supply or ±2.048V bipolar inputs from ±5V supplies.

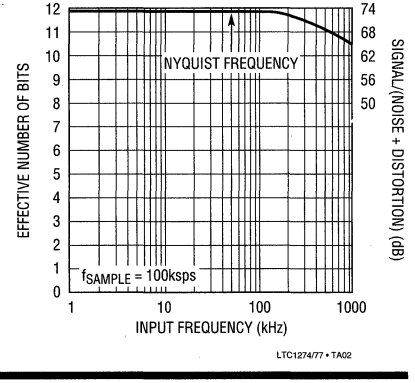
The LTC1274 has a single-ended input and a 12-bit parallel data format. The LTC1277 offers a differential input and a 2-byte read format. The bipolar mode is formatted as 2's complement for the LTC1274 and offset binary for the LTC1277.

TYPICAL APPLICATION

Single 5V Supply, 10mW, 100kHz, 12-Bit ADC



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency



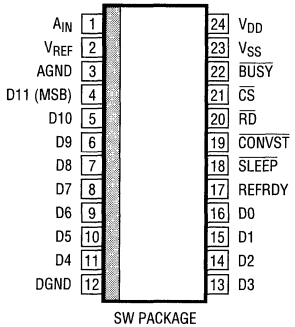
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 7V
Negative Supply Voltage (V_{SS})
  Bipolar Operation Only ..... –6V to GND
Total Supply Voltage (V_{DD} to V_{SS})
  Bipolar Operation Only 12V
Analog Input Voltage (Note 3)
  Unipolar Operation ..... – 0.3V to V_{DD} + 0.3V
  Bipolar Operation..... V_{SS} – 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4)
  Unipolar Operation ..... – 0.3V to 12V
  Bipolar Operation..... V_{SS} – 0.3V to 12V
Digital Output Voltage
  Unipolar Operation ..... – 0.3V to V_{DD} + 0.3V
  Bipolar Operation..... –0.3V to V_{DD} + 0.3V
Power Dissipation..... 500mW
Operating Temperature Range
  Commercial ..... 0°C to 70°C
  Industrial ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW

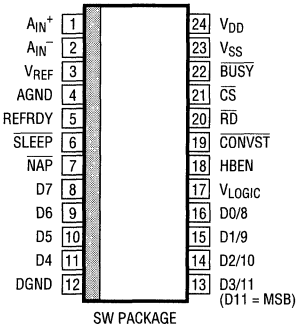


SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1274CSW
LTC1274AISW
LTC1274ISW

TOP VIEW



SW PACKAGE
24-LEAD PLASTIC SO WIDE

T_{JMAX} = 110°C, θ_{JA} = 130°C/W

ORDER PART NUMBER
LTC1277CSW
LTC1277AISW
LTC1277ISW

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		LTC1274A/LTC1277A MIN	TYP	MAX	LTC1274/LTC1277 MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			12			Bits
Integral Linearity Error	(Note 7)	●			±0.5			±1	LSB
Differential Linearity Error		●			±0.75			±1	LSB
Offset Error	(Note 8)				±4			±5	LSB
		●			±5			±7	LSB
Gain Error					±15			±20	LSB
Gain Error Tempco	$I_{OUT(REF)}$ = 0	●		±5	±30		±10	±45	ppm/°C

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ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 10)	$4.75V \le V_{DD} \le 5.25V$ (Unipolar) $4.75V \le V_{DD} \le 5.25V$, $-5.25V \le V_{SS} \le -2.45V$ (Bipolar)	● ●		0 to 4.096 ±2.048		V V
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode) During Conversions (Hold Mode)			45 5		pF pF

DYNAMIC ACCURACY (Notes 5, 9)

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A MIN	TYP	MAX	LTC1274/LTC1277 MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	50kHz Input Signal 100kHz Input Signal	 ●	 71	73 72.5		 70	73 72.5		dB dB
THD	Total Harmonic Distortion Up to 5th Harmonic	50kHz Input Signal 100kHz Input Signal	 ●		−84 −82	 −77		−84 −82	 −76	dB dB
	Peak Harmonic or Spurious Noise	50kHz Input Signal 100kHz Input Signal	 ●		−84 −82	 −77		−84 −82	 −76	dB dB
IMD	Intermodulation Distortion	f_{IN1} = 96.95kHz, f_{IN2} = 97.68kHz 2nd Order Terms 3rd Order Terms			 −78 −81			 −78 −81		 dB dB
	Full Power Bandwidth				2			2		MHz
	Full Linear Bandwidth [S/(N + D) ≥ 68dB]				400			400		kHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		LTC1274A/LTC1277A MIN	TYP	MAX	LTC1274/LTC1277 MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.400	2.420	2.440	2.400	2.420	2.440	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±5	±30		±10	±45	ppm/°C
V_{REF} Line Regulation	$4.75V \le V_{DD} \le 5.25V$ $-5.25V \le V_{SS} \le -4.75V$			0.01 0.01			0.01 0.01		LSB/V LSB/V
V_{REF} Load Regulation	$70\mu A \ge I_{OUT} \ge -5mA$		2			2		LSB/mA	

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage, All Logic Outputs	V_{DD} = 4.75V $I_O = -10\mu A$ $I_O = -200\mu A$	 ●	 4.0	4.7		 V V

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage, All Logic Outputs	V_{DD} = 4.75V I_O = 160µA I_O = 1.6mA	 ●		 0.05 0.10	 0.4	 V V
I_{OZ}	High-Z Output Leakage D11 to D0/8	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
C_{OZ}	High-Z Output Capacitance D11 to D0/8	$\overline{CS}$ High (Note 10)	●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
V_{DD}	Positive Supply Voltage (Notes 11, 12)	Unipolar and Bipolar Mode		4.75		5.25	V
V_{SS}	Negative Supply Voltage (Note 11)	Bipolar Mode Only		–2.45		–5.25	V
I_{DD}	Positive Supply Current	f_{SAMPLE} = 100ksps $\overline{NAP}$ = 0V (LTC1277 Only) $\overline{SLEEP}$ = 0V	● ● ●		2 160 0.3	4 320 5	mA µA µA
I_{SS}	Negative Supply Current	f_{SAMPLE} = 100ksps, Bipolar Mode Only $\overline{SLEEP}$ = 0V	● ●		40 0.3	70 5	µA µA
P_{DISS}	Power Dissipation	f_{SAMPLE} = 100ksps $\overline{NAP}$ = 0V (LTC1277 Only) $\overline{SLEEP}$ = 0V (Unipolar/Bipolar)	● ● ●		10 0.8	20 1.8 25/50	mW mW µW

TIMING CHARACTERISTICS (Note 5) See Figures 4 to 8.

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	(Note 11)	●	100			ksps
t_{CONV}	Conversion Time		●		6	8	µs
t_{ACQ}	Acquisition Time		●		0.35	2	µs
t_1	$\overline{CS}\downarrow$ to $\overline{RD}\downarrow$ Setup Time	(Note 10)	●	0			ns
t_2	$\overline{CS}\downarrow$ to $\overline{CONVST}\downarrow$ Setup Time	(Note 10)	●	30			ns
t_3	$\overline{NAP}\uparrow$ to $\overline{CONVST}\downarrow$ Wake-Up Time	(LTC1277 Only) (Note 11)			2		µs
t_4	$\overline{CONVST}$ Low Time	(Note 13)	●	40			ns
t_5	$\overline{CONVST}\downarrow$ to $\overline{BUSY}\downarrow$ Delay	C_L = 100pF	●		70	150	ns
t_6	Data Ready Before $\overline{BUSY}\uparrow$	C_L = 100pF	●	20	65		ns
t_7	Delay Between Conversions	(Note 11)	●		0.35	2	µs
t_8	Wait Time $\overline{RD}\downarrow$ After $\overline{BUSY}\uparrow$	(Note 10)	●	–20			ns
t_9	Data Access Time After $\overline{RD}\downarrow$	C_L = 20pF (Note 10)	 ●		50	110 140	ns ns
		C_L = 100pF	 ●		65	125 170	ns ns
t_{10}	Bus Relinquish Time	C_L = 100pF	 ●	20 20	60	90 100	ns ns

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TIMING CHARACTERISTICS (Note 5) See Figures 4 to 8.

SYMBOL	PARAMETER	CONDITIONS		LTC1274A/LTC1277A LTC1274/LTC1277 MIN	TYP	MAX	UNITS
t_{11}	$\overline{RD}$ Low Time	(Note 10)	●	t_9			ns
t_{12}	$\overline{CONVST}$ High Time	(Notes 10, 13)	●	40			ns
t_{13}	Aperture Delay of Sample-and-Hold				35		ns
t_{14}	$\overline{SLEEP}\uparrow$ to REFRDY↑ Wake-Up Time	10µF Bypass at V_{REF} Pin			4		ms
t_{15}	HBEN↑ to High Byte Data Valid	C_L = 100pF (LTC1277 Only)	●		35	100	ns
t_{16}	HBEN↓ to Low Byte Data Valid	C_L = 100pF (LTC1277 Only)	●		45	100	ns
t_{17}	HBEN↑ to $\overline{RD}\downarrow$ Setup Time	(Note 10) (LTC1277 Only)	●	10			ns
t_{18}	$\overline{RD}\uparrow$ to HBEN↓ Setup Time	(Note 10) (LTC1277 Only)	●	10			ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} (ground for unipolar mode) or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for unipolar mode) or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} (ground for unipolar mode), they will be clamped by internal diodes. This product can handle input currents greater than 60mA below V_{SS} (ground for unipolar mode) without latch-up. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V (V_{SS} = –5V for bipolar mode), f_{SAMPLE} = 100ksps, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for unipolar and bipolar modes.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: For LTC1274, bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111. For LTC1277, bipolar offset voltage is measured from –0.5LSB when the output code flickers between 0111 1111 1111 and 1000 0000 0000.

Note 9: The AC tests apply to bipolar mode only and the S/(N + D) is 71dB (typ) for unipolar mode at 100kHz input frequency.

Note 10: Guaranteed by design, not subject to test.

Note 11: Recommended operating conditions.

Note 12: A_{IN} must not exceed V_{DD} or fall below V_{SS} by more than 50mV to specified accuracy.

Note 13: The falling $\overline{CONVST}$ edge starts a conversion. If $\overline{CONVST}$ returns high at a bit decision point during the conversion it can create small errors. For best performance ensure that $\overline{CONVST}$ returns high either within 400ns after conversion start (i.e., before the first bit decision) or after $\overline{BUSY}$ rises (i.e., after bit test). See timing diagrams mode 1a and 1b (Figures 4, 5).

PIN FUNCTIONS

LTC1274

A_{IN} (Pin 1): Analog Input. 0V to 4.096V (unipolar) or ±2.048V (bipolar).

V_{REF} (Pin 2): 2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic). V_{REF} can be overdriven positive with an external reference voltage.

AGND (Pin 3): Analog Ground.

D11 to D4 (Pins 4 to 11): Three-State Data Outputs. D11 is the Most Significant Bit.

DGND (Pin 12): Digital Ground.

D3 to D0 (Pins 13 to 16): Three-State Data Outputs.

REFRDY (Pin 17): Reference Ready Signal. It goes HIGH when the reference has settled after $\overline{SLEEP}$ and the ADC is ready to sample.

$\overline{SLEEP}$ (Pin 18): Sleep Mode Input. Tie this pin to LOW to put the ADC in Sleep mode and save power (REFRDY will go LOW). The device will draw 1µA in this mode.

$\overline{CONVST}$ (Pin 19): Conversion Start Signal. This active LOW signal starts a conversion on its falling edge (to recognize $\overline{CONVST}$, $\overline{CS}$ has to be LOW.)

PIN FUNCTIONS

$\overline{RD}$ (Pin 20): Read Input. This enables the output drivers when $\overline{CS}$ is LOW.

$\overline{CS}$ (Pin 21): The Chip Select input must be low for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs.

$\overline{BUSY}$ (Pin 21): The Busy output shows the converter status. It is LOW when a conversion is in progress. The rising Busy edge can be used to latch the conversion result.

V_{SS} (Pin 23): Negative 5V Supply. –5V will select bipolar operation. Bypass to AGND with 0.1µF ceramic. Tie this pin to analog ground to select unipolar operation.

V_{DD} (Pin 24): Positive 5V Supply. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

LTC1277

A_{IN}^+ (Pin 1): Positive Analog Input. ($A_{IN}^+ - A_{IN}^-$) = 0V to 4.096V (unipolar) or ±2.048V (bipolar).

A_{IN}^- (Pin 2): Negative Analog Input. This pin needs to be free of noise during conversion. For single-ended inputs tie A_{IN}^- to analog ground.

V_{REF} (Pin 3): 2.42V Reference Output. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic). V_{REF} can be overdriven positive with an external reference voltage.

AGND (Pin 4): Analog Ground.

REFRDY (Pin 5): Reference Ready Signal. It goes HIGH when the reference has settled after $\overline{SLEEP}$ and the ADC is ready to sample.

$\overline{SLEEP}$ (Pin 6): Sleep Mode Input. Tie this pin to LOW to put the ADC in Sleep mode and save power (REFRDY will go LOW). The device will draw 1µA in this mode.

$\overline{NAP}$ (Pin 7): Nap Mode Input. Pulling this pin LOW will shut down all currents in the ADC except the reference. In this mode the ADC draws 160µA. Wake-up from Nap mode is about 2µs.

D7 to D4* (Pins 8 to 11): Three-State Data Outputs.

DGND (Pin 12): Digital Ground.

D3/11 to D0/8* (Pins 13 to 16): Three-State Data Outputs. D11 is the Most Significant Bit.

V_{LOGIC} (Pin 17): 5V or 3V Digital Power Supply. This pin allows a 5V or 3V logic interface with the processor. All logic outputs (Data Bits, $\overline{BUSY}$ and REFRDY) will swing between 0V and V_{LOGIC}.

HBEN (Pin 18): High Byte Enable Input. The four Most Significant Bits will appear at pins 13 to 16 when this pin is HIGH. The LTC1277 uses straight binary for unipolar mode and offset binary for bipolar mode.

$\overline{CONVST}$ (Pin 19): Conversion Start Signal. This active low signal starts a conversion on its falling edge (to recognize $\overline{CONVST}$, $\overline{CS}$ has to be LOW).

$\overline{RD}$ (Pin 20): Read Input. This enables the output drivers when $\overline{CS}$ is LOW.

$\overline{CS}$ (Pin 21): The Chip Select input must be LOW for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs.

$\overline{BUSY}$ (Pin 22): The $\overline{BUSY}$ output shows the converter status. It is LOW when a conversion is in progress.

V_{SS} (Pin 23): –5V negative supply will select bipolar operation. Bypass to AGND with a 0.1µF ceramic. Tie this pin to analog ground to select unipolar operation.

V_{DD} (Pin 24): 5V Positive Supply. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

*The LTC1277 bipolar mode is in offset binary.

Table 1. LTC1277 Two-Byte Read Data Bus Status

DATA OUTPUTS	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
LOW Byte	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HIGH Byte	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

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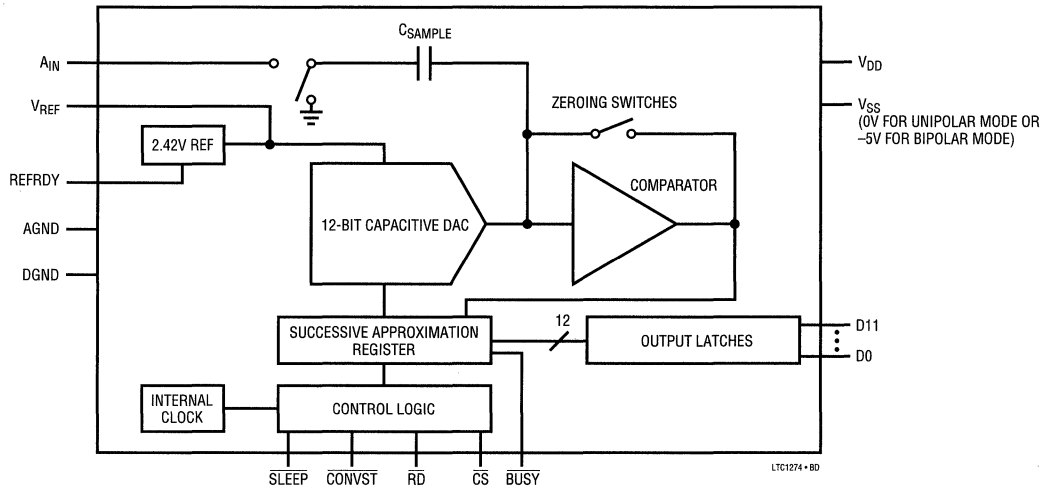
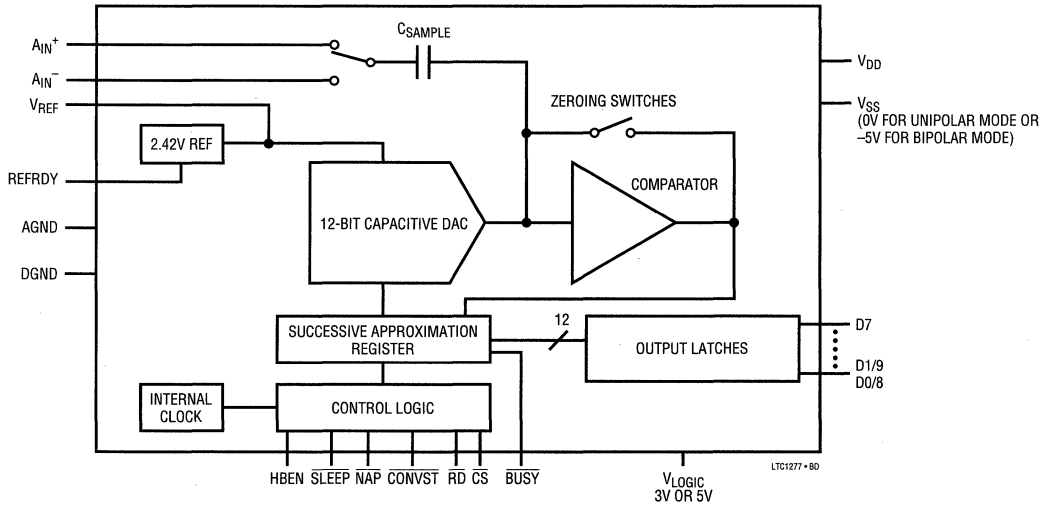
BLOCK DIAGRAMS

LTC1274

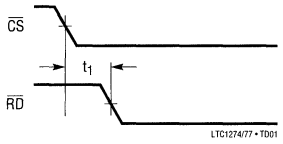


LTC1277

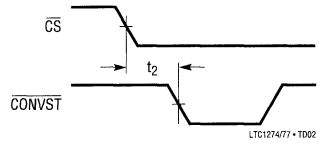


TIMING DIAGRAM

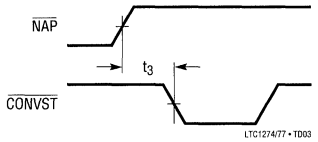
$\overline{CS}$ to $\overline{RD}$ Setup Timing



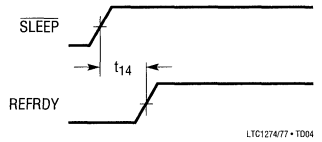
$\overline{CS}$ to $\overline{CONVST}$ Setup Timing



$\overline{NAP}$ to $\overline{CONVST}$ Setup Timing (LTC1277)



$\overline{SLEEP}$ to REFRDY Wake-Up Timing



APPLICATIONS INFORMATION

Driving the Analog Input

The analog input of the LTC1274/LTC1277 is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion the analog input draws only a small leakage current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 2µs to small current transients will allow maximum speed operation. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADCs' A_{IN} input include the LT®1006, LT1007, LT1220, LT1223 and LT1224 op amps.

LTC1277 A_{IN}^+/A_{IN}^- Input Settling

The input capacitor for the LTC1277 is switched onto the A_{IN}^+ input during the sample phase. The voltage on the A_{IN}^+ input must settle completely within the sample period. At the end of the sample phase the input capacitor switches to the A_{IN}^- input and the conversion starts. During the conversion, the A_{IN}^+ input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. It is critical that the A_{IN}^- input voltage be free of noise and settles completely during the conversion.

Internal Reference

The ADCs have an on-chip, temperature compensated, curvature corrected, bandgap reference which is factory trimmed to 2.42V. It is internally connected to the DAC and is available at pin 2 (LTC1274) or pin 3 (LTC1277) to provide up to 1mA current to an external load.

For minimum code transition noise the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic).

The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment. The V_{REF} pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should be driven to no more than 3V to keep the input span within the 5V supply in unipolar mode. In bipolar mode the reference should be driven to no more than 5V, the positive supply voltage of the chip.

APPLICATIONS INFORMATION

Figure 1 shows an LT1006 op amp driving the reference pin. In unipolar mode, the reference can be driven up to 2.95V at which point it will provide a 0V to 5V input span. For the bipolar mode, the reference can be driven up to 5V at which point it will provide a ±4.23V input span. Figure 2 shows a typical reference, the LT1019A-2.5 connected to the LTC1274. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-2.5) and a ±2.115V (bipolar) or 4.231V (unipolar) full scale.

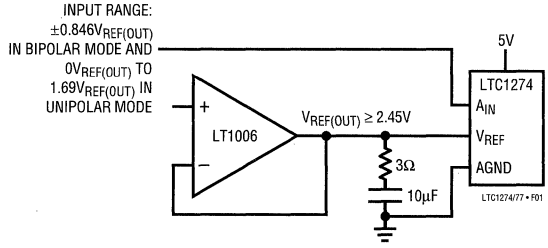


Figure 1. Driving the V_{REF} with the LT1006 Op Amp

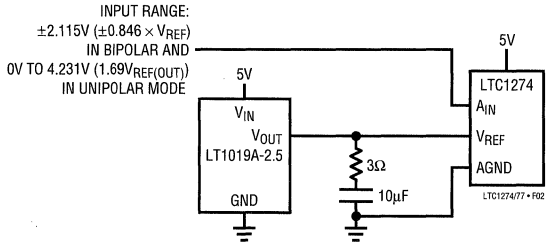


Figure 2. Supplying a 2.5V Reference Voltage to the LTC1274 with the LT1019A-2.5

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1274/LTC1277, a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD} and V_{REF} pins as shown in Figure 3. For bipolar mode, a 0.1µF ceramic provides adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

Input signal leads to A_{IN} and signal return leads from AGND (pin 3 for LTC1274, pin 4 for LTC1277) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible a shielded cable between source and ADC is recommended.

Also, since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

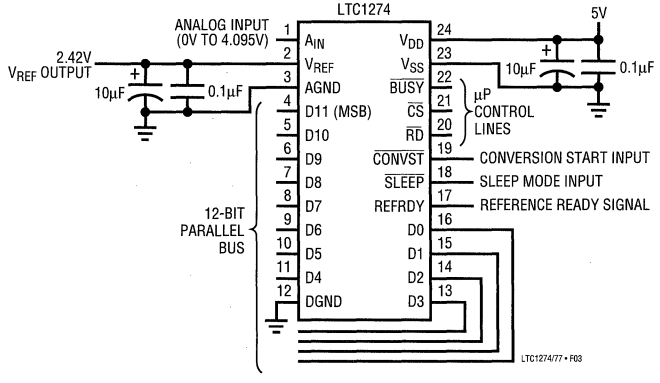


Figure 3. LTC1274 Typical Circuit

APPLICATIONS INFORMATION

A single point analog ground separate from the logic system ground should be established with an analog ground plane at AGND or as close as possible to the ADC. Pin 12 (DGND) and all other analog grounds should be connected to this single analog ground point. No other digital grounds should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a Wait state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The ADCs are designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing. A separate $\overline{CONVST}$ is used to initiate a conversion. Figures 4a to 4c are the input/output characteristics of the ADCs.

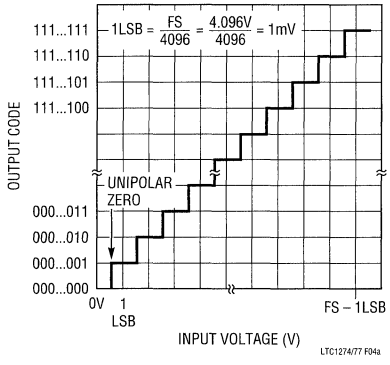


Figure 4a. LTC1274/LTC1277 Unipolar Transfer Characteristics

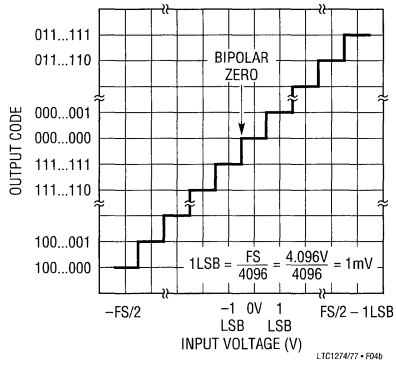


Figure 4b. LTC1274 Bipolar Transfer Characteristics (2's Complement)

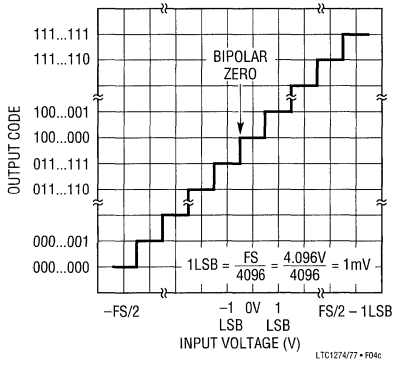


Figure 4c. LTC1277 Bipolar Transfer Characteristics (Offset Binary)

Unipolar Offset and Full-Scale Error Adjustments

In applications where absolute accuracy is important, then offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 5a shows the extra components required for full-scale error adjustment. If both offset and full-scale adjustments are needed, the circuit in Figure 5b can be used. For zero offset error apply 0.50mV (i.e., 0.5LSB) at the input and adjust the offset trim until the LTC1274/LTC1277 output code

APPLICATIONS INFORMATION

flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error apply an analog input of 4.0945V (i.e., FS – 1.5LSB or last code transition) at the input and adjust R5 until the ADC's output code flickers between 1111 1111 1110 and 1111 1111 1111.

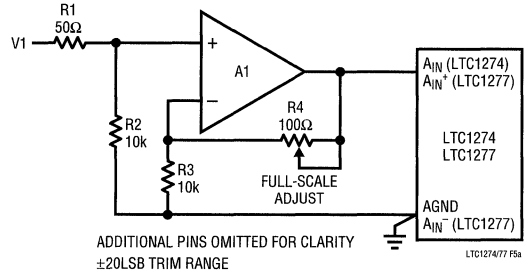


Figure 5a. Full-Scale Adjust Circuit

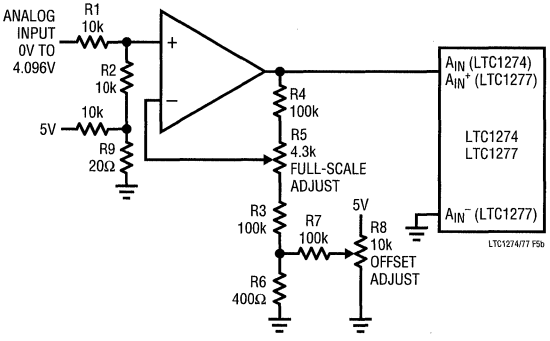


Figure 5b. LTC1274/LTC1277 Unipolar Offset and Full-Scale Adjust Circuit

LTC1274 Bipolar Offset and Full-Scale Error Adjustments

Bipolar offset and full-scale errors for LTC1274 are adjusted in a similar fashion to the unipolar case. Again, bipolar offset must be adjusted before full-scale error. Bipolar offset error adjustment is achieved by trimming the offset of the op amp driving the analog input of the

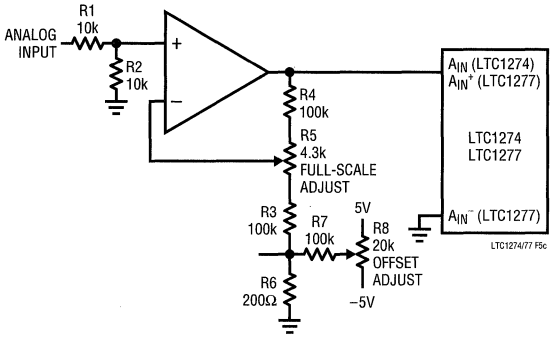


Figure 5c. LTC1274/LTC1277 Bipolar Offset and Full-Scale Adjust Circuit

LTC1274 while the input voltage is 0.5LSB below ground. This is done by applying an input voltage of –0.50mV (–0.5LSB) to the input in Figure 5c and adjusting the R8 until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.0465V (FS – 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

LTC1277 Bipolar Offset and Full-Scale Error Adjustments

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Again, bipolar offset must be adjusted before full-scale error. Bipolar offset error adjustment is achieved by trimming the offset of the op amp driving the analog input of the LTC1277 while the input voltage is 0.5LSB below ground. This is done by applying an input voltage of –0.50mV (–0.5LSB) to the input in Figure 5c and adjusting the R8 until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000. For full-scale adjustment, an input voltage of 2.0465V (FS – 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between the input 1111 1111 1110 and 1111 1111 1111.

APPLICATIONS INFORMATION

Power Shutdown

The LTC1274/LTC1277 provide shutdown features that will save power when the ADC is in inactive periods. Both ADCs have a Sleep mode. To power down the ADCs, $\overline{SLEEP}$ (pin 18 in LTC1274 or pin 6 in LTC1277) needs to be tied low. When in Sleep mode, the LTC1274/LTC1277 will not start a conversion even though the $\overline{CONVST}$ goes low. The parts are drawing 1µA. After releasing from the Sleep mode, the ADCs need 4ms (10µF bypass capacitor on V_{REF} pin) to wake up and a REFRDY signal will go to high to indicate the ADC is ready to do conversions.

For the LTC1277, it has an additional Nap mode. When pin 7 ($\overline{NAP}$ pin the LTC1277) is tied low, all the power is off except the internal reference which is still active and provides 2.42V output voltage to the other circuitry. In this mode the ADC draws 0.8mW instead of 10mW (for minimum power, the logic inputs must be within 600mV from the supply rails). The wake-up time from the power shutdown to active state is 2µs.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs in the LTC1274: $\overline{CS}$, $\overline{CONVST}$ and $\overline{RD}$. For the LTC1277 there are four digital inputs: $\overline{CS}$, $\overline{CONVST}$, $\overline{RD}$ and HBEN. A logic "0" for $\overline{CONVST}$ will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output and this is LOW while conversion is in progress. The High Byte Enable input (HBEN) in the LTC1277 is to multiplex the 12 bits of conversion data onto the lower D7 to D0/8 outputs.

Figures 6 through 10 show several different modes of operation. In modes 1a and 1b (Figures 6 and 7) $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling edge of $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

In mode 2 (Figure 8) $\overline{CS}$ is tied low. The falling edge of $\overline{CONVST}$ signal again starts the conversion. Data outputs are in three-state until read by the MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared MPU databus.

In slow memory and ROM modes (Figures 9 and 10) $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts the conversion and reads the output with the $\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting the conversion. $\overline{BUSY}$ goes low, forcing the processor into a Wait state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high releasing the processor; the processor applies a logic high to $\overline{RD}$ (= $\overline{CONVST}$) and reads the new conversion data.

In ROM mode, the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$), starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

APPLICATIONS INFORMATION

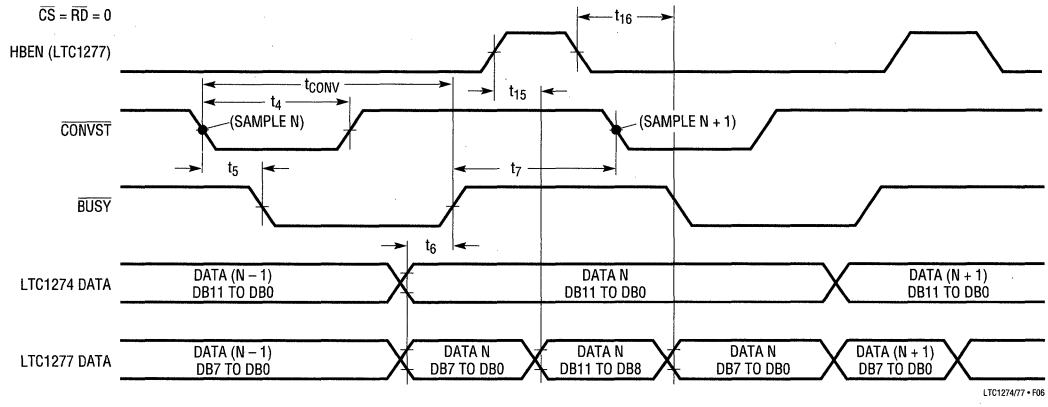


Figure 6. Mode 1a. $\overline{\text{CONVST}}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{\text{CONVST}}$ = ⊓_⊓)

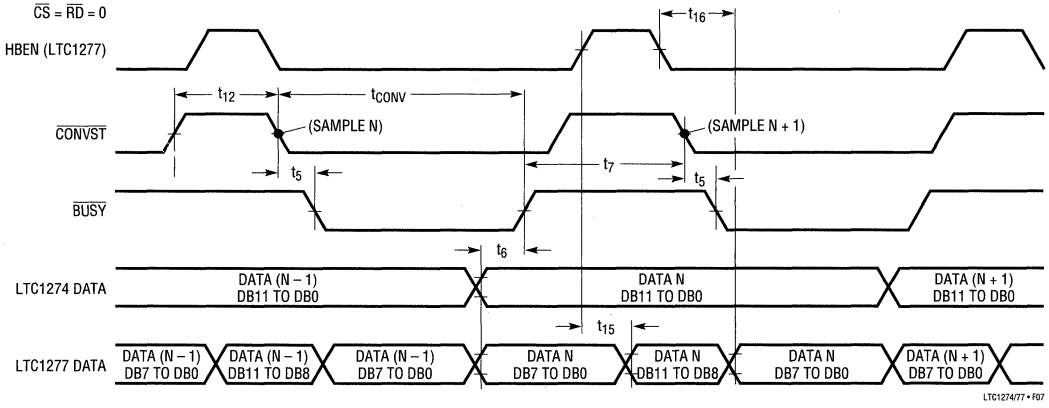


Figure 7. Mode 1b. $\overline{\text{CONVST}}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{\text{CONVST}}$ = ⊓_⊓)

APPLICATIONS INFORMATION

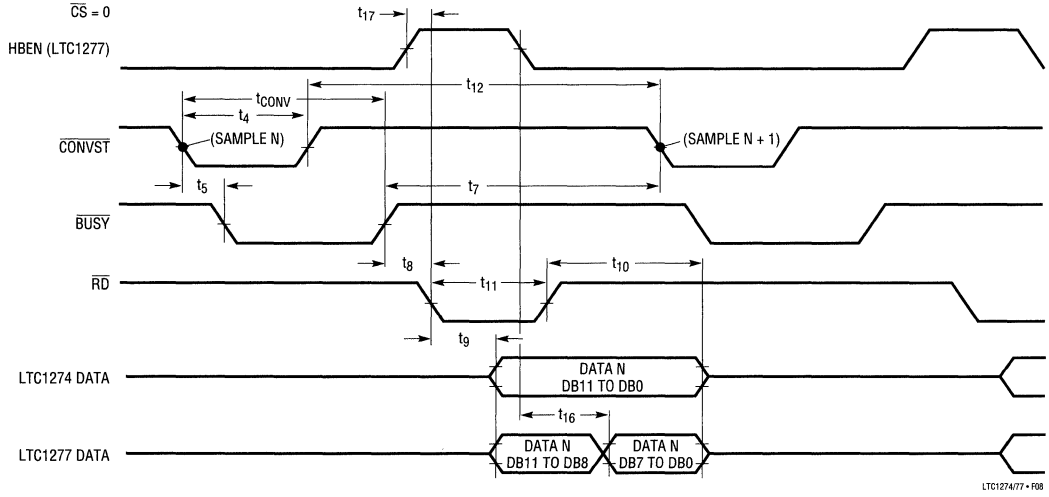


Figure 8. Mode 2. $\overline{CONVST}$ Starts a Conversion. Data is Read by $\overline{RD}$

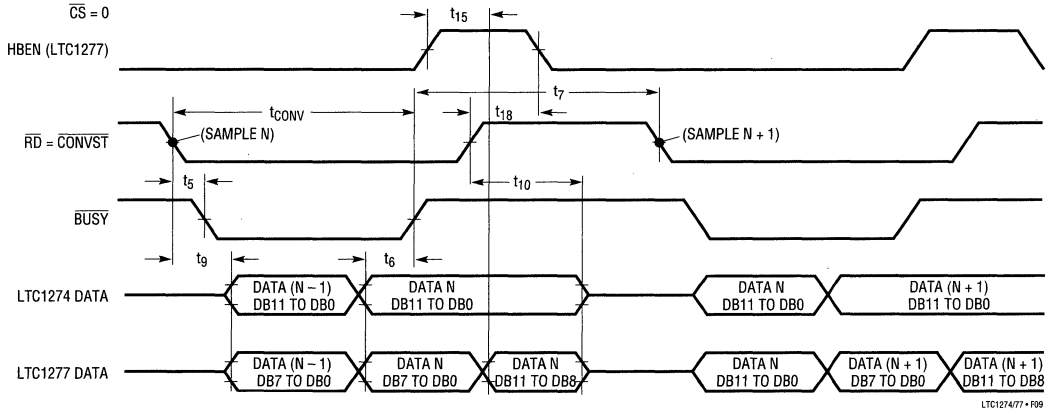


Figure 9. Slow Memory Mode

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APPLICATIONS INFORMATION

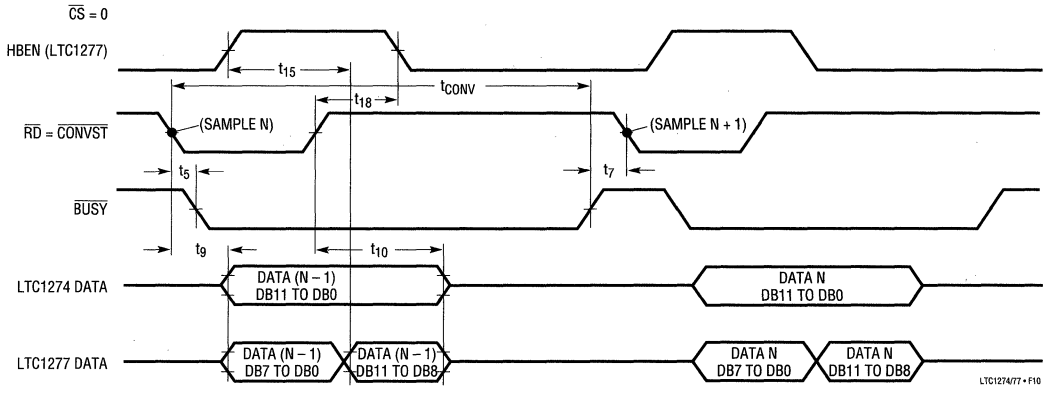


Figure 10. ROM Mode Timing

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1272	12-Bit, 3µs, 250kHz Sampling A/D Converter	Single 5V, Sampling 7572 Upgrade
LTC1273/75/76	12-Bit, 300ksps Sampling A/D Converters with Reference	Complete with Clock, Reference
LTC1278	12-Bit, 500ksps Sampling A/D Converter with Shutdown	70dB SINAD at Nyquist, Low Power
LTC1279	12-Bit, 600ksps Sampling A/D Converter with Shutdown	70dB SINAD at Nyquist, Low Power
LTC1282	12-Bit, 140ksps Sampling A/D Converter with Reference	3V or ±3V ADC with Reference, Clock
LTC1409	12-Bit, 800ksps Sampling A/D Converter with Shutdown	Fast, Complete Low Power ADC
LTC1410	12-Bit, 1.25Msps Sampling A/D Converter with Shutdown	Fast, Complete Wideband ADC

LT1304/LT1304-3.3/LT1304-5

Micropower DC/DC Converters with Low-Battery Detector Active in Shutdown

May 1995

FEATURES

- 5V at 200mA from Two Cells
- **10μA Quiescent Current in Shutdown**
- Operates with V_{IN} as Low as 1.5V
- **Low-Battery Detector Active in Shutdown**
- Low Switch V_{CESAT}: 500mV at 1A Typical
- 120μA Quiescent Current in Active Mode
- Frequency Up to 300kHz
- Programmable Peak Current with One Resistor
- 8-Lead SO Package

APPLICATIONS

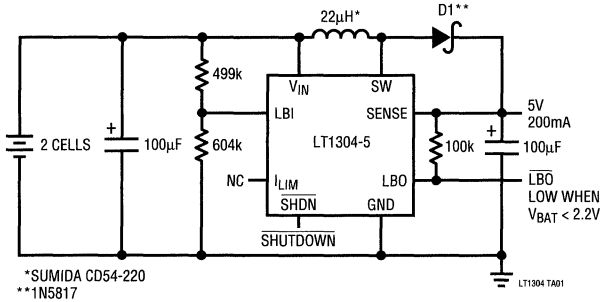
- 2-, 3-, or 4-Cell to 5V or 3.3V Step-Up
- Portable Instruments
- Bar-Code Scanners
- Palmtop Computers
- Diagnostic Medical Instrumentation
- Personal Data Communicators/Computers

DESCRIPTION

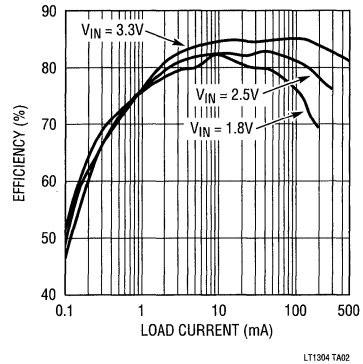
The LT®1304 is a micropower step-up DC/DC converter ideal for use in small, low voltage battery-operated systems. The devices operate from a wide input supply range of 1.6V to 8V. The LT1304-3.3 and LT1304-5 generate regulated outputs of 3.3V and 5V and the adjustable LT1304 can deliver output voltages up to 25V. Quiescent current, 120μA in active mode, decreases to just 10μA in shutdown, with the low-battery detector still active. Peak switch current, internally set at 1A, can be reduced by adding a single resistor from the I_{LIM} pin to ground. The high speed operation of the LT1304 allows the use of small, surface-mountable inductors and capacitors. The LT1304 is available in an 8-lead SO package.

TYPICAL APPLICATION

2-Cell to 5V Step-Up Converter



Efficiency



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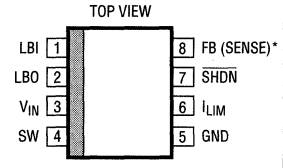
ABSOLUTE MAXIMUM RATINGS

V_{IN} Voltage 8V
SW Voltage ..... −0.4V to 25V
FB Voltage (LT1304) ..... V_{IN} + 0.3V
Sense Voltage (LT1304-3.3/LT1304-5) 8V
I_{LIM} Voltage 5V
$\overline{SHDN}$ Voltage 6V
LBI Voltage ..... V_{IN}
LBO Voltage 8V
Maximum Power Dissipation 500mW
Junction Temperature ..... 125°C
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

*FIXED OUTPUT VERSION

T_{JMAX} = 125°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1304CS8 LT1304CS8-3.3 LT1304CS8-5
S8 PART MARKING
1304 13043 13045

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 2V, $V_{\overline{SHDN}}$ = 2V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage		●		1.5	1.65	V
Operating Voltage Range		●			8	V
Quiescent Current	$V_{\overline{SHDN}}$ = 2V, Not Switching	●		120	200	µA
Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V, V_{IN} = 2V $V_{\overline{SHDN}}$ = 0V, V_{IN} = 5V	● ●		7 27	15 50	µA µA
Comparator Trip Point	LT1304	●	1.22	1.24	1.26	V
FB Pin Bias Current	LT1304	●		10	25	nA
Sense Pin Leakage in Shutdown	$V_{\overline{SHDN}}$ = 0V, Fixed Output Versions	●		0.002	1	µA
Output Sense Voltage	LT1304-3.3 LT1304-5	● ●	3.17 4.80	3.3 5.05	3.43 5.25	V V
Line Regulation	1.8V ≤ V_{IN} ≤ 8V	●		0.04	0.15	%/V
LBI Input Threshold	Falling Edge	●	1.10	1.17	1.24	V
LBI Bias Current		●		6	20	nA
LBI Input Hysteresis		●		35	65	mV
LBO Output Voltage Low	I_{SINK} = 500µA	●		0.2	0.4	V
LBO Output Leakage Current	LBI = 1.5V, LBO = 5V	●		0.01	0.1	µA
$\overline{SHDN}$ Input Voltage High $\overline{SHDN}$ Input Voltage Low		● ●	1.4		 0.4	V V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 5V $V_{\overline{SHDN}}$ = 0V	● ●	 −5	5 −2	8	µA µA
Switch Off Time		●	1	1.5	2	µs
Switch On Time	Current Limit Not Asserted	●	4	6	8	µs
Maximum Duty Cycle	Current Limit Not Asserted	●	76	80	88	%
Peak Switch Current	I_{LIM} Pin Open, V_{IN} = 5V 20k from I_{LIM} to GND		0.8	1 500	1.2	A mA
Switch Saturation Voltage	I_{SW} = 1A I_{SW} = 700mA	 ●		0.50 0.26	 0.35	V V
Switch Leakage	Switch Off, V_{SW} = 5V	●		0.01	7	µA

ELECTRICAL CHARACTERISTICS

V_{IN} = 2V, $V_{\overline{SHDN}}$ = 2V unless otherwise noted.

The ● denotes specifications which apply over the 0°C to 70°C operating temperature range.

PIN FUNCTIONS

LBI (Pin 1): Low-Battery Detector Input. When voltage on this pin is less than 1.17V, detector output is low.

LBO (Pin 2): Low-Battery Detector Output. Open collector can sink up to 500µA. Low-battery detector remains active when device is shut down.

V_{IN} (Pin 3): Input Supply. Must be bypassed with a large value capacitor close (<0.2") to the pin. See required layout in the Typical Applications.

SW (Pin 4): Collector of Power NPN. Keep copper traces on this pin short and direct to minimize RFI.

GND (Pin 5): Device Ground. Must be low impedance; solder directly to ground plane.

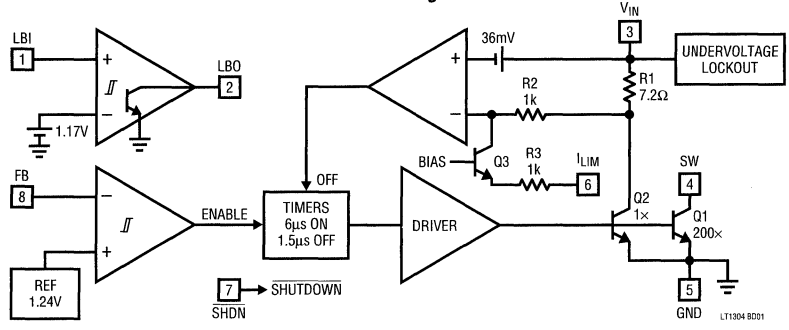
I_{LIM} (Pin 6): Current Limit Set Pin. Float for 1A peak switch current; a resistor to ground will lower peak current.

$\overline{SHDN}$ (Pin 7): Shutdown Input. When low, switching regulator is turned off. The low-battery detector remains active.

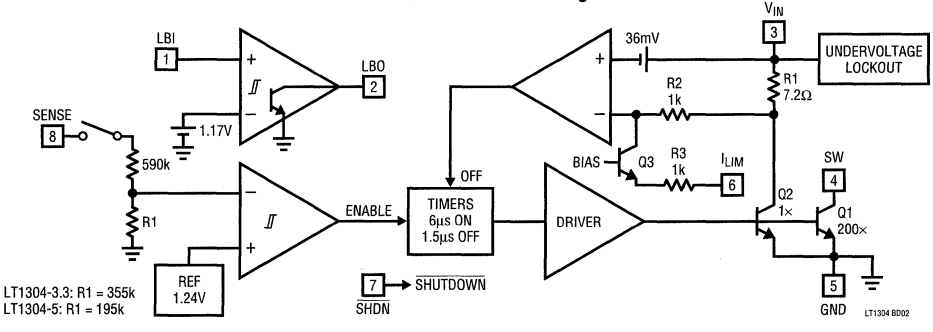
FB/SENSE (Pin 8): On the LT1304 (adjustable) this pin goes to the comparator input. On the fixed-output versions, the pin connects to the resistor divider which sets output voltage. The divider is disconnected from the pin during shutdown.

BLOCK DIAGRAMS

LT1304 Block Diagram

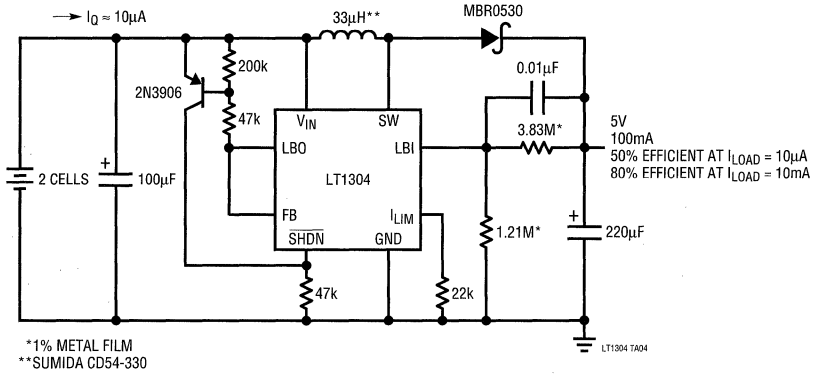


LT1304-3.3/LT1304-5 Block Diagram

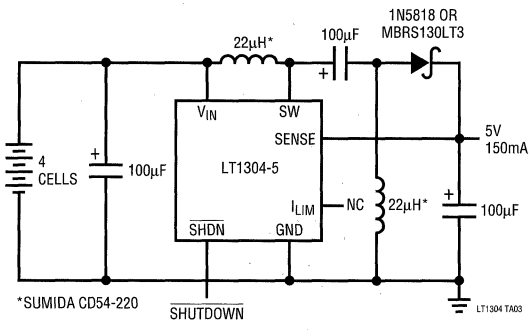


TYPICAL APPLICATIONS

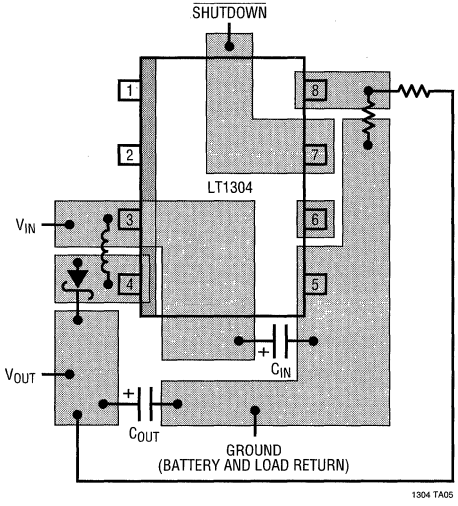
Ultra-Low I_Q 2-Cell Boost Converter



4-Cell to 5V Converter



Required Layout for Specified Performance. Input Capacitor Must be Placed as Shown



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1073	Single Cell, Micropower DC/DC Converter	95µA Quiescent Current, 1V Minimum Input
LT1121	150mA Low Dropout Regulator	45µA Quiescent Current, 400mV Dropout at Full Load
LTC®1174	Micropower Step-Down DC/DC Converter	Over 90% Efficiency at 5V/425mA Output
LT1301	Fixed 5V/12V Micropower DC/DC Converter	12V/200mA from 5V, 120µA I_Q, 88% Efficiency
LT1302	High Output Current Micropower DC/DC Converter	5V/600mA from 2V, 2A Internal Switch, 200µA I_Q

500kHz Micropower DC/DC Converter for Flash Memory

May 1995

FEATURES

- **60mA Output Current at 12V from 3V or 5V Supply**
- **Shutdown to 9µA**
- $\overline{\text{VPP VALID}}$ Comparator
- **Up to 85% Efficiency**
- Switching Frequency: 650kHz (Typical)
- Quiescent Current: 500µA
- Low V_{CESAT} Switch: 300mV at 0.5A (Typical)
- Soft Start Reduces Supply Current Transients
- Uses Low Value, Small Size, Surface Mount Inductors
- Available in 8-Lead SO Package

APPLICATIONS

- Flash Memory VPP Generators
- Type II and III PCMCIA Card DC/DC Converters
- 3V to 12V, 5V to 12V Converters
- Portable Computers and Instruments
- Cellular Telephones
- DC/DC Converter Module Replacements

DESCRIPTION

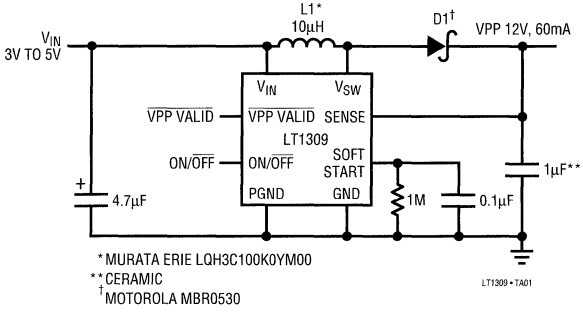
The LT®1309 is a 500kHz micropower DC/DC converter for Flash Memory. The regulator features Burst Mode™ operation with a 0.5A, 300mV switch, enabling 85% efficiency at the fixed 12V output. High frequency operation permits the use of small value, and therefore small size, surface mount inductors and capacitors. The LT1309 comes in an 8-lead SO package allowing extremely compact PC board layouts. These features make the device attractive for PCMCIA cards, cellular phones and other applications where PC board space is limited.

Quiescent current is 650µA decreasing to 9µA when the part shuts down. The device includes a Soft Start feature which limits supply current transients during turn-on.

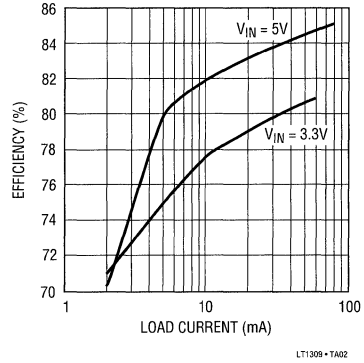
The LT1309 contains a $\overline{\text{VPP VALID}}$ comparator with a logic output that goes low when the output voltage is ready to program 12V Flash Memory. This comparator simplifies the interface to external control logic.

TYPICAL APPLICATION

12V, 60mA Flash Memory Programming Supply



12V Output Efficiency



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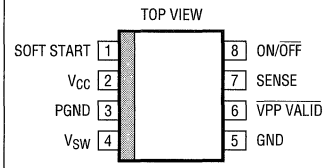
ABSOLUTE MAXIMUM RATINGS

V_{CC} Voltage 7V
V_{SW} Voltage 20V
V_{SENSE} Voltage 20V
$V_{ON/\overline{OFF}}$ Voltage 7V
V_{SEL} Voltage 7V
I_{LIM} Voltage 7V
Maximum Power Dissipation 500mW
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LT1309CS8
S8 PART MARKING
1309

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

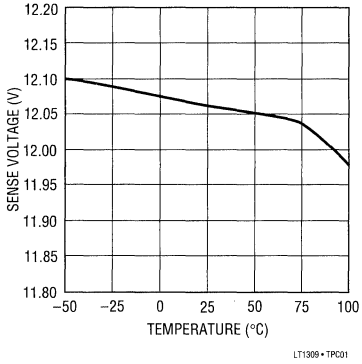
T_A = 25°C, V_{CC} = 5V, $V_{ON/\overline{OFF}}$ = 3V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_Q	Quiescent Current	V_{SENSE} = 12V			650	900	µA
	Quiescent Current, Shutdown	$V_{ON/\overline{OFF}}$ = 0.2V			9	15	µA
	Input Voltage Range			2		6	V
	Output Sense Voltage		●	11.5	12	12.6	V
	Output Referred Comparator Hysteresis				35		mV
f_{OSC}	Oscillator Frequency	Current Limit Not Asserted		400	500	700	kHz
DC	Maximum Duty Cycle		●	80	85	92	%
t_{ON}	Switch On Time				1.7		µs
	Reference Line Regulation	2V < V_{IN} < 6V			0.06	0.15	%/V
V_{CESAT}	Switch Saturation Voltage	I_{SW} = 0.5A			230	350	mV
	Switch Leakage Current	V_{SW} = 12V, Switch Off			0.1	10	µA
	Switch Current Limit	V_{IN} = 5V, Soft Start Floating V_{IN} = 3V, Soft Start Floating		450 500	600 650	900 950	mA mA
	Soft Start Current	Soft Start Grounded			80	120	µA
	ON/$\overline{OFF}$ Input Voltage Low					0.8	V
	ON/$\overline{OFF}$ Input Voltage High			1.6			V
	ON/$\overline{OFF}$ Bias Current	$V_{ON/\overline{OFF}}$ = 5V $V_{ON/\overline{OFF}}$ = 3V $V_{ON/\overline{OFF}}$ = 0V			16.0 8.0 0.1	24.0 14.0 1.0	µA µA µA
	Sense Pin Input Current	 $V_{ON/\overline{OFF}}$ = 0.2V			50.0 0.1	90 1	µA µA
	$\overline{VPP\ VALID}$ Threshold	V_{SENSE} Rising (High to Low Transition)	●	11.4		12	V
	$\overline{VPP\ VALID}$ Output Voltage Low	I_{SINK} = 100µA			0.13	0.3	V
	$\overline{VPP\ VALID}$ Output Voltage High	I_{SOURCE} = 2.5µA		4	4.5		V

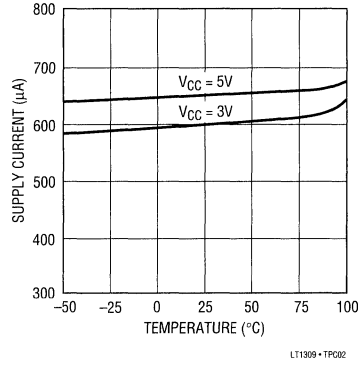
The ● denotes specifications which apply over the full operating temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

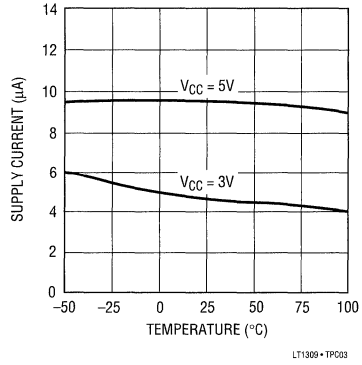
Sense Voltage



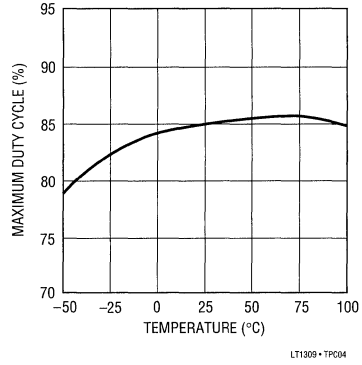
Supply Current



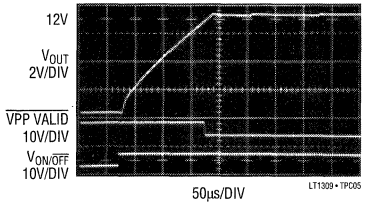
Supply Current In Shutdown



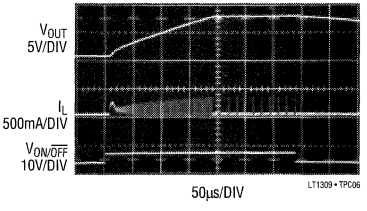
Maximum Duty Cycle



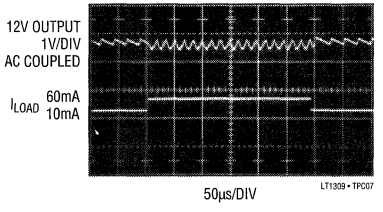
Start-Up Waveforms, I_{LOAD} = 1mA



Start-Up Waveforms, I_{LOAD} = 10mA



Load Transient Response, C_{OUT} = 1µF



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PIN FUNCTIONS

SOFT START (Pin 1): A 0.1µF/1MΩ parallel RC from this pin to GND provides a Soft Start function upon device turn-on. Initially about 80µA will flow from the pin into the capacitor. When the voltage at the pin reaches approximately 0.4V, current ceases flowing out of the pin.

V_{CC} (Pin 2): Input Supply. Both pins should be tied together. At least 1µF input bypass capacitance is required. More capacitance reduces ringing on the supply line.

PGND (Pin 3): Power Ground. Connect to ground plane.

V_{SW} (Pin 4): Collector of Power Switch. High dV/dt present on this pin. To minimize radiated noise keep layout short and direct.

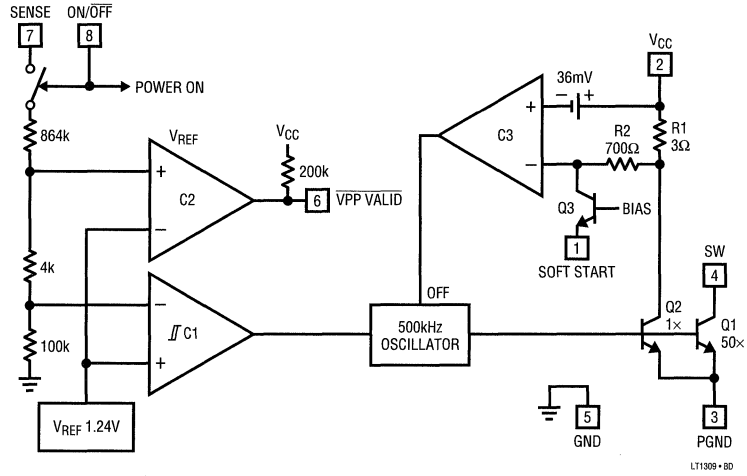
GND (Pin 5): Signal Ground. Connect to ground plane.

$\overline{\text{VPP VALID}}$ (Pin 6): This pin provides a logic signal indicating that output voltage is greater than 11.4V. Active low with internal 200k pull-up resistor.

SENSE (Pin 7): Output Sense Pin. This pin connects to a resistive divider that sets the output voltage. In shutdown, the resistor string is disconnected and current into this pin reduces to < 1µA.

ON/$\overline{\text{OFF}}$ (Pin 8): Shutdown Control. When pulled below 1.5V, this pin disables the LT1309 and reduces supply current to 9µA. All circuitry is disabled in shutdown. The part is enabled when ON/$\overline{\text{OFF}}$ is greater than 1.5V.

BLOCK DIAGRAM



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1106	Micropower Step-Up DC/DC Converter, 12V at 60mA	Thin TSSOP Package for Type I PCMCIA Card
LT1109-12	Micropower Step-Up DC/DC Converter, 12V at 60mA	Flash Memory VPP Generator, Adjustable Also
LT1109A-12	Micropower Step-Up DC/DC Converter, 12V at 120mA	VPP Generator, Adjustable Also
LTC®1262	Inductorless Flash Memory Programming Supply, 12V at 30mA	Switched Capacitor Converter, No Inductor
LT1303	Micropower High Efficiency DC/DC Converter with Low-Battery Detector	Adjustable and Fixed 5V, I_{OUT} up to 200mA

LTC1324

Single Supply LocalTalk® Transceiver

April 1995

FEATURES

- **Single Chip 5V LocalTalk Port**
- **Low Power: I_{CC} = 1mA Typ**
- Shutdown Pin Reduces I_{CC} to 1µA Typ
- **Digitally Selectable Low Slew Rate Mode for Reduced EMI Emmisions**
- ESD Protection to ±10kV on Receiver Inputs and Driver Outputs
- Drivers Maintain High Impedance in Three-State or with Power Off
- Thermal Shutdown Protection
- Drivers Are Short-Circuit Protected

APPLICATIONS

- LocalTalk Peripherals
- Notebook and Palmtop Computers
- Battery-Powered Systems

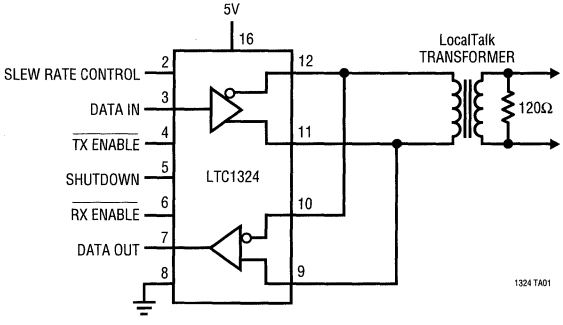
DESCRIPTION

The LTC®1324 is a single 5V line transceiver designed to operate on Apple®LocalTalk networks. The driver features a digitally selectable low slew rate mode for reduced EMI emissions. The chip draws only 1mA quiescent current when active and 1µA in shutdown. The differential driver outputs three-state when disabled, during shutdown or when the power is off. The driver outputs will maintain high impedance even with output common-mode voltages beyond the power supply rails. Both the driver outputs and receiver inputs are protected against ESD damage to ±10kV.

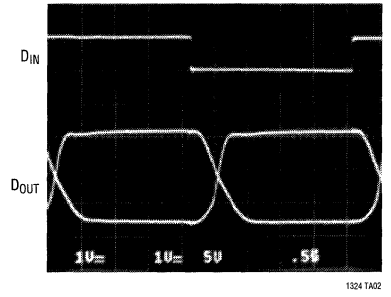
The LTC1324 is available in a 16-pin SO Wide package.

TYPICAL APPLICATION

Typical LocalTalk Connection for Low EMI



Waveform of Driver



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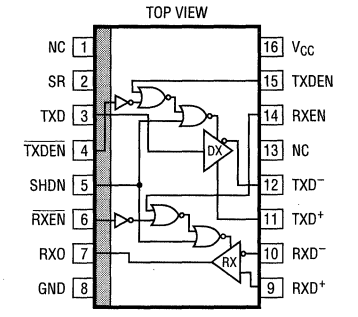
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 7V
Input Voltage (Logic Inputs) ..... −0.3V to (V_{CC} + 0.3V)
Input Voltage (Receiver Inputs) ..... ±15V
Driver Output Voltage (Forced) ..... ±15V
Driver Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
16-LEAD PDIP

SW PACKAGE
16-LEAD PLASTIC SO WIDE

T_{JMAX} = 150°C, θ_{JA} = 110°C/W (N)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S)

ORDER PART NUMBER
LTC1324CN
LTC1324CSW

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 0°C to 70°C (Notes 2, 3), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
I_{CC}	Normal Operation Supply Current Shutdown Supply Current	No Load, SHDN = 0V, $\overline{TXDEN}$ = 0V, $\overline{RXEN}$ = 0V No Load, SHDN = V_{CC}	● ●		1 1	2 10	mA µA
Differential Driver							
V_{OD}	Differential Output Voltage	No Load R_L = 50Ω (Figure 1)	● ●	±4.0 ±2.0			V V
ΔV_{OD}	Change in Magnitude of Differential Output Voltage	R_L = 50Ω (Figure 1)			0.2		V
V_{OC}	Differential Common-Mode Output Voltage	R_L = 50Ω (Figure 1)			3.0		V
I_{SS}	Short-Circuit Current	0V ≤ V_O ≤ 5V	●	35	120	250	mA
I_{OZ}	Three-State Output Current	($\overline{TXDEN}$ = V_{CC} and TXDEN = GND) or SHDN = V_{CC} or or Power Off, −10V ≤ V_O ≤ 10V	●		±2	±200	µA
Logic Inputs							
V_{IH}	Input High Voltage	All Logic Input Pins	●	2.4			V
V_{IL}	Input Low Voltage	All Logic Input Pins	●			0.8	V
I_{IN}	Input Current	SHDN, $\overline{TXDEN}$, $\overline{RXDEN}$, V_{IN} = 0V to V_{CC}	●		±1	±20	µA
I_{DN}	Pull-Down Current	RXDEN, TXDEN, SR, V_{IN} = 0V to V_{CC}	●		15	60	µA

ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, T_A = 0°C to 70°C (Notes 2, 3), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver							
R_{IN}	Input Resistance	$-7V \le V_{IN} \le 7V$		12			kΩ
	Receiver Threshold Voltage	$-7V \le V_{CM} \le 7V$	●	−200		200	mV
	Receiver Input Hysteresis	$-7V \le V_{CM} \le 7V$			70		mV
V_{OH}	Output High Voltage	$I_O = -4mA$	●	3.5			V
V_{OL}	Output Low Voltage	$I_O = 4mA$	●			0.4	V
I_{OS}	Output Short-Circuit Current	$0V \le V_O \le 5V$	●	7		85	mA
I_{OZ}	Output Three-State Current	$0V \le V_O \le 5V$, $\overline{RXEN} = V_{CC}$, RXEN = GND	●		±2	±100	µA
Switching Characteristics							
t_{PLH}, t_{PHL}	Driver Propagation Delay Without Slew Rate Control	$R_L = 100\Omega$, $C_L = 100\Omega$ (Figures 2, 4) SR = GND	●		40	120	ns
	Driver Propagation Delay with Slew Rate Control	$R_L = 100\Omega$, $C_L = 100pF$ (Figures 2, 4) SR = V_{CC}	●		0.4	1	µs
	Receiver Propagation Delay	C_L = 15pF (Figures 2, 6)	●		70	160	ns
t_{SKEW}	Driver Output to Output Without Slew Rate Control	$R_L = 100\Omega$, $C_L = 100pF$ (Figures 2, 4) SR = GND	●		10	50	ns
	Driver Output to Output with Slew Rate Control	$R_L = 100\Omega$, $C_L = 100pF$ (Figures 2, 4) SR = GND	●		25	100	ns
t_r, t_f	Driver Rise/Fall Time Without Slew Rate Control	$R_L = 100\Omega$, $C_L = 100pF$ (Figures 2,4) SR = GND	●		50	150	ns
	Driver Rise/Fall Time with Slew Rate Control	$R_L = 100\Omega$, $C_L = 100pF$ (Figures 2, 4) SR = V_{CC}	●		0.4	1	µs
t_{DHZ}, t_{DLZ}	Driver Output Active to Disable Without Slew Rate Control	C_L = 15pF (Figures 3, 5) SR = GND	●		50	150	ns
	Driver Output Active to Disable with Slew Rate Control	C_L = 15pF (Figures 3, 5) SR = V_{CC}	●		0.7	2	µs
	Receiver Output Active to Disable	C_L = 15pF (Figures 3, 7)	●		30	100	ns
t_{ZH}, t_{ZL}	Driver Enable to Output Active Without Slew Rate Control	C_L = 15pF (Figures 3, 5) SR = GND	●		50	150	ns
	Driver Enable to Output Active with Slew Rate Control	C_L = 15pF (Figures 3, 5) SR = V_{CC}	●		250	750	ns
	Receiver Enable to Output Active	C_L = 15pF (Figures 3, 7)	●		30	100	ns

e ● denotes specifications which apply over the full operating nperature range.

ite 1: Absolute maximum ratings are those values beyond which the life a device may be impaired.

Note 2: All currents into device pins are positive and all currents out of device pins are negative. All voltages are reference to ground unless otherwise specified.

Note 3: All typicals are given at V_{CC} = 5V, T_A = 25°C.

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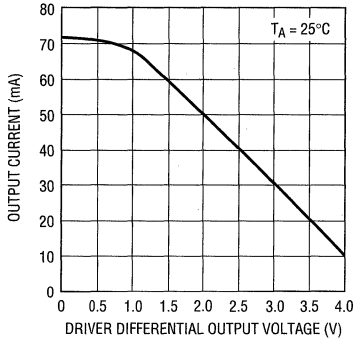
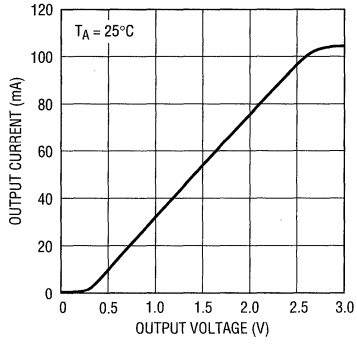
TYPICAL PERFORMANCE CHARACTERISTICS

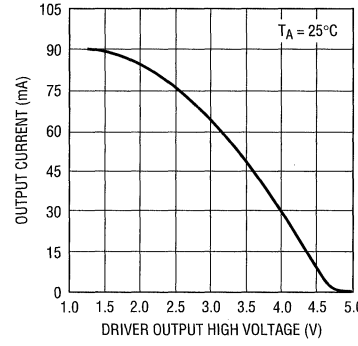
Driver Differential Output Voltage vs Output Current



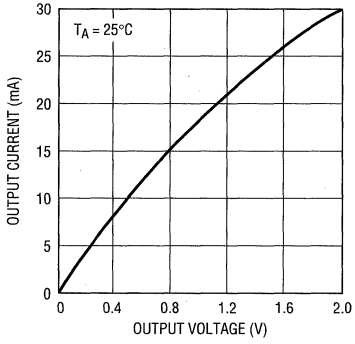
Driver Output Low Voltage vs Output Current



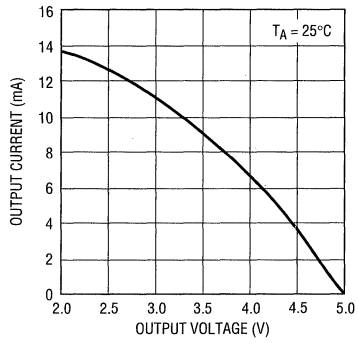
Driver Output High Voltage vs Output Current



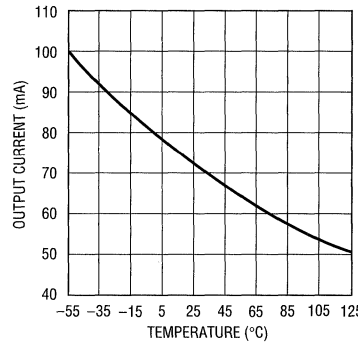
Receiver Output Low Voltage vs Output Current



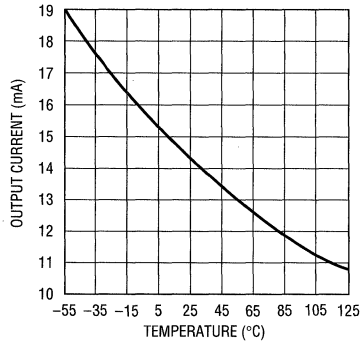
Receiver Output High Voltage vs Output Current



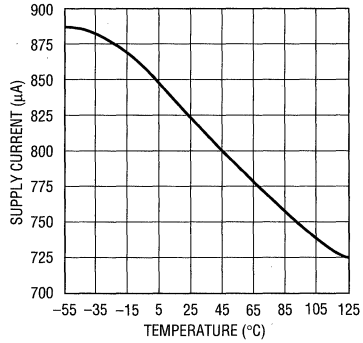
Driver Short-Circuit Current vs Temperature



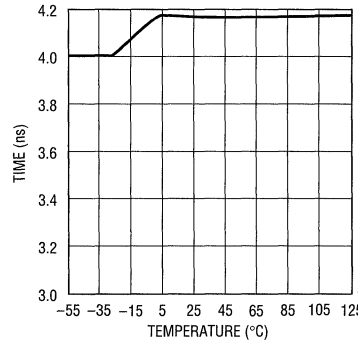
Receiver Short-Circuit Current vs Temperature



Supply Current (Driver and Receiver Enabled) vs Temperature

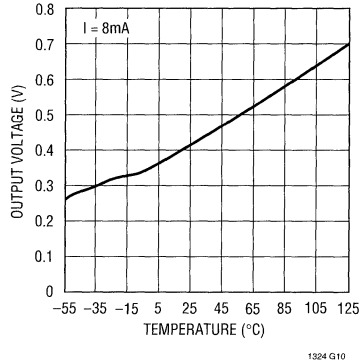


Driver Skew vs Temperature

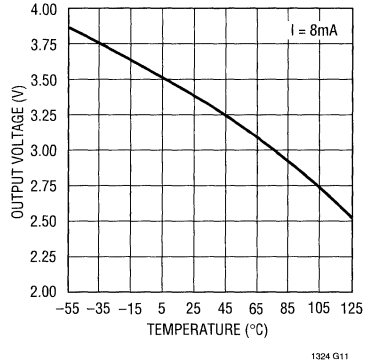


TYPICAL PERFORMANCE CHARACTERISTICS

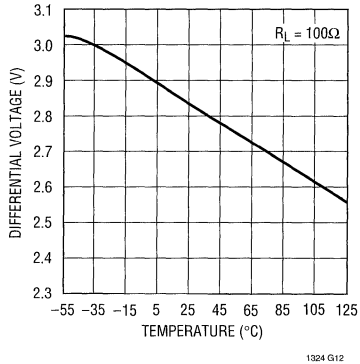
Receiver Output Low Voltage vs Temperature



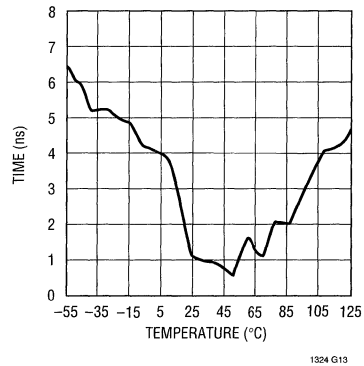
Receiver Output High Voltage vs Temperature



Driver Differential Output Voltage vs Temperature



Receiver $|t_{PLH} - t_{PHL}|$ vs Temperature



PIN FUNCTIONS

C (Pin 1, 13): No Internal Connection.

R (Pin 2): Slew Rate Control (TTL Compatible). A high vel on this pin forces the RS485 driver into the low slew ıte mode. A low level enables the driver into the high slew ıte or normal mode. Connected to an internal pull-down.

XD (Pin 3): RS485 Driver Input (TTL Compatible).

$\overline{\text{XDEN}}$ (Pin 4): Driver Output Enable (TTL Compatible). A gh level on this pin and a low level on TXDEN (pin 15) ırces the RS485 driver into three-state. A low level ıables the driver.

SHDN (Pin 5): Shutdown Input (TTL Compatible). When this pin is high, the chip is shut down; the driver and receiver outputs three-state; and the supply current drops to 1μA. A low level on this pin allows normal operation.

$\overline{\text{RXEN}}$ (Pin 6): Receiver Enable (TTL Compatible). A high level on this pin and a low level on RXEN (pin 14) disables the receiver and three-states the logic outputs. A low level allows normal operation.

RXDO (Pin 7): RS485 Receiver Output.

GND (Pin 8): Ground.

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PIN FUNCTIONS

RXD⁺ (Pin 9): RS485 Receiver Noninverting Input. When this pin is ≥ 200mV above RXD⁻, RXDO will be high. When this pin is ≥ 200mV below RXD⁻, RXDO will be low.

RXD⁻ (Pin 10): RS485 Receiver Inverting Input.

TXD⁺ (Pin 11): RS485 Driver Noninverting Output.

TXD⁻ (Pin 12): RS485 Driver Inverting Output.

RXEN (Pin 14): Receiver Enable (TTL Compatible). A low level on this pin and a high level on $\overline{RXEN}$ (pin 6) disables the receiver and three-states the logic outputs. A high level allows normal operation. Connected to an internal pull-down.

TXDEN (Pin 15): Driver Output Enable (TTL Compatible). A low level on this pin and a high level on $\overline{TXDEN}$ (pin 4) forces the RS485 driver into three-state. A high level enables the driver. Connected to an internal pull-down.

V_{CC} (Pin 16): The Positive Supply Input. 4.75V ≤ V_{CC} ≤ 5.25V. Requires a 1μF bypass capacitor to ground.

TEST CIRCUITS

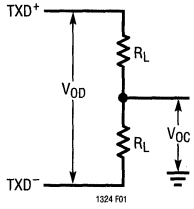

Figure 1.

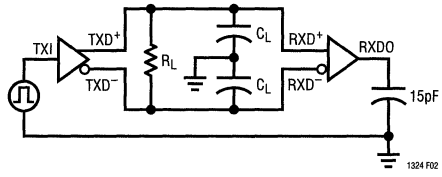

Figure 2.

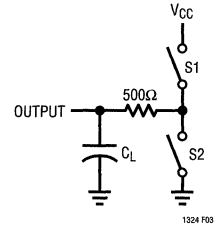

Figure 3.

SWITCHING WAVEFORMS

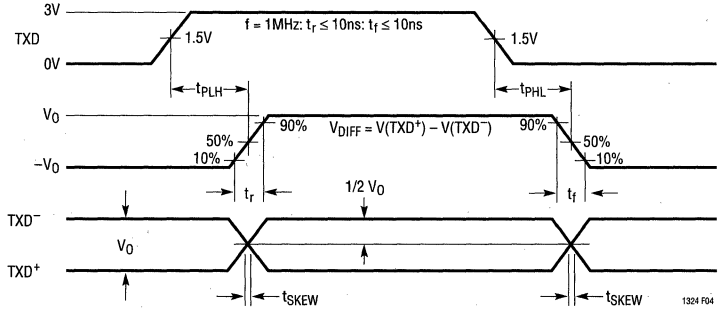

Figure 4. Differential Driver

SWITCHING WAVEFORMS

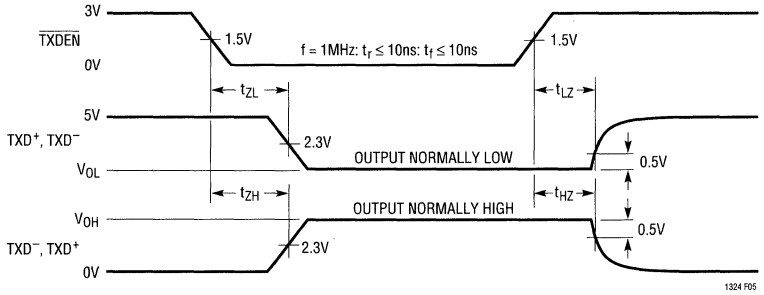

Figure 5. Differential Driver Enable and Disable

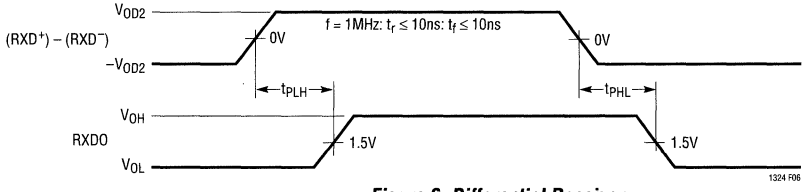

Figure 6. Differential Receiver

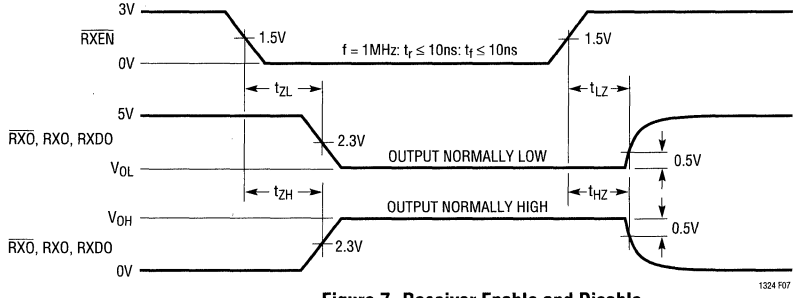

Figure 7. Receiver Enable and Disable

APPLICATIONS INFORMATION

Thermal Shutdown Protection

The LTC1324 includes a thermal shutdown circuit which protects against prolonged shorts at the driver outputs. If a driver output is shorted to another output or to the power supply, the current will be initially limited to a maximum of 250mA. When the die temperature rises above 150°C, the thermal shutdown circuit turns off the driver outputs. When the die cools to about 130°C, the outputs re-enable. If the short still exists, the part will heat again and the cycle will repeat. This oscillation occurs at about 10Hz and prevents the part from being damaged by excessive power dissipation. When the short is removed, the part will return to normal operation.

Power Shutdown

The power shutdown feature of the LTC1324 is designed for battery-powered systems. When SHDN is forced high, the part events shutdown mode. In shutdown, the supply current typically drops from 1mA to 1µA and the driver and receiver outputs are three-stated.

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APPLICATIONS INFORMATION

Supply Bypassing

The LTC1324 requires V_{CC} be bypassed to prevent data errors. A 1µF capacitor from V_{CC} to ground is adequate.

EMI Filters and Slew Rate Control

Most LocalTalk applications need to use an electromagnetic interference (EMI) filter consisting of a resistor-capacitor T network between each driver, receiver and the connector. Unfortunately, the resistors will attenuate the driver's output signal applied to the cable. Because the LTC1324 uses a single 5V supply, the resistors' values should be reduced from 22Ω which is normally used to 5.1Ω to insure enough voltage swing on the cable (Figure 8). Another way to get maximum swing and EMI immunity is to use a ferrite bead and capacitor as the T network (Figure 9). For data rates below 250kb/s, the LTC1324 features a low EMI mode which limits the rise time of the drivers to 400ns. With a lower rise time, the EMI network can be eliminated, allowing more signal voltage to reach the cable. Figures 10 and 11 show the output signals of the driver with different slew rates.

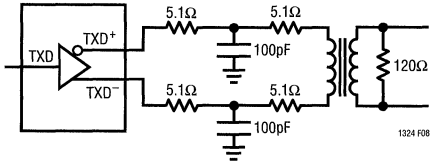


Figure 8.

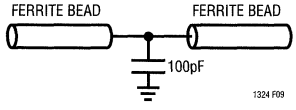


Figure 9.

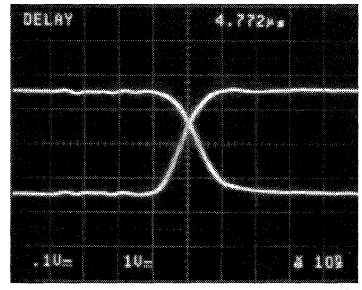


Figure 10. High Slew Rate Mode

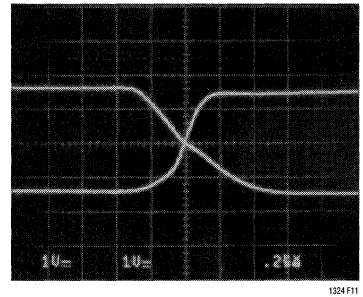


Figure 11. Low Slew Rate Mode

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1318	Single 5V Powered RS232/RS422 Transceiver	Pin Selectable RS232/RS422 Receiver. Available in 24-Pin SO Wide Package
LTC1320	RS422/RS562 Transceiver	Available in 18-Pin SO Wide Package
LTC1323	Single 5V Powered RS422/RS562 Transceiver	Available in 16-Pin and 24-Pin SO Wide Package

LTC1334

Single 5V RS232/RS485 Multi-Protocol Transceiver

June 1995

FEATURES

- **Four RS232 Transceivers or Two RS485 Transceivers on One Chip**
- **Operates from a Single 5V Supply**
- **Withstands Repeated ±10kV ESD Pulses**
- Uses Small Charge Pump Capacitors: 0.1µF
- Low Supply Current: 8mA Typical
- 10µA Supply Current in Shutdown
- 250kBaud in RS232 Mode
- 10MBaud in RS485/RS422 Mode
- Self-Testing Capability in Loopback Mode
- Power-Up/Down Glitch-Free Outputs
- Driver Maintains High Impedance in Three-State, Shutdown or with Power Off
- Thermal Shutdown Protection
- I/O Lines Can Withstand ±25V

APPLICATIONS

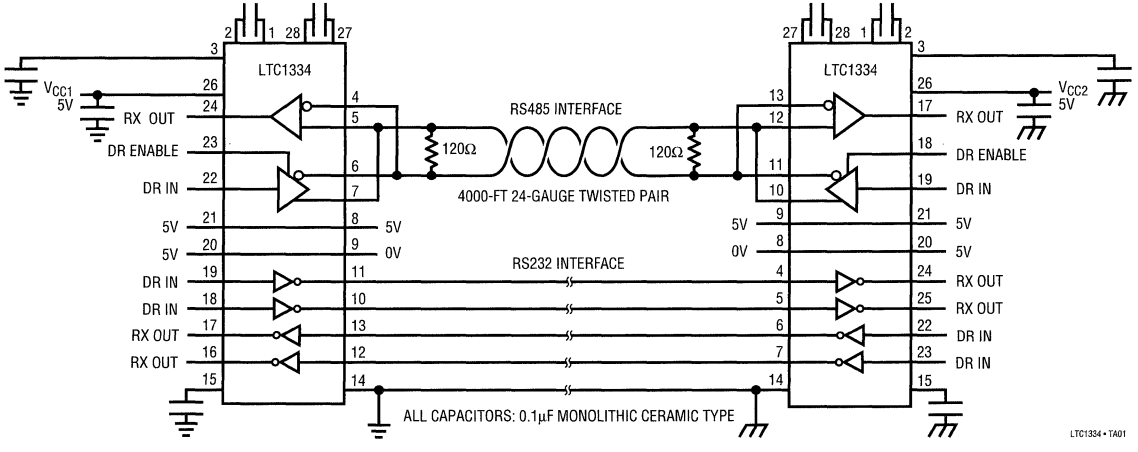
- Low Power RS485/RS422/RS232/EIA562 Interface
- Software-Selectable Multi-Protocol Interface Port
- Cable Repeaters
- Level Translators

DESCRIPTION

The LTC®1334 is a low power CMOS bidirectional transceiver featuring two reconfigurable interface ports. It can be configured as two RS485 differential ports, as two dual RS232 single-ended ports or as one RS485 differential port and one dual RS232 single-ended port. An onboard charge pump requires four 0.1µF capacitors to generate boosted positive and negative supplies, allowing the RS232 drivers to meet the RS232 ±5V output swing requirement with only a single 5V supply. A shutdown mode reduces the I_{CC} supply current to 10µA.

The RS232 transceivers operate to 250kbaud typical and are in full compliance with RS232 specifications. The RS485 transceivers operate to 10Mbaud and are in full compliance with RS485 and RS422 specifications. All interface drivers feature short-circuit and thermal shutdown protection. An enable pin allows RS485 driver outputs to be forced into high impedance, which is maintained even when the outputs are forced beyond supply rails or power is off. Both driver outputs and receiver inputs feature ±10kV ESD protection. A loopback mode allows the driver outputs to be connected back to the receiver inputs for diagnostic self-test.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 6.5V

Input Voltage

- Drivers ..... −0.3V to (V_{CC} + 0.3V)
- Receivers ..... −25V to 25V
- ON/$\overline{OFF}$, $\overline{LB}$, SEL1, SEL2 ..... −0.3V to (V_{CC} + 0.3V)

Output Voltage

- Drivers ..... −18V to 18V
- Receivers ..... −0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration

- Output ..... Indefinite
- V_{DD}, V_{EE}, $C1^+$, $C1^-$, $C2^+$, $C2^-$ ..... 30 sec

Operating Temperature Range

- Commercial ..... 0°C to 70°C

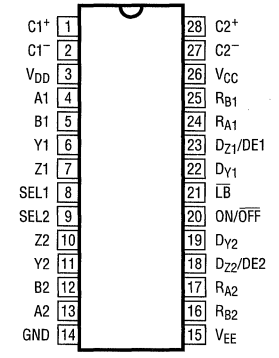
Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

TWO: RS485 TRANSCEIVERS
FOUR: RS232 TRANSCEIVERS

TOP VIEW



NW PACKAGE
28-LEAD PDIP WIDE

SW PACKAGE
28-LEAD PLASTIC SO WIDE

T_{JMAX} = 125°C, θ_{JA} = 56°C/W (NW)
T_{JMAX} = 125°C, θ_{JA} = 85°C/W (SW)

ORDER PART NUMBER
LTC1334CNW
LTC1334CSW

Consult factory for Industrial and Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS485 Driver (SEL1 = SEL2 = HIGH)							
V_{OD1}	Differential Driver Output Voltage (Unloaded)	I_O = 0	●			6	V
V_{OD2}	Differential Driver Output Voltage (With Load)	Figure 1, R = 50Ω (RS422) Figure 1, R = 27Ω (RS485)	● ●	2.0 1.5		6 6	V V
ΔV_{OD}	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	Figure 1, R = 27Ω or R = 50Ω	●			0.2	V
V_{OC}	Driver Common-Mode Output Voltage	Figure 1, R = 27Ω or R = 50Ω	●			3	V
$\Delta\lvert V_{OC}\rvert$	Change in Magnitude of Driver Common-Mode Output Voltage for Complementary Output States	Figure 1, R = 27Ω or R = 50Ω	●			0.2	V
I_{OSD}	Driver Short-Circuit Current	−7V ≤ V_O ≤ 12V, V_O = HIGH −7V ≤ V_O ≤ 12V, V_O = LOW (Note 4)	● ●	35 10		250 250	mA mA
I_{OZD}	Three-State Output Current (Y, Z)	−7V ≤ V_O ≤ 12V			±5		µA
RS232 Driver (SEL1 = SEL2 = LOW)							
V_O	Output Voltage Swing	Figure 4, R_L = 3k, Positive Figure 4, R_L = 3k, Negative	● ●	5 −5	6.5 −6.5		V V
I_{OSD}	Output Short-Circuit Current	V_O = 0V	●		±11	±60	mA
Driver Inputs and Control Inputs							
V_{IH}	Input High Voltage	D, DE, ON/$\overline{OFF}$, SEL1, SEL2, $\overline{LB}$	●	2			V
V_{IL}	Input Low Voltage	D, DE, ON/$\overline{OFF}$, SEL1, SEL2, $\overline{LB}$	●			0.8	V
I_{IN}	Input Current	D, SEL1, SEL2 DE, ON/$\overline{OFF}$, $\overline{LB}$	● ●		 −4	±10 −15	µA µA

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS485 Receiver (SEL1 = SEL2 = HIGH)							
V_{TH}	Differential Input Threshold Voltage	$-7V \le V_{CM} \le 12V$	●	−0.2		0.2	V
ΔV_{TH}	Input Hysteresis	V_{CM} = 0V			70		mV
I_{IN}	Input Current (A, B)	$-7V \le V_{IN} \le 12V$	●			±1	mA
R_{IN}	Input Resistance	$-7V \le V_{IN} \le 12V$	●	12	24		kΩ
RS232 Receiver (SEL1 = SEL2 = LOW)							
V_{TH}	Receiver Input Threshold Voltage	Input Low Threshold Input High Threshold	● ●	0.8		 2.4	V V
ΔV_{TH}	Receiver Input Hysteresis				0.6		V
R_{IN}	Receiver Input Resistance	V_{IN} = ±10		3	5	7	kΩ
Receiver Output							
V_{OH}	Receiver Output High Voltage	I_O = −3mA, V_{IN} = 0V, SEL1 = SEL2 = LOW	●	3.5	4.6		V
V_{OL}	Receiver Output Low Voltage	I_O = 3mA, V_{IN} = 3V, SEL1 = SEL2 = LOW	●		0.2	0.4	V
I_{OSR}	Short-Circuit Current	$0V \le V_O \le V_{CC}$	●	7		85	mA
I_{OZR}	Three-State Output Current	ON/$\overline{OFF}$ = 0V	●			±10	µA
R_{OB}	Inactive "B" Output Pull-Up Resistance (Note 5)	ON/$\overline{OFF}$ = HIGH, SEL1 = SEL2 = HIGH			50		kΩ
Power Supply Generator							
V_{DD}	V_{DD} Output Voltage	No Load, ON/$\overline{OFF}$ = HIGH I_{DD} = −10mA, ON/$\overline{OFF}$ = HIGH			8 6.5		V V
V_{EE}	V_{EE} Output Voltage	No Load, ON/$\overline{OFF}$ = HIGH I_{EE} = 10mA, ON/$\overline{OFF}$ = HIGH			−7.6 −6.5		V V
Power Supply							
I_{CC}	V_{CC} Supply Current	No Load, SEL1 = SEL2 = HIGH Shutdown, ON/$\overline{OFF}$ = 0V			8 10		mA µA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS232 Mode (SEL1 = SEL2 = LOW)							
BR_{MAX}	Maximum Data Rate (Note 6)	Figure 4, R_L = 3k, C_L = 51pF			250		kBaud
SR	Slew Rate	Figure 4, R_L = 3k, C_L = 51pF Figure 4, R_L = 3k, C_L = 1000pF	● ●	 4		30	V/µs V/µs
t_T	Transition Time	Figure 4, R_L = 3k, C_L = 2500pF			1.9		µs
t_{PLH}	Driver Input to Output	Figures 4, 9, R_L = 3k, C_L = 51pF			0.6		µs
t_{PHL}	Driver Input to Output	Figures 4, 9, R_L = 3k, C_L = 51pF			0.6		µs
t_{PLH}	Receiver Input to Output	Figures 5, 10			0.3		µs
t_{PHL}	Receiver Input to Output	Figures 5, 10			0.4		µs
RS485 Mode (SEL1 = SEL2 = HIGH)							
BR_{MAX}	Maximum Data Rate (Note 6)	Figures 2, 6, R_L = 54Ω, C_L = 100pF			15		MBaud
t_{PLH}	Driver Input to Output	Figures 2, 6, R_L = 54Ω, C_L = 100pF			40		ns
t_{PHL}	Driver Input to Output	Figures 2, 6, R_L = 54Ω, C_L = 100pF			40		ns
t_{SKEW}	Driver Output to Output	Figures 2, 6, R_L = 54Ω, C_L = 100pF			5		ns
t_r, t_f	Driver Rise and Fall Time	Figures 2, 6, R_L = 54Ω, C_L = 100pF			15		ns

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS485 Mode (SEL1 = SEL2 = HIGH)							
t_{ZL}	Driver Enable to Output Low	Figures 3, 7, C_L = 100pF, S1 Closed			50		ns
t_{ZH}	Driver Enable to Output High	Figures 3, 7, C_L = 100pF, S2 Closed			50		ns
t_{LZ}	Driver Disable from LOW	Figures 3, 7, C_L = 15pF, S1 Closed			50		ns
t_{HZ}	Driver Disable from HIGH	Figures 3, 7, C_L = 15pF, S2 Closed			60		ns
t_{PLH}	Receiver Input to Output	Figures 2, 8, R_L = 54Ω, C_L = 100pF			60		ns
t_{PHL}	Receiver Input to Output	Figures 2, 8, R_L = 54Ω, C_L = 100pF			70		ns
t_{SKEW}	Differential Receiver Skew, $\lvert t_{PLH} - t_{PHL} \rvert$	Figures 2, 8, R_L = 54Ω, C_L = 100pF			10		ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

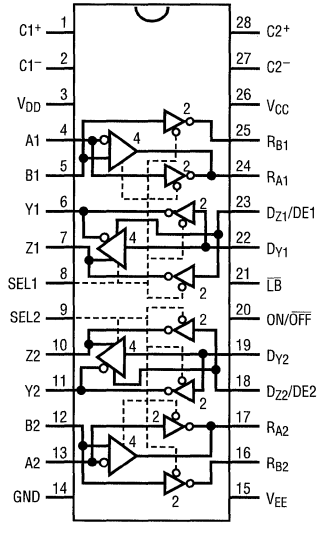
Note 3: All typicals are given at V_{CC} = 5V, C1 = C2 = C3 = C4 = 0.1µF and T_A = 25°C.

Note 4: Short-circuit current for RS485 driver output low state folds back above V_{CC}. Peak current occurs around V_O = 3V.

Note 5: The "B" RS232 receiver output is disabled in RS485 mode (SEL1 = SEL2 = HIGH). The unused output goes into a high impedance mode and has a resistor to V_{CC}. See Applications Information section for more details.

Note 6: The maximum data rate is specified for NRZ data encoding scheme. The maximum data rate may be different for other data encoding schemes. Data rate is guaranteed by correlation and is not tested.

PIN FUNCTIONS



$C1^+$ (Pin 1): Commutating Capacitor C1 Positive Terminal. Requires 0.1µF external capacitor between Pins 1 and 2.

$C1^-$ (Pin 2): Commutating Capacitor C1 Negative Terminal.

V_{DD} (Pin 3): Positive Supply Output for RS232 Drivers. Requires an external 0.1µF capacitor to ground.

A1 (Pin 4): Receiver Input.

B1 (Pin 5): Receiver Input.

Y1 (Pin 6): Driver Output.

Z1 (Pin 7): Driver Output.

SEL1 (Pin 8): Interface Mode Select Input.

SEL2 (Pin 9): Interface Mode Select Input.

Z2 (Pin 10): Driver Output.

Y2 (Pin 11): Driver Output.

B2 (Pin 12): Receiver Input.

A2 (Pin 13): Receiver Input.

GND (Pin 14): Ground.

V_{EE} (Pin 15): Negative Supply Output. Requires an external 0.1µF capacitor to ground.

R_{B2} (Pin 16): Receiver Output.

R_{A2} (Pin 17): Receiver Output.

D_{Z2}/DE2 (Pin 18): RS232 Driver Input in RS232 Mode. RS485 Driver Enable with internal pull-up in RS485 mode.

PIN FUNCTIONS

D_{Y2} (Pin 19): Driver Input.

ON/$\overline{OFF}$ (Pin 20): A HIGH logic input enables the transceivers. A LOW puts the device into shutdown mode and reduces I_{CC} to 10µA. This pin has an internal pull-up.

$\overline{LB}$ (Pin 21): Loopback Control Input. A LOW logic level enables internal loopback connections. This pin has an internal pull-up.

D_{Y1} (Pin 22): Driver Input.

D_{Z1}/DE1 (Pin 23): RS232 Driver Input in RS232 Mode. RS485 Driver Enable with internal pull-up in RS485 mode.

R_{A1} (Pin 24): Receiver Output.

R_{B1} (Pin 25): Receiver Output.

V_{CC} (Pin 26): Positive Supply; $4.75V \leq V_{CC} \leq 5.25V$

$C2^-$ (Pin 27): Commutating Capacitor C2 Negative Terminal. Requires 0.1µF external capacitor between Pins 27 and 28.

$C2^+$ (Pin 28): Commutating Capacitor C2 Positive Terminal.

FUNCTION TABLES

RS485 Driver Mode

INPUTS					OUTPUTS	
ON/$\overline{OFF}$	SEL	DE	D	CONDITIONS	Z	Y
1	1	1	0	No Fault	0	1
1	1	1	1	No Fault	1	0
1	1	1	X	Thermal Fault	Z	Z
1	1	0	X	X	Z	Z
0	1	X	X	X	Z	Z

RS232 Driver Mode

INPUTS				OUTPUTS
ON/$\overline{OFF}$	SEL	D	CONDITIONS	Y, Z
1	0	0	No Fault	1
1	0	1	No Fault	0
1	0	X	Thermal Fault	Z
0	0	X	X	Z

RS485 Receiver Mode

INPUTS			OUTPUTS	
ON/$\overline{OFF}$	SEL	B – A	R_A	R_B*
1	1	< –0.2V	0	1
1	1	> 0.2V	1	1
1	1	Inputs Open	1	1
0	1	X	Z	Z

*See Note 5

RS232 Receiver Mode

INPUTS			OUTPUTS
ON/$\overline{OFF}$	SEL	A, B	R_A, R_B
1	0	0	1
1	0	1	0
1	0	Inputs Open	1
0	0	X	Z

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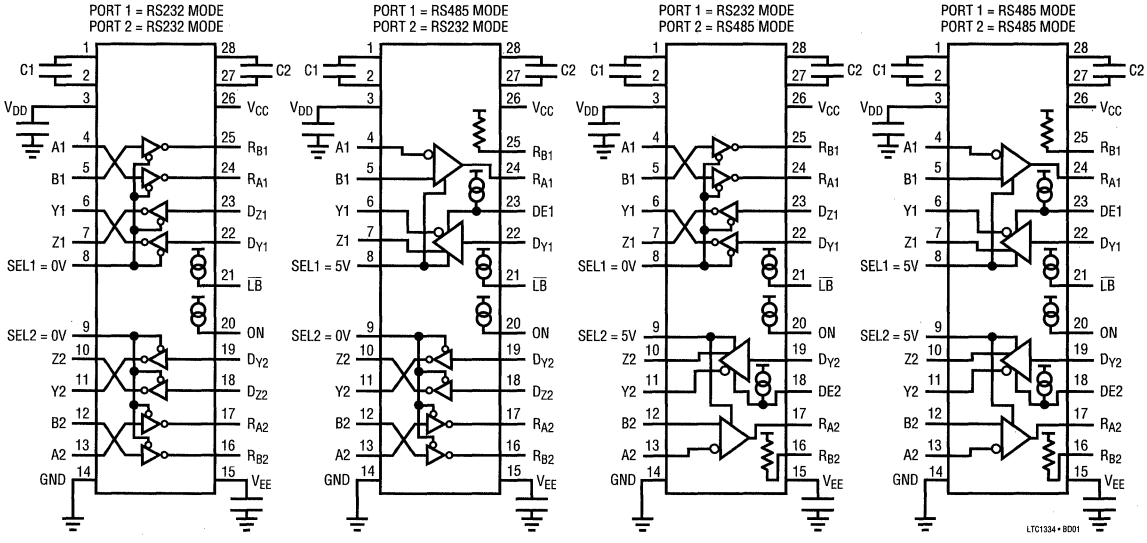
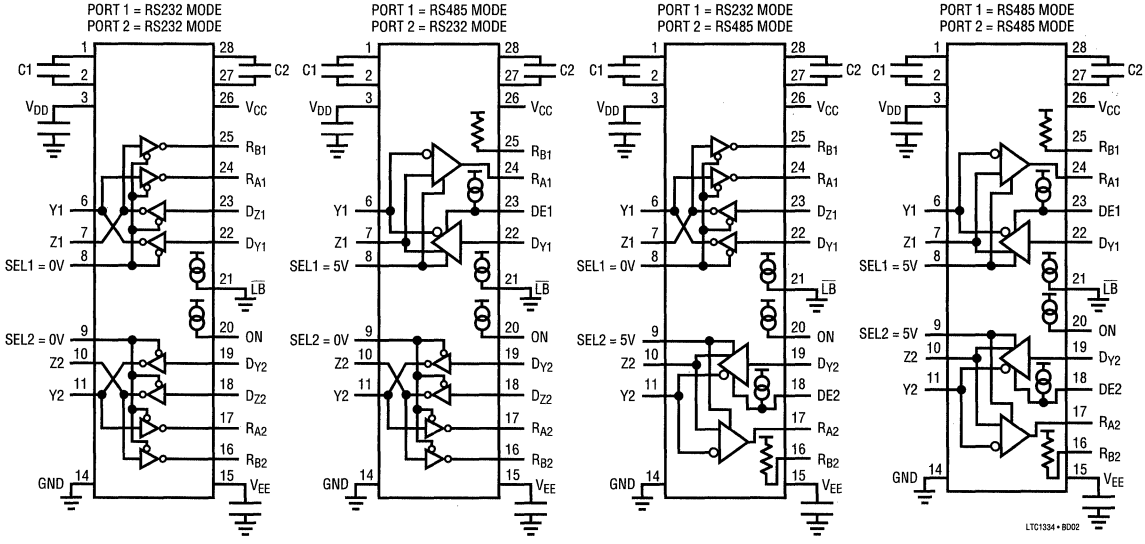
BLOCK DIAGRAMS

Interface Configuration with Loopback Disabled



Interface Configuration with Loopback Enabled



TEST CIRCUITS

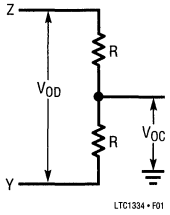


Figure 1. RS485 Driver Test Load

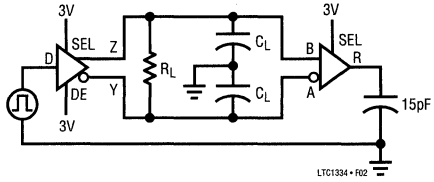


Figure 2. RS485 Driver/Receiver Timing Test Circuit

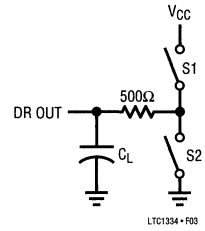


Figure 3. RS485 Driver Output Enable/Disable Timing Test Load

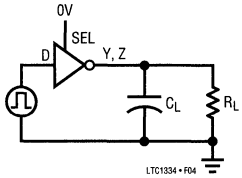


Figure 4. RS232 Driver Timing Test Circuit

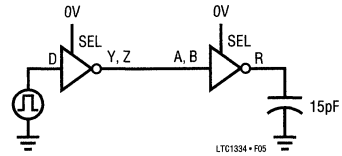


Figure 5. RS232 Receiver Timing Test Circuit

SWITCHING WAVEFORMS

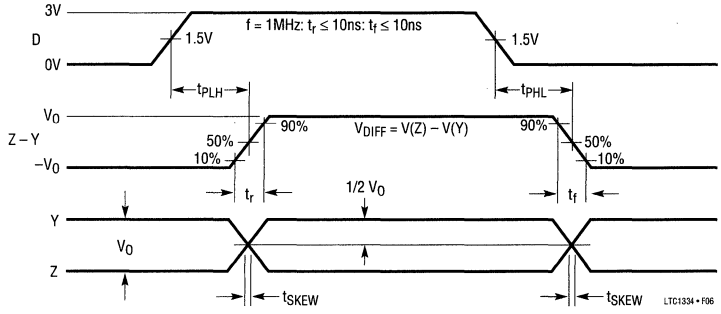


Figure 6. RS485 Driver Propagation Delays

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SWITCHING WAVEFORMS

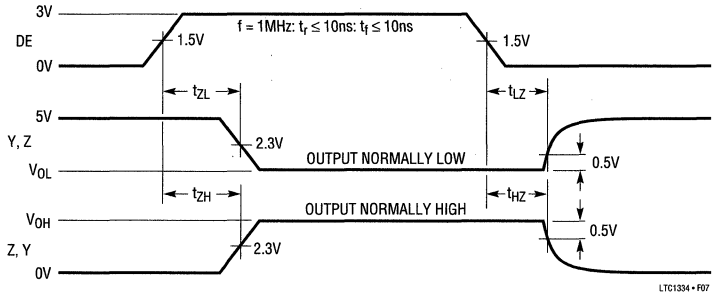

Figure 7. RS485 Driver Enable and Disable Times

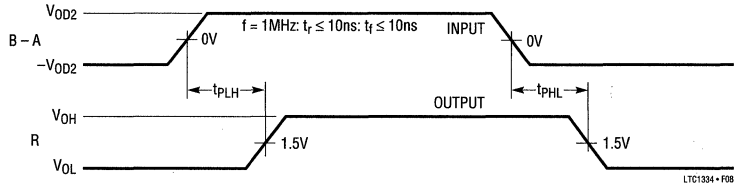

Figure 8. RS485 Receiver Propagation Delays

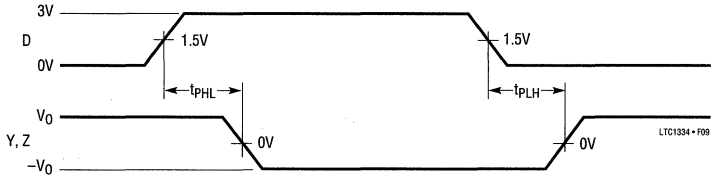

Figure 9. RS232 Driver Propagation Delays

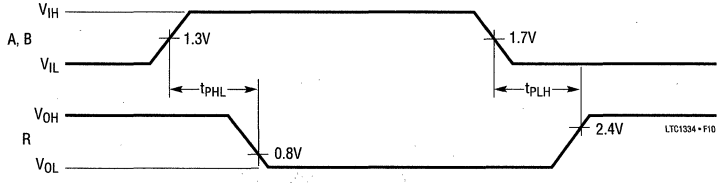

Figure 10. RS232 Receiver Propagation Delays

APPLICATIONS INFORMATION

Basic Theory of Operation

The LTC1334 has two interface ports. Each port may be configured as a pair of single-ended RS232 transceivers or as a differential RS485 transceiver by forcing the port's selection input to a LOW or HIGH, respectively. The LTC1334 provides two RS232 drivers and two RS232 receivers or one RS485 driver and one RS485 receiver per port. All the interface drivers feature three-state outputs. Interface outputs are forced into high impedance when the driver is disabled in the shutdown mode or with the power off.

All the interface driver outputs are fault-protected by a current limiting and thermal shutdown circuit. The thermal shutdown circuit disables both the RS232 and RS485 driver outputs when the die temperature reaches 150°C. The thermal shutdown circuit re-enables the drivers when the die temperature cools to 130°C.

In RS485 mode, Shutdown mode or with the power off, the input resistance of the receiver is 24k. The input resistance drops to 5k in RS232 mode.

A logic LOW at the ON/$\overline{OFF}$ pin shuts down the device and forces all the outputs into a high impedance state. A logic HIGH enables the device. An internal 4µA current source to V_{CC} pulls the ON/$\overline{OFF}$ pin HIGH if it is left open.

In RS485 mode, an internal 4µA current source pulls the driver enable pin HIGH if left open. The RS485 receiver has a 4µA current source at the noninverting input. If both the RS485 receiver inputs are open, the output goes to a high state. Both the current sources are disabled in the RS232 mode. The receiver output B is inactive in RS485 mode and has a 50k pull-up resistor to provide a known output state in this mode.

A loopback mode enables internal connections from driver outputs to receiver inputs for self-test when the $\overline{LB}$ pin has a LOW logic state. The driver outputs are not isolated from the external loads. This allows transmitter verification under the loaded condition. An internal 4µA current source pulls the $\overline{LB}$ pin HIGH if left open and disables the loopback configuration.

RS232/RS485 Applications

The LTC1334 can support both RS232 and RS485 levels with a single 5V supply as shown in Figure 11.

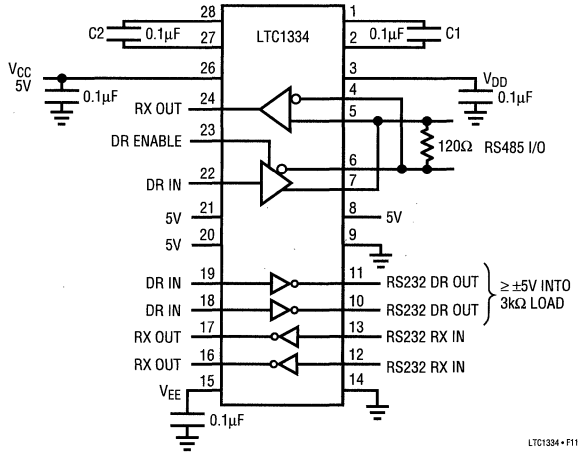

Figure 11. RS232/RS485 Interfaces

APPLICATIONS INFORMATION

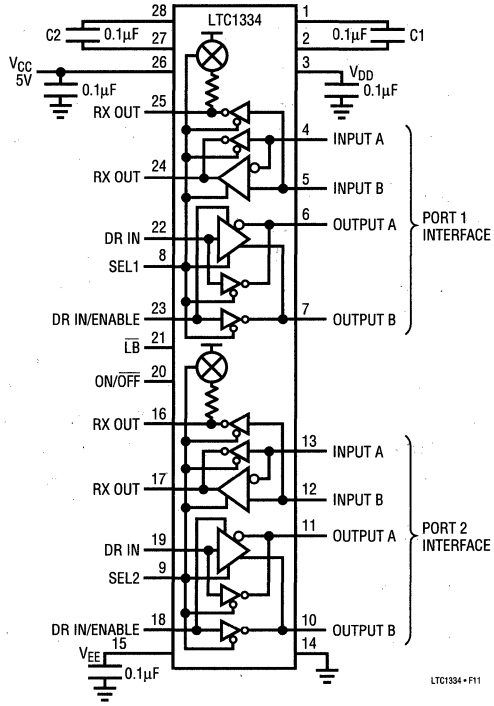

Figure 12. Multi-Protocol Interface

Multi-Protocol Applications

The LTC1334 is well-suited for software controlled interface mode selection. Each port has a selection pin as shown in Figure 12. The single-ended transceivers support both RS232 and EIA562 levels. The differential transceivers support both RS485 and RS422.

Typical Applications

A typical RS232/EIA562 interface application is shown in Figure 13 with the LTC1334.

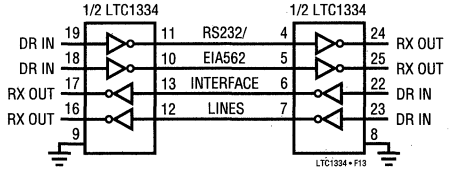

Figure 13. Typical Connection for RS232/EIA562 Interface

A typical connection for a RS485 transceiver is shown in Figure 14. A twisted pair of wires connects up to 32 drivers and receivers for half duplex multipoint data transmission. The wires must be terminated at both ends with resistors equal to the wire's characteristic impedance. An optional shield around the twisted pair helps to reduce unwanted noise and should be connected to ground at only one end.

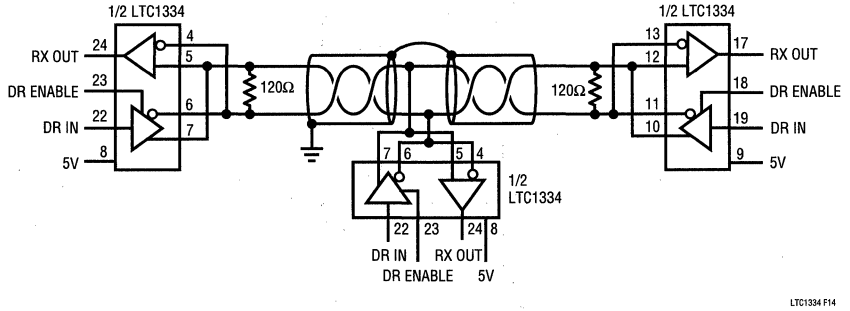

Figure 14. Typical Connection for RS485 Interface

APPLICATIONS INFORMATION

A typical RS422 connection (Figure 15) allows one driver and ten receivers on a twisted pair of wires terminated with a 100Ω resistor at one end.

A typical twisted-pair line repeater is shown in Figure 16. As data transmission rate drops with increased cable length, repeaters can be inserted to improve transmission rate or to transmit beyond the RS422 4000-foot limit.

The LTC1334 can be used to translate RS232 to RS422 interface levels or vice versa as shown in Figure 17. One port is configured as an RS232 transceiver and the other as an RS485 transceiver.

Using two LTC1334s as level translators, the RS232/EIA562 interface distance can be extended to 4000 feet with twisted-pair wires (Figure 18).

AppleTalk®/LocalTalk® Applications

An AppleTalk application is shown in Figure 19 with the LTC1323 and the LTC1334.

AppleTalk and LocalTalk are registered trademarks of Apple Computer, Inc.

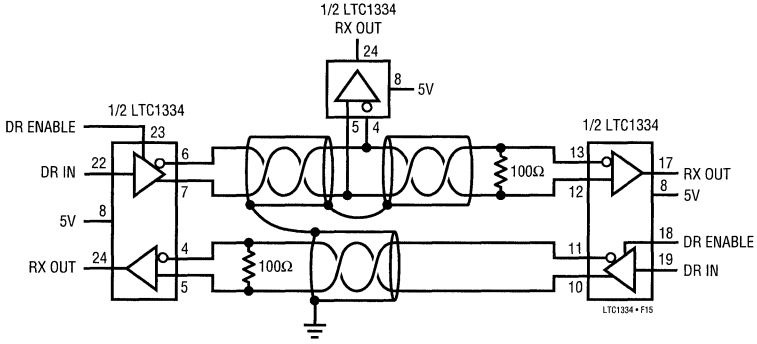

Figure 15. Typical Connection for RS422 Interface

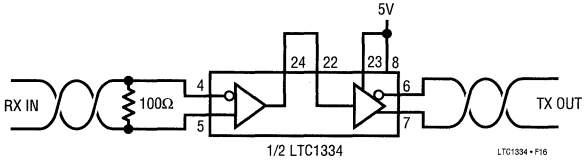

Figure 16. Typical Cable Repeater for RS422 Interface

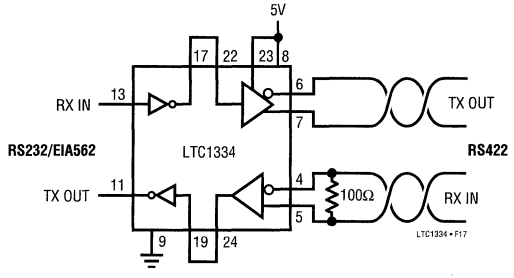

Figure 17. Typical RS232/EIA562 to RS422 Level Translator

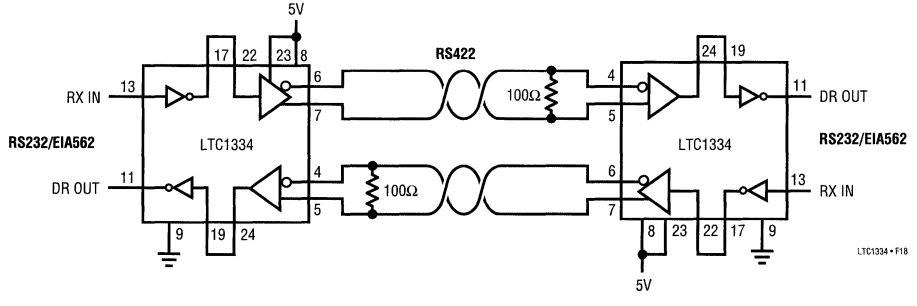

Figure 18. Typical Cable Extension for RS232/EIA562 Interface

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APPLICATIONS INFORMATION

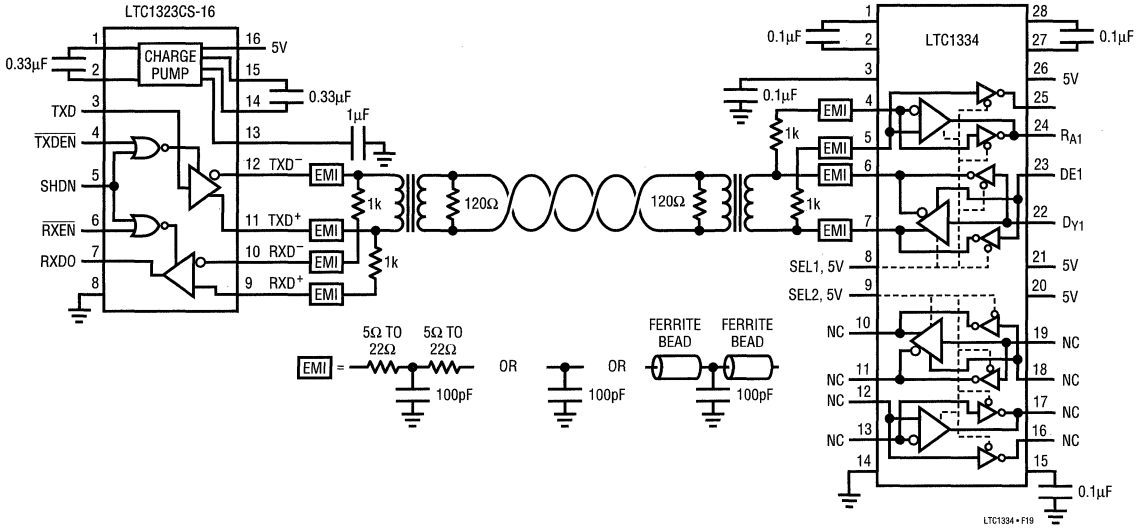


Figure 19. AppleTalk/LocalTalk Implemented Using the LTC1323CS-16 and LTC1334 Transceivers

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC485	Low Power RS485 Interface Transceiver	Single 5V Supply, Wide Common-Mode Range
LT®1137A	Low Power RS232 Transceiver	±15kV IEC-801 ESD Protection, Three Drivers, Five Receivers
LTC1320	AppleTalk Transceiver	AppleTalk/Local Talk Compliant
LTC1321/LTC1322/LTC1335	RS232/EIA562/RS485 Transceivers	Configurable, 10kV ESD Protection
LTC1323	Single 5V AppleTalk Transceiver	LocalTalk/AppleTalk Compliant 10kV ESD
LTC1347	5V Low Power RS232	Three Drivers/Five Receivers, Five Receivers Alive in Shutdown

10Mbps DCE/DTE V.35 Transceiver

June 1995

FEATURES

- **Single Chip Provides Complete Differential Signal Interface for V.35 Port**
- **Drivers and Receivers Will Withstand Repeated ±10kV ESD Pulses**
- 10MBaud Transmission Rate
- Meets CCITT V.35 Specification
- **Operates from ±5V Supplies**
- Shutdown Mode Reduces I_{CC} to Below 1µA
- Selectable Transmitter and Receiver Configurations
- Transmitter Maintains High Impedance When Disabled, Shutdown or with Power Off
- Transmitters Are Short-Circuit Protected

APPLICATIONS

- Modems
- Telecommunications
- Data Routers

DESCRIPTION

The LTC®1346 is a single chip transceiver that provides the differential clock and data signals for a V.35 interface from ±5V supplies. Combined with an external resistor termination network and an LT®1134A RS232 transceiver for the control signals, the LTC1346 forms a complete low power DTE or DCE V.35 interface port.

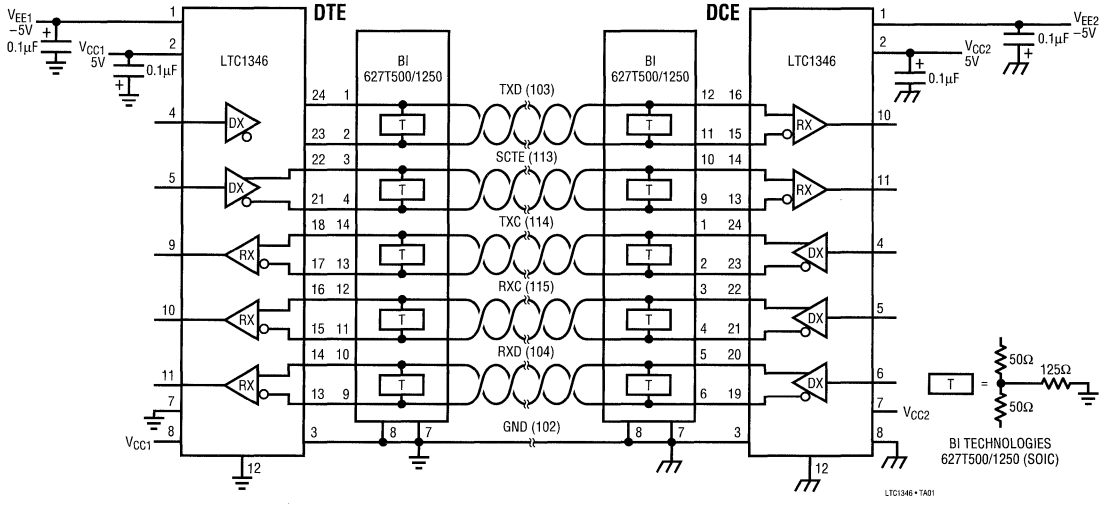
The LTC1346 features three current output differential transmitters and three differential receivers. The transceiver can be configured for DTE or DCE operation or Shutdown using two Select pins. In the Shutdown mode, the supply current is reduced to below 1µA.

The LTC1346 transceiver operates up to 10MBaud. All transmitters feature short-circuit protection and a Receiver Output Enable pin that allows the receiver outputs to be forced into a high impedance state. Both transmitter outputs and receiver inputs feature ±10kV ESD protection.

For single 5V applications that do not have –5V available, the LTC1345 provides the same functionality as the LTC1346 and includes an on-board –5V generator.

TYPICAL APPLICATION

Clock and Data Signals for V.35 Interface



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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} 6.5V
- V_{EE} ..... −6.5V

Input Voltage
- Transmitters ..... −0.3V to (V_{CC} + 0.3V)
- Receivers ..... −18V to 18V
- S1, S2, $\overline{OE}$ ..... −0.3V to (V_{CC} + 0.3V)

Output Voltage
- Transmitters ..... −18V to 18V
- Receivers ..... −0.3V to (V_{CC} + 0.3V)

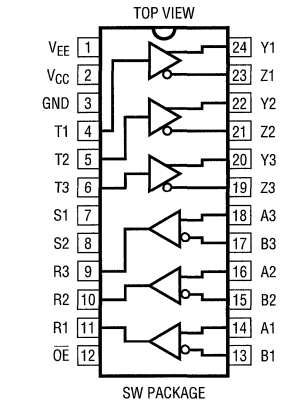
Short-Circuit Duration
- Transmitter Output ..... Indefinite
- Receiver Output ..... Indefinite

Operating Temperature Range
- Commercial ..... 0°C to 70°C
- Industrial ..... −40°C to 85°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



SW PACKAGE
24-LEAD PLASTIC SO WIDE

THREE V.35 TRANSMITTERS AND THREE RECEIVERS

T_{JMAX} = 150°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LTC1346CSW
LTC1346ISW

Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5%, V_{EE} = −5V ±5% (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OD}	Transmitter Differential Output Voltage	−4V ≤ V_{OS} ≤ 4V (Figure 1)	●	0.44	0.55	0.66	V
V_{OC}	Transmitter Common-Mode Output Voltage	V_{OS} = 0V (Figure 1)	●	−0.6	0	0.6	V
I_{OH}	Transmitter Output High Current	$V_{Y, Z}$ = 0V	●	−12.6	−11	−9.4	mA
I_{OL}	Transmitter Output Low Current	$V_{Y, Z}$ = 0V	●	9.4	11	12.6	mA
I_{OZ}	Transmitter Output Leakage Current	−5V ≤ $V_{Y, Z}$ ≤ 5V, S1 = S2 = 0V	 ●			±20 ±1	µA µA
R_O	Transmitter Output Impedance	−2V ≤ $V_{Y, Z}$ ≤ 2V			100		kΩ
V_{TH}	Differential Receiver Input Threshold Voltage	−7V ≤ (V_A + V_B)/2 ≤ 7V	●		25	200	mV
ΔV_{TH}	Receiver Input Hysterisis	−7V ≤ (V_A + V_B)/2 ≤ 7V			50		mV
I_{IN}	Receiver Input Current (A, B)	−7V ≤ $V_{A, B}$ ≤ 7V	●			0.4	mA
R_{IN}	Receiver Input Impedance	−7V ≤ $V_{A, B}$ ≤ 7V	●	17.5	30		kΩ
V_{OH}	Receiver Output High Voltage	I_O = 4mA, $V_{A, B}$ = 0.2V	●	3	4.5		V
V_{OL}	Receiver Output Low Voltage	I_O = 4mA, $V_{A, B}$ = −0.2V	●		0.2	0.4	V
I_{OSR}	Receiver Output Short-Circuit Current	0V ≤ V_O ≤ V_{CC}	●	7	40	85	mA
I_{OZR}	Receiver Three-State Output Current	$\overline{OE}$ = V_{CC}, 0V ≤ V_O ≤ V_{CC}	●			±10	µA
V_{IH}	Logic Input High Voltage	T, S1, S2, $\overline{OE}$	●	2			V
V_{IL}	Logic Input Low Voltage	T, S1, S2, $\overline{OE}$	●			0.8	V
I_{IN}	Logic Input Current	T, S1, S2, $\overline{OE}$	●			±10	µA
I_{CC}	V_{CC} Supply Current	V_{OS} = 0V, S1 = S2 = HIGH (Figure 1) No Load, S1 = S2 = HIGH Shutdown, S1 = S2 = 0V, $\overline{OE}$ = V_{CC}			40 6 0.1		mA mA µA
I_{EE}	V_{EE} Supply Current	V_{OS} = 0V, S1 = S2 = HIGH (Figure 1) No Load, S1 = S2 = HIGH Shutdown, S1 = S2 = 0V, $\overline{OE}$ = V_{CC}			−40 −6 −0.1		mA mA µA

AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V ±5%, V_{EE} = −5V ±5% (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_R, t_F	Transmitter Rise or Fall Time	V_{OS} = 0V (Figures 1, 3)	●		7	40	ns
t_{PLH}	Transmitter Input to Output ↑	V_{OS} = 0V (Figures 1, 3)	●		25	70	ns
t_{PHL}	Transmitter Input to Output ↓	V_{OS} = 0V (Figures 1, 3)	●		30	70	ns
t_{SKEW}	Transmitter Output to Output	V_{OS} = 0V (Figures 1, 3)			5		ns
t_{PLH}	Receiver Input to Output ↑	V_{OS} = 0V (Figures 1, 4)	●		60	100	ns
t_{PHL}	Receiver Input to Output ↓	V_{OS} = 0V (Figures 1, 4)	●		65	100	ns
t_{SKEW}	Differential Receiver Skew, $\lvert t_{PLH} - t_{PHL} \rvert$	V_{OS} = 0V (Figures 1, 4)			5		ns
t_{ZL}	Receiver Enable to Output LOW	C_L = 15pF, SW1 Closed (Figures 2, 5)	●		40	70	ns
t_{ZH}	Receiver Enable to Output HIGH	C_L = 15pF, SW2 Closed (Figures 2, 5)	●		35	70	ns
t_{LZ}	Receiver Disable From LOW	C_L = 15pF, SW1 Closed (Figures 2, 5)	●		30	70	ns
t_{HZ}	Receiver Disable From HIGH	C_L = 15pF, SW2 Closed (Figures 2, 5)	●		35	70	ns
BR_{MAX}	Maximum Data Rate (Note 3)		●	10	15		MBaud

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed.

Note 2: All currents into device pins are termed positive; all currents out of device pins are termed negative. All voltages are referenced to device ground unless otherwise specified.

Note 3: Maximum data rate is specified for NRZ data encoding scheme. The maximum data rate may be different for other data encoding schemes. Data rate is guaranteed by a propagation delay test.

PIN FUNCTIONS

V_{EE} (Pin 1): Negative Supply, $-4.75V \geq V_{EE} \geq -5.25V$.

V_{CC} (Pin 2): Positive Supply, $4.75V \leq V_{CC} \leq 5.25V$.

GND (Pin 3): Ground.

T1 (Pin 4): Transmitter 1 Input.

T2 (Pin 5): Transmitter 2 Input.

T3 (Pin 6): Transmitter 3 Input.

S1 (Pin 7): Select Input 1.

S2 (Pin 8): Select Input 2.

R3 (Pin 9): Receiver 3 Output.

R2 (Pin 10): Receiver 2 Output.

R1 (Pin 11): Receiver 1 Output.

$\overline{OE}$ (Pin 12): Receiver Output Enable. To ensure shutdown mode, both S1 and S2 should be LOW and $\overline{OE}$ should be HIGH.

B1 (Pin 13): Receiver 1 Inverting Input.

A1 (Pin 14): Receiver 1 Noninverting Input.

B2 (Pin 15): Receiver 2 Inverting Input.

A2 (Pin 16): Receiver 2 Noninverting Input.

B3 (Pin 17): Receiver 3 Inverting Input.

A3 (Pin 18): Receiver 3 Noninverting Input.

Z3 (Pin 19): Transmitter 3 Inverting Output.

Y3 (Pin 20): Transmitter 3 Noninverting Output.

Z2 (Pin 21): Transmitter 2 Inverting Output.

Y2 (Pin 22): Transmitter 2 Noninverting Output

Z1 (Pin 23): Transmitter 1 Inverting Output.

Y1 (Pin 24): Transmitter 1 Noninverting Output.

FUNCTION TABLES

Transmitter and Receiver Configuration

S1	S2	TX#	RX#	REMARKS
0	0	—	—	All Shut Down*
1	0	1, 2, 3	1, 2	DCE Mode, RX3 Shut Down
0	1	1, 2	1, 2, 3	DTE Mode, TX3 Shut Down
1	1	1, 2, 3	1, 2, 3	All Active

Transmitter

	INPUTS				OUTPUTS			
CONFIGURATION	S1	S2	$\overline{OE}$	T	Y1 AND Y2	Z1 AND Z2	Y3	Z3
DTE	0	1	X	0	0	1	Z	Z
DTE	0	1	X	1	1	0	Z	Z
DCE or All ON	1	X	X	0	0	1	0	1
DCE or All ON	1	X	X	1	1	0	1	0
Shutdown*	0	0	1	X	Z	Z	Z	Z

Receiver

	INPUTS				OUTPUTS	
CONFIGURATION	S1	S2	$\overline{OE}$	A – B	R1 AND R2	R3
DTE or All ON	X	1	0	≥0.2V	1	1
DTE or All ON	X	1	0	≤–0.2V	0	0
DCE	1	0	0	≥0.2V	1	Z
DCE	1	0	0	≤–0.2V	0	Z
Disabled	X	X	1	X	Z	Z
Shutdown*	0	0	1	X	Z	Z

*To ensure shutdown mode, both S1 and S2 should be LOW and $\overline{OE}$ should be HIGH

TEST CIRCUITS

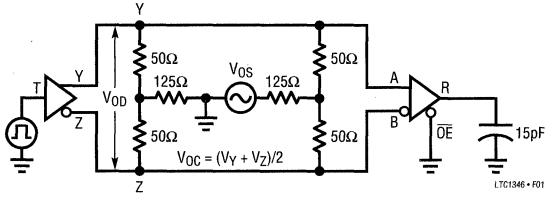


Figure 1. V.35 Transmitter/Receiver Test Circuit

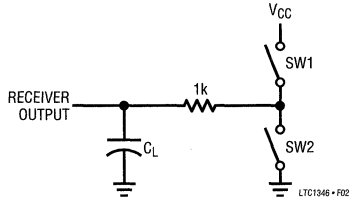


Figure 2. Receiver Output Enable and Disable Timing Test Load

SWITCHING TIME WAVEFORMS

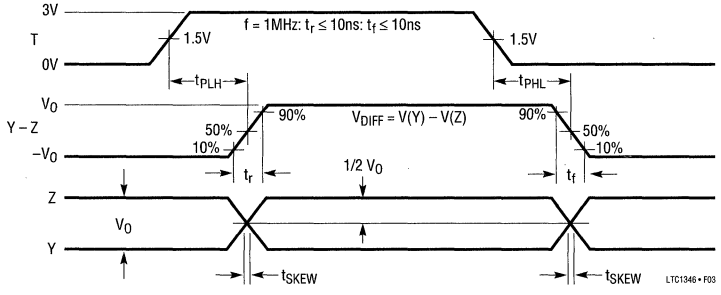


Figure 3. V.35 Transmitter Propagation Delays

SWITCHING TIME WAVEFORMS

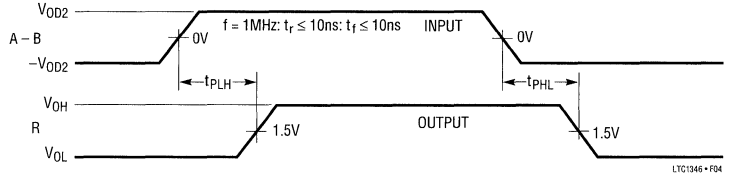


Figure 4. V.35 Receiver Propagation Delays

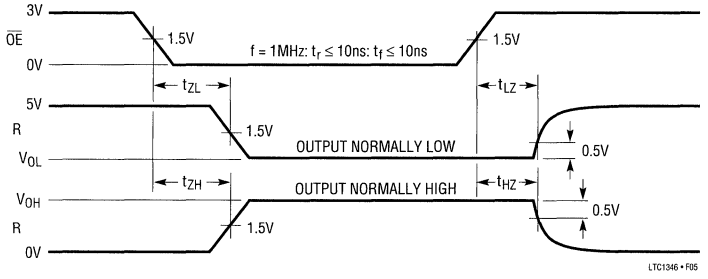


Figure 5. Receiver Enable and Disable Times

APPLICATIONS INFORMATION

Review of CCITT Recommendation V.35 Electrical Specifications

V.35 is a CCITT recommendation for synchronous data transmission via modems. Appendix 2 of the recommendation describes the electrical specifications which are summarized below:

1. The interface cable is a balanced twisted-pair with 80Ω to 120Ω impedance.
2. The transmitter's source impedance is between 50Ω and 150Ω.
3. The transmitter's resistance between shorted terminals and ground is 150Ω ±15Ω.
4. When terminated by a 100Ω resistive load, the terminal-to-terminal voltage should be 0.55V ±20%.
5. The transmitter's rise time should be less than 1% of the signal pulse or 40ns, whichever is greater.
6. The common-mode voltage at the transmitter output should not exceed 0.6V.
7. The receiver impedance is 100Ω ±10Ω.
8. The receiver impedance to ground is 150Ω ±15Ω.
9. The transmitter or receiver should not be damaged by connection to earth ground, short-circuiting, or cross connection to other lines.
10. No data errors should occur with ±2V common-mode change at either the transmitter or receiver, or ±4V ground potential difference between transmitter and receiver.

Cable Termination

Each end of the cable connected to an LTC1346 must be terminated by an external Y or Δ resistor network for proper operation. The Y-termination has two series connected 50Ω resistors and a 125Ω resistor connected between ground and the center tap of the two 50Ω resistors as shown in Figure 6.

APPLICATIONS INFORMATION

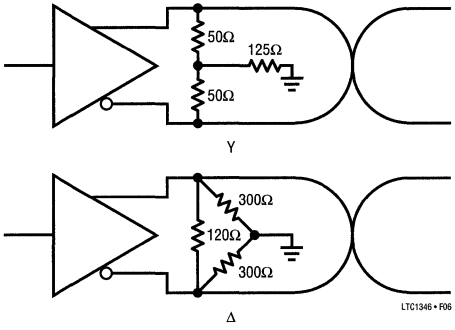


Figure 6. Y and Δ Termination Networks

The alternative Δ-termination has a 120Ω resistor across the twisted wires and two 300Ω resistors between each wire and ground. Standard 1/8W, 5% surface mount resistors can be used for the termination network. To maintain the proper differential output swing, the resistor tolerance must be 5% or less. A termination network that combines all the resistors into an 14-pin SO package is available from:

BI Technologies (Formerly Beckman Industrial)
Resistor Networks
4200 Bonita Place
Fullerton, CA 92635
Phone: (714) 447-2357
FAX: (714) 447-2500
Part #: BI Technologies 627T500/1250 (SO)
899TR50/125 (DIP)

Theory of Operation

The transmitter output consists of complementary switched-current sources as shown in Figure 7.

With a logic zero at the transmitter input, the inverting output Z sources 11mA and the noninverting output Y sinks 11mA. The differential transmitter output voltage is then set by the termination resistors. With two differential 50Ω resistors at each end of the cable, the voltage is set to (50Ω × 11mA) = 0.55V. With a logic 1 at the transmitter input, output Z sinks 11mA and Y sources 11mA. The common-mode voltage of Y and Z is 0V when both current sources are matched and there is no ground potential

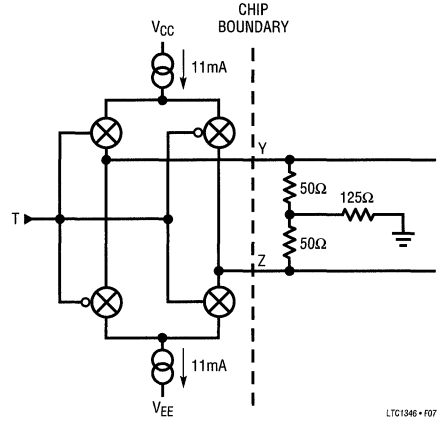


Figure 7. Simplified Transmitter Schematic

difference between the cable terminations. The transmitter current sources have a common-mode range of ±2V, which allows for a ground difference between cable terminations of ±4V.

Each receiver input has a 30k resistance to ground and requires external termination to meet the V.35 input impedance specification. The receivers have an input hysteresis of 50mV to improve noise immunity. The receiver output may be forced into a high impedance state by pulling the output enable ($\overline{OE}$) pin HIGH. For normal operation $\overline{OE}$ should be pulled LOW.

Two Select pins, S1 and S2, configure the chip for DTE, DCE, all transmitter and receivers ON, or Shutdown. To ensure shutdown mode, both S1 and S2 should be LOW and $\overline{OE}$ should be HIGH. In Shutdown mode, I_{CC} drops to 1μA. The outputs of the transmitters and receivers are in high impedance states.

Complete V.35 Port

Figure 8 shows the schematic of a complete surface mounted, single 5V DTE and DCE V.35 port using only three ICs and six capacitors per port. The LTC1346 is used to transmit the clock and data signals, and the LT1134A to transmit the control signals. If test signals 140, 141, and 142 are not used, the transmitter inputs should be tied to V_{CC}.

APPLICATIONS INFORMATION

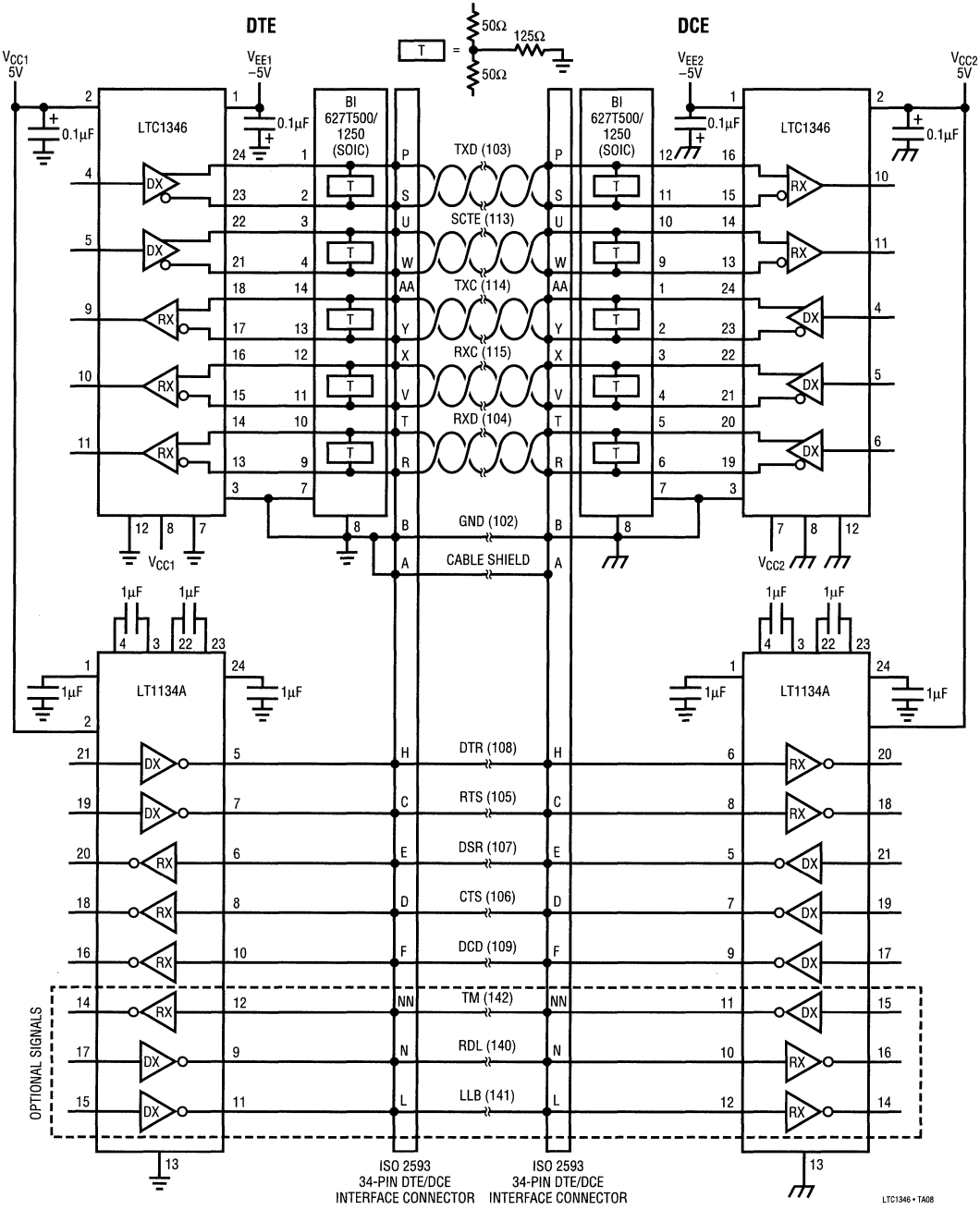


Figure 8. Complete ±5V V.35 Interface

APPLICATIONS INFORMATION

RS422/RS485 Applications

The receivers on the LTC1346 are ideal for RS422 and RS485 applications. Using the test circuit in Figure 9, the LTC1346 receivers are able to successfully reconstruct the data stream with the common-mode voltage meeting RS422 and RS485 requirements (12V to –7V).

Figures 10 and 11 show that the LTC1346 receivers are very capable of reconstructing data at frequencies up to 10MHz.

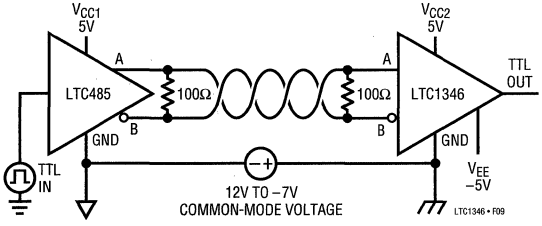


Figure 9 RS422/RS485 Receiver Interface

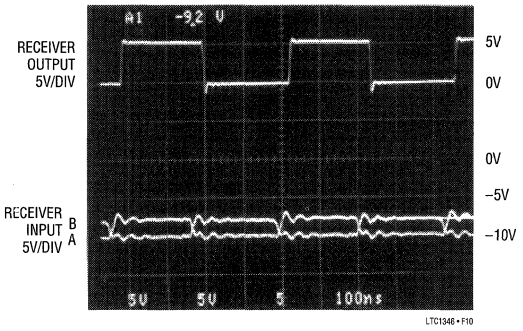


Figure 10. –7V Common Mode

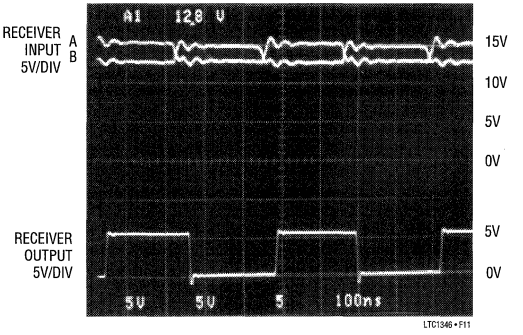


Figure 11. 12V Common Mode

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1345	Single Supply V.35 Transceiver	Requires Only Single 5V Power

LT1389

AppleTalk® Peripheral Interface Transceiver

June 1995

FEATURES

- **Provides Complete AppleTalk DCE Interface**
- **Supports Direct Connect or LocalTalk®**
- Transmit Enable Controls Three-State Driver Outputs
- Flow-Through Architecture for Easy PC Layout
- Rugged Bipolar Design
- Thermal Shutdown Protection
- Outputs Assume a High Impedance State when Off or Powered Down
- Short-Circuit Protection on All Outputs

APPLICATIONS

- Printers
- Modems
- Local Area Networks

DESCRIPTION

The LT®1389 is a complete AppleTalk DCE interface transceiver. The circuit includes one differential driver, one differential receiver, two high speed single-ended drivers and one RS232/RS562 receiver. Logic inputs provide driver and receiver three-state modes and a low power shutdown control. The differential driver may be used as an additional single-ended driver, supporting RS562 output levels.

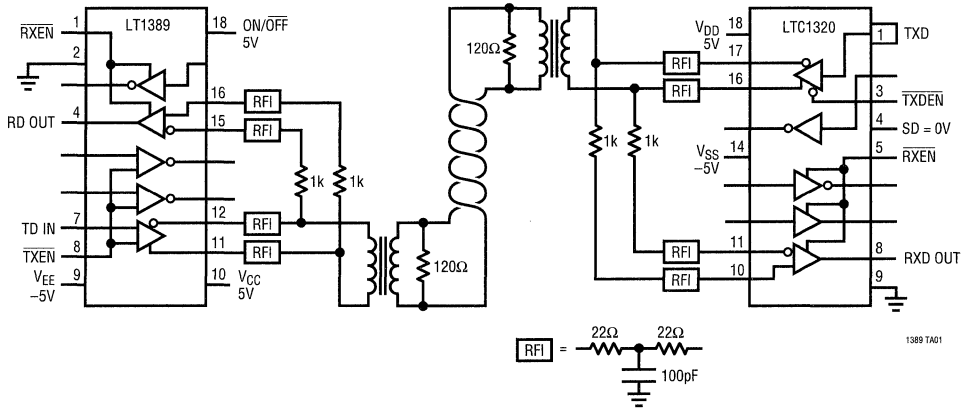
The high speed single-ended driver and differential driver support data clock rates to 1Mbaud, allowing direct connect operation with all Macintosh peripheral devices.

The Transmit and Receive Enable controls provide flexible operating mode control for sharing data lines between multiple circuits.

The LT1389 is available in 18-lead PDIP and SO Wide packages.

TYPICAL APPLICATION

Typical LocalTalk Application



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V_{CC} 6V
- V_{EE} ..... −6V

Input Voltage
- Driver ..... −0.2V to 6V
- $\overline{TXEN}$, $\overline{RXEN}$, ON/$\overline{OFF}$ ..... −0.2V to 6V
- Single-Ended Receiver ..... −30V to 30V
- Differential Receiver ..... −7V to 12V

Output Voltage
- Driver ..... −30V to V_{CC} + 12V
- Receiver ..... −0.3V to V_{CC} + 0.3V

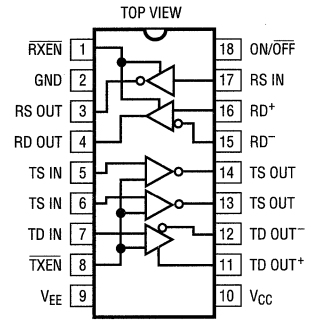
Short-Circuit Duration
- Driver Output ..... Indefinite
- Receiver Output ..... Indefinite

Operating Temperature Range ..... 0°C to 70°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N PACKAGE
18-LEAD PDIP

SW PACKAGE
18-LEAD PLASTIC SO WIDE

T_{JMAX} = 150°C, θ_{JA} = 100°C/ W (N)
T_{JMAX} = 150°C, θ_{JA} = 100°C/ W (SW)

ORDER PART NUMBER
LT1389CN LT1389CSW

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	V_{CC} V_{EE}	$V_{ON/\overline{OFF}}$ = 5V		8 3	15 5	mA mA
Supply Current in Shutdown	V_{CC} V_{EE}	$V_{ON/\overline{OFF}}$ = 0V			10 10	µA µA
Logic Input Thresholds ($\overline{TXEN}$, ON/$\overline{OFF}$, TS IN, TD IN)		Input Low Level Input High Level	0.8	1.4 1.4	 2.0	V V
Differential/Single-Ended Driver						
Differential Output Voltage, V_{OD}		No Load (Figure 1) R_L = 100Ω R_L = 50Ω	7 2 1.5	8 3 3	10	V V V
Output Common-Mode Voltage, V_{OC}		R_L = 100Ω (Figure 1)	2.0		3.0	V
Single-Ended Output Voltage		Output High, R_L = 3k (Figure 2) Output Low, R_L = 3k	3.7	4.2 −4.0	 −3.7	V V
Input Current		0V ≤ V_{IN} ≤ 5V	−10		10	µA
Output Leakage Current		$V_{\overline{TXEN}}$ = 2V, −5V ≤ V_{OUT} ≤ 5V	−100		100	µA
Output Short-Circuit Current		I_{SC}^+ I_{SC}^-, V_{OUT} = 5V I_{SC}^-, V_{OUT} = 0V	35 −200 −20	150	 −35 −8	mA mA mA
Differential Mode Propagation Delay		R_L = 100Ω		40	75	ns
Driver Disable Delay				40	75	ns
Driver Enable Delay				40	75	ns
Single-Ended Output Fall Time		R_L = 3k, C_L = 2500pF, V_{OUT} = 3V to −3V		1	2	µs
Single-Ended Output Rise Time		R_L = 3k, C_L = 2500pF, V_{OUT} = −3V to 3V		1	2	µs

ELECTRICAL CHARACTERISTICS $0°C \le T_A \le 70°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Receiver					
Differential Input Voltage Thresholds	$-7V \le V_{CM} \le 12V$	−0.2		0.2	V
Receiver Input Hysteresis	$-7V \le V_{CM} \le 12V$		70		mV
Input Resistance		12			kΩ
Input Common-Mode Voltage		−7		12	V
Output Voltage	Output High, I_{OUT} = 160µA Output Low, I_{OUT} = −1.6mA	2.4	4.0 0.2	 0.4	V V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$ Sourcing Current, V_{OUT} = 0V	−20	−10 10	 20	mA mA
Propagation Delay			40	70	ns
Single-Ended Receiver					
Input Voltage Threshold	Input Low Threshold Input High Threshold	0.8	1.3 1.7	 2.4	V V
Hysteresis		0.1	0.4	1.0	V
Input Resistance	$-5V \le V_{IN} \le 5V$	3	5	7	kΩ
Output Voltage	Output Low, I_{OUT} = −1.6mA Output High, I_{OUT} = 160mA (V_{CC} = 5V)	 3.5	0.2 4.2	0.4 	V V
Output Short-Circuit Current	Sinking Current, $V_{OUT} = V_{CC}$ Sourcing Current, V_{OUT} = 0V	−20	−10 10	 20	mA mA
Propagation Delay	Output Transition High to Low, t_{HL} Output Transition Low to High, t_{LH}		250 350	600 600	ns ns
Single-Ended Drivers					
Output Voltage	Output High, R_L = 3k Output Low, R_L = 3k	3.7	4.0 −4.4	 −3.7	V V
Logic Input Current		−10		10	µA
Output Leakage Current	Shutdown or Driver Disable Modes	−100		100	µA
Output Short-Circuit Current	Sinking Current, V_{OUT} = 0V Sourcing Current, V_{OUT} = 0V	−40	−10 50		mA mA
Slew Rate		60	100		V/µs
Propagation Delay			60	100	ns
Driver Disable Delay			40	75	ns
Driver Enable Delay			60	100	ns

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: Unless otherwise specified, testing done at V_{CC} = 5V, V_{EE} = −5V and $V_{\overline{TXEN}}$ = 0V. Outputs and single-ended receiver inputs are open. Driver inputs are tied to V_{CC}. Differential receiver input RD^- is biased at 2.6V, RD^+ at 2.4V.

Note 3: For driver delay measurements, R_L = 3k and C_L = 51pF. Trigger points are set between the driver's input logic threshold and the output transition to the zero crossing. ($t_{HL} = t_{LH}$ = 1.4V to 0V)

Note 4: For receiver delay measurements, C_L = 51pF. Trigger points are set between the receiver's input logic threshold and the output transition to standard TTL/CMOS logic threshold. (t_{HL} = 1.3V to 2.4V and t_{LH} = 1.7V to 0.8V)

13

PIN FUNCTIONS

$\overline{RXEN}$ (Pin 1): Receiver Enable Control. An open pin or a logic low allows normal operation of the receivers. A logic high causes receiver outputs to become high impedance, allowing sharing of the receiver output data lines.

GND (Pin 2): Ground Pin.

RS OUT (Pin 3): Single-Ended Receiver Output with TTL/CMOS Voltage Levels. The output is fully short-circuit protected to GND or V_{CC}.

PIN FUNCTIONS

RD OUT (Pin 4): Differential Receiver Output Pin with TTL/CMOS Voltage Levels. The output is fully short-circuit protected to GND or V_{CC}.

TS IN (Pins 5, 6): Single-Ended Driver Input Pins. These inputs are TTL/CMOS compatible. An input logic low causes a driver output high. Tie unused inputs to GND.

TD IN (Pin 7): Differential Driver Input Pin. A TTL/CMOS compatible logic input. A logic high causes driver output RD^+ to swing high and RD^- low. Tie input to V_{CC} when not in use.

$\overline{TXEN}$ (Pin 8): A TTL/CMOS logic high places the driver outputs into a high impedance state. A logic low fully enables the transmit capabilities. Transitions occur at data rate speeds to facilitate data line multiplexing.

V_{EE}: (Pin 9): –5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor.

V_{CC} (Pin 10): 5V Input Supply Pin. This pin should be decoupled with a 0.1µF ceramic capacitor.

TD OUT^+, TD OUT^- (Pins 11, 12): Differential Driver Output Pins. Outputs drive 100Ω differential loads to RS422 levels, and are also capable of supplying RS562 levels to single-ended loads greater than 3kΩ. Outputs are in a high impedance state when $\overline{TXEN}$ is high or V_{CC} = 0V. Outputs are fully short-circuit protected from $V_{OUT} = V_{EE}$ + 20V to $V_{OUT} = V_{CC}$ – 20V. Applying higher voltages will not damage the device if the overdrive is moderately current limited.

TS OUT (Pins 13, 14): Single-Ended Driver Outputs at RS562 Voltage Levels. Outputs are in a high impedance state when $\overline{TXEN}$ is high or V_{CC} = 0V. Outputs are fully short-circuit protected from $V_{OUT} = V_{EE}$ + 20V to $V_{OUT} = V_{CC}$ – 20V. Applying higher voltage will not damage the device if the overdrive is moderately current limited.

RD^-, RD^+ (Pins 15, 16): Differential Receiver Input Pins. Common-mode input range is –7V to 12V. Receiver inputs have 50mV of hysteresis for noise immunity.

RS IN (Pin 17): Single-Ended Receiver Input. This pin accepts RS232 or RS562 level signals (±30V) into a protected 5k terminating resistor. The receiver input provides 0.4V of hysteresis for noise immunity. Data rates to 120kbaud are supported.

ON/$\overline{OFF}$ (Pin 18): A logic low level on this pin shuts down the circuit. All receiver and driver outputs are high impedance. A logic high allows normal operation of the circuit.

TEST CIRCUITS

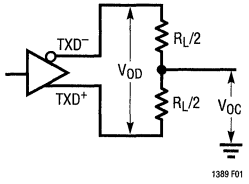


Figure 1. Differential Output Test Circuit

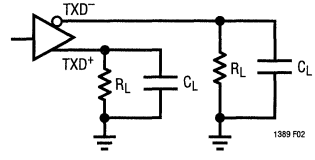


Figure 2. Single-Ended Output Test Circuit

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1320	Appletalk Transceiver	Complete DTE Port
LTC1334	RS232/RS485 Multi-Protocol Transceiver	Appletalk Compatible
LTC1337	5V 3-Driver/5-Receiver Micropower RS232 Transceiver	500µA Quiescent Current
LTC1345	V.35 Differential Transceiver	Low Power V.35 Solution
LTC1348	3.3V 3-Driver/5-Receiver RS232 Transceiver	True RS232 from 3.3V Supplies

Micropower Temperature, Power Supply and Differential Voltage Monitor

July 1995

FEATURES

- **Complete Ambient Temperature Sensor Onboard**
- **Power Supply Monitor**
- **10-Bit Resolution Rail-to-Rail Common-Mode Differential Voltage Input**
- Available in 8-Pin SO
- 0.2µA Supply Current When Idle
- 350µA Supply Current When Converting
- Single Supply Voltage: 4.5V to 6V
- Three-Wire Half-Duplex Serial I/O
- Communicates with Most MPU Serial Ports and All MPU Parallel I/O Ports

APPLICATIONS

- Temperature Measurement
- Power Supply Measurement
- Current Measurement
- Remote Data Acquisition

DESCRIPTION

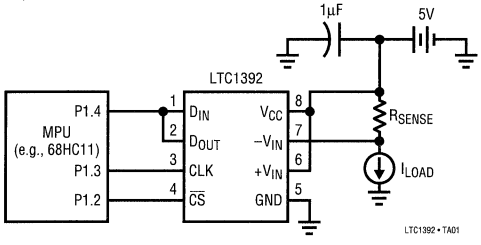
The LTC®1392 is a micropower data acquisition system designed to measure temperature, on-chip supply voltage and differential rail-to-rail common-mode voltage. The device features a temperature sensor, a 10-Bit A/D converter with sample-and-hold, a high accuracy bandgap reference and a three-wire half-duplex serial interface.

The LTC1392 can be programmed to measure ambient temperature, power supply voltage and external voltage at the differential input pins, which can be used for current measurement. When measuring temperature, the output code of the A/D converter is linearly proportional to the temperature in °Celsius. Wafer level trimming achieves ±2°C initial accuracy at room temperature and ±4°C over the full –40°C to 85°C temperature range.

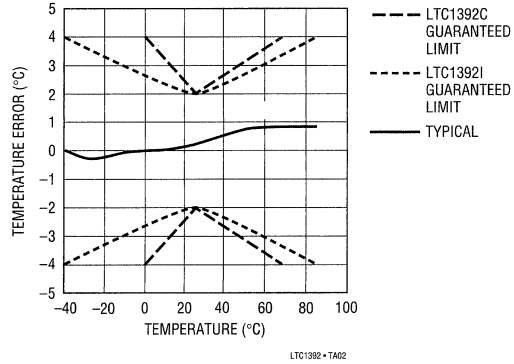
The on-chip serial port allows efficient data transfer to a wide range of MPUs over three wires. This, coupled with low power consumption, makes remote location sensing possible and facilitates transmitting data through isolation barriers.

TYPICAL APPLICATION

Complete Temperature, Supply Voltage and Supply Current Monitor



Output Temperature Error



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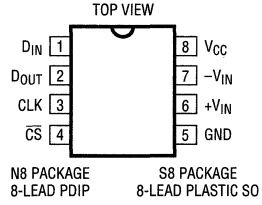
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V_{CC}) 7V
Input Voltage ..... −0.3V to V_{CC} + 0.3V
Output Voltage ..... −0.3V to V_{CC} + 0.3V
Operating Temperature Range
  Commercial ..... 0°C to 70°C
  Industrial ..... −40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)

ORDER PART NUMBER
LTC1392CN8 LTC1392CS8 LTC1392IN8 LTC1392IS8
S8 PART MARKING
1392 1392I

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply To Digital Conversion						
Resolution	V_{CC} = 4.5V to 6V				10	Bit
Total Absolute Error	V_{CC} = 4.5V to 6V, 0°C ≤ T_A ≤ 70°C V_{CC} = 4.5V to 6V, −40°C ≤ T_A ≤ 85°C				±5 ±8	LSB LSB
Differential Voltage to Digital Conversion (Full-Scale Input = 1V)						
Resolution					10	Bit
Integral Linearity Error (Note 5)		●		±2		LSB
Differential Linearity Error		●		±1		LSB
Offset Error		●		±4		LSB
Full-Scale Error		●			±10	LSB
Input Refered Noise				±1		LSB_{RMS}
Differential Voltage to Digital Conversion (Full-Scale Input = 0.5V)						
Resolution					10	Bit
Integral Linearity Error (Note 5)		●		±4		LSB
Differential Linearity Error		●		±2		LSB
Offset Error		●		±8		LSB
Full-Scale Error		●			±20	LSB
Input Refered Noise				±2		LSB_{RMS}
Temperature to Digital Conversion (LTC1392)						
Accuracy	T_A = 25°C (Note 7) T_A = T_{MAX} or T_{MIN} (Note 7)	● ●			±2 ±4	°C °C
Nonlinearity	T_{MIN} ≤ T_A ≤ T_{MAX} (Note 4)			±1		°C

ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{ON\ LEAKAGE}$	On-Channel Leakage Current (Note 6)		●			±1	µA
$I_{OFF\ LEAKAGE}$	Off-Channel Leakage Current (Note 6)		●			±1	µA
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.4	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_{OUT} = 10µA V_{CC} = 4.75V, I_{OUT} = 360µA	●	4.5 2.4	4.74 4.72		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_{OUT} = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Current	$\overline{CS}$ High	●			±5	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–25		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			45		mA
I_{CC}	Supply Current	$\overline{CS}$ High t_{CYC} = 76µs, f_{CLK} = 250kHz	●		0.1 300	5 500	µA µA
t_{SMPL}	Analog Input Sample Time	See Figure 1			1.5		CLK Cycles
t_{CONV}	Conversion Time	See Figure 1			10		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	C_{LOAD} = 100pF	●		150	300	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Data Enabled	C_{LOAD} = 100pF	●		60	150	ns
t_{dis}	Delay Time, $\overline{CS}$ ↑ to D_{OUT} Hi-Z		●		170	450	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			30		ns
t_f	D_{OUT} Fall Time	C_{LOAD} = 100pF	●		70	250	ns
t_r	D_{OUT} Rise Time	C_{LOAD} = 100pF	●		25	100	ns
C_{IN}	Input Capacitance	Analog Input On-Channel Analog Input Off-Channel			30 5		pF pF
		Digital Input			5		pF

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		4.5		6	V
f_{CLK}	Clock Frequency	V_{CC} = 5V	50		250	kHz
t_{CYC}	Total Cycle Time	f_{CLK} = 250kHz Temperature Conversion Only	74 144			µs µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 5V	150			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Figure 1)	V_{CC} = 5V	2			µs
t_{WAKEUP}	Wakeup Time $\overline{CS}$↓ Before Start Bit↑ (See Figure 1)	V_{CC} = 5V Temperature Conversion Only	10 80			µs µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 5V	150			ns
t_{WHCLK}	Clock High Time	V_{CC} = 5V	1.6			µs
t_{WLCLK}	Clock Low Time	V_{CC} = 5V	2			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	V_{CC} = 5V, f_{CLK} = 250kHz	2			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	V_{CC} = 5V, f_{CLK} = 250kHz Temperature Conversion Only	72 142			µs µs

RECOMMENDED OPERATING CONDITIONS

The ● denotes specifications which apply over the operating temperature range ($0°C \le T_A \le 70°C$ for commercial grade and $-40°C \le T_A \le 85°C$ for industrial grade).

Note 1: Absolute maximum ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: Testing done at V_{CC} = 5V, CLK = 250kHz and $T_A = 25°C$ unless otherwise specified.

Note 4: Temperature integral nonlinearity is defined as the deviation of the A/D code versus temperature curve from the best-fit straight line over the device's rated temperature range.

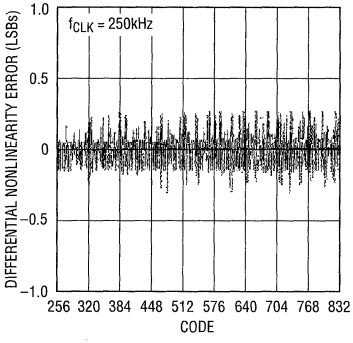
Note 5: Voltage integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual end points of the transfer curve.

Note 6: Channel leakage current is measured after the channel selection.

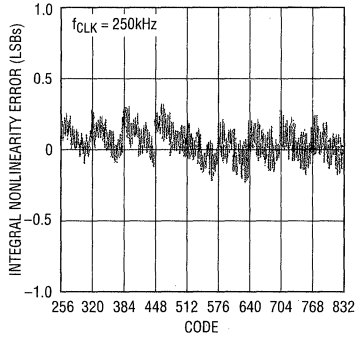
Note 7: See guaranteed temperature limit curves vs temperature range on the first page of this data sheet.

TYPICAL PERFORMANCE CHARACTERISTICS

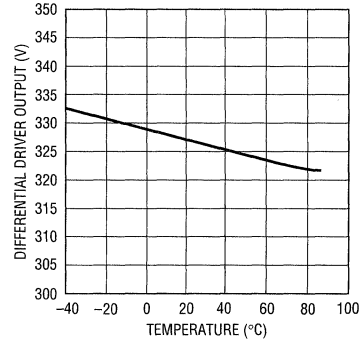
Differential Nonlinearity, Power Supply Voltage Mode



Integral Nonlinearity, Power Supply Voltage Mode



Supply Current vs Temperature



PIN FUNCTIONS

D_{IN} (Pin 1): Digital Input. The A/D configuration word is shifted into this input.

D_{OUT} (Pin 2): Digital Output. The A/D result is shifted out of this output.

CLK (Pin 3): Shift Clock. This clock synchronizes the serial data.

$\overline{CS}$ (Pin 4): Chip Select Input. A logic low on this input enables the LTC1392.

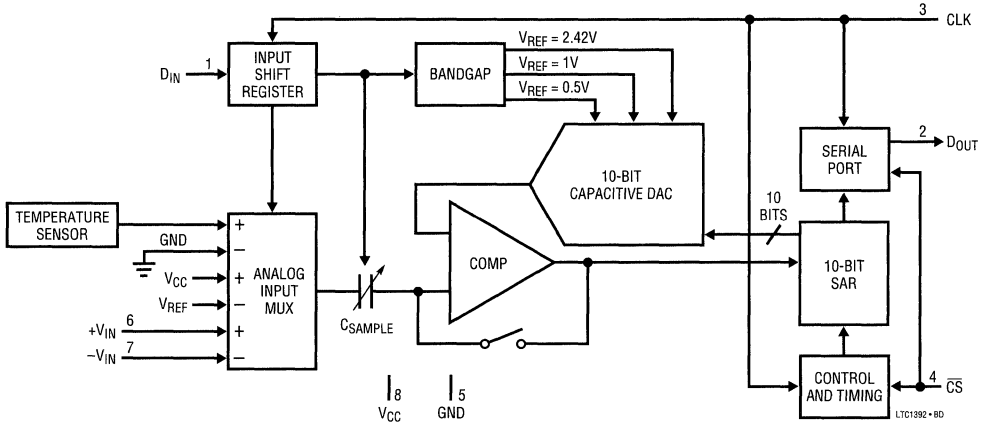
GND (Pin 5): Ground Pin. GND should be tied directly to an analog ground plane.

$+V_{IN}$ (Pin 6): Positive Analog Differential Input. The pin can be used as a single-ended input by grounding $-V_{IN}$.

$-V_{IN}$ (Pin 7): Negative Analog Differential Input. The input must be free from noise.

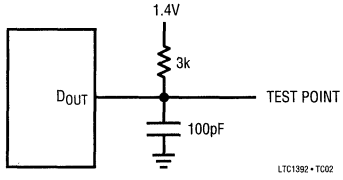
V_{CC} (Pin8): Positive Supply. This supply must be kept free from noise and ripple by bypassing directly to the ground plane.

BLOCK DIAGRAM

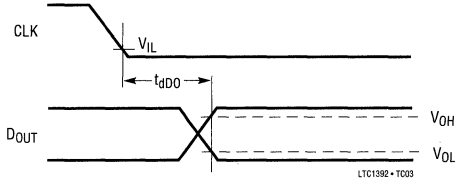


TEST CIRCUITS

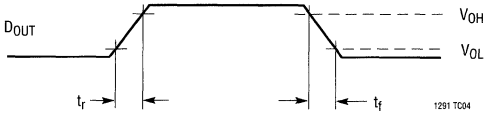
Load Circuit for t_{dDO}, t_r and t_f



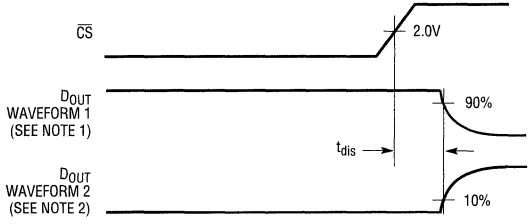
Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r and t_f



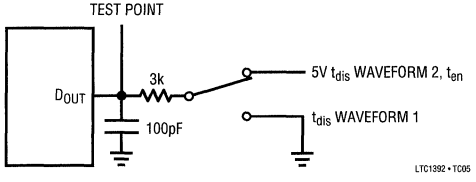
Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNTIL DISABLED BY THE OUTPUT CONTROL.
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNTIL DISABLED BY THE OUTPUT CONTROL.

LTC1392 • TC06

Load Circuit for t_{dis} and t_{en}



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APPLICATIONS INFORMATION

The LTC1392 is a micropower data acquisition system designed to measure temperature, on-chip power supply voltage and differential input voltage. The LTC1392 contains the following functional blocks:

1. On-chip temperature sensor
2. 10-bit successive approximation capacitive ADC
3. Bandgap reference
4. Analog multiplexer (MUX)
5. Sample-and-hold (S/H)
6. Synchronous, half-duplex serial interface
7. Control and timing logic

DIGITAL CONSIDERATIONS

Serial Interface

The LTC1392 communicates with microprocessors and other external circuitry via a synchronous, half-duplex, three-wire serial interface (see Figure 1). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems. The input data is first received and then the A/D conversion result is transmitted (half-duplex). Half-duplex operation allows D_{IN} and D_{OUT} to be tied together allowing transmission over three wires: $\overline{CS}$, CLK and DATA (D_{IN}/D_{OUT}). Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After the falling $\overline{CS}$ is recognized, an 80µs delay is needed for temperature measurement or a 10µs delay for other measurements, followed by a 4-bit input word which configures the LTC1392 for the current conversion. This data word is shifted into the D_{IN} input. D_{IN} is then disabled from shifting in any data and the D_{OUT} pin is configured from three-state to an output pin. A null bit and the result of the current conversion are serially transmitted on the falling CLK edge onto the D_{OUT} line. The format of the A/D result can be either MSB-first sequence or MSB-first sequence followed by an LSB-first sequence. This provides easy interface to MSB- or LSB-first serial ports. Bringing $\overline{CS}$ high resets the LTC1392 for the next data exchange.

INPUT DATA WORD

The LTC1392 4-bit input word is clocked into the D_{IN} input on the first four rising CLK edges after $\overline{CS}$ is recognized. Further inputs on the D_{IN} input are then ignored until the next $\overline{CS}$ cycle. The four bits of the input word are defined as follows:

BIT 3	BIT 2	BIT 1	BIT 0
Start	Select 1	Select 0	MSBF

Start Bit

The first "logic one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the Start Bit. The Start Bit initiates the data transfer and all leading zeros which precede this logical one will be ignored. After the Start Bit is received the remaining bits of the input word will be clocked in. Further input on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

Measurement Modes Selection

The two bits of the input word following the Start Bit assign the measurement mode for the requested conversion. Table 1 shows the modes selection. Whenever there is a mode change from another mode to temperature measurement, a temperature mode initializing cycle is needed. The first temperature data measurement after a mode change should be ignored.

Table 1. Measurement Modes Selection

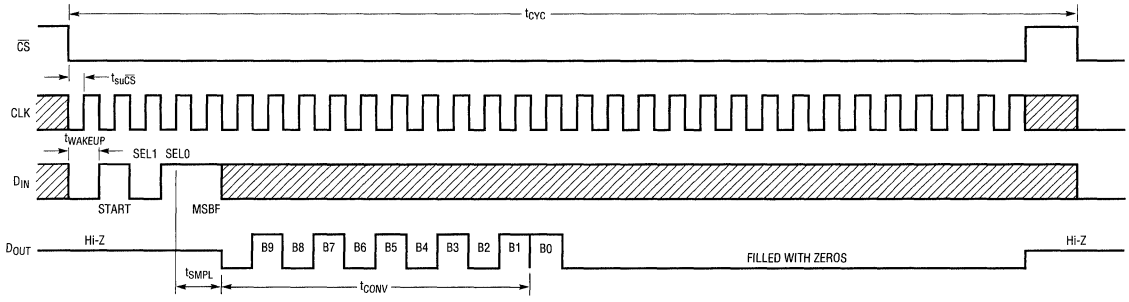
SELECT 1	SELECT 0	MEASUREMENT MODE
0	0	Temperature
0	1	Power Supply Voltage
1	0	Differential Input, 1V Full Scale
1	1	Differential Input, 0.5V Full Scale

MSB-First/LSB-First (MSBF)

The output data of the LTC1392 is programmed for MSB-first or LSB-first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT}

APPLICATIONS INFORMATION

MSB-First Data (MSBF = 1)



MSB-First Data (MSBF = 0)

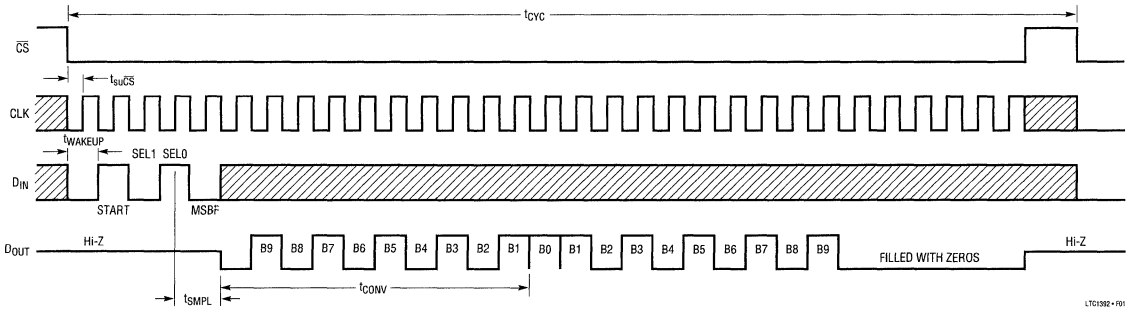


Figure 1.

line in MSB-first format. Logical zeros will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB-first data will follow the normal MSB-first data on the D_{OUT} line.

CONVERSIONS

Temperature Conversion

The LTC1392 measures temperature through the use of an on-chip, proprietary temperature measurement technique. The temperature reading is provided in a 10-bit, unipolar format. Table 2 describes the exact relationship of output data to measured temperature or equation 1 can be used to calculate the temperature.

$$\text{Temperature (°C)} = \text{Output Code}/4 - 130 \qquad (1)$$

Note that the LTC1392I is only specified for use over the –40°C to 85°C operating temperature range. Temperature outside this range may have errors greater than those shown in the electrical characteristic table.

Table 2. Codes for Temperature Conversion

OUTPUT CODE	TEMPERATURE (°C)
1111111111	125.75
1111111110	125.50
...	...
1001110101	27.25
1001110100	27.00
1001110011	26.75
...	...
0000000001	–129.75
0000000000	–130.00

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APPLICATIONS INFORMATION

Voltage Supply (V_{CC}) Monitor

The LTC1392 measures supply voltage through the on-chip V_{CC} supply line. The V_{CC} reading is provided in a 10-bit, unipolar format. Table 3 describes the exact relationship of output data to measured V_{CC} or equation (2) can be used to calculate the measured V_{CC}.

$$\text{Measured } V_{CC} = (7.26 - 2.42) \times \text{Output Code}/1024 + 2.42 \quad (2)$$

The guaranteed supply voltage monitor range is from 4.5V to 6V. Typical parts are able to maintain the measurement accuracy with V_{CC} as low as 3.25V. The typical INL and DNL error plots shown on page 4 are measured with V_{CC} from 3.63V to 6.353V.

Table 3. Codes for Voltage Supply Conversion

OUTPUT CODE	Supply Voltage (V_{CC})
1011110110	6.003V
1011110101	5.998V
...	...
1000100010	5.001V
...	...
0110111001	4.504V
0110111000	4.500V

Differential Voltage Conversion

The LTC1392 measures the differential input voltage through pins $+V_{IN}$ and $-V_{IN}$. Input ranges of 0.5V or 1V full scale are available for differential voltage measurement with resolutions of 10 bits. Tables 4a and 4b describe the exact relationship of output data to measured differential input voltage in the 1V and 0.5V input range. Equations (3) and (4) can be used to calculate the differential voltage in the 1V and 0.5V input voltage range respectively. The output code is in unipolar format.

$$\text{Differential Voltage} = \text{10-bit code}/1024 \quad (3)$$

$$\text{Differential Voltage} = 0.5 \times (\text{10-bit code})/1024 \quad (4)$$

Table 4a. Codes for 1V Differential Voltage Range

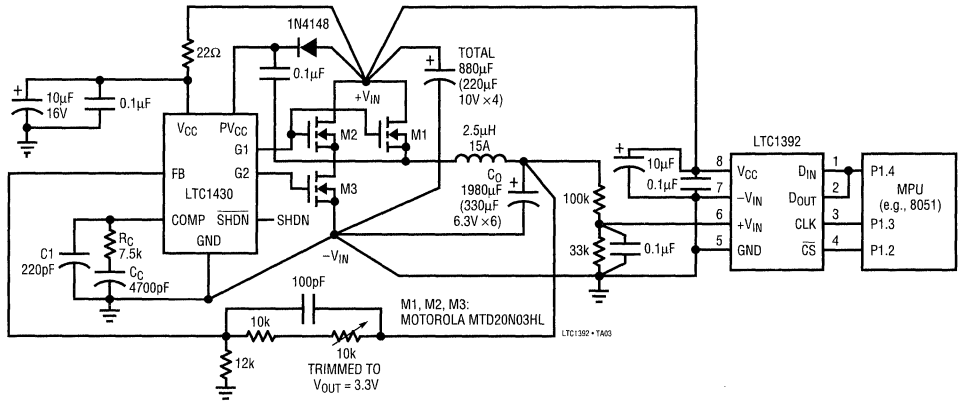
OUTPUT CODE	INPUT VOLTAGE	INPUT RANGE = 1V	REMARKS
1111111111	1V – 1LSB	999.0mV	
1111111110	1V – 2LSB	998.0mV	
...	...	...	
0000000001	1LSB	0.977mV	1LSB = 1/1024
0000000000	0LSB	0.00mV	

Table 4b. Codes for 0.5V Differential Voltage Range

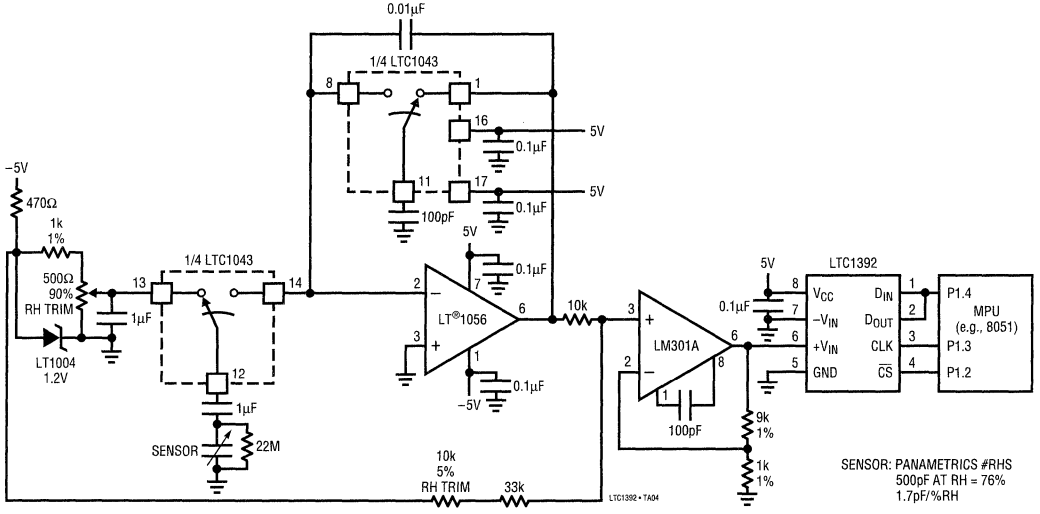
OUTPUT CODE	INPUT VOLTAGE	INPUT RANGE = 0.5V	REMARKS
1111111111	0.5V – 1LSB	499.0mV	
1111111110	0.5V – 2LSB	498.1mV	
...	...	...	
0000000001	1LSB	0.488mV	1LSB = 0.5/1024
0000000000	0LSB	0.00mV	

TYPICAL APPLICATIONS

System Monitor for Two Supply Voltages and Ambient Temperature



System Monitor for Relative Humidity, Supply Voltage and Ambient Temperature



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENT
LT1025	Micropower Thermocouple Cold Junction Compensator	Compatible with Standard Thermocouples (E, J, K, R, S, T)
LTC1285/LTC1288	3V Micropower 12-Bit ADC with Auto Shutdown	Differential or 2-Channel Multiplexed, Single Supply
LTC1286/LTC1298	Micropower 12-Bit ADC with Auto Shutdown	Differential or 2-Channel Multiplexed, Single Supply
LTC1390	Low Power, Precision 8-to-1 Analog Multiplexer	SPI, QSPI Compatible, Single 5V or 3V, Low R_{ON}, Low Charge Injection

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LTC1400

Complete SO-8, 12-Bit, 400ksps ADC with Shutdown

May 1995

FEATURES

- **Complete 12-Bit ADC in SO-8**
- **Single Supply 5V or ±5V Operation**
- **Sample Rate: 400ksps**
- Power Dissipation: 75mW (Typ)
- 70dB S/(N + D) and 74dB THD at Nyquist
- No Missing Codes over Temperature
- NAP Mode with Instant Wake-Up: 6mW
- SLEEP Mode: 30µW
- High Impendance Analog Input
- Input Range (1mV/LSB): 0V to 4.096 or ±2.048V
- Internal Reference Can Be Overdriven Externally
- 3-Wire Interface to DSPs and Processors

APPLICATIONS

- High Speed Data Acquisition
- Digital Signal Processing
- Multiplexed Data Acquisition Systems
- Audio and Telecom Processing
- Digital Radio
- Spectrum Analysis
- Low Power and Battery-Operated Systems
- Handheld or Portable Instruments

DESCRIPTION

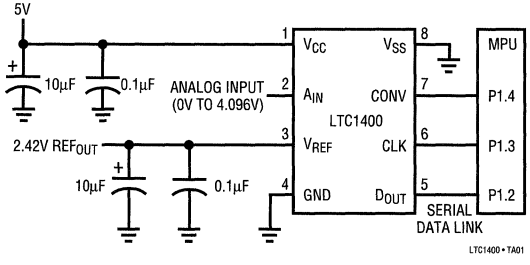
The LTC®1400 is a complete 400ksps, 12-bit A/D converter which draws only 75mW from a 5V or ± 5V supplies. This easy-to-use device comes complete with a 200ns sample-and-hold and a precision reference. Unipolar and bipolar conversion modes add to the flexibility of the ADC. The LTC1400 is capable of going into two power saving modes: NAP and SLEEP. In SLEEP mode, it consumes only 6mW of power and can wake up and convert immediately. In the SLEEP mode, it consumes 30µW of power typically. Upon power-up from SLEEP mode, a reference ready (REFRDY) signal is available in the serial data word to indicate that the reference has settled and the chip is ready to convert.

The LTC1400 converts 0V to 4.096V unipolar inputs from a single 5V supply and ±2.048V bipolar inputs from ±5V supplies. Maximum DC specs include ±1LSB INL, ±1LSB DNL and 25ppm/°C drift over temperature. Guaranteed AC performance includes 70dB S/(N + D) and 76dB THD at an input frequency of 100kHz, over temperature.

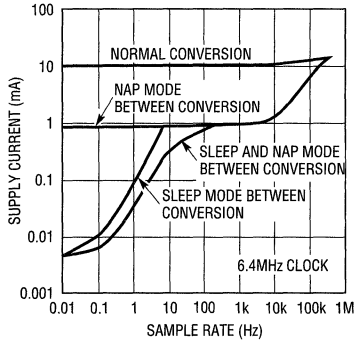
The 3-wire serial port allows compact and efficient data transfer to a wide range of microprocessors, microcontrollers and DSPs.

TYPICAL APPLICATION

Single 5V Supply, 400kHz, 12-Bit Sampling A/D Converter



Power Consumption vs Sample Rate

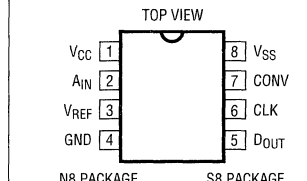


ABSOLUTE MAXIMUM RATINGS

Notes 1, 2)

Supply Voltage (V_{CC}) 7V
Negative Supply Voltage (V_{SS}) ..... −6V to GND
Total Supply Voltage (V_{CC} to V_{SS})
  Bipolar Operation Only 12V
Analog Input Voltage (Note 3)
  Unipolar Operation ..... −0.3V to (V_{CC} + 0.3V)
  Bipolar Operation ..... (V_{SS} − 0.3V) to (V_{CC} + 0.3V)
Digital Input Voltage (Note 4)
  Unipolar Operation ..... −0.3V to 12V
  Bipolar Operation ..... (V_{SS} − 0.3V) to 12V
Digital Output Voltage
  Unipolar Operation ..... −0.3V to (V_{CC} + 0.3V)
  Bipolar Operation ..... (V_{SS} − 0.3V) to (V_{CC} + 0.3V)
Power Dissipation 500mW
Operation Temperature Range
  LTC1400C ..... 0°C to 70°C
  LTC1400I ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 175°C/W (S8)

ORDER PART NUMBER
LTC1400CN8 LTC1400CS8 LTC1400IN8 LTC1400IS8
S8 PART MARKING
1400 1400I

Consult factory for Military grade parts.

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage (Note 6)	Unipolar		4.75		5.25	V
		Bipolar		4.75		5.25	V
V_{SS}	Negative Supply Voltage (Note 6)	Bipolar Only		−2.45		−5.25	V
I_{DD}	Positive Supply Current	f_{SAMPLE} = 400ksps	●		15	30	mA
		NAP Mode	●		1.0	3.0	mA
		SLEEP Mode	●		5.0	20.0	µA
I_{SS}	Negative Supply Current	f_{SAMPLE} = 400ksps, V_{SS} = −5V	●		0.3	0.6	mA
		NAP Mode	●		0.2	0.5	mA
		SLEEP Mode	●		1	5	µA
P_D	Power Dissipation	f_{SAMPLE} = 400ksps	●		75	160	mW
		NAP Mode	●		6	20	mW
		SLEEP Mode	●		30	125	µW

ANALOG INPUT (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range (Note 7)	4.75V ≤ V_{CC} ≤ 5.25V (Unipolar)	●		0 to 4.096		V
		4.75V ≤ V_{CC} ≤ 5.25V, −5.25V ≤ V_{SS} ≤ −2.45V (Bipolar)	●		±2.048		V
I_{IN}	Analog Input Leakage Current	During Conversions (Hold Mode)	●			±1	µA
C_{IN}	Analog Input Capacitance	Between Conversions (Sample Mode)			45		pF
		During Conversions (Hold Mode)			5		pF

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CONVERTER CHARACTERISTICS With internal reference (Notes 5, 8)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 9)	●			±1	LSB
Differential Linearity Error		●			±1	LSB
Offset Error	(Note 10)				±4	LSB
		●			±6	LSB
Full-Scale Error					±15	LSB
Full-Scale Tempco	$I_{OUT(REF)}$ = 0	●		±10	±45	ppm/°C

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal	●	70	72		dB
		200kHz Input Signal			70		dB
THD	Total Harmonic Distortion Up to 5th Harmonic	100kHz Input Signal	●		–80	–76	dB
		200kHz Input Signal			–74		dB
	Peak Harmonic or Spurious Noise	100kHz Input Signal	●		–84	–76	dB
		200kHz Input Signal			–74		dB
IMD	Intermodulation Distortion	f_{IN1} = 99.3kHz, f_{IN2} = 102.4kHz			–82		dB
		f_{IN1} = 199.37kHz, f_{IN2} = 202.4kHz			–70		dB
	Full Power Bandwidth				4		MHz
	Full Linear Bandwidth (S/(N + D) ≥ 68dB)				350		kHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.400	2.420	2.440	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±10	±45	ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{CC} ≤ 5.25V			0.01		LSB/V
	–5.25V ≤ V_{SS} ≤ 0V			0.01		LSB/V
V_{REF} Load Regulation	0 ≤ $\lvert I_{OUT} \rvert$ ≤ 1mA			2		LSB/mA

DIGITAL INPUTS AND OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{CC}	●			±10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = –10µA			4.7		V
		V_{CC} = 4.75V, I_O = –200µA	●	4.0			V
V_{OL}	Low Level Output Voltage	V_{CC} = 5.25V, I_O = 160µA			0.05		V
		V_{CC} = 5.25V, I_O = 1.6mA	●		0.10	0.4	V
I_{OZ}	Hi-Z Output Leakage D_{OUT}	V_{OUT} = 0V to V_{CC}	●			±10	µA
C_{OZ}	Hi-Z Output Capacitance D_{OUT} (Note 7)		●			15	pF
I_{SOURCE}	Output Source Current	V_{OUT} = 0			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			10		mA

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency	(Note 6)	●			400	kHz
t_{CONV}	Minimum Conversion Time		●	2.1			µs
t_{ACQ}	Acquisition Time (Unipolar Mode) (Bipolar Mode $V_{SS} = -5V$)	(Note 7)	● ●		230 200	300 270	ns ns
f_{CLK}	CLK Frequency		●	0.1		6.4	MHz
$t_{WK(NAP)}$	Time to Wake Up from NAP Mode	(Note 7)			350		ns
t_1	Minimum CLK Pulse Width to Return to Active Mode		●		20	50	ns
t_2	Minimum CONV↑ to CLK↑ Setup Time		●		40	80	ns
t_3	Maximum CONV↑ After Leading CLK↑		●		–20	0	ns
t_4	Minimum CONV Pulse Width	(Note 11)	●		20	50	ns
t_5	Time from CLK↑ to Sample Mode	(Note 7)	●		80		ns
t_6	Aperture Delay of Sample-and-Hold (Note 7)	Jitter < 50ps	●		45	65	ns
t_7	Minimum Delay Between Conversion (Unipolar Mode) (Bipolar Mode $V_{SS} = -5V$)		● ●		265 235	385 355	ns ns
t_8	Delay Time, CLK↑ to D_{OUT} Valid	$C_{LOAD} = 20pF$	●		40	65	ns
t_9	Delay Time, CLK↑ to D_{OUT} Hi-Z	$C_{LOAD} = 20pF$	●		40	80	ns
t_{10}	Time from Previous Data Remain Valid After CLK↑	$C_{LOAD} = 20pF$	●	14	25		ns

The ● denotes specifications which apply over the full operating temperature range; all other limits and typicals $T_A = 25°C$.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: When these pin voltages are taken below V_{SS} (ground for unipolar mode) or above V_{CC}, they will be clamped by internal diodes. This product can handle input currents greater than 40mA below V_{SS} (ground for unipolar mode) or above V_{CC} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} (ground for unipolar mode), they will be clamped by internal diodes. This product can handle input currents greater than 40mA below V_{SS} (ground for unipolar mode) without latch-up. These pins are not clamped to V_{CC}.

Note 5: $V_{CC} = 5V$, $f_{SAMPLE} = 400kHz$, $t_r = t_f = 5ns$ unless otherwise specified.

Note 6: Recommended operating conditions.

Note 7: Guaranteed by design, not subject to test.

Note 8: Linearity, offset and full-scale specifications apply for unipolar and bipolar modes.

Note 9: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 10: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 11: The rising edge of CONV starts a conversion. If CONV returns low at a bit decision point during the conversion, it can create small errors. For best performance ensure that CONV returns low either within 120ns after conversion starts (i.e., before the first bit decision) or after the 14 clock cycle. (Figure 9 Timing Diagram).

PIN FUNCTIONS

V_{CC} (Pin 1): Positive Supply, 5V. Bypass to GND (10µF tantalum in parallel with 0.1µF ceramic).

A_{IN} (Pin 2): Analog Input. 0V to 4.096V (Unipolar), ±2.048V (Bipolar).

V_{REF} (Pin 3): 2.42V Reference Output. Bypass to GND (10µF tantalum in parallel with 0.1µF ceramic).

GND (Pin 4): Ground. GND should be tied directly to an analog ground plane.

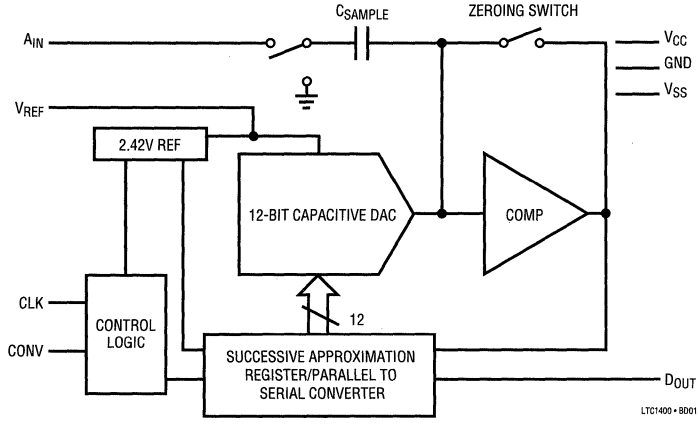
D_{OUT} (Pin 5): The A/D conversion result is shifted out from this pin.

CLK (Pin 6): Clock. This clock synchronizes the serial data transfer. A minimum CLK pulse of 50ns will cause the ADC to wake up from NAP or SLEEP mode.

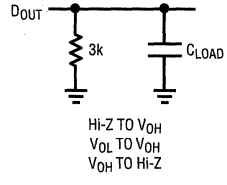
CONV (Pin 7): Conversion Start Signal. This active high signal starts a conversion on its rising edge. Keeping CLK low and pulsing CONV two/four times will put the ADC into NAP/SLEEP mode.

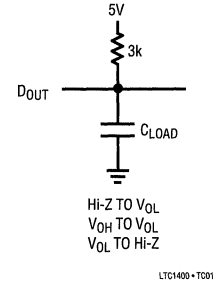
V_{SS} (Pin 8): Negative Supply. –5V for bipolar operation. Bypass to GND with 0.1µF ceramic. V_{SS} should short to GND for unipolar operation.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS





APPLICATIONS INFORMATION

Conversion Details

The LTC1400 uses a successive approximation algorithm and an internal sample-and-hold circuit to convert an analog signal to a 12-bit serial output based on a precision internal reference. The control logic provides easy interface to microprocessors and DSPs through 3-wire connections.

Start of conversion is controlled by the CONV input. At the start of conversion the successive approximation register (SAR) is reset. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit capacitive DAC output is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 1, the A_{IN} input connects to the sample-and-hold capacitor during the acquired phase and the comparator offset is nulled by the feedback switch. In this acquire phase, a minimum delay of 200ns will provide enough time for the sample-and-hold capacitor to acquire the analog signal. During the convert phase, the comparator feedback switch opens, putting the comparator into the compare mode. The input switches C_{SAMPLE} to ground, injecting the analog input charge onto the summing junction. This input charge is successively compared with the binary-weighted charges supplied by the capacitive DAC. Bit decisions are made by the high speed comparator. At the end of a conversion, the DAC output balances the A_{IN} input charge. The SAR contents (a 12-bit data word) which represent the A_{IN}, are output through the serial pin D_{OUT}.

Driving the Analog Input

The analog input of the LTC1400 is easy to drive. It draws only one small current spike while charging the sample-and-hold capacitor at the end of conversion. During conversion, the analog input draws only a small leakage current. The only requirement is that the amplifier driving the analog input must settle after the small current spike before the next conversion starts. Any op amp that settles in 200ns to small current transients will allow maximum speed operation. If a slower op amp is used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's A_{IN} input include LT®1006, LT1007, LT1220, LT1223 and LT1224 op amps.

Internal Reference

The LTC1400 has an on-chip, temperature compensated, curvature corrected, bandgap reference, which is factory trimmed to 2.42V. It is internally connected to the DAC and is available at Pin 3 to provide up to 1mA of current to an external load. For minimum code transition noise, the reference output should be decoupled with a capacitor to filter wideband noise from the reference (10µF tantalum in parallel with a 0.1µF ceramic). The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment in bipolar mode. The V_{REF} pin must be driven to at least 2.45V to prevent conflict with the internal reference. The reference should not be driven to more than 5V. Figure 2 shows an LT1006 op amp driving the reference

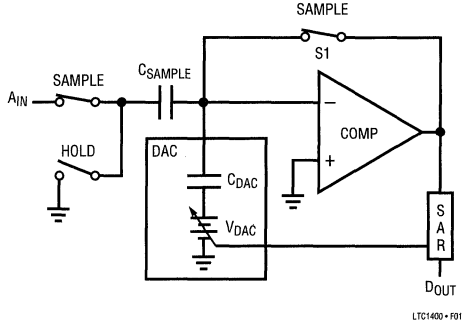


Figure 1. A_{IN} Input

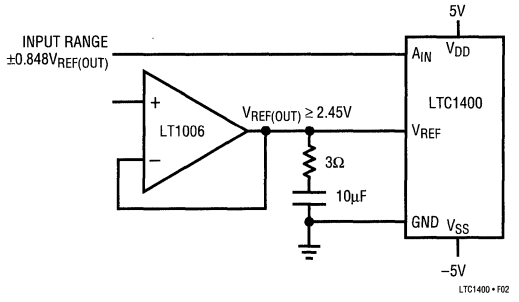


Figure 2. Driving the V_{REF} with the LT1006 Op Amp

APPLICATIONS INFORMATION

pin. Figure 3 shows a typical reference, the LT1019A-5 connected to the LTC1400. This will provide an improved drift (equal to the maximum 5ppm/°C of the LT1019A-5) and a ±4.231V full scale.

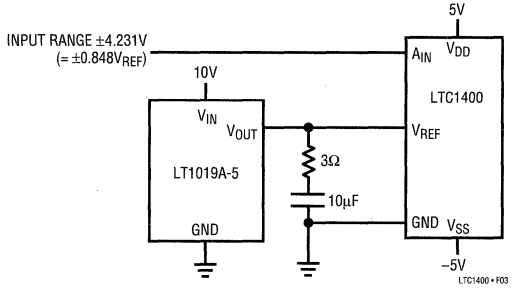


Figure 3. Supplying a 5V Reference Voltage to the LTC1400 with the LT1019A-5

UNIPOLAR / BIPOLAR OPERATION AND ADJUSTMENT

Figure 4 shows the ideal input/output characteristics for LTC1400. The code transitions occur midway between successive integer LSB values (i.e., 0.5LSB, 1.5LSB, 2.5LSB, ... FS – 1.5LSB). The output code is naturally binary with 1LSB = 4.096/4096 = 1mV. Figure 5 shows the input/output transfer characteristics for the bipolar mode in two's complement format.

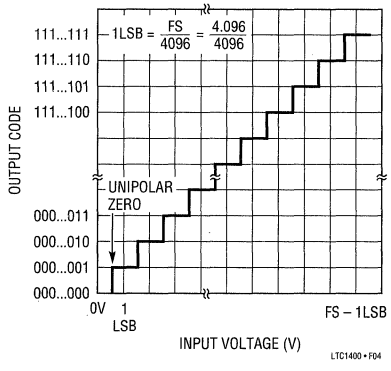


Figure 4. LTC1400 Unipolar Transfer Characteristics

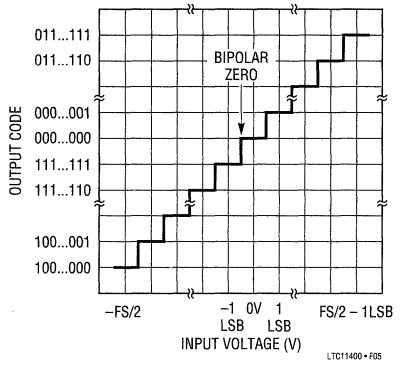


Figure 5. LTC1400 Bipolar Transfer Characteristics

Unipolar Offset and Full-Scale Error Adjustments

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 6a shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving A_{IN} (i.e., A1 in Figure 6b). For zero offset error, apply 0.5mV (i.e., 0.5LSB) at the input and adjust the offset trim until the LTC1400 output code flickers between 0000 0000 0000 and 0000 0000 0001. For zero full-scale error, apply an analog input of 4.0945V (FS – 1.5LSB or last code transition) at the input and adjust R5 until the LTC1400 output code flickers between 1111 1111 1110 and 1111 1111 1111.

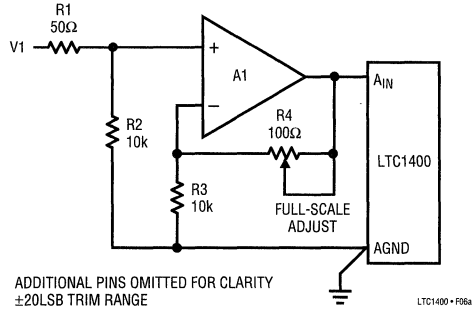


Figure 6a. Full-Scale Adjust Circuit

APPLICATIONS INFORMATION

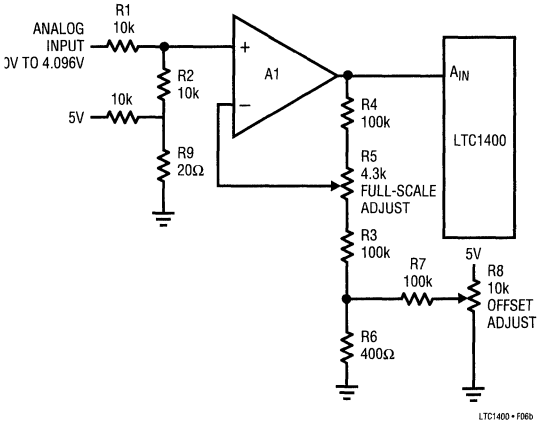


Figure 6b. LTC1400 Offset and Full-Scale Adjust Circuit

Bipolar Offset and Full-Scale Error Adjustments

Bipolar offset and full-scale errors are adjusted in a similar fashion to the unipolar case. Bipolar offset error adjustment is achieved by trimming the offset of the op amp driving the analog input of the LTC1400 while the input voltage is 0.5LSB below ground. This is done by applying an input voltage of –0.5mV (–0.5LSB) to the input in Figure 6c and adjusting the op amp until the ADC output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.0465V (FS – 1.5LSBs) is applied to the input and R5 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

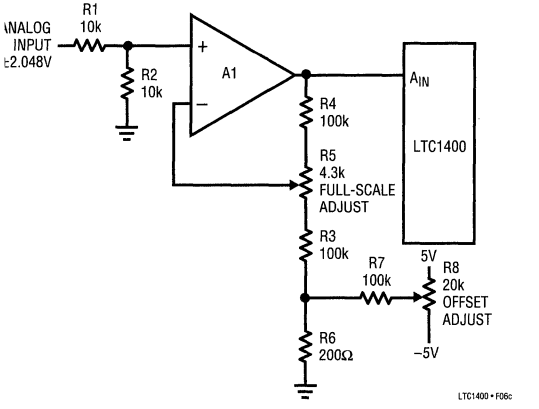


Figure 6c. LTC1400 Bipolar Offset and Full-Scale Adjust Circuit

BOARD LAYOUT AND BYPASSING

Wire-wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1400, a printed circuit board is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by GND.

High quality tantalum and ceramic bypass capacitors should be used at the V_{CC} and V_{REF} pins as shown in the Typical Application on the first page of this data sheet. For the bipolar mode, a 0.1µF ceramic provides adequate bypassing for the V_{SS} pin. The capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Input signal leads to A_{IN} and signal return leads from GND (Pin 4) should be kept as short as possible to minimize noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible.

Figure 7 shows the recommended system ground connections. All analog circuitry grounds should be terminated at the LTC1400 GND pin. The ground return from the LTC1400

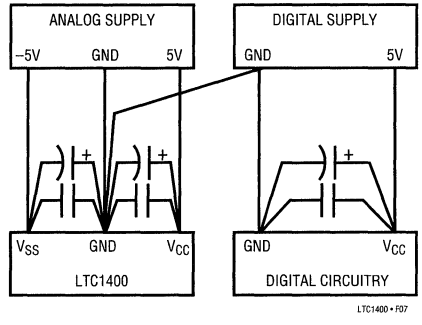


Figure 7. Power Supply Connection

APPLICATIONS INFORMATION

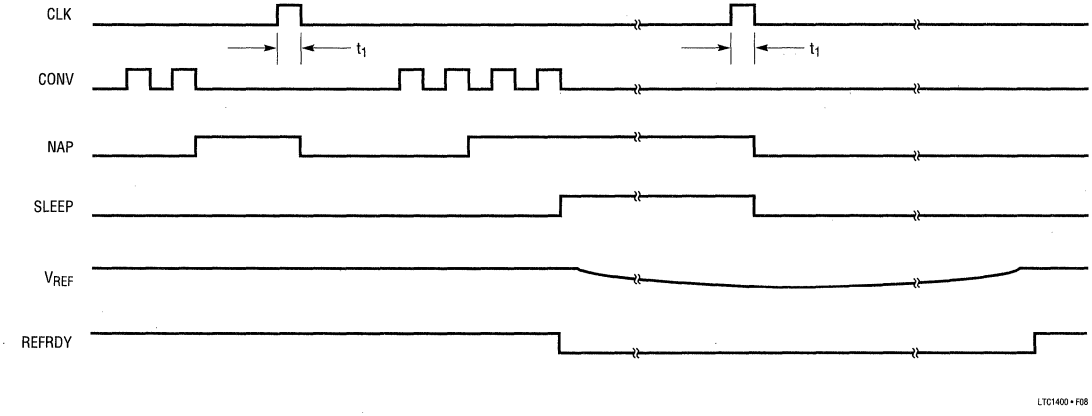
Pin 4 to the power supply should be low impedance for noise free operation. Digital circuitry grounds must be connected to the digital supply common.

In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a Wait state during conversion or by using three-state buffers to isolate the ADC data bus.

Power-Down Mode

Upon power-up, the LTC1400 is initialized to the active state and is ready for conversion. However, the chip can be easily placed into the NAP or SLEEP mode by exercising the right combination of CLK and CONV signal. In the NAP mode all power is off except the internal reference, which is still active and provides 2.42V output voltage to the other circuitry. In this mode, the ADC draws only 6mW of power instead of 75mW (for minimum power, the logic inputs must be within 500mV of the supply rails). The wake-up time from the NAP mode to the active mode is 350ns. In the SLEEP mode, the power consumption is reduced to minimum by cutting off the supply to all internal circuitry including the reference. Figure 8 shows the ways to power down LTC1400. The chip can enter the NAP mode by keeping the CLK signal low and pulsing the CONV signal twice. For SLEEP mode operation, CONV signal should be activated four times while CLK is kept low.

The LTC1400 can be returned to active mode easily. This can be achieved by pulsing the CLK signal. During the transition from SLEEP mode to active mode, the V_{REF} voltage ramp-up time is a function of the loading conditions. With a 10µF bypass capacitor, the wake-up time from SLEEP mode is typically 4ms. A REFRDY signal will be activated once the reference has settled and is ready for A/D conversion. This REFRDY bit is output to the D_{OUT} pin before the rest of the A/D converted code.



NOTE: NAP AND SLEEP ARE INTERNAL SIGNALS. REFRDY APPEARS AS A BIT IN THE D_{OUT} WORD.

Figure 8. NAP Mode and SLEEP Mode Waveforms

IPPLICATIONS INFORMATION

IGITAL INTERFACE

he digital interface requires only three digital lines. CLK nd CONV are both inputs, and the D_{OUT} output provides ıe conversion result in serial form.

igure 9 shows the digital timing diagram of the LTC1400 uring the A/D conversion. The CONV rising edge starts ıe conversion. Once initiated, it can not be restarted until the conversion is completed. If the time from CONV signal to CLK rising edge is less than t_2, the digital output will be delayed by one clock cycle.

The digital output data is updated on the rising edge of the CLK line. D_{OUT} data should be captured by the receiving system on the rising CLK edge. Data remains valid for a minimum time of t_{10} after the rising CLK edge to allow capture to occur.

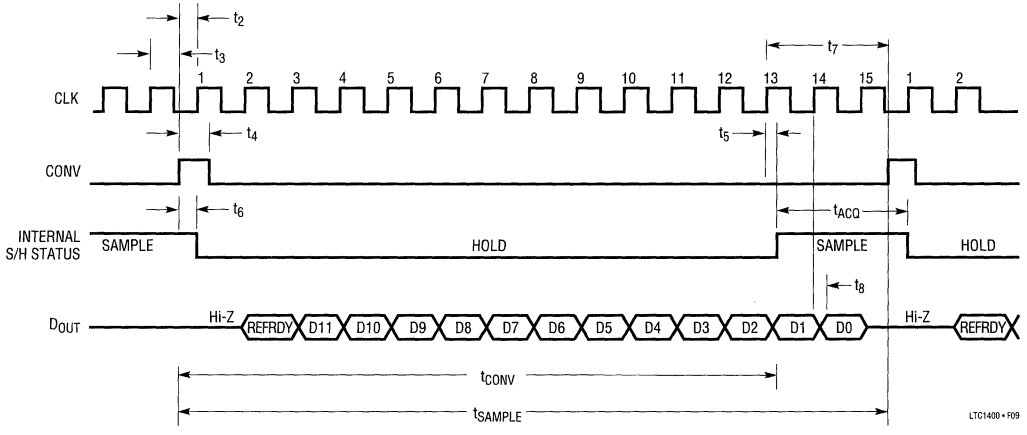


Figure 9. ADC Digital Timing Diagram

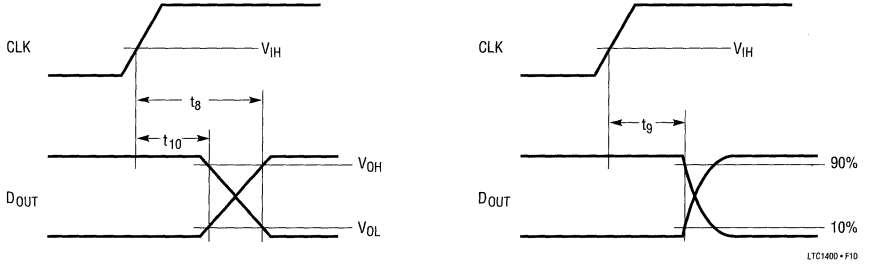


Figure 10. CLK to D_{OUT} Delay

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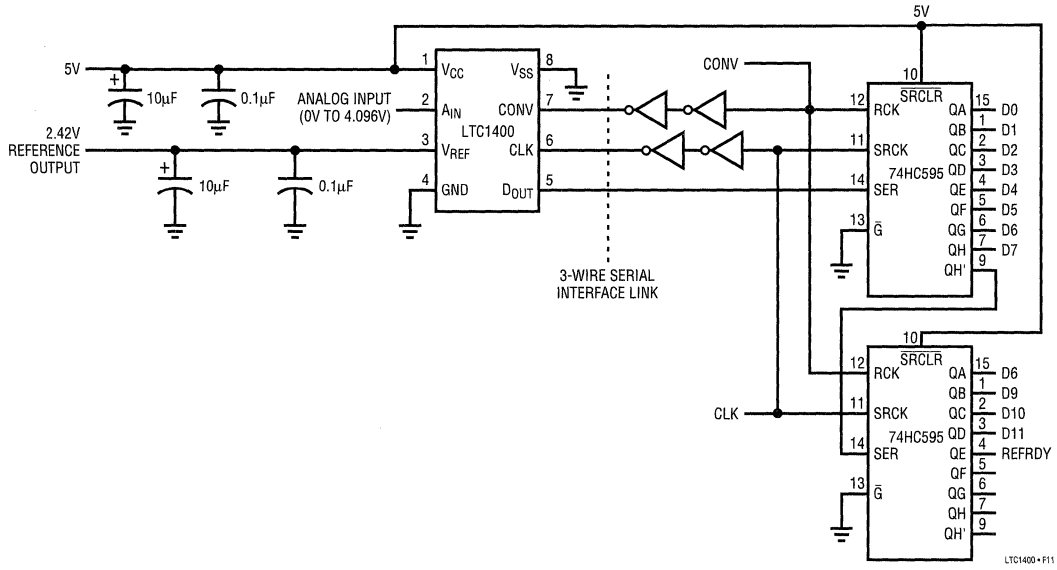
TYPICAL APPLICATION

LTC1400 with Parallel Output



RELATED PARTS

12-Bit Parallel Output ADCs

PART NUMBER	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
LTC1272	250ksps	75mW	Single 5V, 7572 Upgrade
LTC1273/LTC1275/LTC1276	300ksps	75mW	With Clock and Reference
LTC1274/LTC1277	100ksps	10mW	Low Power ADCs with 1µA Shutdown
LTC1278/LTC1279	500/600ksps	75mW	70dB at Nyquist, Low Power, Single 5V
LTC1282	140ksps	12mW	3V or ±3V ADC with Clock and Reference
LTC1410	1.25Msps	160mW	70dB at Nyquist, Differential Input

12-Bit Serial Output ADCs

PART NUMBER	VCC	SAMPLE RATE	POWER DISSIPATION	DESCRIPTION
LTC1285/LTC1288	3V	7.5/6.6ksps	0.48mW	3V, One or Two Input, Micropower, SO-8
LTC1286/LTC1298	5V	12.5/11.1ksps	1.25mV	One or Two Input, Micropower, SO-8
LTC1290	5/±5V	50ksps	30mW	8 Input, Full-Duplex Serial I/O
LTC1296	5/±5V	46.5ksps	30mW	8 Input, Half-Duplex Serial I/O, Power Shutdown Output

LTC1410

12-Bit, 1.25Msps Sampling A/D Converter with Shutdown

April 1995

FEATURES

Complete 1.25Msps ADC
Power Dissipation: 160mW (Typ)
Nap (7mW) and Sleep (10μW) Shutdown Modes
Operates with Internal 25ppm/°C Reference
or External Reference
True Differential Inputs Reject Common-Mode Noise
71dB S/(N + D) and 82dB THD at Nyquist
20MHz Full Power Bandwidth
±2.5V Bipolar Input Range
Internal Synchronized Clock
28-Pin SO Wide Package

APPLICATIONS

Telecommunications
Digital Signal Processing
Multiplexed Data Acquisition Systems
High Speed Data Acquisition
Spectrum Analysis
Imaging Systems

DESCRIPTION

The LTC®1410 is a 650ns, 1.25Msps, sampling 12-bit A/D converter which draws only 160mW from ±5V supplies. This easy-to-use device includes a high dynamic range sample-and-hold, a precision reference and a trimmed internal clock. Two digitally selectable power shutdown modes provide flexibility for low power systems.

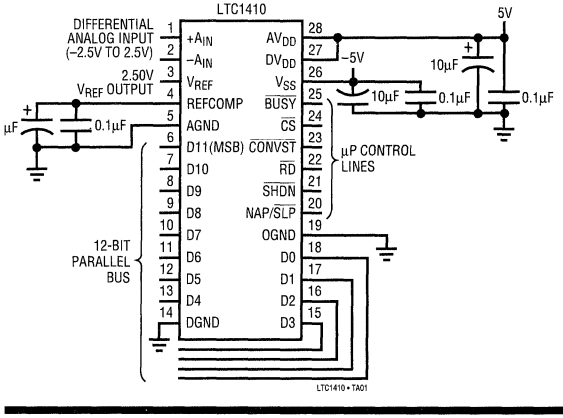
The LTC1410's full-scale input range is ±2.5V. Maximum DC specs include ±1LSB INL and ±1LSB DNL over temperature. Outstanding AC performance includes 71dB S/(N + D) and 82dB THD at the Nyquist input frequency of 625kHz.

The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 20MHz bandwidth. The 60dB common-mode rejection allows users to eliminate ground loops and common-mode noise by measuring signals differentially from the source.

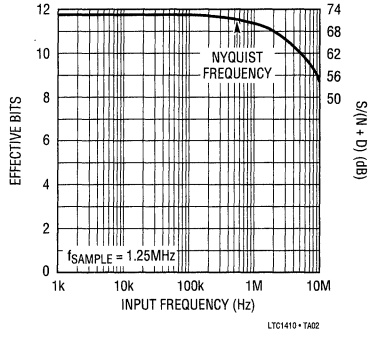
The internal clock is trimmed for 750ns maximum conversion time. The clock automatically synchronizes to each sample command. A separate convert start input and a data ready signal ($\overline{BUSY}$) ease connections to FIFOs, DSPs and microprocessors.

TYPICAL APPLICATION

Complete 1.25MHz, 12-Bit Sampling A/D Converter



Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency



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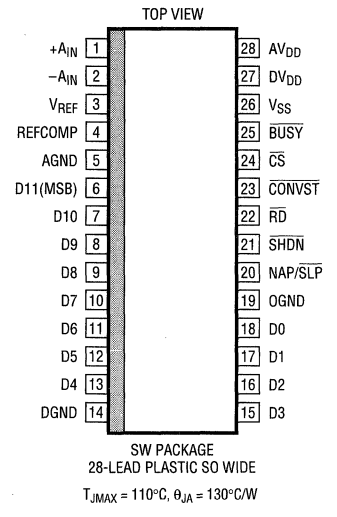
ABSOLUTE MAXIMUM RATINGS

AV_{DD} = DV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Negative Supply Voltage (V_{SS}) ..... –6V
Total Supply Voltage (V_{DD} to V_{SS}) 12V
Analog Input Voltage
(Note 3) ..... V_{SS} – 0.3V to V_{DD} + 0.3V
Digital Input Voltage (Note 4) ..... V_{SS} – 0.3V to 10V
Digital Output Voltage ..... – 0.3V to V_{DD} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
LTC1410C ..... 0°C to 70°C
LTC1410I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



ORDER PART NUMBER

LTC1410CSW
LTC1410ISW

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

With Internal Reference (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Resolution (No Missing Codes)		●	12			Bi
Integral Linearity Error	(Note 7)	●			±1	LS
Differential Linearity Error		●			±1	LS
Offset Error	(Note 8)				±6	LS
		●			±8	LS
Full-Scale Error					±15	LS
Full-Scale Tempco	$I_{OUT(REF)}$ = 0	●		±15		ppm/

ANALOG INPUT

(Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Analog Input Range (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V, –5.25V ≤ V_{SS} ≤ –4.75V	●		±2.5	·	
I_{IN}	Analog Input Leakage Current	$\overline{CS}$ = High	●			±1	μ
C_{IN}	Analog Input Capacitance	Between Conversions			17		p
		During Conversions			5		p
t_{ACQ}	Sample-and-Hold Acquisition Time		●		50	100	n
t_{AP}	Sample-and-Hold Acquisition Delay Time				–1.5		n
t_{jitter}	Sample-and-Hold Acquisition Delay Time Jitter				5		ps$_{RM}$
CMRR	Analog Input Common-Mode Rejection Ratio	–2.5V < V_{CM} < 2.5V, DC to 1MHz			60		d

DYNAMIC ACCURACY (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	100kHz Input Signal (Note 12) 600kHz Input Signal (Note 12)	● ●	70 68			dB dB
THD	Total Harmonic Distortion	100kHz Input Signal, First Five Harmonics 600kHz Input Signal, First Five Harmonics	 ●		−85 −82	 −74	dB dB
	Peak Harmonic or Spurious Noise	600kHz Input Signal	●		−84	−74	dB
IMD	Intermodulation Distortion	f_{IN1} = 29.37kHz, f_{IN2} = 32.446kHz			−84		dB
	Full Power Bandwidth				20		MHz
	Full Linear Bandwidth	(S/(N + D) ≥ 68dB)			2.5		MHz

INTERNAL REFERENCE CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF} Output Voltage	I_{OUT} = 0		2.480	2.500	2.520	V
V_{REF} Output Tempco	I_{OUT} = 0	●		±15		ppm/°C
V_{REF} Line Regulation	4.75V ≤ V_{DD} ≤ 5.25V −5.25V ≤ V_{SS} ≤ −4.75V			0.01 0.01		LSB/V LSB/V
V_{REF} Output Resistance	0.1V ≤ $\lvert I_{OUT} \rvert$ ≤ 0.1mA			2		kΩ
REFCOMP Output Voltage	I_{OUT} = 0			4.06		V

DIGITAL INPUTS AND DIGITAL OUTPUTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
IIN	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±10	µA
CIN	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V I_O = −10µA I_O = −200µA	 ●	 4.0	 4.5	 	 V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V I_O = 160µA I_O = 1.6mA	 ●		 0.05 0.10	 0.4	 V V
IOZ	High-Z Output Leakage D11 to D0	V_{OUT} = 0V to V_{DD}, $\overline{CS}$ High	●			±10	µA
COZ	High-Z Output Capacitance D11 to D0	$\overline{CS}$ High (Note 9)	●			15	pF
ISOURCE	Output Source Current	V_{OUT} = 0V			−10		mA
ISINK	Output Sink Current	V_{OUT} = V_{DD}			10		mA

POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VDD	Positive Supply Voltage	(Notes 10, 11)		4.75		5.25	V
VSS	Negative Supply Voltage	(Note 10)		−4.75		−5.25	V
IDD	Positive Supply Current Nap Mode Sleep Mode	$\overline{CS}$ High $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V $\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V	●		12 1.5 1.0	16 2.3	mA mA µA

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POWER REQUIREMENTS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SS}	Negative Supply Current	$\overline{CS}$ High	●		20	30	mA
	Nap Mode	$\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V			10	200	µA
	Sleep Mode	$\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V			1		µA
P_{DISS}	Power Dissipation	$\overline{CS}$ High			160	230	mW
	Nap Mode	$\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 5V			7.5	12	mW
	Sleep Mode	$\overline{SHDN}$ = 0V, NAP/$\overline{SLP}$ = 0V			0.01		mW

TIMING CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SAMPLE(MAX)}$	Maximum Sampling Frequency		●	1.25			MHz
$t_{SAMPLE(MIN)}$	Conversion and Acquisition Time		●			800	ns
t_{CONV}	Conversion Time		●			750	ns
t_{ACQ}	Acquisition Time		●			100	ns
t_1	$\overline{CS}$ to $\overline{RD}$ Setup Time	(Notes 9, 10)	●	0			ns
t_2	$\overline{CS}$↓ to $\overline{CONVST}$↓ Setup Time	(Notes 9, 10)	●	10			ns
t_3	NAP/$\overline{SLP}$↑ to $\overline{SHDN}$↓ Setup Time	(Notes 9, 10)	●	10			ns
t_4	$\overline{SHDN}$↑ to $\overline{CONVST}$↓ Wake-Up Time	Nap Mode (Note 10)			200		ns
		Sleep Mode, $C_{REFCOMP}$ = 10µF			10		ms
t_5	$\overline{CONVST}$ Low Time	(Notes 10, 11)	●	40			ns
t_6	$\overline{CONVST}$ to $\overline{BUSY}$ Delay	C_L = 25pF			10		ns
			●			50	ns
t_7	Data Ready Before $\overline{BUSY}$↑			20	35		ns
			●	15			ns
t_8	Delay Between Conversions	(Note 10)	●	50			ns
t_9	Wait Time $\overline{RD}$↓ After $\overline{BUSY}$↑		●	−5			ns
t_{10}	Data Access Time After $\overline{RD}$↓	C_L = 25pF			15	25	ns
			●			35	ns
		C_L = 100pF			20	35	ns
			●			50	ns
t_{11}	Bus Relinquish Time				8	20	ns
		Commercial	●			25	ns
		Industrial	●			30	ns
t_{12}	$\overline{RD}$ Low Time		●	t_{10}			ns
t_{13}	$\overline{CONVST}$ High Time		●	40			ns
t_{14}	Aperture Delay of Sample-and-Hold				−1.5		ns

The ● indicates specifications which apply over the full operating temperature range; all other limits and typicals T_A = 25°C.

Note 1: Absolute maximum ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below V_{SS} or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} or above V_{DD} without latch-up.

Note 4: When these pin voltages are taken below V_{SS} they will be clamped by internal diodes. This product can handle input currents greater than 100mA below V_{SS} without latch-up. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, V_{SS} = −5V, f_{SAMPLE} = 1.25MHz, $t_r = t_f$ = 5ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended $+A_{IN}$ input with $-A_{IN}$ grounded.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from −0.5LSB when the output code flickers between 0000 0000 0000 and 1111 1111 1111.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

TIMING CHARACTERISTICS

Note 11: The falling $\overline{CONVST}$ edge starts a conversion. If $\overline{CONVST}$ returns high at a critical point during the conversion it can create small errors. For best performance ensure that $\overline{CONVST}$ returns high either within 425ns after conversion start or after $\overline{BUSY}$ rises.

Note 12: Signal-to-noise ratio (SNR) is measured at 100kHz and distortion is measured at 600kHz. These results are used to calculate signal-to-noise plus distortion (SINAD).

PIN FUNCTIONS

+A_{IN} (Pin 1): Analog Input, ±2.5V. The ADC converts the difference voltage between +A_{IN} and –A_{IN} with a differential range of ±2.5V.

–A_{IN} (Pin 2): Negative Analog Input, ±2.5V.

V_{REF} (Pin 3): 2.500V Reference Output.

REFCOMP (Pin 4): 4.06V Reference Compensation Pin. Bypass to AGND (10µF tantalum in parallel with 0.1µF ceramic).

AGND (Pin 5): Analog Ground.

D11 to D4 (Pins 6 to 13): Three-State Data Outputs.

DGND (Pin 14): Digital Ground for Internal Logic.

D3 to D0 (Pins 15 to 18): Three-State Data Outputs.

DGND (Pin 19): Digital Ground for Output Drivers.

NAP/$\overline{SLP}$ (Pin 20): Power Shutdown Mode. Defines power down mode when $\overline{SHDN}$ goes low. High for quick wake-up Nap mode. Low for Sleep.

$\overline{SHDN}$ (Pin 21): Power Shutdown.

$\overline{RD}$ (Pin 22): Read Input. This enables the output drivers when $\overline{CS}$ is low.

$\overline{CONVST}$ (Pin 23): Conversion Start Signal. This active low signal starts a conversion on its falling edge when $\overline{CS}$ is low.

$\overline{CS}$ (Pin 24): The Chip Select input must be low for the ADC to recognize $\overline{CONVST}$ and $\overline{RD}$ inputs.

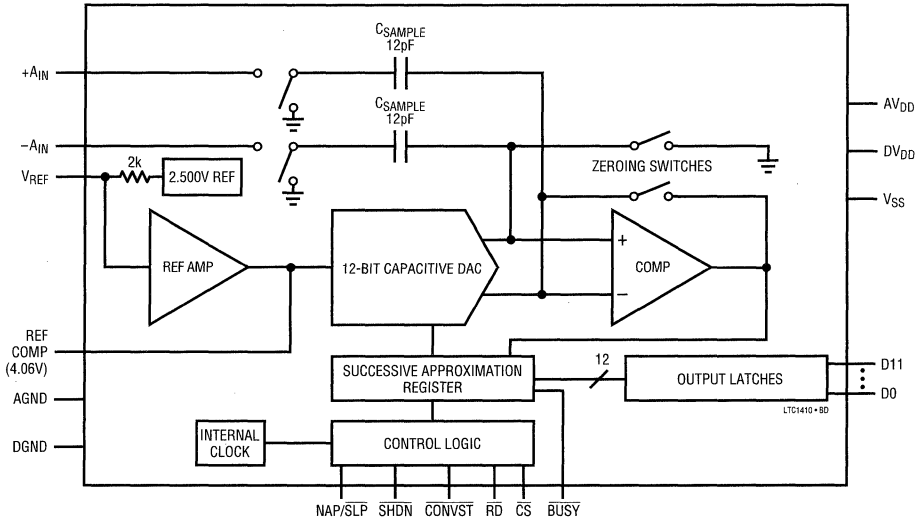
$\overline{BUSY}$ (Pin 25): The $\overline{BUSY}$ output shows the converter status. It is low when a conversion is in progress. Data valid on the rising edge of $\overline{BUSY}$.

V_{SS} (Pin 26): –5V Negative Supply. Bypass to AGND with 10µF tantalum in parallel 0.1µF ceramic.

DV_{DD} (Pin 27): 5V Positive Supply. Short to pin 28.

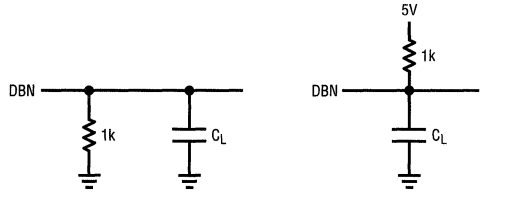
AV_{DD} (Pin 28): 5V Positive Supply. Bypass to AGND with 10µF tantalum in parallel with 0.1µF ceramic.

FUNCTIONAL BLOCK DIAGRAM

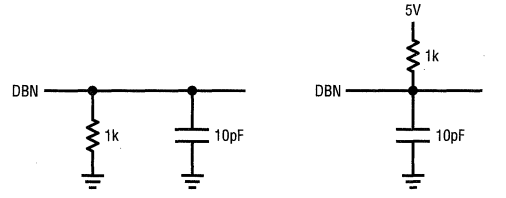


TEST CIRCUITS

Load Circuits for Access Timing



Load Circuits for Output Float Delay



APPLICATIONS INFORMATION

Driving the Analog Input

The differential analog inputs of the LTC1410 are easy to drive. The inputs may be driven differentially or as a single-ended input (i.e., the $-A_{IN}$ input is grounded). The $+A_{IN}$ and $-A_{IN}$ inputs are sampled at the same instant. Any unwanted signal that is common-mode to both inputs will be reduced by the 60dB common-mode rejection of the sample-and-hold circuit. The inputs draw only one small current spike while charging the sample-and-hold capacitors at the end of conversion. During conversion the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low then the LTC1410 inputs can be driven directly. As source impedance increases so will acquisition time (see Figure 1). For minimum acquisition time, with high source impedance, a buffer amplifier should be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 100ns for full throughput rate).

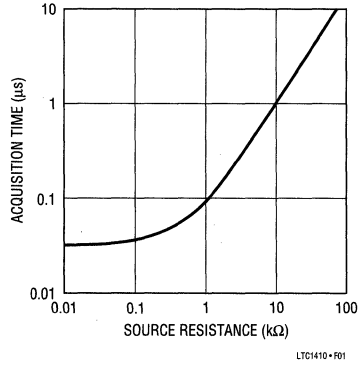


Figure 1 Acquisition Time vs Source Resistance

Choosing an input amplifier is easy if a few requirements are taken into consideration, First, choose an amplifier that has a low output impedance (< 100Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of +1 and has a closed-loop bandwidth of 50MHz, then the output impedance at 50MHz must be less than 100Ω. The second requirement is that the closed-loop bandwidth must be greater than 20MHz to ensure adequate small-signal settling for full throughput rate. If slower op amps are used, more settling time can be provided by increasing the time between conversions. Suitable devices capable of driving the ADC's inputs include the LT®1360, LT1220, LT1223 and LT1224 op amps.

The noise and the distortion of the input amplifier must also be considered since they will add to the LTC1410 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 20MHz. Any noise that is present at the analog inputs will be summed over this entire bandwidth. Noisy input signals should be filtered prior to the analog inputs to minimize noise. A simple one-pole RC filter is usually sufficient. For example, a 1000pF capacitor from $+A_{IN}$ to ground and a 100Ω source resistor will limit the input bandwidth to 1.6MHz. Simple RC filters work well for AC applications, but they will limit the transient response. Raising the bandwidth of the RC filter will improve the transient response. For full speed operation, fast settling, low noise amplifiers should be chosen.

APPLICATIONS INFORMATION

Internal Reference

The LTC1410 has an on-chip, temperature compensated, curvature corrected, bandgap reference which is factory trimmed to 2.50V. It is connected internally to a reference amplifier and is available at pin 3. A 2k resistor is in series with the output so that it can be easily overdriven in applications where an external reference is required. The reference buffer compensation pin, REFCOMP (pin 4), must be bypassed with a capacitor to ground. The reference is stable with capacitors of 1µF or greater. For the best noise performance, Linear Technology recommends 10µF in parallel with 0.1µF ceramic (see Figure 2).

The V_{REF} pin can be driven with a DAC or other means to provide input span adjustment. The reference should be kept in the range of 2.25V to 2.75V for specified linearity.

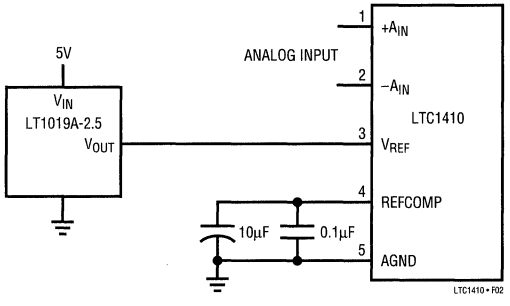


Figure 2. Using the LT1019-2.5 as an External Reference

Full-Scale and Offset Adjustment

Figure 3 shows the ideal input/output characteristics for the LTC1410. The code transitions occur midway between successive integer LSB values (i.e., –FS/2 + 0.5LSB, –FS/2 + 1.5LSB, –FS/2 + 2.5LSB,... FS/2 – 1.5LSB, FS/2 – 2.5LSB. The output is two's complement binary with 1LSB = FS/4096 = 5V/4096 = 1.22mV.

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 4 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset applied to the $-A_{IN}$ input. For zero offset error apply –0.61mV (i.e., –0.5LSB at $+A_{IN}$ and adjust the voltage at the $-A_{IN}$ input until the output code flickers between 0000 0000 0000 and 1111 1111 1111. For full-scale adjustment, an input voltage of 2.49817V (FS/2 – 1.5LSBs) is applied to A_{IN} and R2 is adjusted until the output code flickers between 0111 1111 1110 and 0111 1111 1111.

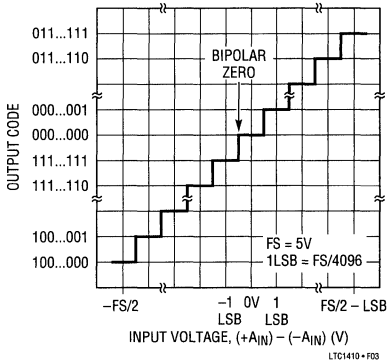


Figure 3. LTC1410 Transfer Characteristics

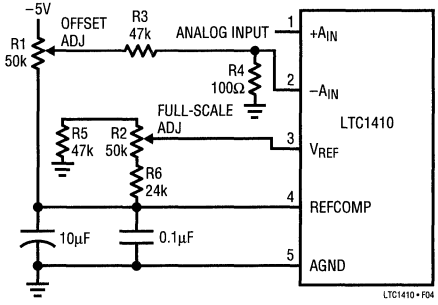


Figure 4. Offset and Full-Scale Adjust Circuit

BOARD LAYOUT AND BYPASSING

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1410, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. The analog input should be screened by AGND.

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APPLICATIONS INFORMATION

High quality tantalum and ceramic bypass capacitors should be used at the V_{DD}, V_{SS} and REFCOMP pins as shown in the Typical Application on the first page of this data sheet. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

The LTC1410 has differential inputs to minimize noise coupling. Common-mode noise on the $+A_{IN}$ and $-A_{IN}$ leads will be rejected by the input CMRR. The $-A_{IN}$ input can be used as a ground sense for the $+A_{IN}$ input; the LTC1410 will hold and convert the voltage difference between $+A_{IN}$ and $-A_{IN}$. The leads to $+A_{IN}$ (pin 1) and $-A_{IN}$ (pin 2) should be kept as short as possible. In applications where this is not possible, the $+A_{IN}$ and $-A_{IN}$ traces should be run side by side to equalize coupling.

A single point analog ground separate from the logic system ground should be established with an analog ground plane at pin 5 (AGND) or as close as possible to the ADC. Pin 14 and pin 19 (ADC's DGND) and all other analog grounds should be connected to this single analog ground point. No other digital ground should be connected to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the successive approximation comparator. The problem can be eliminated by forcing the microprocessor into a wait state during conversion or by using three-state buffers to isolate the ADC data bus.

DIGITAL INTERFACE

The A/D converter is designed to interface with microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ control inputs are common to all peripheral memory interfacing.

Internal Clock

The A/D converter has an internal clock that eliminates the need of synchronization between the external clock and the $\overline{CS}$ and $\overline{RD}$ signals found in other ADCs. The internal clock is factory trimmed to achieve a typical conversion time of 0.65µs and a maximum conversion time over the full operating temperature range of 0.75µs. No external adjustments are required. The guaranteed maximum acquisition time is 100ns. In addition, throughput performance is also guaranteed at 800ns so that 1.25Msps is assured.

Power Shutdown

The LTC1410 provides two power shutdown modes, Nap and Sleep, to save power during inactive periods. The Nap mode reduces the power by 95% and leaves only the digital logic and reference powered up. The wake-up time from NAP to active is 200ns. Follow the setup time shown in Figure 5a to avoid inadvertently invoking sleep mode. In Sleep mode all bias currents are shut down and only leakage current remains, about 1µA. Wake-up time from Sleep mode is much slower since the reference circuit must power up and settle to 0.01% for full 12-bit accuracy. Sleep mode wake-up time is dependent on the value of the capacitor connected to the REFCOMP (pin 4). The wake-up time is 10ms with the recommended 10µF capacitor. (See Figure 5b).

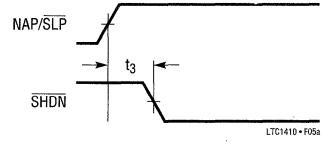

Figure 5a. NAP/$\overline{SLP}$ to $\overline{SHDN}$ Timing to Ensure Nap Mode

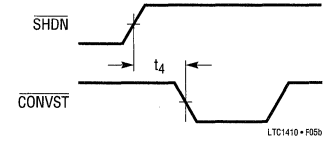

Figure 5b. $\overline{SHDN}$ to $\overline{CONVST}$ Wake-Up Timing

APPLICATIONS INFORMATION

Shutdown is controlled by pin 21 (SHDN), the ADC is in shutdown when it is low. The shutdown mode is selected with pin 20 (NAP/SLP); high selects NAP.

Timing and Control

Conversion start and data read operations are controlled by three digital inputs: $\overline{CONVST}$, $\overline{CS}$ and $\overline{RD}$. (See Figure 6.) A falling edge applied to the $\overline{CONVST}$ pin will start a conversion after the ADC has been selected (i.e., $\overline{CS}$ is low). Once initiated, it cannot be restarted until the conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output. $\overline{BUSY}$ is low during a conversion.

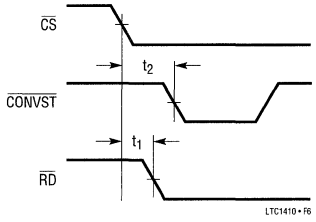

Figure 6. $\overline{CS}$ to $\overline{CONVST}$ Setup Timing

Figures 7 through 11 show several different modes of operation. In modes 1a and 1b (Figures 7 and 8) $\overline{CS}$ and $\overline{RD}$ are both tied low. The falling edge of $\overline{CONVST}$ starts the conversion. The data outputs are always enabled and data can be latched with the $\overline{BUSY}$ rising edge. Mode 1a shows operation with a narrow logic low $\overline{CONVST}$ pulse. Mode 1b shows a narrow logic high $\overline{CONVST}$ pulse.

In mode 2 (Figure 9) $\overline{CS}$ is tied low. The falling edge of $\overline{CONVST}$ signal again starts the conversion. Data outputs are in three-state until read by the MPU with the $\overline{RD}$ signal. Mode 2 can be used for operation with a shared MPU databus.

In slow memory and ROM modes (Figures 10 and 11) $\overline{CS}$ is tied low and $\overline{CONVST}$ and $\overline{RD}$ are tied together. The MPU starts the conversion and reads the output with the $\overline{RD}$ signal. Conversions are started by the MPU or DSP (no external sample clock).

In slow memory mode the processor applies a logic low to $\overline{RD}$ (= $\overline{CONVST}$) starting the conversion. $\overline{BUSY}$ goes low forcing the processor into a wait state. The previous conversion result appears on the data outputs. When the conversion is complete, the new conversion results appear on the data outputs; $\overline{BUSY}$ goes high releasing the processor, and the processor takes $\overline{RD}$ (= $\overline{CONVST}$) back high and reads the new conversion data.

In ROM mode, the processor takes $\overline{RD}$ (= $\overline{CONVST}$) low, starting a conversion and reading the previous conversion result. After the conversion is complete, the processor can read the new result and initiate another conversion.

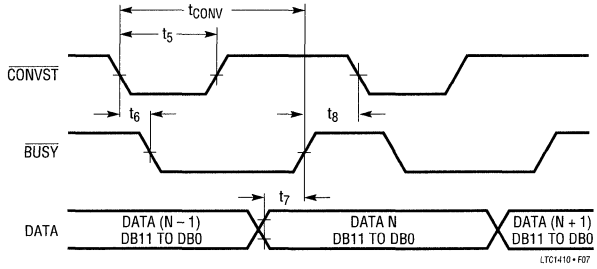

Figure 7. Mode 1a. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled
($\overline{CONVST}$ = ⊓⊔⊓⊔⊓⊔⊓)

APPLICATIONS INFORMATION

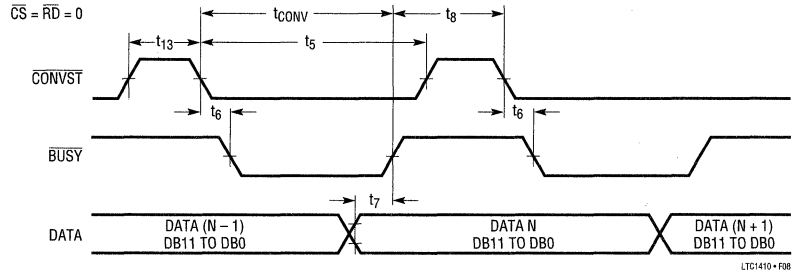

Figure 8. Mode 1b. $\overline{CONVST}$ Starts a Conversion. Data Outputs Always Enabled ($\overline{CONVST}$ = ⎍⎍⎍)

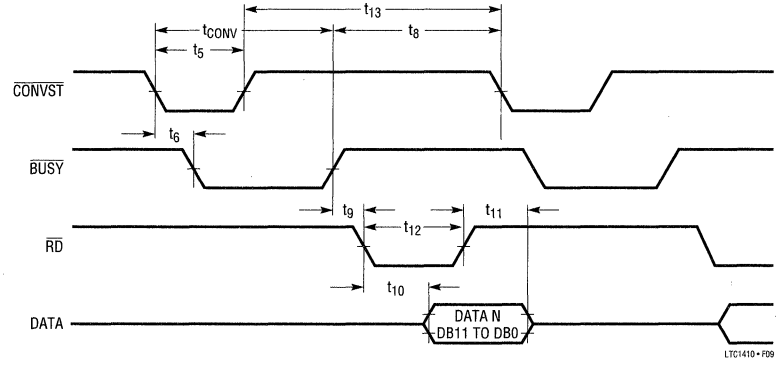

Figure 9. Mode 2. $\overline{CONVST}$ Starts a Conversion. Data is Read by $\overline{RD}$

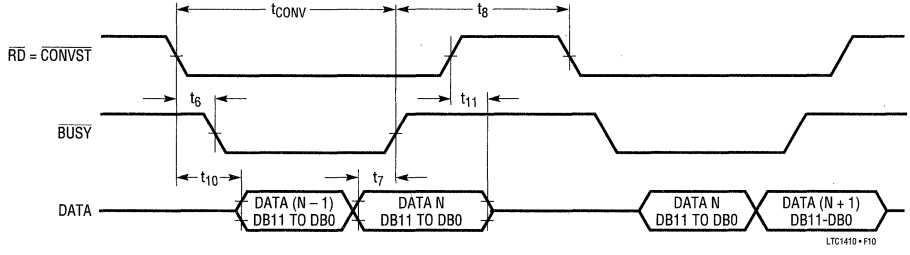

Figure 10. Slow Memory Mode Timing

APPLICATIONS INFORMATION

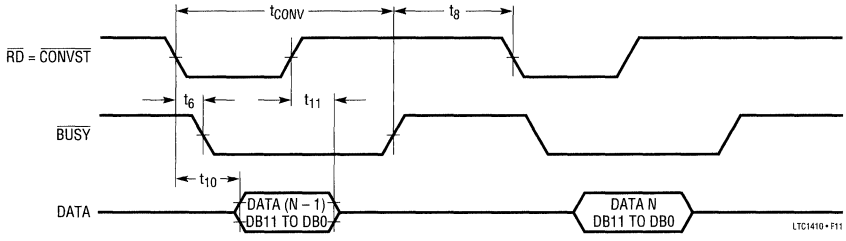

Figure 11. ROM Mode Timing

RELATED PARTS

12-Bit Sampling A/D Converters

PART NUMBER	SAMPLE RATE	DESCRIPTION	COMMENTS
LTC1273/75/76	300ksps	Complete 5V Sampling 12-Bit ADCs with 70dB SINAD at Nyquist	Lower Power and Cost Effective for $f_{SAMPLE} \leq 300$ksps
LTC1274/77	100ksps	Low Power 12-Bit ADCs with Nap and Sleep Mode Shutdown	Lowest Power for $f_{SAMPLE} \leq 100$ksps
LTC1278/79	500/600ksps	High Speed Sampling 12-Bit ADCs with Shutdown	Cost Effective 12-Bit ADCs — Best for 2-Pair HDSL
LTC1282	140ksps	Complete 3V 12-Bit ADCs with 12mW Power Dissipation	Fully Specified for 3V-Powered Applications

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LTC1443/LTC1444/LTC1445

Micropower Quad Comparators

May 1995

FEATURES

- **Ultra-Low Quiescent Current: 8.5µA Max Over Extended Temperature Range**
- **Reference Output Drives 0.01µF Capacitor**
- **Reference Output Can Source 100µA (Min)**
- Power Supplies
  - Single: 2V to 11V
  - Dual: ±1V to ±5.5V
- Input Voltage Range Includes Negative Supply
- Adjustable Hysteresis (LTC1444/LTC1445)
- TTL/CMOS Compatible Outputs
- Propagation Delay: 12µs (10mV Overdrive)
- No Crowbar Current
- 40mA Continuous Source Current
- Pin Compatible to MAX924 (LTC1443)

APPLICATIONS

- Battery-Powered Systems
- Threshold Detectors
- Window Comparators
- Oscillator Circuits

DESCRIPTION

The LTC®1443/LTC1444/LTC1445 quad micropower, low voltage comparators feature 8.5µA over extended temperature range. Four comparators and a reference draw less than 8.5µA supply current over temperature and include an internal reference (1.182V ±1% for LTC1443, 1.221V ±1% for LTC1444/LTC1445), programmable hysteresis (LTC1444/LTC1445) and TTL/CMOS outputs that sink and source current. The reference output can drive up to a 0.01µF capacitor without oscillation.

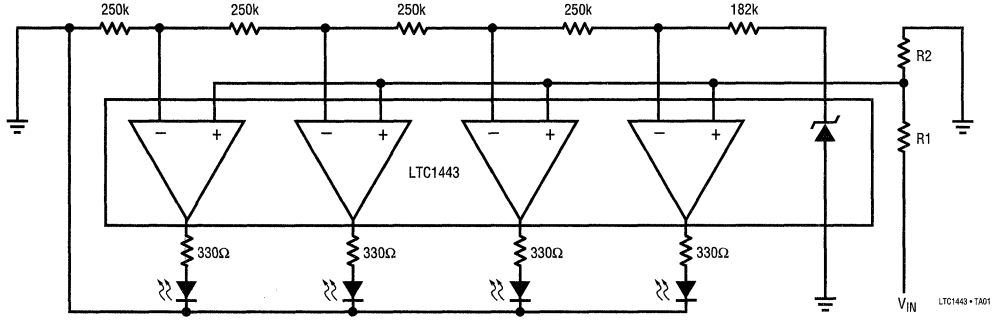
Ideal for 3V or 5V single supply applications, the LTC1443/LTC1444/LTC1445 operate from a single 2V to 11V supply or a ±1V to ±5.5V dual supply; each comparator's input voltage range swings from the negative supply rail to within 1.3V of the positive supply.

The LTC1443/LTC1445's unique output stage continuously sources as much as 40mA. The LTC1444 is an open-drain output with active pull-down NMOS. By eliminating power supply glitches that commonly occur when comparators change logic states, the LTC1443/LTC1444/LTC1445 minimize parasitic feedback, which makes them easier to use.

Simply by using the HYST pin and two resistors the LTC1444/LTC1445 provide a unique and simple method for adding hysteresis without feedback and complicated equations.

TYPICAL APPLICATION

Bar Graph Level Gauge

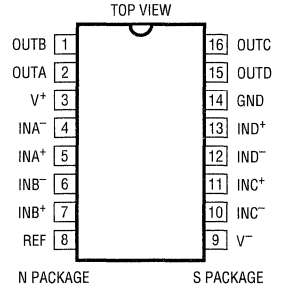


ABSOLUTE MAXIMUM RATINGS

Voltage:
V^+ to V^-, V^+ to GND, GND to V^- ..... 12V to –0.3V
IN^+, IN^-, HYST ..... (V^+ + 0.3V) to (V^- – 0.3V)
OUT, REF ..... (V^+ + 0.3V) to (V^- – 0.3V)
Lead Temperature Range (Soldering, 10 sec)..... 300°C

Current:
REF 20mA
OUT 50mA
IN^+, IN^-, HYST 20mA
Storage Temperature Range ..... –65°C to 150°C

PACKAGE/ORDER INFORMATION

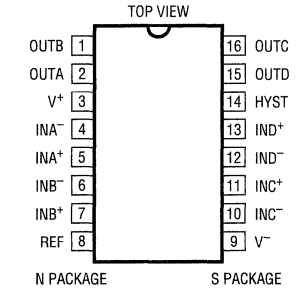


N PACKAGE 16-LEAD PDIP
S PACKAGE 16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 90°C/W (S)

ORDER PART NUMBER

LTC1443CN
LTC1443CS



N PACKAGE 16-LEAD PDIP
S PACKAGE 16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 70°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 90°C/W (S)

ORDER PART NUMBER

LTC1444CN
LTC1444CS
LTC1445CN
LTC1445CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V^+ = 5V, V^- = GND = 0V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+	Supply Voltage Range		●	2.0		11.0	V
I_{CC}	Supply Current	IN^+ = IN^- + 80mV			5.5	6.5	µA
		HYST = REF (LTC1444/LTC1445)	●		5.5	8.5	µA
V_{OS}	Comparator Input Offset Voltage	V_{CM} = 2.5V				±10	mV
I_{IN}	Input Leakage Current		●			±1	nA
V_{CM}	Comparator Input Common-Mode Range		●	V^-		V^+ – 1.3	V
CMRR	Common-Mode Rejection Ratio	V^- to (V^+ – 1.3V)	●		0.1	1.0	mV/V
PSRR	Power Supply Rejection Ratio	V^+ = 2.5V to 11V	●		0.1	1.0	mV/V
t_{PD}	Propagation Delay	Overdrive = 10mV, C_{OUT} = 100pF			12		µs
		Overdrive = 100mV, C_{OUT} = 100pF			4		µs
V_{HYST}	Hysteresis Input Voltage Range	LTC1444/LTC1445		REF – 50mV		REF	V
V_{OH}	Output High Voltage	I_{SOURCE} = 17mA; LTC1443/LTC1445	●	4.6			V
V_{OL}	Output Low Voltage	I_{SINK} = 1.8mA	●			0.4	V
V_{REF}	Reference Voltage	No Load, LTC1443C	●	1.170	1.182	1.194	V
		No Load, LTC1445C/LTC1444C	●	1.209	1.221	1.233	V
I_{SOURCE}	Reference Output Source Current	LTC1443	●	100	200		µA
		LTC1444/LTC1445	●	100	200		µA
I_{SINK}	Reference Output Sink Current	LTC1443/LTC1444/LTC1445	●	4	15		µA
Noise	100Hz to 100kHz, REF	LTC1443/LTC1444/LTC1445			100		μV_{RMS}

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ELECTRICAL CHARACTERISTICS

V^+ = 3V, V^- = GND = 0V, T_A = 25°C unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+	Supply Voltage Range		●	2.0		11.0	V
I_{CC}	Supply Current	$IN^+ = IN^- + 80mV$			5.2	6.2	µA
		HYST = REF (LTC1444/LTC1445)	●			8.0	µA
V_{OS}	Comparator Input Offset Voltage	V_{CM} = 1.5V				±10	mV
I_{IN}	Input Leakage Current		●			±1	nA
V_{CM}	Comparator Input Common-Mode Range		●	V^-		$V^+ - 1.3$	V
CMRR	Common-Mode Rejection Ratio	V^- to (V^+ –1.3V)	●		0.1	1.0	mV/V
PSRR	Power Supply Rejection Ratio	V^+ = 2.5V to 11V	●		0.1	1.0	mV/V
t_{PD}	Propagation Delay	Overdrive = 10mV, C_{OUT} = 100pF			14		µs
		Overdrive = 100mV, C_{OUT} = 100pF			5		µs
V_{HYST}	Hysteresis Input Voltage Range	LTC1444/LTC1445		REF – 50mV		REF	V
V_{OH}	Output High Voltage	I_{SOURCE} = 10mA; LTC1443/LTC1445	●	2.6			V
V_{OL}	Output Low Voltage	I_{SINK} = 0.8mA	●			0.4	V
V_{REF}	Reference Voltage	No Load, LTC1443C	●	1.170	1.182	1.194	V
		No Load, LTC1445C/LTC1444C	●	1.209	1.221	1.233	V
I_{SOURCE}	Reference Output Source Current	LTC1443	●	60	120		µA
		LTC1444/LTC1445	●	60	120		µA
I_{SINK}	Reference Output Sink Current	LTC1443/LTC1444/LTC1445	●	4	15		µA
Noise	100Hz to 100kHz, REF	LTC1444/LTC1444/LTC1445			100		μV_{RMS}

The ● denotes specifications which apply over the operating temperature range.

PIN FUNCTIONS

OUTB (Pin 1): Comparator B Output. (Open-drain output for LTC1444.)

OUTA (Pin 2): Comparator A Output. (Open-drain output for LTC1444.)

V^+ (Pin 3): Positive Supply.

INA^- (Pin 4): Inverting Input of Comparator A.

INA^+ (Pin 5): Noninverting Input of Comparator A.

INB^- (Pin 6): Inverting Input of Comparator B.

INB^+ (Pin 7): Noninverting Input of Comparator B.

REF (Pin 8): Reference Output. With respect to V^-.

V^- (Pin 9): Negative Supply. Connect to ground for single supply operation.

INC^- (Pin 10): Inverting Input of Comparator C.

INC^+ (Pin 11): Noninverting Input of Comparator C.

IND^- (Pin 12): Inverting Input of Comparator D.

IND^+ (Pin 13): Noninverting Input of Comparator D.

GND (Pin 14): LTC1443 Ground. Connect to V^- for single supply operation.

HYST (Pin 14): LTC1444/LTC1445 Hysteresis Input. Connect to REF if not used. Input voltage range is from V_{REF} to V_{REF} – 50mV.

OUTD (Pin 15): Comparator D Output. (Open-drain output for LTC1444.)

OUTC (Pin 16): Comparator C Output. (Open-drain output for LTC1444.)

APPLICATIONS INFORMATION

The LTC1443/LTC1444/LTC1445 is comprised of a micropower 1.182V/1.221V reference and four micropower comparators. Each comparator continuously sources up to 40mA, and the unique output stage eliminates crowbar glitches during output transitions. This makes them immune to parasitic feedback (which can cause instability) and provides excellent performance, even when circuit board layout is not optimal.

Internal hysteresis in the LTC1444/LTC1445 provides the easiest method for implementing hysteresis. It also produces faster hysteresis action and consumes much less current than circuits using external positive feedback.

Power Supply and Input Signal Ranges

This family of devices operates from a single 2V to 11V power supply. The LTC1443 has a separate ground for the output driver, allowing operation with dual supplies ranging from ±1V to ±5.5V. Connect V^- to GND when operating the LTC1443 from a single supply. The maximum supply voltage in this case is still 11V.

For proper comparator operation, the input signal can swing from the negative supply (V^-) to within one volt of the positive supply ($V^+ - 1V$). The guaranteed common-mode input voltage range extends from V^- to ($V^+ - 1.3V$). The inputs can be taken above and below the supply rails by up to 300mV without damage.

Comparator Output

With 100mV of overdrive, propagation delay is typically 4µs. The LTC1443 output swings from V^+ to GND so TTL compatibility is assured by using a 5V ±10% supply. The negative supply does not affect the output swing and can range from 0V to –5V ±10%.

The LTC1444 and LTC1445 have no GND pin and their outputs swing from V^+ to V^-. Connect V^- to ground and V^+ to a 5V supply to achieve TTL compatibility.

The LTC1443/LTC1445's unique design achieves an output source current of more than 40mA and a sink current of over 5mA, while keeping quiescent currents in the microampere range. The output can source 100mA (at $V^+ = 5V$) for short pulses, as long as the package's maximum power dissipation is not exceeded. The output stage does not generate crowbar switching currents during transitions, which minimizes feedback through the supplies and helps ensure stability without bypassing.

Voltage Reference

The internal bandgap voltage reference has an output of 1.182V above V^- for the LTC1443 and 1.221V for the LTC1444/LTC1445. Note that the REF voltage is referenced to V^-, not to GND. Its accuracy is ±1% in the commercial range. The REF output is typically capable of sourcing 30µA and sinking 10µA. The REF output can drive up to 0.01µF of output capacitance without oscillation.

Noise Considerations

Although the comparators have a very high gain, useful gain is limited by noise. As the input voltage approaches the comparator's offset, the output begins to bounce back and forth; this peaks when $V_{IN} = V_{OS}$. Consequently, the comparator has an effective wideband peak-to-peak noise of around 0.3mV. The voltage reference has peak-to-peak noise approaching 1mV. Thus, when a comparator is used with the reference, the combined peak-to-peak noise is above 1mV. This, of course, is much higher than the RMS noise of the individual components. Care should be taken in the layout to avoid capacitive coupling from any output to the reference pin. Crosstalk can significantly increase the actual noise of the reference.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1034	Micropower Dual Reference	1.2V or 2.5V with 7V Auxiliary Reference
LT1179	Quad Micropower Single Supply Precision Op Amp	17µA Max per Amplifier
LTC1285/LTC1288	3V Micropower Sampling 12-Bit ADCs	SO-8 Package, Auto Shutdown to 1nA
LT1521	300mA Low Dropout Regulator	12µA Quiescent Current

LTC1477/LTC1478

Single and Dual Protected High-Side Switches

May 1995

FEATURES

- **Extremely Low $R_{DS(ON)}$ Switch: 0.07Ω**
- **No Parasitic Body Diode**
- **Built-In Short Circuit Protection: 2A**
- Built-In Thermal Overload Protection
- Operates from 2.7V to 5.5V
- Inrush Current Limited
- Ultra-Low Standby Current: 0.01μA
- Built-In Charge Pump
- Controlled Rise and Fall Times: t_R = 1ms
- Single Switch in 8-Pin SO Package
- Dual Switch in 16-Pin SO Package

APPLICATIONS

- Notebook Computer Power Management
- Power Supply/Load Protection
- Supply/Battery Switch-Over Circuits
- Circuit Breaker Function
- "Hot Swap" Board Protection
- Peripheral Power Protection

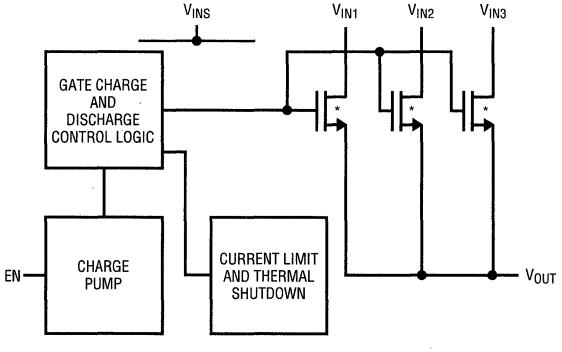
DESCRIPTION

The LTC®1477/LTC1478 protected high-side switches provide extremely low $R_{DS(ON)}$ switching with built-in protection against short-circuit and thermal overload conditions. A built-in charge pump generates gate drive higher than the supply voltage to fully enhance the internal NMOS switch. This switch has no parasitic body diode and therefore no current flows through the switch when it is turned off and the output is forced above the input supply voltage. (DMOS switches have parasitic body diodes that become forward biased under these conditions.)

Two levels of protection are provided by the LTC1477/LTC1478. The first level of protection is short-circuit current limit which is set at 2A. The short-circuit current can be reduced to as low as 0.85A by disconnecting portions of the power device (see Applications Information). The second level of protection is provided by thermal overload protection which limits the die temperature to approximately 130°C.

The LTC1477 single is available in 8-lead SO packaging. The LTC1478 dual is available in 16-lead SO packaging.

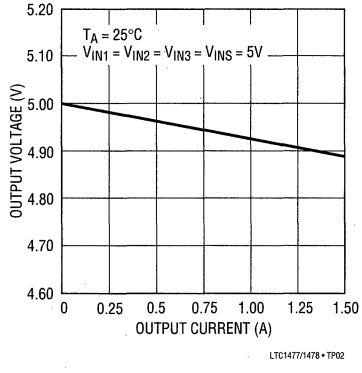
SIMPLIFIED BLOCK DIAGRAM



*NMOS SWITCHES WITH NO PARASITIC BODY DIODES

LTC1477/1478 • TA01

Switch Output Voltage



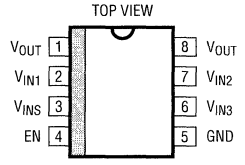
LTC1477/1478 • TP02

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 7V
Enable Input Voltage ..... (7V) to (GND –0.3V)
Output Voltage (OFF) (Note 1) ..... (7V) to (GND –0.3V)
Output Short-Circuit Duration ..... Indefinite
Junction Temperature ..... 110°C

Operating Temperature
LTC1477C/LTC1478C ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

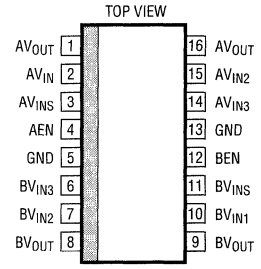
PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 110°C, θ_{JA} = 120°C/W

ORDER PART NUMBER
LTC1477CS8
S8 PART MARKING
1477



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 110°C, θ_{JA} = 100°C/W

ORDER PART NUMBER
LTC1478CS

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{INS} = V_{IN1} = V_{IN2} = V_{IN3} = 5V (Note 2), T_A = 25°C, unless otherwise noted. Each channel of the LTC1478 is tested separately (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Supply Voltage Range			2.7		5.5	V
I_{VIN}	Supply Current	Switch OFF, Enable = 0V	●		0.01	10	µA
		Switch ON, Enable = 5V, V_{IN} = 5V	●		120	180	µA
		Switch ON, Enable = 3.3V, V_{IN} = 3.3V	●		80	120	µA
R_{ON}	ON Resistance	V_{INS} = V_{IN1} = V_{IN2} = V_{IN3} = 5V, I_{OUT} = 1A			0.07	0.12	Ω
		V_{INS} = V_{IN1} = V_{IN2} = V_{IN3} = 3.3V, I_{OUT} = 1A			0.08	0.12	Ω
		V_{INS} = V_{IN1} = 5V, V_{IN2} = V_{IN3} = NC, I_{OUT} = 0.5A			0.12	0.20	Ω
		V_{INS} = V_{IN1} = 3.3V, V_{IN2} = V_{IN3} = NC, I_{OUT} = 0.5A			0.13	0.20	Ω
I_{LKG}	Output Leakage Current OFF	Switch OFF, Enable = 0V	●			±20	µA
I_{SC}	Short-Circuit Current Limit	V_{INS} = V_{IN1} = V_{IN2} = V_{IN3} = 5V, V_{OUT} = 0V, (Note 4)		1.60	2.00	2.40	A
		V_{INS} = V_{IN1} = 5V, V_{IN2} = V_{IN3} = NC, V_{OUT} = 0V, (Note 4)		0.68	0.85	1.02	A
V_{ENH}	Enable Input High Voltage	3.0V ≤ V_{INS} ≤ 5.5V	●	2.0			V
V_{ENL}	Enable Input Low Voltage	3.0V ≤ V_{INS} ≤ 5.5V	●			0.8	V
I_{EN}	Enable Input Current	0V ≤ V_{EN} ≤ 5.5V	●			±1	µA
t_{D+R}	Delay and Rise Time	R_{OUT} = 100Ω, C_{OUT} = 1µF, to 90% of Final Value		0.50	1.00	2.00	ms

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The V_{OUT} pins must be connected together.

Note 2: The V_{INS} and V_{IN1} pins must be connected together. The V_{IN2} and V_{IN3} pins are typically connected to V_{INS} and V_{IN1} pins but can be selectively disconnected to reduce the short-circuit current limit and increase the ON resistance of the switch. The LTC1478 GND pins must be connected together. (See Pin Functions and Block Diagram for more detail.)

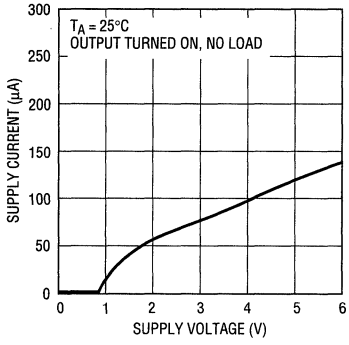
Note 3: Other channel turned OFF, i.e. AEN and BEN = 0V.

Note 4: The output is protected with fold-back current limit which reduces the short-circuit (0V) currents below peak permissible current levels at higher output voltages. (See Typical Performance Characteristics for further detail on output current versus output voltage).

13

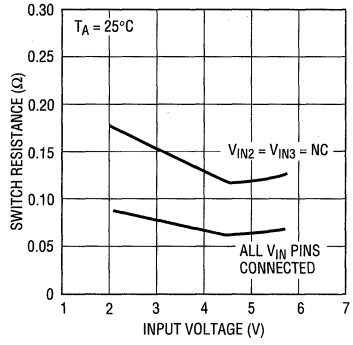
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current (ON)



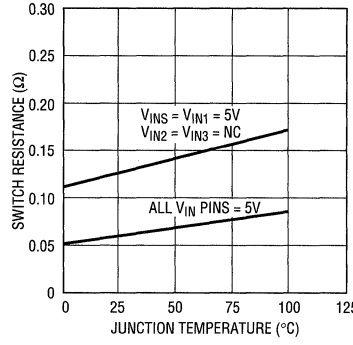
LTC1477/1478 • TPC01

Switch Resistance



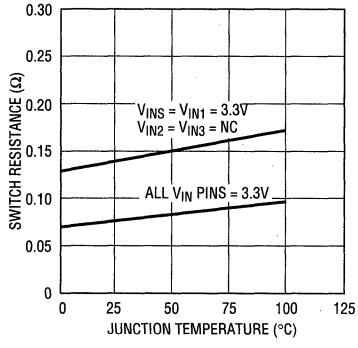
LTC1477/1478 • TPC02

Switch Resistance (5V)



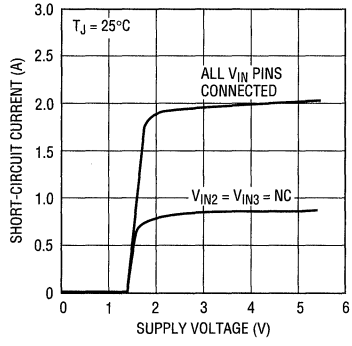
LTC1477/1478 • TPC03

Switch Resistance (3.3V)



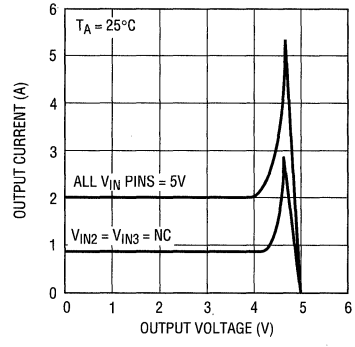
LTC1477/1478 • TPC04

Short-Circuit Current



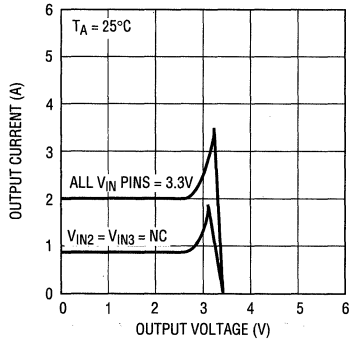
LTC1477/1478 • TPC05

Output Current (5V)



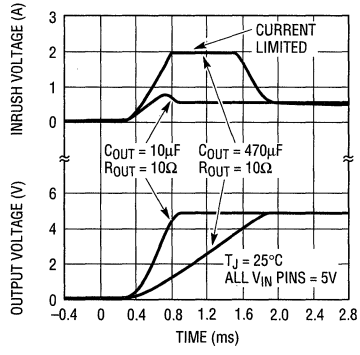
LTC1477/1478 • TPC06

Output Current (3.3V)



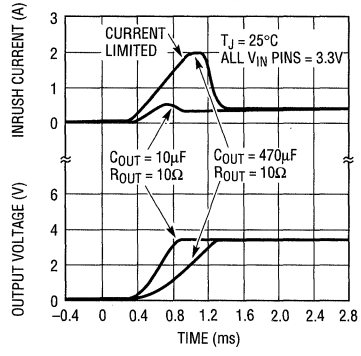
LTC1477/1478 • TPC07

Inrush Current (5V)



LTC1477/1478 • TPC08

Inrush Current (3.3V)



LTC1477/1478 • TPC09

PIN FUNCTIONS

LTC1477

EN (Pin 4): The enable input is a high impendance CMOS gate with an ESD protection diode to ground and should not be forced below ground. This input has about 100mV of built-in hysteresis to ensure clean switching.

V_{INS}, V_{IN1} (Pins 3,2): The V_{INS} supply pin must always be connected to the V_{IN1} supply pin (see Block Diagram). The V_{INS} supply pin provides power for the input control logic, the current limit and thermal shutdown circuitry; plus provides a sense connection to the input power supply. The gate of the NMOS switch is powered by a charge pump from the V_{INS} supply pin (see Block Diagram). The V_{IN1} supply pin provides connection to the drain of 1/2 of the output power device.

V_{IN2}, V_{IN3} (Pins 7,6): The V_{IN2} and V_{IN3} supply pins are typically tied to the V_{INS} and V_{IN1} supply pins for lowest on resistance; i.e., when all four V_{IN} pins are connected together the entire power device is connected (see Block Diagram). Each auxiliary supply pin, V_{IN2} and V_{IN3}, is connected to the drain of 1/4 of the power device. The V_{IN2} and V_{IN3} pins can be selectively disconnected to reduce the short-circuit current limit at the expense of higher $R_{DS(ON)}$. (See Applications Information section for more detail.)

V_{OUT} (Pins 1,8): The output pins of the LTC1477 must always be tied together. The output is protected against accidental short-circuits to ground by a current-limit circuit which protects the system power supply and load against damage. A second level of protection is provided by thermal shutdown circuitry which limits the die temperature to 130°C.

LTC1478

AEN, BEN (Pins 4,12): The enable inputs are high impedance CMOS gates with ESD protection diodes to ground and should not be forced below ground. These inputs have about 100mV of built-in hysteresis to ensure clean switching.

AV_{INS}, AV_{IN1}, BV_{INS}, BV_{IN1} (Pins 3,2; 11,10): The AV_{INS} or BV_{INS} supply pin must always be connected to the AV_{IN1} or BV_{IN1} supply pin (see Block Diagram). The AV_{INS} and BV_{INS} supply pins provide power for the input control logic, the current limit and thermal shutdown circuitry; plus provides a sense connection to the input power supply. The gate of the NMOS switch is powered by a charge pump from the AV_{INS} and BV_{INS} supply pins (see Block Diagram). The AV_{IN1} and BV_{IN1} supply pins provide connection to the drain of 1/2 of the output power device.

AV_{IN2}, AV_{IN3}, BV_{IN2}, BV_{IN3}, (Pins 15,14; 7,6): The AV_{IN2}, AV_{IN3}, BV_{IN2} and BV_{IN3} supply pins are typically tied to the AV_{INS}, AV_{IN1}, BV_{INS} and BV_{IN1} supply pins for lowest on resistance; i.e., when all four AV_{IN}, BV_{IN} pins are connected together the entire power device is connected (see Block Diagram). Each auxiliary supply pin, AV_{IN2}, AV_{IN3}, BV_{IN2} and BV_{IN3}, is connected to the drain of approximately 1/4 of the corresponding power device. The AV_{IN2}, AV_{IN3}, BV_{IN2} and BV_{IN3} pins can be selectively disconnected to reduce the short-circuit limit at the expense of higher $R_{DS(ON)}$. (See Applications Information section for more detail.)

AV_{OUT}, BV_{OUT} (Pins 1,16; 8,9): The outputs of the LTC1478 are protected against accidental short-circuits to ground by a current-limit circuit which protects the system power supplies and loads against damage. A second level of protection is provided by thermal shutdown circuitry which limits the die temperature to approximately 130°C.

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OPERATION (LTC1477 or single channel of LTC1478)

Input TTL-CMOS Converter

The LTC1477 enable input is designed to accommodate a wide range of 3V and 5V logic families. The input threshold voltage is approximately 1.4V with 100mV of hysteresis. The input enables the bias generator, the gate charge pump and the protection circuitry. Therefore, when the enable input is turned off, the entire circuit is powered down and the supply current drops below 1μA.

Ramped Switch Control

The LTC1477 gate charge pump includes circuitry which ramps the NMOS switch on slowly (1ms typical rise time) but turns it off much more quickly (typically 20μs).

Bias, Oscillator and Gate Charge Pump

When the switch is enabled, a bias current generator and high frequency oscillator are turned on. The on-chip capacitive charge pump generates approximately 12V of gate drive for the internal low $R_{DS(ON)}$ NMOS switch from the power supply. No external 12V supply is required to switch the output.

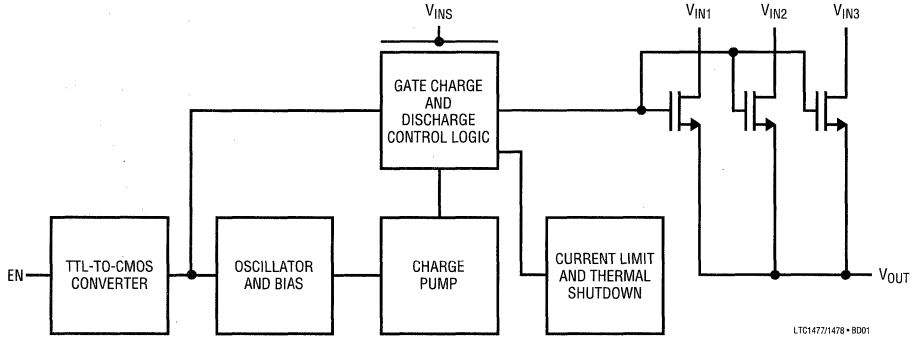
Switch Protection

Two levels of protection are designed into the power switch in the LTC1477. The switch is protected against accidental short-circuits with a current limit circuit which limits the output current to typically 2A when the output is shorted to ground. The LTC1477 also has thermal shutdown set at approximately 130°C which limits the power dissipation to safe levels.

LTC1478 Operation

The LTC1478 dual protected switch can be thought of as two independent LTC1477 single protected switches. The input supply voltages may be from separate power sources. The ground connection, however, is common to both channels and must be connected to the same potential.

BLOCK DIAGRAM (LTC1477 or single channel of LTC1478)



APPLICATIONS INFORMATION

Tailoring I_{LIMIT} and $R_{DS(ON)}$ for Load Requirements

The LTC1477 is designed to current limit at approximately 2A during a short-circuit with all the V_{IN} pins connected to the input power supply. It is possible however, to reduce this current by selectively disconnecting two of the four power supply pins (V_{IN2} and V_{IN3}). Table 1 lists the effects of disconnecting these pins on $R_{DS(ON)}$ and short-circuit current limit

Table 1. Effects of Disconnecting V_{IN2} and V_{IN3}

	ALL V_{IN} PINS CONNECTED	V_{IN3} DISCONNECTED	V_{IN2} AND V_{IN3} DISCONNECTED
$R_{DS(ON)}$	0.07Ω	0.09Ω	0.12Ω
I_{LIMIT}	2A	1.5A	0.85A

Note: 5V Operation

Note that there is an inverse relationship between output current limit and switch resistance. This allows the tailoring of the switch parameter to the expected load current and system current limit requirements.

A couple of examples are helpful:

1. If a nominal load of 1A was controlled by the switch configured to current limit at 2A (all V_{IN} pins connected together), the $R_{DS(ON)}$ would be 0.07Ω and the voltage drop across the switch would be 70mV. The power dissipated by the switch would only be 70mW.
2. If a nominal load of 0.5A was controlled by the switch configured to current limit at 0.85A (V_{IN2} and V_{IN3} disconnected), the $R_{DS(ON)}$ would increase to 0.14Ω. But the voltage drop would remain at 70mV and the switch power dissipation would drop to 35mW.

Supply Bypassing

For best results, bypass the supply input pins with a single 1.0µF capacitor as close as possible to the LTC1477. Sometimes, much larger capacitors are already available at the output of the power supply. In this case, it is still good practice to use a 0.1µF capacitor as close as possible to the LTC1477, especially if the power supply output capacitor is more than 2" away on the printed circuit board.

Output Capacitor

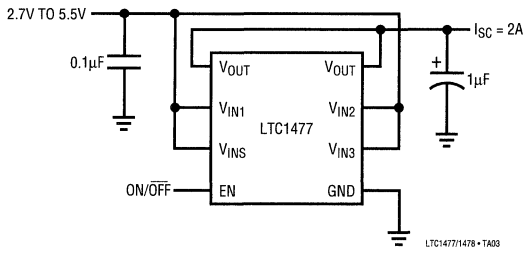
The output pin is designed to ramp on slowly, typically 1ms rise time. Therefore, very large output capacitors can be driven without producing voltage spikes on the supply pins (see graphs in Typical Performance Characteristics). The output pin should have a 1µF capacitor for noise reduction and smoothing.

Supply and Input Sequencing

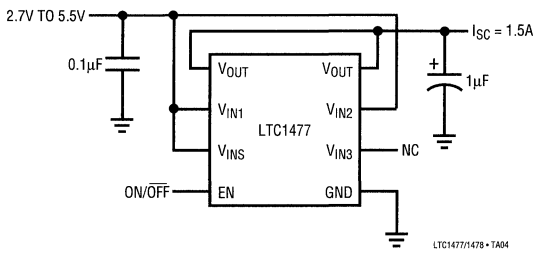
The LTC1477 is designed to operate with continuous power (quiescent current drops to < 1µA when disabled). If the power must be turned off, for example to enter a system "sleep" mode, the enable input must be turned off 100µs before the input supply is turned off to ensure that the gate of the NMOS switch is completely discharged before power is removed. However, the input control and power can be applied simultaneously during power up.

TYPICAL APPLICATIONS

2A Protected Switch



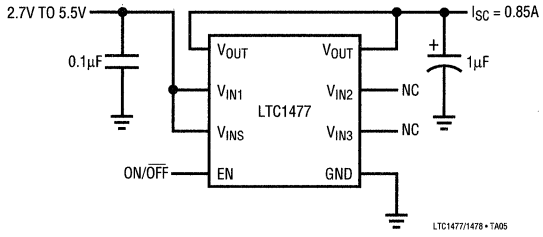
1.5A Protected Switch



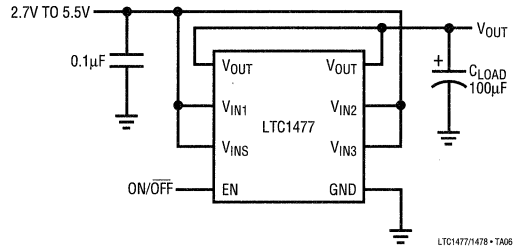
13

TYPICAL APPLICATIONS

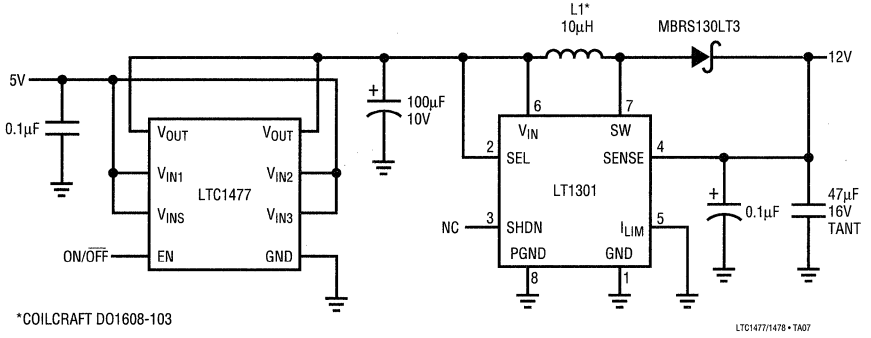
0.85A Protected Switch



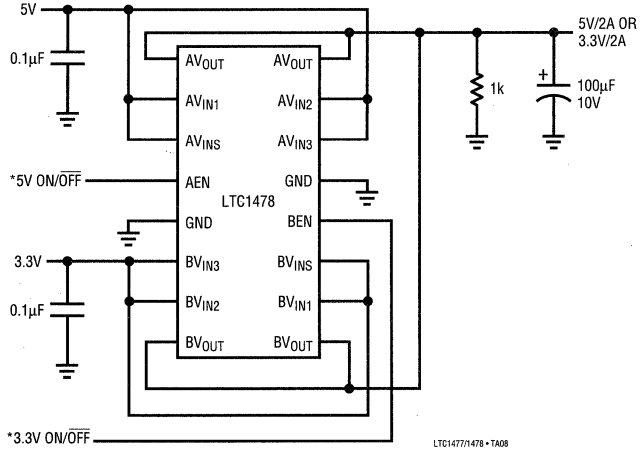
2A Protected Switch Driving a Large Capacitive Load



Adding Short-Circuit Protection to an LT1301 Step-Up Switching Regulator (0.01µA Standby Current)



5V to 3.3V Selector Switch with Slope Control and 0.01µA Standby Current



*ALLOW AT LEAST 100ms BETWEEN 5V AND 3.3V SWITCHING FOR DISCHARGE OF 100µF OUTPUT CAPACITOR

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1153	Electronic Circuit Breaker	MOSFET Driver with Adjustable Reset Time
LTC1154	Single High-Side Driver	MOSFET Driver with Switch Status Output
LTC1155	Dual High-Side Driver	Dual MOSFET Driver with Protection
LTC1470	5V and 3.3V V_{CC} Switch	SafeSlot™ Protected Switch in 8-Lead SO
LTC1471	Dual 5V and 3.3V V_{CC} Switch	Dual Version of LTC1470 in 16-Lead SO
LTC1472	PCMCIA V_{CC} and VPP Switches	Complete Single Channel SafeSlot Protection

SafeSlot is a trademark of Linear Technology Corporation.

Constant-Voltage/ Constant-Current Battery Charger

June 1995

FEATURES

- **Charges NiCd, NiMH and Lithium-Ion Batteries — One Resistor Is Needed to Program Charging Current**
- **High Efficiency Current Mode PWM with 2A Internal Switch and Sense Resistor**
- **Precision 5% Accuracy at Full Charging Current**
- **Precision 0.5% Voltage Reference for Voltage Mode Charging or Overvoltage Protection**
- Current Sensing Can Be at Either Terminal of the Battery
- Low Reverse Battery Drain Current: 3μA
- Charging Current Soft Start
- Shutdown Control

APPLICATIONS

- Chargers for NiCd, NiMH and Lithium Batteries
- Step-Down Switching Regulator with Precision Adjustable Current Limit

DESCRIPTION

The LT®1510 current mode PWM battery charger is the simplest, most efficient solution to fast-charge modern rechargeable batteries including lithium-ion (Li-Ion), nickel-metal-hydride (NiMH)* and nickel-cadmium (NiCd)* that require constant-current and/or constant-voltage charging. The internal switch is capable of delivering 1.5A DC current (2A peak current). The 0.1Ω onboard current sense resistor makes the charging current programming very simple. One resistor (or a programming current from a DAC) is required to set the full charging current (1.5A) to within 5% or the trickle charge current (150mA) to 10% accuracy. The LT1510 with 0.5% reference voltage accuracy meets the critical constant-voltage charging requirement for lithium cells.

The LT1510 can charge batteries ranging from 2V to 20V. Ground sensing of current is not required and the battery's negative terminal can be tied directly to ground. A saturating switch running at 200kHz gives high charging efficiency and small inductor size. A blocking diode is not required between the chip and the battery because the chip goes into sleep mode and drains only 3μA when the wall adaptor is unplugged. Soft start and shutdown features are also provided. The LT1510 is available in a 16-pin fused lead power SO package with a thermal resistance of 50°C/W, an 8-pin SO and a 16-pin PDIP.

* NiCd and NiMH batteries require charge termination circuitry (not shown in Figure 1).

TYPICAL APPLICATIONS

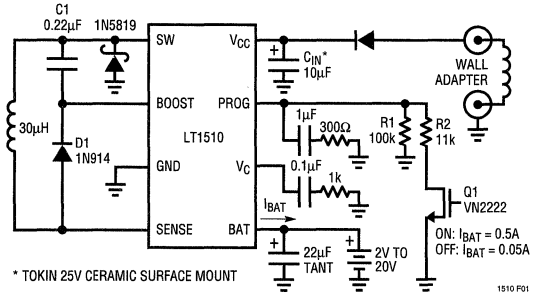


Figure 1. Charging NiMH or NiCd Batteries (Efficiency at 0.5A ≈ 90%)

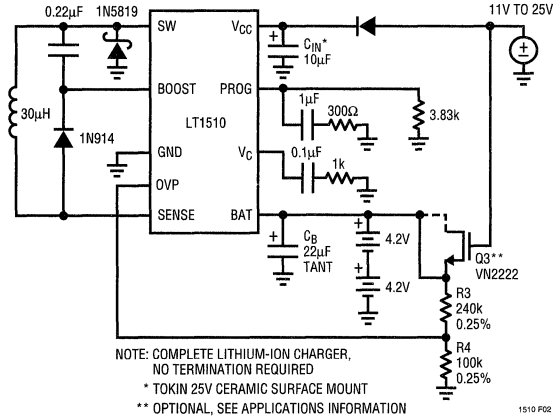
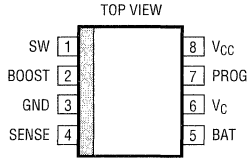


Figure 2. Charging Lithium Batteries (Efficiency at 1.3A > 87%)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{MAX}) 27V
Switch Voltage with Respect to GND ..... –3V
Boost Pin Voltage with Respect to V_{CC} 30V
Boost Pin Voltage with Respect to GND ..... –5V
V_C, PROG, OVP Pin Voltage 8V
I_{BAT} (Average) 1.5A
Switch Current (Peak) 2A
Operating Junction
Temperature Range ..... 0°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S8 PACKAGE
8-LEAD PLASTIC SO

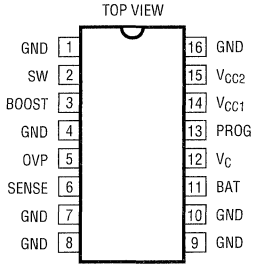
T_{JMAX} = 125°C, θ_{JA} = 125°C/W

ORDER PART NUMBER

LT1510CS8

S8 PART MARKING

1510



N PACKAGE
16-LEAD PDIP

S PACKAGE*
16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 75°C/W (N)
T_{JMAX} = 125°C, θ_{JA} = 50°C/W (S)*

ORDER PART NUMBER

LT1510CN
LT1510CS

* FOUR CORNER PINS ARE FUSED TO INTERNAL DIE ATTACH PADDLE FOR HEAT SINKING. CONNECT THESE FOUR PINS TO EXPANDED PC LANDS FOR PROPER HEAT SINKING.

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 16V, V_{BAT} = 8V, V_{MAX} (maximum operating V_{CC}) = 25V, no load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Overall						
Supply Current	V_{PROG} = 2.7V, $V_{CC} \le$ 20V	●		2.90	3.9	mA
	V_{PROG} = 2.7V, 20V < $V_{CC} \le V_{MAX}$	●		2.91	4.1	mA
DC Battery Current, I_{BAT} (Note 1)	8V ≤ $V_{CC} \le V_{MAX}$, 0V ≤ $V_{BAT} \le$ 20V					
	R_{PROG} = 4.93k	●	0.950	1.0	1.050	A
	R_{PROG} = 3.28k (Note 4)	●	1.425	1.5	1.575	A
	R_{PROG} = 49.3k	●	90	100	110	mA
V_{CC} Undervoltage Lockout (Switch OFF) Threshold		●	6	7	8	V
Reverse Current from Battery (When V_{CC} Is Not Connected, V_{SW} Is Floating)	$V_{BAT} \le$ 20V	●		3	6	µA
	20V < $V_{BAT} \le V_{MAX}$	●		3	8	µA
Boost Pin Current	$V_{CC} - V_{BOOST} \le$ 20V	●		0.10	10	µA
	20V < $V_{CC} - V_{BOOST} \le V_{MAX}$	●		0.25	20	µA
	2V ≤ $V_{BOOST} - V_{CC} \le$ 8V (Switch ON)	●		6	9	mA
	8V < $V_{BOOST} - V_{CC} \le$ 25V (Switch ON)	●		8	12	mA

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ELECTRICAL CHARACTERISTICS

V_{CC} = 16V, V_{BAT} = 8V, V_{MAX} (maximum operating V_{CC}) = 25V, no load on any outputs, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switch						
Switch ON Resistance	$8V \le V_{CC} \le V_{MAX}$ I_{SW} = 1.5A, $V_{BOOST} - V_{SW} \ge 2V$ (Note 4) I_{SW} = 1A, $V_{BOOST} - V_{SW} < 2V$	 ● ●		 0.3	 0.42 1.50	 Ω Ω
$\Delta I_{BOOST}/\Delta I_{SW}$ During Switch ON	V_{BOOST} = 24V			25	35	mA/A
Switch OFF Leakage Current	V_{SW} = 0V, $V_{CC} \le 20V$ $20V < V_{CC} \le V_{MAX}$	● ●		2 4	100 200	µA µA
Maximum V_{BAT} with Switch ON		●			$V_{CC} - 2$	V
Minimum I_{PROG} for Switch ON		●	2	4	7	µA
Minimum I_{PROG} for Switch OFF at $V_{PROG} \le 1V$		●	1	1.2		mA
Current Sense Amplifier Inputs (SENSE, BAT)						
Sense Resistance (R_{S1})				0.08	0.12	Ω
Total Resistance from SENSE to BAT (Note 3)				0.2	0.25	Ω
Input Bias Current		●		–100	–200	µA
Input Common-Mode Low		●	–0.25			V
Input Common-Mode High		●			$V_{CC} - 2$	V
Reference						
Reference Voltage (Note 1) S8 Package	R_{PROG} = 4.93k, Measured at PROG Pin		2.430	2.465	2.495	V
Reference Voltage (Note 2) N16, S16 Packages	R_{PROG} = 3.28k, Measured at OVP with VA Supplying I_{PROG} and Switch OFF		2.453	2.465	2.477	V
Reference Voltage Tolerance	All Conditions of V_{CC}, Temperature	●	2.441		2.489	V
Oscillator						
Switching Frequency			190	200	210	kHz
Switching Frequency Tolerance	All Conditions of V_{CC}, Temperature	●	180	200	220	kHz
Maximum Duty Cycle		●	85	93		%
Current Amplifier (CA2)						
Transconductance	V_C = 1V, I_{VC} = ±1µA		150	250	400	µmho
Maximum V_C for Switch OFF		●			0.7	V
I_{VC} Current (Out of Pin)	$V_C \ge 0.45V$ $V_C < 0.45V$	● ●			42 3	µA mA
Voltage Amplifier (VA)						
Transconductance (Note 2)	Output Currrent from 100µA to 500µA		0.4	0.6	1	mho
Output Source Current	V_{PROG} = 2.5V, V_{OVP} = 2.5V	●	1.1		3	mA
OVP Input Bias Current	At 0.75mA VA Output Current	●		50	150	nA

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Tested with Test Circuit 1.

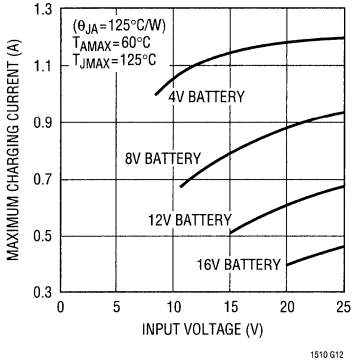
Note 2: Tested with Test Circuit 2.

Note 3: Sense resistor R_{S1} and package bond wires.

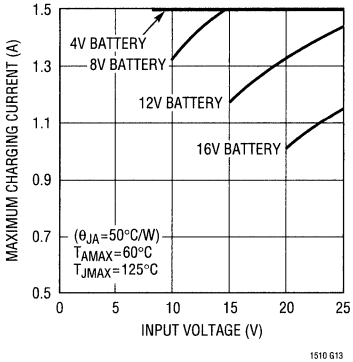
Note 4: Applies to 16-pin only.

TYPICAL PERFORMANCE CHARACTERISTICS

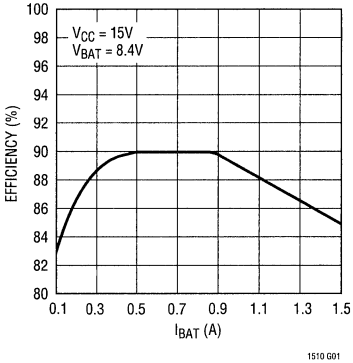
Thermally Limited Maximum Charging Current, 8-Pin SOIC



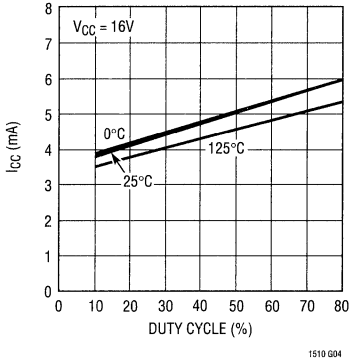
Thermally Limited Maximum Charging Current, 16-Pin SOIC



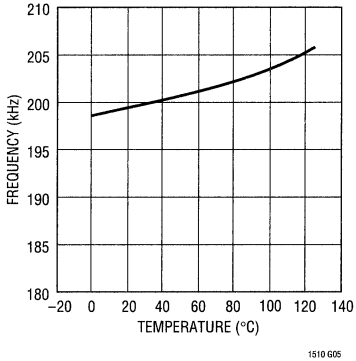
Efficiency of Figure 2 Circuit



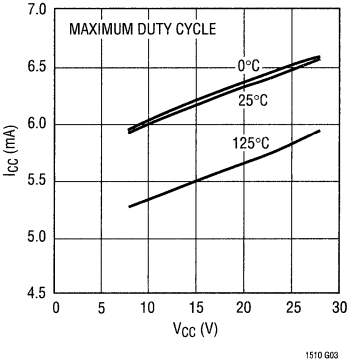
I_{CC} vs Duty Cycle



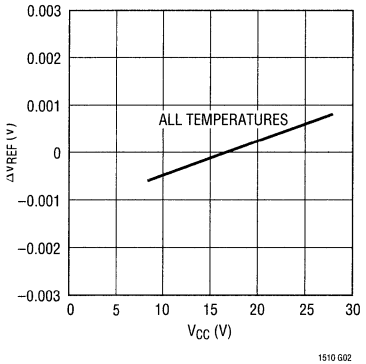
Switching Frequency vs Temperature



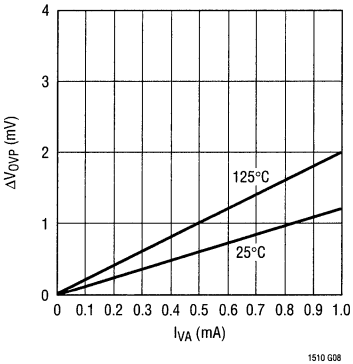
I_{CC} vs V_{CC}



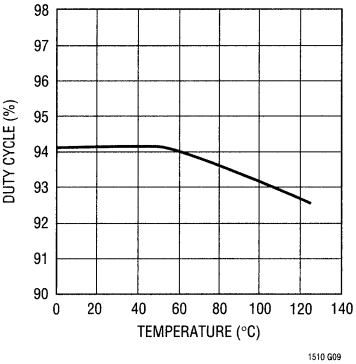
V_{REF} Line Regulation



I_{VA} vs ΔV_{OVP} (Voltage Amplifier)



Maximum Duty Cycle



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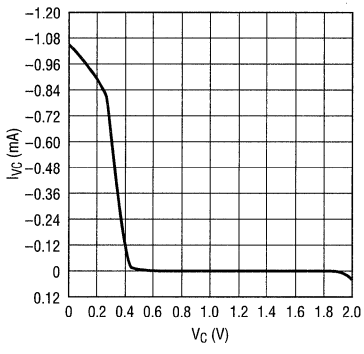
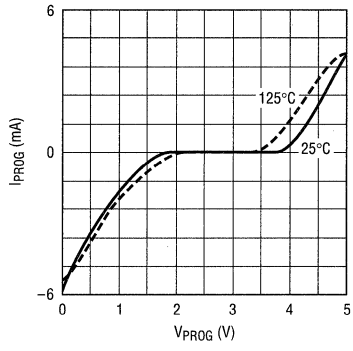
TYPICAL PERFORMANCE CHARACTERISTICS

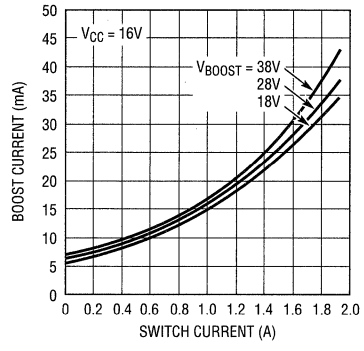
V_C Pin Characteristic



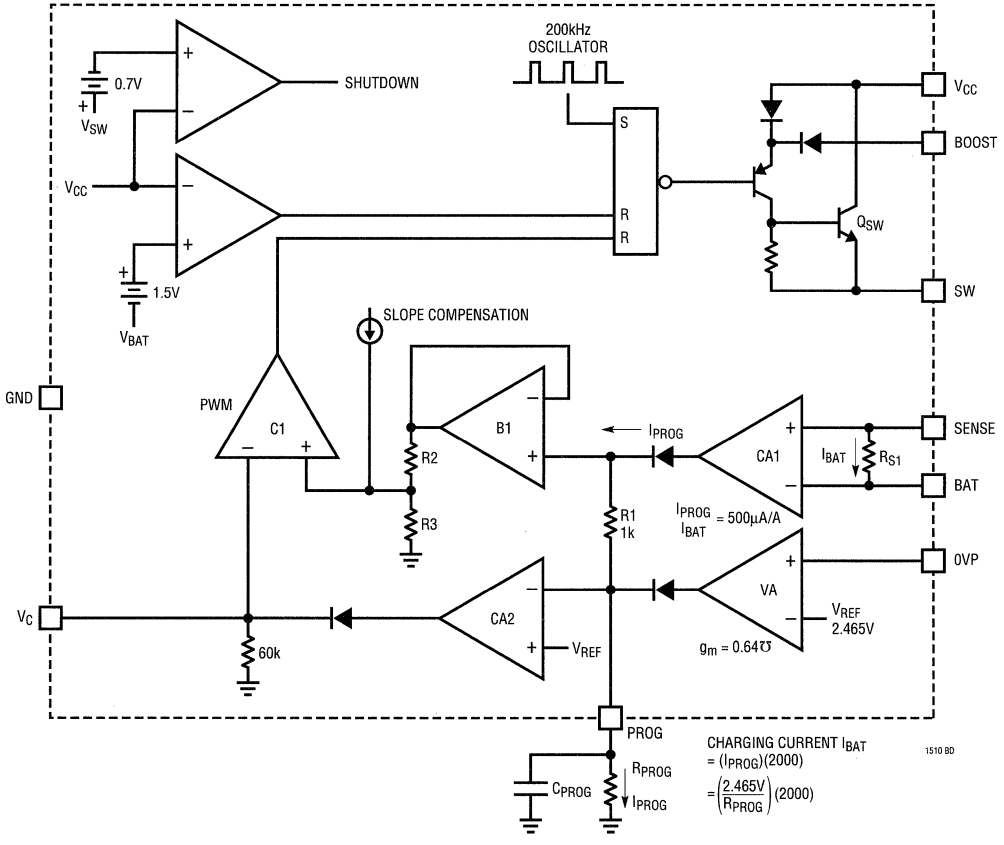
PROG Pin Characteristic



Switch Current vs Boost Current vs Boost Voltage



BLOCK DIAGRAM



OPERATION

The LT1510 is a current mode PWM step-down (buck) switcher. The battery DC charging current is programmed by a resistor R_{PROG} (or a DAC output current) at the PROG pin (see Block Diagram). Amplifier CA1 converts the charging current through R_{S1} to a much lower current I_{PROG} (500μA/A) fed into the PROG pin. Amplifier CA2 compares the output of CA1 with the programmed current and drives the PWM loop to force them to be equal. High DC accuracy is achieved with averaging capacitor C_{PROG}. Note that I_{PROG} has both AC and DC components. I_{PROG} goes through R1 and generates a ramp signal that is fed to the PWM control comparator C1 through buffer B1 and level shift resistors R2 and R3, forming the current mode inner loop. The Boost pin drives the switch NPN Q_{SW} into saturation and reduces power loss. For batteries like lithium-ion that require both constant-current and constant-voltage charging, the 0.5%, 2.465V reference and the amplifier VA reduce the charging current when battery voltage reaches the preset level. For NiMH and NiCd, VA can be used for overvoltage protection. When input voltage is not present, the charger goes into low current (3μA typically) sleep mode as input drops down to 0.7V below battery voltage. To shut down the charger, simply pull the V_C pin low with a transistor.

APPLICATIONS INFORMATION

Input and Output Capacitors

The input capacitor is assumed to absorb all input switching ripple current in the converter, so it must have adequate ripple current rating. Worst-case RMS ripple current will be equal to one half of output charging current. Actual capacitance value is not important. Solid tantalum capacitors such as the AVX TPS and Sprague 593D series have high ripple current rating in a relatively small surface mount package, but *caution must be used when tantalum capacitors are used for input bypass.* High input surge currents can be created when the adapter is hot-plugged to the charger and solid tantalum capacitors have a known failure mechanism when subjected to very high turn on surge currents. Highest possible voltage rating on the capacitor will minimize problems. Consult with the manufacturer before use. Alternatives include new high capacity ceramic (5μF to 10μF) from Tokin, et al., and the old standby, aluminum electrolytic, which will require more microfarads to achieve adequate ripple rating.

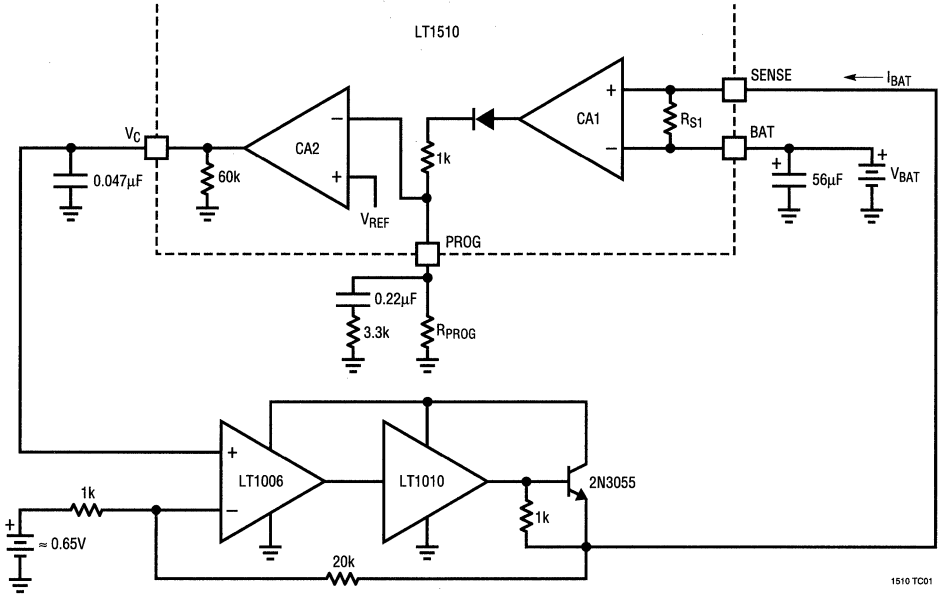
The output capacitor is also assumed to absorb all output switching ripple, which has a worst-case RMS value of approximately $(10e^{-6})$/(inductance L) or 0.33A for a 30μH inductor. EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the 200kHz switching frequency. Output switching ripple will then split between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance.

Thermal Calculations

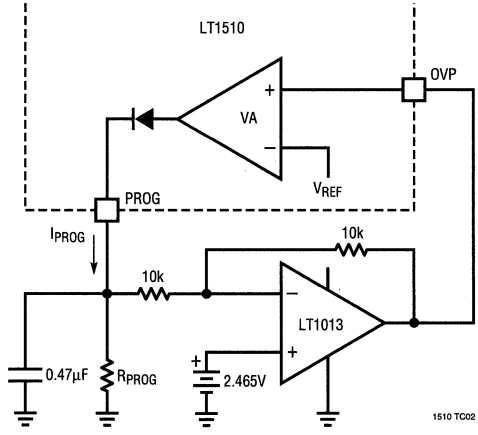
If the LT1510 is used for charging currents above 0.4A, a thermal calculation should be done to ensure that junction temperature will not exceed 125°C. Power dissipation in the IC is caused by bias and driver current, switch resistance, switch transition losses and the current sense resistor. The following equations show that maximum practical charging current for the 8-pin SO package (125°C/W thermal resistance) is about 0.8A for an 8.4V battery and 1.1A for a 4.2V battery. This assumes a 60°C maximum ambient temperature. The 16-pin SO, with a thermal resistance of 50°C/W, can provide a full 1.5A charging current in many situations. The 16-pin PDIP falls between these extremes. Graphs are shown in the Typical Performance Characteristics section.

TEST CIRCUITS

Test Circuit 1



Test Circuit 2



APPLICATIONS INFORMATION

$$P_{BIAS} = (3.5mA)(V_{IN}) + 1.5mA(V_{BAT}) + \frac{(V_{BAT})^2}{V_{IN}}\left[7.5mA + (0.012)(I_{BAT})\right]$$

$$P_{DRIVER} = \frac{(I_{BAT})(V_{BAT})^2}{50(V_{IN})}$$

$$P_{SW} = \frac{(I_{BAT})^2(R_{SW})(V_{BAT})}{V_{IN}} + (t_{OL})(V_{IN})(I_{BAT})(f)$$

$$P_{SENSE} = (0.18\Omega)(I_{BAT})^2$$

R_{SW} = Switch ON resistance ≈ 0.35Ω
t_{OL} = Effective switch overlap time ≈ 10ns
f = 200kHz

Example: V_{IN} = 15V, V_{BAT} = 8.4V, I_{BAT} = 1.2A;

$$P_{BIAS} = (3.5mA)(15) + 1.5mA(8.4) + \frac{(8.4)^2}{15}\left[7.5mA + (0.012)(1.2)\right] = 0.17W$$

$$P_{DRIVER} = \frac{(1.2)(8.4)^2}{50(15)} = 0.11W$$

$$P_{SW} = \frac{(1.2)^2(0.35)(8.4)}{15} + 10e^{-9}(15)(1.2)(200kHz) = 0.28 + 0.04 = 0.32W$$

$$P_{SENSE} = (0.18)(1.2)^2 = 0.26W$$

Total Power in the IC is:
0.17 + 0.11 + 0.32+ 0.26 = 0.86W

Nickel-Cadmium and Nickel-Metal-Hydride Charging

The circuit in Figure 1 on the first page of this data sheet uses the 8-pin LT1510 to charge NiCd or NiMH batteries up to 12V with charging currents of 0.5A when Q1 is on and 50mA when Q1 is off. The basic formula for charging current is:

$$I_{CHRG} = \frac{(2000)(2.465)}{R_{PROG}}$$

I_{CHRG} = Battery charging current
R_{PROG} = Total resistance from PROG pin to ground

For a 2-level charger, R1 and R2 are found from;

$$R1 = \frac{(2.465)(2000)}{I_{LOW}} \qquad R2 = \frac{(2.465)(2000)}{I_{HI} - I_{LOW}}$$

All battery chargers with fast-charge rates require some means to detect full charge state in the battery to terminate the high charging current. NiCd batteries are typically charged at high current until temperature rise or battery voltage decrease is detected as an indication of near full charge. The charging current is then reduced to a much lower value and maintained as a constant trickle charge. An intermediate "top off" current may be used for a fixed time period to reduce 100% charge time.

NiMH batteries are similar in chemistry to NiCd but have two differences related to charging. First, the inflection characteristic in battery voltage as full charge is approached is not nearly as pronounced. This makes it more difficult to use dV/dt as an indicator of full charge, and change of temperature is more often used with a temperature sensor in the battery pack. Secondly, constant trickle charge may not be recommended. Instead, a moderate level of current is used on a pulse basis (≈ 1% to 5% duty cycle) with the time-averaged value substituting for a constant low trickle.

When a microprocessor DAC output is used to control charging current, it must be capable of sinking current at a compliance up to 2.5V if connected directly to the PROG pin.

Lithium-Ion Charging

The circuit in Figure 2 uses the 16-pin LT1510 to charge lithium-ion batteries at a constant 1.3A until battery voltage reaches a limit set by R3 and R4. The charger will then automatically go into a constant-voltage mode with current decreasing to zero over time as the battery reaches full charge. This is the normal regimen for lithium-ion charg-

APPLICATIONS INFORMATION

ing, with the charger holding the battery at "float" voltage indefinitely. In this case no external sensing of full charge is needed.

Current through the R3/R4 divider is set at a compromise value of 25μA to minimize battery drain when the charger is off and to avoid large errors due to the 50nA bias current of the OVP pin. Q3 can be added if it is desired to eliminate even this low current drain. A 47k resistor from adapter output to ground should be added if Q3 is used to ensure that the gate is pulled to ground.

With divider current set at 25μA, R4 = 2.465/25μA = 100k and,

$$R3 = \frac{(R4)(V_{BAT} - 2.465)}{2.465 + R4(0.05\mu A)} = \frac{100k(8.4 - 2.465)}{2.465 + 100k(0.05\mu A)}$$

$$= 240k$$

Lithium-ion batteries typically require float voltage accuracy of 1% to 2%. Accuracy of the LT1510 OVP voltage is ±0.5% at 25°C and ±1% over full temperature. This leads to the possibility that very accurate (0.1%) resistors might be needed for R3 and R4. Actually, the temperature of the LT1510 will rarely exceed 50°C in float mode because charging currents have tapered off to a low level, so 0.25% resistors will normally provide the required level of overall accuracy.

Some battery manufacturers recommend termination of constant-voltage float mode after charging current has dropped below a specified level (typically 50mA to 100mA) *and* a further timeout period of 30 minutes to 90 minutes has elapsed. This may extend the life of the battery, so check with manufacturers for details. The circuit in Figure 3 will detect when charging current has dropped below 75mA. This logic signal is used to initiate a timeout period, after which the LT1510 can be shut down by pulling the V_C pin low with an open collector or drain. Some external means must be used to detect the need for additional charging if needed, or the charger may be turned on periodically to complete a short float-voltage cycle.

Current trip level is determined by the battery voltage, R1 through R3, and the internal LT1510 sense resistor (≈ 0.18Ω pin-to-pin). D2 generates hysteresis in the trip level to avoid multiple comparator transitions.

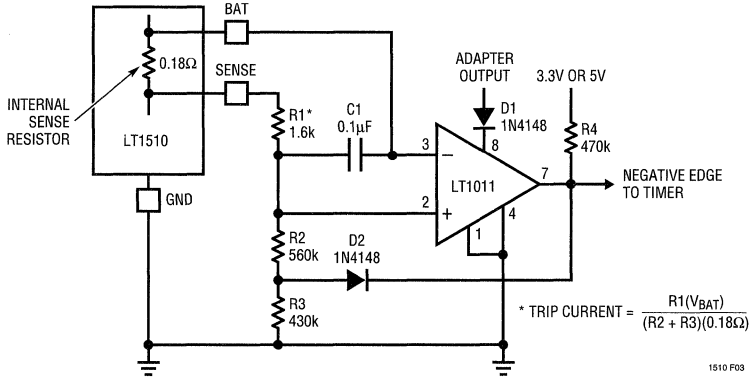
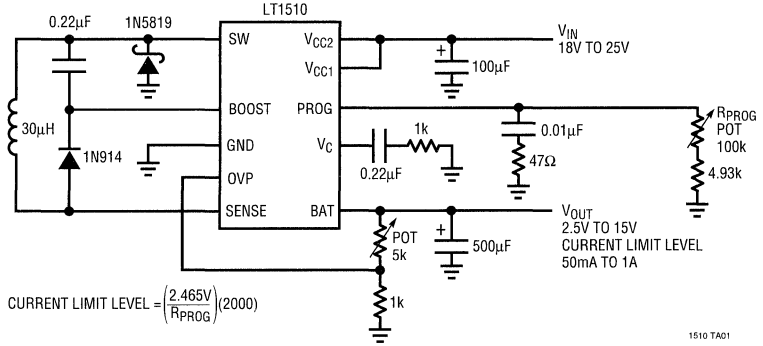


Figure 3. Current Comparator for Initiating Float Timeout

TYPICAL APPLICATION

Adjustable Voltage Regulator with Precision Adjustable Current Limit



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1325	Microprocessor-Controlled Battery Management System	Can Charge, Discharge and Gas Gauge NiCd, NiMH and Pb-Acid Batteries with Software Charging Profiles
LT1372/LT1377	500kHz/1MHz Step-Up Switching Regulators	High Frequency, Small Inductor, High Efficiency Switchers, 1.5A Switch
LT1373	250kHz Step-Up Switching Regulator	High Efficiency, Low Quiescent Current, 1.5A Switch
LT1376	500kHz Step-Down Switching Regulator	High Frequency, Small Inductor, High Efficiency Switcher, 1.5A Switch
LT1512	SEPIC Battery Charger	V_{IN} Can Be Higher or Lower Than Battery Voltage

SEPIC Constant-Current/ Constant-Voltage Battery Charger

May 1995

FEATURES

- **Charger Input Voltage May Be Higher or Lower Than Battery Voltage**
- Charges Any Number of Cells Up to 20V
- 1% Voltage Feedback Accuracy for Lithium Batteries
- 100mV Current Sense Voltage for High Efficiency
- **Battery Can Be Grounded Directly**
- **500kHz Switching Frequency Minimizes Inductor Size**
- Charging Current Easily Programmable or Shut Down

APPLICATIONS

- Battery Charging of NiCd, NiMH or Lithium Cells
- Precision Current Limited Power Supply
- Constant-Voltage, Constant-Current Supply
- Transducer Excitation

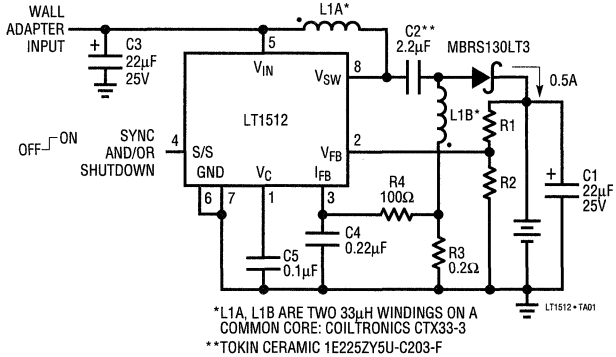
DESCRIPTION

The LT®1512 is a 500kHz current mode switching regulator specially configured to create a constant-current, constant-voltage battery charger. In addition to the usual voltage feedback node, it has a current sense feedback circuit for accurately controlling output current of a flyback or SEPIC topology charger. These topologies allow the current sense circuit to be ground referred and completely separated from the battery itself, simplifying battery switching and eliminating ground loop errors. In addition, these topologies allow charging even when the input voltage is lower than the battery voltage.

Maximum switch current on the LT1512 is 1.5A. This allows battery charging currents up to 0.75A. Overall size of the charger circuit is typically less than 0.7 in^2, and all components can be low profile surface mount. Accuracy of 1% in constant-voltage mode is perfect for lithium battery applications. Charging current can be easily programmed for NiCd or NiMH batteries. A 3A version of the LT1512 will be available in the near future.

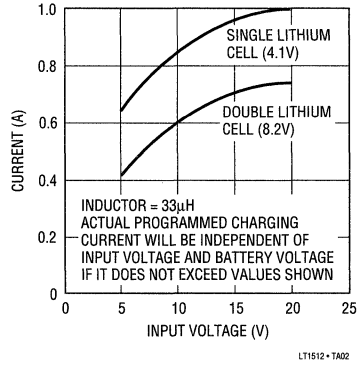
TYPICAL APPLICATION

SEPIC Charger with 0.5A Output Current



*L1A, L1B ARE TWO 33µH WINDINGS ON A COMMON CORE: COILTRONICS CTX33-3
**TOKIN CERAMIC 1E225ZY5U-C203-F

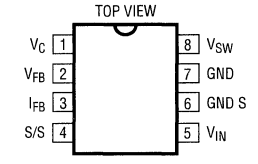
Maximum Charging Current



ABSOLUTE MAXIMUM RATINGS

Supply Voltage 30V
Switch Voltage 35V
S/S Pin Voltage 30V
V_{FB} Pin Voltage (Transient, 10ms) ..... ±10V
V_{FB} Pin Current 10mA
I_{FB} Pin Voltage (Transient, 10ms) ..... ±10V
Operating Junction Temperature Range
Operating ..... 0°C to 125°C
Short Circuit ..... 0°C to 150°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 120°C/W (S8)

ORDER PART NUMBER
LT1512CN8 LT1512CS8
S8 PART MARKING
1512

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, I_{FB} =0V, V_{SW} and S/S pins open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	V_{FB} Reference Voltage	Measured at V_{FB} Pin		1.233	1.245	1.257	V
		V_C = 0.8V	●	1.228	1.245	1.262	V
	V_{FB} Input Current	V_{FB} = V_{REF}			250	550	nA
			●			600	nA
	V_{FB} Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.03	%/V
I_{REF}	I_{FB} Reference Voltage	Measured at I_{FB} Pin			−100		mV
		V_{FB} =0V, V_C = 0.8V	●		−100		mV
	I_{FB} Input Current	V_{IFB} = V_{IREF}	●		−20		µA
	I_{FB} Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.05	%/V
g_m	Error Amplifier Transconductance	ΔI_C = ±25µA		1100	1500	1900	µmho
			●	700		2300	µmho
	Error Amplifier Source Current	V_{FB} = V_{REF} − 150mV, V_C = 1.5V	●	120	200	350	µA
	Error Amplifier Sink Current	V_{FB} = V_{REF} + 150mV, V_C = 1.5V	●		1400	2400	µA
	Error Amplifier Clamp Voltage	High Clamp, V_{FB} = 1V		1.70	1.95	2.30	V
		Low Clamp, V_{FB} = 1.5V		0.25	0.40	0.52	V
A_V	Error Amplifier Voltage Gain				500		V/V
	V_C Pin Threshold	Duty Cycle = 0%		0.8	1	1.25	V
f	Switching Frequency	2.7V ≤ V_{IN} ≤ 25V		460	500	540	kHz
			●	440	500	560	kHz
	Maximum Switch Duty Cycle		●	90	95		%
	Switch Current Limit Blanking Time				130	260	ns
BV	Output Switch Breakdown Voltage	2.7V ≤ V_{IN} ≤ 25V	●	35	47		V
V_{SAT}	Output Switch "On" Resistance	I_{SW} = 1A	●		0.5	0.8	Ω
I_{LIM}	Switch Current Limit	Duty Cycle = 50%	●	1.5	1.9	2.4	A
		Duty Cycle = 80% (Note 1)	●	1.3	1.7	2.2	A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On Time				15	25	mA/A

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ELECTRICAL CHARACTERISTICS

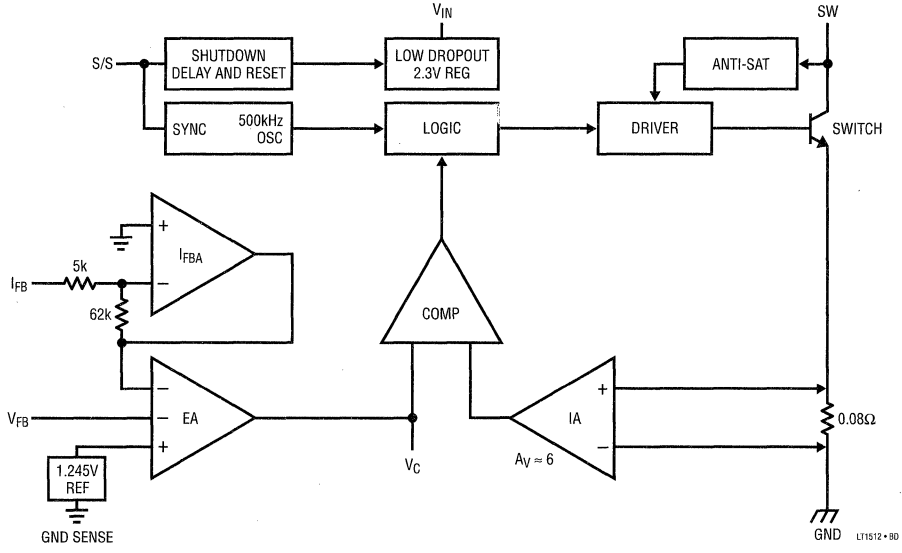
V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, I_{FB} =0V, V_{SW} and S/S pins open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Control Voltage to Switch Current Transconductance				2		A/V
	Minimum Input Voltage		●		2.4	2.7	V
I_Q	Supply Current	2.7V ≤ V_{IN} ≤ 25V	●		4	5.5	mA
	Shutdown Supply Current	2.7V ≤ V_{IN} ≤ 25V, $V_{S/S}$ ≤ 0.6V	●		12	30	µA
	Shutdown Threshold	2.7V ≤ V_{IN} ≤ 25V	●	0.6	1.3	2	V
	Shutdown Delay		●	5	12	25	µs
	S/S Pin Input Current	0V ≤ $V_{S/S}$ ≤ 5V	●	–10		12	µA
	Synchronization Frequency Range		●	600		800	kHz

The ● denotes specifications which apply over the full operating temperature range.

Note 1: For duty cycles (DC) between 50% and 90%, minimum guaranteed switch current is given by I_{LIM} = 0.667 (2.75 – DC).

BLOCK DIAGRAM



OPERATION

The LT1512 is a current mode switcher. This means that switch duty cycle is directly controlled by switch current rather than by output voltage or current. Referring to the Block Diagram, the switch is turned "on" at the start of each oscillator cycle. It is turned "off" when switch current reaches a predetermined level. Control of output voltage and current is obtained by using the output of a dual feedback voltage sensing error amplifier to set switch current trip level. This technique has the advantage of simplified loop frequency compensation. A low dropout internal regulator provides a 2.3V supply for all internal circuitry on the LT1512. This low dropout design allows input voltage to vary from 2.7V to 25V. A 500kHz oscillator is the basic clock for all internal timing. It turns "on" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A unique error amplifier design has two inverting inputs which allow for sensing both output voltage and current. A 1.245V bandgap reference biases the noninverting input. The first inverting input of the error amplifier is brought out for positive output voltage sensing. The second inverting input is driven by a "current" amplifier which is sensing output current via an external current sense resistor. The current amplifier is set to a fixed gain of ≈ -12 which provides a -100mV current limit sense voltage.

The error signal developed at the amplifier output is brought out externally and is used for frequency compensation. During normal regulator operation this pin sits at a voltage between 1V (low output current) and 1.9V (high output current). Switch duty cycle goes to zero if the V_C pin is pulled below the V_C pin threshold, placing the LT1512 in an idle mode.

APPLICATIONS INFORMATION

The LT1512 is an IC battery charger chip specifically optimized to use the SEPIC converter topology. A complete charger schematic is shown in the Typical Application. The SEPIC (Single-Ended Primary Inductance Converter) topology has unique advantages for battery charging. It will operate with input voltages above or below the battery voltage, has no path for battery discharge when turned off, and eliminates the snubber losses of flyback designs. It also has a current sense point that is ground referred and need not be connected directly to the battery. The two inductors shown are actually just two identical windings on one inductor core, although two separate inductors can be used.

A current sense voltage of -100mV is generated with respect to ground across R3. This sets maximum charging current to 0.5A when the battery is below float voltage (I_{MAX} = 100mV/R3). The average current through R3 is always identical to the current delivered to the battery. R4 and C4 filter the current signal to deliver a smooth feedback to the I_{FB} pin. R1 and R2 form a divider for battery voltage sensing and set the battery float voltage. The suggested value for R2 is 12.4k. R1 is calculated from:

$$R1 = \frac{V_{OUT} - 1.245}{\frac{1.245}{R2} + (3 \times 10^{-7})}$$

V_{OUT} = battery float voltage

Maximum input voltage for this circuit is partly determined by battery voltage. A SEPIC converter has an off-state switch voltage equal to input voltage plus output voltage. The LT1512 has a maximum input voltage of 30V and a maximum switch voltage of 35V, so this limits maximum input voltage to 30V, or 35V – $V_{BATTERY}$, whichever is less.

The dual function S/S pin provides easy shutdown and synchronization. It is logic level compatible and can be pulled high or left floating for normal operation. A logic low on the S/S pin activates shutdown, reducing input supply current to 12μA. To synchronize switching, drive the S/S pin between 600kHz and 800kHz.

More Information

For further LT1512 characteristics and applications information, please consult the LT1372 data sheet. Except for the error amplifier circuitry, the LT1512 is similar to the LT1372.

LTC1522

4-Channel, 3V Micropower Sampling 12-Bit Serial I/O A/D Converter

June 1995

FEATURES

- **12-Bit Resolution**
- **Auto Shutdown to 1nA**
- **Guaranteed ±3/4LSB Max DNL**
- Low Supply Current: 160µA
- Single Supply 3V Operation
- 4-Channel Multiplexer
- On-Chip Sample-and-Hold
- Conversion Time: 60µs
- Sampling Rates: 10.5ksps
- I/O Compatible with SPI, MICROWIRE™, etc.
- 16-Pin SO Package

APPLICATIONS

- Pen Screen Digitizing
- Battery-Operated Systems
- Remote Data Acquisition
- Isolated Data Acquisition
- Battery Monitoring
- Temperature Measurement

DESCRIPTION

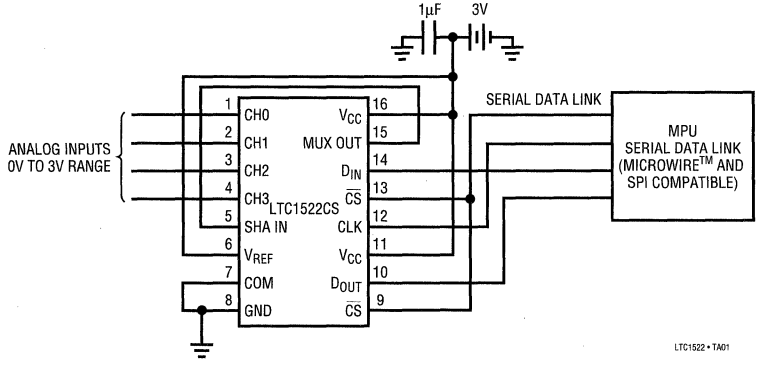
The LTC®1522 is a 4-channel, 3V micropower, 12-bit sampling A/D converter. Whenever it is not performing conversions, it typically draws only 160µA of supply current when converting and automatically powering down to a typical supply current of 1nA. The LTC1522 is available in a 16-pin SOIC package and operates on a 3V supply. The 12-bit, switched-capacitor, successive approximation ADC includes a software configurable 4-channel MUX as well as sample-and-hold.

On-chip serial ports allow efficient data transfer to a wide range of microprocessors and microcontrollers over three wires. This, coupled with micropower consumption, makes remote location possible and facilitates transmitting data through isolation barriers.

The circuit can be used in ratiometric applications or with an external reference. The high impedance analog inputs and the ability to operate with reduced spans (to 1.5V full scale) allow direct connection to sensors and transducers in many applications, eliminating the need for gain stages.

TYPICAL APPLICATION

12µW, 4-Channel, 12-Bit ADC Samples at 200Hz and Runs Off a 3V Battery



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND 12V

Voltage

- Analog Reference ..... −0.3V to (V_{CC} + 0.3V)
- Analog Input ..... −0.3V to (V_{CC} + 0.3V)
- Digital Inputs ..... −0.3V to 12V
- Digital Output ..... −0.3V to (V_{CC} +0.3V)

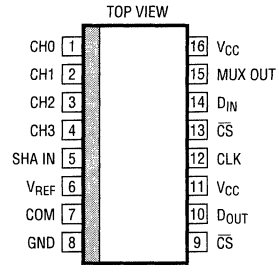
Power Dissipation 500mW

Operating Temperature Range ..... 0°C to 70°C

Storage Temperature Range ..... −65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 120°C/W

ORDER PART NUMBER
LTC1522CS

Consult factory for Industrial and Military grade parts.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage (Note 3)		2.7		3.6	V
f_{CLK}	Clock Frequency	V_{CC} = 2.7V	(Note 4)		200	kHz
t_{CYC}	Total Cycle Time	f_{CLK} = 200kHz	95			µs
t_{hDI}	Hold Time, D_{IN} After CLK↑	V_{CC} = 2.7V	450			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Operating Sequence)	V_{CC} = 2.7V	2			µs
t_{suDI}	Setup Time, D_{IN} Stable Before CLK↑	V_{CC} = 2.7V	600			ns
t_{WHCLK}	CLK High Time	V_{CC} = 2.7V	1.5			µs
t_{WLCLK}	CLK Low Time	V_{CC} = 2.7V	1.5			µs
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time Between Data Transfer Cycles	f_{CLK} = 200kHz	25			µs
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	f_{CLK} = 200kHz	70			µs

CONVERTER AND MULTIPLEXER CHARACTERISTICS (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	12			Bits
Integral Linearity Error	(Note 6)	●			±3	LSB
Differential Linearity Error		●			±3/4	LSB
Offset Error		●			±3	LSB
Gain Error		●			±8	LSB
VREF Input Range	(Notes 7, 8)		1.5V to V_{CC} + 0.05V			V
Analog Input Range	(Notes 7, 8)		−0.05V to V_{CC} + 0.05V			V
Analog Input Leakage Current	(Note 9)	●			±1	µA

DYNAMIC ACCURACY (Note 5) f_{SMPL} = 10.5kHz

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	1kHz Input Signal		68		dB
THD	Total Harmonic Distortion (Up to 5th Harmonic)	1kHz Input Signal		−78		dB
SFDR	Spurious-Free Dynamic Range	1kHz Input Signal		80		dB
	Peak Harmonic or Spurious Noise	1kHz Input Signal		−80		dB

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DIGITAL AND DC ELECTRICAL CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA V_{CC} = 2.7V, I_O = 360µA	● ●	2.40 2.10	2.64 2.30		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = High	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			15		mA
R_{REF}	Reference Input Resistance	$\overline{CS} = V_{IH}$ $\overline{CS} = V_{IL}$			2700 60		MΩ kΩ
I_{REF}	Reference Current	$\overline{CS} = V_{CC}$ $t_{CYC} \geq 760\mu s$, $f_{CLK} \leq 25kHz$ $t_{CYC} \geq 95\mu s$, $f_{CLK} \leq 200kHz$	● ●		0.001 50 50	2.5 70	µA µA µA
I_{CC}	Supply Current	$\overline{CS} = V_{CC}$, CLK = V_{CC}, $D_{IN} = V_{CC}$ $t_{CYC} \geq 760\mu s$, $f_{CLK} \leq 25kHz$ $t_{CYC} \geq 95\mu s$, $f_{CLK} \leq 200kHz$	● ●		0.001 160 160	±3 320	µA µA µA

AC CHARACTERISTICS (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SMPL}	Analog Input Sample Time	See Operating Sequence 1			1.5		CLK Cycles
$t_{SMPL(MAX)}$	Maximum Sampling Frequency	See Operating Sequence 1		10.5			kHz
t_{CONV}	Conversion Time	See Operating Sequence 1			12		CLK Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		600	1500	ns
t_{dis}	Delay Time, CS↑ to D_{OUT} Hi-Z	See Test Circuits	●		220	600	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		180	500	ns
t_{hDO}	Time Output Data Remains Valid After CLK↓	C_{LOAD} = 100pF			520		ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		60	180	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		80	180	ns
t_{ON}	Enable Turn-On Time	See Operating Sequence 1			490	700	ns
t_{OFF}	Enable Turn-Off Time	See Operating Sequence 2			190	300	ns
t_{OPEN}	Break-Before-Make Interval			125	290		ns
C_{IN}	Input Capacitance	Analog Inputs On-Channel Off-Channel Digital Input			20 5 5		pF pF pF

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: This device is specified at 2.7V. Consult factory for 5V specified devices.

Note 4: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $f_{CLK} \geq 120kHz$ at 70°C and $f_{CLK} \geq 1kHz$ at 25°C.

Note 5: V_{CC} = 2.7V, V_{REF} = 2.5V and CLK = 200kHz unless otherwise specified.

Note 6: Linearity error is specified between the actual end points of the A/D transfer curve.

Note 7: Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below GND or one diode drop above V_{CC}. This spec allows 50mV forward bias of either diode for $2.7V \leq V_{CC} \leq 3.6V$. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 3V input voltage range will therefore require a minimum supply voltage of 2.950V over initial tolerance, temperature variations and loading.

Note 8: Recommended operating condition.

Note 9: Channel leakage current is measured after the channel selection.

PIN FUNCTIONS

CH0 (Pin 1): Analog Multiplexer Input.

CH1 (Pin 2): Analog Multiplexer Input.

CH2 (Pin 3): Analog Multiplexer Input.

CH3 (Pin 4): Analog Multiplexer Input.

SHA IN (Pin 5): Sample-and-Hold Amplifier Input. This input is the positive analog input to the ADC. Tie to MUX OUT for normal operation.

V_{REF} (Pin 6): Reference Input. The reference input defines the span of the A/D converter.

COM (Pin 7): Negative Analog Input. This input is the negative analog input to the ADC and must be free of noise with respect to GND.

GND (Pin 8): Analog Ground. GND should be tied directly to an analog ground plane.

$\overline{CS}$ (Pin 9): Chip Select Input. A logic high on this input allows the LTC1522 to select a particular channel. A logic low on this input enables the LTC1522 to sample the selected channel and start the conversion.

D_{OUT} (Pin 10): Digital Data Output. The A/D conversion result is shifted out of this output.

V_{CC} (Pin 11): Power Supply Voltage. This pin provides power to the A/D converter. It must be bypassed directly to the analog ground plane.

CLK (Pin 12): Shift Clock. This clock synchronizes the serial data transfer.

$\overline{CS}$ (Pin 13): Chip Select Input. This input should be tied to pin 9.

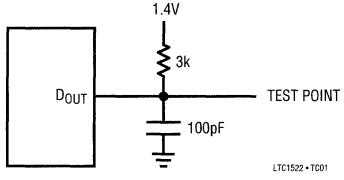
D_{IN} (Pin 14): Digital Data Input. The multiplexer address is shifted into this input.

MUX OUT (Pin 15): MUX Output. This pin is the output of the multiplexer. Tie to SHA IN for normal operation.

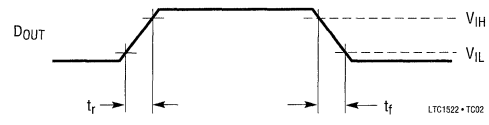
V_{CC} (Pin 16): Power Supply Voltage. This pin should be tied to pin 11.

TEST CIRCUITS

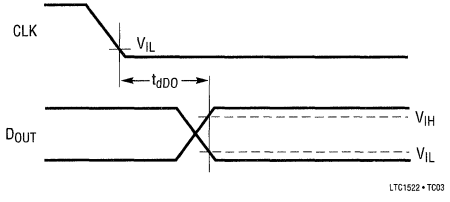
Load Circuit for t_{dDO}, t_r and t_f



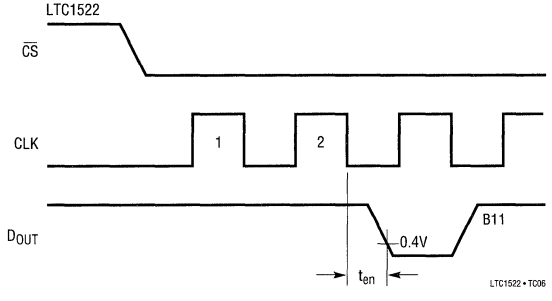
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}

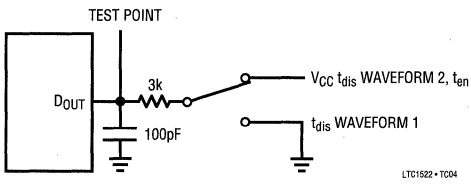


Voltage Waveforms for t_{en}

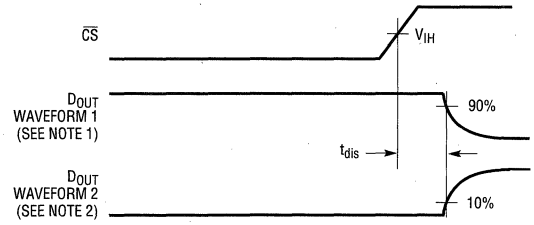


TEST CIRCUITS

Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

LTC1522 • TC05

APPLICATIONS INFORMATION

INPUT DATA WORD

The LTC1522 uses $\overline{CS}$ and D_{IN} to select one of its four channels as shown in the operating sequence figures and Table 1.

When $\overline{CS}$ is high, the input data on the D_{IN} pin is latched into the four-bit shift register on the rising edge of the clock. The input data word consists of an "EN" bit and a string of three bits for channel selection. If the "EN" bit is logic high as illustrated in Operating Sequence 1, it enables the selected channel. To ensure correct operation, the $\overline{CS}$ must be pulled low before the next rising edge of the clock. More than four input bits can be sent to the ADC without problems. The channel will be determined by the last four bits clocked in before $\overline{CS}$ falls.

Once the $\overline{CS}$ is pulled low, all channels are simultaneously switched off to ensure a break-before-make interval. After a delay of t_{ON}, the selected channel is switched on allowing signal transmission. The selected channel remains on until the next falling edge of $\overline{CS}$; and after a delay of t_{OFF}, it turns off and subsequently allows the selection of the next channel. If the "EN" bit is logic low, as illustrated in Operating Sequence 2, it disables all channels. Table 1 shows the various bit combinations for channel selection.

Table 1. Logic Table for Channel Selection

Channel Status	EN	D2	D1	D0
All Off	0	X	X	X
CH0	1	0	0	0
CH1	1	0	0	1
CH2	1	0	1	0
CH3	1	0	1	1

ANALOG CONSIDERATIONS

Grounding

The LTC1522 should be used with an analog ground plane and single-point grounding techniques. Do not use wire-wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance use a printed circuit board. The Ground pin (Pin 8) should be tied directly to the ground plane with minimum lead length.

Bypassing

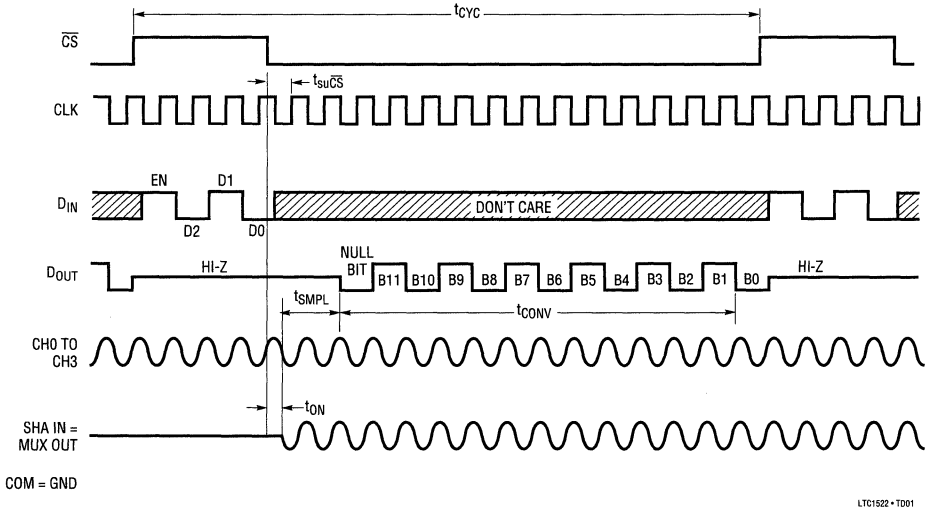
For good performance, the LTC1522 V_{CC} and V_{REF} pins must be free of noise and ripple. Any changes in the V_{CC}/V_{REF} voltage with respect to ground during the conversion cycle can induce errors or noise in the output code. Bypass the V_{CC}/V_{REF} pin directly to the analog ground plane with a minimum of a 0.1µF capacitor and leads as short as possible.

IPPLICATIONS INFORMATION

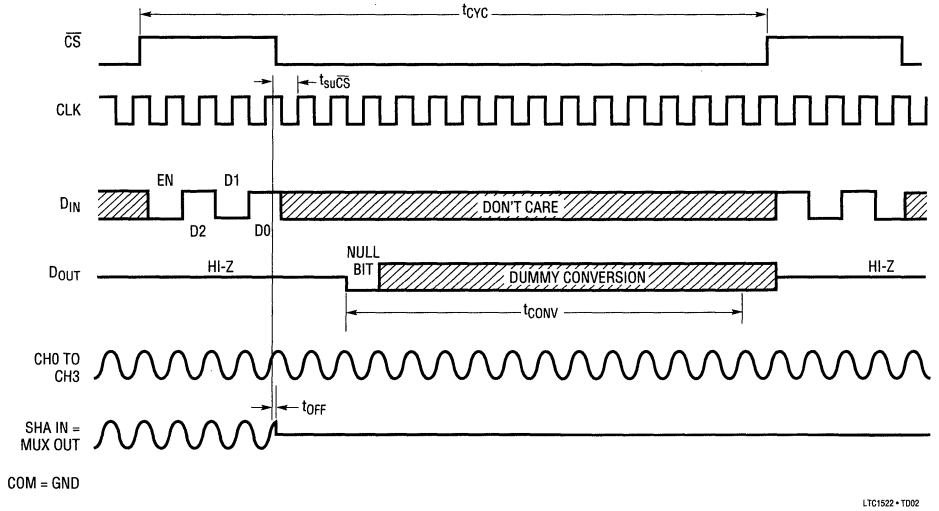
nalog Inputs

ecause of the capacitive redistribution A/D conversion chniques used, the analog inputs of the LTC1522 have apacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. But if large source resistances are used or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.

Operating Sequence 1
Example: (CH2, GND)



Operating Sequence 2
Example: (ALL Channels Off)



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TYPICAL APPLICATIONS

Microprocessor Interfaces

The LTC1522 can interface directly (without external hardware) to most popular microprocessors' (MPU) synchronous serial formats (see Table 2). If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1522. Included here is one serial interface example.

Table 2. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1522**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPi
Hitachi	
HD6305	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE
COP800 Family	MICROWIRE/PLUS™
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port
TMS370C050	SPI

* Requires external hardware.

** Contact factory for interface information for processors not on this list.

MICROWIRE/PLUS is a trademark of National Semiconductor Corp.

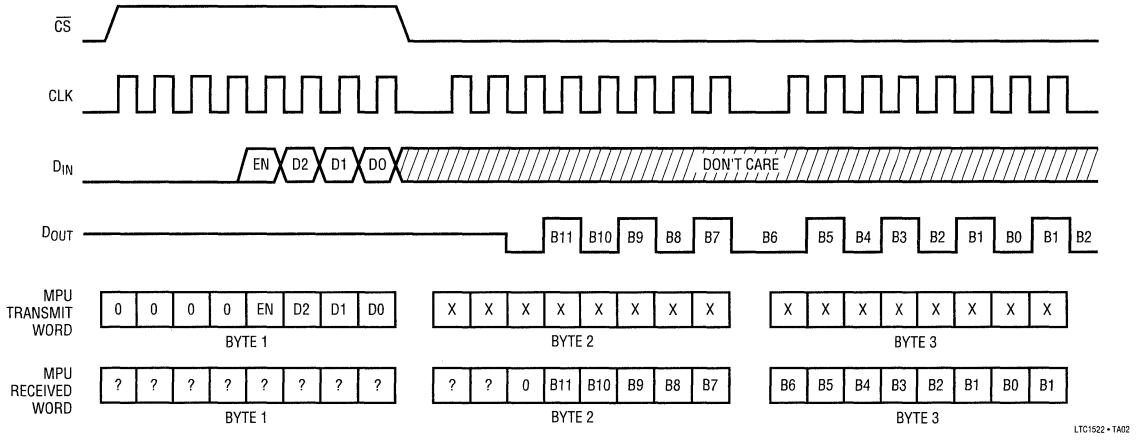
Motorola SPI (MC68HC05)

The MC68HC05 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB first and in 8-bit increments. The D_{IN} word sent to the data register starts the SPI process. With three 8-bit transfers the A/D result is read into the MPU. The second 8-bit transfer clocks B11 through B7 of the A/D conversion result into the processor. The third 8-bit transfer clocks the remaining bits B6 through B0 into the MPU. ANDing the second byte with $1F_{HEX}$ clears the three most significant bits and ANDing the third byte with FE_{HEX} clears the least significant bit.

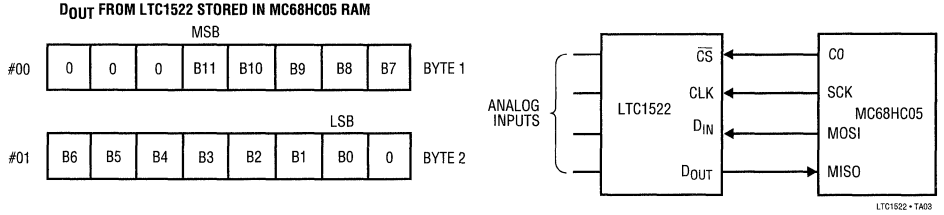
MC68HC05 CODE			
	LDA	#$52	Configuration data for serial peripheral control register (Interrupts disabled, output enabled, master, Norm = 0, Ph = 0, Clk/16)
	STA	$0A	Load configuration data into location $0A (SPCR)
	LDA	#$FF	Configuration data for I/O ports (all bits are set as outputs)
	STA	$04	Load configuration data into Port A DDR ($04)
	STA	$05	Load configuration data into Port B DDR ($05)
	STA	$06	Load configuration data into Port C DDR ($06)
	LDA	#$08	Put D_{IN} word for LTC1522 into Accumulator (CH0 with respect to GND)
	STA	$50	Load D_{IN} word into memory location $50
START	BSET	0,$02	Bit 0 Port C ($02) goes high ($\overline{CS}$ goes high)
	LDA	$50	Load D_{IN} word at $50 into Accumulator
	STA	$0C	Load D_{IN} word into SPI data register ($0C) and start clocking data
LOOP1	TST	$0B	Test status of SPIF bit in SPI status register ($0B)
	BPL	LOOP1	Loop if not done with transfer to previous instruction
	BCLR	0,$02	Bit 0 Port C ($02) goes low ($\overline{CS}$ goes low)
	LDA	$0C	Load contents of SPI data register into Accumulator
	STA	$0C	Start next SPI cycle
LOOP2	TST	$0B	Test status of SPIF
	BPL	LOOP2	Loop if not done
	LDA	$0C	Load contents of SPI data register into Accumulator
	STA	$0C	Start next SPI cycle
	AND	#$IF	Clear 3 MSBs of first D_{OUT} word
	STA	$00	Load Port A ($00) with MSBs
LOOP3	TST	$0B	Test status of SPIF
	BPL	LOOP3	Loop if not done
	LDA	$0C	Load contents of SPI data register into Accumulator
	AND	#$FE	Clear LSB of second D_{OUT} word
	STA	$01	Load Port B ($01) with LSBs
	JMP	START	Go back to start and repeat program

TYPICAL APPLICATIONS

Data Exchange Between LTC1522 and MC68HC05



Hardware and Software Interface to Motorola MC68HC05



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1096/LTC1098	8-Pin SO, Micropower 8-Bit ADC	Low Power, Small Size, Low Cost
LTC1196/LTC1198	8-Pin SO, 1Msps 8-Bit ADC	Low Power, Small Size, Low Cost
LTC1282	3V High Speed Parallel 12-Bit ADC	140ksps, Complete with V_{REF}, CLK, Sample-and-Hold
LTC1285/LTC1288	8-Pin SO, 3V Micropower 12-Bit ADC	12-Bit ADC in SO-8
LTC1289	Mutiplexed 3V 1A 12-Bit ADC	8-Channel 12-Bit Serial I/O

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PRELIMINARY

LTC1550/LTC1551

Low Noise, Switched Capacitor-Regulated Voltage Inverters

June 1995

FEATURES

- **Regulated Negative Voltage from Single Positive Supply**
- **Low Output Ripple: Less Than 1mV Typ**
- **High Charge Pump Frequency: 900kHz Typ**
- **REG Output Indicates Output Is in Regulation**
- Small Charge Pump Capacitors: 0.1µF
- Requires Only Four External Capacitors
- Fixed –4.1V or Adjustable Output
- Shutdown Mode Drops Supply Current to 1µA
- Output Current: Up to 20mA
- Output Regulation: 5%
- Available in 8-Pin SO and 16-Pin SSOP Packages

APPLICATIONS

- GaAs FET Bias Generators
- Negative Supply Generators
- Battery-Powered Systems
- Single Supply Applications

DESCRIPTION

The LTC®1550/LTC1551 are switched-capacitor voltage inverters with internal linear post regulators. Each is available in a fixed –4.1V version while the LTC1550 also offers an adjustable output voltage version. Typical output ripple is below 1mV. The LTC1550/LTC1551 are designed for use as bias voltage generators for GaAs transmitter FETs in portable RF and cellular telephone applications.

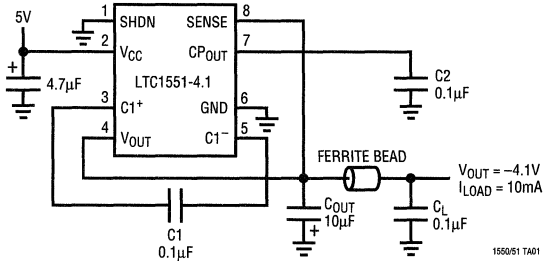
The LTC1550/LTC1551 operate from a single 4.5V to 6.5V supply, with a typical quiescent current of 5mA at V_{CC} = 5V. Both devices include a TTL compatible shutdown pin which drops supply current to 0.2µA typically. The LTC1550 shutdown pin is active low ($\overline{SHDN}$) while the LTC1551 shutdown pin is active high (SHDN). Only four external components are required for fixed output parts: an input bypass capacitor, two 0.1µF charge pump capacitors and a 10µF filter capacitor at the linear regulator output. Adjustable parts require two additional resistors to set the output voltage.

Each version of the LTC1550/LTC1551 will supply up to 20mA output current with guaranteed output regulation of ±5%. The 16-pin version of the LTC1550/LTC1551 includes an open-drain REG output which pulls low to indicate that the output is within 5% of the set value.

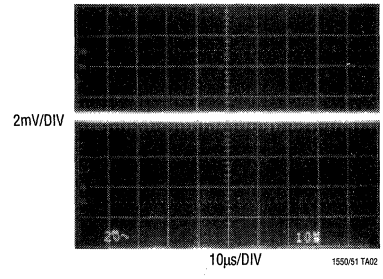
For applications with V_{CC} supplies as low as 3V, see the LTC1261. For applications requiring an external synchronization clock and V_{CC} as low as 3V, see the LTC1429.

TYPICAL APPLICATION

–4V Generator with 1mV$_{P-P}$ Noise



V_{OUT} Output Noise and Ripple



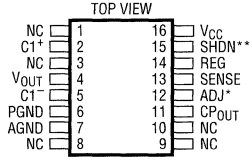
ıBSOLUTE MAXIMUM RATINGS

lote 1)

upply Voltage (Note 2) 7V
utput Voltage ..... 0.3V to (V_{CC} – 14V)
otal Voltage, V_{CC} to CP_{OUT} (Note 2) 14V
ıput Voltage (SHDN Pin) ..... –0.3V to (V_{CC} + 0.3V)
ıput Voltage (REG Pin) ..... –0.3V to 12V

Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range ..... 0°C to 70°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

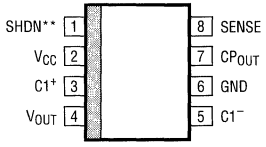
'ACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1550CGN LTC1550CGN-4.1 LTC1551CGN-4.1
GN PART MARKING
1550 15504I 15514I



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 150°C/W

ORDER PART NUMBER
LTC1550CS8-4.1 LTC1551CS8-4.1
S8 PART MARKING
15504 15514

ınsult factory for Industrial and Military grade parts.

* NC for fixed output versions.
** $\overline{SHDN}$ for LTC1550, SHDN for LTC1551

LECTRICAL CHARACTERISTICS (Note 3)

C = 4.5V to 6.5V, C1 = C2 = 0.1µF, C_{OUT} = 10µF, unless otherwise specified.

MBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C	Supply Voltage	(Note 2)		4.5		6.5	V
EF	Reference Voltage				1.24		V
	Supply Current	V_{SHDN} = GND (LTC1551)or V_{CC} (LTC1550)	●		5.0	7.0	mA
		V_{SHDN} = V_{CC} = 5V (LTC1551) or GND (LTC1550)	●		0.2	10.0	µA
SC	Internal Oscillator Frequency				900		kHz
L	REG Output Low Voltage	I_{REG} = 1mA, V_{CC} = 5V	●		0.1	0.8	V
EG	REG Sink Current	V_{REG} = 0.8V, V_{CC} = 5V	●	8	15		mA
H	SHDN Input High Voltage		●	2.0			V
L	SHDN Input Low Voltage		●			0.8	V
	SHDN Input Current	V_{SHDN} = V_{CC}	●		0.1	1	µA
N	Turn On Time	I_{OUT} = 10mA			1		ms

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ELECTRICAL CHARACTERISTICS (Note 3)

V_S = 4.5V to 6.5V, C1 = C2 = 0.1μF, C_{OUT} = 10μF, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔV_{OUT}	Output Regulation (LTC1550 Only)	V_{CC} = 5V, 0 ≤ I_{OUT} ≤ 10mA	●		1	5	%
		V_{CC} = 6V, 0 ≤ I_{OUT} ≤ 20mA	●		1	5	%
V_{OUT}	Output Voltage (LTC1550-4.1, LTC1551-4.1)	V_{CC} = 4.5V, 0 ≤ I_{OUT} ≤ 5mA	●	–3.9	–4.1	–4.3	V
		V_{CC} = 5V, 0 ≤ I_{OUT} ≤ 10mA	●	–3.9	–4.1	–4.3	V
		V_{CC} = 6V, 0 ≤ I_{OUT} ≤ 20mA	●	–3.9	–4.1	–4.3	V
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 5V	●		50	125	mA
		V_{OUT} = 0V, V_{CC} = 6V	●		60	125	mA
V_{RIPPLE}	Output Ripple Voltage				1		mV

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The output should never be set to exceed V_{CC} – 14V.

Note 3: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified. All typicals are given at T_A = 25°C.

PIN FUNCTIONS

SHDN: Shutdown (TTL Compatible). This pin is active low ($\overline{SHDN}$) for the LTC1550 and active high (SHDN) for the LTC1551. When this pin is at V_{CC} (GND for LTC1551), the LTC1550 operates normally. When SHDN is pulled LOW (HIGH for LTC1551), the LTC1550 enters shutdown mode. In shutdown, the charge pump stops, the output collapses to 0V, and the quiescent current drops typically to 0.2μA.

V_{CC}: Power Supply. V_{CC} requires an input voltage between 4.5V and 6.5V. The difference between the input voltage and output should never be set to exceed 14V or damage to the chip may occur. V_{CC} must be bypassed to PGND (GND for the 8-pin package) with at least a 1μF capacitor placed in close proximity to the chip. A 4.7μF or larger bypass capacitor is recommended to minimize noise and ripple at the output.

C1⁺: C1 Positive Input. Connect a 0.1μF capacitor between C1⁺ and C1⁻.

V_{OUT}: Negative Voltage Output. This pin must be bypassed to ground with a 4.7μF or larger capacitor to ensure regulator loop stability. At least 10μF is recommended to provide specified output ripple. An additional low ESR 0.1μF capacitor is recommended to minimize high frequency spikes at the output.

C1⁻: C1 Negative Input. Connect a 0.1μF capacitor from C1⁺ to C1⁻.

GND: Ground. Connect to a low impedance ground. A ground plane will help minimize regulation errors.

CP_{OUT}: Negative Charge Pump Output. This pin requires a 0.1μF storage capacitor to ground.

SENSE: Connect to V_{OUT}. The LTC1550/LTC1551 internal regulator uses this pin to sense the output voltage. For optimum regulation, SENSE should be connected close to the output load.

16-Pin SSOP Only

PGND: Power Ground. Connect to a low impedance ground. PGND should be connected to the same potential as AGND.

AGND: Analog Ground. Connect to a low impedance ground. AGND should be connected to a ground plane to minimize regulation errors.

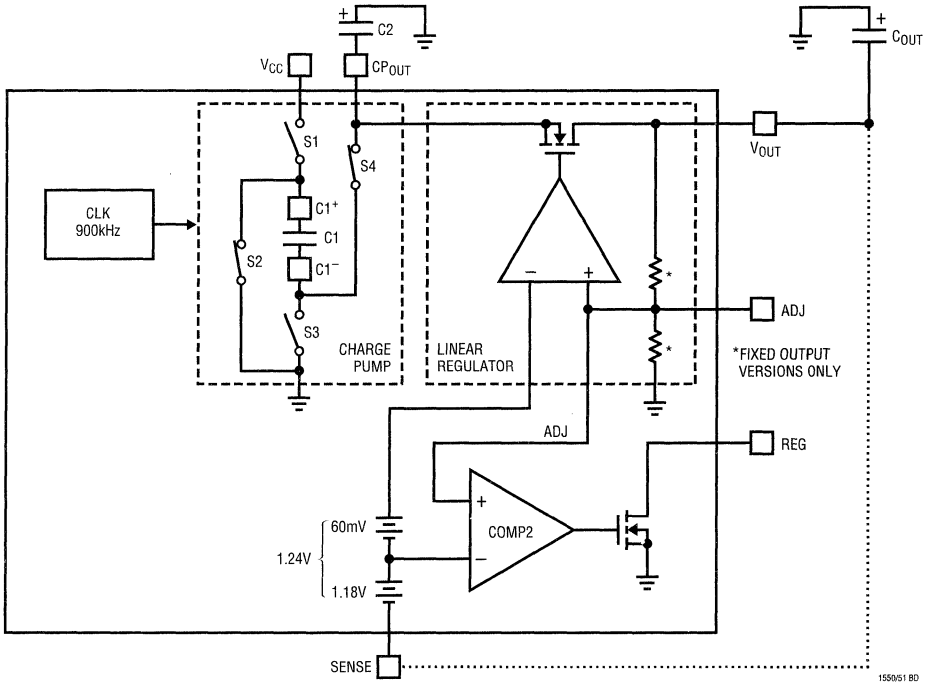
REG: This is an open-drain output that pulls low when the output voltage is within 5% of the set value. It will sink 8mA to ground with a 5V supply. The external circuitry must provide a pull-up or REG will not swing high. The voltage at REG may exceed V_{CC} and can be pulled up to 12V above ground without damage.

PIN FUNCTIONS

ADJ: For adjustable versions only, this is the feedback point for the external resistor divider string. Connect a divider string from AGND to V_{OUT} with the divided tap connected to ADJ. Note that the resistor string needs to be connected "upside-down" from a traditional negative regulator. See the Applications Information section for hook-up details.

NC: No Internal Connection.

BLOCK DIAGRAM



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APPLICATIONS INFORMATION

THEORY OF OPERATION

The LTC1550/LTC1551 are switched-capacitor, inverting charge pumps with integral linear post regulators to provide a regulated, low ripple negative output voltage. The charge pump runs at a high 900kHz frequency to keep noise out of the 400kHz to 600kHz IF bands commonly used by portable radio frequency systems, and to minimize the size of the external capacitors required. The LTC1550/LTC1551 require only two external 0.1µF charge pump capacitors: an input bypass capacitor and a single output capacitor. At least 4.7µF is required at the output to maintain loop stability; for optimum output stability over temperature and minimum ripple, 10µF or greater is recommended.

The LTC1550 features an active-low shutdown pin which drops quiescent current to below 1µA. The LTC1551 is identical to the LTC1550 but the shutdown pin is active high. Both the LTC1550/LTC1551 are available with fixed –4.1V output voltage, and the LTC1550 is also available in an adjustable output version. Both devices can be configured with other output voltages. Contact the Linear Technology marketing for more information.

Minimizing Output Noise and Ripple

Output ripple is largely eliminated by the internal linear regulator. It is typically below $1mV_{P-P}$ with output loads between zero and 10mA. Residual ripple is at the 900kHz switching frequency of the charge pump and is usually not a problem in most systems. This high frequency ripple can be minimized by using a low ESR capacitor at the output. An 0.1µF ceramic capacitor in parallel with a 10µF tantalum makes a good combination.

Figure 1a shows the test circuit used for spectrum analysis with test conditions V_{CC} = 6V, I_{OUT} = 5mA. Figures 1b and 1c are the V_{OUT} spectrum plots for the test circuit in Figure 1a, covering from 100Hz to 1MHz and to 10MHz respectively. The fundamental switching frequency appears at 900kHz.

Output ripple can be further reduced by increasing the size of the output capacitor, or by including a small external RC or LC filter at the output. A ferrite bead in series with the output capacitor will reduce the output ripple to negligible levels.

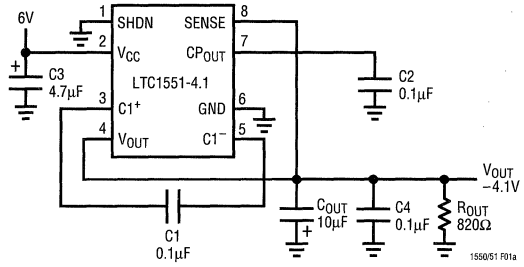


Figure 1a. Test Circuit Used for Spectrum Analysis

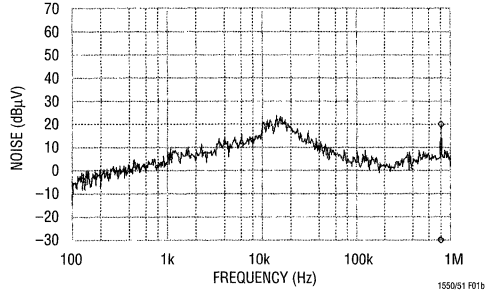


Figure 1b. Spectrum Plot of V_{OUT} from 100Hz to 1MHz

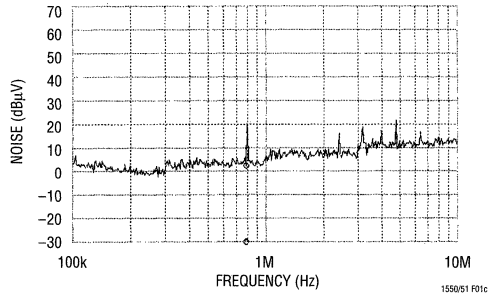


Figure 1c. Spectrum Plot of V_{OUT} from 100kHz to 10MHz

Output load and line transient response can be optimized by increasing the size of the output bypass capacitor. Adjustable parts can further improve transient response by bypassing the upper resistor R1 (Figure 2) in the feedback divider with a capacitor. A 100pF bypass capacitor is usually adequate.

APPLICATIONS INFORMATION

Adjustable Hookup

The LTC1550 is available in an adjustable output version in the 16-pin SSOP package. The output voltage is set with a resistor divider from GND to SENSE/V_{OUT} (Figure 2). Note that the internal reference and the internal feedback amplifier are set up as a positive-output regulator referenced to the SENSE pin, not a negative regulator referenced to ground. The output resistor divider must be set to provide a 1.24V at the ADJ pin with respect to V_{OUT}. For example, a –3.0V output would require a 13k resistor from GND to ADJ, and a 9.1k resistor to SENSE/V_{OUT}. If, after connecting the divider resistors, the output voltage is not what you expected, try swapping them.

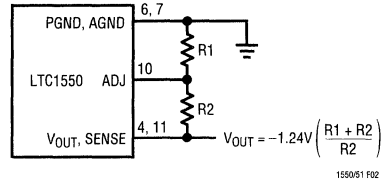
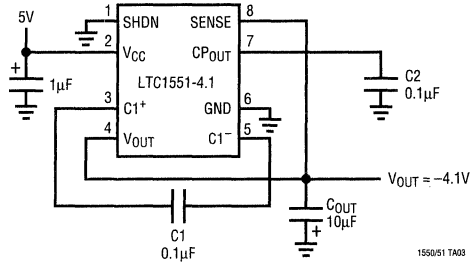


Figure 2. External Resistor Connections

TYPICAL APPLICATION

Minimum Part Count, Negative –4.1V Generator



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1054	Switched Capacitor Voltage Converter with Regulator	100mA Switched Capacitor Converter
LTC1261	Switched Capacitor Regulated Voltage Inverter	Selectable Fixed Output Voltages
LTC1429	Clock-Synchronized Switched Capacitor Voltage Inverter	Synchronizable

LT1580/LT1580-2.5

7A, Very Low Dropout Regulator

June 1995

FEATURES

- **Low Dropout, 540mV at 7A Output Current in Dual Supply Mode**
- **Fast Transient Response**
- **Remote Sense**
- 1mV Load Regulation
- Fixed 2.5V Output and Adjustable Output
- No Supply Sequencing Problems in Dual Supply Mode

APPLICATIONS

- Microprocessor Supplies
- Post Regulators for Switching Supplies
- High Current Regulators
- 5V to 3.XXV for Pentium® Processors Operating at 90MHz, 100MHz, 120MHz and Beyond
- 3.3V to 2.9V for Portable Pentium Processor
- Power PC™ Series

DESCRIPTION

The LT®1580 is a 7A low dropout regulator designed to power the new generation of microprocessors. The dropout voltage of this device is 100mV at light loads rising to just 540mV at 7A. To achieve this dropout a second low current input voltage, 1V greater than the output voltage, is required. The device can also be used as a single supply device where dropout is comparable to an LT1584. Several other new features have been added to this device.

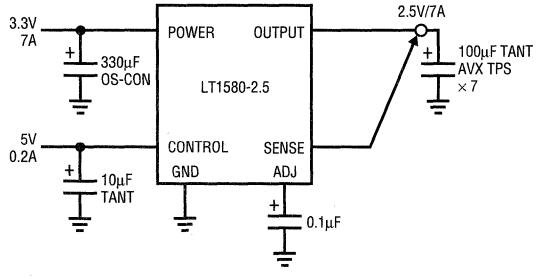
A remote Sense pin is brought out. This feature virtually eliminates output voltage variations due to load changes. Typical load regulation, measured at the Sense pin, for a load current step of 100mA to 7A is less than 1mV.

The LT1580 has fast transient response, equal to the LT1584. On fixed voltage devices, the Adjust pin is brought out. A small capacitor on the Adjust pin further improves transient response.

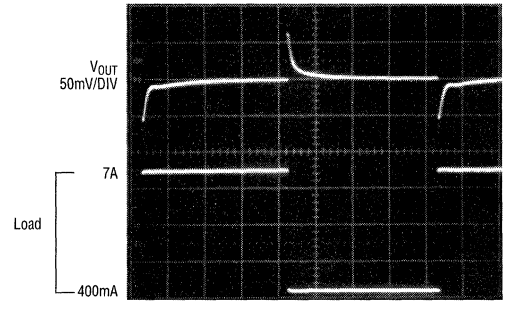
This device is ideal for generating processor supplies of 2V to 3V on motherboards where both 5V and 3.3V supplies are available.

TYPICAL APPLICATION

2.5V Microprocessor Supply



Load Current Step Response



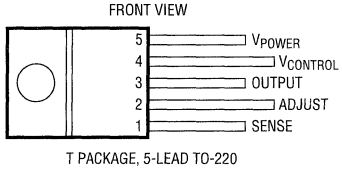
ABSOLUTE MAXIMUM RATINGS

V_{POWER} Input Voltage 6V
$V_{CONTROL}$ Input Voltage 13V
Storage Temperature ..... –65°C to 150°C
Operating Junction Temperature Range
Control Section ..... 0°C to 125°C
Power Transistor ..... 0°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PRECONDITIONING

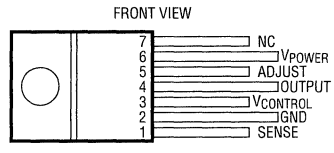
100% Thermal Limit Functional Test

PACKAGE/ORDER INFORMATION



T PACKAGE, 5-LEAD TO-220
θ_{JA} = 50°C/W

ORDER PART NUMBER
LT1580CT



T7 PACKAGE, 7-LEAD TO-220
θ_{JA} = 50°C/W

ORDER PART NUMBER
LT1580CT7-2.5

Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage - LT1580-2.5	$V_{CONTROL}$ = 5V, V_{POWER} = 3.3V, I_{LOAD} = 0mA		2.485	2.500	2.515	V
	$V_{CONTROL}$ = 4V to 12V, V_{POWER} = 3V to 5.5V, I_{LOAD} = 0mA to 4A	●	2.475	2.500	2.525	V
	$V_{CONTROL}$ = 4V to 12V, V_{POWER} = 3.3V to 5.5V, I_{LOAD} = 0mA to 7A	●	2.475	2.500	2.525	V
Reference Voltage - LT1580 (V_{ADJ} = 0)	$V_{CONTROL}$ = 2.75V, V_{POWER} = 2V, I_{LOAD} = 10mA		1.243	1.250	1.257	V
	$V_{CONTROL}$ = 2.7V to 12V, V_{POWER} = 1.75V to 5.5V, I_{OUT} = 10mA to 4A	●	1.237	1.250	1.263	V
	$V_{CONTROL}$ = 2.7V to 12V, V_{POWER} = 2.05V to 5.5V, I_{OUT} = 10mA to 7A	●	1.237	1.250	1.263	V
Line Regulation - LT1580-2.5	$V_{CONTROL}$ = 3.65V to 12V, V_{POWER} = 3V to 5.5V, I_{LOAD} = 10mA	●		1	3	mV
LT1580	$V_{CONTROL}$ = 2.5V to 12V, V_{POWER} = 1.75V to 5.5V, I_{LOAD} = 10mA	●		1	3	mV
Load Regulation - LT1580-2.5	$V_{CONTROL}$ = 5V, V_{POWER} = 3.3V, I_{LOAD} = 0mA to 7A	●		1	5	mV
LT1580 (V_{ADJ} = 0V)	$V_{CONTROL}$ = 2.75V, V_{POWER} = 2.1V, I_{LOAD} = 10mA to 7A	●		1	5	mV
Minimum Load Current - LT1580	$V_{CONTROL}$ = 5V, V_{POWER} = 3.3V, V_{ADJ} = 0V (Note 3)	●		5	10	mA
Control Pin Current - LT1580-2.5 (Note 4)	$V_{CONTROL}$ = 5V, V_{POWER} = 3.3V, I_{LOAD} = 100mA	●		6	10	mA
	$V_{CONTROL}$ = 5V, V_{POWER} = 3.3V, I_{LOAD} = 4A	●		30	60	mA
	$V_{CONTROL}$ = 5V, V_{POWER} = 3V, I_{LOAD} = 4A	●		33	70	mA
	$V_{CONTROL}$ = 5V, V_{POWER} = 3.3V, I_{LOAD} = 7A	●		60	120	mA
Control Pin Current - LT1580 (Note 4)	$V_{CONTROL}$ = 2.75V, V_{POWER} = 2.05V, I_{LOAD} = 100mA	●		6	10	mA
	$V_{CONTROL}$ = 2.75V, V_{POWER} = 2.05V, I_{LOAD} = 4A	●		30	60	mA
	$V_{CONTROL}$ = 2.75V, V_{POWER} = 1.75V, I_{LOAD} = 4A	●		33	70	mA
	$V_{CONTROL}$ = 2.75V, V_{POWER} = 2.05V, I_{LOAD} = 7A	●		60	120	mA
Ground Pin Current - LT1580-2.5	$V_{CONTROL}$ = 5V, V_{POWER} = 3.3V, I_{LOAD} = 0mA	●		6	10	mA
Adjust Pin Current - LT1580 (V_{ADJ} = 0V)	$V_{CONTROL}$ = 2.75V, V_{POWER} = 2.05V, I_{LOAD} = 0mA	●		50	120	µA
Current Limit - LT1580-2.5	$V_{CONTROL}$ = 5V, V_{POWER} = 3.3V, ΔV_{OUT} = 100mV	●	7.1	8		A
LT1580 (V_{ADJ} = 0V)	$V_{CONTROL}$ = 2.75V, V_{POWER} = 2.05V, ΔV_{OUT} = 100mV	●	7.1	8		A
Ripple Rejection - LT1580-2.5	V_C = V_P = 5V Avg, V_{RIPPLE} = $1V_{P-P}$, I_{OUT} = 4A, T_J = 25°C		60	80		dB
LT1580	V_C = V_P = 3.75V Avg, V_{RIPPLE} = $1V_{P-P}$, V_{ADJ} = 0V, I_{OUT} = 4A, T_J = 25°C		60	80		dB

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ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Thermal Regulation	30ms Pulse			0.002	0.020	%/W
Thermal Resistance, Junction-to-Case	T, T7 Packages, Control Circuitry/Power Transistor			0.65	2.70	°C/W
Dropout Voltage (Note 2)						
Minimum $V_{CONTROL}$ - LT1580-2.5 ($V_{CONTROL} - V_{OUT}$)	V_{POWER} = 3.3V, I_{LOAD} = 100mA	●		1.00	1.15	V
	V_{POWER} = 3.3V, I_{LOAD} = 1A	●		1.00	1.15	V
	V_{POWER} = 3.3V, I_{LOAD} = 4A	●		1.06	1.20	V
	V_{POWER} = 3.3V, I_{LOAD} = 7A	●		1.15	1.30	V
Minimum $V_{CONTROL}$ - LT1580 ($V_{CONTROL} - V_{OUT}$) (V_{ADJ} = 0)	V_{POWER} = 2.05V, I_{LOAD} = 100mA	●		1.00	1.15	V
	V_{POWER} = 2.05V, I_{LOAD} = 1A	●		1.00	1.15	V
	V_{POWER} = 2.05V, I_{LOAD} = 2.75A	●		1.05	1.18	V
	V_{POWER} = 2.05V, I_{LOAD} = 4A	●		1.06	1.20	V
	V_{POWER} = 2.05V, I_{LOAD} = 7A	●		1.15	1.30	V
Minimum V_{POWER} - LT1580-2.5 ($V_{POWER} - V_{OUT}$)	$V_{CONTROL}$ = 5V, I_{LOAD} = 100mA	●		0.10	0.17	V
	$V_{CONTROL}$ = 5V, I_{LOAD} = 1A	●		0.15	0.22	V
	$V_{CONTROL}$ = 5V, I_{LOAD} = 4A, T_J = 25°C			0.34	0.40	V
	$V_{CONTROL}$ = 5V, I_{LOAD} = 4A	●			0.50	V
	$V_{CONTROL}$ = 5V, I_{LOAD} = 7A, T_J = 25°C			0.54	0.62	V
	$V_{CONTROL}$ = 5V, I_{LOAD} = 7A	●		0.70	0.80	V
Minimum V_{POWER} - LT1580 ($V_{POWER} - V_{OUT}$) (V_{ADJ} = 0)	$V_{CONTROL}$ = 2.75V, I_{LOAD} = 100mA	●		0.10	0.17	V
	$V_{CONTROL}$ = 2.75V, I_{LOAD} = 1A	●		0.15	0.22	V
	$V_{CONTROL}$ = 2.75V, I_{LOAD} 2.75A	●		0.26	0.38	V
	$V_{CONTROL}$ = 2.75V, I_{LOAD} = 4A, T_J = 25°C			0.34	0.40	V
	$V_{CONTROL}$ = 2.75V, I_{LOAD} = 4A	●			0.50	V
	$V_{CONTROL}$ = 2.75V, I_{LOAD} = 7A, T_J = 25°C			0.54	0.62	V
	$V_{CONTROL}$ = 2.75V, I_{LOAD} = 7A	●		0.70	0.80	V

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Unless otherwise specified $V_{OUT} = V_{SENSE}$. For the LT1580 adjustable device V_{ADJ} = 0V.

Note 2: For the LT1580, dropout is caused by either minimum control voltage ($V_{CONTROL}$) or minimum power voltage (V_{POWER}). Both parameters are specified with respect to the output voltage. The specifications represent the minimum input/output voltage required to maintain 1% regulation.

Note 3: For the LT1580 adjustable device the minimum load current is the minimum current required to maintain regulation. Normally the current in the resistor divider used to set the output voltage is selected to meet the minimum load current requirement.

Note 4: The control pin current is the drive current required for the output transistor. This current will track output current with roughly a 1:100 ratio. The minimum value is equal to the quiescent current of the device.

PIN FUNCTIONS (5-Lead TO-220/7-Lead TO-220)

SENSE (Pin 1): This pin is the positive side of the reference voltage for the device. With this pin it is possible to Kelvin Sense the output voltage at the load.

ADJUST (Pin 2/5): This pin is the negative side of the reference voltage for the device. Transient response can be improved by adding a small bypass capacitor from the Adjust pin to ground. For fixed voltage devices the Adjust pin is also brought out to allow the user to add a bypass capacitor.

GND (Pin 2, 7-Lead Only): For fixed voltage devices this is the bottom of the resistor divider that sets the output voltage.

V_{POWER} (Pin 5/6): This is the collector to the power device of the LT1580. The output load current is supplied through this pin. For the device to regulate, the voltage at this pin must be between 0.1V and 0.8V greater than the output voltage (see Dropout specifications).

$V_{CONTROL}$ (Pin 4/3): This pin is the supply pin for the control circuitry of the device. The current flow into this pin will be about 1% of the output current. For the device to regulate, the voltage at this pin must be between 1.0V and 1.3V greater than the output voltage (see Dropout specifications).

OUTPUT (Pin 3/4): This is the power output of the device.

APPLICATIONS INFORMATION

The LT1580 is a low dropout regulator designed to power the new generation of microprocessors. The device uses a two supply approach to maximize efficiency. The collector of the output power device is brought out to minimize the dropout at high current. A separate input control voltage with an input current of approximately 1% of the output current requires a slightly higher input voltage (1V to 1.5V). The device is designed to take advantage of the fact that most motherboards will have both 5V and 3.3V supplies available. The main output current will come from the 3.3V supply while the 5V supply only has to supply a relatively small drive current.

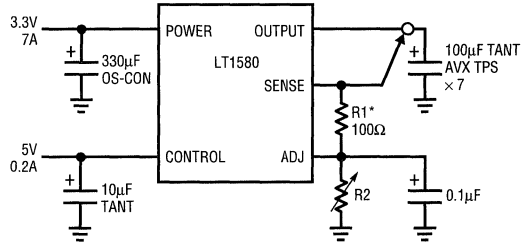
Two other new features have been added to this device. An output sense pin has been added to allow true Kelvin sensing of the output voltage. This feature can virtually eliminate errors in the output voltage due to load regulation. Regulation will be optimum at the point where the sense pin is tied to the output pin. For fixed voltage devices the adjust pin, not normally available, is brought out to allow bypassing. Bypassing the adjust pin with a small capacitor in the range of 0.1µF to 0.3µF can improve transient response significantly. Good transient response becomes even more important as processor operating margins continue to shrink.

Special care has been taken to ensure that there are no supply sequencing problems. The output voltage will not turn on until both supplies are operating. If the control voltage comes up first, the output current will be limited to a few milliamperes until the power input voltage comes up. If the power input comes up first the output will not turn on at all until the control voltage comes up. The output can never come up unregulated.

The LT1580 can also be used as a single supply device with the control and power inputs tied together. In this mode, the dropout will be determined by the minimum control voltage (1.15V to 1.3V).

Adjustable Operation

The output voltage of the LT1580 can be adjusted using a resistor divider as shown in Figure 1. The reference voltage of the device is connected between the sense pin and the adjust pin. R1 should be 100Ω or less to ensure that the minimum load current specification is met.



*MAKING R1 = 100Ω ENSURES THAT MINIMUM OUTPUT CURRENT REQUIREMENT IS MET.

Figure 1. Adjustable Operation

RELATED PARTS

ART NUMBER	DESCRIPTION	COMMENTS
TC®1266	Synchronous Switching Controller	>90% Efficient High Current Microprocessor Supply
TC1267	Dual High Efficiency Synchronous Switching Regulator	>90% Efficiency with Fixed 5V, 3.3V or Adjustable Outputs
T1430	High Power Synchronous Step-Down Switching Regulator	>90% Efficient High Current Microprocessor Supply
T1584	7A Low Dropout Fast Transient Response Regulator	For High Performance Microprocessors
T1585	4.6A Low Dropout Fast Transient Response Regulator	For High Performance Microprocessors
T1587	3A Low Dropout Fast Transient Response Regulator	For High Performance Microprocessors

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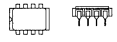
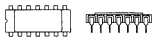
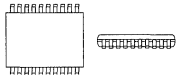
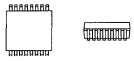
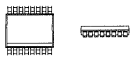
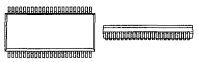
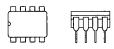
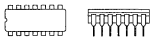
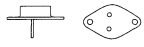
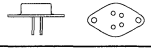
SECTION 14—PACKAGE INFORMATION

SECTION 14—PACKAGE DIMENSIONS

	PACKAGE OUTLINE	DESCRIPTION	LTC	NSC	ADI/PMI		MOT	TI	LINFIN	MAXIM
SIDE BRAZED		8-Lead Side Brazed (Hermetic)	D8	D	D	—	I	—	—	DA
		14-, 16-, 18- and 20-Lead Side Brazed (Hermetic)	D	D	D	YB QB XB	L	—	—	DD, DE, DN, DP
TSSOP Thin Shrink Small Outline		20-Lead Plastic TSSOP (0.173)	F		U	—		DL PW	—	UP, UG, UI
SSOP Shrink Small Outline		16-, 20-, 24- and 28-Lead Plastic SSOP (0.209)	G	MSA	RS		—	DB		AP, AG, AT
		16-, 20- and 24-Lead Plastic SSOP (Narrow 0.150)	GN							
		36- and 44-Lead Plastic SSOP (Wide 0.300)	GW	MSA	—	—		DB		AX
METAL CANS		8- or 10-Lead TO-5 Metal Can	H	H	H	H J K	G	—	T	TV, TW, VS
		3- or 4-Lead TO-39 Metal Can	H	H	H	H J K	G	—	T	TV, TW, VS
		2-, 3- or 4-Lead Standard TO-46 Metal Can or in Thermal Caps	H	H	H		—	—	T	—
		3-Lead TO-52 Metal Can	H							SR
CERDIP Ceramic Dual-In-Line		8-Lead Ceramic DIP (Hermetic)	J8	J J8	Q	Z	U	JG	Y	JA
		14-, 16-, 18-, 20- and 24-Lead Ceramic DIP (Narrow 0.300, Hermetic)	J	J J14 J16	D Q	Y Q X	L J	J	J	RD, RN, RE, RP
		28-Lead Ceramic DIP (Wide 0.600, Hermetic)	JW	—	Q	T	L			JG, JI
METAL CAN		2-Lead TO-3 Metal Can	K	K Steel	—	—	K	—	K	KQ
		4-Lead TO-3 Metal Can	K	K	—	—	—	KJ	K	KS
LCC		20-Pin Leadless Chip Carrier (Rectangular, Hermetic)	L	E	E	F	FN	FN FK	L	L
		20-Pin Leadless Chip Carrier (Square 0.350, Hermetic)	LS	E	E	F	FN	FN FK	L	L
Proprietary Device Prefixes			LT LTC	LF LP LH MF LM	AD	OP REF CMP	MC	TL	LX SG	MAX

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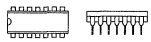
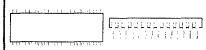
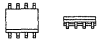
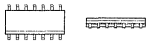
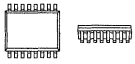
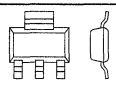
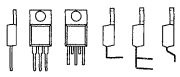
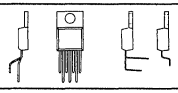
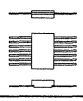
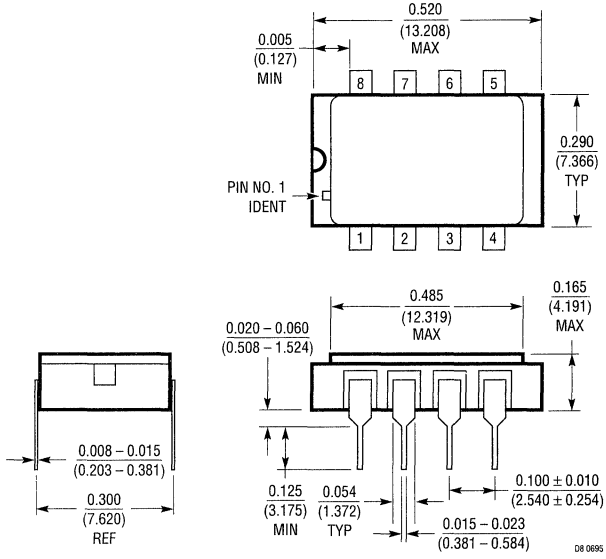
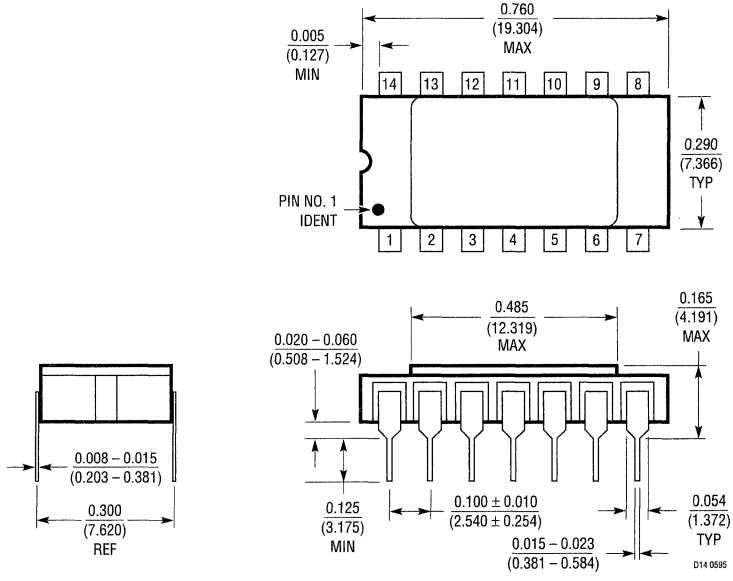
PACKAGE CROSS REFERENCE

	PACKAGE OUTLINE	DESCRIPTION	LTC	NSC	ADI/PMI		PMI	TI	LINFIN	MAXIM
DD PAK		3-Lead Plastic DD Pak	M	—	—	—	—	—	—	—
		5-Lead Plastic DD Pak	Q	—	—	—	—	—	—	—
		7-Lead Plastic DD Pak	R	—	—	—	—	—	—	—
PDIP Plastic Dual-In-Line		8-Lead PDIP, Plastic Dual-In-Line	N8	N N8	N	P	P1	P	M	P
		14-, 16-, 18-, 20- and 24-Lead PDIP, Plastic Dual-In-Line (Narrow 0.300)	N	N N14	N	P	P2	N NE	N	ND, NE, NN, NP, NG
		28-Lead PDIP, Plastic Dual-In-Line (Wide 0.600)	NW	—	N	P	P	N	—	PI
TO-3P (TO-247)		3-Lead Plastic TO-3P (Similar to TO-247)	P	—	—	—	—	—	—	K
SO Small Outline		8-Lead Plastic SO (Narrow 0.150)	S8	M	R	SO8	D	D	—	SA
		14- and 16-Lead Plastic SO (Narrow 0.150)	S	M	R	SO14 SO16	D	D	—	SD SE
		16-, 18-, 20-, 24- and 28-Lead Plastic SO (Wide 0.300)	SW	M	R	SO16 SO18 SO20 SO24 SO28	D	D	—	WE, WN, WP, WF WG, WI
		3-Lead Plastic SOT-223 Small Outline Transistor	ST	—	—	—	—	—	—	UR
TO-220		3- or 5-Lead Plastic TO-220	T T	T T	— —	— —	T —	KC KV	P P	C C
		7-Lead Plastic TO-220 (Formerly Y Package)	T7	—	—	—	—	—	—	C
FLATPAK		10-Lead Flatpak, Glass Sealed (Hermetic)	W	W	L	RC	F	U010	F	FB
		10- or 14-Lead Flatpak, Metal Sealed, Bottom Brazed (Hermetic)	WB	F	AH-148 LM	OH-148	—	WO10 WO14	—	M
TO-92		3-Lead, Plastic TO-92 Package	Z	Z	—	—	P	LP	—	ZR
Proprietary Device Prefixes			LT LTC	LF LP LH MF LM	AD	OP REF CMP	MC	TL	LX SG	MAX

D8 Package
8-Lead Side Brazed (Hermetic)
(LTC DWG # 05-08-1210)

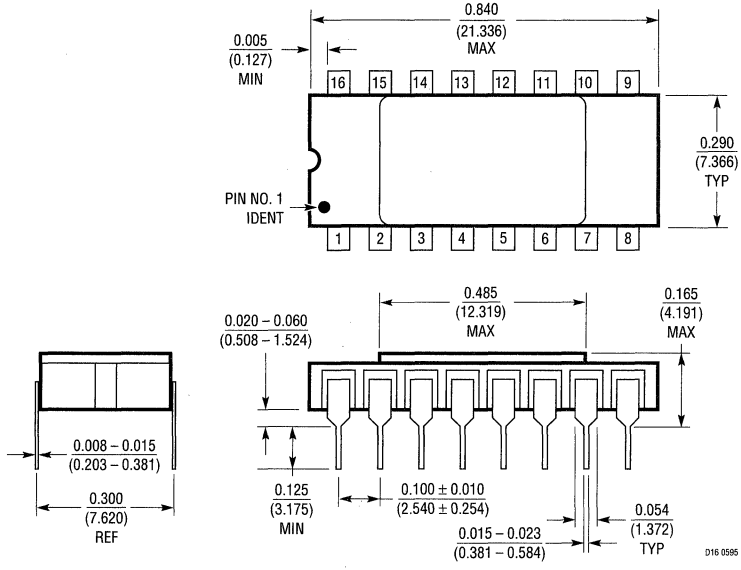


D Package
14-Lead Side Brazed (Hermetic)
(LTC DWG # 05-08-1210)

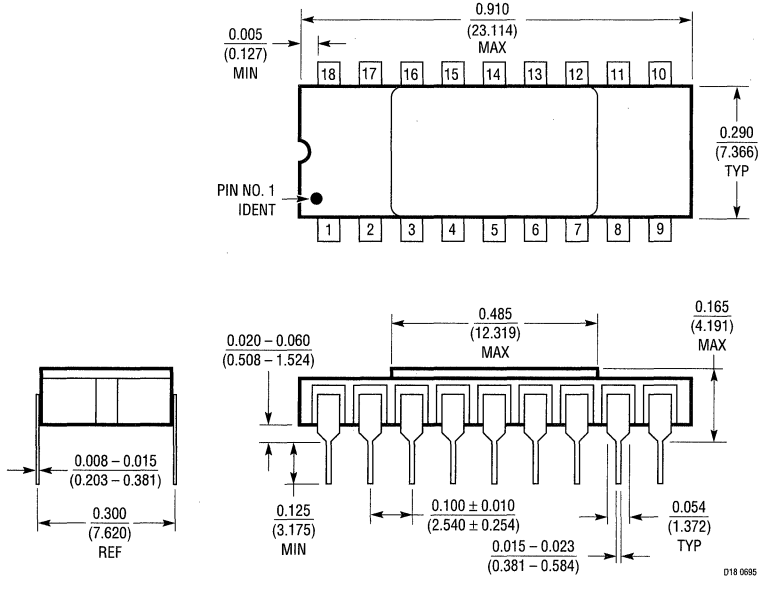


14

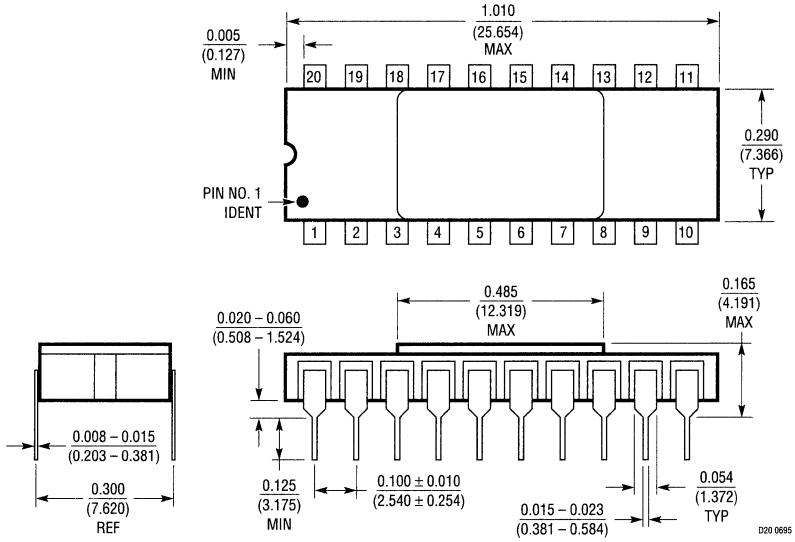
D Package
16-Lead Side Brazed (Hermetic)
(LTC DWG # 05-08-1210)



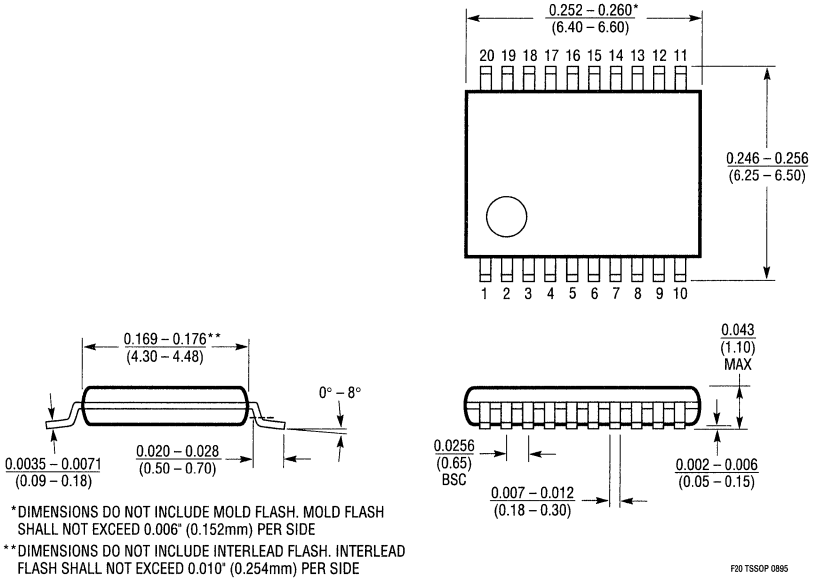
D Package
18-Lead Side Brazed (Hermetic)
(LTC DWG # 05-08-1210)



D Package
20-Lead Side Brazed (Hermetic)
(LTC DWG # 05-08-1210)



F Package
20-Lead Plastic TSSOP (0.173)
(LTC DWG # 05-08-1650)



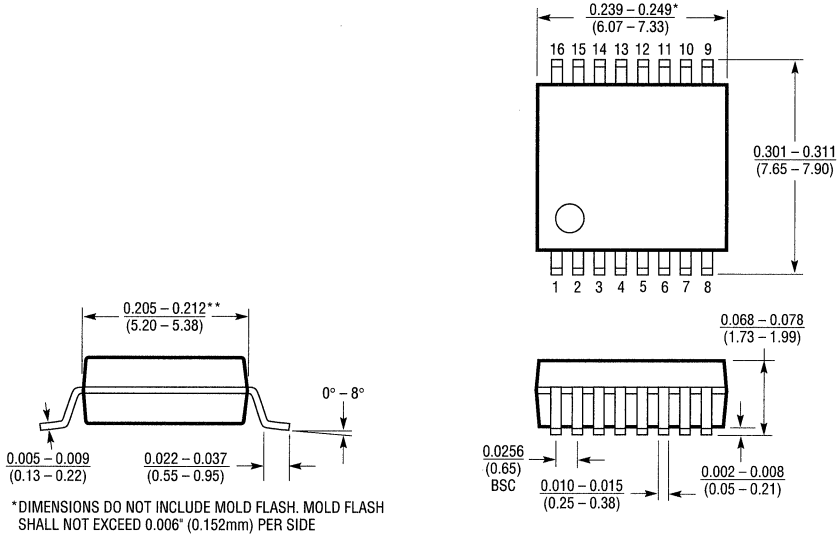
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

F20 TSSOP 0895

14

G Package
16-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)

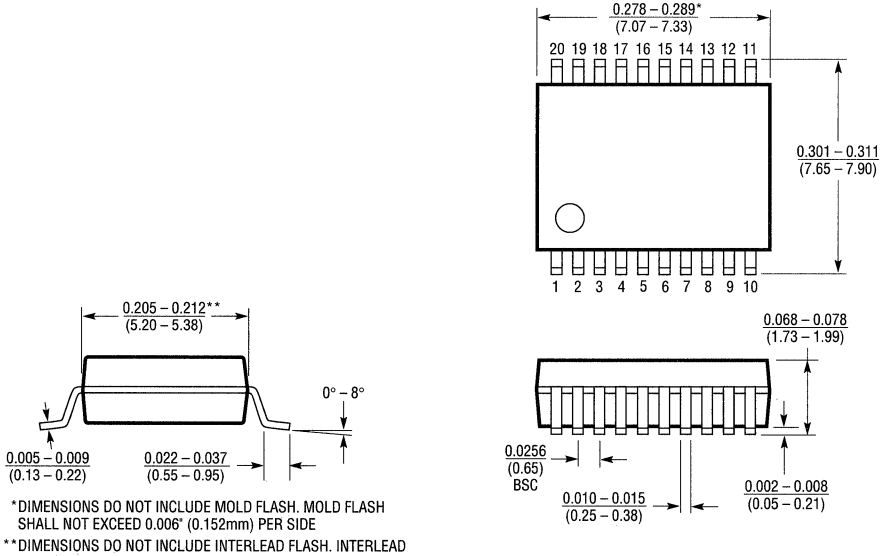


*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

G16 SSOP 0795

G Package
20-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)

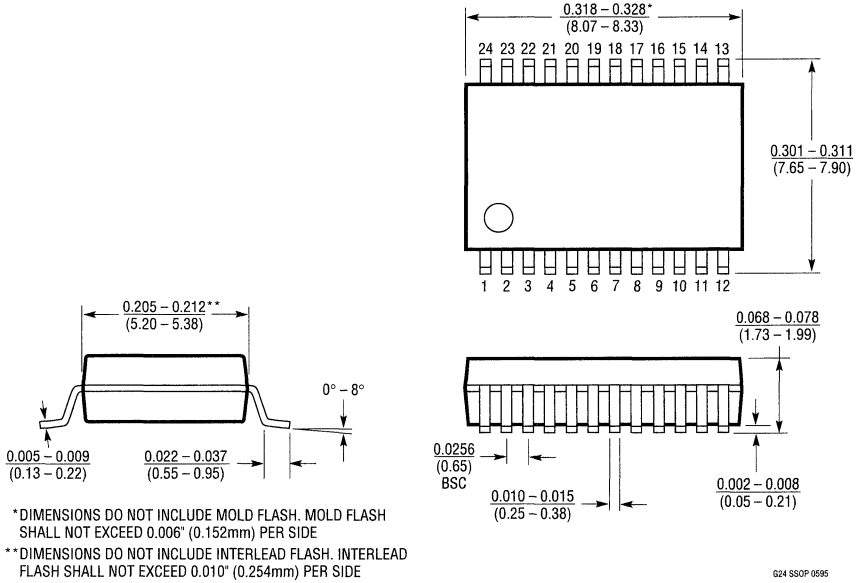


*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

G20 SSOP 0595

G Package
24-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)

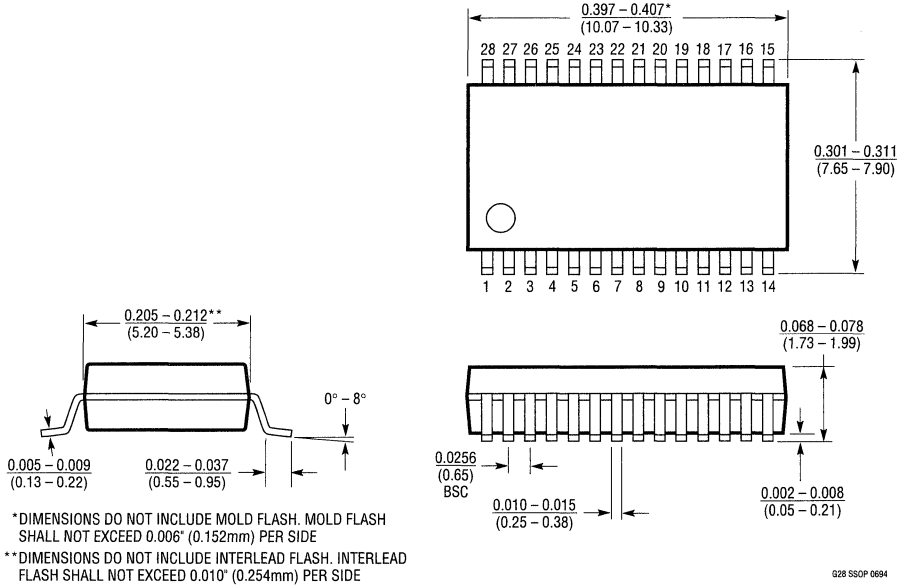


*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

G24 SSOP 0595

G Package
28-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



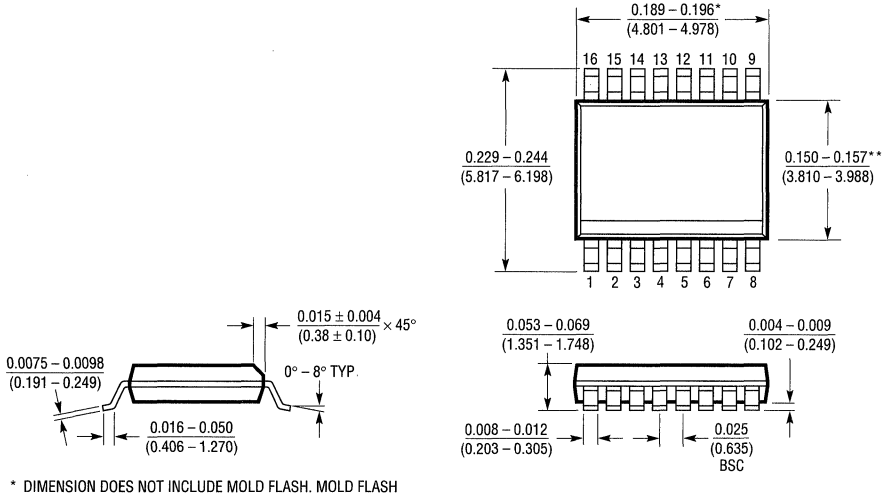
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

G28 SSOP 0694

14

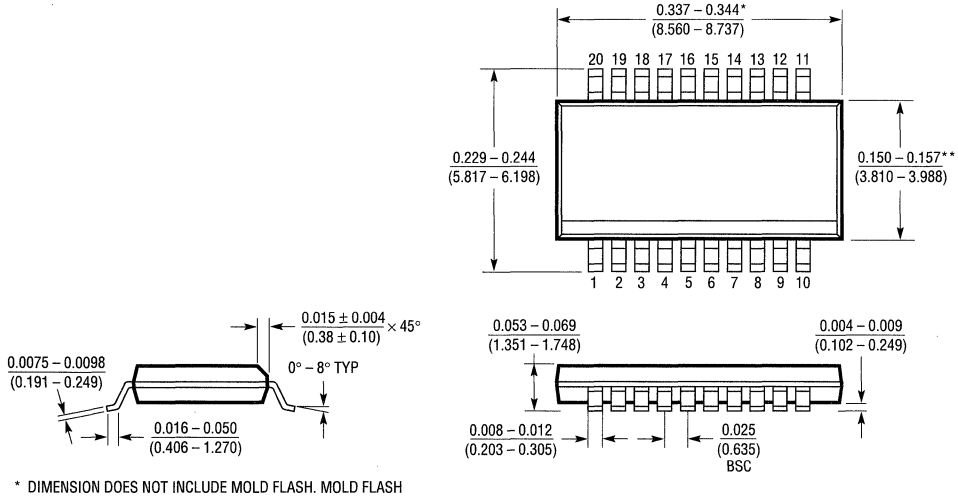
GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

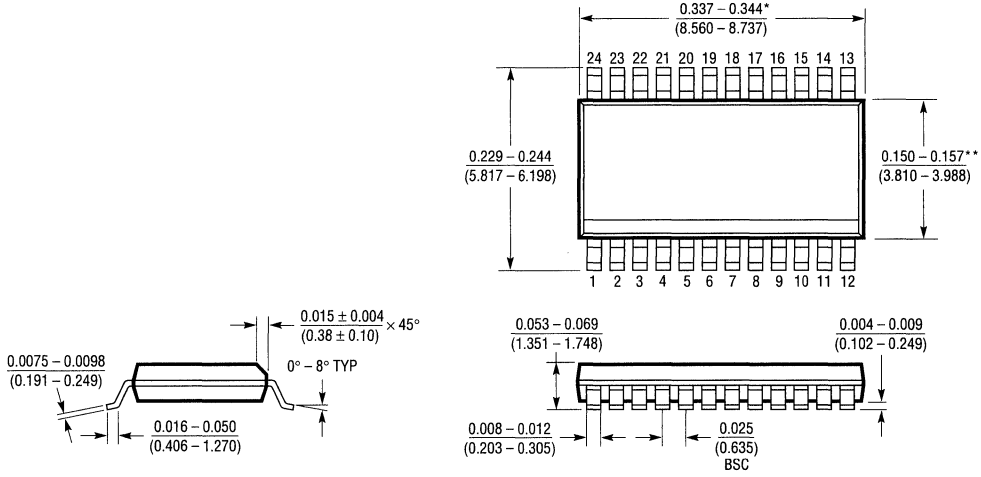
GN Package
20-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN Package
24-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)

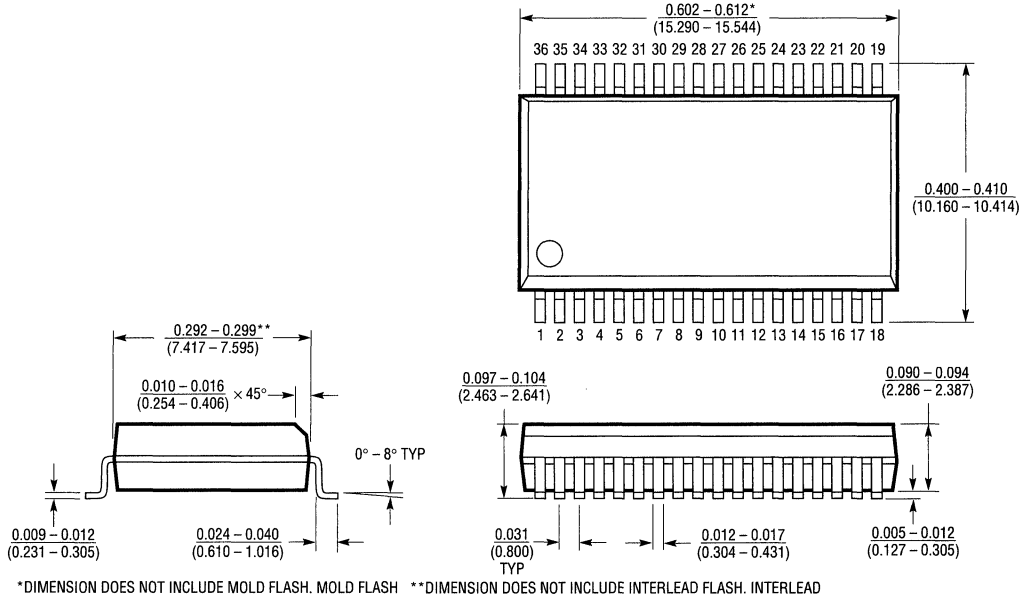


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN24 (SSOP) 0595

GW Package
36-Lead Plastic SSOP (Wide 0.300)
(LTC DWG # 05-08-1642)



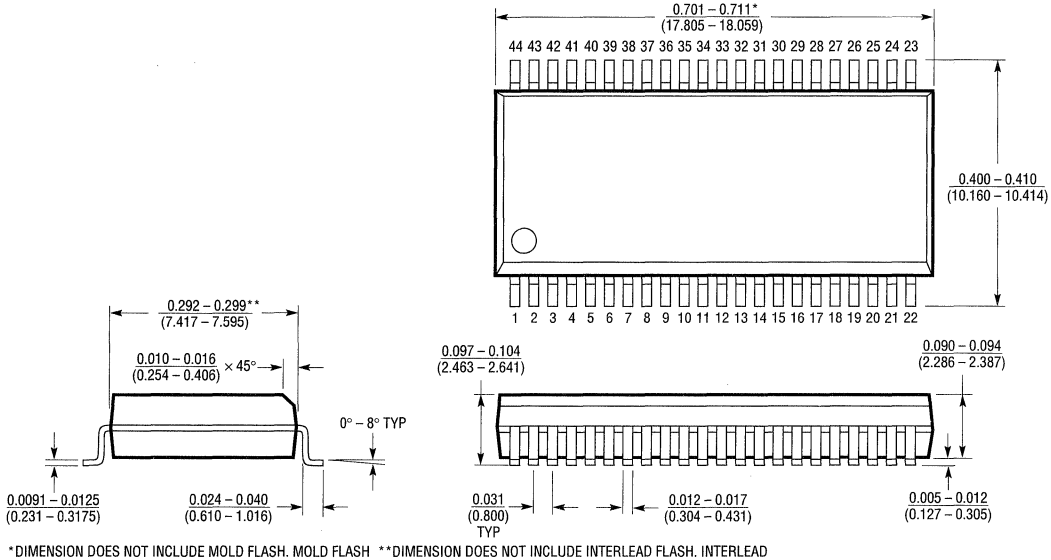
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GW36 SSOP 0795

14

GW Package
44-Lead Plastic SSOP (Wide 0.300)
(LTC DWG # 05-08-1642)

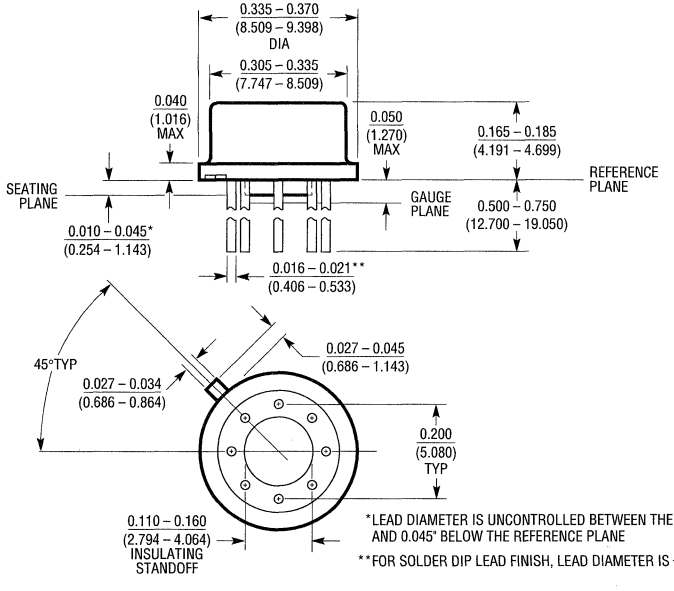


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

G44 SSOP 0895

H Package
8-Lead TO-5 Metal Can (0.200 PCD)
(LTC DWG # 05-08-1320)

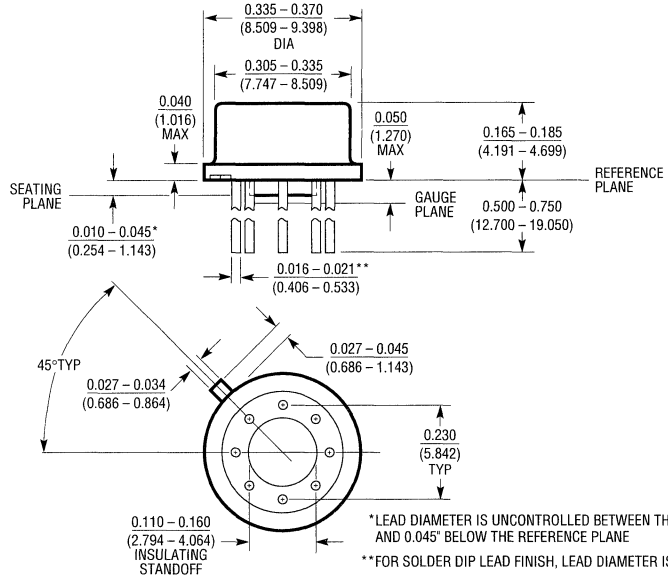


*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

H8(TO-5) 0.200 PCD 0595

H Package
8-Lead TO-5 Metal Can (0.230 PCD)
(LTC DWG # 05-08-1321)

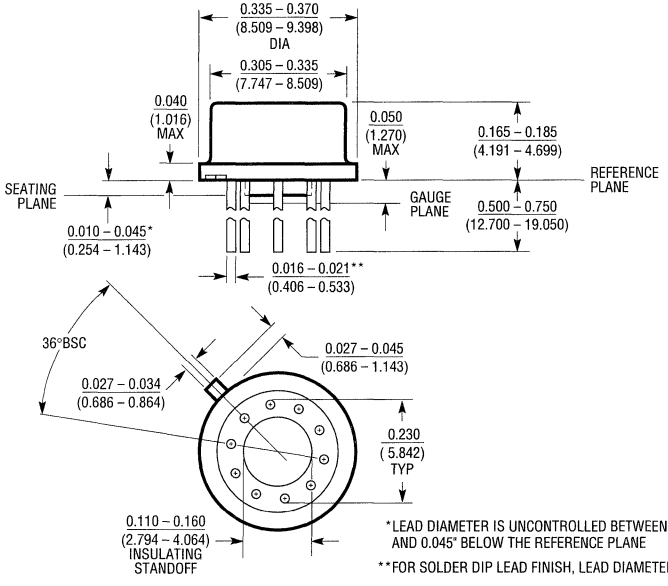


*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

H8 (TO-5) 0.230 PCD 0595

H Package
10-Lead TO-5 Metal Can
(LTC DWG # 05-08-1322)



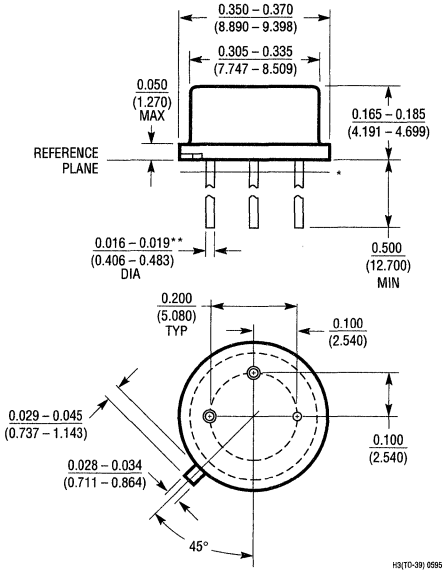
*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS 0.016 – 0.024 (0.406 – 0.610)

H10(TO-5) 0595

14

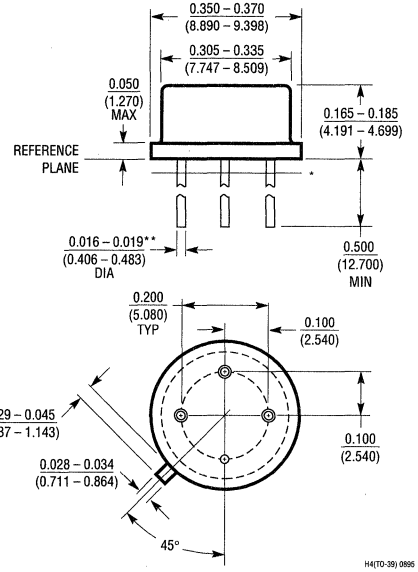
H Package
3-Lead TO-39 Metal Can
(LTC DWG # 05-08-1330)



*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

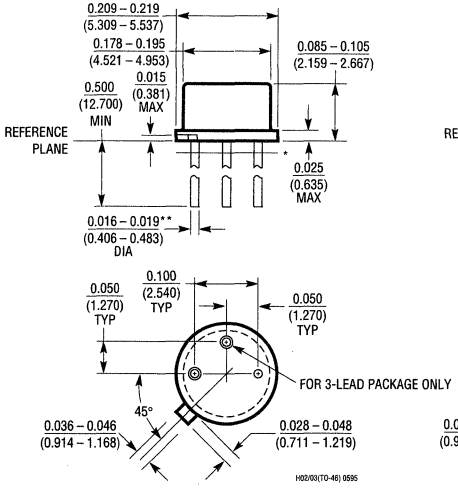
H Package
4-Lead TO-39 Metal Can
(LTC DWG # 05-08-1331)



*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

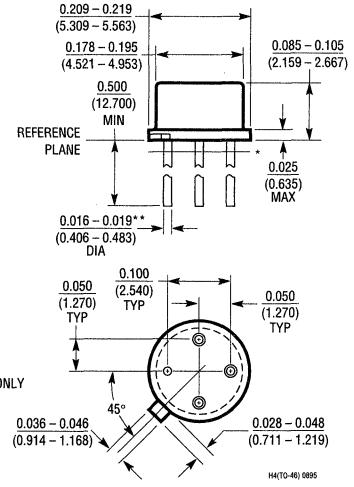
H Package
2-Lead and 3-Lead TO-46 Metal Can
(LTC DWG # 05-08-1340)



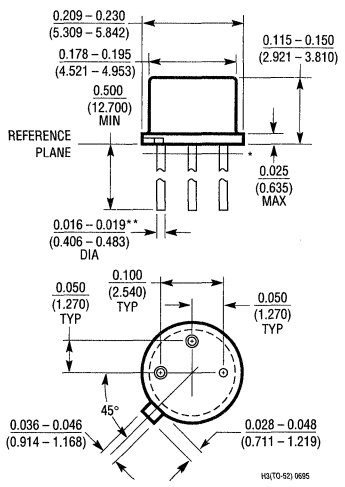
*LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND 0.045" BELOW THE REFERENCE PLANE

**FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS $\frac{0.016 - 0.024}{(0.406 - 0.610)}$

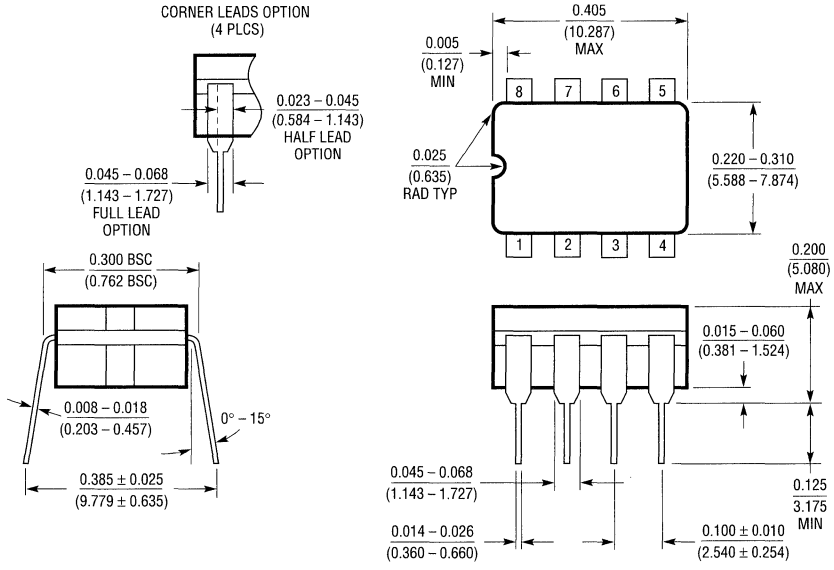
H Package
4-Lead TO-46 Metal Can
(LTC DWG # 05-08-1341)



H Package
3-Lead TO-52 Metal Can
(LTC DWG # 05-08-1350)



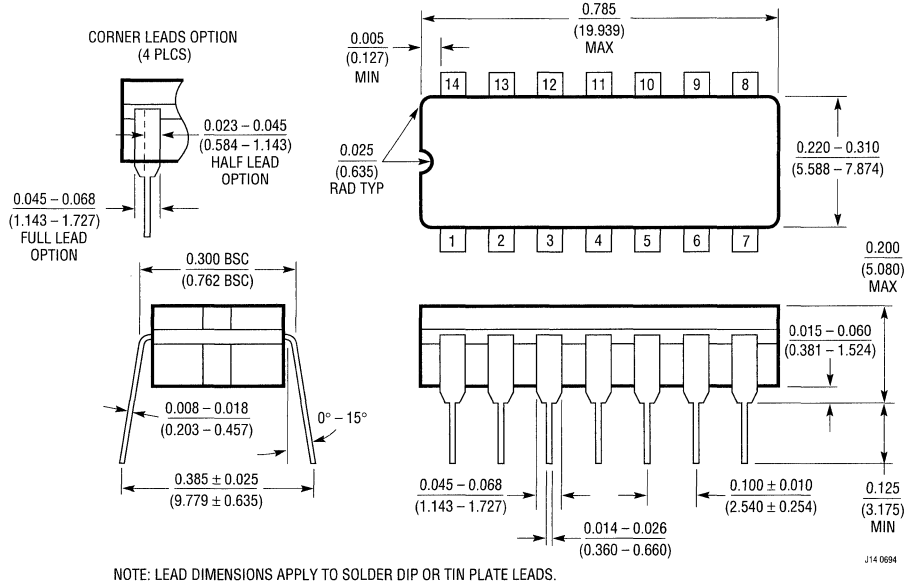
J8 Package
8-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J8 0694

J Package
14-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)

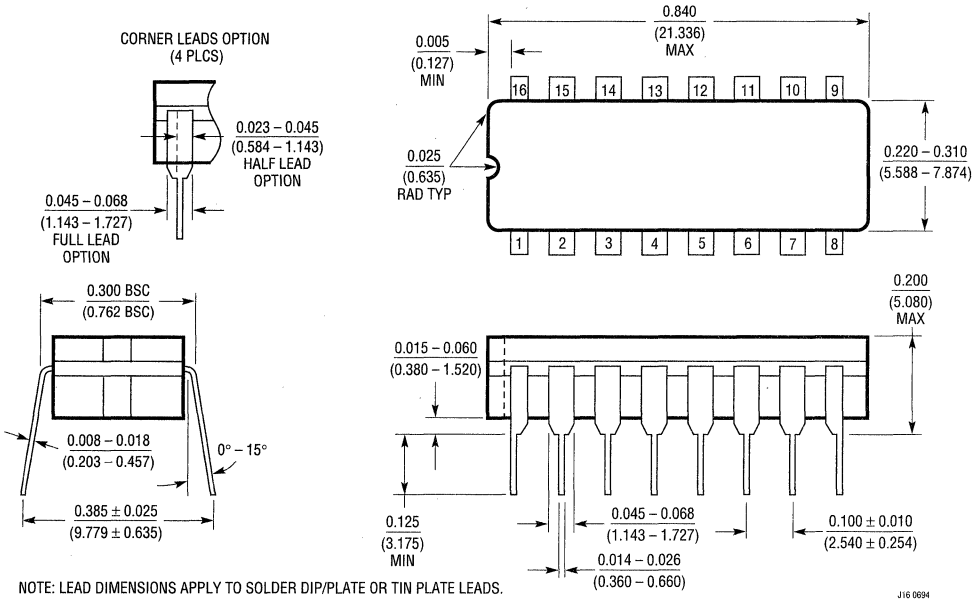


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.

J14 0694

14

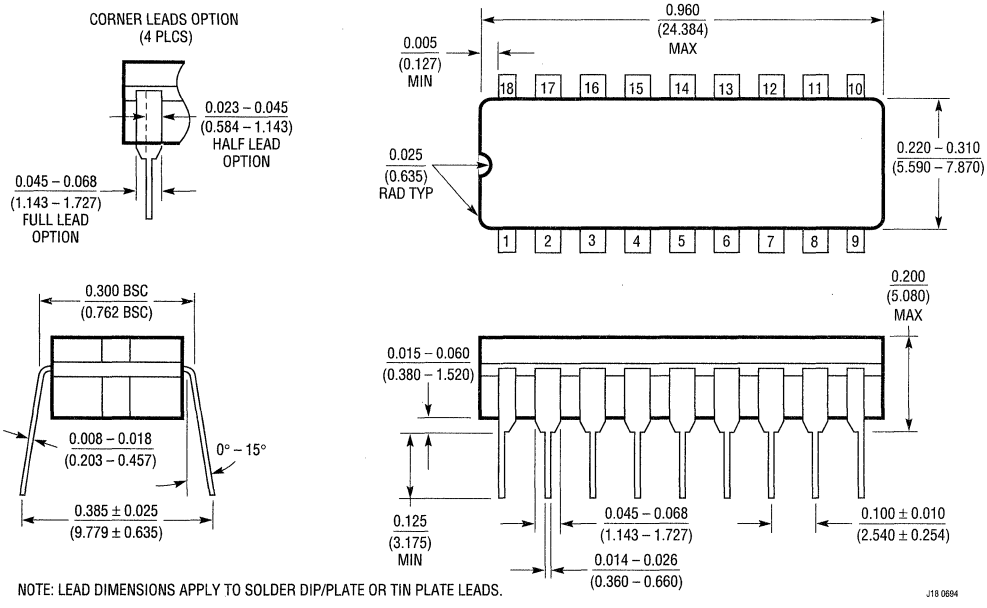
J Package
16-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J16 0694

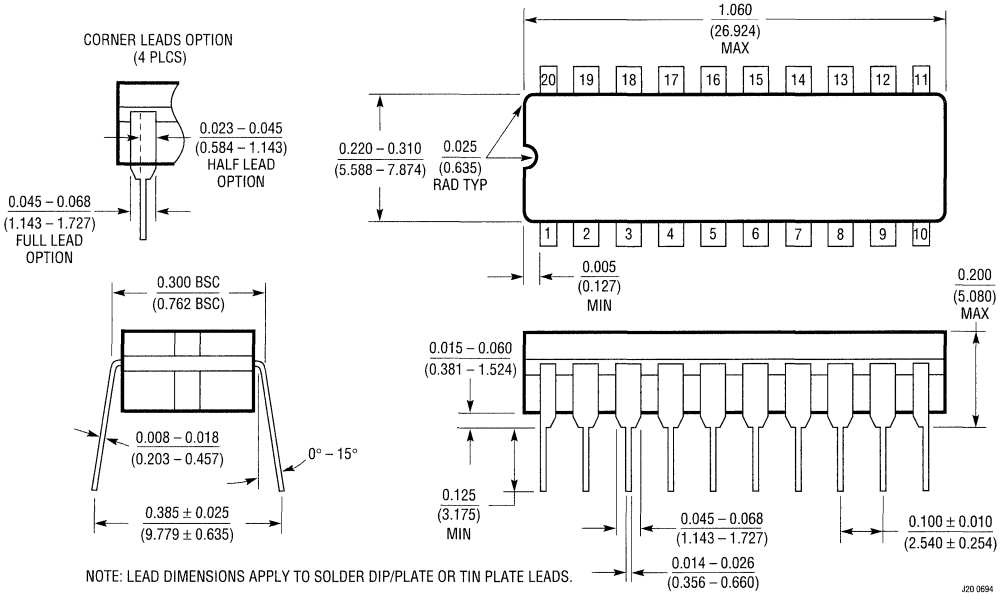
J Package
18-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J18 0694

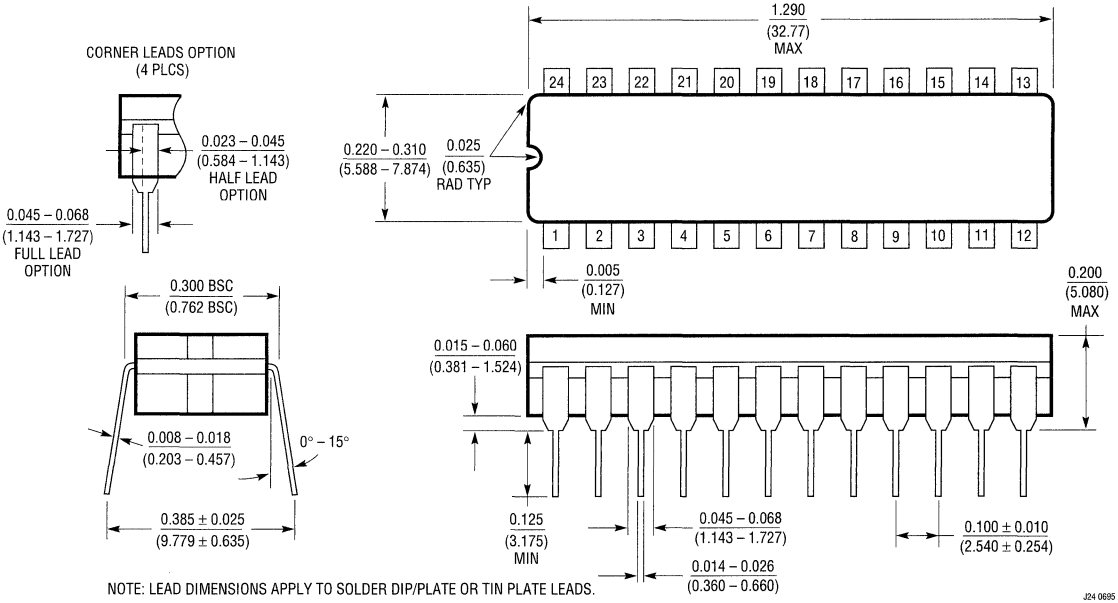
J Package
20-Lead CERDIP (Narrow 0.300, Hermetic)
(LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J20 0694

J Package
24-Lead CERDIP (Narrow 0.300, Hermetic)
(DWG # 05-08-1110)

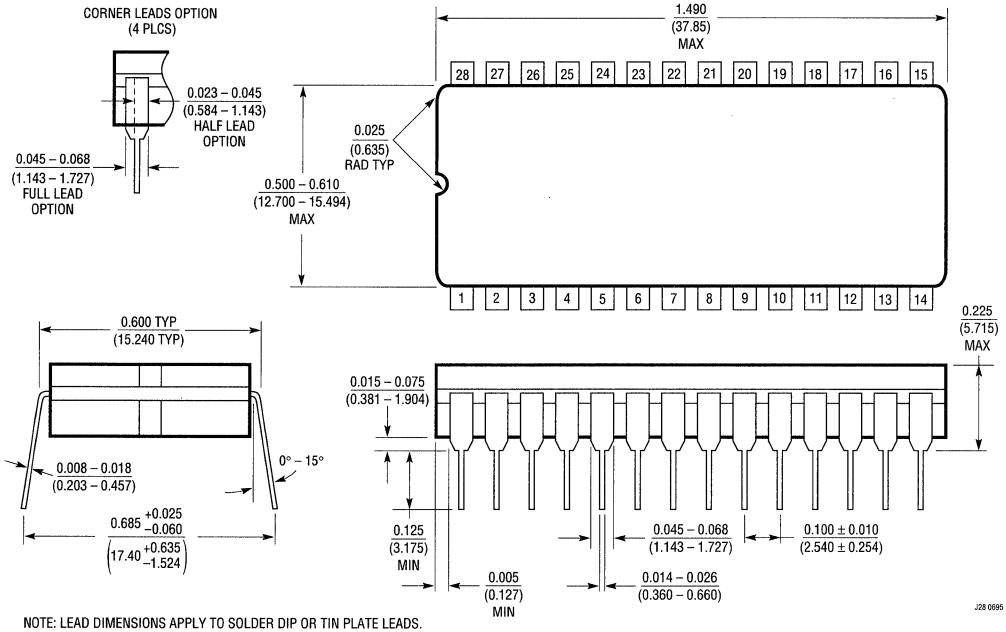


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS.

J24 0695

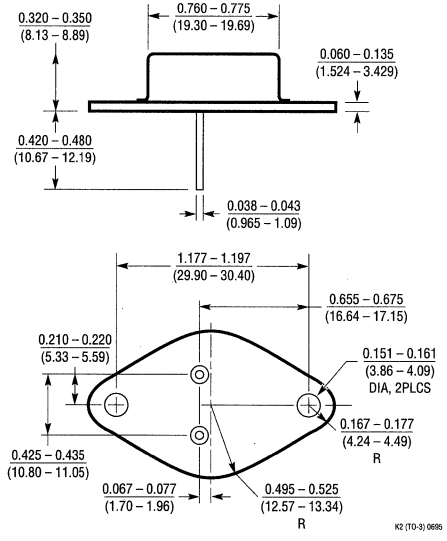
14

JW Package
28-Lead CERDIP (Wide 0.600, Hermetic)
(LTC DWG # 05-08-1120)

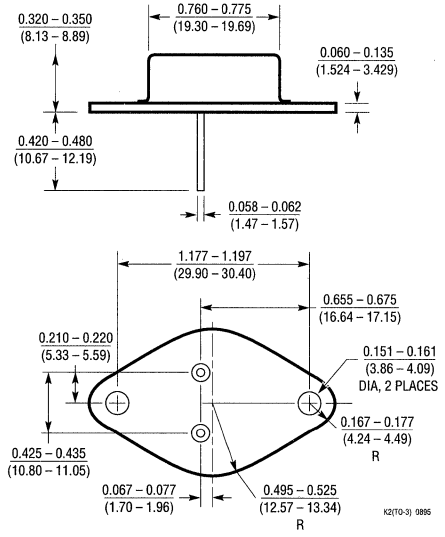


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP OR TIN PLATE LEADS.

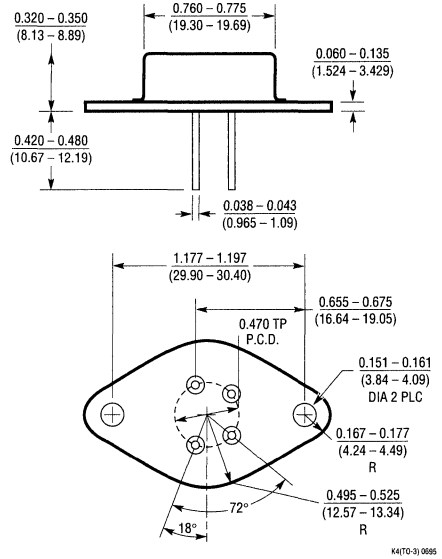
K Package
2-Lead TO-3 Metal Can
(LTC DWG # 05-08-1310)



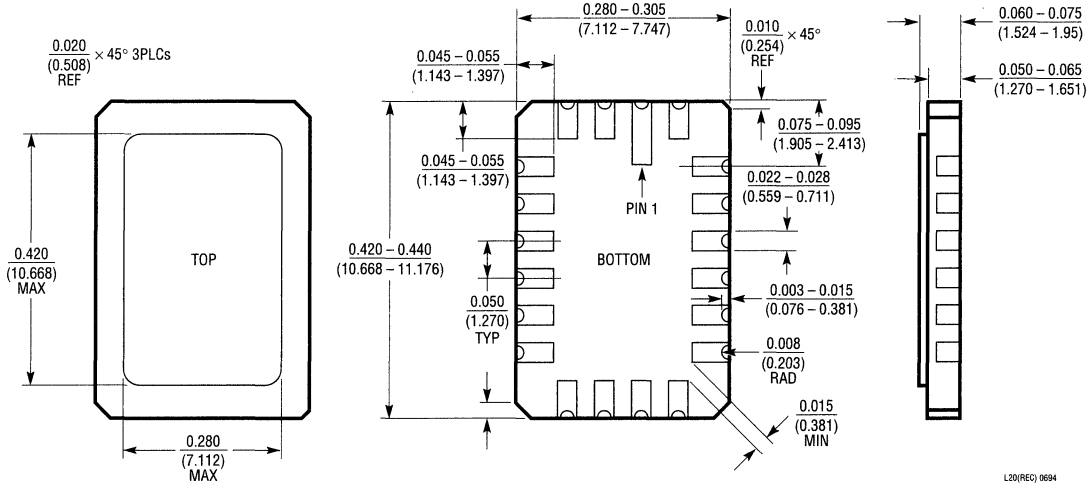
K Package
2-Lead TO-3 Metal Can
(60mil Diameter Leads)
(LTC DWG # 05-08-1312)



K Package
4-Lead TO-3 Metal Can
(LTC DWG # 05-08-1311)

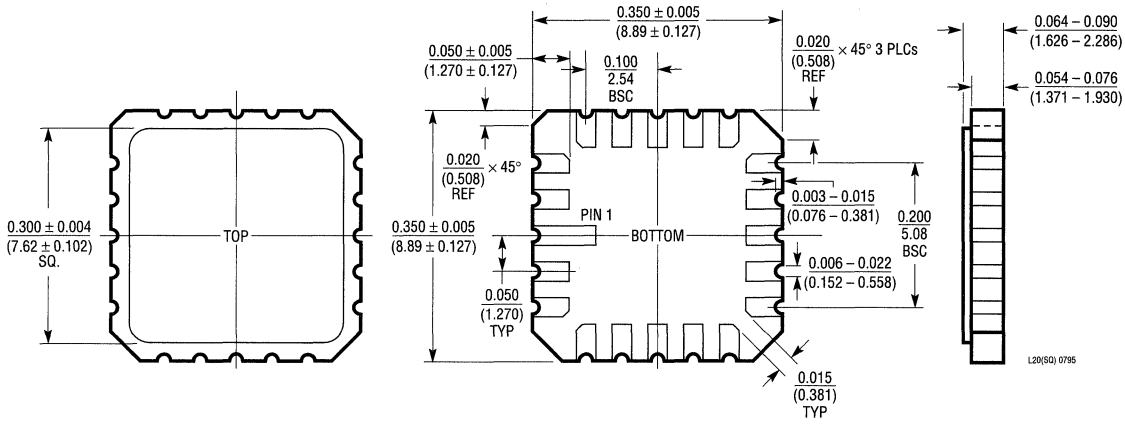


L Package
20-Pin Leadless Chip Carrier (Rectangular, Hermetic)
(LTC DWG # 05-08-1250)

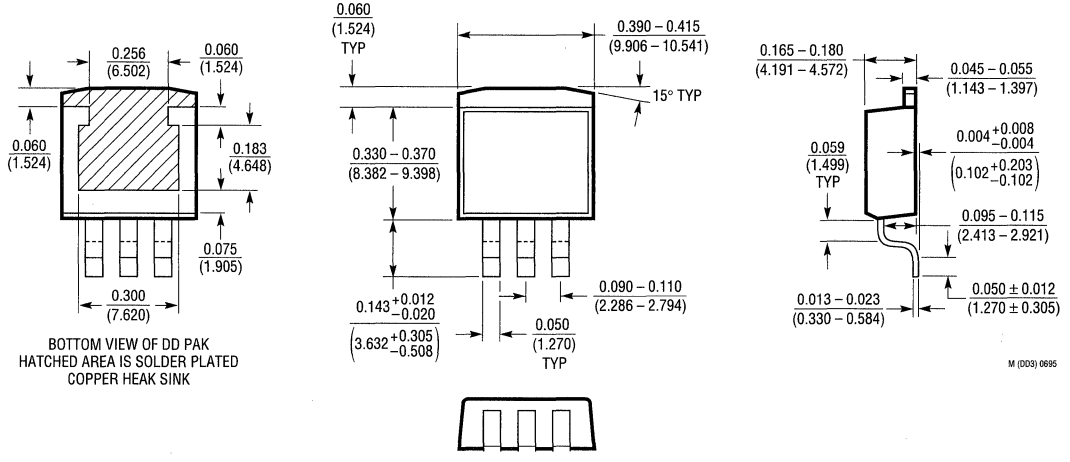


14

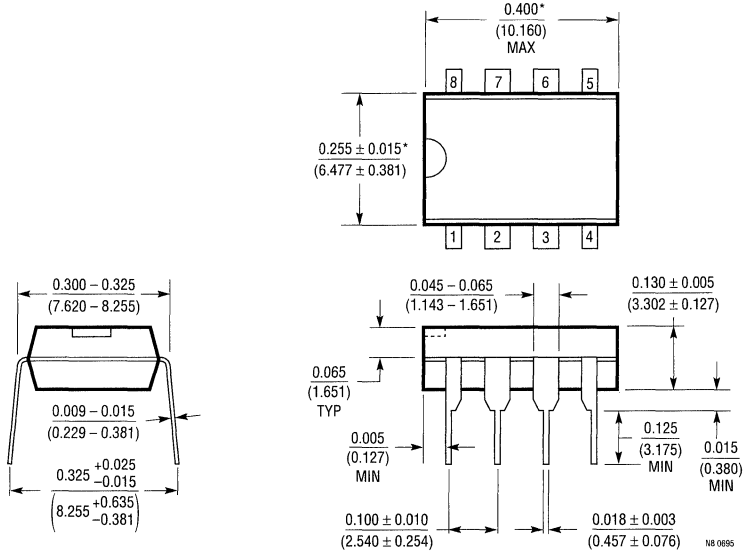
LS Package
20-Pin Leadless Chip Carrier (Square 0.350, Hermetic)
(LTC DWG # 05-08-1260)



M Package
3-Lead Plastic DD Pak
(LTC DWG # 05-08-1460)

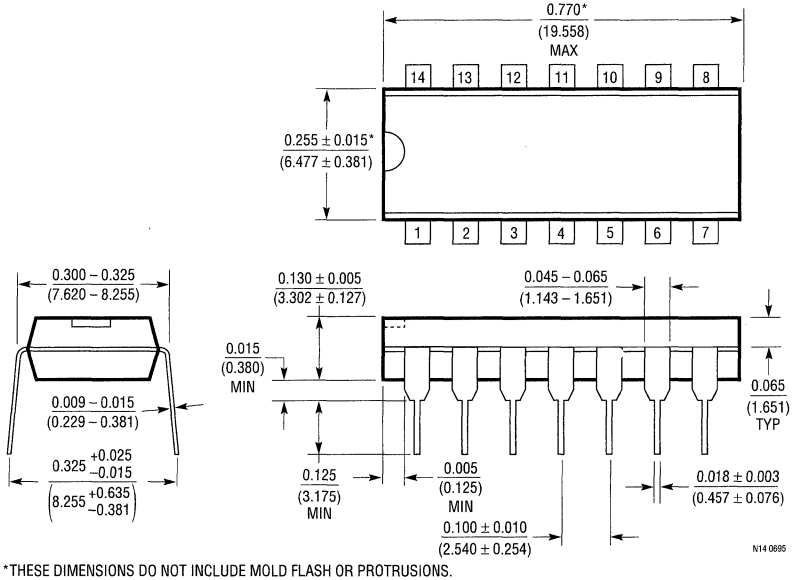


N8 Package
8-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

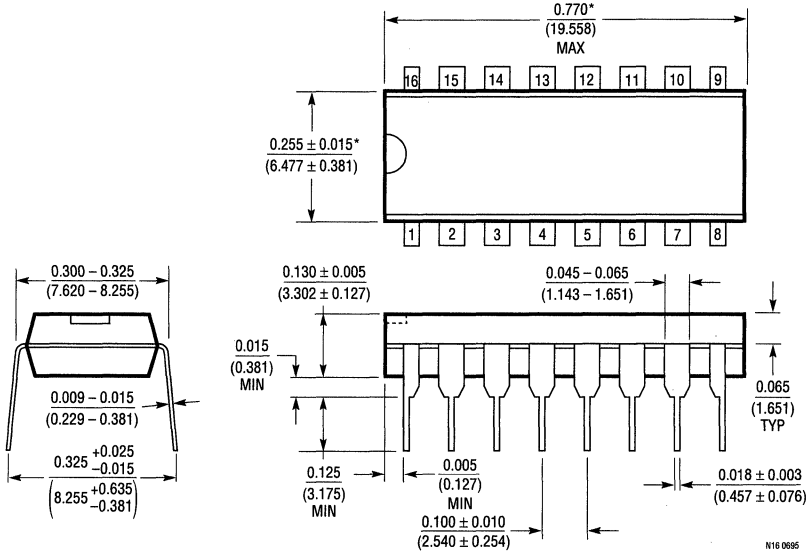
N Package
14-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

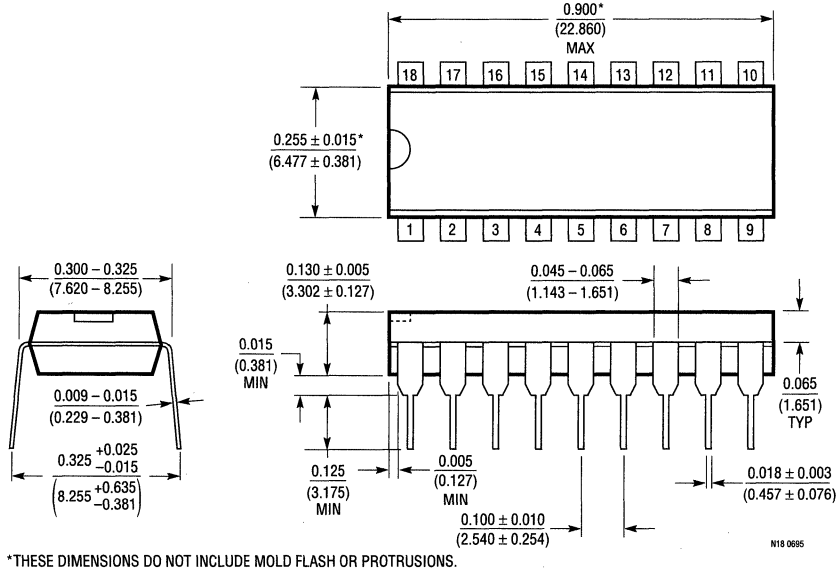
14

N Package
16-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



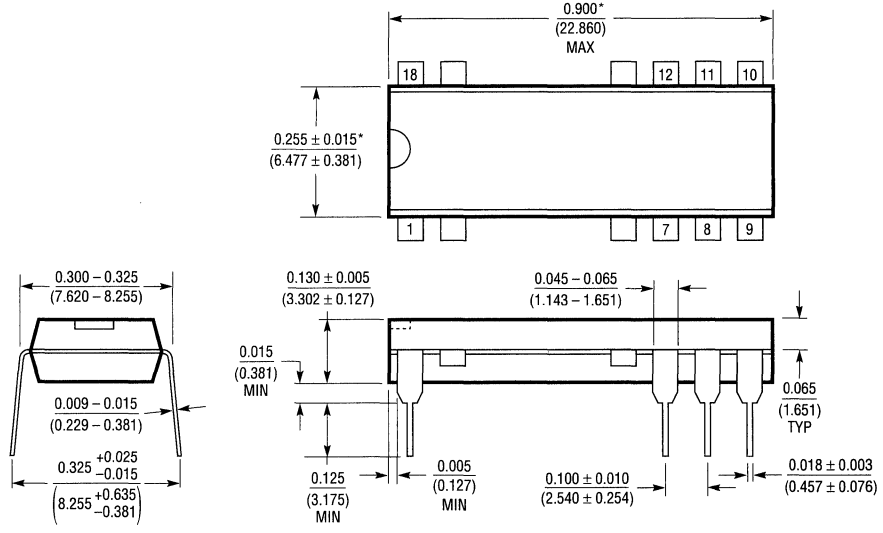
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N Package
18-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

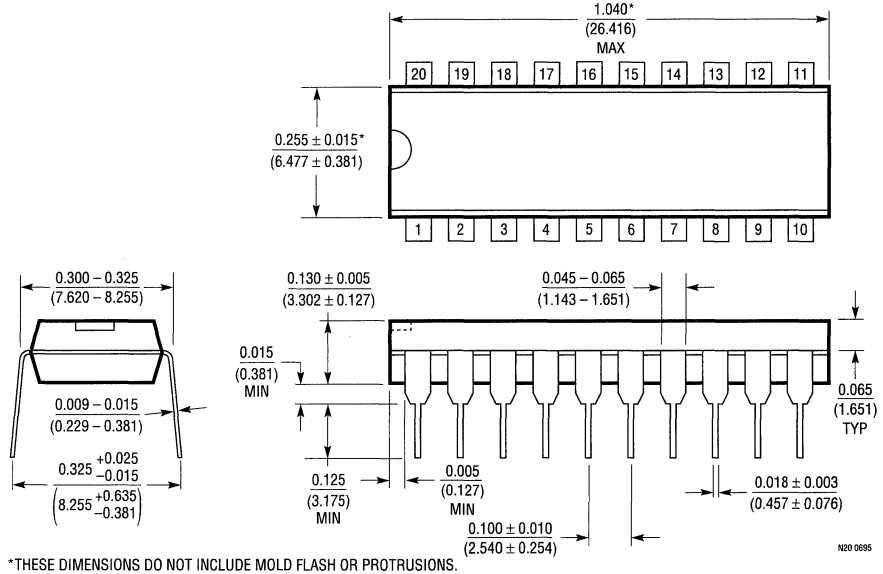
N Package
18-Lead PDIP Isolation Barrier (Narrow 0.300)
(LTC DWG # 05-08-1590)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N18 0695

N Package
20-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

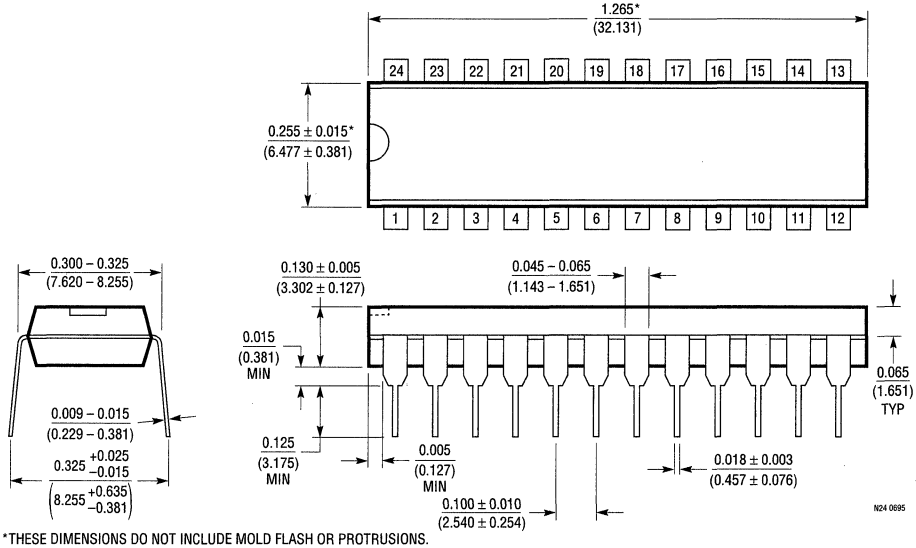


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N20 0695

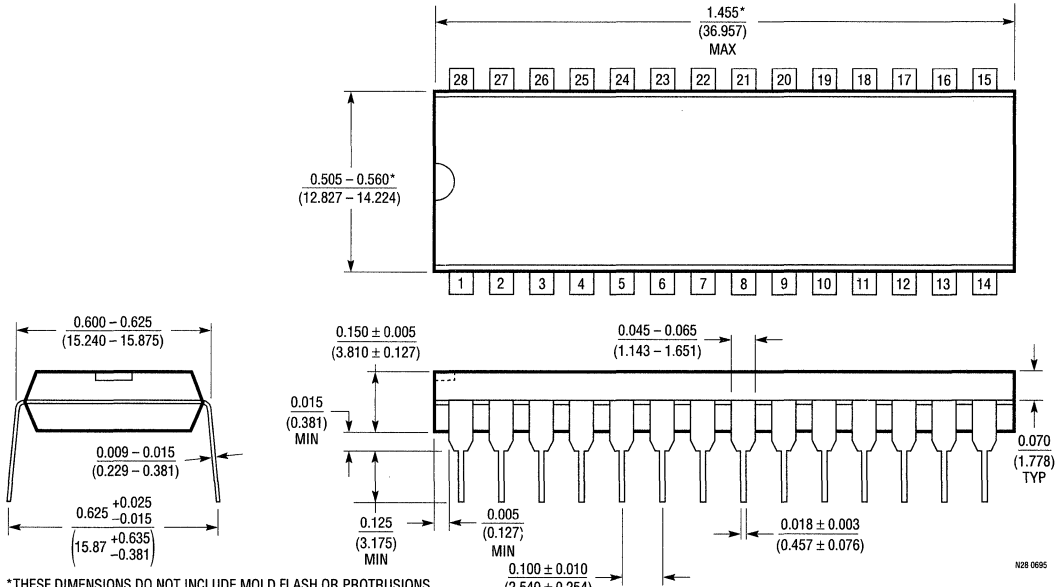
14

N Package
24-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



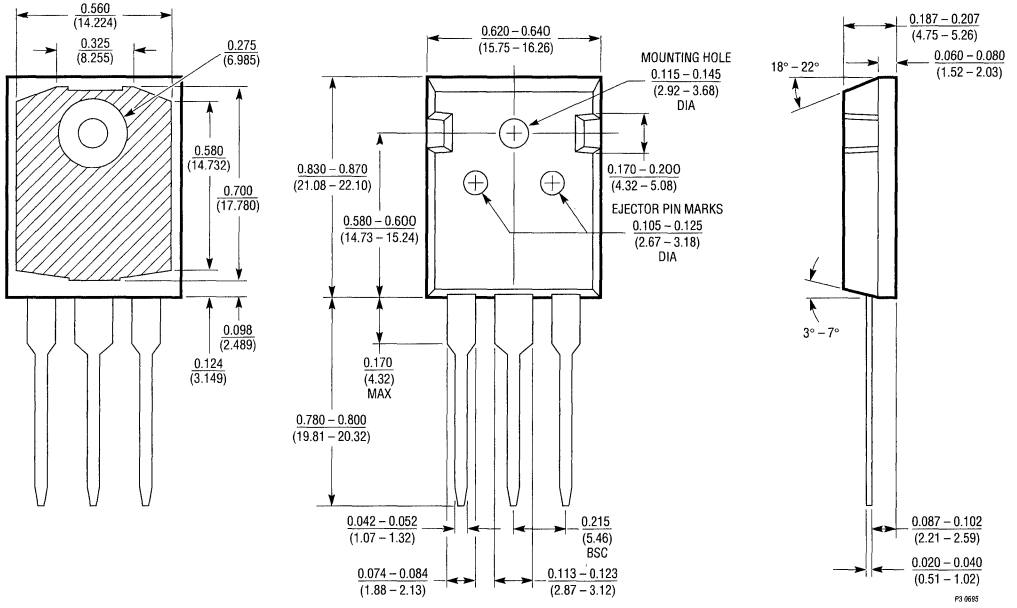
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

NW Package
28-Lead PDIP (Wide 0.600)
(LTC DWG # 05-08-1520)

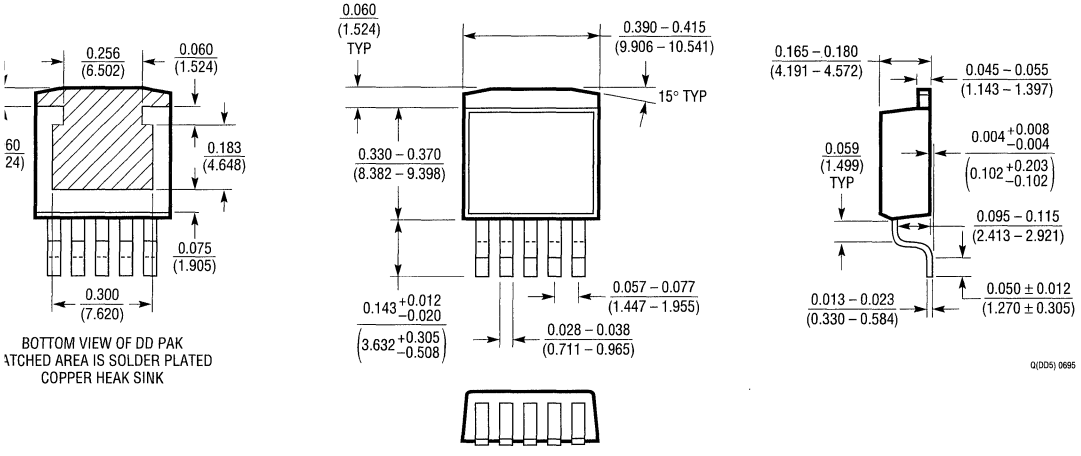


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

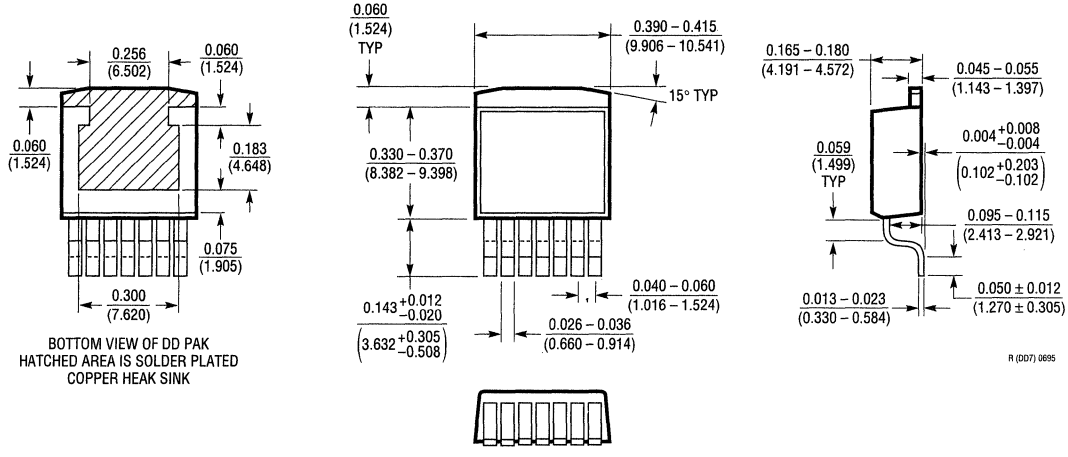
P Package
3-Lead Plastic TO-3P (Similar to TO-247)
(LTC DWG # 05-08-1450)



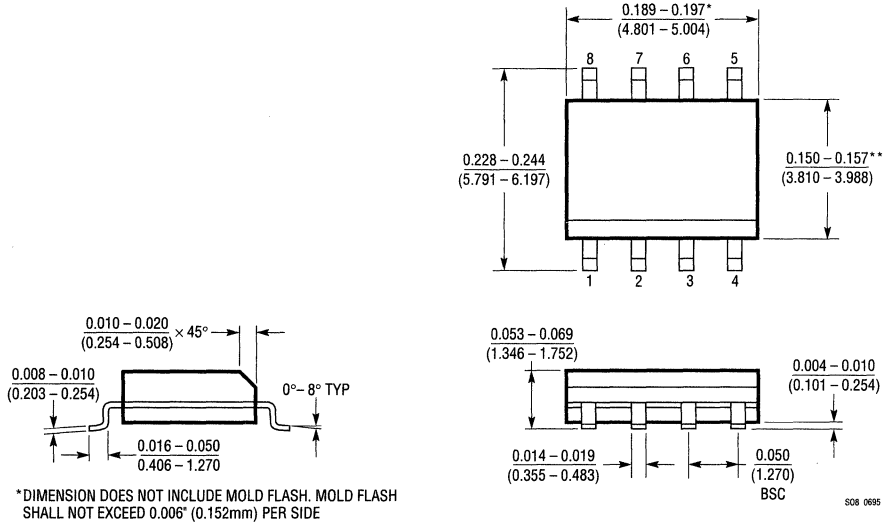
Q Package
5-Lead Plastic DD Pak
(LTC DWG # 05-08-1461)



R Package
7-Lead Plastic DD Pak
(LTC DWG # 05-08-1462)



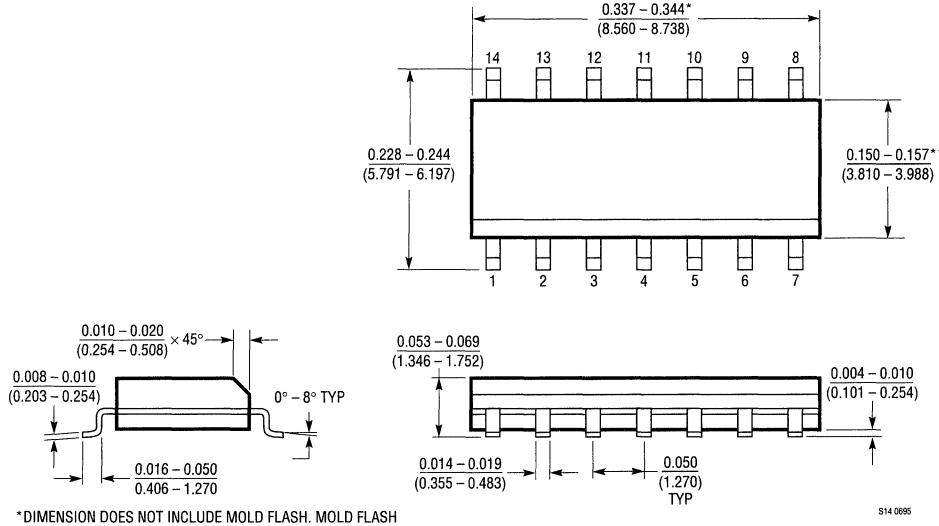
S8 Package
8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

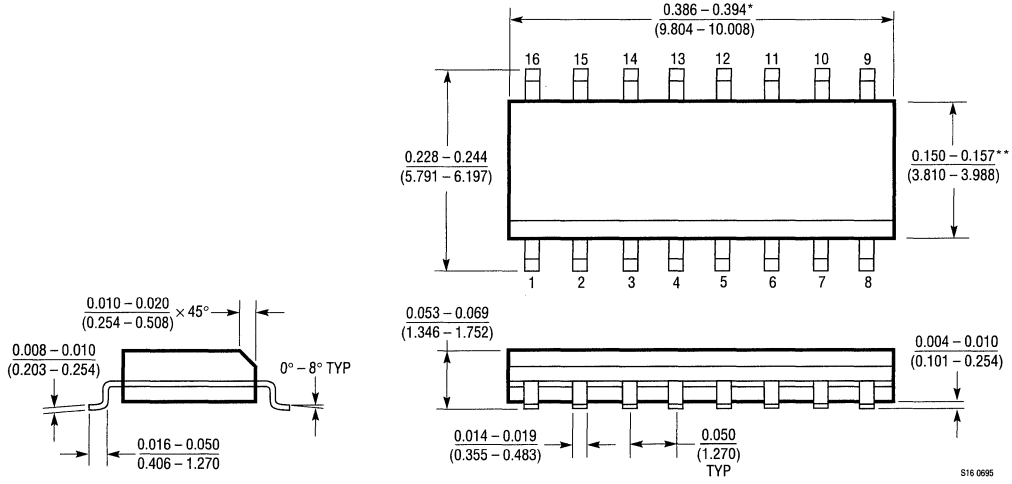
S Package
14-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

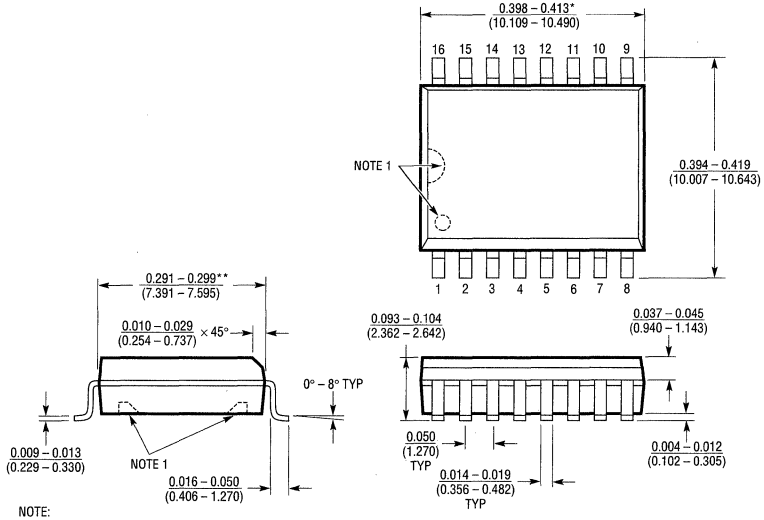
S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SW Package
16-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



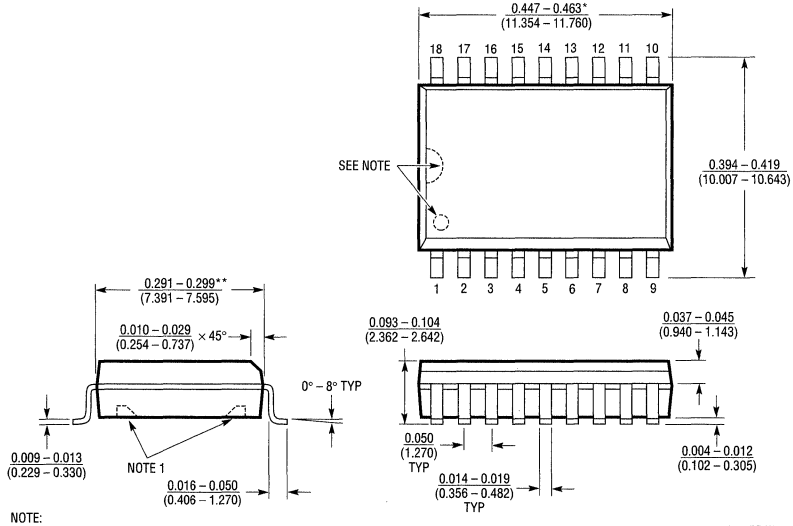
NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

S16 (WIDE) 0695

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SW Package
18-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



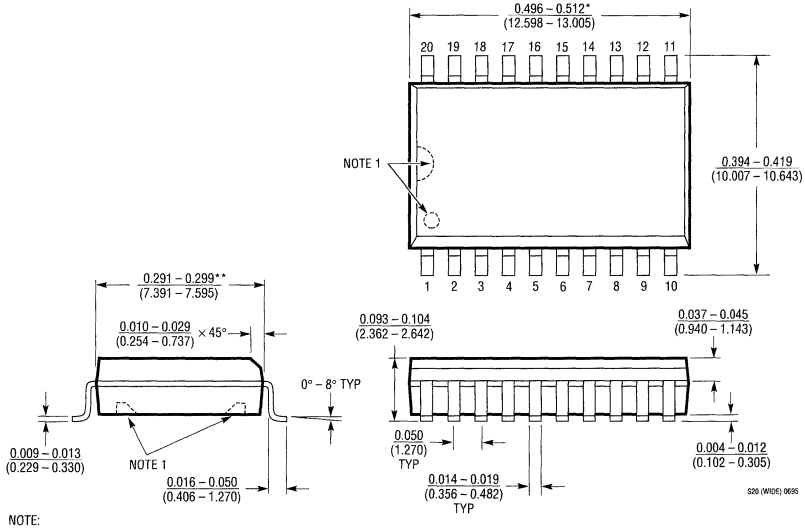
NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

S16 (WIDE) 0695

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SW Package
20-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)

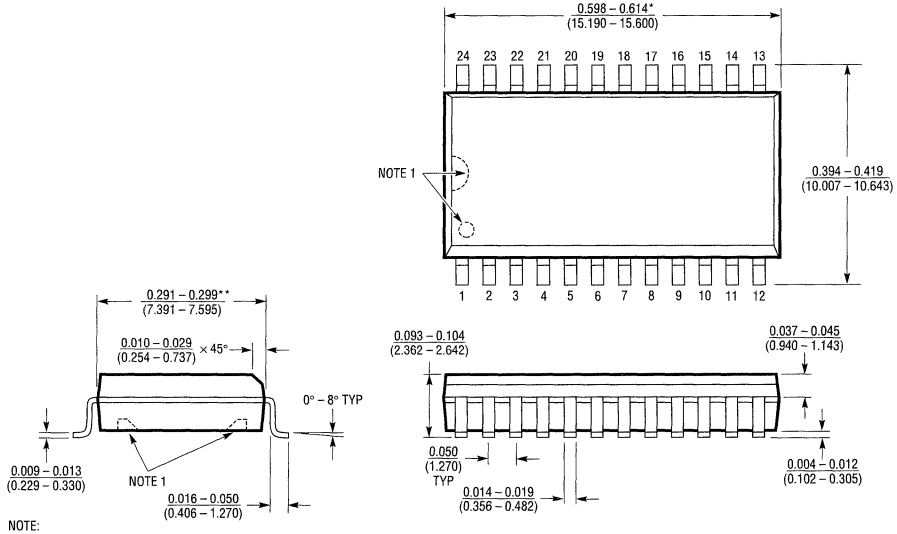


NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SW Package
24-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)

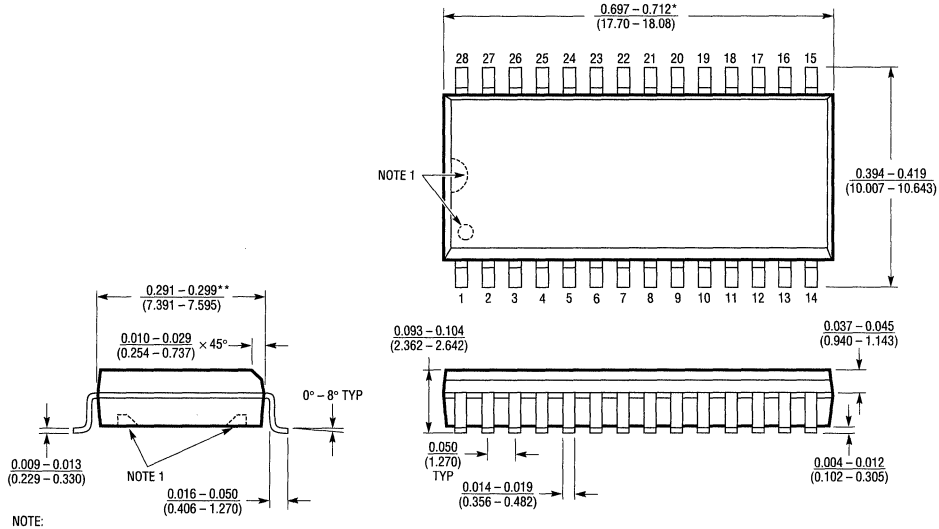


NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS
THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SW Package
28-Lead Plastic Small Outline (Wide 0.300)
(LTC DWG # 05-08-1620)



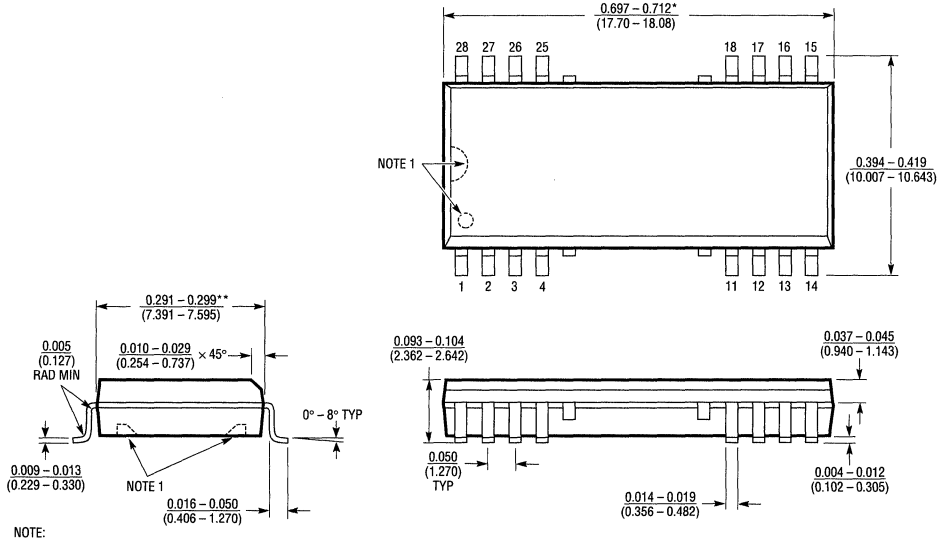
NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS
   THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S28 (WIDE) 0695

SW Package
28-Lead Plastic Small Outline Isolation Barrier (Wide 0.300)
(LTC DWG # 05-08-1690)



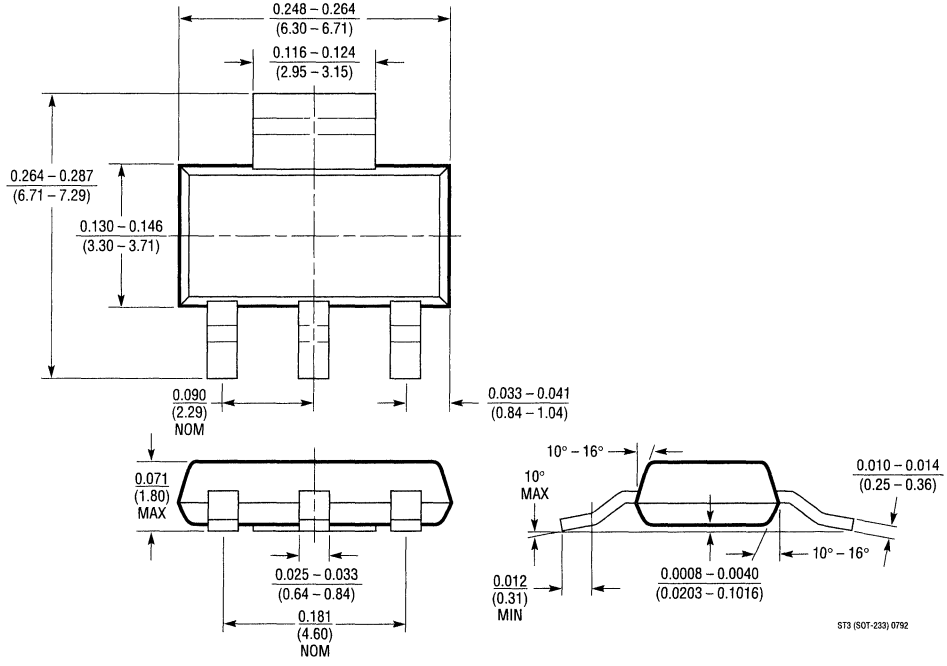
NOTE:
1. PIN 1 IDENT, NOTCH ON TOP AND CAVITIES ON THE BOTTOM OF PACKAGES ARE THE MANUFACTURING OPTIONS
   THE PART MAY BE SUPPLIED WITH OR WITHOUT ANY OF THE OPTIONS.

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

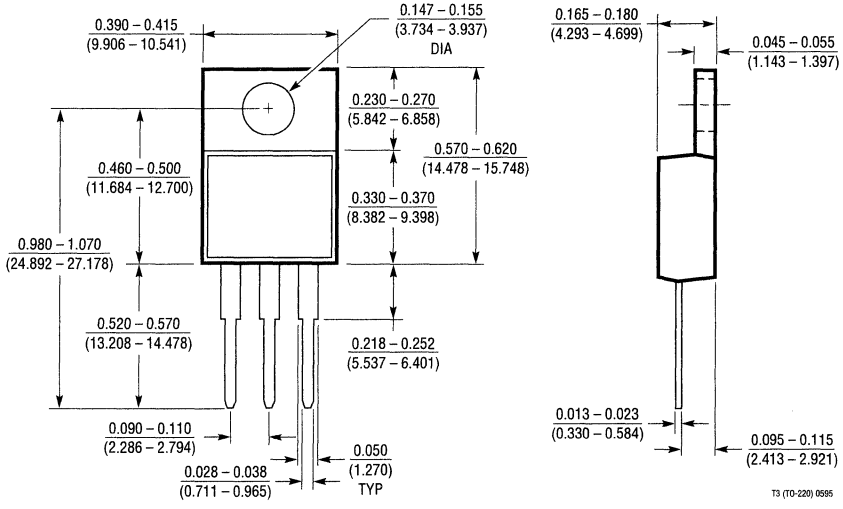
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SW28 (ISO) 0695

ST Package
3-Lead Plastic SOT-223
(LTC DWG # 05-08-1630)

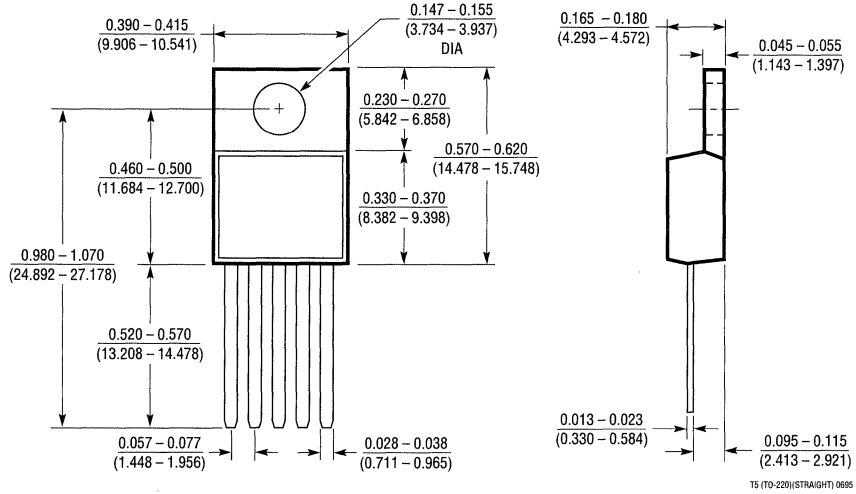


T Package
3-Lead Plastic TO-220
(LTC DWG # 05-08-1420)



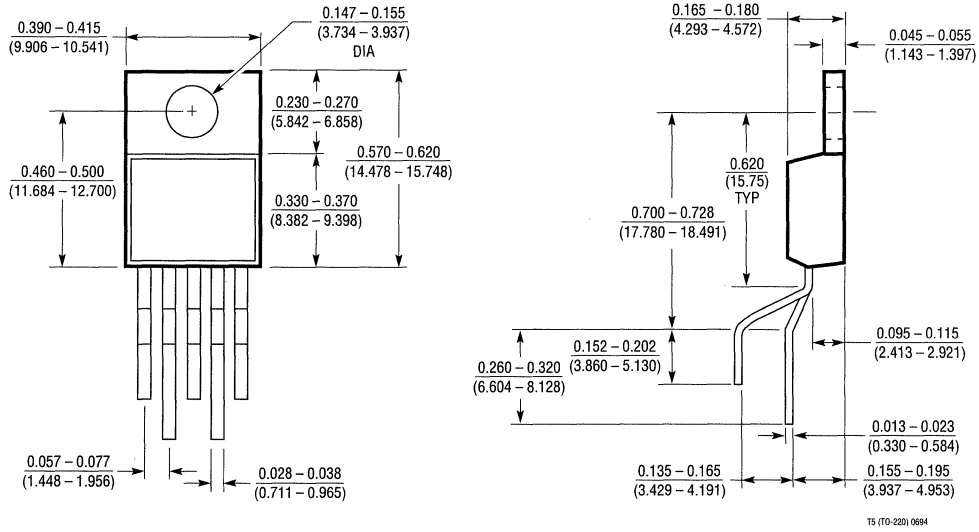
For Lead Bend Options See Page 14-54

T Package
5-Lead Plastic TO-220 (Straight Lead)
(Nonstandard Flow 06)
(LTC DWG # 05-08-1421)



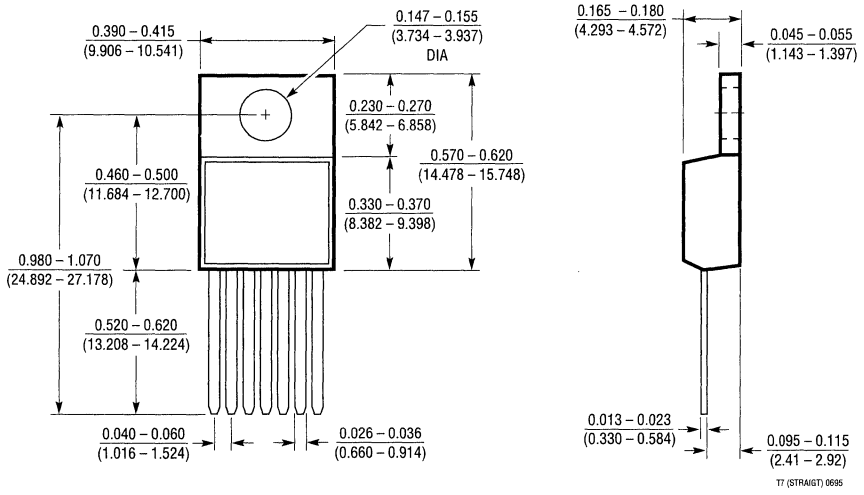
For Lead Bend Options See Page 14-54

T Package
5-Lead Plastic TO-220 (Standard)
(LTC DWG # 05-08-1421)



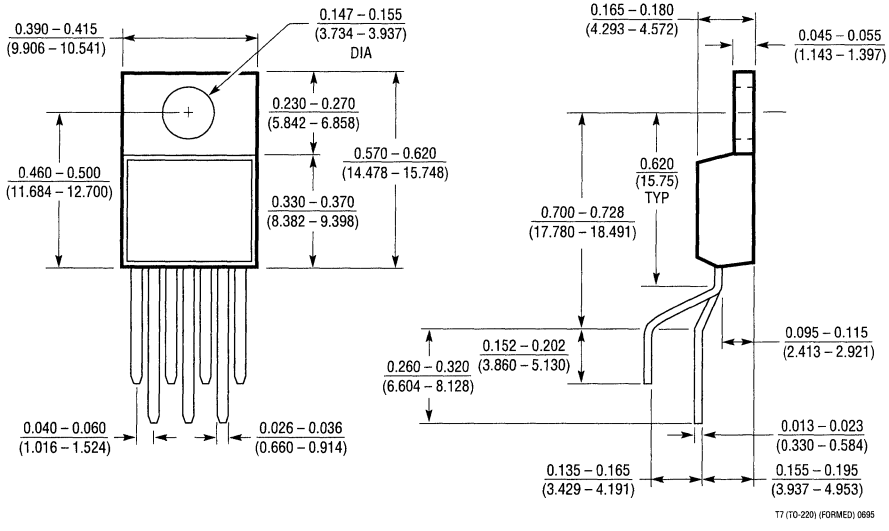
For Lead Bend Options See Page 14-54

T7 Package
7-Lead Plastic TO-220 (Straight Lead)
(Nonstandard Flow 06)
(LTC DWG # 05-08-1422)



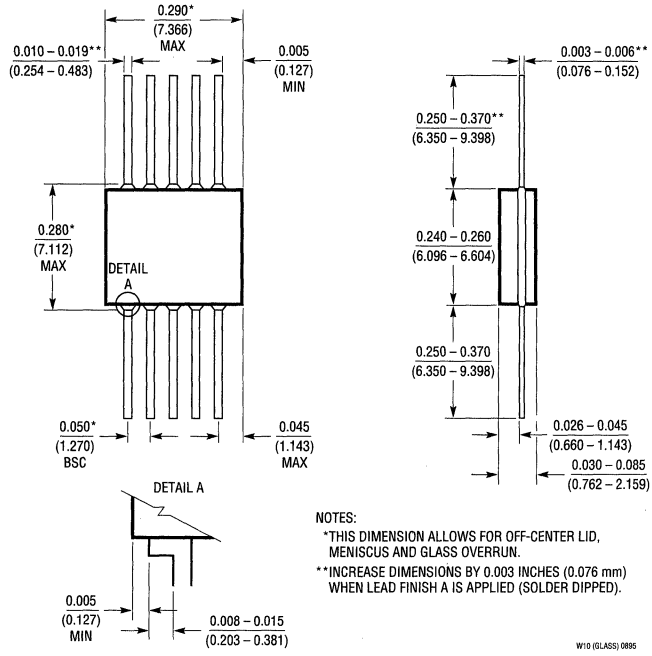
For Lead Bend Options See Page 14-54

T7 Package
7-Lead Plastic TO-220 (Standard)
(LTC DWG # 05-08-1422)



For Lead Bend Options See Page 14-54

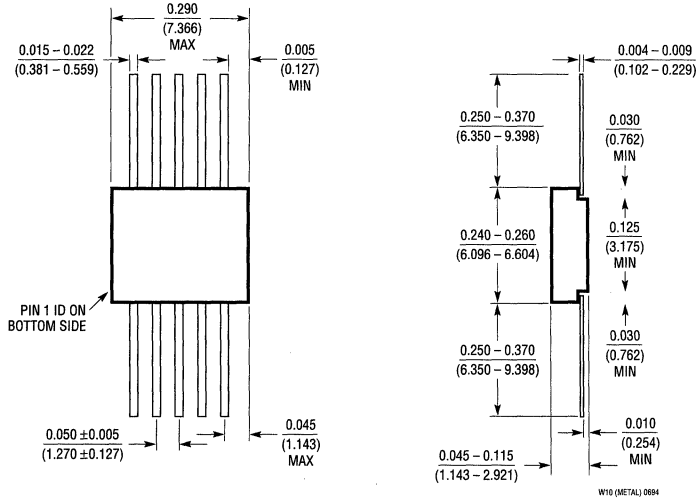
W Package
10-Lead Flatpak Glass Sealed (Hermetic)
(LTC DWG # 05-08-1130)



NOTES:
*THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
**INCREASE DIMENSIONS BY 0.003 INCHES (0.076 mm) WHEN LEAD FINISH A IS APPLIED (SOLDER DIPPED).

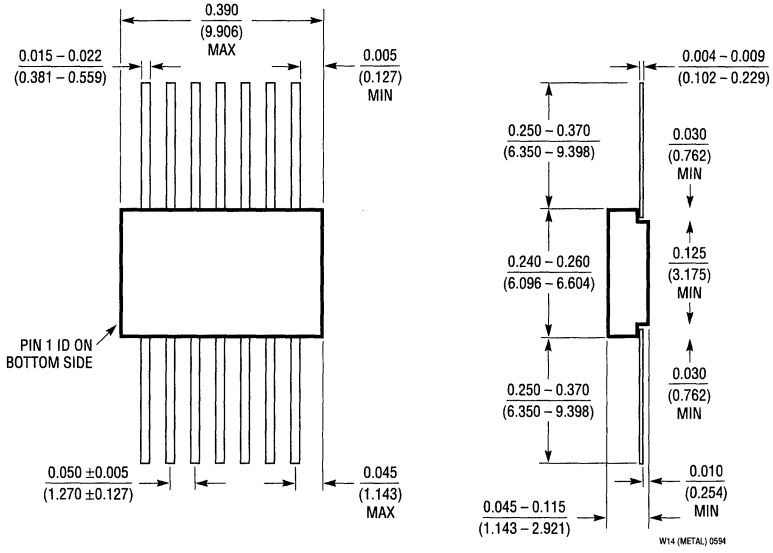
W10 (GLASS) 0895

WB Package
10-Lead Flatpak Metal Sealed Bottom Brazed (Hermetic)
(LTC DWG # 05-08-1230)

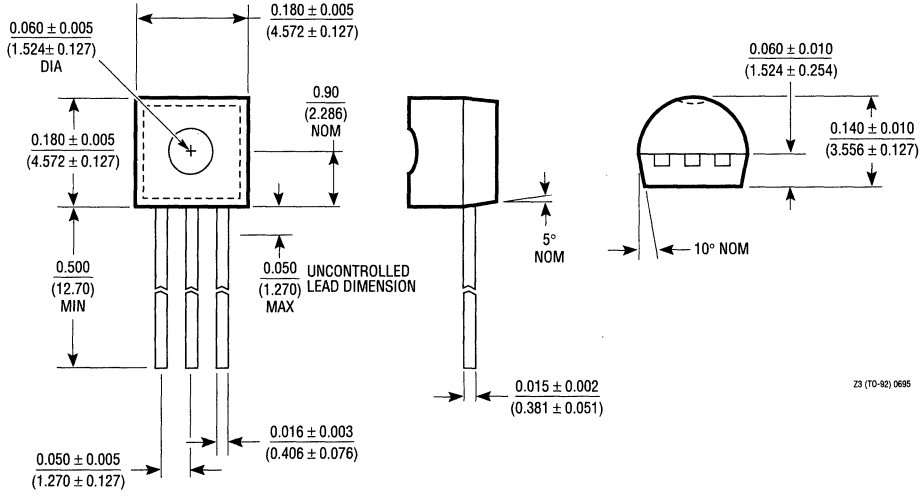


W10 (METAL) 0894

WB Package
14-Lead Flatpak Metal Sealed Bottom Brazed (Hermetic)
(LTC DWG # 05-08-1240)



Z Package
3-Lead Plastic TO-92 (Similar to TO-226)
(LTC DWG # 05-08-1410)



14

Introduction

Linear Technology Corporation (LTC) was founded in 1981 to address the growing demand for high performance and superior quality linear integrated circuits.

Today, LTC has successfully established a leadership position by introducing and supplying leading edge products in each of the industry's basic functional groups—op amps, comparators, voltage regulators, references, switched-capacitor filters, interface, data conversion, and a variety of special function CMOS devices, in all major package styles.

Early on, LTC made the commitment to provide advanced technology, *surface mount packaging.* This made Linear Technology the first company to offer true precision and high performance linear devices across the full range of functional categories, plus many of the popular second-source devices in JEDEC Standard packages:

SO (0.150) 8, 14, 16

SO (0.300) 16, 18, 20, 24, 28

SSOP (0.150) 16, 20, 24

SSOP (0.209) 16, 20, 24, 28

SSOP (0.300) 36, 44

TSSOP (0.173) 20

The continuing demand for more complete surface mount designs has spurred the introduction of two power surface mount packages by LTC—the 3-lead SOT-223 and the DD package available in 3-, 5- and 7-lead versions. Many LTC power products are now being introduced in these packages which, for the first time, enable high power designs to be realized using 100% surface mount devices. Support for LTC's surface mount devices includes service for tape and reel, antistatic rails, quality and reliability data, and data sheets on each product.

LTC intends to address customer demand for surface mount devices where technology and die sizes permit, making the combination of small package size and high performance linear devices readily available to our users.

This section contains information summarizing LTC's capabilities and services for surface mount packaged products, as well as specific device data sheets.

Package Descriptions

LTC's SO packages conform to Standard JEDEC Small Outline drawings.

In some instances, an LTC product available in an 8-pin standard DIP package is offered in a 16-pin SO package. This covers the situation where the die is too large to be accommodated by the smaller SO-8 package. Although it is preferable for an SO-8 device to have the same pinout as the standard 8-pin dual-in-line version, some devices necessitate a rotation of the die to fit in the SO-8 package. Please refer to the applicable SO device data sheet, or consult with the factory to verify exact pinouts for each device.

Electrical Specifications

Wherever possible, electrical specifications for a surface mount technology (SMT)* device are the same as the plastic molded equivalent. Exceptions to this are identified by the omission of the standard product electrical grade designator from the part number.

For example:

- LT1013DS8 has the same electrical specifications as LT1013DN8, since the "D" is common to both product numbers.
- LT1012S8 has one or more different electrical specifications than LT1012CN8, as the "C" is missing from this product designator suffix.

Please consult the appropriate SMT package data sheet for complete electrical specifications.

* Terminology: SO = Small Outline, SOT = Small Outline Transistor, SSOP = Shrink Small Outline Package, TSSOP = Thin Shrink Small Outline Package.

LTC package code designators for SMT products are:
F = TSSOP, G = SSOP, GN = Narrow Body SSOP, GW = Wide Body SSOP, M, Q and R = DD Pak, S = Narrow Body SO, SW = Wide Body SO, ST = SOT-223.

Marking

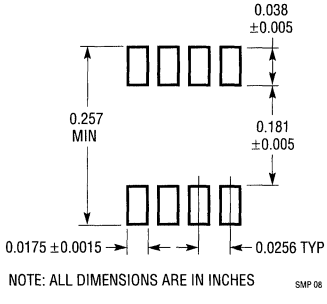
Because of the limited space available for part marking on some SMT packages, abbreviated marking codes are used to identify the device. These codes, if used, are identified in the individual SMT package data sheets.

Lead Finish and Solderability

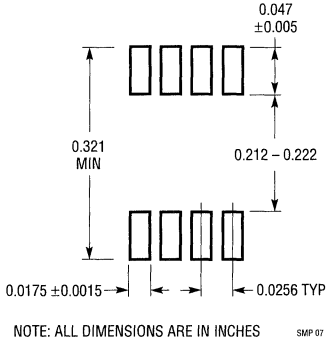
Lead finish is electroplated, lead-tin, with a low carbon content. Solderability meets the requirements of MIL-STD-883C, Method 2003. Recommended solder pads are given in Figure 1.

Recommended Solder Pads

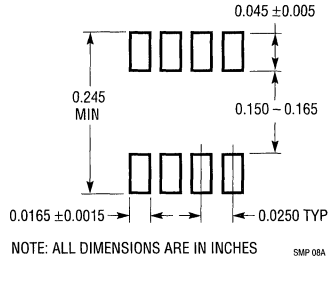
F Package (0.173)
TSSOP-20



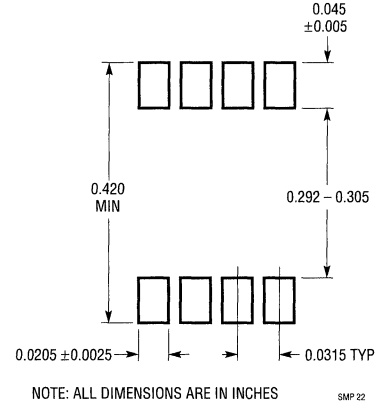
G Package (0.209)
SSOP-20, SSOP-24, SSOP-28



GN Package Narrow (0.150)
SSOP-16, SSOP-20, SSOP-24



GW Package Wide (0.300)
SSOP-36, SSOP-44



M Package
3-Lead DD

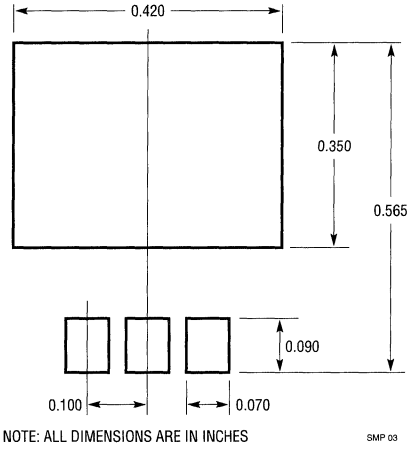
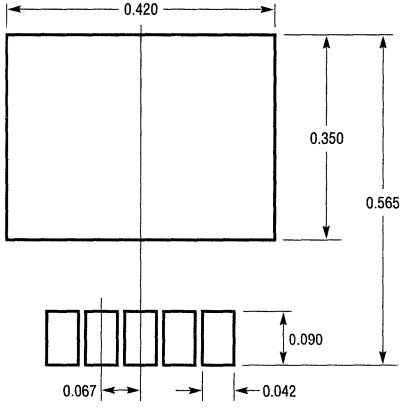


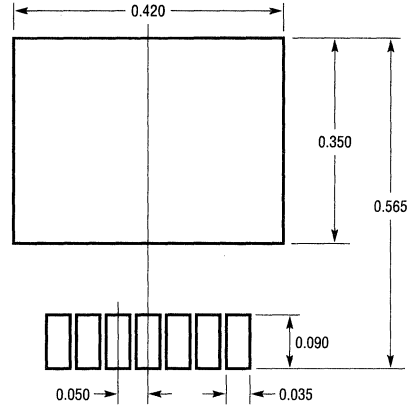
Figure 1. Recommended Solder Pads

Q Package
5-Lead DD



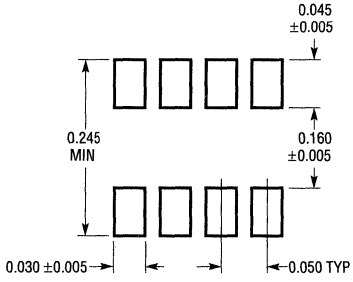
NOTE: ALL DIMENSIONS ARE IN INCHES SMP 04

R Package
7-Lead DD



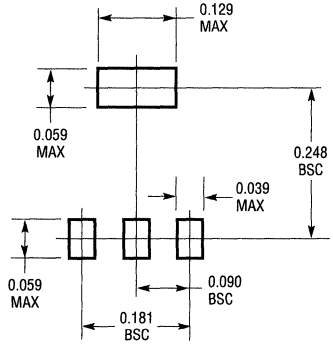
NOTE: ALL DIMENSIONS ARE IN INCHES SMP 05

S Package (0.150)
SO-8, SO-14, SO-16



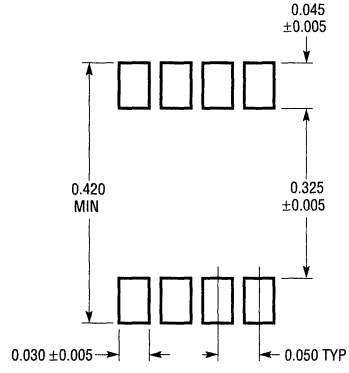
NOTE: ALL DIMENSIONS ARE IN INCHES SMP 01

ST Package
3-Lead SOT-223



NOTE: ALL DIMENSIONS ARE IN INCHES SMP 06

SW Package Wide (0.300)
SO-16, SO-18, SO-20, SO-24, SO-28



NOTE: ALL DIMENSIONS ARE IN INCHES SMP 02

Figure 1. Recommended Solder Pads (Continued)

Vave and Reflow Soldering

ollowing are the recommended procedures for soldering urface mount packages to PC boards.

. Wave Soldering

- Use solder plating boards.
- Dispense adhesive to hold components on board.
- Place components on board.
- Cure adhesive per adhesive manufacturer's specification.
- Foam flux using RMA (Rosin Mildly Activating) flux.
- Wave solder using a dual wave soldering system at 240°C to 260°C for 2 seconds per wave.
- Clean board.

. Reflow Soldering

- Use of solder plating boards is recommended.
- Screen solder paste on board.
- Mount components on board.
- Infrared or forced hot air convection reflow is recommended for best performance.
- Preheat peak temperature 125°C ± 15°C and 2°C to 5°C per second rise.
- Activation temperature 130°C to 150°C.
- Reflow begins at 183°C (63Sn/37Pb).
- Time above 183°C for at least 30 seconds.
- Peak package body temperature 220°C maximum.
- Cooling rate 2°C to 5°C per second.
- Clean boards.
- For Vapor Phase Reflow, recommended parameter ranges for:
  - Heating rate: 6°C per second maximum
  - Preheat temperature: 45°C to 80°C
  - Time above 200°C: 50 seconds to 90 seconds
  - Peak package temperature: 212°C to 219°C
- Hand soldering of DD and SOT-223 package is not recommended.

hermal Information

able 1 shows the range of junction-to-ambient thermal sistance of SO devices mounted on a PCB of FR4 material with copper traces, in still air at 25°C. θ_{JA} with a ceramic substrate is about 70% of the FR4 value. Maximum power dissipation may be calculated by the following formula:

$$P_{DMAX}(T_A) = \frac{T_{JMAX} - T_A}{\theta_{JA}}$$

where,

T_{JMAX} = Maximum operating junction temperature.
T_A = Desired ambient operating temperature.
θ_{JA} = Junction-to-ambient thermal resistance.

Table 1. Typical Thermal Resistance Values

SO-8	150°C/W to 200°C/W	SO-18	70°C/W to 100°C/W
SO-14	100°C/W to 140°C/W	SO-20	70°C/W to 90°C/W
SO-16 (0.150)	90°C/W to 130°C/W	SO-24	60°C/W to 80°C/W
SO-16 (0.300)	85°C/W to 100°C/W	SO-28	55°C/W to 75°C/W

Conditions: PCB mount on FR4 material, still air at 25°C, copper trace.

Thermal resistance for power packages (DD and SOT-223) depends greatly on the individual device type. Please consult the device data sheets for thermal information.

More current data, by device type, may be obtained by contacting LTC, Marketing Department.

Tape and Reel Packing (See Tape and Reel Section)

Plastic Tube Packing

LTC's Surface Mount products are packed in "antistatic" plastic tubes with the tube dimensions indicated in Figure 2. Unit quantities packaged per tube are listed below in Table 2.

Table 2. Devices Per Tube

LTC Package Code Designator	LTC Package Style	Actual Lead Count	Number of Units
F	TSSOP (0.173)	20	74
G	SSOP (0.209)	16	77
G	SSOP (0.209)	20	66
G	SSOP (0.209)	24	59
G	SSOP (0.209)	28	47
GN	SSOP (0.150)	16	100
GN	SSOP (0.150)	20, 24	55
GW	SSOP (0.300)	36	32
GW	SSOP (0.300)	44	27

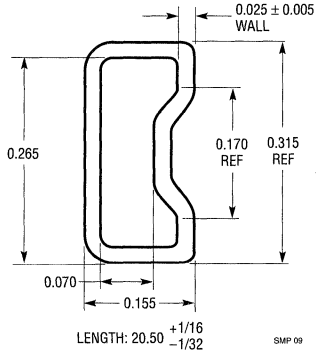
Table 2. Devices Per Tube

LTC Package Code Designator	LTC Package Style	Actual Lead Count	Number of Units
M, Q, R	DD	3, 5, 7	50
S8	S8 (0.150)	8	100
S	S (0.150)	14	55
S	S (0.150)	16	50
ST	SOT-223	3	78

LTC Package Code Designator	LTC Package Style	Actual Lead Count	Number of Units
SW	SW (0.300)	16	47
SW	SW (0.300)	18	40
SW	SW (0.300)	20	38
SW	SW (0.300)	24	32
SW	SW (0.300)	28	27

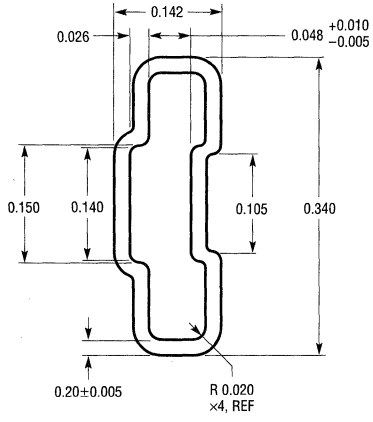
PLASTIC TUBE SPECIFICATIONS

S (0.150)
SO Package Shipping Tube



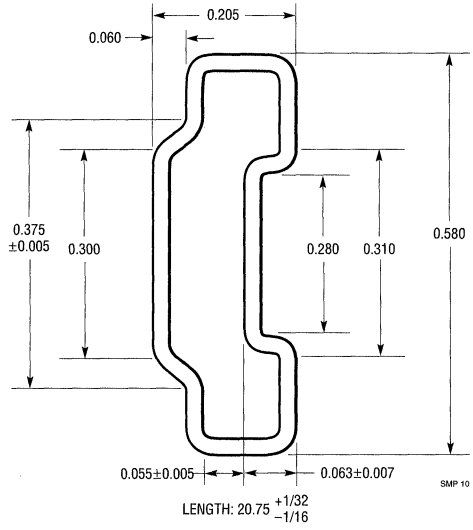
NOTE: ALL DIMENSIONS ARE IN INCHES

ST
SOT-223 Package Shipping Tube



NOTE: ALL DIMENSIONS ARE IN INCHES
SMP 11

SW (0.300)
SO Package Shipping Tube



NOTE: ALL DIMENSIONS ARE IN INCHES

Note 1: Tolerances: ±0.010 unless otherwise specified.

Note 2: Material: antistatic treated rigid transparent PVC or rigid black conductive.

Note 3: Printing: "LTC logo, Linear Technology Corp., Antistatic" on topside of tube.

Figure 2

urface Mount Small Outline (SO), DD and SOT Device Packaging

near Technology now offers a continually increasing number of high ırformance CMOS and bipolar linear devices in surface mount packages. sted in the next several pages are device types now available in the DD power ıckages and the JEDEC standard outline packages; SO (Small Outline 0.150 ıd 0.300 body widths), SSOP (Shrink Small Outline 0.150, 0.209 and 0.300 body widths), TSSOP (Thin Shrink Small Outline 0.173 body width) and SOT-223 (Small Outline Transistor). For pinout configurations and electrical specification limits, consult either your LTC sales representative or the factory.

Surface Mount Packages:	DD	SO	SOT-223	SSOP	TSSOP
LTC Package Suffix:	M, Q, R	S8, S, SW	ST	G, GN, GW	F

PRODUCT		DESCRIPTION
Operational Amplifiers		
LF398	S8	Sample & Hold Amp
LM318	S8	Fast Op Amp
LT1001C	S8	Precision Op Amp
LT1006	S8	Precision Single Supply Op Amp
LT1007C	S8	Low Noise, High Speed, Precision Op Amp
LT1008	S8	Uncompensated, Picoamp Input, Precision Op Amp
LT1012	S8	Picoamp Input Current, Precision Op Amp, C-Load™
LT1013D	S8	Dual Precision Single Supply Op Amp
LT1013I	S8	Dual Precision Single Supply Op Amp
LT1014D	SW	Quad Precision Single Supply Op Amp
LT1014I	SW	Quad Precision Single Supply Op Amp
LT1028C	S8	Ultra Low Noise Op Amp
LT1037C	S8	Low Noise, High Speed Precision Op Amp
LTC1047C	SW	Dual Micropower Zero-Drift Op Amp w/Internal Caps
LTC1049C	S8	Low Power Zero-Drift Op Amp w/Internal Caps
LTC1050C	S8	Zero-Drift Op Amp w/Internal Caps
LTC1051C	SW	Dual Zero-Drift Op Amp w/Internal Caps
LTC1052C	SW	Low Noise Zero-Drift Op Amp
LTC1053C	SW	Quad Precision Zero-Drift Op Amp w/Internal Caps
LT1055	S8	JFET Input, High Speed, Precision Op Amp
LT1056	S8	JFET Input, High Speed, Precision Op Amp
LT1057	S8	Dual JFET Input, High Speed, Precision Op Amp
LT1057I	S8	Dual JFET Input, High Speed, Precision Op Amp
LT1058	SW	Quad JFET Input, High Speed, Precision Op Amp
LT1058I	SW	Quad JFET Input, High Speed, Precision Op Amp
LT1077	S8	Precision Micropower Op Amp
LT1078	S8	Dual Precision Micropower Op Amp
LT1078I	S8	Dual Precision Micropower Op Amp
LT1079	SW	Quad Precision Micropower Op Amp
LT1079I	SW	Quad Precision Micropower Op Amp
LT1097	S8	Low Cost, Low Power, Precision Op Amp
LT1112	S8	Dual Precision Op Amp, C-Load
LT1113C	S8	Dual Low Noise, Precision, JFET Input Op Amp
LT1114	SW	Quad Precision Op Amp, C-Load
LT1115C	SW	50MHz, 11V/µs, 1nV/√Hz Audio Op Amp
LT1122C	S8	Fast Settling, JFET Input Op Amp
LT1122D	S8	Fast Settling, JFET Input Op Amp
LT1124C	S8	Dual Low Noise, High Speed, Precision Op Amp
LT1125C	SW	Quad Low Noise, High Speed, Precision Op Amp
LT1126C	S8	Decomp Dual Low Noise, High Speed, Precision Op Amp
LT1127C	SW	Decomp Dual Low Noise, High Speed, Precision Op Amp
LT1128C	S8	Unity-Gain Stable Ultra Low Noise Op Amp
LTC1150C	S8	±15V Zero-Drift Op Amp w/Internal Caps
LTC1151C	SW	Dual ±15V Zero-Drift Op Amp
LTC1152C	S8	Rail-to-Rail Input/Output Zero-Drift Op Amp, C-Load
LTC1152I	S8	Rail-to-Rail Input/Output Zero-Drift Op Amp
LT1178	S8	Dual Precision Micropower Op Amp
LT1179	SW	Quad Precision Micropower Op Amp
LT1187C	S8	Low Power Video Difference Amp
LT1189C	S8	Low Power Video Difference Amp
LT1190C	S8	50MHz High Speed Video Op Amp
LT1191C	S8	90MHz High Speed Video Op Amp
LT1192C	S8	350MHz ($A_V \geq 25$)High Speed Video Op Amp
LT1193C	S8	80MHz (Adj Gain) High Speed Video Op Amp
LT1194C	S8	35MHz ($A_V = 10$) Fixed Differential Video Op Amp
LT1195C	S8	Low Power, High Speed Op Amp

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PRODUCT		DESCRIPTION
LT1200C	S8	Low Power, High Speed Op Amp, C-Load
LT1201C	S8	Dual Low Power, High Speed Op Amp, C-Load
LT1202C	S	Quad Low Power, High Speed Op Amp, C-Load
LT1206C	S8, R	250mA, 60MHz Current Feedback Amplifier, C-Load
LT1208C	S8	Dual Very High Speed Op Amp, C-Load
LT1209C	S	Quad Very High Speed Op Amp, C-Load
LT1211C	S8	14MHz Dual Precision Op Amp
LT1212C	S	14MHz Quad Precision Op Amp
LT1213C	S8	28MHz Dual Precision Op Amp
LT1214C	S	28MHz Quad Precision Op Amp
LT1215C	S8	23MHz Dual Precision Op Amp
LT1216C	S	23MHz Quad Precision Op Amp
LT1217C	S8	Low Power, 10MHz Current Feedback Amplifier
LT1220C	S8	Very High Speed Op Amp
LT1221C	S8	Very High Speed Op Amp ($A_V \geq 4$)
LT1222C	S8	Very High Speed Op Amp ($A_V \geq 10$,Ext Comp)
LT1223C	S8	100MHz Current Feedback Amplifier
LT1224C	S8	45MHz Very High Speed Op Amp, C-Load
LT1225C	S8	150MHz ($A_V \geq 5$) High Speed Op Amp
LT1226C	S8	1GHz ($A_V \geq 25$) High Speed Op Amp
LT1227C	S8	140MHz High Speed Current Feedback Op Amp
LT1228C	S8	100MHz Current Feedback Amplifier w/DC Gain Control
LT1229C	S8	Dual 100MHz Current Feedback Amplifier
LT1230C	S	Quad 100MHz Current Feedback Amplifier
LTC1250C	S8	Ultra Low Noise Zero-Drift Op Amp
LT1251C	S	40MHz Video Fader/Amplifier
LT1252C	S8	Low Cost Video Amplifier
LT1253C	S8	Low Cost Dual Video Amplifier
LT1254C	S	Low Cost Quad Video Amplifier
LT1256C	S	40MHz DC Gain Controller Amplifier
LT1259C	S	Dual 130MHz CFA with SHUTDOWN
LT1260C	S	Triple 130MHz CFA with SHUTDOWN
LT1311C	S	Quad 12Mhz, 145ns Settling Precision Current-to-Voltage Converter for Optical Disk Drives
LT1354C	S8	12MHz, 400V/µs Op Amp, C-Load
LT1355C	S8	Dual 12MHz, 400V/µs Op Amp, C-Load
LT1356C	S	Quad 12MHz, 400V/µs Op Amp, C-Load
LT1357C	S8	25MHz, 600V/µs Op Amp, C-Load
LT1358C	S8	Dual 25MHz, 600V/µs Op Amp, C-Load
LT1359C	S	Quad 25MHz, 600V/µs Op Amp, C-Load
LT1360C	S8	50MHz, 800V/µs Op Amp, C-Load
LT1361C	S8	Dual 4mA, 50MHz, 800V/µs Op Amp, C-Load
LT1362C	S	Quad 50MHz, 800V/µs Op Amp, C-Load
LT1363C	S8	70MHz, 1000V/µs Op Amp, C-Load
LT1364C	S8	Dual 6mA, 70MHz, 1000V/µs Op Amp, C-Load
LT1365C	S	Quad 70MHz, 1000V/µs Op Amp, C-Load
LT1366C	S8	Dual Rail-to-Rail Input/Output Op Amp
LT1367C	S	Quad Rail-to-Rail Input/Output Op Amp
LT1368C	S8	Dual Rail-to-Rail Input/Output Op Amp
LT1369C	S	Quad Rail-to-Rail Input/Output Op Amp
LT1413	S8	Dual Single-Supply, Precision Op Amp
LT1457	S8	Dual Precision JFET Op Amp, C-Load
OP-07C	S8	Precision Op Amp
OP-27G	S8	Low Noise, High Speed, Precision Op Amp
OP-37G	S8	Low Noise, High Speed, Precision Op Amp
OP-470G	S	Quad Low Noise, Precision Op Amp

Surface Mount Small Outline (SO), DD and SOT Device Packaging

PRODUCT		DESCRIPTION
Battery Management/Charging		
LT1239C	S	Backup Battery Management IC, Li-Ion or NiCd
LT1510C	S8	Battery Charger
LT1510C	S	Battery Charger
LT1512C	S8	SEPIC Battery Charger
LTC1325C	SW	µP-Controlled Battery Management System
Instrumentation Amps		
LTC1100AC	S8	Consult Factory
LTC1100C	SW	Chopper Stabilized Instrumentation Amp
LT1101	SW	Precision Micropower Instrumentation Amp
LT1101I	SW	Precision Micropower Instrumentation Amp
Comparators		
LT1011C	S8	Precision Volt Comparator
LT1016C	S8	High Speed Comparator
LT1016I	S8	High Speed Comparator
LT1017C	S8	Micropower Dual Comparator
LT1017I	S8	Micropower Dual Comparator
LT1018C	S8	Micropower Dual Comparator
LTC1040C	SW	Micropower Dual Sampling Comparator
LTC1041C	S8	Bang-Bang Controller
LT1116C	S8	High Speed, Ground-Sensing Comparator
LTC1443C	S	Quad Micropower Comparator and Reference
LTC1444C	S	Quad Micropower Comparator and Reference
LTC1445C	S	Quad Micropower Comparator and Reference
Data Acquisition		
LTC1090C	SW	10-Bit A/D with 8-Channel MUX & S/H
LTC1093C	SW	10-Bit A/D with 6-Channel MUX & S/H
LTC1096AC	S8	8-Bit Micropower A/D with S/H
LTC1096C	S8	8-Bit Micropower A/D with S/H
LTC1098AC	S8	8-Bit Micropower A/D with S/H
LTC1098C	S8	8-Bit Micropower A/D with S/H
LTC1099C	SW	8-Bit High Speed ADC with S/H
LTC1099I	SW	8-Bit High Speed ADC with S/H
LTC1196-1AC	S8	8-Bit, 600ns, 1MHz Sampling ADC
LTC1196-1BC	S8	8-Bit, 600ns, 1MHz Sampling ADC
LTC1196-2AC	S8	8-Bit, 710ns, 800kHz Sampling ADC
LTC1196-2BC	S8	8-Bit, 710ns, 800kHz Sampling ADC
LTC1198-1AC	S8	2-Channel, 8-Bit, 600ns, 750kHz, Sampling ADC
LTC1198-1BC	S8	2-Channel, 8-Bit, 600ns, 750kHz, Sampling ADC
LTC1198-2AC	S8	2-Channel, 8-Bit, 710ns, 750kHz, Sampling ADC
LTC1198-2BC	S8	2-Channel, 8-Bit, 710ns, 750kHz, Sampling ADC
LTC1257C	S8	12-Bit Complete V_{OUT} DAC
LTC1257I	S8	12-Bit Complete V_{OUT} DAC
LTC1272-3AC	SW	12-Bit 3µs Parallel I/O A/D with S/H
LTC1272-3BC	SW	12-Bit 3µs Parallel I/O A/D with S/H
LTC1272-3CC	SW	12-Bit 3µs Parallel I/O A/D with S/H
LTC1272-8AC	SW	12-Bit 8µs Parallel I/O A/D with S/H
LTC1272-8BC	SW	12-Bit 8µs Parallel I/O A/D with S/H
LTC1272-8CC	SW	12-Bit 8µs Parallel I/O A/D with S/H
LTC1273AC	SW	12-Bit 3µs Parallel I/O with S/H & Reference
LTC1273BC	SW	12-Bit 3µs Parallel I/O with S/H & Reference
LTC1274AI	SW	12-Bit 6µs Parallel I/O A/D with Reference and Shutdown
LTC1274C	SW	12-Bit 6µs Parallel I/O A/D with Reference and Shutdown
LTC1274I	SW	12-Bit 6µs Parallel I/O A/D with Reference and Shutdown
LTC1275AC	SW	12-Bit 3µs Parallel I/O with S/H & Reference
LTC1275BC	SW	12-Bit 3µs Parallel I/O with S/H & Reference
LTC1276AC	SW	12-Bit 3µs Parallel I/O with S/H & Reference
LTC1276BC	SW	12-Bit 3µs Parallel I/O with S/H & Reference
LTC1277AI	SW	12-Bit 6µs Parallel I/O with S/H & Reference
LTC1277C	SW	12-Bit 6µs Parallel I/O with S/H & Reference
LTC1277I	SW	12-Bit 6µs Parallel I/O with S/H & Reference
LTC1278-4C	SW	12-Bit 2.5µs High Speed Sampling A/D
LTC1278-4I	SW	12-Bit 2.5µs High Speed Sampling A/D
LTC1278-5C	SW	12-Bit 2.5µs High Speed Sampling A/D
LTC1278-5I	SW	12-Bit 2.5µs High Speed Sampling A/D

PRODUCT		DESCRIPTION
LTC1279C	SW	12-Bit 1.6µs Parallel I/O with S/H & Reference
LTC1279I	SW	12-Bit 1.6µs Parallel I/O with S/H & Reference
LTC1282AC	SW	12-Bit 6µs Parallel I/O with S/H & Reference
LTC1282BC	SW	12-Bit 6µs Parallel I/O with S/H & Reference
LTC1285C	S8	12-Bit 3V Micropower ADC with S/H
LTC1285I	S8	12-Bit 3V Micropower ADC with S/H
LTC1286C	S8	12-Bit Micropower A/D with S/H
LTC1286I	S8	12-Bit Micropower A/D with S/H
LTC1288C	S8	12-Bit 3V Micropower ADC with S/H
LTC1288I	S8	12-Bit 3V Micropower ADC with S/H
LTC1289BC	SW	12-Bit 3V 8-Channel MUX, S/H Full Duplex I/O
LTC1289CC	SW	12-Bit 3V 8-Channel MUX, S/H Full Duplex I/O
LTC1290BC	SW	12-Bit A/D with 8-Channel MUX & S/H
LTC1290BI	SW	12-Bit A/D with 8-Channel MUX & S/H
LTC1290CC	SW	12-Bit A/D with 8-Channel MUX & S/H
LTC1290CI	SW	12-Bit A/D with 8-Channel MUX & S/H
LTC1290DC	SW	12-Bit A/D with 8-Channel MUX & S/H
LTC1290DI	SW	12-Bit A/D with 8-Channel MUX & S/H
LTC1293BC	SW	12-Bit A/D with 6-Channel MUX & S/H
LTC1293CC	SW	12-Bit A/D with 6-Channel MUX & S/H
LTC1293DC	SW	12-Bit A/D with 6-Channel MUX & S/H
LTC1294BC	SW	12-Bit A/D with 8-Channel MUX & S/H
LTC1294BI	SW	12-Bit A/D with 8-Channel MUX & S/H
LTC1294CC	SW	12-Bit A/D with 8-Channel MUX & S/H
LTC1294DC	SW	12-Bit A/D with 8-Channel MUX & S/H
LTC1296BC	SW	12-Bit A/D with 8-Channel MUX & S/H, Single Supply
LTC1296BI	SW	12-Bit A/D with 8-Channel MUX & S/H, Single Supply
LTC1296CC	SW	12-Bit A/D with 8-Channel MUX & S/H, Single Supply
LTC1296CI	SW	12-Bit A/D with 8-Channel MUX & S/H, Single Supply
LTC1296DC	SW	12-Bit A/D with 8-Channel MUX & S/H, Single Supply
LTC1296DI	SW	12-Bit A/D with 8-Channel MUX & S/H, Single Supply
LTC1298C	S8	12-Bit Micropower A/D with S/H
LTC1298I	S8	12-Bit Micropower A/D with S/H
LTC1390C	S	8-Channel Serial I/O Analog MUX
LTC1392C	S8	10-Bit Environment Monitor ADC
LTC1392I	S8	10-Bit Environment Monitor ADC
LTC1400C	S8	Complete SO-8, 12-Bit 400ksps ADC with Shutdown
LTC1400I	S8	Complete SO-8, 12-Bit 400ksps ADC with Shutdown
LTC1410AC	SW	12-Bit 700ns Parallel I/O ADC with Reference and Shutdown
LTC1410BC	SW	12-Bit 700ns Parallel I/O ADC with Reference and Shutdown
LTC1410AI	SW	12-Bit 700ns Parallel I/O ADC with Reference and Shutdown
LTC1410BI	SW	12-Bit 700ns Parallel I/O ADC with Reference and Shutdown
LTC1410C	SW	12-Bit 700ns Parallel I/O ADC with Reference and Shutdown
LTC1410I	SW	12-Bit 700ns Parallel I/O ADC with Reference and Shutdown
LTC1451C	S8	12-Bit Complete V_{OUT} DAC
LTC1451I	S8	12-Bit Complete V_{OUT} DAC
LTC1452C	S8	12-Bit V_{OUT} Mulitplying Rail-to-Rail DAC
LTC1452I	S8	12-Bit V_{OUT} Mulitplying Rail-to-Rail DAC
LTC1453C	S8	12-Bit Complete V_{OUT} DAC 3V/5V Operation
LTC1453I	S8	12-Bit Complete V_{OUT} DAC 3V/5V Operation
LTC1522C	S	4-Channel 3V Micropower Sampling 12-Bit Serial I/O ADC
LTC7541AJ	S	Improved Industry Std CMOS 12-Bit Multiplying DAC
LTC7541AK	SW	Improved Industry Std CMOS 12-Bit Multiplying DAC
LTC7543GK	SW	Improved Industry Std Serial 12-Bit Multiplying DAC
LTC7543K	SW	Improved Industry Std Serial 12-Bit Multiplying DAC
LTC8043E	S8	Serial 12-Bit Multiplying DAC in SO-8
LTC8043F	S8	Serial 12-Bit Multiplying DAC in SO-8
LTC8143E	SW	Improved Industry Std Serial 12-Bit Multiplying DAC
LTC8143F	SW	Improved Industry Std Serial 12-Bit Multiplying DAC

Surface Mount Small Outline (SO), DD and SOT Device Packaging

PRODUCT		DESCRIPTION
Regulators, PWMs, DC/DC Converters		
LT1020C	SW	µPower Low Dropout Regulator with Comparator
LT1020I	SW	µPower Low Dropout Regulator with Comparator
LT1072C	S8	40kHz 1.25A Switching Regulator
LT1073C	S8 S8-5,12	µPower Switching Regulator Works Down to 1V Input, Adjustable & Fixed 5V, 12V Outputs
LT1076C	Q	2A Step-Down Switching Regulator
LT1076C	Q	2A Step-Down Switching Regulator, +5V Output
LT1076C	R	2A Step-Down Switching Regulator with Shutdown, 5-Lead DD Package, Adjustable Output
LT1076C	R-5	2A Step-Down Switching Regulator with Shutdown, 7-Lead DD Package, 5V
LT1076HVC	R	2A Step-Down Switching Regulator, 7-Lead DD Pkg
LT1084C	M	5A Low Dropout Regulator, 3-Lead DD Package
LT1085C	M	Adjustable Low Dropout Pos Voltage Regulator, 3A
LT1085C	M-3.3	3.3V Low Dropout Voltage Regulator, 3A
LT1085C	M-3.6	3.6V Low Dropout Voltage Regulator, 3A
LT1086C	M	1.5A Low Dropout Regulator, 3-Lead DD Pkg
LT1086C	M-3.3	3.3V Low Dropout Positive Voltage Regulator, 1.5A
LT1086C	M-3.6	3.6V Low Dropout Positive Voltage Regulator, 1.5A
LT1107C	S8 S8-5,12	µPower DC/DC Converter Works Down to 2V Input, Adjustable & Fixed 5V, 12V Outputs
LT1108C	S8, S8-5, S8-12	µPower DC/DC Converter Works Down to 2V Input, Adjustable & Fixed 5V, 12V Outputs
LT1109AC	S8	µPower DC/DC Converter with Shutdown & 100kHz Swtiching Frequency, Adjustable & Fixed 5V, 12V Outputs
LT1109AC	S8-5	µPower Switching Regulator, 5V Output
LT1109AC	S8-12	µPower Switching Regulator, 12V Output
LT1109C	S8, S8-5, S8-12	µPower DC/DC Converter with Shutdown & 100kHz Switching Frequency, Adjustable & Fixed 5V, 12V Outputs
LT1110C	S8, S8-5, S8-12	µPower DC/DC Converter Works Down to 1V Input, Adjustable & Fixed 5V, 12V Outputs
LT1111C	S8, S8-5, S8-12	µPower Switching Regulator Works Down to 2V Input, Adjustable & Fixed 5V, 12V Outputs
LT1111I	S8	µPower Adjustable Switching Regulator
LT1117C	M	Adjustable Low Dropout Regulator
LT1117C	M-3.3	3.3V Low Dropout Regulator
LT1117C	M-5	5V Low Dropout Regulator
LT1117C	ST	Low Dropout 800mA Adjustable Regulator
LT1117C	ST-5	Low Dropout 800mA Regulator, 5V
LT1117C	ST-2.85	Active SCSI-2 Terminator, 2.85V
LT1117C	ST-3.3	Low Dropout 800mA Fixed 3.3V Regulator
LT1118C	S8-2.5	2.5V Source/Sink Low Dropout Regulator
LT1118C	S8-2.85	SCSI Source/Sink Terminator
LT1118C	S8-5	5V Source/Sink Low Dropout Regulator
LT1118C	ST-2.5	2.5V Source/Sink Low Dropout Regulator
LT1118C	ST-2.85	SCSI Source/Sink Terminator
LT1118C	ST-5	5V Source/Sink Low Dropout Regulator
LT1120AC	S8	µPower Voltage Regulator and Comparator with Shutdown
LT1120C	S8	µPower Low Dropout Regulator with Shutdown
LT1121AC	S8, S8-3.3, 5	µPower Low Dropout Regulator with Shutdown, Adjustable & Fixed 3.3V, 5V Outputs
LT1121AI	S8	Adjustable Low Dropout µP Regulator
LT1121AI	S8-3.3	3.3V Low Dropout µPower Regulator
LT1121AI	S8-5	5V Low Dropout µPower Regulator
LT1121C	S8, S8-3.3, 5	µPower Low Dropout Regulator with Shutdown, Adjustable & Fixed 3.3V, 5V Outputs
LT1121C	ST-3.3, 5	µPower Low Dropout Regulator, Fixed 3.3V, 5V Output
LT1121I	S8	Adjustable Low Dropout µPower Regulator
LT1121I	S8-3.3	3.3V Low Dropout µPower Regulator
LT1121I	S8-5	5V Low Dropout µPower Regulator
LT1121I	ST-3.3	3.3V Low Dropout µPower Regulator
LT1121I	ST-5	5V Low Dropout µPower Regulator
LT1123C	ST	Low Dropout Regulator Driver
LT1129C	Q, Q-3.3	700mA µPower Low Dropout Voltage Regulator
LT1129C	Q-5	µPower Low Dropout Regulator, Fixed 5V Output
LT1129C	S8	Adjustable 700mA µPower Low Droput Regulator
LT1129C	S8-3.3	3.3V 700mA µPower Low Droput Regulator

PRODUCT		DESCRIPTION
LT1129C	S8-5	5V 700mA µPower Low Droput Regulator
LT1129C	ST-3.3	700mA µPower Low Droput Regulator
LT1129C	ST-5	µPower Low Dropout Regulator, Fixed 5V Output
LT1129I	Q, Q-3.3, Q-5	700mA µPower Low Dropout Voltage Regulator
LT1129I	S8	Adjustable 700mA µPower Low Droput Regulator
LT1129I	S8-3.3, 5	3.3V and 5V 700mA µPower Low Droput Regulator
LT1129I	ST-3.3, 5	700mA µPower Low Droput Regulator, 3.3V and 5V Fixed
LTC1142C	G	Dual High Efficiency Switching Regulator Controller
LTC1142HVC	G	HV Dual High Efficiency Switching Regulator Controller
LTC1142HVC	G-ADJ	Adjustable HV Dual High Efficiency Sw. Reg. Controller
LTC1143C	SW	Dual High Efficiency Switching Regulator Controller
LTC1144C	S8	20V Switched Capacitor Voltage Converter
LTC1144I	S8	20V Switched Capacitor Voltage Converter
LTC1147C	S8-3.3, 5	High Efficiency Step-Down Switching Regulator Controller
LTC1147LC	S8, S8-3.3	High Efficiency Step-Down Switching Regulator Controller
LTC1148C	S, S-3.3, 5	High Efficiency Step-Down Synchronous Switching Regulator Controller
LTC1148HVC	S, S-3.3, 5	High Efficiency Step-Down Synchronous Switching Regulator Controller
LTC1148LC	S, S-3.3	High Efficiency Step-Down Synchronous Switching Regulator Controller
LTC1149C	S, S-3.3, 5	High Efficiency Step-Down Synchronous Switching Regulator Controller, 48V Inputs
LTC1159C	S, S-3.3, 5	High Efficiency Step-Down Synchronous Switching Regulator Controller
LTC1159C	G, G-3.3, 5	High Efficiency Step-Down Synchronous Switching Regulator Controller
LT1170C	Q	100kHz 5A Switching Regulator, 5-Lead DD Pkg
LT1171C	Q	100kHz 2.5A Switching Regulator, 5-Lead DD Pkg
LT1172C	SW	100kHz 1.25A Switching Regulator
LT1172C	S8	1.25A High Efficiency 100kHz Switching Regulator
LT1172C	Q	100kHz 1.25A Switching Regulator, 5-Lead DD Pkg
LT1172I	S8	100kHz 1.25A Power Switching Regulator
LT1173C	S8 S8-5,12	µPower Switching Regulator for Inputs Greater than 2V, Adjustable & Fixed 5V, 12V Versions
LTC1174C	S8, S8-3.3, 5	High Efficiency, 400mA Step-Down Switching Regulator
LTC1174HVC	S8	HV Adjustable µPower Step-Down DC/DC Converter
LTC1174HVC	S8-3.3	HV 3.3V µPower Step-Down DC/DC Converter
LTC1174HVC	S8-5	HV 5V µPower Step-Down DC/DC Converter
LTC1174I	S8	Adjustable µPower Step-Down DC/DC Converter
LT1175C	S8-5	–5V Micropower Low Dropout Regulator
LT1175C	S8-ADJ	Negative Adjustable Low Dropout Regulator
LT1176C	SW	100kHz 1A Step-Down Switching Regulator with Shutdown
LT1176C	SW-5	5V 1A Step-Down Switching Regulator
LT1182C	S	LCD/CCFL Dual Switching Regulator
LT1183C	S	LTC/CCFL Dual Switching Regulator
LT1184C	S	CCFL Switching Regulator for Grounded Bulbs
LT1184FC	S	CCFL Switching Regulator for Floating or Grounded Bulbs
LT1186C	S	CCFL Switching Regulator w/Digital Brightness Control
LT1241C	S8	Current Mode PWM Controller
LT1241I	S8	Current Mode PWM Controller
LT1242C	S8	Current Mode PWM Controller
LT1242I	S8	Current Mode PWM Controller
LT1243C	S8	Current Mode PWM Controller
LT1243I	S8	Current Mode PWM Controller
LT1244C	S8	Current Mode PWM Controller
LT1244I	S8	Current Mode PWM Controller
LT1245C	S8	Current Mode PWM Controller
LT1245I	S8	Current Mode PWM Controller
LT1246C	S8	1MHz Current Mode PWM Controller
LT1247C	S8	1MHz Current Mode PWM Controller
LT1248C	S	Power Factor Correction Contoller
LT1248I	S	Power Factor Correction Contoller
LT1249C	S8	8-Pin Power Factor Correction Controller
LT1249I	S8	8-Pin Power Factor Correction Controller

Surface Mount Small Outline (SO), DD and SOT Device Packaging

PRODUCT		DESCRIPTION
LTC1262C	S8	12V, 30mA VPP Generator
LTC1265C	S, S-3.3, 5	1.2A High Efficiency Step-Down DC/DC Converter in Adjustable, Fixed 3.3V and 5V Output
LTC1266C	S, S-3.3, 5	High Efficiency Synchronous Switching Regulator Controller in Adjustable, Fixed 3.3V and 5V Output
LTC1267C	G, G-ADJ, G-ADJ5	Dual High Voltage High Efficiency Synchronous Switching Regulator Controller
LT1268BC	Q	7.5A, 150kHz Switching Regulator
LT1268C	Q	7.5A, 150kHz Switching Regulator, 5-Lead Package
LT1269C	Q	4A, Power Switching Regulator, 5-Lead DD Package
LT1269C	SW	100kHz 4A Switching Regulator, 20-Lead SOIC
LT1271C	Q	60kHz 4A Switching Regulator, 5-Lead DD Package
LT1300C	S8	µPower Step-Up DC/DC Converter, 1.8V Input
LT1301C	S8	µPower Step-Up DC/DC Converter, 1.8V Input
LT1301I	S8	5V/12V µPower DC/DC Boost Converter
LT1302C	S8	µPower High Current Step-Up DC/DC Converter
LT1302C	S8-5	µPower High Current Step-Up Fixed 5V Output DC/DC Converter
LT1303C	S8	5V/12V µPower DC/DC Boost Converter with LBD
LT1303C	S8-5	5V µPower DC/DC Boost Converter with LBD
LT1304C	S8, S8-3.3, 5	Micropower DC/DC Converter with Low-Batery Detector Active in Shutdown
LT1305C	S8	Micropower High Current DC/DC Converter
LT1309C	S8	500kHz Micropower DC/DC Converter
LT1371C	R	3A/500kHz High Efficiency Switching Regulator
LT1371C	SW	3A/500kHz High Efficiency Switching Regulator
LT1372C	S8	1.5A/500kHz Step-Up Switching Regulator
LT1373C	S8	1.5A/250kHz Step-Up Switching Regulator
LT1375C	S8, S8-5	1.5A/500kHz Step-Down Switching Regulator in Adjustable and Fixed 5V Outputs
LT1375I	S8, S8-5	1.5A/500kHz Step-Down Switching Regulator in Adjustable and Fixed 5V Outputs
LT1376C	S8, S8-5	1.5A/500kHz Step-Down Switching Regulator in Adjustable and Fixed 5V Outputs
LT1376I	S8, S8-5	1.5A/500kHz Step-Down Switching Regulator in Adjustable and Fixed 5V Outputs
LT1377C	S8	1.5A/1MHz Step-Up Switching Regulator
LTC1430C	S, S8	High Power Step-Down Switching Regulator
LT1432C	S8	High Efficiency Switching Regulator Controller
LT1432C	S8-3.3	High Efficiency 3.3V Controller
LT1521C	S8	300mA µPower Low Dropout Adjustable Voltage Regulator
LT1521C	S8-3.0	300mA µPower Low Dropout 3V Voltage Regulator
LT1521C	S8-3.3	300mA µPower Low Dropout 3.3V Voltage Regulator
LT1521C	S8-5	300mA µPower Low Dropout 5V Voltage Regulator
LT1521C	ST-3.0	300mA µPower Low Dropout 3V Voltage Regulator
LT1521C	ST-3.3	300mA µPower Low Dropout 3.3V Voltage Regulator
LT1521C	ST-5	300mA µPower Low Dropout 5V Voltage Regulator
LT1521I	S8	300mA µPower Low Dropout Adj Voltage Regulator
LT1521I	S8-3.0	300mA µPower Low Dropout 3V Voltage Regulator
LT1521I	S8-3.3	300mA µPower Low Dropout 3.3V Voltage Regulator
LT1521I	S8-5	300mA µPower Low Dropout 5V Voltage Regulator
LT1521I	ST-3.0	300mA µPower Low Dropout 3V Voltage Regulator
LT1521I	ST-3.3	300mA µPower Low Dropout 3.3V Voltage Regulator
LT1521I	ST-5	300mA µPower Low Dropout 5V Voltage Regulator
LT1572C	S	1.5A Switching Regulator w/Built-In Schottky Rectifier
LTC1574C	S, S-3.3, S-5	High Efficiency Step-Down Switching Regulator with Internal Schottky Rectifier
LT1585C	M	4A and 4.6A Low Dropout Regulator, 3-Lead DD Package, Fixed Output
LT1585C	M-3.3, M-3.38, M-3.45, M-3.6	3.3V, 3.38V, 3.45V, 3.6V and Adjustable Outputs
LT1587C	M, M-3.3 M-3.45, M-3.6	3A Low Dropout Regulator, 3-Lead DD Package, Fixed and Adjustable Output Voltage
SG3524	S	Pulse Width Modulator

PRODUCT		DESCRIPTION
Switched-Capacitor Voltage Converters		
LTC660C	S8	High Current Switched-Capacitor Voltage Converter
LT1026C	S8	5V to ±10V Switched-Capacitor Voltage Converter
LTC1043C	SW	Dual Precision Instrumentation Switched Capacitor Building Block
LTC1044AC	S8	Switched-Capacitor Voltage Converter, 13V
LTC1044C	S8	Switched-Capacitor Voltage Converter
LTC1044AI	S8	Switched-Capacitor Voltage Converter, 13V
LTC1046C	S8	50mA Switched-Capacitor Voltage Converter
LTC1046I	S8	50mA Switched-Capacitor Voltage Converter
LT1054C	S8, SW	100mA Switched-Capacitor Voltage Converter
LT1054I	SW	100mA Switched-Capacitor Voltage Converter
LTC1144C	S8	20V Switched-Capacitor Voltage Converter
LTC1144I	S8	20V Switched-Capacitor Voltage Converter
LTC1261C	S, S8, S8-4 S8-4.5	Switched-Capacitor Voltage Inverter for GaAs FET Bias
LTC1429C	S, S8-4	(+)-to-(–) Converter w/Regulation, External Clock
LTC1550C	G, G-4.1 G8-4.1	Low Noise, (+)-to(–) Switched-Capacitor Converter
LTC1550C	S, S8-4.1	Low Noise, (+)-to(–) Switched-Capacitor Converter
LTC1551C	G-4.1 G8-4.1 S-4.1 S8-4.1	Low Noise, (+)-to(–) Switched-Capacitor Converter
Switched-Capacitor Filters		
LTC1059C	S	2nd Order Universal Filter
LTC1060C	SW	Dual 2nd Order Universal Filter
LTC1061C	SW	Triple 2nd Order Universal Filter
LTC1062C	SW	5th Order Lowpass Filter (Patented)
LTC1063C	SW	Low Offset Clock-Tunable Lowpass Filter
LTC1064C	SW	100kHz Quad 2nd Order Universal Filter
LTC1064-1C	SW	8th Order Cauer Lowpass Filter
LTC1064-2C	SW	8th Order Butterworth Lowpass Filter
LTC1064-3C	SW	8th Order Bessel (Linear Phase) Lowpass Filter
LTC1064-4C	SW	8th Order Cauer/Transitional Lowpass Filter
LTC1064-7C	SW	100kHz Phase Corrected Lowpass Filter
LTC1064-XXC	SW	High Speed, Low Noise Quad Semi-Custom Filter
LTC1065C	SW	Low Offset Clock-Tunable Lowpass Filter
LTC1065I	SW	Low Offset Clock Sweep. Bessel Filter
LTC1066-1C	SW	14-Bit Accurate, 8th Order, LP Filter
LTC1164C	SW	Low Power Quad 2nd Order Universal Filter
LTC1164AC	SW	Quad 20kHz Low Power
LTC1164-5C	SW	Low Power, 8th Order, Butterworth Filter
LTC1164-6C	SW	Low Power, 8th Order, Cauer Filter
LTC1164-7C	SW	Low Power, 8th Order, Linear Phase Filter
LTC1164-8	SW	Ultra-Selective Elliptic Bandpass Filter w/Adjustable Gain
LTC1164-XXC	SW	Low Power, Low Noise Quad Semi-Custom Filter
LTC1264C	SW	High Speed, Quad 2nd Order Universal Filter
LTC1264-7C	SW	High Speed, 8th Order, Linear Phase Filter
References		
LM334	S8	Constant Current Source & Temperature Sensor Reference
LM385	S8-1.2	1.2V Bandgap Voltage Reference
LM385	S8-2.5	2.5V Bandgap Voltage Reference
LM385B	S8-1.2	1.2V Bandgap Voltage Reference
LM385B	S8-2.5	2.5V Bandgap Voltage Reference
LT1004C	S8-1.2	1.2V Bandgap Voltage Reference
LT1004C	S8-2.5	2.5V Bandgap Voltage Reference
LT1004I	S8-1.2	1.2V Bandgap Voltage Reference
LT1004I	S8-2.5	2.5V Bandgap Voltage Reference
LT1009	S8	2.5V Reference
LT1009I	S8	2.5V Reference
LT1019C	S8-2.5	2.5V Precision Reference
LT1019C	S8-4.5	4.5V Precision Reference
LT1019C	S8-5	5V Precision Reference
LT1019C	S8-10	10V Precision Reference

Surface Mount Small Outline (SO), DD and SOT Device Packaging

PRODUCT		DESCRIPTION
LT1021DC	S8-5	5V Precision Reference
LT1021DC	S8-7	7V Precision Reference
LT1021DC	S8-10	10V Precision Reference
LT1027DC	S8-5	5V 5.0ppm Buried Zener Precision Reference
LT1027EC	S8-5	5V 7.5ppm Buried Zener Precision Reference
LT1034C	S8-1.2	Micropower Dual Reference: 1.2V, 7V
LT1034C	S8-2.5	Micropower Dual Reference: 2.5V, 7V
LT1034I	S8-2.5	2.5V Reference, 40ppm/°C Max TC
LT1236AC	S8-5	5V Precision Reference
LT1236AC	S8-10	10V Precison Reference
LT1236AI	S8-10	10V Precison Reference
LT1236BC	S8-5	5V Precision Reference
LT1236BC	S8-10	10V Precison Reference
LT1236BI	S8-5	5V Precision Reference
LT1236BI	S8-10	10V Precision Reference
LT1236CC	S8-5	5V Precision Reference
LT1236CC	S8-10	10V Precision Reference
LT1236CI	S8-5	5V Precision Reference
LT1236CI	S8-10	10V Precision Reference
LT1431C	S8	Programmable Reference
LT1431I	S8	Programmable Reference
Interface Circuits		
LTC485C	S8	Ultralow Power RS485 Transceiver
LTC485I	S8	Ultralow Power RS485 Transceiver
LTC486C	SW	Ultralow Power RS485 Interface Device
LTC486I	SW	Ultralow Power RS485 Interface Device
LTC487C	SW	Ultralow Power RS485 Interface Device
LTC487I	SW	Ultralow Power RS485 Interface Device
LTC488C	SW	Ultralow Power RS485 Quad Receiver
LTC488I	SW	Ultralow Power RS485 Quad Receiver
LTC489C	SW	Ultralow Power RS485 Quad Receiver
LTC489I	SW	Ultralow Power RS485 Quad Receiver
LTC490C	S8	Ultralow Power RS485 Full-Duplex Transceiver
LTC490I	S8	Ultralow Power RS485 Full-Duplex Transceiver
LTC491C	S	Ultralow Power RS485 Full-Duplex Transceiver
LTC491I	S	Ultralow Power RS485 Full-Duplex Transceiver
LT1030C	SW	Quad Low Power Line Driver
LT1032C	SW	Quad Low Power Line Driver with Response Time Control
LT1039C	SW16	3-DX/3-RX RS232 Transceiver with Shutdown
LT1039I	SW16	3-DX/3-RX RS232 Transceiver with Shutdown
LT1039C	SW18	3-DX/3-RX RS232 Transceiver
LT1080C	SW	Dual RS232 Transceiver with 5V to ±9V Pump & Shutdown
LT1080I	SW	Dual RS232 Transceiver with 5V to ±9V Pump
LT1081C	SW	Dual RS232 Transceiver with 5V to ±9V Pump & Shutdown
LT1081I	SW	Dual RS232 Transceiver with 5V to ±9V Pump
LT1130AC	SW	5-DX/5-RX RS232 Transceiver with 5V to ±9V Pump
LT1131AC	SW	5-DX/4-RX RS232 Transceiver with 5V to ±9V Pump & Shutdown
LT1132AC	SW	5-DX/3-RX RS232 Transceiver with 5V to ±9V Pump
LT1133AC	SW	3-DX/5-RX RS232 Transceiver with 5V to ±9V Pump
LT1134AC	SW	4-DX/4-RX RS232 Transceiver with 5V to ±9V Pump
LT1134AI	SW	4-DX/4-RX 5V RS232 Transceiver
LT1135AC	SW	5-DX/3-RX RS232 Transceiver
LT1136AC	SW	4-DX/5-RX RS232 Transceiver with 5V to ±9V Pump & Shutdown
LT1137AC	G, SW	3-DX/5-RX RS232 Transceiver with 5V to ±9V Pump & Shutdown & ±10kV ESD
LT1137AI	SW	3-DX/5-RX RS232 Transceiver with 5V and Shutdown
LT1138AC	G, SW	5-DX/3-RX RS232 Transceiver with 5V to ±9V Pump & Shutdown
LT1139AC	SW	4-DX/4-RX RS232 Transceiver, 5V/12V Powered with Shutdown

PRODUCT		DESCRIPTION
LT1140AC	SW	5-DX/3-RX RS232 Transceiver with Shutdown
LT1141AC	SW	3-DX/5-RX RS232 Transceiver with Shutdown
LT1180AC	SW	±10kV, 5V RS232 DX/RX with Shutdown, 0.1µF
LT1180AI	SW	Dual RS232 Transceiver with 5V to ±9V Pump & Shutdown
LT1181AC	SW	Dual RS232 Transceiver with 5V to ±9V Pump
LT1237C	G, SW	3-DX/5-RX RS232 Transceiver with 5V to ±9V Pump, Single RX Keep-Alive & Shutdown
LT1280AC	SW	Dual RS232 Transceiver with 5V to ±9V Pump & Shutdown
LT1281AC	SW	Dual RS232 Transceiver with 5V to ±9V Pump
LT1281I	SW	Low Power Dual RS232 Transceiver with 5V to ±9V Pump
LTC1318C	SW	Single 5V AppleTalk® DCE Transceiver
LT1319C	S	Infrared Receiver, Dual Channel
LTC1320C	S	AppleTalk Transceiver
LTC1321C	S	Programmable EIA/TIA562/RS232 and RS485 Transceiver
LTC1321I	S	Programmable EIA/TIA562/RS232 and RS485 Transceiver
LTC1322C	S	Programmable EIA/TIA562/RS232 and RS485 Transceiver
LTC1322I	S	Programmable EIA/TIA562/RS232 and RS485 Transceiver
LTC1323C	G, SW	Single 5V AppleTalk Transceiver
LTC1324C	SW	5V Powered Apple/LocalTalk® Transceiver
LTC1327C	G, SW	3V Low Power EIA562 3-DX/5-RX Transceiver
LT1330C	G, S	5V RS232 Transceiver with 3V Logic Interface and 1 RX Active in Shutdown
LT1331C	G, SW	3-DX/5-RX RS232 Transceiver with 3V-Only Supply
LT1332C	G, SW	3-DX/5-RX RS232 Transceiver with Low Power
LTC1334C	SW	5V Powered Programmable EIA/TIA232/485 Transceiver
LTC1334I	SW	5V Powered Programmable EIA/TIA232/485 Transceiver
LTC1335C	SW	Programmable EIA/TIA562 and RS485 Transceiver
LTC1335I	SW	Programmable EIA/TIA562 and RS485 Transceiver
LTC1337C	G, SW	3-DX/5-RX RS232 Transceiver with µPower
LTC1338C	G, SW	5V Low Power RS232 Transceiver with µPower
LTC1338I	G, SW	5V Low Power RS232 Transceiver with µPower
LT1341C	G, SW	3-DX/5-RX RS232 Transceiver with Shutdown and DX Disable
LT1342C	G, SW	3-DX/5-RX RS232 Transceiver with 3V & 5V Logic Supplies
LTC1345C	SW	Single Supply V.25 Transceiver
LTC1345I	SW	Single Supply V.35 Transceiver
LTC1346C	SW	±5V powered V.35 Transceiver
LTC1346I	SW	±5V powered V.35 Transceiver
LTC1347C	G, SW	5V Low Power RS232 3-DX/5-RX Transceiver with 5 RX Active in Shutdown
LTC1348C	G, SW	3.3V Low Power RS232 3-DX/5-RX Transceiver
LTC1349C	G, SW	5V Low Power RS232 3-DX/5-RX Transceiver with 2 RX Active in Shutdown
LTC1349I	G, SW	5V Low Power RS232 3-DX/5-RX Transceiver with 2 RX Active in Shutdown
LTC1350C	G, SW	3.3V Low Power EIA/TIA562 3-DX/5-RX Transceiver
LTC1350I	G, SW	3.3V Low Power EIA/TIA562 3-DX/5-RX Transceiver
LT1381C	S	Dual RS232 Transceiver with Narrow 16-Lead SOIC
LT1381I	S	Dual RS232 Transceiver with Narrow 16-Lead SOIC
LTC1382C	SW	5V Low Power RS232 Transceiver
LTC1383C	S	5V Low Power RS232 Transceiver
LTC1384C	G, SW	5V Low Power RS232 Transceiver with 3 RX Active in Shutdown
LTC1385C	G, SW	3V Low Power EIA/TIA562 Transceiver with 2 RX Active in Shutdown
LTC1386C	S	RS232 2-DX/2-RX in Narrow SOIC
LTC1480C	S8	3V powered RS485 Transceiver
LTC1480I	S8	3V powered RS485 Transceiver
LTC1481C	S8	Ultralow Power RS485 Transceiver with Shutdown
LTC1482C	S8	Low Power RS485 Transceiver with Carrier Detect
LTC1482I	S8	Low Power RS485 Transceiver with Carrier Detect

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Surface Mount Small Outline (SO), DD and SOT Device Packaging

PRODUCT		DESCRIPTION
LTC1483C	S8	Low EMI Ultralow Power RS485 Transceiver with Shutdown
LTC1483I	S8	Low EMI Ultralow Power RS485 Transceiver with Shutdown
LTC1484C	S8	Low Power RS485 Transceiver w/Fail-Safe Receiver Input
LTC1484I	S8	Low Power RS485 Transceiver w/Fail-Safe Receiver Input
LTC1485C	S8	10Mbit/s Low Power RS485 Half-Duplex Transceiver
LTC1485I	S8	High Speed RS485 DX/RX
LTC1487C	S8	High Input Impedance Ultralow Power RS485 Transceiver with Shutdown
LTC1487I	S8	High Input Impedance Ultralow Power RS485 Transceiver with Shutdown
LT1537C	G, SW	±15kV ESD Protected RS232 3-DX/5-RX
LT1537I	G, SW	±15kV ESD Protected RS232 3-DX/5-RX
Analog Switches		
LTC201AC	S	Micropower, Low Charge Injection, Quad CMOS Analog Switch
LTC202C	S	Micropower, Low Charge Injection, Quad CMOS Analog Switch
LTC203C	S	Micropower, Low Charge Injection, Quad CMOS Analog Switch
LTC221C	S	Micropower, Low Charge Injection, Quad CMOS Analog Switch with Data Latches
LTC222C	S	Micropower, Low Charge Injection, Quad CMOS Analog Switch with Data Latches
High Side Switches and Drivers		
LTC1153C	S8	Electronic Circuit Breaker
LTC1154C	S8	Single High Side MOSFET Switch Driver
LTC1155C	S8	Dual High Side MOSFET Switch Driver
LTC1155I	S8	Dual High Side MOSFET Switch Driver
LTC1156C	SW	Quad High Side MOSFET Switch Driver
LTC1157C	S8	Dual 3.3V Supply High-Side MOSFET Switch Driver
LT1158C	SW	Half-Bridge N-Channel Power MOSFET Driver
LT1158I	SW	Half-Bridge N-Channel Power MOSFET Driver
LT1161C	SW	Quad High Side MOSFET Driver
LT1161I	SW	Quad High Voltage, High Side N-Channel MOSFET Driver
LTC1163C	S8	Triple 1.8V Supply High-Side MOSFET Switch
LTC1165C	S8	Triple 1.8V Supply High-Side MOSFET Switch
LTC1177C	S, S-5 S-12	High Side Switch Driver
LTC1255C	S8	Dual 24V High Side Switch Driver
LTC1255I	S8	Dual 24V High Side Switch Driver
LTC1477C	S8	High Side Switches and Drivers
LTC1478C	S8	High Side Switches and Drivers

PRODUCT		DESCRIPTION
Watchdog Timer/Microprocessor Supervisory		
LTC690C	S8	Microprocessor Supervisory Circuit
LTC690I	S8	Microprocessor Supervisory Circuit
LTC691C	SW	Microprocessor Supervisory Circuit
LTC691I	SW	Microprocessor Supervisory Circuit
LTC692C	S8	Microprocessor Supervisory Circuit
LTC692I	S8	Microprocessor Supervisory Circuit
LTC693C	SW	Microprocessor Supervisory Circuit
LTC693I	SW	Microprocessor Supervisory Circuit
LTC694C	S8	Microprocessor Supervisory Circuit
LTC694C	S8-3.3	3.3V Microprocessor Supervisory Circuit
LTC694I	S8	Microprocessor Supervisory Circuit
LTC694I	S8-3.3	3.3V Microprocessor Supervisory Circuit
LTC695C	SW	Microprocessor Supervisory Circuit
LTC695C	S-3.3	3.3V Microprocessor Supervisory Circuit
LTC695I	SW	Microprocessor Supervisory Circuit
LTC695I	S-3.3	3.3V Microprocessor Supervisory Circuit
LTC699C	S8	Microprocessor Supervisory Circuit
LTC699I	S8	Microprocessor Supervisory Circuit
LTC1232C	S8	Microprocessor Supervisory Circuit
LTC1232I	S8	Microprocessor Supervisory Circuit
LTC1235C	SW	Microprocessor Supervisory Circuit
LTC1235I	SW	Microprocessor Supervisory Circuit
Video Mulitplexers		
LT1203	S8	150MHz, 2:1 Video Multiplexer
LT1204	SW	4-Input Video Multiplexer with 75MHz CFA
LT1205	S	Dual 150MHz, 2:1 or 4:1 Video Multiplexer
PCMCIA Power Management		
LT1106C	F	µPower DC/DC Converter for PCMCIA Flash Memory Cards
LT1312C	S8	Single PCMCIA VPP Regulator
LT1313C	S	Dual PCMCIA VPP Regulator
LTC1314C	G, S	Single PCMCIA VPP Switch/V_{CC} Driver
LTC1315C	G, S	Dual PCMCIA VPP Switch/V_{CC} Driver
LTC1470C	S8	Single Protected 1A PCMCIA V_{CC} Switch
LTC1471C	S	Dual Protected 1A PCMCIA V_{CC} Switch
LTC1472C	S	Single Protected PCMCIA VPP and V_{CC} Switch

TAPE AND REEL SPECIFICATIONS—SURFACE MOUNT

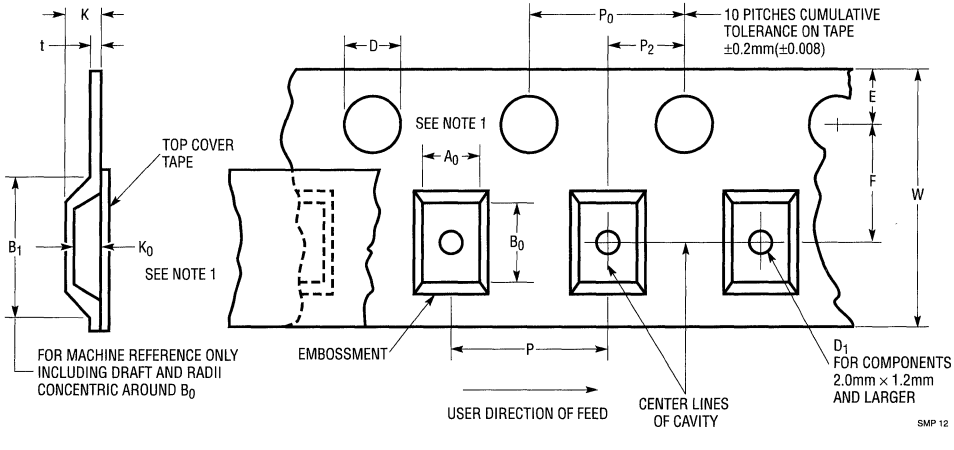
Tape and Reel Packing

Tape and reel packing is available for all SO, SOT-223, SSOP, TSSOP and DD packages in accordance with EIA Specification 481-A. Table 1 lists the applicable tape widths, dimensions and quantities for all LTC small outline products. Consult factory for tape and reel pricing and minimum order requirements.

Table 1. Tape and Reel Specifications

LTC Package Code Designator	LTC Package Style	Number of Leads Offered	W Tape Width	P Component Pitch	P_0 Hole Pitch	Reel Diameter	Units per Reel
F	TSSOP (0.173)	20	16mm	8mm	4mm	13"	2,500
G	SSOP (0.209)	16	16mm	12mm	4mm	13"	2,000
G	SSOP (0.209)	20, 24	16mm	12mm	4mm	13"	1,800
G	SSOP (0.209)	28	24mm	12mm	4mm	13"	2,000
GN	SSOP (0.150)	16	12mm	8mm	4mm	13"	2,500
GN	SSOP (0.150)	20, 24	16mm	8mm	4mm	13"	2,500
GW	SSOP (0.300)	36, 44	24mm	12mm	4mm	13"	1,000
M, Q, R	DD	3, 5 or 7	24mm	16mm	4mm	13"	750
S8	S8 (0.150)	8	12mm	8mm	4mm	13"	2,500
S	S (0.150)	14	16mm	8mm	4mm	13"	2,500
S	S (0.150)	16	16mm	8mm	4mm	13"	2,500
ST	SOT-223	3	16mm	12mm	4mm	13"	2,000
SW	SW (0.300)	16	16mm	12mm	4mm	13"	1,000
SW	SW (0.300)	18	24mm	12mm	4mm	13"	1,000
SW	SW (0.300)	20	24mm	12mm	4mm	13"	1,000
SW	SW (0.300)	24	24mm	12mm	4mm	13"	1,000
SW	SW (0.300)	28	24mm	12mm	4mm	13"	1,000

Embossed Carrier Dimensions (12mm, 16mm, 24mm Tape Only)



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TAPE AND REEL SPECIFICATIONS—SURFACE MOUNT

Embossed Tape — Constant Dimensions

Tape Size	D	E	P_0	t(Max.)	A_0 B_0 K_0
12mm 16mm 24mm	1.5 $^{+0.10}_{-0.0}$ (0.059) $^{+0.004}_{-0.0}$	1.75 ± 0.10 (0.069 ± 0.004)	4.0 ± 0.10 (0.157 ± 0.004)	0.600 (0.024)	See Note 1

Embossed Tape Variable Dimensions

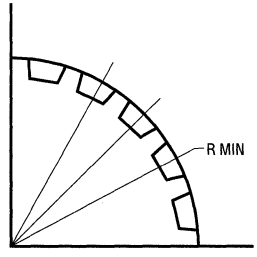
Tape Size	B_1 Max.	D_1 Min.	F	K Max.	P_2	R Min.	W
12mm	8.2 (0.323)	1.5 (0.059)	5.5 ± 0.05 (0.217 ± 0.002)	6.5 (0.256)	2.0 ± 0.05 (0.079 ± 0.002)	30 (1.181)	12.0 ± 0.30 (0.472 ± 0.012)
16mm	12.1 (0.476)		7.5 ± 0.10 (0.295 ± 0.004)		2.0 ± 0.10 (0.079 ± 0.004)	40 (1.575)	16 ± 0.30 (0.630 ± 0.012)
24mm	20.1 (0.791)		11.5 ± 0.10 (0.453 ± 0.004)			50 (1.969)	24 ± 0.30 (0.945 ± 0.012)

Note 1: A_0 B_0 K_0 are determined by component size. The clearance between the component and the cavity must be within 0.05 (0.002) min. to 0.65 (0.026) max. for 12mm tape, 0.05 (0.002) min. to 0.90 (0.035) max. for 16mm tape and 0.050 (0.002) min. to 1.00 (0.039) max. for 24mm tape and larger. The component cannot rotate more than 10° within the determined cavity.

Note 2: Tape and components shall pass around radius "R" without damage.

Note 3: Dimensions are in millimeters (inches) unless otherwise noted.

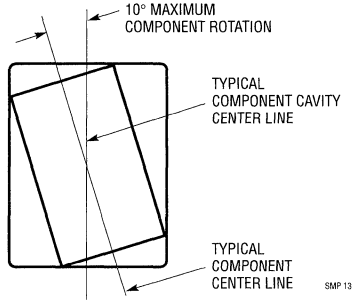
Bending Radius



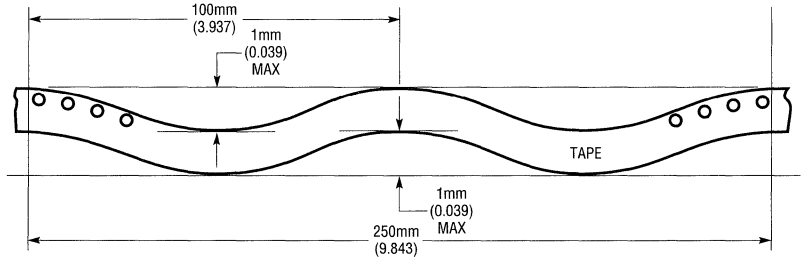
SMP 14

TAPE AND REEL SPECIFICATIONS—SURFACE MOUNT

Component Rotation



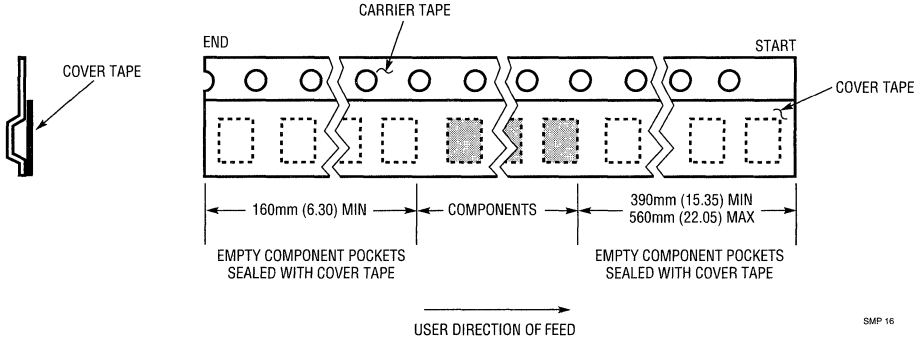
Tape Camber (Top View)



ALLOWABLE CAMBER TO BE 1mm/100mm NONACCUMULATIVE OVER 250mm

SMP 15

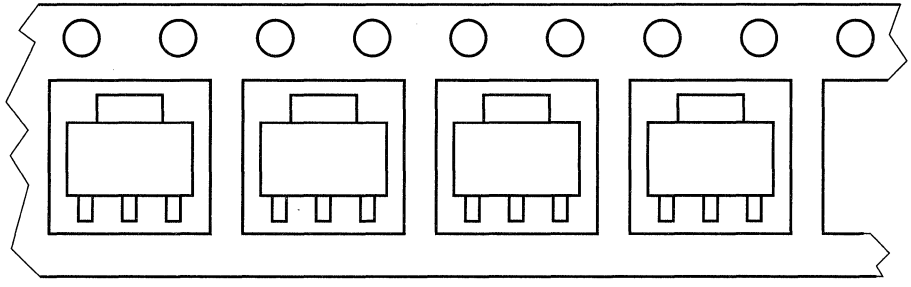
Tape Leader (Start/End) Specification



SMP 16

TAPE AND REEL SPECIFICATIONS—SURFACE MOUNT

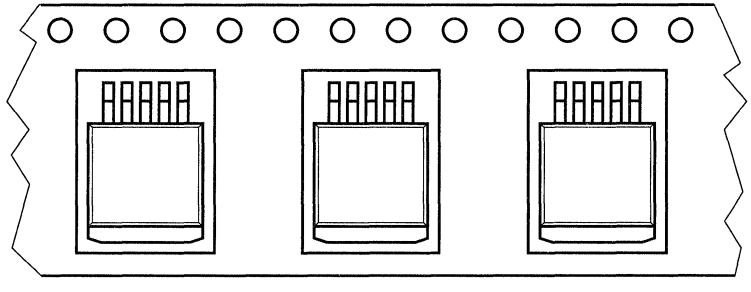
ST
SOT-223 Devices



USER DIRECTION OF FEED

SMP 17

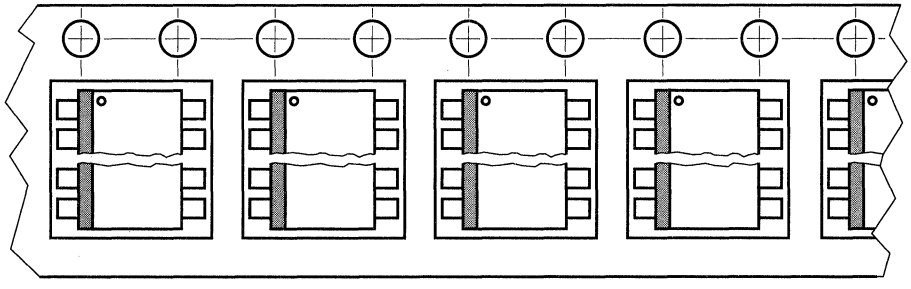
M, Q, R
DD Pak Devices



USER DIRECTION OF FEED

SMP 18

F, G, GN, GW, S8, S, SW
SSOP, TSSOP Devices

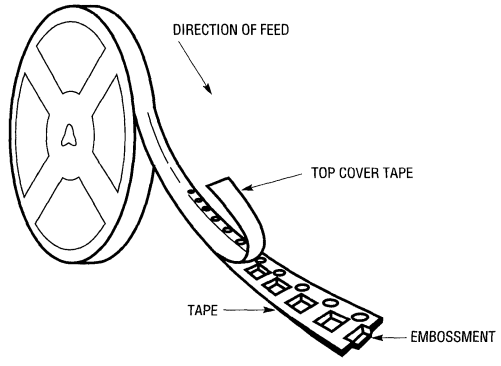


USER DIRECTION OF FEED

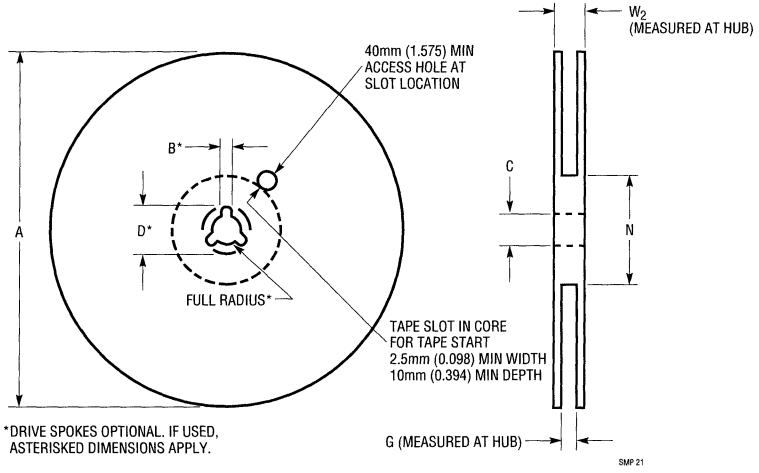
SMP 19

REEL DIMENSIONS—SURFACE MOUNT

Direction of Feed



Reel Dimensions



TAPE SIZE	A MAX	B MIN	C	D* MIN	N MIN	G MAX	W_2 MAX
12mm	330 (12.992)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$12.4^{+2.0}_{-0.0}$ $\left(0.488^{+0.078}_{-0.00}\right)$	18.4 (0.724)
16mm	330 (12.992)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$16.4^{+2.0}_{-0.00}$ $\left(0.646^{+0.078}_{-0.00}\right)$	22.4 (0.882)
24mm	330 (12.992)	1.5 (0.059)	13.0 ± 0.20 (0.512 ± 0.008)	20.2 (0.795)	50 (1.969)	$24.4^{+2.0}_{-0.00}$ $\left(0.961^{+0.078}_{-0.00}\right)$	30.4 (1.197)

Metric dimensions will govern.

Note 1: All dimensions in millimeters (inches) unless otherwise noted.
Note 2: English measurements rounded and for reference only.

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TAPE AND REEL SPECIFICATIONS—TO-92

TO-92 Tape Dimension

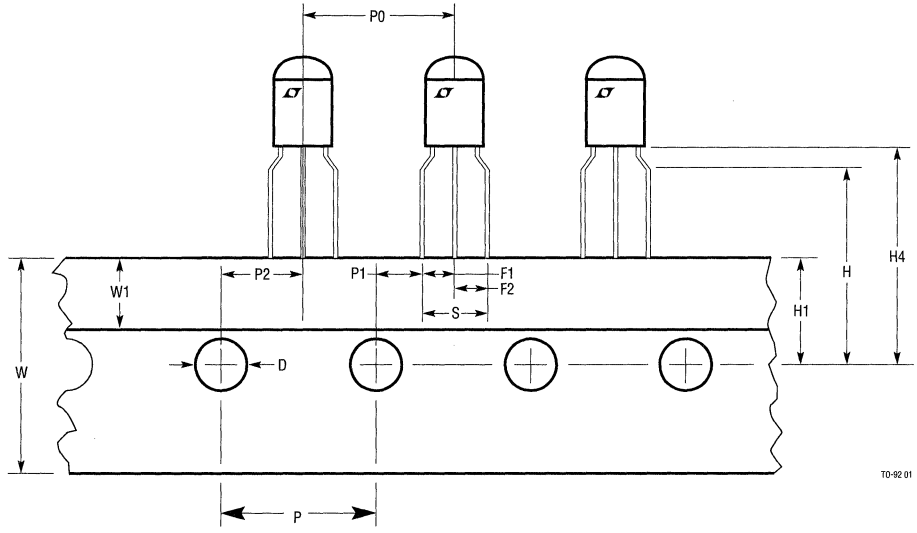
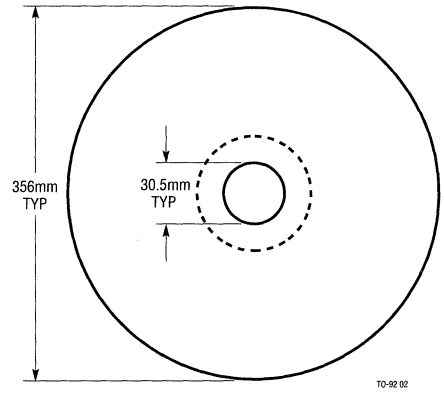


Table 1

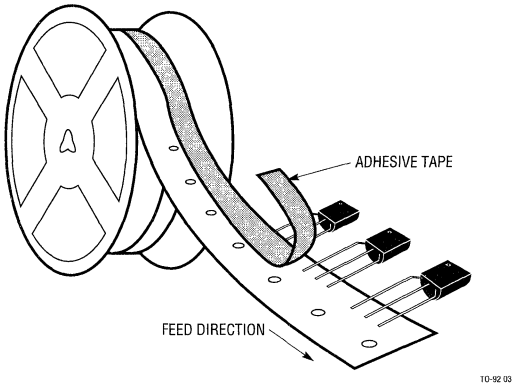
SYMBOL	DESCRIPTION	DIMENSION (mm)
D	Sprocket Hole Diameter	4 ± 0.2
H	Length from Seating Plane	16 ± 0.5
H1	Sprocket Hole Location	9 ± 0.5
H4	Component Base Height	20 Max
P	Sprocket Hole Pitch	12.7 ± 0.2
P0	Pitch of Component	12.7 ± 0.5
P1	Lead Location	3.85 ± 0.5
P2	Center of Seating Plane Location	6.35 ± 0.4
S	Component Lead Spacing	5 +8, −0.2
W	Carrier Tape Width	18 +1, −0.5
W1	Adhesive Tape Width	6.0 ± 1.0
F1, F2	Lead-to-Lead Distance	2.5 +0.4, −0.1

TO-92 Reel Dimensions

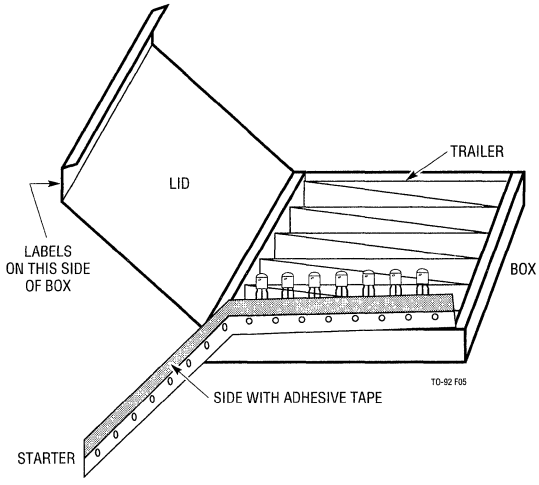


TAPE AND REEL SPECIFICATIONS—TO-92

Tape Orientation on Reel

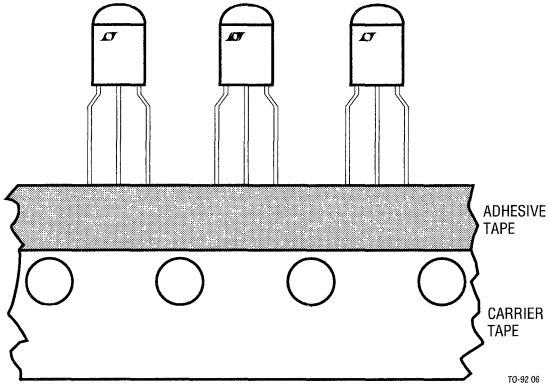


Ammo Pak Tape Orientation Inside Box

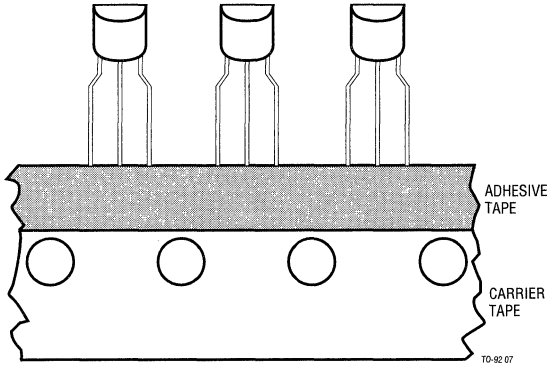


Package Orientation on Tape

STYLE E: Standard
(Flat Side of Package Faces Toward the Adhesive Tape)



STYLE A: Special Lot
(Rounded Side of Package Faces Toward the Adhesive Tape)



14

Introduction

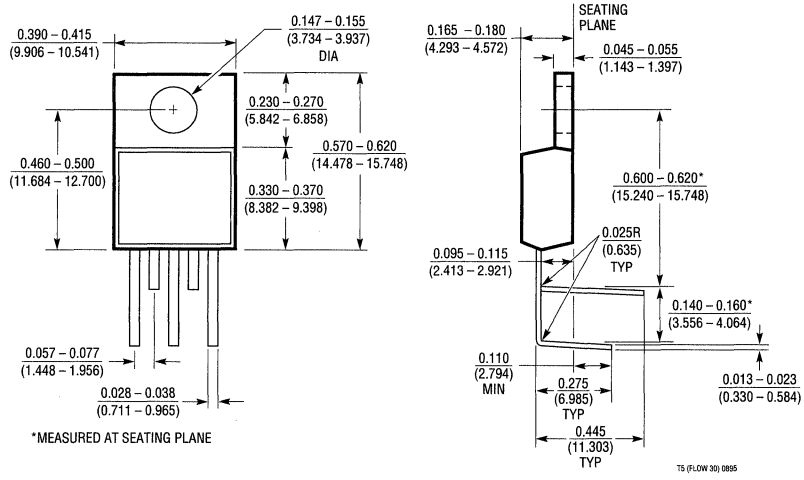
On the following pages are a variety of lead bend options available for TO-220 packages from Linear Technology Corporation. The special adders, flows, and minimums that have been established for these lead bend options are:

Flows 30 to 37 Special Lead Bends for TO-220
(Minimum Order: 1,000 units)

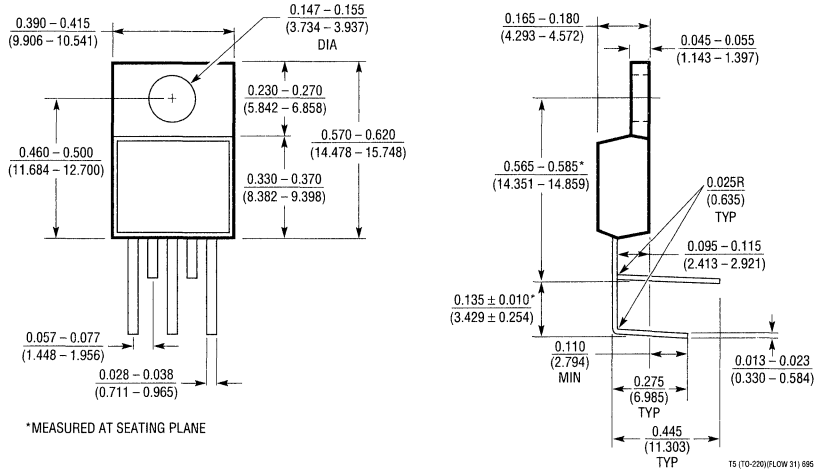
1,000 to 4,999 units	Special lead bends subject to additional charges and order conditions. Contact LTC, Sales/Marketing for more information.
5,000 to 9,999 units	
10,000 to 24,999 units	
> 25,000 units	

It is important to remember orders for these nonstandard flows require a minimum 90-day notification for cancellation or rescheduling. Also note that special flow orders for U.S. distribution must be approved in advance.

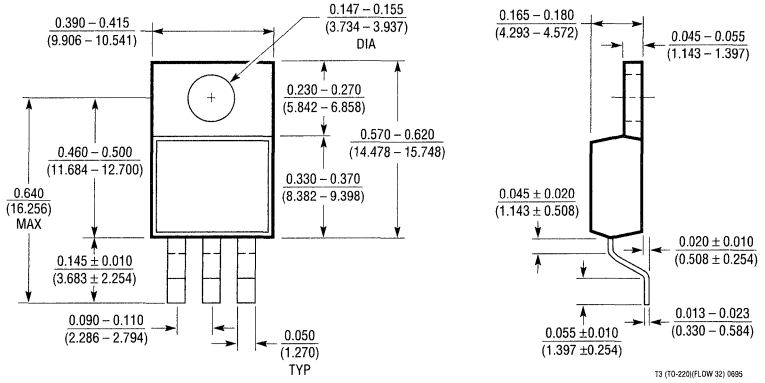
TO-220 5-Lead Package Outline (Flow 30)



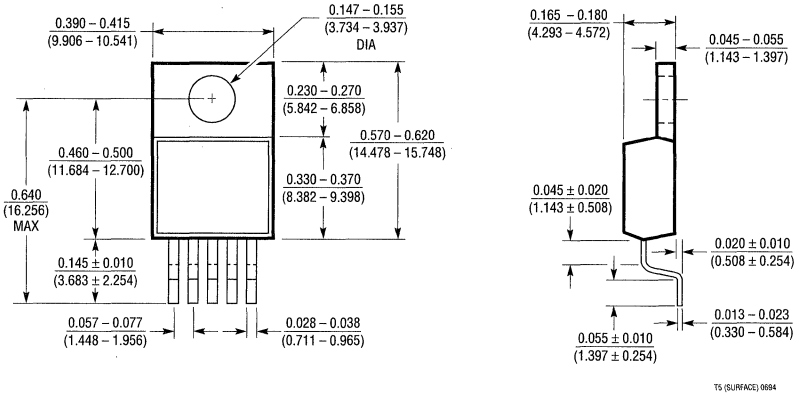
TO-220 5-Lead Package Outline (Flow 31)



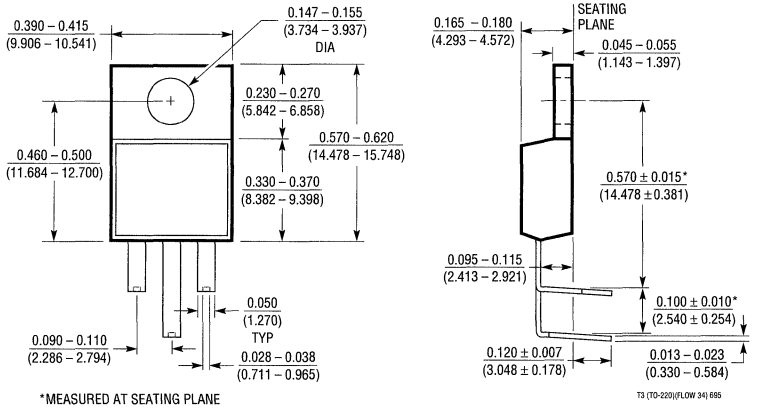
TO-220 3-Lead Package Outline (Flow 32)



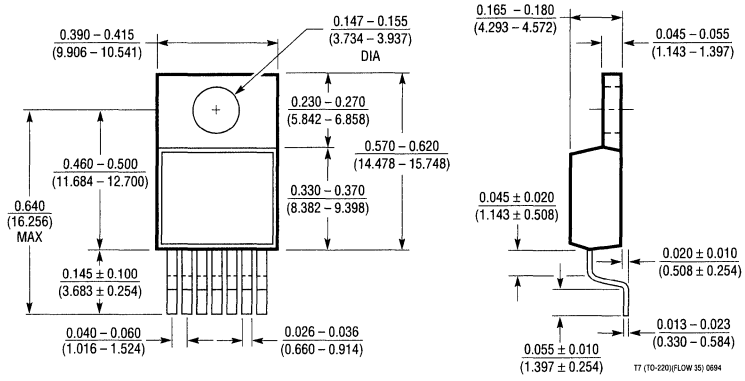
TO-220 5-Lead Package Outline (Flow 33)



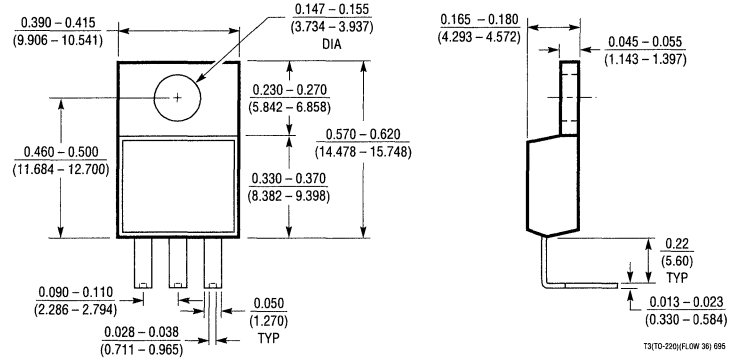
TO-220 3-Lead Package Outline (Flow 34)



TO-220 7-Lead Package Outline (Flow 35)

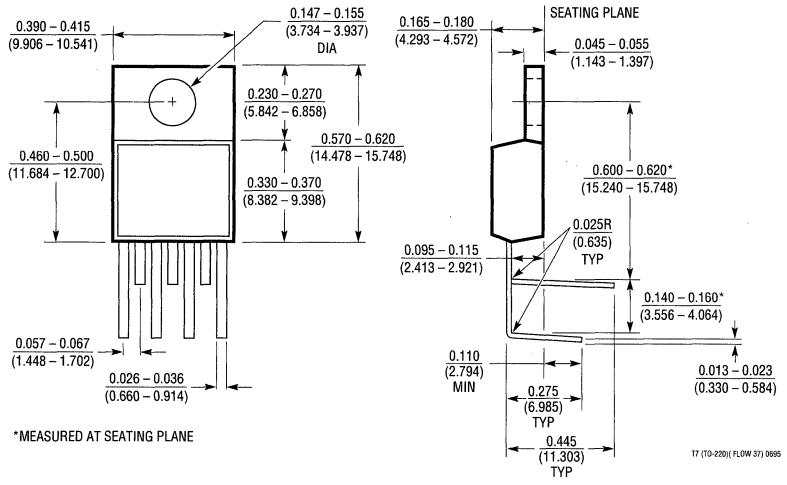


TO-220 3-Lead Package Outline (Flow 36)



14

T7 7-Lead Package Outline (Flow 37)



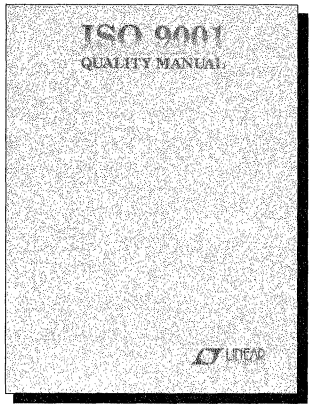
SECTION 15—APPENDICES

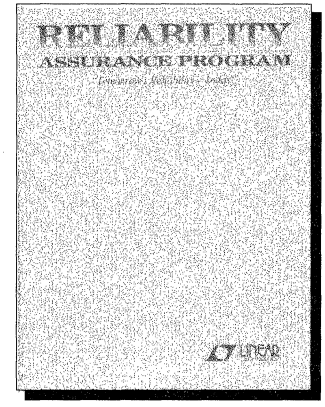
SECTION 15—APPENDICES

Quality and Reliability Assurance Programs

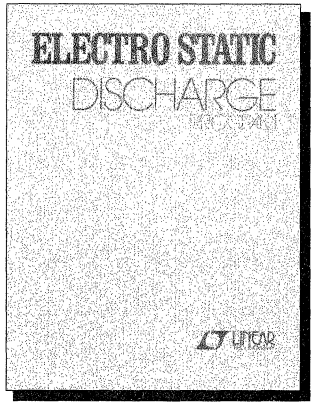
Linear Technology Corporation (LTC) has a wide-ranging program integrating vendor participation, design engineering, and manufacturing to produce the most reliable and highest quality linear integrated circuits available on the market. Our modern manufacturing facility in Milpitas, California is DESC Class S and Class B line certified; MIL-I-38535 QML transitional certified, and ISO 9001 certified. We have successfully completed over 90 major OEM quality system surveys to MIL-Q-9858 and MIL-I-45208 including achieving several major customer quality awards. Our Quality and Reliability Assurance Programs are summarized below:

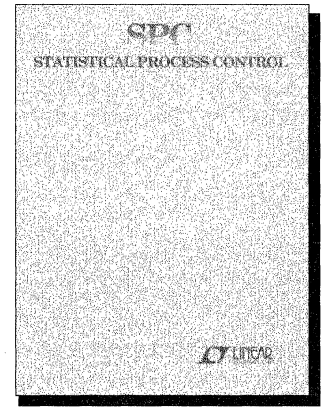
- **Wafer Fabrication** — A modern class 100 area modular clean room construction with full environmental monitors. Emphasis is placed on statistical process control, CV plots, SEM monitors and on our proprietary dual layer passivation system.
- **SPC (Statistical Process Control)** — LTC is committed to SPC as the cornerstone of our continuous quality improvement and Total Quality Management System (TQMS) programs. SPC is fully implemented in all manufacturing areas.
- **Assembly and End of Line** — Incoming inspection of all materials and piece-parts, line surveillance and process control monitors.
- **Testing** — Incoming inspection and acceptance of all offshore lots prior to release to test. LTX and Eagle testers, multipass testing with closed-loop binning to reduce outgoing electrical defective levels. Many "beyond data sheet" tests and full temperature QA lot buy-offs are performed as standard processing.
- **Traceability** — A backside or side mark is placed on all units, where space permits, to give information on each unit to identify the wafer fab lot, assembly, end of line (e.o.l.) and test lots. The information provided exceeds the seal week traceability control required by MIL-STD-883.
- **ESD (Electrostatic Discharge)** — A full program is in place from design through manufacturing. Products are fully characterized to MIL-STD-883 (Method 3015) and strict controls on handling and packaging are observed.
- **Training and Certification** — Operator training has been established for all operations and recertification is performed every 6 months.
- **Major Change Control** — Major change controls are in place to notify our customers in accordance with MIL-I-38535, LTC internal specifications, or specific customer specifications as required.
- **Quality Assurance** — Full monitoring and reporting of quality data with emphasis on Statistical Process Control (SPC) charts and continuous quality improvement. Refer to our section on Quality Assurance Program.
- **Failure Analysis and Reporting** — A full analytical lab and formal program exists to record, analyze and take appropriate corrective action on all returns. A report is generated and sent to the customer stating our findings and action.
- **Reliability Flows** — LTC reliability flows include Class S and Class B JAN-38510, Standard Military Drawings (SMD), DESC Drawings, 883, R-Flow, LTC proprietary Hi-Rel Radiation Hardered (RH) products, and Hi-Rel (Source Controlled Drawings). In addition, specialized processing such as SEM, PIND and other tests can be performed as required.
- **Reliability Monitor** — LTC has a unique reliability structure built into each wafer that is used to obtain rapid feedback on reliability. This data is obtained in less than one week, versus 40 weeks for a typical reliability audit. See the LTC Reliability Assurance Program for more details. LTC has a comprehensive Quick Reaction Reliability (QR^2) monitor program for plastic packaged devices. A variety of tests are performed on every one-week date code, for every package type and lead count and real time feedback to the assembly facilities.
- **Reliability Reporting** — Data is gathered on a monthly basis for selected process technology/product family/package combinations. This data is summarized each quarter and published in a Reliability Data Pack showing Operating Life, 85/85, HAST, Autoclave, Temperature Cycle, Thermal Shock, 883 Group C, and 883 Group D summary data. Copies of Reliability Data Pack summaries are available by writing or calling Linear Technology Corporation, 1630 McCarthy Blvd., Milpitas, CA 95035. 1-800-4-LINEAR (1-800-454-6327).


ISO 9001
QUALITY MANUAL
LINEAR


RELIABILITY
ASSURANCE PROGRAM
LINEAR


TÜV
CERT
CERTIFICATE
DAR
The TÜV-Zertifizierungsgemeinschaft e.V.
hereby certifies that
Linear Technology Corporation
Milpitas, CA
has established and applies
a quality system for
Design and manufacturing of a broad line of
high performance linear integrated circuits
An audit was performed, Report No. 5098
Proof has been furnished that the requirements according to
DIN ISO 9001 / EN 29001
are fulfilled
The certificate is valid until
March 31, 1999
Certificate Registration No.
09 100 2098
TÜV Rheinland
Gruppe


ELECTRO STATIC
DISCHARGE
LINEAR


SPC
STATISTICAL PROCESS CONTROL
LINEAR

TÜV CERT

CERTIFICATE

DAR

The TÜV-Zertifizierungsgemeinschaft e.V.
hereby certifies that

Linear Technology Corporation

Milpitas, CA

has established and applies
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Design and manufacturing of a broad line of high performance linear integrated circuits

An audit was performed, Report No. **3098**
Proof has been furnished that the requirements according to

DIN ISO 9001 / EN 29001

are fulfilled.

The certificate is valid until
March 31, 1996
Certificate Registration No.
09 100 3098

Bonn, 07.06.1993

TÜV CERT Executive Board

TÜV Rheinland Gruppe

Cologne, 07.06.1993

Certifying Body

15

QUALITY, RELIABILITY, AND SERVICE POLICY STATEMENT

The cornerstone of Linear Technology's Quality, Reliability, & Service (QRS) Program is to achieve 100% customer satisfaction by producing the most technically advanced product with the best quality, on-time delivery, and service. Top management is fully committed to this goal, but to achieve this goal requires the involvement and dedication of every employee.

Since 1983 when the first product was shipped, Linear Technology has achieved numerous accomplishments in the area of quality and service, among which are:

- 1st company in the industry to achieve the Department Of Defense line certification for MIL-M-38510 Class B products during its first audit in 1984.
- Among the first group of manufacturers to be certified in the Ship-To-Stock Program at Compaq Computers in 1986.
- 1st company in Silicon Valley to achieve the Ford Q1 Award for Excellence in Quality in 1988.

The above achievements were made possible by the commitment and dedication of employees who pay attention to details and whose motto is *"Do the job right the first time"* .

Customer requirements and expectations in the areas of Quality and Service are becoming increasingly more demanding. Linear Technology not only intends to *meet* those requirements and expectations for survival, but also to *exceed* them to maintain a *world-class leadership* position.

The standard will be error-free products and error-free performance. This standard commits all of Linear Technology's employees to a QRS Policy that takes precedence over all other considerations and leaves no room for error or failures. LTC's goal is zero defects.

Robert Swanson
President and Chief Executive Officer

Clive Davies
Vice President and Chief Operating Officer

Paul Chantalat
Vice President of Quality and Reliability

QUALITY SYSTEM FOR DESIGN, DEVELOPMENT, PRODUCTION, AND SERVICING

0 INTRODUCTION

This policy defines the organization and policies of Linear Technology Corporation (LTC) and assures conformance to requirements during design, development, production, testing, inspection and shipment of products. It sets out the general quality policies, procedures and practices of LTC.

1.0 SCOPE

The requirements specified in this Quality Manual are designed to prevent and detect any nonconformances during design, development, production, testing and inspection.

2.0 FIELD OF APPLICATION

The Quality Program specified herein is designed to ensure 100% customer satisfaction by ensuring product conformance to achieve and maintain the highest level of product quality and reliability and to ensure a program for continuous improvement. This manual applies to all manufacturing locations and to all military and commercial products manufactured by LTC.

REFERENCES

ISO 8402	Quality Vocabulary
ISO 9000	Quality Management and Quality Assurance Standards: Guidelines for Selection and Use
ISO 9001	Quality Systems: Models for Quality Assurance in Design/Development, Production, Installation and Servicing
ISO 9002	Quality Systems: Model for Quality Assurance in Production and Installation.
ISO 9004	Quality Management and Quality System Elements Guidelines
ISO 10011-1	Guidelines for Auditing Quality Systems, Part 1
ISO 10011-2	Guidelines for Auditing Quality Systems, Part 2
ISO 10013-3	Guidelines for Auditing Quality Systems, Part 3
ISO 10012-1	Quality Assurance Requirements for Measuring

3.0 DEFINITIONS

For the purpose of this quality manual, the definitions given in ISO 8402 shall apply.

Below is a list of acronyms used by LTC:

CMR	Customer Material Return
CSI	Customer Source Inspection
DI	De-Ionized
DMR	Discrepant Material Report
DRC	Design Rules Check
ECN	Engineering Change Notice
EOL	End-of-Line
F/A	Failure Analysis
GAUGE R&R	Gauge Repeatability and Reproducibility
GSI	Government Source Inspection
IFR	Inspection Failure Report
IQC	Incoming Quality Control
MPS	Material Procurement Specifications
MRB	Material Review Board
MSE	Measurement System Evaluation
OCAP	Out-of-Control Action Plan
PO	Purchase Order
PAT	Process (or Preventive) Action Team
PG	Pattern Generation
QA	Quality Assurance
QAP	Quality Assurance Policy
QAR	Quality Audit Report
QCT	Quality Control Teams
RMA	Return Material Authorization
RPL	Released Product Listing
SL	Special Lot
SOP	Standard Operating Procedure
SPC	Statistical Process Control
SSS	Stop/Start Sheet
TECN	Temporary Engineering Change Notice
TML	Top Mark Layout
TQMS	Total Quality Management System
VCAR	Vendor Corrective Action Request

4.0 QUALITY SYSTEM REQUIREMENT

LTC's Total Quality Management System (TQMS) encompasses the concept of strategic quality planning and management to ensure a program of continuous quality and reliability improvement.

The quality system is designed to meet the requirements of:

- ISO 9001
- MIL-STD-883
- MIL-STD-976
- MIL-M-38510 (Class B and Class S)
- MIL-I-38535, Appendix A
- MIL-I-45208
- MIL-STD-45662
- MIL-Q-9858
- ANSI/NCSL Z540-1-1994
- Our commercial customers
- Our goal of defect-free products

LTC pledges that its products shall be manufactured in accordance with the applicable specifications or to specific customer requirements.

4.1 MANAGEMENT RESPONSIBILITY

LTC's management with executive responsibility shall ensure that the Quality policy is understood, implemented, and maintained at all levels in the organization.

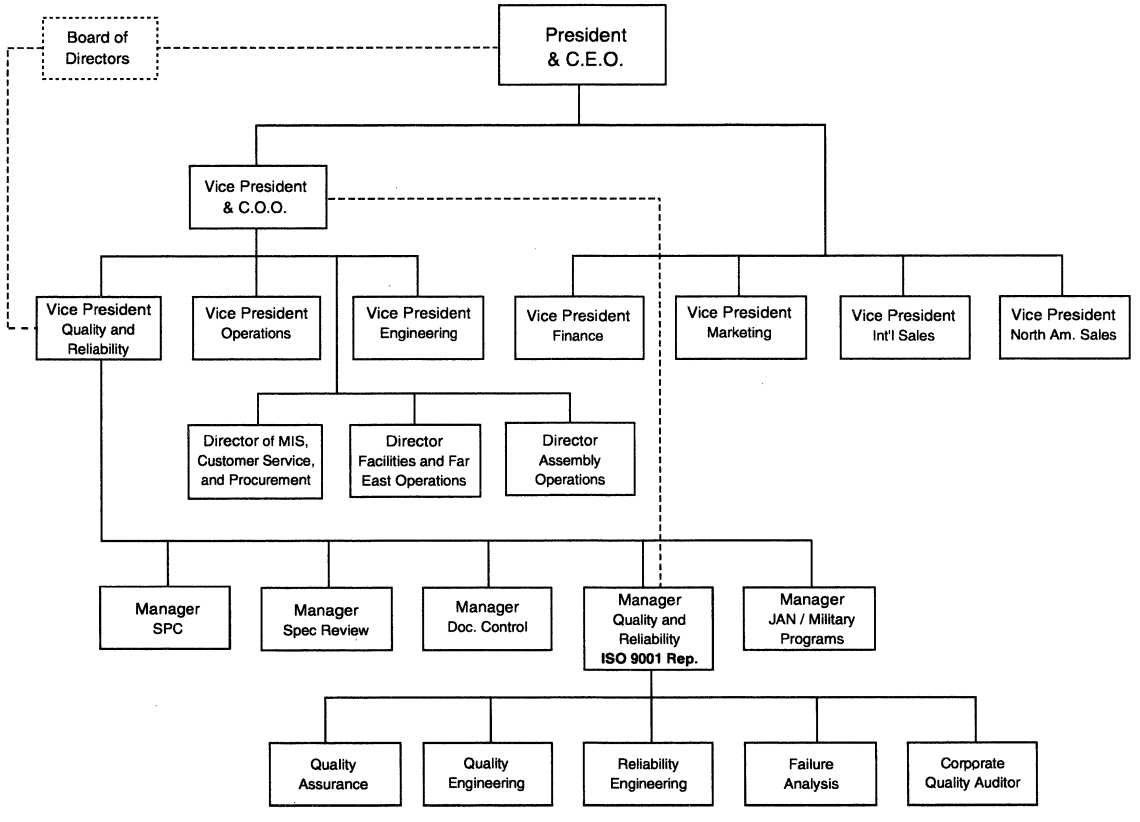
4.1.1 Quality Policy

See Policy Statement in the front of this manual.

4.1.2 Organizational Chart

A current organizational chart showing senior management and the organizational reporting structure is available upon request from the secretary of the Vice President of Finance.

LTC Organizational Chart



4.1.2.1 Responsibility and Authority

A) All employees in this organization have the authority to initiate action to prevent the occurrence of product, process, and quality system nonconformity by notifying the appropriate support or management personnel.

B) Inspectors have the responsibility to identify and record product and process problems via a Stop/Start or Inspection Failure Report.

C) Any employee in the organization has the organizational freedom and authority to initiate, recommend, or provide solutions relating to product, process and quality system nonconformances.

D) Engineering, Quality Assurance and management have the responsibility to verify the implementation of solutions.

E) Any employee in the factory that is running a process at an SPC location has the responsibility to suspend an operation in the event of an out-of-control process or to control further processing in accordance with the associated Out-of-Control Action Plan (OCAP) by issuing a Stop/Start.

Quality Assurance, Engineering, Production Control and Customer Service have the responsibility to suspend or control the further processing and delivery of nonconforming product until the deficiency or unsatisfactory condition has been corrected. This can be done via the issuance of a Stop/Start or Inspection Failure Report (IFR) via an ECN/TECN to a specification or via a ship-hold.

4.1.2.2 Verification Resources and Personnel

All verification activities and requirements shall be documented in the appropriate standard operating procedures (SOP) or detailed specifications to include inspection, test, and monitoring of the design, production, and product. Design reviews and audits of the quality system, processes, and/or product shall be carried out by personnel independent of those having responsibility for the work being performed.

All verification personnel are required to be trained and certified per the LTC training and certification program (spec 06-09-0002 and 05-06-0007), and records of training are to be maintained. Adequate resources shall be identified and assigned for the areas of management, performance of work and verification activities, including internal quality audits.

4.1.2.3 Management Representative

The Manager of Quality Assurance and Reliability has the authority and responsibility for ensuring that the requirements of this Quality Manual are implemented and maintained.

A multidisciplinary approach is used for decision-making and to manage concept development through production and shipping.

4.1.3 Management Review

The Quality and Reliability Manager shall assure that the effectiveness of the quality system is reviewed and reported on, as shown below:

A) Annual strategic quality planning and goal setting to drive continuous quality and reliability improvement programs. This meeting is held at the beginning of each fiscal year with all department heads participating. The resulting goals are reviewed and approved by the management.

B) Quarterly management review of company performance vs. the Corporate Quality goals. The performance to goals is summarized by the Quality Assurance manager and distributed to the department heads. Semiannual reviews are distributed to the President and Vice Presidents.

C) Quality systems audit results shall be reviewed annually and at the end of each period by middle and upper management to determine the adequacy of, and compliance to, the documented quality system. Upper management includes the COO and President/CEO.

D) Quarterly Cpk reports of all critical process nodes by the SPC Manager.

E) Monthly QA reports to management including the President and COO, to report detailed results and trend analysis of QA monitors and gates.

F) On a real-time basis, the following reviews and/or actions are performed:

* Quality system audit results shall be reviewed to determine the effectiveness of the quality system.
* Failure analysis, root cause identification, and corrective action.
* Customer request for corrective action.
* Process/Preventive Action Teams (PATs) findings and recommendations.
* Review of nonconforming material/product reports.

G) The Quality Manual and/or procedures shall be revised when necessary to reflect the decisions of management reviews.

H) Records of all reviews shall be maintained for evaluation, as required.

4.2 QUALITY SYSTEM

4.2.1 General

The quality system of LTC consists of the Quality Manual, quality procedures for inspection, surveillance, and monitoring to ensure that our products conform to customer requirements.

4.2.2 Quality System Procedures

Documented and implemented procedures consistent with the requirements of ISO 9001 and stated quality policy shall form a part of the quality system.

4.2.3 Quality Planning

The system is designed to meet the requirements of ISO 9001, and the other requirements outlined in Section 4.0. The quality planning process covers all processes from incoming inspection through shipping.

Quality planning includes:

A) The preparation of quality plans in accordance with the specific requirements.

B) The identification and acquisition of any controls, processes, inspection equipment, fixtures, and total production resources and skills that may be needed to achieve the required quality.

C) Ensuring the compatibility of the design, the production process installation, servicing, inspection and test procedures, and the applicable documentation.

D) The updating, as necessary of quality control; inspection, and testing techniques, including the development of new instrumentation.

E) The identification of any measurement requirement involving capability that exceeds the known state of the art in sufficient time for the needed capability to be developed.

F) The identification of suitable verification at all required test, and inspection gates.

G) The clarification of standards of acceptability for all features and requirements, including those which contain a subjective element (i.e., workmanship standards).

H) The identification and preparation of quality records. (*For records, see Section 4.16.)*

REFERENCES

Spec Number	Title
06-03-5000	Customer Specification Review
06-03-5001	Internal SL Specification Procedure
06-04-0011	Design to RPL Flowchart
00-01-1006	SOP: Engineering Change Notice
08-07-1001	Calibration Program Requirements
05-03-8082	Assembly Workmanship Standards
06-03-7050	Record Keeping

4.3 CONTRACT REVIEW

4.3.1 General

Documented procedures shall be implemented and maintained for the performance of contract review and for the coordination of these activities.

4.3.2 Review

Prior to acceptance of a contract or order, it shall be reviewed in accordance with the referenced specifications herein, resolving issues, and determining the capability of the organization to meet customer requirements. Any differences identified during contract review will be documented and defined by an "SL" (Specified Lot) or by a special flow per the specifications below. If LTC cannot agree to any portion of the contract, a waiver agreement must be approved by the end-customer before the product is delivered.
(For records, see Section 4.16.)

REFERENCES

Spec Number	Title
06-03-5000	Customer Specification
06-03-5001	SL (Special Lot) Specification Procedure
Current Rev.	Device Catalogs, Data Book, Supplements

4.4 DESIGN CONTROL

4.4.1 General

LTC produces a broad line of standard, high performance linear integrated circuits which are defined in the marketing catalogs and data books. Design criteria and manufacturing capabilities have been established to support these products. (*For records, see Section 4.16.)*

4.4.2 Design and Development Planning

LTC Spec 06-04-0011 provides a guideline flowchart from design conception to product qualification and RPL. Since LTC manufactures primarily standard products, as opposed to custom products, there is no need to establish milestone

charts for the customer. Design and verification activities are planned and assigned to qualified personnel equipped with adequate resources.

4.4.3 Organizational and Technical Interfaces

A design review meeting is held weekly with engineering and management to review the status, document progress, and technical requirements of each design.

4.4.4 Design Input

Inputs for design typically come from review of customer's requirements, contract review, and marketing research to identify features which should be incorporated into a product. The primary goal is to provide customers with designs that reduce their component and board level costs, while providing leading edge technology. LTC manufactures primarily standard (non-custom) products. Based on the above inputs, the final design concept is developed in-house.

4.4.5 Design Output

The design output, an integrated circuit, is defined and described in a data sheet, which is released when the product is qualified. Product characterization and qualification are conducted to verify conformance to data sheet requirements.

The data sheet specifies the product performance limits as well as any other pertinent information pertaining to the product, e.g., design considerations that are critical in the safe and proper functioning of the product, regulatory requirements, etc.

4.4.6 Design Review

Design shall plan, conduct design reviews which are documented, and assigned to competent personnel representing all applicable functions.

4.4.7 Design Verification

Design verification shall establish that the product meets the data sheet requirements. Since the products designed by LTC are proprietary products (defined by LTC), LTC may change the final data sheet to match the characterization results prior to release. This further ensures that the design input matches the design output.

4.4.8 Design Validation

Design validation shall be performed prior to release to ensure that the product conforms to design requirements in accordance with Quality Assurance and Reliability Assurance Qualification requirements, 06-04-0001.

4.4.9 Design Documentation

The identification, documentation, and appropriate review and approval of all changes and modifications are accomplished via ECNs to the *Mask Sequence Specification, 02-01-xxxx .*

Design changes are controlled via LTC-supplied designs and bills of material to subcontractors.
(For records, see Section 4.16.)

REFERENCES (Company proprietary)

Spec Number	Title
80-01-xxxx	CMOS Design Rules
80-02-xxxx	Bipolar Design Rules
02-01-xxxx	Mask Sequence Specifications
02-02-1000	LTC Milpitas Fab New Product Documentation Requirements
02-02-1002	LTC Product Release to Fab Procedure
05-01-xxxx	Assembly Bonding Diagram and Bill of Materials
06-04-0001	Quality Assurance/Reliability Assurance Qualification Requirements
06-04-0011	Design to RPL Flowchart
09-01-0001	Released Product Listing/Top Mark Content and Layout Procedure

4.5 DOCUMENT AND DATA CONTROL

4.5.1 General

Documented and implemented procedures shall govern the control of all documents and data relating to the quality system.

4.5.2 Document and Data Approval and Issue

Pertinent issues of appropriate documents are available at all locations where operations are essential to the effective functioning of the quality system. Any initiation or change of the documentation required for procurement, manufacturing, and inspection of materials and product is controlled by the Document Control department to ensure review and approval by authorized personnel prior to issue.

Data associated with this Quality System shall be maintained and documented per Section 4.16, Control of Quality Records.

The Document Control group is responsible for the maintenance, control, reproduction, distribution and historical archiving of all of LTC's product and procedural documentation. Document Control services all internal areas in which Document Control Books (DCBs) are located, per the internal specifications listed on following page:

REFERENCES

Spec Number	Title
00-01-0010	Specification ID Master Plan
00-01-0005	Temporary Engineering Change Notice Procedure
00-01-1006	Standard Operating Procedure (SOP): Engineering Change Notice
00-01-1008	SOP: Specification Format and Organization
00-01-3100	ECN Approval Matrix
00-01-0001	Standard Operating Procedure: Document Control
00-01-0003	Distribution of Level 1 Specifications
00-01-3111	DCB Locations Report

4.5.3 Document and Data Changes

Document Control shall promptly post or route ECNs (Engineering Change Notices) and TECNs (Temporary Engineering Change Notices) to the appropriate locations when ECN approval is complete. The information on the ECN shall contain, as a minimum, the affected document number, description of the change, effective date and duration, affected documentation, justification for the change, documentation of material disposition, distribution, and approval signatures.

Previous revision history is available from the Document Control department. Additional justification and background information shall be provided by the ECN originator upon request of the designated signatory.

Document Control maintains a Master Spec Listing which includes the revision letter, effectivity date, specification number, product number (when applicable), and title. *See 00-01-0001, SOP: Document Control.*

When any change is made, LTC's standard practice is to generate an ECN or TECN to a specification or process. Each time an ECN or a TECN is generated, the revision changes and spec copies are reissued to all required Level 1 and Level 2 Document Control Book locations within the factory and all satellite locations as called out on the document footer.

REFERENCES

Spec Number	Title
00-01-1006	SOP: Engineering Change Notice
00-01-3100	ECN Approval Matrix
00-01-1008	SOP: Specification Format and Organization
00-01-0005	Temporary Engineering Change Notice
00-01-0001	SOP: Document Control

4.6 PURCHASING

4.6.1 General

Purchasing shall ensure that material purchased from suppliers and subcontractors is in conformance to specified requirements. Records of qualified suppliers shall be maintained.

4.6.1.1 Supplier Responsibility

It is the responsibility of the supplier to provide and maintain a quality system which will assure compliance with the requirements of the applicable material procurement specification, 01-xx-xxxx and the specifications listed below.

REFERENCES

Spec Number	Title
06-09-0003	Purchasing Procedure
01-xx-xxxx	Material Procurement Specification
09-01-0004	Qualified Vendor Listing Procedure
09-01-0008	Approved Subcontractor Listing
06-01-0011	Vendor Corrective Action
06-09-0018	SOP: Inventory Control
06-01-0006	Incoming Inspection, General
06-01-0007	Incoming Inspection, Subcontracted Materials
01-xx-xxxx	Applicable Drawing And Stores Item Numbers

4.6.2 Assessment of Subcontractors

Selection of sources to be qualified will be made upon the supplier's ability to conform to agreed upon requirements for quality, cost, delivery, and based upon previous performance.

LTC exercises tight control over critical subcontractors to prevent field reliability problems. The effectiveness of these controls is continually assessed through on-site engineering surveillances, incoming inspection results, reliability monitor results, and subcontractor-supplied SPC and Cpk data. This is defined in Specification 06-01-0020.

Previously qualified suppliers may continue to be used as long as they demonstrate the capability to meet all conditions and requirements.

Suppliers and subcontractors are granted approval after qualification testing and inspection of materials purchased under preliminary approval status. A monthly record of approved suppliers' and subcontractors' history is maintained and updated after completion of inspections and the disposition of all lots.

Suppliers and subcontractors that consistently demonstrate exceptionally high acceptance rates will become candidates for participation in the Preferred Vendor Program. Determination of suitability will be based on the following:

A) Consistently high acceptance rate through Incoming Inspection.

B) No field-related problems.

C) Recommendation by LTC's Preferred Vendor Board after reviewing the survey results from the vendor.

D) Willingness on the part of the supplier to provide periodic statistical data on the critical nodes/parameters that have been identified.

E) Suppliers and subcontractors that qualify for the partnership program will be placed on a reduced surveillance schedule, and they will be awarded a greater share of the business.

REFERENCES

Spec Number	Title
06-09-0003	Purchasing Procedure
01-xx-xxxx	Material Procurement Specifications
09-01-0004	Approved Vendor List
06-01-0007	Incoming Inspection, Subcontracted Material
09-01-0008	Approved Subcontractor Listing
06-01-0020	Distributor/Supplier/Subcontractor Survey and Audit for Qualification and Disqualification Procedures
06-06-0001	Statistical Process Control (SPC)
06-04-0002	Reliability Audit Program
06-05-7001	Failure Analysis Program
06-09-0008	Preferred Vendor Program

4.6.3 Purchasing Data

The purchase order shall list the LTC stock number, the description of the part, and designate the material as Type A, B, C, or D if applicable. The purchase order shall also state the drawing number or part number and the current revision level, the quantity needed, the applicable material procurement spec. and revision (for Type A & B materials only), the required delivery date(s) and the negotiated price. It shall also include inspection, test, and packaging requirements, as applicable. All Type A and B parts and materials shall be purchased from original equipment manufacturers, approved vendors and subcontractors, and authorized distributors. Below is a list of the categories:

Type A: Direct material that has distinct value-added identity on the finished product.

Type B: Indirect material consists of all material other than direct that is directly used in the manufacture of a product.

Type C: Indirect material consists of all material not directly used in the manufacture of a product.

Type D: Engineering evaluations consist of material specifically purchased for evaluations purposes and which Engineering will inspect. Type D material is not used as direct material, and will not be stored in an area where Type A material is stored. Type D material can be upgraded to Type A by having the requester complete a "Request to Enter a Part into Stores" and by having QA perform an incoming inspection on the material.

The purchase order is reviewed and approved by the management of the originating department. Additionally, Quality Assurance reviews and approves Purchase Orders for Type A and B material.

REFERENCES

Spec Number	Title
06-09-0003	Purchasing Procedure
01-xx-xxxx	Material Procurement Specifications

4.6.4 Verification of Purchased Products

When specified in the contract, the purchaser or his/her representative shall be afforded the right to verify at source or upon receipt that the purchased product conforms to specific requirements. Verification by the purchaser shall not absolve the supplier/subcontractor of his/her responsibility to provide acceptable products, nor shall it preclude subsequent rejection.

When the purchaser or his/her representative elects to carry out verification at the subcontractor's plant, such verification shall not be used by the supplier or subcontractor as evidence of effective controls of quality by the supplier/subcontractor.

4.7 CONTROL OF CUSTOMER-SUPPLIED PRODUCT

It is currently not LTC's practice to include purchaser-supplied materials in products. Therefore, this clause of ISO 9001 does not apply. In the event that LTC should agree contractually to accept/use purchaser-supplied product, LTC will document the procedures to verify, store, and maintain such product. Verification by the supplier does not absolve the customer of the responsibility to provide acceptable product.

4.8 PRODUCT IDENTIFICATION AND TRACEABILITY

Inventory identification and traceability shall be controlled through the assignment of product numbers, run numbers, lot numbers, serial numbers, date codes and back mark codes as appropriate.

Run card and lot traveler must, as a minimum, specify the lot number or run number, operation, device type or stock number, quantity in/out or quantity inspected/rejected (for inspection points). Runcards and lot travelers accompany the material through the factory until it reaches Boxstock.

Offshore subcontracted material shall be identified by general back mark codes.

The device back mark code is used to provide complete traceability to test lot traveler, assembly lot traveler, wafer fab traveler, and raw materials used. Where space allows, the *complete* backside mark code is imprinted, as follows: *(For records, see Section 4.16.)*

C/AA/BBB/XX/YY, where:	
C	Denotes Plant of Origin: Country of Origin (COO)
AA	Denotes Device Type
BBB	Denotes Assembly Lot Number
XX	Denotes Year
YY	Denotes Seal Week

REFERENCES

Spec Number	Title
05-03-4601	Country of Origin and Backside Mark
MIL-M-38510	Slash Sheet Drawings
SMD	Standard Military Drawings
DESC Drawing	SMD or Slash Sheet Drawings
MIL-STD-883	Compliant Data Sheets, LTC Data Book

4.9 PROCESS CONTROL

4.9.1 General

Processes which directly affect the quality of products or services delivered by LTC shall be carried out under controlled conditions. Controlled conditions include a production plan as well as appropriate controls for material, production and servicing equipment, processes and procedures, computer software, personnel, associated supplies, facilities, and environment.

A) Documented work instructions and necessary equipment and facilities shall be available and approved for all processes that affect the quality of the product.

B) It is the responsibility of each organization that handles product to monitor and control its processes.

C) Each organization has the responsibility for establishing requirements for the approval of processes and equipment.

D) Standards for workmanship shall be defined in each area either in documents called "workmanship standards" or "standard operating procedures," or by physical examples of product that conforms to requirement.

E) It is the responsibility of each department to assure its equipment is suitably maintained.

F) Only certified personnel perform qualified processes.

G) *For records, see Section 4.16.*

REFERENCES

Spec Number	Title
00-01-1008	SOP: Specification Format and Organization
06-02-XXXX	Quality Process Monitor Specs
06-08-XXXX	Procedures, Quality Audit
06-09-XXXX	Procedures, QA Standard Operating
05-03-8082	Assembly Workmanship Standards
08-07-1001	Calibration Program Requirements
06-09-0002	Operator Training and Certification Program
06-03-7050	Record Keeping
08-07-1003	Fab Maintenance P.M.
08-07-0656	Special Facilities Safety Guidelines and Procedures

4.9.2 Special Processes

Statistical Process Control (SPC) is implemented on all critical processes throughout the manufacturing flow.

All products shipped by LTC are 100% tested and inspected several times. All new products are fully characterized and qualified before release. LTC's Reliability program is designed to continually assess the performance of LTC devices in the field.

All of the above controls work together to ensure that any processing deficiencies become apparent before the product is delivered to the end customer. *Therefore, LTC does **not** have any "**special** processes."* See specifications listed on following page.

REFERENCES

Spec Number	Title
)0-01-1006	SOP: Engineering Change Notice
)6-03-5001	SL (Special Lot) Specification Procedure
)6-06-0001	Statistical Process Control (SPC)
)6-04-0002	Reliability Audit Program
)6-04-0011	Reliability Monitor Program
)6-04-0012	QR2 (Quick Reaction Reliability) Program
)6-04-0001	Quality Assurance/Reliability Assurance Qualification Requirements
(x-xx-xxxx	Applicable Standard Operating Procedures
(x-xx-xxxx	(Also, Specifications referenced in 4.10.2 apply to 4.9.)

4.10 INSPECTION AND TESTING

4.10.1 General

All final inspection and testing shall be performed in accordance with referenced procedures to verify acceptance to specified requirements.

4.10.2 Receiving Inspection and Testing

Receiving/Production Control shall be responsible for segregating all incoming material until completion of IQC inspection and for routing subcontracted assembly lots to QC for inspection.

4.10.2.1

In accordance with LTC's Quality Assurance procedures, all Type A and Type B purchased materials shall be subjected to QA Incoming Inspection.

Type A: Direct material that has distinct value-added identity on the finished product.

Type B: Indirect material consists of all material other than direct that is directly used in the manufacture of a product.

4.10.2.2

Lots may be released for further processing prior to completion of incoming inspection. However, IQC must be completed within 24 hours or 72 hours, depending upon the type of material that was released. If the sample fails, IQC notifies Production Control who works together to recapture the lot, provided that PC ensures that the affected lot(s) are not shipped prior to completion of IQC inspection.

Lots which pass all the criteria specified shall be considered acceptable. All logs, lot travelers, and boxes are stamped with a box IQC accept-date stamp prior to releasing the appropriate location.

If a lot fails any criteria, the lot is rejected and an inspection failure report (IFR) is initiated. All reject samples must be segregated and attached to the IFR. The responsible QA and Manufacturing Engineer must review and disposition the rejects and complete the IFR form.

The applicable Package and QA Engineers shall be responsible for notifying the supplier of any rejections and for following up on corrective action Discrepant Material Reports (DMR).

REFERENCES

Spec Number	Title
06-09-0003	Purchasing Procedure
06-01-0006	Incoming Inspection, General
06-01-0007	Incoming Inspection, Sub-Material
06-01-0011	Vendor Corrective Action
06-02-0020	Inspection Failure Report (IFR) Procedure
01-xx-xxxx	Material Procurement Specifications
06-08-0013	Control of Age/Temperature Sensitive Materials
08-07-1001	Calibration Program Requirements

4.10.3 In-Process Inspection and Testing

LTC shall:

A) Inspect, test and identify product as required by the quality plan or documented procedures.

B) Establish product conformance to specified requirements by use of process monitoring and control methods. *See Section 4.20 for specifics.*

C) Hold product until the required inspections and tests have been completed or necessary reports have been received and verified except when product is released under positive recall procedures. *See Section 4.10.1.* Release under positive recall procedures shall not preclude the activities outlined in Section 4.10.2A.

D) Identify nonconforming products.

See specifications listed on following page.

REFERENCES (Representative)

Inspection	Hold	Monitors	Test	Records
06-02-0001	06-02-0020	06-02-0002	06-02-0006	06-03-7050
06-02-0003		06-02-0004	06-02-0011	06-03-7051
06-02-0005		06-02-0008	06-02-0019	06-03-5000
06-02-0007		06-02-0012	06-02-0031	06-03-5001
06-02-0009		06-02-0017	06-03-0011	06-03-7068
06-02-0014		06-02-0022	06-03-0012	09-01-0002
06-02-7002		06-02-5001	06-03-7001	09-01-0004
06-02-7003		06-02-7036	06-03-7003	09-01-0005
06-02-7004		06-08-0002	06-03-7004	09-01-0008
06-02-7070		06-08-0003	06-03-7006	
06-03-7028		06-08-0004	06-03-7007	
06-03-7029		06-08-0005	06-03-7008	
06-03-7030		06-08-0015	06-03-7009	
06-03-7031		06-09-0018	06-03-7011	
06-03-7035		06-09-0019	06-03-7012	
06-03-7036		06-09-9001	06-03-7016	
06-03-7038		06-09-9003	06-03-7017	
06-03-7061			06-03-7018	
06-03-7062			06-03-7019	
06-03-7066			06-03-7025	
06-06-0001			06-03-7026	
06-08-0014			06-03-7027	
08-07-1001			06-03-7032	
			06-03-7033	
			06-03-7034	
			06-03-7063	
			06-03-7064	
			06-03-7065	
			06-03-7067	
			06-04-0001	
			06-08-0006	

4.10.4 Final Inspection and Testing

All products will undergo a final test according to the applicable test procedure, and will be inspected for completeness of specified requirements, appearance against applicable workmanship standards, and all associated data and documentation are available and authorized.

Electrical test and visual/mechanical acceptance shall precede transfer to the Finished Goods inventory area. Finished Goods inventory consists only of products formally on the released product listing (RPL). Additionally, it is impossible to ship product that is not on the RPL, as the computer will not print a shipper. Inspection of product prior to shipment shall assure compliance to contractual requirements as described by referenced procedures and applicable "SL" or special flow requirements.

The government shall be allowed access to LTC and subcontractor facilities to verify acceptability, when contractually required.

REFERENCES

Spec Number	Title
06-02-0014	Outgoing QA Electrical Test for 883, STANDARD MIL, and Commercial Devices
06-02-0013	QA External Visual Inspection
06-02-7002	QA Post Pack Inspection
06-02-7003	QA Shipbench Inspection
04-04-XXXX	Final Test Set-Up Specifications

4.10.5 All Inspection and Test Records

Records that product has passed all required inspections and tests as defined in the Quality plan must be maintained. These include records from: Test, Visual/Mechanical, Post-pack, Boxstock, Shipbench, SL, and Flows.

Specific procedures defining acceptance criteria for inspection and test records may be found by referring to the specifications listed below, or on the applicable lot travelers. Records shall identify the inspection authority responsible for the release of product, and shall clearly show the acceptance or failure of required inspections or tests (reference Section 4.12).

Nonconforming material shall be identified, segregated, and dispositioned in accordance with Section 4.13 and referenced procedures. *See Section 4.16 for specifics.*

REFERENCES

Spec Number	Title
06-03-7050	Record Keeping
00-01-1006	SOP: Engineering Change Notice

4.10.6 Test Software Control

Test software shall be approved before use by Test Engineering. Test software shall be stored for use in a controlled access "server," from which only the most current and approved software shall be used to test product.

A document-controlled Test Program Book contains released (04-12-xxxx) test program listings, including the program name and latest revision for each device type for Wafer Sort, Final Test, and QA tests. Revisions used are recorded on the test flow traveler, which also serves as a test specification.

Changes to test procedures can only be made after an ECN has been approved and signed off. Major changes to software (as defined in spec 06-04-0007) can only be made after an ECN has been approved and signed off.

Whenever possible, equipment accuracy to parameter tolerance shall be of at least a 10:1 ratio. However, when 10:1 accuracy is not possible, electrical quality is guaranteed by guard banding test limits against the published data sheet.

Guard bands are set by a combination of published test equipment specifications and SPC techniques. This ensures that parametric readings outside device specifications are deleted, resulting in the faulty unit being rejected.

Additionally, a final QA sampling plan guarantees acceptance to quality limits inside of published data sheet parameters.

REFERENCES

Spec Number	Title
00-01-1006	SOP: Engineering Change Notice
04-04-6300	Test Area SOP
04-01-xxxx	Standard Product Test Flows
04-13-xxxx	SL Product Test Flows
04-21-xxxx	SMD and DESC Drawing Test Flows
04-12-xxxx	Test Program List
04-14-xxxx	SL Product Test Program Index
04-25-xxxx	SMD and DESC Drawing Test Programs
06-04-0007	Customer Notification of Major Changes
06-04-0009	Datasheet Change Control

4.11 CONTROL OF INSPECTION, MEASURING, AND TEST EQUIPMENT

A) LTC measuring and test equipment shall be controlled, calibrated, and maintained prior to release for use during production, installation, or servicing to demonstrate the conformance of product to the specified requirements. Subcontractors and vendors shall demonstrate conformance to the intent of MIL-STD-45662.

B) A unique identification must be provided for all equipment and tools requiring calibration. This will be included on the calibration recall list which includes the department number, equipment type and due date.

C) The re-calibration frequency must be determined and recorded. The calibration of inspection, measuring and test equipment, including torque tools, shall be checked before use or if the equipment is dropped (or otherwise subjected to impact).

D) LTC uses outside calibration laboratories or services provided by the original equipment manufacturer.

Prior to any contractual agreement, all outside calibration labs used to calibrate any of LTC's test and measurement equipment must be audited by QA to MIL-STD-45662 and 08-07-1001 "Calibration Program" requirements. The outside calibration system and controls must comply with MIL-STD-45662 requirements.

Outside calibration labs shall be responsible for maintaining a complete and accurate list of instruments and equipment from LTC under the service agreement.

The list shall identify the instruments to be serviced by means of coded symbols to identify the service performed and recall period.

The outside lab shall furnish data sheets or certification for each calibration performed.

E) Criteria are established for review of equipment to determine if calibration is required. If **any** of the following conditions is met, calibration will **not** be required.

1) Equipment performs a particular function, but it is required that other calibrated equipment be used with equipment at initial setup.
2) The performance of equipment is monitored through the use of calibrated equipment.
3) Equipment is used for indication only.
4) Equipment where calibration has no meaning or cannot be performed.
5) Equipment will be identified with a sticker stating, "calibration not required."

F) New equipment calibrated directly by original manufacturers shall be accepted if they meet the following requirements:

1) Calibrates equipment in accordance with established written calibration procedures.
2) Records all out-of-spec conditions with *before* and *after* values.
3) Supplies original calibration data and paperwork which satisfy these requirements:
   a) The appropriate inspection, measuring, and test equipment are selected to provide the required accuracy for all measurements to be made. The equipment to be used and measurements to be made shall be defined in the detailed procedures or travelers.
   b) Calibration and adjustment are performed as required by the individual calibration procedure and/or manufacturer's specifications. Primary, secondary, and working standards are to be traceable to the National Institute of Standards and Technology (NIST) or to natural physical constants.

G) Where test hardware or test software is used, correlation units are tested to ensure equipment has been set up and running properly. Correlation units are run at the frequency defined in the applicable procedures. Correlation wafer/units are also used to verify the set-ups and test programs if the operators are experiencing a large number of rejects.

In general, test hardware, software, and techniques are considered proprietary to LTC. Such information is not released except by non-disclosure agreement and by authorization of the Chief Operating Officer. However, to resolve correlation difficulties with customers, LTC can provide serialized and data logged devices.

H) Procedures describing the verification of calibrated equipment are listed below:
   1) The accuracy, precision, and capability of inspection and measurement equipment must be sufficient to provide meaningful results. Equipment is selected based on manufacturers' guaranteed operating specifications and tolerances. During initial inspection/test development, correlation studies are conducted to verify desired results.
   2) For critical inspections or where an SPC control chart is to be used, a Measurement System Evaluation (MSE) or Gauge Repeatability and Reproducibility (Gauge R & R) is conducted to ensure capability.
   3) Every user is responsible for checking the calibration status of a calibrated tool or piece of equipment *before it is used* and is responsible to see that it is **not** used if calibration is required before use. This is done by verifying the data on the calibration sticker and/or as defined in the applicable detailed procedure.

I) Records of recall notices shall also be maintained along with calibration certificates of conformance (C of C) in the applicable equipment history file.

A history file shall be kept by QA for each piece of calibrated equipment. The file shall consist of calibration data sheets, calibration certificate of conformance, and out-of-tolerance evaluation forms (if applicable).

The test maintenance group shall be responsible for maintaining the calibration data sheets on equipment under their calibration program, with a copy going to QA for the history file.

Records shall be kept a minimum period of 5 years (or longer, if required by customer contract).

J) In the event that a piece of equipment is found to be out of calibration, consideration is given to review all previous work completed with the equipment since the previous calibration.

Any out-of-calibration condition that is determined to adversely affect product quality or reliability will require rectification, customer notification and possible recall of product.

K) Calibration procedures shall have the specified temperature and humidity for specific environmental conditions listed in the various equipment calibration specifications. Areas where operations are sensitive to surrounding environment shall be specified, monitored, and controlled.

L) Upon receipt and before use, equipment is inspected for damage and verification that appropriate calibration stickers have been affixed to the equipment.

M) Production tooling used as inspection media shall be controlled and checked for accuracy at set intervals, according to calibration procedures.

N) As deemed necessary to verify acceptability, government and customer representatives shall be allowed access to personnel and use of calibrated equipment.

O) Any advanced metrology requirement (exceeding the known state-of-the-art technology) identified during contract review shall be addressed by Test Engineering and reported on the spec review form.

REFERENCES

Spec Number	Title
MIL-STD-45662	Calibration Systems Requirements
08-07-1001	Calibration Program Requirements
04-05-xxxx	*Applicable Test Preventive Maintenance (PM) Calibration Procedures*
02-05-xxxx	Applicable Fabrication P.M. Calibration Procedures
08-07-1003	Fab Maintenance P.M. Specification
06-06-0001	Statistical Process Control (SPC)
06-08-0002	Controlled Environment Surveillance
08-07-xxxx	Applicable Facilities P.M. Procedures

4.12 INSPECTION AND TEST STATUS

Inspection stamps serve to identify the inspector who has accepted or made an authorized disposition of material or product. Trained and certified inspectors shall be issued inspection stamps which are to be used to indicate completion of acceptance testing.

Inspection stamp design is unique to LTC.

Each inspection area shall segregate inventory according to inspection status and implement positive controls to segregate accepted materials from rejected material.

Manufacturing lot travelers shall accompany all material. The traveler shall show at least those manufacturing steps from the last quality gate function and/or all manufacturing operations which describe work operations being inspected. Lot travelers shall indicate completion of manufacturing operations by operator initials or number, date and quantity out.

The identification of inspection and test status shall be maintained (as defined in the procedures referenced herein); throughout production of the product to ensure that only product that has passed the required inspections and tests is shipped.

Each gate inspection shall include verification that specified manufacturing and inspection steps have been completed.

Only accepted material which passes QA Final Inspection is allowed in the Boxstock area. All containers are identified with a QA stamp on the label of the box. Only product which is fully qualified and on the Released Products List (RPL) can be shipped from Boxstock.

REFERENCES

Spec Number	Title
06-02-0001	Quality Assurance Inspection, Wafer Sort
06-02-1000	Quality Control Checkpoints
06-06-0002	QA Inspection Stamp Control
06-02-0020	Inspection Failure Report
06-02-7003	QA Boxstock Inspection
06-02-7002	QA Post-Pack Inspection
06-02-0003	QA 2nd Optical Inspection
06-02-0007	QA 3rd Optical Inspection
06-02-0009	Group-A Electrical Test
06-02-0014	Outgoing QA Electrical Test for 883, STANDARD MIL, and Commercial
09-01-0002	Released Product Listing

4.13 CONTROL OF NONCONFORMING PRODUCT

4.13.1 General

Nonconforming material shall be identified and segregated to prevent unauthorized or accidental use. Where nonconformance is detected during a verification step, the nonconformance shall be recorded and corrected before the product is moved to the next step in the process, with notification to the functions concerned.

All processes, work operations, quality records, service reports, and customer complaints are analyzed to detect and eliminate potential causes of nonconforming product.

4.13.2 Review and Disposition of Nonconforming Material

Where a nonconformance is detected in process, the product shall be scrapped, reworked, or returned to the preceding step for correction. MRB dispositions for raw materials are as specified in #06-01-0006.

All rework shall be performed per approved procedures and results shall be recorded on the appropriate rework traveler. Reworked product shall be re-inspected/re-screened in accordance with documented procedures.

LTC does not perform *repair* on any shippable product.

The responsibility for review and the authority for disposition of nonconforming product and materials are described in the following procedures:

REFERENCES

Spec Number	Title
06-02-0020	Inspection Failure Report
06-01-0006	Incoming Inspection, General (¶9.8-9.16)
06-01-xxxx	Applicable Incoming Inspection Procedures
06-02-xxxx	Applicable Inspections and Monitoring Procedures
06-03-xxxx	Applicable Inspection and Test Operational Procedures
06-09-0018	SOP: Inventory Control
06-09-0019	Engineering Alert: Minimum Yield Requirements
06-09-0022	Nonconforming Material Control Procedure
02-04-1102	Stop/Start Procedure
06-02-3000	CMR

4.14 CORRECTIVE AND PREVENTIVE ACTION

4.14.1 General

Prevention procedures and corrective action procedures to ensure that the product conforms to established specification and quality standards are vital parts of LTC's continuous quality improvement program.

A) The intent is to identify the **root cause** of a nonconformance and for correction and prevention of recurrence. This applies to all manufacturing and support operations responsible for the manufacture of product, and shall apply to (but not be limited to): Design, Purchasing, Manufacturing, Testing, Final Packaging for Shipment, Customer Material Returns and Failure Analysis.

Emphasis shall be placed on identifying the root cause and the prevention of recurrence of the nonconformance. This may include containment, an interim corrective action, a final corrective action, and subsequent audits to ensure that the required corrective action measures are in place and are effective in preventing recurrence of nonconformances.

The response time goals are:
- Containment within 24 hours.
- Verification within 48 hours.
- Root cause and corrective action identification plan within 10 days.

B) Discrepancies found during incoming inspection of raw material lots are documented on a Discrepant Material Report (DMR) by the QA group. Once a rejection is determined by the MRB to be valid, the QA Group is required to generate a Vendor Corrective Action Request (VCAR). Upon receipt of the completed VCAR from the supplier, Quality Engineering shall determine if the corrective action is sufficient to prevent a recurrence of the problem. If a supplier does not provide effective corrective action, the supplier may be disqualified.

Discrepancies found during in-process or outgoing inspection are documented on an Inspection Failure Report (IFR) by QA, or on a Stop/Start by Production if the in-process inspection is performed by the production group. The IFR or Stop/Start is reviewed by the appropriate Engineering group to determine lot disposition and appropriate corrective action. All IFRs are summarized in a monthly trend report by the QA department. The report is issued to the responsible Production and Engineering groups for review with emphasis placed on eliminating recurring problems.

Other activities which may identify the need for initiating corrective action are:
- calibration (out of tolerance)
- failures from a QA inspection step (IFR)
- results from reliability monitoring
- results from quality measurement analysis
- corrective action reports
- SPC chart OCAPs
- findings from process audits and quality system audits
- management reviews of the quality system and quality trends
- customer feedback
- vendor ratings and audits
- failure analysis

C) When quality problems or undesirable trends occur, the Quality Control Team (QCT) is responsible for initiating a meeting or series of meetings to establish a Process Action Team (PAT) to identify and define corrective action measures. These meetings are held until the problems are resolved or when quality levels are improved to an acceptable level.

D) The responsibility for taking appropriate preventive and corrective action is to be shared among Production, Quality Assurance, Reliability, and Engineering groups. Representation on the PATs should reflect this shared responsibility of preventive/corrective action. All of the above groups are responsible for ensuring that the corrective actions are effective.

E) Any changes in procedures which result from a corrective action are documented through the Engineering Change Notice (ECN) procedure and are recorded in the Document Control department.

F) All customer failure analysis reports are distributed to management, including the president and chief operating officer.

REFERENCES

Spec Number	Title
06-02-0020	Inspection Failure Report (IFR) Procedure
06-01-0011	Vendor Corrective Action
02-04-1102	Stop/Start Procedure
06-02-3000	Customer Material Return Processing Procedure
06-05-7001	Failure Analysis Program
06-06-0001	Statistical Process Control
06-08-0014	Quality Audit Procedure
06-01-0006 / 06-09-0003	Material Review Board (MRB) Procedures
06-06-0003	Team Problem-Solving
06-09-0020	Corrective and Preventive Action Program

4.14.2 Corrective Action

The procedures for corrective action shall include:

A) the effective handling of customer complaints and reports of product nonconformities;

B) investigation of the cause of nonconformities relating to product, process, and quality system, and recording the results of the investigation (see 4.16);

C) determination of the corrective action needed to eliminate the cause of nonconformities;

D) application of controls to ensure that corrective action is taken and that it is effective.

4.14.3 Preventive Action

The procedures for preventive action shall include:

A) the use of appropriate sources of information such as processes and work operations which affect product quality, audit results, quality records, service reports, and customer complaints to detect, analyze, and eliminate potential causes of nonconformities;

B) determination of the steps needed to deal with any problems requiring preventive action;

C) initiation of preventive action and application of controls to ensure that it is effective;

D) confirmation that relevant information on actions taken is submitted for management review *(see 4.1.3)*.

4.15 HANDLING, STORAGE, PACKAGING, AND DELIVERY

4.15.1 General

Documented procedures define the system for the preservation, segregation, and handling of all items and government-owned property throughout the entire manufacturing and inspection flow through storage and shipping. Precautions shall be taken to protect material from abuse, misuse, damage, deterioration, and unauthorized use.

4.15.2 Handling

All production parts, supplies, and components shall be handled in a manner that will prevent damage or deterioration. Handling requirements are further defined in the following:

REFERENCES

Spec Number	Title
06-09-0015	SOP to Prevent Product Mixing
06-09-9001	Electrostatic Discharge Control Requirements
06-08-0005	Environment Requirements for Processing and Storage
06-09-0018	SOP: Inventory Control
04-04-6300	Test Area SOP
05-03-7903	Mark and Pack SOP
06-01-0006	Incoming Inspection, General
06-01-0007	Incoming Inspection, Subcontracted Material
06-09-0001	Quality Assurance Policy

4.15.3 Storage

All materials processed shall be stored in a manner that will minimize the possibility of incurring damage or deterioration. During the scheduled quality system audit, samples of stock shall be checked for damage and deterioration of packaging. Access to the Stores, Boxstock, and Dispatch areas shall be limited to authorized personnel.

The condition of product in stock shall be assessed at appropriate intervals for the detection of deterioration.

Procedures for receipt, dispatch, and storage of material are referenced in the following specifications:

REFERENCES

Spec Number	Title
06-07-0001	Dispatch Procedure
06-07-0002	Boxstock Procedure
06-08-0005	Environment Requirements for Processing and Storage
06-09-0004	SOP: Stores
06-09-0018	SOP: Inventory Control
06-09-9001	Electrostatic Discharge Control Requirement
09-07-0003	Special Flows
06-04-0011	Reliability Monitor Program (Boxstock Audit)
06-08-0013	Control of Age/Temperature Sensitive Materials

4.15.4 Packaging

All materials shall be packaged in a manner that will minimize the possibility of incurring damage or deterioration during storage and handling. Procedures defining further requirements for packaging may be found by referencing procedures in the following specs:

REFERENCES

Spec Number	Title
05-03-2000	Wafer Pack
05-03-2003	Break and Plate
05-03-4601	Back/Side Mark
05-03-4604	Mark and Pack Incoming Procedure
05-03-7899	Pack Partial Finish Product Singapore
05-03-7900	Pack
05-03-7901	Die Pack
05-03-7903	Mark and Pack SOP
06-01-0026	Incoming Inspection Age Sensitive Material
06-01-0010	Incoming Inspection Anti-Static/Conductive Packaging Material
06-02-7002	QA Post-Pack Inspection
06-07-0002	Boxstock Procedure
06-08-0013	Control of Age/Temperature Sensitive Materials
06-09-9001	Electrostatic Discharge Control Requirements
09-01-0005	Top Mark Layout Listing (TML)
09-07-0003	Special Flows

4.15.5 Preservation

(Does not apply)

4.15.6 Delivery

Unless specified in the contract, the Customer Service department is responsible for the selection of carriers and the arrangement of shipments. The final boxing and shipping of finished products is the responsibility of the shipping department to ensure protection of product quality after final inspection and during transit to its final destination.

Specific procedures defining the details of these processes are listed below:

REFERENCES

Spec Number	Title
06-07-0002	Boxstock Procedure
06-02-7003	QA Shipbench Inspection
06-09-9001	Electrostatic Discharge Control Requirements

4.16 CONTROL OF QUALITY RECORDS

Quality records shall be retained in such a manner as to be retrievable. These records document conformance to specifications and the effective operation of the quality system.

All records used to substantiate controls for military/aerospace, high reliability, MIL-M-38510 and MIL-STD-883 product shall be retained for a minimum of five (5) years.

For commercial products not covered by customer purchase order record retention requirements, records of manufacturing, quality assurance, and support groups are retained for a period shown below.

All quality records shall be legible and traceable to the product involved. Quality records shall be stored and maintained so that they are readily retrievable in facilities that provide a suitable environment to minimize deterioration, damage, or loss.

Where contractually agreed upon, quality records shall be made available for evaluation by the customer or the customer's representative for an agreed period.

The following procedures contain additional requirements regarding record keeping:

REFERENCES

Spec Number	Title
06-03-7050	Record Keeping
06-03-7051	Electronic Archiving Operating Procedure

4.16.1 Quality Records Matrix

The following table (Quality Records Matrix) identifies the types of quality record, where the record is kept, the method of storage, the position or function responsible and the minimum retention period.

Quality Records Matrix

Quality Record	Location	Method	Responsible	Period
Quality System Review Report	QA	File	QA	Min. 3 Years
Design Verification	Engineering	File	P.E./D. Engr.	Life of Product
Contract Review	Cust. Spec. Review	File	QA	5 Years
Inspection Records	QA/IQC	Elect. File	QA/IQC	Min. 5 Years
Failure Analysis Reports	QA/Rel.	Elect. File/Data Base	QA/Rel.	Min. 5 Years
Initial Documentation/Subsequent Changes in Design Material or Processing, Qualification Test and Change Records	QA/Hi Rel.	Elect. File/Data Base	QA/Hi Rel.	Min. 5 Years
Specification (Documents, Applicable Forms)	Doc. Control	File/Data Base	Doc. Control	Life of Document
Calibration	QA/Test Maint.	File/Data Base	QA/Test Maint.	Life of Equipment
In-Process Monitor Inspection Logs Control Charts Stop/Start Sheets/ IFRs	QA/IQC	Elect. File	QA/IQC	Min. 5 Years
All JAN 38510, 883, Customer Rel, Wafer Fab Assembly, Screening Qualification, Quality Inspection Records including all printouts, read/record data)	Hi Rel/JAN Prog/QA	Elect. File	Hi Rel/Jan Prog/QA	Min. 5 Years
All Commercial Fab Travellers, Wafer Sort Summaries, Final Electrical Screening, QA Inspection Records, and Mark and Pack Travellers	QA/Manufacturing	Manufacturing/ VAX File/QA Elect. File	Wafer Fab, Test, Mark & Pack	Min. 3 Years
All Commercial Assembly, Qualification and Quality Inspection Records, (including all printouts, read/record data)	QA	Elect. File/File	QA	Min. 1 Year
All Procurement Documents	Purchasing	File/Data Base	Purchasing	Min. 5 Years
All QA Inspection Stamp Control Records	Doc. Control	File	Doc. Control	Min. 5 Years
Quality Audit Reports (QARs), Audit Logs (two years), Vendor/Sub-Contractor Audits, Customer Audits, Quality Deficiency Records (QDRs) generated by DESC or DCMC, Distributor Audit Reports	QA Audit	File	QA Audit	Min. 5 Years
Operator Training/ Certification	Personnel/ Applicable Trainer	File Elect. File	Personnel Applicable Trainer	Active File, 1 Yr. Active File, 1 Yr.
Control Charts (SPC)	Applicable Area	File	Area Supervisor	Min. 3 Years
MIL-SPEC Library	QA	File	QA	Life of Document
POE Results, Problem Analysis and Preferred Vendor Records	SPC Dept.	File	QA	Min. 5 Years

4.17 INTERNAL QUALITY AUDITS

Internal audits of the quality system shall be conducted according to a schedule established by the Corporate Quality Audit department. The schedule shall ensure that all areas operating under the quality system described in this quality manual are audited at least once per year.

The results of these audits shall be documented and communicated to the management of the area being audited. Management will ensure that corrective actions are taken to resolve audit findings. *(See Section 4.16).*

Quality system audit results shall be reviewed to determine the adequacy of, and compliance to, the documented quality system.

The corporate auditor will follow-up until corrective action is implemented. *(See Section 4.16).*

The results of internal quality audits shall be part of the input to management review activities. *(See Section 4.1.3).*

The audit process is detailed in the following procedures:

REFERENCES

Spec Number	Title
06-08-0014	Quality Audit
06-08-0015	MIL-M-38510 Quality Audit Checklist
06-01-0020	Distributor/Supplier/Sub-Contractor/ Vendor Survey/Audit Qualification/Disqualification Procedure
09-01-0008	Approved Subcontractor Listing
09-01-0004	Approved Vendor Listing
06-03-7050	Record Keeping
06-03-7051	Electronic Archiving Operating Procedure

4.18 TRAINING

Each department shall establish training requirements for all jobs that effect the quality of product shipped to customers. Individual departments shall maintain records to indicate that a person has satisfactorily completed the appropriate training for his/her assigned job.

It is the responsibility of each functional manager to insure that his/her personnel receive proper training. All employees are to be trained and motivated to provide excellence in workmanship throughout the manufacturing process and to provide the service to our customers which is the standard by which other companies are judged.

Personnel performing specific assigned tasks shall be qualified on the basis of appropriate education, training and/or experience, as required.

Training records shall be maintained by each functional supervisor, and a copy is to be sent to Human Resources. Records shall indicate: Employee Name, Date of Hire, Badge Number, Department Number, Supervisor, Spec Trained to (Title of Spec and Number), number of training hours, Initials of Trainer, Operator's Initials, Date Certified. *(See Section 4.16).*

It shall be the responsibility of the quality systems audit department to monitor the training and certification records to ensure compliance with the documented requirements.

REFERENCES

Spec Number	Title
06-09-0002	Operator Training and Certification Program
05-06-0007	EOL Operator Training and Certification Program
06-09-0007	LTC Safety Policy (Required By 06-09-0002)
06-09-9001	ESD Control Procedure
06-08-0005	Environmental Requirements for Processing and Storage
08-07-0028	Wafer Fab Smock Procedure
06-03-7050	Record Keeping Procedure
xx-xx-xxxx	Applicable Specifications / Training Specifications per Work Area

4.19 SERVICING (FAILURE ANALYSIS)

Failure analysis of devices returned from customers is the only service which is provided by LTC.

Failure analysis is the joint responsibility of the Reliability group, Product Engineering, and Design Engineering. Outside analytical labs are utilized in special areas which require capabilities beyond the scope of the in-house equipment.

Procedures for identification, handling, and analysis of reject or defective devices shall be documented. This information will be conveyed to the customer and government representative via a formal Failure Analysis Report in accordance with established industry standards including, but not limited to, MIL-M-38510, MIL-I-38535 Appendix A, and MIL-Q-9858.

A summary report of failure analysis activity findings shall be prepared and submitted to management on a quarterly basis, or more frequently, if necessary.

REFERENCES

Spec Number	Title
06-05-7001	Failure Analysis Program
MIL-I-38535	General Spec for Microcircuits
MIL-Q-9858	Quality Program Requirement

4.20 STATISTICAL TECHNIQUES

4.20.1 Identification of Need

A Statistical Process Control (SPC) program is in place to improve process capability, reduce process variations, provide continuous improvement, and provide robust designs along with the statistical sampling plans used as an integral part of inspection and testing.

The SPC program is applicable to all manufacturing processes, to operations which use statistical sampling for control or acceptance purposes, and to designs that are deemed critical.

Statistical techniques are employed by LTC to analyze process data and to identify the root causes of process variation so that the process can be modified to achieve:

A) Continuous reduction of variability around the desired target;
B) Consistency over time;
C) Conformance to requirements.

The SPC program comprises the following key elements:

A) An SPC structure: Steering Committee (Corporate level), Quality Control Teams (area SPC facilitators/ management), and Process Action Teams (PATs).
B) Employee training: Basic SPC, Advanced SPC, Design of Experiments, and Team Organization.
C) Establishment and documentation of Critical Nodes in manufacturing/related processes via flow charts and Control Plan Detail tables.
D) LTC's Self-Audit program of the SPC program.
E) Application of SPC to manufacturing, inspection, calibration, maintenance, preventive maintenance, environmental control, document control, purchasing materials, service data, and other areas as the need arises.
F) Formation of SPC Process Action Teams (PATs) composed of representation from manufacturing, engineering, maintenance, (and as applicable, quality engineering) with the objective of applying SPC to solve problems, improve process capabilities and reduce process variation.
G) Reports shall be established to measure progress made in terms of improved process capabilities (Cp & Cpk indexes) and quality improvements.
H) Statistical Sampling procedures are employed for those operations not requiring 100% inspection or which are destructive in nature.
I) Goal setting for continuous quality improvement.

Specific statistical methods and applications available include, but are not limited to, the following:

A) Design of Experiments/factorial analysis
B) Analysis of variance/factorial analysis
C) Safety evaluation/risk analysis
D) Tests of significance
E) Quality control charts/Cum-Sum techniques
F) Statistical sampling inspection

4.20.2 Procedures

Documented procedures shall be implemented and maintained for controlling the application of the identified statistical techniques.

REFERENCES

Spec Number	Title
MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
06-06-0001	Statistical Process Control (SPC) Procedure
06-06-0003	Team Problem Solving

4.21 QUALITY COST

Quality cost data, the cost of scrap, rework, and prevention of defective material are of primary concern at LTC.

Quality cost data shall be collected, analyzed, and used to improve effectiveness, efficiency, and control waste. This data is in the form of yield reports and scrap reports, which are compared to their respective specified goals.

The overall operating expenses of the Quality Assurance Department are forecast and budgeted on an annual basis. The cost of department operation is broken down into specific categories. Each category is reviewed on a monthly basis to assess actual cost versus planned cost.

All yield, scrap, and cost data are considered *LTC Confidential,* and may only be reviewed with customers upon the express, written permission of LTC's Chief Operating Officer.

APPENDIX A—RELIABILITY ASSURANCE

- The Reliability Assurance group shall be made up of professional individuals with training and experience in environmental stress testing, failure analysis techniques, reliability calculations, and reliability predictions of integrated circuits.
- The activities of the Reliability Assurance group shall focus on measurements of product reliability, as well as the identification and timely elimination of design and processing deficiencies which limit or otherwise compromise product reliability.
- Reliability Assurance shall exercise full authority over the qualification of all products, processes, materials, and manufacturing locations.
- The Reliability Assurance group shall prepare and implement written program plans and detailed procedures covering, *as a minimum*, these areas:

  Wafer Fabrication Reliability Monitor Program

  Quick Reaction Reliability Audit Program

  Long-Term Reliability Audit Program

  New Product/Process/Material Qualification Program

  Major Change Qualification

  Assembly Subcontractor Qualification

  Failure Analysis and Corrective Action Program
- Achieving extremely low failure rates during product life in the field demands that the integrated circuit manufacturer audit reliability performance of outgoing products.
- Product reliability audits are the responsibility of the Reliability group, with immediate responsibility for program implementation, performance, and reporting assigned to the Manager of Quality and Reliability Assurance.
- A summary data file shall be maintained on all product families. This summary shall include, *as a minimum*, the device type tested, the package type, the assembly location, the manufacturing date code, the actual test condition used, the sample size, the duration of the test, and the number of failures observed.
- Management shall be apprised *immediately* of any audit results which indicate that failure rate goals are not being met or that significant degradation in performance is evident.

PRODUCT QUALIFICATION PROGRAM

- New products will not be released without acceptable reliability data as defined by Reliability and Quality Assurance and the responsible engineering groups.
- Before any major design or process change is considered qualified, sufficient test data shall be collected to demonstrate that the processes used conform to applicable government, industry, customer, and internal specifications. The finished devices must be capable of passing all tests as required by applicable government, industry, customer and LTC specifications.
- *A **major change*** is defined as a significant departure from the existing approved process/design, as agreed by Reliability Assurance and Manufacturing, or Design and documented in LTC's 06-04-0001 and 06-04-0006 Qualification Specifications.
- Similarity in materials and design to previously qualified products shall be considered sufficient for purposes of new product or ***process change qualification***. Similarity data may be supplemented with test data on the product in question in those areas where similarity does not justify blanket qualification of the product or change approval.
- Life test data on one device within a product family can be used to generically qualify other devices within the same product family, providing the devices are encapsulated in packages made from the same materials and sealed using the same sealing process. For purposes of qualification, a product family includes all microcircuit chips of equivalent complexity or function made in the same wafer fab area using the same process.
- Qualification requirements shall be established and documented for all products and processes. Documentation shall include the tests, test conditions, and pass/fail criteria which must be met before the product or process is considered fully qualified.
- Qualification tests shall include environmental tests and mechanical tests as specified in the LTC 06-04-0001 spec, but shall not necessarily be limited to these tests where device service conditions are known to be more severe than the test conditions in the standard qualification.
- Qualification requirements on MIL-STD-883, SMD (standard military device), and MIL-M-38510 devices shall be per Method 5005 of MIL-STD-883, *as a minimum*.

- Major changes on MIL-M-38510 devices shall be as defined in MIL-M-38510 and qualification requirements as specified in MIL-M-38510.
- Qualification test reports shall be retained for a *minimum* period of five years.

REFERENCES

Spec Number	Title
06-04-0001	Quality Assurance/Reliability Assurance Qualification Requirements
06-04-0006	Qualification of Changes on 38510 Products
06-04-0011	Reliability Monitor Program
06-04-0012	QR² (Quick Reaction Reliability) Program

APPENDIX B—MAJOR CHANGE NOTIFICATION

- The major change definitions and requirements per MIL-M-38510 for military products, LTC's major change requirements for commercial products, and specific customer change requirements shall be fully documented by the Quality Assurance group.
- The responsible Engineering group and/or Quality Assurance group is responsible for initiating a major change via an ECN processed through the Document Control group. Appropriate qualification and test data justifying the major change shall support the ECN.
- The Quality Assurance and Reliability manager is responsible for maintaining a database of customers who require major change notification.
- The Quality Assurance and Reliability manager is responsible for ensuring that a major change is not implemented until customers who have major change notification requirements are notified and have approved the major change.
- The Quality Assurance and Reliability manager is responsible for sending the customer appropriate qualification and test data justifying the major change and for maintaining a record of all customer major change notifications.

REFERENCES

Spec Number	Title
06-04-0007	Customer Notification of Major Changes
06-04-0006	Qualification of Changes on 38510 Products

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APPENDIX C—ENVIRONMENTAL CONTROL

- The Facilities and Maintenance departments are responsible for control of following items to support the manufacture of integrated circuits:

  Temperature and humidity control

  Controlled filtered air hoods

  Airborne particle control

  De-ionized (DI) water

  Gases

  Clean dry air

- It shall be the responsibility of the Facilities Engineering and Maintenance departments to establish and maintain the necessary equipment and controls to provide the services listed above.
- It shall be the responsibility of the Facilities Engineering and Maintenance departments to define and document the requirements for such facilities based on the requirements of the various product groups.
- It shall be the responsibility of the Quality Assurance and Systems Quality Audit departments to monitor the quality of these services listed above.
- The Quality and Reliability Assurance department shall perform a periodic surveillance of the environmental controls.
- Surveillance inspection records shall be maintained by Quality Assurance and shall include *as a minimum* a monthly report of hood/area temperature, humidity and particle count, and DI water bacteria count and resistivity.
- Surveillance inspection records shall be maintained for a minimum of *five years*, per MIL-M-38510.

REFERENCES

Spec Number	Title
06-08-0002	Controlled Environment Surveillance
06-08-0004	Deionized Water Monitor
06-01-0016	Incoming Inspection: Gases
01-07-0001	MPS: Gases
06-01-0005	Incoming Inspection: Chemicals
01-65-0001	MPS: Chemicals

ıPPENDIX D—MILITARY STANDARD CROSS REFERENCE MATRIX

ɔ-09-0005 ɛction Number	Quality System Element	ISO 9001 1994	MIL-Q-9858	MIL-I-45208	MIL-I-38535 Appendix C	MIL-STD-45662
ɛface	Quality Policy	4.1.1	N/A	N/A	N/A	N/A
1.2	Organizational Chart	4.1.2	3.1	N/A	30.1.3.1	N/A
1	Management Responsibility	4.1.2.1-4.1.3	1.3	3.1	30.1	4.1
2	Quality System	4.2	1.3	3.1	30.1, 30.1.3	4.1, 5.1
3	Contract Review	4.3	3.2	N/A	30.1.1.1	N/A
4	Design Control	4.4	1.3	N/A	30.1.1.6	N/A
5	Document and Data Control	4.5	3.3, 4.1	3.2.1, 3.2.4	30.1.1.8, 30.1.2.4	5.5, 5.8
6	Purchasing	4.6	5.1, 5.2, 7.1	3.11.2, 3.11.3	30.1.1.1	5.11
7	Control of Customer Supplied Product	4.7	7.2	3.6	N/A	N/A
8	Product Identification and Traceability	4.8	6.1	3.5	30.1.1.12, 30.1.2	5.2, 5.10
9	Process Control	4.9	6.2	3.4	30.1.1.4, 30.1.2.6	N/A
10	Inspection and Testing	4.10	6.1-6.3, 7.1	3.1, 3.10-3.12	30.1.1.3, 30.1.1.5, 30.1.1.6, 30.1.1.12	N/A
11	Control of Inspection, Measuring, and Test Equipment	4.11	4.2-4.5	3.3	30.1.1.9, 30.1.2.5	5.2, 5.4
12	Inspection and Test Status	4.12	6.7	3.5	30.1.2.2	5.10
13	Control of Nonconforming Product	4.13	6.5	3.7	30.1.1.10	5.6
14	Corrective and Preventive Action	4.14	3.5	3.2.3	30.1.1.11	5.6, 5.7
15	Handling, Storage, Packaging, and Delivery	4.15	6.4	N/A	30.1.1.14	5.12
16	Control of Quality Records	4.16	3.4	3.2.2	30.1.2, 30.1.2.2	5.9
17	Internal Quality Audits	4.17	N/A	N/A	40.3.1	5.7
18	Training	4.18	N/A	N/A	30.1.1.2, 30.1.2.1	N/A
19	Servicing (Failure Analysis)	4.19	3.5	N/A	30.1.1.10, 30.1.2.3	N/A
20	Statistical Techniques	4.20	6.6	3.9	30.1.1.3	N/A
21	Quality Cost	N/A	3.6	N/A	N/A	N/A
ıpendix A	Reliability Assurance	N/A	N/A	N/A	N/A	5.4
ıpendix B	Major Change Notification	N/A	N/A	3.1	30.1.2.4	5.6
ıpendix C	Environmental Control	N/A	6.2	N/A	30.1.1.7	5.3

INTRODUCTION

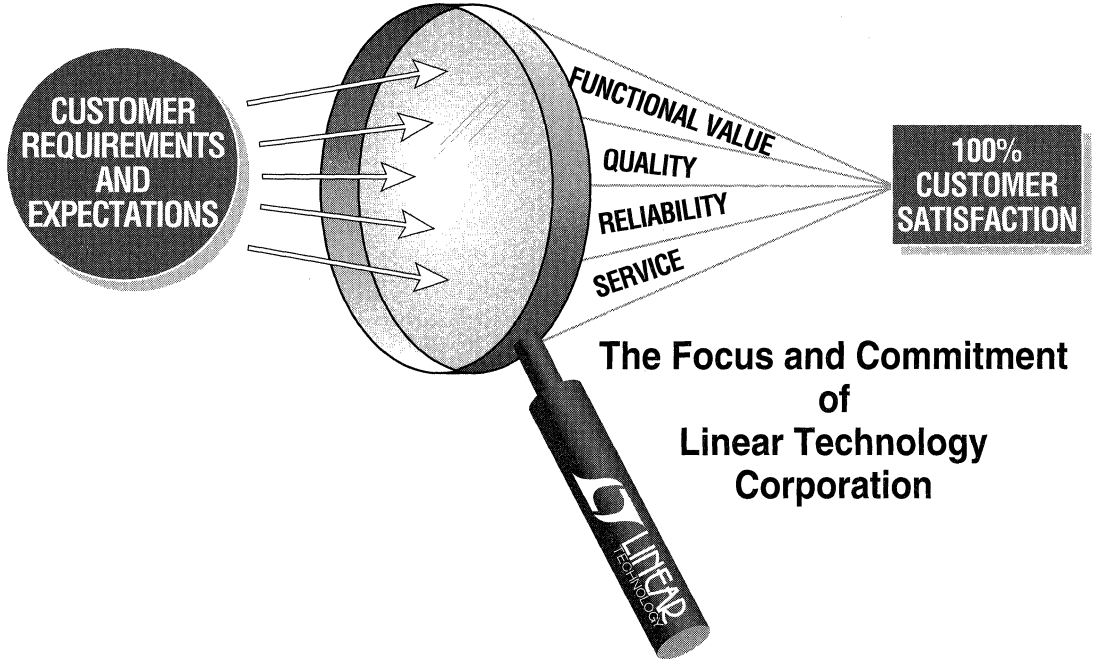
In 1981 Linear Technology Corporation was founded with the intention of becoming a world leader in high performance analog semiconductors. To achieve this goal Linear Technology Corporation committed itself to consistently meet its customers' needs in four areas:

- ❒ Functional Value
- ❒ Quality
- ❒ Reliability
- ❒ Service

Linear Technology Corporation has achieved its primar goal and is now focused to achieve 100% custome satisfaction.

This brochure defines the key elements of Linear Technolog Corporation's Reliability Assurance Program which is divide into three groups:

- ❒ Reliability Planning
- ❒ Manufacturing for Reliability
- ❒ Reliability Assessment and Improvement



ELIABILITY PLANNING

eliability planning takes three forms at Linear Technology orporation (LTC). The first is the establishment of the liability requirements for a product to be released to anufacturing. The second is the definition and mplementation of a predictive reliability system. The third is esigning for reliability, which includes new product evelopment, materials selection, and construction chniques.

'e fully realize that the cost of failure in the field is many 'ders of magnitude more than the initial component cost. nerefore, the goal of the reliability planning process is to 'ovide reliable product to reduce the cost of ownership to ır customers.

eliability Criteria

key element of reliability planning is LTC's internal ecification entitled "Quality Assurance/Reliability ssurance Qualification Requirement." It contains a complete escription of the interrelationships of the various groups volved in meeting LTC's reliability objectives and defines e guidelines for release decisions which affect quality and liability of the device.

redictive Reliability System

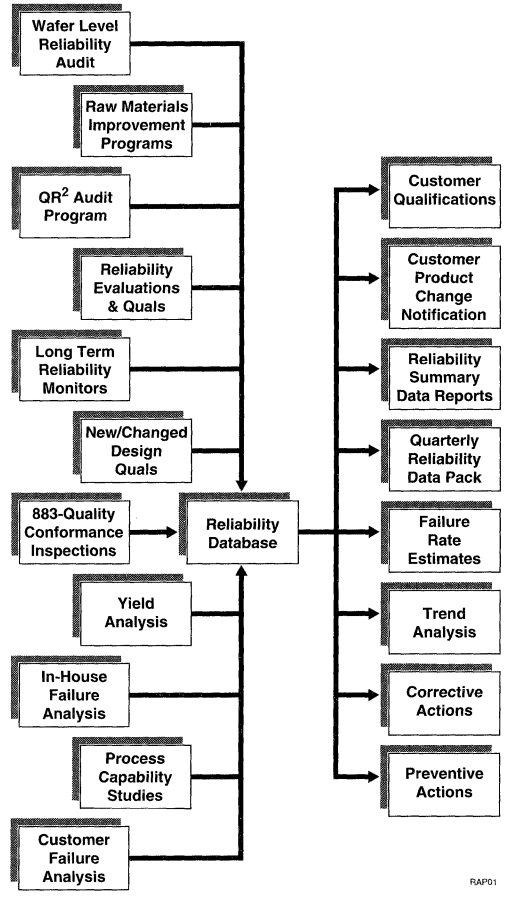
TC has developed a predictive reliability system which mbines quality and reliability information in a database to ovide reliability summaries and trend analysis. A block agram of the system is shown on this page.

esigning for Reliability

nsiderable planning goes into the design of LTC's products. iis planning includes device layout considerations, selection input and output protection schemes, selection of fab ocessing technology, and specification of materials and anufacturing techniques.

stringent set of bipolar and CMOS design rules have been tablished to enhance reliability and optimize anufacturability through robust design. At the design age the reliability of the circuit is heavily dependent ı layout considerations. The rules for thickness and width metallization have been defined to minimize the current nsity and prevent electromigration. Current density lculations are required to be performed on all products to sure that the designs are conservative. The routing of the etal pattern is designed to eliminate potential inversion or akage failures and guard ring structures are used where propriate. The positions of bonding pads are carefully selected to optimize device performance and also to fit easily into a variety of packages without creating potential bond loop problems that could result in shorted wires.

The Predictive Reliability System

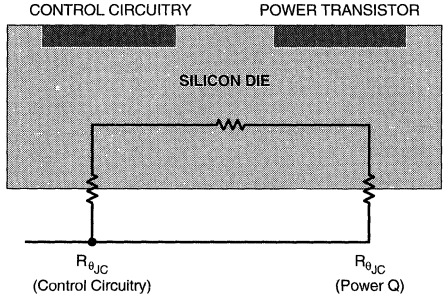


The thermal layout of our circuits also receives considerable attention to minimize parametric drift and optimize performance. In the case of voltage regulators, for any given power dissipation, there will be some temperature difference between the power transistor and the control circuitry due to their separation on the die. This temperature difference is a desirable situation which is used to reduce the power transistor's temperature effect on the control circuitry. Additionally, the power transistor has a higher maximum

junction temperature rating than that of the control circuitry and may be allowed to run warmer without degradation. Such LTC products are also designed for maximum efficiency to reduce power dissipation and thereby improve reliability and reduce the cost of heat sinking in the customer's product.

All of our voltage regulators include thermal limiting in the circuitry to shut down the device if the temperature exceeds the safe operating conditions. Additional insurance is provided by employing short-circuit current protection to safeguard against catastrophic failure. The philosophy of incorporating fault-tolerant designs with innovative circuit protection concepts is a fundamental design rule at LTC.

Thermal Resistance Model of LTC's Voltage Regulators



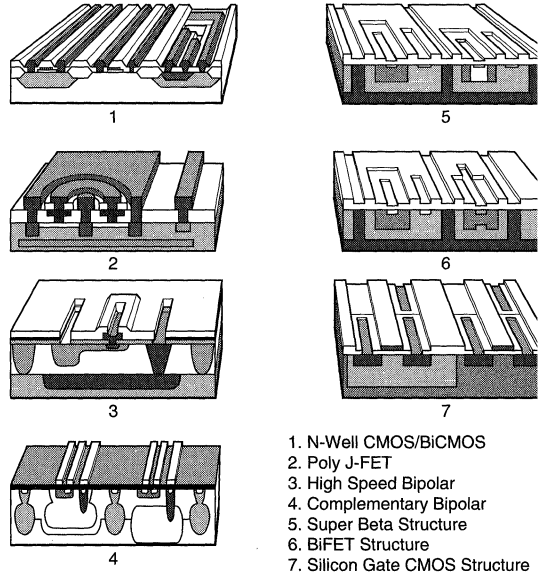
Another major design consideration in circuit reliability is tolerance to electrostatic discharge (ESD) and electrical overstress (EOS). ESD is a problem encountered both in normal handling and circuit assembly. It also affects the reliability of the final product when cables are exposed to ESD such as in line drivers and receivers.

The implementation of ESD protection structures in linear integrated circuits is much more difficult than in digital circuits. The linear circuit must provide protection for electrical overstress while maintaining the ability to measure current levels in the picoamp range. Interface circuits have input and output connections that normally operate at voltages in excess of the power supply, thereby precluding the use of clamp structures to the power supply for ESD protection. LTC, using a combination of circuit design and proprietary structures, provides high levels of overstress immunity to its devices which enhances their reliability. As a goal, all devices are designed for a minimum of 2,000V ESD protection with some devices achieving 5,000V to 10,000V ESD protection.

Linear circuits with total supply currents in the microam range cannot tolerate leakages induced by contaminatior Whether the circuit is bipolar, CMOS or complementar bipolar, the circuit must withstand high operating voltag and high temperature for thousands of hours without leakag currents degrading device performance. LTC uses advance process techniques to shield the die from sodiur contamination while preventing electron accumulatio causing surface inversions. This, combined with continuou monitoring of the assembly process, ensures high reliabilit devices.

LTC utilizes state-of-the-art processes in manufacturing it products. Our high voltage bipolar process provides hig gain, low noise general purpose devices as well as hig power integrated circuits. CMOS can provide high complexit ICs with a large digital content. Complementary bipolar, new process developed in-house by LTC, provides hig speed NPNs and PNPs on the same monolithic die Complementary bipolar enables an expanded product rang for linear circuits and is suitable for very high speed amplifiers general purpose linear signal processing or even high spee D/A converters. All of these products are characterized b high reliability, low power consumption and the ability t operate from a wide range of power supplies and over a wid range of ambient temperatures.

LTC's Process Structures



1. N-Well CMOS/BiCMOS
2. Poly J-FET
3. High Speed Bipolar
4. Complementary Bipolar
5. Super Beta Structure
6. BiFET Structure
7. Silicon Gate CMOS Structure

In order to ensure that device performance and reliability goals are achieved on new products, design review meetings are held regularly during the design and development phase.

Material Selection

LTC has selected assembly processes and materials that are closely matched to achieve the highest reliability level in both ultra-precision and high power devices. Compatibility between the different package elements, such as the molding compound and lead frame, are carefully researched and qualified. The choice of materials and assembly processes is especially critical in surface mount devices, which must maintain reliability after being subjected to harsh board soldering environments. At LTC we are using the latest state-of-the-art assembly equipment and materials to guarantee reliability. Our low stress epoxy molding compound is extremely low in ionic impurities.

Similar improvements have been made in hermetic packages in the modern low temperature glass ceramic seals and improved die attach materials.

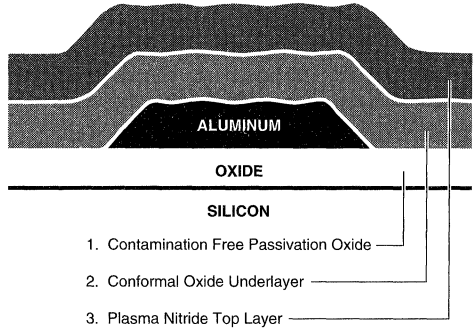
To protect the die from degradation before assembly, and from the long term effects of the package environment, LTC has developed a proprietary dual layer passivation. This dual layer passivation system is free from cracks and pinhole defects and offers an outstanding moisture barrier without detrimental side effects to device performance.

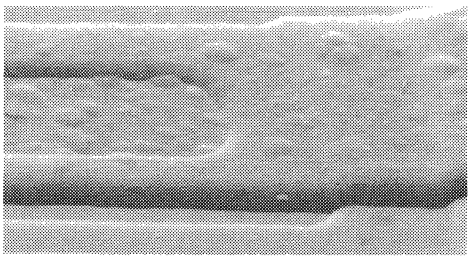
Design of Experiments

LTC is committed to the use of design of experiments (DOE) when developing new products and processes. We firmly believe that design of experiments will be the new industry standard for product and process development.

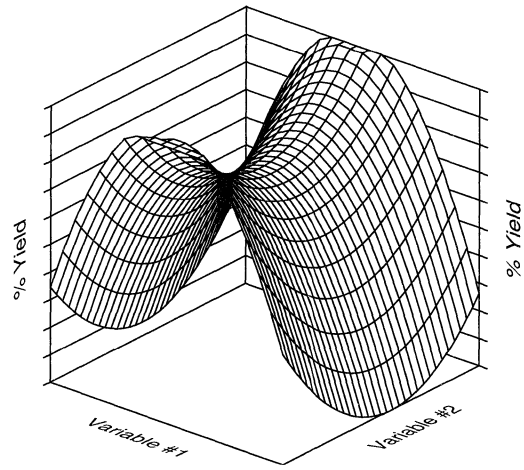
DOE has been successfully utilized on numerous products and processes at LTC. DOE, coupled with response surface methodology, has provided LTC the ability to solve complex problems that were previously unsolvable. We have used DOE to characterize wafer fab processes and provided this information to our IC designers which enabled them to produce devices that were less sensitive to manufacturing variations.

LTC's Dual Layer Passivation System





Response Surface Model of PIND Yield after Welding Operation



MANUFACTURING FOR RELIABILITY

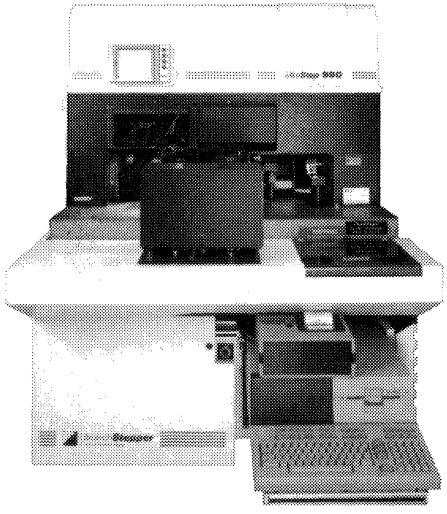
LTC is keenly aware of the influence which the manufacturing process has on the quality and reliability of the finished product. For this reason, LTC has placed critical emphasis on the manufacturing facility and associated process controls. LTC's claims of outstanding manufacturing capability and controls are validated by the fact that we achieved Class S Certification by DESC in November of 1987.

LTC's strategy in manufacturing for reliability includes the use of automated state-of-the-art equipment, protection of the product as it moves through manufacturing, effective inspection and screening, device traceability and statistical process control. These and other similar tight controls are applied from wafer fabrication through product shipment.

Wafer Fab

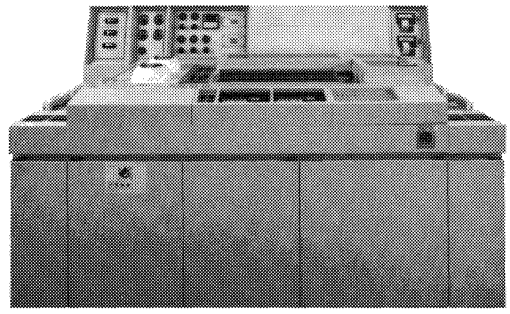
In wafer fabrication, the key to a reliable process is process control. Two major thrusts of process control in the wafer fab are the application of statistical process control (SPC) and the use of automated processing equipment. Automated equipment employing cassette-to-cassette wafer transfer, proximity mode aligners and projection steppers has significantly reduced handling related defects.

Projection Stepper



Microprocessor-controlled furnaces are used to eliminate the effects of process variations and human errors. Thin film processing employs fully automated sputtering and metal etch systems.

Automated Metal Etch System



All of these equipment enhancements work together to yield a process that is consistent and repeatable with a minimum of wafer handling. Quality control monitors and inspections at various points in the process, coupled with the use of control charting throughout the fab area, ensure consistent processing. The quality of the oxide is checked regularly using CV plots to check for contamination and surface state anomalies. Scanning electron microscope inspection is performed periodically each day to ensure the integrity of the metallization system.

Assembly

The introduction of new equipment and techniques in the assembly process has had a tremendous impact on device reliability. The use of automated equipment has reduced the handling and subsequent damage of die and wafers. In situations where die or wafers must be handled, vacuum wands and vacuum pens have replaced tweezers and thereby decreased damage due to scratches. Automated wire bonding machines have produced more consistent wire bonding quality and improved productivity.

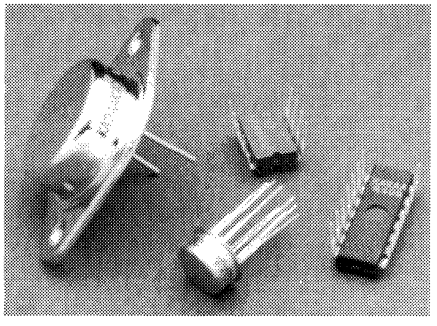
All products receive a thorough visual inspection per Mil-Std-883 Method 2010 Condition B or an equivalent visual criteria prior to encapsulation.

High Speed Automatic Bonder

Traceability

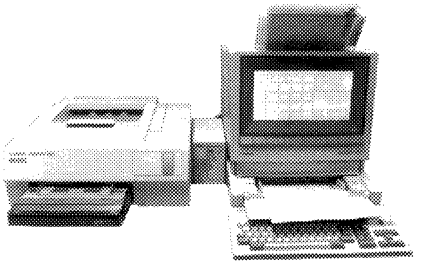
LTC has an outstanding traceability control system. A backside mark or a side mark is used to code information including the country of assembly, assembly facility, exact assembly or seal date, wafer fab lot, die type and revision. Additionally, this backside mark will identify any nonstandard processing which may have been required using a custom flow. At the wafer level, each wafer is laser-scribed to include the fab run number and wafer serial number. This traceability benefit is offered as a standard feature on all packages where space allows and is part of the "added value" of LTC products.

Traceability Control Using Backside Mark or Side Mark Coding



To enhance traceability LTC is using the latest state-of-the-art document archival system. This computerized system incorporates a document scanner which digitizes and compresses documents to be stored on optical disks. As the documents are stored, their ID number, date and classification are recorded in the system's database to facilitate retrieval. This system allows fab travelers, test travelers and other critical documents to be retrieved in minutes as opposed to hours or days.

Optical Disk Archive System



Reliability Screening

Although our standard product families are recognized for their very low infant mortality, customer-requested additional reliability screening can be provided by LTC. This added reliability screening for commercial or industrial level products is offered for both hermetic and plastic devices and is designated as our "R" flow process signified by a /R symbol as a suffix to the part number.

The "R" flow includes temperature cycle, burn-in and QA testing at 0°C, 25°C, and 70°C. A simplified flow chart of the "R" flow is shown in Table 1 at the end of the Reliability Assurance Program section. The hermetic devices are also offered as JAN Class S or Class B, Standardized Military Drawings (SMDs) and also as MIL-STD-883 devices.

LTC offers a cost-effective reliability screen for hermetic product using the MIL-STD-883 screening and quality conformance inspection. This flow is defined in our "MIL-STD-883" brochure and depicted in a brief flow diagram shown in Table 2.

The MIL-STD-883 burn-in at 125°C for 160 hours is roughly equivalent to 80,000 hours or approximately 9 years of continuous operation at a normal operating temperature of around 55°C (assuming an activation energy of 1.0 electron volts).

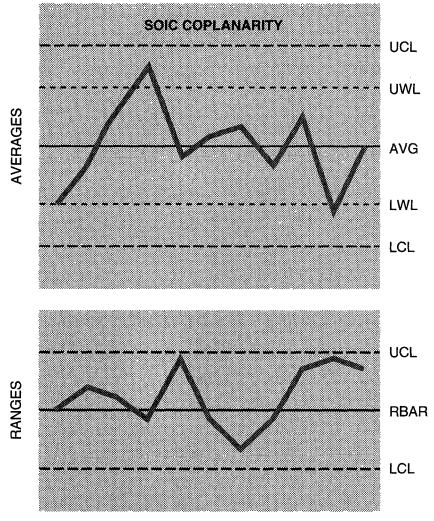
Whether testing plastic or hermetic devices, the engineers at LTC routinely add tests in addition to the standard data sheet tests. These added tests are used to detect potential flaws that could impact reliability and provide additional device compatibility with subtle application-related performance characteristics. Examples of such additional tests are the exercising of thermal shutdown mode of regulators prior to burn-in or the stressing of on-chip capacitors with voltages in excess of the device maximum rating to induce failure in substandard lots.

Data sheet electrical parameters are measured before and after the specified stress testing to ensure the electrical integrity of the devices.

Statistical Process Control

At LTC we believe that quality and reliability should be built into a product as opposed to simply screening out bad devices. Statistical process control (SPC) is ideally suited to our manufacturing goals. SPC has enabled us to run processes with uniform and centered distributions which have not only optimized yields, but have also produced a finished product that is rugged and reliable.

Example of Control Chart for SOIC Coplanarity



Control charting at all critical processes is used to identify the need for corrective action before an out-of-control situation occurs, thus reducing the overall process variation. LTC has an active SPC program. The generic process from wafer fabrication through shipping has been flow-charted with critical nodes defined. The Control Plan Detail outlines the various attributes of the activities surrounding that particular activity. Organization for SPC is comprised of the:

- Steering Committee
- SPC Quality Control Teams (QCTs)
- Process/Preventive Action Teams (PATs)

The Steering Committee provides the leadership for the SPC process, while the QCTs are responsible for the implementation and maintenance of SPC within their respective operational groups. PATs are formed by the QCTs to implement certain initial or corrective measures with specific stated goals using SPC tools. There are four QCTs in place:

- Wafer Fab
- Quality and Reliability
- Local Assembly
- End-of-Line (which includes Test, Mark, Pack, Product and Test Engineering)

Since, by definition, a PAT functions until its stated goal is attained, their number and tasks are constantly changing. We have had as many as 23 active PATs which include operators and maintenance personnel.

Training is provided in-house for a majority of LTC's employees, who receive test materials and 135 to 279 hours of instruction in one or more of the following courses:

- Basic SPC
- Advanced SPC
- Design of Experiments
- Team Organization

An important aspect of the SPC program at LTC involves the use of Design of Experiments to solve specific problems, develop new products/processes, and characterize new products and/or processes.

LTC is driving SPC beyond our own factory. A Preferred Supplier Program has been implemented with our raw materials suppliers, wherein parameters deemed critical to the manufacturing process at LTC are controlled statistically by the raw material supplier. Evidence of this control is supplied to LTC on a regular basis. This system of customer-supplier cooperation ensures the integrity of the materials and maintains a mutual focus on improvement.

RELIABILITY ASSESSMENT AND IMPROVEMENT

LTC combines a traditional approach to reliability which incorporates product qualification and long term reliability assessment with a "leading edge" approach, which incorporates wafer level reliability testing and in-line assembly reliability monitoring.

Qualification Testing

Before a new product can be released to production, strict qualification testing requirements must be met. These same qualification requirements apply to new processes, new materials, new designs and major changes in any of these areas. The guidelines for qualification of process or product changes are detailed in MIL-M-38510. At LTC we adhere to those guidelines and in many cases impose additional testing per our own requirements. Examples of some of the qualification tests which are used by LTC are shown in Table 3 at the end of the Reliability Assurance Program.

As part of new product qualification, LTC performs ESD sensitivity classification testing of devices to Method 3015 of MIL-STD-883. This ESD sensitivity testing uses both the human body model and the machine model. During this rigorous testing, every pin combination on at least three devices is subjected to three positive pulses followed by three negative pulses at the specified voltage increment with a one-second cool down period between pulses. Following this ESD testing, the device is tested for opens or shorts on a curve tracer and then must pass the full data sheet limits on the automatic test equipment.

Additionally for CMOS circuits, latch-up testing is performed on every pin to determine the device's ability to source or sink current without destructive latch-up. We require new LTC products to handle increasingly high currents without latch-up and subsequently meet all data sheet parameters.

Reliable radiation-hardened devices are produced by LTC using a proprietary process technology designed to meet or exceed 100k RADS total dose. Qualification testing of these devices using a Cobalt 60 source has demonstrated excellent results on a number of products. Data sheets for our RAD-hard product line are available from your local sales representative.

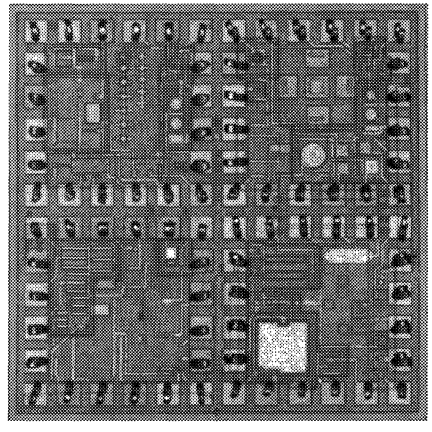
Wafer Level Reliability Assessment

As an additional reliability control, LTC has innovated a strategy for auditing the wafer fab process. Diagnostic structures, in addition to the device structures, are specifically designed as either bipolar or CMOS reliability test patterns and are stepped into all wafers. These structures are tested during fabrication using a parametric analyzer. Then these test vehicles are used to investigate and detect potential yield and reliability hazards after assembly.

The bipolar process version of this structure is optimized to accelerate, under temperature and bias, the two most common failure mechanisms in linear circuits; mobile positive ions and surface charge-induced inversions. This three-terminal structure is scribed from a wafer and assembled in either a hermetic or plastic package. These devices are burned in for a predetermined temperature and time. The same structures becomes sensitive to either failure mechanism depending upon the bias scheme used during burn-in. A limit is defined for the leakage current change during burn-in; a failure indicates a wafer fab problem which will be addressed by the process engineering group.

The CMOS process version allows measurements of thresholds of various sizes and kinds of N-channel and P-channel MOSFETs. Body effects, L effective, sheet resistance, zener breakdown voltage, contact metal resistance and impact ionization current are measurable with this chip which is assembled in a 20-lead DIP.

Bipolar Test Pattern



Electrical testing is performed on the structure before and after burn-in. After evaluating any sample population shifts or failures, process engineering is apprised of the results of this process monitor.

The use of test patterns allows any device to be monitored and also gives faster unambiguous feedback than is normally achieved by performing reliability testing on assembled product. Reliability data is generated in less than one week, giving immediate feedback to the production line.

LTC utilizes this new reliability control technique in addition to the conventional reliability audit on randomly pulled finished product. Operating Life tests are performed and the distributions of key parameters before and after testing are evaluated for stability and control.

Quick Reaction Reliability Monitor

As a complement to the wafer level reliability program, a monitor program focused on assembly-related issues has been fully implemented. This reliability monitor program, known as the Quick Reaction Reliability (QR^2) monitor, has been specifically tailored to provide quick feedback of reliability assessment of the assembly operation. The tests in the QR^2 program are designed to identify reliability weaknesses associated with wire bonding, die attach, package encapsulation and contamination-related failures. The actual tests performed in the QR^2 Monitor Program are shown in Table 4.

In order to ensure that representative reliability assessment is made, the QR^2 sampling matrix requires QR^2 testing of every date code from each assembly location on each package type and lead count from that assembly location. This provides a weekly snapshot of the reliability of all packages from all assembly locations. The basic strategy is to evaluate as many production lots as possible to provide maximum confidence to our customers.

Should a failure occur during QR^2 testing, the entire production lot is impounded before shipment. Failures are analyzed to determine validity and the root cause of any valid failure. Quite often additional samples are pulled and tested for an extended period of time. Lots with substandard reliability performance are scrapped. The data generated from this program is used to establish a program for continuous quality improvement with our assembly facilities.

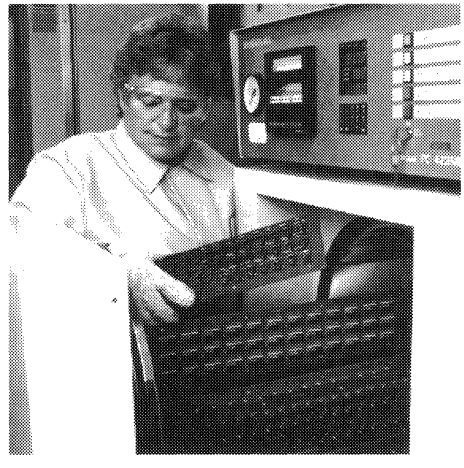
Long Term Reliability Monitor

LTC also conducts a traditional long term reliability monitor program on devices pulled from Boxstock. This long-term reliability monitor is used for extended life and end-of-life approximations such as Failure in Time (FIT) calculations. The long term reliability monitor also serves as a check against our short-term reliability estimates.

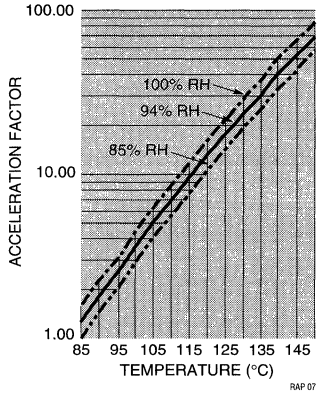
The long-term reliability tests are designed to evaluate design, wafer fab and assembly-related weaknesses. Industry standard reliability tests and the relatively new Highly Accelerated Stress Test (HAST) have been incorporated into this program. The long term reliability monitor tests are shown in Table 5.

The most severe tests for plastic package devices are the temperature and humidity tests, particularly HAST testing. We have included HAST testing in the long-term reliability monitor program due to the highly accelerated nature of this test. This test accelerates the penetration of moisture through the external protective encapsulant or along the interface between the encapsulant and the metallic lead frame. Additionally, the HAST test is conducted with the device under bias. The HAST test places the plastic devices in a humid environment of 85% relative humidity under 45psi of pressure at 130°C to 140°C. Under these conditions, 24 hours of HAST testing at 140°C is roughly equivalent to 1,000 hours of 85°C/85% RH testing. The employment of HAST testing has dramatically reduced the length of time required for qualification.

Qual Samples Being Loaded into the HAST System



Acceleration Factor Using HAST Compared to 85/85



Group C and D Testing

Since LTC is a certified producer of JAN 38510 and 883 product, we perform Group C and D testing regularly on our devices. This data is also incorporated into the reliability datapack (consult LTC). The Group C and D test lists are shown in Tables 6 and 7.

Failure Analysis and Corrective Action

LTC is extremely concerned with all failures whether they occur in-house or at a customer location. We have focused significant resources in the area of failure verification and analysis.

LTC offers failure analysis services to its customers, free of charge. In an emergency situation a preliminary failure analysis report can be issued within 24 hours. Our failure analysis database revealed that the vast majority of all devices returned for failure analysis are invalid due to improper application, gross misuse, or they are fully functional and meet all data sheet parameters. LTC also offers outstanding applications assistance to help the customer achieve the full value of our products.

Scanning Electron Microscope with X-RAY Dispersive Analysis

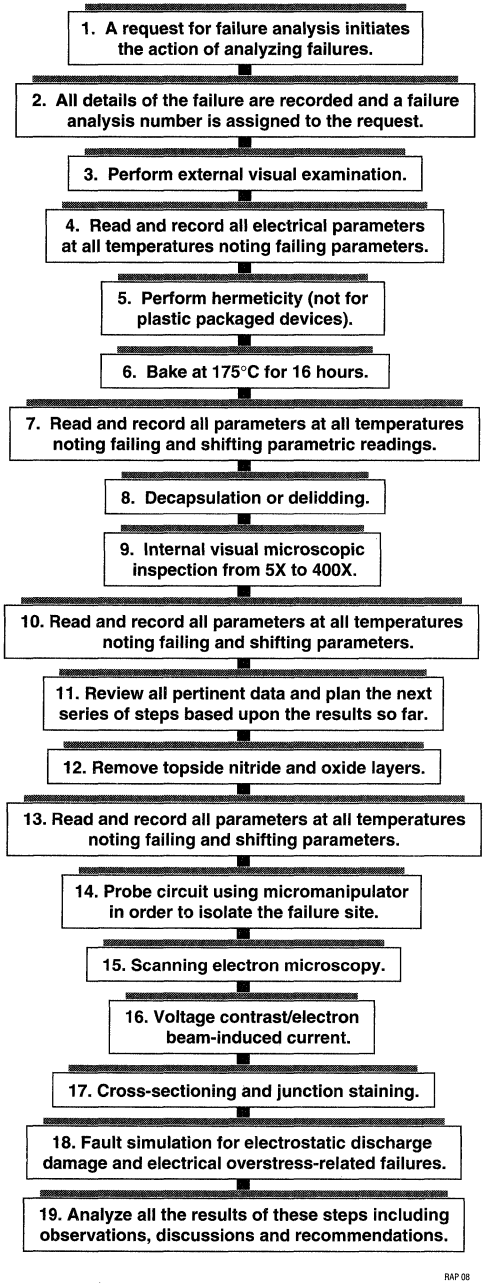
We are equally concerned with failures that are identified during reliability and qualification testing. As with field failures, the in-house failures are analyzed in detail to pinpoint the exact failure mechanism and to identify the root cause. In many cases where ESD or EOS is the suspected cause of the failure, fault simulation is carried out by over-stressing good devices to recreate the fault condition.

LTC has invested in failure analysis resources in the form of experienced, seasoned engineers, and equipment such as a full metallurgical lab, IC deprocessing equipment and a scanning electron microscope with voltage contrasts, Electron Beam-Induced Current (EBIC), Energy Dispersive X-ray Analysis (EDAX), and a computerized database.

All failure analysis reports are documented in detail and distributed appropriately. All valid failure analyses require prompt and effective corrective action which is driven to completion by the quality and reliability organization.

Corrective actions are implemented in accordance with LTC's internal document "Corrective Action Procedure" which details the method and responsibilities for timely corrective action. This procedure is summarized in a separate brochure which is available to our customers upon request.

Typical Failure Analysis Flow



RAP 08

Failure Rate Calculations

Failure rates at LTC are calculated using MIL-STD-690B which is based upon the exponential distribution model for predicting microelectronic device reliability. Examples of FIT and Mean Time Between Failure (MTBF) are shown in the sample calculation below.

Sample Calculation:

Step 1. Calculate Failure Rate at Test Condition (150°C).

Assume 77 units of Op-Life for 1000 hours with Ø failures:

Device Hours at Test Condition = 77 Units × 1000 Hours equals 77,000 Device Hours at 150°C

$$\text{Fail Rate} = \frac{\text{Value from Table A-1(MIL-STD-690B)}}{\text{Device Hours}}$$

$$= \frac{91{,}641}{77{,}000} = 1.19\%\ 1\text{k Hours}\ (11{,}900\ \text{FITs})$$

The Arrhenius model is used to extrapolate a failure rate from an accelerated test condition to a use temperature condition.

Step 2. Calculate Acceleration Factor and Extrapolate Equivalent Failure Rate to 55°C.

Af = Acceleration Factor

$$Af = e^{\frac{E_a}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

$$Af = e^{\frac{E_a}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)}$$

$$Af = e^{\left(\frac{1.0}{0.0000863}\right)\left(\frac{1}{328} - \frac{1}{423}\right)}$$

$$Af = 2791$$

Where:

E_a = Activation Energy (Assume 1.0 eV)
K = Boltzmann's Constant = 8.63 X 10^{-5} eV/°Kelvin
T_2 = Test Condition Temperature in °Kelvin
T_1 = Use Condition Temperature in °Kelvin
e = 2.71828 (Natural Antilog)

Now the equivalent failure rate is calculated:

$$\text{Failure Rate (55°C)} = \frac{\text{Failure Rate at Test Condition}}{\text{Acceleration Factor}}$$

$$= \frac{11{,}900\ \text{FITs}}{2791}$$

$$= 4.2637\ \text{FITs}$$

Finally MTBF is calculated:

$$\text{MTBF} = \frac{100{,}000}{0.000426} = \frac{234{,}700{,}000\ \text{Hours}}{\text{or } 26{,}778\ \text{Years.}}$$

Reliability Datapack

On a quarterly basis, the reliability department compiles and publishes a report which summarizes all the reliability testing results. This report is intended to provide our customers with a means of determining system reliability. The data is presented at 150°C and at 125°C for those customers who wish to perform their own failure rate calculations. Contact LTC for this report.

In addition, up to the minute reliability summary data reports on particular devices can be generated from the computerized reliability database. ESD simulation testing reports and current density calculations of individual device types are also available upon request.

Should you desire additional information, please contact your local LTC representative.

Table 1. "R" Flow for Plastic Dual-In-Line Packages

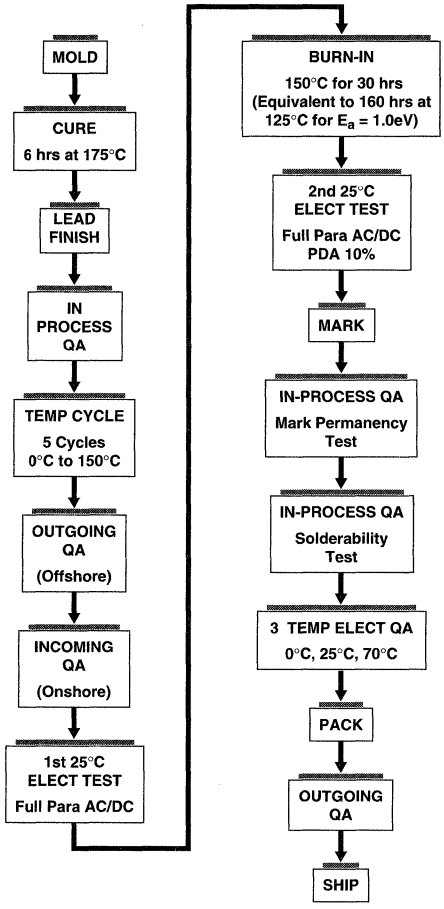


Table 2. Screening Flow per MIL-STD-883, Method 5004

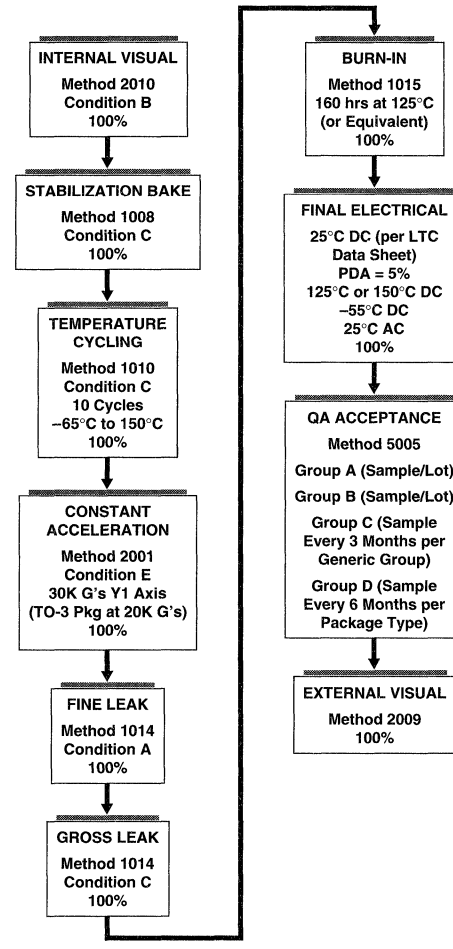


Table 3. Reliability Qualification Test Guidelines for Plastic Packages

TEST	METHOD	CONDITIONS	FULL RELEASE DURATION	CONTINGENT RELEASE DURATION	FULL AND CONTINGENT RELEASE LTPD
High Temperature Bias Operating Life (Op-Life)	MIL-STD-883 Method 1005	Continuous Operation at Max Rated Supply Voltage T_A = 125°C or T_A = 150°C	 1000 Hours 500 Hours	 500 Hours 168 Hours	 5%, A_{CC} = 0 5%, A_{CC} = 0
Temperature Humidity Bias Life (85/85)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current T_A = 85°C, 85% RH	1000 Hours	500 Hours	5%, A_{CC} = 0
Highly Accelerated Stress Test (HAST)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current T_A = 140°C, 85% RH, 3 Atmospheres	Equivalent to 1000 Hours 85/85	Equivalent to 500 Hours 85/85	5%, A_{CC} = 0
Temperature Cycle (T/C)	MIL-STD-883 Method 1010 Condition C	Air-to-Air, –65°C to 150°C, >10 Minutes Dwell Time	1000 Cycles	500 Cycles	5%, A_{CC} = 0
Thermal Shock (T/S)	MIL-STD-883 Method 1011 Condition C	Liquid-to-Liquid, –65°C to 125°C, > 5 Minutes Dwell Time	1000 Cycles	500 Cycles	5%, A_{CC} = 0
Autoclave (Pressure Pot with Bias) (BPPT)	JEDEC Spec 22	Continuous Storage at T_A = 105°C, 100% RH, 1.67 Atmospheres, Max Rated Supply Voltage for the Last 3 Hours	350 Hours	350 Hours	5%, A_{CC} = 0
Autoclave (Pressure Pot without Bias) (PPT)	JEDEC Spec 22	Continuous Storage at T_A = 121°C, 100% RH, 2 Atmospheres	350 Hours	350 Hours	5%, A_{CC} = 0
Power Cycle (PW) Regulators Only	MIL-STD-883 Method 1006	Power Cycled "ON" and "OFF" as Required to Cycle Case Temperature Between 60°C and 120°C	50,000 Cycles	10,000 Cycles	15%, A_{CC} = 0
Thermal Resistance (TMLR)	MIL-STD-883 Method 1012 Condition C	Junction to Case or Junction to Ambient as Appropriate	N/A	N/A	15%, A_{CC} = 0
Dye Penetrant (DY)	MIL-STD-883 Method 1014	Immersion in Dye Penetrant at 60 PSIG for 2 Hours Minimum	N/A	N/A	15%, A_{CC} = 0
X-Ray Inspection Radiography (XRAY)	MIL-STD-883 Method 2012	Top View Only	N/A	N/A	15%, A_{CC} = 0

Table 4. Quick Reaction Reliability (QR^2) Monitor Program

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Operating Life Test (Op-Life)	MIL-STD-883 Method 1005	Continuous Operation at Max Rated Supply Voltage, T_A = 125°C or T_A = 150°C	168 Hours	45	5%, Acc = 0
Biased Moisture Life Test (85/85)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = 85°C, 85% RH	168 Hours	45	5%, Acc = 0
or					
Highly Accelerated Stress Test (HAST)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = 140°C, 85% RH, 3 Atmospheres	48 Hours	45	5%, Acc = 0
Temperature Cycle (T/C)	MIL-STD-883 Method 1010 Condition C	Air-to-Air, –65°C to 150°C, >10 Minutes Dwell Time	100 Cycles	45	5%, Acc = 0
Thermal Shock (T/S)	MIL-STD-883 Method 1011 Condition C	Liquid-to-Liquid, –65°C to 150°C, >5 Minutes Dwell Time	100 Cycles	45	5%, Acc = 0
Autoclave (Pressure Pot without Bias) (PPT)	JEDEC Spec 22	Continuous Storage at T_A = 121°C, 100% RH, 2 Atmospheres	48 Hours	45	5%, Acc = 0
X-Ray Inspection Radiography (XRAY)	MIL-STD-883 Method 2012	Top View Only	N/A	45	5%, Acc = 0
Package Separation Visual Inspection	N/A	30X Magnification	N/A	45	5%, Acc = 0
Unmolded Strip Evaluation	N/A	30X Magnification	N/A	1 Strip	N/A
Hot Intermittent Opens Test at Subcontractor	N/A	Automated Electrical Test at 125°C	N/A	250	N/A

Table 5. Long-Term Reliability Monitor Program

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Operating Life Test (Op-Life)	MIL-STD-883 Method 1005	Continuous Operation at Max Rated Supply Voltage, T_A = 125°C or T_A = +150°C	1000 Hours	45	5%, Acc = 0
Biased Moisture Life Test (85/85)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = 85°C, 85% RH	1000 Hours	45	5%, Acc = 0
or					
Highly Accelerated Stress Test (HAST)	JEDEC Spec 22	Continuous Operation at Max Rated Supply Voltage, Min Supply Current, T_A = 140°C, 85% RH, 3 Atmospheres	48 Hours	45	5%, Acc = 0
Temperature Cycle (T/C)	MIL-STD-883 Method 1010 Condition C	Air-to-Air, –65°C to 150°C, >10 Minutes Dwell Time	1000 Cycles	45	5%, Acc = 0
Thermal Shock (T/S)	MIL-STD-883 Method 1011 Condition B	Liquid-to-Liquid, –65°C to 50°C, >5 Minutes Dwell Time	1000 Cycles	45	5%, Acc = 0
Autoclave (Pressure Pot without Bias) (PPT)	JEDEC Spec 22	Continuous Storage at T_A = 121°C, 100% RH, 2 Atmospheres	1000 Hours	45	5%, Acc = 0

Table 6. Group C per MIL-STD-883C Method 5005

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Group C-1 Operating Life Test (Op-Life)	MIL-STD-883 Method 1005	Continuous Operation at Max Rated Supply Voltage T_A = +125°C or T_A = +150°C	 1000 Hours 500 Hours	45	5%, Acc = 0

Table 7. Group D per MIL-STD-883C Method 5005

TEST	METHOD	CONDITIONS	TEST DURATION	SAMPLE SIZE	LTPD, ACC NO.
Group D-1 Physical Dimensions	MIL-STD-883 Method 2016	N/A	N/A	15	15%, Acc = 0
Group D-2 Lead Integrity	MIL-STD-883 Method 2004	Condition B2 (Lead Fatigue)	N/A	15	15%, Acc = 0
Group D-3 Thermal Shock Temperature Cycle Moisture Resistance Hermeticity Visual Exam End Point Electricals	MIL-STD-883 Method 1011 Method 1010 Method 1004 Method 1014 Method 1004/10	 Condition B Condition C	 15 Cycles 100 Cycles	15	15%, Acc = 0
Group D-4 Mechanical Shock Vib. Variable Frequency Constant Acceleration Hermeticity Visual Exam End Point Electricals	MIL-STD-883 Method 2002 Method 2007 Method 2001 Method 1014 Method 1010/11	 Condition B Condition A Condition E (Y1 Only)	N/A	15	15%, Acc = 0
Group D-5 Salt Atmosphere Hermeticity Visual Exam	MIL-STD-883 Method 1009 Method 1014 Method 1009	 Condition A	 24 Hours	15	15%, Acc = 0
Group D-6 Internal Water Vapor	MIL-STD-883 Method 1018	 < 5000ppm	N/A	3	0
Group D-7 Adhesion of Lead Finish	MIL-STD-883 Method 2025	N/A	N/A	15	15%, Acc = 0
Group D-8 Lid Torque	MIL-STD-883 Method 2024	(Glass Frit Seal Only)	N/A	5	15%, Acc = 0

At Linear Technology Corporation (LTC) our overriding commitment is to achieve excellence in Quality, Reliability and Service (QRS) and total customer satisfaction. We interpret the word "excellence" to mean delivering products that consistently exceed all the requirements and expectations of our customers. The commitment to QRS extends from the president to every employee, from design to product qualification, and from manufacturing to shipping. To meet this commitment, LTC has established a comprehensive program called "Quality for the Nineties."

This program is divided into four separate, but highly interrelated programs; Quality Environment, Total Quality Management System (TQMS), Vendor Participation, and Focus for the Nineties.

Quality Environment

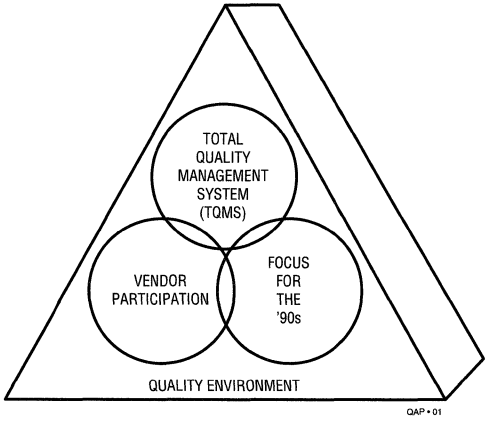
The first program, Quality Environment, serves as the building block for three other programs. It entails establishing an environment that is conducive to the participation of each and every employee in helping to build quality into our products. This program encourages every employee to identify any quality problem and participate in recommending solutions.

A comprehensive operator training and certification program has been established that covers every area of manufacturing from incoming raw material inspection, wafer fabrication, assembly, and test to shipping. Emphasis is placed on compliance with specifications, statistical process control (SPC) performance to quality goals, electrostatic discharge damage (ESD) awareness and controls, encouraging operators to think quality and recommend quality improvement ideas.

To ensure compliance with specifications, a Quality Audit Team performs a systems audit of key manufacturing areas and suppliers at periodic intervals. Compliance with process specifications and the detailed programs of the Corporate ISO9001 Quality Policy are verified, and discrepancies reported for quick resolution with special emphasis to eliminate recurring problems. The performance of each area is then rated, providing a strong incentive for each area to excel.

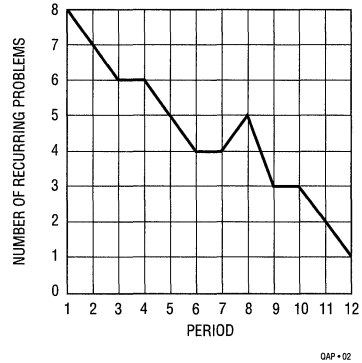
With the philosophy that each department, starting from incoming raw materials, is considered a customer of the preceding department, every effort is made by working closely together to meet or exceed our end-customer requirements and goals.

Quality for the '90s



QAP • 01

Systems Quality Audit-Tracking Recurring Problems



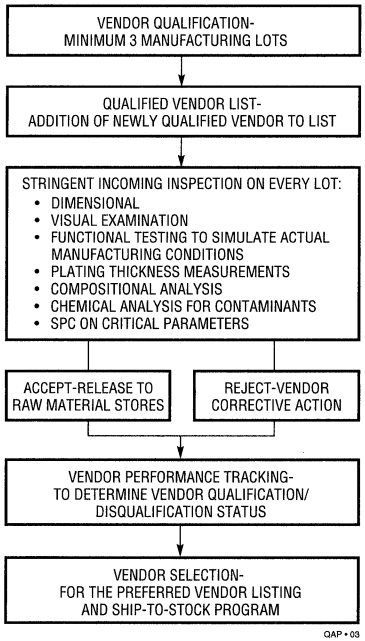
QAP • 02

Total Quality Management System (TQMS)

The second program starts with the incorporation of innovative but conservative design and layout rules to achieve the best performance without sacrificing quality and reliability. During the design and development cycle, design, product, package, manufacturing, quality and reliability engineering groups participate in design reviews to ensure that all program aspects are covered, ranging from product performance objectives to ensuring reproducibility and repeatability in wafer fabrication and assembly. Special emphasis is placed on devising input protection circuitry to minimize susceptibility to voltage spikes and ESD, optimizing thermal layout to minimize parametric drift, and optimizing bond pad layout to maximize assembly and electrical test yields, at the same time allowing the die to be assembled in a wide selection of packages.

Once the design is approved, a stringent manufacturing qualification test plan is conducted on the initial engineering runs. The test plan is selected to bring out any weaknesses in the design and any manufacturability problems, and includes reliability stress tests such as high temperature Operational Life and HAST (Highly Accelerated Stress Testing) for plastic packages, and MIL-STD-883 method 5005 qualification testing for hermetic packages. Product performance on these tests must be equal to or better than similar products within the same generic group to be considered qualified. Major design, package, material and process changes are also subjected to these same stringent qualification requirements. In addition to achieving the required reliability performance, an engineering change must also achieve manufacturing yield and quality performance levels equal to or better than the original product to be considered qualified. A major change control procedure is in place to notify customers of major changes for approval prior to implementation when required.

Raw Material Controls

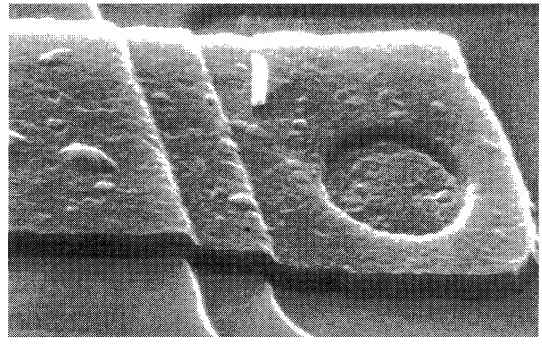


QAP • 03

In manufacturing, process controls start with vendor qualification on raw material piece parts. A Qualified Vendor List is maintained and performance of each vendor is continuously monitored on a Vendor Rating Program. A dimensional, visual, functional and, where applicable, compositional analysis is performed on each direct raw material lot. Automated state-of-the-art wafer fabrication, assembly and test equipment, cassette-to-cassette handling in wafer fabrication and automated handling in assembly are utilized, where possible, to maintain manufacturing consistency and quality. Only fully trained and certified operators are allowed to work on production material.

Stringent statistical process controls, typically beyond industry standards, are established for each critical manufacturing step in wafer fabrication, wafer test, assembly,

SEM Monitor of Metallization Quality



package finishing, mark and pack and shipping as depicted in the Wafer Fabrication, Assembly,Test and End-of-Line flowcharts.

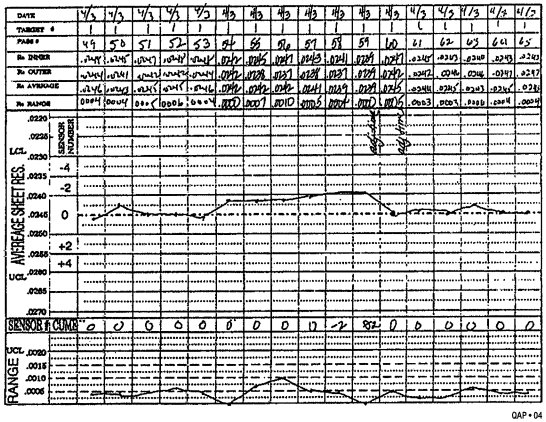
The process controls include monitors of critical assembly processes and lot acceptance inspection for operations requiring 100% production inspection. Preseal visual inspection is performed per MIL-STD-883 Method 2010 Test Condition B. Statistical process control techniques are employed in optimizing process parameters, and monitoring process performance through the use of control charts with action limits and upper and lower control limits, and in parametric distribution analysis at electrical test.

Electrical quality is guaranteed by conservative guardbanding on production test programs of a minimum of three machine guardbands, by using state-of-the-art test equipment and 0.04% AQL for lot acceptance testing at 25°C for all military and commercial lots. Additional tests, like rack burn-in, beyond the data sheet specifications on regulator products are performed by exercising the parts in a thermal shutdown mode. These tests are incorporated into the test flow to improve reliability and weed out infant mortality failures. Visual and mechanical quality is optimized by minimizing handling of parts in assembly, test and end-of-line operations. Lead finish processes have been selected that minimize solderability problems and all lots are subjected to a stringent major visual/mechanical inspection. Administrative errors due to mixed and wrong parts are minimized by strictly adhering to a one lot per station policy, and double-checking orders at order entry and shipping. Before shipment of a lot to the customer each lot is inspected to ensure that it meets internal and customer specifications and purchase order requirements. The level of attention paid to each unit is demonstrated by the fact that each unit is traceable to the wafer fabrication lot number via a side or back mark on both 883 and commercial products on all packages, except where there is a physical constraint.

Through the use of automated equipment, strict process controls (utilizing proven statistical process control techniques), periodic systems and quality audits (conducted by the Quality Audit Team), stringent facilities and environmental controls and monitors, LTC is able to ensure that quality is built into the product and to guarantee a consistently high quality level.

The manufacturing quality controls are complimented by a reliability audit program designed to weed out design, fabrication, packaging and assembly deficiencies. Additionally, controls are supported by a comprehensive failure analysis and corrective action program designed to provide timely feedback of findings to all operating groups for resolution. The analysis of customer returns, and corrective action taken, completes the closed loop of our Total Quality Management System.

Actual $\bar{X}$ and R Chart of Aluminum Sputter Deposition Using Sensor Number Control

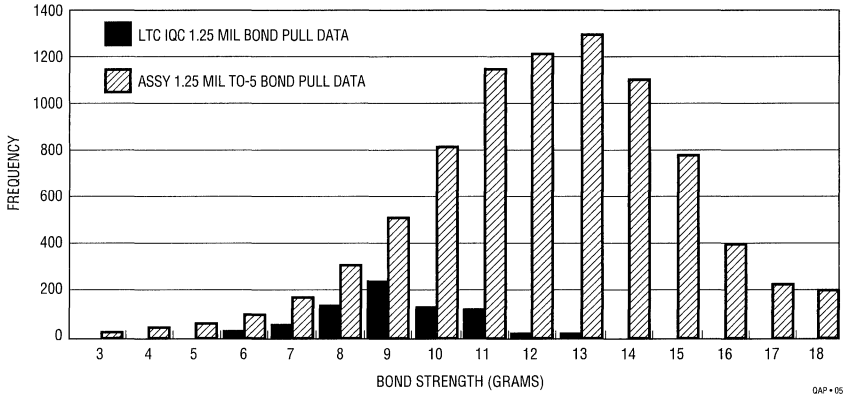


QAP • 04

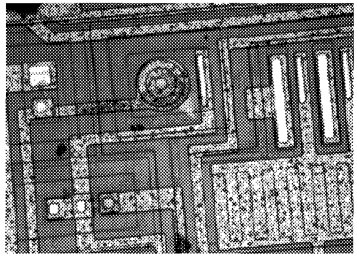
Military and Commerical Products Share the Same Stringent Inspections and Controls

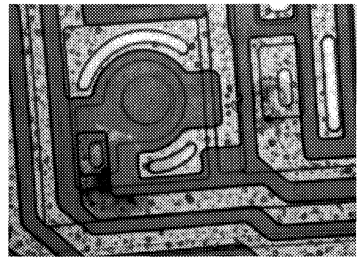
- WAFER FABRICATION PROCESS CONTROLS AND CLASS 100 PROCESSING.
- REGULAR SEM MONITORS.
- PRE-SEAL VISUAL INSPECTION PER MIL-STD-883 METHOD 2010. TEST CONDITION B.
- DIE SHEAR TEST PER MIL-STD-883 METHOD 2019.
- BOND PULL TEST PER MIL-STD-883 METHOD 2011.
- SOLDERABILITY TEST PER MIL-STD-883 METHOD 2003.
- MARK PERMANENCY TEST PER MIL-STD-883 METHOD 2015.
- HERMETICITY TESTING PER MIL-STD-883 METHOD 1014.
- QA ELECTRICAL TEST TO 0.04% AQL AT 25°C, AND TEMPERATURE TESTING.
- EXTERNAL VISUAL PER MIL-STD-883 METHOD 2009.

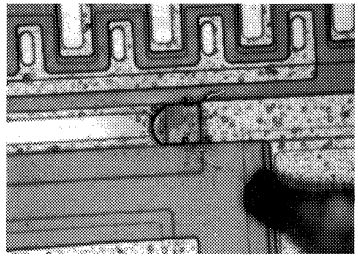
Bond Strength Histogram

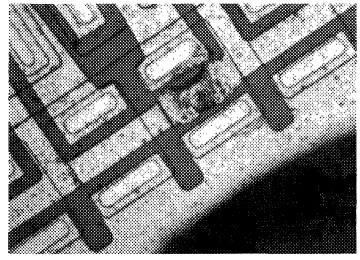


Failure Analysis Photomicrographs









Vendor Participation

The requirements of high quality raw materials for integrated circuit manufacture range from ppb (parts per billion) impurity levels for electronic grade chemicals to ppm (parts per million) defective levels for lead frame packaging materials. It is not only essential, but critical for the semiconductor manufacturer to work closely with its vendors to attain the high quality levels needed in raw materials. At LTC a program has been established and implemented to allow vendor participation in formulating specifications and establishing percentage defective and lot rejection rate goals. This vendor participation ensures that the direct and raw material quality levels received are consistent with our manufacturing and end-product quality goals. Clearly, achieving optimum quality product requires the use of the best possible materials available and with continuous communication and feedback from our vendors to improve in this key area. A Preferred Vendor Program helps to drive vendors to manufacturing excellence.

Focus for the '90s

The following key quality improvements programs have been established to meet the quality requirements of the '90s.

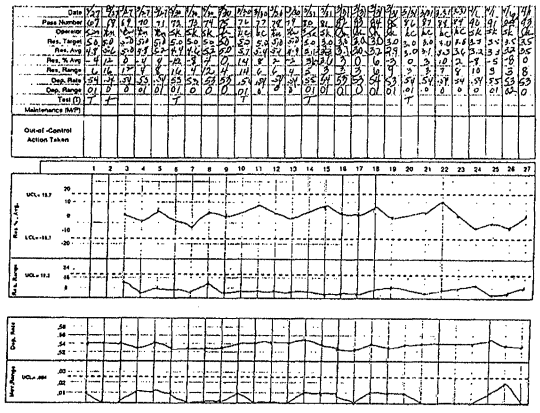
PPM Goals

As demand for quality semiconductor components becomes increasingly more stringent, the percentage goals from the 1970s have given way to ppm goals in the '80s and '90s. At LTC ppm quality goals are established for every major operation, from incoming inspection to customer returns. Performance to goals is reviewed quarterly and, where goals are not met, quality improvement programs are defined and implemented. Quality goals are updated and tightened on an annual basis, and quality programs are redefined to achieve the new goals established. One of the early benefits of this program is demonstrated by the excellent average outgoing electrical quality (AOQ).

Statistical Process Control (SPC)

The increased reliance on automated manufacturing and test equipment underlines the need for strict process control techniques. SPC is a valuable tool and at LTC we realize the importance of these methods. Engineering analysis is performed regularly using SPC techniques to establish the process capability. Various variable and attribute control charts are used to ensure that processes are within normal limits and action and shutdown limits are established for critical operations. The process capability of key processes are calculated using the Cpk capability index on an ongoing basis to ensure a program for continuous quality improvement.

Actual Normalized X and Moving R Chart of Epitaxial Growth Reactor Controlling Resistivity and Deposition Rate

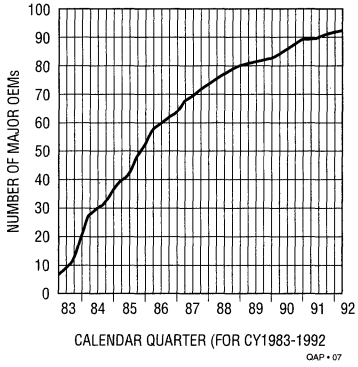


QAP • 06

ESD Control

A comprehensive ESD control program has been established which encompasses design, handling, testing, storage and final packaging for shipment. The program includes the use of grounded table tops, floor mats, wrist straps and heel straps, topical antistatic treatment of floor coverings, banning of static bearing materials from the manufacturing environment, ionizers, and use of conductive or antistatic materials for handling and final packaging. Areas where ESD control must be enforced are designated as ESD Protected areas. ESD awareness training programs help to increase the operator's awareness for successful implementation of this program. Every effort is made to stamp out this silent chip killer. The benefits of this program are improved quality and reliability to the customer.

Quality System Surveys MIL-Q-9858 and MIL-I-45208 Approval



Based on the foregoing quality programs, Linear Technology Corporation is positioned to continuously improve its product quality and exceed the demands of its customers in the '90s and beyond.

ISO 9001 Certification

Realizing the importance of the ISO 9000 international standard for quality management, LTC received ISO 9001 certification in 1993 covering the company's design, manufacturing and service organizations. This has also helped to solidify customer confidence that they are dealing with a manufacturer with a proven international quality system.


TÜV CERT

CERTIFICATE

The TÜV-Zertifizierungsgemeinschaft e.V.
hereby certifies that

Linear Technology Corporation

Milpitas, CA

has established and applies
a quality system for

Design and manufacturing of a broad line of
high performance linear integrated circuits

An audit was performed, Report No. 9008
Proof has been furnished that the requirements according to

DIN ISO 9001 / EN 29001

are fulfilled

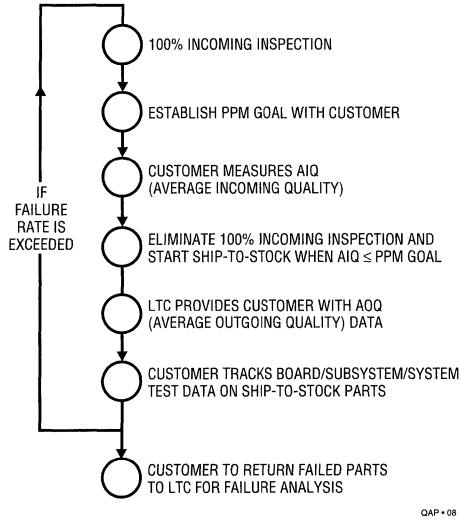
The certificate is valid until
March 31, 1998
Certificate Registration No.
08 100 9008

TÜV Rheinland Gruppe

Customer Ship-To-Stock Program

LTC is working hand-in-hand with customers to consistently supply high quality products to achieve a ship-to-stock program by eliminating the need to do an incoming inspection. We recognize the benefits to our customers of a ship-to-stock program, namely, savings in the need to purchase and maintain incoming test equipment, savings in the need to maintain a safety stock in case of incoming lot rejections, and reduction in board failures and rework costs because of higher component quality.

Ship-To-Stock Program Flow

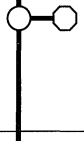
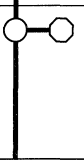


WAFER FABRICATION FLOWCHART
Generic Bipolar Process

Vendor: Linear Technology Corporation
Package: Plastic SOIC/DIP
Location of Wafer Fab: Linear Technology Corporation, Milpitas, CA
Assembly: Carsem Unisem Penang Malaysia, ASAT Hong Kong
Final Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Q.C. Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Source Accept Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Quality Contact: QA Manager, LTC, Milpitas, CA
(408) 432-1900

▽ INCOMING
◇ QUALITY INSPECTION AND GATE
○ MANUFACTURING PROCESS
⬡ QUALITY MONITOR/SURVEILLANCE
□ REWORK

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
▽	Incoming Raw Material Inspection	Wafers	Visual: Scratches, Pits, Haze, Craters, Dimples, Contamination,	1X Inspection	1.0% AQL to 2.5% AQL Level 1	% LAR Trend Chart and % Defective Trend Chart
			Oxygen/Carbon Measurement	Infrared Spectrometer	S/S = 2, A_{CC} = 0	$\bar{X}$ and R
			Resistivity/ Conductivity	Magnetron V/I Meter	S/S = 2, A_{CC} = 0	$\bar{X}$ and S
			Dimensional	Calipers	2.5% AQL, Level S1	X and Moving R Run Chart
			Thickness and Taper/Bow	Dial Thickness Gauge	2.5% AQL, Level S1	
			Orientation	Break Test	S/S = 1, A_{CC} = 0 Each Batch	
			C of C Verification Against "MPS" Requirements			
○		Photo Mask Plates	Visual C.D. Measurement	AMS-100 Calipers Comparator UV Lamp	Each Plate	Logbook
○		Chemicals	C of C Verification Against "MPS" Requirements		Each Batch	Logbook
		Gases	Plus Yearly Gas Analysis	Outside Lab		Logbook
		Targets	C of C Verification		Each Target	Logbook
○—◇	Initial Oxidation	Oxidation Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Logbook
			Oxide Thickness	Nanospec	3 Wafers/Cycle	
○—◇	Collector Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log
○	Collector Implant	Implant				Logbook

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Collector Diffusion	Oxidation and Diffusion Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field	Logbook
			Oxide Thickness	Nanospec	2 Wafers/Run	
			$R_{\square}$	4 Point Probe	1 Test Wafer/Run	
			XJ	Philtec Groove	1 Test Wafer/Cycle	
	EPI	Deposit EPI Gemini Reactor	Visual	UV Lamp	100% for EPI Spike More Than 5 Wafers is Reject	
				Interference Contrast Microscope	More Than 1 Slip and Stacking Fault is Reject	
			$R_{\square}$	4 Point Probe	2 Reading/Pass	X and Moving R
			EPI Thickness	Nicolet	2 Reading/Pass	Run Chart
	EPI Re-Ox	Oxidation Furnace	Visual	UV Lamp	100%	Logbook
				20X Microscope	2 Wafers/Run < 2 Defects/Field of View	
			Oxide Thickness	Nanospec	2 Wafers/Run	
	Isolation Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
	Isolation Predeposition	Boron Deposition Furnace	Visual	UV Lamp	100% < 10 Defects/ Wafer	Trend Chart
				20X Microscope	2 Wafers/Run < 4 Defects/Field of View	
			$R_{\square}$	4 Point Probe	2 Test Wafers/Run	
	Isolation Diffusion	Diffusion Furnace	Visual	UV Lamp	100% < 10 Defects/ Wafer	Logbook
				20X Microscope	2 Wafers/Run < 2 Defects/Field of View	
			$R_{\square}$	4 Point Probe	2 Test Wafers/Run	
			XJ	Philtec Groove	1 Test Chip/Run	Production Logbook
			TOX	Nanospec	2 Product Wafers/ Run	
	Sinker Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	
	Sinker Predeposition	Deposition Furnace	Visual	UV Lamp	100% < 10 Defects/ Wafer	Trend Chart
			$R_{\square}$	4 Point Probe	2 Test Wafers/Run	
	Sinker Diffusion	Diffusion Furnace	Visual	UV Lamp	100%	Logbook
				20X Microscope	< 3 Defects/Field of View	
			$R_{\square}$	4 Point Probe	2 Test Wafers/Run	
			TOX	Nanospec	2 Test Wafers/Run	

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FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Base Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	$\overline{X}$ and R
	ISO Diode Check	Curve Tracer BVCSO	BVCSO	Curve Tracer	4 Wafers/Run >1 Per 12 Readings Is Fail	Logbook
	Base Predeposition	Deposition Furnace	Visual	UV Lamp	100% < 10 Defects/ Wafer	$\overline{X}$ and R
				20X Microscope	2 Wafers/Run < 4 Defects/Field of View	
			$R_{\square}$	4 Point Probe	2 Test Wafers/Run	
	Base Diffusion	Diffusion Furnace	Visual	UV Lamp	100% < 10 Defects/ Wafer	Trend Chart
				20X Microscope	2 Wafers/Run < 4 Defects/Field of View	
			$R_{\square}$	4 Point Probe	2 Test Wafers/Run	
			TOX	Nanospec	2 Product Wafers/ Run	
	Emitter Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log
	CB Diode Check	Curve Tracer	BVCBO	Curve Tracer	< 1 Out of 16 Readings is Fail	Logbook
	Emitter Diffusion	Deposition Furnace	$R_{\square}$	4 Point Probe	2 Test Chip/Cycle	Logbook
			Beta/LV	Curve Tracer	3 Sites/Wafer Every Fourth Wafer > 2 Readings Out of Spec	
	Contact Mask	Resist Mask HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log
				Optical Microscope 1000X	Critical Dimension Measure. 2 Wafers/ Run Lot, Accept on 0 Failures	Trend Chart
	Metal Deposition	Deposition Sputter Machine	Visual	UV Lamp	< 5 Defects/Wafer 100%	$\overline{X}$ and R
			$R_{\square}$/Thickness	4 Point Probe	2 Readings/Pass	
	Metal Mask	Resist Mask Etchant Bath	Final Inspection	Optical Microscope 200X	"Z" Pattern Scan 100% of the Wafers	Production Log
				Optical Microscope 1000X	Critical Dimension Measure. 2 Wafers/ Run Lot, Accept on 0 Failures	CD Logbook

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Alloy	Anneal Furnace	Visual	UV Lamp	100% < 10 Defects/ Wafer	Logbook
	Electrical Test	To Evaluate Electrical Parameters LOMAC			2 Wafers/Run	Logbook
	LPOM	Passivation LPCVD Furnace	Visual	UV Lamp	100%, > 2 Color Changes is Fail	$\overline{X}$ and R
				10X Microscope	3 Wafers/Cycle < 3 Defects/Field of View	
			TOX	Nanospec	3 Wafers/Cycle	
			Phosphorous Concentration	10:1 HP Etch Rate	3 Wafers/Cycle	
	PEN	PECVD Nitride Deposition Furnace	Visual	UV Lamp	100%, >2 Color Changes Is Fail	Trend Chart
				10X Microscope	2 Wafers/Run, < 5 Defects/Field of View	
			Thickness	Nanospec	3 Wafers/Cycle	
			Index of Refraction	Elipsometer	3 Wafers/Cycle	
	Pad Mask	Resist Mask RF Plasma Etch and Oxide Wet Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan. 100% of the Wafers	Production Log
	Electrical Test	Evaluate Electrical Parameters			100%	Logbook
	Backlap	Disco.	N/A	N/A	N/A	Logbook
	Backside Metal	Backside Metallization	Visual	Unaided Eye	100%	Logbook
	SEM	Step Coverage	2 Photos	Scanning	1 Wafer/Week	Logbook
		General Metallization	1 Photo	Electron Microscope		

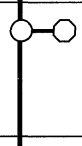
WAFER FABRICATION FLOWCHART
Generic CMOS Process

Vendor: Linear Technology Corporation
Package: Plastic SOIC/DIP
Location of Wafer Fab: Linear Technology Corporation, Milpitas, CA
Assembly: Carsem Unisem Penang Malaysia, ASAT Hong Kong
Final Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Q.C. Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Source Accept Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Quality Contact: QA Manager, LTC, Milpitas, CA
(408) 432-1900

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
▽	Incoming Raw Material Inspection	Wafers	Visual: Scratches, Pits, Haze, Craters, Dimples, Contamination,	1X Inspection	1.0% AQL to 2.5% AQL Level 1	% LAR Trend Chart and % Defective Trend Chart
			Oxygen/Carbon Measurement	Infrared Spectrometer	S/S = 2, A_{CC} = 0	
			Resistivity/ Conductivity	Magnetron V/I Meter	S/S = 2, A_{CC} = 0	
			Dimensional	Calipers	2.5% AQL, Level S1	
			Thickness and Taper/Bow	Dial Thickness Gauge	2.5% AQL, Level S1	
			Orientation	Break Test	S/S = 1, A_{CC} = 0 Each Batch	
			C of C Verification Against "MPS" Requirements			
○		Photo Mask Plates	Visual C.D. Measurement	AMS-100 Calipers Comparator	Each Plate	Logbook
				UV Lamp	Each Batch	Logbook
○		Chemicals	C of C Verification Against "MPS" Requirements			
		Gases	Plus Yearly Gas Analysis	Outside Lab	Each Target	Logbook
		Targets	C of C Verification			
○—○	Initial Oxidation	Oxidation Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/ Field of View	Logbook
			Oxide Thickness	Nanospec	3 Wafers/Cycle	
○—○	P-Well Mask	Resist Mask HF Etchant Bath	Visual	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log
○—○	Pre-Implant Oxidation	Oxidation Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/ Field of View	Logbook
			Oxide Thickness	Nanospec	3 Wafer/Cycle	

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	P-Well Implant	Implant				Logbook
	P-Well Drive	Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Logbook
			Oxide Thickness	Nanospec	3 Wafers/Cycle	
	Strip All Oxide	HF Etchant Bath				Logbook
	Pad Oxidation	Oxidation Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Logbook
			Oxide Thickness	Nanospec	3 Wafers/Cycle	
	Nitride Deposition	Nitride Furnace	Visual	UP Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Logbook
			Nitride Thickness	Nanospec	3 Wafers/Cycle	
	Active Mask	RF Plasma Etch	Visual Inspection Critical Dimensions	Microscope 400X	"Z" Pattern Scan 100% of the Wafers	Production Log
	Field Implant Mask	Resist Mask HF Etchant Bath	Visual Inspection	Microscope 400X	"Z" Pattern Scan 100% of the Wafers	Production Log
	Boron Field Implant	Implant				Logbook
	CMOS Strip Resist	RF Plasma Sulfuric Acid	Visual Inspection	Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Logbook
	N-Field Implant Mask	Resist Mask HF Etchant Bath	UV Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Production Log
			Visual Inspection	Microscope 100X	"Z" Pattern Scan 100% of the Wafers	
	Photo Field Implant	Implant				Logbook
	CMOS Strip Resist	RF Plasma Sulfuric Acid	Visual Inspection	Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Logbook
	LOCOS Oxide	Oxidation Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Logbook
			Oxide Thickness	Nanospec	3 Wafers/Cycle	
	Plasma Nitride Strip	RF Plasma Etch	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Logbook
	CMOS Cap Mask	Resist Mask HF Etchant Bath	Critical Dimensions	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log
	Cap Implant	Implant				Logbook
	CMOS Strip Resist	RF Plasma Sulfuric Acid	Visual Inspection	Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Logbook
	Etch Pad Oxide	HF Etchant Bath				Logbook

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Gate Oxide	Oxidation Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Logbook
			P-Channel Oxide Thickness	Nanospec	3 Wafers/Cycle	
			Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	
			N-Channel Oxide Thickness	Nanospec	3 Wafers/Cycle	
	VTP Implant Mask	Resist Mask HF Etchant Bath	Visual	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log
	Boron VT Implant	Implant				Logbook
	CMOS Strip Resist	RF Plasma Sulfuric Acid	Visual Inspection	Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Logbook
	Poly Deposition	Furnace	Poly Thickness			Logbook
	Back Etch Mask	Resist Mask RF Plasma and HF Etchant Bath	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Logbook
	Sinker Pre-Desposition	Deposition Furnace	Visual	UV Lamp (100%) 20X Microscope	100% < 10 Defects/ Wafer	Trend Chart
			RS (Ω/sq)	4 Point Probe	2 Test Wafers/Run	
	CMOS Gate Mask	Resist Mask RF Plasma and HF Etchant Bath	Visual Inspection	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log
	P + Implant Mask	Resist Mask	Visual Inspection	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log
	P and S/D Implant	Implant				Logbook
	CMOS Strip Resist	RF Plasma Sulfuric Acid	Visual Inspection	Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log
	N + Implant Mask	Resist Mask	Visual Inspection	Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Logbook
	N + S/D Implant	Implant				Logbook
	CMOS Strip Resist	RF Plasma Sulfuric Acid	Visual Inspection	Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Logbook
	Source Drain Re-Ox	Oxidation Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Logbook
			P + Oxide Thickness	Nanospec	3 Wafers/Cycle	
			Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	
			N + Oxide Thickness	Nanospec	3 Wafers/Cycle	

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	LPOE	LPOE LPCVD Furnace	Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Logbook
			LPOE Thickness	Nanospec	3 Wafers/Cycle	
	CMOS Getter	Furnace	RS (Ω/sq)	4 Point Probe	2 Test Wafers/Run	Trend Chart
	CMOS Contact Mask	Resist Mask HF Etchant Bath	UV Visual	UV Lamp (100%) 20X Microscope	2 Wafers/Run < 2 Defects/Field of View	Production Log
			Visual Inspection	Microscope 100X	"Z" Pattern Scan 100% of the Wafers	
	Aluminum Desposition	Deposition Sputter Machine	Visual	UV Lamp	< 5 Defects/Wafer 100%	Logbook
			RS (Ω/sq)	4 Point Probe	2 Test Chip/Cycle	
	CMOS Metal Mask	Resist Mask Metal Etchant Bath	Final Inspection Critical Dimensions	Optical Microscope 2 200X	"Z" Pattern Scan 100% of the Wafers	Production Log
				Optical Microscope 2 1000X	Critical Dimension Measure 2 Wafers/ Run Lot, Accept On 0 Failures	
	Alloy	Anneal Furnace	Visual	UV Lamp	100% < 10 Defects/ Wafer	Logbook
	Electrical Test	LOMAC Parametric Analyzer			2 Wafers/Run	Logbook
	LPOM	Passivation LPCVD Furnace	Visual	UV Lamp	100%, More Than 2 Color Change Is Fail	Trend Chart
				10X Microscope	3 Wafers/Cycle < 3 Defects/Field of View	
			LPOM Thickness	Nanospec	3 Wafers/Cycle	
			Phosphorous Concentration	10:1 HF Etch Rate	3 Wafers/Cycle	
	PEN	PECVD Nitride Deposition Furnace	Visual	UV Lamp	100%, More Than 2 Color Change Is Fail	Trend Chart
				10X Microscope	3 Wafers/Cycle < 5 Defects/Field of View	
			LPOM Thickness	Nanospec	3 Wafers/Cycle	
			Index of Refraction	Elipsometer	3 Wafers/Cycle	
	Pad Mask	Resist Mask RF Plasma Etch and HF Etchant Bath	Final Inspection	Optical Microscope 100X	"Z" Pattern Scan 100% of the Wafers	Production Log

FLOWCHART INCOMING FAB REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Electrical Test	LOMAC Parametric Analyzer			100%	Logbook
	Backlap	DISCO	N/A	N/A	N/A	Logbook
	Backside Gold	Backside Metallization	Visual	Unaided Eye	100%	
	SEM	Step Coverage	2 Photos	Scanning Electron Microscope	CMOS = 1 Wafer/ Week	Logbook
		General Metal	1 Photo		N-Well and P-Well = 1 Wafer Every Run	

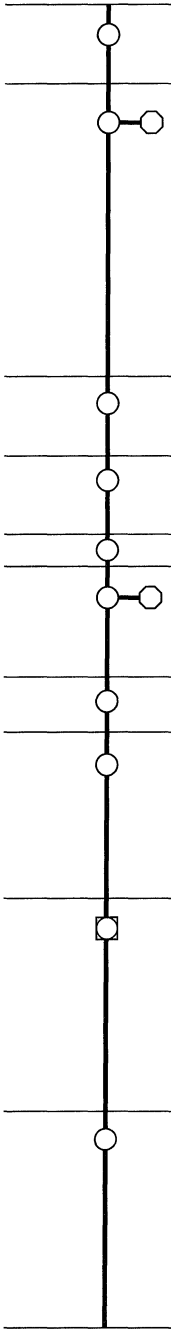
ASSEMBLY FLOWCHART
Generic CMOS or Bipolar Process

Vendor: Linear Technology Corporation
Package: Plastic SOIC
Location of Wafer Fab: Linear Technology Corporation, Milpitas, CA
Assembly: Carsem/Unisem/Penang-Malaysia, ASAT-Hong Kong
Final Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Q.C. Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Source Accept Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Quality Contact: QA Manager, LTC, Milpitas, CA
(408) 432-1900

▽ INCOMING
▣ QUALITY INSPECTION AND GATE
◯ MANUFACTURING PROCESS
◯ QUALITY MONITOR/SURVEILLANCE
□ REWORK

FLOWCHART INCOMING ASSY REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
▽	Incoming Raw Material Inspection	Wafers	Visual; Scratches Pits, Haze, Craters Dimples, Contamination	1X Inspection	1.0% AQL to 2.5% AQL Level I	% LAR Trend Chart and % Defective Trend Chart
			Oxygen/Carbon Measurement	Infrared Spectrometer	S/S = 2, ACC = 0	
			Resistivity/ Conductivity	Magnetron V/I Meter	S/S = 2, ACC = 0	
			Dimentional	Calipers		
			Thickness and Taper/Bow	Dial Thickness Gauge	2.5% AQL, Level S1	
			Orientation	Break Test	S/S = 1, ACC = 0	
			C of C Verification Against "MPS"		Each Bach	
		Chemicals	Requirements Plus yearly		Each Bath	
		Gases	Gas Analysis			
◯	Wafer Sort	100% Die Level Electrical Test Rejects Are Red Inked		Wafer Prober		
	Wafer Sort Monitor	Monitor Probing and 2nd Optical Quality	Probe Defects 2nd Optical Defects	3X to 75X Microscope	Minimum of 3 Times/Shift S/S = 1, ACC = 0	% Defective Trend Chart
◯	Kit for Overseas Assembly	Wafers Are Kitted with LTC Bonding Diagram and LTC Assembly Traveler				

FLOWCHART INCOMING ASSY REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Incoming Piece Parts Inspection	Lead Frame	Visual	10X to 30X Microscope	1% AQL, Level 2	% LAR Trend Chart
			Mechanical	Optical Comparator, Calipers, X-Ray Fluorescence		
			Functional (Assembly Process Simulation): Bond Pull Test Die Shear Test			
	Wafer Mount	Preparation for Die Separation	Visual Inspection	Unaided Eye	3 Wafers/Shift 0 PPM Target	Go/No Go Inspection
	Waver Mount Monitor					
	Wafer Saw	Die Separation	Alignment Accuracy	TV Alignment Micro Automation on Disco Saw 10X to 30X Microscope	Every Wafer/ Machine, 6 Cuts/ Wafer 0 PPM Target	nP Chart
	Wafer Saw Monitor	Saw KERF	Saw Quality Saw Accuracy	TM Microscope or Equivalent	Once/Shift 4 Cuts/Machine CPK 1.5 Target	$\bar{X}$ R Chart
	Die Attach	Die Bonded to Lead Frame with Epoxy	Visual Inspection	Auto Die Bonder	2 Strips/Mag 0 PPM	nP Chart
	Die Attach Monitor		Visual Quality Die Shear Test	10X to 30X Microscope Die Shear Tester	4 Units 1X/Machine/ Shift (or Per Customer Request)	Go/No Go
	Epoxy Cure		Epoxy Cure	Pyrometer/TC	1X/Machine/Shift CPK 1.5 Target	$\bar{X}$ R
	Wire Bond	Ball Bonds Gold 1.00 Mil Wire	Defects	Auto Thermosonic Ball Bonder		
	Wire Bond Monitor		Visual	Microscope	4 Strip/Mag 0 PPM	nP Chart
			Bond Pull Strength	Bond Pull Tester	10 Wires 1X/Machine/Shift CPK 1.5	$\bar{X}$ R Chart
			Ball Shear	Ball Shear Tester	10 Balls 1X/Machine/Shift CPK 1.5	$\bar{X}$ R Chart
			Cratering Test	Visual	4 Units/Day/Shift 0 PPM	Go/No Go
			Peel Test	Visual	10 Wires 1X/Machine/Shift 0 PPM	Go/No Go
	QA 3rd Optical Inspection	Check for Workmanship Quality Prior to Molding	Die, Die Bond, Wire Bond Visual Quality	30X to 60X Microscope	Every Lot AQL = 0.04% 0 PPM	

FLOWCHART INCOMING ASSY REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Mold	Encapsulation with Epoxy Novalac		Transfer Mold		nP Chart
	Mold Monitor	Molding Quality	Visual: Chip, Void and Cracks, Misalignment, etc.	Unaided Eye 0 PPM	7X/Shift/Machine 0 PPM	nP Chart
			Mold Temperature	Pyrometer	1X/Shift/Machine CPK 1.5	$\bar{X}$ R Chart
			Transfer Press	Hydr Load Cell	1X/Month/Machine 4 Strips (Min)	Go/No Go
			Voids/Wire Sweep Visual Quality	X-Ray	1X/Machine/Shift Change of Device Change of Compnd 0 PPM	nP Chart
	Mechanical Deflash	Remove Mold Flash from Package	L/F and Heat Sink Must Be Free from Mold Flash	3X to 10X Microscope	4 Strips (Min) 1X/Sublot/Machine 0 PPM	nP Chart
	Slurry Deflash	Remove Mold Flash from Package	L/F and Heat Sink Must Be Free from Mold Flash	Unaided Eye	10 Strips/4X/Shift/ Machine 0 PPM	nP Chart
	Marking					
	Marking Permanency Test	Visual Inspection	Visual	Unaided Eye	100% Inspect 0 PPM	Go/No Go
			MPT	Unaided Eye	10 Units/Sublot 0 PPM	Go/No Go
	Post Mold Cure	Mold Quality	Temperature	Pyrometer	1X/Machine/Shift CPK 1.5	$\bar{X}$ R Chart
	Solder Plate	Solder Plate Bath	Visual Inspection	Unaided Eye	5 Strips/4X/Shift 0 PPM	nP Chart
				Thermometer	1 Reading 2X/Shift CPK 1.5	
			Thickness and Composition	XRF	5 Frames/Shift CPK 1.5	$\bar{X}$ R Chart
	Solder Plate Inspection	Solder Plate Quality	Visual Inspection	Unaided Eye Solderability Tester	5 Units/Sublot 0 PPM	Go/No Go
			Steam Aging	3X to 10X Microscope	5 Units/Day/ Different Type of Package 0 PPM	Go/No Go
			Thickness and Composition	XRF	5 Readings/Sublot 0 PPM	Go/No Go
	Trim and Form Singulation	Visual Inspection	Visual	Unaided Eye	2 Tubes/Sublot 0 PPM	nP Chart
			Lead Gap/ Microcrack	3X to 10X Microscope	10 Units 1X/ Machine/Shift 0 PPM	Go/No Go
			Coplanarity	Jig and Microscope	6 Units/Machine Min 1X/Shift 0 PPM	$\bar{X}$ R Chart

FLOWCHART INCOMING ASSY REWORK	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	Final Visual	Visual	Mark, Correct Mark, Marking Permanency Test (If Ink Marked) Visual: Bent Leads Mold Flash, Solder Quality, Etc.	Unaided Eye	100% 0 PPM	Go/No Go
	Final Visual Inspection	Visual Quality	Mark, Correct Mark, Marking Permanency Test (If Ink Marked) Visual: Bent Leads Mold Flash, Solder Quality, Etc.	Unaided Eye	S/S = 15 ACC = 0	Go/No Go
	Pack	Packing and Preparation for Delivery		Antistatic Shipping Tube	Every Lot 100% Basis	
	Ship to LTC					

EOL (END-OF-LINE) FLOWCHART
Generic CMOS or Bipolar Process

Vendor: Linear Technology Corporation
Package: Plastic SOIC
Location of Wafer Fab: Linear Technology Corporation, Milpitas, CA
Assembly: Carsem/Unisem/Penang-Malaysia, ASAT-Hong Kong
Final Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Q.C. Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Source Accept Test: Linear Technology Corporation, Milpitas, CA, or Singapore
Quality Contact: QA Manager, LTC, Milpitas, CA
(408) 432-1900

▽ INCOMING
◯ QUALITY INSPECTION AND GATE
◯ MANUFACTURING PROCESS
◯ QUALITY MONITOR/SURVEILLANCE
□ REWORK

FLOWCHART	PROCESS STEP	DESCRIPTION	INSPECTION/ TEST CRITERIA	METHOD AND EQUIPMENT	SAMPLING PLAN	SPC TECHNIQUE
	LTC Incoming Inspection	Check Quality of Incoming Assembled Material	Package Dimension	Optical Comparator and Calipers	S/S = 2, A_{CC} = 0	% LAR Trend Chart
			External Visual	3X to 30X Microscope	S/S = 76, A_{CC} = 0	
			Mark Permanency (If Ink-Marked)	MIL-STD-883 Method 2015	S/S = 4, A_{CC} = 0	
			Solderability	MIL-STD-883 Method 2003	S/S = 3, A_{CC} = 0	
			Die Attach Quality	Pliers	S/S = 5, A_{CC} = 0	
			Lead Fatigue Test	Lead Fatigue Tester	S/S = 10, A_{CC} = 0	
	Class Test	Electrical Test	Test to Guard-Banded Data Sheet Test Limits	LTX Integrated Circuit Test System	100%	
	QA Electrical Test at 25°C	Electrical Quality	Test to Guard-Banded Data Sheet Test Limits	LTX Integrated Circuit Test System	S/S = 125, A_{CC} = 0	PPM Chart
	QA Electrical Test at 70°C and at 0°C	Electrical Quality	Test to Guard-Banded Data Sheet Test Limits	LTX Integrated Circuit Test System	S/S = 125, A_{CC} = 3	PPM Chart
	External Visual Inspection	Check for Package Quality	Visual: Bent Leads, Lead Form Criteria, Mold Voids/Cracks, etc.	3X Eyepiece	100%	Yield Chart
	QA Post Pack Inspection	Package/ Pack Quality Inspection	Verify Correct Top Mark, Correct Pack Method, Correct Labeling, External Visual Inspection	3X to 10X Microscope Inspection	S/S = 125, A_{CC} = 0	% LAR and PPM P.A. Chart
	QA Shipbench Inspection	Plant Clearance Inspection	Paperwork Check, Verify Correct Part Number and Correct PAR Count	Unaided Eye Inspection	LTPD = 2% S/S = 116, A_{CC} = 0	
	Ship to Customer					

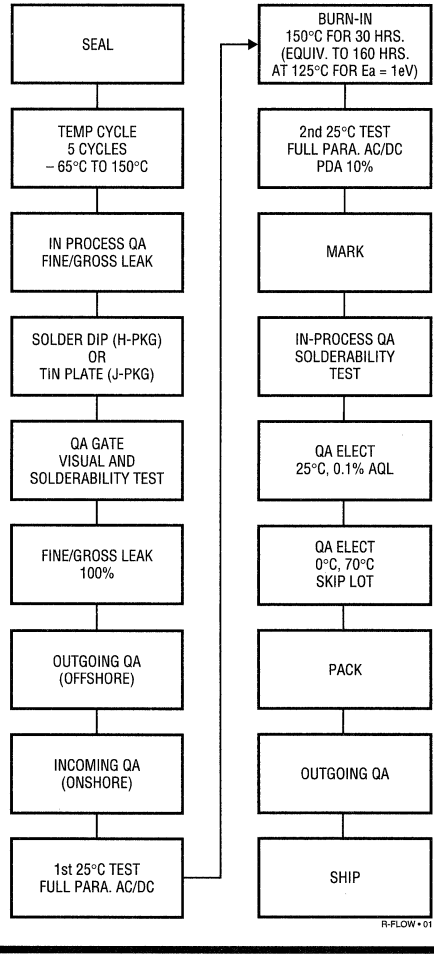
Linear Technology Corporation R-Flow

Reliability has been a key focal point at Linear Technology Corporation (LTC) since its inception in 1981. Our standard product reliability is monitored closely and we have generated an extensive reliability database for both hermetic and plastic devices. This data is published on a quarterly basis and we are seeing very low reliability failure rates in the under 1 FIT range at 55°C.*

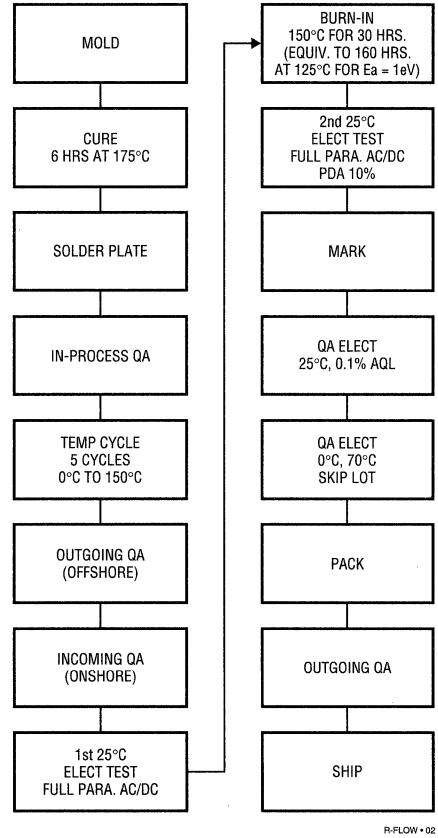
In response to customer requests, we have added an even higher level of reliability screening for commercial hermetic and plastic components. LTC's R-Flow adds a burn-in equivalent to 160 hours at 125°C to the standard commercial process flow. Following burn-in, a 100% room temperature test is performed and a 10% PDA (Percent Defective Allowed) is applied. This PDA limit affords an additional level of insurance on a lot-by-lot basis and prevents the occasional disparate lot from being shipped for critical applications. The additional room temperature insertion also decreases the probability of any electrical defectives in the R-Flow lot.

*1 FIT = 1 failure in 10^9 device hours.

R-Flow for TO-5 and CERDIP Packages



R-Flow for Plastic Dual-In-Line Packages



Introduction

As integrated circuit technologies achieve higher speed, smaller geometries, lower power and lower voltage, there is a trend toward greater ESD (Electrostatic Discharge Damage) susceptibility. State-of-the-art CMOS ICs can be susceptible to as little as 50V, a static level that is way below the 500V to 15,000V commonly found in an ESD unprotected work environment. As these state-of-the-art ICs get designed into systems, the ESD susceptibility of system hardware also increases proportionately. Industry estimates of losses due to ESD are in the range of a few billion dollars annually.

It has now become increasingly more important for all semiconductor manufacturers and users of semiconductors and other electronic components to fully understand the nature of ESD, the sources of ESD, and its impact on quality and reliability, to effectively deal with this *silent chip killer.*

Linear Technology Corporation (LTC) has successfully undertaken a simple but effective ESD Protection Program as part of an overall program designed to enhance product quality and reliability. Described in this section are the key points of this program.

This objective is to provide increased ESD awareness by showing the sources of ESD in the work environment, and to recommend key points for the successful implementation of an ESD program on a company-wide basis.

The end result of a successful ESD program would be the reduction of line failures, final inspection failures and field failures, improved manufacturing yields, improved product quality and reliability and lower warranty costs. We hope that this will help to convince the reader that an ESD Protection Program must be an integral part of every electronic company's product quality and reliability program.

Key Elements of a Successful ESD Protection Program

Recent improvements in failure analysis techniques to correctly identify ESD failures together with an increase in ESD related information from technical publications, EOS/ESD symposiums and vendors have significantly helped to increase ESD awareness.

The ESD Protection Program at LTC was successfully launched in 1983 when production of ICs was first started. A constant upgrading of the program is still underway. During the ongoing efforts to improve product quality and reliability, previously unrecognized ESD related problems have been brought to light and corrected.

An effective ESD Protection Program must start at product design, and encompass all manufacturing and handling steps up to and including field service and repair. Our design goal is to achieve an ESD susceptibility level of 2,000V or greater.

Since the sources of static in any work environment are similar, key elements of the program successfully implemented at LTC can also be applied to all users of electronic components. Where these key elements apply, static controls generic to an electronic systems manufacturer are included.

The key elements of a successful ESD Protection Program include:

1. Understanding static electricity.
2. Understanding ESD related failure mechanisms.
3. ESD sensitivity testing.
4. Establishing an ESD task force to outline the requirements of the program, sell the program to management, implement the program, review progress against milestones, and follow up to ensure the program is continuously improved and upgraded. Selecting an ESD coordinator to interface with all departments affected.
5. Conducting a facility evaluation to help identify the sources of ESD and establish static control measures.
6. Setting up an audit program.
7. Selecting ESD protective materials and equipment.
8. Establishing a training and ESD awareness program.

What is Static Electricity?

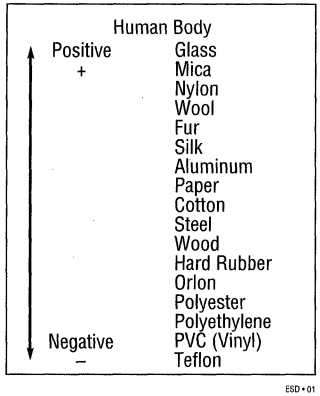
Lightning and sparks from a metallic doorknob during a dry month are examples of static electricity. The magnitude of static charge is dependent on many variables, among them the size, shape, material composition, surface characteristics and humidity. There are basically three primary static generators: triboelectric, inductive and capacitive charging.

Triboelectric Charging

The most common static generator is triboelectric charging. It is caused when two materials (one or both of which are insulators) come in contact and are suddenly separated or rubbed together, creating an imbalance of electrons on the materials and thus static charge.

Some materials readily give up electrons whereas others tend to accumulate excess electrons. The Triboelectric Series lists materials in descending order from positive to negative charging due to this triboelectric effect. A sample triboelectric series is shown here. A material that is higher on the list, e.g., a human body, will become positively charged when rubbed with a material, e.g., polyester, that is lower on the list, due to the transfer of electrons from the human body to the polyester material.

Triboelectric Series



ESD • 01

Inductive Charging

Static can also be caused by induction, where a charged surface induces polarization on a nearby material. If there is a path to ground for the induced charge, an ESD event may take place immediately. An example of an induced charge is when the plastic portion of a molded IC package acquires a charge either through triboelectric charging or other means, produces an electrostatic field and induces a charge on the conductive leads of the device. When the device leads are grounded, a short duration damaging static pulse can take place.

Capacitive Charging

The capacitance of a charged body relative in position to another body also has an effect on the static field. To see that this is true, one need only look at the equation $Q = CV$ (charge equals capacitance times voltage). If the charge is constant, voltage increases as capacitance decreases to maintain equilibrium. As capacitance decreases the voltage will increase until discharge occurs via an arc. A low voltage on a body with a high capacitance to ground can become a damaging voltage when the body moves away from the ground plane. For example, a 100V charge on a common plastic bag lying on a bench may increase to a few thousand volts when picked up by an operator, due to a decrease in capacitance.

These sources of static can be found almost anywhere in an unprotected work environment, on personnel wearing synthetic clothing and smocks, on equipment with painted or anodized surfaces, and on materials such as carpets, waxed vinyl floors, and ungrounded work surfaces.

Understanding the Failure Mechanisms

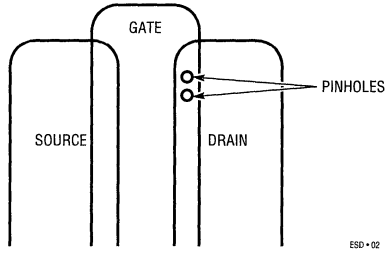
In the past, analysis of electrical failures to pinpoint ESD as a cause was often difficult. But with a better understanding of failure mechanisms and their causes, and the use of more sophisticated techniques like scanning electron microscopy (SEM), pinpointing ESD failures can now be part of a routine failure analysis.

arametric or functional failure of bipolar and MOS ICs an occur as a result of ESD.

he primary ESD failure mechanisms include:

. **Dielectric Breakdown:** This is a predominant failure mechanism on MOS devices when the voltage across the oxide exceeds the dielectric breakdown strength. This failure mechanism is basically voltage dependent where the voltage must be high enough to cause dielectric breakdown. As such, the thinner the oxide, the higher the susceptibility to ESD. MOS device failures are characterized by resistive shorts from the input to V_{DD} or V_{SS}.

MOS Transistor Structure
Showing ESD Included Pinholes at Gate Oxide



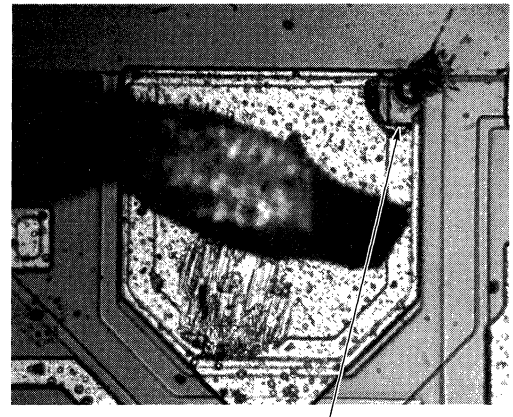
This failure mechanism can also be found on bipolar ICs which have metallization runs over active semiconductor regions separated by a thin oxide. Device failures are characterized by resistive or high leakage paths.

. **Thermal Runaway (Second Breakdown):** This failure mechanism results in junction melting when the melting temperature of silicon (1415°C) is reached. This is basically a power dependent failure mechanism; the ESD pulse shape, duration and energy can produce power levels resulting in localized heating and eventually junction melting, even though the voltage level is below that required to cause dielectric breakdown. Breakdown of the emitter-base junction of a NPN transistor is a common ESD related failure mode on bipolar ICs, since the highest current density occurs on the smallest current carrying area which is typically the emitter-base junction. Low current gain (h_{FE}) is very sensitive indicator of emitter-base junction damage on bipolar linear ICs.

3. **Parametric Degradation:** On precision, high speed ICs (e.g., bipolar operational amplifiers with a typical input bias current of 10pA and low input offset voltage of typically 50μV) ESD can cause device degradation, besides functional failures. This can impact electrical performance and adversely affect device reliability.

   This degradation in device parametric performance is far more difficult to pinpoint as an ESD related failure mode. It is also the least understood among the failure modes. The extent of this degradation is dependent on the number of ESD pulses and the level of damage sustained. The first ESD pulse may not cause an IC to fail the electrical data sheet limits but with each subsequent ESD pulse, the parametric performance can degrade to the point where the device no longer meets the data sheet limits.

   There is a great deal of current research focused on ESD induced latent failures, and there now appears to be more evidence of this type of failure mechanism.



RESISTIVE SHORT ON A METALLIZATION STRIP OVER A THIN OXIDE N + REGION ON A BIPOLAR IC

ESD Failure Analysis Program

ESD defect identification must be an integral part of a failure analysis program. The key objectives are to help identify the ESD failure mechanism, isolate the cause for failure, and implement corrective action to prevent recurrence. All devices suspected of being damaged by ESD after initial electrical verification, should be failure analyzed.

An ESD failure analysis program is outlined below.

1. Initial electrical test verification.
2. Review device history to determine if there are any similar failures in the past. Review ESD sensitivity data if available.
3. Investigate conditions in any area that can potentially cause ESD damage.Common potential problem areas include:
   - Proper grounding procedures not being followed (e.g., conductive table/floor mats not grounded, personnel not wearing wrist strap, etc.)
   - Improper handling (e.g., handling devices at non-ESD protected station)
   - Transporting devices in unapproved containers (e.g., in common plastic bags/tubes/tote boxes)
   - Changes in procedures or operation
   - Changes in equipment
   - Design deficiencies
4. Failure analysis sequence:
   - Bench testing and curve tracer analysis
   - Pin-to-pin analysis
   - Internal visual (10× to 1000×)
   - Liquid crystal hot spot detection
   - Scanning electron microscopy (SEM), secondary ion mass spectrometry (SIMS), energy dispersive X-ray analysis (EDX), scanning auger microprobe (SAM), radiography, voltage contrast, electron beam induced current (EBIC)
   - Plasma/chemical etching
   - Special fault decoration
   - Micro-sectioning
   - Documentation

   An excellent failure analysis manual is published by the Rome Air Development Center titled *Failure Analysis Techniques—A Procedural Guide.*
5. Duplication of failure by stressing identical devices. The same or similar electrical failure mode is a good indicator of an ESD induced failure mode.
6. Implement corrective action to prevent recurrence. Corrective action may include:
   - Component, board, sub-system or system level re-design
   - Improve ESD controls
   - Improve part handling
   - Improve ESD awareness
   - Improve compliance with ESD protection procedures
   - Increase audit frequencies
   - Improve packaging materials and procedures

Corrective action taken by the end user should include a thorough review of electrical and mechanical packaging designs. In addition the end users should consult with the IC manufacturer on their findings, request failure analysis of suspected ESD failures if needed and require the IC manufacturer to take appropriate corrective action on any confirmed ESD failure.

ESD Sensitivity (ESDS) Testing

ESDS testing is crucial in helping the IC designer and the end user evaluate the ESD susceptibility of a particular device. At LTC, ESDS testing is incorporated into the failure analysis program and is performed on each device as part of the product characterization program. The ESDS testing is also part of new product qualification. LTC performs this ESDS testing according to MIL-STD-883 Method 3015.

The ESDS testing provides immediate feedback to the IC designer on any weakness found in the design and permits design correction before product release. The ESDS data collected is also used as baseline data to evaluate the effect of any future design changes on the ESDS testing performance, and to help ensure that the final packaging methods meet MIL-M-38510 requirements. Devices are categorized as either Class One, Class two or Class Three, each with a susceptibility range from 0V to 2000V, above 2000V but below 4000V, and above 4000V respectively. Topside marking with equilateral triangles is specified by MIL-M-38510.

Since people are considered to be a prime source of ESD, the ESDS test circuit is based on a human ESD model. A 1500Ω resistor and a 100pF capacitor are used in the test circuit. Human capacitance is typically 50pF to 250pF, with the majority of people at 100pF or less, and human

resistance ranges from 1000Ω to 5000Ω. An ESD failure is defined as a voltage level which causes sufficient damage to the device such that it no longer meets the electrical data sheet limits.

After initial ESDS testing, it is important that ESDS test monitoring be performed periodically on devices from various lots to determine lot-to-lot variation. The VZAP-2 report titled "Electrostatic Discharge (ESD) Susceptibility of Electronic Devices" published by the Reliability Analysis Center, Rome Air Development Center, contains a wealth of information on ESDS testing data on devices of different process technologies from many manufactures. The data in this report clearly indicates a large lot-to-lot variation relating to ESD susceptibility on the same device.

Design for ESD Protection

ESD protection designs employed on LTC devices include:

1. Input clamp diodes
2. Input series resistors to limit ESD current in conjunction with clamp diodes
3. New ESD structures
4. Eliminating metallization runs over thin oxide regions when they are tied directly to external pins

ESD Task Force

An ESD task force should consist of members from each effected department to do the foundation work, sell the program to management, and implement the program with the following objective:

1. Develop, approve and implement an ESD control specification covering all aspects of design, ESD protected materials and equipment, and manufacturing
2. Raise the level of ESD awareness
3. Develop a training and certification program
4. Work with all departments on any ESD questions or problems
5. Develop a program to educate and assist sales personnel, distributors and customers to minimize ESD
6. Review and qualify new ESD protective materials and equipment, and keep specification and training program upgraded
7. Measure the cost-to-benefit ratio of the program

Facilities Evaluation

The ESD task force should be responsible for facility evaluation. This evaluation should be guided by the ESD coordinator. The ESD coordinator should be chosen for strong knowledge of ESD controls and for the ability to effectively interface with all effected departments. The primary objective of the task force is to pinpoint areas that represent the source of static electricity and potential yield losses due to ESD.

A representative, preferably the engineering or production manager, from each of the key manufacturing areas should be represented on this task force. At LTC this effort is headed by the Quality Assurance Manager and the Package Engineering Manager. The balance of the ESD task force members are the Test Engineering, Product Engineering and Production Managers.

The only equipment needed for this survey is a field static meter which measures static up to a level of 50kV. Both nuclear and electronic type static meters are available from manufactures like 3M, Simco, Wescorp, Scientific Enterprises, Voyager Technologies and ACL.

Regardless of area classification, all manufacturing areas can be broken down into the following categories for evaluation purposes.

1. **Personnel:** Personnel represents one of the largest source of static, form the type of clothing, smocks and shoes that they wear (for example, polyester or nylon smocks).
2. **The Environment:** The environment includes the room humidity and floors. Relative humidity plays a major part in determining the level of static generated. For example, at 10% to 20% RH a person walking across a carpeted floor can develop 35kV versus 1.5kV when the relative humidity is increased to 70% to 80%. Therefore the humidity level must be controlled and should not be allowed to fluctuate over a broad range.

   Floors also represent one of the greatest contributors of static generation on personnel, moving carts or equipment because of movement across its surface. Carpeted and waxed vinyl floors are prime static generators.

3. **Work Surfaces**: Painted or vinyl-covered table tops, vinyl-covered chairs, conveyor belts, racks, carts and shelving are also static generators.
4. **Equipment**: Anodized surfaces, plexiglass covers, ungrounded solder guns, plastic solder suckers, heat guns and blowers are also static generators.
5. **Materials**: Look out for common plastic work holders, foam, common plastic tote boxes and packaging containers.

Examples of typical static levels are shown in the table below.

ESD SOURCE	RELATIVE HUMIDITY 10% ~ 20%	70% ~ 80%
Walking across a carpeted floor	35kV	1.5kV
Walking across a vinyl floor	12kV	0.3kV
Picking up a common plastic bag	15kV	0.5kV
Sliding plastic box over bench/conveyor	15kV	2.0kV
Ungrounded solder sucker	8kV	1.0kV
Plastic cabinets	8kV	1.0kV

This ESD survey should include all direct and support manufacturing areas where semiconductor and other electronic components are handled and should be extended to cover distribution offices. Once the facility evaluation is completed, the results are reviewed by the ESD task force, and controls are selected to combat each potential ESD problem area.

The ESD Protection Program

The degree of static control should be determined by the most static sensitive device or assembly in the operation. Top management support and implementing the same basic controls in all areas with no double standards will help to ensure success.

The basic concept of complete static protection is the prevention of static buildup, the removal of any already existing charges, and the protection of electronic components from induced fields. The first and foremost line of defense is the personnel wrist strap together with grounded conductive or static dissipative table tops, and conductive heel straps and grounded conductive or static dissipative floor mats.

To increase ESD awareness at LTC, all ESD Protection Areas are marked by an identifying label (for example, label shown below). This label alerts all personnel that ESD protection procedures are enforced in the area.

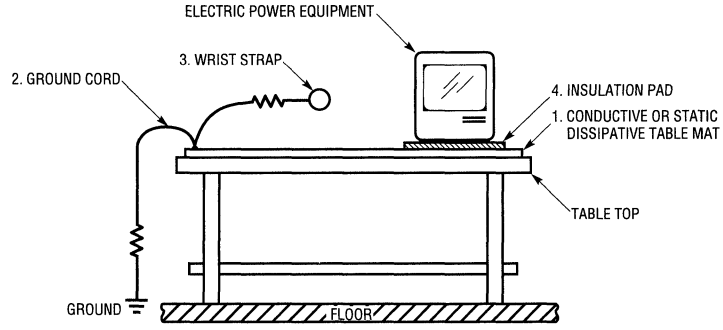
ESD Protected Workstation

Example of ESD Protected Workstations are shown in Figures 1 and 2.

Option 1 (Figure 1): All electronic components, subassemblies and assemblies must be handled at an ESD protected workstation only. The figure illustrates an ESD protected workstation consisting of a static dissipative table mat grounded to earth or electrical ground through a 1MΩ series resistor, with the requirement that the operator wears a grounded insulated conductive wrist strap with a 1MΩ series resistor. This 1MΩ series resistor protects the operator from electrical shock, should the operator come in contact with a potentially lethal voltage. Option 1 should be used where the operator does not require a large degree of freedom, e.g., during product inspection, etc.

Option 2 (Figure 2): Shows an alternate installation method for an ESD protected workstation. It consists of a conductive or static dissipative floor mat grounded to earth or electrical ground through a 1MΩ series resistor with the operator wearing a conductive shoe strap. This installation is typically used where the operator needs freedom of movement over a large area, e.g., environmental chamber loading and unloading, electrical testing, etc. To be effective the conductive shoe strap must make contact with the wearer's foot or thin sock and be attached to the wearer's shoe to maximize contact between the strap and the conductive or static dissipative floor.

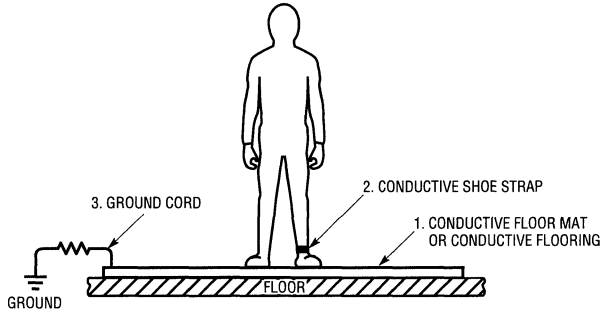
)ption 3: Utilizes the same conductive or static dissipative oor mat installation as Option 2 with the exception that ıe operator is grounded via a wrist strap through the quipment ground instead of a conductive shoe strap. It is utilized where an operator is working with a piece of freestanding equipment and does not require a great deal of freedom of movement.



MATERIALS:
1. 1/16" THICK CONDUCTIVE OR STATIC DISSIPATIVE TABLE MAT WITH SURFACE RESISTIVITY OF $\leq 10^8\Omega$ PER SQUARE.
2. INSULATED CONDUCTIVE GROUND CORD WITH A SERIES RESISTOR OF 1/2W MINIMUM, 1MΩ ± 10%, AND 18AWG OR LARGER INSULATED WIRE.
3. INSULATED CONDUCTIVE WRIST STRAP WITH 1/4W MINIMUM, 1MΩ ± 10% AND 20AWG OR LARGER INSULATED WIRE. THE CURRENT LIMITING 1MΩ RESISTOR MUST BE LOCATED RIGHT NEXT TO THE WRIST TO PREVENT THE POSSIBILITY OF SHUNTING THE RESISTOR.
4. POWER TEST EQUIPMENT MUST BE CHASSIS GROUNDED VIA A 3-PRONG PLUG, AND PLACED ON AN INSULATION PAD MADE OF FORMICA, FIBERGLASS OR EQUIVALENT MATERIAL.

ESD F01

Figure 1



MATERIALS:
1. OPTIONAL 1/8" THICK CONDUCTIVE OR STATIC DISSIPATIVE MAT OR CONDUCTIVE FLOORING (e.g., CONDUCTIVE FLOOR TILES) WITH A SURFACE RESISTIVITY OF $\leq 10^8\Omega$ PER SQUARE.
2. CONDUCTIVE SHOE STRAP WITH A SURFACE RESISTIVITY OF $\leq 10^8\Omega$ PER SQUARE.
3. INSULATED CONDUCTIVE GROUND CORD WITH A SERIES RESISTOR OF 1/2W MINIMUM, 1MΩ ±10%, AND 18AWG OR LARGER INSULATED WIRE.

ESD F02

Figure 2

Handling

At LTC all products are handled, transported and staged in volume conductive tote boxes. This offers maximum protection to the components from triboelectrically generated and inductive static charges. The rule is—under no circumstances should components be removed from their approved containers except at an ESD protected workstation.

Final Packaging

Only antistatic, static dissipative and conductive final packaging containers (for example, antistatic or conductive dip tubes, volume conductive carbon loaded plastic bags or metallic film laminate bags, foil lined boxes) are used. Filler (dunnage) material used should be antistatic, noncorrosive, and should not crumble, flake, powder, shred or be of fibrous construction. Conductive packing materials are preferred since they not only prevent buildup of triboelectric charge, but also provide shielding from external fields.

Other ESD Preventative Measures

- Where possible, ban all static bearing materials, e.g., common plastics, styrofoam from the work environment.
- Use only synthetic material smocks with 1% to 2% interwoven steel.
- Ensure all electronic and electromechanical equipment is chassis grounded, including conveyor belts, vapor degreasers and baskets, solder pots, etc.
- Tips of hand soldering irons are to be grounded.
- All parts of hand tools (e.g., pliers, etc.) which can be expected to come in contact with electronic components are to be made of conductive material and grounded.
- Conductive shorting bars are to be installed on all terminations for PC boards with electronic components during assembly, loading, inspecting, repairing, soldering, storing and transporting.
- All PC boards with electronic components are not to be handled by their circuitry, connector points or connector pins.
- High velocity air movement is to be delivered through a static neutralizer.
- Air ionizers are to be employed in neutralizing static buildup on insulators if they have to be used or as an extra precautionary measure for extremely sensitive devices.
- Do not slide electronic components over a surface.

Air ionizers come in three basic types: nuclear, AC and pulsed DC. These ionizers can neutralize static charges on nonconductive materials by supplying the materials with a stream of both positive and negative ions.

The advantage of the AC or pulsed DC type air ionizer is that there is no recurring annual replacement cost. The disadvantages are: it emits ozone which can damage rubber in equipment; EMI (Elector Magnetic Interference); and an imbalance in the stream of ions if not properly maintained, therefore necessitating frequent preventive maintenance.

The advantages of the nuclear type air ionizer are low maintenance, no ozone, no EMI and no imbalance problems. The disadvantages are that it requires careful handling because of the radioactive source and the annual recurring cost to replace the radioactive source.

The selection of air ionizers must be done with care and with awareness of the above limitations. The squirrel cage ionized air blower has been proven to produce a significantly more even distribution of ion patterns than does a conventional fan blower design.

Maintenance

ESD protective floor and table coverings must be properly maintained. Do not wax them. Cleaners must not degrade their electrical properties. Vacuum to remove loose particles, followed by a wet mop with a solution of mild detergent and hot water.

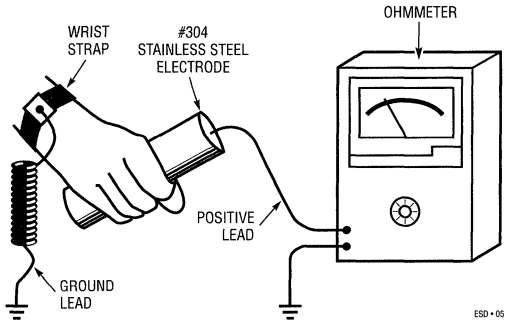
Periodic Audits

At LTC periodic audits are conducted to check on the following at least quarterly unless otherwise noted.

- Compliance with ESD control procedures.
- Ensure that the conductive ground cord connection is intact by measuring the series resistance to ground with an ohmmeter.

Ensure that wrist straps are still functional by measuring the resistance from the person to ground. The ground lead of the ohmmeter is connected to the ground connection of the wrist strap, and the positve lead is connected to a stainless steel electrode (one inch in diameter and three inches long #304 stainless steel) which is held by the person. This test method not only checks the resistance of the series resistor, but also resistance through the ground cord and any contact resistance between the wrist strap and the person's skin. This test procedure is required when wrist straps with an elastic nylon band with interwoven metallic strands are used, since the metallic strands break down with prolonged use. This monitor frequency may be shortened depending on audit results.

Wrist Strap Resistance Test Setup



- Measure the surface resistivity of conductive or static dissipative table tops once every quarter using ASTM-F-150-72, ASTM-D-257 or ASTM-D-991 test methods as appropriate.

Materials Selection and Specification

Based on the tremendous amount of ESD protective materials available, it is important that materials are selected based on a stringent qualification. Once the materials have been selected and specifications defined, a material procurement specification needs to be initiated that defines the materials and quality requirements to the vendor. One of the major pitfalls is to procure material in haste, e.g., a wrist strap, only to find out it does not perform reliably.

The SOAR-1 report titled "ESD Protective Material and Equipment: A Critical Review" published by the Rome Air Development Center is an excellent reference on the various types of ESD protective materials available.

At LTC a minimum of three manufacturing lots from a potential vendor are subjected to qualification testing per the requirements of the material procurement specification for ESD protective materials. The vendor is considered qualified only when all three lots are found to be acceptable. Once vendors have been qualified, all incoming ESD protective materials are subjected to a stringent incoming inspection.

The following table summarizes a sample material and test specification for ESD protective materials.

MATERIAL	PROPERTIES/DESCRIPTION	TEST METHODS
Wrist Strap	• Insulated coil cord with a 1MΩ ±10%, 1/4W minimum series resistor molded into snap fastener (at wrist end), and an elastic wrist band with inner metallic filaments and insulative exterior	Measure series resistance with ohmmeter. Apply normal tug to both ends of strap and remeasure series resistance. Resistance must be between 0.8MΩ to 1.2MΩ.
Conductive or Static Dissipative Table and Floor Coverings, Conductive Tote Boxes, Conductive Shoe Straps	• Must not shed particles • Must not support bacterial or fungal growth • Conductive: surface resistivity < 10^5Ω/square, Static Dissipative: surface resistivity > 10^5 < 109Ω/square	Test per ASTM-F-150-72, ASTM-D-257, ASTM-D-991 (for surface resistivity < 10^6Ω/square).
Conductive Foam	• Shall not contain more than 30ppm Cl, K, Na when a quantitative chemical analysis is performed • Must not support bacterial or fungal growth	With devices inserted into the foam, the foam must not cause lead corrosion after a 24-hour 85°C/85% RH temperature/humidity storage.
Antistatic and Conductive Dip Tubes	• Must not exhibit an oily film	Must meet an Electrostatic Decay test per Federal Test Method Standard 101 Test Method 4046. Material charged to 5000V must be discharged to 1% of its initial value (50V) in 2 seconds after a 24-hour conditioning at 15% relative humidity.
Antistatic and Conductive Bags	• Antistatic bags must meet MIL-B-81705 type . • Conductive bags must meet MIL-B-117 and sealing requirements of MIL-B-81705 • Must not support bacterial or fungal growth	Test method for antistatic bags same as for antistatic/ conductive dip tubes. Test method for conductive bags same as for conductive table/floor coverings.
Static Eliminators/Ionized Air Blowers	• Ozone level: 0.1ppm maximum for 8-hour exposure • Noise: 60dB maximum • EMI: nondetectable when measured 6 inches away	Voltage Decay test: A nonconductive sheet of material charged to 5kV must be discharged to 1% of its initial value (50V) in 2 seconds at a distance of 2 feet from the ionizer or larger distance if application calls for a larger distance.

Training and Certification Program

The training program should be developed to increase ESD awareness and to assist all personnel in complying with the ESD control specification. The program should include:

1. A discussion on "What is Static Electricity?"
2. How ESD affects ICs
3. Estimated cost of ESD related losses
4. Materials and equipment for controlling static
5. The importance of wearing the wrist strap
6. The importance of an audit program
7. Encourage floor personnel to alert the ESD task force to any ESD potential areas

ESD training should be incorporated into the personnel training and certification program. At LTC only fully trained and certified personnel are allowed to do actual production work. To help increase ESD awareness, it is often a good idea to show ESD awareness films and video tapes which are available from a variety of sources (Reference 3 provides a list of films and video tapes). Personnel are retrained and recertified at a minimum frequency of once per year.

Measuring the Benefits

Where possible, the benefits of an ESD Protection Program should be tracked and quantified. The two yardsticks used at LTC are final test yields and QA electrical average outgoing quality (AOQ). Since the implementation of this program, there has been a significant improvement in final test yields especially on static sensitive CMOS devices. With the elimination of ESD as a potential failure cause, the electrical AOQ has averaged well under 100ppm for all products combined. Improvements such as this help to provide positive feedback to manufacturing and support personnel on the importance of an ESD Protection Program, and also help to ensure its continuing success.

References

1. DOD-STD-1686 *Electrostatic Discharge Control Program for Electrical and Electronic Parts, Assemblies and Equipment*
2. DOD-HDBK-263 *Electrostatic Discharge Control Handbook for Electrical and Electronic Parts, Assemblies and Equipment*
3. SOAR-1 *State-of-the-Art Report ESD Protective Materials and Equipment: A Critical Review*, published by the Rome Air Development Center
4. VZAP-2 *Electrostatic Discharge (ESD) Susceptibility Data*, published by the Rome Air Development Center
5. EOS-1, EOS-2, etc. *Electrical Overstress/Electrostatic Discharge Symposium Proceedings, 1979 to Current Year*
6. MIL-STD-883 *Test Methods and Procedures For Microelectronics*
7. MIL-I-38534 *General Specification for Integrated Circuits (Microcircuits) Manufacturing*
8. MIL-M-55565 *Microcircuits, Packaging of*
9. MIL-M-81705 *Barrier Materials, Flexible, Electrostatic* — Free, Heat Sealable
10. FED-STD-101 *Preservation, Packaging and Packing Materials Test Procedures; Test Methods, 4046: Electrostatic Properties of*
11. EIA-625 *Requirements for Handling Electrostatic Discharge-Sensitive (EDSS) Devices*

Linear Technology Corporation (LTC) has an active Statistical Process Control (SPC) system. It operates via the interrelated mechanisms of: a structure, control charts with built-in contingency action plans, operational area documentation (flowcharts and control plan details), an SPC training program, each of which is defined in the Company's officially controlled SPC specification.

Structure

At the core of the SPC system are the Process (or Preventive) Action Teams (PATs). These cross-functional teams are comprised of individuals directly involved with a process element or problem. In a production operation, they typically involve production operators, lead operators, maintenance, engineering and/or supervision. In a nonproduction operation, the PATs are comprised of operating employees and representatives of related functions.

Each operating group (e.g., Wafer Fab) has a formal SPC presence in the form of an SPC Quality Control Team (QCT). These SPC QCTs are comprised mostly of the manager and staff of that particular operating unit bearing the responsibility to implement and maintain SPC within their respective areas.

This QCT structure is the leadership of that operating unit, and as such, sanctions the various PATs within its jurisdiction as they implement and maintain SPC and/or solve specific problems in their respective areas. In addition, the QCT conducts monthly reviews of SPC charts, action items and new programs.

The QCTs, in turn, report to the SPC Steering Committee. This body consists of the President, Chief Operating Officer, Vice President of Operations, Vice President of Quality & Reliability and the SPC Manager. Thus, it has the corporate leadership responsibility for SPC at Linear Technology.

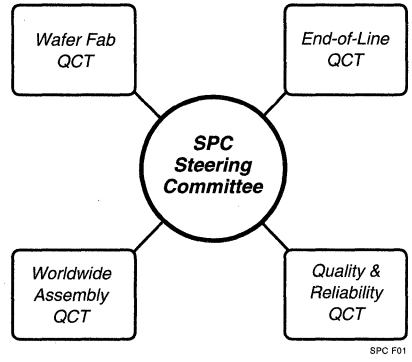


Figure 1. Linear Technology Corporation SPC Quality Control Teams

Control Charts

The control charts at LTC are manually charted by the operators to ensure that they are the custodians of the process, its trends, and defined corrective measures (as opposed to computerized SPC charting).

The contingency action plan, known as the Out-of-Control Action Plan (OCAP), defines the specific corrective actions when the process experiences out-of-control situations. No control chart is put in place without an OCAP. This strategy has in effect empowered the work force, while freeing the engineering staff for systematic and continuous improvement.

Flowcharts and Control Plan Details

The flowcharts serve to graphically display the flow of products in each operational area, as well as define and communicate the critical nodes of that operation. The details of each critical node are defined in the Control Plan Detail, which serves as a planning, reporting and communication tool.

n example of a flowchart and the related Control Plan etail for one operational area (e.g., The Wafer Fabrication rea) Figure 2 and Table 1 follow:

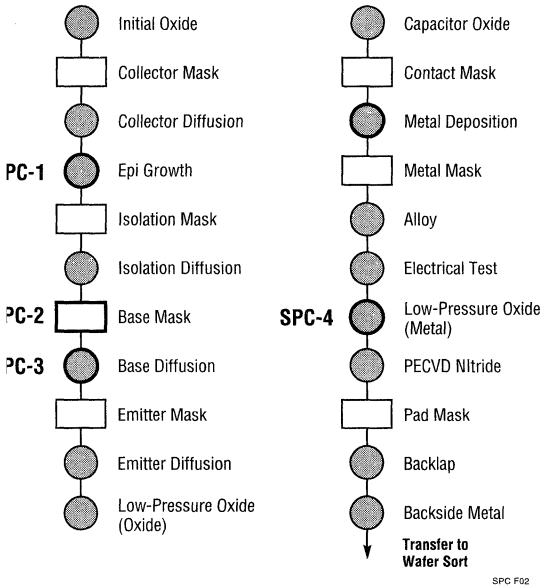


Figure 2. General Bipolar Wafer Fabrication Flowchart

Training Program

In order to pursue and continue the smooth operation of the SPC system within LTC, an all-encompassing instructional program for employees was initiated according to the following plan.

Each employee designated for SPC training is classified into one of three groups, and attends the specific classroom instruction for that classification. The courses and length of training (hours) for each group are designated in Table 2.

The content of the training courses is as follows:

BASIC SPC: Philosophy of SPC, concepts of variation, control, capability; tools and techniques for control and capability, including histograms, capability studies, control charting; 8D problem solving, including normality, brainstorming, cause and effect diagramming, Pareto analysis, capability index/ratio.

ADVANCED SPC: Review of basic concepts, fundamentals of Measurement System Evaluation (Gauge R&R), process capability studies, determination and use of control charts, i.e., $\bar{X}$ & R, Median & R, X & Moving R, p, np, u, and c chart techniques. Chart interpretation and the basics of attributes sampling system.

ıble 1. Linear Technology Corporation Process Control Plan Detail for Bipolar Wafer Fab

;PC Node ıd Process	Critical Features	Measurement Method	Sample Size	Sample Frequency	SPC Control System	MSE (Gauge R&R)	Process Capability		Status
							Cp	Cpk	
(SPC-1) Epi Growth	Resistivity	4-Point Probe	2	Batch	X & Moving R Chart with Adaptive Control	Acceptable	1.59 ~ 1.89	1.12 ~ 1.41	On Line
(SPC-2) ıase Mask	CDs	OSI-VLS1	1 Site/ 3 Wafers	Batch	$\bar{X}$ & R Chart with Adaptive Control	Acceptable	1.54	1.54	Out of Control*
(SPC-3) Base ıeposition	Sheet Resistance	4-Point Probe	3 Sites/ 3 Wafers	Batch	$\bar{X}$ & R Chart	Acceptable	1.87 ~ >2.0	1.70 ~ 1.95	On Line
(SPC-4) LPOM	Thickness	Nanospec	5 Sites/ 3 Wafers	Batch	$\bar{X}$ & R Chart	Acceptable	1.82 ~ 2.31	1.74 ~ 1.94	On Line

A Process Action Team (PAT) has been initiated to bring process under control.

Table 2.

Group #	Trainee Audience	Basic SPC	Advanced SPC	DOE	Team Org.	Total
1	Engineering (Technical)	15	20	24	4	63
2	Management/Supervision Technicians	15	20	—	4	39
3	Operators	15	—	—	—	15

DESIGN OF EXPERIMENTS (DOE): Philosophy and need of experimental design, experimental methodologies utilizing Fisher & Taguchi concepts. Response Surface Methodology for parameters and tolerance designs, including ANOVA and analysis of co-variance.

TEAM ORGANIZATION: An outline of the SPC organization within LTC, the concepts of the SPC Quality Control Teams (SPC QCTs) and Preventive/Process Action Teams (PATs). Strategies for Detailed Control Plans and Out-of-Control Action Plans (OCAPs). Concepts of team effectiveness.

Manufacturing Excellence

One of the LTC goals is *manufacturing excellence.* The traditional SPC techniques seek to produce processes that are capable and in control. To improve those processes and to determine rational parameters and specification tolerance of new products and processes requires the *Design of Experiments* (DOEs) methodology.

LTC actively pursues the screening techniques described by Fisher as well as the optimization techniques of Box and Taguchi. These latter techniques, known as *Response Surface Methodology* and *Taguchi Methods*, are particularly useful in developing robust products and processes, with a minimum of sensitivity to process variation.

Contribution to Quality

Contribution to quality improvement has evolved from one dominated by ATTRIBUTE INSPECTION (pass/fail) to one involving a mixture of SPC and attribute inspection. As we progress further, the contribution of Design of Experiments will become significant. Products and processe developed using the DOE tools will have the *quality bui in.* The consequence of this built-in quality is predictabl performance at the lowest possible cost.

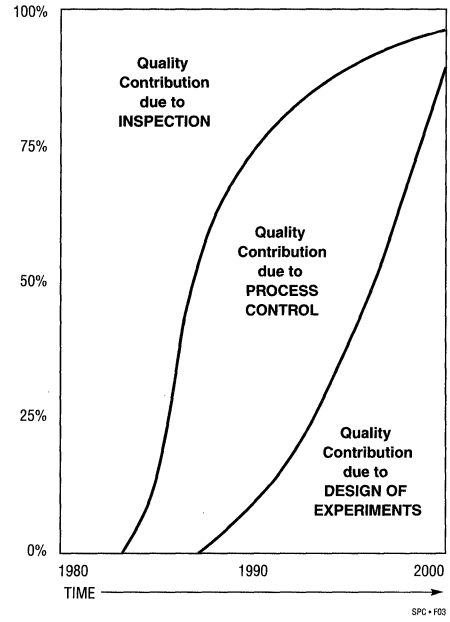


Figure 3. The Semiconductor Quality Evolution

The concepts of SPC and DOE have already been institu tionalized within LTC and will provide the methodology t ensure a process of continuing improvement.

INTRODUCTION

Linear Technology Corporation (LTC) offers a wide variety of precision linear ICs in die form. It is our intent to offer dice electrically tested to levels which can be expected to yield the best possible performance in hybrid circuits. Complicating this task is the fact that many specifications given for our standard packaged products cannot be tested at the wafer level. Further, parameters which are 100% tested at wafer probe testing may shift during the die attach/assembly process.

Data sheets are available that contain ordering information for obtaining dice products. They are available from your local LTC Sales Rep, or from LTC Marketing.

GENERAL INFORMATION

Electrical Testing

Dice are 100% tested in wafer form at 25°C to the DC limits shown on the dice data sheet for a given device type. Many LTC packaged products have multiple electrical grades associated with a basic die type. A cross reference appears on each dice data sheet indicating which die product grade should be ordered to optimize candidates to meet the specifications of the desired finished product grade. This information should be used as a guideline only since LTC does not guarantee electrical specifications after assembly. Since electrical testing is done only at 25°C, no absolute guarantee can be made regarding performance at other temperatures. Some LTC products require post-package trimming to overcome certain assembly-related parameter shifts. Details on this trimming may be obtained by contacting the factory.

Visual Inspection

Dice are 100% visually inspected in accordance with MIL-STD-883, Method 2010 Condition B.

Chip Dimensions

Chip dimensions are as indicated on individual dice data sheets. Tolerance is ±1 mil. Chip thickness ranges from 12 mils to 20 mils, depending on product type. Bond pad dimensions are 4.5 mils × 4.5 mils minimum.

Topside Passivation

LTC products are passivated with a 2- layer system: a proprietary deposited oxide gives a crack-free conformal coverage of metal and oxide steps. A plasma nitride overcoat protects the die from ionic contamination and scratches during handling, testing and assembly. Note that LTC uses fuse link, laser and zener zap trimming techniques which may require windows in the passivation over the trim points. This passivation system is a major contributor to the extremely high reliability demonstrated throughout millions of device hours of accelerated testing of LTC devices in plastic and hermetic packages.

Topside Metallization

The metallization is a minimum of 11,000 Å thick unless otherwise specified. The quality of the metallization step coverage is monitored via a weekly SEM inspection per MIL-STD-883, Method 2018.

Backside Metal

Dice products are normally provided without backside metallization. Contact LTC for details about availability of LTC products with a particular backside metallization.

Backside Potential

LTC products are junction isolated. For proper operation the backside must be electrically connected to either the most negative potential seen by the IC or the most positive potential. This information is given in the individual dice data sheets.

Packaging

Dice are packaged in compartmentalized waffle packs for ease of handling and storage. Each waffle pack contains 100 dice. Special packaging methods are also available by contacting the factory.

Quality Levels of Dice Shipped

Each dice lot is guaranteed to meet the following requirements:

- Internal visual per MIL-STD-883, Method 2010, Condition B: 1.0% AQL Level II.
- Electrical: Due to variations in assembly methods and packaging techniques LTC does not guarantee electrical specifications after assembly. When a determination as to the finished products assembly yield is needed, the lot acceptance testing available at extra cost should be pursued.

Reliability Assurance

In addition to the more conventional reliability audits performed on finished products, LTC has innovated a unique periodic wafer fab reliability audit using a specially designed reliability structure that is stepped into all wafers. The test structure is optimized to accelerate the two primary failure mechanisms in linear circuits: mobile positive ions and surface charge-induced inversions. This provides a continuous monitor on the reliability performance of LTC's wafer fab processes and provides immediate feedback to wafer fab typically within one week.

Electrostatic Discharge (ESD) Precautions

Precision linear devices, especially those with very low (pA) input bias current levels and low (< 50μV) input offset voltages are susceptible to shifts in electrical performance and ESD damage as a result of improper handling. LTC recommends that ESD precautions, such as grounded conductive work stations, grounded conductive wrist straps and grounded equipment, be taken to prevent ESD damage.

ORDERING INFORMATION

Dice may be ordered by the part number defined in the dice data sheet. Minimum direct dice order per *delivery* is 1,000 pieces or $5,000, whichever is greater. Other minimums and conditions may also apply. Smaller quantities are available from authorized dice processing companies. In some cases, tighter parameter selections than indicated on the dice data sheets can be obtained by special order. Please contact the factory for details.

Lot Acceptance Testing

Lot acceptance testing (LAT) based on sample assembly and testing is available at extra cost. Sample sizes and acceptable electrical test limits vary from device to device and must be negotiated at the time of quoting. Contact the factory for details.

Application Notes

AN1 **Understanding and Applying the LT1005 Multifunction Regulator**
This application note describes the unique operating characteristics of the LT1005 and describes a number of useful applications which take advantage of the regulator's ability to control the output with a logic control signal.

AN2 **Performance Enhancement Techniques for 3-Terminal Regulators**
This application note describes a number of enhancement circuit techniques used with existing 3-terminal regulators which extend current capability, limit power dissipation, provide high voltage output, operate from 110VAC or 220VAC without the need to switch transformer windings, and many other useful application ideas.

AN3 **Applications for a Switched-Capacitor Instrumentation Building Block**
This application note describes a wide range of useful applications for the LTC1043 dual precision instrumentation switched-capacitor building block. Some of the applications described are ultra high performance instrumentation amplifier, lock-in amplifier, wide range digitally controlled variable gain amplifier, relative humidity sensor signal conditioner, LVDT signal conditioner, charge pump F/V and V/F converters, 12-bit A/D converter and more.

AN4 **Application for a New Power Buffer**
The LT1010 150mA power buffer is described in a number of useful applications such as boosted op amp, a feed-forward, wideband DC stabilized buffer, a video line driver amplifier, a fast sample-hold with hold step compensation, an overload protected motor speed controller, and a piezoelectric fan servo.

AN5 **Thermal Techniques in Measurement and Control Circuitry**
Six applications utilizing thermally based circuits are detailed. Included are a 50MHz RMS to DC converter, and anemometer, a liquid flowmeter and others. A general discussion of thermodynamic considerations involved in circuitry is also presented.

AN6 **Applications of New Precision Op Amps**
Application considerations and circuits for the LT1001 and LT1002 single and dual precision amplifiers are illustrated in a number of circuits, including strain gauge signal conditioners, linearized platinum RTD circuits, an ultra precision dead zone circuit for motor servos and other examples.

AN7 **Some Techniques for Direct Digitization of Transducer Outputs**
Analog-to-digital conversion circuits which directly digitize low level transducer outputs, without DC preamplification, are presented. Covered are circuits which operate with thermocouples, strain gauges, humidity sensors, level transducers and other sensors.

AN8 **Power Conditioning Techniques for Batteries**
A variety of approaches for power conditioning batteries is given. Switching and linear regulators and converters are shown, with attention to efficiency and low power operation. 14 circuits are presented with performance data.

AN9 **Application Considerations and Circuits for a New Chopper-Stabilized Op Amp**
A discussion of circuit, layout and construction considerations for low level DC circuits includes error analysis of solder, wire and connector junctions. Applications include sub-microvolt instrumentation and isolation amplifiers, stabilized buffers and comparators and precision data converters.

AN10 **Methods for Measuring Op Amp Settling Time**
The AN10 begins with a survey of methods for measuring op amp settling time. This commentary develops into circuits for measuring settling time to 0.0005%. Construction details and results are presented. Appended sections cover oscilloscope overload limitations and amplifier frequency compensation.

AN11 **Designing Linear Circuits for 5V Operation**
This note covers the considerations for designing precision linear circuits which must operate from a single 5V supply. Applications include various transducer signal conditioners, instrumentation amplifiers, controllers and isolated data converters.

AN12 **Circuit Techniques for Clock Sources**
Circuits for clock sources are presented. Special attention is given to crystal-based designs including TXCOs and VXCOs.

AN13 **High Speed Comparator Techniques**
The AN13 is an extensive discussion of the causes and cures of problems in very high speed comparator circuits. A separate applications section presents circuits, including a 0.025% accurate 1Hz to 30MHz V/F converter, a 200ns 0.01% sample-hold and a 10MHz fiber-optic receiver. Five appendices covering related topics complete this note.

AN14 **Designs for High Frequency Voltage-to-Frequency Converters**
A variety of high performance V/F circuits is presented. Included are a 1Hz to 100MHz design, a quartz-stabilized type and a 0.0007% linear unit. Other circuits feature 1.5V operation, sine wave output an nonlinear transfer functions. A separate section examines the trade-offs and advantages of various approaches to V/F conversion.

AN15 **Circuitry for Single Cell Operation**
1.5V powered circuits for complex linear functions are detailed. Designs include a V/F converter, a 10-bit A/D, sample-hold amplifiers, a switching regulator and other circuits. Also included is a section of component considerations for 1.5V powered linear circuits.

AN16 **Unique IC Buffer Enhances Op Amp Designs, Tames Fast Amplifiers**
This note describes some of the unique IC design techniques incorporated into a fast, monolithic power buffer, the LT1010. Also, some application ideas are described such as capacitive load driving, boosting fast op amp output current and power supply circuits.

AN17 **Consideration for Successive Approximation A/D Converters**
A tutorial on SAR type A/D converters, this note contains detailed information on several 12-bit circuits. Comparator, clocking, and preamplifier designs are discussed. A final circuit gives a 12-bit conversion in 1.8μs. Appended sections explain the basic SAR technique and explore D/A considerations.

AN18 **Power Gain Stages for Monolithic Amplifiers**
This note presents output state circuits which provide power gain for monolithic amplifiers. The circuits feature voltage gain, current gain, or both. Eleven designs are shown, and performance is summarized. A generalized method for frequency compensation appears in a separate section.

AN19 **LT1070 Design Manual**
This design manual is an extensive discussion of all standard switching configurations for the LT1070; including buck, boost, flyback, forward, inverting and "Cuk." The manual includes comprehensive information on the LT1070, the external components used with it, and complete formulas for calculating component values.

AN20 **Applications for a DC Accurate Lowpass Switched-Capacitor Filter**
Discusses the principles of operation of the LTC1062 and helpful hints for its application. Various application circuits are explained in detail with focus on how to cascade two LTC1062s and how to obtain notches. Noise and distortion performance are fully illustrated.

AN21 **Composite Amplifiers**
Applications often require an amplifier that has extremely high performance in several areas. For example, high speed and DC precision are often needed. If a single device cannot simultaneously achieve the desired characteristics, a composite amplifier made up of two (or more) devices can be configured to do the job. AN21 shows examples of composite approaches in designs combining speed, precision, low noise and high power.

AN22 **A Monolithic IC for 100MHz RMS/DC Conversion**
AN22 details the theoretical and application aspects of the LT1088 thermal RMS/DC converter. The basic theory behind thermal RMS/DC conversion is discussed and design details of the LT1088 are presented. Circuitry for RMS/DC converters, wideband input buffers and heater protection is shown.

AN23 **Micropower Circuits for Signal Conditioning**
Low power operation of electronic apparatus has become increasingly desirable. AN23 describes a variety of low power circuits for transducer signal conditioning. Also included are designs for data converters and switching regulators. Three appended sections discuss guidelines for micropower design, strobed power operation and effects of test equipment on micropower circuits.

AN24 **Unique Applications for the LTC1062 Lowpass Filter**
Highlights the LTC1062 as a lowpass filter in a phase lock loop. Describes how the loop's bandwidth can be increased and the VCO output jitter reduced when the LTC1062 is the loop filter. Compares it with a passive RC loop filter.

Also discussed is the use of LTC1062 as simple bandpass and bandstop filter.

AN25 **Switching Regulators for Poets**
Subtitled "A Gentle Guide for the Trepidatious," this is a tutorial on switching regulator design. The text assumes no switching regulator design experience, contains no equations, and requires no inductor construction to build the circuits described.

Designs detailed include flyback, isolated telecom, off-line, and others. Appended sections cover component considerations, measurement techniques and steps involved in developing a working circuit.

AN26 A collection of interface applications between various microprocessors/controllers and the LTC1090 family of data acquisition systems. The note is divided into sections specific to each interface. The following sections are available:

Number	A/D	Microprocessor/ Microcontroller
AN26A	LTC1090	8051
AN26B	LTC1090	68HC05
AN26C	LTC1090	63705
AN26D	LTC1090	COP820
AN26E	LTC1090	TMS7742
AN26F	LTC1090	COP402N
AN26G	LTC1091	8051
AN26H	LTC1091	68HC05
AN26I	LTC1091	COP820
AN26J	LTC1091	TMS7742
AN26K	LTC1091	COP402N
AN26L	LTC1091	HD63705V0
AN26M	LTC1090	TMS320C25
AN26N	LTC1091/92	TMS320C25
AN26O	LTC1090	Z-80
AN26P	LTC1090	HD64180
AN26Q	LTC1091	HD64180
AN26R	LTC1094	TMS320C25

These interface notes demonstrate the ease with which the LTC1090 family can be interfaced to microprocessors/controllers having either parallel or serial ports. A complete hardware and software description of the interface is included.

AN27A **A Simple Method of Designing Multiple Order All Pole Bandpass Filters by Cascading 2nd Order Sections**
Presents two methods of designing high quality switched-capacitor bandpass filters. Both methods are intended to vastly simplify the mathematics involved in filter design by using tabular methods. The text assumed no filter design experience but allows high quality filters to be implemented by techniques not presented before in the literature. The designs are implemented by numerous examples using devices from LTC's Switched-Capacitor filter family: LTC1060, LTC1061, and LTC1064. Butterworth and Chebyshev bandpass filters are discussed.

AN28 **Thermocouple Measurement**
Considerations for thermocouple-based temperature measurement are discussed. A tutorial on temperature sensors summarizes performance of various types, establishing a perspective on thermocouples. Thermocouples are then focused on. Included are sections covering cold-junction compensation, amplifier selection, differential/isolation techniques, protection, and linearization. Complete schematics are given for all circuits. Processor-based linearization is also presented with the necessary software detailed.

AN29 **Some Thoughts on DC/DC Converters**
This note examines a wide range of DC/DC converter applications. Single inductor, transformer, and switched-capacitor converter designs are shown. Special topics like low noise, high efficiency, low quiescent current, high voltage, and wide-input voltage range converters are covered. Appended sections explain some fundamental properties of different types of converters.

AN30 **Switching Regulator Circuit Collection**
Switching regulators are of universal interest. Linear Technology has made a major effort to address this topic. A catalog of circuits has been compiled so that a design engineer can swiftly determine which converter type is best. This catalog serves as a visual index to be browsed through for a specific or general interest.

AN31 Linear Circuits for Digital Systems
Subtitled "Some Affable Analogs for Digital Devotees," discusses a number of analog circuits useful in predominantly digital systems. V_{PP} generators for flash memories receive extensive treatment. Other examples include a current loop transmitter, dropout detectors, power management circuits, and clocks.

AN32 High Efficiency Linear Regulators
Presents circuit techniques permitting high efficiency to be obtained with linear regulation. Particular attention is given to the problem of maintaining high efficiency with widely varying inputs, outputs and loading. Appendix sections review component characteristics and measurement methods.

AN33 Converting Light to Digits: LTC1099 Half-Flash 8-Bit A/D Converter Digitizes Photodiode Array
This application note describes a Linear Technology "Half-Flash" A/D converter, the LTC1099, being connected to a 256 element line scan photodiode array. This technology adapts itself to handheld (i.e., low power) bar code readers, as well as high resolution automated machine inspection applications.

AN34 LTC1099 Enables PC-Based Data Acquisition Board to Operate DC-20kHz
A complete design for a data acquisition card for the IBM PC is detailed in this application note. Additionally, C language code is provided to allow sampling of data at speed of more than 20kHz. The speed limitation is strictly based on the execution speed of the "C" data acquisition loop. A "Turbo" XT can acquire data at speeds greater than 20kHz. Machines with 80286 and 80386 processors can go faster than 20kHz. The computer that was used as a test bed in this application was an XT running at 4.77MHz and therefore all system timing and acquisition time measurements are based on a 4.77MHz clock speed.

AN35 Step-Down Switching Regulators
Discusses the LT1074, an easily applied step-down regulator IC. Basic concepts and circuits are described along with more sophisticated applications. Six appended sections cover LT1074 circuitry detail, inductor and discrete component selection, current measuring techniques, efficiency considerations and other topics.

AN36 A collection of interface applications between various microprocessors/controllers and the LTC1290 family of data acquisition systems. The note is divided into sections specific to each interface. The following sections are available:

Number	A/D	Microprocessor/ Microcontroller
AN36A	LTC1290	8051
AN36B	LTC1290	MC68HC05
AN36C	LTC1290/LTC1090	TMS370
AN36D	LTC1290	COP820C
AN36E	LTC1290	TMS7742
AN36F	LTC1290	COP402N
AN36O	LTC1290	Z-80
AN36P	LTC1290	HD64180

These interface notes demonstrate the ease with which the LTC1290 can be interfaced to microprocessors/controllers having either parallel or serial ports. A complete hardware and software description of the interface is included.

AN37 Fast Charge Circuits for NiCad Batteries
Safe, fast charging of NiCad batteries is attractive in many applications. This note details simple, thermally-based fast charge circuitry for NiCads. Performance data is summarized and compared to other charging methods.

AN38 FilterCAD User's Manual, Version 1.00
This note is the manual for FCAD, a computer-aided design program for designing filters with LTC's switched-capacitor filter family. FCAD helps users design good filters with a minimum amount of effort. The experienced filter designer can use the program to achieve better results by providing the ability to play "what if" with the values and configuration of various components.

AN39 Parasitic Capacitance Effects in Step-Up Transformer Design
This note explores the causes of the large resonating current spikes on the leading edge of the switch current waveform. These anomalies are exacerbated in very high voltage designs.

AN40 Take the Mystery Out of the Switched-Capacitor Filter: The System Designer's Filter Compendium
This note presents guidelines for circuits utilizing LTC's switched-capacitor filters. The discussion focuses on how to optimize filter performance by optimizing the printed wiring board, the power supply, and the output buffering of the filter. Many additional topics are discussed such as how to select the proper filter response for the application and how to characterize a filter's THD for DSP applications.

AN41 Questions and Answers on the SPICE Macromodel Library
This note provides answers to some of the more common questions concerning LTC's Macromodel Library. Topics include hardware and software requirements, model characteristics, and limitations and interpretation of results.

AN42 Voltage Reference Circuit Collection
A wide variety of voltage reference circuits are detailed in this extensive guidebook of circuits. The detailed schematics cover simple and precision approaches at a variety of power levels. Included are 2 and 3 terminal devices in series and shunt modes for positive and negative polarities. Appended sections cover resistor and capacitor selection and trimming techniques.

AN43 Bridge Circuits
Subtitled "Marrying Gain and Balance," this note covers signal conditioning circuits for various types of bridges. Included are transducer bridges, AC bridges, Wien bridge oscillators, Schottky bridges, and others. Special attention is given to amplifier selection criteria. Appended sections cover strain gauge transducers, understanding distortion measurements, and historical perspectives on bridge readout mechanisms and Wein bridge oscillators.

AN44 LT1074/LT1076 Design Manual
This note discusses the use of the LT1074 and LT1076 high efficiency switching regulators. These regulators are specifically designed for ease of use. This application note is intended to eliminate the most common errors that customers make when using switching regulators as well as offering insight into the inner workings of switching designs. There is an entirely new treatment of inductor design based upon simple mathematical formulas that yield direct results. There are extensive tutorial sections devoted to the care and feeding of the Positive Step-Down (Buck) Converter, the Tapped Inductor Buck Converter, the Positive-to-Negative Converter and the Negative Boost Converter. Additionally, many troubleshooting hints are included as well as oscilloscope techniques,

soft-start architectures, and micropower shutdown and EMI suppression methods.

AN45 Measurement and Control Circuit Collection
A variety of measurement and control circuits are included in this application note. Eighteen circuits, including ultra-low noise amplifiers, current sources, transducer signal conditioners, oscillators, data converters and power supplies are presented. The circuits emphasize precision specifications with relatively simple configurations.

AN46 Efficiency Characteristics of Switching Regulator Circuits
Efficiency varies for different DC/DC converters. This application note compares the efficiency characteristics of some of the more popular types. Step-up, step-down, flyback, negative-to- positive, and positive-to-negative are shown. Appended sections discuss how to select the proper aluminum electrolytic capacitor and explain power switch and output diode loss calculations.

AN47 High Speed Amplifier Techniques
This application note, subtitled "A Designer's Companion for Wideband Circuitry," is intended as a reference source for designing with fast amplifiers. Approximately 150 pages and 300 figures cover frequently encountered problems and their possible causes. Circuits include a wide range of amplifiers, filters, oscillators, data converters and signal conditioners. Eleven appended sections discuss related topics including oscilloscopes, probe selection, measurement and equipment considerations, and breadboarding techniques.

AN48 Using the LTC Op Amp Macromodels
LTC's op amp macromodels are described in detail, along with the theory behind each model and complete schematics of each topology. Extended modeling topics are discussed, such as phase/frequency response modifications and asymmetric slew rate for JFET op amp models. LTC's macromodels are optimized for accuracy and fast simulation times. Simulation times can be further reduced by using streamlining techniques found throughout AN48.

AN49 Illumination Circuitry for Liquid Crystal Displays
Current generation portable computers and instruments utilize backlit liquid crystal displays. The back light requires a highly efficient, high voltage AC source as well as other supply circuitry. AN49 details these circuits and also includes sections on efficiency measurements and instrumentation considerations. A separate section discusses physical and layout considerations for the display.

AN50 Interfacing to Microprocessor Based 5V Systems
This application note discusses a variety of approaches for interfacing analog signals to 5V powered systems. Synthesizing a "rail-to-rail" op amp and scaling techniques for A/D converters are covered. A voltage-to-frequency converter, applicable where high resolution is required, is also presented.

AN51 Power Conditioning for Notebook and Palmtop Systems
Notebook and palmtop systems need a number of voltages developed from a battery. Competitive solutions require small size, high efficiency and light weight. This publication includes circuits for high efficiency 5V and 3.3V switching and linear regulators, back light display drivers and battery chargers. All the circuits are specifically tailored for the requirements outlined above.

AN52 Linear Technology Magazine Circuit Collection, Vol 1
This application note consolidates the circuits from the first few years of Linear Technology Magazine into one publication. Presented in the note are a variety of circuits ranging from a 50W high efficiency (>90%) switching regulator to steep roll-off filter circuits with low distortion to 12-bit differential temperature measurement systems.

AN53 Micropower High-Side MOSFET Drivers
This application note describes the operation of high-side N-channel MOSFET switch drivers designed specifically for operation in battery-powered equipment, such as notebook and palmtop computers and portable medical instruments. A selection guide simplifies the proper choice of MOSFET and driver for a particular high-side switch application. Circuits to drive and protect load impedances ranging from large inductors to large capacitors are described and a section on surface mount and copper clad shunts is included.

AN54 Power Conversion from Milliamps to Amps at Ultra High Efficiency (Up to 95%)
This application note discusses the use of the LTC1147, LTC1148, and LTC1149 ultra high efficiency switching regulators in a wide variety of applications. These controllers feature a current-mode architecture which includes an automatic low current operating mode called Burst Mode™ operation, making greater than 90% efficiencies possible at output currents as low as 10mA. This feature maximizes battery life while a product is in sleep or standby modes. In addition, the LTC1148 and LTC1149 are synchronous switching regulators which achieve high efficiency conversion from 10mA to 10A.

AN55 Techniques for 92% Efficient LCD Illumination
This publication details several LCD backlight circuits which feature 92% efficiency. Other benefits include low voltage operation, synchronizing capability, higher output power for color displays, and extended dimming range. Extensive coverage of practical issues includes lay out problems, multi-lamp displays, safety and reliability concerns and efficiency and photometric measurements. Also included is a review of circuits which did not work along with appropriate commentary.

AN56 "Better Than Bessel" Linear Phase Filters for Data Communications
The pace of the world of digital communications is increasing at a tremendous rate. Each day the engineer is requested to compact more data in the same channel bandwidth with closer channel spacing. This application note discusses some of the requirements and techniques for using the new LTC1064/1164 and LTC1264-7 filters which were designed specifically for digital communications. The terms "channel bandwidth," "eye diagrams" and "linear phase" filtering are discussed without the need for the "engineering speak" which permeates many textbook explanations of the same subjects.

AN57 Video Circuit Collection
AN57, the Video Circuit Collection, features a variety of video circuits designed at LTC. The LT1204 70MHz multiplexer is featured in a number of circuits which require excellent video isolation from channel to channel. High speed voltage and current feedback amplifiers are highlighted throughout the section on video processing circuits. There is a section on applying Current Feedback Amplifiers (CFAs) and a number of articles taken from the Linear Technology Magazine.

AN58 5V to 3.3V Converters for Microprocessor Systems
Many popular microprocessors operate from 3.3V supplies, yet they are used in systems where the predominate source of power is 5V. AN58 presents a collection of both linear and switching regulator solutions for conversion of 5V to 3.3V at currents ranging from 100mA to 20A. Applications information and a comparison of various bypass capacitor types is included. Most of the designs can be easily modified for other intermediate voltages such as 3.45V, 3.7V, and 4.1V.

AN59 Applications of the LT1300 and LT1301 Micropower DC/DC Converters
This note covers operation and applications of the LT1300 and LT1301 high efficiency micropower step-up DC/DC converter ICs. Internal operation of the ICs is described in detail. A variety of applications are presented, ranging from straightforward 2-cell to 5V converters and 5V to 12V converters to exotic transducer-based circuits such as flame detectors and CCFL drivers. Converters from both 2-cell and 4-cell inputs are included. Operating hours at various load currents are presented and relative merits of different battery types are discussed.

AN60 PCMCIA Card and Card Socket Power Management
Most portable systems have expansion sockets conforming to the standards set by the Personal Computer Memory Card International Association (PCMCIA). This standard requires the host to perform an unusual amount of switching on both the V_{CC} and VPP voltage lines. Card designers face difficult power management and DC/DC conversion issues of their own. Board real estate and component height are at a premium making design difficult and component selection critical. This application note discusses in detail both the host and card designer issues and highlights several new products designed specifically for these applications.

AN61 Practical Circuitry for Measurement and Control Problems
This collection of circuits was worked out between June 1991 and July of 1994. Most were designed at customer request or are derivatives of such efforts. Types of circuits include power converters, transducer signal conditioners, amplifiers and signal generators. Specific circuits include low noise amplifiers, high power single cell DC/DC converters, portable high accuracy barometers, a 10mHz 1% accuracy RMS/DC converter, and random noise generators. Appended sections cover noise theory and present a historical perspective of wideband amplifiers.

AN62 Data Acquisition Circuit Collection
This application note presents a wide variety of data acquisition circuits. The detailed circuit schematics cover 8-, 10-, and 12-bit ADC and DAC applications, serial and parallel digital interfaces, battery monitoring, temperature sensing, isolated interfaces, and connections to various popular microprocessors and microcontrollers. An appendix covers suggested voltage references.

AN63 Power Supply Modules for the P54C-VR Pentium® Microprocessor
This application note describes the design of both linear and switching regulators which provide power for 90MHz Pentium processors. The circuits are intended to comply with Intel's modular power supply specification and provide sufficient power for cache RAM and chip sets in addition to the CPU. They are also capable of providing the additional power required by an upgrade "overdrive" processor.

Burst Mode is a trademark of Linear Technology Corporation.
Pentium is a registered trademark of Intel Corporation.

Design Notes

DESIGN NOTE 1
New Data Acquisition Systems Communicate With Microprocessors Over Four Wires

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Sampling Of Signals For Digital Filtering And Gate Measurements

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Operational Amplifier Selection Guide For Optimum Noise Performance

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Temperature Measurement Using The LTC1090/91/92 Series Of Data Acquisition Systems

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C-Load and SafeSlot are trademarks of Linear Technology Corporation.
LocalTalk is a registered trademark of Apple Computer, Inc.

Applications on Disk

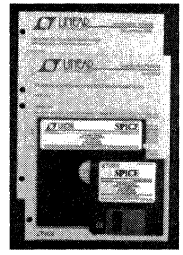
NOISE DISK

This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise, and calculate noise using specs for any op amp.

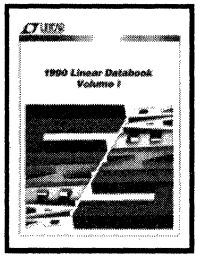
SPICE MACROMODEL DISK

This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models, and a demonstration copy of PSpice™ by MircoSim. Also included are Application Notes 41 and 48 which describe the macromodels.

PSpice is a trademark of MicroSim Corporation.

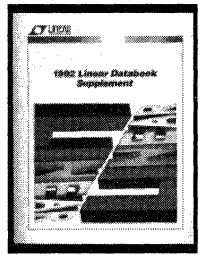


Technical Publications



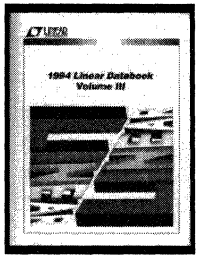
1990 Linear Databook, Vol I — This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

$10.00



1992 Linear Databook Supplement (will become the 1992 Linear Databook, Vol II) — This 1248 page supplement to the *1990 Linear Databook* is a collection of all products introduced in 1991 and 1992 The catalog contains full data sheets for over 140 devices. The *1992 Linear Databook Supplement* is a companion to the *1990 Linear Databook*, which should not be discarded. $10.00

$10.00

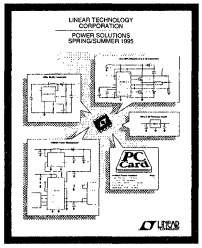


1994 Linear Databook, Vol III — This 1826 page supplement to the *1990 and 1992 Linear Databooks* is a collection of all products introduced since 1992. A total of 152 product data sheets are included with updated selection guides. The *1994 Linear Databook Vol III* is a companion to the *1990 and 1992 Linear Databooks*, which should not be discarded. $10.00

$10.00

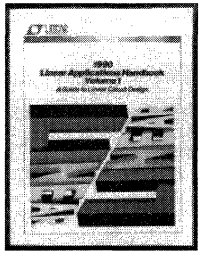
To Order These Publications Call Toll Free 1-800-4-LINEAR

Technical Publications



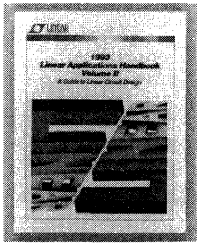
Power Solutions Brochure —
This 64 page collection of circuits contains real-life solutions for common power supply design problems. There are over 45 circuits, including descriptions, graphs and performance specifications. Topics covered include PCMCIA power management, microprocessor power supplies, portable equipment power supplies, micropower DC/DC, step-up and step-down switching regulators, off-line switching regulators, linear regulators and switched capacitor conversion.

Interface Product Handbook —
This 424 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422, V.35 and AppleTalk applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, mixed RS232 and RS485 devices, 10kV ESD protection of RS232 devices and surface mount packages.



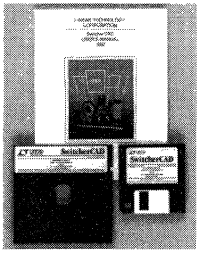
$20.00

1990 Linear Applications Handbook • Volume I —
928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00



$20.00

1993 Linear Applications Handbook • Volume II —
Continues the stream of "real world" linear circuitry initiated by the *1990 Handbook*. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. Additionally, references and articles from non-LTC publications that we have found useful are also included. $20.00



$20.00

SwitcherCAD Handbook —
This 144 page manual, including disk, guides the user through SwitcherCAD – a powerful PC software tool which aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. $20.00

To Order These Publications
Call Toll Free 1-800-4-LINEAR

QUICK REFERENCE INDEX

Note: All products in **BOLD** are in this Databook, others appear in LTC's 1990, 1992 and 1994 Databooks ('90DB = LTC's 1990 Databook, '92DB = LTC's 1992 Databook Supplement and '94DB = LTC's 1994 Databook).

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