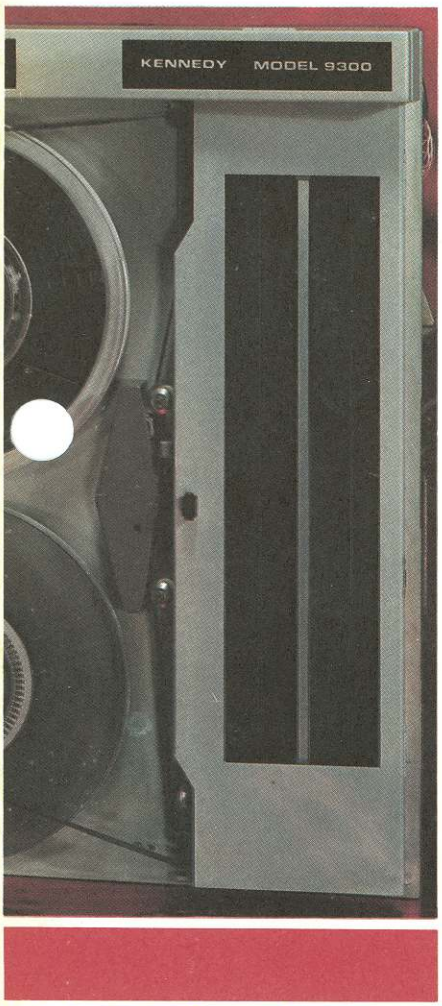
Operation and Maintenance Manual

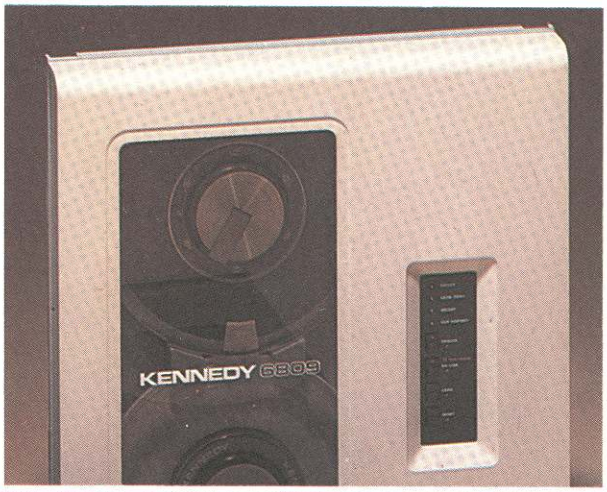
KENNEDY

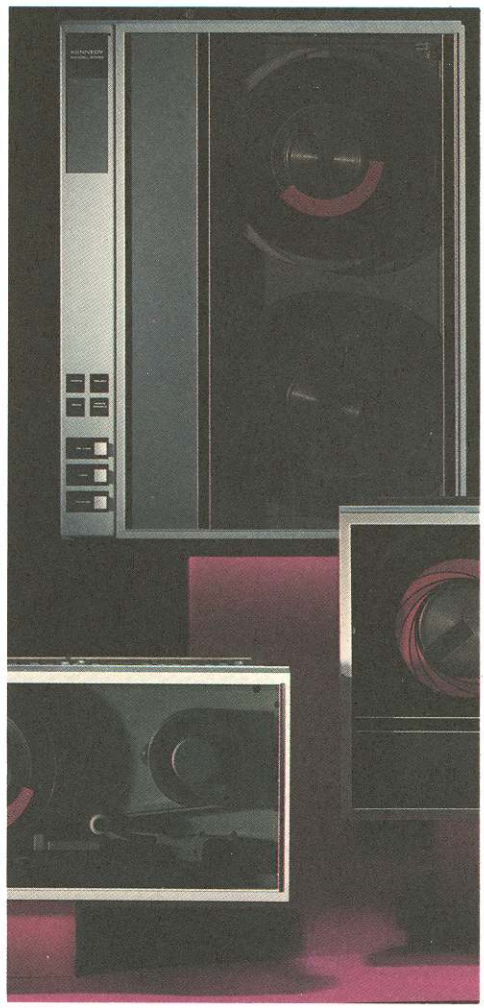
ALLEGHENY INTERNATIONAL

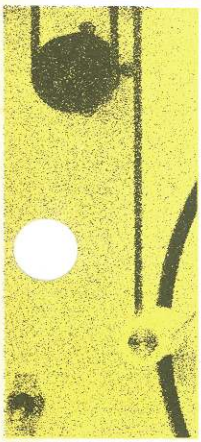
Model 5380

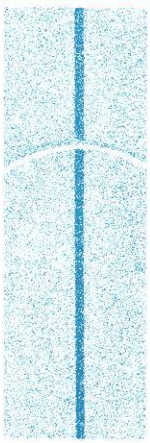
Fixed Disk Drive

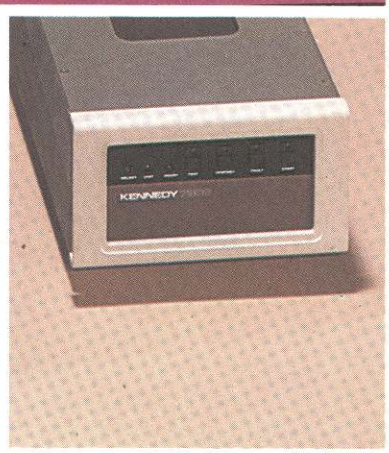












FCC NONCERTIFIED EQUIPMENT

Warning: This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

SECTION I

APPLICATION DATA

1.1 INTRODUCTION

The Kennedy Model 5380 disk drive, using Winchester technology, offers 80 megabytes of unformatted data storage capacity at a low cost per bit. The high storage capacity is achieved by converting input NRZ data supplied by the controller into modified frequency modulation (MFM) format prior to recording it. The MFM format utilizes a recording density of up to 6330 bits per inch with a track density of 429 per inch. With a platter revolution rate of 3000 rpm, the data transfer rate of the Model 5380 is 1 megabyte per second. During a read operation the internal electronics of the 5380 convert the MFM data back to NRZ prior to returning it to the controller.

The bottom surface of the lowest disk is prerecorded with servo tracks. The servo track information ensures accurate read alignment, essential for dependable data recovery. The servo track output is also used to provide timing information to the controller, eliminating possible timing errors due to different cable lengths.

The Model 5380 is designed for compactness and ease of maintenance and service. While occupying only 7 inches of vertical space in a standard 19 inch wide rack (with a depth of 24.75 inches) the Model 5380 electronics are easily accessible. The bulk of the electronics are located on small, replaceable PC boards that facilitate troubleshooting and minimize down time. A Fault PC board pinpoints existing faulty conditions using a set of 9 indicator LEDs.

The features included are:

* Closed loop air filtration
* Daisychaining of up to four drives
* Address mark capability for variable length records
* Built-in power supply
* Easy service access
* Small easily replaceable PC boards
* SMD interface
* Dynamic braking
* Mechanical braking (optional)

1.2 ELECTRICAL AND MECHANICAL SPECIFICATIONS

Data capacity (unformatted 8 bit bytes)

Per surface	16M bytes
Per track	20,160 bytes
Per cylinder	201,600 bytes
Per drive	80M bytes

Cylinders per surface	412
Tracks per surface	823

Processing speed

Data transfer rate	1M byte/second
Bit rate	8.0 MHz
Spindle speed	3000 rpm

Accessing time

Full stroke	65 msec (max)
Average	35 msec
One track	10 msec (max)

Number of sectors	1-256 (switch selectable)
Recording method	Write compensated MFM
Number of heads	10 plus servo head
Operator controls	Start/stop switch
Indicators	Start Select Ready Fault (9 different fault indicators on Fault PC board)

Dimensions (see figure 1-1)

Disk drive mounting	Standard 19 inch (48.26 cm) RETMA rack
Height	7 inches (17.78 cm)
Width	19 inches (48.26 cm)
Depth overall	24.75 inches (62.86) cm)
Weight	75 pounds (34 Kgm)
Shipping weight	90 pounds (41 Kgm)

Operating environment

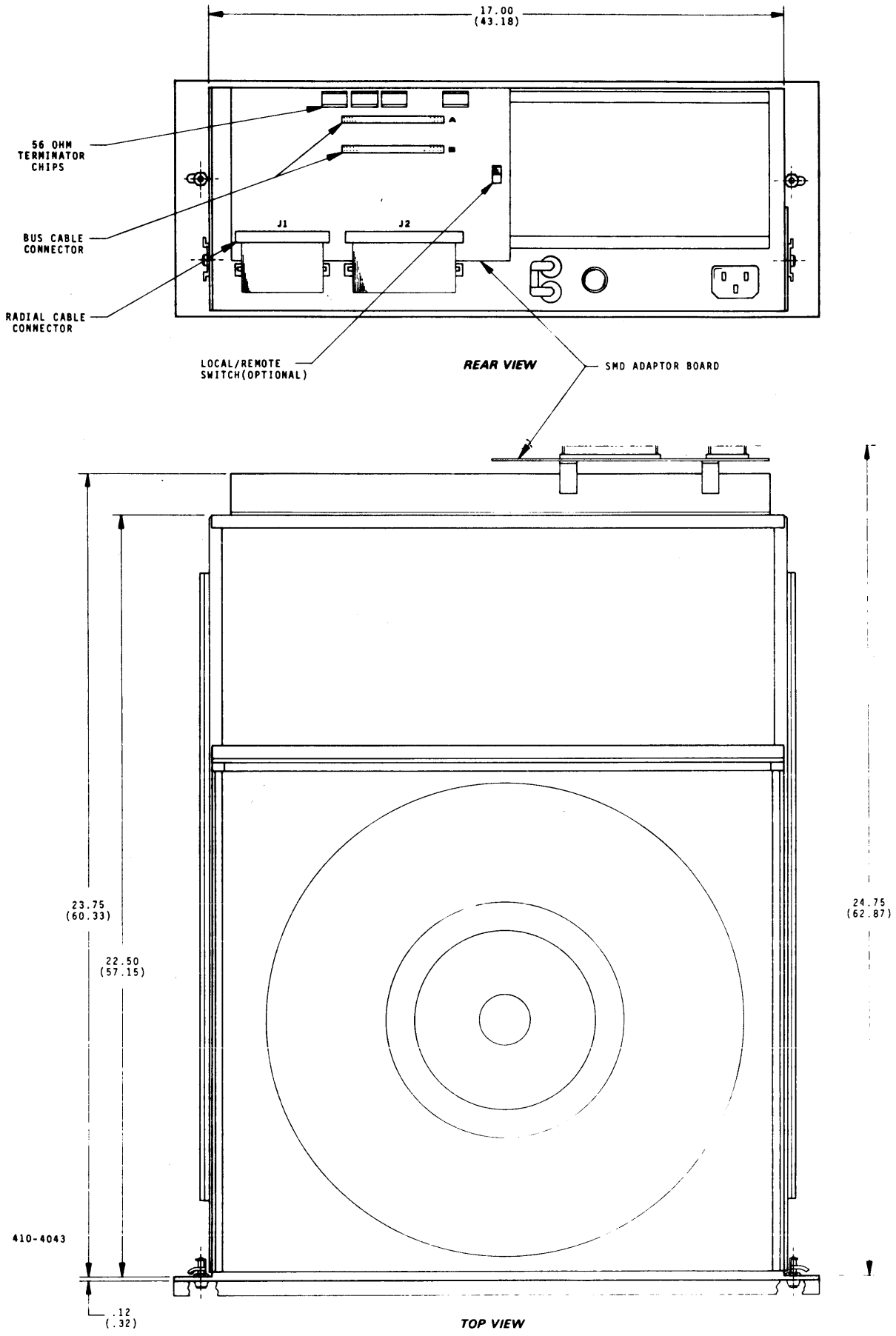
Ambient temperature	$+10^{o}$ to $+40^{o}$C ($+50^{o}$ to $+104^{o}$F)
Relative humidity	20% to 80%
Storage temperature	-10^{o} to 50^{o}C (14^{o} to 122^{o}F)

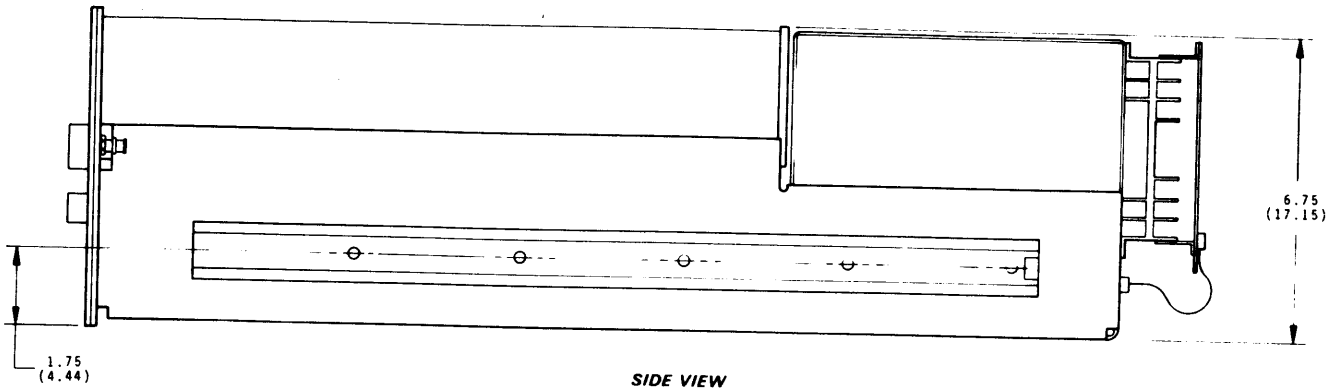
Power requirements

115 +/- 10% vac, 60 Hz standard
220/230/240 +/- 10% vac, 50 Hz optional

1.3 INTERFACE CONNECTIONS

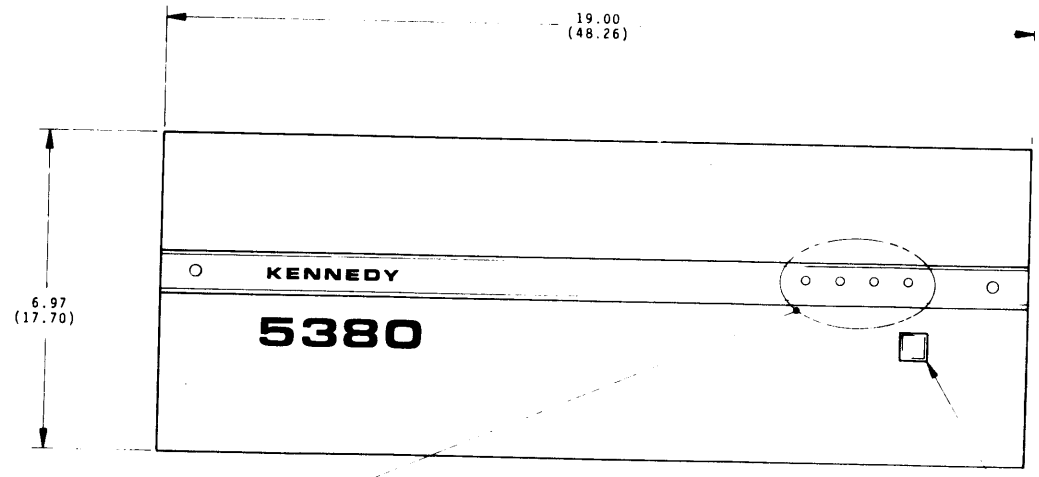
The Model 5380 interface includes a radial high speed cable for write/read data and clock transmission, and a bus cable for control and address signal transmission. The bus cable allows for the daisychaining of up to four disk drives to a single controller. The write clock, timed to the servo track, is transmitted to the controller for data synchronization and then returned to the drive, eliminating the need for accurate cable lengths.


17.00
(43.18)
56 OHM
TERMINATOR
CHIPS
BUS CABLE
CONNECTOR
RADIAL CABLE
CONNECTOR
J1
J2
LOCAL/REMOTE
SWITCH(OPTIONAL)
REAR VIEW
SMD ADAPTOR BOARD
23.75
(60.33)
22.50
(57.15)
24.75
(62.87)
410-4043
.12
(.32)
TOP VIEW



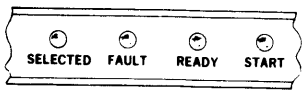
SIDE VIEW

FIRST DIMENSIONS SHOWN IN INCHES.
DIMENSIONS IN PARENTHESES ARE IN CENTIMETERS.



FRONT VIEW

START PUSH BUTTON



INDICATOR LEDS

310-4043

Figure 1-1.
Outline and Installation Drawing
Model 5380

Both the radial and bus interfaces utilize 3M flat cables and connectors. The bus cable is a 60 conductor 3M ribbon cable that should not exceed 100 feet in length. Each signal of the differential pairs on the bus cable is terminated with 56 ohm resistance to ground, matching the characteristic impedance of the cable. The exceptions are the optional Pick and Hold lines and the Open Cable Detect line, which are not terminated in the controller. Note that in daisychained units the terminating resistance should be installed in the controller and in the physical last drive only. All other drives should have the 56 ohm terminator chips removed from the SMD Adaptor board on the back of the drive. The pin list of the bus cable is shown in figure 1-2. When daisychaining units connect controller to bus connector A, connect bus connector B to bus connector A of next unit, and so on.

The radial cable has 26 conductors and should not exceed 50 feet in length. Each radial cable signal is terminated with a 62 ohm resistance to ground. The pin list of the radial cable is shown in figure 1-3.

1.4 INTERFACE SIGNAL DESCRIPTION

1.4.1 COMMAND SIGNALS

UNIT SELECT
FSEL0/ J4-53(+), 23(-)
FSEL1/ J4-54(+), 24(-)

The binary code on these lines selects one of up to four disk drives. The leading edge of FSEL0/; FSEL1/ must occur simultaneously and 200 ns prior to the leading edge of FSELTAG true, which enables unit selection. The UNIT SELECT signals must remain true at least 200 ns after the leading edge of FSELTAG true, as shown in figure 1-12.

UNIT SELECT TAG
FSELTAG/ Level J4-52(+), 22(-), see figure 1-12

When true, this level enables unit selection. It shall go true 200 ns after the leading edges of FSEL0/; FSEL1/ true. It shall remain active throughout the entire period the disk drive is commanded, status is read or data is transferred. It need not remain active after a SEEK or RESTORE operation has been initiated.

F BUS LINES
FBUS0-9/

These lines are multiplexed disk drive inputs providing either a 10 bit cylinder address, a 3 bit head address, or a control command depending on whether FCYLTAG/, FHDTAG/ or FCMDTAG/ is true. For pin assignments see pin list in figure 1-2.

CYLINDER SELECT
FCYLTAG/ Pulse J4-31(+), 1(-1)

When true, this pulse initiates a SEEK operation to the cylinder whose 10 bit address is on BUS lines. The bus lines should be stable throughout the tag time.

HEAD SELECT
FHDTAG/ Pulse J4-32(+), 2(-)

When true, this pulse causes selection of the head addressed by F Bus lines 0-2.

COMMAND SELECT
FCMDTAG/ Level J4-33(+), 3(-)

When true this level enables controller commands for its duration. It must be held true for the entire operation.

WRITE GATE
FBUS0/ Level J4-34(+), 4(-)

When true, this level enables the write driver.

READ GATE
FBUS1/ Level J4-35(+), 5(-)

When true, this level enables digital read data. The read chain synchronizes on an all zeros pattern on the leading edge of the read gate signal.

FAULT CLEAR
FBUS4/ Pulse J4-38(+), 8(-)

This is a 100 nsec (min) pulse which clears the fault logic.

AM ENABLE
FBUS5/ Level J4-39(+), 9(-)

When AM (Address Mark) ENABLE is true together with either a write or read gate, address marks may be written or read. When used in conjunction with a write gate, the writer stops toggling and data is erased to create an address mark. Write fault detection is inhibited by this signal.

Note: FBUS5 must be held inactive during command select functions if the address mark will not be used.

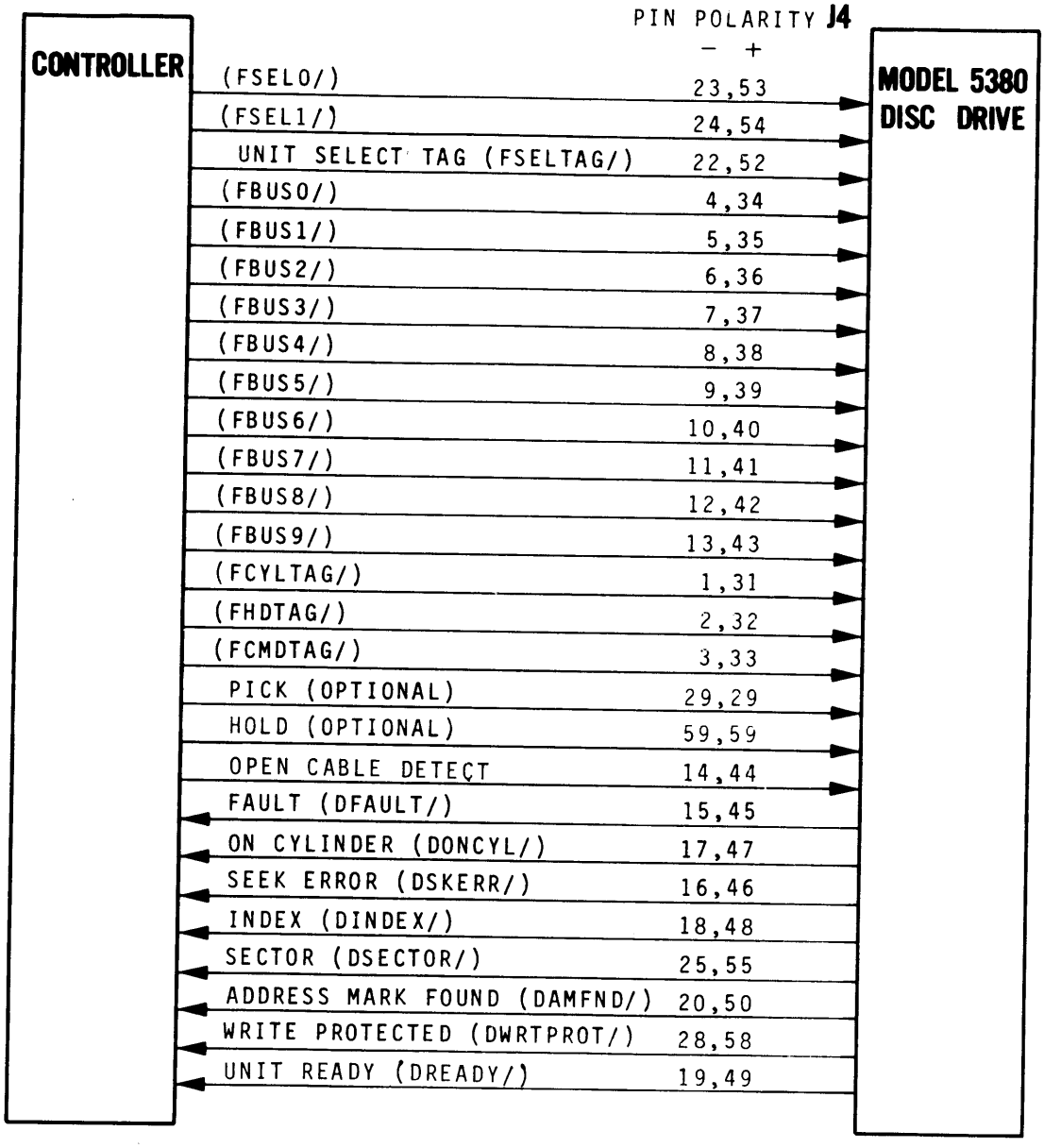
When AM ENABLE is applied in conjunction with a read gate, an analog voltage comparator will detect the absence of read data and flag an address mark in any read data gaps greater than 20 bits and less than 28 bits.

RTZ
FBUS6/ Pulse J4-40(+), 10(-)

This pulse (100 nsec min/100 usec max) will cause the head positioner to seek track 0, clear the seek error flip-flop and reset the head register.

KENNEDY 14 INCH FIXED DRIVE

BUS CABLE



	FBUS0/ THROUGH FBUS9/									
	9	8	7	6	5	4	3	2	1	0
FCYLTAG/*	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
FHDTAG/**								2^2	2^1	2^0
FCMDTAG/		STROBE LATE	STROBE EARLY	RTZ	AM ENABLE	FAULT CLEAR			READ	WRITE

* MAXIMUM CYLINDER ADDRESS = DECIMAL 822.
** MAXIMUM HEAD ADDRESS = DECIMAL 4.

110-0202

Figure 1—2. Bus Cable Pin List

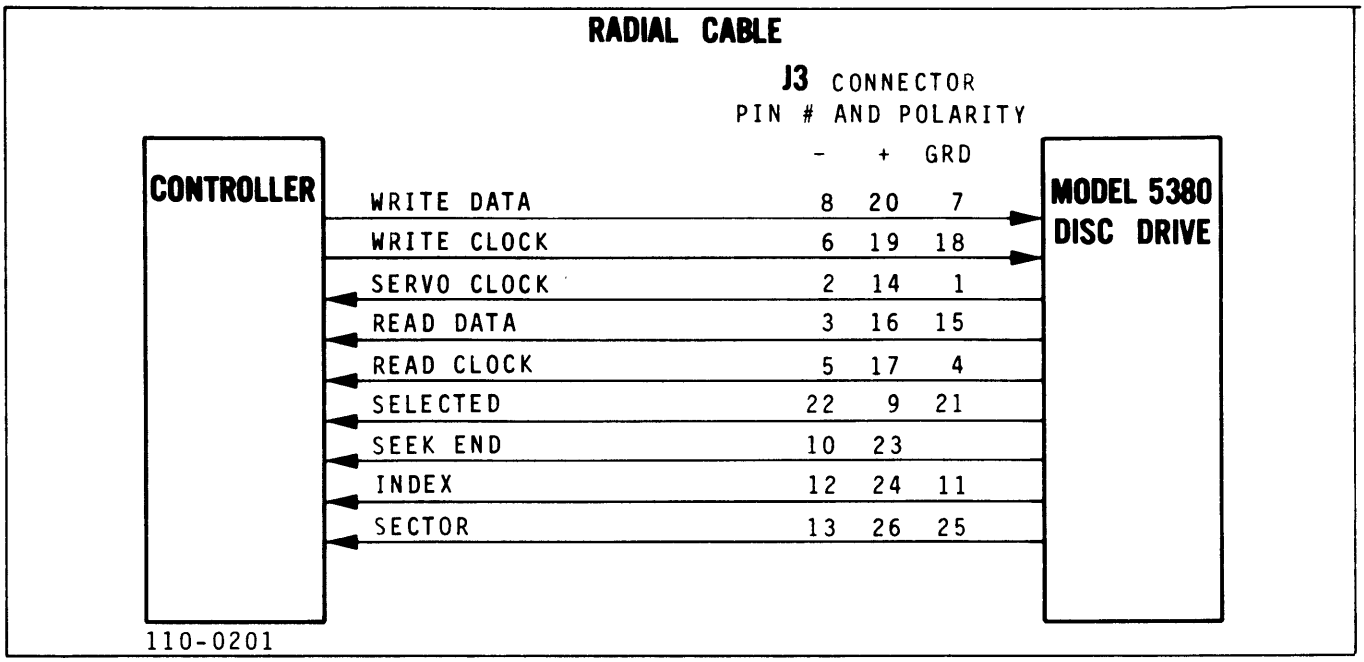


Figure 1—3. Radial Cable Pin List

This pulse should be used only for recalibration, since it is significantly longer than a nominal seek to track 0.

DATA STROBE EARLY
FBUS7/ Level J4-41(+), 11(-)

A true condition on this line causes the Read Data Separator in the disk drive to strobe data earlier than optimum strobe timing. Used for recovering marginal data.

DATA STROBE LATE
FBUS8/ Level J4-42(+), 12(-)

A true condition on this line causes the Read Data Separator in the disk drive to strobe data later than optimum strobe timing. Used for recovering marginal data.

1.4.2 STATUS SIGNALS

(Active low disk drive outputs are supplied only when disk drive is selected.)

UNIT READY
DREADY/ Level J4-49(+), 19(-)

When true the disk is up to speed. The heads are loaded and no fault condition exists. UNIT READY will be dropped after a load sequence if servo track pulses are not sensed within 350 msec. Further load attempts will require operator intervention.

FAULT
DFAULT/ Level J4-45(+), 15(-)

When true, some of the following disk drive faults have occurred: DC Power Fault, Write Fault, Head Select Fault, Write or Read while Off Cylinder, or Write Gate true during a read operation. DFAULT true immediately inhibits writing to prevent possible data erasure. Here is a description of some fault types cited above. Faults not described are self-explanatory.

DC Power Fault: Abnormal DC voltage

Head Select Fault: More than one head selected

Write Fault: Abnormally low write current/no write transitions

A FAULT CLEAR · COMMAND SELECT, will clear the FAULT line, provided no fault now exists. Fault conditions are stored in flip-flops for maintenance aid and may be cleared by means of a fault clear switch on the fault card.

SEEK ERROR
DSKERR/ Level J4-46(+), 16(-)

When true, a seek error has occurred and may be cleared only by performing an RTZ. DSKERR true indicates:

a. the unit couldn't complete a SEEK within 500 msec, or

b. an address greater than track 822 was selected, or

c. the carriage has moved outside the recording field. Where the address exceeds 822 tracks the seek error signal goes true within 200 nsec of FCYLSEL/. No carriage movement occurs.

ON CYLINDER
DONCYL/ Level J4-47(+), 17(-)

When true, this signal indicates the heads are positioned over a track.

INDEX
DINDEX/ Pulse J4-48(+), 18(-)

This pulse occurs once per disk revolution and defines sector zero. Width is nominally 2.5 microseconds. This pulse is derived from the servo track on the bottom of the disk.

SECTOR MARK
DSECTOR/ Pulse J4-55(+), 25(-)

This mark is also derived from the servo track on the bottom of the disk. The number of sectors per revolution is determined by counting servo track pulses. Timing integrity is maintained throughout seek operations. The number of sectors is switch selectable. Nominal width is 1.25 microseconds.

ADDRESS MARK FOUND
DAMFND/ Pulse J4-50(+), 20(-)

When true, this pulse indicates at least 20, but not more than 28, missing data transitions have occurred, together with the first zero of an all zeros pattern. The controller should now drop ADDRESS MARK ENABLE following DAMFND/ true. Nominal width is 8 microseconds.

WRITE PROTECTED
(DWRTPROT/) Level J4-58(+), 28(-)

When DWRPROT/ is true, the write driver has been disabled to prevent data destruction.

OPEN CABLE DETECT
Level J4-14(-), 44(+)

This line disables the interface in the event that the Bus Cable is disconnected or the controller loses power. Generation of this signal in the Controller should be the last step in a power up sequence or the first step in a power down sequence. No 56 ohm terminators should be used at the controller on this line. If the circuit is driven by 75110 transmitters and four drives are daisychained, two transmitters should be connected in parallel to drive this line.

UNIT SELECTED
DSELECTED/ Level J3-9(+), 22(-), 21(GRD), radial cable

DSLECTED goes true within 300 ns after disk drive selection and will remain true not longer than 300 ns after the disk drive has been deselected.

SEEK END
DSEEK END/ Level J3-23(+), 10(-)

This signal goes true when either SEEK ERROR or ON CYLINDER is true. Thus a seek operation has been terminated.

1.4.3 DATA AND CLOCK SIGNALS

WRITE DATA POSITIVE
FWDAT J3-20(+), 8(-), 7(GRD)

These differential signals input NRZ data to the disk drive. Writing will occur so long as WRITE GATE COMMAND SELECT is active and the unit is READY and ON CYLINDER.

WRITE CLOCK POSITIVE
FWCLK Pulse J3-19(+), 6(-), 18(GRD)

This differential clock pulse must be used to synchronize the NRZ write data.

SERVO CLOCK
DSRVCLK Pulse J3-14(+), 2(-), 1(GRD)

This is a differential, phase locked 8 MHz clock generated from the servo track pulses on the bottom of the lower disk.

READ DATA
DRDAT Pulse J3-20(+), 8(-), 7(GRD)

These lines output recovered NRZ read data from the disk drive.

READ CLOCK
DRDCLK Pulse J3-17(+), 5(-), 4(GRD)

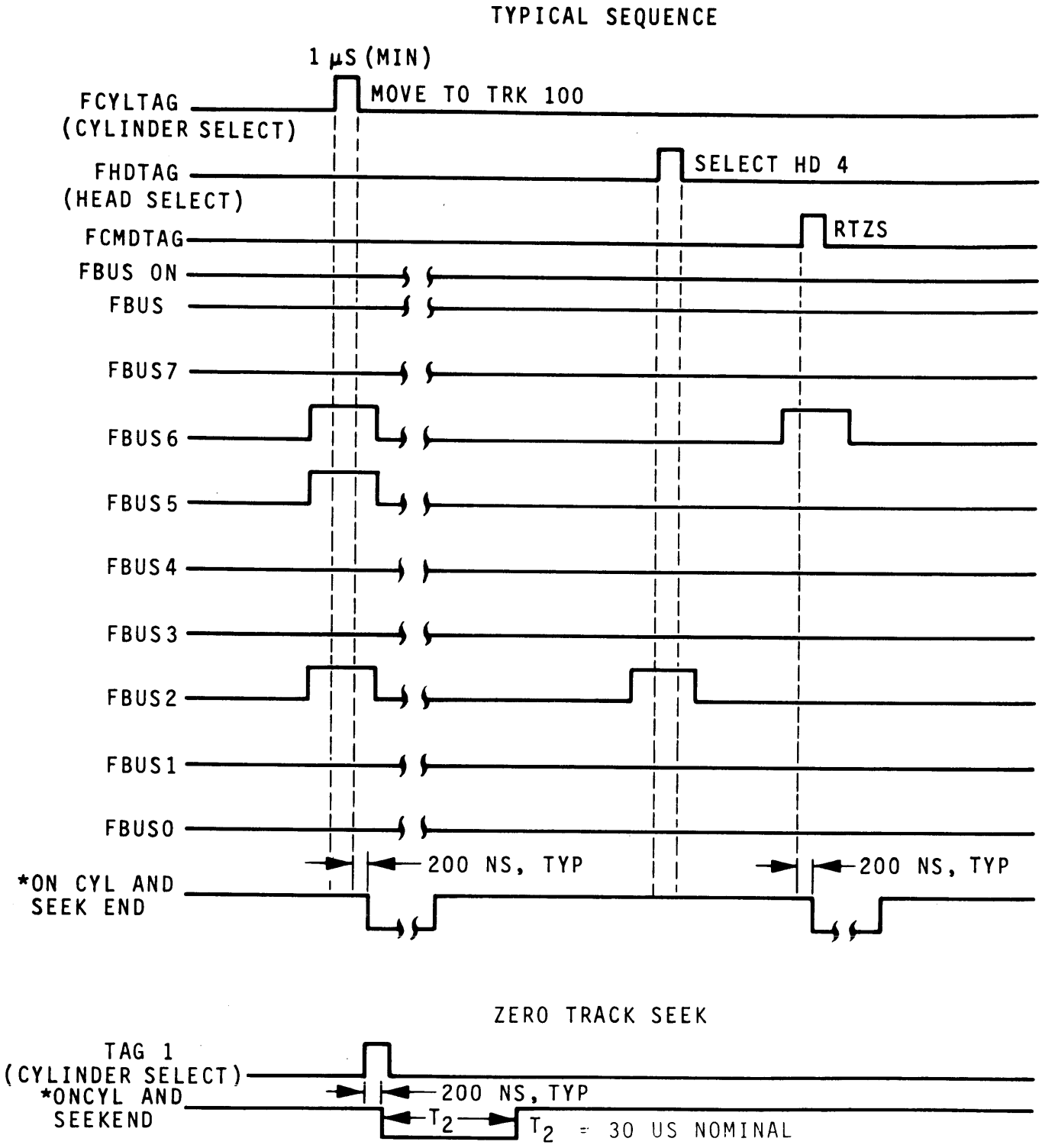
This clock is derived internally and is synchronous with detected read data so that the negative edge of the clock precedes significant edge of the data by 6 (+/-4) ns at the I/O connector.

INDEX
DINDEX/ Pulse J3-24(+), 12(-), 11(GRD)

This is the same INDEX signal output on the bus cable.

SECTOR MARK
DSECTOR/ Pulse J3-26(+), 13(-), 25(GRD)

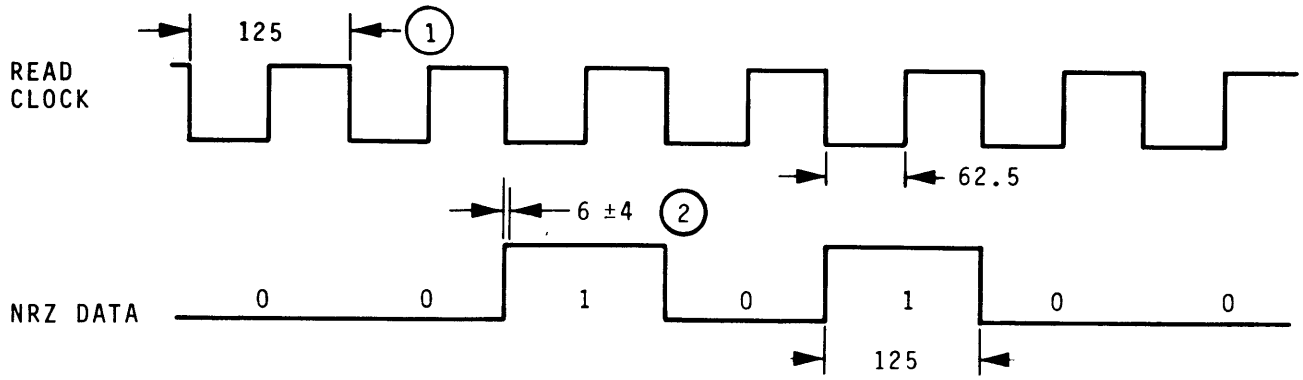
This is the same SECTOR MARK signal output on the bus cable.



*ONCYL AND SEEKEND SIGNALS ARE IDENTICAL UNLESS SEEK ERROR OCCURS. SEEK ERROR INITIATES A CONSTANT SEEKEND. TIMING SHOWN IS AT THE INPUT TO THE 75110 DIFFERENTIAL LINE DRIVERS.

110-0162

Figure 1-4. Tag and Bus Timing

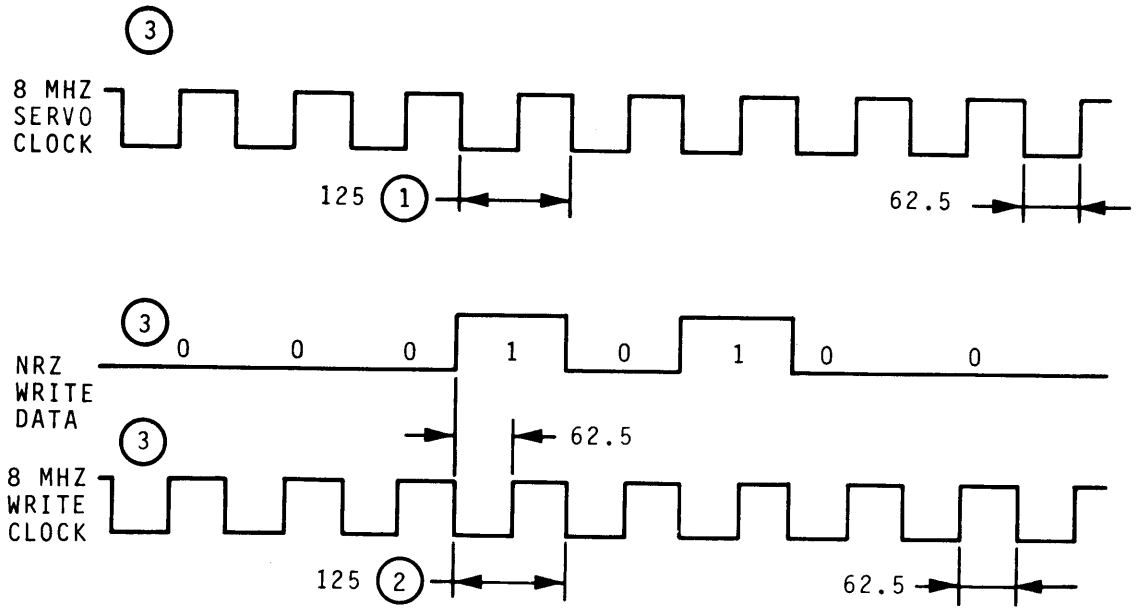


NOTES:

1. ALL TIMES IN NSEC.
2. NEGATIVE EDGE OF CLOCK PRECEDES SIGNIFICANT EDGE OF DATA AT I/O CONNECTOR.

110-0159

Figure 1-5. Read Data Timing



NOTES:

1. ALL TIMES IN NS
2. SIMILAR PERIOD SYMMETRY SHALL BE ·15 NS AT I/O CONNECTOR IN DRIVE SPEED VARIATION TOLERANCE SHALL BE ±5% OF PERIOD WHICH INCLUDES SPINDLE SPEED TOLERANCE AND DIBIT DROPOUT WHILE CARRIAGE IS MOVING.
3. AT I/O CONNECTOR IN CONTROLLER.

110-0158

Figure 1-6. Write Data/Servo Clock Timing

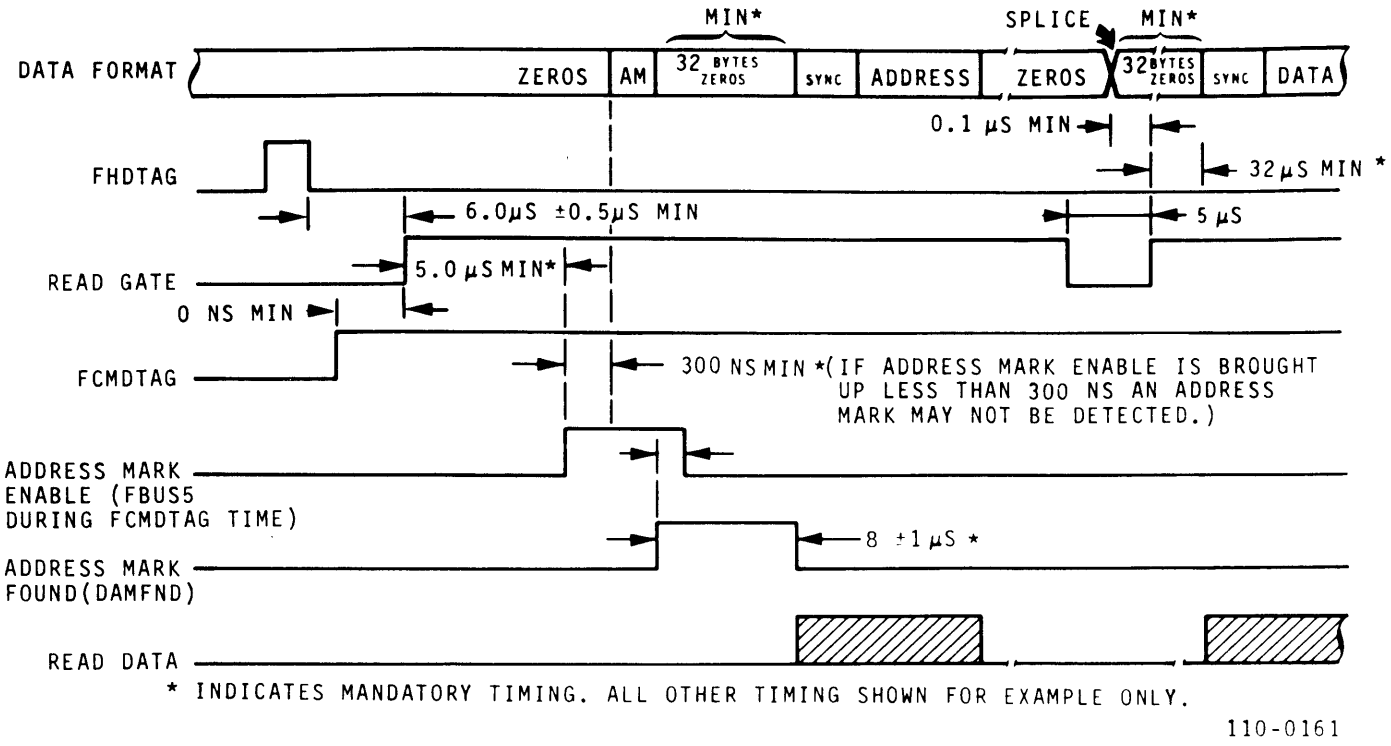
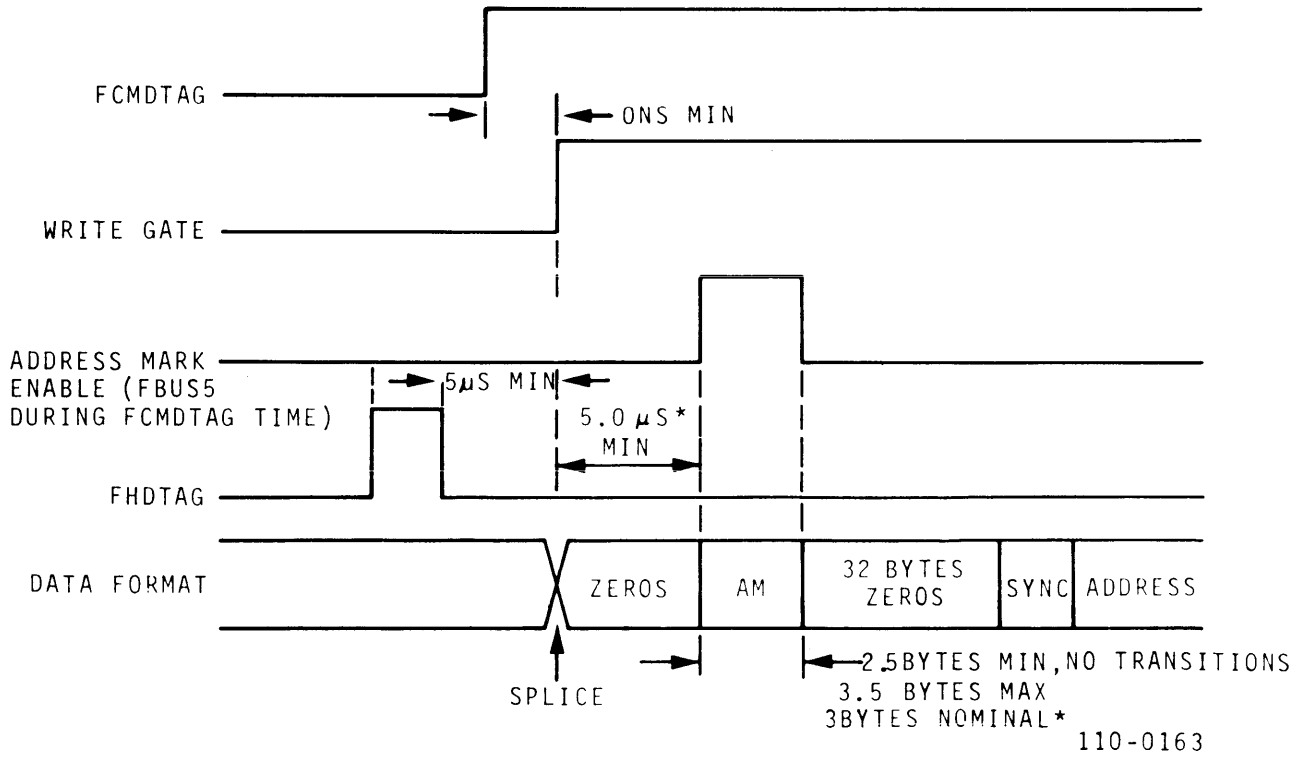
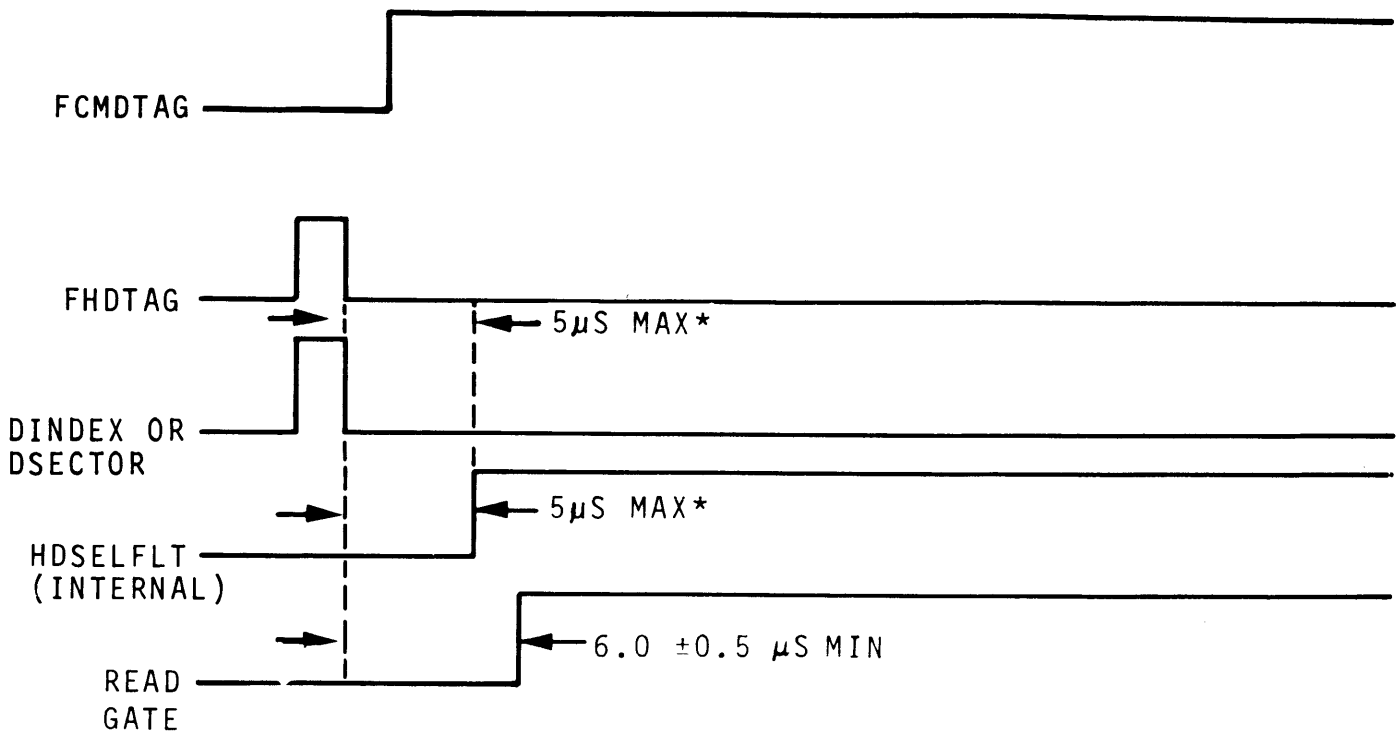


Figure 1-7. Read Timing (Address Mark time)

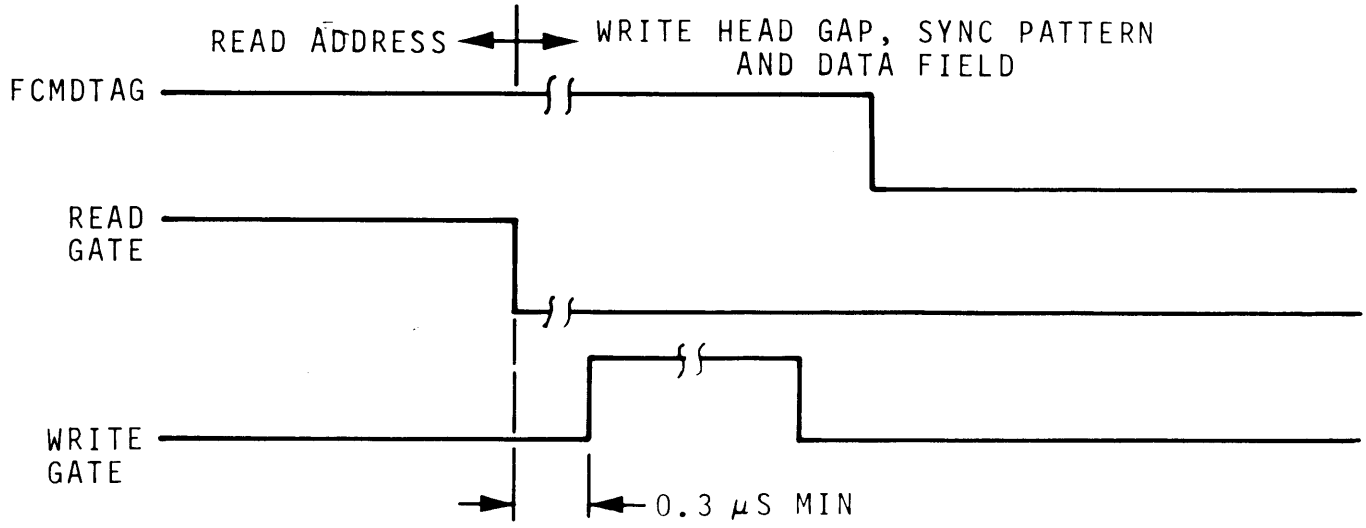


* INDICATES MANDATORY TIMING. ALL OTHER TIMING SHOWN FOR EXAMPLE ONLY.

Figure 1-8. Write Timing (Address Mark time)



A. TYPICAL READ CONTROL TIMING



B. TYPICAL WRITE CONTROL TIMING

*INDICATES MANDATORY TIMING. ALL OTHER TIMING SHOWN FOR EXAMPLE ONLY.

110-0160

Figure 1-9. Control Timing

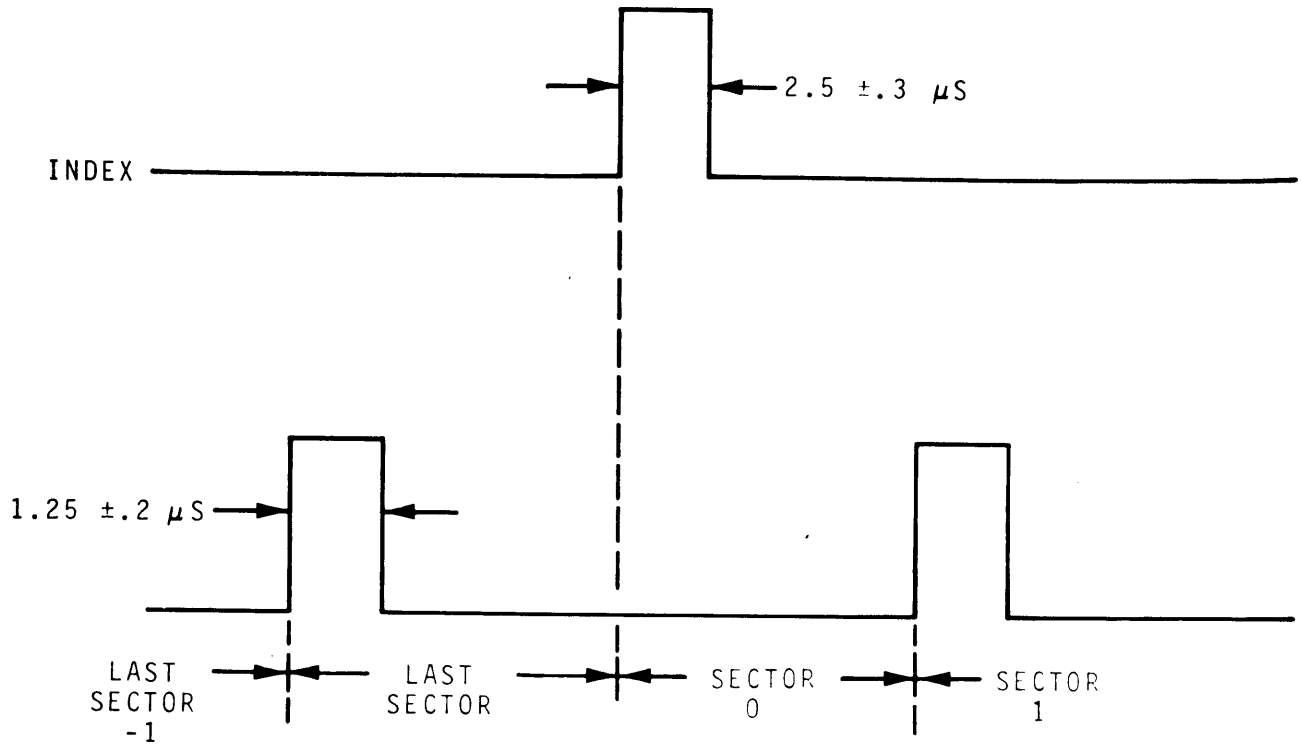
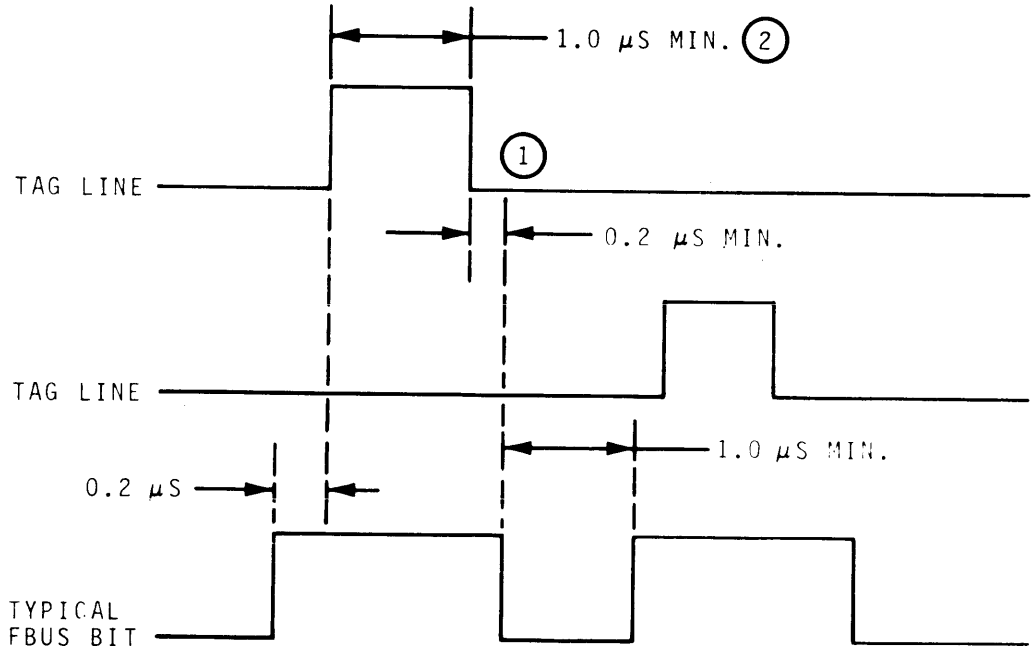


Figure 1-10. Index and Sector Timing



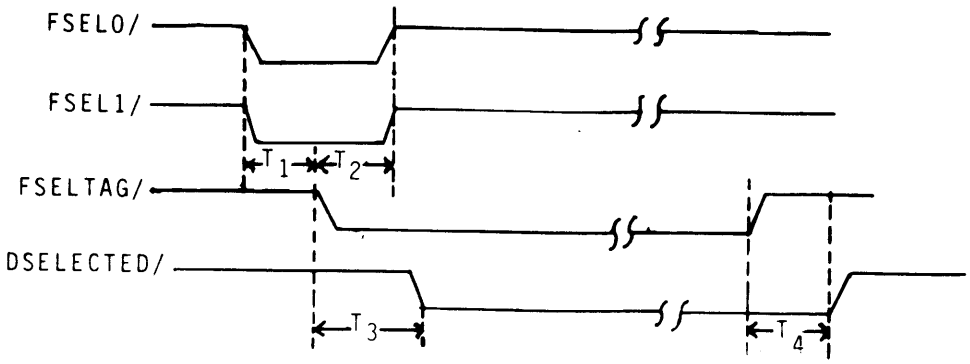
NOTES

(1) DOES NOT APPLY TO CONTROL SELECT FUNCTIONS.

(2) FCYLTAG MAX. LENGTH IS 0.5 MS.

110-0164

Figure 1-11. Tag Line/Bus Timing Tolerance



110-0176

T_1 = 200ns minimum
T_2 = 200ns minimum
T_3 = 300ns maximum
T_4 = 300ns maximum

Figure 1-12. Disk Drive Selection Timing

SECTION II

INSTALLATION AND OPERATION

2.1 INSTALLATION

2.1.1 INSPECTION

Prior to installation thoroughly inspect the disk drive and remove any foreign material which may have become lodged in the drive mechanism. Also, disable the spindle and position arm restraints per the packing labels. The Model 5380 incorporates an improved actuator arm lock which automatically locks the arm when power is removed. When unpacking or reshipping the 5380, only the spindle lock needs to be manually locked with a screwdriver. This lock is identified on the bottom cover.

2.1.2 MOUNTING

Physical dimensions of the disk drive are provided in the outline and installation drawing, figure 1-1. The disk drive requires 7 inches vertical space in standard 19 inch wide rack. For daisychain applications, the maximum bus cable length is 100 feet. The maximum radial cable length is 50 feet.

When mounting the series 5380 disk drive in a cabinet, please ensure that there is sufficient clearance around the unit to allow unobstructed air flow.

In addition, forced air circulation may be required to maintain the maximum air temperature around the drive below 40°C. A temperature indication label has been attached to the left side panel. If the surface temperature indicated exceeds 54°C, insufficient cooling has been provided.

2.1.3 SERVICE ACCESS

Most of the PC boards are socket-connected to the masterboard and are removed from the top of the disk drive.

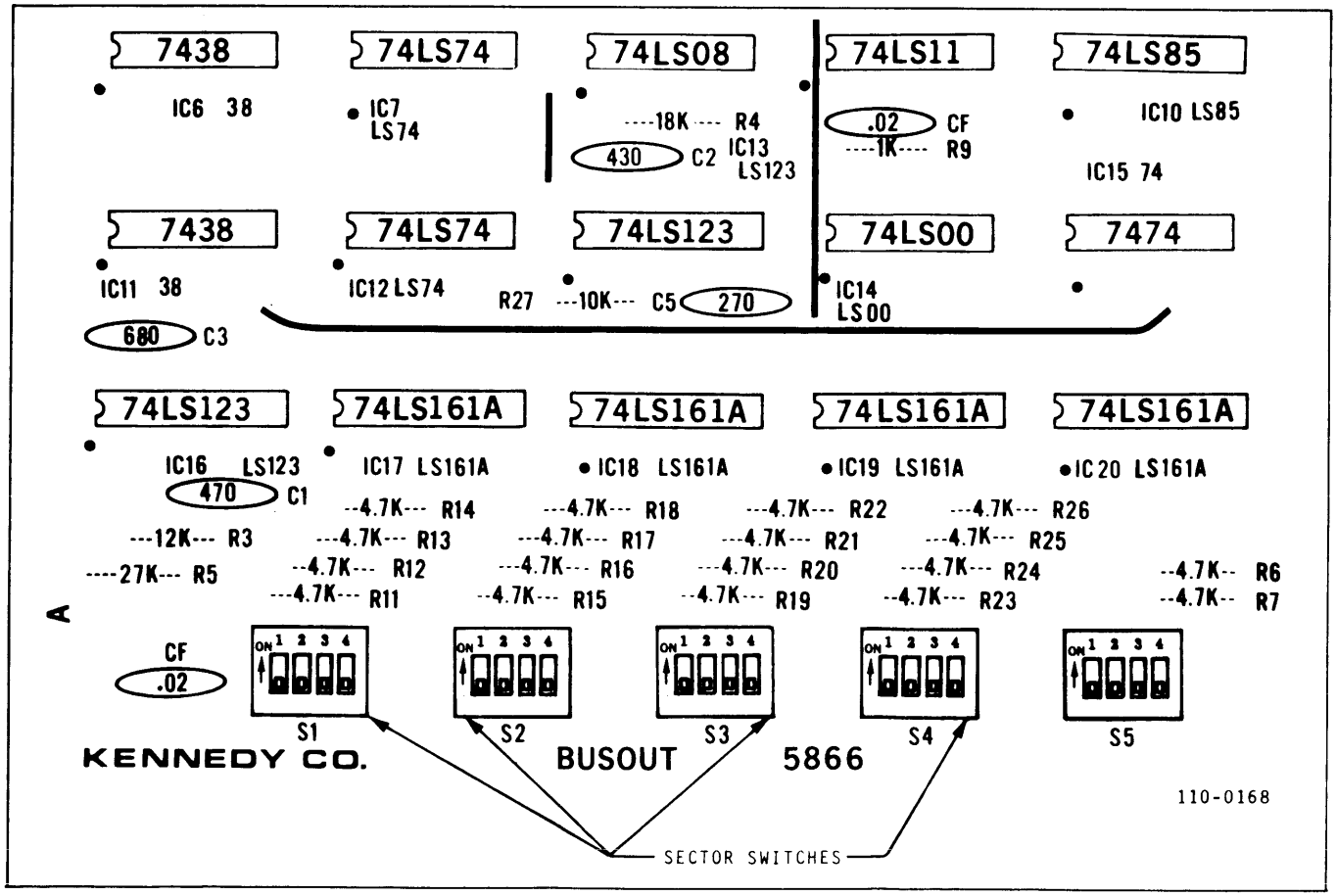


Figure 2-1. Sector Switches, Busout Board

The power supply/disk drive motor assembly can be detached as a unit. The Model 5380 incorporates twin circuit breakers connected in series with the positive and negative primary input lines, as well as a smaller fuse for protection against voltage transients. The power connector, fuse, circuit breakers, bus connectors and the radial connectors are accessible from the rear of the unit.

PC board test points are standoff pins and are identified as TPA, TPB, etc., on both the PC board and its schematic.

2.1.4 POWER CONNECTIONS

CAUTION

Before connecting the unit to the power source, make certain fusing and the line voltage are correct. (See fuse label.)

2.2 OPERATION

Before operating the disk drive, make certain that the bus and radial interface connectors are properly attached. Note that connector pin numbers rise from RIGHT to LEFT.

2.2.1 MEDIA FLAW MAP

The 5380 is tested by writing and reading a specified amount of data, heat testing for 2 days, and then writing and reading again. During this testing, a flaw map of the media defects is generated. We are providing this flaw map with the drive only as a reference. As we use 65 sectors per track and use unique preambles and postambles, our map may not correlate with the map generated on your computer. The map will give you an idea of how many defects you can expect, however.

Note: The computer printout will give you the cylinder, head, and physical sector (CYL, HD, and PS) where the defect is located. The physical sector will not match yours unless you use the same sectoring that we do.

2.2.2 SECTOR SELECTION

When fixed length records will be written, the track can be divided into 1 to 256 sectors by using 16 switches located on 4 DIP switches, S1 through S4, on Busout type 5866 PC board. These switches preset a 16 bit counter which outputs a 1.25 usec SECTOR pulse each time the counter overflows.

The sector switches should be set to the binary value of the number of bytes per sector minus 1. Switch 1 of S4 outputs the least significant bit while switch 4 of S1 outputs the most significant bit. To calculate the required switch settings, divide the total number of available bytes per track (20,160) by the number of desired sectors (N), and subtract 1 from this value. Convert the result to binary numbers and set the switches accordingly. For example, if 32 sectors are desired apply the formula as follows:

$$\frac{20,160}{N} - 1 = \frac{20,160}{32} - 1 = 630 - 1 = 629$$

The number 629 is then converted to a binary value and switches S1 through S4 are set as shown in figure 2-2.

If variable length records are to be written, address marks rather than sectors should be used. An address mark is a 3 microsecond erasure within an all-zeros preamble made prior to the first record bit. When address marks are employed, the controller may disregard the DSECTOR signal from the disk drive. It is not relevant for address mark applications.

2.2.3 UNIT SELECT SWITCHES

These are S5-1 and S5-2 on the Busout board. (S54 should always be off; S5-3 is not used and can be ON or OFF.) The unit address assures that only one disk drive in a daisychain reacts to controller commands and returns status. Even in a single disk drive application, a unit address must be assigned. Here is a table showing the unit addresses and their respective switch positions:

S5-1	S5-2	Unit Selected
ON	ON	UNIT 0
ON	OFF	UNIT 1
OFF	ON	UNIT 2
OFF	OFF	UNIT 3

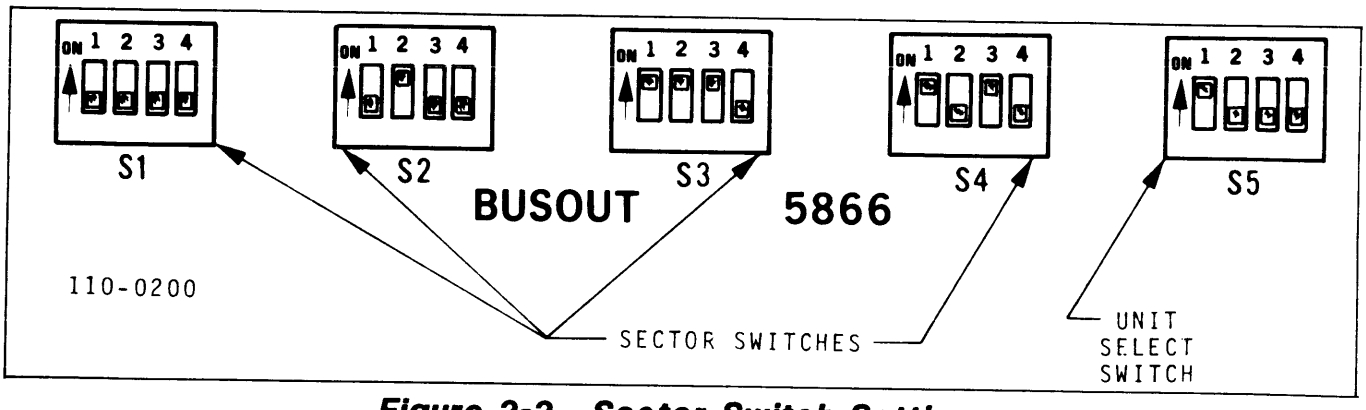


Figure 2-2. Sector Switch Settings

2.3 CONTROLS AND INDICATORS

2.3.1 FRONT PANEL

The Model 5380 front panel includes a spindle start/stop switch and four LED status indicators. Pressing the front panel switch once will initiate spindle spin up. Pressing the switch again will initiate spin down. The status indicators are:

SELECT When illuminated this LED indicates that the drive has been selected by the disk controller. The drive address is set by switch S-5 on the Busout PC board.

FAULT When illuminated this LED indicates the existence of a fault condition. The specific fault can be determined by checking the Fault PC board.

READY When illuminated this indicator shows that the drive is ready for data transfer operations.

START This indicator illuminates when the Start/Stop front panel pushbutton has been depressed, initiating spindle spin up.

2.3.2 MAINTENANCE SWITCH AND INDICATOR

The Fault PC board supplies the gating for several status signals based on disk speed, head selection, track selection, line voltage, etc. The printed circuit board also contains nine indicator lamps which light individually when a specific fault condition exists. These are:

(1) LIMIT - an attempted seek is made past cylinder 823_{10}.

(2) SERVO - loading operation in progress or an indication of a loading condition.

(3) TIMEOUT - selected track not found in 500 usec or less.

(4) UNLOADED - disk not loaded after a seek.

(5) HDSL (Head Select) - two heads are selected simultaneously.

(6) POWER - logic voltages are NOT within specifications.

(7) WRTFLT (Write Fault) - disk is inoperative in write mode after Write Gate is true.

(8) RDNR (Read Not Ready) - disk is inoperative in read mode after Read Gate is true.

(9) R/W - Read mode attempted while in Write mode or vice versa.

In addition, the Fault PC board contains a manual reset switch.

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

The Model 5380 disk drive is a data storage device capable of rapid data access and high density MFM (Modified Frequency Modulation) Write Compensated format recording. To accomplish this the unit contains the electronics required to:

a. Quickly and accurately locate data on the disk during read and write operations.

b. Convert read data from MFM to NRZI format and reverse the process when writing data.

c. Accurately synchronize data propagation to disk speed to assure a constant block length.

d. Process controller commands and disk drive status signals.

e. Detect system faults and disable the WRITE operation until the fault is cleared.

Figure 3-1 is a physical representation of the disk drive, showing the position arm, data heads, fixed disks and servo head for a three disk machine. Note that there is only one servo head located adjacent to the bottom surface of the lowest disk in the pack. The servo track produces the pulses required for converting write data from NRZI to MFM format, as well as a cylinder, track and sector location. Data storage is performed on the remaining five disk surfaces, which have inner and outer heads positioned over them. (Two heads are used for faster data access.) When the disk pack is up to speed (3000 rpm), the heads "fly" on a thin, 19 microinch air bearing.

It is important to understand the difference between cylinders and tracks. The term, cylinder, refers to a position arm location. There are 412 such locations, each corresponding to a phase reversal in the prerecorded servo track on the bottom disk surface. The term, track, refers to the location of the position arm's data heads over the disk surface when it is at a given cylinder location. Since there are two data heads per position arm, there are twice as many tracks as there are cylinders. Figure 3-2 illustrates the track layout. Tracks are in odd and even numbered bands corresponding to the sweep of each

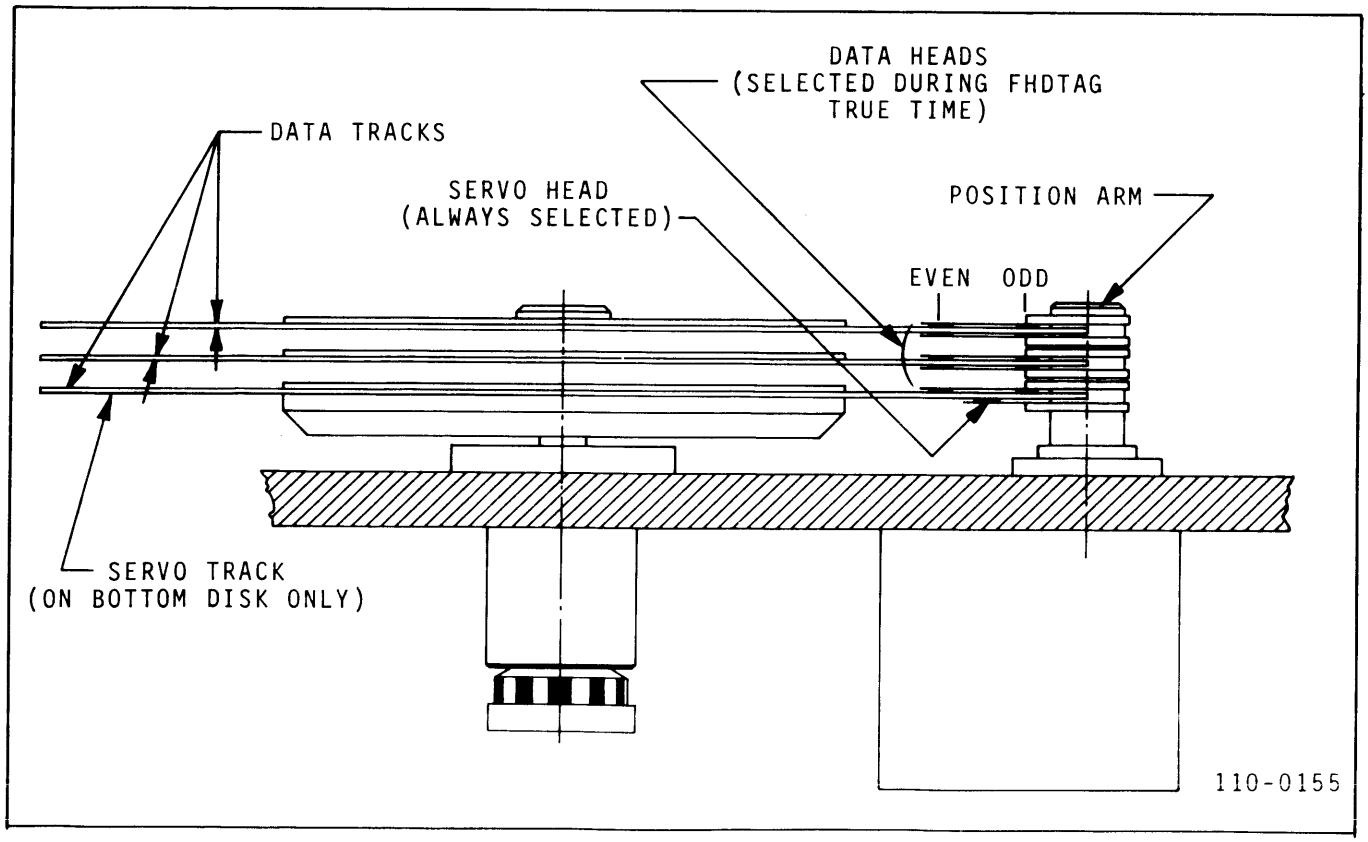


Figure 3-1. Side View, Model 5380 Disk Pack

data head. An odd or even numbered track may be selected, which is really done by selecting an odd or even numbered head. The disk surface to be accessed is determined by the head address. On a three disk machine there are ten data heads. Here is the typical addressing sequence: First, FCYLTAG/ is output from the controller to tell the disk drive that the bits on the F bus are a track address. A seek operation is initiated to locate the position arm over the selected cylinder and track. Next the controller outputs the head address on the F bus, along with FHDTAG/, to select the data head and thus indicate the disk surface to be accessed.

3.1.1 TRACK DIVISION

Depending upon application, each track is divided into either fixed length sectors or variable length records which are accessed by address marks.

Sectoring: (Refer to figure 3-2.) There may be as few as one or as many as 256 sectors assigned to a track. Sector length is user determined by the binary value on four selectable switches which load a counter on the Busout board.

When the sector counter overflows, it outputs a 1.25 microseconds SECTOR pulse to the controller, indicating the beginning of a new sector. Obviously, the higher the binary value of the sector switch setting the greater the number of sector pulses and sectors per revolution. Incidentally, since the servo head is always selected, sector pulses are constantly being output to the controller, even while the arm is in motion.

Address marks: These are especially suited to variable length recording requirements. The controller outputs an all zeros preamble containing a three byte erasure prior to the first data bit. During a read operation, this 3 microsecond erasure is detected by circuitry on the Busout board and ADDRESS MARK FOUND (DAMFND/) is returned to the controller.

3.2 SEEK OPERATION

The positioning of the arm is performed by circuitry on the Seek Control and Servo Boards. As we stated earlier, one of 823 tracks can be selected. The cylinder address is input on controller lines FBUS0 through FBUS9 during FCYLTAG/ true time. (FHDTAG/ true in conjunction with FBUS0-FBUS2 would initiate head selection; FCMDTAG/ true in conjunction with one or more true F bus lines is interpreted as a command.)

The track address is applied to the Seek Control board and compared with the current track address. The absolute difference between old and new track addresses is converted into an analog voltage RAMP signal. This ramp voltage is directed to the Servo board and combined with VELOCITY signal output from the position arm stator and other signals to develop an ANALOG OUTPUT voltage for controlling the position arm. Naturally, this servo requires

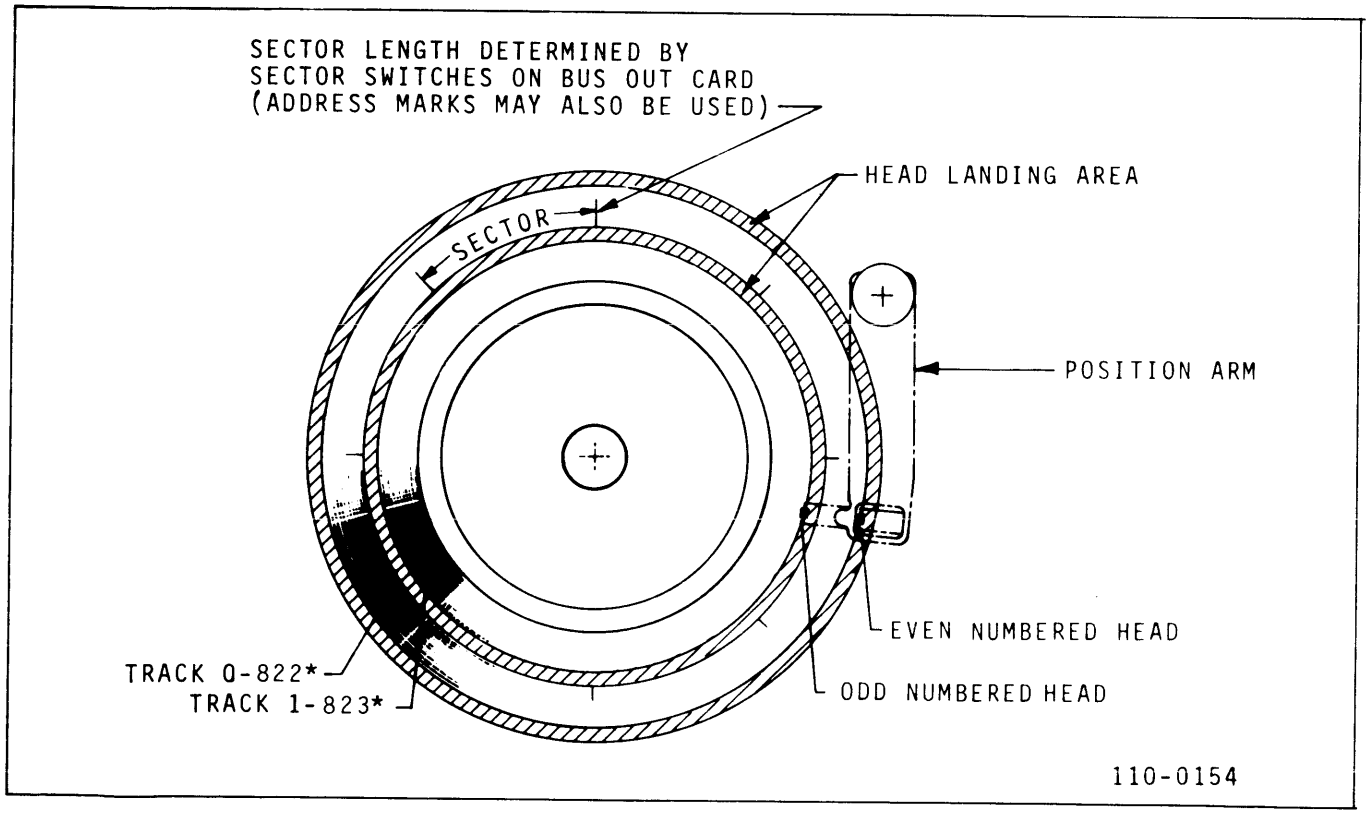


Figure 3-2. Data Surface Layout

feedback to determine when the selected head is over the selected cylinder track. So, as the servo head on the bottom disk surface crosses servo tracks of opposing polarity — the next track pair, or cylinder, is on the opposite disk surface — a cylinder pulse (CYL PULSE/) is generated. This decrements the counter on the Seek Control board, which in turn outputs a smaller binary value to the digital-to-analog converter producing the RAMP signal. As the position arm nears the selected track, the ramp voltage decreases in steps, and the arm slows down. When the counter is decremented to zero, the position arm will stop over the track selected.

How is the data head kept on track? This is accomplished by the servo tracks, servo head and the Servo board circuitry. Figure 3-3 illustrates the waveforms developed from the servo tracks. Alternating servo tracks produce waveforms of opposite polarity. When the position arm is locked on cylinder, the servo head is precisely centered on the boundary between two servo tracks. The composite waveform developed by the TRACK FOUND circuitry on the Servo board exhibits two positive pulses of equal amplitude for each two data bytes. If the servo head drifts off track, these pulses become unequal in amplitude and the servo will issue a corrective voltage to recenter the servo head and thus recenter the data heads.

3.2.1 HEAD AND TRACK SELECTION

In figure 3-1 there are ten data heads, numbered 0 through 9, and one servo head. The servo head is always selected and operational. Head selection is performed during HDSELTAG true time, when FBUS0/ through FBUS2/ from the controller are input to the head register on the fault logic card. This register outputs HDSEL1-HDSEL8. HDSEL1 is the least significant bit; HDSEL8 is the most significant bit. These lines are input to a binary to BCD decoder on the Preamplifier board. One of the decoder's ten output lines will go low true, selecting one of the data heads.

3.3 WRITE OPERATION

After the data head is selected and on track, on cylinder (DONCYL/) true status signal is returned to the controller. Now, the controller can issue write enable (WRTENB/) true as well as a command tag (FCMDTAG/) and FBUS0/ true to initiate a write operation. To synchronize write data to disk speed so that the proper write density will be maintained, an 8 MHz DSRVCLK signal derived from the servo track information is output to the controller. This signal is used to clock write data into the Radial board as well as to generate the write clock (FWCLK).

3.3.1 NRZI-MFM WRITE DATA CONVERSION

NRZI write data from the controller is converted to write compensated MFM data by the Radial board; then amplified and serially applied to the selected data head by the Read/Write Amplifier PC board. Figure 3-4 illustrates a typical write data pattern.

Unlike NRZI formatted data, MFM formatted zeroes and ones are detected by their location within the bit

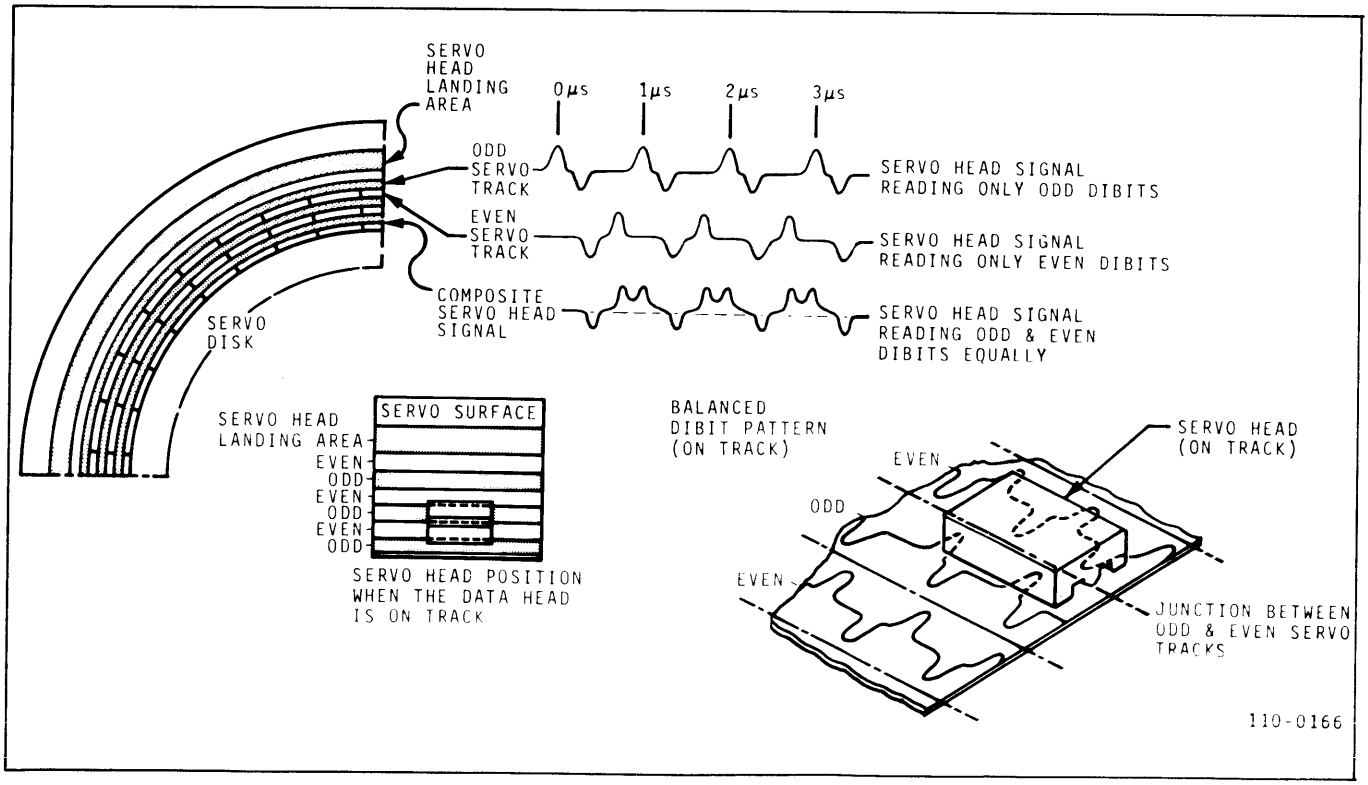


Figure 3-3. Servo Track Operation

cell. (A bit cell is a single positive and negative excursion of the write clock.) Normally zero bits are written at the start of the bit cell, while one bits are written in the center of the bit cell.

In addition, certain bit patterns require that the bits be shifted early or late within the data cell to prevent bit crowding. This is known as write compensation. Write compensation is required for MFM format because, without it, the extremely high bit density (6400 bpi on the average) would result in bit crowding and possible lost data.

On the Radial board, write compensation and zero/one bit detection is performed by a programmable read only memory (PROM). The PROM looks at five bits at a time, and determines whether the middle bit is a zero or a one, as well as any write compensation required. The resultant ZERO, ONE, EARLY or LATE signals are converted to ECL to develop the extremely accurate MFM data transitions.

The differential WTOG+ and WTOG- output from the Radial board are complementary transitions. These write transitions are amplified by the Read/Write Amplifier PC board and applied to the selected data head, provided the controller is issuing a write enable command.

Circuitry on the Read/Write board will detect the absence of write current (WRTCURSNS/ false) or write data transitions (WTRANS/ false). Either condition would cause WRITE FAULT/ true status signal to be returned to the controller from the Fault PC board.

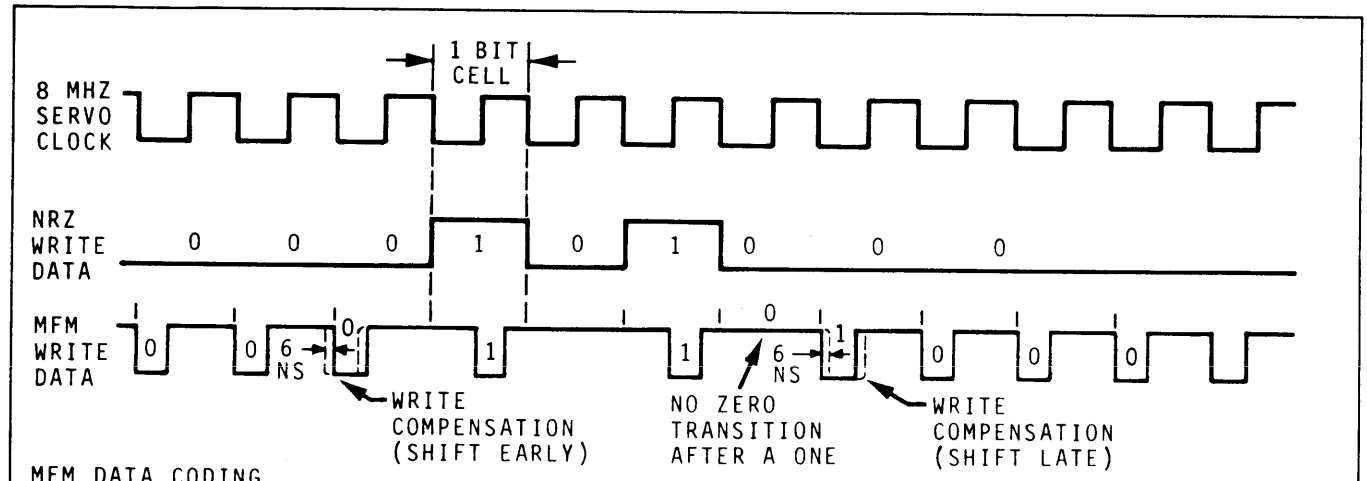
3.4 READ OPERATION

Read operations are handled by the Read/Write Amplifier, Read/Data Separator, PLO board and the Radial board. First, the controller outputs a command tag and FBUS1/ true. These signals are combined on the Busin card to develop READ true.

This signal enables read data to be output from the Read/Data Separator in the form of TRANSITION pulses and the ENABLE level. At this point the read data is still in MFM format. It is converted to NRZI TTL format on the Phase Locked Oscillator board, which also develops the NRZI read clock. These signals are output to the controller through the Radial board.

3.5 DISK DRIVE COMMANDS

The Busin board processes the command lines which are input from the controller on the bus cable. Command signals include: cylinder tag (FGYLTAG/),



MFM DATA CODING

A. A "1" BIT IS DEFINED BY THE LEADING EDGE OF THE PULSE OCCURRING AT THE MIDDLE OF THE BIT CELL.

B. A "0" BIT IS DEFINED BY THE LEADING EDGE OF THE PULSE OCCURRING AT THE START OF A CELL TIME EXCEPT THE PULSE IS OMITTED FOR THE FIRST "0" FOLLOWING A "1" BIT.

MFM WRITE COMPENSATION X011, XX10, 1000 and X001 ARE WRITE COMPENSATED AS FOLLOWS:

RULE	DATA PATTERN	COMPENSATION
1	1000	DELAY SECOND ZERO 6 ±1 NS
2	X001	ADVANCE SECOND ZERO 6 ±1 NS
3	XX10	ADVANCE THE ONE 6 ±1 NS
4	X011	DELAY THE FIRST ONE 6 ±1 NS

110-0167

Figure 3-4. MFM Recording

head tag (FHDTAG), the command tag (FCMDTAG) and FBUS lines 0-9, write enable (WRTENB), as well as the unit select lines (FSEL0/, FSEL1/, FSELTAG/).

The UNIT SELECT switches on the Busout card are set by the user to the desired disk drive address. These switches are connected to the unit address comparator, which compares the binary address on UNIT SEL0 and UNIT SEL1 with the switch selected address. If there is a match and the UNIT SELECT TAG is true, a SELECTED/ true level will be output to the Busin card to enable the next command from the controller.

As stated earlier, commands FCYLTAG, FHDTAG and FCMDTAG determine the function of the bits on controller lines FBUS0 through FBUS9. Thus, 10 FBUS bits determine the cylinder address during FCYLTAG time, three bits determine head address during FHDTAG time and one bit determines read, write or other commanded operations during FCMDTAG time.

3.6 FAULT DETECTION

This is accomplished by the logic on the Fault board. The three basic fault signals output to the controller are: DFAULT/, DONCYL/ and DSKERR. DFAULT/ goes true due to insufficient write current, lack of write transitions or simultaneous selection of more than one head. DONCYL/ goes false when the cylinder address exceeds 822, when a RESTORE operation is occurring, or when TRACK END signal is false. DSKERR/ goes true when the unit is unloading or in time out mode.

Unloading occurs if the phase locked oscillator on the Servo board unlocks or ON TRK signal goes false after DELAYED LOCKED true signal has been issued. Under these conditions, the position arm retracts to a guard band and head landing area near the center of the disk. Time Out (TOUT/) true would also activate DSKERR. TOUT/ goes true if 500 msec have elapsed since a SEEK command and the unit is still not on track.

SECTION IV

MAINTENANCE INSTRUCTIONS

4.1 PREVENTIVE MAINTENANCE

Even under optimum conditions, a simple preventive maintenance program should be followed regularly. It consists of daily connector checks, monthly makeup filter replacement and drive belt checks.

VISUAL INSPECTION – PERFORM DAILY

Check radial cable, bus cable and ac power cord for proper connection and signs of wear. All cables should be long enough to provide slack.

4.2 FILTER MAINTENANCE

Cleanliness is crucial to trouble-free disk drive operation, since the heads literally float on a minute, 19 microinch air bearing created by the rapidly spinning disk surface. This dimension is dwarfed by the thickness of a human hair or even the size of the average dust particle.

To assure cleanliness, the disk(s) and heads are assembled in a cleanroom environment, then factory sealed. To maintain this level of cleanliness, the Model 5380 incorporates an air filtration system capable of filtering out particulate matter larger than 0.3 micron. This is 99.9% effective. The system consists of:

a. A pressure pump powered by the disk drive motor which pressurizes the disk chamber.

b. An air recirculation filter which cleans the pump's output air, then returns the filtered air to the disk chamber under pressure.

c. A makeup, or intake, filter for cleaning ambient air used for disk chamber replenishment.

Since the makeup filter is exposed to relatively contaminated air outside the system, it must be replaced at least twice a year, or more frequently in a less than optimum environment.

The recirculation filter rarely requires replacement. However, it should be checked and replaced as required.

4.2.1 MAKEUP FILTER REPLACEMENT
(Yearly replacement, minimum)

Equipment required:

Makeup Filter, Kennedy PN 126-0020-001

Procedure:

a. Disconnect the power cord or set the circuit breaker to TRIP position.

b. Turn disk drive on its side to gain access to the makeup filter located on chassis underside.

c. Unsnap the makeup filter (this filter is connected to only one tube, as shown in figure 4-1) from its retaining plate and disconnect the tube from the filter. Do not disconnect the tube from the deck.

d. Check the intake side of the makeup filter for signs of dirt. If it is dirty, the makeup filter must be replaced even more frequently.

e. Immediately install a new makeup filter, Kennedy PN 126-0020-001.

4.2.2 DRIVE BELT CHECK
(Perform during makeup filter replacement)

Equipment required:

1 Disk Drive Belt, Kennedy PN 135-0064-001.

Procedure:

a. Set circuit breaker switch to TRIP position.

b. Belt is located on underside of chassis. Check it for cracks, fraying or excess slack. (Belt tension adjustments should be made only by a qualified service technician.) Replace as required.

4.3 CONTAMINATION AND HDI

HDI stands for head to disk interference, a direct result of dirt contamination on disk and head surfaces. Frequent makeup filter replacements will minimize the HDI problem, but one should be aware of its symptoms.

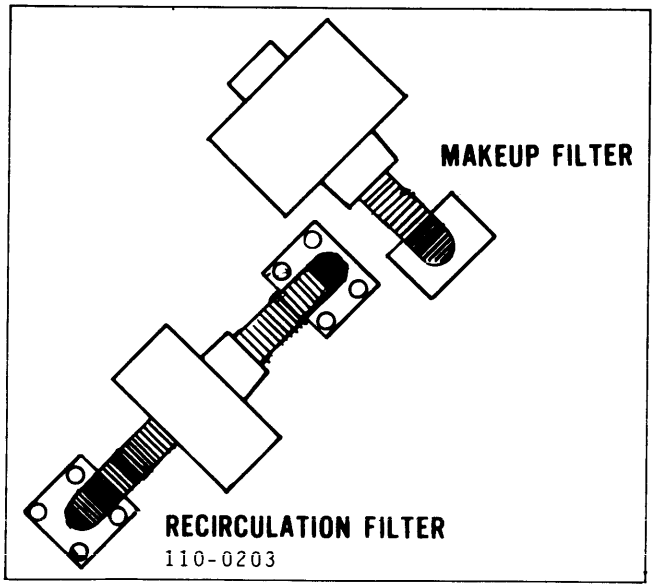


Figure 4-1. Filter Identification

HDI varies in severity from an instantaneous head/disk contact resulting in slight oxide traces on the head and superficial disk damage to constant head/disk contact causing total head and disk destruction.

The first symptom of dirt buildup is difficulty in recovering data, with several read retries required. (Note that data recovery problems may be related to other troubles, however.)

As contamination progresses, data recovery becomes impossible. At this point, head and disk cleaning becomes mandatory. This is a job for a qualified service technician.

If contamination is allowed to continue, a head crash becomes inevitable, scoring the disk(s), obliterating the recorded data and ruining the head(s).

4.4 HDI PROPAGATION

This is a post-head crash problem. HDI can be propagated, unless both the damaged head and disk are replaced at the same time. Otherwise, the part replaced may be damaged by the defective unreplaced part due to the finite head-to-disk gap.

SECTION VI

SCHEMATICS

This section contains the circuit schematics for the individual circuit cards used in the disk drive. The schematics are arranged by functional groups as shown below. Electronic symbols used in the drawings conform to MIL-STD-12 unless otherwise specified.

Functional Group	Module Name and Type
Overall	Notes to Schematics Motherboard Power Regulator PC Board Power Supply PC Board
Control	Storage Module Adapter PC Board Pushbutton Control PC Board Busin SMD PC Board Seek Control SMD PC Board Busout PC Board Fault Logic PC Board
Servo System	Velocity Preamplifier PC Board Servo PC Board Servo Power Amplifier PC Board
Read/Write Electronics	Read/Write Amplifier PC Board Data Detector PC Board PLO PC Board Radial PC Board

NOTES TO SCHEMATICS

Certain conventions have been observed in preparing schematics for this manual.

1. Resistor values are given in ohms. If wattage is unspecified the resistor may be either $\frac{1}{4}$ or $\frac{1}{2}$ watt.

2. Capacitor values may be given in picofarads or microfarads. Those values for which neither designation is provided are assumed to be obvious from circuit function. Filter capacitors on certain supply lines do not have logic significance. In general, they are not shown on schematics. On PC board silkscreens they are designated as CF.

3. Normally, IC power connections are on pins 14 (+5v) and 7 (ground) for 14 pin packages, and 16 (+5v) and 8 (ground) for 16 pin packages. Some ICs — 7476, 7492, 7493 for example — have power connections on pin 5 (+5v) and pin 10 (ground). Operational amplifiers in the 8 pin package have power connections on pin 4 (-Vcc) and pin 7 (+Vcc). Power connections are not shown unless they are nonstandard.

4. Where multiple inputs are tied together only one pin may be designated on the schematic.

5. Unused inputs that are tied high are not normally indicated unless the connection has logic significance.

6. From and to designations are intended to describe inputs and outputs only. The same signal may be connected to several other points not shown on a particular drawing.

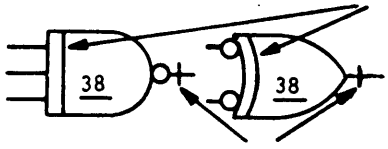
7. Positive logic is shown for all internal connections. Interface connections are zero true but the bar is omitted.

8. Integrated circuit symbols contain a circuit designator that corresponds to the number silkscreened onto the circuit module above an underlined number representing the IC type.

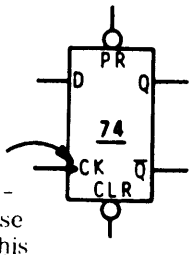
   The IC type number is abbreviated and omits the portions of the manufacturer's type number pertaining to case and vendor identification. Further, since the TTL 7400 series makes up most of the circuitry, the 74 is omitted on these. Thus a 00 designation indicates a 7400 quad two input NAND gate. T.I.'s complete part number is SN7400N. In multifunctional units in close proximity to each other the type designation may be omitted. The type designation may appear outside the symbol if the symbol is too small.

   Military Standard 806C is the base for logic symbols. Additional conventions are shown below.

   Line indicates buffer or power driver



   Line indicates open collector

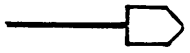


   Triangle indicates response to edge (in this case positive)

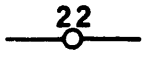
9. Semiconductor types on schematics may be replaced by their functional equivalents. If not indicated, diodes are 1N914, NPN transistors are 2N2714, and PNP transistors are MPS6517.

10. Unless otherwise specified, light emitting diodes are FLV102 or equivalent.

11. Module connector pins are shown as



    where no further connections is shown on the schematic, and as



    when there is a connection shown.

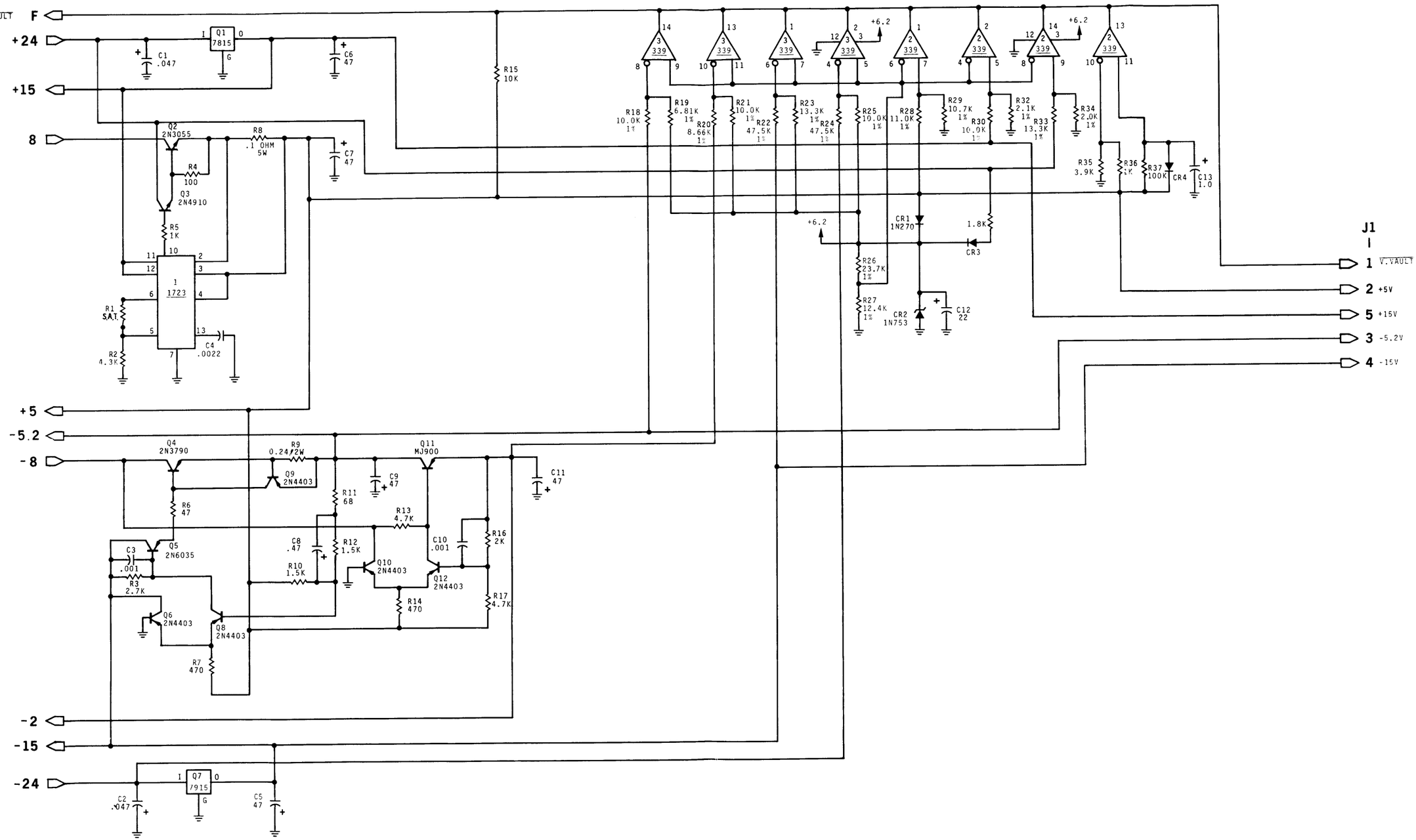
12. Where an input is represented by an arrow instead of a complete line, the input source is designated. Where outputs are so shown their destinations may not be shown.

13. Some schematics of modules include certain external elements which aid in understanding the circuit function. In this case all the connections to the element may not be shown in the interest of clarity.

14. 

designates a test point provided on the module. Letters proceed from top to bottom of card with the ground test point, if present, as the bottommost terminal.

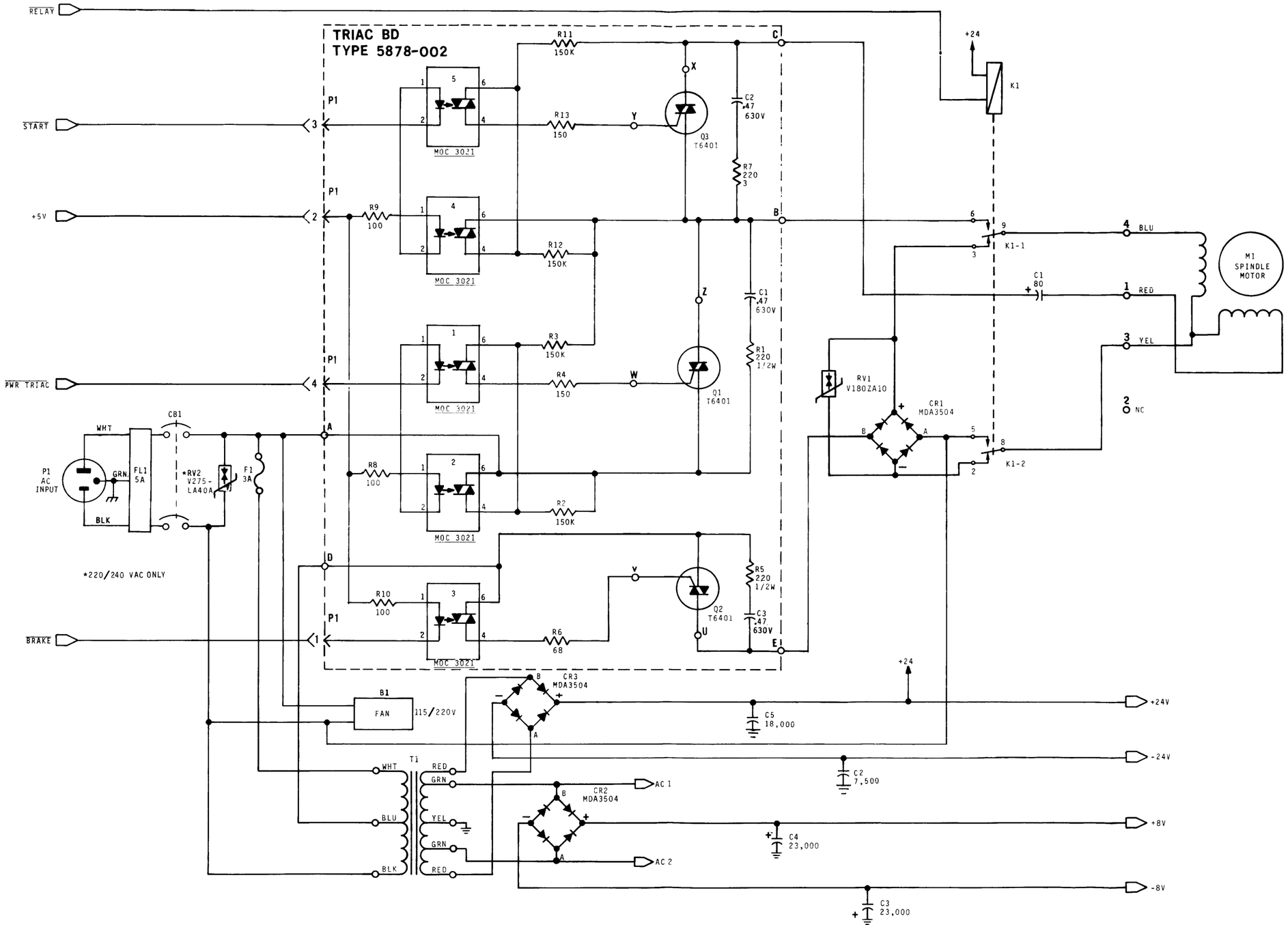
15. Socket terminals are designated with numbers for component side connections and letters for circuit side connections when a double sided socket is used. These are the designations on the socket. When a single sided socket is provided, all connections are designated by letters regardless of which side of the board they lie on the etch. Letters follow the 22 pin alphabet, ABCDEFHJKLMNPRSTUVWXYZ; numbers are 1 through 22.



NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Power Regulator
Type 5882-001
Schematic Diagram

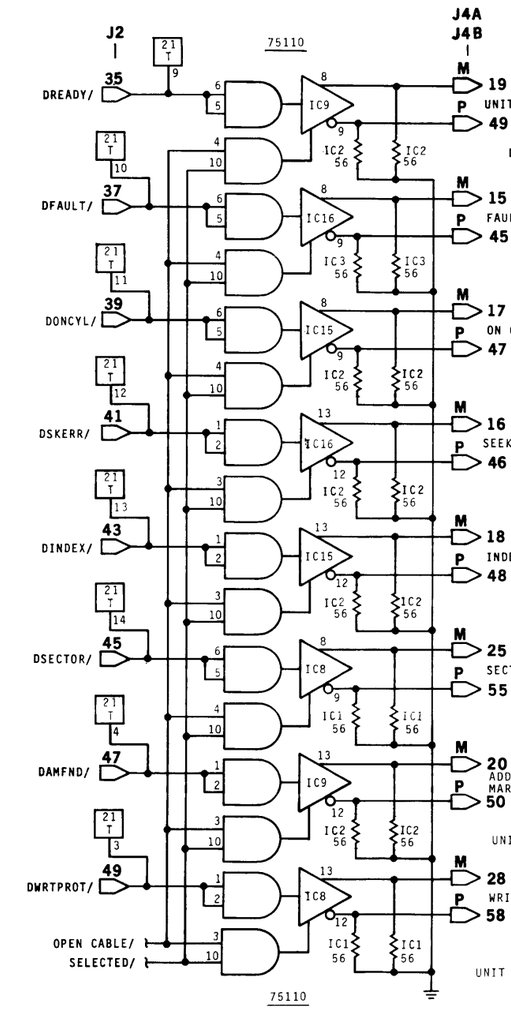
401-5300-001 C

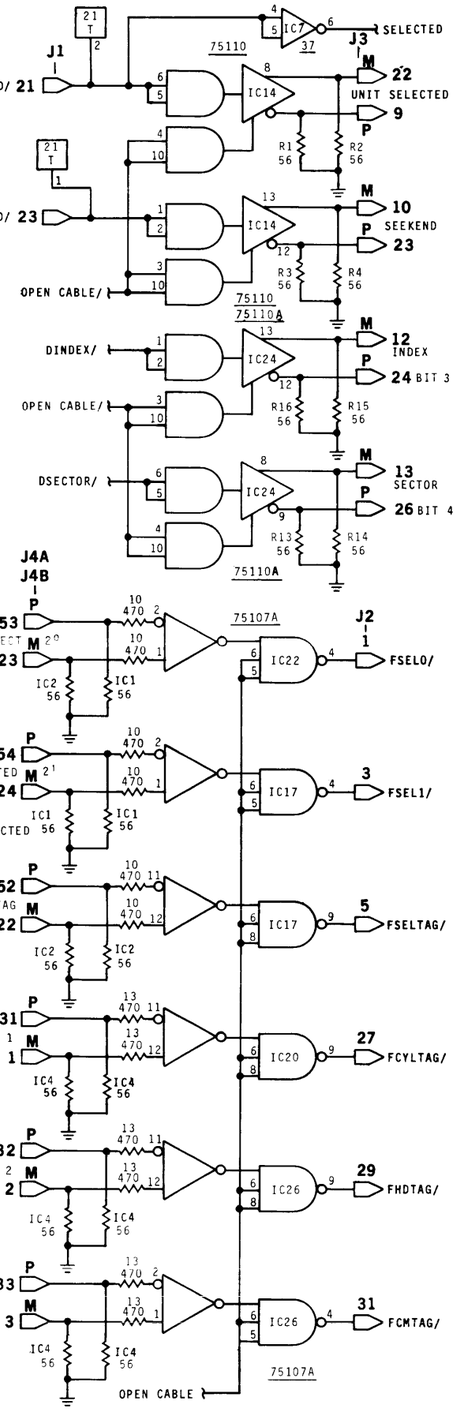


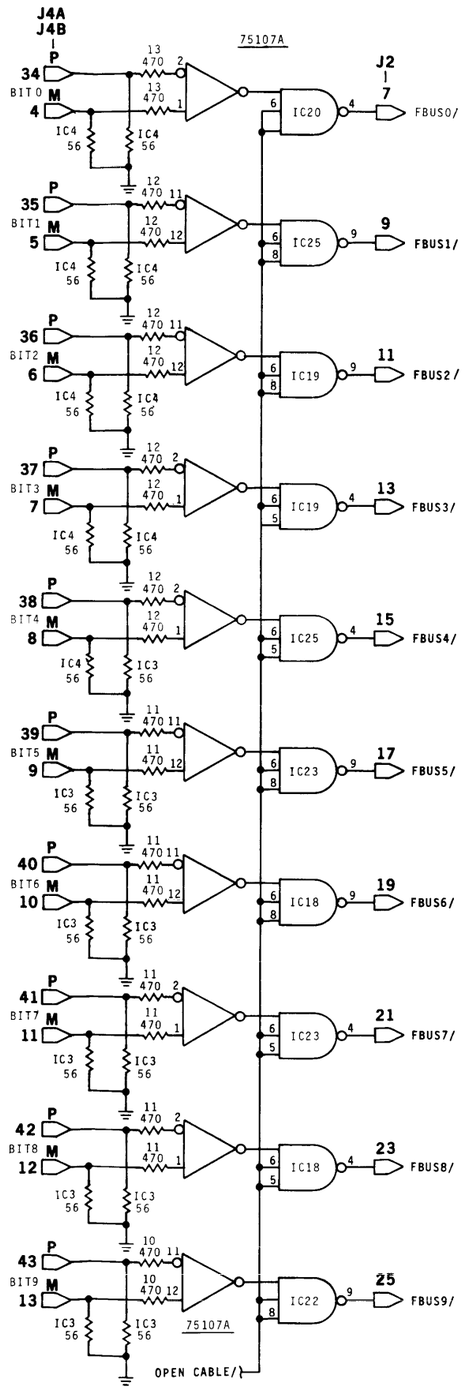
Model 5300 Power Supply, Schematic Diagram

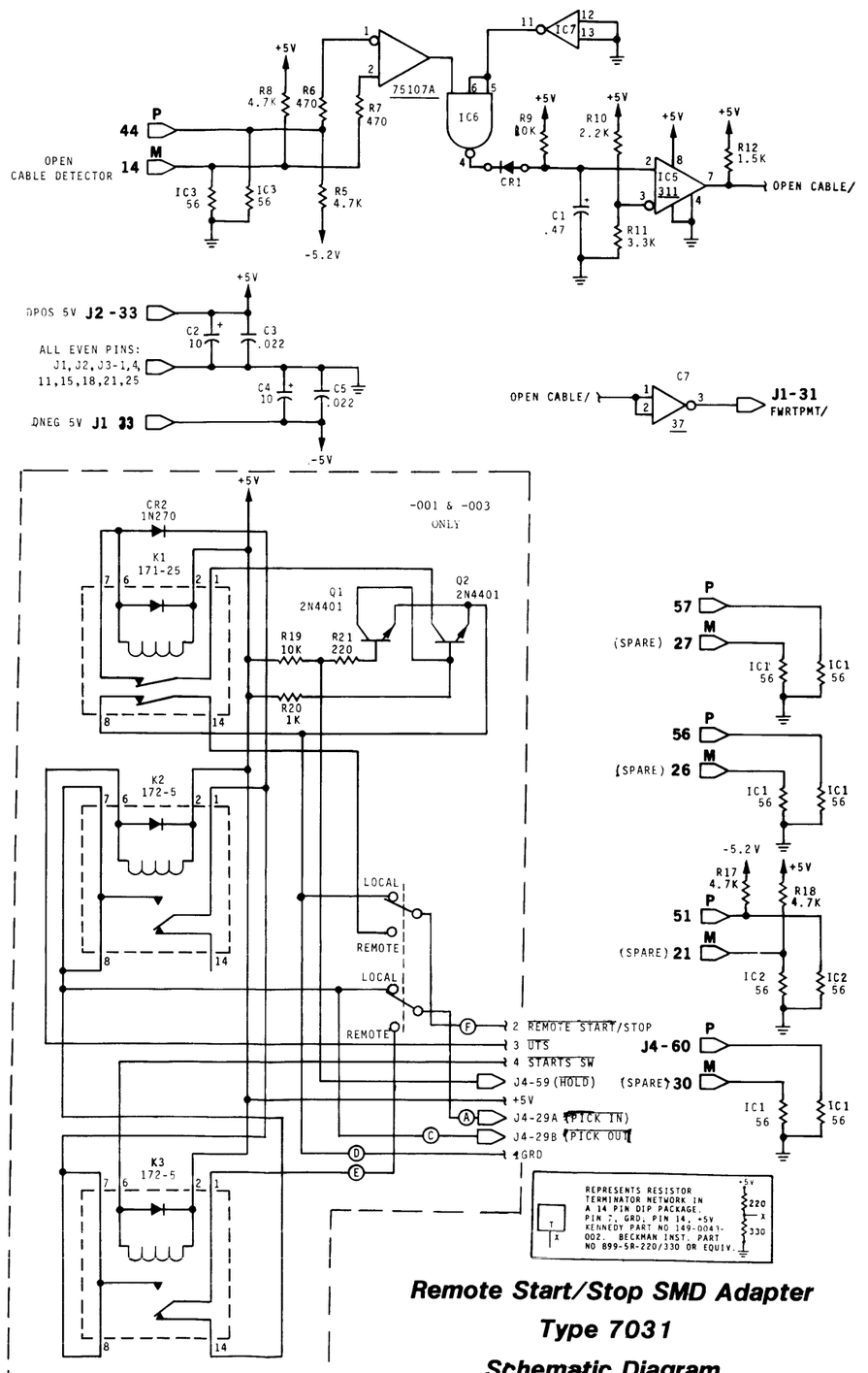
NOTES:
1. ALL NON-DISCRETE RESISTORS ARE CALLED OUT BY THE RESISTOR NETWORK IC DESIGNATORS OF WHICH THEY ARE PART.

401-7031-001 D









WRITE DATA	J3-20	J1-1	FWDATP
	J3-8	J1-3	FWDATN
WRITE CLOCK	J3-19	J1-5	FWCLKP
	J3-6	J1-7	FWCLKN
DSRVCLKP J1-9		J3-14	SERVO CLOCK
DSRVCLKN J1-11		J3-2	
DRDATP J1-13		J3-16	READ DATA
DRDATN J1-15		J3-3	
DRCLKP J1-17		J3-17	READ CLOCK
DRCLKN J1-19		J3-5	

Remote Start/Stop SMD Adapter Type 7031 Schematic Diagram

401-5868-003 B

TABULATION BLOCK				
DASH NO.	ST 1	ST 2	ST 3	C16
003	OMIT	OMIT	STRAP	22
004	STRAP	STRAP	OMIT	22
005	OMIT	OMIT	STRAP	10

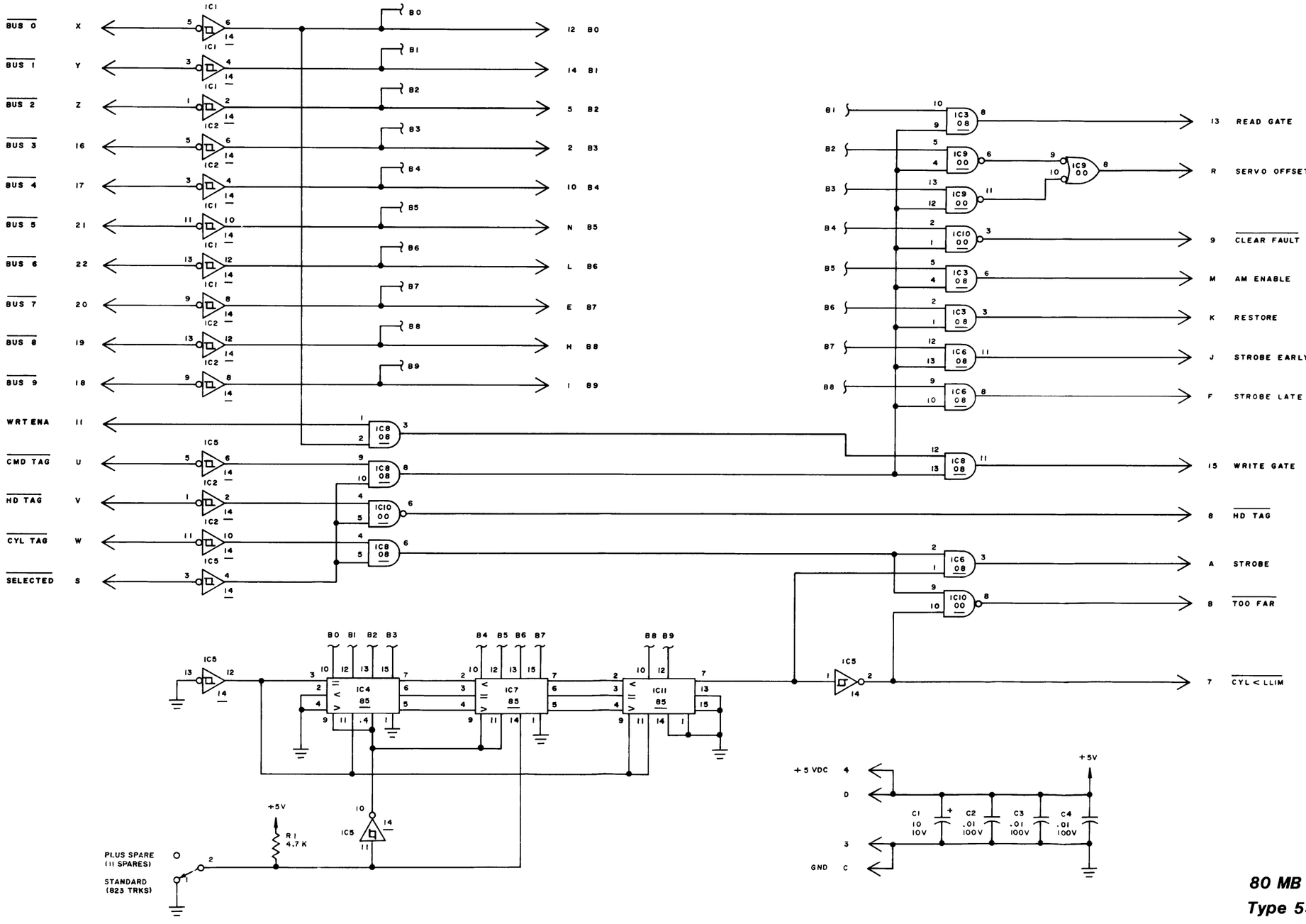
REF DESIGNATOR	
LAST USED	NOT USED
R61	
C17	C1
Q3	
IC14	
CR10	
TP6	
P4	

Pushbutton Control
Type 5868
Schematic Diagram

NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE 1/4 W, ±5%, VALUE IN OHMS.
2. CAPACITANCE IN MICROFARADS.

401-5379-001 B



80 MB Busin
Type 5379A
Schematic Diagram

401-6879-001D1

B9 P
B8 R
B7 S
B6 T
B5 U
B4 V
B3 W
B2 X
B1 Y
STROBE 12
RESTORE 5
RESTRT N
+5V 4
GRD 3
-15V A
+15V B

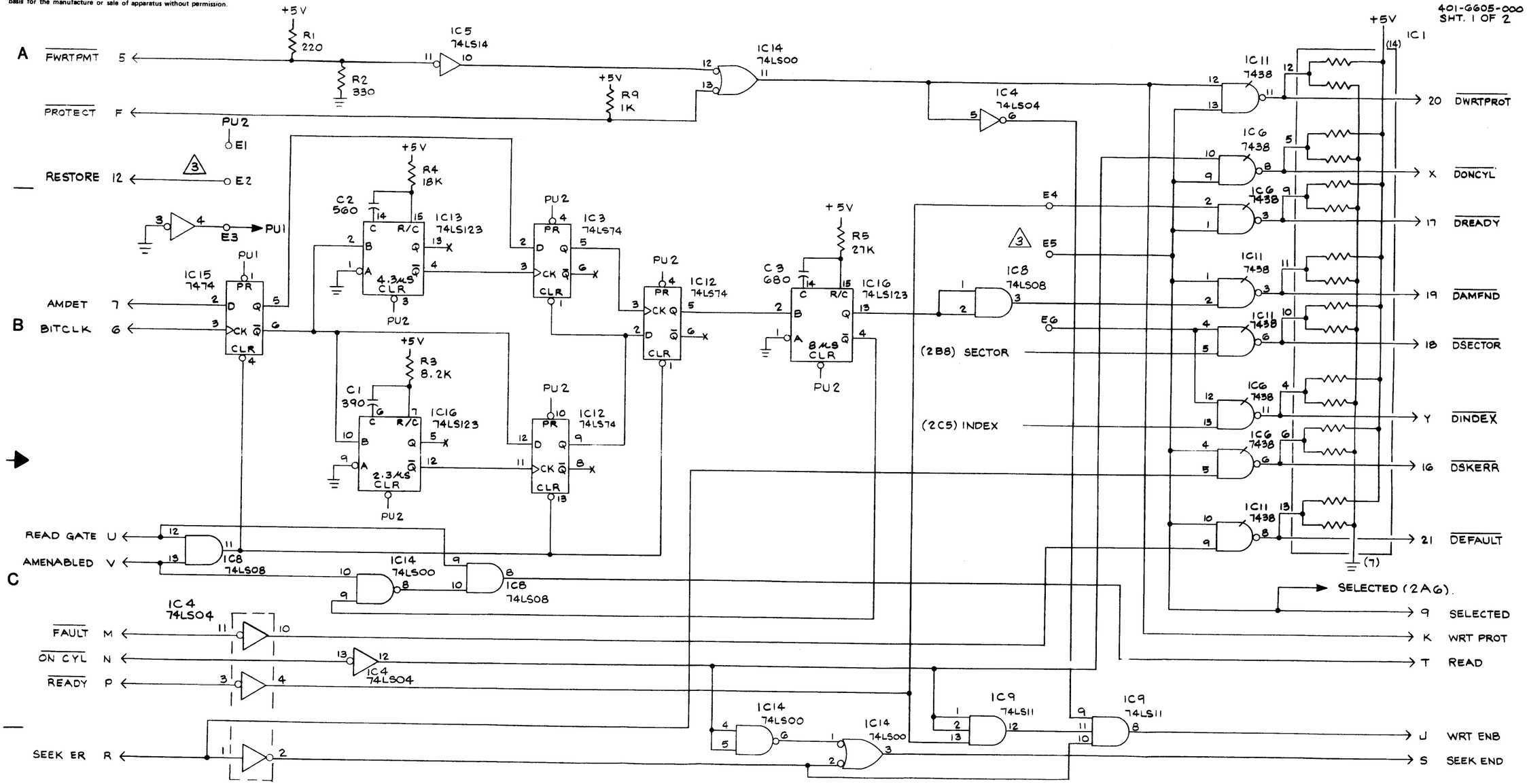
M SEEK/ LOCK
F RAMP
J CYL PULSE
K ON TRACKS
22 FWD/ REV
7 UTS/ RETRACT
H LIMIT
21 EVEN/ ODD

RSTRNG

NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

Seek Control (SMD), Type 6879-001,D Schematic Diagram

401-G605-000
SHT. 1 OF 2



DASH NO.	DESCRIPT.	S1, S2, S3, S4	E1 TO		E6 TO		R30,31	IC 1
			E2	E3	E5	E4	32,33	
-001	5866-001	INSTALL	—	STRAP	STRAP	—	—	—
-002	-002	INSTALL	—	STRAP	STRAP	—	—	220/330
-003	-003	INSTALL	—	STRAP	STRAP	—	—	1K/1.5K
-101	-101		—	STRAP	STRAP	—	3.3Ω	—
-102	-102		—	STRAP	STRAP	—	3.3Ω	220/330
-103	-103	—	—	STRAP	STRAP	—	3.3Ω	1K/1.5K
-004	-004	INSTALL	—	STRAP	—	STRAP	—	—
-005	—	INSTALL	STRAP	—	—	STRAP	—	—

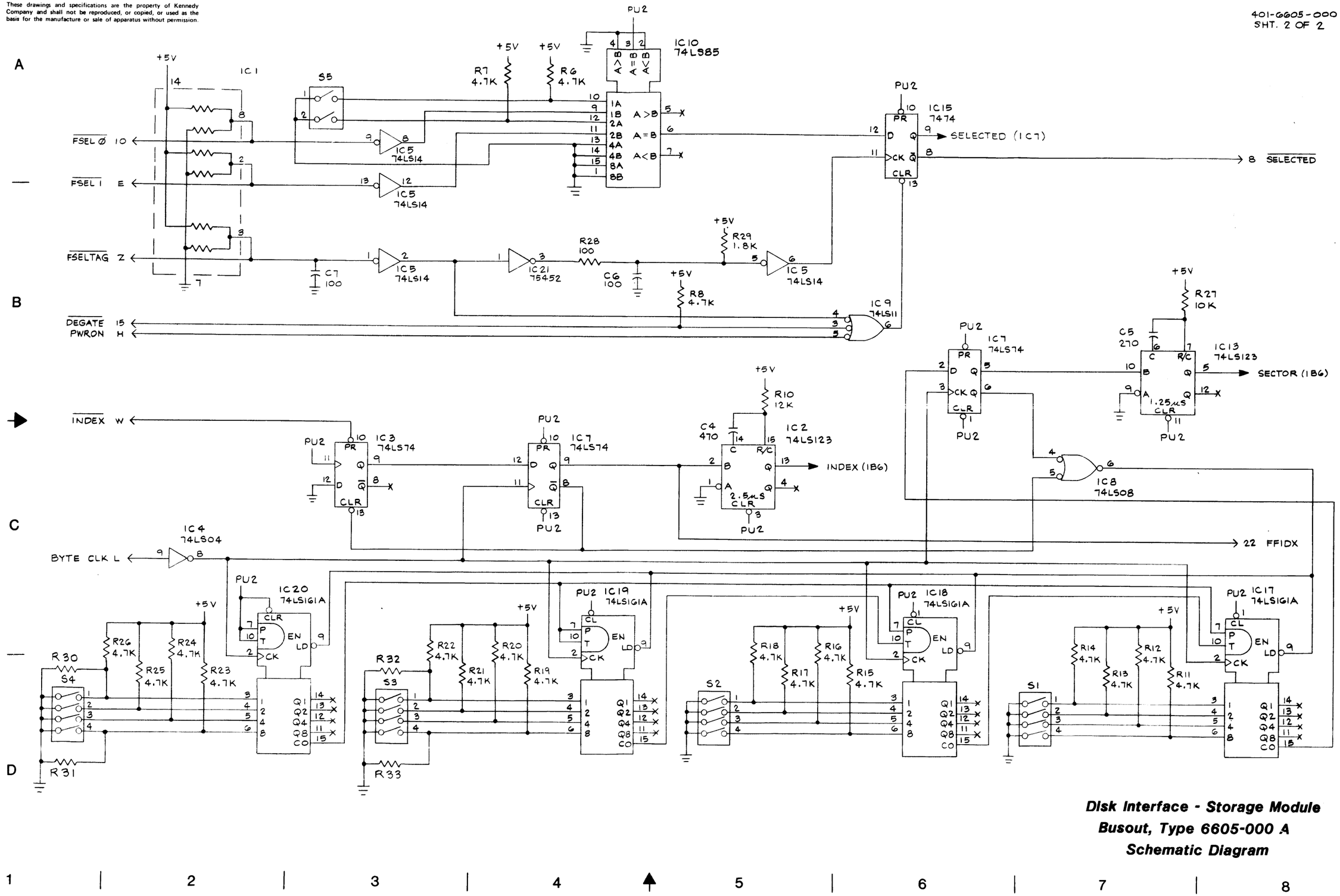
REF. DES	TYPE	+5V	GND
IC 1	220/330	14	7
IC 2,13,16	74LS123	16	8
IC 3, 7, 12	74LS74	14	7
IC 4	74LS04	14	7
IC 5	74LS14	14	7
IC 6, 11	7438	14	7
IC 8	74LS08	14	7
IC 9	74LS11	14	7
IC 10	74LS85	16	8
IC 14	74LS00	14	7
IC 15	7474	14	7
IC 17-20	74LS161A	16	8
IC 21	75452B	8	4

REF. DES.	
LAST USED	NOT USED
C 11	
R 29	
IC 21	

4. X INDICATES NO CONNECTION.
3. INSTALL JUMPERS PER CHART.
2. ALL CAPACITOR VALUES ARE IN MICROFARADS
1. ALL RESISTOR VALUES ARE IN OHMS ± 5%, ¼WATT.

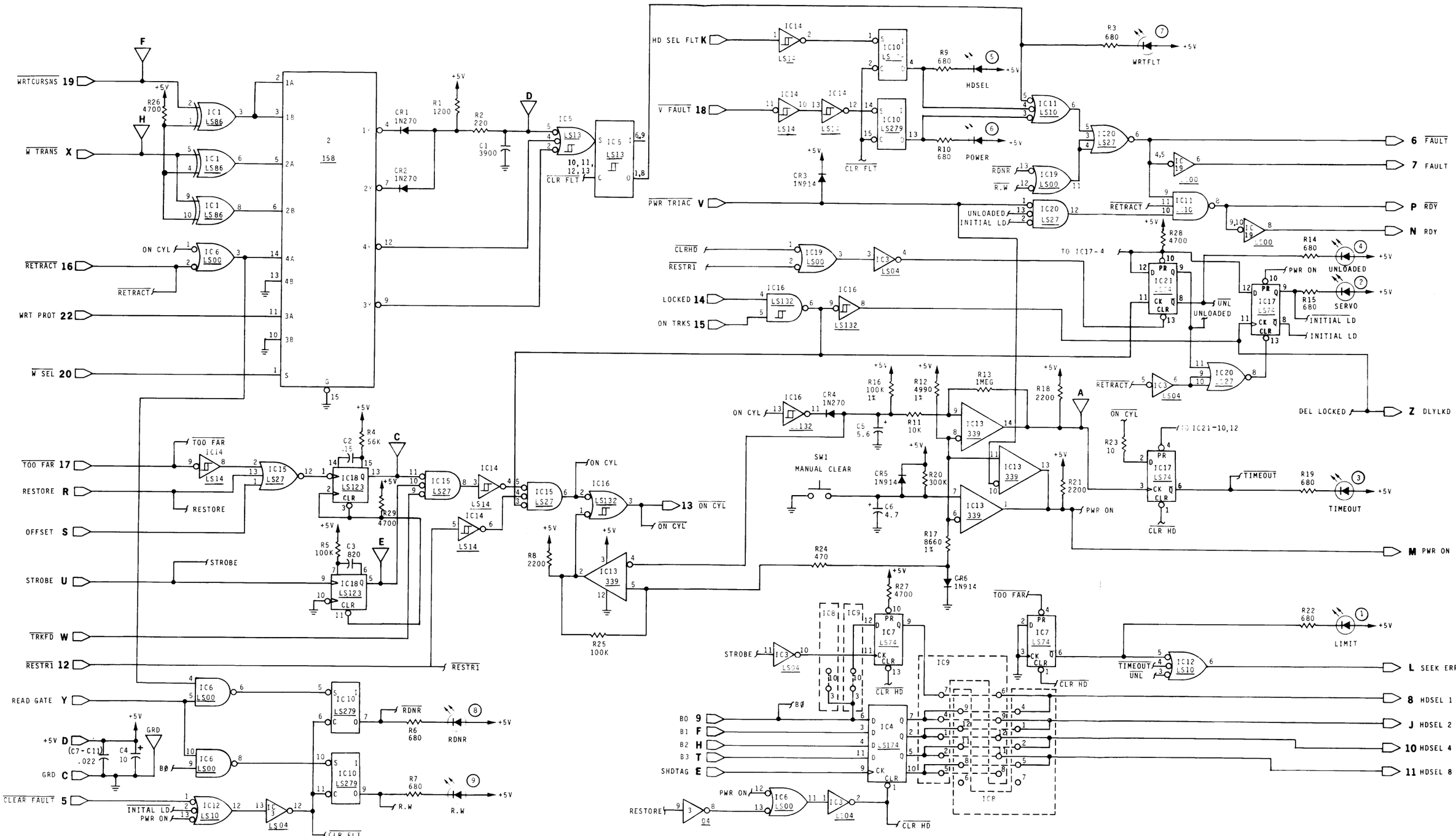
NOTES: UNLESS OTHERWISE SPECIFIED

Disk Interface-Storage Module, Busout, Type 6605-000 A Schematic Diagram



Disk Interface - Storage Module
Busout, Type 6605-000 A
Schematic Diagram

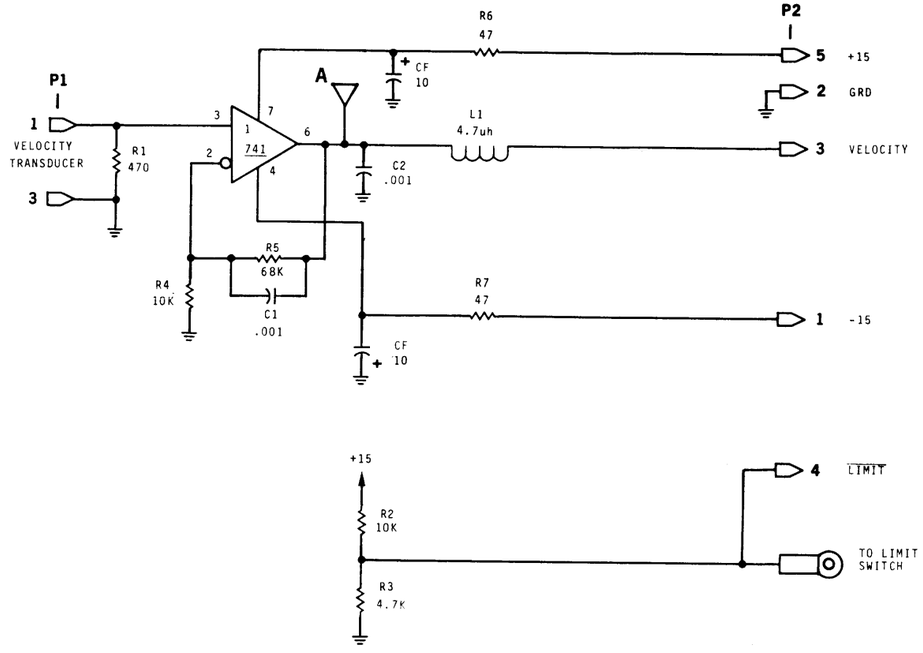
401-7967-003A



INDICATOR NO.	1	2	3	4	5	6	7	8	9
FAULT	LIM	SERVO	TIMEOUT	UNLOADED	HDSEL	POWER	WRTFLT	RDNR	R.W

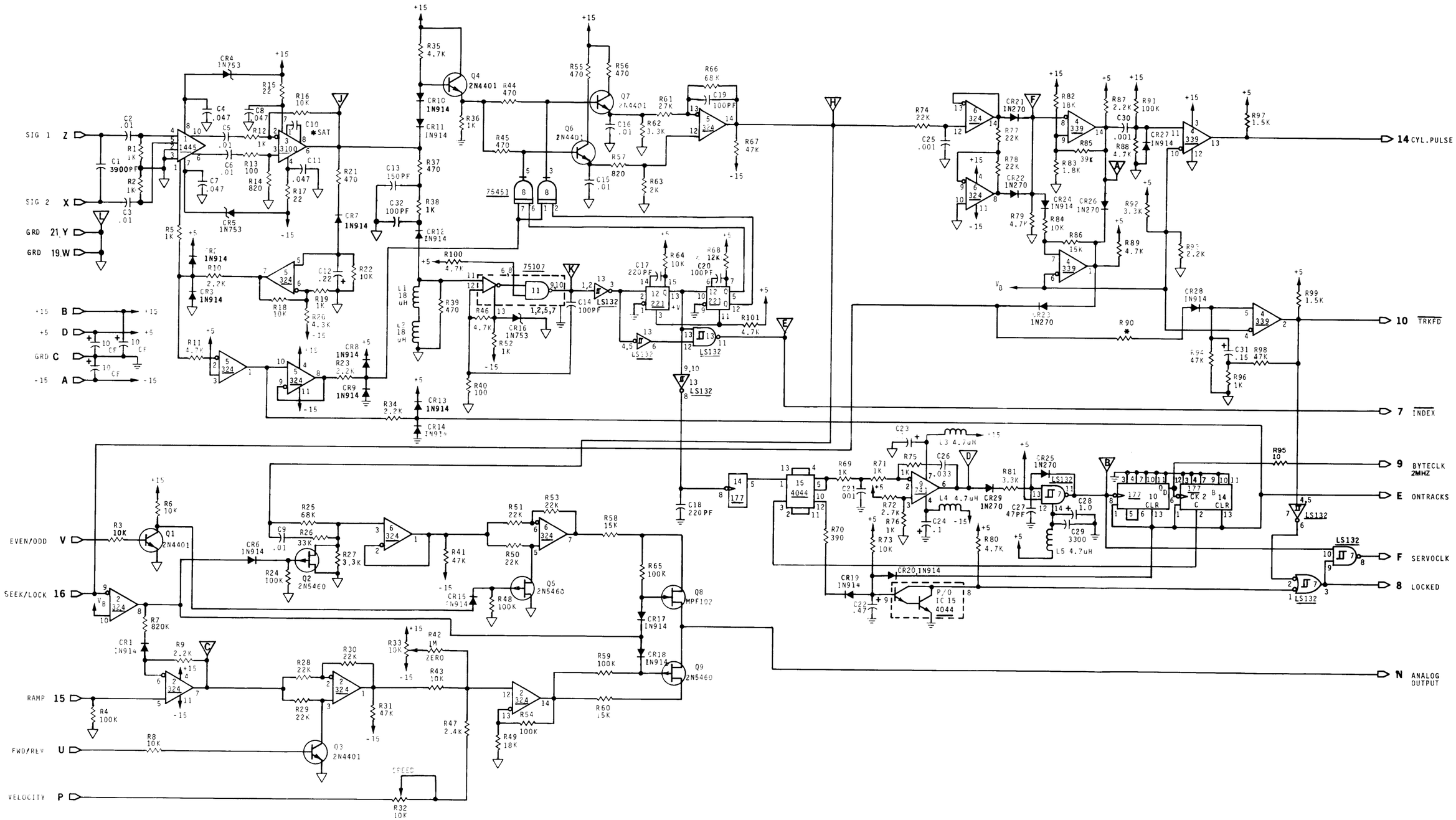
DASH	IC8	IC9
-003	OMIT	INSTALL

Fault Logic
Type 7967
Schematic Diagram

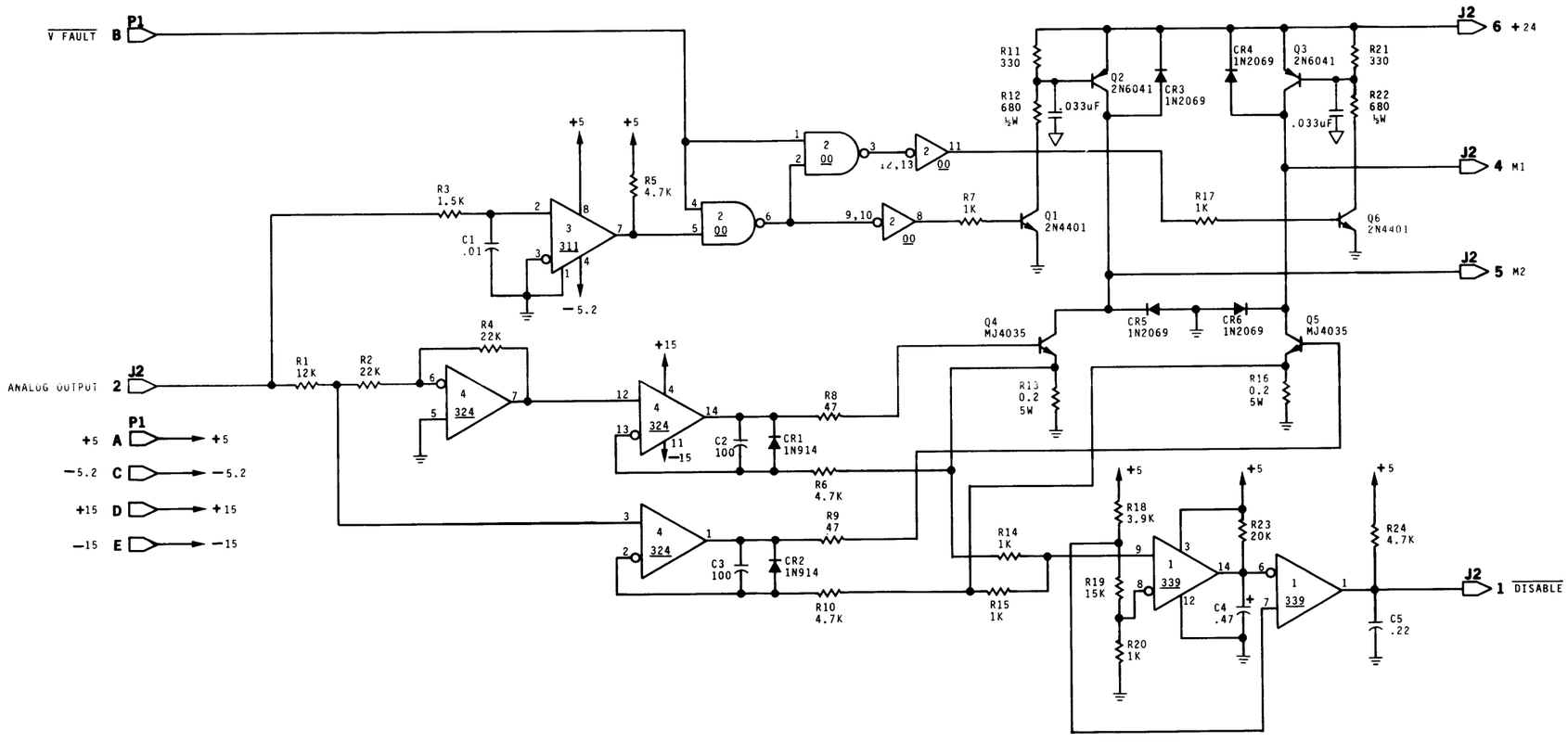


Velocity Preamp,
Type 5886-001C
Schematic Diagram

401-5884-002C



Servo Board
Type 5884-002
Schematic Diagram



Servo Power Amp,
Type 5869-001 E
Schematic Diagram

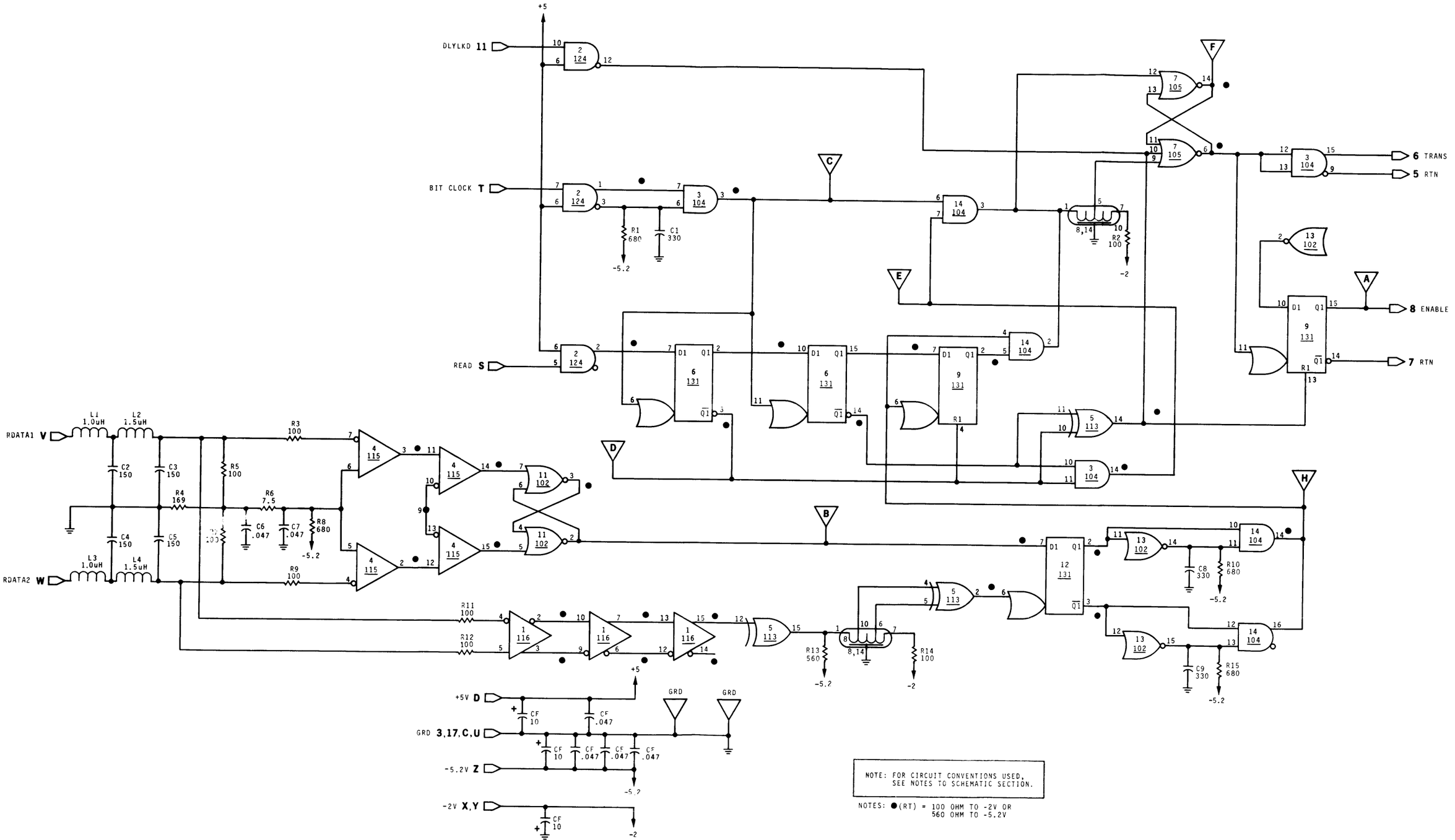
401-5525-001E1

REF DESIGNATOR	
LAST USED	NOT USED
R97	
C35	C15, C20
IC9	
Q15	
L4	
CR12	

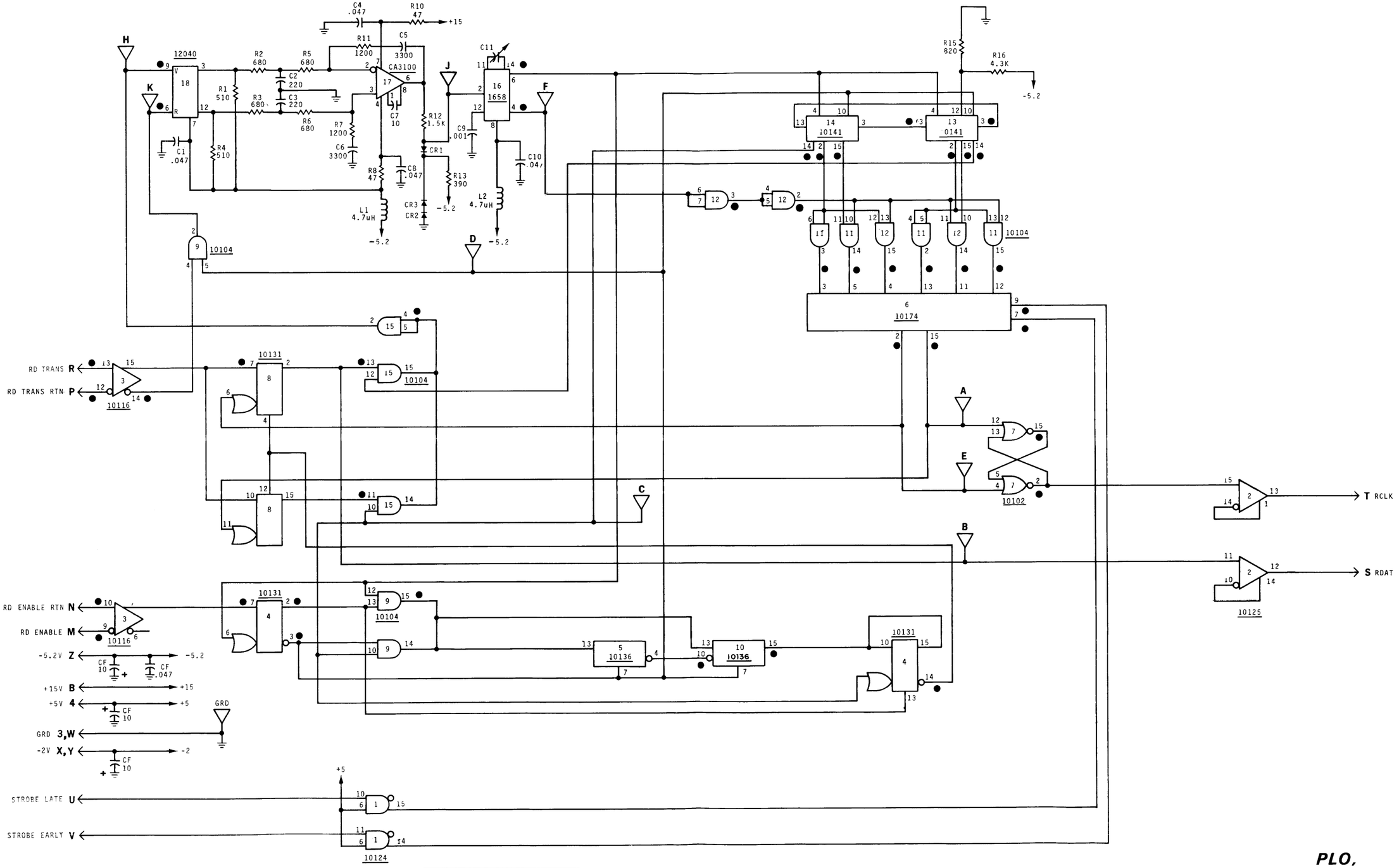
P2
Dx 2
Dy 1
R1 100
R2 200
R3 200
R4 120
R5 120
C1 100PF
Q1 MPF4392
R6 10K
C2
R7 220
33PF
L1 1.5μH
IC4 592
R8 10
+6V
C3 .01
C4 .01
R12 270
R13 270
L2 8.2μH
L3 8.2μH
C5 47PF
C6 100PF
C7 100PF
C8 .047
C9 .047
R14 1K
R15 1K
Q15 MPF4392
R16 3.9K
C10 .1
L4 1.5μH
IC7 592
R17 10
C11 .01
C12 .01
TP2
R18 2.2K
TP1
R20 2.2K
R19 47
Q8 2N2369
Q9 2N2369
R22 270, ½W
R23 270, ½W
-5.2
C13 .047
C14 .047
R21 47
P
Y RDA1
Z RDA2
9 WD2
8 WD1
WS
12 WCURRSENS
T ANDET
W +15V
U +5V
20, X GND
P -5.2V
V -15V
K AC1
L AC2
S HD SEL FAULT
R WTRANS
Q3 2N2369
Q2 2N2369
R26 510
R10 47
R11 47
R25 10K
R27 510
R9 1.5K
CR1 1N750 4.7V
CR2 1N753
R24 150, 1W
C18 .022
C17 .022
Q4 2N4401
R28 3.3K
R30 220
R31 510
Q5 2N4403
R32 750
R54 750
R33 680
R34 4.7K
R62 680 ½W
CR7 1N749
CR8 1N914
R63 3.3K
C16 47
IC1 319
R61 330
R64 100K
R59 4.7K
R58 1K
R55 1K
R56 500
R60 22
R57 10K
R29 10K
Q7 2N4401
Q6 2N4401
CR6 1N5221B 2.4V
R97 10
C35 100PF
R73 3.3K
R72 3.3K
R71 3.3K
R86 4.7K
R87 4.7K
IC2 38
IC6 06
MC10124
IC3
R84 510
R85 510
R40 1K
R41 1K
CR4 1N914
CR5 1N914
Q10 2N4401
R42 150K
R43 10K
R39 10K
R49 3.3K
C19 .0068
R44 150K
Q11 2N4403
R37 10K
R38 1K
Q12 2N4403
R45 22K
R46 1K
R35 100
CR3 1N5221B 2.4V
R36 470
R48 10K
C21 75PF
R51 100K
R50 2.2K
R53 120K
R52 1M
R47 1.5K
IC1 319
R74 10
R75 1K
R76 1K
R77 10K
C23 .001
C24 .01
C25 .01
C26 .001
IC8 741
R83 10K
R88 4.7K
Q13 2N4403
R89 750
R90 680
R91 100K
R93 3.3K
CR9 1N753 5.6V
R92 18K
IC5 339
CR11 1N914
CR10 1N914
R94 330K
C27 .1
R78 47K
R81 2K
R82 2K
R79 1M
R80 3.3K
ST1
R65 2K
R66 2K
R67 6.8K
R68 10K
C22 .001
R69 4.7K
R70 100K
IC9 7806
R95 25 3W
C31 10
C28 0.1
C29 10
C30 10
C33 10
C32 .1
C34 10
Q14 2N4403
CR12 1N750 4.7V
R96 470 ½W
WS 16
Iw 15
CE2 18
CE3 14
CE1 20
+6Vs 9
HS2 19
HS1 17
US 13
3, 4 GND
-4V 5
P1
H 1 HD SEL
F 2
E 1
D 2 ARM SEL

Read/Write Amp Bd.
Type 5525,
Schematic Diagram

401-5980-001B



Data Detector Type 5980-001B, Schematic Diagram



NOTE: FOR CIRCUIT CONVENTIONS USED, SEE NOTES TO SCHEMATIC SECTION.

NOTE: ● = RT, 100 OHM TO -2V

PLO,
Type 5885-001 H
Schematic Diagram

CONTENTS OF 3601

ADDR	DATA	ADDR	DATA
00	2	10	6
01	2	11	6
02	A	12	2
03	A	13	2
04	1	14	1
05	1	15	1
06	5	16	5
07	5	17	5
08	0	18	0
09	0	19	0
0A	0	1A	0
0B	0	1B	0
0C	9	1C	9
0D	9	1D	9
0E	1	1E	1
0F	1	1F	1

401-5865-001F1

FWDATP V
FWDATN W
FWCLKP R
FWCLKN P
SERVO CLK (16MHz) F
AM ENABLED I
WRITE GATE 5
+5VDC 4
+5VDC D
GND 3
GND C
-2VDC Z
-2VDC 22
-5.2VDC E
RDAT N
READ GATE M
RCLK 8
SELECTED/ U
SEEK END T

S BIT CLK
J DSRVCLKP
H DSRVCLKN
2 WSEL/
Y WD1
X WD2
L DRDATP
K DRDATN
10 DRCKLP
9 DRCKLN
7 DSELECTED/
6 DSEEKEND/

E ONE
E ZERO
E LATE
E EARLY
E EARLY

NOTE: ● DENOTES 100Ω PULLDOWN RESISTOR TO -2V.

Radial
Type 5865A-001K
Schematic Diagram