PERKIN-ELMER

INTELLIGENT DISK CONTROLLER (IDC) DISK SYSTEM

Installation and Maintenance Manual

47-032 R13

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Printed in the United States of America

PREFACE

This manual documents the installation, operation and maintenance of a Perkin-Elmer Intelligent Disk Controller (IDC) Disk System. An IDC disk system is a Mass Storage Module (MSM) system or a Medium Capacity - Cartridge Disk Drive (MC-CDD) system having as its controller a printed circuit board referred to as the IDC.

Chapters 1 and 2 are directed towards all users, e.g., sales personnel, instructors, customer engineers, technicians and programmers. Chapter 1 defines what an IDC disk system is. Chapter 2 presents detailed parts lists for possible IDC disk systems and discusses procedures for installing an IDC disk system. Chapters 3 and 4 are directed to customer engineers, technicians and programmers. Chapter 3 describes the operation of the IDC board at the block-diagram level. Chapter 4 presents detailed information necessary for the maintenance of an IDC disk system.

Revisions 10, 11, 12 and 13 include text and drawing changes. Information on the CDD 50 Disk System has also been added.

For information on the contents of all Perkin-Elmer 32-bit manuals, see the 32-Bit Systems User Documentation Summary.

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CHAPTER 1

OVERVIEW

1-1 DESCRIPTION OF AN IDC DISK SYSTEM

A disk system, as defined here, is the hardware that provides a processor with disk support. That is, it provides a processor with the capability of writing to and reading from disk media. And, basically, a disk system consists of these hardware components:

(a) one or more disk files (a disk file is a disk drive with removable or fixed disk media);

(b) a controller for interfacing these disk files to the processor; and

(c) necessary cabling for interconnecting the controller hardware and disk files.

A Perkin-Elmer Intelligent Disk Controller (IDC) Disk System, then, is hardware that provides a Perkin-Elmer 3200-Series processor with support for direct-access devices, or disk files. Chapter 2 specifies all components of the various IDC disk systems. But, as basically shown in Figure 1-1, an IDC disk system consists of:

(a) one controller board, a printed circuit (PC) board referred to as the IDC;

(b) one to four Perkin-Elmer disk files, with specially formatted disk media; and

(c) necessary cabling for connecting the IDC and disk files.

Figure 1-2 shows the IDC PC-board. This board contains microprocessor logic for directly interfacing disk files with the 3200-Series processor. Data transfer to and from the processor, via a Direct Memory Access (DMA) port, is through either a 3200 Selector Channel (SELCH) or Channel Manager (CM). For data recovery from disk read errors, the IDC has the capability of performing strobe-offset or track-offset sequences. It also has an automatic error-correction capability for correcting error bursts of up to 11 bits in length. For detailed programming information on the characteristics of the IDC, refer to Perkin-Elmer Publication 50-007; see Table 1-1.

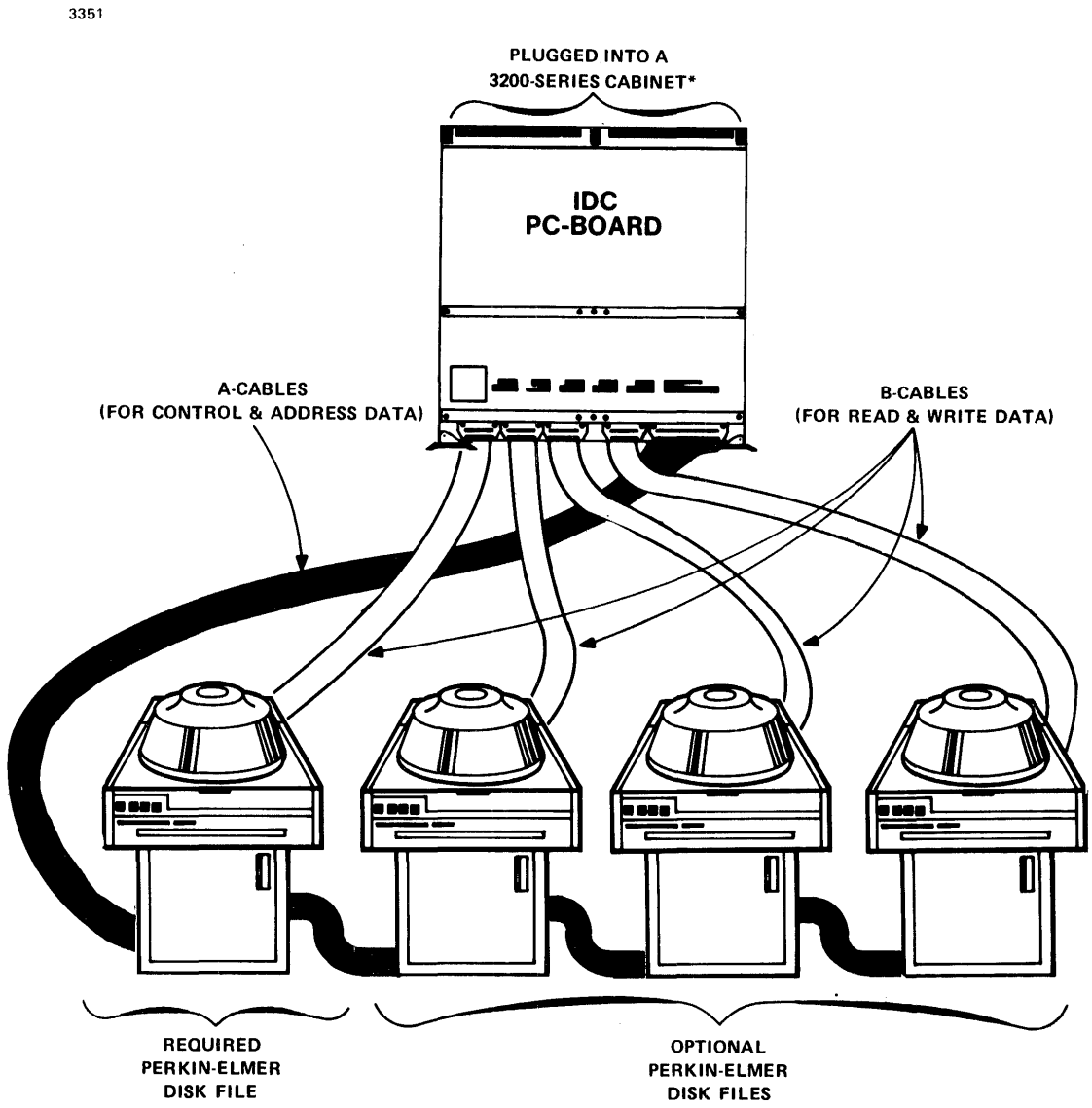
The IDC can interface a maximum of four disk files to the 3200-Series processor, with overlapping seek and restore operations. These can be any combination of Perkin-Elmer disk files, i.e., Mass Storage Modules (MSMs) and/or Medium Capacity - Cartridge Disk Drives (MC-CDDs). For example, four interfaced files might be this combination: 67-Megabyte (Mb) MSM, 256-Mb MSM, 256-Mb MSM, and 81-Mb CDD; or, this combination: 256-Mb MSM, 256-Mb MSM, 256-Mb MSM, and 54-Mb CDD; or, this: 27-Mb CDD, 54-Mb CDD, 81-Mb CDD, and 256-Mb MSM. The IDC board will also support future Perkin-Elmer disk files. For performance data and other information on the supported disk files, refer to the vendor manuals listed in Table 1-1.

NOTE

The disk media of an IDC system have a physical format that is different from and incompatible with the format of MSM disk media. For additional information on these differences, refer to Perkin-Elmer Publication 50-007.

MSM disk drives allow installation of a dual-port option which permits two controllers to share a single disk file; these two controllers can be in the same processor cabinet or in separate processor cabinets. The MC-CDD and CDD 50 systems are not capable of dual-port operation.

Cabling from the IDC board to the disk files is simple and direct because there is no interface, like a control panel, between the board and interfaced files.



* For special applications requiring a Perkin-Elmer I/O Bus Switch, the IDC is installed in a slot under the I/O Bus Switch.

Figure 1-1. Basic IDC Disk System

5001

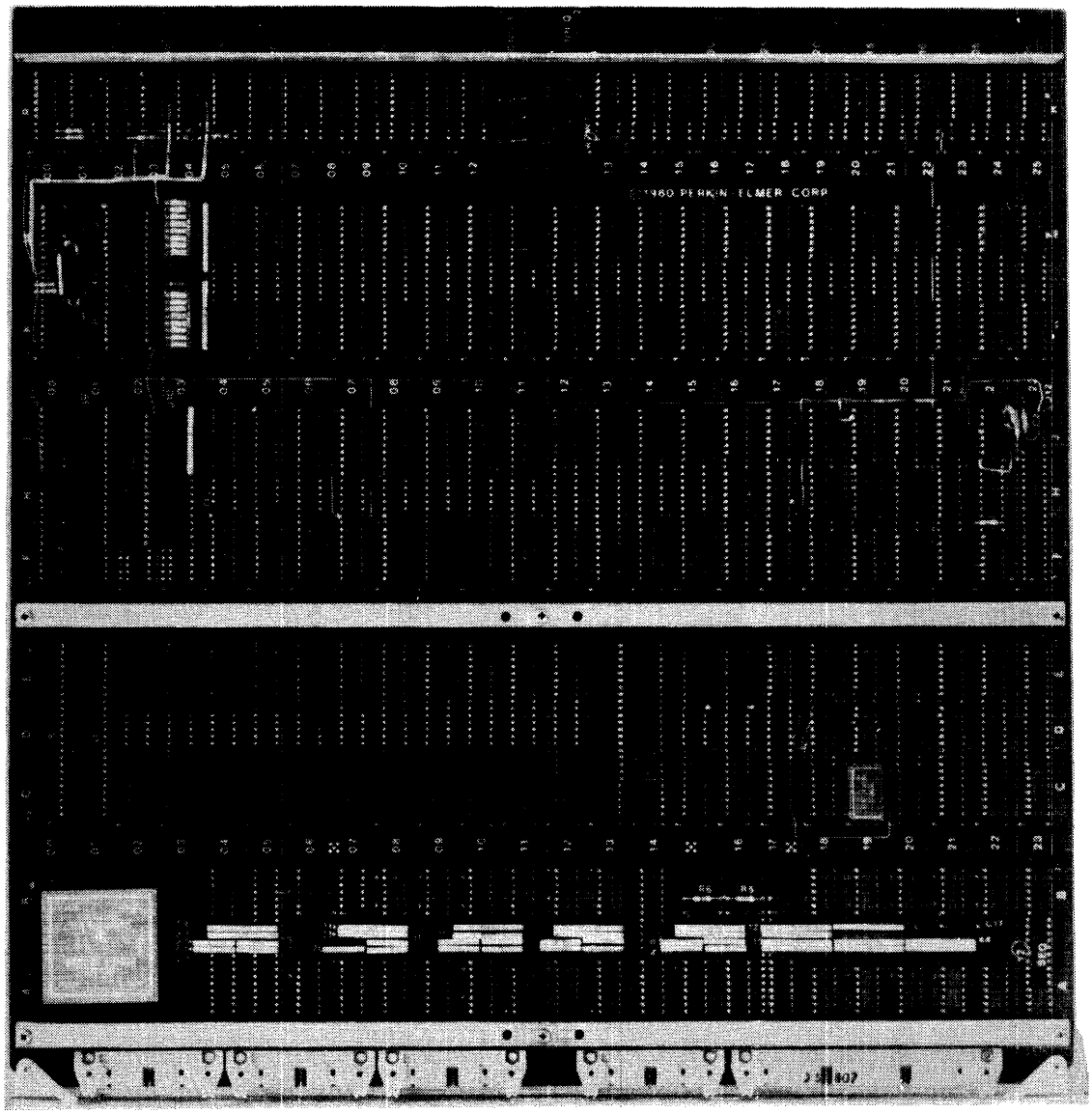


Figure 1-2. IDC PC-Board

1-2 LIST OF RELATED PUBLICATIONS

Table 1-1 lists the Perkin-Elmer manuals related to IDC disk systems.

Table 1-1. List of Related Publications

PUBLICATION NUMBER	PERKIN-ELMER MANUAL
29-356	M48-018 Input/Output Bus Switch Manual-Control Panel Installation Manual
29-585	80-Mb Maintenance Manual Package (This package contains vendor manuals for the 67-Mb MSM removable-media disk systems.)
29-586	300-Mb Maintenance Manual Package (This package contains vendor manuals for the 256-Mb MSM removable-media disk systems.)
29-727	Model 3200 Selector Channel (SELCH) Maintenance Manual
29-729	80-Mb (Fixed) Maintenance Manual Package (This package contains vendor manuals for the 67-Mb MSM fixed-media disk systems.)
29-749	Vendor Manual Cartridge Disk Drive (This manual is for the 27-Mb, 54-Mb, and 81-Mb MC-CDD systems.)
47-016	Channel Manager (CM)
50-007	Intelligent Disk Controller (IDC) Programmer Reference Manual (includes CDD 50 system)
51-041	330-Mb Disk Drive Vendor Manual

CHAPTER 2

INSTALLATION

2-1 INTRODUCTION

This chapter gives detailed parts lists and instructions for installing an intelligent disk controller (IDC) system. Before reading it, you should be familiar with Chapter 1.

2-2 DETAILED PARTS LISTS

Tables 2-1 through 2-18 in this section list the components and give a product number-to-part number cross reference for the disk systems supported by the IDC. Corresponding to these tables are the 18 IDC disk systems:

TABLE	DISK SYSTEM	DESCRIPTION
2-1	1	Removable-Media 67-Mb MSM Disk System, 60 Hertz (Hz)
2-2	2	Removable-Media 67-Mb MSM Disk System, 50 Hz
2-3	3	Fixed-Media 67-Mb MSM Disk System, 60 Hz
2-4	4	Fixed-Media 67-Mb MSM Disk System, 50 Hz
2-5	5	Fixed-Media 67-Mb MSM Disk System, 60 Hz, with HPT*
2-6	6	Fixed-Media 67-Mb MSM Disk System, 50 Hz, with HPT*
2-7	7	Removable-Media 256-Mb MSM Disk System, 60 Hz
2-8	8	Removable-Media 256-Mb MSM Disk System, 50 Hz
2-9	9	27-Mb MC-CDD System, 60 Hz
2-10	10	27-Mb MC-CDD System, 50 Hz
2-11	11	54-Mb MC-CDD System, 60 Hz
2-12	12	54-Mb MC-CDD System, 50 Hz
2-13	13	81-Mb MC-CDD System, 60 Hz
2-14	14	81-Mb MC-CDD System, 50 Hz
2-15	15	Fixed-Media 330-Mb Disk System, 60 Hz
2-16	16	Fixed-Media 330-Mb Disk System, 50 Hz
2-17	17	CDD 50 Disk System, 60 Hz
2-18	18	CDD 50 Disk System, 50 Hz

See Section 2-2.1 for additional cabling information.

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* HPT refers to the Head Per Track option available with the 67-Mb fixed-media disk.

Table 2-1. Removable-Media 67-Mb MSM Disk System, 60 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-102	Single Drive System, 60 Hz, 115 V	02-798F01
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual Package	29-585
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	67-Mb Disk Drive, 60 Hz, and Cable	27-081F04
(1)	Ext A- and B-Cable, 9.14 m (30 ft)	17-447
(1)	Formatted Disk Pack	24-080F02
(1)	Disk-Drive Terminator	35-636
(1)	IDC Board	35-807
M60-110	Expansion Drive, 60 Hz	02-801F01
(1)	Vendor Maintenance Manual Package	29-585
(1)	Ground Strap, 4.57 m (15 ft)	17-295F03
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	External B-Cable, 9.14 m (30 ft)	17-448
(1)	67-Mb Disk Drive, 60 Hz, and Cable	27-081F04
(1)	External A-Cable, 4.57 m (15 ft)	17-449
(1)	Formatted Disk Pack	24-080F02
M60-116	67-Mb Formatted Disk Pack	24-080F02

Table 2-2. Removable-Media 67-Mb MSM Disk System, 50 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-103	Single Drive System, 50 Hz, 220 V	02-798F02
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual Package	29-585
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	67-Mb Disk Drive, 50 Hz, and Cable	27-081F05
(1)	Ext A- and B-Cable, 9.14 m (30 ft)	17-448
(1)	Formatted Disk Pack	24-080F02
(1)	Disk-Drive Terminator	35-636
(1)	IDC Board	35-807
M60-111	Expansion Drive, 50 Hz	02-801F02
(1)	Vendor Maintenance Manual Package	29-585
(1)	Ground Strap, 4.57 m (15 ft)	17-295F03
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	External B-Cable, 9.14 m (30 ft)	17-448
(1)	67-Mb Disk Drive, 50 Hz, and Cable	27-081F05
(1)	External A-Cable, 4.57 m (15 ft)	17-449
(1)	Formatted Disk Pack	24-080F02
M60-116	67-Mb Formatted Disk Pack	24-080F02

Table 2-3. Fixed-Media 67-Mb MSM Disk System, 60 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-104	MSM 80-F, 60 Hz, 115 V	02-799F01
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual Package	29-729
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	67-Mb Fixed-Media Disk Drive, 115 V	27-115F05
(1)	Heavy-Duty Shielded MSM A-Cable, 60 pins, 4.57 m (15 ft)	17-521F01
(1)	Heavy-Duty Shielded MSM B-Cable, 26 pins, 4.57 m (15 ft)	17-520F01
(1)	Disk-Drive Terminator	35-636
(1)	IDC Board	35-807
M60-112	MSM 80-F Expansion, 60 Hz, 115 V	02-802F01
(1)	Vendor Maintenance Manual Package	29-729
(1)	Chassis Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	67-Mb Fixed-Media Disk Drive, 115 V	27-115F05
(1)	Heavy-Duty Shielded MSM A-Cable, 60 Pins, 2.44 m (8 ft)	17-521F02
(1)	Heavy-Duty Shielded MSM B-Cable, 26 Pins, 4.57 m (15 ft)	17-520F01

Table 2-4. Fixed-Media 67-Mb MSM Disk System, 50 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-105	MSM 80-F, 50 Hz, 220 V	02-799F02
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual Package	29-729
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	67-Mb Fixed-Media Disk Drive, 220 V	27-115F06
(1)	Heavy-Duty Shielded MSM A-Cable, 60 pins, 4.57 m (15 ft)	17-521F01
(1)	Heavy-Duty Shielded MSM B-Cable, 26 pins, 4.57 m (15 ft)	17-520F01
(1)	Disk-Drive Terminator	35-636
(1)	IDC Board	35-807
M60-113	MSM 80-F Expansion, 50 Hz, 220V	02-802F02
(1)	Vendor Maintenance Manual Package	29-729
(1)	Chassis Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	67-Mb Fixed-Media Disk Drive, 220 V	27-115F06
(1)	Heavy-Duty Shielded MSM A-Cable, 60 Pins, 2.44 m (8 ft)	17-521F02
(1)	Heavy-Duty Shielded MSM B-Cable, 26 Pins, 4.57 m (15 ft)	17-520F01

Table 2-5. Fixed-Media 67-Mb MSM Disk System, 60 Hz, with HPT

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-106	MSM 80-F w/HPT Option, 60 Hz, 115 V	02-799F03
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual Package	29-729
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	67-Mb Fixed-Media Disk Drive, with 1.6-Mb HPT, 115 V	27-115F07
(1)	Heavy-Duty Shielded MSM A-Cable, 60 pins, 4.57 m (15 ft)	17-521F01
(1)	Heavy-Duty Shielded MSM B-Cable, 26 pins, 4.57 m (15 ft)	17-520F01
(1)	Disk-Drive Terminator	35-636
(1)	IDC Board	35-807
M60-114	MSM 80-F Expansion with HPT, 60 Hz, 115 V	02-802F03
(1)	Vendor Maintenance Manual Package	29-729
(1)	Chassis Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	67-Mb Fixed-Media Disk Drive, with 1.6-Mb HPT, 115 V	27-115F07
(1)	Heavy-Duty Shielded MSM A-Cable, 60 Pins, 2.44 m (8 ft)	17-521F02
(1)	Heavy-Duty Shielded MSM B-Cable, 26 Pins, 4.57 m (15 ft)	17-520F01

Table 2-6. Fixed-Media 67-Mb MSM Disk System, 50 Hz, with HPT

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-107	MSM 80-F w/HPT Option, 50 Hz, 220 V	02-799F04
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual Package	29-729
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	67-Mb Fixed-Media Disk Drive, with 1.6-Mb HPT, 220 V	27-115F08
(1)	Heavy-Duty Shielded MSM A-Cable, 60 pins, 4.57 m (15 ft)	17-521F01
(1)	Heavy-Duty Shielded MSM B-Cable, 26 pins, 4.57 m (15 ft)	17-520F01
(1)	Disk-Drive Terminator	35-636
(1)	IDC Board	35-807
M60-115	MSM 80-F Expansion with HPT, 50 Hz, 220 V	02-802F04
(1)	Vendor Maintenance Manual Package	29-729
(1)	Chassis Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	67-Mb Fixed-Media Disk Drive, with 1.6-Mb HPT, 220 V	27-115F08
(1)	Heavy-Duty Shielded MSM A-Cable, 60 Pins, 2.44 m (8 ft)	17-521F02
(1)	Heavy-Duty Shielded MSM B-Cable, 26 Pins, 4.57 m (15 ft)	17-520F01

Table 2-7. Removable-Media 256-Mb MSM Disk System, 60 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-100	Single Drive System, 60 Hz, 115 V	02-797F01
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual	29-586
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	256-Mb Disk Drive, 60 Hz	27-082F04
(1)	Ext A- and B-Cable, 9.14 m (30 ft)	17-447
(1)	Formatted Disk Pack	24-079F02
(1)	Disk-Drive Terminator	35-636
(1)	IDC Board	35-807
M60-108	Expansion Drive, 60 Hz	02-800F01
(1)	Vendor Maintenance Manual	29-586
(1)	Ground Strap, 4.57 m (15 ft)	17-295F03
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	External B-Cable, 9.14 m (30 ft)	17-448
(1)	256-Mb Disk Drive, 60 Hz	27-082F04
(1)	External A-Cable, 4.57 m (15 ft)	17-449
(1)	Formatted Disk Pack	24-079F02
M60-117	256-Mb Formatted Disk Pack	24-079F02

Table 2-8. Removable-Media 256-Mb MSM Disk System, 50 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-101	Single Drive System, 50 Hz, 220 V	02-797F02
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual	29-586
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	256-Mb Disk Drive, 50 Hz	27-082F05
(1)	Ext A- and B-Cable, 9.14 m (30 ft)	17-447
(1)	Formatted Disk Pack	24-079F02
(1)	Disk-Drive Terminator	35-636
(1)	IDC Board	35-807
M60-109	Expansion Drive, 50 Hz	02-800F02
(1)	Vendor Maintenance Manual	29-586
(1)	Ground Strap, 4.57 m (15 ft)	17-295F03
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	External B-Cable, 9.14 m (30 ft)	17-448
(1)	256-Mb Disk Drive, 50 Hz, and Cable	27-082F05
(1)	External A-Cable, 4.57 m (15 ft)	17-449
(1)	Formatted Disk Pack	24-079F02
M60-117	256-Mb Formatted Disk Pack	24-079F02

Table 2-9. 27-Mb MC-CDD System, 60 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M46-770	MC-CDD 27, 60 Hz, 115 V	02-777F03
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual	29-749
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	27-Mb MC-CDD, 60 Hz, 115 V	27-131F03
(1)	Ext A- and B-Cable, 4.57 m (15 ft)	17-447F01M01
(1)	Disk-Drive Terminator	35-815
(1)	IDC Board	35-807
(1)	Mounting Kit	16-876
M46-732	Expansion Drive, MC-CDD 27, 60 Hz	02-761F01
(1)	Vendor Maintenance Manual	29-749
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	External B-Cable, 4.57 m (15 ft)	17-448F01
(1)	27-Mb MC-CDD, 60 Hz, 115 V	27-131F03
(1)	External A-Cable, 1.07 m (42 in)	17-411F03M01
(1)	External A-Cable, 4.57 m (15 ft)	17-449
(1)	Formatted Disk Cartridge, 13.5 Mb	24-104F02
(1)	Mounting Kit	16-876
M46-776	13.5-Mb Formatted Disk Cartridge	24-104F02

Table 2-10. 27-Mb MC-CDD System, 50 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M46-771	MC-CDD 27, 50 Hz, 220 V	02-777F04
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual	29-749
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	27-Mb MC-CDD, 50 Hz, 220 V	27-131F04
(1)	Ext A- and B-Cable, 4.57 m (15 ft)	17-447F01M01
(1)	Disk-Drive Terminator	35-815
(1)	IDC Board	35-807
(1)	Mounting Kit	16-876
M46-733	Expansion Drive, MC-CDD 27, 50 Hz	02-761F02
(1)	Vendor Maintenance Manual	29-749
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	External B-Cable, 4.57 m (15 ft)	17-448F01
(1)	27-Mb MC-CDD, 50 Hz, 220 V	27-131F04
(1)	External A-Cable, 1.07 m (42 in)	17-411F03M01
(1)	External A-Cable, 4.57 m (15 ft)	17-449
(1)	Formatted Disk Cartridge, 13.5 Mb	24-104F02
(1)	Mounting Kit	16-876

Table 2-11. 54-Mb MC-CDD System, 60 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M46-772	MC-CDD 54, 60 Hz, 115 V	02-778F03
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual	29-749
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	54-Mb MC-CDD, 60 Hz, 115 V	27-130F03
(1)	Ext A- and B-Cable, 4.57 m (15 ft)	17-447F01M01
(1)	Disk-Drive Terminator	35-815
(1)	IDC Board	35-807
(1)	Mounting Kit	16-876
M46-734	Expansion Drive, MC-CDD 54, 60 Hz	02-762F01
(1)	Vendor Maintenance Manual	29-749
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	External B-Cable, 4.57 m (15 ft)	17-448F01
(1)	54-Mb MC-CDD, 60 Hz, 115 V	27-130F03
(1)	External A-Cable, 1.07 m (42 in)	17-411F03M01
(1)	External A-Cable, 4.57 m (15 ft)	17-449
(1)	Formatted Disk Cartridge, 13.5 Mb	24-104F02
(1)	Mounting Kit	16-876

Table 2-12. 54-Mb MC-CDD System, 50 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M46-773	MC-CDD 54, 50 Hz, 220 V	02-778F04
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual	29-749
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	54-Mb MC-CDD, 50 Hz, 220V	27-130F04
(1)	Ext A- and B-Cable, 4.57 m (15 ft)	17-447F01M01
(1)	Disk-Drive Terminator	35-815
(1)	IDC Board	35-807
(1)	Mounting Kit	16-876
M46-735	Expansion Drive, MC-CDD 54, 50 Hz	02-762F02
(1)	Vendor Maintenance Manual	29-749
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	External B-Cable, 4.57 m (15 ft)	17-448F01
(1)	54-Mb MC-CDD, 50 Hz, 220 V	27-130F04
(1)	External A-Cable, 1.07 m (42 in)	17-411F03M01
(1)	External A-Cable, 4.57 m (15 ft)	17-449
(1)	Formatted Disk Cartridge, 13.5 Mb	24-104F02
(1)	Mounting Kit	16-876

Table 2-13. 81-Mb MC-CDD System, 60 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M46-774	MC-CDD 81, 60 Hz, 115 V	02-779F03
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual	29-749
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	81-Mb MC-CDD, 60 Hz, 115V	27-129F03
(1)	Ext A- and B-Cable, 4.57 m (15 ft)	17-447F01M01
(1)	Disk-Drive Terminator	35-815
(1)	IDC Board	35-807
(1)	Mounting Kit	16-876
M46-736	Expansion Drive, MC-CDD 81, 60 Hz	02-763F01
(1)	Vendor Maintenance Manual	29-749
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	External B-Cable, 4.57 m (15 ft)	17-448F01
(1)	81-Mb MC-CDD, 60 Hz, 115 V	27-129F03
(1)	External A-Cable, 1.07 m (42 in)	17-411F03M01
(1)	External A-Cable, 4.57 m (15 ft)	17-449
(1)	Formatted Disk Cartridge, 13.5 Mb	24-104F02
(1)	Mounting Kit	16-876

Table 2-14. 81-Mb MC-CDD System, 50 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M46-775	MC-CDD 81, 50 Hz, 220 V	02-779F04
(1)	IDC Installation/Maintenance Manual	47-032
(1)	Vendor Maintenance Manual	29-749
(1)	IDC Programming Manual	50-007
(1)	Test Program	06-267
(1)	Format Program	06-268
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	81-Mb MC-CDD, 50 Hz, 220 V	27-129F04
(1)	Ext A- and B-Cable, 4.57 m (15 ft)	17-447F01M01
(1)	Disk-Drive Terminator	35-815
(1)	IDC Board	35-807
(1)	Mounting Kit	16-876
M46-737	Expansion Drive, MC-CDD 81, 50 Hz	02-763F02
(1)	Vendor Maintenance Manual	29-749
(1)	Ground Strap, 1.07 m (42 in)	17-295F05
(1)	Ground Strap, 1.83 m (6 ft)	17-295F04
(1)	External B-Cable, 4.57 m (15 ft)	17-448F01
(1)	81-Mb MC-CDD, 50 Hz, 220 V	27-129F04
(1)	External A-Cable, 1.07 m (42 in)	17-411F03M01
(1)	External A-Cable, 4.57 m (15 ft)	17-449
(1)	Formatted Disk Cartridge, 13.5 Mb	24-104F02
(1)	Mounting Kit	16-876

Table 2-15. Fixed-Media 330-Mb Disk System 60 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-120	MSM300F Disk System 115 V,60 Hz	02-830F01
(1)	IDC Disk Test Program	06-267
(1)	IDC Disk Format Program	06-268
(1)	Installation Kit	16-932
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	Ext A- and B-Cable, 4.57 m (15 ft)	17-447F01
(1)	330-Mb Disk Drive 115 V, 60 Hz	27-148F01
(1)	Intelligent Disk Controller	35-807
(1)	Disk-Drive Terminator	35-852
(1)	Installation/Maintenance Manual	47-032
(1)	IDC Programming Manual	50-007
(1)	Vendor Maintenance Manual	51-041
M60-122	MSM300FE Disk Exp. 115 V, 60 Hz	02-831F01
(1)	IDC Disk Test Program	06-267
(1)	IDC Disk Format Program	06-268
(1)	Installation Kit	16-932
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	External A-Cable, 2.44 m (8 ft)	17-449F01
(1)	External B-Cable, 4.57 m (15 ft)	17-448F01
(1)	330-Mb Disk Drive 115 V, 60 Hz	27-148F01
(1)	Vendor Maintenance Manual	51-041

Table 2-16. Fixed-Media 330-Mb Disk System, 50 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-121	MSM300F Disk System 230 V, 50 Hz	02-830F02
(1)	IDC Disk Test Program	06-267
(1)	IDC Disk Format Program	06-268
(1)	Installation Kit	16-932
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	Ext A- and B-Cable, 4.57 m (15 ft)	17-447F01
(1)	330 Mb Disk Drive 230 V, 50 Hz	27-148F02
(1)	Intelligent Disk Controller	35-807
(1)	Disk-Drive Terminator	35-852
(1)	Installation/Maintenance Manual	47-032
(1)	IDC Programming Manual	50-007
(1)	Vendor Maintenance Manual	51-041
M60-123	MSM300FE Disk Exp. 230 V, 50 Hz	02-831F02
(1)	IDC Disk Test Program	06-267
(1)	IDC Disk Format Program	06-268
(1)	Installation Kit	16-932
(1)	Ground Strap, 9.14 m (30 ft)	17-295F01
(1)	External A-Cable, 2.44 m (8 ft)	17-449F01
(1)	External B-Cable, 4.57 m (15 ft)	17-448F01
(1)	330-Mb Disk Drive 230 V, 50 Hz	27-148F02
(1)	Vendor Maintenance Manual	51-041

Table 2-17. CDD 50 Disk System 60 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-140	CDD 50 Disk System 115 V, 60 Hz	02-841F01
(1)	Disk Test Program	06-267
(1)	IDC Disk Format Program	06-268
(1)	Installation Kit	16-942F01
(1)	Intelligent Disk Controller	02-734
(1)	Disk Drive 50Mb (115 V AC)	27-149F01
(1)	Cartridge Disk-25 Mb	24-109
(1)	Terminator Board	35-876
(1)	A/B Cable (shielded)	17-663
(1)	10" Ground Cable	17-584F01
(1)	24" Ground Cable	17-584F02
(1)	36" Ground Cable	17-585F02
(1)	Manual, Installation & Maintenance	47-032
(1)	Manual, Programming	50-007
(1)	Manual, Vendor Maintenance	51-054
M60-142	CDD 50E Disk System 115 V, 60 Hz	02-842F01
(1)	IDC Disk Test Program	06-267
(1)	IDC Disk Format Program	06-268
(1)	Installation Kit	16-942F02
(1)	Disk Drive 50 Mb (115 V AC)	27-149F01
(1)	Cartridge Disk-25 Mb	24-109F01
(1)	"A" Cable	17-664
(1)	"B" Cable	17-665
(1)	10" Ground Cable	17-584F01
(1)	24" Ground Cable	17-584F02
(1)	36" Ground Cable	17-585F02
(1)	Manual, Vendor Maintenance	51-054

Table 2-18. CDD 50 Disk System 50 Hz

PRODUCT NO (QUANTITY)	DESCRIPTION	PART NUMBER
M60-141	CDD 50 Disk System 230 V, 50 Hz	02-841F02
(1)	IDC Disk Test Program	06-267
(1)	IDC Disk Format Program	06-268
(1)	Installation Kit	16-942F01
(1)	Intelligent Disk Controller	02-734
(1)	Disk Drive 50 Mb (230 V AC)	27-149F02
(1)	Cartridge Disk-25 Mb	24-109F01
(1)	Terminator Board	35-876
(1)	A/B Cable (shielded)	17-663
(1)	10" Ground Cable	17-584F01
(1)	24" Ground Cable	17-584F02
(1)	36" Ground Cable	17-585F02
(1)	Manual, Installation & Maintenance	47-032
(1)	Manual, Programming	50-007
(1)	Manual, Vendor Maintenance	51-054
M60-143	CDD 50E Disk System 230 V, 50 Hz	02-842F02
(1)	IDC Disk Test Program	06-267
(1)	IDC Disk Format Program	06-268
(1)	Installation Kit	16-942F02
(1)	Disk Drive 50 Mb (230 V AC)	27-149F02
(1)	Cartridge Disk-25 Mb	24-109F01
(1)	"A" Cable	17-664
(1)	"B" Cable	17-665
(1)	10" Ground Cable	17-584F01
(1)	24" Ground Cable	17-584F02
(1)	36" Ground Cable	17-585F02
(1)	Manual, Vendor Maintenance	51-054

2-2.1 Additional Cabling Information

Table 2-19 is a summary of all the cables and straps associated with the IDC disk systems. As listed in the table, those cables and straps having a functional variation with the part number are selectable for your particular system. For example, instead of installing the 15-ft A-cable numbered 17-521F01, you can select the 8-ft A-cable numbered 17-521F02.

Table 2-19. Standard Cabling Supplied with IDC Disk Systems

PART NO.	CABLE/STRAP	DESCRIPTION
17-447	External A-Cable and B-Cable	Shielded, 9.14m (30 ft), for 1st drive of all removable-media systems.
17-447F01 M01	External A-Cable and B-Cable	Shielded, 4.57m (15 ft), for 1st drive of all MC-CDD systems.
17-448	External B-Cable	Shielded, 9.14m (30 ft), for 2nd, 3rd, and 4th drives of all removable-media disk systems.
17-448F01	External B-Cable	Shielded, 4.57m (15 ft), for 2nd, 3rd, and 4th drives of all MC-CDD systems.
17-449	External A-Cable	Shielded, 4.57m (15 ft), for 2nd 3rd, and 4th drives of all removable-media disk systems.
17-520F01	External B-Cable	Heavy-duty, shielded, 4.57m (15 ft), for all drives of fixed-media 67-Mb systems.
17-521F01	External A-Cable	Heavy-duty, shielded, 4.57m (15 ft), for first drive of fixed-media 67-Mb systems.
17-521F02	External A-Cable	Heavy-duty, shielded, 2.44m (8 ft), for 2nd, 3rd, and 4th drives of fixed-media 67-Mb systems.
17-411F03 M01	External A-Cable	Heavy-duty, shielded, 1.07m (42 in), for 2nd, 3rd, and 4th drives of MC-CDD systems.
17-663	External A-Cable and B-Cable	Shielded, 1.52m (5 ft), for 1st drive of CDD 50 systems.
17-664	External A-Cable	Shielded, 1.07m (3.5 ft), for all drives of CDD 50 systems.
17-665	External B-Cable	Shielded, 1.52m (5 ft), for all drives of CDD 50 systems.
17-295F01	Ground Strap	9.14m (30 ft)
17-295F03	Ground Strap	4.57m (15 ft)
17-295F04	Ground Strap	1.83m (6 ft)
17-295F05	Ground Strap	1.07m (42 in)

2-3 UNPACKING INSTRUCTIONS

For instructions on how to unpack your particular IDC disk system, see the supplied vendor manuals. These manuals are listed in Table 1-1 and in the tables of Section 2-2.

2-4 INSTALLING AN IDC DISK SYSTEM

Figure 2-1 is a general illustration of how to install a normal IDC disk system. A normal IDC disk system is one which has the IDC board plugged into the processor cabinet and employs the normal SELCH protocol. IDC (35-807) revision level 10 and above must have its backpanel pin 224-1 wired to its SELCH backpanel pin 224-1. But if the IDC board for your system is installed with a Perkin-Elmer I/O Bus Switch, and consequently employs the "new" high-speed SELCH protocol, then your system is not normal. Its installation requires the additional information presented in Perkin-Elmer Publication 29-356.

Along with the applicable vendor manuals listed in Table 1-1 and the relevant tables in Section 2-2, Figure 2-1 should enable you to install your particular IDC disk system. However, before plugging in your IDC board and connecting the cables as shown in the figure, you must set two address switches; see Section 2-4.1. For optional IDC board strapping, see Section 2-4.2.

Refer to Section 2-5 if one or more of your disk drives are to be equipped with a dual-port option.

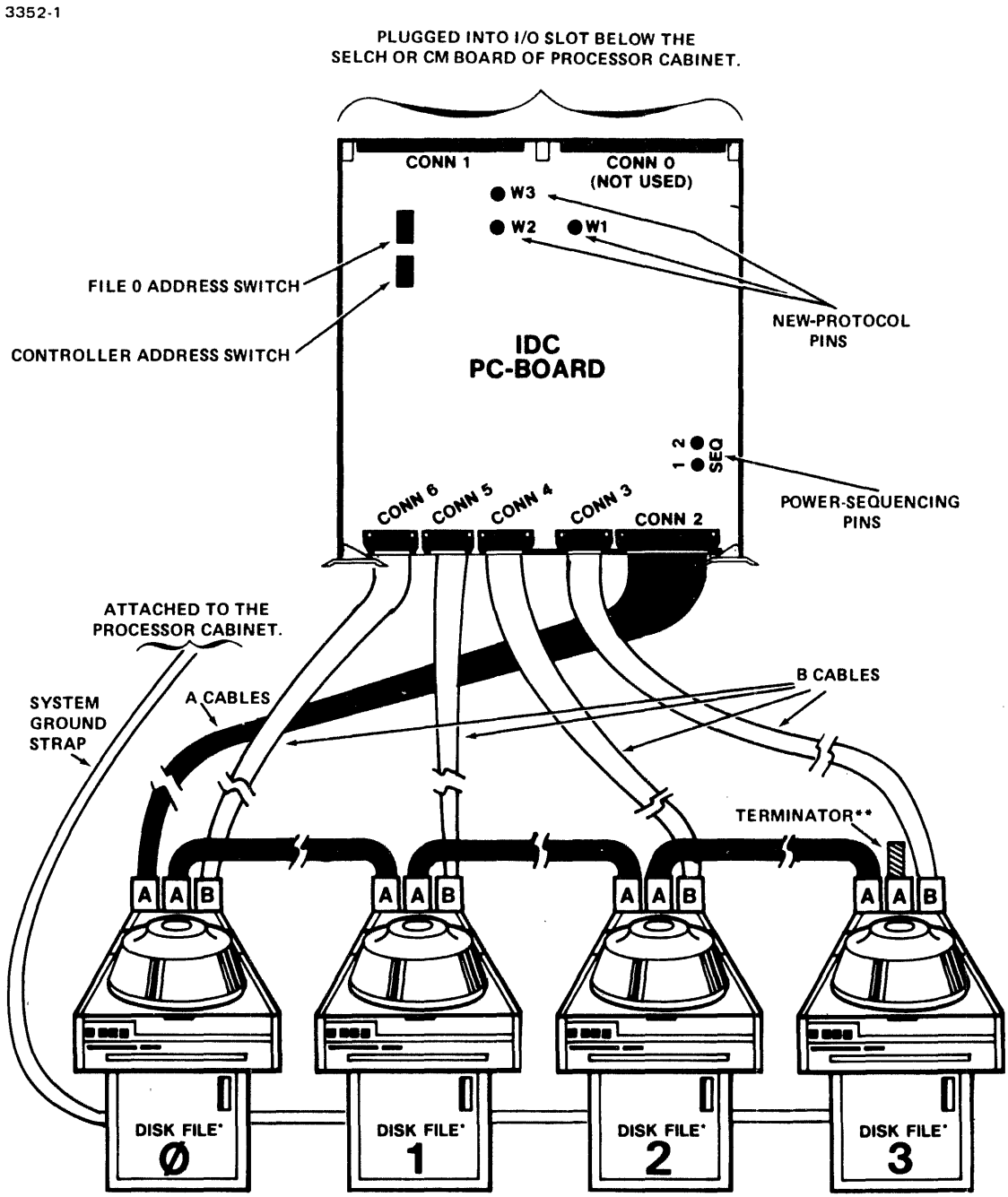
2-4.1 Setting the Address Switches on the IDC Board

As seen from Figures 1-2 and 2-1, the IDC board has two address switches in its upper-left corner:

(1) Controller Address Switch (or Device Address Switch)
(2) File-0 Address Switch

Figures 2-2 and 2-3 present an up-close view of these switches. As shown in Figure 2-2, the Controller Address Switch has eight toggles, numbered 1 through 8, each with two possible settings: 0 or 1. Each toggle setting represents a bit in a 1-byte controller address, with toggle-1 being the most significant bit (MSB) and toggle-8 being the least significant bit (LSB). You must set the toggles to the address wanted for your IDC.

As shown in Figure 2-3, the File-0 Address Switch also has eight toggles, numbered 1 through 8, each with two possible settings: 0 or 1. Toggles 1 through 6 represent six bits in a 1-byte address for your disk file 0, with toggle-1 being the MSB. The other two bits of the 1-byte address are always considered as zero. Toggles 7 and 8, which will be discussed shortly, are for selecting the new high-speed SELCH protocol and for enabling or disabling IDC formatting capability. They are not used for addressing.



* Connector numbers depend on the disk files configured.
** Last disk drive must have a terminator, as shown with the A-cable plug.

Figure 2-1. Installation of an IDC Disk System

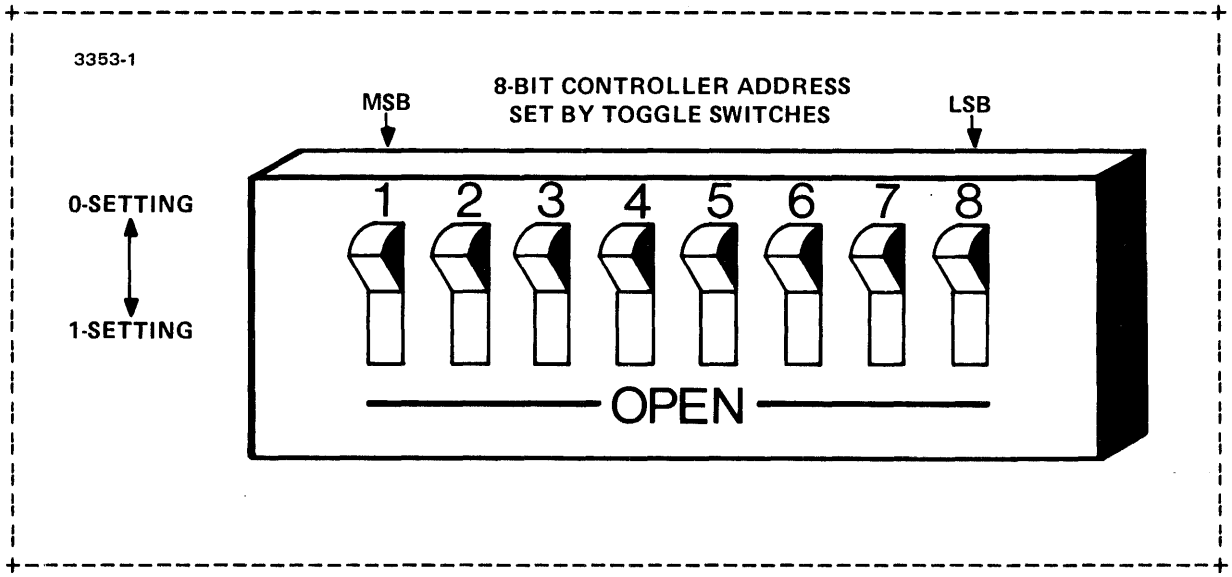


Figure 2-2. Controller Address Switch

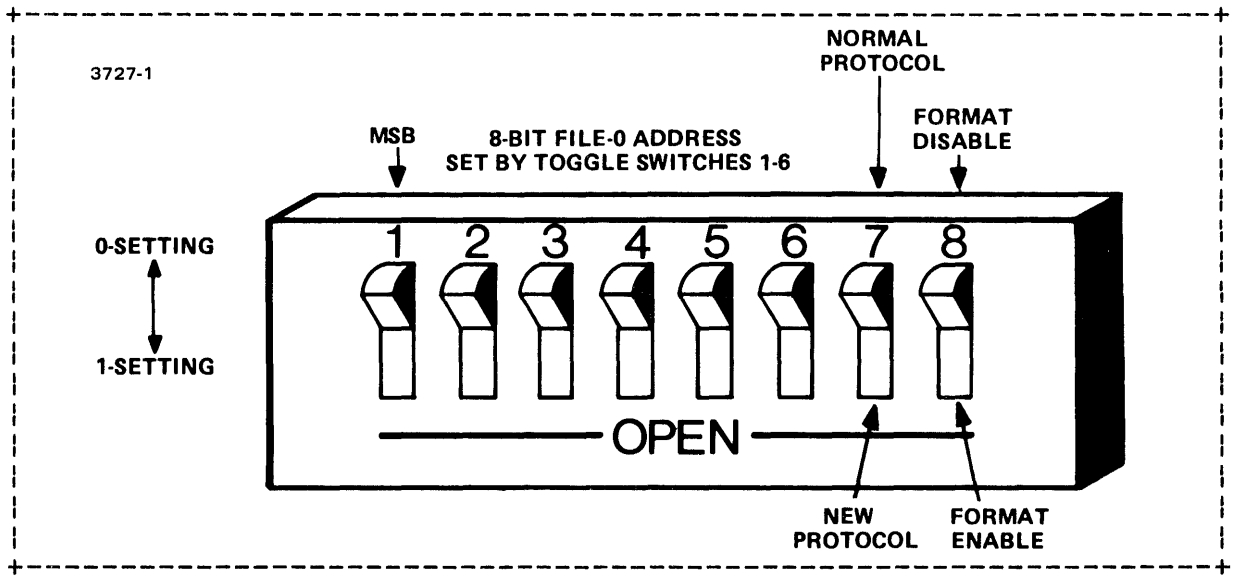


Figure 2-3. File-0 Address Switch

As an example for setting addresses on these switches, suppose you have an IDC system consisting of one IDC board and four disk files. You want the controller address to be X'FB' and the four disk file addresses to be X'FC' through X'FF'. Before installing the IDC board, you would set the Controller Address Switch to the binary value of '11111011' (for X'FB') and the File-0 Address Switch to '11111100' (for X'FC'). Disk files 1 through 3 are automatically addressed at X'FD', X'FE' and X'FF', respectively.

Now, with the wanted addresses set on the two switches, you have the option of setting toggle-7 and/or toggle-8 in the File-0 Address Switch. If you want to employ the normal SELCH protocol, you push toggle-7 up to the 0-setting. But if your IDC is plugged into the 25-foot cable of an I/O Bus Switch, you must push toggle-7 down to the 1-setting, thereby employing the "new" high-speed SELCH protocol. For additional information on the I/O Bus Switch, see Perkin-Elmer Publication 29-356. (Also, as discussed in Section 2-4.2, the new-protocol pins W1 and W3 should be strapped when toggle-7 is at the 1-setting.) In summary, then, place toggle-7 in the 0-setting when your IDC board is plugged into the processor cabinet; place toggle-7 in the 1-position when your IDC board is plugged into the I/O Bus Switch.

Toggle-8 of the File-0 Address Switch is usually left in the 1-setting to enable IDC formatting. That is, if you want the capability of formatting an unformatted disk according to IDC format, leave toggle-8 down. Perkin-Elmer Publication 50-007 describes the IDC disk-media format in detail. But if, for some reason, you want to disable the IDC formatting capability, push toggle-8 up to the 0-position.

2-4.2 IDC Strapping Information

As shown in Figures 2-1 and 1-2, the IDC board has two sets of pins:

(1) Power Sequencing (SEQ) Pins 1 and 2
(2) New-Protocol Pins W1 thru W3

Power sequencing refers to the serial application of power to the disk files once the processor is turned on, where: after disk file 0 is powered and comes up to speed, disk file 1 is powered up; after disk file 1 comes up to speed, disk file 2 is powered up; and so forth. When you want your disk files to power up sequentially, do not place a jumper wire across the Power Sequencing (SEQ) Pins 1 and 2. Also ensure that the Local/Remote Switch on each attached disk file is in the Remote position. Subsequently, when the processor is turned off, the disk files power down simultaneously. When pins 1 and 2 are strapped, or when the Local/Remote Switch on each attached disk file is in the Local position, the disk files can be simultaneously powered up -- in parallel, as opposed to serial. Occasionally, simultaneous application of power to the disk files causes an excessive power surge. To determine the advisability of power sequencing to prevent this, refer to the AC power requirements presented in Section 2-6.

The New-Protocol Pins W1, W2, and W3 apply to the use of the "new" high-speed SELCH protocol for special applications. When your IDC is installed under an I/O Bus Switch, and when toggle-7 of the File-0 Address Switch is down in the 1-setting, you must strap pins W1 and W3.

2-5 INSTALLING DUAL-PORT OPTIONS

Only the 67-Mb and 256-Mb removable-media disk systems can be equipped for dual-port operation. Hardware for the dual-port option consists of four items:

(1) IDC Board
(2) Dual-Port Kit
(3) A-Cable and B-Cable
(4) Disk-Drive Terminator

Sections 2-5.1 thru 2-5.4 discuss the installation of these items.

2-5.1 IDC Board

The additional IDC board supplied with the dual-port option can be plugged into the same processor cabinet with the other controller, or it can be plugged into another processor cabinet. To install the controller in the same cabinet, plug it into the first available backpanel I/O slot below the other controller -- after removing the RACK0/TACK0 wire from that backpanel. Or, to install the controller into another cabinet, plug it into the first available I/O slot immediately below the SELCH or Channel Manager (CM) board.

2-5.2 Dual-Port Kit

The Dual-Port Kit consists of these components: Driver/Receiver PC-Boards, Add-On Connectors for the disk file and a Dual-Port Steering Card.

After installing the two PC-boards and the Add-On Connectors to the disk drive according to supplied instructions, install the Dual-Port Steering Card. But first, set three switches on this card according to the operational requirements. Figure 2-4 illustrates and Table 2-20 describes these switches and associated indicator lights.

2-5.3 A-Cable and B-Cable

A- and B-cable connections depend on whether you are installing just one dual-port option or more than one. Cable connections for a single dual-port disk file are similar to those shown for disk file 0 in Figure 2-1, with one exception: instead of plugging the cables into the plugs labeled A and B in that figure, you plug them into the corresponding A and B Add-On Connectors. On a second, third or fourth dual-ported drive, the A-cable connects to a previously dual-ported drive. With the exception just mentioned, Figure 2-1 also illustrates cable connections for a completely dual-ported IDC disk system.

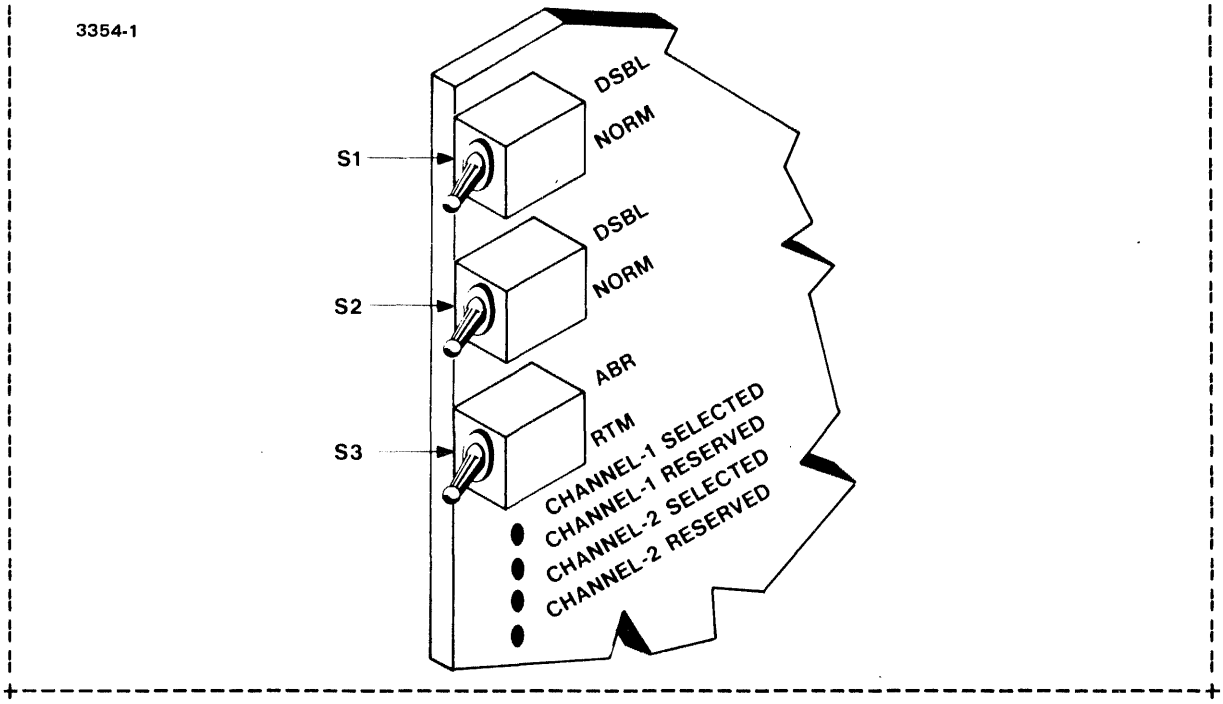


Figure 2-4. Switches and Indicators on Dual-Port Steering Card

Table 2-20. Switches and Indicators on Dual-Port Steering Card

SWITCHES/INDICATORS	FUNCTION
S1, Maintenance Unit-Disable Switch for Channel-1	This switch has two positions: Normal (NORM) and Disable (DSBL). It lets you disable Channel-1 in the disk drive; i.e., it allows you to disable all transmissions from the disk drive to the controller connected to Channel-1. For dual-port operation, S1 should be set to the NORM position, along with S2. During maintenance, S1 should be set to the DSBL position, along with S2.
S2, Maintenance Unit-Disable Switch for Channel-2	This switch has two positions: Normal (NORM) and Disable (DSBL). It lets you disable Channel-2 in the disk drive; i.e., it allows you to disable all transmissions from the disk drive to the controller connected to Channel-2.

Table 2-20. Switches and Indicators on Dual-Port Steering Card (Continued)

SWITCHES/INDICATORS	FUNCTION
	For dual-port operation, S2 should be set to the NORM position, along with S1. During maintenance, S2 should be set to the DSBL position, along with S1.
S3, Release Timer Select Switch	This switch has two positions: Reserve Timer (RTM) and Absolute Reserve (ABR). If you set S3 to RTM, the controller at either channel has about 5 seconds to use the disk file after selecting it. If the controller does not use the file within 5 seconds, it becomes available to the controller at the other channel. If you set the switch to ABR, the controller at either channel has exclusive, uninterruptible use of a disk file; i.e., the controller continues uninterrupted use of that disk file until it issues a Release command.
Channel-1 Selected Indicator	Lights to indicate that the Channel-1 controller has selected the drive in RTM mode.
Channel-1 Reserved Indicator	Lights to indicate that the Channel-1 controller has reserved the drive in ABR mode.
Channel-2 Selected Indicator	Lights to indicate that the Channel-2 controller has selected the drive in RTM mode.
Channel-2 Reserved Indicator	Lights to indicate that the Channel-2 controller has reserved the drive in ABR mode.

2-5.4 Disk-Drive Terminator

As with single-port disk drives, the last dual-port disk drive attached to the IDC board must have a terminator plugged into the Add-On Connector of its A-cable plug.

2-6 AC-POWER REQUIREMENTS

Table 2-21 lists power requirements for the disk drives supported by IDC.

Table 2-21. AC Voltage and Current Requirements for Disk Files*

DISK DRIVES (PART NO'S)	INPUT VOLTS	CURRENT REQUIREMENTS	
		STARTING CURRENT	RUNNING CURRENT
27-081F04	115 V 60 Hz	30 amps for 15 seconds	8.9 amps maximum
27-081F05	220 V 50 Hz	23 amps for 15 seconds	4.6 amps maximum
27-115F05	115 V 60 Hz	23 amps for 7 seconds	4.7 amps maximum
27-115F06	220 V 50 Hz	14 amps for 7 seconds	2.7 amps maximum
27-115F07	115 V 60 Hz	23 amps for 7 seconds	4.7 amps maximum
27-115F08	220 V 50 Hz	14 amps for 7 seconds	2.7 amps maximum
27-082F04	115 V 60 Hz	38 amps for 10 seconds	8.6 amps maximum
27-082F05	220 V 50 Hz	41 amps for 7 seconds	9.2 amps maximum
27-131F03	115 V 60 Hz	23 amps for 7 seconds	5.0 amps maximum
27-131F04	220 V 50 Hz	13 amps for 7 seconds	2.7 amps maximum
27-130F03	115 V 60 Hz	23 amps for 7 seconds	5.0 amps maximum
27-130F04	220 V 50 Hz	13 amps for 7 seconds	2.7 amps maximum
27-129F03	115 V 60 Hz	23 amps for 7 seconds	5.0 amps maximum
27-129F04	220 V 50 Hz	13 amps for 7 seconds	2.7 amps maximum
27-148F01	115 V 60 Hz	20 amps for 10 seconds	5.0 amps maximum
27-148F02	230 V 50 Hz	12 amps for 10 seconds	3.0 amps maximum
27-149F01	115 V 60 Hz	2.1 amps for 20 seconds	1.2 amps maximum
27-149F02	230 V 50 Hz	1.0 amps for 20 seconds	0.8 amps maximum

* See Tables 2-1 thru 2-21 in Section 2-2 for more information on these disk files supported by IDC.

2-7 APPLICATION OF AC POWER

Depending on how you strap the SEQ Pins 1 and 2 on the IDC board, you can apply power to the disk drives either simultaneously (in parallel) or sequentially (in serial). Section 2-7.1 describes simultaneous application of power, where the SEQ Pins are strapped or the Local/Remote Switch of each disk file is in the Local position. Section 2-7.2 describes sequential application of power, also referred to as power sequencing, where the SEQ Pins are not strapped and the Local/Remote Switch of each disk file is in the Remote position.

2-7.1 Simultaneous Application of Power

To apply power simultaneously to the disk files attached to your controller(s), follow this procedure:

1. Ensure correctness of all AC power-input connections.

2. At the front of each disk file, depress the START/STOP switch so it is unlit, i.e., so it is in the STOP position. (This step applies only to the removable-media disk systems.)

3. At the rear of each disk file, set the AC Input-Power switch to the OFF position.

4. Apply primary AC power.

5. At disk file 0, the first drive in the IDC system, set the AC Input-Power switch to the ON position. (At this time, a fixed-media disk would start up.)

6. Depress the START/STOP switch so it is lit, i.e., so it is in the START position. This disk file should now start up; the disk-media rotation should come up to speed. If the disk file does not start up, make these additional checks:

   a. Ensure that the Remote/Local switch in the disk drive is set to the Local position.

   b. Check AC input power.

   c. Check fuses in the disk drive.

7. Repeat steps 5 and 6 for remaining disk files. Consequently, the IDC disk files simultaneously come up to speed.

2-7.2 Power Sequencing

To apply power serially to the disk files attached to your controller(s), follow this procedure:

1. Ensure correctness of all AC power-input connections.

2. In each disk drive, set the Remote/Local switch to the Remote position.

3. Apply primary AC power.

4. At the rear of each disk file, ensure that the AC Input-Power switch is in the ON position.

5. At the front of each disk file, depress the START/STOP switch to the START position. (This step applies only to removable-media disk files.)

6. Power-up the processor in which the controller is connected. The disk files now start-up sequentially, starting with disk file 0.

2-8 IDC TESTING AND FORMATTING

Once your IDC system is installed and powered up, you can run the IDC Test Program to check for proper operation of your system. Follow this procedure:

1. Ensure you have an IDC-formatted media on your disk drive. If you do not, your disk must be formatted by loading and running the IDC Format Program, Publication Number 06-268. This program and appropriate instructions are supplied with your IDC disk system.

2. Load and run the IDC Test Program, Publication Number 06-267. This program and appropriate instructions are supplied with your IDC disk system.

C A U T I O N

OPTIMUM PERFORMANCE OF AN IDC DISK SYSTEM REQUIRES PROPERLY CERTIFIED DISK MEDIA. TO MINIMIZE THE EFFECTS OF LATENT DEFECTS, PERKIN-ELMER REMOVABLE DISK MEDIA HAVE BEEN CAREFULLY SCREENED AND CERTIFIED ON A CALIBRATED DISK DRIVE. THIS CERTIFICATION ASSURES TRANSPORTABILITY OF DISK MEDIA AND MINIMIZES THE OCCURRENCE OF DATA ERRORS.

THE 67-MB MSM, 256-MB MSM, AND MC-CDD DISK MEDIA (AVAILABLE ONLY FROM PERKIN-ELMER) ARE RECOMMENDED FOR THE HIGH-PERFORMANCE IDC DISK SYSTEMS.

COMPATIBLE DISK MEDIA MAY BE OBTAINED FROM A VENDOR AND CERTIFIED WITH THE IDC FORMAT PROGRAM, WITH ITS PARAMETERS SET UP EXACTLY AS SPECIFIED WITH THE SUPPLIED INSTRUCTIONS. HOWEVER, THE USER IS CAUTIONED THAT THESE MEDIA MAY RESULT IN REDUCED SYSTEM PERFORMANCE. SPECIFICALLY, DATA MAY NOT BE RECOVERABLE FROM THE MEDIA WHEN IT IS TRANSPORTED BETWEEN DRIVES. SUCH UNRECOVERABLE DATA COULD ALSO RESULT IN AN OPERATING SYSTEM CRASH. IN COMPARISON, A PERKIN-ELMER DISK DRIVE, DURING CERTIFICATION, CAN FLAG CERTAIN MEDIA DEFECTS THAT WOULD CAUSE A CRASH.

CHAPTER 3

THEORY OF OPERATION

3-1 BLACKBOX OVERVIEW OF IDC BOARD

By understanding the flow of external I/O signals associated with the IDC board, you will gain a general idea of what the IDC does. With this objective in mind, Section 3-1 treats the IDC as a blackbox circuit and presents an overview of all the I/O lines to and from the IDC connectors. Later sections discuss the internal operation of the IDC.

Refer to Figure 2-1 in Chapter 2. This figure illustrates the physical connections of an IDC board. Now refer to Figure 3-1 on the next page. This figure illustrates the I/O lines associated with the physical connectors, CONN 1 thru CONN 6, of the IDC board. The following sections briefly describe these I/O lines: Section 3-1.1 describes the lines from IDC CONN 1 to the SELCH or CM board plugged into the processor. Section 3-1.2 describes the A-cable lines between IDC connector CONN 2 and the attached disk files. Section 3-1.3 describes the B-cable lines between IDC connectors CONN 3 thru CONN 6 and the attached disk files.

NOTE

References in this chapter to the Selector Channel (SELCH) also apply to the Channel Manager (CM).

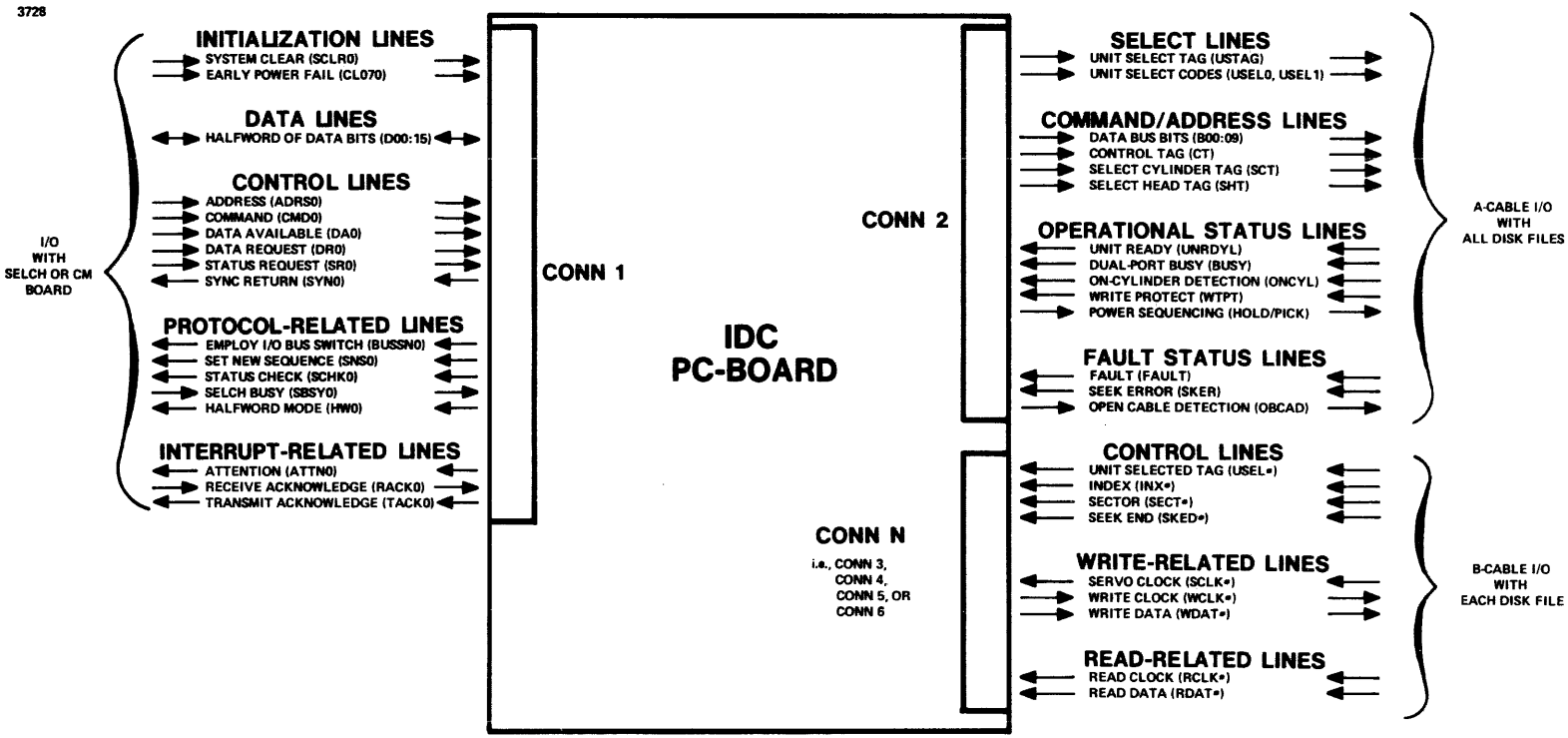


Figure 3-1. Blackbox Diagram of IDC Logic

3-1.1 I/O Lines at Connector CONN 1

See Figure 3-1. The I/O lines at CONN 1 are connected with the SELCH or CM board plugged into the same processor chassis with the IDC or installed under an I/O Bus Switch. These lines are classified here into five functional groups:

(1) Initialization Lines
(2) Data Lines
(3) Control Lines
(4) Protocol-Related Lines
(5) Interrupt-Related Lines

The following paragraphs, numbered (1) thru (5), describe the I/O lines within these groups.

(1) Initialization Lines

This group of lines initializes the IDC logic:

(a) System Clear (SCLR0)

Input from the processor to initialize IDC logic during a system power-up, shutdown, or initialization operation.

(b) Early Power Fail (CL070)

Input from the processor to warn the IDC of an imminent power failure.

(2) Data Lines

This group of sixteen I/O lines transfers data between the SELCH and the IDC board:

(a) Halfword Data Bits (D00:15)

SELCH or processor I/O consisting of a halfword or a byte of data. With halfword I/O, data bits D00:15 transfer the data for a read/write operation or the address for a disk cylinder or head. With byte I/O, D08:15 transfer an IDC or disk file address, a processor command, an IDC or disk file status, a sector address, or Rotational Position Sensing (RPS) data.

(3) Control Lines

This group consists of these I/O lines:

(a) Address (ADRS0)

Input from the processor to inform IDC that data bits D08:15 contain an IDC address or a disk file address. The addressed device is to be selected for subsequent I/O operation.

(b) Command (CMD0)

Input from the processor to inform IDC that data bits D08:15 contain a command for the selected device, i.e., the IDC or disk file.

(c) Data Available (DA0)

Input from the SELCH or processor to inform IDC that a halfword of data is available on D00:15 for a write operation to IDC.

(d) Data Request (DR0)

Input from the SELCH or processor that requests IDC for a halfword of data on D00:15 for a read operation from IDC.

(e) Status Request (SR0)

Input from the SELCH or the processor to request an IDC status or disk file status byte from data bits D08:15.

(f) Sync Return (SYN0)

IDC output signaling the SELCH or processor that the IDC has properly accepted and responded to a received control line signal.

(4) Protocol-Related Lines

This group of lines relates to the protocol exchanges between the SELCH and the IDC board:

(a) Employ I/O Bus Switch (BUSSW0)

IDC output informing the SELCH that the IDC employs the "new" high-speed SELCH protocol with an I/O Bus Switch.

(b) Set New Sequence (SNS0)

IDC output informing the SELCH that the IDC uses "new" high-speed SELCH protocol without an I/O Bus Switch.

(c) Status Check (SCHK0)

IDC output informing the SELCH of a bad IDC status. This output applies only when the IDC uses the high-speed SELCH protocol.

(d) SELCH Busy (SBSY0)

Input from the SELCH to inform IDC that the SELCH is currently busy with a block-data transfer.

(e) Halfword Mode (HW0)

IDC output informing the SELCH that this controller (IDC) is a halfword-oriented device.

(5) Interrupt-Related Lines

This group of lines relates to an interrupt request from the IDC board:

(a) Attention (ATN0)

IDC output requesting a processor interrupt, placing the IDC into an interrupt-pending state.

(b) Receive Acknowledge (RACK0)

Input from the processor to acknowledge an interrupt from an IDC; see item (a) above. If the IDC has no interrupt pending, it passes the RACK0 signal out as a TACK0 signal to the next IDC board stacked in the processor.

(c) Transmit Acknowledge (TACK0)

IDC output consisting of a RACK0 signal received by an IDC having no interrupt pending.

3-1.2 I/O Lines at Connector CONN 2

See Figure 3-1. The I/O lines at CONN 2 are through the A-cable to the attached disk files. These lines are classified here into four functional groups:

(1) Select Lines
(2) Command/Address Lines
(3) Operational Status Lines
(4) Fault Status Lines

The following paragraphs, numbered (1) thru (4), describe the I/O lines within these groups.

(1) Select Lines

This group of lines is involved with the selection of a disk file:

(a) Unit Select Tag (USTAG)

IDC output informing the attached disk files that the two Unit Select Lines (USEL0 and USEL1, described below) are supplying a binary-coded number, 0-3, to select a disk file.

(b) Unit Select Lines (USEL0, USEL1)

IDC output consisting of a binary-coded number, 0-3, to select a particular disk file for I/O with the IDC.

(2) Command/Address Lines

This group of lines supplies command and address data as control input to a selected disk file:

(a) Data Bus Bits (B00:09)

IDC output consisting of control or address data, e.g., a driver command, a cylinder address, or a head

address. The content of these lines depends on the three tags discussed in items (b), (c), and (d) below.

(b) Control Tag (CT)

IDC output indicating that B00:09 are supplying a driver command.

(c) Select-Cylinder Tag (SCT)

IDC output indicating that B00:09 are supplying a cylinder address.

(d) Select-Head Tag (SHT)

IDC output indicating that B00:09 are supplying head-select or volume-select data.

(3) Operational Status Lines

This group of lines supplies various operational statuses of a disk file:

(a) Unit Ready (UNRDYL)

Disk file output signaling IDC that the selected disk file is ready for I/O with the IDC.

(b) Dual-Port Busy (BUSY)

Disk file output applicable only to dual-port operation of a disk file. It informs IDC that the disk file is currently selected by another IDC.

(c) On-Cylinder Detection (ONCYL)

Disk file output that signals the IDC once the heads of the selected disk file are positioned over an addressed cylinder.

(d) Write Protect (WTPT)

Disk file output informing IDC that the write-protect button on the disk file is depressed, i.e., that the disk file is in the write-protect mode.

(e) Power Sequencing (HOLD/PICK)

IDC output of a ground signal that "picks and holds" power sequencing for the attached disk files in the remote mode. (This signal is present when the processor is on and IDC SEQ Pins 1 and 2 are not strapped.)

(4) Fault Status Lines

This group of lines supplies various fault statuses of a disk file.

(a) Fault (FAULT)

Disk file output informing IDC of a fault condition at a disk file.

(b) Seek Error (SKER)

Disk file output informing IDC of a seek error at a disk file.

(c) Open Cable Detection (OBCAD)

Disk file output informing IDC of an open cable or a loss of power. This signal prevents IDC from outputting select or control data to the disk file.

3-1.3 I/O Lines at Connectors CONN 3 thru CONN 6

See Figure 3-1. The I/O lines on any one of these connectors -- CONN 3, CONN 4, CONN 5, or CONN 6 -- are through a B-cable to a disk file. These lines are classified here into three functional groups:

(1) Control Lines
(2) Write-Related Lines
(3) Read-Related Lines

The following paragraphs, numbered (1) thru (3), describe the I/O lines within these groups.

(1) Control Lines

This group of lines passes various control signals to IDC in order to coordinate the transfer of read/write data. The # symbol with each mnemonic denotes one of four numbers, 0-3, for one of the four possible disk files.

(a) Unit Selected Tag (USEL#)

Disk file output signaling IDC that the disk file is now acquired, i.e., selected, by the IDC.

(b) Index (INX#)

Disk file output consisting of a pulse for every disk revolution. This pulse serves as an index for disk sector 0.

(c) Sector (SECT#)

Disk file output consisting of a pulse to mark the beginning of each physical sector of an IDC-formatted disk. (See Perkin-Elmer Publication 50-007 for a description of a physical sector.)

(d) Seek End (SKED#)

Disk file output signaling the end of a seek operation, either successful or unsuccessful.

(2) Write-Related Lines

This group of lines relates to write operations from the IDC to a disk file.

(a) Servo Clock (SCLK#)

Disk file output used by the IDC as input for the WCLK# signal; see (b) below.

(b) Write Clock (WCLK#)

IDC output that synchronizes data written to the disk file.

(c) Write Data (WDAT#)

IDC output consisting of data written to the disk file.

(3) Read-Related Lines

This group of lines relates to read operations from the disk file to the IDC:

(a) Read Clock (RCLK#)

Disk file output that synchronizes data read from the disk file.

(b) Read Data (RDAT#)

Disk file output consisting of data read from the disk file.

3-2 I/O LINES OF THE IDC BOARD

This section presents detailed descriptions of the same external I/O lines just overviewed in Section 3-1. Figure 3-2 shows the connectors of the IDC board and serves as a reference to other figures that illustrate the I/O lines attached to the connector pins. Sections 3-2.1 thru 3-2.3 describe these I/O lines.

NOTE

References in these descriptions to the Selector Channel (SELCH) also apply to the Channel Manager (CM).

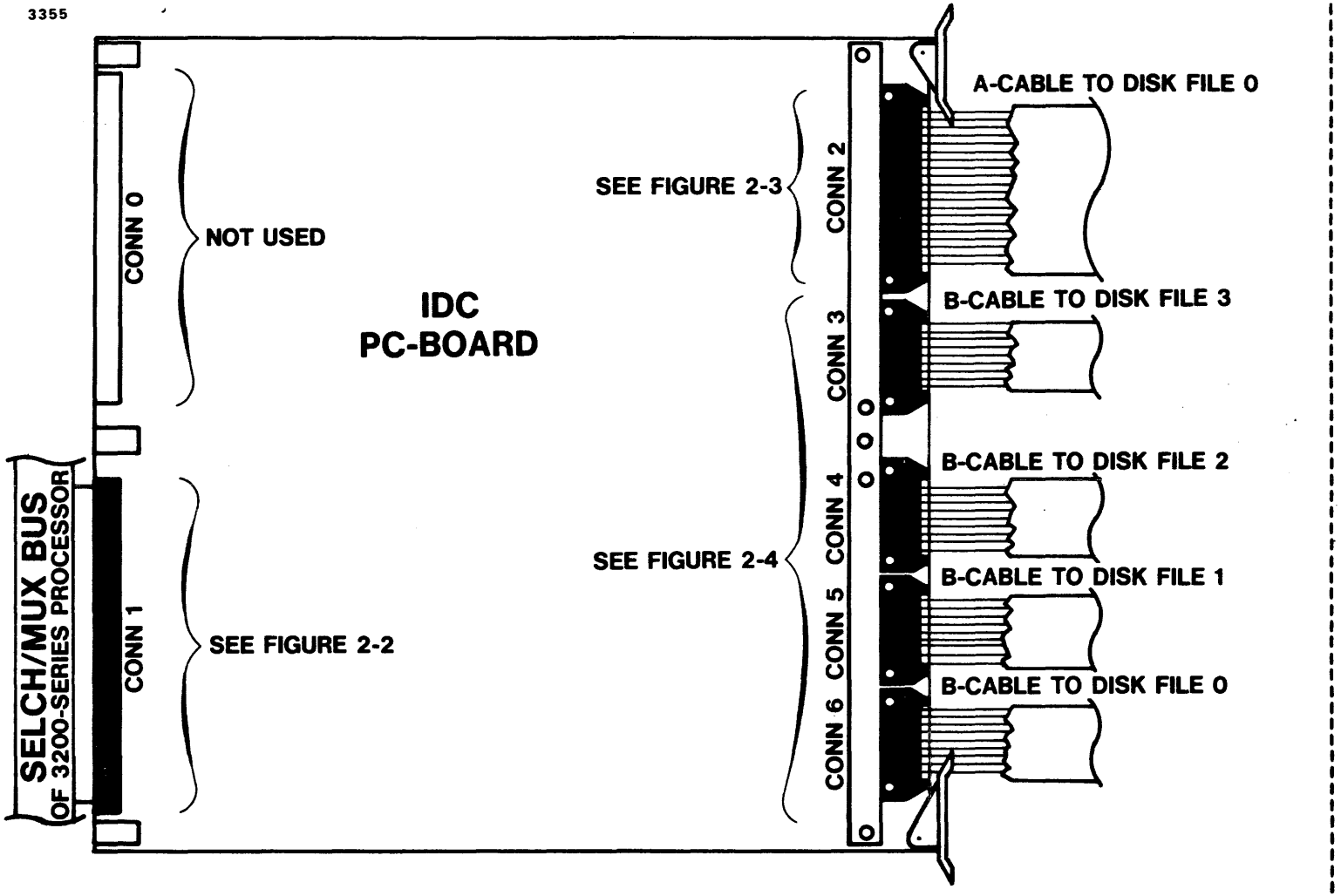


Figure 3-2. Connectors on IDC Board

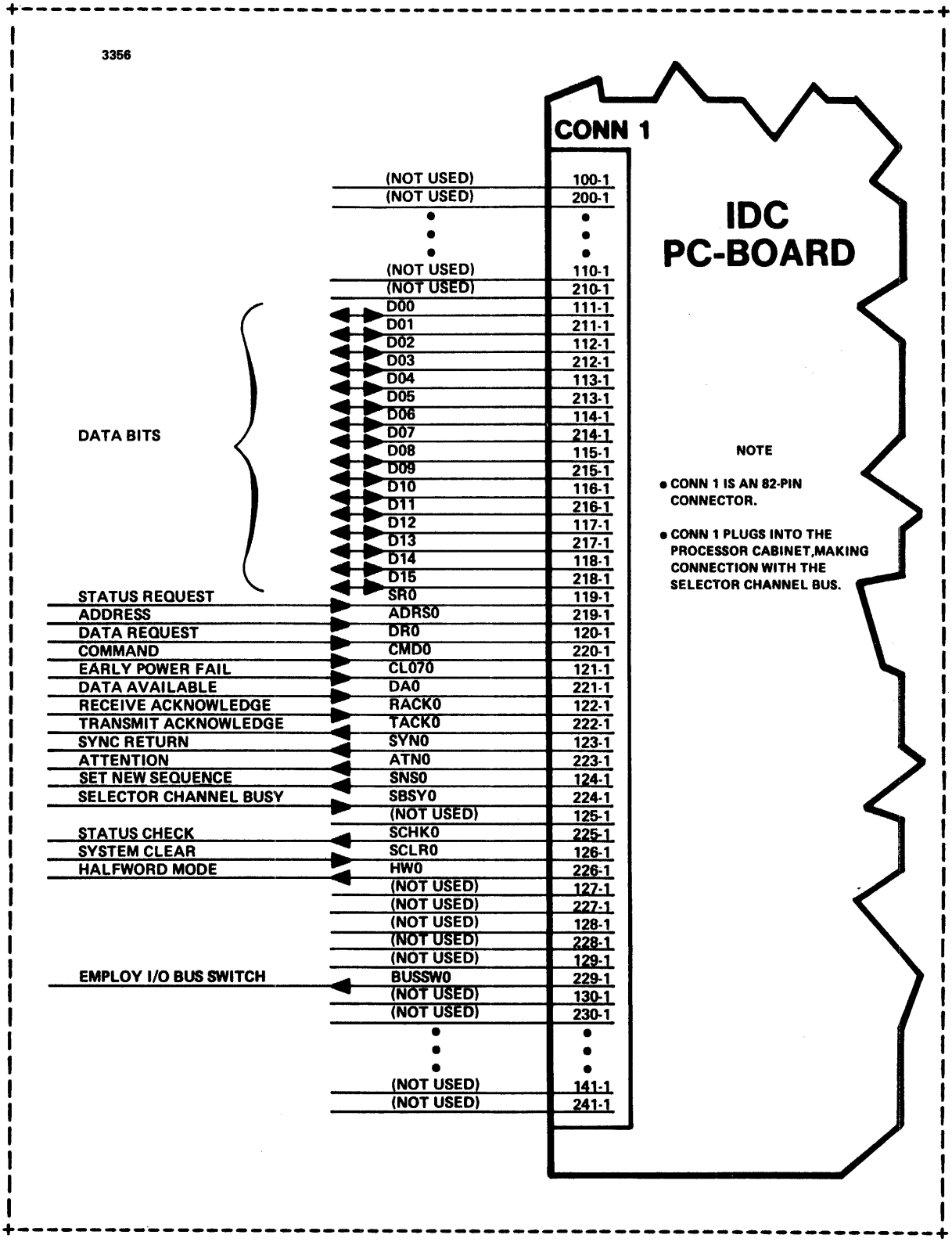


Figure 3-3. IDC CONN-1 Connections to SELCH/MUX Bus

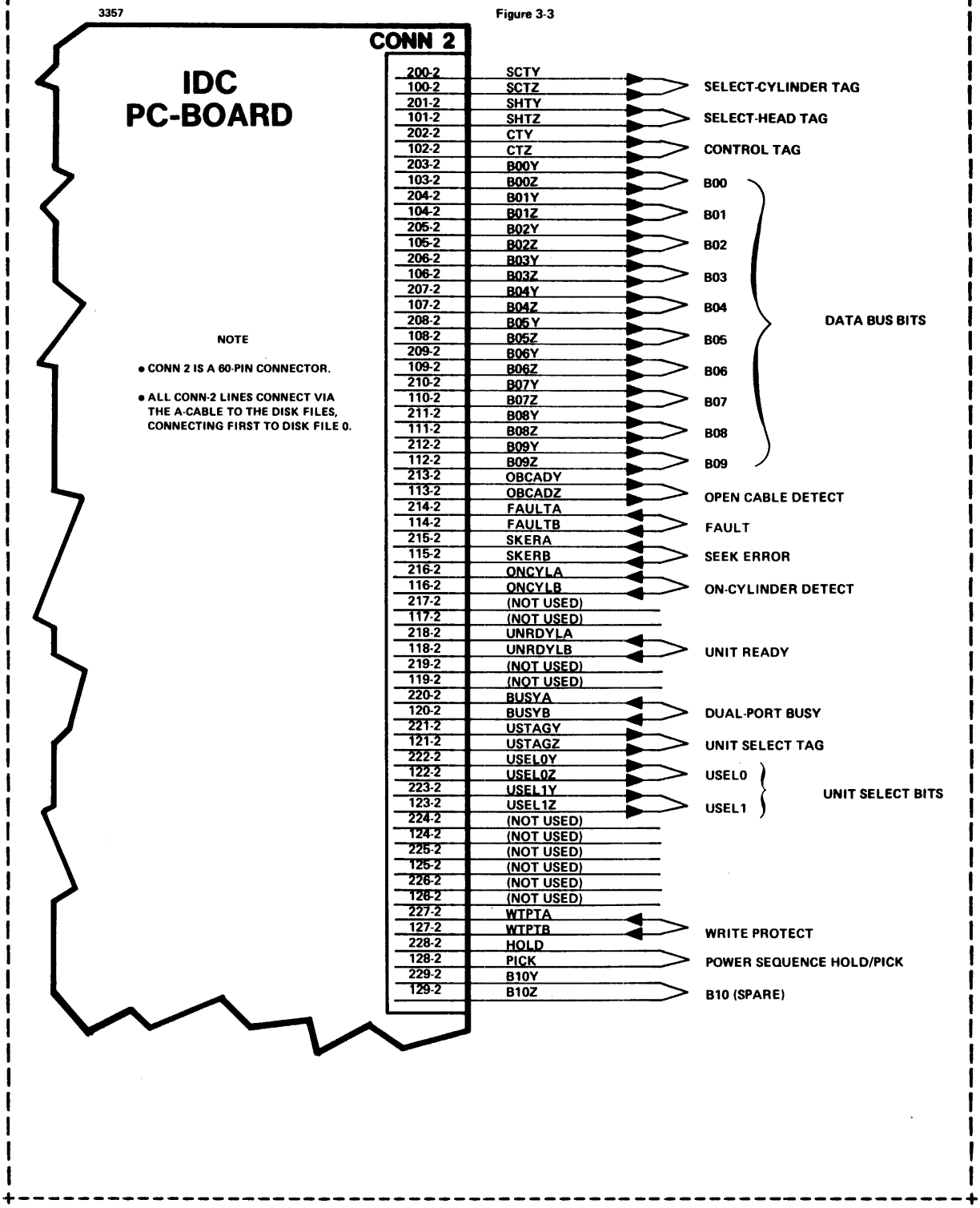


Figure 3-4. IDC CONN-2 Connections with A-Cable to Disk Files

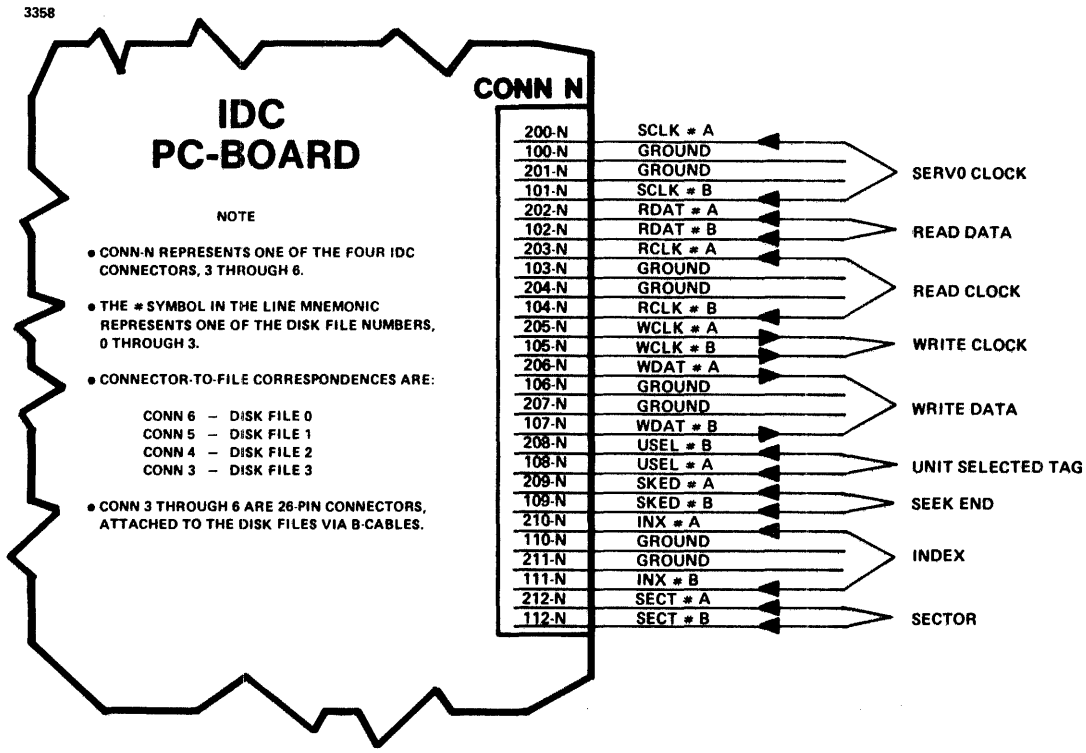


Figure 3-5. IDC CONN-3, CONN-4, CONN-5, and CONN-6 Connections with B-Cables to Disk Files

3-2.1 IDC Connector-1 Pins

Figure 3-3 illustrates and identifies all of the CONN-1 pins from the IDC board to the SELCH bus. The following paragraphs, presented alphabetically according to pin mnemonics, describe the inputs and outputs associated with these pins.

(a) ADRS0 (Address)

Input from the processor to IDC pin 219-1. When active, this signal informs the IDC that data bits D08 thru D15 contain the address of an IDC or a disk file. This address selects a particular device for a subsequent operation, e.g., a read/write or a status request. ADRS0 must result in device selection before any one of these signals, described below, can have effect: CMD0, DA0, DR0, and SR0.

(b) ATN0 (Attention)

Output from IDC pin 223-1 to the processor. When active, this signal indicates that the IDC needs to interrupt the processor. The IDC sends this signal after completing an operation, and consequently has an interrupt pending.

(c) BUSSW0 (Employ I/O Bus Switch)

Output from IDC pin 229-1. When active, this signal informs the SELCH that this IDC supports the "new" high-speed SELCH protocol and employs an I/O Bus Switch.

NOTE

This signal can be active only if these conditions are met: New-Protocol Pins W1 and W3 are strapped; toggle-7 of the File-0 Address Switch is pushed down to the 1-setting; and the IDC is installed under an I/O Bus Switch.

(d) CL070 (Early Power Fail)

Input from the processor to IDC pin 121-1. When active, this signal serves as a warning that a power failure is imminent.

(e) CMDO (Command)

Input from the processor to IDC pin 220-1. When active, this signal informs the IDC that data bits D08 thru D15 contain a command for the selected IDC or disk file. Perkin-Elmer Publication 50-007 discusses these commands.

(f) DAO (Data Available)

Input from the processor or SELCH to IDC pin 221-1. When active, this signal informs the IDC of a write operation to the selected IDC or disk file. Data is available on IDC bits D00 thru D15.

(g) DRO (Data Request)

Input from the processor or SELCH to IDC pin 120-1. When active, this signal informs the IDC of a read operation from the selected IDC or disk file to the processor. A halfword of data is read from IDC bits D00 thru D15.

(h) D00 thru D15 (Data Bits 0 thru 15)

Input/output data on IDC pins 111-1 thru 118-1 and 211-1 thru 218-1. For halfword I/O, bits D00 thru D15 hold read/write data; these bits can also hold a cylinder or head address as input from the processor. For byte I/O, bits D08 thru D15 can hold one of the following: processor command, IDC address, IDC status, disk file address, disk file status, sector address, and Rotational Position Sensing (RPS) data.

(i) HWO (Halfword Mode)

Output from IDC pin 226-1 to the SELCH. When active, this signal informs the SELCH that this IDC is a halfword-oriented device.

(j) RACKO (Receive Acknowledge)

Input from the processor to IDC pin 122-1. When active, this input indicates an interrupt acknowledgment from the processor. Whenever an IDC sends an ATNO signal, thereby requesting a processor interrupt, that IDC then has an interrupt pending. The RACKO input acknowledges this interrupt request. If a RACKO is received at an IDC having no interrupt pending, that IDC passes this RACKO as a TACKO (see its description) to the next IDC in the processor cabinet. That IDC then receives the TACKO as a RACKO.

In summary, the RACK0 is a daisy-chained interrupt acknowledgment from the processor to an IDC with an interrupt pending.

(k) SBSY0 (SELCH Busy)

Input from the SELCH to IDC pin 224-1. When active, this signal indicates that a block-data transfer to or from the SELCH is in progress.

(l) SCHK0 (Status Check)

Output, applicable only for the high-speed SELCH protocol, from IDC pin 225-1 to the SELCH. When active, this signal indicates the occurrence of a bad IDC status: EXAMINE, CONTROLLER IDLE, or DATA ERROR. For information on these statuses, refer to Perkin-Elmer Publication 50-007.

(m) SCLR0 (System Clear)

Input from the processor to IDC pin 126-1. When active, this signal causes the initialization of IDC logic. It is active during system power-up, shutdown, and initialization.

(n) SNS0 (Set New Sequence)

Output from IDC pin 124-1 to the SELCH. When active, this signal informs the SELCH that this IDC supports the "new" high-speed SELCH protocol without an I/O Bus Switch.

NOTE

This signal can be active only if these conditions are met: the IDC is installed under an I/O Bus Switch; New-Protocol Pins W1 and W2 are strapped; and toggle-7 of the File-0 Address Switch is pushed down to the 1-setting. Employing the high-speed protocol by strapping W1 and W2, however, is not a recommended procedure. Standard procedure is to strap W1 and W3 and to employ an I/O Bus Switch; see item (c) above.

(o) SR0 (Status Request)

Input signal from the processor or SELCH to IDC pin 119-1. When active, this signal requests the current status of the IDC or an attached disk file. The requested status is

passed as one byte of data, bits D08 thru D15. Perkin-Elmer Publication 50-007 discusses these statuses.

(p) SYN0 (Sync Return)

Output from IDC pin 123-1 to the processor or SELCH. When active, this signal informs the processor or SELCH that this IDC has properly accepted and responded to a control line signal.

(q) TACK0 (Transmit Acknowledge)

Output from IDC pin 222-1 to the next controller plugged into the I/O slot. This output, consisting of a received RACK0, indicates that this IDC did not have an interrupt pending. See the description above for the RACK0 input.

3-2.2 IDC Connector-2 Pins

Figure 3-4 illustrates and identifies all of the CONN-2 pins and A-cable lines from the IDC board to the disk files. The following paragraphs, presented alphabetically according to the line mnemonics, describe the inputs and outputs associated with the A-cable lines.

(a) B00Y (Differential Data Bus Bit 0 +) and
B00Z (Differential Data Bus Bit 0 -)
thru
B09Y (Differential Data Bus Bit 9 +) and
B09Z (Differential Data Bus Bit 9 -)

Ten output lines, subsequently referred to as B00 thru B09, from IDC pins 203-2 and 103-2 (for B00) thru pins 212-2 and 112-2 (for B09) to the disk files. These multipurpose bus lines supply control and address data to the attached disk files. The actual content of B00 thru B09 depends on one of three tags:

(1) CTY/CTZ (Differential Control Tag +/-)

(2) SCTY/SCTZ (Differential Select-Cylinder Tag +/-)

(3) SHTY/SHTZ (Differential Select-Head Tag +/-)

As shown in Table 3-1 below, B00 thru B09 can supply a control function, a cylinder address, or a head address depending on which of the three tags is active. For further information on bus line contents, refer to the subsequent tag descriptions.

Table 3-1. Bus Line Contents Corresponding to Active Output Tag

BUS LINE	CONTROL* FUNCTION	CYLINDER** ADDRESS	HEAD*** ADDRESS
B00	Write Gate	1	1
B01	Read Gate	2	2
B02	Servo Offset +	4	4
B03	Servo Offset -	8	8
B04	Fault Clear	16	16
B05	(Not Applicable)	32	N/A
B06	Return to Zero (RTZ)	64	N/A
B07	Data Strobe Early	128	N/A
B08	Data Strobe Late	256	N/A
B09	Release (Dual-Port Operation)	512	N/A

* Applies when CTY/CTZ tag is active.
** Applies when SCTY/SCTZ tag is active.
*** Applies when SHTY/SHTZ tag is active.

(b) B10Y (Differential Data Bus Bit-10 +) and
B10Z (Differential Data Bus Bit-10 -)

This is a spare differential data bus line.

(c) BUSYA (Differential Dual-Port Busy +) and
BUSYB (Differential Dual-Port Busy -)

Input from a disk file to IDC pins 220-2 and 120-2, applicable only to dual-port operation of a particular disk file. When active, this line indicates to the IDC that the selected disk file has been acquired by another IDC.

(d) CTY (Differential Control Tag +) and
CTZ (Differential Control Tag -)

Output from IDC pins 202-1 and 102-2 to the disk files. When active, this input tag informs the disk files that bus lines B00 thru B09 are supplying a binary-coded control function (i.e., a disk driver command). Table 3-2 below lists and describes the control functions corresponding to the settings of these ten bus lines.

Table 3-2. Control Functions Activated by Control Tag CTY/CTZ

BUS* LINE	CONTROL FUNCTION	DESCRIPTION
B00	Write Gate	Informs the selected disk drive (selected by USEL0 and USEL1 on the A-cable) that the IDC will write data over the Write Data line of the B-cable to the current location of the disk medium.
B01	Read Gate	Informs the selected disk drive that the IDC will read data over the Read Data line of the B-cable from the current location of the disk medium.
B02	Servo Offset +	Offsets the head of the selected disk file in a positive direction, i.e., towards the spindle of the disk drive.
B03	Servo Offset -	Offsets the head of the selected disk file in a negative direction, i.e., away from spindle.
B04	Fault Clear	Clears the fault condition that resulted from a DC power failure, a simultaneously active Read Gate and Write Gate, or a selection of a nonexistent head. (See the description for the FAULTA/FAULTB line.)
B05	------	Not applicable. Must equal zero.
B06	Return to Zero	Restores the selected disk file to cylinder 000.
B07	Data Strobe Early	Causes the disk file to advance the Read Clock in order to retrieve marginal data.
B08	Date Strobe Late	Causes the disk file to retard the Read Clock in order to retrieve marginal data.
B09	Release	Releases a dual-port operational disk file so another processor can access it.

* These ten lines are read as a binary number with B00 representing 2 to the 0 power, B01 representing 2 to the 1st power, B02 representing 2 to the 2nd power, and so forth.

(e) FAULTA (Differential Fault +) and
FAULTB (Differential Fault -)

Input from a disk file to IDC pins 214-2 and 114-2. When active, this line indicates a fault condition at a disk file.

(f) HOLD/PICK (Power Sequence Hold/Pick)

A power sequencing ground provided by IDC logic from pins 228-2 and 128-2 to attached disk files. If SEQ Pins 1 and 2 are not strapped and if attached disk files have their Local/Remote switch in the Remote position, the IDC logic switches a ground onto these lines to permit power sequencing once the processor is turned on. When the processor is turned off, IDC logic removes the ground to power-down the disk files. Essentially, then, these lines "pick and hold" the power sequencing capability.

(g) OBCADY (Differential Open Cable Detection +) and
OBCADZ (Differential Open Cable Detection -)

Output from IDC pins 213-2 and 113-2 to a disk file. When active, this line indicates an open A-cable or a loss of IDC power. While this condition exists, no selection or control data will be sent from the IDC.

(h) ONCYLA (Differential On-Cylinder Detection +) and
ONCYLB (Differential On-Cylinder Detection -)

Input status from a disk file to IDC pins 216-2 and 116-2. When active, this line signals the IDC that the heads of the selected disk file are positioned; i.e., in response to a Seek instruction, they are positioned over a selected track. The on-cylinder status clears with another Seek instruction, and again becomes active once the heads are positioned. A carriage offset results in the loss of the on-cylinder status for 2.75 milliseconds (nominal); i.e., about 2.75 ms are required to move the head to a + or - offset.

(i) SCTY (Differential Select-Cylinder Tag +) and
SCTZ (Differential Select-Cylinder Tag -)

Output from IDC pins 200-2 and 100-2 to the disk files. When active, this output tag informs the disk file that the ten bus lines, B00 thru B09, are supplying a binary-coded cylinder address. B00 represents 2 to the 0 power, B01 represents 2 to the 1st power, etc.

(j) SHTY (Differential Select-Head Tag) and
SHTZ (Differential Select-Head Tag)

Output from IDC pins 201-2 and 101-2 to the disk files. When active, this output tag informs the disk file that B00 thru B09 are supplying head-select or volume-select data.

For an MSM file, bus lines B00 thru B04 supply head-select data, where B00 represents 2 to the 0 power, B01 represents 2 to the 1st power, etc. See Table 3-1 for further illustration.

For an MC-CDD, however, bit B04 represents a volume select bit; B00 thru B03 are nonapplicable. B04, which represents 2 to the 4th power, supplies part of the data for a volume-select address: when reset, it denotes a removable disk; when set, it denotes a fixed disk. The remainder of the volume-select address is supplied by another input, a cylinder address, on B00 thru B09. This input is associated with the select-cylinder tag SCTY/SCTZ. In summary, then, supplying a volume-select address to an MC-CDD requires two tag sequences:

(1) An active SHTY/SHTZ tag with bus line B04 set or reset.

(2) An active SCTY/SCTZ tag with bus lines B00 thru B09 containing a valid cylinder address. (The worst-case switching delay is 4 milliseconds.)

(k) SKERA (Differential Seek Error +) and
SKERB (Differential Seek Error -)

Input from a disk file to IDC pins 215-2 and 115-2. When active, this line indicates that a seek error occured at a disk file. A seek error refers to one of these three conditions:

(1) The disk drive could not move the head within a specified time interval.

(2) The disk drive moved the head to a position outside the recording area of the disk.

(3) The disk drive received an illegal track address.

A seek error can be cleared only by an RTZ control function.

(l) UNRDYLA (Differential Unit Ready +) and
UNDRYLB (Differential Unit Ready -)

Input from a disk file to IDC pins 218-2 and 118-2. When active, this line indicates that the selected disk file is up-to-speed, that the heads are positioned over the recording tracks, and that no fault condition exists within the disk file.

(m) USEL0Y (Differential Unit Select 0 +),
USEL0Z (Differential Unit Select 0 -),
USEL1Y (Differential Unit Select 1 +), and
USEL1Z (Differential Unit Select 1 -)

Two output lines, subsequently referred to as USEL0 and USEL1, from IDC pins 222-2 and 122-2 (for USEL0) and pins 223-2 and 123-2 (for USEL1). These binary-coded lines supply a number, 0 thru 3, of the disk file to be selected. USEL0 represents 2 to the 0 power; USEL1 represents 2 to the 1st power.

(n) USTAGY (Differential Unit Select Tag +) and
USTAGZ (Differential Unit Select Tag -)

Output from IDC pins 221-2 and 121-2 to the disk files. When active, this output tag informs the disk files that the two unit-select lines, USEL0 and USEL1, are supplying a binary-coded number, as mentioned above.

(o) WTPTA (Differential Write Protect +) and
WTPTB (Differential Write Protect -)

Input from a disk file to IDC pins 227-2 and 127-2. When active, this line indicates that the particular disk file is in write-protected mode: a write-protect button on the disk file has been depressed.

3-2.3 IDC Connector-3 thru Connector-6 Pins

Figure 3-5 illustrates and identifies all of the pins and B-cable lines from these IDC connectors: CONN 3, CONN 4, CONN 5, and CONN 6. The following paragraphs, presented alphabetically according to line mnemonics, describe the inputs and outputs associated with the lines. These descriptions, which apply to all four connectors, use the letter N to represent the connector numbers (3, 4, 5, or 6) and the symbol # to represent the disk file number (0, 1, 2, or 3).

(a) INX#A (Differential Index +) and
INX#B (Differential Index -)

Input from disk file # to IDC pins 210-N and 111-N. This line receives a pulse for every disk revolution. The leading edge of the pulse is treated as the leading edge of sector 0. Pulse width is typically 2.5 microseconds.

(b) RCLK#A (Differential Read Clock +) and
RCLK#B (Differential Read Block -)

Input from disk file # to IDC pins 203-N and 104-N. The IDC uses this input to clock-in, or synchronize, data read from disk file #.

(c) RDAT#A (Differential Read Data +) and
RDAT#B (Differential Read Data -)

Input from disk file # to IDC pins 202-N and 102-N. This line carries read data from disk file #. Read data is in Non-Return to Zero (NRZ) form.

(d) SCLK#A (Differential Servo Clock +) and
SCLK#B (Differential Servo Clock -)

Input from disk file # to controler pins 200-N and 101-N. The IDC uses this input as the write clock; see WCLK#A/WCLK#B below.

(e) SECT#A (Differential Sector +) and
SECT#B (Differential Sector -)

Input from disk file # to IDC pins 212-N and 112-N. This input pulse marks the beginning of each physical sector of the IDC-formatted disk. (There are 33 physical sectors per disk revolution.)

(f) SKED#A (Differential Seek End +) and
SKED#B (Differential Seek End -)

Input from disk file # to IDC pins 209-N and 109-N. This input line is a combination of the On-Cylinder Detect line (ONCYLA/ONCYLB) and the Seek Error line (SKERA/SKERB). These two lines connect through the A-cable to IDC CONN 2. It indicates to the IDC that a seek operation has ended, either successfully or unsuccessfully.

(g) USEL#A (Differential Unit Selected Tag +) and
USEL#B (Differential Unit Selected Tag -)

Input from disk file # to IDC pins 108-N and 208-N. It indicates that the attached disk file is now acquired by the IDC; i.e., the disk has been selected.

(h) WCLK#A (Differential Write Clock +) and
WCLK#B (Differential Write Clock -)

Output from IDC pins 205-N and 105-N to disk file #. The IDC uses this output to clock-out, or synchronize, data written to the disk file.

(i) WDAT#A (Differential Write Data +) and
WDAT#B (Differential Write Data -)

Output from IDC pins 206-N and 107-N to disk file #. This line carries write data to be recorded on the disk. Written data is in NRZ form.

3-3 BLOCK-DIAGRAM ANALYSIS OF IDC

The foldout Figure 3-6 is a block diagram of the IDC logic circuitry. As shown, this block diagram has three logical sections:

(1) SELCH/MUX Bus Interface
(2) Disk File Interface
(3) Microprocessor Controller Logic

Section 3-3.1 describes the constituent blocks for the SELCH/MUX bus interface; Section 3-3.2, the microprocessor controller logic; and Section 3-3.2, the disk file interface.

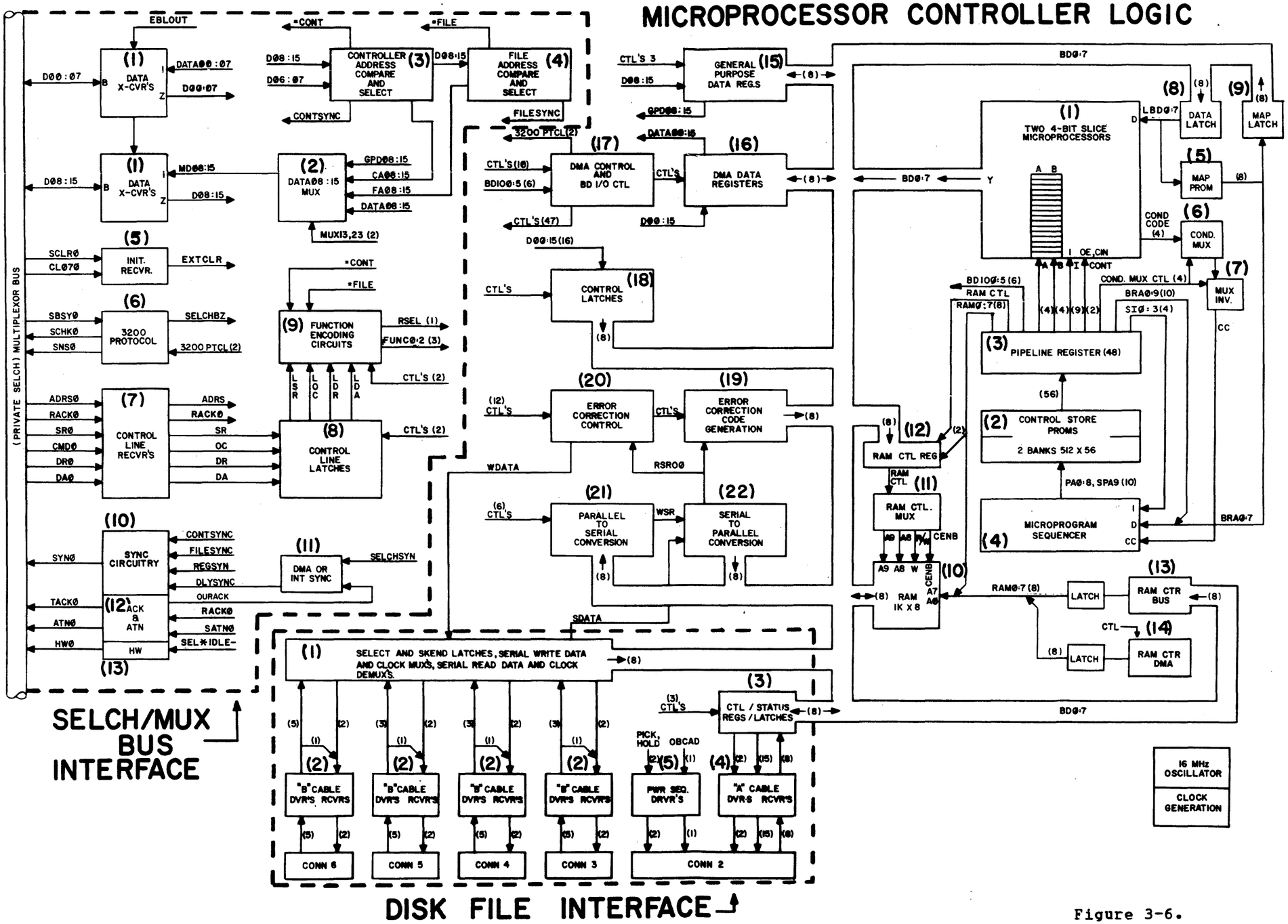


Figure 3-6.

Block Diagram of the IDC Logic

3-3.1 SELCH/MUX Bus Interface

This portion of the IDC board serves as the interface to the SELCH/MUX bus. It consists of thirteen functional blocks:

(1) Data Transceivers
(2) Data Multiplexer for Bits 08:15
(3) Controller Address Compare-and-Select Circuitry
(4) File Address Compare-and-Select Circuitry
(5) Initialization Receiver
(6) 3200-Protocol Circuitry
(7) Control Line Receivers
(8) Control Line Latches
(9) Function Encoding Circuits
(10) Synchronization Circuitry
(11) DMA and Interrupt Sync Circuits
(12) Acknowledgment and Attention Circuitry
(13) Halfword-Mode Circuitry

The following paragraphs describe these functional blocks and their associated I/O lines.

(1) Data Transceivers

Transmit data to or receive data from the SELCH/MUX bus. I/O lines are:

(a) EBLOUT (Driver Control), Input

Signal for setting the transceiver mode to transmit or receive.

(b) D00:15 (Data Bits D00 thru D15), Input/Output

Data to or from the SELCH/MUX bus. See Section 3-2.1 for a more complete description.

(c) DATA00:07 (Data Bits 00 thru 07), Input

More significant byte of Direct Memory Access (DMA) data to be transmitted to the SELCH.

(d) MD08:15 (Multiplexed Data Bits 08 thru 15), Input

One of four multiplexed data sources to be sent to the SELCH or processor.

(e) D00:07 (Receive Data Bits 00 thru 07), Output

More significant byte of data received from the SELCH/MUX bus, i.e., from the processor or SELCH.

(f) D08:15 (Receive Data Bits 08 thru 15), Output

Less significant byte of data received from the SELCH/MUX bus, i.e., from the processor or SELCH.

(2) Data Multiplexer for Bits 08:15

Selects one of four data sources as MD08:15 input to the Data Transceivers. I/O lines are:

(a) MUX13,23 (Multiplexer Control Bits), Input

Binary value for selecting one of the following four data-source inputs.

(b) GPD08:15 (General-Purpose Data), Input

General-purpose control data like status, Rotational Position Sensing (RPS), etc., to be sent as MD08:15 input to the Data Transceivers.

(c) CA08:15 (Controller-Address Bits 08 thru 15), Input

IDC address (of this controller) to be sent as MD08:15 input to the Data Transceivers.

(d) FA08:15 (File-Address Bits 08 thru 15), Input

File address (of a disk file attached to this controller) to be sent as MD08:15 input to the Data Transceivers.

(e) DATA08:15 (Data Bits 08 thru 15), Input

Less significant byte of DMA data to be transmitted, via the Data Transceivers, to the SELCH.

(f) MD08:15 (Multiplexed Data Bits 08 thru 15), Output

One of four multiplexed data sources to be sent to the SELCH or processor.

(3) Controller Address Compare-and-Select Circuitry

Detects when this IDC is addressed by the processor. More specifically, this circuitry compares a received controller address with the address of this IDC; if the two addresses match, then this IDC is selected for I/O with the processor via the SELCH/MUX bus. (The IDC address is determined by the setting of the Controller Address Switch on the IDC board, discussed in Section 2-4.1.) I/O lines are:

(a) D08:15 (Receive Data Bits 08 thru 15), Input

Controller address received from the processor.

(b) D06:07 (Receive Data Bits 06 and 07), Input

Controller address bits appended to D08:15 for a full 10-bit address selection. These two bits must equal zero for address comparison to occur.

(c) =CONT (Equals Controller), Output

Signal for indicating that the received controller address matches the address of this IDC.

(d) CONTSYNC (Controller Sync Return), Output

A sync signal indicating that the IDC has properly accepted and responded to control line signals.

(e) CA08:15 (Controller-Address Bits 08 thru 15), Output

IDC address (of this controller) to be sent to the processor, along with the sync signal SYN0.

(4) File Address Compare-and-Select Circuitry

Detects when an attached disk file is addressed by the processor. More specifically, this circuitry compares a received disk file address with the addresses of the disk files attached to this IDC; if there is a match, then the

addressed disk file is selected for I/O with the processor via the SELCH/MUX bus. (Disk file addresses are determined by the setting of the File-0 Address Switch on the IDC board, discussed in Section 2-4.1.) I/O lines are:

(a) DO8:15 (Receive Data Bits 08 thru 15), Input

Disk file address received from the processor.

(b) =FILE (Equals File), Output

Signal for indicating that the received file address matches the address of a disk file at this IDC.

(c) FILESYNC (File Sync Return), Output

A sync signal indicating that an attached disk file has properly accepted and responded to control line signals.

(d) FA08:15 (File Address Bits 08 thru 15), Output

File address (of the selected disk file) to be sent to the processor, along with the sync signal SYN0.

(5) Initialization Receiver

Initializes IDC logic to permit controller comunication with the 3200-Series processor, or to prepare the IDC logic for an imminent power failure. I/O lines are:

(a) SCLR0 (System Clear), Input

Signal from the processor for initializing IDC circuitry. See Section 3-2.1 for more information.

(b) CL070 (Early Power Fail), Input

Signal from the processor as a warning that a power failure is about to occur. See Section 3-2.1.

(c) EXTCLR (External Clear), Output

Signal for initializing the IDC logic.

(6) 3200-Protocol Circuitry

Enables the IDC to employ the "new" high-speed SELCH protocol. This protocol applies only when the New-Protocol Pins W1 and W3 or W1 and W2 are strapped. I/O lines are:

(a) SBSY0 (SELCH Busy), Input

Signal for indicating that the SELCH is currently busy with a block-data transfer. See Section 3-2.1 for further description.

(b) SELCHBZ (SELCH Busy), Output

Same description as above with SBSY0.

(c) 3200 PTCL (3200 Protocol), Input

Data indicating the occurrence of a bad IDC status, namely: S13, EXAMINE; S14, CONTROLLER IDLE; or S15, DATA ERROR. The indicated status results from bits 13, 14, and 15 of a status register within the Random Access Memory (RAM) circuitry. Refer to Perkin-Elmer Publication 50-007 for further description. (Physically, 3200 PTCL represents two lines: STCHK and CTLOPTC. Refer to Appendix A for further description.)

(d) SCHK0 (Status Check), Output

Output to SELCH to indicate a bad IDC status associated with the high-speed SELCH protocol. See item (c) above. Refer to Section 3-2.1 for more information.

(e) SNS0 (Set New Sequence), Output

Signal for indicating that the controller is set-up for the optional "new" high-speed SELCH protocol. This signal results when toggle-7 of the File-0 Address Switch is pushed down to the 1-setting, and when the New-Protocol Pins W1 and W2 are strapped. See Sections 2-4.1 and 2-4.2 for detailed information.

(7) Control Line Receivers

Receive control signals from the SELCH/MUX bus. I/O lines are:

(a) ADRS0 (Address), Input

Signal indicating that D08:15 (input lines to the Data Transceivers) contain the address of an IDC or disk file. This signal must result in device selection at the IDC before any one of these signals, described below, can have effect: SR0, CMD0, DR0, and DA0. See Section 3-2.1 for more information.

(b) ADRS (Address), Output

Same description as above with ADRS0.

(c) RACK0 (Receive Acknowledgment), Input

Signal acknowledging that the processor received an ATN0 from an IDC with an interrupt pending, possibly this one. In effect, RACK0 acknowledges an interrupt request signaled by the ATN0 signal. See Section 3-2.1 for a more complete description.

(d) RACK0 (Receive Acknowledgment), Output

Same description as above. If the IDC does not have an interrupt pending, RACK0 is passed as TACK0 output to the next IDC in the I/O slot of the processor cabinet. See paragraph (12) below for further description.

(e) SR0 (Status Request), Input

Signal for requesting the status of a selected IDC or disk file. See Section 3-2.1 for further description.

(f) SR (Status Request), Output

Same description as above with SR0.

(g) CMD0 (Command), Input

Signal indicating that input lines D08:15 contain a command for this selected IDC or for a selected disk file. See Section 3-2.1 for further description.

(h) OC (Output Command), Output

Same description as above with CMD0.

(i) DR0 (Data Request), Input

Signal indicating a read operation from output lines D00:15. See Section 3-2.1 for further description.

(j) DR (Data Request), Output

Same description as above with DR0.

(k) DA0 (Data Available), Input

Signal indicating a write operation from the processor to input lines D00:15. See Section 3-2.1 for further description.

(l) DA (Data Available), Output

Same description as above with DA0.

(8) Control Line Latches

Temporarily store (i.e., latch) control inputs for later use by the IDC microprocessor logic. I/O lines are:

(a) CTL'S (Control Lines), Input

Binary-coded control lines to enable or disable latching of the four control inputs SR, OC, DR, and DA.

(b) SR (Status Request), Input

Control input resulting from a received SR0 signal.

(c) LSR (Latched Status Request), Output

Latch signal corresponding to the above SR input.

(d) OC (Output Command), Input

Control input resulting from a received CMD0 signal.

(e) LOC (Latched Output Command), Output

Latch signal corresponding to the above OC input.

(f) DR (Data Request), Input

Control input resulting from a received DR0 signal.

(g) LDR (Latched Data Request), Output

Latch signal corresponding to the above DR input.

(h) DA (Data Available), Input

Control input resulting from a received DA0 signal.

(i) LDA (Latched Data Available), Output

Latch signal corresponding to the above DA input.

(9) Function Encoding Circuits

Encodes the latched control lines (LSR, LOC, LDR, and LDA) into a 3-bit code for a selected IDC or disk file. I/O lines are:

(a) LSR (Latched Status Request), Input

Latch signal corresponding to the SR0 input from the SELCH/MUX bus.

(b) LOC (Latched Output Command), Input

Latch signal corresponding to the CMD0 input from the SELCH/MUX bus.

(c) LDR (Latched Data Request), Input

Latch signal corresponding to the DR0 input from the SELCH/MUX bus.

(d) LDA (Latched Data Available), Input

Latch signal corresponding to the DA0 input from the SELCH/MUX bus.

(e) FUNC0:2 (Function Code), Output

Binary-coded signal representing one of eight possible functions. This output goes onto the microprocessor bus, BD0:7, when RSEL is also active. Refer to Appendix A for further description.

(f) RSEL (Register Select), Output

Signal indicating that the encoded FUNC0:2 bits are now active.

(g) CTL'S (Control Lines), Input

Control lines to gate the FUNC0:2 bits onto BD0:7.

(h) =CONT (Equals Controller), Input

Signal for indicating that the FUNC0:2 bits apply to this selected IDC.

(i) =FILE (Equals File), Input

Signal for indicating that the FUNC0:2 bits apply to a selected disk file.

(10) Synchronization Circuitry

Receives synchronization signals from the IDC logic and ouputs a synchronization signal to the processor or SELCH. I/O lines are:

(a) CONTSYNC (Controller Sync Return), Input

Sync signal indicating that this IDC has properly accepted and responded to a control line signal.

(b) FILESYNC (File Sync Return), Input

Sync signal indicating that a selected disk file attached to this IDC has properly accepted and responded to a control line signal.

(c) REGSYN (Register Sync), Input

Sync signal indicating that the IDC received one of the four control functions -- SR0, CMD0, DR0, or DA0. See paragraph (7) above for more information.

(d) DLYSYNC (Delayed Sync Return), Input

Either the DMA sync signal to the SELCH (resulting from SELCHSYN) or the interrupt-acknowledgment sync signal (resulting from OURACK0) to the processor. See paragraph (11) below for further description.

(e) SYN0 (Sync Return), Output

Sync signal informing the processor or SELCH that this IDC or an attached disk file has properly accepted and responded to control line signals. See the corresponding description in Section 3-2.1.

(11) DMA and Interrupt Sync Circuits

Outputs a delayed sync signal resulting from either SELCHSYN or OURACK0. I/O lines are:

(a) SELCHSYN (SELCH Sync Return), Input

Sync return in response to a DMA transfer with the SELCH. (Physically, SELCHSYN represents two lines: DMASR and XFRSYNCH. See Appendix A for further description.)

(b) OURACK0 (Our RACK0), Input

Signal indicating that a RACK0 signal was received by this IDC, which had an interrupt pending.

(c) DLYSYNC (Delayed Sync Return), Output

A DMA sync signal (resulting from SELCHSYN) to the SELCH or an interrupt-acknowledgment sync signal (resulting from OURACK0) to the processor.

(12) Acknowledgment and Attention Circuitry

Handles controller interrupt requests (ATN0) and interrupt acknowledgments (RACK0/TACK0). I/O lines are:

(a) RACK0 (Receive Acknowledge), Input

Signal (resulting from a received RACK0) acknowledging that the processor received an interrupt request (ATN0 signal) from a controller.

(b) OURACK0 (Our RACK0), Output

Signal indicating that the received RACK0 signal was for this IDC, which had an interrupt pending. If this IDC had no interrupt pending, output would be TACK0 instead of OURACK0.

(c) TACK0 (Transmit Acknowledge), Output

Signal, consisting of a received RACK0, passed onto the next controller in the processor cabinet. Refer to Section 3-2.1 for further description.

(d) SATN0 (Set Attention), Input

Signal for activating ATN0 output.

(e) ATN0 (Attention), Output

Signal indicating that this IDC wants to interrupt the processor, i.e., that this IDC has an interrupt pending. See Section 3-2.1 for further description.

(13) Halfword-Mode Circuitry

Informs the SELCH that this controller is in the halfword-mode of operation via lines D00 thru D15. I/O lines are:

(a) SEL*IDLE- (Selected and Not Idle), Input

Signal indicating that this IDC is selected and is not idle. It activates the HW0 output. (Physically, SEL*IDLE- represents two lines: CONTSEL and IDLE. Refer to Appendix A for further description.)

(b) HW0 (Halfword-Mode), Output

Signal informing the SELCH that this IDC is a halfword-oriented device. See Section 3-2.1 for more information.

3-3.2 Disk File Interface

This portion of the IDC board serves as the interface to the Perkin-Elmer disk files. It consists of five functional blocks:

(1) Select and Seek-End (SKEND) Latches,
Serial-Write-Data and Clock Multiplexers (MUXs), and
Serial-Read-Data and Clock Demultiplexers (DEMUXs)
(2) B-Cable Drivers/Receivers
(3) Control and Status Registers/Latches
(4) A-Cable Drivers/Receivers
(5) Power Sequencing Drivers

The following paragraphs describe these functinal blocks and their associated I/O lines.

(1) Select and Seek-End (SKEND) Latches,
Serial-Write-Data and Clock Multiplexers (MUXs), and
Serial-Read-Data and Clock Demultiplexers (DEMUXs)

These circuits serve as the interface between the 8-bit microprocessor bus, BD0:7, and the B-cable circuitry to the disk drives. Select latches are available for selecting one of four possible disk drives attached to the IDC; SKEND latches are available for signaling a Seek-End from the drives. MUXs transmit serial write data and clock signals to the disk drives. And in the other direction, DEMUXs receive serial read data and clock signals from the disk drives. Associated with these MUX and DEMUX operations are write clocks, write data registers, and read clocks. I/O lines are:

(a) WDATA (Serial Write Data), Input

Serial data, along with Error Correction Code (ECC), to be written to a disk file.

(b) SDATA (Serial Read Data), Output

Serial data, along with ECC, read from a disk file.

(c) BD0:7 (Bus Data Lines 0 thru 7), Input/Output

Various data and control bytes.

NOTE

BD0:7 is the 8-bit microprocessor bus of the IDC -- the main data path among the the functional blocks, or modules, of the IDC.

(d) Driver Lines (not labeled), Output

Serial write data and clock signals to the B-cable drivers.

(e) Receiver Lines (not labeled), Input

Serial read data and clock signals from the B-cable receivers.

(2) B-Cable Drivers/Receivers

B-cable drivers receive serial write data and clock signals from the MUXs and transfer them to the disk files. B-cable receivers receive serial data and clock signals from the disk files and transfer them to the DEMUXs. For detailed descriptions of all I/O lines connected to the drivers/receivers via these four connectors, CONN 3 thru CONN 6, refer to Sections 3-1.3 and 3-2.3.

(3) Control and Status Registers/Latches

Latch data and controls associated with the A-cable. I/O lines are:

(a) BD0:7 (Bus Data Lines 0 thru 7), Input/Output

Various data and controls to and from the registers and latches.

(b) CTL'S (Control Lines), Input

Control signals to latch or enable data and controls for BD0:7.

(c) Driver/Receiver Lines (not labeled), Input/Output

See paragraph (4) below.

(4) A-Cable Drivers/Receivers

By means of registers and latches, A-cable drivers receive various data and controls from BD0:7 and transfer them to the disk files. A-cable receivers receive data and controls from the disk files and transfer them to BD0:7 by means of registers and latches. For detailed descriptions of all I/O lines connected to the A-cable drivers/receivers via CONN 2, refer to Sections 3-1.2 and 3-2.2.

(5) Power Sequencing Drivers

Control the power sequencing grounds, PICK and HOLD, and the Open Cable Detect signal. I/O lines are:

(a) PICK,HOLD (Power Sequence Pick/Hold), Input/Output

Signals for enabling or disabling power sequencing. Both of these signals are active (ground) when IDC SEQ Pins 1 and 2 are not strapped and when the processor is turned on. For more details, refer to Section 3-2.2.

(b) OBCAD (Open Cable Detect), Input/Output

Signal for indicating an open A-cable or loss of IDC power. Refer to Section 3-2.2 for more details.

3-3.3 Microprocessor Controller Logic

This portion of the IDC board interprets and acts on the 3200-Series processor commands (e.g., Seek, Read, Write, and Format), causing the disk drives to perform specific operations or data transfers. It also controls the IDC interface circuitry between the SELCH/MUX bus and the disk files. Microprocessor control logic consists of twenty-two functional blocks:

(1) Two 4-Bit Slice Microprocessors
(2) Control-Store Programmable Read Only Memory (PROM) Banks
(3) Pipeline Register
(4) Microprogram Sequencer
(5) Map PROM
(6) Condition Code MUX
(7) MUX Inverter
(8) Data Latch
(9) Map Latch
(10) Random Access Memory (RAM)
(11) RAM Control MUX
(12) RAM Control Register
(13) RAM-Address Counter for Disk File Transfer, and Latch
(14) RAM-Address Counter for DMA Transfer, and Latch
(15) General-Purpose Data Registers
(16) DMA Data Registers
(17) DMA Control and Bus Data (BD) I/O Control
(18) Control Latches
(19) Error Correction Code (ECC) Generation
(20) Error Correction Control
(21) Parallel-to-Serial Conversion
(22) Serial-to-Parallel Conversion

The following paragraphs describe these functional blocks and their associated I/O lines.

(1) Two 4-Bit Slice Microprocessors

Serve as the 8-bit Arithmetic Logic Unit (ALU) of the IDC. This ALU includes sixteen 8-bit ALU registers: each register consists of two 4-bit slices, with two address ports labeled A and B. Chapter 4 presents a more thorough description of this functional block. I/O lines are:

(a) BD0:7 (Bus Data Lines 0 thru 7), Input/Output

Various data and controls to and from the microprocessor controller logic.

(b) LBD0:7 (Latched Bus Data Bits 0 thru 7), Input

Latched data (i.e., temporarily stored data) from BD0:7. This data is used by the ALU as input.

(c) A (A-Register Address Bits), Input

A 4-bit binary-coded value for selecting one of the sixteen ALU registers as the A-register. (Physically, A represents four lines: A0 thru A3. Refer to Appendix A for further description.)

(d) B (B-Register Address Bits), Input

A 4-bit binary-coded value for selecting one of the sixteen ALU registers as the B-register. (Physically, B represents four lines: B0 thru B3. Refer to Appendix A for further description.)

(e) I (ALU Instruction Bits), Input

A 9-bit binary-coded field for ALU instruction input. The first 3-bit value of this field yields the source of the ALU input data. The second 3-bit value gives a specific ALU instruction, arithmetic or logical. The third 3-bit value yields the destination for the resulting ALU output data. (Physically, I represents nine lines: I0 thru I8. Refer to Appendix A for further description.)

(f) CONT (Control), Input

Two control bits: one for enabling output onto BD0:7, and one for arithmetic carry-in. (Physically, CONT represents two lines: CIN and POE. Refer to Appendix A for further description.)

(g) COND CODE (Condition Code), Output

A 4-bit condition code associated with ALU instruction execution: overflow, sign bit, carry, and zero result. (Physically, COND CODE represents four lines: OFLOW, SIGN, CARRY7, and F=0. Refer to Appendix A for further description.)

(2) Control Store PROM Banks

Consist of PPOM for storing the IDC microcode -- the internal IDC program which controls the microprocessor circuitry to provide controller operations. PROM is organized into 1024 (two banks of 512) 56-bit words. Throughout the following descriptions, these 56-bit words are referred to as microinstructions or microcode. I/O lines are:

(a) PA0:8, SPA9 (Program Address Lines 0 thru 9), Input

A 10-bit address from the Microprogram Sequencer for selecting one of the 1024 microcode locations.

(b) 56 Lines (not labeled), Output

A 56-bit word containing microcode as output to the Pipeline Register.

(3) Pipeline Register

Provides "pipeline" storage of the next sequential microinstruction. I/O lines are:

(a) 56 Lines (not labeled), Input

A 56-bit word, from Control Store PROM, containing the next sequential microinstruction.

(b) RAM0:7 (RAM Address Bits), Output

An 8-bit address of a RAM location.

(c) RAM CTL (RAM Control), Output

Lines for controlling RAM enable, read, and write. (Physically, RAM CTL represents five lines: MWE, MCE, AE/OE, PZ, and CNT. See Appendix A for further description.)

(d) BDIO0:5 (Bus Data I/O Control), Output

A 6-bit code for controlling the source and destination of BD0:7 data and for controlling IDC operations like

latching and ECC-register shifting. Refer to Appendix A for further description of these controls.

(e) A (A-Register Address Bits), Output

A 4-bit binary-coded value for selecting one of the sixteen ALU registers as the A-register. (Physically, A represents four lines: A0 thru A3. Refer to Appendix A for further description.)

(f) B (B-Register Address Bits), Output

A 4-bit binary-coded value for selecting one of the sixteen ALU registers as the B-register. (Physically, B represents four lines: B0 thru B3. Refer to Appendix A for further description.)

(g) I (ALU Instruction Bits), Output

A 9-bit binary-coded field for ALU instruction input. The first 3-bit value of this field yields the source of the ALU input data. The second 3-bit value gives a specific ALU instruction, arithmetic or logical. The third 3-bit value yields the destination for the resulting ALU output data. (Physically, I represents nine lines: I0 thru I8. Refer to Appendix A for further description.)

(h) CONT (Control), Output

Two control bits: one for enabling output onto BD0:7, and one for arithmetic carry-in. (Physically, CONT represents two lines: CIN and POE. Refer to Appendix A for further description.)

(i) COND MUX CTL (Condition Code MUX Control), Output

Four bits of which three select one of eight conditions to be output by the Condition Code MUX. The fourth bit controls the MUX Inverter. (Physically, COND MUX CTL represents four lines: MA, MB, MC, and MI. For further description refer to Appendix A.)

(j) BRA0:9 (Branch Address Bits), Output

A 10-bit address serving as a possible microprogram branch address or as a count value for the Microprogram Sequencer.

(k) SI0:3 (Sequencer Instruction Bits), Output

A hexadecimal value for one of sixteen sequencer instructions. See Appendix A for further description.

(4) Microprogram Sequencer

Calculates the next address within Control Store PROM. It performs any one of sixteen "next address" calculations, including sequential, branch conditional, and return conditional. I/O lines are:

(a) SI0:3 (Sequencer Instruction Bits), Input

A hexadecimal value for one of sixteen sequencer instructions. Refer to Appendix A for further description.

(b) BRA0:9 (Branch Address Bits), Input

A 10-bit microprogram branch address or count value from the Pipeline Register.

(c) BRA0:7 (Branch Address), Input

An alternate 8-bit microprogram branch address or count value from the Map PROM.

(d) CC (Condition Code), Input

A pass or fail condition code for one of eight possible conditions determined by MA:MC. Refer to Appendix A. The Microprogram Sequencer uses CC for a "next address" calculation, e.g., a conditional branch or conditional return.

(e) PA0:8, SPA9 (Program Address Lines 0 thru 9), Output

A 10-bit address for selecting one of the 1024 microcode locations in Control Store PROM.

(5) Map PROM

Contains constant data used by the microcode program, and contains addresses of routines within Control-Store PROM. Map PROM is organized into 512 8-bit locations: 256 bytes for the routine addresses and 256 bytes for the constant data. During power-up, the second set of 256 bytes (containing the constant data) is copied into RAM. Later, the first set of 256 bytes (containing a table of routine addresses) is used for vectoring to a particular microcode routine: on receiving an instruction from the processor, e.g., Read, Write, or Format Track, the IDC logic references this table, gets the address of the microroutine for executing that instruction, and vectors to the routine. I/O lines are:

(a) LBD0:7 (Latched Bus Data Bits 0 thru 7), Input

Latched BD0:7 data which will result in the Map PROM outputting either constant data or a microroutine address.

(b) BRA0:7 (Branch Address), Output

Either a constant value or a microroutine address. If BRA0:7 contain a constant, it goes to the Map Latch. If BRA0:7 contain a microroutine address, it goes to the Microprogram Sequencer.

(6) Condition Code MUX

Provides the Condition Code (CC) input to the Microprogram Sequencer. I/O lines are:

(a) COND CODE (Condition Code), Input

A 4-bit condition code associated with an ALU instruction execution: overflow, sign bit, carry, and zero result. (Physically, COND CODE represents four lines: OFLOW, SIGN, CARRY7, and F=0. Refer to Appendix A for further description.)

(b) COND MUX CTL (Condition Code MUX Control), Input

Three bits for selecting one of eight conditions to be output by the Condition Code MUX. The selected condition is output as the CC to the Microprogram Sequencer. (Here, COND MUX CTL represents three lines:

MA, MB, and MC. Refer to Appendix A for further description.)

(c) CC (Condition Code), Output

Selected condition code sent to the Microprogram Seuencer, via the MUX Inverter.

(7) MUX Inverter

Passes the selected condition code to the Microprogram Sequencer, with or without inversion according to the received MI bit. I/O lines are:

(a) MI (MUX Inverter Bit), Input

The fourth bit of the COND MUX CTL output from the Pipeline Register. If the MI bit is set, the CC output is inverted; otherwise, the CC is passed as received from the Condition Code MUX.

(b) CC (Condition Code), Input/Output

As input, CC is the selection of one of eight possible condition codes from the Condition Code MUX. As output, CC is in either true or complement form according to the MI input.

(8) Data Latch

Latches BD0:7 data for input to either the ALU (the two 4-bit slice microprocessors) or the Map PROM. I/O lines are:

(a) BD0:7 (Bus Data Lines 0 thru 7), Input

Various microprocessor bus data.

(b) LBD0:7 (Latch Bus Data Bits 0 thru 7), Output

Data as input to the ALU or the Map PROM.

(9) Map Latch

Latches data constants output from the Map PROM and outputs this data onto BD0:7. I/O lines are:

(a) BRA0:7 (Constant Data), Input

Data constants from the Map PROM. (At power-up, the Map PROM must write data constants to the RAM.)

(b) BD0:7 (Bus Data Lines 0 thru 7), Output

Data constants written to the RAM.

(10) Random Access Memory (RAM)

Stores data constants and buffers read/write data. RAM consists of 1024 8-bit locations. It is equally divided into four pages: Page 0, consisting of 256 bytes, holds tabularized data constants from the Map PROM. Pages 1, 2, and 3 buffer data read from and written to one of the disk files; each of these pages holds one logical sector (256 bytes) for the IDC-formatted disk media. I/O lines are:

(a) BD0:7 (Bus Data Lines 0 thru 7), Input/Output

Data bytes to and from various functional blocks throughout the microprocesssor control logic.

(b) RAM0:7 (RAM Address Bits), Input

An 8-bit address within a page of RAM memory. One of the two RAM-Address Counters generate this address; see paragraphs (13) and (14) below.

(c) RAM0:7 (RAM Address Bits), Input

An 8-bit address within a page of RAM memory. Control Store PROM generates this address in order to read a data constant.

(d) A8, A9 (RAM Page Address Lines), Input

Two binary bits for selecting one of four pages in RAM. (Physically, A8 and A9 represent two lines: PAGE13 and PAGE23. Refer to Appendix A for further description.)

(e) R/W (Read/Write Enable), Input

Signal for selecting a RAM read operation or a RAM write operation over BD0:7. (Physically, R/W represents one line: WENB. Refer to Appendix A for further description.)

(f) CENB (Chip Enable), Input

Signal for enabling RAM output onto BD0:7.

(11) RAM Control MUX

Controls the multiplexing of I/O operations at the RAM. (See paragraph (10) above for a description of RAM organization.)

The RAM Control MUX multiplexes simultaneous read operations at the RAM, as follows: During a read operation from a disk file, RAM first reads a logical sector from the disk file into page 1. If this operation is a multisector read, RAM also reads another logical sector into page 2. Once page 1 is filled with a logical sector, and the ECC circuitry validates the ECC, DMA transfer to the SELCH/MUX bus begins. This transfer occurs simultaneously with the filling of page 2, as directed by the RAM Control MUX. The filling of pages 2 and 3, and pages 3 and 1, proceed in the same manner.

Likewise, the RAM Control MUX multiplexes simultaneous write operations at the RAM, as follows: During a write operation to a disk file, RAM first writes a logical sector from the SELCH/MUX bus into page 1. Once page 1 is filled with a logical sector, data transfer to the selected disk file may begin. While this transfer is in progress, page 2 is filled with an additional sector of DMA data from the SELCH/MUX bus. The filling of pages 2 and 3, and pages 3 and 1, proceed in the same manner.

In summary, the RAM Control MUX directs the multiplexing of RAM operations for DMA and disk file I/O. This multiplexing ensures that these operations are performed simultaneously at their required speeds. I/O lines are:

(a) RAM CTL (RAM Control), Input

Control information required for multiplexing the DMA and disk file I/O. (Physically, RAM CTL represents five lines: MWE, MCE, AE/OE, PZ, and CNT. See Appendix A for further description.)

(b) A8, A9 (RAM Page Address Lines), Output

Two binary bits for selecting one of the three buffering pages: page 1, 2, or 3. (Physically, A8 and A9 represent two lines: PAGE13 and PAGE23. Refer to Appendix A for further description.)

(c) R/W (Read/Write Enable), Output

Signal for selecting a RAM read or RAM write operation over BD0:7. (Physically, R/W represents one line: WENB. Refer to Appendix A for further description.)

(d) CENB (Chip Enable), Output

Signal for enabling RAM output onto BD0:7.

(12) RAM Control Register

Holds information necessary for generating the RAM page number, read/write control, and chip enable as described above in paragraph (11). I/O lines are:

(a) BD0:7 (Bus Data Lines 0 thru 7), Input

Input data related to the page number and control signals needed for I/O multiplexing at the RAM.

(b) RAM CTL (RAM Control), Output

Control information required for multiplexing the DMA and disk file I/O. (Physically, RAM CTL represents five lines: MWE, MCE, AE/OE, PZ, and CNT. See Appendix A for further description.)

(13) RAM-Address Counter for Disk File Transfer, and Latch

Specifies the address of a RAM location written to or read from a disk file. The associated latch controls the counter output to the RAM0:7 lines.

(a) BD0:7 (Bus Data Lines 0 thru 7), Input

Value for determining the RAM page location from which data transfer shall occur.

(b) RAM0:7 (RAM Address Bits), Output

RAM memory location for the disk file transfer.

(14) RAM-Address Counter for DMA Transfer, and Latch

Specifies the address of the RAM location written to or read from the SELCH/MUX bus. The DMA transfer is always 256 bytes, i.e., 128 halfwords. The associated latch controls the counter output to the RAM0:7 lines.

(a) CTL (Control Line), Input

Signal for initializing the counter, which then counts up to 255 for the transfer of 256 bytes.

(b) RAM0:7 (RAM Address Bits), Output

RAM memory location for the DMA transfer.

(15) General-Purpose Data Registers

Store various data to be sent to the SELCH/MUX bus, e.g., status, sector addresses, or RPS data. These registers also store various data received from the SELCH/MUX bus for RAM input, e.g., a cylinder or head address. I/O lines are:

(a) CTL'S (Control Lines), Input

Three controls for determining whether general-register data is to be transmitted to the SELCH/MUX bus, received from the SELCH/MUX bus, or enabled for output over BD0:7.

(b) D08:15 (Data Bits 8 thru 15), Input

Byte of information from the SELCH/MUX bus.

(c) GPD08:15 (General-Purpose Data), Output

Register data to be sent to the SELCH/MUX bus.

(d) BD0:7 (Bus Data Lines 0 thru 7, Input/Output

General-purpose data sent to and received from the microprocessor controller logic.

(16) DMA Data Registers

Hold data received and transmitted between the SELCH/MUX bus and RAM. I/O lines are:

(a) BD0:7 (Bus Data Lines 0 thru 7), Input/Output

DMA data transfered between RAM and the SELCH/MUX bus.

(b) CTL'S (Control Lines), Input

Ten control/timing signals for loading the registers and enabling them to output data to the applicable buses.

(c) D00:15 (Receive Data Bits 00 thru 15), Input

Halfword of data received from the SELCH/MUX bus, to be output to the RAM.

(d) DATA00:15 (Data Bits 00 thru 15), Output

Halfword of data to be sent to the SELCH/MUX bus.

(17) DMA Control and Bus Data (BD) I/O Control

Sets up and maintains DMA transfers, via the DMA Data Registers, between the SELCH/MUX bus and the RAM. I/O lines are:

(a) CTL'S (Control Lines), Input

Ten control/timing signals. These are also passed on to the DMA Data Registers.

(b) BDI00:5 (Bus Data I/O and Controls), Input

A 6-bit code that controls the source and destination for BD0:7 and provides numerous control signals. See Appendix A for further description.

(c) CTL'S (Control Lines), Output

Control for one of the operations selected by the decoding of BDI00:5 input.

(d) 3200 PTCL (3200 Protocol), Output

Control signals to the SELCH for the "new" high-speed SELCH protocol. (Physically, 3200 PTCL represents two lines: STCHK and CTLOPTC. Refer to Appendix A for further description.)

(18) Control Latches

Latches halfword data (e.g., cylinder or head address) from the processor for subsequent input to the RAM. I/O lines are:

(a) D00:15 (Data Halfword), Input

Data halfword received over the SELCH/MUX bus from the processor.

(b) CTL'S (Control Lines), Input

Control/timing functions required for receiving halfword data from the processor.

(c) BD0:7 (Bus Data Lines 0 thru 7), Output

Halfword data latched from the processor and sent as bytes to the RAM.

(19) Error Correction Code (ECC) Generation

Generates a 32-bit ECC for a disk file write or read operation.

With a write operation, ECC Generation receives serial write data from input line RSR00, as described in paragraph (21) below. The circuitry then generates an ECC, which Error Correction Control appends to the end of the 256 bytes of data written to the selected disk file.

With a read operation, ECC Generation receives serial read data from input line RSR00, as described in paragraph (22) below. This input, consisting of 256-bytes of data and a 32-bit ECC, is serially shifted into the ECC Generation circuitry. ECC Generation then generates a new ECC from the 256 data bytes, and compares it with the read ECC. If the two ECCs match, the ECC is "validated."

I/O lines are:

(a) CTL'S (Control Lines), Input

Control/timing signals necessary for generating ECCs.

(b) RSR00 (Read/Write Serial Data), Input

Serial data shifted into the ECC circuitry during a read or write operation. During a read operation, this serial input data also includes an ECC.

(c) BD0:7 (Bus Data Lines 0 thru 7), Output

Error correction information output to the microprocessor logic whenever an ECC is not validated, i.e., whenever an ECC is found erroneous.

(20) Error Correction Control

Provides control circuitry necessary for ECC operations. I/O lines are:

(a) RSR00 (Read/Write Serial Data), Input

Serial data shifted into the ECC circuitry during a write operation to a disk file.

(b) CTL'S (Control Lines), Input/Output

Control/timing signals necessary for generating ECCs and for detecting ECC errors.

(c) WDATA (Write Data), Output

Serial data, along with a generated ECC, to be written to a disk file.

(21) Parallel-to-Serial Conversion

Converts parallel RAM data from BD0:7 to serial data to be written to a disk file. This conversion circuitry applies only during disk file write operations, where data is written from the SELCH/MUX bus, via the RAM, to a disk file. I/O lines are:

(a) CTL'S (Control Lines), Input

Control/timing signals necessary for synchronizing the resulting serial write data to the disk file.

(b) BD0:7 (Bus Data Lines 0 thru 7), Input

Parallel data written from the RAM. The RAM originally received this data from the SELCH/MUX bus.

(c) WSR (Write Serial Data), Output

Serial data to be written to a disk file. WSR output is passed, via Serial-to-Parallel Conversion, as RSR00 to Error Correction Control. There, a 32-bit ECC from ECC Generation circuitry is appended to the end of the 256 bytes of write data.

(22) Serial-to-Parallel Conversion:

Converts serial disk file data from the SDATA input to parallel data, to be sent to the RAM. This conversion circuitry applies during disk file read operations, where data is read from a disk file, to the RAM, and to the SELCH/MUX bus. Also, during a write operation, this circuitry passes WSR input as RSR00 output to Error Correction Control and ECC Generation. I/O lines are:

(a) SDATA (Serial Data), Input

Serial data and ECC read from the disk file.

(b) RSR00 (Read/Write Serial Data), Output

Same serial data and ECC as above, output to the ECC Generation circuitry. More specifically, for a single disk file read operation, RSR00 contains 256 bytes of data and a trailing 32-bit ECC. This data and ECC are input to ECC Generation circuitry which checks for errors. See paragraph (19) above.

(c) BD0:7 (Bus Data Lines 0 thru 7), Output

Parallel data sent to the RAM.

CHAPTER 4

MAINTENANCE

4-1 INTRODUCTION

Along with the table of mnemonics in Appendix A and the IDC board schematics in Appendix B, Chapter 4 presents detailed information necessary for troubleshooting the IDC board. Before reading this chapter, you should be thoroughly familiar with Chapter 3. For information pertaining to preventive maintenance on IDC disk files, refer to the list of related publications in Section 1-2.

4-2 MICROPROCESSOR/SEQUENCER CIRCUITRY

The heart of the IDC board is the Microprocessor/Sequencer circuitry. It provides, sequences, executes, and routes the various microinstructions for interfacing a 3200-Series processor and SELCH/MUX bus with the IDC disk files. Illustrated in Figure 3-6, Microprocessor/Sequencer circuitry consists of these functional blocks:

- Microprocessor (Two 4-Bit Microprocessor Chips)
- Pipeline Register
- Control Store PROM
- Microprogram Sequencer

Microinstructions are stored as part of the microprogram within Programmable Read Only Memory (Control Store PROM). Section 4-2.1 discusses these microinstructions.

The Pipeline Register latches each microinstruction (output from PROM) for input to the Microprocessor and to the various functional blocks of the IDC controller logic.

The Microprocessor, alternately referred to as the ALU, executes ALU instructions which are part of each microinstruction received from the Pipeline Register. Section 4-2.2 discusses the Microprocessor.

The Microprogram Sequencer gives the IDC the capability of executing its stored microprogram from PROM. This capability classifies the IDC as "intelligent." By acting on condition code, sequencer instruction, and branch address inputs, the Microprogram Sequencer controls the execution sequence of the microprogram. Each 10-bit address output from the Microprogram Sequencer selects one of the 1024 microinstructions as the next instruction to be executed. Section 4-2.3 discusses the Microprogram Sequencer.

Section 4-2.4 describes the clock signals associated with Microprocessor/Sequencer operation.

Section 4-2.5 discusses general operation of the Microprocessor/Sequencer circuitry and presents examples of typical operations.

4-2.1 Microcode Instructions

A microcode instruction, or microinstruction, is a 56-bit output from Control Store PROM. Corresponding to these 56 bits are 56 output lines. Refer to Figure 3-6, to the right side of the block diagram. As shown, going into the Pipeline Register from PROM are 56 lines (unlabeled). These same lines, which represent the 56 bits of a stored microinstruction, are output from the top of the Pipeline Register to these destinations: the RAM circuitry, the Bus Data I/O Control circuitry, the Microprocessor (i.e., the two 4-bit microprocessor chips), and the Microprogram Sequencer.

Table 4-1 on the next page lists the line mnemonics corresponding to the 56 microinstruction bits. These bits or lines are classified into five functional fields:

(1) RAM Address/Control
(2) Bus Data I/O Control
(3) ALU Address/Control
(4) Branch Address/Control
(5) Microprogram Sequencer

Sections 4-2.1.1 thru 4-2.1.5 discuss the 56 output lines within these five fields.

Table 4-1. Bit Definitions of the 56-Bit Microinstruction

BIT*	MNEMONIC	NAME	BIT*	MNEMONIC	NAME
55	BRA7	Branch Address Bit 7	26	CIN	Carry-In
54	BRA6	Branch Address Bit 6	25	POE	ALU Output Enable
53	BRA5	Branch Address Bit 5	24	MI	CC MUX Inverter Bit
52	BRA4	Branch Address Bit 4	23	RAM7	RAM Address Bit 7
51	BRA3	Branch Address Bit 3	22	RAM6	RAM Address Bit 6
50	BRA2	Branch Address Bit 2	21	RAM5	RAM Address Bit 5
49	BRA1	Branch Address Bit 1	20	RAM4	RAM Address Bit 4
48	BRA0	Branch Address Bit 0	19	RAM3	RAM Address Bit 3
47	SI3	Sequencer Instruction Bit 3	18	RAM2	RAM Address Bit 2
46	SI2	Sequencer Instruction Bit 2	17	RAM1	RAM Address Bit 1
45	SI1	Sequencer Instruction Bit 1	16	RAM0	RAM Address Bit 0
44	SI0	Sequencer Instruction Bit 0	15	BDIO5	Bus Data I/O Bit 5
43	A3	A-Register Address Bit 3	14	PZ	RAM Page Zero
42	A2	A-Register Address Bit 2	13	AE/OE	RAM Address Enable
41	A1	A-Register Address Bit 1	12	MCE	RAM Chip Enable
40	A0	A-Register Address Bit 0	11	MWE	RAM Write Enable
39	B3	B-Register Address Bit 3	10	CNT	RAM Page Counter Enable
38	B2	B-Register Address Bit 2	09	BRA9	Branch Address Bit 9
37	B1	B-Register Address Bit 1	08	BRA8	Branch Address Bit 8
36	B0	B-Register Address Bit 0	07	MC	CC MUX Selection Bit C
35	I8	ALU Instruction Bit 8	06	MB	CC MUX Selection Bit B
34	I7	ALU Instruction Bit 7	05	MA	CC MUX Selection Bit A
33	I6	ALU Instruction Bit 6	04	BDIO4	Bus Data I/O Bit 4
32	I5	ALU Instruction Bit 5	03	BDIO3	Bus Data I/O Bit 3
31	I4	ALU Instruction Bit 4	02	BDIO2	Bus Data I/O Bit 2
30	I3	ALU Instruction Bit 3	01	BDIO1	Bus Data I/O Bit 1
29	I2	ALU Instruction Bit 2	00	BDIO0	Bus Data I/O Bit 0
28	I1	AIU Instruction Bit 1			
27	I0	ALU Instruction Bit 0			

* MSB is bit 55; LSB is bit 00.

4-2.1.1 RAM Address/Control Field

This field has thirteen bits. As shown in Figure 3-6, two outputs leave the top of the Pipeline Register and go to the RAM control circuitry: RAM Address Lines (RAM0:7) and RAM Control (RAM CTL). RAM0:7 is an 8-bit address for selecting one of 256 locations within one of the four RAM pages. RAM CTL represents five control lines:

(1) RAM Address Enable (AE/OE)

A high on this line selects RAM0:7 from the Pipeline Register as the RAM address source. A low selects RAM0:7 from the RAM Address Counter as the address source.

(2) RAM Page Counter Enable (CNT)

When high, this line enables the RAM Page Counter to increment to the next page.

(3) RAM Chip Enable (MCE)

This line enables the RAM for a read or write operation.

(4) RAM Write Enable (MWE)

This line enables RAM to be written to.

(5) Page Zero (PZ)

This line selects RAM page zero.

4-2.1.2 Bus Data I/O Control Field

This field has six bits: Bus Data I/O and Control Bits (BDIO0:5). BDIO0:5 contain a 6-bit code for controlling I/O over the Microprocessor Bus BD0:7. Table 4-2 on the next three pages lists the BDIO0:5 codes and the corresponding BD0:7 contents. For additional information to interpret this table, refer to the table of mnemonics in Appendix A.

Notice that the MODE column of Table 4-2 specifies either a Read, a Write, or a Strobe. A Read denotes BD0:7 source data going into the Microprocessor or RAM. A Write denotes BD0:7 destination data going out of the Microprocessor, RAM, or Map PROM. A Strobe denotes one of the numerous bus data control functions. Refer to Section 4-2.4.2 for further detail.

Table 4-2. BDI00:5 Values for Microprocessor Bus Functions

BDI00:5 OCT.	BDI00:5 HEX.	MODE & TIMING	FUNCTION MNEMONIC	FUNCTION NAME	CONTENTS OF BD0:7 BITS* BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
00	00	------ CLK23	NOP	No Operation								
01	01	Strobe CLK23	CINTCLR	Internal Clear								
02	02	Read CLK23	ECCLO	Load ECC Low	ECC23	ECC22	ECC21					
03	03	Read CLK23	ECCHI	Load ECC High	ECC31	ECC30	ECC29	ECC28	ECC27	ECC26	ECC25	ECC24
04	04	R/W CLK23	XFERLO	Transfer Low Byte	**	**	**	**	**	**	**	**
05	05	R/W CLK23	XFERHI	Transfer High Byte	**	**	**	**	**	**	**	**
06	06	Read CLK23	DE	Data Enable	**	**	**	**	**	**	**	**
07	07	Strobe CLK23	RSTATN	Reset Attention								
10	08	Read CLK23	RBC	Read Bus Control	NEWFILE	INTREQ	EXTCLR	FILE23	FILE13	FUNC2	FUNC1	FUNC0
11	09	Read CLK23	RRA	Read RAM Address	RAM7	RAM6	RAM5	RAM4	RAM3	RAM2	RAM1	RAM0
12	0A	Read CLK23	EDS	Enable Disk Status	BUSY	WPROT	READY	ONCYL	SKER	FAULT	SECTOR	INDEX
13	0B	Read CLK23	ESE	Enable Seek End and Drive Select	SKEND3	SKEND2	SKEND1	SKEND0	SEL3	SEL2	SEL1	SEL0
14	0C	Read CLK23	RBD	Read Bus Data	D08	D09	D10	D11	D12	D13	D14	D15
15	0D	Read CLK23	RBS	Read Bus Status	DMAGO	SELCHBZ	PARTIAL	OVERRUN	BITSR0	SECTOV	TIMFOUT	FMTENBL

Table 4-2. BDI00:5 Values for Microprocessor Bus Functions (Continued)

BDI00:5		MODE & TIMING	FUNCTION MNEMONIC	FUNCTION NAME	CONTENTS OF BD0:7 BITS*							
OCT.	HEX.				BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
16	0E	Read CLK23	ESTBRA	Establish Branch Address	Mask BUSY	Mask WPROT	Mask READY	Mask ONCYL	Mask SKER	Mask FAULT	***	
17	0F	Strobe CLK23	SSYN	Set Sync								
20	10	Write CLK3	LDPAGE	Load RAM Page Number					****	****	LP23	LP13
21	11	Write CLK3	LDDSK	Load Disk	RAM7	RAM6	RAM5	RAM4	RAM3	RAM2	RAM1	RAM0
22	12	Write CLK3	LDCB	Load Disk Data Bus	B07	B06	B05	B04	B03	B02	B01	B00
23	13	Write CLK3	LDCT	Load Disk Control Tag	SCT	SHT	CT	USEL Tag	(spare)	(spare)	B09	B08
24	14	Write CLK3	LDDMA	Load DMA					****	Write/ Read	DMA23	DMA13
25	15	Strobe CLK3	SATN	Set Attention								
26	16	Write CLK3	TBD	Transmitted Bus Data	GPD08	GPD09	GPD10	GPD11	GPD12	GPD13	GPD14	GPD15
27	17	Strobe CLK3	LON	Turn On Diagnostic								
30	18	Strobe CLK3	CON	Microcode Clear to Zero								
31	19	Write CLK3	INTDATA	Interrupt Data					CINT/ FINT	****	FA14	FA15
32	1A	Strobe CLK3	LOF	Clear Diagnostic								
33	1B	Strobe CLK3	DMASTRT	DMA Start								

Table 4-2. BDI00:5 Values for Microprocessor Bus Functions (Continued)

BDI00:5		MODE & TIMING	FUNCTION MNEMONIC	FUNCTION NAME	CONTENTS OF BD0:7 BITS*							
OCT.	HEX.				BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
34	1C	Strobe CLK3	SAVCRY0	Save Carry								
35	1D	Strobe CLK3	STPSLCH	Stop SELCH Strobe								
36	1E	Strobe CLK3	SETIDL	Set Idle								
37	1F	Strobe CLK3	RSTIDL	Reset Idle								
40	20	Read CLK23	DCL	Disk Status Clear and Enable	BUSY	WPROT	READY	ONCYL	SKER	FAULT	SECTOR	INDEX
41	21	Strobe CLK23	OFF	ECC Off								
42	22	Strobe CLK23	ON	ECC On								
43	23	Strobe CLK23	SEC	Shift ECC								
44	24	Strobe CLK23	MEC	Enable ECC Shift								
45	25	Strobe CLK23	ME	Map PROM Enable								
46	26	Strobe CLK23	FOUND	Sector Found								
47	27	Write CLK23	SEL	Select Pulse							DRV23	DRV13

* Blank entries indicate that the bit position is neither latched nor used.
** Register data I/O. See descriptions of corresponding mnemonics in Appendix A.
*** Bits BD7:2 associated with ESTBRA do not actually contain the specified mask data. However, the BD7:2 bits are ANDed with the specified mask mnemonics to enable status branches.
**** These entries indicate that the bit position is latched but not currently used.

4-2.1.3 ALU Address/Control Field

This field has nineteen bits. As shown in Figure 3-6, four outputs leave the top of the Pipeline Register and go to the Microprocessor circuitry: A, B, CONT, and I.

A-output represents four lines: A-Register Address Bits (A0:3). A0:3 contain a binary value for selecting one of the ALU registers as the source A-Register. Section 4-2.2 further discusses this selection.

B-output represents four lines: B-Register Address Bits (B0:3). B0:3 contain a binary value for selecting one of the ALU registers as the source/destination B-Register. Section 4-2.2 further discusses this selection.

CONT output represents two lines: Carry-In (CIN) and ALU Output Enable (POE). CIN is a microcode-generated carry input to the ALU. POE enables ALU output onto BD0:7. Section 4-2.2 further discusses these lines.

I output represents nine lines: ALU Instruction Bits (I0:8). I0:8 contain a 9-bit instruction for an ALU operation. The first three bits of this code, I0:2, denote the source of input data; the second three bits, I3:5, specify the particular ALU operation; and the third three bits, I6:8, denote the destination of results. Refer to Tables 4-4 thru 4-7 in Section 4-2.2 for detailed descriptions of I0:8.

4.2.1.4 Branch Address/Control Field

This field has ten bits: Branch Address Bits (BRA0:9). BRA0:9 contain either a 10-bit branch address or a constant count value as input to the Microprogram Sequencer. These bits specify either the location of the next microinstruction to branch to or the count value for controlling microinstruction loop executions. Execution of a particular branch address depends on the Microprogram Sequencer field discussed below.

4-2.1.5 Microprogram Sequencer Field

This field has eight bits. As shown in Figure 3-6, two outputs leave the top of the Pipeline Register and go to the Microprogram Sequencer, via the Condition Code MUX and the MUX Inverter. These outputs are: Condition Code MUX Control (COND MUX CTL) and Microprogram Sequencer Controls (CTL).

COND MUX CTL represents four lines: Condition Code MUX Selection Bits (MA:MC) and the CC MUX Inverter Bit (MI). MA:MC contain a 3-bit code that results in a Condition Code (CC) output, via the Condition Code MUX, to the Microprogram Sequencer. This CC output, along with BRA0:9, is used for a "next address" calculation. Table 4-3 gives the MA:MC possibilities; where necessary, refer to Appendix A for further description of the mnemonics. MI, the fourth bit of COND MUX CTL, inverts the CC output from the MUX Inverter when required.

Sequencer Instruction Bits (SI0:3) contain a hexadecimal value for one of sixteen possible sequencer instructions to generate the next microinstruction address within PROM. Table 4-8 in Section 4-2.3.1 presents a detailed description of these bits.

Table 4-3. MA:MC Values for CC Output

MA:MC VALUE	CONDITION MNEMONIC	CONDITION NAME
0	CCMUXP	CC MUX Output
1	OFLOW	Overflow
2	SIGN	Sign Bit
3	CARRY7	Carry Bit 7
4	RSEL	Register Select
5	IPRY	Input Ready
6	SON	Latched Sync On
7	F=0	Function Equals Zero

* Condition Code (CC) output from the Condition Code Multiplexer consists of one of the eight conditions selected by the octal value of the three bits, MA:MC. (MC is the most significant bit.) Refer to Appendix A for further description of the selected conditions.

4-2.2 The 4-Bit Slice Microprocessors

Two identical 4-bit slice microprocessor chips are connected on the IDC board to form the 8-bit ALU circuitry. One chip handles the most significant four bits (MSBs) of each I/O byte, and the other handles the least significant four bits (LSBs). Figure 4-1 on shows a functional block diagram of one 4-Bit Slice Microprocessor; for further orientation, refer to the block diagram of Figure 3-6. The following paragraphs discuss the functional blocks and I/O lines in Figure 4-1. Labeling in this figure is according to manufacturer's specification.

(a) MicroRAM

This block, also referred to as local RAM, consists of sixteen 4-bit RAM locations. These are addressed by the A- and B-Register Address Lines (A0:3 and B0:3). That is, A0:3 and B0:3 inputs determine which of the sixteen locations are read into the A- and B-Latches.

A0:3 and B0:3 inputs can specify the same address. Also, B0:3 specifies the RAM write location for data input via the RAM Shift MUX.

(b) A- and B-Latches

These two latches hold output from the MicroRAM and serve as inputs to the R- and S-MUXs. Data is held in the A- and B-Latches while CLK6 (see Section 4-2.4) is low, thereby avoiding any race condition.

(c) R-MUX and S-MUX

These multiplexers are the two input ports to the ALU. As shown in Figure 4-1, the R-MUX passes input from either of two sources: Latched Bus Data Bits (LBD0:3 or LBD4:7, depending on whether the microprocessor is the less significant or more significant chip) or A-Latch output. LBD0:7 input is also referred to as direct data. The S-MUX passes input from one of three sources: A-Latch output, B-Latch output, or Q-Register output (Q0:3). In addition to the inputs just specified, the R- and S-MUXs can output a zero to the ALU.

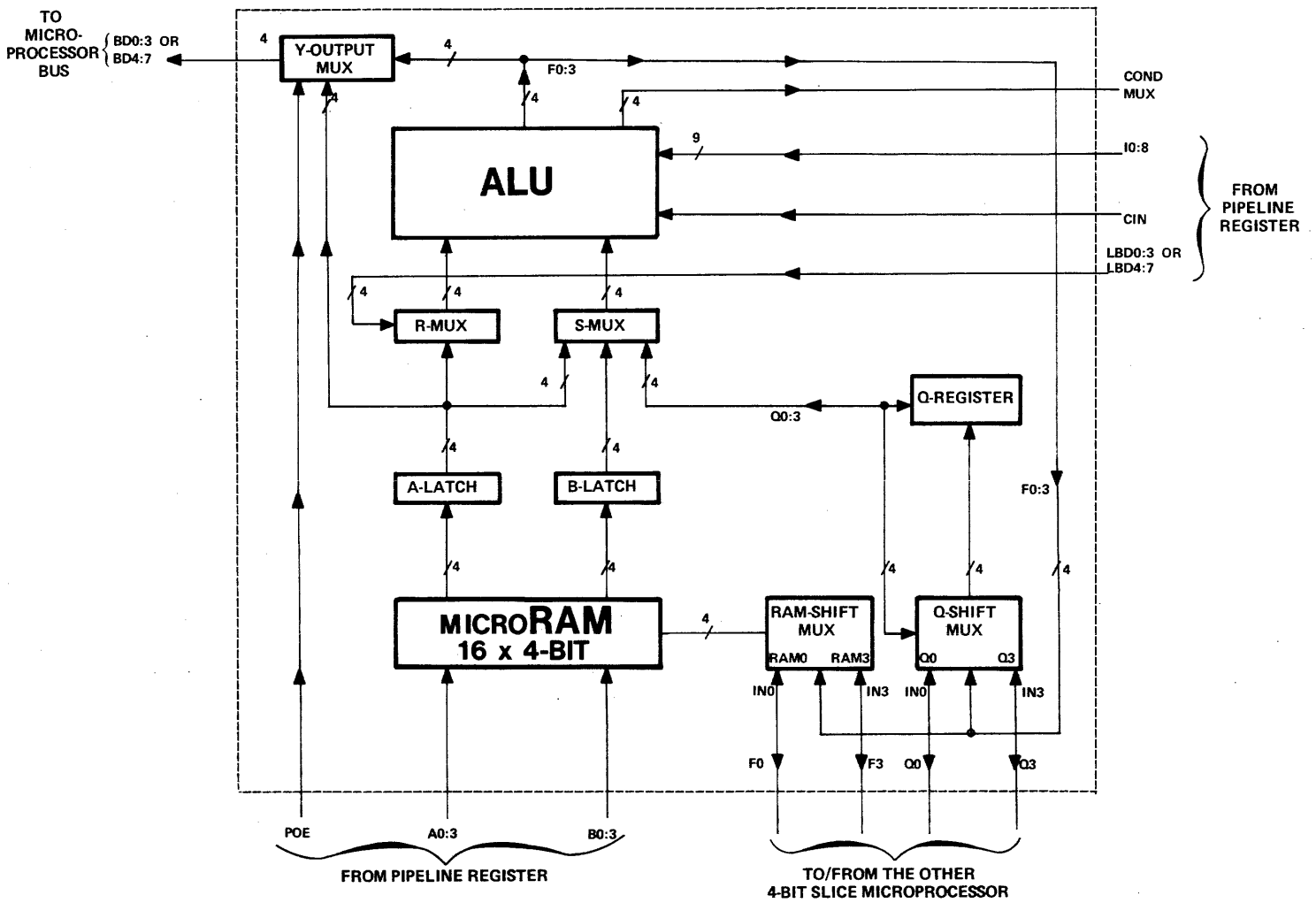


Figure 4-1. Block Diagram of the 4-Bit Slice Microprocessor

(d) Q-Register

The main purpose of the Q-Register is to enable the double-length shifts required by binary multiplication and division. Therefore, the Q-Register receives, via the Q-Shift MUX, both ALU output (F0:3) and its own output (Q0:3). Shifts are controlled by the ALU destination control bits I6:8; Table 4-7 specifies I6:8 values for up and down shifting.

The Q-Register is also employed as a holding register or accumulator.

(e) Q-Shift MUX

This multiplexer receives F0:3 as input from the ALU and Q0:3 as input from the Q-Register. Output to the Q-Register can be shifted one bit in either direction, up or down, or not shifted at all.

The IN0/IN3 inputs and the Q0/Q3 outputs carry overflow bits resulting from an up or down shift operation. Table 4-7 presents further information on this operation.

(f) RAM-Shift MUX

This multiplexer receives F0:03 as input from the ALU. Output goes to the MicroRAM and, like the Q-Shift MUX, this output can be shifted one bit in either direction, or not shifted at all.

The IN0/IN3 inputs and the F0/F3 outputs carry overflow bits resulting from an up or down shift operation. Table 4-7 presents further information on this operation.

(g) Y-Output MUX

This multiplexer receives input from either the ALU or the A-Latch. When the ALU Output Enable (POE) signal is active, low, the Y-Output MUX outputs F0:3 or the A-Register contents onto the Microprocessor Bus (BD0:3 or BD4:7, depending on whether this microprocessor is the less significant or more significant chip).

Microprocessor output lines to BD0:7 are in the high-impedance state whenever POE is high.

(h) ALU

Depending on the input of the ALU Instruction Bits (I0:I8), the ALU performs arithmetic or Boolean functions. Refer to Tables 4-4 thru 4-7 for detailed information. The Carry-In (CIN) input is generated by microcode to increase the number of possible functions. Or, for the more significant ALU, CIN is the carry-out of the less significant ALU. Condition Code (COND CODE) output indicates the results of ALU instruction execution, i.e., the execution of the I0:8 bits. It is a 4-bit condition code representing four lines: Overflow (OFLOW), Sign Bit (SIGN), Carry Bit (CARRY7), and Function Equals Zero (F=0). For further description of these four lines, refer to Appendix A.

4-2.2.1 ALU Instructions from I0:8

ALU instructions are input to the ALU through nine lines: I0:8. (As previously discussed, an ALU instruction is part of the 56-bit microinstruction output from Control Store PROM; see Figure 3-6.) These nine bits determine data flow and control function. The first three bits, I0:2, select the input source to the ALU. The second three bits, I3:5, specify the ALU function to be performed. The third three bits, I6:8, select the destination for the results of the executed function. Tables 4-4 thru 4-7 define the contents of I0:8, and paragraphs (1) thru (3) below discuss these bits.

(1) ALU Source Selection with I0:2

Refer to Figure 4-1. As illustrated there, input to the ALU is from the R-MUX and S-MUX. Furthermore, as discussed earlier:

(a) Input from the R-MUX to the ALU can be one of three sources: LBD0:3/LBD4:7, A-Latch data, or zero.

(b) Input from the S-MUX to the ALU can be one of four sources: A-Latch data, B-Latch data, Q0:3, or zero.

Consequently, the ALU has twelve possible input combinations, as shown below, where: A refers to A-Latch, B refers to B-Latch, D refers to direct data of LBD0:7, Q refers to Q-Register, and Z refers to zero.

```
R-MUX Input:  AAAA DDDD ZZZZ
S-MUX Input:  ABQZ ABQZ ABQZ
```

Since only three bits of the instruction code are available for specifying source input, only eight of the twelve combinations can be defined. However, since A and B can refer to the same MicroRAM location, the AA, AZ, and DB combinations are redundant. Also, since zero/zero input is considered meaningless, ZZ is redundant. Consequently, I0:2 can specify all eight of the effective combinations. See Table 4-4.

Table 4-4. Microinstruction Bits I0:2 for ALU Source Control

I0:2 VALUE			OCTAL CODE	ALU SOURCE INPUT		SOURCE MNEMONIC
I2	I1	I0		R-MUX*	S-MUX*	
0	0	0	0	A-Latch	Q-Register	AQ
0	0	1	1	A-Latch	B-Latch	AB
0	1	0	2	Zero	Q-Register	ZQ
0	1	1	3	Zero	B-Latch	ZB
1	0	0	4	Zero	A-Latch	ZA
1	0	1	5	LBD0:7	A-Latch	DA
1	1	0	6	LBD0:7	Q-Register	DQ
1	1	1	7	LBD0:7	Zero	DZ

* As represented in Figure 4-1, R-MUX and S-MUX are the two input ports to the ALU. Refer to Table 4-6 for I0:2 combinations with the I3:5 bits.

(2) ALU Function Control with I3:5

Basically, I3:5 bits allow eight ALU functions to be specified -- three arithmetic and five Boolean. See Table 4-5. However, since there are eight different ALU input combinations from I0:2, I3:5 actually allow more than just eight ALU functions. Also, the Carry-In (CIN) bit permits additional operations. Table 4-6 shows all functions permited with I3:5, I0:2, and CIN inputs.

Table 4-5. Microinstruction Bits I3:5 for ALU Functions

I3:5 VALUE			OCTAL CODE	ALU FUNCTION*	FUNCTION MNEMONIC
I5	I4	I3			
0	0	0	0	R+S (R plus S)	ADD
0	0	1	1	S-R (S minus R)	SUBR
0	1	0	2	R-S (R minus S)	SUBS
0	1	1	3	R OR S	OR
1	0	0	4	R AND S	AND
1	0	1	5	$\overline{R}$ AND S (not R and S)	NRS
1	1	0	6	R XOR S (R exclusive or S)	XOR
1	1	1	7	$\overline{R \text{ XOR } S}$ (R exclusive nor S)	XNOR

* R and S respectively refer to the two input ports, R-MUX and S-MUX, represented in Figure 4-1. Refer to Table 4-6 for I3:5 combinations with the I0:2 bits.

(3) ALU Destination Selection with I6:8

I6:8 bits select the destination of the F0:3 output resulting from ALU execution of bits I0:5. As illustrated in Figure 4-1, ALU output goes to one or more destinations: the MicroRAM circuitry, the Q-Register circuitry, and the Y-Output MUX. And, depending on the value of I6:8, this output can be up- or down-shifted. Table 4-7 shows the destination control associated with I6:8. With any value of I6:8, and with an active (low) POE input, the Y-Output MUX outputs the F0:3 results over the Microprocessor Bus BD0:7.

Table 4-6. Source-Function Matrix for Microinstruction Bits I0:5*

ALU FUNCTION BITS I3:5 (OCTAL VALUE)		ALU SOURCE INPUT BITS I0:2 (OCTAL VALUE) AQ (0)	AB (1)	ZQ (2)	ZB (3)	ZA (4)	DA (5)	DQ (6)	DZ (7)
ADD (0)	R+S with CIN=0	A+Q	A+B	Q	B	A	D+A	D+Q	D
	R+S with CIN=1	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
SUBR (1)	S-R with CIN=0	Q-A-1	B-A-1	Q-1	B-1	A-1	A-D-1	Q-D-1	-D-1
	S-R with CIN=1	Q-A	B-A	Q	B	A	A-D	Q-D	-D
SUBS (2)	R-S with CIN=0	A-Q-1	A-B-1	-Q-1	-B-1	-A-1	D-A-1	D-Q-1	D-1
	R-S with CIN=1	A-Q	A-B	-Q	-B	-A	D-A	D-Q	D
OR (3)	R OR S	A OR Q	A OR B	Q	B	A	D OR A	D OR Q	D
AND (4)	R AND S	A AND Q	A AND B	0	0	0	D AND A	D AND Q	0
NRS (5)	NOT R AND S	$\overline{A}$ AND Q	$\overline{A}$ AND B	Q	B	A	$\overline{D}$ AND A	$\overline{D}$ AND Q	0
XOR (6)	R XOR S	A XOR Q	A XOR B	Q	B	A	D XOR A	D XOR Q	D
XNOR (7)	R XNOR S	$\overline{A \text{ XOR } Q}$	$\overline{A \text{ XOR } B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \text{ XOR } A}$	$\overline{D \text{ XOR } Q}$	$\overline{D}$

* This table is a combination of Tables 4-4 and 4-5. If necessary, refer to these tables for further detail.

Table 4-7. Microinstruction Bits I6:8 for ALU Destination Control*

I6:8 VALUE			OCTAL CODE	RAM SHIFTER IN/OUT		RAM FUNCTION		Q-SHIFTER IN/OUT		Q-REGISTER FUNCTION		COMMENTS
I8	I7	I6		RAM0	RAM3	SHIFT	LOAD	Q0	Q3	SHIFT	LOAD	
0	0	0	0	n/a	n/a	n/a	none	n/a	n/a	none	F to Q	Loads F0:3 to the Q-Register.
0	0	1	1	n/a	n/a	n/a	none	n/a	n/a	n/a	none	Generates BD0:3/BD4:7 output only if POE control input is low.
0	1	0	2	n/a	n/a	none	F to B	n/a	n/a	n/a	none	Generates BD0:3/BD4:7 output directly from a MicroRAM A-Register. F0:3 output is to a MicroRAM B-Register.
0	1	1	3	n/a	n/a	none	F to B	n/a	n/a	n/a	none	F0:3 output is to a MicroRAM B-Register.
1	0	0	4	F0	IN3	down	F/2 to B	Q0	IN3	down	Q/2 to Q	F0:3 output is down-shifted and input to a MicroRAM B-Register: F0 output, resulting from the down-shift of the less significant MicroRAM, wraps around as IN3 input to the MSB of the more significant MicroRAM. Q-Register output is down-shifted and again input to the Q-Register: Q0 output, resulting from the down-shift of the less significant Q-Register, wraps around as IN3 input to the more significant Q-Register.
1	0	1	5	F0	IN3	down	F/2 to B	Q0	n/a	n/a	none	F0:3 output is down-shifted and input to a MicroRAM B-Register as just discussed above.
1	1	0	6	IN0	F3	up	2xF to B	IN0	Q3	up	2xQ to Q	F0:3 output is up-shifted and input to a MicroRAM B-Register: F3 output, resulting from the up-shift of the more significant MicroRAM, wraps around as IN0 input to the LSB of the less significant MicroRAM. Q-Register output is up-shifted and again input to the Q-Register: Q3 output, resulting from the up-shift of the more significant Q-Register, wraps around as IN0 input to the less significant Q-Register.
1	1	1	7	IN0	F3	up	2xF to B	n/a	Q3	n/a	none	F0:3 output is up-shifted and input to the MicroRAM B-Register as just discussed above.

* Every I6:8 value generates a BD0:3/BD4:7 output, provided the POE input to the Y-Output MUX is low. The letters n/a (non-applicable) denote a "don't care" combination where the associated output is in a high-impedance state. (Specifically, the shift pin is a TTL input internally connected to a 3-state output in the high-impedance state.) The terms up and down respectively refer to a shift up towards the MSB or a shift down towards the LSB.

4-2.3 Microprogram Sequencer

As its name implies, the Microprogram Sequencer controls the sequence of microinstruction execution. Refer to the block diagram of Figure 3-6. To output the 10-bit address (PA0:8, SPA9) to PROM for the next microinstruction to be executed, the Microprogram Sequencer receives three inputs:

(1) Branch Address Bits (BRA0:9)
(2) Condition Code (CC)
(3) Sequencer Instruction Bits (SI0:3)

From the Pipeline Register, BRA0:9 supplies a 10-bit branch address for the next microinstruction to be executed by IDC controller circuitry. BRA0:9 can address all of the 1024 56-bit locations within Control Store PROM. The actual branch address, if any, depends on the CC and SI0:3 inputs. Alternately, instead of a branch address, BRA0:9 can supply a count value for iterations (repetitive executions) of a microinstruction loop.

CC supplies one of eight condition code tests used by the Microprogram Sequencer for a "next address" calculation. Table 4-3 describes the MA:MC bits associated with the CC.

SI0:3 specify one of sixteen possible sequencer instructions. These are described later in Section 4-2.3.1. (To more easily understand the following discussions, you might want to refer there now and scan Table 4-8 to gain an overview of these instructions.)

Figure 4-2 on the next page shows a functional block diagram of the Microprogram Sequencer. The following paragraphs discuss the functional blocks and I/O lines shown in the figure.

(a) Address/Down-Counter Register and Zero Detector

This register functions either as an Addess Register or a Down Counter. As an Address Register, it functions as a holding register to temporarily store a branch address from BRA0:9. Or, as a Down Counter, it controls microinstruction loop iterations. Specifically, BRA0:9 loads the register with a count value of one less than the wanted number of iterations. Before each successive execution of a microinstrution loop, the Zero Detector examines the count for a zero value; if not equal to zero, the count is decremented and the loop executes. This operation continues until a zero is detected, terminating loop execution. [The Decrement Repeat Loop (DRL), Decrement Repeat Instruction (DRI), and Three-Way Branch (TWB) sequencer instructions in Table 4-8 use the register as a Down Counter.]

The Address/Down-Counter Register is loaded with either of two sequencer instructions from Table 4-8: Load Counter (LDCT) or Push Conditional Load (PCL). LDCT explicitly loads the Down Counter Register with a count value from BRA0:9. PCL conditionally loads the Address Register with a branch address from BRA0:9.

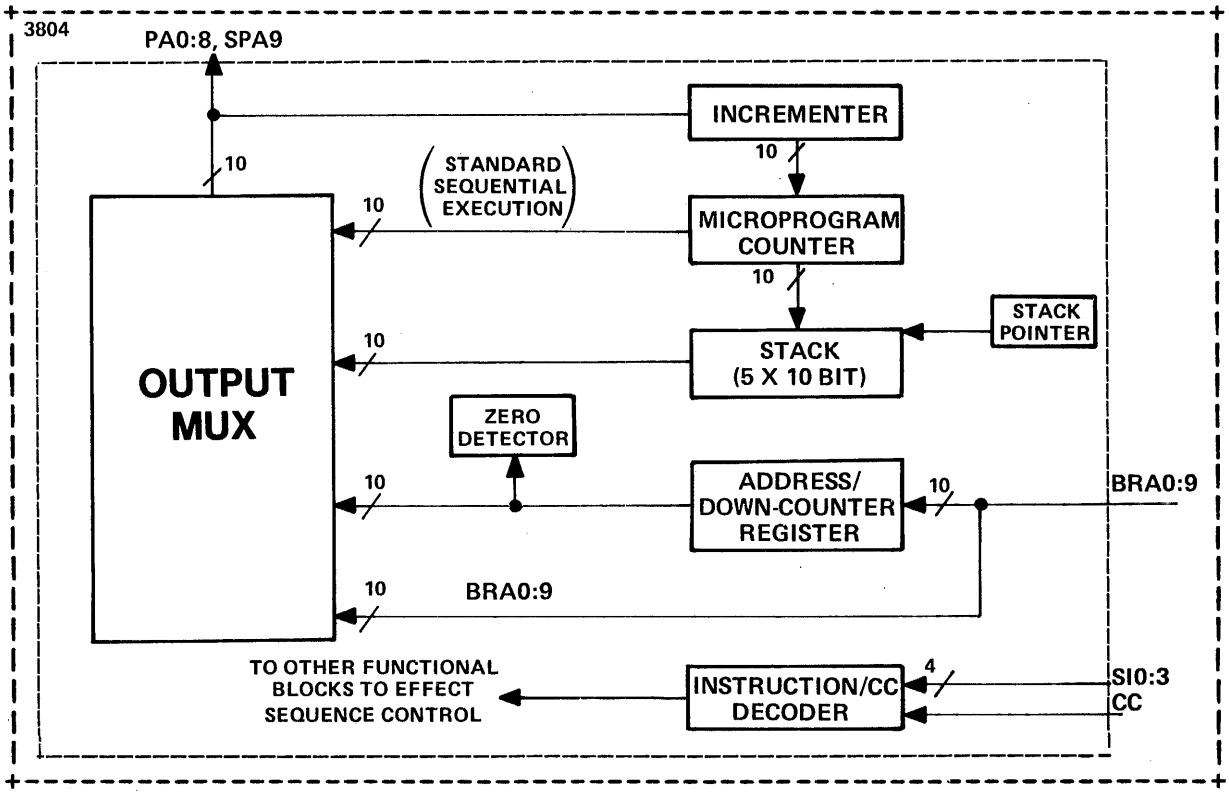


Figure 4-2. Block Diagram of the Microprogram Sequencer

(b) Incrementer

The 10-bit address from the Output MUX is always input to the Incrementer which increments the address by a value of one before passing it to the Microprogram Counter.

(c) Microprogram Counter

Once incremented, the 10-bit address from the Output MUX is stored in the Microprogram Counter. During standard sequential microinstruction execution, this functional block supplies the Output MUX with the address of the next microinstruction to be executed by the IDC logic.

(d) 5x10 Bit Stack with Stack Pointer

This functional block stores return addresses for subroutine calls. It is a 5-level First-In/First-Out (FIFO) stack with a Stack Pointer pointing to the top address. Return address inputs and outputs of this stack are performed by "push" and "pop" operations from the sequencer instructions. A push operation increments the Stack Pointer and pushes an address from the Microprogram Counter to the top-of-stack. (Should the stack be full when an address is pushed in, the current address at top-of-stack is overwritten and lost.) A pop operation decrements the Stack Pointer and "pops" the formerly current return address from the top-of-stack. [Push operations are performed by the Conditional Call (CC), Push Conditional Load (PCL), and Conditional Call 2 Places (CC2) sequencer instructions. Pop operations are performed by the Decrement Repeat Loop (DRL), Conditional Return (CR), Conditional Jump and Pop (CJP), Loop on Fail (LOOP), and Three-Way Branch (TWB) sequencer instructions.]

(e) Instruction/CC Decoder

This functional block receives the Sequence Instruction Bits (SI0:3) and Condition Code (CC) input that control other-than-standard sequencing of microinstruction execution. Section 4-2.3.1 discusses the sixteen possible sequencer instruction input from SI0:3. For information pertaining to the CC bit, refer to Table 4-3.

With the SI0:3 and CC inputs, the Instruction/CC Decoder outputs the sequence control signals to numerous points throughout the Microprogram Sequencer to effect sequence control.

(f) Output MUX

Depending on the sequencer instruction received via SI0:3, the Output MUX selects an address from one of four sources:

(1) BRA0:9 (direct data)
(2) Address Register
(3) Stack
(4) Microprogram Counter

For specific source inputs, refer to the list of sequencer instructions in Table 4-8.

4-2.3.1 Sequencer Instructions from SI0:3

Sequencer instructions are input to the Microprogram Sequencer through four lines: SI0:3. (As discussed in Section 4-2.1.5, SI0:3 are part of the 56-bit microinstruction output from Control Store PROM.) These four lines specify a hexadecimal code for one of sixteen sequencer instructions.

Table 4-8 lists and describes these instructions. By briefly scanning the descriptions in this table, you can see that a conditional pass or fail test is used frequently to effect various operations. A pass condition occurs when the CC input is low; a fail condition occurs when CC input is high.

Table 4-8. SI0:3 Input to Microprogram Sequencer

SI0:3 VALUE	INSTRUCTION NAME (MNEMONIC)	DESCRIPTION
0	Jump-to-Zero (JZ)	Used at power-up or initialization. As a result of this instruction, the address of the next microinstruction is zero, and the Stack Pointer resets to zero. The The Microprogram Counter now holds an address value of 0.
1	Conditional Call (CC)	A conditional call to a subroutine, depending on whether a condition passes or fails. If the condition passes, contents of the Microprogram Counter are pushed onto the Stack, and the microinstruction addressed by BRA0:9 is executed by the IDC logic. But if the condition fails, the next sequential instruction from the Microprogram Counter is executed by the IDC logic.
2	Unconditional Jump (JT)	An unconditional jump to the start of a new microprogram. As a result of this instruction, the microinstruction addressed by BRA0:9 is executed, and the Microprogram Counter is loaded with the BRA0:9 address plus one.
3	Conditional Jump Microcode (CJ)	A conditional jump or branch in microinstruction execution, depending on whether a condition passes or fails. If the condition passes, the microinstruction addressed by BRA0:9 is executed. If the condition fails, the next sequential instruction from the Microprogram Counter is executed.
4	Push, Conditional Load (PCL)	Used primarily to set-up loop execution. It causes the contents of the Microprogram Counter to be pushed onto the Stack. Then the condition is tested to determine if the Down Counter is to be loaded. If the condition passes, BRA0:9 contents are loaded into the Down Counter to become the count value. If the condition fails, the Down Counter is not loaded.
5	Conditional Call, 2 Places (CC2)	A conditional call to one of two subroutines, depending on whether a condition passes or fails. After the contents of the Microprogram Counter are pushed into the Stack, the condition is tested. If it passes, the subroutine addressed by BRA0:9 is executed; i.e., the Output MUX selects the BRA0:9 address. If the condition fails, the subroutine addressed by the Address Register is executed; i.e., the Output MUX selects the output of the Address Register.
6	Conditional Jump Map (CMAP)	A conditional jump or branch based on the input of BRA0:7 from Map PROM. The branch depends on a conditional test. If it passes, the next microinstruction addressed by BRA0:7 is executed. If it fails, the next sequential instruction from the Microprogram Coounter is executed.
7	Conditional Jump, 2 Places (CJ2)	A conditional jump or branch to one of two locations, depending on the conditional test results. (This instruction is like CC2 described above, but without a Stack push.) If the condition passes, the microinstruction addressed by BRA0:9 is executed. If it fails, the microinstruction at the address held by the Address Register is executed.
8	Decrement, Repeat Loop (DRL)	Repeats a microinstruction loop until Down Counter contents equal zero. Stack contains the starting address of the microinstruction loop. Before this instruction can execute, the Down Counter must have been loaded with a

Table 4-8. SIO:3 Input to Microprogram Sequencer (Continued)

SIO:3 VALUE	INSTRUCTION NAME (MNEMONIC)	DESCRIPTION
		value of one less than the wanted number of iterations. Before each loop, the Down Counter contents are examined: if contents do not equal zero, the Down Counter decrements and the address at top-of-stack executes; or, if contents equal zero, the Stack "pops" and the next sequential instruction from the Microprogram Counter executes.
9	Decrement, Repeat Instruction (DRI)	Repeats execution of a microinstruction until the Down Counter contents equal zero. BRA0:9 contain the address of the microinstruction to be repeatedly executed. Before this instruction can execute, the Down Counter must have been loaded with a value of one less than the wanted number of iterations. Before each repetitive execution, Down Counter contents are examined: if contents do not equal zero, the Down Counter decrements and the BRA0:9 address executes; if contents equal zero, the next sequential instruction from the Microprogram Counter executes.
A	Conditional Return (CR)	A conditional return from a subroutine to the microinstruction following the call to that subroutine. The return depends on a pass or fail condition. If the condition passes, the microinstruction given by the Stack Address is executed. If it fails, the next sequential instruction of the subroutine loop is executed; i.e., the Output MUX takes the microinstruction address from the Microprogram Counter.
B	Conditional Jump and Pop (CJP)	A conditional loop termination with Stack maintenance, depending on conditional testing. If the test passes, the Stack "pops" and the microinstruction addressed by BRA0:9 executes. If it fails, the next sequential microinstruction from the Microprogram Counter executes.
C	Load Counter (LDCT)	Loads the Down Counter with a count from BRA0:9 for subsequent loop iteration. It then executes the next sequential microinstruction from the Microprogram Counter.
D	Loop on Fail (LOOP)	Causes a loop to be executed for failure of a conditional test. That is, if the test fails, the microinstruction addressed by the contents of Stack is executed. If the test passes, the Stack pops and the microinstruction addressed by the Microprogram Counter executes.
E	No Operation (NOP)	A default instruction resulting in an increment of the Microprogram Counter contents and the execution of the next sequential microinstruction from the Microprogram Counter.
F	Three-Way Branch (TWB)	A conditional loop instruction that permits a branch to three possible microinstructions. Before TWB executes, the Down Counter is loaded with a count value, and the Stack has a branch address pushed in. During TWB execution, the Down Counter value decrements by one and a conditional test occurs. If the test passes, the next sequential microinstruction addressed from the Microprogram Counter executes; the Stack then pops. If the test fails, the Down Counter contents are examined: if contents do not equal zero, the microinstruction addressed by BRA0:9 executes and the Stackpops.

4-2.4 IDC Operational Cycle

The IDC is a sequential state machine with a 16-MHz clock as the basic timing signal. All other timing signals are either divisions of the 16-MHz clock or summations of divisions. Refer to the IDC schematics in Appendix B, to sheet 19B2 (sheet 19, grid coordinates B and 2). This sheet shows the 16-MHz oscillator of the IDC. Output from this oscillator is the OSC signal from which the other clock signals, also shown on sheet 19, are derived. For brief descriptions of the clock signals shown on this sheet, refer to the table of mnemonics in Appendix A.

An IDC operational cycle is 375 nanoseconds (ns), made up of six negative-going clock phases of 62.5 ns. Figure 4-3 illustrates this basic system timing. The following sections describe the IDC operations occurring for the operational phases of the IDC cycle.

4-2.4.1 IDC Instruction Decoding Phase (CLK1)

At the falling edge of CLK1, the Microprocessor (the two 4-Bit Slice Microprocessors) and the Microprogram Sequencer clock-in their respective fields of the 56-bit microinstruction. More specifically, the Microprocessor clocks-in the ALU instructions from I0:8, and the Microprogram Sequencer clocks-in the sequencer instructions from SI0:3. At the rising edge of CLK1, instruction decoding finishes. (Although there appears to be a conflict in the figure between the active CLK1 and the DMA Bus Low phases, internal decoding times associated with these phases absorb the contention.)

4-2.4.2 IDC Instruction Cycle

As shown in Figure 4-3, the IDC instruction cycle consists of three phases:

(1) Interal IDC Operation
(2) DMA Bus High
(3) DMA Bus Low

The following paragraphs discuss these phases of the instruction cycle.

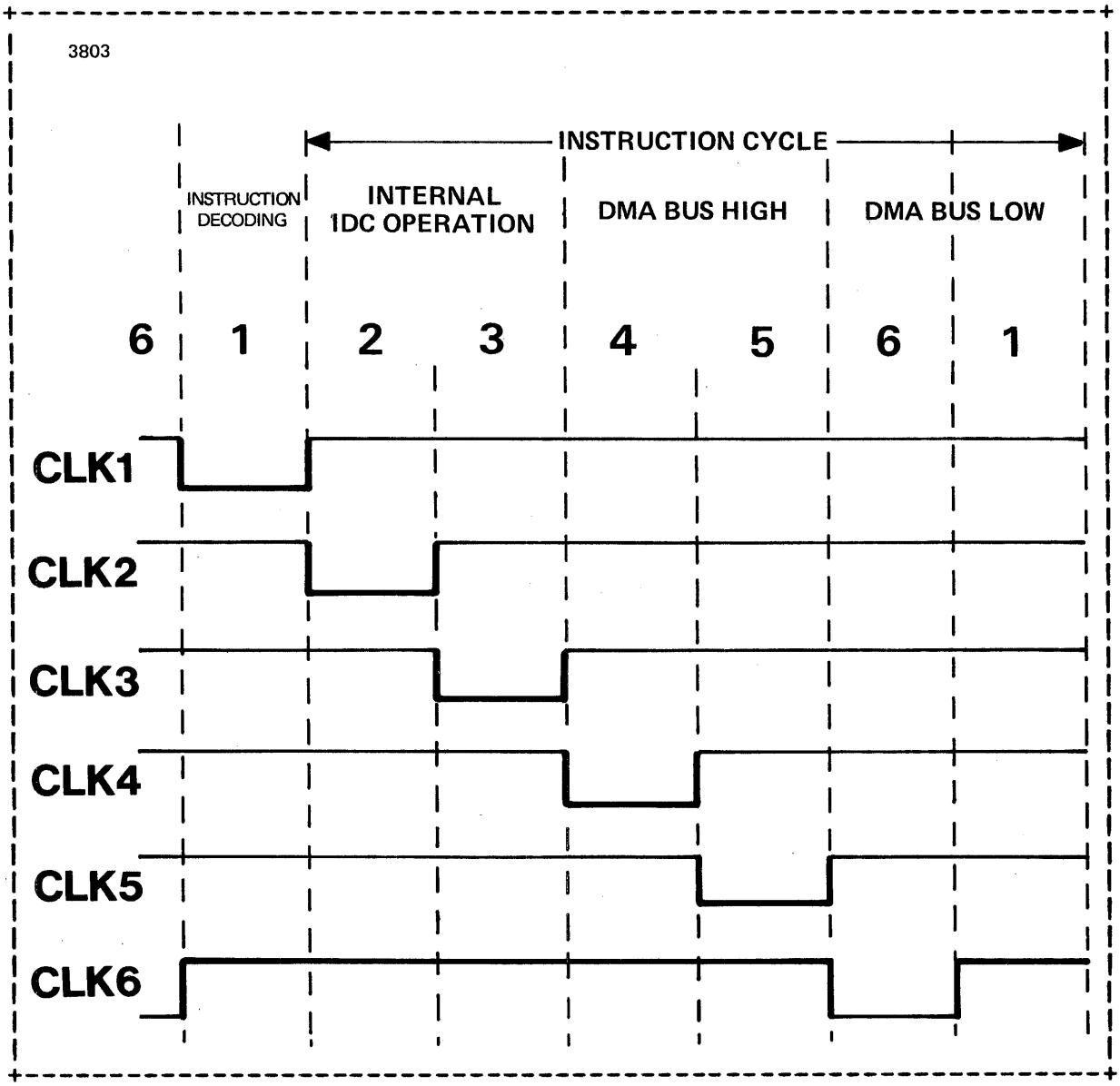


Figure 4-3. IDC Operational Cycle

(1) Internal IDC Operation

This phase, occurring during CLK23 (summation of CLK2 and CLK3), encompass IDC operations not directly related with a DMA transfer. During CLK23, the IDC RAM circuitry may be written or read with disk data. Also during CLK23, BDI00:5 functions are active. These functions control the source and destination of BD0:7 data and provide numerous control signals.

NOTE

As was shown in Table 4-2, under the MODE column, each bus function is a Read, a Write, or a Strobe. A Read signifies a data source; a Write, a destination; and a Strobe, a control signal.

The BD0:7 bus source, as determined by BDI00:5, can be the Serial-to-Parallel Converter, the General-Purpose Data Register, etc., as illustrated in Figure 3-6. During CLK23, the selected source data goes to the Microprocessor/Sequencer circuitry or to the RAM. The internal destinations and control strobes are active during CLK3. A destination can be the RAM Address Counter, the disk data bus, the disk control tag, or DMA circuitry. If the BDI00:5 function is a strobe, it performs one of the numerous control functions listed in Table 4-2.

(2) DMA Bus High, and
(3) DMA Bus Low

All DMA transfer is in halfword mode. Therefore, to transfer a halfword to/from the SELCH/MUX bus, two accesses with the IDC RAM circuitry are required: one access writes or reads the more significant (high) byte to or from RAM, and the other access writes or reads the less significant (low) byte to or from RAM.

If the DMA transfer is to the IDC, the IDC lines D00:15 receive a halfword from SELCH. IDC then stores this halfword into the DMA Data Register. (See Figure 3-6.) Thus, during CLK45 (sum of CLK4 and CLK5 phases), the high byte of data from the DMA Data Register is written to RAM. And, during CLK61 (sum of CLK6 and CLK1 phases), the low byte of data from the DMA Data Register is written to RAM.

If the DMA transfer is from the IDC, then the IDC lines D00:15 send a halfword of data to SELCH. As above, this data is first stored in the DMA Data Register. So, during CLK45 and CLK61 respectively, the high and low bytes of data are read to the DMA Data Register from RAM.

As evident from the preceding paragraphs, the IDC can simultaneously perform instruction execution and DMA transfer during one 375-ns operational cycle. In addition, during the internal IDC operational phase, the IDC can write or read a byte of data to or from a disk file. Consequently a DMA transfer to or from a disk file, via the IDC controller logic, does not need IDC microprogram intervention until the transfer ends. Or, stated in broader terms, one sector of data can be written to or read from a

disk file while, at the same time, a sector of data is transferred to or from the SELCH. During these simultaneous transfers, the microprocessor controller logic checks for track boundaries and DMA statuses.

4-2.5 Microprocessor/Sequencer Operation

At the start of an IDC operational cycle, with CLK6 going high, the ALU instructions on I0:8 and the sequencer instructions on SI0:3 are latched, respectively, into the Microprocessor and the Microprogram Sequencer. Concurrent with the latching of these inputs, the next 56-bit microinstruction is latched into the Pipeline Register.

The I0:8 and SI0:3 instructions decoded during the CLK1 phase are executed during the CLK23 phase. Also during CLK23, BDI00:5 contain a value whenever a microinstruction requires bus data I/O. When a data transfer from the Microprocessor onto BD0:7 is required, BDI00:5 determines either a source or a destination, but not both. See Table 4-2. If BDI00:5 determine a data source (Read Mode), the destination is the IDC RAM or the A/B registers of the ALU. If BDI00:5 determine a destination (Write Mode), the source is RAM, the ALU, or the Map PROM. Instead of determining a source read or a destination write, BDI00:5 can specify a control strobe.

The actual microinstruction latched into the Pipeline Register, as discussed in Section 4-2.3, depends on the CC and SI0:3 inputs and, depending on the particular sequencer instruction from SI0:3, the BRA0:9 input. These inputs alter the normal sequence of microinstruction execution. Normally, microinstructions are executed from sequential PROM locations unless the CC and SI0:3 inputs determine a branch address.

The following paragraphs present three examples of typical Microprocessor/Sequencer operation.

(1) Example 1

Objective:

Illustrate ALU-RAM interaction by adding the contents of an IDC RAM location to the contents of a Microprocessor B-Register.

Initial Conditions:

(a) I0:8 contain a value of 502. From Tables 4-4 thru 4-7 and Figure 4-1. A01:31 specifies register 4; B01:31 specifies register 4.

- 5 denotes an R-MUX source of LBD0:7 and an S-MUX source of A-Latch, which specifies MicroRAM Register 4.
- 0 denotes an ADD function of R-MUX input and S-MUX input.
- 3 denotes an output over BD0:7 and a load of the same output to a MicroRAM B-Register.

(b) RAM0:7 specify RAM address 87, the contents of which are to be added to B-Register 4.

(c) SI0:3 contain a value of X'E' for NOP.

(d) BDI00:5 contain a value of X'00' for NOP.

(e) BRA0:9 has no address.

Operational Sequence:

1. During CLK1, the Microprocessor decodes I0:8.

2. During CLK23, these RAM controls are asserted: RAM Page Address Bits (PAGE13,23) and RAM Chip Enable (CENB). These assertions result in the contents of RAM location 87 being read into BD0:7 as LBD0:7 input to the Microprocessor.

3. During CLK23, according to the I0:8 value of 503, the Microprocessor adds LBD0:7 input data to B-Register 4.

(2) Example 2

Objective:

Illustrate how the Microprocessor/Sequencer circuitry performs a branch within the microprogram.

Initial Conditions:

(a) I0:8 has a value of 001. From Tables 4-4 thru 4-7 and Figure 4-1:

- 0 denotes an R-MUX source of A-Latch and an S-MUX source of B-Latch.
- 0 denotes an ADD function of R-MUX input and S-MUX input.
- 1 denotes only an output onto BD0:7 from the ALU should POE be active.

(b) POE input is inactive, inhibiting BD0:7 output from the ALU. Hence, the I0:8 instruction is effectively a "no op."

(c) SI0:3 has a value of X'3' for a Conditional Jump (CJ).

(d) BRA0:9 specify PROM address 34 as the branch address for the conditional jump.

(e) CC is low to indicate a pass condition for RSEL.

Operational Sequence:

1. During CLK1, I0:8 and SI0:3 are decoded.
2. During the entire instruction cycle, RSEL is active (i.e., CC is enabled with a low) and BRA0:9 specifies the address.
3. During CIK23, the Microprogram Sequencer sees an enabled CC input and executes the SI0:3 input. The resulting 10-bit address output from the Microprogram Sequencer causes a PROM microprogram branch to address 34.

(3) Example 3

Objective:

Illustrate how BDI00:5 lines put data onto the BD0:7 bus and into a MicroRAM B-Register.

Initial Conditions:

(a) BDI00:5 has a value of X'0A' for an EDS signal to enable disk status.

(b) I0:8 has a value of 543. From Tables 4-4 thru 4-7 and Figure 4-1. A01:31 specifies register 3; B01:31 specifies register 3.

- 5 denotes an R-MUX source of LBD0:7 and an S-MUX source of A-Latch, which specifies ALU Register 3.
- 4 denotes an AND function of R-MUX input and S-MUX input.
- 3 denotes a load function of the resulting F0:F3 to a MicroRAM B-Register.

(c) SI0:3 have a value of X'E' for a NOP.

(d) RAM0:7 have no address.

(e) BRA0:9 have no address.

Operational Sequence:

1. During CLK1, the Microprocessor decodes ALU instruction 543.

2. During CLK23, the BDI00:5 function of EDS causes the contents of the Disk File Status Register to be output onto BD0:7 and to be input to the Microprocessor through LBD0:7.

3. During CLK23, execution of the ALU instruction ANDs two values: the disk status input from LBD0:7 and the contents of A-Register 3. The ANDed value is then stored into MicroRAM B-Register 3.

4-3 SELCH/MUX BUS INTERFACE

This portion of the IDC board interfaces the SELCH/MUX bus of a 3200-Series processor with the IDC controller logic. The bus interface works with the Microprocessor/Sequencer logic in generating the commands, data, and control sequences necessary for disk file I/O. I/O through the SELCH/MUX bus is either programmed or DMA. Section 4-3.1 discusses programmed I/O, and Section 4-3.2 discusses DMA I/O. For supplemental information on signal flow and mnemonics within these two sections, refer to the IDC block diagram of Figure 3-6, the table of mnemonics of Appendix A, and the 23 IDC schematic sheets of Appendix B.

4-3.1 Programmed I/O.

The SELCH/MUX bus interface supports the standard addressing functions:

- IDC or Disk File Address (ADRS)
- Receive Acknowledgment (RACK)

As illustrated in Figure 3-6, the IDC receives an ADRS0 signal into the Control Line Receivers. The Controller Address/File Address Compare and Select circuitry uses ADRS0 for the address comparison and selection. If the address input through D08:15 pertains to this IDC or to an attached file, either Equals Controller (=CONT) or Equals File (=FILE) is output accordingly. This output goes to the Function Encoding Circuits discussed later.

A received RACK0 signal, if applicable to this IDC, results in the bus interface gating the IDC address or a disk file address to the processor. That is, the Controller Address (CA8:15) or the File Address (FA8:15) is input to the Data MUX, where it is gated and output to the processor via the Data Transceivers. If this IDC has no interrupt pending, RACK0 is passed on out as TACK0.

In addition to the two addressing functions described above, the SELCH/MUX bus interface supports the four standard bus I/O functions:

- Status Request (SR)
- Output Command (OC)
- Data Request (DR)
- Data Available (DA)

As illustrated in Figure 3-6, the IDC receives an SR0, OC0, DR0, or DA0 signal into the Control Line Receivers, where they are output to the Control Line Latches. The latched signal is then output to the Function Encoding Circuits, which also receive the =CONT or =FILE input from the Controller Address/File Address Compare and Select circuitry. The encoding circuits AND the received inputs to generate an encoded (octal) signal over the IDC Function Lines (FUNC0:2). Table 4-9 lists the eight bus functions associated with FUNC0:2.

The assertion of one of the FUNC0:2 functions enables the Register Select (RSEL) signal from the Function Encoding Circuits. During the Microprocessor/Sequencer idle loop, microcode monitors RSEL. On finding RSEL enabled, the microcode acts on the encoded function, along with any associated input data, and performs the necessary operations. Afterwards, microcode responds with a Controller Sync (CONTSYNC) or File Sync (FILESYNC) to indicate successful completion of the received bus I/O function.

Table 4-9. FUNC0:2 Values for Encoded MUX Bus Functions*

FUNC0:2 VALUE	FUNCTION MNEMONIC	FUNCTION NAME
0	ILDR	Idle Controller Data Request
1	ILDA	Idle Controller Data Available
2	ILSR	Idle Controller Status Request
3	CLOC	Controller Latched Output Command
4	FLDR	File Data Request
5	FLDA	File Data Available
6	FLSR	File Status Request
7	FLOC	File Output Command

* FUNC0:2 output is an octal value corresponding to one of the eight functions. (FUNC2 is the most significant bit.) Refer to Appendix A for further description of the specified mnemonics.

Three of the bus functions -- SR0, DR0, and RACK0 -- require the IDC to respond with output data to the processor. MUX Control Bits (MUX13,23) select the particular register whose contents are to be transferred through the Data Transceivers. (Refer to Appendix A for a description of these bits.) The Enable MUX Output (EBLOUT) signal goes active to transmit this data. However, to ensure sufficient time for the register contents to be propagated through the Data MUX, EBLOUT goes active 50 ns after MUX13,23.

4-3.2 DMA I/O

Microprocessor/Sequencer microcode initiates DMA I/O, a halfword transfer, by generating DMA Start (DMASTRT). If the transfer is a read operation from IDC to SELCH, IDC RAM circuits are read in two sequences:

(1) Load High Byte (LDHIBYT) loads the more significant RAM byte into the DMA Register (chip 6F, sheet 5).

(2) Load Low Byte (LDLOBYT) loads the less significant RAM byte into the other DMA Register (chip 5F, sheet 5).

Once the RAM halfword is at the DMA Registers, SELCH Transfer (SELCHXFR) starts the DMA transfer over the SELCH/MUX bus.

If the transfer is a write operation from SELCH to IDC, the SELCHXFR signal first causes the received halfword to be loaded into the DMA Registers (Chips 7J and 5J, sheet 5). Then:

(1) Read High Byte (RDHIBYT) loads the more significant SELCH byte into RAM.

(2) Read Low Byte (RDLOBYT) loads the less significant SELCH byte into RAM.

Proper synchronization between SELCH and IDC for I/O is established by two DMA Transfer Flip-Flops (chip 17J, sheet 7). During the read operation from RAM to SELCH, these flip-flops ensure the sequential activation of the RAM and DMA transfer controls, as follows: RAMXFR, DMAXFR, RAMXFR, ... The less significant 17J flip-flop is initially set high by IDC Read (READ) to establish this sequence. During the write operation from SELCH to RAM, the flip-flops ensure the sequential activation of the DMA and RAM transfer controls, as follows: DMAXFR, RAMXFR, DMAXFR, ... The less significant 17J flip-flop is initially set low by IDC Write (WRITE) to establish this sequence.

Before any disk file read/write operation, the processor performs these operational steps to position the disk read/write heads to the proper track and to select a specified sector:

1. Writes the specified cylinder number to the selected disk file.

2. Issues a Seek command to the selected disk file.

3. Writes the specific head number to the selected disk file.

4. Issues a Set Head command to the selected disk file.

5. Writes the starting sector number to the IDC.

Refer to Section 4-4 for further discussion of the above operations. Sections 4-3.2.1 and 4-3.2.2 futher discuss the DMA read and write operations.

4-3.2.1 DMA Read Operation

Steps 1-10 below present the sequence of operations occurring with a DMA read, i.e., a read of a data sector from a disk file via IDC to SELCH. Figure 4-4 shows the timing signals involved with a DMA read operation; refer to Appendix A for further description of the mnemonics there.

1. IDC receives a Read command (a CMD0 function along with associated input data) from the processor. IDC then reads a previously specified sector into RAM page 1.

2. IDC receives a SELCH DR0 function.

3. Microprocessor/Sequencer microcode then asserts DMA Start (DMASTRT).

4. DMASTRT assertion sets the DMA Go (DMAGO) flip-flop and line, and resets the Last Word (LASTWRD) flip-flop. DMAGO starts the DMA transfer from RAM (i.e., RAMXFR goes active).

5. The Delayed DMA Go (DDMAGO) line ensures that the two bytes read from RAM are stored in the DMA Registers before being transferred to SELCH. During the RAMXFR operation, LDHIBYT loads the even RAM location of one byte to the DMA Register; LDLOBYT loads the odd RAM location of one byte to the other DMA Register.

6. To start the transfer to SELCH, provided a DR is asserted from SELCH, these signals go active: SELCHXFR, DMAXFR, and XFERSYNCH. RAMXFR goes inactive.

7. A Sync Return (SYN) is output to SELCH after successful completion of the SELCH DR function.

8. SELCHXFR remains asserted after the SYN output to prevent another DMA operation, just yet, for another SELCH DR0 reception. XFRSYNCH, DMAXFR, and SYN go inactive.

9. Transfer Done (XFRDONE) is asserted once the IDC completes another RAM transfer, inactivating SELCHXFR.

10. RAM transfer repeats, starting at step 6 above, for each additional SELCH DR0 function received.

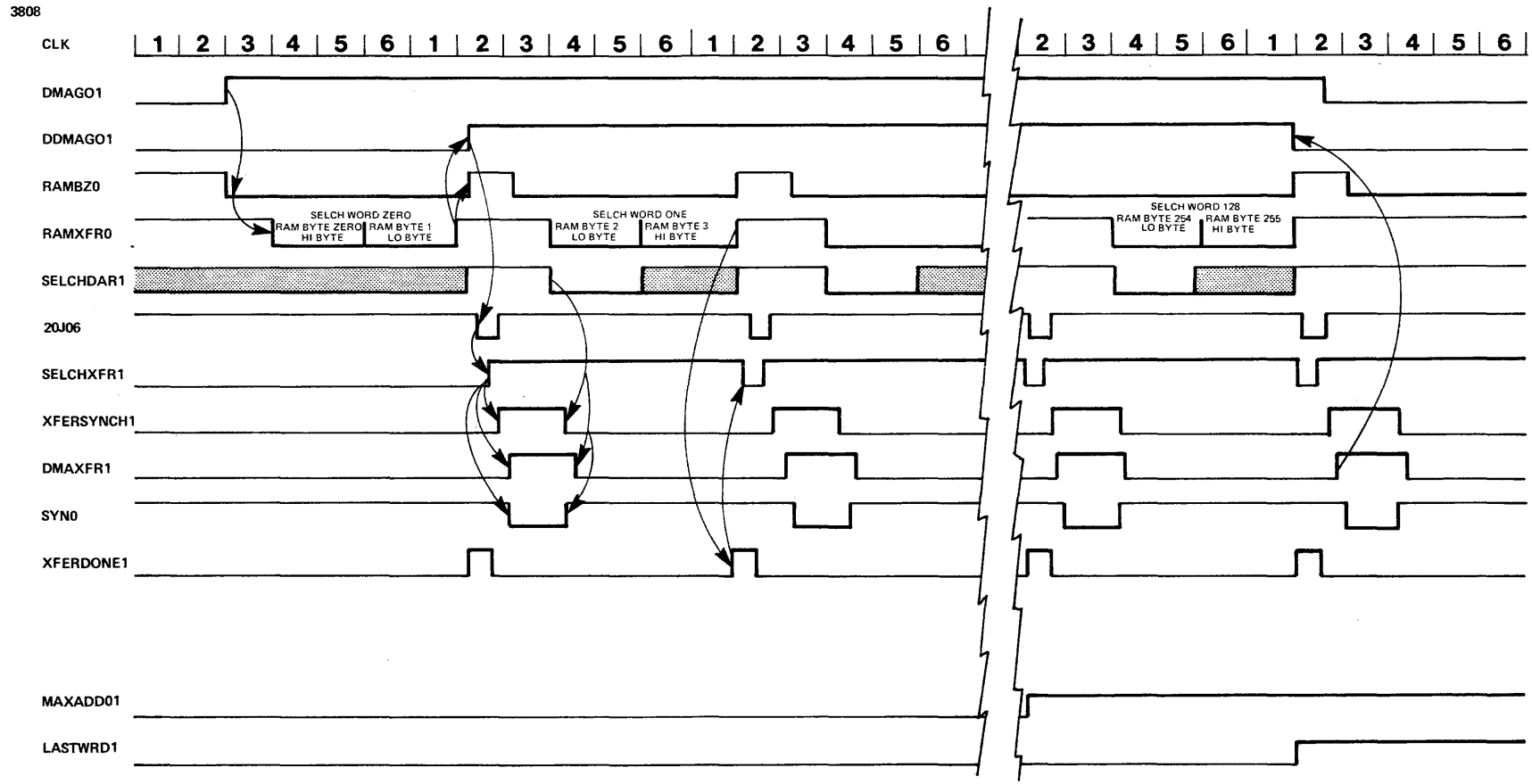


Figure 4-4. Timing Signals for a DMA Read Operation

Switching among RAM pages 1-3 during a DMA read operation is enabled with an active Maximum Sector Count (MAXADD). MAXADD indicates that all 256 bytes of the current RAM page have been read. Once MAXADD is active, another RAMXFR operation occurs to transfer the last halfword from the current RAM page to the DMA Registers. Then LASTWRD goes active, and a final DMAXFR occurs. Once this final halfword is transferred from the DMA Registers, DMAGO resets. Additional pages read from the disk file are transferred in the idential manner as discussed above.

A DMA read operation ends normally by an active Partial Transfer (PARTIAL). PARTIAL indicates nonreception of a SELCH DRO for 3 microseconds (us). More specifically, if the IDC receives no DRO from SELCH for 3 us during a DMA read operation, PARTIAL is asserted. Its assertion indicates a termination of SELCH transfer.

4-3.2.2 DMA Write Operation

Steps 1-10 below present the sequence of operations occurring with a DMA write, i.e., a write of a data sector to a disk file via IDC. Figure 4-5 shows the timing signals involved with a DMA write operation; refer to Appendix A for further description of the mnemonics.

1. IDC receives a Write command (CMDO function with associated data) from the processor.

2. IDC receives a SELCH DAO function.

3. Microprocessor/Sequencer microcode then asserts DMASTRT.

4. Step 3 sets DMAGO and resets LASTWRD. Activating DMAGO starts the DMA transfer from SELCH; i.e., SELCHXFR, DMAXFR, and XFRSYNCH go active.

5. Transfer Sync (XFRSYNCH) clocks SELCH DMA data into the DMA Registers.

6. A SYN is output to SELCH after successful completion of the SELCH DA function.

7. RAMXFR goes high: LDHIBYT loads the more significant byte of DMA data into the even RAM location; LDLOBYT loads the less significant byte of DMA data into the odd RAM location.

8. SELCHXFR remains asserted after the SYN output to prevent another DMA operation, just yet, for another SELCH DAO reception. XFRSYNCH, DMAXFR, and SYN go inactive.

9. XFRDONE activates, clearing SELCHXFR once both bytes are written into RAM.

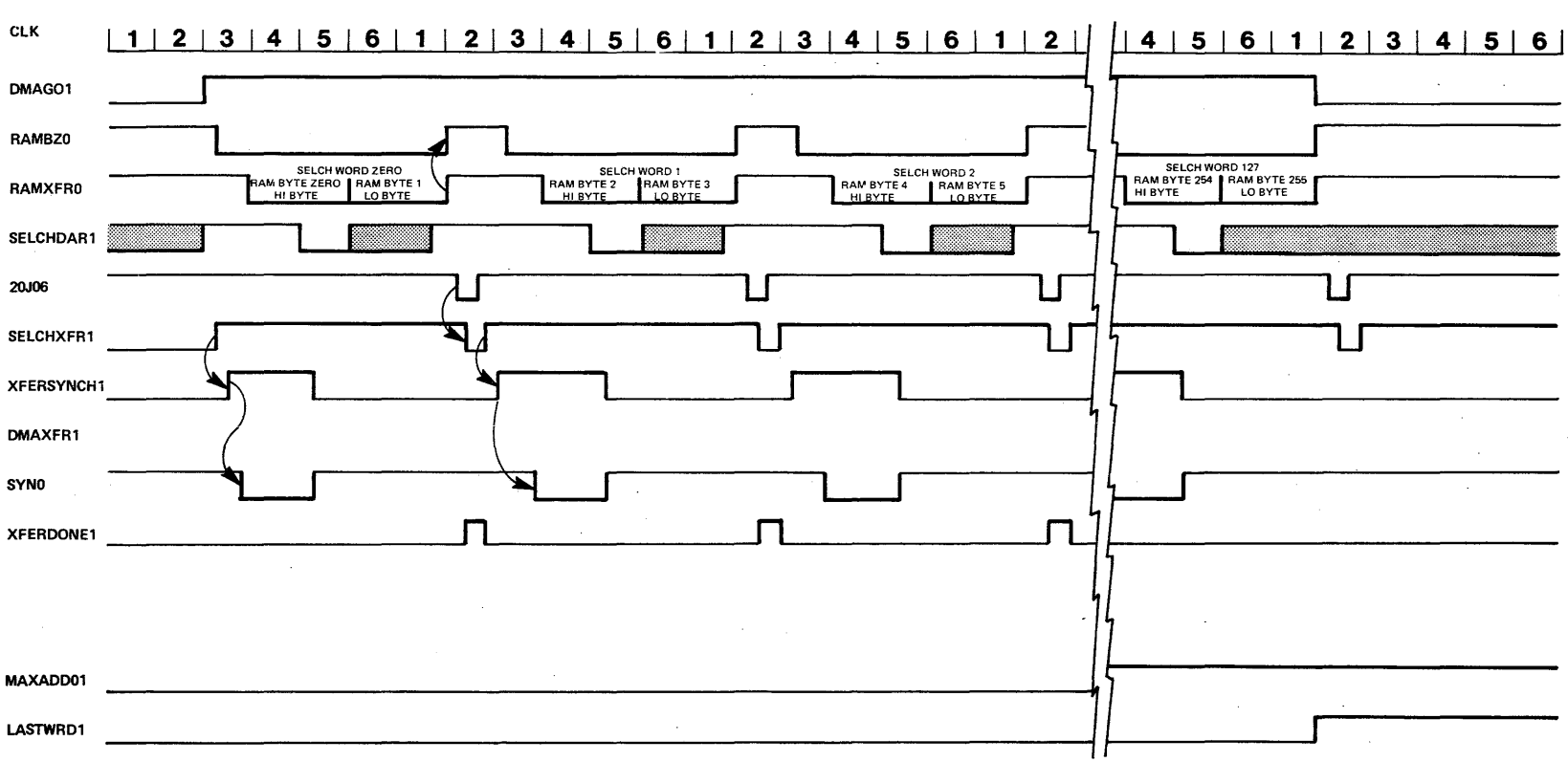


Figure 4-5. Timing Signals for a DMA Write Operation

10. DMA transfer repeats, starting from step 5, for each subsequently received SELCH DAO function.

Switching among RAM pages 1-3 during a DMA write operation is enabled with an active MAXADD, which indicates that 256 bytes have been written to the current RAM page. Once MAXADD is active, another RAMXFR operation occurs to transfer the last halfword from the DMA Register to RAM. This final transfer activates LASTWRD to stop the DMA. LASTWRD gated with WRITE inactivates DMAGO. Additional pages read from the DMA Registers are transferred in an identical manner.

A DMA write operation ends normally by an active PARTIAL, which indicates nonreception of a SELCH DAO for 3 us. That is, if the IDC receives no DAO from SELCH for 3 us during a DMA write operation, PARTIAL is asserted. Its assertion indicates a termination of SELCH transfer.

4-4 DISK FILE INTERFACE

This portion of the IDC board intefaces Perkin-Elmer disk files with the IDC controller logic. Specifically, it works with the Microprocessor/Sequencer logic to generate necessary control sequences, data, and Error Correction Code (ECC). Sections 4-4.1 thru 4-4.6 discuss the major operational areas required for disk file I/O. Figure 4-6 presents timing signals for the various control and address lines discussed in these sections. For supplemental descriptions, refer to Appendix A.

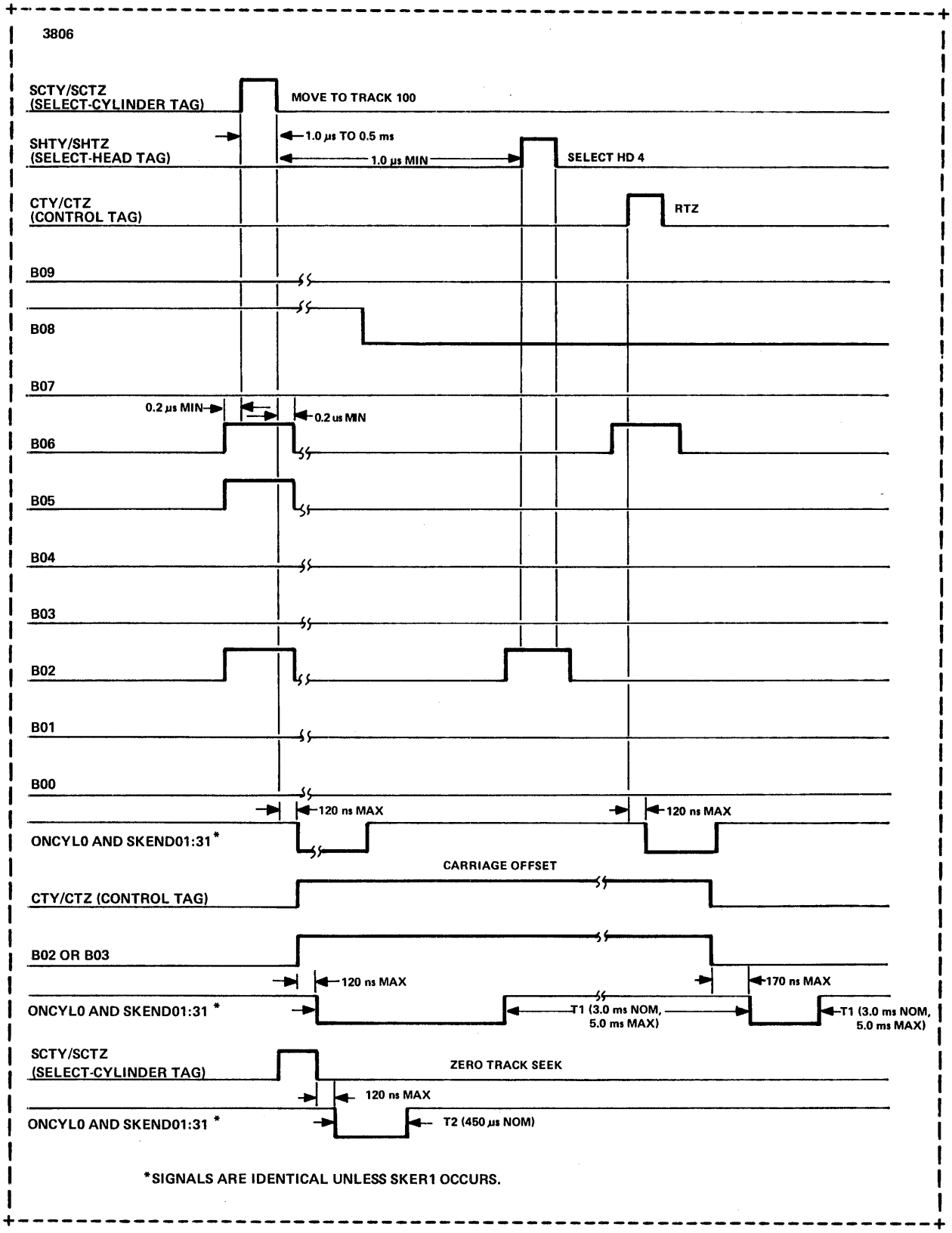


Figure 4-6. Tag and Bus Timing

4-4.1 Unit Selection

The first operation the interface must perform is disk file selection. To do this, the microcode places the unit select number (from RAM page 0) onto BD0:7. From BD0:7, the microcode-generated Select Pulse (SEL) loads the unit select number into the Disk File Number Flip-Flop (chip 23, sheet 17). The Dual Line Driver (chip 18A, sheet 17) puts the disk file number onto the A-cable Unit Select Lines (USEL0,USEL1). Next the microcode generates a Unit Select Tag (USTAG). To do this, the microcode generates BDI00:5 output specifying a Load Control Tag (LDCT) function; see Table 4-2. To ensure proper disk file selection, the microcode issues a BDI00:5 specifying an Enable Drive Select (ESE) function. This ESE latches the Unit Selected Tag (USEL0:3) and enables it as Disk File Selected (SEL0:3) onto BD0:7. Finally, the microcode compares SEL0:3 with the actual Driver Select Bits 13 and 23 (DRV13,23) value. They should match to indicate proper selection.

4-4.2 Selecting Disk File Cylinder and Head

The next operation in any read or write operation is to correctly position the disk file heads to the correct head and cylinder address. To position the heads, the microcode issues two BDI00:5 outputs: the first specifies a Load Disk Data Bus (LDCB); the second specifies an LDCT. The LDCB loads the head address, latched in the Load Disk Bus Register (chip 15E, sheet 14), to BD0:7 and transmits it over the A-cable. The LDCT sends a Select-Head Tag (SHT), latched in the Load Disk Control Tag Register (chip 16E, sheet 15), to BD0:7 and transmits it over the A-cable.

Likewise, to select the particular cylinder, microcode issues a BDI00:5 specifying an LDCB and another BDI00:5 specifying an LDCT for the Select Cylinder Tag (SCT). See Table 4-2. Since cylinder selection may take up to 65 milliseconds (ms), the IDC goes idle once the SCT is issued. The IDC is then free to perform another command if the processor should issue one. While in the idle state, the ALU checks for a Seek End (SKEND) from any disk file with the SHT in progress. To do this, the microcode issues a BDI00:5 Enable Seek End (ESE) and loads SKEND onto BD0:7 via the Selected Seek-End Register (chip 16C, sheet 15).

4-4.3 Disk File Status Check

When the processor requests a disk file status check, the IDC first ensures the particular disk file is currently selected. If that file is not selected, IDC selects it. The status of the disk file is latched by BDI00:5 Enable Disk Status (EDS) and put onto BD0:7 via the Enable Disk Status Register (chip 15C, sheet

14). The IDC then maps these status bits into the corresponding status bits for the 3200-Series processor.

4-4.4 Decoding Index and Sector Pulses

During various read/write operations, the IDC must decode Index (INX) and Sector (SECT) pulses. INX pulses received from the B-cable are multiplexed into the Disk Drive Index Pulse (INDEX) via the Selected Index MUX (chip 12A, sheet 16), depending on the selected disk file. Likewise, the SECT pulses from the B-cable are multiplexed into the Sector Pulse (SECTOR) via the Selected Sector MUX (chip 12A, sheet 17), according to the selected drive. INDEX and SECTOR are output onto BD0:7 under microprogram control via the Enabled Disk Status Register (chip 15C, sheet 14) and Disk Status Clear and Enable (DCL).

4-4.5 Disk File Read Data Path

Once disk file heads are positioned over the data field of the sector to be read, microcode activates the Read Gate (RGATE). Then, Read Data (RDAT) and Read Clock (RCLK) from the selected disk file are received through the B-cable. Data read from the disk is selected by the 8-to-1 MUX (chip 9A, sheet 16), emerging as Read/Write Clock (RWCLK).

SDATA is clocked into the Serial-to-Parallel Converter (chips 14K and 15K, sheet 18) by RWCLK. When a sync word is detected here, SYNC goes active to enable the Byte Synchronizer (chip 22R, sheet 7) to generate Data Register Ready (IPRDY). IPRDY indicates the Serial-to-Parallel Converter contains two bytes of data to be written to IDC RAM. Microcode, which monitors IPRDY, then generates XFERHI and XFERLO to enable the less significant and more significant byte of read data to be transferred over BD0:7 to the IDC RAM. This halfword transfer occurs repeatedly until a full sector of 256 bytes are read. The same serial data is also fed to the ECC circuitry (sheet 11) as Read Serial Disk Data (RSRO) for accumulation and comparison.

4-4.6 Disk File Write Data Path

When the heads are positioned over the data field of the sector to be written, microcode turns on the Write Gate (WGATE). At this time, the microcode will have filled the Parallel-to-Serial Converter (chips 14J and 15J, sheet 18) with the first two bytes of RAM data to be written to the sector. To fill the Parallel-to-Serial Converter with a halfword, microcode issues a BDI00:5 Transfer Low Byte (XFERLO) and Transfer High Byte (XFRHI). The less significant byte is loaded into the Write

Shift Register (chip 14F, sheet 18) from BD0:7. The more significant byte is loaded into the other half of the Write Shift Register (chip 15F, sheet 18) from BD0:7.

The Byte Synchronizer (chip 22R, sheet 7) generates Bit 151 Inverted (09R08) to control the loading and shifting of the Parallel-to-Serial Converter. When 09R08 is low and RWCLK jumps to high, data from chips 14F and 15F are loaded into the converter. When 09R08 is high and RWCLK jumps to high, data from the converter is serially shifted. Thus, the Serial-to-Parallel Register is loaded by RWCLK and shifted for fifteen RWCLK periods.

Data emerges from the registers as Write Serial Data (WSR) and goes to the Data 8-to-1 MUX (chip 9A, sheet 16). The asserted WGATE signal causes this data to emerge as Serial Read Data (SDATA). SDATA is fed into the Shift Register (chip 14K, sheet 18) and is shifted with RWCLK to produce RSR0. RSR0 now goes to the Data/ECC Selector (gate 18R01, sheet 7), where it emerges as WDATA to be sent to the selected disk file over the B-cable. WDATA is also fed to the ECC Input (gate 16R04, sheet 11), where it is used to form the ECC.

The parallel-to-serial halfword transfer repeats until 256 bytes of data are written to the sector. Microcode then enables ECC Feedback Bit 31 (ECC31), the output of the ECC Registers, onto the WDATA line. Consequently, the 32-bit ECC is appended to the sector of write data.

4-5 ERROR CORRECTION CODE (ECC) CIRCUITRY

This circuitry, although part of the IDC controller Logic of Figure 3-6, is discussed here, after the disk file interface, because of its logical association.

The ECC circuitry shown on Sheet 11 of Appendix B uses this formula to generate a 32-bit ECC:

$$X^{32} + X^{23} + X^{21} + X^{11} + X^{2} + 1$$

During a write operation, the ECC circuitry appends the generated ECC to the sector written to a selected disk file. During a read operation, the ECC circuitry compares the generated ECC with the ECC appended to the sector read from the selected disk. Whenever a mismatch occurs during this comparison, the ECC Error Detection Bit (BITSR) becomes active (low).

The following operations occur for ECC generation during a disk file write:

1. The ECC Registers (sheet 11) are initialized by a shift of

32 0-bits from the Phase Lock Oscillator (PLO) field of the formatted disk media.

2. Microcode sets the Accumulate ECC (ACCECC) signal.

3. Serial Data (RSRO) to be written to a disk sector is fed through the ECC Registers. The first 1-bit input sets ECC contents according to the above generation formula; i.e., the first 1-bit sets the 32nd, 23rd, 21st, 11th, and 2nd flip-flops.

4. Each additional bit causes mixing, or accumulation.

5. Once the ECC Registers accumulate the last bit of the sector to be written, microcode asserts ECC Off (OFF) to place the registers into the shift mode. Consequently, the ECC is appended to the written sector.

The following operations occur for ECC generation/comparison during a disk file read:

1. The ECC Registers (sheet 11) are initialized by a shift of 32 0-bits from the Phase Lock Oscillator (PLO) field of the formatted disk media.

2. Microcode sets the Accumulate ECC (ACCECC) signal.

3. Serial Data (RSRO) read from a disk sector is fed through the ECC Registers. ECC accumulation begins with the first 1-bit after the sector sync word. This bit sets ECC contents according to the above generation formula.

4. Each additional bit causes mixing, or accumulation.

5. Once the ECC Register accumulates the last bit of the read sector, the ECC appended to that sector is compared to the newly accumulated ECC. The comparison is accomplished by shifting the 32-bit ECC into the ECC Registers.

6. If the two ECCs match, BITSR remains inactive (high) and the ECC Registers contain only zeros. The current sector, just loaded into IDC RAM, is enabled for DMA transfer.

7. If the two ECCs mismatch, indicating an ECC error, BITSR goes active (low) and the ECC Register contents are non-zero.

8. Microcode automatically rereads the same sector. If the error persists, microcode implements ECC operation as discussed below.

9. To internally correct an ECC error of 11 bits or less, the microcode:

a. Generates BDI00:5 Load ECC Low (ECCLO), which results in ECC21:23 being read onto BD5:7 of the BD0:7 bus. (See Table 4-2, BDI00:5 value X'02'.) These three "syndrome" bits, needed to perform the correction, are stored in RAM.

b. Generates BDI00:5 Load ECC High (ECCHI), which results in ECC24:31 being read on to BD0:7. (See Table 4-2, BDI00:5 value X'03'.) These eight syndrome bits, needed to perform the correction, are also stored in RAM.

c. Shifts the ECC Register, still containing the syndrome bits, 40,907 times to initialize it to the first bit position of the read sector, which is now in the current RAM page.

d. Shifts the ECC Register one bit at a time -- up to 2,048 bit shifts. After each shift, microcode examines BITSR for a low (error) setting:

   If BITSR is low, the microcode ORs the ECC21:31 syndrome bits with eleven bits in RAM, starting at the same bit position. This operation implements the correction. Execution now repeats from step (5).

   If BITSR is not found as low throughout the 2,048 shifts, an additional 32 bit shifts are examined to see if the error occured in the 32-bit ECC itself. If BITSR equals low here, the error occurred in the ECC, thus the data was read correctly; execution repeats from step 5. However, if BITSR is still not found as low, an uncorrectable ECC error exists. The IDC controller status will be set to X'0B'. Refer to Perkin-Elmer Publication 50-007 for further description of this status.

APPENDIX A

TABLE OF IDC MNEMONICS

The following pages contain the mnemonics found in the IDC schematics of Appendix B and discussed throughout Chapters 1 thru 4 of this manual. The SOURCE column in this table specifies the sheet number and grid coordinates of the location for each mnemonic.

MNEMONIC	SOURCE	NAME	COMMENT
ACCECC1	7C4	Accumulate ECC	Allows ECC generation.
ADRS01	3B8	IDC or Disk File Address	Input from the processor to select a device (IDC or disk file) for an I/O operation. Data bits D080:150 contain this address.
ADRS1	3D8	Received ADRS0	Indicates an active ADRS0 signal.
ADRSYN0	3N9	Address Sync	A sync return for address selection.
AE/OE1	8L4	RAM Address Enable	Gates the address lines to the RAM. That is, it selects the RAM address source: a high selects RAM0:7 from the Pipeline Register, or a low selects RAM0:7 from the RAM Address Counter.
ANYCRY1	13M1	Carry into ALU	The carry generated from the previous ALU cycle or or the microcode.
AR01:31	9H2	ALU A-Register Selection Bits 0-3	A01:31 before the Pipeline Register.
ASERV000:30	17D5	Disk Drive Write Clocks 0-3	Output to disk files.
ATN01	3M3	Attention	Output to the processor to signal an interrupt pending.
A01:31	9M2	A-Register Address Bits 0-3	A 4-bit binary value for selecting one of the ALU registers as the source A-register.
BAOE1	13C9	Inverted RAM Address Enable	AE/OE1 inverted.
BD01:71	12C6	8-Bit Microprocessor Data Bus	The main data path among the functional blocks of the IDC. It buses various data and control bytes.
BDIO01:51	8M9	Bus Data I/O and Control Bits 0-5	A 6-bit code that controls the source and destination for BD0:7 and provides numerous control signals. Refer to Table 4-2 for detailed description.
BITON0	6B1	Masked CC Bit	Masked condition-code bit of the disk file status.
BIT151	7F3	Carry Bit 15	Carry bit from the Serial-to-Parallel Converter for synchronizing microprocessor data with serial disk data.

MNEMONIC	SOURCE	NAME	COMMENT
BITSR01	11L2	ECC Error Detection Bit	A zero indicates a data read error.
BL	6K8	Reset SELCH Transfer	Terminates DMA transfer to/from SELCH.
BRA01:91	10L6	Branch Address Bits 0-9	A 10-bit branch address to the Microprogram Sequencer. When output from the Pipeline Register, BRA0:9 specify the location of the next microinstruction to branch to. BRA0:9 also load the Microprogram Sequencer with a count value for loop iteration. When output from the Map PROM, BRA0:7 provide constant data or a branch address for a map jump.
BUSAOE0	13D9	LDR Counter RAM Address	Selects the LDR Counter as the RAM address.
BUSSW0	6G3	Bus Switch	Output to SELCH to indicate IDC support for the "new" high-speed SELCH protocol, with an I/O Bus Switch. Pins W1 and W3 on the IDC board should be strapped for this support.
BUSYA1,B1	14A6	Differential Dual-Port Busy	Informs this IDC that a disk file has been acquired by another IDC. (Applicable only to dual-port operation.)
BUSY1	14D6	Busy Signal	Received from disk file.
B00Y1,B00Z1 thru B10Y1,B10Z1	14M-, 15M-	Differential Data Bus Bits 0-10	Output to disk files for control and address data. B10Y1,B10Z1 is a spare. These lines are alternately referred to as B00:10. Refer to Tables 3-1 and 3-2 for further description.
B01:31	9M5	B-Register Address Bits 0-3	A 4-bit binary value for selecting one of the ALU registers as the source/destination B-register.
CARRY31	12C3	Carry Bit 3	Carry-out associated with the last operation of of the less significant ALU slice.
CARRY71	12E3	Carry Bit 7	Carry-out associated with the last operation of the more significant ALU slice.
CA081:151	3C2-	Controller Address Bits 8-15	IDC address (of this controller) to be sent as MD08:15 input to the Data Transceivers or to the processor along with the SYN0 signal.

MNEMONIC	SOURCE	NAME	COMMENT
CBIT0	14J2	Data Bit 0	With CTAG3, it indicates an ongoing write operation to a disk file; i.e., when both CTAG3 and CBIT are high, a write is in progress.
CBIT1	14J2	Data Bit 1	With CTAG3, it indicates an ongoing read operation to disk file; i.e., when both CTAG3 and CBIT are high, a read is in progress.
CCLK0	19D3	Gated 10-MHz Clock	Used to generate timing signals within the IDC.
CCMUXP1	6D2	CC MUX Output	The multiplexed condition code resulting from the disk file status.
CC0	12H1	Condition Code	Indicates a pass or fail for one of eight conditions. The Microprogram Sequencer uses CC for a "next address" calculation, like a conditional branch or return. See MA:MC.
CENB0	12L8	RAM Chip Enable	Enables RAM output onto BD0:7.
CINTCLR0	10J3	Internal Clear	Resets SECTOV, the Watchdog Timer, and various statuses of the IDC.
CINT1	4L6	Controller Interrupt	Indicates the controller portion of the IDC is generating an interrupt to the processor.
CIN1	9M9	Carry-In	Microcode-generated carry input to the ALU.
CLK10:60	19J2	Clock Phases 1-6	One of six 62.5-ns phases of the 375-ns IDC cycle.
CLK12D0	19K3	Delayed Clock Phase 1/2	Delayed summation of CLK10 and CLK20.
CLK12345D1	19G1	Delayed Clock Phase 1-5	The clock phase feedback to the input stage of the Clock Generator to regenerate the other clock signals.
CLK150,151	19M2	Clock Phase 1/5	Summation of CLK10 and CLK50.
CLK230,231	19M3	Clock Phase 2/3	Summation of CLK20 and CLK30.
CLK34D0	19K3	Delayed Clock Phase 3/4	Delayed summation of CLK30 and CLK40.
CLK450,451	19M3	Clock Phase 4/5	Summation of CLK40 and CLK50.

MNEMONIC	SOURCE	NAME	COMMENT
CLK641	19K2	Clock Phase 6/4	Summation of CLK60 and CLK40.
CLOC0	3L6	Controller Latched Output Command	Indicates a received CMD0 signal from the processor, e.g., Read, Write, or Format Sector.
CLO701	3B9	Early Power Failure	Input from the processor to signal an imminent power failure.
CMD01	3J4	Command	Input from the processor to signal the presence of a command on data bits D080:150.
CNT1	8L6	RAM Page Counter Enable	When high, it enables the RAM Page Counter to increment to the next page.
=CONT	3E6	Equals Controller	Indicates that the received controller address matches the address of this IDC. Also, it indicates that the FUNC0:2 bits apply to this selected IDC.
CONTACK0	4N5	Controller Acknowledge	An acknowledgment from the processor for the controller address of this IDC.
CONTSEL1	3H6	Controller Selected	Indicates the processor has selected the controller address of this IDC.
CONTSYNC0	3E8	Controller Sync Return	Indicates the IDC has properly accepted and responded to a control line signal.
CON0	5M5	Microcode Clear to Zero	Internally resets the IDC and causes the microcode to go to zero.
CRST0	19F7	Controller Reset	Either an EXTCLR or an OCRST.
CTAG31	15J8	Control Tag 3	Causes execution of the disk file function associated with the contents of B00:B09. See Table 3-1.
CTLOPTCL1	3F5	Controller in Optional Protocol	See OPTPTCL1.
CTY1,Z1	15M-	Differential Control Tag	Output to disk files to indicate that bus lines B00:09 are supplying a driver command.

MNEMONIC	SOURCE	NAME	COMMENT
DAR1	7H7	Data Available or Requested	Indicates a DA0 or a DR0 received from the SELCH during a DMA.
DATA001:071	5G2-	Data Bits 0-7	More significant byte of DMA data to be sent to SELCH.
DATA081:151	5G5-	Data Bits 8-15	Less significant byte of DMA data to be sent to SELCH.
DA01	3J2	Data Available	Input from processor or SELCH to inform the IDC of a write operation to the selected IDC or disk file. Data is available on data bits D000:150.
DA1	3K2	DA0 Received	Output resulting from a DA0 input.
DCL0	5M7	Disk Status Clear and Enable	Clears various counters and registers associated with the disk file interface.
DDMAGO0,1	6C7	Delayed DMA Go	A delayed DMAGO signal -- a one-buffer delay on a read operation.
DE0	5K3	Data Enable	Reads the Map PROM Register to BD0:7.
DLYSUS1	6L9	Delay 3 Microseconds	Sets Partial Flip-Flop if SELCHDAR1 is not received within 3 us and if the Partial Counter is not enabled.
DLYSYNC0	6M2	Delayed Sync Return	Either the DMA sync signal to the SELCH (resulting from SELCHSYN) or the interrupt-acknowledgment signal (resulting from OURACK0) to the processor.
DMAGO0,1	6J6	DMA Go	Indicates that the IDC is performing a DMA transfer to the SELCH.
DMASR0	6H1	DMA Status Request	A status request from the SELCH to this idle IDC.
DMASTRT0	5M5	DMA Start	Microcode bit to start DMA operation. It sets the DMAGO Flip-Flop and resets the LASTWRD Flip-Flop.
DMAXFR1	6S5	DMA Transfer	Indicates an ongoing DMA transfer.
DMA130,230	12K8	DMA Bits 13 and 23	DMA RAM-page bits, encoded.

MNEMONIC	SOURCE	NAME	COMMENT
DRV131:231	17K4	Drive Select Bits 13 and 23	Two binary bits to select one of four disk files.
DRO1	3J2	Data Request	Input from procesor or SELCH to inform the IDC of a read operation from the selected IDC or disk file. Data is requested from D000:150.
DR1	3K1	DRO Received	Output resulting from DRO input.
DSBCRY0	13J1	Disable Carry	Clears CARRY7.
D000:150	4E-	Data Bits 0-15	I/O consisting of data, an address, a command, or a status.
D001:151	4E-	Received-Data Bits 0-15	Output corresponding to D000:150 for received data from the SELCH/MUX bus.
EBLD01:41	5J7	Enable-Decoder Bits 0-4	Select one of the five BDIO Decoders (the 3-8 decoders).
EBLOUT0	4G3	Enable MUX Output	Enables MUX bus data output, i.e., sets the transceiver mode to transmit or receive.
EBLPRTL1	6H9	Fnable Partial	Enables the Partial Counter to determine if a partial DMA has occurred.
EBLTCLK0	14D9	Enable Clock	Can be used in an IDC developmental system to disable the 16-MHz clock and to enable TSTCLK.
ECCCLK1	7M3	ECC Clock	Clock to ECC circuitry for generating correction code.
ECCHI0	5K3	Load ECC High	Indicates the more significant byte of the ECC syndrome is loaded onto BD0:7. Specifically, it reads ECC24:31 to BD0:7.
ECCLO0	5K3	Load ECC Low	Indicates the less significant byte of the ECC syndrome is loaded onto BD0:7. Specifically, it reads ECC21:23 to BD5:7.
ECC001:311	11-	ECC Output Bits 0-21	The 32 bits of the ECC Generator.
ECC311	11A6	ECC Feedback Bit 31	The 32nd bit of ECC fed back into ECC circuitry.

MNEMONIC	SOURCE	NAME	COMMENT
EDS0	5K5	Enable Disk Status	Indicates that the Disk File Status Register is loaded onto BD0:7.
EOXFR1	6R4	End of Transfer	Inverted PARTIAL0 input.
ESE0	5K5	Enable Seek End and Drive Select	Indicates that the Seek-End/Drive-Select Register is loaded onto BD0:7.
ESTBRA0	5K6	Establish Branch Address	Enables disk status into the Condition Code MUX.
EXTCLK1	19C4	External Clock	A test clock signal associated with TSTCLK0.
EXTCLR0	3H7	External Clear	An externally generated IDC reset resulting from the ORing of three signals: TESTCLR0, SCLR0, and CL070.
FAULTA1,B1	14A1	Differential Fault	Input indicating a fault condition at a disk file.
FAULT1	14D2	Disk Drive Fault	Indicates that the selected disk file is experiencing a fault condition.
FA081:151	3G1	File Address Bits 8-15	File address to be sent as MD081:151 input to the Data Transceivers, or to be sent to the processor along with the sync signal SYN0.
FILEACK0	4N6	File Address Acknowledge	An acknowledgment from the processor for one of the disk file addresses of this IDC.
FILESEL1	3J7	File Selected	Indicates the processor has selected one of the disk file addresses of this IDC.
FILESYNC0	3L9	File Sync Return	Indicates that an attached disk file has properly accepted and responded to a control line signal.
=FILE1	3F6	Equals File	Indicates that the received file address matches the address of a disk file at the IDC. It also indicates that the FUNC0:2 bits apply to a selected disk file.
FILE130,131 and FILE230,231	3H8-	File Address Bits 13 and 23	Two binary bits with one of the four disk file addresses (0-3).

MNEMONIC	SOURCE	NAME	COMMENT
FINT1	4L6	File Interrupt	Indicates a disk file is generating an interrupt to the processor.
FLDA0	3L7	File Data Available	Indicates a disk file received a DA0 signal from the processor. The data available is the cylinder or head address of the currently selected disk file.
FLDR0	3L7	File Data Request	Indicates a disk file received a DR0 signal from the processor. Consequently, the disk file returns an RPS or an X'FE' to the processor.
FLOC0	3L8	File Output Command	Indicates a disk file received a CMD0 signal from the processor, e.g., Seek, Set Head, or RTZ.
FLSR0	3L7	File Status Request	Indicates a disk file received an SR0 signal from the processor. As a result, the IDC returns the status of the currently selected disk file.
FMTENBL1	3G6	Format Enabled	Indicates that toggle-8 of the File-0 Address Switch is pushed down to the 1-position to enable IDC formatting.
FOUND0	5M8	Sector Found	Test point to indicate whether or not the IDC has found the sector to be writtten to or read from.
FUNC00:20	3N6	IDC Function Lines 0-2	One of eight encoded functions output to BD0:7. See Table 4-9.
F=0	12F2	Function Equals Zero	Indicates ALU computation equals zero.
GME0	12K1	Gated Map PROM Enable	Enables the Map PROM outputs onto BRA0:7.
GOTO00	19M6	Go to Address Zero	Forces microcode to address zero.
GPD081:151	5F9	General-Purpose Data Bits 8-15	Control data to be sent as MD081:151 input to the Data Transceivers.
HOLD0/PICK0	17K2	Power Sequence Hold/Pick	Two lines with which the processor "picks and holds" the power sequencing capability for disk files in the remote mode. When the processor is turned on, IDC logic applies a ground to these lines to sequentially power-up the attached disk files.

MNEMONIC	SOURCE	NAME	COMMENT
HWO	6F2	Halfword Mode	Output to SELCH indicating that this IDC is a halfword-oriented device.
IDLE0,1	6D9	Controller Idle	Indicates IDC not performing any operation.
ILDA0	3L5	Idle Controller Data Available a	Indicates a received DA0 signal from the processor while the IDC was idle. Specifically, it indicates the processor has data (sector number) to be written to the IDC.
ILDR0	3L5	Idle Controller Data Request	Indicates a received DR0 signal from the processor while the IDC was idle. Serves no function; just results in zero being returned to the processor.
ILSR0	3L6	Idle Controller Status Request	Indicates a received SR0 signal from the processor while the IDC was idle. It directs the IDC to return the current IDC status to the processor.
INDEX1	16M2	Disk-Drive Index Pulse	Indicates that the index pulse is being received from the selected disk file.
INGPG1	13C8	Enable Page Counter Increment	Enables the Page Counter to be incremented while sectors are read from a disk file.
INTCLK1	19C3	Internal Clock	A 16-MHz signal associated with OSC0.
INTCLR0	10M3	Internal Clear	Internally generated IDC reset signal.
INTDATA0	5M5	Interrupt Data	Loads Interrupt Register with data.
INTREQ1	4K3	Interrupt Request	Indicates that this IDC is requesting an interrupt from the processor.
INX0A1,0B1 thru INX3A1,3B1	16H1-	Differential Index	Input from a disk file to mark the leading edge of sector zero for every disk revolution.
IPRDY1	7F4	Data Register Ready	For a read it indicates the Serial-to-Parallel Converter contains the two bytes of data written to the IDC RAM. For write, it indicates the Parallel-to-Serial Converter is empty.

MNEMONIC	SOURCE	NAME	COMMENT
IPRY0,1	3M4	Input Ready	Indicates the Write Shift Register (WSR) is filled or that the Read Shift Register (RSR) is emptied.
I01:81	9N6	ALU Instruction Bits 0-8	The nine instruction bits required by the ALU to perform an operation. See Tables 4-4 thru 4-7 for further description.
LASTDA0	6J5	Last Data Available	Indicates the last DA0 signal received from SELCH during a DMA transfer.
LASTWRD1	6K7	DMA Last Halfword	Indicates the last halfword of a sector is being DMAed via SELCH.
LBD01:71	12K1	Latched Bus Data Bits 0-7	Latched data from BD0:7 for ALU input. Or, as input to the Map PROM, LBD01:71 causes output of either constant data or a microroutine address.
LDA1	3N2	Latched Data Available	Latch signal corresponding to DA input.
LDCB0	5N3	Load Disk Data Bus	Loads disk Data Bus Bits, B00:07. See Table 4-2.
LDCT0	5N3	Load Disk Control Tag	Loads control tags and B08:09. See Table 4-2.
LDDMA0,1	5N3	Load DMA	Loads RAM page and mode (read or write) into DMA.
LDDSK0	5N3	Load Disk	Loads the Bus RAM-Address Counter for disk I/O.
LDHIBYT1/ LDLOBYT1	6C6	Load High/Low Byte	Loads the halfword data registers for MUX bus I/O from BD0:7.
LDPAGE0	5N3	Load RAM Page Number	Causes the RAM page number to be loaded from BD0:7.
LDR1	3M1	Latched Data Request	Latch signal correspponding to DR input.
LME1	12L4	Latched ME0	Latch signal corresponding to ME0.
LOC1	3N3	Latched Output Command	Latch signal corresponding to the OC input.
LOF0	5N5	Clear Diagnostic	Causes the Diagnostic Flip-Flop to reset and and the Error LED to go off.

MNEMONIC	SOURCE	NAME	COMMENT
LON0	5N4	Turn On Diagnostic	Causes the Diagnostic Flip-Flop to set and the Error LED to light.
LP131:231	12H8	Page Counter Bits	Binary value to identify RAM pages 1-3 of the disk file during a read. (Page 0 is reserved for constants, statuses, etc.)
LSR	3N2	Latched Status Request	Latch signal corresponding to the SR1 input.
MAXADD01	6H8	Maximum Sector Count	Indicates that 256 bytes of data have been DMAed via the SELCH.
MAXADD11	13D2	Maximum Address Counter 1	Indicates that the maximum DMA count is reached with the less significant DMA counter.
MAXADD21	13D4	Maximum Address Counter 2	Indicates that the maximum DMA count is reached with the more significant DMA counter.
MA1:MC1	8M7	Condition Code MUX Selection Bits A-C	Three bits to select one of eight condition codes for the "next address" calculation. See Table 4-3.
MCE1	8L5	RAM Chip Enable	Enables the RAM for a read or write operation.
MD081:151	4C-	Multiplexed Data Bits	One of four multiplexed data sources to be sent to the SELCH or processor.
MEC0	5M7	Enable ECC Shift	Enables the ECC Register to shift continually.
ME0	5M8	Map PROM Enable	Reads the Map PROM location to BRA0:7 and to the Map Register.
MI1	9M9	CC MUX Inverter Bit	Fourth bit of the COND MUX CTL line; see Figure 3-6. If MI is not set, condition code (CC) output is inverted.
MOUT1	12G1	Condition Code MUX Output	Output consisting of one of the eight condition code inputs.

MNEMONIC	SOURCE	NAME	COMMENT
MUX131,231	4H2	MUX Control Bits 13 and 23	Two binary bits for selecting one of four registers to be output to the MUX bus: General-Purpose Data Register, File Address Register, Controller Address Register, or DMA Data Register.
MWE1	8L5	RAM Write Enable	Enables RAM to be written to.
NEWFILE1	3M8	New File	Indicates a new disk file has been addressed by by the processor.
NOP0	5K2	No Operation	(Not connected or used.)
NOWRDS0	6M5	No Words	Indicates no words have yet been transferred in this DMA sequence.
NXCIN1	13L1	Latched ALU Carry Bit	CARRY71 latched.
OBCADY1,Z1	17K3	Differential Open Cable Detect	Output to disk files to indicate an open A-cable or a loss of IDC power.
OCRST0	4L9	Output Command Reset	A reset command from the processor to the IDC.
OC1	3K4	CMD0 Received	Output resulting from CMD0 input.
OFF0	5N7	ECC Off	Terminates ECC generation on read. On write, it causes ECC to be written.
OFLOW1	12E2	Overflow	Indicates the ALU operation produced an overflow.
ONCYLA1,B1	14A3	Differential On-Cylinder Detection	Input status from a disk file to indicate positioned heads.
ONCYL0	14D3	Not On Cylinder	Indicates the disk drive head is not on cylinder.
ON0	5N7	ECC On	Starts ECC generation on read. On write, it causes Write Shift Register (WSR) data to be written.
OPTPTCL1	3F6	Optional Protocol	Indicates that toggle-7 of the File-0 Address Switch is pushed down to the 1-position to employ the "new" high-speed SELCH protocol.

MNEMONIC	SOURCE	NAME	COMMENT
OSC0	19B3	Oscillator	The 16-MHz oscillator of the IDC.
OURACK0	4M4	Our RACK0	Indicates a received RACK0 is for this IDC, which has an interrupt pending.
OVERRUN0,1	6M6	Data Overrun	Indicates a data overrun during a DMA operation with SELCH.
PAD1	4J9	Program Controller Reset	Indicates that the processor has sent an OCRST to the IDC.
PAGE131:231	12M8	RAM Page Address Bits 13 and 23	Two bits to select one of three RAM pages (1, 2, or 3) for either DMA or disk file I/O.
PARTIAL0	6M7	Partial Transfer	A partial sector transfer occurred.
PA0SPA90	10K2	SPA91 Inverted	See comment for SPA91.
PA01:81	10A1	PROM Address Bits 0-8	The nine least significant bits of the PROM address.
PA90,91	10M2	PROM Bank Address Bit 9	PA90 selects the second PROM bank of 512 words. PA91 selects the first PROM bank of 512 words.
PICK0	17K1	Power Sequence Pick	See HOLD0/PICK0 in this table.
POE0,1	9M9	ALU Output Enable	Indicates that the ALU output goes to BD0:7.
PROMEN1	10J1	PROM Enable	When low it enables access to the PROM banks.
PZ0	8L4	RAM Page Zero	Indicates selection of RAM page 0.
P11:31	Global	Pull-Up Resistor	5-volt pull-ups for guaranteed highs as inputs to to IDC logic.
QSHFT21	12A2	Right-Shift of Q-Register	Right-shifts the contents of the Q-register (a barrel shifter) of the ALU.
RACK01	4J6	Receive Acknowledgment	Input from the processor to signal an interrupt acknowledgment.
RAE/OE1	8C5	PROM's RAM Enable or Output Enable	AE/OE1 before it enters the Pipeline Register.

MNEMONIC	SOURCE	NAME	COMMENT
RAMBZ0	7G9	RAM Busy	Indicates the RAM is busy with a read or write.
RAMXFER0,1	7G7	RAM Transfer	Indicates the IDC is performing a data transfer to the RAM.
RAM01:71	8M1	RAM Address Lines 0-7	Eight bits that select one of 256 RAM locations in a page.
RBC0	5K5	Read Bus Control	Various IDC statuses gated onto BD0:7.
RBDI001:51	8C5-	PROM's BDIO Bits 0-5	Bus data I/O and controls before the Pipeline Register.
RBD0	5K5	Read Bus Data	Indicates DATA08:15 are gated onto BD0:7.
RBRA01:91	8H7, 10D6-	PROM's Branch Address Bits 0-9	BRA01:91 before they enter the Pipeline Register.
RBS0	5K6	Read Bus Status	Reads bus status to BD0:7.
RB01:31	9D4	PROM's ALU B-Register Selection Bits 0-3	B01:31 before they enter the Pipeline Register.
RCLK0A1,0B1 thru RCLK3A1,3B1	16A6-	Differential Read Clock	Input from a disk file to to synchronize data read from it.
RCLK01:31	16D5-	Read Clock	Read clocks from a disk file to IDC.
RCNT1	8H6	PROM's RAM Page Counter Enable	CNT1 before it enters the Pipeline Register.
RCN1	9D8	PROM's Carry Bit	CIN1 before it enters the Pipeline Register.
RDATA01:31	16D1-	Read Data	Data read from a disk file to the IDC.
RDAT0A1,0B1 thru RDAT3A1,3B1	16A1-	Differential Read Data	Input data read from the disk file.
RDHIBYT0, RDLOBYT0	6D5-	Read High, Low Byte	Reads the high- or low-order data byte to BD0:7.
READY0	14D4	Selected Disk File Ready	Indicates the selected disk file is ready for I/O.

MNEMONIC	SOURCE	NAME	COMMENT
READ1	12D8	IDC Read	Indicates the IDC is currently executing a read operation.
REGSYN0	6J4	Register Sync	Indicates that the IDC received one of the four control functions -- SR0, CMD0, DR0, or DA0.
RGATE0, RGATE1	18J9, 16D9	Read Gate	Read Gate of the selected disk file.
RI01:81	9D4	PROM's ALU Instruction Bits 0-8	I01:81 before they enter the Pipeline Register.
RMA1:MC1	8H8	PROM's Condition Code MUX Selection Bits	MA1:MC1 before they enter the Pipeline Register.
RMCE1	8C5	PROM's RAM Chip Enable	MCE1 before it enters the Pipeline Register.
RMI1	9D9	PROM's MUX Inverter Bit	MI1 before it enters the Pipeline Register.
RMWE1	8H5	PROM's RAM Write Enable	MWE1 before the Pipeline Register.
RPOE1	9D8	PROM's ALU Output Enable	POE1 before it enters the Pipeline Register.
RPZ0	8D5	PROM's RAM Page Zero	PZ0 before it enters the Pipeline Register.
RRA0	5K5	Read RAM Address	Microcode signal to read the RAM Address Counter Bus (RADD CTR BUS).
RRA01:71	8D2	PROM's RAM Address	RAM address before it enters the Pipeline Register.
RSEL1	3N6	Register Select	Indicates that the encoded FUNC0:2 bits are now active. An I/O operation is now active for the IDC or a disk file.
RSHFT21	12A2	RAM Shift 2nd ALU Slice	Shifts the RAM either up or down according to the ALU operation.
RSI01:31	9D2	PROM's Sequence Instruction Bits 0-3	SI01:31 before they enter the Pipeline Register.
RSR001	18H1	Read/Write Serial Disk Data	Serial data shifted into the ECC circuitry during a read/write operation.

MNEMONIC	SOURCE	NAME	COMMENT
RSR00:15	18J-	Read Shift Register Bits 0-15	Accumulated bits associated with a disk file read operation.
RSTATN0	5K4	Reset Attention	Microcode signal to reset ATN0.
RSTIDL0	5N6	Reset Idle	Indicates the Idle Flip-Flop is reset and the Idle LED is off.
RWCLK1	16F7	Read/Write Clock	Read/Write Clock from the selected disk file.
RWGATE0,1	16G9	Read/Write Gate	Indicates the Read Gate or the Write Gate of the disk file is on.
SATN0	5M3	Set Attention	Sets the INTREQ Flip-Flop, thus activating ATN0 output.
SAVCRY0	13G1	Save Carry	Enables the Save Carry Flip-Flop.
SBSY01	6A4	SELCH Busy	Input from SELCH indicating SELCH is currently busy with a block data transfer.
SCHK01	6F2	Status Check	Output to SELCH to indicate a bad IDC status. (Applicable only to the "new" SELCH protocol.)
SCLK0A1,0B1 thru SCLK3A1,3B1	17A5-	Differential Servo Clock	Input from a disk file for the write clock (WCLK0A1,0B1 thru WCLK3A1,3B1).
SCLR01	3B9	System Clear	Input from the processor to initialize IDC logic.
SCTY1,Z1	15M-	Differential Select-Cylinder Tag	Output to a disk file to indicate that bus lines B00:09 are supplying a cylinder address.
SDATA1	16F3	Serial Read Data	Serial data, including ECC, read from a disk file.
SECTOR0,1	17M6	Sector Pulse	Sector pulses from selected disk file.
SECTOV0,1	19C6	Sector Overflow	Error condition indicating the Read or Write Gate is up when the sector pulse is active.
SECT0A1,0B1 thru SECT3A1,3B1	17H6-	Differential Sector	Input pulse to mark the beginning of each physical sector.

MNEMONIC	SOURCE	NAME	COMMENT
SEC0	5M7	Shift ECC	Shifts the ECC register once.
SELCHBZ1	6C4	SELCH Busy	Indicates that the SELCH is currently busy with a block data transfer.
SELCHDAR1	7M7	SELCH Data Available or Requested	Indicates a received DA0 or DR0 via the SELCH.
SELCHDR0	7M6	SELCH Data Request	Indicates a data request from the SELCH.
SELCHXFR0,1	7M9	SELCH Transfer	Indicates SELCH is transferring data.
SEL01:31	15D2-	Disk File Selected	Indicates that the disk file is now selected.
SEL1	5M8	Select Pulse	Loads the disk file number (0-3) onto USEL0,USEL1.
SETIDL0	5M6	Set Idle Flip-Flop	Sets the Idle Flip-Flop and turns on the Idle LED.
SHTY1,Z1	15M-	Differential Select-Head Tag	Output to disk files to indicate that the bus lines are supplying head-select or volume-select data.
SIGN1	12E3	Sign Bit	Represents the most significant bit of the high-order slice from an ALU operation.
SI01:31	9M1	Sequencer Instruction Bits 0-3	Sequencer instruction bits input to the Microprogram Sequencer. See Table 4-8.
SKED0A1,0B1 thru SKED3A1,3B1	16H6-	Differential Seek End	Input from a disk file to indicate the end of a seek operation.
SKEND01:31	16L6	Seek End	Indicates the end of a seek operation at a disk file.
SKERA1,B1	14A2-	Seek Error	Indicates a seek error on a selected disk file.
SKER1	14D2	Seek Error	Indicates a seek error on a selected disk file.
SNS	6F3	Set New Sequence	Output to SELCH to indicate IDC support for the "new" high-speed SELCH protocol.

MNEMONIC	SOURCE	NAME	COMMENT
SNS0	6G3	Set New Sequence without Bus Switch	Output to SELCH to indicate IDC support for the "new" high-speed SELCH protocol, without an I/O Bus Switch. Jumping pins W1 and W2 on the IDC board for this support is not recommended.
SON1	3M3	Latched Sync On	Indicates a latched sync word received from a disk file; i.e., a sync mark is now in the Read Shift Register (RSR).
SPA91	10E2	Most-Significant PROM Bit 9	Most significant bit of the 10-bit PROM address which also includes PA01:81.
SR01	3J3	Status Request	Input from the processor requesting the current status (onto D080:150) of IDC or a disk file.
SR1	3K3	SR0 Received	Output resulting from SR0 input.
SSYN0	5J6	Set Sync	Microcode-generated sync return.
STCHK1	6E3	Status Check	See comment with SCHK01.
STOPDMA0	6G5	Stop DMA	Stops DMA when a partial DMA transfer occurs.
SYNCON1	7A4	Sync On	Indicates a received sync word from a disk file.
STPSLCH0	5M6	Stop SELCH Strobe	Generates SCHK0. (Applicable only to the "new" high-speed SELCH protocol.)
SYNC0,1	18M1, 7C2	Sync Word Detect	Indicates a sync word was detected while IDC was reading disk file data.
SYN0,1	6M4	Sync Return	Output to the processor or SELCH indicating that this IDC or an attached disk file has properly accepted and responded to a control line signal.
TACK0	4M3	Transmit Acknowledge	Output to the next IDC board to signal an interrupt acknowledgment from the processor.
TBD0	5M4	Transmitted Bus Data	Latches bus data to GPD8:15.

MNEMONIC	SOURCE	NAME	COMMENT
TESTCLR0	3B9	Test Clear	A ground signal manually placed here clears IDC logic.
TIMEOUT0,1	10M4	IDC Timeout	IDC timed out during an operation.
TSTCLK0	14F8	Test Clock	System clock for an IDC developmental system.
UNRDYLA1,B1	14A4-	Differential Unit Ready	Input from a disk file indicating its readiness for I/O.
UPWE1	12K9	Clocked RAM Write Enable	MWE1 gated with CLK341. See comment for MWE1.
UP130:230	12K8	Page Counter Bits	Binary value to identify RAM pages 0-3 of the disk file during a read.
USEL0A1,0B1 thru USEL3A1,3B1	15A2	Differential Unit-Selected Tag	Input from a disk file indicating its selection.
USEL0Y1,0Z1 and USEL1Y1,1Z1	17M4-	Differential Unit Select	Output to disk files consisting of the address number (0-3) of the disk file to be selected.
USTAGY1,Z1	15M-	Differential Unit-Select Tag	Output to disk files informing them that the unit select lines (see above) are supplying a file address.
WCLK0A1,0B1 thru WCLK3A1,3B1	17F5-	Differential Write Clock	Output to a disk file to synchronize data written to the disk file.
WDATA1	7M5	Serial Write Data	Serial data, including ECC, written to a disk file.
WDAT0A1,0B1 thru WDAT3A1,3B1	17F1-	Differential Write Data	Output data written to a disk file.
WECC0	7H5	Write ECC	Enables the ECC circuitry.
WENB0	12M9	Read/Write Enable to RAM	Selects a read/write operation over BD0:7.

MNEMONIC	SOURCE	NAME	COMMENT
WGATE1	16D9	Write Gate to Disk File	Indicates a write operation is being performed to the selected disk file.
WPROT1	14D5	Write Protected	Indicates a write-protected disk file.
WRITE1	12D8	IDC Write	Indicates this IDC is performing a write to a disk file.
WRRAM1	12K9	Write RAM Enable	Enables the IDC RAM to be written with DMA data.
WSR0:15	18E-	Write Shift Register Bits 0-15	Loaded into the WSR from BD0:7. They are written to the selected disk file.
WSR1	18F7	Write Serial Data	Serial data written to a disk file.
WTPTA1,B1	14A5-	Differential Write Protect	Input from a disk file to indicate it is in the write-protected mode.
XFERHI0	5K3	Transfer High Byte	Reads RSR08:15 to BD0:7; writes BD0:7 to WSR08:15.
XFERLO0	5K3	Transfer Low Byte	Reads RSR00:07 to BD0:7; writes BD0:7 to WSR00:07.
XFRDONE1	7J9	Transfer Done	A particular DMA transfer is complete.
XFRGPD0	3N5	Transfer General-Purpose Data	Selects the General-Purpose Register to be output onto the SELCH/MUX bus.
XFRREQ1	7C8	Transfer Required	DMA transfer is required.
XFRSYNCH0,1	7M8	Transfer Sync	Transfers SYN0 to the SELCH. It also clocks SELCH DMA data into the IDC.
09R08	7G3	Bit 151 Inverted	Loads data from the Serial-to-Parallel Converter into the BD0:7 Register.
09R10	7G1	DCL0 Inverted	Resets ECC clock generation.

CONNECTOR 10 (J10)

ROW 2			ROW 1		
PIN NO.	BRD. LOC.	MNEMONIC	PIN NO.	BRD. LOC.	MNEMONIC
24	01C61	TSTCLKØ	24	01C31	GND
23	01C62	GND	23	01C32	
22	01C63	WCSRETI	22	01C33	
21	01C64	GND	21	01C34	
20	01C65	EBLTCLKØ	20	01C35	
19	01C66	PROMENI	19	01C36	
18	01C67		18	01C37	
17	01C68		17	01C38	
16	01C69	RBRA4I	16	01C39	
15	01C70	RBRA3I	15	01C40	
14	01C71	RBRA5I	14	01C41	
13	01C72	RBRA2I	13	01C42	
12	01C73	RBRA6I	12	01C43	
11	01C74	RBRA1I	11	01C44	
10	01C75	RBRA7I	10	01C45	
09	01C76	RBRAØI	09	01C46	
08	01C77	PA4I	08	01C47	
07	01C78	PA5I	07	01C48	
06	01C79	PA3I	06	01C49	
05	01C80	PA6I	05	01C50	
04	01C81	PA2I	04	01C51	
03	01C82	PA7I	03	01C52	
02	01C83	PA1I	02	01C53	
01	01C84	PAØI	01	01C54	
00	01C85	PAØI	00	01C55	GND

CONNECTOR 11 (J11)

ROW 2			ROW 1		
PIN NO.	BRD. LOC.	MNEMONIC	PIN NO.	BRD. LOC.	MNEMONIC
24	00C61	RBDIØ4I	24	00C51	GND
23	00C62	RBDIØ3I	23	00C52	
22	00C63	RMAI	22	00C53	
21	00C64	RBDIØ2I	21	00C54	
20	00C65	RMBI	20	00C55	
19	00C66	RBDIØ1I	19	00C56	
18	00C67	RMCI	18	00C57	
17	00C68	RBDIØØI	17	00C58	
16	00C69	RMCEI	16	00C59	
15	00C70	RMWEI	15	00C60	
14	00C71	RAE/OEI	14	00C61	
13	00C72	RCNTI	13	00C62	
12	00C73	RPZØ	12	00C63	
11	00C74	RBRA9I	11	00C64	
10	00C75	RBDIØ5I	10	00C65	
09	00C76	RBRA8I	09	00C66	
08	00C77	RRA4I	08	00C67	
07	00C78	RRA3I	07	00C68	
06	00C79	RRA5I	06	00C69	
05	00C80	RRA2I	05	00C70	
04	00C81	RRA6I	04	00C71	
03	00C82	RRA1I	03	00C72	
02	00C83	RRA7I	02	00C73	
01	00C84	RRAØI	01	00C74	
00	00C85	SPA9I	00	00C75	GND

CONNECTOR 12 (J12)

ROW 2			ROW 1		
PIN NO.	BRD. LOC.	MNEMONIC	PIN NO.	BRD. LOC.	MNEMONIC
24	01F61	RI1I	24	01F31	GND
23	01F62	RIØI	23	01F32	
22	01F63	RI2I	22	01F33	
21	01F64	RCNI	21	01F34	
20	01F65	RI3I	20	01F35	
19	01F66	RPOEI	19	01F36	
18	01F67	RI4I	18	01F37	
17	01F68	RMII	17	01F38	
16	01F69	RBØI	16	01F39	
15	01F70	RI8I	15	01F40	
14	01F71	RBII	14	01F41	
13	01F72	RI7I	13	01F42	
12	01F73	RB2I	12	01F43	
11	01F74	RI6I	11	01F44	
10	01F75	RB3I	10	01F45	
09	01F76	RI5I	09	01F46	
08	01F77	RSIØI	08	01F47	
07	01F78	AR3I	07	01F48	
06	01F79	RSI1I	06	01F49	
05	01F80	AR2I	05	01F50	
04	01F81	RSI2I	04	01F51	
03	01F82	ARII	03	01F52	
02	01F83	RSI3I	02	01F53	
01	01F84	ARØI	01	01F54	
00	01F85		00	01F55	GND

CONNECTOR 13 (J13)

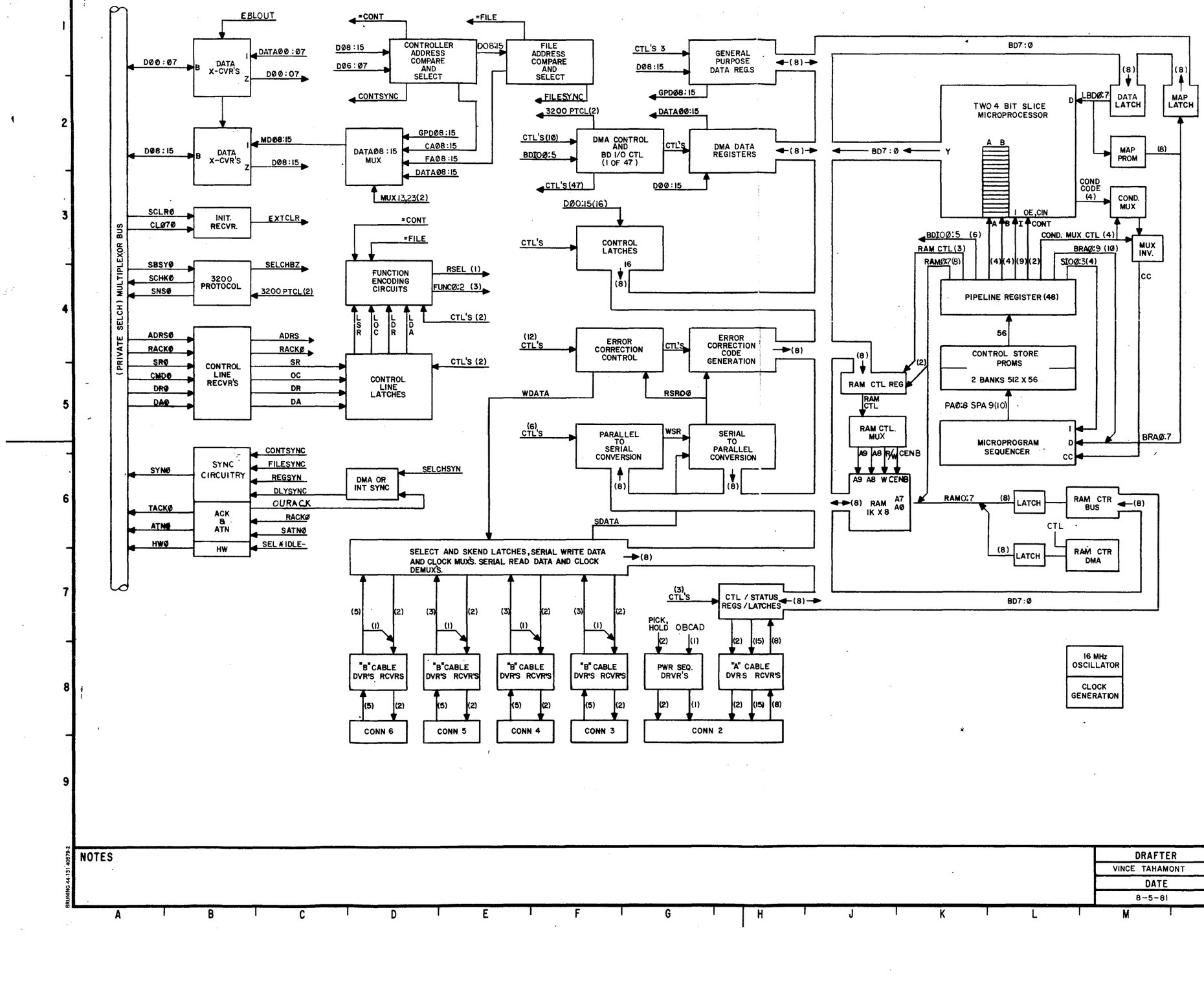
ROW 2			ROW 1		
PIN NO.	BRD. LOC.	MNEMONIC	PIN NO.	BRD. LOC.	MNEMONIC
19	03F61	BRA4I	19	03F31	GND
18	03F62	BRA3I	18	03F32	
17	03F63	BRA5I	17	03F33	
16	03F64	BRA2I	16	03F34	
15	03F65	BRA6I	15	03F35	
14	03F66	BRA1I	14	03F36	
13	03F67	BRA7I	13	03F37	
12	03F68	BRAØI	12	03F38	
11	03F69		11	03F39	
10	03F70		10	03F40	
09	03F71		09	03F41	
08	03F72	MEØ	08	03F42	
07	03F73	LBD4I	07	03F43	
06	03F74	LBD5I	06	03F44	
05	03F75	LBD3I	05	03F45	
04	03F76	LBD6I	04	03F46	
03	03F77	LBD2I	03	03F47	
02	03F78	LBD7I	02	03F48	
01	03F79	LBD1I	01	03F49	GND
00	03F80	PZØ	00	03F50	LBDØI

CABLE CONNECTOR MAP

CONN	TERM. NO.	ROW 2	ROW 1
6	12	SECTØAI	SECTØBI
	11	GND	INXØBI
	10	INXØAI	GND
	09	SKEDØAI	SKEDØBI
	08	USELØBI	USELØAI
	07	GND	WDATØBI
	06	WDATØAI	GND
	05	WCLKØAI	WCLKØBI
	04	GND	RCLKØBI
	03	RCLKØAI	GND
	02	RDATØAI	RDATØBI
	01	GND	SCLKØBI
	00	SCLKØAI	GND
5	12	SECT1AI	SECT1BI
	11	GND	INX1BI
	10	INX1AI	GND
	09	SKED1AI	SKED1BI
	08	USEL1BI	USEL1AI
	07	GND	WDAT1BI
	06	WDAT1AI	GND
	05	WCLK1AI	WCLK1BI
	04	GND	RCLK1BI
	03	RCLK1AI	GND
	02	RDAT1AI	RDAT1BI
	01	GND	SCLK1BI
	00	SCLK1AI	GND
4	12	SECT2AI	SECT2BI
	11	GND	INX2BI
	10	INX2AI	GND
	09	SKED2AI	SKED2BI
	08	USEL2BI	USEL2AI
	07	GND	WDAT2BI
	06	WDAT2AI	GND
	05	WCLK2AI	WCLK2BI
	04	GND	RCLK2BI
	03	RCLK2AI	GND
	02	RDAT2AI	RDAT2BI
	01	GND	SCLK2BI
	00	SCLK2AI	GND
3	12	SECT3AI	SECT3BI
	11	GND	INX3BI
	10	INX3AI	GND
	09	SKED3AI	SKED3BI
	08	USEL3BI	USEL3AI
	07	GND	WDAT3BI
	06	WDAT3AI	GND
	05	WCLK3AI	WCLK3BI
	04	GND	RCLK3BI
	03	RCLK3AI	GND
	02	RDAT3AI	RDAT3BI
	01	GND	SCLK3BI
	00	SCLK3AI	GND
2	29	BIØYI	BIØZI
	28	HOLDØ	PICKØ
	27	WTPTAI	WTPTBI
	26		
	25		
	24		
	23	USELIYI	USELIZI
	22	USELØYI	USELØZI
	21	USTAGYI	USTAGZI
	20	BUSYAI	BUSYBI
	19		
	18	UNRDYLA I	UNRDYLBI
	17		
	16	ONCYLAI	ONCYLBI
	15	SKERAI	SKERBI
	14	FAULTAI	FAULTBI
	13	OBCADY:	OBCADZI
	12	BØ9YI	BØ9ZI
	11	BØ8YI	BØ8ZI
	10	BØ7YI	BØ7ZI
	09	BØ6YI	BØ6ZI
	08	BØ5YI	BØ5ZI
	07	BØ4YI	BØ4ZI
	06	BØ3YI	BØ3ZI
	05	BØ2YI	BØ2ZI
	04	BØ1YI	BØ1ZI
	03	BØØYI	BØØZI
	02	CTYI	CTZI
	01	SHTYI	SHTZI
	00	SCTYI	SCTZI

BACK PANEL MAP

ROW 1	ROW 2



REVISIONS

PROTO REL AT R01.				
E.C.J. 0176	——	——	11-18-81	R01
2ND PROTO REL AT R02				
E.C. [illegible]	——	——	12-30-81	R02
EXTENSIVE CHANGES				
ES [illegible]	4986	—	2-5-82	R03
EXTENSIVE CHANGES TO CORRECT NUMEROUS DOCUMENT ERRORS. SEE R03 MICROFILM FOR PREVIOUS REV LEVEL.				
JLV [illegible]	5127	M	7-27-82	R04 X

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Oceanport, N.J. 07757

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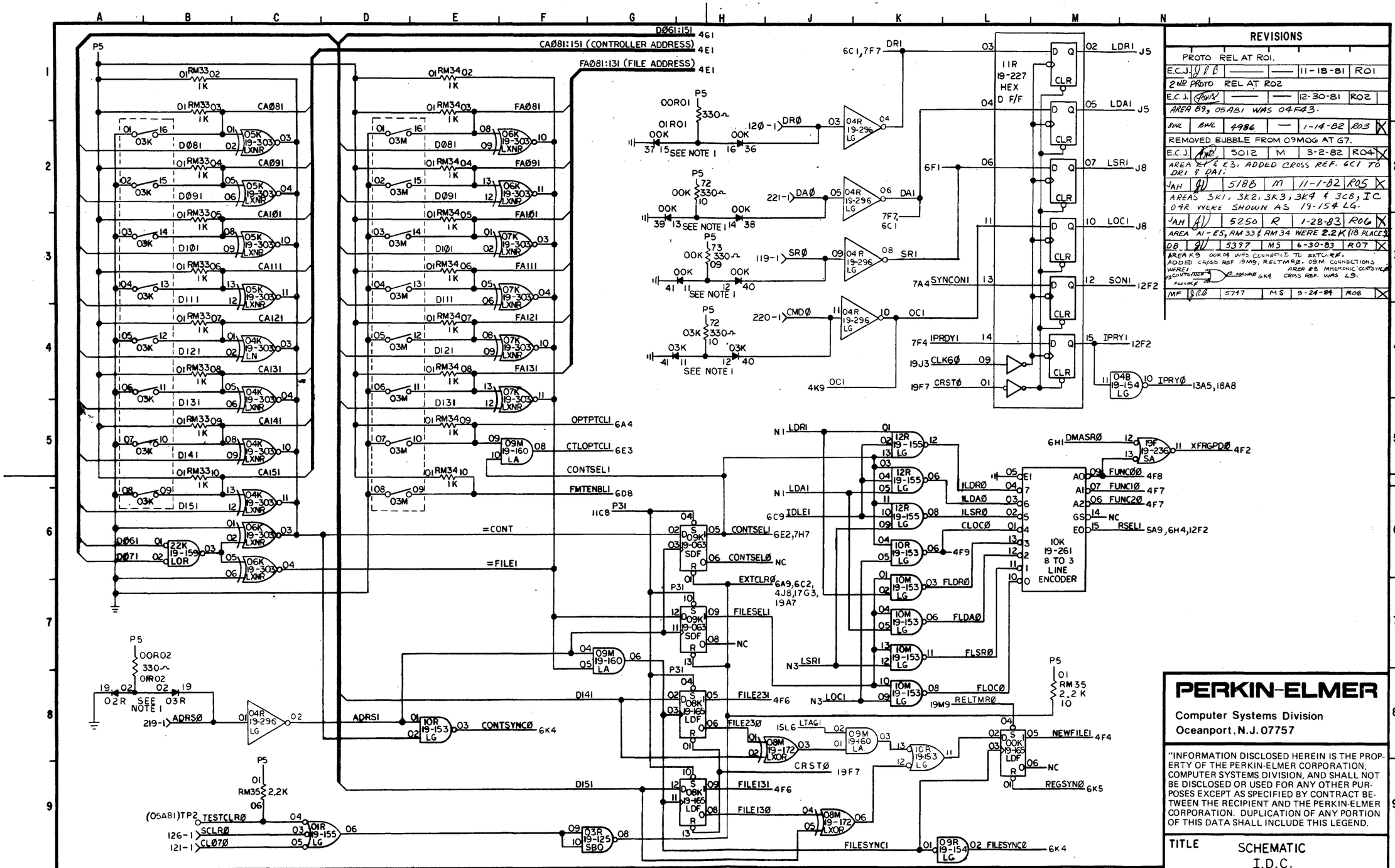
TITLE: SCHEMATIC
I. D. C.

NOTES

DRAFTER	VINCE TAHAMONT
DATE	8-5-81
TASK	03983
DWG	35-807 R04 D08
SHT	2-23

BRUNING 44-137 40579-2



REVISIONS

PROTO REL AT R01.

E.C.J.		—	—	11-18-81	R01
2ND PROTO REL AT R02					
E.C.J.		—	—	12-30-81	R02
AREA B9, 05A81 WAS 04F43.					
BWL	BWL	4986	—	1-14-82	R03
REMOVED BUBBLE FROM 09M06 AT G7.					
E.C.J.		5012	M	3-2-82	R04
AREA K3, ADDED CROSS REF. 6C1 TO DRI & DAI.					
JAH		5188	M	11-1-82	R05
AREAS 3K1, 3K2, 3K3, 3K4 & 3C8, IC 09R WERE SHOWN AS 19-154 LG.					
JAH		5250	R	1-28-83	R06
AREA A1-E5, RM33 & RM34 WERE 2.2K (18 PLACES)					
DB		5397	MS	6-30-83	R07
AREA K9 OOK09 WAS CONNECTED TO EXTCLRØ. ADDED CROSS REF 19M9, RELTMRØ. 09M CONNECTIONS WERE1 TO 13 CONTINUED FROM PAGE 7 TO ADDRESS 6K4 AREA E8 MNEMONIC CONTSYNC1 CROSS REF. WAS LS.					
MF		5747	MS	9-24-84	R08

NOTES

1. ALL DIODES ARE 23-040.
2. 03M AND 03K ARE 33-035.
3. ALL RESISTOR VALUES ARE IN OHMS, 1/4 WATT, ± 5%

BRUNING 44-131 40579-2

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TITLE: SCHEMATIC I.D.C.

DRAFTER	TASK	SHT
V. TAHAMONT	DWG 35-807R08 D08	3-23
DATE 7-8-81		

REVISIONS					
PROTO REL AT R01.					
E.C.J.				11-18-81	R01
2ND PROTO REL AT R02					
E.C.J.				12-30-81	R02
AREA K9, ADDED 22D (19-063)					
BWL	BWL	4986	—	2-5-82	R03 X
19D13 AT M2 WAS P5. I.C. 22D AT AT L9 WAS 19-063					
E.C.J.		5012	M	3-2-82	R04 X
AREA M-2, IC 19D WAS 19-063, SDF. AREA K-6, IC 09R WAS 19-154 LG.					
JAH		5250	R	1-28-83	R05 X

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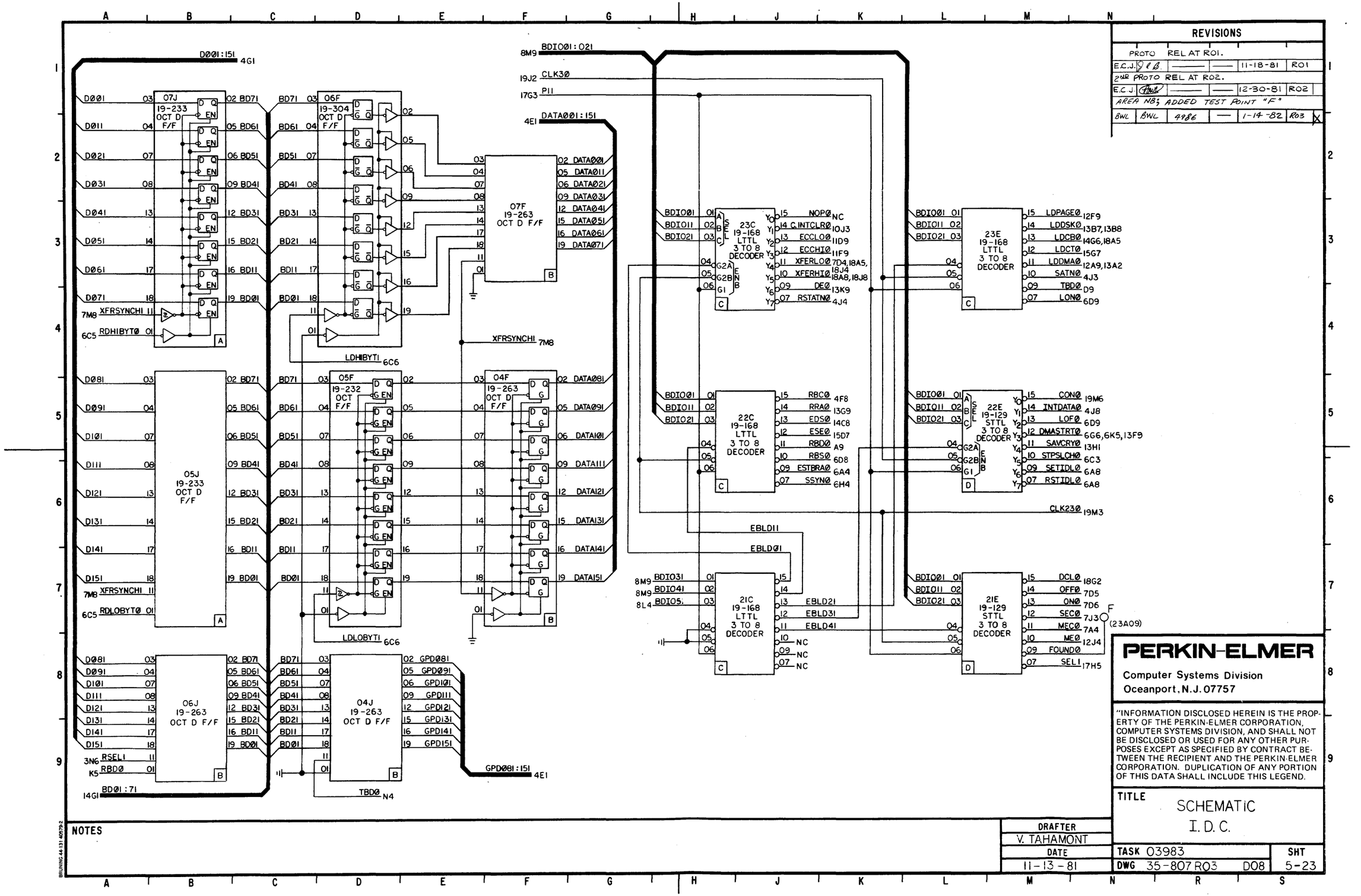
TITLE SCHEMATIC

IDC

DRAFTER	TASK 03983	SHT
R JOHNSON / ES	DWG 35-807R05 D08	4 -23
DATE 7-7-81		

NOTES

BRUNING 44-131 405792-2



REVISIONS					
PROTO REL AT R01.					
E.C.J.	S & B.	———	———	11-18-81	R01
2ND PROTO REL AT R02.					
E.C.J	[illegible]	———	———	12-30-81	R02
AREA NB; ADDED TEST POINT "F"					
BWL	BWL	4986	———	1-14-82	R03

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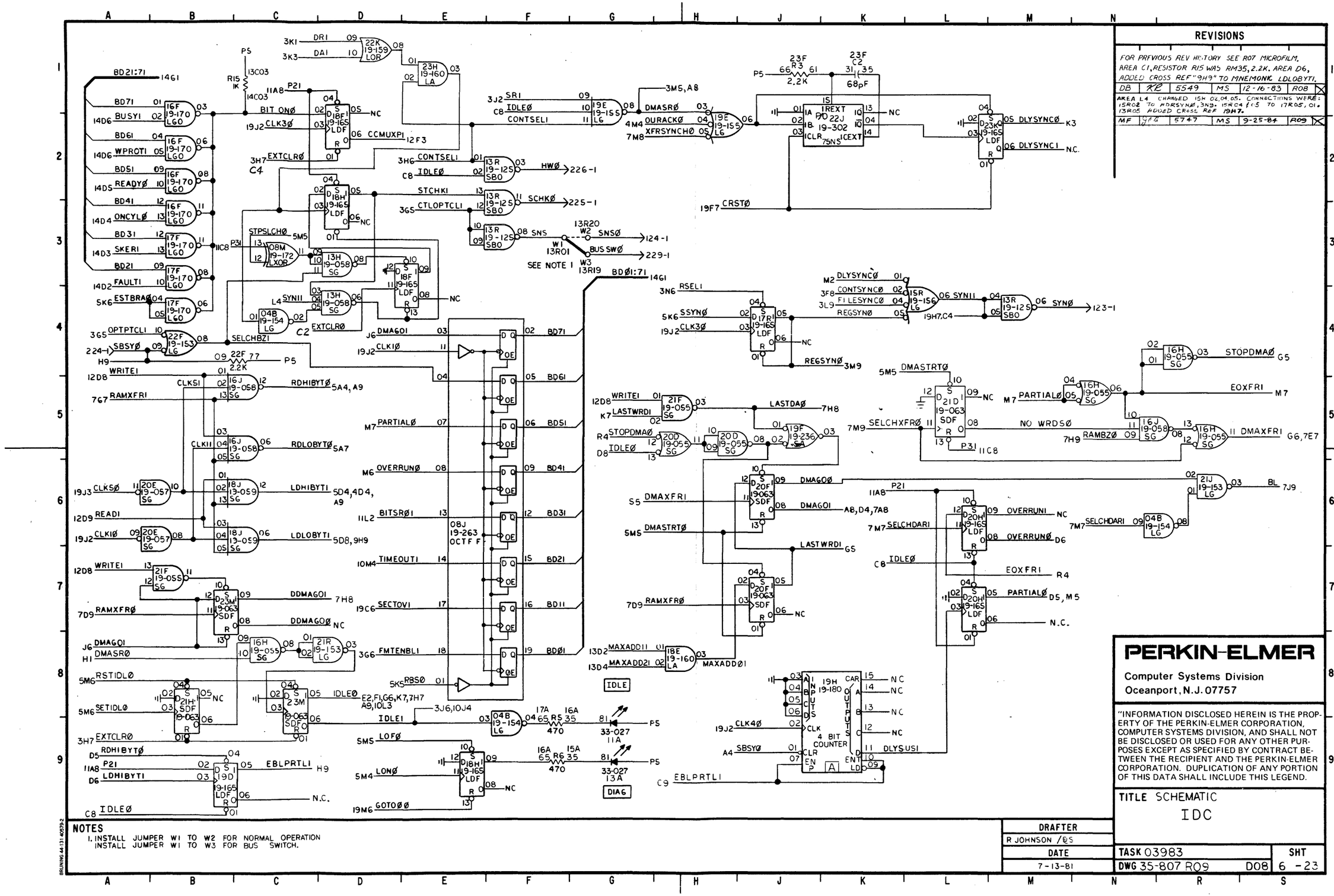
TITLE
SCHEMATIC
I. D. C.

NOTES

DRAFTER	
V. TAHAMONT	
DATE	
11-13-81	

TASK 03983 | SHT 5-23
DWG 35-807 R03 D08

BRUNING 44-131 405792


REVISIONS
FOR PREVIOUS REV HISTORY SEE R07 MICROFILM.
AREA C1, RESISTOR R15 WAS RM35, 2.2K. AREA D6, ADDED CROSS REF "9H9" TO MNEMONIC LDLOBYTI.
DB | RR | 5549 | MS | 12-16-83 | R08
AREA L4 CHANGED 15N 04,04,05. CONNECTIONS WERE: 15R02 TO MDRSYNØ, 3N9. 15RC4 TO 5 TO 17R05, 01. 13R05 ADDED CROSS REF 19H7.
MF | JJA | 5747 | MS | 9-25-84 | R09
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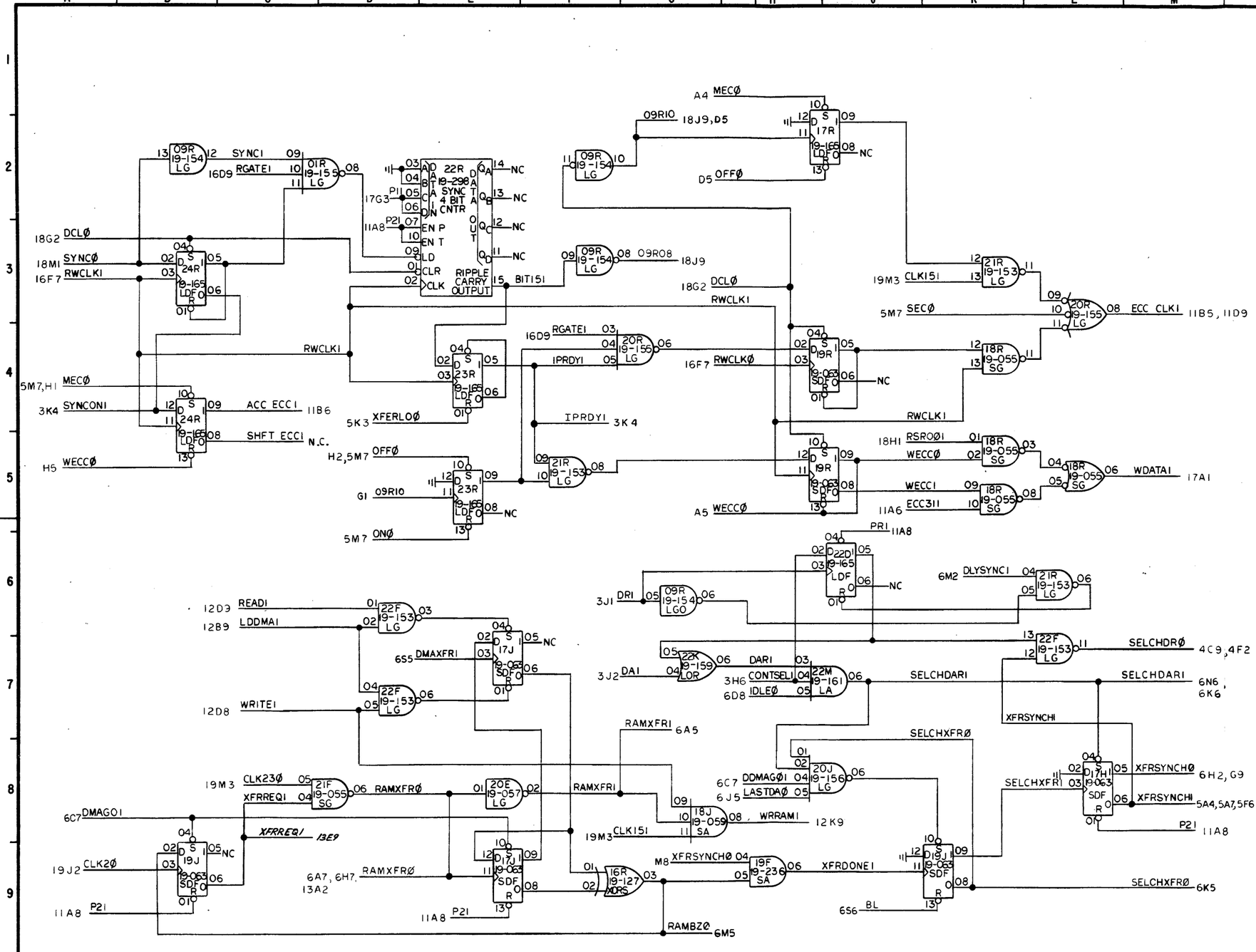
TITLE SCHEMATIC
IDC
NOTES
1. INSTALL JUMPER W1 TO W2 FOR NORMAL OPERATION
INSTALL JUMPER W1 TO W3 FOR BUS SWITCH.
DRAFTER
R JOHNSON /RS
DATE
7-13-81
TASK 03983
SHT
DWG 35-807 R09 D08
6 - 23
BRUNING 44-131 40579-2



REVISIONS

PROTO REL AT R01.				
E.C.J.			11-18-81	R01
2ND PROTO REL AT R02				
E.C.J.			12-30-81	R02
GATE 09R AT GG WAS ADDED. GATE 21R AT LG WAS ADDED. 22D AT JG WAS ADDED. 22K05 AT G7 WAS "DR1". I.C. 17H AT L8 WAS 19-165.				
E.C.J.	5012	M	3-2-82	R03
22D02 (22D03 AT JG WERE GND. 22D04 AT JG WAS CONN TO 09R06.				
E C J	5024	M	3-15-82	R04
AREA G1: ADDED D5 TO 09R10. AREA D5: 23R11 WAS MNEM. "DCLØ" DEST 18G2.				
JLV	5127	M	7-26-82	R05
AREA M7, DELETE GC3 FROM "SELCHDAR1"				
JAH	5188	M	11-3-82	R06
AREA G-8, IC 18J WAS 19-058 SG.				
JAH	5250	R	1-28-83	R07
AREA M7, "6N6" WAS "6H9". AREA J9, "6S6" WAS "6K8".				
KR	5311	MS	4-7-83	R08
AREA L7, IC 22F12 WAS CONNECTED TO 17H03				
DB	5541	MS	11-16-83	R09
AREA C9 ADDED SIGNAL XFRREQ1 / CROSS REF. AREA D9 SIGNAL "RAMXFRØ" DELETED CROSS REF "13F9."				
HH	5668	MS	9-12-84	R10

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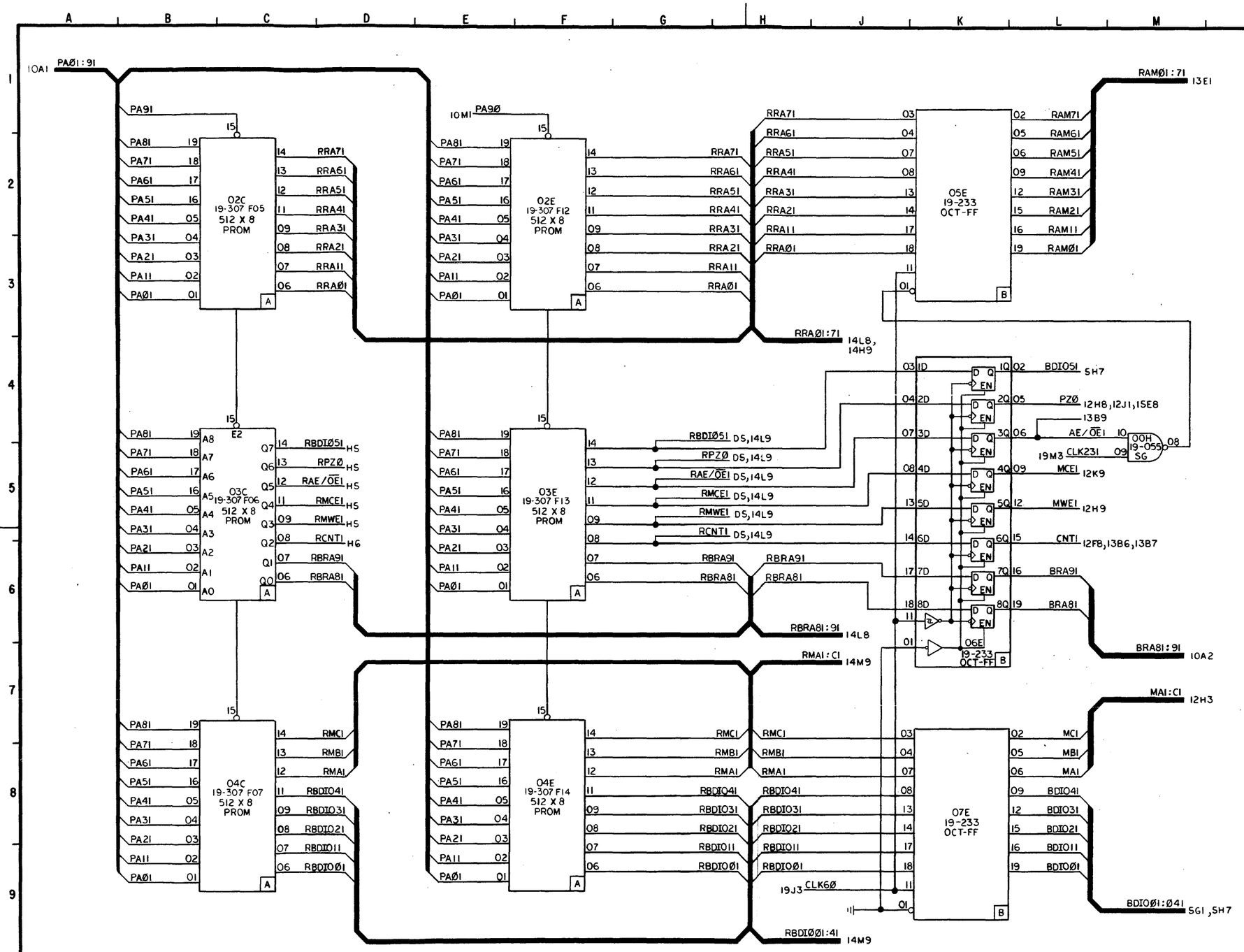
TITLE: SCHEMATIC
I. D. C.

NOTES

DRAFTER	E. JOHNSON
DATE	7-20-81
TASK	03983
DWG	35-807 R10 D08
SHT	7-23

BRUNING 44-131-40579-2



REVISIONS

PROTO REL AT R01.					
E.C.J.			11-19-81	R01	
2ND PROTO REL AT R02					
E.C.J.			12-30-81	R02	X
ADDED FUNCTION VARIATION DESIGNATION TO ALL 19-307 IC (6 PLCS)					
JLV		5127	M	7-26-82	R03 X

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TITLE SCHEMATIC I.D.C.

NOTES

DRAFTER V. TAHAMONT

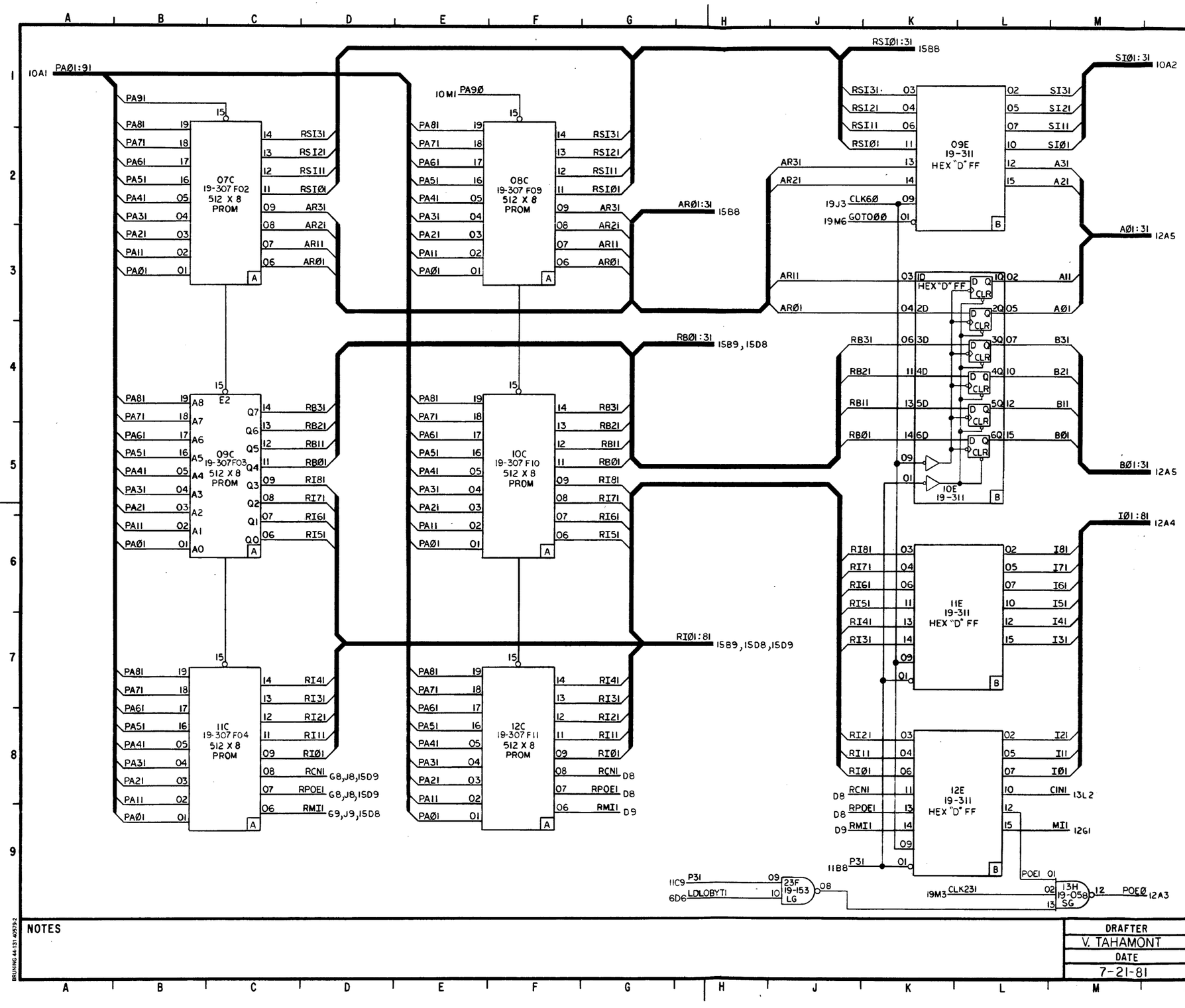
DATE 7-15-81

TASK 03983

DWG 35-807R03 D08

SHT 8-23

BRUNING 44 131 40579-2



REVISIONS

PROTO REL AT R01.					
E.C.J.	0 I B.	——	——	11-19-81	R01
2ND PROTO REL AT R02.					
E.C.J.	[illegible]	——	——	12-30-81	R02 X
ADDED FUNCTION VARIATION DESIGNATION TO ALL 19-307 ICs (6 PLCS)					
JLV	JV	5127	M	7-26-82	R03 X
AREA M9, GATE 13H WAS 00H, 19-055. ADDED NEW IC 23 F, 19-153.					
DB	RC	5549	M5	12-16-83	R04 X

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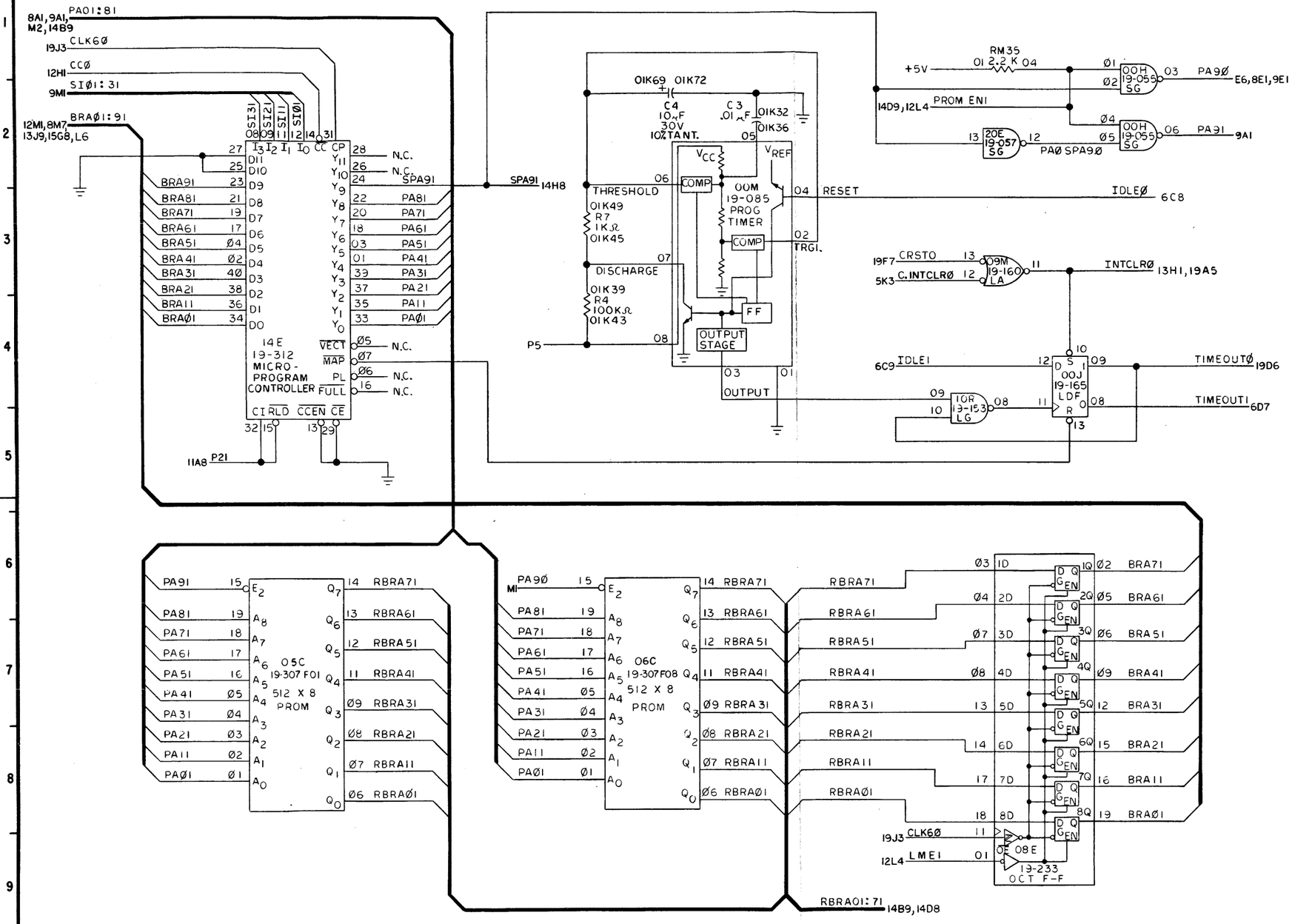
TITLE
SCHEMATIC
I. D. C.

NOTES

DRAFTER	
V. TAHAMONT	
DATE	
7-21-81	

TASK 03983 | SHT 9-23
DWG 35-807 R04 D08

BRUNING 44-131 40579-2



REVISIONS					
PROTO REL AT R01					
E.C.J. JVB	———	———	11-19-81	R01	
2ND PROTO REL AT R02					
E.C.J. PWB	———	———	12-30-81	R02	X
ADDED FUNCT. VARIATION DESIGNATION TO 19-307, I.C.'S 05C & 06C					
JLV	GV	5127	M	7-26-82	R03	X
AREA K-2, IC-20E, PART # WAS 19-154.					
JAH	GV	5250	R	1-28-83	R04	X

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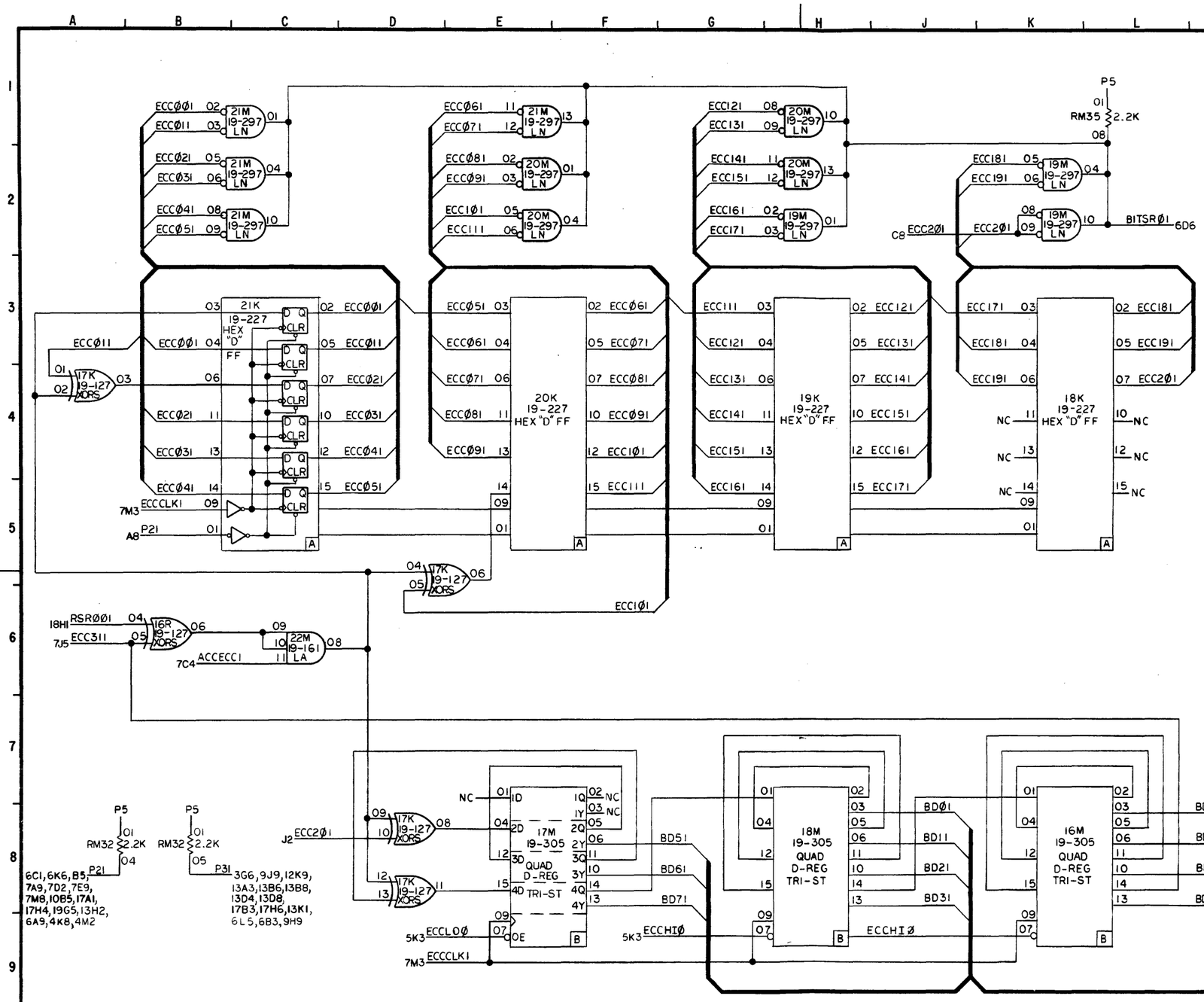
TITLE
SCHEMATIC
IDC

NOTES

DRAFTER	TASK	SHT
P. MARCUS	03983	10-23
DATE	DWG 35-807R04 D08	
7-21-81		

BRUNING 44-131 40579-2



REVISIONS

PROTO REL AT R01.					
E.C.J.	JTB	———	———	11-19-81	R01
2ND PROTO REL AT R02					
E.C.J.	JTB	———	———	12-30-81	R02
AREA A9, ADDED X-REF 6A9 TO "P21"					
BWL	BWL	4986	—	1-20-82	R03 X
AT A9, ADDED X-REF 4M2 TO "P21".					
E.C.J.	JTB	5012	M	3-2-82	R04 X
AREA C8, ADDED "683" TO P31.					
KR		5311	MS	4-7-83	R05 X
AREA C9, ADDED CROSS REF "9H9" TO MNEMONIC P31.					
DB	KR	5549	MS	12-17-83	R06 X

NOTES

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TITLE
SCHEMATIC
I.D.C.

DRAFTER	V. TAHAMONT
DATE	7-22-81
TASK	03983
DWG	35-807R06 D08
SHT	11-23

BRUNING 44 131 40572

REVISIONS

PROTO REL AT R01.

E.C.J.	J.P.B.	———	———	11-19-81	R01
2ND PROTO	REL AT R02				
E.C.J.	[illegible]	———	———	12-31-81	R02 X
18E13 AT H9 WAS CLK2Ø WITH X-REF 19J2					
E.C.J.	J.P.B.	5024	M	3-15-82	R03 X
AREAS C3 & D3 02J & 02M WERE 19-313.					
JLV	[illegible]	4921	R	4-16-82	R04 X
AREA R9: 12K10 WAS MNEM P31 DEST. 11C8. ADDED "F15" TO 1C 09F (AREA K2)					
JLV	[illegible]	5127	M	7-26-82	R05 X
AREA K4: ADDED Ed LOCATION TO DC TO DC CONVERTER (10A).					
JAH	[illegible]	5250	R	1-28-83	R06 X

NOTES

DRAFTER	V TAHAMONT
DATE	7-24-81

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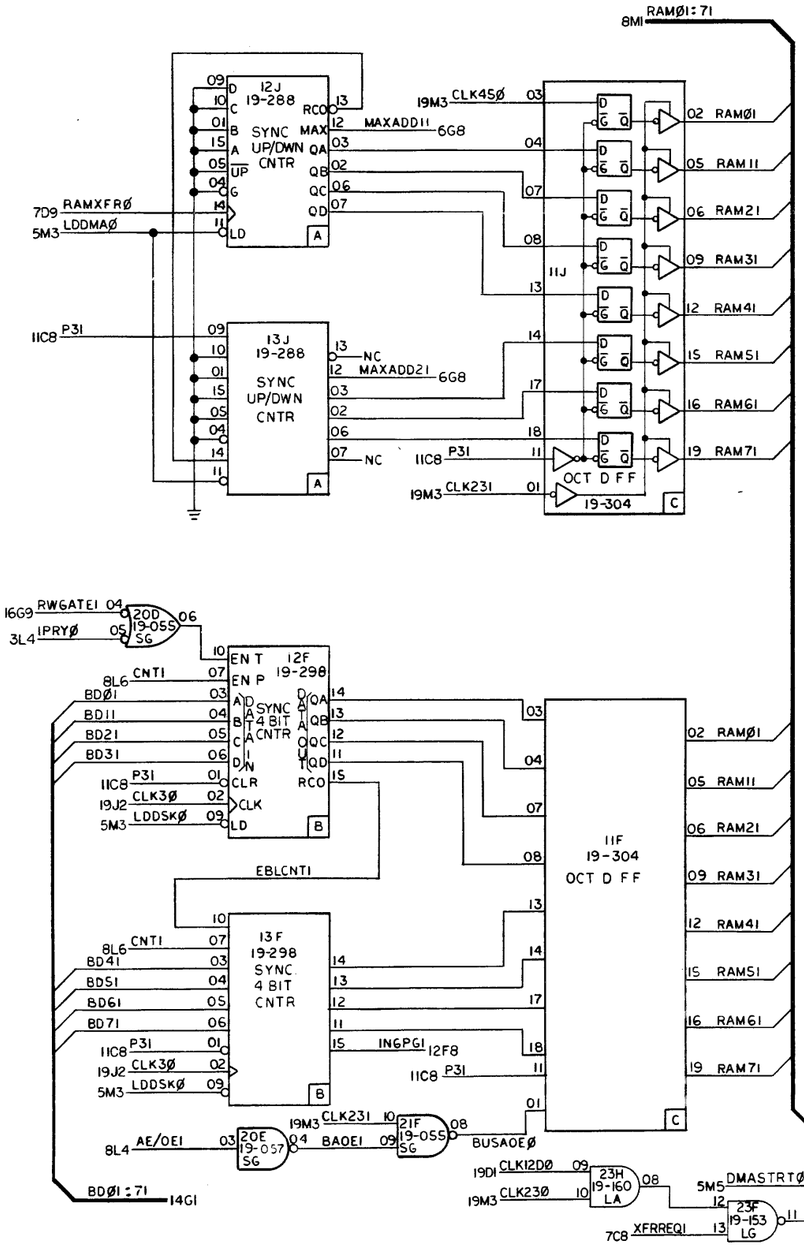
TITLE: SCHEMATIC I. D. C.

TASK 03983 | SHT 12-23

DWG 35-807R06 D08

BRUNING 44-1311 40979-2



REVISIONS					
PROTO REL AT R01.					
E.C.J.				11-19-81	R01
2ND PROTO REL AT R02.					
E.C.J.				12-31-81	R02 X
AT H1, 17H WAS 19-165.					
E.C.J.		5012	M	3-2-82	R03 X
AREA B9, IC 20E, PART # WAS 19-154.					
JAH		5250	R	1-28-83	R04 X
AREA E8 ADDED IC'S 23H, 23F. AREA G9 IC 19F PIN 09 WAS SIGNAL RAMXFRØ, CROSS REF TD9.					
HH		5668	MS	4-12-84	R05 X

NOTES

DRAFTER	DS
DATE	4-21-81

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TITLE SCHEMATIC

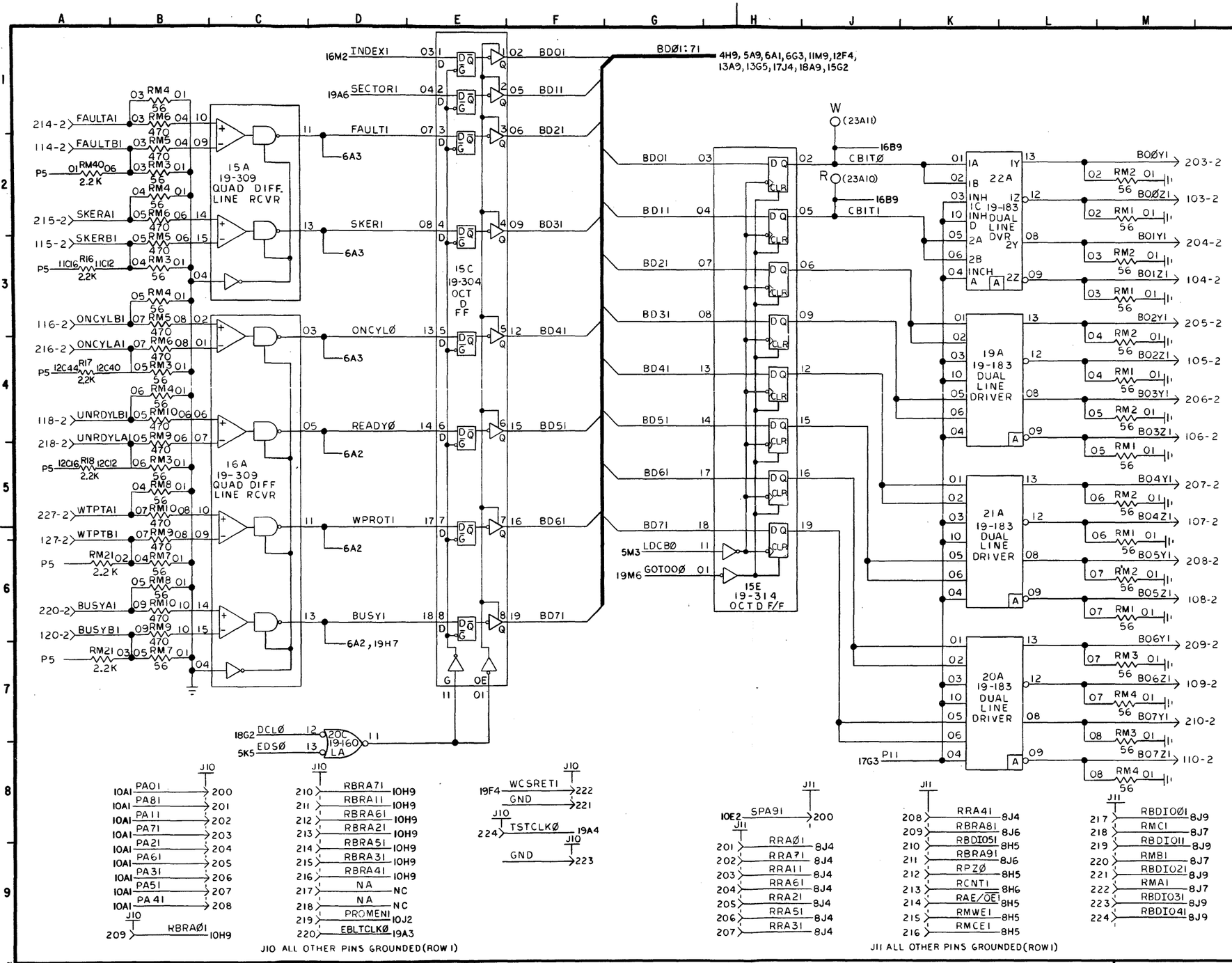
IDC

TASK 03983

DWG 35-807R05 D08

SHT 13 -23

BRUNING 44-131 40579-2



REVISIONS

PROTO REL AT R01.				
E.C.J.		—	—	11-19-81 R01
REL AT R02.				
E.C.J.		—	—	12-31-81 R02
AREAS J1&J2; ADDED TESTPOINTS W&R				
BWL	BWL	4986	—	1-14-82 R03 X
AREA A2, ADDED RESISTOR RM40.				
KR		5311	MS	3-31-83 R04 X
AREA A3-A5, ADDED RESISTORS R16, R17 & R18.				
DB	KR	5549	MS	12-17-83 R05 X
AREA H4; 15E, 'CLR' WAS 'OE' (6PLC'S). AREA D6 ADDED; X-REF 19H7 TO MNEMONIC 'BUSY1'.				
MF		5747	MS	3-25-84 R06 X

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NOTES

DRAFTER	P MARCUS
DATE	7-23-81
TITLE	SCHEMATIC I.D.C.
TASK	03983
DWG	35-807R06 D08
SHT	14 -23

BRUNING 44-131 40579-2

REVISIONS				
PROTO REL AT R01.				
E.C.J.		—	11-19-81	R01
2ND PROTO REL AT R02.				
E.C.J.		—	12-31-81	R02
SIGS' USTAGY1, & USTAGZ1 OF AREA M6 WERE USTAGY1 & USTAGZ1 RESPECTIVELY.				
DS		4986	—	12-5-82 R03
AREA H3 - THE 'CLK' WAS 'OE' (RPLC'S). AREA J5 ADDED X-REF LTAG1. AREA G7 X-REF 13M3 WAS 13M6 GOTOOG.				
MF		5747	MS	9-26-84 R04 X

BDØ1:71 14G1

108-6 USELØAI — RM31 02 56; RM30 03 470 04 02
208-6 USELØBI — RM29 03 470 04 01
P5 — RM32 01 2.2K 02; RM31 03 56 01
108-5 USEL1AI — RM26 02 56; RM25 03 470 04 06
208-5 USEL1BI — RM24 03 470 04 07
P5 — RM32 03; RM26 03 56 01
108-4 USEL2AI — RM20 02 56 01; RM19 03 470 04 10
208-4 USEL2BI — RM18 03 470 04 09
P5 — RM21 01 2.2K; RM20 03 56 01
108-3 USEL3AI — RM15 02 56 01; RM14 03 470 04 14
208-3 USEL3BI — RM13 03 470 04 15
P5 — RM21 06; RM15 03 56 01 04

17A 19-309 QUAD DIFF. LINE RCVR

03 SELØ1 — 17B2
05 SEL11 — 17B3
11 SEL21 — 17B4
13 SEL31 — 17B5

16C 19-304 OCT D FF

03 1D 1Q 02 BDØ1
04 2D 2Q 05 BD11
07 3D 3Q 06 BD21
08 4D 4Q 09 BD31
13 5D 5Q 12 BD41
14 6D 6Q 15 BD51
17 7D 7Q 16 BD61
18 8D 8Q 19 BD71

SKENDØ1 13
SKEND11 14
SKEND21 17
SKEND31 18
16M6 SKENDØ1:31

G OE
5K5 ESEO 11 Q1

BDØ1 03
BD11 04
BD21 07
BD31 08
BD41 13
BD51 14
BD61 17
BD71 18

16E 19-314 OCT D F/F

5M3 LDCTØ 11
19M9 RELTMRØ 01

02 CLR 16
19 CLR

198 19-183 DUAL LINE DRIVER

01 1A 1Y 13 — BØ8Y1 → 211-2
02 1B
03 INH
10 1C
05 2A 2Y 08 — BØ9Y1 → 212-2
06 2B
04 INH
A A 2Z 09 — BØ9Z1 → 112 2

RM3 01 56 BØ8Z1 → 111-2
RM4 01 56 BØ9Z1 → 112 2
RM3 01 56
RM4 01 56

21B 19-183 DUAL LINE DRIVER

01 13 — BIØY1 → 229-2
02
03 12 — BIØZ1 → 129-2
10
05 08 (SPARE) — HI1 → N.C.
06
04 A 09 (SPARE) — LO1 → N.C.

RM8 01 56
RM7 01 56
RM8 01 56
RM7 01 56

LTAG1 19L7, 3J4, 19K5

198 19-183 DUAL LINE DRIVER

01 13 — USTAGY1 → 221-2
02
03 12 — USTAGZ1 → 121-2
10
05 08 — SCTY1 → 200-2
06
04 A 09 — SCTZ1 → 100-2

RM8 01 56
RM7 01 56
RM2 01 56
RM1 01 56

228 19-183 DUAL LINE DRIVER

01 13 — SHTY1 → 201-2
02
CTAG31 16B9 03 12 — SHTZ1 → 101-2
10
05 08 — CTY1 → 202-2
06
17G3 P11 04 A 09 — CTZ1 → 102-2

RM2 01 56
RM1 01 56
RM2 01 56
RM1 01 56

P5 — RM21 04 2.2K; RM7 07 56 01

J12

200	N.A.		NC
201	ARØ1	9H2	
202	RSI31	9K1	
203	AR11	9H2	
204	RSI21	9K1	
205	AR21	9H2	
206	RSI11	9K1	
207	AR31	9H2	
208	RSIØ1	9K1	
209	RI51	9H7	
210	RB31	9H4	
211	RI61	9H7	
212	RB21	9H4	

J12

213	RI71	9H7	
214	RB11	9H4	
215	RI81	9H7	
216	RBØ1	9H4	
217	RMI1	9H9	
218	RI41	9H7	
219	RPØE1	9D8	
220	RI31	9H7	
221	RCN1	9D8	
222	RI21	9H7	
223	RIØ1	9H7	
224	RI11	9H7	

J12 ALL OTHER PINS GROUNDED (ROW 1)

J13

12KI	LBDØ1		100
8L4	PZØ		200
12KI	LBD11		201
12KI	LBD71		202
12KI	LBD21		203
12KI	LBD61		204
12KI	LBD31		205
12KI	LBD51		206
12KI	LBD41		207
12J4	MEØ		208
NC	N.A.		209
NC	N.A.		210

J13

NC	N.A.		211

J13

212	BRAØ1	10A2	
213	BRA71	10A2	
214	BRA11	10A2	
215	BRA61	10A2	
216	BRA21	10A2	
217	BRA51	10A2	
218	BRA31	10A2	
219	BRA41	10A2	

J13 ALL OTHER PINS EXCEPT, PIN 100 ARE GROUNDED (ROW 1)

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Oceanport, N.J. 07757

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NOTES

DRAFTER	P. MARCUS
DATE	7-24-81
TITLE	SCHEMATIC I.D.C.
TASK	03983
DWG	35-807R04 D08
SHT	15-23

BRUNING 44-131 40572-2

REVISIONS					
PROTO REL AT R01.					
E.C.J.	2ND PROTO	—	—	11-19-81	R01
2ND PROTO REL AT R02					
E.C.J.	2ND PROTO	—	—	12-31-81	R02
AREAS M2 & M3, ADDED TEST POINT "I".					
BWL	BWL	4986	—	1-14-82	R03

07A 19-309 QUAD DIFF LINE RCVR

06A 19-309 QUAD DIFF LINE RCVR

14A 19-309 QUAD DIFF LINE RCVR

13A 19-309 QUAD DIFF LINE RCVR

09A 19-069 8TO1 MUX

08A 19-069 8TO1 MUX

P/O 12A 19-177 4TO1 MUX

20C 19-160 LA

08B 19-127 XOR

04B 19-154 LG

NOTES

DRAFTER	D STINE
DATE	7-24-81

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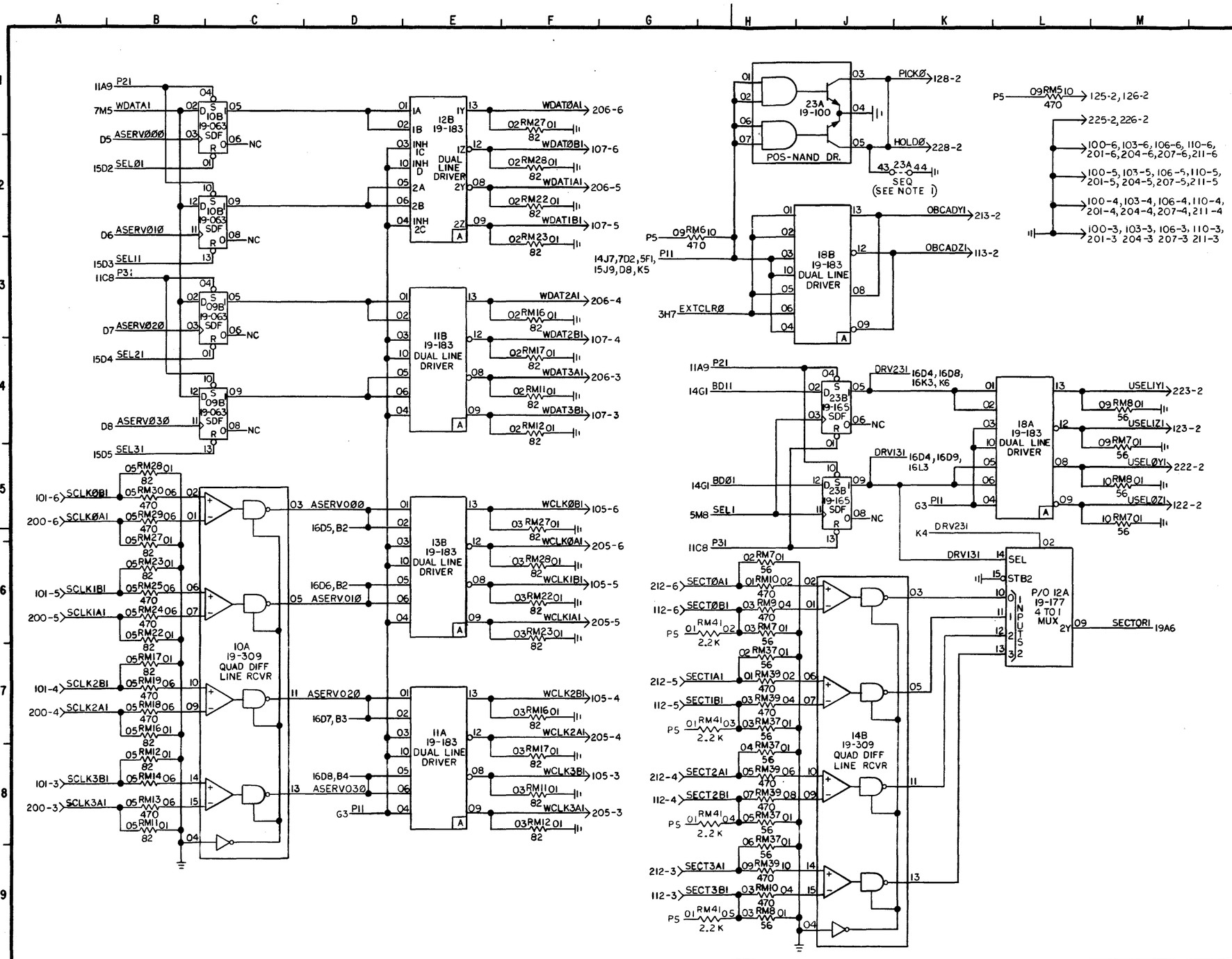
TITLE SCHEMATIC

IDC

TASK 03983	SHT
DWG 35-807R03 D08	16 -23

BRUNING 44-131 40579-2



REVISIONS

PROTO	REL AT R01.				
E.C.J.		—	—	11-19-81	R01
2ND PROTO	REL AT R02.				
BWC	BWC	—	—	12-31-81	R02 X
AREA J1 23A04 WAS NC. NOTE 1 WAS ENABLE, POWER SEQUENCING"					
JLV	JV	5127	M	7-26-82	R03 X
AREA M-2 VALUE OF RM6 WAS 450 IN ERROR.					
JAH	JH	5250	R	1-28-83	R04 X

NOTES

1. INSTALL JUMPER TO DISABLE POWER SEQUENCING.

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TITLE: SCHEMATIC I.D.C.

DRAFTER: V. TAHAMONT

DATE: 7-27-81

TASK 03983

DWG 35-807R04 D08

SHT 17-23

BRUNING 44-131 40579-2

REVISIONS				
PROTO REL AT R01.				
E.C.J.			11-19-81	R01
2ND PROTO REL AT R02.				
E.C.J.			12-31-81	R02 X
AREA G2 DELETED "7D5" FROM DCLØ				
JLV	5127	M	7-27-82	R03 X

BDØ1 BD11 BD21 BD31 BD41 BD51 BD61 BD71

14F 19-314 OCT D F/F

5K3 XFERLOØ

5M3 LDCBØ

OCT D F/F A

14J 19-300 8 BIT PARA S/S REG

SERIAL INPUTS

PARA INPUTS A B C D

QH OUTPUT

SHFT LOAD

CLK

CLK INIBIT

B

DCLØ G6, 5M7, 7A3, 7H3, 14C7

RWCLK1 16F7

7J5, 11A6 RSRØØ1

14K 19-299 8BIT SHFT REG

16F3 SDATA1

SERIN A B

C

14M 19-301 4 BIT D TYPE TRI ST REG

ENB G1 G2

INPUTS 1D 2D 3D 4D

OUTPUTS Q1 Q2 Q3 Q4

D

13K 19-301 4 BIT D TYPE TRI ST REG

15M 19-301 D TYPE TRI ST REG

16K 19-301 D TYPE TRI ST REG

5K3 XFERLOØ

5K3 XFERHIØ

7G3 Ø9RØ8

7G1 Ø9RIØ

ISR 19-156 LG

SYNCØ 7A3

15F 19-314 OCT D F/F

15J 19-300 8 BIT PARA S/S REG

WSR1 16D4

15K 19-299 8 BIT SHFT REG

DCLØ G2

RWCLK1 16F7

5K3 XFERHIØ

3L4 IPRYØ

22K 19-159 LOR

7C2 RGATE1

18C 19-296

RGATEØ

14G1 BDØ1:71

BDØ1:71

NOTES

DRAFTER	
R JOHNSON /DS	
DATE	
7-22-81	

TASK 03983 SHT 18-23

DWG 35-807R03 D08

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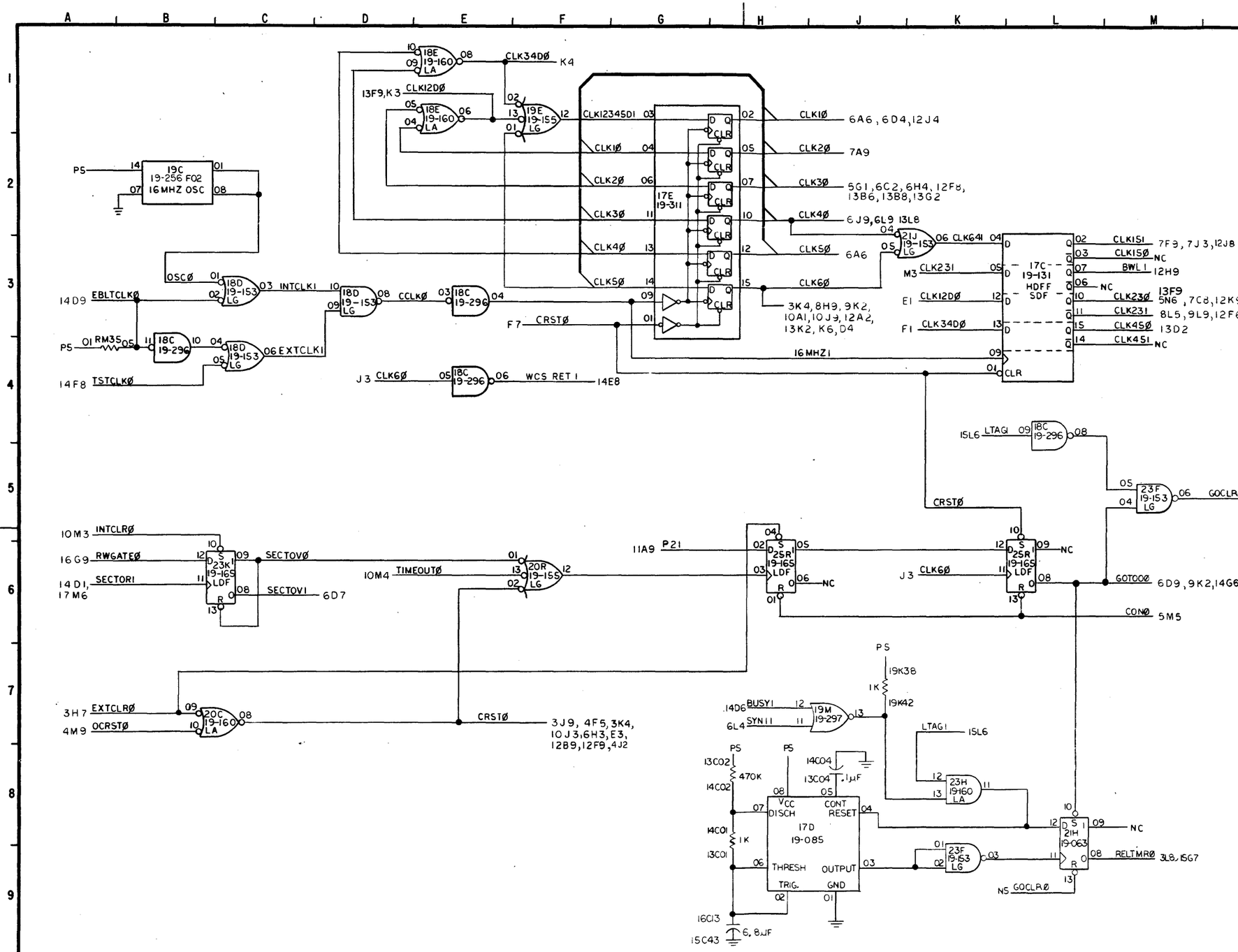
TITLE SCHEMATIC

IDC

BRUNING 44-151 40979-2



REVISIONS

AREA K4-N8. DEL. 15G7 FROM GOTOOØ X-REF. EXTENSIVE ADDITIONS MADE. FOR PREVIOUS REV HISTORY SEE R07 MICRO-FILM COPY.

MF	JEF	5747	MS	9-25-84	R08

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TITLE SCHEMATIC
IDC

NOTES

DRAFTER	
E. JOHNSON	
DATE	
7-23-81	

TASK 03983
DWG 35-807R08 D08
SHT 19-23

BRUNING 44-131 40579-2

IDC RESISTOR MODULE CONVERSION CHART

RESISTOR MODULE	PIN NO.	CONN. NO.	ROW	PIN NO.	MNEMONIC
RM1	01	8	1	44	GND
	02			43	BØØZ1
	03			42	BØ1Z1
	04			41	BØ2Z1
	05			40	BØ3Z1
	06			39	BØ4Z1
	07			38	BØ5Z1
	08			37	SCTZ1
	09			36	SHTZ1
RM1	10	8	1	35	CTZ1
RM2	01	8	2	44	GND
	02			43	BØØY1
	03			42	BØ1Y1
	04			41	BØ2Y1
	05			40	BØ3Y1
	06			39	BØ4Y1
	07			38	BØ5Y1
	08			37	SCTY1
	09			36	SHTY1
RM2	10	8	2	35	CTY1
RM3	01	8	1	34	GND
	02			33	INXØB1
	03			32	FAULTB1
	04			31	SKERB1
	05			30	ONCYLA1
	06			29	UNRDYLA1
	07			28	BØ6Y1
	08			27	BØ7Y1
	09			26	BØ8Y1
RM3	10	8	1	25	BØ9Y1
RM4	01	8	2	34	GND
	02			33	INXØA1
	03			32	FAULTA1
	04			31	SKERA1
	05			30	ONCYLB1
	06			29	ONRDYLB1
	07			28	BØ6Z1
	08			27	BØ7Z1
	09			26	BØ8Z1
RM4	10	8	2	25	BØ9Z1
RM5	01	7	2	34	INXØB1
	02			33	14A01
	03			32	FAULTB1
	04			31	15A09
	05			30	SKERB1
	06			29	15A15
	07			28	ONCYLB1
	08			27	16A02
	09			26	P5
RM5	10	7	2	25	125-2
RM6	01	7	1	34	INXØA1
	02			33	14A02
	03			32	FAULTA1
	04			31	15A10
	05			30	SKERA1
	06			29	15A14
	07			28	ONCYLA1
	08			27	16A01
	09			26	P5
RM6	10	7	1	25	18803

EXAMPLE: RM5 PIN 1 = 72 X 34
- CONNECTOR
- ROW
- PIN NO.

RM25 PIN 6 = 94 X 26
- CONNECTOR
- ROW
- PIN NO.

RESISTOR MODULE	PIN NO.	CONN. NO.	ROW	PIN NO.	MNEMONIC
RM 7	01	8	1	24	GND
	02			23	SECTØA1
	03			22	SECTØB1
	04			21	WTPTB1
	05			20	BUSYB1
	06			19	B1ØZ1
	07			18	USTA6Z1
	08			17	LO
	09			16	USELIZ1
RM 7	10	8	1	15	USELØZ1
RM 8	01	8	2	24	GND
	02			23	INX3B1
	03			22	SECT3B1
	04			21	WTPTA1
	05			20	BUSYA1
	06			19	B1ØY1
	07			18	USTA6Y1
	08			17	H1
	09			16	USELIY1
RM 8	10	8	2	15	USELØY1
RM 9	01	7	2	24	INX3B1
	02			23	14A15
	03			22	SECTØB1
	04			21	14B01
	05			20	UNRDYLA1
	06			19	16A07
	07			18	WTPTB1
	08			17	16A09
	09			16	BUSYB1
RM 9	10	7	2	15	16A15
RM 10	01	7	1	24	SECTØIA
	02			23	14B02
	03			22	SECT3B1
	04			21	14B15
	05			20	UNRDYLB1
	06			19	16A06
	07			18	WTPTA1
	08			17	16A10
	09			16	BUSYA1
RM 10	10	7	1	15	16A14
RM 11	01	8	1	12	GND
	02			11	WDAT3A1
	03			10	WCLK3B1
	04			09	
	05			08	SCLK3A1
RM 11	06	8	1	07	
RM 12	01	8	2	12	GND
	02			11	WDAT3B1
	03			10	WCLK3A1
	04			09	
	05			08	SCLK3B1
RM 12	06	8	2	07	
RM 13	01	7	2	12	
	02			11	
	03			10	USEL3B1
	04			09	17A15
	05			08	SCLK3A1
	06			07	10A15
	07			06	
	08			05	
	09			04	SKED3A1
RM 13	10	7	2	03	13A14
RM 14	01	7	1	12	
	02			11	
	03			10	USEL3A1
	04			09	17A14
	05			08	SCLK3B1
	06			07	10A14
	07			06	
	08			05	
	09			04	SKED3A1
RM 14	10	7	1	03	13A15

RESISTOR MODULE	PIN NO.	CONN. NO.	ROW	PIN NO.	MNEMONIC
RM15	01	8	1	06	GND
	02			05	USEL3A1
	03			04	USEL3B1
	04			03	SKED3A1
	05			02	SKED3B1
RM15	06	8	1	01	
RM16	01	9	1	47	GND
	02			46	WDAT2A1
	03			45	WCLK2B1
	04			44	
	05			43	SCLK2A1
RM16	06	9	1	42	
RM17	01	9	2	47	GND
	02			46	WDAT2B1
	03			45	WCLK2A1
	04			44	
	05			43	SCLK2B1
RM17	06	9	2	42	
RM18	01	9	3	47	
	02			46	
	03			45	USEL2B1
	04			44	17A09
	05			43	SCLK2A1
	06			42	10A09
	07			41	
	08			40	
	09			39	SKED2A1
RM18	10	9	3	38	13A10
RM19	01	9	4	47	
	02			46	
	03			45	USEL2A1
	04			44	17A10
	05			43	SCLK2B1
	06			42	10A10
	07			41	
	08			40	
	09			39	SKED2B1
RM19	10	9	4	38	13A09
RM20	01	9	1	41	GND
	02			40	USEL2A1
	03			39	USEL2B1
	04			38	SKED2A1
	05			37	SKED2B1
RM20	06	9	1	36	
RM21	01	9	2	41	P5
	02			40	WTPTB1
	03			39	BUSYB1
	04			38	USTA6Z1
	05			37	USEL2B1
RM21	06	9	2	36	USEL3B1
RM22	01	9	1	31	GND
	02			30	WDATIA1
	03			29	WCLKIB1
	04			28	
	05			27	SCLKIA1
RM22	06	9	1	26	
RM23	01	9	2	31	GND
	02			30	WDATIB1
	03			29	WCLKIA1
	04			28	
	05			27	SCLKIB1
RM23	06	9	2	26	
RM24	01	9	3	31	
	02			30	
	03			29	USELIB1
	04			28	17A07
	05			27	SCLKIA1
	06			26	10A07
	07			25	
	08			24	
	09			23	SKEDIA1
RM24	10	9	3	22	13A06

REVISIONS

PROTO	REL AT R01.			
E.C.J.			11-19-81	R01
2ND PROTO	REL AT R02			
J.RB			12-31-81	R02

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NOTES

DRAFTER	E. JOHNSON
DATE	11-4-81

TITLE: SCHEMATIC
INTELLIGENT DISC CONTROLLER

TASK 03983	SHT 20-23
DWG 35-807R02 D08	

BRUNING 44-131 40579-2

IDC RESISTOR MODULE CONVERSION CHART

RESISTOR MODULE	PIN NO.	CONN. NO.	ROW	PIN NO.	MNEMONIC
RM25	01	9	4	31	
	02			30	
	03			29	USELIAI
	04			28	17A06
	05			27	SCLKIBI
	06			26	10A06
	07			25	
	08			24	
	09			23	SKEDIBI
RM25	10	9	4	22	13A07
RM26	01	9	1	25	GND
	02			24	USELIAI
	03			23	USELIBI
	04			22	SKEDIAI
	05			21	SKEDIBI
RM26	06	9	1	20	
RM27	01	9	1	13	GND
	02			12	WDATØAI
	03			11	WCLKØBI
	04			10	
	05			09	SCLKØAI
RM27	06	9	1	08	
RM28	01	9	2	13	GND
	02			12	WDATØBI
	03			11	WCLKØAI
	04			10	
	05			09	SCLKØBI
RM28	06	9	2	08	
RM29	01	9	3	13	
	02			12	
	03			11	USELØBI
	04			10	17A01
	05			09	SCLKØAI
	06			08	10A01
	07			07	
	08			06	
	09			05	SKEDØAI
RM29	10	9	3	04	13A02
RM30	01	9	4	13	
	02			12	
	03			11	USELØAI
	04			10	17A02
	05			09	SCLKØBI
	06			08	10A02
	07			07	
	08			06	
	09			05	SKEDØBI
RM30	10	9	4	04	13A01
RM31	01	9	1	07	GND
	02			06	USELØAI
	03			05	USELØBI
	04			04	SKEDØAI
	05			03	SKEDØBI
RM31	06	9	1	02	
RM32	01	9	2	07	P5
	02			06	USELØBI
	03			05	USELIBI
	04			04	P2I
	05			03	P3I
RM32	06	9	2	02	
RM36	01	9	1	61	
	02			60	INXIAI
	03			59	INXIBI
	04			58	INX2A
	05			57	INX2B
RM36	06	9	1	56	INX3AI
RM37	01	9	2	61	GND
	02			60	SECTIAI
	03			59	SECTIBI
	04			58	SECT2AI
	05			57	SECT2BI
RM37	06	9	2	56	SECT3AI

RESISTOR MODULE	PIN NO.	CONN. NO.	ROW	PIN NO.	MNEMONIC
RM 38	01	9	3	61	INXIAI
	02			60	14A06
	03			59	INXIBI
	04			58	14A07
	05			57	INX2AI
	06			56	14A10
	07			55	INX2BI
	08			54	14A09
	09			53	INX3AI
RM 38	10	9	3	52	14A14
RM 39	01	9	4	61	SECTIAI
	02			60	14B06
	03			59	SECTIBI
	04			58	14B07
	05			57	SECT2AI
	06			56	14B10
	07			55	SECT2BI
	08			54	14B09
	09			53	SECT3AI
RM 39	10	9	4	52	14B14
RM40	01	8	2	06	P5
	02			05	INXØBI
	03			04	INXIBI
	04			03	INX2BI
	05			02	INX3BI
RM40	06	8	2	01	FAULTBI
RM41	01	9	2	55	P5
	02			54	SECTØBI
	03			53	SECTIBI
	04			52	SECT2BI
	05			51	SECT3BI
RM41	06	9	2	50	
RM42	01	9	1	55	P5
	02			54	SKEDØBI
	03			53	SKEDIBI
	04			52	SKED2BI
	05			51	SKED3BI
RM42	06	9	1	50	

RESISTOR MODULE	PIN NO.	CONN. NO.	ROW	PIN NO.	MNEMONIC

REVISIONS

PROTO REL AT R01.					
E.C.J.	JPB	——	——	11-19-21	R01
2ND PROTO REL AT R02.					
E.C.J.	[illegible]	——	——	12-31-81	R02
RM 32 PIN 04, ADDED "P2I". RM32 PIN 05, ADDED "P3I". RM40 PIN 06, ADDED "FAULTBI".					
KR	[illegible]	5311	MS	3-31-83	R03

NOTES

DRAFTER	E. JOHNSON
DATE	11-11-81

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TITLE
SCHEMATIC
INTELLIGENT DISC CONTROLLER

TASK 03983	SHT 21-23
DWG 35-807 R03 D08	

BRUNING 44-131 40579-2

NET	MNEMONIC	SHT
0001	A11	09
0002	A21	09
0003	A31	09
0004	ACCECC1	07
0005	ADRS1	03
0006	ADRS0	03
0007	AE/OE1	08
0008	ANYCRY1	13
0009	AR01	09
0010	AR11	09
0011	AR21	09
0012	AR31	09
0013	ASERV000	17
0014	ASERV010	17
0015	ASERV020	17
0016	ASERV030	17
0017	ATN0	04
0018	B01	09
0019	B11	09
0020	B21	09
0021	B31	09
0022	BA0E1	13
0023	BD01	18
0024	BD11	18
0025	BD21	18
0026	BD31	18
0027	BD41	18
0028	BD51	18
0029	BD61	18
0030	BD71	18
0031	A01	09
0046	BDI001	08
0047	BDI011	08
0048	BDI021	08
0049	BDI031	08
0050	BDI041	08
0051	BDI051	08
0052	B00Y1	14
0053	B00Z1	14
0054	B01Y1	14
0055	B01Z1	14
0056	B02Y1	14
0057	B02Z1	14
0058	B03Y1	14
0059	B03Z1	14
0060	B04Y1	14
0061	B04Z1	14
0062	B05Y1	14
0063	B05Z1	14
0064	B06Y1	14
0065	B06Z1	14
0066	B07Y1	14
0067	B07Z1	14
0068	B08Y1	15
0069	B08Z1	15
0070	B09Y1	15
0071	B09Z1	15
0072	B10Y1	15
0073	B10Z1	15
0074	BIT151	07
0075	BITONO	06
0076	BITSR01	11
0078	BRA01	10
0079	BRA11	10
0080	BRA21	10
0081	BRA31	10
0082	BRA41	10
0083	BRA51	10
0084	BRA61	10
0085	BRA71	10
0086	BRA81	10
0087	BRA91	10
0088	BUSAOE0	13
0089	BUSYA1	14
0090	BUSYB1	14
0091	BUSY1	14
0092	=CONT	03
0094	CA081	03
0095	CA091	03
0096	CA101	03
0097	CA111	03
0098	CA121	03
0099	CA131	03
0100	CA141	03
0101	CA151	03
0102	CARRY31	12
0103	CARRY71	12
0104	CB1I0	14
0105	CB1I1	14
0106	CC0	12
0107	CCLK0	19
0108	CCMUXPI	06
0109	CENBO	12
0110	DDMAG01	06
0111		
0112	C1MT1	04
0113	CIMTCLR0	05
0114	C1M1	09
0115	CLK641	19
0116	CLK450	19
0118	CLK231	19
0119	CLK230	19
0120	CLK151	19
0121	CLK34D0	19
0122	CLK12D0	19
0123	CLK12345D1	19
0124	CLK11	06
0125	CLK10	19
0126	CLK20	19
0127	CLK30	19
0128	CLK40	19
0129	CLK51	06
0130	CLK50	19
0131	CLK60	19
0133	CL070	03
0134	CLOC0	03
0135	CMD0	03
0136	CNT1	08
0137	CONO	19
0138	CONTACK0	04
0139	CONTSEL1	03
0140	CONTSYNC0	03
0141	CTAG31	15
0142	CTLOPTCL1	03
0143	D001	04
0144	D011	04
0145	D021	04
0146	D031	04
0147	D041	04
0148	D051	04
0149	D061	04
0150	D071	04
0151	D081	04
0152	D091	04
0153	D101	04
0154	D111	04
0155	D121	04
0156	D131	04
0157	D141	04
0158	D151	04
0159	D000	04
0160	D010	04
0161	D020	04
0162	D030	04
0163	D040	04
0164	D050	04
0165	D060	04
0166	D070	04
0167	D080	04
0168	D090	04
0169	D100	04
0170	D110	04
0171	D120	04
0172	D130	04
0173	D140	04
0174	D150	04
0175	DA1	03
0176	DAR1	07
0177	DA01	03
0178	DATA001	05
0179	DATA011	05
0180	DATA021	05
0181	DATA031	05
0182	DATA041	05
0183	DATA051	05
0184	DATA061	05
0185	DATA071	05
0186	DATA081	05
0187	DATA091	05
0188	DATA101	05
0189	DATA111	05
0190	DATA121	05
0191	DATA131	05
0192	DATA141	05
0193	DATA151	05
0194	DCL0	18
0196	DE0	05
0197	DLY3US1	06
0198	DLYSYNC0	06
0199	DMA130	12
0200	DMA230	12
0201	DMAG01	06
0202	DMASTPTG	05
0203	DR1	07
0204	DRV131	17
0205	DRV231	17
0206	DR0	03
0207	EBLCNT1	13
0208	EBLOUT0	04
0209	19E06	06
0210	ECC001	11
0211	ECC011	11
0212	ECC021	11
0213	ECC031	11
0214	ECC041	11
0215	ECC051	11
0216	ECC061	11
0217	ECC071	11
0218	ECC081	11
0219	ECC091	11
0220	ECC101	11
0221	ECC111	11
0222	ECC121	11
0223	ECC131	11
0224	ECC141	11
0225	ECC151	11
0226	ECC161	11
0227	ECC171	11
0228	ECC181	11
0229	ECC191	11
0230	ECC201	11
0231	ECC311	11
0232	ECCCLK1	07
0233	ECCHIC	05
0234	ECCL00	05
0235	EDS0	05
0236	EBLD01	05
0237	EBLD11	05
0238	EBLD21	05
0239	EBLD31	05
0240	EBLD41	05
0241	EBLTCLK0	19
0242	ESE0	05
0243	ESTBBA0	05
0244	EXTCLK1	19
0245	EXTCLR0	03
0247	FA081	04
0248	FA091	04
0249	FA101	04
0250	FA111	04
0251	FA121	04
0252	FA131	04
0253	FA141	04
0254	FA151	04
0255	FAULT1	14
0256	FAULTA1	14
0257	FAULTB1	14
0258	FILE131	03
0259	FILE130	03
0260	FILE231	03
0261	FILE230	03
0262	FILEACK0	04
0263	FILESEL1	03
0264	FILESYNC1	03
0265	FILESYNC0	03
0266	FINT1	04
0267	=FILE1	03
0268	FLDA0	03
0269	FLDR0	03
0270	FLOC0	03
0271	FLSR0	03
0272	FMTENBL1	03
0274	FUNC00	03
0275	FUNC10	03
0276	FUNC20	03
0277	F=0	12
0278	GOTO00	19
0279	GPDO01	05
0280	GPD091	05
0281	GPD101	05
0282	GPD111	05
0283	GPD121	05
0284	GPD131	05
0285	GPD141	05
0286	GPD151	05
0287	HW0	06
0288	I01	09
0289	I11	09
0290	I21	09
0291	I31	09
0292	I41	09
0293	I51	09
0295	I61	09
0296	I71	09
0297	I81	09
0298	IDLE0	06
0299	IDLE1	06
0300	ILDA0	03
0301	ILDR0	03
0302	ILSR0	03
0303	INIOA1	16
0304	INIOB1	16
0305	INI1A1	16
0306	INI1B1	16
0307	INI2A1	16
0308	INI2B1	16
0309	INI3A1	16
0310	INI3B1	16
0311	INDEX1	16
0312	INTCLK1	19
0313	INTCLR0	10
0314	INTDATA0	05
0315	00K09	08
0316	IPRDY1	07
0317	IPRY1	03
0318	LASTDA0	06
0319	LASTWRD1	06
0320	LBD01	12
0321	LBD11	12
0322	LBD21	12
0323	LBD31	12
0324	LBD41	12
0325	LBD51	12
0326	LBD61	12
0327	LBD71	12
0328	LDA1	03
0329	LDE1	03
0330	LDCT0	05
0331	LDCB0	05
0332	LDDMA1	12
0333	LDDMA0	05
0334	LDDSK0	05
0335	LDHIBYT1	06
0336	LDLOBYT1	06
0337	LDPAGEC	05
0338	LOC1	03
0339	LOF0	05
0340	LOW0	05
0341	LP131	12
0342	LP231	12
0343	LSR1	03
0344	MA1	08
0345	MAXADD01	06
0346	MAXADD11	13
0347	MAXADD21	13
0348	MB1	08
0349	MC1	08
0350	MCE1	08
0351	MD081	04
0352	MD091	04
0353	MD101	04
0354	MD111	04
0355	MD121	04
0356	MD131	04
0357	MD141	04
0358	MD151	04
0359	ME0	12
0360	MEC0	07
0361	MI1	09
0362	MOUT1	12
0363	MUX131	04
0364	MUX231	04
0365	MWE1	08
0366	MFWFILE1	03
0367	22F03	03
0368	01E06	03
0369	08M03	03
0370	08M06	03
0371	10B11	03
0372	02B11	04
0373	02R08	04
0374	02R06	04
0375	02R03	04
0376	06F02	05
0377	06F05	05
0378	06F06	05
0379	06F09	05
0380	06F12	05
0381	06F15	05
0382	06F16	05
0383	06F19	05
0384	05F02	05
0385	05F05	05
0386	05F06	05
0387	05F09	05
0388	05F12	05
0389	05F15	05
0390	05F16	05
0391	05F19	05
0392	19F03	06
0393	22F03	07
0394	22F06	07
0395	17J06	07
0396	17J09	07
0397	17J08	07
0398	21F11	06
0399	22J04	06
0400	18F09	06
0401	12F14	13
0402	12F13	13
0403	12F12	13
0404	12F11	13
0405	13F14	13
0406	13F13	13
0407	13F12	13
0408	13F11	13
0409	12J03	13
0410	12J02	13
0411	12J06	13
0412	12J07	13
0413	13J03	13
0414	13J02	13
0415	13J06	13
0416	12J13	13
0417	14F05	18
0418	14F06	18
0419	14F09	18
0420	14F12	18
0421	14F15	18
0422	14F16	18
0423	14F19	18
0424	15F02	18
0425	15F05	18
0426	15F06	18
0427	15F09	18
0428	15F12	18
0429	15F15	18
0430	15F16	18
0431	15F19	18
0432	09R08	07
0433	14K04	18
0434	14K05	18
0435	14K06	18
0436	14K10	18
0437	14K11	18
0438	14K12	18
0439	14K13	18
0440	15K03	18
0441	15K04	18
0442	15K05	18
0443	15K06	18
0444	15K10	18
0445	15K11	18
0446	15K12	18
0447	15K13	18
0448	09B10	07
0449	24R05	07
0450	01R08	07
0451	23R06	07
0452	23R09	07
0453	21R08	07
0454	20R06	07
0455	17R09	07
0456	21R11	07
0457	18R11	07
0458	19R05	07
0459	18R03	07
0460	18R08	07
0461	16R06	11
0462	22M08	11
0463	17K03	11
0464	17K06	11
0465	17K08	11
0466	17K11	11
0467	17M05	11
0468	17M11	11
0469	17M14	11
0470	18M02	11
0471	18M05	11
0472	18M11	11
0473	18M14	11
0474	16M02	11
0475	16M05	11
0476	16M11	11
0477	15C11	14
0478	15E06	14
0479	15E09	14
0480	15E12	14
0481	15E15	14
0482	15E16	14
0483	15E19	14
0484	16E02	15
0485	16E05	15
0486	16E06	15
0487	16E09	15
0488	LTAG1	15
0489	16E15	15
0490	16E16	15
0491	10B05	17
0492	10B09	17
0493	09B05	17
0494	09R09	17
0495	20D06	13
0496	OUTPUT	10
0497	10R08	10
0498	00H08	08
0500	20R12	19
0501	25B05	19
0502	14J13	18
0503	14F02	18
0504	18C10	19
0505	22K11	18
0506	14A03	16
0507	14A05	16
0508	14A11	16
0509	14A13	16
0510	14B03	17
0511	14B05	17
0512	14B11	17
0513	14B13	17
0514	RM6-02	16
0515	RM5-02	16
0516	RM38-02	16
0517	RM38-04	16
0518	RM38-06	16
0519	RM38-08	16
0520	RM38-10	16
0521	RM9-02	16
0522	RM10-02	17
0523	RM9-04	17
0524	RM39-02	17
0525	RM39-04	17
0526	RM39-06	17
0527	RM39-08	17

REVISIONS

PROTO RELEASED AT R01					
VT	JCB	—	—	11-19-81	R01
2ND PROTO RELEASE AT R02:					
JAH	[illegible]	—	—	12-31-81	R02 X
AREA M4 NET 488 WAS 16E12.					
MF	JCB	5747	MS	9-26-84	R03 X

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Oceanport, N.J. 07757

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TITLE SCHEMATIC
CROSS REF., NET#, MNEMONIC, SHT#
I. D. C.

TASK 03983 | SHT 22-23
DWG 35-807 R03 D08

DRAFTER: P. MARCUS
DATE: 8-13-81

NOTES

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NET	MNEMONIC	SHT
0528	RM39-10	17
0529	RM10-04	17
0530	RM6-04	14
0531	RM5-04	14
0532	RM6-06	14
0533	RM5-06	14
0534	RM5-08	14
0535	RM6-08	14
0536	RM10-06	14
0537	RM9-06	14
0538	RM10-08	14
0539	RM9-08	14
0540	RM10-10	14
0541	RM9-10	14
0542	RM30-04	15
0543	RM29-04	15
0544	RM25-04	15
0545	RM24-04	15
0546	RM19-04	15
0547	RM18-04	15
0548	RM14-04	15
0549	RM13-04	15
0550	RM30-06	17
0551	RM29-06	17
0552	RM25-06	17
0553	RM24-06	17
0554	RM19-06	17
0555	RM18-06	17
0556	RM14-06	17
0557	RM13-06	17
0558	RM30-08	16
0559	RM29-08	16
0560	RM25-08	16
0561	RM24-08	16
0562	RM19-08	16
0563	RM18-08	16
0564	RM14-08	16
0565	RM13-08	16
0566	RM30-02	16
0567	RM29-02	16
0568	RM25-02	16
0569	RM24-02	16
0570	RM19-02	16
0571	RM18-02	16
0572	RM14-02	16
0573	RM13-02	16
0574	RM29-10	16
0575	RM30-10	16
0576	RM24-10	16
0577	RM25-10	16
0578	RM18-10	16
0579	RM19-10	16
0580	RM13-10	16
0581	RM14-10	16
0582	RM5-10	17
0583	04R04	05

NET	MNEMONIC	SHT
0585	18H09	06
0587	SNSO	05
0588	BUSSWO	06
0589	04B08	06
0592	WXCIN1	13
0593	OC1	03
0594	OFFO	07
0595	OFLOW1	12
0596	ONO	07
0597	ONCYLA1	14
0598	ONCYLB1	14
0599	ONCYLO	14
0600	OBCADY1	17
0601	OBCADZ1	17
0602	OPTPTCL1	03
0603	OSCO	19
0604	OUPACKO	04
0605	09R04	04
0606	OVERRUNO	06
0607	P11	17
0608	P21	11
0609	P31	11
0610	PA01	08
0611	PA11	08
0612	PA21	08
0613	PA31	08
0614	PA41	08
0615	PA51	08
0616	PA61	08
0617	PA71	08
0618	PA81	08
0619	PA91	08
0620	PA90	10
0637	PAGE131	12
0638	PAGE231	12
0640	HOLDO	17
0641	POEO	09
0642	POE1	09
0643	PROMEN1	10
0644	PZO	08
0645	QSH1FT11	12
0646	QSHIFT21	12
0647	RAM01	08
0648	RAM11	08
0649	RAM21	08
0650	RAM31	08
0651	RAM41	08
0652	RAM51	08
0653	RAM61	08
0654	RAM71	08
0655	04R12	04
0656	RACKO	04
0657	RAF/OE1	08
0658	RAMBZO	07
0659	RAMIFR1	07
0660	RAMXFRO	07

NET	MNEMONIC	SHT
0661	RBO1	09
0662	RB11	09
0663	RB21	09
0664	RB31	09
0665	RBCO	05
0666	RBDO	05
0667	RBDI001	08
0668	RBDI011	08
0669	RBDI021	08
0670	RBDI031	08
0671	RBDI041	08
0672	RBDI051	08
0673	RBRA01	10
0674	RBRA11	10
0675	RBRA21	10
0676	RBRA31	10
0677	RBRA41	10
0678	RBRA51	10
0679	RBRA61	10
0680	RBRA71	10
0681	RBRA81	08
0682	RBRA91	08
0683	RBSO	05
0684	RCLK01	16
0685	RCLK11	16
0686	RCLK21	16
0687	RCLK31	16
0688	RCLKOA1	16
0689	RCLKOB1	16
0690	RCLK1A1	16
0691	RCLK1B1	16
0692	RCLK2A1	16
0693	RCLK2B1	16
0694	RCLK3A1	16
0695	RCLK3B1	16
0696	RCM1	09
0697	RCMT1	08
0698	RDATOA1	16
0699	RDATOB1	16
0700	RDAT1A1	16
0701	RDAT1B1	16
0702	RDAT2A1	16
0703	RDAT2B1	16
0704	RDAT3A1	16
0705	RDAT3B1	16
0706	RDATAO1	16
0707	RDATA11	16
0708	RDATA21	16
0709	RDATA31	16
0710	RDHIBYTO	06
0711	RDLOBYTO	06
0712	READ1	12
0713	UNRDYLAI	14
0714	UNRDYLBI	14
0715	READIO	14
0716	REGSYNC	06

NET	MNEMONIC	SHT
0717	RGATE1	07
0718	RGATEO	18
0719	RI01	09
0720	RI11	09
0721	RI21	09
0722	RI31	09
0723	RI41	09
0724	RI51	09
0725	RI61	09
0726	RI71	09
0727	RI81	09
0728	RMA1	08
0729	RMB1	08
0730	RMC1	08
0731	RMCE1	08
0732	RMI1	09
0733	RMWE1	08
0734	RPOE1	09
0735	RPZO	08
0736	RRAO	05
0737	RRA01	08
0738	RRA11	08
0739	RRA21	08
0740	RRA31	08
0741	RRA41	08
0742	RRA51	08
0743	RRA61	08
0744	RRA71	08
0745	RSEL1	03
0746	RSHIFT11	12
0747	RSHIFT21	12
0748	RSI01	09
0749	RSI11	09
0750	RSI21	09
0751	RSI31	09
0752	RSR001	18
0753	RSTIDLO	05
0754	RWCLKO	07
0755	RWCLK1	16
0757	RWGATEO	19
0758	SATNO	04
0759	SBSI01	06
0761	SCHKO	06
0762	SCLRC	03
0763	SDATA1	18
0764	SECO	05
0765	SECTOR1	19
0766	SECTOA1	17
0767	SECTOB1	17
0768	SECT1A1	17
0769	SECT1B1	17
0770	SECT2A1	17
0771	SECT2B1	17
0772	SECT3A1	17
0773	SECT3B1	17
0774	SECTOV0	19

NET	MNEMONIC	SHT
0775	SEL1	17
0776	SELO1	15
0777	SEL11	15
0778	SEL21	15
0779	SEL31	15
0780	USELOA1	15
0781	USELOB1	15
0782	USEL1A1	15
0783	USEL1B1	15
0784	USEL2A1	15
0785	USEL2B1	15
0786	USEL3A1	15
0787	USEL3B1	15
0788	USFLOI1	17
0789	USELOZ1	17
0791	USELIZI	17
0792	SELCHDAR1	07
0793	SELCHDRO	07
0794	SELCHBZ1	06
0795	SELCHXFR0	07
0796	SELCHXFR1	07
0797	SCLKOA1	17
0798	SCLKOB1	17
0799	SCLK1A1	17
0800	SCLK1B1	17
0801	SCLK2A1	17
0802	SCLK2B1	17
0803	SCLK3A1	17
0804	SCLK3B1	17
0805	SETIDLO	05
0806	20J06	07
0808	SIO1	09
0809	SI11	09
0810	SI21	09
0811	SI31	09
0812	SIGN1	12
0813	SKENDO1	16
0814	SKEND11	16
0815	SKEND21	16
0816	SKEND31	16
0817	SKEDOA1	16
0818	SKEDOB1	16
0819	SKED1A1	16
0820	SKED1B1	16
0821	SKED2A1	16
0822	SKED2B1	16
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0833	LOI	15
0834	SR1	03
0835	SR0	03
0836	SSYNO	05
0837	STCHK1	06
0838	14E07	10
0839	STPSLCHO	05
0840	STNO1	06
0841	STN11	06
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0846	SCTZ1	15
0847	SHTY1	15
0848	SHTZ1	15
0849	CTY1	15
0850	CTZ1	15
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0890	XFERLOO	05
0891	XFRDONE1	07
0892	XFRREQ1	07
0893	XFRSYNCO	07
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0897	LME1	12
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0901	IPRTO	03
0902	23J61	06
0903	22J35	06
0904	GND00F	12
0905	GND06A	16
0906	GND07A	16
0907	GND09A	16
0908	GND10A	17
0909	GND12A	16
0910	GND13A	16
0911	GND14A	16
0912	GND15A	14
0913	GND16A	14
0914	GND17A	15
0915	GND14B	17
0916	GND19C	19
0917	GND21C	05
0918	GND06E	08
0919	GND07E	08
0920	GND14E	10
0921		
0922		
0923	GND04F	05
0924	GND05F	05
0925	GND06F	05
0926	GND07F	05
0927	GND08F	12
0930	GND18F	06
0931	GND04J	05
0933	GND12J	13
0934	GND13J	13
0935	GND14J	18
0936	GND15J	18
0937	GND19J	07
0938	GND22J	06
0939	GND10K	03
0940	GND12K	12
0941	GND13K	18
0942	GND16K	18
0943	GND23K	06
0944	GND04M	04
0945	GND05M	04

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0947	GND07M	04
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0957	GND23R	07
0958	GND00K	04
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0980	EBLPRTL1	06
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0982		
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0984	EOXFR1	06
0985	STOPDMAO	06
0986	DMAXFR1	06
0987	GND19D	06
0988	16J08	06
0989	20D11	06
0990	20D08	06
0992	00K16	03
0993	00K12	03
0994	03K12	03
0995	00K14	03
0996	03R02	03
0997	DISCHARGE	10
0998	BL	06
0999	GND17H	07
1000	GND21D	06
1001	GND20H	06
1002	XFRSYNCH1	07
1003	P504K	03
1004	P522J	06

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1005	GND03K	03
1006	GND06K	03
1007	22M12	04
1008	22E06	04
1009	22J06	04
1010	22J07	04
1011	22J12	04
1012		
1013	21H06	06
1014	16H08	06
1015	21R03	06
1016	GND21H	06
1017	FOUNDØ	05
1018	22D08	04
1019	DLYSYNC1	07
1020	09R06	07
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1030	13H08	6
1031	04B02	6
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1045	17D07	19
1046	17 D06	19
1047	17D05	19
1048	GND17D	19
1049	P517D	19
1050	P519K	19
1051	23H11	19

REVISIONS

PROTO RELEASED AT R01					
VT	JRB	—	—	11-19-81	R01
2ND PROTO REL AT R02.					
E.C.J.	BWL	—	—	12-31-81	R02
ADDED NETS 1017-1020, AREA M3.					
BWL	BWL	—	—	1-14-82	R03 X
NET 1012 WAS P519D. NET 1019 WAS GND23F, SHT 6. NET 1020 WAS 23F15, SHT 6. NETS 1021 THRU 1023 WERE ADDED.					
E.C.J.	BWL	5012	M	3-2-82	R04
DELETED NET 1023, ADDED NET 1024.					
BWL	SKE	5024	M	3-15-82	R05 X
DELETED "P21" SHT "4" FROM NET 1012					
JLV	JLV	5127	M	7-26-82	R06 X
ADDED NEW NETS 1025-1028:					
JAH	JLV	5188	M	11-1-82	R07 X
ADDED NETS 1029 THRU 1033.					
KR	JLV	5311	MS	3-31-83	R08 X
ADDED NETS 1034 & 1035.					
DB	KR	5549	MS	12-20-83	R09 X
ADDED NETS 1036 & 1037					
HH	JLV	5668	MS	4-30-84	R10 X
ADDED NEW NETS 1038-1051. DELETED NET 970					
MF	JRB	5747	MS	9-26-84	R11 X

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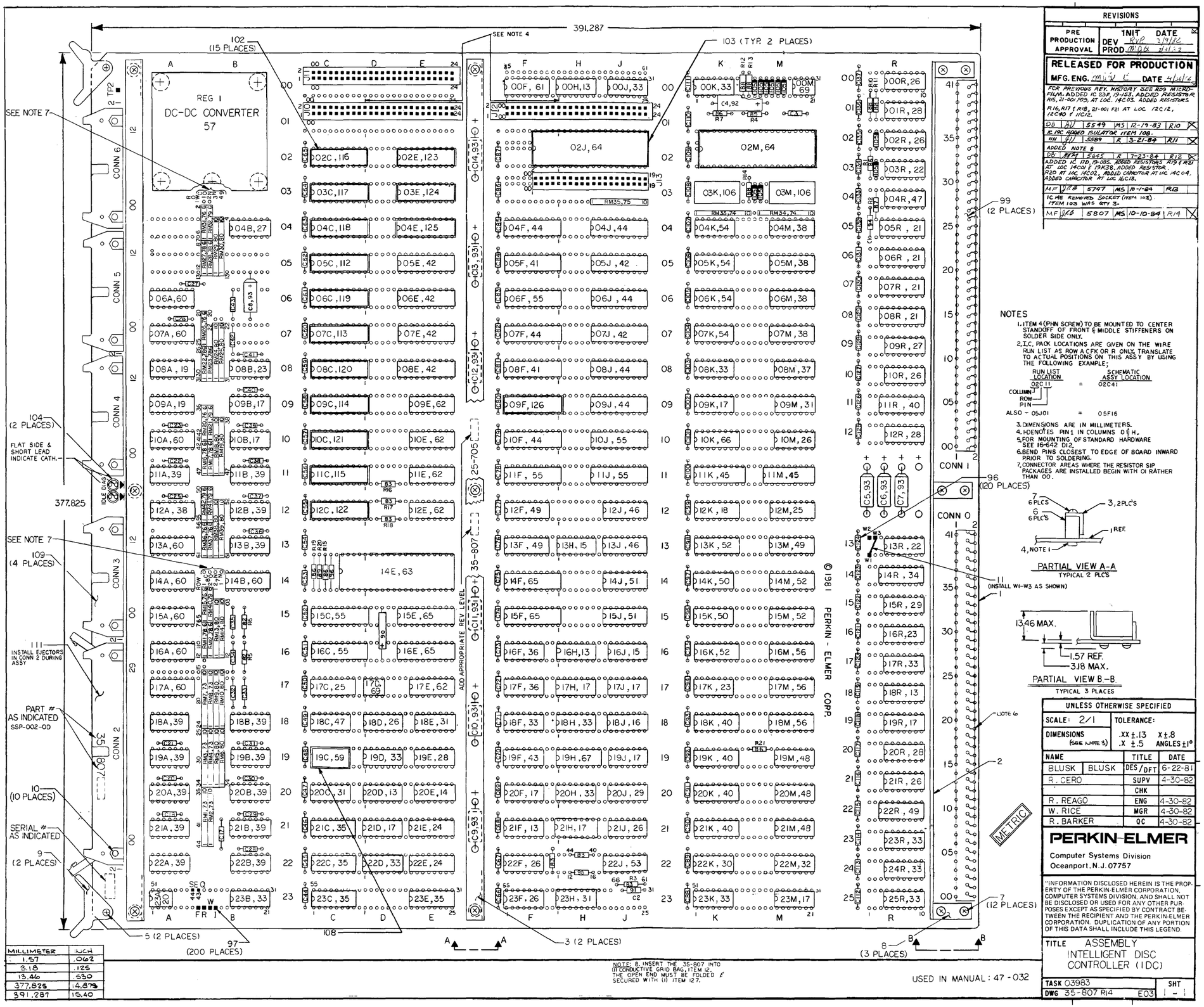
TITLE SCHEMATIC
CROSS REF, NET#, MNEMONIC, SHT#
I.D.C.

DRAFTER: P. MARCUS
DATE: 8-13-81

TASK 03983
DWG 35-807 R11 D08
SHT 23-23

NOTES

BRUNING 44-131 40579-2



MILLIMETER	INCH
1.57	.062
3.18	.125
13.46	.530
377.825	14.873
391.287	15.40

NOTE: 8. INSERT THE 35-807 INTO (1) CONDUCTIVE GRID BAG, ITEM 12. THE OPEN END MUST BE FOLDED & SECURED WITH (1) ITEM 127.

USED IN MANUAL : 47 - 032

REVISIONS		
PRE PRODUCTION APPROVAL	INIT	DATE
	DEV RVB	2/9/82
	PROD MDK	2/21/82

RELEASED FOR PRODUCTION

MFG. ENG. MJW DATE 4/6/84

FOR PREVIOUS REV. HISTORY SEE ROS MICRO FILM. ADDED IC 23J, 19-123. ADDED RESISTOR R15, 21-001 703, AT LOC. 14C03. ADDED RESISTORS R16, R17 & R18, 21-001 F21 AT LOC. 12C12, 12C90 & 11C12.

DB	RVB	5549	MS 12-19-83	R10
IC PRC ADDED ISULATOR ITEM 108.				
NH	RVB	5589	R 3-21-84	R11
ADDED NOTE 8				
DB	RVB	5645	R 7-23-84	R12
ADDED IC 17D, 19-085. ADDED RESISTORS R19 & R21 AT LOC. 14C01 & 19K38. ADDED RESISTOR R20 AT LOC. 14C02. ADDED CAPACITOR AT LOC. 14C04. ADDED CAPACITOR AT LOC. 16C13.				
MF	RVB	5747	MS 10-1-84	R13
IC ME REMOVED SOCKET (ITEM 103). ITEM 103 WAS QTY 3.				
MF	RVB	5807	MS 10-10-84	R14

NOTES
1. ITEM 4 (PHN SCREW) TO BE MOUNTED TO CENTER STANDOFF OF FRONT & MIDDLE STIFFENERS ON SOLDER SIDE ONLY.
2. I.C. PACK LOCATIONS ARE GIVEN ON THE WIRE RUN LIST AS ROW A CFK OR R ONLY. TRANSLATE TO ACTUAL POSITIONS ON THIS ASSY BY USING THE FOLLOWING EXAMPLE;

RUN LIST LOCATION		SCHEMATIC ASSY LOCATION
02C11	=	02C41

COLUMN
ROW
PIN

ALSO - 05J01 = 05F16

3. DIMENSIONS ARE IN MILLIMETERS.
4. H DENOTES PIN 1 IN COLUMNS D & H.
5. FOR MOUNTING OF STANDARD HARDWARE SEE 16-642 D12.
6. BEND PINS CLOSEST TO EDGE OF BOARD INWARD PRIOR TO SOLDERING.
7. CONNECTOR AREAS WHERE THE RESISTOR SIP PACKAGES ARE INSTALLED BEGIN WITH 01 RATHER THAN 00.

PARTIAL VIEW A-A
TYPICAL 2 PLCS

PARTIAL VIEW B-B
TYPICAL 3 PLACES

11 (INSTALL W1-W3 AS SHOWN)

NOTE 6

METRIC

UNLESS OTHERWISE SPECIFIED		
SCALE: 2/1	TOLERANCE:	
DIMENSIONS (SEE NOTE 3)	.XX ±.13 .X ±.5	X ±.8 ANGLES ±1°

NAME		TITLE	DATE
BLUSK	BLUSK	DES/DFT	6-22-81
R. CERO		SUPV	4-30-82
		CHK	
R. REAGO		ENG	4-30-82
W. RICE		MGR	4-30-82
R. BARKER		QC	4-30-82

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TITLE ASSEMBLY
INTELLIGENT DISC CONTROLLER (IDC)

TASK 03983 SHT 1 - 1
DWG 35-807 R14 E03

CAUTION
PRINTED CIRCUIT PATHS AND PADS ARE SHOWN FOR PERKIN-ELMER'S INTERNAL REFERENCE INFORMATION ONLY.

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