C3

DUAL PORT COMMUNICATIONS ADAPTER

HARDWARE REFERENCE MANUAL

Document: 49-522 R00

Assembly: 480040

23 September, 1985

Table of Contents

6 Installation

Appendix A: 2661C EPCI Data Sheet

Appendix B: Engineering Drawings

List of Figures

List of Tables

Revision History

Rev	Date	Description
RØØ	Ø9/23/85	Initial Release

1 Introduction

1.1 Product Overview

The C3, Inc. Dual Port Communications Adapter (DPCA) interfaces the Perkin-Elmer Multiplexor (MUX) bus with two serial communications interfaces. These interfaces may be used for communication with a variety of terminals, serial printers, modems, and other equipment.

Each of the two ports has the following features:

- Complies with EIA standards RS-232 and RS-423, FED-STD-1030A, and MIL-STD-188-114 (unbalanced) - Inverted or non-inverted data
- Operates in synchronous, asynchronous, or isochronous modes
- Uses internal or external baud rate clocking
- Operates in full or half duplex modes
- 16 software programmable baud rates ranging from 50 to 19200 baud
- Data character lengths of 5 to 8 bits with an additional parity bit (odd or even) if desired
- Synchronous operation with 8- or 16-bit synchronization, transparent or non-transparent, automatic sync insertion and stripping
- Asynchronous operation with 1, 1.5, or 2 stop bits; parity, overrun, and framing error detection; line break detection and generation; and false start bit detection
- Dynamic reconfiguration of operating mode, character length, and baud rate
- Full modem control capability including reverse channel (secondary transmit and receive data) and ring detect

1.2 Product Specifications

Board size	7 inch Perkin-Elmer format
Power requirements	+5 VDC: 2.0 amp +15 -0.4/+1.0 VDC: 0.1 amp -15 -1.0/+0.4 VDC: 0.1 amp
Data transmission format	5-8 data bits, 50-19200 baud async or sync
Comm output levels	±5.5 volts

2 Programming Specification

2.1 Overview

The DPCA contains two identical serial ports. Each serial port may independently operate in half or full duplex mode. Two consecutive addresses are used for each port, the first even, the second, odd. The even address is used for receive transfers while the odd is used for transmit transfers. In half duplex operation, receive and transmit both use the even address.

The heart of each serial port (or channel) is a Signetics 2661C Enhanced Programmable Communications Interface (EPCI) integrated circuit. This is a bus-oriented version of a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) which is designed to operate on a microprocessor data bus. The DPCA adapts this device to the Perkin-Elmer MUX bus.

The 2661C's contain several registers used for setting up operating modes, determining device status, and for transmitting and receiving data. Perkin-Elmer Output Commands to the DPCA select these internal registers, control interrupts, and select general DPCA modes. Data written to a DPCA channel (via a Write Data instruction) goes into the register of the EPCI specified in the last Output Command to that channel. Data read from the DPCA also comes from the register last specified.

Appendix A of this document is the data sheet from Signetics which describes in detail the capabilities, operation, and techniques for use of the EPCI.

The following sections of this chapter detail the various Perkin-Elmer I/O operations available on the DPCA.

2.2 Command Byte

The DPCA command byte controls interrupts, sets operating mode (half/full duplex, read/write), controls communication interface signals, and selects which register in the 2661C EPCI may be accessed by Read or Write Data instructions. It may be issued to the even or odd device address with the same results EXCEPT for the setting of transmit/receive mode. See the discussion of command bit 15, below for details.

The command byte has the following format.

08	09	10	11	12	13	14	15
Interrupt Control		Half Duplex	Reset EPCI	RCT	Register Sel. A0	A1	Trans. Mode

Bit 08 and 09 - Interrupt Control
These bits are used together following Perkin-Elmer interrupt control convention with bit 15 selecting either the transmit or receive side of the port being addressed. Their function is defined in Table 2-1, below.

Bit 08	Bit 09	Bit 15	Function
0	0	0	No change to receive interrupts
0	1	0	Enable receive interrupts
1	0	0	Disable (queue) receive interrupts
1	1	0	Disarm receive interrupt
0	0	1	No change to transmit interrupts
0	1	1	Enable transmit interrupts
1	0	1	Disable (queue) transmit interrupts
1	1	1	Disarm transmit interrupts

Table 2-1. Interrupt State Command Bits

Bit 10 - Half Duplex
When 1, this bit selects the half duplex mode of operation. When 0, it selects full duplex operation. This bit affects how the transmit or receive sense status register is selected (see section 2.3), whether transmit interrupts occur on the even or odd address (see section 2.5), how "clear to send" transmit interrupts are generated (see section 2.5), and how the "request to send" output is enabled (see discussion of bit 15, below).

Bit 11 - Reset EPCI
This bit activates the RESET pin on the 2661C when 1. This causes a master reset of the 2661C EPCI for the channel being accessed, on both the transmit and receive sections of the device. It terminates any EPCI activity and clears its internal mode, command, and status registers. The EPCI is in its idle mode until reinitialized.

Bit 12 - Reverse Channel Transmit (RCT)
This bit controls the state of the Reverse Channel Transmit output pin, pin 14, on the communication connector for the port being addressed. When this bit is 1, pin 14 assumes an active (high) state. When this bit is Ø, pin 14 assumes an inactive (low) state.

Bit 13 and 14 - Register Select
These bits select which of the internal registers of the 2661C EPCI will be accessed by subsequent read and write data commands. Table 2-2, below, describes the registers selected by these bits.

AØ	A1	Read Data	Write Data
Ø	Ø	Recv Holding Reg	Trans Holding Reg
Ø	1	Mode Reg 1 & 2	Mode Reg 1 & 2
1	Ø	EPCI Status Reg	Syn1/Syn2/DLE Reg
1	1	EPCI Command Reg	EPCI Command Reg

Table 2-2. Register Select Command Bits

Bit 15 - Transmit Mode
This bit controls whether this command applies to the transmit or receive side of the addressed DPCA channel. When 1 this bit indicates an affect on the transmit side, when Ø to the receive side. It is used in conjunction with the interrupt control bits, Ø8 and Ø9, to determine if transmit or receive interrupts are to be affected. When in half duplex mode, it puts the channel in either transmit or receive mode (affecting transmit or receive status register selection and the generation of "clear to send" interrupts on the transmit side).

In either full or half duplex mode, this bit affects generation of the "request to send" (RTS) output, pin 4. RTS is generated by the DPCA if the corresponding bit is set in the 2661C EPCI Command Register (refer to Appendix A, page 7) and the channel is in transmit mode.

SPECIAL NOTE: In full duplex operation (bit 1Ø off), transmit or receive mode may only be selected from the odd (transmit) device address. In full duplex mode, bit 15 of the even (receive) address may be used for selecting transmit or receive interrupt

control but it has no affect on enabling of the "RTS" output.

At system power-up (or system clear), the board is in a state that can be emulated by output commands of C1h then D0h, that is, interrupts (both transmit and receive) are disarmed, the 2661C EPCI is reset, the board is in full duplex and receive modes, RCT is off, and A0,A1 is 00 (selecting the 2661C holding registers).

2.3 Status Byte

The DPCA has two separate status bytes, one for transmit status, one for receive status. In full duplex mode, receive status is returned when a sense status is issued to the even device address while transmit status is returned from the odd address.

In half duplex mode, receive status is returned when the last command issued had a 0 in bit 15 (the Transmit Mode bit). Transmit status is returned if bit 15 was 1. In half duplex mode the same status is returned from either the even or odd device address.

Several of the status bits are extracted from the 2661C internal status register by the DPCA logic. The 2661C status register is read once by each sense status (or interrupt acknowledge cycle) from the Perkin-Elmer processor.

The receive status byte has the following format.

08	09	10	11	12	13	14	15
Over Run	Parity Error	FE/ Sync D	Ring	Recv Busy	RCR	-DCD	-DSR

Bit 08 - Overrun
This bit, when 1, indicates that the previous character received into the receive holding register of the 2661C was not read by the processor at the time a new character was received into it. This bit is cleared when the Reset command bit is issued via an output command, when the 2661C receiver is disabled, or when a reset error command is written to the 2661C command register. This bit is extracted from the 2661C internal status register.

Bit 09 - Parity Error
This bit, when set, indicates a received parity

error. It is cleared when the next character is loaded into the receive holding register of the 2661C, when the Reset command bit is issued via an output command, when the 2661C receiver is disabled, or when a reset error command is written to the 2661C command register. This bit is extracted from the 2661C status register. Consult Appendix A for further details.

Bit 10 - Framing Error/Sync Detect
In asynchronous modes of operation, this bit indicates that the received character was not framed by a stop bit. (Only the first stop bit is checked if more than one was received.) If the received character was 0 and this bit is 1, it is likely that a break condition may be present. This bit is cleared in asynchronous mode when the reset error command is written to the 2661C command register.

In synchronous transparent mode it indicates the receipt of the specified 8 or 16 bit sync sequence or, after initial synchronization, the receipt of a DLE-Sync pair. In synchronous mode, this bit is cleared by a sense status or by reading the 2661C status register. CAUTION: It has been observed that the 2661C occasionally clears this bit before it can be read if the DPCA is in a tight sense status loop.

This bit is also cleared when the Reset command bit is issued via an output command or when the 2661C receiver is disabled in either sync or async mode. This bit is extracted from the 2661C status register. Consult Appendix A for further details.

Bit 11 - Ring
This bit is 1 when the Ring signal line from the communication line, pin 22, is on (high).

Bit 12 - Receive Busy
This bit, when 1, indicates that no data byte is ready to be read from the 2661C receive holding register. It is generated directly by the -RxRDY output pin from the 2661C. This bit is set when the processor reads the receive holding register or when the receiver is disabled.

Bit 13 - RCR (Reverse Channel Receive)
This bit is 1 when the RCR signal line from the communication line, pin 16, is on (high).

Bit 14 - -DCD (Not Data Carrier Detect)
This bit is 1 when the DCD signal line from the communication line, pin 8, is off (low). This bit is extracted from the 2661C status register.

Bit 15 - -DSR (Not Data Set Ready)
This bit is 1 when the DSR signal line from the communication line, pin 6, is off (low). This bit is extracted from the 2661C status register.

The transmit status byte has the following format.

08	09	10	11	12	13	14	15
0	0	0	Ring	Trans Busy	RCR	-CTS	-DSR

Bit 11 - Ring
(See Transmit Status register bit 11, above.)

Bit 12 - Transmit Busy
This bit, when 1, indicates that the transmit holding register of the 2661C has been loaded by the processor and the data has not been transferred to the transmit shift register. This bit is initially 0 when the transmitter is enabled. It is generated directly by the -TxRDY output pin from the 2661C. Consult Appendix A for further information.

Bit 13 - RCR (Reverse Channel Receive)
(See Transmit Status register bit 13, above.)

Bit 14 - -CTS (Not Clear to Send)
This bit is 1 when the CTS signal line from the communication line, pin 5, is off (low). This bit reflects the -CTS input bit to the 2661C. It must be 0 for the transmitter to operate. If it goes high during transmission, the character in the transmit shift register is completed before transmission stops. Consult Appendix A for further explanation.

Bit 15 - -DSR (Not Data Set Ready)
(See Transmit Status register bit 15, above.)

2.4 Data Transfers

Data transfers, read data and write data, on the DPCA transfer data into or out of the 2661C register specified in the last output command instruction. Refer to Table 2-2, above, for the register select codes. Data transfers may be done to either the even or odd address with exactly the same effect.

Transfers to the transmit holding register in the 2661C (A0=A1=0) should be done only when the transmit sense status register Transmit Busy bit, 12, is 0. Likewise, reading of data from the 2661C internal receive holding register (A0=A1=0) should only occur when the receive sense status register Receive Busy bit is 0. Transfers to the other internal registers are not governed by the busy bits.

Refer to Appendix A for 2661C EPCI usage. This document defines the 2661C's internal registers and the recommended initialization sequence for the device. If the device has been initialized for transmitting, the Transmit Busy status bit should be 0, indicating that the 2661C is ready to accept a data byte. If initialized for receiving data, Receive Busy status should be 1, indicating no data available. If Receive Busy is 0, a byte may be read from the receive holding register to force Receive Busy to 1.

2.5 Interrupts

Each channel of the DPCA has two different types of interrupts, one for transmit and one for receive. These interrupts are separately controllable by command to the DPCA, see section 2.2 for details. These interrupt circuits may be in one of three states. (These states are standard for Perkin-Elmer controllers.) They are:

1) Enabled - Interrupts generated by the channel are passed through to the processor.

2) Disabled - Interrupts generated by the channel are not passed to the processor but are queued. When the interrupt logic is later enabled, a queued interrupt will be passed to the processor.

3) Disarmed - Interrupts generated by the channel are neither passed on to the processor nor queued. Any queued interrupts are ignored.

At power up, all interrupt circuits on the DPCA are disarmed.

The conditions which cause transmit and receive interrupts are shown in Table 2-3, below. NOTE: The transmit interrupt caused by the 1 to Ø transition of the -CTS signal only occurs when the channel is in half duplex, transmit mode. This interrupt is also generated if -CTS is Ø when half duplex, transmit mode is entered.

Signal	Transition	Interrupt
Ring	Ø to 1	Receive
-DCD	Ø to 1, 1 to Ø	Receive
RCR	Ø to 1, 1 to Ø	Receive
-DSR	Ø to 1	Receive
RxBusy	1 to Ø	Receive
TxBusy	1 to Ø	Transmit
-CTS	Ø to 1, 1 to Ø*	Transmit

*see note in text

Table 2-3. DPCA Interrupt Sources

In full duplex operation, receive interrupts come from the even device address and transmit interrupts from the odd device address. In half duplex mode, both receive and transmit interrupts use the even device address.

Within the DPCA board, the following interrupt priority is followed:

1) Channel A Receive Interrupt (highest)

2) Channel A Transmit Interrupt

3) Channel B Receive Interrupt

4) Channel B Transmit Interrupt (lowest)

NOTE: During the interrupt acknowledge cycle, the Perkin-Elmer processor issues a sense status to the interrupting device. This sense status resets the "Sync Detect" status bit, if set. See section 2.3, above, for more information.

2.6 Typical Code Sequence

This section presents the flow for a few typical code sequences for controlling a DPCA.

Note in these examples that the last Output Command to the channel contains 00 in the register select field and that processor interrupts are disallowed while the register select bits are nonzero. This keeps transmit and receive logic from interfering with each other during full duplex operation.

```
/*   Reset the DPCA hardware.  This sequence    */
/*   emulates conditions found at Power-up or   */
/*   Init for the channel being accessed        */
ResetChannel:
     OutputCommand C1h   /* disarm Tx ints */
     OutputCommand D0h   /* disarm Rx ints,init 2661 */

/*   Initialize the 2661C internal registers    */
InitChannel:
     LockoutInterrupts
     OutputCommand 02h        /* select mode regs */
     Call InitEpciModeRegs    /* see appendix A */
     OutputCommand 04h        /* select sync regs */
     Call InitEpciSyncRegs    /* see appendix A */
     OutputCommand 00h        /* select hold regs */
     AllowInterrupts

/*   Start-up transmitter                       */
StartTransmitter:
     LockoutInterrupts
     OutputCommand 06h        /* select cmd reg */
     WriteData (TxInitCmd)    /* init cmd reg */
     OutputCommand 41h        /* select holding regs
                                 & enable Tx ints */
     AllowInterrupts

/*   Stop transmitter                           */
StopTransmitter:
     LockoutInterrupts
     OutputCommand 06h        /* select cmd reg */
     WriteData (TxStopCmd)    /* modify cmd reg */
     OutputCommand C1h        /* select holding regs
                                 & disarm Tx ints */
     AllowInterrupts
```

```
/*   Start-up receiver                                    */
StartReceiver:
     LockoutInterrupts
     OutputCommand Ø6h          /* select cmd reg */
     WriteData (RxInitCmd)      /* init cmd reg */
     OutputCommand 4Øh          /* select holding regs
                                   & enable Rx ints */
     AllowInterrupts

/*   Stop receiver                                        */
StopReceiver:
     LockoutInterrupts
     OutputCommand Ø6h          /* select cmd reg */
     WriteData (RxStopCmd)      /* modify cmd reg */
     OutputCommand CØh          /* select holding regs
                                   & disarm Rx ints */
     AllowInterrupts
```

3 Theory of Operation

3.1 Overview

The C3 Dual Port Communication Adapter (DPCA) contains two independent serial communication ports on a single half-board. The two ports (or channels) are identical in function.

The functional block diagram for the DPCA is shown on sheet 1 of the schematic drawings in Appendix B. This chapter presents the theory of operation for each functional block. Where the two ports have separate but identical blocks, only the A port is discussed.

References are made throughout this chapter to the schematic drawing for the DPCA contained in Appendix B. These references are of the form [pPzZZ] where "P" is the page (sheet) number of the schematic and "ZZ" is the zone on that sheet in alphabetic column and numeric row. Signal names ending with "Ø" are active low, those ending with "1" are active high.

3.2 Bus Transceiver Logic

The DPCA is a byte oriented device and therefore uses only the low-order eight bits of the MUX bus for data transfers. These signals are buffered using a pair of 8T26A tri-state transceivers [p6zD2]. This buffered tri-state bus, TSBØ81 through TSB151, is used throughout the DPCA by both the A and the B port logics. This bus normally is driven from the MUX bus. During transfers from the DPCA to the processor, the transceivers are turned around to drive the MUX bus from the tri-state bus.

This turn around occurs during data requests (ADRGØ or BDRGØ), status requests (ASRGØ or BSRGØ), or interrupt acknowledgment cycles (ARATNØ or BRATNØ), controlled by a 7430 8-input NAND gate [p6zC2].

The transceiver logic also provides Schmidt input receivers for the system clear signal (SCLRØ) and the data signals (DØ6Ø and DØ7Ø) from the MUX bus. These extra data bits are used for address recognition purposes only. The buffered system clear signal, CSCLRØ, is used throughout the board for initializing latches and the 2661C EPCI's at system power-up and system reset.

3.3 Address Logic

The DPCA has separate address logic for the A and the B ports. Each port responds to two addresses, determined by the high-order nine bits of the ten bit device address. The even port (low-order address bit is Ø) is used for receive side transfers in full duplex mode and for all transfers in half duplex mode. The odd port is used for transmit transfers in full duplex mode.

This logic has the function of recognizing the port address, determining if the even or odd address is being used, acknowledging the address transfer from the processor, and generating the interrupt vector for interrupt acknowledgment cycles.

The Perkin-Elmer MUX bus uses a 1Ø-bit device address. The low order ten data bits of the MUX bus are used for this address. To select a device, the processor places the board's address on the MUX bus and then asserts ADRSØ on the bus. This address is held on the bus until the addressed board responds with SYNCØ to acknowledge this transfer.

The port address is configured by a 7-position device address jumper strip [p2zD2] and by a 6-position extra address jumper [p2zE2]. The selected address is constantly being compared with the contents of bits Ø6 through 14 of the local tri-state bus by an XOR gate [p2zF1], which produces a low when DØ61 matches the high order selection, and a 25LS2521 8-bit comparator [p2zC1].

The leading edge of ADRSØ from the processor latches the output of this comparison into the address flag latch [p2zF3] to produce the signal AADF1, which indicates that this port is addressed. Simultaneously, the low order address bit is latched from TSB151 by a 7474 [p2zE3] to determine if the even (receive) or odd (transmit) device address has been selected.

If the port is addressed and in full duplex mode, the A Send Address signal, ASADR1 [p2zG3], or the A Receive Address signal, ARADR1 [p2zG3], is activated if this odd address latch is 1 or Ø, respectively.

The signal AADSYNØ [p2zG3] is used to generate the SYNCØ output to the processor. This signal acknowledges that the board has been addressed. It is active only while ADRSØ is on and the address flag latch is active.

During the interrupt acknowledge cycle, the address logic places the device address onto the tri-state bus for transfer to the processor. This is done by a 74LS241 non-inverting octal buffer [p2zC5] on receipt of the A Receive Attention (ARATNØ) signal [p2zC6]. The low order bit of this returned address is 1, indicating the odd (transmit) device, only when a transmit interrupt is present (AWRTINT1) and the port is in full duplex mode. The two high order address bits are driven directly onto the MUX bus by the 7438 gates located at [p2zF1] and [p2zF2].

3.4 Bus Control Logic

This logic receives the MUX bus data transfer control signals and gates them with the address flag signals from the A and B port address logic to generate the gated control signals used throughout the DPCA logic modules. In addition, the data transfer acknowledge signal, SYNCØ, is generated by this logic.

Four MUX bus control signals, command (CMDØ), status request (SRØ), data request (DRØ), and data available (DAØ), are received by a 74LS241 non-inverting tri-state buffer [p7zB5]. This buffer is enabled by the A Address Flag signal, AADF1. When not enabled, the outputs of the '241 are in high impedance mode, allowing the 4.7 Kohm pull-up resistors to force the signals inactive (high) when the port is not addressed by the processor.

The MUX bus data transfer acknowledge signal, SYNCØ (or SYNØ) [p7zG3] must be generated by the addressed port in response to all transfers to or from that port on the MUX bus. The six types of transfers are:

1) Address transfer (ADRSØ)
2) Command (CMDØ)
3) Status Request (SRØ)
4) Data Available (DAØ)
5) Data Request (DRØ)
6) Interrupt acknowledge (RACKØ)

These signals, after appropriate gating through both ports, are logically ORed by the 74S133 13-input NAND gate [p7zF3]. When any of these signals is asserted, C66 [p7zF4] begins

charging through R66. After approximately 350 ns., the output of the 7408 [p7zG3] goes high, generating SYN0. When the control signal is deasserted, SYN0 is immediately released and C66 is quickly discharged through CR9. The 350 ns. delay allows data to stabilize on the MUX bus when the DPCA is transmitting to the host. Although generated for data coming from the processor as well, the delay is not required in this case.

3.5 Status Logic

Each port of the DPCA has two status registers, one for receive status and one for transmit. The A port receive status register is generated by a 74LS241 8-bit non-inverting buffer [p2zB5]. This buffer, when enabled, places a variety of signals onto the DPCA's tri-state bus. The buffer is enabled when the gated status request signal, ASRG1 [p2zA6], is active and either the port is in full duplex mode and the even device is being addressed (ARADR1) or the port is in half duplex receive mode (AHWRT0 false).

Similarly, the transmit status register is a 74LS241 [p2zB3] which is enabled when gated status request is active and either the port is in full duplex mode and the odd device is being addressed (ASADR1) or the port is in half duplex transmit mode (AHWRT1).

3.6 Command Logic

Each port of the DPCA has its own command logic, and these logics are identical in function. The DPCA command logic captures command data transmitted by the processor.

The command data processed by the command logic set the operating modes for the port, select which internal register(s) of the 2661C EPCI are to be accessed, reset the 2661C, and determine the state of the Reverse Channel Transmit output on the communication port. The high-order two command data bits are used for interrupt control and are discussed in section 3.8.1, below.

When the port is addressed (either even or odd address) and CMD0 is asserted on the MUX bus, the gated command signal, ACMG1 [p3zA4] is generated by the DPCA control logic. On the leading edge of this signal, bits 10, 12, 13, and 14 are latched into a 74175 quad D-type latch [p3zC3&C4]. These bits are "Half Duplex", "RCT", "A0", and "A1", respectively.

Data bit 15, "Transmit Mode", is latched into the transmit/receive mode latch [p3zC1] at this time only if the port is in (or entering) half duplex mode (command bit 10 = 1) or if the port is in full duplex mode and the odd (transmit) address is being accessed. Therefore, if the channel is in full duplex mode and a command is issued to the even (receive) address, transmit/receive mode is not modified.

If the "Reset EPCI" bit of the command, bit 11, is on, the signal ARST1 [p3zB4] is generated for the duration of the CMD0 pulse from the processor. This signal causes the 2661C EPCI reset pin to be activated. Note that ARST1 is also generated by system clear (CSCLR0), which comes from the MUX bus SCLR0 signal.

Two additional signals are generated by this logic, AHWRT1 [p3zD2] and AHWRT0 [p3zE2]. The first signal is generated when the board is in half duplex and transmit (write) mode. The second is generated when the board is in half duplex and receive mode.

3.7 2661C/Control Logic

This logic contains the 2661C Enhanced Programmable Communications Interface (EPCI) and the logic which directly controls it. Refer to Appendix A for a detailed discussion of the 2661C and its pin functions.

Three MUX bus operations transfer data into or out of the 2661C: data request (DR0), data available (DA0), and status request (SR0). During status requests, the 2661C is disconnected from the tri-state bus, its internal status register is selected, and three of the status bits are routed to the receive status register.

The 7400 and 7408 gating on the A0 and A1 inputs to the 2661C [p3zE2&E3] allows the A0 and A1 bits from the command latches through to the 2661C unless a status request is in process for this port. In that case, A0 and A1 are forced to 1 and 0, respectively, to select the internal status register.

A 74LS245 8-bit tri-state transceiver [p3zG3] is used for controlling the 2661C's access to the tri-state bus. During a status request, the transceiver is disabled, allowing the 2661C data pins to freely drive the appropriate receive status register bits.

At all other times, the transceiver is enabled. It normally transfers data on the tri-state bus to the 2661C data pins. When a data request is issued to the port, however, the direction of the transceiver is altered to allow the 2661C to drive its data onto the tri-state bus and from there onto the MUX bus.

The 2661C has several requirements on its chip enable (-CE) input. The chip enable signal must be active for a minimum of 250 ns. On reads from the 2661C, data is not valid until 200 ns. after chip enable is asserted and it is valid for at least 100 ns. after chip enable is deasserted. On writes to the 2661C, data is accepted on the trailing edge of the chip enable signal. (This differs from Perkin-Elmer convention, where data is normally accepted from the processor on the leading edge of the control signal - ADRS0, CMD0, or DA0.)

To handle these requirements, two one-shots and some special timing circuitry have been provided. Refer to the timing diagram in Figure 3-1, below, for an illustration of the chip enable timing for status requests, data requests, and data available. For both status requests and data requests, the 26S02 chip enable one-shot [p3zD4] is triggered for a maximum of approximately 350 ns. This triggering is delayed slightly (approximately 35 ns.) by C20 [p3zD5] from the leading edge of ASRG1 and ADRG1.

For writes to the 2661C, data available (ADAG1) triggers the chip enable one-shot, delayed about 35 ns. by C20. Simultaneously, C32 [p3zC6] starts charging up. After approximately 230 ns., the voltage on C32 gets to a sufficient level to trigger the chip enable reset one-shot. This resets the chip enable one-shot, ending the chip enable (-CE) for the 2661C. At this point, the data presented to the 2661C data pins is loaded into the specified register.

The transmit and receive ready pins on the 2661C, -TxRDY and -RxRDY, are open drain outputs. These signals are pulled up by 10 Kohm resistors and buffered by 74LS08 gates [p3zG4] to form the receive and transmit busy signals, ARXBSY1 and ATXBSY1.

The transmit and receive clock pins on the 2661C, TxC and RxC, are bidirectional - they may be either inputs or outputs. Direction for these pins is determined by the 2661C internal mode register setting. Figure 3-2, below, is a representation of the transmit and receive clock circuitry on the board. When using an externally supplied transmit clock on port A, jumper X17 must be opened to keep the DPCA driver from controlling pin 15 of the communication connector. X44 is installed to allow the external transmit clock

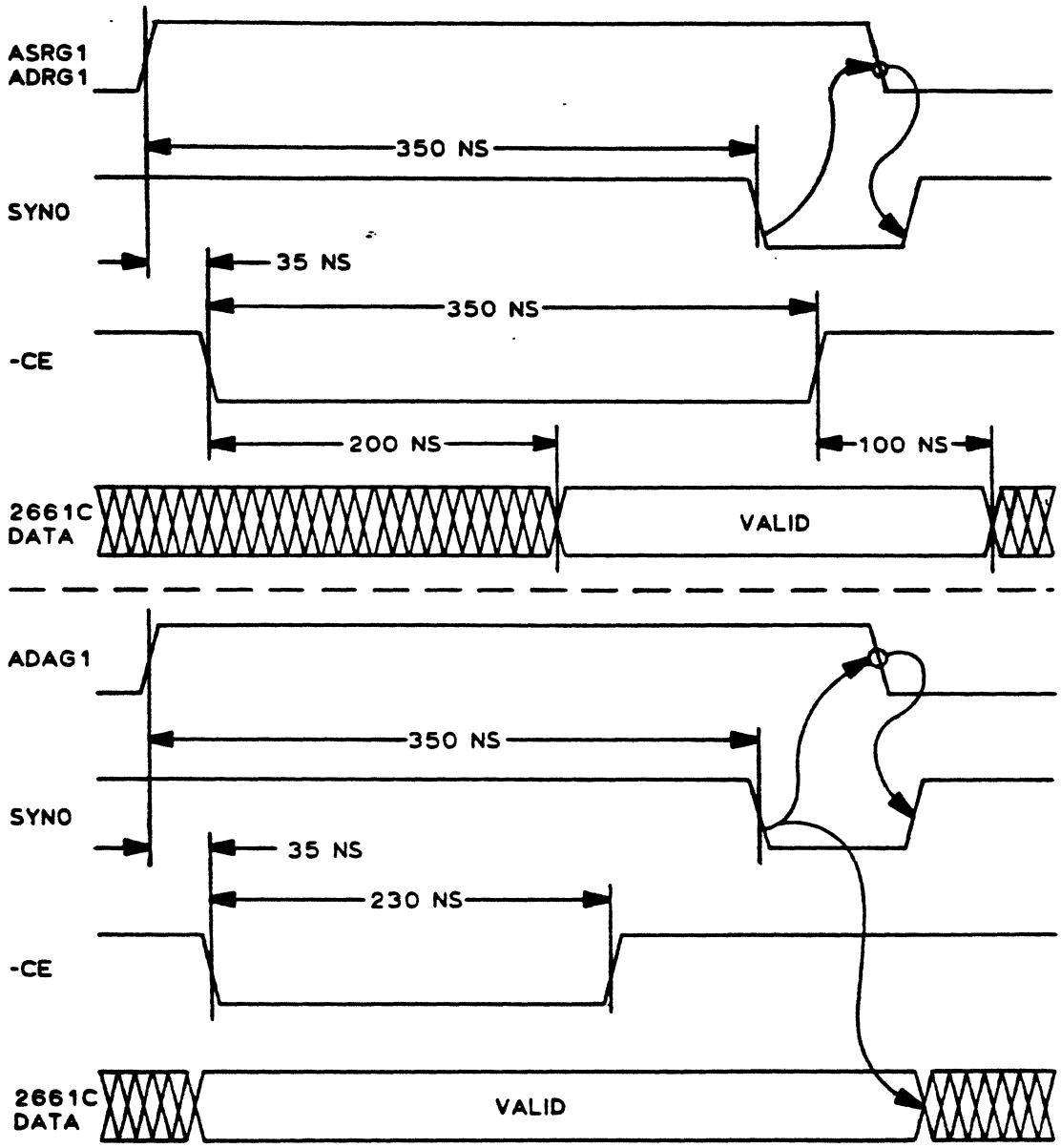


Figure 3-1. 2661C Chip Enable Timing

to enter the 2661C. When the receiver output is high, the 10 Kohm pull-up resistor at the 2661C keeps its input high. When the receiver output goes low, the 2661C pin is pulled low through the diode.

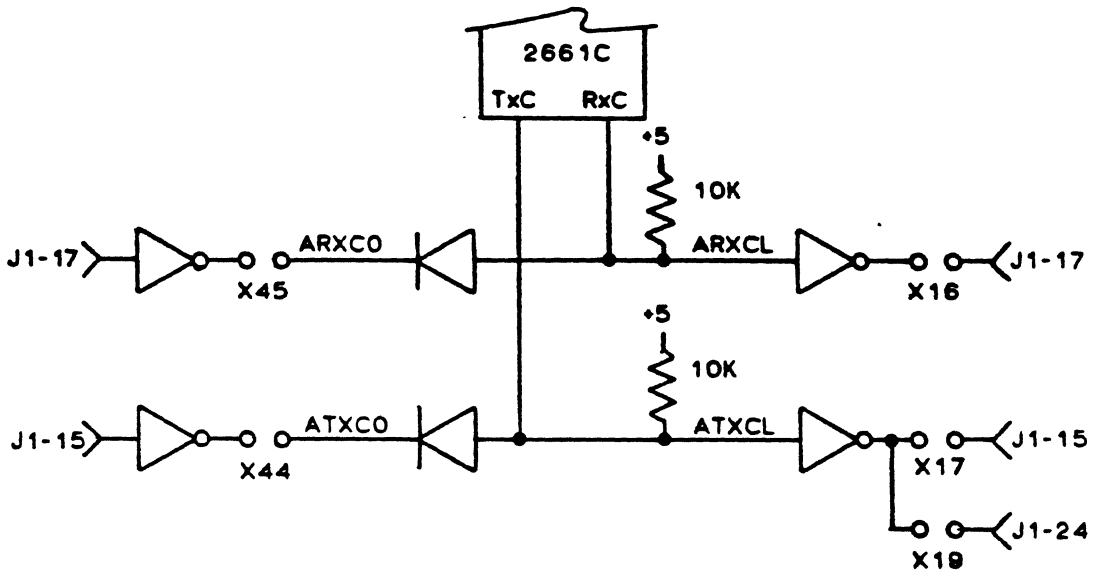


Figure 3-2. Transmit/Receive Clock Logic

When using an internally supplied receive clock on port A, X45 should be removed and X16 installed. With X15 open, the output of the receiver, ARXCØ, goes high. For externally supplied clocks, X45 should be installed and X16 removed.

3.8 Interrupt Logic

The DPCA has four sources of interrupts: transmit interrupts and receive interrupts from both the A and B ports. The logic for these interrupts is more closely shared by the two ports than that for most other functions on the board. The DPCA interrupt logic consists of three parts: the interrupt state logic, the interrupt setting logic, and the interrupt arbitration logic.

3.8.1 Interrupt State Logic

As discussed in section 2.5, the interrupt logic for the DPCA may be in three states: enabled, disabled, and disarmed. For each of the four sources of interrupts, two latches are used to maintain that source's state. One latch is active if the interrupt is enabled, the other if it is armed.

The port A receive state latches are typical of the four. These latches are 74276 J-K latches with negative clocking. The enable latch [p6zB4] has as its clock the gated command signal, ACMG1, ANDed with TSB15Ø. Therefore the latch changes state on the trailing edge of an A port command having a Ø in bit 15. Its J input is TSBØ91 and its -K input is TSBØ81. Therefore, there is no change when bits 8 and 9 are Ø, it goes high when bit 8 is 1 and bit 9 is Ø, it goes low when bit 8 is Ø and bit 9 is 1. When both bits 8 and 9 are high, this latch changes state. Therefore, when a disarm command is issued, the output of the enable latch is unknown. (In this case, it doesn't matter.)

The interrupt armed latch [p6zC4] has the same clocking as the enable latch. Its J input is 1 if bits 8 and 9 differ. Its -K input is Ø only if bits 8 and 9 are 1. Therefore, there is no change when bits 8 and 9 are Ø, it goes high when bits 8 and 9 differ, and it goes low when bits 8 and 9 are 1. This latch cannot enter the toggling state.

Both latches are cleared at system clear.

3.8.2 Interrupt Setting Logic

The interrupt setting logic for the A port is identical to that for the B port. The A port logic is discussed here. There are separate interrupt latches for transmit and receive interrupts. The transmit interrupt latch [p4zB5] is held cleared when the transmit state is disarmed.

When interrupts are armed (enabled or disabled), the transmit interrupt latch may be set by firing any of three one-shots. The rising edge of ACTSØ (CTS comm signal going inactive) fires a 26SØ2 [p4zB1]. A 74123 [p4zB2] is triggered when ACTSØ is low and AHWRT1 is high (the port is in half duplex transmit mode). Therefore this triggering occurs if in half duplex transmit mode when CTS is activated or if CTS is active when the port is placed into half duplex transmit mode. A third one-shot, a 74123 [p4zB4], is triggered when transmit busy (ATXBSY1) falls.

Once the transmit interrupt latch is set, it is gated with the enable and armed (ASEN1 and ASDSMØ) signals to generate the MUX bus attention signal, ATNØ [p4zG6]. This latch stays set until the transmit interrupt is acknowledged.

To acknowledge the transmit interrupt, the interrupt arbitration logic generates the A port received attention (ARATN1) signal [p4zC6].

The receive interrupt request is inverted and fed to the transmit interrupt logic as AWRTINT1 [p4zB6]. If no receive interrupt request is present, the output of the 7400 NAND gate [p4zB5] goes low when ARATN1 goes active and the transmit latch is clocked when ARATN1 ends. While a transmit interrupt request is being acknowledged, receive interrupts are redundantly inhibited by the 7408 gate [p4zE6] and by CR7 [p4zD6].

Receive interrupts have priority over transmit interrupts. If the receive interrupt latch [p4zE6] is active and enabled, the 7400 transmit interrupt acknowledge gate [p4zB5] is disabled because AWRTINT1 is off. The receipt of ARATN1 therefore clears the receive interrupt latch [p4zE6].

The receive interrupt latch is set when:

- The data set ready (DSR) comm signal drops, forcing ADSRØ to go high and trigger a 26SØ2 one-shot [p4zE1],
- The receive busy signal (ARXBSY1) signal drops, triggering a 26SØ2 one-shot [p4zE3],
- The ring comm signal becomes active, forcing ARING1 high and thereby triggering a 26SØ2 one-shot [p4zE4],
- The reverse channel receive (RCR) comm signal changes, forcing ARCR1 to change. This causes a momentary low from a 7486 XOR gate [p4zE4], or
- The data carrier detect (DCD) comm signal changes, changing ADCD1 and thereby pulsing the output of an XOR gate [p4zE5] low.

3.8.3 Interrupt Arbitration Logic

The RACKØ signal is sent by the processor in response to an attention request (ATNØ) by one or more boards on the MUX bus. The RACKØ signal is daisy-chained from board to board. The board with the highest interrupt priority gets RACKØ first. If it does not have an interrupt pending it passes it to the next board in the interrupt chain by activating

TACKØ, which is connected to the RACKØ signal of the next board.

The interrupt arbitration logic is used to route the received interrupt acknowledge signal, RACKØ [p6zA2], to either the A port, the B port, or to the next board in the interrupt acknowledge chain.

If the A port is requesting an interrupt (AINT1 is high), the acknowledge is passed to the A port via ARATNØ [p6zC4]. If the A port is not requesting an interrupt but the B port is (BINT1 is high), the acknowledge is passed to the B port via BRATNØ [p6zG3]. Otherwise, the transmit acknowledge signal, TACKØ [p6zG2], is activated and sent to the next board in the acknowledge chain.

Cross-coupled NAND gates are used to inhibit changes to the acknowledge routing while an acknowledge is in progress. For instance, if a B port interrupt is being acknowledged and AINT1 comes active while BRATNØ is active, BRATNØ continues to be active for the duration of the RACKØ signal, even though the A port has a higher interrupt priority than the B port. ARATNØ does not go active until the next RACKØ signal comes to the board.

3.9 Line Drivers and Receivers

The DPCA is designed to comply with EIA standards RS-232 and RS-423 (FED-STD-1030A). It also complies with MIL-STD-188-114 for unbalanced signals. The receivers are 88LS120 balanced receivers configured as inverters. All receivers have a common ground reference line which connects to pin 7 of the comm connector. This ground is also connected to logic ground on the DPCA via jumper X50 [p5zC1] for the A port (jumper X28 [p11zC1] for the B port). For RS-423 and MIL-STD-188-114 usage, this jumper should be removed so that pin 7 becomes receive common and is isolated from logic ground. For RS-232, this jumper should be installed.

Each receiver has a .001 mfd response control capacitor, for example, C61 [p5zB2]. This is used for suppression of high frequency noise on the input line. An offset voltage of approximately -6 volts is generated by the R52/R53 divider network. This offset voltage forces the inverting input to be above approximately 0.6 volts before the gate switches. This is to ensure that the receiver output is high if its inverting output is disconnected.

The drivers used on the DPCA are 9636As. These drivers are inverting and generate output signal levels of 5.5 volts or -5.5 volts. These levels allow compatibility with all the comm standards met by this board.

Pin 1 of the 9636As is used for a waveshaping resistor. A value of 120 Kohm is used, causing a rise and fall time in the output of approximately 15 microseconds. This allows compliance with MIL-STD-188-114 for baud rates up to 19.2 Kbaud. The signal rise and fall transitions are shaped as linear ramps. These slower rise and fall times cut down on cross talk generated within comm cabling connected to the DPCA.

In certain MIL-STD-188-114 applications, it is necessary to invert the sense of the transmit and receive data signals. This inversion is accomplished using 7486 XOR gates [p5zG4&F5]. When jumper X6 [p5zE6] (X5 [p11zE6] for the B port) is installed, ADINV1 is low and the XORs do not invert the data signals. X6 is usually installed.

Four V18ZA1 varistors are used on each port to protect the most commonly used signal lines: frame ground (pin 1), transmit data (pin 2), receive data (pin 3), and signal ground (pin 7), from high energy transients on the comm line.

Note: Sheet 12 of the DPCA schematics depicts RS-232 line receivers which are no longer used on the DPCA. These receivers are not compliant with RS-423 and MIL-STD-188-114. Also, the schematics indicate that 75150s may be substituted for the 9636As in RS-232 applications. To maintain compatibility with RS-423, 75150s are no longer used on DPCAs.

3.10 Baud Rate Clock

A standard crystal oscillator circuit is used on the DPCA. This circuit [p2zE5&F5] uses a 5.0688 MHz crystal only, since only the 2661C (formerly 2661-3) version of the EPCI is used on the board.

4 Configuration Specification

4.1 Overview

As stated in chapter 1, the DPCA is a flexible communication interface board. Much of its flexibility is due to the power of the 2661C Enhanced Programmable Communication Interface (EPCI) chip. The rest of its flexibility is due to the configuration options available on the board.

Hardware configuration of the DPCA is performed using DIP switches and jumper shunts.

4.2 Address Selection

The DPCA contains two independently addressable ports, designated A and B. Each port recognizes two 10-bit addresses. The nine high-order address bits are selectable and the low-order bit is either 0 or 1 to select the receive logic or the transmit logic when the port is operating in full duplex mode.

The two high-order address bits for both ports are selected by the jumper strip at coordinate 9G on the circuit board. Refer to Figure 4-1. This jumper strip has a column labeled "A" and one labeled "B". To select the proper address range for the ports, set the jumpers in the appropriate column as indicated in Table 4-1, below.

Address Range	Bit 6	Bit 7
0xxh	1-2	4-5
1xxh	1-2	5-6
2xxh	2-3	4-5
3xxh	2-3	5-6

Table 4-1. High Order Address Selection

The low order address selection for the A and B ports is accomplished using the jumper strips at board location 10C and 5C, respectively. (On some board versions, there are DIP switches at these locations.) There are only seven

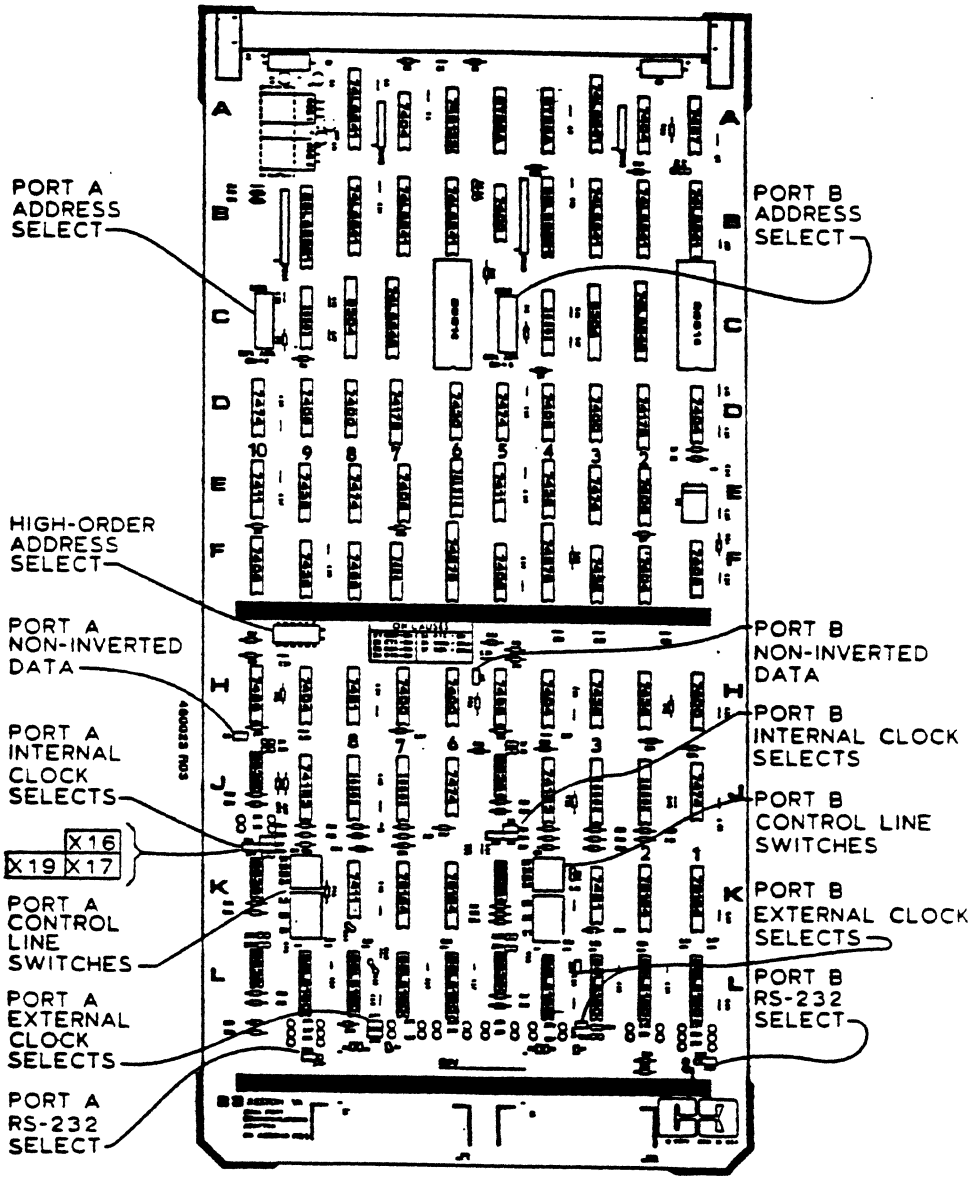


Figure 4-1. DPCA Configuration Option Locations

positions to be selected here since the least significant address bit is software selected.

The most significant bit (MSB) of these seven is indicated on the board. (Refer to Figure 4-1.) When a jumper is installed across a position (or a DIP switch position is "on" or "closed"), the corresponding address bit is 0.

For example, to select address xC4h (where x is set by the high-order address select jumpers):

	(MSB)							
Address Bit:	08	09	10	11	12	13	14	(15)
Selection:	-	-	X	X	X	-	X	
Binary:	1	1	0	0	0	1	0	(0) = C4h

where: - = off (open)
X = on (closed)

4.3 Control Line Switches

Certain of the communication line control signals may be forced active or inactive. Such forcing may be required in certain applications where control signals are not provided by the comm line cable.

Two packages of DIP switches are used for controlling these functions. These switches are at board location 9K for the A port and 4K for the B port. (Refer to Figure 4-1.) The switch positions are labeled "S1" through "S7". The function of these switches is shown in Table 4-2, below. In the table, "Enable" means the signal transitions normally, "On" means the signal is forced active, "Off" means the signal is forced inactive.

Pos	Signal	Pin	Dir	Off	On
S1	DCD	8	In	Enable	On
S2	CTS	5	In	Enable	On
S3	DSR	6	In	Enable	On
S4	DTR	20	Out	Enable	On
S5	RTS	4	Out	Enable	On
S6	Ring	22	In	Off	Enable
S7	RCR	16	In	Off	Enable

Table 4-2. Control Line Switch Settings

Note that the DCD signal must be active (or forced active) for the DPCA to receive data from the comm line. Similarly, the CTS signal must be active (or forced active) to transmit data to the comm line. These signals must be supplied for the hardware (the 2661C) to allow transfers in the appropriate direction. If not supplied by the comm line connector, the appropriate switch must be turned on for these transfers to occur.

4.4 Clock Selection Jumpers

The DPCA allows for selection of internal or external clocking of data. Clock signals are used during synchronous and isochronous data transfers for timing the transitions of the transmit and receive data lines. Clocks are unused in asynchronous operations.

The jumper positions used for clock selection and their functions are shown in Table 4-3, below. Table 4-4 illustrates standard configurations for these jumpers.

A Port	B Port	Function
X16	X11	Connect RxC Driver to pin 17
X17	X12	Connect TxC Driver to pin 15
X19	X13	Connect TxC Driver to pin 24
X44	X55	Connect TxC Receiver Output
X45	X54	Connect RxC Receiver Output

Table 4-3. Clock Selection Jumpers

	A: X16	X17	X19	X44	X45
Clock Selection	B: X11	X12	X13	X55	X54
Internal RxC	X				-
External RxC	-				X
Internal TxC		X		-	
External TxC		-		X	
TxC to pin 24			X		
No pin 24 connection			-		

where: - = jumper removed
X = jumper installed

Table 4-4. Clock Selection Configurations

When using asynchronous communications, the port may be configured for external or internal clocks, even though internal clocking is used. Care should be used, however, if external clocking is configured. The corresponding clock pins on the comm connector must be either disconnected, grounded, or at a negative voltage. They must not be at a high signalling level, which may in time result in damage to the 2661C EPCI. In asynchronous cabling, pins 15 and 17 usually are disconnected.

4.5 Communication Standard Selection

The DPCA is compliant with several communications standards, RS-232, RS-423 (FED-STD-1030A), and the unbalanced signalling requirements of MIL-STD-188-114. The operational differences between these standards are few on the DPCA.

For RS-232 communications, a common signalling ground is used for signals being transmitted and received by a device. For RS-423 and MIL-STD-188-114, a separate ground must be provided for signals being transmitted and those being received. These grounds are called "send common" and "receive common".

When using RS-423 and MIL-STD-188-114 signalling, jumper X50 for port A or jumper X28 for port B must be removed. (Refer to Figure 4-1 for these jumper locations.) These jumpers connect the send and receive commons. These jumpers should be installed for RS-232 operation.

There are no standard pin locations defined in RS-423 or MIL-STD-188-114 for the send and receive commons. On the DPCA, pin 1 is send common and pin 7 is receive common. When interconnecting two devices, send common on one device should be connected to receive common on the other.

In certain MIL-STD-188-114 communications systems transmit and receive data (pins 2 and 3) are inverted in sense from those used for RS-232 and RS-423. Jumper X6 for port A and X5 for port B allow for inversion of these two signals. When one of these jumpers is installed, data has customary sense for the corresponding channel. When removed, data is inverted.

The communication standard selection options are summarized in Table 4-5, below.

Function	A: X6 B: X5	X50 X28
RS-423 operation	X	-
MIL-STD-188-114, inverted data	-	-
MIL-STD-188-114, normal data	X	-
RS-232 operation	X	X

where: - = jumper removed
X = jumper installed

Table 4-5. Communication Standards Selection

5 External Interfaces

5.1 Overview

The Dual Port Communication Adapter (DPCA) has three external connections, one to the Perkin-Elmer MUX Bus (Connector Ø), and two 25-pin D-type communication line connectors.

This chapter presents the pinouts for these connectors.

5.2 Connector Ø

Connector Ø is an 84-pin connector which mates with the Perkin-Elmer Multiplexor (MUX) bus. It contains all of the data, handshake, and power connections required for operation on the channel Ø side of this bus. The connector used is AMP type 3-86018-4, or equivalent.

The following pins are used on Connector Ø:

Pin	Dir	Signal	Pin	Dir	Signal
1ØØ		+5 VDC	2ØØ		GND
1Ø1		GND	2Ø1		GND
114	I/O	DØ6Ø	214	I/O	DØ7Ø
115	I/O	DØ8Ø	215	I/O	DØ9Ø
116	I/O	D1ØØ	216	I/O	D11Ø
117	I/O	D12Ø	217	I/O	D13Ø
118	I/O	D14Ø	218	I/O	D15Ø
119	I	SRØ	219	I	ADRSØ
12Ø	I	DRØ	22Ø	I	CMDØ
121			221	I	DAØ
122	I	RACKØ	222	O	TACKØ
123	O	SYNØ	223	O	ATNØ
126	I	SCLRØ	226		
138		-15 VDC	238		
139		+15 VDC	239		
14Ø		GND	24Ø		GND
141		+5 VDC	241		GND

Table 5-1. Connector Ø Pinout

5.3 Connectors 1 and 2

Connectors 1 and 2 are 25-pin D-type male connectors used, respectively, for the port A and B communication channels. The connector pinouts are defined in accordance with EIA standard RS-232. The connectors used are AMP type 206604-1, or equivalent.

The following pins are used on both Connectors 1 (port A) and 2 (port B):

Pin	Dir	Signal	
1	-	RC	Recv Common, Sig Gnd
2	O	TxD	Transmit Data
3	I	RxD	Receive Data
4	O	RTS	Request to Send
5	I	CTS	Clear to Send
6	I	DSR	Data Set Ready
7	-	GND	Send Common, Sig Gnd
8	I	DCD	Data Carrier Detect
14	O	RCT	Reverse Channel Transmit
15	I/O	TxC	Transmit Clock
16	I	RCR	Reverse Channel Receive
17	I/O	RxC	Receive Clock
20	O	DTR	Data Terminal Ready
22	I	RI	Ring Indicator
24	O	TT	Transmit Timing (TxC)

Table 5-2. Connector 1 and 2 Pinout

6 Installation

6.1 Overview

This chapter provides the necessary information for the installation of one or two Dual Port Communications Adapters (DPCAs). The DPCA is contained on a 7 inch Perkin-Elmer format half-board. This half-board must be combined with another half-board device or a half-board blank to be properly installed in the 15 inch Perkin-Elmer I/O chassis. These must be joined using a Perkin-Elmer 16-398 Half Board Adapter Kit. Depending on configuration, the DPCA may be either the left or right half-board - or both.

6.2 Unpacking

The DPCA is normally installed at the factory and no special unpacking instructions are required. It is only necessary to ensure that the module is properly seated on the backplane connector.

If the DPCA is shipped separately, unpack it carefully and check for damage and loose integrated circuits before installation. Verify that the various jumper options are properly installed. (Refer to Chapter 4 for details.)

If the DPCA is replacing an existing board, ensure that the configuration strapping and switch settings match the unit being replaced.

6.3 Location

The DPCA may be installed in an I/O slot in a CPU chassis or I/O expansion chassis. This slot must be under direct control of the processor MUX bus or under a DIOS, subchannel controller, or C3 Manual Bus Switch.

6.4 Backplane Considerations

The RACKØ/TACKØ jumper must be removed from any slot containing a DPCA. (This jumper runs between pins 122 and 222 on the backplane connector for the board.)

The DPCA requires ±15 volt power. This power is available on 7/32 chassis on pins 138 (-15 volts) and 139 (+15 volts). If this power is not present on the chassis, an external power supply must be provided to furnish these voltages. The supply must be properly sized to meet the requirements of all the DPCAs which it is to power. (Refer to Chapter 1 for these power requirements.)

APPENDIX A

2661C EPCI Data Sheet

The following data sheet is reprinted by permission of Signetics Corporation, a subsidiary of U.S. Philips Corporation.

Signetics

SCN2661/SCN68661
Enhanced Programmable Communications Interface (EPCI)

Microprocessor Products

Product Specification

DESCRIPTION

The Signetics SCN2661 EPCI is a universal synchronous/asynchronous data communications controller chip that is an enhanced version of the SCN2651. It interfaces easily to all 8-bit and 16-bit microprocessors and may be used in a polled or interrupt driven system environment. The SCN2661 accepts programmed instructions from the microprocessor while supporting many serial data communications disciplines – synchronous and asynchronous – in the full or half-duplex mode. Special support for BISYNC is provided.

The EPCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The SCN2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode. Each version of the EPCI (A, B, C) has a different set of baud rates.

FEATURES

- Synchronous operation
  - 5- to 8-bit characters plus parity
  - Single or double SYN operation
  - Internal or external character synchronization
  - Transparent or non-transparent mode
  - Transparent mode DLE stuffing (Tx) and detection (Rx)
  - Automatic SYN or DLE-SYN insertion SYN, DLE and DLE-SYN stripping
  - Odd, even, or no parity
  - Local or remote maintenance loopback mode
  - Baud rate: dc to 1M bps (1X clock)
- Asynchronous operation
  - 5- to 8-bit characters plus parity
  - 1, 1½ or 2 stop bits transmitted
  - Odd, even, or no parity
  - Parity, overrun and framing error detection
  - Line break detection and generation
  - False start bit detection
  - Automatic serial echo mode (echoplex)
  - Local or remote maintenance loopback mode
  - Baud rate: dc to 1M bps (1X clock)
    dc to 62.5K bps (16X clock)
    dc to 15.625K bps (64X clock)

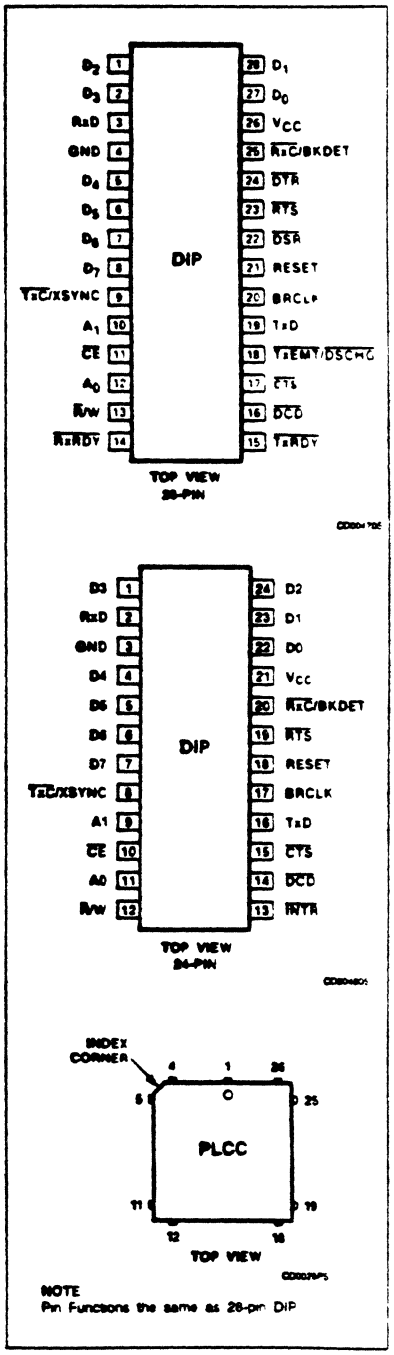
OTHER FEATURES

- Internal or external baud rate clock
- 3 baud rate sets
- 16 internal rates for each set
- Double buffered transmitter and receiver
- Dynamic character length switching
- Full or half-duplex operation
- TTL compatible inputs and outputs
- RxC and TxC pins are short circuit protected
- Single 5V power supply
- No system clock required

APPLICATIONS

- Intelligent terminals
- Network processors
- Front-end processors
- Remote data concentrators
- Computer-to-computer links
- Serial peripherals
- BISYNC adaptors

PIN CONFIGURATION



Enhanced Programmable Communications Interface (EPCI)

SCN2661/SCN68661

ORDERING CODE

PACKAGES	V_{CC} = 5V ± 5%		
	Commercial	Automotive	Military
	0°C to +70°C	-40°C to +85°C	-55°C to +125°C
Ceramic DIP 28-Pin 0.6" Wide	SCN2661AC1I28 SCN2661BC1I28 SCN2661CC1I28	SCN2661AA1I28 SCN2661BA1I28 SCN2661CA1I28	SCN2661AM1I28 SCN2661BM1I28 SCN2661CM1I28
Plastic DIP 28-Pin 0.6" Wide	SCN2661AC1N28 SCN2661BC1N28 SCN2661CC1N28	Contact Factory	Not Available
Plastic DIP 24-Pin 0.4" Wide	SCN2661AC1N24 SCN2661BC1N24 SCN2661CC1N24	Contact Factory	Not Available
Plastic LCC	SCN2661AC1A28 SCN2661BC1A28 SCN2661CC1A28	Contact Factory	Not Available

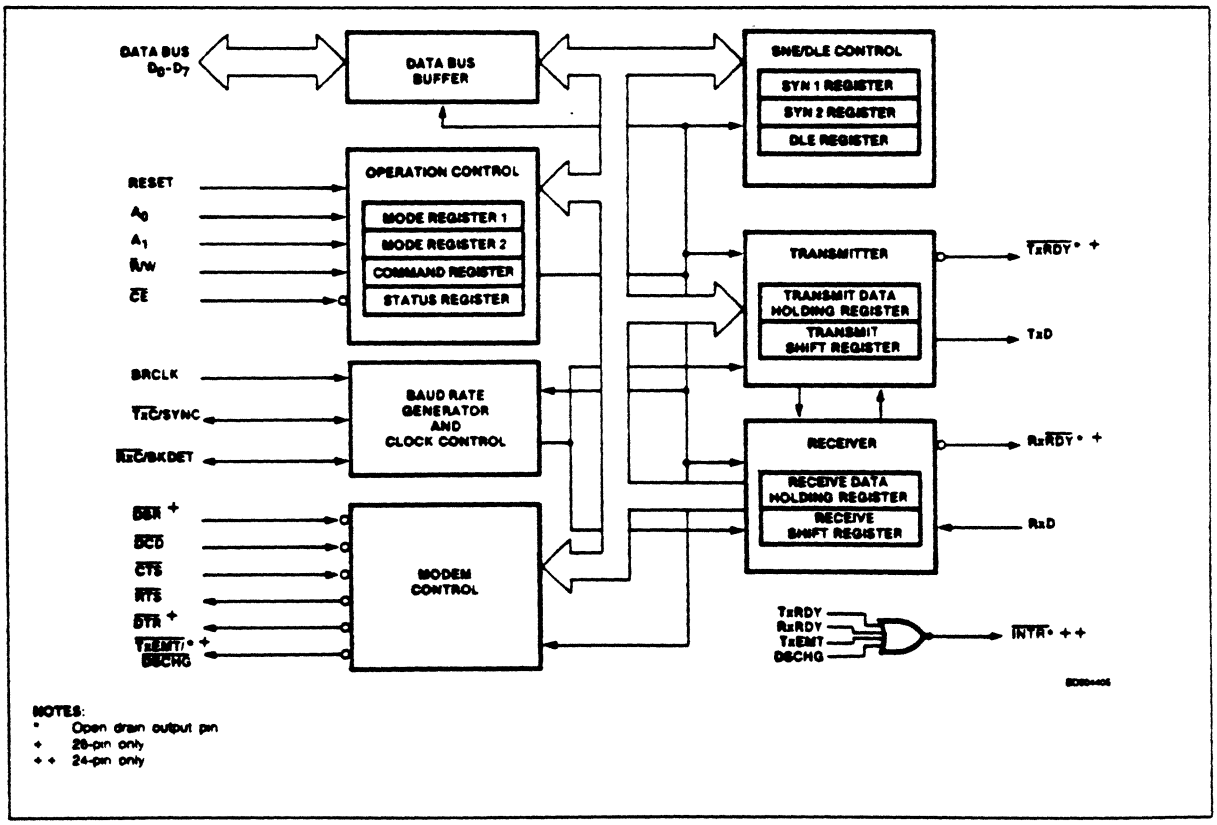
NOTES:
1. See table 1 for baud rates. Specify SCN2661A, B, or C depending on baud rate selected.
2. The SCN68661 is identical to the SCN2661. Order using part numbers above.

The EPCI is available in two packages a 28-pin (0.6" wide) DIP and a 24-pin (0.4" wide) DIP. The following are the differences between the 24-pin and the 28-pin versions.

1. The 24-pin version provides a single interrupt output ($\overline{INTR}$) instead of the three interrupt outputs ($\overline{RxRDY}$, $\overline{TxRDY}$, $\overline{TxEMT/DSCHG}$) supplied on the 28-pin version. $\overline{INTR}$ will be asserted (low) when one or more of the status bits SR0, SR1 or SR2 is a logic one.
2. Two modem interface pins, the $\overline{DTR}$ output and the $\overline{DSR}$ input, are eliminated in the 24-pin version. Because of this, status bit SR7 should be ignored and the setting of status bit SR2 due to a data set change (DSCHG) can be caused only by a change of the $\overline{DCD}$ input. Since the $\overline{DTR}$ output is eliminated, command register bit CR1 does not perform any function, although it remains writable and readable.

Other than the above, the functional operation, DC electrical characteristics, and AC electrical characteristics of the 24-pin version are identical to the 28-pin version.

BLOCK DIAGRAM



NOTES:
* Open drain output pin
\+ 28-pin only
\+ + 24-pin only

BLOCK DIAGRAM

The EPCI consists of six major sections These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control These sections communicate with each other via an internal data bus and an internal control bus The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains mode registers 1 and 2, the command register, and the status register Details of register addressing and protocol are presented in the EPCI programming section of this data sheet

Timing

The EPCI contains a baud rate generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications The unit can generate 16 commonly used baud rates, any one of which can be selected for full-duplex operation. See table 1.

Receiver

The receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled character to the CPU

Transmitter

The transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency

Table 1. BAUD RATE GENERATOR CHARACTERISTICS

SCN2661A (BRCLK = 4.9152MHz)

MR23 - 20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6144
0001	75	1.2	—	4096
0010	110	1.7598	-0.01	2793
0011	134.5	2.152	—	2284
0100	150	2.4	—	2048
0101	200	3.2	—	1536
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1050	16.8329	0.196	292
1001	1200	19.2	—	256
1010	1800	28.7438	-0.19	171
1011	2000	31.9168	-0.26	154
1100	2400	38.4	—	128
1101	4800	76.8	—	64
1110	9600	153.6	—	32
1111	19200	307.2	—	16

SCN2661B (BRCLK = 4.9152MHz)

MR23 - 20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	45.5	0.7279kHz	0.005	6752
0001	50	0.8	—	6144
0010	75	1.2	—	4096
0011	110	1.7598	-0.01	2793
0100	134 5	2.152	—	2284
0101	150	2.4	—	2048
0110	300	4.8	—	1024
0111	600	9.6	—	512
1000	1200	19.2	—	256
1001	1800	28.7438	-0 19	171
1010	2000	31.9168	-0.26	154
1011	2400	38.4	—	128
1100	4800	76.8	—	64
1101	9600	153.6	—	32
1110	19200	307.2	—	16
1111	38400	614.4	—	8

SCN2661C (BRCLK = 5.0688MHz)

MR23 - 20	BAUD RATE	ACTUAL FREQUENCY 16X CLOCK	PERCENT ERROR	DIVISOR
0000	50	0.8kHz	—	6336
0001	75	1.2	—	4224
0010	110	1.76	—	2880
0011	134.5	2.1523	0.016	2355
0100	150	2.4	—	2112
0101	300	4.8	—	1056
0110	600	9.6	—	528
0111	1200	19.2	—	264
1000	1800	28.8	—	176
1001	2000	32.081	0.253	158
1010	2400	38.4	—	132
1011	3600	57.6	—	88
1100	4800	76.8	—	66
1101	7200	115.2	—	44
1110	9600	153.6	—	33
1111	19200	316.8	3.125	16

NOTE:
16X clock is used in asynchronous mode In synchronous mode, clock multiplier is 1X and BRG can be used only for TxC

OPERATION

The functional operation of the SCN2661 is programmed by a set of control words supplied by the CPU. These control words specify items such as synchronous or asynchronous mode, baud rate, number of bits per character, etc. The programming procedure is described in the EPCI programming section of the data sheet.

After programming, the EPCI is ready to perform the desired communications functions. The receiver performs serial to parallel conversion of data received from a modem or equivalent device. The transmitter converts parallel data received from the CPU to a serial bit stream. These actions are accomplished within the framework specified by the control words

Receiver

The SCN2661 is conditioned to receive data when the $\overline{DCD}$ input is low and the RxEN bit in the command register is true. In the asynchronous mode, the receiver looks for a high-to-low (mark to space) transition of the start bit on the RxD input line. If a transition is detected, the state of the RxD line is sampled again after a delay of one-half of a bit time. If RxD is now high, the search for a valid start bit is begun again. If RxD is still low, a valid start bit is assumed and the receiver continues to sample the input line at one bit time intervals until the proper number of data bits, the parity bit, and one stop bit have been assembled. The data are then transferred to the receive data holding register, the RxRDY bit in the status register is set, and the $\overline{RxRDY}$ output is asserted. If the character length is less than 8 bits, the high order unused bits in the holding register are set to zero. The parity error, framing error, and overrun error status bits are strobed into the status register on the positive going edge of $\overline{RxC}$ corresponding to the received character boundary. If the stop bit is present, the receiver will immediately begin its search for the next start bit. If the stop bit is absent (framing error), the receiver will interpret a space as a start bit if it persists into the next bit time interval. If a break condition is detected (RxD is low for the entire character as well as the stop bit), only one character consisting of all zeros (with the FE status bit SR5 set) will be transferred to the holding register. The RxD input must return to a high condition before a search for the next start bit begins.

Pin 25 can be programmed to be a break detect output by appropriate setting of MR27-MR24. If so, a detected break will cause that pin to go high. When RxD returns to mark for one RxC time, pin 25 will go low. Refer to the break detection timing diagram.

Table 2. CPU-RELATED SIGNALS

PIN NAME	24-PIN	28-PIN	INPUT/OUTPUT	FUNCTION
RESET	X	X	I	A high on this input performs a master reset on the 2661. This signal asynchronously terminates any device activity and clears the mode, command and status registers. The device assumes the idle state and remains there until initialized with the appropriate control words
$A_1 - A_0$	X	X	I	Address lines used to select internal EPCI registers.
R/$\overline{W}$	X	X	I	Read command when low, write command when high.
$\overline{CE}$	X	X	I	Chip enable command. When low, indicates that control and data lines to the EPCI are valid and that the operation specified by the R/$\overline{W}$, A_1 and A_0 inputs should be performed. When high, places the $D_0 - D_7$ lines in the three-state condition.
$D_7 - D_0$	X	X	I/O	8-bit, three-state data bus used to transfer commands, data and status between EPCI and the CPU. D_0 is the least significant bit, D_7 the most significant bit.
$\overline{TxRDY}$		X	O	This output is the complement of status register bit SR0. When low, it indicates that the transmit data holding register (THR) is ready to accept a data character from the CPU. It goes high when the data character is loaded. This output is valid only when the transmitter is enabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{RxRDY}$		X	O	This output is the complement of status register bit SR1. When low, it indicates that the receive data holding register (RHR) has a character ready for input to the CPU. It goes high when the RHR is read by the CPU, and also when the receiver is disabled. It is an open drain output which can be used as an interrupt to the CPU.
$\overline{TxEMT}$/$\overline{DSCHG}$		X	O	This output is the complement of status register bit SR2. When low, it indicates that the transmitter has completed serialization of the last character loaded by the CPU, or that a change of state of the $\overline{DSR}$ or $\overline{DCD}$ inputs has occurred. This output goes high when the status register is read by the CPU, if the TxEMT condition does not exist. Otherwise, the THR must be loaded by the CPU for this line to go high. It is an open drain output which can be used as an interrupt to the CPU. See Status Register (SR2) for details.
$\overline{INTR}$	X		O	This is an active low output which is the wire-OR of the $\overline{TxRDY}$, $\overline{RxRDY}$, and $\overline{TxEMT}$/$\overline{DSCHG}$ outputs on the 28-pin version. See above.

When the EPCI is initialized into the synchronous mode, the receiver first enters the hunt mode on a 0 to 1 transition of RxEN(CR2). In this mode, as data are shifted into the receiver shift register a bit at a time, the contents of the register are compared to the contents of the SYN1 register. If the two are not equal, the next bit is shifted in and the comparison is

repeated When the two registers match, the hunt mode is terminated and character assembly mode begins If single SYN operation is programmed, the SYN DETECT status bit is set. If double SYN operation is programmed, the first character assembled after SYN1 must be SYN2 in order for the SYN DETECT bit to be set. Otherwise, the EPCI returns to the hunt mode. (Note that the sequence SYN1 – SYN1 – SYN2 will not achieve synchronization.) When synchronization has been achieved, the EPCI continues to assemble characters and transfer them to the holding register, setting the RxRDY status bit and asserting the $\overline{\text{RxRDY}}$ output each time a character is transferred The PE and OE status bits are set as appropriate Further receipt of the appropriate SYN sequence sets the SYN DETECT status bit If the SYN stripping mode is commanded, SYN characters are not transferred to the holding register. Note that the SYN characters used to establish initial synchronization are not transferred to the holding register in any case

External jam synchronization can be achieved via pin 9 by appropriate setting of MR27 – MR24. When pin 9 is an XSYNC input, the internal SYN1, SYN1 – SYN2, and DLE – SYN1 detection is disabled Each positive going signal on XSYNC will cause the receiver to establish synchronization on the rising edge of the next RxC pulse Character assembly will start with the RxD input at this edge. XSYNC may be lowered on the next rising edge of RxC. This external synchronization will cause the SYN DETECT status bit to be set until the status register is read Refer to XSYNC timing diagram.

Transmitter

The EPCI is conditioned to transmit data when the $\overline{\text{CTS}}$ input is low and the TxEN command register bit is set The SCN2661 indicates to the CPU that it can accept a character for transmission by setting the TxRDY status bit and asserting the $\overline{\text{TxRDY}}$ output. When the CPU writes a character into the transmit data holding register, these conditions are negated Data are transferred from the holding register to the transmit shift register when it is idle or has completed transmission of the previous character The TxRDY conditions are then asserted again. Thus, one full character time of buffering is provided

In the asynchronous mode, the transmitter automatically sends a start bit followed by the programmed number of data bits, the least significant bit being sent first It then appends an optional odd or even parity bit and the programmed number of stop bits. If, following transmission of the data bits, a new character is not available in the transmit holding register, the TxD output remains in the marking (high) condition and the $\overline{\text{TxEMT}}/\overline{\text{DSCHG}}$ output and its corresponding status bit are asserted Transmission resumes when the CPU loads a new character into the holding register. The transmitter can be forced to output a continuous low (BREAK) condition by setting the send break command bit (CR3) high.

In the synchronous mode, when the SCN2661 is initially conditioned to transmit, the TxD output remains high and the TxRDY condition is asserted until the first character to be transmitted (usually a SYN character) is loaded by the CPU. Subsequent to this, a continuous stream of characters is transmitted No extra bits (other than parity, if commanded) are generated by the EPCI

Table 3. DEVICE RELATED SIGNALS

PIN NAME	24-PIN	28-PIN	INPUT/OUTPUT	FUNCTION
BRCLK	X	X	I	Clock input to the internal baud rate generator (see table 1). Not required if external receiver and transmitter clocks are used.
$\overline{\text{RxC}}$/BKDET	X	X	I/O	Receiver clock. If external receiver clock is programmed, this input controls the rate at which the character is to be received Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. Data are sampled on the rising edge of the clock. If internal receiver clock is programmed, this pin can be a 1X/16X clock or a break detect output pin.
$\overline{\text{TxC}}$/XSYNC	X	X	I/O	Transmitter clock. If external transmitter clock is programmed, this input controls the rate at which the character is transmitted Its frequency is 1X, 16X or 64X the baud rate, as programmed by mode register 1. The transmitted data changes on the falling edge of the clock. If internal transmitter clock is programmed, this pin can be a 1X/16X clock output or an external jam synchronization input
RxD	X	X	I	Serial data input to the receiver. "Mark" is high, "space" is low.
TxD	X	X	O	Serial data output from the transmitter "Mark" is high, "space" is low. Held in mark condition when the transmitter is disabled
$\overline{\text{DSR}}$		X	I	General purpose input which can be used for data set ready or ring indicator condition Its complement appears as status register bit SR7. Causes a low output on $\overline{\text{TxEMT}}/\overline{\text{DSCHG}}$ when its state changes if CR2 or CR0 = 1.
$\overline{\text{DCD}}$	X	X	I	Data carrier detect input. Must be low in order for the receiver to operate. Its complement appears as status register bit SR6. Causes a low output on $\overline{\text{TxEMT}}/\overline{\text{DSCHG}}$ when its state changes if CR2 or CR0 = 1. If $\overline{\text{DCD}}$ goes high while receiving, the RxC is internally inhibited
$\overline{\text{CTS}}$	X	X	I	Clear to send input. Must be low in order for the transmitter to operate If it goes high during transmission, the character in the transmit shift register will be transmitted before termination
$\overline{\text{DTR}}$		X	O	General purpose output which is the complement of command register bit CR1. Normally used to indicate data terminal ready
$\overline{\text{RTS}}$	X	X	O	General purpose output which is the complement of command register bit CR5 Normally used to indicate request to send. See Command Register (CR5) for details

Table 4. SCN2661 REGISTER ADDRESSING

$\overline{CE}$	A_1	A_0	$\overline{R}/W$	FUNCTION
1	X	X	X	Three-state data bus
0	0	0	0	Read receive holding register
0	0	0	1	Write transmit holding register
0	0	1	0	Read status register
0	0	1	1	Write SYN1/SYN2/DLE registers
0	1	0	0	Read mode register ½
0	1	0	1	Write mode register ½
0	1	1	0	Read command register
0	1	1	1	Write command register

NOTE:
See AC characteristics section for timing requirements

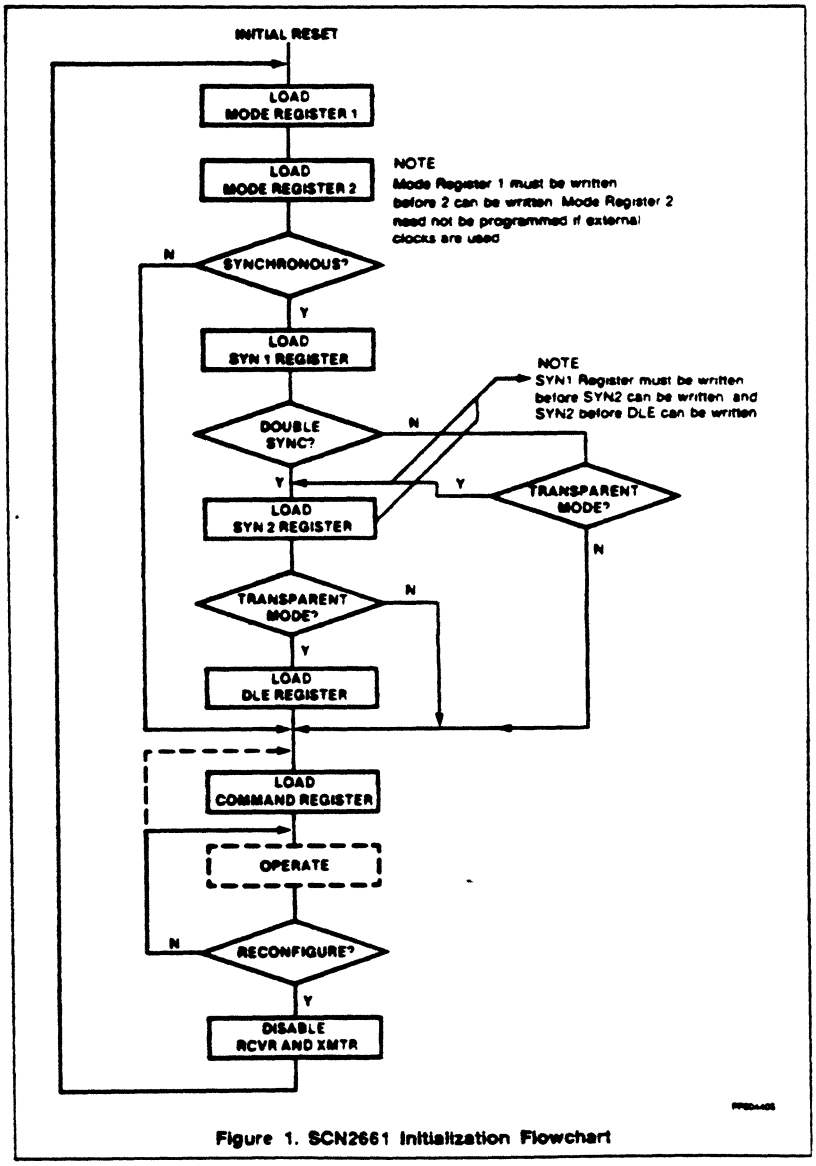


Figure 1. SCN2661 Initialization Flowchart

unless the CPU fails to send a new character to the EPCI by the time the transmitter has completed sending the previous character. Since synchronous communication does not allow gaps between characters, the EPCI asserts TxEMT and automatically "fills" the gap by transmitting SYN1s, SYN1 – SYN2 doublets, or DLE – SYN1 doublets, depending on the state of MR16 and MR17. Normal transmission of the message resumes when a new character is available in the transmit data holding register. If the send DLE bit in the command register is true, the DLE character is automatically transmitted prior to transmission of the message character in the THR.

EPCI PROGRAMMING

Prior to initiating data communications, the SCN2661 operational mode must be programmed by performing write operations to the mode and command registers. In addition, if synchronous operation is programmed, the appropriate SYN/DLE registers must be loaded. The EPCI can be reconfigured at any time during program execution. A flowchart of the initialization process appears in figure 1.

The internal registers of the EPCI are accessed by applying specific signals to the $\overline{CE}$, $\overline{R}/W$, A_1 and A_0 inputs. The conditions necessary to address each register are shown in table 4.

The SYN1, SYN2, and DLE registers are accessed by performing write operations with the conditions $A_1 = 0$, $A_0 = 1$, and $\overline{R}/W = 1$. The first operation loads the SYN1 register. The next loads the SYN2 register, and the third loads the DLE register. Reading or loading the mode registers is done in a similar manner. The first write (or read) operation addresses mode register 1, and a subsequent operation addresses mode register 2. If more than the required number of accesses are made, the internal sequencer recycles to point at the first register. The pointers are reset to SYN1 register and mode register 1 by a RESET input or by performing a read command register operation, but are unaffected by any other read or write operation.

The SCN2661 register formats are summarized in tables 5, 6, 7 and 8. Mode registers 1 and 2 define the general operational characteristics of the EPCI, while the command register controls the operation within this basic framework. The EPCI indicates its status in the status register. These registers are cleared when a RESET input is applied.

Mode Register 1 (MR1)

Table 5 illustrates mode register 1. Bits MR11 and MR10 select the communication format and baud rate multiplier. 00 specifies syn-

Table 5. MODE REGISTER 1 (MR1)

MR17	MR16	MR15	MR14	MR13	MR12	MR11	MR10
Sync/Async		Parity Type	Parity Control	Character Length		Mode and Baud Rate Factor	
Async: Stop bit length 00 = Invalid 01 = 1 stop bit 10 = 1½ stop bits 11 = 2 stop bits		0 = Odd 1 = Even	0 = Disabled 1 = Enabled	00 = 5 bits 01 = 6 bits 10 = 7 bits 11 = 8 bits		00 = Synchronous 1X rate 01 = Asynchronous 1X rate 10 = Asynchronous 16X rate 11 = Asynchronous 64X rate	
Sync: Number of SYN char 0 = Double SYN 1 = Single SYN	Sync: Transparency control 0 = Normal 1 = Transparent						

NOTE:
Baud rate factor in asynchronous applies only if external clock is selected. Factor is 16X if internal clock is selected. Mode must be selected (MR11, MR10) in any case.

Table 6. MODE REGISTER 2 (MR2)

MR27 - MR24										MR23 - MR20
	TxC	RxC	Pin 9	Pin 25		TxC	RxC	Pin 9	Pin 25	Mode	Baud Rate Selection
0000	E	E	TxC	RxC	1000	E	E	XSYNC[1]	RxC/TxC	sync	See baud rates in table 1
0001	E	I	TxC	1X	1001	E	I	TxC	BKDET	async	
0010	I	E	1X	RxC	1010	I	E	XSYNC[1]	RxC	sync	
0011	I	I	1X	1X	1011	I	I	1X	BKDET	async	
0100	E	E	TxC	RxC	1100	E	E	XSYNC[1]	RxC/TxC	sync	
0101	E	I	TxC	16X	1101	E	I	TxC	BKDET	async	
0110	I	E	16X	RxC	1110	I	E	XSYNC[1]	RxC	sync	
0111	I	I	16X	16X	1111	I	I	16X	BKDET	async	

NOTES:
1. When pin 9 is programmed as XSYNC input, SYN1, SYN1-SYN2, and DLE-SYN1 detection is disabled.
E = External clock
I = Internal clock (BRG)
1X and 16X are clock outputs

chronous mode and 1X multiplier. 1X, 16X, and 64X multipliers are programmable for asynchronous format. However, the multiplier in asynchronous format applies only if the external clock input option is selected by MR24 or MR25.

MR13 and MR12 select a character length of 5, 6, 7 or 8 bits. The character length does not include the parity bit, if programmed, and does not include the start and stop bits in asynchronous mode.

MR14 controls parity generation. If enabled, a parity bit is added to the transmitted character and the receiver performs a parity check on incoming data. MR15 selects odd or even parity when parity is enabled by MR14.

In asynchronous mode, MR17 and MR16 select character framing of 1, 1.5, or 2 stop bits. (If 1X baud rate is programmed, 1.5 stop bits defaults to 1 stop bits on transmit.) In synchronous mode, MR17 controls the number of SYN characters used to establish synchronization and for character fill when the transmitter is idle. SYN1 alone is used if MR17 = 1, and SYN1 - SYN2 is used when MR17 = 0. If the transparent mode is specified by MR16, DLE - SYN1 is used for character fill and SYN detect, but the normal synchronization sequence is used to establish character sync. When transmitting, a DLE character in the transmit holding register will cause a second DLE character to be transmitted. This DLE stuffing eliminates the software DLE compare and stuff on each transparent mode data character. If the send DLE command (CR3) is active when a DLE is loaded into THR, only one additional DLE will be transmitted. Also, DLE stripping and DLE detect (with MR14 = 0) are enabled.

The bits in the mode register affecting character assembly and disassembly (MR12 - MR16) can be changed dynamically (during active receive/transmit operation). The character mode register affects both the transmitter and receiver, therefore in synchronous mode, changes should be made only in half-duplex mode (RxEN = 1 or TxEN = 1, but not both simultaneously = 1). In asynchronous mode, character changes should be made when RxEN and TxEN = 0 or when TxEN = 1 and the transmitter is marking in half-duplex mode (RxEN = 0).

To effect assembly/disassembly of the next received/transmitted character, MR12 - 15 must be changed within n bit times of the active going state of $\overline{\text{RxRDY}}$/$\overline{\text{TxRDY}}$. Transparent and non-transparent mode changes (MR16) must occur within n - 1 bit times of the character to be affected when the receiver or transmitter is active (n = smaller of the new and old character lengths.)

Table 7. COMMAND REGISTER (CR)

CR7 CR6	CR5	CR4	CR3	CR2	CR1	CR0
Operating Mode	**Request To Send**	**Reset Error**	**Sync/ Async**	**Receive Control (RxEN)**	**Data Terminal Ready**	**Transmit Control (TxEN)**
00 = Normal operation 01 = Async: Automatic echo mode Sync: SYN and/or DLE stripping mode 10 = Local loopback 11 = Remote loopback	0 = Force $\overline{RTS}$ output high one clock time after TxSR serialization 1 = Force $\overline{RTS}$ output low	0 = Normal 1 = Reset error flags in status register (FE, OE, PE/DLE detect.)	**Async:** **Force break** 0 = Normal 1 = Force break **Sync** **Send DLE** 0 = Normal 1 = SendDLE	0 = Disable 1 = Enable Not applicable in	0 = Force $\overline{DTR}$ output high 1 = Force $\overline{DTR}$ output low 24-pin version.)	0 = Disable 1 = Enable

Table 8. STATUS REGISTER (SR)

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
Data Set Ready	**Data Carrier Detect**	**FE/SYN Detect**	**Overrun**	**PE/DLE Detect**	**TxEMT DSCHG**	**RxRDY**	**TxRDY**
0 = $\overline{DSR}$ input is high 1 = $\overline{DSR}$ input is low (Should be ignored in 24-pin version)	0 = $\overline{DCD}$ input is high 1 = $\overline{DCD}$ input is low	**Async:** 0 = Normal 1 = Framing error **Sync:** 0 = Normal 1 = SYN detected	0 = Normal 1 = Overrun error **Sync:**	**Async:** 0 = Normal 1 = Parity error 0 = Normal 1 = Parity error or DLE received	0 = Normal 1 = Change in $\overline{DSR}$ (28-pin version only), or $\overline{DCD}$, or transmit shift register is empty	0 = Receive holding register empty 1 = Receive holding register has data	0 = Transmit holding register busy 1 = Transmit holding register empty

Mode Register 2 (MR2)

Table 6 illustrates mode register 2. MR23, MR22, MR21 and MR20 control the frequency of the internal baud rate generator (BRG). Sixteen rates are selectable for each EPCI version (-1, -2, -3). Versions 1 and 2 specify a 4.9152MHz TTL input at BRCLK (pin 20); version 3 specifies a 5.0688MHz input which is identical to the Signetics 2651 MR23 - 20 are don't cares if external clocks are selected (MR25 - MR24 = 0). The individual rates are given in table 1.

MR24 - MR27 select the receive and transmit clock source (either the BRG or an external input) and the function at pins 9 and 25. Refer to table 6.

Command Register (CR)

Table 7 illustrates the command register. Bits CR0 (TxEN) and CR2 (RxEN) enable or disable the transmitter and receiver respectively. A 0 to 1 transition of CR2 forces start bit search (async mode) or hunt mode (sync mode) on the second $\overline{RxC}$ rising edge. Disabling the receiver causes $\overline{RxRDY}$ to go high (inactive) if the transmitter is disabled, it will complete the transmission of the character in the transmit shift register (if any) prior to terminating operation. The TxD output will then remain in the marking state (high) while $\overline{TxRDY}$ and $\overline{TxEMT}$ will go high (inactive). If the receiver is disabled, it will terminate operation immediately. Any character being assembled will be neglected. A 0 to 1 transition of CR2 will initiate start bit search (async) or hunt mode (sync).

Bits CR1 (28-pin only) (DTR) and CR5 (RTS) control the $\overline{DTR}$ and $\overline{RTS}$ outputs. Data at the outputs are the logical complement of the register data.

In asynchronous mode, setting CR3 will force and hold the TxD output low (spacing condition) at the end of the current transmitted character. Normal operation resumes when CR3 is cleared. The TxD line will go high for at least one bit time before beginning transmission of the next character in the transmit data holding register. In synchronous mode, setting CR3 causes the transmission of the DLE register contents prior to sending the character in the transmit data holding register. Since this is a one time command, CR3 does not have to be reset by software. CR3 should be set when entering and exiting transparent mode and for all DLE - non-DLE character sequences.

Setting CR4 causes the error flags in the status register (SR3, SR4, and SR5) to be cleared. This is a one time command. There is no internal latch for this bit.

When CR5 (RTS) is set, the $\overline{RTS}$ pin is forced low. A 1 to 0 transition of CR5 will cause $\overline{RTS}$ to go high (inactive) one TxC time after the last serial bit has been transmitted. If a 1-to-0 transition of CR5 occurs while data is being transmitted, $\overline{RTS}$ will remain low (active) until both the THR and the transmit shift register are empty and then go high (inactive) one TxC time later.

The EPCI can operate in one of four submodes within each major mode (synchronous or asynchronous). The operational sub-mode is determined by CR7 and CR6. CR7 - CR6 = 00 is the normal mode, with the transmitter and receiver operating independently in accordance with the mode and status register instructions.

In asynchronous mode, CR7 - CR6 = 01 places the EPCI in the automatic echo mode. Clocked, regenerated received data are automatically directed to the TxD line while normal receiver operation continues. The receiver must be enabled (CR2 = 1), but the transmitter need not be enabled. CPU to receiver

Table 9. SCN2661 EPCI vs SCN2651 PCI

FEATURE	EPCI	PCI
1. MR2 Bit 6, 7	Control pin 9, 25	Not used
2. DLE detect - SR3	SR3 = 0 for DLE - DLE, DLE - SYN1	SR3 = 1 for DLE - DLE, DLE - SYN1
3. Reset of SR3, DLE detect	Second character after DLE, or receiver disable, or CR4 = 1	Receiver disable, or CR4 = 1
4. Send DLE - CR3	One time command	Reset via CR3 on next $\overline{TxRDY}$
5. DLE stuffing in transparent mode	Automatic DLE stuffing when DLE is loaded except if CR3 = 1	None
6. SYN1 stripping in double sync non-transparent mode	All SYN1	First SYN1 of pair
7. Baud rate versions	Three	One
8. Terminate ASYNC transmission (drop RTS)	Reset CR5 in response to $\overline{TxEMT}$ changing from 1 to 0	Reset CR0 when $\overline{TxEMT}$ goes from 1 to 0 Then reset CR5 when $\overline{TxEMT}$ goes from 1 to 0
9. Break detect	Pin 25[1]	FE and null character
10. Stop bit searched	One	Two
11. External jam sync	Pin 9[2]	No
12. Data bus timing	Improved over 2651	—
13. Data bus drivers	Sink 2.2mA Source 400μA	Sink 1.6mA Source 100μA

NOTES:
1. Internal BRG used for RxC
2. Internal BRG used for TxC

communications continues normally, but the CPU to transmitter link is disabled. Only the first character of a break condition is echoed. The TxD output will go high until the next valid start is detected. The following conditions are true while in automatic echo mode.

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. $\overline{TxRDY}$ output = 1.
4. The $\overline{TxEMT/DSCHG}$ pin will reflect only the data set change condition.
5. The TxEN command (CR0) is ignored.

In synchronous mode, CR7 - CR6 = 01 places the EPCI in the automatic SYN/DLE stripping mode. The exact action taken depends on the setting of bits MR17 and MR16.

1. In the non-transparent, single SYN mode (MR17 - MR16 = 10), characters in the data stream matching SYN1 are not transferred to the receive data holding register (RHR).
2. In the non-transparent, double SYN mode (MR17 - MR16 = 00), characters in the data stream matching SYN1, or SYN2 if immediately preceded by SYN1, are not transferred to the RHR.
3. In transparent mode (MR16 = 1), characters in the data stream matching DLE, or SYN1 if immediately preceded by DLE, are not transferred to the RHR. However, only the first DLE of a DLE-DLE pair is stripped.

Note that automatic stripping mode does not affect the setting of the DLE detect and SYN detect status bits (SR3 and SR5).

Two diagnostic sub-modes can also be configured. In local loopback mode (CR7 - CR6 = 10), the following loops are connected internally:

1. The transmitter output is connected to the receiver input.
2. $\overline{DTR}$ is connected to $\overline{DCD}$ and $\overline{RTS}$ is connected to $\overline{CTS}$.
3. The receiver is clocked by the transmit clock.
4. The $\overline{DTR}$, $\overline{RTS}$ and $\overline{TxD}$ outputs are held high.
5. The $\overline{CTS}$, $\overline{DCD}$, $\overline{DSR}$ and RxD inputs are ignored.

Additional requirements to operate in the local loopback mode are that CR0 (TxEN), CR1 (DTR), and CR5 (RTS) must be set to 1. CR2 (RxEN) is ignored by the EPCI.

The second diagnostic mode is the remote loopback mode (CR7 - CR6 = 11). In this mode:

1. Data assembled by the receiver are automatically placed in the transmit holding register and retransmitted by the transmitter on the TxD output.
2. The transmitter is clocked by the receive clock.
3. No data are sent to the local CPU, but the error status conditions (PE, FE) are set.
4. The $\overline{RxRDY}$, $\overline{TxRDY}$, and $\overline{TxEMT/DSCHG}$ outputs are held high.
5. CR0 (TxEN) is ignored.
6. All other signals operate normally.

Status Register

The data contained in the status register (as shown in table 8) indicate receiver and transmitter conditions and modem/data set status.

SR0 is the transmitter ready (TxRDY) status bit. It, and its corresponding output, are valid only when the transmitter is enabled. If equal to 0, it indicates that the transmit data holding register has been loaded by the CPU and the data has not been transferred to the transmit shift register. If set equal to 1, it indicates that the holding register is ready to accept data from the CPU. This bit is initially set when the transmitter is enabled by CR0, unless a character has previously been loaded into the holding register. It is not set when the automatic echo or remote loopback modes are programmed. When this bit is set, the $\overline{TxRDY}$ output pin is low. In the automatic echo and remote loopback modes, the output is held high.

SR1, the receiver ready (RxRDY) status bit, indicates the condition of the receive data holding register. If set, it indicates that a character has been loaded into the holding register from the receive shift register and is ready to be read by the CPU. If equal to zero, there is no new character in the holding register. This bit is cleared when the CPU reads the receive data holding register or when the receiver is disabled by CR2. When set, the $\overline{RxRDY}$ output is low.

The TxEMT/DSCHG bit, SR2, when set, indicates either a change of state of the $\overline{DSR}$ (28-pin only) or $\overline{DCD}$ inputs (when CR2 or CR0 = 1) or that the transmit shift register has completed transmission of a character and no new character has been loaded into the transmit data holding register. Note that in synchronous mode this bit will be set even though the appropriate "fill" character is transmitted. TxEMT will not go active until at least one character has been transmitted. It is cleared by loading the transmit data holding register. The DSCHG condition is enabled when TxEN = 1 or RxEN = 1. It is cleared when the status register is read by the CPU. If the status register is read twice and SR2 = 1

while SR6 and SR7 remain unchanged, then a TxEMT condition exists. When SR2 is set, the $\overline{\text{TxEMT}}/\overline{\text{DSCHG}}$ output is low.

SR3, when set, indicates a received parity error when parity is enabled by MR14. In synchronous transparent mode (MR16 = 1), with parity disabled, it indicates that a character matching DLE register was received and the present character is neither SYN1 nor DLE. This bit is cleared when the next character following the above sequence is loaded into RHR, when the receiver is disabled, or by a reset error command, CR4.

The overrun error status bit, SR4, indicates that the previous character loaded into the receive holding register was not read by the CPU at the time a new received character was transferred into it. This bit is cleared when the receiver is disabled or by the reset error command, CR4.

In asynchronous mode, bit SR5 signifies that the received character was not framed by a stop bit; i.e., only the first stop bit is checked. If RHR = 0 when SR5 = 1, a break condition is present. In synchronous nontransparent mode (MR16 = 0), it indicates receipt of the SYN1 character in single SYN mode or the SYN1 - SYN2 pair in double SYN mode. In synchronous transparent mode (MR16 = 1), this bit is set upon detection of the initial synchronizing characters (SYN1 or SYN1 - SYN2) and, after synchronization has been achieved, when a DLE - SYN1 pair is received. The bit is reset when the receiver is disabled, when the reset error command is given in asynchronous mode, or when the status register is read by the CPU in the synchronous mode.

SR6 and SR7 (28-pin only) reflect the conditions of the $\overline{\text{DCD}}$ and $\overline{\text{DSR}}$ inputs respectively. A low input sets its corresponding status bit, and a high input clears it.

ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	Note 4	°C
Storage temperature	−65 to +150	°C
All voltages with respect to ground[3]	−0.5 to +6.0	V

DC ELECTRICAL CHARACTERISTICS[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Input voltage						V
V_{IL}	Low				0.8	
V_{IH}	High		2.0			
Output voltage						V
V_{OL}	Low	I_{OL} = 2.2mA			0.4	
V_{OH}[7]	High	I_{OH} = −400μA	2.4			
I_{IL}	Input leakage current	V_{IN} = 0 to 5.5V			10	μA
3-state output leakage current						μA
I_{LH}	Data bus high	V_O = 4.0V			10	
I_{LL}	Data bus low	V_O = 0.45V			10	
I_{CC}	Power supply current				150	mA

CAPACITANCE T_A = 25°C, V_{CC} = 0V

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Capacitance						pF
C_{IN}	Input				20	
C_{OUT}	Output	fc = 1MHz			20	
$C_{I/O}$	Input/Output	Unmeasured pins tied to ground			20	

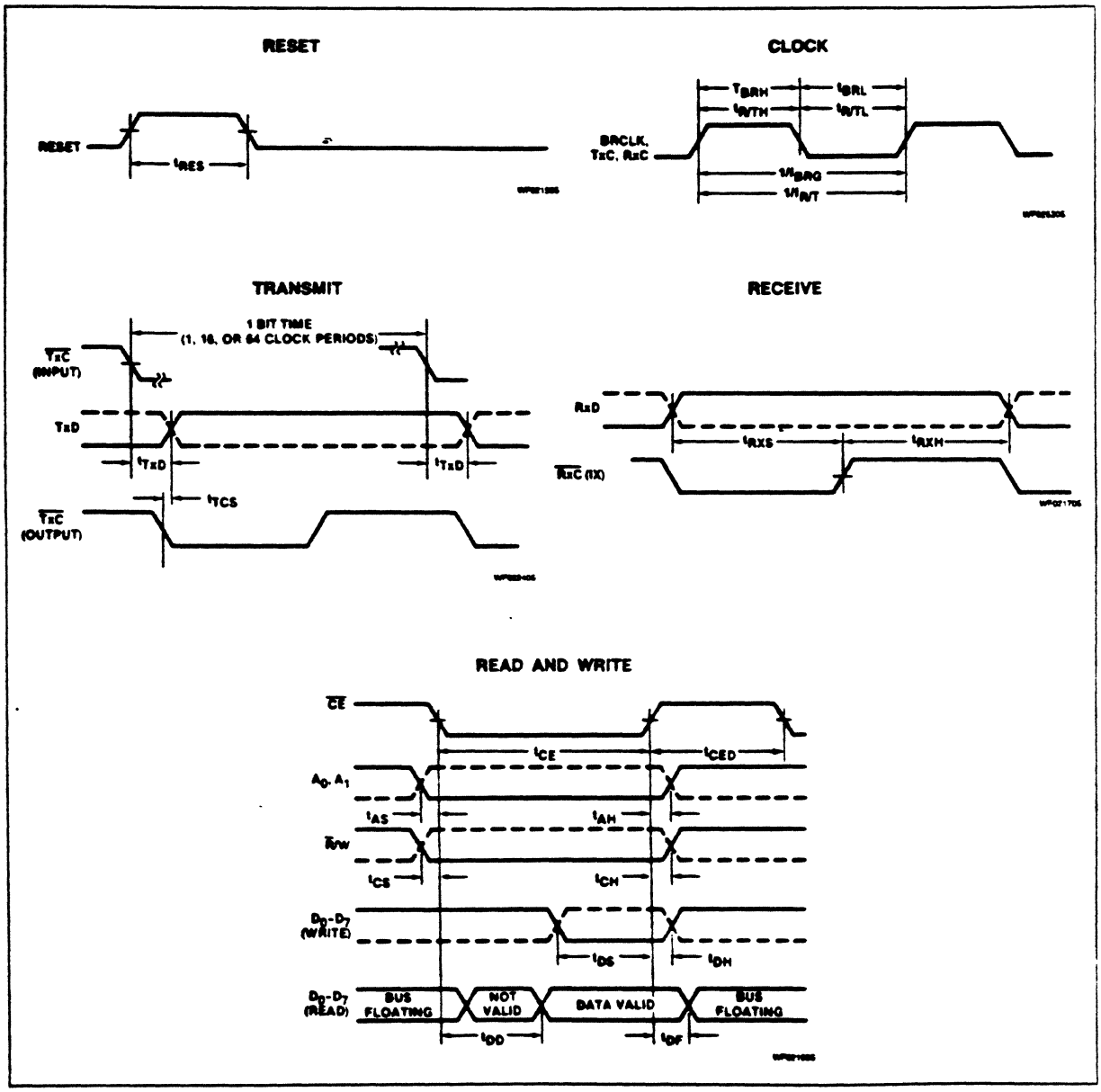
AC ELECTRICAL CHARACTERISTICS[4,5,6]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
Pulse width						ns
t_{RES}	Reset		1000			
t_{CE}	Chip enable		250			
Set-up and hold time						ns
t_{AS}	Address set-up		10			
t_{AH}	Address hold		10			
t_{CS}	R/W control set-up		10			
t_{CH}	R/W control hold		10			
t_{DS}	Data set-up for write		150			
t_{DH}	Data hold for write		10			
t_{RXS}	RX data set-up		300			
t_{RXH}	RX data hold		350			
t_{DD}	Data delay time for read	C_L = 150pF			200	ns
t_{DF}	Data bus floating time for read	C_L = 150pF			100	
t_{CED}	CE to CE delay		600			
Input clock frequency						MHz
f_{BRG}	Baud rate generator (2661A,B)		1.0	4.9152	4.9202	
f_{BRG}	Baud rate generator (2661C)		1.0	5.0688	5.0738	
$f_{R/T}$[10]	$\overline{TxC}$ or $\overline{RxC}$		dc		1.0	
Clock width						ns
t_{BRH}[9]	Baud rate high (2661A,B)		75			
t_{BRH}[9]	Baud rate high (2661C)		70			
t_{BRL}[9]	Baud rate low (2661A,B)		75			
t_{BRL}[9]	Baud rate low (2661C)		70			
$t_{R/TH}$	$\overline{TxC}$ or $\overline{RxC}$ high		480			
$t_{R/TL}$[10]	$\overline{TxC}$ or $\overline{RxC}$ low		480			
t_{TXD}	TxD delay from falling edge of $\overline{TxC}$	C_L = 150pF			650	ns
t_{TCS}	Skew between TxD changing and falling edge of $\overline{TxC}$ output[8]	C_L = 150pF		0		

NOTES:

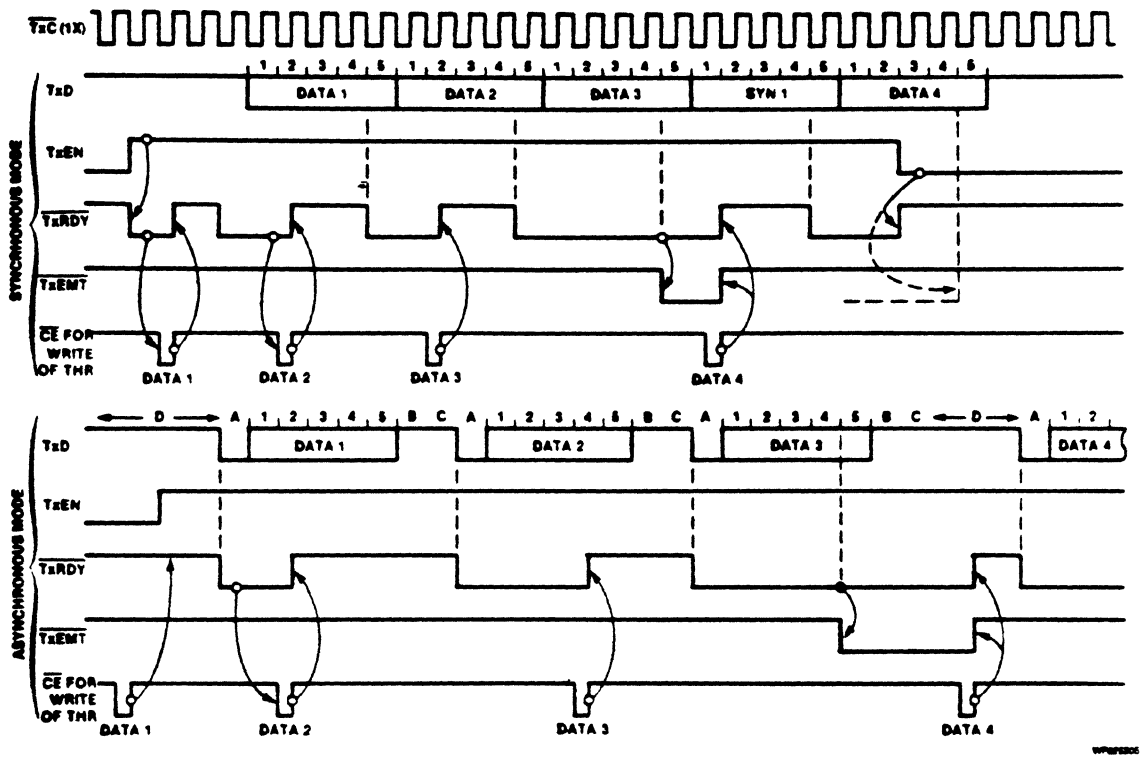
1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on + 150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over operating temperature range unless otherwise specified. See ordering code table for applicable temperature range and operating supply range.
5. All voltage measurements are referenced to ground. All time measurements are at the 50% level for inputs (except t_{BRH} and t_{BRL}) and at 0.8V and 2.0V for outputs. Input levels swing between 0.4V and 2.4V, with a transition time of 20ns maximum.
6. Typical values are at + 20°C, typical supply voltages and typical processing parameters.
7. $\overline{INTR}$, $\overline{TxRDY}$, $\overline{RxRDY}$ and $\overline{TxEMT/DSCHG}$ outputs are open drain.
8. Parameter applies when internal transmitter clock is used.
9. Under test conditions of 5.0688MHz f_{BRG} (2661C) and 4.9152MHz f_{BRG} (2661A,B), t_{BRH} and t_{BRL} measured at V_{IH} and V_{IL} respectively.
10. In asynchronous local loopback mode, using 1X clock the following parameters apply: $f_{R/T}$ = 0.83MHz max and $t_{R/TL}$ = 700ns min.

TIMING DIAGRAMS



TIMING DIAGRAMS (Continued)

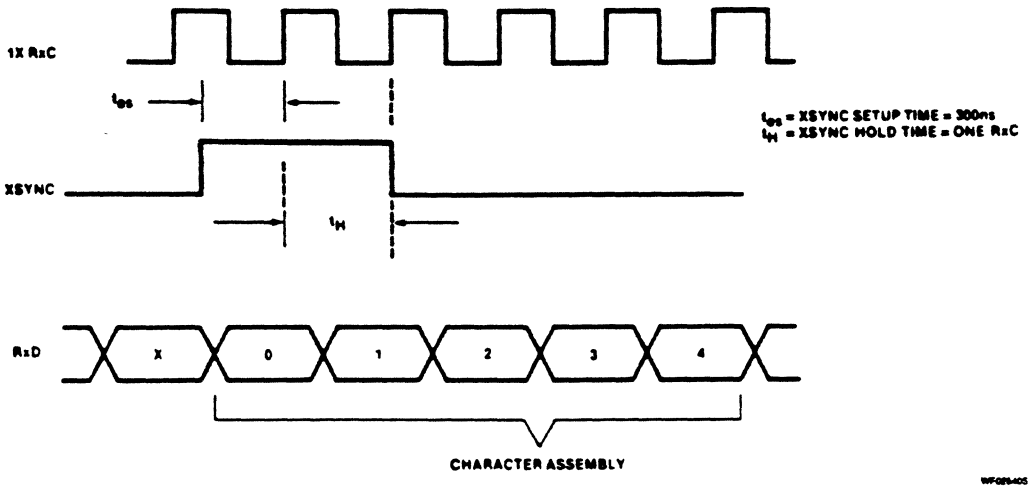
TxRDY, TxEMT (Shown for 5-bit characters, no parity, 2 stop bits [in asynchronous mode])



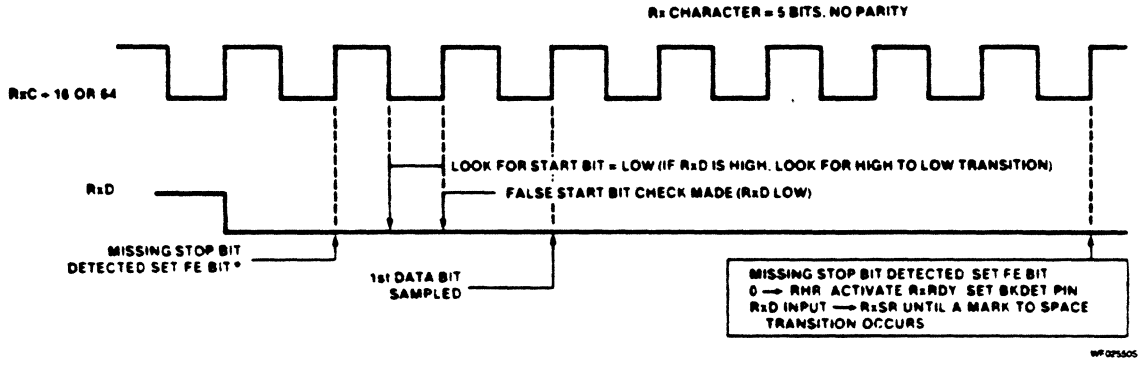
NOTES:
A = Start bit
B = Stop bit 1
C = Stop bit 2
D = TxD marking condition
TxEMT goes low at the beginning of the last data bit, or if parity is enabled, at the beginning of the parity bit.

TIMING DIAGRAMS (Continued)

EXTERNAL SYNCHRONIZATION WITH XSYNC

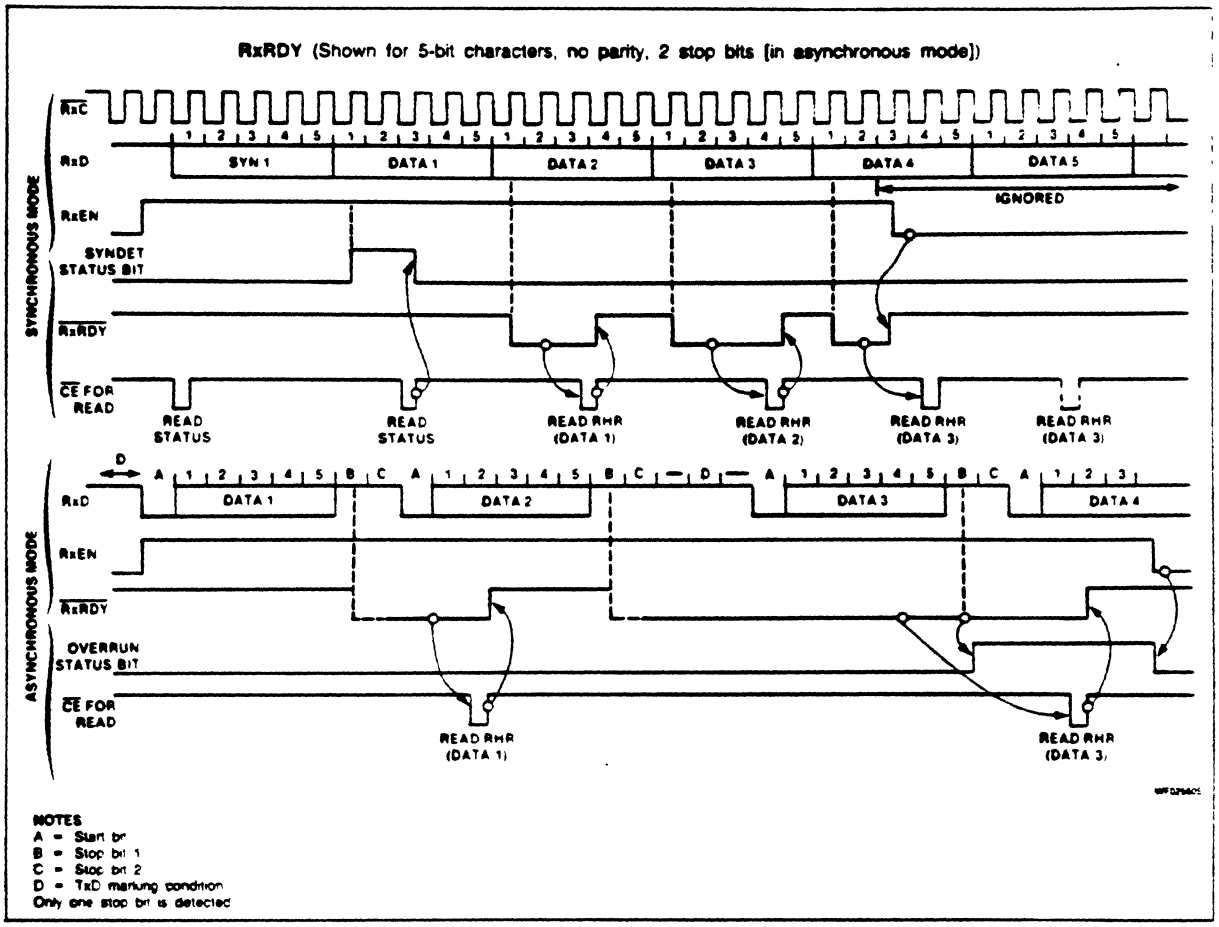


BREAK DETECTION TIMING



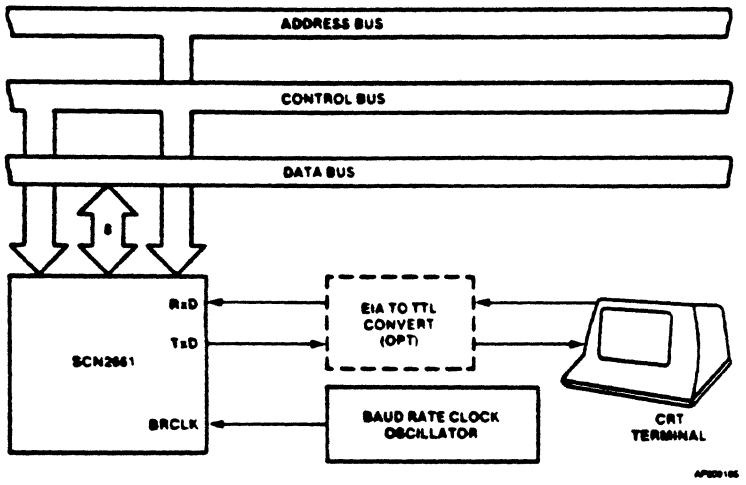
NOTE:
* If the stop bit is present the start bit search will commence immediately

TIMING DIAGRAMS (Continued)

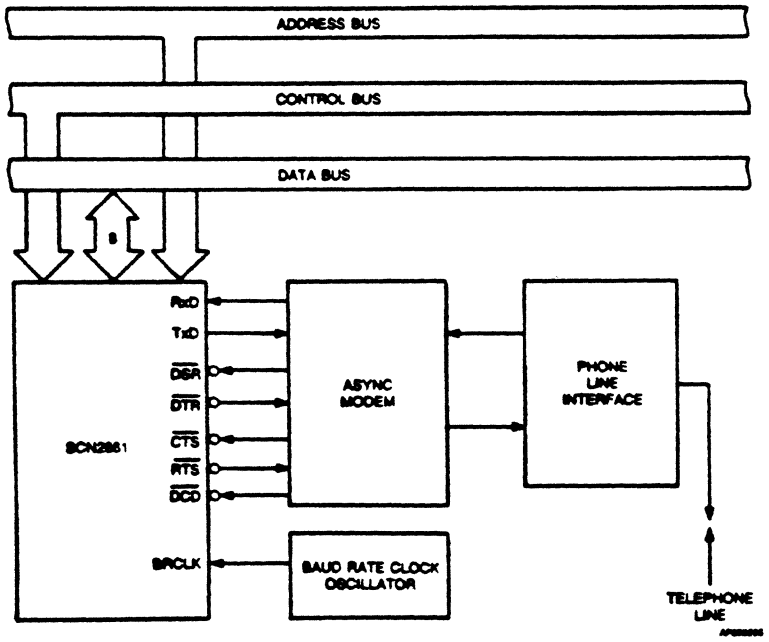


TYPICAL APPLICATIONS

ASYNCHRONOUS INTERFACE TO CRT TERMINAL

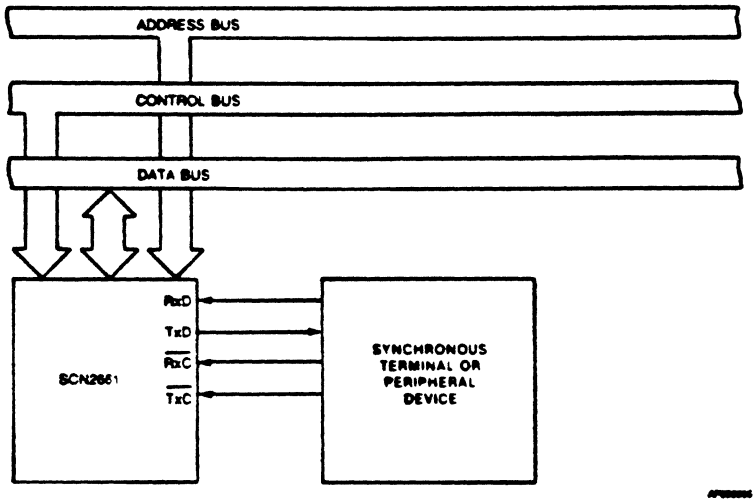


ASYNCHRONOUS INTERFACE TO TELEPHONE LINES

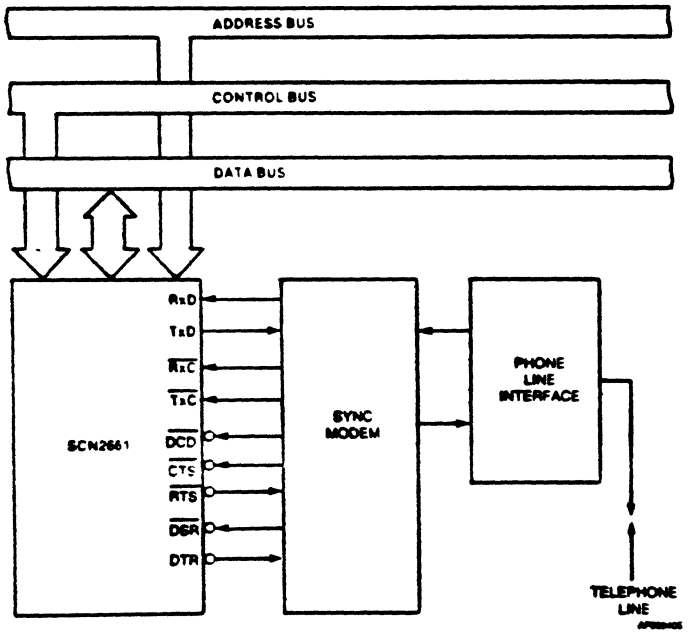


TYPICAL APPLICATIONS (Continued)

SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES



DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Signetics
a subsidiary of U.S. Philips Corporation

Signetics Corporation
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, California 94088-3409
Telephone 408/739-7700

98-8026-610 SI/DD3MCR385

APPENDIX B

Engineering Drawings

P A R T S L I S T

C3 INC. RESTON, VIRGINIA

NEW DUAL PORT COMMUNICATIONS ADAPTOR (DPCA) ASSY NO. 480040 R06

PARTS LIST NO. 400025 REV 10 05/02/85 AUTHORIZATION L G Brennenan

* REVISIONS *

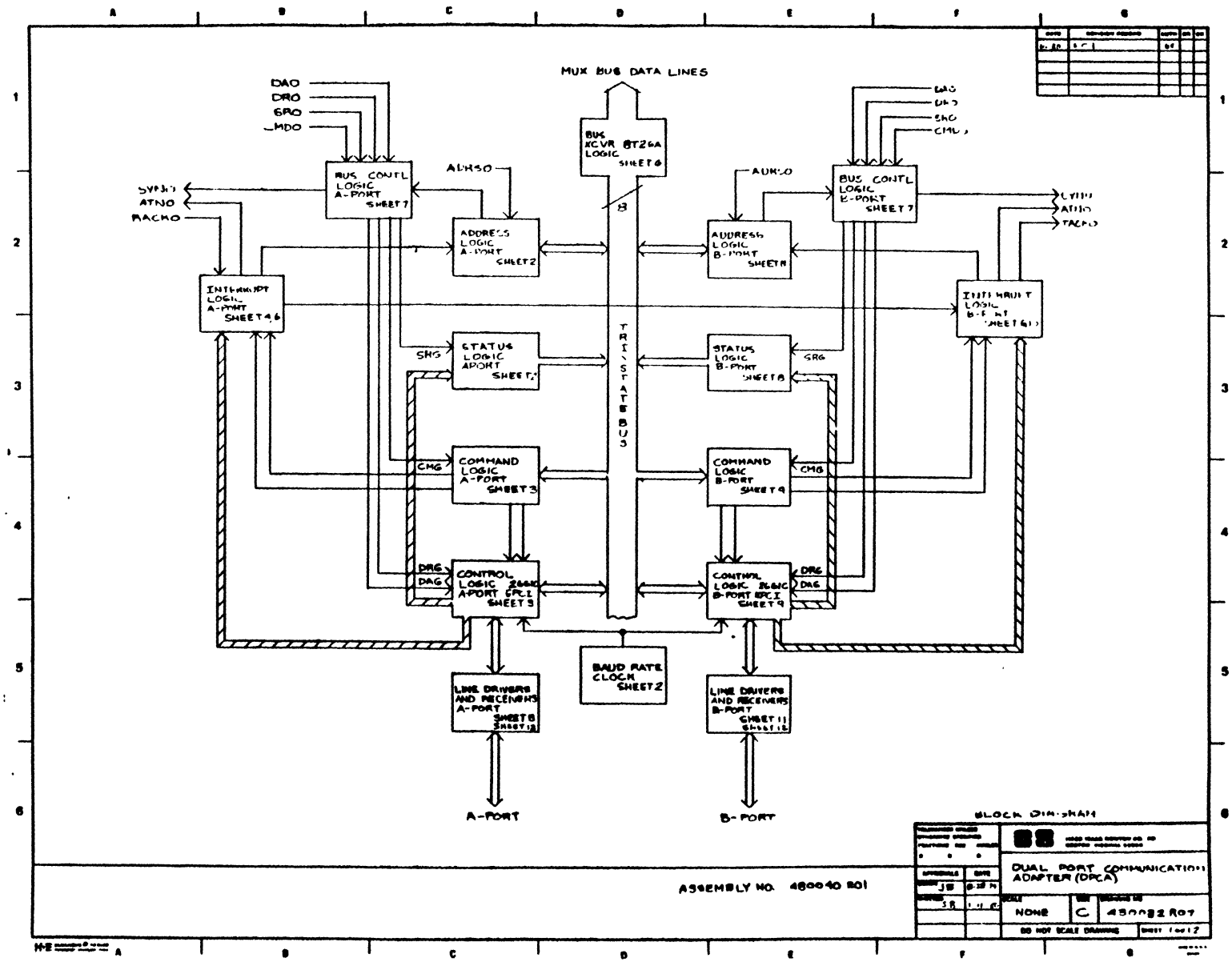
DATE	ITEM	CHANGE AND AUTH	
03/19/80	CORRECTED COSTS & QTY		
03/19/80	ADDED 10K, DIODES FOR 480040R01		
07/23/80	UPDATED PARTS LIST		
08/18/80	CHANGED .01 CAP (SYNC) TO .0068 TO MATCH 74LS133		
09/29/80	ITEM 1 R01 TO R02; ITEM 26 PRIME SOURCE		
09/29/80	ITEM 68,79,SPECIFIED		
06/21/83	added 1N914, 1K, 1000pf. Del .0068 per ECN-83-002		LGB
06/07/84	R08: Modified per ECN-84-007		LGB
11/27/84	R09: Modified per ECN-84-009		LGB
05/02/85	R10: Modified per ECN-85-007		LGB

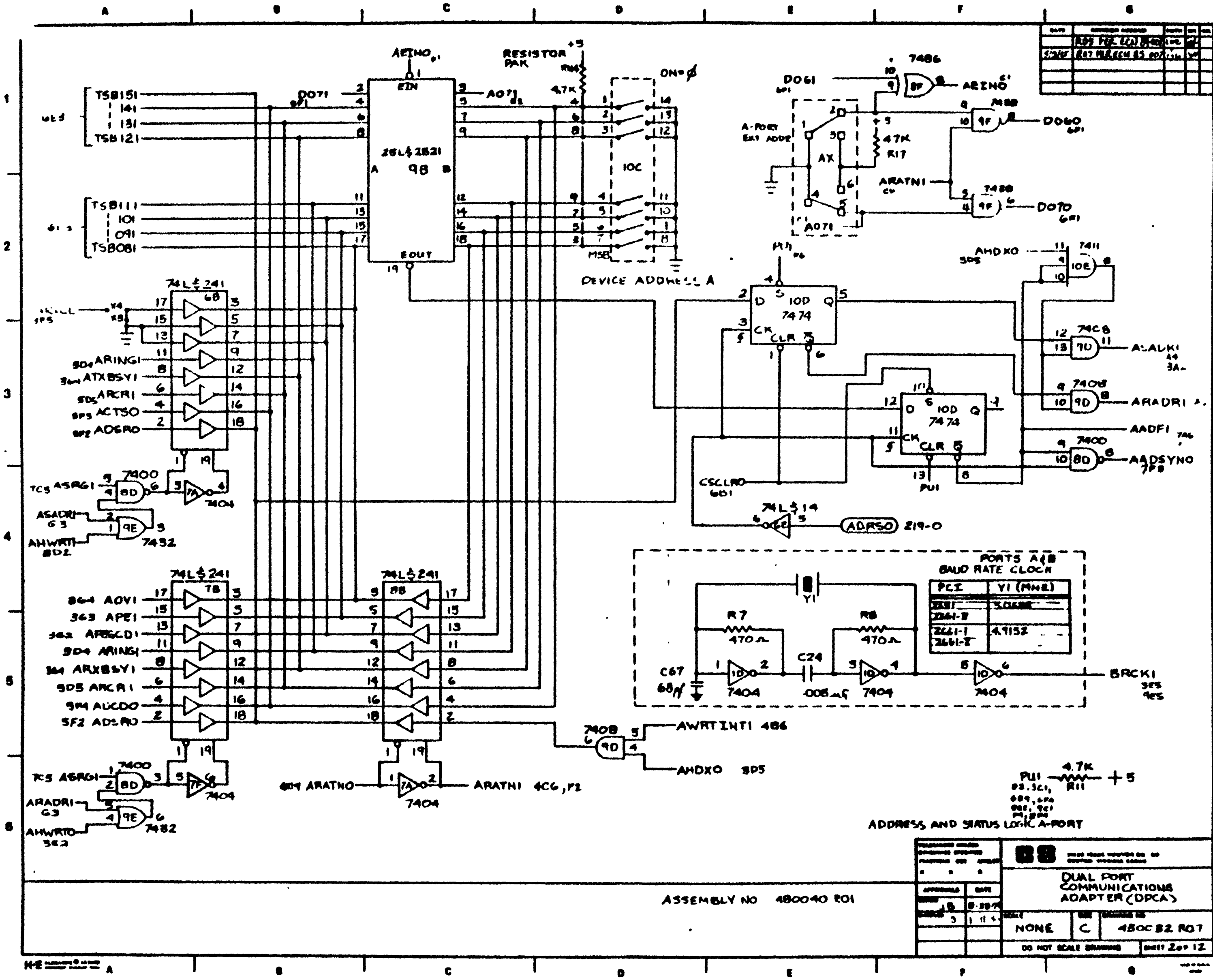
ITEM	* PART NUMBER *	* MFGR *	* DESCRIPTION *	QTY
1	460023 R03	C3	DPCA PCB per 440018 R02	1
2	7400		QUAD 2 INPUT NAND	6
3	7404		HEX INVERTER	7
4	7408		QUAD 2 INPUT AND	7
5	7411		TRIPLE 3 INPUT AND	3
6	74LS14		HEX INVERTER (SCHMIT)	1
7	7421		DUAL 4 IN AND	2
8	7427		TRIPLE 3 INPUT NOR	1
9	7430		8 INPUT NAND	1
10	7432		QUAD 2 INPUT OR	4
11	7438		QUAD 2 INPUT NAND BUFFER (OC)	2
12	7474		DUAL D FLIP FLOP	6
13	7486		QUAD 2 INPUT EXCLUSIVE OR	3
14	74175		QUAD D FLIP-FLOP	2
15	74LS241		OCTAL BUFFER	8
16	74S241		OCTAL BUFFER	ALT
17	74LS245		OCTAL BUS TRANSCEIVER (TS)	2
18	8T245	SIG*		ALT
19	DP8304	NAT,AMD	ENGN ALT FOR 74LS245	ENGN
20	74S133		13 INPUT NAND	1
21	74276	TI	QUAD J-K FLOP	2
22	25LS2521	AMD	8 BIT COMPARITOR	2
23	8T26A		QUAD BUS RECEIVER (TS)	2
24	26S02	AMD	DUAL ONE SHOT	6
25	9602			LT
26	74123	TI	DUAL RETRIG MULTI	2
27	2661C	SIG	EPCI	2
28	88LS120	NATL	DUAL LINE RCVR	8
29	88C120	NATL	ALT CMOS	ALT

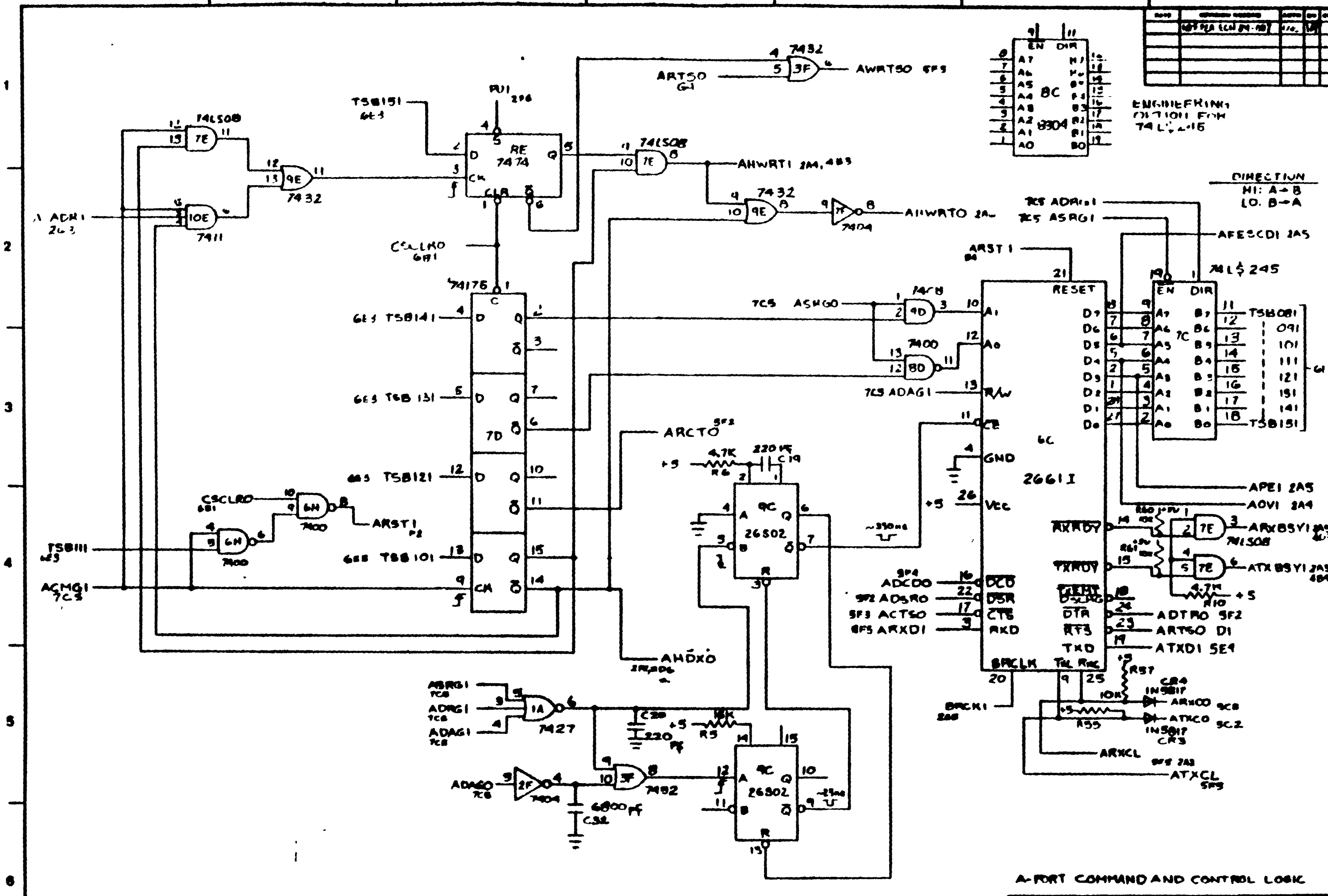
ITEM	* PART NUMBER *	* MFGR *	* DESCRIPTION *	QTY
30	9636A	FCHLD,TI	DUAL LINE DRIVER	6
31	MC3488A	MOT	DUAL LINE DRIVER	ALT
32	4310R101472	BOURNS	4.7K SIP RES PAK	2
33	750-101-R4.7K	CTS	4.7K SIP RES PAK	ALT
34	4306R101472	BOURNS	4.7K SIP RES PAK	2
35	750-61-R4.7K	CTS	4.7K SIP RES PAK	ALT
36	240004G	EECO	SPST FORM A 4 POS SWTCH	2
37	241003G	EECO	SPDT FORM C 3 POS SWTCH	2
38	87227-7	AMP*	7-pos .025" sq double row hdr	2
39	MF050	CTS KNIGHT	5.0688 MHZ XTAL	1
40	7812CP	MOTOROLA	+12V REGULATOR	1
41	UA7812C	TI	+12V REGULATOR	ALT
42	LM340T-12	NATIONAL	+12V REGULATOR	ALT
43	UA7812UC	FCHLD	+12V REGULATOR	ALT
44	7912CP	MOTOROLA	-12V REGULATOR	1
45	UA7912C	TI	-12V REGULATOR	ALT
46	LM320T-12	NATIONAL	-12V REGULATOR	ALT
47	UA7912UC	FCHLD	-12V REGULATOR	ALT
48	100 OHM 1-4W 5%		RESISTOR	5
49	470 OHM 1-4W 5%		RESISTOR	2
50	1K 1-4W 5%		RESISTOR	1
51	4.7K 1-4W 5%		RESISTOR	10
52	10K 1-4W 5%		RESISTOR	20
53	15K 1-4W 5%		RESISTOR	2
54	33K 1-4W 5%		RESISTOR	12
55	120K 1-4W 5%		RESISTOR	6
56	1N5817	MOTOROLA	DIODE	6
57	1N914		DIODE	3
58	1N4445		FAST SW DIODE	ALT

ITEM	* PART NUMBER *	* MFGR *	* DESCRIPTION *	QTY
59	5GA-T22	SPRAGUE	220 PF CAP	4
60	5GA-D10	SPRAGUE	.001 UF (1000 PF)	22
61	5GA-D50	SPRAGUE	.005 MICROFARAD CAP	1
62	5GA-D68	SPRAGUE	.0068 MICROFARAD CAP	2
63	T362A334K050AS	KEMET	.33 MICROFARAD TANTALUM CAP	2
64	T362A105K050AS	KEMET	1.0 MICROFARAD TANTALUM CAP	2
65	TVA 1148	SPRAGUE	25 MICROFARAD CAP	2
66	CK05 104K		DECOUPLING CAP	32
67	V18ZA1	GE	Varistor, 14VDC continuous	6
68	206604-1	AMP	25 PIN MALE CONN	2
69	205817-1	AMP	25 PIN FEMALE HDWRE	2
70	3-86018-4	AMP	84 PIN CONNECTOR	1
71	87224-2	AMP*	2-pos .025" sq header	14
72	87227-6	AMP*	6-pos .025" sq double row hdr	1
73	530153-2	AMP*	0.100" 2-pos shunt	26
74			8 PIN IC SOCKET	6
75			14 PIN IC SOCKET	0
76			16 PIN IC SOCKET	8
77			20 PIN IC SOCKET	0
78			28 PIN IC SOCKET	2
79	350-1300-09-07	CAMBION	STANDOFF	4
80	4-40 1/4 screw		4-40 1/4" ss phillips screw	4
81	4-40 hex nut		4-40 hex nut	4
82	5GA-Q68	SPRAGUE*	68pf,20%(mx),10v(mn) cer cap	1
*				
*	Alternates for item 36 - EECO 240004C:			
*				
83	435166-2	AMP	SPST 4 position DIP switch	ALT
84	78R04	Grayhill	SPST 4 position DIP switch	ALT

ITEM	* PART NUMBER *	* MFGR *	* DESCRIPTION *	QTY
85	206-4	CTS	SPST 4 position DIP switch	ALT
*				
*	Alternates for item 37 - EECO 241003G:			
*				
86	435470-2	AMP	SPDT 3 position DIP switch	ALT
87	78J03	Grayhill	SPDT 3 position DIP switch	ALT
88	206-123	CTS	SPDT 3 position DIP switch	ALT
*				
*	The following items, although not part of			
*	the PC board assembly, should be purchased			
*	in coordination with the PC boards.			
*	(These items should be included in the "Half-Board" Kit.)			
*				
89	415-7036-01	CAMBION	CARD EJECTOR	2
90			PIN GUIDE	2
91	4-40 1/4 SCREW		4-40 1/4 SS PHILLIPS SCREW	6
92	4-40 HEX NUT		4-40 SS HEX NUT	4
*		*Or equivalent		


MUX BUS DATA LINES
DAO
DRO
SRO
CMDO
BUS XCVR BT26A LOGIC SHEET6
BUS CONTL LOGIC A-PORT SHEET7
BUS CONTL LOGIC B-PORT SHEET7
ADRSO
SYNO
ATNO
RACKO
ADDRESS LOGIC A-PORT SHEET2
ADDRESS LOGIC B-PORT SHEET8
INTERRUPT LOGIC A-PORT SHEET4&5
INTERRUPT LOGIC B-PORT SHEET10
STATUS LOGIC A-PORT SHEET
STATUS LOGIC B-PORT SHEET8
SRG
COMMAND LOGIC A-PORT SHEET3
COMMAND LOGIC B-PORT SHEET9
CMG
DRG
DAG
CONTROL LOGIC 2646 A-PORT DPCI SHEET3
CONTROL LOGIC 8L61C B-PORT DPCI SHEET9
TRISTATE BUS
BAUD RATE CLOCK SHEET2
LINE DRIVERS AND RECEIVERS A-PORT SHEET5 SHEET12
LINE DRIVERS AND RECEIVERS B-PORT SHEET11 SHEET12
A-PORT
B-PORT
BLOCK DIAGRAM
DUAL PORT COMMUNICATION ADAPTER (DPCA)
ASSEMBLY NO. 480040 R01
NONE
C
480032 R07
DO NOT SCALE DRAWING


DEVICE ADDRESS A
RESISTOR PAK
26LS2821
9B
10C
74LS241
6B
7B
8B
7474
10D
74LS14
ADRSO 219-0
PORTS A&B BAUD RATE CLOCK
PCI
Y1 (MHZ)
2661-1
2661-2
4.9152
C67
68pf
C24
.005 μf
R7
470Ω
R8
470Ω
BRCK1
7404
7400
7408
7432
7486
7411
AWRTINT1 4B6
AHDXO 5D5
ARATNO
ARATNI 4C6, F2
PU1
4.7K
R11
+5
CSCLRO
AARDI
AADFI
AADSYNO
ARADRI
ARINO
DO60
DO70
DO61
A071
ON=Ø
MSB
TSB151
TSB121
TSB111
TSB081
ADDRESS AND STATUS LOGIC A-PORT
ASSEMBLY NO 480040 R01
DUAL PORT COMMUNICATIONS ADAPTER (DPCA)
NONE
C
480C32 R07
DO NOT SCALE DRAWING
SHEET 2 OF 12



A-PORT COMMAND AND CONTROL LOGIC

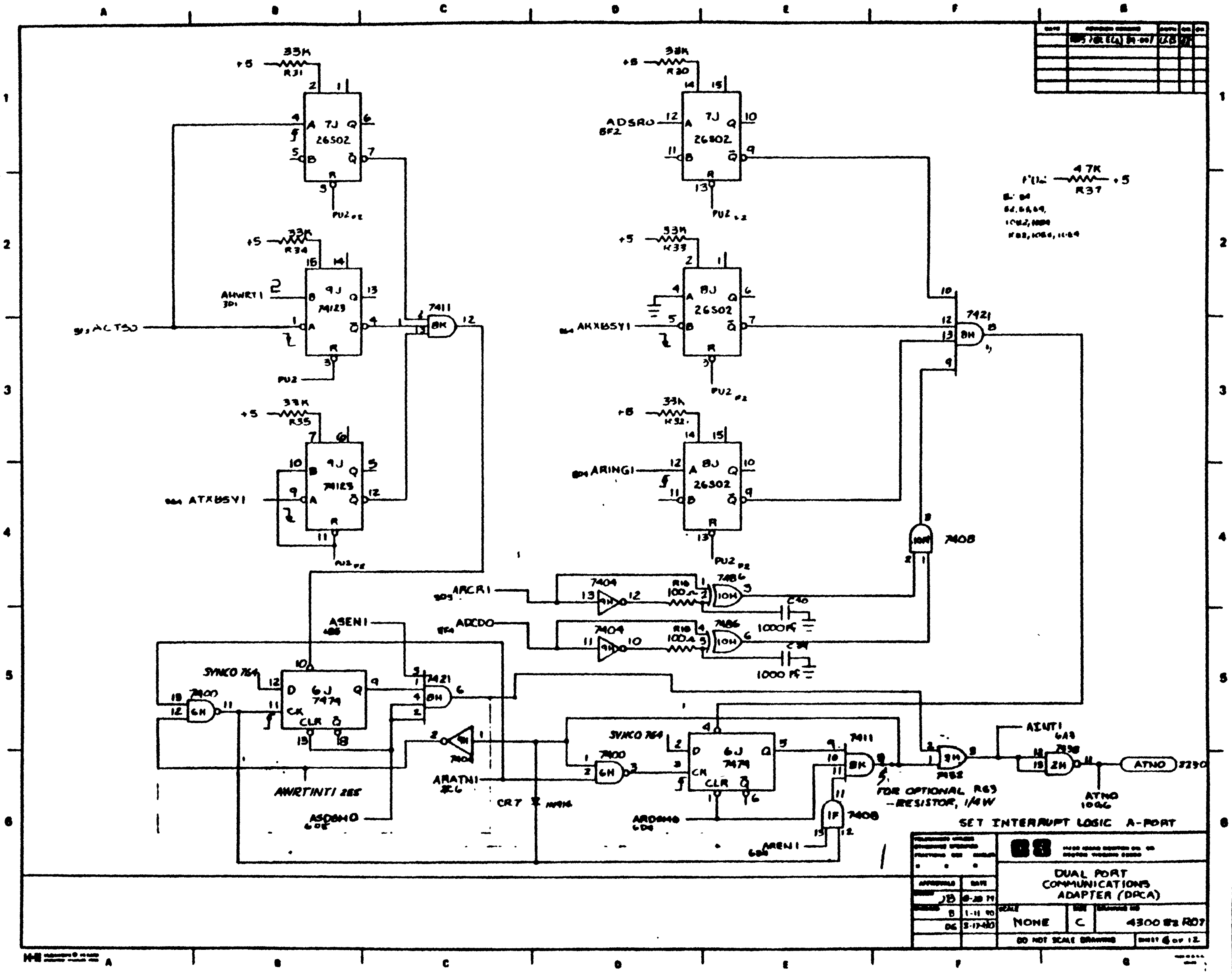
NOTE: AHDXO HI, INDICATES FULL DUPLEX, A-PORT

DUAL PORT COMMUNICATIONS ADAPTER (DPCA)

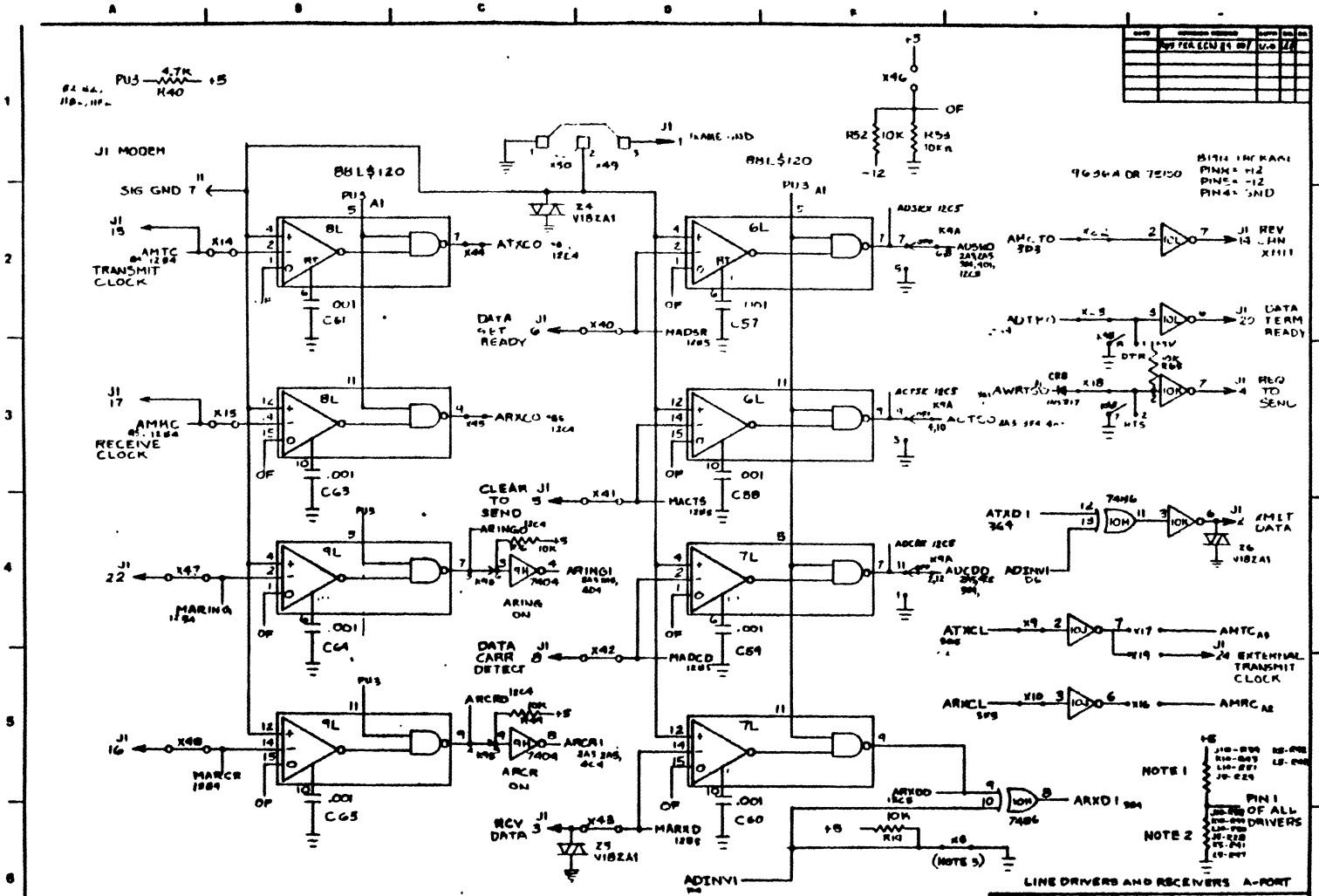
NONE | C | 4500052 R07

DO NOT SCALE DRAWING

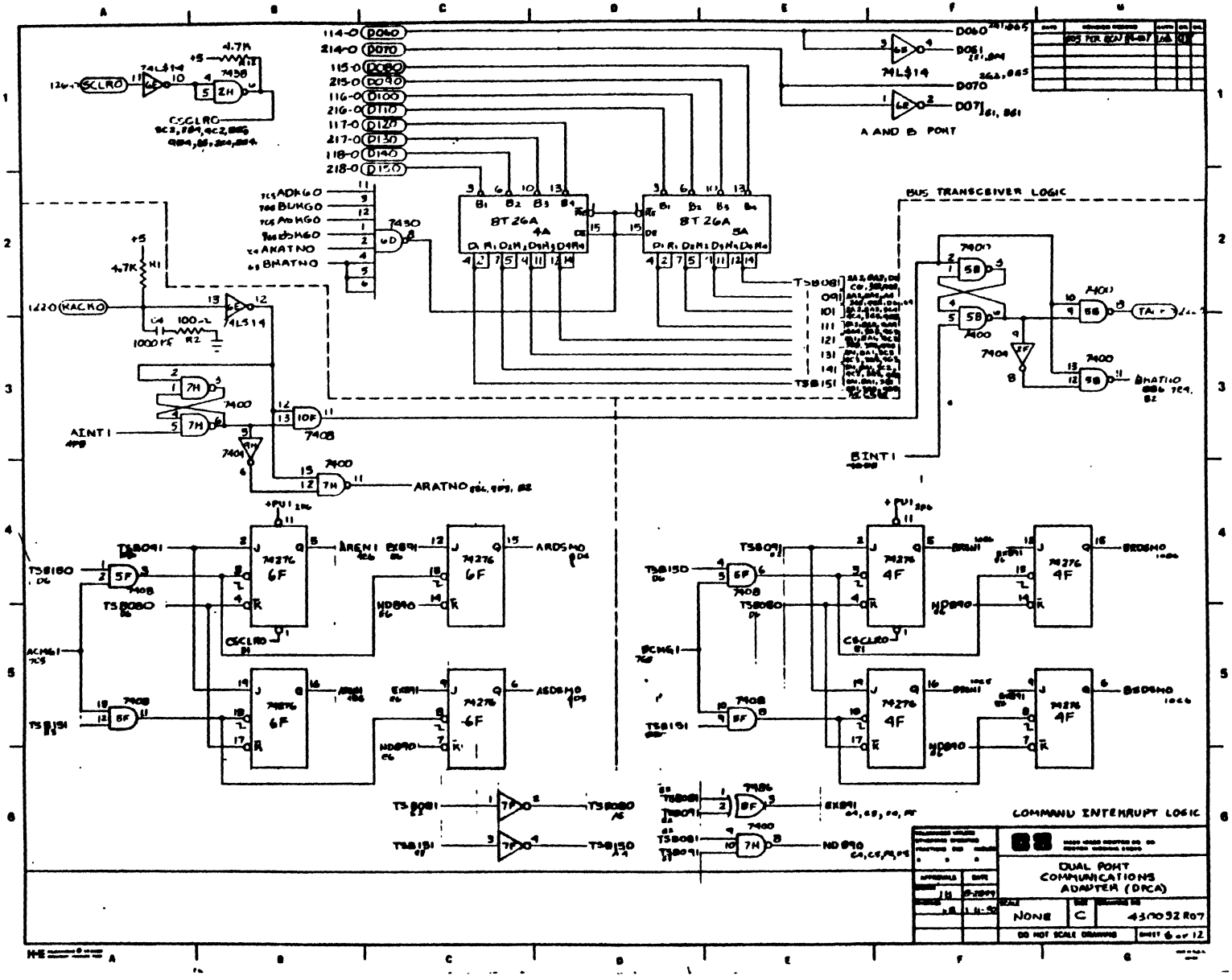
SHEET 5 OF 12

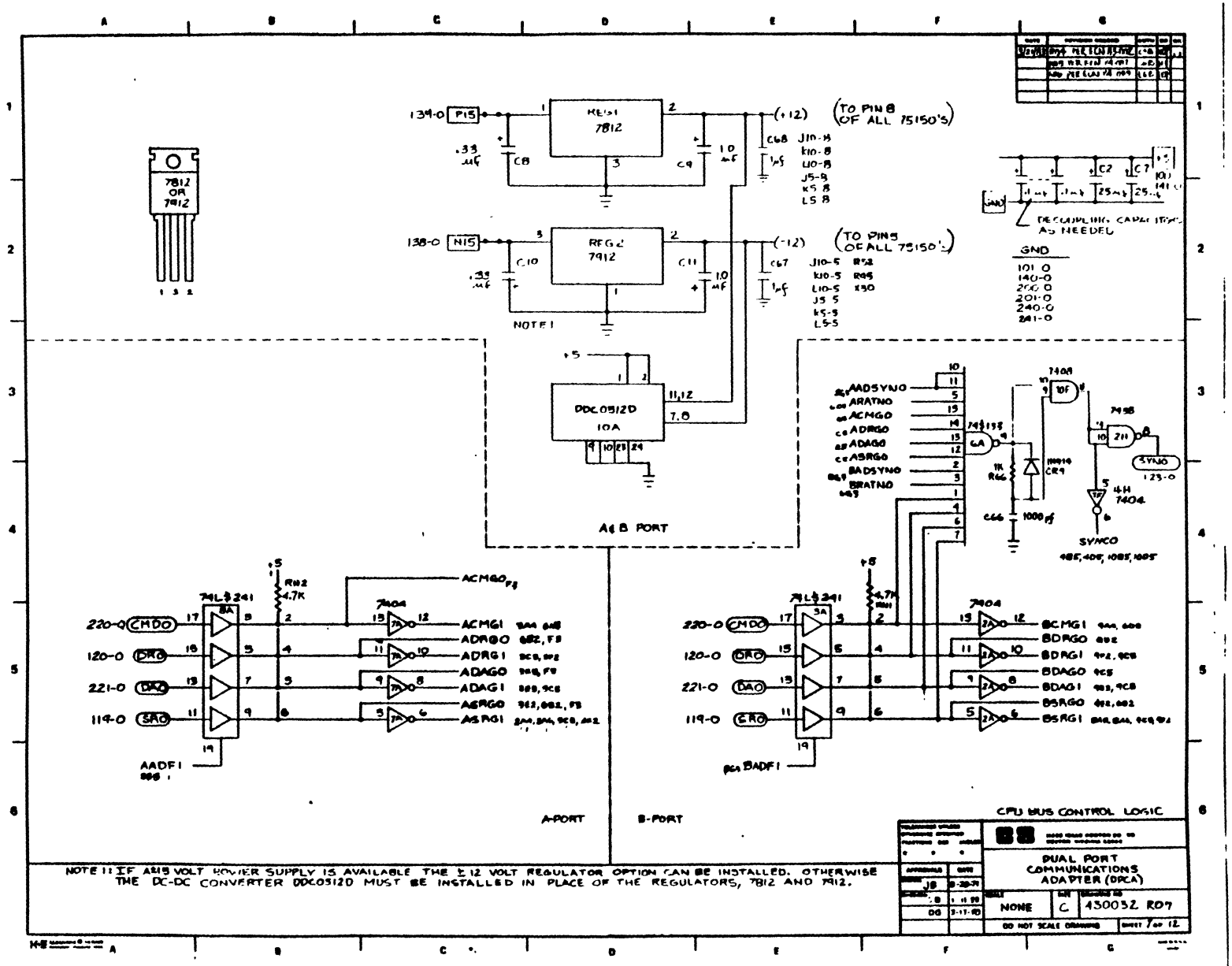


SET INTERRUPT LOGIC A-PORT
DUAL PORT COMMUNICATIONS ADAPTER (DPCA)
NONE
C
DO NOT SCALE DRAWING
26502
74123
7474
7421
7411
7400
7404
7486
7408
ACTSO
AHWRT1
ATXBSY1
ADSRO
AKXBSY1
ARING1
ARCR1
ARCDO
ASEN1
ARATN1
ASDBHO
ARDBHO
AREN1
AINT1
ATNO
CR7
FOR OPTIONAL R63
RESISTOR, 1/4W

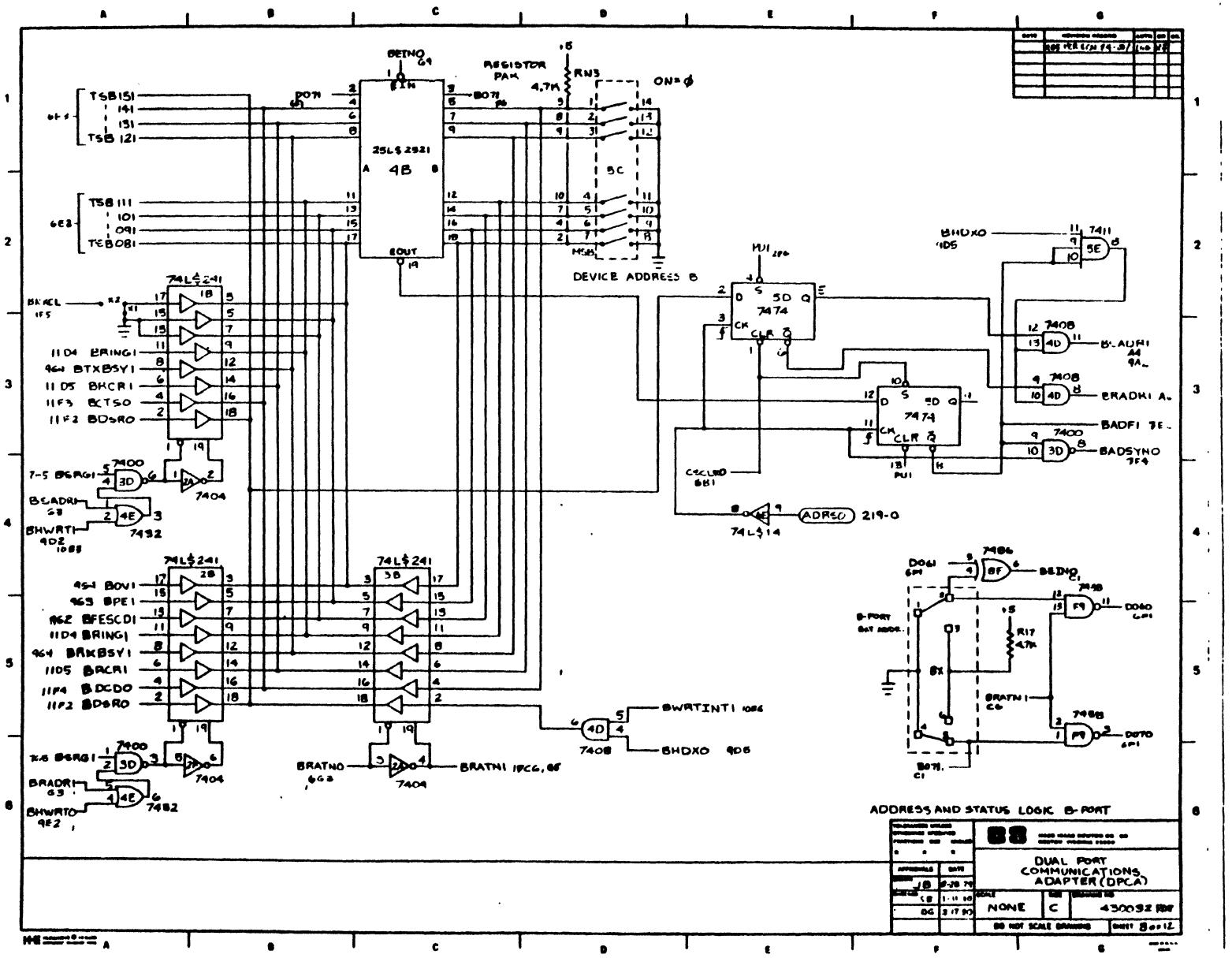


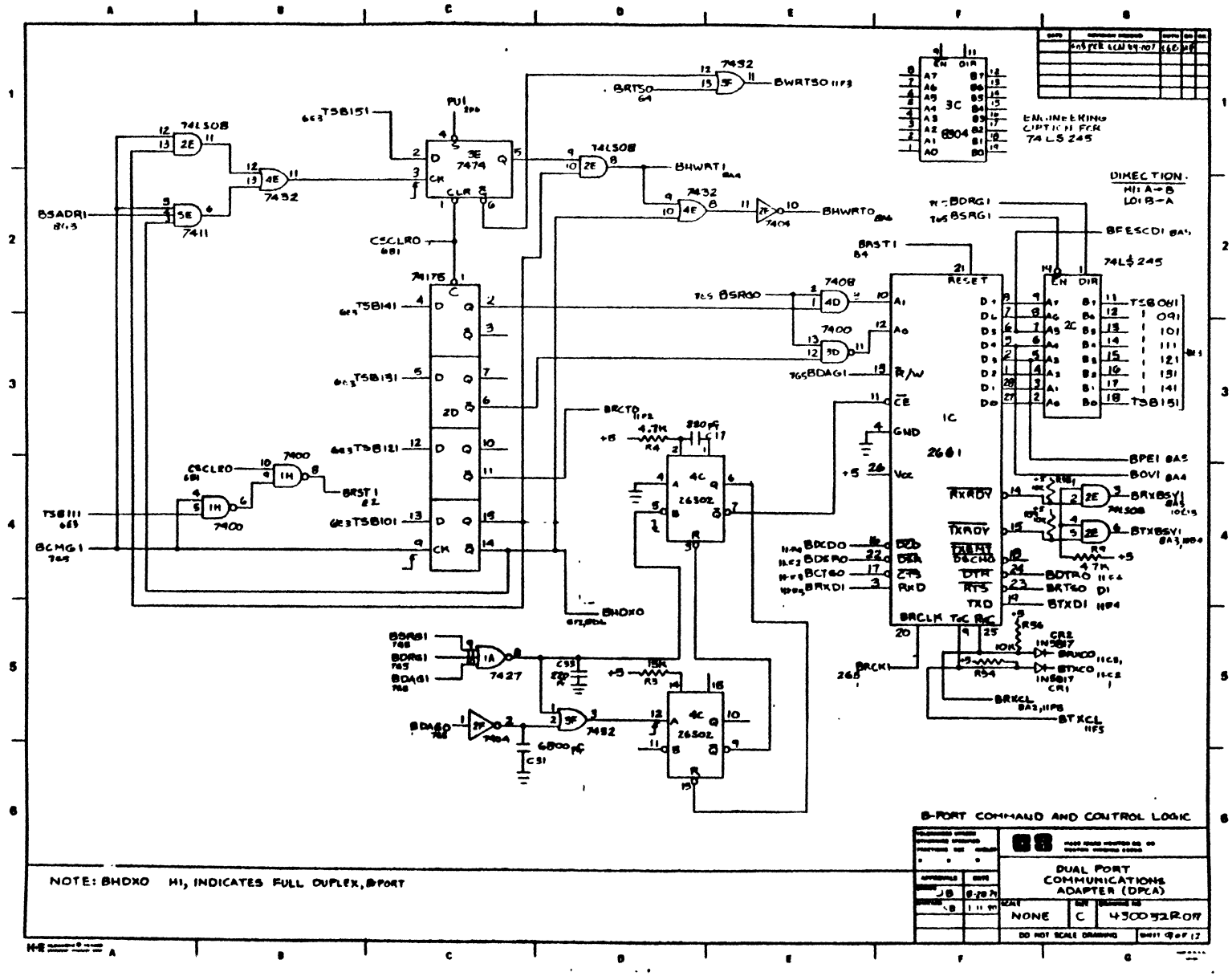
NOTES:
1. INSTALL 10K RESISTORS FOR 75150 (RS232)
2. INSTALL 82K RESISTORS FOR 9696 (MIL.STD.188)
3. REMOVE JUMPER (X6) FOR INVERTED MIL.188 OPERATION.

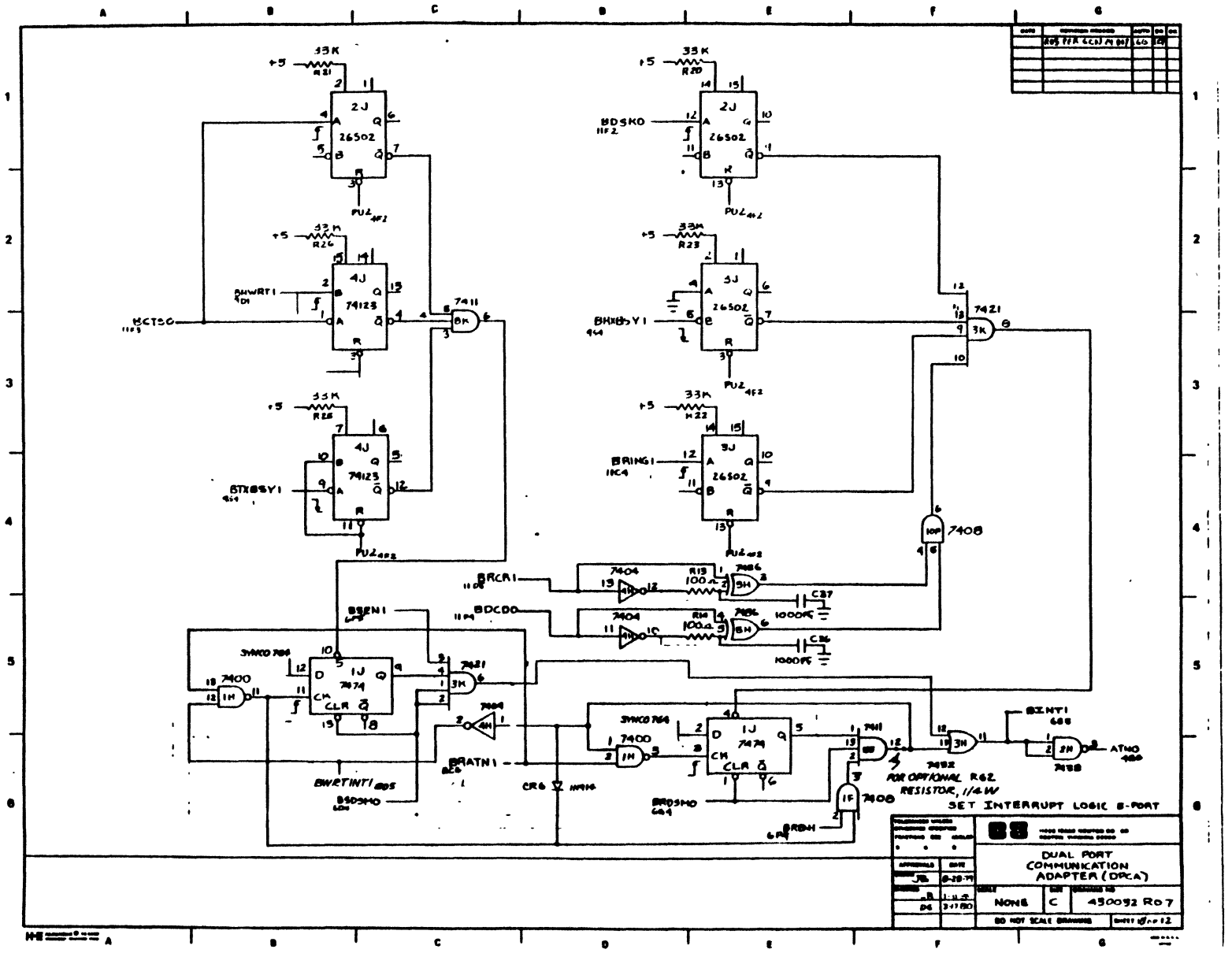

BUS TRANSCEIVER LOGIC
A AND B PORT
COMMAND INTERRUPT LOGIC
DUAL PORT COMMUNICATIONS ADAPTER (DPCA)
NONE
C
1430092 R07

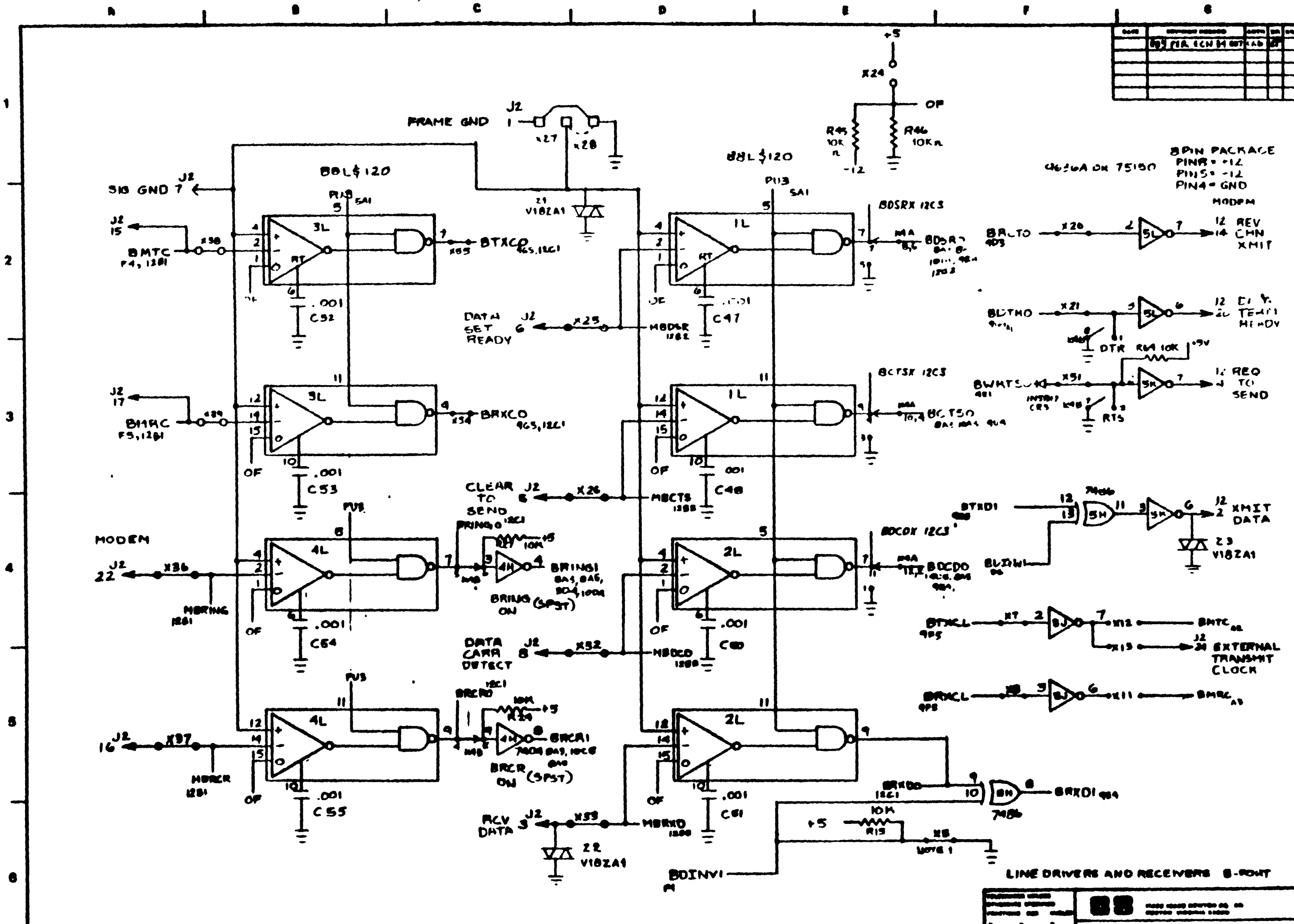


NOTE 1: IF A ±15 VOLT POWER SUPPLY IS AVAILABLE THE ± 12 VOLT REGULATOR OPTION CAN BE INSTALLED. OTHERWISE THE DC-DC CONVERTER DDC0512D MUST BE INSTALLED IN PLACE OF THE REGULATORS, 7812 AND 7912.


TSB151
141
131
TSB121
TSB111
101
091
TSB081
BEINO
BIN
BOUT
25LS2521
4B
REGISTER PAK
4.7K
RN3
ON=0
5C
DEVICE ADDRESS B
74LS241
74LS14
7474
7400
7404
7402
7408
7411
7486
BHDXO
BWRTINT1
BRATNO
BRATN1
ADRS0 21-0
DEVICE ADDRESS AND STATUS LOGIC B-PORT
DUAL PORT COMMUNICATIONS ADAPTER (DPCA)
NONE
C
430092


B-PORT COMMAND AND CONTROL LOGIC
NOTE: BHDXO HI, INDICATES FULL DUPLEX, B PORT
DUAL PORT COMMUNICATIONS ADAPTER (DPCA)
NONE
C
4300352R017
DIRECTION. HI: A→B LO: B→A
ENGINEERING OPTION FOR 74LS245
DO NOT SCALE DRAWING


33K
+5
2J
26502
PUZ 4F1
33K
4J
74123
7411
BHWRT1
BCTSO
PUZ 4F2
BSTXBSY1
PUZ 4F3
33K
R20
BDSKO
PUZ 4F1
33K
R23
3J
BHRBSY1
7421
PUZ 4F2
33K
R22
BRING1
PUZ 4F3
7408
7404
7086
R13
100Ω
C37
1000PF
BRCA1
BDCDO
R14
C36
BSEN1
SYNCO 76H
7400
1H
7474
CLR
BWRTINT1
BSDSMO
BRATN1
CR6
7441
7432
FOR OPTIONAL R62
RESISTOR, 1/4W
BINT1
ATNO
7438
SET INTERRUPT LOGIC B-PORT
BRDSMO
BRDH
DUAL PORT
COMMUNICATION
ADAPTER (DPCA)
NONE
C
450092 R07

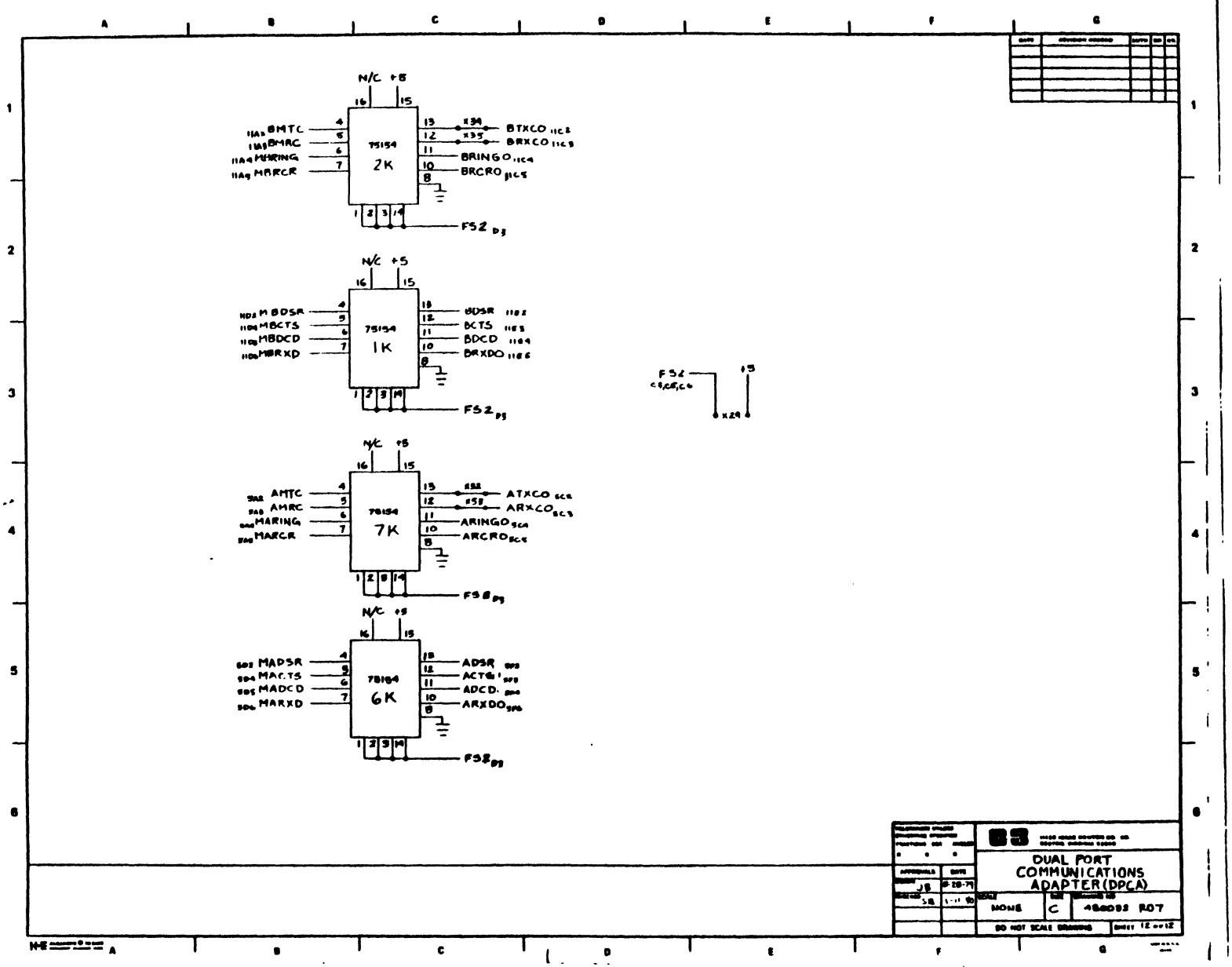


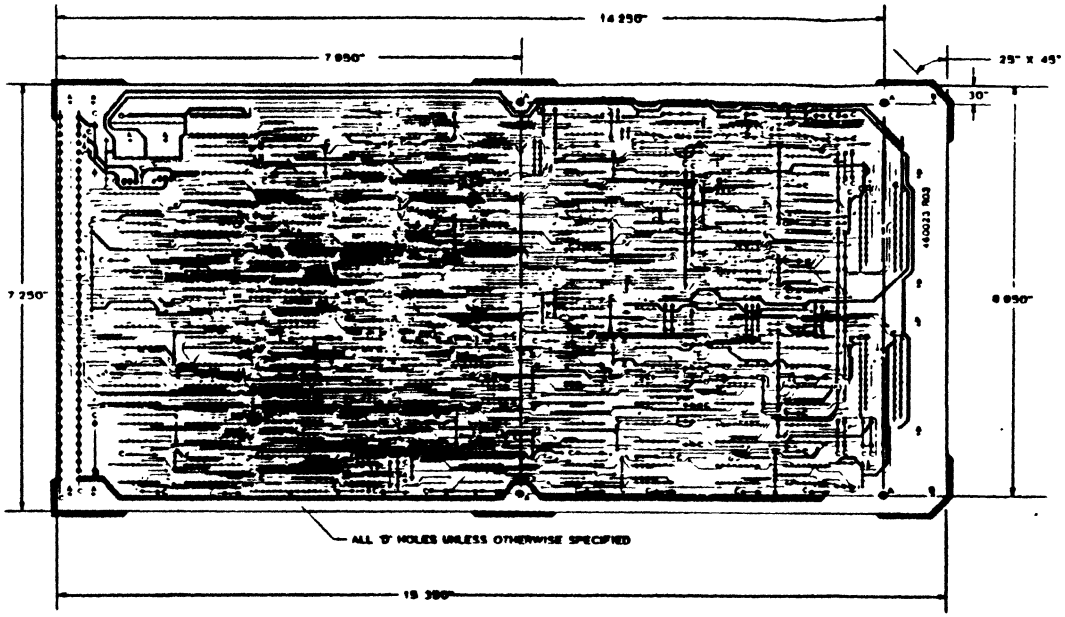
NOTE: 1. REMOVE JUMPER (X5) FOR INVERTED MIL.188 OPERATION.

DUAL PORT COMMUNICATION ADAPTER (DPCA)

SCALE	NONE
SIZE	C
DWG NO.	430032 R07
SHEET	13 OF 12

DO NOT SCALE DRAWING


N/C +5
75154
2K
BMTC
BMRC
MRING
MRRCR
BTXCO
BRXCO
BRINGO
BRCRO
FS2
N/C +5
75154
1K
MBDSR
MBCTS
MBDCD
MBRXD
BDSR
BCTS
BDCD
BRXDO
FS2
FS2
+5
X29
N/C +5
75154
7K
AMTC
AMRC
MARING
MARCR
ATXCO
ARXCO
ARINGO
ARCRO
FS8
N/C +5
75154
6K
MADSR
MACTS
MADCD
MARXD
ADSR
ACTS
ADCD
ARXDO
FS8
DUAL PORT
COMMUNICATIONS
ADAPTER(DPCA)
NONE
C
48D93 R07
DO NOT SCALE DRAWING



CIRCUIT SIDE

NOTES.

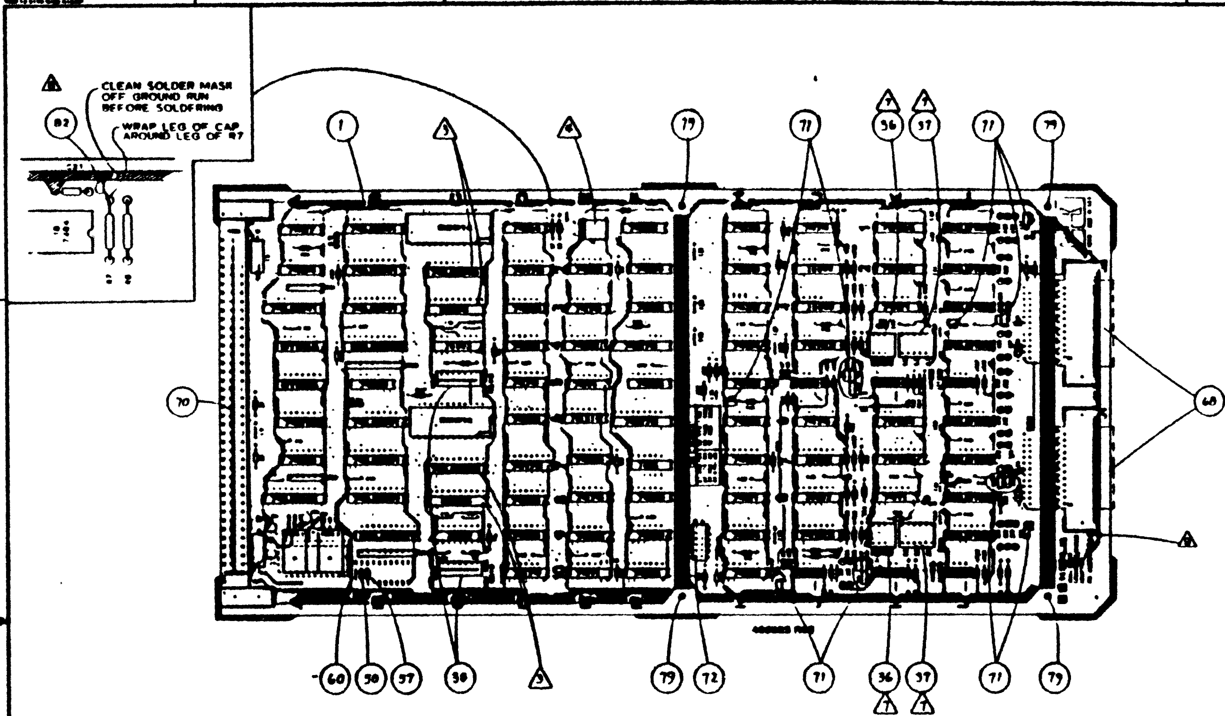
1. MATERIAL
   A) .062" THICK EPOXY BOARD TYPE: FR4, COLOR: NATURAL. 1 OZ. THICK COPPER CLAD 2 SIDES. UL APPROVED
2. DRILLING
   A) ALL HOLES ARE FINISHED SIZE AFTER PLATING
   B) ALL HOLES TO BE DRILLED TO BEST COMMERCIAL STANDARDS.
   C) ALL HOLES SHALL BE LOCATED WITHIN .003" OF THEIR TRUE POSITION WITH RESPECT TO CENTER OF PAD
   D) HOLE DIAMETER, UNLESS OTHERWISE NOTED, ±.004"
   E) SCHEDULE

SYMBOL	SIZE - DIA.	QTY
A	.145"	14
B	.125"	2
C	.040"	516
D	.038"	1678
UNMRKD	.034"	NC

3. FINISH
   A) PLATE-THRU WITH COPPER, UNLESS OTHERWISE NOTED MINIMUM PLATING THICKNESS .0012"
   B) TIN-LEAD ELECTRO-PLATE BOARD SURFACES. TIN CONTENT TO BE 60% ±10%.
   C) APPLY SOLDER MASK FRONT & BACK. USE SUPPLIED FILMWORK. CURE PER RECOMMENDED DIRECTIONS. MASK TYPE: EPOXY. COLOR: GREEN. MFG: MODERMAT
   D) APPLY SILKSCREEN TO FRONTSIDE. LETTERING & LINEWORK TO BE CLEAR & NON-SMEARED. INK TYPE: EPOXY. COLOR: WHITE.
4. GENERAL
   A) FRONT TO BACK REGISTRATION BETTER THAN .005"
   B) MECHANICAL TOLERANCE: .XX" ± .010", .XXX" ± .005"
   C) MINIMUM CONDUCTOR WIDTH: .012"
      MAXIMUM CONDUCTOR WIDTH: ——
      MINIMUM AIR GAP: .012"
   D) THIS PRINTED CIRCUIT BOARD IS TO BE FABRICATED TO BEST STANDARDS. THE FINISHED BOARD IS TO MEET THE ABOVE REQUIREMENTS, & SPECIFICATIONS. THE FINISHED BOARD WILL NOT HAVE THE FOLLOWING: NICKS, SCRATCHES, VOIDS, EXPOSED COPPER, POOR PLATING, OR MISDRILLED HOLES.
   E) PACK FINISHED BOARDS WITH PROTECTIVE COVERING.

RE: 400023

	AF-AMPE	C3	11495 ISAAC NEWTON SQUARE SO RESTON, VIRGINIA 22090 5084 (703)471-6000 TELEX 901759
			DUAL PORT COMMUNICATION ADAPTER
		D	440018 02
		SCALE: FULL	1150 AF AMPE



1. ITEM NUMBERS REFER TO PARTS LIST. IC'S & DISCRETE COMPONENTS ARE IDENTIFIED IN THE SCHEDULE AT RIGHT.
2. THESE LOCATIONS ARE SOCKETED.
3. USE EITHER ITEM 17 OR 18, NOT BOTH.
4. PLACE PAD OF SILICON RUBBER CEMENT, (RTV-108 OR EQUIV.) UNDER CRYSTAL.
5. SEE SHEET 2 FOR FINAL CONFIGURATION INFORMATION.
6. ITEMS ON PARTS LIST CAN BE LOCATED IN ABOVE DRAWING EXCEPT ITEMS 69, 73, 80 & 81 WHICH APPEAR ON SHEET 2 OF THIS DRAWING.
7. INSTALL DIP SWITCHES AFTER VAPOR DEGREASE.
8. ADD ITEM 82 PER ILLUSTRATION.
9. CHANGE REVISION LEVEL MARKING TO R06

COMPONENTS SCHEDULE

PARTS LIST

PCB ARTWORK	460023
PCB FABRICATION	440016
SCHEMATIC	430032
PARTS LIST	400025
NAME	NUMBER

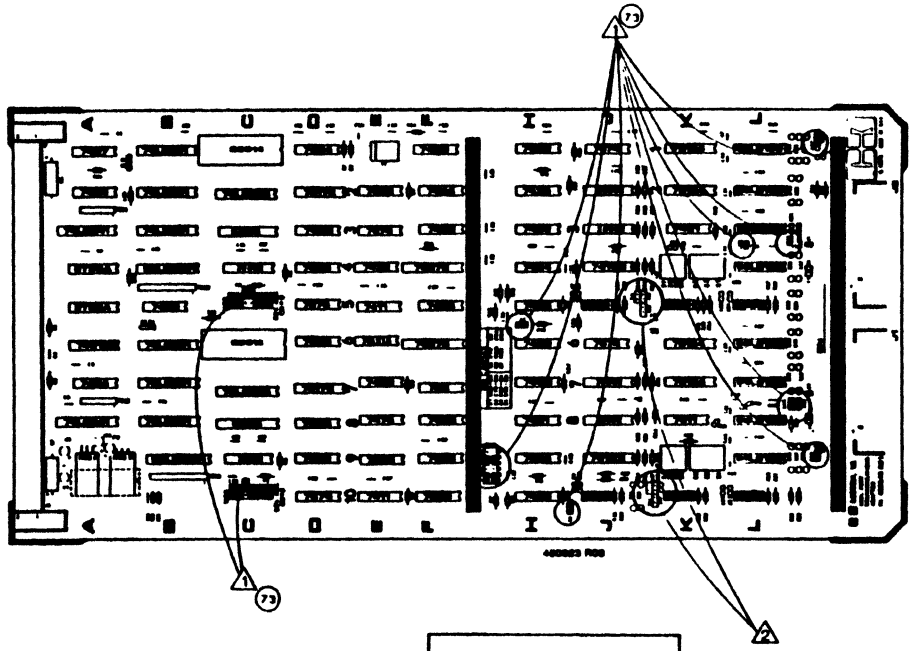
DOCUMENTATION CROSS-REF

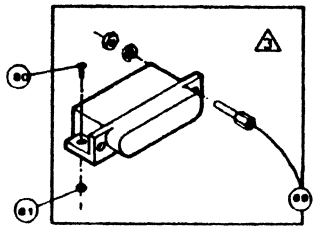
11425 ISAAC NEWTON SQUARE, SO.
RESTON, VIRGINIA 22090 5094
(703)471-0000 TELEX 901750

DUAL PORT COMMUNICATIONS ADAPTOR
PCB ASSEMBLY

SIZE	DWG NO.	REV
D	480040	06

SCALE NONE | 1:50 | SHEET 1 OF 2





NOTES:

1. INSTALL 0.100" SHUNTS, TWENTY SIX LOCATIONS AS SHOWN.
2. DO NOT INSTALL SHUNTS IN LOCATIONS INDICATED.
3. INSTALL ITEM 69 FOUR PLACES AS SHOWN, RIGHT.

FINAL CONFIGURATION

C3	D	480040	06
NONE	AF AMPE 1150	SHEET 2 OF 2	

11425 Isaac Newton Square
Reston, Virginia 22090