iSBX 351™ SERIAL MULTIMODULE™ BOARD HARDWARE REFERENCE MANUAL

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PREFACE

This manual provides general information, installation considerations, programming information, principles of operation, and service information for the Intel iSBX 351 Serial Multimodule Board. Additional information is available in the following documents:

- *Intel MCS-85 User's Manual,* Order Number 9800366
- *Intel 8080/8085 Assembly Language Programming Manual,* Order Number 9800301
- *Intel Peripheral Design Handbook,* Order No. 9800676
- *Intel Multibus Specifications,* Order No. 9800683

CONTENTS

TABLES

TABLES (Continued)

ILLUSTRATIONS

CHAPTER 1
GENERAL INFORMATION

1-1. INTRODUCTION

The iSBX 351 Serial Multimodule Board is a member of Intel's growing line of expansion Multimodule boards designed to augment the iSBC microcomputers. The Multimodule board provides for expansion of the system serial communications capability by adding one complete, independent, synchronous/asynchronous, RS232C and RS422/RS449 compatible, serial communications channel. This chapter contains a description of the Multimodule board, and lists the equipment supplied, compatible equipment, and specifications.

1-2. DESCRIPTION

The Multimodule board (figure 1-1) is designed to be plugged onto a host iSBC microcomputer to provide an additional serail I/O interface capability. The Multimodule board contains an 8251A USART (Universal Synchronous Asynchronous Receiver-Transmitter) device to handle RS232C or RS422 compatible serial I/O communication schemes. The board also holds an 8253 PIT (Programmable Interval Timer) device that controls frequency and timing functions generated from an on-board 8224 Clock Generator. Baud rates, data formats, and interrupts are jumper and program selectable on the Multimodule board. When operating as an RS232C interface, the Multimodule board requires +5V, −12V, and +12V power. However, as an RS422 interface, only +5V power is required.

The serial I/O port is fully RS232C and RS422/449 compatible; the Multimodule board is electrically compatible with RS422, and mechanically compatible with RS449. Serial communication is implemented with an 8251A USART that may be programmed for operation in most synchronous or asynchronous serial data transmission formats. The serial I/O port features full- or half-duplex, buffered, transmit and receive capability.

An RS422/449 application of the Multimodule board allows operation in a full- or half-duplex multidrop configuration, in which several iSBX 351 Serial Multimodule Boards share the same two-wire data line. This requires that the user exert software control over each slaves' output to the data line.

The programmable interval timer provides three separate time/rate clocks, two of which are available for off-board timing and synchronization. The third clock provides timing for the receive and transmit circuitry on the 8251A USART.

The Multimodule board may be wired to generate interrupt requests continuously at a clock rate or on request from the 8251A USART. Interrupt priority is determined on the host iSBC microcomputer.

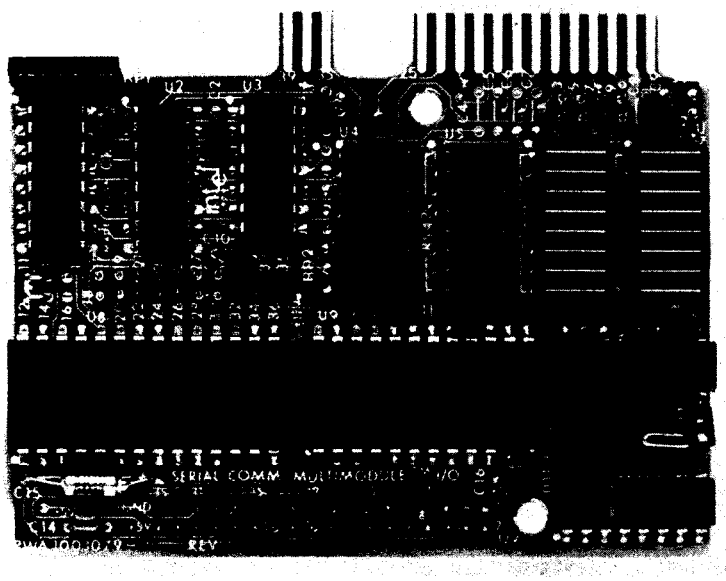


Figure 1-1. iSBX 351™ Serial Multimodule™ Board

1-3. EQUIPMENT SUPPLIED

The following equipment is supplied with the Multimodule board:

a. Schematic Diagram, dwg. no. 142842.
b. Assembly Diagram, dwg. no. 1003079.
c. 2 Screws, ¼" x 6/32 nylon.
d. 1 spacer, ½" x 6/32 nylon.

1-4. COMPATIBLE EQUIPMENT

The Multimodule board must be used with a host iSBC microcomputer that includes an iSBX bus connector.

The Multimodule board cannot directly access the Multibus bus structure. Multibus interfacing is provided through the P1 Multibus connector on the host iSBC microcomputer.

1-5. SPECIFICATIONS

Specifications for the iSBX 351 Serial Multimodule Board are provided in table 1-1.

Table 1-1. Specifications

I/O ADDRESSING

I/O addressing is dependent on the Multimodule connector used on the host iSBC microcomputer. Reference table 3-1.

SERIAL INTERFACE

EIA Standard RS232C signals provided and supported:
- Clear to Send (CTS)
- Data Set Ready (DSR)
- Data Terminal Ready (DTR)
- Request to Send (RTS)
- Receive Clock (RXC)
- Receive Data (RXD)
- Transmit Clock (DTE TXC)
- Transmit Data (TXD)

EIA Standard RS449 signals provided and supported:
- Clear to Send (CS)
- Data Mode (DM)
- Terminal Ready (TR)
- Request to Send (RS)
- Receive Timing (RT)
- Receive Data (RD)
- Terminal Timing (TT)
- Send Data (SD)

POWER REQUIREMENT

Mode	Voltage	Amps (Max.)
RS232C	+5V ±0.25V	460 mA
	+12V ±0.6V	30 mA
	−12V ±0.6V	30 mA
RS422	+5V ±0.25V	530 mA

INTERFACE CONNECTORS

Interface	No. of Pins	Pin Centers		Mating Connectors
		in.	mm	
J1 Channel	26	0.1	2.54	3M 3462-0001 (RS232C)
J1 Channel	40	0.1	2.54	3M 3464-0001 (RS449)

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0° to 55°C (32° to 131°F).

Relative Humidity: To 90% without condensation.

PHYSICAL CHARACTERISTICS

Width: 7.27 cm (2.85 inches).
Length: 9.40 cm (3.70 inches).
Height: 1.40 cm (0.56 inch) Multimodule board only.
2.82 (1.13 inches) Multimodule and iSBC board.
Weight: 51 gm (1.79 ounces).

Table 1-1. Specifications (Continued)

SERIAL COMMUNICATIONS

Synchronous:

5-, 6-, 7-, or 8-bit characters.
Internal; 1 or 2 sync characters.
Automatic sync insertion.

Asychronous:

5-, 6-, 7-, or 8-bit characters.
Break character generation and detection.
1, 1½, or 2 stop bits.
False start bit detection.

Sample Baud Rate:

8253 PIT Frequency[1] (kHz, Software Selectable)	8251 USART Baud Rate (Hz)[2]		
	Synchronous	Asynchronous	
		÷16	÷64
307.2	—	19200	4800
153.6	—	9600	2400
76.8	—	4800	1200
38.4	38400	2400	600
19.2	19200	1200	300
9.6	9600	600	150
4.8	4800	300	75
2.4	2400	150	—
1.76	1760	110	—

Notes:
1. Frequency selected by I/O writes of appropriate 16-bit frequency factor to Baud Rate Register.
2. Baud rates shown here are only a sample subset of possible software-programmable rates available. Any frequency from 18.75 Hz to 614.4 kHz may be generated utilizing on-board crystal oscillator and 16-bit Programmable Interval Timer (used here as frequency divider).

INTERVAL TIMER AND BAUD RATE GENERATOR

Input Frequency (selectable):

1.23 MHz ±0.1% (0.82 μsec period nominal), and
153.6 kHz ±0.1% (6.5 μsec period nominal).

Output Frequencies:

Reference table 3-11 for output frequencies.

CHAPTER 2
PREPARATION FOR USE

2-1. INTRODUCTION

This chapter provides instructions for installing the iSBX 351 Serial Multimodule Board onto a host iSBC microcomputer. Included are instructions on unpacking and inspection; installation considerations, such as power, cooling, mounting, and size requirements; dc characteristics; connector pin assignments; jumper configurations; and installation procedures.

2-2. UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, contact the Intel Technical Support Center to obtain a Return Authorization Number and further instructions. A purchase order will be required to complete the repair. A copy of the purchase order should be submitted to the carrier with your claim.

It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

2-3. INSTALLATION CONSIDERATIONS

The iSBX 351 Serial Multimodule Board is designed to interface with all Intel Single Board Computers that contain the I/O interface connector required for Multimodule boards. Other installation considerations such as power, cooling, mounting, and physical size requirements, are outlined in the following text.

2-4. POWER REQUIREMENT

The power requirement for the Multimodule board depends on the type of interface used. An RS232C application requires that the Multimodule board have +5V (±0.25V) at 460 mA maximum, ±12V, (±0.6V) at 30 mA maximum, and ground. An RS422 configuration requires that the Multimodule board have +5V (±0.25V) at 530 mA maximum and ground. All power is drawn from the host iSBC microcomputer via the iSBX bus connector (P1).

NOTE

If modification of the Multimodule board is required, ensure that any changes conform to the specifications for the Multimodule boards.

2-5. COOLING REQUIREMENT

The iSBX 351 Serial Multimodule Board dissipates 43.20 gram-calories/minute (0.17 BTU/minute) and adequate circulation of air must be provided to prevent a temperature rise above 55°C (131°F).

2-6. MOUNTING REQUIREMENT

Figure 2-1 shows the iSBX bus connector and spacer locations. The Multimodule board will mount onto any iSBC microcomputer containing an iSBX bus connector and mounting hole. The mounting hardware supplied as part of the Multimodule board includes:

a. 1 nylon spacer, ½" threaded, separate from the board.

b. 2 nylon screws, ¼" x 6/32, separate from the board.

c. 36-pin connector P1, factory-installed onto the board.

NOTE

The Multimodule board, when installed onto a host microcomputer, occupies an additional card slot adjacent to the host microcomputer in an iSBC 604/614 Cardcage.

2-7. PHYSICAL DIMENSIONS

Physical dimensions of the Multimodule board are as follows:

a. Width: 7.27 cm (2.85 inches).

b. Length: 9.40 cm (3.70 inches).

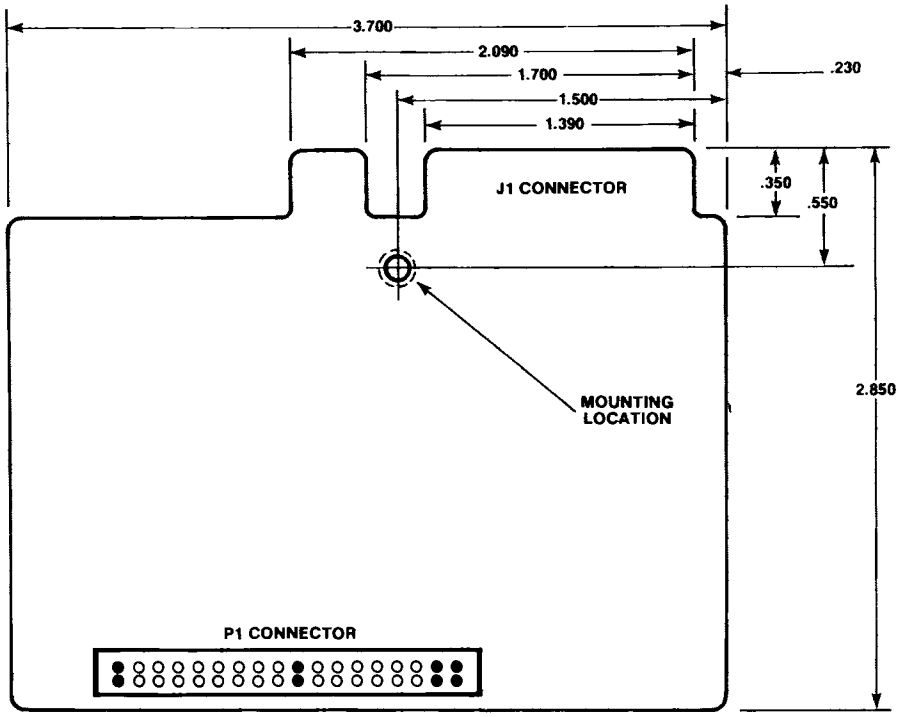


Figure 2-1. Board Dimensions (Inches)

c. Height: 1.40 cm (0.56 inch)
Multimodule board only.
2.82 cm (1.13 inches)
Multimodule with microcomputer board.

Figure 2-2 shows the clearances for a Multimodule board mounted onto a host iSBC microcomputer. Height dimensions shown are maximum.

2-8. DC INTERFACE REQUIREMENTS

The dc characteristics of the iSBX 351 Serial Multimodule Board are listed in table 2-1.

2-9. CONNECTOR CONFIGURATION

Connector P1 is the Multimodule board interface to the host iSBC microcomputer. A pin assignment for connector P1 is found in table 2-2. Edge connector J1 is the RS232C/RS449 interface for the Multimodule board. Table 2-3 contains a pin assignment listing for RS232C and RS449 applications.

CAUTION

J1 pin numbers refer to the Multimodule board edge connector only. The pin numbers on the mating connectors may not be the same.

2-10. JUMPER CONFIGURATION

The Multimodule board contains 30 jumper posts that may be user-configured independently or in pairs to perform many different functions. Table 2-4 lists some connections that perform commonly used functions and lists the "as shipped" configuration of the Multimodule board.

Table 2-4 shows some of the jumper configurations possible on the Multimodule board. For example, the OUT clock signals from the 8253 PIT may be used as the Receive or Transmit clock; used to generate interrupt requests (MINTR0, MINTR1); connected to the option lines (OPT0, OPT1) for user-defined off-board functions; or used to generate the clock signals (CLK0, CLK1) for the Multimodule board. Notice that, as the table shows, not all signals may be interfaced. Table 2-5 lists the descriptions of the signals included in table 2-4, and lists the source and/or destination of each.

Grounding. Jumpers E3 through E10 equalize any grounding differences between the power supply, chassis, signal, and data line shield. Factory configuration includes jumpers from E6 to E5, E4 to E3, and E10 to E9.

Power. Jumpers E1 and E2 are used to supply +5V (.5A maximum) signal at the RS449 connector (J1), if required by the application.

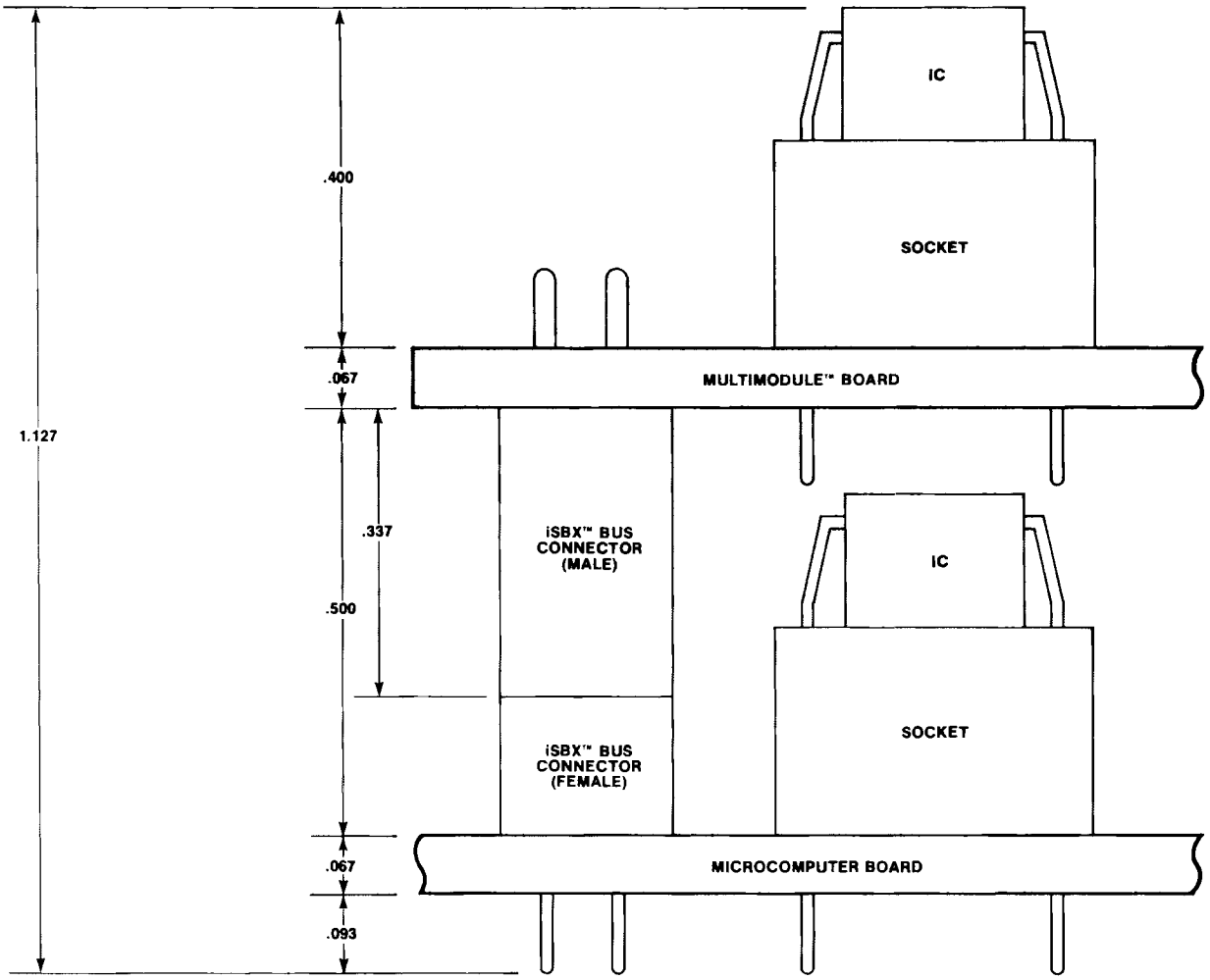


Figure 2-2. Mounting Clearances (Inches)

CAUTION

If installing a jumper between E1 and E2, ensure that the shorting plug between pins 2 and 15 at socket XU5 is removed. Failure to do so could result in damage to the equipment.

Buffer Control. Jumpers E11 through E14 are used to condition the output buffer devices during RS422 operation. Factory configuration of the jumpers includes connections from E11 to E12. By installing a jumper between E11 and E13, and removing the connection between E11 and E12, the user can configure the Multimodule board so that the DTR (Data Terminal Ready) line from the USART is connected to control the output buffer device (U2).

Buffer output control may also be accomplished by connecting one of the option lines (OPT0, OPT1) to E13. This allows the host iSBC microcomputer to control the buffer output through a line originating on the host.

The jumper between E13 and E14 connects the enable terms (pin 4 and pin 12 of U2) for the RS422 output buffer together so that both are asserted simultaneously. The iSBX 351 Serial Multimodule Board, as shipped from the factory, may contain either an MC3487 or an AM26LS31 line driver device at location U2. If the MC3487 device is used, the jumper between E13 and E14 must remain. However, if the AM26LS31 device is used, the jumper between E13 and E14 must be removed before installing the buffer control jumper between E11 and E13 or between E13 and an option line.

Timer Control. Jumpers E21 and E22 allow easy access to the gate inputs to the 8253 PIT. Some applications may require using the gate inputs for control of counters. See section 3-15.

Table 2-1. DC Specifications

Connector J1 Signal	Parameter	Test Conditions	Min.	Max	Units
RS232C Output	High Output Voltage	R_L = 3K ohms	7.7	—	V
	Low Output Voltage		-7.7	—	V
	High Short Circuit Current	V_{AA}, V_{DD} = min.	-8.0	-16.0	mA
	Low Short Circuit Current		8.0	16.0	mA
RS232C/422 Input	Input High Threshold (Differential)		—	0.5	V
	Input Low Threshold (Differential)		—	-0.5	V
	Input Current	V_{IN} = +3V	—	+1.5	mA
		V_{IN} = -3V	—	-1.5	mA
		V_{IN} = +10V	—	+3.25	mA
		V_{IN} = -10V	—	-3.25	mA
	Input Common Mode		—	±15.0	V
	Input Differential		—	±15.0	V
RS422 Output	High Out Voltage	I_{OH} = -20mA	2.5	—	V
	Low Out Voltage	I_{OL} = 20mA	—	0.5	V
	Short Circuit Current	V_{CC} = max.	-30	-150	mA
	High Output Leakage Current (Power Off)	V_{OH} = 6.0V V_{CC} = 0.0V	—	+100.00	μA
	Low Output Leakage Current (Power Off)	V_{OL} = -0.25V V_{CC} = 0.0V	—	-100.0	μA
	High or Low Output Leakage Current (High Impedance Condition)			±100.0	μA
	DTRD Current	V_{OH} = 2.0V min. V_{OL} = 0.8V max.		100.0 −2.0	μA mA
	Buffer Control Current	V_{OH} = 2.0V min. V_{OL} = 0.8V max.		20.0 −1.2	μA mA

Table 2-2. iSBX™ Bus Connector (P1) Pin Assignment

Pin	Mnemonic	Description	Pin	Mnemonic	Description
35	GND	SIGNAL GROUND	36	+5V	+5 Volts
33	MD0	MDATA BIT 0	34	—	Reserved
31	MD1	MDATA BIT 1	32	—	Reserved
29	MD2	MDATA BIT 2	30	OPT0	OPTION 0
27	MD3	MDATA BIT 3	28	OPT1	OPTION 1
25	MD4	MDATA BIT 4	26	—	Reserved
23	MD5	MDATA BIT 5	24	—	Reserved
21	MD6	MDATA BIT 6	22	MCS0/	M CHIP SELECT 0
19	MD7	MDATA BIT 7	20	MCS1/	M CHIP SELECT 1
17	GND	SIGNAL GROUND	18	+5V	+5 Volts
15	IORD/	IO READ COMMAND	16	MWAIT/	M WAIT
13	IOWRT/	IO WRITE COMMAND	14	MINTR0	M INTERRUPT 0
11	MA0	M ADDRESS 0	12	MINTR1	M INTERRUPT 1
9	MA1	M ADDRESS 1	10	—	Reserved
7	—	Reserved	8	MPST/	M PRESENT
5	RESET	RESET	6	MCLK/	M CLOCK
3	GND	SIGNAL GROUND	4	+5V	+5 Volts
1	+12V	+12 Volts	2	-12V	-12 Volts

Table 2-3. Connector J1 Pin Assignment

J1 Pin	RS232C Pin	iSBX 351™ Support	RS232 Name	RS232 Function	RS422 Pin	iSBX 351™ Support	RS449 Name	RS449 Function
1	14		(S) TXD	Secondary Transmit Data	20	YES	RC	Receive Common
2	1	YES	FG	Frame Ground	1	YES	Shield	Shield
3	15		DTE TXC	Transmit Clock	21	**	Spare	Terminal Timing (TT)
4	2	YES	TXD	Transmit Data	2		SI (I)	Signaling Rate Indicator
5	16		(S) RXD	Secondary Receive Data	22	YES	SD (N)	Send Data
6	3	YES	RXD	Receive Data	3	*	Spare (N)	Terminal Timing (TT)
7	17	YES	RXC	Receive Clock	23		ST (N)	Send Timing
8	4	YES	RTS	Request to Send	4	YES	SD (I)	Send Data
9	18		—	—	24	YES	RD (N)	Receive Data
10	5	YES	CTS	Clear to Send	5		ST (I)	Send Timing
11	19		(S) RTS	Secondary Request to Send	25	YES	RS (N)	Request to Send
12	6	YES	DSR	Data Set Ready	6	YES	RD (I)	Receive Data
13	20	YES	DTR	Data Terminal Ready	26	YES	RT (N)	Receive Timing
14	7	YES	SG	Signal Ground	7	YES	RS (I)	Request to Send
15	21		SQ	Signal Quality	27	YES	CS (N)	Clear to Send
16	8		DCD	Data Carrier Detect	8	YES	RT (I)	Receive Timing
17	22		RI	Ring Indicator	28		IS (I)	In Service
18	9		—	—	9	YES	CS (I)	Clear to Send
19	23	*	—	-12V Power	29	YES	DM (N)	Data Mode
20	10		—	—	10		LL (I)	Local Loopback
21	24	YES *	(TXC)	Ext Transmit Clock	30	YES	TR (N)	Terminal Ready
22	11	*	—	+12V Power	11	YES	DM (I)	Data Mode
23	25		—	+5V Power	31		RR (N)	Receiver Ready
24	12		(S) DCD	Secondary Data Carrier Detect	12	YES	TR (I)	Terminal Ready
25	N/C		—	—	32		SS (I)	Select Standby
26	13		(S) CTS	Secondary Clear to Send	13		RR (I)	Receiver Ready
35	N/C				37	YES	SC	Send Common
36	N/C				18		TM (I)	Test Mode
37	N/C				N/C		—	—
38	N/C				19	YES	SG	Signal Ground
39	N/C				N/C		—	—
40	N/C				N/C		—	—

NOTES:
* Non-standard usage of this line; used with TTX.
** Refer to paragraph 2-17.
(N) = Non-inverting signal.
(I) = Inverting signal.

Table 2-4. Jumper Configuration

Destination Connections	Source Connections										
	OUT0	OUT1	OUT2	1.23 MHz	156.3 KHz	Ext RxC	TxRdy	RxRdy	OPT0	OPT1	DTRS
RxC	E24-E29	E26-E29	E30-E29*	—	—	E32-E31	—	—	E25-E29	E23-E29	—
TxC	E24-E27	E26-E27	E28-E27	—	—	E32-E27	—	—	E25-E27	E23-E27	—
MINTR0	E24-E35	E26-E35	—	—	—	—	E34-E35	E36-E35	—	—	—
MINTR1	E24-E33	E26-E33	—	—	—	—	E34-E33	E36-E33	—	—	—
CLK0	—	E26-E18	E30-E18	E19-E18	E17-E18*	E32-E18	—	—	E25-E18	E23-E18	E11-E18
CLK1	E24-E20	—	E30-E20	E19-E20*	E17-E20	E32-E20	—	—	E25-E20	E23-E20	E11-E20
OPT0	E24-E25	E26-E25	E30-E25	E19-E25	E17-E25	E32-E25	E34-E25	E36-E25	—	—	E11-E25
OPT1	E24-E23	E26-E23	E30-E23	E19-E23	E17-E23	E32-E23	E34-E23	E36-E23	—	—	E11-E23
GATE0	—	—	—	—	—	—	—	—	E25-E21	E23-E21	E11-E21
GATE1	—	—	—	—	—	—	—	—	E25-E22	E23-E22	E11-E22
DEN**	—	—	—	—	—	—	—	—	E25-E13	E23-E13	E11-E13
DTRD	—	—	—	—	—	—	—	—	E25-E12	E23-E12	E11-E12*

NOTES:
** Factory default includes a jumper from E13 to E14. If DEN is to be used for controlling the output buffers in a Multidrop system, see paragraph 2-10 and Appendix A.
* Indicates default jumpers.
Each signal is described in table 2-5.

Table 2-5. Signal Description

OUT0	This signal is output on pin 10 of the PIT and may be used as an event clock.
OUT1	This signal is output on pin 13 of the PIT and may be used as an event clock.
OUT2	This signal is output on pin 17 of the PIT and may be used as an event clock.
1.23 MHz	This signal is generated on-board to clock the PIT.
156.3 KHz	This signal is generated on-board to clock the PIT.
Ext RxC	This clock output from the Multimodule board provides an external receive clock that is synchronous with the clock operating the on-board USART device.
TxRdy	This output from the USART indicates that it is ready to accept a data character for transmission.
RxRdy	This output from the USART indicates that it contains a character ready for input to the CPU.
RxC	This clock controls the rate at which a character is received into the USART.
TxC	This clock controls the rate at which a character is received into the USART.
MINTR0/MINTR1	These are the interrupt request lines and may be user-configured as required.
CLK0	This clock input to the PIT controls the frequency at which OUT0 is generated.
CLK1	This clock input to the PIT controls the frequency at which OUT1 is generated.
OPT0/OPT1	These option lines afford the user some configuration options for the application.
GATE0	This input to the PIT controls the activation of counter 0 (OUT0).
GATE1	This input to the PIT controls the activation of counter 1 (OUT1).
DTRS	(Data Terminal Ready Source) General purpose output line from USART, active low.
DTRD	(Data Terminal Ready Destination) Modem control line input to interface.
DEN	(Driver Enable) active high control line to RS422 buffers.

Teletype Power. When operating in an RS232C configuration, connect jumpers E7 and E8 to provide a ground for the iSBC 530 TTY Adapter on pin 2 of edge connector J1. If no interface to the TTY Adapter is required, E7 and E8 may be ignored.

2-11. RS232C CONFIGURATION

There are several wiring and cabling options available to the user of a Multimodule board in an RS232C (as-shipped) configuration. These options include:

- Addition of user-supplied capacitors to the Multimodule board to control rise/fall time and crosstalk.
- Rewiring of the headers located at DIP sockets XU6 and XU7 to operate the Multimodule board in one of several modes.

- Configuration of a user-supplied edge connector and flat cable for standard or non-standard RS232C applications.

The following text gives details on user-supplied capacitors and header wiring for RS232C configuration. Information on cabling for RS232C (and RS422) is contained in paragraph 2-17.

2-12. SPEED CONTROL

In the RS232C configuration, the Multimodule board includes mounting positions for optional speed control capacitors (C4 through C7), which aid in controlling rise and fall times and in reducing crosstalk. Exact values of capacitance will depend on the requirements of the application; some applications will not need these capacitors.

2-13. HEADER WIRING

Figure 2-3 shows the header wiring for the Data Terminal (as-shipped) mode of the Multimodule board. Rewiring the header allows use of the Multimodule board in a Data Set (DCE) mode, a Data Terminal (DTE) mode with loop-back, or a DTE mode without TTY Adapter power.

NOTE

When the Multimodule board is used with an Intel iSBC 530 TTY Adapter, jumper post E7 should be connected to E8 to provide a ground on pin 2 of connector J1.

The header located at XU7 may be modified to individually disable any of the power signals supplied to an iSBC 530 TTY Adapter via connector J1.

2-14. RS422 CONFIGURATION

To convert from RS232C (as-shipped) to an RS422 configuration requires only the movement of the two header blocks. In addition, there are several optional modifications that the user may perform, including:

- Addition of an optional user-supplied resistor pack (RP2) for termination of the RS422 receivers.
- Rewiring and relocation of the headers to DIP sockets XU4 and XU5 to operate the Multimodule board in one of several modes.
- Configuration of a user-supplied edge connector and flat cable for standard or non-standard RS422 applications.
- Configuration for a multidrop application.

The following text gives details on user-supplied resistor packs and header wiring for the RS422 configuration. Information on cabling for RS422 is contained in paragraph 2-17. For operation of the Multimodule board in an RS422 multidrop application, some special considerations are required, as outlined in Appendix A.

2-15. TERMINATION

In some RS422 configurations, the Multimodule board may require an optional user-supplied resistor pack (RP2) to allow proper termination of the signal lines. The resistor pack aids in controlling ringing, crosstalk, and noise pick-up. Actual resistor values are dictated by the requirements of the application, however, a 100 ohm resistance should be acceptable in most situations. Refer to the RS422 specifications for more information. Table 2-6 is a cross reference of manufacturers of compatible resistor packs. Any functional and physical equivalent may be substituted.

Table 2-6. Compatible Resistor Packs

Manufacturer	Part Number
DALE	CSP08E/SIP08A(01)-XXX
CTS	750-XXX
BOURNS	4408R-001-XXX
BECKMAN	784-1-XXX
SPRAGUE	216C-PD-XXX
MEPCO/ELECTRA	S08AZG-XXX
STACKPOLE	8-7-2-1-XXX

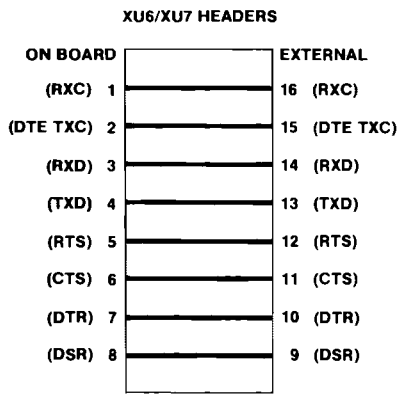
NOTE:
Part numbers specify resistor packs with .100 inch pin center spacing and .350 inch height. In most cases, the part number also specifies a resistor value and tolerance (XXX).

2-16. HEADER WIRING

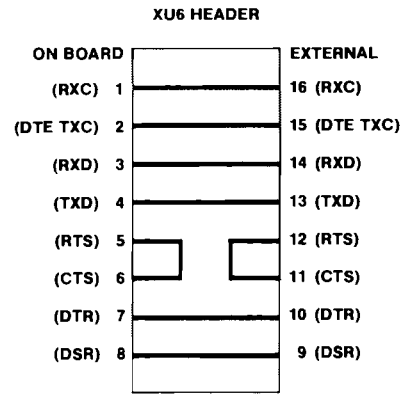
Figure 2-4 shows some header wiring options available for an RS449 configuration. The RS449 configuration requires that the two headers be located in DIP sockets XU4 and XU5, and that the two headers be wired the same; this accommodates the "A" and "B" circuit requirements of the configuration.

2-17. I/O CABLING

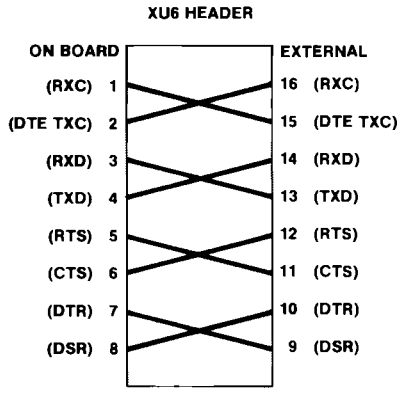
The user-supplied cabling for the Multimodule board varies slightly, according to the mode in which the board is configured. An RS232C configuration requires a 26-pin edge connector, a 25-conductor cable, and a 25-pin RS232C connector. An RS449 configuration requires a 40-pin edge connector, a 37-conductor cable, and a 37-pin RS449 connector.



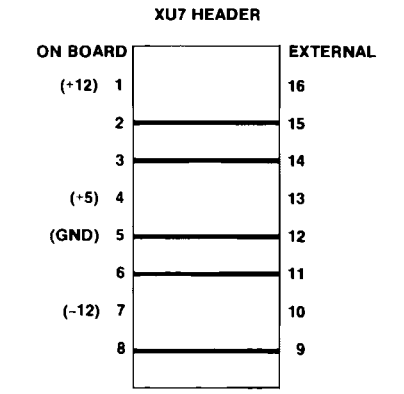
RS232C application for Data Terminal mode, configured as-shipped.



RS232C application for Data Terminal mode with the CTS-RTS Loopback. XU7 Header configured as-shipped.



RS232C application for Data Set mode. XU7 Header configured as-shipped.

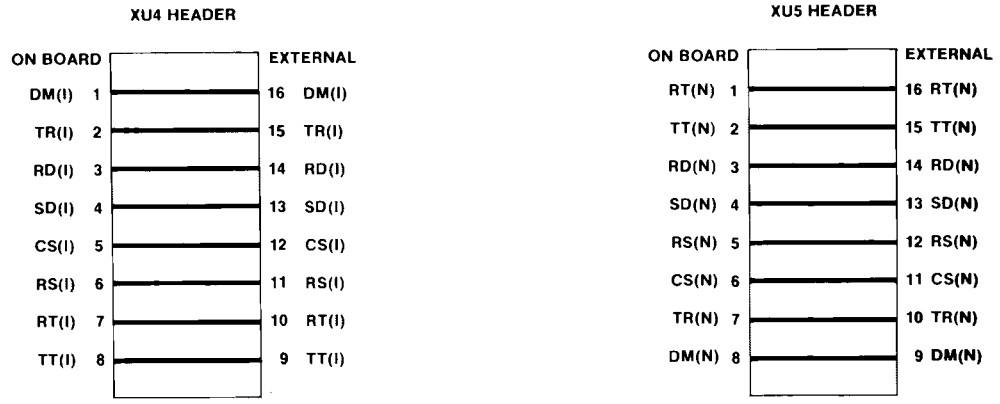


RS232C application for Data Terminal mode with TTY Adapter power disabled. XU6 Header configured as-shipped.

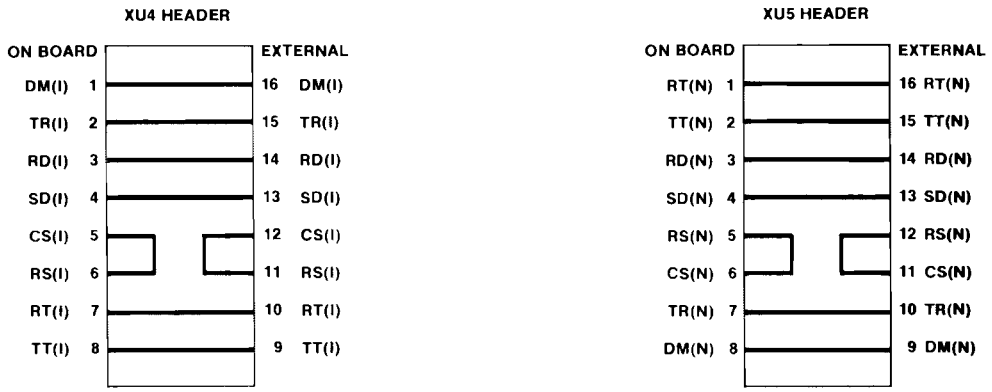
NOTE:
IN RS232C configuration, the headers (XU6 and XU7) may be wired differently to create a "combination" mode.

PSI58

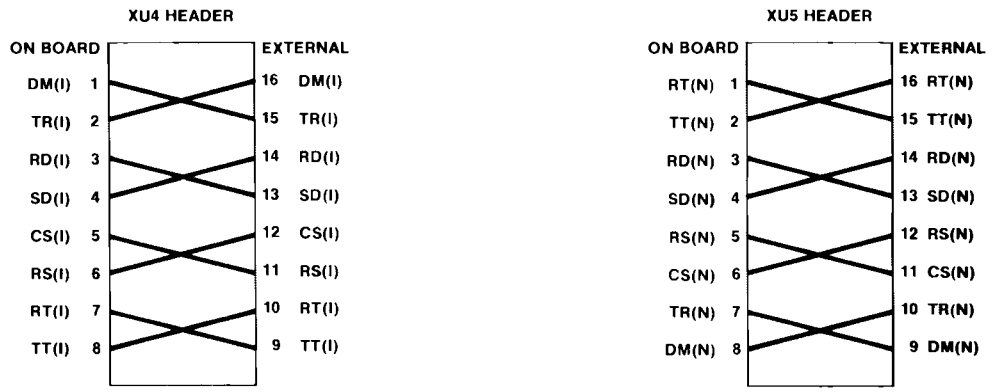
Figure 2-3. Header Wiring For RS232C



As-shipped configuration of the header, for RS422 applications in Data Terminal mode.



RS422 application for Data Terminal mode with CS-RS Loopback.



RS422 application for Data Set mode.

PS159

Note: (I) = Inverted (N) = Non-Inverted

Figure 2-4. Header Wiring For RS422

Table 2-7 lists recommended cable and connector part numbers and manufacturers. Any functionally equivalent parts may be substituted.

When assembling the RS232C cable, ensure that pin 25 of the 3M-3462 connector is *not* connected to a cable conductor, and ensure tha pin 1 of both connectors is connected together. Reference figure 2-5.

When assembling an RS449 cable, ensure that pins 37, 39, and 40 of the 3M-3464 connector are *not* connected to a cable conductor, and ensure that pin 1 of both connectors is connected together. Reference figure 2-6.

NOTE

In an RS422 configuration, the Terminal Timing (TT) signals are on non-standard pins at the Multimodule board edge connector. They may be used "as-is" or with a special user-supplied cable that converts the non-standard pin-out to standard.

Table 2-7. Cable Configuration

Configuration	Mode[2]	Multimodule Edge Connector	Cable	Connector
RS232C	DTE	26-pin[5], 3M-3462-0001	3M[3]-3349/25	25-pin[7], 3M-3482-1000
RS232C	DCE	26-pin[5], 3M-3462-0001	3M[3]-3349/25	25-pin[7], 3M-3483-1000
RS449	DTE	40-pin[6], 3M-3464-0001	3M[4]-3349/37	37-pin[1], 3M-3502-1000
RS449	DCE	40-pin[6], 3M-3464-0001	3M[4]-3349/37	37-pin[1], 3M-3503-1000

NOTES:
1. Cable housing 3M-3485-4000 may be used with the connector.
2. DTE - Data Terminal mode (male connector), DCE - Data Set mode (female connector).
3. Cable is tapered at one end to fit the 3M-3462 connector.
4. Cable is tapered to fit 3M-3464 connector.
5. Pin 26 of the edge connector is not connected to the flat cable.
6. Pins 37, 39, and 40 of the edge connector are not connected to the flat cable.
7. May be used with cable housing 3M-3485-1000.

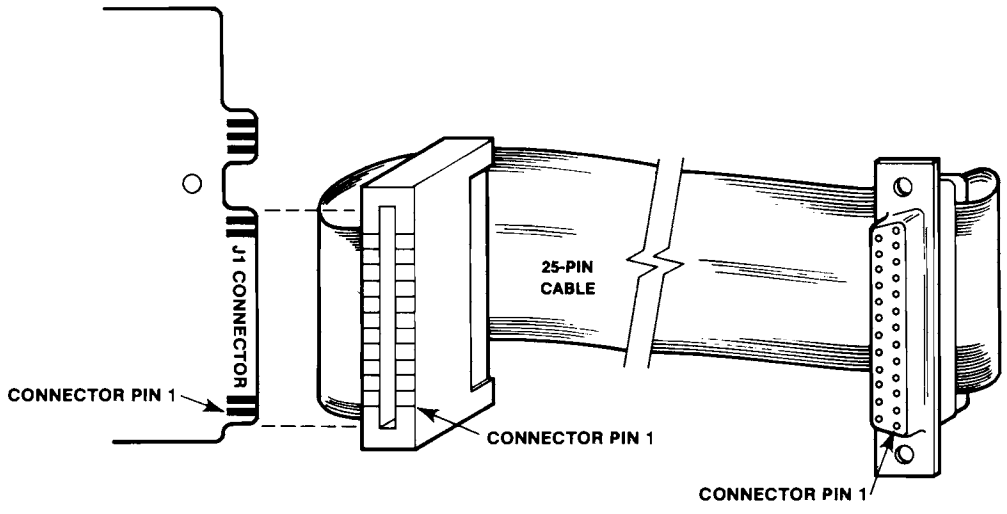


Figure 2-5. RS232C Cabling

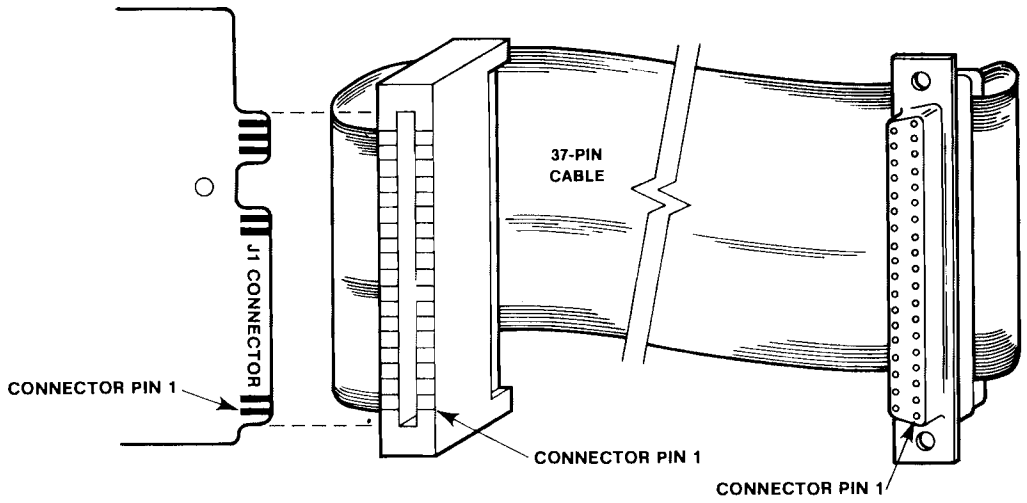


Figure 2-6. RS422/449 Cabling

2-18. INSTALLATION PROCEDURE

The iSBX 351 Serial Multimodule Board mounts onto the host iSBC microcomputer. Install the board as follows:

a. With one 6/32 screw, secure the ½ inch plastic spacer to the host iSBC microcomputer as shown in figure 2-7.

b. Locate pin 1 on the iSBX bus connector (P1) and align it with pin 1 of the iSBX bus connector on the host iSBC microcomputer.

c. Align the Multimodule board mounting hole with the spacer on the host iSBC microcomputer. Reference figure 2-1 for hole location.

d. Gently press the two boards together until the connector seats.

e. Fasten the Multimodule board to spacer with a 6/32 screw.

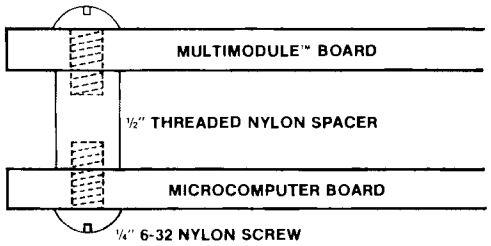


Figure 2-7. Mounting Technique

NOTE

The position of an installed Multimodule board and the host board connector number may vary according to the type of host iSBC microcomputer that is used.

CHAPTER 3
PROGRAMMING INFORMATION

3-1. INTRODUCTION

This chapter lists the programming information for the iSBX 351 Serial Multimodule Board. Included is information on I/O addressing, system initialization, 8251A USART programming and 8253 PIT programming.

More programming information for the 8251A and 8253 is located in the *MCS-85 User's Manual,* Order Number 9800366.

3-2. I/O ADDRESSING

The microprocessor on the host iSBC microcomputer communicates with the programmable chips through a sequence of I/O Read and I/O Write Commands. As shown in table 3-1, each of these chips recognizes eight separate hexadecimal I/O addresses that are used to control the various programmable functions.

Table 3-1. I/O Address Assignments

I/O Address	Chip Select	Function
X0, X2, X4, or X6	8251A USART	Write: Data Read: Data
X1, X3, X5, or X7		Write: Mode or Command Read: Status
X8 or XC	8253 PIT	Write: Counter 0 (Load Count ÷ N) Read: Counter 0
X9 or XD		Write: Counter 1 (Load Count ÷ N) Read: Counter 1
XA or XE		Write: Counter 2 (Load Count ÷ N) Read: Counter 2
XB or XF		Write: Control Read: None

NOTE: The first digit of each port I/O address is listed as "X" since it will change depending on the type of host iSBC microcomputer used. Refer to the Hardware Reference Manual for your host iSBC microcomputer to determine the first digit of the I/O address.

Where two or four hexadecimal addresses are listed for a single function, either address may be used. For example, an I/O Read Command to X1, X3, X5 or X7 will read the status of the 8251A USART.

NOTE

The Multimodule board I/O functions are not accessible to another bus master via the Multibus connectors.

3-3. SYSTEM INITIALIZATION

When power is initially applied to the system, a reset (RESET) signal is generated by the host iSBC microcomputer to "reset" the 8251A USART to an "idle" mode, waiting for a set of Initialization Words to program the desired function. The 8253 PIT is not affected by the RESET signal. Reset may also be generated under other conditions as defined by the host.

3-4. 8251A USART PROGRAMMING

The USART converts parallel output data into virtually any serial output data format (including IBM Bi-Sync) for half- or full-duplex operation. The USART also converts serial input data into parallel data format.

Prior to starting transmitting or receiving data, the USART must be loaded with a set of control words. These control words, which define the complete functional operation of the USART, must immediately follow a reset (internal or external). The control words are either a Mode instruction or a Command instruction.

3-5. MODE INSTRUCTION FORMAT

The Mode instruction word defines the general characteristics of the USART and must follow a reset operation. Once the Mode instruction word has been written into the USART, sync characters or command instructions may be inserted. The Mode instruction word defines the following:

a. For Sync Mode:
   (1) Character length
   (2) Parity enable
   (3) Even/odd parity generation and check
   (4) External sync detect (not supported by iSBX 351 board)
   (5) Single or double character sync

b. For Async Mode:
   (1) Baud rate factor (X1, X16, or X64)
   (2) Character length
   (3) Parity enable
   (4) Even/odd parity generation and check
   (5) Number of stop bits

Instruction word and data transmission formats for synchronous and asynchronous modes are shown in figures 3-1 through 3-4.

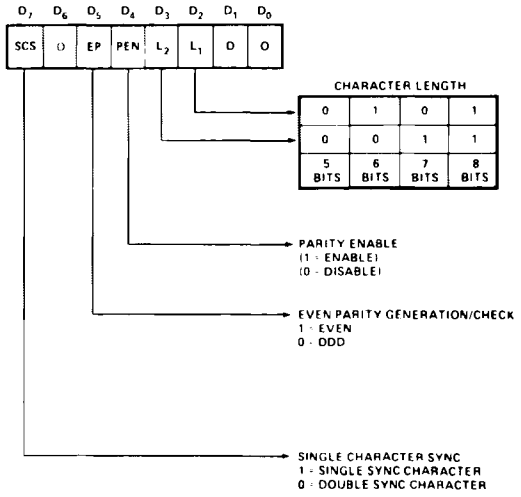


Figure 3-1. USART Synchronous Mode Instruction Word Format

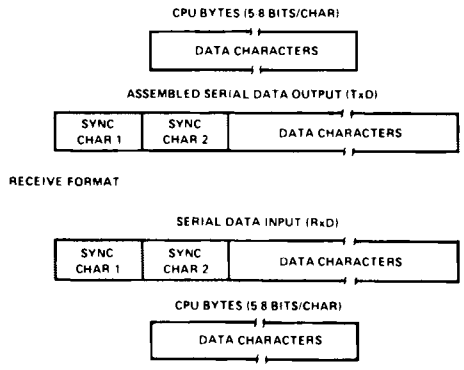


Figure 3-2. USART Synchronous Mode Transmission Format

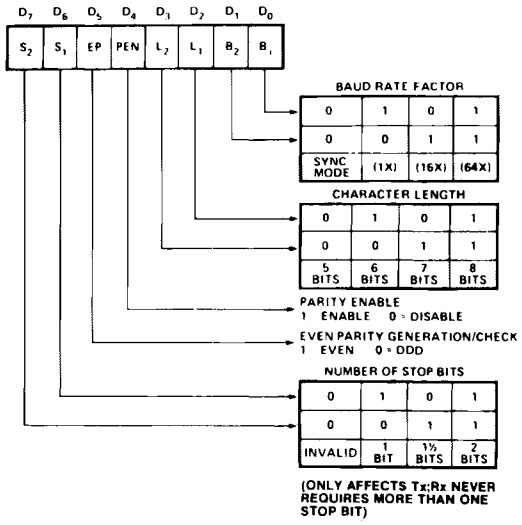


Figure 3-3. USART Asynchronous Mode Instruction Word Format

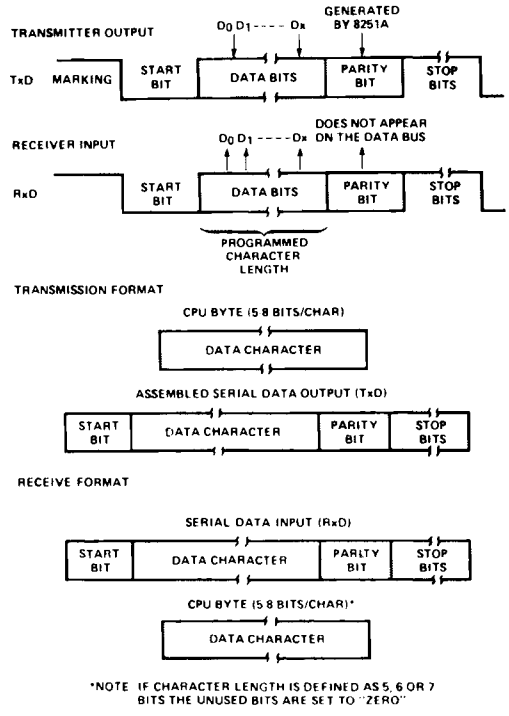


Figure 3-4. USART Asynchronous Mode Transmission Format

3-6. SYNC CHARACTERS

Sync characters are written to the USART in the synchronous mode only. The USART can be programmed for either one or two sync characters; the format of the sync characters is at the option of the programmer.

3-7. COMMAND INSTRUCTION FORMAT

The Command instruction word shown in figure 3-5 controls the operation of the addressed USART. A Command instruction must follow the mode and/or sync words and, once the Command instruction is written, data can be transmitted or received by the USART.

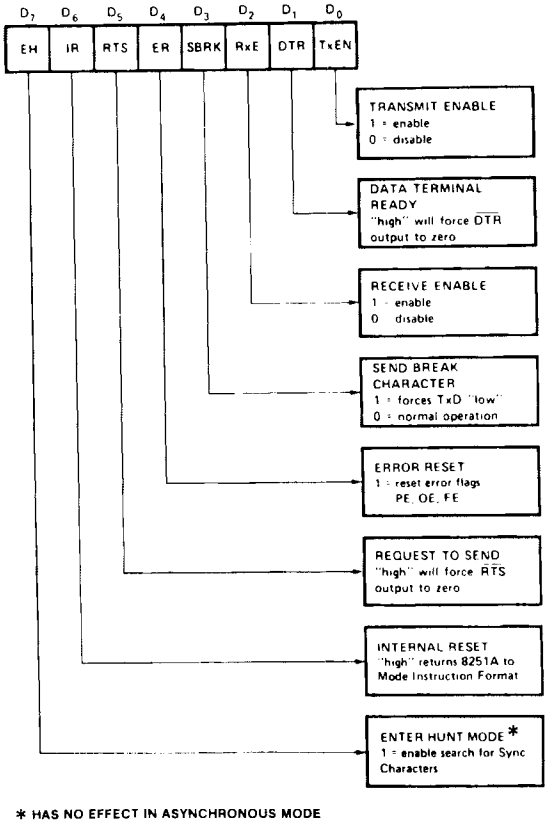


Figure 3-5. USART Command Instruction Word Format

It is not necessary for a Command instruction to precede all data transactions; only those transmissions that require a change in the Command instruction. An example is a change in the enable transmit bit or enable receive bit. Command instructions can be written to the USART at any time after one or more data operations.

After initialization, always read the chip status and check for the TXRDY bit prior to writing data words to the USART. This ensures that any prior input is not overwritten and lost. Note that issuing a Command instruciton with bit 6 (IR) set will return the USART to the Mode instruction format.

3-8. RESET

To change the Mode instruction word, the USART must receive a Reset command. The next word written to the USART after a Reset command is assumed to be a Mode instruction. Similarly, for sync mode, the next word after a Mode instruction is assumed to be one or more sync characters. All control words written into the USART after the Mode instruction (and/or the sync character) are assumed to be Command instructions.

3-9. ADDRESSING

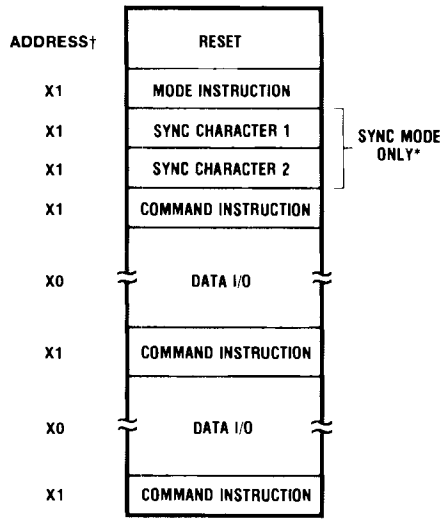
The USART chip uses four consecutive pairs of addresses. The lower of the two addresses (even) in each pair is used to read and write I/O data; the upper address (odd) in each pair is used to write mode and command words and to read the USART status. (Refer to table 3-1).

3-10. INITIALIZATION

A typical USART initialization and I/O data sequence is presented in figure 3-6. The USART chip is initialized in four steps:

a. Reset USART to Mode instruction format.

b. Write Mode instruction word. One function of mode word is to specify synchronous or asynchronous operation.



*The second sync character is skipped if Mode instruction has programmed USART to single character internal sync mode. Both sync characters are skipped if Mode instruction has programmed USART to async mode.

†Upper address (X) is determined by the host iSBC microcomputer.

611-6 **Figure 3-6. Typical USART Initialization and Data I/O Sequence**

c. If synchronous mode is selected, write one or two sync characters as required.

d. Write Command instruction word.

To avoid spurious interrupts during USART initialization, disable the USART interrupt on the host iSBC microcomputer. This can be done by either masking the appropriate interrupt request input or by disabling the CPU interrupts through execution of a DI instruction.

First, reset the USART chip by writing a Command instruction to port address X1 (or X3, X5, X7). The Command instruction must have bit 6 set (IR6 = 1); all other bits are immaterial.

NOTE

This reset procedure should be used only if the USART has been completely initialized, or if the initialization procedure has reached the point that the USART is ready to receive a Command word. For example, if the reset command is written when the initialization sequence calls for a sync character, then subsequent programming will be in error.

Next, write a Mode instruction word to the USART. (See figures 3-1 through 3-4.) A typical subroutine for writing both Mode and Command instructions is given in table 3-2.

If the USART is programmed for the synchronous mode, write one or two sync characters depending on the transmission format.

Finally, write a Command instruction word to the USART. Refer to figure 3-5 and table 3-2.

3-11. OPERATION

Normal operating procedures use data I/O read and write, status read, and Command instruction write operations. Programming and addressing procedures for the above are summarized in following paragraphs.

NOTE

After the USART has been initialized, always check the status of the TXRDY bit *prior* to writing data to the USART. The TXRDY bit *must* be *true* to prevent overwriting and subsequent loss of data words. The TXRDY bit is inactive until initialization has been completed; therefore, do not check TXRDY until after the command word, which concludes the initialization procedure, has been written.

Prior to any operating change, a new command word must be written with command bits changed as appropriate. (Refer to figure 3-5 and table 3-2.)

3-12. DATA INPUT/OUTPUT. For data receive or transmit operations perform a read or write, respectively, to the USART. Tables 3-3 and 3-4 provide examples of typical character read and write subroutines.

During normal transmit operation, the USART generates a Transmit Ready (TXRDY) signal that indicates that the USART is ready to accept a data character for transmission. TXRDY is automatically reset when the CPU loads a character into the USART.

Similarly, during normal receive operation, the USART generates a Receive Ready (RXRDY) signal that indicates that a character has been received and

Table 3-2. Typical USART Mode or Command Instruction Subroutine

```
;CMD2 OUTPUTS CONTROL WORD FROM A TO THE USART.
;USES-A, STAT; DESTROYS-NOTHING.

            PUBLIC      CMD2, INIT
            EXTRN       STAT, BASAD

CMD2;       PUSH        PSW
LP:         CALL        STAT
            ANI         1                   ;CHECK TXRDY
            JZ          LP                  ;TXRDY MUST BE TRUE
            POP         PSW
INIT:                                       ;ENTER HERE FOR INITIALIZATION (TXRDY IS NOT CHECKED).
            OUT         LOW BASAD + 1       ;OUTPUT TO COMMAND PORT (BASE ADDRESS + 1).
            RET

            END
```

Table 3-3. Typical USART Data Character Read Subroutine

```
;RX1 READS DATA CHARACTER FROM USART INTO A.
;USES-STAT; DESTROYS-A, FLAGS.

            PUBLIC      RX1, RX1A
            EXTRN       STAT, BASAD

RX1:        CALL        STAT
            ANI         2                   ;CHECK FOR RXRDY
            JZ          RX1
RX1A:                                       ;ENTER HERE IF RXRDY IS TRUE (RXRDY IS NOT CHECKED).
            IN          LOW BASAD + 0       ;INPUT FROM DATA PORT (BASE ADDRESS)
            RET

            END
```

Table 3-4. Typical USART Data Character Write Subroutine

```
;TX1 WRITES DATA CHARACTER FROM REG A TO USART.
;USES-A, STAT; DESTROYS-FLAGS.

            PUBLIC      TX1, TX1A
            EXTRN       STAT, BASAD

TX1:        PUSH        PSW                 ;SAVE DATA
TX11:       CALL        STAT
            ANI         1                   ;CHECK FOR TXRDY
            JZ          TX11
            POP         PSW
TX1A:                                       ;ENTER HERE IF TXRDY IS TRUE (TXRDY IS NOT CHECKED).
            OUT         LOW BASAD + 0       ;OUTPUT TO DATA PORT (BASE ADDRESS)
            RET

            END
```

is ready for input to the CPU. RXRDY is automatically reset when a character is read by the CPU.

The TXRDY and RXRDY outputs of the USART are available to a priority interrupt jumper matrix on the host iSBC microcomputer. If, for instance, TXRDY and RXRDY are input to an 8259A PIC, the PIC resolves the priority and drives the INTR input high to the CPU. TXRDY and RXRDY are also available in the status word. (Refer to paragraph 3-13.)

3-13. STATUS READ. The CPU can determine the status of the serial I/O port by issuing an I/O Read Command to the upper (odd) address (X1) of the USART chip. The format of the status word is shown in figure 3-7. A typical status read subroutine is given in table 3-5.

3-14. 8253 PIT PROGRAMMING

A 22.1184-MHz crystal oscillator supplies the basic clock frequency for the programmable chips. This clock frequency is divided by 18 and 144 to produce two jumper-selectable clocks: 1.2288 MHz and 153.6 KHz. These clocks are available for input to Counter 0, Counter 1, and Counter 2 of the 8253 PIT. The default (factory connected) and optional jumpers for selecting the clock inputs to the three counters are listed in table 2-4.

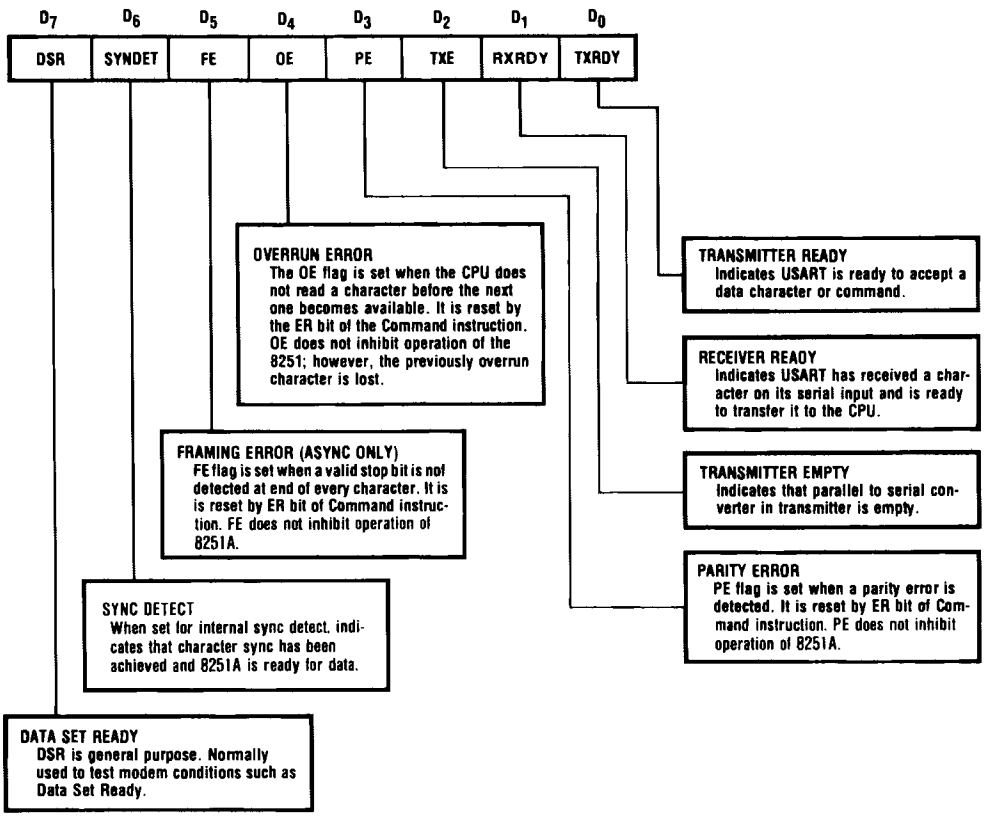
Default jumpers connect Counters 1 and 2 to the 1.2288 MHz clock and connect Counter 0 to the 153.6 KHz clock. Counter 2 generates a baud rate for the USART. Counters 0 and 1 may be cascaded or used separately to provide real-time interrupts, an event clock, or a count out clock to the host iSBC microcomputer.

Before programming the 8253 PIT, ascertain the input clock frequency and the output function of each of the three counters. These factors are determined and established by the user during the installation.

3-15. MODE CONTROL WORD AND COUNT

All three counters must be initialized separately prior to their use. The initialization for each counter consists of two steps:

a. A mode control word (figure 3-8) is written to the control register for each individual counter.



450-14

Figure 3-7. USART Status Read Format

Table 3-5. Typical USART Status Read Subroutine

```
;STAT READS STATUS FROM USART INTO A.
;USES-NOTHING; DESTROYS-A.

            PUBLIC      STAT
            EXTRN       BASAD

;STAT       IN          LOW BASAD + 1       ;GET STATUS (BASE ADDRESS + 1)
            RET

            END
```

b. A down-count number is loaded into each counter; number is in one or two 8-bit bytes as determined by mode control word.

The mode control word (figure 3-8) does the following:

a. Selects counter to be loaded.

b. Selects counter operating mode.

c. Selects one of the following four counter read/load functions:
   (1) Counter latch (for stable read operation).
   (2) Read or load most-significant byte only.
   (3) Read or load least-significant byte only.
   (4) Read or load least-significant byte first, then most-significant byte.

d. Sets counter for either binary or BCD count.

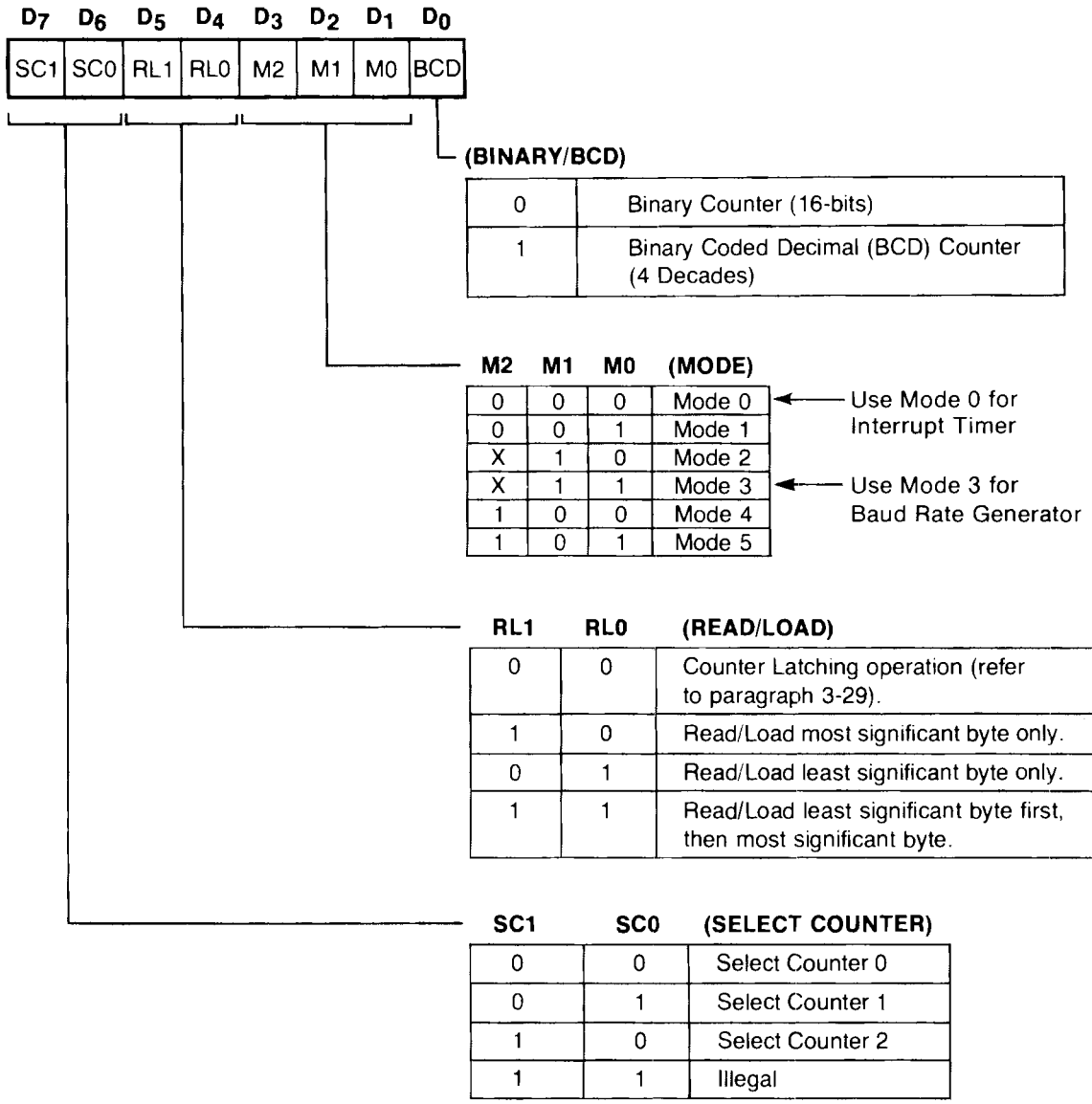
The mode control word and the count register bytes for any given counter must be entered in the following sequence:

a. Mode control word.

b. Least-significant count register byte.

c. Most-significant count register byte.

As long as the above procedure is followed *for each counter*, the chip can be programmed in any



611-7

Figure 3-8. PIT Mode Control Word Format

convenient sequence. For example, mode control words first can be loaded into each of three counters, followed by the least-significant byte, etc. Figure 3-9 shows the two programming sequences.

Since all counters in the PIT chip are downcounters, the value loaded in the count registers is decremented. Loading all zeroes into a count register results in a maximum count of 2^{16} for binary numbers or 10^4 for BCD numbers.

When a selected count register is to be loaded, it *must* be loaded with the number of bytes programmed in the mode control word. One or two bytes can be loaded, depending on the appropriate down count. These two bytes can be programmed at any time following the mode control word, as long as the correct number of bytes is loaded in order.

The count mode selected in the control word controls the counter output. As shown in figure 3-8, the PIT chip can operate in any of six modes:

a. Mode 0: Interrupt on terminal count. In this mode, Counters 0 and 1 can be used for auxiliary functions such as generating real-time interrupt intervals. After the count value is loaded into the count register, the counter output goes low and remains low until the terminal count is reached. The output then goes high until either the count register or the mode control register is reloaded.

PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter n
2	LSB	Count Register Byte Counter n
3	MSB	Count Register Byte Counter n

ALTERNATE PROGRAMMING FORMAT

Step		
1		Mode Control Word Counter 0
2		Mode Control Word Counter 1
3		Mode Control Word Counter 2
4	LSB	Counter Register Byte Counter 1
5	MSB	Count Register Byte Counter 1
6	LSB	Count Register Byte Counter 2
7	MSB	Count Register Byte Counter 2
8	LSB	Count Register Byte Counter 0
9	MSB	Count Register Byte Counter 0

450-18 **Figure 3-9. PIT Programming Sequence Examples**

b. Mode 1: Programmable one-shot. In this mode, the output of Counter 0 and/or Counter 1 will go low on the count following the rising edge of the respective GATE input. The output will go high on the terminal count. If a new count value is loaded while the output is low, it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse. The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

c. Mode 2: Rate generator. In this mode, the output of Counter 0 and/or Counter 1 will be low for one period of the clock input. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses, the present period will not be affected but the subsequent period will reflect the new value. The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter. When Mode 2 is set, the output will remain high until after the count register is loaded; thus, the count can be synchronized by software.

d. Mode 3: Square wave generator. Mode 3, which is the primary operating mode for Counter 2, is used for generating Baud rate clock signals. In this mode, the counter output remains high until one-half of the count value in the count register has been decremented (for even numbers). The output then goes low for the other half of the count. If the value in the count register is odd, the counter output is high for (N + 1)/2 counts, and low for (N - 1)/2 counts.

e. Mode 4. Software triggered strobe. After this mode is set, the output will be high. When the count is loaded, the counter begins counting. On terminal count, the output will go low for one input clock period and then go high again. If the count register is reloaded between output pulses, the present count will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the count register will restart the counting for the new value.

f. Mode 5: Hardware triggered strobe. The counter will start counting on the rising edge of the gate input and the output will go low for one clock period when the terminal count is reached. The counter is retriggerable; the output will not go low until the full count after the rising edge of the gate input.

Table 3-6 provides a summary of the counter operation versus the gate inputs. The gate inputs to Counters 0 and 1 are tied high by default jumpers; these gates may optionally be controlled by a user-defined source. The gate input to Counter 2 is tied high and not optionally controlled.

Table 3-6. PIT Counter Operation Vs. Gate Inputs

Signal Status / Modes	Low Or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output high immediately	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output high immediately	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

3-16. ADDRESSING

As listed in table 3-1, the PIT uses four consecutive I/O addresses: X8 through XB (or XC through XF). Addresses X8, X9 and XA respectively, are used in loading and reading the count in Counters 0, 1, and 2. Address XB is used in writing the mode control word to the desired counter. Again, recall that the first digit (X) of the port address is determined by the host iSBC microcomputer.

3-17. INITIALIZATION

To initialize the PIT chip, perform the following:

a. Write mode control word for Counter 0 to XB. Note that *all* mode control words are written to XB, since mode control word must specify which counter is being programmed. (Refer to figure 3-8.) Table 3-7 provides a sample subroutine for writing mode control words to all three counters.

b. Assuming mode control word has selected a 2-byte load, load least-significant byte of count into Counter 0 at X8 (Count value to be loaded is described in paragraphs 3-20 through 3-22). Table 3-8 provides a sample subroutine for loading 2-byte count value.

c. Load most-significant byte of count into Counter 0 at X8.

NOTE

Be sure to enter the downcount in two bytes if the counter was programmed for a two-byte entry in the mode control word. Similarly, enter the downcount value in BCD if the counter was so programmed.

d. Repeat steps a, b, and c for Counters 1 and 2.

3-18. OPERATION

The following paragraphs describe operating procedures for a counter read, clock frequency divider/ratio selection, and interrupt timer count selection.

3-19. COUNTER READ. There are two methods that can be used to read the contents of a particular counter. The first method involves a simple read of the desired counter. The only requirement with this method is that, in order to ensure a stable count reading, the desired counter must be *inhibited* by controlling its gate input. Only Counter 0 and Counter 1 can be read using this method because the gate input to Counter 2 is not controllable.

The second method allows the counter to be read "on-the-fly". The recommended procedure is to use a mode control word to latch the contents of the count register; this ensures that the count reading is accurate and stable. The latched value of the count can then be read.

NOTE

If a counter is read during count, it is mandatory to complete the read procedure; that is, if two bytes were programmed to the counter, then two bytes *must* be read before any other operations are performed with that counter.

To read the count of a particular counter, proceed as follows (a typical counter read subroutine is given in table 3-9):

a. Write counter register latch control word (figure 3-10) to XB. Control word specifies desired counter and selects counter latching operation.

b. Perform a read operation of desired counter; refer to table 3-1 for counter addresses.

Table 3-7. Typical PIT Control Word Subroutine

```
;INTTMR INITIALIZES COUNTERS 0, 1, 2.
;COUNTERS 0 AND 1 ARE INITIALIZED AS INTERRUPT TIMERS.
;COUNTER 2 IS INITIALIZED AS BAUD RATE GENERATOR.
;ALL THREE COUNTERS ARE SET UP FOR 16-BIT BINARY OPERATION.
;USES-NOTHING; DESTROYS-A.

            PUBLIC      INTTMR
            EXTRN       BASAD

INTTMR:     MVI         A,30H           ;MODE CONTROL WORD FOR COUNTER 0
            OUT         LOW BASAD + 0BH ;BASE ADDRESS + 11
            MVI         A,70H           ;MODE CONTROL WORD FOR COUNTER 1
            OUT         LOW BASAD + 0BH ;BASE ADDRESS + 11
            MVI         A,B6H           ;MODE CONTROL WORD FOR COUNTER 2
            OUT         LOW BASAD + 0BH ;BASE ADDRESS + 11
            RET

            END
```

Table 3-8. Typical PIT Count Value Load Subroutine

```
;LOAD0 LOADS COUNTER 0 FROM D & E, D IS MSB, E IS LSB.
;USES-D,E; DESTROYS-A.

            PUBLIC      LOAD 0
            EXTRN       BASAD

LOAD0:      MOV         A,E             ;GET LSB
            OUT         LOW BASAD + 8   ;BASE ADDRESS + 8
            MOV         A,D             ;GET MSB
            OUT         LOW BASAD + 8   ;BASE ADDRESS + 8
            RET

            END
```

Table 3-9. Typical PIT Counter Read Subroutine

```
;READ 1 READS COUNTER 1 ON-THE-FLY INTO D & E, MSB IN D, LSB IN E.
;USES-NOTHING; DESTROYS-A, D, E.

            PUBLIC      READ 1
            EXTRN       BASAD

READ1:      MVI         A,40H           ;MODE WORD FOR LATCHING COUNTER 1 VALUE
            OUT         LOW BASAD + 0BH ;BASE ADDRESS + 11
            IN          LOW BASAD + 9   ;LSB OF COUNTER, BASE ADDRESS + 9
            MOV         E,A
            IN          LOW BASAD + 9   ;MSB OF COUNTER, BASE ADDRESS + 9
            RET

            END
```

NOTE

Be sure to read one or two bytes, whichever was specified in the initialization mode control word. For two bytes, read in the order specified.

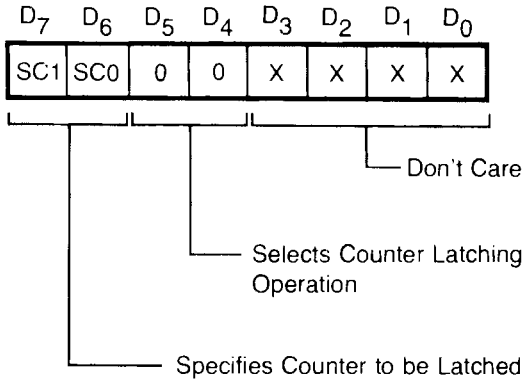


Figure 3-10. PIT Counter Register Latch Control Word Format

450-19A

3-20. CLOCK FREQUENCY/DIVIDE RATIO SELECTION. Table 1-1 lists the default and optional timer input frequencies to Counters 0 through 2. The timer input frequencies are divided by the counters to generate two interrupt outputs (Counter 0 and Counter 1), and an 8251A Baud Rate Clock (Counter 2).

Each counter must be programmed with a downcount number, or count value N. When count value N is loaded into a counter, it becomes the clock divisor. To derive N for either synchronous or asynchronous RS232C or RS422 operation, use the procedures described in following paragraphs.

3-21. SYNCHRONOUS MODE. In the synchronous mode, the TXC and/or RXC rates equal the Baud rate. Therefore the count value is determined by:

$$N = C/B$$

where N is the count value,
B is the desired Baud rate, and
C is 1.23 MHz, the input clock frequency.

Thus, for a 4800 Baud rate, the required count value (N) is:

$$N = \frac{1.23 \times 10^6}{4800} = 256.$$

If the binary equivalent of count value N = 256 is loaded into Counter 2, then the output frequency is 4800 Hz, which is the desired clock rate for synchronous mode operation.

3-22. ASYNCHRONOUS MODE. In the asynchronous mode, the TXC and/or RXC rates equal the Baud rate times one of the following multipliers: X1, X16, or X64. Therefore, the count value is determined by:

$$N = C/BM$$

where N is the count value,
B is the desired Baud rate,
M is the Baud rate multiplier (1, 16, or 64), and
C is 1.23 MHz, the input clock frequency.

Thus, for a 4800 Baud rate with M = 16, the required count value (N) is

$$N = \frac{1.23 \times 10^6}{4800 \times 16} = 16.$$

If the binary equivalent of count value N = 16 is loaded into Counter 2, then the output frequency is 4800 × 16 Hz, which is the desired clock rate for asynchronous mode operation. Count values (N) versus rate multiplier (M) for each Baud rate are listed in table 3-10.

NOTE

During initialization, be sure to load the count value (N) into the appropriate counter and the Baud rate multiplier (M) into the 8251A USART.

Table 3-10. PIT Count Value Vs. Rate Multiplier for Each Baud Rate

Baud Rate (B)	*Count Value (N) For		
	M = 1	M = 16	M = 64
75	16384	1024	256
110	11171	698	175
150	8192	512	128
300	4096	256	64
600	2048	128	32
1200	1024	64	16
2400	512	32	8
4800	256	16	4
9600	128	8	
19200	64	4	
38400	32		
64000	19		

* Count Values (N) assume clock is 1.23 MHz. Count Values (N) and Rate Multipliers (M) are in decimal.

3-23. RATE GENERATOR/INTERVAL TIMER. Table 3-11 shows the maximum and minimum rate generator frequencies and timer intervals for Counters 0 and 1 when these counters, respectively, have 1.23 MHz and 153.6 KHz clock inputs. The table also provides the maximum and minimum generator frequencies and time intervals that may be obtained by connecting Counters 0 and 1 in series.

3-24. INTERRUPT TIMER. To program an interval timer for an interruption terminal count, program the appropriate timer for the correct operating mode (Mode 0) in the control word. Reference table 3-12. Then load the count value (N), which is derived by

$$N = TC$$

where

N is the count value for Counter 0,
T is the desired interrupt time interval in seconds, and
C is the internal clock frequency (Hz).

Thus, for an interrupt time interval of 10 μsec, the required count value (N) is:

$$N = (10 \times 10^{-6})\ (1.23 \times 10^{6}) = 12$$

Table 3-12 shows the count value (N) required for several time intervals (T) that can be generated for Counters 0 and 1.

Table 3-12. PIT Timer Intervals Vs. Timer Counts

T	N*
100 μsec	123
1 msec	1229
10 msec	12288
50 msec	61440

*Count Values (N) assume clock is 1.23 MHz. Count Values (N) are in decimal.

3-25. COUNTER CASCADING. When two timers are cascaded, the first counter should be set up for mode 3. The second counter should be set up in either mode 0 (for an interrupt timer) or mode 3 (for a rate generator). The time interval obtained from the second counter alone is multiplied by the value loaded into the first counter.

3-26. COUNTER CONFIGURATION. The two counters on the Multimodule board (Counter 0 and Counter 1) are available for user-configuration to operate an off-board application. By properly configuring the OPT0, OPT1, MINTR0, or MINTR1 jumpers, you will make the OUT0, and OUT1 clock outputs available on the host iSBC microcomputer. Recall that CLK0, CLK1, GATE0, and GATE1 must be jumpered properly to allow Counter 0 and Counter 1 to begin operation.

Table 3-11. PIT Rate Generator Frequencies and Timer Intervals

	Single Timer[1] (Counter 0)		Single Timer[2] (Counter 1)		Dual Timer[3] (0 and 1 in Series)	
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum
Rate Generator (Frequency)	18.76 Hz	614.4 kHz	2.34 Hz	76.8 kHz	0.000286 Hz	307.2 kHz
Real-Time Interrupt (Interval)	1.63 μsec	53.3 msec	13.0 μsec	426.7 msec	3.26 μsec	58.25 minutes

NOTES:
1. Assuming a 1.23-MHz clock input
2. Assuming a 153.6-kHz clock input.
3. Assuming Counter 0 has 1.23-MHz clock input.

CHAPTER 4
PRINCIPLES OF OPERATION

4-1. INTRODUCTION

This chapter provides a functional description and circuit analysis of the iSBX 351 Serial Multimodule Board. The functional description includes details on the RS232C and RS422/449 communications interface signals, the interface signals between the Multimodule board and the host iSBC microcomputer, and the clock generation hardware on the Multimodule board. Figure 4-1 shows a Block Diagram of the Multimodule board.

4-2. SERIAL COMMUNICATIONS CHANNEL INTERFACE

The communications interface on the Multimodule board may be configured for either RS232C or RS422/449 operation via jumper modifications. Default wiring of the Multimodule board is for RS232C operation. To convert to RS422/449 operation, move the two 8-circuit shorting plugs from sockets XU6 and XU7 to XU4 and XU5.

CAUTION

Remove power from the Multimodule board before moving the shorting plugs. When installing the plugs, ensure that BOTH are in the correct sockets for the desired mode. Failure to observe these precautions may damage the circuits.

The serial interface provides RS232C or RS422 buffers for eight lines; Data In, Data Out, Request to Send, Clear to Send, Data Set Ready, Data Terminal Ready, Receive Clock, and DTE Transmit Clock. All necessary driver and receiver chips are supplied with the board.

NOTE

The requirement to supply both RS232C and RS449 interfaces precludes the use of standard pin connection for the RS449 Terminal Timing (TT) clock signal. The TT signal is routed through two spare pins and the standard pins are unconnected. Special user-wiring is required to move the TT signal from the spare pins to the standard pins.

4-3. iSBX™ BUS INTERFACE

The interface between the host iSBC microcomputer and the Multimodule board consists of several signals that are defined in the following paragraphs. Each signal may be found in the schematic diagram included as figure 5-2 in this manual.

RESET (Reset). This active high input signal to the 8251A USART places the USART chip into the IDLE mode until a new set of control words is written to the chip.

MA0 (Address bit 0). This active high input to the 8251A USART and to the 8253 is used in conjunction with IORD/ and IOWRT/ signals to define which register on the 8251A or the 8253 is addressed.

MA1 (Address bit 1). This active high input signal to the 8253 is used in conjunction with MA0 to select one of the counters to be operated on in the 8253 and to address the control word register for mode selection.

IORD/ (Read). This active low input to the Multimodule board performs one of two functions depending on the chip selected. When low, IORD/ informs the 8251A that the host iSBC microcomputer is reading data or status from the 8251A, and it informs the 8253 that the host iSBC microcomputer is reading the value of a counter.

IOWRT/ (Write). This active low input to the Multimodule board may perform one of two functions dependent on chip select. When low, IOWRT/ informs the 8251A that the host iSBC microcomputer is writing data or control words to the 8251A. IOWRT/ also informs the 8253 that the host iSBC microcomputer is outputting mode information or loading counters.

MCS0/ (Chip Select). This active low input to the 8251A USART enables it to perform read and write operations. When MCS0/ is high, the USART data bus is held in a float state and the IORD/ and IOWRT/ signals do not effect the USART.

MCS1/ (Chip Select). This active low input to the 8253 PIT enables it to perform read and write operations. However, MCS1/ has no effect on the operation of the internal counters in the 8253.

MD0-MD7 (Bidirectional Data Bus). These active high I/O lines are the Multimodule boards' tie-in to the host iSBC microcomputer data bus. MD0 through

MD7 transfer data, commands, and status between the Multimodule board and the host iSBC microcomputer.

MINTR0, MINTR1 (Interrupt request lines). These active high output lines may be jumpered to Out0, or Out1 on the 8253, or to TxRDY on the 8251A.

OPT0, OPT1 (Option lines). These active high I/O lines are included to give the Multimodule board greater functional flexibility. These lines may be user-defined for special functions.

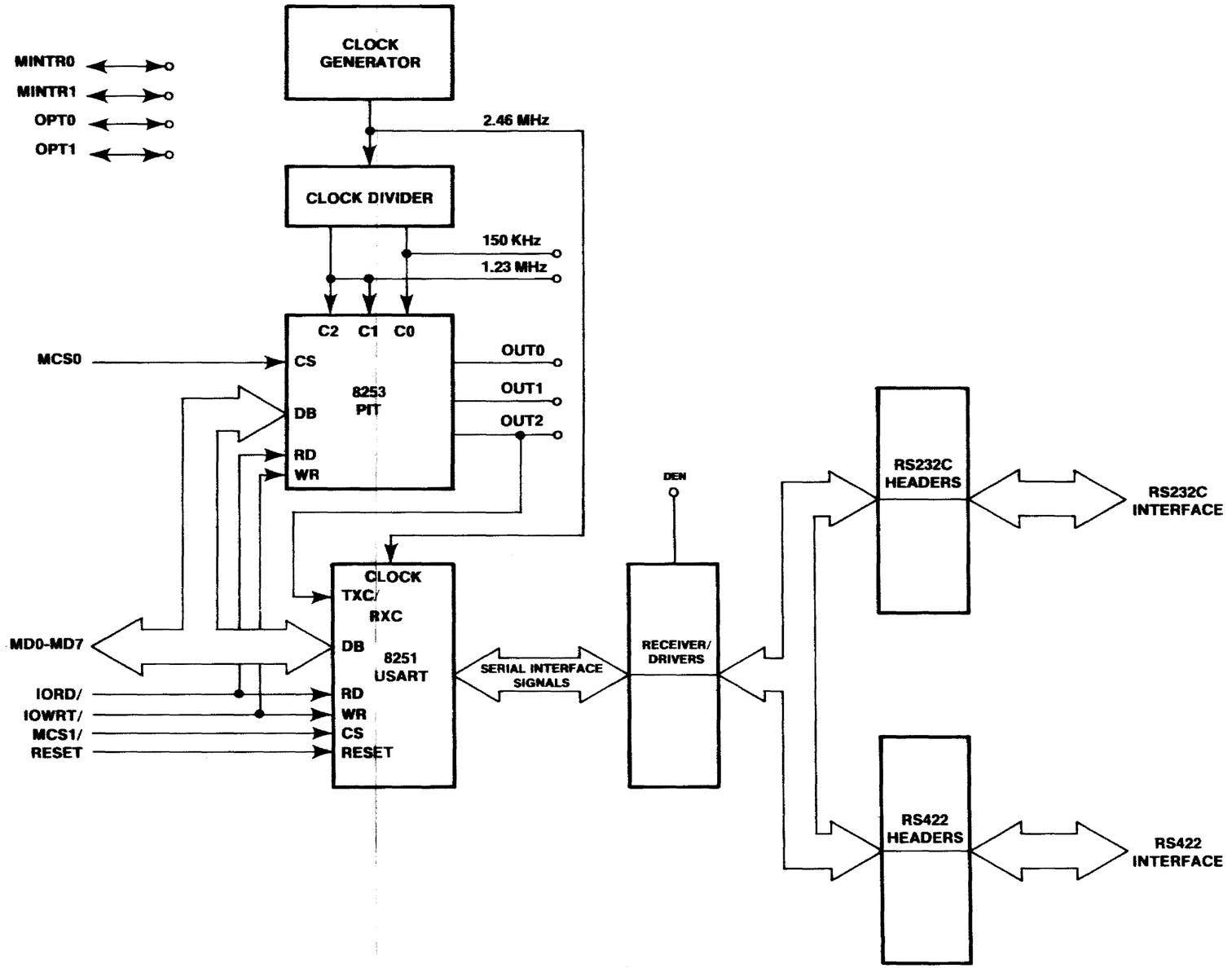
4-4. INTERFACE BUFFERING

Interface buffering is provided by logic elements U1, U2, and U3. U1 is an input buffer that may be used with either RS232C or RS422 configuration, depending on the position of the mode selection header blocks (Reference figures 2-3 and 2-4). U2 provides RS422 output buffering, and U3 provides RS232C output buffering.

4-5. CLOCK GENERATION CIRCUITRY

The Multimodule board includes an 8224 Clock Generator chip that creates a 2.46 MHz output from a 22.1148 MHz crystal input. The output is then passed through a 74LS161 Synchronous Four-Bit Counter which generates a 1.23 MHz clock and a 153.6 KHz clock to drive the 8253 PIT. The clock output frequency labeled OUT2, which is produced by the 8253 PIT, will vary according to the configuration and programming of the PIT chip. Tables 1-1 and 3-10 list some typical clock frequencies available from the 8253 and shows how those clock frequencies translate to baud rate at the 8251 USART.

The two remaining clock frequencies output from the 8253 PIT are jumper selectable to generate interrupts for the Multimodule board.



ure 4-1. iSBX 351™ Block Diagram

CHAPTER 5
SERVICE INFORMATION

5-1. INTRODUCTION

This chapter provides a list of replaceable parts, service diagrams, and service and repair assistance instructions for the iSBX 351 Serial Multimodule Board.

5-2. REPLACEABLE PARTS

Table 5-1 provides a list of replaceable parts for the Multimodule board. Table 5-2 identifies and locates the manufacturers specified in the MFR CODE column in table 5-1. Intel parts that are available on the open market are listed in the MFR CODE column as "COML"; every effort should be made to procure these parts from a local (commercial) distributor.

Table 5-2. Manufacturer Codes

Mfr. Code	Manufacturer	Location
AMD	Advanced Micro Devices	Sunnyvale, CA
CTS	CTS Corporation	Elkhart, IN
INTEL	Intel Corporation	Santa Clara, CA
TI	Texas Instruments	Dallas, TX
AMP	AMP, Incorporated	Harrisburg, PA
PEI	Pulse Engineering, Inc.	San Diego, CA
AUG	Augat, Inc.	Attelboro, MA
MOT	Motorola	Phoenix, AZ
COML	Any Commercial Source; Order by Description (OBD)	

5-3. SERVICE DIAGRAMS

The parts location diagram and schematic diagram are provided in figures 5-1 and 5-2, respectively. On the schematic diagram, a signal mnemonic that ends with a slash (e.g., MCS0/) is active low. Conversely, a signal mnemonic without a slash (e.g., OPT0) is active high.

5-4. SERVICE AND REPAIR ASSISTANCE

United States customers can obtain service and repair assistance from Intel by contacting the MCSD Technical Support Center in Santa Clara, California at one of the following numbers:

Table 5-1. Replaceable Parts

Reference Designation	Description	Mfr. Part No.	Mfr. Code	Qty.
U1	IC,3486/26LS33	MC3486P/AM26LS33	MOT/AMD	1
U2	IC,3487/26LS31	MC3487P/AM26LS31	MOT/AMD	1
U3	IC,1488, Quad RS232C Line Driver	SN75188	TI	1
U8	IC,8251A USART	8251A	INTEL	
U9	IC,8253-5 PIT	8253-5	INTEL	1
U10	IC,74LS161, Synchronous 4-bit Counter	SN74LS161A	TI	1
U11	IC,8224	8224	INTEL	1
XU4-XU7	Sockets, 16 pin, Low Profile	516-AG37D	AUG	4
RP1, RP3	Resistor Pack, 6.8k, 2%, 1.5W, 6 pin	OBD	COML	2
C1, C2, C3, C8 C9, C10, C11 C12, C14, C16	Capacitor, 0.1 μf, mono, ±80%-20%, 50V	OBD	COML	10
C13	Capacitor, 10 pf, Mica, 500V, ±5%	OBD	COML	1
C15	Capacitor, 4.7 μf, tant., 10V, ±10%	OBD	COML	1
	Shorting Block, 16 pin	PE-80005	PEI	2
P1	Connector, 36 pin, male	103109-001	INTEL	1
E3-E10 E17-E38	Post, Interconnect, Wire wrap	87022-1	AMP	30
	Shorting Plug, 2 position	530153-2	AMP	1
Y1	Crystal, 22.1148 MHz	H45	CTS	1

Telephone:

From Alaska, Arizona, or Hawaii call:
(602) 869-4600

From all other U.S. locations call toll free:
(800) 528-0595

TWX Number: 910-951-1330

Always contact the MCSD Technical Support Center before returning a product to Intel for service or repair. You will be given a "Repair Authorization Number", shipping instructions, and other important information which will help Intel provide you with fast, efficient service. If the product is being returned because of damage sustained during shipment from Intel, or if the product is out of warranty, a purchase order is necessary in order for the MCSD Technical Support Center to initiate the repair.

In preparing the product for shipment to the MCSD Technical Support Center, use the original factory packaging material, if available. If the original packaging is not available, wrap the product in a cushioning material such as Air Cap TH-240 (or equivalent) manufactured by the Sealed Air Corporation, Hawthorne, N.J., and enclose in a heavy-duty corrugated shipping carton. Seal the carton securely, mark it "FRAGILE" to ensure careful handling, and ship it to the address specified by MCSD Technical Support Center personnel.

NOTE

Customers outside of the United States should contact their sales source (Intel Sales Office or Authorized Intel Distributor) for directions on obtaining service or repair assistance.

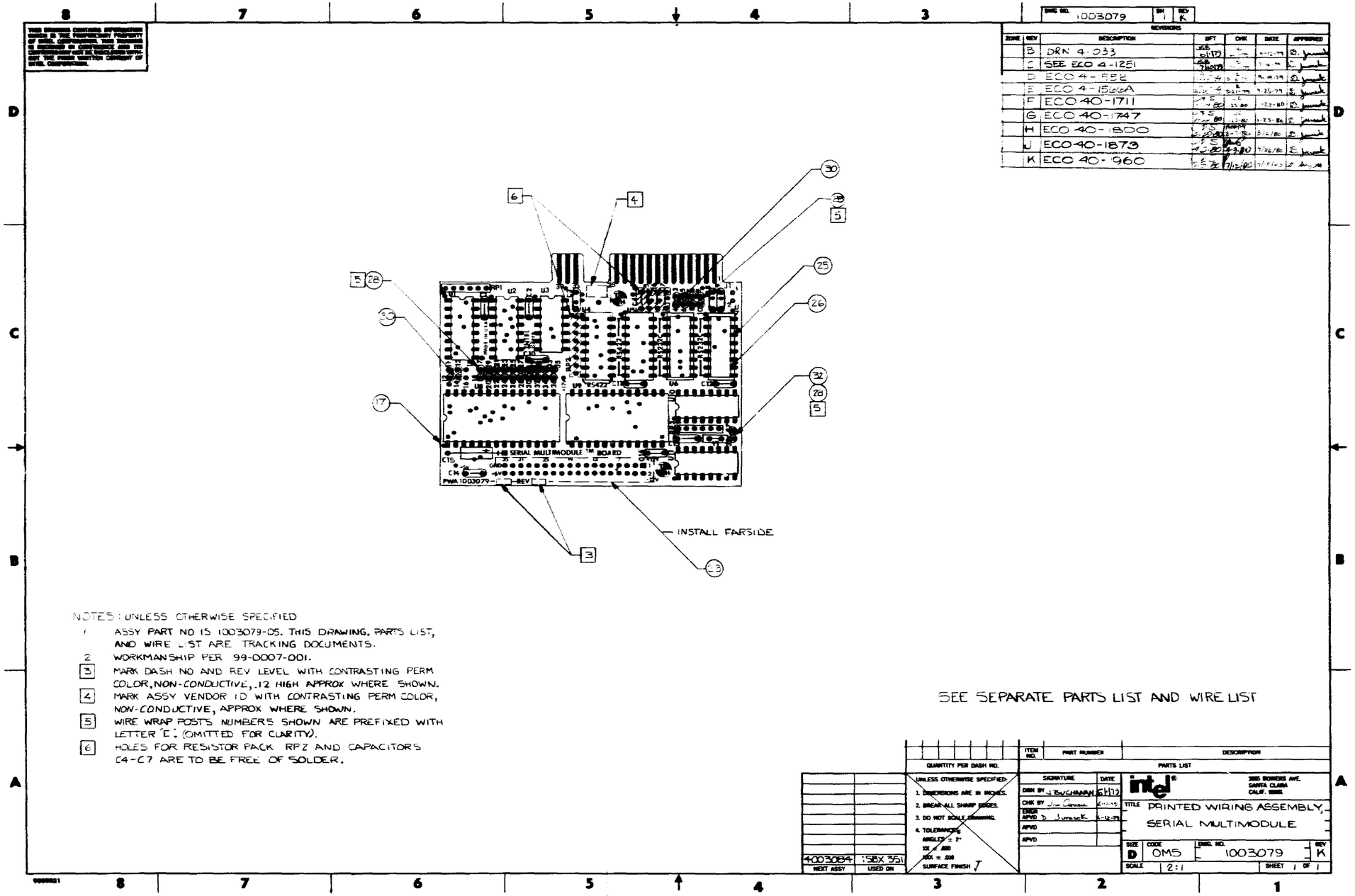


Figure 5-1. iSBX 351™ Serial Multimodule™ Parts Location Diagram

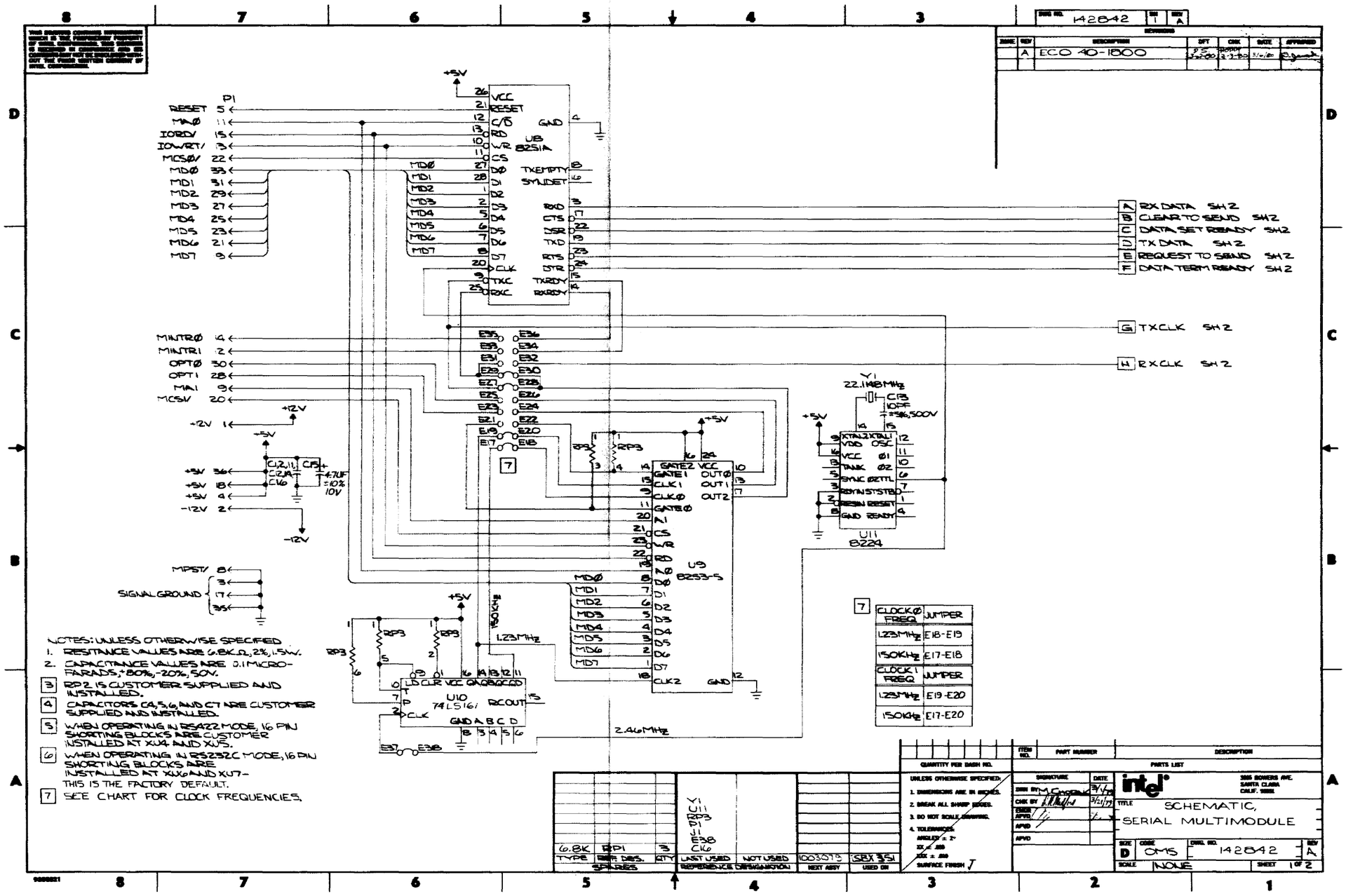


Figure 5-2. iSBX 351™ Serial Multimodule™ Schematic Diagram (Sheet 1 of 2)

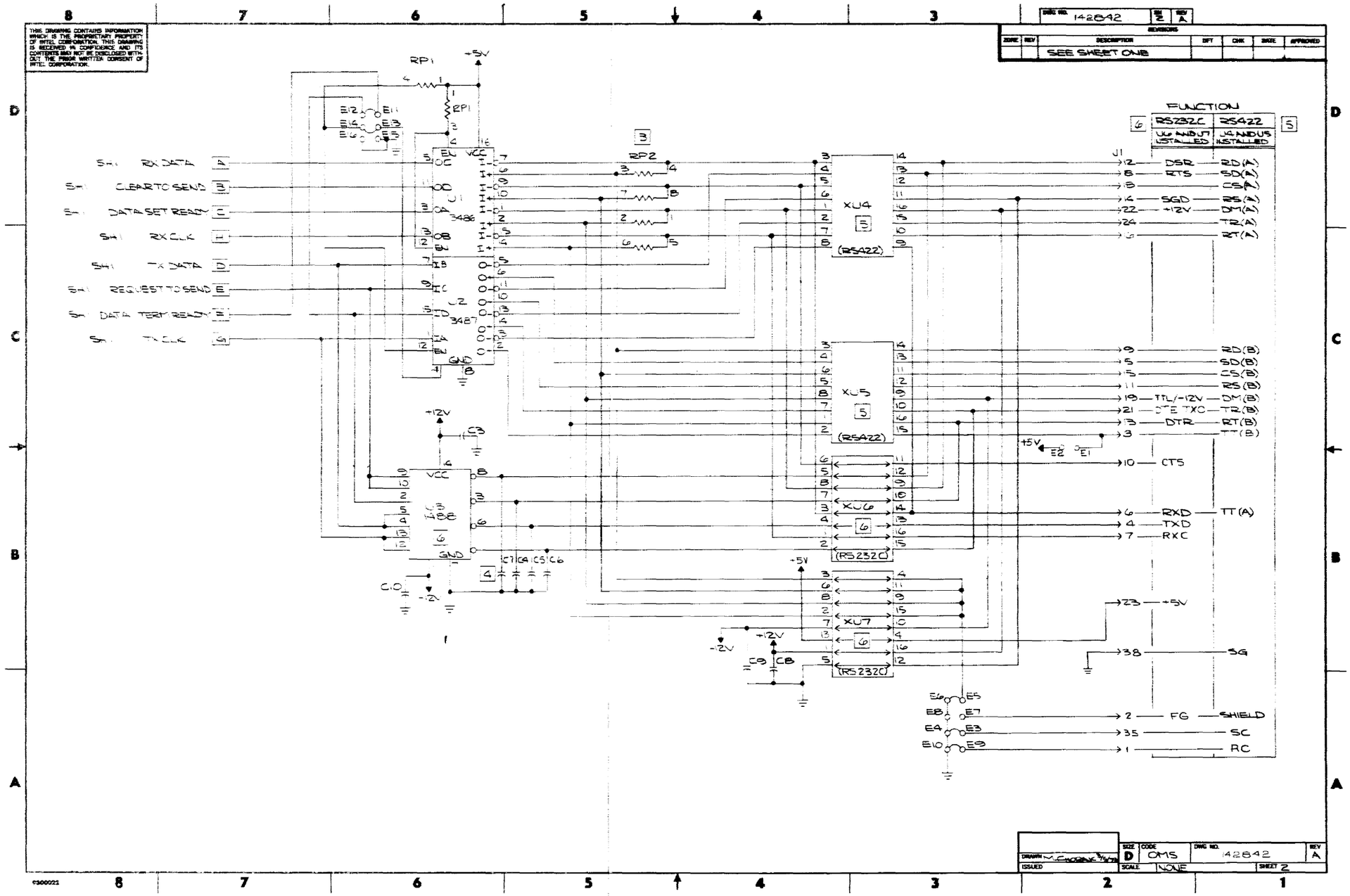


Figure 5-2. iSBX 351™ Serial Multimodule™ Schematic Diagram (Sheet 2 of 2)

APPENDIX A
MULTIDROP CONSIDERATIONS

A-1. INTRODUCTION

An iSBX 351 Serial Multimodule Board lends itself readily to a multidrop application. This appendix shows a full-duplex RS422 multidrop application with details on configuration of the Multimodule board. Some of the considerations for configuring a multidrop system are listed in the following text.

a. The hardware must be set up via jumpers to allow program control of the enable/disable signal (DEN) for the output buffers.

b. The header plugs (XU4 and XU5) must be configured for a full-duplex RS422 multidrop application.

c. Termination resistor values must be calculated for the system.

e. The output buffer current requirement must be calculated to ensure that the current draw will not damage the components.

f. The USART communication protocol must be defined by the user for both the master and the slave units.

Each of these considerations will be discussed in detail in the following text. Figure A-1 shows a block diagram of the configuration that will be used as an example for explanation purposes. Each of the blocks labeled "slave" and "master" is shown in greater detail in figures A-2 and A-3.

Figure A-1 shows a typical RS422 full-duplex multidrop configuration that assumes only one master station is attached to the system and always drives the output lines. Bear in mind that a full-duplex system allows all slaves to listen to the data line, and to perform some task in parallel with a task performed by another slave, however, only the selected slave may transmit to the master. In this example, there may be any number (n) of slave stations attached, however, the slaves are under strict program control to output only on command from the master.

A simpler RS422 multidrop system can be configured for half-duplex operation, however, the protocol is more strict. A half-duplex configuration requires two data lines to carry a differential signal and a ground line (return) between the master and all slaves in the system. Recall, however, that a half-duplex system is limited to communication in only one direction at a time. For all practical purposes, this system allows no priority for masters and slaves; all units may listen to whomever is using the data line. The system software protocol for half-duplex operation must be designed to allow only one unit to transmit at any given instant.

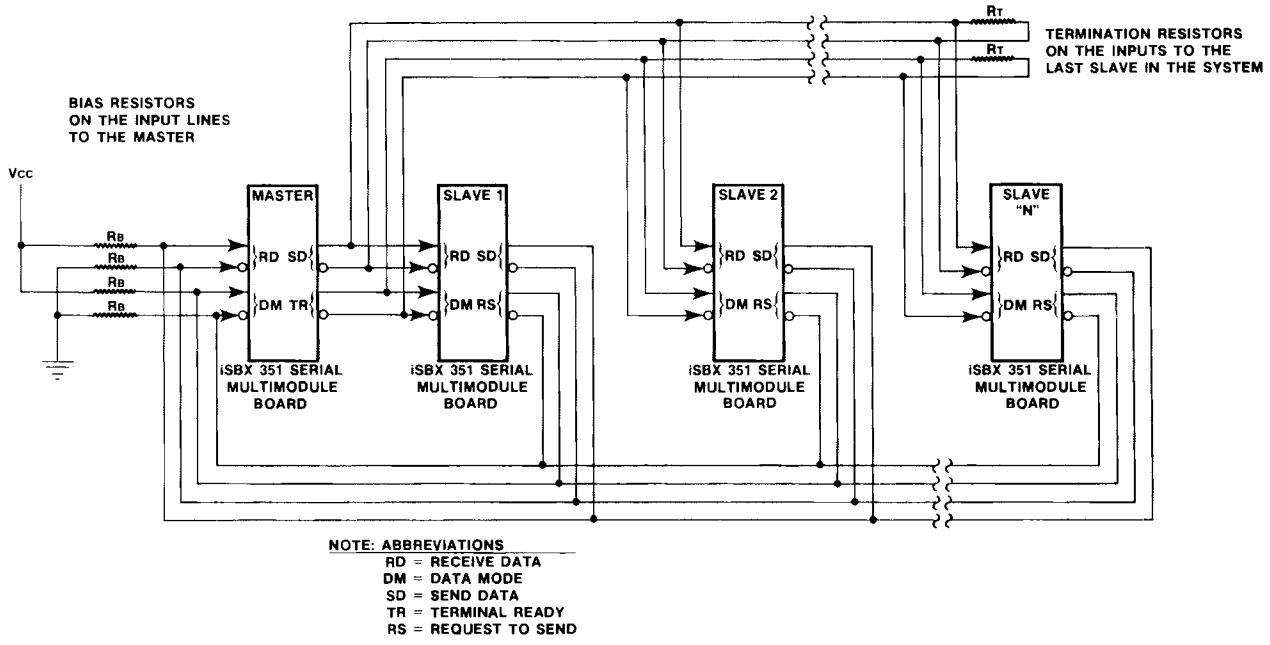


Figure A-1. Full-duplex RS422 Multidrop Configuration Block Diagram

A-2. JUMPER CONFIGURATION

Figures A-2 and A-3 shows the jumper configuration required in the master and slave to configure for an RS422 multidrop application. Factory configuration of the Multimodule board includes jumpers on the master from E11 to E12. By removing it and installing one from E11 to E13, the user can configure a slave Multimodule board so that the DTR (Data Terminal Ready) line from the slave USART controls the output buffer (U2).

A-3. HEADER WIRING

In this example, each Multimodule board contains two header blocks, in locations XU4 and XU5, that must be wired properly. Figures A-5 and A-6 show the header wiring required for the master and slave units to perform the functions shown in figure A-1. More information on header block wiring may be found in Chapter 2 of the text.

NOTE

As shown in figure A-1, a simple cross-over is performed in the external wiring with the Receive Data (RD) input to the master and the Send Data (SD) output from the slave. Another is performed between the Data Mode (DM) input to the master and to Request to Send (RS) output from the slave.

A-4. MULTIDROP BIAS RESISTOR REQUIREMENT

With an RS422 multidrop application, it is strongly recommended that the open or floating data lines in the system be biased by means of user supplied bias resistors, as shown in figure A-1. Without the resistors, the state of a floating line cannot be guaranteed. The exact value of the bias resistors may be calculated only on an individual application basis since the controlling parameters will vary from one application to another. The following procedure steps through an example for calculating bias resistance in a full-duplex RS422 multidrop application.

To calculate the size of the bias resistors (R_B) for the example shown in figure A-1, proceed as follows:

a. Determine the necessary output buffer specification (from table 2-1) for RS422 mode.

V_{OL} = 0.5V @ I_{OL} = 20 mA

V_{OH} = 2.5V @ I_{OH} = −20 mA

Input Current = 1.5 mA

Leakage Current = 100 μA

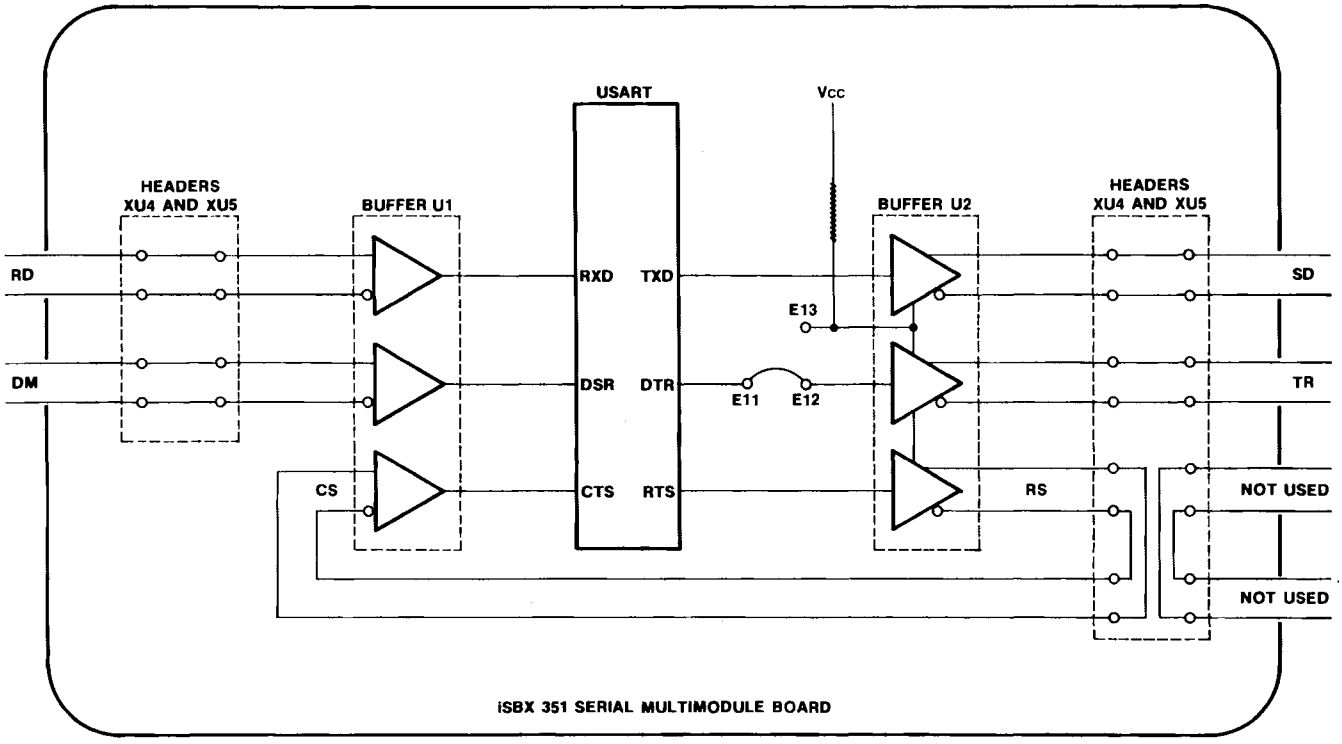


Figure A-2. Master Configuration Detail

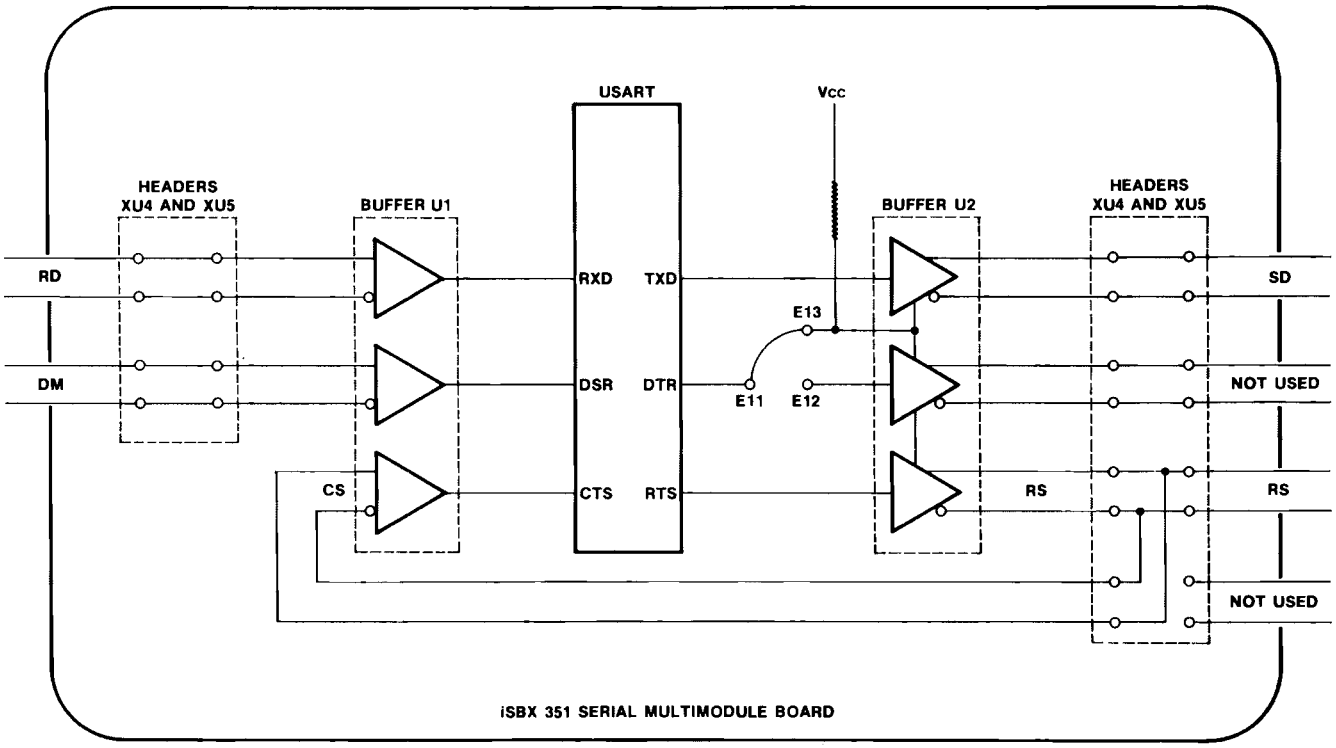


Figure A-3. Slave Configuration Detail

b. As an example to calculate the bias resistance (R_B), assume that the system being configured contains four slaves as shown in figure A-4.

c. Calculate R_B as follows:

1) Voltage at R_{B1} is

$$V_{R1} = V_{CC} - V_{OL}$$
$$= 5.0 - 0.5$$
$$= 4.5 \text{ Volts}$$
$$V_{R2} = V_{OH}$$
$$= 2.5 \text{ Volts}$$

2) Current drawn by the receivers (I_R) is

$$I_R = 1.5 \text{ mA} + 1.5 \text{ mA} + 1.5 \text{ mA} + 1.5 \text{ mA} + 1.5 \text{ mA}$$
$$I_R = 7.5 \text{ mA}$$

The leakage current (I_L) drawn by the drivers on the inactive (high impedance) slaves must also be included.

$$I_T = I_R + I_L$$
$$= 7.5 \text{ mA} + (0.1 \text{ mA} + 0.1 \text{ mA} + 0.1 \text{ mA})$$
$$I_T = 7.8 \text{ mA current draw}$$

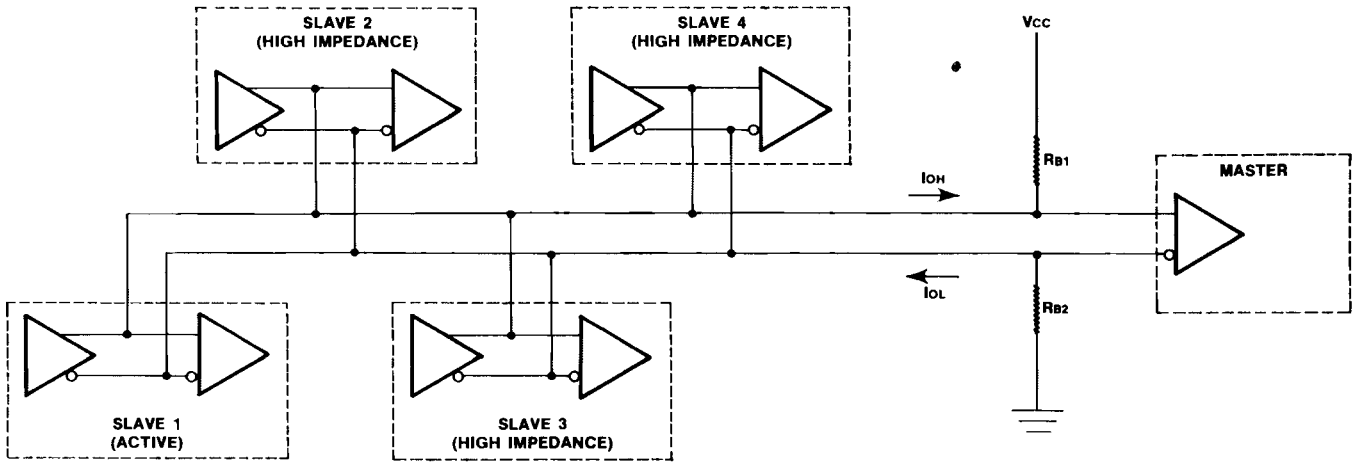


Figure A-4. System Example — Bias Resistance

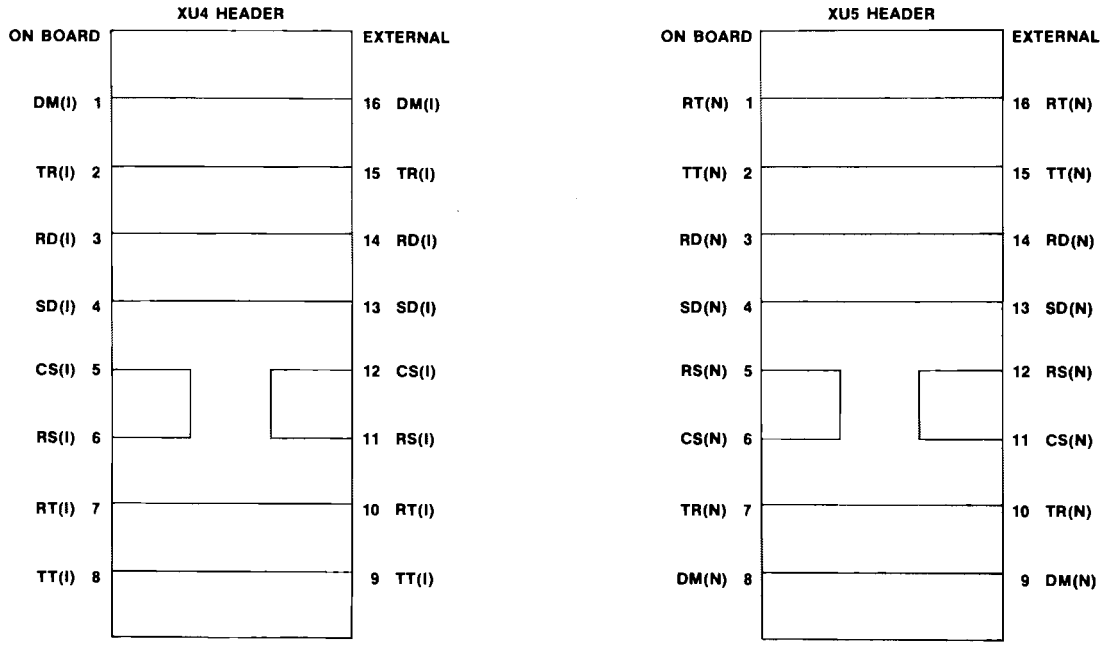


Figure A-5. Master Header Wiring Diagram

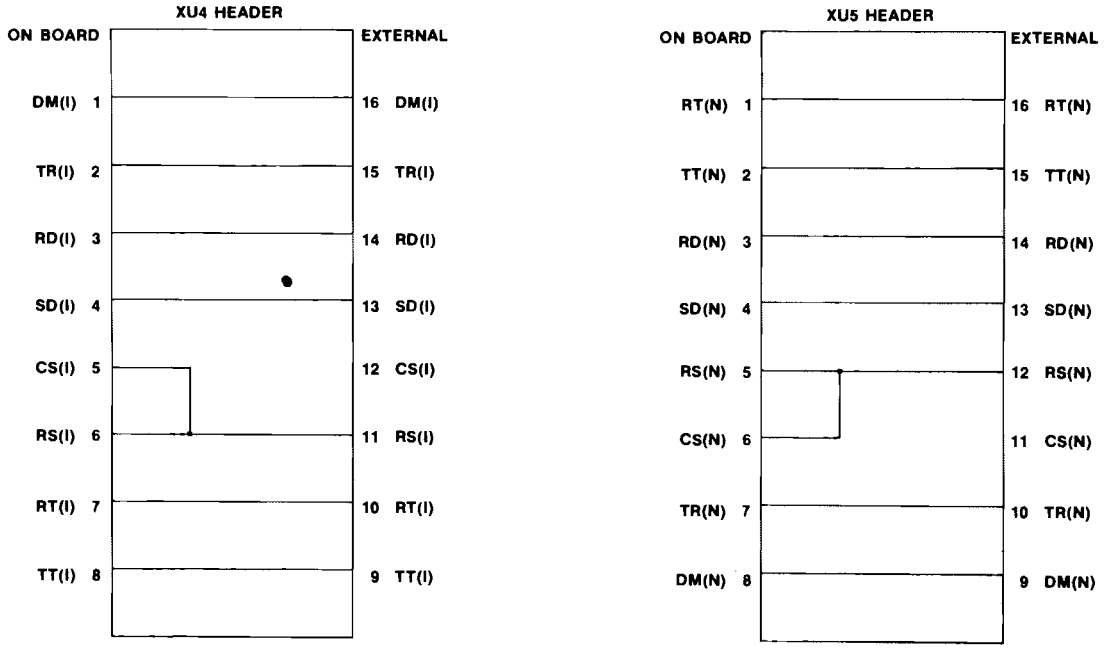


Figure A-6. Slave Header Wiring Diagram

3) Current available at the bias resistors (I_B) is

$$I_B = I_{OH} - I_T$$
$$= 20\ mA - 7.8\ mA$$
$$I_B = 12.2\ mA$$

4) Resistance (R_B) needed to satisfy I_B is

$$R_{B1} = \frac{V_{R1}}{I_B}$$
$$= \frac{4.5}{.0122}$$
$$R_{B1} = 370 \text{ ohms (minimum)}$$

and $$R_{B2} = \frac{V_{R2}}{I_B}$$
$$= \frac{2.5}{.0122}$$
$$R_{B2} = 205 \text{ ohms (minimum)}$$

A-5. MULTIDROP TERMINATION REQUIREMENT

With an RS422 multidrop application, it is strongly recommended that the inputs to the slaves be terminated as shown in figure A-1 to reduce the line reflection. The exact value of the termination resistors can be calculated only on an individual application basis since the contributing parameters will vary from one application to another. The following text shows an example of how to calculate termination resistance for a full-duplex RS422 multidrop application.

To calculate the size of the termination resistors (R_T) for the example in figure A-1, assume the following:

a. Determine the necessary output buffer specifications (available in table 2-1) for RS422 mode.

V_{OL} = 0.5V @ I_{OL} = 20 mA
V_{OH} = 2.5V @ I_{OH} = −20 mA

Input Current = 1.5 mA
Leakage Current = 100 μA

b. As an example to calculate the termination resistance (R_T), assume that the system being configured contains four slaves, as shown in figure A-7.

c. Calculate R_T as follows:

1) Voltage at R_T is

$$V_T = V_{OH} - V_{OL}$$
$$= 2.5 - 0.5$$
$$= 2.0 \text{ Volts differential}$$

2) Current drawn by the slaves is

$$I_S = 1.5\ mA + 1.5\ mA + 1.5\ mA + 1.5\ mA$$
$$I_S = 6.0\ mA$$

3) Excess current available at R_T is

$$I_E = 20\ mA - I_S$$
$$= 20\ mA - 6\ mA$$
$$I_E = 14\ mA \text{ excess current}$$

4) Resistance (R_T) needed to terminate I_E is

$$R_T = \frac{V_T}{I_E}$$
$$= \frac{2.0V}{.014A}$$
$$R_T = 143 \text{ ohms (minimum) termination resistance.}$$

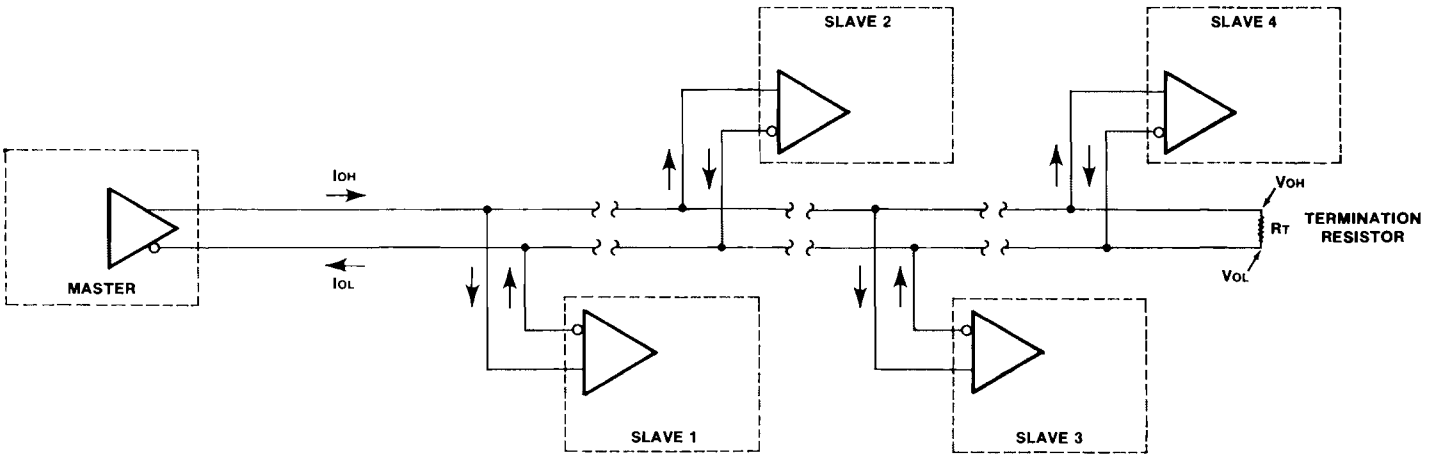


Figure A-7. System Example — Termination Resistance

A-6. MULTIDROP OUTPUT BUFFER CURRENT REQUIREMENT

In a multidrop application, special attention must be given to the current requirement put on the output buffer device at U2. The user must calculate the sum of the current required by all of the receivers attached to the line, the current required by the termination resistors, and the current required by any other devices on the line. This sum must not exceed the maximum drive current available from the output buffers on the Multimodule board.

As shipped from the factory, the Multimodule board may contain either an MC3487 or an AM26LS31 line driver device at location U2. The current drive limitations for each of these devices is as follows:

V_{OL} = 0.5 volts @ I_{OL} = 20 mA

V_{OH} = 2.5 volts @ I_{OH} = −20 mA

Input Current = 1.5 mA

Leakage Current = 0.1 mA

NOTE

The configuration for jumper E13 to E14 will vary depending on the type of output buffer device used at U2 on the Multimodule board.

A-7. PROGRAMMING CONSIDERATIONS

Most programming for the Multimodule boards in an RS422 multidrop application revolves around the operation and use of the USART device. Programming for the USART is detailed in Chapter 3, and some specific points that may be useful in configuring a multidrop system are included in the following text.

A-8. SYSTEM INITIALIZATION

When the USART on a slave Multimodule board is reset (i.e., power on), the DTR (Data Terminal Ready) line is reset, enabling the output buffers for that slave. This could cause a data-line contention problem among the slaves in the system. To alleviate the possiblity of contention, it is strongly recommended that the user software initialize the slaves immediately after power-up, by raising DTR in the slave to disable all outputs. Table A-1 shows a typical slave initialization subroutine.

A-9. SLAVE SELECTION

When DTR is pulled LOW by the master, the slave senses a DSR (Data Set Ready) signal and reinitializes its protocol. DTR provides a means for the master to reinitialize all slaves to a known state. After receiving the DTR signal, all slaves are off-line, but listening to the master. When the master transmits an address, a specific slave is allowed on-line to communicate. The address of each slave must be unique to that slave and must be verified by the software in that slave. After a slave decodes its address, it turns OFF the DTR line to enable the output buffers. The slave then generates RTS (Request to Send) to the master to inform that the slave is indeed on-line. Figures A-2 and A-3 show that the RTS signal from the slave also generates CTS (Clear to Send) to fully enable the slave for output.

A-10. SLAVE STATUS TEST

The master can sense the state of the slave at any time by reading the DM (Data Mode) line from the slave. DM is available in the master in the form of the DSR status bit from the masters' USART status register. The DSR bit, bit 7 of the Status Read Word, is defined as follows:

DSR = 1 a slave is on-line, and driving its RS (Request to Send) line.

DSR = 0 all slaves are off-line.

Table A-1. Slave Initialization Subroutine

```
INTSLV INITIALIZES THE SLAVE OUTPUT BUFFERS ON POWER-UP.
USES-NOTHING, DESTROYS-A.

        PUBLIC    INTSLV
        EXTERN    BASAD

INTSLV:                          ;ENTER HERE FOR SLAVE INITIALIZATION
        MVI       A, (MODE WORD) ;MOVE USART MODE WORD INTO A
        OUT       LOW BASAD + 1  ;BASE ADDRESS + 1
        MVI       A, (COMMAND WORD) ;MOVE USART COMMAND WORD, WITH BIT 1 = 1, INTO A.
        OUT       LOW BASAD + 1  ;BASE ADDRESS + 1
        RET
        END
```

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