# iSBX-251

## TECHNICAL MANUAL

112924

Revision B

November 1982



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Memory Systems Operation
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Santa Clara, California 95051

## COPYRIGHT STATEMENT

## Revisions

| REV | DESCRIPTION | DATE | APPR |
|---|---|---|---|
| | **Released** | | |
| A | Updated specifications and refined software-related information. Added jumper configuration table. | 04/82 | MB/kf |
| | Released per ECO # | 04/82 | MB/kf |
| B | Added specifications for iSBX 251C. | 11/82 | MB/pd |

# ADDITIONAL SPECIFICATIONS FOR THE iSBX 251C (113432)

The following outlines the differences between the iSBX 251C and the iSBX 251:

A. iSBX 251C Temperature Range: Operating – 10°C to 40°C
Storage – -20°C to 75°C

B. W7 – Boot Swap Enable Inhibit (iSBX 251C)
To write the bootloop W7 must be installed, without W7 no bootloop writes will take place.

C. W5, W6 – Or-ing Jumpers

With W5 in place, W6 removed, the iSBX 251C has the same interrupt jumper configurations as the iSBX 251.

With W6 in place, W5 removed, the signal and the DRQ signal from the 7220 are or-ed and are on the MINTR0 line. W1 and W2 still select whether the 7220 DRQ signal is on the MDRQT or MINTR1 line.

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# CHAPTER 1
# GENERAL INFORMATION

## 1.1 INTRODUCTION

The iSBX-251 Magnetic Bubble Memory Multimodule Board (here after called the iSBX-251 board) is a member of Intel's growing line of expansion Multimodule boards. These boards are designed to augment boards containing an iSBX multimodule connector, such as the iSBC series of single board computers.

The iSBX bus is an interface facilitating on-board expansion with iSBX Multimodule boards. The iSBX bus is derived directly from the on-board CPU bus and, as such, an iSBX Multimodule board plugged into the iSBX bus becomes an integral element of the single board computer. The physical interface between the single board computer and the iSBX Multimodule board is a unique connector designed specifically for the iSBX bus. The iSBX bus is brought out to a female iSBX bus connector on the single board computer and mates with its male equivalent resident on the iSBX Multimodule board (Figure 1-1).

The iSBX-251 board integrates system mass storage by supplying 131,072 bytes (128K bytes) of magnetic bubble memory on one plug-in card. This chapter contains a description of the iSBX-251 board with specifications and lists the equipment supplied with the board and other compatible equipment.

## 1.2 DESCRIPTION

The iSBX-251 board is a double-wide Multimodule printed circuit board that interfaces with Intel iSBC boards equipped with iSBX connectors conforming to the iSBX Bus Specifications. Design of the board is based on the Intel 7110 Magnetic Bubble Memory chip and support circuitry and includes all the logic necessary to control the 7110 Magnetic Bubble Memory chip. The board components operate off the +5 VDC and +12 VDC supplied via the iSBX connector. The 7220 Bubble Memory Controller

chip, which controls the 7110 bubble memory chip, utilizes 16 commands for communication between the host iSBC board and the bubble memory board, making the 7110 operation transparent to the user.

The iSBX-251 board can be wired to operate in the polled access mode, generate an interrupt on request from the 7220 BMC chip, or operate in DMA mode. Interrupt priority is established on the host iSBC board.

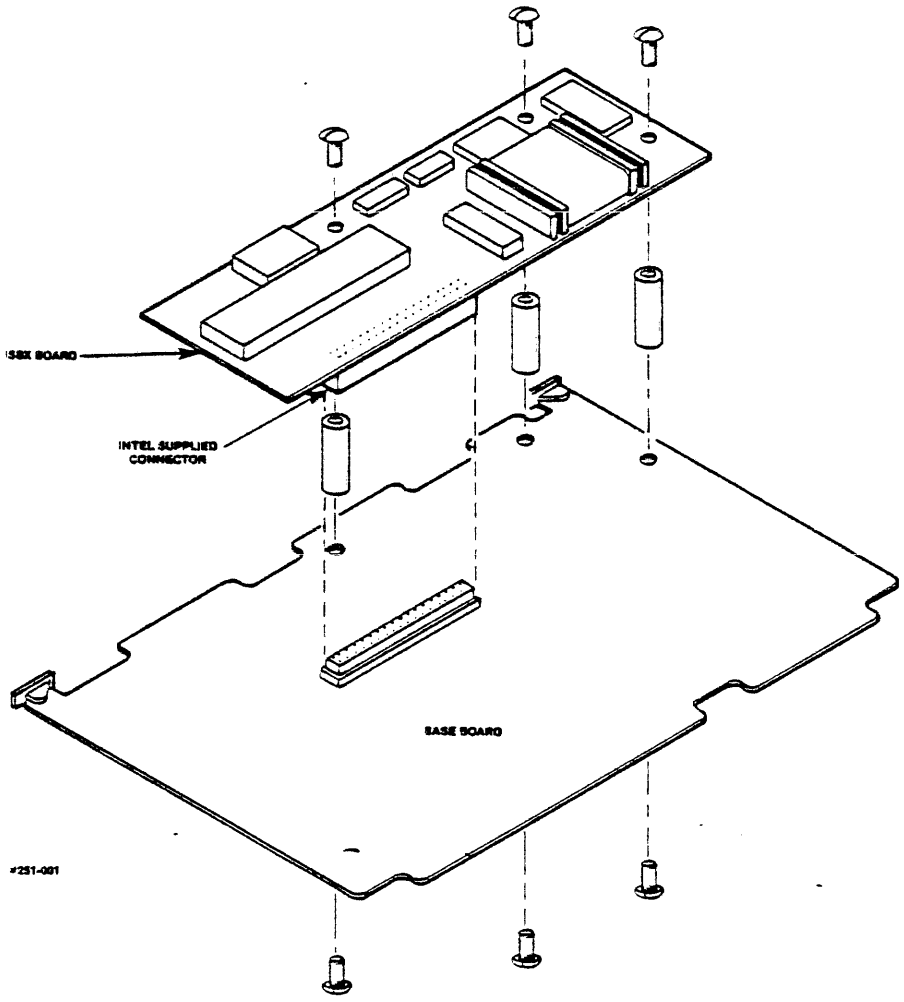


Figure 1-1. iSBX Multimodule Board Concept

## 1.3 EQUIPMENT SUPPLIED

The following equipment is supplied with the iSBX-251 board:

a. Schematic Diagram, drawing number 162795
b. 6 Screws, 1/4" 6-32 nylon.
c. 3 Spacers, 1/2" 6-32 nylon.

## 1.4 COMPATIBLE EQUIPMENT

The iSBX-251 board must be used with a host board containing an iSBX multimodule connector. Multimodule interfacing is provided through the P1 Multimodule connector on the iSBC host board.

## 1.5 SPECIFICATIONS

Specifications for the iSBX-251 board are provided in Table 1-1.

Table 1-1. iSBX-251 Board Specifications

| ITEM | DESCRIPTION |
|---|---|
| I/O ADDRESSING: | I/O addressing with one address line and one select line via the iSBX connector bus (see Chapter 2). |
| POWER REQUIREMENTS: | +5 Volts, ±.25 Volts, at 385 mA (max).<br>12 Volts, ±0.6 Volts, at 400 mA (max). |
| INTERFACE CONNECTORS: | <table><tr><th>Interface</th><th>No. of Pins</th><th colspan="2">Pin Center</th><th>Mating Connector</th></tr><tr><th></th><th></th><th>(in)</th><th>(mm)</th><th></th></tr><tr><td>iSBX P1 Connector Host Board</td><td>36</td><td>0.1</td><td>2.54</td><td>Intel 103059-001</td></tr></table> |
| ENVIRONMENTAL REQUIREMENTS: | |
| Operating Temperature | 0° C to 55° C above 80% duty cycle<br>(32° F to 131° F)<br><br>0° C to 60° up to 80% duty cycle<br>(32° F to 140° F) |
| Non-Operating Temperature | -40°C to 85°C<br>(-40°F to 185°F) |
| Air Flow | 100 linear feet per minute |
| Relative Humidity | 5% to 95% without condensation |
| PHYSICAL CHARACTERISTICS: | |
| Width | 7.24 cm (2.85 inches) |
| Length | 19.1 cm (7.50 inches) |
| Height | 1.26 cm (0.498 inches) iSBX 251 board only<br><br>3.14 cm (1.238 inches) iSBX 251 board and iSBC host board. |
| Weight | 362.9 gm (12.8 ounces) |

# CHAPTER 2

# PREPARATION FOR USE

## 2.1 INTRODUCTION

This chapter provides instructions for installing the iSBX-251 board on an iSBC single board computer or other host board equipped with an iSBX connector. Included are instructions on unpacking and inspection; installation considerations such as power, cooling, mounting and size requirements; DC characteristics; connector pin assignments; jumper configurations; and installation procedures.

## 2.2 UNPACKING AND INSPECTION

Inspect the shipping carton immediately upon receipt for evidence of mishandling during transit. If the shipping carton is severely damaged or water-stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is not present when the carton is opened and the contents are damaged, keep the carton and packing materials for the agent's inspection.

It is suggested that all salvageable shipping cartons and packing material be retained for future use in the event the product must be shipped.

## 2.3 INSTALLATION CONSIDERATIONS

The iSBX-251 board is designed to interface with Intel products that support the I/O interface connector required for the Multimodule boards.

Power and environmental requirements are given in Table 1-1.

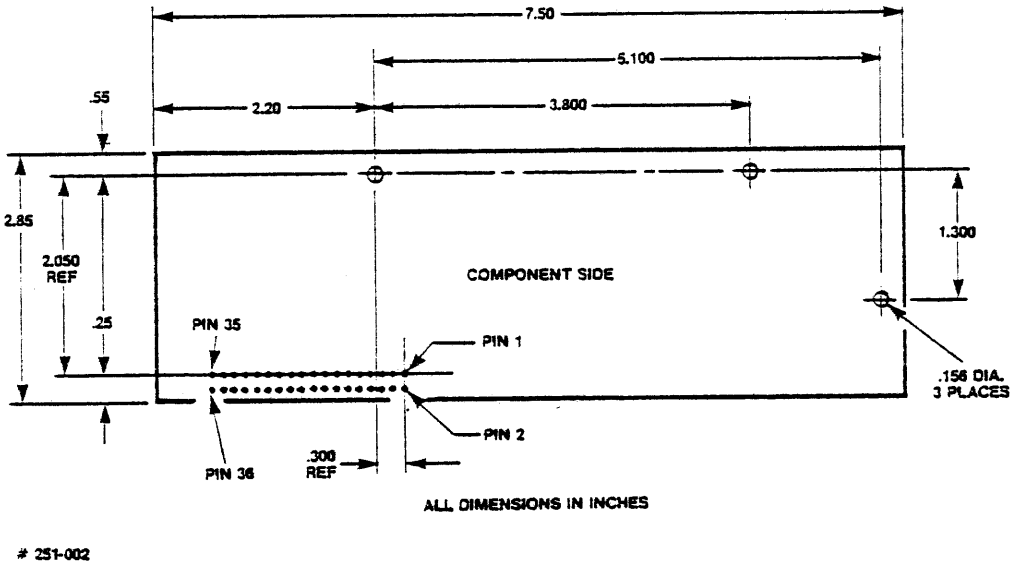


Figure 2-1. iSBX Connector and Spacer Locations

## 2.3.1 Mounting Requirement

Figure 2-1 shows the iSBX connector locations, spacer locations, and the board dimensions. Table 2-1 lists the pin assignments of the iSBX connector. The iSBX-251 board mounts onto a host board supporting an iSBX mating connector and the proper mounting holes. The mounting hardware supplied as part of the iSBX board includes:

a. 3 nylon spacers, 1/2" threaded, separate from the board.
b. 6 nylon screws, 1/4" 6-32, separate from the board.
c. One 36-pin connector (P1), factor-installed onto the board.

NOTE

The iSBX-251 board, when installed onto a host iSBC board, occupies two additional card slots adjacent to the host iSBC board in the 604/614 card cage.

Figure 2-2 shows the clearances for an iSBX-251 Multimodule board mounted onto a host iSBC board. Height dimensions shown are maximum.

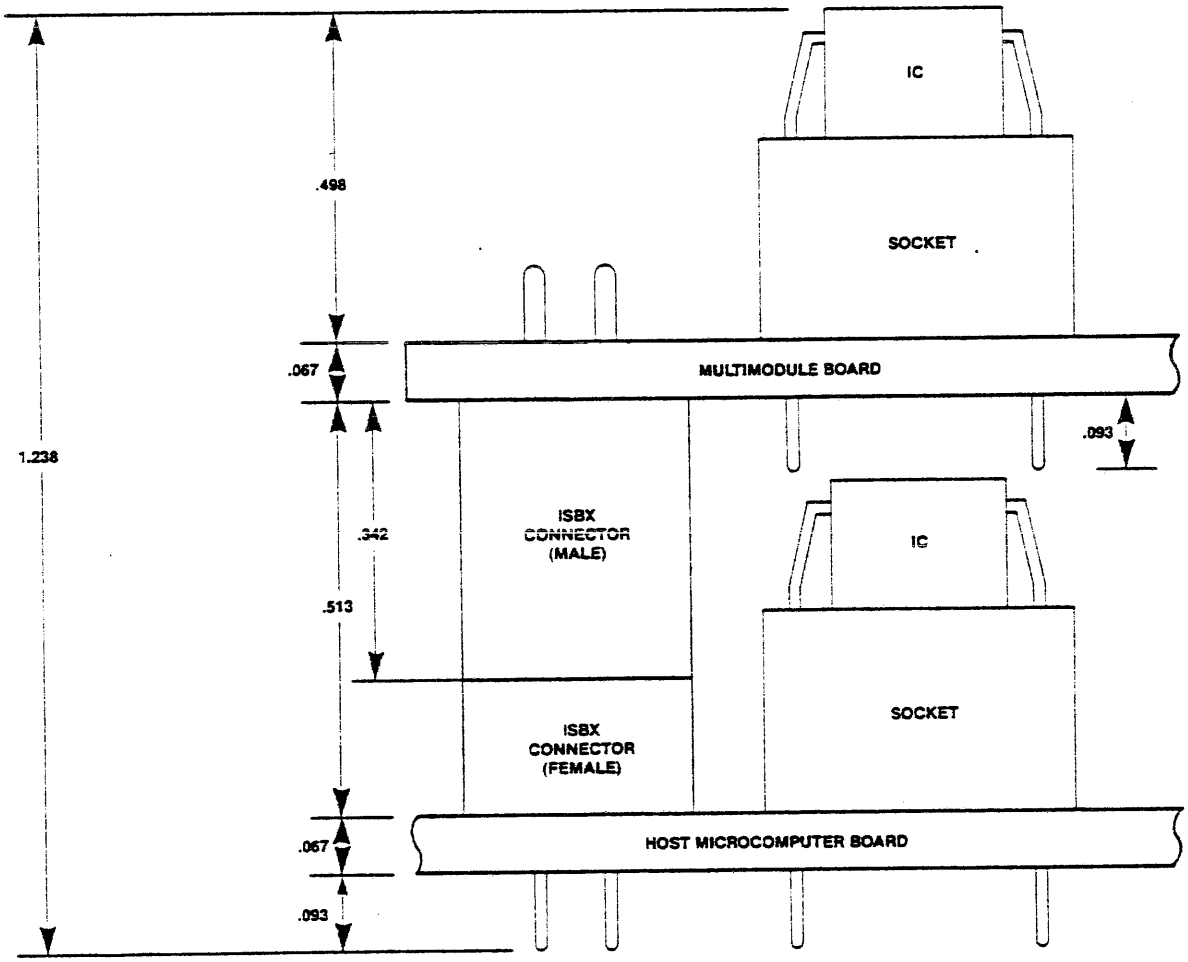


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Figure 2-2. Mounting Clearances (Inches)

Table 2-1. iSBX P1 Pin Assignment

| Pin | Mnemonic | Description | Pin | Mnemonic | Description |
|---|---|---|---|---|---|
| 35 | GND | Signal Ground | 36 | +5V | +5Volts |
| 33 | MD0 | MDATA Bit 0 | 34 | MDRQT | M DMA Request |
| 31 | MD1 | MDATA Bit 1 | 32 | MDACK/ | M DMA Acknowledge |
| 29 | MD2 | MDATA Bit 2 | 30 | OPT0 | Option 0 |
| 27 | MD3 | MDATA Bit 3 | 28 | OPT1 | Option 1 |
| 25 | MD4 | MDATA Bit 4 | 26 | | Unused |
| 23 | MD5 | MDATA Bit 5 | 24 | | Unused |
| 21 | MD6 | MDATA Bit 6 | 22 | MCS0/ | M Chip Select 0 |
| 19 | MD7 | MDATA Bit 7 | 20 | | Unused |
| 17 | GND | Signal Gnd | 18 | +5V | +5 Volts |
| 15 | IORD/ | I/O Read Cmd | 16 | | Unused |
| 13 | IOWRT/ | I/O Write Cmd | 14 | MINTR0 | M Interrupt 0 |
| 11 | MA0 | M Address 0 | 12 | MINTR1 | M Interrupt 1 |
| 9 | - | Unused | 10 | | Unused |
| 7 | | Unused | 8 | MPST/ | M Present |
| 5 | RESET | Reset | 6 | | Unused |
| 3 | GND | Signal Gnd | 4 | +5V | +5 Volts |
| 1 | +12V | +12 Volts | 2 | | Unused |

## 2.4 ELECTRICAL CONSIDERATIONS

The iSBX-251 board communicates with the host board via a 36-pin connector that comprises data lines, power lines, and control signal lines. The following paragraphs define the DC specifications of these lines, while the operational description is deferred until Chapter 4.

### 2.4.1 DC Specifications

The DC specifications for the iSBX bus interface (P1) are summarized in Tables 2-2 and 2-3. Table 2-2 is the output specifications; Table 2-3 is the input specifications. The output specifications are the minimum drive requirements on the output drivers of the iSBX-251 board (that is, the data bus output drivers must guarantee at least 1.6 mA at 0.5V.). The input specifications are the specifications of the receivers on the iSBX-251 board (for example, the loading of the address lines (MA0-MA2) can not exceed 0.5 mA at .8 volts.

**Table 2-2 iSBX-251 Connector P1 Output Specifications**

| Bus Signal Name | Type Drive | $I_{OL}$ Max (mA) | $V_{OL}$ Max (Volts) | $I_{OH}$ Max (µA) | $V_{OH}$ Min (Volts) | $C_O$ Min (pf) |
|---|---|---|---|---|---|---|
| MD0-MD7 | TRI | 1.6 | 0.5 | -200 | 2.4 | 130 |
| MINTR0-1 | TTL | 2.0 | 0.5 | -100 | 2.4 | 40 |
| MDRQT | TTL | 1.6 | 0.5 | -50 | 2.4 | 40 |
| OPT0 | TTL | 1.6 | 0.5 | -50 | 2.4 | 40 |
| MPST/ | TTL | NOTE 2 | | | | |

1. TTL = Standard totem pole output. TRI = Tri-state.
2. iSBX-251 board must connect this signal to ground.

**Note:**

$I_{OL}$ = Current output, low

$I_{OH}$ = Current output, high

$C_O$ = Capacitance output

Table 2-3 iSBX-251 Connector P1 Input Specifications

| Bus Signal Name | Type Receiver | $I_{IL}$ Max (mA) | Vin Max (Volts) | $I_{IH}$ Max (µA) | Vin Max (Volts) | $C_I$ Max (pf) |
|---|---|---|---|---|---|---|
| MD0-MD7 | TR1 | -0.5 | 0.8 | 70 | 2.0 | 40 |
| MA0 | TTL | -0.5 | 0.8 | 70 | 2.0 | 40 |
| MCS0 | TTL | -4.0 | 0.8 | 100 | 2.0 | 40 |
| MRESET | TTL | -2.1 | 0.8 | 100 | 2.0 | 40 |
| MDACK/ | TTL | -1.0 | 0.8 | 100 | 2.0 | 40 |
| IORD/ IOWRT/ | TR1 | -1.0 | 0.8 | 100 | 2.0 | 40 |
| OPT0 | TR1 | -2.0 | 0.8 | 100 | 2.0 | 40 |

1. TTL = Standard totem pole output. TR1 = Tri-state.

**Note:**

$I_{IL}$ = Current input, low

$I_{IH}$ = Current input, high

$C_I$ = Capacitance input

## 2.5 JUMPER CONFIGURATIONS

Either W1 (A to B) or W2 (A to B) must be jumpered. W1 selects DRQ interrupt mode and W2 selects DMA mode. Either setting will allow the board to operate in polled mode. Modes of operation are explained in Section 3.

W3 and W4 are set at manufacture time according to observed characteristics of the 7110 memory device. They should not be changed by the user.

## 2.6 INSTALLATION PROCEDURE

**CAUTION**

Power down the system before continuing.

The iSBX-251 board mounts onto the host iSBC board. Install the board as follows:

a. With the 6-32 screws, secure the three 1/2" plastic spacers to the host iSBC board as shown in Figure 2-3.

b. Locate pin 1 on the iSBX connector (P1) of the Multimodule board and align it with pin 1 of the iSBX connector on the host iSBC board.

c. Align the iSBX-251 board mounting holes with the spacers on the host iSBC board. See Figure 2-1 for hole location.

d. Gently press the two boards together until the connector seats.

e. Fasten the iSBX-251 board to the spacer with the three remaining 6-32 nylon screws.

**NOTE**

The position of an installed Multimodule board and the hostboard connector may vary according to the type of hostboard that is used.

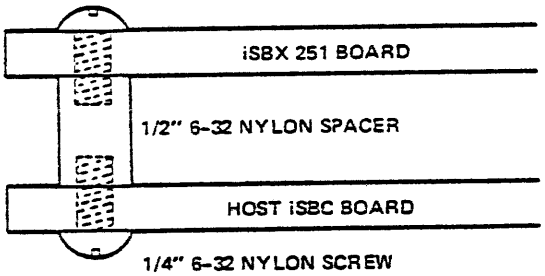


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Figure 2-3. Mounting Technique

# CHAPTER 3

# PROGRAMMING INFORMATION

## 3.1 INTRODUCTION

This chapter provides programming information for the iSBX-251 board. Included is information on how the board manipulates data, I/O addressing, system initialization, and 7220 Bubble Memory Controller (BMC) utilization. The logic and design of the iSBX-251 board is based on the 7110 Magnetic Bubble Memory (MBM) and its support circuitry, consisting primarily of the 7220 BMC. The 7220 BMC is the only user programmable device on the board.

This chapter provides information on how to invoke the 7220 BMC command set from the host base board. This command set provides total control over the iSBX-251 board. Included in the programming information are the complete status register bit definitions, DMA operation, and interrupt handling.

The following text presents an overview of how data is stored and accessed on the iSBX-251 board. Following the overview, the 7220 BMC chip command set and its implementation are explained. Each host board must be configured to provide the necessary software to meet these requirements.

## 3.2 DATA STORAGE OVERVIEW

The iSBX-251 board can be configured via software to resemble a floppy disk or similar data storage device, but the user must provide the programs to do this. Internally, the iSBX-251 operates on one byte of data at a time.

When writing data, the host board transfers from one to 40 bytes to an internal buffer in the 7220 BMC. The 7220 BMC performs a parallel-to-serial conversion on each byte and transfers the serialized data to the 7242 FSA. The 7242 and the remaining board components store the serialized data in the 7110 MBM.

When reading data, the opposite operation occurs. The 7242 FSA and support components obtain eight bits of data from the 7110 MBM and transfer it to the 7220 BMC. The 7220 BMC performs a serial-to-parallel conversion on the data, collects up to 40 bytes of data and stores the data in its internal buffer until the host board is ready for data transfer.

## 3.3 7220 BMC OPERATION

The 7220 is an LSI Magnetic Bubble Memory Controller chip that contains the circuitry and control functions for interfacing the host microprocessor board with a 7110 MBM chip and its support circuits. The 7220 makes the 7110 MBM look like a peripheral to the microprocessor system bus. The 7220 performs all serial-to-parallel and parallel-to-serial data conversions, and generates all timing signals necessary for the proper operation of the MBM's immediate support circuitry. It contains a 40-byte "First-In-First-Out" buffer (FIFO) for transmittal of data to and from the host board. The details of the operations are discussed in Chapter 4.

Signals provided by the 7220 BMC permit the iSBX-251 board to be wired to operate in the Direct Memory Access (DMA) mode, the Interrupt-driven mode, or in the Polled I/O mode. In the polled I/O method, the user must periodically check to determine when a data transfer can take place. In the Interrupt-driven mode, the BMC DRQ line doubles as a "FIFO HALF FULL/HALF EMPTY" indicator and generates an interrupt when at least 20 bytes of data can be transferred. In the DMA mode, the user initializes the DMA controller on the host board to perform all data transfers and then loads the BMC with the proper command to begin data transfer. These modes are explained in detail later in this chapter.

Jumper configurations for DRQ Interrupt mode and DMA mode are described in Section 2.6.

### 3.3.1 7220 Registers

The 7220 contains three primary registers with which the user interacts. These are the 8-bit Status Register (STR), the 4-bit Command Register (CMDR), and the 4-bit Register Address Counter (RAC). The Utility Register, Block Length Register LSB, Block Length Register MSB, Enable Register, Address Register LSB, Address Register

MSB, and FIFO Data Buffer are accessable via the RAC. The STR, CMDR, and RAC are selected and accessed in one operation each, while the balance are selected by first loading the RAC with the correct access code, then performing the desired operation. Table 3-1 specifies the registers and access codes that can be selected via the RAC.

Table 3-1. Registers Accessed Via Register Address Counter Contents

| Register | Code (Hex)* |
|---|---|
| FIFO | 00 |
| Reserved | 00-09 |
| Utility Register | 0A |
| Block Length LSB | 0B |
| Block Length MSB | 0C |
| Enable | 0D |
| Address LSB | 0E |
| Address MSB | 0F |

*1) Register codes 01 to 09 (Hex) are reserved. Random errors may be generated if the reserved register codes are used.

2) The code is sent on the iSBX data lines D0-D7 when iSBX signal WR/ is asserted. If D0-D7 are in the range 10-20 (Hex), the Command Register is accessed (see Table 3-3).

### 3.3.2 I/O Addressing

The microprocessor on the host iSBC board communicates with the programmable 7220 BMC chip through a sequence of I/O Read and Write Commands. The address of the iSBX I/O connector is determined by the host board configuration.

The iSBX-251 requires two I/O ports for operation; a Command/Status Port controls access to reading the status register and loading the CMDR or RAC, while a Data Port controls access to reading or writing the register specified by the RAC.

To access the Command/Status Port, set A0=1; to access the Data Port set A0=0. Table 3-2 shows the I/O signals and corresponding registers.

**Table 3-2. iSBX-251 Register Selection**

| | 7220 BMC Pins | | | | Function |
|---|---|---|---|---|---|
| | AO | D0-D7 | RD/* | WR/ | |
| Data Port | 0 | Register Data | 0 | 1 | Read Register Addressed by RAC |
| | 0 | Register Data | 1 | 0 | Load Register Addressed by RAC |
| Command Status Port | 1 | BMC Status (Table 3-4) | 0 | 1 | Read BMC Status Register |
| | 1 | 00 (Hex)-0F (Hex) | 1 | 0 | Load RAC |
| | 1 | 10 (Hex)-1F (Hex) | 1 | 0 | Issue Command |
| | 1 | 20 (Hex) | 1 | 0 | Clear interrupt and point RAC to FIFO |

*RD/=0 means I/O port read;
WR/=0 means I/O port write

For an 8-bit iSBX connector, such as on the iSBC 208 floppy disk controller, iSBX address line MAO is typically the least significant bit of the Multibus I/O port address bit AO. For a 16-bit connector, such as on the iSBC 86/05 processor board, Multibus I/O port address bit AO is used to select 8- or 16-bit mode. Multibus bit A1 is then connected to iSBX signal MAO.

For example, the iSBC 208 has two iSBX connectors and the iSBX 251 can be mounted on one of them. When the system is configured, the user selects an I/O port address for the iSBC 208. The two ports of the iSBX 251 are addressed by offsets from this port address.

Circuitry on the iSBC 208 decodes the Multibus I/O port address to select the iSBX 251 ports. iSBX address bit MAO then selects either the 7220 Data Port or the 7220 Command/Status Port.

As an example, consider a host whose I/O port address is 80 (Hex). The possible 7220 I/O port addresses are:

| | 16-bit I/O Port Address (Hex) | 8-bit I/O Port Address (Hex) |
|---|---|---|
| iSBX Base Address | 80 | 80 |
| 7220 Data Port | 80,84,... | 80, 82,... |
| 7220 CMD/Status Port | 82, 86,... | 81, 83,... |

### 3.3.3 7220 Command Set

The 7220 BMC command set comprises 16 commands. These commands are transferred to the iSBX-251 board from the host board. Most of these commands require multiple bytes to fully specify the operation that the BMC is to perform. The command set is listed in Table 3-3 along with the operation codes.

If bit 5 in the Command Register is set, the INT pin on the 7220 BMC will be set low, clearing the interrupt. The command specified by bits 0-4 will then be executed.

For example, writing a 32 (Hex) to the Command Register will clear any interrupt and then cause a 'READ BUBBLE DATA' to be executed.

If the previous command caused an interrupt, that interrupt must be cleared before the next command is executed. Typically, the user's interrupt routine will write a 20 (Hex) to the Command Register to clear the interrupt and point the RAC to the FIFO.

### 3.3.4 Command Implementation

The RAC provides a means of addressing the remaining registers required for operation of the 7220 BMC and its support circuitry. The registers accessed via the RAC are frequently called Parametric Registers, because they contain parameters to commands written to the CMDR. Generally, it is necessary to load the required parameter information into these registers before issuing commands to the BMC. A frequently used procedure is to first load the parametric registers in the order of increasing register addresses, and then issue a read or write command to the CMDR.

Table 3-3. 7220 BMC Command Set

| Command (Hex)* | Function |
|---|---|
| 10 | Write Bootloop Register Masked |
| 11 | Initialize |
| 12 | Read Bubble Data |
| 13 | Write Bubble Data |
| 14 | Read Seek |
| 15 | Read Bootloop Register |
| 16 | Write Bootloop Register |
| 17 | Write Bootloop |
| 18 | Read FSA Status |
| 19 | Abort |
| 1A | Write Seek |
| 1B | Read Bootloop |
| 1C | Read Corrected Data |
| 1D | FIFO Reset |
| 1E | MBM Purge |
| 1F | Software Reset |
| 20 | Clear BMC Interrupt and point RAC to FIFO |

*The command is sent on the iSBX data lines D0-D7 when iSBX signal WR/ is asserted. If D0-D7 are in the range 00-0A (Hex), the RAC is accessed (see Table 3-1).

The commands are detailed in Section 3.4.

To facilitate this procedure, the BMC automatically increments the RAC, if non-zero, by one count after each transfer of data to or from a parametric register. This enables the user to access the next register without having to make another write reference to the RAC, thus cutting down on the number of operations required to load all the parametric registers.

The RAC increments from the initially loaded value through address 1111 binary and then on to 0000 binary (the FIFO address). At this point it no longer increments. All subsequent data transfers to the data port will be to or from the FIFO until the RAC is loaded with a different register address.

The user issues a command by writing a command code to the command register (CMDR).

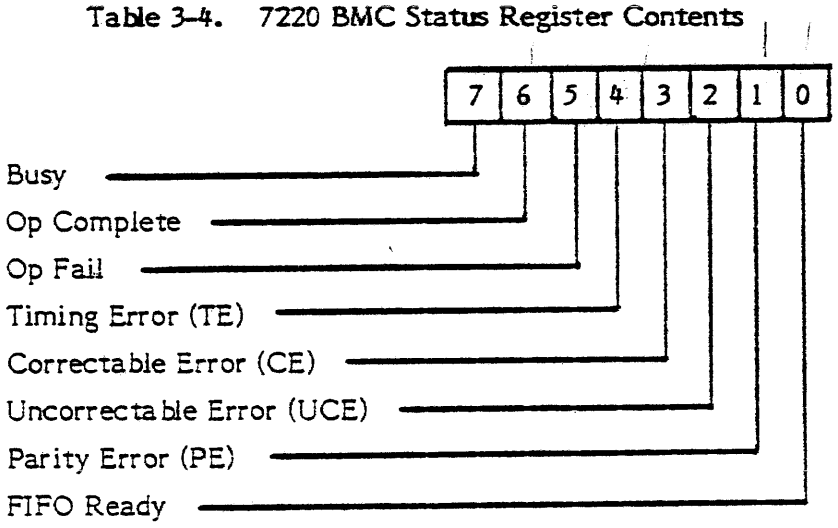
### 3.3.5 7220 BMC Status Register

The 7220 BMC status register (STR) provides information about error conditions, completion or termination of commands, and the BMC's readiness to transfer data or accept new commands. The register is eight (8) bits wide. Table 3-4 shows the relevant position of each status indicator in the register.

**NOTE**

The 7220 Status Register is cleared when the host clears the 7220 interrupt (the INT pin). This is done by writing a 20 (Hex) to the 7220 Command Register.

**Table 3-4. 7220 BMC Status Register Contents**



The Status indicator bits have the following meanings:

**BUSY –**
(when=1)

Indicates the BMC is in the process of executing a command. In the case of a Read command, Busy may also indicate that the data has not been completely removed from the FIFO, and therefore DRQ is still active. Busy will then drop as soon as DRQ drops (after the user has finished reading the data remaining in the FIFO).

When BUSY is high, none of the other status indicators are valid, except for FIFO READY. ABORT is the only command that can be issued while BUSY is high.

**OP COMPLETE –**
(when=1)

Indicates the successful completion of a command.

Note that on a read command, BUSY will remain active until the FIFO is drained, even though OP COMPLETE is asserted as soon as data is transferred from the 7110 bubble chip to the FIFO.

**OP FAIL –**
(when=1)

Indicates that the BMC was unable to successfully complete the current command. The reason for failure can be determined from other bits in the Status Register (TE, CE, UCE, PE).

TIMING ERROR (TE) –
(when=1)

Indicates that an FSA has reported a timing error of the BMC, or that the host system has failed to keep up with the BMC, thereby causing the BMC FIFO to overflow or to become empty. TIMING ERROR is also set if no bootloop sync byte is found during initialization, or if a Write Bootloop command is issued when the WRITE BOOTLOOP ENABLE bit is equal to zero in the enable register.

CORRECTABLE ERROR (CE) –
(when=1)

Indicates that an FSA has reported to the BMC that a correctable error has been detected in the last data block transferred.

UNCORRECTABLE ERROR (UCE) –
(when=1)

Indicates that an FSA has reported to the BMC that an uncorrectable error has been detected in the last data block transferred.

PARITY ERROR (PE) –
(when=1)

Indicates that the BMC's parity check circuitry has detected a parity error on a data byte sent to the BMC by the user on the data lines D0-D8. Since Parity is not supported by the iSBX Bus (except through the option pins), this bit should be ignored by user software.

FIFO READY – Has two functions. When the BMC is not busy (BUSY=0) FIFO READY = 0 indicates that the FIFO and its input and output latches are all completely empty. When BUSY=0, FIFO READY=1 indicates that there is data in the FIFO or in its latches. When the BMC is busy (BUSY=1) FIFO READY = 1 indicates (during read operations) that the BMC output latch has data for the user or (during write operations) that the BMC input latch is ready to receive data from the user.

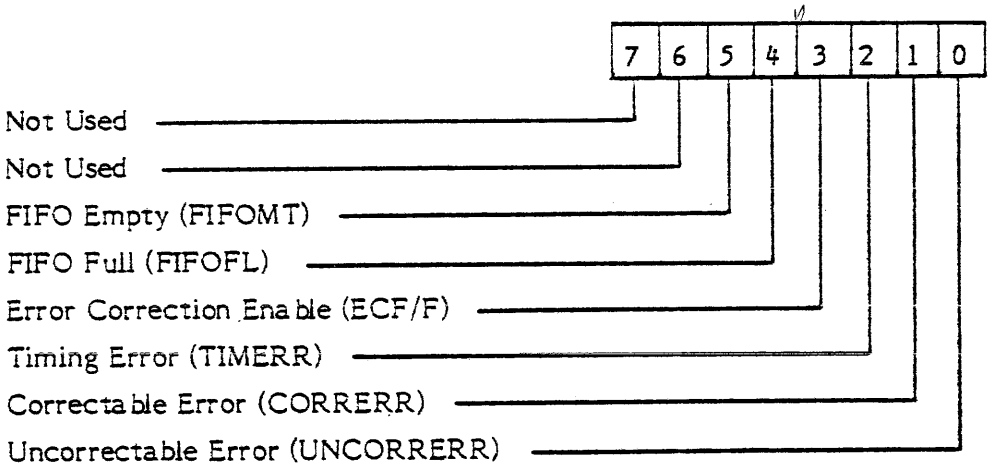
Status Register bits 1 through 6 are reset when interrupts are cleared. The status bits and the FIFO are discussed in more detail later in this chapter.

### 3.3.6 7242 FSA Status Register

The 7242 FSA contains an 8-bit status register that reflects the internal status of the chip. The status information is available to the 7220 BMC and the user via a 7220 Read FSA status command.

Although the user does not normally read this register, the 7220 BMC uses the FSA status information to modify some of its internal operations. For additional technical detail, consult the 7242 FSA data sheet. The FSA status register contents, shown in Table 3-5, is accessed with the 7220 Read Status Register command.

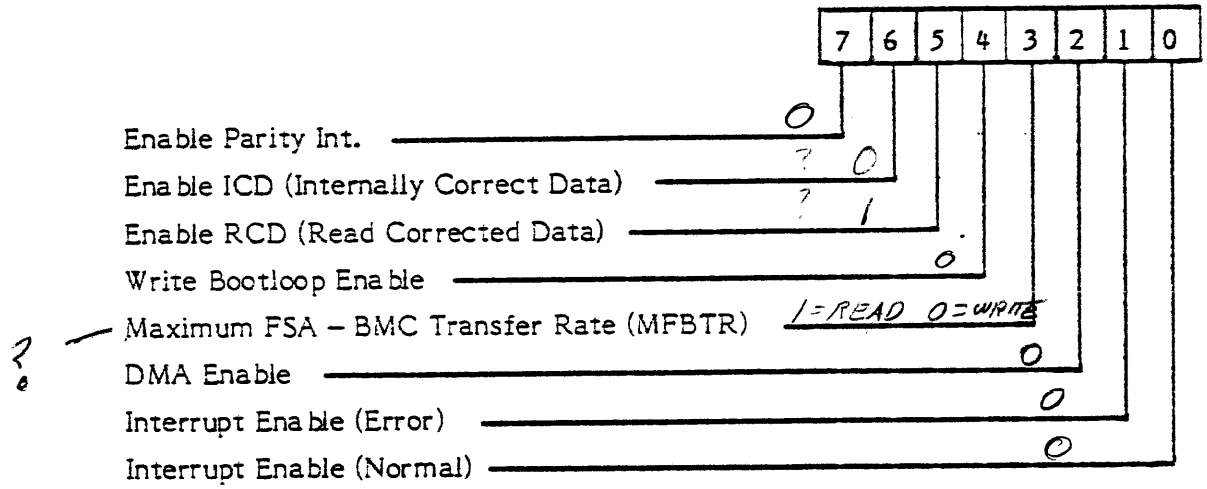
Table 3-5. 7242 FSA Status Register Contents




### 3.3.7 7220 BMC Enable Register

The Enable Register (ER) is accessed by the user to enable or disable various functions within the BMC or the FSA. Table 3-6 shows the relevant position of each function controlled by the Enable Register.

Table 3-6. Enable Register Contents




Each Enable Register bit is described below.

ENABLE PARITY INTERRUPT –

Enables the BMC to interrupt the host system (via the INT line) when the BMC detects a parity error on the data bus lines D0-D7.

ENABLE INTERNALLY ~~CORRECT~~ TEST DATA (ICD) –

Enables the BMC to give the Internally Correct Data command to an FSA when an error has been detected by the FSA's error detection and correction circuitry. The FSA responds to such a command by internally cycling the data through its error correction network. When finished, the FSA returns status to the BMC as to whether or not the error is correctable. The value of ENABLE ICD affects the action of INTERRUPT ENABLE (ERROR), as explained below.

ENABLE READ CORRECTED DATA (RCD) –

Enables the BMC to give the Read Corrected Data command to an FSA in which an error has been detected. This causes the FSA to correct the error (if possible) and also to transfer the corrected data to the BMC. The Read Corrected Data command is also used to read into the BMC data previously corrected by the FSA in response to an Internally Correct Data command. In either case, when the data transfer has been completed, the BMC can read FSA status to determine whether or not the error was correctable.

ENABLE READ CORRECTED (Continued) DATA (RCD) –

YES

In the case of an uncorrectable error, bad data may have been sent to the user. The value of ENABLE RCD affects the action of INTERRUPT ENABLE (ERROR), as explained below.

WRITE BOOTLOOP ENABLE – (when=1)

Enables the bootloop to be written. If this bit is equal to zero and a Write Bootloop command is received by the BMC, the command is aborted and the TIMING ERROR bit is set in the STR.

CAUTION

The bootloop should only be written with the value printed on the 7110 memory device label.

MAXIMUM FSA-BMC TRANSFER RATE– (MFBTR)– (when=0)

MFBTR controls the maximum burst transfer rate from FSA(s) to BMC FIFO. This rate is variable on the "last page" of a multiple page transfer. (In one page transfers the last page is the only page.) See Table 3-7 for effects of this bit on the various 7220-1 commands.

DMA ENABLE – (when=1)

NO

Enables the BMC to operate in DMA data transfer mode, using the DRQ and DACK/ signals in interaction with a DMA controller. When equal to zero, DMA ENABLE sets up the controller to support interrupt driven or polled data transfer.

INTERRUPT ENABLE (ERROR) –

NO

Selects error conditions under which the BMC stops command execution and interrupts the host processor (via the INT line). INTERRUPT ENABLE (ERROR) operates in conjunction with ENABLE ICD and ENABLE RCD, as shown in Table 3-8.

INTERRUPT ENABLE (NORMAL) – (when=1)

NO

Enables the BMC to interrupt the host system (via the INT line), when a command execution has been successfully completed (OP COMPLETE=1 in the STR).

When reading data or reading the bootloop, the assertion of OP COMPLETE means that data has been transferred from the 7110 bubble chip to the FIFO. The BUSY flag in the 7220 Status Register will not go away until the FIFO is drained by the user.

**Table 3-7. MFBTR Bit Definitions**

| Number of MBMs Operated in Parallel | Maximum Required Host Interface Data Rate | MFBTR Bit | |
|---|---|---|---|
| | | Read Command | Write Command |
| 1 | 50K byte/sec | 20 µs 0 | N/A |
| 1 | 12.5K byte/sec | 80 µs 1 | 0 |

NOTE: The MTBTR bit should always be set to "0" for all commands except "Read Bubble Data."

### 3.3.8 Error Correction

The 7220 BMC provides several levels of error correction options and multiple interrupt options. Table 3-8 shows how the Enable ICD, Enable RCD, Interrupt Enable, and the indicated status register bits produce the error correction and interrupt options.

**Table 3-8. Error Interrupt Decoding**

Interrupt Enable (Error)
Enable RCD
Enable ICD

| OPTION | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Error Interrupts Disabled | . | 0 | 0 | . | . | . | 0 | . |
| Interrupt on TE only | . | 0 | 0 | . | . | . | 1 | . |
| RCD and Interrupt on UCE, CE, or TE | . | 0 | 1 | . | . | . | 1 | . |
| RCD and Interrupt on UCE or TE<br>Level 1 error correction | . | 0 | 1 | . | . | . | 0 | . |
| ICD and Interrupt on UCE or TE<br>Level 2 error correction | . | 1 | 0 | . | . | . | 0 | . |
| ICD and Interrupt on UCE, CE, or TE<br>Level 3 error correction | . | 1 | 0 | . | . | . | 1 | . |

TE = Timing Error
UCE = Uncorrectable Error
CE = Correctable Error
ICD = Internally Correct Data
RCD = Read Correct Data

Level 1 error correction is used when the user is not concerned with correctable errors or error logging. When a read error occurs, the BMC automatically issues a Read Corrected Data command to the 7242 FSA. The FSA cycles the data through its error correction circuitry, updates its status register, and transmits the data to the BMC. The BMC stores the data, with no regard to correct or incorrect data, in its FIFO, then checks the 7242 FSA status register. If the data was correctable, normal operation continues; if the data was not correctable, the FSA stops command execution and interrupts the host board. The entire read operation must be repeated if the host board wants to reread the bad page of data. The parametric registers in the BMC should be reloaded prior to repeating the operation.

In level 2 error correction, the BMC and FSA function similar to level 1 when a read error occurs, except the bad data is not sent to the BMC and the BMC Address Register contents point at the bad page address. The host board can read the bad page address and add it to a bad address table. The bad address table could be used over a period of time to observe whether specific error patterns develop in the bubble. If specific patterns develop, the bubble bootloop could be rewritten to ignore these areas. The bad data can be retrieved, if desired, by issuing a Read Corrected Data command. The read operation can be issued repeatedly without reloading the parametric registers.

Level 3 operation provides interrupts for both correctable and uncorrectable errors; thus, the host board can build an error address table that reflects all locations where errors have occurred. The remaining operation is similar to Level 2 operation.

When either RCD or ICD is enabled, there are 64 data bytes per page. When both are off, there are 68 data bytes per page.

RCD and ICD should never be on simultaneously.

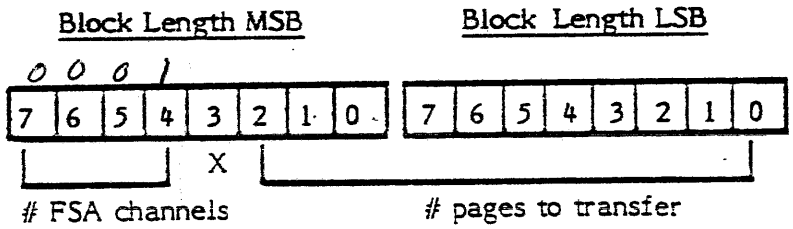
### 3.3.9 7220 Utility Register

The Utility Register (UR) is an 8-bit general purpose register available to the user. It can be used in general program applications where a temporary storage location is required.

### 3.3.10 7220 BMC Block Length Register

The Block Length Register (BLR) is composed of two 8-bit registers whose contents determine the system page size and also the number of pages to be transferred in response to a single read or write bubble data command. The bit configuration is given in Table 3-9.

**Table 3-9. Block Length Register Configuration**




BLR MSB bits 7-4 determine the number of FSA channels used. For iSBX-251 these bits should always be set at 0001.

BLR MSB bit 3 is not used.

BLR MSB bits 2-0 and BLR LSB bits 7-0 determine the number of pages to be transferred.

The MBM requires two FSA channels. Bits 7-4 of BLR MSB specify the number of FSA channels to be accessed. These bits will always be set as 0001 binary for the iSBX-251 board. Each page transferred will consist of 64 bytes of information if error correction is enabled or 68 bytes if error correction is disabled. The iSBX-251 board contains a maximum of 2048 pages of data.

1024

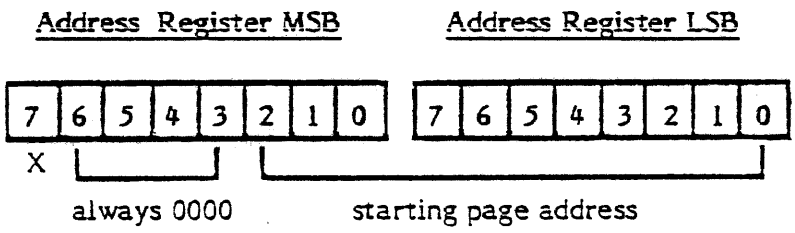
The BLR LSB, together with the 3 least significant bits of the BLR MSB, specifies the number of pages to be transferred during a single bubble data read or write command. Up to 2048 pages can be transferred at one time. All 11 bits equal to zero specifies a 2048 page transfer.

### 3.3.11 7220 BMC Address Register

The Address Register (AR) consists of two 8-bit registers, whose contents specify the 7110 MBM and the starting address location in the MBM to be used in a data read or write operation. Table 3-10 shows the bit configuration of these registers.

The low-order eleven bits designate the starting page address of the data transfer. The MSB bits 6-3 specify that one MBM is used on the iSBX-251. For the iSBX-251, the AR MSB bits 6-3 should be set equal to 0000.

**Table 3-10. Address Register Configuration**




AR MSB bit 7 is not used.

AR MSB bits 6-3 always set to 0000 to specify one MBM being used.

AR MSB bit 2-0 and AR LSB bit 7-0 specify the starting page address within the MBM.

### 3.3.12 7220 BMC FIFO

The BMC FIFO Data Buffer is a 40-byte buffer through which data is transferred. The primary purpose of the FIFO is reconciliation of the timing requirements between the user interface to the BMC and the BMC interface to the FSAs. This allows the data transfer to proceed asynchronously and relaxes timing constraints, both to the FSAs and also to the user's equipment.

When the BMC is busy (executing a command) the FIFO functions as a data buffer. When the BMC is not busy, the FIFO is available to the user as a general purpose FIFO.

The FIFO is dual port, allowing data to be written at one port while data is simultaneously read at the other port. A total of 40 bytes of data may be stored in the FIFO. During execution of a command involving data transfer (between the user and the FSAs) the data passes through the FIFO. The status of the FIFO is indicated by both the FIFO READY bit and the BUSY bit in the status register. When BUSY=1, FIFO READY=1 indicates that the FIFO has available space for data or has data ready to be read. When BUSY=0, FIFO READY=0 indicates the FIFO is empty.

The DRQ line, on the user interface, also indicates FIFO status. In DMA data transfer mode (DMA ENABLE=1 in the enable register), the DRQ line and the DACK/line together provide a standard DMA data transfer capability; the BMC can handshake with an 8257 or 8237 DMA controller.

The DRQ line indicates 'FIFO HALF FULL' or 'FIFO HALF EMPTY' in the polled and interrupt driven data transfer modes (DMA ENABLE=0 in the enable register). This provides an interrupt capability. During write operations, DRQ indicates when there is room in the FIFO for 20 more bytes of data. During read operations, DRQ indicates when there are 20 bytes of data in the FIFO for the user to read. It is recommended that the user transfer data in blocks of 20 bytes, so that the user's processor doesn't have to spend a large amount of time servicing this type of interrupt.

In general purpose FIFO mode (BMC not busy), FIFO READY=0 indicates that the FIFO and its input and output latches are empty. When the BMC is not busy, the FIFO is available to the user as a standard FIFO register file. This gives the user the capability to use the FIFO in general purpose programming or to preload the FIFO with data before issuing a Write command to the BMC. For example, the user may write up to 40 bytes of data into the FIFO and then issue a Write Bubble Data command.

Table 3-11 provides a summary of the status and control lines connected with the 7220 BMC FIFO in the non-DMA mode of operation.

The FIFO is addressed automatically after the last parametric register has been written, since the RAC is self-incrementing. Alternatively, the user can explicitly address the FIFO by writing address zero into the RAC. It is important, however, that the user never write any address (even the FIFO address itself) into the RAC when the FIFO already has some data in it. This rule prevents accidental loss of data.

**Table 3-11. Summary of 7220 FIFO Indicators (Non-DMA Operation)**

| Indicator | Meaning |
|---|---|
| DRQ=1 | There is room for 20 bytes of data on a write operation, or 20 bytes are available on a read operation. |
| FIFO READY=1 | There is room in the FIFO for at least one byte on a write operation, or at least one byte is available on a read operation. |
| BUSY=0 | An operation has completed or failed - check the 7220 BMC Status Register. |

After a Write Bubble Data command is issued, the BMC will not start the data transfer until the FIFO contains at least two bytes of data. During the execution of read or write commands, it is the user's responsibility to keep up with the data transfer process, so that the FIFO does not overflow or underflow. If the FIFO does overflow or underflow before the specified data transfer is complete, the TIMING ERROR (TE) bit will be set in the STR. To reset the TE status bit in the event of an error, either a software reset followed by a FIFO reset, or an ABORT command must be issued.

## 3.4 COMMAND DESCRIPTIONS

As mentioned earlier, the user operates the bubble memory system by reading from or writing to the user-accessible registers in the BMC. The user issues commands to the BMC by writing to the command register (CMDR). This is done by sending a command code (10 Hex to 1F Hex) to the Command/Status Port (address bit A0=1). Before issuing a command, the parametric registers must already contain any required operands or modifiers. After the registers have been loaded, the actual command is issued. While the BMC is executing the command, the user must not write to any BMC register except the FIFO. The user can read the STR at any time to determine whether or not the BMC is busy. Commands can be written to CMDR only when BUSY=0 is in the STR. When in the BMC accepts the command, BUSY is set to 1. An Abort command, however, is accepted by the BMC at any time. When a command has been completed (or terminated), BUSY is reset to 0. An interrupt is generated if the corresponding interrupt enable bits are set in the enable register (ER).

The 7220 command set will be described in the following sections. The description gives the command name, the actual bit code, the Hexadecimal code, and a description of the commands use.

### 3.4.1 Write Bootloop Register Masked

Code = 00010000 (10 Hex)

Proper operation of the FSAs during data transfer to or from the MBMs requires that the bootloop register contain (if error correction is used) exactly 270 logic 1s for each FSA bootloop register. The user may select any subset of 270 "good" loops from the total number of available loops (if error correction is not used, 270 replaced by 272). As an alternative, the Write Bootloop Register Masked command may be used. This command counts the number of logic 1s and masks out the remaining 1s after the proper count has been reached.

### 3.4.2 Initialize

Code = 00010001 (11 Hex)

The BMC executes the Initialize command by first interrogating the bubble memory system to determine how many FSAs are present, then reading and decoding the bootstrap loop from each MBM and storing the results in the corresponding FSAs bootstrap loop register. The BLR MSB must be set to 0001 binary before issuing the Initialize command. This allows the BMC to read both bootloops of the bubble and logically OR them to create a bootloop redundancy factor (a common map of both bootloops). When the sequence is completed, the BMC leaves each bubble module at a known address location and sets its own internal "next available page address" register location to zero. The following parametric registers must be preloaded as shown.

Address Register MSB (bits 6-3) = 0000 binary

Block Length Register MSB = 0001 0000 binary

As described in Section 3.5.5, an Initialize must be performed after an Abort when the power is turned on. An Initialize command should also be issued when the mode of error correction is changed (ICD or RCD).

### 3.4.3 Read Bubble Data

Code = 00010010 (12 Hex)

The Read Bubble Data command causes data to be read from the MBM into the BMC FIFO. As data is read into the FIFO, the host system will be reading it from the other end. All the parametric registers must be properly set up before issuing the command. The host system must be capable of keeping up with the data transfer rate so FIFO overflow will not occur. The following parameter registers must be preloaded as shown:

Block Length Register MSB (bits 7-4) = 0001 binary

Block Length Register MSB (bits 3-0) and LSB (bits 7-0) = number of pages to be transferred

Address Register MSB (bits 6-3) = 0000 binary

Address Register MSB (bits 2-0) and LSB (bits 7-0) = desired starting page address

### 3.4.4 Write Bubble Data

Code = 00010011 (13 Hex)

The Write Bubble Data command causes data to be read from the BMC FIFO and written into the MBM. The host system writes data to one end of the FIFO and the bubble system takes it from the other end. All parametric registers must be properly set before issuing the command. The following parameter registers must be preloaded as shown:

Block Length Register MSB (bits 7-4) = 0001 binary

Block Length Register MSB (bits 3-0) and LSB (bits 7-0) = number of pages to be written

Address Register MSB (bits 6-3) = 0000 binary

Address Register MSB (bits 2-0) and LSB (bits 7-0) = desired starting page address

It is recommended that the user fill the FIFO with the first 40 bytes of data before the write command is issued.

### 3.4.5 Read Seek

Code = 00010100 (14 Hex)

The Read Seek command rotates the MBM to a designated address location with respect to the MBM's output track. No data transfer occurs. The MBM is rotated until the next data location available to be read is the specified page address (in the AR) plus one. The Read Seek command may be used to reduce latency (access time) in cases where information is available for the user to predict the location of an impending read reference to the MBM. After the Read Seek command is executed, the parametric registers must be written before any subsequent data transfer commands take place. The Address Register must be preloaded as shown:

Address Register MSB (bits 6-3) = 0000 binary

Address Register MSB (bits 2-0) and LSB (bits 7-0) = desired next page address minus one

### 3.4.6 Read Bootloop Register

Code = 00010101 (15 Hex)

The Read Bootloop Register command causes the BMC to read the bootloop register of the selected FSA channel, decode, and store this information in the BMC FIFO. Twenty bytes are transferred for each FSA channel selected. The BLR MSB bits 7-4 specify the desired FSA channel. The user sets these bits to 0000 binary to read FSA channel A and 0001 binary to read both channels of the 7242 FSA. Channel B can not be read by itself. The Address Register must be preloaded as shown:

Block Length Register MSB (bits 7-4) = desired FSA channel

### 3.4.7 Write Bootloop Register

Code = 00010110 (16 Hex)

The Write Bootloop Register command causes the BMC to write the contents of the BMC FIFO into the bootloop register of the selected FSA channel. Twenty bytes are needed for each FSA channel selected. The BLR MSB bits 7-4 specify the desired

FSA channel. The user sets these bits to 0000 binary to read FSA channel A and 0001 binary to write both channels of the 7242 FSA. Channel B can not be written by itself. The Address Register must be preloaded as shown:

Block Length Register MSB (bits 7-4) = desired FSA channel

### 3.4.8 Write Bootloop

Code = 00010111 (17 Hex)

The Write Bootloop command causes the existing contents of the MBM bootloop to be replaced by new bootloop data based on 40 bytes of information stored in the FIFO. The data to be transferred must have been previously set up by the Write Bootloop Register command. As a precaution, this command also requires an enable bit be set in the Enable Register before execution is permitted.

### 3.4.9 Read FSA Status

Code = 00011000 (18 Hex)

The Read FSA Status command causes the BMC to read both FSA 8-bit status registers and to store this information in the BMC FIFO. The status bytes are stored in the first two bytes of the BMC FIFO. The command reads channel A status register first, followed by channel B. The Read Status command is independent of all parametric registers.

### 3.4.10 Abort

Code = 00011001 (19 Hex)

The Abort command causes the termination of the command currently being executed by the BMC. The 7110 MBM is stopped in a controlled manner, where no bubble data is lost. The Abort command is accepted by the BMC (and is typically issued) when the BMC is busy. An Abort results in a status of 40H (OP COMPLETE).

### 3.4.11 Write Seek

Code = 00011010 (1A Hex)

The Write Seek command rotates the MBM to a designated address location with respect to the MBM's input track. No data transfer occurs. The MBM is rotated until the next data location available to be written is the specified page address (in the AR) plus one. The Write Seek command may be used to reduce latency (access time) in cases where information is available for the user to predict the location of an impending write reference to the MBM. After the Write Seek command is executed, the parametric registers must be rewritten before any data transfer commands may be executed. The Address Register must be preloaded as shown:

Address Register MSB (bits 63) = 0000 binary

Address Register MSB (bits 2-0) and LSB (bits 7-0) = desired next page address minus one

### 3.4.12 Read Bootloop

Code = 00011011 (1B Hex)

The Read Bootloop command causes the BMC to read the bootloop of the MBM and store the decoded bootloop information in the BMC FIFO. The Read Bootloop command must be immediately preceded by a Reset FIFO command. The BLR MSB bits must be preloaded as shown below to indicate the number of FSA's:

Block Length Register MSB (bits 7-4) = 0001 binary

### 3.4.13 Read Corrected Data

Code = 00011100 (1C Hex)

The Read Corrected Data command causes the BMC to read into the BMC FIFO a 256-bit block of data from the FIFO of each selected FSA channel after an error has been detected. The data cycles through the error correction network of the FSA. After the data has been read, the FSA reports to the BMC whether or not the error was correctable. The Read Corrected Data command is used only if ENABLE ICD or ENABLE RCD is set in the enable register (ER). The Block Length Register must be preset as shown:

Block Length Register MSB (bits 7-4) = desired FSA

### 3.4.14 FIFO Reset

Code = 00011101 (1D Hex)

The FIFO Reset command clears the BMC FIFO and its input and output latches.

### 3.4.15 MBM Purge

Code = 00011110 (1E Hex)

The MBM Purge command clears all BMC registers, counters, and the BMCs internal "next available page address" register location. The block length register, BLR MSB bits 7-4, the FSA present counter, and the four high-level bits of the address register are not cleared.

### 3.4.16 Software Reset

Code = 00011111 (1F Hex)

The Software Reset command clears all BMC registers, except those containing initialization parameters. It causes the BMC to send the Software Reset command to the FSA. No re-initialization is needed after this command. Additional commands can be executed immediately after the Software Reset command.

### 3.4.17 Clear Interrupt and Point RAC to FIFO

Code = 00100000 (20 Hex)

This command clears the INT pin on the 7220 and sets the Register Address Counter (RAC) to point to the FIFO. An interrupt must be cleared before any other new command is issued.

This command does not clear the DRQ pin.

## 3.5 SOFTWARE PROTOCOLS

This section contains recommendations that may be used when writing iSBX 251 software.

### 3.5.1 Mode Selection (DMA/Polled or DRQ/Polled)

The iSBX-251 board has jumpers that are configured to allow it to operate in DMA and polled mode, or in interrupt (DRQ) mode and polled mode. The selection between DMA and polled mode, or between interrupt and polled mode, is made by user software.

As referred to in Section 3.3.7, DMA is selected by setting bit 2 of the 7220 enable register to a '1'. User software must also load DMA parameters, such as terminal count and address, in the host DMA controller. (Figure 3-3 is a suggested outline of this process.)

Due to timing constraints, it is recommended that the Extended Write bit be set in the host DMA controller. The Extended Write bit is bit 5 of the Command Register in the Intel 8237 DMA controller, and it is bit 5 of the Mode Set Register in the Intel 8257 DMA controller.

### 3.5.2 Issuing Commands to the 7220 BMC

When issuing commands to the 7220 Controller, make sure that the BUSY bit in the 7220 Status Register is zero, indicating that the previous command has finished. The parametric registers can then be loaded and the appropriate command code can be written to the command register. ABORT is the only command that can be issued while the BUSY bit in the Status Register is equal to one.

It is also recommended that an Abort command be sent to the 7220 controller on power-up, before the Initialize command is issued.

### 3.5.3 DRQ Interrupt or Polled Mode

It is recommended that the user keep a byte count during Interrupt or Polled Mode data transfers, and not count on BUSY=0 or OP COMPLETE in the 7220 Status Register to indicate that the transfer is complete. This also makes it possible to use BUSY=0 as an error indication if it occurs prematurely.

### 3.5.4 General Interrupt Procedure

Follow this general procedure when the 7220 BMC INT pin becomes active:

1. Wait for the Busy bit in the 7220 Status Register to go low.

2. Check the 7220 Status Register to see what caused the interrupt. Depending on what you have set in the 7220 Enable Register, the interrupt could mean OP COMPLETE, OP FAIL, or a data error.

3. If you received an OP COMPLETE from a read operation, it will be necessary to drain the FIFO. OP COMPLETE actually means that the operation between the 7220 controller and rest of the bubble system has finished. The BUSY bit in the 7220 Status Register won't go away until the operation between the 7220 Controller and the host system has completed.

4. In any case, wait for the BUSY bit in the 7220 Status Register to go off. Even though the 7220 has issued the interrupt, it still may have some internal cleanup tasks to perform.

5. Service the interrupt (save status, log errors, etc.)

6. Clear the 7220 interrupt (the INT pin) by writing a 20 (Hex) to the 7220 Command register. This will also clear the 7220 Status Register.

7. Return from your interrupt routine.

### 3.5.5 Command Implementation Flow Charts

Figure 3-1 is a general flow diagram designed to cover the most commonly used modes of operation. This, along with Figures 3-2 through 3-7, can be used as a guide when writing software to drive the iSBX-251.

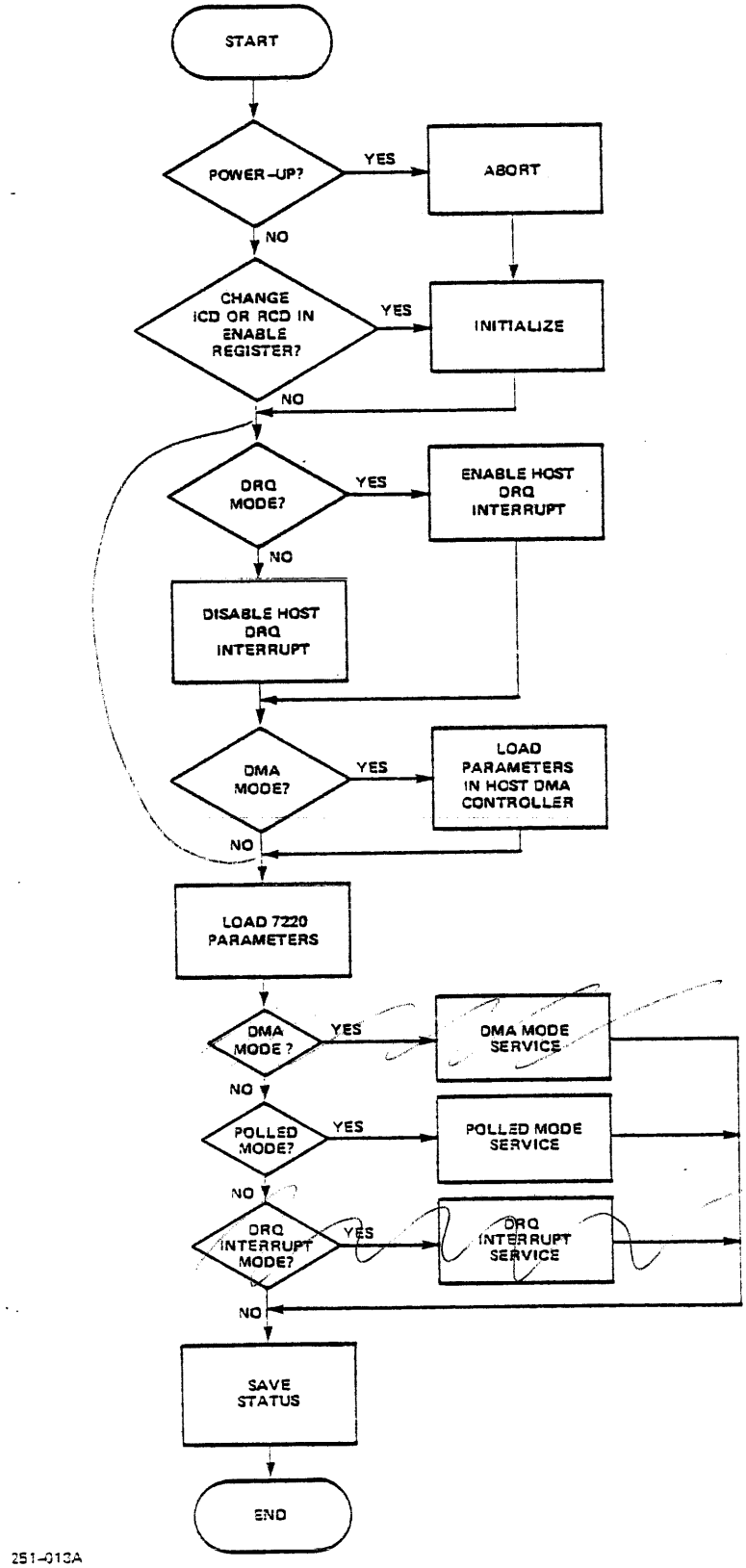
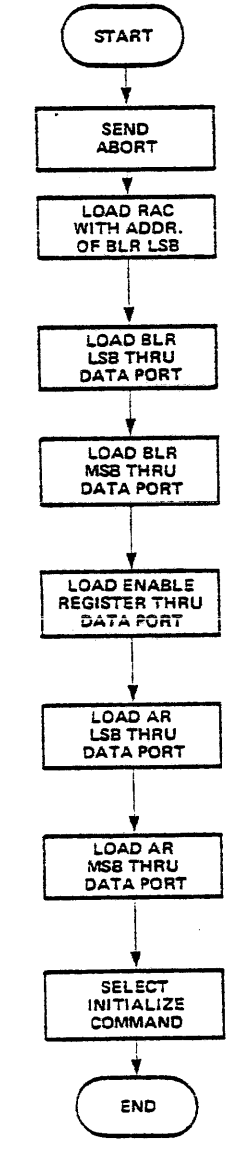



Figure 3-1. Software Overview

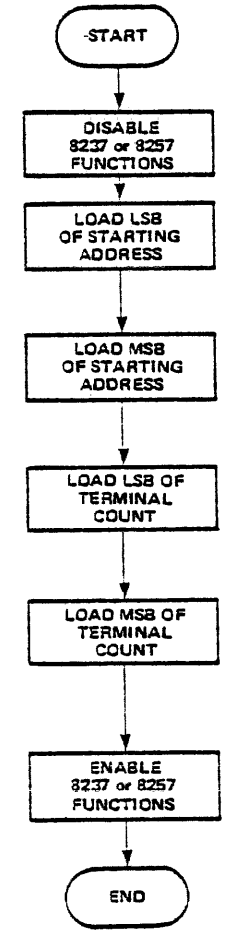



| COMMAND | ADDRESS* (HEX) | DATA (HEX) |
|---|---|---|
| I/O WRITE | 0E9 | 19; ABORT COMMAND |
| I/O WRITE | 0E9 | 0B; SELECTS RAC AND LOADS ADDRESS OF BLR LSB |
| I/O WRITE | 0E8 | DON'T CARE (ON INITIALIZE ONLY) |
| I/O WRITE | 0E8 | 10; SELECTS 2 FSA CHANNELS |
| I/O WRITE | 0E8 | ENABLE FUNCTIONS (SEE SEC. 3-3-7) |
| I/O WRITE | 0E8 | DON'T CARE (ON INITIALIZE ONLY) |
| I/O WRITE | 0E8 | SELECT LAST BUBBLE GROUP BITS 6-3 = 0000 |
| I/O WRITE | 0E9 | 11 (INITIALIZE) |

251-014A

*As an example, a base address of 0E8 is assumed. The port addresses would then be 0E8 and 0E9 for an 8-bit host, and 0E8 and 0EA for a 16-bit host.

Figure 3-2. Initialization

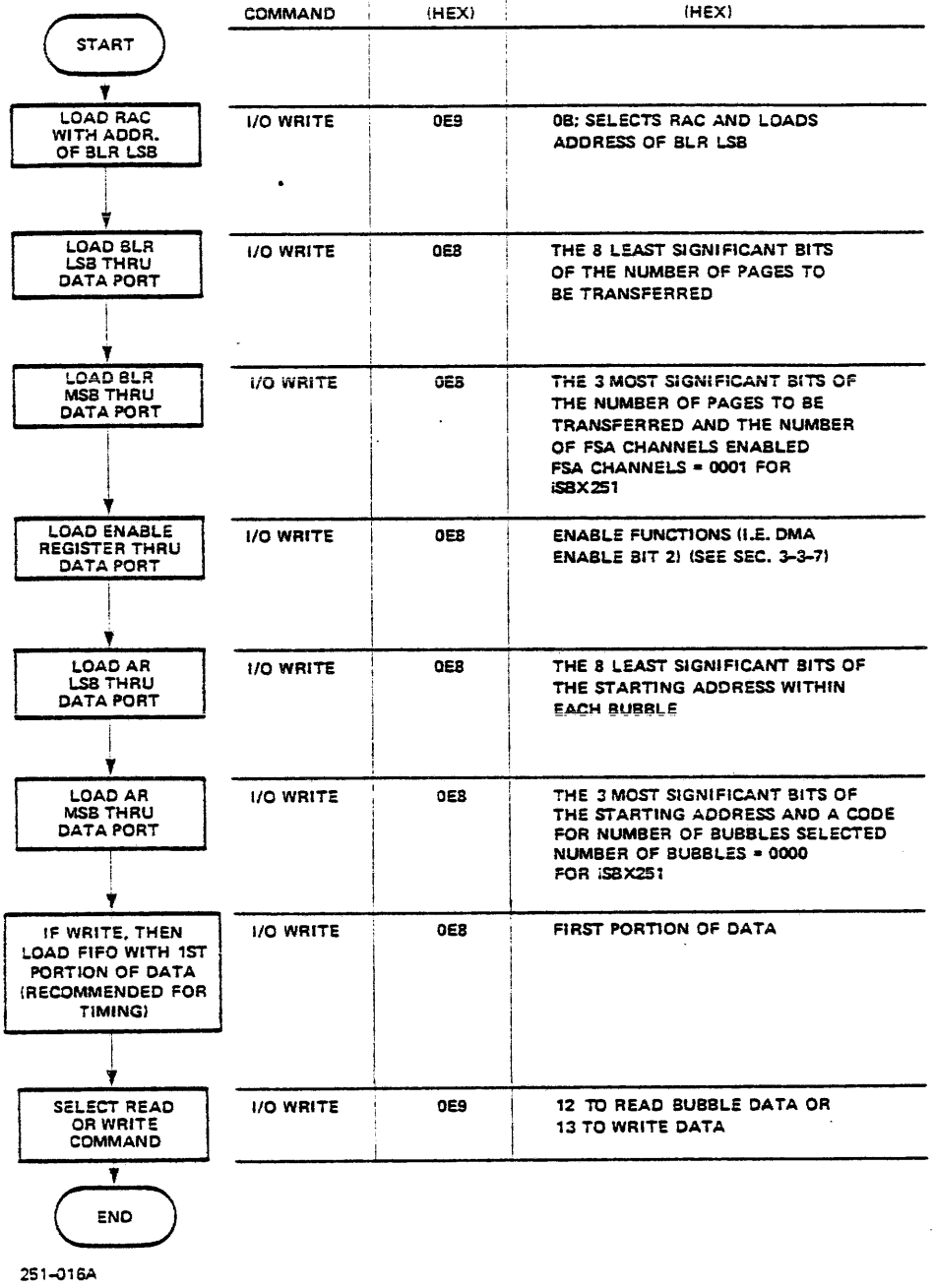



| | COMMAND | ADDRESS* (HEX) | DATA (HEX) |
|---|---|---|---|
| DISABLE 8237 or 8257 FUNCTIONS | I/O WRITE | 0F8 | 0 |
| LOAD LSB OF STARTING ADDRESS | I/O WRITE | 0F0 | THE 8 LEAST SIGNIFICANT BITS OF THE STARTING ADDRESS |
| LOAD MSB OF STARTING ADDRESS | I/O WRITE | 0F0 | THE 8 MOST SIGNIFICANT BITS OF THE STARTING ADDRESS |
| LOAD LSB OF TERMINAL COUNT | I/O WRITE | 0F1 | THE 8 LEAST SIGNIFICANT BITS OF THE TERMINAL COUNT |
| LOAD MSB OF TERMINAL COUNT | I/O WRITE | 0F1 | THE 6 MOST SIGNIFICANT BITS OF THE TERMINAL COUNT AND THE 2-BIT OF CODE (READ, WRITE, OR VERIFY) |
| ENABLE 8237 or 8257 FUNCTIONS | I/O WRITE | 0F8 | 41; ENABLE DMA CHANNEL 0 AND TC STOP |

251-015A

*Assuming base address of 0F0, 8-bit host

Figure 3-3. Loading Host DMA Parameters




*Assuming base address of 0E8, 8-bit host.

Figure 3-4. Loading 7220 Controller Parameters

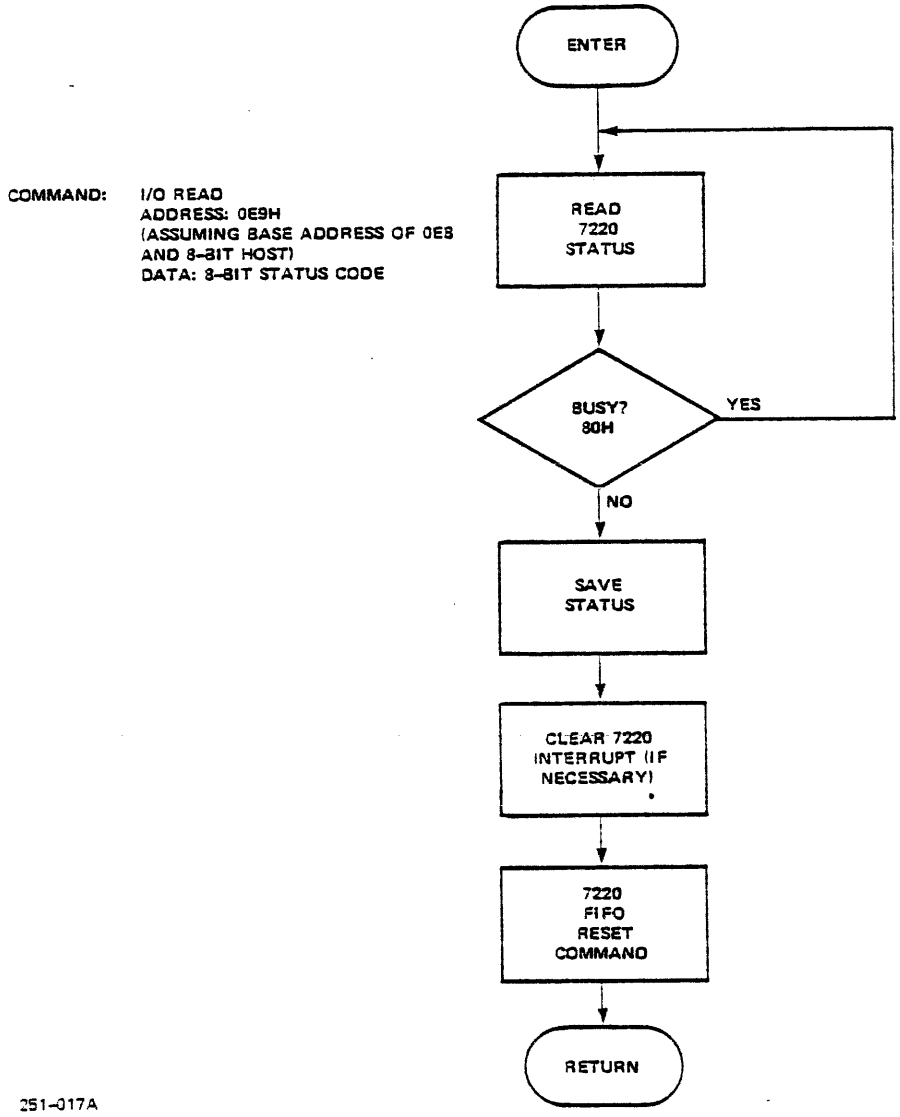
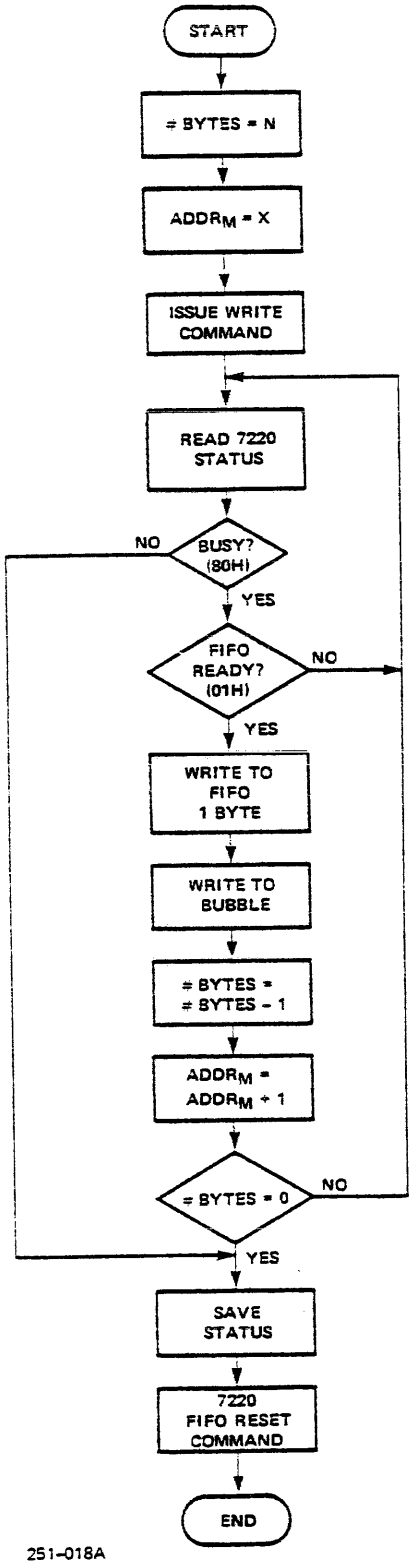
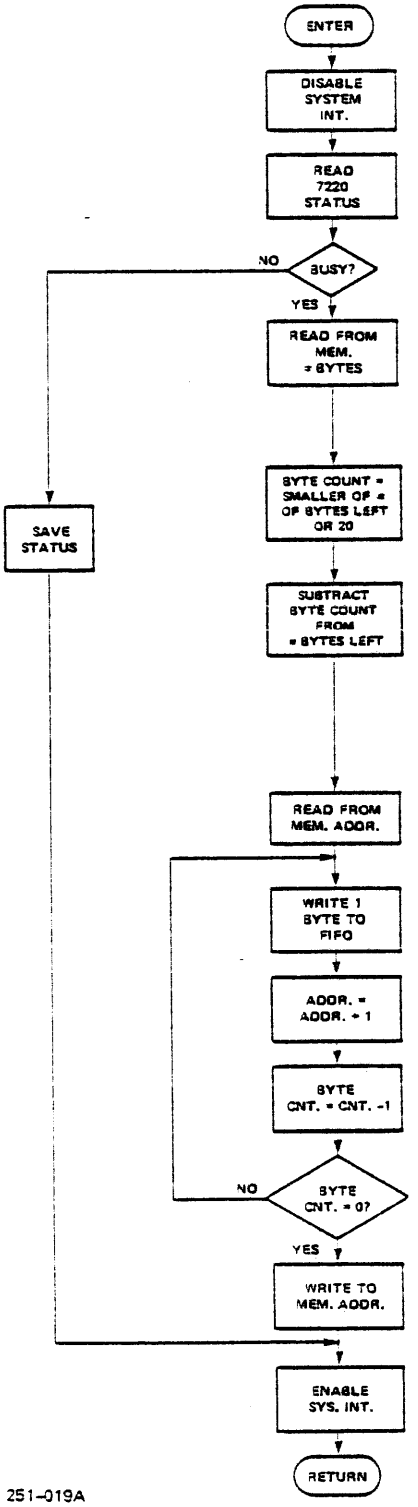



Figure 3-5. DMA Service




| COMMAND | ADDRESS* (HEX) | DATA (HEX) |
|---|---|---|
| | | |
| I/O WRITE | 0E9 | 13 |
| I/O READ | 0E9 | 8-BIT STATUS CODE |
| | | |
| I/O WRITE | 0E8 | 1 BYTE OF DATA |
| | | |
| | | |
| I/O WRITE | 0E9 | 1D |

Figure 3-6. Polled Mode Service (Write)




| COMMAND | ADDRESS* (HEX) | DATA (HEX) |
|---|---|---|
| | | |
| I/O READ | 0E9 | 8-BIT STATUS CODE |
| | | |
| I/O WRITE | 0E8 | 1 BYTE OF DATA |

*Assuming base address of 0E8, 8-bit host.

Figure 3-7. DRQ Interrupt Service (Write)

# CHAPTER 4

# PRINCIPLES OF OPERATION

## 4.1 INTRODUCTION

This chapter provides a functional description and circuit analysis of the iSBX-251 Bubble Memory Multimodule I/O board. The functional description includes details on the iSBX-251 board interface to the host iSBC board. A description of data handling on the iSBX-251 board and the method of transferring this data to the host memory location is included. Figure 4-1 shows a block diagram of the iSBX-251 board.

## 4.2 INTERFACE SIGNAL DESCRIPTION

The following paragraphs describe the function and use of the signals that communicate data and commands between the host iSBC board and the iSBX-251 board.

### 4.2.1 iSBX Bus Interface

The iSBX bus interface is grouped into six functional classes:

1. Control Lines
2. Address and Chip Select Lines
3. Data Lines
4. Interrupt Lines
5. Option Lines
6. Power Lines

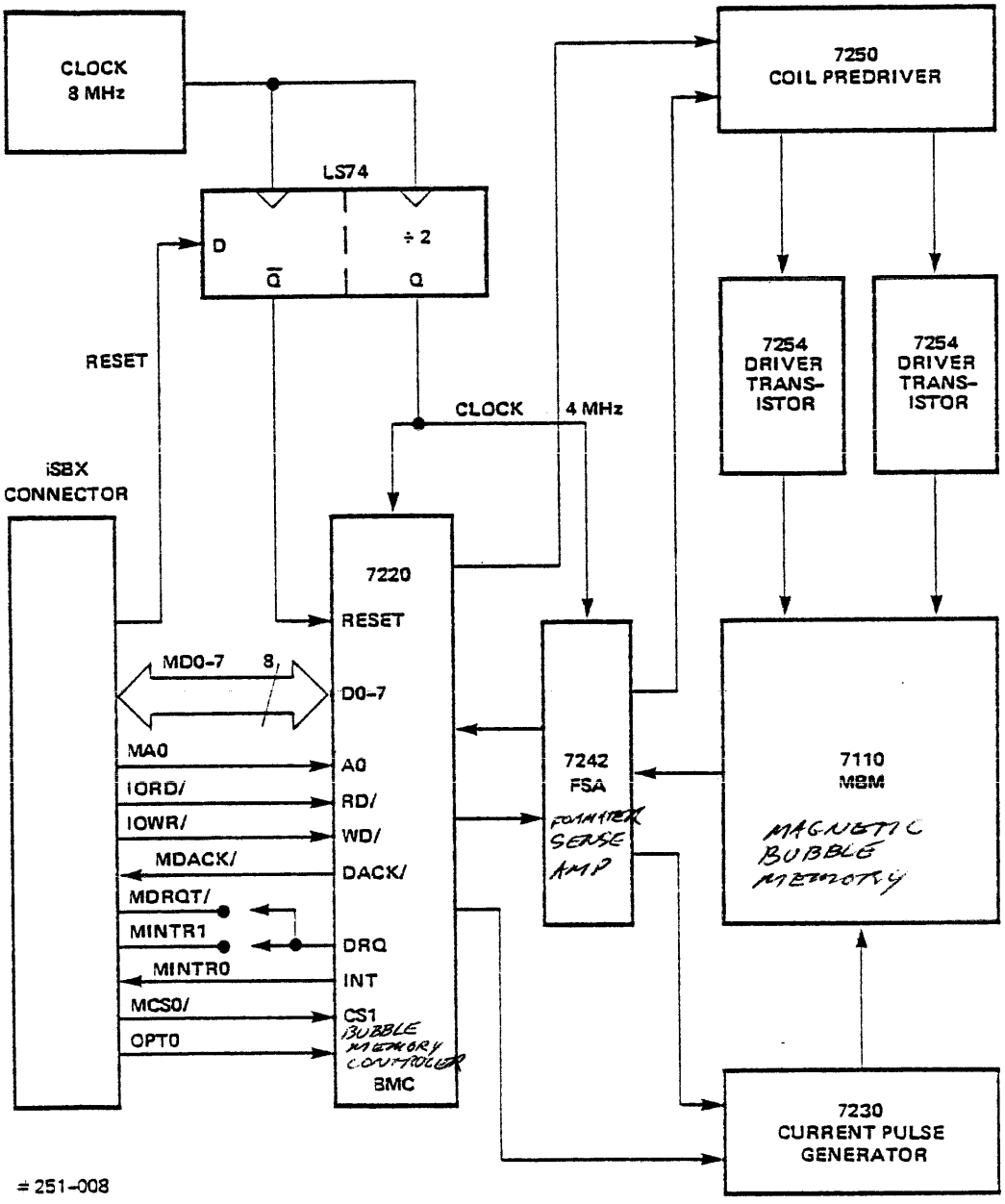



Figure 4-1. Block Diagram of iSBX-251 Board

### 1. Control Lines

The Control Lines provide a communication path between the iSBC host board and the iSBX-251. This communication link is broken down into four unique functions. These functions, Command Lines, DMA Control, Initialize, and System Control, are listed and described in the following text.

### 2. Command Lines

The Command Lines (IORD/, IOWRT/) are active low signals that provide the communications link between the base board and the iSBX-251 board. An active command line, conditioned by Chip Select (MCS0/), indicates to the iSBX-251 board that the address lines are valid and the board should perform the specified operations.

### 3. DMA Lines

The DMA lines (MDRQT, MDACK/) are the communication link between the DMA controller device on the host board and the iSBX-251 board. MDRQT is an active high output signal from the iSBX-251 board to the DMA device on the host iSBC board, requesting a DMA cycle. MDACK/ is an active low input signal to the iSBX-251 board from the DMA device on the host board, acknowledging that the requested DMA cycle has been granted. One byte of data is transferred between the iSBX-251 board and the host board for each DMA cycle.

### 4. Initialize Line

The Initialize Line (RESET) sent to the iSBX-251 board is generated by the base board to put the iSBX-251 board in a known state.

### 5. System Control Line

The System Control Line (MPST/) is an output signal from the iSBX-251 board to the base board. The signal, identified as Multimodule Board Present, is an active low signal and indicates to the base board I/O decode logic that an iSBX-251 board is installed. The MPST/ signal is physically grounded on the iSBX-251 board.

### 6. Address And Chip Select Lines

The iSBX connector provides three address lines (MA0, MA1, MA2). However, the iSBX-251 board uses only MA0. The same is true for the Chip Select Lines, two are provided (MCS0/, MCS1/), but only MCS0/ is used by the iSBX-251 board.

The base board decodes I/O addresses and generates the chip selects for the multimodule boards. The base board decodes all but the lower order three address bits in generating all multimodule board chip selects. Thus, a base board would normally reserve two blocks of 8 I/O ports for each iSBX socket provided.

### 7. Address Line

The single address line to the iSBX-251 board, MA0, is used in conjunction with the Chip Select Line to establish the I/O ports being addressed. When data is to be written into or read out of any of the primary registers (CMDR, RAC, or STR) MA0 is set high. When any of the secondary registers (those accessed via the RAC address) are being used, MA0 is set low.

### 8. Chip Select Line

A single chip select line to the iSBX-251 board, MCS0/, is used in conjunction with the address line to establish the I/O port being addressed. This line being active (low) conditions the I/O command signals and thus enables communication with the iSBX-251 board.

### 9. Data Lines

Eight bidirectional data lines (MD0-MD7) are used to transmit or receive information to or from the iSBX ports. A data line is active or set when high. MD0 is the least significant bit.

10. **Interrupt Lines**

The Interrupt Lines (MINTR0, MINTR1) are active high output lines used to make interrupt requests to the host iSBC board. The iSBX-251 board requires only one interrupt line, MINTR0. MINTR0 is used in DRQ Interrupt mode.

11. **Option Lines**

There are two option lines (OPT0, OPT1) provided OPT0 is connected to the D8 pin on the 7220 controller and thus provides an optional parity line. OPT1 is connected to the iSBX-251's on-board oscillator to provide the 8MHz clock signal for testing purposes.

12. **Power Lines**

The iSBX connector provides for the base board to send +5 and ±12 Volts; however, the iSBX-251 board requires only +5 and +12 Volts.

## 4.3 MULTIMODULE I/O COMMAND OPERATIONS

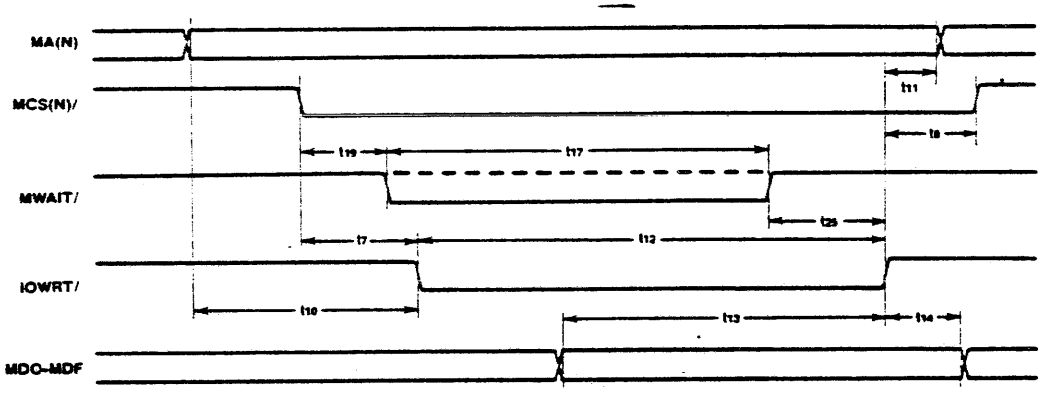
The command lines from the base board are driven by tri-state drivers with pull-up resistors or standard TTL totem pole drivers. These lines indicate to the iSBX-251 board what action is being requested. The following sections will give the timing diagram for iSBX-251 board commands and Figure 4-2 and Table 4-1 give iSBX bus timing. Refer to the Intel iSBX BUS SPECIFICATION, manual order number 142686-001, for further information.

Table 4-1. iSBX Multimodule Board I/O AC Specifications

| Symbol | Parameter | Min (ns) | Max (ns) |
|---|---|---|---|
| $t_1$ | Address stable before read | 50 | – |
| $t_2$ | Address stable after read | 30 | – |
| $t_3$ | Read pulse width | 300 | – |
| $t_4$[2] | Data valid from read | 0 | 250 |
| $t_5$[2] | Data float after read | 10 | 150 |
| $t_6$ | Time between RD and/or WRT | 150 | – |
| $t_7$ | CS stable before CMD | 25 | – |
| $t_8$ | CS stable after CMD | 30 | – |
| $t_9$ | Power up reset pulse width | 50 msec | – |
| $t_{10}$ | Address stable before WRT | 50 | – |
| $t_{11}$ | Address stable after WRT | 30 | – |
| $t_{12}$[2] | Write pulse width | 300 | – |
| $t_{13}$[2] | Data valid to write | 250 | – |
| $t_{14}$ | Data valid after write | 30 | – |
| $t_{15}$[3] | MCLK cycle | | |
| $t_{16}$[3] | MCLK width | | |
| $t_{17}$[1,3] | MWAIT/ pulse width | | |
| $t_{18}$ | Reset pulse width | 10 msec | – |
| $t_{19}$[3] | MCS/ to MWAIT/ valid | | |
| $t_{20}$ | DACK set up to I/O CMD | 100 | – |
| $t_{21}$ | DACK hold | 30 | – |
| $t_{22}$ | CMD to DMA RQT removed to end of DMA cycle | – | 200 |
| $t_{23}$[3] | TDMA pulse width | | |
| $t_{24}$[1,3] | MWAIT/ to valid read data | | |
| $t_{25}$[1,3] | MWAIT/ to WRT CMD | | |

NOTES:

1. Required only if wait is activated.
2. If MWAIT/ not activated.
3. Not used on iSBX-251

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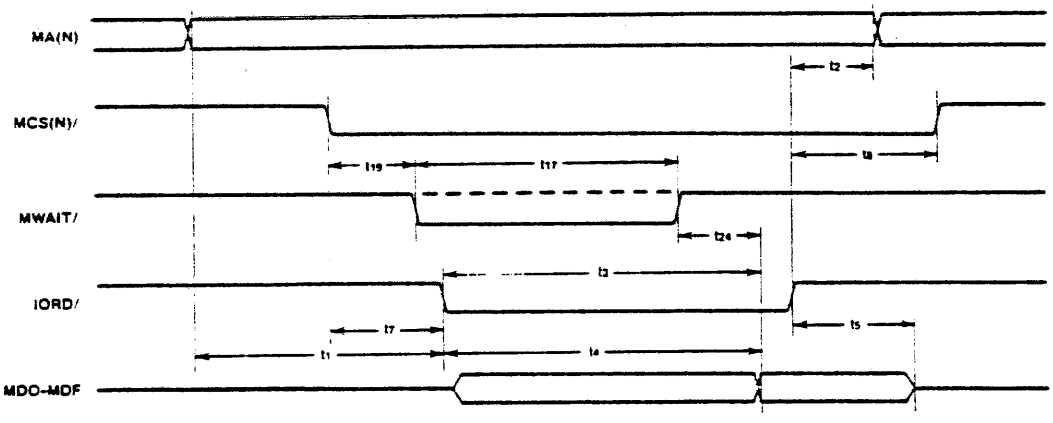
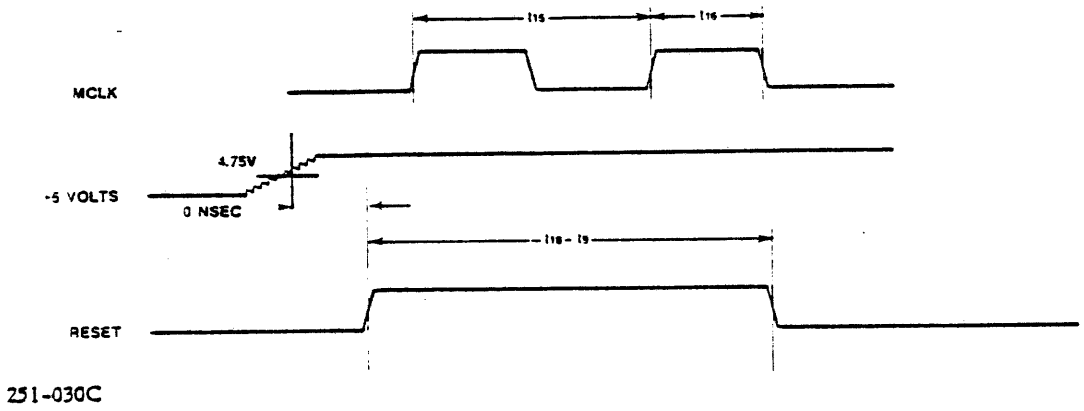
iSBX Multimodule Board Write Timing



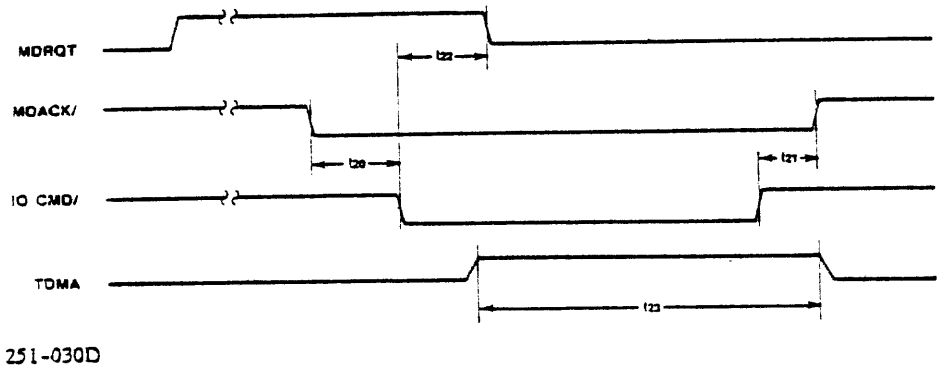

251-030B

iSBX Multimodule Board Read Timing

Figure 4-2. iSBX Bus Timing




iSBX Multimodule Board Reset Timing




iSBX Multimodule Board DMA Timing

Figure 4-2. iSBX Bus Timing (Continued)

### 4.3.1 I/O Read

The I/O Read command timing is shown in Figure 4-3 and Table 4-2. The base board generates a valid I/O address and chip select for the iSBX-251 board. In the performance of an I/O read operation, the host iSBC board can address either the Status Register or indirectly, the Utility Register, Address Register LSB, Address Register MSB, or FIFO Data Buffer. To address the Status Register, the host iSBC board sets MA0 high; to address the remaining registers (assuming the RAC was previously set up), MA0 is set low. The iSBX-251 board must put valid data on the data bus (MD0-MD7) within 250 ns. The host iSBC board reads the data and removes the read command, address, and chip select.

**Table 4-2. I/O Read Timing**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{AC}$ | Select Setup to RD L | 0 | | ns |
| $t_{CA}$ | Select Hold from RD L | 0 | | ns |
| $t_{RR}$ | RD L Pulse Width | 200 | | ns |
| $t_{AD}$ | Data Delay from Address | | 150 | ns |
| $t_{RD}$ | Data Delay from RD L | | 150 | ns |
| $t_{DF}$ | Output Float Delay | 10 | 100 | ns |
| $t_{DC}$ | DACK Setup to RD L | 0 | | ns |
| $t_{CD}$ | DACK Hold from RD L | 0 | | ns |
| $t_{KD}$ | Data Delay from DACK L | | 150 | ns |
| $t_{CYCR}$ | "Read" Cycle Time | (DMA Mode) $4t_p-t_0$ | | ns |

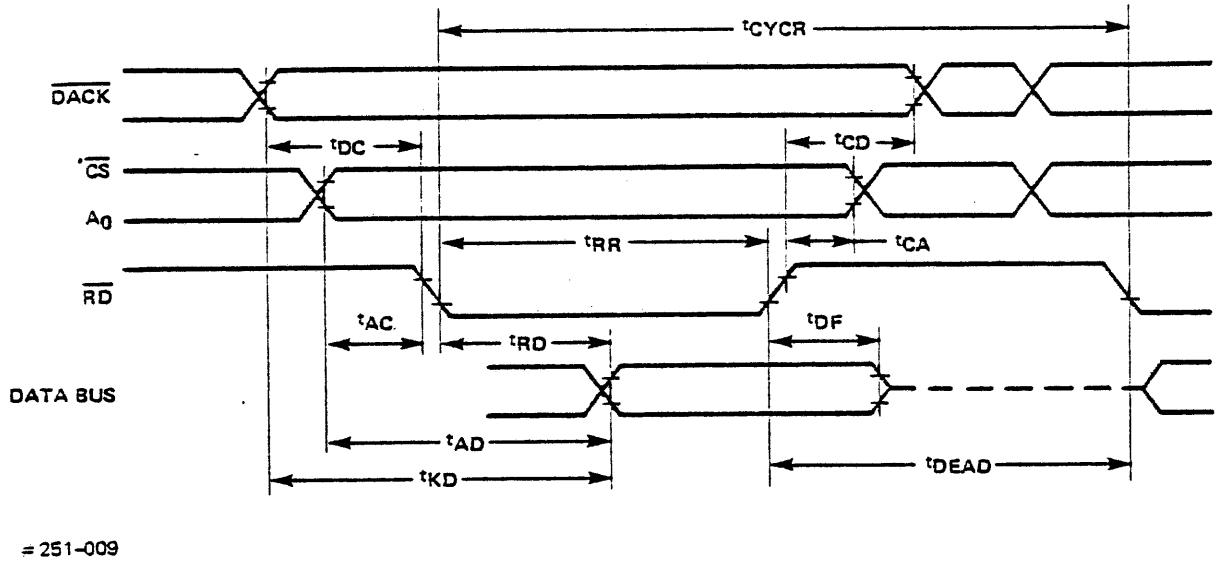



Figure 4-3. I/O Read Timing

### 4.3.2 I/O Write

The I/O Write command timing is shown in Figure 4-4 and Table 4-3. The host iSBC board generates a valid I/O address and chip select for the iSBX-251 board. In the performance of an I/O write operation, the iSBC board can address the Command Register, Register Address Counter, or any of the secondary registers (assuming the RAC would have been previously set up). To address the Command Register or the Register Address, MA0 must be set high. To address any of the secondary registers, MA0 must be set low. After the set up timings are met, the base board activates the IOWRT/ line. The IOWRT/ line remains active (low) for 300ns and the data is valid for 250ns before IOWRT/ is removed. The host iSBC board then removes the data address and chip select signals.

Table 4-3. I/O Write Timing

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{AC}$ | Select Setup to WR L | 0 | | ns |
| $t_{CA}$ | Select Hold from WR L | 0 | | ns |
| $t_{WW}$ | WR L Pulse Width | 200 | | ns |
| $t_{DW}$ | Data Setup to WR L | 200 | | ns |
| $t_{WD}$ | Data Hold from WR L | 0 | | ns |
| $t_{DC}$ | DACK L Setup to WR L | 0 | | ns |
| $t_{CD}$ | DACK L Hold from WR L | 0 | | ns |
| $t_{CYCW}$ | "Write Cycle Time | $4t_p-t_0$ | | |
| $t_{CQ}$ | Request Hold from RD L or WR L (Non-Burst Mode) | | 150 | ns |
| $t_{DEAD}$ | Inactive Time between RD L and WR L | 150 | | ns |

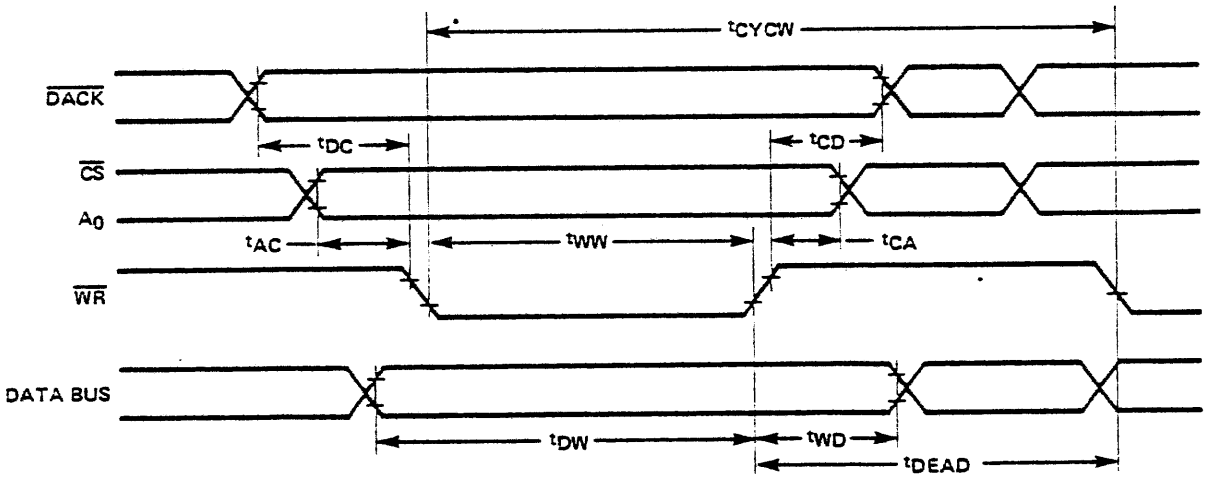



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Figure 4-4. I/O Write Timing

### 4.3.3 Direct Memory Access (DMA)

The iSBX-251 board can be wired to operate in DMA or non-DMA mode. When the base board is equipped with a DMA controller, the iSBX bus will support DMA operation, permitting the host board processor to perform other tasks while data is being transferred. The following timing example shows the interface lines in their operational sequence. The DMA cycle is illustrated in Figure 4-5.

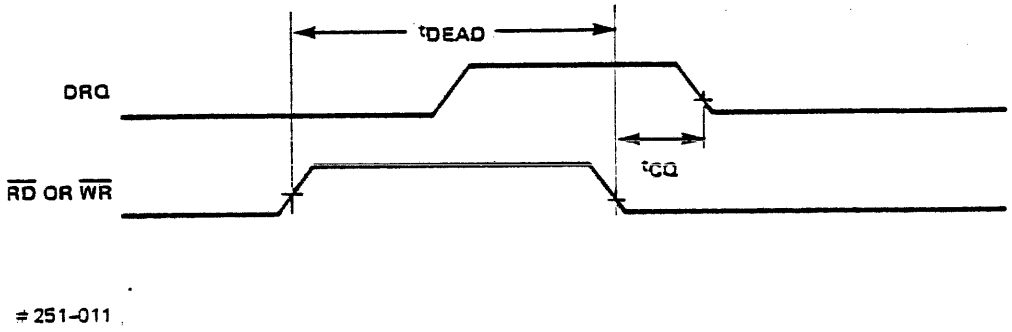



Figure 4-5. DMA Read Timing

A DMA cycle is initiated when the iSBX-251 board activates MDREQ to the DMA controller on the base board. Once the DMA controller gains control of the iSBX bus, it acknowledges back to the iSBX-251 board with MDACK/. The DMA controller then activates an I/O Read, and iSBX-251 board puts valid data on the data bus (MD0-MD7) within 250ns from the leading edge of IORD/. The DMA controller then activates MEM WRITE/ to load the Read data into the host iSBC board memory. The MDACK/ signal acts as a chip select and address to the Multimodule board (the MCS and MA0-MA1 signals are undetermined as they are driven by the memory address). The iSBX-251 board removes the MDRQT during the cycle to stop the DMA cycle. Once the read operation is complete, the DMA controller deactivates the read command providing a data hold time. If the DMA request signal was removed, the DMA controller will release the iSBX bus to the host processor and remove MDACK/. If the request is not removed, the DMA controller will proceed to another DMA cycle.

## 4.4 BOARD CIRCUIT DESCRIPTION

The iSBX-251 Bubble Memory Controller board provides complete interfacing between the 7110 Magnetic Bubble Memory chip and the iSBC host board. The following paragraphs present a functional description of the circuits resident on the iSBX-251 board. Block diagrams of the chips are given only when they help clarify operation of the iSBX-251 board. The internal operation of the chips is very complex and is not covered here. The chip data sheets provide a detailed description of how each chip operates.

### 4.4.1 Clock Circuit

The clock circuit consists of U2 and Y1. The 8 MHz signal from Y1 is divided by U2 to produce the 4MHz clock signal, which is routed to the 7220 BMC and the 7242 FSA. This circuit sets up the main timing for the iSBX-251 board.

### 4.4.2 7220 BMC Chip

The internal block diagram of the 7220 Bubble Memory Controller chip (U2) is shown in Figure 4-6. The 7220 provides all the control and timing functions needed to operate the Intel 7110 MBM and its immediate support circuitry. The 7220 provides a MULTIBUS compatible user interface and also provides suitable interfaces to the remaining support circuits that are described later.

1. Serial Data Bus

   The iSBX-251 board contains a serial data bus that connects the 7220 BMC and the 7242 FSA. The 7220 uses this bus to communicate with the 7242. The 7242 is controlled by 16 commands that are discussed later in this chapter. The bus consists of the following signal lines:

   U1-22 DI0
   U1-23 SYNC/
   U1-24 SHIFT CLK/
   U1-29 C/D/

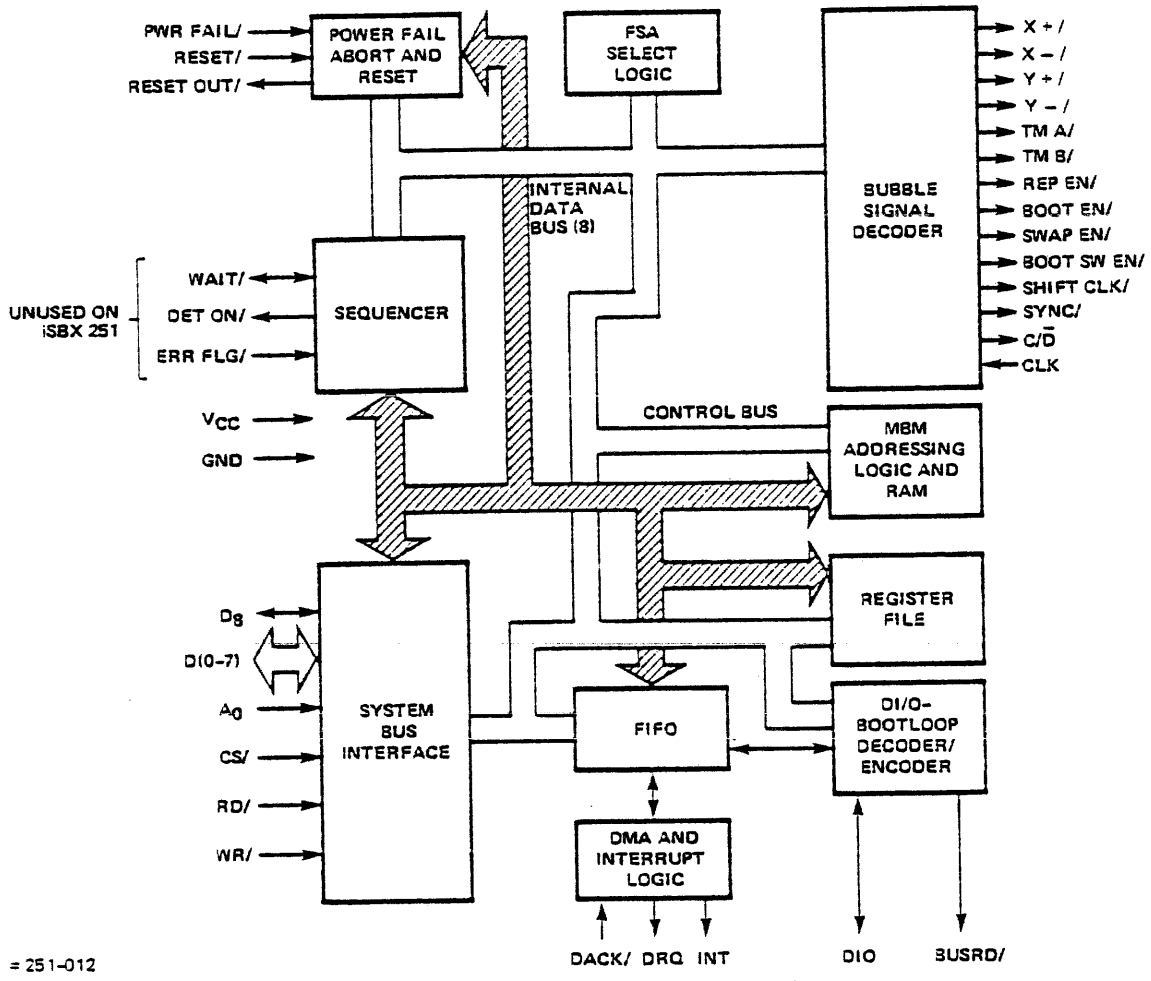



Figure 4-6. 7220 BMC Block Diagram

2. Control Lines

The 7220 provides 10 signal lines for enabling various MBM control functions. These signal lines are logically grouped below:

| | |
|---|---|
| X+/, X-/, Y+/, Y-/ | These lines are used to create coil driver current via the 7250 Coil Pre-Driver. These signals are present on pins U1-39,38,37,36 respectively. |
| SWAP EN/, REP EN/, BOOT SW EN/, BOOT EN/ | These lines enable Bubble control via the 7230 Current Pulse Generator. These signals are present on pin U1-31,33,30,32 respectively. |
| TM A/, TM B/ | These lines are timing signals used to determine CUT and TRANSFER pulse widths respectively within the 7230 Current Pulse Generator. These signals are present on pins U1-35 and 34 respectively. |

### 4.4.3 7230 Current Pulse Generator

The 7230 CPG (U4) converts digital timing pulses to analog current pulses to drive the MBM. It controls the writing of data onto the MBM and the selection of the loop within the MBM into which data is written. For a more detailed discussion of the 7230, refer to the 7230 data sheet.

### 4.4.4 7242 Dual Formatter/Sense Amplifier

The 7242 FSA (U8) is the internal controller of the iSBX-251 board. It is controlled by the 7220 and contains its own command set for communicating with the BMC. The 7242 provides for automatically handling the bubble memories redundant loops so the loops appear transparent to the user and also provides for automatic burst error detection and correction. The 7242 provides the following functions:

| | |
|---|---|
| Serial Communincations | - This block handles all transfers on the serial bus and is shared by both channels of the FSA. |

**Command Decoder** - The 7242 contains a set of 16 commands to control its internal logic and the 7230. The Command Decoder interprets the commands and sets the appropriate command and enable lines. It maintains the FSA status and generates various reset lines.

**Internal Data Bus** - This is the main data link between the Serial communications block and all other data sources in each half of the FSA.

**I/O Latches, Flags, and Bus Control** - These blocks insure that data transfers within the FSA occur at the appropriate times and under controlled conditions.

**FIFO** - The FIFO is used to store data passing to and from the MBM module. It is logically 272 bits long in the "no error correction" mode and 270 bits in the "error correction" mode. A maximum block length of 320 bits (40 bytes) may be used.

**Bootstrap Loop Register** - This register is 160 bits long. It contains information detailing the location of bad loops in the MBM module. This data enables bubble I/O to ensure that data is not loaded into or written from the FIFO into bad loops. A logic zero is written into bad loops.

**Bubble I/O and Enables** - These blocks are user in controlling the 7230, 7250, and the MBM. For further information on the operation of these blocks, see the 7242 data sheet.

Error Correction Logic - When enabled, this block can correct any single burst error less than or equal to 5 bits anywhere in the 270-bit data steam, including the 14-bit error correction code. The FSA must be operated in a buffered mode (for example, an entire block is read prior to passing any data to the Controller) before error correction can be used.

### 4.4.5 7250 Coil Pre-Driver and 7254 Quad VMOS Drive Transistors

These packages (U4, U5, and U6 respectively) contain all the logic necessary to completely drive the coils within the MBM module. The appropriate data sheets should be consulted for a complete description of each package.

### 4.4.6 7110 Magnetic Bubble Memory Module

The 7110 MBM (U7) provides 1,048,576 bits of non-volatile solid-state data storage. It is organized as 2048 512-bit pages and is controlled by the circuits described above. Since the MBM is completely transparent to the user, its operation is not covered here. The user is referred to the 7110 MBM data sheet and support literature for a complete description of the chip.

# SECTION 5

# MAINTENANCE

## 5.1 INTRODUCTION

This section describes required test equipment and provides preventive maintenance procedures, troubleshooting procedures, a procedure for checking the power supplies, and service repair assistance information.

## 5.2 REQUIRED TEST EQUIPMENT

1. Digital multimeter: 0 to +15VDC ±0.001%, 0 to 10K Ohm ±3%.
2. Oscilloscope: 0 to 15MHz.

## 5.3 PREVENTIVE MAINTENANCE

The following is a list of the preventive maintenance activities that should be routinely performed to ensure satisfactory operation of the iSBX-251.

Table 5-1. Preventive Maintenance Schedule

| CHECK | FREQUENCY | ACTION |
|---|---|---|
| System power supply voltages | Every 90 days | Adjust the system power supply voltages to comply with the values specified in Section 2.5. |
| Air filters for system cooling | Every two to four weeks. | Clean as necessary. |

## 5.4 TROUBLESHOOTING PROCEDURES

If a problem arises, the following general procedure should be performed:

1. Check the power supplies and make sure they comply with the specifications given in Section 2.5.

2. Make sure the board is properly seated in the chassis.

3. Look for obvious causes of failure, such as faulty connectors, loose wires, and so forth.

4. Check the inputs to the board. The I/O connections are listed in Table 2-1. (Check that waveforms and timing are correct).

## 5.5 CHECKING THE POWER SUPPLY

To check the power supply:

1. Verify that the following pins have voltages as shown (all voltages should be referenced to the P1-3 ground):

| | |
|---|---|
| P1-4 | +5VDC $\pm$5% |
| P1-1 | +12VDC $\pm$5% |

2. Verify that the output ripple is less than or equal to the value shown below:

   50mV peak-to-peak (DC to 500KHz).

3. If the supply voltages and/or the output ripple are out of tolerance, correct the condition.

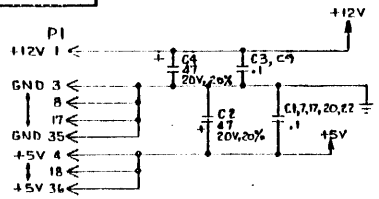
# SECTION 6

# ENGINEERING DRAWINGS

## 6.1 INTRODUCTION

This section contains the schematic, an assembly drawing, and a parts list for the iSBX-251 Multimodule card.

| Drawing Number | Description |
|---|---|
| 162795 | Schematic Diagram for iSBX-251 |
| 162793 | Assembly Drawing and Parts List for iSBX-251 |
| 112975 | Subassembly Drawing and Parts List for iSBX-251 |




ASSEMBLIES USING THIS SCHEMATIC
112975-001

POWER & GROUND LOCATOR CHART

| REFERENCE DESIGNATOR | DEVICE TYPE | POWER PINS GROUND | +5V | +12V |
|---|---|---|---|---|
| U1 | 7220 | 20 | 40 | — |
| U4 | 7250 | 8 | — | 16 |
| U3 | 7230 | 11,12 | 22 | 1 |
| U8 | 7242 | 10 | 20 | — |
| U5,6 | 7254 | 2,9 | — | 6,13 |
| U2 | 74LS74 | 7 | 14 | — |
| U7 | 7110 | — | — | — |
| U9 | 74LS38 | 7 | 14 | — |
| U10 | 75463 | 4 | 8 | — |

DWG NO. 162795 SH 1 REV A

REVISIONS

| ZONE | REV | DESCRIPTION | DFT | CHK | DATE | APPROVED |
|---|---|---|---|---|---|---|
| | 5 | History | | | | |
| | A | DRF 6-22 | | | | |
| | B | DRF 9-13 | | | | |
| | B | ECO 13099 | | | | |
| | C | PER ECO 13200 | | | | |
| | D | PER ECO 13172 | | | | |
| | E | PER ECO 13387 | | | | |
| | F | PER ECO 13391 | | | | |
| | F | ECO 13407 | | | | |
| | G | ECO 12-73507 | | | | |

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES ARE IN OHMS, 1/4 W, ± 5%
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS, +80%, -20%, 50V.

SPARE GATES

| TYPE | REF DES | QTY |
|---|---|---|
| | | |

REF DESIGNATOR

| LAST USED | NOT USED |
|---|---|
| CR2 | |
| W4 | |
| P1 | |
| Y1 | |
| U10 | |
| R17 | |
| CJ | |
| C28 | |
| R15 | |

| | |
|---|---|
| 1134.32 | 158×251C |
| 162773 | 158X 251 |
| NEXT ASSY | USED ON |

QUANTITY PER DASH NO.

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES:
ANGLES ± 2°
XX ± .030
XXX ± .010
SURFACE FINISH 32

| ITEM NO. | PART NUMBER | DESCRIPTION |
|---|---|---|

PARTS LIST

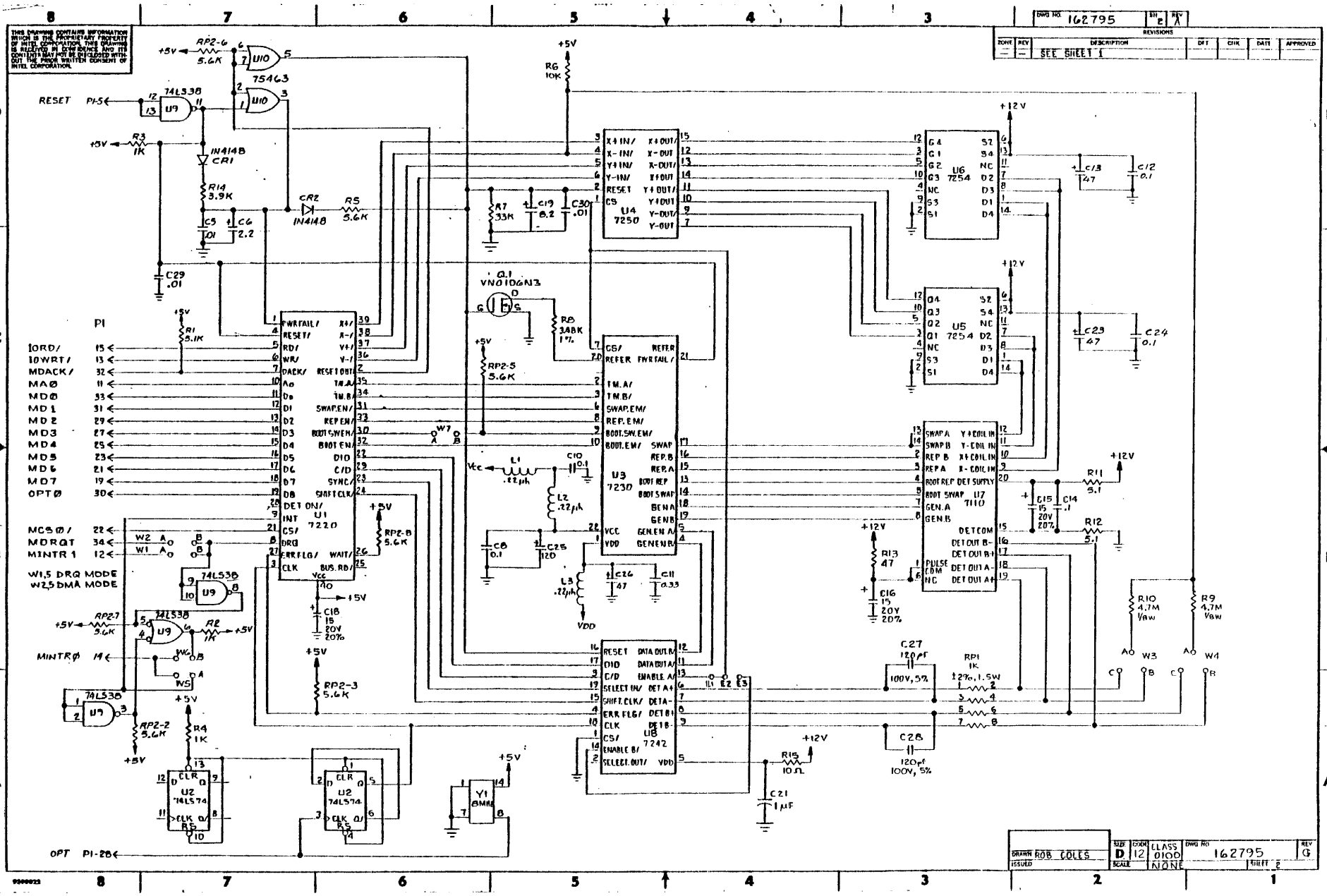
| SIGNATURE | DATE |
|---|---|
| DRN BY ROB COLES | 1-21-81 |
| CHK BY L. Abbott | 9/1/81 |
| ENGR APVD P.R. Miller | 9/1/81 |
| APVD V.P. | 9/1/81 |
| APVD | |

intel® 3065 BOWERS AVE. SANTA CLARA CALIF. 95051

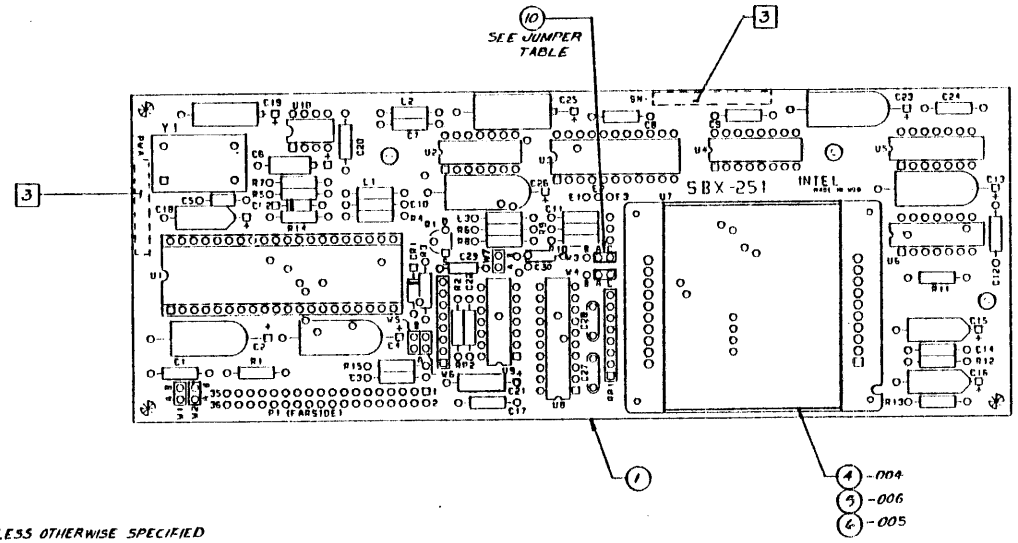
TITLE: SCHEMATIC, BUBBLE MEMORY

| SIZE | CODE | CLASS | DWG NO. | REV |
|---|---|---|---|---|
| D | 12 | 0100 | 162795 | G |

SCALE NONE SHEET 1 OF 2


DWG NO. 162795
REVISIONS
SEE SHEET 1
RESET
74LS38
75463
IN4148
CR1
CR2
RP2-6
RP2-5
RP2-3
RP2-2
RP2-7
RP2-8
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
RP1
C5
C6
C8
C10
C11
C12
C13
C14
C15
C16
C18
C19
C21
C23
C24
C25
C26
C27
C28
C29
C30
L1
L2
L3
Q1
VN0106N3
U1
7220
U2
74LS74
U3
7230
U4
7250
U5
7254
U6
7254
U7
7110
U8
7242
Y1
8MHz
PI
IORD/
IOWRT/
MDACK/
MA0
MD0
MD1
MD2
MD3
MD4
MD5
MD6
MD7
OPT0
MCS0/
MDRQT
MINTR1
MINTR0
W1,5 DRQ MODE
W2,5 DMA MODE
OPT
PI-28
+5V
+12V
VDD
Vcc
DRAWN ROB COLES
ISSUED
SIZE D
CODE 12
CLASS 0100
SCALE NONE
DWG NO 162795
REV G
SHEET 2

| REVISIONS | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| REV | DESCRIPTION | DFT | DATE | CHK | DATE | APVD | DATE |
| E | PER ECO # 13380 | JM | 5/4/81 | NES | 5/6/81 | NES | 5/6/81 |
| F | PER ECO # 13397 | JM | 5/11/81 | NES | 5/12/81 | NES | 5/12/81 |
| F | ECO 13408 | JL | 5/14/81 | JM | 5/15/81 | JMP | 5/15/81 |
| G | ECO 12-13906 | JL | 10/19/81 | JM | 10/19/81 | JMP | 10/19/81 |
| H | ECO 12-13949 | JL | 11/19/81 | JM | 11/19/81 | JMP | 11/19/81 |




| JUMPER TABLE | | | | | | |
|---|---|---|---|---|---|---|
| DASH NO | W2 | W3 | W4 | W5 | W6 | W7 |
| 004 | A-B | – | – | A-B | – | – |
| 005 | A-B | A-C | A-C | A-B | – | – |
| 006 | A-B | A-B | A-B | A-B | – | – |

NOTES : UNLESS OTHERWISE SPECIFIED

1. ASSEMBLY PART NO IS 162793-004/006.
   THIS DOCUMENT AND PARTS LIST ARE TRACKING DOCUMENTS
2. WORKMANSHIP PER 99-0007-001
3. MARK ASSY NO, ASSY DASH NO, AND SERIAL NO WITH CONTRASTING PERM. COLOR, NON-CONDUCTIVE APPROX. WHERE SHOWN

-004/006

QUANTITY PER DASH NO

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES
2. BREAK ALL SHARP EDGES
3. DO NOT SCALE DRAWING
4. TOLERANCES: ANGLES ±, XX ±, XXX ±

| ITEM NO | DESCRIPTION |
|---|---|
| | PARTS LIST |

| SIGNATURE | | DATE |
|---|---|---|
| DRN BY | | 5/4/81 |
| CHK BY | M Patterson | 5/6/81 |
| ENGR APVD | M Patterson | 5/6/81 |
| APVD | | |
| APVD | | |

intel®
3065 POWERS AVE
SANTA CLARA
CALIF. 95051

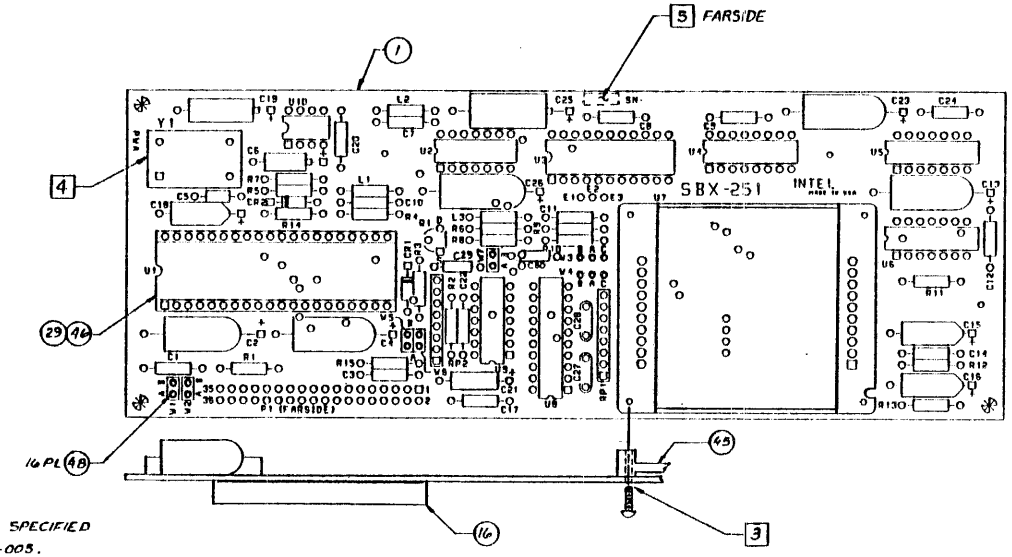
TITLE: PWA
BUBBLE MEMORY SBX-251

| SIZE | DELC | CL CODE | REV LVL | DOCUMENT NUMBER | REV |
|---|---|---|---|---|---|
| D | 12 | 0501 | P | 162793 | H |

SCALE 2/1 SHEET 1 OF 1

REVISIONS

| REV | DESCRIPTION | DFT | DATE | CHK | DATE | APVD | DATE |
|---|---|---|---|---|---|---|---|
| D | PER ECO # 13389 | JH | 5/4/82 | MFS | 5/4/82 | MFS | 5/4/82 |
| E | PER ECO 13397 | JH | 5/4/82 | MFS | 5/6/82 | MFS | 5/6/82 |
| E* | ECO 13408 | JH | 5/5/82 | JH | 5/6/82 | JH | 5/6/82 |
| F | ECO 12-13507 | VCL | 9/6/82 | JH | 9/7/82 | JH | 9/7/82 |
| G | ECO 12-13949 | VCL | 11/4/82 | JH | 11/5/82 | JH | 11/5/82 |




NOTES: UNLESS OTHERWISE SPECIFIED

1 SUB-ASSY NO. IS 112975-005.
THIS DOCUMENT AND PARTS LIST ARE TRACKING DOCUMENTS

2 WORKMANSHIP PER 99-0007-001

[3] SCREWS SUPPLIED WITH SOCKET (ITEM 45).

[4] CRYSTAL Y1 MUST SIT A MIN OF .02 IN OFF BOARD.

[5] MARK SUB-ASSY DASH NO WITH CONTRASTING PERM. COLOR, NON-CONDUCTIVE APPROX WHERE SHOWN.

-005

QUANTITY PER DASH NO.

ITEM NO | DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED
1. DIMENSIONS ARE IN INCHES
2. BREAK ALL SHARP EDGES
3. DO NOT SCALE DRAWING.
4. TOLERANCES:
ANGLES ±
XX ±
XXX ±

| SIGNATURE | DATE |
|---|---|
| DRN BY [illegible] | 5/4/82 |
| CHK BY M. Pettis | 5/6/82 |
| ENGR APVD M. Pettis | 5/6/82 |
| APVD | |
| APVD | |

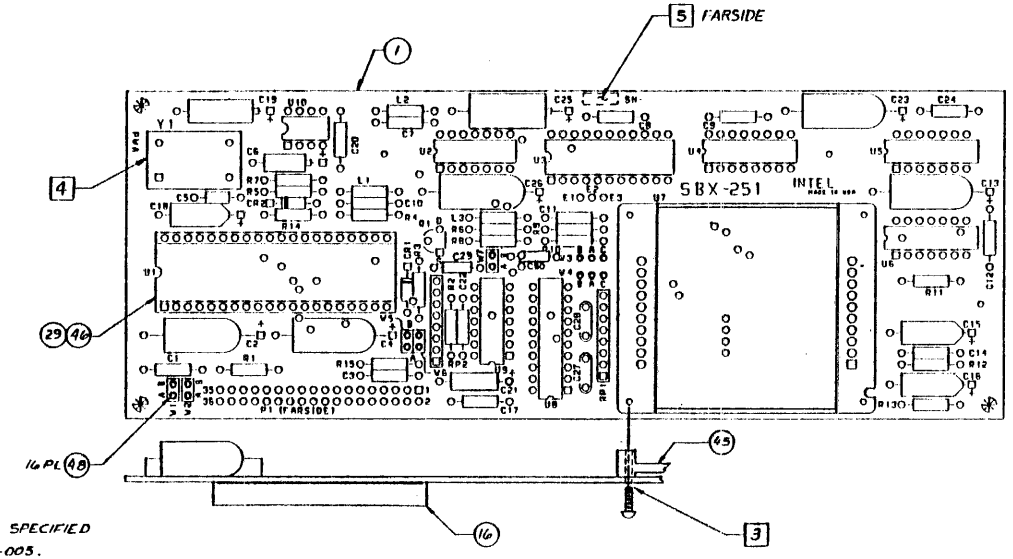
intel® 3065 POWERS AVE SANTA CLARA CALIF 95051

TITLE PWSA
BUBBLE MEMORY, SBX-251

| SIZE | DCLC | I.D. CODE | RELEASE LVL | TECHNICAL NUMBER | REV |
|---|---|---|---|---|---|
| D | 12 | 05001 | P | 112975 | G |

SCALE 2/1 SHEET 1 OF 1

| REVISIONS | | | | | | | |
|---|---|---|---|---|---|---|---|
| REV | DESCRIPTION | DFT | DATE | CHK | DATE | APVD | DATE |
| D | PER ECO # 13389 | JH | 5/4/82 | NFS | 5/6/82 | NFS | 5/6/82 |
| E | PER ECO 13397 | JH | 5/14/82 | NFS | 5/6/82 | NFS | 5/14/82 |
| K | ECO 13608 | JH | 5/14/82 | JH | 5/14/82 | JH | 5/14/82 |
| F | ECO 12-13907 | VCL | 9/16/82 | JH | 9/16/82 | JH | 9/16/82 |
| G | ECO 12-13949 | VCL | 9/16/82 | JH | 9/16/82 | JH | 9/16/82 |




NOTES: UNLESS OTHERWISE SPECIFIED

1 SUB-ASSY NO. IS 112975-005.
THIS DOCUMENT AND PARTS LIST ARE TRACKING DOCUMENTS

2 WORKMANSHIP PER 99-0007-001

3 SCREWS SUPPLIED WITH SOCKET (ITEM 45).

4 CRYSTAL Y1 MUST SIT A MIN OF .02 IN OFF BOARD.

5 MARK SUB-ASSY DASH NO WITH CONTRASTING PERM. COLOR, NON-CONDUCTIVE APPROX WHERE SHOWN.

-005

QUANTITY PER DASH NO

UNLESS OTHERWISE SPECIFIED:
1. DIMENSIONS ARE IN INCHES.
2. BREAK ALL SHARP EDGES.
3. DO NOT SCALE DRAWING.
4. TOLERANCES: ANGLES ±, XX ±, XXX ±.

| SIGNATURE | | DATE |
|---|---|---|
| DRN BY | JH | 5/4/82 |
| CHK BY | N Bottelo | 5/6/82 |
| ENGR APVD | N Bottelo | 5/6/82 |
| APVD | | |
| APVD | | |

ITEM NO. | DESCRIPTION
PARTS LIST

intel
3065 POWERS AVE
SANTA CLARA
CALIF. 95051

TITLE: PWSA
BUBBLE MEMORY, SBX-251

| SIZE | DCLC | CL CODE | RLSE LVL | DOCUMENT NUMBER | REV |
|---|---|---|---|---|---|
| D | 12 | 0501 | P | 112975 | G |

SCALE 2/1 | SHEET 1 OF 1

REVISIONS

| REV | DESCRIPTION | DFT | DATE | CHK | DATE | APVD | DATE |
|---|---|---|---|---|---|---|---|
| C | PER DRF 9-13 | J.C. | 9/23/81 | LP | 11/18/81 | LP | 9/23/81 |
| C | E.CO 13089 | DE | 10/21/81 | DE | 10/21/81 | DE | 10/21/81 |
| D | PER ECO # 13200 | DE | 2/2/82 | NES | 2-2-82 | NES | 2-2-82 |
| E | PER ECO# 13389 | DE | 5/4/82 | NES | 5/6/82 | NES | 5/6/82 |
| F | PER ECO# 13397 | DE | 5/4/82 | NES | 5/6/82 | NES | 5/6/82 |
| F | ECO 13608 | DE | 8/12/82 | DE | 8/12/82 | DE | 8/12/82 |
| G | ECO 12-13906 | JC | 11/12/82 | RH | 11/15/82 | RH | 11/15/82 |
| H | ECO 12-13949 | JC | 11/12/82 | RH | 11/15/82 | RH | 11/15/82 |

NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS DOCUMENT AND ASSY DRAWING ARE TRACKING DOCUMENTS.

-004/006

| UNLESS OTHERWISE SPECIFIED: | SIGNATURE | DATE |
|---|---|---|
| DIMENSIONS ARE IN INCHES. | DRN BY J.C. Chan | 9/21 |
| BREAK ALL SHARP EDGES. | CHK BY LP | 9/21 |
| DO NOT SCALE DRAWING. | ENGR APVD LP | 9/82 |
| TOLERANCES: | APVD | |
| ANGLES ± | | |
| XX ± | APVD | |
| XXX ± | | |

intel

3065 BOWERS AVE.
SANTA CLARA
CALIF 95051

TITLE
PRINTED WIRING ASSY
BUBBLE MEMORY

| SIZE | DCLC | CL CODE | RLSE LVL | DOCUMENT NUMBER | REV |
|---|---|---|---|---|---|
| A | 12 | 0501 | P | PL 162793 | H |

SCALE NONE SHEET 1 OF 2

1091 109507

| ITEM NO. | PART NUMBER | DESCRIPTION | REFERENCE DESIGNATION | QUANTITY PER DASH NUMBER | | | | | | UNIT OF MEAS. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 004 | 005 | 006 | | | | |
| 1 | 112975-005 | PWSA iSBX 251 | | 1 | 1 | 1 | | | | EA |
| 2 | 162795 | SCHEMATIC iSBX 251 | | REF | REF | REF | | | | |
| 3 | | | | | | | | | | |
| 4 | 101167-002 | I.C. 7110 MBM, CENTER BIN | U7 | 1 | — | — | | | | EA |
| 5 | 101167-003 | I.C. 7110 MBM, SUPP., S9006 | U7 | — | — | 1 | | | | EA |
| 6 | 101167-004 | I.C. 7110 MBM, ENHANC., S900T | U7 | — | 1 | — | | | | EA |
| 7 | | | | | | | | | | |
| 8 | | | | | | | | | | |
| 9 | | | | | | | | | | |
| 10 | 102480-001 | CONN, HSG, RCPT, 2 PIN | W2, W3, W4, W5 | 2 | 4 | 4 | | | | EA |

intel
3065 BOWERS AVE.
SANTA CLARA
CALIF 95051

PARTS LIST

SIZE A

DOCUMENT NUMBER PL 162793

SHEET NO. 2

REV. H

REVISIONS

| REV | DESCRIPTION | DFT | DATE | CHK | DATE | APVD | DATE |
|---|---|---|---|---|---|---|---|
| C | PER ECO # 13200 | [illegible] | 2/2/82 | NES | 2-2-82 | NES | 2-2-82 |
| D | PER ECO # 13389 | [illegible] | 5/4 | NES | 5/6/82 | NES | 5/6/82 |
| E | PER ECO # 13397 | [illegible] | 5/4 | NES | 5/6/82 | NES | 5/6/82 |
| E | ECO 13608 | DE | 5/12/82 | DE | 8/12/82 | DE | 8/12/82 |
| F | ECO 12-13907 | Vc | 11/15/82 | [illegible] | 11/15/82 | [illegible] | 11/15/82 |
| G | ECO 12-13949 | Vc | 11/15/82 | [illegible] | 11/15/82 | [illegible] | 11/15/82 |

NOTES: UNLESS OTHERWISE SPECIFIED

1. THIS PARTS LIST & SUB-ASSY DRAWING ARE TRACKING DOCUMENTS.

-005

| 113432 | iSBX-251C |
|---|---|
| 162793 | iSBX-251 |
| NEXT ASSY | USED ON |

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES.
BREAK ALL SHARP EDGES.
DO NOT SCALE DRAWING.
TOLERANCES:
ANGLES ±
XX ±
XXX ±

| | SIGNATURE | DATE |
|---|---|---|
| DRN BY | [signature] | 2/2/82 |
| CHK BY | [signature] | 2/2/82 |
| ENGR APVD | [signature] | 2/2/82 |
| APVD | | |
| APVD | | |

intel
3065 BOWERS AVE.
SANTA CLARA
CALIF 95051

TITLE
PWSA
BUBBLE MEMORY- SBX 251

| SIZE | DCLC | CL CODE | RLSE LVL | DOCUMENT NUMBER | REV |
|---|---|---|---|---|---|
| A | 12 | 0501 | L | PL 112975 | G |

SCALE

SHEET 1 OF 4

1091 109507

| ITEM NO. | PART NUMBER | DESCRIPTION | REFERENCE DESIGNATION | QUANTITY PER DASH NUMBER 005 | | | | | | UNIT OF MEAS. |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 162794-006 | PB, BUBBLE MEM-iSBX 251 | | 1 | | | | | | EA |
| 2 | 162795 | SCHEMATIC, BUBBLE MEM | | REF | | | | | | |
| 3 | | | | | | | | | | |
| 4 | | | | | | | | | | |
| 5 | | | | | | | | | | |
| 6 | 101762-049 | CAP, CER, .1μf $^{+80}_{-20}$ %, 50V | C1, C3, C7-C10, C12 C14, C17, C20, C22, C24 | 12 | | | | | | EA |
| 7 | 101762-055 | CAP, CER, .33μf $^{+80}_{-20}$ %, 50V | C11 | 1 | | | | | | |
| 8 | 101762-037 | CAP, CER, .01μf $^{+80}_{-20}$ %, 50V | C5, C29, C30 | 3 | | | | | | |
| 9 | 101762-061 | CAP, CER, 1.0μf $^{+80}_{-20}$ %, 50V | C21 | 1 | | | | | | |
| 10 | 101775-029 | CAP, TANT, 2.2μf ±10%, 20V | C6 | 1 | | | | | | |
| 11 | 101776-039 | CAP, TANT, 15μf ±20%, 20V | C15, C16, C18 | 3 | | | | | | |
| 12 | 101776-045 | CAP, TANT, 47μf ±20%, 20V | C2, C4, C13, C23, C26 | 5 | | | | | | |
| 13 | 101753-035 | CAP, MICA, 120PF ±5%, 100V | C27, C28 | 2 | | | | | | |
| 14 | 101771-050 | CAP, TANT, 120μF ±20%, 10V | C25 | 1 | | | | | | |
| 15 | 101771-036 | CAP, TANT, 120μF ±20% 10V | C19 | 1 | | | | | | |
| 16 | 103109-001 | CONN, 18/36 PIN | P1 | 1 | | | | | | |
| 17 | 101582-001 | CRYSTAL, OSC, 8MHZ | Y1 | 1 | | | | | | |
| 18 | 101350-001 | DIODE, SW IN4148 | CR1, CR2 | 2 | | | | | | |
| 19 | | | | | | | | | | |
| 20 | 101808-003 | INDUCTOR, .22μh | L1-L3 | 3 | | | | | | EA |

| ITEM NO. | PART NUMBER | DESCRIPTION | REFERENCE DESIGNATION | QUANTITY PER DASH NUMBER 005 | | | | | | UNIT OF MEAS. |
|---|---|---|---|---|---|---|---|---|---|---|
| 21 | | | | | | | | | | EA |
| 22 | 102831-004 | IC, 7230, RED DOT | U3 | 1 | | | | | | |
| 23 | 102832-001 | IC 7242 | U8 | 1 | | | | | | |
| 24 | 101168-001 | IC 7250 | U4 | 1 | | | | | | |
| 25 | 100699-031 | IC 74LS38 | U9 | 1 | | | | | | |
| 26 | 101338-001 | IC 7254 | U5, U6 | 2 | | | | | | |
| 27 | 100713-031 | IC 74LS74 | U2 | 1 | | | | | | |
| 28 | 100857-001 | IC 75463 | U10 | 1 | | | | | | |
| 29 | 106899-004 | IC 7220-1 | U1 | 1 | | | | | | |
| 30 | 101655-001 | RES, CARB, 10Ω ±5%, 1/4W | R15 | 1 | | | | | | |
| 31 | 101654-026 | RES, CARB, 4.7M ±5%, 1/8W | R9, R10 | 2 | | | | | | |
| 32 | 101656-036 | RES, CARB, 5.1Ω ±5%, 1/4W | R11, R12 | 2 | | | | | | |
| 33 | 101656-021 | RES, CARB, 47Ω ±5%, 1/4W | R13 | 1 | | | | | | |
| 34 | 101655-003 | RES, CARB, 1K ±5%, 1/4W | R4, R3, R2 | 3 | | | | | | |
| 35 | 101656-031 | RES, CARB, 5.1K ±5%, 1/4W | R1 | 1 | | | | | | |
| 36 | 101656-039 | RES, CARB, 5.6K ±5%, 1/4W | R5 | 1 | | | | | | |
| 37 | 101655-004 | RES, CARB, 10K ±5%, 1/4W | R6 | 1 | | | | | | |
| 38 | 101656-007 | RES, CARB, 3.9K, ±5%, 1/4W | R14 | 1 | | | | | | |
| 39 | 101655-091 | RES, CARB, 33K ±5%, 1/4W | R7 | 1 | | | | | | |
| 40 | 101668-053 | RES, CARB, 3.48K ±1%, 1/4W | R8 | 1 | | | | | | EA |

| ITEM NO. | PART NUMBER | DESCRIPTION | REFERENCE DESIGNATION | QUANTITY PER DASH NUMBER 005 | UNIT OF MEAS. |
|---|---|---|---|---|---|
| 41 | | | | | |
| 42 | 101729-034 | R-PACK, 8PIN, 5.6K | RP2 | 1 | |
| 43 | 101732-023 | R-PACK, 8PIN, 1K ±2%, 1.5W | RP1 | 1 | EA |
| 44 | | | | | |
| 45 | 101569-002 | SOCKET, BUBBLE, 20 PIN | XU7 | 1 | EA |
| 46 | 101552-040 | SOCKET, 40 PIN | XU1 | 1 | EA |
| 47 | | | | | |
| 48 | 102743-001 | TERM, POST .025 SQ x .443 | | 16 | EA |
| 49 | 103919-001 | TRAN VN0106N3 | Q1 | 1 | EA |
| 50 | | | | | |
| 51 | 103431-002 | WASHER, FLAT, NYLON, #2 | | — | EA |
| 52 | 107646-001 | FASTENER, PUSH-ON, MINIATURE | | — | EA |

| | | | | | | |
|---|---|---|---|---|---|---|
| intel 3065 BOWERS AVE. SANTA CLARA CALIF 95051 | PARTS LIST | | SIZE A | DOCUMENT NUMBER PL 112975 | SHEET NO. 4 | REV. G |

109510

# APPENDIX A

## FILING A FREIGHT CLAIM

The following procedures are required to obtain a quick and precise settlement of a freight claim with any carrier.

1. Notify Intel Corporation, Memory Systems Operation, Marketing, of the damage in order to begin claim procedures with Intel's insurance company.

2. List any discrepancies on both consignee's and carrier's copy of the freight bill (such as missing packages, damages to the container, or anything seeming out of the ordinary). Many freight claims are denied because the freight bill is signed off as being clear of any damages. Initial the carrier's copy and have the carrier initial the consignee's copy.

3. If any damage is found:

   a. Save the container.

   b. Hold the damaged articles until an inspection has been made by an authorized agent.

   c. Do not move or transport articles from the immediate area.

   d. Notify the carrier of damage and request an inspection.

   e. Photograph the damage, if possible.

   f. Obtain copies of:

      1) Freight Bill
      2) Invoice
      3) Packing List

4. Inspection will usually be made within several days. The inspector will usually be from an agency which specifically handles inspections for the carrier. The inspector will try to ascertain two points: a) a description and the degree of damage; and b) who was responsible for damage, that is, whether it is shipper's or carrier's negligence. It will also be necessary to have someone present at the time of inspection who is aware of the damages. After the inspection is made, a copy of the report will be given to the consignee. The claim can then be filed with the insurance company.

5. Claim forms can be obtained from the inspector or from the carrier. Upon completion of the claim form, submit the following documents to the carrier for disposition:

   a. Copy of the claim form

   b. Copy of the inspection report

c. Copy of the original invoice

d. Copy of the packing slip

e. Copy of the freight bill

f. Copy of the repair cost estimate

g. Any other information which might be helpful, such as photographs.

NOTE

It is the responsibility of the party which had legal ownership of the freight during transportation to file the claim.

# APPENDIX B

# RETURNED MATERIAL AUTHORIZATION (RMA) PROCEDURE

## B.1 GENERAL INSTRUCTIONS

If failure occurs in any printed circuit module (in warranty, or out of warranty), that module can be returned to Intel for repair.

**CAUTION**

Repair of in-warranty modules by the customer may void the warranty.

## B.2 RETURNED MATERIAL AUTHORIZATION PROCEDURE

Intel offers several repair and replacement plans. To determine which is best suited for your needs call the Intel Hot Line 800-528-0595, 7:00 a.m. to 5:00 p.m. Mountain Standard Time.

A brief description of each plan is provided in paragraphs B.3, B.4, B.5 and B.6.

## B.3 ON-SITE SERVICE

Certain of Intel's Memory Products are designated for on-site maintenance support. Two types of on-site services are available. The preferred type of service is the purchase of an annual maintenance contract for which you will be billed monthly. You are assured of a reasonable field engineer response time, local stock of spares, and unlimited service calls.

The second type of on-site support is per-call. The field engineer will respond on a best efforts basis and local stocking of spares is not assured.

## B.4 BRR (BEFORE RETURN REPLACEMENT)

A replacement part usually ships within 24 hours of a customer's call. This plan provides the quickest response. This plan is for products not supported by the on-site service defined above.

## B.5 DRA (DIRECT RETURN AUTHORIZATION)

A defective board is sent to Intel for repair. Turnaround is targeted for 30 days. This plan is used for economical repair or when return of same part (serial number) is required.

## B.6 RRA (RETURN REPLACEMENT AUTHORIZATION)

Replacement part shipped within 24 hours of receipt of defective part. This plan offers advantages of both quick turnaround and reduced cost of repair. Original part, however, is not returned.